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應用於量子計算之低溫微波電路及量測系統

Cryogenic Microwave Electronics and Measurement Systems for Quantum Computing Applications

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本論文係 陳士允 (姓名) R10942016 （學號）在國立臺灣大學電信工程學研究所完成之碩士學位論文，於民國 113 年 7 月 18 日承下列考試委員審查通過及口試及格，特此證明。

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中文摘要

量子計算被視為是顛覆人類生活與科技的重要技術之一。除了核心的量子元件，其用於控制和讀取量子位元之傳統半導體積體電路也是量子計算系統發展中不可或缺的基石。本論文中，我們將探究射頻/微波技術在數個與量子計算相關的應用。

本論文的第一部分聚焦於設計並實現一應用於固態自旋量子位元讀取系統中之低溫互補式金屬氧化物半導體低雜訊放大器。此次設計提出之創新電路架構，有效緩解在傳統雜訊消除技術中各參數間之拮抗，實現了在增益、雜訊指數、頻寬和功耗方面的綜合性高性能指標。

論文的第二部分則著墨於低溫樣品測量系統之建立，開發、設計與測試樣品量測載板套件，並討論了多種低溫微波量測相關之應用與其所需之考量。為了在低溫環境中進行微波量測與校正，我們規劃並開發了與樣品載板套件相容之校正系統。作為校正系統中的重要元件之一，我們透過提出的系統化設計程序，並應用 LC 梯形低通濾波器理論，實現了一顆低溫寬頻單極四擲（SP4T）切換器。在將此固態切換器與校正量測載板整合後，我們驗證了此校正與量測系統之效能，並顯示其可有效提升在極低溫量測設備中之校正準確度，能為未來相關之量子元件提供更可靠的微波測量環境，加速量子計算領域之發展。

關鍵字： 低溫互補式金屬氧化物半導體低雜訊放大器、低溫射頻切換器、低溫微波量測系統、低溫 *S* 參數校正技術。

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ABSTRACT

Quantum computing has recently become one of the most captivating keywords in the field of science and technology. In addition to the core quantum devices, control and readout circuitries developed based on conventional solid-state and electronic technologies are also indispensable cornerstones in system integration and scaling up. In this thesis, we explored and investigated the application of RF/microwave technologies in several quantum computing-related areas.

The first part of this thesis focuses on a cryo-CMOS low-noise amplifier designed specifically for use in readout circuitries for solid-state spin qubit systems. A novel topology is proposed to alleviate the trade-offs in the noise-canceling technique, achieving a superior figure of merit in terms of gain, noise figure, bandwidth, and power consumption.

In the establishment of a cryogenic measurement system based on a dilution fridge, a prototype of sample holder kits is presented. Various considerations regarding several different applications are discussed. For performing calibration in a cryogenic environment, we designed a calibration system integrated with the sample holder kits. A cryogenic broadband single-pole-four-throw (SP4T) switch is developed with a proposed systematic design procedure utilizing LC-ladder low-pass filter theory. The implemented calibration system, incorporating the solid-state switch, achieves enhanced calibration accuracy within cryogenic microwave measurements, paving the way for advanced research in quantum-computing-relevant microwave devices.

Keywords – Cryo-CMOS low noise amplifiers (LNAs), cryogenic RF switches, cryogenic microwave measurement, cryogenic *S*-parameter calibration.

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Chapter 1 Introduction

Quantum computing is acknowledged as a pivotal technology with the potential to revolutionize numerous fields across human society. Various forms of quantum accelerators are being developed, originating from diverse fields within physics and advancing through engineering innovations. Superconducting qubits have quickly emerged as a forefront platform in quantum computing research, facilitated by their relative ease of fabrication and development in laboratory settings [1]. With the advancement bolstered by collaboration among several prominent research groups and industry partnerships, the technology has achieved a notable milestone in demonstrating quantum supremacy [2]. On the other hand, despite slower development, semiconductor spin qubits are highly regarded as promising candidates due to their seamless integration into mature semiconductor manufacturing processes. With their capacity for miniaturization, scalability, and potential ability to operate at higher temperatures, semiconductor spin qubits have become a robust contender in advancing quantum computing towards practical applications [3].

Apart from the core quantum devices, the control and readout electronics implemented in semiconductor integrated circuits (ICs) are also essential in the development of quantum computing systems. In early laboratory research on quantum devices, experimental setups typically involve bulky commercial measuring instruments at room temperature, located outside the dilution fridge. This arrangement requires complex routing through the cooling stages to the base temperature stage where the device operates. For practical quantum algorithms requiring thousands to millions of qubits, using such extensive general-purpose equipment is impractical. Moreover, these complex systems increase the issues of mismatches, synchronization problems, and other potential errors. To address these challenges, integrating specially designed control and readout

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electronics that operate in the cryogenic environment within the dilution fridge is widely proposed as part of the envisioned architecture for scaling up quantum systems. Several studies in the literature have demonstrated system-on-chips (SoCs) manipulating and acquiring quantum signals from the corresponding qubit platforms [4-7]. The periphery integrated circuitries within the cryogenic system not only reduce complex routing issues during quantum system scaling but also envision potential on-chip integration with core quantum devices. These specially designed circuits, positioned near the quantum device with minimized electrical paths, are beneficial for enabling multiple operations within the limited decoherence time of the qubits. The reduced round-trip time thereby facilitates more complex operations, including error correction schemes, applied to the qubit systems.

Motivated by the development of integrated periphery electronics, the first part of this thesis delves into designing a cryogenic low-noise amplifier (LNA), serving as the initial input block in the readout receiver chain. In laboratory setups involving a few qubit levels, this critical amplifying block facing the quantum device is typically realized using III-V compound semiconductor LNAs (such as InP and GaAs processes) or SiGe HBT LNAs. These technologies are chosen for their superior noise and gain performance compared to bulk CMOS processes. Moreover, advanced experiments are integrating superconducting parametric amplifiers as the first stage of the readout channels, offering noise performance near the quantum limit that significantly surpasses solid-state amplifiers. However, these amplifier electronics, implemented in various technologies, present challenges when integrating with SoC systems typically realized in CMOS processes for digital circuitry. This often requires discrete connectorized packaging of these amplifiers for connection in the readout cable paths from quantum devices to receiver chips. This approach runs counter to the vision of integrating traditional control

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and readout ICs directly with quantum devices to facilitate qubit scaling.

To enhance the performance of low-noise amplifiers in bulk CMOS processes, Chapter 2 introduces a cryo-CMOS low-noise amplifier designed for spin qubit reflectometry readout applications. Reflectometry readout of spin qubits shortens measurement acquisition time by widening the bandwidth of the receiver chain with an up-converted carrier tone. Typically, operational frequencies for reflectometry readout in spin qubits range from hundreds of MHz to a few GHz in the literature. The first part of Chapter 2 discusses topology selection for the frequency band used in spin qubit reflectometry readouts, reviews relevant literature at room temperature, and considers cryogenic design, alongside evaluating reported cryogenic LNAs for spin qubit readouts. Later in this chapter, a novel topology is introduced to alleviate inherent trade-offs in traditional noise-canceling techniques. The proposed LNA is designed and implemented using a 40-nm CMOS process, with detailed derivations of the small-signal and noise responses of the circuits. Despite unresolved issues in noise measurement results at low frequencies, the fabricated circuit demonstrates superior performance at room temperature compared to other reported works in the literature.

The second part of this thesis focuses on another aspect related to quantum device measurements. As part of the initial phase in constructing experimental environments for quantum-related research, alongside cryogenic and vacuum facilities, the second part of the thesis explores the development of electrical and microwave measurement systems at cryogenic temperatures. Chapter 3 introduces a cryogenic broadband single-pole-four-throw (SP4T) RF switch, which serves as an essential element of the refined cryogenic calibration system presented in Chapter 5. The chapter outlines a systematic design procedure for analyzing and synthesizing such a broadband switch. By decomposing the SP4T switch into two low-pass filters connected with the on-resistance of the series transistor in the middle, a three-step design approach is proposed. Utilizing LC-ladder low-pass filter theory allows for precise synthesis of the SP4T switch response tailored to specific applications. Measurements of the implemented circuit are conducted at both room temperature and 4 K. The SP4T switch achieves a broad bandwidth of 67 GHz and high isolation at room temperature, with power leakage reduced to as low as 0.6 μW at 4 K. This ensures operation within the cooling power limits of the dilution fridge's base temperature stage, making it well-suited for integration as the core component of the cryogenic calibration system detailed in Chapter 5.

Chapter 4 discusses various studies and considerations involved in constructing measurement systems for quantum devices. This includes material selection suitable for cryogenic temperatures and the electrical and mechanical design of testing boards for diverse applications. The chapter also emphasizes efforts in designing high-frequency routings and addressing microwave transmission challenges. To improve microwave measurements of quantum devices within the dilution fridge, a straightforward calibration scheme is implemented to de-embed responses contributed by the cryogenic system apart from the device in this initial experiment phase. Despite encountering significant errors within the straightforward calibration scheme, the experiments in this chapter confirm the suitability of selected materials for constructing cryogenic measurement systems.

To improve the cryogenic calibration scheme, the first part of Chapter 5 revises the sample holder design for more practical applications. A multi-board structure is implemented, with various daughterboards designed for specific experiments. This includes a series of sample holders for superconducting device measurements, addressing the box-mode issue and incorporating the necessary magnetic shielding for sensitive samples under test. Later, a refined calibration scheme is proposed, incorporating additional directional couplers and cryogenic amplifiers within the dilution fridge to

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enhance the sensitivity of measurements, accommodating the extremely low input power required for quantum devices. To minimize calibration errors within the system, the proposed scheme includes two on-board solid-state RF switches, replacing the bulky connectorized electromechanical switches commonly used in the literature. The broadband SP4T switch introduced in Chapter 3 is integrated into the calibration and measurement board, which also serves as a daughterboard compatible with the multi-board system. Compared to a set of control groups using the straightforward calibration approach in Chapter 4, the refined calibration scheme in Chapter 5 successfully eliminates fluctuation ripples in the calibrated responses. The experiments in this chapter demonstrate an improved calibration system for microwave measurements of quantum devices, facilitating a more detailed understanding of quantum devices in future research by reducing environmental interference within the measurement setup.

Chapter 2 A Cryo-CMOS LNA for Spin Qubit Reflectometry Readout Applications

2.1 Introduction

2.1.1 Literature Review of CMOS Noise Canceling LNAs in VHF and UHF Bands

The design of a low noise amplifier (LNA) typically involves parameters such as gain, noise figure, input matching, stability, power, and linearity. In particular, the challenge of ensuring broadband low input return loss when interfacing with the RF environment ahead of the receiver chain is a key factor in determining suitable topology candidates. An interesting review of the early histories to the 2010s of broadband LNAs can be found in [8]. Various techniques incorporating passive LC components and transformers are widely explored in the literature [9, 10]. However, the need for functionality at relatively low frequencies around 100 MHz presents difficulties for the matching network. This requires the use of large inductors at the LNA input, which can introduce loss, degrade both gain and noise performance, and necessitate a large footprint.

To achieve the desired broadband return loss starting from dc, in addition to passive LC approaches, three primary topologies are reported to realize input matching by synthesizing the resistive part of the input impedance. Firstly, the common-gate (CG) LNA, which utilizes the intrinsic input impedance from the source of common-gate transistors, is one of the most popular topologies. Secondly, the resistive feedback topology incorporates a shunt resistor with common-source (CS) transistors, enabling input matching by carefully selecting the value of the feedback resistor in conjunction with the amplifier's gain. Finally, the active feedback topology achieves the desired input

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resistance using a source follower in the feedback route of a CS transistor.

Despite realizing the input matching at low frequencies, the three topologies above suffer from various trade-offs between input return loss and other parameters. In the case of CG LNAs, some studies attempt to mitigate the effects on intrinsic input impedance when aiming for better noise figures by incorporating feedback mechanisms to decouple the two parameters [11, 12]. Nevertheless, akin to the resistive-feedback and active-feedback configurations, reducing the noise figure often entails increasing the transconductance of the transistors, leading to higher power consumption. Furthermore, in the pursuit of ultra-low noise characteristics, the continuous increase in transconductance can still impact input matching, often resulting in inadequate noise performance. A more prevalent approach in CG LNA design involves employing feed-forward techniques, wherein the noise figure is significantly improved through the gain-boosting mechanism, thereby easing the design trade-offs with input power matching. However, to mitigate the additional noise contribution from feed-forward circuitries, the approach is usually implemented in a differential configuration with passive components [13, 14].

To explore noise reduction techniques and efforts to decouple input power matching, a noise-canceling concept is proposed in [15]. Leveraging the inherent phase opposition between the signal and noise voltages at the input and output nodes of the main amplifier block, this mechanism integrates an additional gain block parallel to the main amplifier. Through a combining network of the two paths, it theoretically cancels out the channel noise of the main amplifier while concurrently amplifying the signal from both routes. This innovative approach effectively mitigates the dependency of the main amplifier's noise behavior on its transconductance, rendering it independent of input matching considerations. The main amplifier block is commonly constructed using either a CG

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transistor or a resistive-feedback CS transistor to achieve the intended input matching. By incorporating the additional CS gain block, noise-canceling LNAs can be divided into two classifications: CG-CS noise-canceling LNAs and shunt-feedback noise-canceling LNAs.

In the literature, considerable effort has been dedicated to studying the CG-CS noise-canceling topology, primarily due to its potential to function as a single-to-differential balun amplifier [16]. Various enhancements to this topology, such as the gm-boosting technique for the CG cell [17] and the current-reuse technique for power reduction [18], continue to be actively explored, keeping the CG-CS noise-canceling topology a dynamic area of research. Given the stringent linearity requirements in communication systems, much of the research also focuses on improving the behavior of IP2 and IP3 [19, 20]. Nonetheless, this topology necessitates a dc path for the CG transistor at the input port, which mandates either an off-chip inductor or an on-chip current source or inductor. The former complicates measurement and future system integration, while the latter often compromises input-referred noise, thus hindering the potential for achieving ultra-low noise performance. In addition to the CG-CS topology, there are numerous captivating reports of broadband LNAs in differential form that exhibit outstanding performance, with some adopting a noise-canceling approach [21]. However, the necessity for differential signals to achieve proper phase implementation is incompatible with the single-ended receiver used in spin qubit readout reflectometry.

On the other hand, given the need for an inductor-less and single-ended design, the shunt-feedback noise-canceling topology emerges as a preferred choice. Following the early exploration in [15], there have also been several studies exploring the shunt-feedback noise-canceling approach. In [22], a CG gain block is introduced to address the trade-off between gain and bandwidth associated with the feedback resistor value, while

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also improving the output buffer's driving capability through the implementation of a resistive shunt-feedback CS block. Despite the inductorless nature promoted within this topology, some studies also utilize on-chip inductors to mitigate capacitive degradation at higher frequencies, thereby widening the bandwidth and preserving the noise-canceling relationship [23, 24]. Similar to the CG-CS topology, the demand in communication system applications prompts several studies to focus on analyzing and improving linearity, particularly through the utilization of pMOS-nMOS pairs for intermodulation distortion cancellation [25, 26].

Further exploration aimed at improving the trade-off between gain and input matching on the feedback resistor of the main amplifier block reveals a few novel topological approaches. [27] introduces a source follower feedback on the auxiliary CS transistor. This active feedback introduces an additional impedance parallel to the original input matching of the main amplifier block, enabling an adjustment in the feedback resistor while maintaining the desired input impedance. This increased feedback resistor enhances the overall gain, reducing the noise contribution from the auxiliary transistors and consequently lowering the noise figure. However, the noise power generated by the additional feedback source follower transistor limits the low noise potential of this topology, especially under a limited power budget. In a subsequent study detailed in [28], a global resistive feedback is integrated at the combination node of the main and auxiliary paths. This topology effectively introduces a shunt impedance in parallel at the input node, allowing for adjustment of the feedback resistor value previously constrained by the input return loss. In addition to mitigating the trade-off between input matching and gain, the circuitry implements self-forward-body-bias (SFBB) on both pMOS-nMOS pairs of the main and auxiliary amplifier blocks, enhancing the transconductance within the limitations of the supply voltage. Furthermore, the design also emphasizes selecting pMOS-nMOS biasing points and sizes to further reduce higher-order nonlinearities through small signal analysis.

2.1.2 Design Considerations for Cryogenic Operation

The brief review in the previous subsection mainly focuses on the reported works in the literature operating at room temperature. Nonetheless, the targeted application of the proposed LNA in this chapter requires functionality at a cryogenic temperature of around 4 K. Therefore, before delving into the literature review of cryogenic LNAs, it is also important to investigate device characterization in a cryogenic environment.

Since the research of interest primarily focuses on analog and radio-frequency circuits, only specific aspects of cryogenic characterization will be discussed. Within this scope, [29] provides an impressive review of the related fields. For standard bulk CMOS processes, [30] and [31] report and analyze dc and analog-design parameters across several technology nodes with different channel lengths. Generally, the threshold voltage of the devices increases due to carrier freeze-out caused by the increased ionization energy. Nevertheless, carrier mobility increases due to the reduction in phonon scattering, resulting in higher drain current and transconductance in strong saturation. However, this enhancement in effective channel mobility is limited by ballistic transport restrictions in short-channel devices, reducing the extent of the improvement. More pertinent to digital circuits, the steeper subthreshold slope reduces leakage current and enhances switching speed. Alongside the high driving current, this feature is advantageous for efficient digital logic implementation. It's worth mentioning that some non-idealities observed in long-channel devices, such as the kink effect and the resulting hysteresis in current sweeping, are mitigated with advanced short-channel devices. For analog circuits, the Gm/Id ratio and intrinsic gain of transistors are often of interest. The Gm/Id ratio improves in the weak inversion region, though a slight reduction is observed in the strong inversion region.

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This feature suggests improved power efficiency for analog circuits biased in the weak inversion region. At the same gate voltage in the strong inversion region, transistors exhibit nearly constant output conductance with varying temperature, and the increased transconductance at cryogenic temperatures results in improved intrinsic gain. Interestingly, under a constant overdrive voltage, a lower intrinsic gain is reported at cryogenic temperatures due to an increase in the channel length modulation factor, which reduces output resistance. Nonetheless, intrinsic gain generally improves for short-channel processes in the weak inversion region.

[32] and [33] report the low-temperature RF performances of bulk CMOS transistors in a body-tied-to-source CPW configuration. The junction capacitance within the devices moderately decreases due to incomplete ionization of dopants in the bulk well, while the external capacitance from metal routings remains nearly unchanged. The gate capacitance reduces because of an additional series capacitance to the gate oxide capacitance caused by the increased depletion region. Overall, this reduction in capacitance and increase in transconductance result in an improved current gain cutoff frequency, which is beneficial and can be traded for lower power consumption while maintaining the required speed at low temperatures. Gate resistance decreases until around 50 K due to increased mobility, then saturates and slightly increases near 4 K due to the freeze-out of gate polysilicon. Other external parasitic resistances, representing the resistance of the electrodes and interconnections between terminals, decrease as the temperature lowers. These changes lead to an improved maximum oscillation frequency, with slight saturation near 4 K where gate resistance increases. By employing a two-phase procedure, notably SOLT calibration and open-short de-embedding techniques, the S-parameter behaviors at cryogenic temperatures are also examined. The enhancement of S_{21} can be attributed to the increase in transconductance. Regarding return loss-related parameters, while S_{11}

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remains nearly constant at low temperatures, S_{22} shows slight variations due to the decrease in output resistance.

In LNA design, the noise performance at cryogenic temperatures is also crucial. The primary noise power contribution in a typical room temperature low noise amplifier comes from channel white noise and thermal noise from gate resistance due to the input-referred effect. Fortunately, gate resistance generally decreases with temperature, resulting in a reduction of noise contribution. Regarding noise within the device, [34] provides an interesting examination of the source at low-temperature. As conventional thermal noise reduces proportionally with the temperature, the saturated improvements of the LNA works at cryogenic oppose the model. This is explained by the ballistic transport of the short channel device under high field reinforces the reduction of phonon scattering at low-temperature, resulting dominance of non-equilibrium shot noise in the channel. Under this scenario, for cryogenic applications, the optimization of low noise performance may lay in device selection of reducing shot noise, instead of thermal white noise, such as using longer channel devices.

For RF/mm-wave designers, the performance of on-chip passive components is also crucial. In [35], several types of on-chip resistors are examined, revealing significantly increased resistance with the n-well resistors due to carrier freeze-out at cryogenic temperatures. Conversely, the n-poly and p-active resistors exhibit rather steady resistance values. Furthermore, the p-n-p BJT, often incorporated in bandgap reference circuitries and temperature sensors, also deteriorates owing to carrier freeze-out in the base. [36] offers a compelling review of the extraction of cryogenic models for an MoM capacitor and a transformer, as well as a resonance tank comprising both components. In the case of the rotative inter-digitated MoM capacitor, the core capacitance experiences a slight increase due to variations in the dielectric constant. Meanwhile, the quality factor

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improves at lower frequencies owing to reductions in dielectric and metal loss. However, this improvement diminishes above certain frequencies when the dielectric loss improvement ceases. Concerning the multi-turn transformer, shielding is excluded due to increased substrate resistance at low temperatures caused by carrier freeze-out. Overall, the inductance decreases slightly, while the coupling factor and quality factor increase. The decrease in inductance is attributed to reduced interior current resulting from increased conductivity, thereby reducing the skin depth and interior inductance. Meanwhile, the quality factor improves due to increased conductivity and reduced substrate loss, and the increase in coupling factor is attributed to variations in parasitic capacitance. The reduction of inductance and effective substrate coupling capacitance also enhances self-resonance and peak quality factor frequency. The transformer-based resonator tank follows a similar trend as the transformer, with increased quality factor, higher resonance frequency, and a larger ratio of the first and second resonance frequency due to an increase in coupling factor, resulting in a wider bandwidth. The insertion loss of the resonator tank also decreases, with the *Z*-parameters enhanced at higher frequencies, leading to increased transfer function. Overall, operating at cryogenic temperatures benefits the performance of high-frequency integrated circuits.

Apart from the characterizations briefly reviewed above, other issues such as self-heating, mismatch, and increased flicker noise are also discussed in the literature. It's worth noting that while the references mentioned above focus on bulk CMOS technologies, several other studies concentrate on examining FDSOI processes. This technology exhibits reduced coupling loss and enables back-gate biasing to tackle the incremental threshold voltage issue at cryogenic temperatures. Finally, while there have been some explorations into the development of compact cryogenic models [37, 38], the studies in this chapter continue to rely on the available standard room-temperature model for simulation.

2.1.3 Literature Review of Cryogenic LNAs

Research on low-noise amplifiers operating in cryogenic environments has been a focus in the field of radio astronomy for decades [39]. Numerous studies have explored various technology nodes, aiming for extremely low power consumption, high gain, and performance near the quantum noise limit [40]. III-V compound semiconductor technologies, such as GaAs and InP, have attracted significant attention due to their inherent characteristics of high gain, high speed, and low noise performance, leading to impressive and pioneering results. Because of their advanced development, commercially available or custom III-V compound semiconductor LNAs are commonly used in experimental setups for quantum processors and quantum-related research. While GaAs HEMT LNAs achieve outstanding noise temperature and high gain in the 4 to 8 GHz frequency range for superconducting qubits, they suffer from immense power consumption due to the required high supply voltage [41]. In contrast, reported InP HEMT LNAs not only demonstrate superb noise and gain performance but also sustain these advantages even with reduced supply voltages. This results in state-of-the-art performance at cryogenic temperatures, featuring sub-mW power consumption and noise temperatures in the few K range [42, 43]. In recent years, despite their inherently inferior minimum noise temperature in the frequency range of 4 to 8 GHz compared to InP processes, SiGe BJT technologies have emerged as candidates in this field, thanks to their cost efficiency and integration capabilities within large-scale multifunctional systems. Using a cryogenic noise-optimized process, researchers implemented a two-stage LNA for superconducting qubit readout in [44]. This design achieved remarkable performance metrics, including a mere 1 mW power consumption, over 30 dB gain, and a noise temperature of 2.6 K at an ambient temperature of 17 K. In the lower frequency range

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spanning from hundreds of MHz to around 3 GHz, which is typically utilized for reflectometry readout of semiconductor spin qubits, fewer reports on InP LNAs are available. In contrast, SiGe LNAs demonstrate state-of-the-art performance in this domain. Lowering the supply voltage headroom, as detailed in [45], a two-stage LNA with RC-feedback achieves sub-mW power consumption while still maintaining 32 dB gain and a noise temperature of 4.6 K at an ambient temperature of 15 K.

With an increasing number of demonstrations showcasing integrated system-on-chip control and readout circuitries, research on implementing cryogenic LNAs utilizing bulk CMOS processes also gains interest and significance. In the field of superconducting qubit readout, common-source amplifiers or cascode amplifiers have been demonstrated, employing narrow-band noise matching through source degeneration techniques [46, 47]. By incorporating transformer-based tanks, a broadband characteristic can be achieved, showcased by the front-end LNA in the integrated readout receiver in [6]. Additionally, [48] presents an enhanced topology, integrating wideband matching techniques with reduced noise contribution from the cascode transistor, resulting in a sub-1 dB noise figure at room temperature and over 35 dB gain. However, despite the theoretical capability of the aforementioned source-degeneration-type topology to approach the minimum noise temperature of the device with low-loss passive components at cryogenic temperatures, the demonstrated power consumptions remain substantial. Addressing this issue, [49] introduces a resistive-feedback cascode inverter topology, consuming only 3.5 mW at room temperature, with a remarkable gain of 54 dB. However, due to the low biasing current, the intrinsic noise performance degrades, necessitating, as their analysis reveals, the addition of a superconducting parametric amplifier in front of the receiver chain. [50] explores a compelling study featuring a hybrid CMOS LNA tailored for radio-astronomy applications in the frequency range of 0.9 to 1.8 GHz. While the circuit

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achieves an impressive gain of 32 dB and an exceptionally low noise temperature of 12 K at room temperature, it consumes an overwhelming power of 105mW. These studies shed light on the challenges and opportunities of pursuing ultra-low noise performance within stringent power limitations at cryogenic temperatures.

Compared to their superconducting counterparts, there have been fewer studies on cryogenic LNAs for spin qubit reflectometry readout. An early demonstration in [35] implements a conventional shunt-feedback noise-canceling LNA with cascode transistors, alongside device characterizations. The LNA chain exhibits a gain of 40 dB and a noise figure of 0.8 dB, which, at a temperature of 4 K, is enhanced to a gain of 57 dB and a noise figure of 0.1 dB. However, the circuit's bandwidth is limited to around 400 MHz at room temperature and 500 MHz at 4 K. Additionally, with the inclusion of three subsequent amplifying stages and an output buffer driver, the circuitry consumes 80 mW at room temperature, increasing to 91 mW at 4 K, with 54.9 mW attributed to the LNA core. In the readout receiver chain described in [5], a 1.4 mW differential negative and positive dual-feedback CG LNA is constructed. However, the low-power design yields a noise figure lower than 3 dB at room temperature, necessitating the incorporation of an additional III-V compound semiconductor LNA in the readout chain before the receiver. In [51] and a subsequent extending article in [52], two noise-canceling LNAs are introduced. The first LNA utilizes a conventional topology enhanced with the self-forward-body-bias (SFBB) technique to mitigate the increased threshold voltage at cryogenic temperatures. Despite the high power consumption associated with this technique, the LNA achieves an exceptional noise figure of 0.63 dB at room temperature and a noise temperature of 2.2 K at 4 K ambient temperature. The second LNA abandons the SFBB technique in favor of a source-follower feedback method on the auxiliary amplifier. This approach provides additional flexibility in input matching and eases the

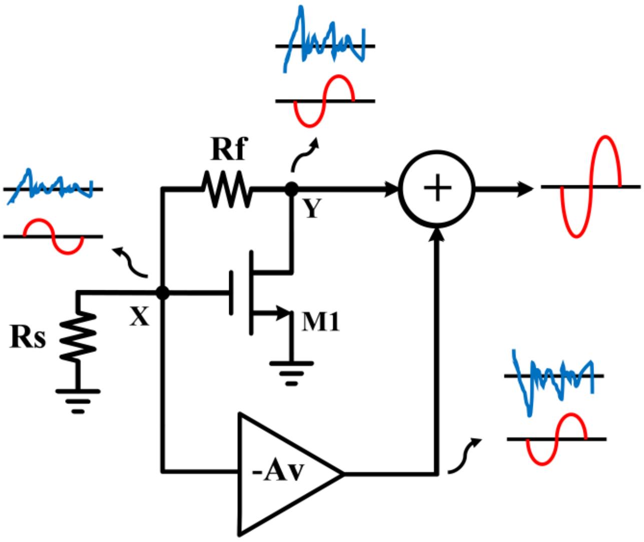

Figure 2.1: Schematic diagram of noise-canceling technique implemented with a shunt-feedback common-source amplifier stage.

constraints imposed by the feedback resistor trade-off on the main inverter amplifier. In [53], the same research group explores another topology that also applies the SFBB technique to the main inverter amplifier. By incorporating inductors, they propose a two-fold current reuse structure for the auxiliary and combining transistors, which effectively reduces power consumption. This LNA achieves less than 10 mW power consumption at 4 K, with a noise temperature of only 6.8 K and a gain of 31 dB over a frequency range of 0.01 to 2.6 GHz.

2.2 Circuit Design

As discussed in Sec. 2.1.1, the resistive-feedback common source (CS) amplifier stage is chosen as the input block of the LNA due to the single-ended requirement in reflectometry readout and its easier future system-on-chip integration, as it eliminates the need for an off-chip biasing inductor required in common-gate transistors. Figure 2.1 illustrates the schematic diagram of conventional noise-canceling technique implemented with a resistive-feedback CS amplifier stage. The noise current from the resistive-feedback CS transistor M1 introduces a corresponding noise voltage at the drain node, depicted by the blue fluctuations at node Y. This noise current flows back through the

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feedback resistor Rf, creating reduced noise voltage fluctuations at the circuit's input node with the same polarity, as shown at node X. The noise-canceling technique introduces an auxiliary amplifier stage parallel to the resistive-feedback CS amplifier. This auxiliary block amplifies the noise voltage at node X, producing a noise voltage at its output node with reversed polarity. By using an ideal voltage combiner and carefully tuning the auxiliary amplification, the noise contribution of transistor M1 can be fully cancelled and mitigated at the output node of the circuit. On the other hand, the input signal at node X undergoes amplification and polarity reversal by both the resistive-feedback CS amplifier and the auxiliary amplifier, as shown by the red sinusoidal waveform in Figure 2.1. The summation of these two paths with the same polarity results in a combined amplified output signal at the output node after the combining stage.

In practical implementation, this conventional noise-canceling architecture encounters several challenges and shortcomings. Firstly, although the technique ideally eliminates the noise contribution of transistor M1 in the main resistive-feedback CS block, it does not address the noise issues of the auxiliary amplifier. This often results in significant power consumption and may require additional current sources for the auxiliary amplifier to reduce inherent noise by increasing the transistor's transconductance. Secondly, there is a trade-off between voltage gain and input impedance within the shunt-feedback CS topology. The need for input matching in a general LNA limits the voltage gain of the input amplifying block. Insufficient first-stage amplification is undesirable as it can increase the noise contribution of subsequent stages in the receiving chain. Finally, the circuit's inadequate gain is further exacerbated by the common practice in the literature of using common-drain transistors in the combining stage. In applications like wireless communication or radio receivers, employing a

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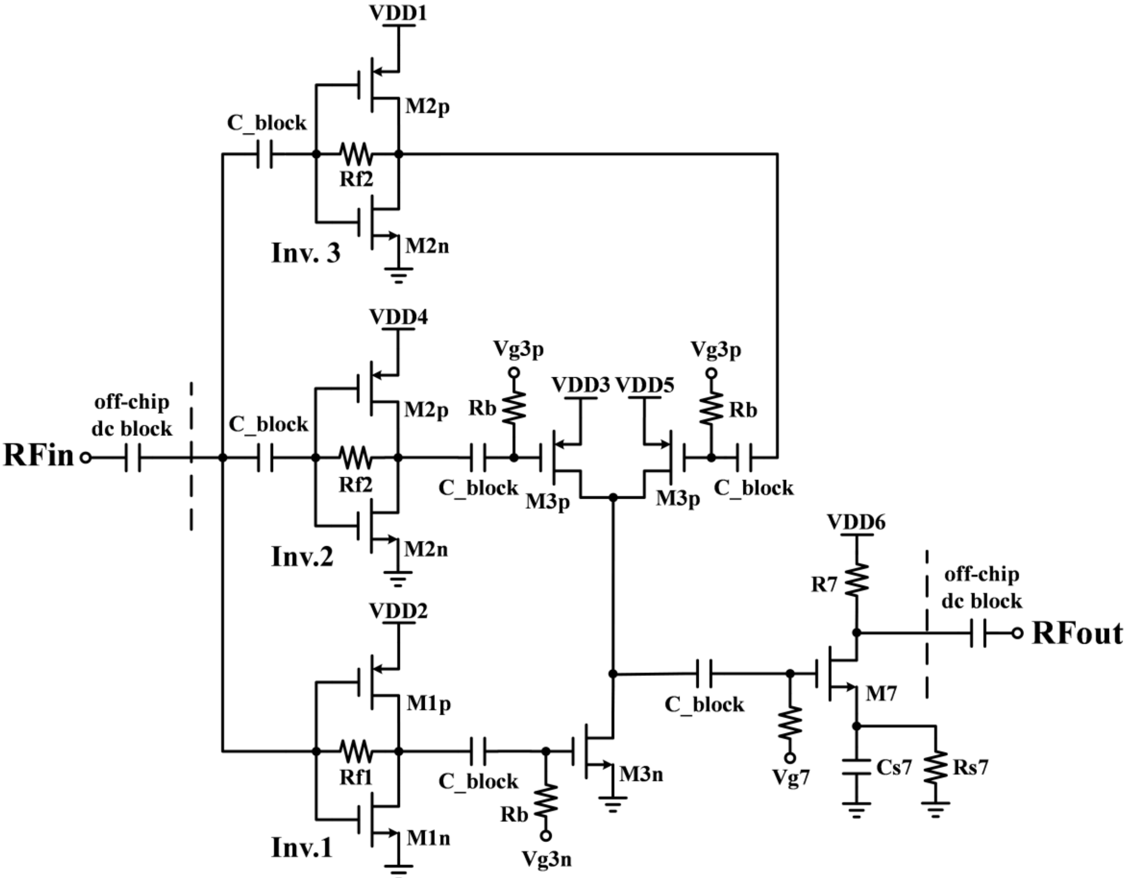

Figure 2.2: Schematic diagram of the proposed cryo-CMOS LNA.

source-follower in the combining stage enhances circuit linearity, which is a primary focus in these studies. However, source followers lack the ability to drive loads with low impedance, often resulting in less than unity amplification in this stage, leading to a reduced overall gain for the LNAs. In contrast, for our targeted application, where the reflected signal from quantum devices in the reflectometry readout is often below -130 dBm, the circuit linearity can be compromised in favor of superior gain and noise performance.

Figure 2.2 shows the schematic diagram of the proposed cryo-CMOS LNA. In contrast to the conventional topology, where typically only the core input amplifier is realized with a resistive-feedback CS amplifier, the proposed design employs resistive-feedback CS amplifiers for both the core input amplifier and the auxiliary amplifier blocks. Additionally, a pMOS transistor is integrated into the resistive-feedback CS amplifier as

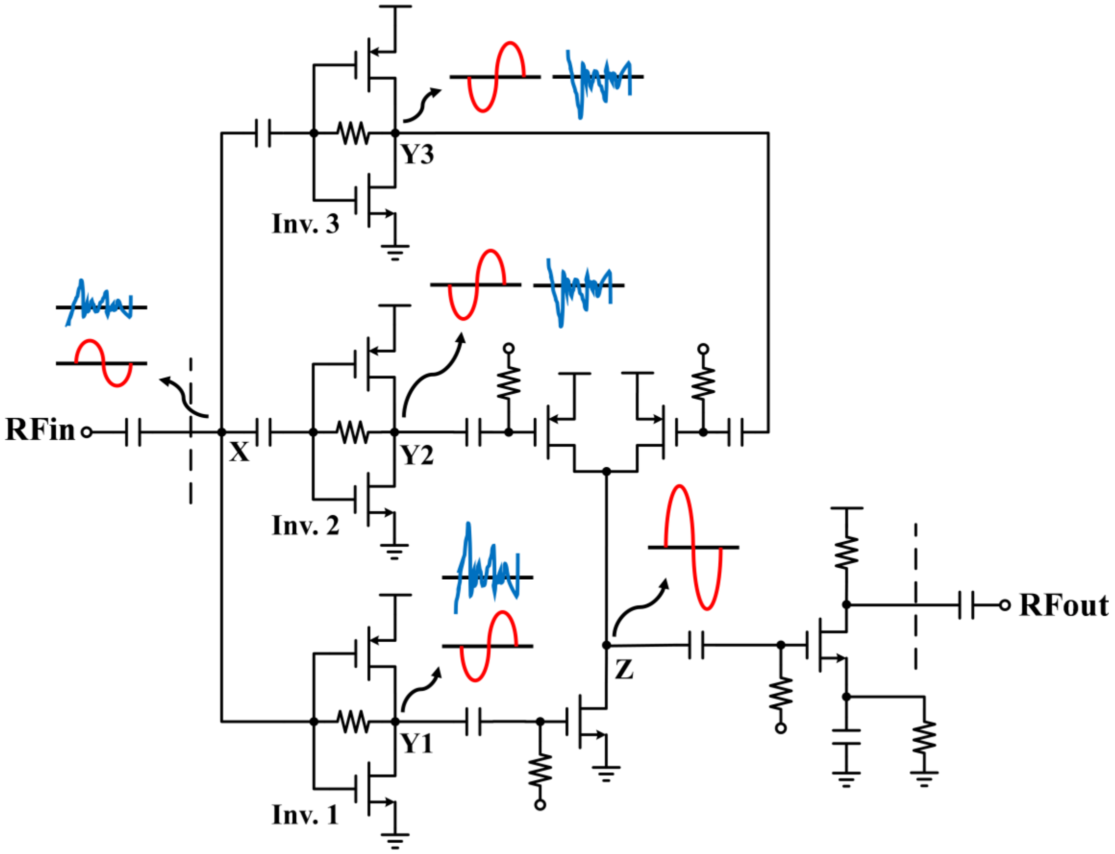

Figure 2.3: Schematic diagram of the noise-canceling mechanism of the noise contributions from the transistors of Inverter 1 in the proposed cryo-CMOS LNA.

an active load, enhancing the transconductance of the inverter amplifier without increasing power consumption. At the combining stage, rather than employing source followers, all combining paths utilize common source amplifiers. This approach allows for further amplification of the voltage gain from the first stage, albeit at the expense of reduced linearity.

Figure 2.3 illustrates the noise canceling mechanism of the proposed topology. The blue noise waveform represents the noise contribution from the transistors of Inverter 1. At node Y1, both the pMOS and nMOS transistors of Inverter 1 introduce noise fluctuations at their drains. These noise currents flow through the feedback resistor of Inverter 1, creating voltage fluctuations at the input node X with reduced amplitude but the same polarity. These fluctuations are then amplified by Inverter 2 and Inverter 3, resulting in noise voltages with reversed polarity at nodes Y2 and Y3. The common

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source amplifiers at the combining stage further amplify and reverse the polarity of these noise signals. At node Z, the resulting noise fluctuation from Inverter 1's transistors is cancelled out due to the opposite polarity contributions from Inverter 2 and Inverter 3. Similarly, the noise contributions from the transistors of auxiliary Inverter 2 and Inverter 3 can be analyzed, where Inverter 1 acts as the noise canceling path, reducing noise fluctuations originating from these auxiliary amplifiers. Conversely, the input signal at node X is amplified through the three separate paths, combined, and magnified at node Z with the same polarity. As a result, the proposed approach effectively cancels the noise contributions of both the core amplifier block and the auxiliary amplifier block, while enhancing the overall voltage gain of the LNA through the summation of three parallel paths and the utilization of common source transistors at the combining stage.

Following the combining stage, an output driver stage employs a common source amplifier is implemented to sustain the overall voltage gain of the LNA. As previously mentioned, a source follower is not suitable for driving the low characteristic impedance of 50 ohms typical in RF systems. The proposed LNA also incorporates capacitive degeneration technique at the output driver stage, thereby broadening the 3-dB gain bandwidth.

Finally, several dc blocking capacitors are added to independently adjust the supply voltage and current of each branch during measurements. This is preferable because predicting the cryogenic performance of the circuit is challenging due to the absence of a compact model. The following subsections delve into the details of the proposed LNA circuit design, beginning with an analysis of the single inverter design.

2.2.1 Single Inverter Design

Beginning with the core block of our proposed LNA, this subsection delves into the analysis of noise and small-signal responses of an inverter amplifier. Figure 2.4 (a) depicts

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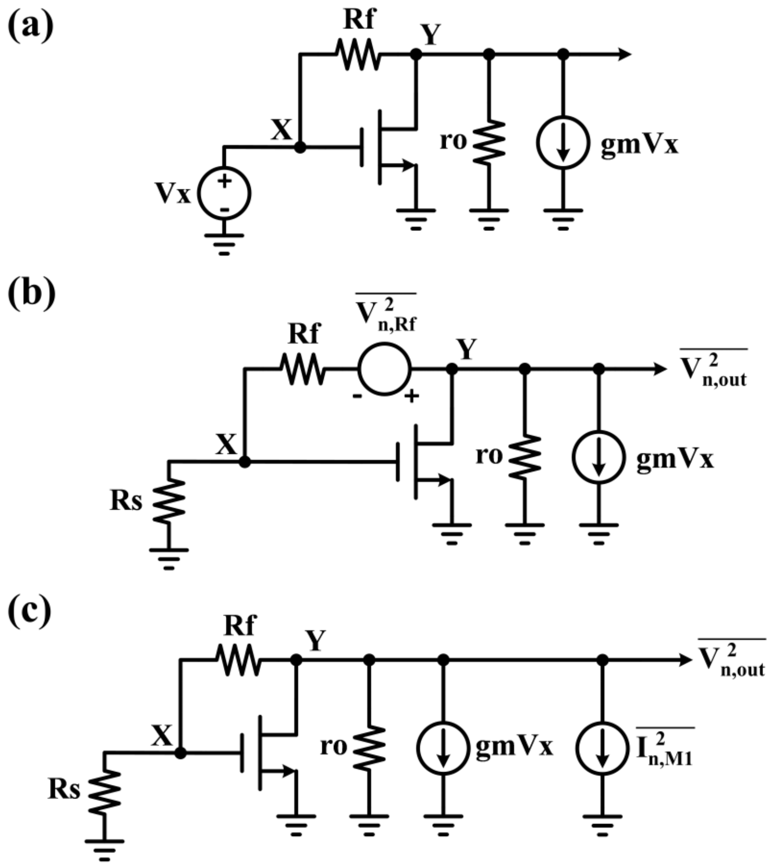

Figure 2.4: Schematic diagram for calculating gain and noise power of an inverter amplifier stage. (a) Gain and input impedance. (b) Noise of the feedback resistor. (c) noise of the transistor.

the schematic diagram used to compute the small-signal response of an inverter amplifier. The transconductance and output impedance of both the pMOS and nMOS transistors are combined to simplify the analysis. Following simple calculation, the low-frequency voltage gain from node X to node Y can be derived as:

$$A_{\mathrm{v}} = -\frac{\left(g_{\mathrm{m}} R_{\mathrm{f}} - 1\right) r_{\mathrm{o}}}{r_{\mathrm{o}} + R_{\mathrm{f}}} \tag{2.1}$$

Similarly, the low-frequency input resistance of the inverter amplifier as seen from node X is calculated as:

$$R_{\mathrm{in}} = \frac{r_{\mathrm{o}} + R_{\mathrm{f}}}{1 + g_{\mathrm{m}} r_{\mathrm{o}}} \tag{2.2}$$

After calculating the low-frequency small-signal responses of the inverter amplifier, the output thermal noise power contributed by the feedback resistor and the transistors

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can also be determined. Illustrated in Figure 2.3 (b), the thermal noise voltage of the feedback resistor at the output node can be derived as:

$$\overline{V_{\mathrm{n,out,Rf}}^{2}} = 4k_{\mathrm{B}}TR_{\mathrm{f}}\left[\frac{r_{\mathrm{o}}(g_{\mathrm{m}}R_{\mathrm{s}}+1)}{r_{\mathrm{o}}(g_{\mathrm{m}}R_{\mathrm{s}}+1)+R_{\mathrm{f}}+R_{\mathrm{s}}}\right]^{2} \tag{2.3}$$

In a similar manner, the thermal noise contribution of the transistors at the output node of an inverter amplifier can be determined, as depicted in Figure 2.4 (c):

$$\overline{V_{\mathrm{n,out,MOS}}^{2}} = 4k_{\mathrm{B}}T\gamma g_{\mathrm{m}}\left[\frac{-r_{\mathrm{o}}(R_{\mathrm{f}}+R_{\mathrm{s}})}{r_{\mathrm{o}}(g_{\mathrm{m}}R_{\mathrm{s}}+1)+R_{\mathrm{f}}+R_{\mathrm{s}}}\right]^{2} \tag{2.4}$$

The noise factor of a low noise amplifier is defined as the ratio of the total output noise power divided by the output noise power contributed solely from the source resistor. Here, the noise power contributed by the source resistor at the output noise of an inverter amplifier can be calculated as:

$$\overline{V_{\mathrm{n,out,Rs}}^{2}} = 4k_{\mathrm{B}}TR_{\mathrm{s}}A_{\mathrm{v}}^{2}\left(\frac{Z_{\mathrm{in}}}{Z_{\mathrm{in}}+R_{\mathrm{s}}}\right)^{2} \tag{2.5}$$

where A_{v} and Z_{in} can be derived using Eqn. (2.1) and Eqn. (2.2) at low frequencies.

Consequently, the noise factor contribution from the feedback resistor, which quantifies the ratio of the output thermal noise power from the feedback resistor to that from the source resistor, is derived and surprisingly results in a clear form:

$$NF_{\mathrm{Rf}} = \frac{R_{\mathrm{f}}(g_{\mathrm{m}}R_{\mathrm{s}}+1)^{2}}{R_{\mathrm{s}}(g_{\mathrm{m}}R_{\mathrm{f}}-1)^{2}} \tag{2.6}$$

A similar calculation can be performed to determine the corresponding contribution of the transistors to the noise factor:

$$NF_{\mathrm{MOS}} = \frac{\gamma g_{\mathrm{m}}(R_{\mathrm{f}}+R_{\mathrm{s}})^{2}}{R_{\mathrm{s}}(g_{\mathrm{m}}R_{\mathrm{f}}-1)^{2}} \tag{2.7}$$

As a result, the noise factor of an inverter amplifier is obtained as:

$$NF = 1 + NF_{\mathrm{Rf}} + NF_{\mathrm{MOS}} \tag{2.8}$$

With the formulas derived above, the small-signal responses and noise performance

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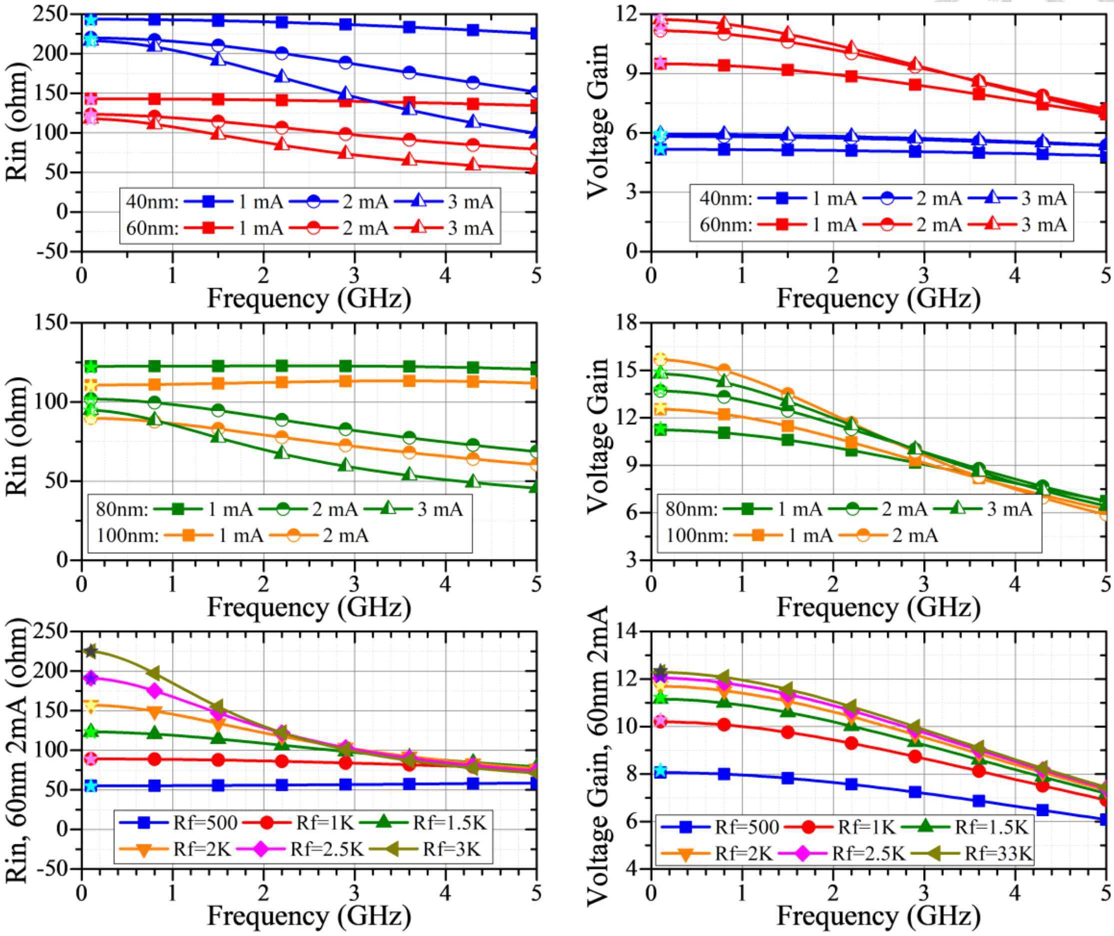

Figure 2.5: Simulated and calculated small-signal responses of an inverter amplifier with different power consumption levels, gate lengths, and feedback resistors.

of an inverter amplifier can be predicted based on the transconductance and output resistance of the transistors provided. In the top two rows of Figure 2.5, the simulated frequency responses of the input impedance and voltage gain of an inverter amplifier with varying levels of biasing current and different transistor lengths are shown. The bottom row compares the responses for different feedback resistor sizes, using identical transistors with a 60 nm gate length and a 2 mA drain current bias. The calculated results obtained from Eqn. (2.1) and Eqn. (2.2) are marked with asterisks at the lowest frequency point. Since the derived formulas do not account for any capacitance, they only predict the low-frequency responses, which align closely with the simulation results.

Firstly, according to Eqn. (2.1) and the data on the right-hand side of Figure 2.5, the voltage gain loosely correlates with the intrinsic gain of the transistor, which typically increases with longer devices under certain biasing currents. However, with a fixed feedback resistor, Eqn. (2.2) indicates that the input resistance of an inverter amplifier is inversely proportional to the intrinsic gain of the transistors, showing opposite trends compared to the voltage gain in Figure 2.5. Increasing the biasing current enhances the voltage gain by increasing the transconductance of the transistors, but it decreases the input resistance, as derived in Eqn. (2.2). When varying the feedback resistor value, higher feedback resistance leads to higher voltage gain, but also increases the input impedance, as observed in Eqn. (2.2). These considerations present challenges and trade-offs in achieving high voltage gain in the circuit while maintaining the required input power match. Furthermore, concerning higher frequency responses involving capacitance at the input and output nodes, larger transistor sizes increase parasitic capacitance values, exacerbating deviations at high frequencies compared to those calculated at low frequencies. This effect is visible in Figure 2.5 for cases involving longer gate lengths or higher biasing currents, which necessitate larger transistor widths. Moreover, larger feedback resistors exhibit a similar increased slope, as the frequency bandwidth of the circuit can be estimated by the RC time constant. In general, the presence of capacitance reduces both the voltage gain and the real parts of the input impedance at high frequencies, thereby degrading the circuit's overall gain, input-matching performance, and the effectiveness of the noise-canceling technique.

Besides the small-signal responses, device selection also affects the noise performance of the inverter amplifier. The left-hand side of Figure 2.6 shows the simulated output thermal noise power from the source resistor, the transistors, and the feedback resistor respectively. On the right-hand side, the ratio between the transistors/feedback resistor and the source resistor is displayed, along with the resulting noise figure. The calculated results using Eqn. (2.3) to Eqn. (2.8) are also marked with

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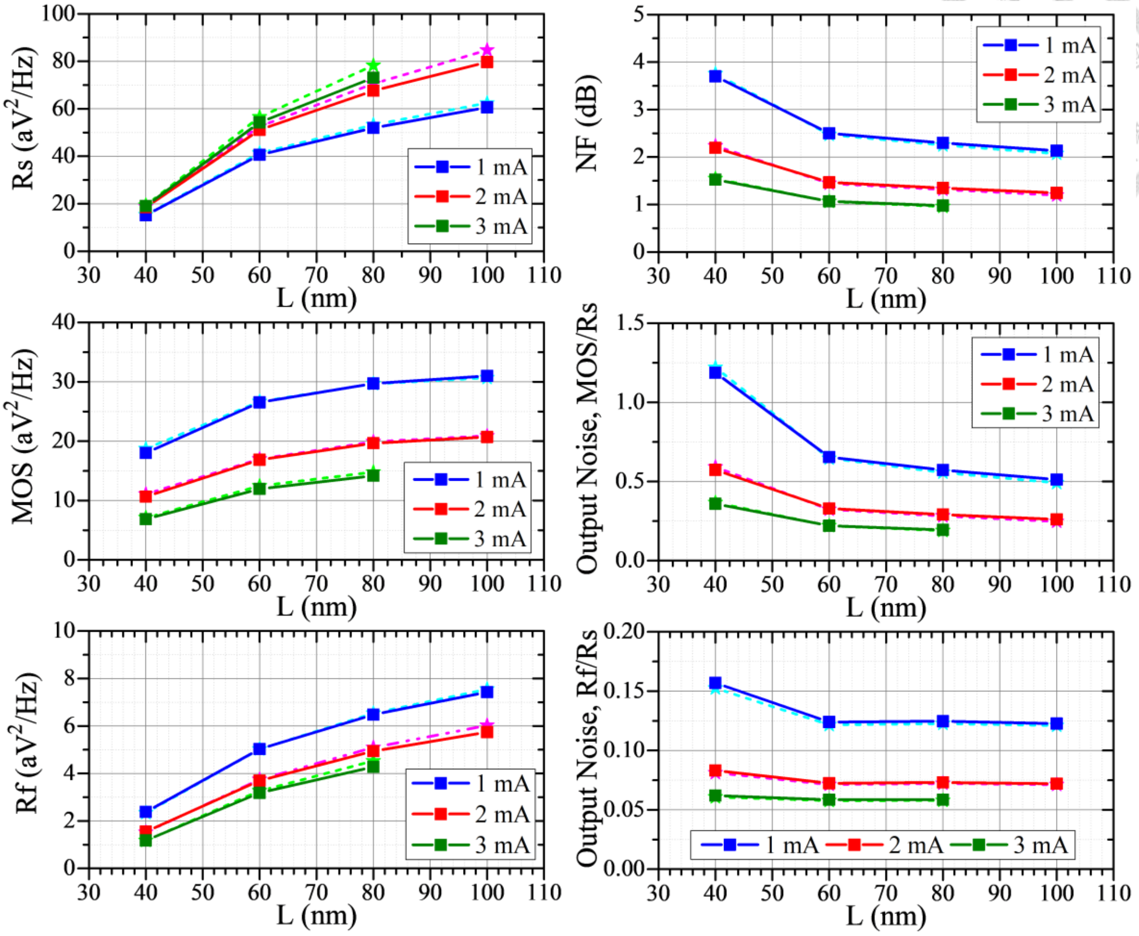

Figure 2.6: Simulated and calculated output noise power contributions from various sources, output noise power ratios, and noise figure of an inverter amplifier with different power consumption levels and gate lengths.

asterisks in the figure. The simulated data is extracted at a frequency point of 800 MHz to eliminate the influence of transistor flicker noise, which is not considered in the calculations. However, this approach results in increased deviation between the simulated and calculated results in Figure 2.6 for the output noise power from the resistors, where the simulation at 800 MHz starts to be affected by degraded gain due to capacitance, particularly with larger devices. the calculated data represents only near dc results, thus overestimating the output noise power in the figure. It has been verified that the calculated data for the resistors aligns well with simulation data at 100 MHz. Nonetheless, to provide practical simulated noise figures at specific frequencies, the simulation results in Figure 2.6 are displayed at 800 MHz across all parameters. Moreover, to align the calculation

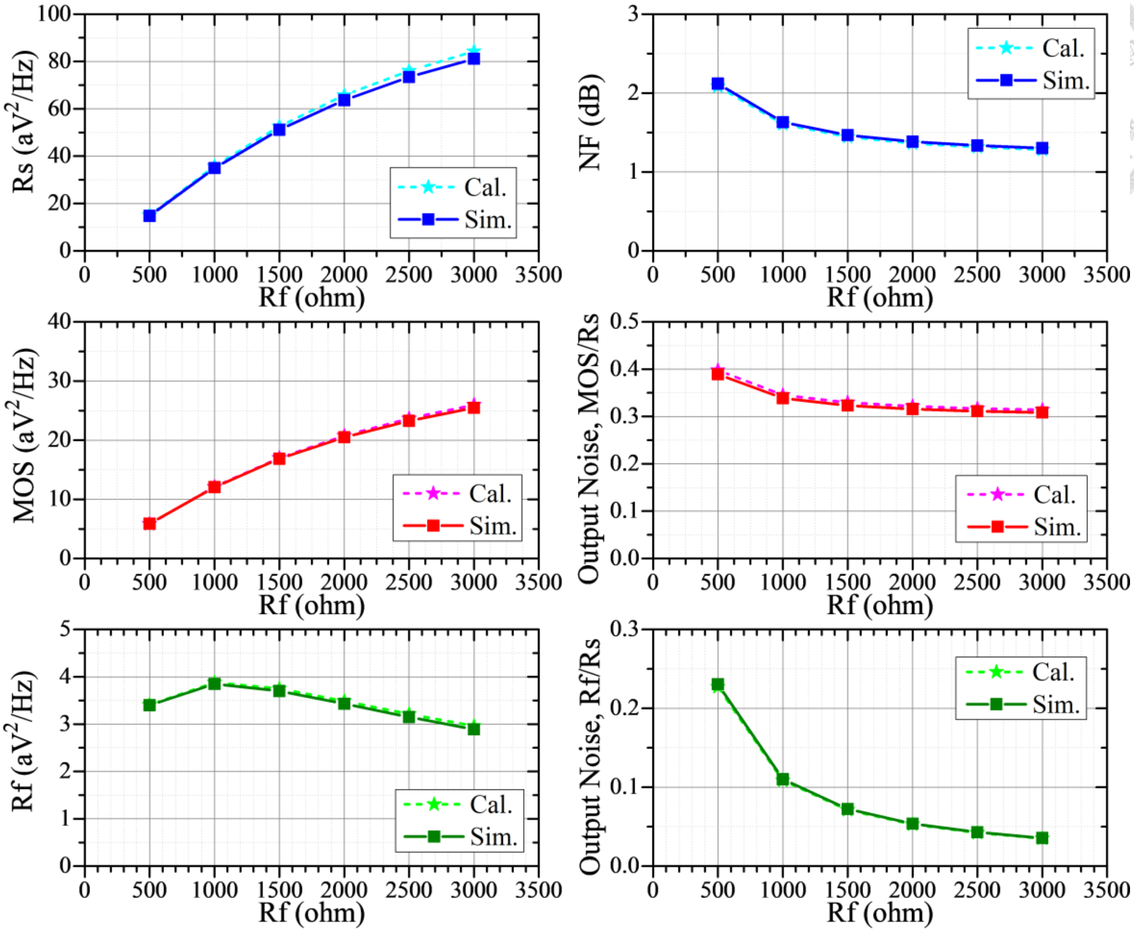

Figure 2.7: Simulated and calculated output noise power contributions from various sources, output noise power ratios, and noise figure of an inverter amplifier with different feedback resistor values.

with the simulated data for the output noise power of the transistors, the coefficient γ is set to 1, 0.67, 0.57, and 0.51 for transistors with gate lengths of 40 nm, 60 nm, 80 nm, and 100 nm respectively.

Interestingly, according to Eqn. (2.6) and Eqn. (2.7), the ratio of output noise power between the transistors/feedback resistors and that of the source resistor doesn’t depend on the output resistance of the transistor. This highlights that the noise factor depends solely on the transconductance under a fixed feedback resistor value, as demonstrated by the lower noise figure in cases with larger gate length and larger biasing current in Figure 2.6. A similar analysis can be conducted for cases where the value of the feedback resistor is varied. As shown in Figure 2.7 and predicted by the formulas above, a larger feedback resistor significantly reduces the output noise power contribution from the feedback resistor itself compared to that from the source resistor. A slight decrease in the output noise ratio from the transistors is also observed when an increase in the feedback resistor size. Lastly, it's worth noting that the values in the simulation and calculation shown in Figure 2.6 and Figure 2.7 focus solely on thermal noise power. In practice, other noise sources such as low-frequency flicker noise and noise induced by gate resistance may additionally degrade the LNA performance.

In summary, in a single inverter amplifier design, the noise contributions from the feedback resistor and the transistors can be reduced by increasing the feedback resistor size and enhancing the transconductance of the transistors, respectively. However, increasing the feedback resistor also raises the input resistance, whereas boosting the transconductance, achieved by increasing the supply voltage or gate length, reduces the input resistance. Although it may seem feasible to strike a balance for achieving improved gain and noise performance while maintaining input matching by enlarging both the feedback resistor and the transistors, these adjustments often result in a sharper roll-off at higher frequencies compared to the designed values. Considering the increased power consumption and reduced bandwidth resulting from enlarging transistors and feedback resistors, a single inverter amplifier inherently faces limitations in achieving comprehensively superior performance.

2.2.2 Inverter Pair and Mutual Noise-Canceling

To further improve the design, an additional inverter amplifier is introduced in parallel with the original one. The sizes of the transistors and the feedback resistors are assumed identical here to simplify the analysis. The two inverter amplifier blocks are connected in parallel at the input node and combined using an ideal voltage combiner with unity gain at the output node. With this parallel configuration and ideal voltage

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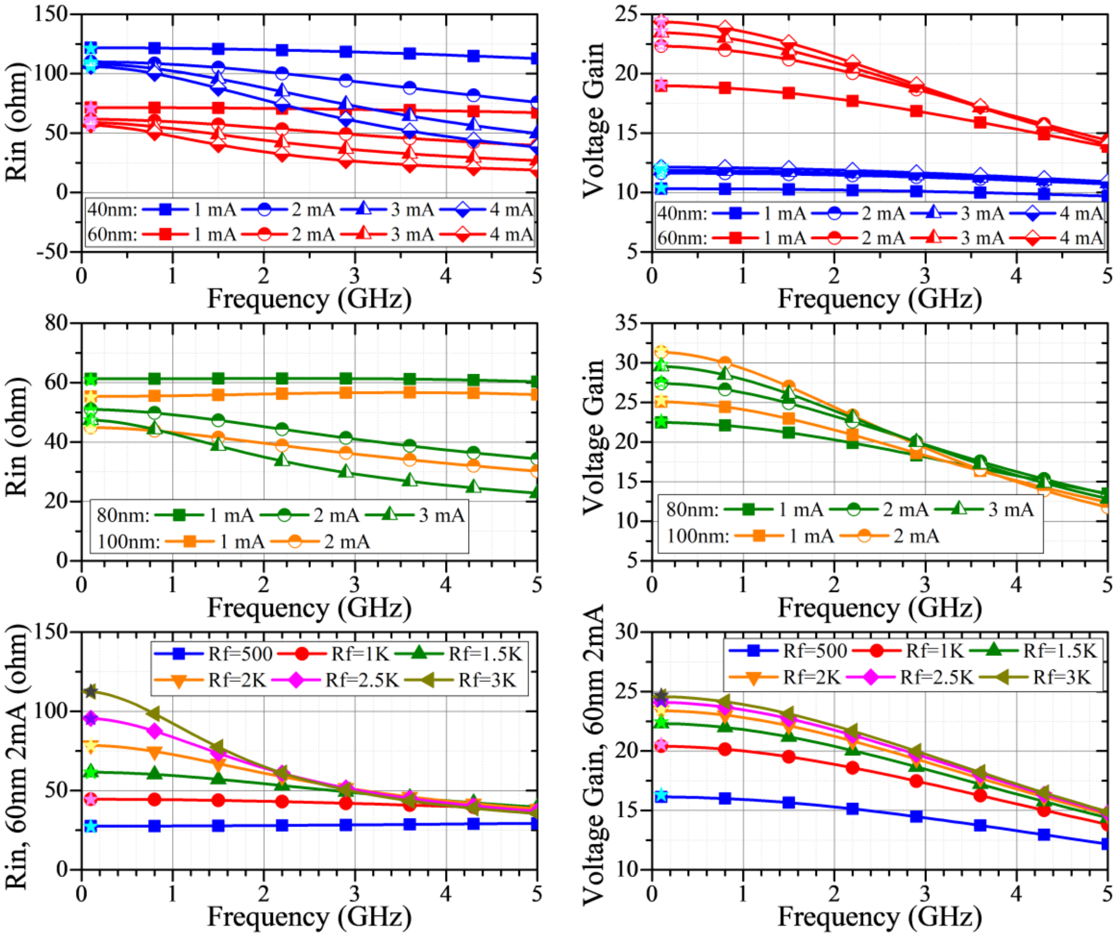

Figure 2.8: Simulated and calculated small-signal responses of inverter amplifier pair with different power consumption levels, gate lengths, and feedback resistors.

combiner, the overall voltage gain of the inverter amplifier pair is doubled of that in Eqn. (2.1). Meanwhile, at the input node, the input resistance is halved compared to that in (2.2). This reduction in input resistance allows for increased flexibility in adjusting the feedback resistor, thereby further improving voltage gain and reducing noise figure. Figure 2.8 depicts the simulated and calculated small signal responses of an inverter amplifier pair, similar to those shown in Figure 2.5. A comparison between the two figures also reveals that at the lowest frequency, the input resistance is halved while the voltage gain is doubled. Additionally, the rate of roll-off in input impedance and voltage gain values follows a consistent pattern, with the input impedance halved and the voltage gain doubled, respectively, owing to the parallel configuration. Therefore, the penalty of reduced bandwidth when increasing feedback resistance is more pronounced in an

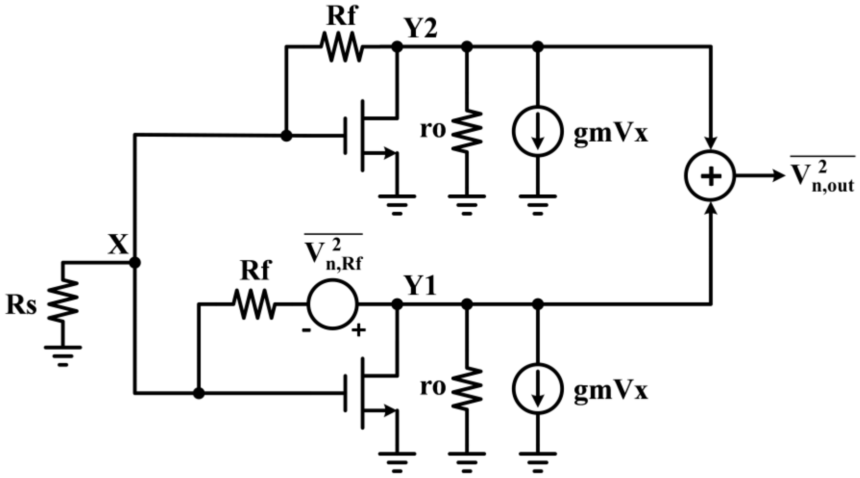

Figure 2.9: Schematic diagram for calculating the noise power contribution from the feedback resistors of inverter amplifier pair.

inverter pair. Nonetheless, the parallel topology inherently doubles the voltage gain compared to a single inverter amplifier, albeit with a corresponding doubling in power consumption.

In order to analyze the noise performance of inverter amplifier pair, Figure 2.9 illustrates the schematic diagram for calculating the noise power contributed by the feedback resistor in the lower inverter amplifier. Assuming an identical inverter pair, the noise power at node Y1 from the feedback resistor of the lower inverter is derived as:

$$\overline{V^2_{\mathrm{n,Y1,Rf}}} = 4k_{\mathrm{B}}TR_{\mathrm{f}}\left[\frac{r_{\mathrm{o}}(g_{\mathrm{m}}R_{\mathrm{s}}(R_{\mathrm{s}}+2r_{\mathrm{o}})+R_{\mathrm{f}}+R_{\mathrm{s}}+r_{\mathrm{o}})}{(R_{\mathrm{f}}+R_{\mathrm{s}})(R_{\mathrm{f}}+2g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}+r_{\mathrm{o}}+2R_{\mathrm{s}})}\right]^2 \tag{2.9}$$

Similarly, the noise power at node Y2 can be determined:

$$\overline{V^2_{\mathrm{n,Y2,Rf}}} = 4k_{\mathrm{B}}TR_{\mathrm{f}}\left[\frac{R_{\mathrm{s}}r_{\mathrm{o}}(g_{\mathrm{m}}R_{\mathrm{f}}-1)}{(R_{\mathrm{f}}+R_{\mathrm{s}})(R_{\mathrm{f}}+2g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}+r_{\mathrm{o}}+2R_{\mathrm{s}})}\right]^2 \tag{2.10}$$

Unfortunately, the noise fluctuations at nodes Y1 and Y2 exhibit the same polarity, as indicated by the signs within brackets in Eqn. (2.9) and Eqn. (2.10), respectively. With an ideal combiner, the output noise power from the feedback resistor in the lower inverter amplifier is obtained as:

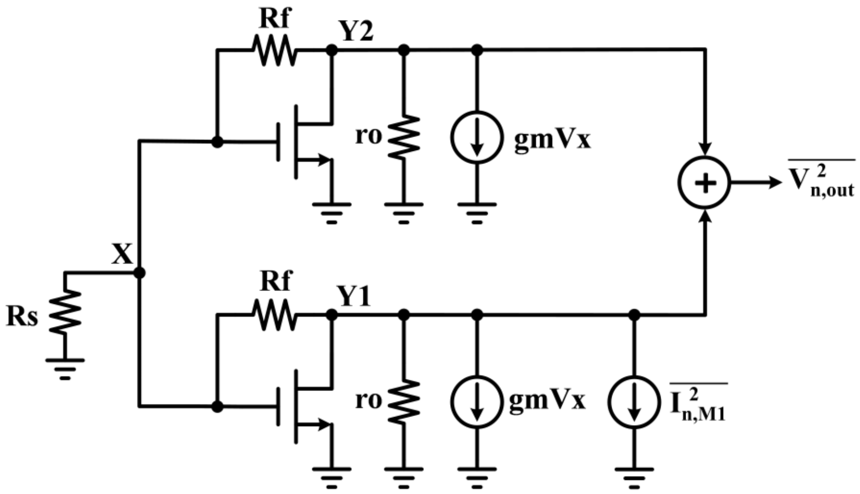

Figure 2.10: Schematic diagram for calculating the noise power contribution from the transistors of inverter amplifier pair.

$$\overline{V^2_{\mathrm{n,out,Rf}}} = 4k_{\mathrm{B}}TR_{\mathrm{f}}\left[\frac{r_{\mathrm{o}}(2g_{\mathrm{m}}R_{\mathrm{s}}+1)}{(R_{\mathrm{f}}+2g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}+r_{\mathrm{o}}+2R_{\mathrm{s}})}\right]^2 \tag{2.11}$$

In a similar fashion, the noise power from the transistors of the lower inverter amplifier is analyzed with the help of Figure 2.10. At node Y1, the noise power is calculated as:

$$\overline{V^2_{\mathrm{n,Y1,MOS}}} = 4k_{\mathrm{B}}T\gamma g_{\mathrm{m}}\left[\frac{-r_{\mathrm{o}}(R_{\mathrm{f}}^2+R_{\mathrm{f}}g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}+R_{\mathrm{f}}r_{\mathrm{o}}+2R_{\mathrm{f}}R_{\mathrm{s}}+R_{\mathrm{s}}r_{\mathrm{o}})}{(R_{\mathrm{f}}+r_{\mathrm{o}})(R_{\mathrm{f}}+2g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}+r_{\mathrm{o}}+2R_{\mathrm{s}})}\right]^2 \tag{2.12}$$

At node Y2, the lengthy calculation results in noise power being:

$$\overline{V^2_{\mathrm{n,Y2,MOS}}} = 4k_{\mathrm{B}}T\gamma g_{\mathrm{m}}\left[\frac{r_{\mathrm{o}}^2R_{\mathrm{s}}(g_{\mathrm{m}}R_{\mathrm{f}}-1)}{(R_{\mathrm{f}}+r_{\mathrm{o}})(R_{\mathrm{f}}+2g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}+r_{\mathrm{o}}+2R_{\mathrm{s}})}\right]^2 \tag{2.13}$$

Interestingly, the sign within the brackets in Eqn. (2.12) and Eqn. (2.13) is opposite to each other, reflecting the noise-canceling mechanism discussed earlier. Here, the noise current from the transistors in the lower inverter flows back through the feedback resistor and is amplified by the upper inverter from input node X. This results in a reversal of the noise voltage polarity at node Y2 compared to node Y1. Using an ideal voltage combiner, the output noise voltage from the transistors of the lower inverter is derived as:

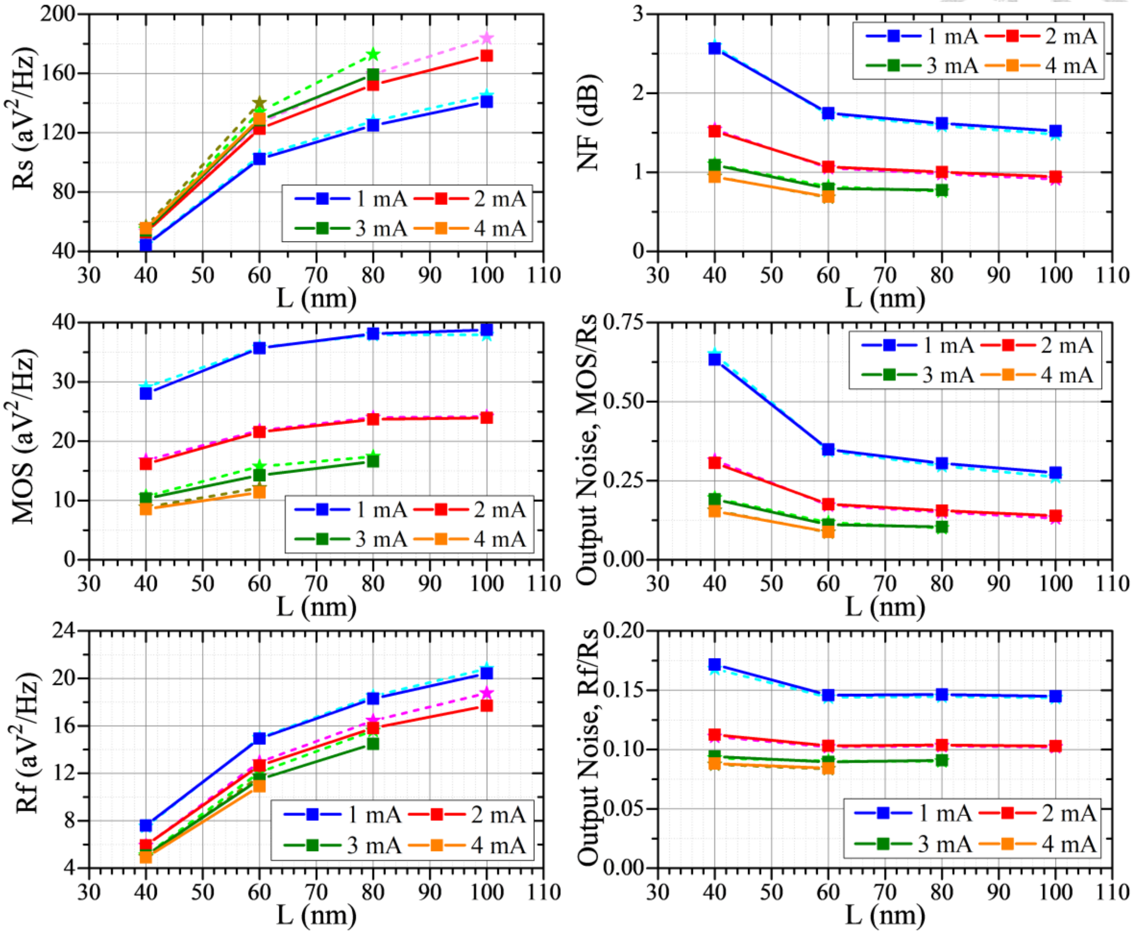

Figure 2.11: Simulated and calculated output noise power contributions from various sources, output noise power ratios, and noise figure of an inverter amplifier pair with different power consumption levels and gate lengths.

$$\overline{V^2_{\mathrm{n,out,MOS}}} = 4k_{\mathrm{B}}T\gamma g_{\mathrm{m}}\left[\frac{-r_{\mathrm{o}}(R_{\mathrm{f}}+2R_{\mathrm{s}})}{(R_{\mathrm{f}}+2g_{\mathrm{m}}r_{\mathrm{o}}R_{\mathrm{s}}+r_{\mathrm{o}}+2R_{\mathrm{s}})}\right]^2 \tag{2.14}$$

The noise power from the source resistor at the output node, after the voltage combiner, can be derived using Eqn. (2.5), with the voltage gain doubled and the input resistance halved compared to the single inverter amplifier case. By doubling the values calculated from Eqn. (2.11) and Eqn. (2.14) to include the contribution of the upper inverter amplifier, the overall output noise ratio of the feedback resistor to the source resistor is then derived as:

$$NF_{\mathrm{Rf}} = \frac{R_{\mathrm{f}}(2g_{\mathrm{m}}R_{\mathrm{s}}+1)^2}{2R_{\mathrm{s}}(g_{\mathrm{m}}R_{\mathrm{f}}-1)^2} \tag{2.15}$$

The overall output noise ratio of the transistors to the source resistor is determined as:

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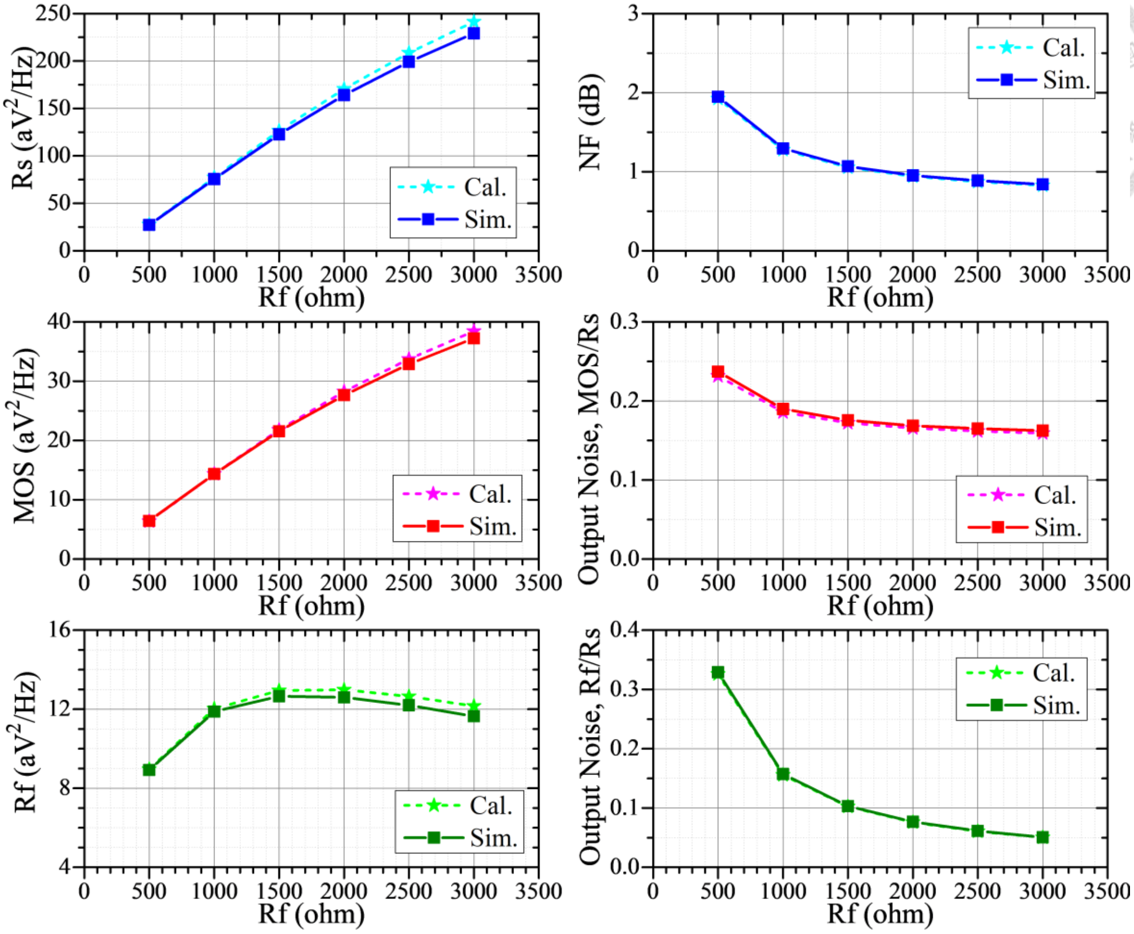

Figure 2.12: Simulated and calculated output noise power contributions from various sources, output noise power ratios, and noise figure of an inverter amplifier pair with different feedback resistor values.

$$NF_{\mathrm{MOS}} = \frac{\gamma g_{\mathrm{m}}(R_{\mathrm{f}} + 2R_{\mathrm{s}})^2}{2R_{\mathrm{s}}(g_{\mathrm{m}}R_{\mathrm{f}} - 1)^2} \tag{2.16}$$

Finally, the overall noise factor of an inverter amplifier pair can be calculated by substituting the results of Eqn. (2.15) and Eqn. (2.16) into Eqn. (2.8).

Comparisons across different gate lengths, biasing current levels, and feedback resistor values, similar to those shown in Figure 2.6 and Figure 2.7 for a single inverter amplifier case, are illustrated in Figure 2.11 and Figure 2.12. The calculated results using the formulas mentioned above are denoted with asterisks in the figures. The enhanced deviation from the 800 MHz simulation data is also attributed to exacerbated roll-off voltage gain responses in the case of inverter amplifier pair. Comparing the simulation results shown in Figure 2.6 and Figure 2.11, it’s observed that the output noise power of the source resistor doesn’t increase by a factor of four despite the doubled voltage gain. This can be attributed to the halved input impedance, which reduces the noise voltage fluctuation magnitude of the source resistor at the input node of the inverter amplifier pair, as described in Eqn. (2.5). On the other hand, according to Eqn. (2.9) and Eqn. (2.10), the parallel inverter pair increases the output noise voltage from the feedback resistor. After doubling the derived value to account for two feedback resistors, the overall output noise power from the feedback resistors increases more significantly than the increase in the source resistor’s output noise power. This results in an expanded ratio compared to that in the single inverter amplifier case, which can also be observe by comparing the coefficients in Eqn. (2.6) and Eqn. (2.15).

In contrast to the feedback resistors, the noise contribution of the transistors is significantly reduced in the inverter pair configuration, as indicated by the factor 2 in the denominator of Eqn. (2.16). This topology facilitates where the noise voltages from the two branches have opposite polarities, nearly halving the resulting output noise power ratio of transistors in Figure 2.11 compared to Figure 2.6. As a result, the inverter amplifier pair topology effectively decreases the noise figure even further compares to a single inverter amplifier stage.

Given that the inverter pair topology consumes twice the power of a single inverter, it is essential to compare the two topologies under the same overall dc power and input impedance. For this comparison, the 500-ohm feedback resistor case from Figure 2.5 is chosen because of its nearly matched input resistance of 54.6 ohms. Accordingly, an inverter pair with two 60-nm, 1 mA inverters and a 1000-ohm feedback resistor is selected. This inverter pair has a similar input resistance of 54.4 ohms, a combined voltage gain of 16.36 dB, and a noise figure of 2.062 dB at 800 MHz. In comparison, the selected single

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inverter results shown in Figure 2.5 and Figure 2.7 achieves a voltage gain of 8.15 dB and a noise figure of 2.117 dB. Therefore, under identical dc power and input impedance, the inverter pair topology delivers nearly double the voltage gain and slightly better noise performance, making it a more favorable choice for the design.

2.2.3 Input Stage Design

The noise analysis in the previous subsection highlights the inherent noise-canceling feature of the inverter amplifier pair topology. However, both simulation and calculations indicate residual noise power originating from the transistors that remains uncancelled and appears at the circuit's output node. This is due to the necessity of achieving adequate voltage gain from the auxiliary amplifier stage to fully nullify the noise contribution from the transistors of the core inverter amplifier, which can be derived as:

$$A_{\mathrm{v}} = -\frac{R_{\mathrm{f}} + Z_{\mathrm{s,input\ node}}}{Z_{\mathrm{s,input\ node}}} \tag{2.17}$$

where R_{f} is the feedback resistor of the core inverter amplifier and $Z_{\mathrm{s,input\ node}}$ is the impedance seen from the input node of the core inverter amplifier to the outside of the inverter. The necessary voltage gain of the auxiliary amplifier is the ratio of the noise voltage induced by the noise current of the transistors in the core inverter amplifier at the core inverter’s output and input nodes. This can be simply understood as a resistive voltage divider. In the inverter amplifier pair topology, the $Z_{\mathrm{s,input\ node}}$ comprises the parallel impedance of the 50-ohm source resistance and the input impedance of the other inverter amplifier. This parallel combination lowers the effective $Z_{\mathrm{s,input\ node}}$ and thereby increasing the necessary voltage gain for the auxiliary amplifier to achieve full noise cancellation criterion. As a consequence, the symmetrical architecture of the inverter amplifier pair topology involves trade-offs in the noise-canceling mechanism. Specifically, one inverter requires a higher auxiliary voltage gain to fully cancel its transistor noise power, which demands an increase in the feedback resistor of the other

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inverter in the pair. This results in a higher auxiliary voltage gain requirement for the auxiliary amplifier when it serves as the core amplifier in its noise-canceling scenario. According to the simulated and calculated voltage gain and feedback resistor values in the previous subsection, the voltage gain of an inverter amplifier is insufficient to meet the required criterion for their corresponding feedback resistor value. As a result, the circuit retains uncanceled residual noise power from the transistors.

In the proposed LNA in Figure 2.2, a hybridized approach is adopted. Based on the analysis in the previous subsections, noise reduction can be achieved in two ways. First, within a single inverter amplifier, noise performance can be improved by either increasing the feedback resistor or boosting the transconductance of the transistor, though this comes with higher power consumption and greater parasitic capacitance. Second, by incorporating an additional inverter amplifier stage in parallel, the noise-canceling mechanism further reduces the transistors' noise contribution to some extent. By leveraging these two methods, the proposed LNA incorporates three inverter amplifier blocks in parallel. In Figure 2.2 , Inverter 1 serves as the core amplifier stage, with a lower feedback resistor to achieve an input resistance around 130 ohms. The noise reduction for Inverter 1 relies on the smaller fully noise-canceling criterion, which could potentially be met by the combined voltage gain of the other two inverter amplifiers. With the core amplifier adding parallel input impedance, the feedback resistor of the auxiliary inverter pair can be further increased, resulting in boosted voltage gain, which is beneficial for the noise-canceling scenario of Inverter 1. The larger feedback resistor and higher biasing current also reduce the noise contribution of the auxiliary inverter amplifiers themselves, resulting in improved noise performance even if the fully noise-canceling criterion is not achieved.

Transistors with a gate length of 60 nm are selected to meet the aforementioned

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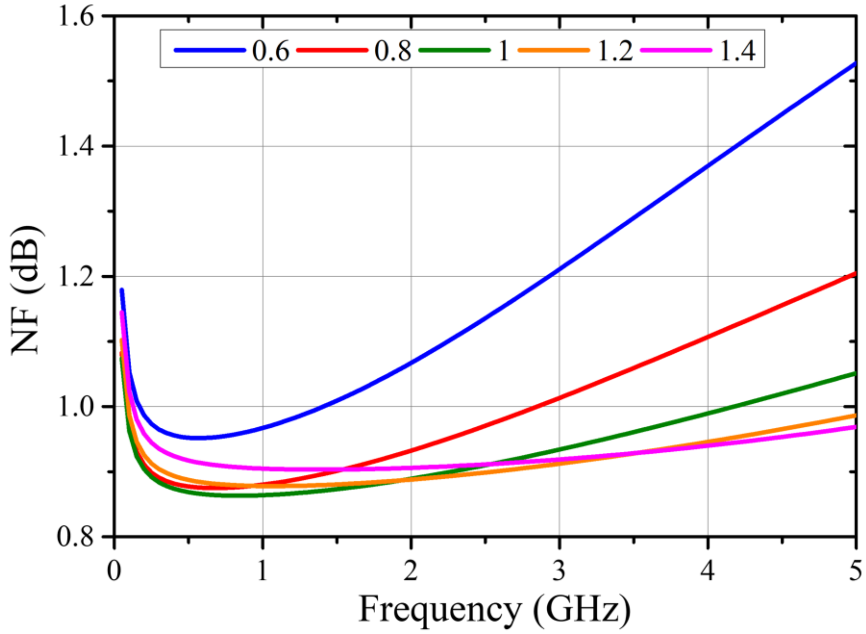

Figure 2.13: Simulated noise figure with varying gain coefficient for Inverter 2 and Inverter 3 at the combining stage, while maintaining unity gain for Inverter 1.

design criteria. Longer transistors have demonstrated superior performance in the analysis of inverter amplifier design discussed in the previous subsections. Additionally, as detailed in Sec. 2.1.2, when operating at cryogenic temperatures, shot noise becomes predominant in the noise behavior of an LNA. Longer devices inherently suppress shot noise by minimizing ballistic transport in the channel. All inverter amplifiers are self-biased with a 1 V supply voltage, maintaining a node voltage of 0.48 V at the transistors' drains. This selection ensures similar transconductance for both the pMOS and nMOS transistors under the same supply current.

2.2.4 Combining Stage

In the proposed LNA, the combining stage is achieved using common source amplifiers, where each amplifier also serves as the active load for the others. Consequently, the common source amplifiers of the three branches share a common load composed of their parallel output resistance. The voltage gain ratio between the branches at the combining stage depends solely on their relative transconductance. To verify the optimal gain ratio between each branch, the selected input stage is combined with an ideal

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voltage combiner with independently tunable gain coefficients for the three branches. Since only the relative gain affects noise performance, the combining coefficient for Inverter 1 is set to unity gain, while an identical variable relative gain coefficient is applied to both Inverter 2 and Inverter 3 at the combining stage.

Figure 2.13 shows the simulated noise figure of the overall circuit as the relative gain coefficient of Inverter 2 and Inverter 3 varies. The results indicate an optimal value of unity gain relative to that of Inverter 1. This optimal setting is due to a mutual canceling mechanism, akin to the trade-off discussed in the previous section, where attempts to achieve fully noise-canceling criteria by increasing the feedback resistor lead to corresponding heightened requirements of fully noise canceling for the other branch. Similarly, increasing the voltage gain at the combining stage for one branch enhances the noise-canceling effectiveness from the perspective of the other branches. However, it amplifies the noise power from its own output node due to the increased gain in the combining stage. Consequently, this reduces the extent to which noise power is canceled by the other two branches and results in degraded noise performance.

As a result, the device and biasing points for the common source transistors in the combining stage are selected to achieve identical transconductance, leading to different gate-to-source voltages applied to the pMOS and nMOS transistors. The gate length in the combining stage is chosen to be 40 nm, as shorter devices have lower parasitic capacitance that could otherwise impact the circuit's bandwidth. The biasing current is limited to approximately 1 mA per branch for Inverter 2 and Inverter 3, ensuring that overall power consumption remains below 10 mW before reaching the output driver.

2.2.5 Output Driver

The common source amplifier block is chosen as the output driver to maintain the voltage gain achieved in previous stages. Achieving near unity gain at this stage

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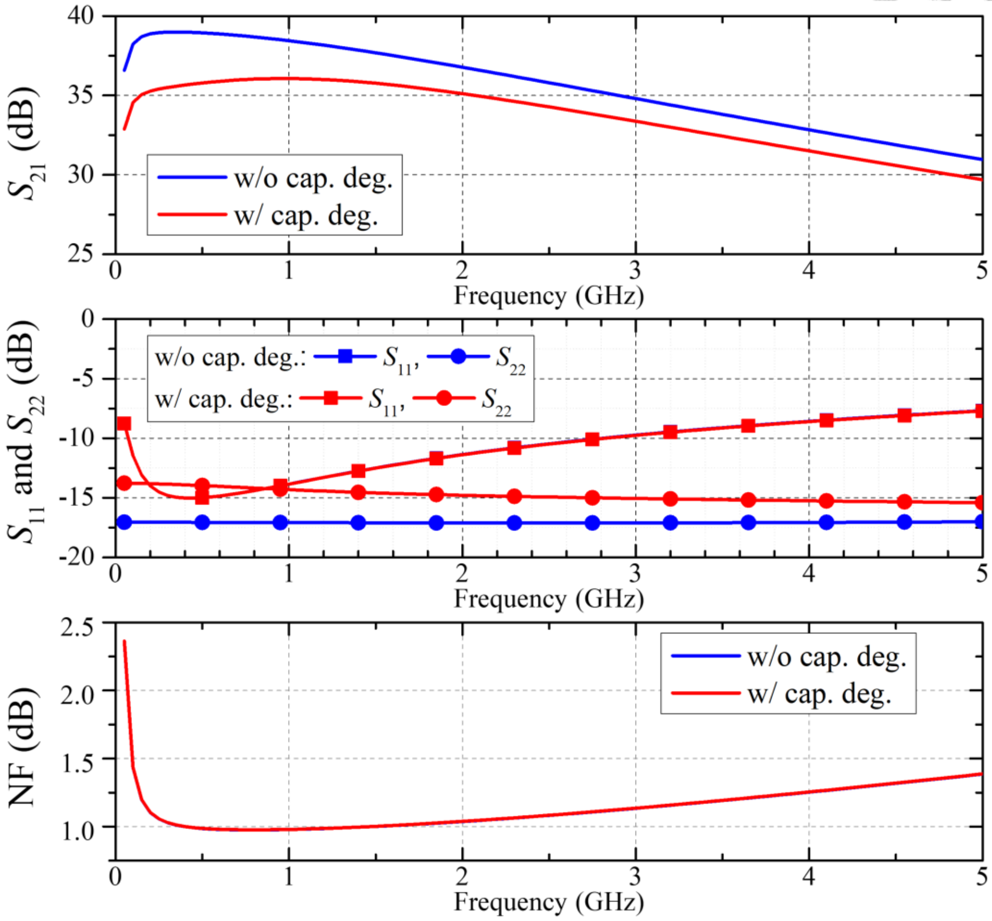

Figure 2.14: Pre-simulated responses of the proposed LNA with and without adopting the capacitive degeneration technique at the output driver stage.

necessitates a large transconductance to effectively drive the small loading impedance. Therefore, a transistor with a 40 nm gate length is selected to meet the circuit's bandwidth requirements, while also minimizing additional parasitic capacitance, as also considered in the combining stage. Additionally, capacitive degeneration is implemented at the output driver stage, as depicted in Figure 2.2, to further enhance the circuit's 3-dB voltage gain bandwidth.

Figure 2.14 compares the pre-simulated responses of the proposed LNA with and without the capacitive degeneration technique. This technique involves introducing a parallel RC pair at the source of the common source transistor. At low frequencies, the degenerated capacitor remains nearly open, causing source degeneration by the resistor and reducing the low-frequency voltage gain. As the frequency increases, the capacitor

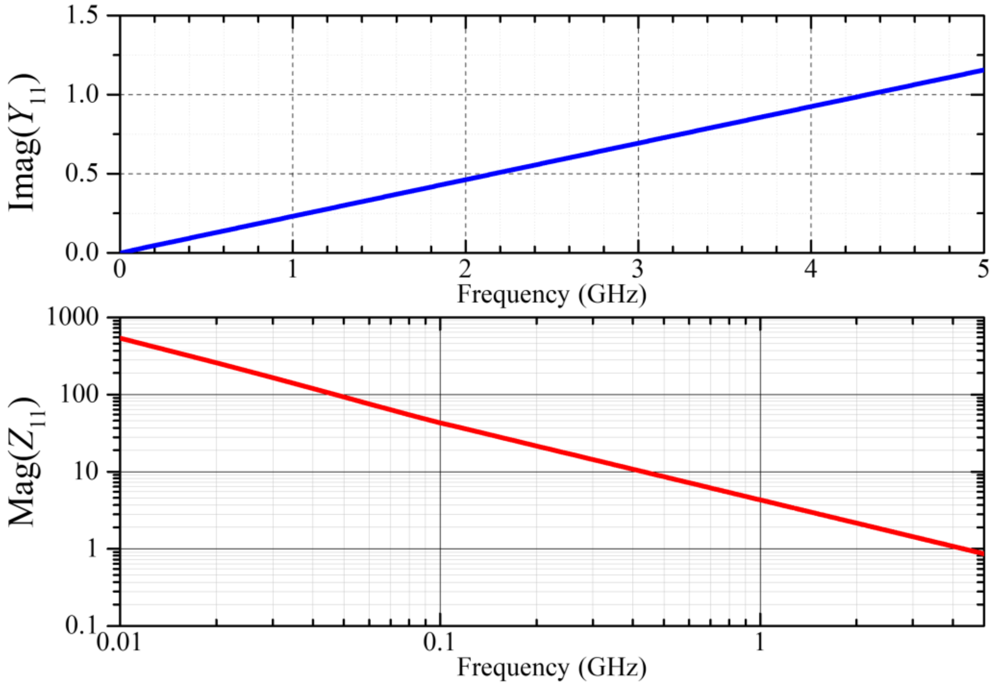

Figure 2.15: Simulated responses of the on-chip bypass networks.

starts to bypass the resistive degeneration, restoring the original gain level, thereby resulting in a flattened voltage gain response as shown in Figure 2.14. Considering only the drain capacitance, the common source stage with capacitive degeneration can be derived as:

$$A_\mathrm{v} = -\frac{g_\mathrm{m}R_\mathrm{d}}{1+g_\mathrm{m}R_\mathrm{s}}\frac{1+sR_\mathrm{s}C_\mathrm{s}}{(1+sR_\mathrm{d}C_\mathrm{d})(1+s\dfrac{R_\mathrm{s}C_\mathrm{s}}{1+g_\mathrm{m}R_\mathrm{s}})} \tag{2.18}$$

where R_d, C_d represent the loading resistance and capacitance seen at the drain of the transistor, respectively. The first term in the voltage gain pertains to a common source amplifier with resistive source degeneration. The capacitive degeneration technique introduces an additional zero and a higher pole compared to that originating from the drain capacitance. It's noteworthy that the reduced gain level and deviated output return loss seen between the two cases in Figure 2.14 are attributed to the different operating point of the transistor. This difference arises because the transistor's size and supply voltage remain unchanged in the simulation when the degeneration resistor is included.

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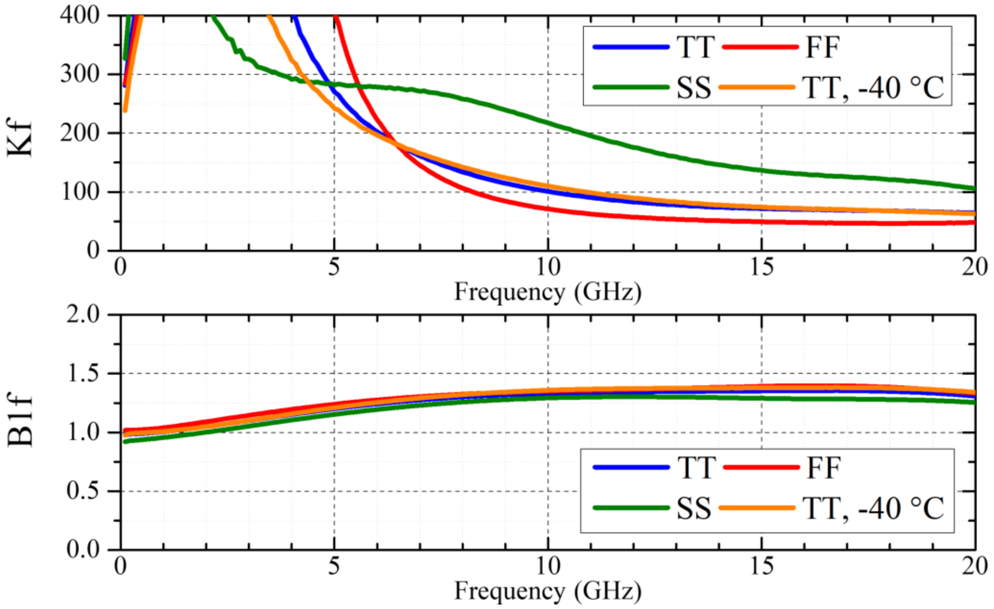

Figure 2.16: Post-simulated stability results of the proposed LNA across various process corners and temperatures.

2.2.6 On-Chip Bypass Networks and Circuit Stability

Owing to the low operating frequency range, the proposed LNA requires a sufficiently large on-chip bypass capacitance to provide an ideal RF-grounding node at the source of the pMOS transistors. The on-chip bypass networks consist of staggered routing lines from metal 1 to metal 9, sequentially connecting to the supply voltage and ground, functioning similarly to a cross-type inter-digitated capacitor. Figure 2.15 illustrates the simulated responses of an array of bypass network unit cells, segmented due to the limited resources in EM simulations. Each of the six supply voltage branches within the proposed LNA is routed to the dc pads through its own bypass network. From the simulated imaginary part of the *Y* parameters, the capacitance value of the bypass network is estimated to be around 36.8 pF. The simulated magnitude of the *Z* parameters indicates an equivalent impedance of the on-chip bypass networks to be over 10 ohms for frequencies below approximately 400 MHz. This results in some non-idealities in the on-wafer measurements, as discussed in the next section.

The stability of the proposed LNA is examined with various approaches. Firstly,

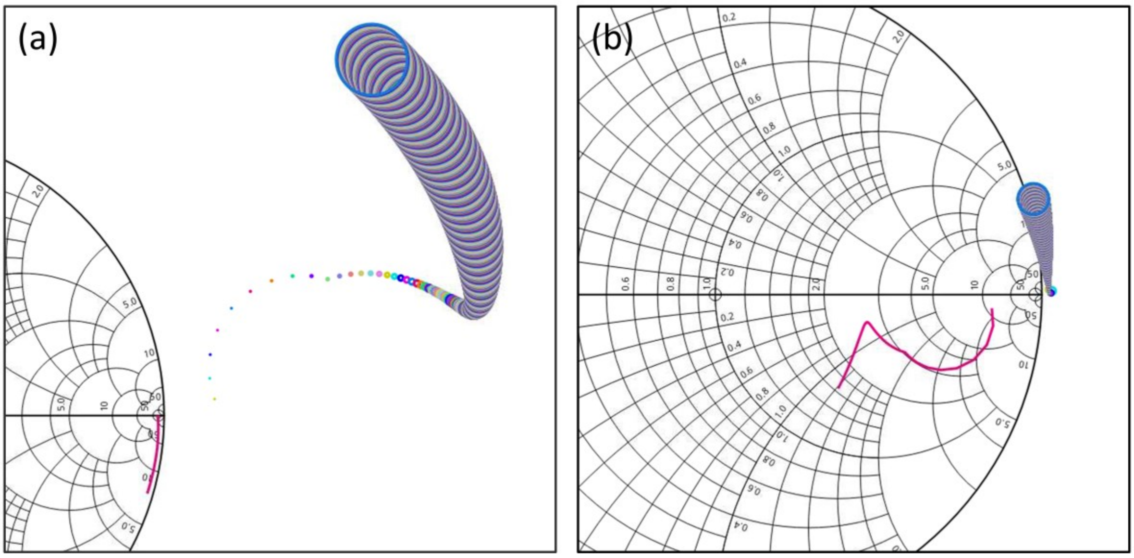

Figure 2.17: Inter-stage stability simulation of the proposed LNA. (a) Load stability circles of the input sub-section and S_{11} of the output sub-section with a 50-ohm load resistance. (b) Source stability circles of the output sub-section and S_{22} of the input sub-section with a 50-ohm source resistance.

two-port validations are conducted with the K factors and the B_1 factors across various process corners and also at a temperature of -40 °C. The post-simulation results in Figure 2.16 shows two-port unconditional stability of the proposed LNA within 20 GHz, with the K factors over unity and B_1 factors above zero.

To further verify the circuit stability, the proposed LNA is separated into two sub-sections at the combining node before the dc blocking capacitor of the output driver stage. Figure 2.17 illustrates the simulation results of the inter-stage stability check of the proposed LNA. Due to the lack of simulation tools in Cadence Virtuoso for examining return loss with varying load (source) impedance, the corresponding return loss is simulated assuming a 50-ohm load (source) impedance. The simulation results, without any intersection within 20 GHz, ensure the inter-stage stability of the proposed LNA.

The intricate structure of the input parallel inverters and the common-source combining stage makes inter-stage stability analysis challenging. Therefore, an experimental simulation of loop gain and loop gain phase is performed within the input

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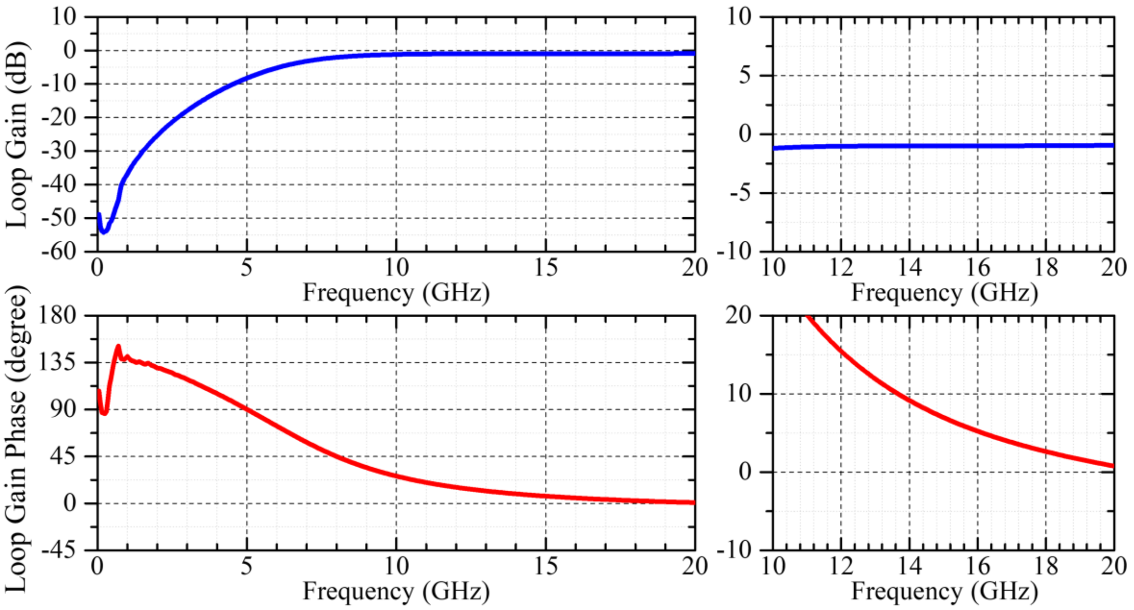

Figure 2.18: Post-simulation results of loop gain and loop gain phase of the input sub-section of the proposed LNA.

sub-section. To achieve this, a current probe is inserted connecting the drain node of the three inverters and the input nodes of the dc blocking capacitors in the three branches, effectively breaking all loops within the input sub-section. Figure 2.18 depicts the simulated loop gain and loop gain phase of the proposed LNA. Within the bandwidth of interest, the input sub-section of the circuit exhibits a loop gain lower than unity and a loop gain phase above zero degrees. At higher frequencies, the loop gain tends to saturate at a certain lower-than-unity value, ensuring the circuit stability within the loops in the input sub-section.

In summary, various methods have been evaluated to ensure the stability of the proposed LNA. Although transient response analysis and other techniques could also be applied, the methods described above effectively confirm the circuit's stability at a fundamental level.

2.3 Experimental Results

The proposed cryo-CMOS LNA is implemented using TSMC 40-nm CMOS process. In the post-simulation, the transmission line routings and RF pads are EM simulated using

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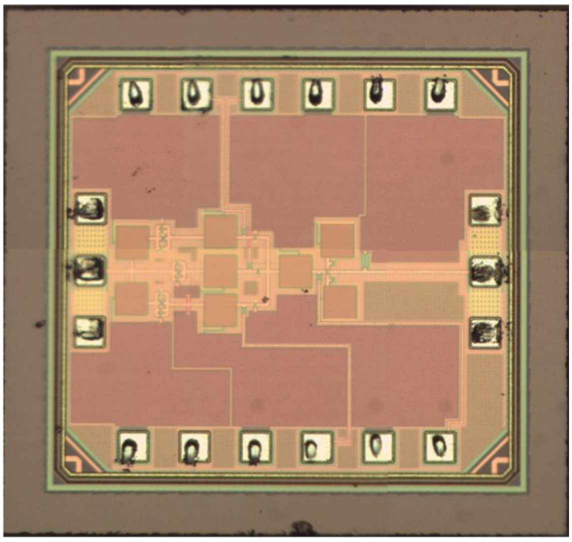

Figure 2.19: Chip photograph of the proposed cryo-CMOS LNA.

Sonnet, while the capacitors and resistors within the circuit are simply modeled using the compact models provided by the manufacturer. Figure 2.19 illustrates the chip photograph of the implemented circuit, with a total chip area of 0.52 mm^2 (755 µm × 691 µm), including the testing pads.

At room temperature, the bare die of the implemented circuit is measured using both dc and RF probes. Figure 2.20 shows the measured and post-simulated *S*-parameter responses of the proposed cryo-CMOS LNA. For better comparison, post-simulation results in both the TT and SS corners are included. The recorded biasing current during measurements indicates that the fabricated circuit is closer to the SS corner. Nonetheless, the measured data in the figures within this section is from the results obtained after fitting the biasing current to the simulation results in the TT corner by tuning the supply voltage of the circuit during the measurements. The measured *S*-parameter responses in Figure 2.20 generally match well with the simulation results, with only a few deviations. Firstly, the measured circuit exhibits higher roll-off in the gain response, which may indicate the presence of unmodeled capacitance within the circuit or parasitic capacitance differences across the corners. At frequencies below 500 MHz, ripples appear in both the transmission and input return loss responses. This is attributed to the lack of on-chip bypass capacitance,

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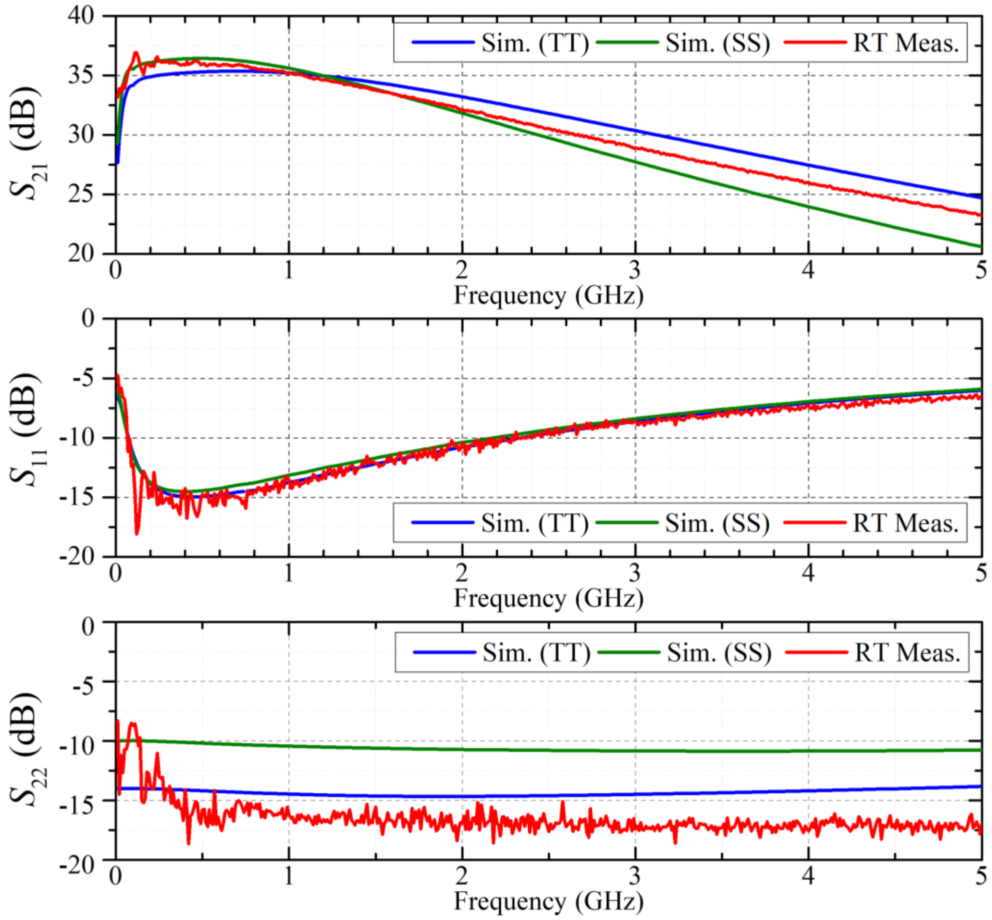

Figure 2.20: Measured and post-simulated (in TT and SS corners) *S*-parameter responses of the proposed cryo-CMOS LNA.

as our EM simulation shows that the effectiveness of on-chip bypass network only extends down to around 400 MHz. Furthermore, the dc probes used in the measurements have an RC series bypass network installed only on the output-port-related VDD 6 path. The lack of an off-chip bypass network for the input-port-related parts of the circuit results in a grounding condition at the source of the pMOS transistors different from that expected in the simulation, leading to the observed ripples. For the output return loss responses, although the dc probe incorporates the on-probe RC series bypass network, the measured results at low frequencies suggest that the electrical routing for the on-probe bypass network is too long, causing the inductance along the path to choke the effectiveness of these bypass devices. The improved output return loss level compared to the simulation is due to the off-chip series resistor used along the VDD6 path behind the

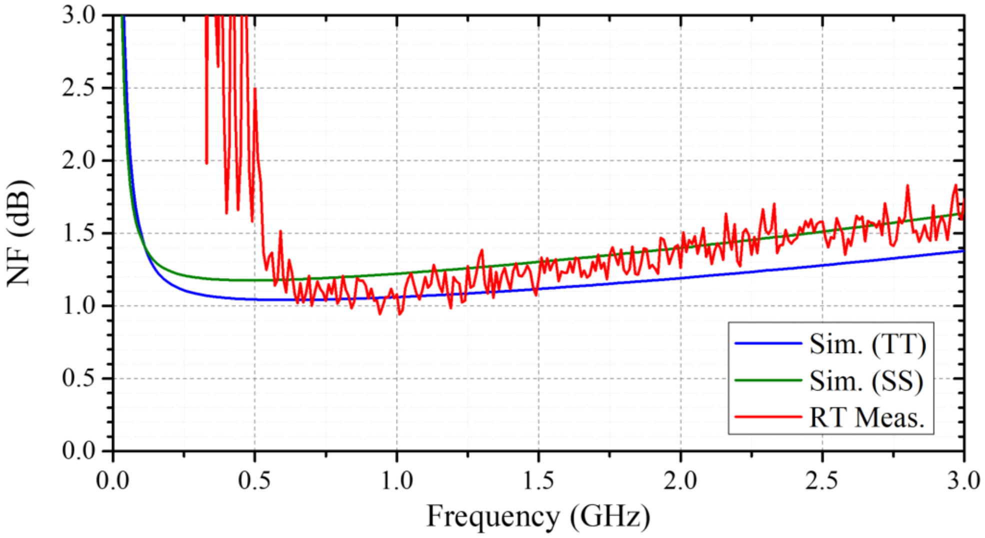

Figure 2.21: Measured and post-simulated (in TT and SS corners) noise figure of the proposed cryo-CMOS LNA.

dc probe during the measurements. This resistor alters the operating point of the output driver stage transistor, even after fitting the supply current. As a result, the output resistance of the transistor changes, affecting the output return loss level.

Figure 2.21 shows the measured noise figure of the proposed LNA using both dc and RF probes at room temperature. The measured results align well with the simulation for frequencies above 500 MHz. The slight increase in the noise figure compared to the simulation in the TT corner at higher frequencies is attributed to a similar reduction in gain response due to unmodeled capacitance. Below 500 MHz, the measured noise figure of the implemented circuit rises sharply compared to the simulation results. This increase is speculated to have two causes. The first is insufficient on-chip bypass capacitance, which leads to suboptimal grounding at the source of the pMOS transistors. As shown in Figure 2.22, adding RF chokes at the source of the pMOS in the simulation results in an increase in noise figure at frequencies below 150 MHz, in addition to the original flicker noise. Interestingly, the simulation also highlights the bypass issue observed in the *S*-parameter responses. A peak in the gain response and a non-flat output return loss, both seen in the measured results, are found in the simulation when RF chokes are added before

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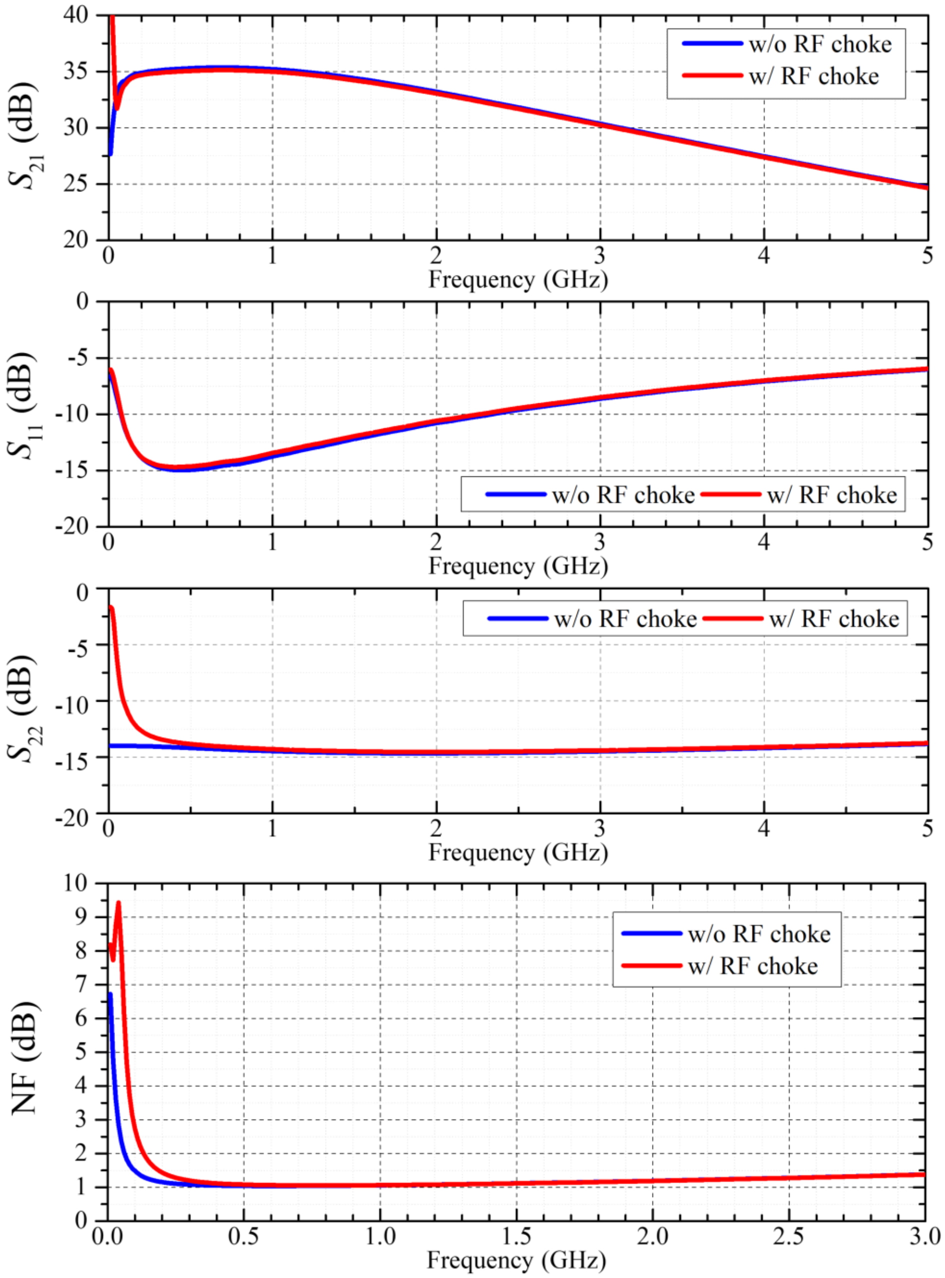

Figure 2.22: Comparison of post-simulation results of the proposed cryo-CMOS LNA with and without RF chokes before the ideal supply voltage source.

the ideal supply voltage source. The other potential cause of the increased noise at low frequencies might be radio and RF interference in the environment. Since the measurements were not conducted in a shielding room, radio and RF signals from various sources could be received by the dc wires in the setup, which act as low-efficiency antennas. These interferences are easily amplified by the high gain of the LNA, causing fluctuations within the circuit. Evidence of this includes the peaks around 2.4 GHz and

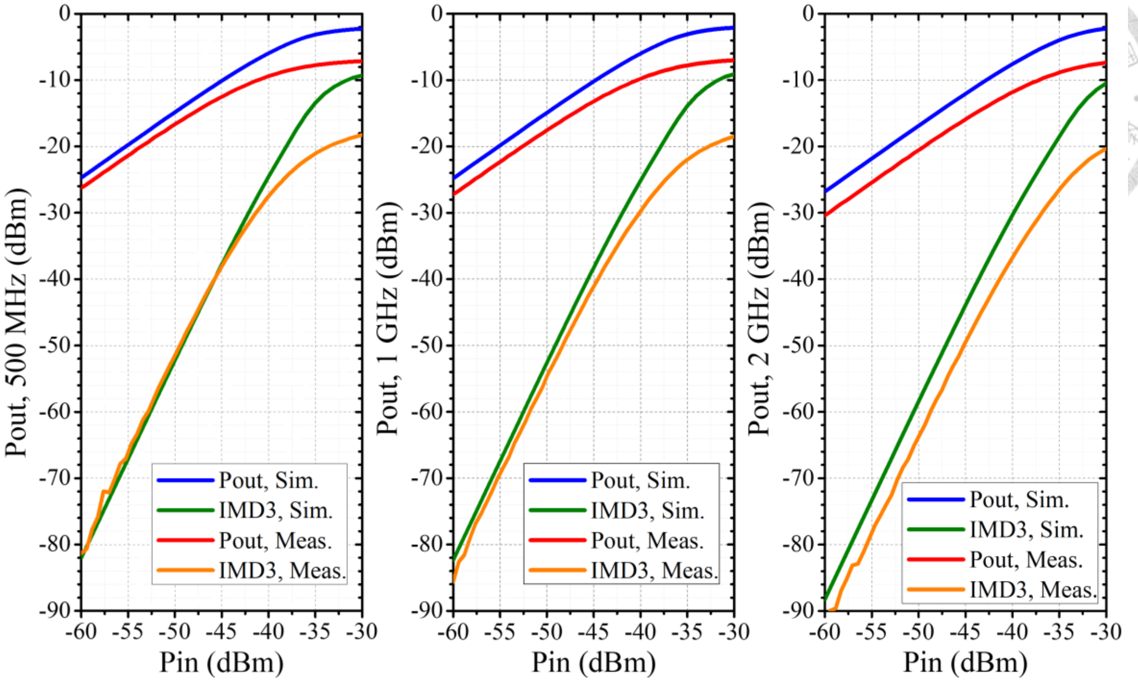

Figure 2.23: Measured and post-simulated (TT) large signal results of the proposed cryo-CMOS LNA at 500 MHz, 1 GHz, and 2 GHz.

900 MHz that occasionally appear during noise figure measurements. Additionally, the two highest peaks at around 90 MHz and 210 MHz in the measured noise figure results may also support this hypothesis. Nonetheless, the origin of the increased low-frequency noise and the corresponding solution to address the issue still require further research.

The large signal behavior of the circuit was also measured by probing the bare die at room temperature. Figure 2.23 compares the measured and post-simulated large signal results at 0.5, 1, and 2 GHz. In the simulation, the input P1dB values are -40.88 dBm, -40.75 dBm, and -38.84 dBm at these frequencies. The measured results are slightly lower at -46 dBm, -44.5 dBm, and -41.5 dBm, respectively. For the input IP3, the simulation shows values of -31.36 dBm, -31.24 dBm, and -29.3 dBm, while the implemented circuit exhibits similar values of -32.1 dBm, -31.03 dBm, and -27.8 dBm at 0.5, 1, and 2 GHz, respectively. The resulting deviations might be attributed to the corner differences, as the post-simulation results shown here are for the TT corner. Despite the slight degradation measured, these values are still significantly higher than the input signals in targeted spin

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qubit reflectometry applications.

2.4 Summary

In this chapter, a novel cryo-CMOS LNA is proposed for reflectometry readout in spin qubit applications. The proposed topology introduces additional inverter amplifiers in parallel at the input stage, offering several advantages. Firstly, paralleling the inverter amplifiers allows for a larger feedback resistor, thereby increasing gain and reducing the noise contribution of each individual amplifier. Additionally, the combination of parallel branches enhances the overall gain of the LNA. Moreover, this configuration at the input node enables noise-canceling characteristics among the three inverter amplifiers, resulting in a significantly reduced noise figure within the limited power budget. By utilizing common-source amplifiers at the combining stage and the output buffer, the voltage gain of the LNA can be maintained or further amplified. Additionally, this approach reduces the effective noise contribution from both the combining stage and the output buffer.

Table 2.1 compares the proposed LNA with several state-of-the-arts reported in the literature. Among these, [5, 35, 51-53] are specifically designed for cryogenic operation in reflectometry readout of spin qubit systems. Although there is still some issue in the measurement of the proposed LNA, the performance listed in Table 2.1 neglects those low-frequency deviations.

When compared to other works at room temperature, the proposed LNA demonstrates superior gain performance and achieves a near-1-dB noise figure with minimized power consumption. This results in the highest figure of merit among the reported works at room temperature. Although the bandwidth of the circuit is reduced after implementation and the linearity degrades within the topology, it remains sufficient for the targeted application. Notably, when integrated within an SoC, the power

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consumption of the proposed LNA can be further reduced to approximately 10 mW when excluding the output driver stage.

Despite demonstrating a proof of concept with the implemented circuit in this chapter, several practical issues have led to less than ideal results in the measurements. Specifically, the low-frequency noise problem requires further investigation. Additionally, cryogenic measurements of the proposed circuit have been paused due to technical challenges. Further research on the circuit is therefore left as future work.

Table 2.1: Comparison of RT and cryogenic LNAs.

Ref.	Tech.	Temp.	BW (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Pdc (mW)	FoM[a]
[27]	65-nm	RT	0.5-7	16.8	2.87-3.77	-4.5	11.3	12.57
[23]	65-nm	RT	0.04-2.9	20	2-2.5	-5	29	4.66
[24]	180-nm	RT	0.4-0.8	17.4	1.35-1.57	-5.11	16.8	-6.3
[28]	65-nm	RT	0.02-2.6	12.8	1.56-2.42	1.2-3.6	6	12.82
[35]	160-nm	RT	dc-0.4	40[b]	0.8-1.1	-29	45.9 (80[b])	7.86[b]
		4 K	dc-0.5	50[b]	0.1	-47	54.9 (91[b])	37.5[b]
[5]	22-nm	RT	0.1-0.6	27	<3	-	1.4	18.1
[51]	40-nm	RT	0.01-2.7	25.6	0.63-1.4	-6	43.4	17.61
		4 K	0.01-3	29	0.033-0.8[c]	-	19.4	55.14
[52]	40-nm	RT	0.05-3.8	27	1.16-2.2	-20	22.6	21.68
		4 K	0.02-4	30.2	0.29-0.91	-	10.8	44.79
[53]	40-nm	RT	0.01-1.9	28	1.16-1.7	-18.6	17.6	18.95
		4 K	0.01-2.6	31	0.1-0.48	-	8.6	53.26
This work	40-nm	RT	0.01-1.75	36	1.04-1.35[d]	-32.1	14.65	28.9

[a] $\mathrm{FoM} = 20\cdot\log_{10}\left(\frac{\mathrm{Gain[lin]}\times\mathrm{BW[GHz]}}{P_{dc}\mathrm{[mW]}\times(\mathrm{NF[lin]}-1)}\right)$

[b] With three cascaded following amplifier stages.

[c] Measured in [52].

[d] Neglecting the low-frequency noise deviation.

Chapter 3 Design of a Broadband SP4T Switch for Cryogenic Measurement and Calibration

3.1 Introduction

In this chapter, a dc to 67 GHz single-pole-four-throw (SP4T) switch is presented. The circuit was designed to serve as one of the key improvements to the cryogenic measurement and calibration system discussed in subsequent chapters. The switch design follows a systematic procedure, utilizing LC-ladder low-pass filter theory. This approach can be extended to design various broadband single-pole-multi-throw switches with precise control over circuit responses. The following subsections provide a brief introduction to the broadband and cryogenic switches reported in the literature.

3.1.1 Literature Review of Broadband RF Switches

Due to their simplicity and importance in integrated circuit systems, switch circuitries are frequently studied across various emerging solid-state technologies. While switches are also utilized in other systems as building blocks, this subsection primarily focuses on studies of broadband RF switches, which are indispensable components in modern communication systems.

For the early studies of RF switches in CMOS technologies, [54] offers a comprehensive overview of this area. The main challenge in broadband CMOS switch design lies in the tradeoff between on-resistance and off-capacitance, which directly affects insertion loss and isolation. Studies such as [55] and [56] have attempted to optimize transistor layout, thereby reducing the associated bandwidth-limiting capacitance and high-frequency loss. In the early stages of bulk CMOS technologies, the impact of substrate resistance on isolation and insertion loss is discussed in [57]. The later triple-well process provides a well-controlled environment for achieving high body resistance and body bias, making it a more standard design choice.

Given the demands of modern communication system development, achieving high linearity has also become a key focus of research. Several techniques have been developed to mitigate the impact of the unintentionally activated junction diodes, which can degrade the power handling capability of the switches. The concept of body-floating technique bootstraps the biasing point of the bulk, thereby keeping the junction-to-body diode off. A LC-tuned method was introduced for the early bulk CMOS device in [58], but the inherently narrowband characteristics make it unsuitable for use in wideband switches. After the triple-well process matured, the resistive body-floating method became widely adopted [55, 59]. The double-well body-floating method was subsequently proposed to additionally protect the substrate-deep-N-well diode [55, 56, 60]. To further increase the power handling capability, the P-well body was negatively biased through the floating resistor in [59] and [61]. A switched body floating technique was implemented in [56], trying to increase isolation by reducing coupling capacitance when series transistors are turned off. However, this approach degrades insertion loss at high frequencies. In addition to improving the structures of transistors and preventing junction diodes from turning-on, a more straight-forward method is by expanding the voltage swinging range of the device. In contrast to III-V compound semiconductor processes, which inherently possess high breakdown voltages, the supply voltage of CMOS technologies decreases with newer processes, presenting an increasingly challenging task to achieve high linearity. The transistor-stacking method has become increasingly popular in recent research, which divides the voltage across each transistor, thereby enhancing the overall power handling capability [62, 63].

Topologically, instead of simple series or shunt switches in the early studies, a series-

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shunt section is highly popular owing to its compact size and good balance between isolation and insertion loss [63, 64]. To increase the bandwidth, inductors were often added to realize matching networks with the shunt transistors, forming a T-section or π-section artificial transmission line [57, 59, 60, 65, 66]. For RF/microwave communities, the travelling-wave concept was implemented in broadband switches, which could be conceptualized as a series of artificial transmission line sections [67, 68]. For multi-throw switches, two methods were adopted for controlling different branches. In [67] and [69], quarter-wavelength transmission lines were added in front of the traveling-wave structures, transforming the low impedance of the on-resistance, connected to ground, to a high impedance, nearly open, thus not affecting the on-branch response. However, the bandwidth of the switches would be constrained by the quarter-wavelength transmission lines. To achieve a broadband response from dc, series transistors were introduced to replace the quarter-wavelength transmission line, albeit at the cost of increased insertion loss [61, 62, 70].

The performance of switches in standard CMOS technologies is inherently limited due to the trade-off between on-resistance and off-capacitance, as well as the lower supply voltage headroom. In recent years, an increasing number of broadband switches have been reported in CMOS SOI processes, aiming for significantly lower insertion loss and higher operating frequencies [63-66, 68, 69]. The buried oxide layer and the smaller junction diodes reduce capacitive coupling from diffusion to substrate, thereby improving bandwidth and insertion loss. However, the low breakdown voltage still limits the power handling capability. Several prototypes have been developed using various compound semiconductor processes, including GaAs pHEMT [70], SiGe BiCMOS [71], and GaN HEMT [72]. Additionally, the integration of phase change materials into semiconductor processes as replacements for transistors in switch circuit cores has emerged as a new area of research [73]. These technologies offer inherent high linearity and improved insertion loss, making them primary focuses of current and future research.

3.1.2 Literature Review of Cryogenic RF Switches

In comparison to reports at room temperature, there have been considerably fewer demonstrations at cryogenic temperatures. An early experiment in [74] introduced a non-reflective SP4T switch in the ABCS InAs/AlSb HEMT process. However, the switch was designed for a relatively low bandwidth of 5 GHz and was only tested at a rather high temperature of 90 K. [75] presents measurement data at a temperature of 78 K for the same switch discussed in [64], illustrating the variations in circuit characteristics observed in SOI technologies under cryogenic conditions. A more recent study in [76] demonstrates an ultra-broadband SPST switch fabricated in 22 nm FDSOI CMOS, tested both in room temperature and 2K temperature.

For more inspiring research in cryogenic and quantum-computing-related circuitries, a team from Imec and KU Leuven has published a series of studies on measuring superconducting quantum devices using semiconductor IC multiplexers. In [77], they introduced the initial version of the SP4T reflective multiplexer in the 28 nm HPC+ process, functioning at room temperature and at a temperature of 32 mK. To showcase the application of cryogenic multiplexing, they conducted measurements on superconducting resonators and confirmed that the residual heat dissipation of the multiplexer did not affect the resonator characterization during the extraction experiments. Identifying the primary source of power leakage as the ESD clamping transistors, an improved version of the multiplexer was presented in [78]. With just 4 ESD cells, the 1.4 μW multiplexer was dispersively coupled to the readout resonator of the transmon qubits. The experiments revealed the thermal noise photons generated by the multiplexer decreases T_2^e of the qubit, while T_1 barely changed. A more thorough analysis of the impact of the multiplexer on superconducting qubits was discussed in [79]. The dynamic and static power consumption of the multiplexer was extracted to estimate the targeted power budget for scaling up qubit channels. Time-division multiplexing experiments were also conducted to demonstrate the influence of active window of the multiplexer on qubit fidelity. These reports illustrate the feasible integration of solid-state IC multiplexer into the futuristic realm of quantum computing systems. However, the reported multiplexers primarily focused on aspects such as power budget and port-to-port isolation within a restricted frequency range of 10 GHz. In the following sections, a broadband SP4T switch is proposed using a systematic design approach aimed at enhancing overall bandwidth and circuit response. Without adding any ESD cells, the switch consumes only 0.6 μW of static power, making it suitable for operation at the base-temperature in dilution fridges.

3.2 Circuit Design

The broadband SP4T switch proposed in this section is designed for multiplexing usage at the base temperature in dilution fridges. The design prioritizes achieving the widest available bandwidth while ensuring acceptable insertion loss and at least 35 dB of isolation within the 4 to 8 GHz operational frequency range of the cryogenic measurement and calibration system. Although power handling capability is not a primary specification for this application, the design also addresses linearity improvement through the transistor configuration discussed in the following subsection.

3.2.1 Transistor Configuration

As discussed in Sec. 3.1.1, several early studies explored the influence of the layout configurations to parasitic capacitance. While we were unable to customize the transistor structure, conventional techniques have been developed with advancements in CMOS technology, particularly towards the standard triple-well process. The inset of Figure 3.1

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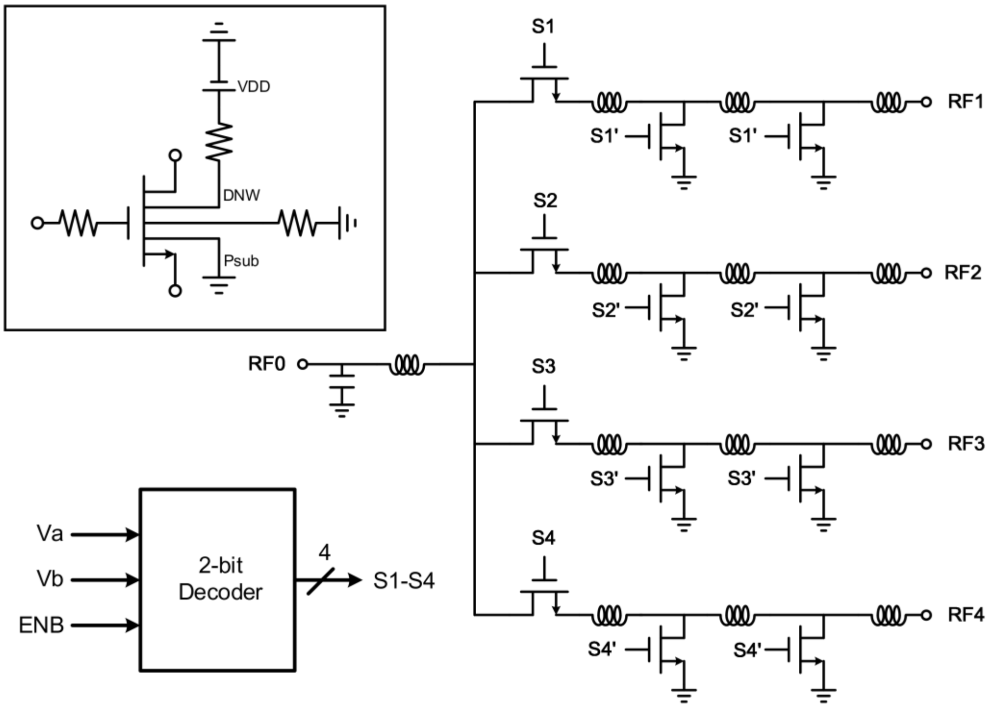

Figure 3.1: Schematic diagram of the proposed SP4T switch.

depicts the configuration of the core transistors of the switch circuitry. Utilizing the available RF transistors with the standard triple-well process, the double-well body-floating technique was applied, and a large gate resistor was added to prevent high-frequency signal leakage. The technique connects the deep n-well (DNW) and the body of the transistors to the ground and VDD, respectively, through a large resistor. This configuration improves the linearity of the switch and creates a high-impedance body, preventing capacitance coupling loss to the lossy p-substrate as seen in bulk CMOS. However, the technique creates a series capacitance of C_{db} and C_{sb} when the series transistors are turned off. To achieve the targeted overall isolation, shunt transistors are necessary. However, without using the stacking method, which degrades insertion loss and bandwidth, adding shunt transistors inevitably sacrifices linearity from the unwanted self-biasing effect. Nevertheless, the double-well body-floating technique was still adopted because it creates a well-controlled environment for the high-frequency signals in the transistors.

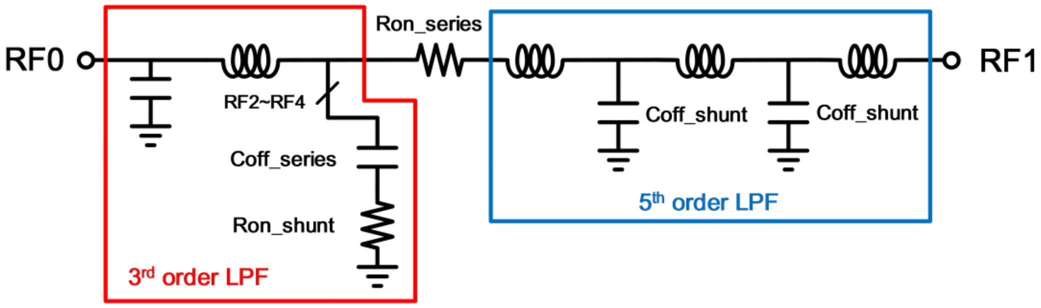

Figure 3.2: Equivalent circuit model of the proposed switch (activating RF1).

3.2.2 Circuit Schematics

Figure 3.1 illustrates the schematic diagram of the proposed SP4T switch. A 2-bit decoder is integrated to reduce the number of required input controlling pads. Additionally, a separated supply voltage ENB is included, which can be turned off to bypass this digital circuitry. As discussed in the previous subsections, each of the four branches comprises a series transistor along with the requisite shunt transistors. The series transistors facilitate operation bandwidth starting from dc. To enhance overall high-frequency performance, matching sections are required at the input and output of each branch. The subsequent subsection delves into the trade-offs associated with device selection and presents a systematic analysis for designing single-pole-multi-throw switches.

3.2.3 Design Procedure

The equivalent circuit model of the proposed SP4T switch, when activating RF1, is depicted in Figure 3.2. In the RF1 branch, the off-state shunt transistors are simplified as shunt capacitance, while the series transistor is represented by a small resistor. The parallel off-state branches of RF2 to RF4 are modeled as an off-state capacitance of series transistor connecting a small on-resistance of the shunt transistors to ground. This equivalent circuit model simplifies the on-state response of a single-pole-multi-throw broadband switch into three parts: the left-hand-side (LHS) input matching section, a small series on-resistance, and the right-hand-side (RHS) output matching section that utilizes the shunt capacitance of the off-state shunt transistors. For the off-state response, isolation is determined by the on-resistance in the off-state branches.

The proposed design procedure can thus be divided into three steps. Begin with the design of the RHS output matching section, which involves the selection of the size and the number of the shunt transistors. In this step, a distinctive analysis of the matching section is proposed, utilizing LC-ladder low-pass-filter (LPF) theory. Secondly, determine the size of the series transistors based on the on-state response. Lastly, design the LHS input matching section, incorporating the off-state capacitance from the previously selected series transistors. The subsequent subsections delve into the details of each step in the design process.

3.2.3.1 RHS Output Series-First LC LPF

In the conventional series-shunt topology, the output matching section typically consists only of an output inductor and the shunt transistor, forming an LC matching section. This configuration is often referred to as an artificial transmission line in some literature. In microwave communities, the concept of the artificial transmission line has further evolved into the traveling wave structure, which essentially comprises a series of multi-sections of artificial transmission lines.

From a different perspective within LC-ladder filter theory, the interpretation of LC-section artificial transmission lines or traveling wave structures can be collectively referred to as a constant-k low-pass filter. This concept clarifies the confusing calculation involved in the well-known inductance value equation:

$$Z_0=\sqrt{L/C} \tag{3.1}$$

where Z_0 is the characteristic impedance of the system, L is the inductance added. For an LC-section, which is a series-shunt half-section in the constant-k filter interpretation,

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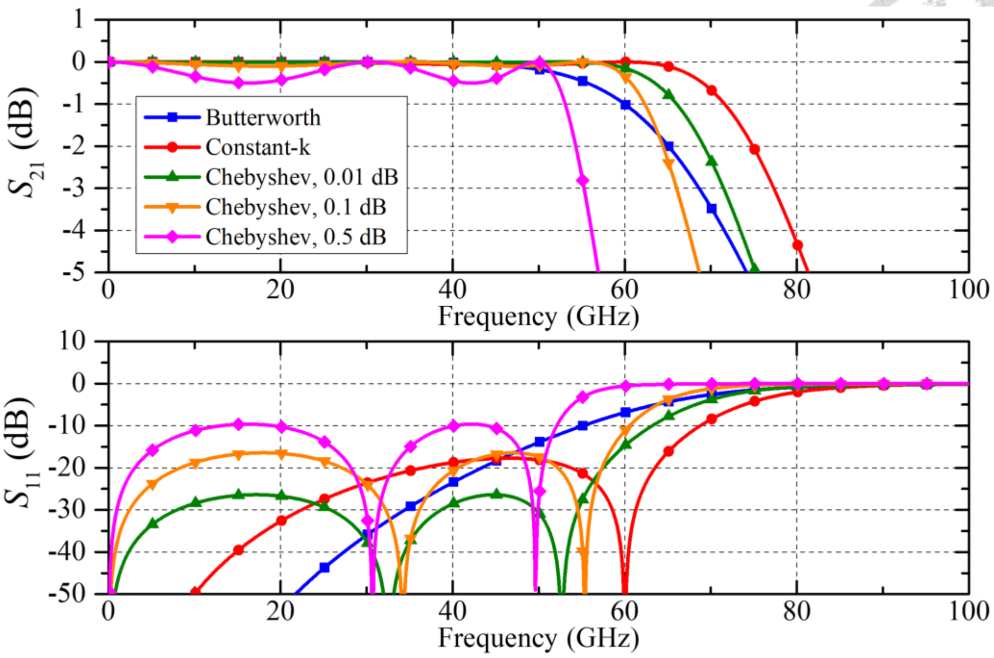

Figure 3.3: Simulated responses of the series-first fifth-order LC-ladder LPFs.

the value of C is straightforwardly taken as the off-state capacitance of the shunt transistor. However, in the calculation of traveling wave structures, the value of C used for calculating L depends on the defined unit cell. For a traveling wave series starting with a series inductor, the unit cell resembles a mid-series section of the constant-k filter. Here, the value of C used in the calculation remains the same as the off-state capacitance of the shunt transistor. Conversely, for the mid-shunt section, which constitutes the unit cell of the traveling wave series starting with a shunt capacitor, the value of C used is half of the off-state capacitance. The choice of unit cell results in a significant difference in the cut-off bandwidth, which can be calculated as:

$$\omega_{\mathrm{c}} = 2/\sqrt{LC} \tag{3.2}$$

When considering the same off-state capacitance value, the inductance needed from a mid-shunt section is four times that required from a mid-series section. As a result, the cut-off bandwidth achievable using a mid-shunt section is halved compared to a mid-series section.

The interpretation of artificial transmission lines as constant-k filters thus extends

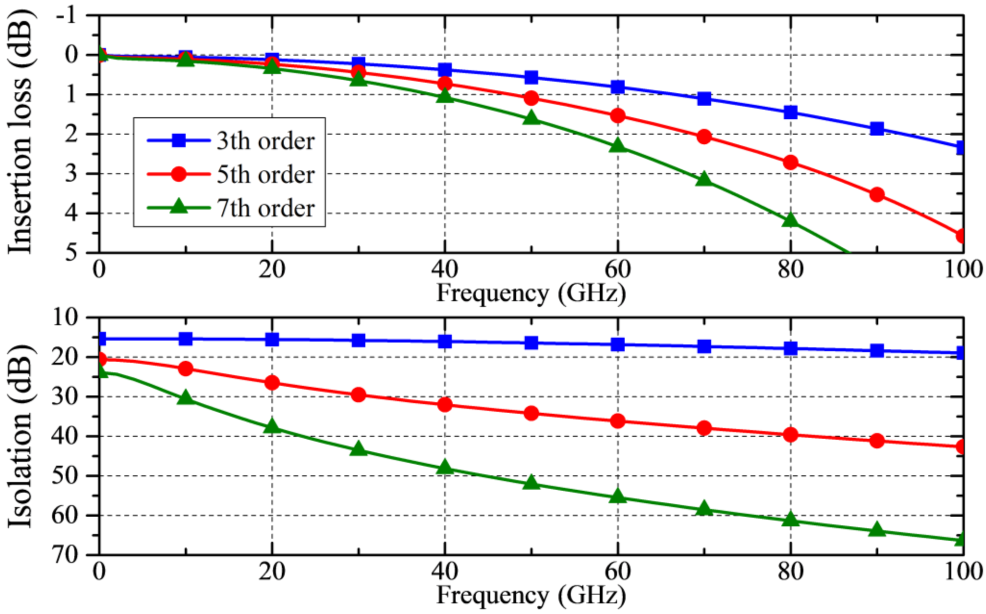

Figure 3.4: Simulated responses of RHS output series-first constant-k filters with different numbers of shunt transistors (different orders of constant-k filters).

the versatility of the design approach, utilizing other types of LC-ladder low-pass filters. Figure 3.3 illustrates five selected cases of series-first fifth-order LC-ladder low-pass filters, all with the same capacitance values. The series-first configuration facilitates using inductors as the connection both preceding the output matching section and to the output pad afterward. The fifth-order constant-k filter comprises two mid-series sections, while the LC-ladder values for the other four filter types are determined using coefficients from [80]. Both the Butterworth filters (maximally flat filters) and the odd-number-order Chebyshev filters offer the advantage of having a load impedance magnitude equal to that of the source, and their coefficient values are symmetric, which simplifies the design complexity. In alternative design scenarios, other types of filters tailored for specific purposes—such as minimal phase shift, passband ripple control, or group delay requirements—can be custom-designed using conventional LC-ladder low-pass filter theory. The primary objective of this work is to achieve the widest operational bandwidth, which leads to the selection of the series-first constant-k filter as the output matching structure.

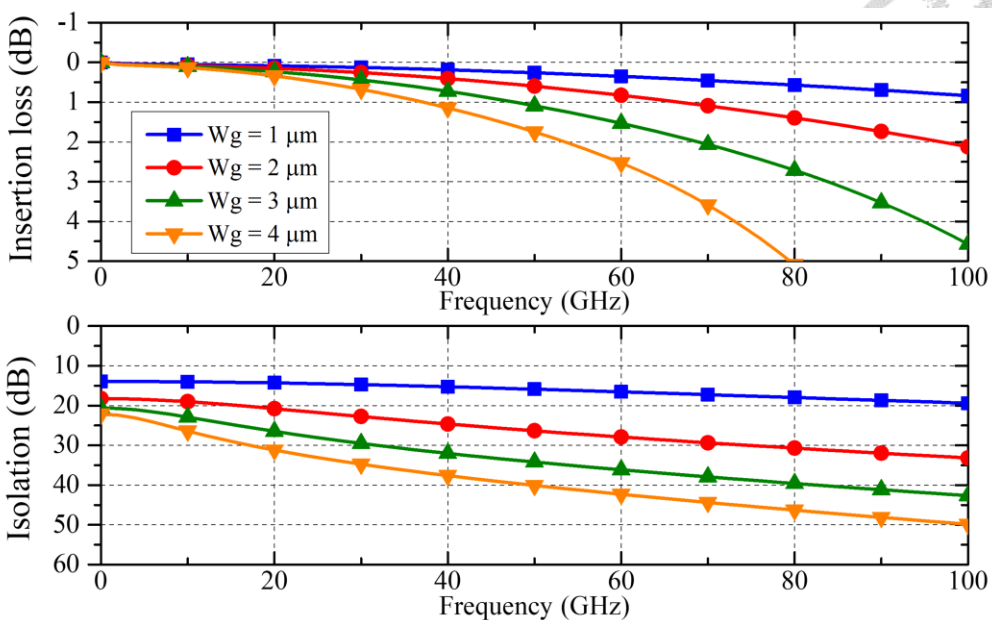

Figure 3.5: Simulated responses of RHS output series-first fifth-order constant-k filters with different shunt transistor widths.

The size and number of shunt transistors involve trade-offs between isolation, bandwidth, and insertion loss. Figure 3.4 illustrates the insertion loss and isolation of the series-first constant-k filters with different orders. Ideally, as the filter order increases, the bandwidth slightly expands. However, in practice, the insertion loss in higher frequency ranges degrades due to the presence of more lossy elements along the signal path. Conversely, increasing the number of shunt transistors enhances isolation by providing more shunt connections to the ground. The responses of varying shunt transistor widths are depicted in Figure 3.5. The larger device provides a smaller shunt on-resistance to the ground, creating a more ideal isolation between the output and input ports. On the other hand, the smaller transistor introduces less parasitic capacitance in the transistor off-state, thereby increasing the overall bandwidth, which could be calculated using Eqn. (3.2). The selection of the size and number of shunt transistors depends on the design specifications. Typically, isolation is a more significant consideration, as the primary bottleneck for a single-pole-multi-throw switch is usually at the input matching section.

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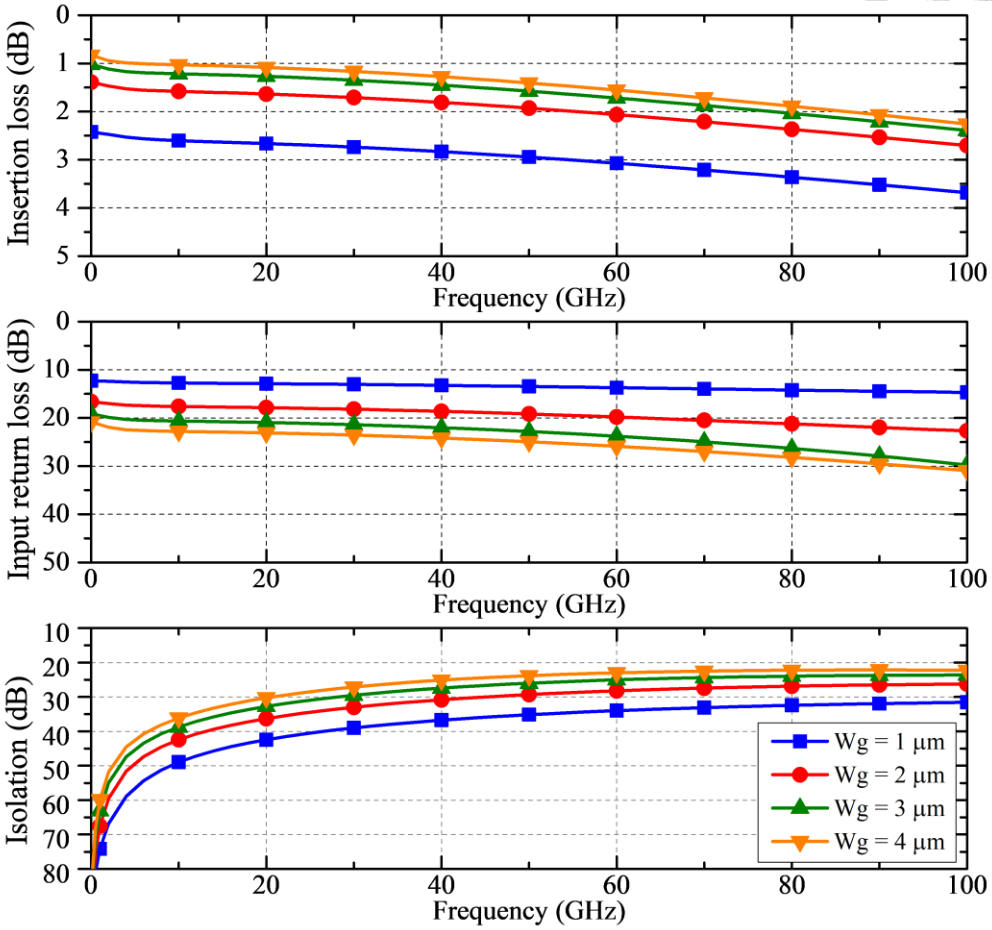

Figure 3.6: Simulated responses of a single branch with varying widths of series transistors connected to the RHS output series-first LC LPF.

3.2.3.2 Series Transistors

After designing the RHS output series-first LC LPF, the next step is to determine the size of the series transistors. Figure 3.6 illustrates the simulated responses of different widths of the series transistors connected to the previously designed RHS output LC LPF. The larger gate width of the transistor, the smaller the series on-resistance, leading to better matching and less penalty on the level of insertion loss. However, as the size of the transistor increases, the off-state series capacitance through the floating body also increases, leading to a degradation in isolation. Simultaneously, the shunt capacitance looking into an off-state branch also rises, which worsens the overall bandwidth of a single-pole-multi-throw switch. Figure 3.7 depicts the imaginary part of Y_{11} of the SP4T switch, activating only the RF1 port, without the inclusion of any input matching circuitry.

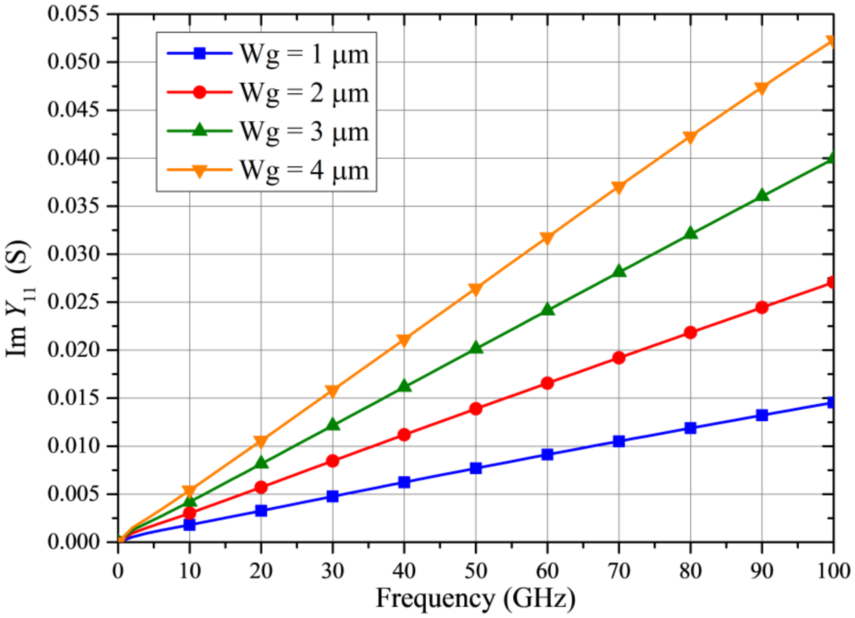

Figure 3.7: Imaginary part of Y_{11} of the SP4T switch (activating RF1) without input matching circuitry, while varying the widths of the series transistors.

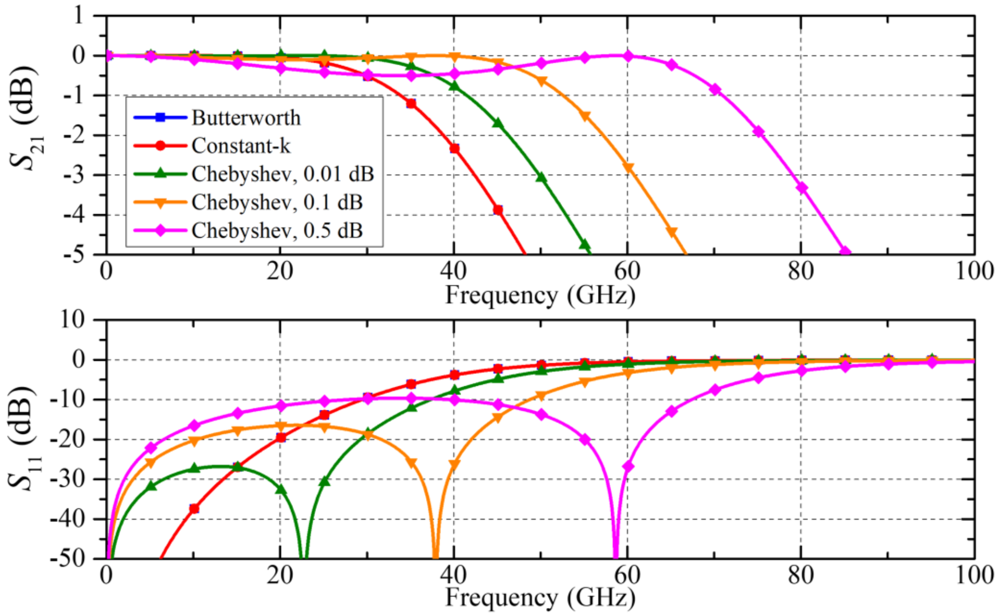

Figure 3.8: Simulated responses of the shunt-first third-order LC-ladder LPFs.

The overall response of the non-input-matched SP4T switch can be simplified to an ideally shunt capacitance, the value of which can be easily calculated using the extracted imaginary part of Y_{11} at a certain frequency point. The larger gate width of the series transistors thus results in a larger shunt capacitance, which in turn limits the achievable bandwidth of the LHS input matching circuitries.

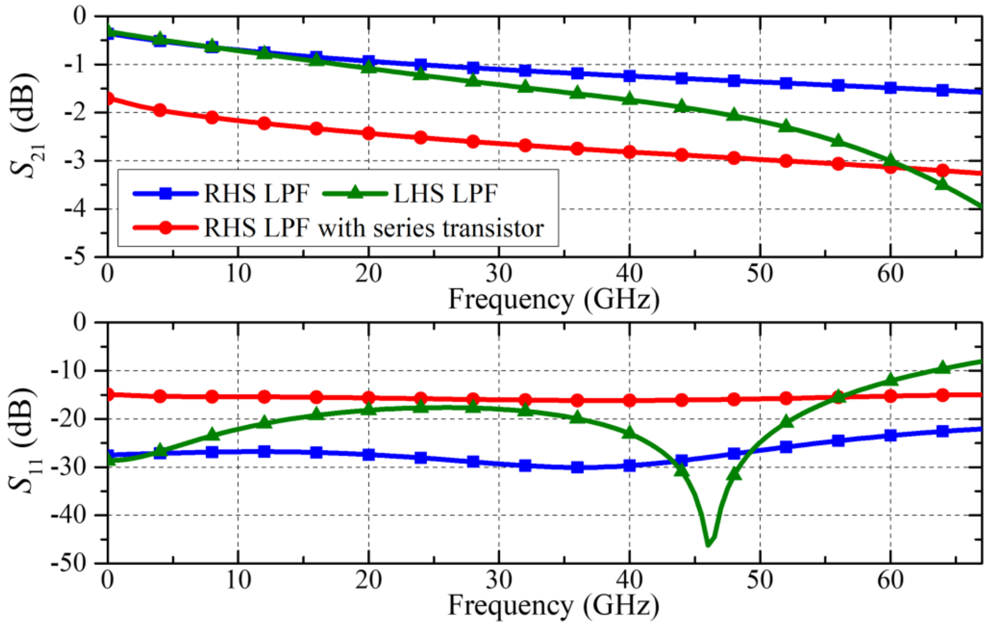

Figure 3.9 : Post-simulated responses of the RHS LPF, the LHS LPF, and the RHS LPF with the series transistor.

3.2.3.3 LHS Input Shunt-First LC LPF

The final stage of the switch design concludes with the LHS input matching section. With the extracted pseudo shunt capacitance in the previous step, a shunt-first LC low pass filter is proposed for the input matching design under the similar line of thought in Sec. 3.2.3.1. A shunt capacitor and a series inductor are added in front of the SP4T switch, consisting of the LHS input shunt-first third-order low-pass filter. Similarly, the responses of the five selected types of LC-ladder LPFs are depicted in Figure 3.8 with the same capacitance value. In contrast to the series-first case, the Chebyshev filters in this scenario offer a wider bandwidth but come with the trade-off of in-band ripple. The excessively increased ripple affects the input return loss, ultimately reducing the effective operational bandwidth. The overall bandwidth performance of the SP4T switch is limited by the input shunt-first low pass filter, due to the larger parallel capacitance of the four branches compared to the shunt capacitance of a single transistor in each branch.

Figure 3.9 illustrates the post-simulated responses of the RHS output series-first LPF, the series transistor with the RHS output series-first LPF, and the LHS input shunt-first

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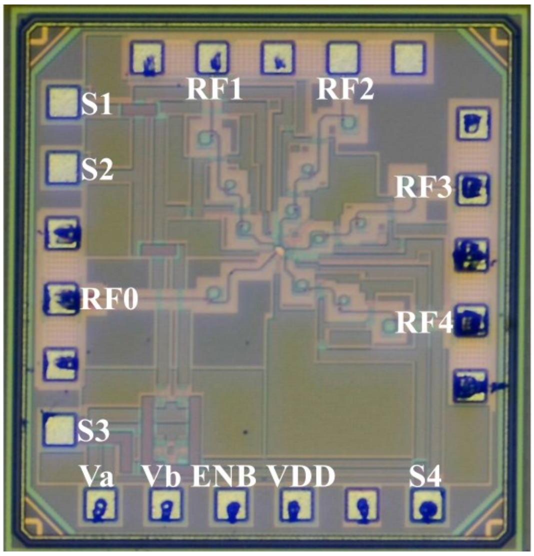

Figure 3.10: Chip photograph of the proposed SP4T switch.

LPF. All the metal routings, RF pads, inductors, and the capacitor in the LHS input LPF are EM simulated. According to the post-simulation results, the LHS input LPF not only limits the overall bandwidth but also contributes nearly 4 dB insertion loss at higher frequencies. This is attributed to the large shunt capacitance of the structure at the combining node of the four branches. When comparing the two cases of the RHS output LPF, with and without the series transistor, the inclusion of the series transistor degrades the overall insertion loss response by approximately 1.5 dB and also deteriorates the return loss due to the series resistance within the transmission path.

In summary, with the aforementioned design approach, a desired response of a single-pole-multi-throw broadband switch can be synthesized through a methodical and systematic procedure that utilizes conventional LC-ladder low pass filter theory.

3.3 Experimental Results

The proposed broadband SP4T switch is implemented in TSMC 40-nm CMOS process. Figure 3.10 shows a chip photograph of the fabricated switch. All the five ports from RF0 to RF4 are connected to GSG pads, enabling the integration with the measurement and calibration system discussed in the following chapters. As depicted in

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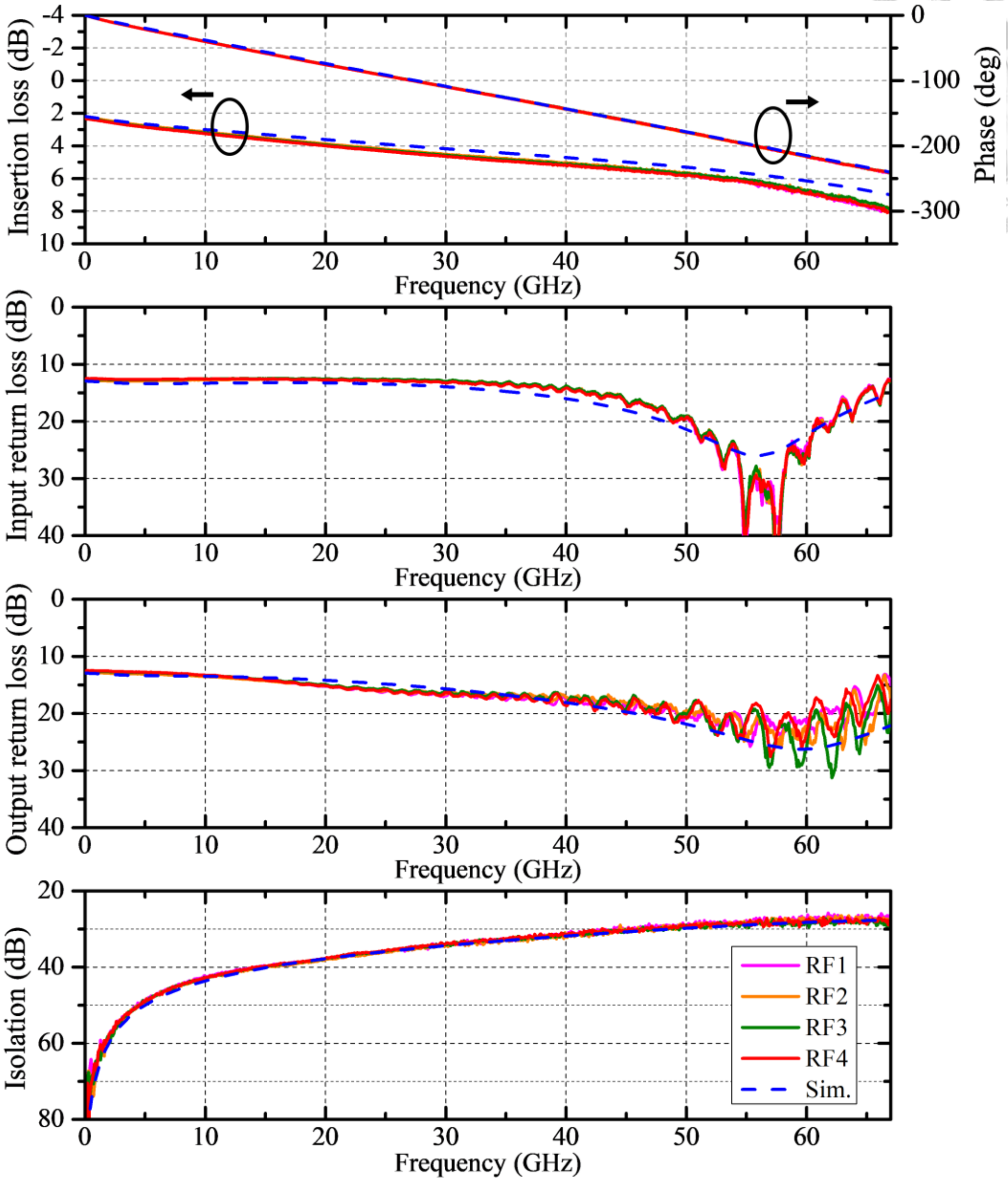

Figure 3.11: Simulated and measured *S*-parameter results at room temperature.

Figure 3.1, the control of the SP4T switch is managed by two logical input, Va and Vb, through an integrated 2-bit decoder, which operates with a separated supply voltage ENB. The logical control through the decoder can be bypassed by disabling ENB and directly inputting the state of the four branches through S1 to S4 pads. The total chip area including testing pads is 0.6 mm^2 (764 µm × 809 µm).

3.3.1 Room Temperature Measurement Results

The bare dies of the proposed switch are measured with both dc and RF probes at room temperature. Due to the limitation of the three-port *S*-parameter calibration standard substrate, the measurement is conducted using three RF GSG probes. One probe contacts RF0, while the other two probes are positioned on the upper and right sides, contacting RF1 or RF2 and RF3 or RF4, respectively. The two non-contacted off-state ports are left open during the measurement. Bias-tees are added after the three probes, providing a 0 V dc level along the signal path to ascertain the state of the switch and the value of parasitic junction capacitance.

Under the described measurement setup, Figure 3.11 compares the simulated and measured responses of the SP4T switch. The measured insertion loss begins around 2 dB, consistent with the simulation, and degrades to slightly above 8 dB at 67 GHz. This is slightly lower than the post-simulation result, likely due to unaccounted losses in the lengthy signal path, considering the negligible difference in phase response. The switch exhibits an input and output return loss above 10 dB across the entire operational bandwidth for all four ports, which also aligns well with the simulation results. Both the measured and simulation isolation results are above 35 dB for frequencies below 30 GHz and remain above 28 dB up to 67 GHz. The high isolation ensures that there is no difference between the measurement results, where only three out of the five ports are probed, and the simulation when all five are terminated. The responses of the four branches align closely with each other, which can be attributed to the symmetrical layout planning. The consistent measured responses from different ports suggest that the switch is well-suited for its intended function of multiplexing in the calibration system, where variations between each electrical path represent the primary source of calibration error.

While linearity isn't a primary concern given the application scenario of a cryogenic measurement system, the power handling capability of the circuit is measured. Because of the high isolation of the switch and the simplicity of the setup, the measurement was performed using only two RF GSG probes: one for RF0 and the other to probe the

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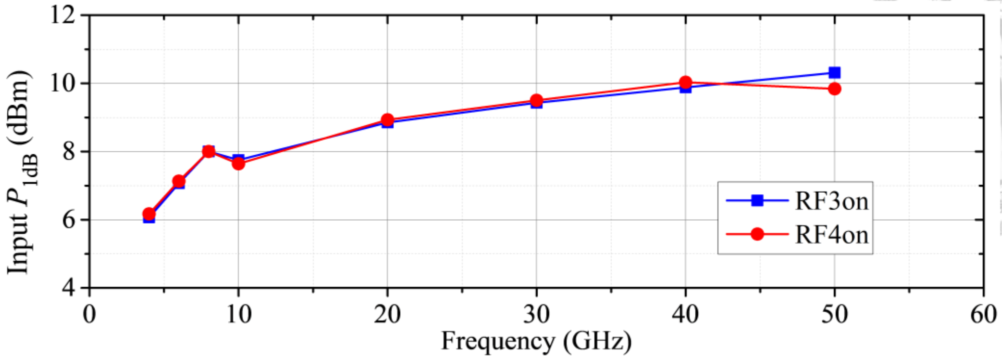

Figure 3.12: Measured input P_{1dB} at room temperature (activating RF3 and RF4).

activated RF3 or RF4, while the other three off-state ports remained unterminated. Figure 3.12 depicts the input P_{1dB} of the SP4T switch for various frequency points. In the low-frequency range of 4 to 10 GHz, where cryogenic measurements of superconducting devices typically be conducted, the input P_{1dB} exceeds 6 dBm. As the frequency increases, the input P_{1dB} also rises and saturates at around 10 dBm at 50 GHz. The measured results for RF3 and RF4 match each other, indicating the good symmetry in the switch.

3.3.2 4 K Temperature Measurement Results

The intended operating environment of the SP4T switch is at mK temperatures within dilution fridges. For a preliminary assessment at cryogenic temperatures, the switch is tested using a CRX-4K prober and a Keysight P5004A VNA at a temperature of 4 K. The prober setup includes only two RF GSG probes. Therefore, similar to the previous experiments at room temperature, the other three off-state ports are left open without termination or probing during the measurement. The measured responses of the SP4T switch at room temperature (RT) and 4 K temperature are illustrated in Figure 3.13. At 4 K temperature, the insertion loss notably improves thanks to the reduced resistivity of the metal routings, with only a slight deviation in the phase response. Furthermore, the slight decrease in the on-state resistance of the series transistor also enhances both the input and output matching. The high isolation response remains almost unchanged at 4 K

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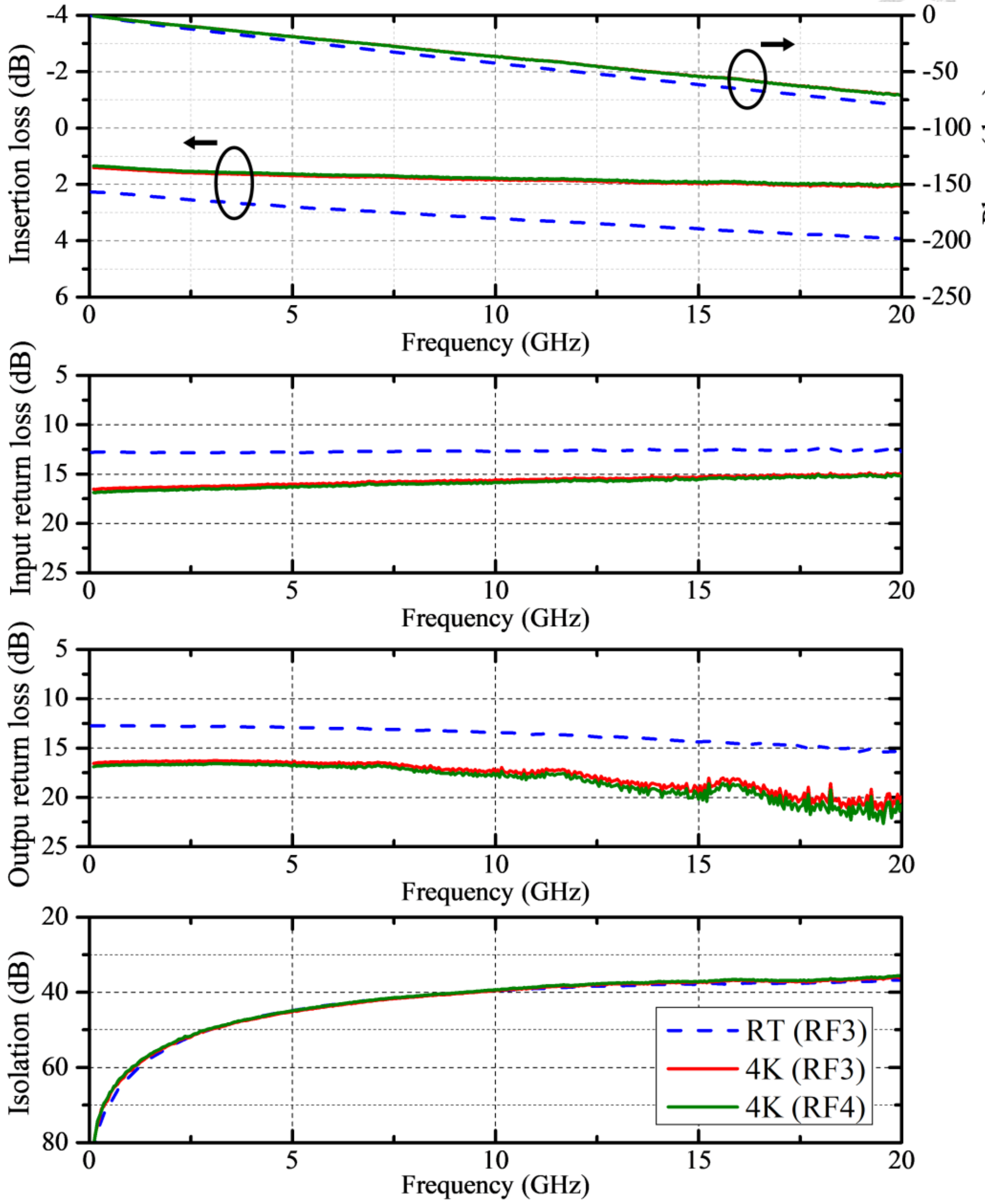

Figure 3.13: *S*-parameter results measured at RT and 4 K.

compared to room temperature. Additionally, the switch still exhibits high symmetry at 4 K temperature, with the responses of RF3 and RF4 closely overlapping, indicating its suitability for cryogenic temperature applications.

To ensure operation at millikelvin temperatures within the dilution fridge, the power leakage of the switch must not exceed the power budget of the cooling system at the base temperature, typically around 10 to 20 μW. In contrast to the multiplexers in [77-79], the proposed SP4T switch intentionally excludes ESD cells. This prototype switch enables testing of the power leakage of the core circuitry. Figure 3.14 displays the insertion loss

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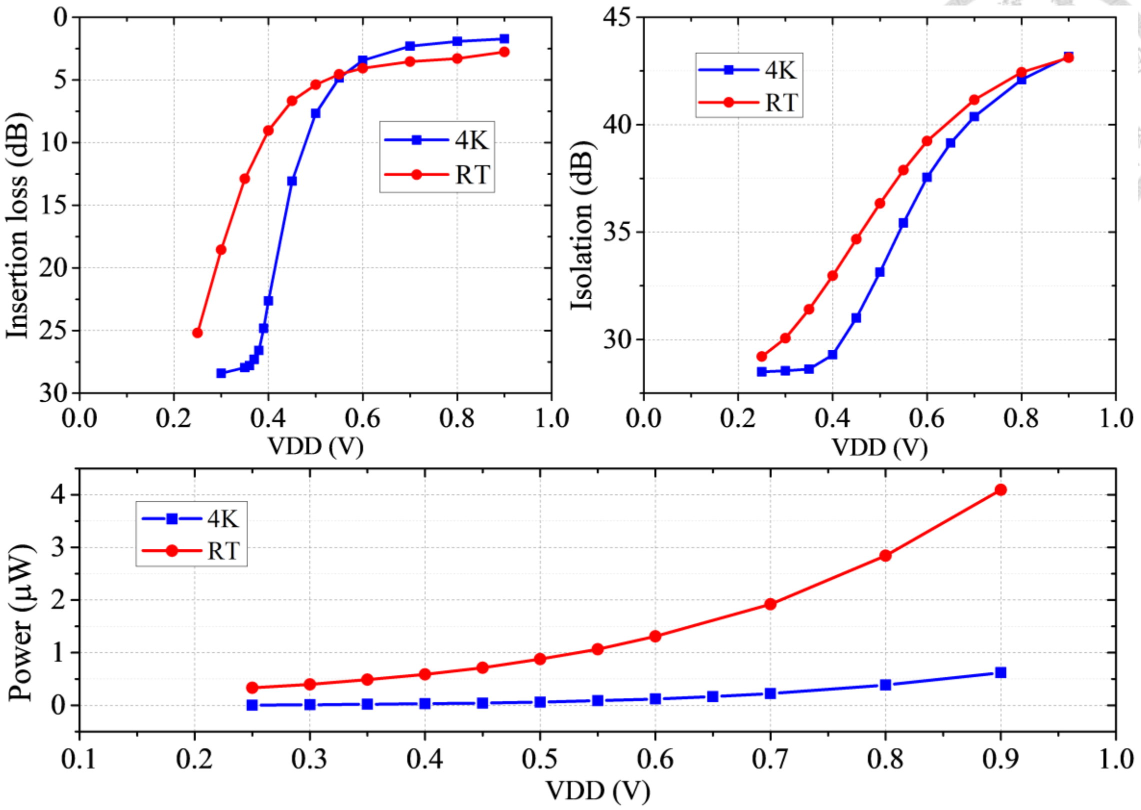

Figure 3.14: Power consumption, insertion loss, and isolation at 6 GHz for various supply voltages measured at RT and 4 K.

and isolation of the switch at both room temperature and 4 K temperature, with varying supply voltage. Additionally, the corresponding static power leakage of the switch is also measured using the Keysight B2901A SMU. At 4 K temperature, the measured insertion loss and isolation results suggest an anticipated rise in threshold voltage and a sharper closing behavior of the transistors. The static power leakage with a standard supply voltage of 0.9 V at room temperature is approximately 4 μW, but drops to only 0.6 μW at 4 K. The measured power is confortably below the budget limit, rendering the switch suitable for the cryogenic measurement applications at mK temperatures.

3.4 Summary

In this chapter, we present the design of a dc to 67-GHz 40-nm CMOS SP4T switch tailored for cryogenic measurement and calibration applications. Following a concise overview of the development and research in broadband and cryogenic switches, we

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propose a systematic analysis and a three-step design procedure for achieving desired responses in a single-pole-multi-throw broadband switch. This approach can be further adapted for other specialized specifications using established LC-ladder low-pass filter theory. At 4 K temperature, the implemented switch demonstrates insertion loss below 2 dB and isolation above 35 dB up to 20 GHz, with excellent symmetry among the four ports. Without the addition of any ESD cells, the chip exhibits a leakage of only 0.6 μW at 4 K, affirming its suitability for operation within cryogenic measurement systems at the base temperature of a dilution fridge.

Table 3.1 compares the proposed switch with other SP4T switches and multiplexers reported in the literature, considering their performance at either room temperature or cryogenic temperatures. To the author’s knowledge, the proposed switch is the first cryogenic broadband SP4T switch reported. At room temperature, compared to other broadband works, the proposed switch exhibits a much higher insertion loss. This discrepancy arises because all four output branches connect to the output pads, necessitating a larger chip area to accommodate a higher number of pads, thereby lengthening the RF routing path. Consequently, the lossy high-frequency routing degrades the insertion loss. The chips in [60, 66, 73] terminate two or three of the four output ports internally with on-chip loads, thereby reducing the overall area by using only one or two output pads and achieving a better reported insertion loss. Compared to the other cryogenic studies, the proposed design approach effectively broadens the operational bandwidth with minimal insertion loss, while also achieving superior isolation. The comparable power leakage of the proposed switch at a temperature of 4 K, compared to the reported static power at 10 mK in [79], confirms the feasibility of its operation and integration with the measurement and calibration system at the base temperature.

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Table 3.1: Comparison of RT and cryogenic SP4T switches and multiplexers.

Ref.	Tech.	Temp.	BW (GHz)	IL (dB)	Iso (dB)	IP_{1dB} (dBm)	DC Power (μW)
[60]	0.13-μm CMOS	RT	dc-70	<3.5	>25	9-10	-
[66]	0.13-μm SOI	RT	dc-50	<4.3	>27	>11	-
[73]	180-nm SiGe PCM	RT	dc-60	0.9	25	-	-
[74]	InAs/AlSb HEMT	90 K	dc-5	0.9	22	8	-
[77]	28-nm HPC+	32 mK	4-8	<3	>30	-	36.2
[78]	28-nm CMOS	10 mK	dc-10	-	>25	-	1.43
[79]	28-nm CMOS	10 mK	dc-10	<3	>30	-	0.6
This work	40-nm CMOS	RT	dc-67	<8	>28	10	4
This work	40-nm CMOS	RT	dc-20	<4	>37.6	9	4
This work	40-nm CMOS	4 K	dc-20[a]	<2	>36	-	0.6

[a] The provided VNA for 4-K measurements has a limited bandwidth of up to 20 GHz.

Chapter 4 Sample Holder Design and RF Characterization within Dilution Fridge

4.1 Introduction

The experimental setup for conducting quantum-related studies requires expertise across various fields, including cooling systems, vacuum systems, and mechanical and electrical engineering. In this chapter, our focus is on designing custom sample holders and exploring materials suitable for operation at cryogenic temperatures.

There are fewer studies reported in the literature regarding the details of sample holder design for quantum-related measurements [81-83]. However, as the demand for control and readout in massive qubit arrays increases, integrating traditional electronics and electrical designs for signal integrity becomes an ever-growing topic alongside the integration of the ultimate quantum system. In addition to literature studies, the commercially available Qboard from QDevil (Quantum Machine) in the lab provides comprehensive guidance on the requirements of the on-board system. The studies in this chapter thus attempts to improve and design for our custom specification, drawing insights from existing reports and commercial products.

All reported literature and the Qboard are primarily designed for spin qubit communities. For a general spin qubit control and readout platform, the system requires the following functionalities:

1. DC lines for energy level biasing.
2. High-frequency gate control lines up to approximately 6 GHz.
3. Microwave lines for frequencies in the tens of GHz range.
4. Low-frequency lines for lock-in measurements up to hundreds of kHz.

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5. High-frequency reflectometry lines up to around 3 GHz.

These specifications serve as a general guideline and may require adjustments based on specific design requirements. With such versatile on-board configurations, maintaining signal integrity between different functionalities is a significant challenge. This includes designing bias-tees, bypass and decoupling networks, and filtering circuitries, particularly in such a high-frequency and highly sensitive system. Apart from the electrical and microwave engineering aspects, designing the sample holder also entails ensuring mechanical compatibility and durability at cryogenic temperatures, along with meeting non-magnetic requirements and heat conductivity specifications.

In the earlier work reported in [81], a two-board configuration is proposed, featuring an additional ground-PCB to protect samples from ESD spikes. A cryostat-PCB serves as an interface, connecting the cables with MMCX-type connectors for up to 6 GHz bandwidth, and the dc line from nano-D connectors passes through on-board surface mount RC bias-tees to connect to the high-frequency lines. The interconnect includes mini-SMP bullets and connectors, with adhesive between the three boards. The device board features a multi-layer structure, including two paths for up to 40 GHz microwave signals, dc tracks with low pass filters, and high-frequency lines from the cryostat-PCB for control and tank-circuit readout. The paper primarily discusses the improved isolation achieved through fencing vias, although degradation from inter-layer coupling of overlapping traces from a common ground plane is also reported. In a subsequent study by the same group, an enhanced version is proposed [82]. The paper introduces a novel board-to-board interconnect structure utilizing Fuzz buttons from Custom Interconnects. This innovation enables the creation of a modular and miniaturized sample holder with interchangeable device boards. Such a design facilitates mass production and measurement of samples without the need for de-bonding or damaging the device under test. The sample holder prototype described in this paper closely resembles the commercially available Qboard. A similar early version of the Qboard is also briefly introduced in the experimental setup in [84].

Another group presents a more complex system in [83], also utilizing a double board configuration with a ground PCB for protection during wire bonding and mounting. They also employ the same mini-SMP bullets for board-to-board connection. A device board separates high-frequency and dc signals in different layers, including low-pass filters to further prevent signal interference. Unlike previous works where only passive components are integrated, the cryo-amplifier board in this paper explores the utilization of a multiplexer and transimpedance amplifier within the sample holder system, though only applicable at a temperature of 4.2 K. In addition to transmission and isolation measurements, the paper also discusses the influence of bias-tees on general gate sequences and impedance-matched via techniques for high-frequency inter-layer tracks.

4.2 Design of First-Phase Testing Boards

Compared to the highly complex sample holders in the literature, the first phase of the design is more reasonable for conducting fundamental tests on material suitability and simple building block structures. The board is targeted to be integrated inside the sample puck of the dilution fridge, facilitating measurements at the base temperature and enabling quicker sample changes without reheating the entire fridge. The following subsections discuss some considerations for the first phase of the design.

4.2.1 Material Selection

Based on the studies reported in the literature, the materials and components tested could serve as references. In the previously discussed papers, all the high-frequency PCB board materials are RO3003 boards. These boards have a low dielectric constant, requiring a thin thickness to maintain a 50-ohm characteristic impedance. This helps

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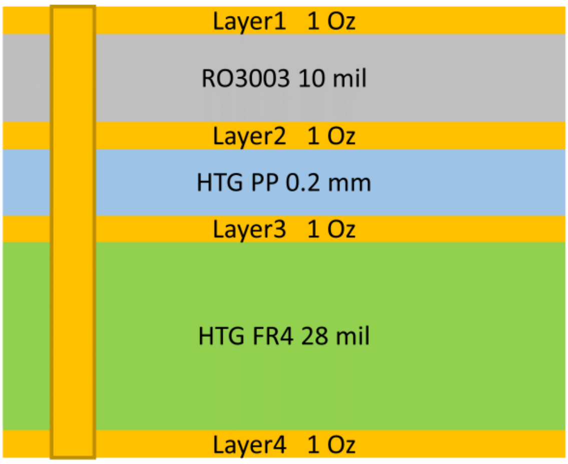

Figure 4.1: PCB stacking arrangement of the first-phase testing boards.

reduce nearby track-to-track coupling, as most of the electric field travels straight to the ground plane vertically. In addition to the low loss tangent feature of the Rogers high-frequency laminates, RO3003 boards have the smallest thermal coefficient of dielectric constant and decent thermal conductivity. Mechanically, RO3003 boards exhibit a coefficient of thermal expansion near that of copper. Overall, the laminate is believed to be suitable for high precision control of high-frequency signal performance at cryogenic temperatures. Figure 4.1 depicts the stacking arrangement of the first-phase testing boards. A four-layer structure is proposed for the early-stage experiment, requiring no complex routing. To minimize costs and provide sufficient thickness for stability, conventional FR4 material is used for the dc track routing. Electroless-nickel electroless-palladium immersion gold (ENEPIG) is chosen as the metallic finishing for the board due to the necessity of wire bonding in some testing structures. The nickel layer thickness is approximately 125 micrometers. However, its potential impact on magnetic-sensitive devices remains uncertain, despite previous reports dismissing concerns due to the small amount of usage involved [81]. To simplify the production and design complexity, all vias are implemented as plated through holes, with epoxy plugs to prevent gas entrapment. This precaution helps avoid potential virtual leaks under vacuum conditions [81].

Utilizing only one layer of the high-frequency laminates suggests the use of unbalanced transmission line structures on the surface layer of the board, simplifying the overall design complexity. On the other hand, although some through-hole structures like impedance-matched vias reported in [83] demonstrate frequency ranges up to around 20 GHz, connecting surface routings to interlayer striplines might be challenging to achieve our targeted 40 GHz bandwidth within fabrication process capabilities. Therefore, for the first phase of testing, planar structures are adopted, which influences the selection of microwave connectors and the corresponding cables. With the requirement of up to 40 GHz operation, several miniaturized and push-on candidates, including SMP, SSMA, Mini-Coax, Mini-SMP, MMPX, and SMPS, are considered. The conventional SK series connectors are dismissed due to their relatively large size and difficulty in assembly. While none of the connector types mentioned above are specifically designed for cryogenic usage, Mini-SMP and Mini-Coax connectors have been reported in previously reviewed literature. However, since they are unavailable from their sole producer, Rosenberger, we have had to explore other alternatives. Considering the component size and the comparable pin radius to the on-board signal track, MMPX and SMPS connectors have been selected. These two selections offer flexibility in testing: MMPX connectors provide stronger and more reliable soldering at cryogenic temperatures due to their long print legs inside through holes, while surface mount type SMPS connectors have a smaller size and do not affect the interlayer structures of the PCB, improving the versatility of board design and easing mechanical limitations. The corresponding cables connect the respective on-board connector to the SMP connector on the feedthrough of the sample puck. While cryogenically verified cable options like CuNi and superconducting materials exist, considerations such as price, bending ability, and diameter may be a concern. Overall, conventional cable materials at room temperature like silver-plated copper and PTFE or FEP dielectric are used, which seem operable at cryogenic

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environments based on several reports in the literature.

The selection of dc connectors and other SMD components is relatively straightforward, as there have been numerous cryogenic experiments conducted. However, since none of the materials discussed above are specifically designed for cryogenic use, their performance at low temperatures is unpredictable. Therefore, as an initial phase of verification, testing across various scenarios is necessary to lay the groundwork for future research.

4.2.2 Considerations of Testing Scenarios

In Section 4.1, we discussed the general functionalities of sample holders for spin qubit platforms, which encompass various specialized control and sensing purposes. For the initial testing phase, we can summarize the versatile specifications into several common testing scenarios. From a microwave engineering perspective, we conclude the listed requirements as follows:

1. The dc to kHz low-frequency tracks, which involve less microwave design. The main challenge lies in filtering and decoupling, preventing signal interference with other high-frequency signals.
2. High-frequency lines up to around 6 GHz, which could be used as gate control lines and the reflectometry lines connected to resonator tanks.
3. ESR microwave transmission lines operating up to 40 GHz, representing the most demanding specification in this on-board high-frequency design.

By the above classification, two quasi-TEM structures are proposed: microstrip lines (MS) and conductor-backed CPW (CBCPW). The CBCPW lines provide better confinement of the field, reducing coupling and radiation loss at higher frequencies, as well as less dispersion and possible parasitic wave mode propagation. Meanwhile, MS lines, with their smaller cross-sectional areas, might be suitable for high-density RF control and

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reflectometry lines.

Instead of directly integrating the required elements into a proper sample puck, the first-phase experiment here divides each part to identify possible functional obstacles. With the need to validate microwave transmission line performance up to high frequency ranges and also quantify the SMD components at cryogenic temperatures, a TRL calibration scheme is proposed. The design includes three different line lengths, each with electrical phases ranging from 20 to 160 degrees. These correspond to frequency ranges from 6.4 GHz to 50.9 GHz, 0.83 GHz to 6.6 GHz, and 1.5 GHz to 11.8 GHz, denoted as L1 to L3. An open standard is selected in the MS case for simplicity in design, while a short standard is chosen in the CBCPW case for better control of the field termination. Each of the TRL standards has its own connectors and cables connected to the adapter on the feedthrough of the sample puck. Due to the restriction of having only eight available cables in the dilution fridge, the TRL board is constrained to four tracks. Consequently, besides incorporating the standards, only one device under test (DUT) or one additional line can be accommodated on the same board. Alternatively, DUTs can be exclusively mounted on other boards without standards, assuming the error box remains the same as the standard board. With this approach, the board containing the device is loaded and measured after unloading the standard board when TRL calibration is performed.

With this possible TRL calibration scheme, several structures and components are selected as devices under test (DUT). Firstly, on the TRL standard boards, either an additional line, which serves as both a DUT and a standard, or a gap for testing the wire bonding effect is constructed. On the MS board, a enhanced coupling ring resonator is designed as a DUT, which could be used to calculate the laminate material properties. Additionally, SMD components with different footprints and bias-tee structures allowing for resistive or inductive choking are integrated within separate boards from the TRL

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standards. These boards also include individual sockets for dc measurements of SMD components.

Extending the on-board TRL concept, on-chip TRL calibration boards are routed with four paths, each with identical electrical lengths traced to the DUT mounting area. As a control group, a similar board without a mounting area, with lines connecting directly to the other end, is added to verify symmetry and check for possible coupling.

In addition to conventional microwave characterization studies, first-phase sample holders with dc routing are designed to assess the impact of high-frequency signals within the same board for quantum devices. These boards feature low-pass filters on the dc tracks near the DUT, which may consist of commercially available individual components or SMD resistors and capacitors, preventing the RF to dc crosstalk. For the sole purpose of conducting pure dc measurements on undiced samples, a board with ample mounting space is implemented, featuring only dc routings.

Besides serving as a sample holder for quantum-related devices, this first-phase testing board is also suitable for verifying the platform of integrated circuit packaging at cryogenic temperatures. Therefore, a two-port GSG routing measurement board is devised, comprising ten dc tracks, each offering five mounting points for bypass capacitors, while another board is further equipped with footprints for dc blocking capacitors.

Finally, in order to prevent mechanical failure in cryogenic environments, most experiments are designed in two versions using either MMPX or SMPS connectors. Additionally, some TRL boards are horizontally routed to avoid cable stress limiting the winding angle and becoming stuck with the enclosure of the sample puck. For reference, Table 4.1 lists the photos of all implemented boards in this first-phase experiments.

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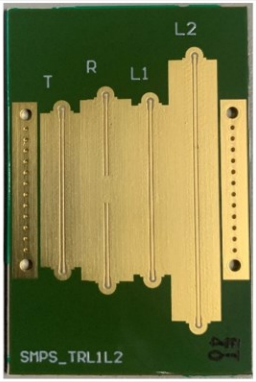
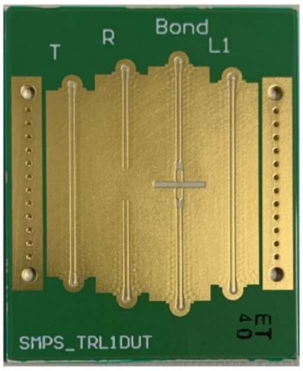
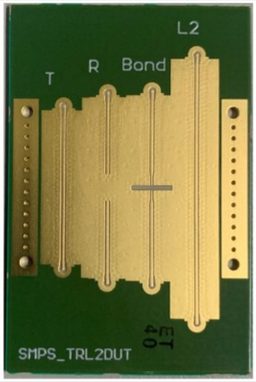
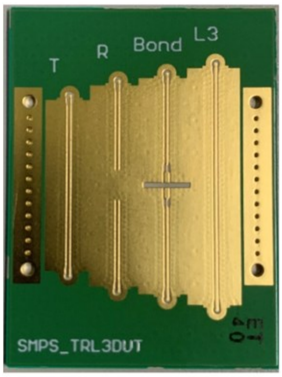
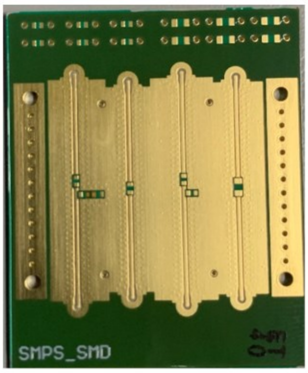
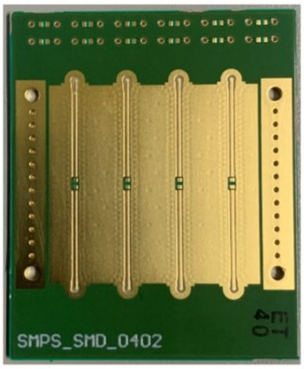
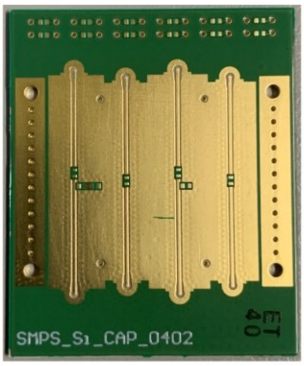
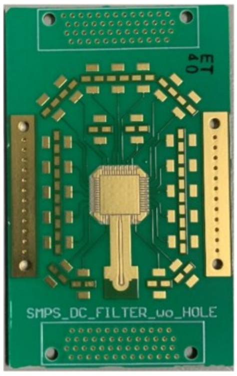
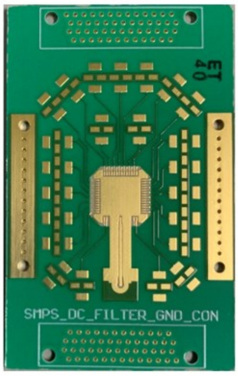
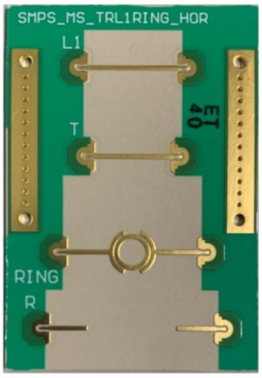
SMPS_TRL1L2	**SMPS_TRL1DUT**	**SMPS_TRL2DUT**
		
SMPS_TRL3DUT	**SMPS_SMD**	**SMPS_SMD_0402**
		
SMPS_Si_CAP_0402	**SMPS_DC_RC_wo_HOLE**	**SMPS_DC_RC_GND_CON**
		
SMPS_DC_FILTER_wo_HOLE	**SMPS_DC_FILTER_GND_CON**	**SMPS_MS_TRL1RING_HOR**
		

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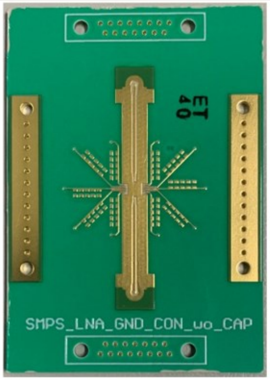
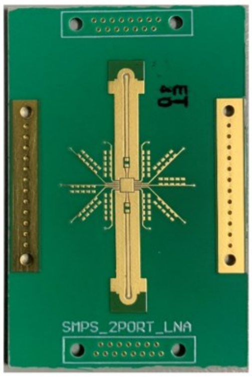
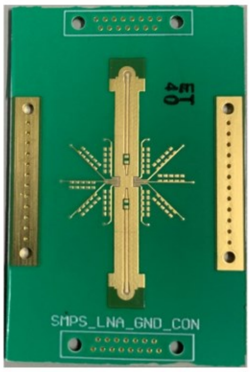
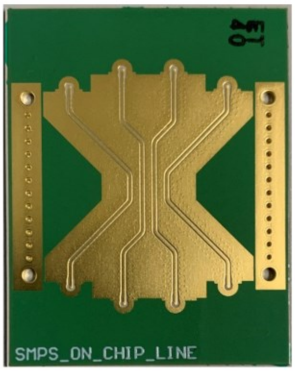
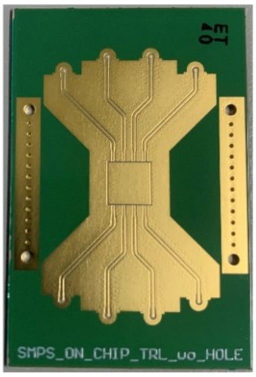
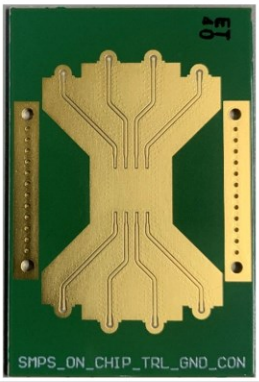
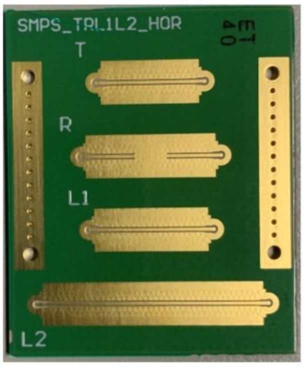
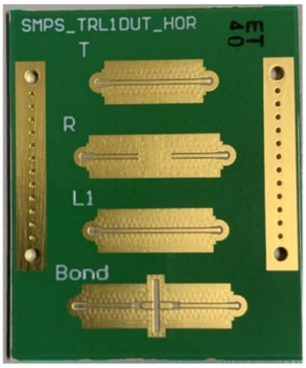
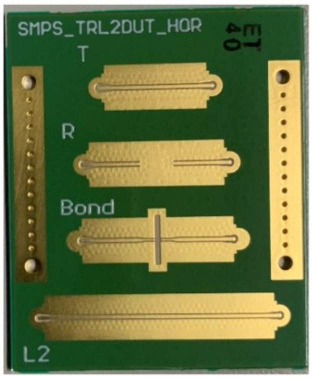
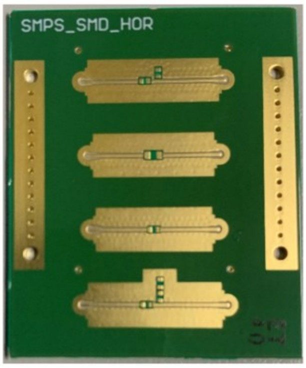
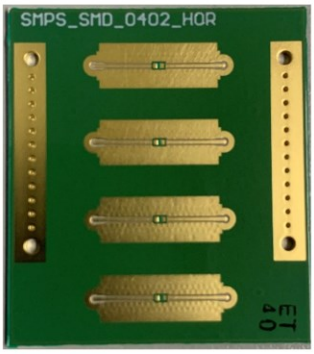
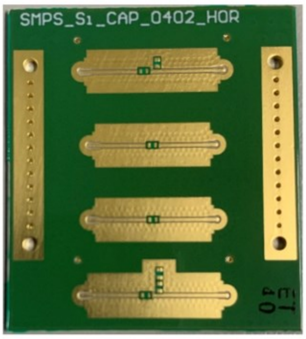
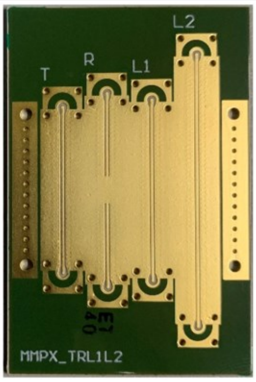
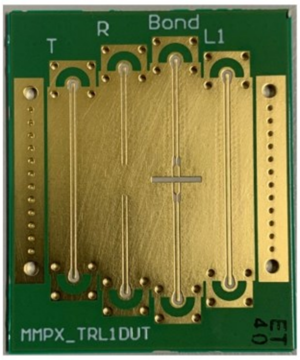
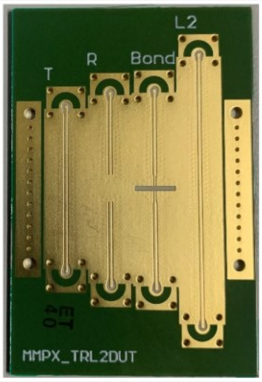
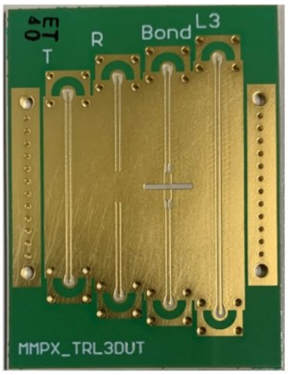
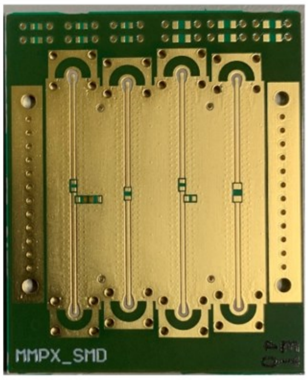
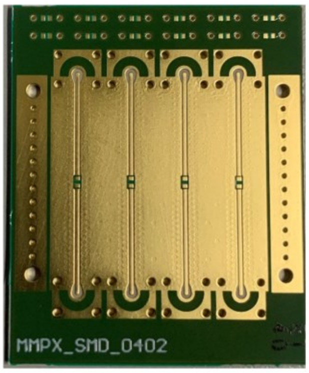
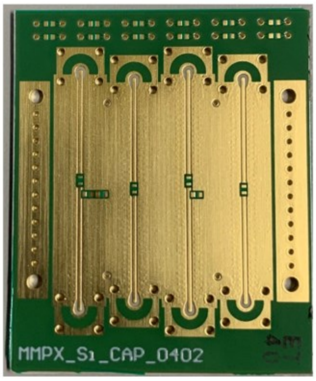
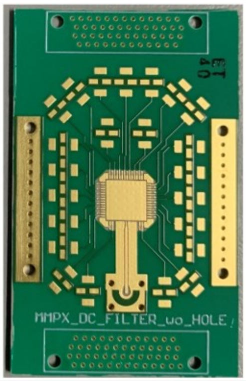
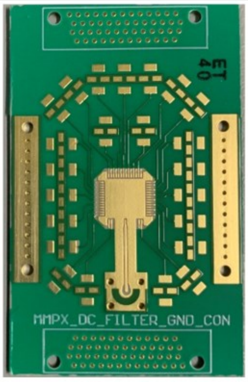
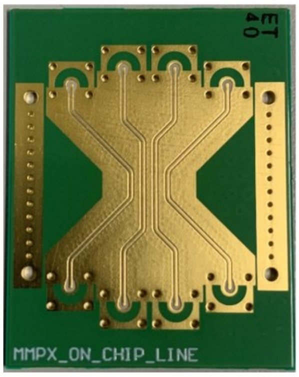
SMPS_LNA_GND_CON_wo_CAP	**SMPS_2PORT_LNA**	**SMPS_LNA_GND_CON**
		
SMPS_ON_CHIP_LINE	**SMPS_ON_CHIP_TRL_wo_HOLE**	**SMPS_ON_CHIP_TRL_GND_CON**
		
SMPS_TRL1L2_HOR	**SMPS_TRL1DUT_HOR**	**SMPS_TRL2DUT_HOR**
		
SMPS_SMD_HOR	**SMPS_SMD_0402_HOR**	**SMPS_Si_CAP_0402_HOR**
		

MMPX_TRL1L2	**MMPX_TRL1DUT**	**MMPX_TRL2DUT**
		
MMPX_TRL3DUT	**MMPX_SMD**	**MMPX_SMD_0402**
		
MMPX_Si_CAP_0402	**MMPX_DC_RC_wo_HOLE**	**MMPX_DC_RC_GND_CON**
		
MMPX_DC_FILTER_wo_HOLE	**MMPX_DC_FILTER_GND_CON**	**MMPX_ON_CHIP_LINE**
		

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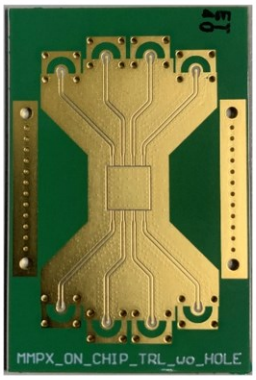
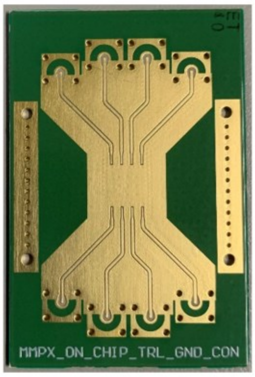
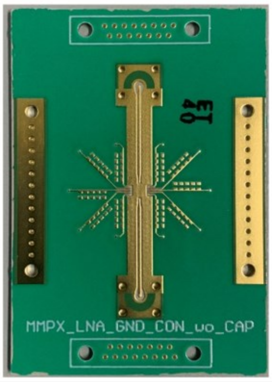
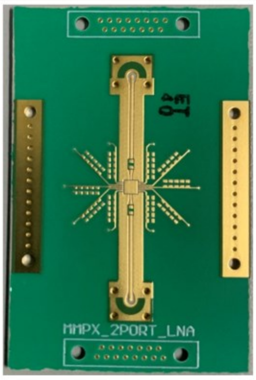
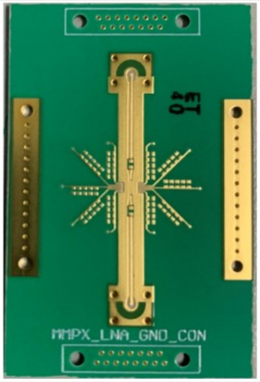
MMPX_ON_CHIP_TRL_wo_HOLE	MMPX_ON_CHIP_TRL_GND_CON	MMPX_LNA_GND_CON_wo_CAP
		
MMPX_2PORT_LNA	**MMPX_LNA_GND_CON**	**DC_CHIP_1.3_wo_HOLE**
		

Table 4.1: List of the first-phase testing boards.

4.2.3 RF Routing Design

One of the primary challenges in microwave design for RF routings is the interconnect structure from on-board connectors to the transmission lines. Typically, a taper section is required due to the difference in size between the pin and outer metal diameter compared to the designed on-board transmission lines. Figure 4.2 and Figure 4.3 depict the footprints of the four layers for MMPX and SMPS connectors respectively. The interconnect section extends the coaxial-like structure from the connector, transitioning to the planar transmission lines with a bending angle of 90 degrees. Different tapper pattern designs ensure that the signal track and the shrinking ground planes combine with the outer metal arch of the connectors to form the proper semi-coaxial-like transmission with a characteristic impedance near 50 ohms. In both designs, a small hole

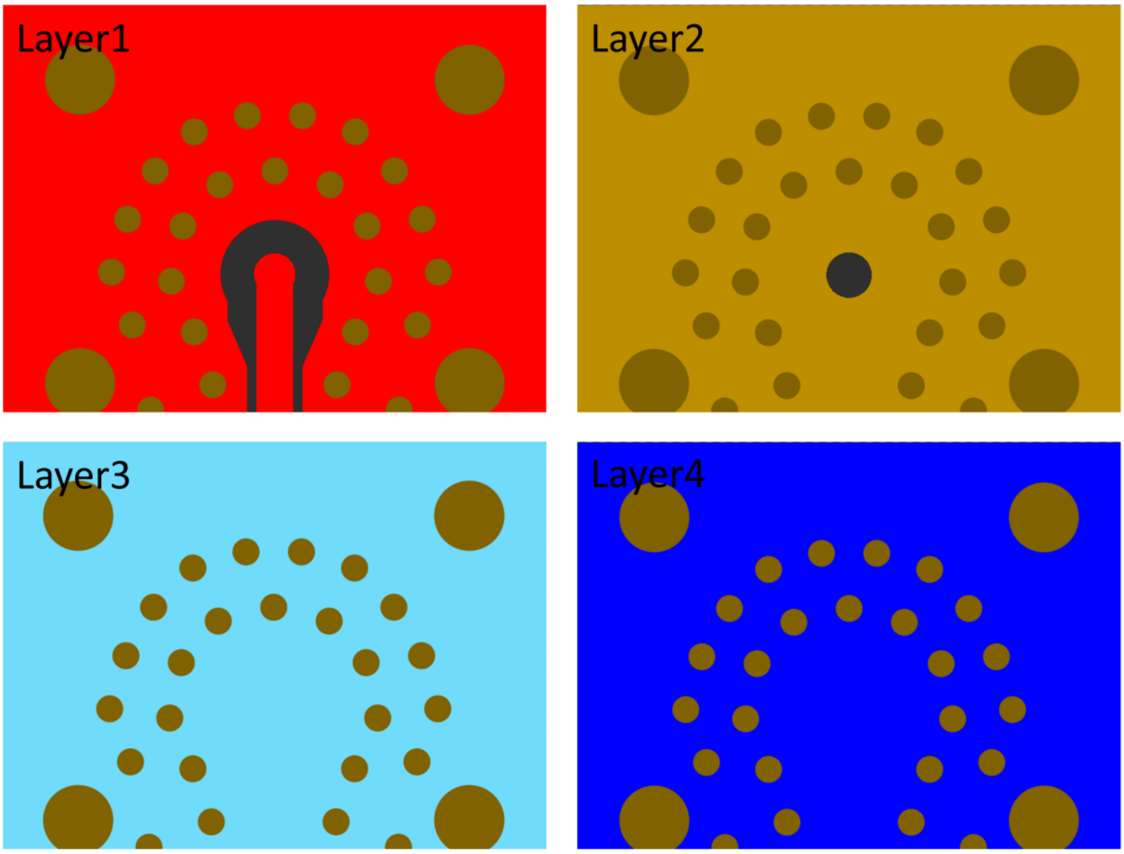


Figure 4.2: Footprints of the four layers for MMPX connectors.

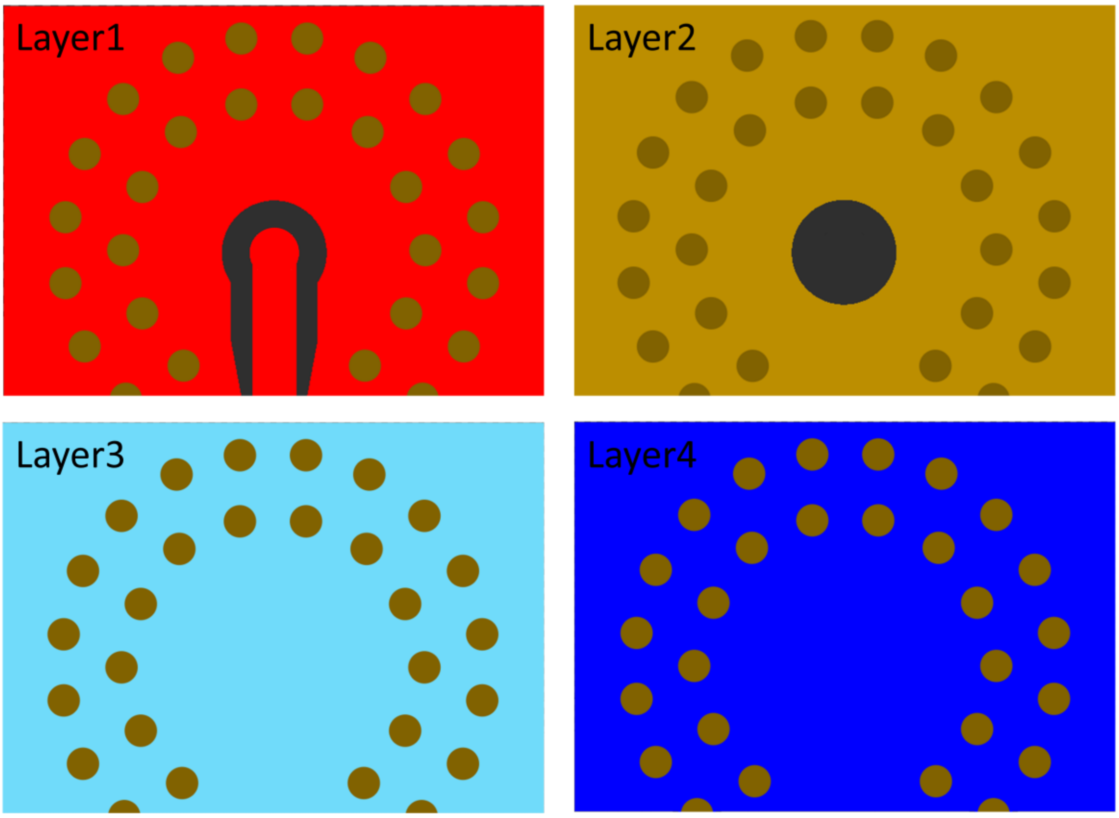


Figure 4.3: Footprints of the four layers for SMPS connectors.

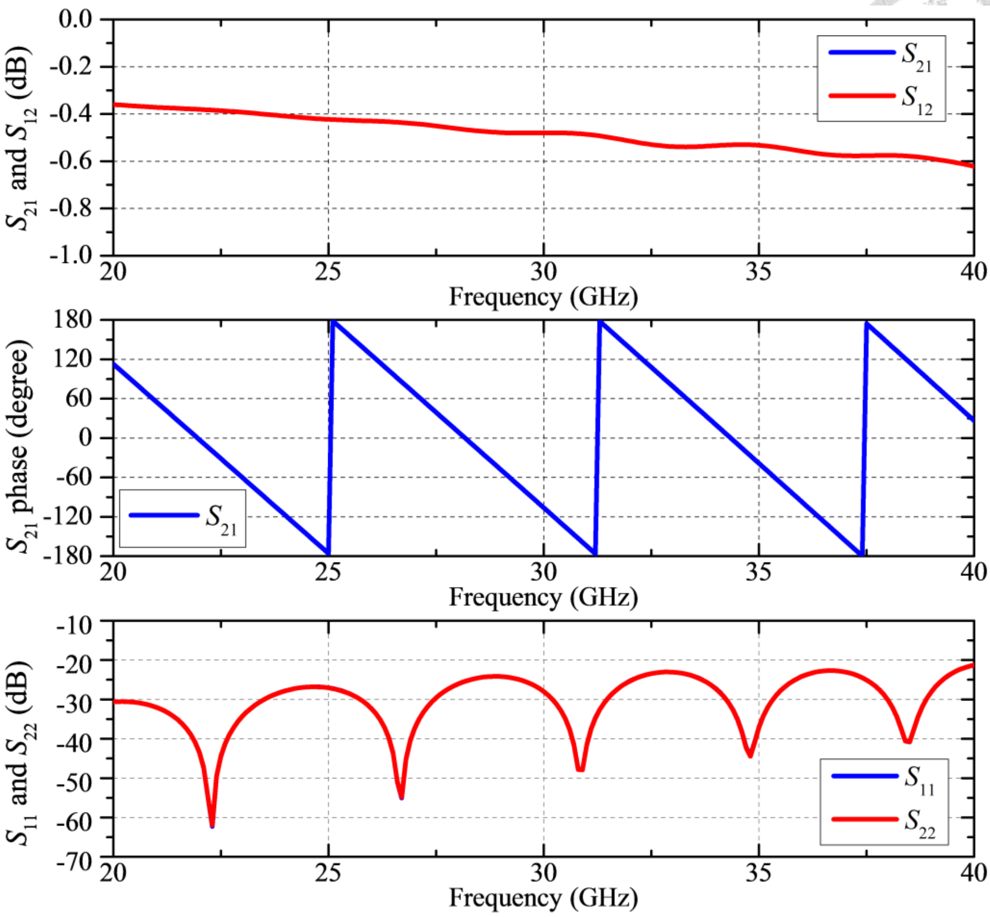


Figure 4.4: Simulated responses of CBCPW L1 standard with MMPX connectors.

is opened in the second layer directly beneath the pin of the connectors. This modification deepens the cavity under the pin with an additional dielectric layer, loosely maintaining the specific proportion between outer and inner conductors required for the coaxial-like transmission characteristic impedance of the connectors in this bending area. The pattern on the fourth layer does not affect the microwave transmission line. However, due to the high density of through holes in this area, a connected ground plane is preferred.

Figure 4.4 and Figure 4.5 illustrate the EM simulated *S*-parameter responses of CBCPW transmission line L1 standard along with MMPX or SMPS connectors respectively. With either connector type, the interconnect section and the CBCPW transmission line effectively propagate the high-frequency fields between the two coaxial-like connectors, achieving a return loss of higher than 20 dB up to 40 GHz. The on-board insertion loss, including two connectors, is lower than 0.6 dB for both types of

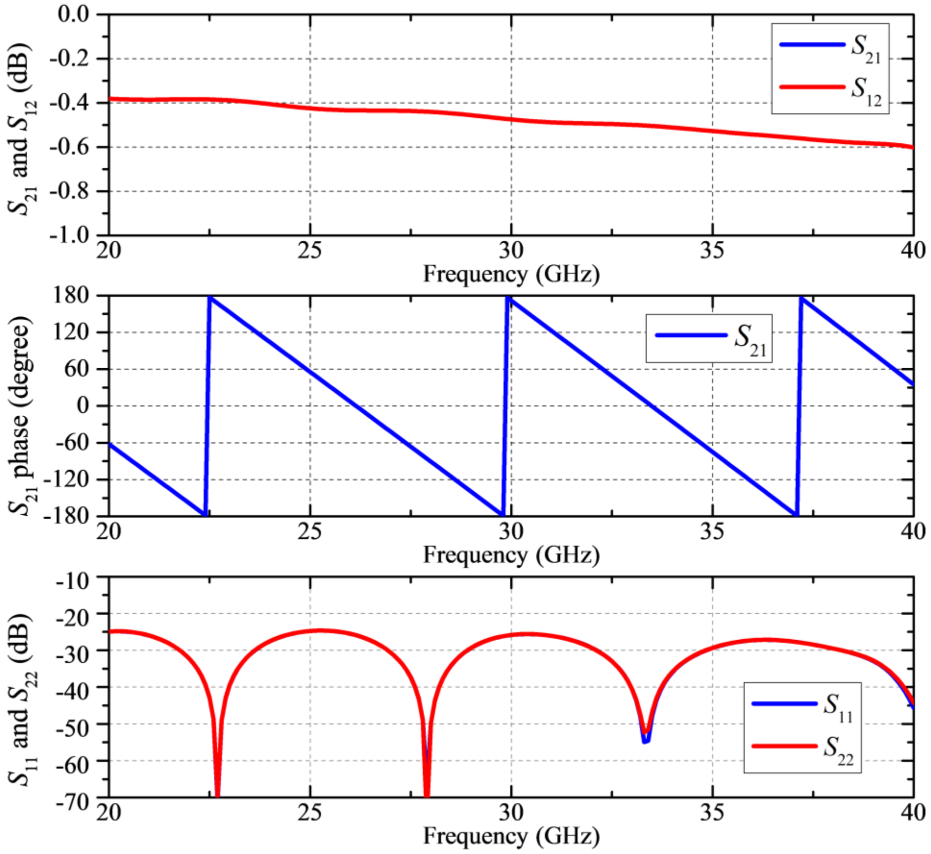


Figure 4.5: Simulated responses of CBCPW L1 standard with SMPS connectors.

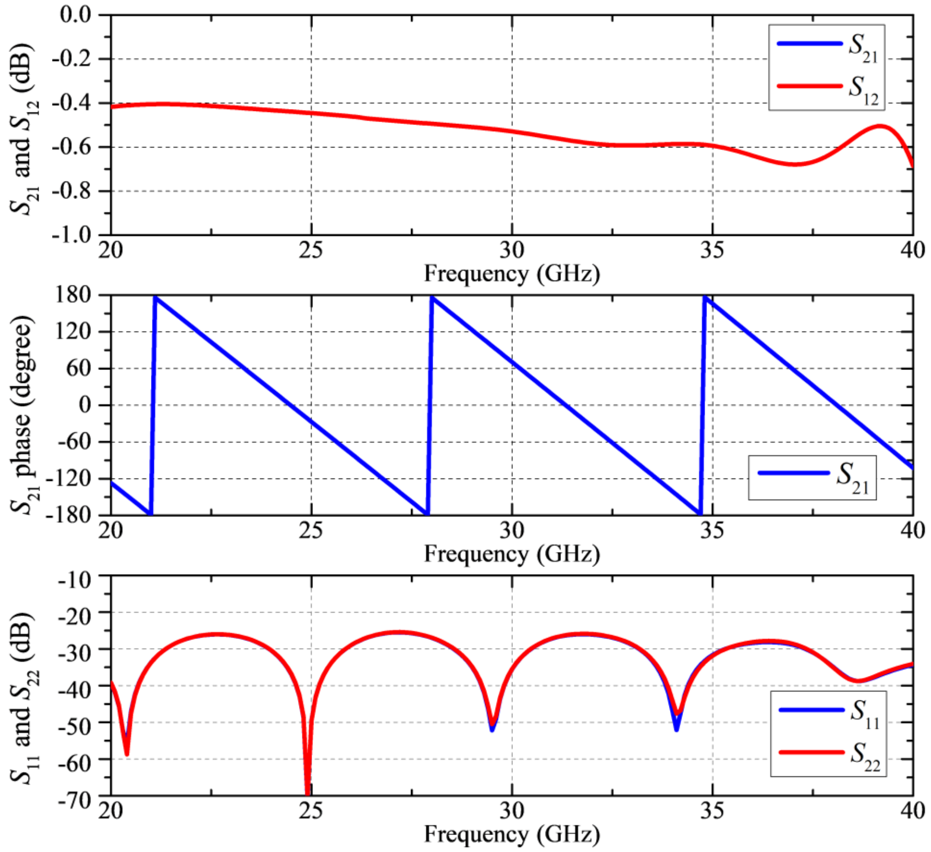


Figure 4.6: Simulated responses of MS L1 standard with SMPS connectors.

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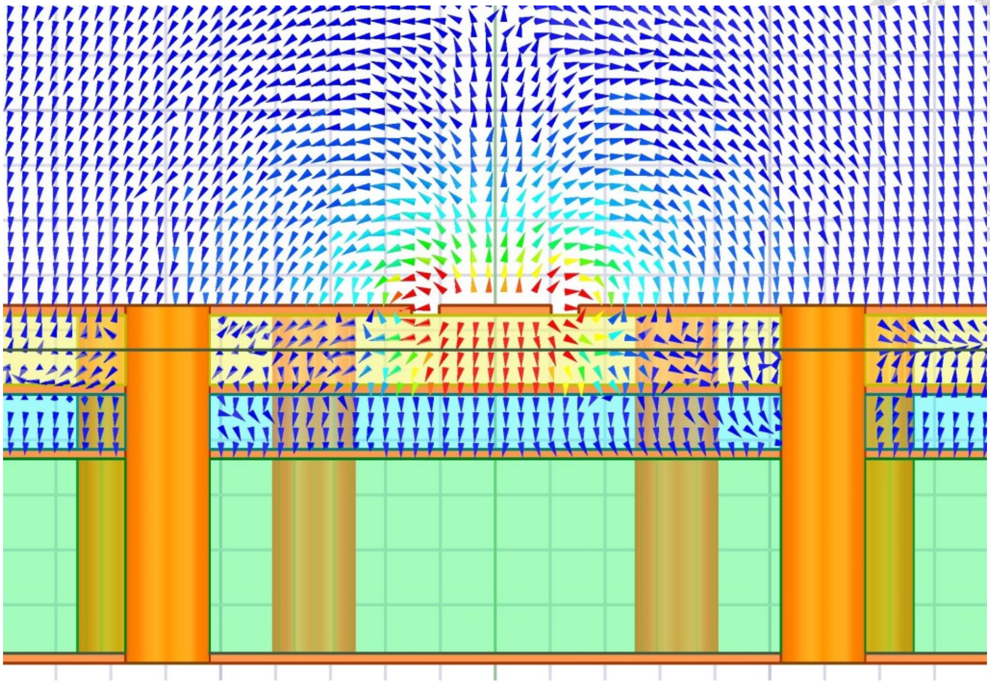

Figure 4.7: The cross-sectional electric field vector of CBCPW transmission lines.

connectors. A similar simulation is conducted for MS transmission line L1 standard with SMPS connectors in Figure 4.6. While the return loss is well above 20 dB in the targeted 40 GHz frequency range, the transmission responses approaching 40 GHz starts to exhibit some nonlinearity. This might be due to dispersion or higher-order mode phenomena in MS lines, which start at a lower frequency for the selected laminate thickness. Nonetheless, both the CBCPW and MS lines, with both MMPX and SMPS connectors, perform admirably within the required bandwidth.

The cross-sectional electric field intensity of a CBCPW transmission line is depicted in vector form in Figure 4.7. Unlike conventional CPW structures, where most of the field lines extend from the signal track to the outer surrounding ground planes, here, due to the thin thickness required for the RO3003 laminate to achieve a 50-ohm characteristic impedance, the signal track is wider. As a result, a greater portion of the field travels directly to the conductor-backed ground, creating a semi-coaxial-like field distribution that integrates the characteristics of microstrip and CPW fields.

Apart from the cross-sectional field distribution, Figure 4.8 illustrates the complex

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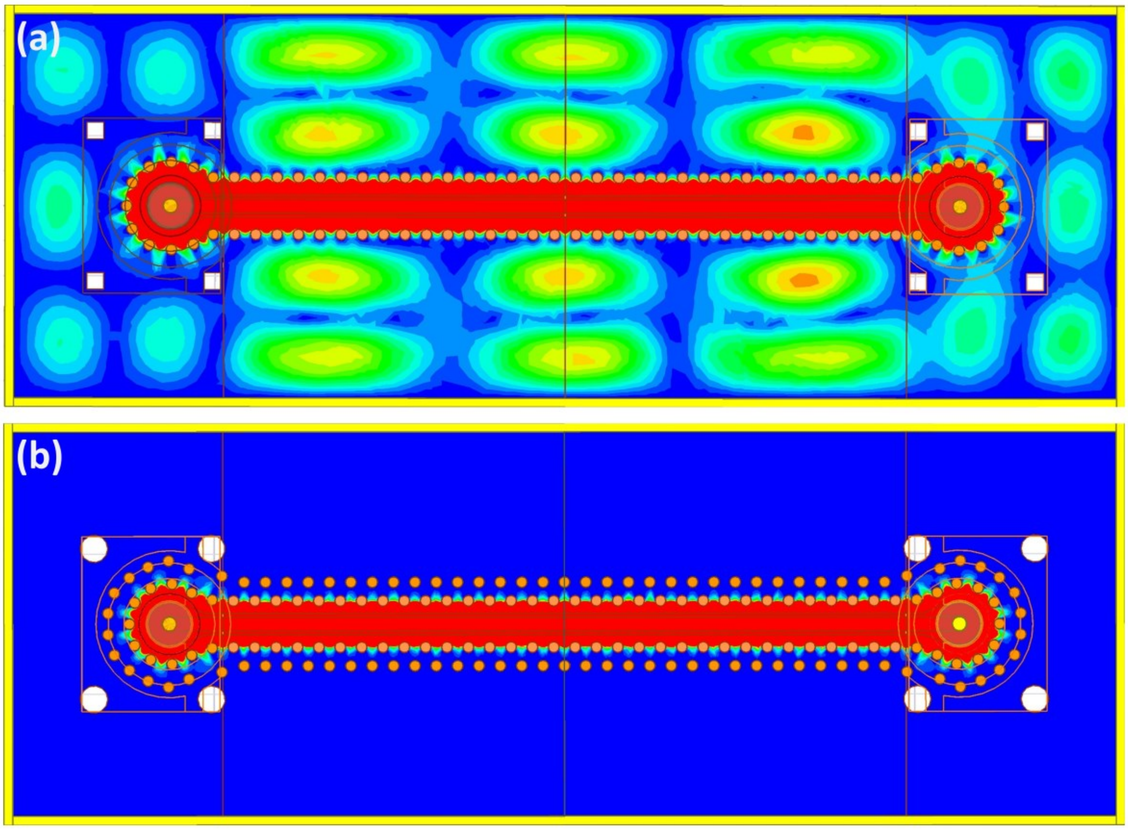

Figure 4.8: The complex magnitude of the electric field in the RO3003 laminate. (a) With a single layer of vias. (b) With a double layer of vias.

magnitude of the electric field within the RO3003 laminate between Layer1 and Layer2 copper metal of a CBCPW transmission line. Grounding vias are conventionally recommended to suppress possible parallel-plate mode propagation between the upper and conductor-backed CBCPW grounds. As shown in the EM simulation at a frequency point of 40 GHz, having only a single layer of vias allows a certain amount of electric field to leak from the process-limited via spacing. Conversely, under the same conditions, the second layer of vias effectively limits the field to a desired extent and suppresses the leakage-induced parallel-plate mode propagation. It's worth mentioning that in the EM simulation, a PEC guarding wall is introduced surrounding the board, depicted as yellow rectangles in Figure 4.8. This prevents the field radiating from the upper area of the CBCPW transmission line from traveling back to the parallel-plated space of the laminates through the non-shielded side openings. In practical implementation, through

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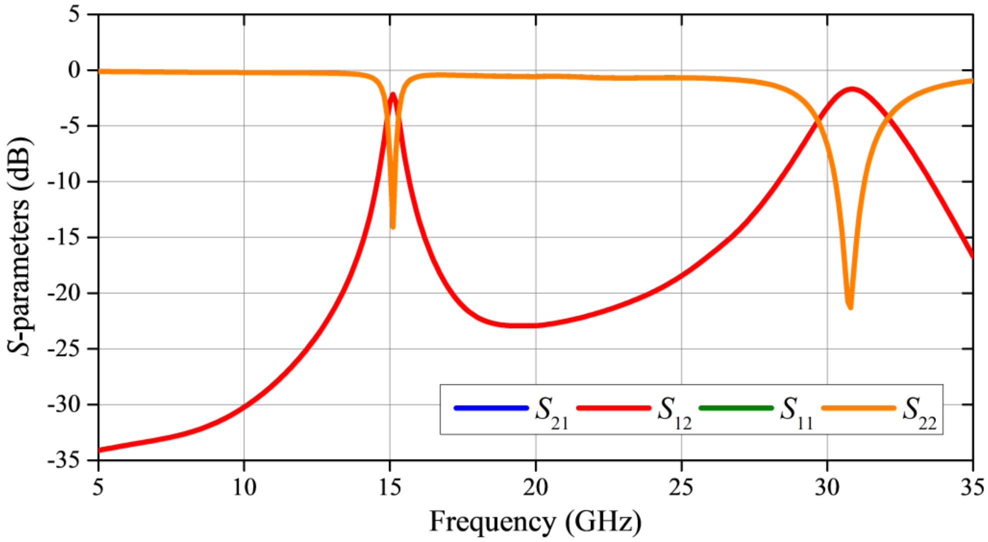

Figure 4.9: Simulated responses of ring resonator with SMPS connectors.

hole vias are randomly added on the idle ground planes outside the transmission line structures, which may disrupt the periodicity of potential parallel-plated mode propagation.

On the MS board, an enhanced coupling ring resonator is implemented as a DUT. Such resonators have been employed in previous studies for measuring dispersion, dielectric constant, and dissipation factor by analyzing the resonant frequency and quality factor [85, 86]. To enhance coupling strength and improve insertion loss, the ring resonator is designed with enhanced coupling configuration, although this may result in more pronounced perturbation of the field from the coupling lines to the ring [87, 88]. Figure 4.9 depicts the EM simulated first and second modes of the implemented enhanced coupling ring resonator, along with the two connectors and MS transmission lines before and after the DUT.

4.2.4 Wire Bonding Issues

Apart from the design challenges presented by on-board high-frequency transmission lines and connector-to-line interconnects, the transition section connecting on-board transmission lines to the DUT poses another microwave transmission challenge.

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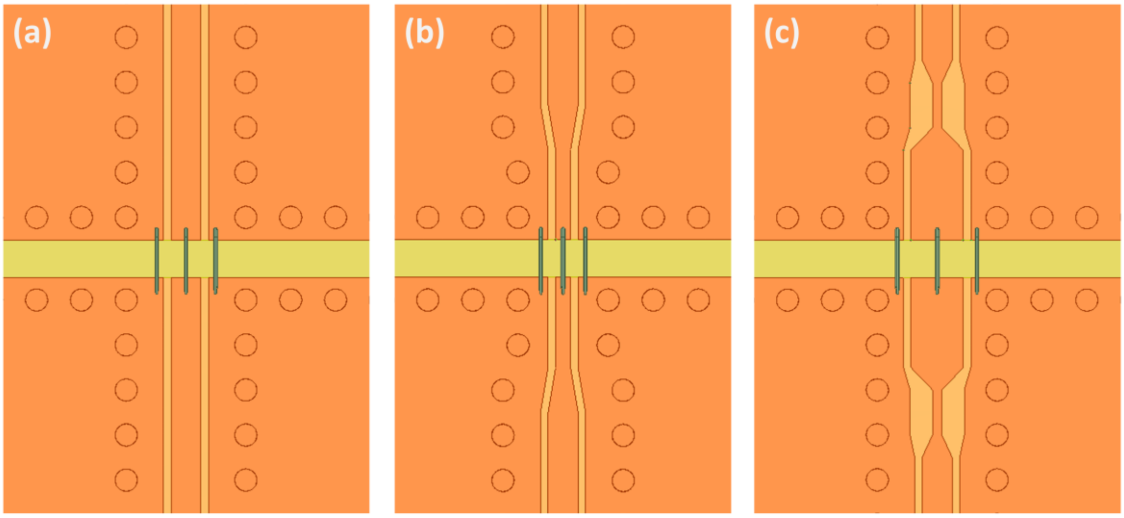

Figure 4.10: Transmission-line-to-bond-wire transition structures under test. (a) Same structure extending CBCPW transmission lines. (b) Shrink-sized wire bonding pads. (c) Impedance-matching structure compensating the bond wire effect at high frequencies.

Given that custom sample devices for experimental measurements typically use bond wires for the DUT-to-board connection, the wire bonding effect at microwave frequency ranges becomes a significant concern. Considering the small pitch size of the on-chip pads primarily intended for probing measurements, the width of the bonding pads may intuitively shrink from that of CBCPW lines to reduce both the length of the bond wire and the peripheral area required for adhering the sample. Nonetheless, at high frequency ranges, the inductive response of the thin bond wires along with the shrink-sized bonding pads form a high impedance section that reduces the transmission coefficient. In response to the inductive component of the bond wires, the simplest modification is implementing an artificial transmission line structure by adding capacitors before and after the bond wires. However, implementing l lumped capacitance solely through copper patterns on PCB boards poses challenges, whereas employing SMD components may demand a larger area and introduce additional coupling and bond wiring issues.

Instead of using conventional lumped LC as matching sections, the approach here adopts the multi-section transformer method [89]. In this approach, the inductance of the bond wire could be modeled as a short section of transmission line with a significantly

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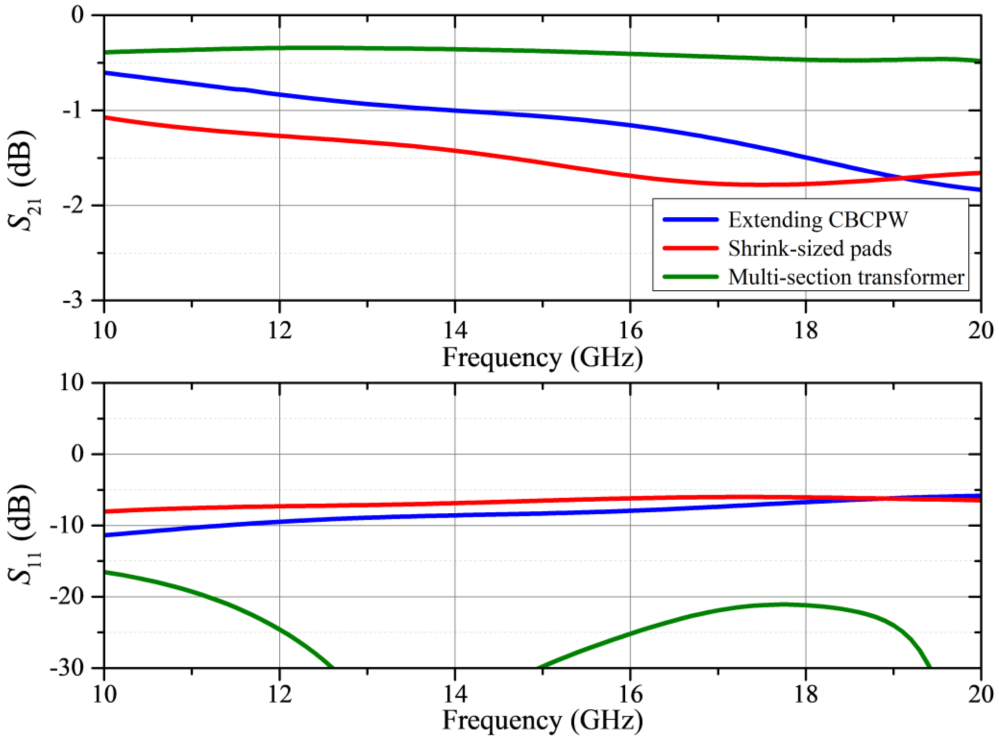

Figure 4.11: Simulated responses of the three different wire bonding structures.

high characteristic impedance. Through a series of different transmission line sections with carefully adjusted characteristic impedance, the multi-section response could be tuned to optimize the transmission coefficient within a desired bandwidth. From another perspective, this could also be interpreted as a step-impedance low-pass filter design. Figure 4.11 compares the EM simulated responses of the three configurations depicted in Figure 4.10, which include the two MMPX connectors and CBCPW transmission lines before and after the transition section. Since the configuration of the DUT is unclear for a sample holder design, the experiment here focuses on verifying the usefulness of the interconnecting structure by employing a symmetry arrangement, enclosing the bond wire in the middle. The EM simulation results in Figure 4.11 are conducted only up to 20 GHz. This limitation arises from the effective bandwidth of the impedance matching section, which is constrained by the inductance value of the bond wire, corresponding to the necessary wire bonding length. As the comparison reveals, both without any modification or using the shrink-sized pad are affected by the bond wire and result in an unacceptable

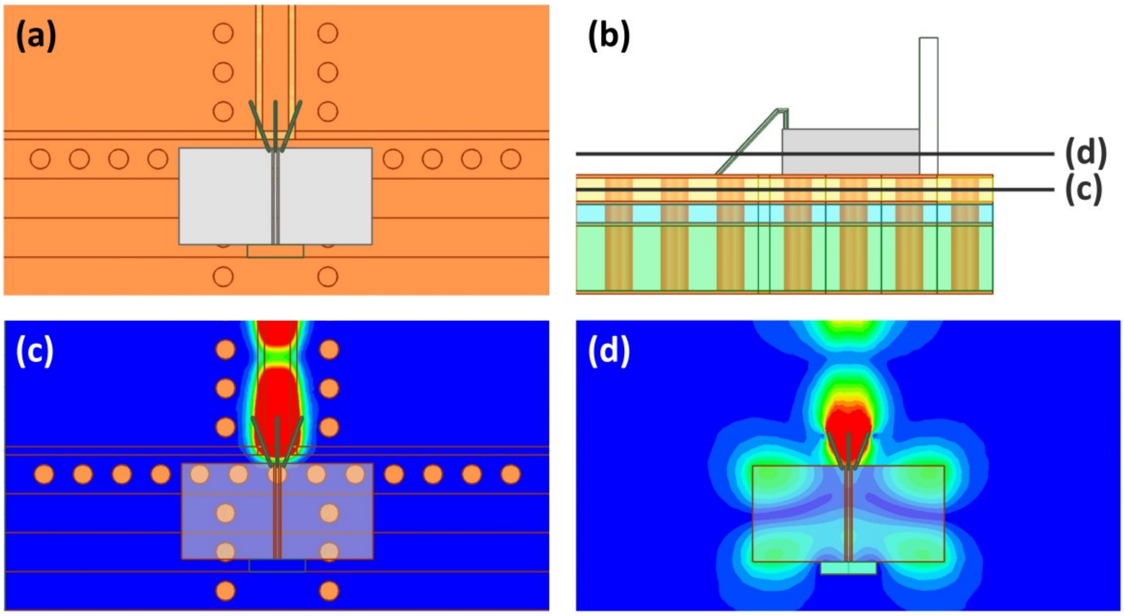

Figure 4.12: EM simulation of the sample holder CBCPW transmission line bond wiring to a fictitious DUT, featuring an aluminum CPW line on a Si substrate. (a) Top view of the setup. (b) Side view of the setup. The lines indicate the slicing planes, on which the complex E fields at 40 GHz are shown in (c) and (d).

return loss. On the other hand, the multi-section impedance structure effectively enhances the matching and achieves an insertion loss of less than 0.5 dB within this frequency range. In practice, without the corresponding symmetrical impedance-matching structure on the sample chip, the overall transmission and bandwidth performance might degrade further; nevertheless, the multi-section transformer improves the overall signal transmission.

Another concern regarding bond wiring issues emerges when incorporating DUTs into the simulation. Figure 4.12 illustrates one such scenario, where a fictitious DUT, comprising an aluminum CPW transmission line above a silicon substrate, is positioned on the sample holder, with wire bonding to the feed-in CBCPW transmission line. Figure 4.12 (b) depicts the side view of the configuration, with two lines indicating the slicing planes where the complex E fields are shown in (c) and (d). At the transition area, the confined field of the feed-in CBCPW transmission line is compelled to be propagate to the upper layer, guided by bond wires and blocked by ground vias. Most of the energy could thus smoothly transfer to the aluminum CPW lines on the fictitious DUT. However,

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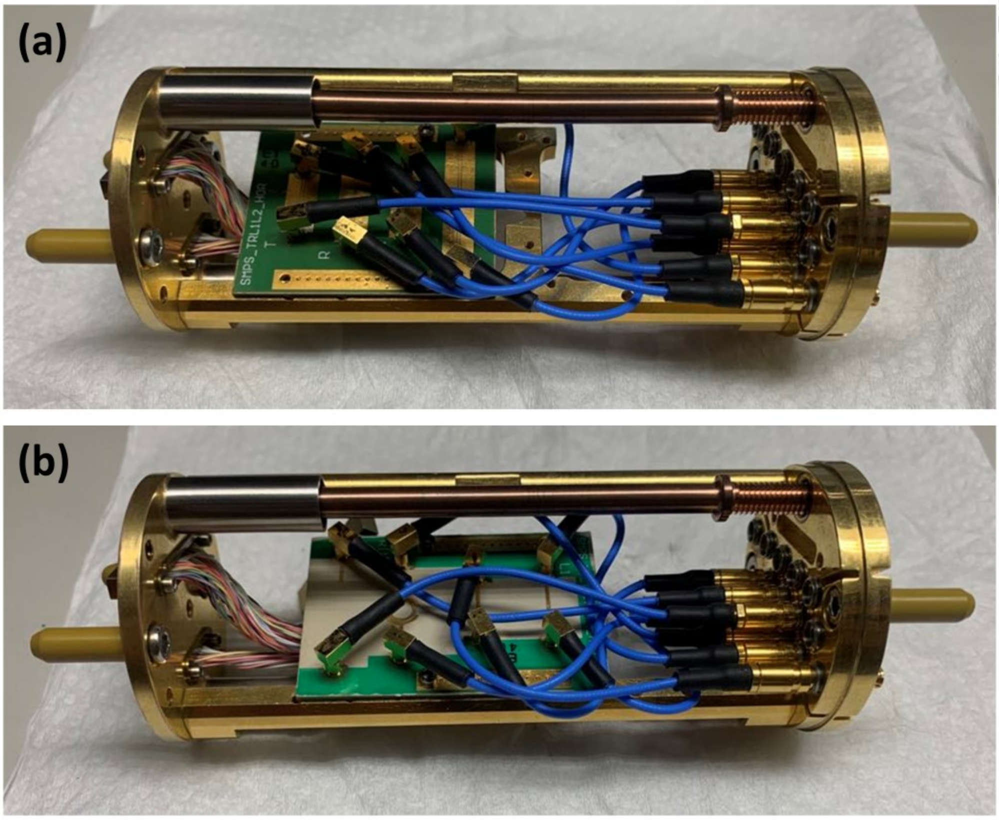

Figure 4.13: Boards assembled within the sample puck. (a) SMPS_TRL1L2_HOR board. (b) SMPS_MS_TRL1RING_HOR board.

as shown in Figure 4.12 (d), when the field is injected within the aperture defined by the bond wires, the aluminum layer of the DUT and Layer1 ground plane of the sample holder board, the Layer1 ground plane and the aluminum ground plane of the DUT form a parallel-plate structure, which may resonate like a patch at certain frequencies. These resonances therefore influence the transmission characteristics of this fictitious CPW line DUT, where in practical scenarios, affects the expected responses of the samples. This phenomenon will be revisited and carefully addressed in the next chapter.

4.3 RF Characterization within Sample Puck

4.3.1 Raw Data Measurement

As the first phase of verification, the functionalities of the seven boards containing microwave transmission lines are measured at room temperature, namely SMPS_TRL1L2, SMPS_TRL1DUT, SMPS_TRL1L2_HOR, SMPS_TRL1DUT_HOR, SMPS_MS_TRL1RING_HOR, MMPX_TRL1L2, and MMPX_TRL1DUT. Although we initially selected both types of connectors and two orientations, it later became apparent that the available space within the sample puck was insufficient to accommodate eight corresponding cables for the MMPX connectors, or for the eight SMPS cables when the transmission lines are in the vertical orientation. The mechanical limitations, such as the available space inside the sample puck and the inevitable bending stress and flexibility of the cables, pose unpredictable challenges during integration within the sample puck. Thankfully, the horizontal versions of transmission lines with SMPS connectors are suitable for testing in this initial phase. The assembled configurations of the SMPS_TRL1L2_HOR and SMPS_MS_TRL1RING_HOR boards within the sample puck are depicted in Figure 4.13.

The measured results of the standards on the SMPS_TRL1L2_HOR board are illustrated in Figure 4.14. To verify the functionalities step-by-step, two configurations are compared. In the "Board only" scenario, the VNA is calibrated to the reference planes at the end of the two 2.92-mm cables in the setup. Moreover, the responses of the required interconnects to the board, including two blue SMP-to-SMPS cables in Figure 4.13 and two SMP-to-2.92-mm adaptors, are involved in the measurement results. It's noteworthy that we use the same two blue cables and adaptors throughout all of the standard measurements in this case. On the other hand, the setup for the "w/ puck" scenario is shown in Figure 4.13, where the 2.92-mm cables from the calibrated VNA setup are affixed to the SMP connectors on the right-hand-side of the sample puck through the SMP-to-2.92mm adaptors. Consequently, the measured responses encompass the adaptors and connectors on the sample puck, as well as the eight different blue SMP-to-SMPS cables for the four standards. Notably, it is important to mention that the standards

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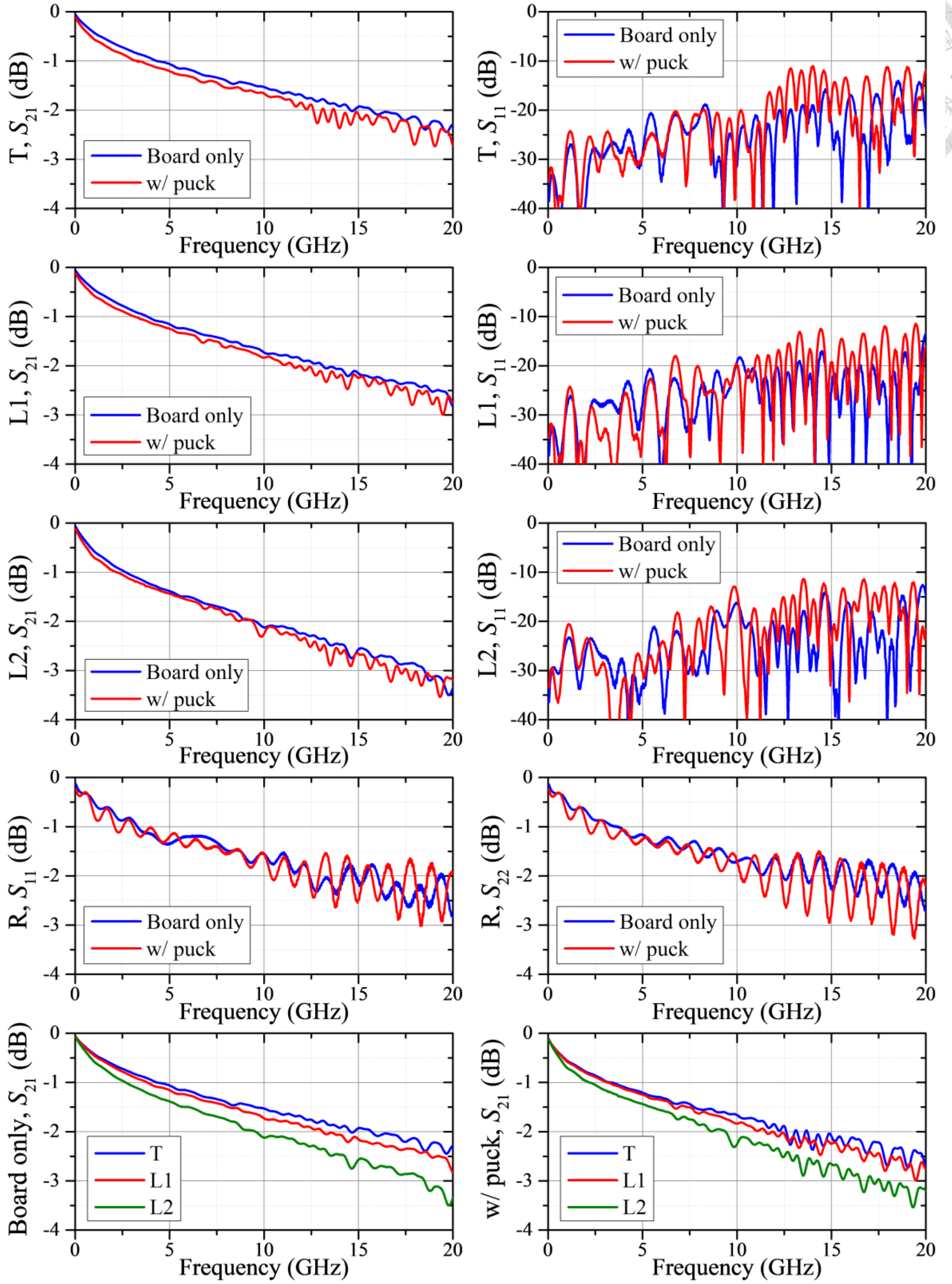

Figure 4.14: Measured responses of the SMPS_TRL1L2_HOR board alone and within the sample puck (without enclosure).

are measured without closing the enclosure of the sample puck in this configuration. The measurement results depicted are limited to 20 GHz for two reasons. Firstly, the bandwidth of the VNA used is restricted. Secondly, the high-frequency cables available

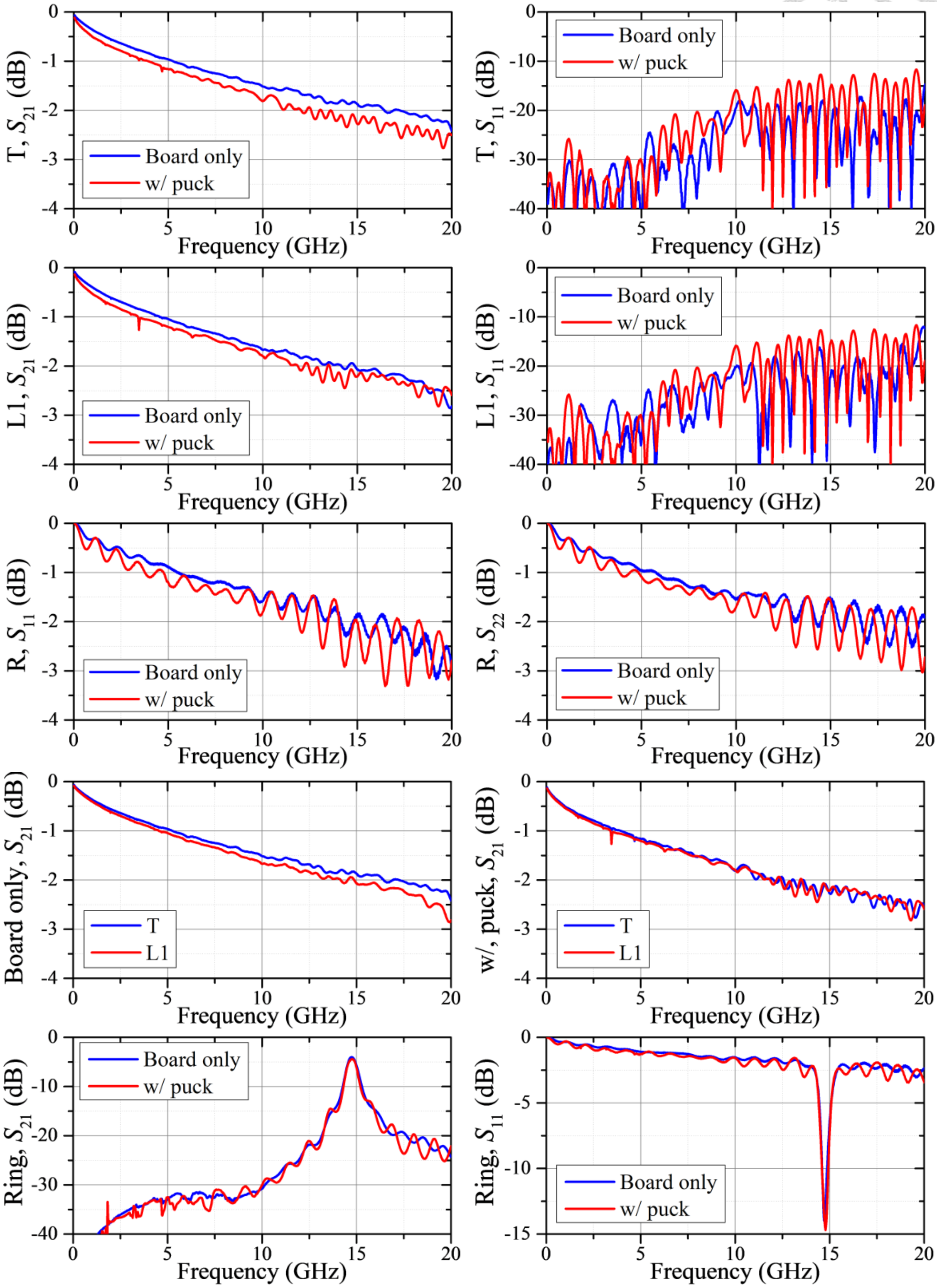

Figure 4.15: Measured responses of the SMPS_MS_TRL1RING_HOR board alone and within the sample puck (without enclosure).

in the dilution fridge used in this first-phase experiment are specified to cover only up to around 18GHz. Although a 20 GHz bandwidth is sufficient for this initial verification, simulations and all the components within the sample puck ensure functionalities up to

40 GHz. As shown in Figure 4.14, the inclusion of the sample puck not only deteriorates the insertion loss but also affects the return loss at higher frequencies. Additionally, the number of ripples in the transmission responses increases and is heightened due to multi-reflections caused by the unmatched impedance at each interconnection plane. Nevertheless, the measured responses continue to demonstrate good matching even under practical configurations within the sample puck, where the return loss is primarily constrained by the specifications of the off-board interconnects such as cables and connectors. By comparing within a single plot, noticeable increases in the insertion loss resulting from the extended CBCPW transmission lines are evident in both scenarios. At certain middle frequencies, ripples in the T and L1 responses overlap for the “w/ puck” case, possibly due to the varied responses of the different cables and connectors involved.

Figure 4.15 presents the measured responses of the SMPS_MS_TRL1RING_HOR board under the same comparison of the two cases. Within the sample puck, a similar degradation in return loss and increase in ripples are observed, although the reflection coefficient remains acceptable. The measured resonance frequency of the ring resonator is approximately 14.75 GHz, slightly lower than the simulated result. Because additional components are involved in the signal path, the measured quality factor is lower, necessitating a calibration scheme to obtain useful data for extracting the board parameters. Some non-idealities may be present in the measurements of this board, as the insertion loss of T1 without and within the sample puck nearly match each other, and some dips are observed in the responses. These defects are likely attributed to loose connections or differences in loss across the interconnections of varying standards when assembled within the sample puck.

To improve the evaluation of the electromagnetic environment in the dilution fridge, we subsequently covered the sample puck with its enclosure. Figure 4.16 compares the

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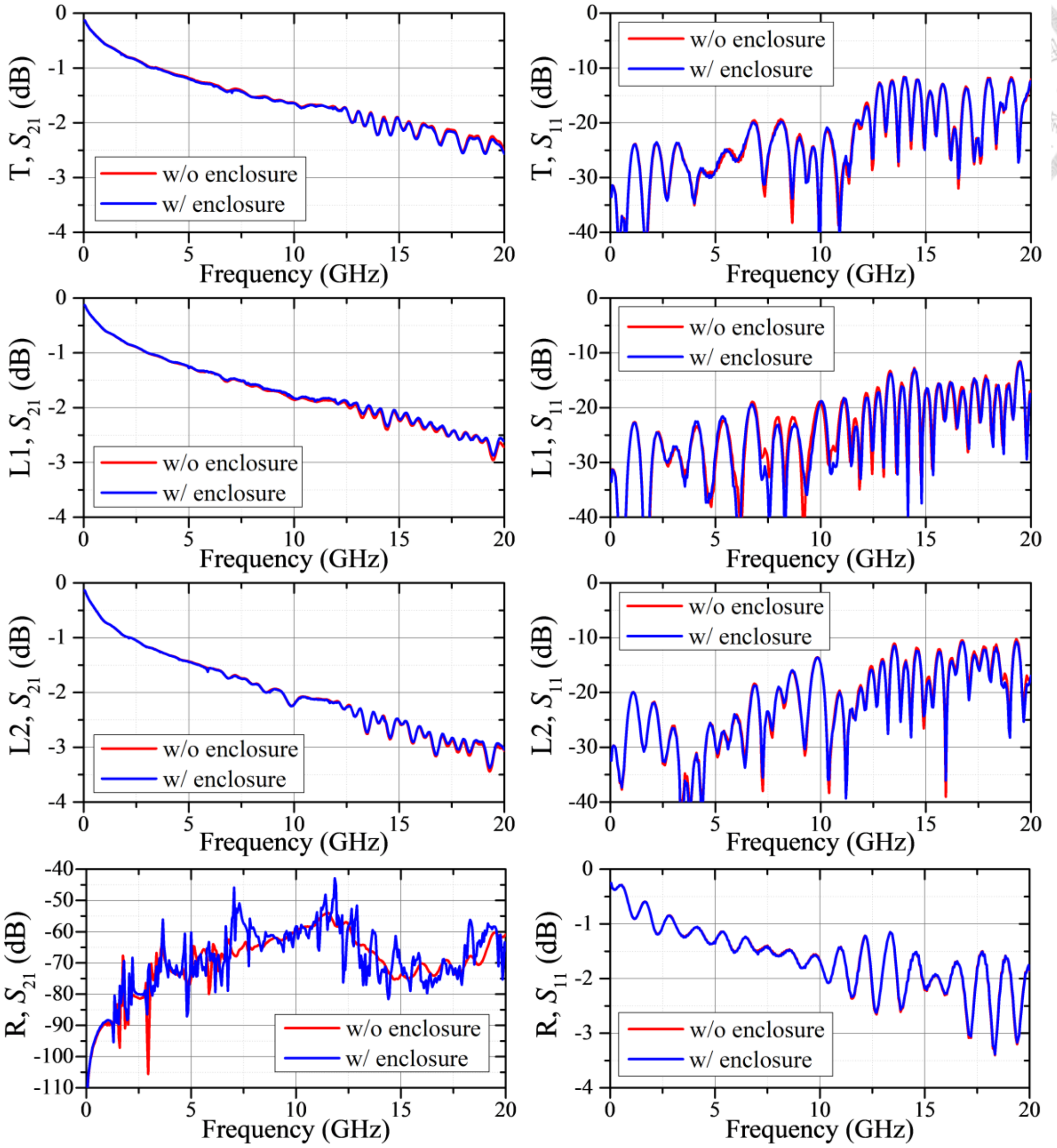

Figure 4.16: Measured responses of the SMPS_TRL1L2_HOR board with and without the sample puck enclosure.

measured results of the SMPS_TRL1L2_HOR board with and without the sample puck enclosure. The CBCPW transmission lines confine most of the field inside the semi-coaxial-like structure, resulting in negligible differences for the transmission-type standards. However, for the Reflect standard, although only minor variations are observed in the return loss, the enclosure influences the transmission of the leakage power. A small amount of the radiation at the shorting end travels inside the cavity and reflects off the metallized enclosure, thereby transmitting to the port at the other end.

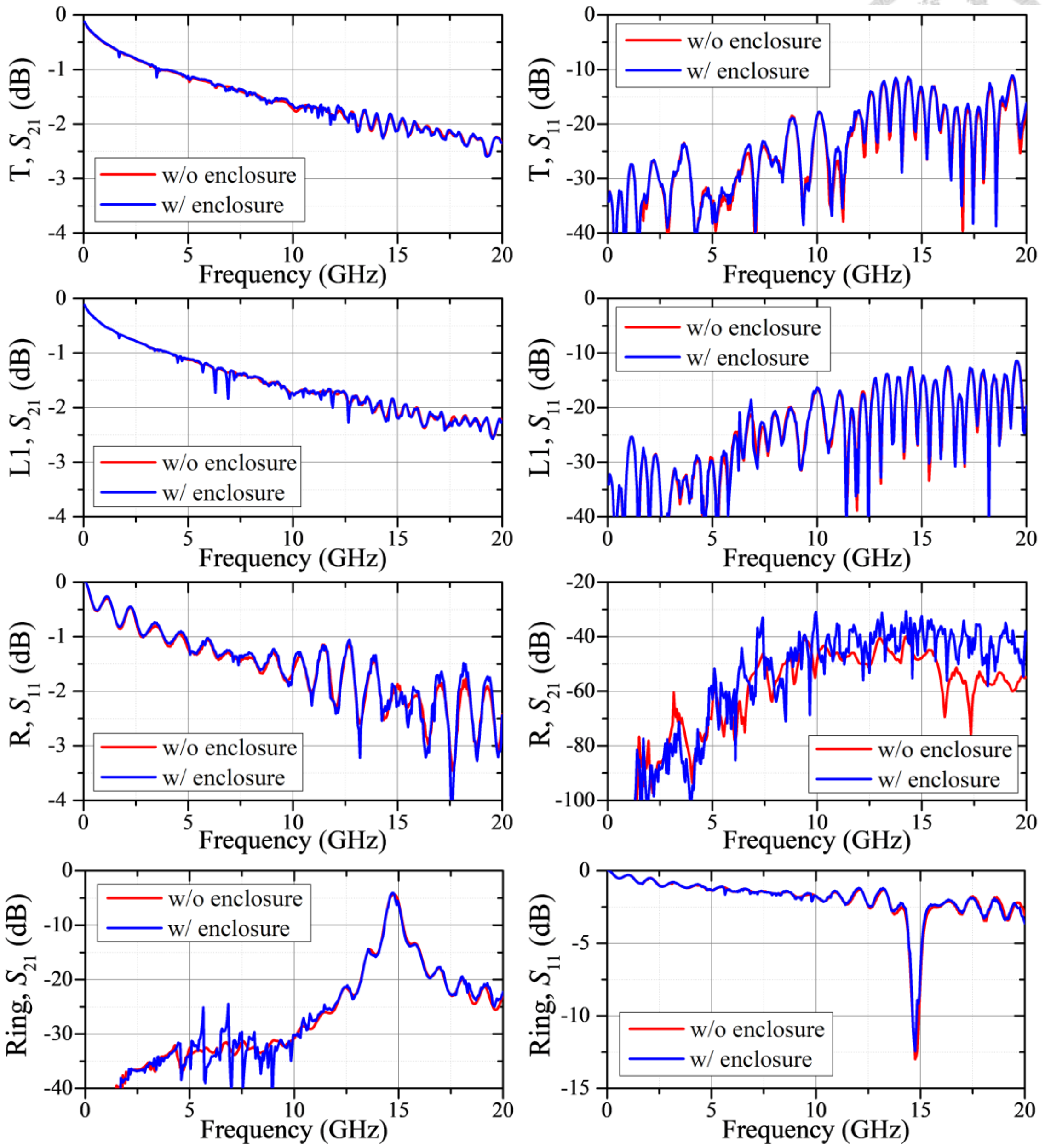

Figure 4.17: Measured responses of the SMPS_MS_TRL1RING_HOR board with and without the sample puck enclosure.

The comparison of the MS transmission lines shows inferior characteristics compared to the CBCPW structure at higher frequency ranges. Illustrated in Figure 4.17, even the simple transmission lines are affected when the enclosure is covered. At moderately high frequencies of around 20 GHz, the inclusion of the enclosure increases the leakage power to around -30 dB for the Reflect standard. Furthermore, the responses of the ring resonator also display some disparities, with variations observed in the resonance dip pattern. These results reaffirm that, although MS lines occupy a smaller

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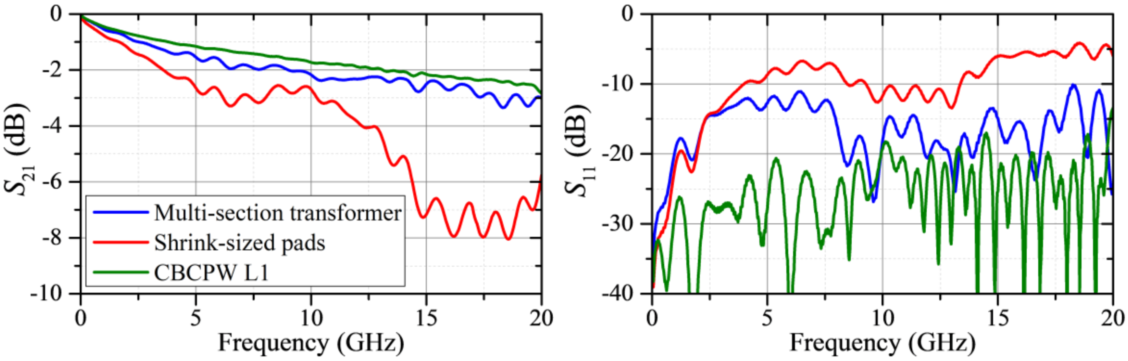

Figure 4.18: Overall measured responses of transmission-line-to-bond-wire transition structures, compared with L1 responses.

footprint compared to CBCPW lines, the expending electric field lines make them susceptible to coupling with nearby signal tracks and affected by the reflection of the surrounding metallized enclosure.

Besides the RF routing designs, we also discussed the impact of bond wires on high-frequency signals. Figure 4.18 compares the measured responses of transmission-line-to-bond-wire transitions, where the bond wires span the gap between the proposed multi-section transformer structures or the shrink-sized pads. The responses of pure CBCPW L1 are also shown. All results are measured without the sample puck, using the same blue cables and adaptors. With the proposed matching section, the harmful effect of bond wires can be effectively eliminated, resulting in a return loss remaining above 10 dB up to 20 GHz. These results demonstrate potential solutions for high-frequency signal transmission when bond-wiring the DUTs on the sample holder.

4.3.2 TRL Calibration at Room Temperature

As discussed in Section 4.2.2, a TRL calibration scheme is devised alongside the verification of the microwave transmission lines in this initial experiment phase. Ideally, the three standards and the DUT are routed and interconnected by identical structures and controllable components. By ensuring uniformity in cables, connectors, and on-board patterns, it may be possible to calibrate the error boxes before and after the standards and DUTs, even without using the same sets of interconnecting branches. Based on this

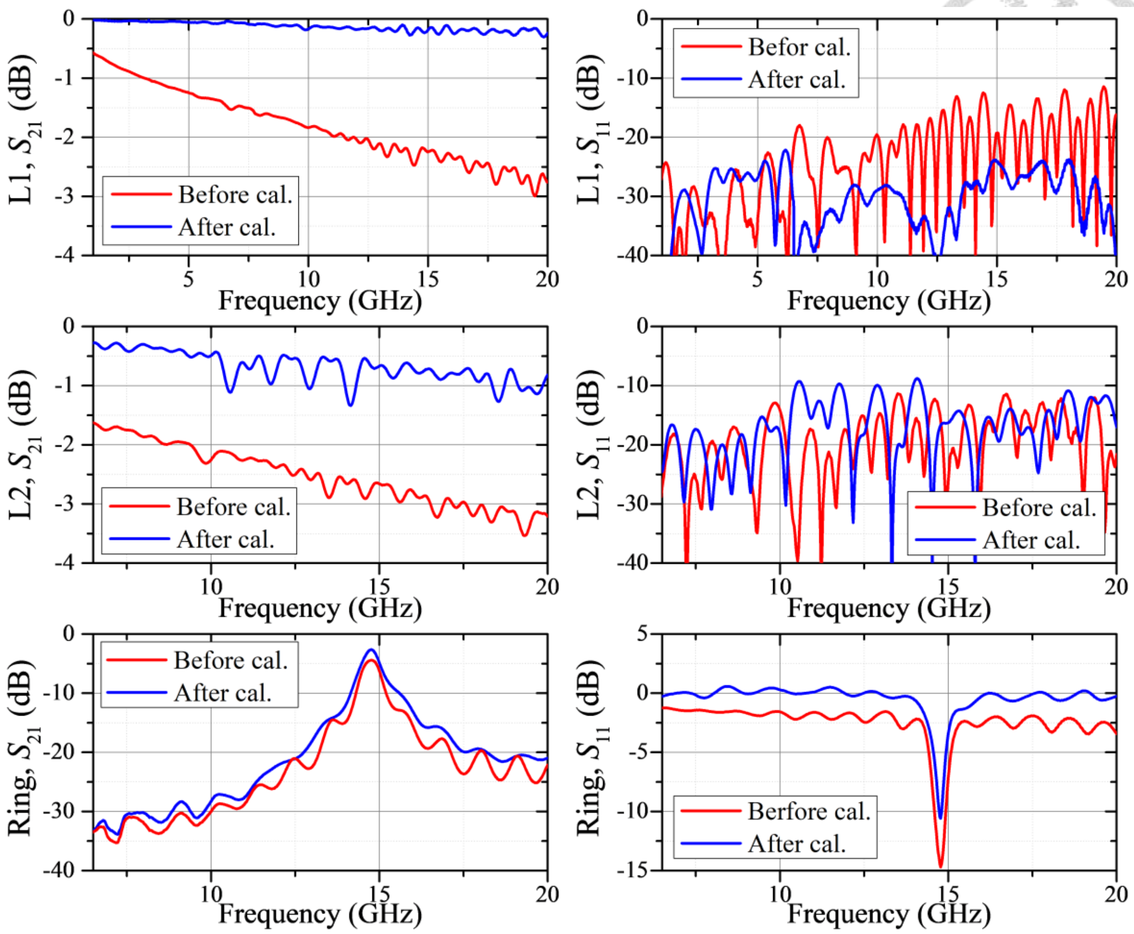

Figure 4.19: Measured responses of L1, L2 and the ring resonator as DUTs within the sample puck, before and after the TRL calibration.

hypothesis, it may also be feasible to allocate the standards and DUTs onto separate boards, conducting different rounds of measurements. This approach circumvents the constraint of the limited number of cables available in the setup and thus increasing the number of samples tested within a single calibration. Furthermore, the separate SMD component evaluation boards are designed based on this assumption.

To validate the concept, an experimental TRL calibration procedure was performed using the measured results of various standards on the SMPS_TRL1L2_HOR, SMPS_TRL1DUT_HOR, and SMPS_MS_TRL1RING_HOR boards, as described in the previous subsection. For the first-phase verification, the calibration was conducted using one of the earliest and simplest versions of the TRL algorithm [90]. The raw data of all measured standards and DUTs were processed in Matlab to obtain the calibrated

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responses. For the CBCPW transmission line platform, calibration is performed using the four standards on the SMPS_TRL1L2_HOR board. To evaluate the calibration results, the L1 standard on the SMPS_TRL1DUT_HOR board and the same L2 standard on the SMPS_TRL1L2_HOR board are used as DUTs. In the MS transmission line scenario, the ring resonator is measured as a DUT after calibration with the three other standards on the same board. Figure 4.19 illustrates the comparisons of the measured results before and after the TRL calibration. All measurements are conducted within the sample puck, under the eight-different-blue-cable configuration mentioned in the previous subsection. The calibration bandwidth of the algorithm is constrained by the electrical length of the line standard. Specifically, in this experiment, the L2 standard covers frequencies from 1 GHz to 6.5 GHz, while the L1 standard covers frequencies beyond 6.5 GHz. Consequently, the calibrated L1 measurement data in Figure 4.19 exhibits a small discontinuity and different behavior surrounding 6.5 GHz frequency point. Conversely, the L2 and the ring resonator are plotted from 6.5 GHz onwards, where the TRL calibration using only L1 as the line standard takes place. The calibration effectively removes path loss for the two CBCPW transmission line cases. Additionally, it results in a much closer 3-dB bandwidth and transmission loss for the ring resonator compared to simulation. However, the calibrated results exhibit two significant flaws. Firstly, as described earlier, there’s a discontinuity due to the line standards covering separate bandwidths and the use of a straightforward calibration algorithm. Secondly, there are post-calibration ripples. In the worst scenario, such as with the L2 results, the calibration exacerbates the ripples, leading to increased uncertainty and even worsening return loss behavior.

As described in Sec. 4.3.1, under the second configuration without integrating the sample puck, measurements were performed using two identical blue cables and adaptors

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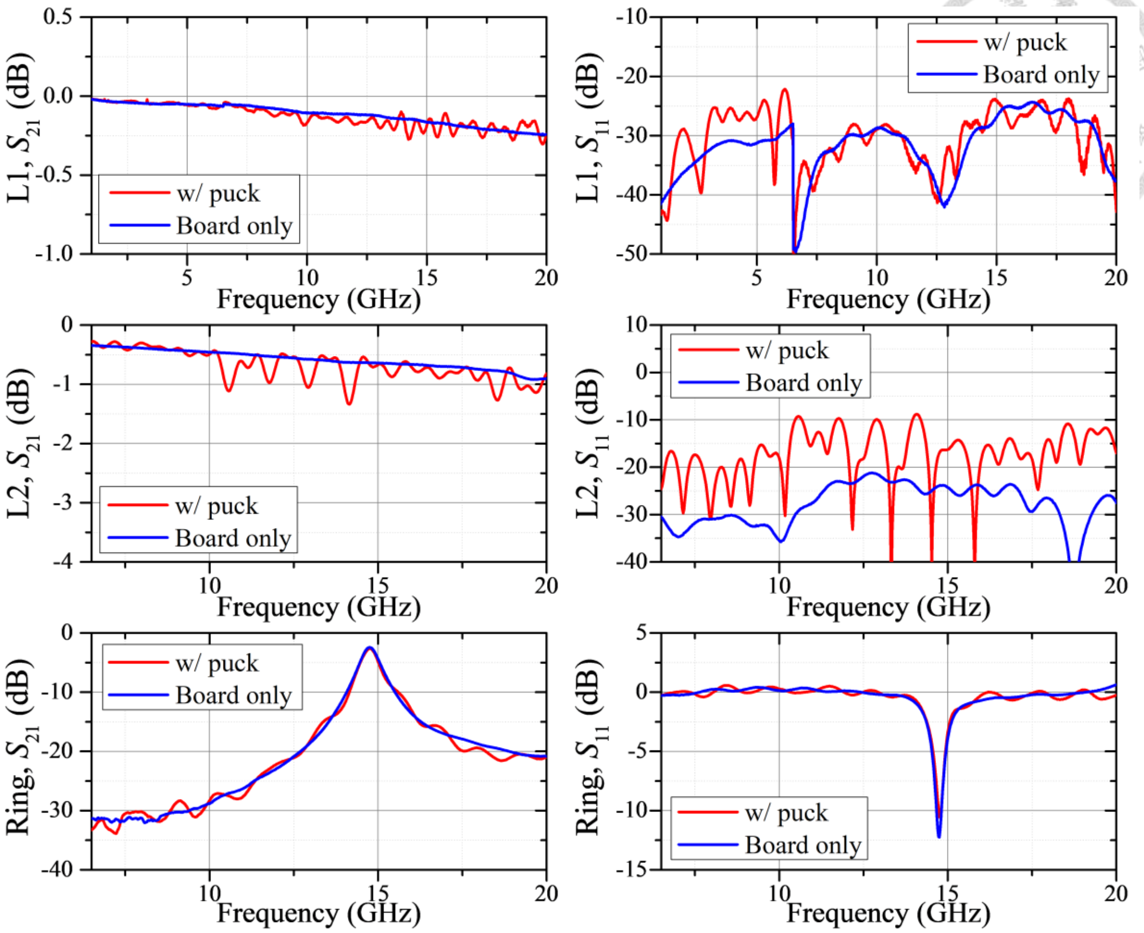

Figure 4.20: Calibrated responses of L1, L2 and the ring resonator as DUTs, measured with the board alone and within the sample puck.

across all standards and DUTs. Figure 4.20 compares the calibrated measurement results of the two configurations with the same standards and DUTs. Using the same cables and adaptors for all measurements effectively removes the harmful ripples. This indicates that differences in error boxes across each standard and DUT are the main cause of the uncertainties in this calibration scheme. Notably, the L2 case shows a significant improvement in return loss in addition to the reduction of ripples.

To further identify the possible error sources, we also tried to use the build-in TRL calibration scheme in the Keysight VNA. However, the results exhibited the same issues of ripples and discontinuities. After excluding potential errors from the custom algorithm, we measured several combinations using the build-in TRL calibration function in the VNA. Without the sample puck, we tested two scenarios: one using the same two blue

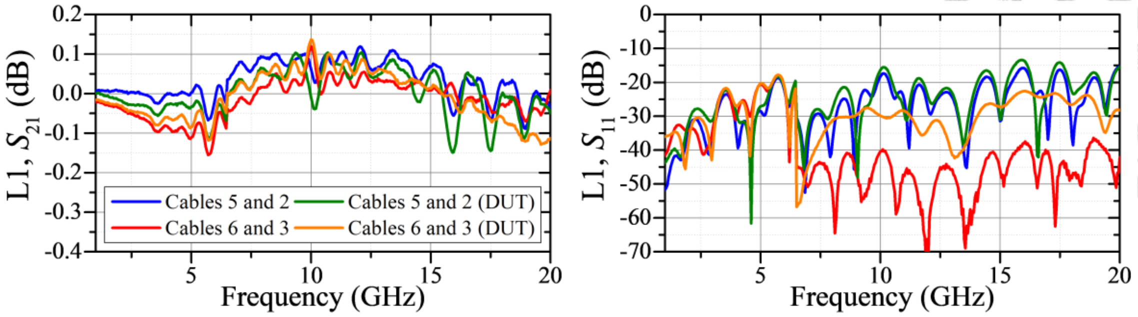

Figure 4.21: Calibrated responses of L1 as DUT, measured using cables 5 and 2 or cables 6 and 3. The label 'DUT' indicates results measured for L1 on the SMPS_TRL1DUT_HOR board, while the unlabeled results are for L1 on the SMPS_TRL1L2_HOR board.

cables across all standards and DUTs as before, and the other using eight different cables for each standard measurement. The cable labeling for the second case is as follows: Thru using cables 8 and 7, L1 using cables 6 and 3, L2 using cables 5 and 2, and Reflect using cables 4 and 1. For both scenarios, calibrations are conducted using the TRL standards on the SMPS_TRL1L2_HOR board. In the second scenario, the L1 calibrated results are depicted in Figure 4.21, where the L1 responses are measured using either cables 5 and 2 or cables 6 and 3. The label 'DUT' indicates results measured for L1 on the SMPS_TRL1DUT_HOR board, while the unlabeled results are for L1 on the SMPS_TRL1L2_HOR board. As in the previous experiments, the results above 6.5 GHz are calibrated using the L1 standard, while the results from 1 to 6.5 GHz are calibrated using the L2 standard. Therefore, the return loss responses exhibit obvious discontinuities. These comparisons reveal several key features. First, when measuring using cables 6 and 3, which are the same cables used for measuring the L1 standard during calibration, the calibrated return loss above 6.5 GHz shows the best results. In this case, not only are the cables the same, but the DUT measured is also the same L1 used in the calibration, resulting in ideal outcomes. In the second-best case, still using cables 6 and 3 but measuring a different L1 on the other board as the DUT, the return loss significantly

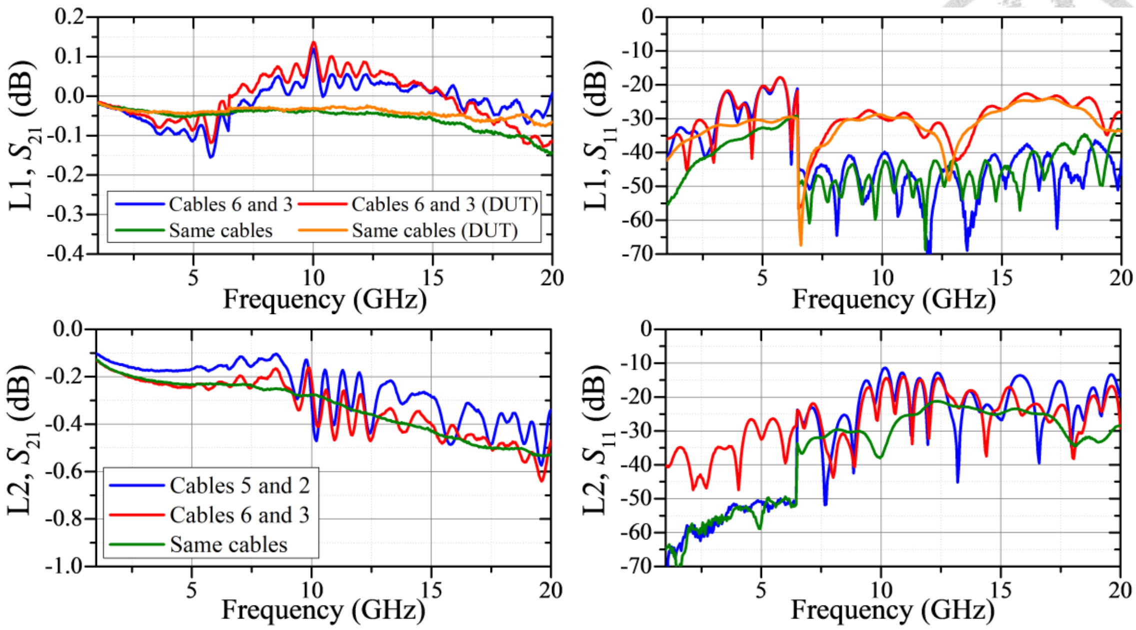

Figure 4.22: Calibrated responses of L1 and L2 as DUTs, measured using cables 6 and 3 or cables 5 and 2, also compared with the cases that using the same two blue cables throughout the calibration and measurement. The label ‘DUT’ indicates results measured for L1 on the SMPS_TRL1DUT_HOR board, while the unlabeled results are for L1 on the SMPS_TRL1L2_HOR board.

degrades. This indicates electrical path disparities between different boards, mainly due to variations in soldering and connectors. In the worst-cases scenario, using cables 5 and 2, the results show less difference between the two boards. This suggests that cable differences are the dominant source of error in this calibration scheme.

To clarify the impact of using different blue cables across each standard, the L1 measured results in Figure 4.22 include comparisons with cases that use the same cables throughout calibration and measurements. Using different cables for Thru and Reflect standard measurements results in increased ripples and slightly uncertainty in the transmission responses.

Similar conclusions can be drawn from the calibrated L2 responses below 6.5 GHz in Figure 4.22. When using cables 5 and 2, where the setup and DUT resemble the L2 standard during calibration, the result is an ideal calibrated return loss response. Additionally, using the same two blue cables for all standards eliminates ripples in the calibrated transmission response. Conversely, the degraded return loss observed when using cables 6 and 3 demonstrates the negative effect of using different cables, even when measuring the same standard as the DUT.

When both L1 and L2 are involved in calibration and measurement, the effect becomes more intricate. In the second scenario of using different cables for the standard measurements, as shown in Figure 4.21 and Figure 4.22, there is merely difference in which pairs of the cables are used, also with less variance in which L1 is measured as the DUT, for both the L1 calibrated responses below 6.5 GHz and the L2 calibrated responses above 6.5 GHz. The only distinction arises when measuring all the standards and DUTs using the same pairs of blue cables, where the return loss level aligns with that of the case of measuring a different L1 from the standard using cables 6 and 3 in Figure 4.22. This result could thus be attributed to the disparity in soldering and connectors between L1 and L2. On the other hand, the similar calibrated results obtained using different cables across each standard indicate that the differing multi-reflection responses of the L1 and L2 on-boards soldering and connectors exaggerate the discrepancy to a similar degree, even when using the same cables for L1 and L2 measurement. This can be compared to the difference between the two calibrated results of the non-standard L1 using fixed or different blue cables in Figure 4.22 without the involvement of L2, and only ripples are enhanced.

In summary, the first-phase calibration scheme discussed in this chapter is affected by the electrical path differences among error boxes associated with each standard and DUT, encompassing factors such as the adaptors on the sample puck, cables, connectors, soldering disparities, and other non-ideal effects. In this simplified experiment conducted at room temperature without integrating into the dilution fridge, the number of error sources have been limited to a more manageable extent, allowing for several analyses to

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be undertaken. However, this somewhat straightforward calibration scheme yields slightly suboptimal results even when confined within the sample puck, suggesting room for improvement in advancement.

4.4 RF Characterization within Dilution Fridge

Following initial verification in the sample puck, the first-phase testing boards are integrated into the dilution fridge system for further validation of practical functionality. The sample puck, housing the testing boards, is bottom-loaded into the cryogenic measurement system of Triton 500 from Oxford Instruments. In this system, the mixing chamber plate reaches a temperature around 20 mK when cooling to the base temperature. Eight microwave cables, capable of transmitting frequencies up to 18 GHz, are routed from the top exterior of the dilution fridge at room temperature, descend through different cooling plates, pass through the adaptors on the sample puck, and connect to the testing boards via the blue cables. In the initial configuration, each branch of the microwave cables is equipped with 10 dB, 20 dB, and 6 dB attenuators at PT1, PT2, and the still plate, respectively, to thermalize the black body radiation and reduce the signal level.

To begin, the microwave system is evaluated at room temperature using the same SMPS_TRL1L2_HOR and SMPS_MS_TRL1RING_HOR boards as in the previous section. The configuration within the sample puck resembles that shown in Figure 4.13, with the eight blue cables connecting via adaptors on the sample puck to eight separate cable branches within the dilution fridge. A portable VNA, calibrated with Ecal, is connected to the front-end of the two 2.92-mm cables and manually measures across the eight different SMA connectors on the top exterior of the dilution fridge.

Figure 4.23 illustrates the measured responses of each standard and DUT on the two boards at room temperature, revealing several interesting and unexpected phenomena. Firstly, the insertion loss responses of all transmission lines begin at nearly -72 dB,

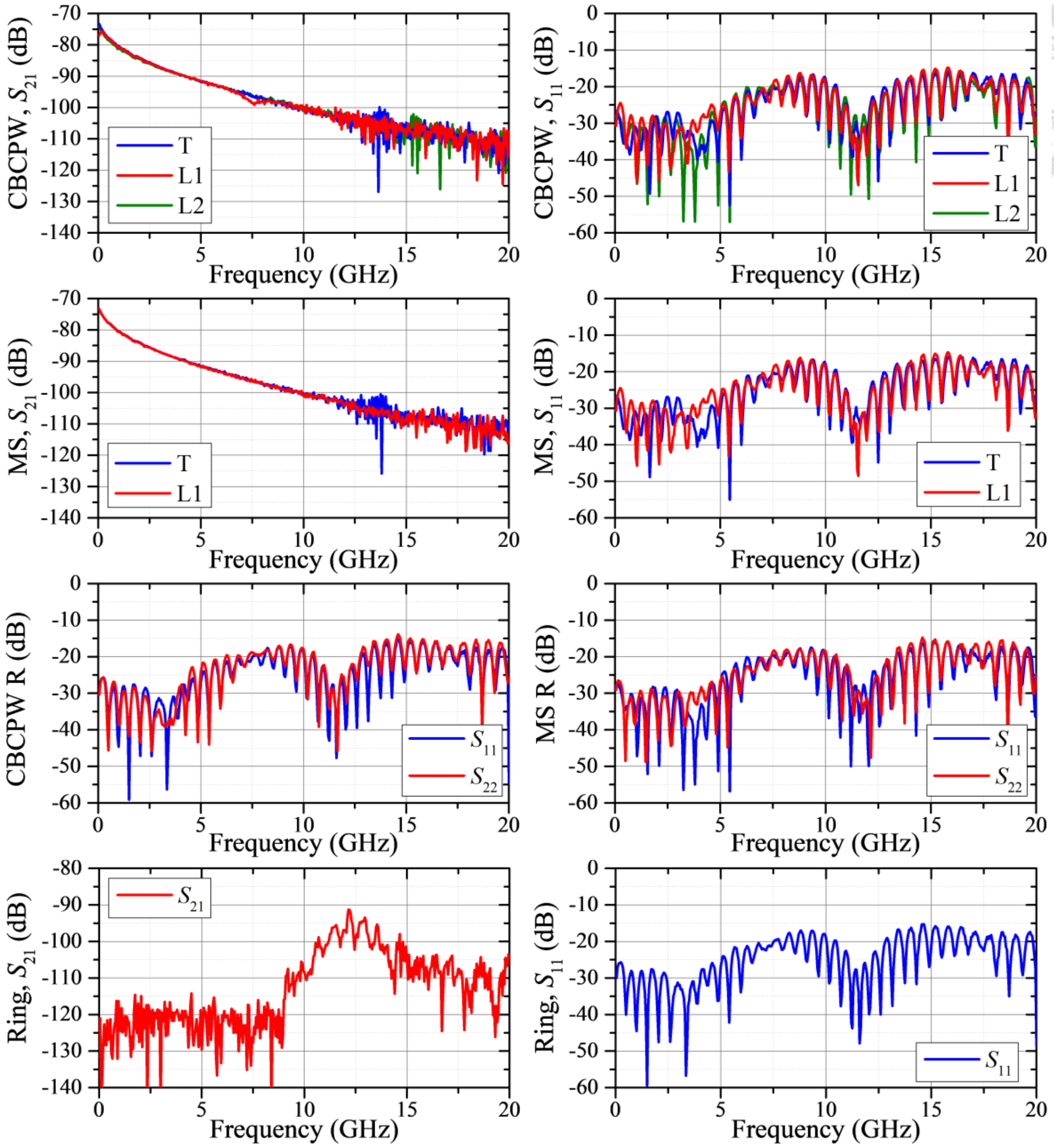

Figure 4.23: Measured responses of the first-phase testing boards within the dilution fridge (with attenuators) at room temperature.

corresponding to the two 36 dB attenuation values on each cable branch. The additional insertion loss at higher frequencies thus arises from other cable and interconnection losses. Remarkably, for both CBCPW and MS transmission lines, the electrical length on the testing boards shows no discernible difference in insertion loss. Apart from a minor concavity, potentially due to loose inter-plate connections, in the CBCPW L1 transmission response, the insertion losses among T, L1 and L2 are nearly identical, even when compared with the SMPS transmission lines. This suggests that the cable and

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interconnection losses in the dilution fridge dominate the entire system.

Secondly, instead of closely maintaining around 0 dB, the return loss of the Reflect standard behaves strangely, resembling a well-matched response. This behavior is attributed to the attenuation on each cable branch. As the reflected signal travels downward and upward, experiencing twice the 36-dB attenuation, the originally nearly total reflection response undergoes degradation similar to the transmission response of the transmission lines, ideally resulting in a return loss larger than 72 dB. However, due to the non-idealities on each interconnecting plane, the initially triggered signal from the exterior of the dilution fridge may encounter multiple reflection when travelling down to the sample puck. This leads to the return loss measured in Figure 4.23, which is, in fact, the reflected responses of the non-ideally matched interphases in the cable branch before entering the sample puck. This argument can be validated by comparing the measured return loss between each component in Figure 4.23. Since the cable branches of port one used for measuring the T and L1 are the same for both CBCPW and MS cases, the measured return losses are identical. A similar situation can be observed in the resemblance between the port one return loss of CBCPW L2 and MS Reflect, as well as between CBCPW Reflect and the ring resonator.

The transmission response of the ring resonator deviates from the measured results within the sample puck alone, especially at the resonance frequency point. This discrepancy arises due to the degraded insertion loss of the transmission response at higher frequencies, which diminishes the resonance peak.

Overall, although the measurement system seems successfully transmits microwave signal in the desired bandwidth at room temperature with a return loss well above10 dB, the undistinguishable return loss among the DUTs and standards, also the highly identical insertion loss of various length of transmission lines, suggest the failure of applying the

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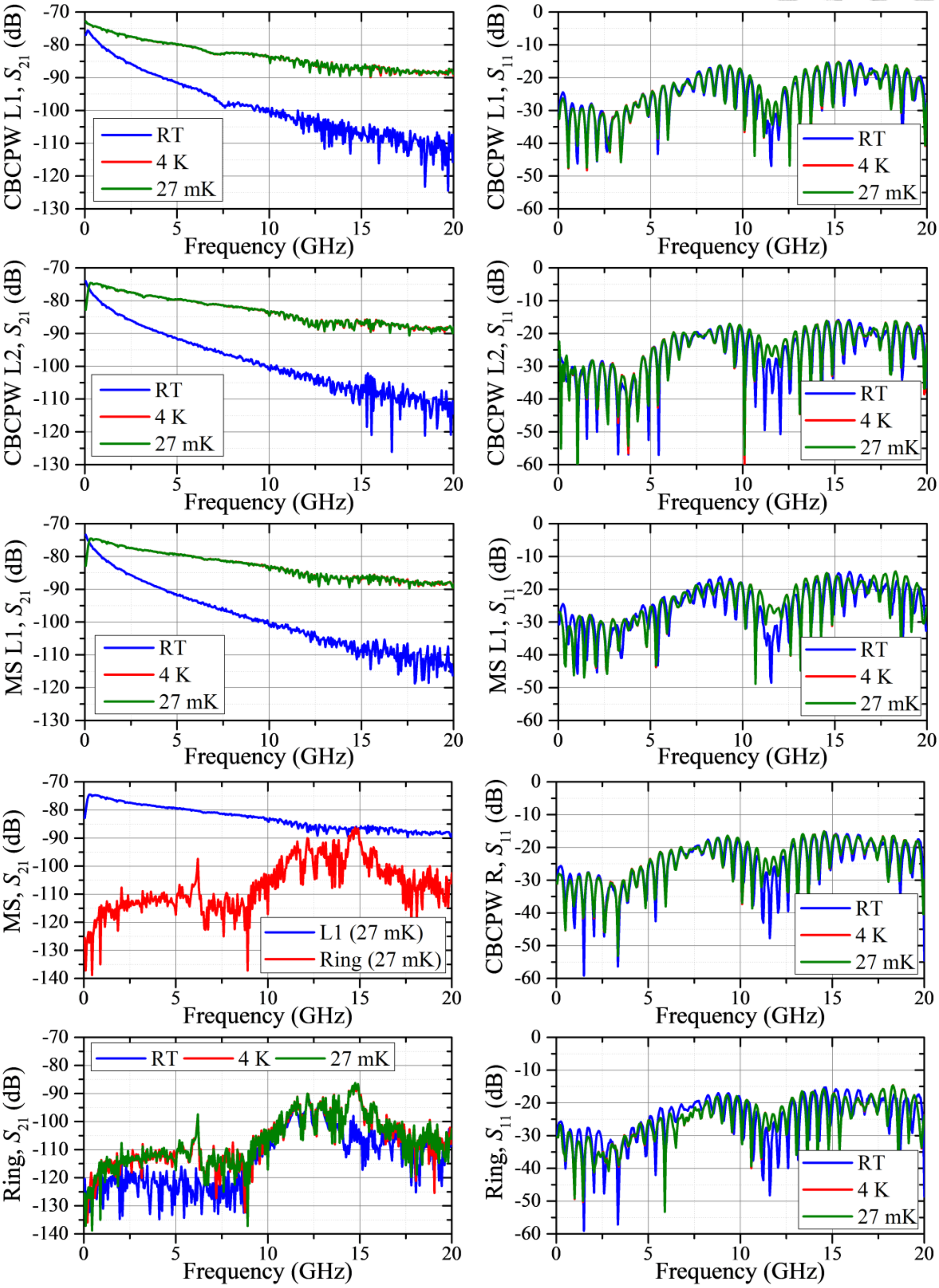

Figure 4.24: Comparison of the measured responses of the first-phase testing boards within the dilution fridge (with attenuators) at various temperatures.

straightforward calibration scheme discussed in previous section directly to the microwave system within the dilution fridge.

To verify the cryogenic functionality of the microwave designs and the mechanical properties of the materials selected for the first-phase testing boards, the dilution fridge was cooled down to the base temperature, monitored at around 27 mK during the measurements. Since one of the purposes of the sample holder experiments in this chapter is to package control and readout integrated circuits, which operate at a temperature of 4 K, the dilution fridge was also warmed up to the corresponding temperature to ensure proper operation. Figure 4.24 compares the measured responses of the testing boards within the dilution fridge at various temperatures, demonstrating that the measured results at 4 K and 27 mK closely match each other. At cryogenic temperatures, some sections of the cable branches in the dilution fridge transition into a superconducting state. This, along with reduced metal loss along the electrical path, significantly lessens the degradation of insertion loss at higher frequencies. Notably, the sharp decay of the transmission responses near dc is attributed to slightly loose cable connections, as this issue does not occur in other measurements and can be avoided by carefully examining the setup.

The measured return losses show only slight deviations with temperature variations, still indicating reflections at higher plates rather than from the device under test. In contrast to the room temperature results, the resonance peak of the ring resonator is clearly observed at cryogenic temperatures, as the reduced insertion loss of the transmission signal prevents attenuation of the peak.

Overall, the cryogenic measurement results validate the functionality of the first-phase testing board materials and assess the microwave channels within the dilution fridge system. While the initial experiments verify the effective propagation of high-frequency signals, the indistinguishable results between various calibration standards constrain the feasibility of conducting precise microwave calibration.

To explore the potential of the straightforward calibration scheme within the dilution

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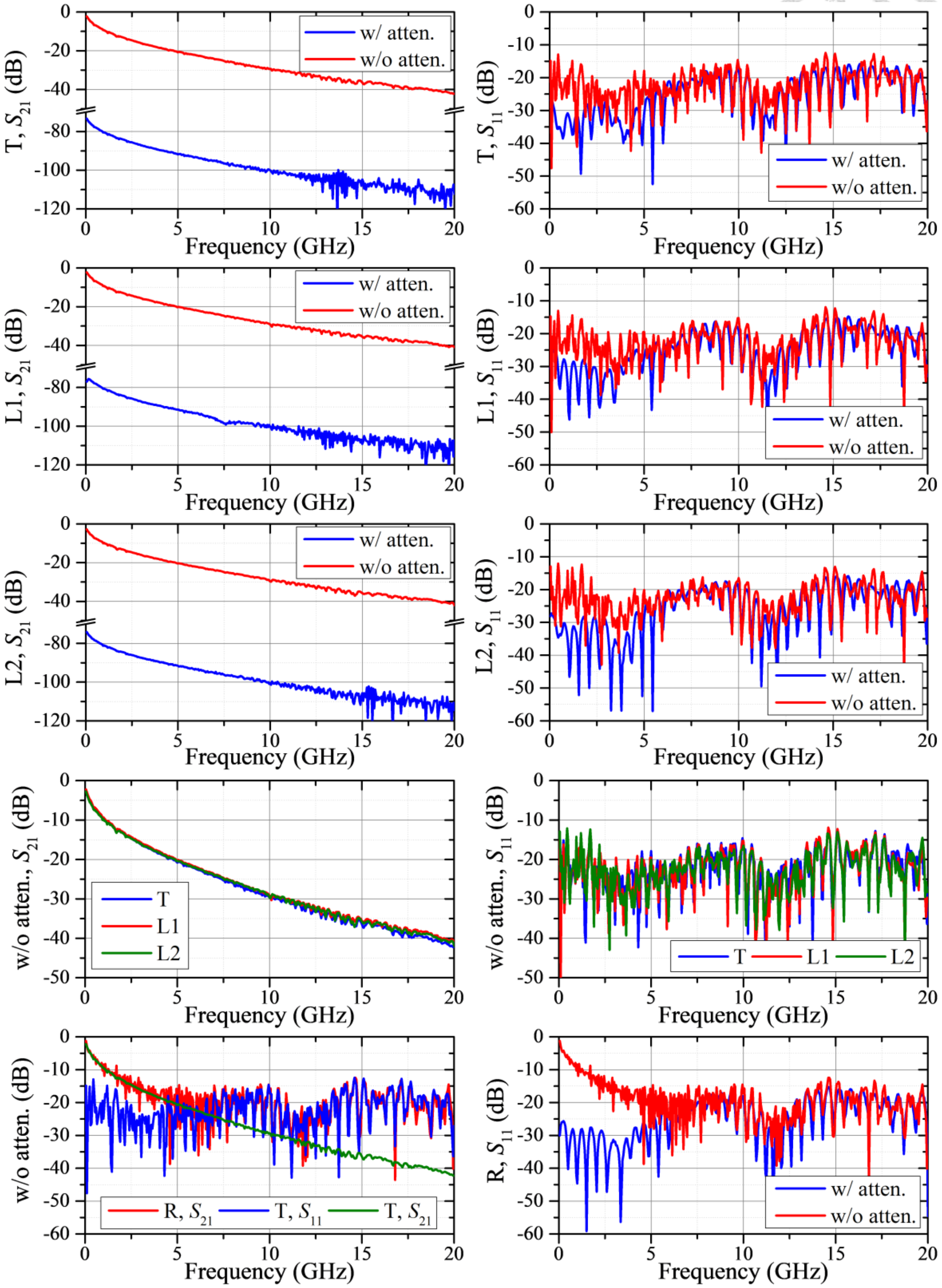

Figure 4.25: Measured responses of the SMPS_TRL1L2_HOR board within the dilution fridge, with and without attenuators, at room temperature.

fridge, the attenuators on each cable branch are replaced by 0 dB adaptors. This adjustment aims to overcome the limitation of identical responses caused by the attenuation of the preferred reflection signals. Figure 4.25 depicts the measured responses of the standards on the SMPS_TRL1L2_HOR board at room temperature, both with and without the attenuators. Comparing the T, L1 and L2 transmission lines reveals that removing the attenuators shifts the responses upward by approximately 72 dB, starting from close to 0 dB at dc, with the degradation at higher frequencies comes from the propagation loss along the cable routings. The measured return losses are worse without the attenuators, especially at lower frequencies. This is attributed to the use of cheap, non-cryogenically specified adapters in this first-phase experiment. Although using better adapters might improve matching at each discontinuous plane, the non-optimal parts used here still provide acceptable results for further exploration. Unfortunately, when stacking the responses of the three transmission lines of different electrical lengths, the insertion losses are not only similar to each other, but the order of the degradation also deviates from the expected correlate with length. This discrepancy raises concerns about potential errors in the calibration results. The results of the Reflect standard exhibit an interesting effect when the attenuators are removed, with the return loss starting from 0 dB at dc, behaving as expected for a reflection response. However, at higher frequencies, the reflected responses with and without attenuators almost match each other, implying that the desired reflection from the device under test is overshadowed by the reflections from the discontinuities of upper layer plates. This phenomenon is further verified by stacking the insertion loss of the transmission line with the reflection signals, revealing that above around 6 GHz, the measured return loss is from the system, rather than the device. This indicates that, even disregarding the issue of insertion loss magnitude, the feasibility of conducting the calibration scheme is limited to a specific frequency range.

The similar comparisons with the SMPS_TRL1DUT_HOR board are illustrated in Figure 4.26. The insertion losses of the transmission lines reaffirm that systematic variance in propagating loss dominates the standard measurement, resulting in the results

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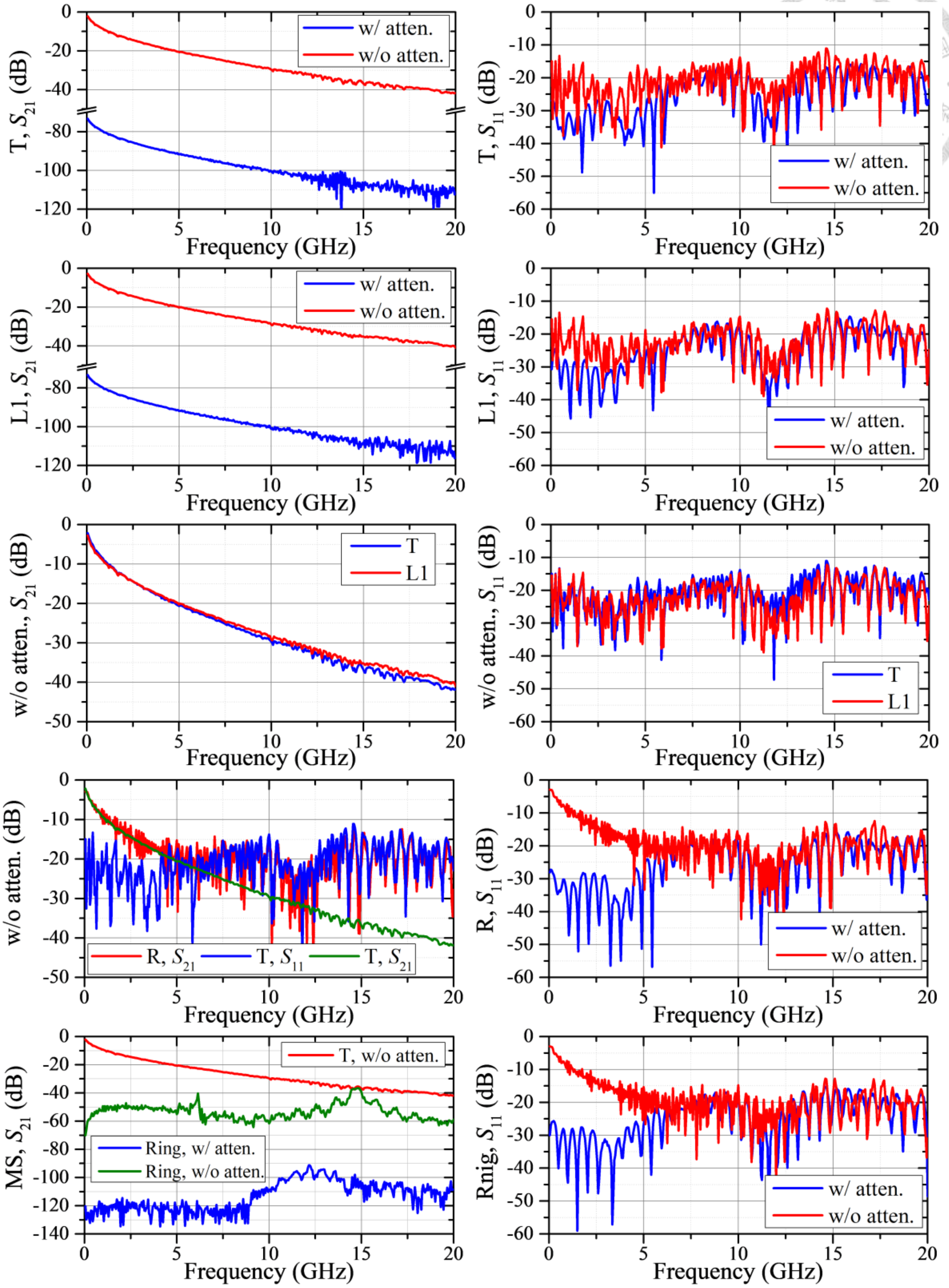

Figure 4.26: Measured responses of the SMPS_MS_TRL1RING_HOR board within the dilution fridge, with and without attenuators, at room temperature.

opposite to the expectation in this case. Without the attenuators, the resonance peak of the ring resonator is allowed to reach the magnitude of that of the propagation loss of the transmission lines. Once again, the limited available bandwidth for obtaining valid

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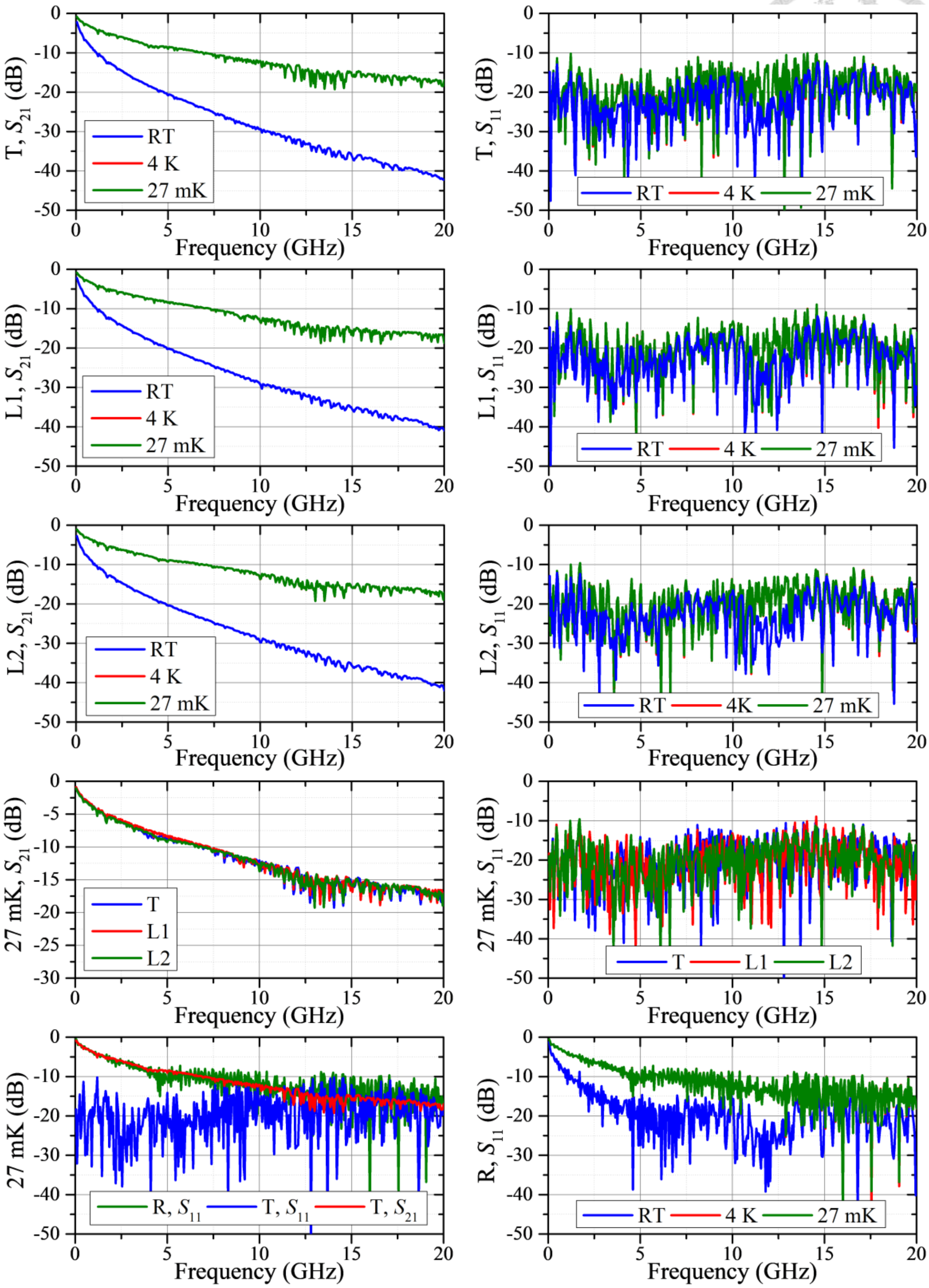

Figure 4.27: Measured responses of the SMPS_TRL1L2_HOR board within the dilution fridge (without attenuators) at various temperatures.

reflected responses hampers the possibility of calibrating the ring resonator responses for further analysis of electrical properties of board materials.

Without the attenuators, the dilution fridge system underwent another cycle of

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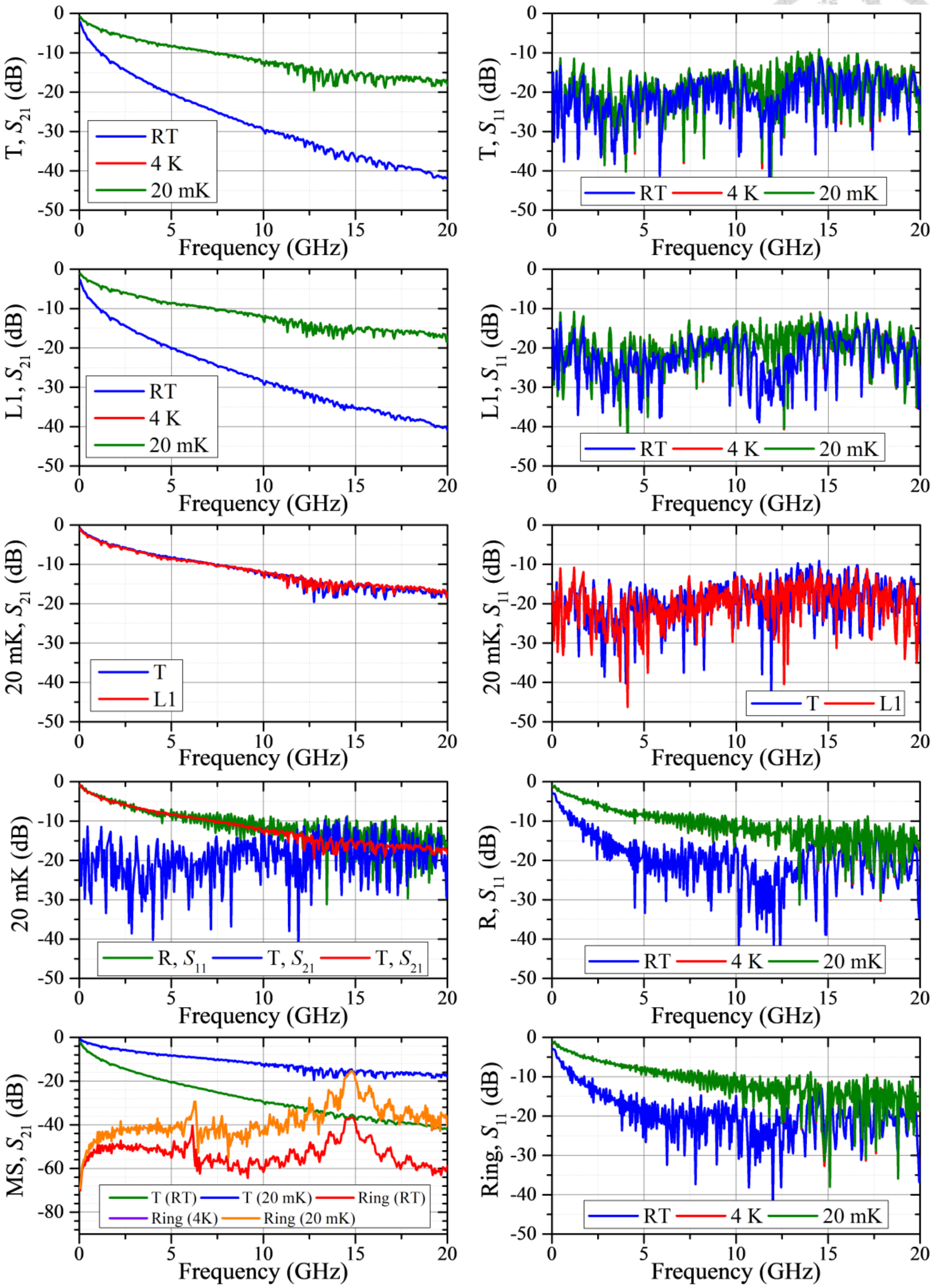

Figure 4.28: Measured responses of the SMPS_MS_TRL1RING_HOR board within the dilution fridge (without attenuators) at various temperatures.

cooling, reaching a temperature of around 27 mK, before being warmed back up to 4 K, as illustrated in Figure 4.27, demonstrating consistency at these two temperatures. At cryogenic temperatures, the insertion loss degradation is significantly reduced, but the

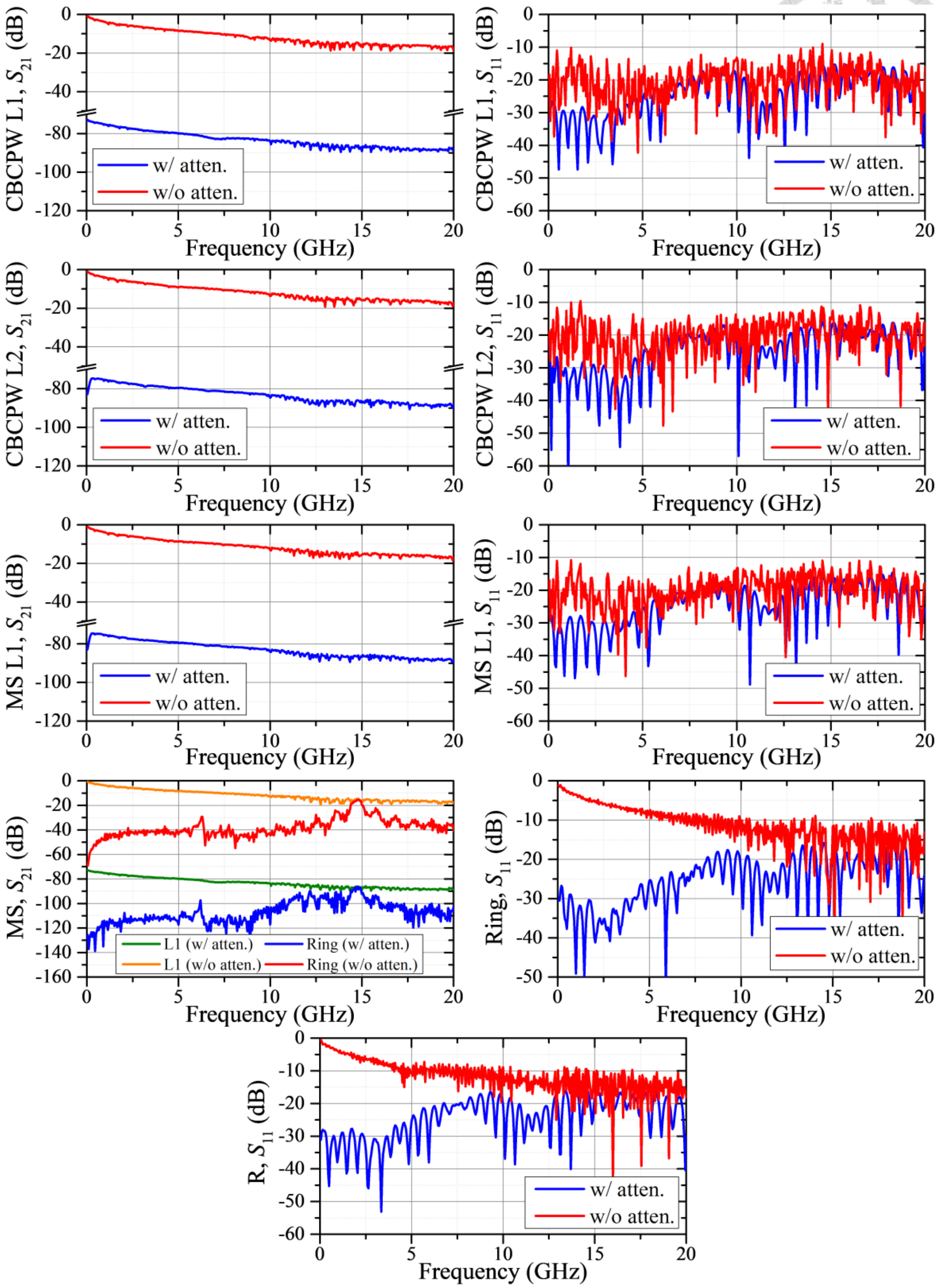

Figure 4.29: Measured responses of the first-phase testing boards within the dilution fridge, with and without attenuators, at a temperature of 27 mK.

return losses worsen further, which is understandable given that the adaptors used are not cryogenically specified. Stacking insertion loss and reflection responses reveals that as the propagation loss decreases, the frequency bandwidth with valid measured return loss data expands, potentially covering the entire desired band or at least extending safely up to 12 GHz. Nevertheless, even after replacing the adaptors to address return loss issues, the comparison of insertion losses of T, L1 and L2 expresses the same possible issue of systematic interference, raising doubts about the feasibility of the straightforward calibration scheme.

A similar comparison measuring the SMPS_MS_TRL1RING_HOR board is depicted in Figure 4.28, where the responses generally show trends and relationships similar to those of the SMPS_TRL1L2_HOR board. The ring resonator transmission responses clearly demonstrates the influence of full-round insertion loss on the peak magnitude and shape.

Finally, at the base temperature of the dilution fridge, Figure 4.29 compares the measured results with setups incorporating either the attenuators or the adaptors. Despite the deteriorated return loss with the adaptors, especially at lower frequencies, the similar curve trend of the transmission responses confirms that the measured results originate solely from the controlled attenuation. The disparate return loss behaviors of the ring resonator and Reflect standards demonstrate that removing the attenuators effectively unveils the actual responses from the device under test. This suggests that reducing the full-round electrical path loss at higher frequencies allows for the extraction the obscured signals within the dilution fridge system.

As a concluding investigation of the first-phase characterization within the dilution fridge, the straightforward calibration scheme in Sec. 4.3.2 is conducted using the measured results of the SMPS_TRL1L2_HOR board in Figure 4.27 as the standards, and re-measuring the same L1 and L2 standard as the DUTs. The calibrated responses of L1 and L2 are depicted in Figure 4.30. As noted in Sec. 4.3.2, the responses above 6.5 GHz are from using L2 as the line standard, while those below 6.5 GHz use L1, resulting in an

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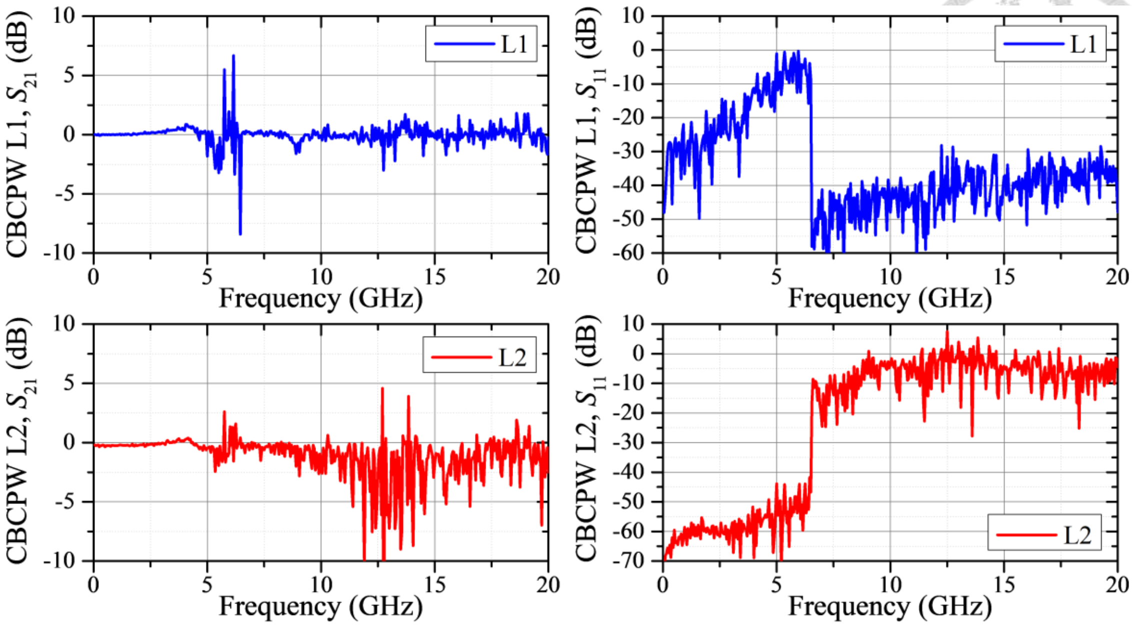

Figure 4.30: Calibrated responses of L1 and L2 on the SMPS_TRL1L2_HOR board as DUTs within the dilution fridge without attenuators, at a temperature of 27 mK.

obvious discontinuity. By comparing the calibrated results in Figure 4.30 with those obtained within only the sample holder in Sec. 4.3.2, it is evident that incorporating the eight different cable branches in the dilution fridge system within the error boxes significantly deteriorates the calibration results. In practice, since the DUT and the standards use different cable branches, calibration uncertainties are evident in the responses in Figure 4.30, particularly in the frequency ranges where different lines are used as the DUT and the line standard.

4.5 Summary

As a foundational component of cryogenic measurements within the dilution fridge, the design and verification of the sample holder require meticulous attention and careful organization. In this chapter, we review relevant literature reports and commercial products while outlining targeted experiments that encompass various potential functionalities for future research. The development of the sample holder entails not only electrical and microwave engineering challenges but also mechanical and cryogenic material examinations. Through systematic and incremental exploration of the initial testing boards, the prototype's functionalities are analyzed and validated at both room and cryogenic temperatures. However, despite the successful microwave designs within the dilution fridge demonstrated by experimental results, the proposed straightforward calibration scheme yields undesired outcomes with systematically interfered errors. Given that exploration requires the usage of the straightforward calibration scheme for other first-phase testing boards and the unavailability of samples to examine the influence of high-frequency signals on quantum devices, this initial verification concludes with validations of the operation capability of microwave circuitries and the cryogenic temperature durability of the materials. An exquisite refinement of the calibration scheme and a corresponding elaboration of sample holder structures are considered necessary for enhanced microwave measurements, a topic that will be discussed in the next chapter.

Chapter 5 *S*-parameter Calibration in mK System

5.1 Introduction

In the first-phase experiments discussed in the previous chapter, the proposed straightforward calibration scheme exhibited errors due to system uncertainties. To enhance calibration results, this subsection reviews various studies on cryogenic microwave calibration from the literature.

Similar to our straightforward calibration scheme, [91] characterizes superconducting and microwave components in the V, W, and D bands at 4 K using TRL and LRL calibrations with eight waveguide channels, assuming their consistency. The calibrated results deviate from simulations, likely due to the high-frequency bands or errors arising from these straightforward assumptions.

In some scenarios where only one-port reflective measurements are required, de-embedding is often implemented through Short-Open-Load (SOL) calibration. An interesting early work in [92] describes a rotational dial capable of switching among the three standards and the DUT, de-embedding to a reference plane at the end of CPW routing, using model-based standards in a rather narrow bandwidth at 4.2 K. Compared to the bulky mechanical rotary switching instrument, most cryogenic calibration studies incorporate electromechanical broadband switches into their systems. By equipping the electromechanical switch at the base temperature stage, along with the circulators, attenuators, and amplifiers needed for low-level probing signals, [93] measures and analyzes the quality factors and loss mechanisms of superconducting resonators after conducting SOL calibration with room-temperature data-based standards.

By incorporating an additional unknown Thru standard, [94] extends the SOL calibration to a two-port SOLT calibration scheme using room-temperature data-based

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air-line standards. By directly connecting two electromechanical switches, this scheme achieves good calibrated results from room temperature to 4 K, with residual systematic errors arising from variations between switch ports.

In [95], one-port SOL calibration with data-based standards is used to characterize the return loss of superconducting cables in qubit driving lines. By incorporating a time-gating technique, the true reflection of the cables is measured and the insertion loss is derived. In another work by the same group, [96], the researchers characterized a commercial sample holder using extended SOLT calibration with the time-gating technique. Both papers also discuss the influence of reflections from unmatched driving lines on control pulse distortion, which leads to deviations in qubit gate fidelity.

Compared to the potential deviations of model-based or room-temperature data-based standards in SOLT calibration at cryogenic temperatures, TRL calibration is inherently preferable due to its only requirement being identical Reflect standard responses for both ports. An early proposal in [97] presents an mK temperature-compatible setup incorporating electromechanical switches, directional couplers, and amplifiers, with an analysis of the system's error terms. To advance the calibration reference plane to the DUT, [98] and [99] propose custom calibration units that convert from the coaxial interface to the CBCPW calibration reference plane, enabling the characterization of integrated circuit chips, including commercial attenuator chips. Within the system, a superconducting flux qubit sample is characterized, with the de-embedded results informing the on-chip responses. In another work from the same group, [100] discusses an improved TRL calibration algorithm. Using custom standard kits, the calibration scheme achieves continuous calibrated results using a weighted function. It also de-embeds to CBCPW-ended reference planes, enabling extraction of only the IC responses involving bond-wire connections.

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The setup for measuring at mK temperatures discussed above focuses on minimizing the probing signal required for quantum-related devices. In a simplified scenario, attenuators are adjusted to an acceptable value without heating up the dilution fridge, while directional couplers and amplifiers are omitted. This setup allows reflection measurements from the same input cable with an increased probing signal magnitude. Using this simplified approach, several measurements were explored. In [101], a custom testing fixture that includes electromechanical switches is introduced. Using custom-made standards fabricated through a superconducting VLSI process, this calibration scheme allows for de-embedding up to the microstrip end in front of the chips. The paper presents calibrated results for a superconducting low-pass filter and a commercial low-noise amplifier. In [102], a coaxial interface scheme is presented, with a focus on discussing the error sources within the system.

In an effort to minimize calibration errors, [103] introduces an unconventional pseudo-open standard utilizing a quasi-2D microwave cavity. Employing Rytting's algorithm and multiple measurements, this method systematically eliminates ground variation issues that cannot be calibrated using traditional TRL techniques. In [104], [105], and the subsequent extended journal paper [106], researchers focus on implementing TRL calibration in the simplified setup using air-line coaxial cables. This approach is chosen because dielectric-filled cables, assumed to have a 50-ohm reference impedance within the calibration scheme, may deviate under cryogenic conditions. They employ a weighted algorithm for discontinuity removal to characterize various coaxial components such as attenuators, matched loads, offset shorts, and a Beatty 25-ohm mismatch line. Parameters of the air-line coaxial cable are also extracted to verify its suitability as a reference impedance standard at cryogenic temperatures.

In addition to employing electromechanical latching switches for directing

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connections across different standards and DUTs, other interface integrations have been explored in the literature. In [107], researchers propose an advanced setup incorporating a microwave wafer probe positioner within a dilution fridge. Despite the challenge of limited visibility inside the cryostat, the paper demonstrates a calibration procedure for positioning by employing TRL calibration with a strip line-based system on a PCB board. Several coupled lines are tested as DUTs. Moreover, the system includes an additional power and phase calibration transfer line, enabling nonlinear and intermodulation VNA measurements. In [108], two commercially available semiconductor integrated circuit SP4T switches are examined as substitutes for bulky electromechanical switches. Operating at 4 K, the study proposes a two-port SOL calibration method employing six standards, including ideally modeled standards and an additional numerically derived zero-length Thru standard. This calibration approach is applied to characterize a planar quasi-complementary diplexer by de-embedding it to the coaxial end. While the diplexer shows minimal deviation from referenced responses at room temperature, it exhibits more significant degradation at 4 K due to discrepancies in the calibration algorithm's assumptions.

5.2 Design of Second-Phase Testing Boards

5.2.1 Multiple Board Structure

In the second phase of testing board design, along with refining the calibration scheme, several auxiliary improvements are introduced. Firstly, a structural modification is proposed in this subsection. Instead of using a plain single-board arrangement, the sample holder is now structured into a multi-board configuration, inspired by the QDevil Qboard design. The sample holder system now comprises a motherboard, a daughter board, and an interposer. By strategically separating the high-frequency and dc routings and implementing sophisticated bypass networks on the daughterboards, the interposer

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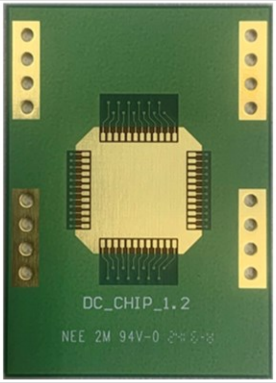
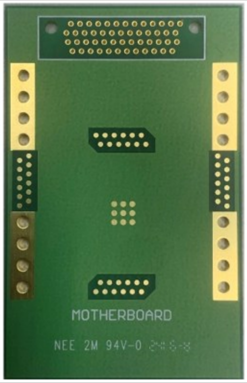
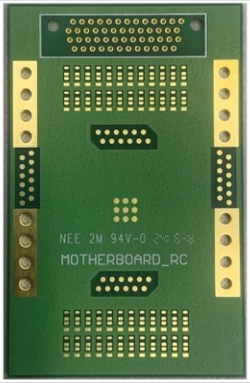
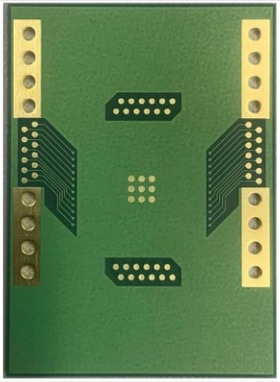
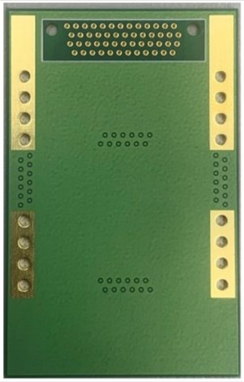
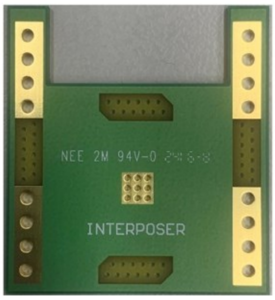
DC_Chip_1.2 (front)	**Motherboard (front)**	**Motherboard_RC**
		
DC_Chip_1.2 (back)	**Motherboard (back)**	**Interposer**
		

Table 5.1: List of the second-phase FR4 testing boards.

and motherboard handle only near-dc low-frequency signals and potentials. Meanwhile, the functionally specialized daughter boards are tailored to specific application needs. This multi-board structure allows for versatile use of the same measurement platform, enabling interchangeability of samples and measurement applications, all unified through the dc routing pad position to the interposer.

Table 5.1 lists the testing boards for near-dc low-frequency routings. Due to fewer requirements on dielectric loss and mutual coupling for these low-frequency tracks, these boards are implemented with four-layer FR4 boards. The front side of the motherboard contains 48 pads, enabling connection to the daughterboard through the interposer, while 9 ground pads are included at the center of the board for better thermal conduction. Besides these 9 ground pads, the system's grounding is connected through screws on the

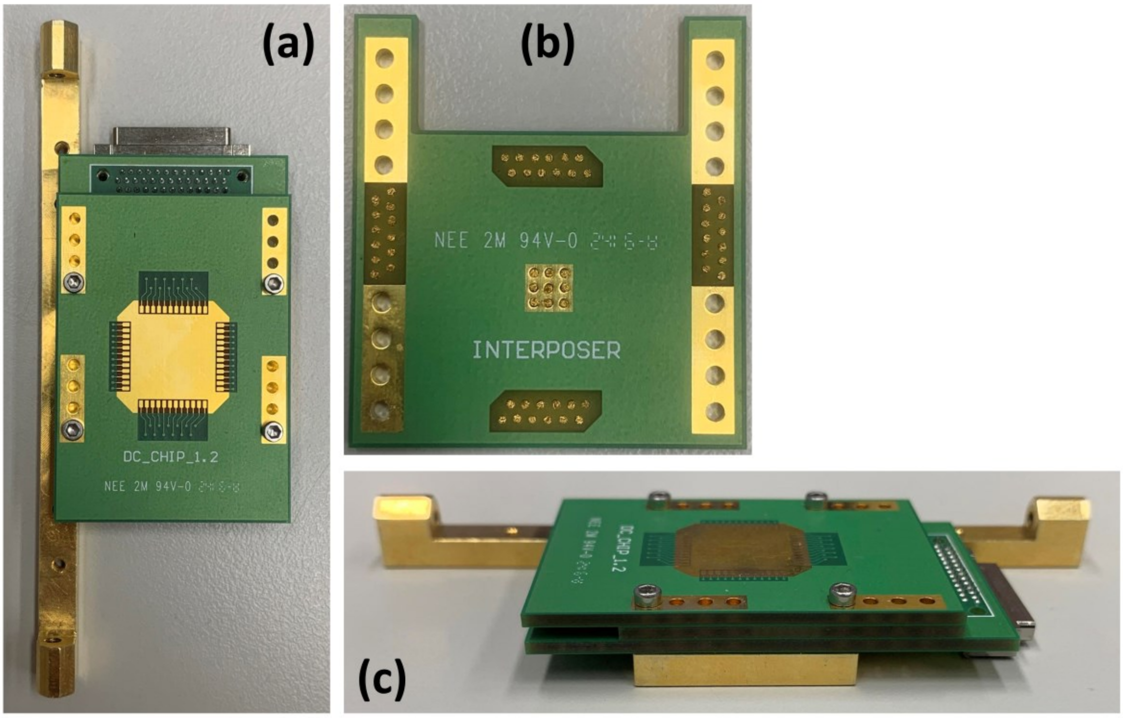


Figure 5.1: Multi-board sample holder after assembling. (b) Interposer filled with the Fuzz Buttons for interconnections.

sides of the boards. This design distributes grounding from the daughterboards, through the interposer, to the motherboard, and finally to the supporting bracket in the sample puck and the entire dilution fridge system. Four sets of screw holes are reserved to allow for board adjustment if mechanical issues arise during assembly. In addition to pure routings to the nano-D connector, another version of the motherboard is also implemented, including footprints for RC low-pass filters along the routing tracks, which might be required for the spin-qubit setup to bypass higher-frequency noise entering the quantum system.

Figure 5.1 shows the multi-board sample holder assembled with the supporting bracket. The interconnection between the motherboard and daughterboard is achieved by filling the 48 holes and 9 ground holes on the interposer board with Fuzz Buttons from Custom Interconnects, as shown in Figure 5.1 (b). These contact pins are compact and durable at low temperatures. Although we use them here for dc routing, they are claimed to be feasible for applications up to the Ka band. In this setup, Figure 5.1 illustrates the

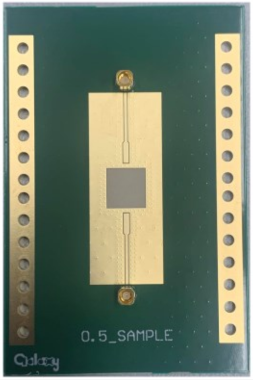
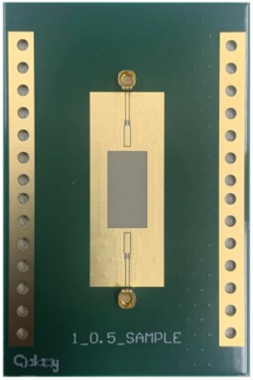
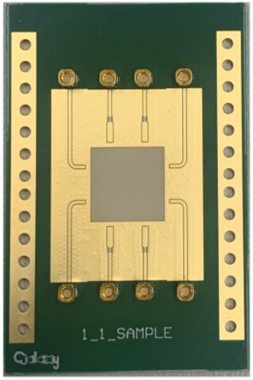
0.5_sample	**1_0.5_sample**	**1_1_sample**
		

Table 5.2: List of the second-phase sample holder boards for superconducting device measurements.

assembly of a daughterboard designed for pure dc and low-frequency measurements, featuring a 1.3 cm mounting space for the sample and 48 dc bonding pads. This separable design allows for easy replacing sample along with its own daughterboard, avoiding the need for another expensive nano-D connector if built within a single board.

5.2.2 Sample Holder Design for Superconducting Devices

In addition to *S*-parameter calibration experiments, the second-phase testing board also incorporates sample holders designed for measuring superconducting devices. Systems for superconducting qubits require high-frequency microwave pumping signals and reflectometry readout. Similarly, other related studies involving superconducting resonators, Josephson junctions, RF-SQUIDs, and Josephson parametric amplifiers also rely on high-frequency microwave characterizations. Hence, setting up the measurement environment is necessary to facilitate conducting experiments for these studies.

In the first phase of the testing board experiment, high-frequency routings were designed using semi-coaxial-like CBCPW structures in Sec. 4.2.3 and later verified at both room temperature and cryogenic temperatures in the previous chapter. This microwave routing design, including the interconnecting structure with on-board connectors, has been carried over into the second-phase design. Table 5.2 presents three sample holder boards designed for measuring superconducting devices. The laminate stacking and the use of SMPS connectors remain consistent with those in the first-phase testing boards. These sample holders are designed with three different mounting sizes to accommodate various devices, with multiple screw holes on both sides of the boards for adjusting and addressing mechanical assembly issues.

In Sec. 4.2.4, we addressed issues concerning bond wires at the interconnecting section from on-board signal tracks to the on-chip routings of the DUTs. Specifically, we proposed a multi-section transformer impedance matching approach to mitigate the induced inductance matching problem. However, another unresolved issue involves resonances facilitated by the on-chip ground plane and sample holder ground plane in wire bonding scenarios. These box-mode resonances, often present within sample holders, can couple to the DUT, potentially leading to undesired loss or dephasing mechanisms in quantum devices. This can adversely affect the parameters under test or reduce qubit fidelities.

To prevent box-mode resonances within the desired operating band, we conducted comprehensive electromagnetic (EM) simulations of the sample holder structure. While HFSS includes eigen-mode analysis, our semi-coaxial-like CBCPW structure, exposing half of the field in the upper-half space of the board, posed challenges with its requirement for a closed metalized boundary in simulations. Although we initially considered using the sample puck as an outer boundary for eigen-mode analysis, this approach generated an excessive number of modes within the complex structure, rendering it impractical for our analysis and validation needs. Instead, we opted for full EM modal network analysis. This method allowed us to design the multi-section transformer matching structure and identify box-mode resonances based on *S*-parameter responses and field distributions at specific frequency points.

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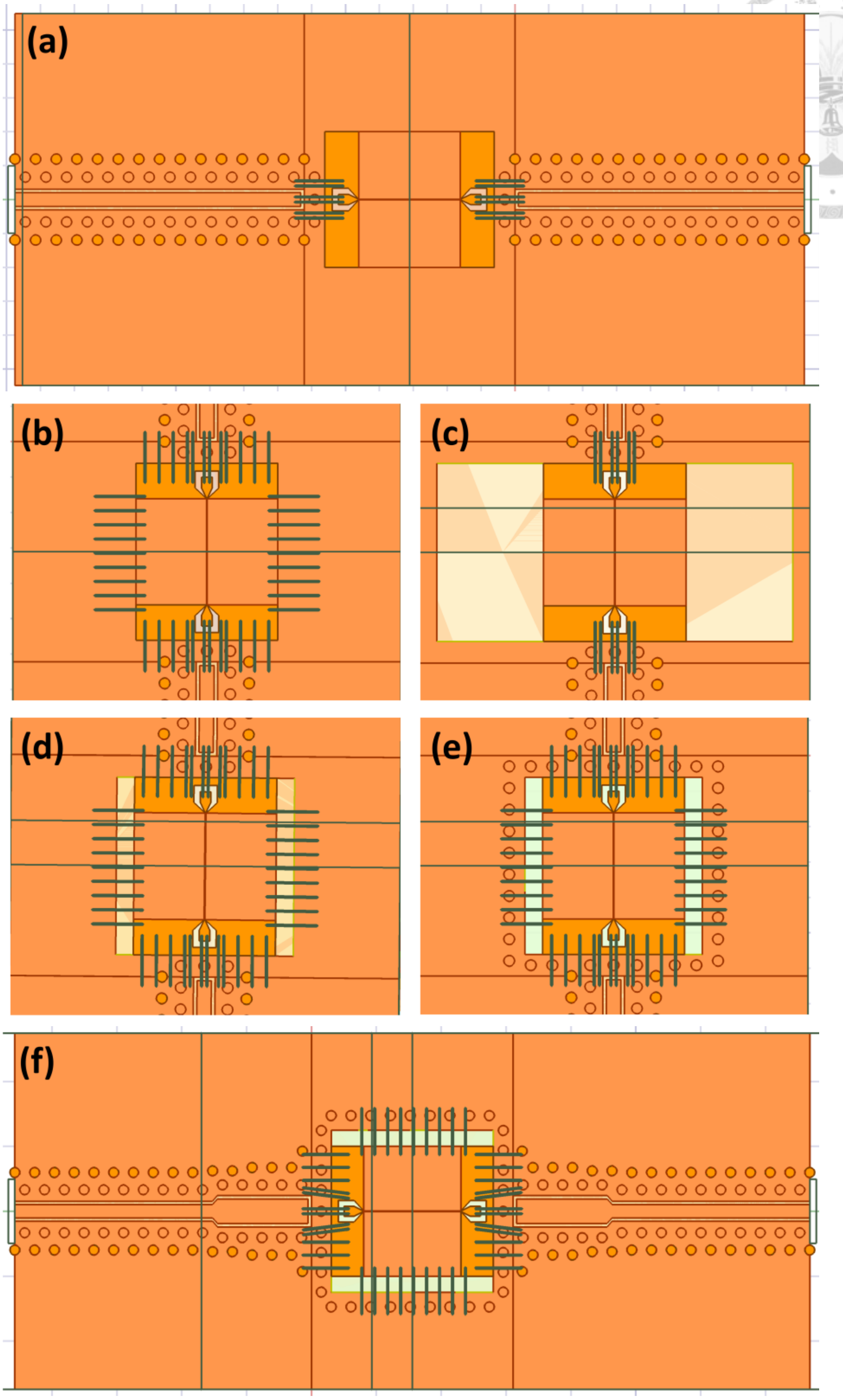

Figure 5.2: Different configurations for the 0.5_sample board EM simulations.

As an example, Figure 5.2 shows various configuration trials during the 0.5_sample board design simulations. In (a), a PEC CPW line on a silicon substrate is introduced as the DUT, placed directly above a complete ground plane on Layer 1 of the sample holder

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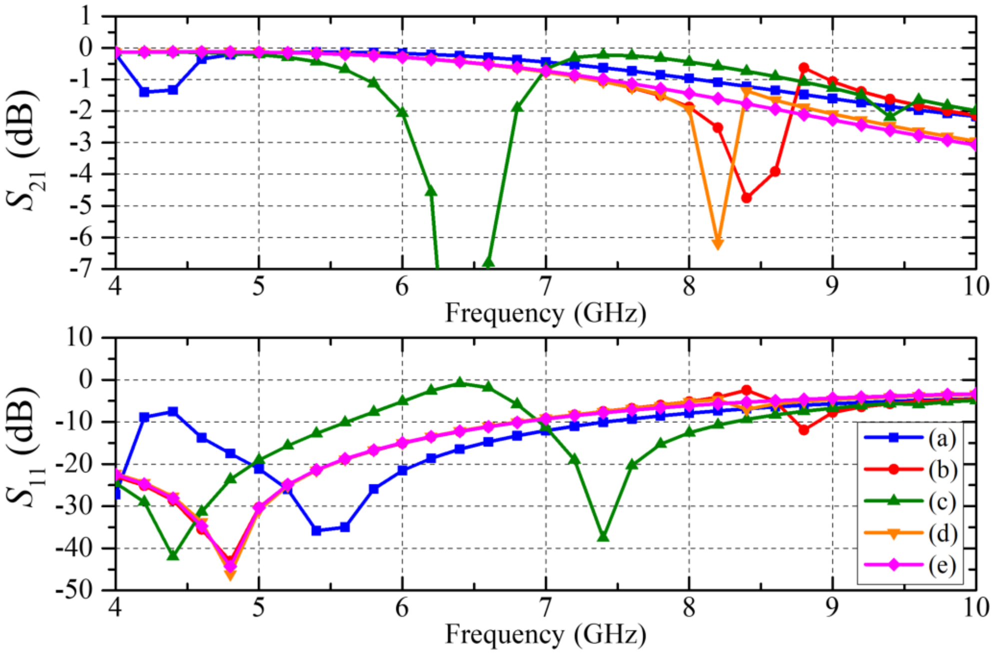

Figure 5.3: Simulated responses of different configurations for the 0.5_sample board.

board, with only the RF tracks wire bonded. Figure 5.2 (b) to (e) present zoomed-in modifications of these configurations. In (b), surrounding bond wires are added around the DUT chip, grounding the on-chip ground plane to the board. In (c), without adding additional bond wires, the ground plane on Layer 1 of the sample holder board directly beneath the DUT chip is removed. (d) is a modification of (b), where, in addition to the surrounding grounding bond wires, the Layer 1 ground plane under the DUT is also removed.

Figure 5.3 depicts the simulation results for the corresponding configurations in Figure 5.2. The dips in transmission responses and the associated fluctuations in return loss indicate box mode resonances affecting the original response of the pure on-board CBCPW and on-chip CPW transmission lines. As illustrated in Figure 5.3, from case (a) to (d), undesired box mode resonances appear in the 4 to 10 GHz band. The resonant conditions in (a) and (b) differ only by the boundary condition of open versus short, with the grounding bond wire in (b) slightly decreasing the effective wavelength of the mode. When the Layer 1 metal is removed in configurations (c) and (d), the box mode resonance

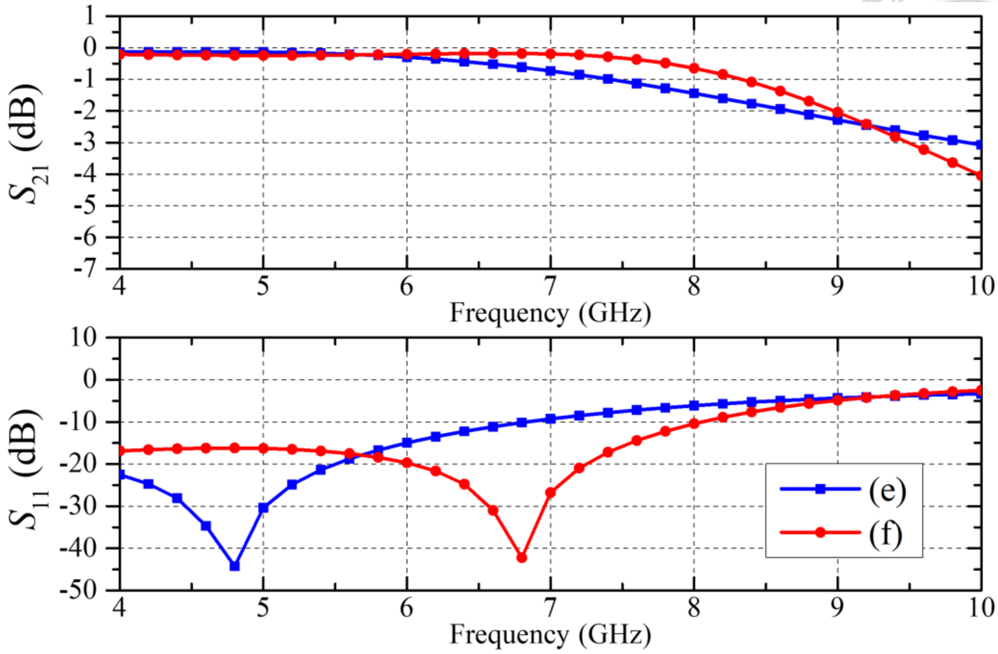

Figure 5.4: Simulated responses of the 0.5_sample board with and without impedance matching network.

field spreads within the RO3003 laminate. Although the resonance space increases, the dielectric constant of RO3003 is smaller than that of the silicon substrate, which still causes the box mode resonance to remain within the operational band. As a conceptual verification, configuration (e) removes all metals from Layer 1 to Layer 4 directly beneath the DUT and places grounding vias around the mounting area to enclose the potential resonance area. The resulting responses of (e) in Figure 5.3 exhibit ideal results, with no box mode resonance observed in the desired band. However, without any backside ground plane, the box mode beneath the DUT may be affected by the available space within the sample puck, potentially influencing the corresponding box mode resonance. In Figure 5.2 (f), it is later verified that adding back the Layer 4 metal does not create on-board box mode resonances within the operational bandwidth. Additionally, an elaborated impedance matching section is designed to mitigate the bond wire effect. Figure 5.4 illustrates the corresponding cases of (e) and (f) in Figure 5.2, demonstrating that the impedance matching section successfully extends the return loss below 10 dB up to 8 GHz. Both the 1_0.5_sample board and the 1_1_sample board are designed with identical

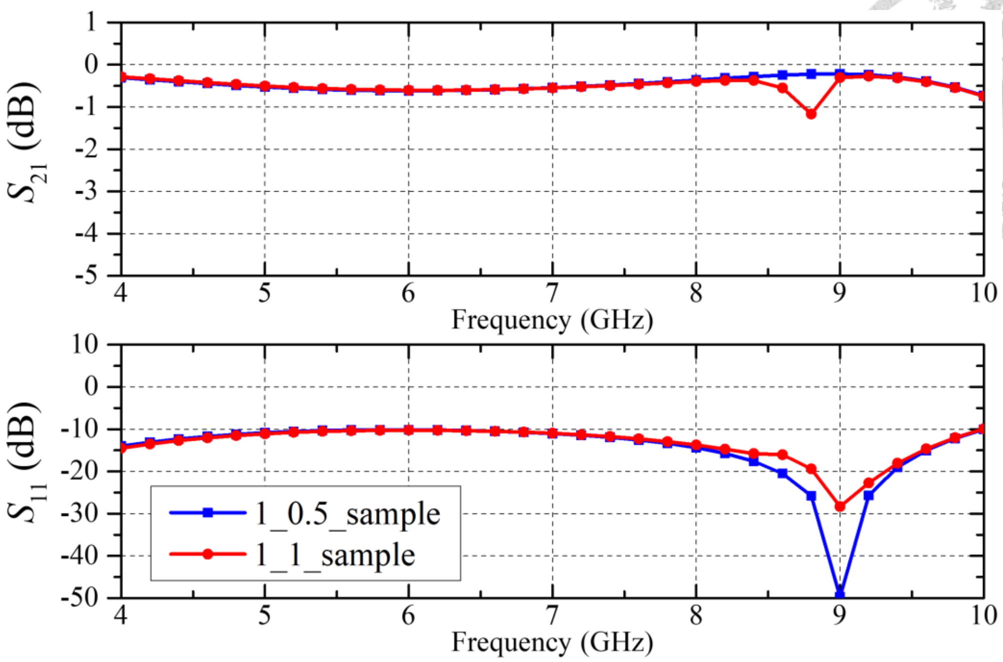

Figure 5.5: Simulated responses of the 1_0.5_sample board and the 1_1_sample board.

layer configurations and a similar multi-section transformer approach. According to the simulation results in Figure 5.5, both boards exhibit good transmission and return loss responses within the 4 to 8 GHz range when a PEC CPW transmission line chip is used as the DUT. While a slight box mode resonance is observed at 8.8 GHz in the 1_1_sample case, its impact on our experiments is considered minimal due to the frequency bandwidth limitation of the HEMT LNA in our superconducting device measurement setup, which extends only up to 8 GHz.

Due to the extreme sensitivity of superconducting devices to magnetic flux fluctuations, experiments often involve shielding the sample with various metals to reduce environmental noise effects. Mu-metal, a nickel-iron ferromagnetic alloy with high permeability, is typically chosen because it can confine magnetic flux within the material without allowing it to penetrate and affect the device under test. However, Mu-metal's permeability can degrade and it can saturate at cryogenic temperatures, making Cryoperm, a cryogenic-specific magnetic shielding material, a preferable alternative. To

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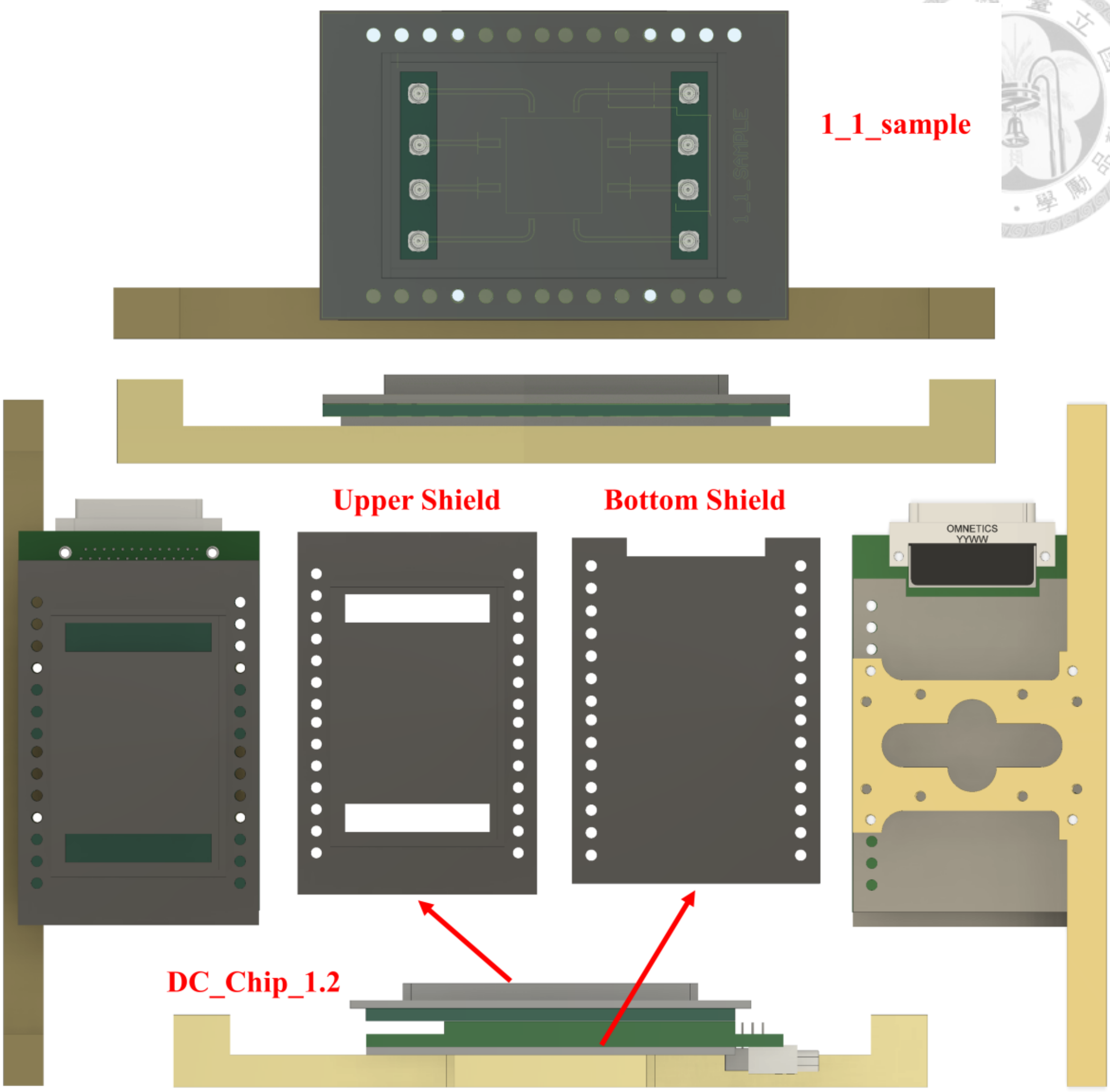

Figure 5.6: Second-layer magnetic shielding design.

ensure effective protection, a two-layer shielding approach is proposed. The first layer mimics the cylindrical shape of the sample puck and covers the entire sample holder directly beneath the copper metal sample puck. The second layer of protection is designed on the sample holder board itself and is assembled using same screws and supporting brackets.

Figure 5.6 the assembly configurations of the second-layer magnetic shielding with the 1_1_sample board and the multiple dc board structure. Due to the high cost associated with these high-permeability metals, the shielding is designed to accommodate various

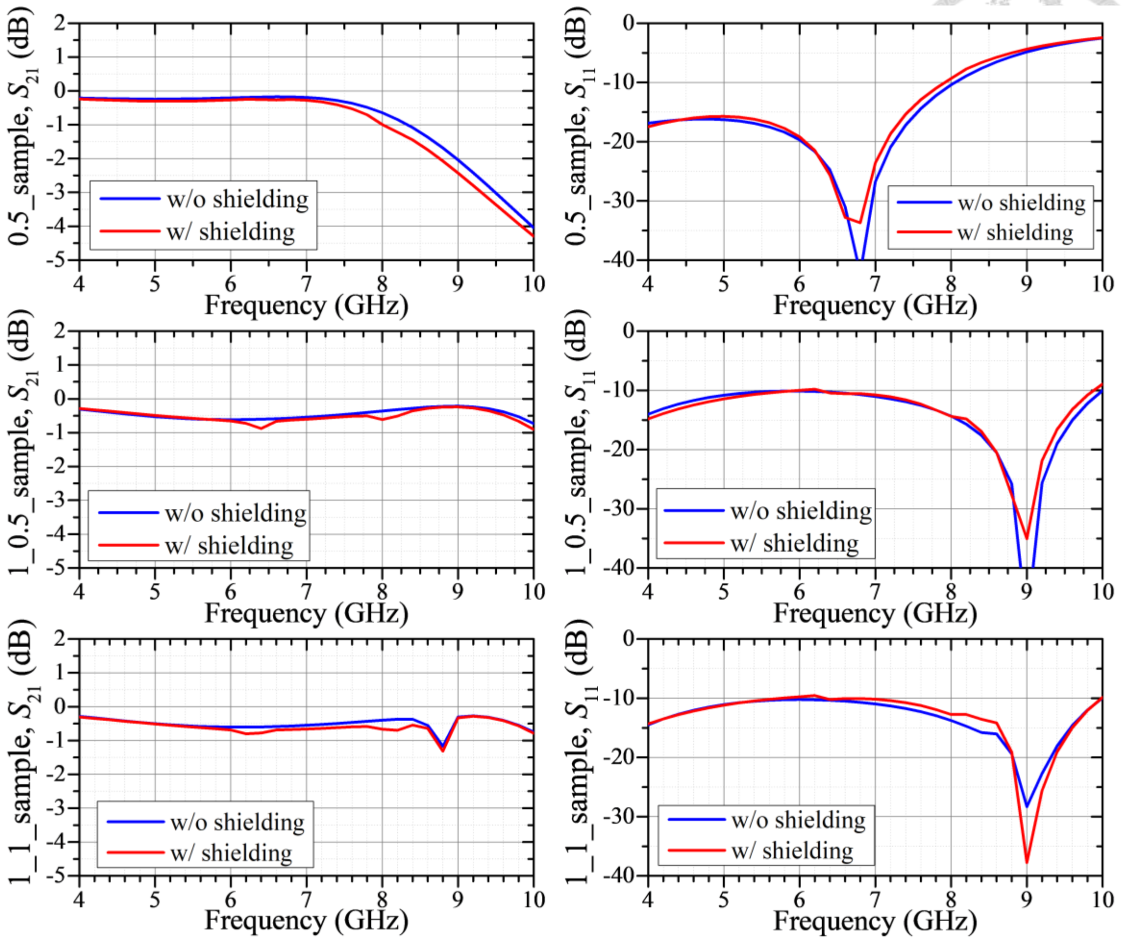

Figure 5.7: Simulated responses of three different sample holders, with and without the second-layer upper magnetic shielding.

configurations and scenarios. This second-layer magnetic shielding consists of two main parts: The bottom shield is a flat sheet with screw holes for adjustments and a concave space for the nano-D connector. The upper shield is shaped like a half-box to accommodate the on-board CBCPW transmission lines, which require upper air spaces for propagation. Its height matches that of the SMPS connector to allow space for cable connection. Additionally, two rectangular openings are included to facilitate the connection of SMPS connectors across different types of sample holder boards designed in this subsection. Overall, the second-layer shielding provides coverage for the sample holder boards from both the top and bottom sides. Any potential leakage from the side edges is addressed by the cylindrical shielding of the first layer beneath the sample puck.

From a microwave design perspective, the inclusion of magnetic shielding requires a careful analysis of potential box mode resonances. Therefore, the sample holders, along with the upper magnetic shielding, are simulated using modal analysis, assuming the high-permeability metal behaves as a PEC. Figure 5.7 compares simulation results for each of the three types of sample holders, both with and without upper magnetic shielding. The 0.5_sample board exhibits no box mode resonance within the desired band, even with the shielding. However, slight resonances are observed in the other two board around 6.2 GHz and 8.2 GHz. Additionally, the 1_1_sample board shows its original bottom box mode resonance at 8.8 GHz. Unfortunately, efforts to mitigate these box mode resonances have shown limited effectiveness. Therefore, the simulation results highlight potential frequency points affected when using magnetic shielding during measurements. It's important to note that the slight variations in results observed with and without magnetic shielding for both the 0.5_sample board and the 1_1_sample board, besides the box mode resonances, are primarily attributed to different DUT metal thickness settings during simulation. This adjustment is necessary to prevent mesh formation failures due to significant dimensional differences compared to the entire structure.

5.2.3 Calibration Scheme Proposal

Despite the gradual standardization of commercially available 4 K probers, microwave calibration and de-embedding remain challenging within a dilution refrigerator at base temperatures of tens of mK. These challenges pose significant obstacles to accurately probing the responses of DUTs. Since most active semiconductor electronics are designed to operate at 4 K, where a larger cooling power budget is feasible for control and readout operations, the proposed calibration scheme in this chapter mainly targets other devices that operate at mK temperatures, such as superconducting devices. These quantum-related devices require ultra-low temperature environments to minimize noise fluctuations and are typically probed with ultra-low power signals below -100 dBm.

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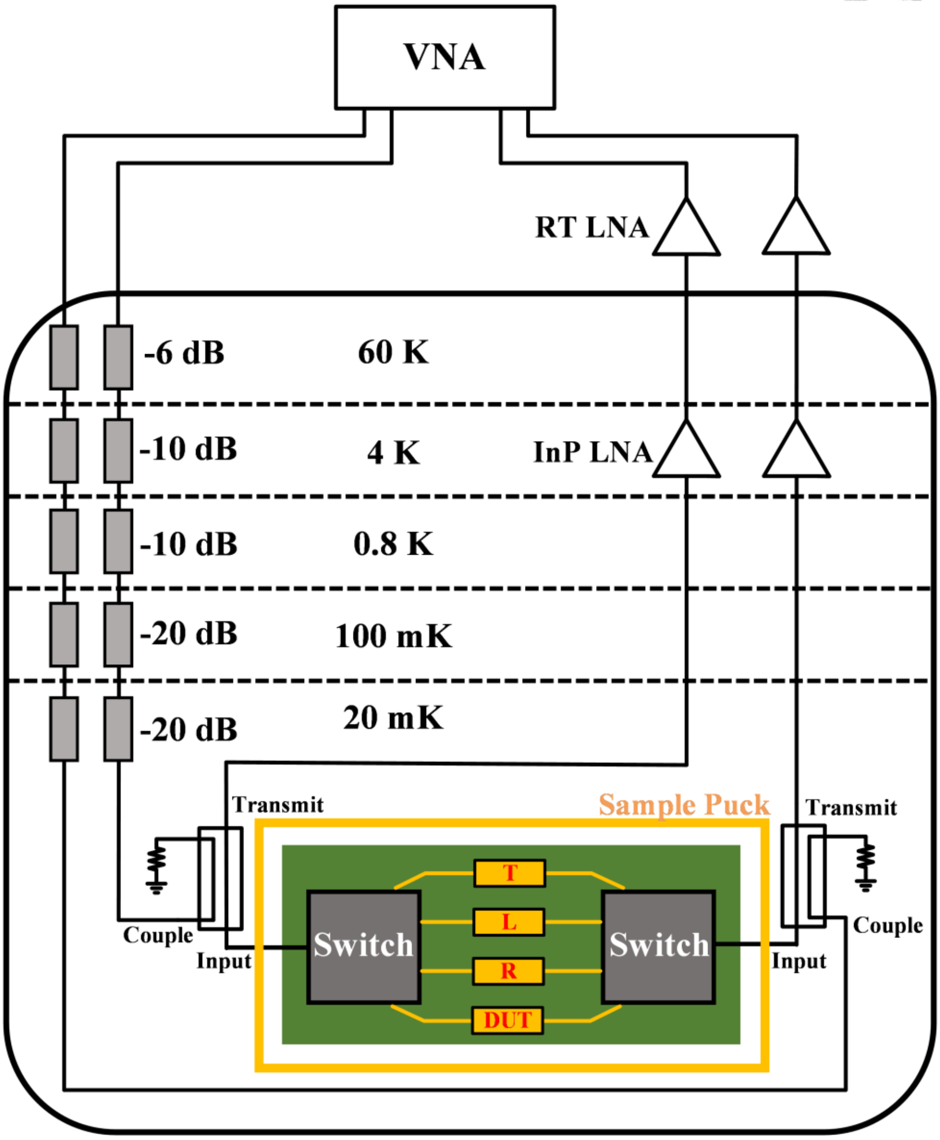

Figure 5.8: Schematic diagram of the setup for the proposed calibration scheme within the dilution fridge.

This often presents challenges in calibration procedures, as demonstrated in Chapter 4. The need for sufficient attenuators to reduce the input signal also reduces the reflected signal due to the large round-trip loss, often to a level lower than the reflection response at the upper stages. As a consequence, this leads to an unchanged return loss across all standards, ultimately resulting in calibration failure. In [97-100], a clever architecture is proposed to address this challenge, which we have adopted in our proposal and illustrated in Figure 5.8. Instead of measuring the reflected signal through the same heavily attenuated input cable path, the architecture incorporates two directional couplers at the base temperature stage. Placing these directional couplers closer to the DUT enhances the sensitivity of the VNA system. This setup allows separate measurement of reflection and transmission using distinct input and output cable paths, thereby amplifying the output signals. The port configuration of the directional couplers isolates the output from the input cable path, while also reducing the input signal level at the DUTs due to the coupling coefficient from the coupled port to the input port. To compensate for the substantial attenuations along the input path, two low-noise amplifiers are placed at the output to enhance the signal level for VNA measurements. For quantum-related or superconducting devices, various filters and isolators may be necessary along the input and output paths to mitigate kick-back noise from the output sensing electronics, as well as other sources of microwave and infrared noise.

Despite capturing the true reflected signals from DUTs, calibration schemes often involve various sources of error, as discussed in Chapter 4 and in literature reports. The primary challenge in calibration procedures is maintaining consistency across the error boxes in front of the corresponding standards and DUTs. This encompasses every electrical path within the system, including cables, connectors, and other electronics. In the straightforward calibration scheme outlined in Chapter 4, significant variations across each cable path from room temperature to the base temperature stage lead to considerable error fluctuations and uncertainties in the calibrated results. In the setup described in [97-100], two commercially available electromechanical latching switches are introduced at the base temperature stage. This configuration limits potential error sources solely to differences in routing from switch ports to DUTs, thereby circumventing the complexities and challenges associated with the complex and challenging-to-control dilution refrigerator system behind the switches.

Instead of employing bulky electromagnetic latching switches, the architecture

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proposed in Figure 5.8 incorporates semiconductor integrated circuit RF switches for transitioning between various standards and DUTs. This approach offers several advantages. Firstly, by implementing RF multiplexing with IC chips, it enables on-board integration, eliminating the need for multiple cables and fixtures connecting switches to standards and DUTs. This significantly reduces the volume required by the bulky electromechanical latching switches and ensures a consistent path to the input port of the on-board IC switches, thereby mitigating discrepancies across different cables and connectors associated with electromechanical latching switches. Secondly, the on-board configuration inherently allows for shifting the calibration reference plane to the edge of the DUT chips, offering advantages over a connectorized calibration scheme by facilitating the de-embedding of on-board routings. Additional refinement can be achieved with on-chip calibration standards, further advancing the reference planes and de-embedding the responses of bond wires. Finally, the on-board configuration enables integrating the calibration system within a sample puck, thereby reducing the need for cooling and warming cycles when changing samples.

With the proposed architecture, the remaining potential sources of calibration errors are primarily variations across the ports of IC switches, differences in bond wire lengths, and discrepancies between various on-board routings. Electrical paths within PCB on-board routings are generally easier to control compared to coaxial cables and connectors. While bond wire lengths can be carefully managed by experienced manufacturers, adopting flip-chip packaging for IC switches could further mitigate this issue. The variations in responses across different ports of IC switches thus predominantly influence calibration discrepancies, necessitating careful selection of commercially available switches or meticulous custom design.

Table 5.3 presents the testing boards designed for validating the proposed calibration

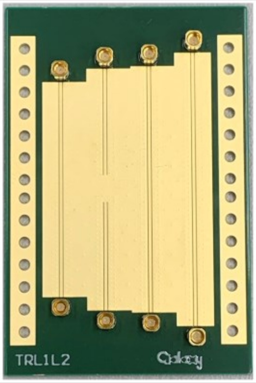
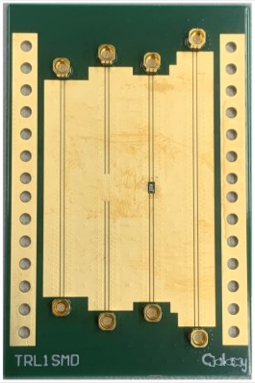
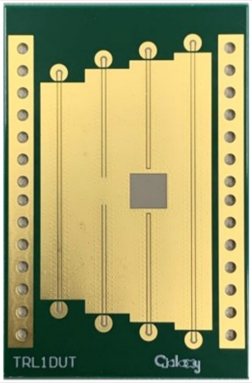
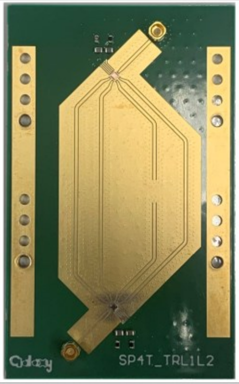
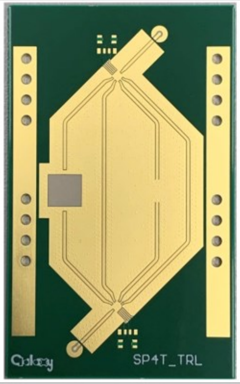
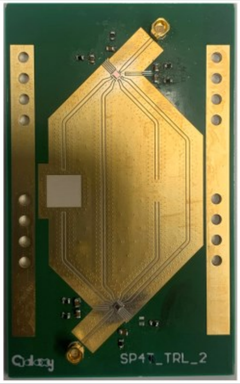
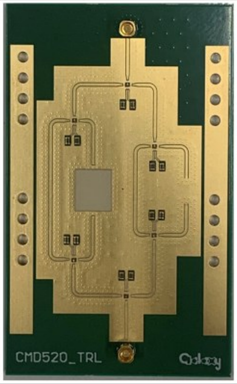
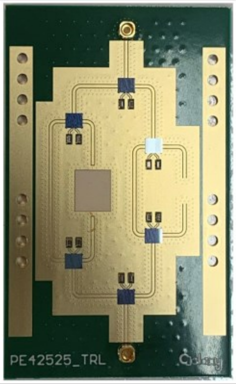
TRL1L2	**TRL1SMD**	**TRL1DUT**
 	 	
SP4T_TRL1L2	**SP4T_TRL1SMD**	**SP4T_TRL**
 	 	
SP4T_TRL_2	**CMD230_TRL**	**PE42525_TRL**
 	 	

Table 5.3: List of second-phase testing boards for *S*-parameter calibrations.

scheme. The proposed architecture is implemented in SP4T boards, where two custom SP4T RF switches, detailed in Chapter 3, are integrated within the calibration board system. Among the SP4T boards, the SP4T_TRL and SP4T_TRL_2 boards provide designated space for mounting DUTs to facilitate device measurements, with the only difference being the available dc pads for the custom RF switches. Additionally, the

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SP4T_TRL1L2 board replace the mounting space with an additional Line standard (L2), serving both as a Line standard and as an initial-phase DUT, as discussed in Chapter 4. Conversely, the SP4T_TRL1SMD board focuses on a Surface-Mounted Device (SMD) as the DUT, particularly examining its cryogenic high-frequency responses within the systems. To compare to the previous straightforward calibration scheme, three corresponding boards with eight separate SMPS connectors are also implemented.

In addition to the custom IC switches, two commercially available broadband switches are integrated into the calibration system. Due to the limited cooling power budget at the base temperature stage of the dilution fridge, to the author's knowledge, only these two SPDT switches, and no other commercially available SP4T switches, are capable of operating without excessive power leakage. The two chips have different packaging configurations: the CMD230 from Qorvo is a bare die requiring bond-wiring, while the PE42525 from pSemi is flip-chip packaged. Although the board routings differ from the SP4T boards that use custom switches, due to the limited ports per chip, the standards are designed identically. Finally, all the calibration boards requiring dc supply voltages are integrated with the multi-board system described in Sec. 5.2.1, serving as daughterboards.

5.3 Room Temperature Validation Results

As an initial validation, the testing boards are examined within the sample puck solely at room temperature, without other electronics shown in Figure 5.8. After performing a standardized ECal on the VNA, the measurement reference plane is set at the SMP connectors on the fixtures of the sample puck for subsequent measurements. Figure 5.9 and Figure 5.10 illustrates the raw data measured with the SP4T_TRL1L2 and SP4T_TRL1SMD boards, respectively. In this second-phase design, the Line standards differ from those in Chapter 4. L1 covers 1.47 to 11.75 GHz, centering around 6.6 GHz,

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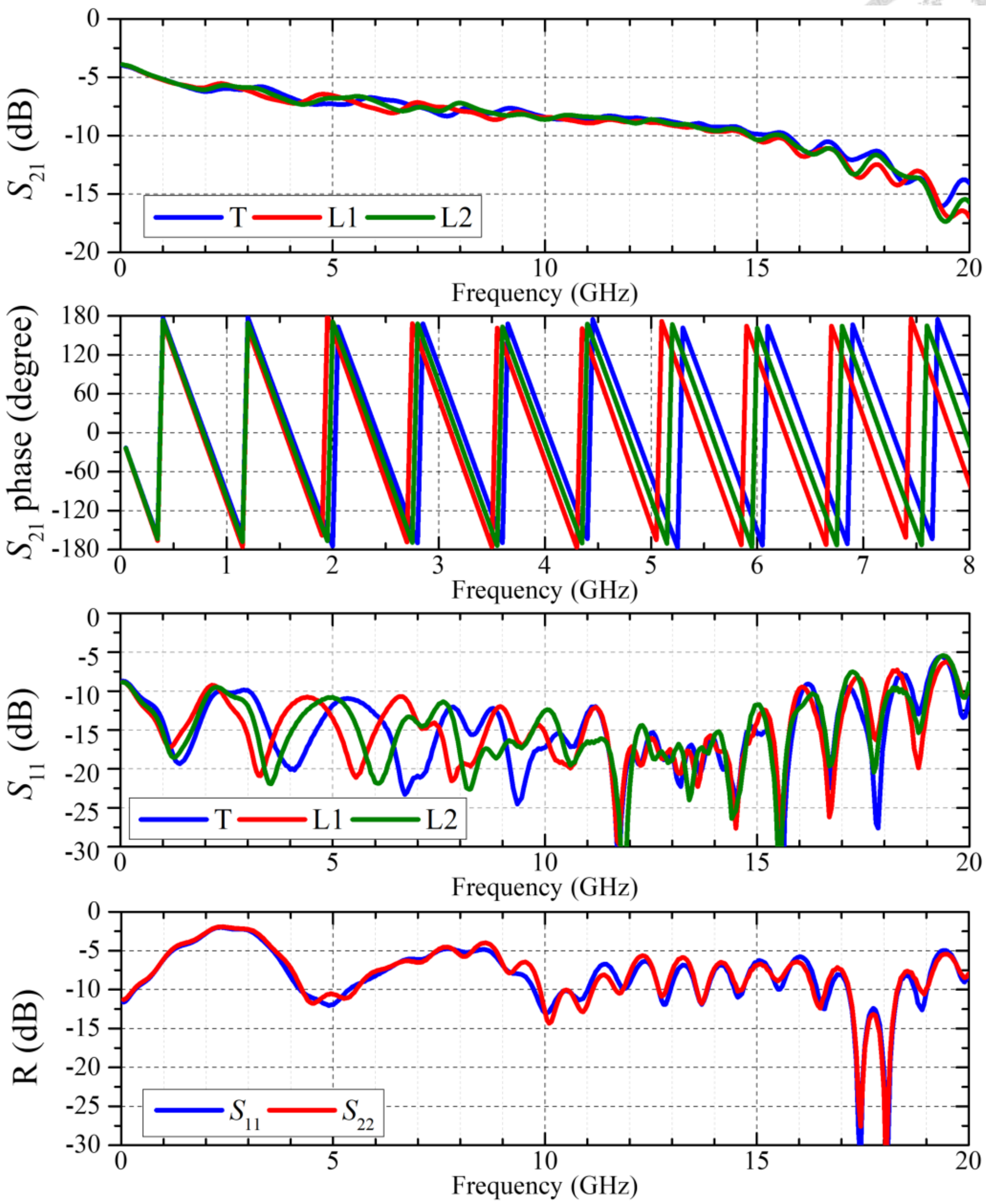

Figure 5.9: Measured responses of the SP4T_TRL1L2 board.

targeting the band of superconducting device measurements. L2 spans from 2.73 to 21.8 GHz, extending to the VNA's available bandwidth limits. Figure 5.9 clearly shows the phase relationships between the different Lines and Thru, with L1 having the longest electrical length. The transmission magnitude relationship is less clear, likely due to multi-reflections, as evidenced by the observed ripples related to the electrical length. The return loss results indicate that the bond wire starts to impact the responses around 15 GHz, which also affects the transmission responses.

The measured responses of the SP4T_TRL1SMD board in Figure 5.10 largely

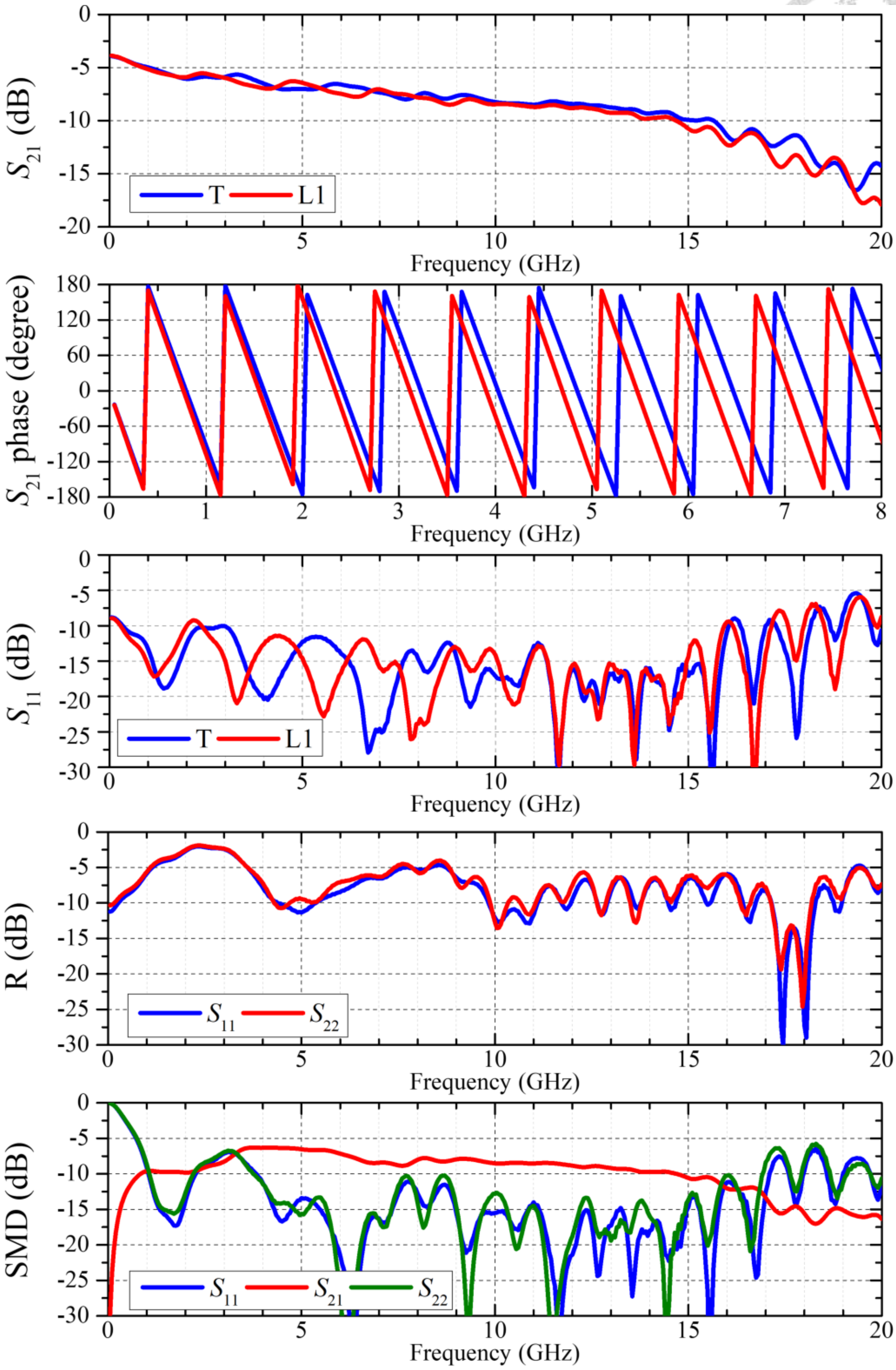

Figure 5.10: Measured responses of the SP4T_TRL1SMD board.

coincide with those in Figure 5.10, demonstrating the robustness of the proposed calibration scheme when the board systems are carefully assembled. A 1 pF SMD ceramic C0G capacitor from Murata is attached to the SP4T_TRL1SMD board as the DUT.

Figure 5.11shows the measured responses of the CMD230_TRL board. The leakage

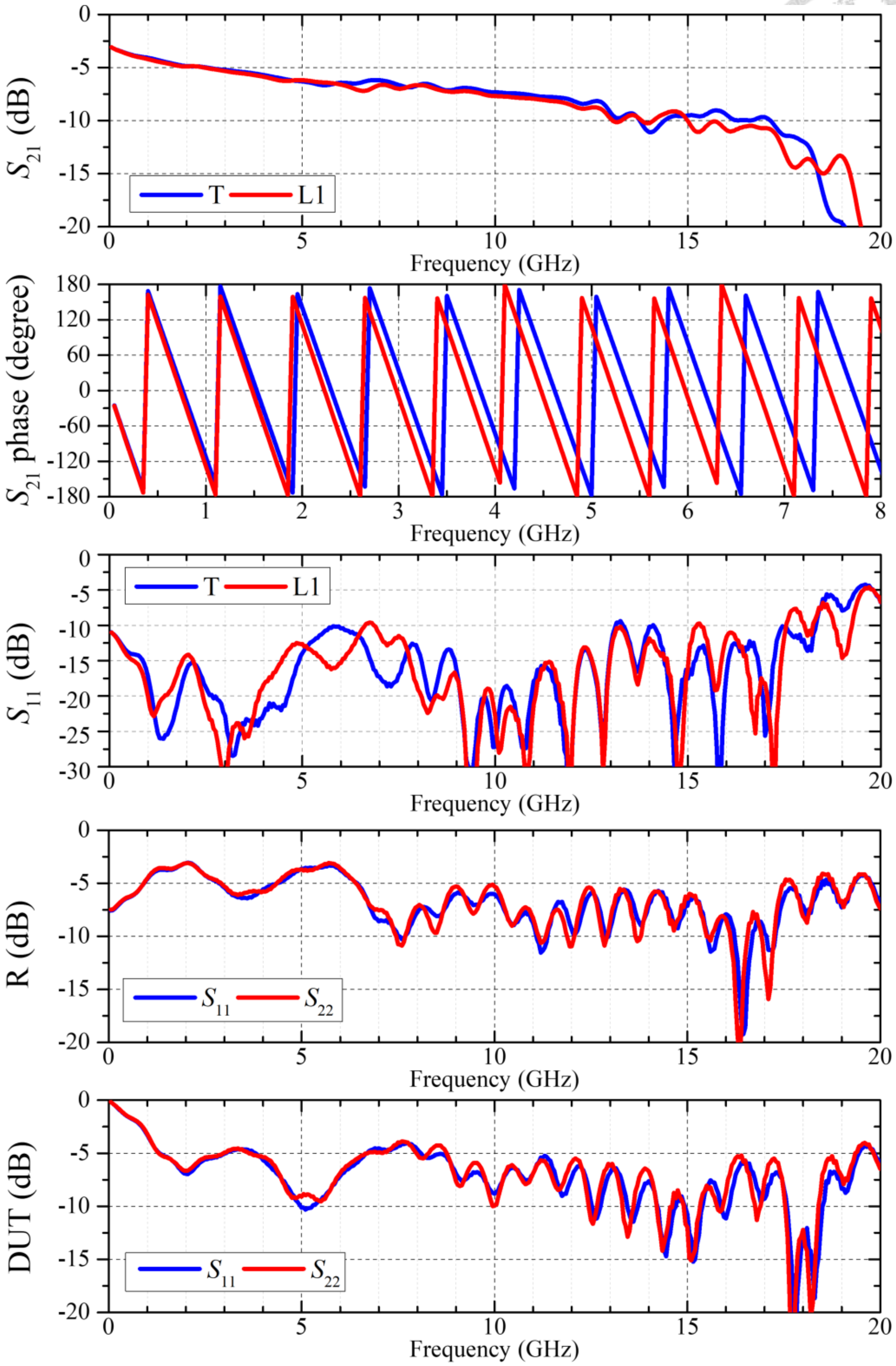

Figure 5.11: Measured responses of the CMD230_TRL board.

power of the SPDT switch IC was measured using a Keysight B2901A SMU, recording only about 1.4 µA per chip, confirming it operates within the power limit of the dilution fridge. Without any device mounted, the DUT responses in Figure 5.11 represent the open-ended stubs of the on-board routings to the bond-wiring pads. Similar to the SP4T

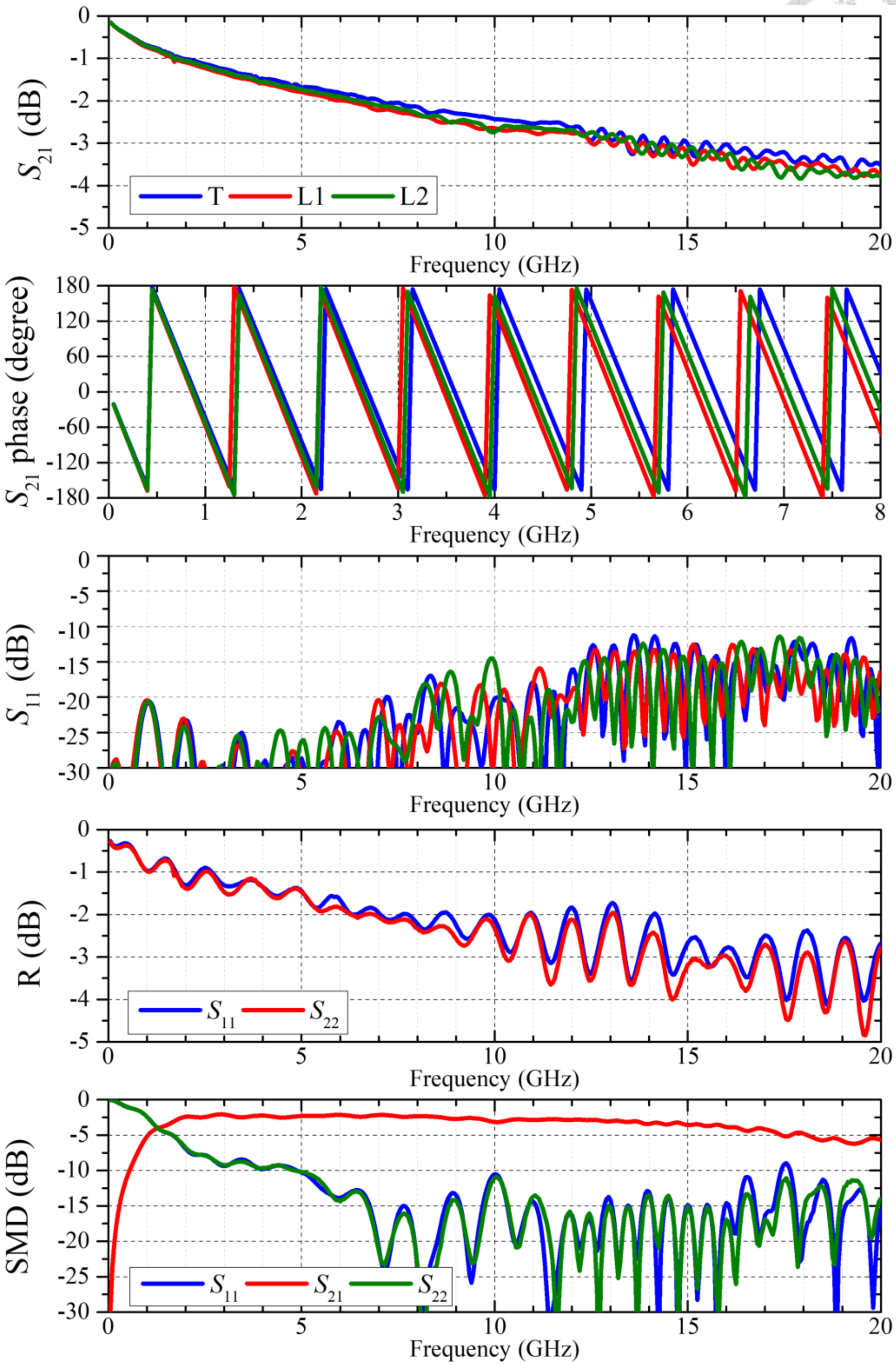

Figure 5.12: Measured responses of the TRL1L2 and TRL1SMD boards with eight different cables within the sample puck.

boards, the bond wires required for the CMD230_TRL board integration affect the transmission response when approaching 20 GHz. The flip-chip trial of the PE42525_TRL board encountered some difficulties during integration; therefore, the

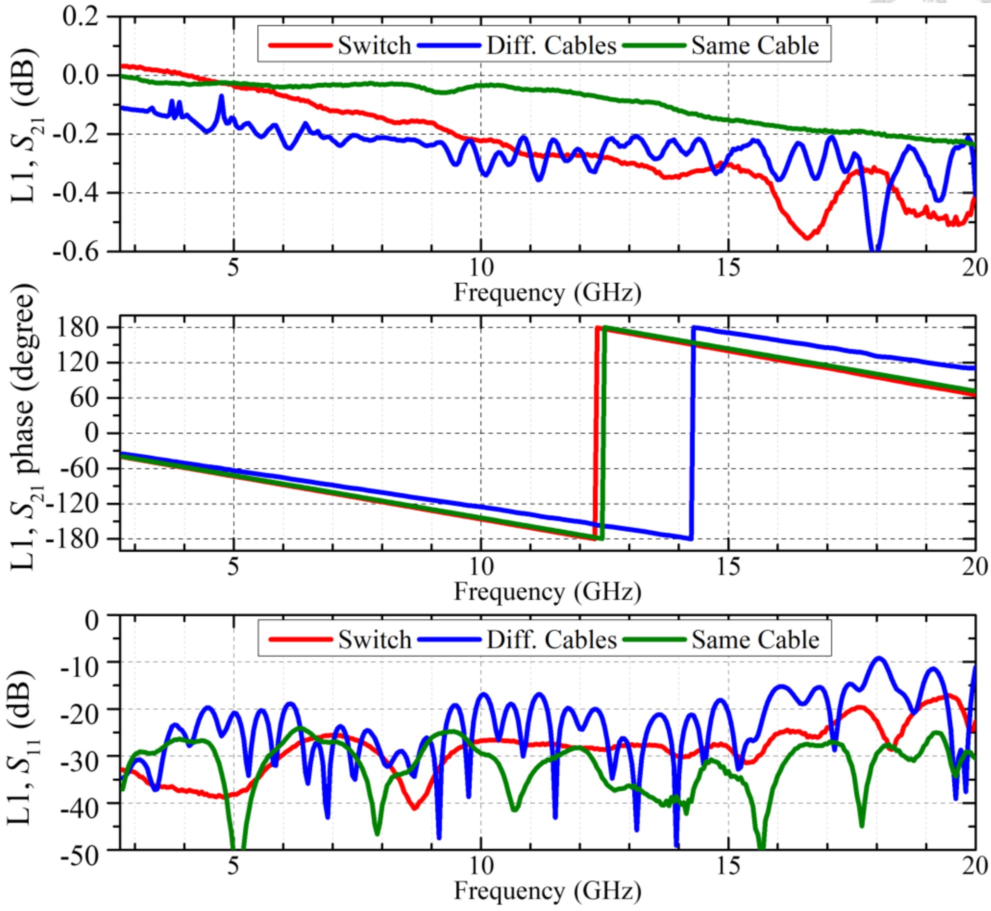

Figure 5.13: Comparison of calibrated responses with L1 as the DUT and L2 as the Line standard under different setup configurations.

measurement results are not shown here. As a reference, Figure 5.12 displays the measured raw data responses of the TRL1L2 and TRL1SMD boards, similar to those in Chapter 4, where the SMD measures the same 1 pF ceramic capacitor as the DUT.

After acquiring all the raw data, the measured responses were post-analyzed using the earliest and basic TRL algorithm introduced in [90]. Since the proposed calibration scheme utilizes only one Line standard, the discontinuity problem for multi-line standards and the corresponding weighted algorithm were not explored. Figure 5.13 illustrates the calibrated results when using L1 as the DUT and L2 as the Line standard. A third measurement configuration, labeled “Same Cable,” is introduced as a reference. This setup involves measuring the testing boards solely using two identical blue cables throughout every standard and DUT, without passing through the SMP connectors on the fixtures and into the sample puck. This method, also detailed in Chapter 4, has been shown to mitigate ripples compared to measurements using eight different blue cables with their corresponding standards and DUTs within the sample puck. Ideally, this setup reduces noise sources to on-board connector adhesion discrepancies and minor potential on-board routing variations for the TRL1L2 and TRL1SMD boards. However, in practice, the push-on connection of SMPS connectors is found to be unstable under this freely unstressed measurement setup, unlike when installed within the sample puck. This instability leads to potential measurement errors from each plugging and unplugging cycle, as well as from different cable angles when attached to each standard and DUT. Nonetheless, by carefully attaching the cables to the on-board connectors and performing multiple measurements to ensure repeatability, the selected measured results represent a best effort to minimize possible deviations for the calibration analysis.

Consequently, the calibrated results using the proposed switch IC integration and the straightforward eight-cable setup are compared with the reference same-cable configuration in Figure 5.13. The results using eight cables show the most deviation from the other two configurations. Specifically, they exhibit worse return loss responses after calibration, with transmission responses showing ripples in magnitude and significant phase deviations compared to the other two cases. For the proposed calibration approach, despite some inconsistency in transmission response amplitude compared to the "Same Cable" case, the transmission phase and return loss responses are more consistent. The discrepancies for the proposed method likely stem from two sources. At high frequencies above 15 GHz, the bond wire effect becomes pronounced, increasing deviations across the electrical paths of the routings to each standard and DUT. Another issue arises from potential transmission response differences between each port within the RF switches. This could result from routing imbalances in the switch layout or variations in the supply

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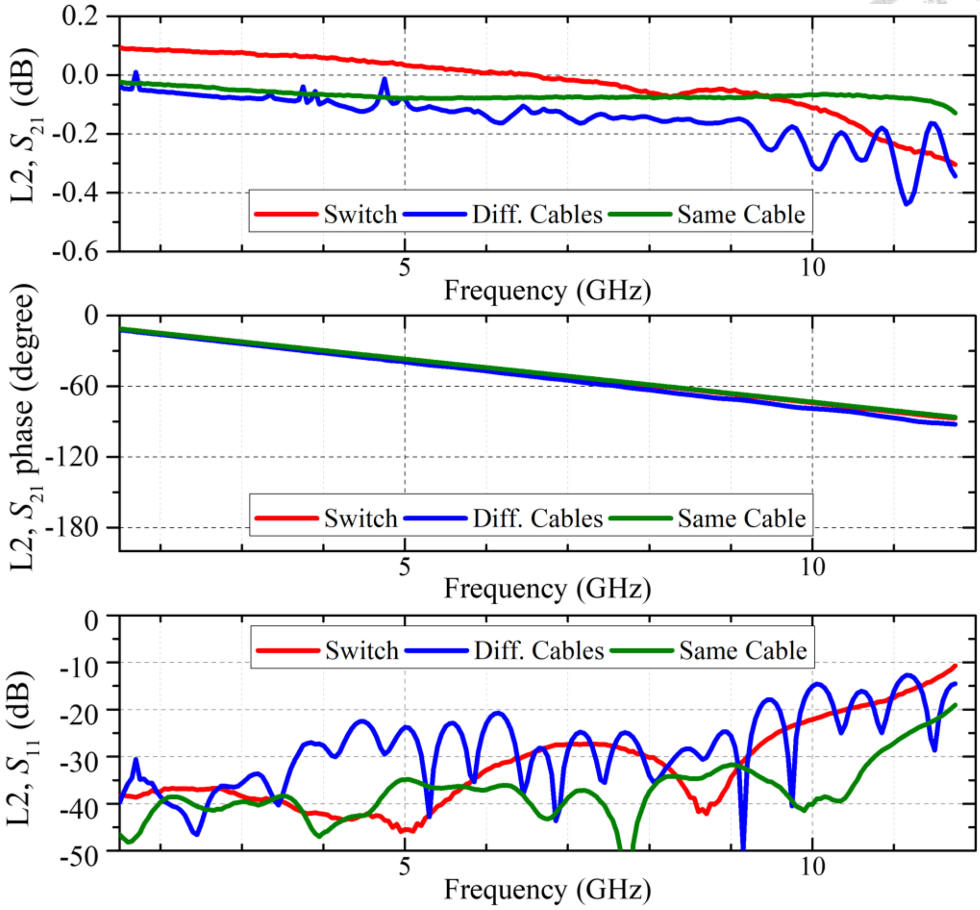

Figure 5.14: Comparison of calibrated responses with L2 as the DUT and L1 as the Line standard under different setup configurations.

voltage at the gate of each switch transistor, influenced by different levels of degradation or fluctuations in power supplies. Upon reviewing the measured data of the custom RF switches in Chapter 3, it was found that there is a maximum magnitude variance of under 0.1 dB across the four output ports. This variance could potentially contribute to the deviations observed in Figure 5.13 compared to the case using identical cables.

Figure 5.14 compares the calibrated results of three configurations, with L2 as the DUT and L1 as the Line standard. Compared to Figure 5.13 and the results in Chapter 4, the calibrated results of the straightforward eight-cable case in Figure 5.14 show fewer ripples and deviations. This can be attributed to the shorter electrical length of L2 compares to that used in Chapter 4 and L1 used in Figure 5.3, which reduces potential deviations. Additionally, unlike the testing boards in Chapter 4 where the SMP connectors

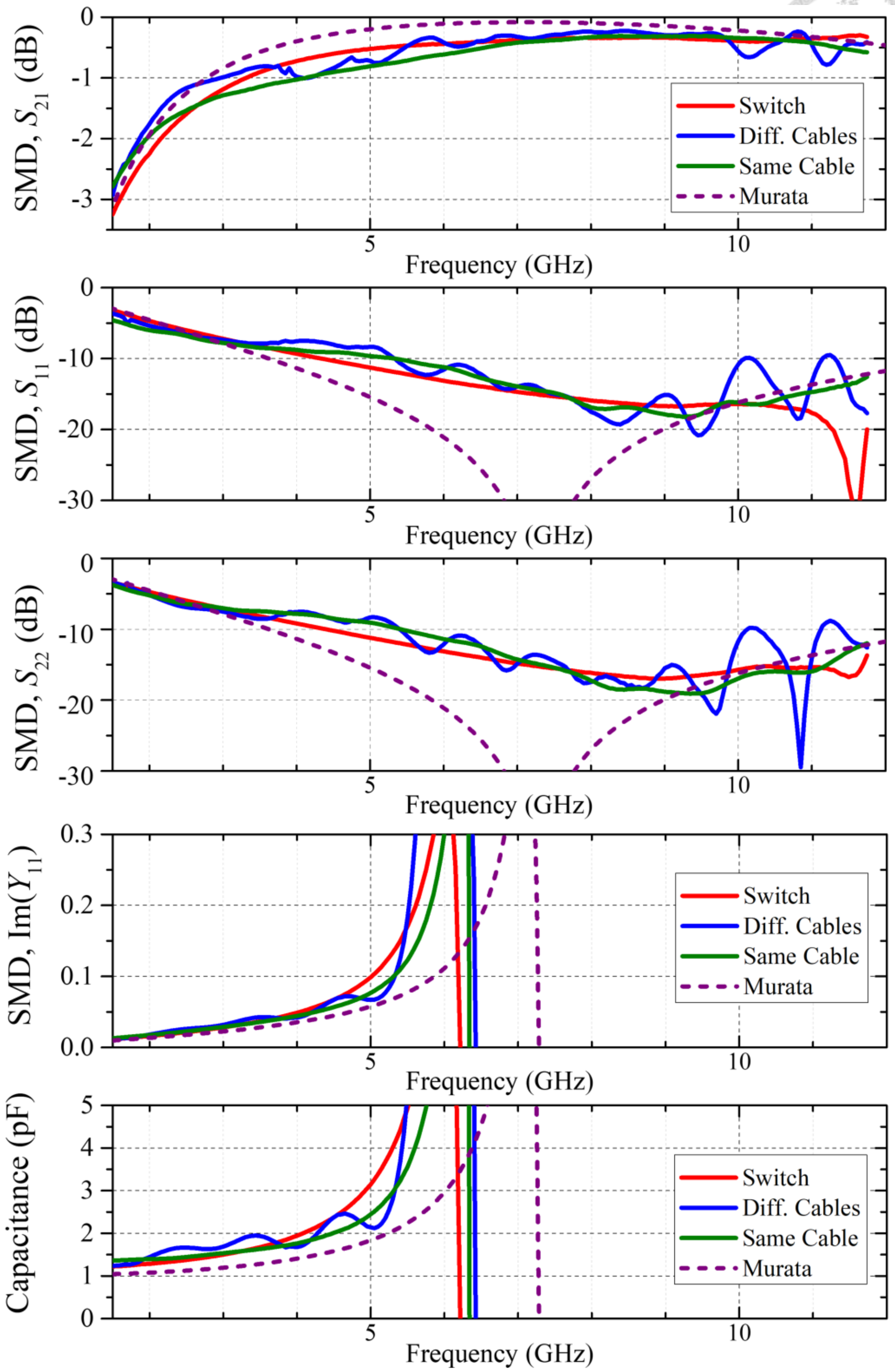

Figure 5.15: Comparison of calibrated responses with a 1 pF SMD ceramic C0G capacitor as the DUT and L1 as the Line standard under different setup configurations.

were soldered in the lab, the boards in the second-phase experiments of this chapter were manufactured with the connectors adhered by an experienced factory. This change further reduces potential sources of error across each standard and DUT. The calibrated results

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of the proposed method exhibit a similar magnitude deviation. At higher frequencies, this may be owing to the phase of the L1 standard approaching 180 degrees, thereby increasing calibration deviation. Nevertheless, the proposed method demonstrates smoother calibrated results and better return loss and phase responses compared to the straightforward eight-cable case.

In addition to interchanging Line standards as DUTs, a 1 pF ceramic C0G capacitor is measured and calibrated using the three methods, with the results depicted in Figure 5.15. The *S*-parameter data from Murata, indicating the capacitor's self-resonance frequency around 7.3 GHz, was also included. The calibrated and referenced *S*-parameters are converted into *Y*-parameters, and the capacitance values are extracted from the imaginary part of Y_{11}, assuming an ideal capacitor measured in series between the two ports. The data provided by the manufacturer differs from all three calibrated responses due to the influence of the board substrate under the SMD capacitor. This substrate effect is not considered in the manufacturer's data but is accounted for after calibration. Each of the three calibration configurations has its own sources of error, as discussed earlier. Generally, the straightforward eight-cable method showed ripples in the measured results, while the “Same Cable” case produced smoother responses. However, the extracted value from the latter serves only as a reference due to potential connector plugging deviations. Our proposed method also yielded smooth calibrated responses, disregarding fluctuations above 11 GHz. The calibrated capacitance value slightly exceeded that of the “Same Cable” case and Murata's provided value. This discrepancy may be attributed to soldering differences of the SMD capacitors on the two boards adhered in the lab, as well as varying responses across switch ports, as mentioned earlier.

To summarize, although there is room for further improvement in accuracy, the proposed calibration scheme shows superior results compared to the straightforward

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eight-cable approach. It's important to note that the calibrated responses above only pertain to scenarios within the sample puck. When integrated into the dilution fridge, additional discrepancies may arise with the straightforward eight-cable configuration due to additional separate electrical paths. In contrast, the proposed approach effectively controls and mitigates error sources outside the sample puck by utilizing identical electrical paths for each standard and DUT.

5.4 Summary

This chapter delves into advancements in sample holder design. A new iteration of the sample holder, featuring a multi-board structure, has been implemented. This design facilitates easy interchangeability of samples, each equipped with its own daughterboard facilitated by an interposer. This configuration effectively isolates high-frequency signals to within the daughterboard. Furthermore, unified dc pad configurations enable customization of daughterboards with specific functionalities tailored to their respective scenarios.

Alongside the revision of testing boards, three sample holders designed for superconducting device measurements have been fabricated. Simulations and discussions are included to address potential box mode resonances arising from chip-board parallel plate interactions, as well as the incorporation of high-permeability magnetic shielding.

Finally, an on-board calibration scheme is proposed alongside an experimental setup designed for measurement and calibration at the base temperature stage within the dilution fridge. This approach aims to minimize error sources by integrating on-board compatible integrated circuit switches, ensuring consistent electrical paths up to the input port of the RF switches. Additionally, this configuration enables measurements within the sample puck, reducing the time required for cooling and warming cycles during sample changes.

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The proposed calibration scheme utilizes custom RF switches introduced in Chapter 3. For comparison, two other configurations discussed in Chapter 4 are included. Initially, calibration tests are conducted exclusively within the sample puck at room temperature. Alongside interchanging Line standards as DUTs, a 1 pF SMD ceramic capacitor is also used as the DUT. The proposed approach demonstrates superior and more consistent calibration results compared to the eight-cable configuration used in the straightforward calibration scheme of Chapter 4, thus affirming the efficacy of the improved proposed method.

Chapter 6 Conclusion

6.1 Summary

In this thesis, several cryogenic microwave circuitries along with calibration and measurement systems for quantum computing-related applications are studied. A cryo-CMOS LNA designed for the reflectometry readout of spin qubit systems is presented. Featuring a novel topology involving a mutual noise-canceling technique, the proposed LNA exhibits superior noise and gain performance with minimized power consumption. Although some issues were encountered in the measured noise figure results at lower frequencies of the implemented circuit, the performance of the prototype LNA achieves a superior figure of merit compared to the reported LNAs in the literature at room temperature.

Motivated by the development of cryogenic measurement systems for quantum devices, a series of studies covering various design purposes and applications were conducted. Several topics in the development of sample holder boards were discussed, including material selection for cryogenic use, microwave engineering in the system, box-mode resonance issues with magnetic shielding for superconducting devices, and other mechanical and electrical challenges. In the first phase of experiments, the cryogenic durability of the testing board materials was verified. Although microwave transmission within the dilution fridge was characterized, the straightforward calibration scheme led to undesired fluctuations and errors.

To improve calibration results within the dilution fridge, a cryogenic broadband SP4T switch is introduced as a core component in the refined calibration scheme. A systematic design approach for a single-pole-multi-throw broadband switch is proposed, utilizing LC-ladder low-pass filter theory to synthesize the desired circuit responses. The

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proposed broadband switch exhibits leakage power of only 0.6 µW at 4 K, making it suitable for operation within the calibration system at the base temperature stage of the dilution fridge. Following the revision of sample holders to multi-board structures, a set of cryogenic calibration boards was implemented, integrating the fabricated SP4T switch. An improved calibration scheme is proposed, incorporating directional couplers and cryogenic amplifiers within the dilution fridge to enhance measurement system sensitivity. Moreover, replacing the connectorized electromechanical switch with our on-board SP4T switch within the sample puck not only reduces sources of error and discrepancies among paths but also minimizes cooling and warming cycle times for changing samples under test. Additionally, the proposed calibration system de-embeds the reference plane of the device measurement to the edge of the sample chip, which is desirable for further minimizing packaging interference in the connectorized system. The calibrated results of the proposed system successfully eliminate fluctuations observed in the results of the previous straightforward calibration scheme. This represents a significant advancement in cryogenic calibration and measurement systems, facilitating a deeper understanding of microwave behavior in future quantum device research.

6.2 Future Work

Further investigation into the low-frequency behavior of the proposed cryo-CMOS LNA is necessary. To mitigate ripples and spikes in the *S*-parameter responses at low frequencies, it is essential to explore the use of off-chip bypass networks on the mounting boards. Despite these efforts, simulations still show residual deviation in the noise figure. This additional noise is suspected to stem from interference from radio and RF signals in the measurement environment. The dc wires in the measurement setup act as antennas, picking up these ambient signals, which are then amplified by the high gain of the LNA, leading to noise fluctuations within the circuit. To verify this hypothesis, the proposed

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LNA may need to be enclosed in a metal housing and tested in a shielding room, with the dc wires covered with aluminum foil. Additionally, packaging the circuit in a connectorized housing allows for stable noise measurement at cryogenic temperatures, where uncertainties in probing can enlarge the variance of the measured noise temperature. In summary, future work on the proposed LNA involves three main directions: first, addressing and potentially resolving the low-frequency noise issue at room temperature; second, resuming on-wafer *S*-parameter measurements using the 4-K prober, which were previously paused due to technical issues; and finally, evaluating the packaged responses of the proposed LNA within the metal housing at both room temperature and cryogenic temperatures, respectively.

Regarding the cryogenic calibration and measurement system, the experiments in this thesis demonstrate operation within the sample puck only at room temperature. The next phase involves measurements with the sample puck installed within the dilution fridge at both room temperature and the base temperature. This also necessitates the characterization and integration of other components required in the calibration system. Further validation of the efficacy of the calibration scheme requires measurements and calibration of truly quantum-related devices, such as Josephson junctions, SQUIDs, superconducting resonators, or superconducting parametric amplifiers. Improving the calibration results may require refining the symmetry of responses among ports of the SP4T switch. In the long term, future work might involve using an SP4T switch with flip-chip packaging, which could further reduce discrepancies originating from bond wires.

References

[1] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver, "A quantum engineer's guide to superconducting qubits," *Applied Physics Reviews,* vol. 6, no. 2, p. 021318, 2019, doi: 10.1063/1.5089550.

[2] F. Arute *et al.*, "Quantum supremacy using a programmable superconducting processor," *Nature,* vol. 574, no. 7779, pp. 505-510, 2019, doi: 10.1038/s41586-019-1666-5.

[3] G. Burkard, T. D. Ladd, A. Pan, J. M. Nichol, and J. R. Petta, "Semiconductor spin qubits," *Reviews of Modern Physics,* vol. 95, no. 2, 2023, doi: 10.1103/revmodphys.95.025003.

[4] J. C. Bardin *et al.*, "Design and characterization of a 28-nm bulk-CMOS cryogenic quantum controller dissipating less than 2 mW at 3 K," *IEEE Journal of Solid-State Circuits,* vol. 54, no. 11, pp. 3043-3060, 2019, doi: 10.1109/jssc.2019.2937234.

[5] J. Park *et al.*, "A fully integrated cryo-CMOS SoC for state manipulation, readout, and high-speed gate pulsing of spin qubits," *IEEE Journal of Solid-State Circuits,* vol. 56, no. 11, pp. 3289-3306, 2021, doi: 10.1109/jssc.2021.3115988.

[6] B. Prabowo *et al.*, "13.3 A 6-to-8GHz 0.17mW/qubit cryo-CMOS receiver for multiple spin qubit readout in 40nm CMOS technology," 2021 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021, pp. 212-214, doi: 10.1109/isscc42613.2021.9365848.

[7] A. Ruffino, Y. Peng, T.-Y. Yang, J. Michniewicz, M. F. Gonzalez-Zalba, and E. Charbon, "13.2 A fully-integrated 40-nm 5-6.5 GHz cryo-CMOS system-on-chip with I/Q receiver and frequency synthesizer for scalable multiplexed readout of quantum dots," 2021 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021: IEEE, pp. 210-212, doi:

doi:10.6342/NTU202402277

10.1109/isscc42613.2021.9365758.

[8] S. Shahrabadi, "Ultrawideband LNA 1960–2019: Review," *IET Circuits, Devices & Systems,* vol. 15, no. 8, pp. 697-727, 2021, doi: 10.1049/cds2.12071.

[9] A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 12, pp. 2259-2268, 2004, doi: 10.1109/jssc.2004.836338.

[10] M. T. Reiha and J. R. Long, "A 1.2 V reactive-feedback 3.1–10.6 GHz low-noise amplifier in 0.13 μm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 42, no. 5, pp. 1023-1033, 2007, doi: 10.1109/jssc.2007.894329.

[11] J. Kim, S. Hoyos, and J. Silva-Martinez, "Wideband common-gate CMOS LNA employing dual negative feedback with simultaneous noise, gain, and bandwidth optimization," *IEEE Transactions on Microwave Theory and Techniques,* vol. 58, no. 9, pp. 2340-2351, 2010, doi: 10.1109/tmtt.2010.2057790.

[12] M. Parvizi, K. Allidina, and M. N. El-Gamal, "An ultra-low-power wideband inductorless CMOS LNA with tunable active shunt-feedback," *IEEE Transactions on Microwave Theory and Techniques,* vol. 64, no. 6, pp. 1843-1853, 2016, doi: 10.1109/tmtt.2016.2562003.

[13] E. A. Sobhy, A. A. Helmy, S. Hoyos, K. Entesari, and E. Sanchez-Sinencio, "A 2.8-mW sub-2-dB noise-figure inductorless wideband CMOS LNA employing multiple feedback," *IEEE Transactions on Microwave Theory and Techniques,* vol. 59, no. 12, pp. 3154-3161, 2011, doi: 10.1109/tmtt.2011.2169081.

[14] Z. Pan, C. Qin, Z. Ye, Y. Wang, and Z. Yu, "Wideband inductorless low-power LNAs with gm enhancement and noise-cancellation," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 65, no. 1, pp. 26-38, 2018, doi: 10.1109/tcsi.2017.2710057.

[15] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 2, pp. 275-282, 2004, doi: 10.1109/jssc.2003.821786.

[16] S. Kim and K. Kwon, "A 50-MHz–1-GHz 2.3-dB NF noise-cancelling balun-LNA employing a modified current-bleeding technique and balanced loads," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 66, no. 2, pp. 546-554, 2019, doi: 10.1109/tcsi.2018.2866184.

[17] S. Kim and K. Kwon, "Broadband balun-LNA employing local feedback gm-boosting technique and balanced loads for low-power low-voltage applications," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 67, no. 12, pp. 4631-4640, 2020, doi: 10.1109/tcsi.2020.3014194.

[18] A. Bozorg and R. B. Staszewski, "A 0.02–4.5-GHz LN(T)A in 28-nm CMOS for 5G exploiting noise reduction and current reuse," *IEEE Journal of Solid-State Circuits,* vol. 56, no. 2, pp. 404-415, 2021, doi: 10.1109/jssc.2020.3018680.

[19] A. Bozorg and R. B. Staszewski, "A 20 MHz–2 GHz inductorless two-fold noise-canceling low-noise amplifier in 28-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 69, no. 1, pp. 42-50, 2022, doi: 10.1109/tcsi.2021.3092960.

[20] R. Zhou, S. Liu, J. Liu, Y. Liang, and Z. Zhu, "A 0.1–3.5-GHz inductorless noise-canceling CMOS LNA with IIP3 optimization technique," *IEEE Transactions on Microwave Theory and Techniques,* vol. 70, no. 6, pp. 3234-3243, 2022, doi: 10.1109/tmtt.2022.3161279.

[21] B. Guo, J. Chen, L. Li, H. Jin, and G. Yang, "A wideband noise-canceling CMOS LNA with enhanced linearity by using complementary nMOS and pMOS configurations," *IEEE Journal of Solid-State Circuits,* vol. 52, no. 5, pp. 1331-1344,

2017, doi: 10.1109/jssc.2017.2657598.

[22] K.-H. Chen and S.-I. Liu, "Inductorless wideband CMOS low-noise amplifiers using noise-canceling technique," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 59, no. 2, pp. 305-314, 2012, doi: 10.1109/tcsi.2011.2162461.

[23] S. S. Regulagadda, B. D. Sahoo, A. Dutta, K. Y. Varma, and V. S. Rao, "A packaged noise-canceling high-gain wideband low noise amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 66, no. 1, pp. 11-15, 2019, doi: 10.1109/tcsii.2018.2828781.

[24] Y.-C. Cheng and H.-C. Chen, "CMOS LNA for DTV-Band cognitive radio applications," 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, 2021, pp. 1-5, doi: 10.1109/iscas51556.2021.9401225.

[25] J.-Y. Bae, S. Kim, H.-S. Cho, I.-Y. Lee, D. S. Ha, and S.-G. Lee, "A CMOS wideband highly linear low-noise amplifier for digital TV applications," *IEEE Transactions on Microwave Theory and Techniques,* vol. 61, no. 10, pp. 3700-3711, 2013, doi: 10.1109/tmtt.2013.2278156.

[26] T. Chung, H. Lee, D. Jeong, J. Yoon, and B. Kim, "A wideband CMOS noise-canceling low-noise amplifier with high linearity," *IEEE Microwave and Wireless Components Letters,* vol. 25, no. 8, pp. 547-549, 2015, doi: 10.1109/lmwc.2015.2440762.

[27] H. Yu, Y. Chen, C. C. Boon, C. Li, P.-I. Mak, and R. P. Martins, "A 0.044-mm^2 0.5-to-7-GHz resistor-plus-source-follower-feedback noise-cancelling LNA achieving a flat NF of 3.3±0.45 dB," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 66, no. 1, pp. 71-75, 2019, doi: 10.1109/tcsii.2018.2833553.

[28] P. B. T. Huynh, J.-H. Kim, and T.-Y. Yun, "Dual-resistive feedback wideband LNA for noise cancellation and robust linearization," *IEEE Transactions on Microwave*

doi:10.6342/NTU202402277

Theory and Techniques, vol. 70, no. 4, pp. 2224-2235, 2022, doi: 10.1109/tmtt.2021.3139331.

[29] Y. Guo *et al.*, "Cryogenic CMOS RF circuits: A promising approach for large-scale quantum computing," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 71, no. 3, pp. 1619-1625, 2024, doi: 10.1109/tcsii.2023.3333540.

[30] A. Beckers, F. Jazaeri, A. Ruffino, C. Bruschini, A. Baschirotto, and C. Enz, "Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing," 2017 47th European Solid-State Device Research Conference (ESSDERC), Leuven, Belgium, 2017, pp. 62-65, doi: 10.1109/essderc.2017.8066592.

[31] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures," *IEEE Journal of the Electron Devices Society,* vol. 6, pp. 996-1006, 2018, doi: 10.1109/jeds.2018.2821763.

[32] S.-H. Hong, G.-B. Choi, R.-H. Baek, H.-S. Kang, S.-W. Jung, and Y.-H. Jeong, "Low-temperature performance of nanoscale MOSFET for deep-space RF applications," *IEEE Electron Device Letters,* vol. 29, no. 7, pp. 775-777, 2008, doi: 10.1109/led.2008.2000614.

[33] Z. Tang *et al.*, "Cryogenic CMOS RF device modeling for scalable quantum computer design," *IEEE Journal of the Electron Devices Society,* vol. 10, pp. 532-539, 2022, doi: 10.1109/jeds.2022.3186979.

[34] X. Chen, H. Elgabra, C.-H. Chen, J. Baugh, and L. Wei, "Estimation of MOSFET channel noise and noise performance of CMOS LNAs at cryogenic temperatures," 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, 2021, pp. 1-5, doi: 10.1109/iscas51556.2021.9401136.

[35] B. Patra *et al.*, "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE Journal of Solid-State Circuits,* vol. 53, no. 1, pp. 309-321, 2018, doi: 10.1109/jssc.2017.2737549.

[36] B. Patra, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon, and M. Babaie, "Characterization and analysis of on-chip microwave passive components at cryogenic temperatures," *IEEE Journal of the Electron Devices Society,* vol. 8, pp. 448-456, 2020, doi: 10.1109/jeds.2020.2986722.

[37] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOS transistor model," *IEEE Transactions on Electron Devices,* vol. 65, no. 9, pp. 3617-3625, 2018, doi: 10.1109/ted.2018.2854701.

[38] A. Beckers, F. Jazaeri, and C. Enz, "Characterization and modeling of 28-nm bulk CMOS technology down to 4.2 K," *IEEE Journal of the Electron Devices Society,* vol. 6, pp. 1007-1018, 2018, doi: 10.1109/jeds.2018.2817458.

[39] M. W. Pospieszalski, "Extremely low-noise cryogenic amplifiers for radio astronomy: past, present and future," 2018 22nd International Microwave and Radar Conference (MIKON), Poznan, Poland, 2018, pp. 1-6, doi: 10.23919/mikon.2018.8514558.

[40] C.-C. Chiong, Y. Wang, K.-C. Chang, and H. Wang, "Low-noise amplifier for next-generation radio astronomy telescopes: Review of the state-of-the-art cryogenic LNAs in the most challenging applications," *IEEE Microwave Magazine,* vol. 23, no. 1, pp. 31-47, 2022, doi: 10.1109/mmm.2021.3117318.

[41] Y. Peng, Y. Zhong, Z. Guo, S. Liu, and D. Yu, "A 3.5~7.5 GHz GaAs HEMT cryogenic low-noise amplifier achieving 5 Kelvin noise temperature for qubits measurement," 2023 IEEE/MTT-S International Microwave Symposium (IMS), San Diego, CA, USA, 2023, pp. 672-675, doi: 10.1109/ims37964.2023.10188012.

doi:10.6342/NTU202402277

[42] E. Cha *et al.*, "0.3-14 and 16-28 GHz wide-bandwidth cryogenic MMIC low-noise amplifiers," *IEEE Transactions on Microwave Theory and Techniques,* pp. 1-10, 2018, doi: 10.1109/tmtt.2018.2872566.

[43] E. Cha, N. Wadefalk, G. Moschetti, A. Pourkabirian, J. Stenarson, and J. Grahn, "A 300-μW cryogenic HEMT LNA for quantum computing," 2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 2020: IEEE, pp. 1299-1302, doi: 10.1109/ims30576.2020.9223865.

[44] W.-T. Wong, M. Hosseini, H. Rucker, and J. C. Bardin, "A 1 mW cryogenic LNA exploiting optimized SiGe HBTs to achieve an average noise temperature of 3.2 K from 4–8 GHz," 2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 2020, pp. 181-184, doi: 10.1109/ims30576.2020.9224049.

[45] M. Hosseini and J. C. Bardin, "A 1 mW 0.1-3 GHz cryogenic SiGe LNA with an average noise temperature of 4.6 K," 2021 IEEE MTT-S International Microwave Symposium (IMS), Atlanta, GA, USA, 2021, pp. 896-899, doi: 10.1109/ims19712.2021.9574993.

[46] J.-O. Plouchart *et al.*, "A 2.57mW 5.9-8.4GHz cryogenic FinFET LNA for qubit readout," 2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Denver, CO, USA, 2022, pp. 27-30, doi: 10.1109/rfic54546.2022.9863158.

[47] S. Das, S. Raman, and J. C. Bardin, "Design and implementation of a 3.9-to-5.3 GHz 65 nm cryo-CMOS LNA with an average noise temperature of 10.2K," 2022 IEEE/MTT-S International Microwave Symposium (IMS), Denver, CO, USA, 2022, pp. 719-722, doi: 10.1109/ims37962.2022.9865392.

[48] Y. Peng, A. Ruffino, and E. Charbon, "A cryogenic broadband sub-1-dB NF CMOS low noise amplifier for quantum applications," *IEEE Journal of Solid-State Circuits,* vol. 56, no. 7, pp. 2040-2053, 2021, doi: 10.1109/jssc.2021.3073068.

[49] A. Caglar, S. Van Winckel, S. Brebels, P. Wambacq, and J. Craninckx, "Design and analysis of a 4.2 mW 4 K 6–8 GHz CMOS LNA for superconducting qubit readout," *IEEE Journal of Solid-State Circuits,* vol. 58, no. 6, pp. 1586-1596, 2023, doi: 10.1109/jssc.2022.3219060.

[50] A. Sheldon and L. Belostotski, "A cryo-CMOS low-noise amplifier with 2.3-to-8.5-K noise temperature at 20 K for highly integrated radio-astronomy receivers," *IEEE Microwave and Wireless Components Letters,* vol. 32, no. 11, pp. 1319-1322, 2022, doi: 10.1109/lmwc.2022.3178579.

[51] M. K. Chaubey, Y. Liu, P.-C. Wu, H.-H. Tsai, and S. S. H. Hsu, "A miniature 10MHz-3GHz sub 1-dB NF cryogenic inductorless noise-canceling Low-noise amplifier for qubit readout," 2023 IEEE/MTT-S International Microwave Symposium (IMS), San Diego, CA, USA, 2023, pp. 668-671, doi: 10.1109/ims37964.2023.10187946.

[52] M. K. Chaubey, Y. Liu, Y.-C. Chang, P.-C. Wu, H.-H. Tsai, and S. S. H. Hsu, "Ultracompact inductorless noise-canceling LNAs in 40-nm CMOS achieving 2.2-K noise temperature for qubit readout," *IEEE Transactions on Microwave Theory and Techniques,* vol. 72, no. 4, pp. 2168-2178, 2024, doi: 10.1109/tmtt.2024.3356653.

[53] M. K. Chaubey, C.-C. Lin, Y.-C. Chang, P.-C. Wu, H.-H. Tsai, and S. S. H. Hsu, "A 0.01-to-2.6-GHz two-fold current reuse dual noise-canceling LNA achieving 6.8-K noise temperature for quantum applications," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 71, no. 5, pp. 2504-2508, 2024, doi: 10.1109/tcsii.2024.3378382.

[54] X. Li and Y. Zhang, "Flipping the CMOS switch," *IEEE Microwave Magazine,* vol. 11, no. 1, pp. 86-96, Feb. 2010, doi: 10.1109/mmm.2009.935203.

[55] Q. Li and Y. P. Zhang, "CMOS T/R switch design: towards ultra-wideband and higher frequency," *IEEE Journal of Solid-State Circuits,* vol. 42, no. 3, pp. 563-570, Mar. 2007, doi: 10.1109/jssc.2006.891442.

[56] Q. Li, Y. P. Zhang, K. S. Yeo, and W. M. Lim, "16.6- and 28-GHz fully integrated CMOS RF switches with improved body floating," *IEEE Transactions on Microwave Theory and Techniques,* vol. 56, no. 2, pp. 339-345, Feb. 2008, doi: 10.1109/tmtt.2007.914364.

[57] B.-W. Min and G. M. Rebeiz, "Ka-band low-loss and high-isolation 0.13-µm CMOS SPST/SPDT switches using high substrate resistance," 2007 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Honolulu, HI, USA, 2007, pp. 569-572, doi: 10.1109/rfic.2007.380948.

[58] N. A. Talwalkar, C. P. Yue, G. Haitao, and S. S. Wong, "Integrated CMOS transmit-receive switch using LC-tuned substrate bias for 2.4-GHz and 5.2-GHz applications," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 6, pp. 863-870, Jun. 2004, doi: 10.1109/jssc.2004.827809.

[59] Y. Jin and C. Nguyen, "Ultra-compact high-linearity high-power fully integrated dc-20-GHz 0.18-µm CMOS T/R switch," *IEEE Transactions on Microwave Theory and Techniques,* vol. 55, no. 1, pp. 30-36, Jan. 2007, doi: 10.1109/tmtt.2006.888944.

[60] B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A miniature dc-70 GHz SP4T switch in 0.13-µm CMOS," 2009 IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA, 2009, pp. 1093-1096, doi: 10.1109/mwsym.2009.5165891.

[61] H.-Y. Chang and C.-Y. Chan, "A low loss high isolation dc-60 GHz SPDT traveling-wave switch with a body bias technique in 90 nm CMOS process," *IEEE Microwave and Wireless Components Letters,* vol. 20, no. 2, pp. 82-84, Feb. 2010,

doi: 10.1109/lmwc.2009.2038518.

[62] Y. Mei-Chao, T. Zuo-Min, and H. Wang, "A miniature dc-to-50 GHz CMOS SPDT distributed switch," 2005 European Gallium Arsenide and Other Semiconductor Application Symposium (GAAS), Paris, France, 2005, pp. 665-668, doi: 10.1109/eumc.2005.1610263.

[63] C. Chen, X. Xu, and T. Yoshimasu, "A dc-50 GHz, low insertion loss and high P1dB SPDT switch IC in 40-nm SOI CMOS," 2017 IEEE Asia Pacific Microwave Conference (APMC), Kuala Lumpur, Malaysia, 2017, pp. 5-8, doi: 10.1109/apmc.2017.8251363.

[64] A. S. Cardoso, P. Saha, P. S. Chakraborty, D. M. Fleischhauer, and J. D. Cressler, "Low-loss, wideband SPDT switches and switched-line phase shifter in 180-nm RF CMOS on SOI technology," 2014 IEEE Radio and Wireless Symposium (RWS), Newport Beach, CA, USA, 2014, pp. 199-201, doi: 10.1109/rws.2014.6830161.

[65] M. Parlak and J. F. Buckwalter, "A 2.5-dB insertion loss, dc-60 GHz CMOS SPDT switch in 45-nm SOI," 2011 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Waikoloa, HI, USA, 2011, pp. 1-4, doi: 10.1109/csics.2011.6062463.

[66] B. Yu *et al.*, "Ultra-wideband low-loss switch design in high-resistivity trap-tich SOI with enhanced channel mobility," *IEEE Transactions on Microwave Theory and Techniques,* vol. 65, no. 10, pp. 3937-3949, Oct. 2017, doi: 10.1109/tmtt.2017.2696944.

[67] K. Y. Lin, T. Wen-Hua, C. Ping-Yu, C. Hong-Yeh, H. Wang, and W. Ruey-Beei, "Millimeter-wave MMIC passive HEMT switches using traveling-wave concept," *IEEE Transactions on Microwave Theory and Techniques,* vol. 52, no. 8, pp. 1798-1808, Aug. 2004, doi: 10.1109/tmtt.2004.831574.

doi:10.6342/NTU202402277

[68] L. Wu, H. Y. Hsu, and S. P. Voinigescu, "A dc to 220-GHz high-isolation SPST switch in 22-nm FDSOI CMOS," *IEEE Microwave and Wireless Components Letters,* vol. 31, no. 6, pp. 775-778, Jun. 2021, doi: 10.1109/lmwc.2021.3067003.

[69] L. M. T. Quémerais, J.-M. Fournier, P. Benech, "A SPDT switch in a standard 45 nm CMOS process for 94 GHz applications," 2010 40th European Microwave Conference (EuMC), Paris, France, 2010, pp. 425-428, doi: 10.23919/eumc.2010.5614766.

[70] H.-R. Zhu, X.-Y. Ning, Z.-X. Huang, Y.-X. Guo, and X.-L. Wu, "Miniaturized, ultra-wideband and high isolation single pole double throw switch by using π-type topology in GaAs pHEMT technology," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 68, no. 1, pp. 191-195, Jan. 2021, doi: 10.1109/tcsii.2020.3001171.

[71] C. D. Cheon, M.-K. Cho, S. G. Rao, A. S. Cardoso, J. D. Connor, and J. D. Cressler, "A new wideband, low insertion soss, high linearity SiGe RF switch," *IEEE Microwave and Wireless Components Letters,* vol. 30, no. 10, pp. 985-988, Oct. 2020, doi: 10.1109/lmwc.2020.3020317.

[72] G. Shen, H. Zhu, Q. Cai, D. Zeng, Q. Xue, and W. Che, "Compact nultipole GaN-on-Si SPDT switch using inductive parasitic effects of hybrid HEMT devices," *IEEE Transactions on Microwave Theory and Techniques,* vol. 71, no. 11, pp. 4778-4786, Nov. 2023, doi: 10.1109/tmtt.2023.3267543.

[73] F. Amin *et al.*, "Wideband SPDT and SP4T RF switches using phase-change material in a SiGe BiCMOS process," 2021 IEEE MTT-S International Microwave Symposium (IMS), Atlanta, GA, USA, 2021, pp. 431-434, doi: 10.1109/ims19712.2021.9574962.

[74] B. Y. Ma, J. Bergman, J. B. Hacker, G. Sullivan, A. Sailer, and B. Brar, "Low loss

doi:10.6342/NTU202402277

cryogenic InAs/AlSb HEMT non-reflective SP4T switch," 2011 IEEE MTT-S International Microwave (IMS), Baltimore, MD, USA, 2011, pp. 1-4, doi: 10.1109/mwsym.2011.5972601.

[75] A. S. Cardoso, P. S. Chakraborty, A. P. Omprakash, N. Karaulac, P. Saha, and J. D. Cressler, "On the cryogenic performance of ultra-low-loss, wideband SPDT RF switches designed in a 180 nm SOI-CMOS technology," 2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Millbrae, CA, USA, 2014, pp. 1-2, doi: 10.1109/s3s.2014.7028204.

[76] T. D. Nhut *et al.*, "Cryogenic compact mm-wave broadband SPST switch in 22nm FDSOI CMOS for monolithic quantum processors," 2022 IEEE/MTT-S International Microwave Symposium (IMS), Denver, CO, USA, 2022, pp. 168-171, doi: 10.1109/ims37962.2022.9865577.

[77] A. Potočnik *et al.*, "Millikelvin temperature cryo-CMOS multiplexer for scalable quantum device characterisation," *Quantum Science and Technology,* vol. 7, no. 1, p. 015004, Oct. 2021, doi: 10.1088/2058-9565/ac29a1.

[78] R. Acharya *et al.*, "Scalable 1.4 μW cryo-CMOS SP4T multiplexer operating at 10 mK for high-fidelity superconducting qubit measurements," 2022 IEEE Symposium on VLSI Technology and Circuits, Honolulu, HI, USA, 2022, pp. 230-231, doi: 10.1109/vlsitechnologyandcir46769.2022.9830396.

[79] R. Acharya *et al.*, "Multiplexed superconducting qubit control at millikelvin temperatures with a low-power cryo-CMOS multiplexer," *Nature Electronics,* vol. 6, no. 11, pp. 900-909, Sep. 2023, doi: 10.1038/s41928-023-01033-8.

[80] G. L. Matthaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance-matching Networks, and Coupling Structures*. Artech House, 1980.

[81] J. I. Colless and D. J. Reilly, "Cryogenic high-frequency readout and control

doi:10.6342/NTU202402277

platform for spin qubits," *Review of Scientific Instruments,* vol. 83, no. 2, p. 023902, 2012, doi: 10.1063/1.3681195.

[82] J. I. Colless and D. J. Reilly, "Modular cryogenic interconnects for multi-qubit devices," *Review of Scientific Instruments,* vol. 85, no. 11, p. 114706, 2014, doi: 10.1063/1.4900948.

[83] M. L. V. Tagliaferri *et al.*, "Modular printed circuit boards for broadband characterization of nanoelectronic quantum devices," *IEEE Transactions on Instrumentation and Measurement,* vol. 65, no. 8, pp. 1827-1835, 2016, doi: 10.1109/tim.2016.2555178.

[84] M. Madsen, "Investigating timescales for quasi-particle poisoning in superconducting quantum dots in InAs nanowires," M.S. thesis, Niels Bohr Institute, Copenhagen University, 2016.

[85] K. Chang and L.-H. Hsieh, *Microwave ring circuits and related structures*. John Wiley & Sons, 2004.

[86] C.-C. Huang, H.-C. Wang, W.-Z. Fu, P.-X. Liu, and Y.-C. Liu, "Determination of dielectric constant and dissipation factor of printed circuit board by microstrip with ring and straight-line resonator measurements," 2022 17th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), Taipei, Taiwan, 2022, pp. 1-4, doi: 10.1109/impact56280.2022.9966721.

[87] Z. Lei and K. Wu, "Line-to-ring coupling circuit model and its parametric effects for optimized design of microstrip ring circuits and antennas," 1997 IEEE MTT-S International Microwave Symposium (IMS), Denver, CO, USA, 1997, vol. 1, pp. 289-292, doi: 10.1109/mwsym.1997.604576.

[88] P. Ji-Yong and L. Jong-Chul, "A new enhanced coupling structure of microstrip

ring resonator with two coupled lines and a slit," 1998 IEEE MTT-S International Microwave Symposium (IMS), Baltimore, MD, USA, 1998, vol. 2, pp. 805-808, doi: 10.1109/mwsym.1998.705112.

[89] D. M. Pozar, *Microwave Engineering*. Wiley, 2011.

[90] G. F. Engen and C. A. Hoer, "Thru-reflect-line: An improved technique for calibrating the dual six-port automatic network analyzer," *IEEE Transactions on Microwave Theory and Techniques,* vol. 27, no. 12, pp. 987-993, 1979, doi: 10.1109/tmtt.1979.1129778.

[91] M. Zannoni, M. Gervasi, A. Bau, and A. Passerini, "A cryogenic set-up for accurate characterization of microwave components for astrophysics," 2013 International Conference on Electromagnetics in Advanced Applications (ICEAA), Turin, Italy, 2013, pp. 113-116, doi: 10.1109/iceaa.2013.6632200.

[92] P. Diener, F. Couëdo, C. Marrache-Kikuchi, M. Aprili, and J. Gabelli, "Cryogenic calibration setup for broadband complex impedance measurements," in *AIP Conference Proceedings*, 2014, vol. 1610, pp. 113-118, doi: 10.1063/1.4893520.

[93] H. Wang *et al.*, "Cryogenic single-port calibration for superconducting microwave resonator measurements," *Quantum Science and Technology,* vol. 6, no. 3, p. 035015, 2021, doi: 10.1088/2058-9565/ac070e.

[94] T. Arakawa and S. Kon, "Calibrated two-port microwave measurement up to 26.5 GHz for wide temperature range from 4 to 300 K," *IEEE Transactions on Instrumentation and Measurement,* vol. 72, pp. 1-8, 2023, doi: 10.1109/tim.2023.3315393.

[95] S. Simbierowicz, V. Y. Monarkha, S. Singh, N. Messaoudi, P. Krantz, and R. E. Lake, "Microwave calibration of qubit drive line components at millikelvin temperatures," *Applied Physics Letters,* vol. 120, no. 5, p. 054004, 2022, doi:

10.1063/5.0081861.

[96] S. Simbierowicz, V. Y. Monarkha, M. Von Soosten, S. Andresen, and R. E. Lake, "Calibrated transmission and reflection from a multi-qubit microwave package," *Review of Scientific Instruments,* vol. 94, no. 5, 2023, doi: 10.1063/5.0144840.

[97] L. Ranzani, L. Spietz, Z. Popovic, and J. Aumentado, "Two-port microwave calibration at millikelvin temperatures," *Review of Scientific Instruments,* vol. 84, no. 3, p. 034704, 2013, doi: 10.1063/1.4794910.

[98] M. Stanley, S. E. De Graaf, T. Lindstrom, M. J. Salter, J. Skinner, and N. M. Ridler, "Design of microwave calibration standards for characterising S-parameters of quantum integrated circuits at millikelvin temperatures," 2021 51st European Microwave Conference (EuMC), London, United Kingdom, 2022, pp. 639-642, doi: 10.23919/eumc50147.2022.9784174.

[99] M. Stanley, S. De Graaf, T. Honigl-Decrinis, T. Lindstrom, and N. M. Ridler, "Characterizing parameters of superconducting quantum integrated circuits at milli-Kelvin temperatures," *IEEE Access,* vol. 10, pp. 43376-43386, 2022, doi: 10.1109/access.2022.3169787.

[100] M. Stanley, R. Parker-Jervis, S. De Graaf, T. Lindström, J. E. Cunningham, and N. M. Ridler, "Validating S-parameter measurements of RF integrated circuits at milli-kelvin temperatures," *Electronics Letters,* 2022, doi: 10.1049/ell2.12545.

[101] D. E. Oates, R. L. Slattery, and D. J. Hover, "Cryogenic test fixture for two-port calibration at 4.2 K and above," 2017 89th ARFTG Microwave Measurement Conference (ARFTG), Honololu, HI, USA, 2017, pp. 1-4, doi: 10.1109/arftg.2017.8000842.

[102] Y. Chen *et al.*, "Fast microwave calibration system for cryogenic device characterization," *Journal of Instrumentation,* vol. 17, no. 11, p. P11021, 2022.

doi:10.6342/NTU202402277

[103] J.-H. Yeh and S. M. Anlage, "In situ broadband cryogenic calibration for two-port superconducting microwave resonators," *Review of Scientific Instruments,* vol. 84, no. 3, 2013.

[104] M. Stanley, S.-H. Shin, J. Skinner, J. Urbonas, and N. Ridler, "Characterising scattering parameters of coaxial microwave devices at milli-kelvin temperatures for quantum computing technologies," 2023 53rd European Microwave Conference (EuMC), Berlin, Germany, 2023, pp. 150-153, doi: 10.23919/eumc58039.2023.10290560.

[105] J. Skinner, M. Stanley, J. Urbonas, S. De Graaf, T. Lindström, and N. Ridler, "Characterizing precision coaxial air lines as reference standards for cryogenic S-parameter measurements at milli-kelvin temperatures," 2023 IEEE/MTT-S International Microwave Symposium (IMS), San Diego, CA, USA, 2023, pp. 561-564, doi: 10.1109/ims37964.2023.10188171.

[106] S.-H. Shin, M. Stanley, J. Skinner, S. E. De Graaf, and N. M. Ridler, "Broadband coaxial S-parameter measurements for cryogenic quantum technologies," *IEEE Transactions on Microwave Theory and Techniques,* vol. 72, no. 4, pp. 2193-2201, 2024, doi: 10.1109/tmtt.2023.3322909.

[107] E. M. Wei, R. A. Chamberlin, N. Kilmer, J. Kast, J. A. Connors, and D. Williams, "On-wafer vector-network-analyzer measurements at mK temperatures," *IEEE Journal of Microwaves,* vol. 3, no. 2, pp. 587-598, 2023, doi: 10.1109/jmw.2022.3232076.

[108] P. Bryndza, "VNA measurement calibration in cryogenic environment," 2022 24th International Microwave and Radar Conference (MIKON), Gdansk, Poland, 2022, pp. 1-6, doi: 10.23919/mikon54314.2022.9924695.

doi:10.6342/NTU202402277