國立臺灣大學電機資訊學院電信工程學研究所

碩士論文

Graduate Institute of Communication Engineering
College of Electrical Engineering and Computer Science
National Taiwan University

Master Thesis

24 GHz 高轉換增益低雜訊混頻器及毫米波高鏡像抑制比率升降頻混頻器與模組之研究

Research on 24 GHz High Conversion Gain, Low Noise Mixer and Millimeter-Wave High Image Rejection Ratio Up-/Down-Conversion Mixer and Module

廖宏博

Hong-Bo Liao

指導教授：林坤佑 博士

Advisor: Kun-You Lin, Ph.D.

中華民國 111 年 9 月

September, 2022

doi:10.6342/NTU202203942

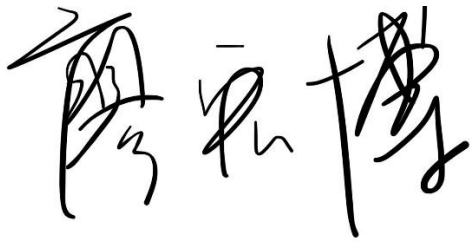
誌謝

首先感謝林坤佑教授的指導，即使電路的 bug 到最後都找不到主因，還是讓我通過口試了。還有感謝 SOSO、譽騰和儷憲學長，三位高手的耐心指導，讓我對 RF 的設計觀念與邏輯更上一層樓。熬了四年，終於要畢業了~

回想起這四年的日子，算是遇到蠻多幫助我的人，從 KY group 的旻憲、致家和秉原學長們，老王那裏的云杉學長和子豪，黃老師實驗室的杰穎、文傑、宜賢和坤展學長們以及婕葦，都是使我邁向畢業之路的好夥伴。我的好同學 1 號昱廷，總是能自己摸索找到解決方法，對於一些程式和軟體也是特別牛皮，還和我一起修了地質調查，雖然只有你找到女友哈哈，真心祝福你們能走到邀請我參加婚禮的那天~我的好同學 2 號柏維，每周 meeting 都看不到你進度的車尾燈，總是每天從早到晚待在實驗室，能夠成為同期最早畢業真的實至名歸；你們兩位總是能夠捧場我的冷笑話讓我備感溫馨<3。還有好同學 3 號宏源，你對於 PA 和模組研究的積極真的也是有點東西，雖然聽說你最近在公司發生了一些事，但我自己覺得你人並不壞只是有點靠北，希望你在職場上還是能交到很多好朋友。學弟妹的部分，首先恭喜雨炫準時畢業而且還比我早 QAQ，感覺你是個很有心事的人，不太會跟我聊天，不過也是祝福你在職場上過得開心；玟辰說真的我沒想過會比你晚離校，只能怪我自己太混，雖然你研究初期也是和我碩二一樣碰壁但真的恭喜你能夠畢業而且進去 MTK~佳君真的是我看過最認真的研究生，兩年準時畢業超強，平時坐我旁邊也是很常跟我聊天，最近聽說你在 Cadence 過得不是很開心，希望你找到自己喜歡的工作然後趕快結婚實現夢想~沛彣也是認真的學妹聲音總是實驗室最高哈哈，做 Mixer 真的很麻煩也很辛苦，

doi:10.6342/NTU202203942

祝你接下來的量測和論文都順利~宥均小姨子和顥庭總是很捧場我的笑話哈哈，我覺得你們最棒了!!梁宏也是可愛的學弟，祝你學會如何認識女生，不要再這麼木訥了~最後我們的家瑋，鬼之簽博，是近期幫我最多的學弟，總是樂於助人，還非常貼心送我拼圖卡片，一起喝完酒後我想說，祝你找到幸福哈哈哈~~



2022.09.23

doi:10.6342/NTU202203942

中文摘要

本論文分為三個部分。第一部分(第二章)提出了設計在 24 GHz 的高轉換增益低雜訊的主動降頻混頻器，使用 0.18 μm CMOS 製程。此電路利用電流注入技巧以及共振電感的使用，有效地降低雜訊指數以及提升轉換增益。然而，兩次下線的量測結果都不如預期，除錯的過程會在內文中討論，目前尚未找到造成嚴重掉增益的原因。

第二部分(第三章)介紹毫米波鏡像抑制的升降頻模組。利用威爾金森分合波器作為主架構，將左手傳輸線上的電容替換成變容二極體藉以實現可調的相位；將 PIN 型二極體引入 T 型衰減器以實現可調的大小。量測的結果在 2.5 到 5 GHz 可以有 80-100°的相位可調範圍以及 (+2)-(-1.1) dB 的大小可調範圍。整個升降頻模組的鏡像抑制比率在 3 到 4.5 GHz 有 50 dB 的水平，在 2.5 和 5 GHz 有 30 dB 的水平。

最後一部分(第四章)提出了應用於第五代行動通訊系統的高鏡像抑制比率升降頻次諧波混頻器，使用 0.15 μm GaAs pHEMT 製程。此電路實現了有很小相位和大小不平衡的 45° LO 分波器，且透過 LO 的級間反射係數的分析，能夠達到高鏡像抑制比率的目的。此外，類集總四分之波長傳輸線的引入，使得端對端的隔離度有很好的表現。藉由第三章的可調式正交分合波器，量測結果在升降頻都有 45 dB 以上的水平。

關鍵字:24 GHz、高增益、低雜訊、電流注入、共振電感、毫米波模組、可調相位、可調大小、第五代行動通訊、高鏡像抑制比率、次諧波升降頻混頻器。

doi:10.6342/NTU202203942

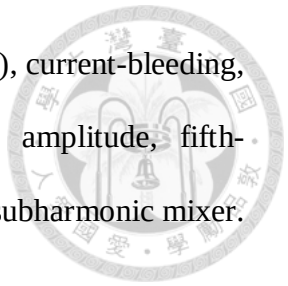
ABSTRACT

This thesis divided into three parts. In the first part (chapter 2), a 24 GHz high conversion gain and low noise down-conversion active mixer in 0.18 μm CMOS process is presented. The current-bleeding technique and the resonant inductor are adopted to obtain high conversion gain and low noise figure. However, after two tape-outs, the reason for the severe reduction in conversion gain has not been found so far.

In the second part (chapter 3), a millimeter-wave up-/down-conversion image rejection module is demonstrated. The capacitors on the left-handed transmission line are replaced with varactors to achieve tunable phase, and the PIN diodes are added to the T-type attenuators to achieve tunable amplitude. The tunable I/Q divider/combiner are based on the Wilkinson power divider. The phase and amplitude tuning at 2.5-5 GHz were measured to be 80-100° and (+2)-(-1.1) dB, respectively. With the great performance of the tunable I/Q divider/combiner, the IRR of the up-/down-conversion image rejection module can reach a 50-dB level at 3-4.5 GHz and a 30-dB level at 2.5 and 5 GHz.

In the last part (chapter 4), a 24-32 GHz high image rejection ratio up-/down-conversion subharmonic mixer in 0.15 μm GaAs pHEMT process is proposed. This circuit realizes a 45° LO power divider with small phase and amplitude imbalances. By analyzing the LO inter-stage reflection coefficient, it is able to achieve the desired high image rejection ratio. Besides, good port-to-port isolation is made possible by the implementation of quasi-lumped $\lambda_{LO}/4$ short/open stubs. With the tunable I/Q divider/combiner in measurement, the IRR in precise phase and amplitude tuning can reach over 45 dB for up-/down-conversion.

doi:10.6342/NTU202203942



Index Terms – 24 GHz, high conversion gain (CG), low noise figure (NF), current-bleeding, resonant inductor, millimeter-wave module, tunable phase, tunable amplitude, fifth-generation (5G), high image rejection ratio (IRR), up-/down-conversion subharmonic mixer.

doi:10.6342/NTU202203942

CONTENTS

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

LIST OF FIGURES

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

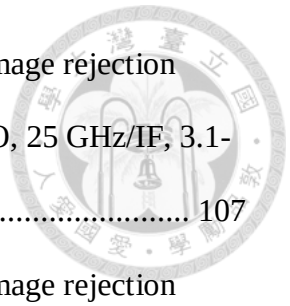
doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942



doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

LIST OF TABLES

doi:10.6342/NTU202203942

doi:10.6342/NTU202203942

Chapter 1 Introduction

1.1 Background and Motivation

Due to the low cost and high level of integration, the rapid expansion of wireless communications has resulted in a significant push toward creating high-performance RF circuits in silicon, particularly CMOS. The increasing demand for wireless applications with high data rates at K band has recently attracted a lot of interest. 24 GHz industrial, scientific, and medical (ISM)-band radar sensors, for example. They are used for automation and interaction in consumer products such as smart appliances, intelligent energy control, and even hands-free trunk and tailgate release on automobiles. Automotive radars use the low-frequency band (24-24.25 GHz) for short/mid-range applications such as blind-spot detection, lane change assistance, rear cross-traffic alert, and collision avoidance. For 24 GHz CMOS receivers, active mixers with high conversion gain, good linearity, low noise figure, high port-to-port isolation, and low power consumption are especially important.

Many countries have already revealed the millimeter-wave frequency ranges that will be used by 5G communication. The US operates at 27.5-28.35 GHz and 37-40 GHz, Europe operates at 24.25-27.5 GHz and 31.8-33.4 GHz, and China operates at 24.25-27.5 GHz and 37 GHz-42.5 GHz. It is evident from the foregoing that 5G communication will be developed in these frequency ranges. The subharmonic mixer is an important technique in millimeter-wave. Subharmonic mixers enable designers to employ lower LO frequencies, decreasing the demand for a high-frequency LO signal and the need for measuring instruments.

doi:10.6342/NTU202203942

Subharmonic mixers are a simpler alternative to traditional mixers without a LO frequency multiplier for high-frequency application design.

In the upcoming 5G communication system, image rejection is also a critical technology for both the receiver and the transmitter. A poor image rejection ratio (IRR) in the transmitter may cause power saturation of the post-stage power amplifier, impacting its operation. While image signal suppression technology has few effects on the receiver's post-stage circuit, it can help filter out the image signal to prevent it converting to the same frequency as the IF signal. A millimeter-wave frequency conversion module that can up and down convert, reducing module complexity and cost while also providing image rejection.

1.2 Contributions

This thesis presents a 24 GHz high conversion gain down-conversion active mixer using noise cancellation technique, a millimeter-wave up-/down-conversion image rejection module, and a 24-32 GHz high image rejection ratio up-/down-conversion subharmonic mixer for 5G communication.

In chapter 2, a 24 GHz high conversion gain and low noise down-conversion active mixer in 0.18 μm CMOS process is presented. The low noise figure is designed based on the current-bleeding technique and the resonant inductor. The conversion gain is efficiently enhanced at the center frequency of 24.1 GHz since the parasitic capacitance is eliminated. The simulated conversion gain is 12.8 dB with a 2 dBm LO power at 24.1 GHz. The noise figure is 34.7 dB at 1 kHz and 9.8 dB at 1 GHz. The corner frequency is about 1 MHz. This mixer shows a high conversion gain at the desired ISM band and a good flicker noise performance in simulation. The severe reduction in conversion gain will be discussed.

doi:10.6342/NTU202203942

In chapter 3, a millimeter-wave up-/down-conversion image rejection module is demonstrated. The tunable phase and amplitude functions are realized by varactors and T-type attenuators. At 2.5-5 GHz, the phase and amplitude tuning ranges of the I/Q divider/combiner were measured to be 80-100° and (+2)-(-1.1) dB, respectively. With the great performance of the tunable I/Q divider/combiner, the IRR of the up-/down-conversion image rejection module can reach a 50-dB level at 3-4.5 GHz and a 30-dB level at 2.5 and 5 GHz.

In chapter 4, a 24-32 GHz high image rejection ratio up-/down-conversion subharmonic mixer in 0.15 μm GaAs pHEMT process is proposed. The analysis and implementation of the 45° LO power divider is utilized to obtain small phase and amplitude imbalances with great isolation, and the quasi-lumped $\lambda_{LO}/4$ short/open stubs of the subharmonic mixer core are designed to have good isolation of 2LO-to-RF, LO-to-RF, and LO-to-IF. Besides, the effect of the LO inter-stage reflection coefficient on IRR is also discussed. With the tunable I/Q divider/combiner in measurement, the proposed mixer achieves about -11.3 dB conversion gain with a 1.3 dB variation for up-conversion and -11 dB with a 1.7 dB variation for down-conversion at 24-32 GHz. The IRR in precise phase and amplitude tuning can reach over 45.7 dB for up-conversion and 46.7 dB for down-conversion. Compared to the published wide-band I/Q mixers, this mixer shows outstanding IRR performance.

1.3 Thesis Organization

This thesis is organized as follows:

doi:10.6342/NTU202203942

Chapter 2 proposes a 24 GHz high conversion gain down-conversion active mixer using noise cancellation technique. The design flow will be introduced. The measured results and the analysis of the reduction in conversion gain will be discussed.

Chapter 3 proposes a millimeter-wave up-/down-conversion image rejection module. The ICs' selection of mixer doubler will be considered. The design methods and experimental results will be illustrated.

Chapter 4 proposes a 24-32 GHz high image rejection ratio up-/down-conversion subharmonic mixer for 5G communication. The design features and results will be demonstrated.

Chapter 5 gives the conclusion of this thesis.

doi:10.6342/NTU202203942

Chapter 2 A 24 GHz High Conversion Gain Down-Conversion Active Mixer Using Noise Cancellation Technique

2.1 Introduction

The rapid evolution of wireless communications has resulted in a strong drive toward building high-performance RF circuits in silicon, particularly CMOS, for its low cost and high level of integration. Recently, the increasing demands for wireless applications with high data rates at K band have received great attention. For example, 24 GHz industrial, scientific, and medical (ISM)-band radar sensors. They are adopted in consumer products for automation and interaction, such as smart appliances, intelligent energy control, or even the hands-free trunk and tailgate release on cars. The low-frequency band (24-24.25 GHz) of automotive radars is adopted in short/mid-range applications such as blind-spot detection, lane change assistance, rear cross-traffic alert, and collision avoidance.

Since the passive down-conversion mixers exhibit conversion loss degrading the overall receiver performances and require high LO power causing more power dissipation (LO buffer), active mixers with high conversion gain, good linearity, low noise figure, high port-to-port isolation, and low power consumption are particularly needed for 24 GHz CMOS receivers [1]-[9].

In previous literatures, a high conversion gain is greater than 10 dB [1]-[7] and a low noise figure is less than 16 dB [3]-[9]. To achieve the above standards, we attempted to use

doi:10.6342/NTU202203942

a double-balanced Gilbert cell as the architecture of the mixer core. It is widely used as the down-converter in CMOS receivers since it has high port-to-port isolation and is capable of adding a cross-coupled pair. The influence of noise on the circuit is considerably decreased with the addition of a parallel resonant inductor [10] and the current-bleeding technique composed of a cross-coupled pair [11], and the conversion gain is efficiently enhanced at the center frequency of 24.1 GHz.

2.2 Circuit Design of A 24 GHz High Conversion Gain Down-Conversion Active Mixer Using Noise Cancellation Technique

2.2.1 Concepts of The High Conversion Gain and Low Noise Down-Conversion Active Mixer

We use 0.18 μm CMOS as the process of the proposed high conversion gain and low noise down-conversion active mixer because of its low complexity and low-cost chip integration.

The transconductance (g_m) stage needs a large current to reach a high conversion gain, this compresses the output voltage headroom, which implies a smaller load resistor is allowable. However, a larger load resistor directly increases the conversion gain. To break the foregoing limitation, the current-bleeding technique effectively satisfies both DC requirements of the g_m stage and output stage. Furthermore, the current-bleeding technique drastically reduces the current flowing through the LO switches. This minimizes the height of the noise pulses, lowering the flicker noise of the LO switches [11].

doi:10.6342/NTU202203942

The configuration of the proposed high conversion gain and low noise down-conversion active mixer is shown in Fig. 2.1. Both the differential RF and LO signals are generated through the transformers. The mixer core is composed of blocks A, B, C, E and the resonant inductor L_{res}. Block A is the g_m stage that dominates the conversion gain of the mixer. Block B is a current-bleeding path made up of a cross-coupled pair and a current source (eight transistors in parallel). Block C is the switching stage for frequency converting. Block E is the load resistors on the output stage. Block D is a differential source follower buffer. The resonant inductor is employed to eliminate the parasitic capacitance from the g_m stage to the switching stage, reducing noise and improving conversion gain [10].

The frequency design goals are the RF frequency ranges from 24 to 24.25 GHz (ISM band), while the LO frequency is 24 GHz, and the IF frequency is 0.1 GHz. The conversion gain design goal is greater than 10 dB without IF combining. Conversion gain is calculated as IF+ or IF- minus RF in Fig. 2.1. The noise figure design goal is less than 10 dB when the frequency is greater than 1 GHz and is less than 40 dB at 1 kHz. The mixer core's DC power consumption is designed to be less than 5 mW when the supply voltage is 1.8 V (V_{DDm} and V_{DDb}).

doi:10.6342/NTU202203942

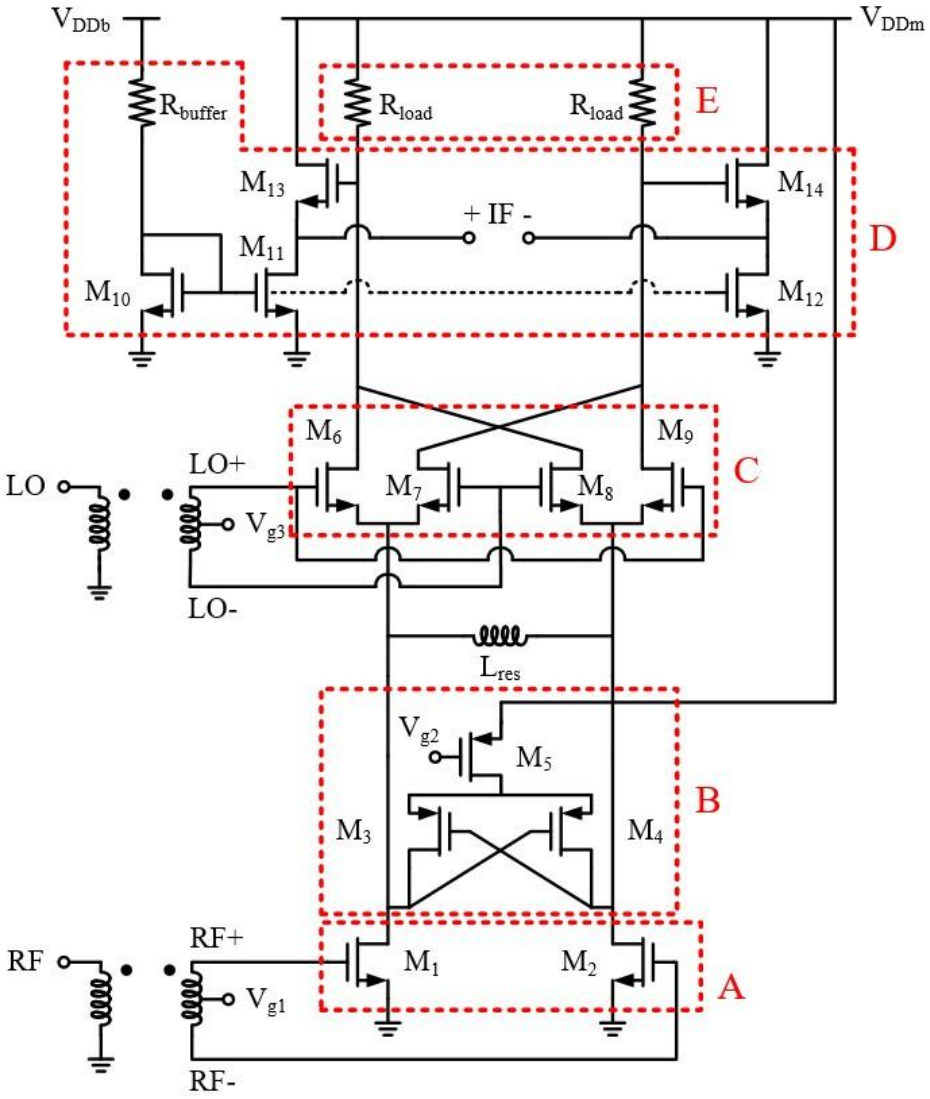


Fig. 2.1 Schematic of the proposed high conversion gain and low noise down-conversion active mixer.

doi:10.6342/NTU202203942

2.2.2 Current Distribution Ratio of The Current-Bleeding Path

We use the ideal current source (I_{CB}) to evaluate the current-bleeding path's current distribution ratio as shown in Fig. 2.2. Since the mixer core's DC power consumption is designed to be less than 5 mW when the supply voltage is 1.8 V, the current I_2 on each side of the differential paths is set to 1.35 mA. Current I_1 flows through R_{load} and LO switches and the combination of I_1 and I_{CB} is I_2. The g_m stage ($M_{1,2}$) and load resistors directly influence the conversion gain. We therefore simulate different current distribution ratios with fixed g_m stage and load resistors. The total width of $M_{1,2}$ is 28 μm for 1.35 mA and the resistance is assumed to be 1000 Ω for easier calculation.

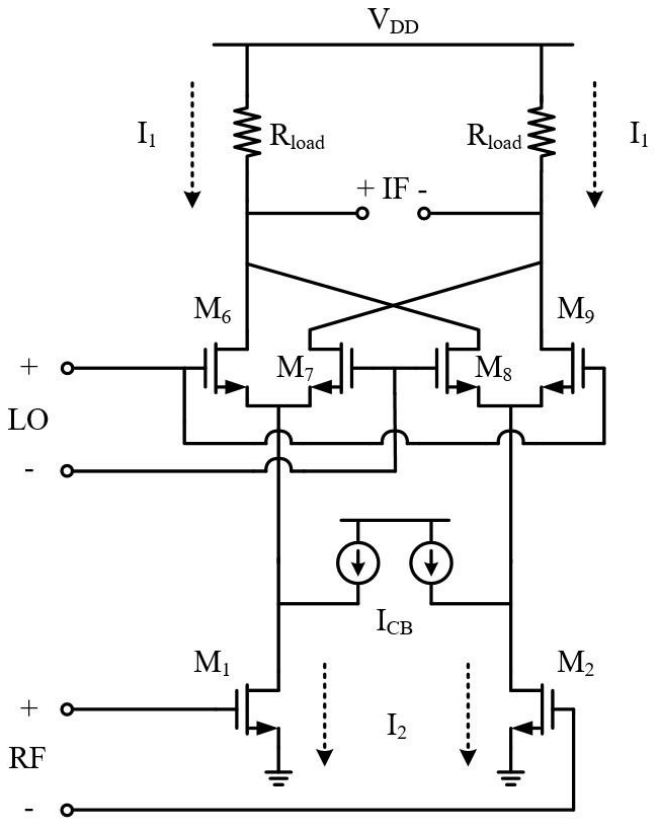


Fig. 2.2 Schematic of the mixer core with current-bleeding consideration.

doi:10.6342/NTU202203942

The simulated conversion gain vs. LO power in different current distribution ratios is shown in Fig. 2.3. When I_1: I_{CB} is 1:3, there is a maximum conversion gain of 4 dB with a 2 dBm LO power. The simulated noise figure vs. LO power in different current distribution ratios is shown in Fig. 2.4. The noise figure has a minimum of 50.4 dB when I_1: I_{CB} is 1:3 at 1 kHz and is about 12.7-12.9 dB when I_1: I_{CB} is 1:1, 1:2, 1:3, and 1:4. The corner frequencies are very close in these four ratios. The ratio of 1:3 has a relatively flat 1/f-slope, which means it has a relatively small flicker noise in low frequencies. Considering the above simulation results, we choose I_1: I_{CB} is 1:3 as the current distribution ratio of the current-bleeding path.

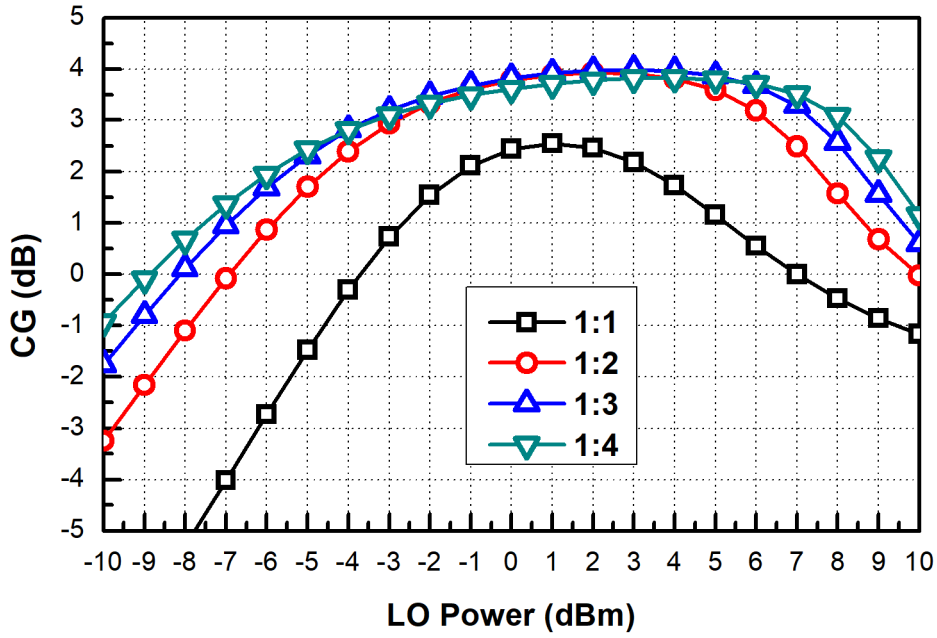


Fig. 2.3 Simulated conversion gain (CG) vs. LO power in different current distribution ratios (I_1: I_{CB}).

doi:10.6342/NTU202203942

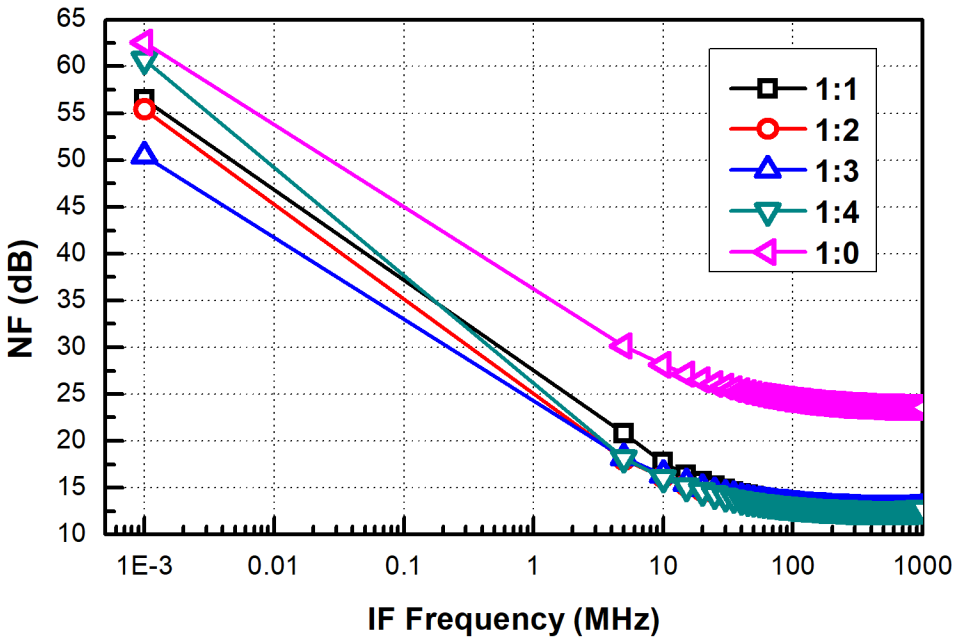


Fig. 2.4 Simulated noise figure (NF) in different current distribution ratios (I_1: I_{CB}).

2.2.3 Size Considerations of The Transistors

We simulate the IP_{1dB} in a 1:3 current distribution ratio as shown in Fig. 2.5. The -6 dBm power has about 160 mV voltage swing (V_{peak}). Since the threshold voltage of $M_{1,2}$ in Fig. 2.1 is about 0.53 V, we set the gate voltage to 0.7 V and the drain voltage to be about 0.6 V (one-third of the supply voltage) to ensure that the transistors are operating in the saturation region. Since the source, drain and gate resistance decrease when the number of fingers is increased, we choose 14 fingers with 2 μm width as the size of $M_{1,2}$ for 1.35 mA. The gm of $M_{1,2}$ is about 9.9 mS.

The current source M_5 in Fig. 2.1 has eight transistors in parallel, and each of them is 20 fingers with 4 μm width for 2 mA. This size is chosen to have proper layout space as shown in the next section. The size of the cross-coupled pair $M_{3,4}$ in Fig. 2.1 is 10 fingers

doi:10.6342/NTU202203942

with 2 μm width for 1 mA. We set the gate voltage of M_5 to 1.2 V and the source voltage of $M_{3,4}$ to be about 1.6 V to ensure that the transistors are operating in the saturation region.

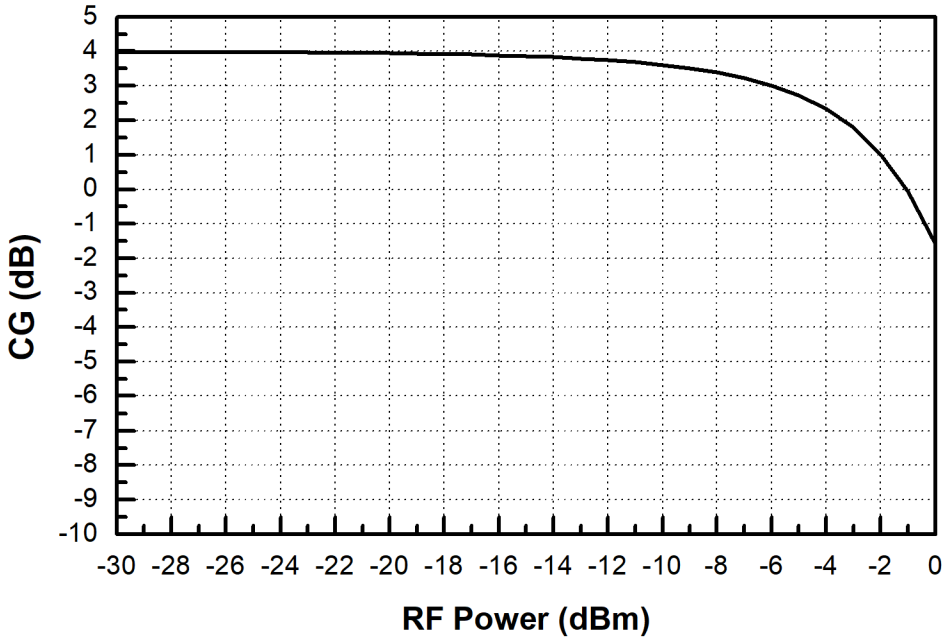


Fig. 2.5 Simulated IP_{1dB} in 1:3 current distribution ratio.

The size of the LO switch $M_{6,7,8,9}$ in Fig. 2.1 is 4 fingers with 1.5 μm width for 175 μA. To have a 0.6 V (one-third of the supply voltage) headroom, the load resistance was changed to 1714 Ω. As shown in Fig. 2.6, it has a maximum conversion gain of -0.91 dB with a -2 dBm LO power when the ideal current source on the current-bleeding path is replaced with $M_{3,4,5}$. We set the gate voltage of $M_{6,7,8,9}$ to 1.3 V to ensure that the transistors are operating in the saturation region.

doi:10.6342/NTU202203942

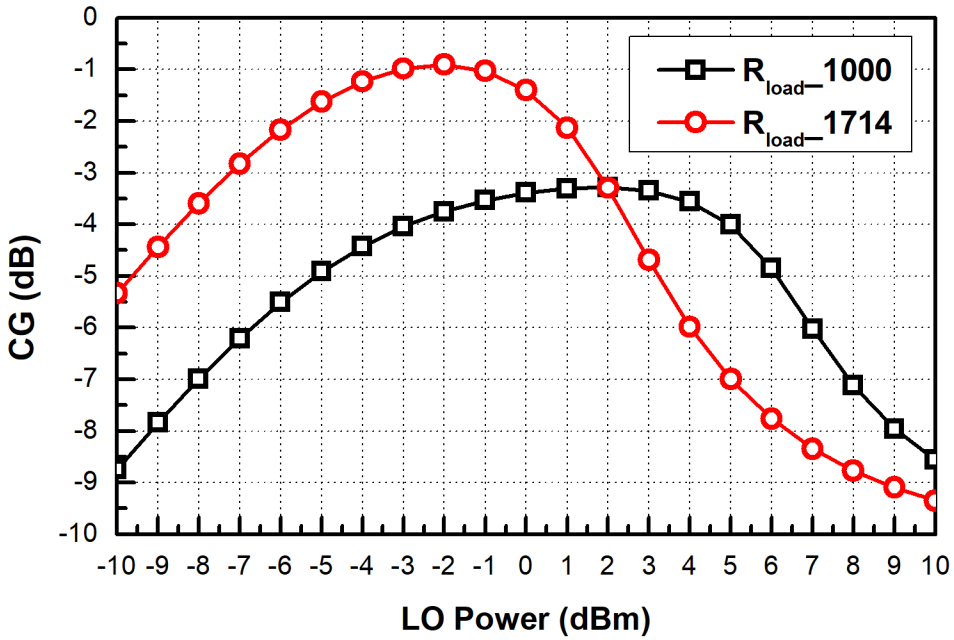


Fig. 2.6 Simulated conversion gain (CG) vs. LO power in different load resistances.

doi:10.6342/NTU202203942

2.2.4 The Resonant Inductor and RF/LO Transformers

We simulate the conversion gain vs. LO power within/out the ideal resonant inductor L_{res} (Q factor is set to 20) in Fig. 2.1 as shown in Fig. 2.7. It has a maximum conversion gain of 11.9 dB with a 0 dBm LO power. After designing the RF/LO transformers, the EM simulation will be considered for a more accurate inductance.

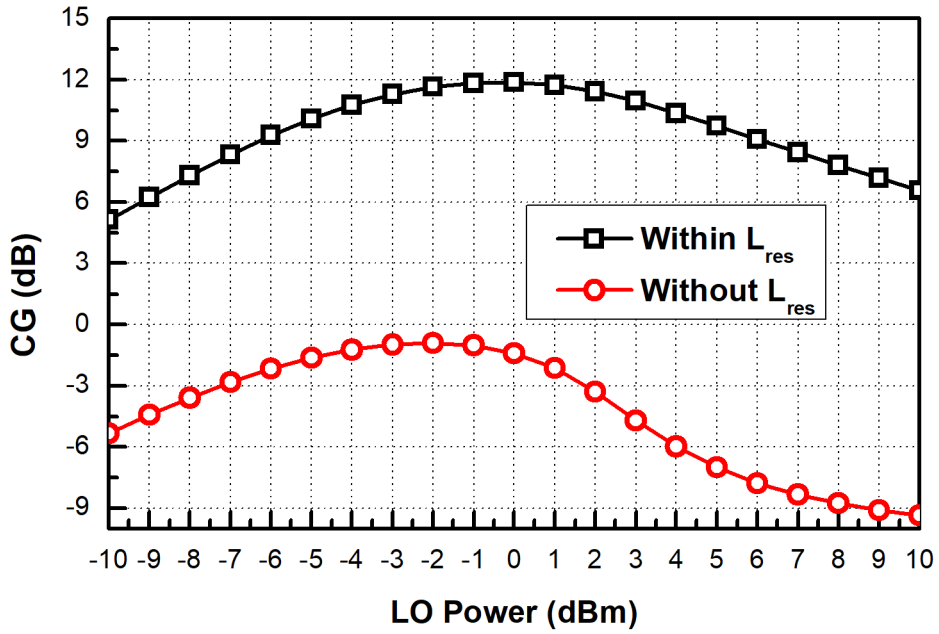


Fig. 2.7 Simulated conversion gain (CG) vs. LO power within/out the resonant inductor.

I. RF Transformer

The schematic of the RF transformer is shown in Fig. 2.8. It is composed of two mutual inductors and two identical capacitors for impedance transforming. Z_{inRF} is the impedance from $M_{1,2}$ in Fig. 2.1 to the mixer core, and it is 100*(0.44- j1.4) at 24.1 GHz. The layout of the RF transformer is shown in Fig. 2.9. Length A is 222 μm and length B is 204 μm. The values of $L_{RF1,2}$, C_{RF} and the coupling coefficient K between these two inductors are shown in Table 2.1.

doi:10.6342/NTU202203942

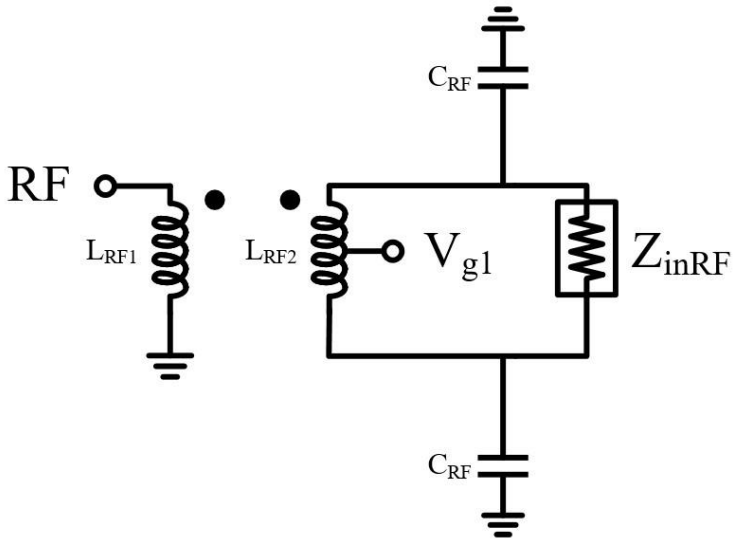


Fig. 2.8 Schematic of the RF transformer.

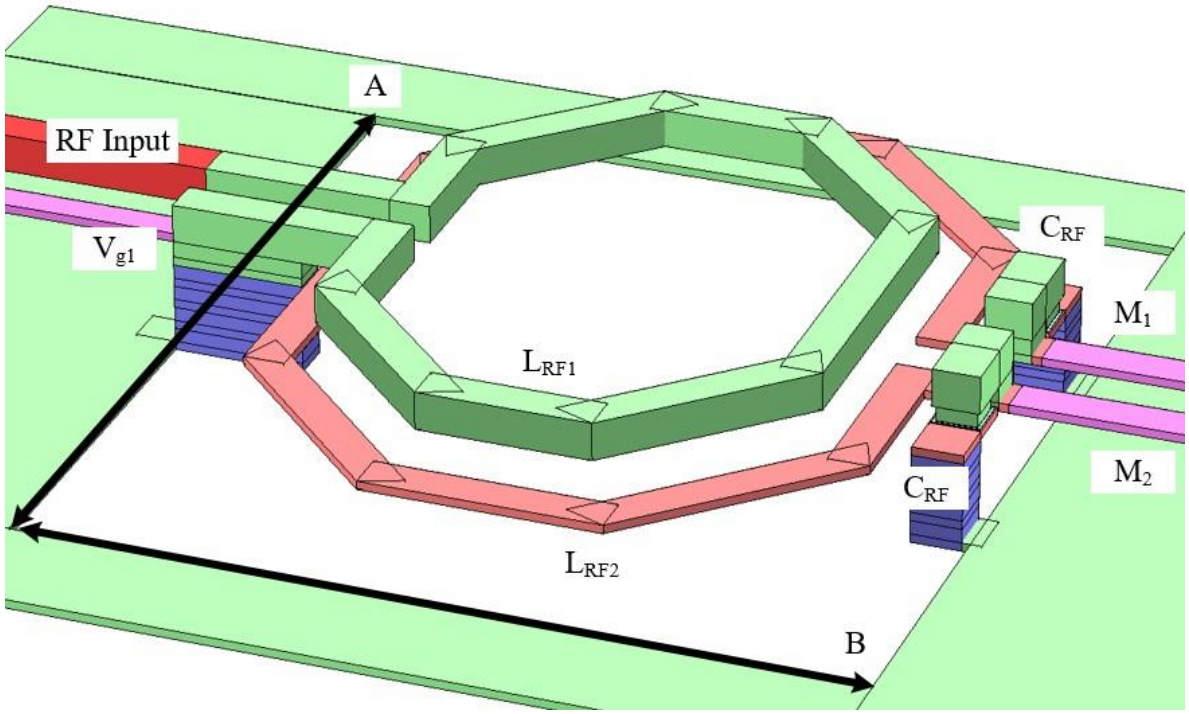


Fig. 2.9 Layout of the RF transformer.

doi:10.6342/NTU202203942

Table 2.1 Values of $L_{RF1,2}$, C_{RF} and coupling coefficient K.

Each Element	Value (at 24.1 GHz)	Q Factor
L_{RF1}	321.7 pH	13.8
L_{RF2}	370.3 pH	7.9
C_{RF}	158.6 fF	
K	0.42	

II. LO Transformer

The schematic of the LO transformer is shown in Fig. 2.10. It is composed of two mutual inductors and two identical capacitors for impedance transforming. Z_{inLO} is the impedance from $M_{6,7,8,9}$ in Fig. 2.1 to the mixer core, and it is 100*(1.374- j6.432) at 24 GHz. The layout of the LO transformer is shown in Fig. 2.11. Length C is 180 μm and length D is 250 μm. The values of $L_{LO1,2}$, C_{LO}, R_{LO} and the coupling coefficient K between these two inductors are shown in Table 2.2.

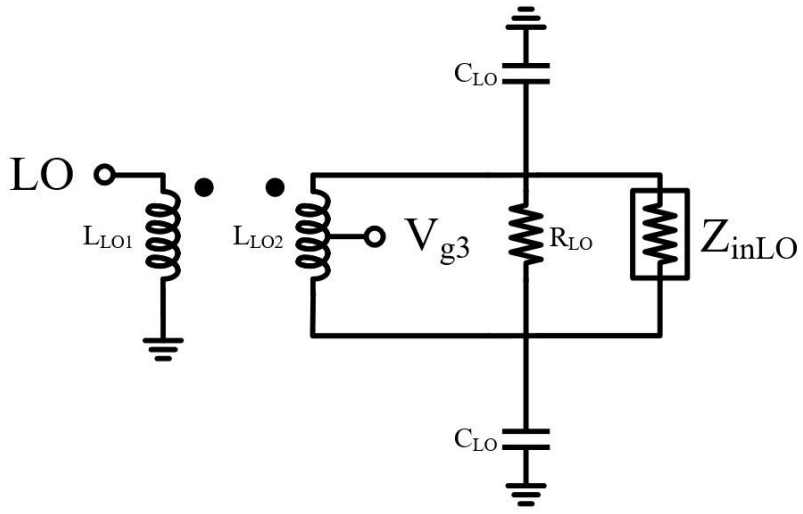


Fig. 2.10 Schematic of the LO transformer.

doi:10.6342/NTU202203942

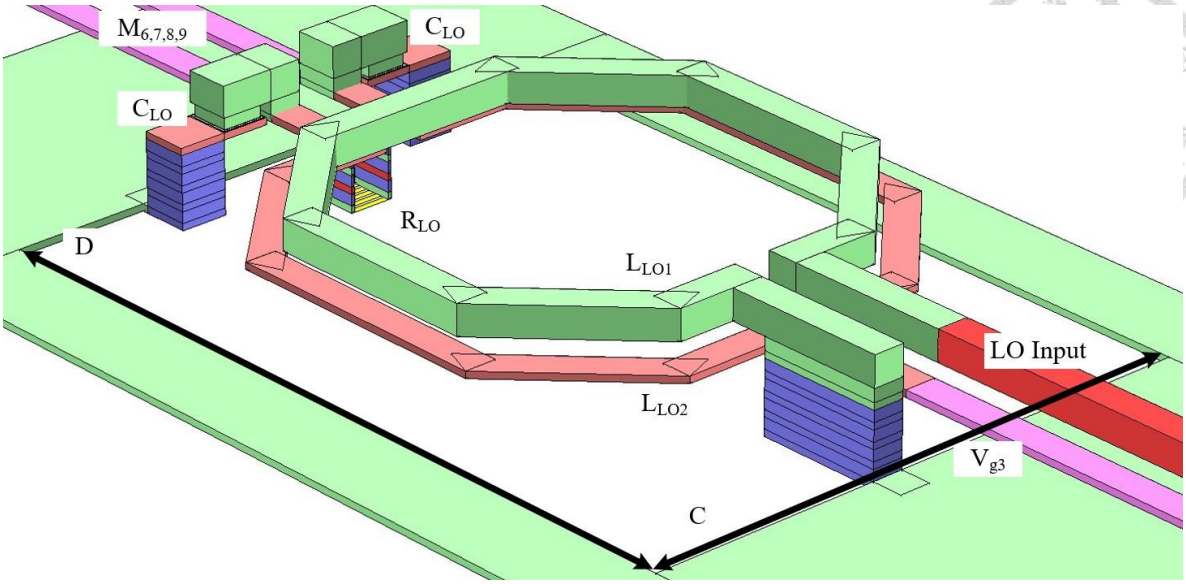


Fig. 2.11 Layout of the LO transformer.

Table 2.2 Values of $L_{LO1,2}$, C_{LO}, R_{LO} and coupling coefficient K.

Each Element	Value (at 24 GHz)	Q Factor
L_{LO1}	398.3 pH	9.8
L_{LO2}	408 pH	7.6
C_{LO}	249.3 fF	
R_{LO}	360 Ω	
K	0.66	

III. Resonant Inductor

The layout of the RF/LO differential paths is shown in Fig. 2.12. With the consideration of the EM simulations of RF/LO transformers and the RF/LO differential paths, we can obtain the optimum resonant inductor. The layout of the resonant inductor is shown in Fig. 2.13. Length E and F are both 160 μm. At 24.1 GHz, L_{res} has a 399.2 pH with a 21.8 Q factor.

doi:10.6342/NTU202203942

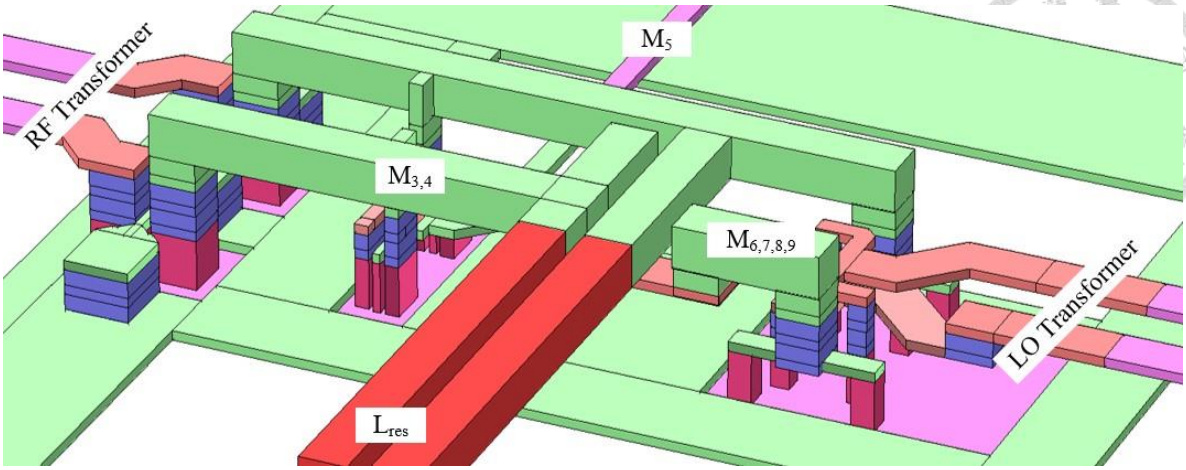


Fig. 2.12 Layout of the RF/LO differential paths.

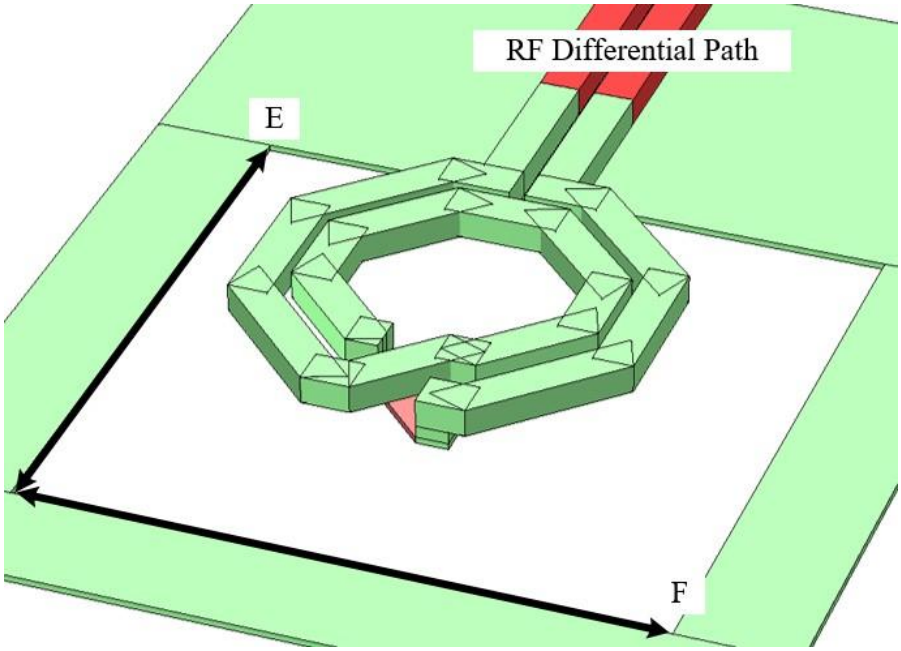


Fig. 2.13 Layout of the resonant inductor.

2.2.5 The IF Buffer

We use the source follower as the configuration of the IF buffer as shown in Fig. 2.14. To measure the expected high conversion gain, the source follower needs a large current. The size of M_{10} is 10 fingers with 8 μm width for 1.58 mA and R_{buffer} is 700 Ω. The size of

doi:10.6342/NTU202203942

$M_{11,12,13,14}$ is 54 fingers with 8 μm width for 20.9 mA. The voltage gain is about 0.84 (-1.536 dB) at 0.1 GHz as shown in Fig. 2.15.

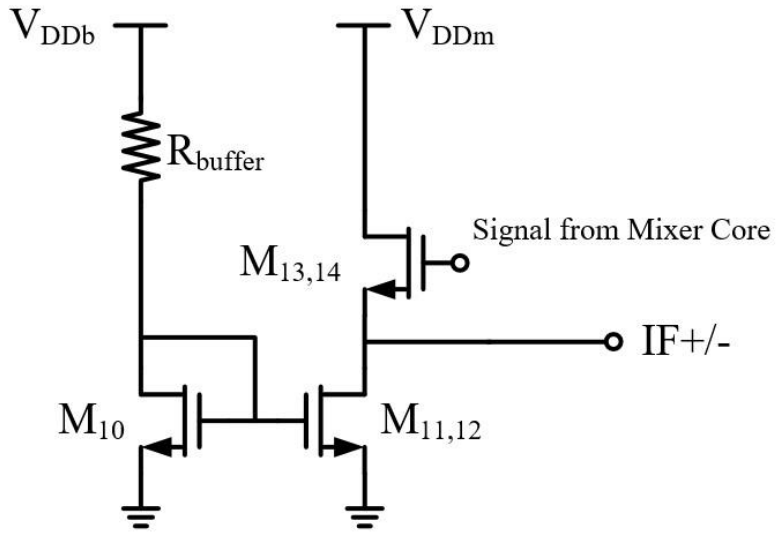


Fig. 2.14 Schematic of the IF buffer.

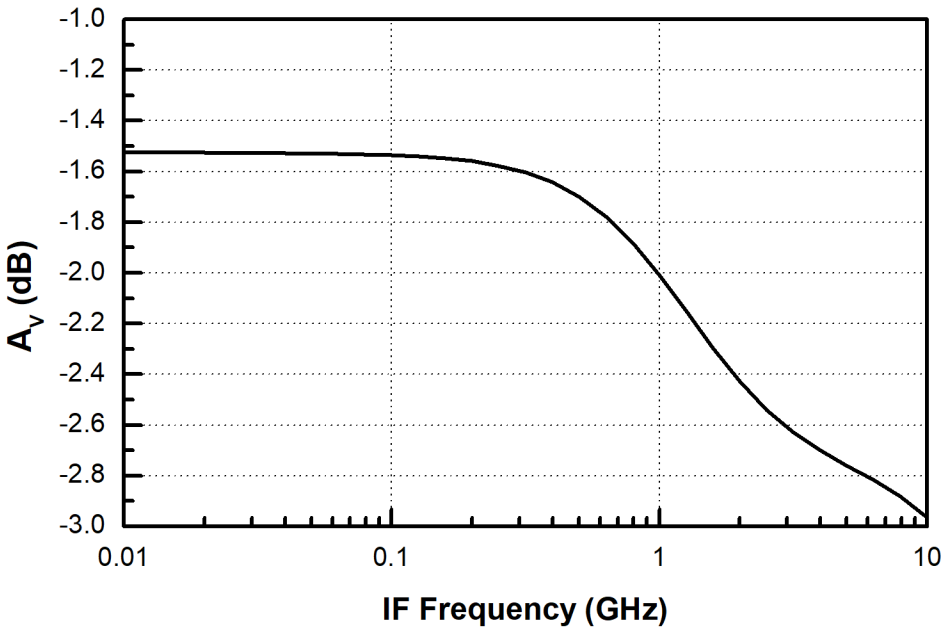


Fig. 2.15 Simulated voltage gain (A_V) of the source follower.

doi:10.6342/NTU202203942

2.2.6 Simulations of The High Conversion Gain and Low Noise Down-Conversion Active Mixer

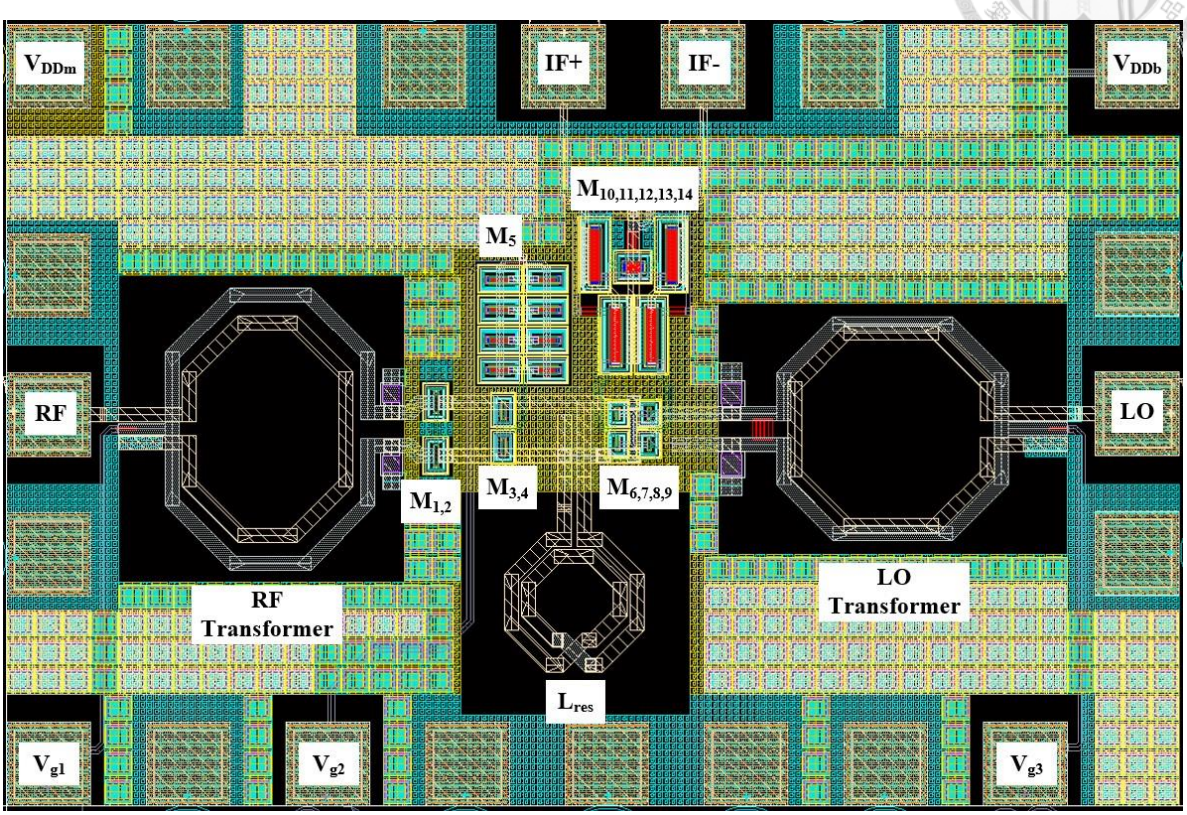


Fig. 2.16 Layout of the high conversion gain and low noise down-conversion active mixer.

The layout of the high conversion gain and low noise down-conversion active mixer is shown in Fig. 2.16. The chip size is 840*560 μm^2.

The simulated conversion gain vs. LO power of the high conversion gain and low noise down-conversion active mixer is shown in Fig. 2.17 when RF frequency is 24.1 GHz, LO frequency is 24 GHz, and IF frequency is 0.1 GHz. Conversion gain is calculated as IF+ or IF- minus RF in Fig. 2.1. It has a 12.8 dB conversion gain with a 2 dBm LO power.

doi:10.6342/NTU202203942

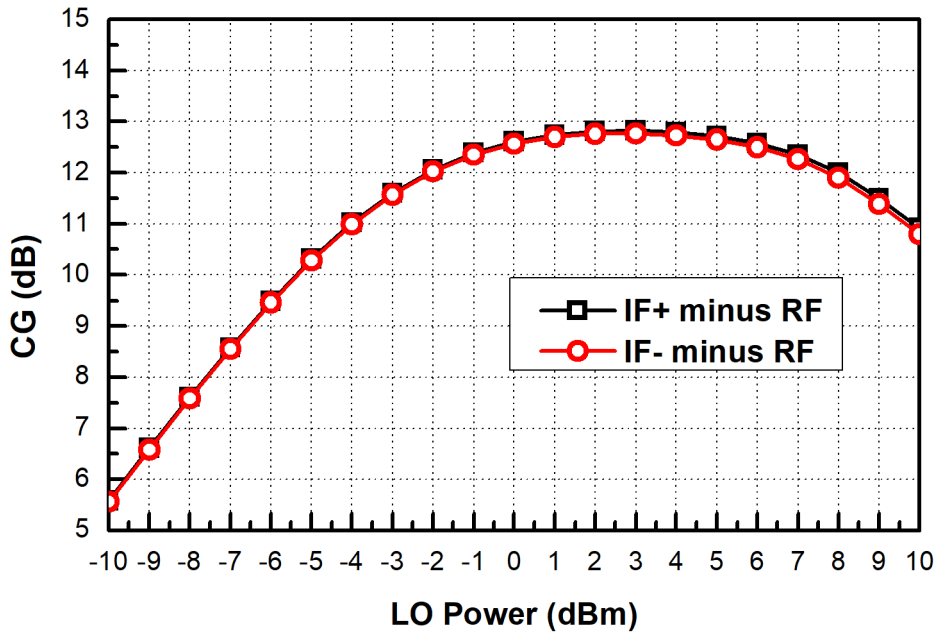


Fig. 2.17 Simulated conversion gain (CG) vs. LO power of the high conversion gain and low noise down-conversion active mixer.

The simulated IP_{1dB} of the high conversion gain and low noise down-conversion active mixer is shown in Fig. 2.18 when RF frequency is 24.1 GHz, LO frequency is 24 GHz, IF frequency is 0.1 GHz, and LO power is 2 dBm. The IP_{1dB} is -15 dBm and OP_{1dB} is about -0.2 dBm with ideal IF combining.

The simulated bandwidth of the high conversion gain and low noise down-conversion active mixer is shown in Fig. 2.19 when IF frequency is 0.1 GHz and LO power is 2 dBm. The 3-dB bandwidth is about 23.1-25.2 GHz. The ISM band (24-24.25 GHz) has a conversion gain range of 12.6-12.8 dB.

doi:10.6342/NTU202203942

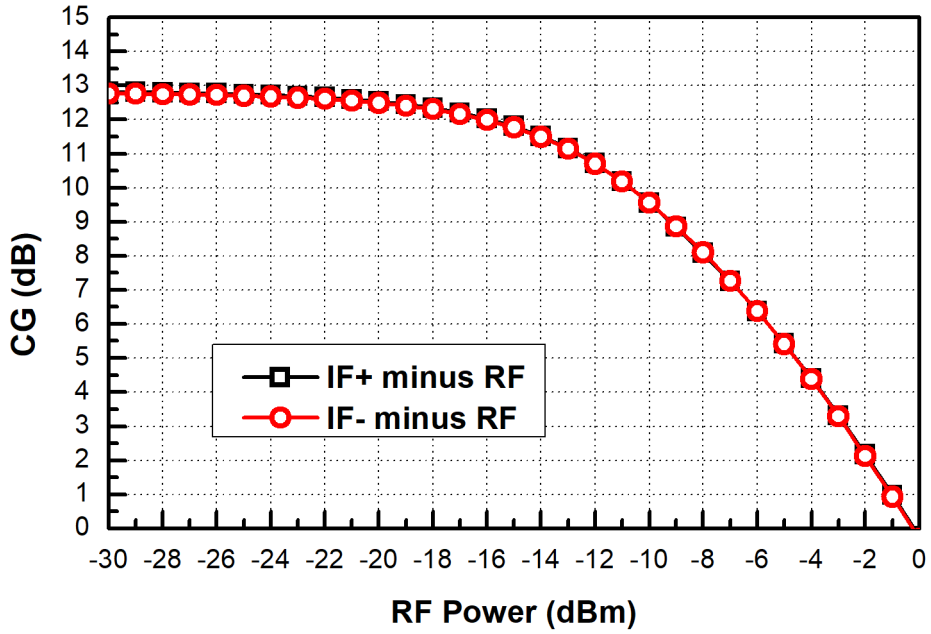


Fig. 2.18 Simulated IP_{1dB} of the high conversion gain and low noise down-conversion active mixer.

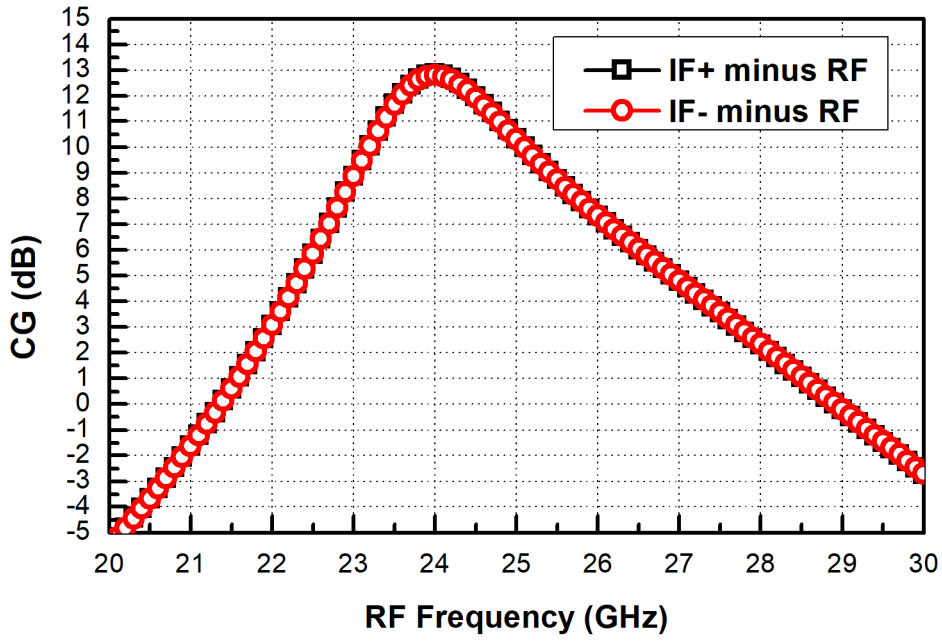


Fig. 2.19 Simulated bandwidth of the high conversion gain and low noise down-conversion active mixer.

doi:10.6342/NTU202203942

The simulated noise figure of the high conversion gain and low noise down-conversion active mixer is shown in Fig. 2.20. It is 34.7 dB at 1 kHz and 9.8 dB at 1 GHz. The corner frequency is about 1 MHz.

The simulated RF/LO reflection coefficients of the high conversion gain and low noise down-conversion active mixer are shown in Fig. 2.21. The RF reflection coefficient has a minimum of -28.1 dB at 24.1 GHz and is less than -10 dB from 23.7-24.6 GHz. The LO reflection coefficient has a minimum of -23.2 dB at 24 GHz and is less than -10 dB from 21.5-27.6 GHz.

The simulated isolations of the high conversion gain and low noise down-conversion active mixer are shown in Fig. 2.22. There are about -60 dB and -73 dB of LO-to-RF and RF-to-LO isolations at 24-24.1 GHz.

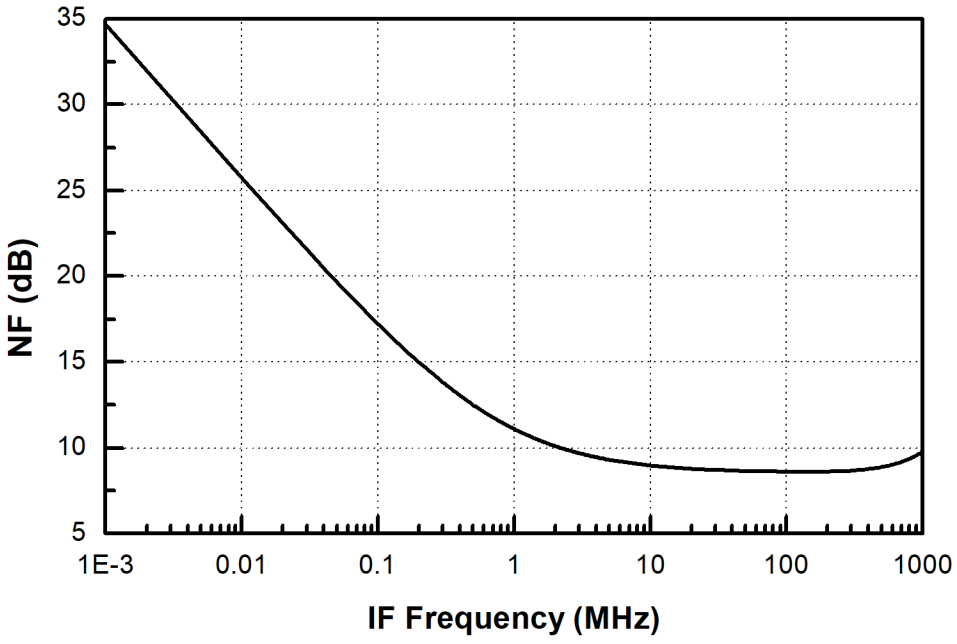


Fig. 2.20 Simulated noise figure (NF) of the high conversion gain and low noise down-conversion active mixer.

doi:10.6342/NTU202203942

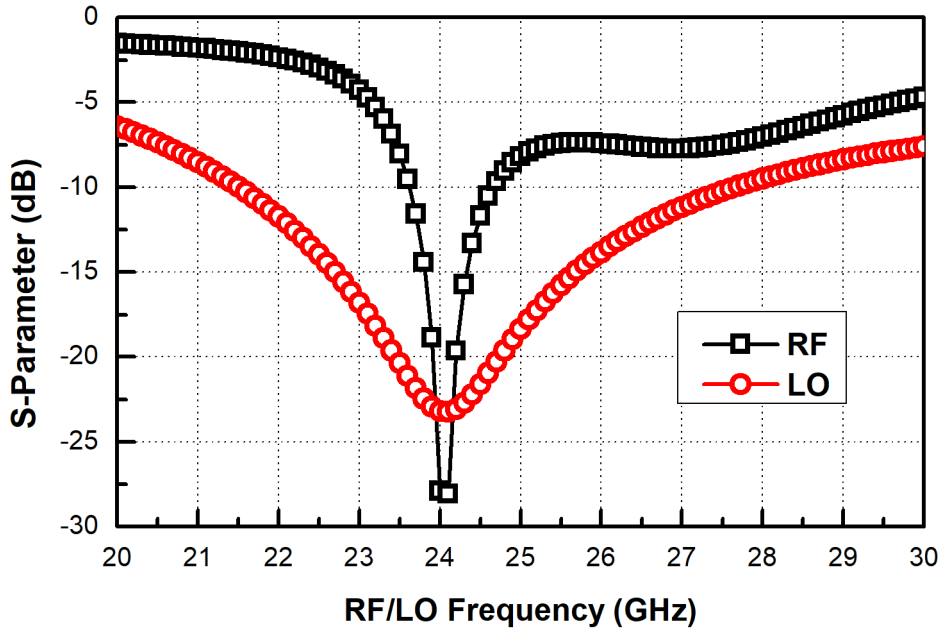


Fig. 2.21 Simulated RF/LO reflection coefficients of the high conversion gain and low noise down-conversion active mixer.

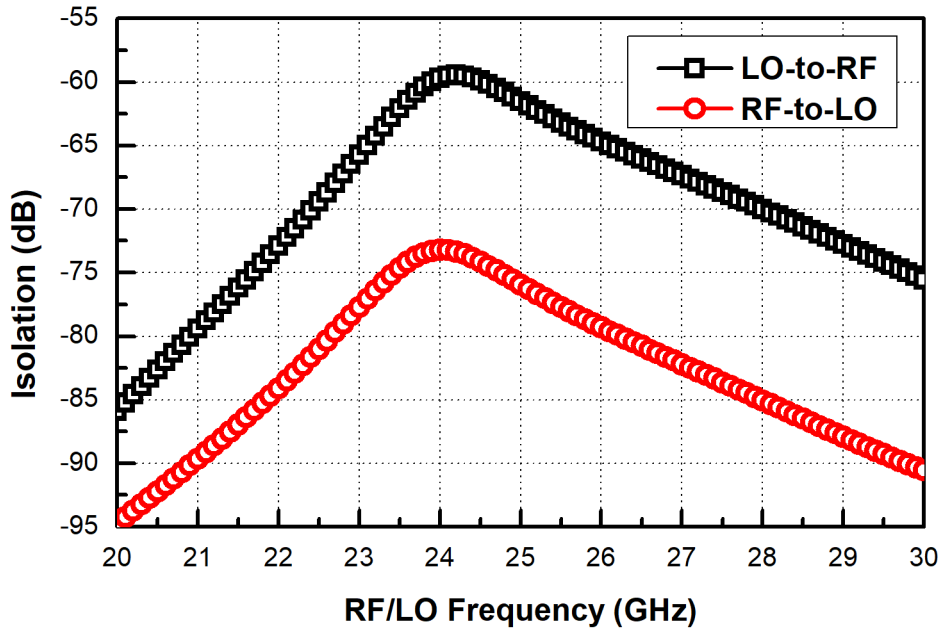


Fig. 2.22 Simulated isolations of the high conversion gain and low noise down-conversion active mixer.

doi:10.6342/NTU202203942

2.3 Experimental Results and Discussions

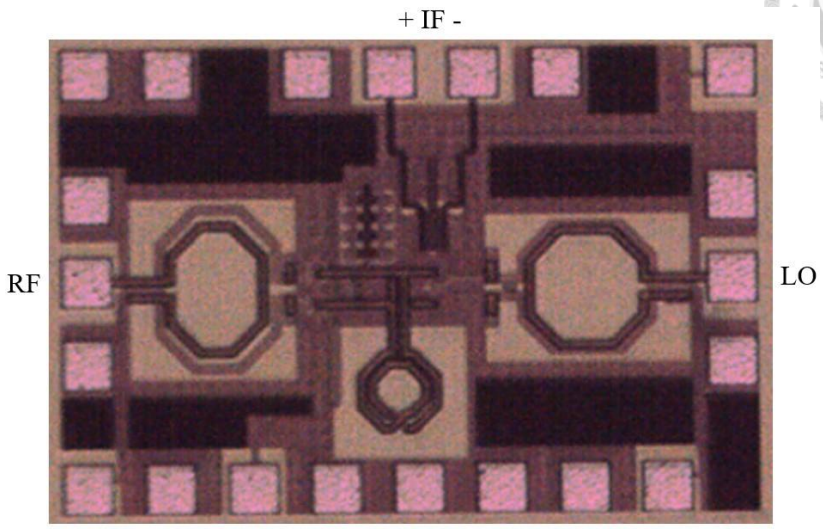


Fig. 2.23 Chip photo of the high conversion gain and low noise down-conversion active mixer.

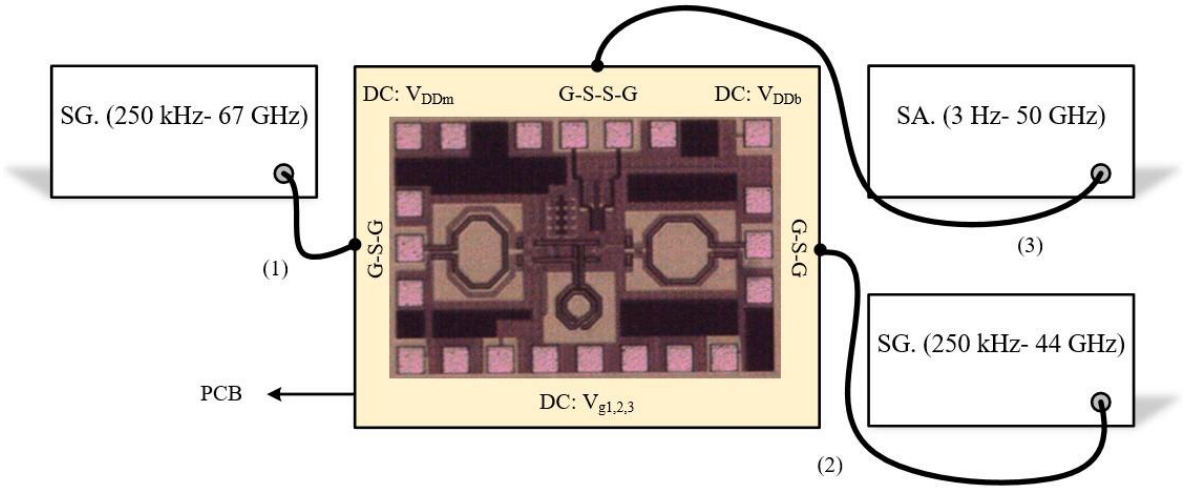


Fig. 2.24 Setup of measurement.

The chip photo is shown in Fig. 2.23. We use an Agilent E8257D (250 kHz- 67 GHz) signal generator for RF signal, a KEYSIGHT E8267D (250 kHz- 44 GHz) signal generator for LO signal, an Agilent E4448A (3 Hz- 50 GHz) spectrum analyzer to measure large signals (IF output power), a GWINSTEK PST-3202 (32 V,2 A x2/6 V, 5 A x1) power supply ($V_{g1,2,3}$)

doi:10.6342/NTU202203942

and a KEYSIGHT E36311A (6 V, 5 A/±25 V, 1 A) power supply ($V_{DDm,b}$) for DC supplying. The measurement setup is shown in Fig. 2.24. Cable 1 (1.85 mm) connects the probe on the LO side to the signal generator. Cables 2 (1.85 mm) connects the probe on the LO side to the signal generator. Cable 3 (2.4 mm) connects the probe on the IF side to the spectrum analyzer. One signal port of the G-S-S-G probe connects to a 50 Ω termination.

The conversion gain vs. LO power measurement of the 1st and 2nd tape-outs and EM simulation of the high conversion gain and low noise down-conversion active mixer as shown in Fig. 2.25 when RF frequency is 24.1 GHz, LO frequency is 24 GHz, and IF frequency is 0.1 GHz. The conversion gain of the two tape-out measurements degrades from the simulation by over 8 dB. The measured IP_{1dB} and bandwidth results are likewise significantly worse than the simulations, as shown in Fig. 2.26 and Fig. 2.27, respectively.

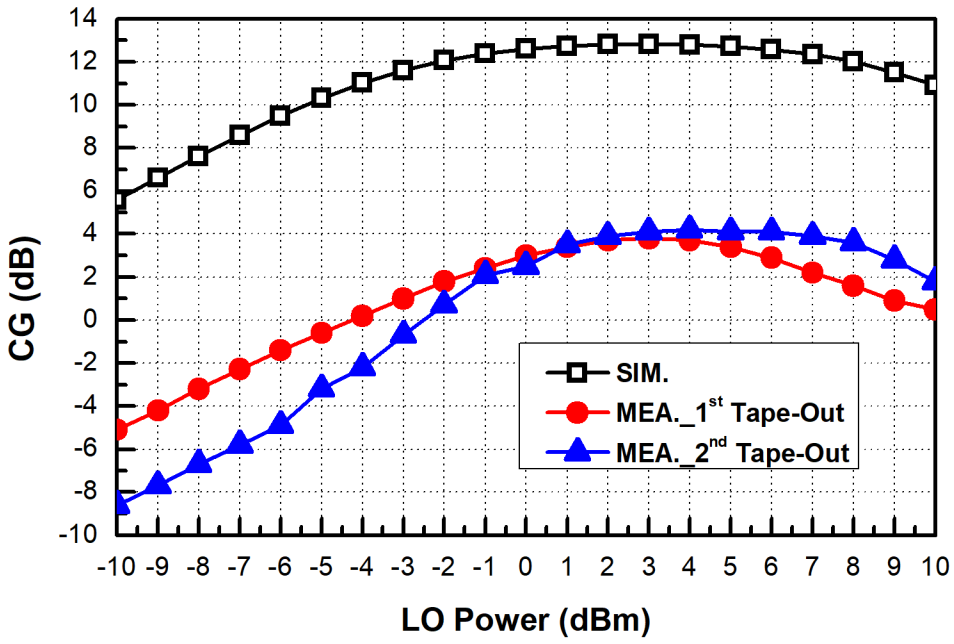


Fig. 2.25 Conversion gain (CG) vs. LO power measurement (1st and 2nd tape-outs) and EM simulation of the high conversion gain and low noise down-conversion active mixer.

doi:10.6342/NTU202203942

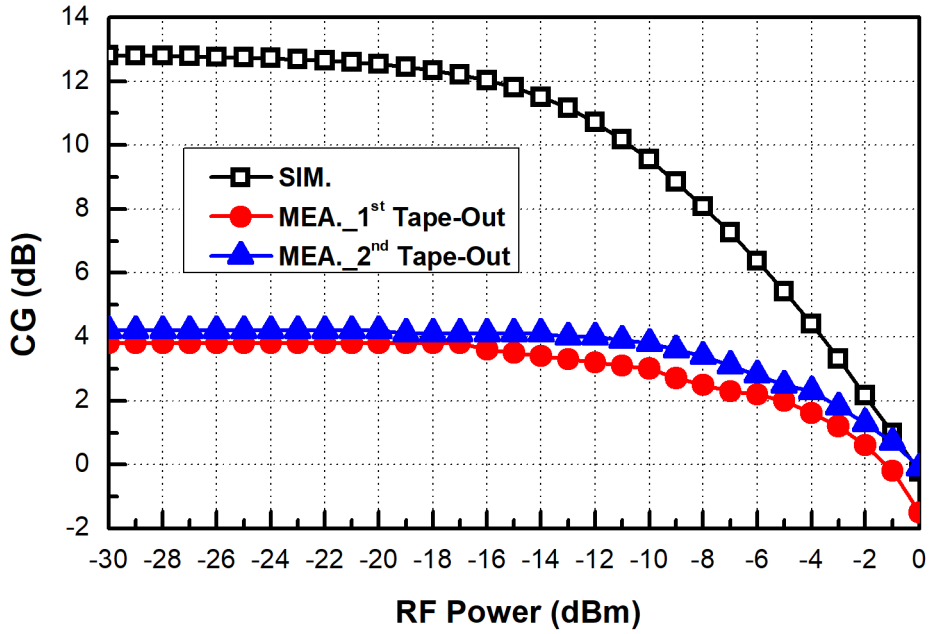


Fig. 2.26 IP_{1dB} measurement (1st and 2nd tape-outs) and EM simulation of the high conversion gain and low noise down-conversion active mixer.

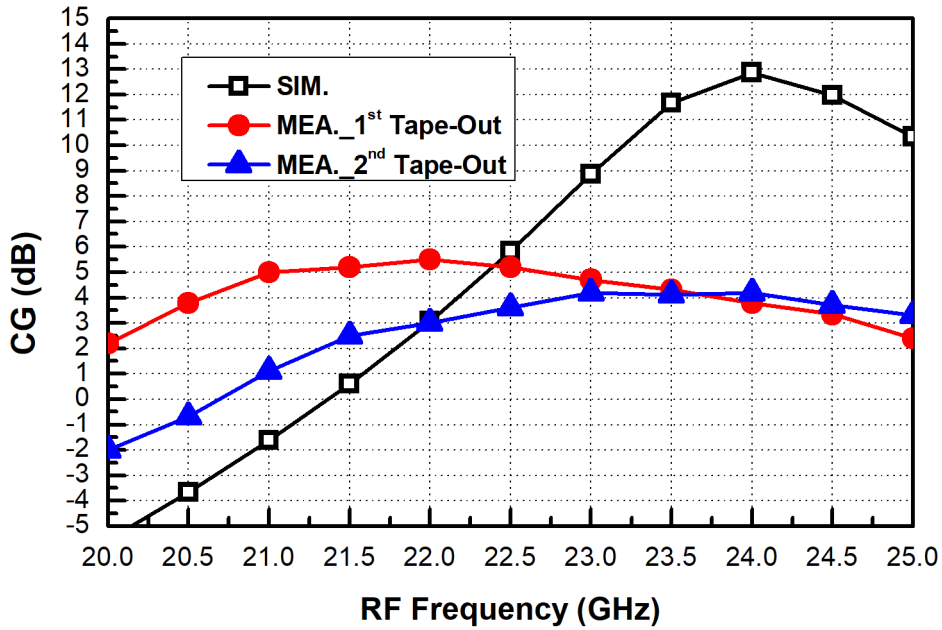


Fig. 2.27 Bandwidth measurement (1st and 2nd tape-outs) and EM simulation of the high conversion gain and low noise down-conversion active mixer.

doi:10.6342/NTU202203942

We look into the reasons for the reduction in conversion gain from the measurements and EM simulations of the 1st tape-out. The layout of the high conversion gain and low noise down-conversion active mixer is shown in Fig. 2.28. The measurement setup is the same in Fig. 2.24. In the 1st tape-out, we only consider the individual EM simulations of RF/LO transformers, RF/LO differential paths, and the resonant inductor. Since we don't have the EM simulation of the entire circuit, we run the EM simulation again and added a precise simulation of the transistor's three terminals (drain, gate, and source). The simulated conversion gain vs. LO power in the 1st tape-out with different conditions is shown in Fig. 2.29. Condition 1 considers the EM simulation of the entire circuit in Fig. 2.30. Condition 2 considers the EM simulation of the RF transformer, RF/LO differential paths, and resonant inductor in Fig. 2.31. Condition 3 considers the EM simulation of the transistors of the g_m stage in Fig. 2.32. The EM simulation of the entire circuit shows evidence of the reduction in conversion gain. The explanations for these three conditions are that the RF transformer is too close to the resonant inductor, and the incomplete grounding effect causes the source degeneration of the g_m stage.

doi:10.6342/NTU202203942

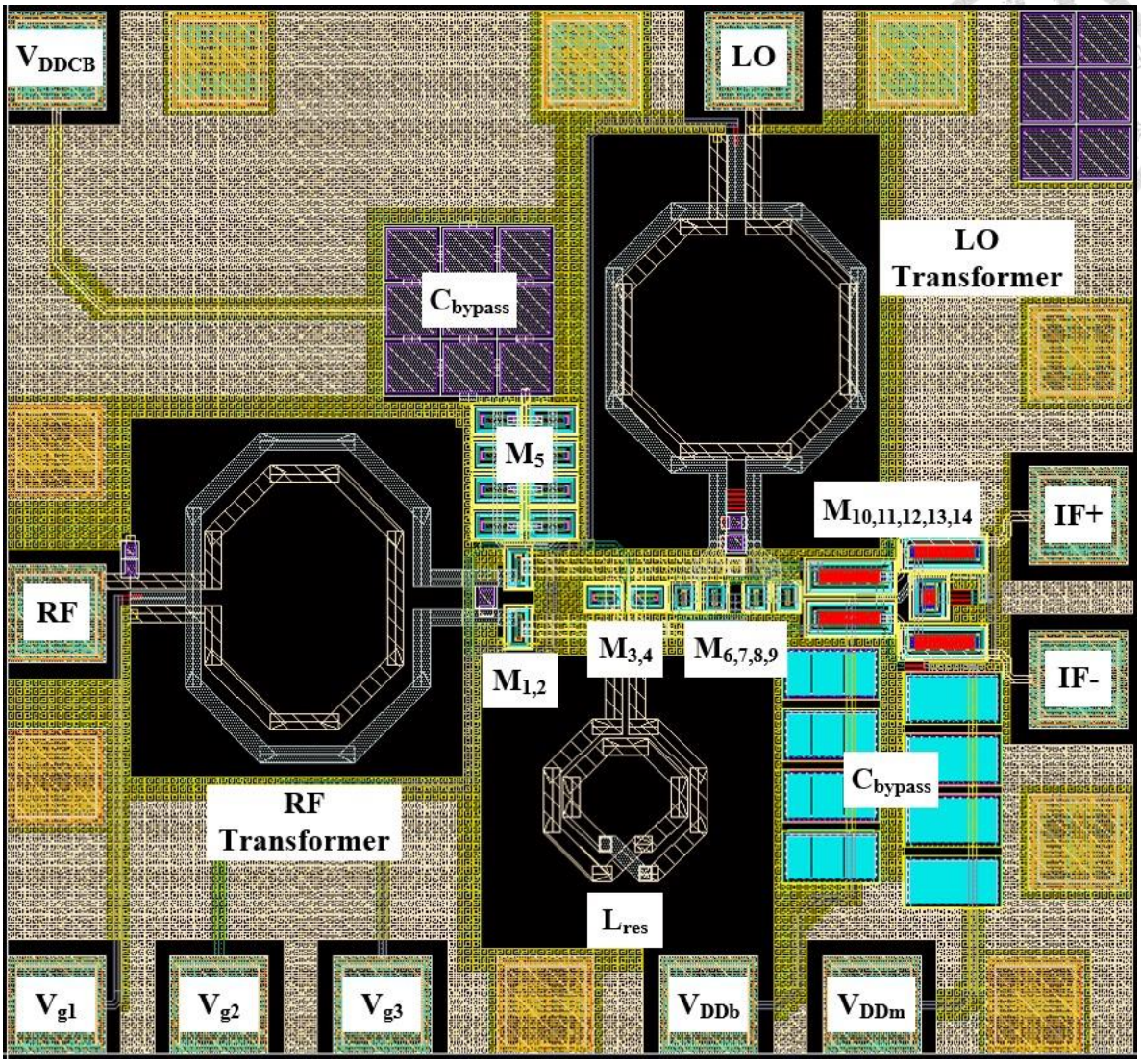


Fig. 2.28 Layout of the high conversion gain and low noise down-conversion active mixer in the 1st tape-out.

doi:10.6342/NTU202203942

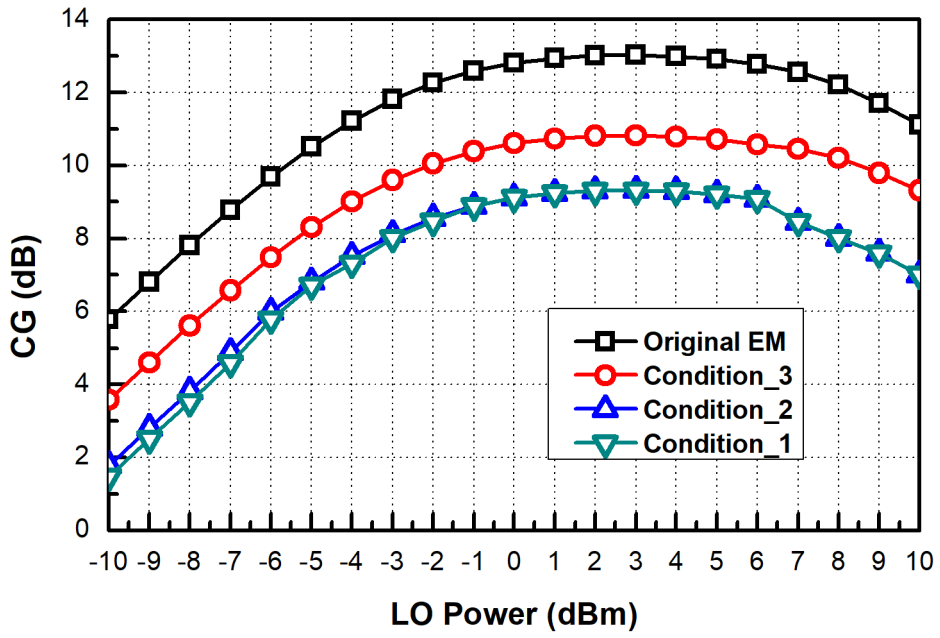


Fig. 2.29 Simulated conversion gain (CG) vs. LO power in the 1st tape-out with different conditions.

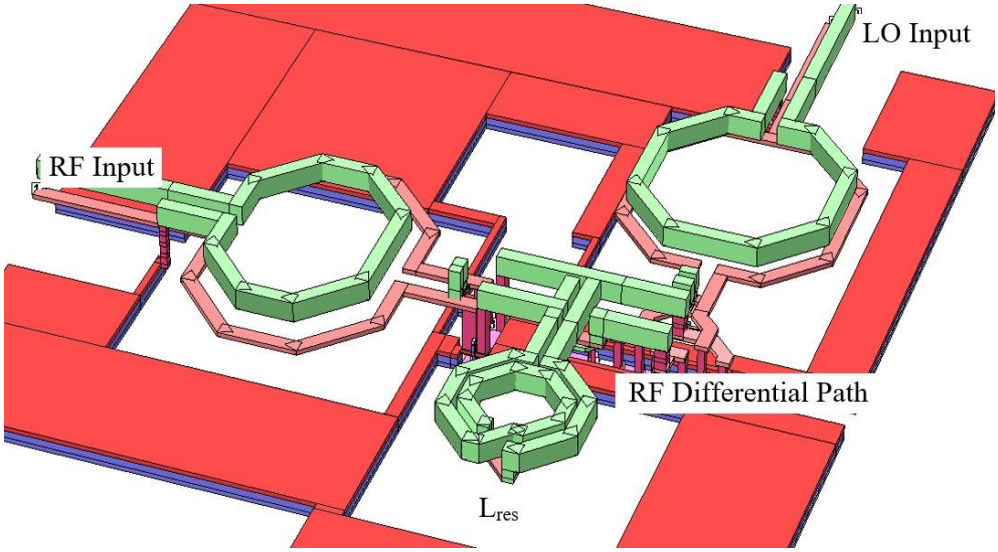


Fig. 2.30 Layout of the entire circuit in the 1st tape-out.

doi:10.6342/NTU202203942

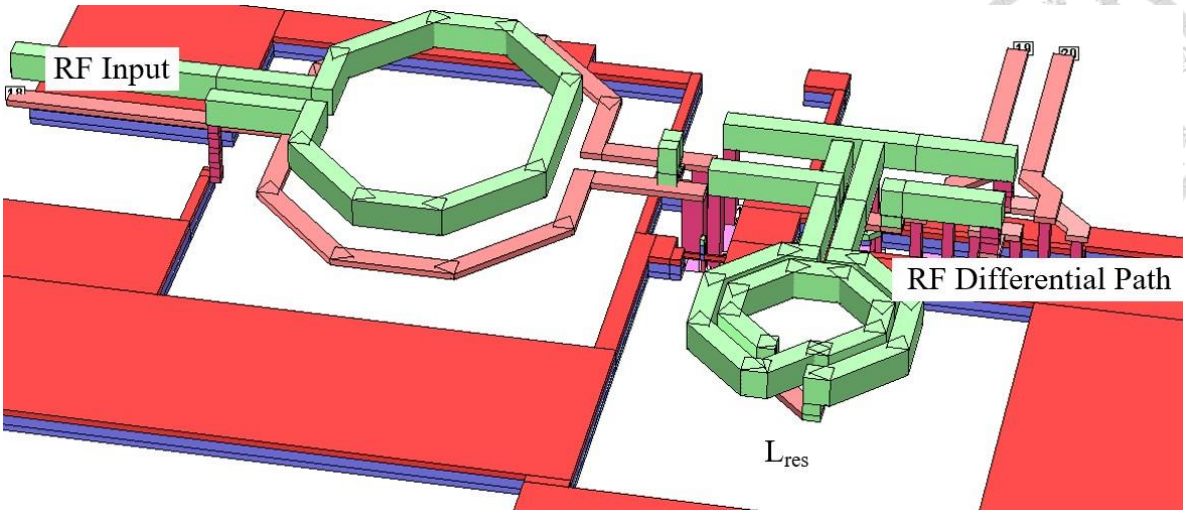


Fig. 2.31 Layout of the RF transformer, RF/LO differential paths, and resonant inductor in the 1st tape-out.

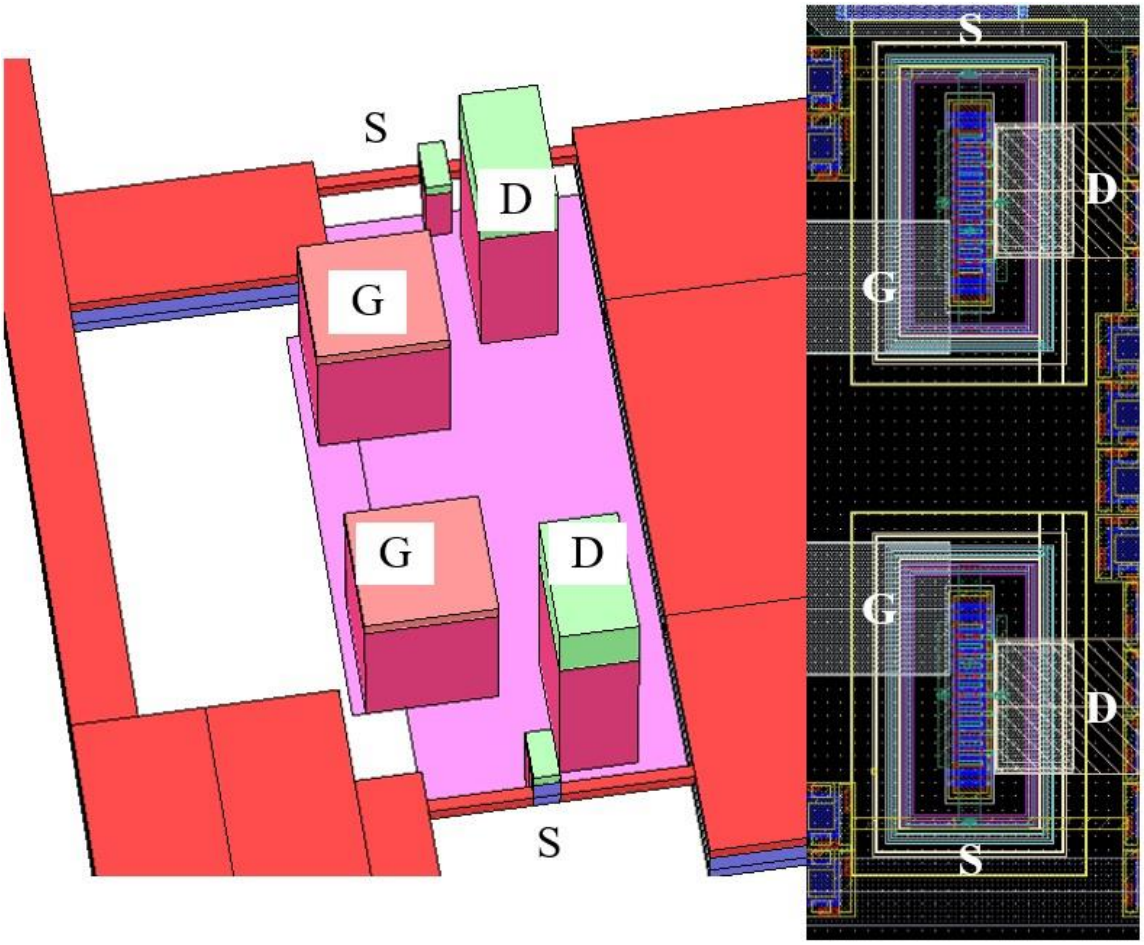


Fig. 2.32 Layout of the transistors of the g_m stage in the 1st tape-out.

doi:10.6342/NTU202203942

In addition, we discovered a large signal near 91 MHz in the spectrum as shown in Fig. 2.33. This signal cannot be suppressed by the off-chip bypass capacitors and occurs when the power supply is turned on.

We conclude from the EM re-simulations and the spectrum data that these are the reasons for the severe reduction in conversion gain. To improve these problems, we have modified the grounding condition of the g_m stage as shown in Fig. 2.34, and the available space on the layout filled with MOS-capacitors has achieved a good bypass function as shown in Fig. 2.35. The bypass capacitance is increased by about 88 pF compared to the 1st tape-out (12 to 100 pF). The modified layout of the 2nd tape-out is shown in Fig. 2.16.

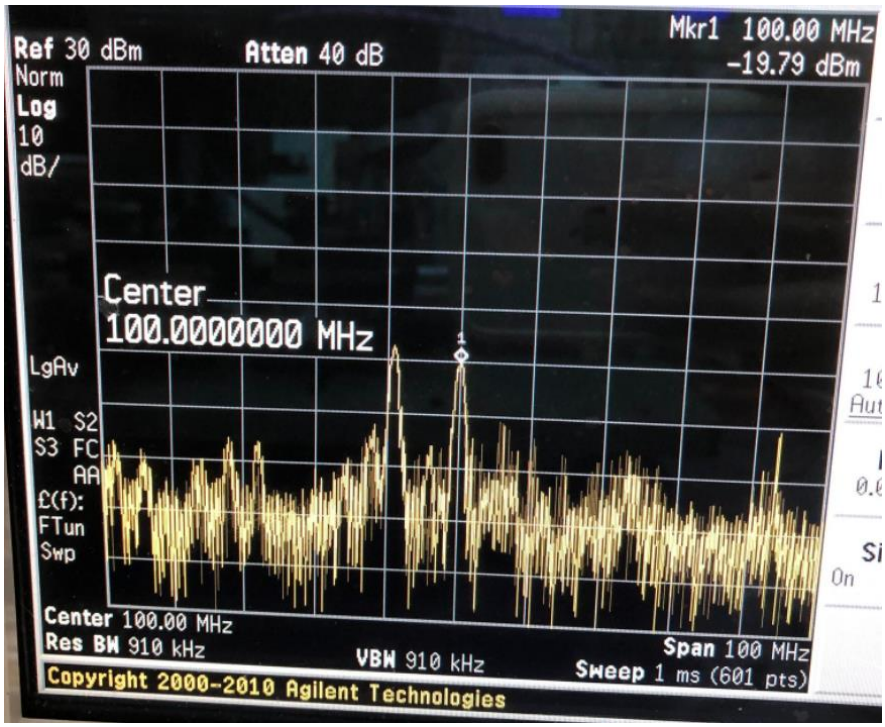


Fig. 2.33 Spectrum of the IF signal in the 1st tape-out.

doi:10.6342/NTU202203942

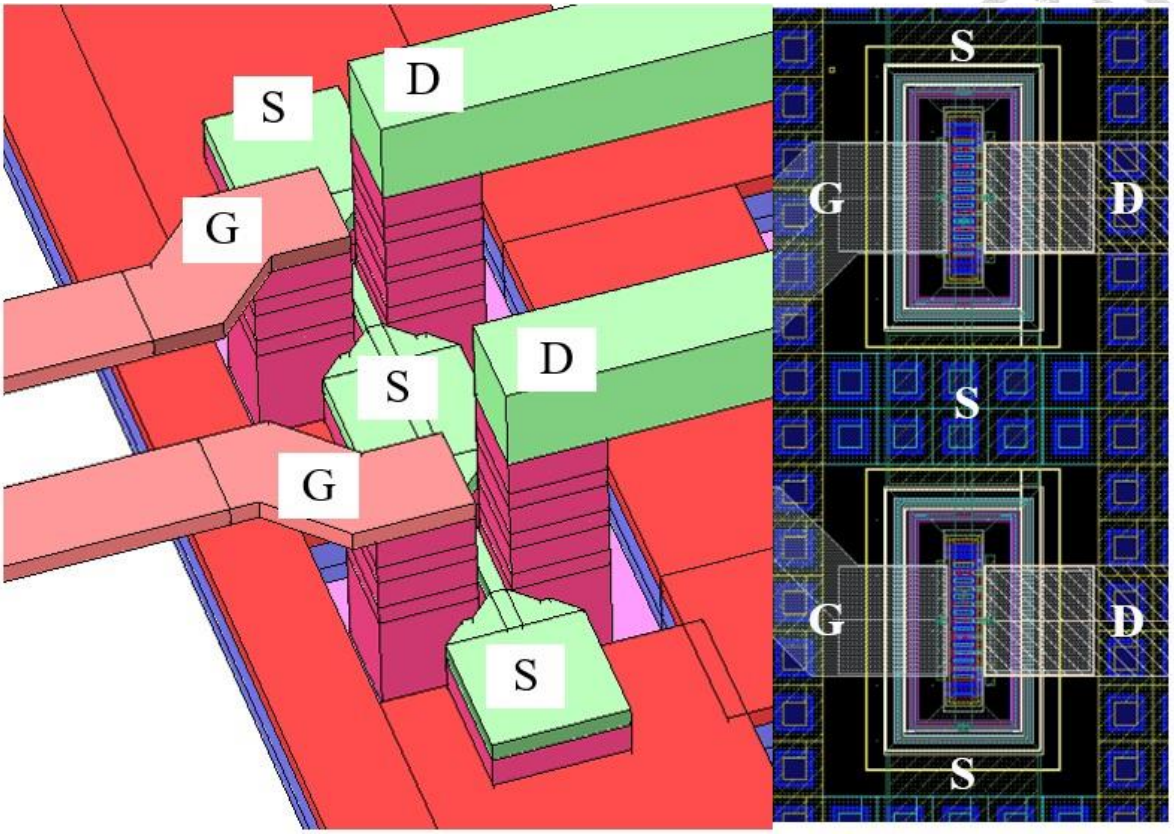


Fig. 2.34 Modified g_m stage in the 2nd tape-out.

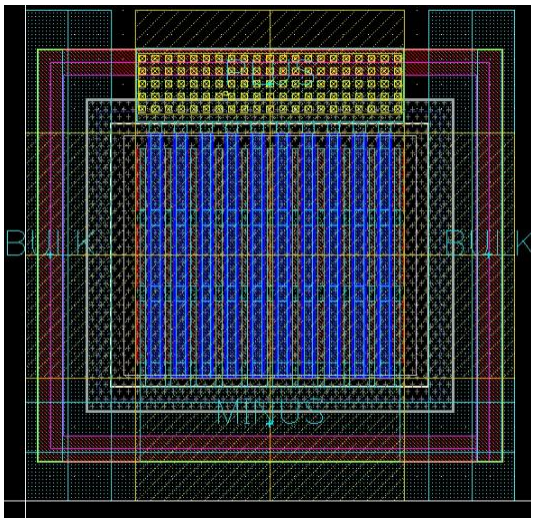


Fig. 2.35 MOS-capacitor unit with grounding (metal 1) for bypass function in the 2nd tape-out.

doi:10.6342/NTU202203942

However, the reduction in conversion gain has not improved. There is no sign of oscillation in the spectrum as shown in Fig. 2.36 and Fig. 2.37. The RF/LO reflection coefficients measurement in the 2nd tape-out and EM simulation of the high conversion gain and low noise down-conversion active mixer are shown in Fig. 2.38. The RF reflection coefficient is much worse. Since the bias voltage and current during measurement match the simulation. As a result, we ignore the issue of corner variation (SS or FF). Meanwhile, the 0.18 μm CMOS is a fairly stable and commonly used process. We do not believe that the variations in transistors' size and inductance will result in such a bad RF reflection coefficient. We have successfully solved the redundant signal near 91 MHz in the 1st tape-out. The measurement of the reflection coefficient reveals that there may be an issue with the RF path, but we cannot specify what is causing the severe reduction in conversion gain.

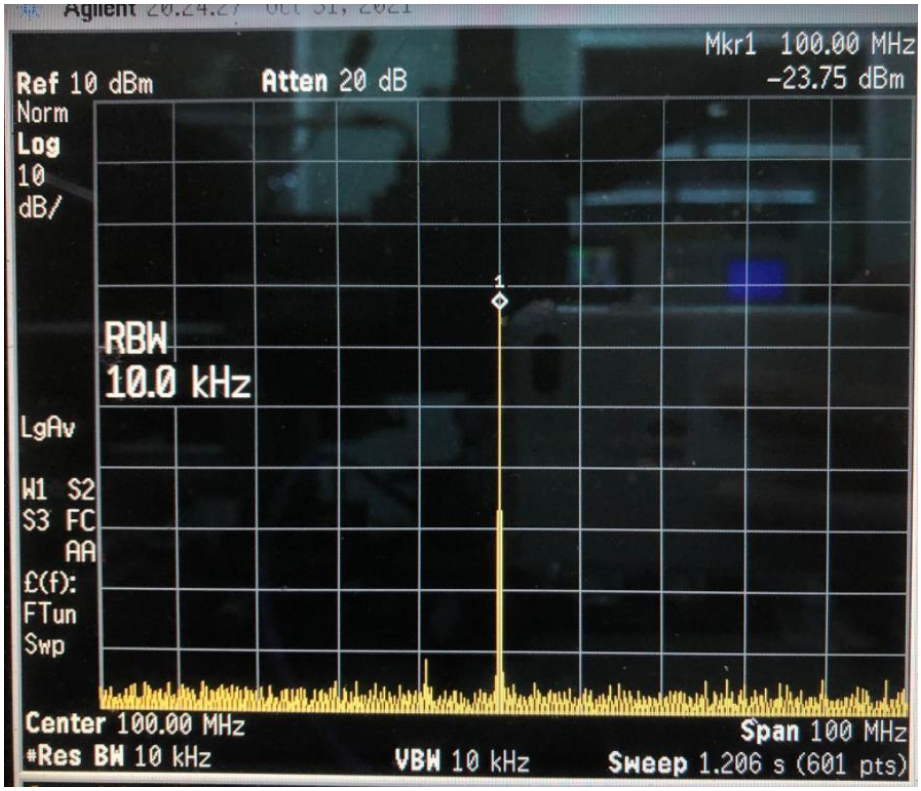


Fig. 2.36 Spectrum of the IF signal in the 2nd tape-out.

doi:10.6342/NTU202203942

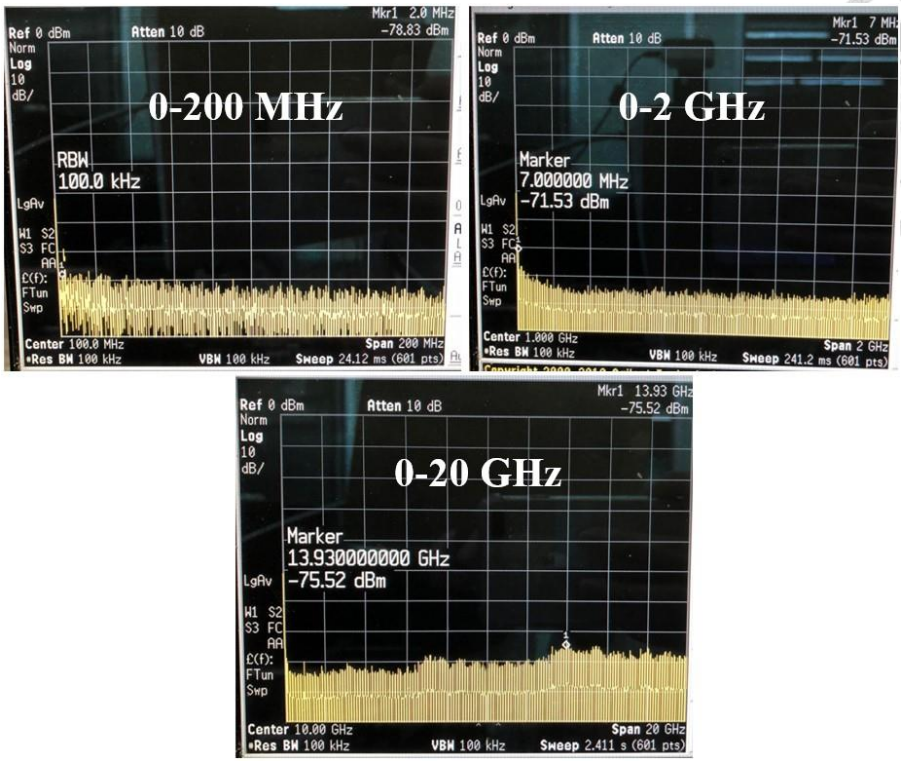


Fig. 2.37 Spectrum with only DC supplying in the 2nd tape-out.

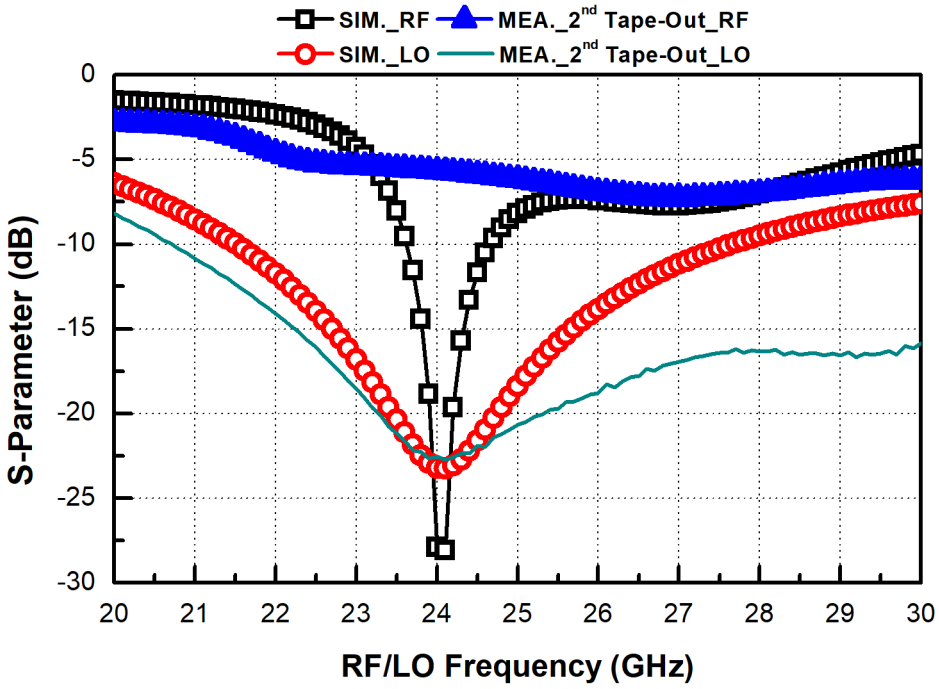


Fig. 2.38 RF/LO reflection coefficients measurement (2nd tape-out) and EM simulation of the high conversion gain and low noise down-conversion active mixer.

doi:10.6342/NTU202203942

2.4 Summary

Table 2.3- Table 2.4 summarize the performance of high conversion gain and low noise mixers in recent years. Reference [45] using the folded gilbert-cell architecture. The advantage is that ac-coupling capacitors between the current-reuse g_m stage and the switch stage allow the independent settings of the DC bias currents for the two stages. Furthermore, the output load employs a cross-coupled pair (negative impedance), allowing for very high conversion gain but the power consumption is relatively large. Compared to the other mixers, the simulated conversion gain and noise figure achieve outstanding performance with small power consumption, although the reason for the severe reduction in conversion gain has not been found so far. The simulated IP_{1dB} only perform -15 dBm but with a maximum conversion gain of 15.8 dB (with ideal IF combining), the OP_{1dB} is about -0.2 dBm. The simulated isolation also has good performance because of the use of double-balanced structure.

Table 2.3 Comparison of the published high conversion gain and low noise mixers (part I).

Ref.	Tech.	Function	Freq. (GHz)	LO Power (dBm)	CG. (dB)
This Work (Post-Sim.)	180 nm CMOS	Gilbert-Cell+ IF Buffer	23.1-25.2	2	12.8 (15.8 with ideal IF combining)
TCS II' 22 [9]	65 nm CMOS	Gilbert-Cell+ IF Buffer	26-39	5	6.5 (26 GHz) 7.2 (28 GHz)

doi:10.6342/NTU202203942

					4.8 (39 GHz)
Access' 19 [45]	130 nm CMOS	Folded Gilbert-Cell+ IF Buffer	23-25	-3	26.1
APMC' 18 [1]	180 nm CMOS	Gilbert-Cell+ IF Buffer	21.7-24.2	3	10.7
APMC' 17 [4]	180 nm CMOS	Gilbert-Cell+ IF Buffer+ I/Q Calibration	22.9-26.3	N/A	24 *
TMTT' 17 [5] ***	130 nm CMOS	Gilbert-Cell+ IF Buffer	23.8-24.5	N/A	15.3
EuMIC' 16 [2]	180 nm CMOS	Gilbert-Cell+ IF Buffer	20-26.5	1	11.9
TCPMT' 16 [6]	180 nm CMOS	Gilbert-Cell+ Active Balun+ IF Buffer	22.6-25.8	0	12.8

*: with pre-amplifier.

***: entire RX.

Table 2.4 Comparison of the published high conversion gain and low noise mixers (part II).

Ref.	IP_{1dB} (dBm)	NF. (dB)	ISO. (dB)	P_{DC} (mW)	Size

doi:10.6342/NTU202203942

This Work (Post-Sim.)	-15	34.7 (1 kHz) 9.8 (1 GHz)	> 60	4.9	0.84*0.56 (mm*mm)
TCS II' 22 [9]	-6.1 (28 GHz) -5.9 (39 GHz)	12.5 (26 GHz) 12.3 (28 GHz) 13.5 (39 GHz)	N/A	10.3	0.4 (mm^2)
Access' 19 [45]	-17.8	7.7 (24.5 GHz)	> 58	16.8	0.96 (mm^2)
APMC' 18 [1]	-13.6	N/A	N/A	6.6	0.51 (mm^2)
APMC' 17 [4]	-20	7.8	57.8	35 **	0.5*0.79 (mm*mm)
TMTT' 17 [5] ***	-13.2	11.6	47.3	111.15	1.53 (mm^2)
EuMIC' 16 [2]	-20	N/A	> 33	12.2	0.8*0.45 (mm*mm)
TCPMT' 16 [6]	-14.5	15.8	> 43	17.9	0.38 (mm^2)

**: include pre-amplifier and IF buffer.

***: entire RX.

doi:10.6342/NTU202203942

Chapter 3 Millimeter-Wave Up-/Down-Conversion Image Rejection Module

3.1 Introduction

Image rejection is a critical technology for both the receiver and the transmitter in the upcoming 5G communication system. In the transmitter, a low image rejection ratio (IRR) might cause power saturation of the post-stage power amplifier, affecting its operation. While image signal suppression technology does not have a big impact on the post-stage circuit in the receiver, it can help filter out the image signal to avoid converting the same frequency of the IF signal. We designed a millimeter-wave frequency conversion module that can up and down convert, decreasing the module's complexity and cost while also providing image rejection. The RF frequency ranges from 27.5 to 29 GHz, while the LO frequency is 25 GHz, and the IF frequency ranges from 2.5 to 4 GHz. The millimeter-wave up-/down-conversion image rejection module is composed of a frequency doubler, a mixer, and a tunable quadrature power divider that serves as the I/Q (in-phase/quadrature) divider/combiner at the IF end.

3.2 Design Concepts of The Millimeter Wave Up-/Down-Conversion Image Rejection Module

The easiest way to eliminate the image signal is to use a filter. However, with the development of millimeter-wave frequencies, there will be a situation where the desired RF

doi:10.6342/NTU202203942

band and the image band overlap as shown in Fig. 3.1. Therefore, using a filter will affect the desired RF signal. The Weaver mixer and the Hartley mixer are two common solutions. The Weaver mixer is a dual-conversion image rejection structure, there will be two image signals, and the Weaver mixer can only eliminate the first image signal. We employ a Hartley mixer due to the simplicity of the image rejection mechanism. The image rejection mechanism of the Hartley mixer is shown in Fig. 3.2. Based on Fig. 3.2, we construct the proposed millimeter-wave up-/down-conversion image rejection module as shown in Fig. 3.3. In this configuration, the I/Q divider/combiner serves as a band-pass filter and quadrature signal generator. When doing up- or down-conversion, the connection to the mixer is reversed. The signal at nodes A, B, C, D, E, and F is discussed below.

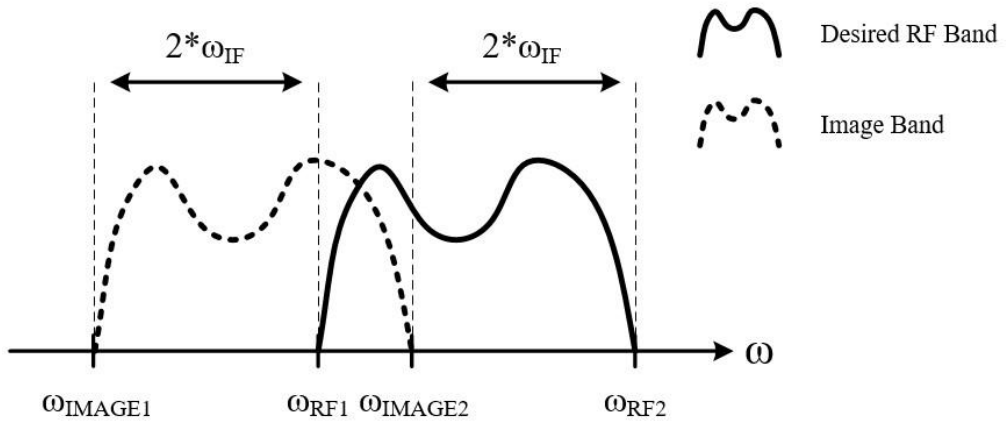


Fig. 3.1 Overlapped band of desired RF and image signals.

doi:10.6342/NTU202203942

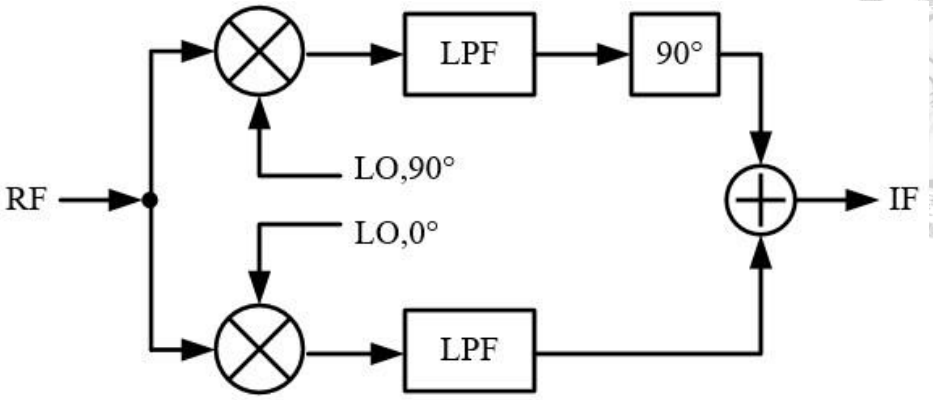


Fig. 3.2 Image rejection mechanism of Hartley mixer.

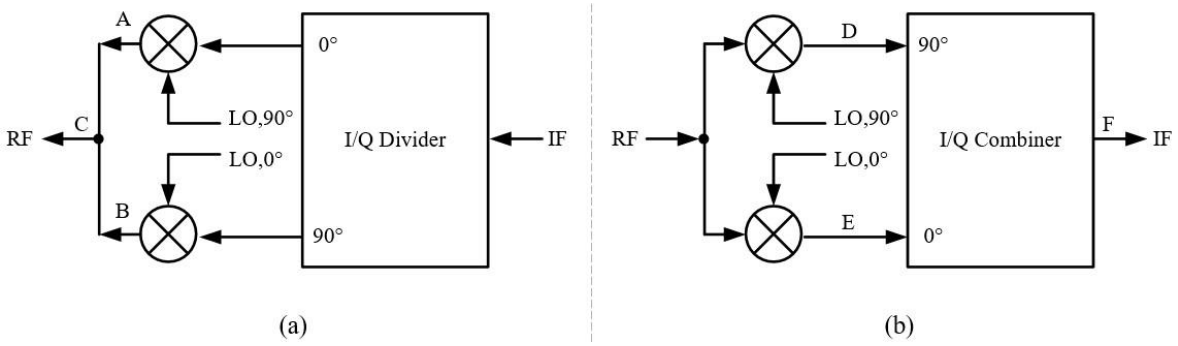


Fig. 3.3 Image rejection mechanism of (a) up- and (b) down-conversion.

First, we look at what happens when a mixer goes down-conversion. V_{RF} and V_{LO} can be used to characterize RF and LO signals, respectively. RF, LO, and image frequency be described as ω_{RF}, ω_{LO}, and ω_{IMG}, respectively, therefore we get

$$V_{RF} = A_{RF} \cdot \cos(\omega_{RF} \cdot t) + A_{IMG} \cdot \cos(\omega_{IMG} \cdot t), \tag{3.1}$$

$$V_{LO} = A_{LO} \cdot \cos(\omega_{LO} \cdot t), \tag{3.2}$$

$$V_{LO,90°} = A_{LO} \cdot \cos(\omega_{LO} \cdot t + 90°) = -A_{LO} \cdot \sin(\omega_{LO} \cdot t), \tag{3.3}$$

and

$$\omega_{RF} - \omega_{LO} = \omega_{LO} - \omega_{IMG}. \tag{3.4}$$

Signal at node D can be described as

doi:10.6342/NTU202203942

$$\frac{1}{2}\cdot\alpha\cdot A_{RF}\cdot A_{LO}\cdot\sin(\omega_{RF}\cdot t-\omega_{LO}\cdot t) \tag{3.5}$$

$$-\frac{1}{2}\cdot\alpha\cdot A_{LO}\cdot A_{IMG}\cdot\sin(\omega_{LO}\cdot t-\omega_{IMG}\cdot t).$$

After 90° phase shifting, signal at node D can be described as

$$\frac{1}{2}\cdot\alpha\cdot A_{RF}\cdot A_{LO}\cdot\cos(\omega_{RF}\cdot t-\omega_{LO}\cdot t) \tag{3.6}$$

$$-\frac{1}{2}\cdot\alpha\cdot A_{LO}\cdot A_{IMG}\cdot\cos(\omega_{LO}\cdot t-\omega_{IMG}\cdot t).$$

Signal at node E can be described as

$$\frac{1}{2}\cdot\alpha\cdot A_{RF}\cdot A_{LO}\cdot\cos(\omega_{RF}\cdot t-\omega_{LO}\cdot t) \tag{3.7}$$

$$+\frac{1}{2}\cdot\alpha\cdot A_{LO}\cdot A_{IMG}\cdot\cos(\omega_{LO}\cdot t-\omega_{IMG}\cdot t).$$

So, signal at node F can be described as

$$\alpha\cdot A_{RF}\cdot A_{LO}\cdot\cos(\omega_{RF}\cdot t-\omega_{LO}\cdot t). \tag{3.8}$$

A_{RF}, A_{LO}, and A_{IMG} denote the amplitudes of the RF, LO, and image signals, respectively, and α is an amplitude coefficient. When the mixer goes down-conversion, Eq. (3.8) shows the desired signal.

Next, we look at what happens when a mixer goes up-conversion. V_{IF} can be used to characterize the IF signal. IF frequency can be described as ω_{IF}, therefore we get

$$V_{IF}=A_{IF}\cdot\cos(\omega_{IF}\cdot t), \tag{3.9}$$

$$\omega_{RF}=\omega_{LO}+\omega_{IF}, \tag{3.10}$$

and

$$\omega_{IMG}=\omega_{LO}-\omega_{IF}. \tag{3.11}$$

Signal at node A can be described as

doi:10.6342/NTU202203942

$$A_{LO} \cdot \cos(\omega_{LO} \cdot t + 90°) \cdot A_{IF} \cdot \cos(\omega_{IF} \cdot t) \tag{3.12}$$

$$= \frac{1}{2} \cdot \alpha \cdot A_{LO} \cdot A_{IF} \cdot [\cos(\omega_{LO} \cdot t + 90° - \omega_{IF} \cdot t) + \cos(\omega_{LO} \cdot t + 90° + \omega_{IF} \cdot t)]$$

$$= \frac{1}{2} \cdot \alpha \cdot A_{LO} \cdot A_{IF} \cdot [-\sin(\omega_{LO} \cdot t - \omega_{IF} \cdot t) + \cos(\omega_{LO} \cdot t + 90° + \omega_{IF} \cdot t)].$$

Signal at node B can be described as

$$A_{LO} \cdot \cos(\omega_{LO} \cdot t) \cdot A_{IF} \cdot \cos(\omega_{IF} \cdot t + 90°) \tag{3.13}$$

$$= \frac{1}{2} \cdot \alpha \cdot A_{LO} \cdot A_{IF} \cdot [\cos(\omega_{LO} \cdot t - \omega_{IF} \cdot t - 90°) + \cos(\omega_{LO} \cdot t + \omega_{IF} \cdot t + 90°)]$$

$$= \frac{1}{2} \cdot \alpha \cdot A_{LO} \cdot A_{IF} \cdot [+\sin(\omega_{LO} \cdot t - \omega_{IF} \cdot t) + \cos(\omega_{LO} \cdot t + \omega_{IF} \cdot t + 90°)].$$

So, signal at node C can be described as

$$\alpha \cdot A_{LO} \cdot A_{IF} \cdot \cos(\omega_{LO} \cdot t + \omega_{IF} \cdot t + 90°). \tag{3.14}$$

A_{LO} and A_{IF} denote the amplitudes of the LO and IF signals, respectively, and α is an amplitude coefficient. When the mixer goes up-conversion, Eq. (3.14) shows the desired signal.

According to Eq. (3.1)- Eq. (3.14), the image signal elimination mechanism of the proposed millimeter-wave up-/down-conversion image rejection module is defined.

The system block diagram of the full millimeter-wave up-/down-conversion image rejection module, divided into two boards for discussion, is shown in Fig. 3.4. Board 1 will be discussed below. The I/Q mixer is HMC524ALC3B [12], as shown in Fig. 3.5 (a). This mixer consists of a 90° hybrid and two passive mixers. According to the datasheet, it supports RF and LO frequencies ranging from 22 to 32 GHz, IF frequencies ranging from DC to 4.5 GHz, and an image rejection ratio of 20 dB. Because the mixing operation is controlled by the large signal at the LO port, no DC bias is required, considerably simplifying the internal

doi:10.6342/NTU202203942

wiring of the module with fewer substrate layers. The frequency doubler is HMC942LP4E [13], as shown in Fig. 3.5 (b). This doubler is an x2 active frequency multiplier. According to the datasheet, it supports input frequencies ranging from 12.5 to 15 GHz. The doubler provides 17 dBm typical output power from 25 to 30 GHz when operated by at least a 4 dBm input signal. The doubler also has typical input-to-output isolation of 55 dB.

Table 3.1 Specifications of HMC524ALC3B and HMC942LP4E.

Spec.	HMC524ALC3B (mixer)	Spec.	HMC942LP4E (doubler)
Freq. (GHz)	22-32 (RF and LO) DC-4.5 (IF)	Freq.	12.5-15 (input) 25-30 (output)
LO drive level (dBm)	17	Input drive level (dBm)	4
Conversion loss	6 (up)/ 9 (down)	Output power (dBm)	17-21
IRR (dB)	18-20	Iso. (dB)	55 (in-to-out)

doi:10.6342/NTU202203942

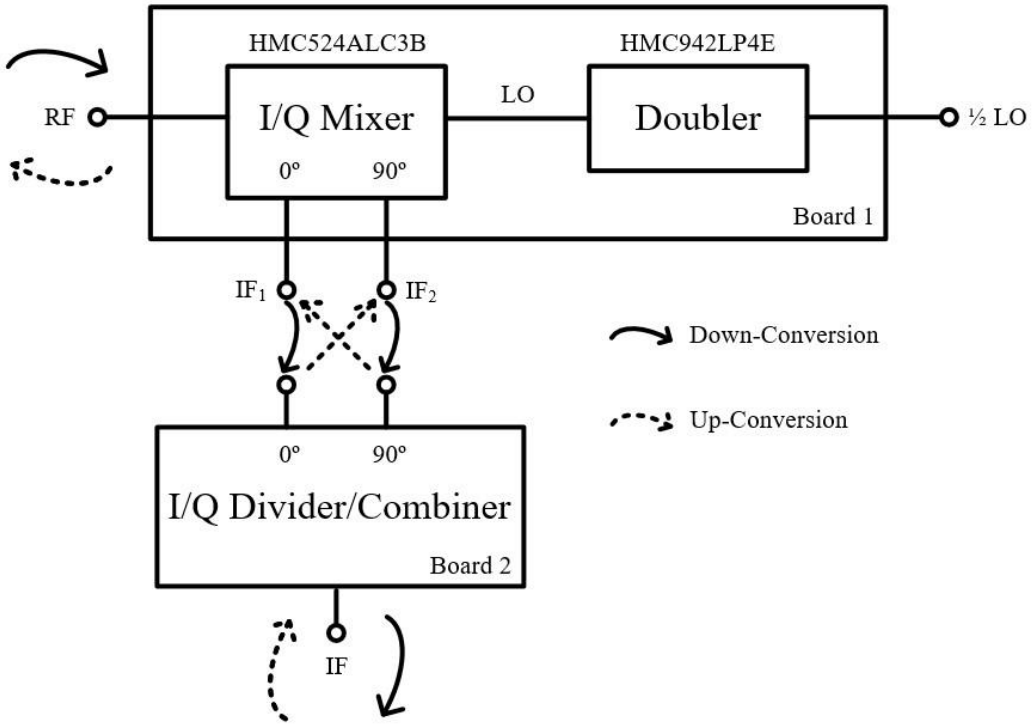


Fig. 3.4 System block diagram of the full millimeter-wave up-/down-conversion image rejection module.

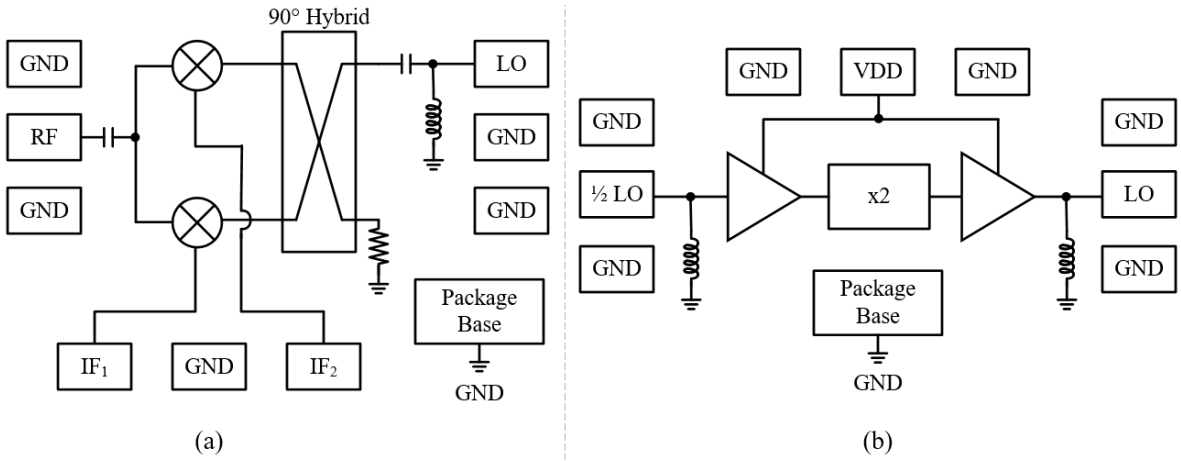


Fig. 3.5 Functional diagrams of (a) HMC524ALC3B and (b) HMC942LP4E.

The IRR design goal of the millimeter-wave up-/down-conversion image rejection module is greater than 20 dB; the frequency design goals are the RF frequency ranges from 27.5 to 29 GHz, while the LO frequency is 25 GHz, and the IF frequency ranges from 2.5 to

doi:10.6342/NTU202203942

4 GHz. Since we will employ a PLL evaluation board to generate LO signal, low-frequency LO generators are easier to obtain and less cost. According to the specification in Table 3.1, this module employs HMC524ALC3B (mixer) and HMC942LP4E (doubler), a 4 dBm input signal at 12.5 GHz is only required for the I/Q mixer to operate at 27.5-29 GHz. We can therefore use the HMC807LP6CE (VCO output power: 4-10 dBm at 12.4-13.4 GHz) [14] as the PLL evaluation board. The millimeter-wave up/down-conversion image rejection module is implemented on a four-layer PCB as shown in Fig. 3.6. The signal will be transmitted on the RO4003C board. The FR4-PP and FR4 boards are added to avoid the RO4003C board being too soft and affecting the measurement.

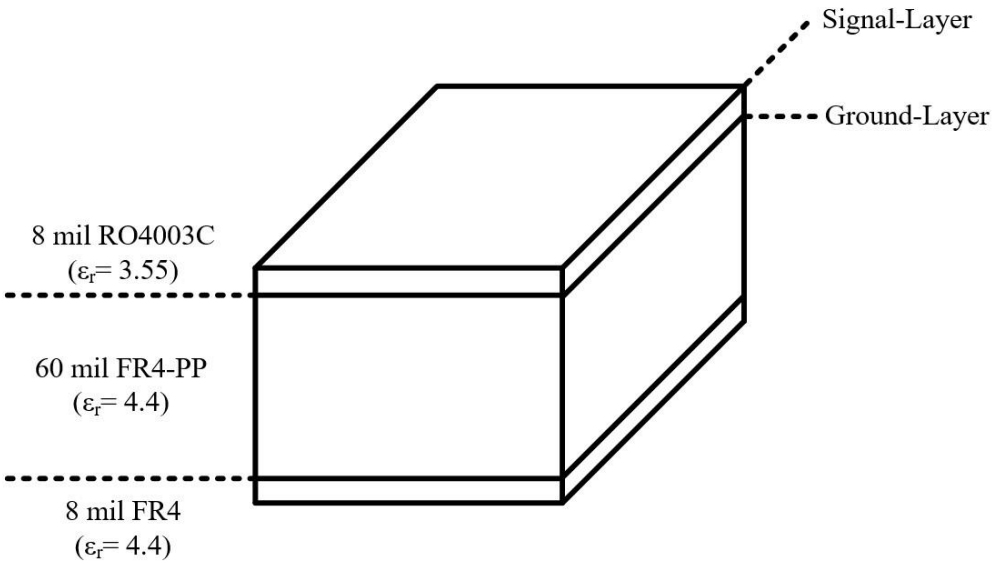


Fig. 3.6 Four-layer PCB stacking.

doi:10.6342/NTU202203942

3.3 Circuit Design of The Tunable I/Q Divider/Combiner

3.3.1 Concepts of The I/Q Divider/Combiner

A complete image rejection mixer, as defined by Eq. (3.1)- Eq. (3.14), requires a quadrature signal divider/combiner at its IF ends, such as board 2 in Fig. 3.4. There are numerous approaches to generating quadrature signals. A branch-line coupler [15], a Lange coupler [15], and a power divider with left-/right-handed transmission lines [16] are three common ways. Since a Lange coupler is constructed by four parallel coupled lines with interconnections, it would be quite difficult to implement on a PCB. When compared with a bandwidth criterion of -10 dB reflection coefficient, the power divider is superior since a broadband branch-line coupler typically requires a multi-section design [17]-[22], which implies it requires a larger area. Both of them can be designed to have a similar phase difference. The amplitude imbalance of the power divider is essentially smaller when the power ratio of the two outputs is designed as 1:1. As a result, the fundamental configuration of the I/Q divider/combiner is a power divider with left-/right-handed transmission lines. However, inaccuracies will occur during the manufacturing of each board or component. The phase imbalance and amplitude imbalance between the two IF outputs of board 1 are measured using a KEYSIGHT DSOS804A digital storage oscilloscope (8 GHz), as shown in Fig. 3.4.

doi:10.6342/NTU202203942

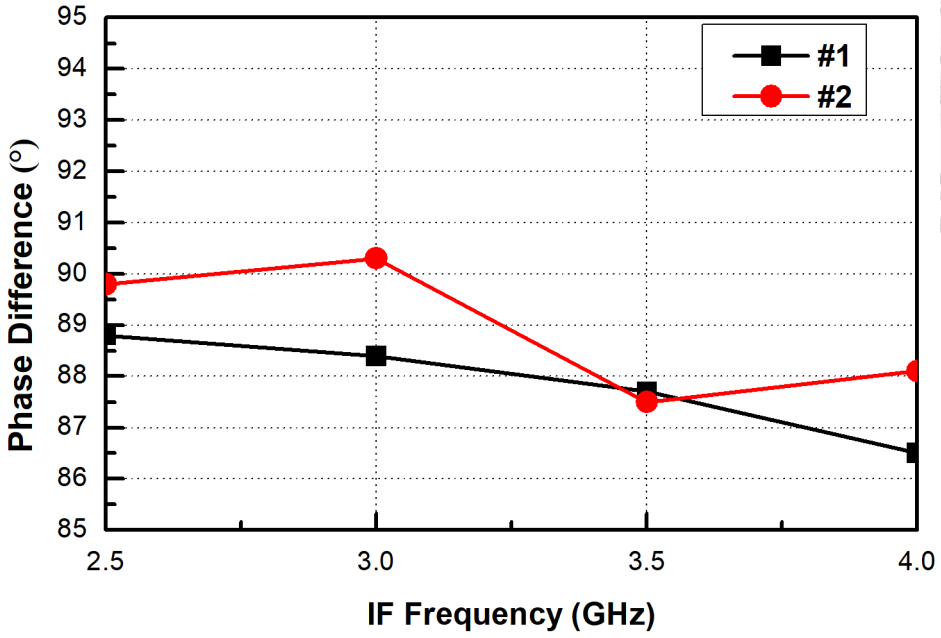


Fig. 3.7 Measured phase difference (IF_2 minus IF_1) of sample #1,2.

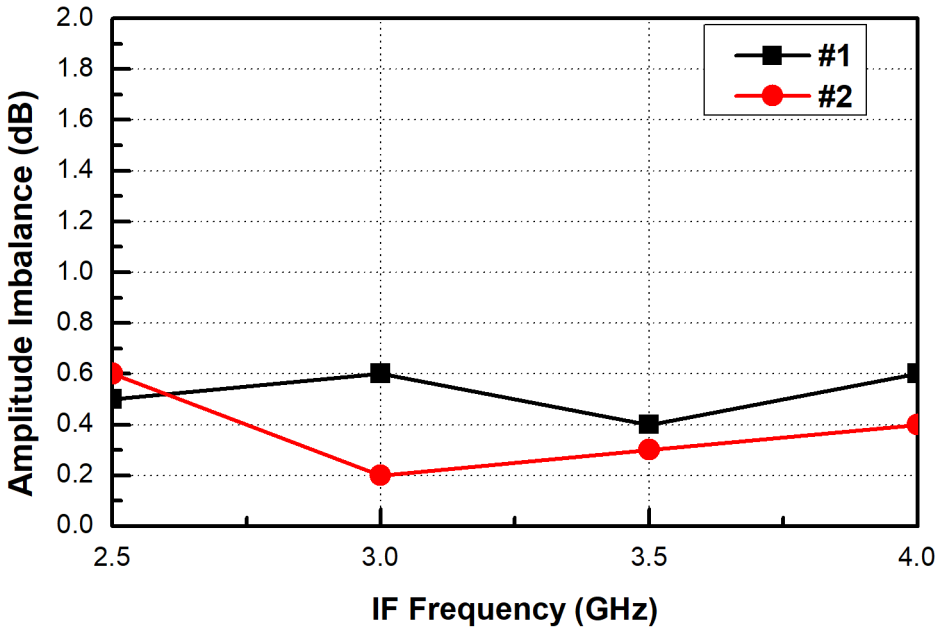


Fig. 3.8 Measured amplitude imbalance (IF_2 minus IF_1) of sample #1,2.

Samples #1 and #2 are both the board 1 in Fig. 3.4. The phase difference and amplitude imbalance of the two IF outputs are different, as shown in Fig. 3.7 and Fig. 3.8. Because of these differences, each sample of this module will have a distinct IRR.

doi:10.6342/NTU202203942

We need to construct an I/Q divider/combiner with tunable phase and amplitude functions to deal with the varied phase difference and amplitude imbalance.

The proposed tunable I/Q divider/combiner is shown in Fig. 3.9. It is composed of a Wilkinson power divider (block A), left/right transmission lines (block B), and a T-type attenuator (block C). Because the right-handed transmission line is generally built as a microstrip line, the capacitors on the left-handed transmission line are replaced with varactors to control the phase tuning. The amplitude tuning is controlled by the T-type attenuator. The proposed tunable I/Q divider/combiner is implemented on a 0.6 mm thick FR4 PCB.

Considering that the IF frequency in the following chapter is 3-5 GHz, the proposed tunable I/Q divider/combiner has a frequency design goal of 2.5-5 GHz and the center frequency is set at 4 GHz. The design goal of the tunable phase difference is 80-100° at 2.5-5 GHz while the tunable amplitude imbalance is (-1)-1 dB. The design goal of the reflection coefficient is less than -10 dB at 2.5-5 GHz.

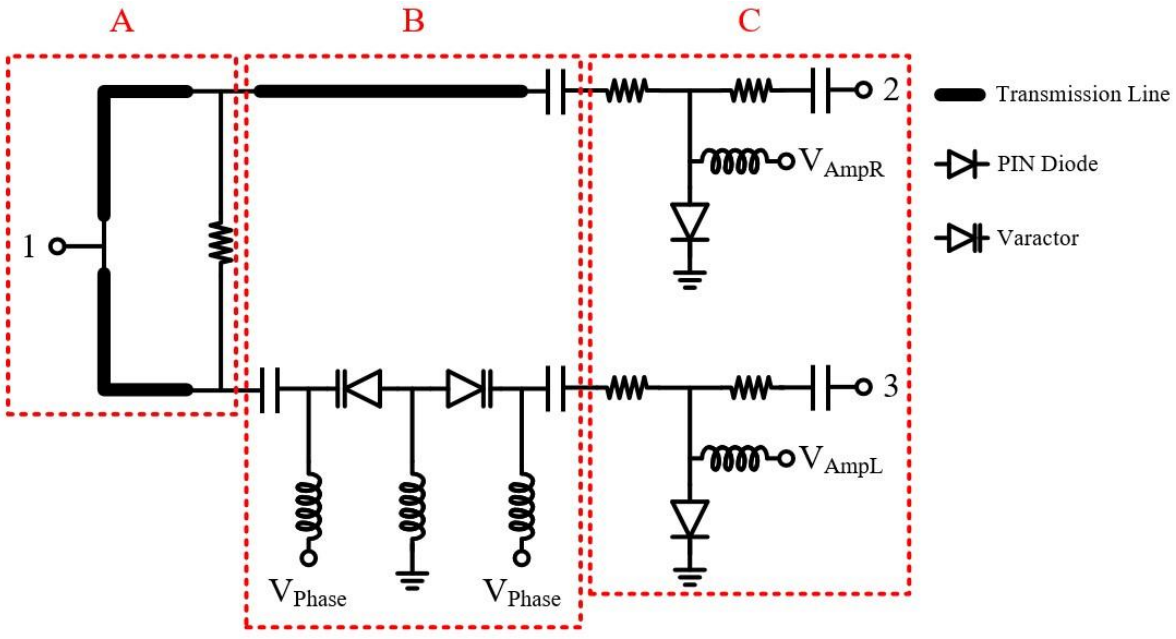


Fig. 3.9 Proposed tunable I/Q divider/combiner.

doi:10.6342/NTU202203942

3.3.2 Design of The Wilkinson Power Divider

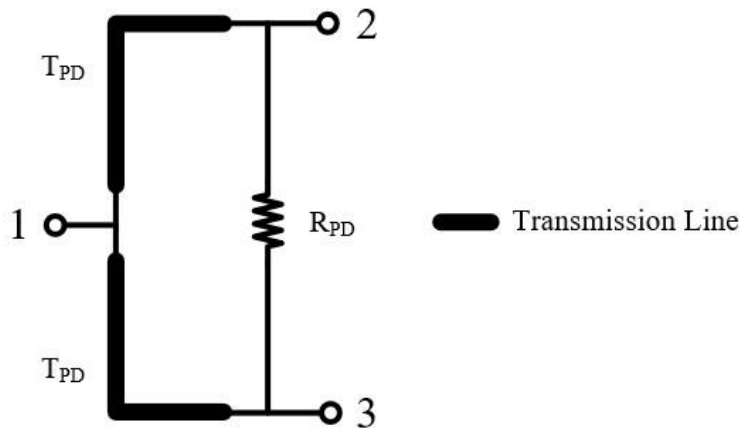


Fig. 3.10 Wilkinson power divider.

The Wilkinson power divider is shown in Fig. 3.10. It is composed of two quarter-wavelength transmission lines (T_{PD}) and a resistor (R_{PD}). The system impedance is 50 Ω, the impedance of T_{PD} is $50\sqrt{2}$ Ω, and R_{PD} is 100 Ω [15]. The Wilkinson power divider's layout is shown in Fig. 3.11.

doi:10.6342/NTU202203942

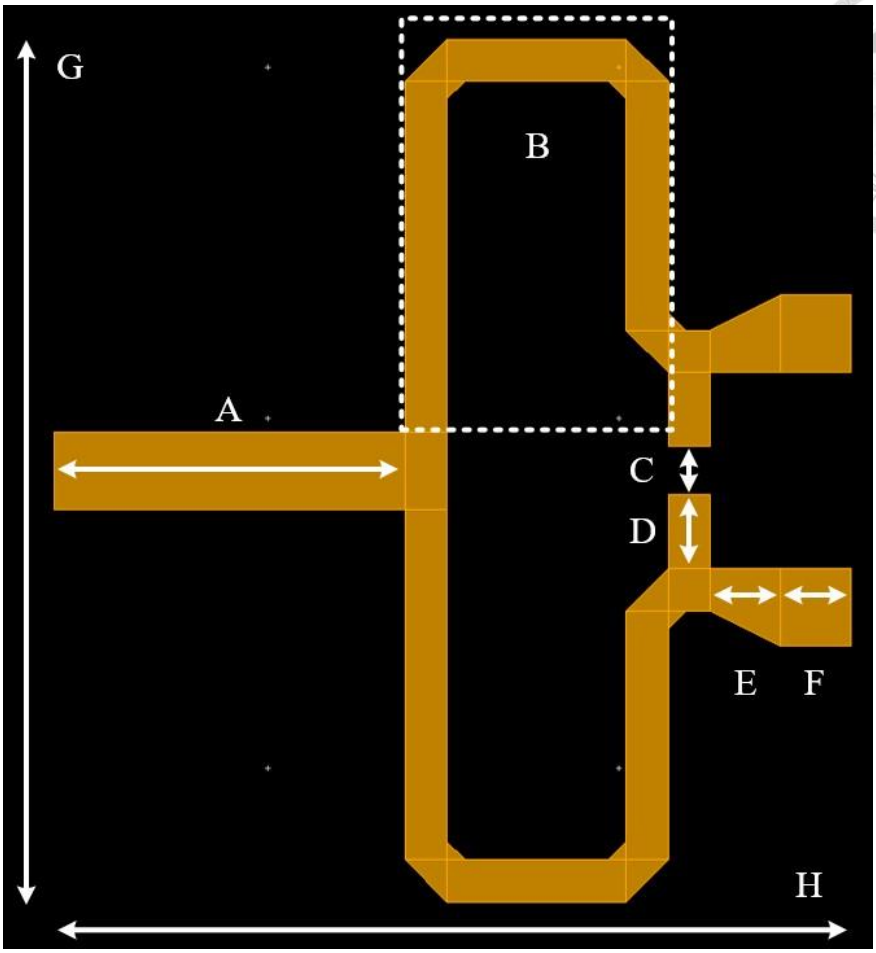


Fig. 3.11 Layout of the Wilkinson power divider.

The Wilkinson power divider is symmetrical, as shown in Fig. 3.11. Line A is a 50 Ω transmission line for soldering the SMA connector. The whole T_{PD} is contained in Block B. Gap C is where R_{PD} will be soldered. The R_{PD} is connected to the T_{PD} through Line D. Lines E and F are connected to the next stage. The detailed dimensions are shown in Table 3.2.

doi:10.6342/NTU202203942

Table 3.2 Dimensions of line A, block B, gap C, line D/E/F, and length G/H.

Each Part	Length (mm)/ Width (mm)
Line A	5/ 1.1
Block B (T_{PD})	12.4/ 0.6
Gap C	0.7
Line D	1.1/ 0.6
Line E	1/ 0.6-1.1 (taper)
Line F	1/ 1.1
Length G	12.3
Length H	11.4

The simulated S-parameters of the Wilkinson power divider are shown in Fig. 3.12 and Fig. 3.13. Port numbers are shown in Fig. 3.10. $|S_{11}|$ has a minimum of -28.9 dB at 3.6 GHz and is less than -10 dB from 2 to 6 GHz. $|S_{22}|$ and $|S_{33}|$ are both less than -20 dB from 2 to 5.6 GHz. $|S_{32}|$ has a minimum of -36.9 dB at 3.9 GHz and is less than -10 dB from 2 to 5.5 GHz. $|S_{21}|$ and $|S_{31}|$ have a maximum of -3.2 dB at 3.4 GHz and a bandwidth of 0.5 dB from 2 to 5.6 GHz.

doi:10.6342/NTU202203942

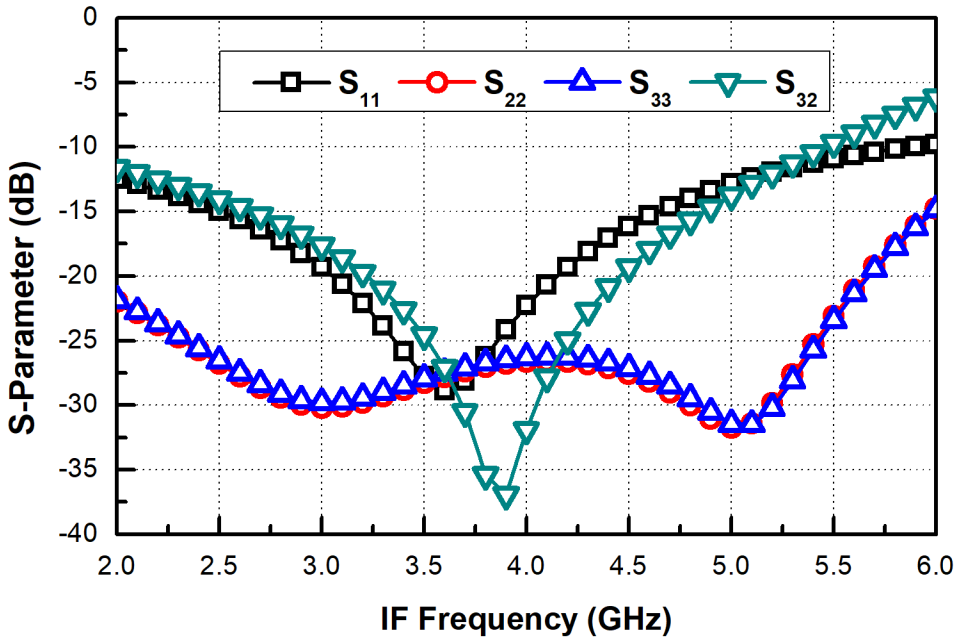


Fig. 3.12 Simulated S-parameter ($S_{11,22,33,32}$) of the Wilkinson power divider in Fig. 3.10.

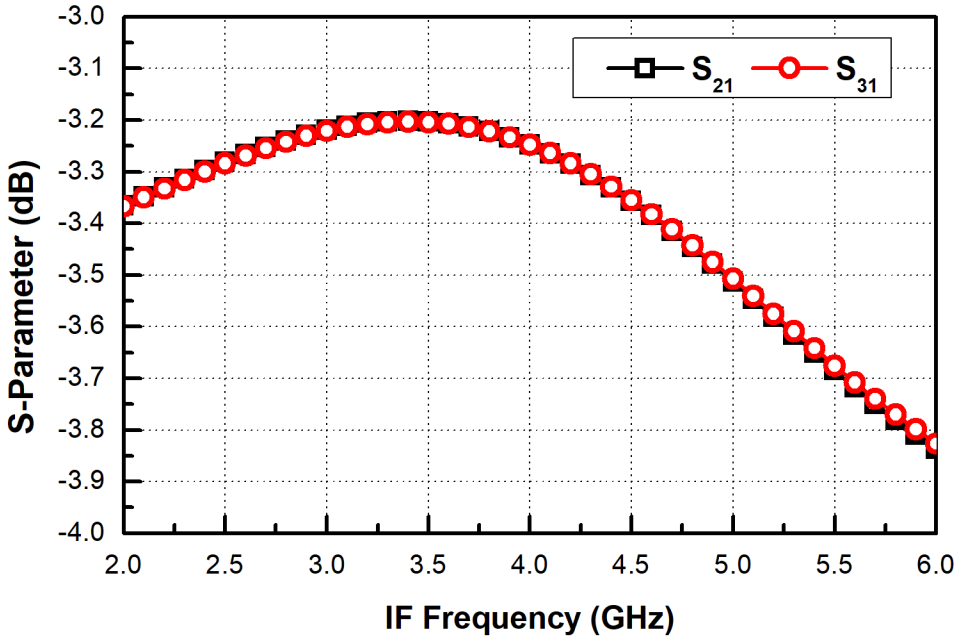


Fig. 3.13 Simulated S-parameter ($S_{21,31}$) of the Wilkinson power divider in Fig. 3.10.

doi:10.6342/NTU202203942

3.3.3 Design of The Tunable Left-/Right-Handed Transmission Lines

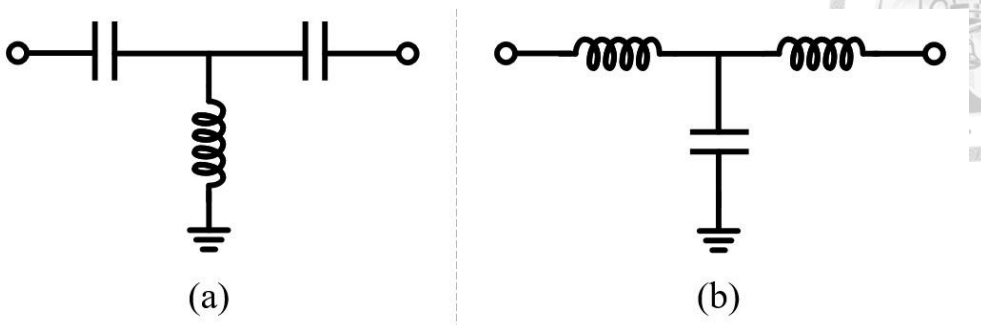


Fig. 3.14 Conventional (a) left- and (b) right-handed transmission lines.

The conventional left-/right-handed transmission lines are shown in Fig. 3.14. We use a microstrip line to implement the right-handed transmission line in general design since they have the same equivalent circuit and can reduce the need for lumped elements. The capacitance and inductance of the left-handed transmission line can be calculated by

$$C = \frac{1}{\sqrt{2} \cdot Z_0 \cdot \omega} \cdot \sqrt{\frac{1 + \cos\theta}{1 - \cos\theta}}, \tag{3.15}$$

and

$$L = \frac{\sqrt{2} \cdot Z_0}{\omega \cdot \sin\theta}. \tag{3.16}$$

Z_0 denotes the system impedance, ω denotes the angular frequency, and θ denotes the phase of the left-handed transmission line [23].

To implement a tunable phase mechanism, the capacitors on the left-handed transmission line are replaced by varactors. As shown in Fig. 3.15, the proposed left-handed transmission line is composed of two reverse-biased varactors and an inductor (L_L). Its input and output are both connected to C_{Block} for DC blocking. The voltage V_{Phase} controls the capacitance of both varactors, and L_{Choke} is an RF choke for DC feeding. The proposed right-

doi:10.6342/NTU202203942

handed transmission line (T_{Right}) is composed of a 50 Ω microstrip line and its output is connected to C_{Block} for DC blocking.

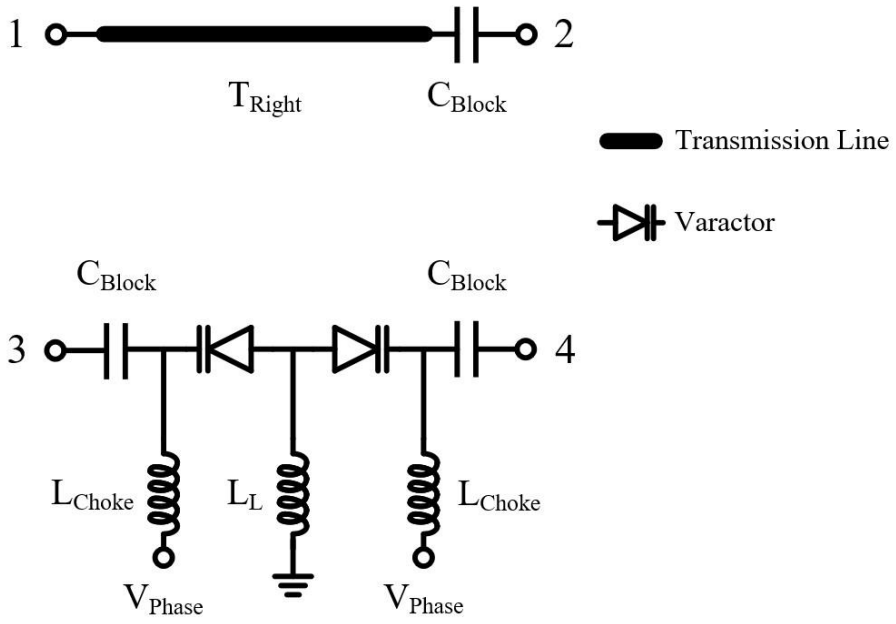


Fig. 3.15 Proposed left-/right-handed transmission lines.

The Skyworks SMV2203-040LF [24] varactor is used in the left-handed transmission line. The simulated frequency response of the varactor's capacitance is shown in Fig. 3.16. Except for V_B= 0 V, the responses of V_B= 1-22 V are relatively flat. As a result, V_B= 1 V is the tunable voltage's minimum. When operating at 4 GHz, 2 pF is the median of the tunable capacitance, therefore we choose 2 pF as varactors' capacitance to design the 90° phase difference between the left- and right-handed transmission lines.

Assuming that the left-handed transmission line has a 45° phase (θ is 45°), we can estimate the capacitance (1.4 pF) and inductance (4 nH) using Eq. (3.15) and Eq. (3.16). Considering that we choose 2 pF as varactors' capacitance, the inductance will be replaced with 2.9 nH to retain the 45° phase provided by the left-handed transmission line.

doi:10.6342/NTU202203942

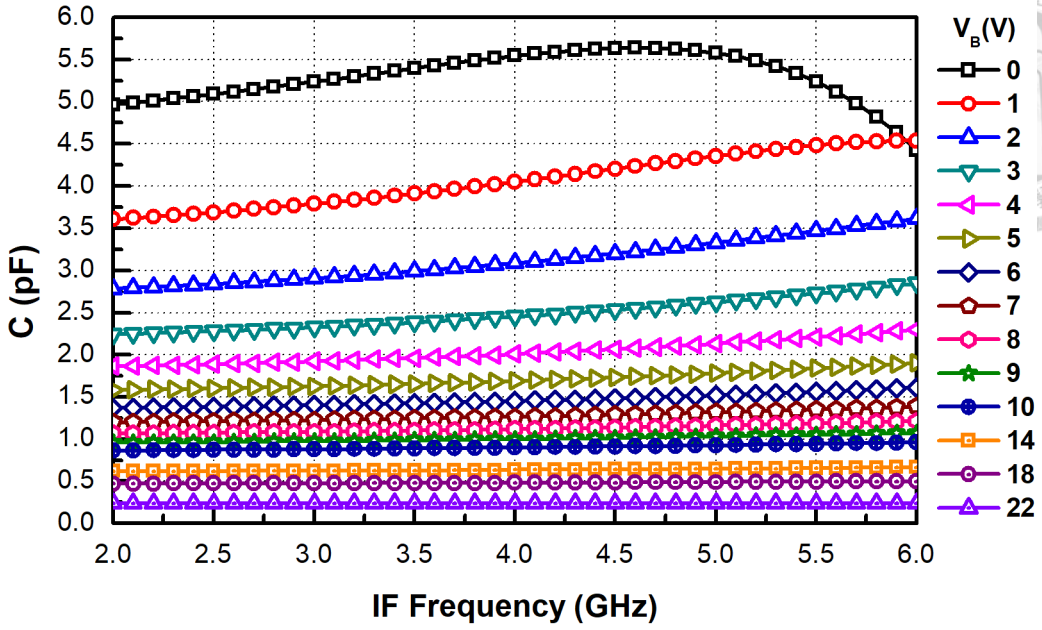


Fig. 3.16 Simulated capacitance of the varactor (SMV2203-040LF) (reverse bias V_B, 0-22 V).

The left-handed transmission line is symmetrical, as shown in Fig. 3.17. Line A connects the L_L to the ground. Gap B is where the varactor will be soldered. Line C is an open stub used to compensate for the parasitic inductance introduced by component soldering. Lines D and E connect the varactor to the C_{Block} and the L_{Choke}, respectively. Gap F is where the inductors (LL and L_{Choke}) will be soldered. Line G connects the L_{Choke} to the DC power supply. Lines H and I connect the two varactors and the L_L. The detailed dimensions and soldering positions are shown in Table 3.3 and Fig. 3.18, respectively.

The S-parameters of the lumped elements measured by TRL calibration are used in the EM simulation of the left-/right-handed transmission lines to obtain accurate phase information. The phase of the left-handed transmission line at 4 GHz is approximate -82°, as shown in Fig. 3.19. To achieve a 90° phase difference, the right-handed transmission line's

doi:10.6342/NTU202203942

phase must be -172°. Block N in Fig. 3.20 shows the right-handed transmission line (T_{Right}). The detailed dimensions are shown in Table 3.3.

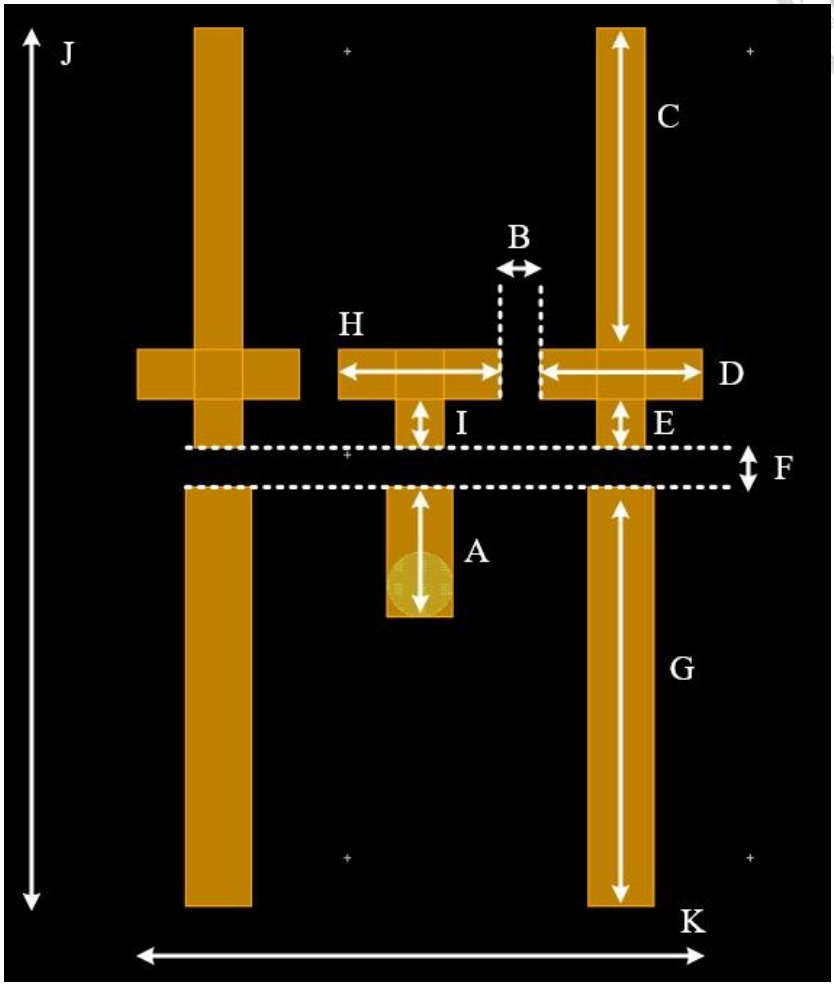


Fig. 3.17 Layout of the left-handed transmission line.

doi:10.6342/NTU202203942

Table 3.3 Dimensions of line A, gap B/F, line C, line D/H, line E/I, line G, length J/K/L/M, and block N.

Each Part	Length (mm)/ Width (mm)
Line A	1.6/ 0.8
Gap B/F	0.5
Line C	4/ 0.6
Line D/H	2/ 0.6
Line E/I	0.6/ 0.6
Line G	5.2/ 0.8
Length J	10.9
Length K	7
Length L	11
Length M	8.7
Block N (T_{Right})	18.4/ 1.1

doi:10.6342/NTU202203942

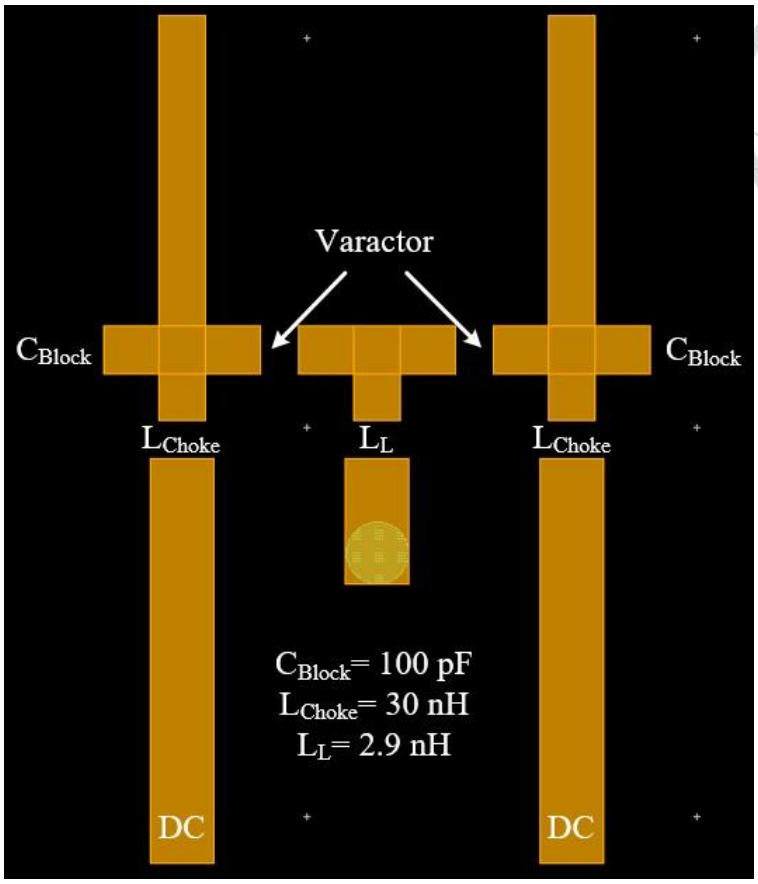


Fig. 3.18 Soldering positions of the left-handed transmission line.

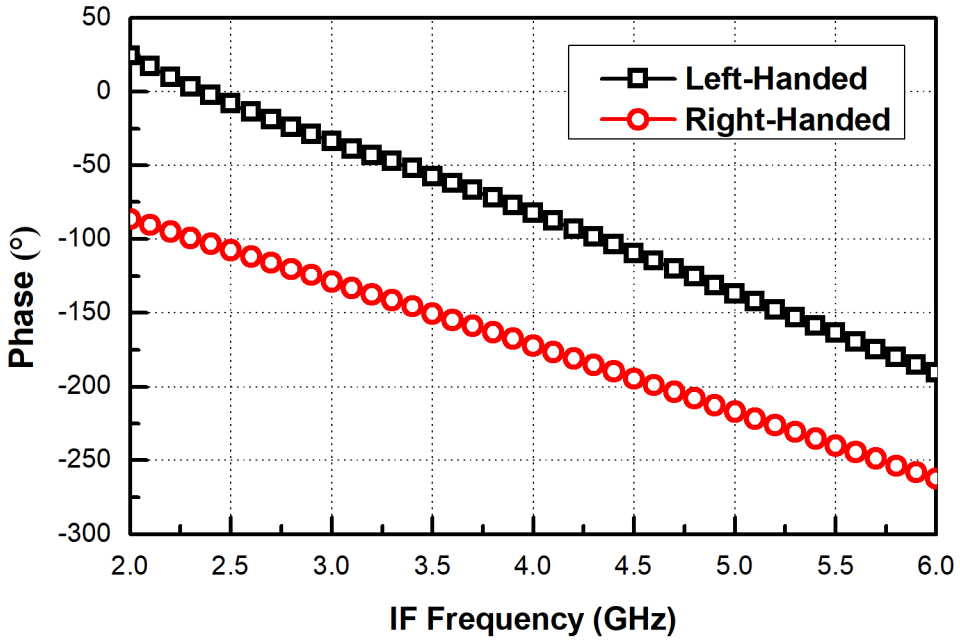


Fig. 3.19 Simulated phase of the left-/right-handed transmission lines.

doi:10.6342/NTU202203942

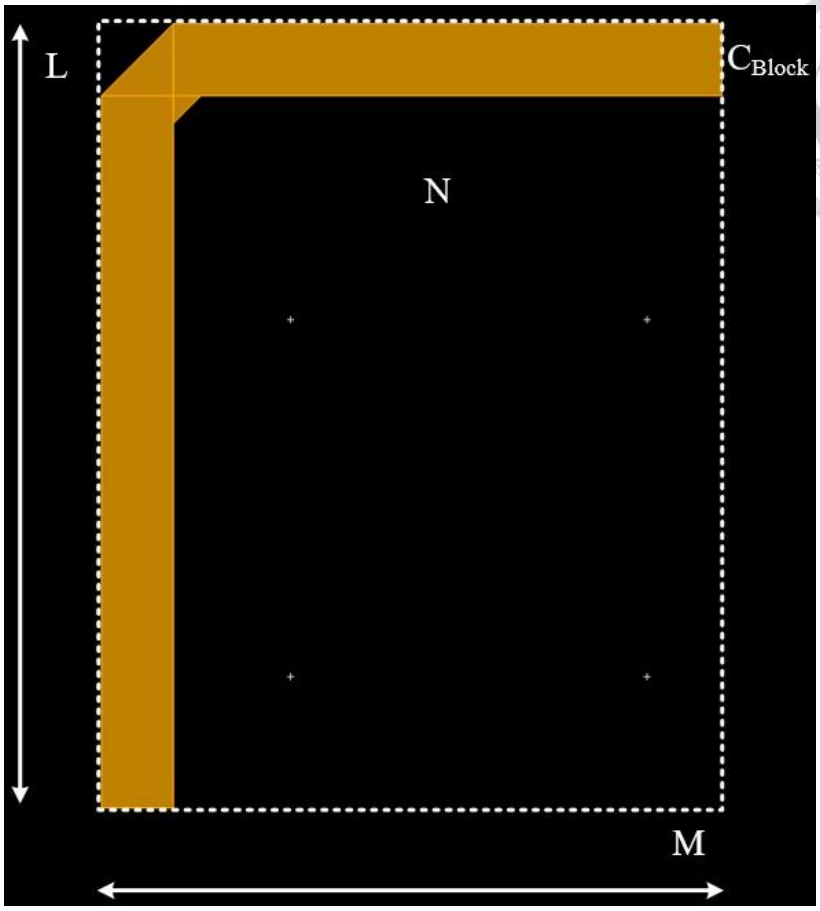


Fig. 3.20 Layout of the right-handed transmission line.

The simulated phase difference between the left-/right-handed transmission lines is shown in Fig. 3.21. When the reverse bias V_B is 1-8 V, it yields a phase of 78.7-104.8° at 4 GHz. The simulated reflection coefficient of the left-handed transmission line is shown in Fig. 3.22. It is less than -10 dB from 2 to 5.2 GHz when the reverse bias V_B is 1-8 V. The simulated reflection coefficient of the right-handed transmission line is shown in Fig. 3.23. It has a minimum of -23.4 dB at 4 GHz and is less than -15 dB from 2 to 6 GHz.

doi:10.6342/NTU202203942

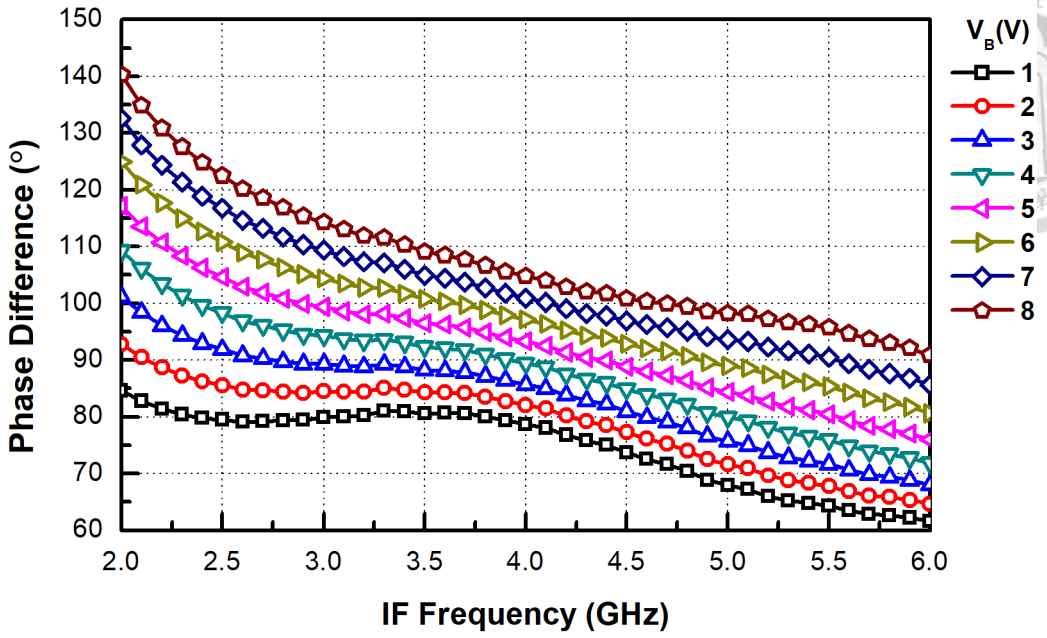


Fig. 3.21 Simulated phase difference between the left-/right-handed transmission lines (reverse bias V_B, 1-8 V).

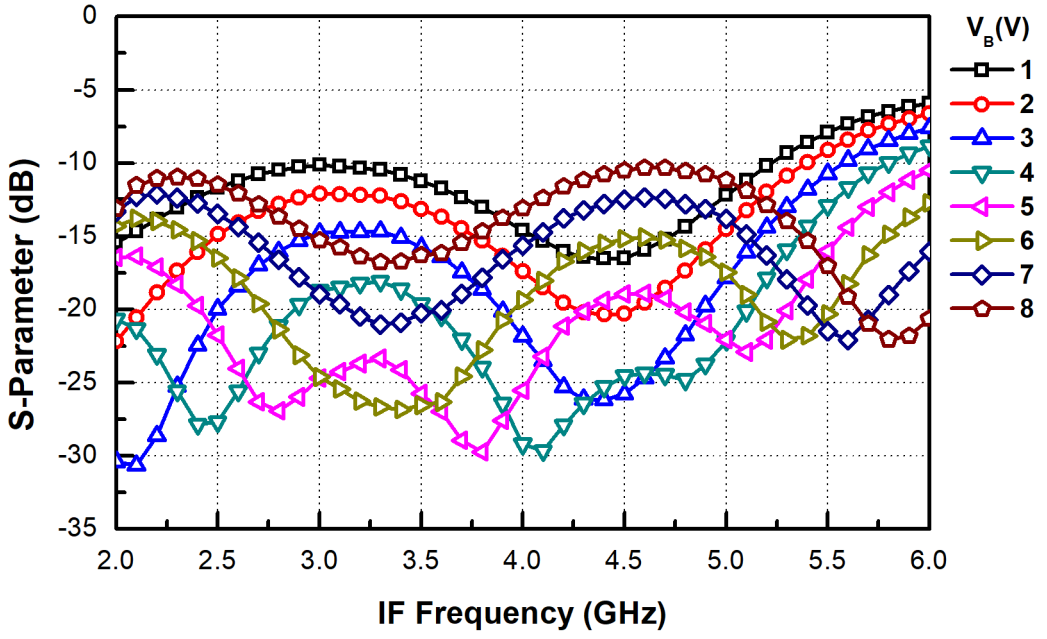


Fig. 3.22 Simulated reflection coefficient of the left-handed transmission line (reverse bias V_B, 1-8 V).

doi:10.6342/NTU202203942

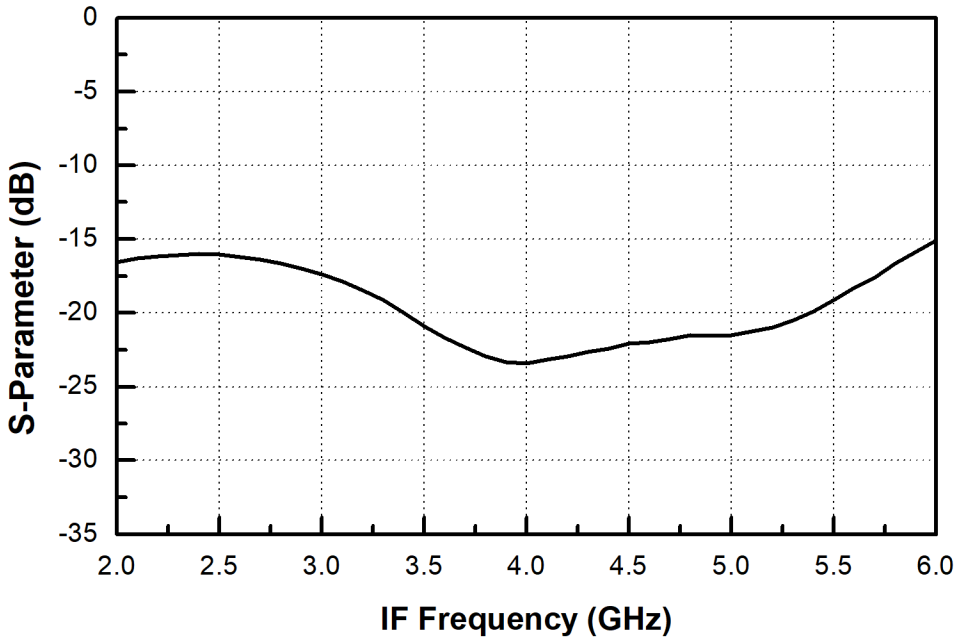


Fig. 3.23 Simulated reflection coefficient of the right-handed transmission line.

3.3.4 Design of The Tunable T-Type Attenuator

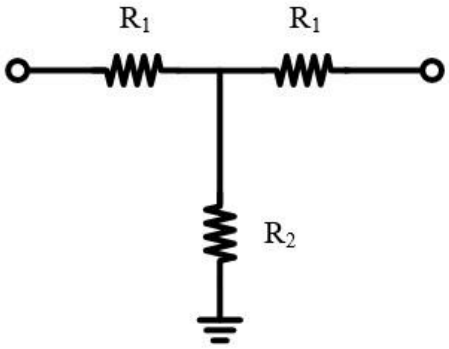


Fig. 3.24 Conventional T-type attenuator.

The conventional T-type attenuator is shown in Fig. 3.24. The resistance of a T-type attenuator is calculated by

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_2}{R_1 + R_2 + Z_0}, \tag{3.17}$$

and

doi:10.6342/NTU202203942

$$\text{Attenuation (dB)} = 20 \cdot \log(\text{A}). \quad (3.18)$$

Z_0 is the system impedance. When R_2 is large, A is extremely near to 1 and Attenuation is very close to 0 dB [23].

We replace the resistor (R_2) of the T-type attenuator with a PIN diode to construct a tunable amplitude mechanism. The proposed T-type attenuator is composed of a forward-biased PIN diode and two resistors, as shown in Fig. 3.25. The attenuation is controlled by a PIN diode via the voltage $V_{AmpR/AmpL}$. L_{Choke} is an RF choke for DC feeding. If we set port 2 to be output, we must connect a C_{Block} for DC blocking of the tunable I/Q divider/combiner.

The PIN diode in the proposed T-type attenuator is MADP-000907-14020P from MACOM [25]. According to the datasheet, it has a maximum total capacitance value of 0.03 pF. This small capacitance has a very large impedance, which allows A to remain near to 1 and Attenuation to remain close to 0 dB. The simulated attenuation of the T-type attenuator with ideal lumped elements (R_A and L_{Choke}) and without EM consideration as shown in Fig. 3.26. Without bias, there is around -0.3 dB attenuation at 4 GHz when R_A is 2 Ω and L_{Choke} is 30 nH. The forward bias 0.9-1 V curves indicate that the PIN diode is about to be turned on, and the attenuation will increase rapidly.

doi:10.6342/NTU202203942

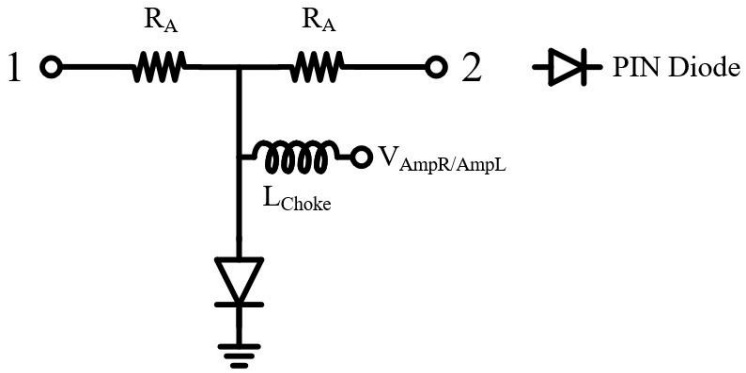


Fig. 3.25 Proposed T-type attenuator.

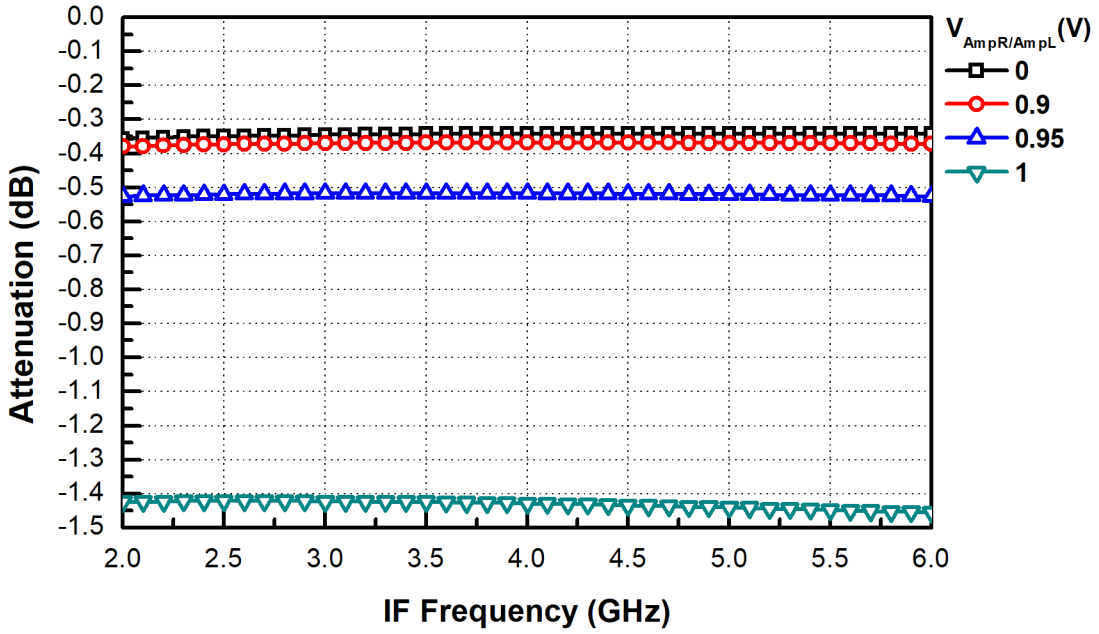


Fig. 3.26 Attenuation's ideal simulation of the T-type attenuator (forward bias $V_{AmpR/AmpL}$, 0-1 V).

The T-type attenuator is symmetrical except for lines G and H and gap F, as shown in Fig. 3.27. The R_A is connected to the front stage via Line A. Gap B is where the R_A will be soldered. Line C is an open stub used to compensate for the parasitic inductance introduced by component soldering. Line D connects the two R_As. Line E connects the two R_As and L_{Choke} and PIN diode. Gap F is the soldering area for the L_{Choke}. Line G connects the L_{Choke}

doi:10.6342/NTU202203942

to the DC power supply. Gap I is where the PIN diode will be soldered. The PIN diode is connected to the ground through Line J. The detailed dimensions and soldering positions are shown in Table 3.4 and Fig. 3.28, respectively.

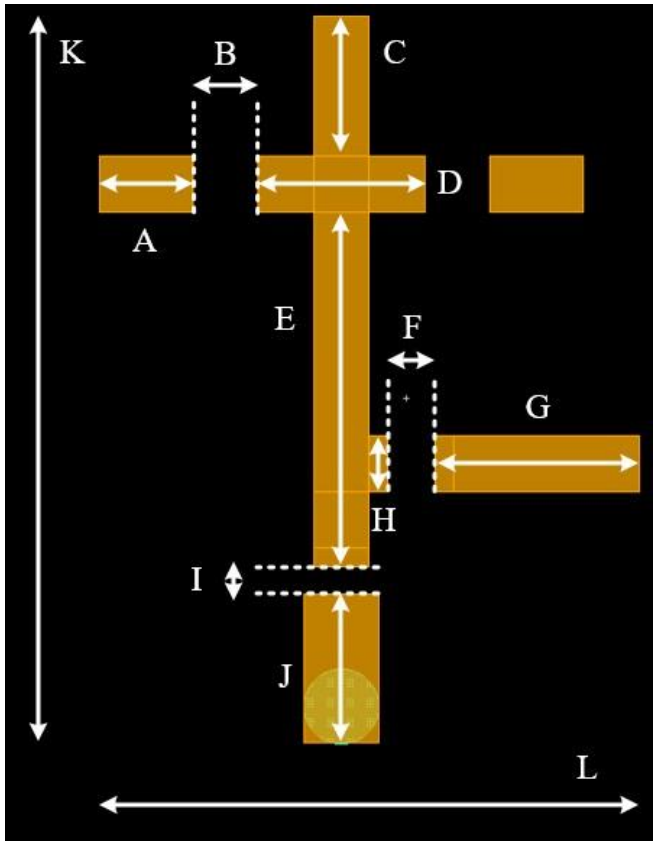


Fig. 3.27 Layout of the T-type attenuator.

Table 3.4 Dimensions of line A, gap B, line C/D/E, gap F, line G/H, gap I, line J, and length K/L.

Each Part	Length (mm)/ Width (mm)
Line A	1/ 0.6
Gap B	0.7
Line C	1.5/ 0.6

doi:10.6342/NTU202203942

Line D	1.8/ 0.6
Line E	3.8/ 0.6
Gap F	0.5
Line G	2.2/ 0.6
Line H	0.6/ 0.2
Gap I	0.3
Line J	1.6/ 0.8
Length K	7.8
Length L	5.8

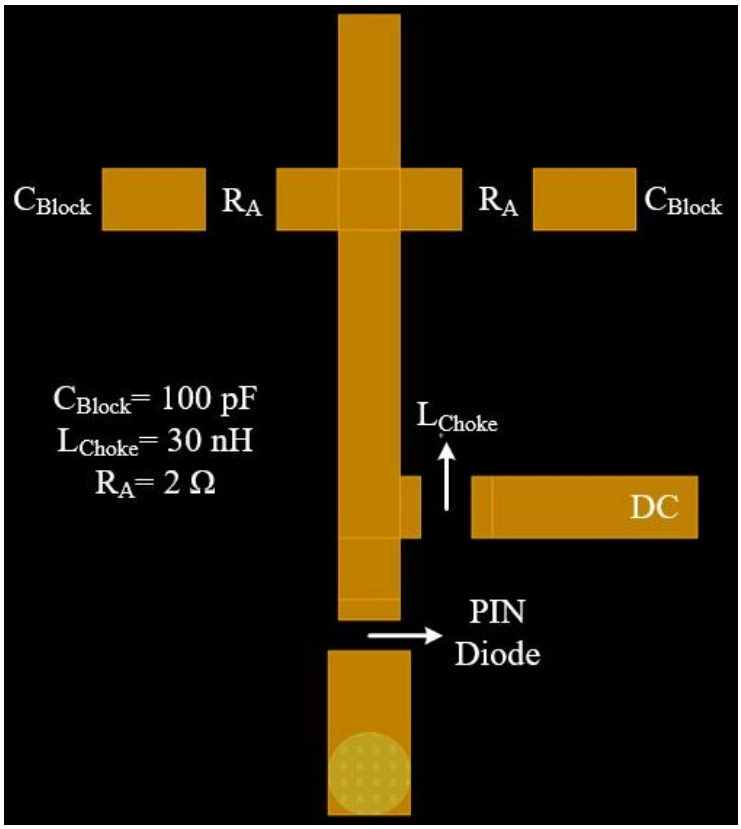


Fig. 3.28 Soldering positions of the T-type attenuator.

doi:10.6342/NTU202203942

The S-parameters of the lumped elements measured by TRL calibration are used in the EM simulation of the T-type attenuator to obtain accurate amplitude information. The simulated attenuation and reflection coefficient of the T-type attenuator with EM consideration (except line E in Fig. 3.27) are shown in Fig. 3.29 and Fig. 3.30. When the forward bias is 0.95-1 V, the attenuation is about 0.5 dB larger than the ideal case at 4 GHz. When the forward bias is 0-1 V, the reflection coefficients are all within (-10)-(-15) dB at 2-6 GHz.

With line E's EM consideration, the attenuation is fast increasing as shown in Fig. 3.31. Without bias, there is around -0.5 dB attenuation at 4 GHz. When the forward bias is 0.9-1 V, the attenuation ranges from -0.57 to -2.48 dB at 4 GHz. With line E's EM consideration, the reflection coefficient is shown in Fig. 3.32. It has a minimum of less than -30 dB at 4 GHz when the forward bias is 0-0.95 V, and a value of less than -10 dB from 2 to 5.2 GHz when the forward bias is 0-1 V. Although the attenuation is fast increasing, a minor difference in attenuation can be tuned due to the amplitude tuning at port 2,3 in Fig. 3.9. When the forward bias is 0-0.95 V, the reflection coefficient is excellent at 4 GHz; when the forward bias is 1 V, it begins to deteriorate but remains less than -10 dB from 2 to 5.2 GHz.

doi:10.6342/NTU202203942

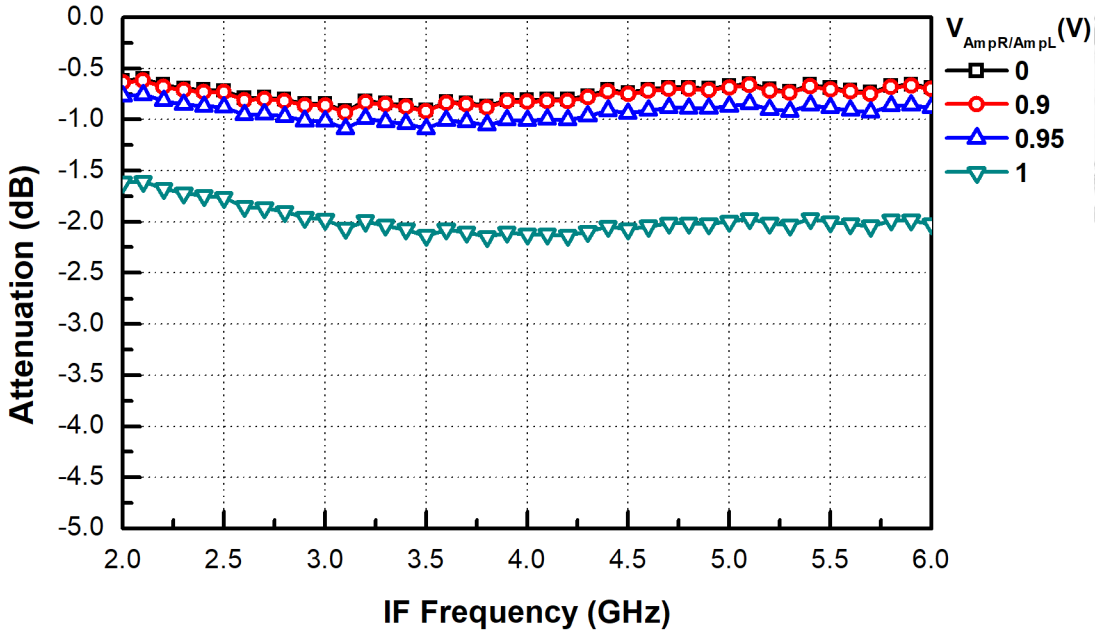


Fig. 3.29 Attenuation's EM simulation (without line E in Fig. 3.27) of the T-type attenuator (forward bias $V_{AmpR/AmpL}$, 0-1 V).

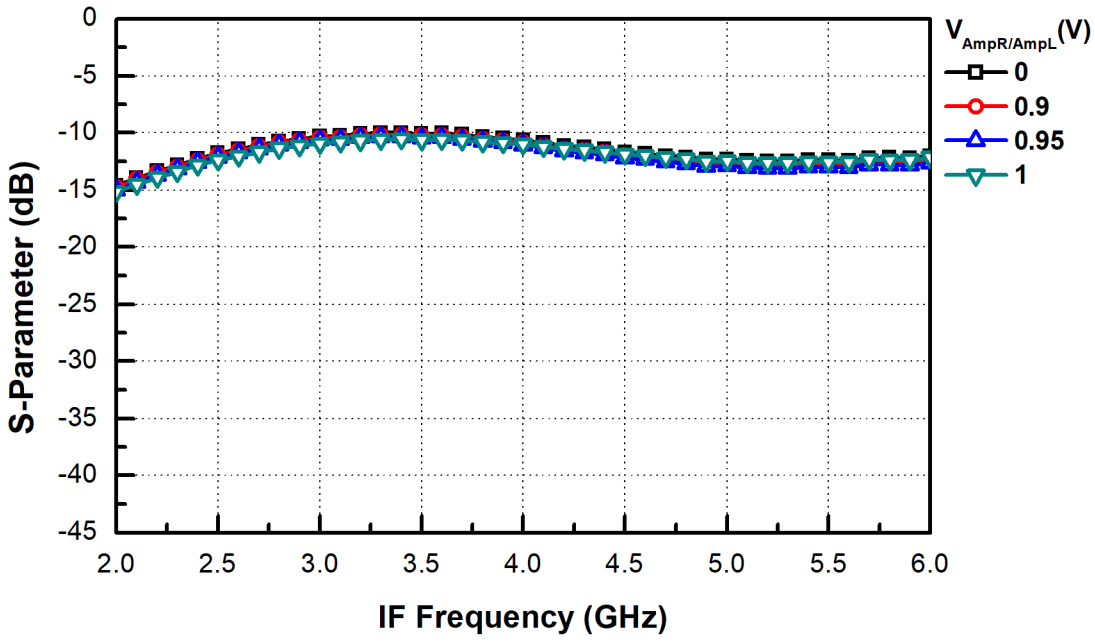


Fig. 3.30 Simulated reflection coefficient (without line E in Fig. 3.27) of the T-type attenuator (forward bias $V_{AmpR/AmpL}$, 0-1 V).

doi:10.6342/NTU202203942

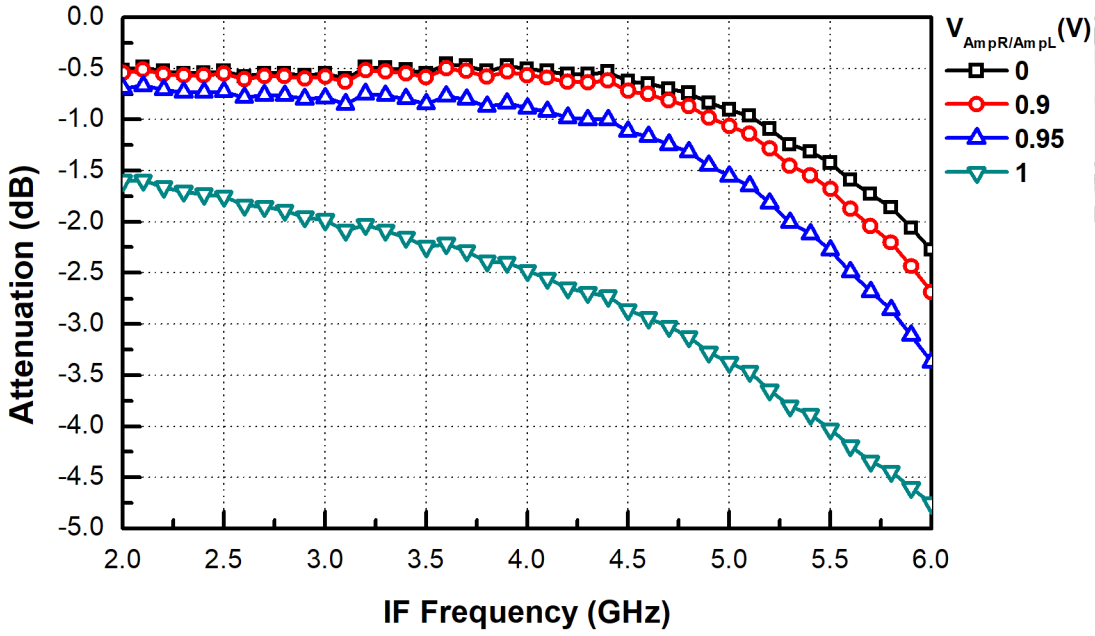


Fig. 3.31 Attenuation's EM simulation of the T-type attenuator (forward bias $V_{AmpR/AmpL}$, 0-1 V).

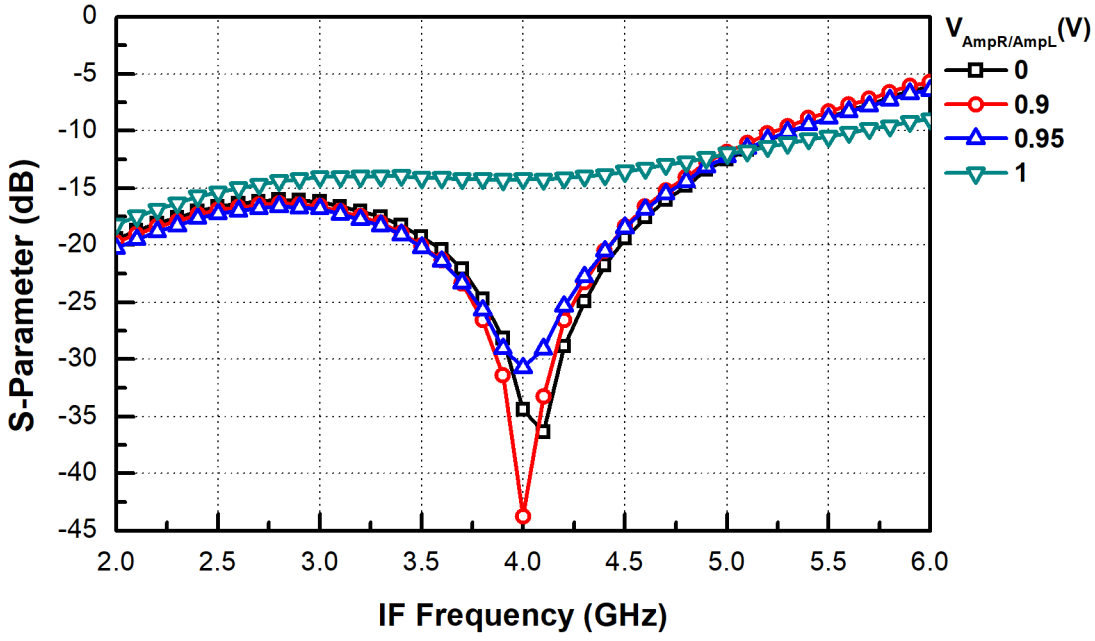


Fig. 3.32 Simulated reflection coefficient of the T-type attenuator (forward bias $V_{AmpR/AmpL}$, 0-1 V).

doi:10.6342/NTU202203942

3.3.5 Simulations of The Tunable I/Q Divider/Combiner

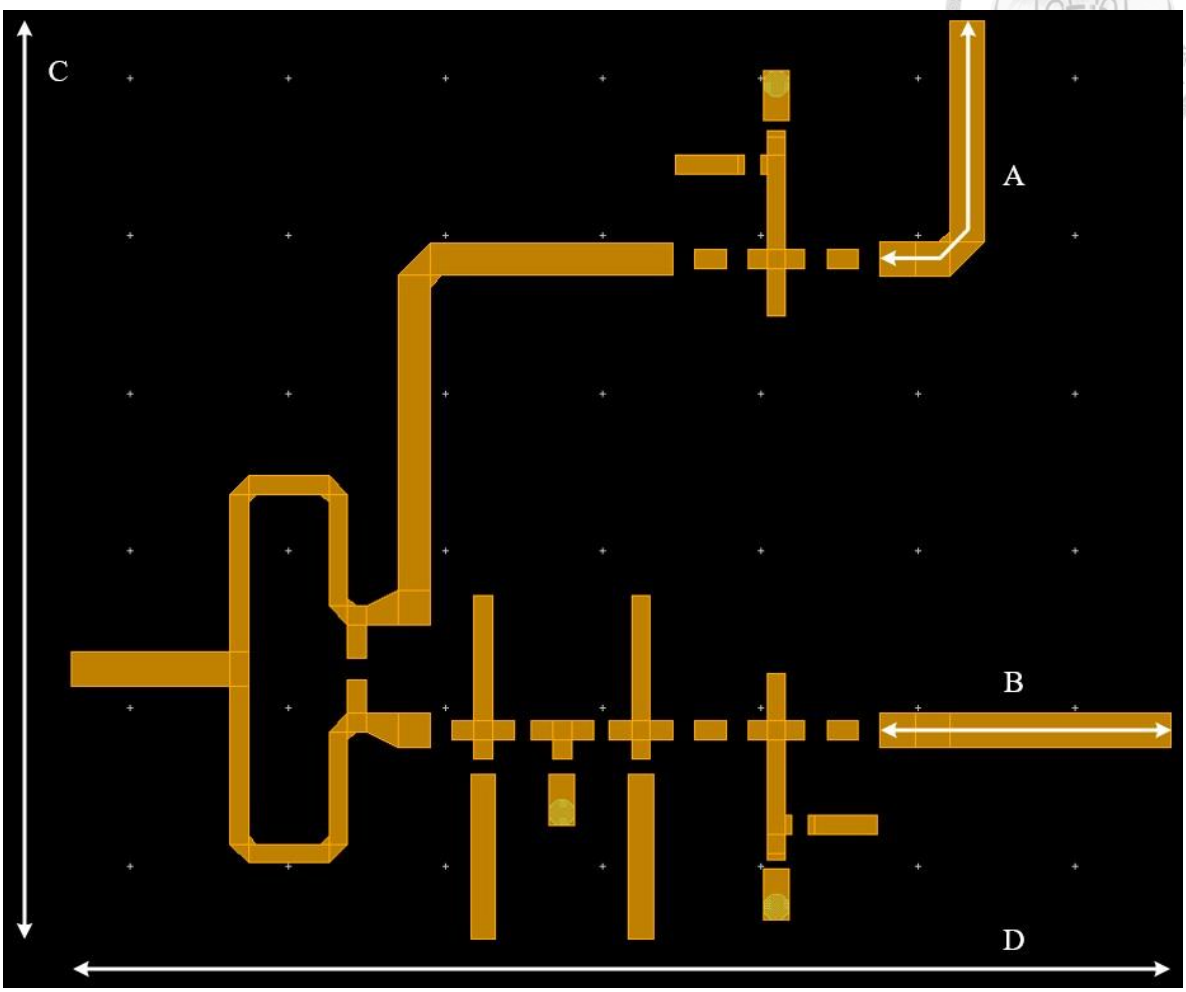


Fig. 3.33 Layout of the tunable I/Q divider/combiner.

The tunable I/Q divider/combiner's layout is shown in Fig. 3.33 and the schematic is shown in Fig. 3.9. Lines A and B are the 50 Ω transmission lines used to solder the SMA connectors. The detailed dimensions are shown in Table 3.5.

doi:10.6342/NTU202203942

Table 3.5 Dimensions of line A/B and length C/D.

Each Part	Length (mm)/ Width (mm)
Line A	10/ 1.1
Line B	10/ 1.1
Length C	29.1
Length D	35.7

When V_{Phase} is 0-6 V, Fig. 3.34 shows the simulated phase difference between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9. In this case, we only have phase tuning; when the phase is close to 90° at 4 GHz, the amplitude imbalance is set close to 0 dB (0.9 V for V_{AmpL} and 0.95 V for V_{AmpR}). From 3.5-4.8 GHz, there are about 80-100° of phase differences that can be tuned, and the reflection coefficients are all less than -10 dB as shown in Fig. 3.35. Fig. 3.36 shows the simulated amplitude imbalance between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 when V_{Phase} is 0-6 V. Without amplitude tuning, the variation of amplitude imbalance does not exceed 0.3 dB at 4 GHz.

doi:10.6342/NTU202203942

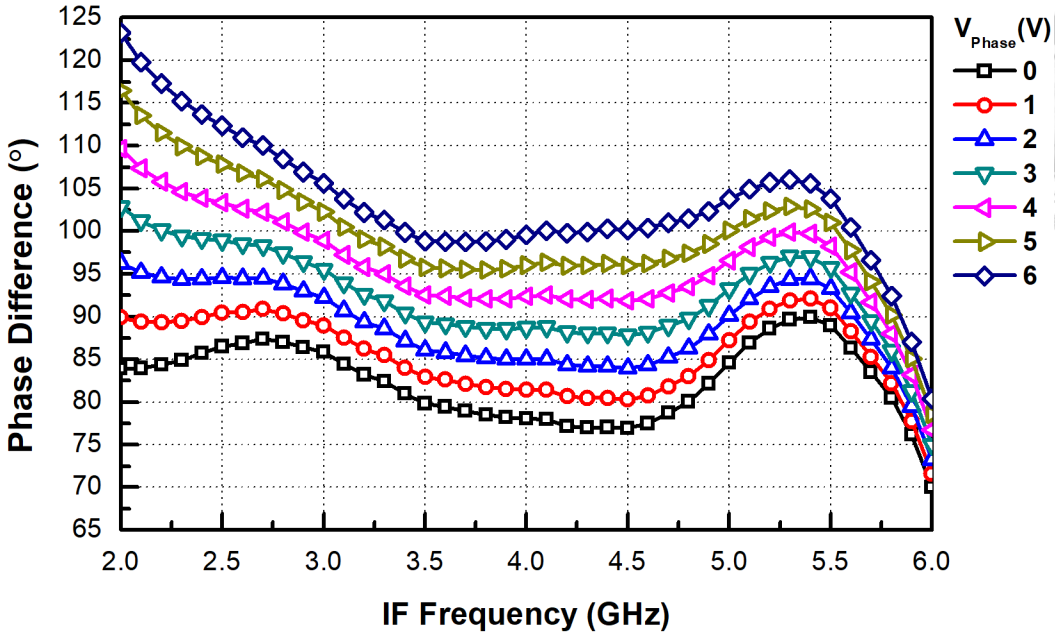


Fig. 3.34 Simulated phase difference between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 (V_X, 0-6 V).

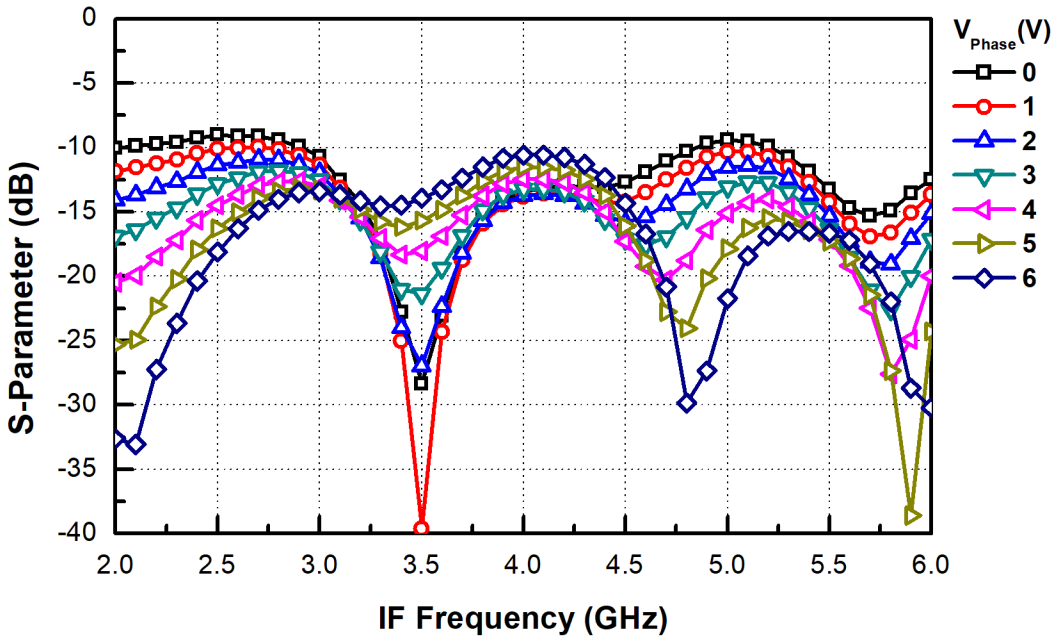


Fig. 3.35 Simulated reflection coefficient of the tunable I/Q divider/combiner's port 3 in Fig. 3.9 V_{Phase}, 0-6 V).

doi:10.6342/NTU202203942

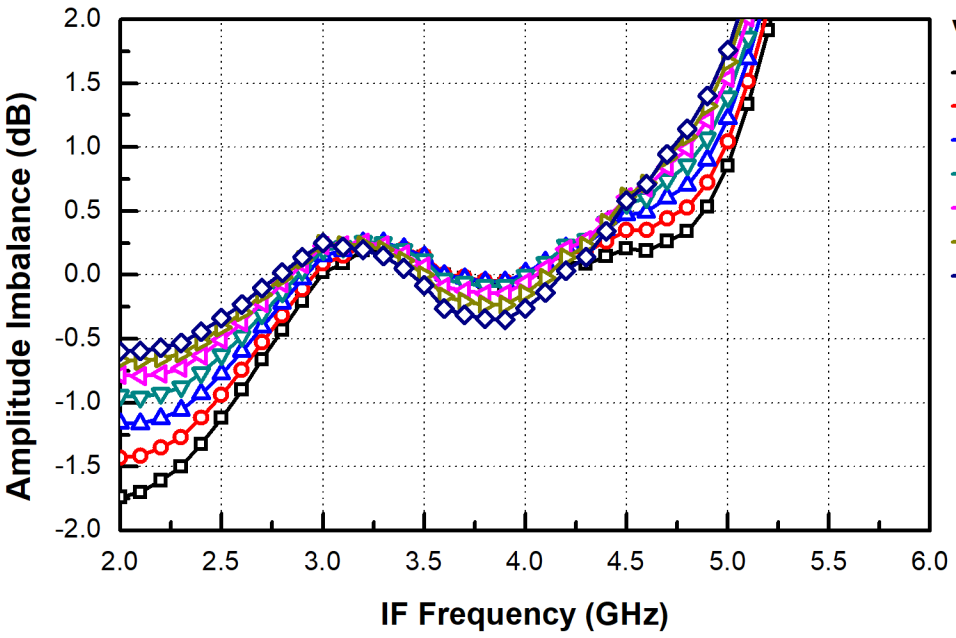


Fig. 3.36 Simulated amplitude imbalance between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 (V_{Phase}, 0-6 V).

When V_{AmpR} is 0.95-1 V, Fig. 3.37 shows the simulated amplitude imbalance between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9. We only have the amplitude tuning of V_{AmpR} in this case, the phase difference is set close to 90° (3.1 V for V_{Phase}) at 4 GHz and V_{AmpL} is 0.9 V. It has a 2 dB amplitude variation at 4 GHz, and the reflection coefficients are all less than -10 dB when V_{AmpR} is 0.95-1 V as shown in Fig. 3.38. Fig. 3.39 shows the simulated phase difference between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 when V_{AmpR} is 0.95-1 V. Without phase tuning, the variation of phase difference does not exceed 7° at 4 GHz.

doi:10.6342/NTU202203942

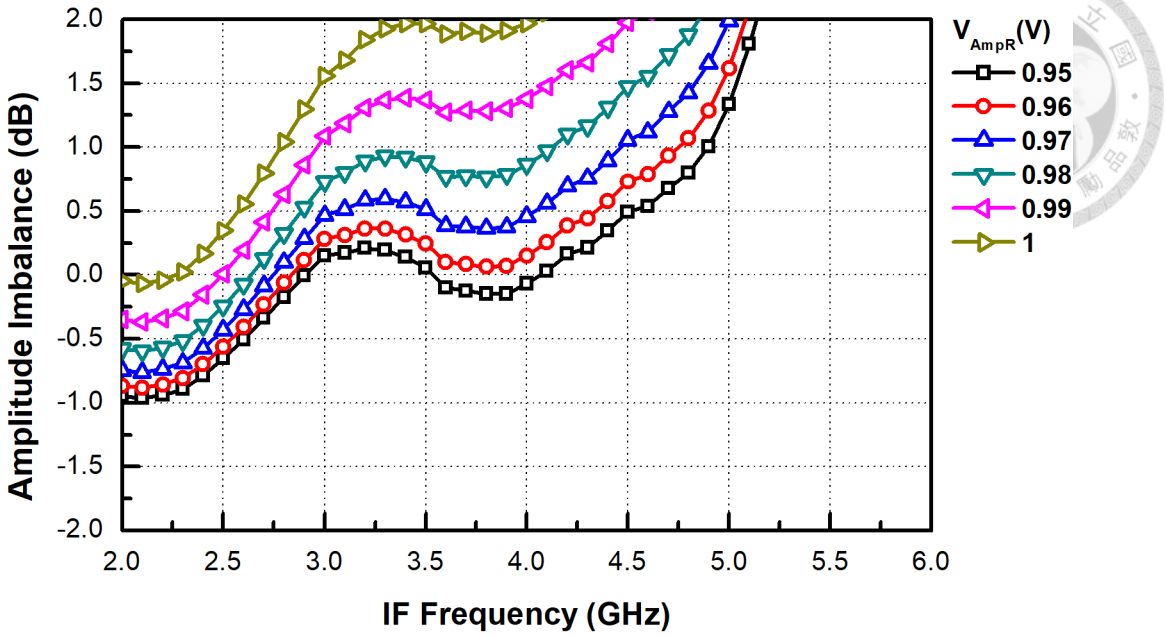


Fig. 3.37 Simulated amplitude imbalance between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 (V_{AmpR}, 0.95-1 V).

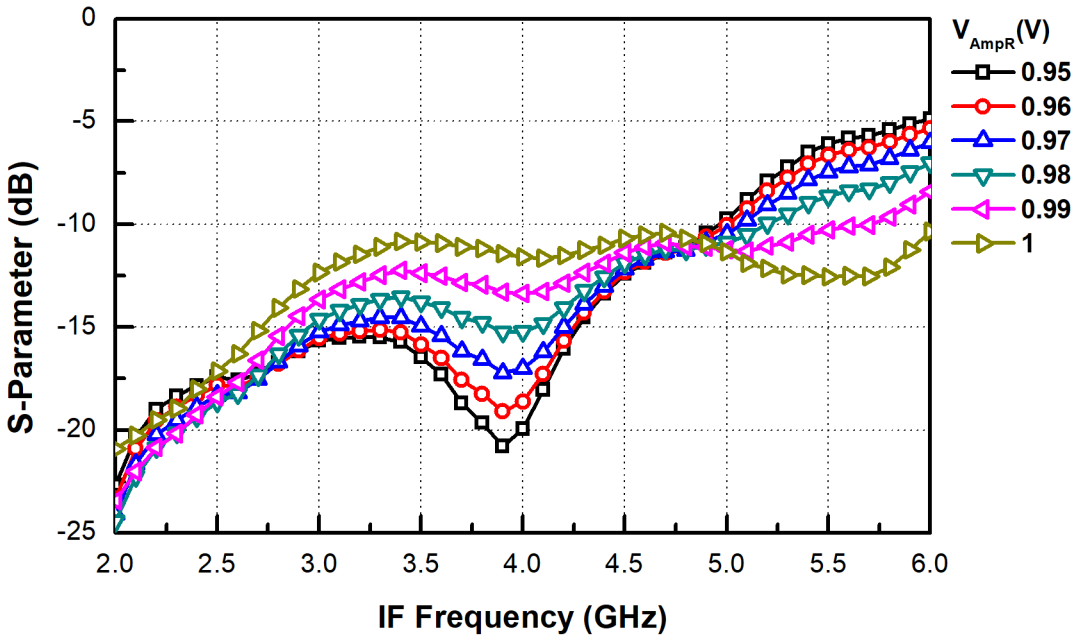


Fig. 3.38 Simulated reflection coefficient of the tunable I/Q divider/combiner's port 2 in Fig. 3.9 (V_{AmpR}, 0.95-1 V).

doi:10.6342/NTU202203942

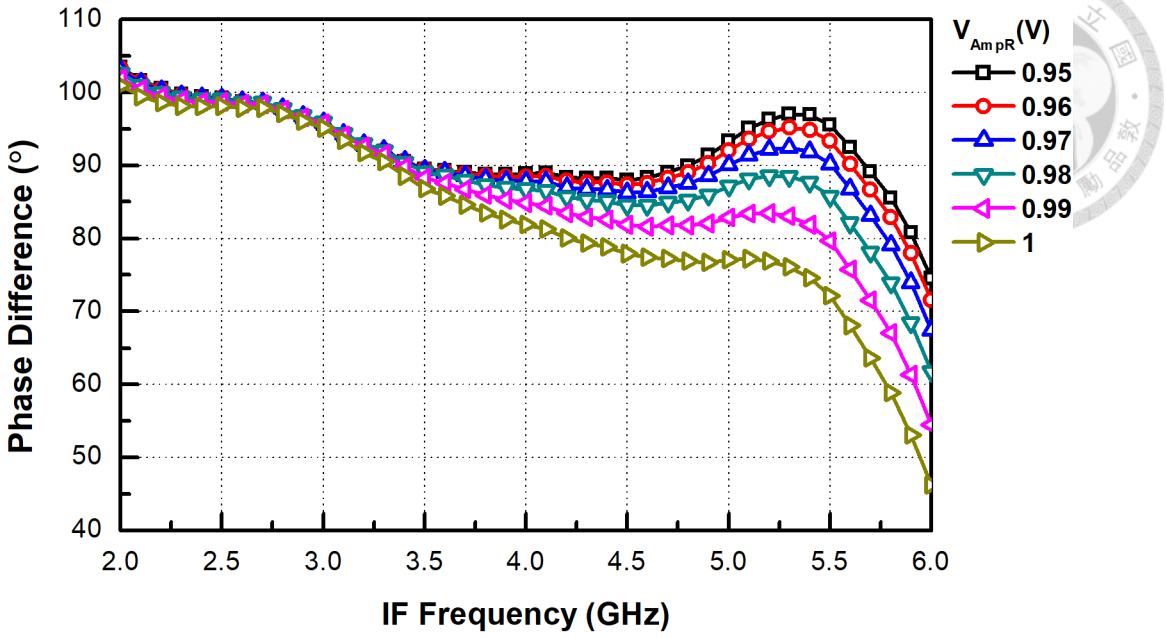


Fig. 3.39 Simulated phase difference between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 (V_{AmpR}, 0.95-1 V).

When V_{AmpL} is 0.9-0.98 V, Fig. 3.40 shows the simulated amplitude imbalance between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9. We only have the amplitude tuning of V_{AmpL} in this case, the phase difference is set close to 90° (3.1 V for V_{Phase}) at 4 GHz and V_{AmpR} is 0.95 V. It has a 1.1 dB amplitude variation at 4 GHz, and the reflection coefficients are all less than -10 dB when V_{AmpL} is 0.9-0.98 V as shown in Fig. 3.41. Fig. 3.42 shows the phase difference between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 when V_{AmpL} is 0.9-0.98 V. Without phase tuning, the variation of phase difference does not exceed 2° at 4 GHz.

doi:10.6342/NTU202203942

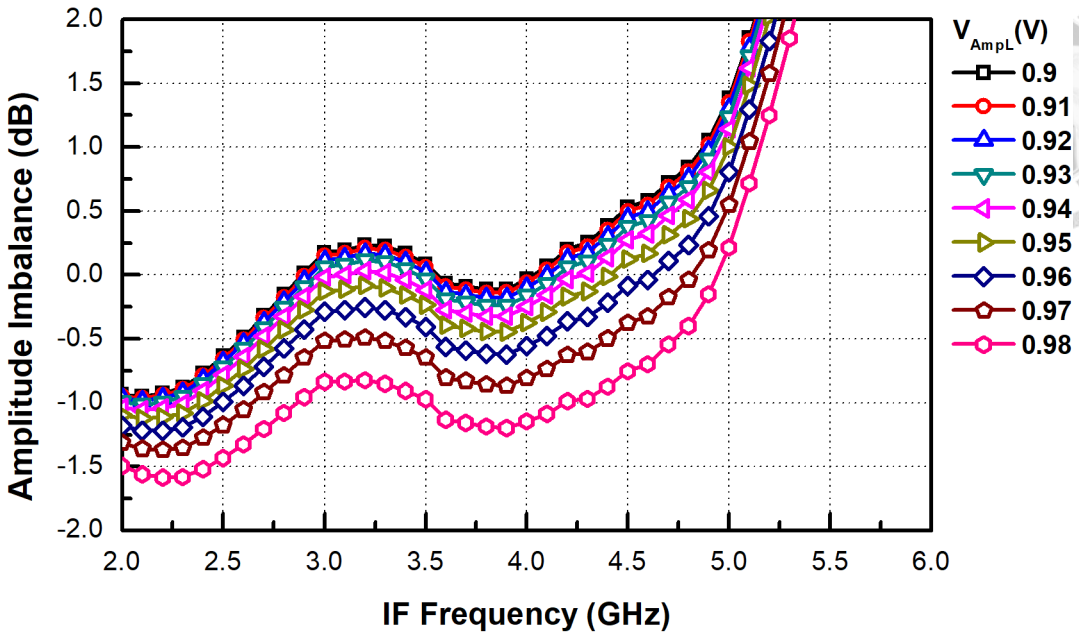


Fig. 3.40 Simulated amplitude imbalance between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 (V_{AmpL}, 0.9-0.98 V).

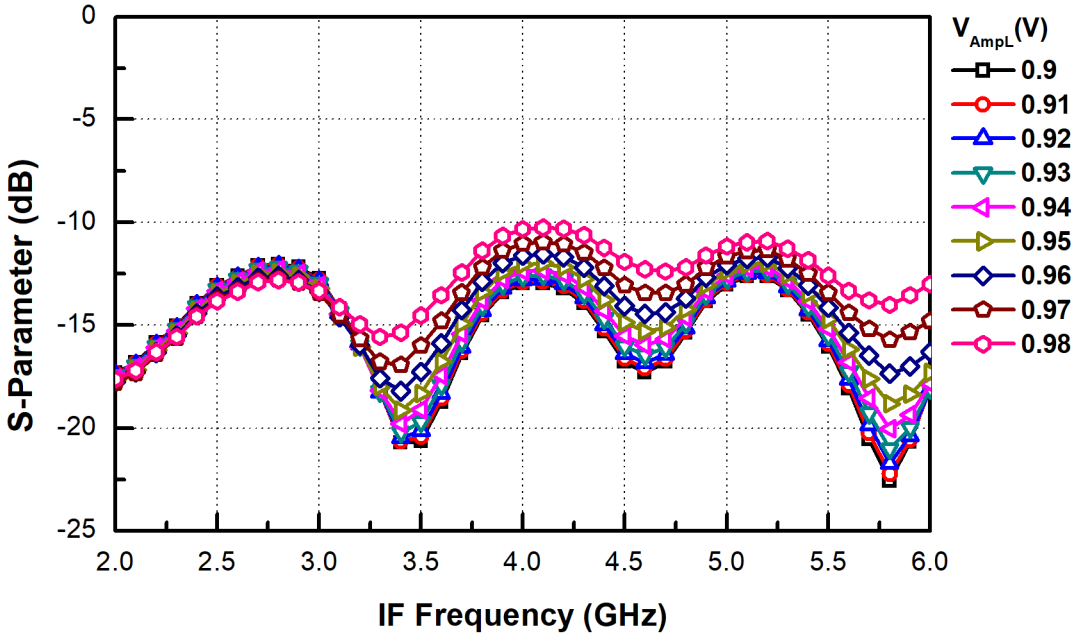


Fig. 3.41 Simulated reflection coefficient of the tunable I/Q divider/combiner's port 3 in Fig. 3.9 (V_{AmpL}, 0.9-0.98 V).

doi:10.6342/NTU202203942

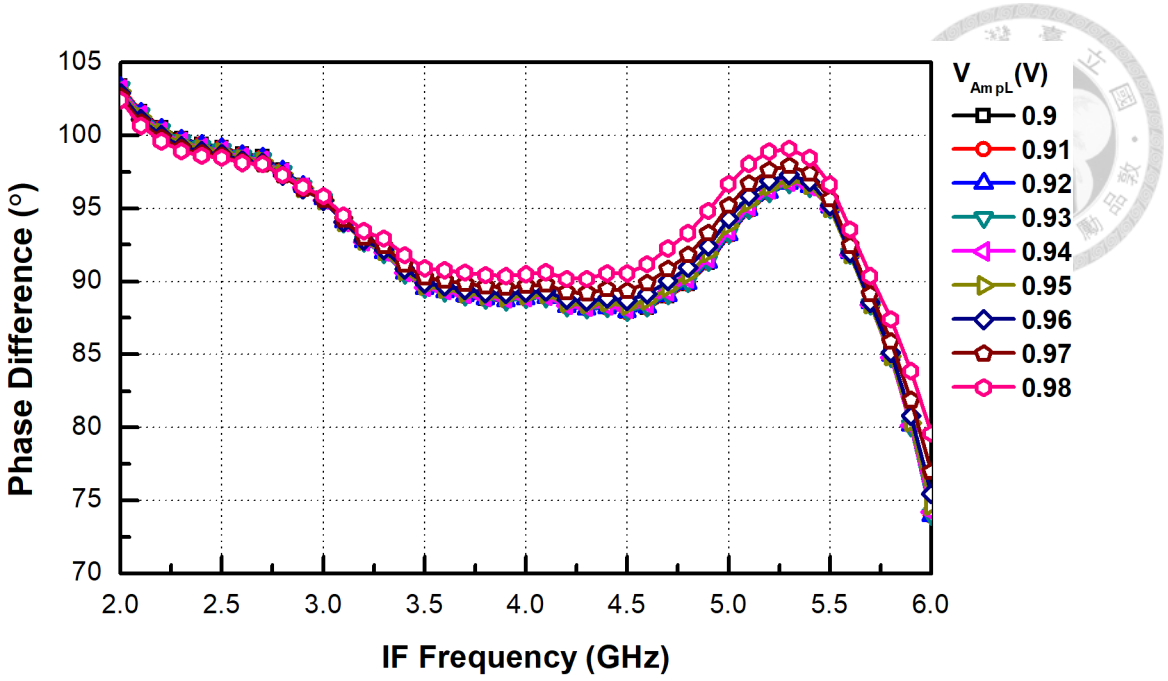


Fig. 3.42 Simulated phase difference between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 (V_{AmpL}, 0.9-0.98 V).

The simulated phase difference and amplitude imbalance between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 with a (-20)-10 dBm power sweep (at 4 GHz) are shown in Fig. 3.43 and Fig. 3.44, respectively. The phase difference is about 10° if the power has to be driven to 6 dBm. The amplitude imbalance is about 0.9 dB if the power has to be driven to -4 dBm. The simulated S-parameter of the tunable I/Q divider/combiner in Fig. 3.9 with a (-20)-10 dBm power sweep (at 4 GHz) is shown in Fig. 3.45. If the power is over 4 dBm, $|S_{22}|$ and $|S_{33}|$ will be greater than -10 dB. Even if the employment of varactors and PIN diodes causes the tunable I/Q divider/combiner's phase and amplitude to vary considerably under high power operation, the tuning function might compensate.

doi:10.6342/NTU202203942

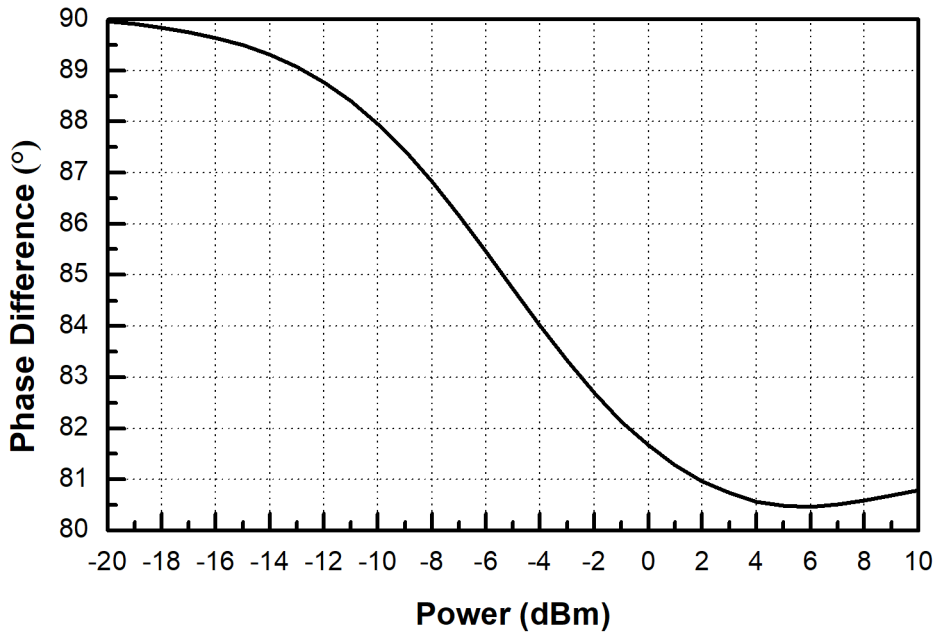


Fig. 3.43 Simulated phase difference between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 with a (-20)-10 dBm power sweep (at 4 GHz).

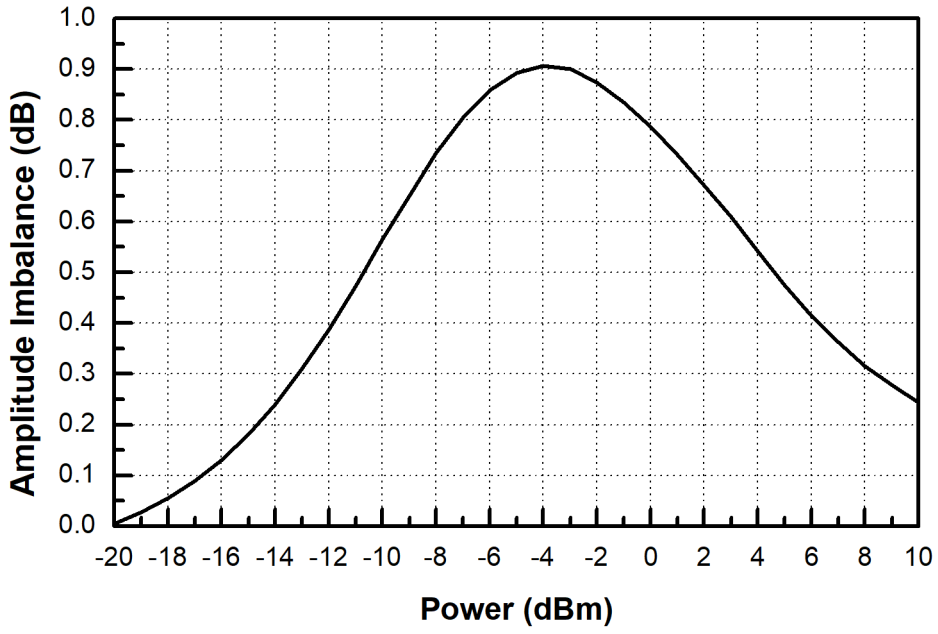


Fig. 3.44 Simulated amplitude imbalance between the tunable I/Q divider/combiner's port 2,3 in Fig. 3.9 with a (-20)-10 dBm power sweep (at 4 GHz).

doi:10.6342/NTU202203942

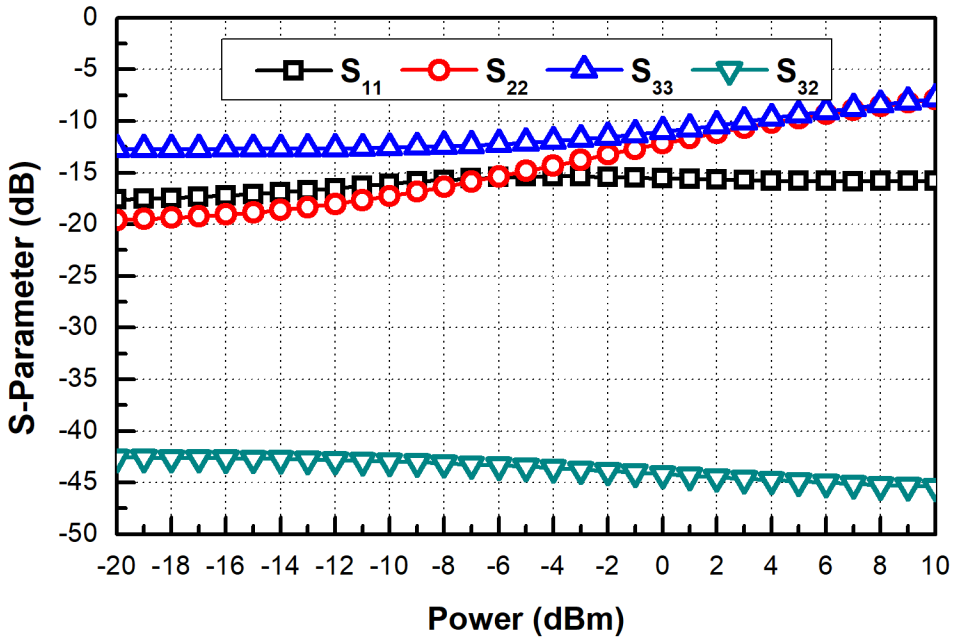


Fig. 3.45 Simulated S-parameter ($S_{11,22,33,32}$) of the tunable I/Q divider/combiner in Fig. 3.9 with a (-20)-10 dBm power sweep (at 4 GHz).

3.4 Experimental Results

3.4.1 Millimeter Wave Up-/Down-Conversion Image Rejection Module

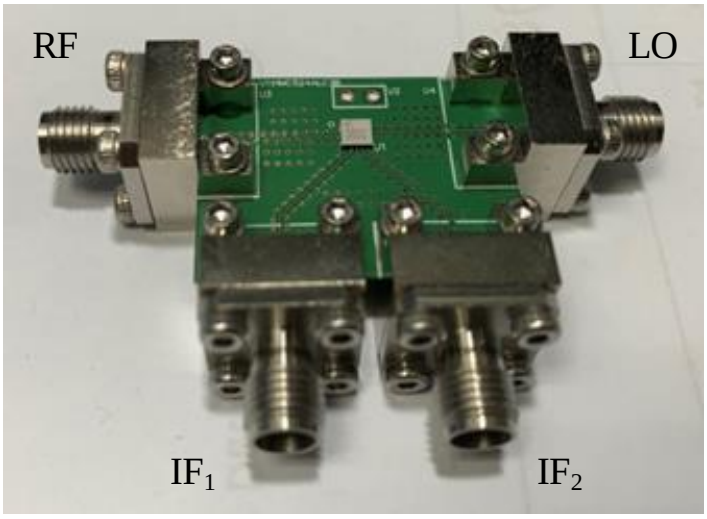


Fig. 3.46 HMC524ALC3B (mixer) evaluation board with 2.92 mm end launch connectors.

doi:10.6342/NTU202203942

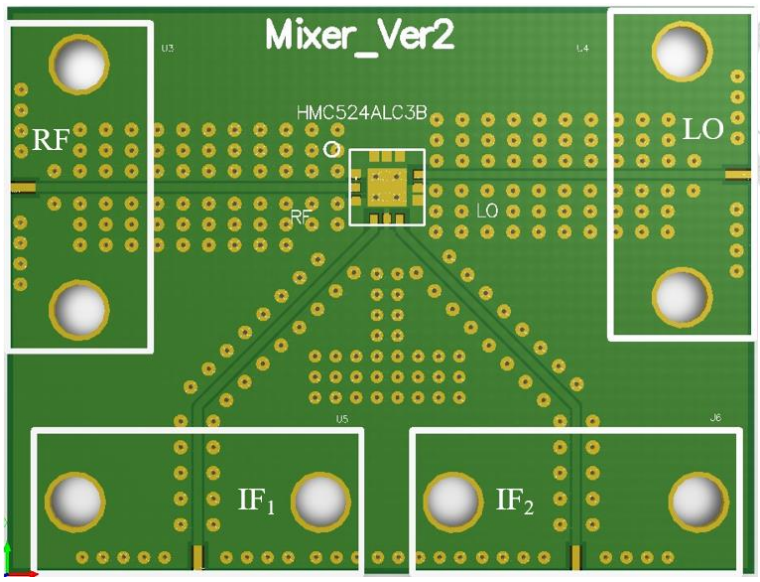


Fig. 3.47 HMC524ALC3B (mixer) evaluation board's layout.

The HMC524ALC3B (mixer) evaluation board with 2.92 mm end launch connectors is shown in Fig. 3.46 and its layout is shown in Fig. 3.47. To measure large signals, we use an Agilent E8257D (250 kHz- 67 GHz) signal generator for RF/IF signal, a KEYSIGHT E8267D (250 kHz- 44 GHz) signal generator for LO signal, and an Agilent E4448A (3 Hz- 50 GHz) spectrum analyzer to measure large signals (RF/IF output power). According to the datasheet [12], the conversion gain is calculated as IF_1 power minus RF power (down-conversion) or RF power minus IF_1 power (up-conversion) in dBm, and the IF_2 port is connected to the 50 Ω termination. Besides, with the conversion gain's definition G (dB) of the mixer core in Fig. 3.48, we can obtain IF power minus RF power (or RF power minus IF power) as G dB and IF_1 power minus RF power (or RF power minus IF_1 power) as (G-3) dB if we connect an ideal IF divider/combiner, and assume that the RF divider/combiner is also ideal (the datasheet does not mention its insertion loss).

doi:10.6342/NTU202203942

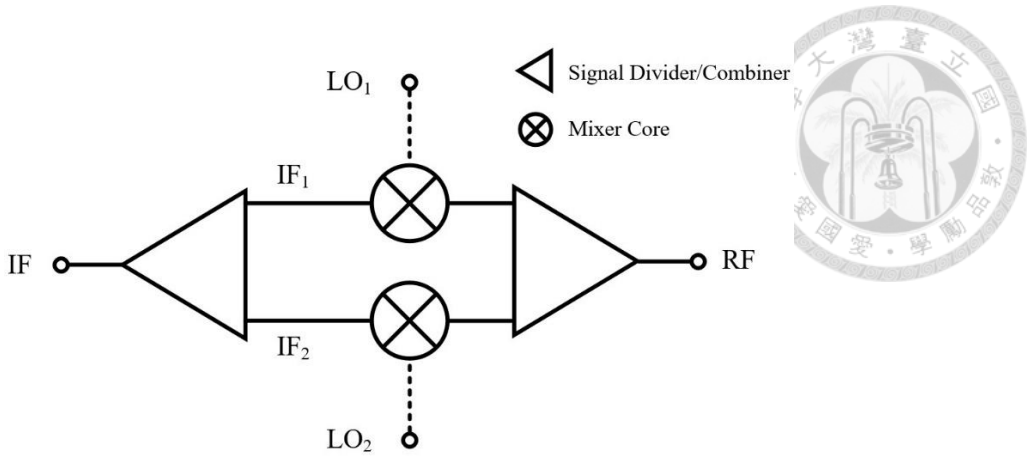


Fig. 3.48 Measured calculation's schematic of conversion gain.

The measured conversion gain vs. LO power of the HMC524ALC3B (mixer) evaluation board is shown in Fig. 3.49 when RF frequency is 28 GHz, LO frequency is 25 GHz, and IF frequency is 3 GHz. When the LO power is greater than 14 dBm, both up-/down-conversion have maximum conversion gain (-5 dB for up-conversion and -8.2 dB for down-conversion).

The measured IP_{1dB} of the HMC524ALC3B (mixer) evaluation board is shown in Fig. 3.50 when RF frequency is 28 GHz, LO frequency is 25 GHz, IF frequency is 3 GHz, and LO power is 14 dBm. Up-conversion is about 2 dBm and down-conversion is about 11 dBm.

The measured bandwidth of the HMC524ALC3B (mixer) evaluation board is shown in Fig. 3.51 when LO frequency is 25 GHz and LO power is 14 dBm. The conversion gain range of up-conversion is 0.5 dB and the conversion gain range of down-conversion is 0.8 dB from 2.5-5 GHz.

doi:10.6342/NTU202203942

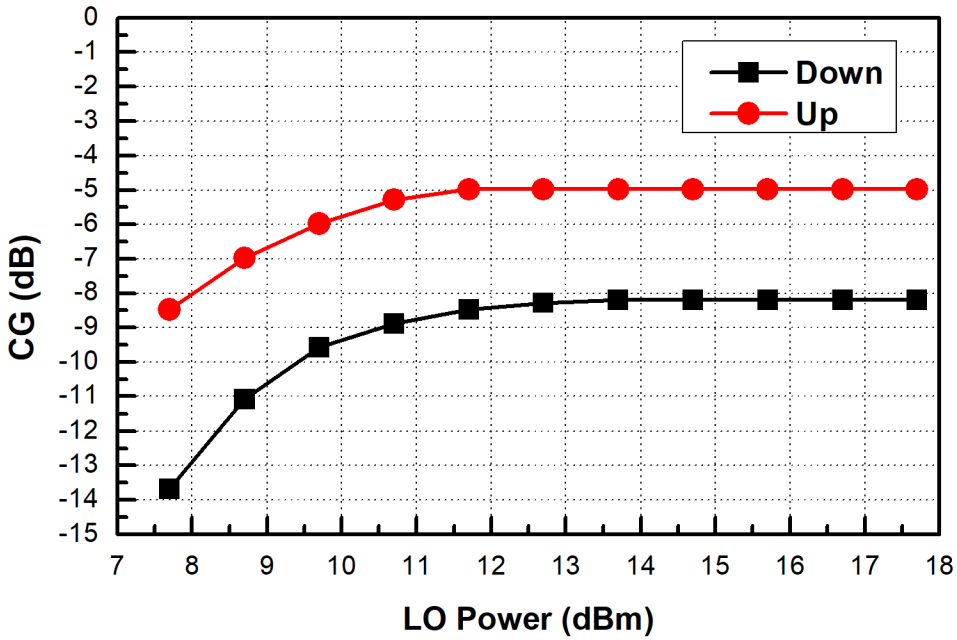


Fig. 3.49 Measured conversion gain (CG) vs. LO power of the HMC524ALC3B (mixer) evaluation board (up-/down-conversion).

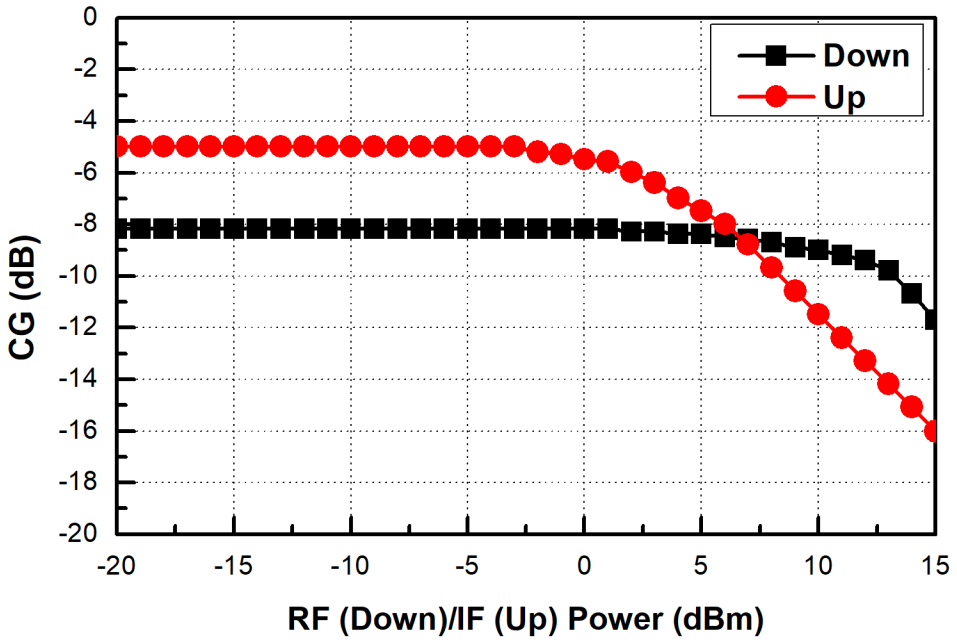


Fig. 3.50 Measured conversion gain (CG) vs. RF (down-conversion)/IF (up-conversion) power of the HMC524ALC3B (mixer) evaluation board.

doi:10.6342/NTU202203942

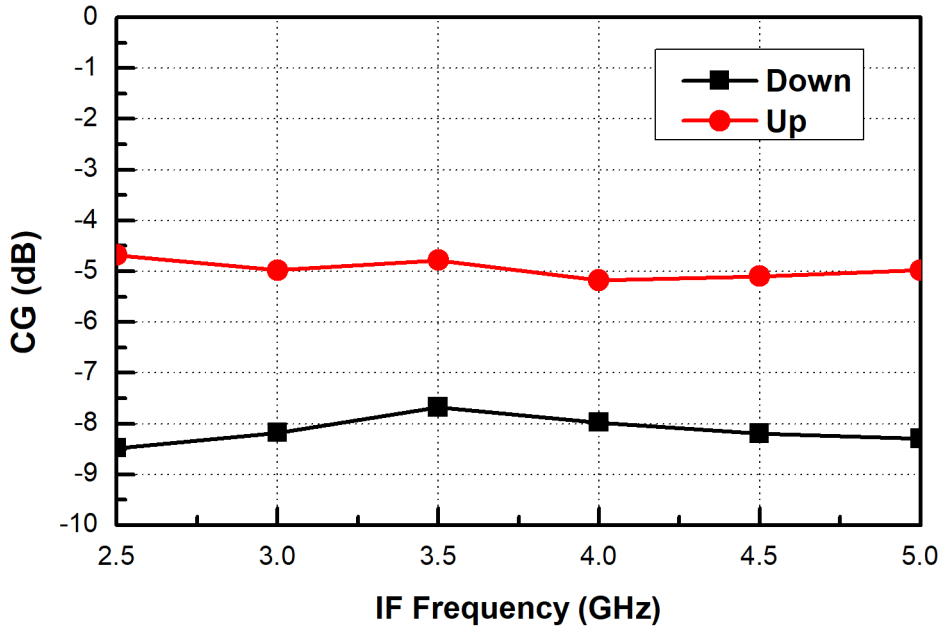


Fig. 3.51 Measured conversion gain (CG) vs. bandwidth of HMC524ALC3B (mixer) evaluation board (up-/down-conversion).

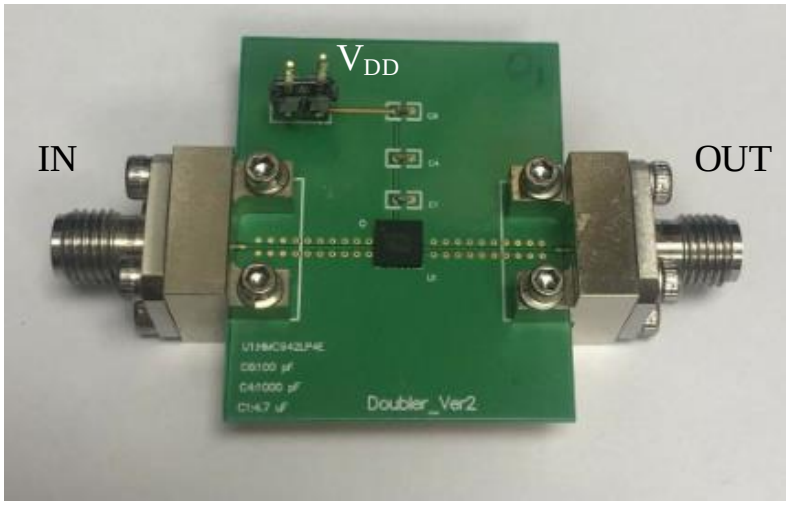


Fig. 3.52 HMC942LP4E (doubler) evaluation board with 2.92 mm end launch connectors.

doi:10.6342/NTU202203942

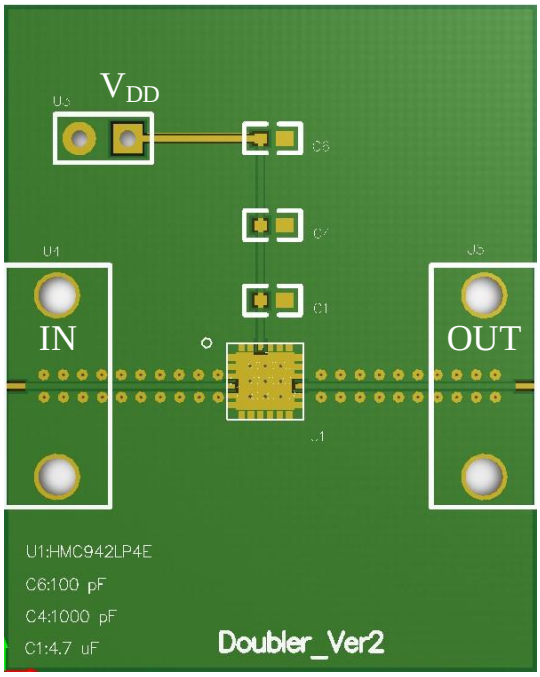


Fig. 3.53 HMC942LP4E (doubler) evaluation board's layout.

The HMC942LP4E (doubler) evaluation board with 2.92 mm end launch connectors is shown in Fig. 3.52 and its layout is shown in Fig. 3.53. We use a KEYSIGHT E8267D (250 kHz- 44 GHz) signal generator for IN signal, an Agilent E4448A (3 Hz- 50 GHz) spectrum analyzer to measure the OUT signal, and a GWINSTEK PST-3202 (32 V,2 A x2/6 V, 5 A x1) power supply for DC supplying (V_{DD}).

The measured IN (12.5 GHz) power vs. OUT (25 GHz) power of the HMC942LP4E (doubler) evaluation board is shown in Fig. 3.54. When the IN power is greater than 2 dBm, it has an OUT power greater than 14 dBm. When the IN power is greater than 8 dBm, it has an OUT power greater than 17 dBm.

doi:10.6342/NTU202203942

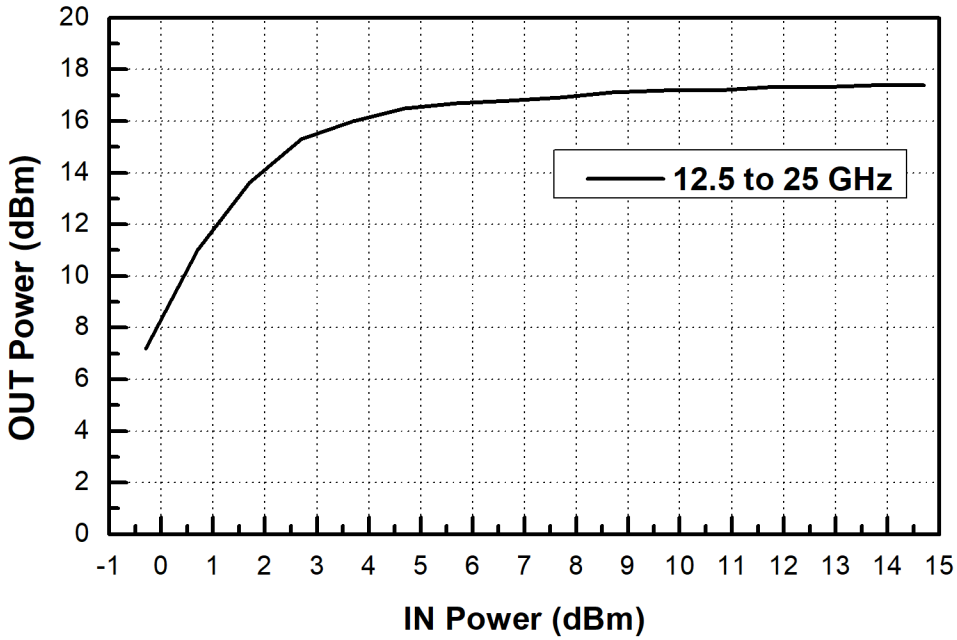


Fig. 3.54 Measured IN (12.5 GHz) power vs. OUT (25 GHz) power of the HMC942LP4E (doubler) evaluation board.

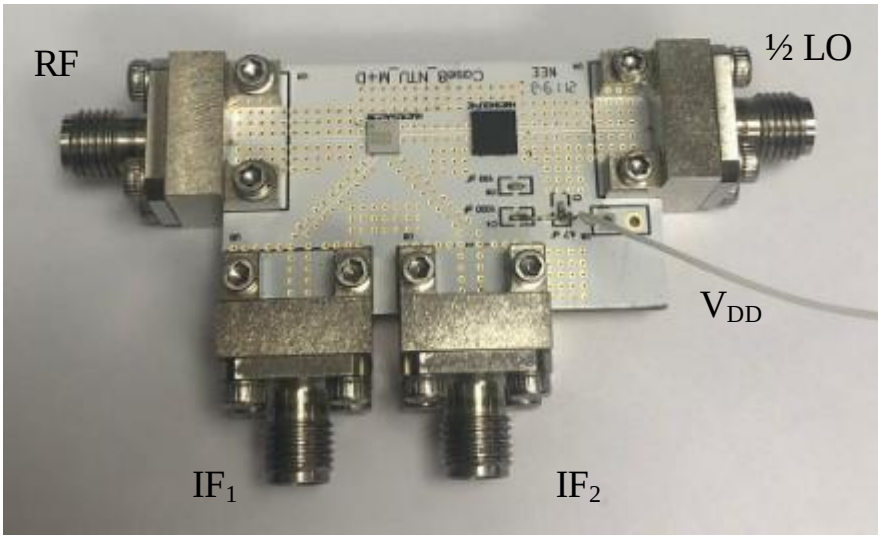


Fig. 3.55 Millimeter-wave up-/down-conversion image rejection module evaluation board (board 1 in Fig. 3.4) with 2.92 mm end launch connectors.

doi:10.6342/NTU202203942

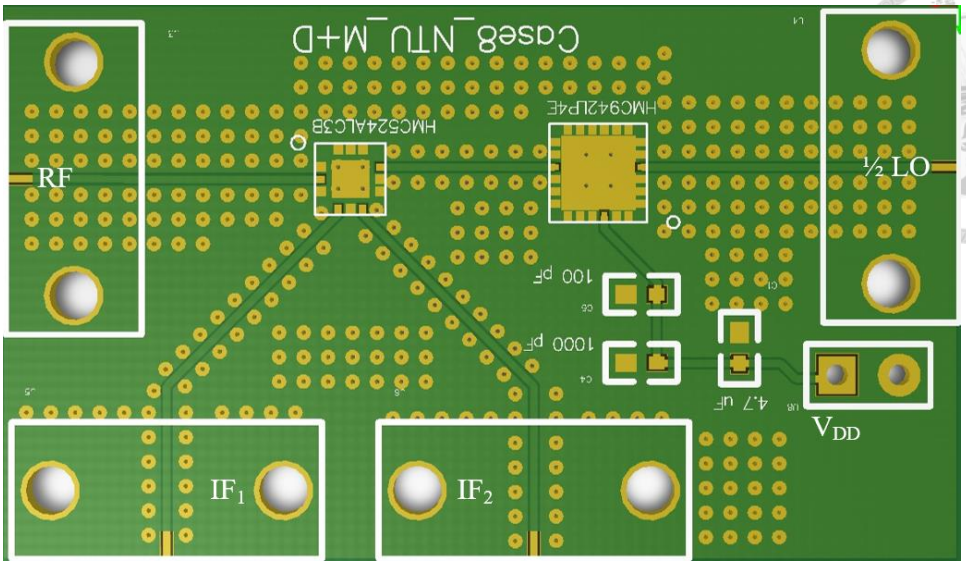


Fig. 3.56 Millimeter-wave up-/down-conversion image rejection module evaluation board's (board 1 in Fig. 3.4) layout.

The millimeter-wave up-/down-conversion image rejection module evaluation board (board 1 in Fig. 3.4) with 2.92 mm end launch connectors is shown in Fig. 3.55 and its layout is shown in Fig. 3.56. The 1/2 LO signal is the same as the IN signal in Fig. 3.52. When giving a signal greater than 2 dBm at 12.5 GHz into the 1/2 LO port, there will be a signal greater than 14 dBm at 25 GHz fed into the LO port in Fig. 3.46. The up-/down-conversion mixer will operate with maximum conversion gain.

doi:10.6342/NTU202203942

3.4.2 Tunable I/Q Divider/Combiner

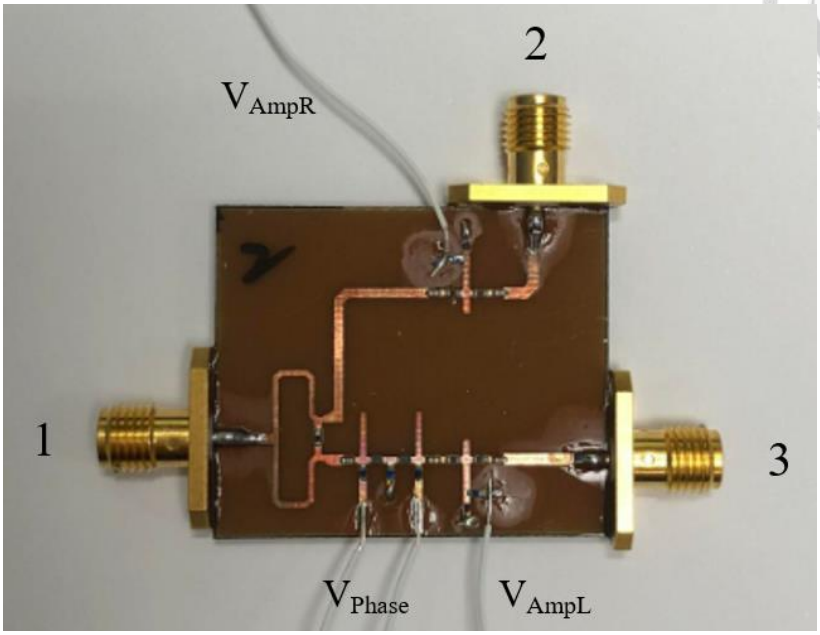


Fig. 3.57 Tunable I/Q divider/combiner with SMA connectors.

The tunable I/Q divider/combiner with SMA connectors is shown in Fig. 3.57. We use an Agilent N5230A (300 kHz- 20 GHz) 4 ports network analyzer to measure S-parameters and a GWINSTEK PST-3202 (32 V,2 A x2/6 V, 5 A x1) power supply for DC supplying (V_{Phase} and $V_{AmpR/AmpL}$). We will present the measurement of three samples with phase differences of 80, 90, and 100° from 2.5-5 GHz (0.5 GHz per step). Each phase difference's measurement status is an amplitude imbalance close to 0 dB.

The S-parameters measurement of sample #1,2,3 and EM simulation of the tunable I/Q divider/combiner when the phase has a 90° tuning and amplitude imbalance is close to 0 dB for each frequency (2.5-5 GHz) are shown in Fig. 3.58- Fig. 3.63. Port numbers are shown in Fig. 3.57. $|S_{11}|$ of three samples is less than -13.7 dB from 2.5-5 GHz. $|S_{22}|$ of three samples is less than -12.4 dB from 2.5-4.5 GHz. $|S_{33}|$ of three samples is less than -10 dB from 3-5 GHz. $|S_{32}|$ of three samples is less than -19 dB from 2.5-5 GHz. $|S_{21}|$ and $|S_{31}|$ of three samples

doi:10.6342/NTU202203942

are both between (-4.7)-(-6.4) dB from 2.5-5 GHz. The detailed phase control voltages (V_{Phase}) are shown in Table 3.6.

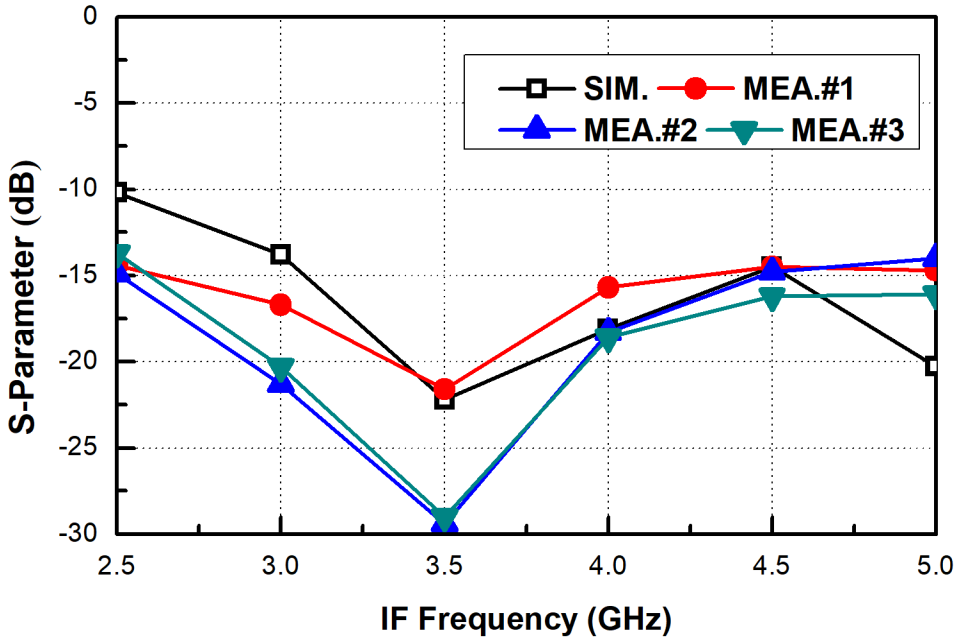
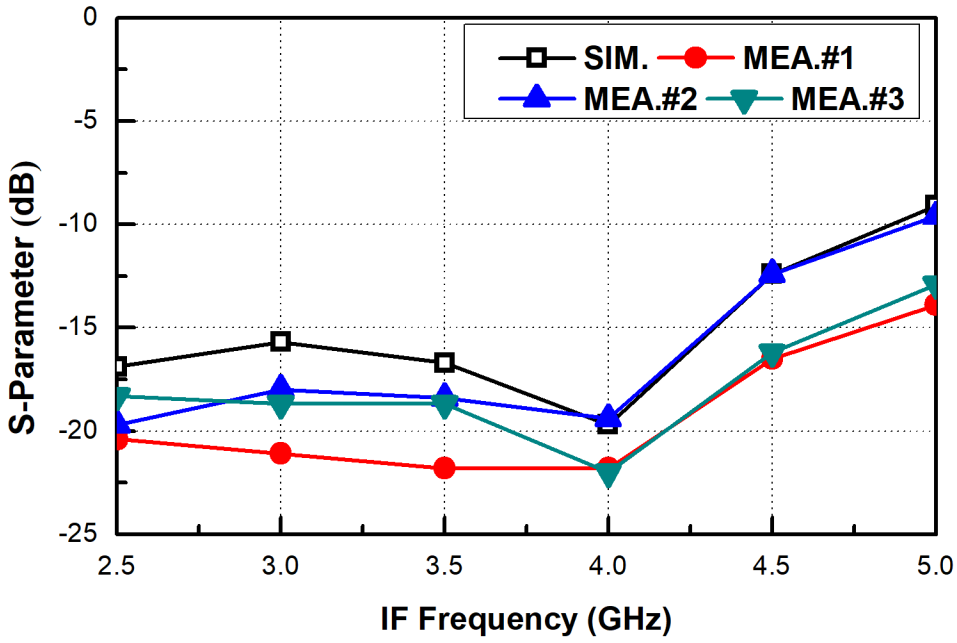


Fig. 3.58 S-parameter (S_{11}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 1 in Fig. 3.57 (90°, 2.5-5 GHz).



doi:10.6342/NTU202203942

Fig. 3.59 S-parameter (S_{22}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 2 in Fig. 3.57 (90°, 2.5-5 GHz).

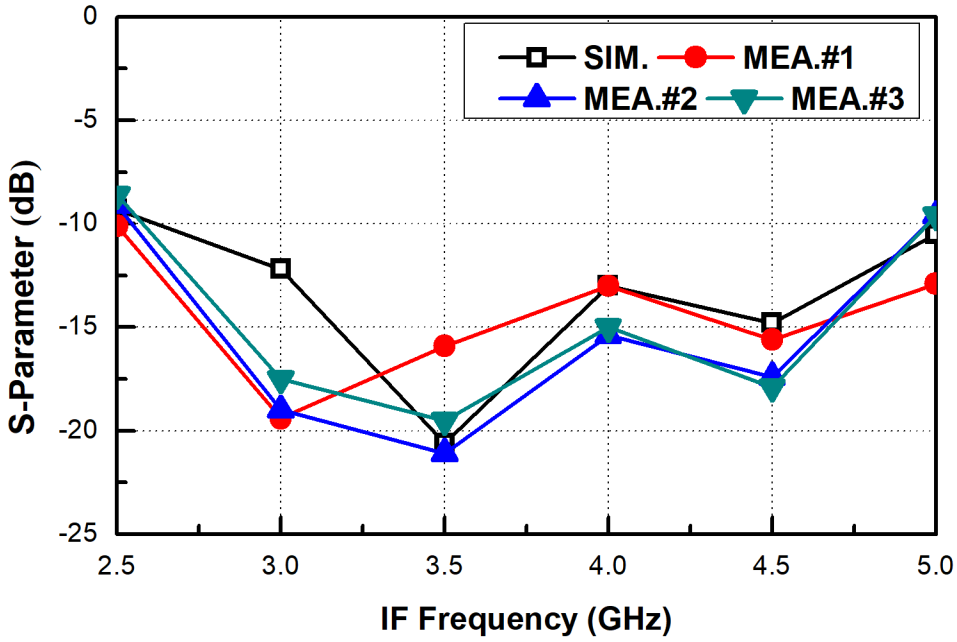
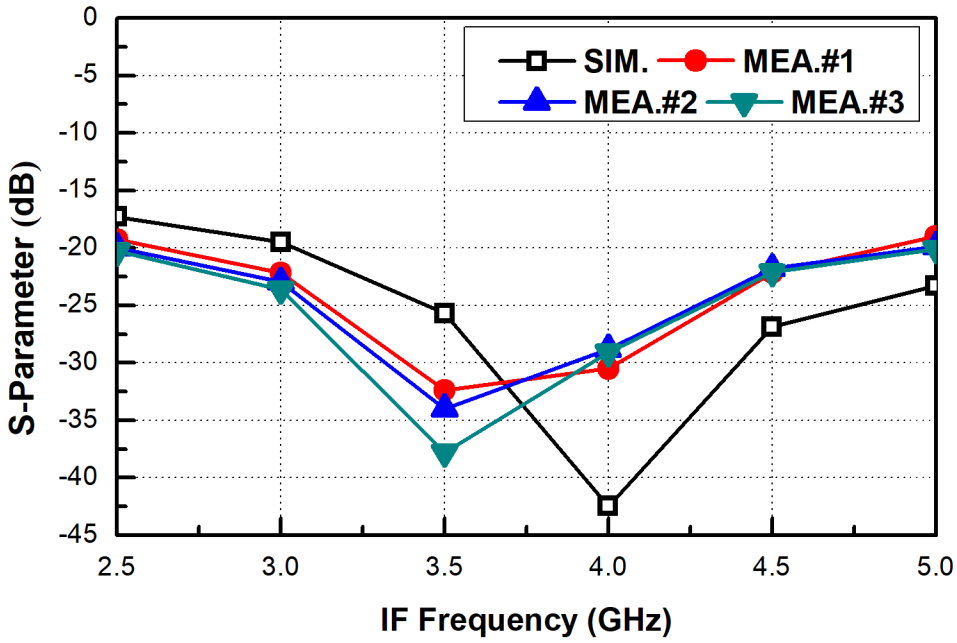


Fig. 3.60 S-parameter (S_{33}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 3 in Fig. 3.57 (90°, 2.5-5 GHz).



doi:10.6342/NTU202203942

Fig. 3.61 S-parameter (S_{32}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 2,3 in Fig. 3.57 (90°, 2.5-5 GHz).

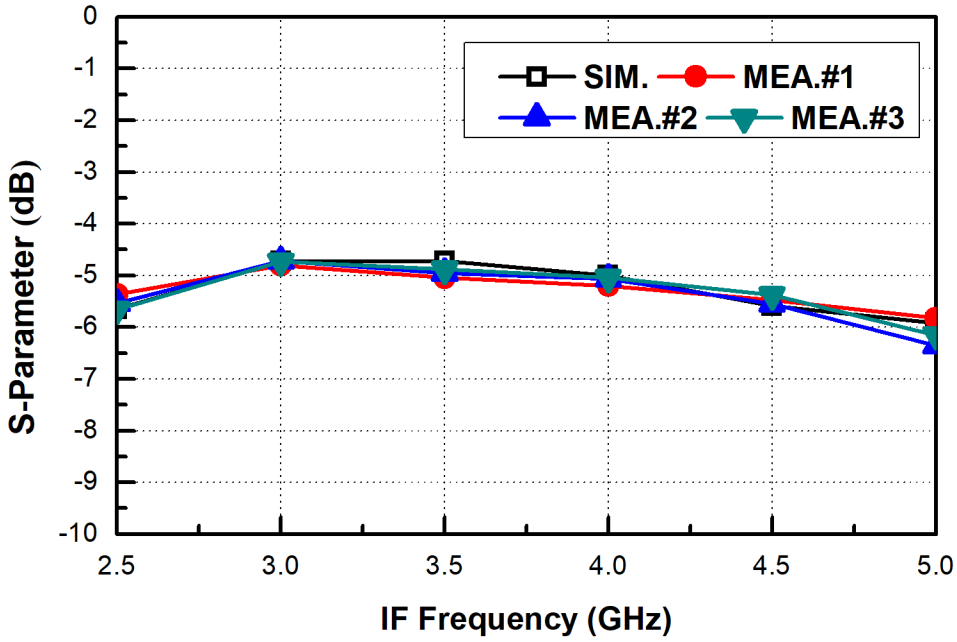
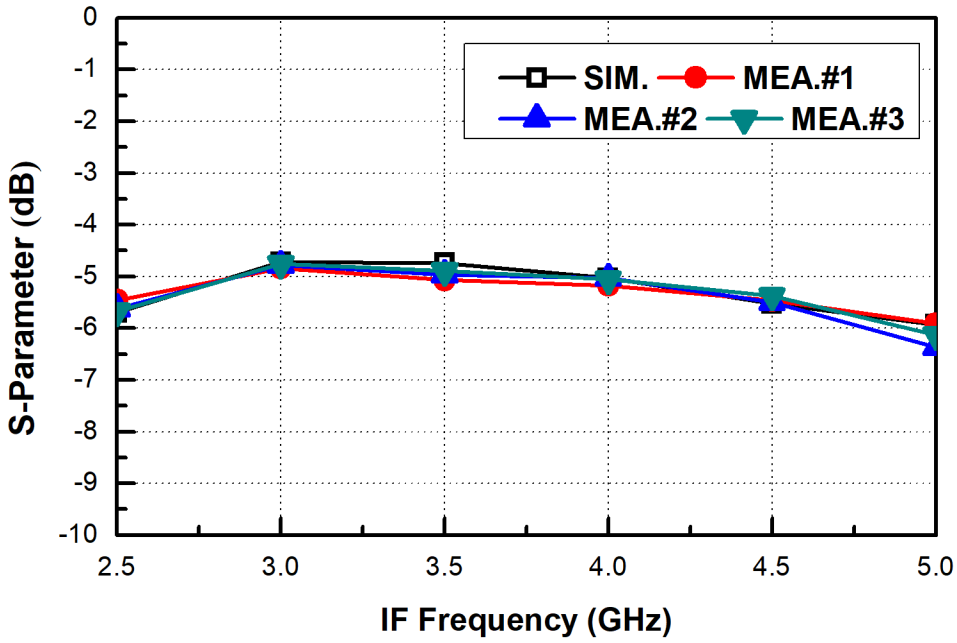


Fig. 3.62 S-parameter (S_{21}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 1,2 in Fig. 3.57 (90°, 2.5-5 GHz).



doi:10.6342/NTU202203942

Fig. 3.63 S-parameter (S_{31}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 1,3 in Fig. 3.57 (90°, 2.5-5 GHz).

Table 3.6 V_{Phase} of 3 samples when the phase is 90° and amplitude imbalance is close to 0 dB from 2.5-5 GHz.

90°_Freq. (GHz)	#1's V_{Phase} (V)	#2's V_{Phase} (V)	#3's V_{Phase} (V)
2.5	0.8	0.2	0.16
3	3	2	2
3.5	4.1	3	3.1
4	4.2	3	3.1
4.5	4.48	3.1	3.35
5	4.16	1.6	1.87

The S-parameters measurement of sample #1,2,3 and EM simulation of the tunable I/Q divider/combiner when the phase has an 80° tuning and amplitude imbalance is close to 0 dB for each frequency (2.5-5 GHz) are shown in Fig. 3.64- Fig. 3.69. Port numbers are shown in Fig. 3.57. Samples #2 and #3 have no data at 2.5 GHz because V_{Phase} can't be less than 0 V. Samples #2 and 3 have no data at 5 GHz since their $|S_{33}|$ is greater than -10 dB. $|S_{11}|$ of three samples is less than -13.4 dB from 2.5-5 GHz. $|S_{22}|$ of three samples is less than -11.8 dB from 2.5-5 GHz. $|S_{33}|$ of sample #1 is less than -10.2 dB from 2.5-5 GHz. $|S_{33}|$ of sample #2 and #3 is less than -12.9 dB from 3-4.5 GHz. $|S_{32}|$ of three samples is less than -19.8 dB from 2.5-5 GHz. $|S_{21}|$ and $|S_{31}|$ of three samples are both between (-4.8)-(-6.6) dB from 2.5-5 GHz. The detailed phase control voltages (V_{Phase}) are shown in Table 3.7.

doi:10.6342/NTU202203942

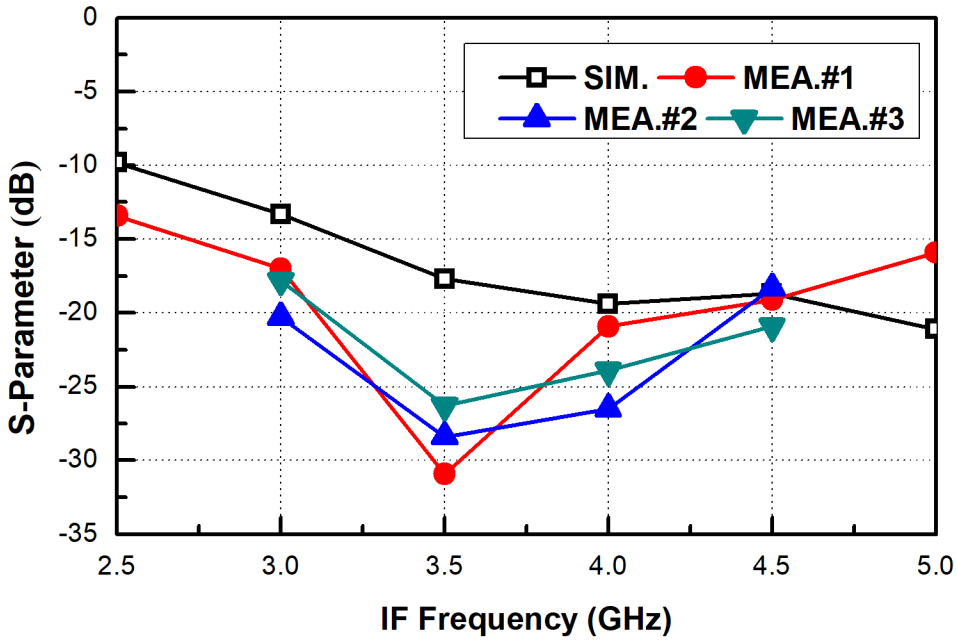


Fig. 3.64 S-parameter (S_{11}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 1 in Fig. 3.57 (80°, 2.5-5 GHz).

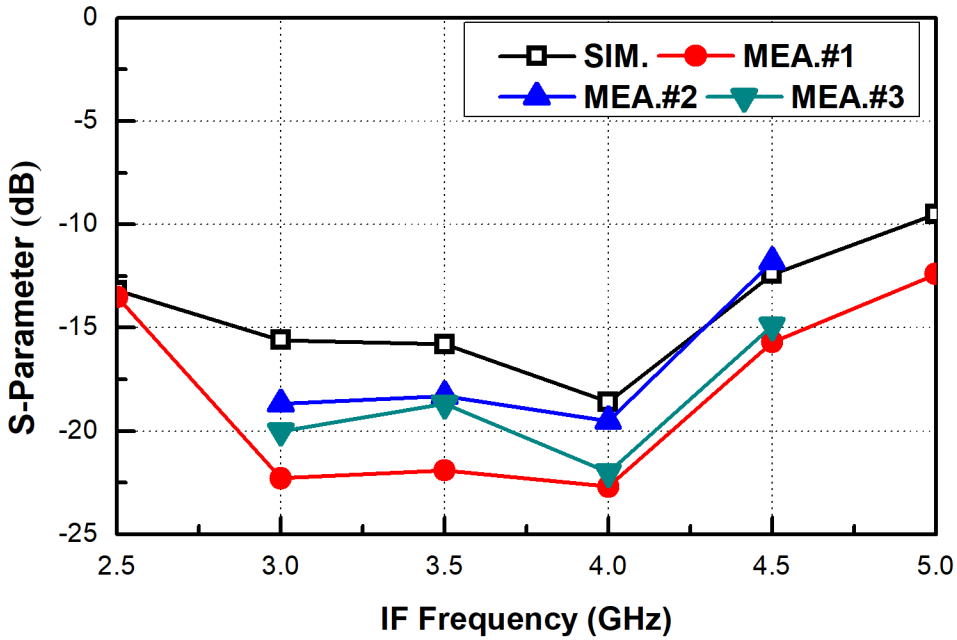


Fig. 3.65 S-parameter (S_{22}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 2 in Fig. 3.57 (80°, 2.5-5 GHz).

doi:10.6342/NTU202203942

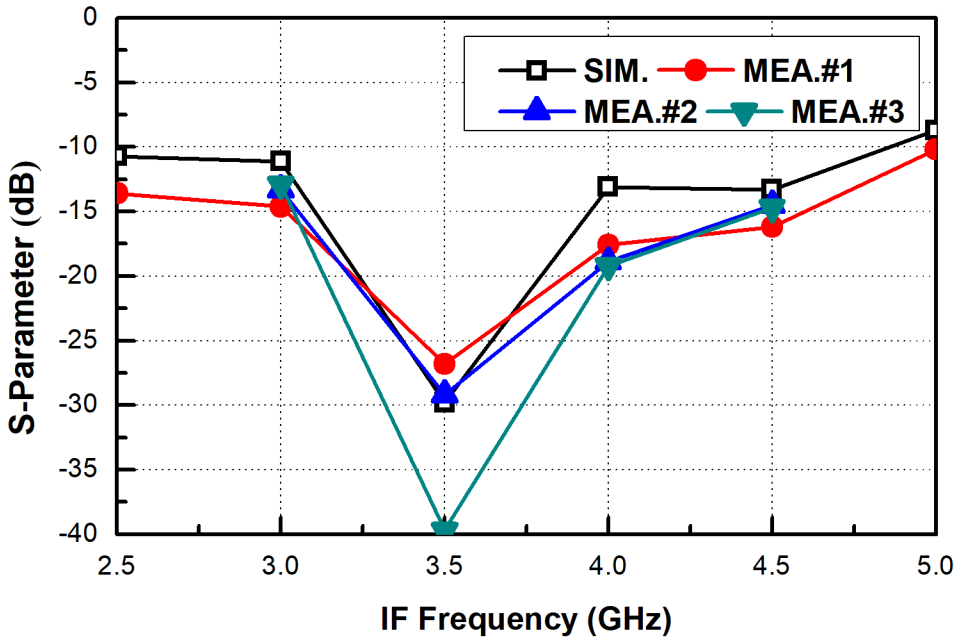


Fig. 3.66 S-parameter (S_{33}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 3 in Fig. 3.57 (80°, 2.5-5 GHz).

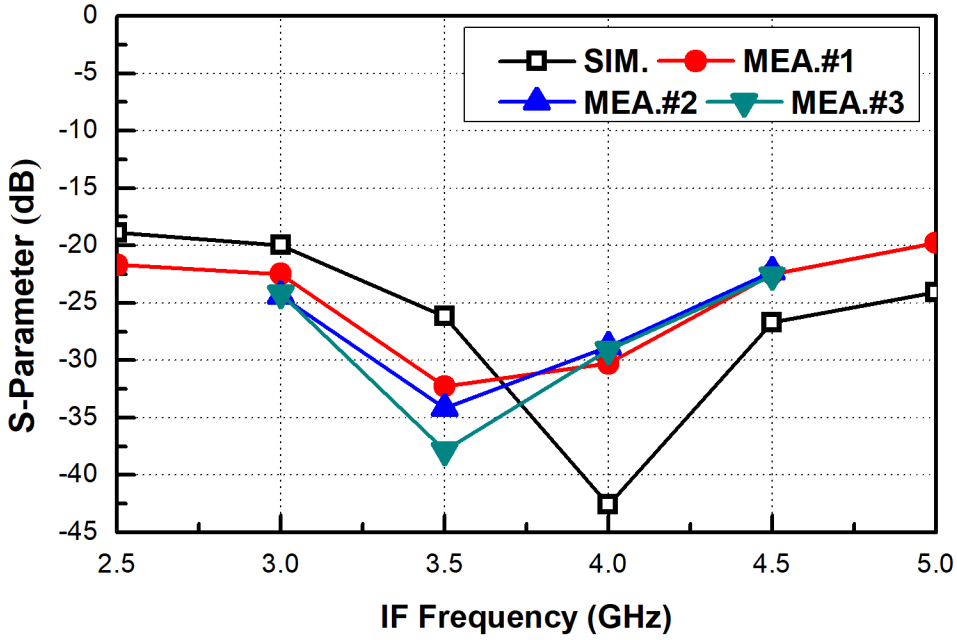


Fig. 3.67 S-parameter (S_{32}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 2,3 in Fig. 3.57 (80°, 2.5-5 GHz).

doi:10.6342/NTU202203942

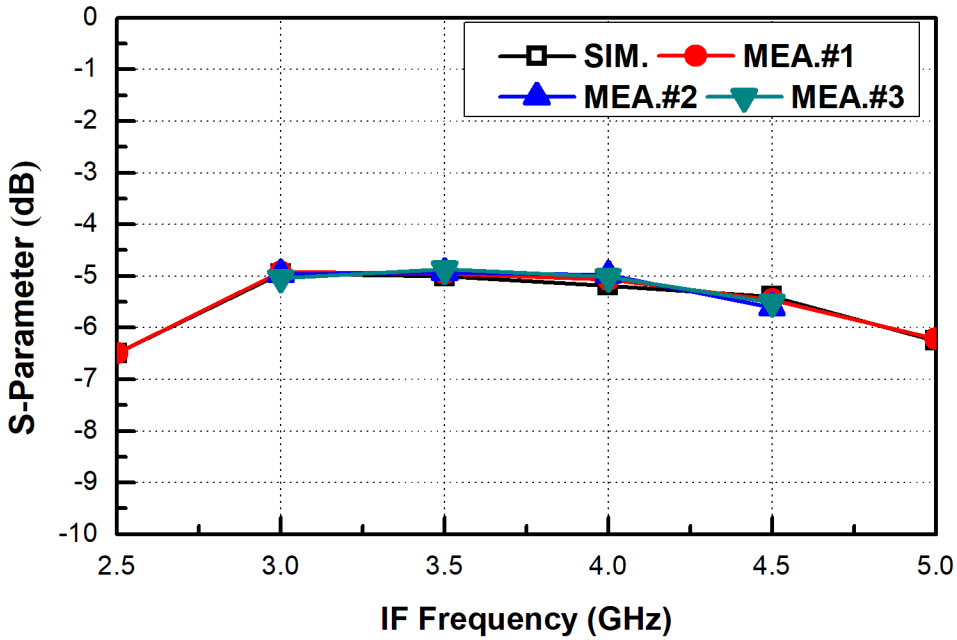


Fig. 3.68 S-parameter (S_{21}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 1,2 in Fig. 3.57 (80°, 2.5-5 GHz).

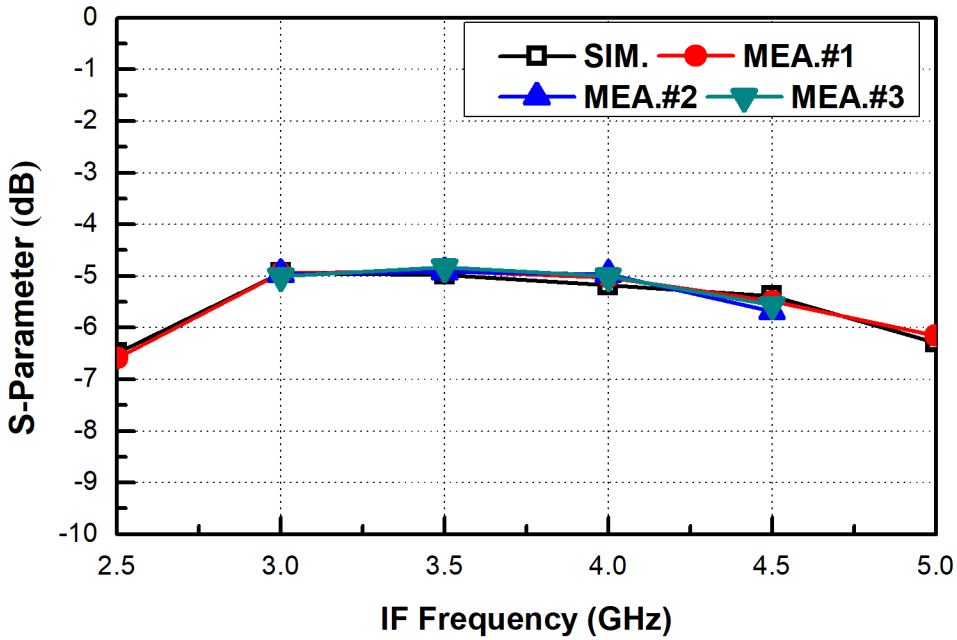


Fig. 3.69 S-parameter (S_{31}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 1,3 in Fig. 3.57 (80°, 2.5-5 GHz).

doi:10.6342/NTU202203942

Table 3.7 V_{Phase} of 3 samples when the phase is 80° and amplitude imbalance is close to 0 dB from 2.5-5 GHz.

80°_Freq. (GHz)	#1's V_{Phase} (V)	#2's V_{Phase} (V)	#3's V_{Phase} (V)
2.5	0	X	X
3	0.5	0 (82°)	0 (82°)
3.5	1.6	0.55	0.7
4	1.9	0.7	0.7
4.5	2.1	0.6	0.85
5	0.9	X	X

The S-parameters measurement of sample #1,2,3 and EM simulation of the tunable I/Q divider/combiner when the phase has a 100° tuning and amplitude imbalance is close to 0 dB for each frequency (2.5-5 GHz) are shown in Fig. 3.70- Fig. 3.75. Port numbers are shown in Fig. 3.57. $|S_{11}|$ of three samples is less than -11.7 dB from 2.5-5 GHz. $|S_{22}|$ of three samples is less than -10.5 dB from 2.5-5 GHz. $|S_{33}|$ of three samples is less than -10 dB from 2.5-5 GHz. $|S_{32}|$ of three samples less than -18.4 dB from 2.5-5 GHz. $|S_{21}|$ and $|S_{31}|$ of three samples are both between (-4.7)-(-6) dB from 2.5-5 GHz. The detailed phase control voltages (V_{Phase}) are shown in Table 3.8.

doi:10.6342/NTU202203942

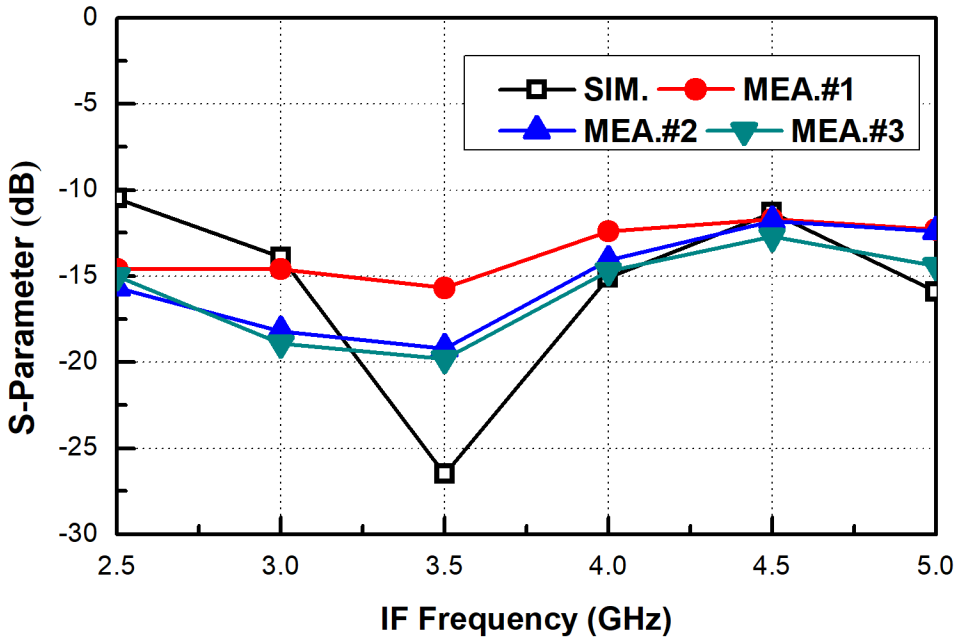


Fig. 3.70 S-parameter (S_{11}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 1 in Fig. 3.57 (100°, 2.5-5 GHz).

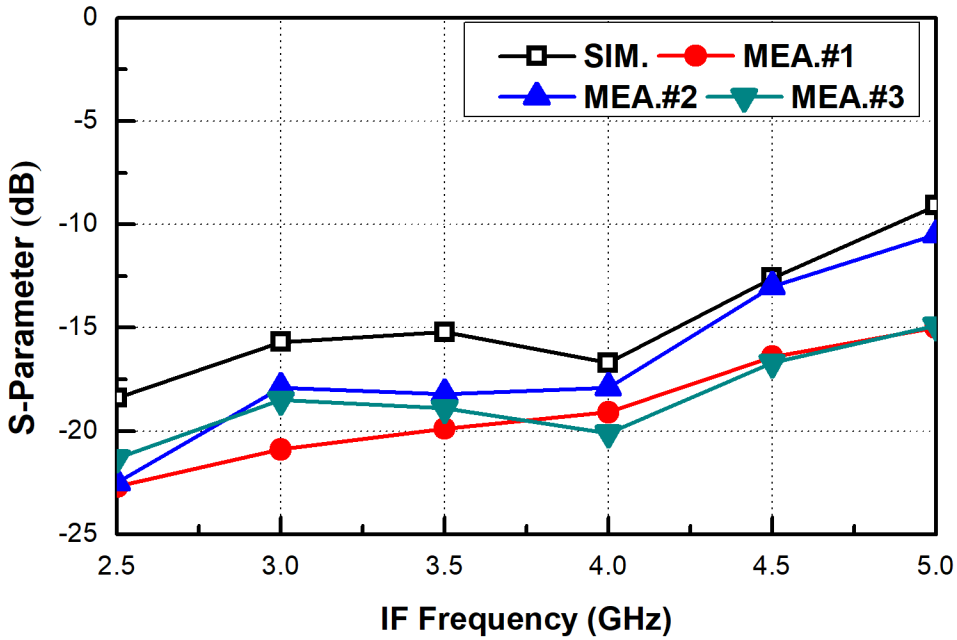


Fig. 3.71 S-parameter (S_{22}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 2 in Fig. 3.57 (100°, 2.5-5 GHz).

doi:10.6342/NTU202203942

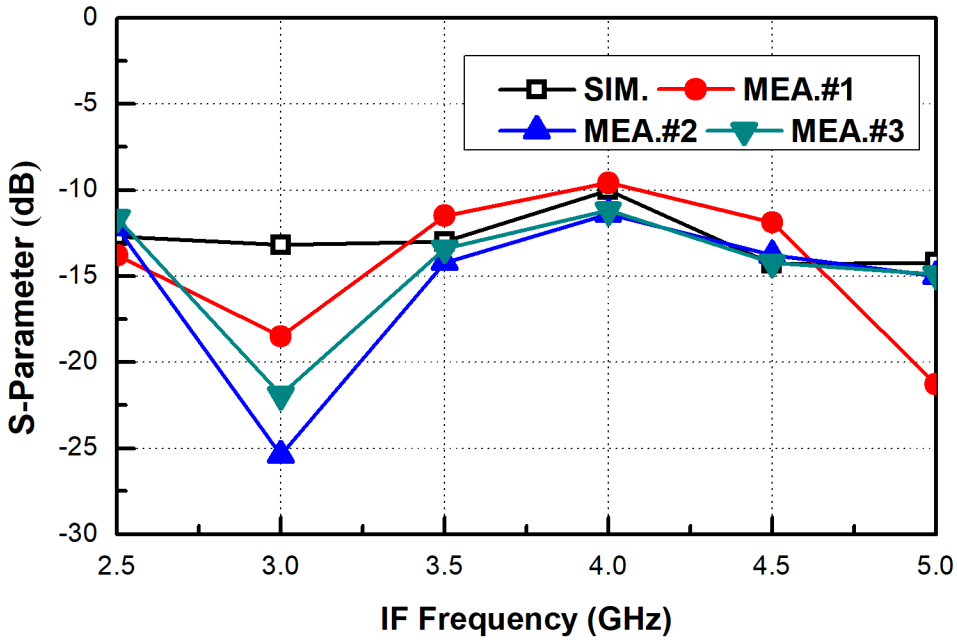


Fig. 3.72 S-parameter (S_{33}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 3 in Fig. 3.57 (100°, 2.5-5 GHz).

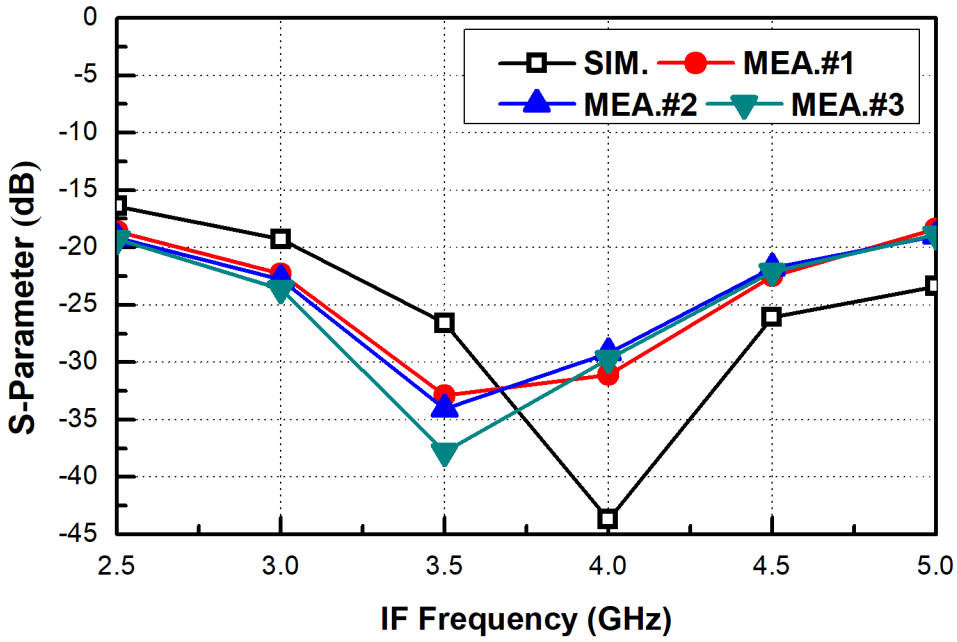


Fig. 3.73 S-parameter (S_{32}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 2,3 in Fig. 3.57 (100°, 2.5-5 GHz).

doi:10.6342/NTU202203942

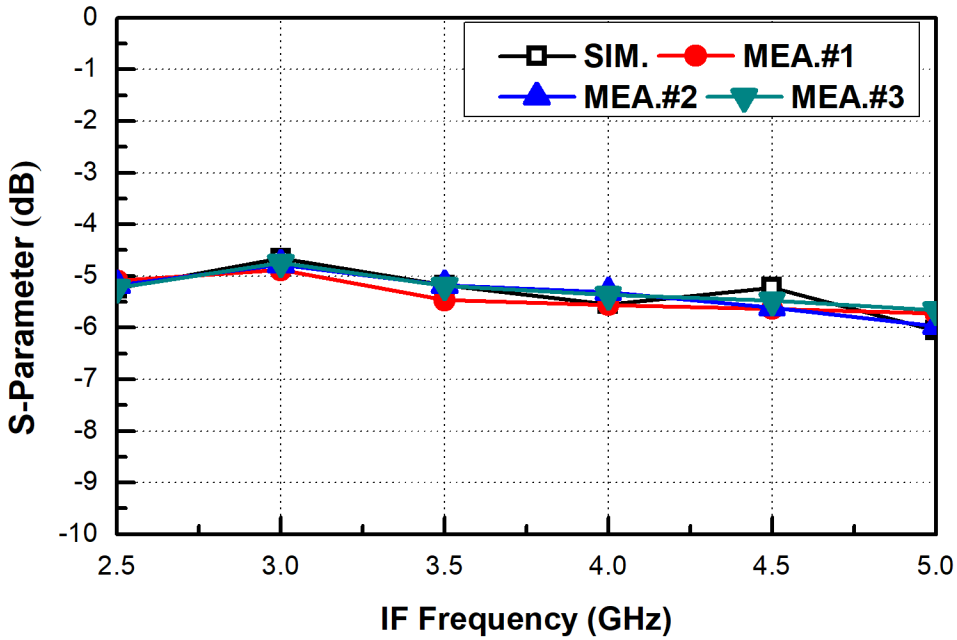


Fig. 3.74 S-parameter (S_{21}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 1,2 in Fig. 3.57 (100°, 2.5-5 GHz).

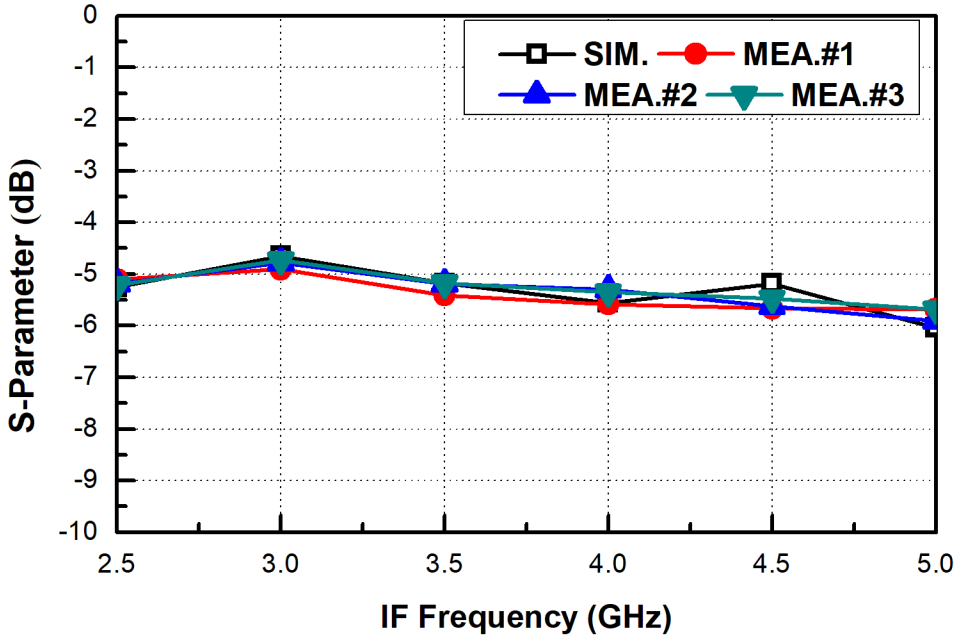


Fig. 3.75 S-parameter (S_{31}) measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner's port 1,3 in Fig. 3.57 (100°, 2.5-5 GHz).

doi:10.6342/NTU202203942

Table 3.8 V_{Phase} of 3 samples when the phase is 100° and amplitude imbalance is close to 0 dB from 2.5-5 GHz.

100°_Freq. (GHz)	#1's V_{Phase} (V)	#2's V_{Phase} (V)	#3's V_{Phase} (V)
2.5	2.9	2	2.1
3	5.2	4.33	4.4
3.5	6	5.15	5.3
4	6	5.1	5.1
4.5	6.05	5.2	5.3
5	6.24	4.75	4.93

The group delay measurement of sample #1,2,3 and EM simulation of the tunable I/Q divider/combiner when the phase has a 90° tuning and amplitude imbalance is close to 0 dB at 2.5-5 GHz is shown in Fig. 3.76. Three samples are less than 0.6 nsec.

doi:10.6342/NTU202203942

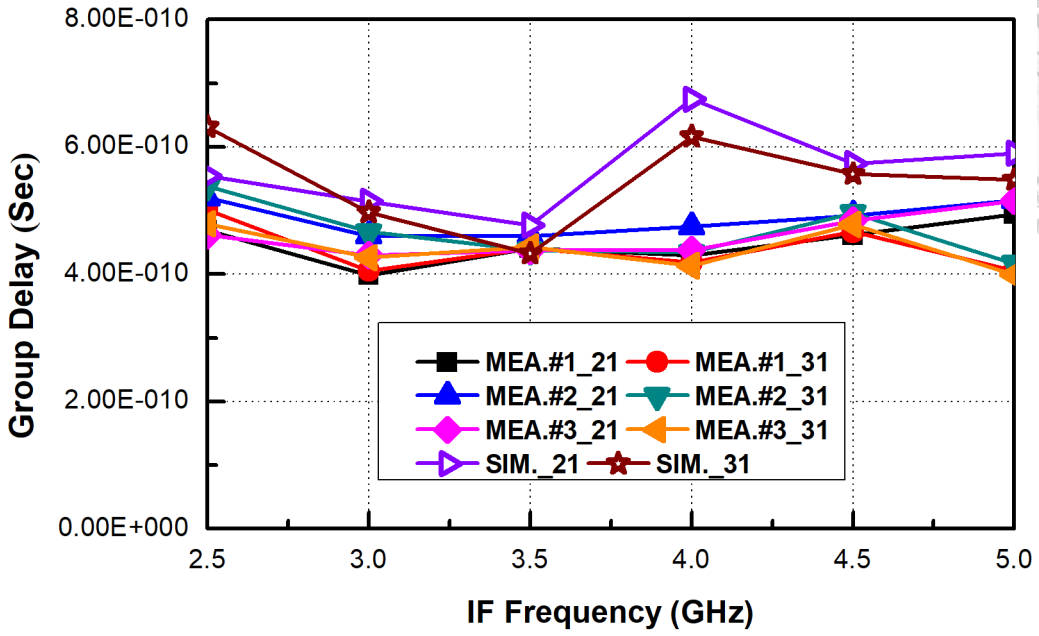


Fig. 3.76 Group delay measurement (#1,2,3) and EM simulation of the tunable I/Q divider/combiner in Fig. 3.57 (90°, 0 dB).

3.4.3 Image Rejection Ratio (IRR)

As shown in Fig. 3.77, we use two identical cables (SMA; phase and amplitude are very close) to connect $IF_{1,2}$ in Fig. 3.55 to port 2,3 in Fig. 3.57. We use an Agilent E8257D (250 kHz- 67 GHz) signal generator for RF/IF signal, a KEYSIGHT E8267D (250 kHz- 44 GHz) signal generator for 1/2 LO signal, an Agilent E4448A (3 Hz- 50 GHz) spectrum analyzer to measure large signals (RF/IF output power), a GWINSTEK PST-3202 (32 V,2 A x2/6 V, 5 A x1) power supply for DC supplying (doubler's V_{DD} and V_{Phase}) and a KEYSIGHT E36311A (6 V, 5 A/±25 V, 1 A) power supply for DC supplying ($V_{AmpR/AmpL}$).

doi:10.6342/NTU202203942

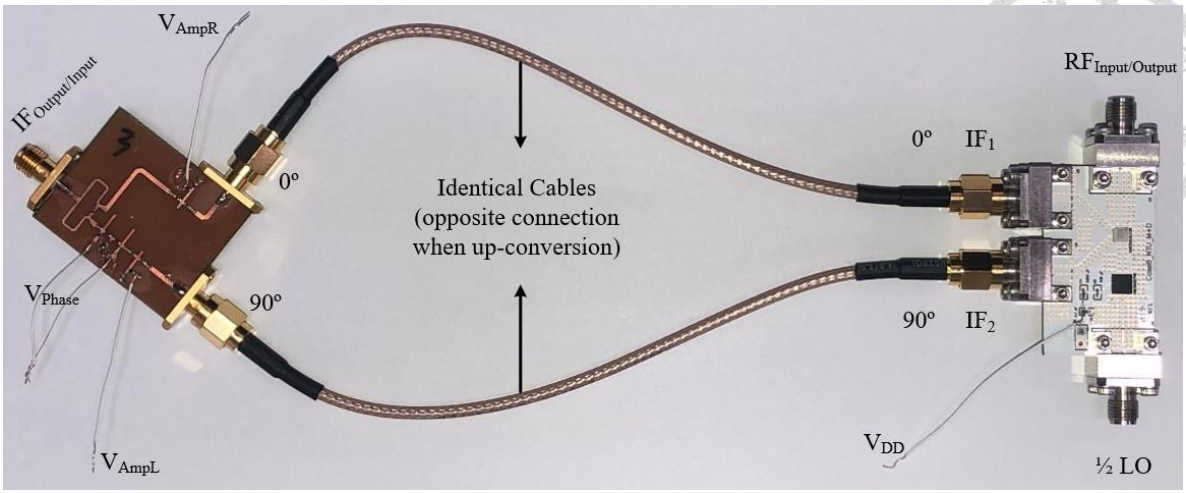


Fig. 3.77 Connection of the millimeter-wave image rejection module (down-conversion).

The measured conversion gain vs. LO power of the millimeter-wave up-/down-conversion image rejection module with the tunable I/Q divider/combiner (sample #3) is shown in Fig. 3.78 when RF frequency is 28 GHz, LO frequency is 25 GHz, and IF frequency is 3 GHz. The conversion gain is calculated as IF power minus RF power (down-conversion) or RF power minus IF power (up-conversion) in dBm, as shown in Fig. 3.48. When the 1/2 LO power is 4 dBm, both up-/down-conversion have maximum conversion gain (-3.7 dB for up-conversion and -6.9 dB for down-conversion).

The measured IP_{1dB} of the millimeter-wave up-/down-conversion image rejection module with the tunable I/Q divider/combiner (sample #3) is shown in Fig. 3.79 when RF frequency is 28 GHz, LO frequency is 25 GHz, IF frequency is 3 GHz, and 1/2 LO power is 4 dBm. Up-conversion is about 1 dBm and down-conversion is about 11 dBm.

doi:10.6342/NTU202203942

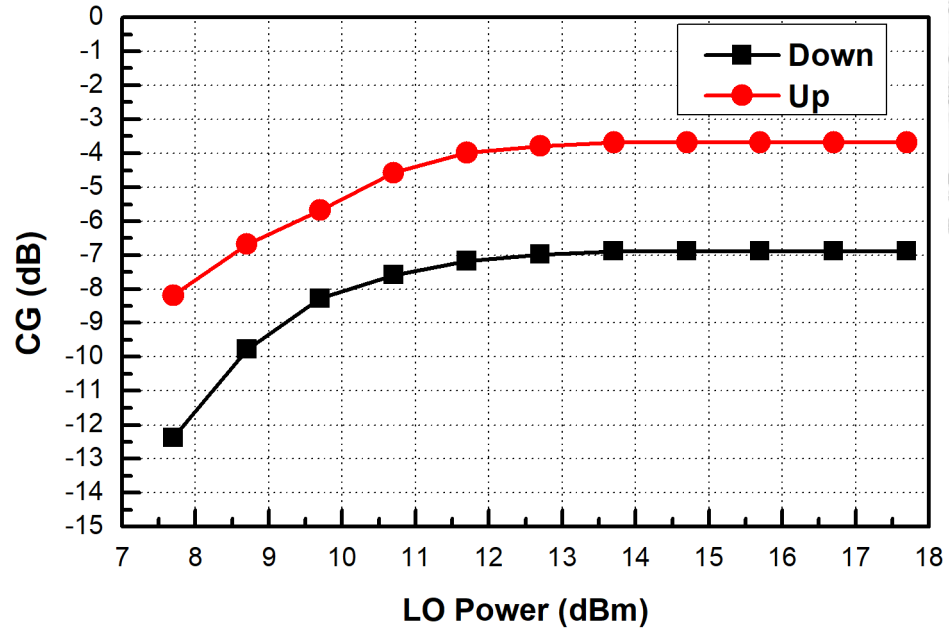


Fig. 3.78 Measured conversion gain (CG) vs. LO power of the millimeter-wave image rejection module (up-/down-conversion).

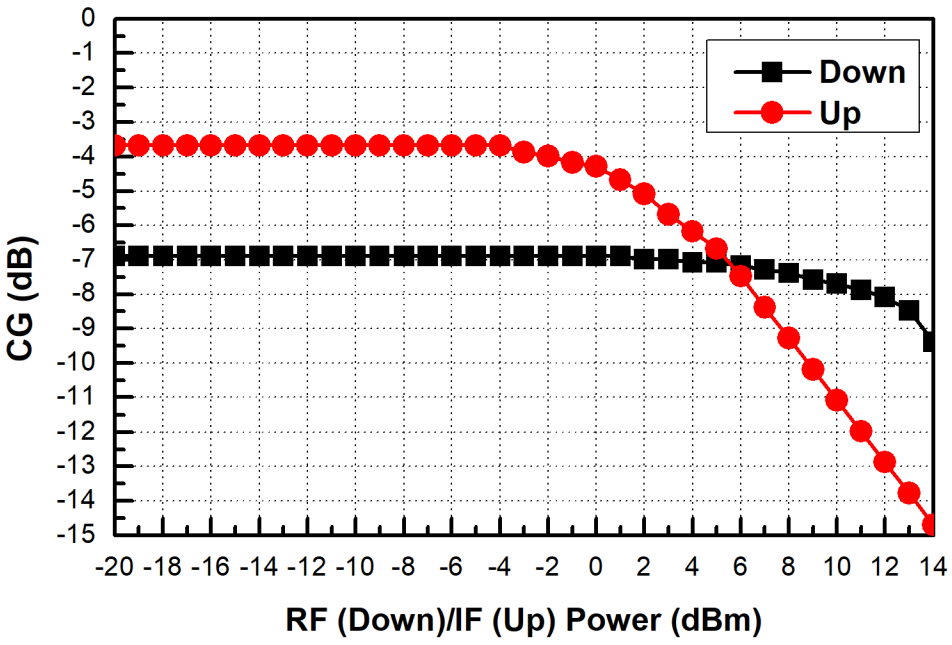


Fig. 3.79 Measured IP_{1dB} of the millimeter-wave image rejection module (up-/down-conversion).

doi:10.6342/NTU202203942

The measured bandwidth of the millimeter-wave up-/down-conversion image rejection module with the tunable I/Q divider/combiner (sample #3) is shown in Fig. 3.80 when LO frequency is 25 GHz and 1/2 LO power is 4 dBm. The conversion gain range of up-conversion is about 1.5 dB and the conversion gain range of down-conversion is about 1.9 dB from 2.5-5 GHz.

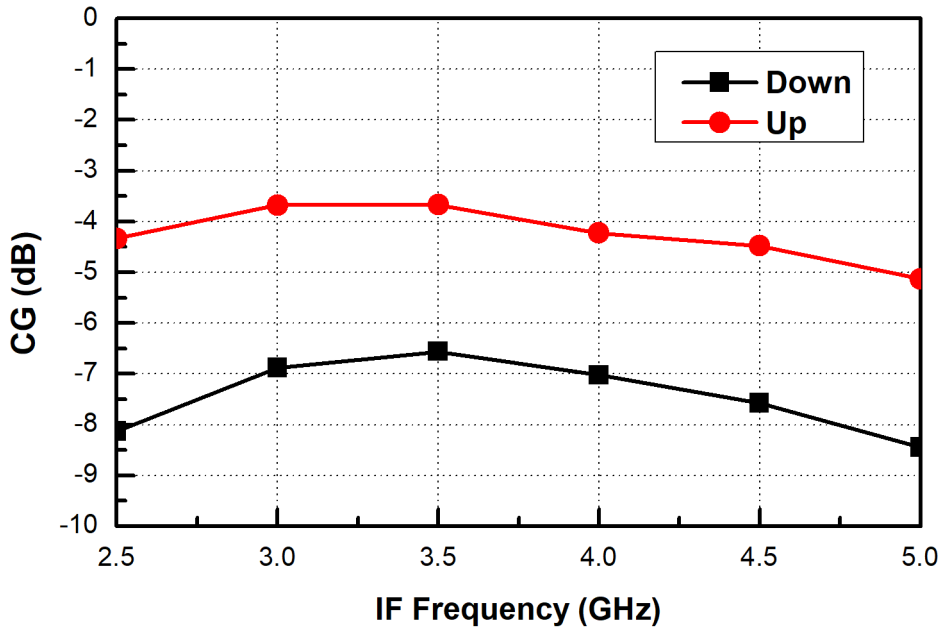


Fig. 3.80 Measured bandwidth of the millimeter-wave image rejection module (up-/down-conversion).

The measured IRR of the millimeter-wave up-/down-conversion image rejection module with the tunable I/Q divider/combiner (sample #3) when LO frequency is 25 GHz, IF frequency is 2.5-5 GHz, and 1/2 LO power is 4 dBm as shown in Fig. 3.81. To achieve the best IRR, we tune the phase and amplitude at each frequency. Except for 2.5 and 5 GHz, the other four frequency points can achieve or exceed 50 dB IRR during up-/down-conversion. The IRRs of 2.5 and 5 GHz are also quite good, at around 30 dB when up-/down-conversion. The detailed control voltages are shown in Table 3.9.

doi:10.6342/NTU202203942

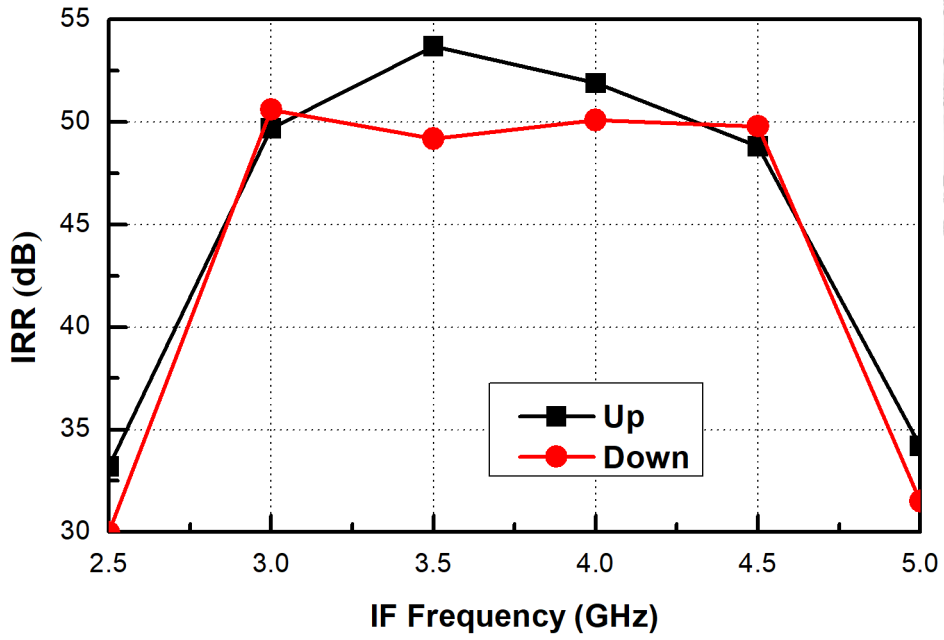


Fig. 3.81 Measured IRR of the millimeter-wave up-/down-conversion image rejection module with the tunable I/Q divider/combiner (LO, 25 GHz/IF, 2.5-5 GHz).

Table 3.9 V_{Phase}, V_{AmpL}, and V_{AmpR} (sample #3) when tuning the phase and amplitude at 2.5, 3, 3.5, 4, 4.5 and 5 GHz to achieve the best IRR.

Up_Freq. (GHz)	V_{Phase} (V)	V_{AmpL} (V)	V_{AmpR} (V)
2.5	2	1.02	0.9
3	6.4	1.04	0
3.5	6.5	0.9	0.98
4	6.6	0	1
4.5	6.3	0.9	0.964
5	6	1.03	0.9
Down_Freq. (GHz)	V_{Phase} (V)	V_{AmpL} (V)	V_{AmpR} (V)

doi:10.6342/NTU202203942

2.5	0	0	1.092
3	3.65	0.9	0.993
3.5	4.3	0	1.014
4	4.05	0	1.002
4.5	4.2	0.8	0.997
5	3.7	0.9	0.965

The measured phase difference and amplitude imbalance of the tunable I/Q divider/combiner (sample #3) are shown in Fig. 3.82 and Fig. 3.83, respectively. At 3, 3.5, 4, and 4.5 GHz, we only have 90° phase tuning and 0 dB amplitude tuning. In an 800 MHz bandwidth, the 3 GHz curve has a 10° phase difference with a 0.6 dB amplitude imbalance, the 3.5 GHz curve has a 3° phase difference with a 0.1 dB amplitude imbalance, the 4 GHz curve has a 0.8° phase difference with 0.3 dB amplitude imbalance, and the 4.5 GHz curve has a 2.4° phase difference with 0.2 dB amplitude imbalance. As shown in Fig. 3.84- Fig. 3.87, the 3.5, 4, and 4.5 GHz curves can reach close to or exceed 30 dB IRR when up-/down-conversion. The 3 GHz curve has an IRR of around 25 dB when up-/down-conversion. The detailed control voltages are shown in Table 3.10.

doi:10.6342/NTU202203942

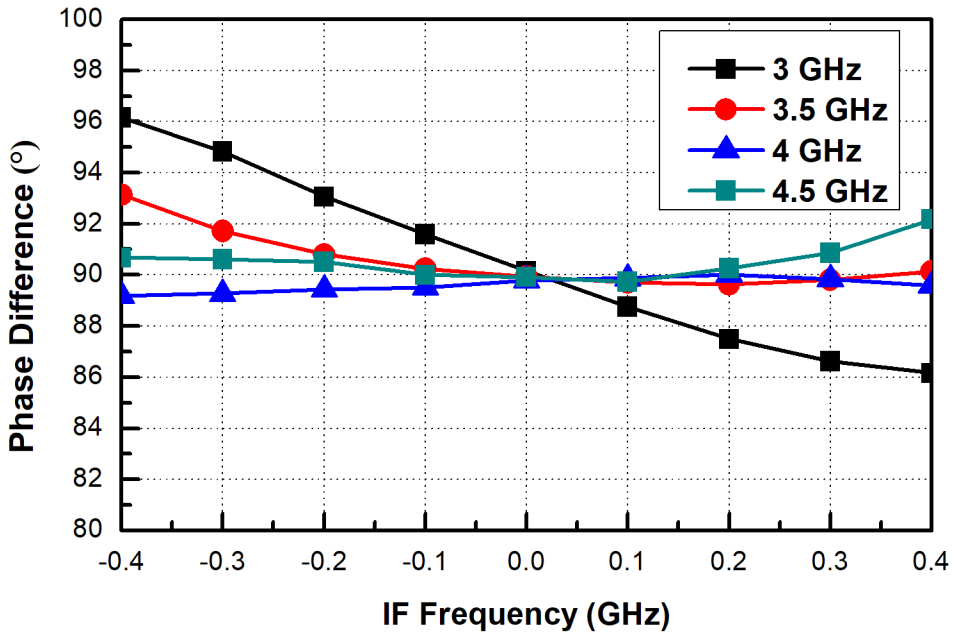


Fig. 3.82 Measured phase difference of the tunable I/Q divider/combiner (sample #3) (800 MHz bandwidth).

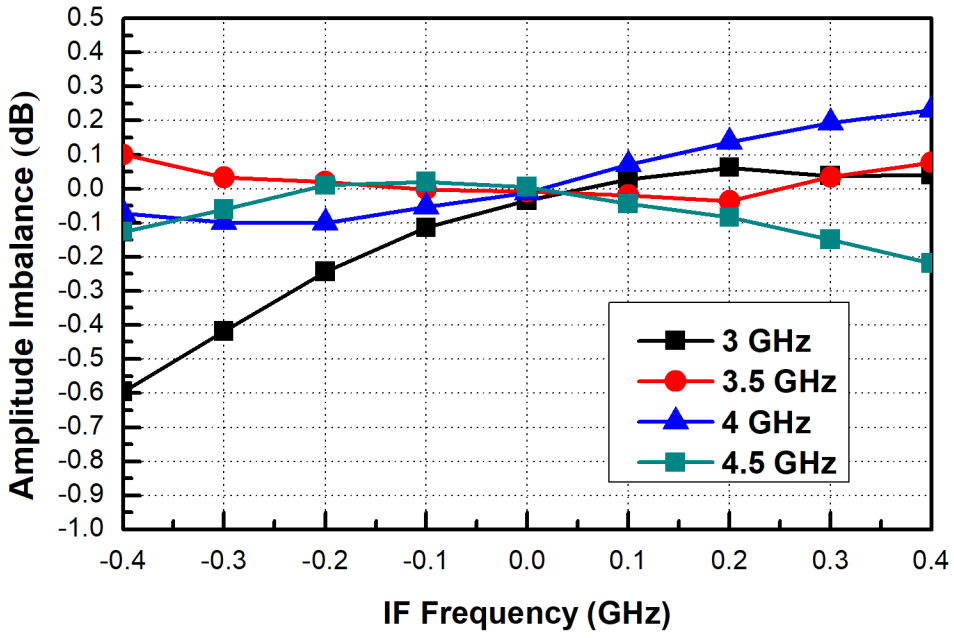


Fig. 3.83 Measured amplitude imbalance of the tunable I/Q divider/combiner (sample #3) (800 MHz bandwidth).

doi:10.6342/NTU202203942

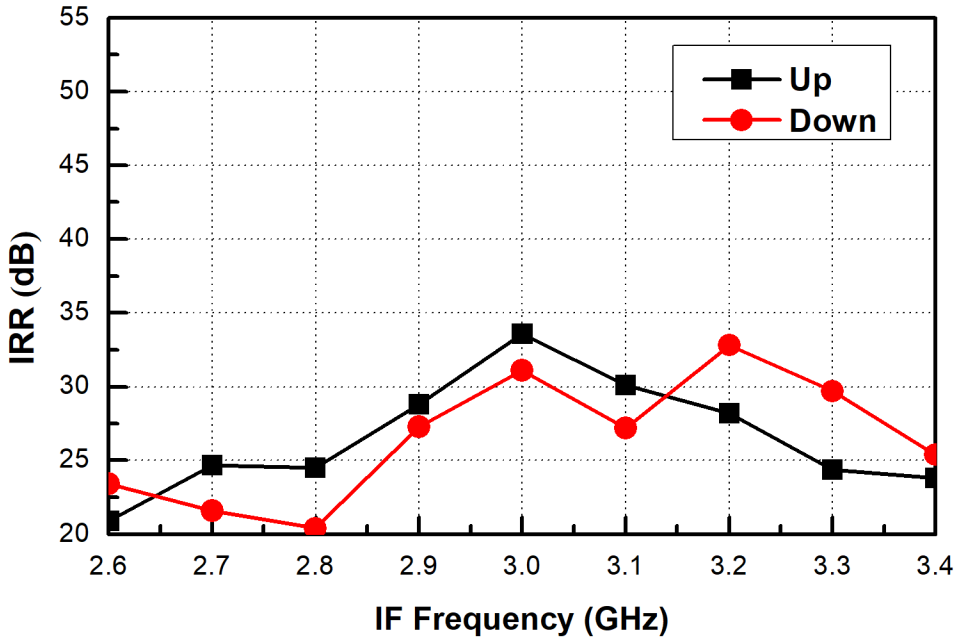


Fig. 3.84 Measured IRR of the millimeter-wave up-/down-conversion image rejection module with the tunable I/Q divider/combiner (sample #3) (LO, 25 GHz/IF, 2.6-3.4 GHz).

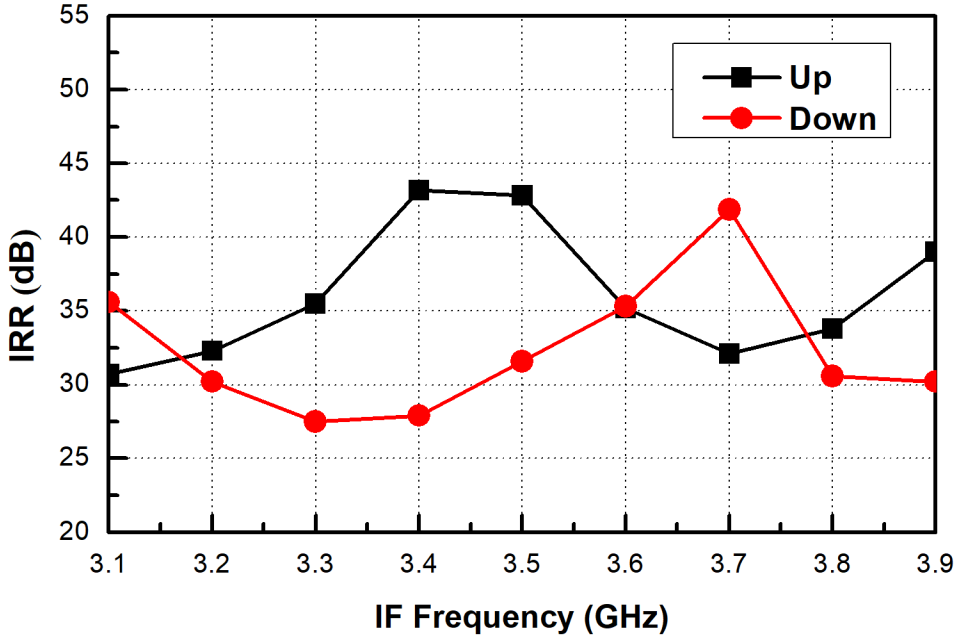


Fig. 3.85 Measured IRR of the millimeter-wave up-/down-conversion image rejection module with the tunable I/Q divider/combiner (sample #3) (LO, 25 GHz/IF, 3.1-3.9 GHz).

doi:10.6342/NTU202203942

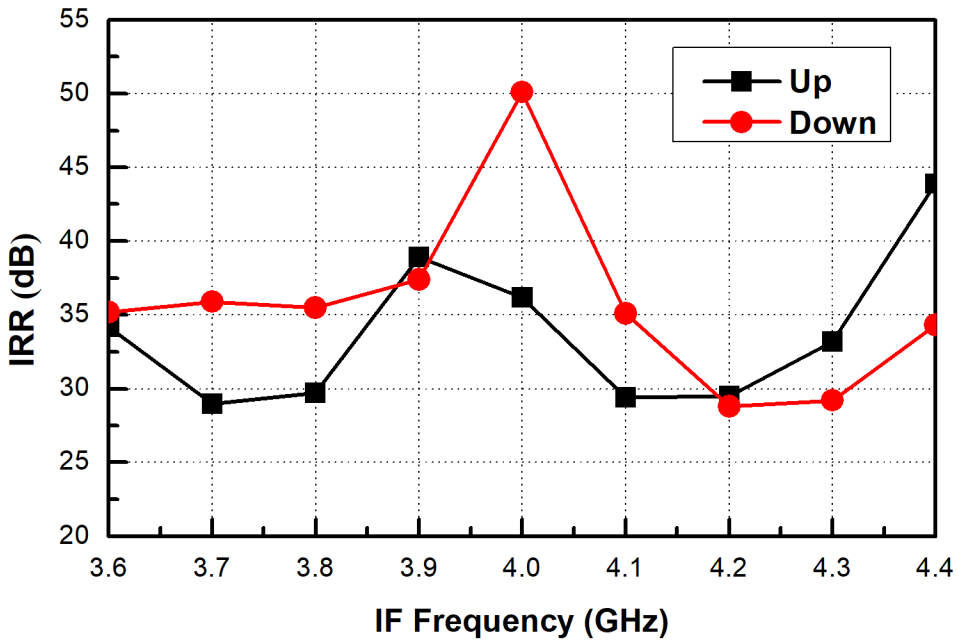


Fig. 3.86 Measured IRR of the millimeter-wave up-/down-conversion image rejection module with the tunable I/Q divider/combiner (sample #3) (LO, 25 GHz/IF, 3.6-4.4 GHz).

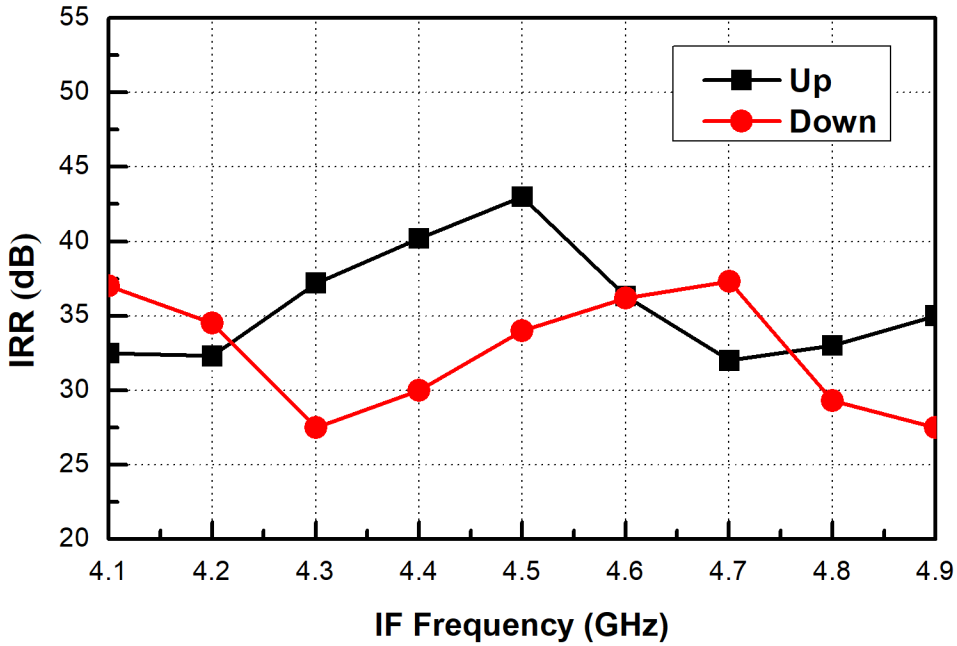


Fig. 3.87 Measured IRR of the millimeter-wave up-/down-conversion image rejection module with the tunable I/Q divider/combiner (sample #3) (LO, 25 GHz/IF, 4.1-4.9 GHz).

doi:10.6342/NTU202203942

Table 3.10 V_{Phase}, $V_{AmpL,}$ and V_{AmpR} (sample #3) when only have a 90° phase tuning and a 0 dB amplitude tuning at 3, 3.5, 4, and 4.5 GHz.

Up_Freq. (GHz)	V_{Phase} (V)	V_{AmpL} (V)	V_{AmpR} (V)
3	6	1.04	0
3.5	6.3	0.9	0.98
4	6.6	0.9	0.95
4.5	6.1	0.9	0.96
Down_Freq. (GHz)	V_{Phase} (V)	V_{AmpL} (V)	V_{AmpR} (V)
3	3	0.9	0.993
3.5	3.5	0	1.014
4	4.05	0	1.002
4.5	3.6	0.9	0.99

3.5 Summary

In this chapter, a millimeter-wave up-/down-conversion image rejection module is presented. By testing the HMC524ALC3B (mixer) and HMC942LP4E (doubler) evaluation boards, we can integrate these two package chips on an evaluation board and plan to connect the IF ends to the tunable I/Q divider/combiner and achieve the image rejection. With the analysis and implementation of the left-/right-handed transmission lines and T-type attenuator, 80-100° phase difference tuning and accurate amplitude tuning can be obtained.

doi:10.6342/NTU202203942

Based on the excellent reflection coefficient (-20 dB, 2-5.6 GHz) of the two outputs of the Wilkinson power divider, it can still maintain a good reflection coefficient (-10 dB) when performing phase or amplitude tuning. Port number is shown in Fig. 3.57. When phase has a 90° tuning, $|S_{33}|$ of 3 samples less than -10 dB from 3-5 GHz and close to -10 dB at 2.5 GHz. When the phase has an 80° tuning, $|S_{33}|$ of sample #1 is less than -10.2 dB from 2.5-5 GHz. $|S_{33}|$ of sample #2,3 (82°) less than -12.9 dB from 3-4.5 GHz. When phase has a 100° tuning, $|S_{33}|$ of 3 samples less than -10 dB from 2.5-5 GHz. The reflection coefficient of the tunable I/Q divider/combiner outputs (port 2,3) will affect its tuning ability. It can be known from the measurement results of IRR. Without considering the reflection coefficient on the IF ends of the millimeter-wave up-/down-conversion image rejection module (board 1 in Fig. 3.4), $|S_{33}|$ (90° at 2.5 and 5 GHz) is relatively poor as shown in Fig. 3.60, therefore the highest IRR value that can be tuned can only approach 30 dB.

In the practical application of the millimeter-wave up-/down-conversion image rejection module, the operating data of the IF frequency of 800 MHz bandwidth should be considered. We measure the phase difference and amplitude imbalance of the 800 MHz bandwidth at 3, 3.5, 4, and 4.5 GHz when have a 90° phase tuning and a 0 dB amplitude tuning. It can be found that a smaller variation of phase difference and amplitude imbalance will have a better IRR in 800 MHz bandwidth.

Table 3.11- Table 3.12 summarize the performance of tunable dividers/combiners fabricated on PCB at IF frequency in recent years. Compared to these tunable dividers/combiners, this work shows a 66.7% bandwidth because the phase tuning range is only 20° with subtle amplitude tuning ability. Under this bandwidth, the 3 ports' reflection coefficient is better than -10 dB, and isolation is better than 18.4 dB. Although the phase can

doi:10.6342/NTU202203942

only be tuned at 80-100°, it is enough for the imbalance of the I/Q signal. Amplitude can be tuned slightly between (+2)-(-1.1) dB, which is very helpful for improving IRR. Even though it lacks the 360° phase tunability of references [26] and [27], having both phase and amplitude tuning functions makes it extremely competitive in the I/Q dividers/combiners. It can be seen that the tunable I/Q divider/combiner exhibits an outstanding comprehensive performance among each parameter for the image rejection system.

Table 3.11 Comparison of the published tunable dividers/combiners (part I).

Ref.	Substrate	Function	Freq. (GHz)	Tuning (°/dB)
This Work	0.6 mm FR4	PD+ TP+ TA	2.5-5	80-100°/ (+2)-(-1.1) dB
MWCL' 20 [26]	25 mil Rogers 6010	PD+ TP	1.15, 1.28, 1.4	0-360°
TCS II' 19 [27]	1.24 mm Rogers 3010	PD+ TP	0.9-1.1	90, 180, 270, 360°
MWCL' 18 [28]	1.27 mm Rogers 3010	DC+ TP	0.9-1.1	45-135°
APMC' 18 [29]	0.5 mm Rogers 4003	FC+ TA	1-2	(+9)-(-20) dB
MWCL' 17 [30]	0.735 mm FR4	PD+ TP	0.5-1.3 **	(-15)-(-120)° *

*: angle($S_{21,31}$) both have (-15)-(-120)° tuning ability.

**: only when the angle ($S_{21,31}$) is -90°.

doi:10.6342/NTU202203942

PD: power divider; DC: directional coupler; FC: forward coupler; TP: tunable phase; TA: tunable amplitude.

Table 3.12 Comparison of the published tunable dividers/combiners (part II).

Ref.	RL. (dB)	IL. (dB)	ISO. (dB)	Size (mm*mm)
This Work	> 10 ($\|S_{11}\|$, $\|S_{22}\|$, and $\|S_{33}\|$)	4.7-6.6	> 18.4	35.7*29.1
MWCL' 20 [26]	> 15 ($\|S_{11}\|$)	5.6-5.9	N/A	N/A
TCS II' 19 [27]	> 10 ($\|S_{11}\|$, $\|S_{22}\|$, and $\|S_{33}\|$)	3.6-4.5	> 20	50*25
MWCL' 18 [28]	> 9 ($\|S_{11}\|$)	3.2-6	> 8	22.6*16.9
APMC' 18 [29]	> 15 ($\|S_{11}\|$)	1-20 (1.5 GHz)	> 20	47*29
MWCL' 17 [30]	> 17 ($\|S_{11}\|$, $\|S_{22}\|$, and $\|S_{33}\|$)	< or = 4.6	> 29	35.6*8 ***

***: excluding the feed lines of 3 ports.

doi:10.6342/NTU202203942

Chapter 4 A 24-32 GHz High Image Rejection Ratio Up-/Down-Conversion Subharmonic Mixer for 5G Communication

4.1 Introduction

At present, numerous countries have revealed the millimeter-wave frequency ranges that will be used by 5G communication. The US is 27.5-28.35 GHz and 37-40 GHz, Europe is 24.25-27.5 GHz and 31.8-33.4 GHz, while China is 24.25-27.5 GHz and 37 GHz-42.5 GHz. From the above, it is apparent that 5G communication will be developed at these frequency ranges.

In the millimeter-wave, the subharmonic mixer is an important technique. Subharmonic mixers enable designers to use lower LO frequencies, reducing the need to generate a high-frequency LO signal and the necessity for measuring instruments. Subharmonic mixers are a simpler alternative to conventional mixers without a LO frequency multiplier for high-frequency application design.

In previous literatures, a high image rejection ratio (IRR) is around 30-40 dB [31]-[35]. To meet this standard, the phase and amplitude imbalances of the fed quadrature signal must be tailored to be within 3° and 0.3 dB, respectively. As a result, we attempted to use two passive subharmonic mixers as mixer cores, a Wilkinson power divider as an RF signal divider/combiner, and a Wilkinson power divider with left-/right-handed transmission lines

doi:10.6342/NTU202203942

as a LO quadrature signal generator [16] to achieve a high image rejection ratio up-/down-conversion mixer with a center frequency of 28 GHz and an 8 GHz bandwidth.

4.2 Circuit Design of A 24-32 GHz High Image Rejection Ratio Up-/Down-Conversion Subharmonic Mixer for 5G Communication

4.2.1 Concepts of The High IRR Up-/Down-Conversion Subharmonic Mixer

We do not contemplate using the mixer architecture with a switch to achieve up-/down-conversion since we want to simplify circuit operation and design, thus we use a passive mixer. To avoid the loss caused by complex wiring, we employ a single-ended anti-parallel diode pair subharmonic as the mixer core as shown in Fig. 4.1. Ports O_I,Q, F_I,Q, and IF_I,Q connect to the LO, RF, and IF ends, respectively.

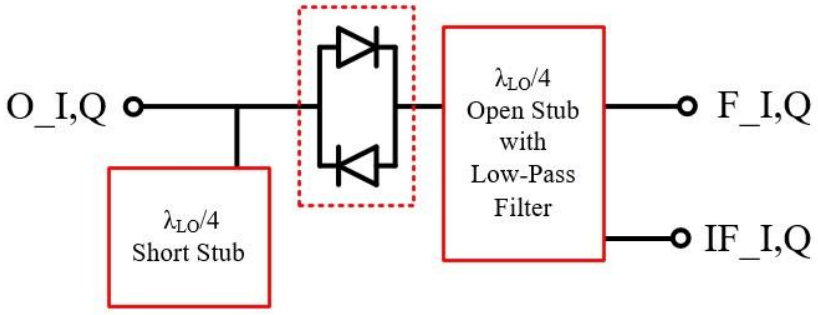


Fig. 4.1 Anti-parallel diode pair subharmonic mixer core.

We compare the performance of the two processes (0.18 μm CMOS and 0.15 μm GaAs pHEMT) under this configuration. Based on [36], we use the gate-source connected nMOS as a diode to obtain a better conversion gain in 0.18 μm CMOS. The LO power sweeping of port O_I,Q's reflection coefficient at 12 GHz as shown in Fig. 4.2. We choose point A

doi:10.6342/NTU202203942

because it is close to the circle whose real part is equal to 1 (make matching easier) and has low LO power (8 dBm in GaAs and 5 dBm in CMOS); the size is 1 finger with 30 μm width for a diode in GaAs and 45 fingers with 1 μm width for a gate-source connected nMOS in CMOS. Then we employ ideal lumped elements for point A's matching (reflection coefficient on port O_I,Q in Fig. 4.1) as shown in Fig. 4.3. The simulated conversion gain vs. LO power is shown in Fig. 4.4. Although GaAs takes 3 dB more LO power to drive the mixer than CMOS, it has a 6.2 dB higher conversion gain. Therefore, we design this circuit using 0.15 m GaAs pHEMT.

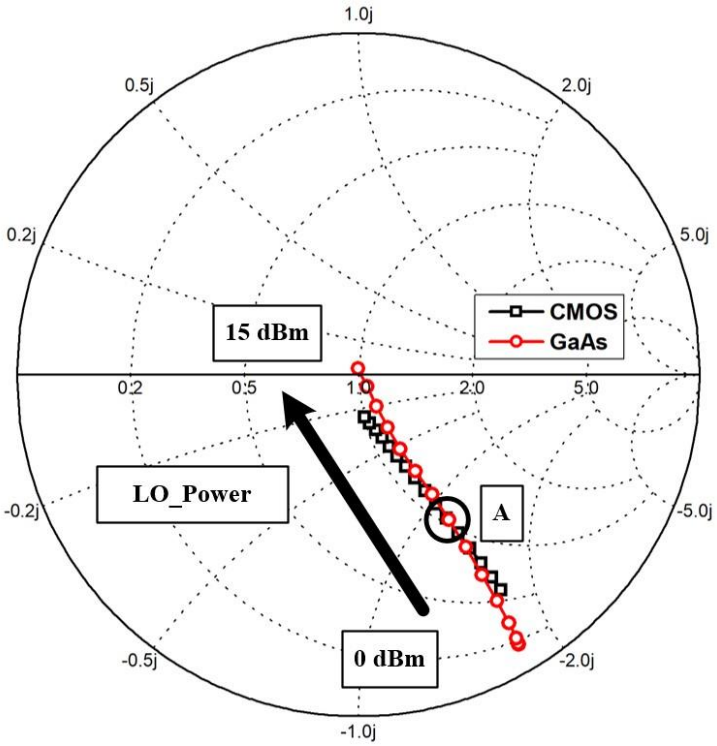


Fig. 4.2 LO power sweeping (reflection coefficient on port O_I,Q in Fig. 4.1) at 12 GHz in the Smith chart in two processes.

doi:10.6342/NTU202203942

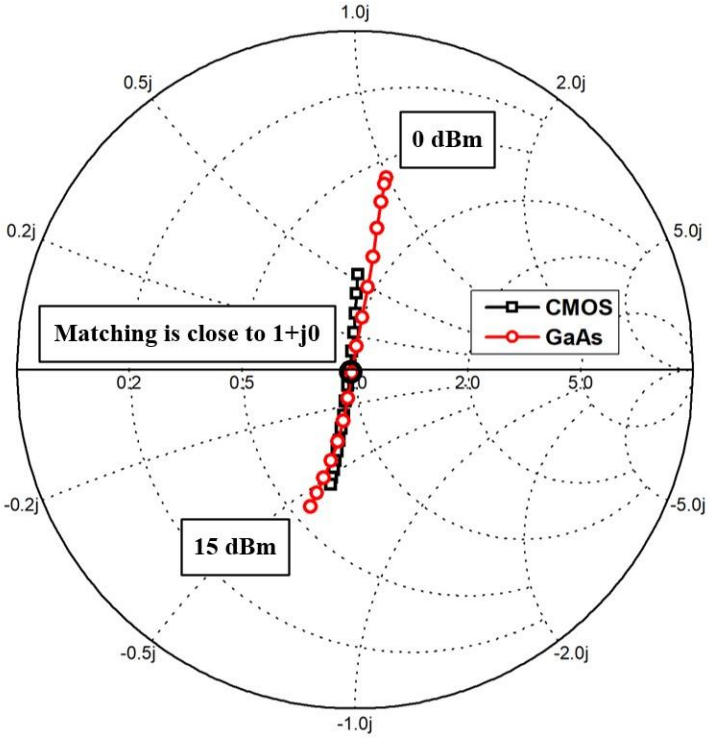


Fig. 4.3 Matching (reflection coefficient on port O_I,Q in Fig. 4.1) with ideal lumped elements of point A in two processes.

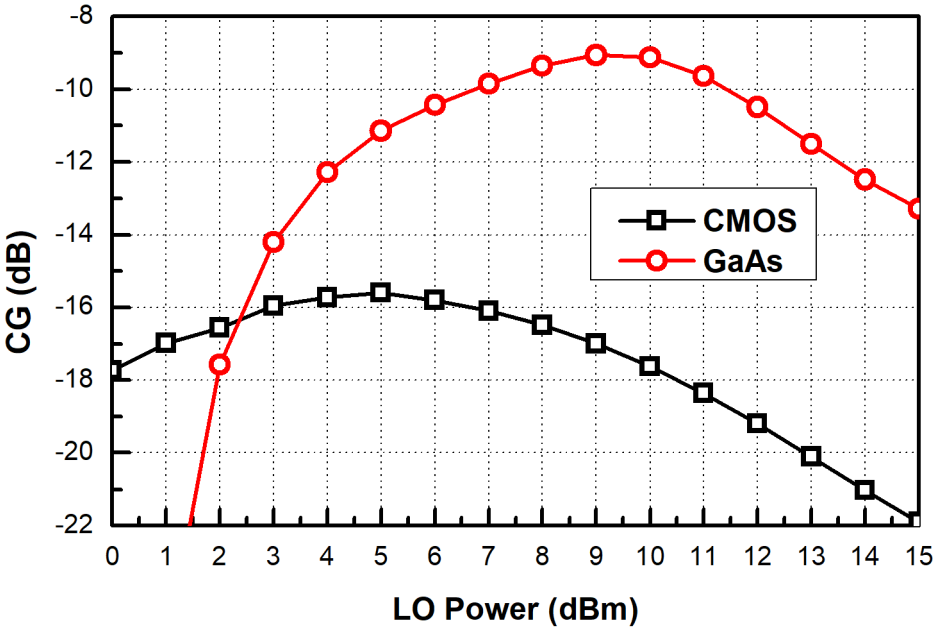


Fig. 4.4 Simulated conversion gain (CG) vs. LO power when considering the matching of point A in two processes.

doi:10.6342/NTU202203942

We also compare the performance of the passive FET mixer (resistive mixer) and the anti-parallel diode pair mixer in 0.15 m GaAs pHEMT as shown in Fig. 4.5. The size is 1 finger with 30 μm width for a diode and 2 fingers with 60 μm width for a FET in CMOS. Then we also employ ideal lumped elements for point A's matching at 12 GHz. The simulated conversion gain vs. LO power is shown in Fig. 4.6. The anti-parallel diode pair mixer has a 15.2 dB higher conversion gain when LO power is 8 dBm. The simulated IP_{1dB} is shown in Fig. 4.7. The FET mixer has a 13.5 dB higher IP_{1dB} when LO power is 8 dBm. Therefore, we design this circuit using anti-parallel diode pair mixer in 0.15 m GaAs pHEMT since its higher conversion gain and OP_{1dB}.

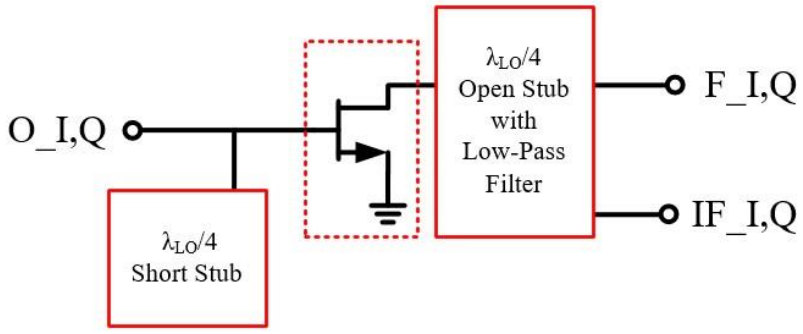


Fig. 4.5 FET subharmonic mixer core.

doi:10.6342/NTU202203942

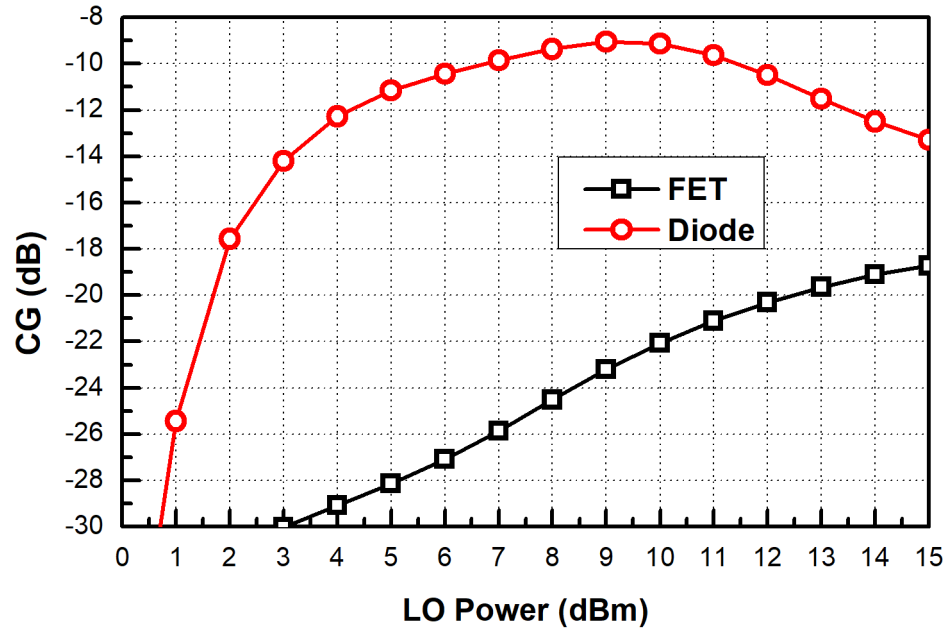


Fig. 4.6 Simulated conversion gain (CG) vs. LO power when considering the matching of point A in FET mixer and anti-parallel diode pair mixer.

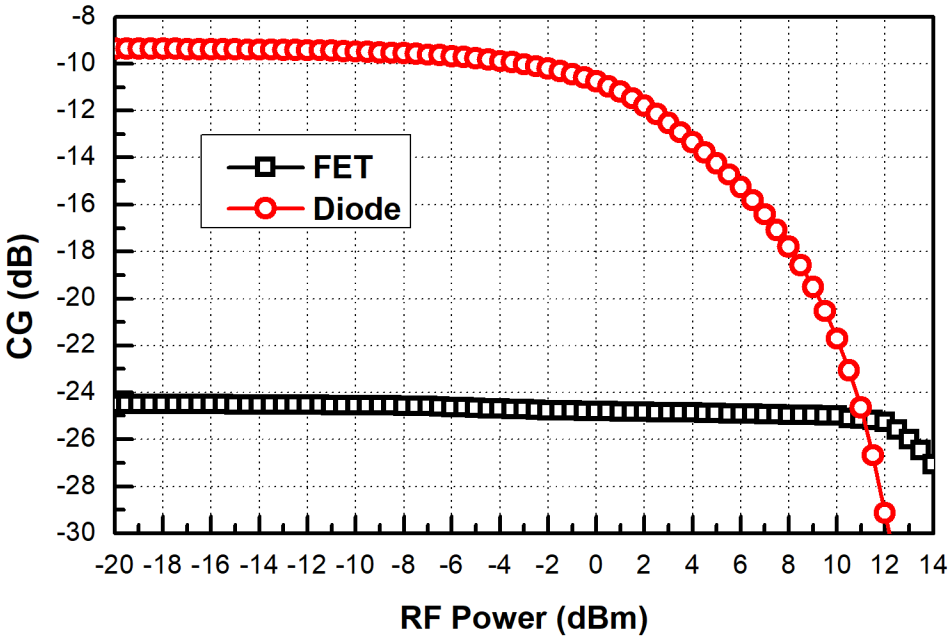


Fig. 4.7 Simulated IP_{1dB} when considering the matching of point A in FET mixer and anti-parallel diode pair mixer.

doi:10.6342/NTU202203942

How much phase or amplitude imbalance can a high IRR of 30-40 dB tolerate? We are referring to an equation [37] that considers ideal mixer cores.

$$\mathrm{IRR} = 10 \cdot \log\left[\frac{\gamma^2 + 2 \cdot \gamma \cdot \cos(\Delta\theta) + 1}{\gamma^2 - 2 \cdot \gamma \cdot \cos(\Delta\theta) + 1}\right] \tag{4.1}$$

$$= 10 \cdot \log\left[\frac{\gamma^2 + 2 \cdot \gamma \cdot \cos(2 \cdot \Delta\theta_{\mathrm{sub}}) + 1}{\gamma^2 - 2 \cdot \gamma \cdot \cos(2 \cdot \Delta\theta_{\mathrm{sub}}) + 1}\right],$$

and

$$\text{Amplitude Imbalance (dB)} = 20 \cdot \log\gamma. \tag{4.2}$$

γ denotes the amplitude imbalance in magnitude, $\Delta\theta$ denotes the phase imbalance in degree when the phase reference is 90°, and $\Delta\theta_{\mathrm{sub}}$ denotes the phase imbalance in degree when the phase reference is 45° (for subharmonic mixer). Using MATLAB, we construct a contour illustrating the relationship between phase and amplitude imbalances to IRR as shown in Fig. 4.8. Since quadrature signals commonly have phase and amplitude imbalances, it is advisable to design the IRR over 30 dB within 3° and 0.3 dB for the fundamental mixer, and within 1.5° and 0.3 dB for the subharmonic mixer.

doi:10.6342/NTU202203942

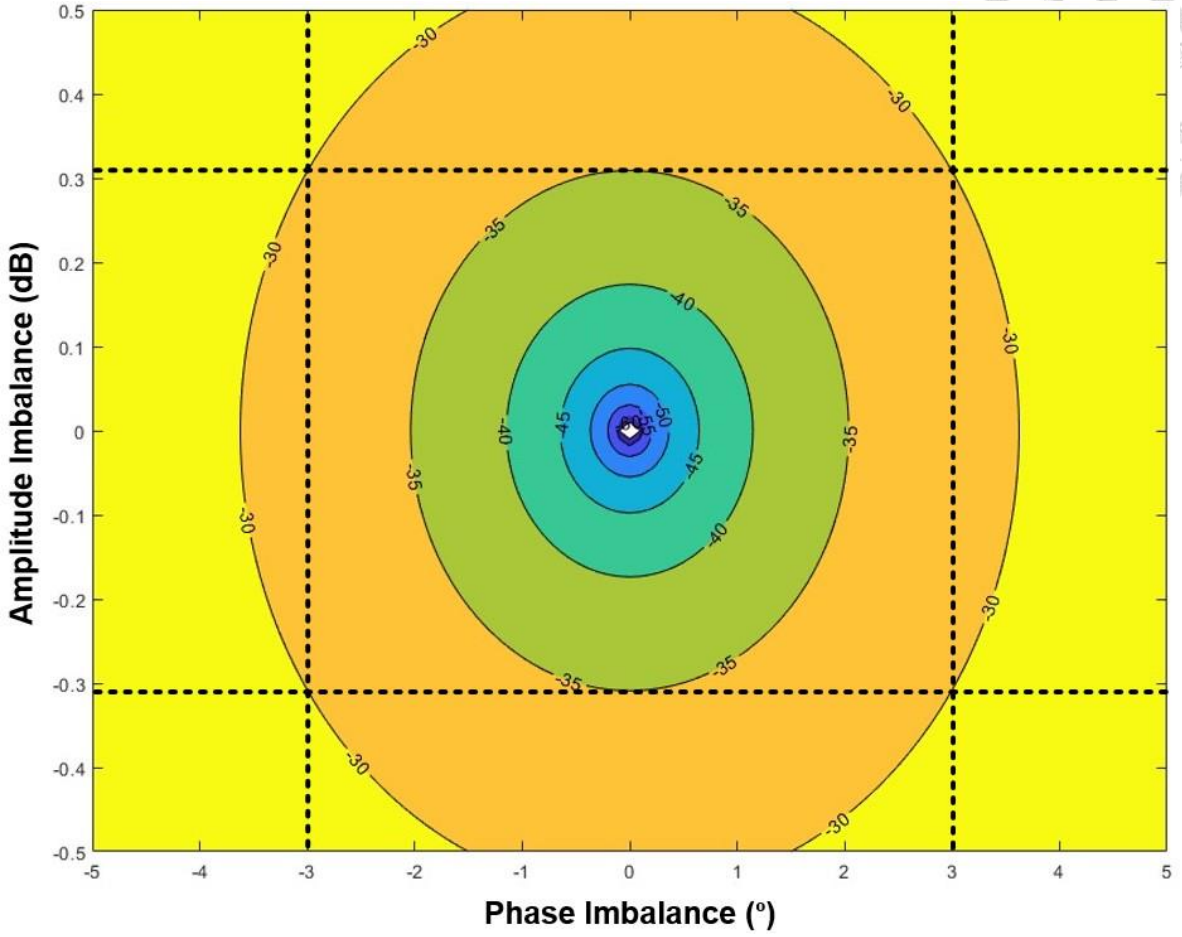


Fig. 4.8 IRR contour with a 5° phase variation and a 0.5 dB amplitude variation when phase reference is 90°.

As the quadrature signal generator on the LO side, we use a Wilkinson power divider with left-/right-handed transmission lines. Since the mixer core is subharmonic, the phase difference of the quadrature signal is altered to 45°; on the RF side, we use a Wilkinson power divider as the signal divider/combiner. The Wilkinson power divider is used on both signal ends because its amplitude imbalance is typically small and it has a more flexible layout composition that can be varied dependent on the front or post circuits.

doi:10.6342/NTU202203942

We avoid the loss caused by complex wiring by employing a single-ended anti-parallel diode pair as the configuration of the subharmonic mixer core due to the few metal layers of 0.15μm GaAs pHEMT.

The high IRR up-/down-conversion subharmonic mixer is shown in Fig. 4.9. It is composed of a 45° LO power divider, an in-phase RF power divider/combiner, and two subharmonic mixer cores for I/Q paths. The IRR design goal is greater than 30 dB. The frequency design goals are the RF frequency ranges from 24 to 32 GHz, the LO frequency ranges from 10 to 14 GHz, and the IF frequency is 4 GHz. The next section will go into the design details of each block.

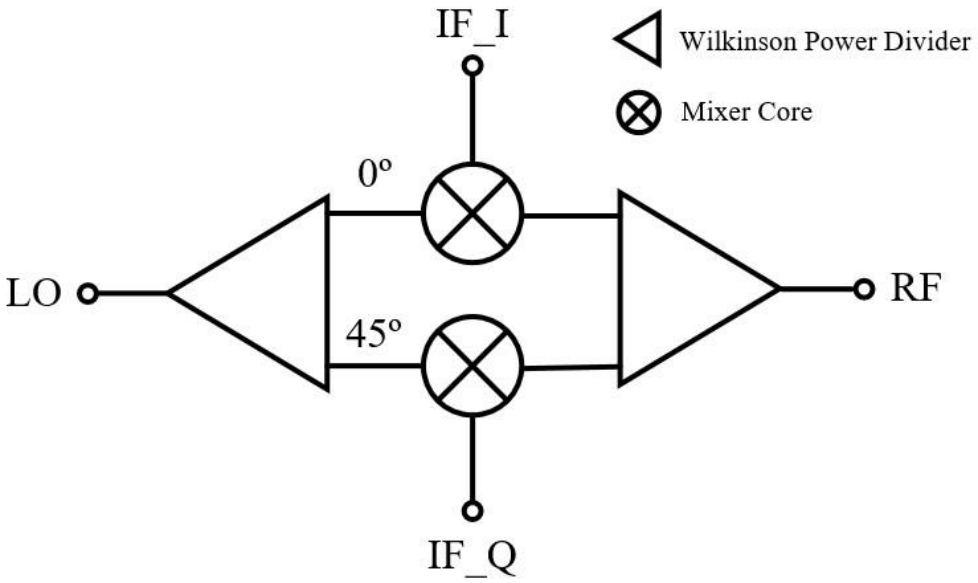


Fig. 4.9 Block diagram of the high IRR up-/down-conversion subharmonic mixer.

doi:10.6342/NTU202203942

4.2.2 45° LO Power Divider and In-Phase RF Power Divider/Combiner

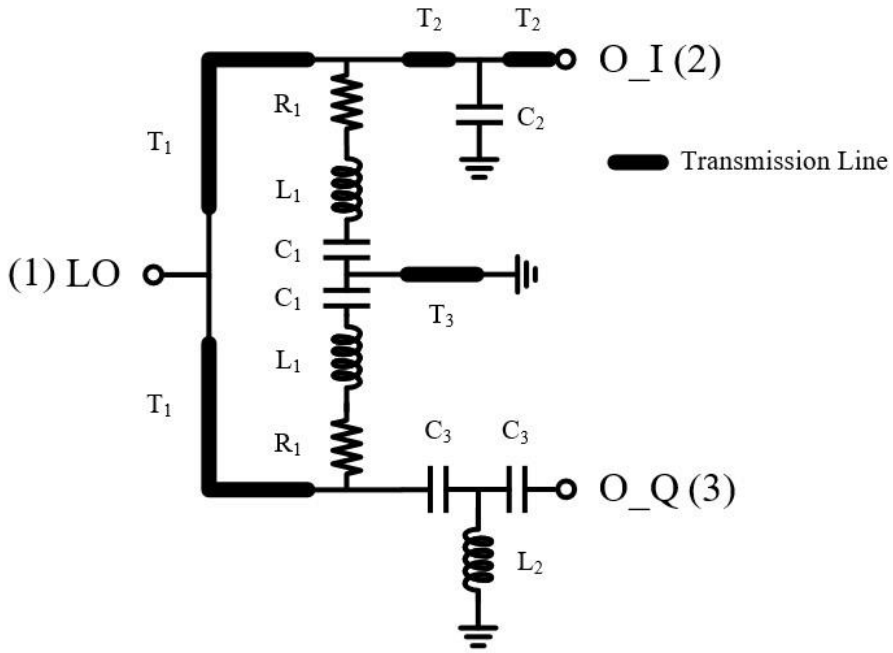


Fig. 4.10 Proposed 45° LO power divider.

As shown in Fig. 4.10, the proposed 45° LO power divider is composed of a modified Wilkinson power divider [38] and left-/right-handed transmission lines with a 45° phase difference. Ports O_I and O_Q connect to the mixer cores. According to [39], the IRR performance will be degraded by limited isolation between the I/Q LO ports even if a perfectly balanced quadrature generator is used. Because the generated I/Q signal will reflect certain signals due to the post-stage circuit's impedance mismatch, if the isolation between the I/Q LO ports is weak, the reflected signal from the I (or Q) path will leak to the Q (or I) path. As a result, the I/Q signal entering the mixer core has a considerable imbalance. To improve the isolation bandwidth, we require a modified Wilkinson power divider. According to [38], we can obtain R_1, L_1, and C_1 by the following equations

doi:10.6342/NTU202203942

$$R_1 = \frac{Y_0}{2 \cdot Y_{T1} \cdot Y_{T1}}, \tag{4.3}$$

$$L_1 = \frac{\pi}{\omega} \cdot \left(\frac{Y_{T1} + Y_{T1}}{8 \cdot Y_{T1} \cdot Y_{T1}} - \frac{R_1^2}{32 \cdot Z_{T3}} \right), \tag{4.4}$$

$$C_1 = \left[\pi \cdot \omega \cdot \left(\frac{Y_{T1} + Y_{T1}}{8 \cdot Y_{T1} \cdot Y_{T1}} - \frac{R_1^2}{32 \cdot Z_{T3}} \right) \right]^{-1}, \tag{4.5}$$

and satisfy

$$Z_{T3} > \frac{R_1^2 \cdot Y_{T1} \cdot Y_{T1}}{4 \cdot (Y_{T1} + Y_{T1})}. \tag{4.6}$$

Y_0 denotes the system admittance, Y_{T1} denotes the admittance of T_1, Z_{T3} denotes the impedance of T_3, and ω denotes the angular frequency.

The system impedance is 50 Ω and the impedance of T_1 is $50\sqrt{2}$ Ω [15]. T_3 is a quarter-wavelength transmission line [38]. Based on Eq. (4.3)- Eq. (4.6), we can obtain $T_{1,3}$'s dimensions and lumped elements' values of the modified Wilkinson power divider at 12 GHz as shown in Table 4.1.

Table 4.1 Dimensions of $T_{1,3}$ and values of R_1, L_1, and C_1.

Each Part	Length (μm)/ Width (μm)
T_1	1916/ 27
T_3	1700/ 10
Each Element	Value (at 12 GHz)
R_1	45 Ω
L_1	558.1 pH

doi:10.6342/NTU202203942

C_1	196.3 fF

The configurations of the left-/right-handed transmission lines are shown in Fig. 3.14. The capacitance and inductance of the left-handed transmission line can be calculated by Eq. (3.15) and Eq. (3.16). A 50 Ω transmission line cannot be used as a right-handed transmission line because its line width occupies a lot of space in the layout. Therefore, we use a transmission line with a line width of 10 μm as the inductor in Fig. 3.14. The capacitance and inductance of the left-handed transmission line can be calculated by

$$C = \frac{\sin\theta}{\omega \cdot \sqrt{2} \cdot Z_0}, \tag{4.7}$$

and

$$L = \frac{\sqrt{2} \cdot Z_0}{\omega} \cdot \sqrt{\frac{1-\cos\theta}{1+\cos\theta}}. \tag{4.8}$$

Z_0 denotes the system impedance, ω denotes the angular frequency, and θ denotes the phase of the right-handed transmission line [23].

The system impedance is 50 Ω. Based on Eq. (3.15), Eq. (3.16), Eq. (4.7), and Eq. (4.8), we can obtain T_2's dimensions and lumped elements' values of the left-/right-handed transmission lines at 12 GHz as shown in Table 4.2.

doi:10.6342/NTU202203942

Table 4.2 Dimensions of T_2 and values of L_2, C_2, and C_3.

Each Part	Length (μm)/ Width (μm)
T_2	263/ 10 (165.1 pH at 12 GHz)
Each Element	Value (at 12 GHz)
L_2	1.52 nH
C_2	73 fF
C_3	1.59 pF

The layout of the 45° LO power divider is shown in Fig. 4.11. Length A is 1551.6 μm and length B is 1059.7 μm. The simulated S-parameters of the 45° LO power divider are shown in Fig. 4.12 and Fig. 4.13. Port numbers are shown in Fig. 4.10. $|S_{11}|$ is less than -18.2 dB from 10 to 14 GHz. $|S_{22}|$ and $|S_{33}|$ are both less than -21.4 dB from 10 to 14 GHz. $|S_{32}|$ is less than -18.3 dB from 10 to 14 GHz. $|S_{21}|$ and $|S_{31}|$ range from -4.1 to -3.5 dB from 10 to 14 GHz. The simulated phase difference and amplitude imbalance of the 45° LO power divider are shown in Fig. 4.14 and Fig. 4.15, respectively. There is a 2.3-(-1.7)° phase imbalance and a (-0.11)-0.04 dB amplitude imbalance from 10 to 14 GHz.

doi:10.6342/NTU202203942

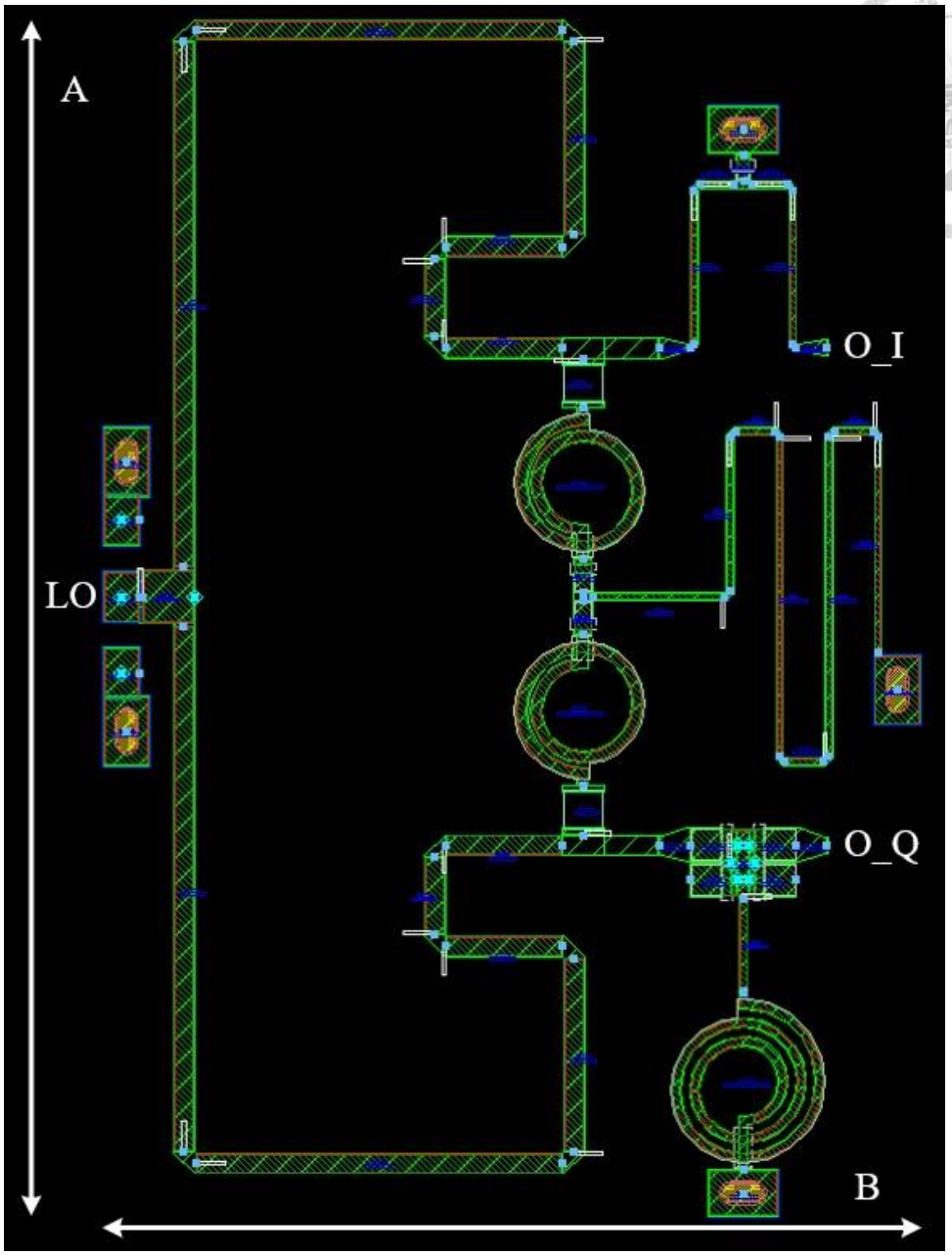


Fig. 4.11 Layout of the 45° LO power divider.

doi:10.6342/NTU202203942

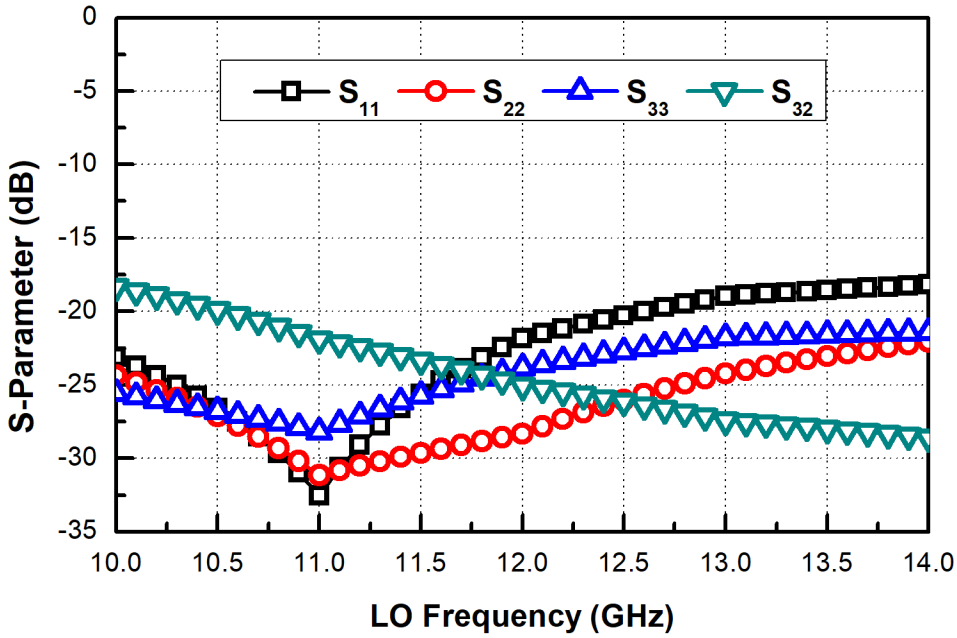


Fig. 4.12 Simulated S-parameter ($S_{11,22,33,32}$) of the 45° LO power divider in Fig. 4.10.

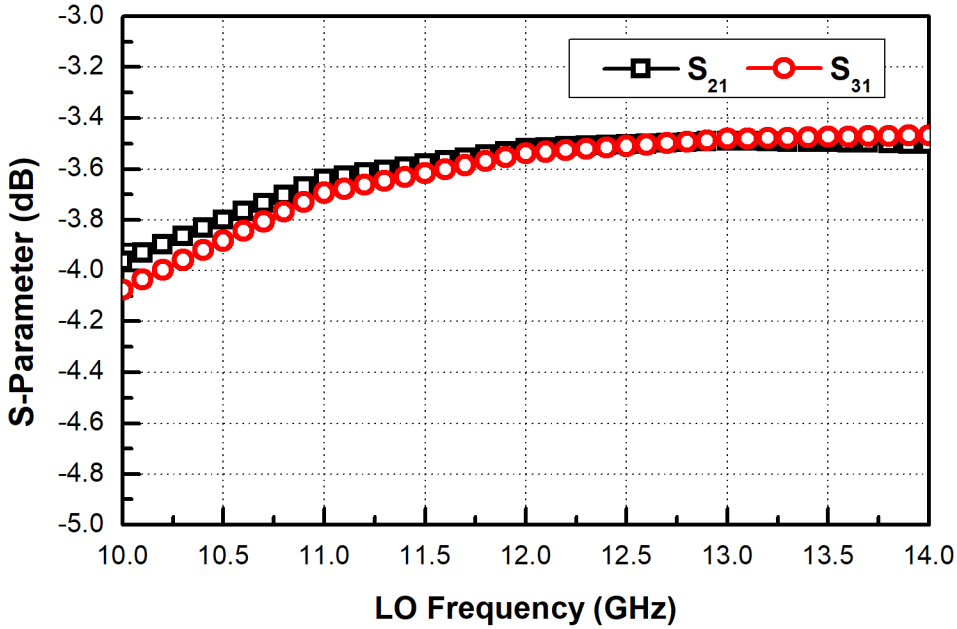


Fig. 4.13 Simulated S-parameter ($S_{21,31}$) of the 45° LO power divider in Fig. 4.10.

doi:10.6342/NTU202203942

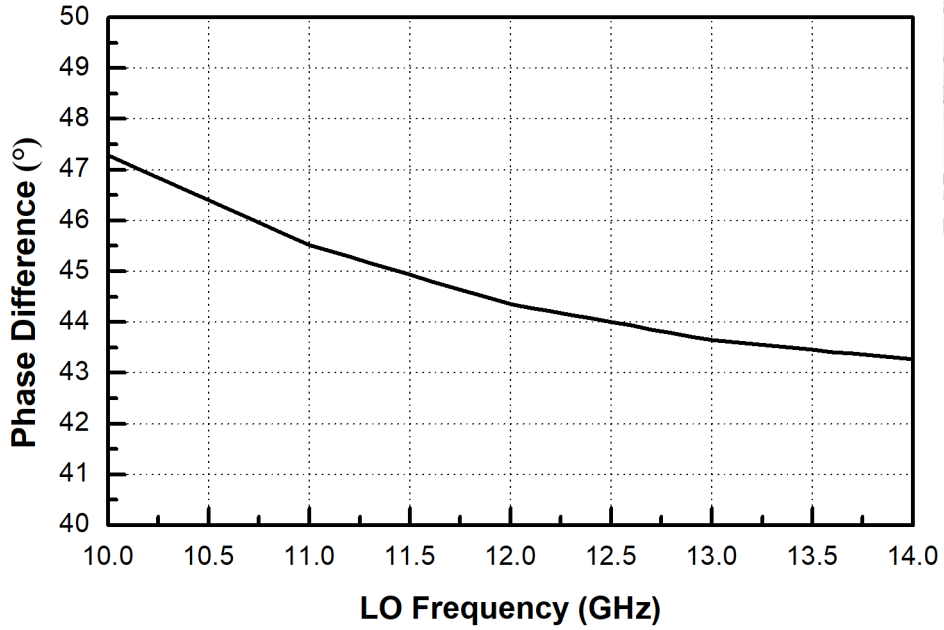


Fig. 4.14 Simulated phase difference between the 45° LO power divider's port 2,3 in Fig. 4.10.

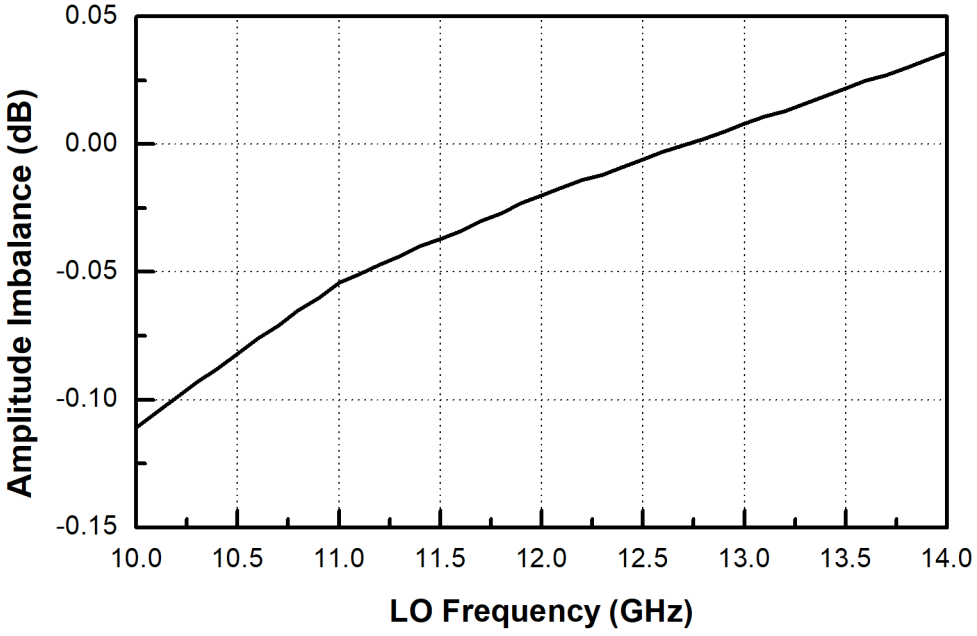


Fig. 4.15 Simulated amplitude imbalance between the 45° LO power divider's port 2,3 in Fig. 4.10.

doi:10.6342/NTU202203942

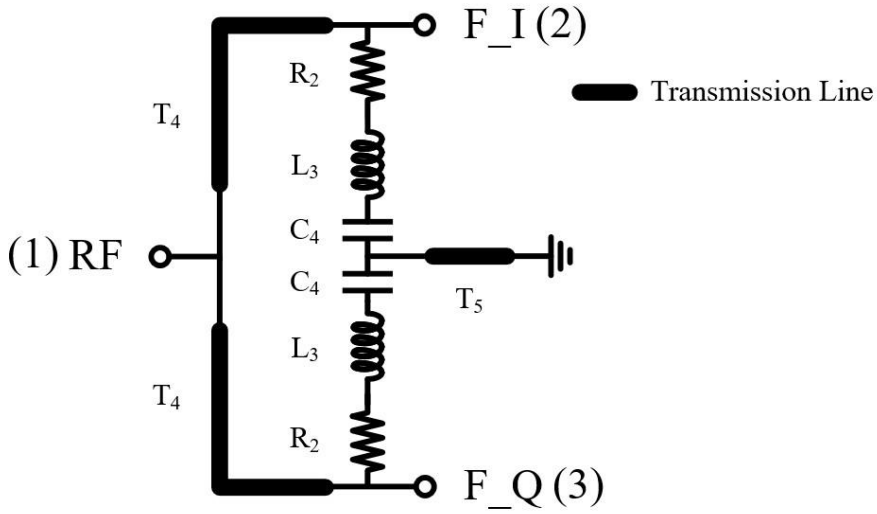


Fig. 4.16 Proposed in-phase RF power divider/combiner.

As shown in Fig. 4.16, the proposed in-phase RF power divider/combiner is a modified Wilkinson power divider. Ports F_I and F_Q connect to the mixer cores. The system impedance is 50 Ω and the impedance of T_4 is $50\sqrt{2}$ Ω [15]. T_5 is a quarter-wavelength transmission line [38]. Based on Eq. (4.3)- Eq. (4.6), we can obtain $T_{4,5}$'s dimensions and lumped elements' values of the modified Wilkinson power divider at 28 GHz as shown in Table 4.3.

doi:10.6342/NTU202203942

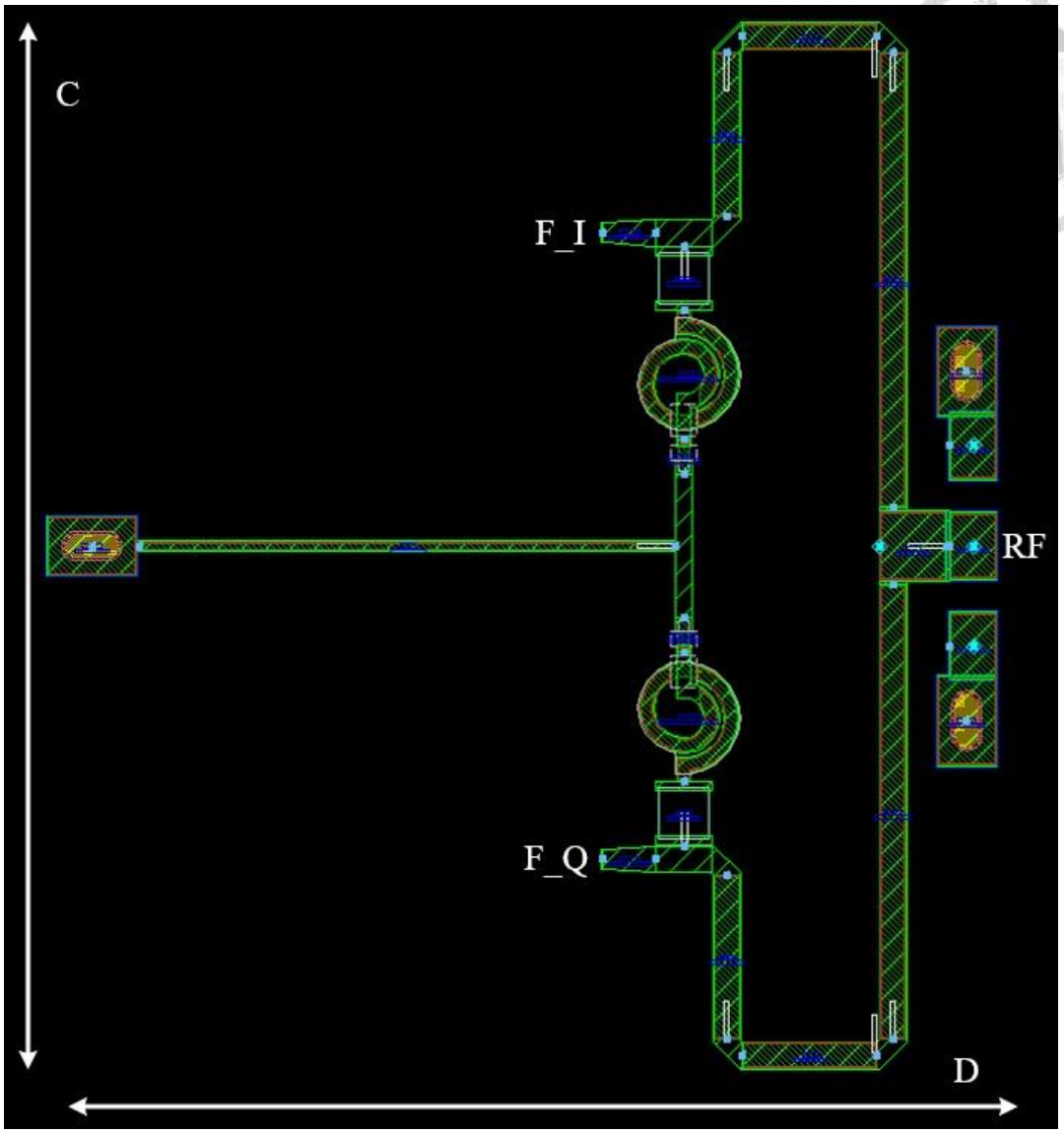


Fig. 4.17 Layout of the in-phase RF power divider/combiner.

doi:10.6342/NTU202203942

Table 4.3 Dimensions of $T_{4,5}$ and values of R_2, L_3, and C_4.

Each Part	Length (μm)/ Width (μm)
T_4	820.5/ 27
T_5	536/ 10
Each Element	Value (at 28 GHz)
R_2	45.1 Ω
L_3	248.2 pH
C_4	63.4 fF

The layout of the in-phase RF power divider/combiner is shown in Fig. 4.17. Length C is 1044.9 μm and length D is 949.6 μm. The simulated S-parameters of the in-phase RF power divider/combiner are shown in Fig. 4.18 and Fig. 4.19. Port numbers are shown in Fig. 4.16. $|S_{11}|$ is less than -15 dB from 24 to 32 GHz. $|S_{22}|$ and $|S_{33}|$ are both less than -19.7 dB from 24 to 32 GHz. $|S_{32}|$ is less than -14.5 dB from 24 to 32 GHz. $|S_{21}|$ and $|S_{31}|$ range from -3.7 to -3.4 dB from 24 to 32 GHz. The simulated phase difference and amplitude imbalance of the in-phase RF power divider/combiner are shown in Fig. 4.20 and Fig. 4.21, respectively. There is a 0.05-0.06° phase difference and a 0.005-0.009 dB amplitude imbalance from 24 to 32 GHz.

doi:10.6342/NTU202203942

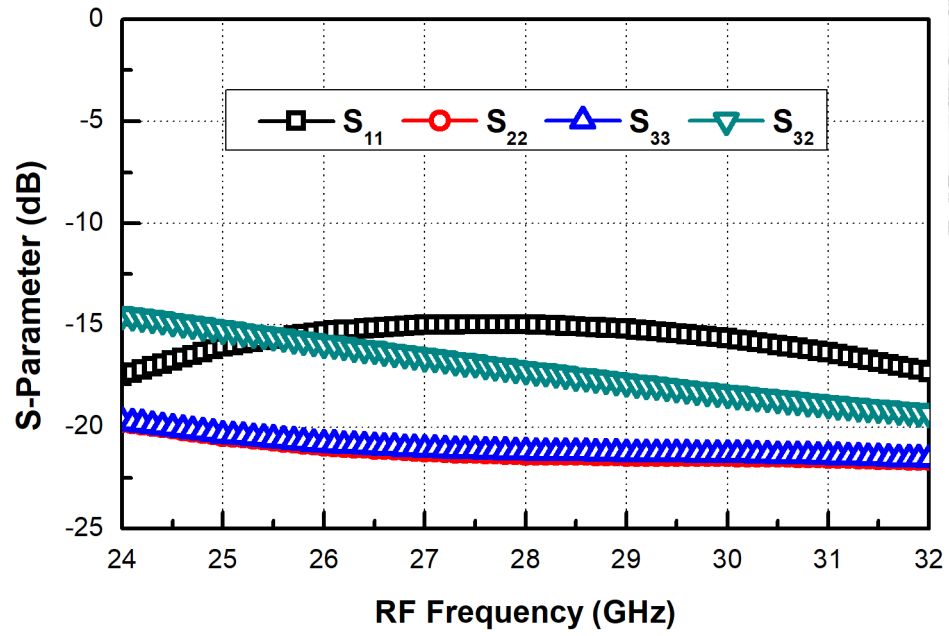


Fig. 4.18 Simulated S-parameter ($S_{11,22,33,32}$) of the in-phase RF power divider/combiner in Fig. 4.16.

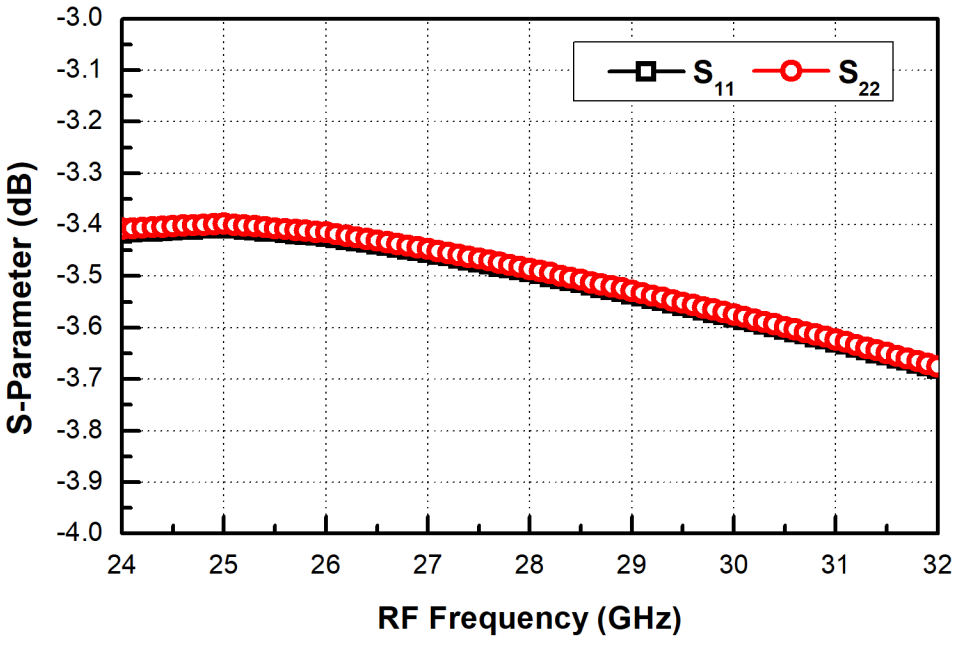


Fig. 4.19 Simulated S-parameter ($S_{21,31}$) of the in-phase RF power divider/combiner in Fig. 4.16.

doi:10.6342/NTU202203942

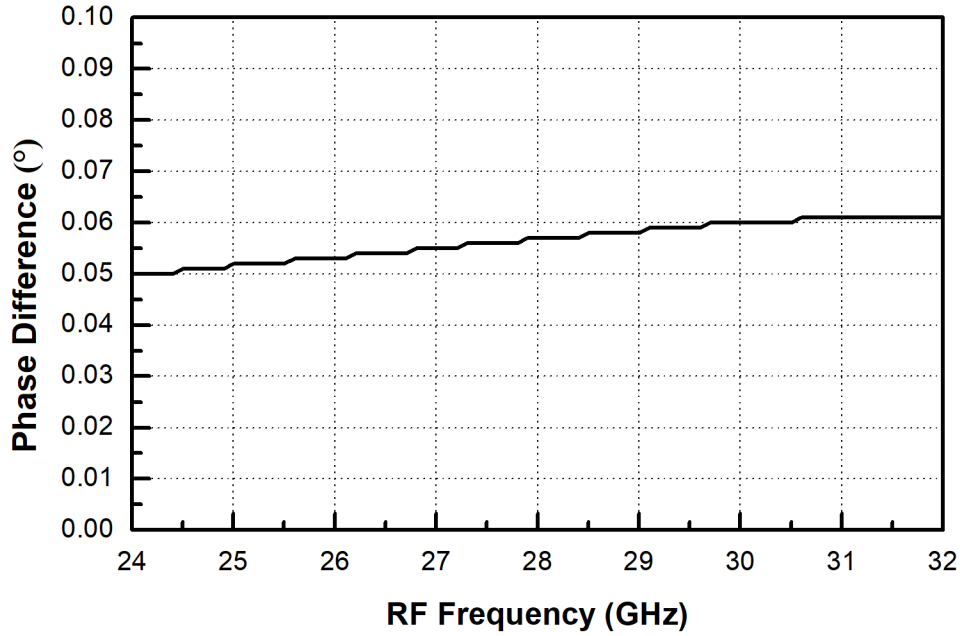


Fig. 4.20 Simulated phase difference of the in-phase RF power divider/combiner in Fig. 4.16.

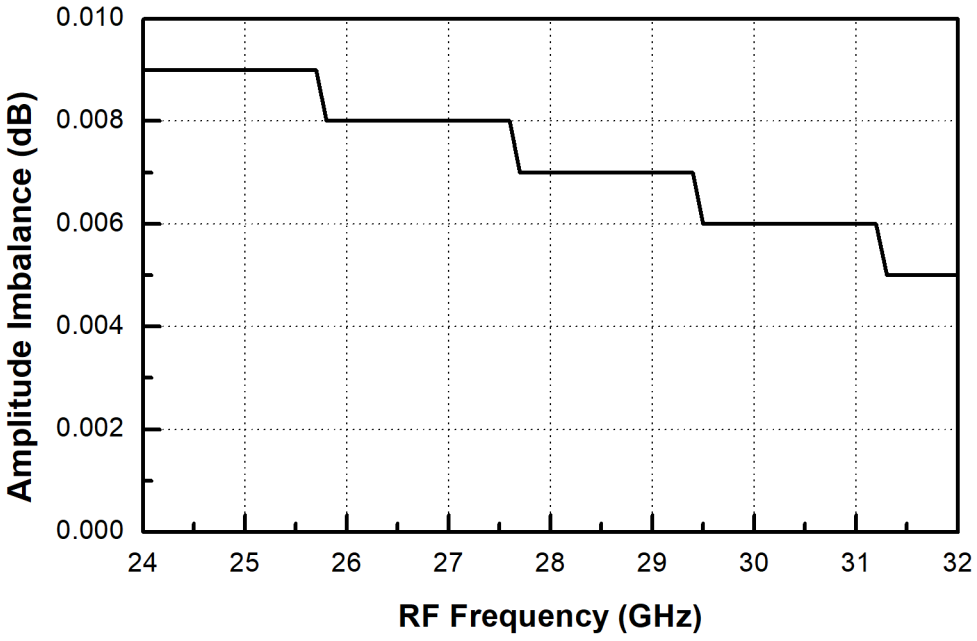


Fig. 4.21 Simulated amplitude imbalance of the in-phase RF power divider/combiner in Fig. 4.16.

doi:10.6342/NTU202203942

4.2.3 Subharmonic Mixer Core

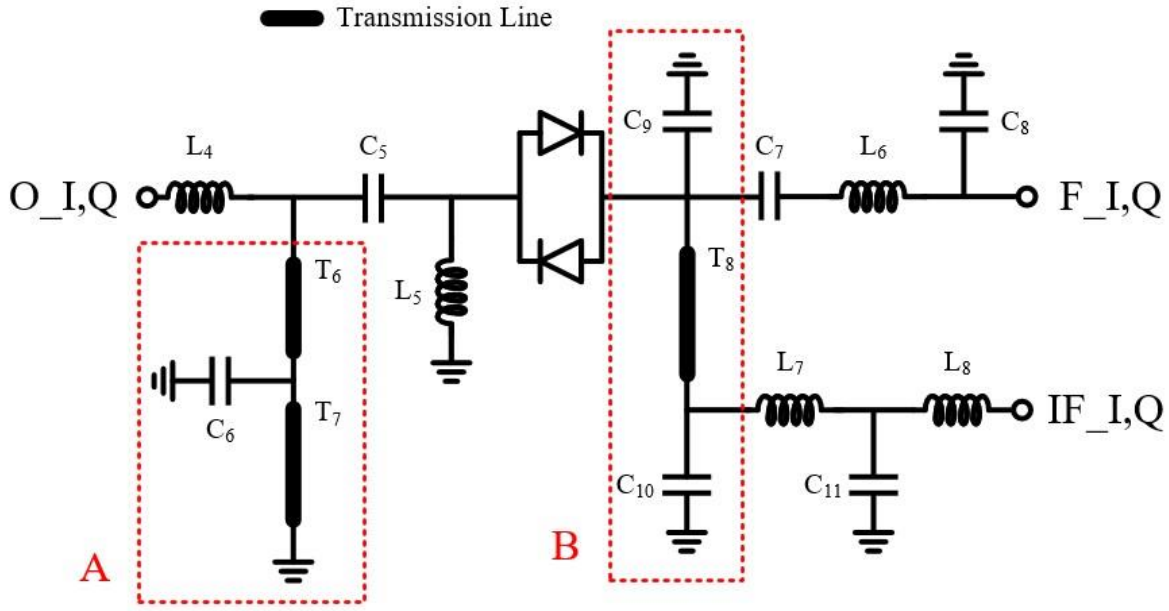


Fig. 4.22 Proposed subharmonic mixer core.

As shown in Fig. 4.22, the proposed subharmonic mixer core is composed of the quasi-lumped $\lambda_{LO}/4$ short/open stubs [40], a low-pass filter, an anti-parallel diode pair, and LO/RF inter-stage matching networks. Ports O_I,Q and F_I,Q connect to the 45° LO power divider and the in-phase RF divider/combiner, respectively. Port IF_I,Q connects to the external I/Q divider/combiner.

I. Quasi-Lumped $\lambda_{LO}/4$ Short/Open Stubs with Low-Pass Filter

Block A shows the quasi-lumped $\lambda_{LO}/4$ short stub, the function is to allow the LO signal through while blocking the RF signal. Block B shows the quasi-lumped $\lambda_{LO}/4$ open stub, the function is to allow the RF signal through while blocking the LO signal. The quasi-lumped $\lambda_{LO}/4$ short/open stubs provide a more compact area and wider bandwidth than the $\lambda_{LO}/4$ short/open stubs constructed by 50 Ω transmission lines. According to [40], we can obtain $T_{6,7}$ and C_6 in block A by the following equations.

doi:10.6342/NTU202203942

$$\tan\theta_{T7} = \alpha \cdot \beta - \sqrt{(\alpha \cdot \beta)^2 - 3}, \tag{4.9}$$

$$C_6 = \frac{1}{\omega_{LO} \cdot Z_{T7}} \cdot \left(\frac{1}{\tan\theta_{T7}} - \beta \cdot \tan\theta_{T6}\right), \tag{4.10}$$

$$\alpha = \frac{1 + 3 \cdot (\tan\theta_{T6})^2}{2 \cdot \tan\theta_{T6}}, \tag{4.11}$$

$$\beta = \frac{Z_{T7}}{Z_{T6}}, \tag{4.12}$$

and satisfy

$$\alpha \cdot \beta > 2. \tag{4.13}$$

$\theta_{T6,7}$ denotes the electrical length of $T_{6,7}$, $Z_{T6,7}$ denotes the impedance of $T_{6,7}$, and ω_{LO} denotes the angular LO frequency.

According to [40], we can obtain T_8 and $C_{9,10}$ in block B by the following equations.

$$C_{10} = \frac{1}{\omega_{LO} \cdot Z_{T8} \cdot \tan\theta_{T8}}, \tag{4.14}$$

and

$$C_9 = \frac{C_{10}}{3 + (\tan\theta_{T8})^2}. \tag{4.15}$$

θ_{T8} denotes the electrical length of T_8, Z_{T8} denotes the impedance of T_8, and ω_{LO} denotes the angular LO frequency.

Based on Eq. (4.9)- Eq. (4.15), we can obtain $T_{6,7,8}$'s dimensions and $C_{6,9,10}$'s capacitance of the quasi-lumped $\lambda_{LO}/4$ short/open stubs at 12 GHz as shown in Table 4.4. We construct a low-pass filter with C_{10}, the lumped elements' values of the low-pass filter at 4 GHz as shown in Table 4.4.

doi:10.6342/NTU202203942

Table 4.4 Dimensions of $T_{6,7,8}$ and values of $L_{7,8}$ and $C_{6,9,10,11}$.

Each Part	Length (μm)/ Width (μm)
T_6	80/ 50
T_7	717.9/ 10
T_8	443.9/ 10
Each Element	Value (at 12 GHz)
C_6	329 fF
C_9	46.9 fF
C_{10}	692.1 fF
Each Element	Value (at 4 GHz)
L_7	1.23 nH
L_8	615.8 pH
C_{10}	614.7 fF
C_{11}	1.07 pF

The layout of the quasi-lumped $\lambda_{LO}/4$ short stub is shown in Fig. 4.23. The simulated insertion coefficient of the quasi-lumped $\lambda_{LO}/4$ short stub is shown in Fig. 4.24. It is -0.9 dB at 10 GHz, -0.6 dB at 14 GHz, and has a maximum of -0.5 dB at 12 GHz; it is -12.7 dB at 24 and 32 GHz and has a minimum of -28.7 dB at 27 GHz.

doi:10.6342/NTU202203942

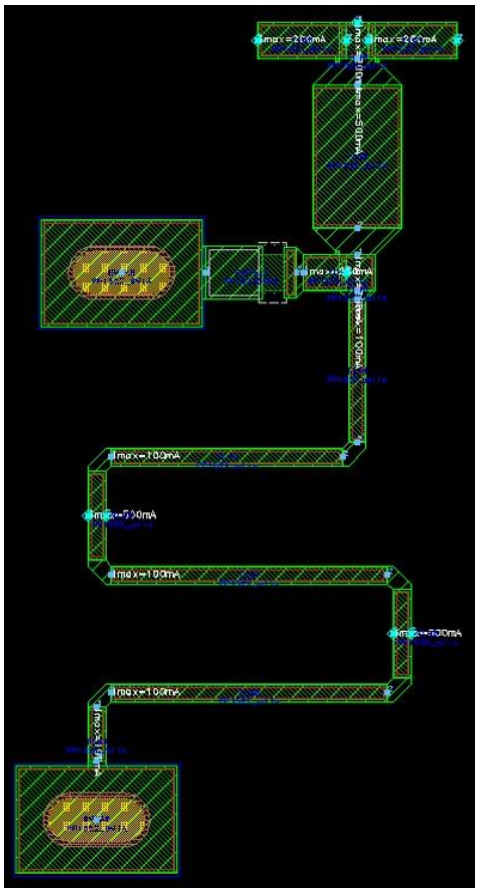


Fig. 4.23 Layout of the quasi-lumped $\lambda_{LO}/4$ short stub.

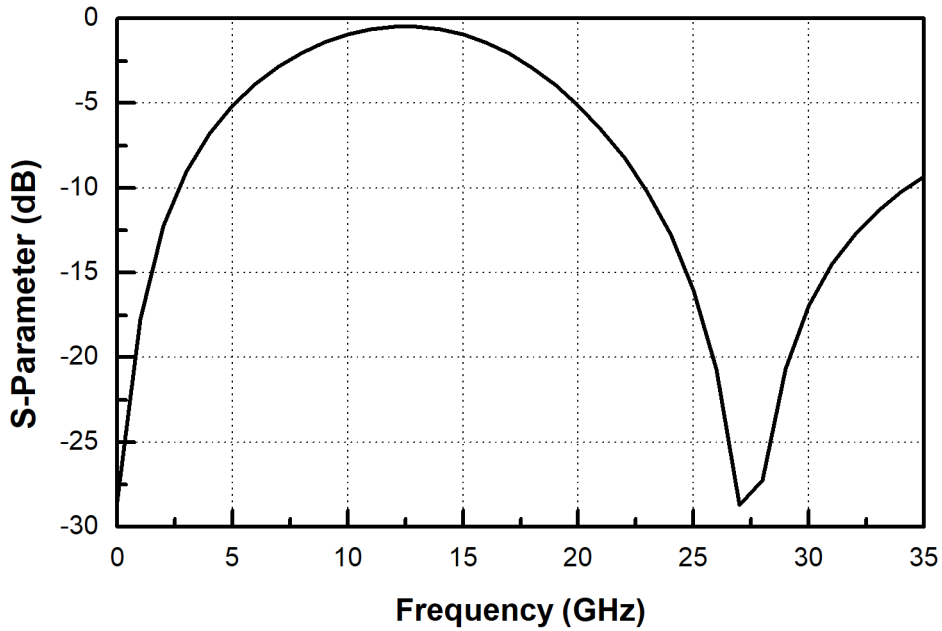


Fig. 4.24 Simulated insertion coefficient of the quasi-lumped $\lambda_{LO}/4$ short stub.

doi:10.6342/NTU202203942

The layout of the quasi-lumped $\lambda_{LO}/4$ open stub with a low-pass filter is shown in Fig. 4.25. The simulated S-parameters of the quasi-lumped $\lambda_{LO}/4$ open stub with a low-pass filter are shown in Fig. 4.26. $|S_{21}|$ is -7 dB at 10 GHz, -9.7 dB at 14 GHz, -23.1 dB at 12 GHz, -1 dB at 24 GHz, and -0.3 dB at 32 GHz. $|S_{13}|$ and $|S_{23}|$ are (-3.7)-(-4.2) dB from 3 to 5 GHz and are both less than -16.8 dB when the frequency is greater than 10 GHz.

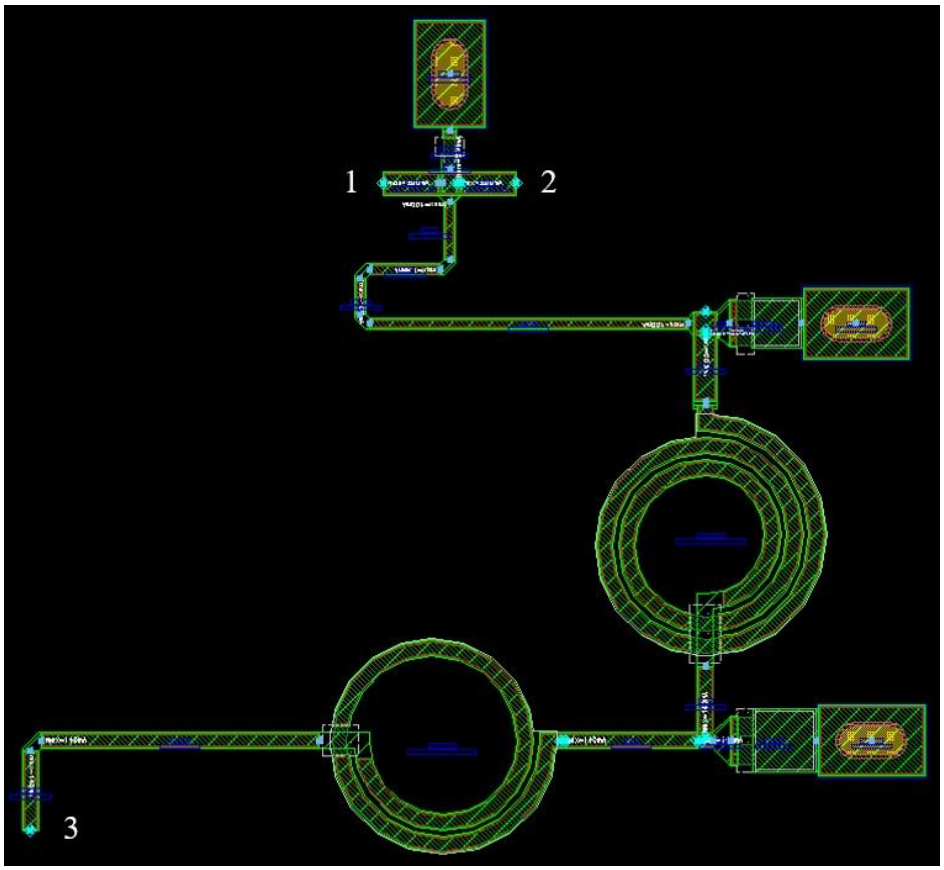


Fig. 4.25 Layout of the quasi-lumped $\lambda_{LO}/4$ open stub with a low-pass filter.

doi:10.6342/NTU202203942

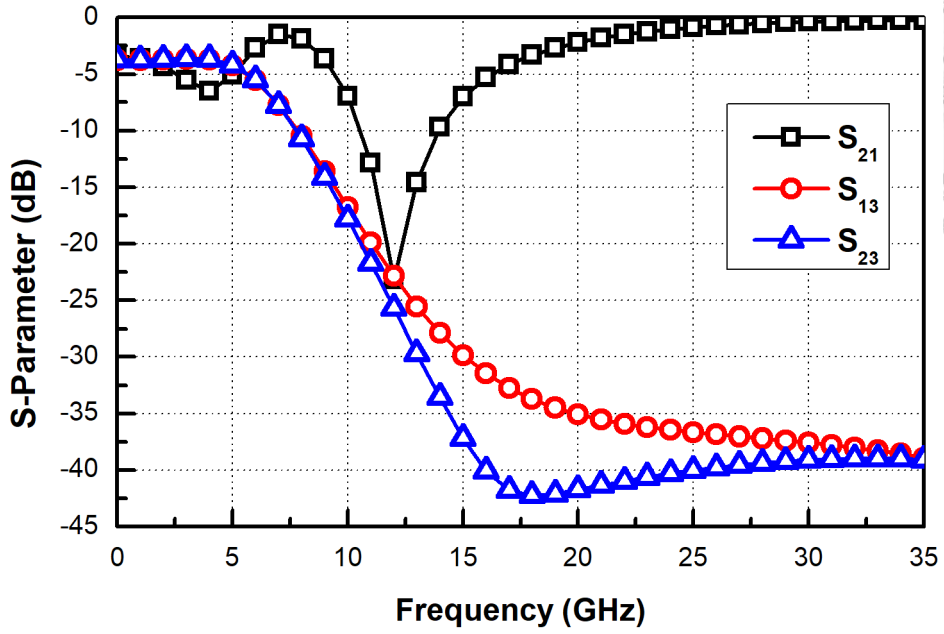


Fig. 4.26 Simulated S-parameter ($S_{21,13,23}$) of the quasi-lumped $\lambda_{LO}/4$ open stub with a low-pass filter (port 1,2,3 is shown in Fig. 4.25).

II. Diodes' Size Consideration

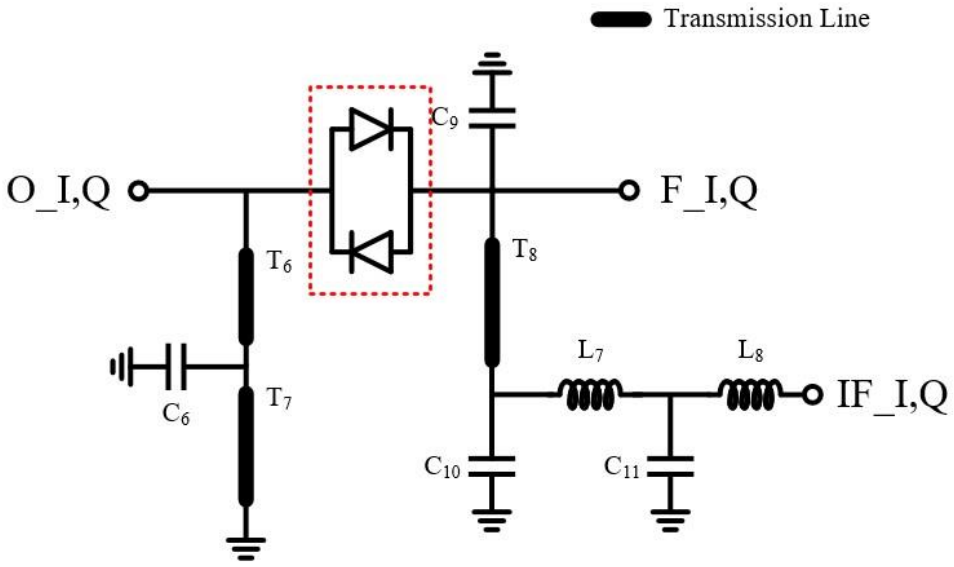


Fig. 4.27 Schematic of the subharmonic mixer core when considering diodes' size.

doi:10.6342/NTU202203942

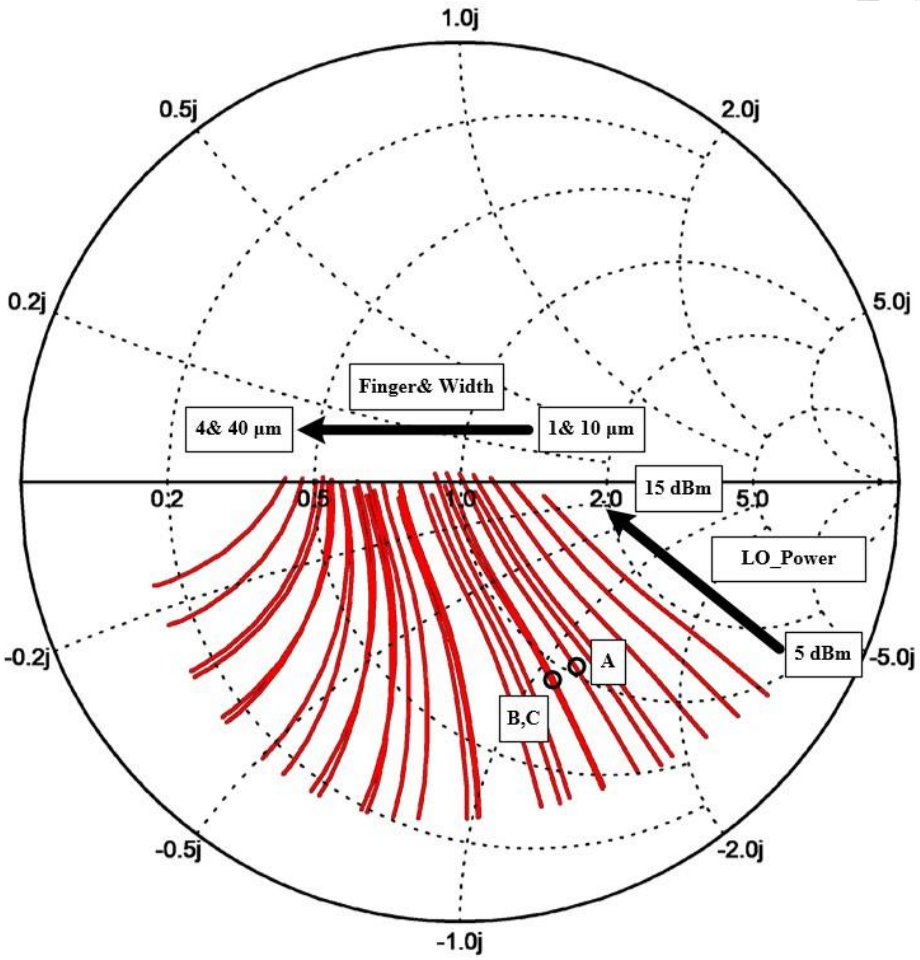


Fig. 4.28 LO power, diodes' finger number, and width sweeping (reflection coefficient on port O_I,Q in Fig. 4.27) at 12 GHz in the Smith chart.

We consider the diodes' size when the anti-parallel diode pair connect to the quasi-lumped $\lambda_{LO}/4$ short/open stubs with a low-pass filter as shown in Fig. 4.27. The LO power, diodes' finger number, and width sweeping of port O_I,Q's reflection coefficient at 12 GHz as shown in Fig. 4.28. The LO power has a sweeping range of 5-15 dBm; the diodes' finger number and width have a sweeping range of 1-4 and 10-40 μm, respectively. We choose points A, B, and C because they are close to the circle whose real part is equal to 1 (make matching easier) and have low LO power (8 dBm). The impedances of points A, B, and C are shown in Table 4.5. Then we employ ideal lumped elements for points A, B, and C's

doi:10.6342/NTU202203942

matching (reflection coefficient on port O_I,Q in Fig. 4.27) as shown in Fig. 4.29. The simulated conversion gain vs. LO power is shown in Fig. 4.30. Since size (finger= 1, width= 30 μm) has the largest conversion gain at 8 dBm, the diodes' size is determined.

Table 4.5 Impedance of points A, B, and C.

Point	Impedance (at 12 GHz, 8 dBm)	Finger/ Width (μm)
A	1.043-j1.179	1/ 30
B	0.902-j1.092	2/ 15
C	0.929-j1.078	1/ 35

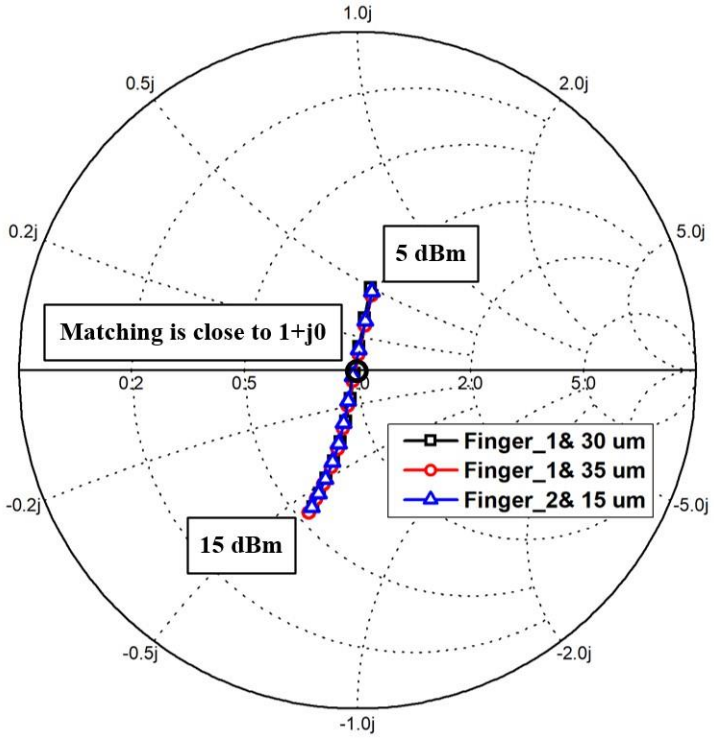


Fig. 4.29 Matching (reflection coefficient on port O_I,Q in Fig. 4.27) with ideal lumped elements of points A, B, and C.

doi:10.6342/NTU202203942

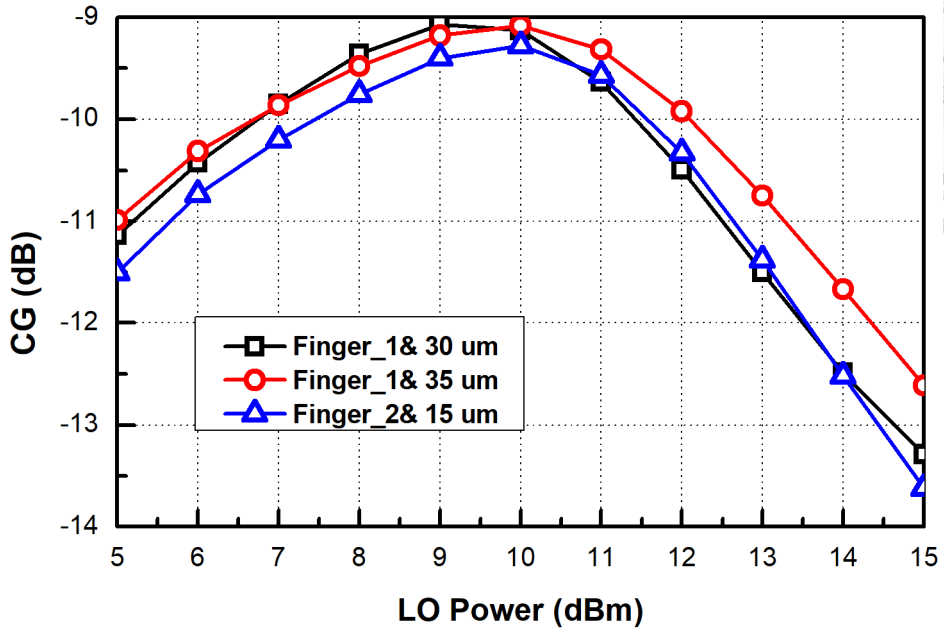


Fig. 4.30 Simulated conversion gain (CG) vs. LO power when considering the matching of points A, B, and C.

III. LO/RF Inter-Stage Matching Networks

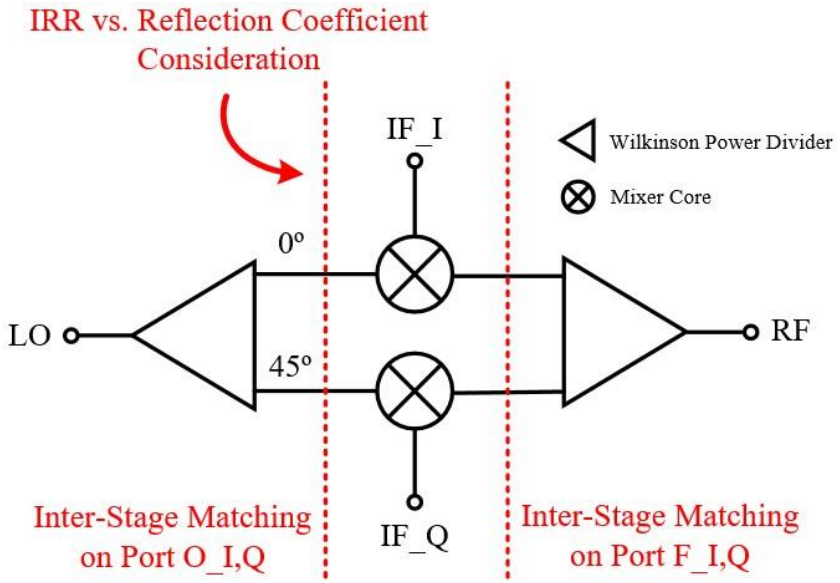


Fig. 4.31 Schematic of the high IRR up-/down-conversion subharmonic mixer when considering LO/RF matching networks (Ports O_I,Q/F_I,Q are shown in Fig. 4.27).

doi:10.6342/NTU202203942

According to [39], to obtain a high IRR over a wide bandwidth, not only the imbalances in phase and amplitude of the 45° LO power divider but also the LO reflections and/or the isolation between the 45° LO power divider's outputs should be improved. The proposed 45° LO power divider and in-phase RF power divider/combiner have small phase and amplitude imbalances with good isolation, we connect them to the mixer core in Fig. 4.27 and simulate the effect of the inter-stage reflection coefficient on IRR when LO power is 12 dBm as shown in Fig. 4.31 and Fig. 4.32. We choose 12 dBm as the LO power since the insertion loss of the 45° LO power divider is about 4 dB (I/Q path) and the mixer core needs 8 dBm for driving. To achieve an IRR greater than 30 dB, the inter-stage reflection coefficient must be at least -10 dB.

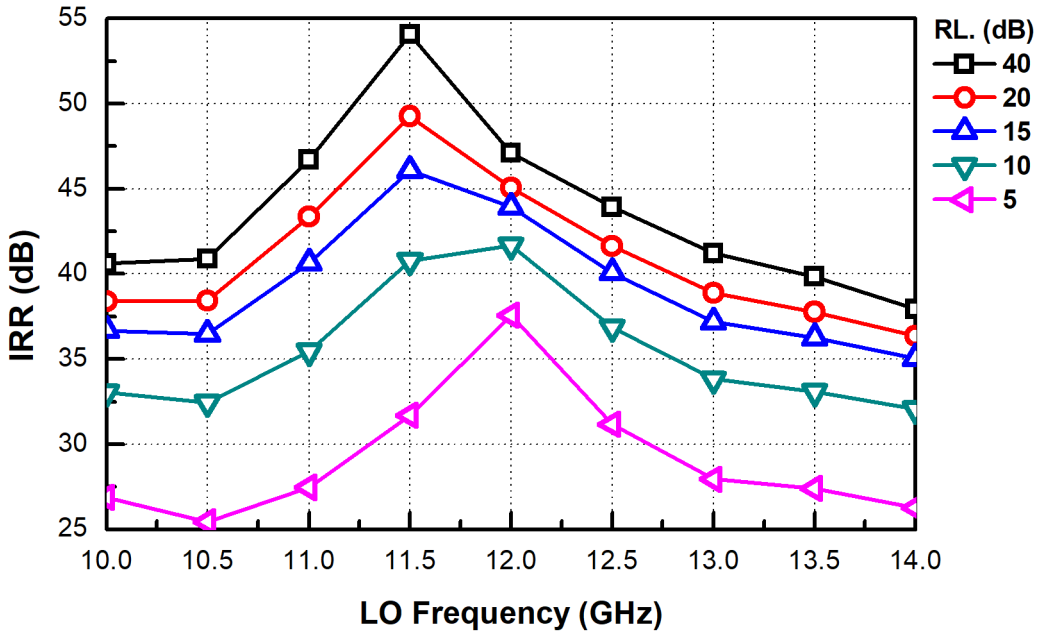


Fig. 4.32 Simulated IRR with different return losses (40, 20, 15, 10, and 5 dB).

doi:10.6342/NTU202203942

We construct the LO inter-stage matching network with a band-pass filter as shown in Fig. 4.33. The effect of the two connection ways (a) and (b) on the reflection coefficient is compared as shown in Fig. 4.34. Way (b) has a wider bandwidth. It is less than -11.8 dB from 10.5-14 GHz and is -8.3 dB at 10 GHz. The values of $L_{4b,5b}$ and C_{5b} as shown in Table 4.6.

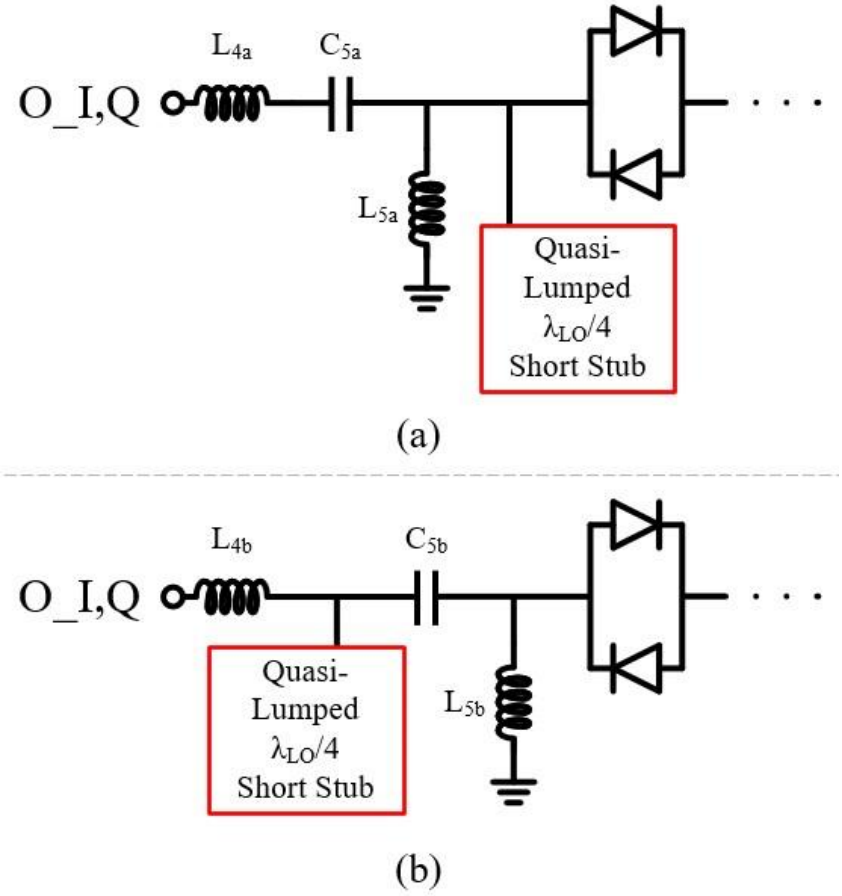


Fig. 4.33 LO inter-stage matching network with band-pass filter in two connection ways.

doi:10.6342/NTU202203942

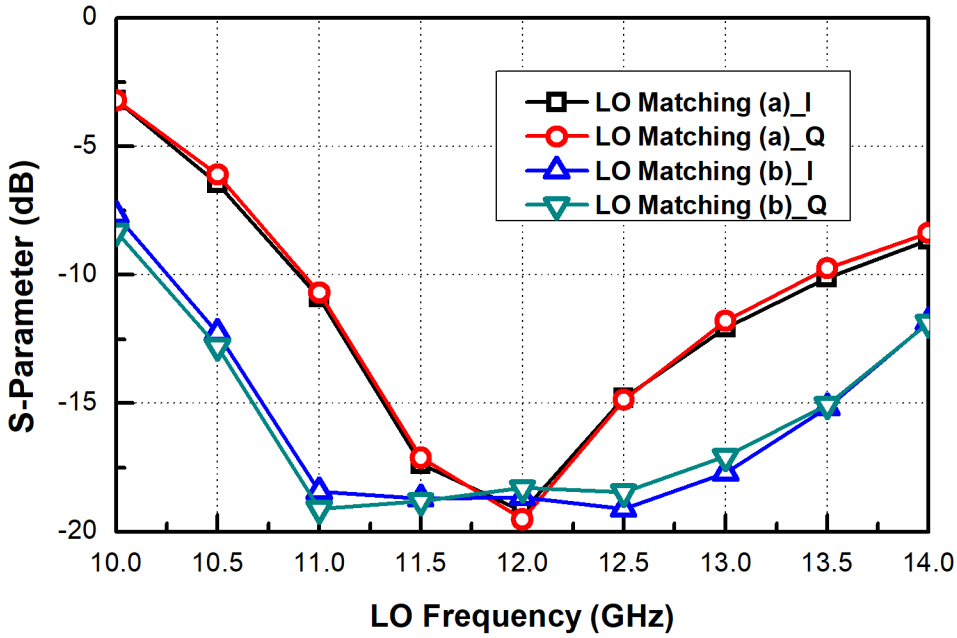


Fig. 4.34 Simulated reflection coefficients on port O_I,Q in Fig. 4.33.

Table 4.6 Values of $L_{4b,5b}$ and C_{5b}.

Each Element	Value (at 12 GHz)
L_{4b}	429.5 pH
L_{5b}	578.5 pH
C_{5b}	145.8 fF

doi:10.6342/NTU202203942

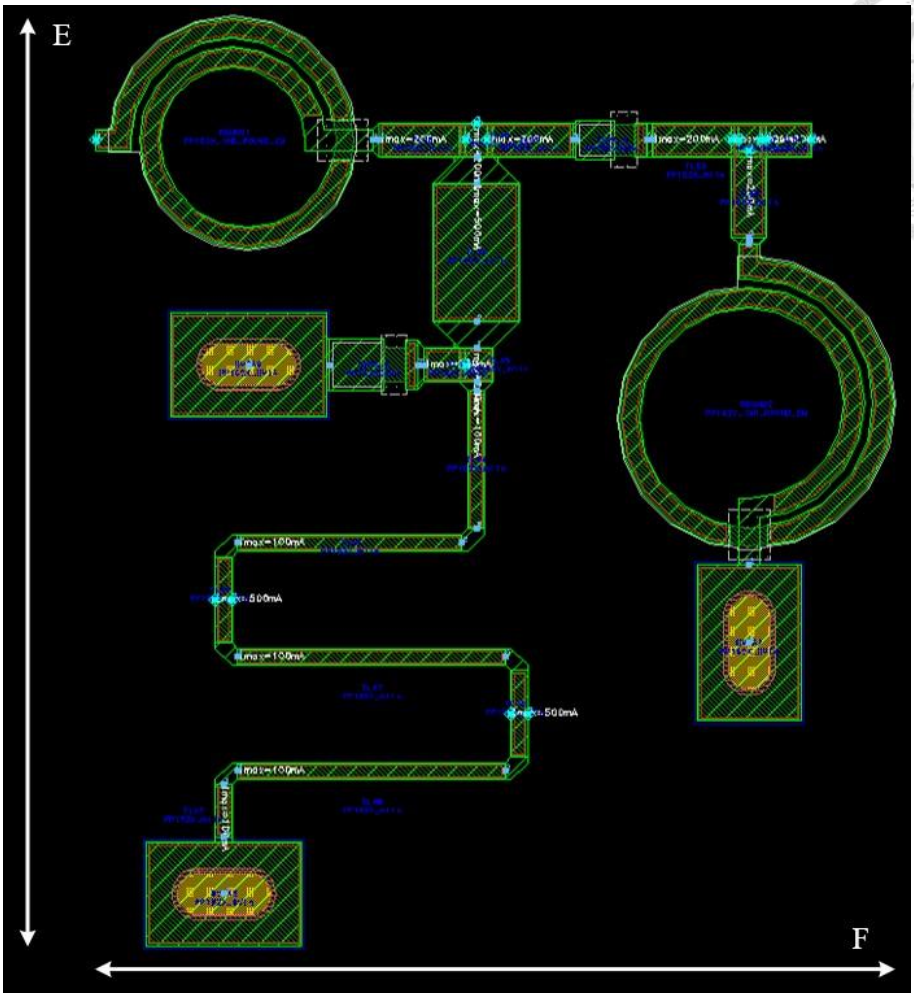


Fig. 4.35 Layout of the LO inter-stage matching network.

The layout of the LO inter-stage matching network is shown in Fig. 4.35. Length E is 537 μm and length F is 462 μm. The simulated insertion coefficient of the LO inter-stage matching network is shown in Fig. 4.36. It is -4.9 dB at 10 GHz, -2.9 dB at 14 GHz, and has a maximum of -2.5 dB at 12 GHz; it is -19.5 dB at 24 GHz, -15.6 dB at 32 GHz and has a minimum of -34.7 dB at 26 GHz.

doi:10.6342/NTU202203942

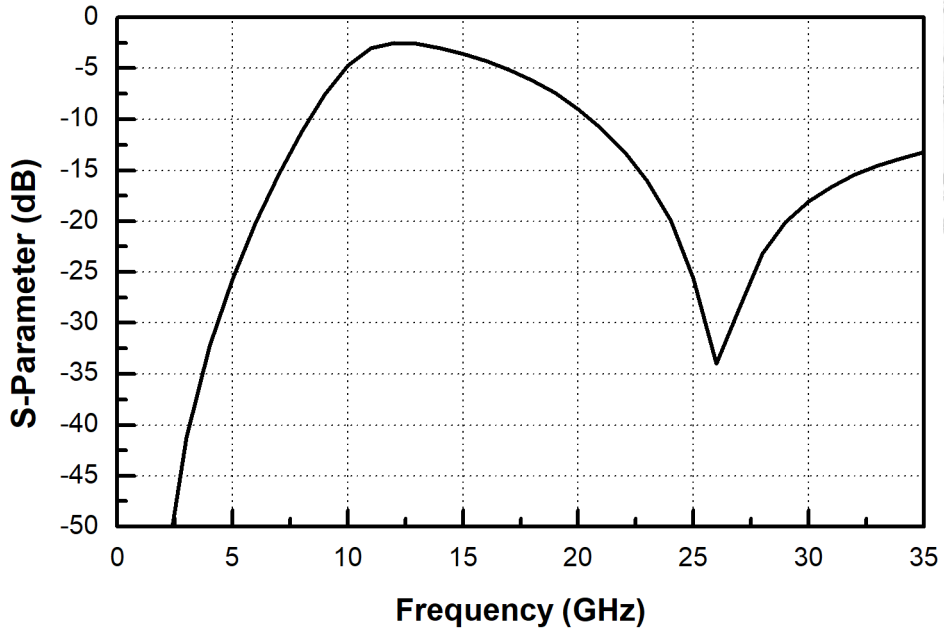


Fig. 4.36 Simulated insertion coefficient of the LO inter-stage matching network.

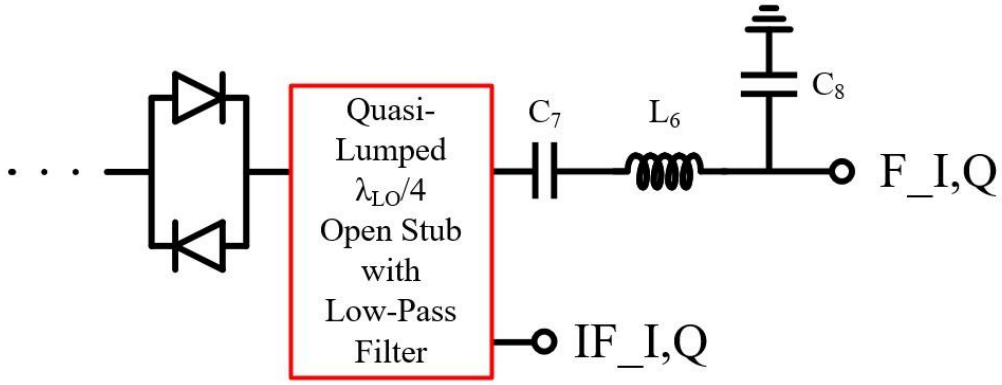


Fig. 4.37 RF inter-stage matching network with lumped elements.

We construct the RF inter-stage matching network with lumped elements as shown in Fig. 4.37. The purpose of this matching network is to block the IF signal and to regulate the gain variation of the RF signal within 3 dB at 24-32 GHz. The simulated reflection coefficient of the RF inter-stage matching network is shown in Fig. 4.38. It is less than -10 dB from 26-

doi:10.6342/NTU202203942

32 GHz and is (-6.3)-(-7.9) dB from 24 to 25 GHz. The values of L_6 and $C_{7,8}$ as shown in Table 4.7.

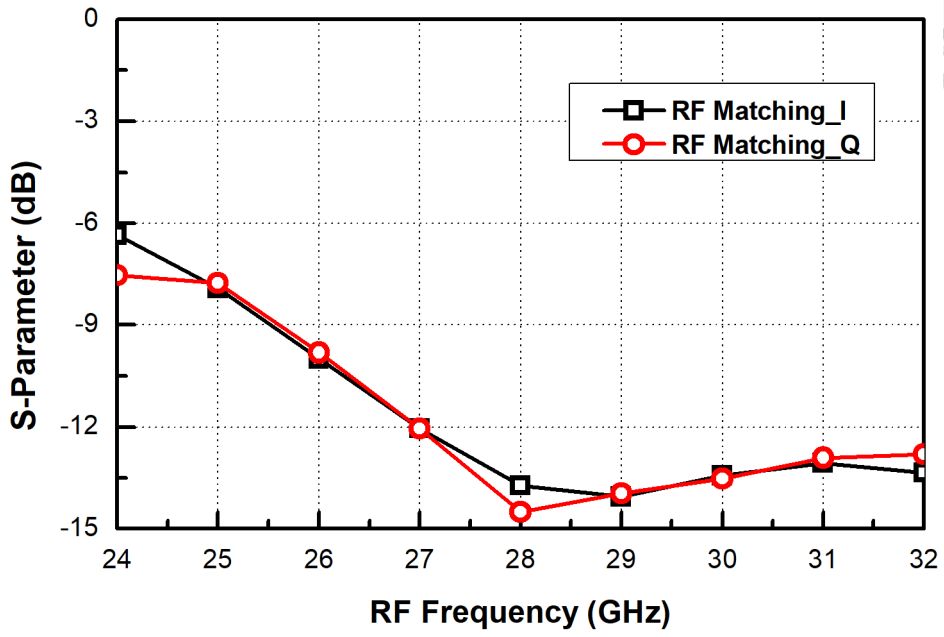


Fig. 4.38 Simulated reflection coefficients on port F_I,Q in Fig. 4.37.

Table 4.7 Values of L_6 and $C_{7,8}$.

Each Element	Value (at 28 GHz)
L_6	265.2 pH
C_7	142.3 fF
C_8	58.1 fF

doi:10.6342/NTU202203942

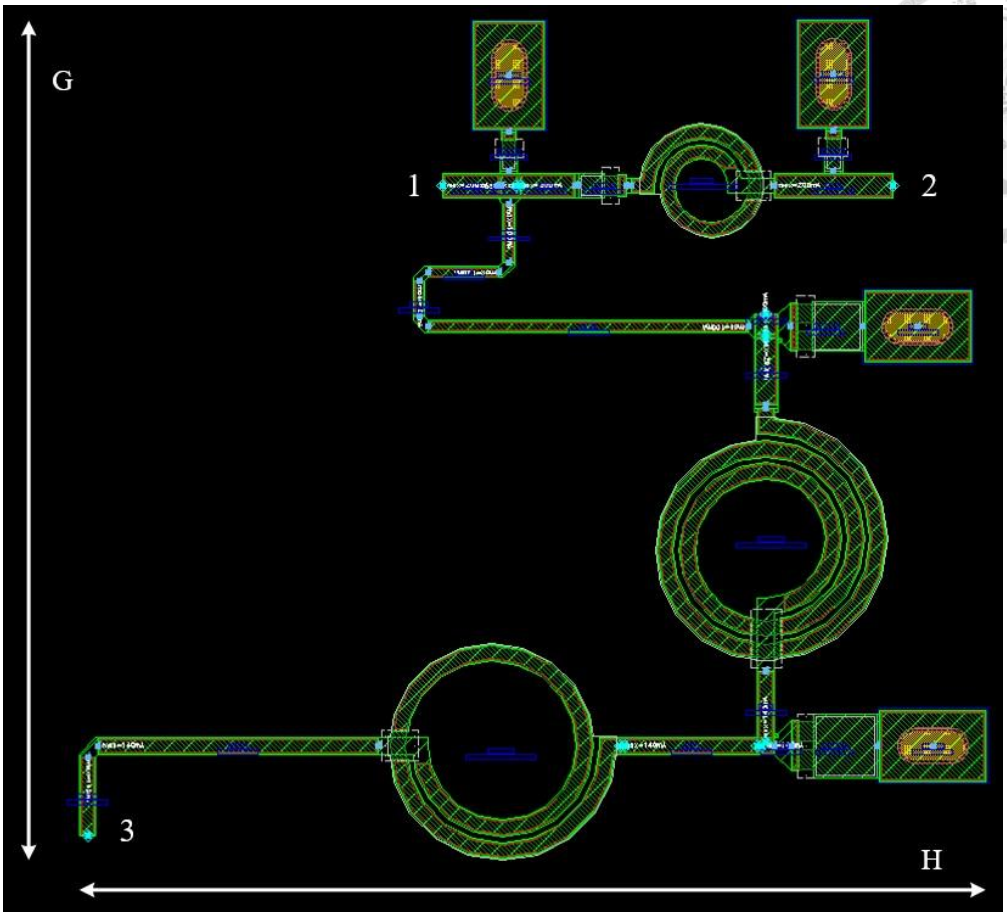


Fig. 4.39 Layout of the RF inter-stage matching network.

The layout of the RF inter-stage matching network is shown in Fig. 4.39. Length G is 707.5 μm and length H is 766 μm. The simulated S-parameters of the RF inter-stage matching network are shown in Fig. 4.40. Port numbers are shown in Fig. 4.39. $|S_{21}|$ is -15.1 dB at 10 GHz, -14.1 dB at 14 GHz, -30 dB at 12 GHz, -0.8 dB at 24 GHz, and -0.4 dB at 32 GHz. $|S_{13}|$ is (-1.2)-(-1.4) from 3 to 5 GHz and is less than -16.5 dB from 10 to 14 GHz. $|S_{23}|$ is less than -39.3 dB from 24 to 32 GHz.

doi:10.6342/NTU202203942

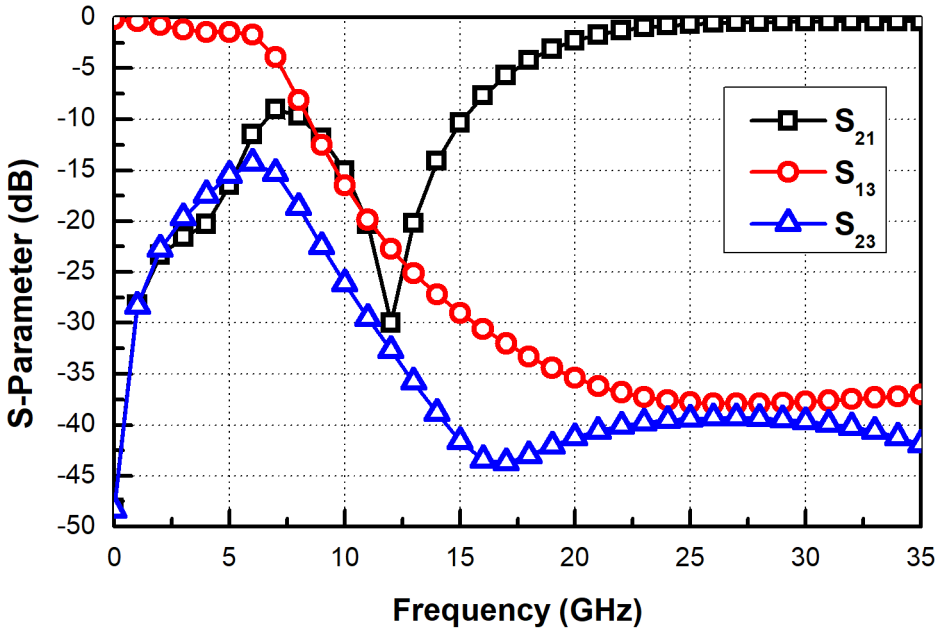


Fig. 4.40 Simulated S-parameter ($S_{21,13,23}$) of the RF matching network (port 1,2,3 is shown in Fig. 4.39).

doi:10.6342/NTU202203942

4.2.4 Simulations of The High IRR Up-/Down-Conversion Subharmonic Mixer

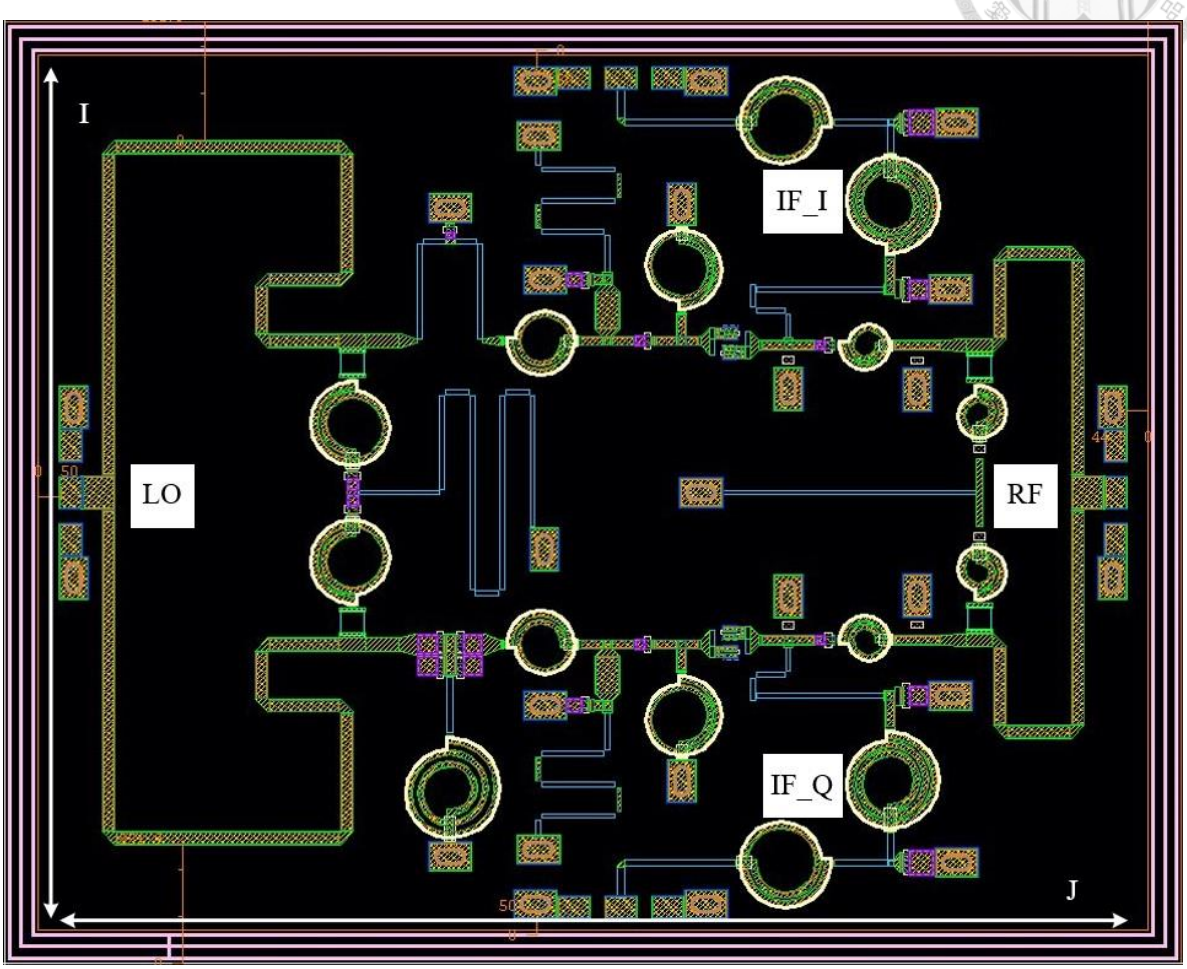


Fig. 4.41 Layout of the high IRR up-/down-conversion subharmonic mixer.

The layout of the high IRR up-/down-conversion subharmonic mixer is shown in Fig. 4.41. Length I is 1810 μm and length J is 2267.5 μm. We perform the simulations with the ideal 90° hybrid as shown in Fig. 4.42.

doi:10.6342/NTU202203942

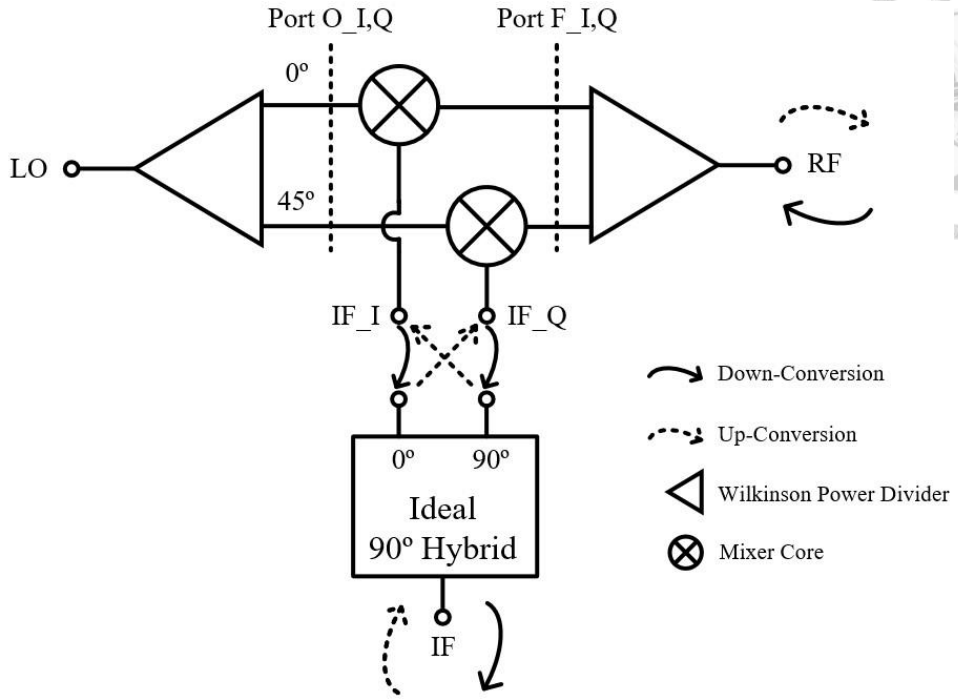


Fig. 4.42 Schematic of the high IRR up-/down-conversion subharmonic mixer when simulating with an ideal 90° hybrid.

The simulated conversion gain vs. LO power of the high IRR up-/down-conversion subharmonic mixer is shown in Fig. 4.43 when RF frequency is 28 GHz, LO frequency is 12 GHz, and IF frequency is 4 GHz. Conversion gain is calculated as IF minus RF (down-conversion) or RF minus IF (up-conversion) in Fig. 4.42. Although there is a maximum conversion gain at 10 dBm, it is reasonable to choose 12 dBm as the LO power since the insertion loss of the 45° LO power divider is about 4 dB (I/Q path) and the mixer core needs 8 dBm power for driving. It has a -10.9 dB conversion gain for up-conversion and -10.8 dB for down-conversion.

The simulated IP_{1dB} of the high IRR up-/down-conversion subharmonic mixer is shown in Fig. 4.44 when RF frequency is 28 GHz, LO frequency is 12 GHz, IF frequency is 4 GHz,

doi:10.6342/NTU202203942

and LO power is 12 dBm. Up-conversion is about 6 dBm and down-conversion is about 5 dBm.

The simulated bandwidth of the high IRR up-/down-conversion subharmonic mixer is shown in Fig. 4.45 when RF frequency is 24-32 GHz, IF frequency is 4 GHz, and LO power is 12 dBm. The conversion gain range of up-conversion is 1.8 dB and the conversion gain range of down-conversion is 1.7 dB from 10-14 GHz.

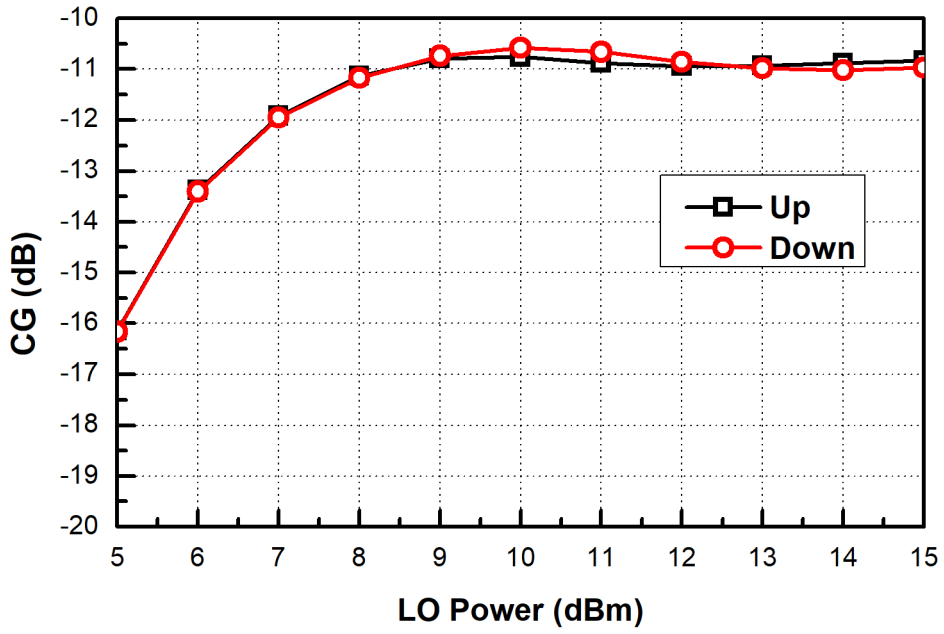


Fig. 4.43 Simulated conversion gain (CG) vs. LO power of the high IRR up-/down-conversion subharmonic mixer.

doi:10.6342/NTU202203942

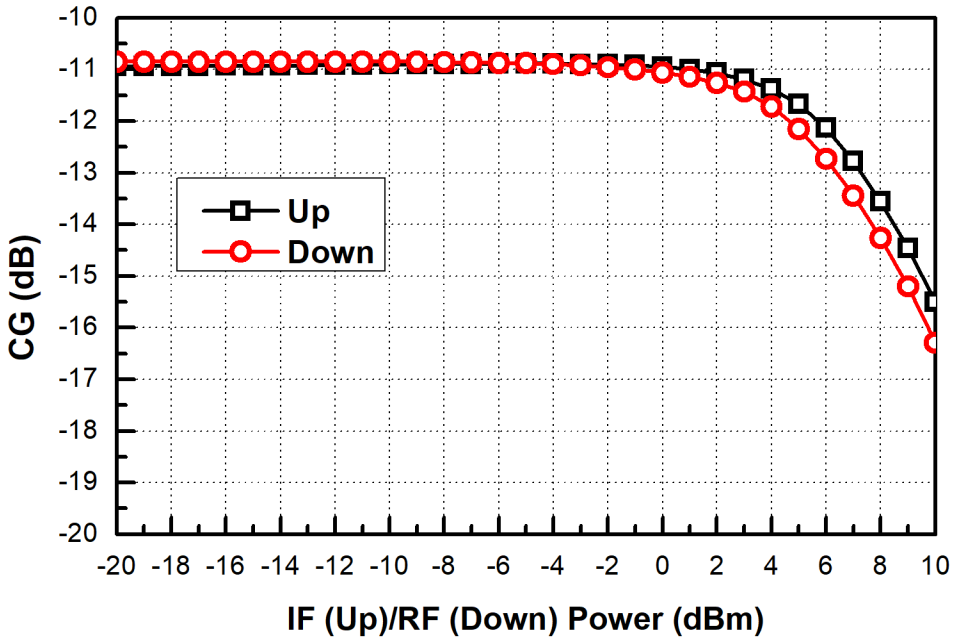


Fig. 4.44 Simulated conversion gain (CG) vs. IF (up-conversion)/RF (down-conversion) power of the high IRR up-/down-conversion subharmonic mixer.

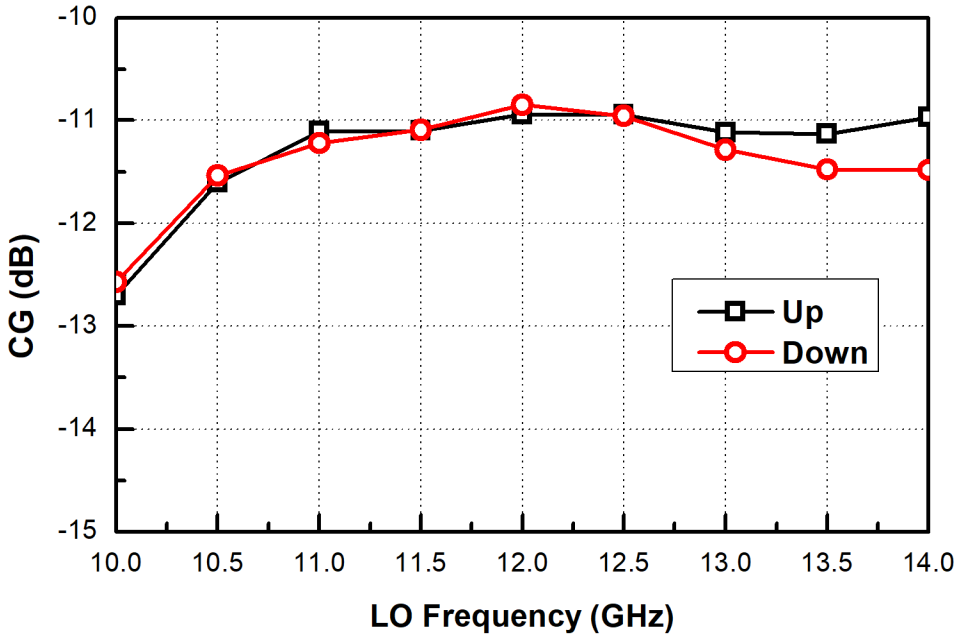


Fig. 4.45 Simulated conversion gain (CG) vs. bandwidth of the high IRR up-/down-conversion subharmonic mixer.

doi:10.6342/NTU202203942

The simulated IRR of the high IRR up-/down-conversion subharmonic mixer is shown in Fig. 4.46 when RF frequency is 24-32 GHz, IF frequency is 4 GHz, and LO power is 12 dBm. It is greater than 40.1 dB for up-conversion and greater than 33.8 dB for down-conversion from 10-14 GHz. According to [39], the nonzero phase and/or amplitude imbalances may partly be compensated by the phase and/or amplitude mismatches caused by the LO reflections. There is a (-0.5)-0.4° phase imbalance that can be obtained after optimizing the LO inter-stage matching network at 11.5-14 GHz as shown in Fig. 4.47. Without RF/IF signal combining, the image signal has less power on port F_I,Q/IF_I,Q in Fig. 4.42 than the RF signal, especially at 10-11.5 GHz as shown in Fig. 4.48/Fig. 4.49, respectively. This compensates for the larger phase imbalance between port O_I,Q at 10-11.5 GHz. Based on Fig. 4.47- Fig. 4.49, we can conclude that the IRR performance is great.

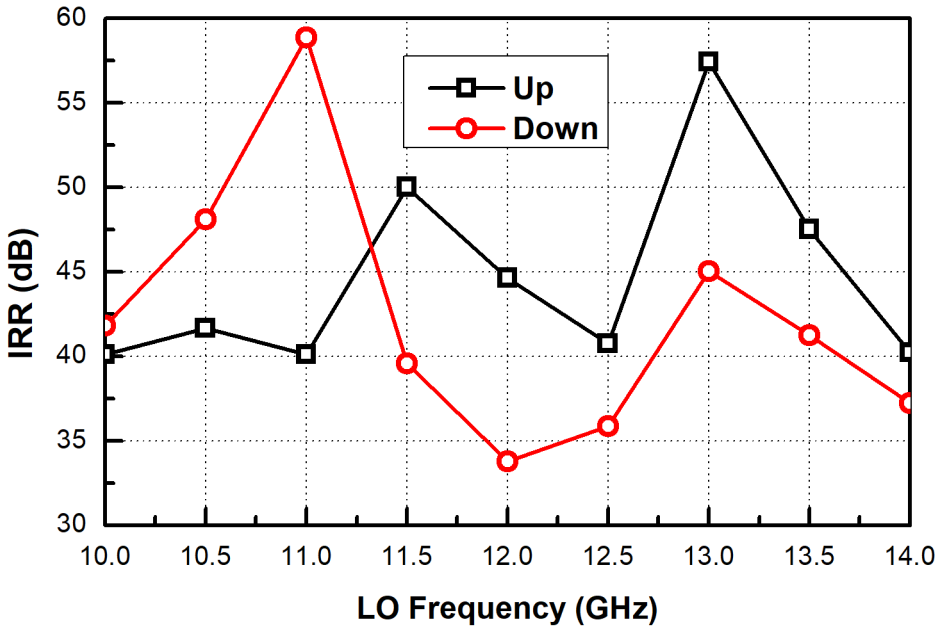


Fig. 4.46 Simulated IRR of the high IRR up-/down-conversion subharmonic mixer.

doi:10.6342/NTU202203942

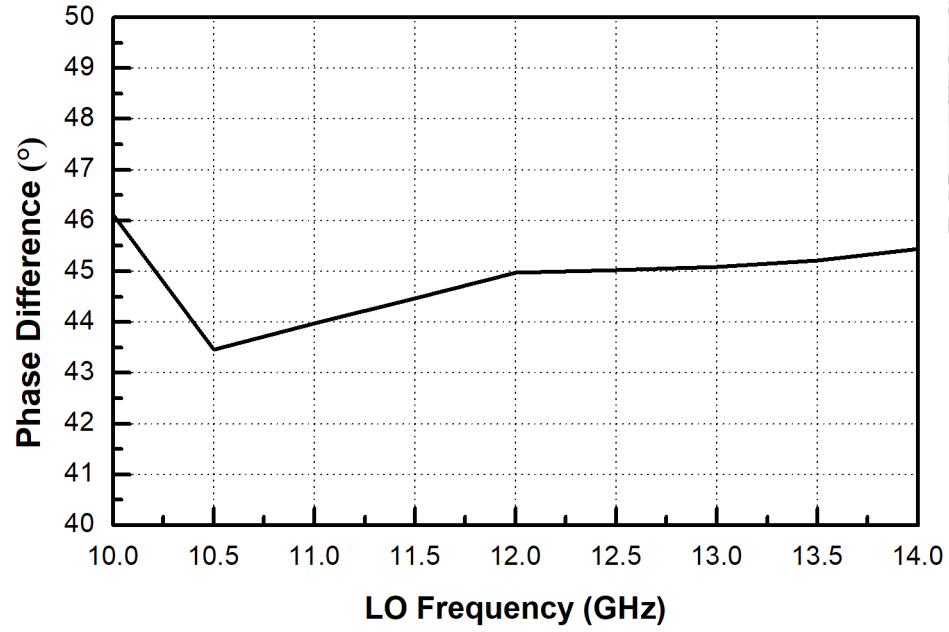


Fig. 4.47 Simulated phase difference between port O_I,Q in Fig. 4.42.

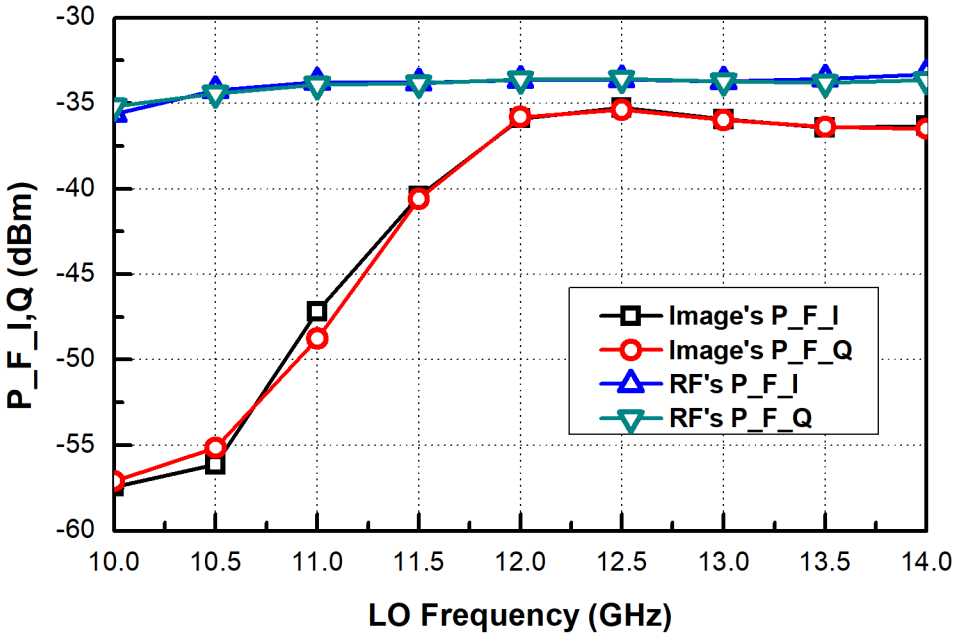


Fig. 4.48 Simulated RF output power (F_I,Q in Fig. 4.42) of the high IRR up-conversion subharmonic mixer at RF/image frequency.

doi:10.6342/NTU202203942

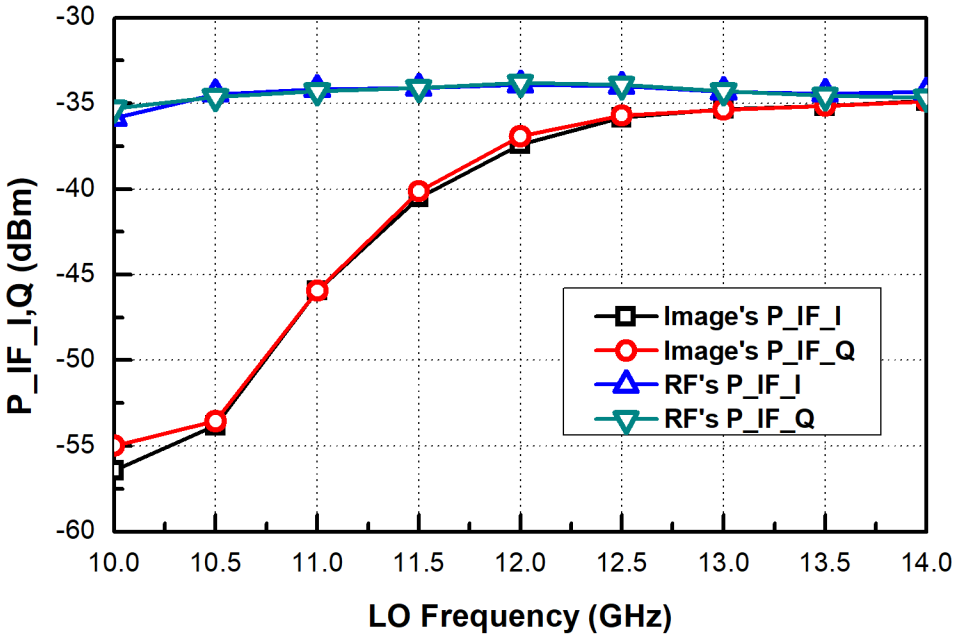


Fig. 4.49 Simulated IF output power (IF_I,Q in Fig. 4.42) of the high IRR down-conversion subharmonic mixer at RF/image frequency.

doi:10.6342/NTU202203942

4.3 Experimental Results

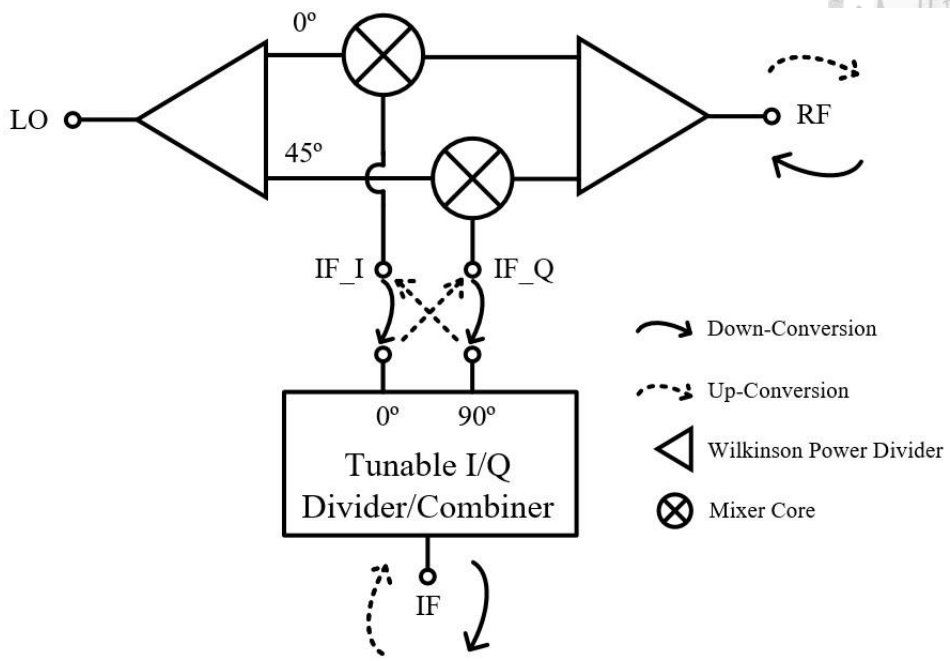


Fig. 4.50 Schematic of the high IRR up-/down-conversion subharmonic mixer when measuring with a 2.5-5 GHz tunable I/Q divider/combiner (sample #3) in Fig. 3.57.

As shown in Fig. 4.50, we perform the measurements with a 2.5-5 GHz tunable I/Q divider/combiner (sample #3) in Fig. 3.57. The chip photo is shown in Fig. 4.51. We use an Agilent E8257D (250 kHz- 67 GHz) signal generator for RF/IF signal, a KEYSIGHT E8267D (250 kHz- 44 GHz) signal generator for LO signal, an Agilent E4448A (3 Hz- 50 GHz) spectrum analyzer to measure large signals (RF/IF output power), a GWINSTEK PST-3202 (32 V,2 A x2/6 V, 5 A x1) power supply and a KEYSIGHT E36311A (6 V, 5 A/±25 V, 1 A) power supply for I/Q divider/combiner's DC supplying. The up-conversion measurement setup is shown in Fig. 4.52. Cable 1 (1.85 mm) connects the probe on the LO side to the signal generator. Cables 2 and 3 (1.85 mm, phase and amplitude are very close) connect the probes on IF_I,Q side to the I/Q divider/combiner's port 2,3 in Fig. 3.57. Cable

doi:10.6342/NTU202203942

4 (1.85 mm) connects the I/Q divider/combiner's port 1 in Fig. 3.57 to the signal generator. Cable 5 (2.4 mm) connects the probe on the RF side to the spectrum analyzer.

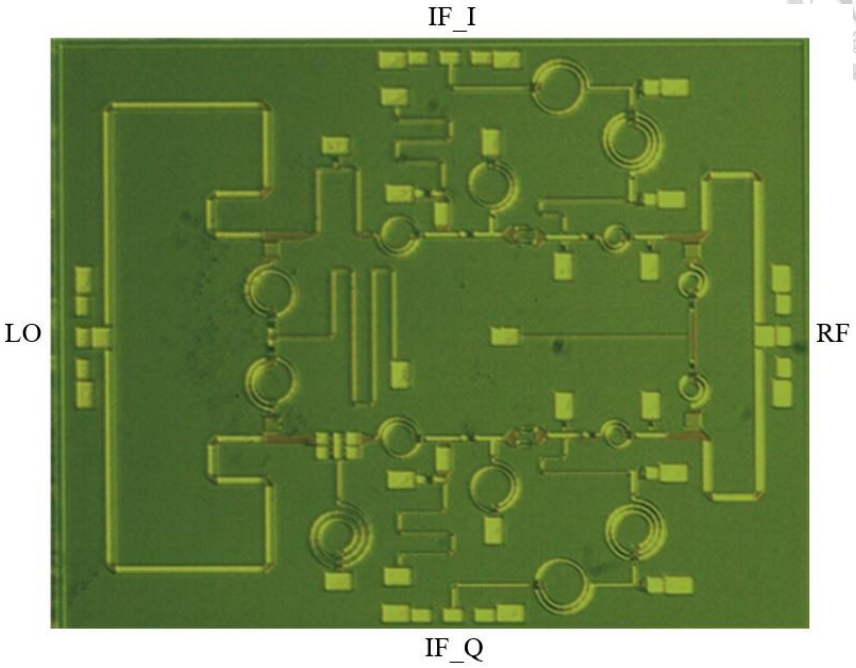


Fig. 4.51 Chip photo of the high IRR up-/down-conversion subharmonic mixer.

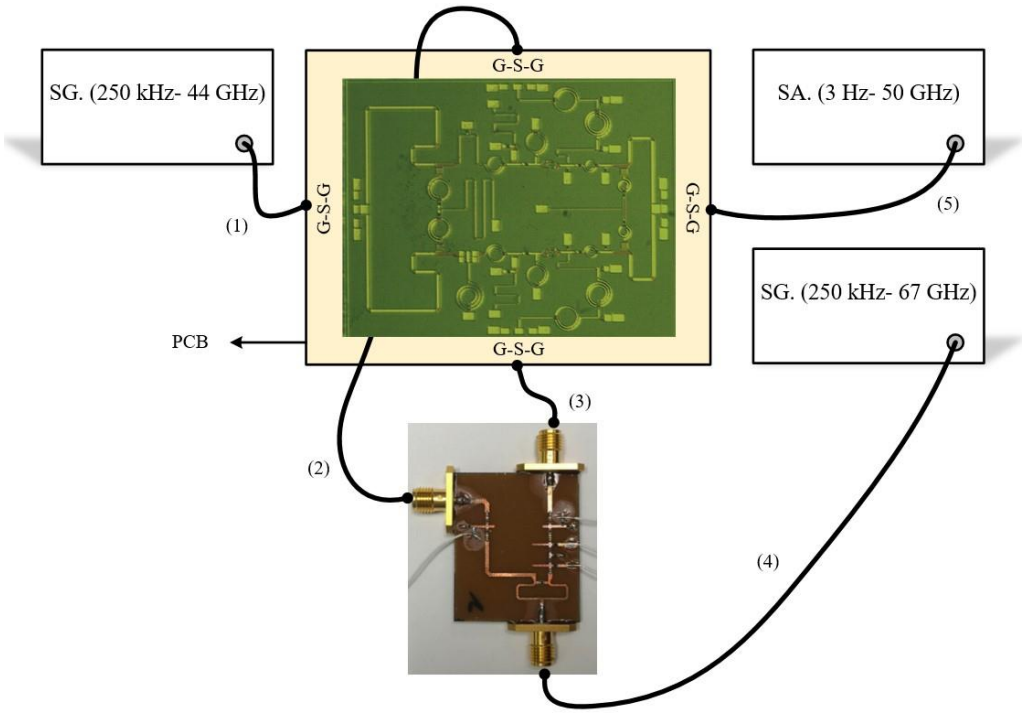


Fig. 4.52 Setup of measurement (up-conversion).

doi:10.6342/NTU202203942

The conversion gain vs. LO power measurement of chip #1,2,3 and EM simulation of the high IRR up-/down-conversion subharmonic mixer as shown in Fig. 4.53 and Fig. 4.54 when RF frequency is 28 GHz, LO frequency is 12 GHz, and IF frequency is 4 GHz. We choose 12 dBm as the LO power for the high IRR up-/down-conversion subharmonic mixer. It has about -11.3 dB conversion gain for up-conversion and -11 dB for down-conversion of three chips.

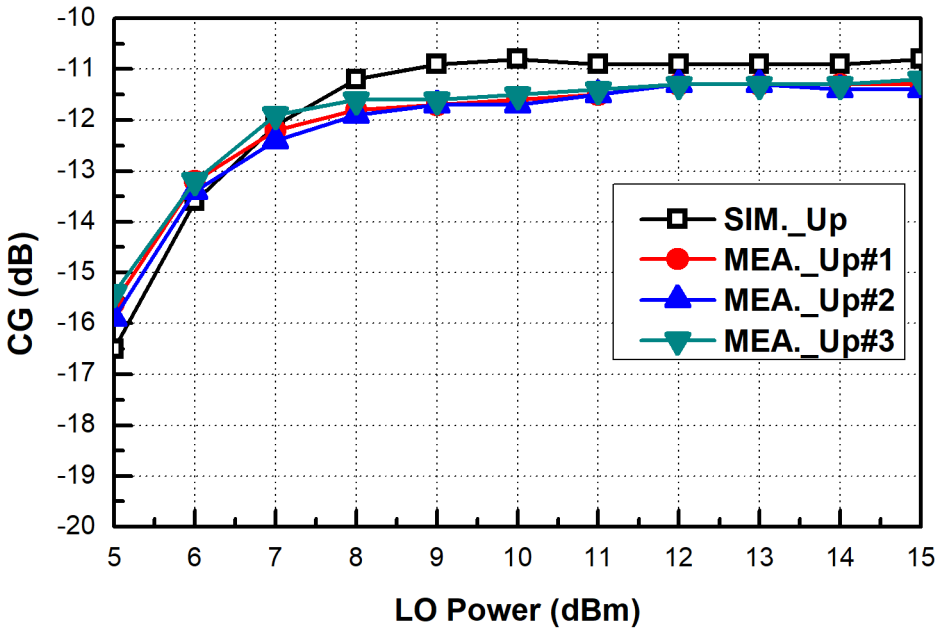


Fig. 4.53 Conversion gain (CG) vs. LO power measurement (#1,2,3) and EM simulation of the high IRR up-conversion subharmonic mixer.

doi:10.6342/NTU202203942

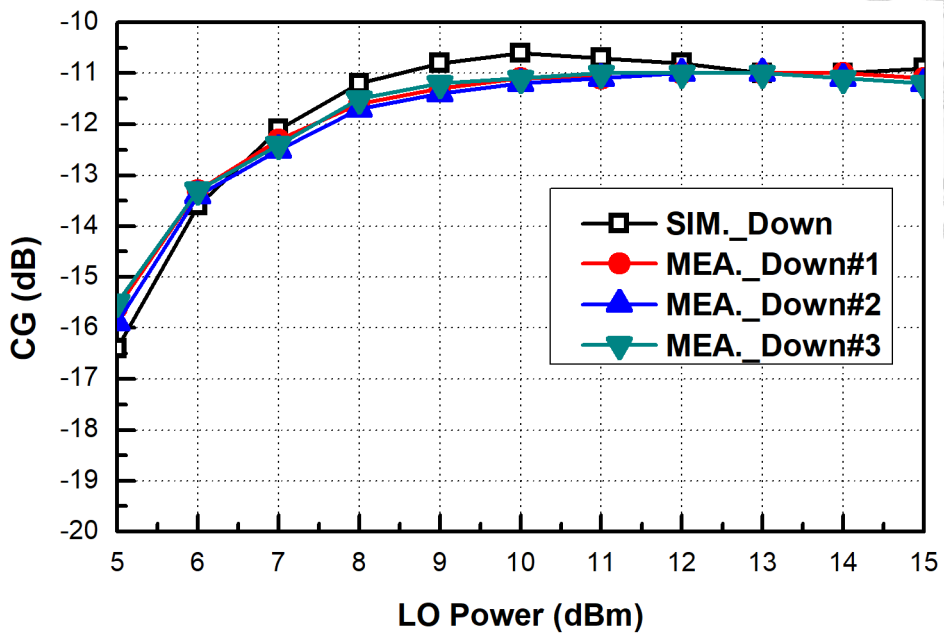


Fig. 4.54 Conversion gain (CG) vs. LO power measurement (#1,2,3) and EM simulation of the high IRR down-conversion subharmonic mixer.

The IP_{1dB} measurement of chip #1,2,3 and EM simulation of the high IRR up-/down-conversion subharmonic mixer as shown in Fig. 4.55 and Fig. 4.56 when RF frequency is 28 GHz, LO frequency is 12 GHz, IF frequency is 4 GHz, and LO power is 12 dBm. It has about 3 dBm for up-conversion and 3.4 dBm for down-conversion of three chips.

doi:10.6342/NTU202203942

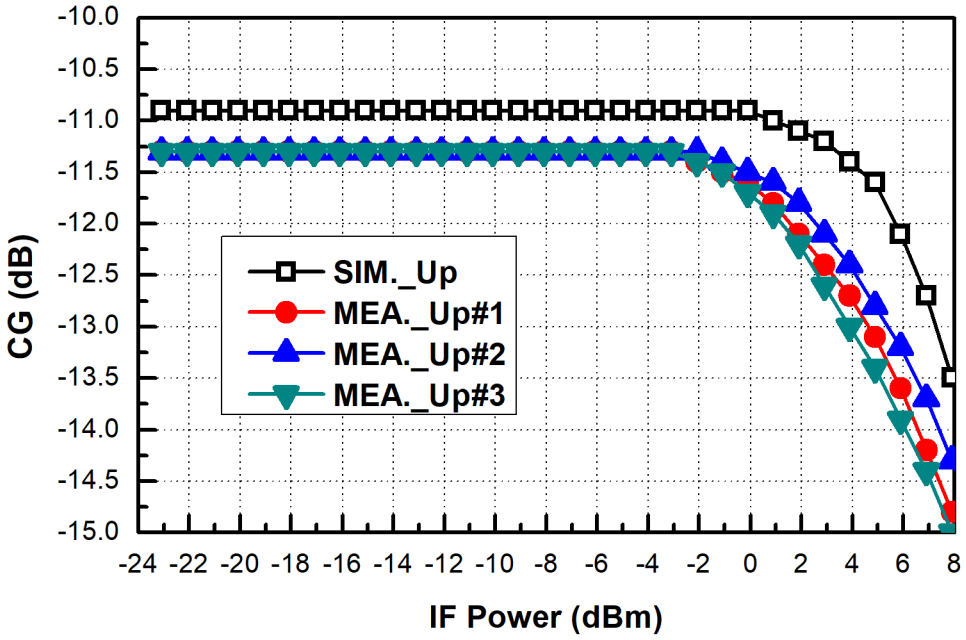


Fig. 4.55 Conversion gain (CG) vs. IF power measurement (#1,2,3) and EM simulation of the high IRR up-conversion subharmonic mixer.

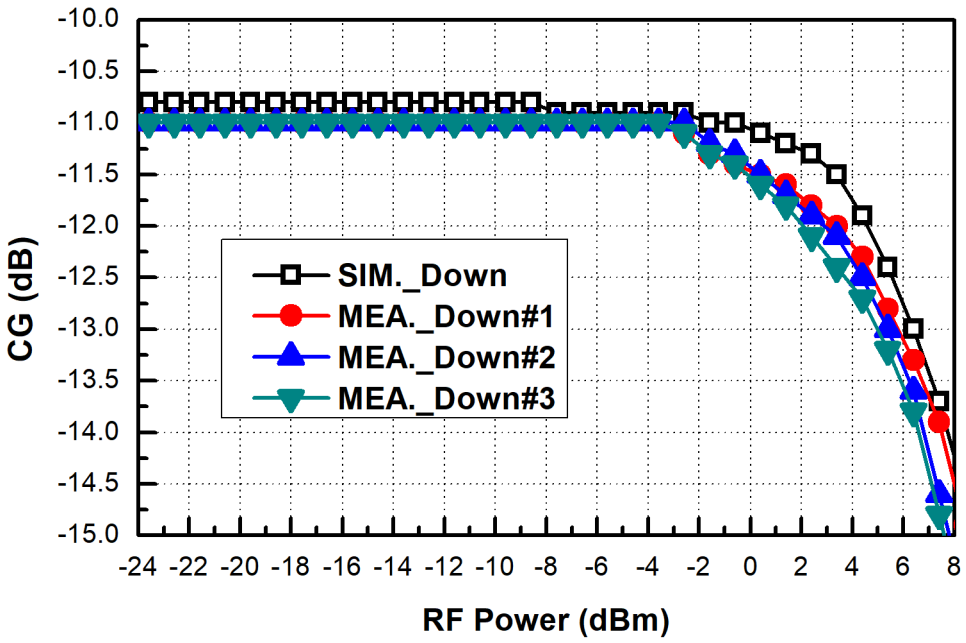


Fig. 4.56 Conversion gain (CG) vs. RF power measurement (#1,2,3) and EM simulation of the high IRR down-conversion subharmonic mixer.

doi:10.6342/NTU202203942

The bandwidth measurement of chip #1,2,3 and EM simulation of the high IRR up-/down-conversion subharmonic mixer as shown in Fig. 4.57 and Fig. 4.58 when RF frequency is 24-32 GHz, IF frequency is 4 GHz, and LO power is 12 dBm. The conversion gain range of up-conversion is 1.3 dB and the conversion gain range of down-conversion is 1.7 dB from 10-14 GHz of three chips.

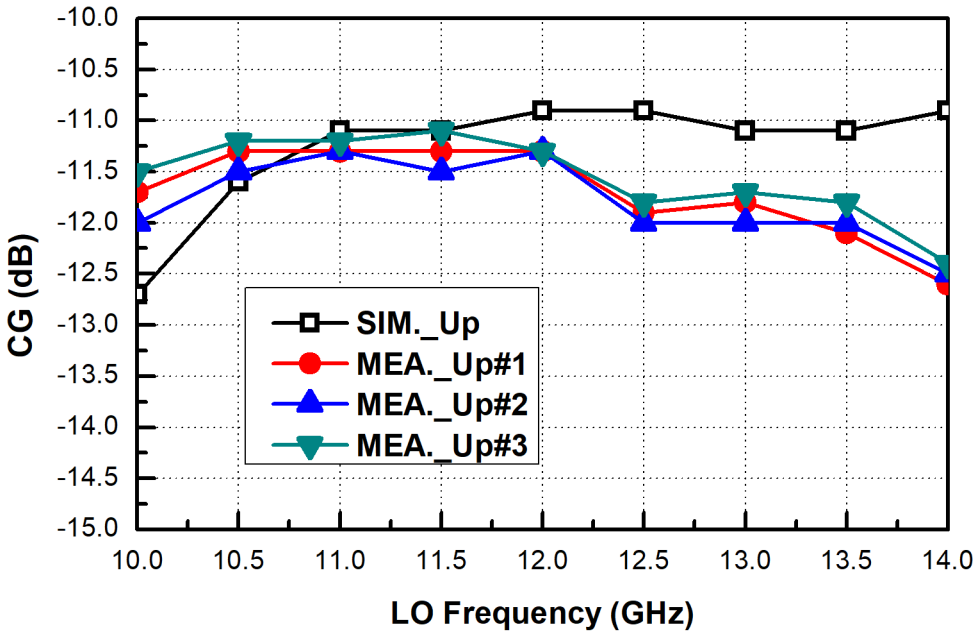


Fig. 4.57 Conversion gain (CG) vs. bandwidth measurement (#1,2,3) and EM simulation of the high IRR up-conversion subharmonic mixer.

doi:10.6342/NTU202203942

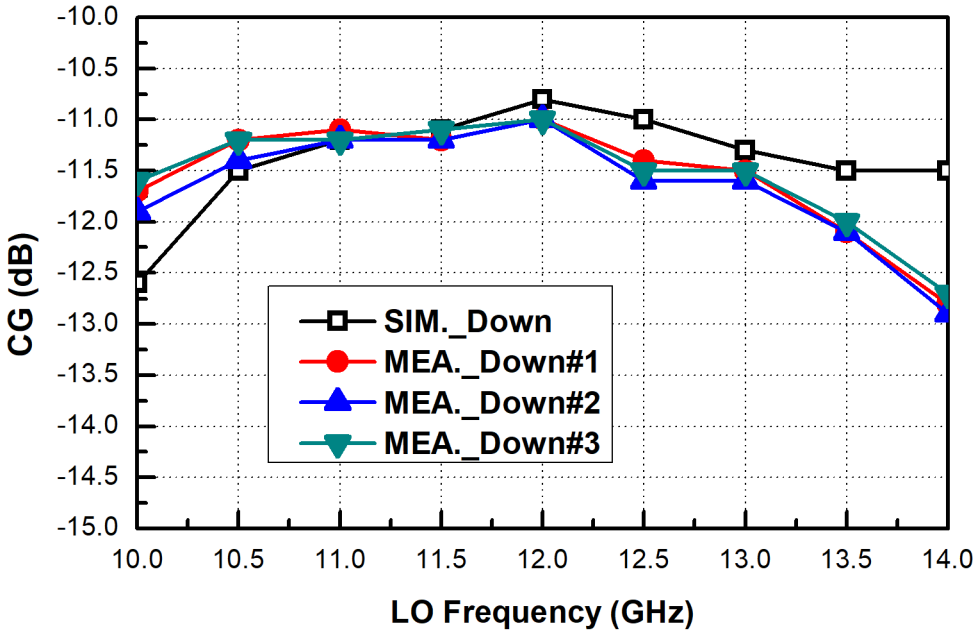


Fig. 4.58 Conversion gain (CG) vs. bandwidth measurement (#1,2,3) and EM simulation of the high IRR down-conversion subharmonic mixer.

The isolation measurement of chip #1,2,3 and EM simulation of the high IRR up-/down-conversion subharmonic mixer as shown in Fig. 4.59- Fig. 4.64 when RF frequency is 24-32 GHz, IF frequency is 4 GHz, and LO power is 12 dBm. The LO-to-RF isolation of up-/down-conversion is less than -25.9 dB from 10-14 GHz of three chips as shown in Fig. 4.59 and Fig. 4.60. The 2LO-to-RF isolation of up-/down-conversion is less than -59.6 dB from 10-14 GHz of three chips as shown in Fig. 4.61 and Fig. 4.62. The LO-to-IF isolation of up-/down-conversion is less than -38.4 dB from 10-14 GHz of three chips as shown in Fig. 4.63 and Fig. 4.64.

doi:10.6342/NTU202203942

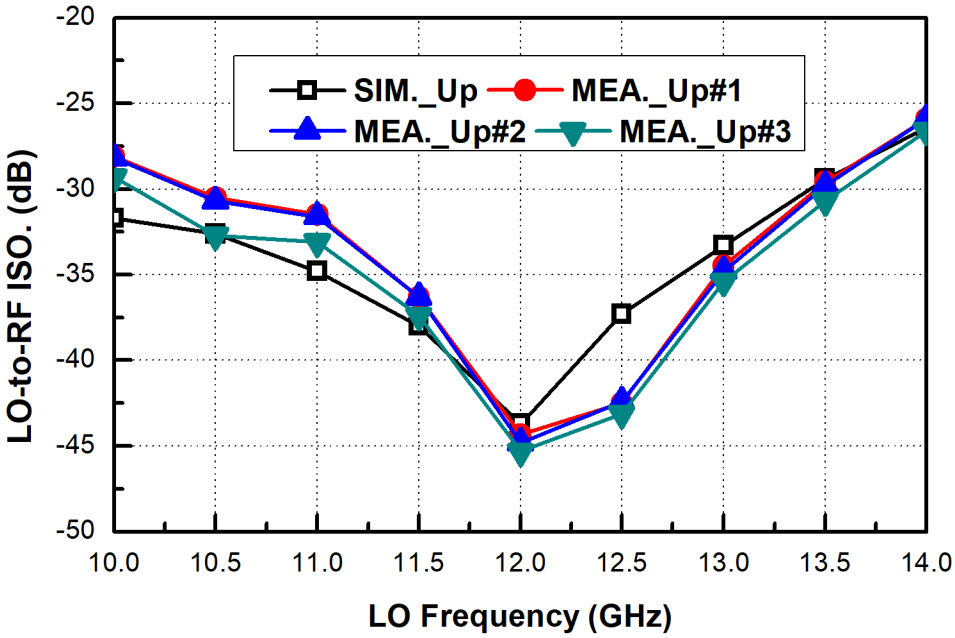


Fig. 4.59 LO-to-RF isolation measurement (#1,2,3) and EM simulation of the high IRR up-conversion subharmonic mixer.

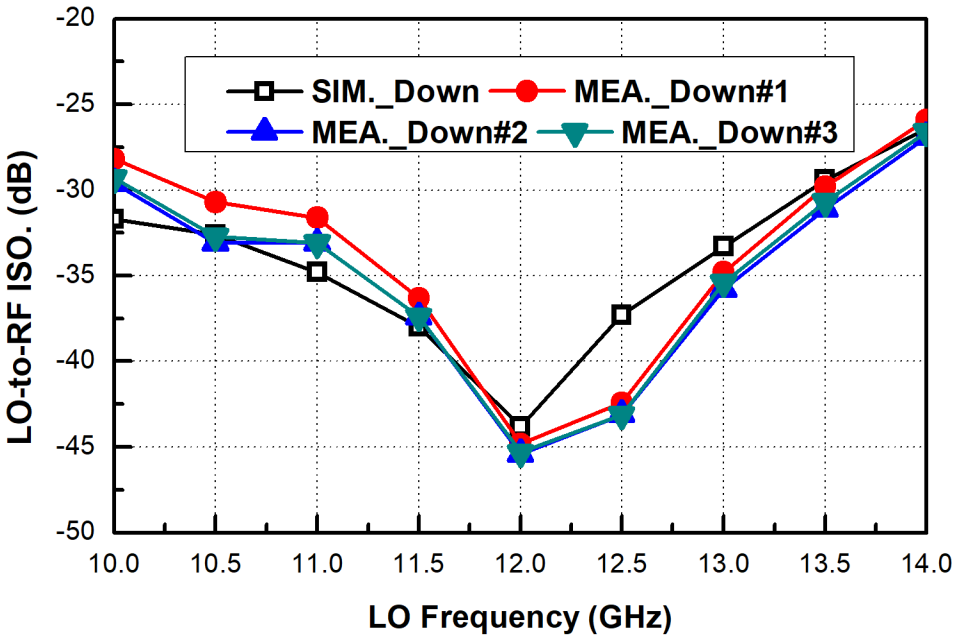


Fig. 4.60 LO-to-RF isolation measurement (#1,2,3) and EM simulation of the high IRR down-conversion subharmonic mixer.

doi:10.6342/NTU202203942

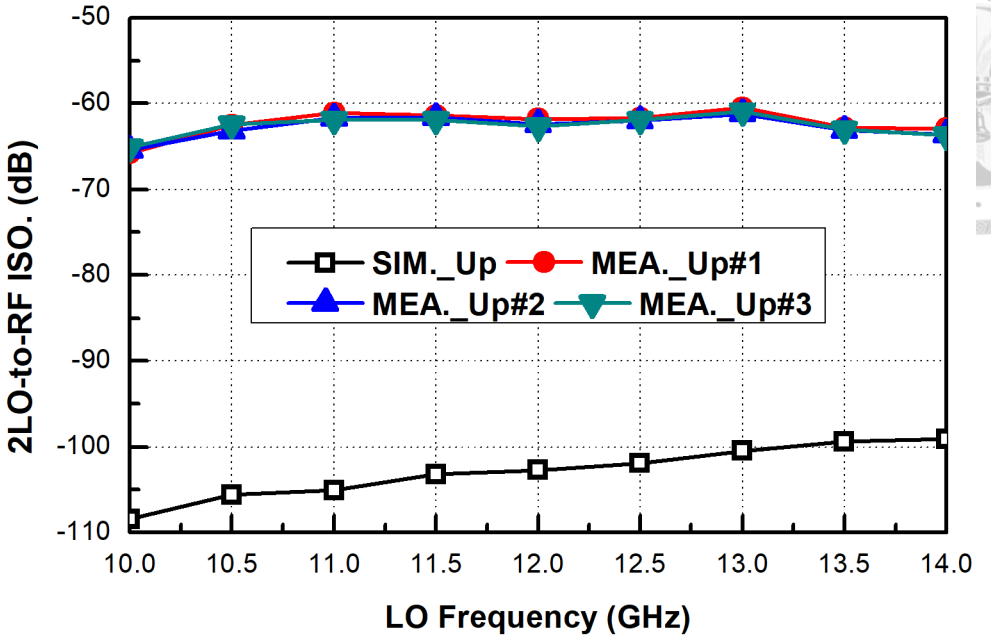


Fig. 4.61 2LO-to-RF isolation measurement (#1,2,3) and EM simulation of the high IRR up-conversion subharmonic mixer.

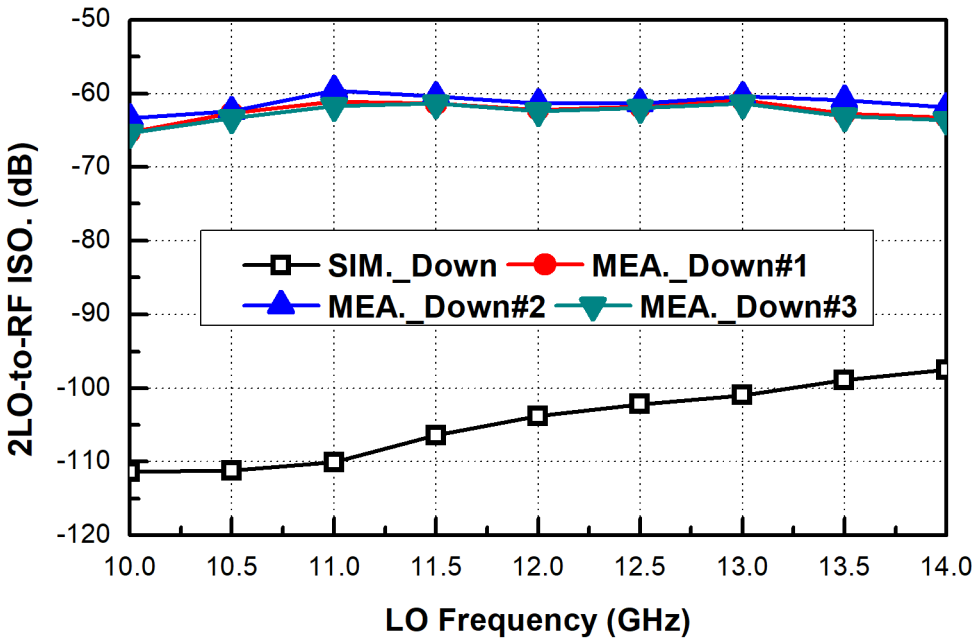


Fig. 4.62 2LO-to-RF isolation measurement (#1,2,3) and EM simulation of the high IRR down-conversion subharmonic mixer.

doi:10.6342/NTU202203942

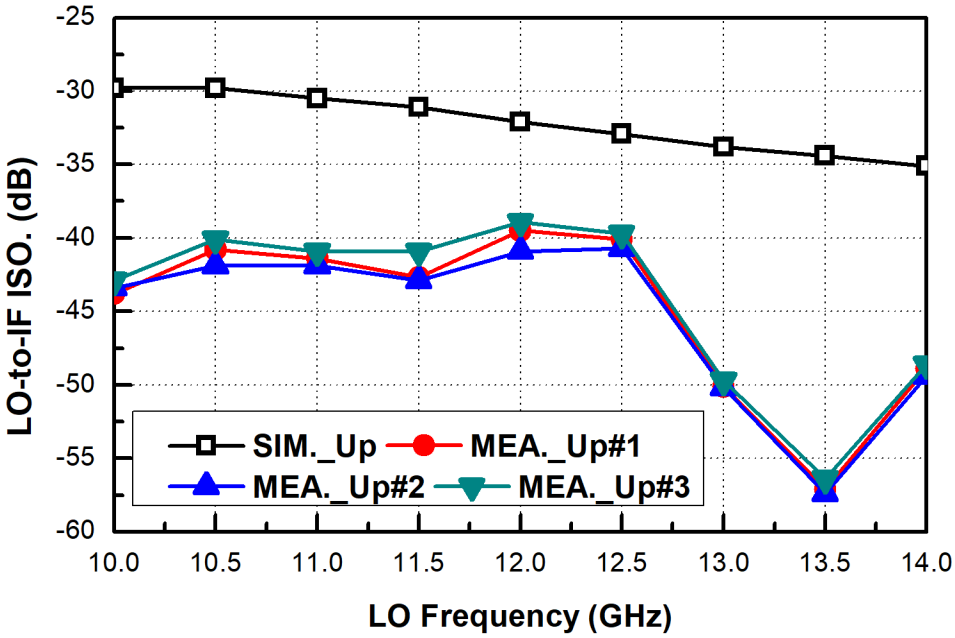


Fig. 4.63 LO-to-IF isolation measurement (#1,2,3) and EM simulation of the high IRR up-conversion subharmonic mixer.

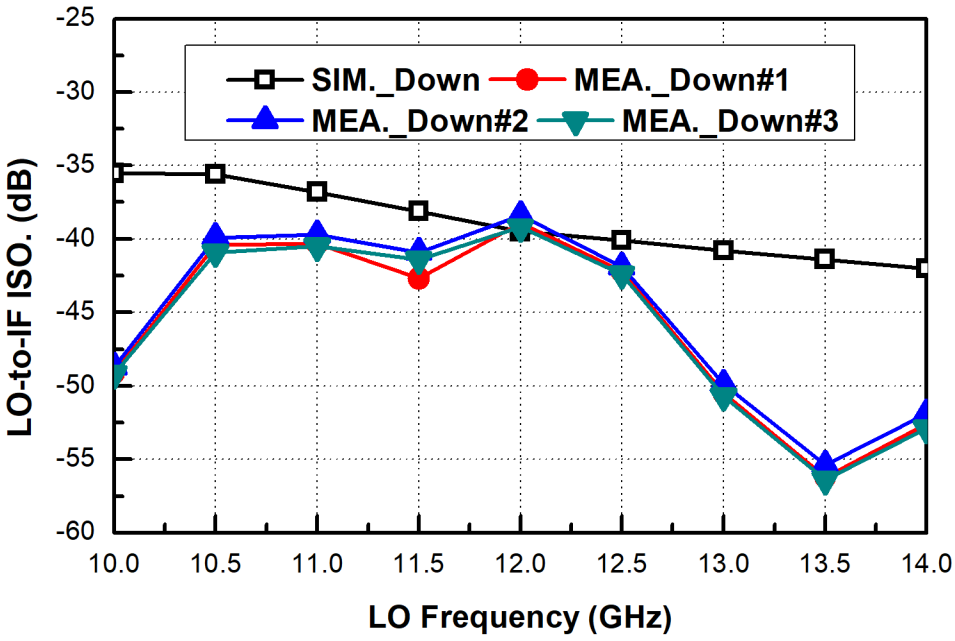


Fig. 4.64 LO-to-IF isolation measurement (#1,2,3) and EM simulation of the high IRR down-conversion subharmonic mixer.

doi:10.6342/NTU202203942

The IRR measurement of chip #1,2,3 and EM simulation of the high IRR up-/down-conversion subharmonic mixer with phase/amplitude tuning to obtain the maximum IRR as shown in Fig. 4.65 and Fig. 4.66 when RF frequency is 24-32 GHz, IF frequency is 4 GHz, and LO power is 12 dBm. The IRR of up-conversion is greater than 45.7 dB and the IRR of down-conversion is greater than 46.7 dB from 10-14 GHz of three chips. The detailed control voltages are shown in Table 4.8.

Table 4.8 V_{Phase}, $V_{AmpL,}$ and V_{AmpR} (sample #3 in Fig. 3.57) when obtaining the maximum IRR of chip #1.

Up_Freq. (GHz)	V_{Phase} (V)	V_{AmpL} (V)	V_{AmpR} (V)
10	3	0.85	0.96
10.5	5.5	0.9	0.9
11	3.5	0.9	0.9
11.5	3.6	0.94	0.9
12	2.5	0.9	0.95
12.5	1.2	0.85	0.965
13	1.8	0.7	1
13.5	2.5	0.9	0.98
14	2.6	0.9	0.93
Down_Freq. (GHz)	V_{Phase} (V)	V_{AmpL} (V)	V_{AmpR} (V)
10	5.5	1	0.9
10.5	5.6	0.9	0.98

doi:10.6342/NTU202203942

11	4	0.8	0.8
11.5	4.4	0.9	0.8
12	3.8	1	0.8
12.5	2.3	0.8	0.9
13	3.8	0.9	0.97
13.5	4.1	0.95	0.9
14	4.1	0.9	0.94

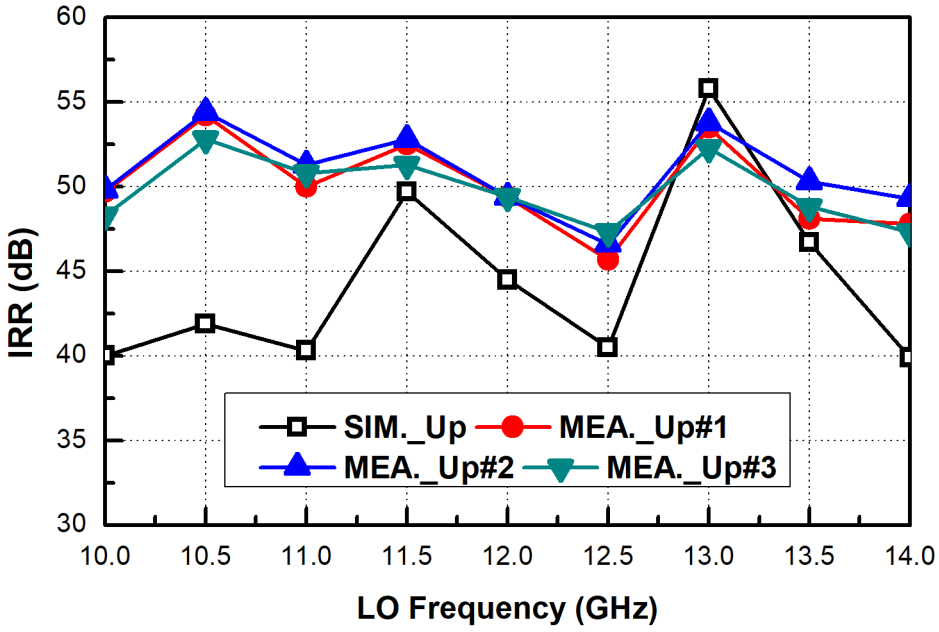


Fig. 4.65 IRR measurement (#1,2,3) and EM simulation of the high IRR up-conversion subharmonic mixer (with phase/amplitude tuning for maximum IRR).

doi:10.6342/NTU202203942

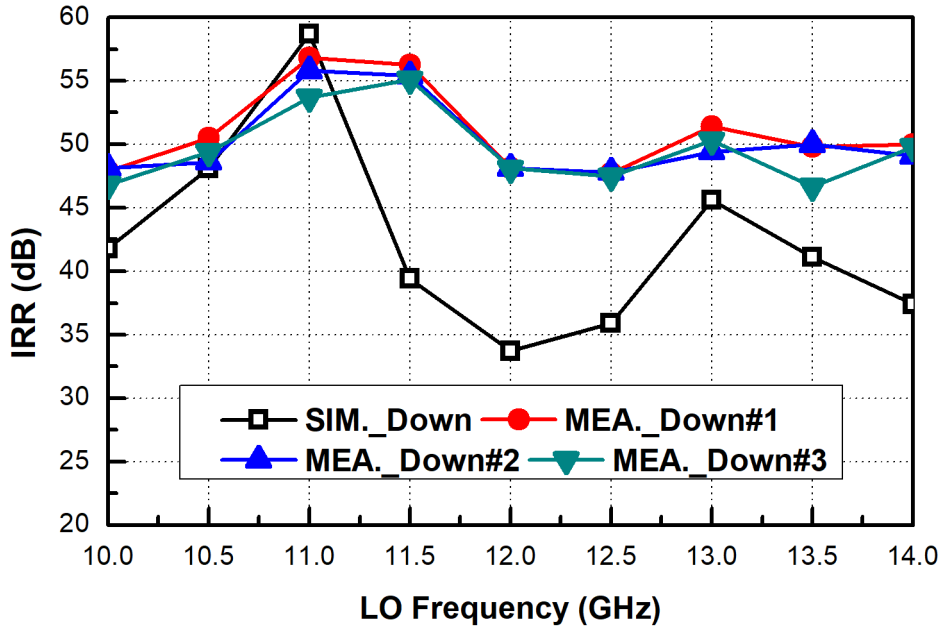


Fig. 4.66 IRR measurement (#1,2,3) and EM simulation of the high IRR down-conversion subharmonic mixer (with phase/amplitude tuning for maximum IRR).

The IRR measurement of chip #1,2,3 and EM simulation of the high IRR up-/down-conversion subharmonic mixer with phase/amplitude tuning only at 12 GHz as shown in Fig. 4.67 and Fig. 4.68 when RF frequency is 24-32 GHz, IF frequency is 4 GHz, and LO power is 12 dBm. Except at 12.5 and 13 GHz, it can reach an IRR of 35 dB for up-conversion of three chips; except at 12.5-14 GHz, it can reach an IRR of 35 dB for down-conversion of three chips.

doi:10.6342/NTU202203942

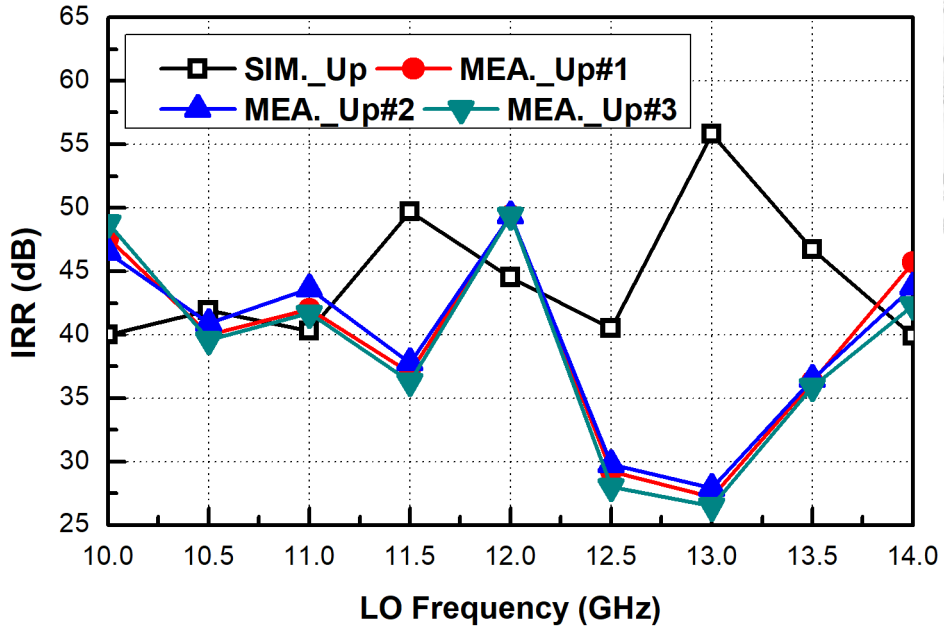


Fig. 4.67 IRR measurement (#1,2,3) and EM simulation of the high IRR up-conversion subharmonic mixer (with phase/amplitude tuning only at 12 GHz).

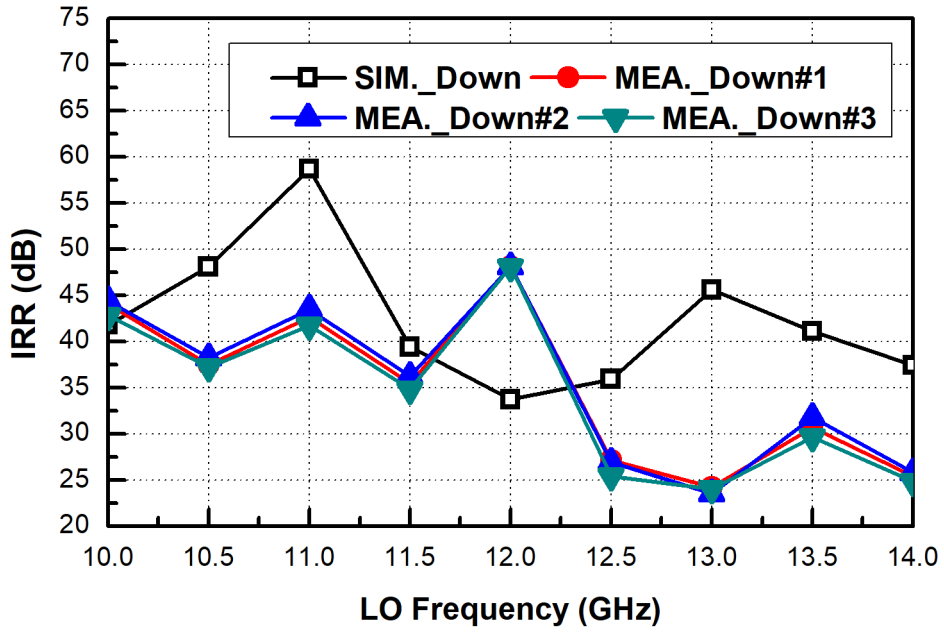


Fig. 4.68 IRR measurement (#1,2,3) and EM simulation of the high IRR down-conversion subharmonic mixer (with phase/amplitude tuning only at 12 GHz).

doi:10.6342/NTU202203942

The measured IRR of the high IRR up-/down-conversion subharmonic mixer (chip #1) with phase/amplitude tuning to obtain the proper IRR as shown in Fig. 4.69 and Fig. 4.70 when RF frequency is 23.6-32.4 GHz, IF frequency is 3.6-4.4 GHz, and LO power is 12 dBm. It can reach an IRR of 25 dB for up-conversion and an IRR of 30 dB for down-conversion from 10 to 14 GHz in 800 MHz IF bandwidth. The detailed control voltages are shown in Table 4.9.

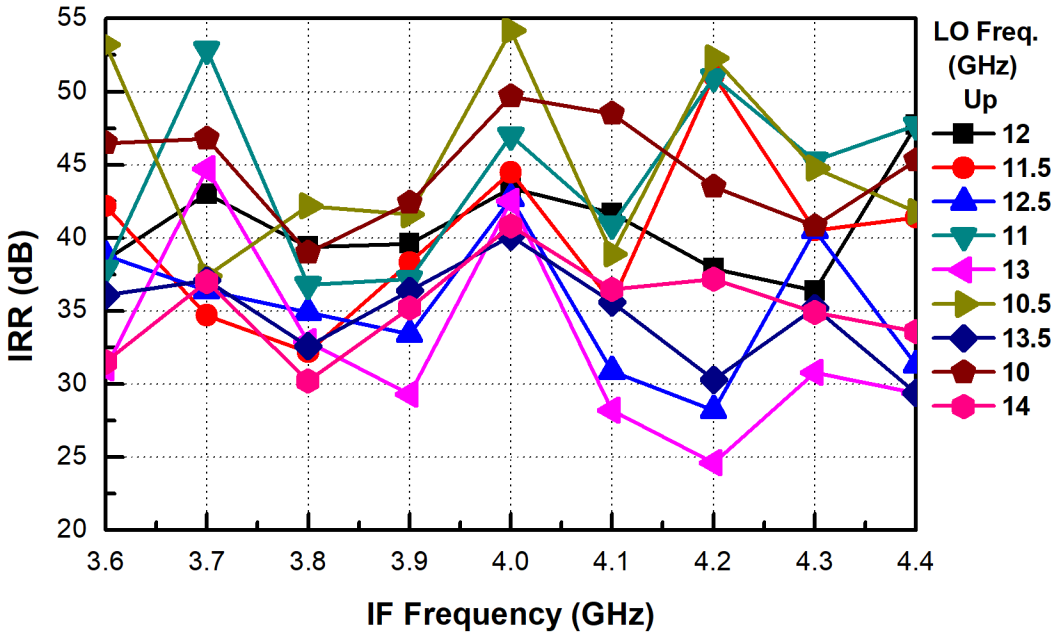


Fig. 4.69 Measured IRR of the high IRR up-conversion subharmonic mixer (chip #1) (with phase/amplitude tuning for proper IRR).

doi:10.6342/NTU202203942

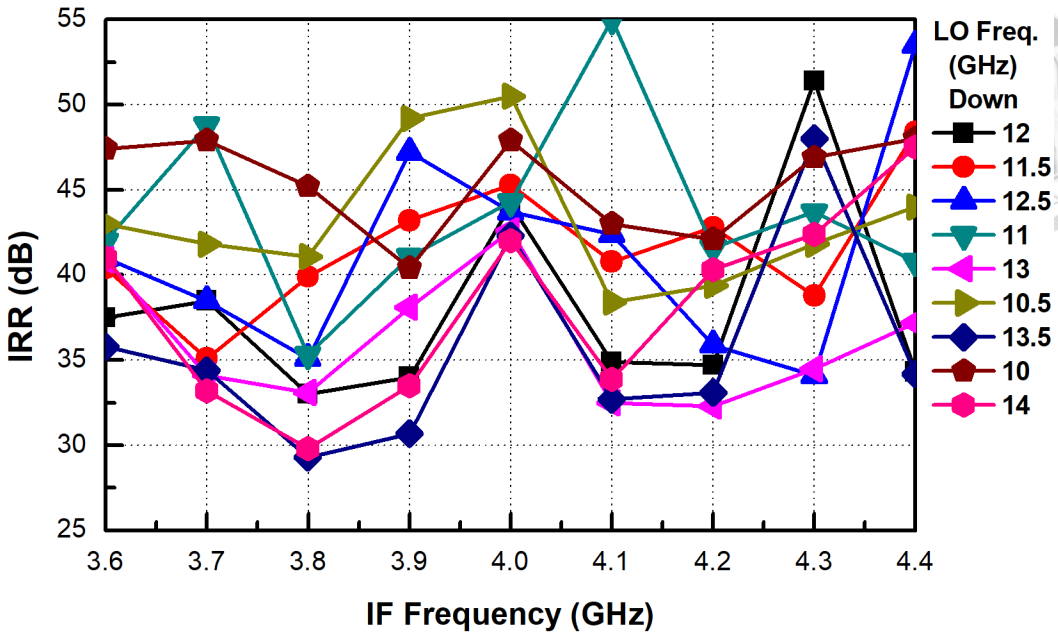


Fig. 4.70 Measured IRR of the high IRR down-conversion subharmonic mixer (chip #1) (with phase/amplitude tuning for proper IRR).

Table 4.9 V_{Phase}, V_{AmpL}, and V_{AmpR} (sample #3 in Fig. 3.57) when obtaining the proper IRR of chip #1.

Up_Freq. (GHz)	V_{Phase} (V)	V_{AmpL} (V)	V_{AmpR} (V)
10	3	0.85	0.96
10.5	5.5	0.9	0.9
11	4	0.9	0.9
11.5	4.2	0.94	0.9
12	2.8	0.9	0.95
12.5	1.3	0.85	0.965
13	2	0.7	1
13.5	2.7	0.93	0.98

doi:10.6342/NTU202203942

14	2.85	0.9	0.93
Down_Freq. (GHz)	V_{Phase} (V)	V_{AmpL} (V)	V_{AmpR} (V)
10	5.5	1	0.9
10.5	5.6	0.9	0.98
11	5	0.8	0.8
11.5	4.4	0.8	0.9
12	3.8	0.98	0.8
12.5	2.3	0.8	0.93
13	3.8	0.82	0.975
13.5	4.1	0.935	0.9
14	4.1	0.9	0.955

doi:10.6342/NTU202203942

4.4 Summary

In this chapter, a 24-32 GHz high image rejection ratio up-/down-conversion subharmonic mixer is presented. With the analysis and implementation of the 45° LO power divider and in-phase RF divider/combiner, small phase and amplitude imbalances with good isolation can be obtained. By employing a subharmonic mixer core constructed by an anti-parallel diode pair, we only need a 12 dBm LO signal from 10-14 GHz with 0 DC consumption.

To achieve a high IRR, we need small phase and amplitude imbalances of the quadrature signal (0°/45°), a good inter-stage reflection coefficient near the quadrature signal (0°/45°) generator side (LO), and a tunable I/Q divider/combiner with good isolation and reflection coefficient. As shown in Fig. 4.12- Fig. 4.15, the isolation of the 45° LO power divider is less than -18.3 dB and there is a 2.3-(-1.7)° phase imbalance and a (-0.11)-0.04 dB amplitude imbalance from 10 to 14 GHz. As shown in Fig. 4.34, the reflection coefficient is less than -11.8 dB from 10.5-14 GHz and is -8.3 dB at 10 GHz. According to [39], the nonzero phase and/or amplitude imbalances may partly be compensated by the phase and/or amplitude mismatches caused by the LO reflections. There is a (-0.5)-0.4° phase imbalance that can be obtained after optimizing the LO inter-stage matching network at 11.5-14 GHz as shown in Fig. 4.47. Without RF/IF signal combining, the image signal has less power on port F_I,Q/IF_I,Q in Fig. 4.42 than the RF signal, especially at 10-11.5 GHz as shown in Fig. 4.48/Fig. 4.49, respectively. This compensates for the larger phase imbalance between port O_I,Q at 10-11.5 GHz. Based on Fig. 4.47- Fig. 4.49, we can conclude that the IRR performance is great.

doi:10.6342/NTU202203942

With the 2.5-5 GHz tunable I/Q divider/combiner (sample #3), we can perform the IRR measurements as shown in Fig. 4.65- Fig. 4.70. The maximum IRR of up-conversion is greater than 45.7 dB and the maximum IRR of down-conversion is greater than 46.7 dB from 10-14 GHz of three chips. With phase/amplitude tuning only at 12 GHz, except at 12.5 and 13 GHz, it can reach an IRR of 35 dB for up-conversion of three chips; except at 12.5-14 GHz, it can reach an IRR of 35 dB for down-conversion of three chips. In the practical application for 5G communication, the operating data of the IF frequency of 800 MHz bandwidth should be considered. It can reach an IRR of 25 dB for up-conversion and an IRR of 30 dB for down-conversion from 10 to 14 GHz in 800 MHz IF bandwidth of Chip #1.

Table 4.10- Table 4.11 summarize the performance of I/Q mixers in GaAs pHEMT, CMOS, and SiGe in recent years. Compared to these I/Q mixers, the proposed high IRR up-/down-conversion subharmonic mixer shows an 8 GHz bandwidth with a center frequency of 28 GHz. Under this bandwidth, there is a 1.3 dB conversion gain range for up-conversion with a -11.3 dB conversion gain at 28 GHz and a 1.7 dB conversion gain range for down-conversion with a -11 dB conversion gain at 28 GHz. It shows a good conversion gain performance in passive mixers and the best IP_{1dB} in all the published I/Q mixers. Since the LO/2LO frequency approaches the RF frequency more closely than the image frequency, LO/2LO leakage is an important consideration. This work shows excellent 2LO-to-RF isolation greater than 59.6 dB. With the tunable I/Q divider/combiner, this work shows the high IRR level in all the published I/Q mixers. Even though the area of this work is relatively large and the bandwidth is only 8 GHz, it exhibits an outstanding comprehensive performance among conversion gain, IP_{1dB}, 2LO-to-RF isolation, and IRR for the image rejection mixer in 5G communication.

doi:10.6342/NTU202203942

Table 4.10 Comparison of the published I/Q mixers (part I).

Ref.	Tech.	Function of I/Q	RF Freq. (GHz)	LO Power (dBm)	CG. (dB)
This Work	0.15 μm GaAs pHEMT	45° PD	24-32	12	-11.3 (Up) -11 (Down)
MWCL' 22 [41]	55 nm CMOS	2-Stage PPF	20-42	12	1.2±1.5
JSSC' 22 [35]	28 nm CMOS	2-Stage Coupler	22-31	N/A	2-22 (Up) 5-29 (Down)
JSSC' 20 [34]	45 nm CMOS SOI	2-Stage Transformer	24.5-43.5	N/A	35.2
APMC' 19 [33]	180 nm CMOS	45° PD	22-40	6	-22
JSSC' 18 [32]	55 nm CMOS	1-Stage PPF	28-44	0	N/A
IMS' 18 [31]	0.12 μm SiGe	2-Stage PPF	35-105	N/A	21-33
ICMMT' 10 [42]	0.5 μm GaAs pHEMT	90° Coupler	24	14.75	-16.25
APMC' 10 [43]	0.15 μm GaAs pHEMT	4-Stage PPF	17	6.7	5.5

doi:10.6342/NTU202203942

APMC' 08 [44]	0.15 μm GaAs pHEMT	90° Coupler	24	14.4	-13

PD: power divider; PPF: poly-phase filter.

Table 4.11 Comparison of the published I/Q mixers (part II).

Ref.	IP_{1dB} (dBm)	ISO. (dB)	IRR. (dB)	P_{DC} (mW)	Size
This Work	3 (Up) 3.4 (Down)	> 25.9 (LO-to-RF) > 59.6 (2LO-to-RF) > 38.4 (LO-to-IF)	> 45.7 (Up) * > 46.7 (Down) *	0	2267.5*1810 (μm*μm)
MWCL' 22 [41]	-2.77	> 35 (LO-to-RF)	< 30	24	0.58 (mm^2)
JSSC' 22 [35]	-9.5 (Up) N/A (Down)	N/A	40 (Up) 30 (Down)	220 (Up) 110 (Down)	N/A
JSSC' 20 [34]	(-7)-(-25.5)	N/A	32-56	60	0.52 (mm^2)
APMC' 19 [33]	-18	N/A	30-40 *	38.4	1.21 (mm^2)
JSSC' 18	N/A	23 (LO Leakage)	> 40 **	39	590*330

doi:10.6342/NTU202203942

[32]					(μm*μm)
IMS' 18 [31]	-21.5	N/A	> 40 **	598.5	2.35*1.3 (mm*mm)
ICMMT' 10 [42]	N/A	N/A	20.4	0	1 (mm^2)
APMC' 10 [43]	0	N/A	30	214.5	2.3*1.6 (mm*mm)
APMC' 08 [44]	N/A	> 10 (LO-to-RF) > 70 (2LO-to-RF) > 15 (IF-to-RF)	19	0	1.5 (mm^2)

*: off-chip I/Q calibration.

**: on-chip I/Q calibration.

doi:10.6342/NTU202203942

Chapter 5 Conclusion

This thesis presents a 24 GHz high conversion gain and low noise down-conversion active mixer, a millimeter-wave up-/down-conversion image rejection module, and a 24-32 GHz high image rejection ratio up-/down-conversion subharmonic mixer.

The first work is a 24 GHz high conversion gain and low noise down-conversion active mixer in 0.18 μm CMOS process. In order to effectively improve the performance of noise and conversion gain, the concepts of the current-bleeding technique and the resonant inductor are utilized in this design. However, after two tape-outs, the reason for the severe reduction in conversion gain has not been found so far.

The second work is a millimeter-wave up-/down-conversion image rejection module. By replacing the capacitors on the left-handed transmission line with the varactors and employing the PIN diodes on the T-type attenuators. The tunable I/Q divider/combiner achieves an 80-100° and a (+2)-(-1.1) dB phase and amplitude tuning ranges at 2.5-5 GHz, respectively. According to the experimental results, the image rejection module has excellent IRR performance at 3-4.5 GHz, and the 800 MHz at 3-4.5 GHz also has good IRR performance.

The last work is a 24-32 GHz high image rejection ratio up-/down-conversion subharmonic mixer in 0.15 μm GaAs pHEMT process. By utilizing the modified Wilkinson power divider, the 45° LO power divider with small phase and amplitude imbalances reaches a great isolation performance. The quasi-lumped $\lambda_{LO}/4$ short/open stubs of the subharmonic mixer core have good isolation of 2LO-to-RF, LO-to-RF, and LO-to-IF. Besides, the analysis of the LO inter-stage reflection coefficient is adopted in designing the matching network to optimize IRR. The proposed I/Q mixer exhibits outstanding IRR performance over a wide

doi:10.6342/NTU202203942

bandwidth with the tunable I/Q divider/combiner in measurement. The conversion gain, IP_{1dB}, and port-to-port isolations also have good performance from the measured results.

In author's opinion, there are four crucial factors to achieving a high IRR. The first is the small phase and amplitude imbalances of the quadrature (or 0°/45°) signal. The second is the good isolation between the quadrature (or 0°/45°) signals. The third is about the LO inter-stage reflection coefficient. A good reflection coefficient directly influences IRR performance, and a poor reflection coefficient may compensate for the impact on IRR caused by non-zero phase and/or amplitude imbalances. The last one is the reflection coefficient and isolation of the I/Q divider/combiner. A poor reflection coefficient and/or weak isolation leads to a bad tuning ability.

doi:10.6342/NTU202203942

REFERENCE

[1] D. -R. Lin, K. -Y. Kao and K. -Y. Lin, "A K-band high-gain linear CMOS mixer with current-bleeding neutralization technique," *2018 Asia-Pacific Microwave Conference (APMC)*, 2018, pp. 267-269.

[2] Y. -T. Chang, H. -Y. Wu and H. -C. Lu, "A K-band high-gain down-converter mixer using cross couple pair active load," *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, 2016, pp. 377-380.

[3] X. Yi *et al*., "A 24/77 GHz dual-band receiver for automotive radar applications," in *IEEE Access*, vol. 7, pp. 48053-48059, 2019.

[4] Z. Liu *et al*., "A 24 GHz CMOS mixer using symmetrical design methodology with I/Q imbalance calibration," *2017 IEEE Asia Pacific Microwave Conference (APMC)*, 2017, pp. 903-905.

[5] G. Pyo, C. -Y. Kim and S. Hong, "Single-antenna FMCW radar CMOS transceiver IC," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 3, pp. 945-954, March 2017.

[6] S. Wang and P. -H. Chen, "An active Marchand balun and its application to a 24-GHz CMOS mixer," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 6, no. 10, pp. 1535-1541, Oct. 2016.

[7] W. Cheng, A. J. Annema, G. J. M. Wienk and B. Nauta, "A flicker noise/IM3 cancellation technique for active mixer using negative impedance," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2390-2402, Oct. 2013.

doi:10.6342/NTU202203942

[8] S. Kong, C. -Y. Kim and S. Hong, "A K-band UWB low-noise CMOS mixer with bleeding path G_m-boosting technique," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 3, pp. 117-121, March 2013.

[9] B. Bae and J. Han, "24–40 GHz gain-boosted wideband CMOS down-conversion mixer employing body-effect control for 5G NR applications," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 3, pp. 1034-1038, March 2022.

[10] J. Yoon *et al.*, "A new RF CMOS Gilbert mixer with improved noise figure and linearity," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 3, pp. 626-631, March 2008.

[11] H. Darabi and J. Chiu, "A noise cancellation technique in active RF-CMOS mixers," in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2628-2632, Dec. 2005.

[12] Analog Devices, Inc., "22 GHz to 32 GHz, GaAs, MMIC, I/Q Mixer," HMC524ALC3B datasheet, 2018.

[13] Analog Devices, Inc., "SMT GaAs MMIC x2 Active Frequency Multiplier, 25-31 GHz Output," HMC942LP4E datasheet.

[14] Analog Devices, Inc., "Fractional-N PLL with Integrated VCO, 12.4-13.4 GHz," HMC807LP6CE datasheet.

[15] David M. Pozar, Microwave Engineering, Fourth Edition, John Wiley & Sons, Inc., 2012.

[16] C. Tseng and C. Chang, "A broadband quadrature power splitter using metamaterial transmission line," in *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 1, pp. 25-27, Jan. 2008.

doi:10.6342/NTU202203942

[17] Young-Hoon Chun and Jia-Sheng Hong, "Compact wide-band branch-line hybrids," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 2, pp. 704-709, Feb. 2006.

[18] S. Jung, R. Negra and F. M. Ghannouchi, "A miniaturized double-stage 3dB broadband branch-line hybrid coupler using distributed capacitors," *2009 Asia Pacific Microwave Conference*, 2009, pp. 1323-1326.

[19] K. Nishikawa, M. Kawashima, T. Seki and K. Hiraga, "Broadband and compact 3-dB MMIC directional coupler with lumped element," *2010 IEEE MTT-S International Microwave Symposium*, 2010, pp. 728-731.

[20] S. Gruszczynski and K. Wincza, "Broadband rat-race couplers with coupled-line section and impedance transformers," in *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 1, pp. 22-24, Jan. 2012.

[21] C. Tang, C. Tseng and K. Hsu, "Design of the modified planar tandem couplers with a wide passband," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 1, pp. 48-54, Jan. 2013.

[22] H. Yoon and B. Min, "Two section wideband 90° hybrid coupler using parallel-coupled three-line," in *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 6, pp. 548-550, June 2017.

[23] Inder Bahl, Lumped Elements for RF and Microwave Circuits, Artech House, Inc., 2003.

[24] Skyworks Solutions, Inc., "SMV2201-SMV2205 Series: Surface Mount, 0402 Silicon Hyperabrupt Tuning Varactor Diodes," SMV2203-040LF datasheet, May 23, 2012.

[25] MACOM Technology Solutions, Inc., "Solderable AlGaAs Flip Chip PIN," MADP-000907-14020P datasheet.

doi:10.6342/NTU202203942

[26] X. Zhu, T. Yang, P. -L. Chi and R. Xu, "A tunable vector-sum filtering power divider with continuously tuned frequency and arbitrary output phase difference," in *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 11, pp. 1033-1036, Nov. 2020.

[27] L. Guo, H. Zhu and A. Abbosh, "Phase reconfigurable microwave power divider," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 1, pp. 21-25, Jan. 2019.

[28] H. Zhu and A. M. Abbosh, "A compact tunable directional coupler with continuously tuned differential phase," in *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 1, pp. 19-21, Jan. 2018.

[29] C. -H. Lai and C. -Y. Chang, "A wideband forward coupler with tunable coupling ratio using varactor based tuning network," *2018 Asia-Pacific Microwave Conference (APMC)*, 2018, pp. 1492-1494.

[30] S. -C. Lin, Y. -M. Chen, P. -Y. Chiou and S. -F. Chang, "Tunable Wilkinson power divider utilizing parallel-coupled-line-based phase shifters," in *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 4, pp. 335-337, April 2017.

[31] Q. Ma, H. Chung and G. M. Rebeiz, "A 35–105 GHz high image-rejection-ratio IQ receiver with integrated LO doubler and > 40 dB IRR," *2018 IEEE/MTT-S International Microwave Symposium - IMS*, 2018, pp. 595-598.

[32] F. Piri, M. Bassi, N. R. Lacaita, A. Mazzanti and F. Svelto, "A PVT-tolerant > 40-dB IRR, 44% fractional-bandwidth ultra-wideband mm-wave quadrature LO generator for 5G networks in 55-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3576-3586, Dec. 2018.

doi:10.6342/NTU202203942

[33] Y. -H. Lin, C. -C. Yeh, H. -H. Hsu, J. -H. Tsai and T. -W. Huang, "A 22 — 40 GHz wideband image rejection mixer in 0.18−μm CMOS process," *2019 IEEE Asia-Pacific Microwave Conference (APMC)*, 2019, pp. 1515-1517.

[34] M. -Y. Huang, T. Chi, S. Li, T. -Y. Huang and H. Wang, "A 24.5–43.5-GHz ultra-compact CMOS receiver front end with calibration-free instantaneous full-band image rejection for multiband 5G massive MIMO," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 5, pp. 1177-1186, May 2020.

[35] F. Quadrelli *et al*., "A broadband 22–31-GHz bidirectional image-reject up/down converter module in 28-nm CMOS for 5G communications," in *IEEE Journal of Solid-State Circuits*, vol. 57, no. 7, pp. 1968-1981, July 2022.

[36] T. -C. Tsai *et al*., "A Ka-band sub-harmonically pumped mixer using diode-connected MOSFET for 5G MM-wave transceivers," *2018 Asia-Pacific Microwave Conference (APMC)*, 2018, pp. 488-490.

[37] Behzad Razavi, RF Microelectronics, Second Edition, Pearson Education, Inc., 2012.

[38] J. Kao, Z. Tsai, K. Lin and H. Wang, "A modified Wilkinson power divider with isolation bandwidth improvement," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 9, pp. 2768-2780, Sept. 2012.

[39] F. Zhu, K. Wang and K. Wu, "Design considerations for image-rejection enhancement of quadrature mixers," in *IEEE Microwave and Wireless Components Letters*, vol. 29, no. 3, pp. 216-218, March 2019.

[40] H. Okazaki and Y. Yamaguchi, "Wide-band SSB subharmonically pumped mixer MMIC," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 12, pp. 2375-2379, Dec. 1997.

doi:10.6342/NTU202203942

[41] K. Hu, K. Ma and Z. Ma, "An ultra-wideband image-reject up-conversion mixer with a sandwich-coupled transformer for 5G mm-wave communication," in *IEEE Microwave and Wireless Components Letters*, 2022.

[42] S. Li, C. Kuo and H. Chiu, "A 24GHz sub-harmonically image rejection mixer with various asymmetrical diode pair," *2010 International Conference on Microwave and Millimeter Wave Technology*, 2010, pp. 521-524.

[43] H. Wei, C. Meng, J. Su, S. Yu and G. Huang, "17-GHz pHEMT Gilbert single-quadrature downconverter with polyphase filters for image rejection," *2010 Asia-Pacific Microwave Conference*, 2010, pp. 690-693.

[44] Po-Yu Ke *et al*., "A fully integrated 24 GHz sub-harmonic image rejection mixer with quadrature coupler," *2008 Asia-Pacific Microwave Conference*, 2008, pp. 1-4.

[45] Y. Peng *et al*., "A K-band high-gain and low-noise folded CMOS mixer using current-reuse and cross-coupled techniques," in *IEEE Access*, vol. 7, pp. 133218-133226, 2019.

doi:10.6342/NTU202203942