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碳化矽金氧半結構氧化層製程開發及元件應用之研究

Oxidation Process Development and Device Applications in 4H-SiC MIS Structure

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本論文係廖威騏 (R11943202) 在國立臺灣大學電子工程學研究所完成之碩士學位論文，於民國 113 年 6 月 6 日承下列考試委員審查通過及口試及格，特此證明。

The undersigned, appointed by the Graduate Institute of Electronics Engineering on 6 (date) 6 (month) 2024 (year) have examined a Master's Thesis entitled above presented by Wei-Chi Liao (R11943202) candidate and hereby certify that it is worthy of acceptance.

口試委員 Oral examination committee:

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系（所、學位學程）主管 Director:

誌謝

時光飛逝，轉眼間碩班已經要畢業了。回首一看，加上大學部專題，我竟已經進入 CV Lab 三年半的時間，非常開心能在這麼歡樂的實驗室跟著這麼好的指導教授做研究。回想當初因為修了老師開的固態電子學並感覺頗有興趣，因緣際會就開始加入老師的專題。很感謝老師的信任，在推甄放榜後把 SiC 的計畫交給我，雖然在我研究路途上前半段都不是很順遂且充滿挑戰，但老師還是都笑笑地給予我鼓勵以及很多我沒有想過的 idea，不禁佩服老師紮實的半導體知識及深厚的研究功力，感謝有老師不斷的鼓勵與指引才能讓我完成這篇論文。另外我也要感謝兩位口試委員在口試時給我論文寶貴的建議與指教。除了研究外，也非常謝謝老師願意讓我暑假去實習兩次，這對我而言都是非常難能可貴的經驗，最後也順利拿到預聘讓我在求職上得以無後顧之憂。

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摘要

本篇論文重點為探討兩種不同在碳化矽基板上成長氧化層的新穎製程方法，透過材料及電性分析探討氧化層及碳化矽介面處的缺陷密度以及其對於電容-電壓和電流-電壓特性的影響，並探究將金屬/二氧化矽/碳化矽與金屬/氧化鋁/二氧化矽/碳化矽兩種結構的半導體元件分別應用於紫外光感測器以及記憶體之表現。本論文首先介紹一種利用爐管在低於 1000 °C 的間歇噴濺水合氧化法的創新製程，其在一小時內可成長出約 3 到 7 奈米厚的二氧化矽層，並且藉由電導方法得出在平能帶處之介面缺陷密度可低至 2×10^{11} $cm^{-2}eV^{-1}$，與其他前人的研究相比幾乎是最低值。此外，利用此法製造之碳化矽金氧半元件於常溫下偏壓在-6 V，發現其在紫外光照射下之光電流與暗電流相比可高出超過三個數量級，並且在不同功率的紫外光下之光電流展現出高度線性相關性。此元件在從常溫到 100 °C 高溫下的紫外光感測性能也表現出極佳的可靠度。另一種氧化層製程方法是在常溫下於純水中將碳化矽晶圓透過陽極氧化的技術成長出一層極薄的二氧化矽，再利用熱蒸鍍薄鋁結合陽極氧化的方式形成高介電常數之氧化鋁絕緣層，發現其於平能帶處之介面缺陷密度更可低至 1×10^{11} $cm^{-2}eV^{-1}$。透過氧化鋁層的堆疊，碳化矽金氧半元件的閘極漏電流可在不降低閘極電容的同時被有效的抑制。此外，氧化鋁與二氧化矽介面處的陷阱可做為電荷儲存之用，使得其電容-電壓特性展現出很大的遲滯現象，此特性可做為記憶體之應用。在記憶體的可靠度測試中，發現在 100 次讀寫操作循環下仍依舊保持穩定的狀態'0'及狀態'1'電容，顯示其具有做為與碳化矽積體電路整合的記憶體元件之潛力。本篇論文於碳化矽氧化層製程方法之研究有突破創新，相信在碳化矽元件的發展及應用上有其重要性。

關鍵詞：碳化矽、金氧半元件、氧化層成長、介面缺陷密度、紫外光感測器、氧化鋁堆疊、記憶體

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ABSTRACT

The purpose of this thesis is to investigate two novel fabrication methods for growing oxide layers on a 4H-SiC substrate. The defect density at the SiO_2 / 4H-SiC interface, the *C-V* and the *I-V* characteristics, and the performance of semiconductor devices with structures of Al/SiO_2/4H-SiC and Al/Al_2O_3/SiO_2/4H-SiC, in applications of UV sensors and memory devices are studied. Firstly, this thesis introduces an innovative fabrication process using intermittent spray hydrated oxidation (ISHO) in a furnace at a temperature below 1000 °C, which is capable of growing about 3 nm to 7 nm of SiO_2 within one hour. The interface trap density (D_{it}) at the flat band voltage is found to be as low as 2×10^{11} $cm^{-2}eV^{-1}$, which is one of the lowest values in the existing literatures. Additionally, the 4H-SiC metal-insulator-semiconductor (MIS) devices fabricated using this method demonstrate outstanding UV sensing capabilities, with demonstrated photocurrent windows extending over three orders of magnitude in amplification and having linear responsivity, as well as maintaining a photo-to-dark current ratio (PDCR) of about two to three orders of magnitude even at high temperatures up to 100 °C. The other process involves growing a thin SiO_2 layer on the 4H-SiC wafers through anodic oxidation (ANO) in DI water at room temperature, followed by thermal evaporation of thin aluminum layers and the ANO technique to form high-κ Al_2O_3 insulating layers. This yields an even

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lower D_{it} of 1×10^{11} $cm^{-2}eV^{-1}$ at the flat band voltage. With stacking of the Al_2O_3 layer, the gate leakage current in the 4H-SiC MIS devices is effectively suppressed without notably degrading the gate capacitance. Furthermore, the traps at the Al_2O_3 / SiO_2 interface can be utilized for charge storage purposes. These traps result in significant hysteresis phenomenon in the *C-V* characteristics, which is suitable for memory applications. In the memory endurance test, the capacitances of the state '0' and the state '1' remained stable through 100 read-write cycles operation, demonstrating the potential for integration as embedded memory with silicon carbide ICs. This thesis presents breakthrough innovations in the fabrication of the oxide layer in silicon carbide devices, highlighting its significance in the development and applications of silicon carbide devices.

Key words: 4H-SiC, Metal-insulator-semiconductor (MIS), Oxidation processes, Interface trap density, UV sensor, Al_2O_3 stacking, Memory

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Chapter 1

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1-1 Motivation

With the rapid growth in the popularity of electric vehicles (EVs) in recent years, there is an urgent demand for power ICs within EVs. SiC's exceptional physical, chemical, electrical, and mechanical properties make it an ideal semiconductor material for high-power IC applications. 4H-SiC can withstand high-voltage [1], [2] and high-temperature conditions [3] attributed to its wide bandgap of 3.26 eV [4] and outstanding thermal conductivity of 280 W/mK [5]. These inherent characteristics of 4H-SiC contribute to its advantages, such as fast switching speed [6] and high efficiency [7], [8], which are essential for power ICs.

Among the common 4H-SiC power devices, the 4H-SiC MOSFETs are the most important devices used in energy storage systems and the ICs in EVs, such as inverters. The oxide quality plays a critical role in the 4H-SiC MOSFETs. 4H-SiC has a merit that it is the only wide-bandgap semiconductor material which can form a SiO_2 layer by thermal oxidation similar to silicon substrates. However, the traditional oxidation processes require very high temperatures over 1000 °C [9], [10], [11], which may increase the cost and have a higher thermal budget. What's worse, the carbon clustering phenomenon which can lead to the degradation of the SiO_2 / 4H-SiC interface in MOSFETs has been revealed in the previous works [12], [13], [14]. The poor interface properties will have an impact on the performance and reliability of the 4H-SiC

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MOSFETs. One of the solutions to improve the interface is to use NO gas for annealing [15], [16], [17]. Nonetheless, NO gas is toxic to the human body since it is a free radical molecule. Concerning these problems, this thesis aims to investigate the low-temperature and non-toxic oxidation processes with good interface properties for the 4H-SiC substrates, and the applications of the metal-insulator-semiconductor (MIS) devices fabricated by these proposed methods have also been explored.

In Chapter 1, we introduce the basic properties of 4H-SiC compared to other semiconductor materials, the polytypes of silicon carbide, the oxidation processes, the methods to analyze the interface properties, the devices for photodetection, the stacking of high-κ dielectric materials, and the charge trapping phenomenon. In Chapter 2, we propose a novel method for the 4H-SiC oxidation process. The oxidation temperature is below 1000 °C, and the only chemical used in this process is the liquid H_2O. The results show extraordinary interface properties. The fabricated MIS devices also exhibit excellent UV sensing performance and reliability against high temperatures. In Chapter 3, we introduce an alternative method to form oxide layers on the 4H-SiC wafers even at room temperature. Via the stacking of the Al_2O_3 layers, the 4H-SiC MIS devices can be utilized as memory due to the charge-trapping effect at the border of Al_2O_3 / SiO_2. Finally, in Chapter 4, we conclude the mentioned oxidation processes and their oxide quality, together with the UV sensors and memory applications of 4H-SiC MIS devices. The

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possible future work directions are also included in this chapter.

1-2 Properties of 4H-SiC Wide Bandgap Semiconductor

Apart from the continuous scaling of the silicon technology, the research for high-power ICs is also getting more and more popular. Silicon offers advantages such as low cost, high yield, and high carrier mobility, but cannot withstand high voltages. The wide-bandgap materials such as SiC, GaN, Ga_2O_3, and diamond have risen their importance for high-voltage devices. Among them, SiC has become popular for high-voltage applications due to its high critical field, high thermal conductivity, and high electron mobility. The properties of several common semiconductor materials are summarized in Table 1-1 [18], [19].

Silicon carbide is a special material that has hundreds of polytypes, and the 4H, 6H, and 3C are three of the most common polytypes, as shown in Fig. 1-1 [20]. The number in the notations of polytypes represents the number of layers in the repeating unit cell, and the letter denotes the stacking structure of hexagonal (H) or cubic (C) layers. Among these three polytypes, 4H-SiC stands out as the preferred choice for power devices due to several key advantages. Its hexagonal crystal structure offers superior crystal quality and reduced defect density compared to 3C-SiC's cubic structure and 6H-SiC's hexagonal structure with stacking faults. This results in higher breakdown voltages, essential for

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handling high voltages reliably. Additionally, 4H-SiC exhibits higher thermal conductivity than both 3C-SiC and 6H-SiC, enabling better heat dissipation in high-power applications. This thermal advantage enhanced the reliability of devices. Furthermore, 4H-SiC typically demonstrates higher electron mobility, allowing for faster switching speeds and lower on-resistance, thereby improving overall device performance and efficiency. In spite of 6H-SiC's easier growth process, it's easy to stack faults, and crystal defects often compromise device quality, whereas 4H-SiC strikes a balance between manufacturability and crystal quality, making it ideal for mass production of high-performance power devices. Consequently, the combination of superior crystal quality, high breakdown voltage, excellent thermal conductivity, and superior electron mobility make 4H-SiC the optimal choice for a wide range of power device applications.

1-3 Oxidation Processes and Interface Characterization

In this section, we will introduce two kinds of processes to form oxide on the SiC wafers, and two methods for characterizing the interface trap density (D_{it}).

1-3-1 Thermal Oxidation and Carbon Clustering

Thermal oxidation with a furnace is a common way to grow a SiO_2 layer for Si and SiC wafers, including dry oxidation and wet oxidation. Dry oxidation involves flowing O_2 gas into a furnace, where it reacts with the substrate's surface to form the oxide layer.

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On the other hand, wet oxidation typically employs steam or a mixture of O_2 and H_2 gases to facilitate the oxidation process within the furnace environment, as shown in Fig. 1-2(a) and (b) [21]. Both techniques offer unique advantages and are widely used in semiconductor manufacturing. The theoretical model for understanding thermal oxidation processes was established by B.E. Deal and A.S. Grove in 1965 [22]. Their model provides insights into the kinetics and mechanisms involved in oxide growth during thermal oxidation, including diffusion and reaction, guiding the optimization of process parameters for desired oxide characteristics.

Nonetheless, previous works have shown the carbon clustering phenomenon in 4H-SiC surface after oxidation, as shown in Fig. 1-3 [12], which will increase D_{it} and degrade the device performance, and this issue is particularly severe in dry oxidation. With an eye to improving the oxide quality, a novel oxidation process by spraying liquid deionized (DI) water into a furnace filled with atmosphere containing 20% oxygen gas will be introduced in section 2-2.

1-3-2 Anodic Oxidation (ANO) Technique

In addition to thermal oxidation, an alternative way to form thin oxide layers is anodic oxidation (ANO) [23]. Its experimental setup is quite simple, with just a DC power supply, two connecting wires, the anode (Si or SiC wafer), the cathode (Pt), and a sink

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filled with DI water. The process is conducted at room temperature. The ANO technique possesses several advantages such as low cost and low thermal budget. Furthermore, the applied electrical field can automatically repair the local defects in the SiO_2, so after an annealing process to remove the H_2O molecules, the oxide can possess excellent quality.

Aside from growing a thin SiO_2 layer, the ANO technique can also be utilized to stack Al_2O_3 layers via depositing a thin aluminum film followed by the ANO process [24]. Chapter 3 will discuss this part further.

1-3-3 Interface Trap Density Analyses

The traps at the insulator and the semiconductor interface can notably affect the devices' electrical characteristics, performance, and reliability. The interface traps are typically classified into two types: acceptor type located above midgap and donor type located below midgap. These interface traps will lead to a shift in the flat band voltage and stretch out of the *C-V* curves, as shown in Fig. 1-4 [25]. The higher D_{it} will lead to lower carrier mobility, and the channel resistance can consequently increase.

Many models have been proposed to evaluate the D_{it} of a MOS capacitor. The conductance method and the high-low frequency capacitance method are the two most common ways to obtain the D_{it} [25]. When the conductance of a device is measured in the depletion region, the conditions are quite simple since the occupancy of the interface

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trap changes only by the capture and emission of the majority carriers, so the near-interface D_{it} can be observed by the signal of energy loss. The AC small-signal equivalent circuit of a MOS capacitor is depicted in Fig. 1-5(a). In this equivalent circuit model, the equivalent parallel capacitance (C_P) and conductance (G_P) are in parallel, and then in series with the gate oxide capacitance (C_{ox}). By applying small AC signals with varying frequencies at a bias voltage, the G_P vs ω relation can be measured. We can then plot the $\frac{G_P}{\omega} - \omega$ curve as shown in Fig. 1-5(b) [26], and the D_{it} and the majority carrier lifetime can be obtained by the values of $\frac{G_P}{\omega}$ and ω at the peak, respectively.

The interface traps can follow the low-frequency signals, but cannot respond to the high-frequency signals. Therefore, the *C-V* curves can exhibit a frequency dispersion phenomenon owing to the interface traps. By measuring the *C-V* characteristics outside the inversion region, we can evaluate the D_{it} at different bias voltages, and further obtain the D_{it} profile along the energy levels in the bandgap.

1-4 Photo-sensing Capability of MIS Devices

In recent years, with the advancement of wireless communication technology, the Internet of Things (IoT) has become more and more popular. Many kinds of sensors are required for IoT, and light sensors are among the important ones. One of the conventional photo sensors is the metal-insulator-semiconductor (MIS) tunnel diode (TD). This

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structure has many advantages, such as low cost, low power, fabricating simplicity, and high sensitivity. Previous works have shown that the MIS TDs on Si(p) substrates can demonstrate outstanding performance and linear responsivity for visible light sensing by the open-circuit voltage (V_{OC}) [27] or the short-circuit current (I_{SC}) [28], as shown in Fig. 1-6(a) and (b), respectively.

On the other hand, MIS devices can also use 4H-SiC as substrates for UV-sensing applications thanks to the wide-bandgap characteristic of 4H-SiC [29], [30]. The energy of visible light is not high enough for the electrons in the valence band to be stimulated to the conduction band so the 4H-SiC MIS devices are insensitive to the visible light spectrum. Additionally, due to the extremely low intrinsic carrier concentration (n_i) of 4H-SiC, the minority carriers are few even in the inversion region in the dark, which offers the advantage of low dark current. However, when a 4H-SiC MIS device is illuminated under UV light, abundant electron-hole pairs generation occurs, and the photocurrent increases tremendously, accordingly enhancing the ON/OFF ratio and making the 4H-SiC MIS device a promising UV sensor.

1-5 High-κ Dielectric Stacking and Charge-trapping Effect

As the transistors keep scaling down, many short-channel effects like the drain-induced barrier lowering (DIBL) effect, poor subthreshold swing (*SS*), the gate-induced

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drain leakage (GIDL), impact ionization, and so on, have significantly affected the static and dynamic performances of the devices, which slows down the progression of Moore's law. To improve these problems, the gate oxide capacitance, which means the capability to control the channel, must be increased. The gate oxide capacitance can be determined by

$$C_{ox} = \frac{\kappa \varepsilon_0}{d_{ox}} A \tag{1-1}$$

where κ, ε_0, d_{ox}, and A are the dielectric constant, permittivity in vacuum, physical oxide thickness, and the area under the gate, respectively. Accordingly, one way to increase C_{ox} is by thinning the d_{ox}. Nonetheless, this method can cause the increment of the tunneling gate leakage. Therefore, the better alternative is to use a high-κ material as the gate dielectric. The high-κ metal gate (HKMG) technology has been introduced by Intel in its 45 nm node with adjustable work function metal (WFM) and high-κ dielectric to enhance the performance of transistors, as shown in Fig. 1-7 [31]. By measuring the C_{ox}, the equivalent oxide thickness (EOT) is defined as

$$EOT = \frac{\varepsilon_{SiO_2}}{C_{ox}} A \tag{1-2}$$

where ε_{SiO_2} is the permittivity of SiO_2. The EOT will be discussed frequently in the later chapters evaluated by the measured *C-V* characteristics, since the measured capacitance (C_m) will approximate the C_{ox} in the accumulation region. Additionally, the subthreshold swing is directly related to the C_{ox} by

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$$SS = ln(10)\frac{kT}{q}\left(1 + \frac{C_s + C_{it}}{C_{ox}}\right) \quad (1\text{-}3)$$

where C_s and C_{it} are capacitances of the semiconductor and the interface traps, respectively. Consequently, with the HKMG technology, the SS can be lowered by enhancing the C_{ox} while not increasing the gate leakage, thereby effectively improving the short-channel effects.

Al_2O_3 is a kind of high-κ dielectric material with a bandgap of 8.8 eV [32] and a dielectric constant of about 7 to 8.5 [33]. Additionally, the interfacial traps at the border of Al_2O_3 / SiO_2 can serve as a charge-trapping layer. Previous works have demonstrated the non-volatile memory (NVM) applications with Al_2O_3 stacking on the MIS TDs on Si(p) substrates by nitrate oxidation, showing a large two-state current window, as shown in Fig. 1-8 [34]. The investigation of the memory applications with Al_2O_3 stacking on the 4H-SiC MIS devices by the ANO technique will be discussed in Chapter 3, which can potentially be integrated with 4H-SiC power ICs as embedded memory devices.

1-6 Summary

In this chapter, we begin with the motivations and the organization of this thesis. Next, the properties of 4H-SiC are compared to other common semiconductor materials, and the polytypes of silicon carbide are introduced. We then introduce two oxidation methods, thermal oxidation and the ANO technique, highlighting the importance of oxide

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quality in 4H-SiC MIS devices. The challenges associated with traditional high-temperature oxidation processes, such as high cost, high thermal budget, and interface degradation due to carbon clustering are noted. Two methods for interface trap density analyses, the conductance method and the high-low frequency capacitance method, are introduced. Finally, the photo-sensing capability of MIS devices and the high-κ dielectric stacking technology as well as the charge-trapping effect are mentioned. Based on this knowledge, the following chapters will investigate the novel oxidation processes with analyses of the interface properties and the applications of the fabricated 4H-SiC MIS devices.

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Table 1-1. Intrinsic property parameters of Si, 4H-SiC, GaN, diamond, and β-Ga_2O_3 [18], [19].

Parameter	Si	4H-SiC	GaN	Diamond	β-Ga_2O_3
E_g (eV)	1.12	3.26	3.39	5.47	4.90
μ_n ($cm^2V^{-1}s^{-1}$)	1350	950	1000	1800	300
μ_p ($cm^2V^{-1}s^{-1}$)	480	120	200	2000	<10
E_C (MV/cm)	0.25	2.2	3.3	5.6	8
V_{sat} (10^7 cm/s)	1	2.5	2	3	2.42
n_i (cm^{-3})	1.5×10^{10}	8×10^{-9}	2×10^{-10}	1×10^{-20}	1.8×10^{-23}
λ ($Wcm^{-1}K^{-1}$)	1.5	4	1.3	20	0.27
BFoM relative to Si	1	500	1300	9000	3444
ε_r	11.9	9.7	9.0	5.7	10

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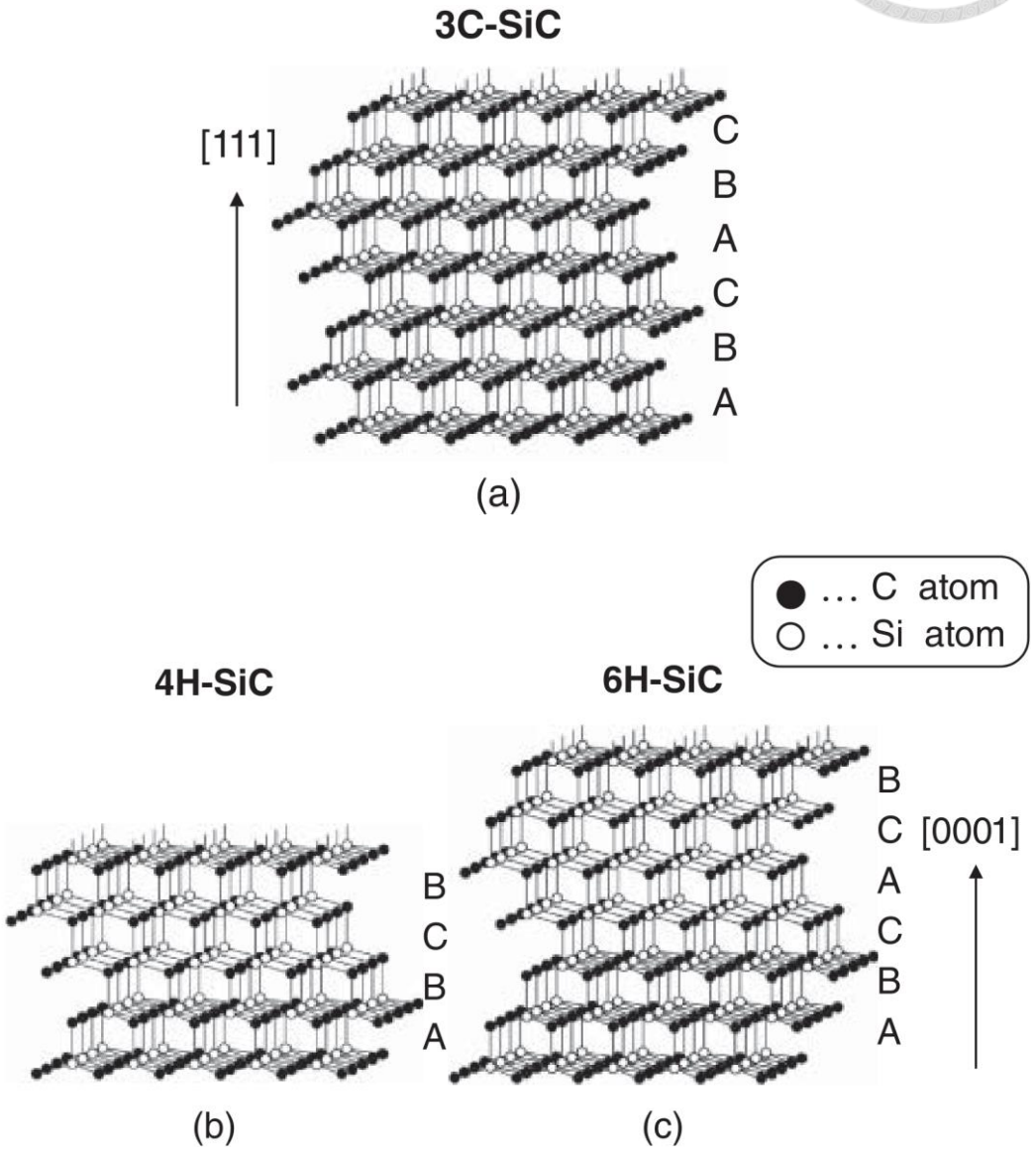

Fig. 1-1. Common layer-stacking structures of 3C-SiC, 4H-SiC, and 6H-SiC polytypes [20].

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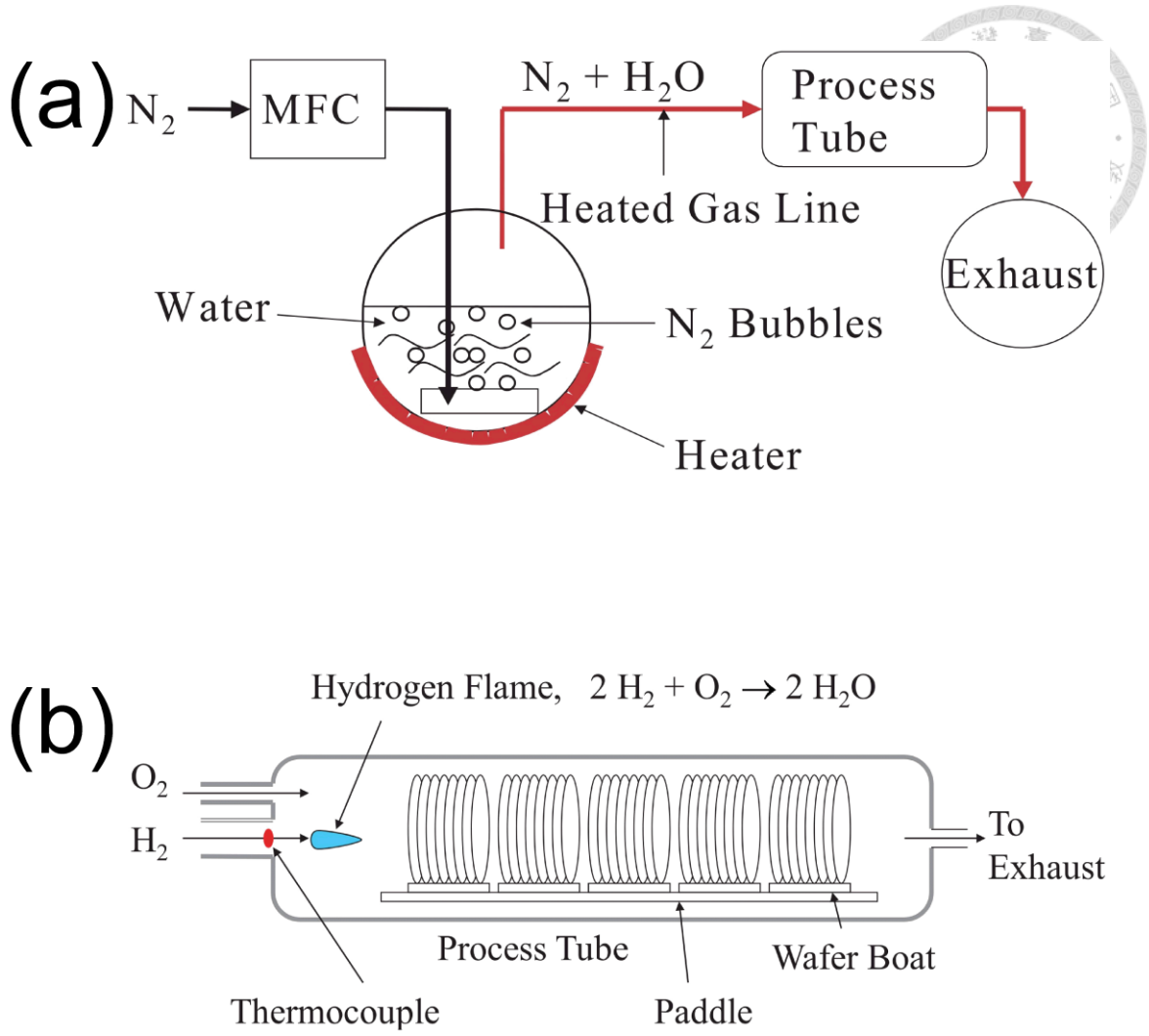

Fig. 1-2. Experimental setups of wet oxidation with (a) steam and (b) mixture of O_2 and H_2 gases [21].

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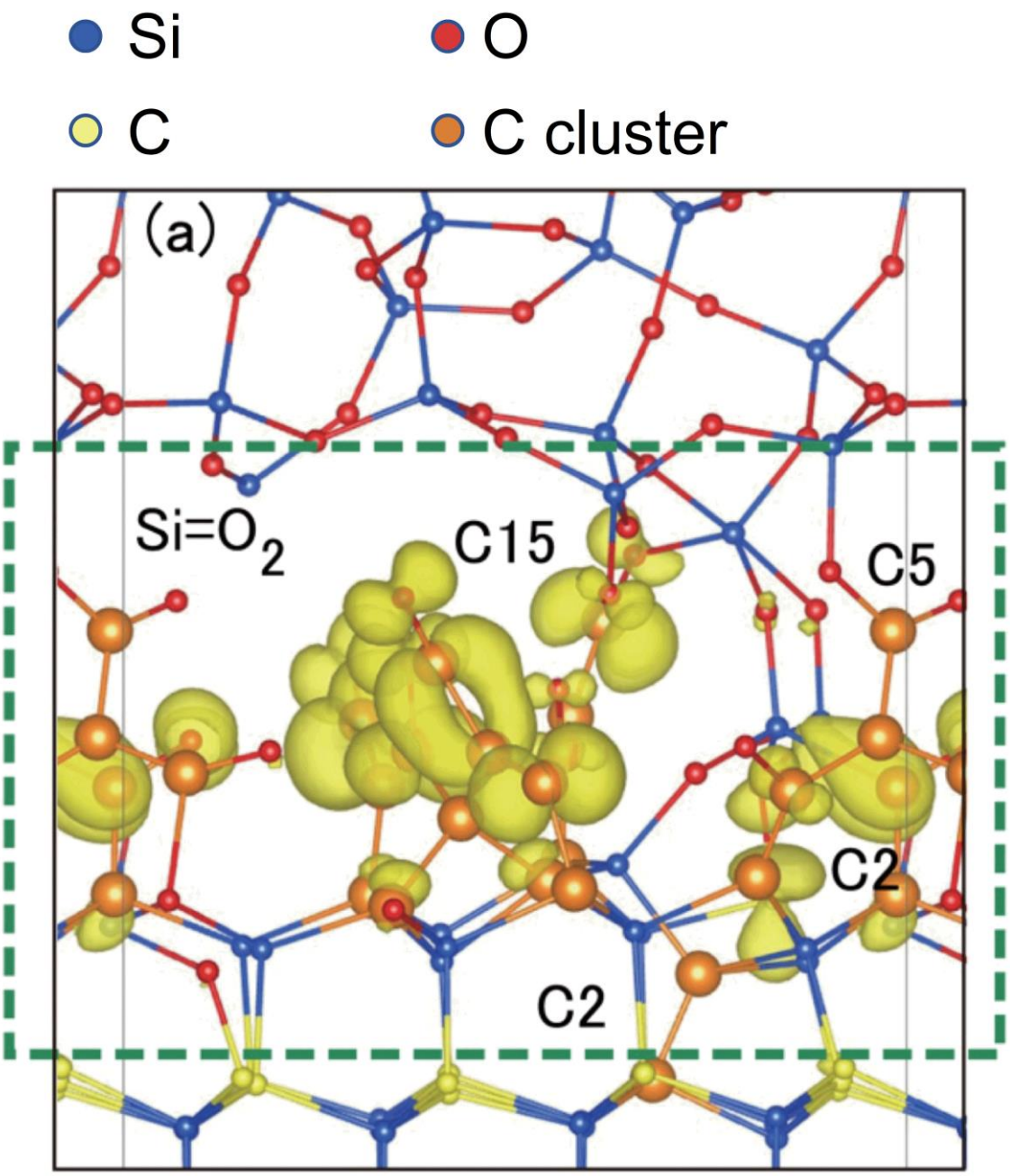

Fig. 1-3. Carbon clustering phenomenon after oxidation [12].

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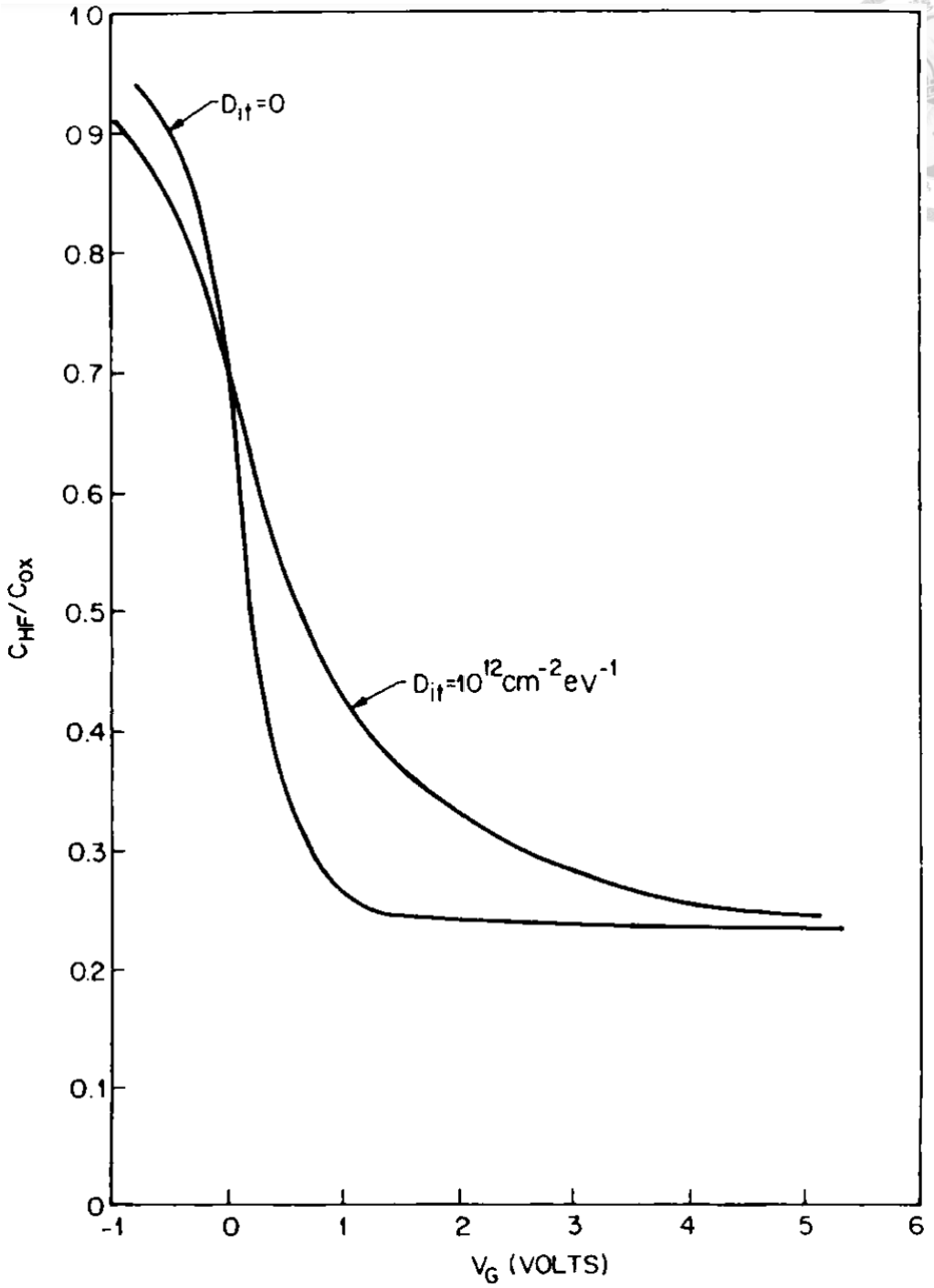

Fig. 1-4. Shift of the flat band voltage and stretch out of the C-V curves caused by D_{it} [25].

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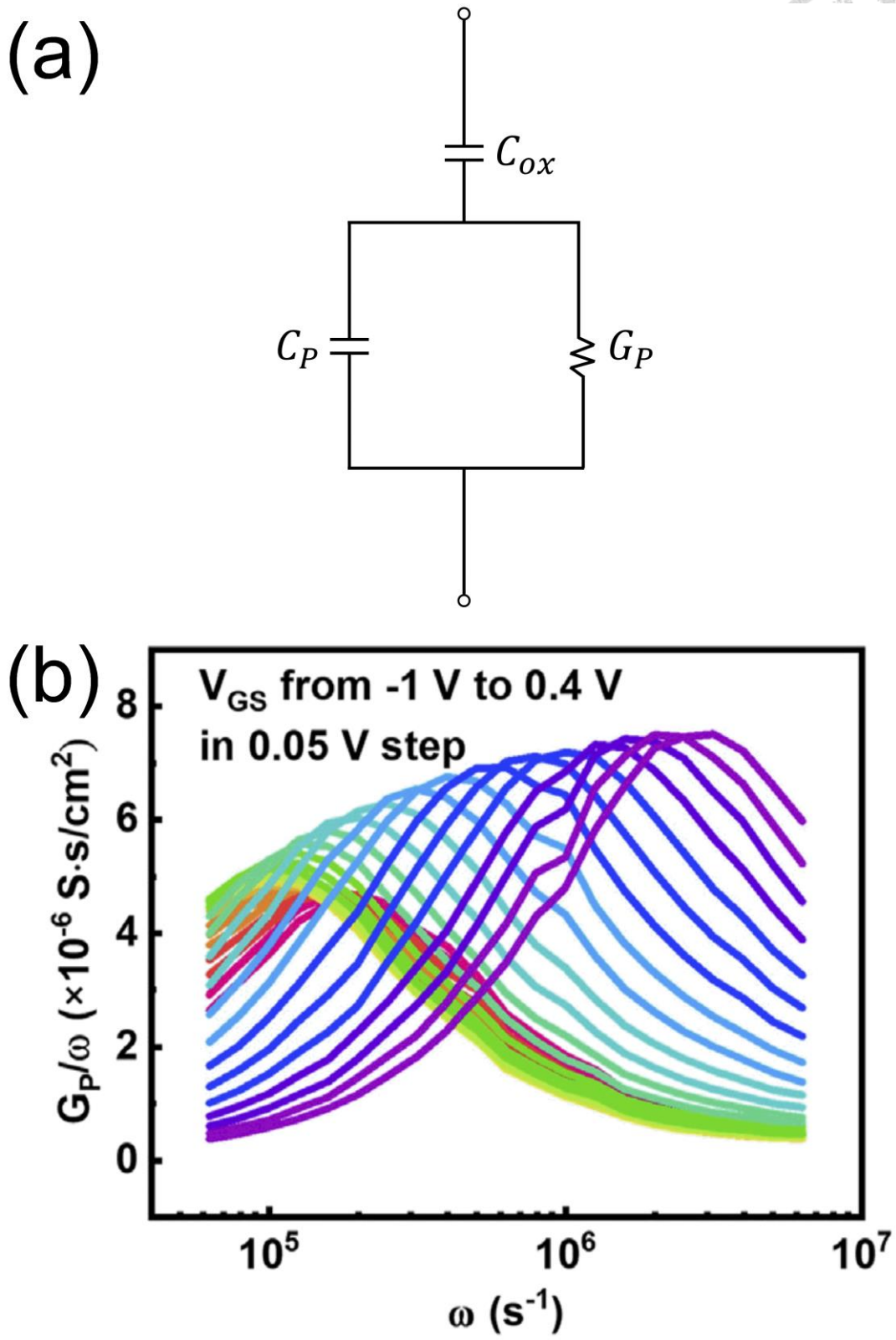

Fig. 1-5. (a) Small-signal equivalent circuit of a MOS capacitor. (b) Conductance method by the plot of G_P/ω vs ω for an ALD In_2O_3 MOS capacitor with 3.5 nm HfO_2 as the gate insulator [26].

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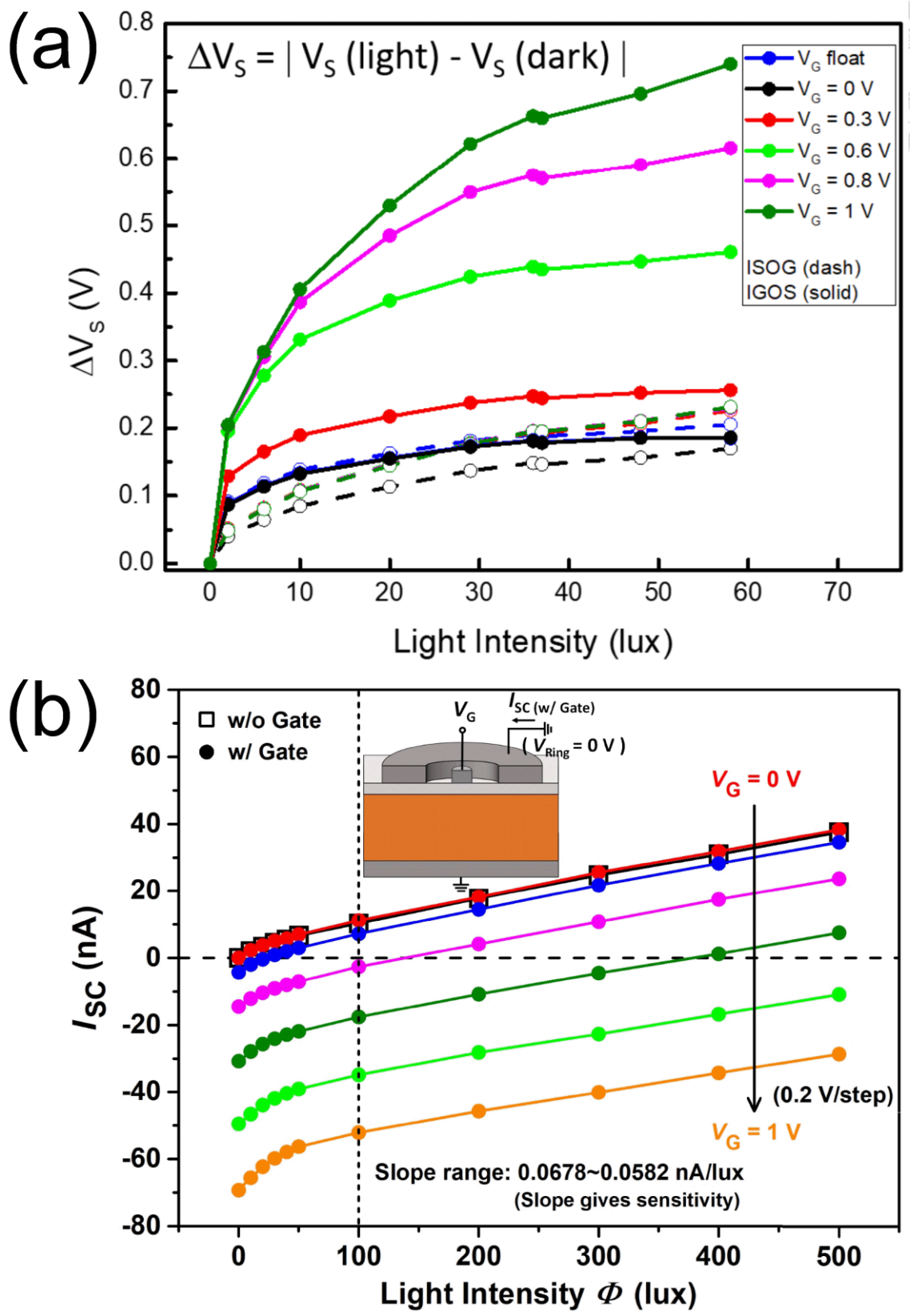

Fig. 1-6. MIS TDs on Si(p) outstanding performance and linear responsivity for visible light sensing by (a) open-circuit voltage (V_{OC}) [27] and (b) short-circuit current (I_{SC}) [28].

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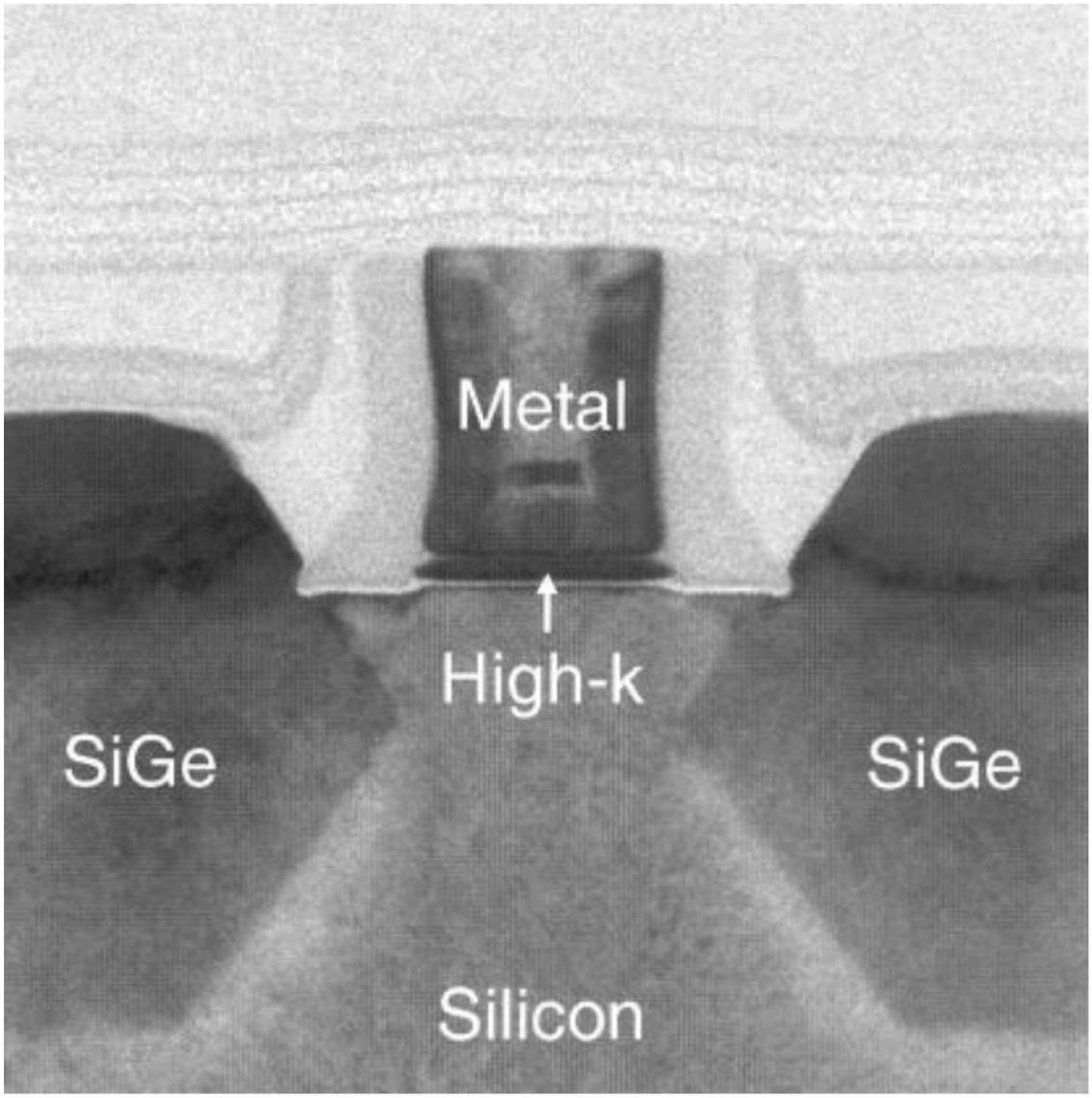

Fig. 1-7. High-κ metal gate (HKMG) technology introduced by Intel in its 45 nm node with adjustable work function metal (WFM) and high-κ dielectric [31].

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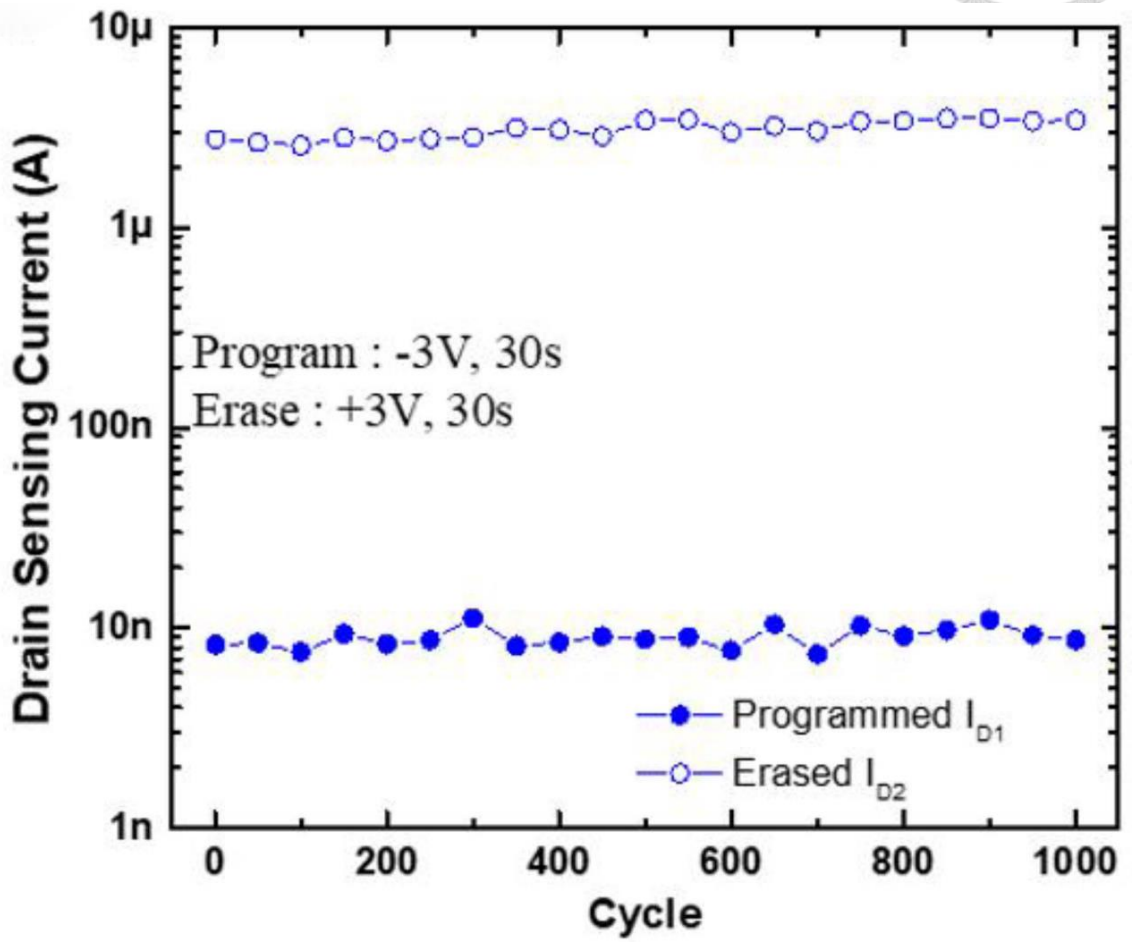

Fig. 1-8. Al_2O_3 stacking MIS TDs on Si(p) substrates by nitrate oxidation, showing a large two-state current window [34].

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Chapter 2

Interface Analyses for SiO_2 Grown by Sub-1000 °C Intermittent Spray Hydrated Oxidation (ISHO) and Investigation for UV Sensor Applications

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2-1 Introduction

As the automotive electronics market grows rapidly, the demand for SiC MOSFETs has also increased significantly. Among all wide-bandgap semiconductors, silicon carbide has a distinctive advantage: it is the only material that can grow a SiO_2 film through thermal oxidation like silicon wafers. Nonetheless, the deterioration of the SiO_2 / 4H-SiC interface in MOSFETs after oxidation owing to carbon clustering has been unveiled, especially for dry oxidation. The higher interface trap density (D_{it}) would lead to higher on-resistance (R_{on}), lower channel mobility (μ_{ch}), and poor subthreshold swing (SS). In view of this, a novel furnace oxidation technique is proposed in this chapter. Unlike the conventional thermal oxidation that typically requires temperatures of over 1000 °C, the oxidation temperature is below 1000 °C for this technique, but can still form a SiO_2 layer with low D_{it} and low oxide charge in this work, which offers advantages such as low cost and low thermal budget compared to other works.

Furthermore, previous works have demonstrated that the 4H-SiC devices can be applied to UV sensors thanks to their wide bandgap characteristics. Due to the high quality of our SiO_2 film, our metal-insulator-semiconductor (MIS) structure devices with thin oxides possess very low reverse leakage current and exhibit a large current window for UV sensing. Additionally, these devices have also been tested at various high temperatures and demonstrated excellent performance and reliability, indicating the high-

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temperature tolerance capability of 4H-SiC.

2-2 Experimental

Nitrogen-doped n-type 4H-SiC epitaxial wafers produced by Cree, Inc. with substrate resistivity of 1.57×10^{-2} Ω-cm were adopted. The doping concentrations were 3.46×10^{15} cm^{-3} for 10-μm thick n^- drift layer and 1.5×10^{18} cm^{-3} for 0.5-μm thick n^+ buffer layer. The entire process flow is shown in Fig. 2-1(a). After Radio Cooperation of America (RCA) cleaning, the intermittent spray hydrated oxidation (ISHO) was employed. The wafers were positioned inside a semi-open furnace and oxidized for 10 to 60 minutes at 950 °C in an ambient of 1 atm air. Meanwhile, liquid deionized (DI) water was intermittently sprayed into the furnace at the beginning, middle, and near the end of each oxidation process. Fig. 2-1(b) shows the schematic diagram of the ISHO experimental setup. Following the ISHO process, the furnace was maintained at 950 °C, and N_2 gas was introduced for annealing for 10 minutes. Subsequently, a 150 nm layer of aluminum was deposited as the metal gate by thermal evaporation, and then the circular gate with a radius of 85 μm was patterned by photolithography and wet etching. Finally, the backside was processed with buffered oxide etch (BOE), and a 150 nm aluminum film was deposited as the back electrode. All the electrical characteristics data were measured by Agilent B1500A semiconductor device analyzer.

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2-3 Results and Discussion

2-3-1 Material Characterization of the SiO_2 Layer and Deal-Grove Model Fitting for ISHO

The structure of the fabricated MIS device is shown in Fig. 2-2(a). The transmission electron microscopy (TEM) image of an MIS sample is shown in Fig. 2-2(b). The oxide thickness was 5.0 nm, including a 4 nm SiO_2 layer and a 1 nm $Al_xSi_yO_z$ transition layer with x: y: z = 1: 0.2: 1. Since there's no thermal process after the top gate aluminum deposition, this transition layer might be formed due to the reduction-oxidation reaction between Al and SiO_2. Furthermore, the energy-dispersive X-ray spectroscopy (EDX) mapping, as shown in Fig. 2-3(a), indicated no obvious carbon atoms clustering at the SiO_2 / 4H-SiC interface. Additionally, Fig. 2-3(b) presents the depth profile obtained by the EDX line scan, with dashed lines marking the borders of different layers which were consistent with the thicknesses of the SiO_2 and transition layers.

The *C-V* characteristics of samples subjected to different ISHO times were measured, as shown in Fig. 2-4(a). The high-frequency *C-V* curves measured at 100 kHz yield equivalent oxide thicknesses (EOTs) of 3.5, 5.0, 5.6, 6.3, and 7.2 nm for samples subjected to ISHO times of 10, 20, 40, 50, and 60 min, respectively. The flat-band voltages (V_{FB}) were all around 0.5 V. Notably, the forward and backward curves were almost overlapping, indicating negligible hysteresis flat-band shift and suggesting the

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oxide possessed few mobile charges as well as minimal trapping and de-trapping phenomena, as illustrated in Fig. 2-4(b).

To further understand the conditions during the ISHO process, the EOTs of different ISHO times were fitted by the Deal-Grove model [22] from the equation

$$\frac{{x_0}^2}{B} + \frac{x_0}{B/A} = t \tag{2-1}$$

where x_0 and t are the oxide thickness and the oxidation time, respectively. Fig. 2-5 shows the results of EOT versus ISHO time with the fitting curve. The parabolic rate constant B related to diffusion was much smaller compared to the linear rate constant B/A related to reaction, which indicated that the process was reaction-dominant. The limitation of diffusion might occur because, for samples with longer ISHO times, the intervals between sprays were too long, resulting in the moisture inside the furnace not reaching saturation. Concerning this, future work will study on the conditions for a constant spray interval.

2-3-2 Electrical Characterization and Interface Trap Density Analysis

As a high-electron-mobility material, 4H-SiC has been reported to exhibit electron mobility exceeding 1000 $cm^2V^{-1}s^{-1}$ [35]. However, the actual mobility in 4H-SiC MOSFETs may degrade to about 100 times lower than its Hall mobility due to the poor SiO_2 / 4H-SiC interface [36]. Accordingly, the following will discuss the interface trap

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density (D_{it}) of our MIS devices. A sample near the position of the one analyzed by TEM and EDX shown in Fig. 2-2(b) and Fig. 2-3(a) was specifically chosen for further analysis. Its EOT of 5.2 nm was close to the physical oxide thickness observed in Fig. 2-2(b). The *I-V* and the *C-V* curves at different frequencies of the sample were measured, as depicted in Fig. 2-6(a) and (b), respectively. Firstly, the gate current in the accumulation region (V_G = +2 V) was only approximately 10 pA, and the saturation current at reverse bias remained around 100 fA, indicating the absence of significant leakage paths in the oxide. The band diagram illustrated in Fig. 2-6(c) explains the mechanisms of the saturation current at reverse bias, which comprises the electrons tunneling from metal to the conduction band of the semiconductor, the holes tunneling from the semiconductor to metal, the trap-assisted tunneling (TAT) electrons via the interface traps, and the recombination of the electrons at the interface traps and the holes in the valance band. Therefore, the lower D_{it} can contribute to the lower saturation current. As for the *C-V* characteristics, minimal frequency dispersion and hysteresis phenomena were observed, with the flat-band voltage found to be 0.325 V. To evaluate D_{it}, the conductance method [25], [37] was applied at the flat-band condition using the following equations

$$\frac{G_P}{\omega} = \frac{\omega {C_{ox}}^2 G_m}{{G_m}^2 + \omega^2 (C_{ox} - C_m)^2} \tag{2-2}$$

and

$$D_{it} = \frac{2.5}{qA}\left(\frac{G_P}{\omega}\right)_{max} \tag{2-3}$$

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where G_P, C_{ox}, G_m and C_m are the equivalent parallel conductance, oxide capacitance, measured conductance and capacitance, respectively, and A is the area of the device. In addition, the carrier lifetime for electrons (τ_n) is given by

$$\tau_n = \frac{1.98}{\omega}. \tag{2-4}$$

Fig. 2-7 shows the results obtained by using the conductance method, revealing a D_{it} of 2×10^{11} cm^{-2}eV^{-1} at the flat-band voltage, and a τ_n of 0.75 μs which is consistent with the results from other studies [38], [39]. Additionally, the effective oxide charge (Q_{eff}) can consequently be estimated to be $Q_{eff}/q = 1.2 \times 10^{11}$ cm^{-2} by the flat-band voltage shift relative to the ideal value. Both D_{it} and Q_{eff} were notably low for the oxide of 4H-SiC [17], [40], [41], [42]. Fig. 2-8 presents the comparison between the measured high-frequency *C-V* and the theoretical high-frequency *C-V* characteristics with uniform D_{it} of 2×10^{11} cm^{-2}eV^{-1} along the band gap computed with MATLAB, demonstrating close agreement and validating the results obtained by the conductance method.

Furthermore, to acquire the D_{it} along the energy levels in the band gap, the high-low frequency capacitance method [25] was also employed for the device with *C-V* curves shown in Fig. 2-6(a). The D_{it} in the depletion region can be estimated as

$$D_{it} = \frac{1}{q}\left(\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}\right)^{-1} \tag{2-5}$$

where C_{LF} and C_{HF} are the low-frequency (1kHz) and high-frequency (1MHz)

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capacitances respectively. The D_{it} distribution along the energy levels in the depletion region is shown in Fig. 2-9. The D_{it} at flat-band voltage was about 3×10^{11} $cm^{-2}eV^{-1}$ by the high-low frequency method, which is closely aligned with the result obtained by the conductance method, further affirming the high quality of the interface.

To further understand the excellent interface properties observed in the electrical characteristics, X-ray photoelectron spectroscopy (XPS) was employed to analyze the bonding composition at the SiO_2 / 4H-SiC interface, as shown in Fig. 2-10. Most carbon bonds remained Si-C bonds, with only 14.2% being C-C bonds, indicating a minimal carbon clustering phenomenon. Additionally, oxygen bonds with hydrogen were observed, probably originating from the H_2O molecules provided during the ISHO process. Moreover, these hydrogen atoms might also bond to the Si atoms at the interface, potentially passivating dangling bonds and reducing D_{it}. Finally, Fig. 2-11 benchmarks the D_{it} at various energy levels near the conduction band of the 4H-SiC MIS device fabricated by ISHO in comparison with those in [17], exhibiting almost the lowest D_{it} for ISHO.

2-3-3 UV Sensing Capabilities and Temperature-dependent Reliability

With few interface traps in the MIS devices, they possessed low saturation current

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in the dark, which is vital for the performance and power saving of UV sensors. The UV sensing capability of the 4H-SiC MIS devices was investigated. Fig. 2-12(a) shows the results of the *C-V* curves measured from -6 V to +1 V at 1 kHz under different lighting conditions: in the dark, under visible light, under UV light, and again in the dark after turning off the UV light. The overlapping *C-V* curves obtained in the dark and under visible light suggested that the 4H-SiC MIS device was insensitive to visible light. One can also observe that when it's illuminated under UV light, the capacitance in the range of -4 V to 0 V was obviously higher than that in the dark, which is the signal of the generation of the minority hole carriers. Additionally, after UV light illumination, a right shift in the *C-V* curve in the accumulation region was observed. This might be attributed to the generation of many high-energy electrons under UV light, and when the device was swept to +1 V, these hot electrons were injected into the oxide and then were trapped, causing the flat-band voltage to shift right. To verify this hypothesis, another sample was examined, as shown in Fig. 2-12(b). The device was subjected to *C-V* curves swept from -6 V to 0 V, ensuring it remained in the depletion region during UV light illumination. The results showed overlapping *C-V* curves in the dark before and after UV light illumination, thereby confirming our speculation.

To evaluate the performance of our MIS devices as UV sensors, samples with EOTs of 5.2 nm and 3.6 nm were analyzed for their *I-V* characteristics under UV light

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illumination with varying intensities, as depicted in Fig. 2-13(a) and (b), respectively. The *I-V* curves obtained in the dark and under visible light exhibited minimal variation, while the UV photocurrents were beyond three orders of magnitude larger than the dark currents at -6 V. The device with an EOT of 5.2 nm demonstrated slightly larger current windows (CWs), i.e., the difference between the dark currents and the UV photocurrents, compared to the device with an EOT of 3.6 nm. This difference can be attributed to the higher tunneling rate through the thinner oxide layer, resulting in increased leakage currents; on the contrary, both devices exhibited similar photocurrents under UV illumination, indicating saturation due to a similar amount of UV-generated holes. The band diagrams for the conditions of thicker and thinner oxide in the dark and under UV light are illustrated in Fig. 2-14(a) and (b), respectively. For the photocurrents under varying UV intensities, both samples demonstrated excellent linear responsivity, as shown in Fig. 2-15. The gate currents at -6 V exhibited a strong correlation between the gate current and the UV power ($R^2 = 0.99$) for both samples, affirming the exceptional performance of the MIS devices as UV sensors.

In addition to the performance at room temperature, the reliability of the 4H-SiC MIS device with EOT = 5.2 nm was also examined at various temperatures. Fig. 2-16(a) demonstrates the *I-V* characteristics swept from 0 V to -6 V at room temperature (21 ˚C) to 100 ˚C in the dark and under the 60 W UV light. The dark currents at -6 V at different

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temperatures were almost the same, which was probably because they were lower than the limit of detection by Agilent B1500A, while the photocurrents remained stable at temperatures lower than 80 ˚C. Even with slight fluctuations in the photocurrents at temperatures exceeding 80 ˚C, the current windows still exhibited no deterioration. Additionally, for the photocurrents, as the gate voltage swept from -6 V to 0 V, the open-circuit voltage (V_{OC}) [27] which is the point where the current approached zero, shifted towards the left with increasing temperature, as shown in Fig. 2-16(b). Because the current formed by electrons tunneling from the metal to the semiconductor was not significantly affected by temperature, and under the same sweeping rate, the displacement current remained constant, this phenomenon could be explained by the rising of the recombination rate for the higher temperature, resulting in the enhancement of the positive recombination current. Finally, Fig. 2-17 summarizes the UV sensing reliability via the current window and the photo-to-dark current ratio (PDCR) [43] as

$$PDCR = \frac{I_{UV} - I_{Dark}}{I_{Dark}} \tag{2-6}$$

at varying temperatures. The PDCR of the MIS device could still maintain at about two to three orders of magnitude at high temperatures, proving the 4H-SiC MIS device as a promising UV sensor.

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2-4 Summary

In this chapter, an innovative approach for fabricating low interface trap density 4H-SiC metal-insulator-semiconductor (MIS) structures through sub-1000 °C intermittent spray hydrated oxidation (ISHO) is presented. Material and electrical characterization results reveal the fabrication of a high-quality SiO_2 layer with a controllable oxide thickness from about 3 nm to 7 nm within 1 hour, showing minimal carbon clustering at the interface and resulting in a remarkably low interface trap density (D_{it}) of 2×10^{11} $cm^{-2}eV^{-1}$ at flat-band voltage. Furthermore, the fabricated MIS devices exhibit outstanding UV sensing capabilities, with demonstrated photocurrent windows extending about three orders of magnitude in amplification and having linear responsivity, as well as maintaining a photo-to-dark current ratio (PDCR) of about two to three orders of magnitude even at high temperatures up to 100 °C, affirming the high-temperature tolerance capability. These findings highlight the ISHO technique as a promising method for forming high-quality oxide for 4H-SiC and the potential of 4H-SiC MIS devices for high-performance UV sensor applications.

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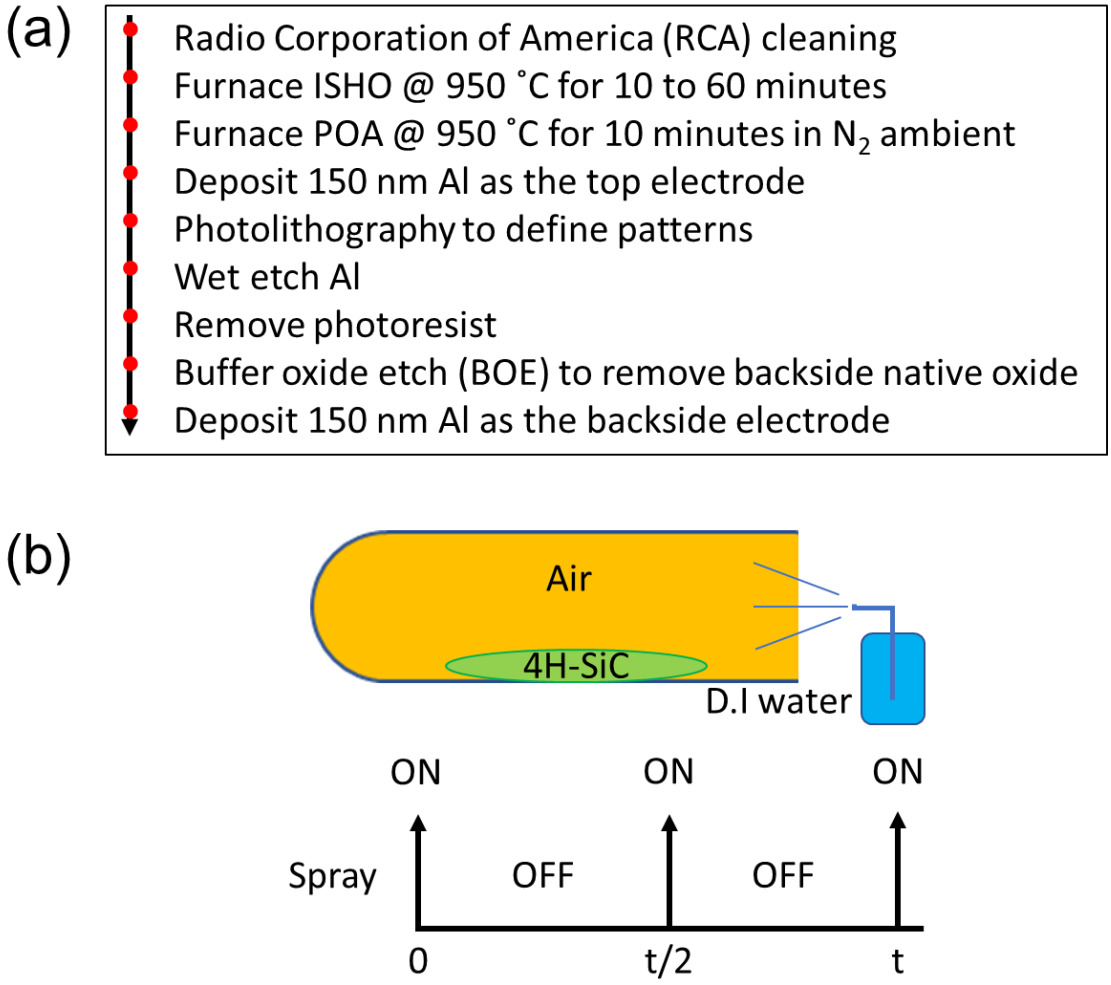

Fig. 2-1. (a) Fabrication process flow. (b) Schematic diagram of the ISHO experimental setup. Note that t = 10, 20, 40, 50, and 60 min.

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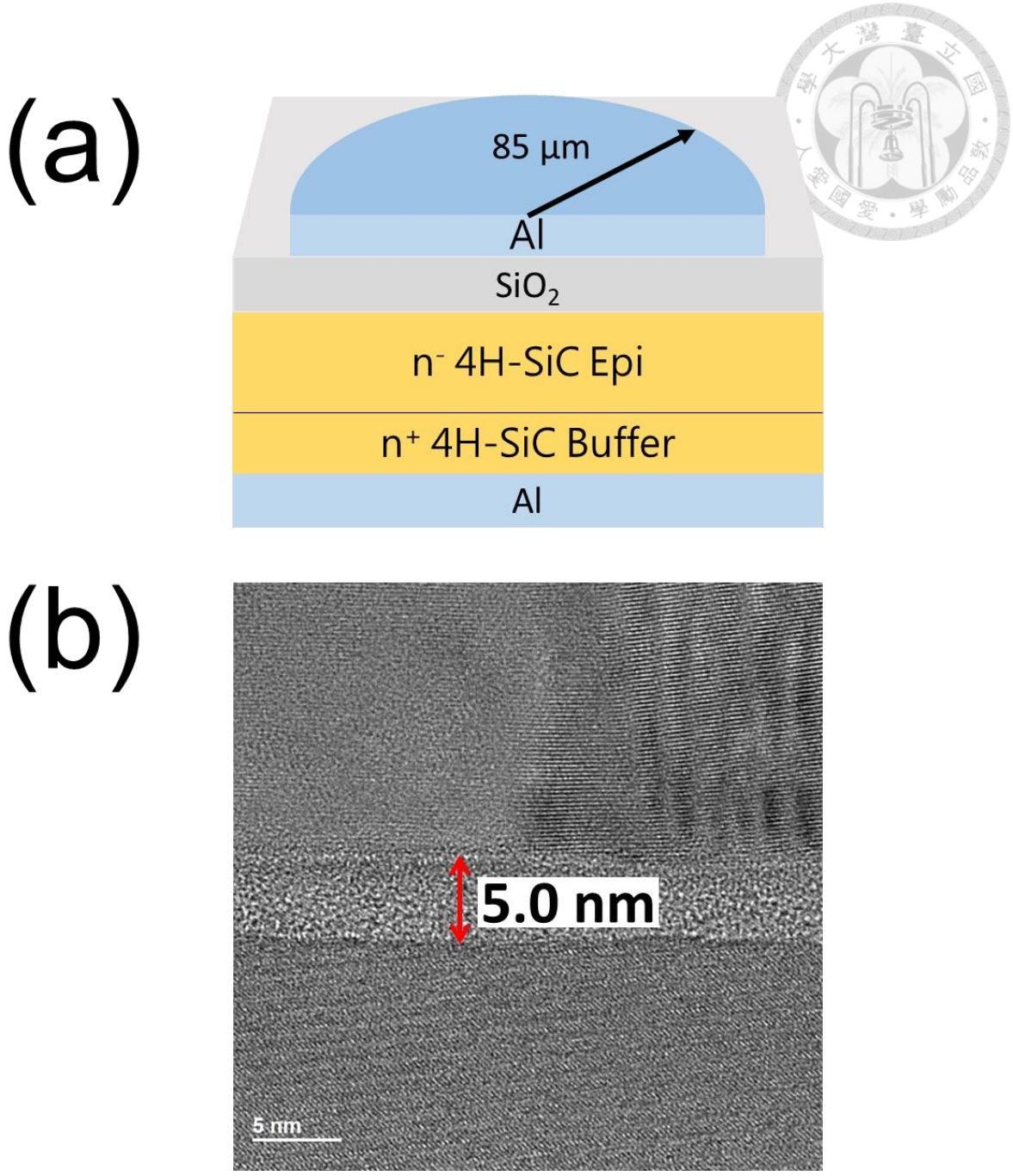

Fig. 2-2. (a) Crosssection of the MIS structure device. (b) TEM image of an MIS sample, showing the oxide thickness being 5.0 nm.

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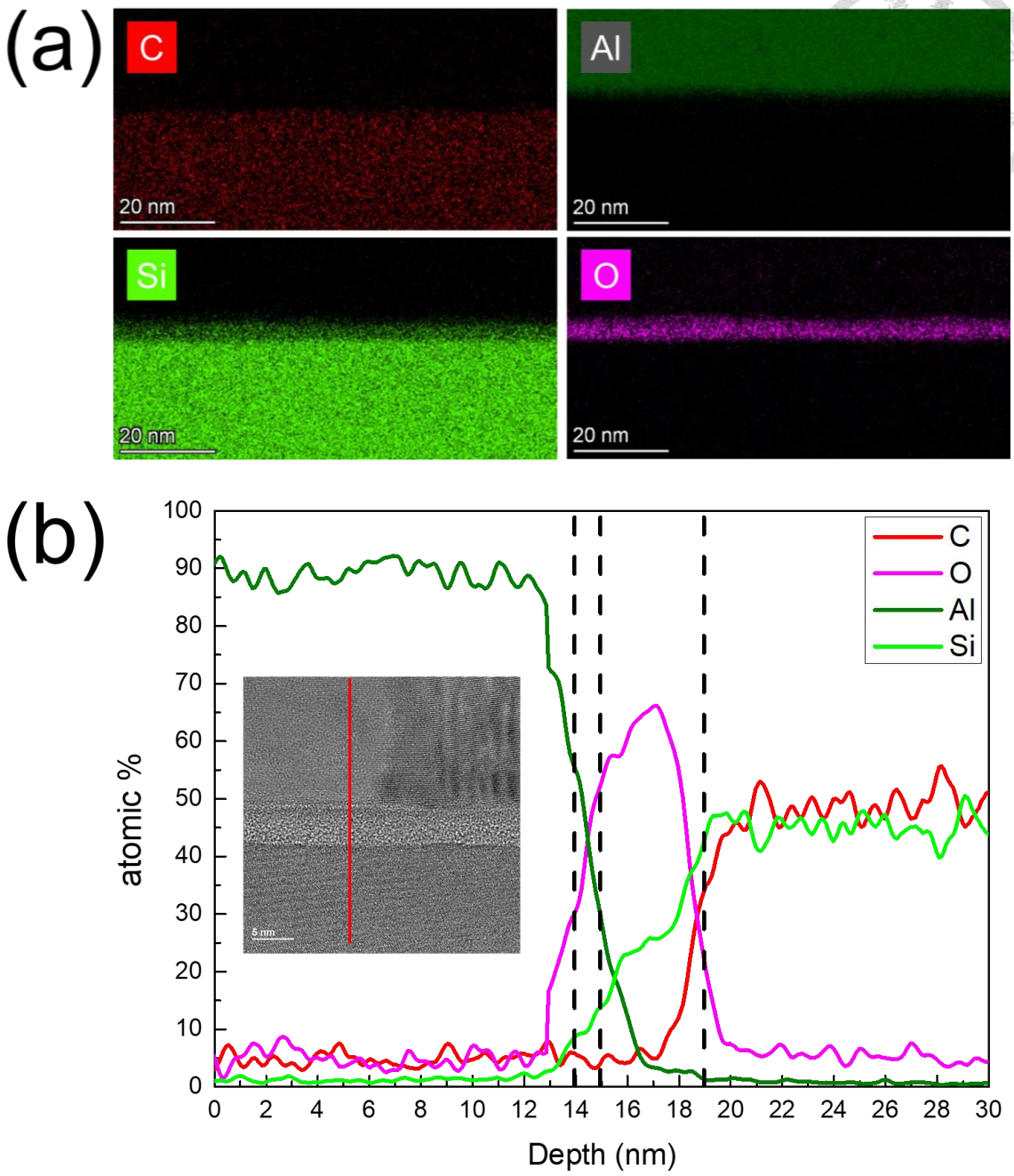

Fig. 2-3. (a) EDX mapping image for the elements of C, Al, Si, and O, presenting no obvious carbon atoms clustering at the SiO_2 / 4H-SiC interface. (b) Depth profile analyzed by the EDX line scan. The thickness of the SiO_2 layer matches the result in the TEM image.

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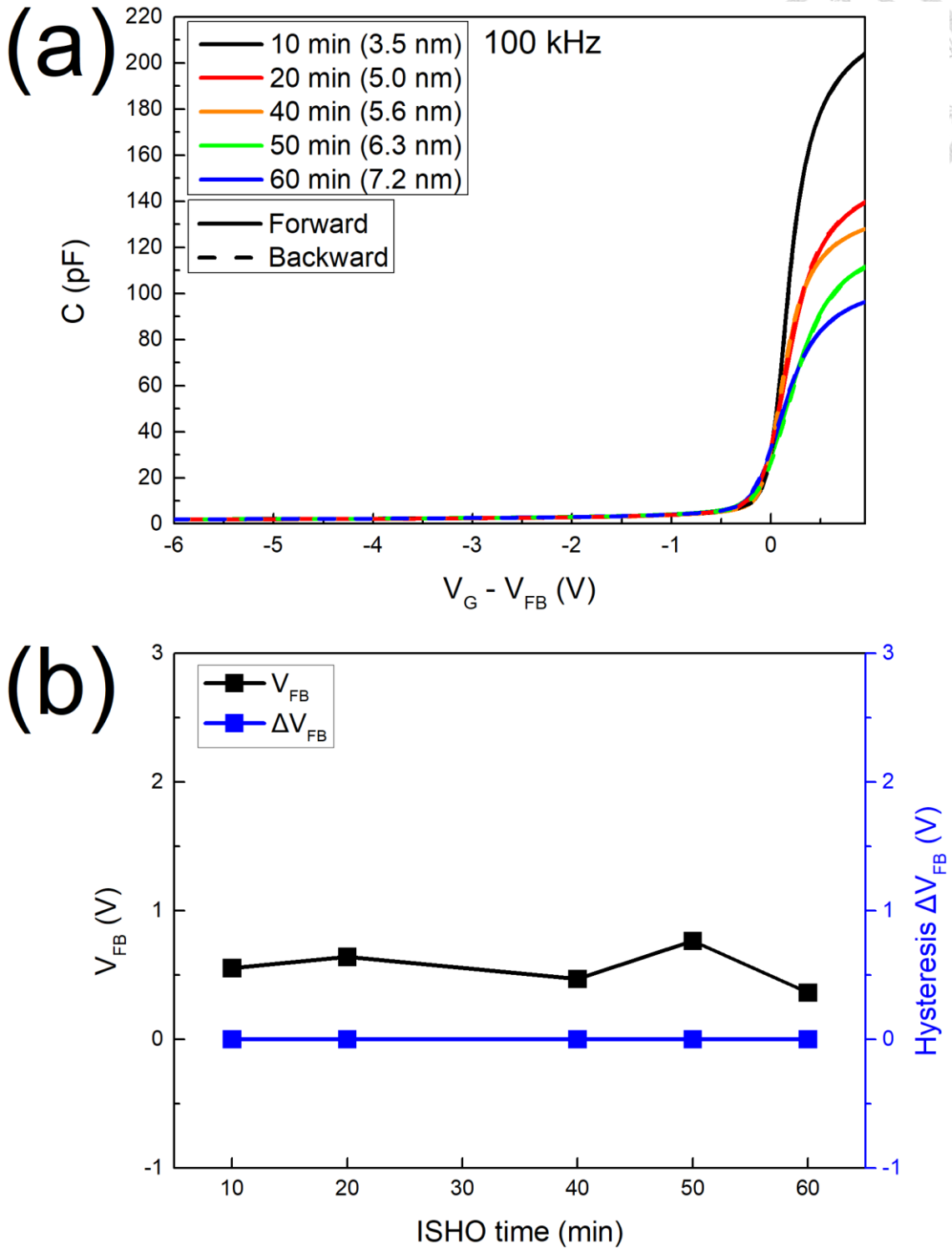

Fig. 2-4. (a) Normalized *C*-*V* characteristics relative to flat-band voltages at 100 kHz and (b) flat-band voltages and hysteresis flat-band shifts of samples with different ISHO times.

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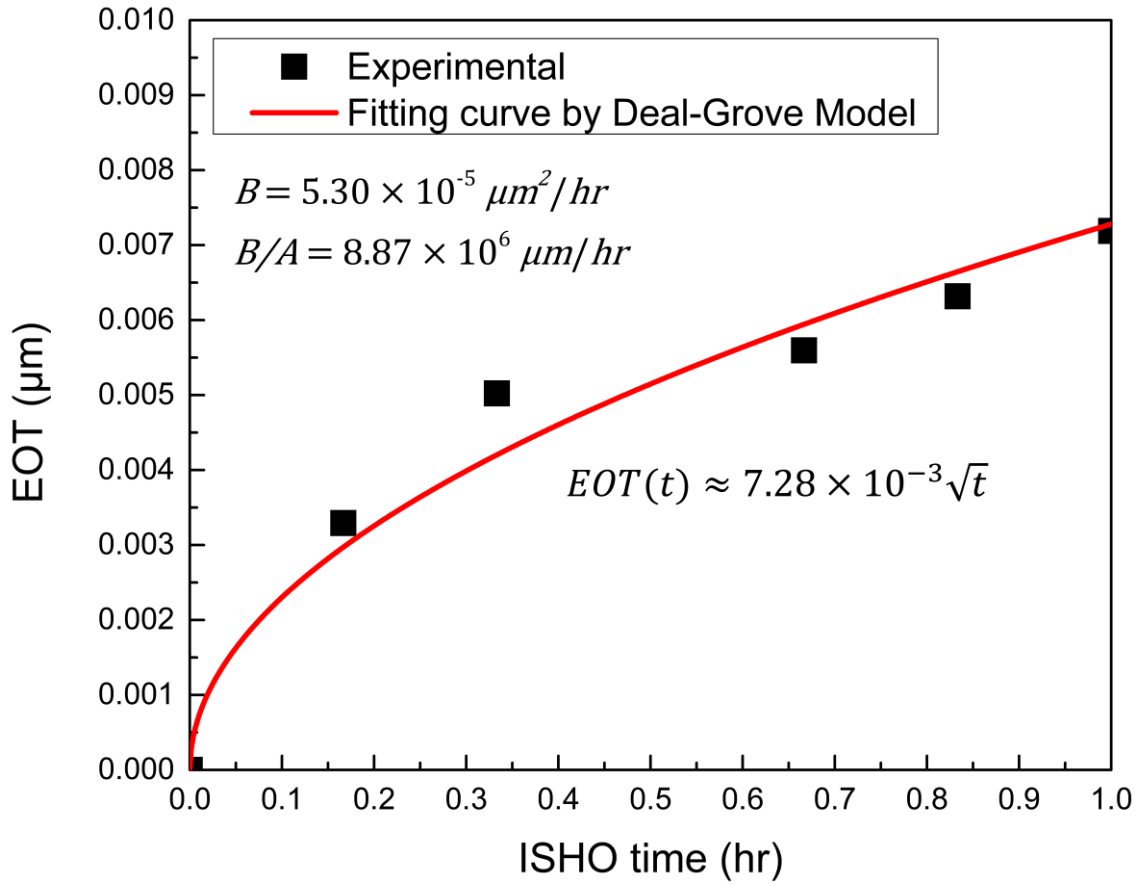

Fig. 2-5. EOT versus ISHO time with the fitting curve by the Deal-Grove model.

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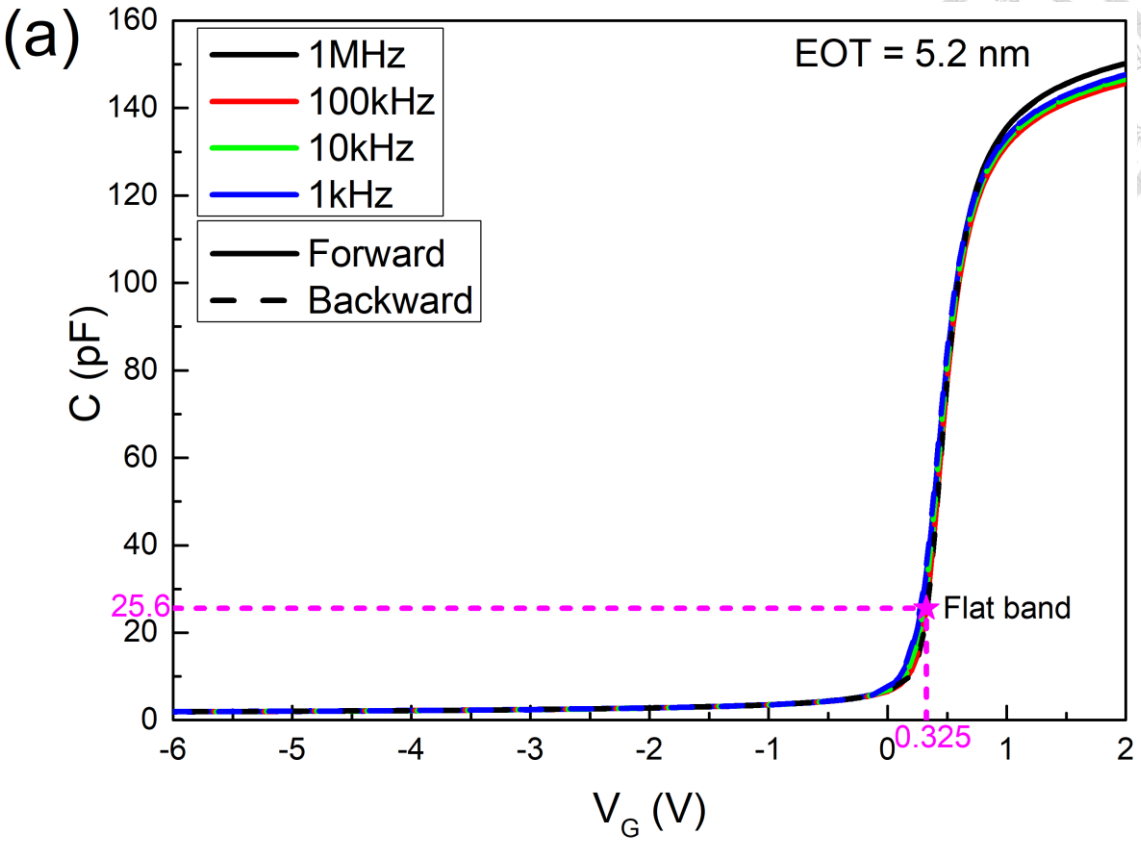

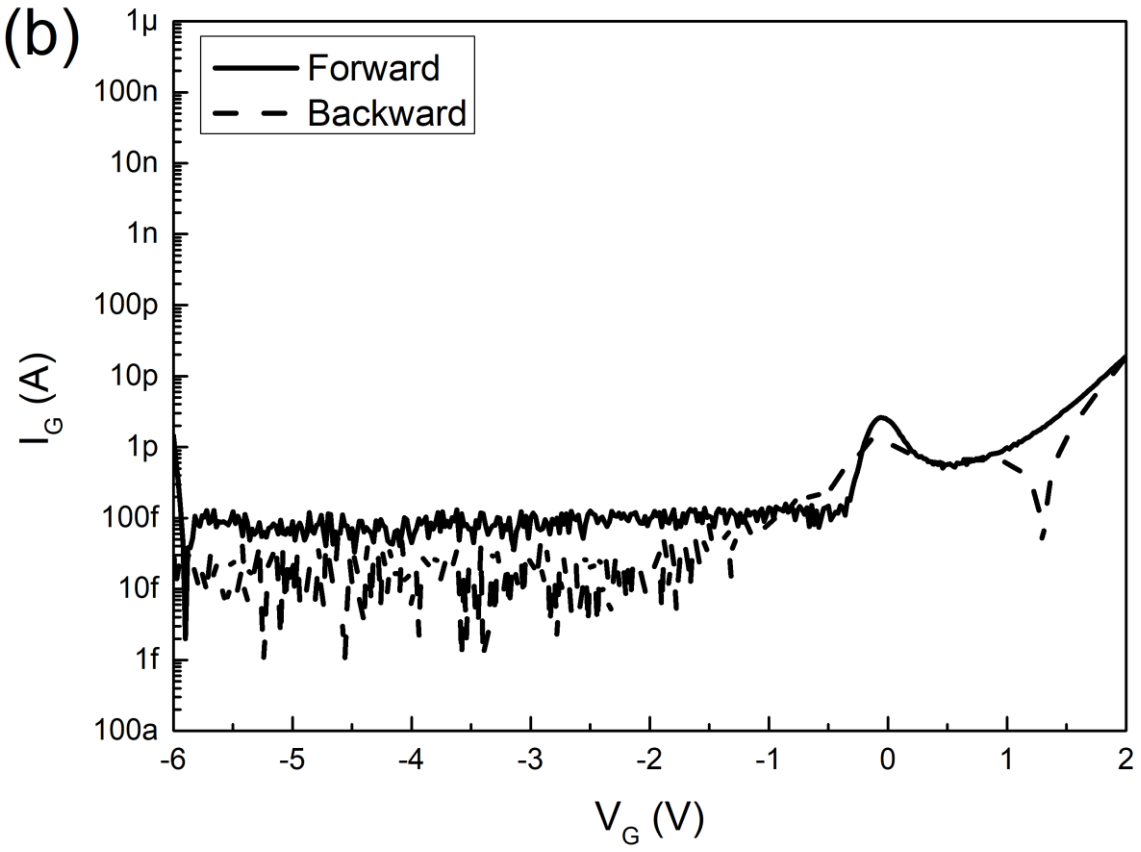

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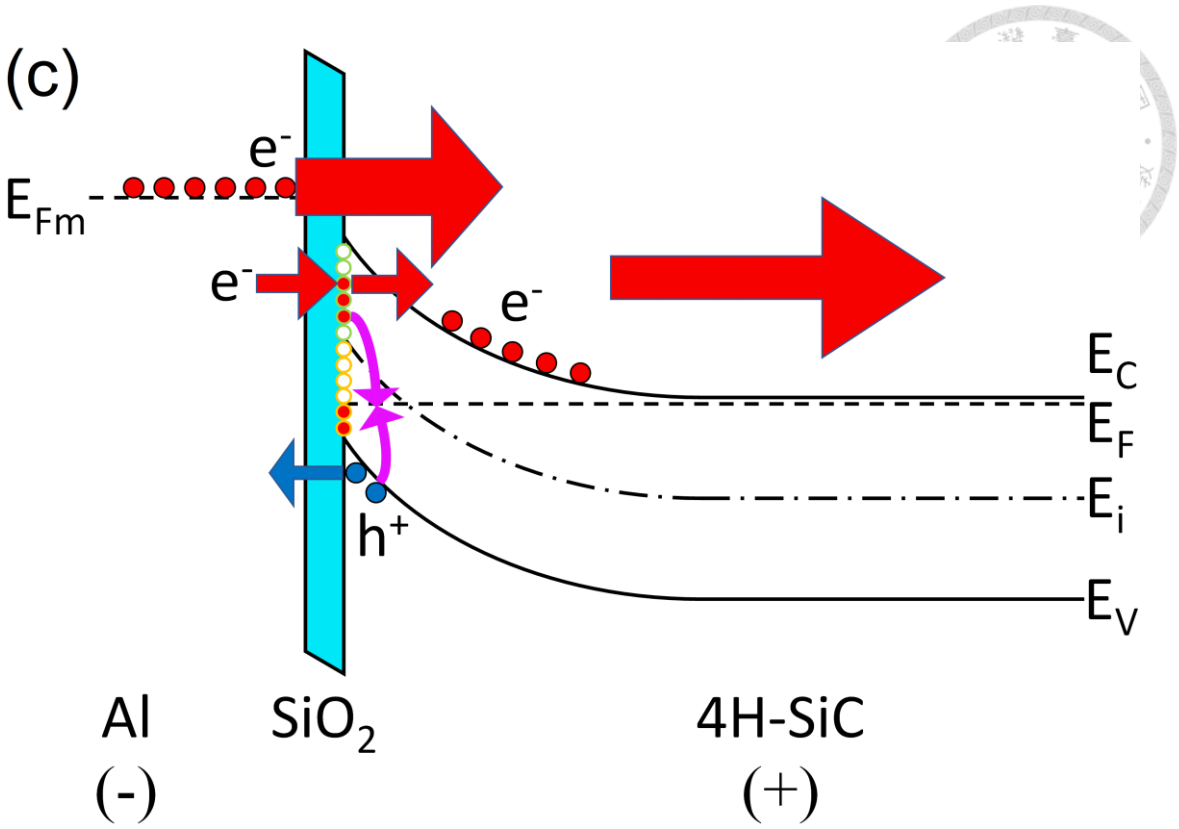

Fig. 2-6. (a) *C-V* and (b) *I-V* characteristics of an MIS device with EOT = 5.2 nm. The flat-band voltage was found to be 0.325 V. (c) Band diagram with interface trap states at reverse bias, explaining the mechanisms of the saturation current.

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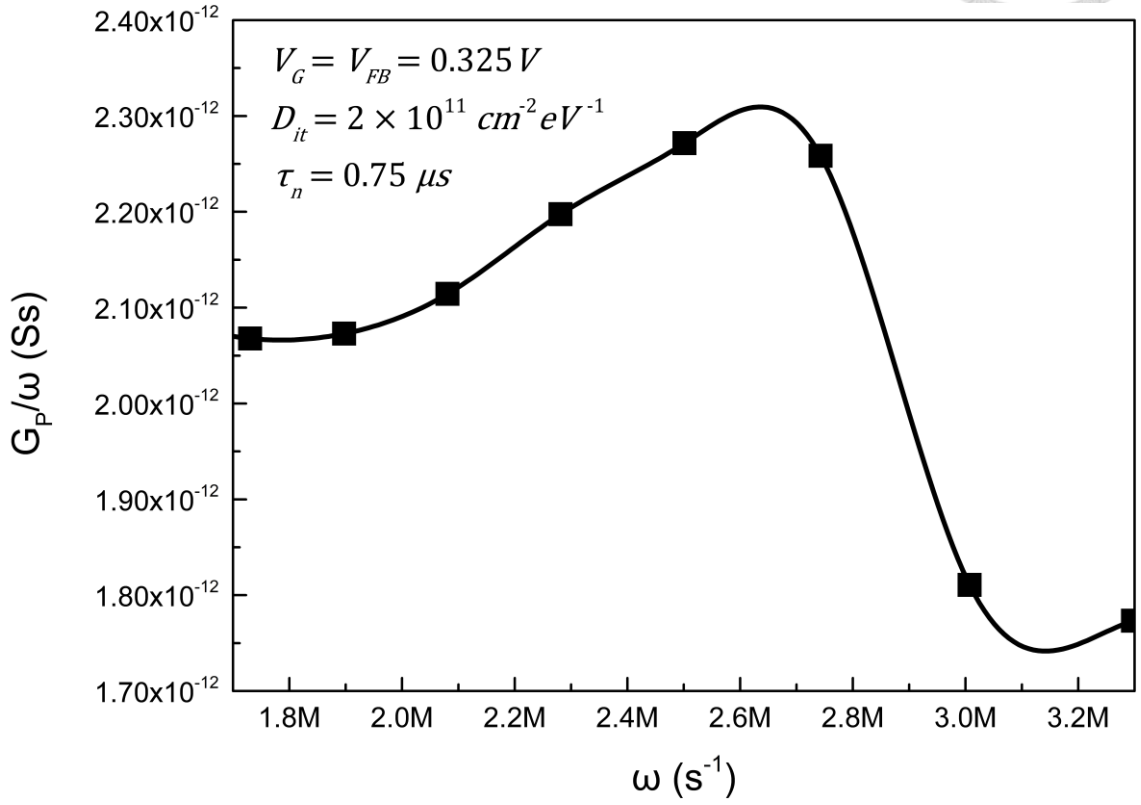

Fig. 2-7. Conductance method analyzed at the flat-band voltage. The interface trap density D_{it} and the electron carrier lifetime τ_n were evaluated.

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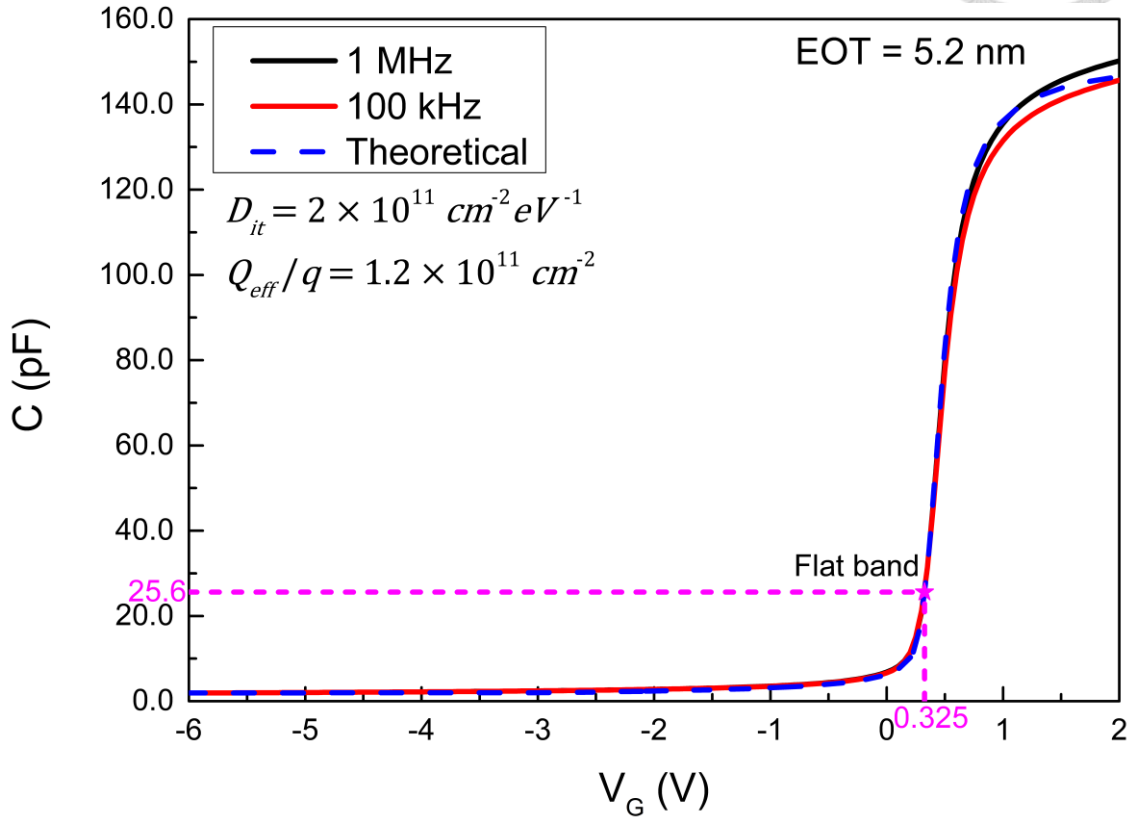

Fig. 2-8. *C-V* characteristics measured at 1 MHz and 100 kHz compared to the theoretical high-frequency *C-V* curves of uniform $D_{it} = 2 \times 10^{11}$ cm^{-2}eV^{-1} and $Q_{eff}/q = 1.2 \times 10^{11}$ cm^{-2} computed with MATLAB.

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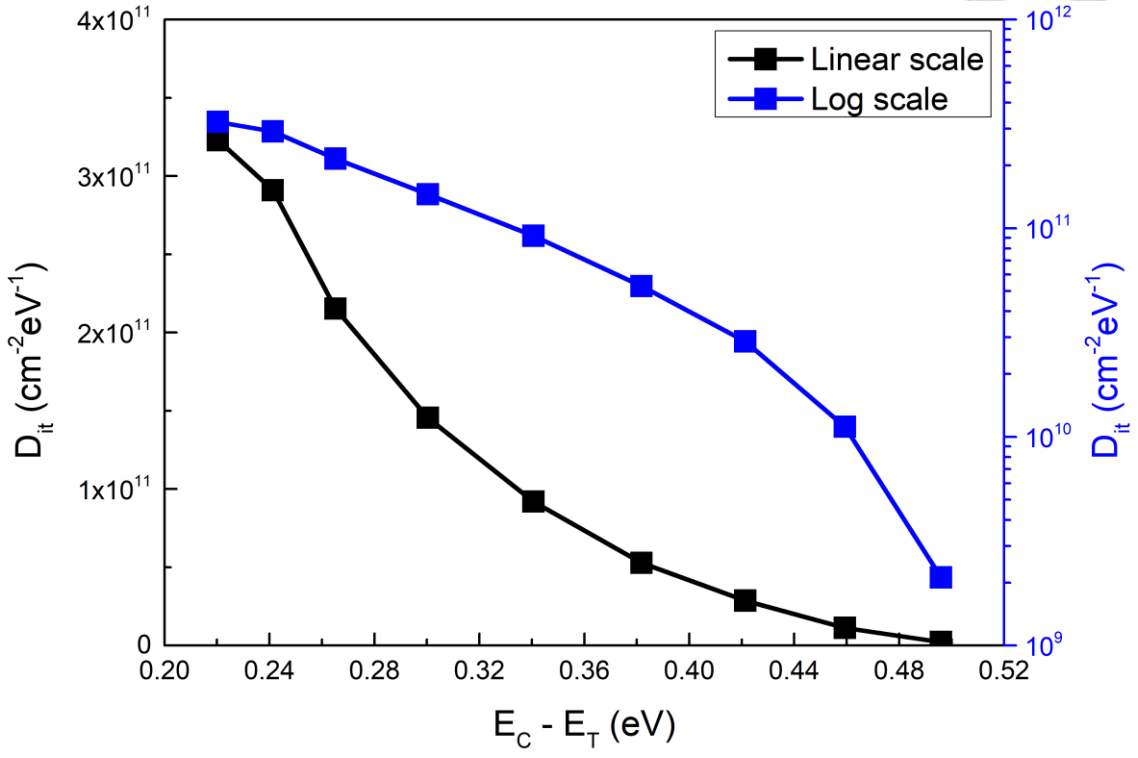

Fig. 2-9. Linear-scale and log-scale D_{it} along the energy levels in the depletion region evaluated by the high-low frequency capacitance method. C_{HF} and C_{LF} were measured at 1 MHz and 1 kHz, respectively.

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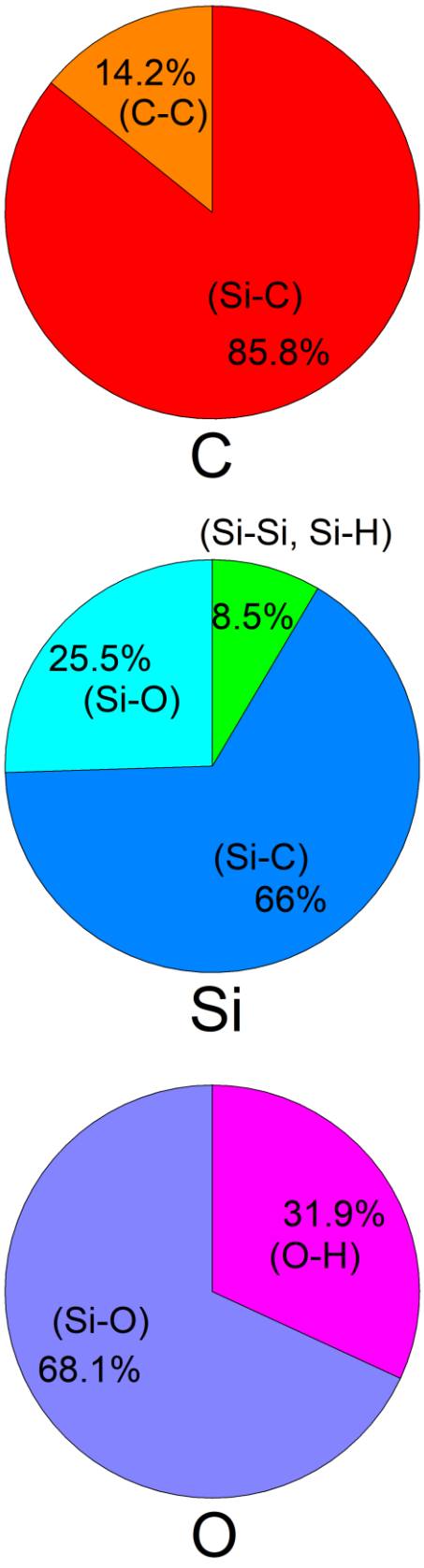

Fig. 2-10. Bonding composition for C, Si, and O at the SiO_2 / 4H-SiC interface analyzed by XPS.

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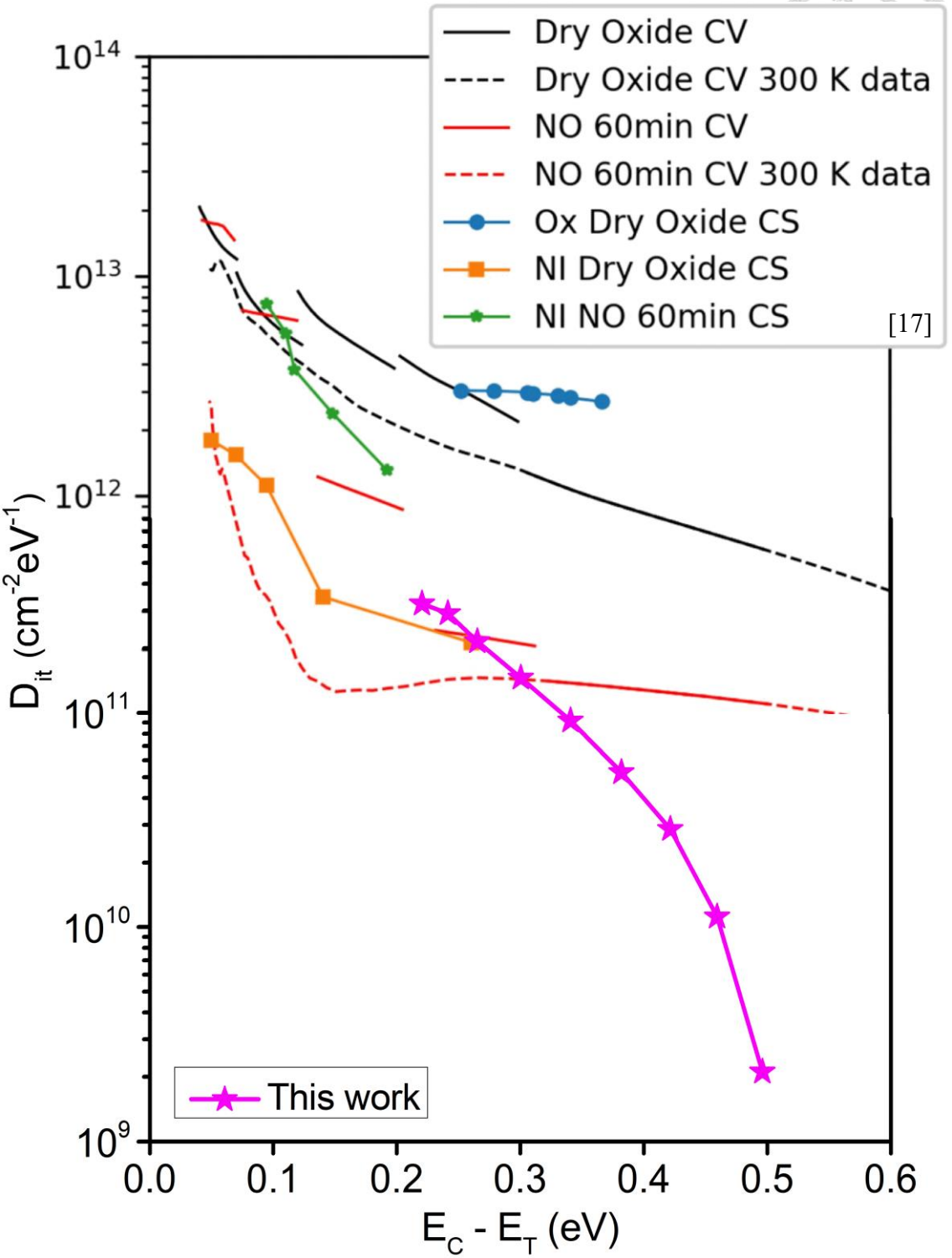

Fig. 2-11. Benchmark of the D_{it} at various energy levels near the conduction band of the 4H-SiC MIS device in comparison with those in [17], showing almost the lowest D_{it} for ISHO. The D_{it} obtained by the high-low frequency capacitance method and the conductance method are plotted as solid lines and marked lines, respectively.

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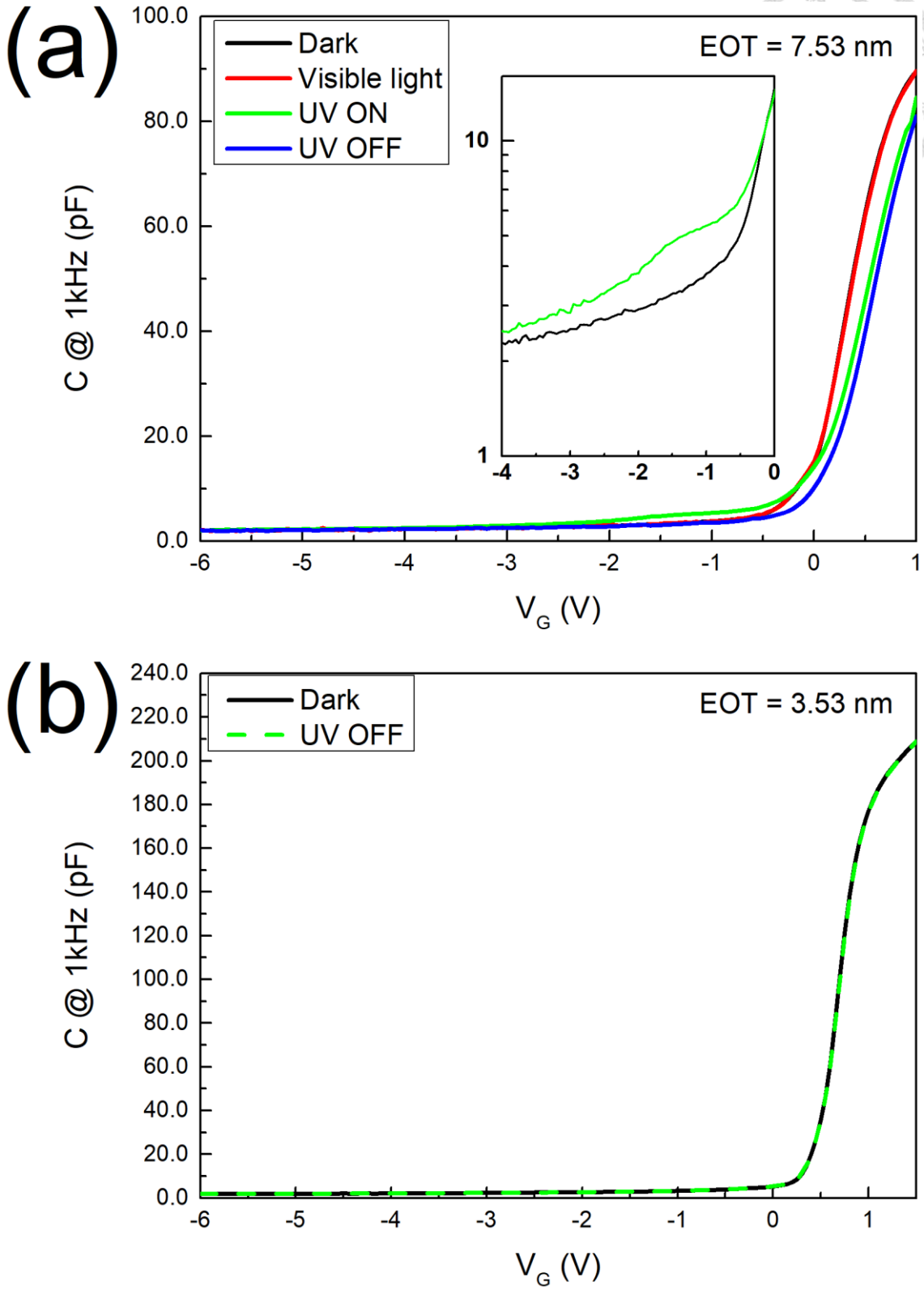

Fig. 2-12. *C-V* characteristics for the devices measured before and after sweeping from (a) -6 V to +1 V and (b) -6 V to 0 V under UV light at 1 kHz.

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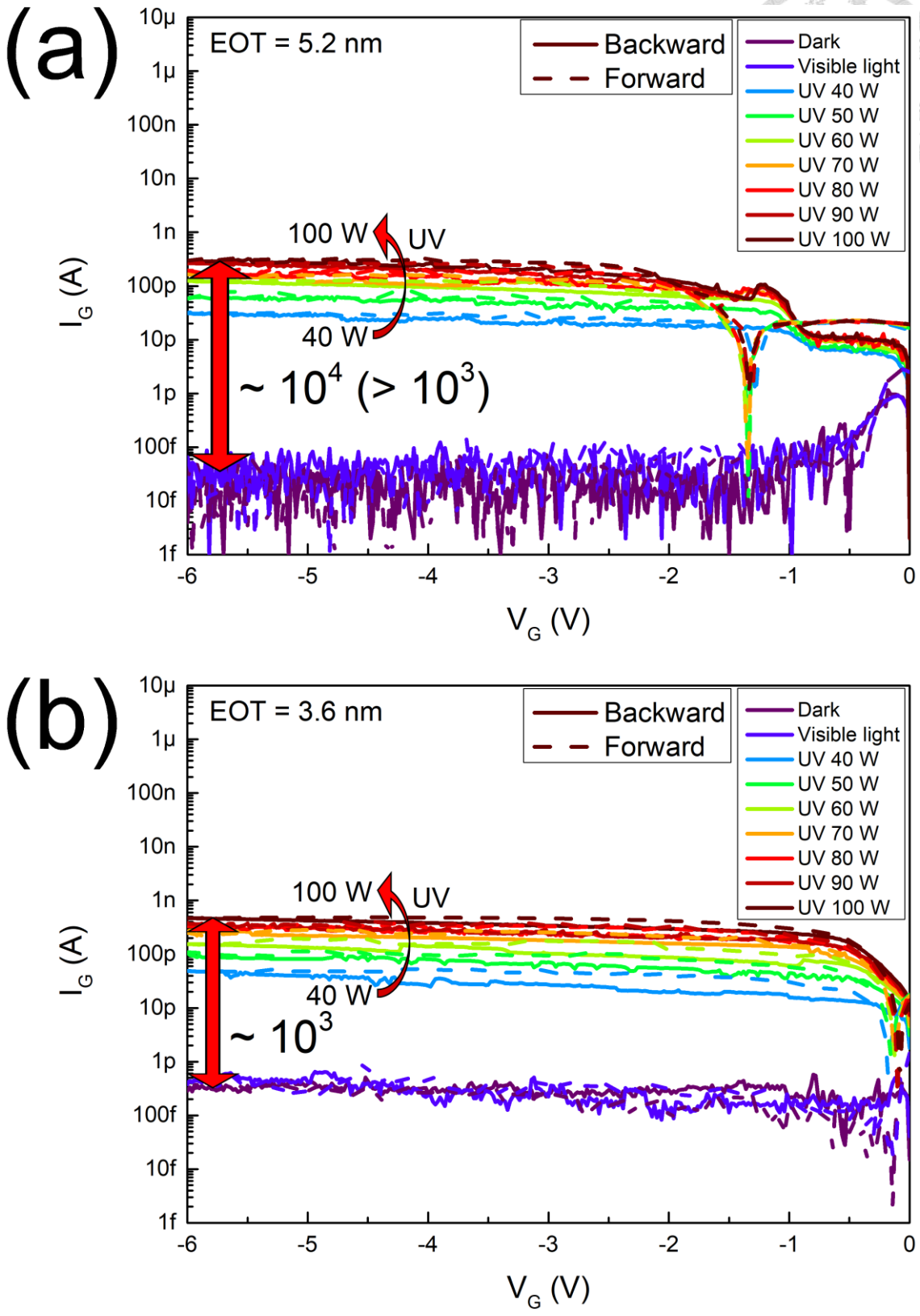

Fig. 2-13. *I-V* characteristics for the devices under varying UV intensities with EOTs of (a) 5.2 nm and (b) 3.6 nm.

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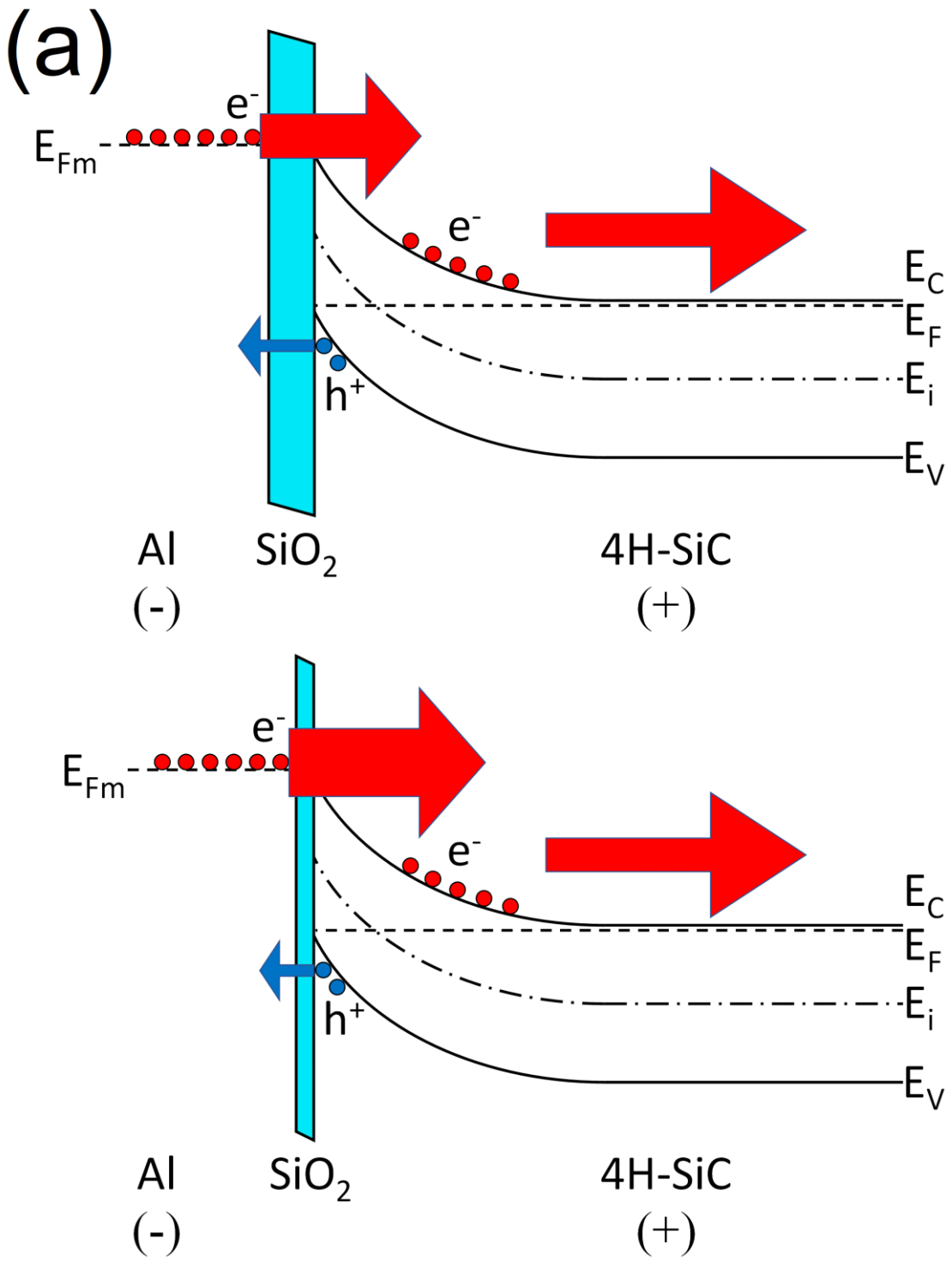

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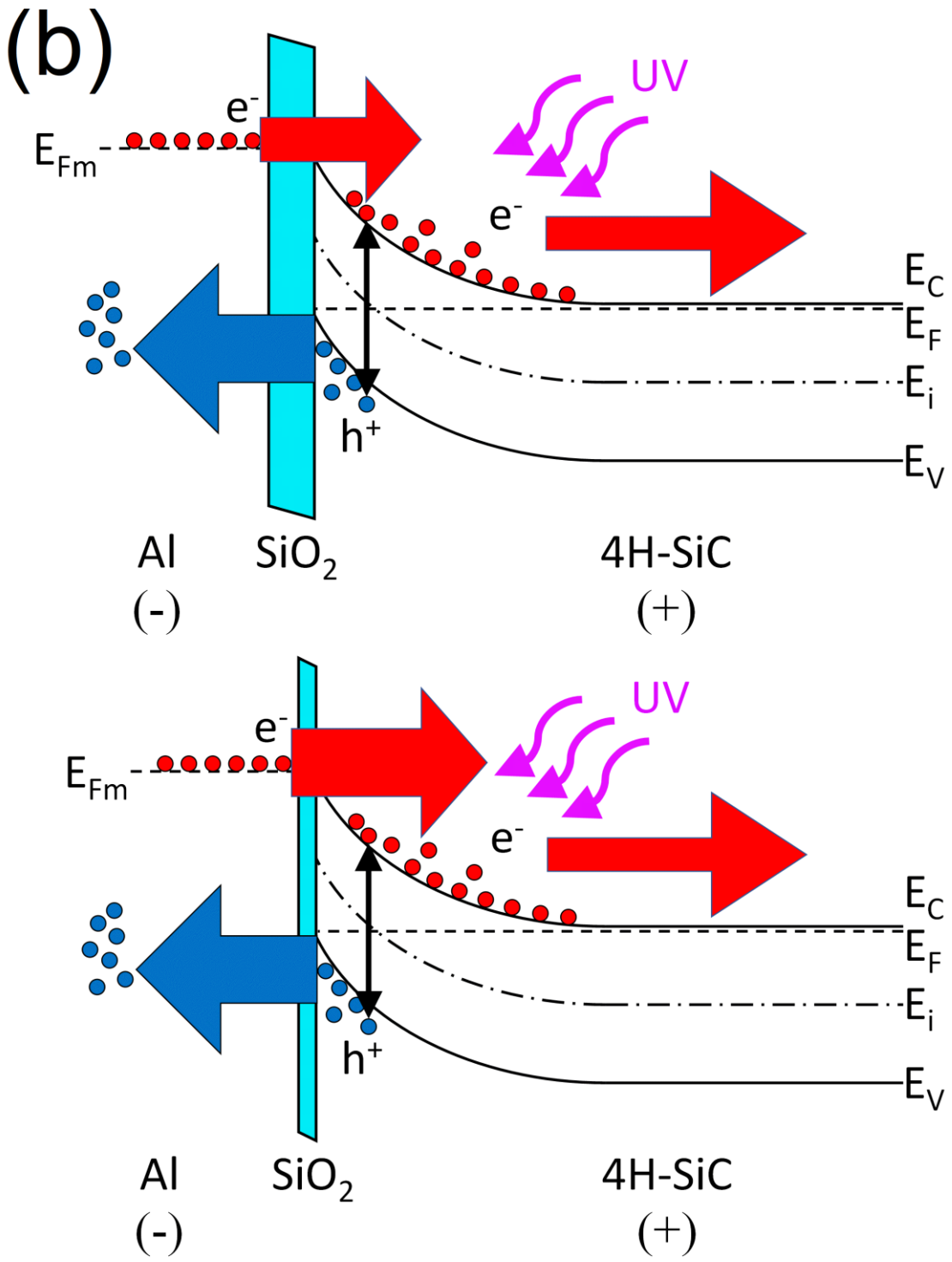

Fig. 2-14. Band diagrams illustrating the conditions of thicker and thinner oxide (a) in the dark and (b) under UV light illumination. The dark currents were dominated by the gate electrons injection, while the photocurrents were dominated by the minority UV-induced hole carriers.

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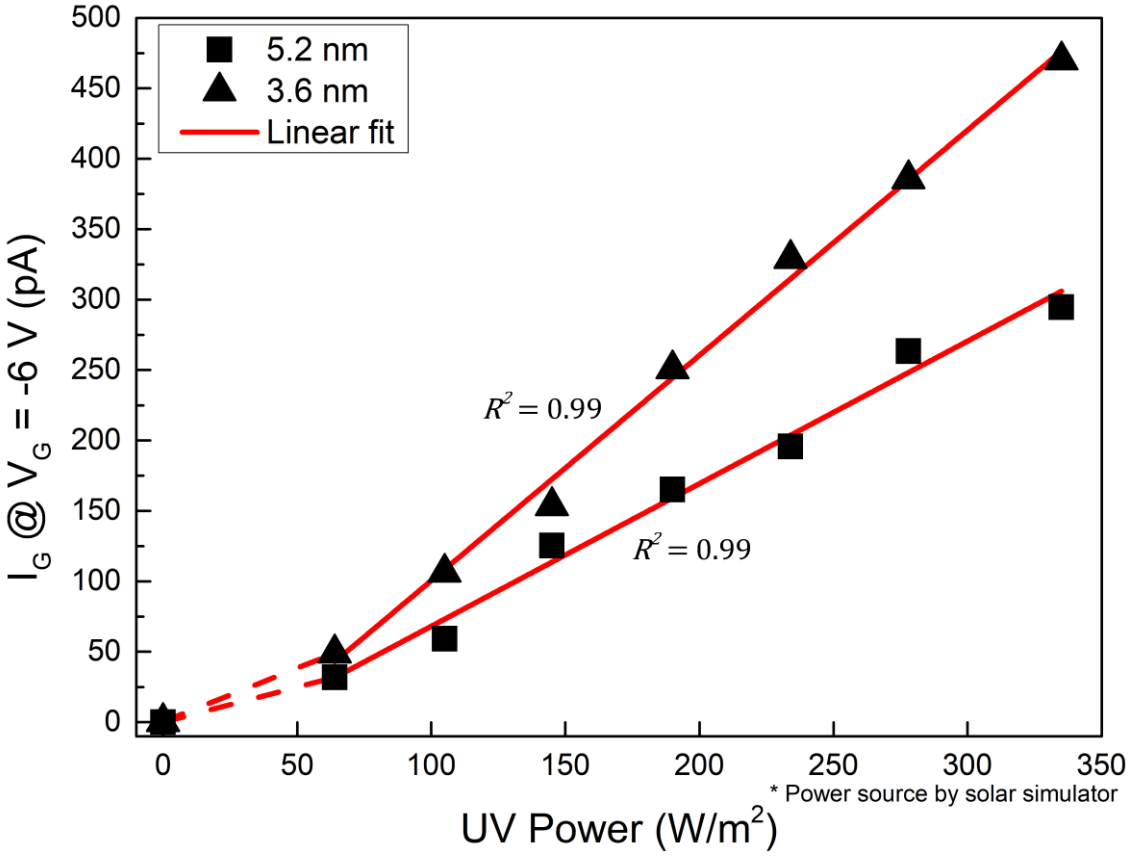

Fig. 2-15. Linear responsivity of the gate currents at -6 V for the samples with EOTs of 5.2 nm and 3.6 nm, both demonstrating a strong correlation between the gate current and the UV power ($R^2 = 0.99$).

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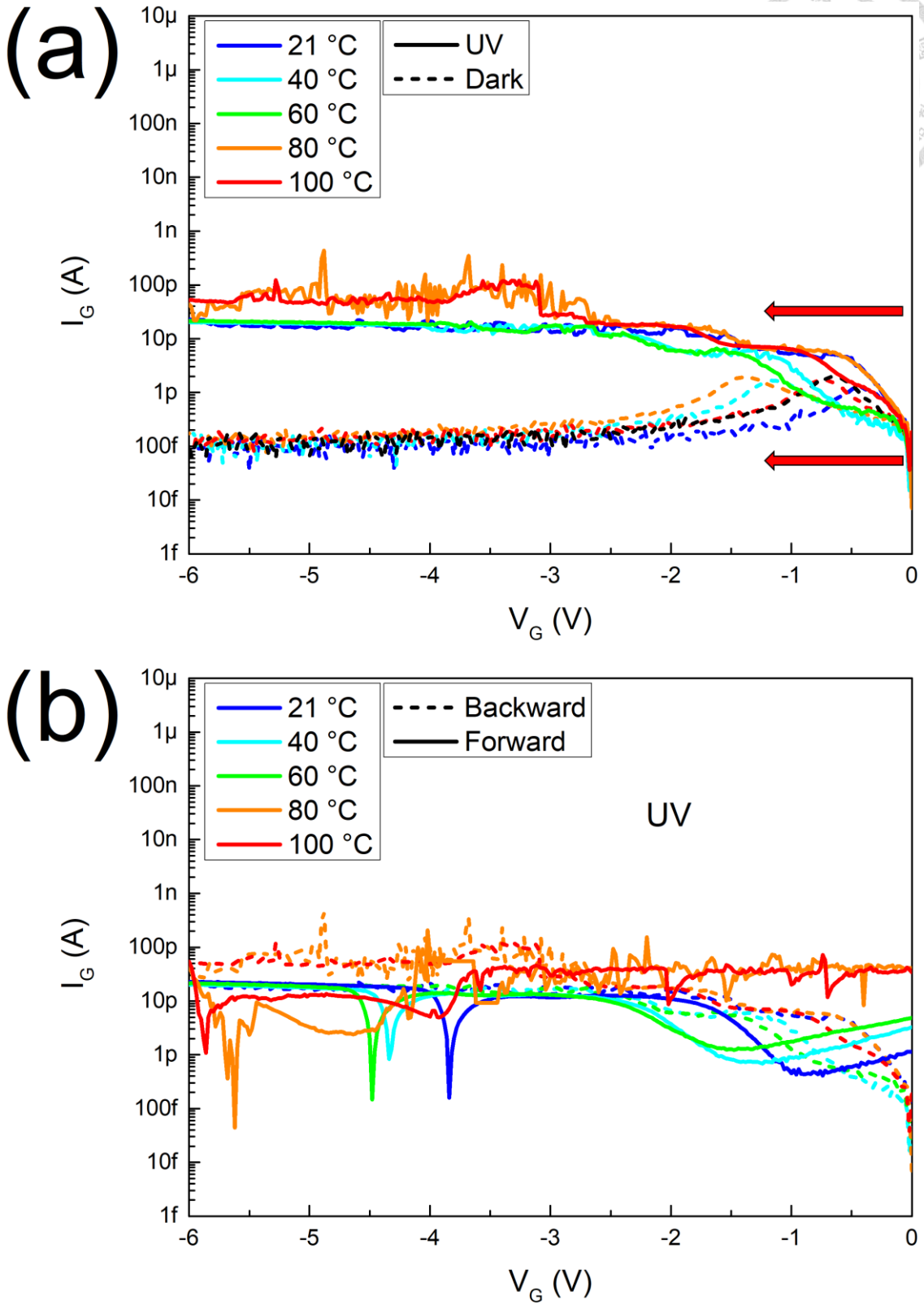

Fig. 2-16. *I-V* characteristics measured at room temperature (21 ˚C) to 100 ˚C by (a) sweeping from 0 V to -6 V in the dark and under the 60 W UV light and (b) sweeping backward and forward under UV illumination.

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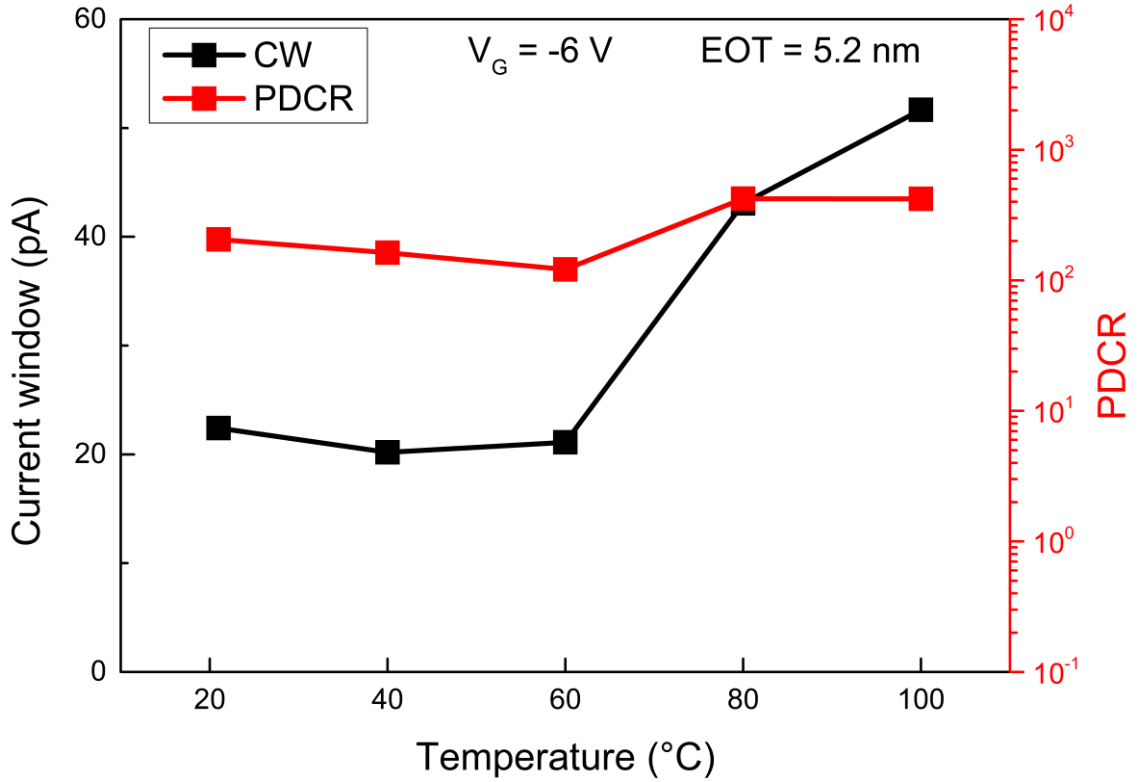

Fig. 2-17. Current window (CW) and the photo-to-dark current ratio (PDCR) at different temperatures, indicating the high-temperature tolerance capability of the MIS devices.

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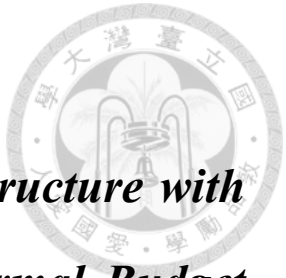

Chapter 3

Low Interface Trap Density 4H-SiC MIS Structure with Al_2O_3 Stacking on Thin SiO_2 for Low Thermal Budget Embedded Memory Applications

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3-1 Introduction

In the previous chapter, we introduced a novel way to grow a SiO_2 layer with a controllable thickness by the intermittent spray hydrated oxidation (ISHO) at a temperature lower than 1000 °C. The produced 4H-SiC MIS can also have useful applications such as UV sensors. In this chapter, we will demonstrate an alternative method to form oxide on the 4H-SiC wafer at room temperature. Previous works have shown that by anodic oxidation (ANO), a thin SiO_2 film could also be grown on a 4H-SiC substrate to fabricate a metal-insulator-semiconductor device, and even without the post-oxidation annealing (POA), it still exhibits good interface properties.

Additionally, as a popular high-κ dielectric material, Al_2O_3 can also be formed by the ANO technique to stack on the 4H-SiC MIS devices, so that the gate leakage current can be effectively suppressed without notably degrading the gate capacitance. This chapter will discuss the gate current behavior of the Al_2O_3-stacking 4H-SiC MIS devices w/ and w/o a SiO_2 layer. Furthermore, the interfacial traps at the border of Al_2O_3 / SiO_2 in the 4H-SiC MIS device can be operated as a charge-trapping layer, which could be integrated with 4H-SiC power ICs as embedded memory.

3-2 Experimental

The n-type nitrogen-doped wafers with epi-layers were used in this work, and the

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doping concentrations were the same as the wafers adopted in Chapter 2. Three kinds of device structures in this chapter: Al/Al_2O_3/Al_2O_3/SiO_2/4H-SiC, Al/Al_2O_3/SiO_2/4H-SiC, and Al/Al_2O_3/4H-SiC are denoted as M(AO)$_2$IS, M(AO)IS, and M(AO)S, respectively. The details of the fabrication processes are shown in Fig. 3-1(a), (b), and (c). Firstly, the Radio Cooperation of America (RCA) cleaning was conducted for all wafers to remove the particles and ions on their surfaces. Next, the wafers of M(AO)$_2$IS and M(AO)IS were deposited with 150 nm dummy Al on the backside as the electrode and immersed into a sink filled with deionized (DI) water, and connected to a DC power supply by alligator clips with a voltage of 50 V for 40 min. The schematic diagram of the ANO experimental setup is illustrated in Fig. 3-1(d). The backside dummy Al was etched after the ANO process was completed. Subsequently, Al thin films were deposited on the top of the wafers by thermal evaporation, followed by ANO. For M(AO)$_2$IS, two layers of Al of 15-nm thick were deposited, and after the deposition of the first and second layers, ANO was adopted with 15 V for 30 min and 20 V for 40 min, respectively. For M(AO)IS and M(AO)S, a 7-nm thick Al layer was deposited, followed by ANO with 20 V for 40 min. Note that there's no POA process in this work, and all the ANO processes were conducted at room temperature for the purpose of low thermal budget. Following, the 150 nm top gate Al was deposited on all the wafers, patterned by photolithography and wet etching. Finally, the buffered oxide etch (BOE) was used to remove the backside native oxide,

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followed by a 150 nm aluminum deposition as the back electrode. All the electrical characteristics data were measured by Agilent B1500A semiconductor device analyzer.

3-3 Results and Discussion

3-3-1 Material and Electrical Characterization of the Devices with $M(AO)_2IS$, M(AO)IS, and M(AO)S Structures

The device schematics of the three structures with $M(AO)_2IS$, M(AO)IS, and M(AO)S are shown in Fig. 3-2(a), (b), and (c), respectively. The radius of the Al gate is 85 μm for the three structures. The TEM image and the EDX mapping of an $M(AO)_2IS$ device are shown in Fig. 3-3 and Fig. 3-4, respectively. The TEM results indicated a thickness of about 29.7 nm for the Al_2O_3 layer and a thickness of about 0.4 nm for the SiO_2 layer. In addition, according to the EDX results shown in Fig. 3-4(a) and (b), the two layers of Al_2O_3 were almost uniform, with only a few localized areas where aluminum was not fully oxidized. Overall, the material analysis results suggest that the ANO technique is a promising low-cost method for fabricating aluminum oxide dielectric layers. From Fig. 3-4(c) and (d), we can also observe the uniformity of the SiO_2 / 4H-SiC interface with no carbon clustering phenomenon.

The interface trap density was extremely low with the thin SiO_2 interfacial layer formed by the ANO process at room temperature. Fig. 3-5(a) shows the *C-V*

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characteristics of the $M(AO)_2IS$ device with an EOT of 22.4 nm. By the high-low frequency capacitance method, the D_{it} at the flat band voltage was evaluated to be only 1×10^{11} $cm^{-2}eV^{-1}$. Additionally, although the SiO_2 layer was very thin, the gate leakage current could still be suppressed by the stacking of the Al_2O_3 high-κ layers while not notably degrading the gate capacitance which is a crucial factor for the capability of the gate's control over the channel. The gate current in the accumulation region (V_G = +3 V) was about 2 nA, and the saturation current at the reverse bias (V_G = -6 V) remained around only 1 pA, as the *I-V* curves shown in Fig. 3-5(b). To further examine the interface properties, the experimental data was compared to the theoretical data computed with MATLAB. The interface traps were assumed to be acceptor-type above the midgap, and donor-type below the midgap. The higher D_{it} would lead to a larger frequency dispersion. Hence, we define the frequency dispersion (FD) as

$$FD = \frac{C_{LF} - C_{HF}}{C_{HF}} \times 100\% \quad (3\text{-}1)$$

where C_{LF} and C_{HF} are the forward low-frequency (1kHz) and high-frequency (1MHz) capacitances, respectively. The experimental FD at the flat band voltage was about 10.14%. Fig. 3-6 illustrates the theoretical *C-V* curves with various D_{it} and their corresponding FD. The D_{it} distribution was assumed to be acceptor type and donor type above and below the midgap. Accordingly, by comparing the experimental and the theoretical data, the D_{it} of the $M(AO)_2IS$ sample at the flat band condition falls between

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1×10^{11} $cm^{-2}eV^{-1}$ and 2×10^{11} $cm^{-2}eV^{-1}$, which is closely aligned with the result obtained by the high-low frequency capacitance method. In contrast, the *C-V* characteristics of the M(AO)S device exhibited very large frequency dispersion, as shown in Fig. 3-7, which might originate from the border traps. The tremendous difference in the *C-V* characteristics indicates that the thin SiO_2 interfacial layer is indispensable for good interface properties.

3-3-2 Interface Property Analysis of Al_2O_3-stacking MIS Devices w/ & w/o SiO_2 Interfacial Layer By TCAD Simulation

In the previous section, we summarized the necessity of the thin SiO_2 interfacial layer by the analysis of the *C-V* characteristics. Now, we will compare the *I-V* characteristics of the Al_2O_3-stacking MIS devices w/ & w/o a SiO_2 interfacial layer, that is, the structures of M(AO)IS, and M(AO)S, as shown in Fig. 3-8. The gate current of the M(AO)IS device was significantly lower than that of the M(AO)S device at the reverse bias, while the gate current of the M(AO)IS device was much higher than that of the M(AO)S device in the accumulation region.

It is unintuitive that the M(AO)IS device had an additional SiO_2 layer but still possessed a higher forward leakage current. To further study this phenomenon, the Silvaco TCAD simulation was adopted. Fig. 3-9(a) and (b) illustrate the band diagrams

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at -6 V for the M(AO)IS and the M(AO)S devices respectively. The D_{it} was set as 1×10^{11} $cm^{-2}eV^{-1}$ for the M(AO)IS structure and 2×10^{11} $cm^{-2}eV^{-1}$ for the M(AO)S structure. Note that the orange line in Fig. 3-9(a) denotes the border of Al_2O_3 and SiO_2. The biggest difference between the band diagrams of these two structures was the position of the hole quasi-Fermi level (QFL). The hole QFL of the M(AO)S structure was further away from the top of the valence band than that of the M(AO)IS structure, which means the M(AO)S structure had fewer holes. This was because more interface traps could enhance the trap-assisted tunneling (TAT) effect and also increase the recombination rate of the holes in the valance band recombining with the electrons in the conduction band and at the interface traps for the M(AO)S structure, consequently reducing the hole concentration. Additionally, the band diagrams of a bias at +2 V for the M(AO)IS and the M(AO)S structures are depicted in Fig. 3-9(c) and (d), respectively. The electron QFL was above the bottom of the conduction band at the surface for the M(AO)IS structure, indicating the accumulation of considerable electrons. On the contrary, although the oxide band was bending downward for the M(AO)S structure, the surface band bending (ψ_s) was upward even at +2 V. This special phenomenon might stem from the electrons trapped at the interface states below the electron QFL, and hence repulsed the electrons in the conduction band. Furthermore, in order to investigate the *I-V* characteristics of the M(AO)IS and the M(AO)S devices, the distribution of the electron concentration was

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analyzed. Fig. 3-10(a) and (b) show the 2-D distribution of the electron concentration for the M(AO)IS and the M(AO)S structures at -6 V. The depth profile along the cut line at the position of 80 μm is shown in Fig. 3-10(c). The electron concentration near the surface was only about 10^{-18} cm^{-3} for the M(AO)IS structure, while it could reach 10^{-13} cm^{-3} to 10^{-12} cm^{-3} for the M(AO)S structure, which consequently explains the fact that the current of the M(AO)S device was higher than the current of the M(AO)IS device. The 2-D distribution of the electron concentration of the M(AO)IS and the M(AO)S structures at +2 V are shown in Fig. 3-11(a) and (b) respectively, and the depth profile of the electron concentration is shown in Fig. 3-11(c). Note that the red curves in the 2-D distribution graphs are the depletion edges. Even though the gate bias was at +2 V, the M(AO)S structure still presented a wide depletion region with 0.2 μm depth under the gate, while the M(AO)IS structure did not. The electron concentration near the surface could reach up to 2×10^{19} cm^{-3} for the M(AO)IS structure; on the contrary, it was much lower for the M(AO)S structure with only around 10^{10} cm^{-3}. These simulation results illustrated the reason why the gate current of the M(AO)IS device would be higher than that of the M(AO)S device at +2 V.

Overall, if the lower reverse current is desired for an Al_2O_3-stacking MIS device, the SiO_2 interfacial layer is necessary. Nonetheless, the issue of the higher gate leakage in the accumulation region should be resolved. A possible solution is to stack one more layer of

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Al_2O_3 just like the $M(AO)_2IS$ as the device demonstrated in section 3-3-1. Since there might be some leakage paths such as a few localized incomplete-oxidized aluminum areas exist in the Al_2O_3 layers, an additional Al_2O_3 layer can effectively block the leakage paths so that the leakage current in the accumulation region can be reduced.

3-3-3 Investigation of Memory Applications

In addition to serving as the high-k dielectric layers to suppress the gate leakage without degrading the gate capacitance, the Al_2O_3 layer can also store charges in the interfacial traps at the border of Al_2O_3 / SiO_2 in the 4H-SiC MIS devices, making it suitable for memory applications. In section 3-3-1, the $M(AO)_2IS$ device exhibited a hysteresis phenomenon in the *C-V* characteristics. Particularly, the ratio of the capacitances in the forward and the backward *C-V* curves of 100 kHz at +2 V could reach about 4x, as shown in Fig. 3-12(a). In view of this, the $M(AO)_2IS$ device could be manipulated by the operation cycle as depicted in Fig. 3-12(a). Firstly, to write the status '0', a stress at -3 V was applied to the device for detrapping of the electrons, and then the capacitance was read at +2 V. And to write the status '1', the device was applied by a voltage of +3 V to trap the electrons, followed by reading again at +2 V. The endurance of the device was tested by operating for 100 cycles, and the results are shown in Fig. 3-12(b). It took 20 cycles to warm up the device, and after that, the capacitances of the state

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‘0’ and the state ‘1’ remained stable at about 7 pF and 20 pF, respectively. These excellent results indicate that the Al_2O_3-stacking 4H-SiC MIS devices have the potential for memory applications and could be integrated into power ICs on a 4H-SiC substrate as the embedded memory.

Besides the memory applications, the charge trapping in the Al_2O_3-stacking 4H-SiC MIS devices might also be able to control the threshold voltage (V_t), and thus, the devices could become V_t-controllable transistors.

3-4 Summary

This chapter explores an alternative method for fabricating metal-insulator-semiconductor (MIS) devices on 4H-SiC substrates, focusing on oxide formation through anodic oxidation (ANO) at room temperature. Through material and electrical characterization of MIS devices with different structures, including $M(AO)_2IS$, M(AO)IS, and M(AO)S, we observe uniform oxide layers and interface properties critical for device performance. Our findings reveal extremely low interface trap density of about only 1×10^{11} $cm^{-2}eV^{-1}$ at the flat band voltage and suppressed gate leakage current in devices with thin SiO_2 interfacial layers, validated through experimental and theoretical data. Additionally, TCAD simulation provides insights into interface properties and current characteristics of Al_2O_3-stacking MIS devices w/ & w/o the SiO_2 interfacial layers,

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emphasizing the necessity of SiO_2 for suppressing leakage currents and improving device performance. Furthermore, this study explores the potential of Al_2O_3-stacking MIS devices for memory applications, demonstrating hysteresis in the *C-V* characteristics and stability in the endurance test and suggesting their suitability for integration with 4H-SiC power ICs as embedded memory.

doi:10.6342/NTU202401607

(a)

- Radio Corporation of America (RCA) cleaning
- Deposit dummy backside Al
- ANO (50V, 40 min) in DI water to grow SiO_2
- Wet etch dummy backside Al
- Deposit 15 nm top Al thin film
- ANO (15V, 30 min) in DI water
- Deposit 15 nm top Al thin film
- ANO (20V, 40 min) in DI water

$(AO)_2$

- Deposit Al as the top electrode
- Photolithography to define patterns
- Wet etch Al
- Remove photoresist
- Buffer oxide etch (BOE) to remove native oxide
- Deposit Al as the backside electrode

(b)

- Radio Corporation of America (RCA) cleaning
- Deposit dummy backside Al
- ANO (50V, 40 min) in DI water to grow SiO_2
- Wet etch dummy backside Al
- Deposit 7 nm top Al thin film
- ANO (20V, 40min) in DI water

(AO)

- Deposit Al as the top electrode
- Photolithography to define patterns
- Wet etch Al
- Remove photoresist
- Buffer oxide etch (BOE) to remove native oxide
- Deposit Al as the backside electrode

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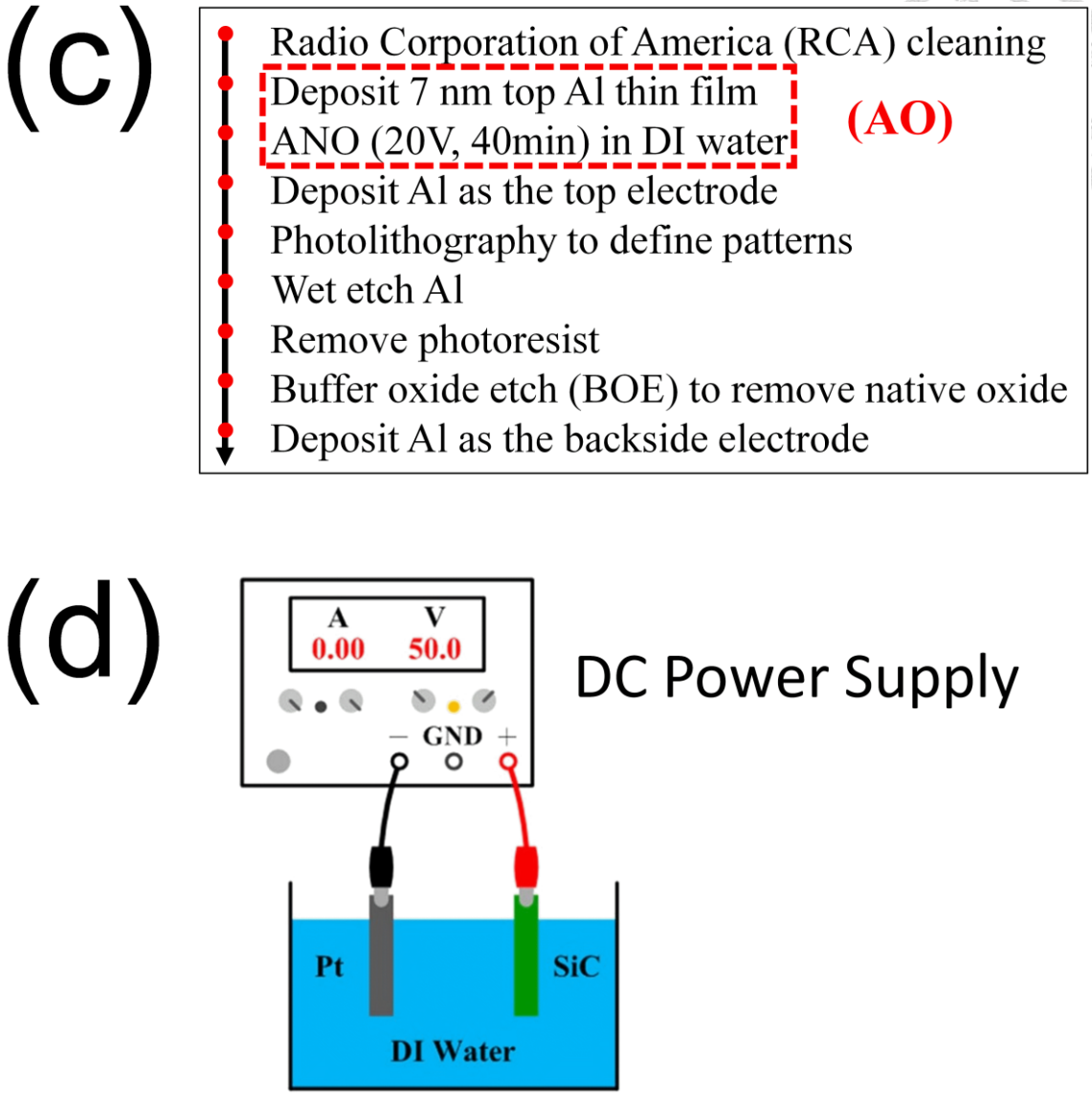

Fig. 3-1. Fabrication process flows for the devices with the structures of (a) $M(AO)_2IS$, (b) M(AO)IS, and (c) M(AO)S. (d) Schematic diagram of the anodic oxidation (ANO) experimental setup with a DC power supply and DI water.

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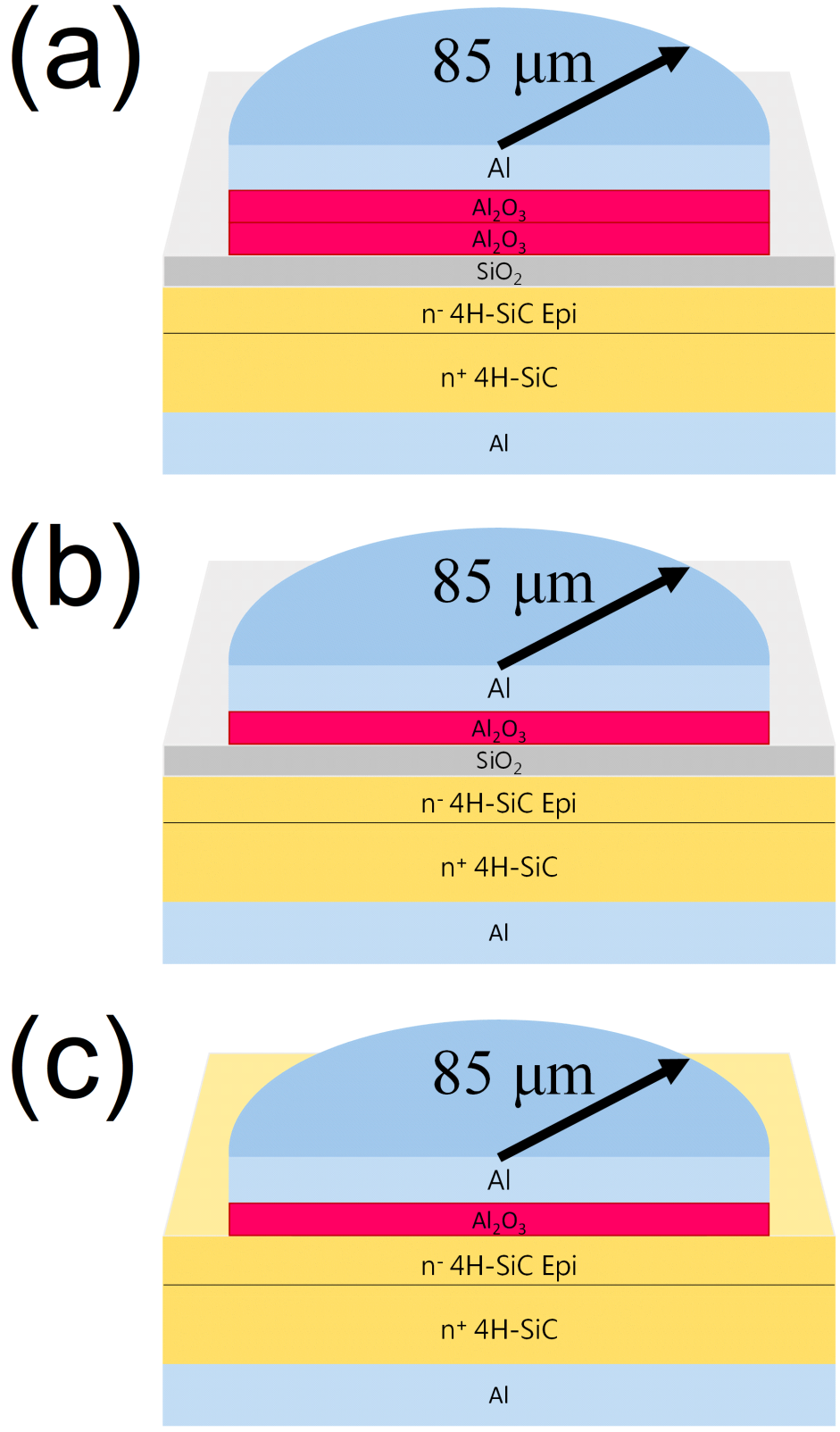

Fig. 3-2. Device schematics of the three structures of $M(AO)_2IS$, (b) M(AO)IS, and (c) M(AO)S.

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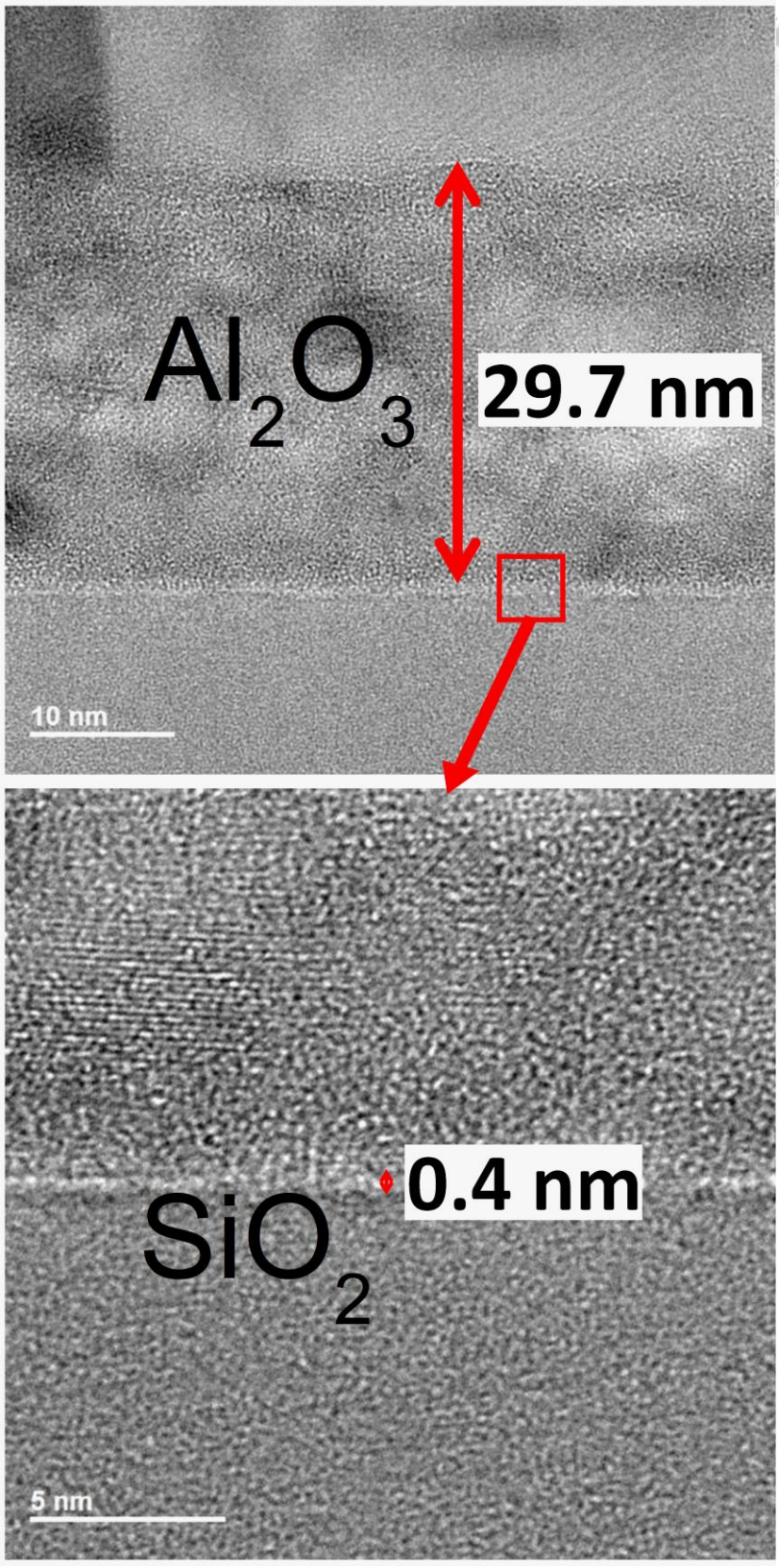

Fig. 3-3. TEM image of an $M(AO)_2IS$ device, showing 29.7-nm thick Al_2O_3 and 0.4-nm thick SiO_2.

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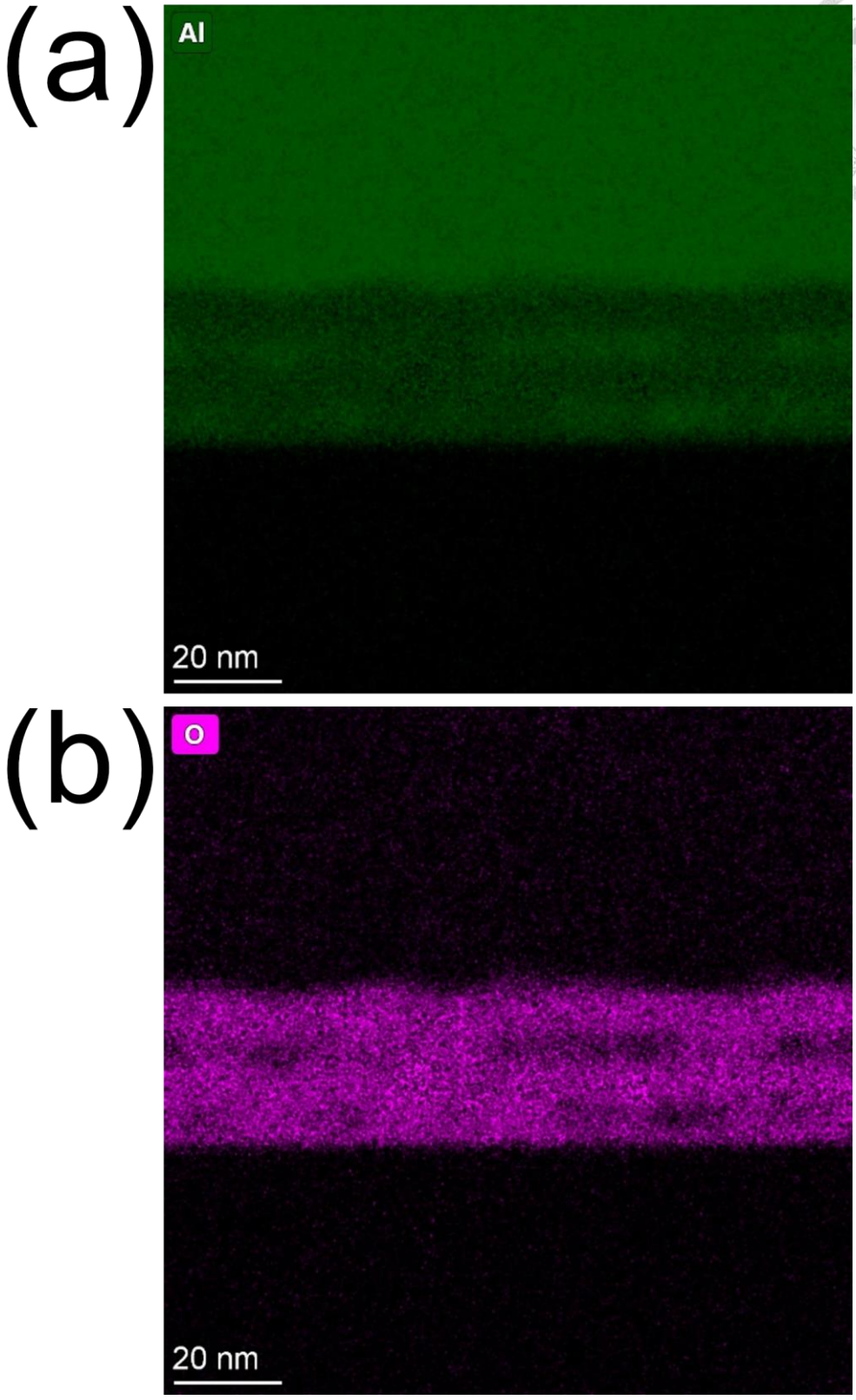

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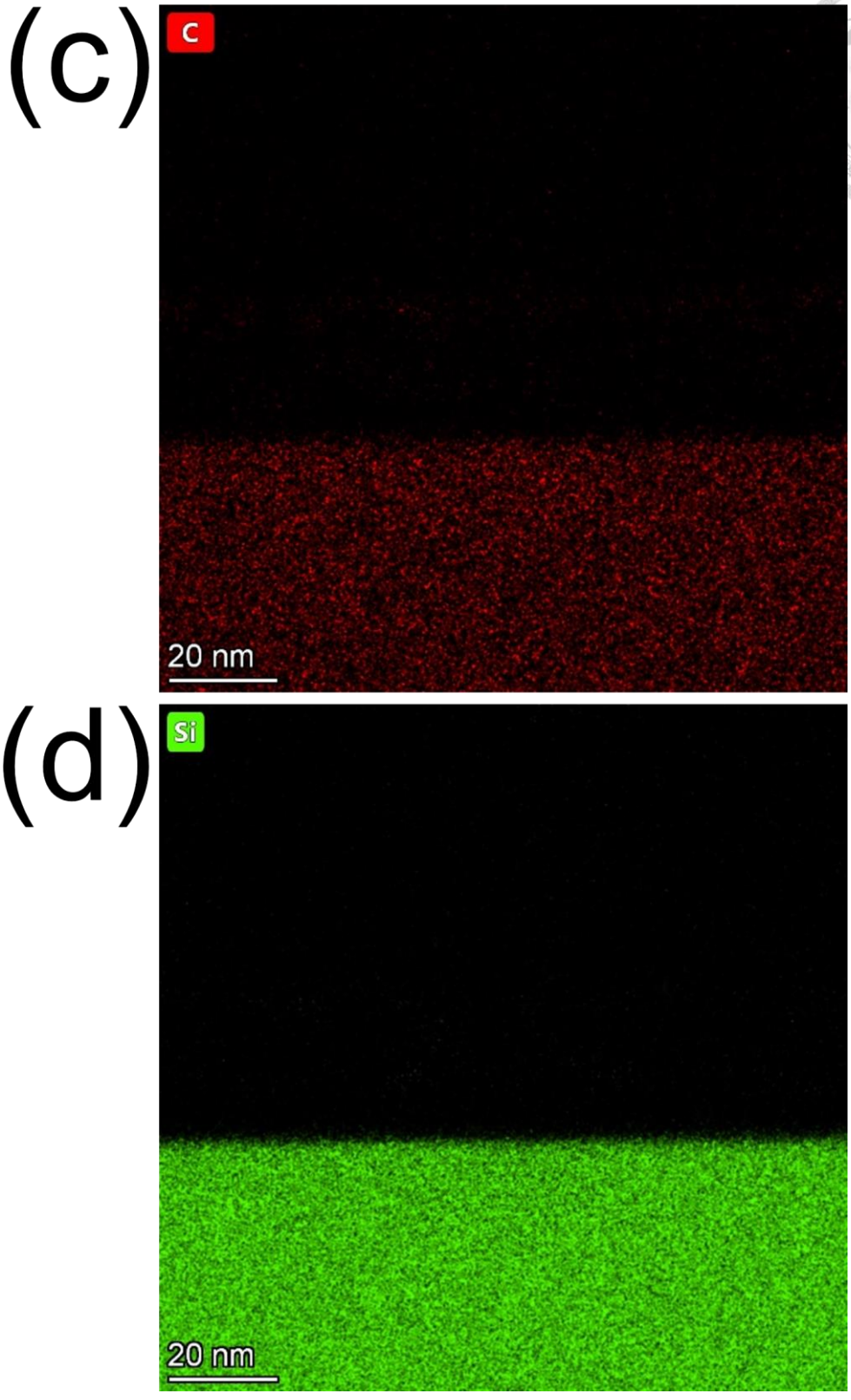

Fig. 3-4. EDX mapping for the elements of (a) Al, (b) O, (c) C, and (d) Si, in an $M(AO)_2IS$ device, exhibiting almost uniform Al_2O_3 layers and the SiO_2 / 4H-SiC interface without carbon clustering phenomenon.

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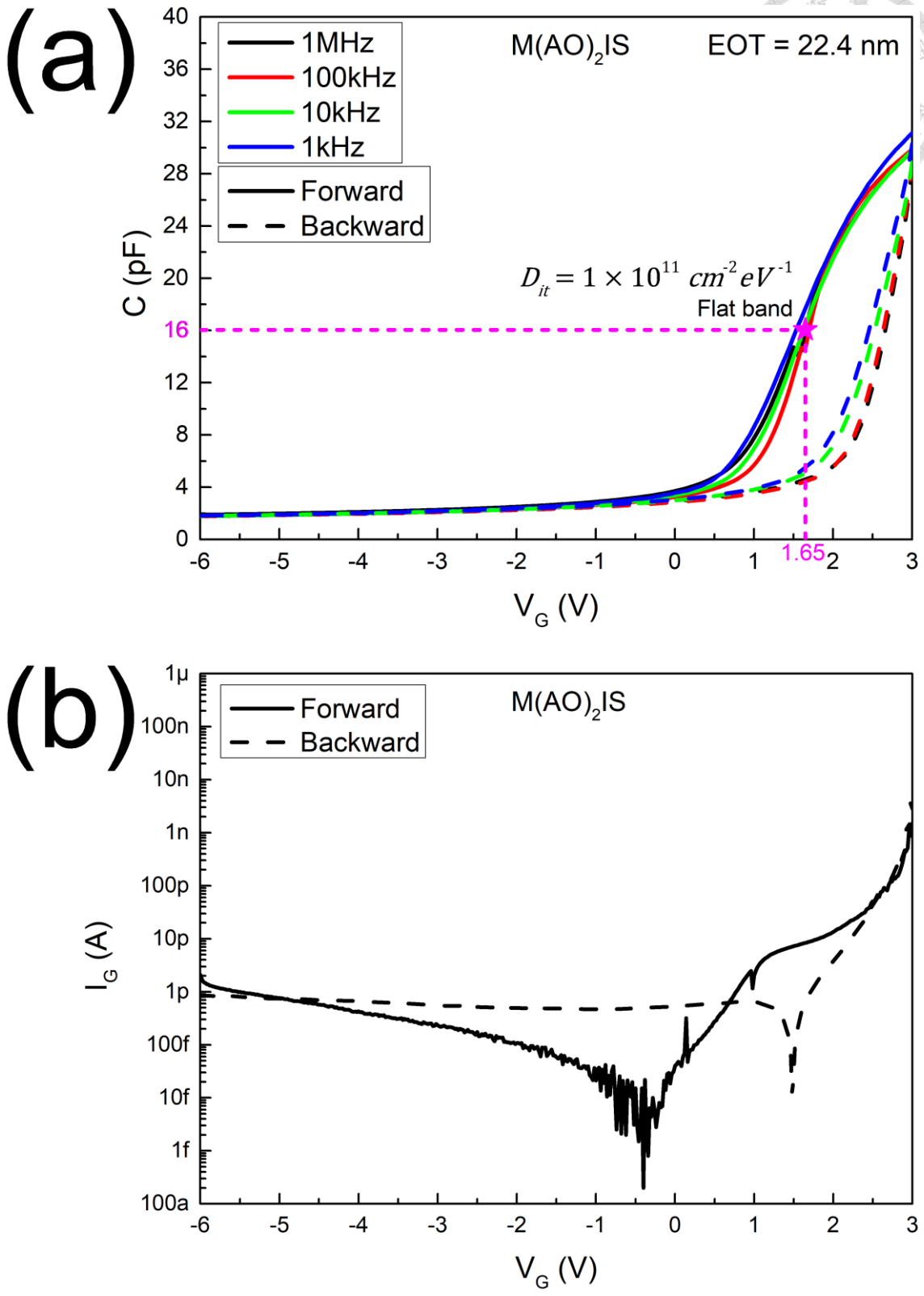

Fig. 3-5. (a) *C-V* and (b) *I-V* characteristics of an $M(AO)_2IS$ device with EOT = 22.4 nm. The flat-band voltage was 1.65 V, and the D_{it} was evaluated to be 1×10^{11} $cm^{-2}eV^{-1}$ by the high-low frequency capacitance method.

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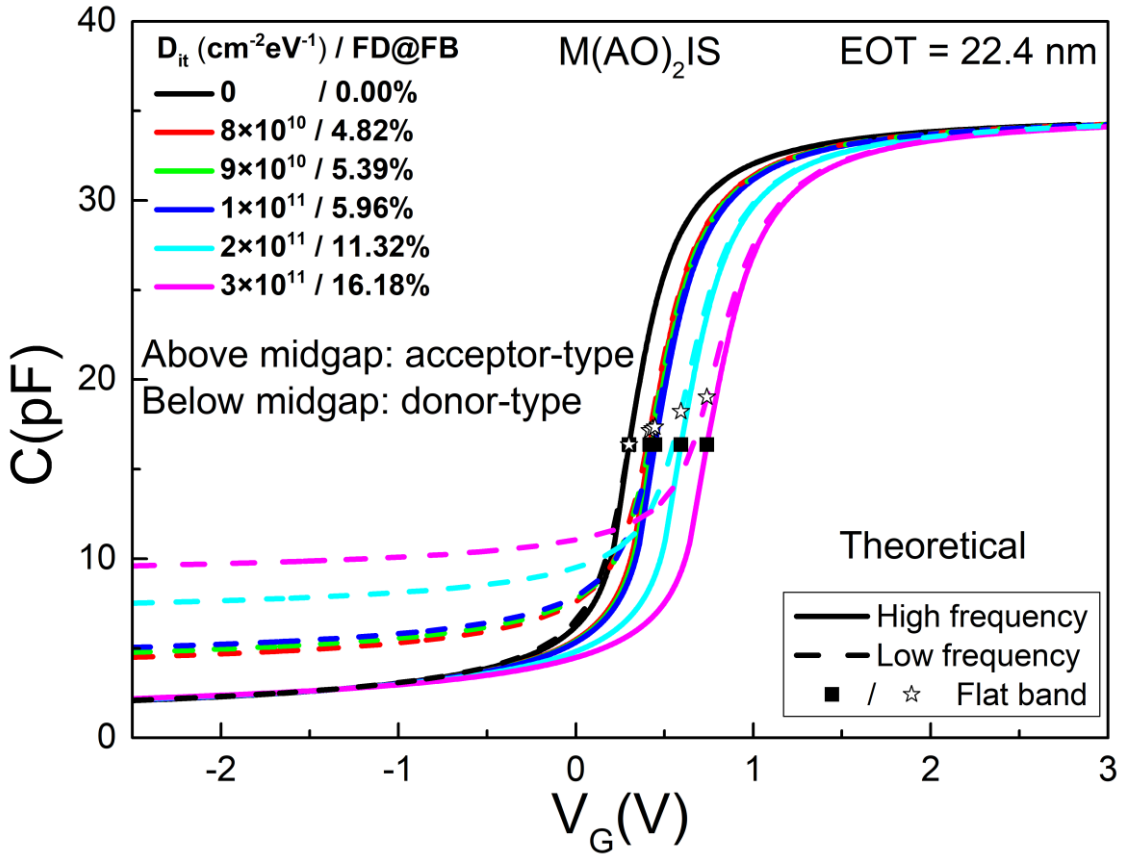

Fig. 3-6. The theoretical *C-V* curves with various D_{it} and corresponding frequency dispersion (*FD*). The *FD* of the experimental data at the flat band voltage was about 10.14%.

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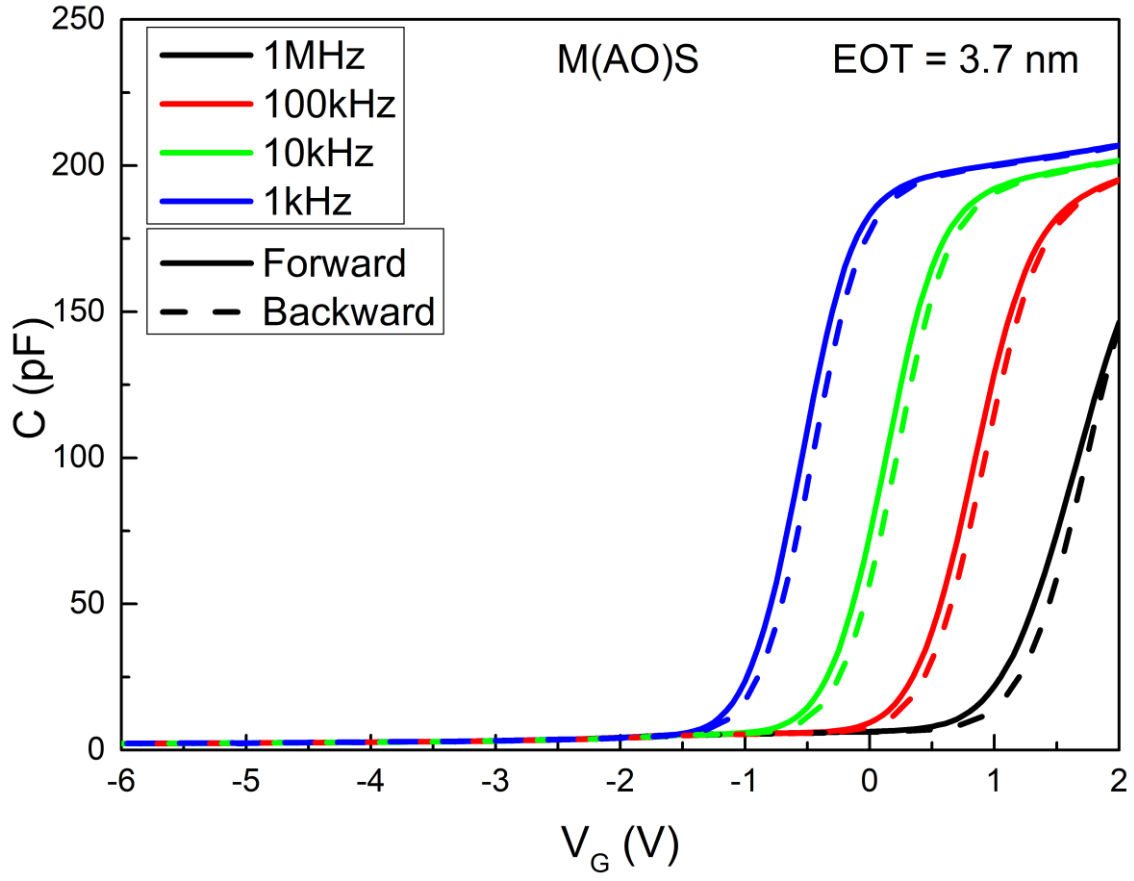

Fig. 3-7. *C-V* characteristics of the M(AO)S device, showing very large frequency dispersion, probably originating from the border traps.

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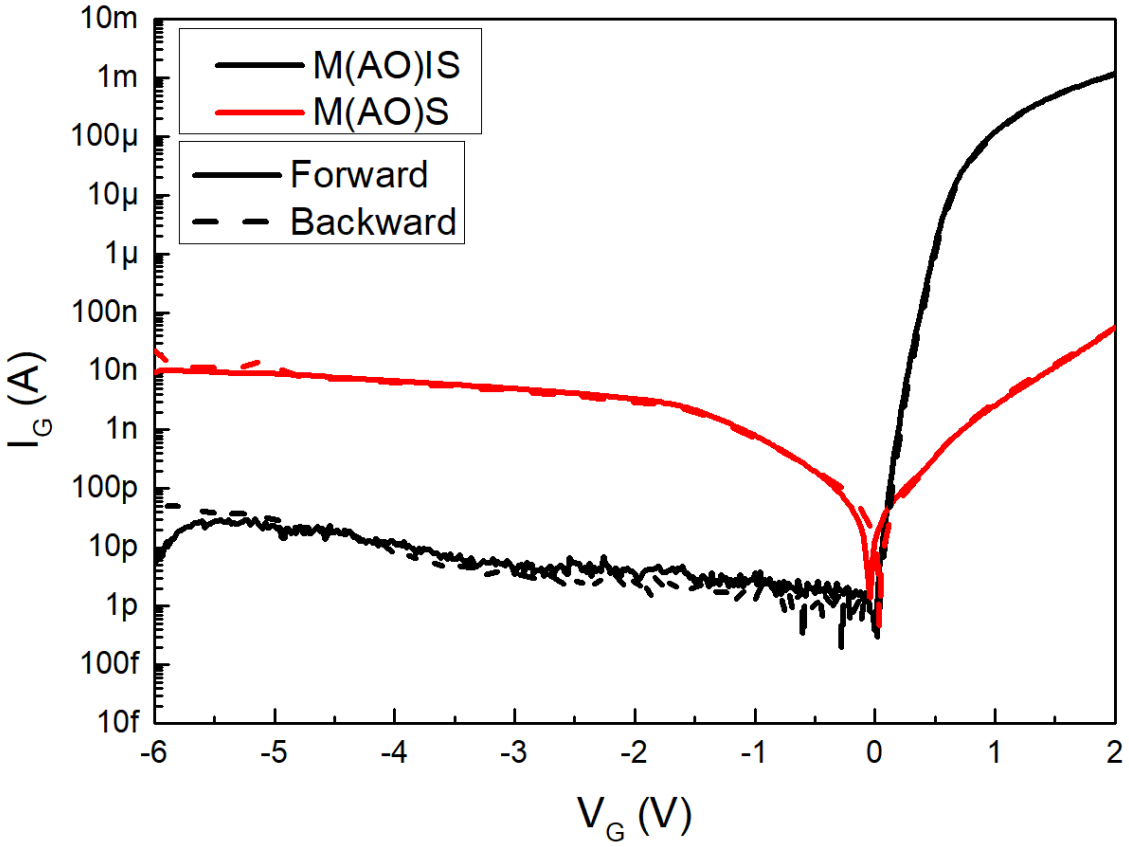

Fig. 3-8. *I-V* characteristics of the Al_2O_3-stacking MIS devices w/ & w/o a SiO_2 interfacial layer, i.e., the structures of M(AO)IS and M(AO)S. The gate current of the M(AO)IS device was significantly lower than that of the M(AO)S device at the reverse bias, while the gate current of the M(AO)IS device was much higher than that of the M(AO)S device in the accumulation region.

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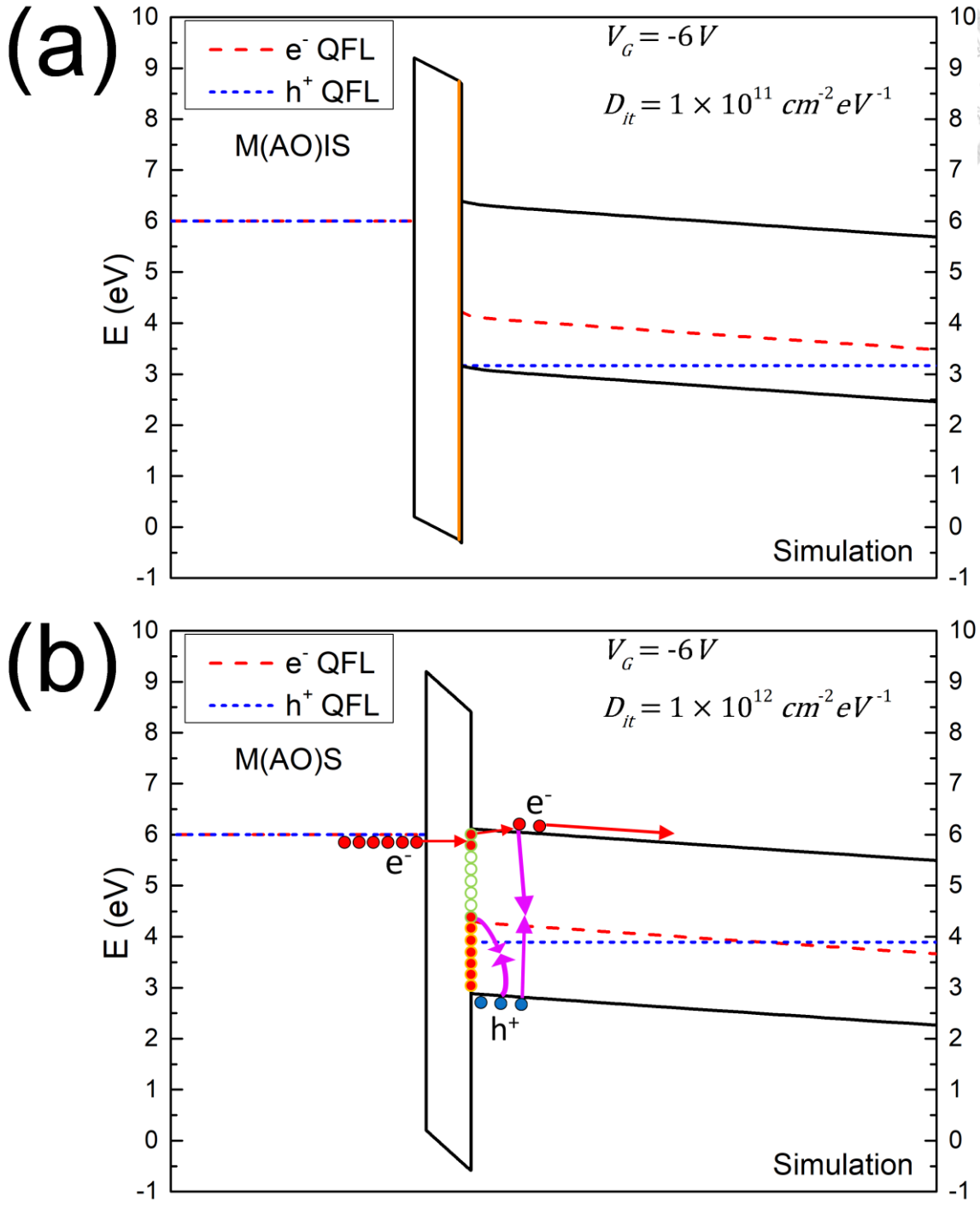

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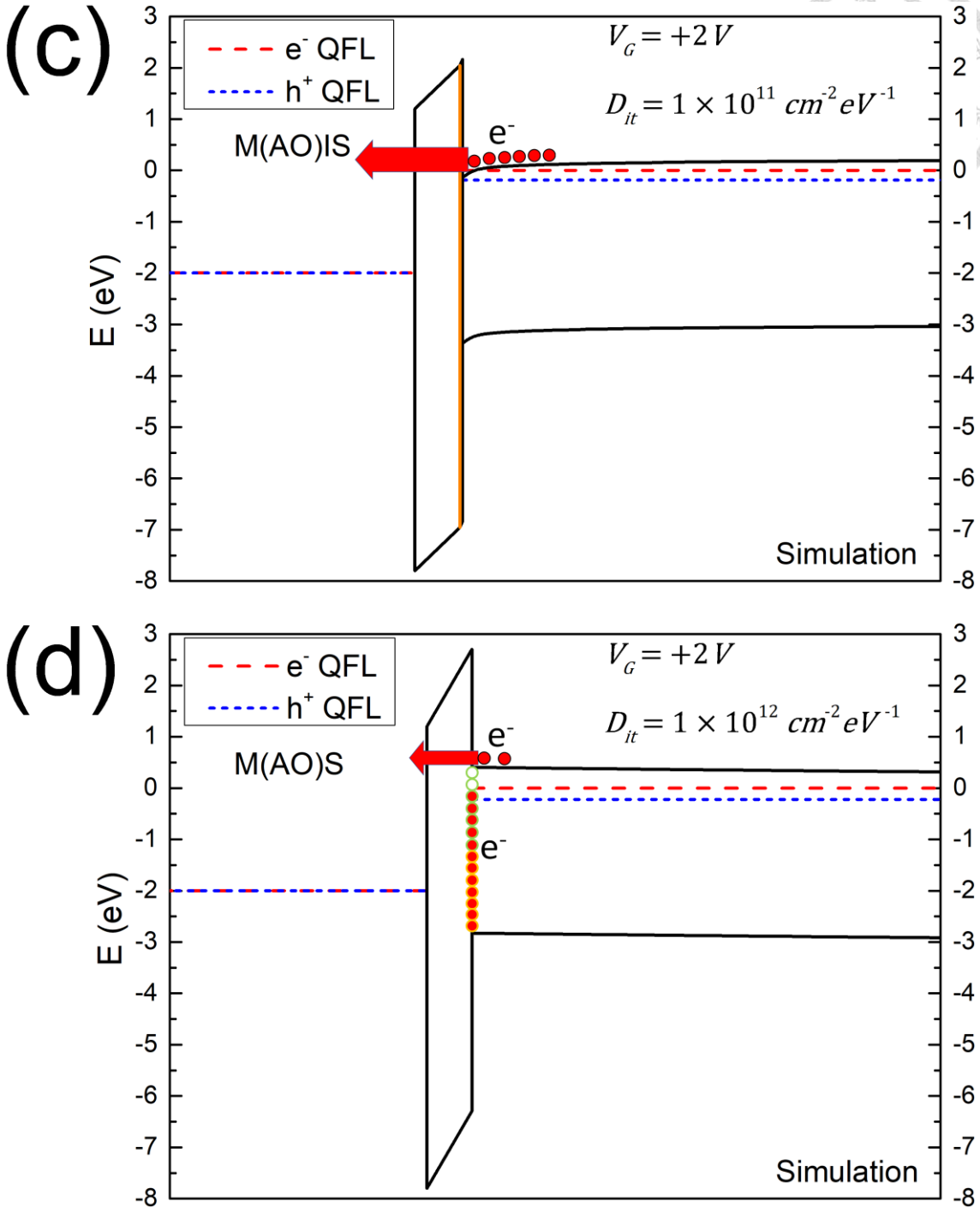

Fig. 3-9. Simulated band diagrams for (a) M(AO)IS and (b) M(AO)S devices at -6 V, and (c) M(AO)IS and (d) M(AO)S at +2 V. The D_{it} was set as 1×10^{11} $cm^{-2}eV^{-1}$ for the M(AO)IS structure and 2×10^{11} $cm^{-2}eV^{-1}$ for the M(AO)S structure.

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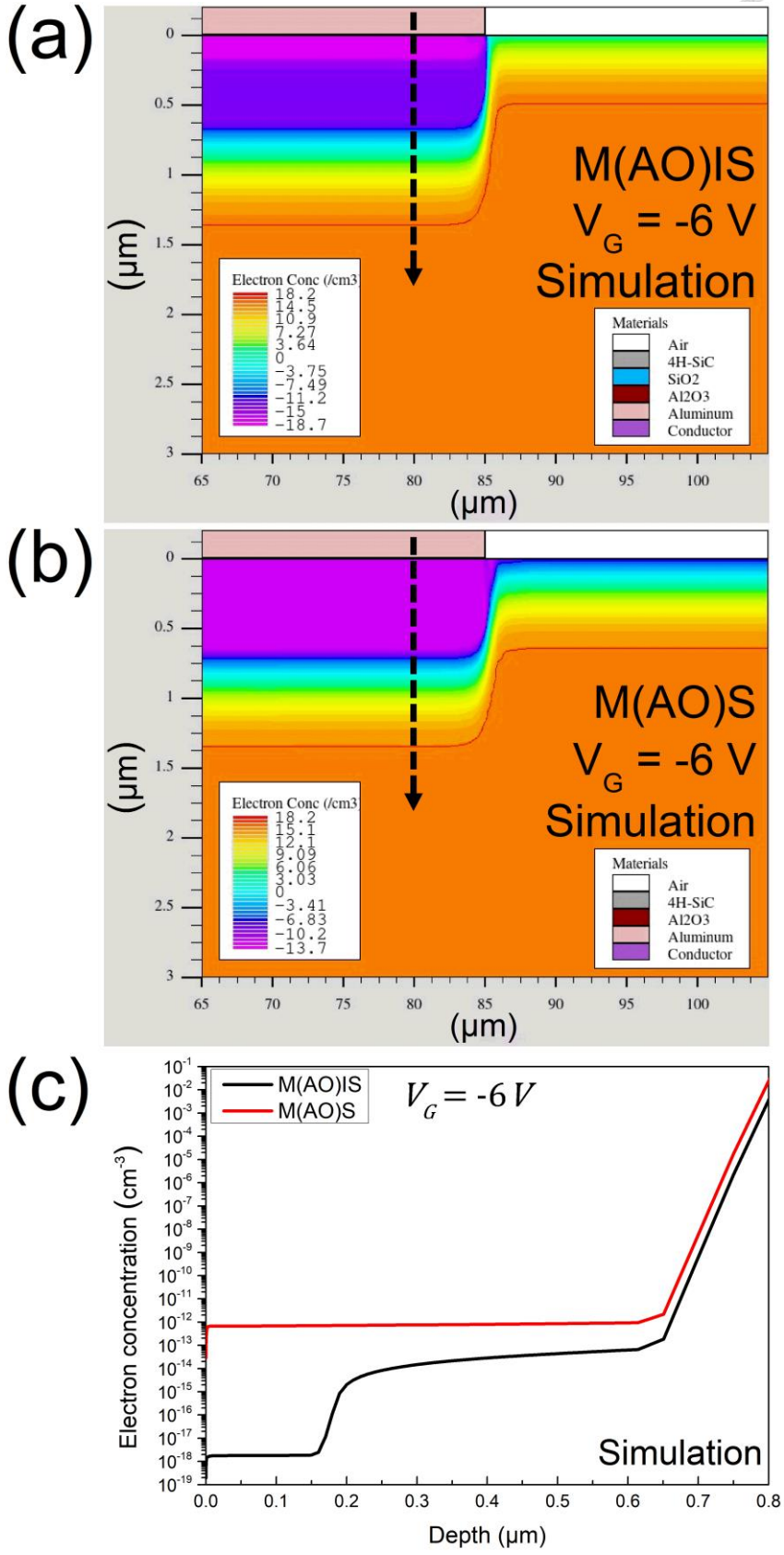

Fig. 3-10. Simulated 2-D distribution of the electron concentration of (a) M(AO)IS and (b) M(AO)S structures, and (c) depth profile of the electron concentration at -6 V.

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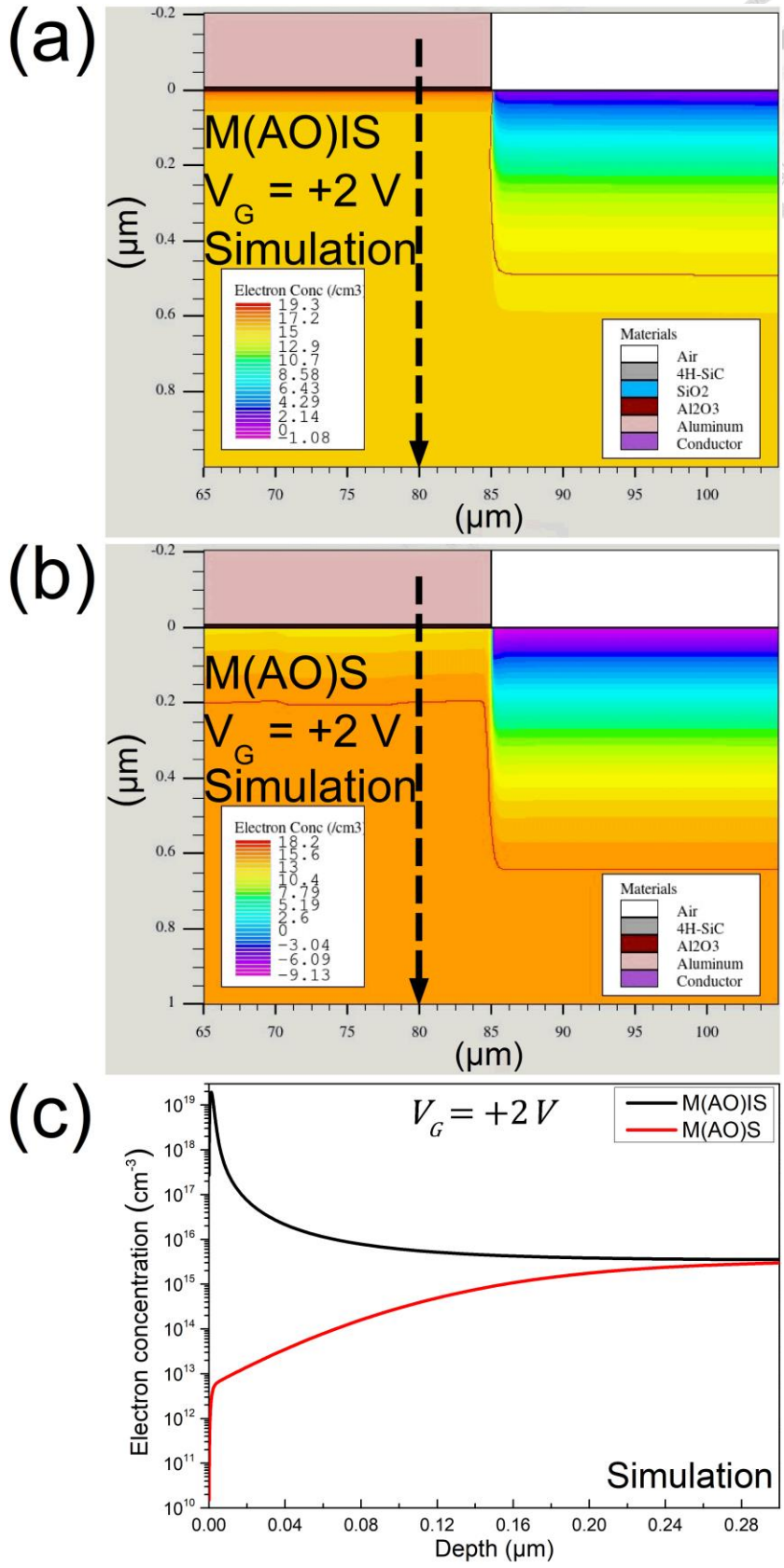

Fig. 3-11. Simulated 2-D distribution of the electron concentration of (a) M(AO)IS and (b) M(AO)S structures, and (c) depth profile of the electron concentration at +2 V.

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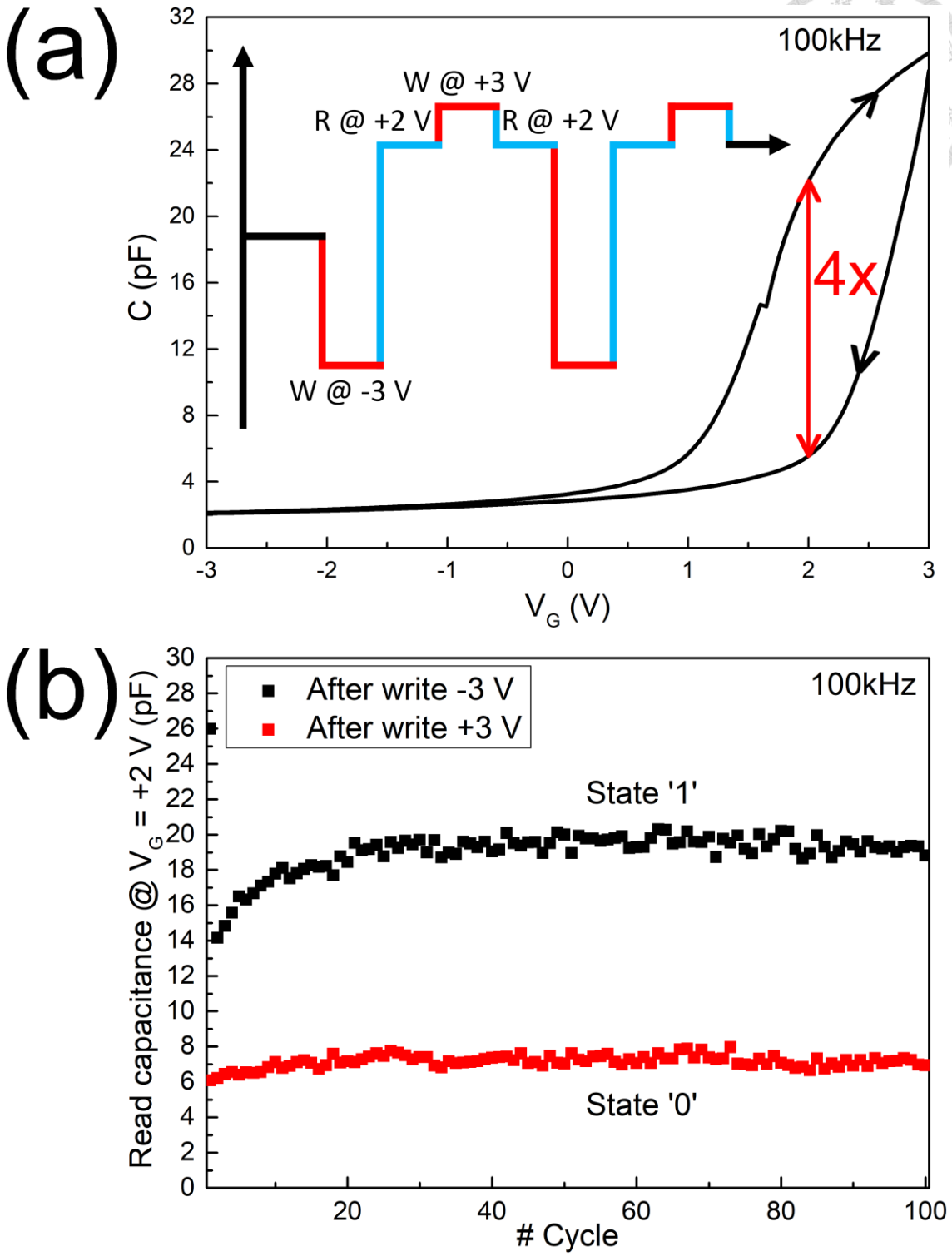

Fig. 3-12. (a) *C-V* curves of 100 kHz at +2 V and a schematic diagram of the memory operation cycle. (b) Endurance test by memory operating for 100 cycles, remaining a stable capacitance window between the state '0' and the state '1'.

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Chapter 4

Conclusion and Future Work

4-1 Conclusion

4-2 Future Work

4-2-1 Parameters Optimization and Mechanism Study for ISHO

4-2-2 ANO Under UV Illumination

4-2-3 High-κ Stacking with HfO_2

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4-1 Conclusion

In conclusion, this thesis has successfully demonstrated novel techniques for oxidizing 4H-SiC substrates and the applications of the fabricated MIS devices for UV sensors and memory.

In Chapter 1, we established the foundational understanding of 4H-SiC, including its comparative properties against other semiconductors and various polytypes, the oxidation processes such as thermal oxidation and ANO technique, and the detailed methods for analyzing oxidation and interface properties. Additionally, the chapter covered the integration of high-κ dielectric materials and the phenomenon of charge trapping for MIS devices.

In Chapter 2, a novel method for fabricating low interface trap density 4H-SiC MIS structures via sub-1000 °C intermittent spray hydrated oxidation (ISHO) is demonstrated. By the material and electrical characterization results, we reveal the fabrication of a high-quality SiO_2 layer with a controllable oxide thickness from about 3 nm to 7 nm within 1 hour, exhibiting minimal carbon clustering at the interface and resulting in a remarkably low D_{it} of 2×10^{11} $cm^{-2}eV^{-1}$ at the flat-band voltage. Furthermore, the fabricated MIS devices show distinguished UV sensing capabilities, with demonstrated photocurrent windows extending about three orders of magnitude in amplification and linear responsivity. The 4H-SiC MIS devices also maintain photo-to-dark current ratios (PDCR)

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of about two to three orders of magnitude even at high temperatures up to 100 °C, verifying the high-temperature tolerance capability. These findings manifest the ISHO technique as a promising method for forming high-quality oxide for 4H-SiC substrates and the potential of 4H-SiC MIS devices for high-performance UV sensor applications.

Finally, Chapter 3 explores an alternative method for fabricating MIS devices on 4H-SiC substrates, aiming at oxide formation by the ANO technique at room temperature. Through material and electrical characterization of MIS devices with different structures, including $M(AO)_2IS$, M(AO)IS, and M(AO)S, we observe uniform oxide layers and interface properties critical for device performance. The results reveal extremely low D_{it} of 1×10^{11} $cm^{-2}eV^{-1}$ at the flat band voltage and suppressed gate leakage current in devices with thin SiO_2 interfacial layers, validated via experimental and theoretical data. Additionally, TCAD simulation provides insights into interface properties and current characteristics of Al_2O_3-stacking MIS devices w/ & w/o the SiO_2 interfacial layers, emphasizing the necessity of SiO_2 for suppressing leakage currents and improving device performance. Furthermore, this study explores the potential of Al_2O_3-stacking MIS devices for memory applications, showing hysteresis in the *C-V* characteristics and stability in the endurance test and suggesting their suitability for integration with 4H-SiC power ICs as embedded memory.

This thesis presents breakthrough innovations in the fabrication of the oxide layer in

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4H-SiC devices, highlighting its significance in the development and applications of silicon carbide devices.

4-2 Future Work

4-2-1 Parameters Optimization and Mechanism Study for ISHO

In section 2-3-1, we have discussed the relation between the EOT and the oxidation time of ISHO fitted by the Deal-Grove model. The results show that the linear rate constant B related to diffusion is much smaller compared to the parabolic rate constant B/A related to reaction, indicating that it's a reaction-dominant process. To improve the growth rate of the SiO_2 layer, the parameters of ISHO should be optimized. The humidity in the furnace has to be saturated for this purpose, so we must ensure that there is always liquid water existing in the furnace. Accordingly, we can spray DI water into the furnace periodically with a constant time interval. The optimal parameters of the amount of spraying DI water and the time interval need further investigation.

The ISHO technique has proved that it is capable of fabricating a high-quality SiO_2 film on a 4H-SiC substrate with low D_{it} and low Q_{eff}. However, the mechanism that makes ISHO such an extraordinary method for SiO_2 growth on 4H-SiC wafers still remains unknown. The biggest differences between ISHO and the conventional wet oxidation are the moisture and the temperature. If the spraying time interval is short

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enough in the ISHO process, the moisture can reach saturation, and there is still original oxygen remaining in the furnace; on the other hand, the moisture and the amount of oxygen in the conventional wet oxidation is determined by the flow rate of the gases flowing into the furnace. Additionally, the lower temperature in the ISHO process compared to the conventional wet oxidation may have contributed to its good performance. The actual mechanism of ISHO still needs further study.

4-2-2 ANO Under UV Illumination

Even though section 3-3-1 has demonstrated the excellent D_{it} of the 4H-SiC MIS device by the ANO technique, the thickness of the SiO_2 layer is still too thin due to the lack of holes in the n-type 4H-SiC substrate. The ANO process needs the •OH radicals and holes to form SiO_2. The reaction formulas of ANO for SiC are [44]

$$\mathrm{SiC} + 2\mathrm{H_2O} + 4\mathrm{h^+} \rightarrow \mathrm{SiO} + 4\mathrm{H^+} + \mathrm{CO(g)} \quad (4\text{-}1)$$

$$\mathrm{SiC} + 4\mathrm{H_2O} + 8\mathrm{h^+} \rightarrow \mathrm{SiO_2} + 8\mathrm{H^+} + \mathrm{CO_2(g)} \quad (4\text{-}2)$$

at anode, and

$$2\mathrm{H_2O} + 2\mathrm{e^-} \rightarrow \mathrm{H_2(g)} + 2\mathrm{OH^-} \quad (4\text{-}3)$$

at cathode. Previous studies have shown that by ANO under UV illumination, the considerable generated holes can enhance the oxidation reaction on the n-type Si substrate [45]. Inspired by this, we have tried this method on 4H-SiC wafers by ANO illuminated

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under UV light, denoted as ANO(UV), with 60 V for 60 min. Fig. 4-1(a) and (b) show the results of its *C-V* and *I-V* characteristics, respectively. It has indeed grown a SiO_2 layer with an EOT of 5.6 nm successfully. Nonetheless, by fitting with the theoretical high-frequency *C-V* curve, the obtained effective oxide charge is $Q_{eff}/q = 1.0 \times 10^{13}$ cm^{-2}, and the D_{it} at flat band voltage is 8.5×10^{12} $cm^{-2}eV^{-1}$, both values are high compared to those of 4H-SiC MIS devices shown in section 2-3-2. Note that there's no annealing process following the ANO(UV) process. Future work can explore the results of ANO(UV) followed by a POA process to further improve the oxide quality.

4-2-3 High-κ Stacking with HfO_2

In Chapter 3, we demonstrate the Al_2O_3-stacking MIS devices with SiO_2 interfacial layer, showing extremely low D_{it} and low leakage current at reverse bias. However, because the Al_2O_3 layers are edge-removed due to the aluminum's wet etch process. The defects at these edges can still become the leakage paths, thereby reducing the effect of gate leakage current suppression. To improve this issue, Al_2O_3 can be replaced by HfO_2 as a high-κ dielectric in the 4H-SiC MIS devices since it can't be removed by the aluminum etchant, as illustrated in Fig. 4-2. The HfO_2 layers can be formed by sputtering and ANO processes.

Furthermore, the dielectric constant of HfO_2 is 25 [46], which is much higher than

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that of Al_2O_3 ranging from 7 to 8.5. This has benefits for the equivalent oxide thickness reduction. Additionally, HfO_2 layers have often been used in ferroelectric field-effect transistors (FeFETs) for memory applications [47], [48], [49]. The HfO_2 FeFET offers many advantages, such as non-volatility, low power, fast switching speed, scalability, good endurance, and compatibility with CMOS technology. Future work can dive into the possibility of integration with the HfO_2 FeFETs on 4H-SiC substrates.

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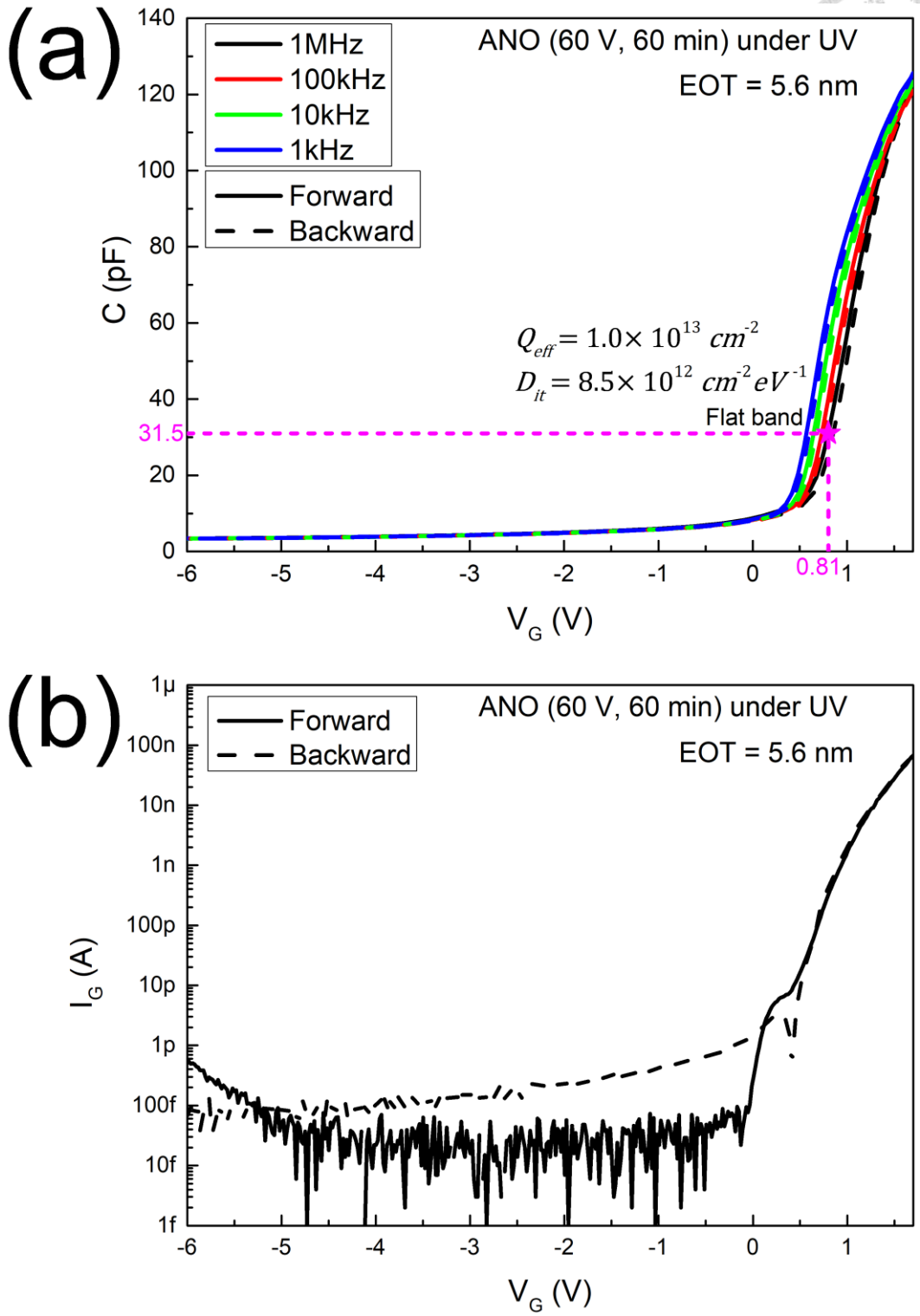

Fig. 4-1. (a) *C-V* and (b) *I-V* characteristics of a 4H-SiC MIS device with an EOT of 5.6 nm SiO_2 layer by ANO illuminated under UV light with 60 V for 60 min. The Q_{eff}/q is 1.0×10^{13} cm^{-2}, and the D_{it} at flat band voltage is 8.5×10^{12} $cm^{-2}eV^{-1}$ by fitting with the theoretical high-frequency *C-V* curve.

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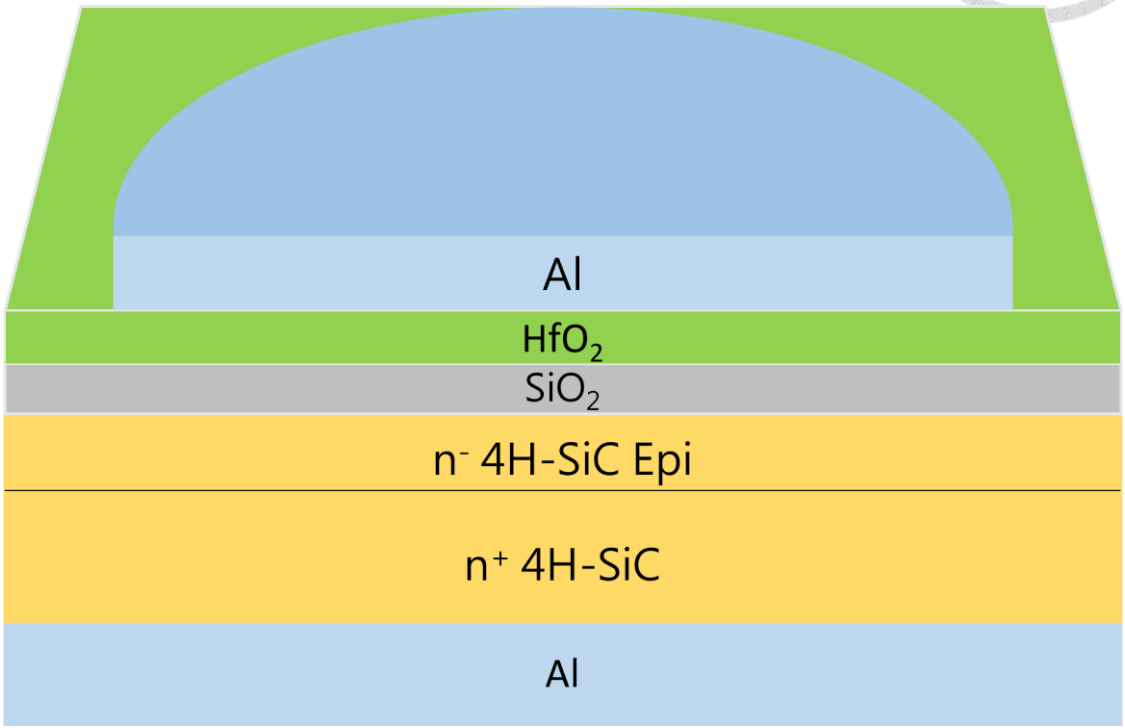

Fig. 4-2. Device schematic of the 4H-SiC MIS structure with HfO_2-stacking.

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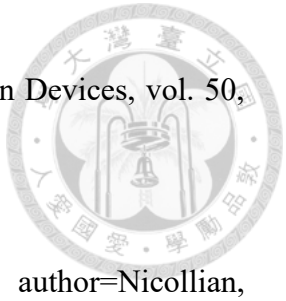

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