國立臺灣大學電機資訊學院電信工程學研究所

碩士論文

Graduate Institute of Communication Engineering
College of Electrical Engineering and Computer Science
National Taiwan University

Master's Thesis

應用於第五代行動通訊系統之低雜訊放大器及寬頻雙向分佈式放大器

Research on Low-Noise Amplifier and Broadband Bidirectional Distributed Amplifier for Fifth-Generation Mobile Communication Systems

蔡瑋軒

Wei-Hsuan Tsai

指導教授：王暉 博士

Advisor: Huei Wang, Ph.D.

中華民國 113 年 5 月

May, 2024

doi:10.6342/NTU202402726

口試委員審定書

國立臺灣大學碩士學位論文
口試委員會審定書
MASTER'S THESIS ACCEPTANCE CERTIFICATE
NATIONAL TAIWAN UNIVERSITY

應用於第五代行動通訊系統之低雜訊放大器及寬頻雙向分佈式放大器

Research on Low-Noise Amplifier and Broadband Bidirectional Distributed Amplifier for Fifth-Generation Mobile Communication Systems

本論文係蔡瑋軒 R09942034 在國立臺灣大學電信工程學研究所完成之碩士學位論文，於民國 113 年 5 月 28 日承下列考試委員審查通過及口試及格，特此證明。

The undersigned, appointed by the Graduate Institute of Communication Engineering on 28, May, 2024 have examined a Master's Thesis entitled above presented by Wei-Hsuan Tsai R09942034 candidate and hereby certify that it is worthy of acceptance.

口試委員 Oral examination committee:

王暉　黃天偉　王雲杉

（指導教授 Advisor）

簧致翰　林坤佑

所長 Director: 劉揚安

doi:10.6342/NTU202402726

致謝

研究所這段時間大概是作為學生的最後時光了，能來到台灣的最高的殿堂學習達成了人生的目標之一。能幸運地來到王暉教授門下學習是一件十分幸運的事情，老師願意給學生很多機會去發揮自己的創意去完成不同的電路，並且不會給太多限制，而且會為學生找來很多先進製程，這些機會是只有在這邊才能接觸到的。像是在上課的時候其他老師提到台積電的 16-nm CMOS 是一個不太可能使用到的製程，我卻能有機會利用 16-nm CMOS 完成 PA 的設計，雖然因為所需要的軟體都不一樣，需要多花很多時間學習與習慣，但都是難得的成長與學習經驗。在老師的悉心教導下，我不僅獲得了電路設計的專業知識，更學習到了處事處人的道理和準則。這些寶貴的教導不僅豐富了我的學識，也讓我在學生時期就能積極為未來踏入社會做好準備。

再來我要感謝王雲杉學長、吳源深學長、林憶錡學長、張楷儁學長、黃煒智學長、邱梓洋學長，在我還對一切不熟悉的時候給我需多教導與建議，讓我能很順利的習慣這邊的環境，並且讓我在研究的道路上少走許多彎路。感謝碩士生涯中一起努力的羚毓、愛晨、俊嘉、傳立、育成、家頤，建平，感謝你們陪伴著我一起學習成長，一同修 MMIC 還有 PA 課的過程都是滿滿的回憶，未來也都要繼續保持聯繫。同時也感謝碩士班的學弟妹們，莉容、又華、致學、唯傑、承翰、致廣、宜恒、仲堯、馬恩學弟妹們，謝謝你們總是帶給實驗室歡笑並且讓實驗室的氣氛更加活躍。

最後，我要感謝一直在背後支持我的家人，特別是爸爸和媽媽。爸爸，雖然來不及在你人生的最後給你看我的畢業證書，但我還是有好好的完成學業應該不算辜負你的期待值得自豪的吧。媽媽，這些日子辛苦你了，很多事情不跟你及時講，只是不希望你擔心我，想對你報喜不報憂，讓你聽到我的事情都是值得開心慶祝的。有你們從小對我的栽培才會有今天的我，謝謝你們。

瑋軒

2024.5

doi:10.6342/NTU202402726

中文摘要

放大器在無線收發機中扮演著重要的腳色。在 5G 和高數據速率應用的時代，對高效且高性能放大器的需求日益增加。隨著第五代行動通訊的蓬勃發展，毫米波的研究與應用已成為當今的主要趨勢。然而，隨著對更高頻寬和更快傳輸速率的需求不斷增長，目前的無線通訊頻率主要在 6 GHz 以下已經相當飽和。因此，往更高頻率的設計已成為技術發展中的關鍵方向。其中，Ka-band 被視為第五代行動通訊的主要潛在發展頻段。在無線通訊系統中，發射機的設計至關重要，而本論文的主要焦點在於對放大器的設計和進行研究。

本篇論文主要分成兩個部分: 第一部分為利用 90-nm CMOS 所設計的雙向分佈式放大器的研究。雙向放大器對收發系統面積的縮減有幫助，藉由電路的架構選擇讓電路可以有寬頻的特性和共用匹配電路。此雙向分佈式放大器從 1.9 到 33.5 GHz 的 3 dB 頻寬，並且有 13.8 dB 的增益，還有著 2.9 dB 的雜訊指數。因此，它是用於高速數據傳輸的系統。

第二部分設計了 3 個以 0.18 μm GaAs pHEMT 製程所設計的 Ka-band 低雜訊放大器，其中設計頻段為 5G 可行通訊頻段。第一個低雜訊放大器利用電容匹配的設計有著 19.4 到 32.1 GHz 的 3 dB 頻寬，還有 23 dB 的增益，與 1.5 dB 的雜訊指數。第二個低雜訊放大器利用傳輸線匹配的設計有著 22.9 到 32.9 GHz 的 3 dB 頻寬，還有 21.5 dB 的增益，與 1.8 dB 的雜訊指數。第三個低雜訊放大器利用 Cascode 的架構設計有著 21.3 到 34 GHz 的 3 dB 頻寬，還有 15.9 dB 的增益，與 2.2 dB 的雜訊指數。

doi:10.6342/NTU202402726

關鍵字：分佈式放大器、低雜訊放大器、雙向放大器、寬頻、高速電子遷移率電晶體

doi:10.6342/NTU202402726

ABSTRACT

Amplifiers play a crucial role in wireless transceivers. The demand for efficient and high-performance amplifiers is increasing in the area of 5G and high-data-rate applications. The booming growth of fifth-generation mobile communication (5G) has made millimeter-wave research and applications an important trend. However, as the demand for higher bandwidth and faster transmission rates continues to grow, the current wireless communication frequencies, primarily below 6 GHz, are becoming saturated. Therefore, designing for higher frequencies has become a key direction in technological development. Among these, the Ka-band is considered a primary potential development frequency band for 5G. In wireless communication systems, the design of the transmitter is crucial, and this thesis focuses primarily on the design and study of amplifiers.

This thesis is primarily divided into two parts. The first part focuses on the study of a bidirectional distributed amplifier using 90-nm CMOS process. Bidirectional amplifiers contribute to the reduction of the overall system area by employing a circuit structure that enables broadband characteristics and shared matching circuits. This bidirectional distributed amplifier achieves a 3 dB bandwidth from 1.9 to 33.5 GHz, with a gain of 13.8 dB and a noise figure of 2.9 dB. Therefore, it is suitable for systems requiring high-speed data transmission.

The second part involves the design of three Ka-band low noise amplifiers (LNAs) using the 0.18 μm GaAs pHEMT process, targeting the communication frequencies for 5G. The first LNA, employing capacitor matching, achieves a 3 dB bandwidth from 19.4 to 32.1 GHz, with a gain of 23 dB and a noise figure of 1.5 dB. The second LNA, utilizing transmission line matching, achieves a 3 dB bandwidth from 22.9 to 32.9 GHz, with a gain of 21.5 dB and a noise figure of 1.8 dB. The third LNA, designed with a Cascode

doi:10.6342/NTU202402726

architecture, achieves a 3 dB bandwidth from 21.3 to 34 GHz, with a gain of 15.9 dB and a noise figure of 2.2 dB.

Index Terms – Distributed Amplifier, Low Noise Amplifier, Bidirectional Amplifier, broadband, pHEMT

doi:10.6342/NTU202402726

CONTENTS

doi:10.6342/NTU202402726

doi:10.6342/NTU202402726

doi:10.6342/NTU202402726

LIST OF FIGURES

doi:10.6342/NTU202402726

doi:10.6342/NTU202402726

doi:10.6342/NTU202402726

doi:10.6342/NTU202402726

doi:10.6342/NTU202402726

LIST OF TABLES

doi:10.6342/NTU202402726

Chapter 1 Introduction

1.1 Background and Motivation

Previous works often utilize the III-V compound process for developing Tx/Rx chipset devices, which remains a prevalent commercial approach due to their superior noise performance and output power capabilities [29]. However, they suffer from challenges such as more extensive chip area requirements, increased DC power consumption, and higher costs [15]. With the rapid advancements in silicon processing technology, RF performance has improved significantly. The integration of silicon-based T/R chipsets facilitates cost reduction and allows for the incorporation of multiple T/R channels within a single die. Nonetheless, the switch loss in bulk CMOS tends to be higher compared to GaAs due to the conductive substrate [13]. To further enhance the gain of the T/R chipset, there is a growing demand for compact, bidirectional amplifiers. Recently, bidirectional amplifiers have been introduced in the literatures [2]-[4]. However, they often suffer from large chip sizes due to the separate transmitting and receiving amplifiers and exhibit a limited fractional operating bandwidth. Therefore, in order to effectively enhance the bandwidth, the distributed amplifier (DA) structure was chosen as the fundamental architecture to complete this bidirectional amplifier, and a shared matching circuit was employed to address the issue, as mentioned earlier, of large chip area.

III-V compound processes are often chosen for applications in RF circuits due to their superior noise characteristics and higher output power. Designing Low-Noise Amplifiers (LNAs) using GaAs technology in the Ka-band offers various advantages. Compared to CMOS technology, GaAs demonstrates superior performance in high-

doi:10.6342/NTU202402726

frequency applications, particularly in terms of noise, contributing to an enhanced performance ceiling for LNAs. In the Ka-band, signal noise sensitivity is crucial, and GaAs technology's electrical characteristics effectively address this challenge [15]. In order to design an LNA for a 5G transceiver with a noise figure in the Ka-band that is less than 2.4 dB, GaAs technology offers a greater chance of achieving the desired results than CMOS technology due to the absence of area and power limitations.

doi:10.6342/NTU202402726

1.2 Literature Survey

The literature surveys include Bidirectional distributed amplifiers and LNA in GaAs pHEMT process.

1.2.1 Bidirectional Distributed Amplifier

In the current landscape of new generation transceivers, there is a growing demand for systems that can achieve wideband operation and high resolution while maintaining a balance between system cost, spatial requirements, and overall integrity. Some bidirectional amplifiers are surveyed. The previously published BDDAs are listed in Table 1.1.

In [13], an X-band bi-directional T/R chipset was presented, where the switch loss in bulk CMOS was attributed to the conductive substrate. To overcome this, a single-stage distributed amplifier paired with the cascode configuration was designed for a bidirectional amplifier, eliminating the use of switches by employing voltage-controlled transistors to control signal flow. Similarly, in [1], a voltage-controlled signal flow was employed but with a multi-stage distributed amplifier, resulting in higher gain and bandwidth.

However, while the distributed amplifier (DA) architecture serves as a promising option for bidirectional amplifiers (BDAs), allowing for the sharing of gate and drain transmission lines in the amplification paths from input to output, it still presents drawbacks such as high DC power consumption (P_{dc}), moderate small-signal gain, and large chip size. To address these challenges, the article [6] provides mathematical analyses of the bidirectional distributed amplifier (BDDA), comparing its performance with a conventional DA to explore more effective design results.

From the listed circuits, most of the BDDAs did not demonstrate the broadband

doi:10.6342/NTU202402726

characteristics of the DA, nor did they exhibit high gain. Therefore, in this study, the aim was to fully exploit the advantages of the DA's broadband capability. Higher gain can be achieved by selecting appropriate stages and employing g_m-boosting techniques.

Table 1.1 Summary of previously published BDDA

Ref.	**Process**	**BW (GHz)**	**Gain (dB)**	**GBW (GHz)**	**Noise Figure (dB)**	**OP_{1dB} (dBm)**	**P_{dc} (mW)**	**Bidirectional**
[13]	0.13-μm CMOS	8.5~10.5	5.3	3.7	NA	7.4	43	Yes
[1]	0.13-μm CMOS	3~20	11	42.6	3.2~6.5	8	68	Yes
[10]	0.13-μm SiGe Bi-CMOS	2~22	9.6	60.4	4.5~5	11	100	Yes
[11]	0.13-μm SiGe Bi-CMOS	2~23	9.6	63.4	<12.7	N.A.	75	Yes
[6]	0.18-μm CMOS	2~12	9	28.2	5.9~7.4	9.5	132	Yes
[12]	0.13-μm SiGe Bi-CMOS	7~30	11.2	83.5	6~10	-2.5	13.8	Yes

doi:10.6342/NTU202402726

1.2.2 LNA in GaAs pHEMT Process

For instance, a study proposed using transformer feedback to enhance the amplifier's bandwidth [16]. However, in III-V compound processes, where multiple metal layers are not available for stacking, the transformer's design could occupy a significant area. Another approach involves using RLC feedback to increase transistor gain and achieve better bandwidth performance. However, this method may impact noise figure stability and is more suitable for use in the second or third stage of amplification [17], [18]. Source degeneration, a negative feedback technique, can assist in bringing the noise figure point and input conjugate point closer, aiding in LNA matching design [19], [20]. Proper bias selection can also contribute to better LNA performance [19], [20]. Simply employing resistor feedback can generate wideband characteristics, but to maintain circuit gain, transistor stacking is required, leading to increased power consumption and potential impacts on noise figure [21].

The mentioned techniques have been proposed to improve noise, gain, and bandwidth in various ways, each with advantages and disadvantages. Therefore, in this study, source degeneration and appropriate bias selection will be employed to design the LNA required for a 5G transceiver system.

doi:10.6342/NTU202402726

Table 1.2 Summary of previously published LNA in GaAs pHEMT process.

Ref.	Process	BW (GHz)	Gain (dB)	Noise Figure (dB)	OP_{1dB} (dBm)	P_{dc} (mW)	Chip Area (mm^2)
[20]	0.15 μm GaAs pHEMT	22~34	14.3	1.75	N.A.	N.A.	1*0.54
[22]	0.15 μm GaAs pHEMT	10~43	24.6	2.4	12.3	110	1.5*0.7
[18]	0.15 μm GaAs pHEMT	0.1~23	27.4	2.7	8.6	335	1.58*0.86
[21]	0.15 μm GaAs pHEMT	0.1~20	28.6	3.1	12.7	505	1.7*0.9
[27]	0.1 μm GaAs pHEMT	30~50	21.1	3.2	9.5	75.6	2*1
[19]	0.15 μm GaAs pHEMT	28.5~50.5	23	3.8	N.A.	62.6	2*1.5
[17]	0.1 μm GaAs pHEMT	18~43	21.6	1.8	11.5	140	2*1
[16]	0.1 μm GaAs pHEMT	11~39	23	2.1	8.6	80	1.7*1

doi:10.6342/NTU202402726

1.3 Contributions

This paper presents research and design on a bidirectional distributed amplifier using 90-nm CMOS process and low-noise amplifiers (LNAs) using 0.18 μm GaAs E-mode pHEMT process. Several design techniques were employed to ensure the satisfactory performance of these circuits. The contributions of this research are described as follows.

In previously published bidirectional distributed amplifiers, narrow bandwidth performance was often observed due to G_m cell structure limitations. In this study, a skew-symmetric layout approach was utilized, allowing for more parameters to be adjusted during the design process, thereby exploring opportunities for improved performance. Additionally, using long transmission lines instead of spiral inductors reduced the chip size, and removing ground metal from the transmission lines improved the inductor's Q factor, resulting in higher gain performance. The proposed bidirectional distributed amplifier achieved a 3 dB bandwidth of 1.9 to 33.5 GHz, a small signal gain of 13.8 dB, and a noise figure of 2.9 to 3.9 dB. This work has been published in the 2022 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT).

In the design of low-noise amplifiers, source degeneration was employed to achieve low noise figure performance in the first stage, while subsequent stages provided gain and bandwidth characteristics to meet the design goals. Each of the three versions of the design has different features. The version using capacitance matching exhibited the highest gain and lowest noise figure; the version using transmission line matching improved on the previous version's large chip size, and insufficient return loss by sacrificing some noise performance to enhance return loss and achieve a smaller chip size, and the cascode version utilized the higher gain characteristics of cascode to reduce the overall number of stages, further minimizing the chip size.

doi:10.6342/NTU202402726

Overall, the study provides valuable insights into the design and performance optimization of bidirectional distributed amplifiers and LNAs for high-frequency applications.

doi:10.6342/NTU202402726

1.4 Thesis Organization

The organization of this thesis is shown as follows.

In chapter 2, a switchless bidirectional distributed amplifier in 90-nm CMOS process is designed and measured. The design procedures are demonstrating, including device size selection, number of stage consideration, bias selection, Gm cell design, gate line and drain line design, optimizing L_m, RF choke design. The simulated, measured results and comparison table are shown. A short conclusion is presented at the end of this chapter.

Chapter 3 introduces three 28 GHz LNAs designed with 0.18 μm GaAs pHEMT. This chapter covers bias selection, transistor size selection, and source degeneration analysis and selection. In the first version, capacitor matching is employed for inter-stage matching. In the second version, the matching approach is changed to transmission lines to achieve better return loss performance and a smaller chip area. Finally, the third version adopts a cascode architecture to increase the gain of a single stage, thereby reducing the total number of stages and further minimizing the chip size.

Finally, a conclusion of this thesis is given in Chapter 4.

doi:10.6342/NTU202402726

Chapter 2 The Design of A Switchless Bidirectional Distributed Amplifier in 90-nm CMOS Process

2.1 Introduction

In the design of a bidirectional amplifier, it is common to see the use of switches to control the signal flow direction, as shown in Fig. 2.1 [2]-[4]. However, in high-frequency situations, CMOS switches often introduce high insertion loss from the conductive silicon substrate, and they also require extra circuit area to place the switch. Using gate voltage to turn on the amplifier or not can help avoid losses at high frequencies [1]. Moreover, the common presentation of bidirectional circuits involves the parallel connection of two amplifiers [2]-[4] rather than a shared matching network. The area required is similar to the parallel connection of two circuits. However, utilizing a distributed amplifier (DA) enables the shared use of these matching networks [6], as all the matching networks are 50-ohm artificial transmission lines (ATL). By selecting suitable inductors on the gate and drain lines, these inductors can be shared, reducing the circuit area to approximately half that of two parallel conventional DAs, as shown in Fig. 2.2.

doi:10.6342/NTU202402726

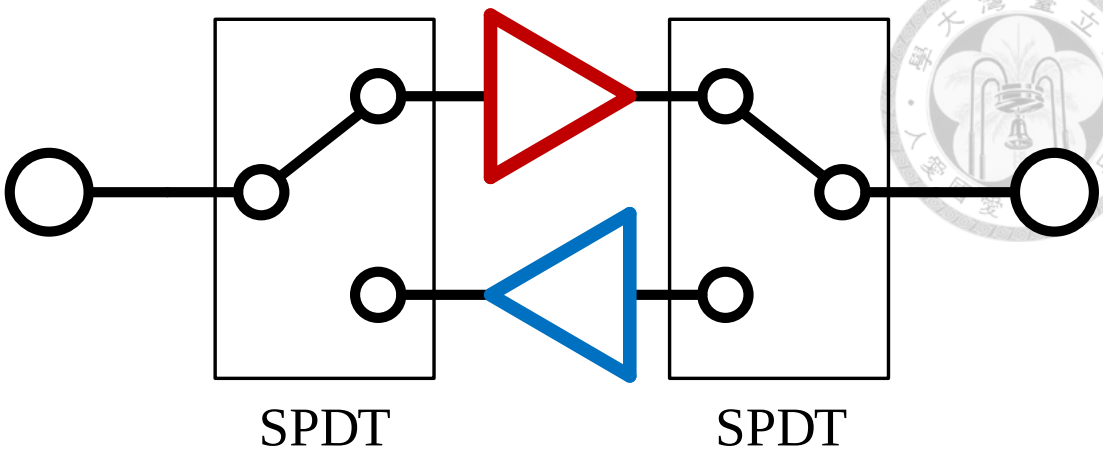

Fig. 2.1. SPDT-based bidirectional amplifier.

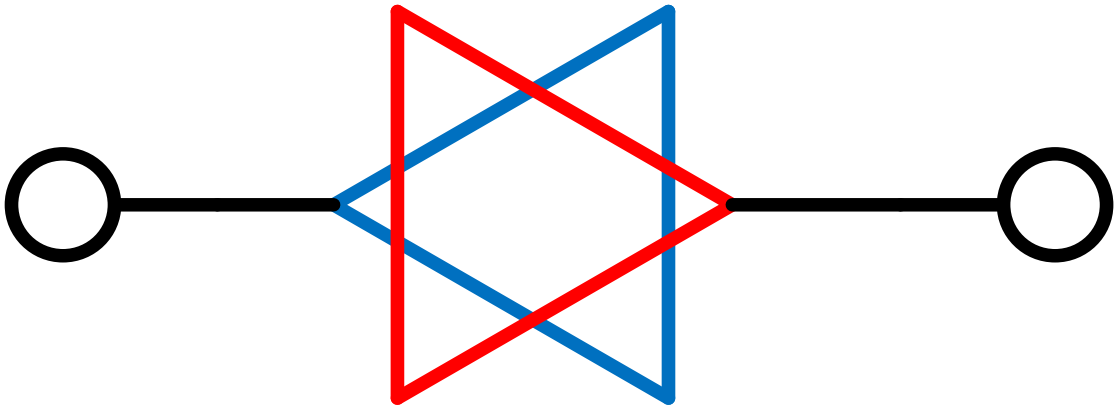

Fig. 2.2. Bidirectional amplifier sharing matching networks.

2.2 Circuit Architecture

During selecting the architecture of the gain cell, to fulfill the requirements of bidirectional design and prevent the reverse signal from generating loop gain and causing oscillation issues, isolation becomes a critical parameter [28]. From Fig. 2.3, it is evident that the isolation of the cascode is 20 dB better than that of the common source (CS) at 16 GHz. Ensuring that the small signal gain does not exceed the isolation of the cascode can prevent instability caused by loop gain. Therefore, utilizing cascode as the gain cell is recommended in the design of the bidirectional distributed amplifier (BDDA).

doi:10.6342/NTU202402726

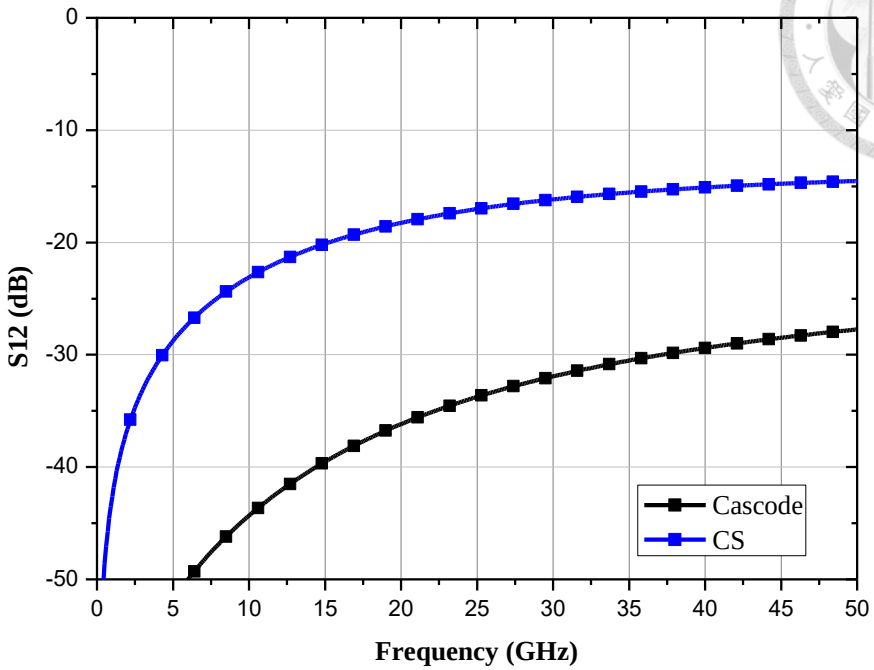

Fig. 2.3. Comparison of Cascode and CS isolation.

2.3 Device Size Selection

In the design of the distributed amplifier (DA), the width size of the transistors is a crucial variable that affects the parasitic capacitance and g_m of the transistors. The increase and decrease of C_{in} can be observed from Fig. 2.4, which is positively correlated with the width of the transistor, and the bandwidth of the distributed amplifier is mainly determined by the cut-off frequency of the artificial transmission lines [5], which are given by

$$f_c = \frac{1}{\pi\sqrt{L_{in}C_{in}}} = \frac{1}{\pi Z_{0g} C_{in}} \tag{2.1}$$

Furthermore, the gain of the DA, as estimated by

$$A_v = \frac{1}{2} n g_m Z_0 \tag{2.2}$$

doi:10.6342/NTU202402726

is directly proportional to the growth of g_m. Consequently, as the width of the transistor increases, the gain increases, and the bandwidth decreases.

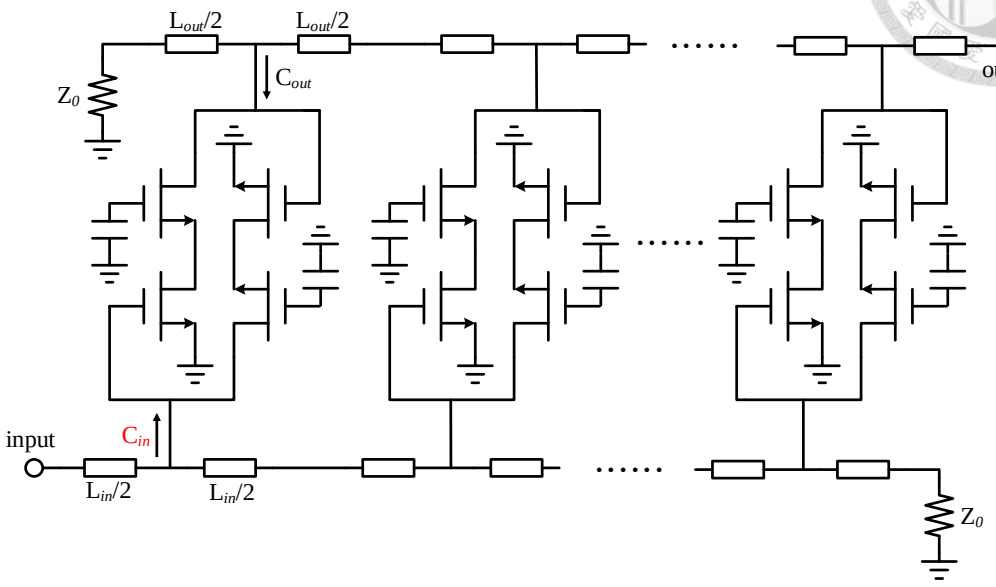

Fig. 2.4. Schematic of the simulation circuit.

In reviewing previously published bidirectional distributed amplifiers, the majority of designs are 3 to 5 stages [1], [6]. Therefore, when selecting the size, a 4-stage DA is initially considered for comparison. Subsequently, a V_d bias of 2 V is applied to each gain cell, with the transistors operating at their maximum g_m levels of 1.7 V and 0.7 V, respectively. Fig. 2.5 shows the result of simulations from 10 to 25 fingers. It is observed that at 10 fingers, the peak gain is only 10.6 dB. However, at 25 fingers, the peak gain increases to 17.2 dB. This observation corresponds to the growth of g_m in the formula, resulting in an increase in gain. Consequently, a wider total width leads to higher gain but a narrower bandwidth. The increase in peak gain gradually slows down, as shown in the figure, such as the 2 dB increase from 10 fingers to 15 fingers and the 1 dB increase from 20 fingers to 25 fingers. Despite consuming the same power, the gain increases by only 1 dB. Considering the trade-off between bandwidth and gain, a width of 2*20 μm is ultimately selected.

doi:10.6342/NTU202402726

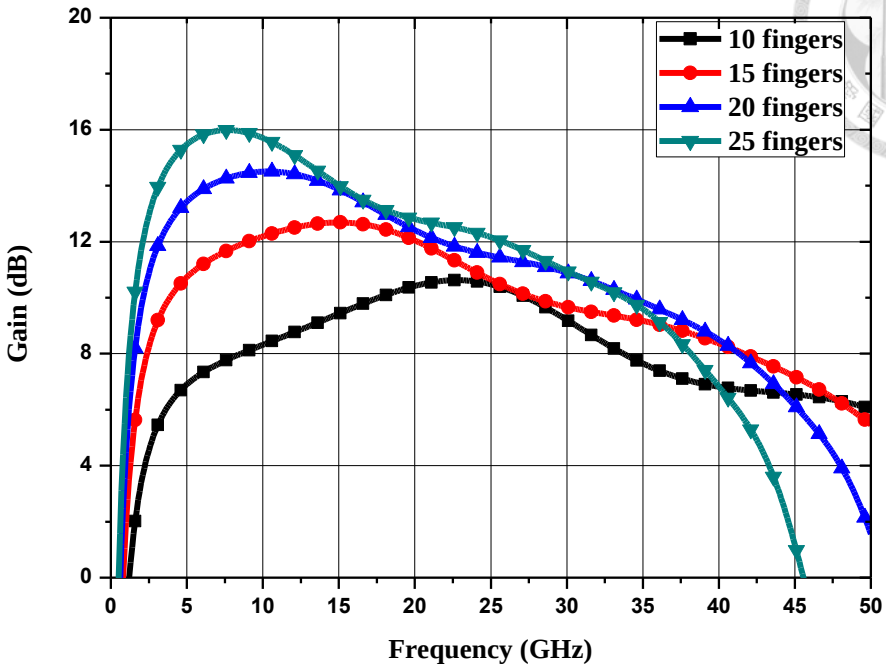

Fig. 2.5. Performance with different finger numbers.

2.4 Number of Stage Considerations

After finalizing the selection of transistor sizes, the next step is to determine the number of stages to be used. According to formula (2.2), having more stages can result in higher gain. However, when more non-ideal inductors are connected in series, there is an increase in loss, and the increase in gain will be offset, leading to a decrease in the overall amplification [5].

Based on the simulated configuration shown in Fig. 2.6, compare the performance of this distributed amplifier at different numbers of stages. As shown in Table 2.1 and Fig. 2.7, when the number of stages, n, increases from 3 to 4, the peak gain increases by nearly 3 dB, but the increase from 4 to 5 stages results in only a 2 dB increment in peak gain. Simultaneously, power consumption similarly increases.

doi:10.6342/NTU202402726

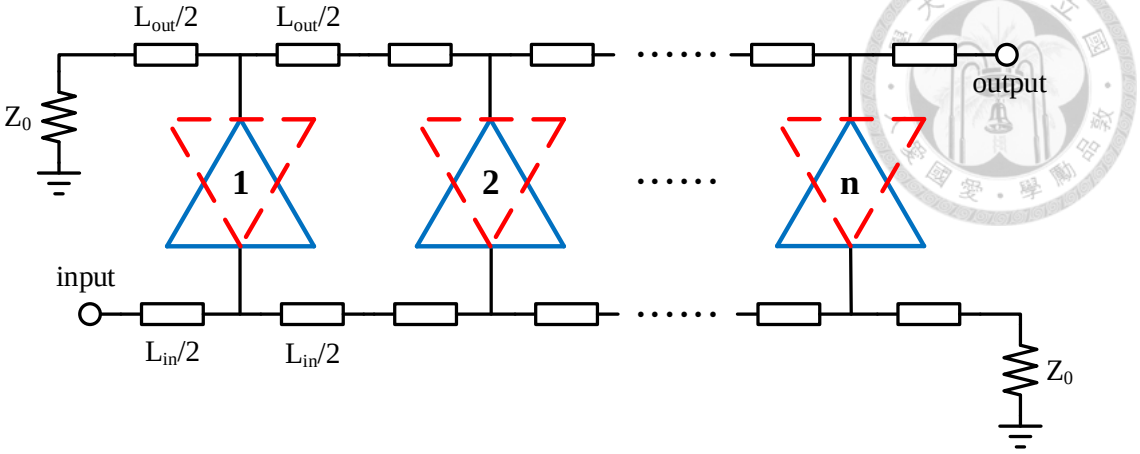

Fig. 2.6. Illustration of n stages.

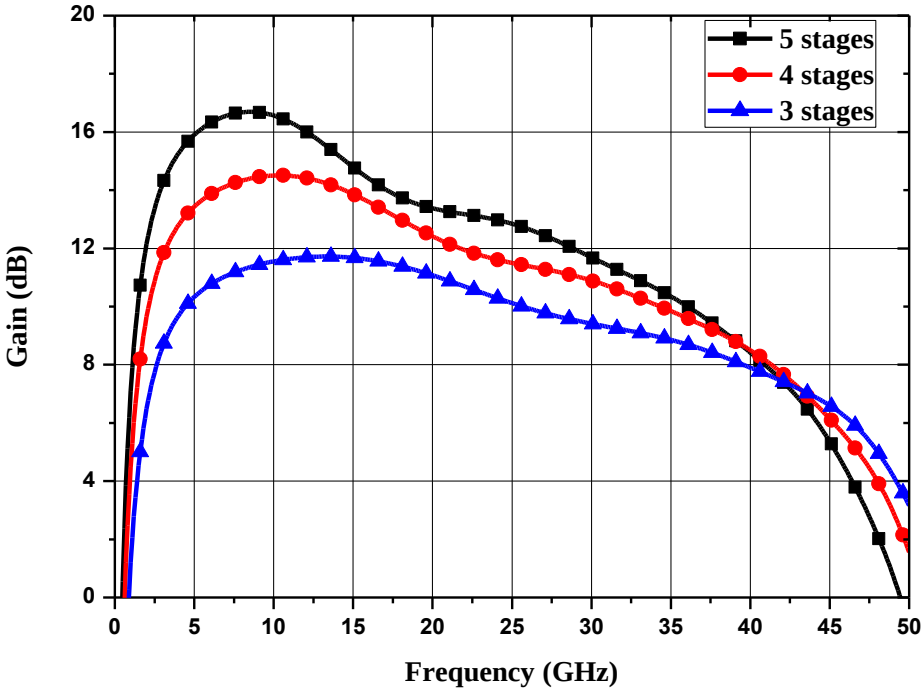

Fig. 2.7 Gain performance with different stage numbers.

doi:10.6342/NTU202402726

Table 2.1 The gain and power consumption provided by different stages n.

Stage number n	Peak gain (dB)	Power consumption (mW)
3	11.7	79.4
4	14.5	105.8
5	16.7	132.3

During the simulation, it was also observed that as the number of stages increases, the noise figure (NF) improves, as shown in Fig. 2.8. However, from both gain and NF, the bandwidth decreases as the number of stages increases. After a trade-off between power consumption, gain, and NF, it was determined that 4 stages would be the better choice.

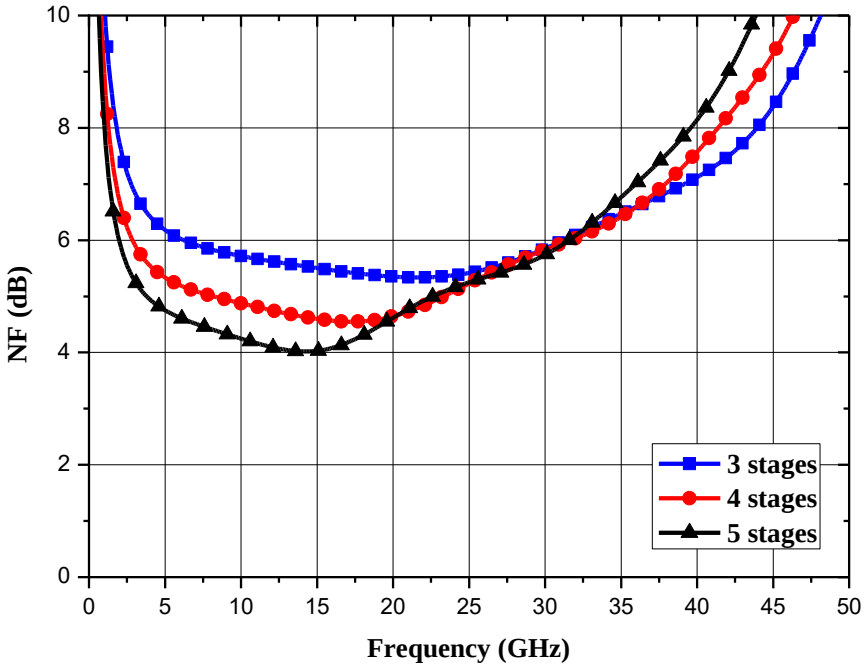

Fig. 2.8 NF performance with different stage numbers.

doi:10.6342/NTU202402726

2.5 Bias Selection

The earlier simulations were based on the transistor's maximum transconductance (g_m) bias point of 0.7 V. The original DA already consumed considerable DC power, and a moderate adjustment of the bias point could be utilized to reduce power consumption without a significant drop in gain.

Fig. 2.9 shows the schematic of a single cascode using to find a better bias point. Investigating a cascode at the center frequency of 16 GHz by sweeping $V_{g1,}$ as shown in Fig. 2.10, revealed the presence of a minimum point in NF_{min} between 0.4 V and 0.5 V. Selecting 0.5 V resulted in a decrease in NF_{min} from 1.7 dB at 0.7 V to 1.4 dB, with minimal changes in G_{max}. Implementing this selected voltage in the DA design reduced the overall power consumption from 106 mW to 46 mW. Moreover, the noise improved with the decrease in bias, while the gain remained relatively unchanged.

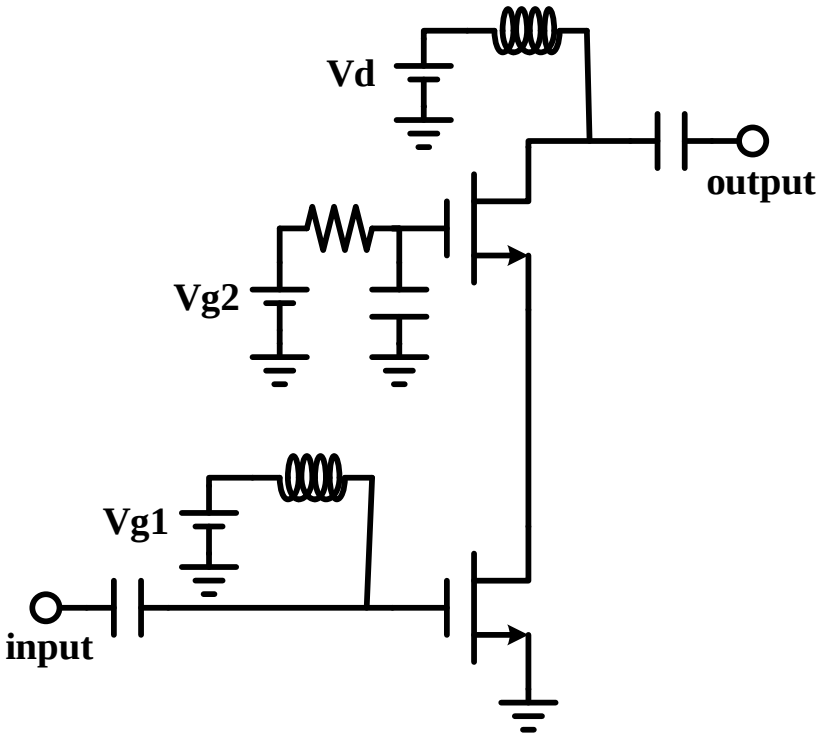

Fig. 2.9 Schematic of the simulation circuit.

doi:10.6342/NTU202402726

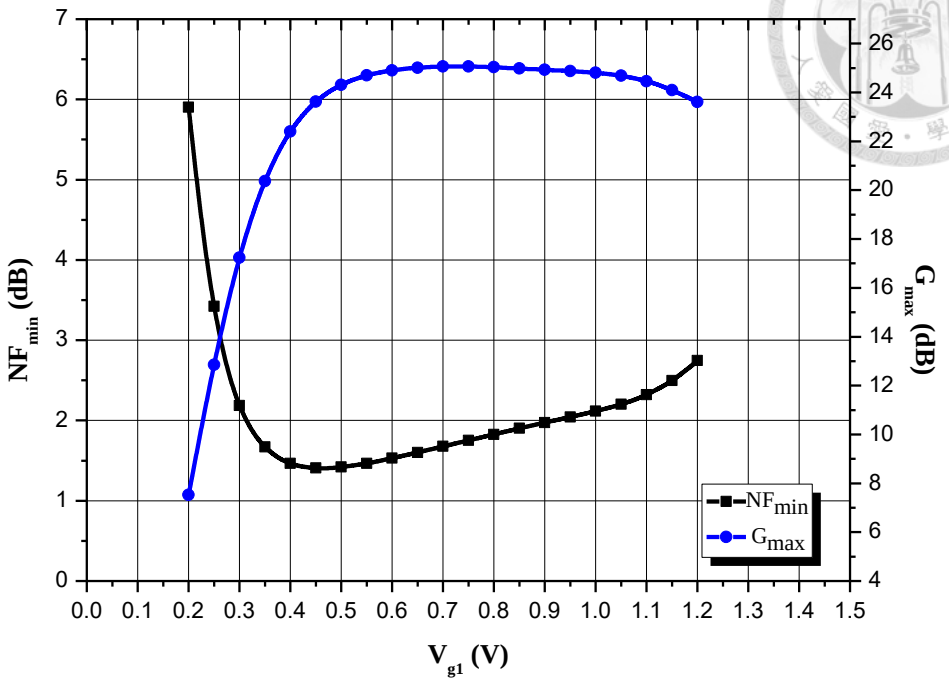

Fig. 2.10 NF_{min} and G_{max} vs V_{g1}.

2.6 G_m Cell Design

2.6.1 Resonate Inductor Design

After the critical parameters of the majority of the DA design were chosen, further efforts were made to enhance the characteristics of the gain cell. Placing an inductor between common source (CS) and common gate (CG) in the cascode architecture is a common approach, as shown in Fig. 2.11, utilizing the inductor to resonate and mitigate the influence of parasitic capacitance [8], [30]. According to [30], the impedance looking in node X(Z_x) can be written as

$$Z_x = \frac{s^2 L C_{p0} + 1}{s(C_{p1} + C_{p0} - \omega^2 L C_{p0} C_{p1})} \tag{2.3}$$

The best performance will occur when Z_x is approximately zero, which can be obtained after the calculation of (2.3)

doi:10.6342/NTU202402726

$$L = \frac{C_{p0}+C_{p1}}{\omega^2 C_{p0} C_{p1}} \quad (2.4)$$

According to (2.4), the influence of parasitic capacitance will be eliminated by L_m. As shown in Fig. 2.12, at 30 GHz, the presence of L_m at 250 pH resulted in 12.2 dB gain, compared to 10.4 dB at L_m of 50 pH, indicating better gain and a 0.6 dB increase in peak gain at 12 GHz. Due to its potential to improve gain performance and enhance the 3 dB bandwidth, the choice was 250 pH inductor for L_m.

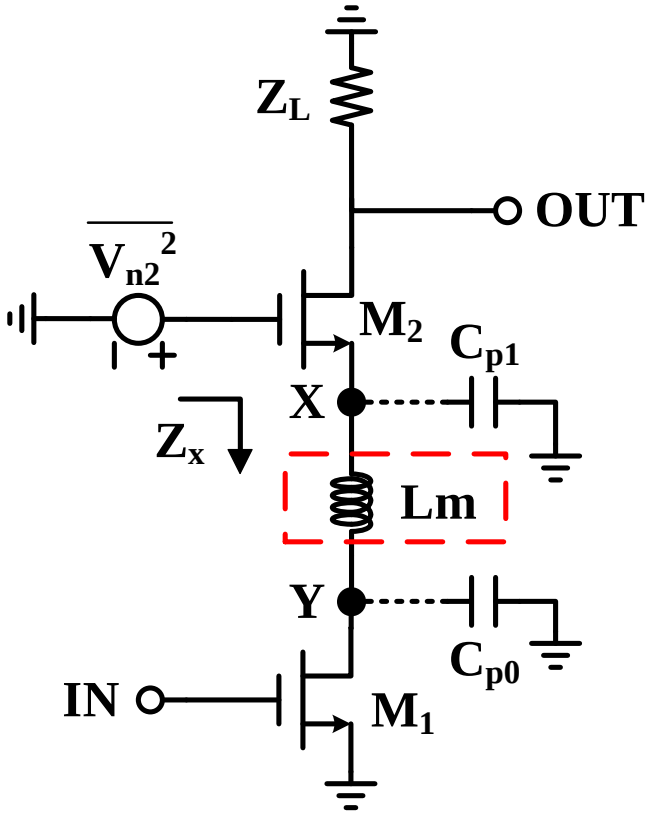

Fig. 2.11 L_m in cascode structure.

doi:10.6342/NTU202402726

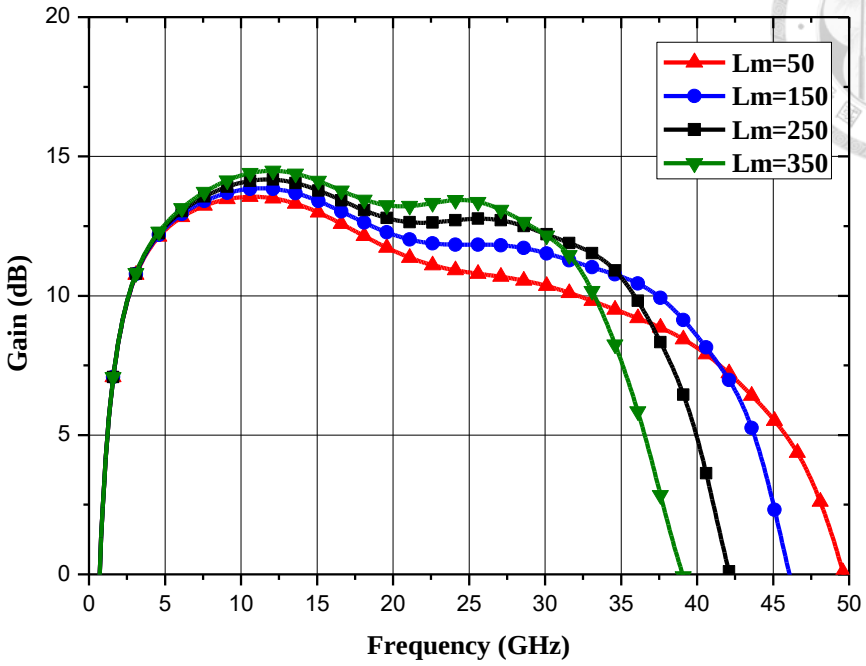

Fig. 2.12 Gain performance by using different L_m.

2.6.2 Positive Feedback Design

By placing an inductor at the gate terminal of CG in the cascode architecture, as shown in Fig. 2.13, this inductor can be used for positive feedback to increase the MSG of the cascode structure [8], enabling the circuit to perform better at high frequency. Adding an inductor L_g in Fig. 2.14 resulted in smoother overall gain and wider bandwidth. The gain increased from 10.7 dB to 12.4 dB at 35 GHz. However, the gain was achieved through positive feedback, which resulted in a trade-off between stability and gain. To ensure stability and avoid the risk of oscillation, an inductor value of 80 pH was selected.

doi:10.6342/NTU202402726

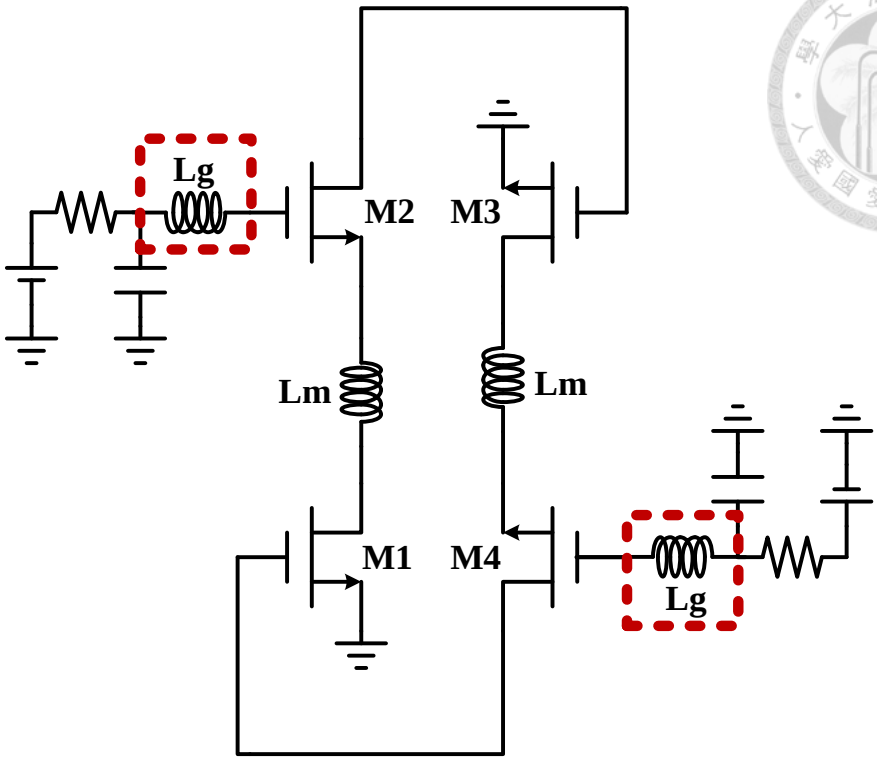

Fig. 2.13 L_g in cascode structure.

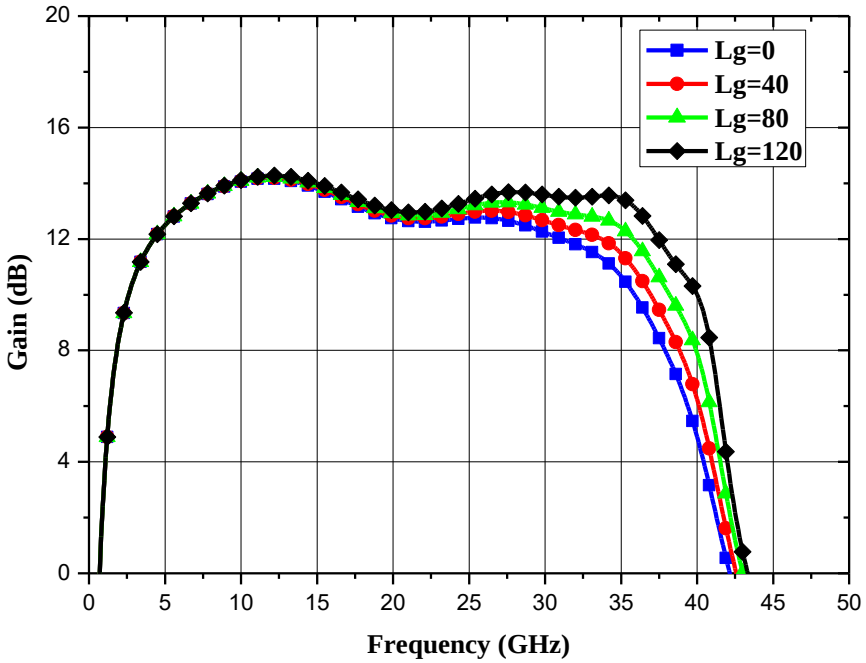

Fig. 2.14 Gain performance by using different L_g.

doi:10.6342/NTU202402726

2.7 Gate Line and Drain Line Design

In order to achieve a bidirectional design with equivalent impedances seen from both ports, traditionally, the inductor values on the gate and drain lines needed to be the same, as shown in Fig. 2.15. However, this approach limited the adjustment of the distributed amplifier's matching, resulting in only one variable for tuning. Therefore, this design employed a skew-symmetrical approach to adjust the inductor values [28], sacrificing some return loss performance in exchange for higher and flatter gain, as depicted in Fig. 2.16. According to Fig. 2.17, it can be observed that the conventional method results in a 1.5 dB gain variation within the bandwidth, whereas the skew-symmetrical approach remains consistent. Moreover, the gain can be approximately 1 dB higher than the conventional method. According to Fig. 2.18, there is a 0.4 dB improvement at the lowest point in NF. This design not only ensured the symmetry of the circuit but also provided N+1 variables for adjusting the performance, enabling us to achieve higher gain, lower gain variation, and an improved noise figure.

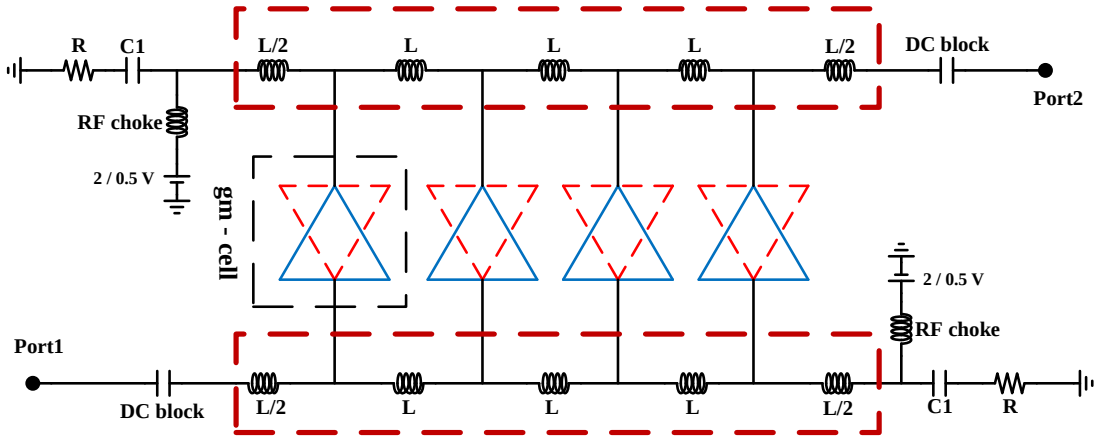

Fig. 2.15 Conventional method BDDA.

doi:10.6342/NTU202402726

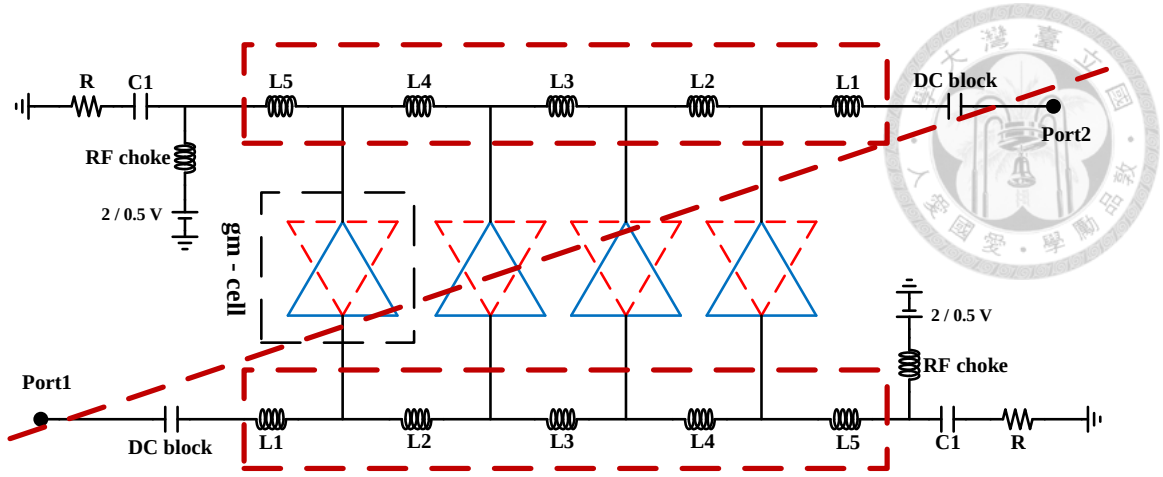

Fig. 2.16 Skew-symmetrical method BDDA.

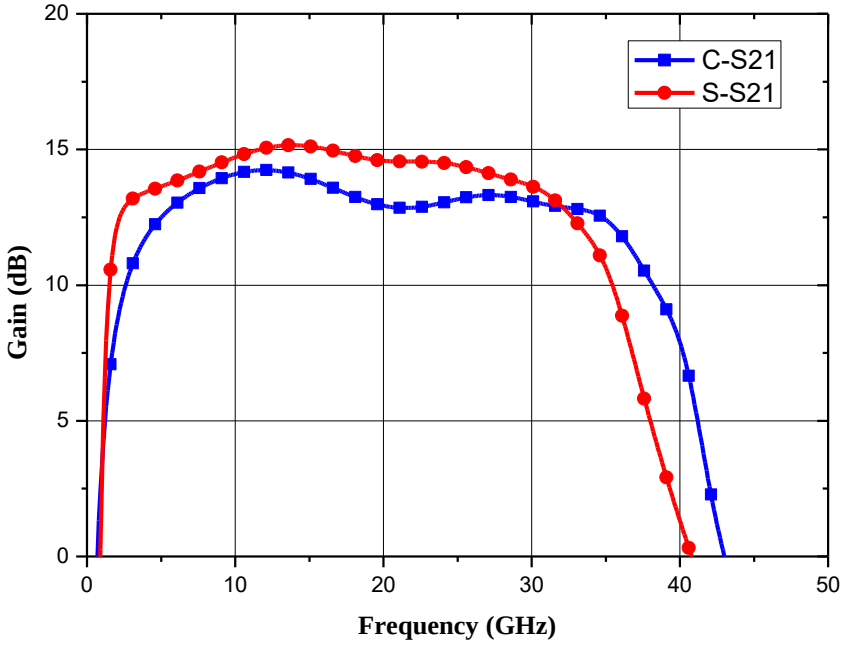

Fig. 2.17 Comparison of gain of conventional method BDDA and skew-symmetrical method BDDA.

doi:10.6342/NTU202402726

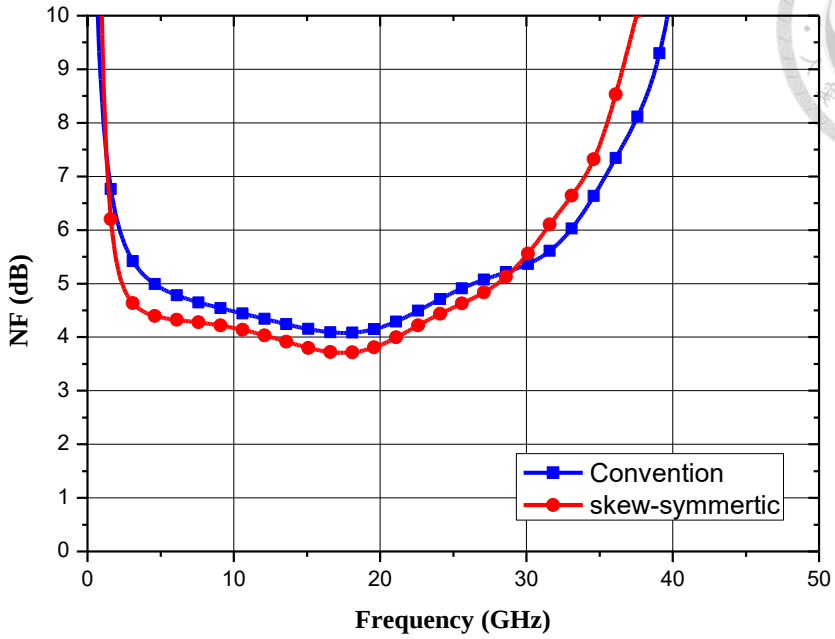

Fig. 2.18 Comparison of NF of conventional method BDDA and skew-symmetrical method BDDA.

2.8 RF Choke Design

In this design, to ensure that the artificial transmission lines (ATLs) see a 50 ohm termination, we should not only place bypass capacitance on the DC path, as it could lead to the circuit seeing RF ground, resulting in a very low matching impedance. To address this issue, only large inductors or λ/4 transmission lines can be used in the bias path of V_d to achieve a high impedance for RF signals. As shown in Fig. 2.20, although the performance of the ideal λ/4 transmission line is better than that of the ideal inductor at a specific frequency, the overall bandwidth is much narrower [9]. The λ/4 transmission line can only achieve this purpose in a very narrow frequency range, making using an inductor the only viable option.

doi:10.6342/NTU202402726

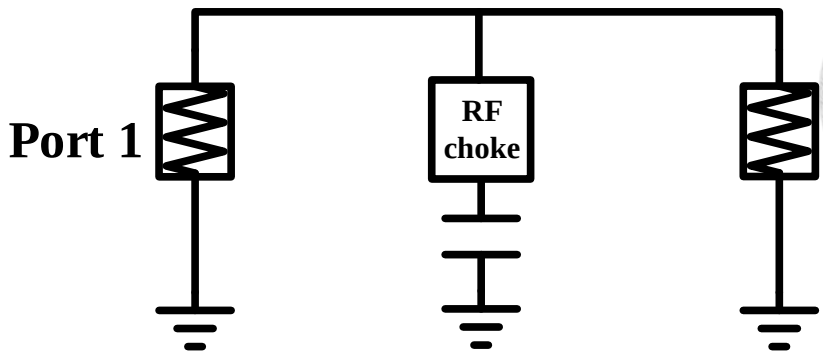

Fig. 2.19 RF choke simulation setup.

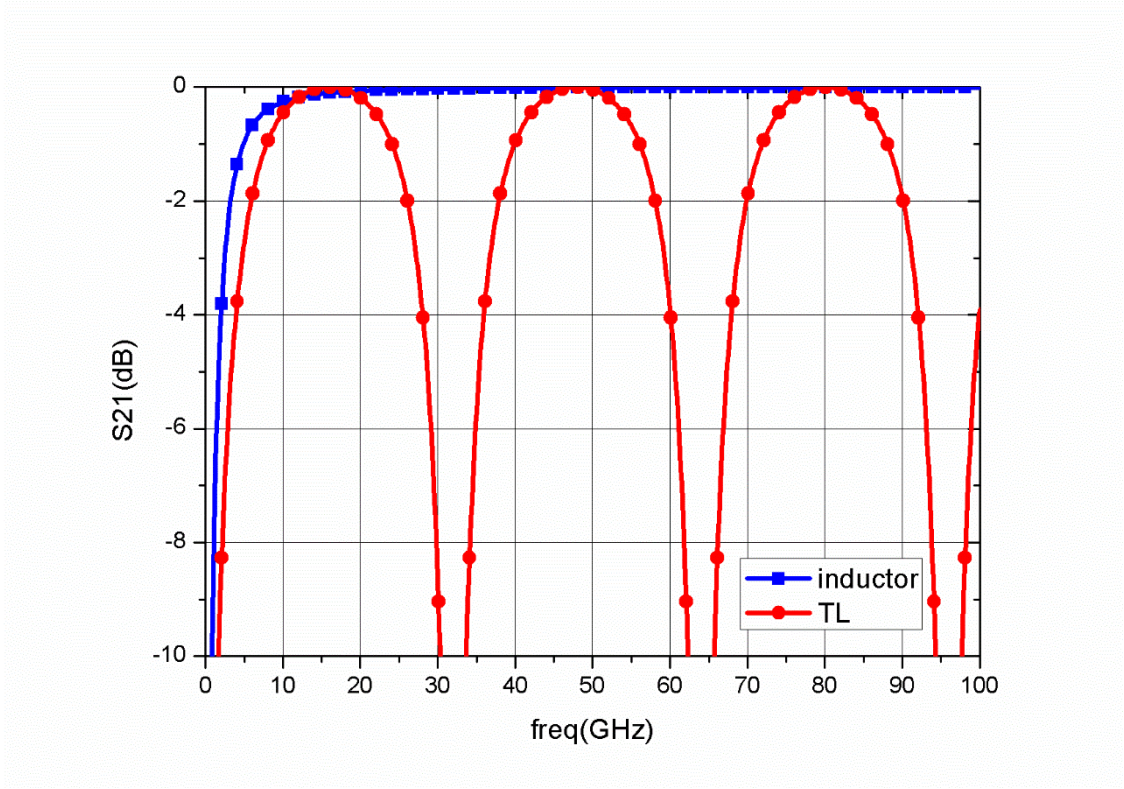

Fig. 2.20 Comparing bandwidth between RF chokes utilizing transmission line and inductor.

doi:10.6342/NTU202402726

To achieve the desired RF choke effect, an appropriate large inductor was selected. Since the target of BDDA maximum frequency is 30 GHz, efforts were made to ensure that the self-resonance frequency (SRF) of this large inductor is approximately 30 GHz. Fig. 2.22 shows that the EM simulation result of the inductor has a value of 1.6 nH and a self-resonance at 32 GHz. From Fig. 2.23, a comparison of the EM results of S21 for the λ/4 transmission line and the large inductor shows that the inductor has better performance in both bandwidth and loss.

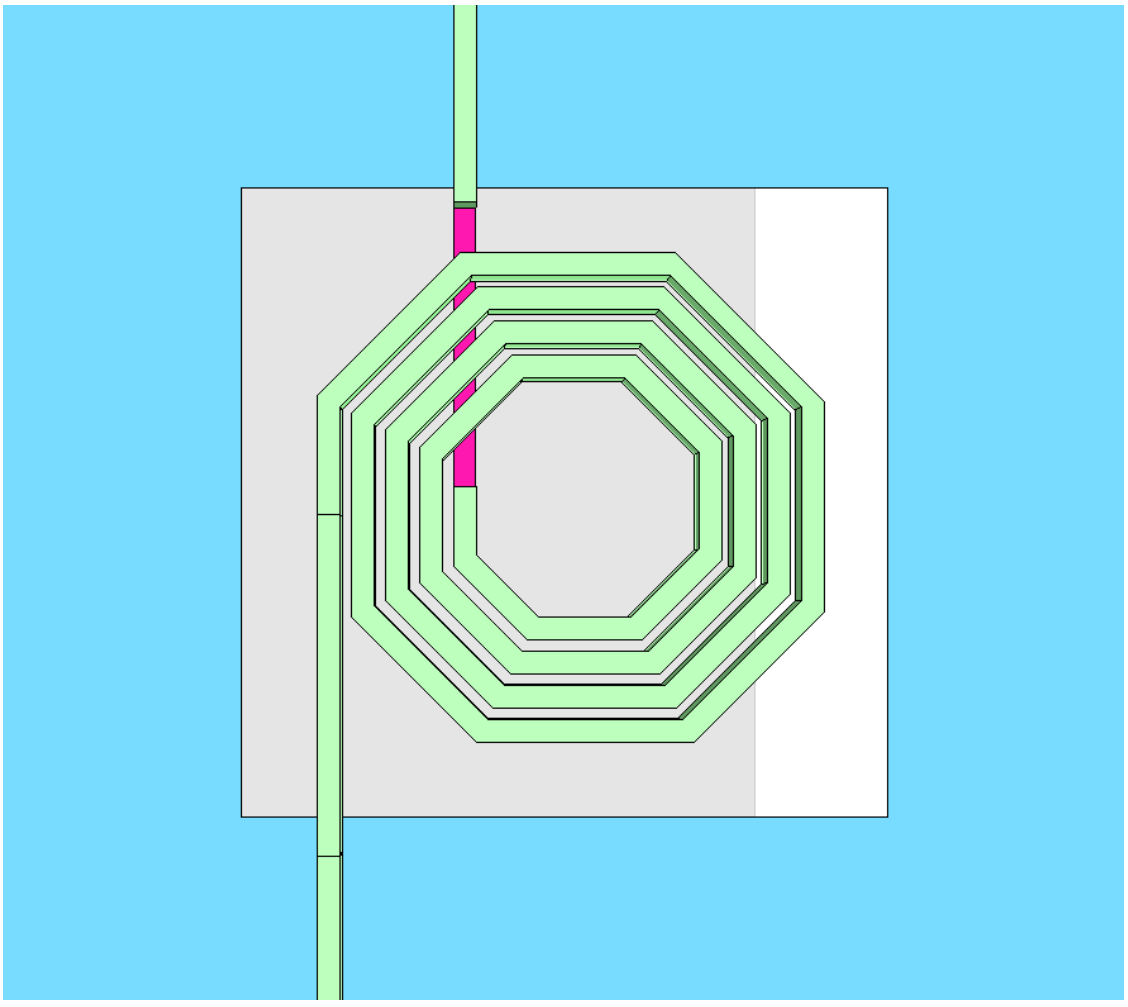

Fig. 2.21 The appearance of the RF choke.

doi:10.6342/NTU202402726

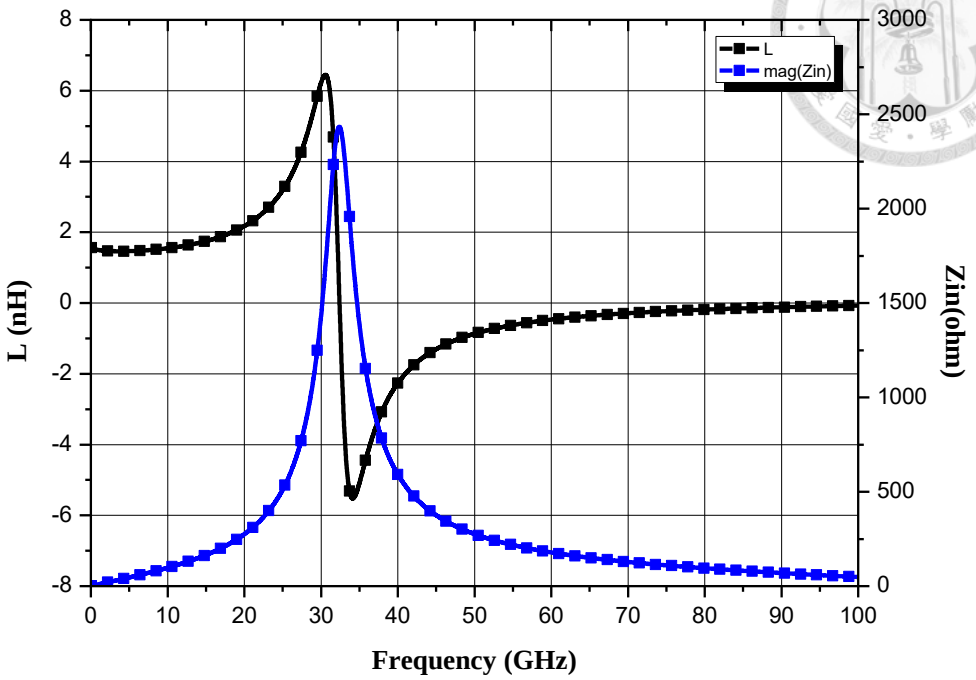

Fig. 2.22 Inductance and Q value of inductor.

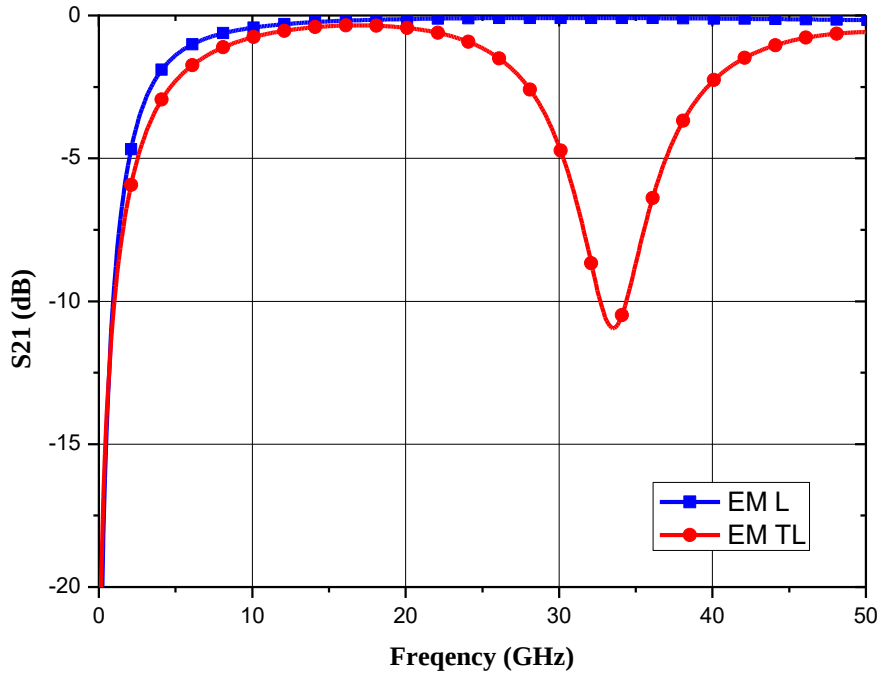

Fig. 2.23 The S21 of the transmission line and inductor's EM results.

doi:10.6342/NTU202402726

2.9 Circuit Schematic and Post-Simulation Result

After the pre-simulation, performing electromagnetic simulations (EM) using Sonnet becomes crucial, as ideal simulations do not account for the self-resonance frequency. In contrast, EM simulations consider the impact of parasitic effects. Firstly, individual simulations are conducted to adjust the inductor values on the gate line and drain line, followed by a comprehensive simulation, as shown in Fig. 2.24, to ensure that mutual inductance and other parasitic effects do not affect the circuit performance. Next, the EM simulation of the central Gm cell is carried out, primarily aiming to ensure that mutual influences between the two L_g do not lead to variations in circuit performance, as shown in Fig. 2.25. Then, for a better matching, change the DA terminal resistance R from 50 ohm to 43 ohm. Finally, the bypass, RF choke, and terminal resistor are simulated together as shown in Fig. 2.26 (a). The simulation results of these three parts combined are shown in Fig. 2.26 (b). S21 shows that the RF choke has good isolation, and S11 shows the matching results of the terminal resistor in a wide frequency range.

The overall circuit schematic of the proposed bidirectional distributed amplifier is shown in Fig. 2.27. Fig. 2.28, Fig. 2.29, and Fig. 2.30 depict the S-parameter simulation results of this BDDA at a V_d bias under 2 V, with a total current of 22.9 mA. The BDDA exhibits a peak gain of 13.2 dB and a 3 d B bandwidth of 30.4 GHz from 1.7 to 32.1 GHz, with gain variation controlled within ±0.5 dB between 3 and 30 GHz. Return losses within the simulated bandwidth range from 5.8 to 18.2 dB at the input port and 6.3 to 24.8 dB at the output port. These three plots indicate that the S-parameters behave almost identically, confirming that the bidirectional design meets the initially established design goal, with consistent results observed in both forward and reverse directions. The isolation of cascode architecture from DC to 30GHz is less than -30 dB, and the total gain of this DA

doi:10.6342/NTU202402726

is 13 dB. After passing through the cascode structure, there is no loop gain to cause instability. Fig. 2.31 shows that the NF reaches a minimum of 4.3 dB at 13 GHz and remains below 5 dB between 2.8 and 23 GHz, exhibiting consistently low values across the entire frequency range rather than at a specific frequency. The group delay (GD) is shown in Fig. 2.32. It varies within ±30 ps between 3 and 30 GHz. The gain and output power versus input power at 5 GHz are shown in Fig. 2.33, while Fig. 2.34 illustrates the simulated OP_{1dB} from 3 to 30 GHz, with the highest point at 7.2 dBm at 5 GHz, consistently above 5.8 dBm overall. The chip layout of the proposed BDDA is shown in Fig. 2.35. The entire chip area, including all pads, is 1.24×0.75 mm^2.

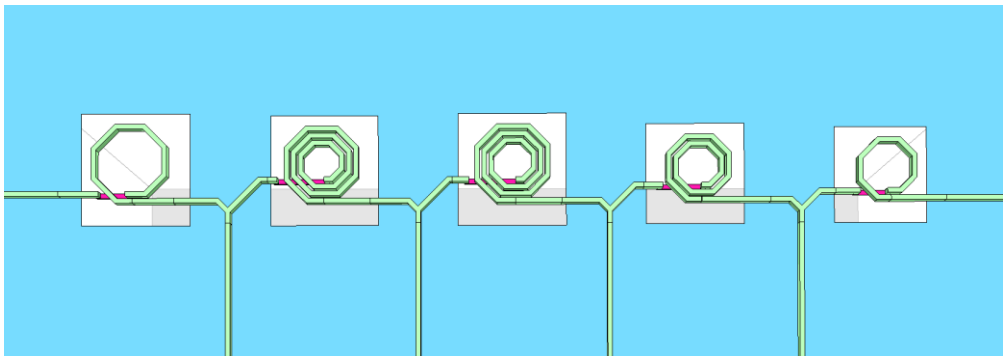

Fig. 2.24 EM simulation of series inductor.

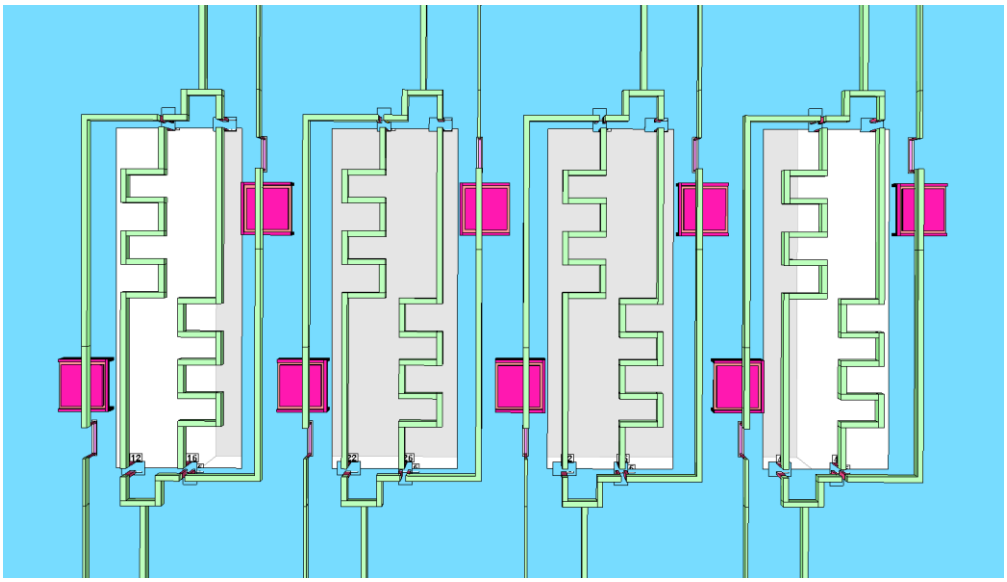

Fig. 2.25. EM simulation of G_m cells.

doi:10.6342/NTU202402726

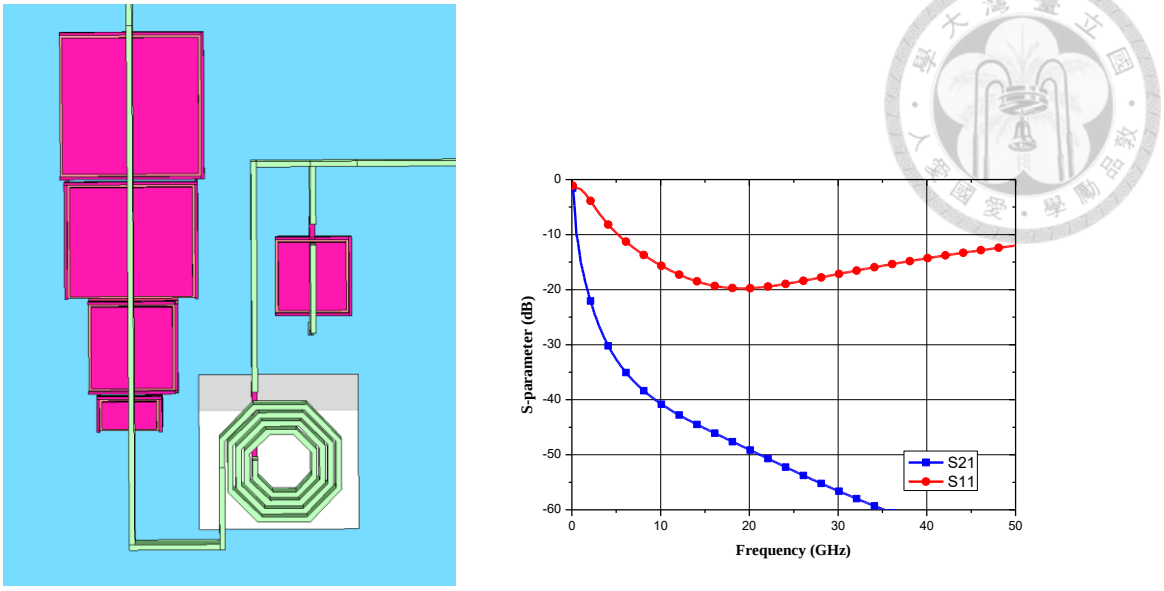

Fig. 2.26. (a) EM simulation of bypass, RF choke, and terminal resistor. (b) S-parameter of bypass, RF choke, and terminal resistor.

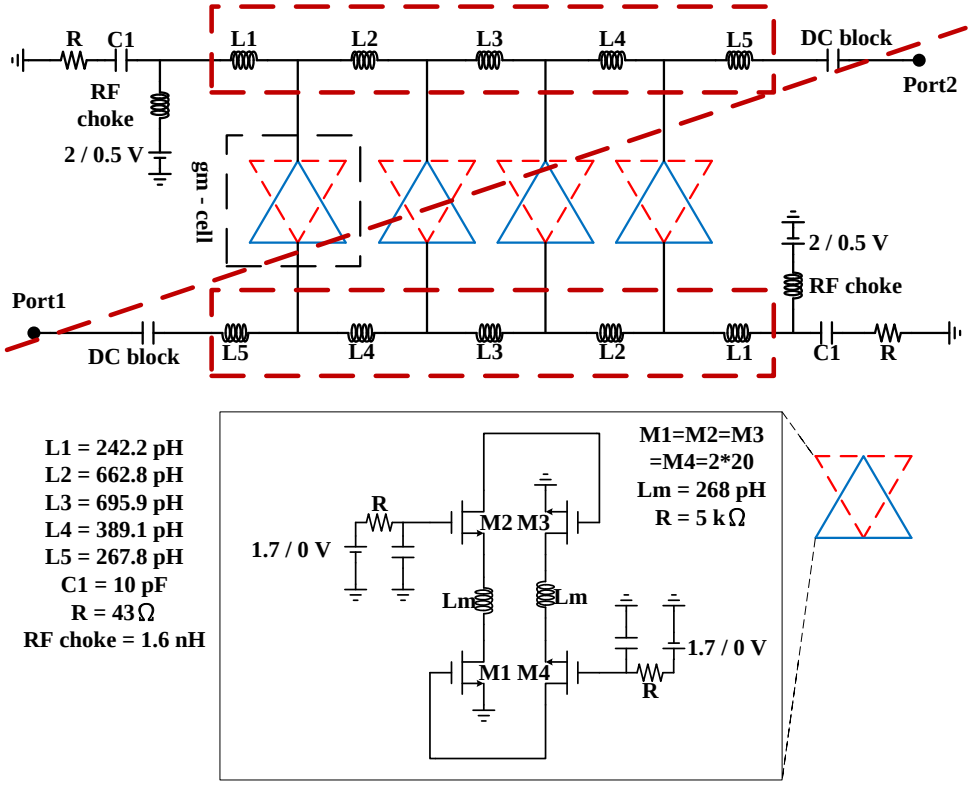

Fig. 2.27. Total Schematic of the BDDA.

doi:10.6342/NTU202402726

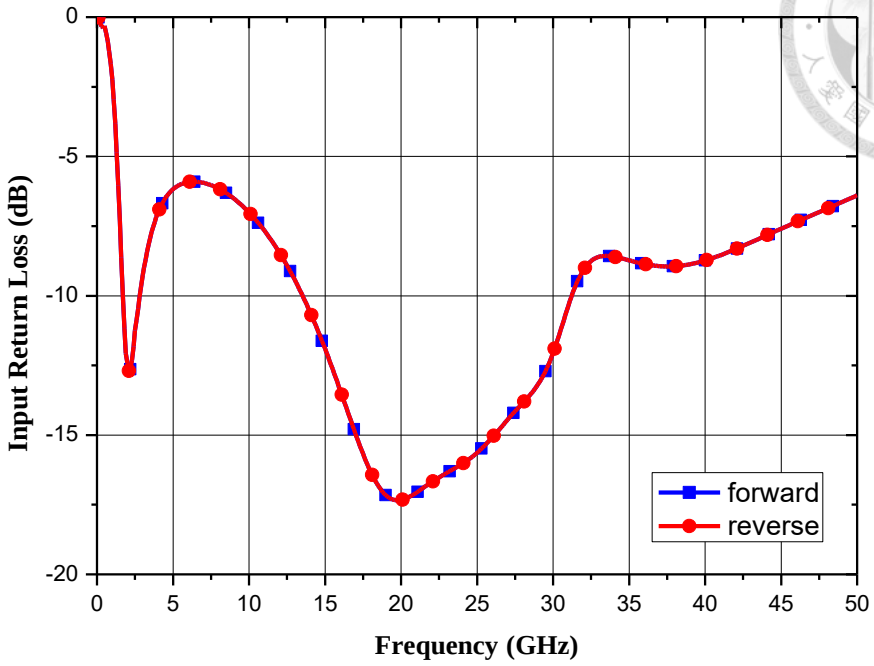

Fig. 2.28 Simulated results of the forward and reverse S11 of the BDDA.

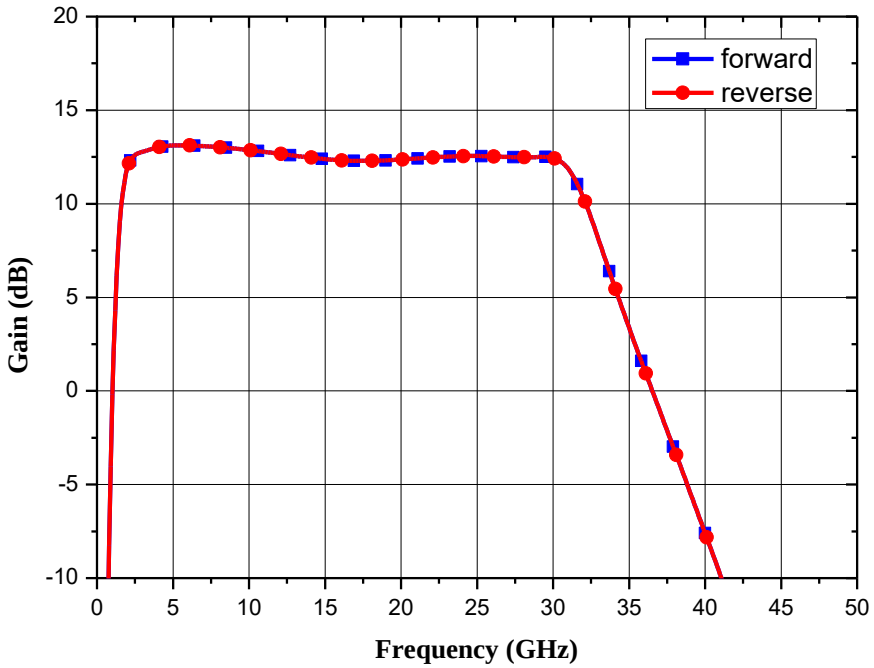

Fig. 2.29 Simulated results of the forward and reverse gain of the BDDA.

doi:10.6342/NTU202402726

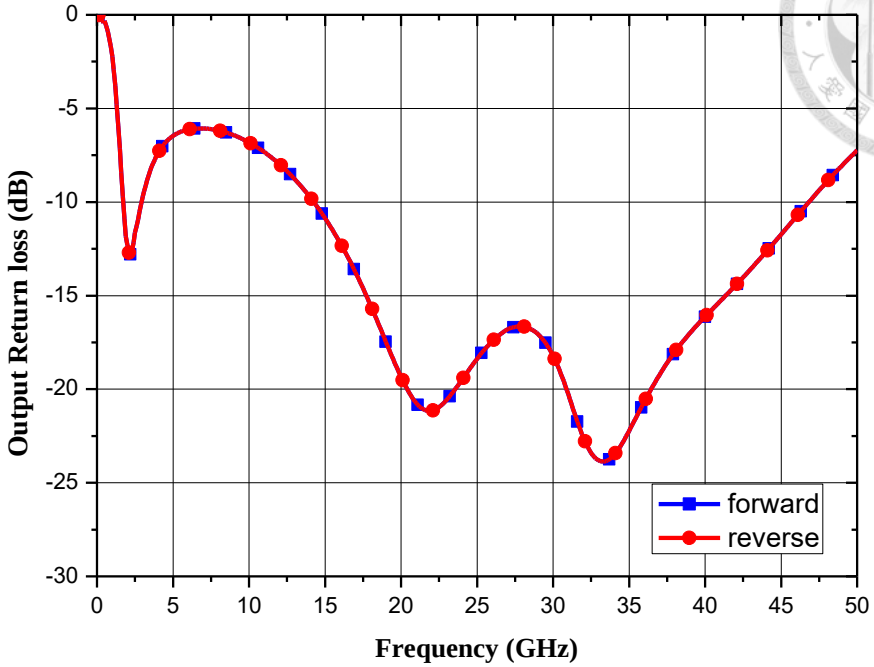

Fig. 2.30 Simulated results of the forward and reverse S22 of the BDDA.

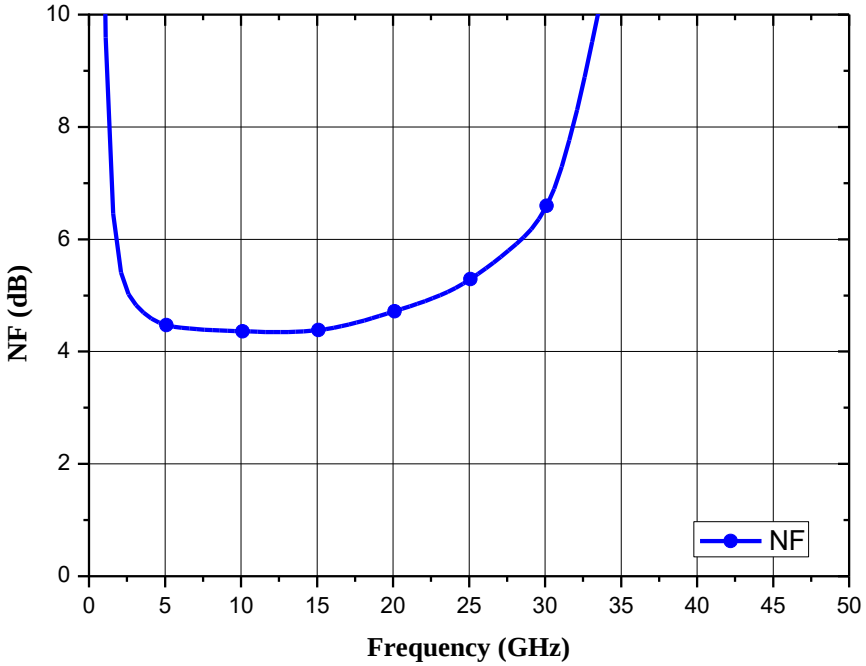

Fig. 2.31 Simulated result of NF of the BDDA.

doi:10.6342/NTU202402726

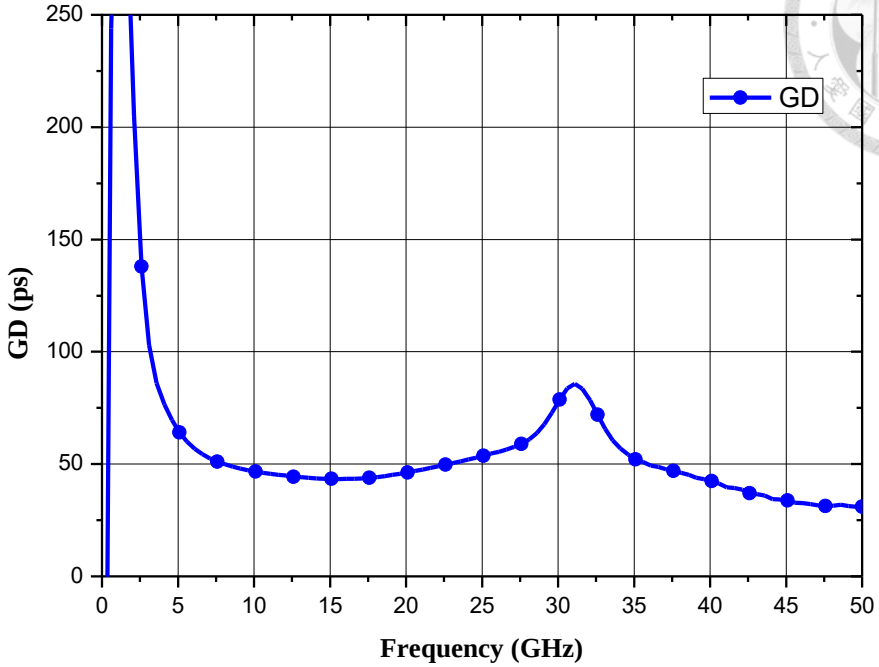

Fig. 2.32 Simulated result of group delay of the BDDA.

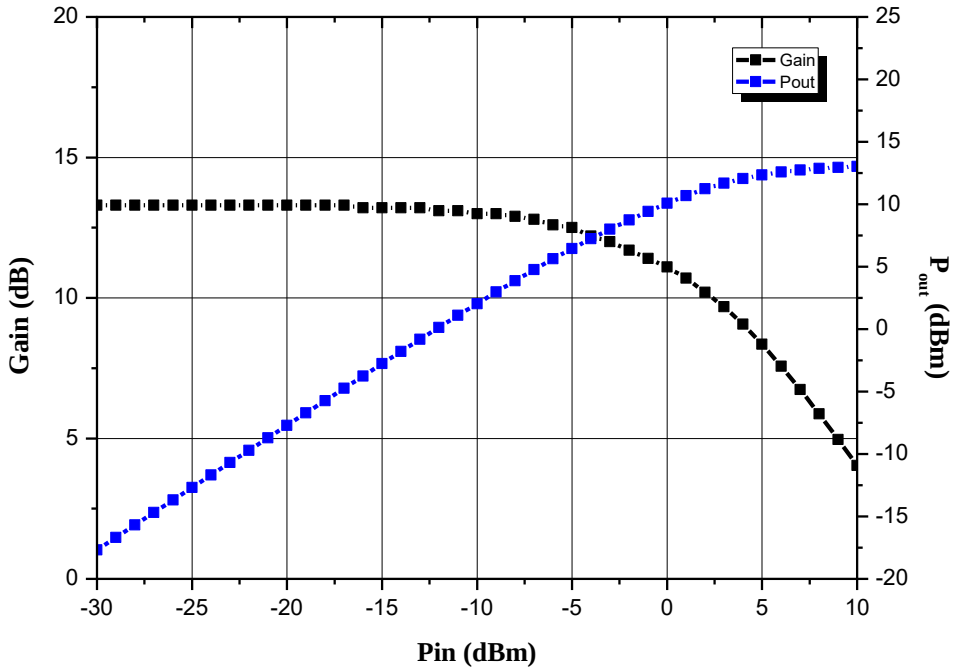

Fig. 2.33 Simulated large signal of the BBDA at 5 GHz.

doi:10.6342/NTU202402726

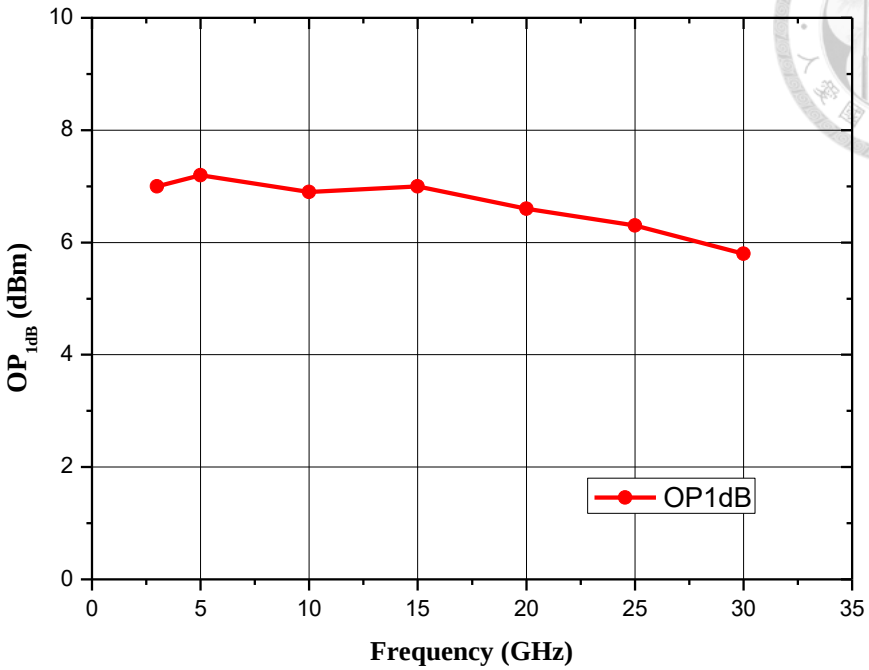

Fig. 2.34 Simulated large signal of the BBDA from 3 to 30 GHz.

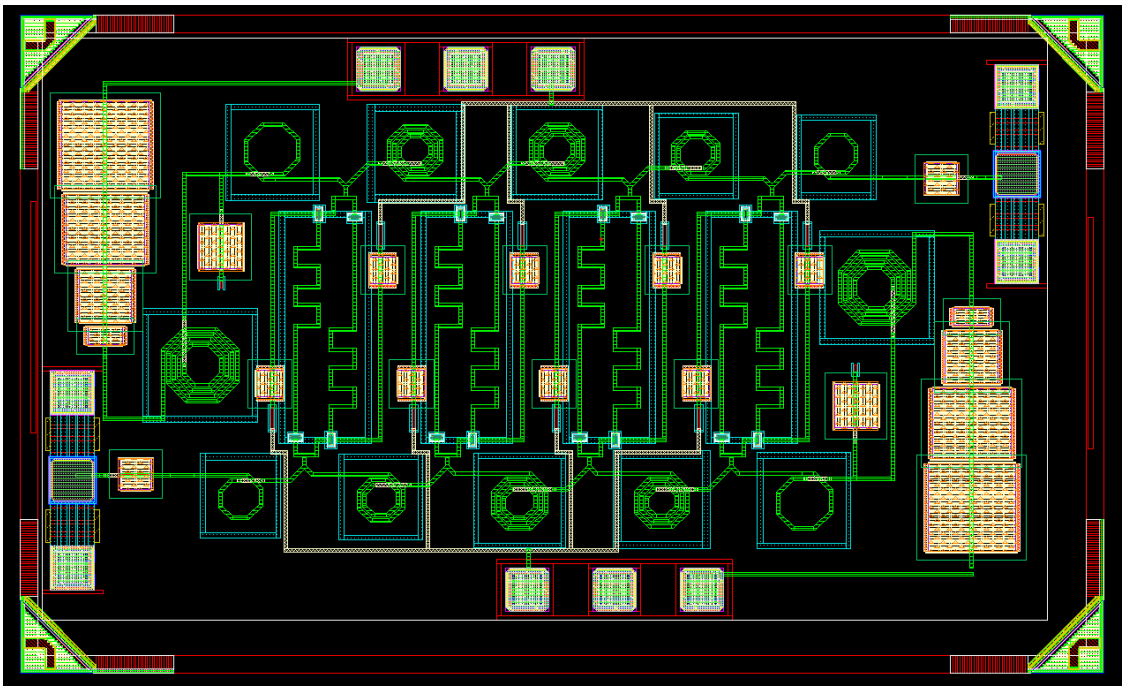

Fig. 2.35 The layout of the BDDA

doi:10.6342/NTU202402726

2.10 Measurement Result

The proposed bidirectional DA is implemented using TSMC 90-nm GP CMOS process. Fig. 2.36 shows the micrograph of the fabricated chip. The area of this circuit is 1.24×0.75 mm^2 including DC and RF pads. The drain bias V_d is 2 V, two gate bias V_{g2} are 1.7 V, and V_{g1} is 0.5V, respectively. The DC power consumption is 45.8 mW. During measurement, one of the transistors will have 2 V applied to its gate. It has been verified with the PDK document to ensure that the transistor gate can endure this voltage.

The measurement results are obtained through on-wafer probing. Fig. 2.37 to Fig. 2.40 illustrate the comparison of the measured S-parameters of the BDDA in forward and reverse operations. The BDDA exhibits a peak gain of 13.8 dB and a 3 dB bandwidth from 1.9 to 33.5 GHz. As there is a gain improvement at 3.5 and 31 GHz, because the ground metal in the EM simulation environment is not ideal, there may be discrepancies between the simulation results and measurement result. Regarding return loss, both S11 and S22 show better performance than 6 dB across the 3 dB bandwidth. Fig. 2.41 and Fig. 2.42 represent the NF and GD results. The measured NF ranges from 2.9 to 3.8 dB across 3 to 30 GHz. The GD variation is within ±30 ps, similar to the simulation, across the 3 to 30 GHz. Moreover, from Fig. 2.38 to Fig. 2.42, it is evident that both forward and reverse operations yield nearly identical results, affirming the effectiveness of the design. The measured OP_{1dB} spans from 3 to 30 GHz, as shown in Fig. 2.43, with the best performance of 7.4 dBm at 5 GHz and consistently higher than 5.5 dBm. From the large signal measurement, it was also confirmed that the isolation of DA will not change as the input power increases, thereby not affecting the stability.

doi:10.6342/NTU202402726

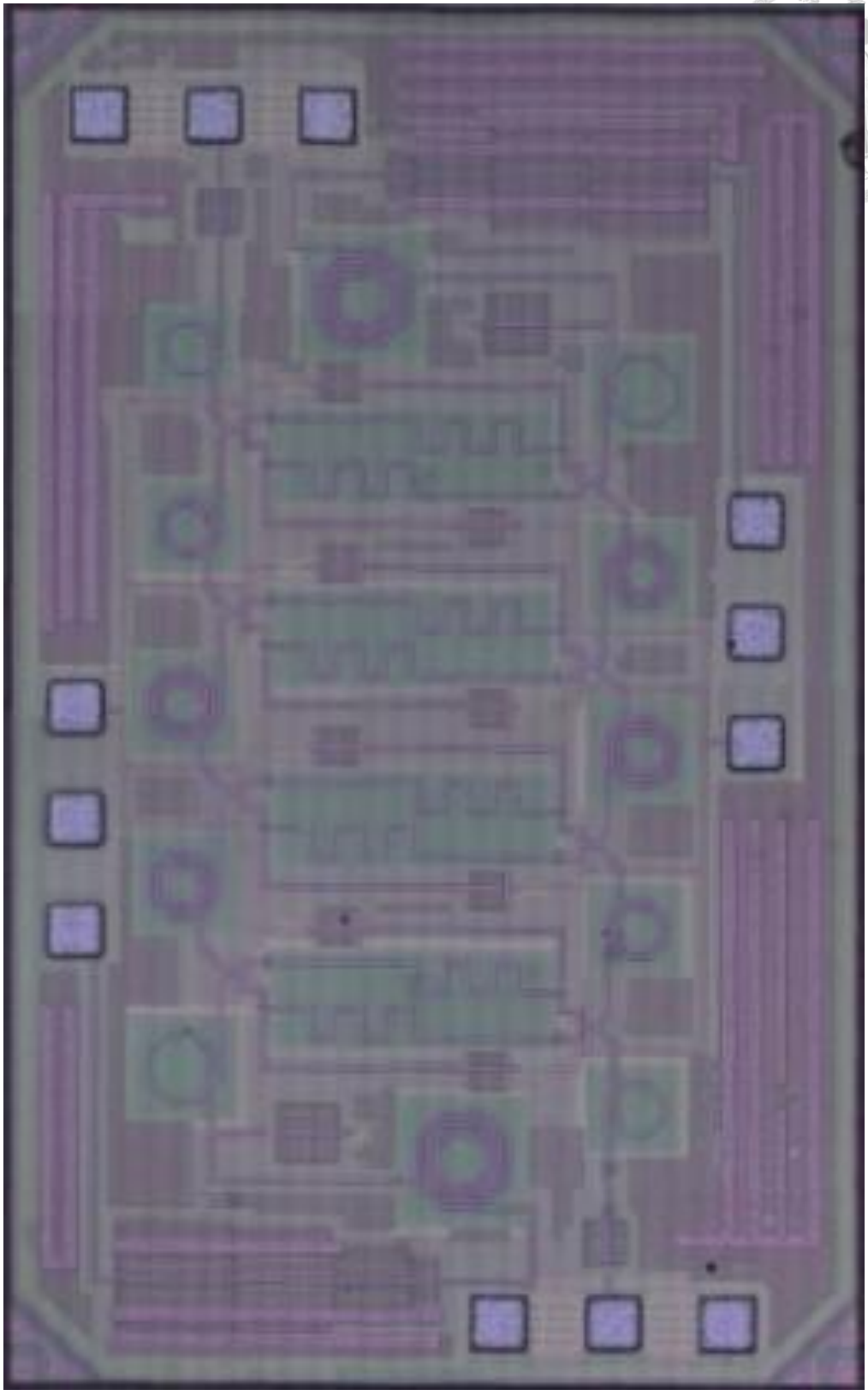

Fig. 2.36 Chip photo of the BDDA.

doi:10.6342/NTU202402726

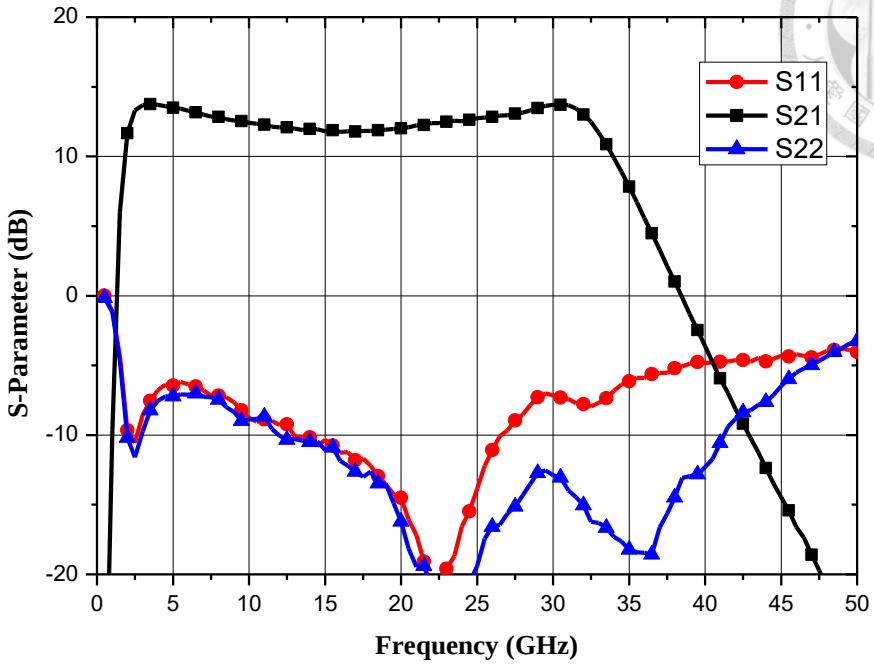

Fig. 2.37 Measured S-parameter of the BDDA.

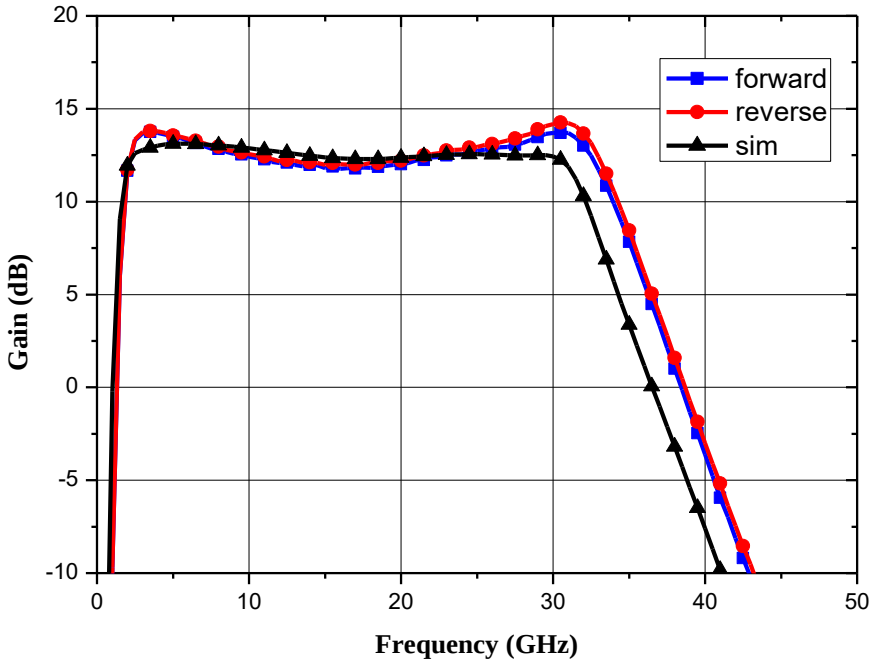

Fig. 2.38 Measurement results of the forward and reverse gain of the BDDA.

doi:10.6342/NTU202402726

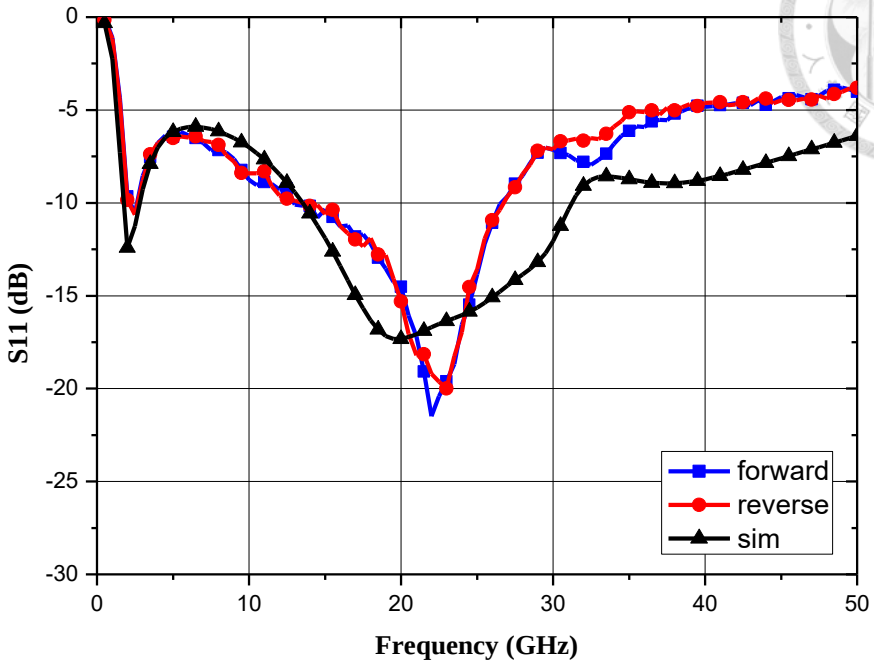

Fig. 2.39 Measurement results of the forward and reverse S11 of the BDDA.

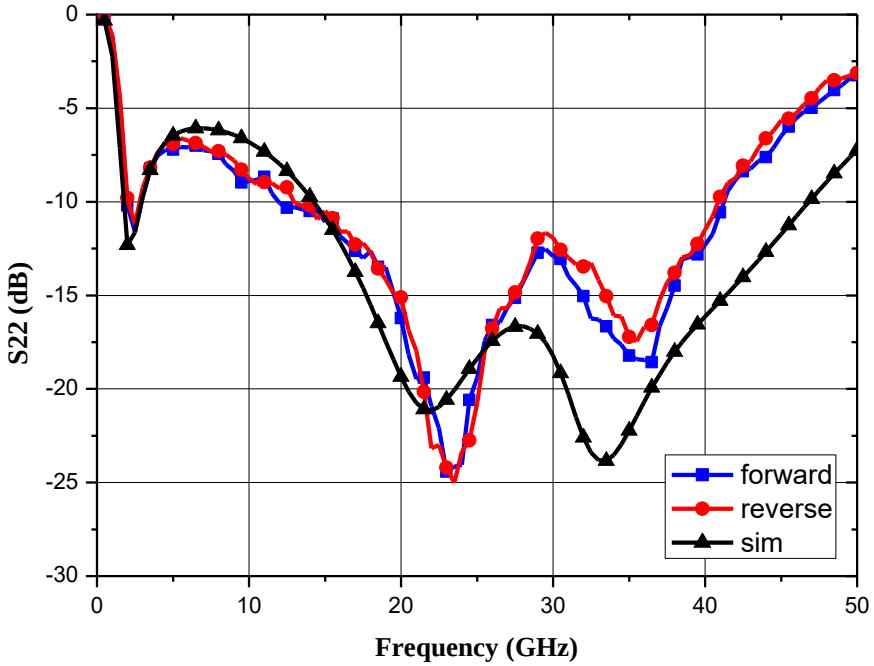

Fig. 2.40 Measurement results of the forward and reverse S22 of the BDDA.

doi:10.6342/NTU202402726

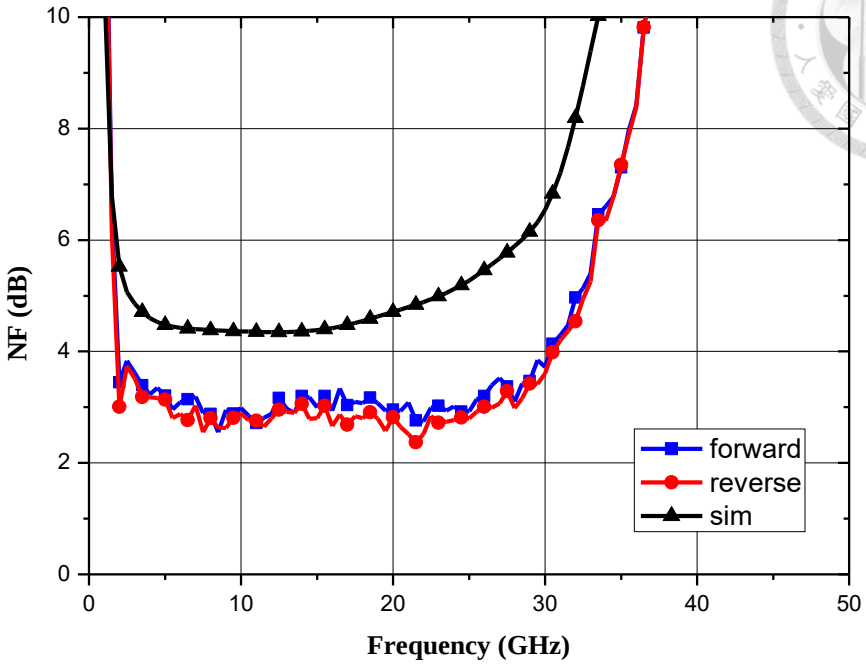

Fig. 2.41 Measurement results of the forward and reverse NF of the BDDA.

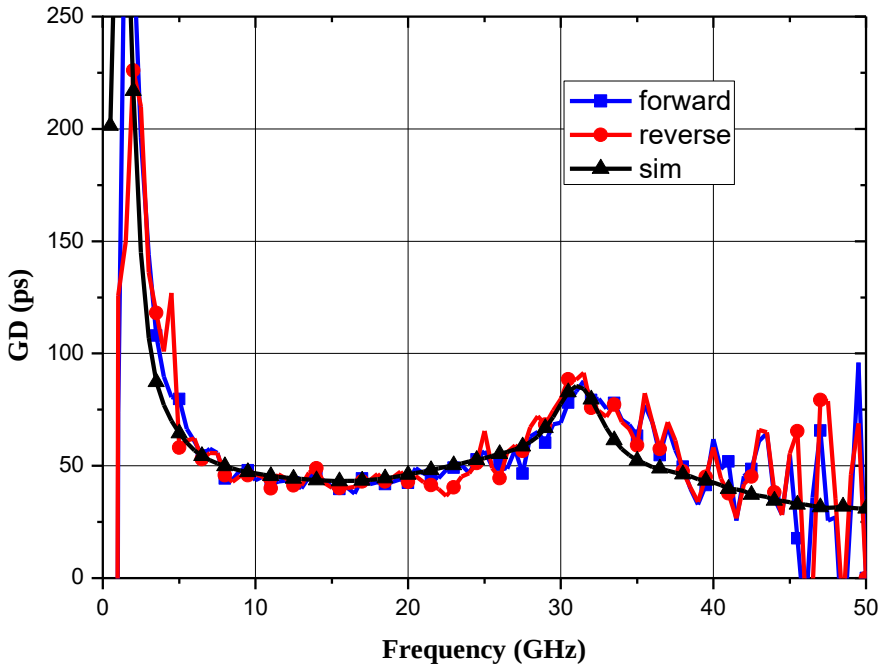

Fig. 2.42 Measurement results of the forward and reverse group delay of the BDDA.

doi:10.6342/NTU202402726

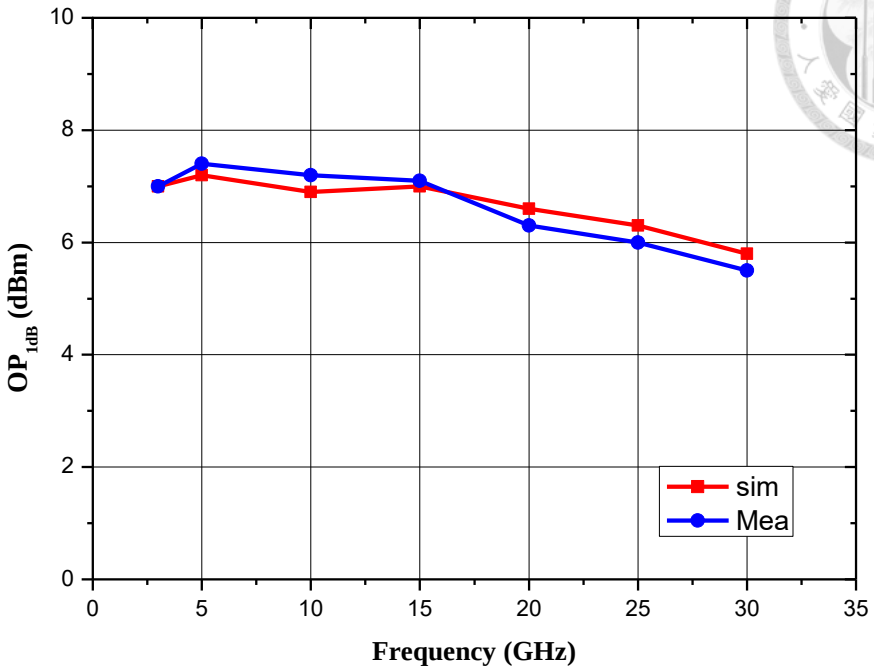

Fig. 2.43 Large signal measurement result of the BBDA from 3 to 30 GHz.

doi:10.6342/NTU202402726

2.11 Summary

In this chapter, a bidirectional distributed amplifier fabricated in 90-nm CMOS is presented. By using the skew-symmetric layout, the bidirectional DA achieves competitive performance. The 3 dB bandwidth of the proposed BDDA covers from 1.9 to 33.5 GHz. The measurement results exhibit a peak gain of 13.8 dB and a noise figure between 2.9 and 3.9 dB, with a DC power consumption of 45.8 mW. Table 2.2 summarizes the performance of the proposed BDDA and recently published BDDAs. Compared to previously published BDDAs, the proposed BDDA demonstrates superior characteristics, including higher gain, wider bandwidth, lower noise figure, and a comparable level of DC power consumption. The remarkable performance of the proposed amplifier positions it as an indispensable component for various applications. In the rapidly evolving landscape of modern high-speed communication systems, the amplifier can significantly enhance signal processing capabilities, ensuring seamless and efficient data transmission. Furthermore, in broadband radio transceivers and high-resolution imaging systems, the amplifier's superior characteristics pave the way for enhanced data reception, processing, and imaging precision[6]. This work has been published in the 2022 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT) [28].

doi:10.6342/NTU202402726

Table 2.2 Comparison table of published BDDA

Ref.	Process	BW (GHz)	Gain (dB)	GBW (GHz)	Noise Figure (dB)	OP_{1dB} (dBm)	P_{dc} (mW)	Bidirectional
[13]	0.13-μm CMOS	8.5~10.5	5.3	3.7	NA	7.4	43	Yes
[1]	0.13-μm CMOS	3~20	11	42.6	3.2~6.5	8	68	Yes
[10]	0.13-μm SiGe Bi-CMOS	2~22	9.6	60.4	4.5~5	11	100	Yes
[11]	0.13-μm SiGe Bi-CMOS	2~23	9.6	63.4	<12.7	N.A.	75	Yes
[6]	0.18-μm CMOS	2~12	9	28.2	5.9~7.4	9.5	132	Yes
[12]	0.13-μm SiGe Bi-CMOS	7~30	11.2	83.5	6~10	-2.5	13.8	Yes
This work	90-nm CMOS	1.9~33.5	13.8	154.8	2.9~3.9	7.4	45.8	Yes

doi:10.6342/NTU202402726

Chapter 3 The Design of Three Ka-band LNAs in 0.18 μm GaAs E-Mode pHEMT Process

3.1 Introduction and Circuit Specification

In this chapter, the 0.18 μm GaAs E-Mode pHEMT process(WIN PIH1-10) is utilized to design the 28 GHz LNA. This process demonstrates devices with a cut-off frequency (ft) of 100 GHz; this level of GaAs integration provides numerous options to increase MMIC functionality and enables single-chip front-end solutions with best-in-class performance at mmWave frequencies. The versatile E-mode pHEMT provides high power density and efficiency with an excellent noise figure through 40GHz. It provides two metal layers with air bridges, backside via holes, metal-insulator-metal (MIM) capacitors, capacitors on via (COV), thin film resistor (TFR) for low-value resistance, Mesa resistors for high-value resistance, and two types of transistors (microstrip (MS) type and CPW type).

Table 3.1 lists the design goals for this Low Noise Amplifier (LNA). The design targets of the LNA are 19 dB small signal gain and 2.4 dB noise figure to make sure that the sensitivity of the receiver system is guaranteed with 6GHz bandwidth between 25 and 31 GHz. Input and output return loss are both better than 10dB. Using 1.4*0.75 mm^2 area.

In the rapidly advancing field of wireless communication technology, the research and application of high-frequency communication systems are attracting increasing attention from academic and industrial communities [29]. Particularly, applications in the Ka-band, especially within the 28 GHz frequency range, have become a focal point of investigation. The utilization of this frequency range provides communication systems with broader bandwidth and higher data transfer rates, making it a crucial technology for 5G communication [22], [23].

doi:10.6342/NTU202402726

In this context, Ka-band LNAs play a critical role in communication systems, as their performance directly influences the sensitivity and efficiency of the entire system. Gallium Arsenide (GaAs) material is an ideal choice for high-frequency electronic components due to its high carrier mobility and excellent high-frequency characteristics. This study will explore leveraging the advantages of GaAs processes to design a 28 GHz LNA, aiming for lower noise and higher gain.

Table 3.1 Design goals of the 28 GHz LNA.

28 GHz LNA Goals	
Process	0.18 μm GaAs E-Mode pHEMT process(WIN PIH1-10)
Frequency	25~31 GHz
Gain	19 dB
Noise Figure	<2.4 dB
I/O Return loss	>10 dB
Chip size	1.4*0.75 mm^2

doi:10.6342/NTU202402726

3.2 Bias Selection

The drain-to-source voltage (V_{ds}) and gate voltage (V_g) selections are critical for ensuring the best possible performance from the LNA. In the common source amplifier, it is essential to operate the transistor in saturation. Fig. 3.1 illustrates the simulated DC-IV curve for a transistor with a size of 2 fingers and a total gate width of 100 μm (abbreviated as 2×50 μm throughout the thesis). The transistor enters saturation when V_{ds} exceeds 0.5 V, as shown in the curve.

Furthermore, transconductance (g_m) directly influences the small signal amplification capability of the amplifier. Higher transconductance results in better gain performance. Fig. 3.2 displays the g_m values for a 2f×50 μm transistor at different V_g voltages. It can be observed that as V_{ds} voltage increases, the peak g_m slightly decreases. However, a V_{ds} bias of 2 V is chosen for the subsequent design to balance good gain performance and large signal behavior.

The selection of the gate bias voltage for the LNA involves a trade-off between power consumption, transconductance, and noise figure. Fig. 3.3 shows the simulated results of Id and g_m for a device size of 2f×50 μm at a V_{ds} bias of 2 V. It can be seen that the peak g_m is reached at V_g = 0.65 V. Previous research suggests that the optimal bias point for noise performance is typically at 50~70% of the max transconductance current [20]. Therefore, a bias point with an I_d current of approximately 10 mA is chosen. Fig. 3.4 illustrates the simulation results of NF_{min} against V_g, showing good noise performance between 0.4 V and 0.5 V. Based on these considerations, V_g is selected as 0.5 V, and I_d is set to 7.4 mA for the design of this LNA.

doi:10.6342/NTU202402726

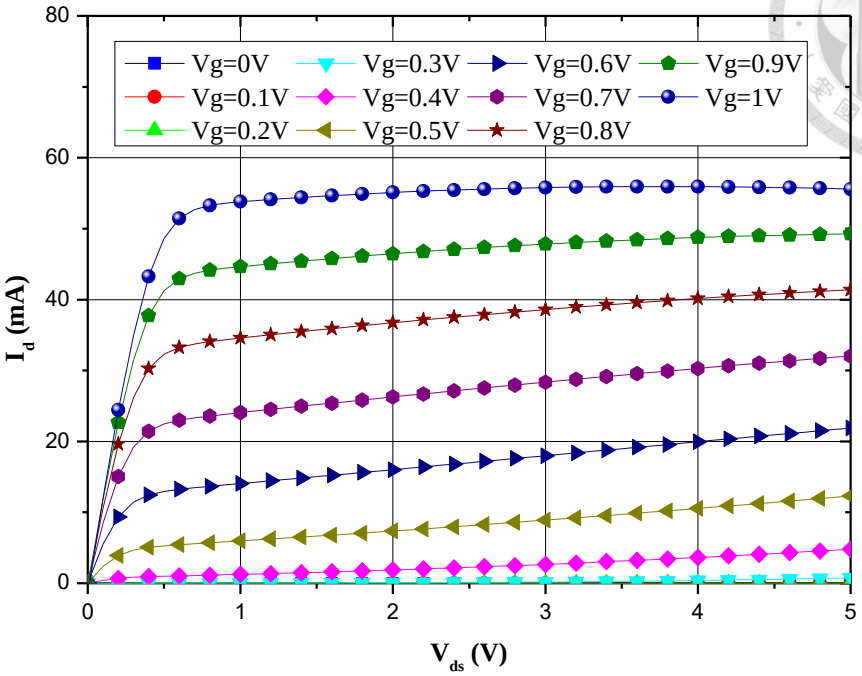

Fig. 3.1. DC-IV curves of the transistor with 100 μm total gate width.

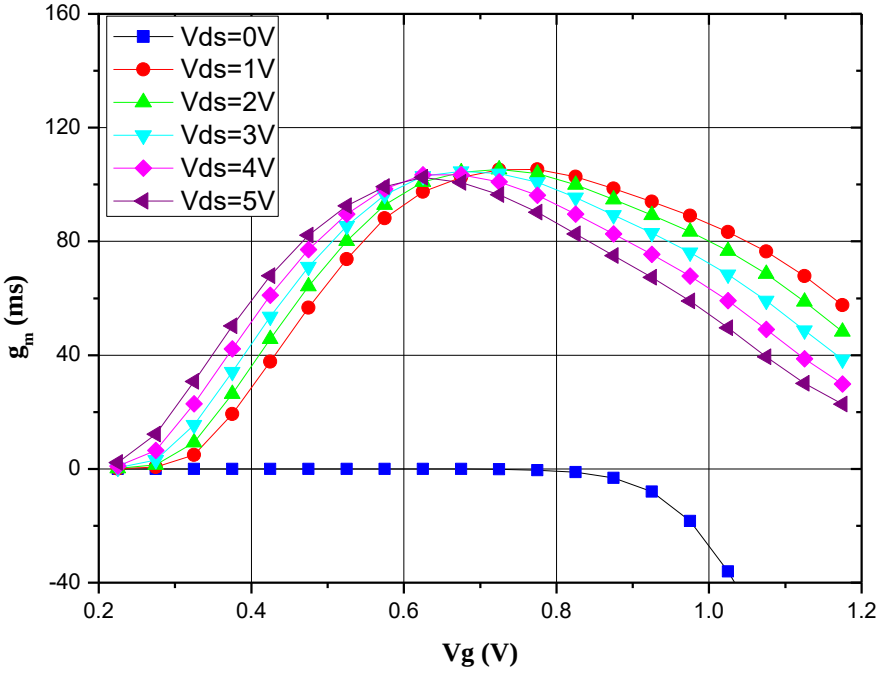

Fig. 3.2. g_m vs. Vg plot for different V_{ds}.

doi:10.6342/NTU202402726

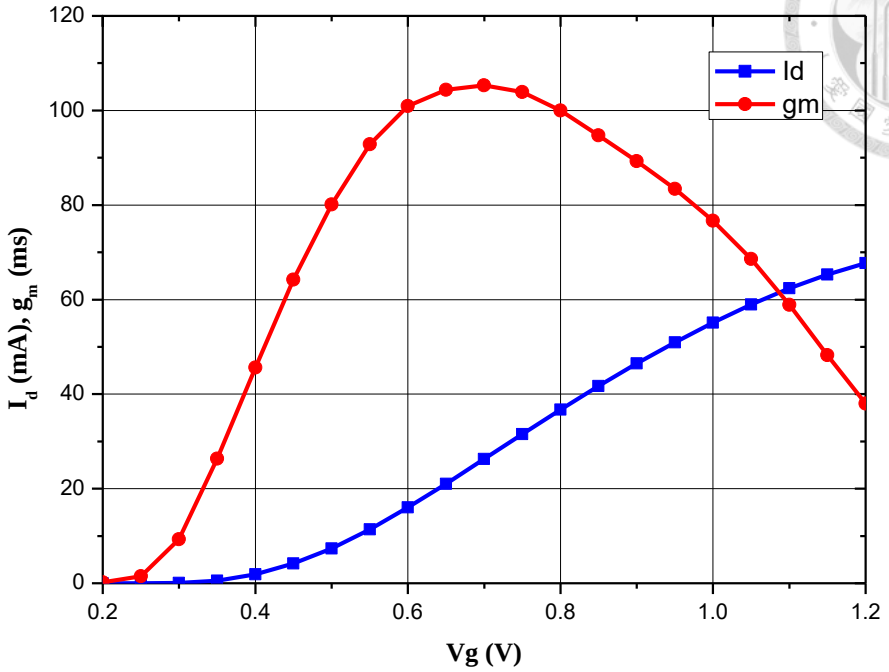

Fig. 3.3. Transconductance and drain current vs. V_g with a total gate width of 100 μm.

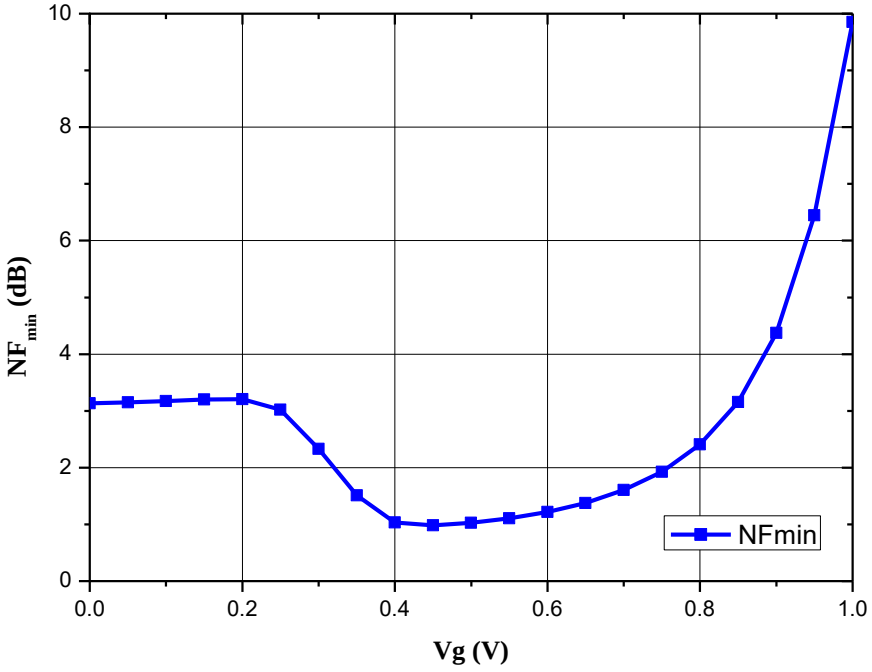

Fig. 3.4. NF_{min} vs. V_g with a total gate width of 100 μm.

doi:10.6342/NTU202402726

3.3 Device Size Selection

The size of the transistors in the MMW circuit design affects the amplifier's MAG/MSG and noise performance. Fig. 3.5 presents simulations for different device sizes under the selected bias conditions (V_{ds}= 2 V and V_g = 0.5 V), demonstrating that a size of 2f×50μm achieves the highest gain performance. Fig. 3.6 illustrates the NF_{min} for various device sizes, indicating that the noise performance gradually degrades as the size increases. Therefore, considering the overall gain and noise performance, a size of 2f×50μm was chosen for the design of this LNA. The same size will be used for each stage for ease of design.

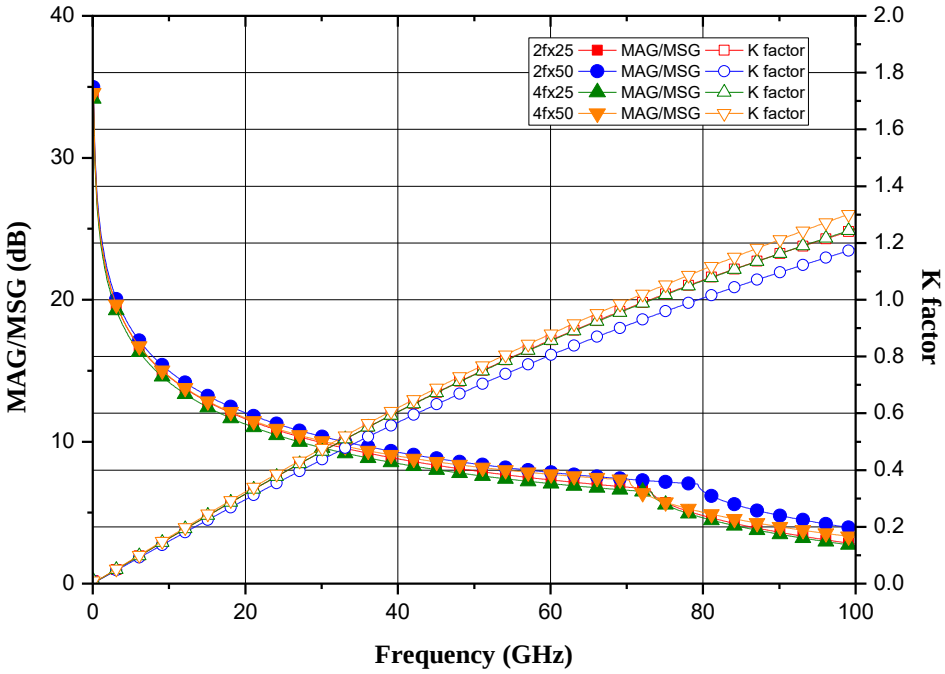

Fig. 3.5. MSG/MAG and stability factor in different device sizes.

doi:10.6342/NTU202402726

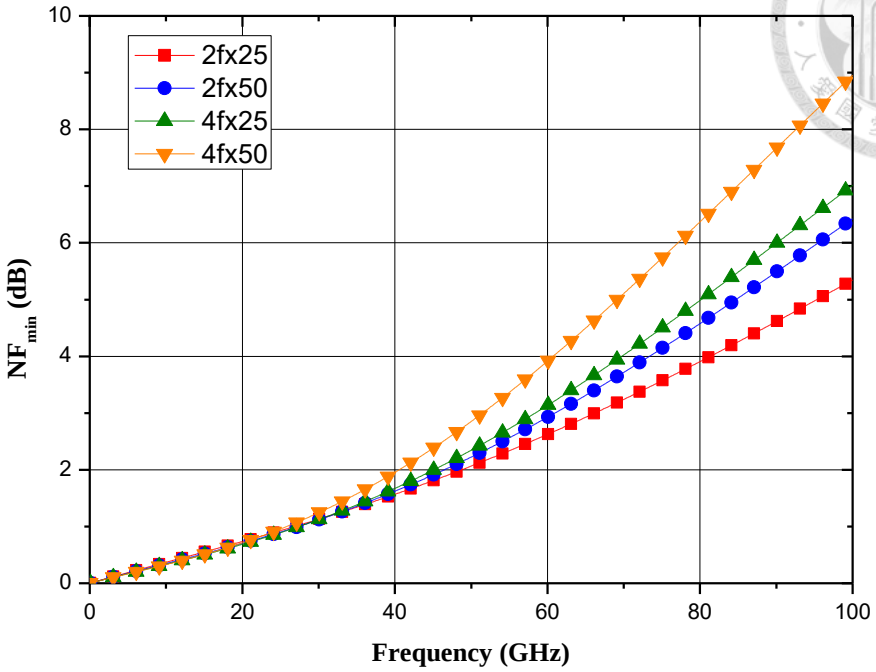

Fig. 3.6. Noise figure in different device sizes.

3.4 Source Degeneration

The primary design goal of the LNA is to achieve the lowest possible NF. The formula (3.1) used to calculate the total noise figure of the multi-stage circuit indicates that the first stage has the greatest impact on the entire circuit, necessitating both a low noise figure and a high gain [14]. As a result, it is important to figure out how to achieve conjugate matching and noise matching simultaneously.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_2 - 1}{G_1 G_2} + \cdots \quad (3.1)$$

Source degeneration is a common technique in LNA circuit design [19], [20], [23], in which the source point is connected to the ground using inductors or transmission lines, as shown in Fig. 3.7 (a). By using this method, the noise matching point and conjugate matching point can be optimized to be closer together, as illustrated in Fig. 3.8, helping

doi:10.6342/NTU202402726

maintain good input return loss when matching for S_{opt}. Fig. 3.9 shows the results of sweeping the length of the L_s transmission line at 28 GHz for transistor MAG/MSG and NF_{min}. It is found that length has a greater effect on gain and less effect on noise figure. To preserve the overall circuit's gain capability, the length of the source degeneration transmission line does not exceed 100 μm.

In GaAs LNA designs, the source inductor is often divided into two transmission lines for symmetry in layout, as shown in Fig. 3.7 (b) [24], [25]. However, due to area constraints in this design, paralleling would require approximately twice the length of transmission lines, resulting in increased area. As a result, the source shunt transmission line has only one side that is grounded. Additionally, source degeneration, as a form of negative feedback [23], enhances the circuit's stability and shifts the MSG frequency to lower frequencies, as shown in Fig. 3.10. Without source degeneration, the stability frequency is greater than 50 GHz. However, after adding 100μm and 200μm transmission lines as source degeneration, the starting frequencies of the MSG are 28 GHz and 20 GHz, respectively. Source degeneration lengths can be adjusted to meet the needs of each circuit and stage's needs, aiming to produce a stable, low noise, high gain amplifier.

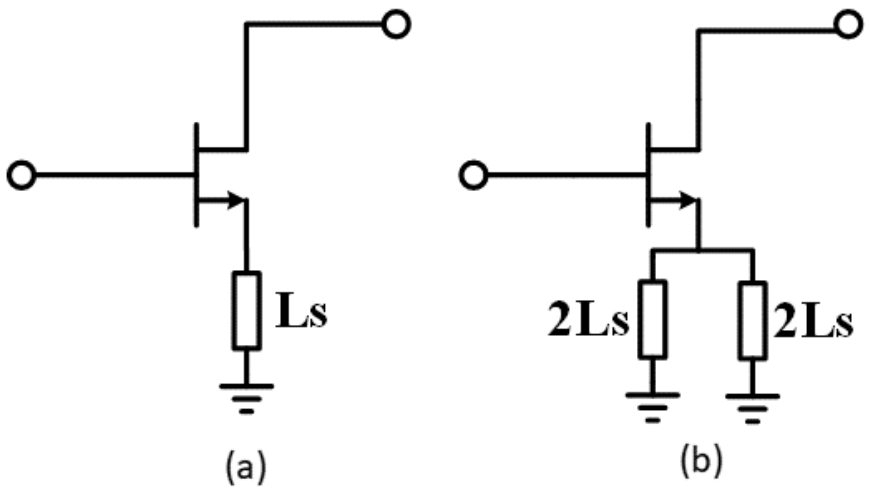

Fig. 3.7. (a) Source degeneration (b) Source degeneration for symmetric layout

doi:10.6342/NTU202402726

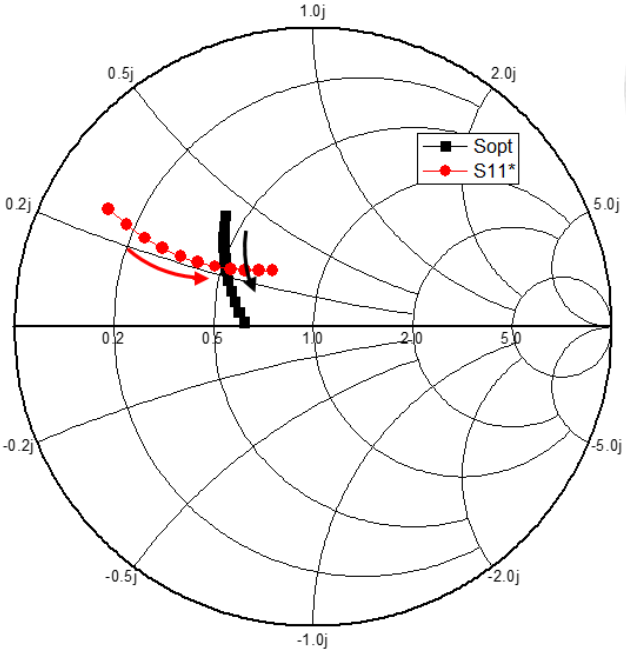

Fig. 3.8. Simulations of S_{opt} and S11* for the common source structure with a sweeping source degeneration transmission line.

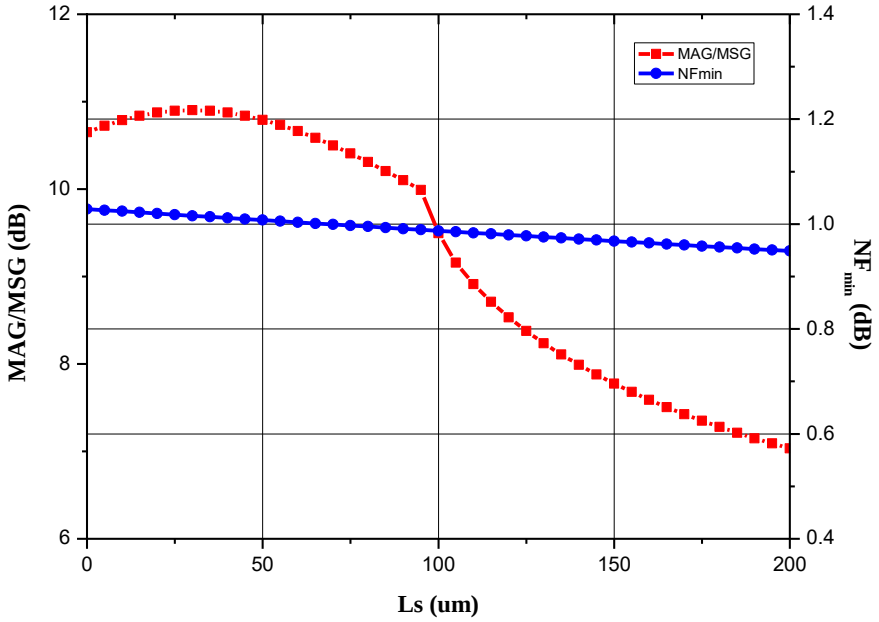

Fig. 3.9. MSG/MAG and NF_{min} with different source degeneration transmission line at 28GHz.

doi:10.6342/NTU202402726

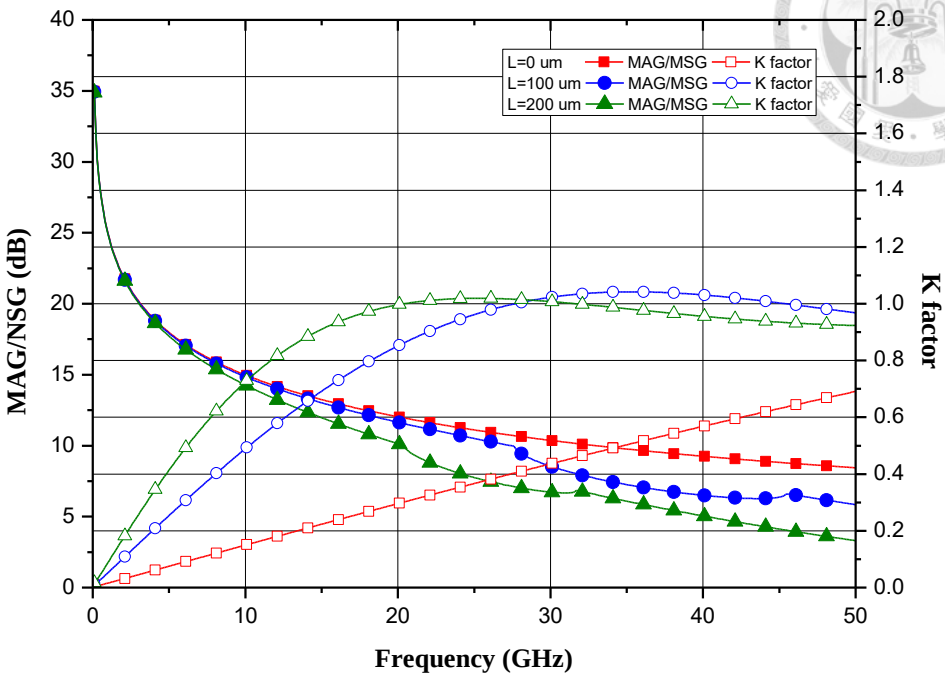

Fig. 3.10. MSG/MAG and NF_{min} with different source degeneration transmission line.

3.5 Common Source LNA using Capacitance Matching (CSC)

3.5.1 Source Degeneration Selection and Bypass Design

From the analysis of source degeneration, it is evident that increasing the length of the transmission line can bring S11* and S_{opt} closer, but doing so also causes the gain to decrease. As shown in Fig. 3.9, the gain starts to decrease rapidly when L = 100 μm. According to formula (3.1) in chapter 3.4, in a multi-stage circuit system, if the gain of the first stage is not sufficiently large, the noise of subsequent stages will significantly impact the overall noise figure. To maximize the gain of the first stage, L = 90 μm was chosen to ensure a higher gain and provide a relatively advantageous matching impedance point. This allows the first stage to contribute to achieving a good balance between noise

doi:10.6342/NTU202402726

figure, gain, and input return loss for the LNA. As seen in Fig. 3.11, it can be observed that, with the addition of a 90 μm transmission line, the transistor ideally achieves a gain of only 10 dB at 28 GHz. In this configuration, the two-stage design is unable to achieve the required 19 dB gain due to the losses caused by the matching circuit. Therefore, the design will be modified to incorporate a 3-stage common source configuration to meet the specifications.

During the design, it was found that return gain occurs near 15 GHz. Adding a small resistor after the bypass capacitor can eliminate the return gain. However, this also affects the matching short to ground, so dual bypass design is used. The first bypass capacitor provides the circuit to see the in-band RF ground, while the second bypass capacitor eliminates the 15-GHz return gain.

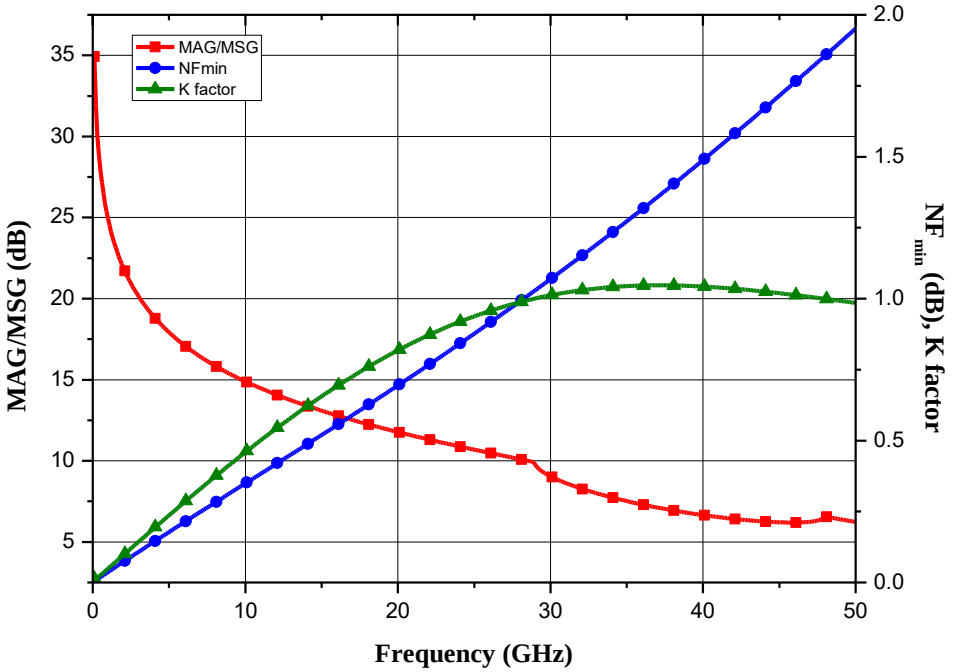

Fig. 3.11. MSG/MAG, K factor and NF_{min} with 90 μm source degeneration transmission line at 28GHz.

doi:10.6342/NTU202402726

3.5.2 Circuit Schematic and Simulation Result

Fig. 3.12 illustrates the schematic of this LNA, and Fig. 3.13 shows the S-parameters of the circuit with V_{ds} at 2 V, V_g at 0.5 V, and a total current of 21 mA. The peak gain is 19.3 dB, and the 3 dB bandwidth is 13.3 GHz, ranging from 19.2 to 32.5 GHz. It has reached its target gain of 19 dB and the original design goal of 25 to 31 GHz. The input return loss is between 6.1 and 10.6 dB within the target bandwidth, while the output return loss ranges from 8.9 to 40 dB. Due to the need for noise matching, the input return loss is farther from the target (>10 dB). Fig. 3.14 shows the simulated NF results, which ranged from 1.7 to 2.2 dB within the 3dB BW, greater than the design goal of 2.4 dB. Fig. 3.15 depicts the gain and output power versus input power of this LNA at 28GHz, with an OP_{1dB} of 7.2 dBm. Fig. 3.16 illustrates the layout of this 28GHz LNA, which has an area of 1.65 × 0.75 mm² that includes the RF and DC pads.

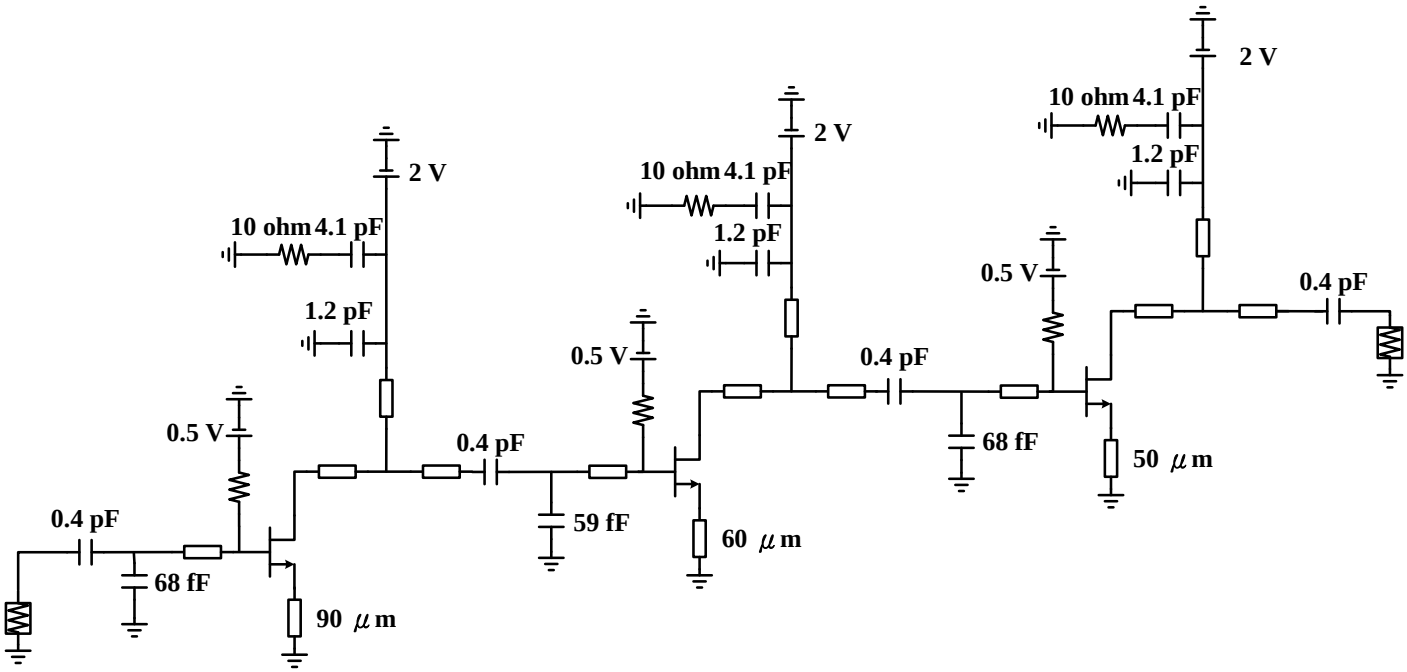

Fig. 3.12. Total schematic of the LNA using capacitance matching.

doi:10.6342/NTU202402726

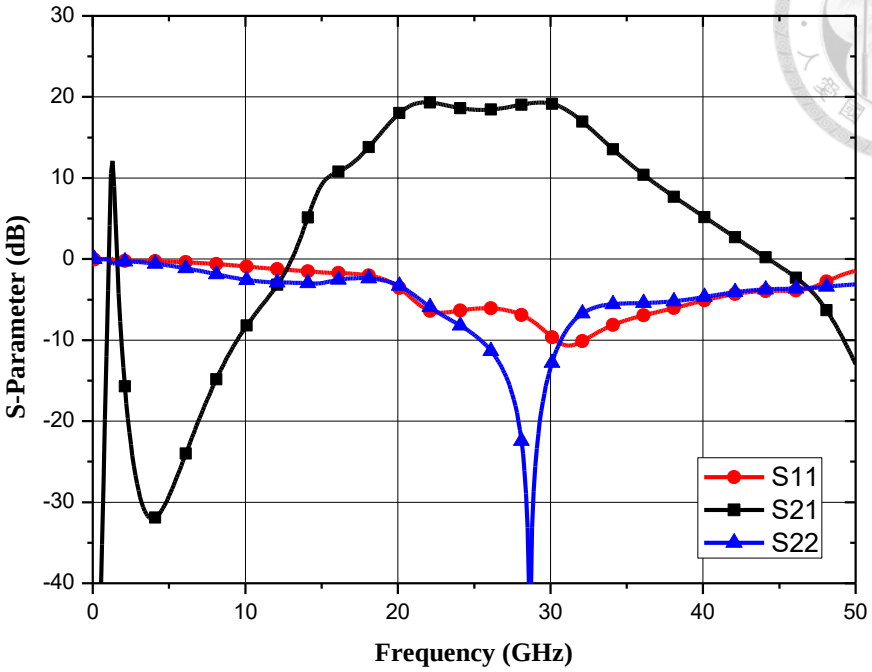

Fig. 3.13. The simulated S-parameters of the LNA using capacitance matching.

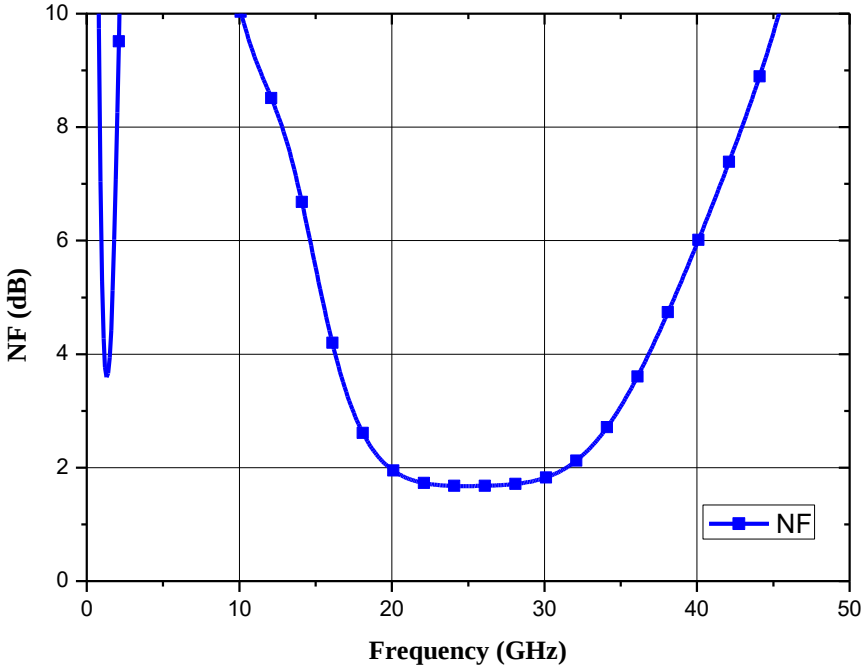

Fig. 3.14. The simulated noise figure of the LNA using capacitance matching.

doi:10.6342/NTU202402726

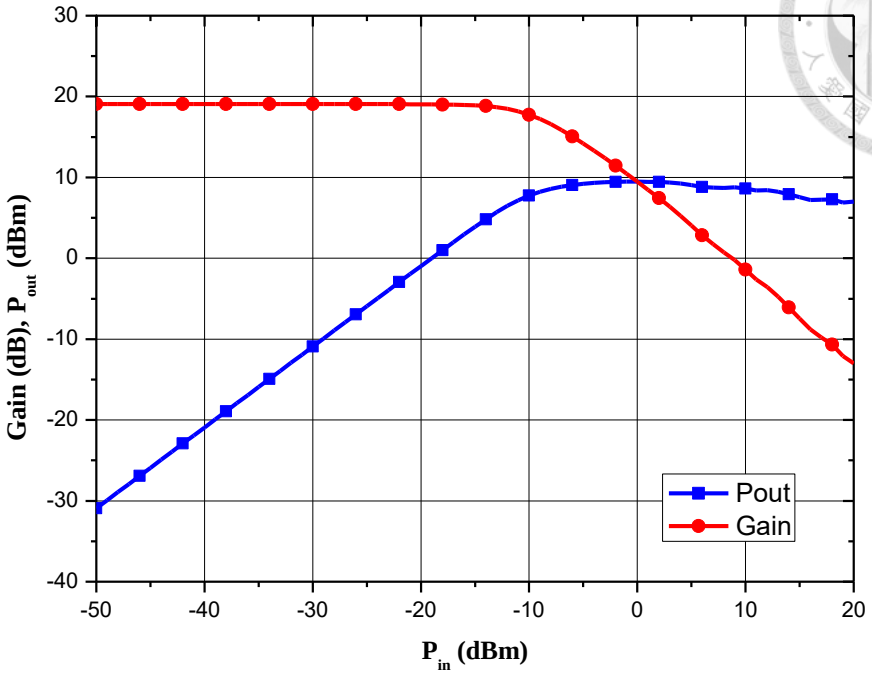

Fig. 3.15. The simulated large-signal results of the LNA using capacitance matching.

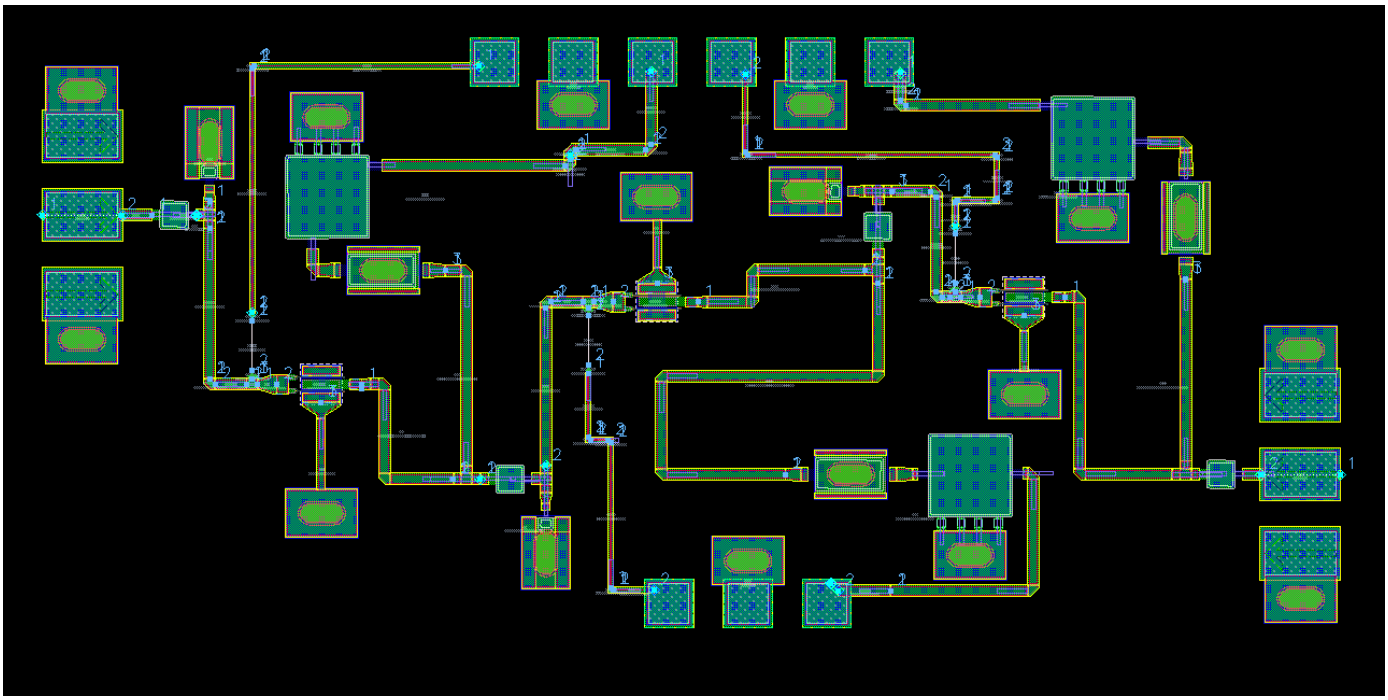

Fig. 3.16. The layout of the LNA using capacitance matching.

doi:10.6342/NTU202402726

3.6 Common Source LNA using Transmission Line Matching (CST)

3.6.1 The Differences from The Previous Version LNA.

Due to the imperfections in the previous design concerning return loss and area and the risk of using capacitors as the primary matching circuit due to variations in the MIM capacitors in the III-V Compound Semiconductors, uncertainties affecting the chip's performance must be addressed. In order to mitigate the impact of variations, open stub transmission lines will be utilized in the matching circuit in place of capacitors. In this process, each via to ground for capacitors occupies a fixed area, and the inter-stage matching configuration is altered, as shown in Fig. 3.17, to reduce the use of capacitors, save area, and attempt to improve return loss. Additionally, as the NF is significantly better than the design target, the length of the source degeneration transmission line is reduced, sacrificing some NF characteristics to minimize the occupied area.

In order to minimize the amount of area used, a source degeneration transmission line determining 60 μm is selected for the first stage. However, the stability of the circuit must still be considered. From Fig. 3.9, it is evident that at 28 GHz, the K factor is 0.9, and adding the losses from the matching network can bring the circuit into a stable state. Fig. 3.18 shows the simulation results for the transistor with 60 μm of source degeneration, revealing that the MSG starts at 34 GHz. This higher gain assists in suppressing the noise provided by the subsequent stages, ensuring that the reduction in source degeneration length does not cause a significant increase in NF. In addition to reducing the length of source degeneration, it is confirmed that the size of the second bypass capacitor will not affect the in-band performance and reducing it appropriately to reduce area usage.

Fig. 3.19 presents the pre-simulation results, showing the highest gain of 24.1 dB at 24.5 GHz. However, the gain quickly attenuates over 3 dB after 30 GHz, and there is a

doi:10.6342/NTU202402726

degradation in input return loss around 25 GHz, failing to meet the specified goals for gain and return loss. To help with matching, 5 ohm resistors were added to the drain terminals of the first two stages, as shown in Fig. 3.20. The result shows a flat gain in the range of 25 to 31 GHz, with gain variation less than 1 dB. Additionally, the return loss is significantly improved, meeting the specified requirements.

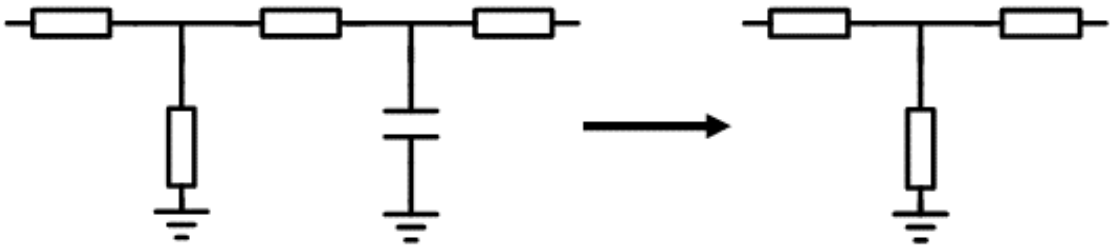

Fig. 3.17. Changes in the inter-stage matching network.

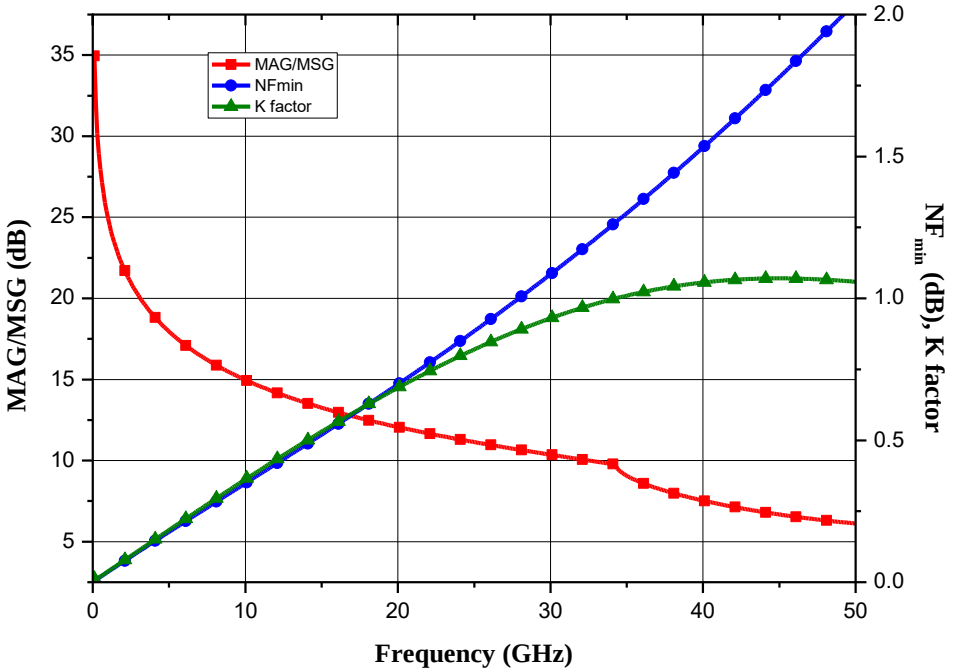

Fig. 3.18. MSG/MAG, K factor and NF_{min} with a 60 μm source degeneration transmission line at 28GHz.

doi:10.6342/NTU202402726

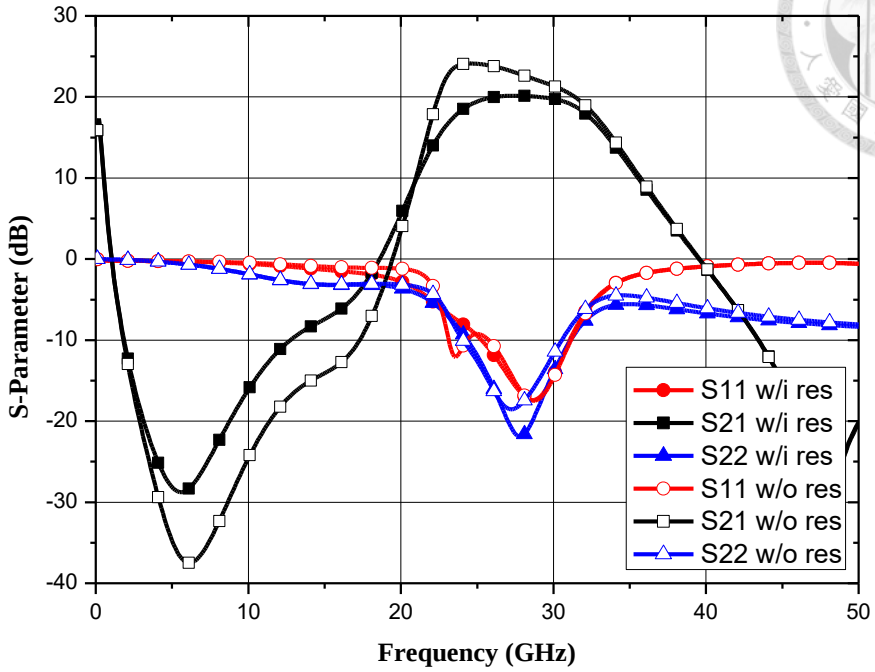

Fig. 3.19. The simulated S-parameters of the LNA with and without small resistors.

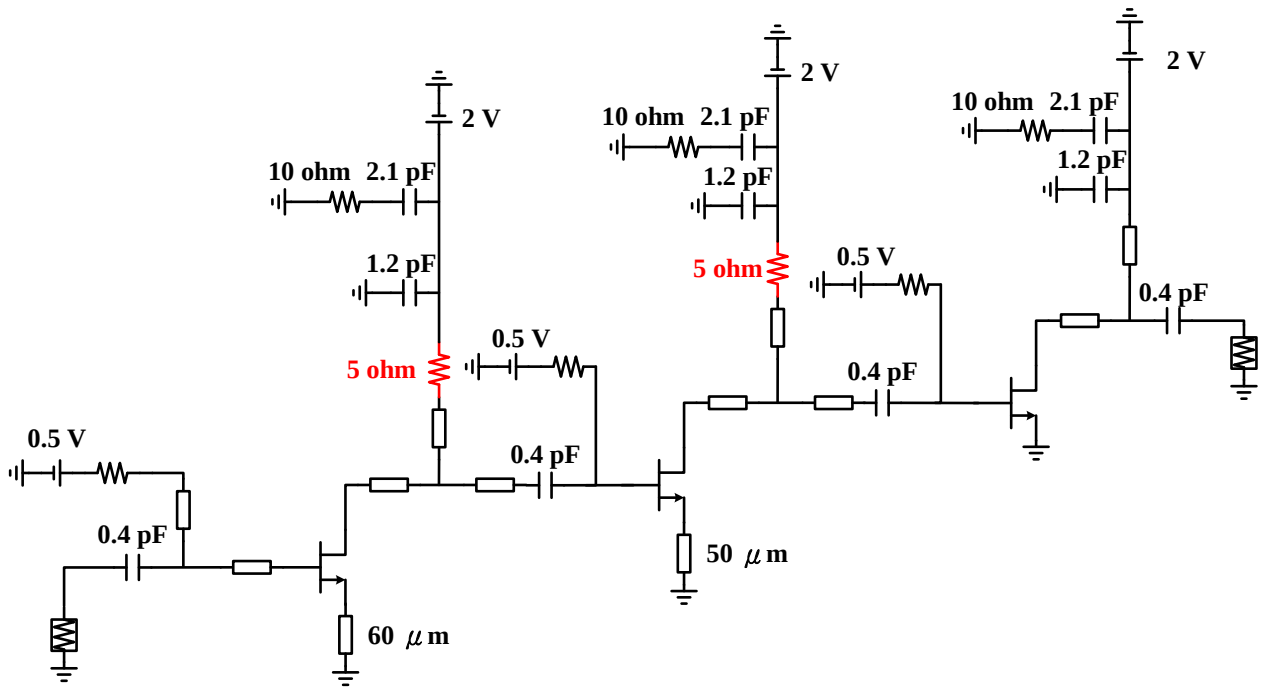

Fig. 3.20. The schematic of the LNA using transmission line matching adding small resistors.

doi:10.6342/NTU202402726

3.6.2 Circuit Schematic and Simulation Result

Fig. 3.21 illustrates the schematic of this LNA, while Fig. 3.22 depicts the S-parameters of the circuit at V_{ds} of 2 V, V_g of 0.5 V, and a total current of 21 mA. The peak gain is 20.5 dB, and the 3 dB bandwidth is from 23 to 33 GHz, covering 10 GHz. This achieves the initial design goals of 25 to 31 GHz with a target gain of 19 dB. The input return loss is between 10.4 and 17.8 dB within the target bandwidth, while the output return loss ranges from 11.8 to 22 dB. Compared to the previous version, the return loss goals are all achieved. Fig. 3.23 presents the simulated NF results, ranging from 1.8 to 2.2 dB within the 3 dB bandwidth, meeting the specified design goal. Fig. 3.24 depicts the gain and output power versus input power of this LNA at 28 GHz, with an OP_{1dB} of 6.2 dBm. Fig. 3.25 shows the layout of the 28 GHz LNA, which includes DC and RF pads. The area is 1.38 x 0.79 mm², slightly smaller than the previous version.

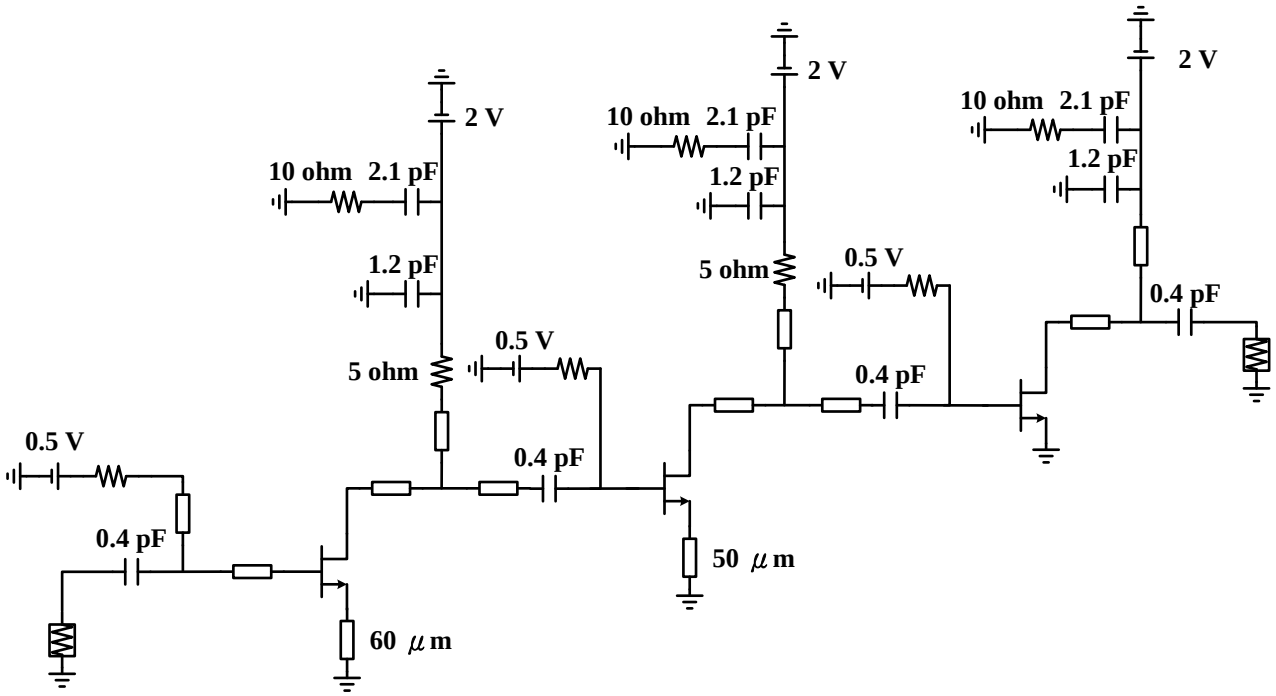

Fig. 3.21. Total schematic of the LNA using transmission line matching.

doi:10.6342/NTU202402726

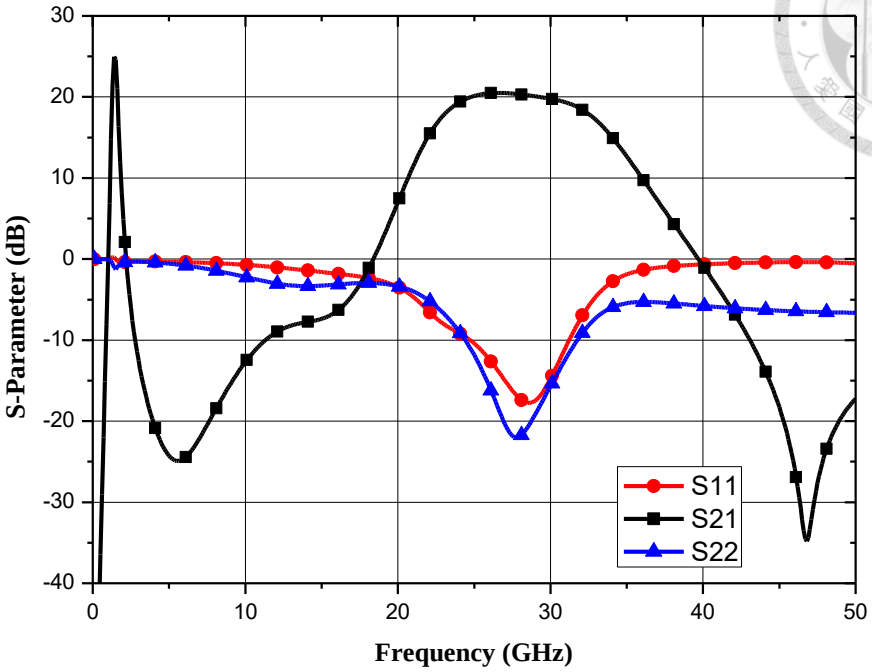

Fig. 3.22. The simulated S-parameters of the LNA using transmission line matching.

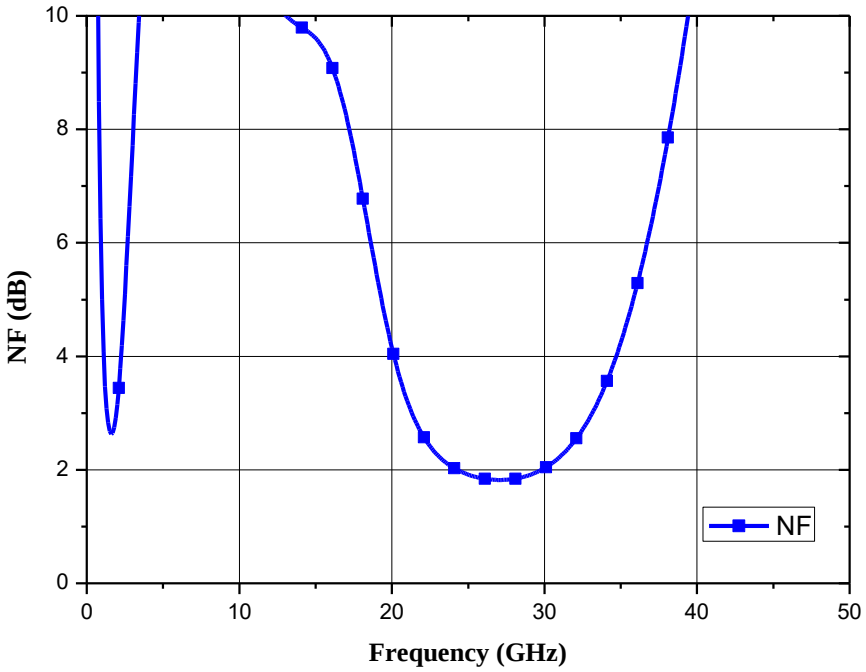

Fig. 3.23. The simulated noise figure of the LNA using transmission line matching.

doi:10.6342/NTU202402726

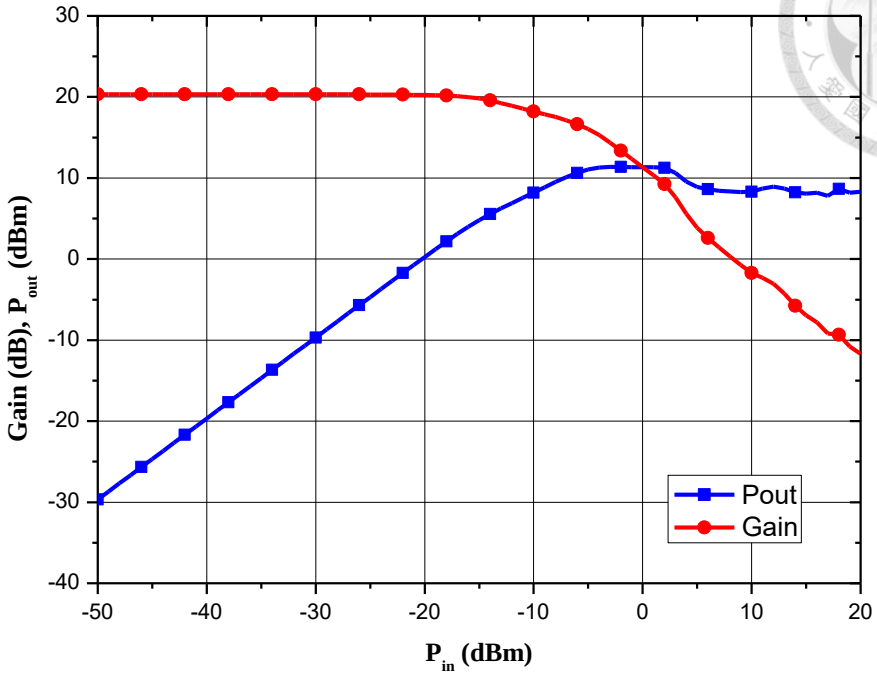

Fig. 3.24. The simulated large-signal results of the LNA using transmission line matching.

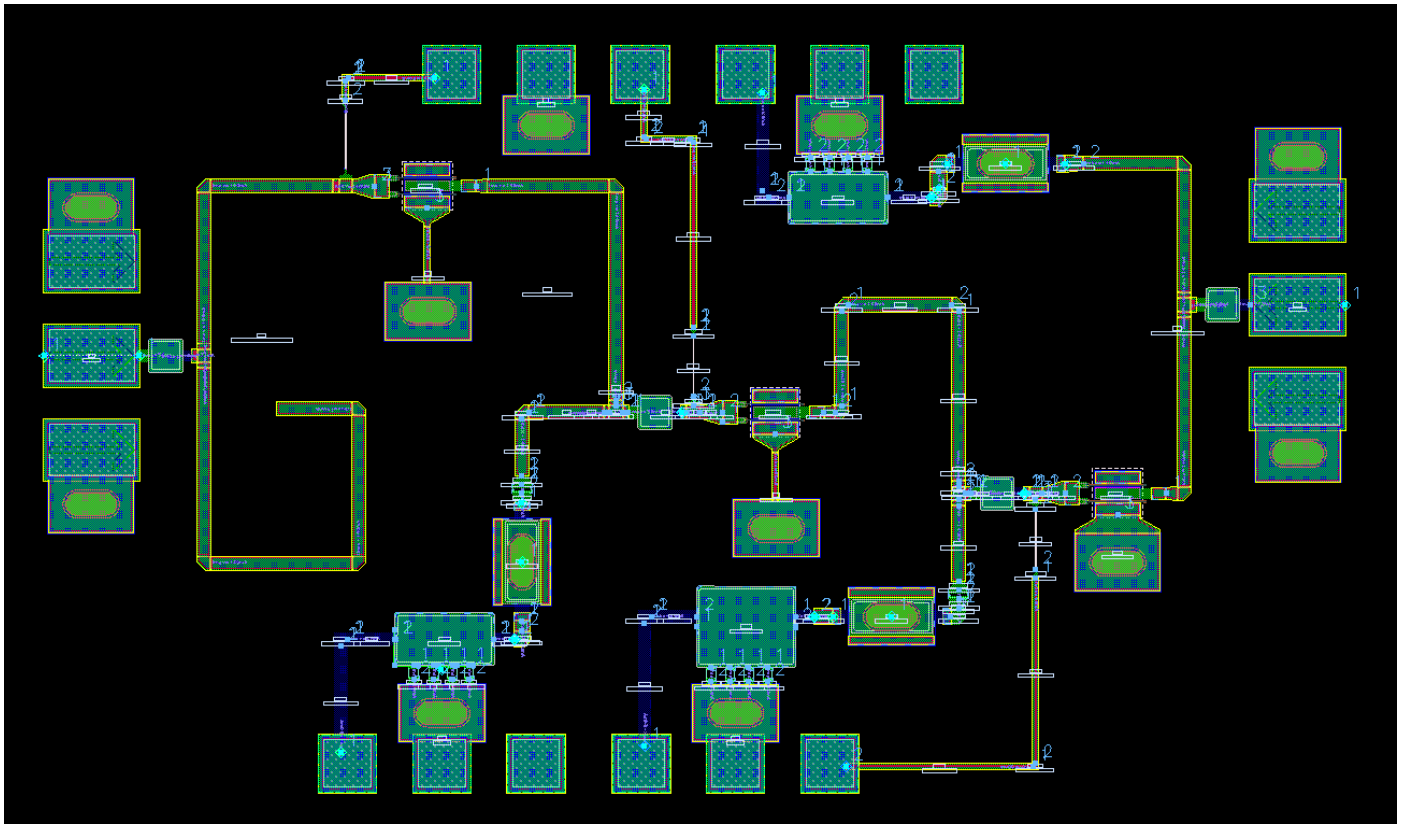

Fig. 3.25. The layout of the LNA using transmission line matching.

doi:10.6342/NTU202402726

3.7 Cascode version LNA

3.7.1 Cascode version Design

Following the design iterations with common source configurations in the previous two versions, exploration is underway for the implementation of a cascode configuration in this design. Cascode configuration allows achieving higher gain in a single stage, reducing the need for multiple stages to reach the same gain target.

A pure cascode architecture can lead to instability, as indicated by negative K factors in Fig. 3.27. To address this, some losses are introduced to help stabilize the circuit. In other publications, instability issues with the cascode structure have been encountered, and a proposed solution involves utilizing RC feedback to stabilize the circuit [17], [18], [21]. Additionally, adding resistors in the output matching network can contribute losses and promote stability. Fig. 3.26 illustrates the original cascode structure, the cascode with output lossy matching, and the cascode with RC feedback. Fig. 3.27 compares the simulation results of these three configurations.

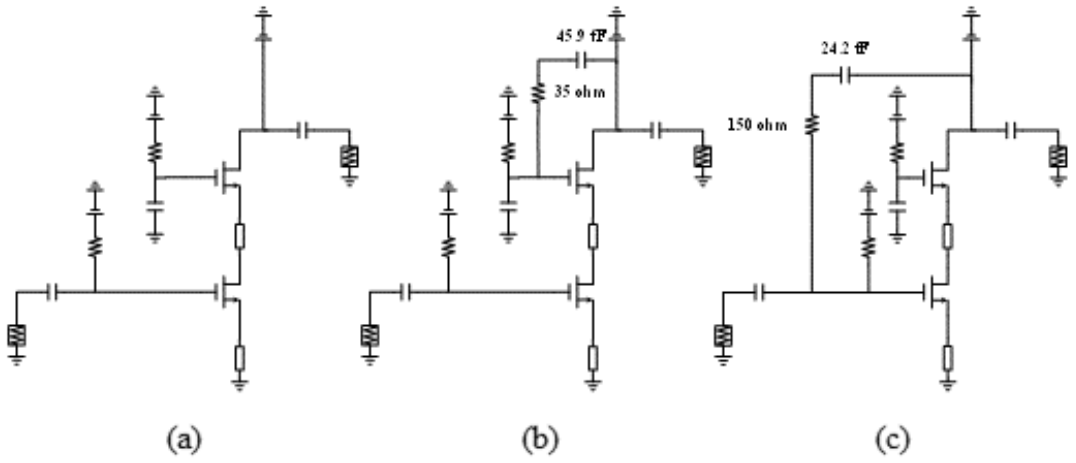

Fig. 3.26. (a) Original cascode structure. (b) Cascode structure with output lossy matching. (c) Cascode structure with RC feedback.

doi:10.6342/NTU202402726

While both strategies successfully stabilize the cascode structure, RC feedback works through negative feedback, resulting in a more significant reduction in MAG/MSG, from 24.8 dB to 13.6 dB at 28 GHz. On the other hand, adding resistive loss to the output matching has less impact. The capacitance and back-via inductance create a bandpass effect at the target frequency, resulting in a MAG/MSG reduction from 24.8 dB to 18.2 dB at 28 GHz. Compared to RC feedback, this method achieves an additional 5 dB of gain. Fig. 3.28 shows the NF comparison of three cascode architectures. It can be seen that the noise performance of lossy matching is slightly better than that of RC feedback. Finally, a common ground for the common gate and the lossy matching was chosen to ensure the most efficient use of space, reducing the need for an additional via.

As mentioned in see 3.6.1, the second bypass capacitor will not affect in-band performance, so the size was reduced because of layout constraint.

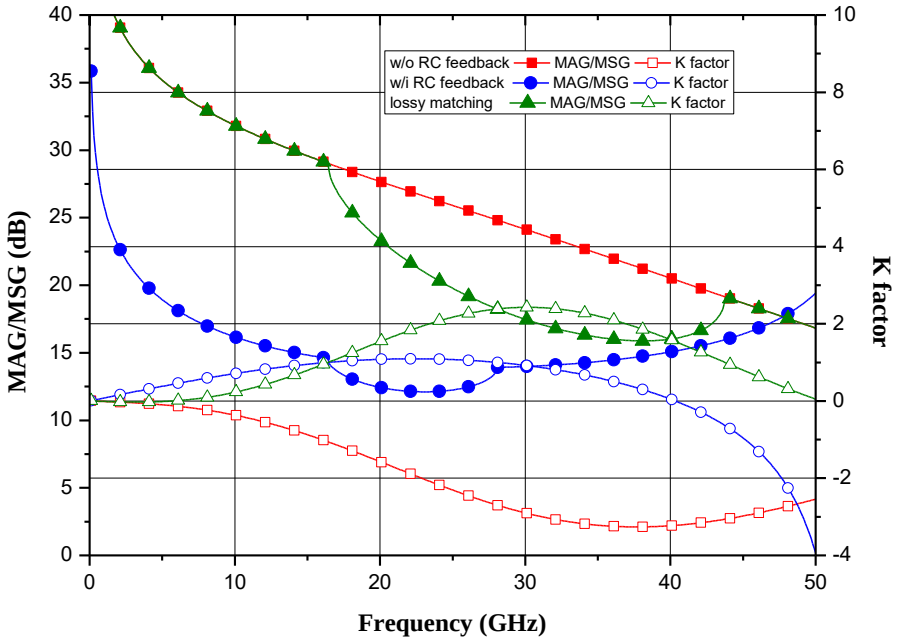

Fig. 3.27. Simulation results of MSG/MAG and K factor for the three architectures.

doi:10.6342/NTU202402726

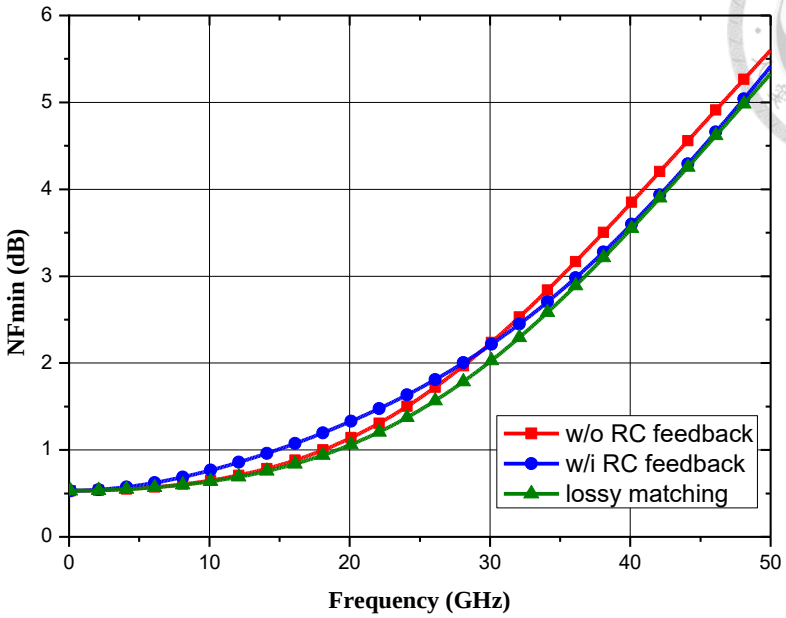

Fig. 3.28. Simulation results of NF_{min} for the three architectures.

3.7.2 Circuit Schematic and Simulation Result

The schematic of this LNA is depicted in Fig. 3.29. The gate capacitor value of 0.52 pF was determined by EM simulation to ensure an RF short at 28 GHz. Fig. 3.30 shows the S-parameters of the circuit with V_{ds} at 4 V, V_{g2} at 2.5 V, and V_{g1} at 0.5 V, resulting in a total current of 14 mA. The peak gain is 20.1 dB, and the 3 dB bandwidth ranging from 22.2 to 32.4 GHz, meeting the initial design targets of 25 to 31 GHz with a target gain of 19 dB. Input return loss falls within 5.3 to 8 dB across the target bandwidth, while output return loss ranges from 7.2 to 17.2 dB. Because of the emphasis on noise matching, the input return loss deviates by more than 10 dB from the target. Fig. 3.31 shows the simulated NF results, ranging from 2.2 to 2.8 dB in the 3 dB bandwidth and 2.2 to 3 dB in the design target bandwidth. The NF performance does not fully meet the 2.4 dB target until after 30 GHz. Fig. 3.32 depicts the gain and output power versus input power of this

doi:10.6342/NTU202402726

LNA at 28 GHz, with an OP_{1dB} of -5.4 dBm. The OP_{1dB} will be lower due to output lossy matching, and the resistor will consume some of the output power. As a result, OP_{1dB} performance is lower than that of the CS design. Fig. 3.33 illustrates the layout of this 28 GHz LNA, which has an area of 1.33 x 0.795 mm² that includes the RF and DC pads.

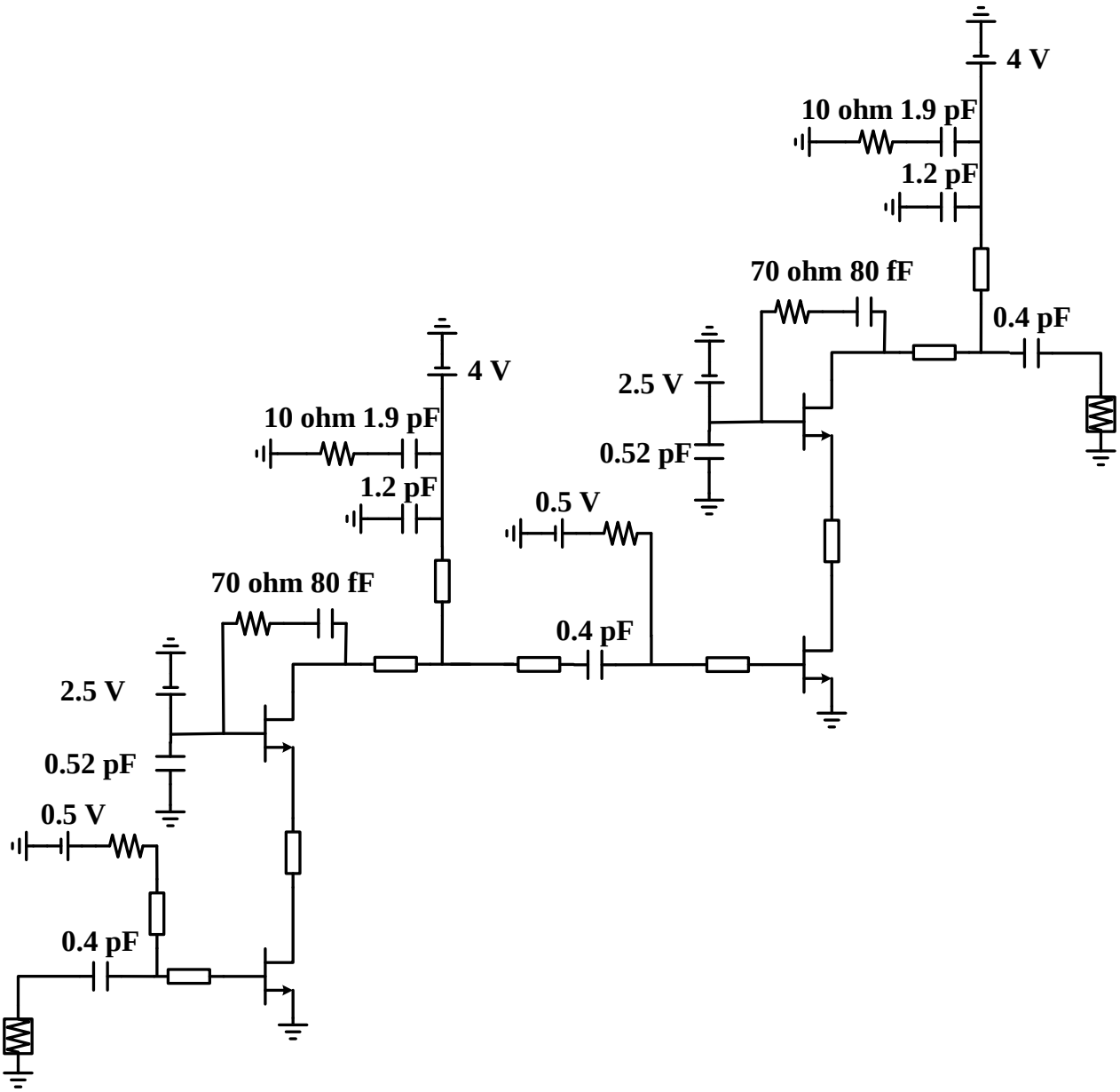

Fig. 3.29. Total schematic of the cascode version LNA.

doi:10.6342/NTU202402726

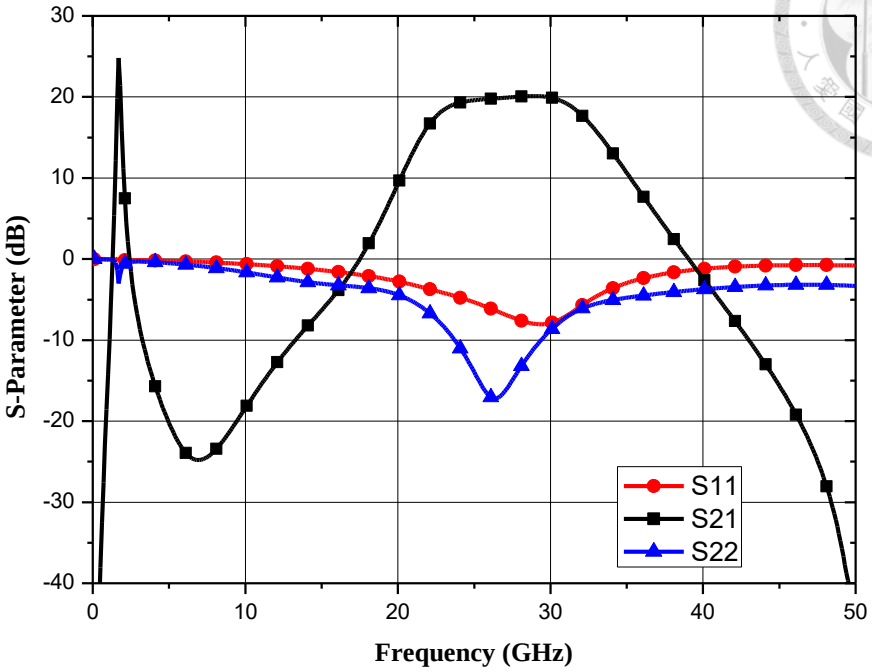

Fig. 3.30. The simulated S-parameters of the cascode version LNA.

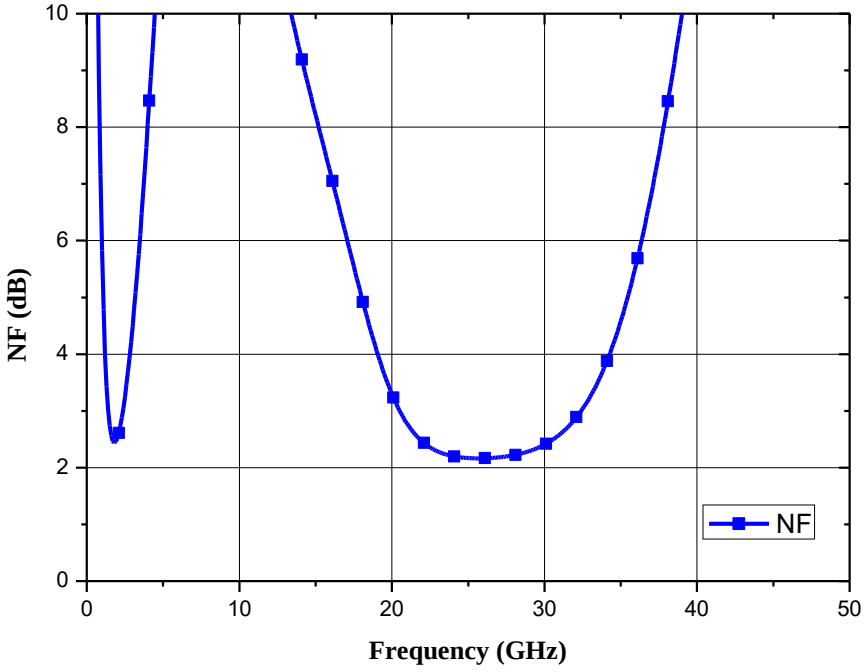

Fig. 3.31. The simulated noise figure of the cascode version LNA.

doi:10.6342/NTU202402726

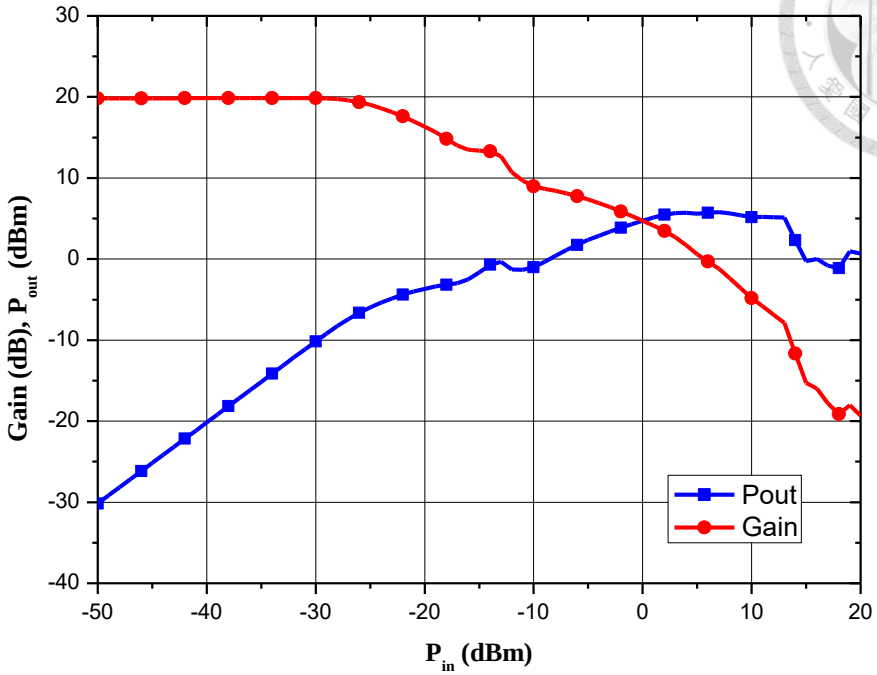

Fig. 3.32. The simulated large-signal results of the cascode version LNA.

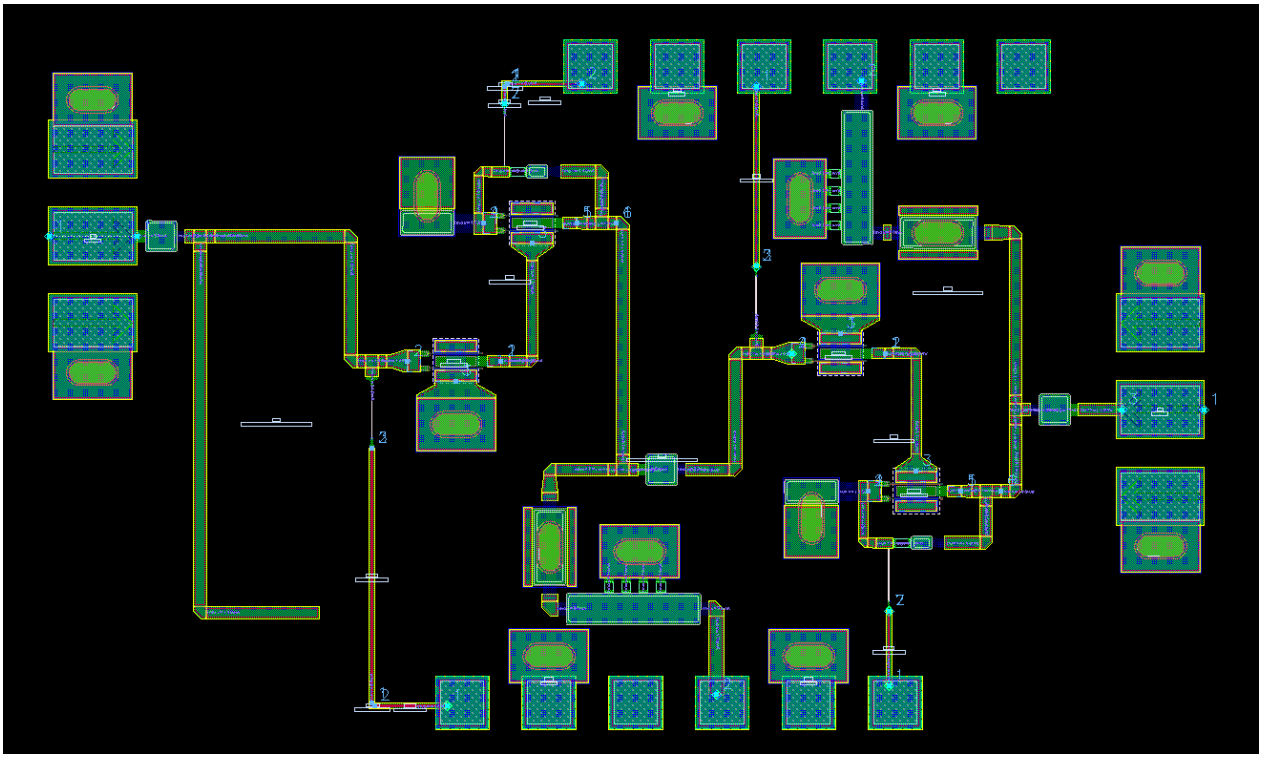

Fig. 3.33. The layout of the cascode version LNA.

doi:10.6342/NTU202402726

3.8 Off-Chip Bypass and Bond Wire Effect

Low frequency oscillation in RF circuits typically refers to the phenomenon of low frequency oscillations or instability occurring in high frequency circuits. Transistors exhibit high gain at low frequencies, and when strong reflective components such as DC blocks and RF shorts are encountered in the circuit, there is a chance of meeting the conditions for oscillation [26]. If the on-chip bypass is insufficient and the frequency range does not extend low enough to provide a release path for the signal, it can affect the circuit's normal operation.

In the initial measurements, all three circuits encountered low-frequency oscillation. By adding test lines to the simulation to check the three circuits, it can be found that the *K* factor is lower than one around 1 GHz. The measurement results for the common source using capacitances matching version without off-chip bypass are shown in Fig. 3.34, and the measurement using a spectrum analyzer (SA) is shown in Fig. 3.35, where low-frequency oscillation causes a tone at 505 MHz with -8.3 dBm, resulting in a decrease in in-band gain of more than 10 dB. Fig. 3.36 depicts the common source using transmission lines matching version without off-chip bypass, while Fig. 3.37 shows a tone at 786 MHz with -4 dBm because of intense low frequency oscillation, which causes the in-band gain to drop by almost 15dB. The cascode version without off-chip bypass is shown in Fig. 3.38, and Fig. 3.39 displays a tone at 786 MHz with -42 dBm. Although the oscillation intensity is less than in the previous two versions, small jitter exists from low frequency up to 16 GHz.

doi:10.6342/NTU202402726

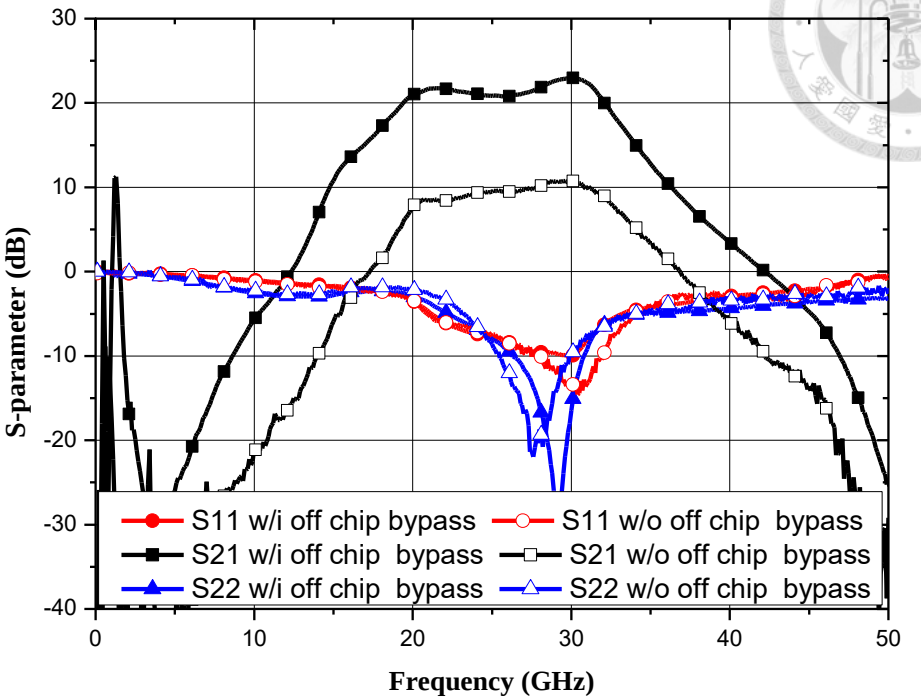

Fig. 3.34. S-parameter measurement results of common source LNA using capacitance matching with and without off-chip bypass.

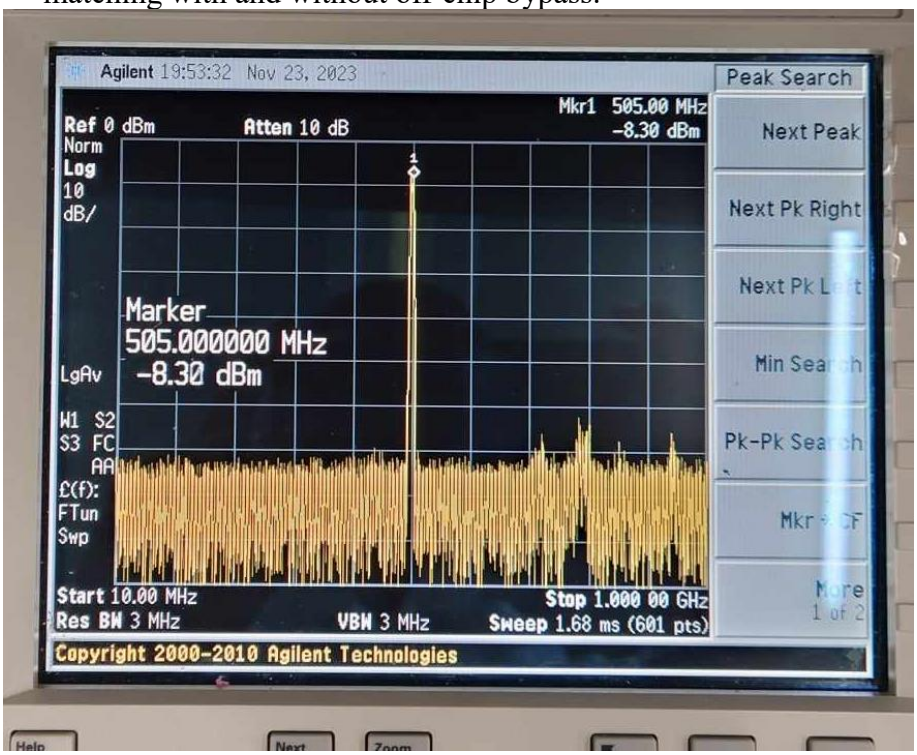

Fig. 3.35. Spectrum analyzer measurement results of the common source LNAs using capacitance matching.

doi:10.6342/NTU202402726

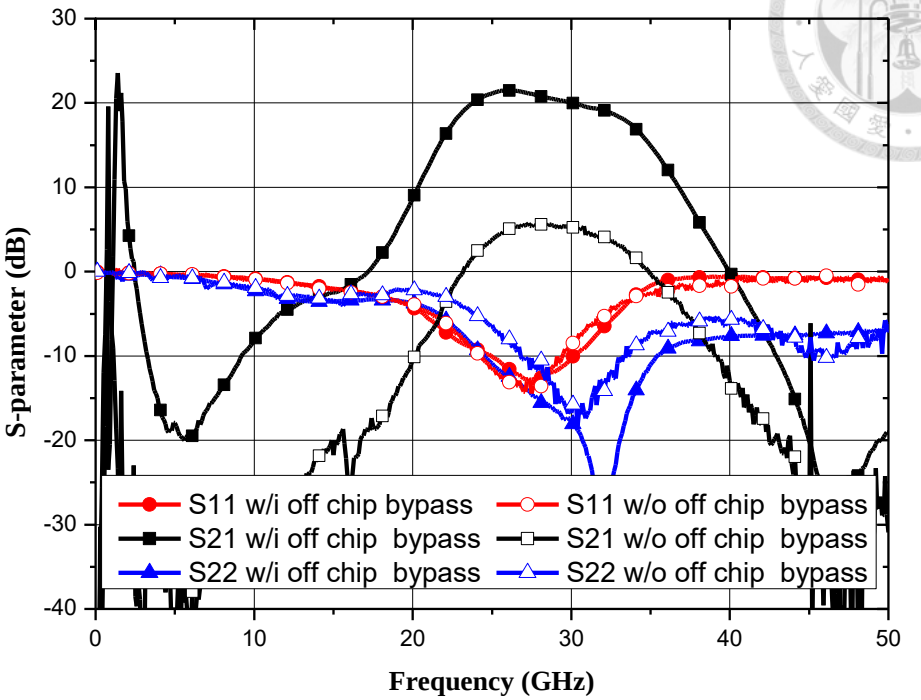

Fig. 3.36. S-parameter measurement results of common source LNA using transmission line matching with and without off-chip bypass.

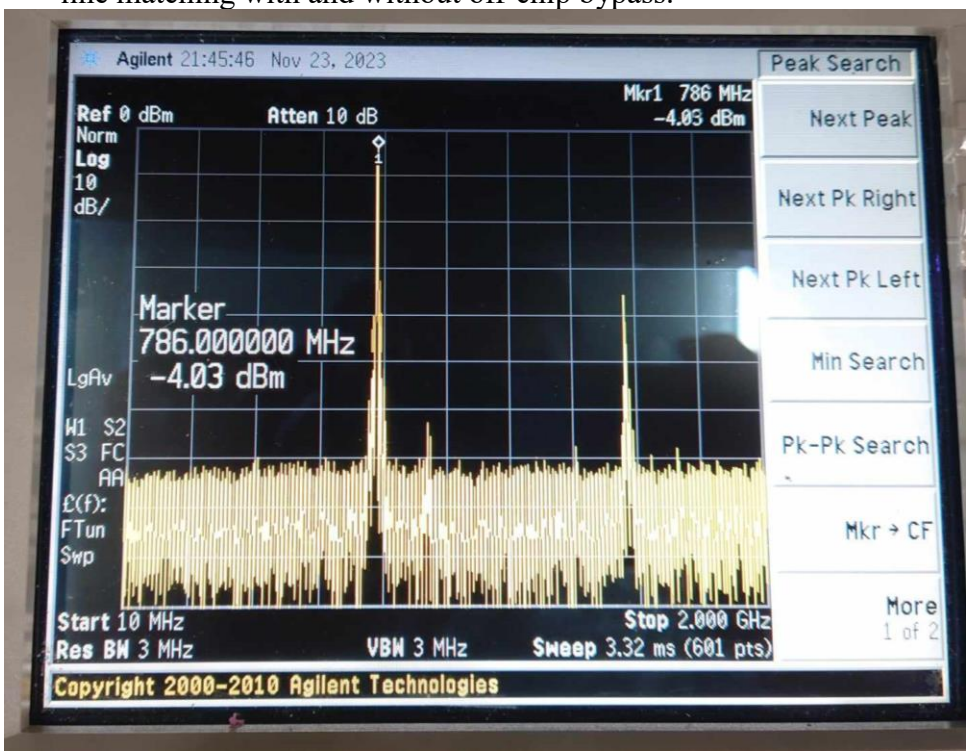

Fig. 3.37. Spectrum analyzer measurement results of the common source LNA using transmission line matching.

doi:10.6342/NTU202402726

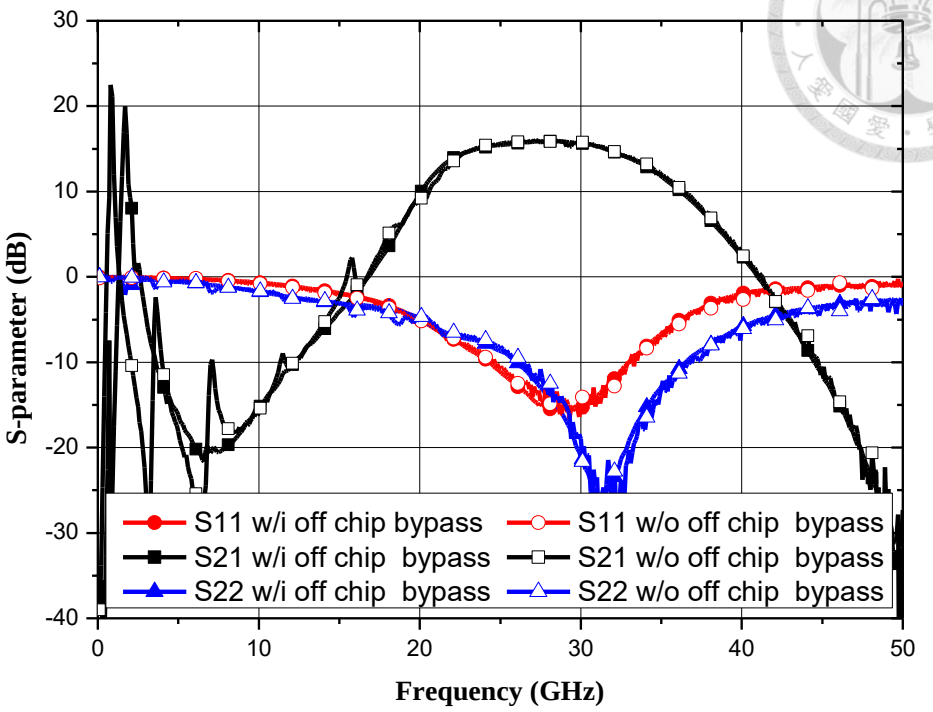

Fig. 3.38. S-parameter measurement results of cascode version LNA with and without off-chip bypass.

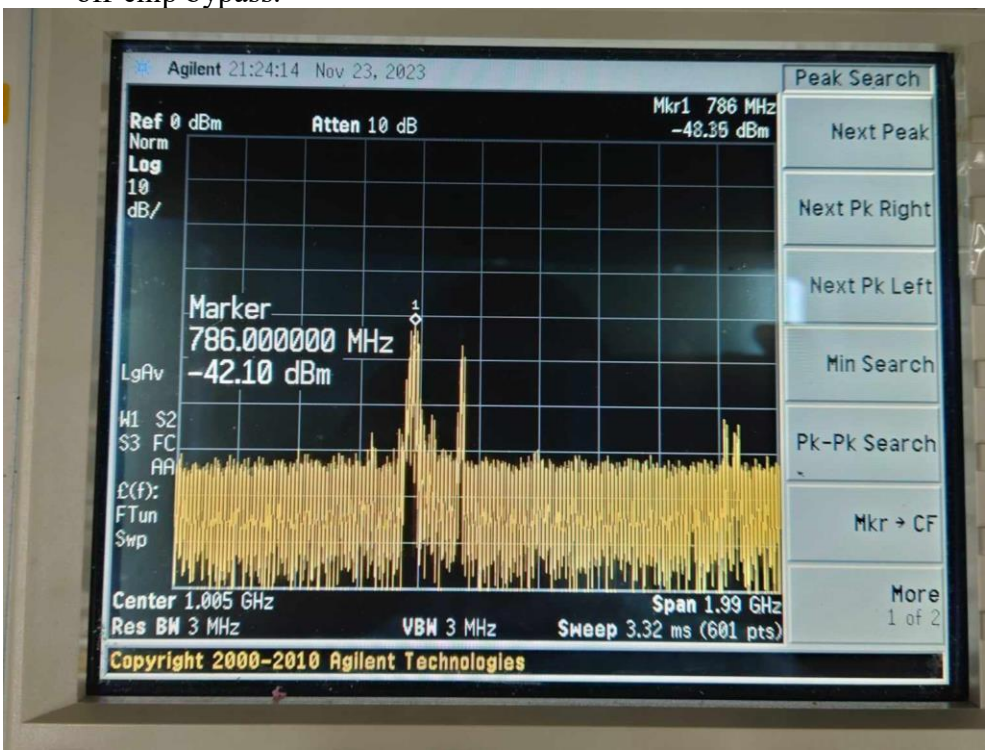

Fig. 3.39. Spectrum analyzer measurement results of the cascode version LNA.

doi:10.6342/NTU202402726

To address the low frequency oscillation, off-chip bypass was added to all three circuits, with the capacitor size designed as shown in Fig. 3.40. Fig. 3.41 shows the simulation results, indicating a capability to attenuate signals down to -40 dB at 500 MHz, allowing the previously observed low-frequency tones to pass through the capacitor toward the ground. Fig. 3.42 shows the *K* factor before and after LNA adding off chip bypass. It can be seen that after adding the off chip, the red line does not show a sudden change in *K* factor at 1GHz.

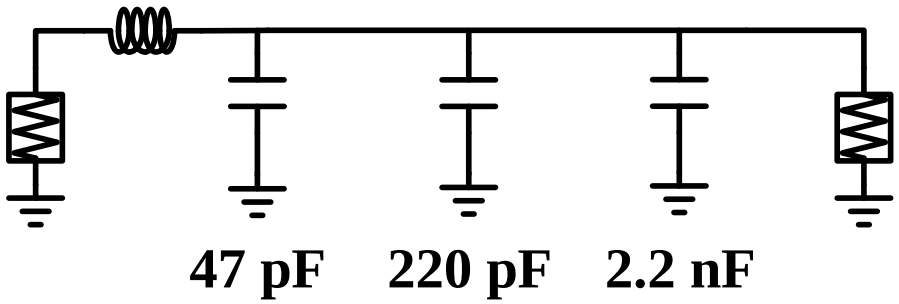

Fig. 3.40. The design schematic of the off-chip bypass circuit.

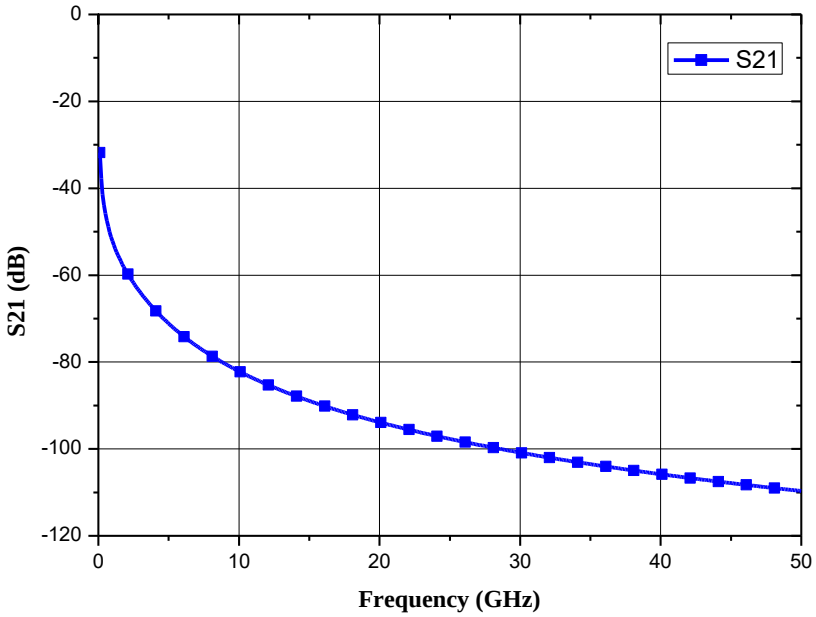

Fig. 3.41. S21 performance of the off-chip bypass.

doi:10.6342/NTU202402726

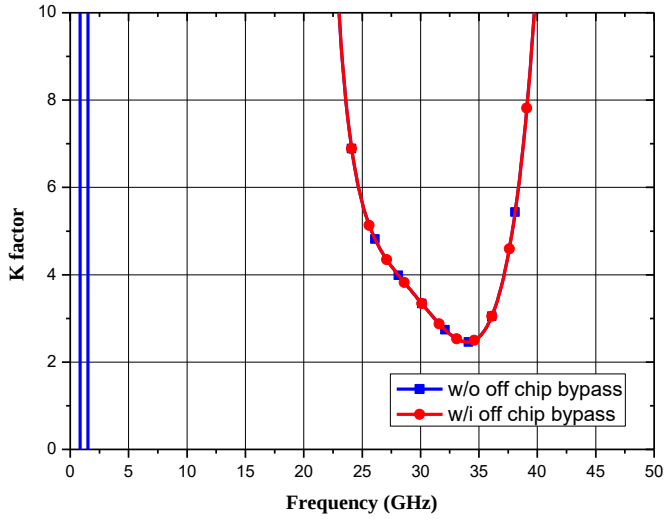

Fig. 3.42. Comparison of *K* factor with and without off chip bypass.

Fig. 3.34, Fig. 3.36, and Fig. 3.38 demonstrate the measurement results with the addition of off-chip bypass, revealing a gain peak between 1 GHz and 2 GHz. Fig. 3.43 shows the Smith chart for the cascode LNA measurement results, indicating a low-frequency matching point. According to the simulation results in section 3.9.3, a similar phenomenon occurs around 1.5GHz after adding the off-chip bypass capacitor. This issue was eventually traced to the inductor used as a substitute for bonding wire, which significantly influenced the low frequency gain.

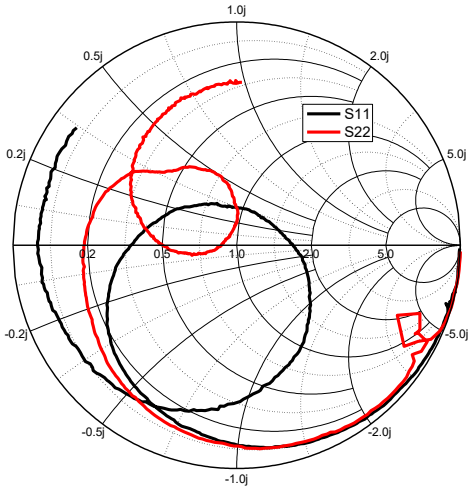

Fig. 3.43. The Smith chart shows the cascode LNA's measured results.

doi:10.6342/NTU202402726

Fig. 3.44 shows the simulated results for common source using capacitance matching with equivalent bonding wire inductances of 0.1 nH and 10 nH. The results indicate that the inductance value does not impact in-band performance, with higher S21 values at 5.1 GHz and 700 MHz. As seen from the simulation results and Table 3.2, increasing inductance value leads to a shift in frequency towards lower frequency.

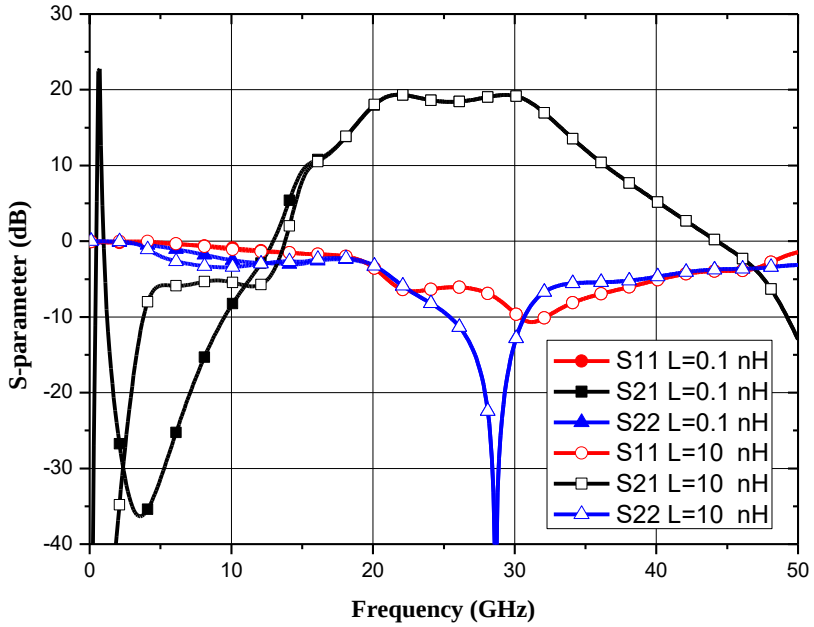

Fig. 3.44. Simulation results of common source LNA using capacitance matching with different lengths of bond wires.

Table 3.2. Low-frequency gain under different values of equivalent inductance.

L (nH)	Frequency (GHz)
0	7.6
0.1	5.1
2	1.4
10	0.6
RF choke	0.1

doi:10.6342/NTU202402726

Fig. 3.45 shows the simulated results for a common source using transmission line matching version with equivalent bonding wire inductances of 0.1nH and 10 nH. Similar to the CS using capacitance matching version case, the inductance value does not impact in-band performance, with gain peaks at 7.6 GHz and 800 MHz. Table 3.3 shows the trend is consistent with the previous circuit, where increasing inductance value shifts the frequency towards a lower frequency.

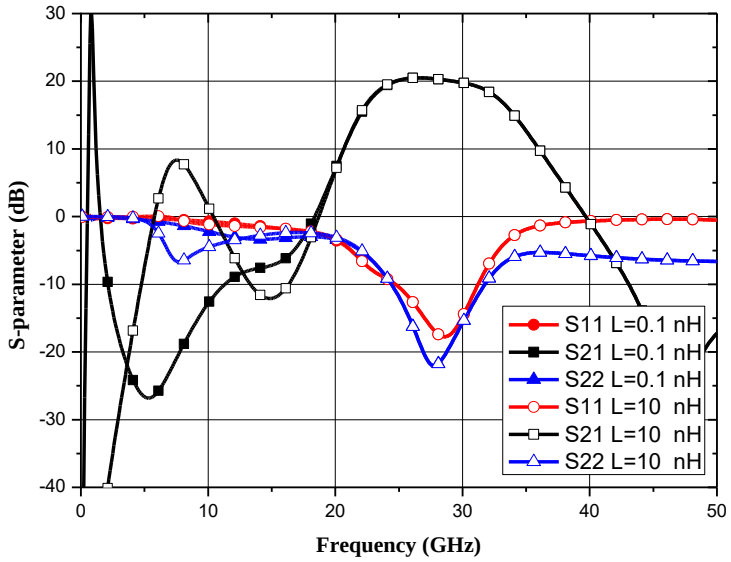

Fig. 3.45. Simulation results of common source LNA using transmission line matching with different lengths of bond wires.

Table 3.3. Low-frequency gain under different values of equivalent inductance

L (nH)	Frequency (GHz)
0	11
0.1	7.6
2	1.8
10	0.8
RF choke	0.2

doi:10.6342/NTU202402726

Fig. 3.46 shows the simulated results for the cascode version with equivalent bonding wire inductances of 0.1nH and 10nH. Similar to the other two circuits, the inductance value does not impact in-band performance, with gain peaks at 6.4GHz and 900MHz. Table 3.4 shows the trend is consistent with the previous circuit. All three circuits exhibit the same trend. The frequency shifts toward a lower frequency as the inductance value increases.

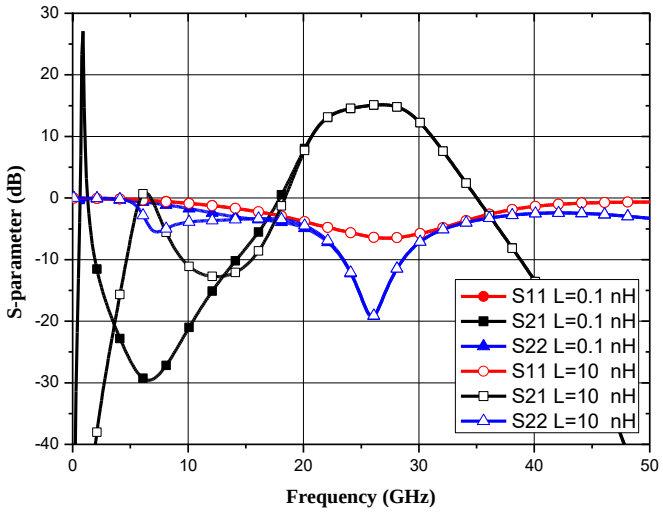

Fig. 3.46. Simulation results of cascode LNA with different lengths of bond wires.

Table 3.4. Low-frequency gain under different values of equivalent inductance

L (nH)	Frequency (GHz)
0	9.1
0.1	6.4
2	1.9
10	0.9
RF choke	0.1

doi:10.6342/NTU202402726

Due to slight discrepancies in the position and length of each circuit's bonding wire, the equivalent inductance values were fine-tuned to 2.5 nH for CS using capacitance matching version, 3.2 nH for CS using transmission line matching version, and 2.5nH for the cascode version, aligning the low-frequency gain adjustment to the same frequency.

doi:10.6342/NTU202402726

3.9 Measurement Result

3.9.1 Common Source LNA using Capacitance Matching

This 28 GHz LNA was fabricated using the 0.18 μm GaAs E-Mode pHEMT process (WIN PIH1-10). Fig. 3.47 displays the micrograph of the fabricated chip, with a total area of 1.65 x 0.75 mm^2, including DC and RF pads. To mitigate the impact of low-frequency oscillations on the circuit, DC bias is provided through bond wires. The drain bias (V_{ds}) is set at 2 V, and the gate bias (V_g) at 0.5 V, resulting in a DC power consumption of 42 mW. The S-parameters and noise figure were measured using an Agilent E8361A PNA with an input power of -30 dBm. A large-signal continuous-wave power sweep was conducted using an E8267D signal generator and an Agilent E4448A spectrum analyzer. All measurements were performed through on-wafer probing.

Fig. 3.48 illustrates the comparison of the measured S-parameters of the LNA. At 30 GHz, the LNA achieves a peak gain of 23 dB, surpassing the simulated gain by approximately 2 dB. The 3dB bandwidth spans from 19.4 to 32.1 GHz, covering 12.7 GHz, which represents 49.3% fractional bandwidth. The input return loss ranges from 2.9 to 9.9 dB within the 3dB bandwidth, and in the design target bandwidth of 25 to 31 GHz, it is within 7.9 to 9.9 dB. The output return loss within the 3dB bandwidth is from 2.5 to 29.9 dB, and in the design target bandwidth, it is within 7.9 to 29.9 dB.

Fig. 3.49 presents the measured noise figure, which ranges from 1.5 to 2.1 dB within the 3dB bandwidth and is within 1.5 to 1.9 dB in the design target bandwidth of 25 to 31 GHz. The measured NF closely matches the simulation results, and this performance significantly exceeds the target of <2.4 dB. Fig. 3.50 depicts the large-signal measurement results at 28 GHz, with an OP_{1dB} reaching 8.6 dBm. Due to the extended gain in the circuit, the measured OP_{1dB} is 1.4 dB higher than the simulation.

doi:10.6342/NTU202402726

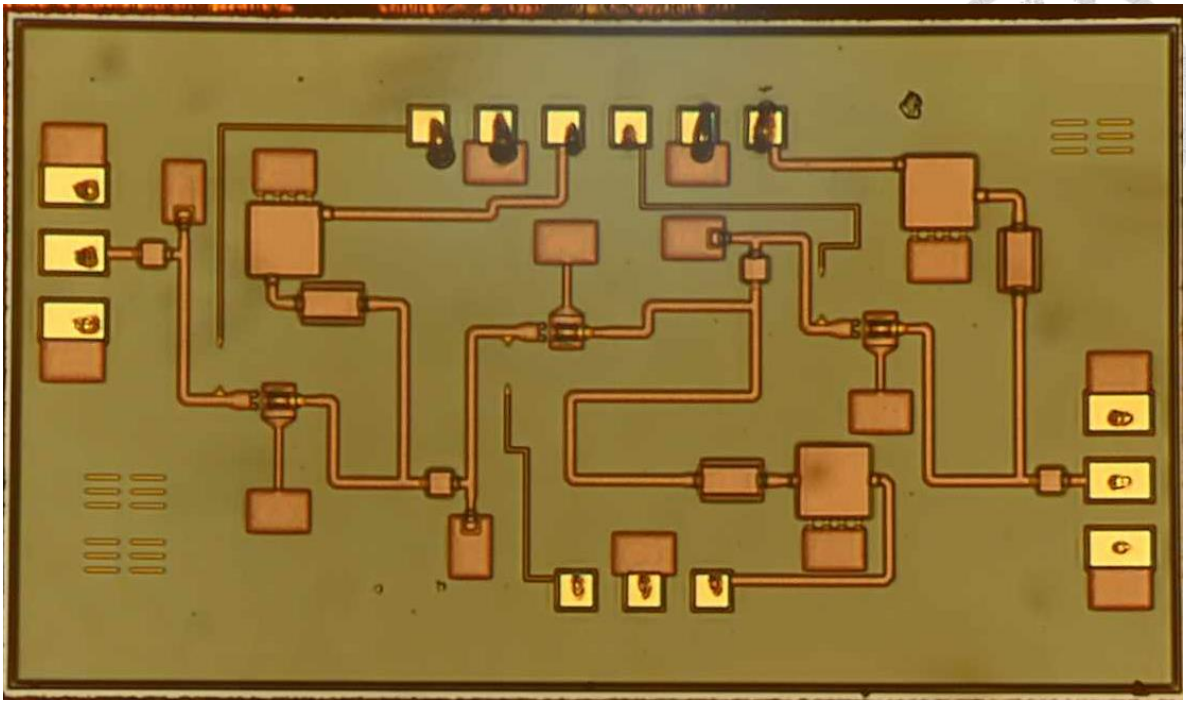

Fig. 3.47. Chip photo of the common source LNA using capacitance matching.

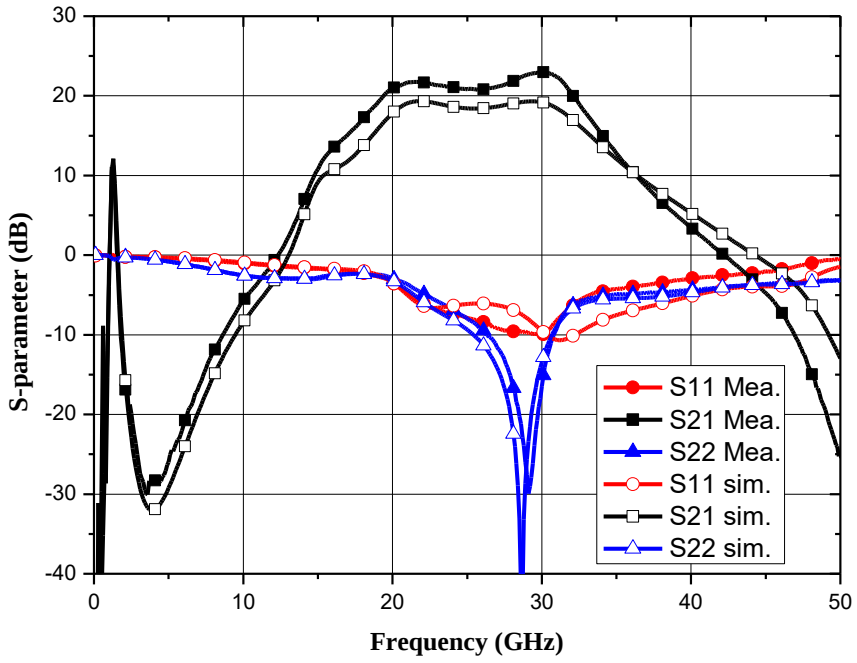

Fig. 3.48. The measured S-parameters of the common source LNA using capacitance matching.

doi:10.6342/NTU202402726

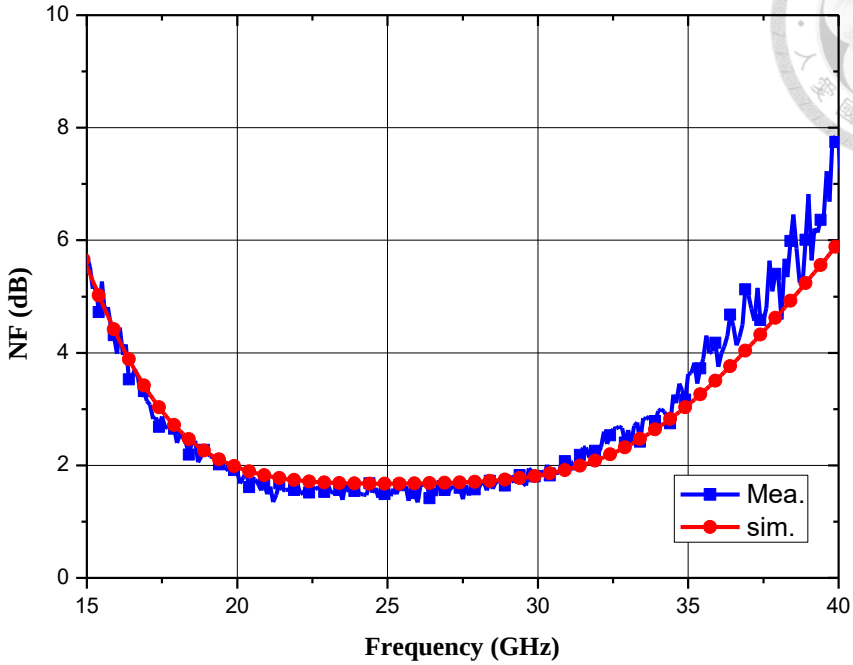

Fig. 3.49. The measured noise figure of the common source LNA using capacitance matching.

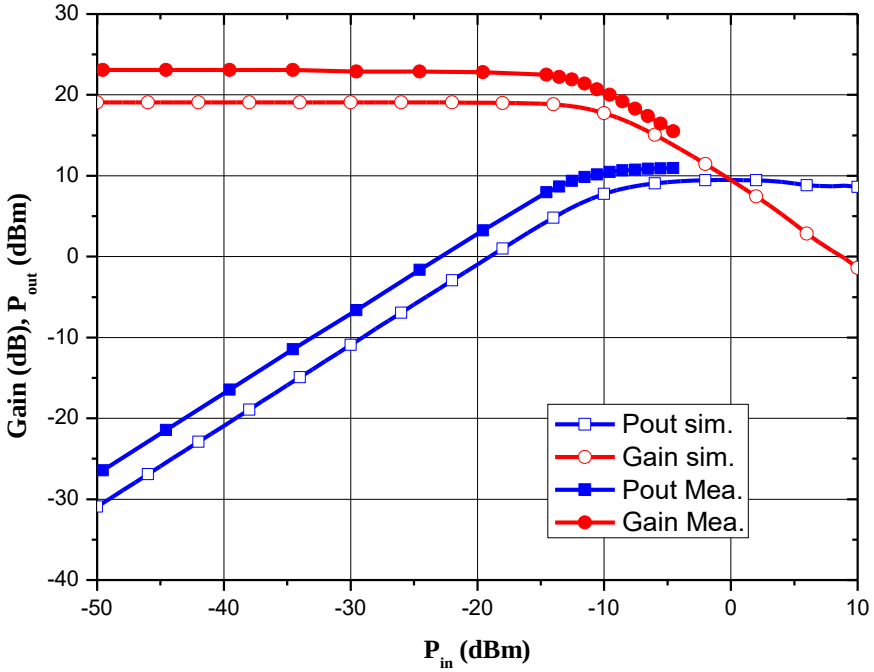

Fig. 3.50. The measured large signal performance at 28 GHz.

doi:10.6342/NTU202402726

3.9.2 Common Source LNA using Transmission Line Matching

This 28 GHz LNA was developed using the 0.18 μm GaAs E-Mode pHEMT process (WIN PIH1-10). Fig. 3.51 displays the micrograph of the fabricated chip, with a total area of 1.38 x 0.79 mm^2, including DC and RF pads. To mitigate the impact of low-frequency oscillations on the circuit, DC bias is provided through bond wires. The drain bias (V_{ds}) is set at 2 V, and the gate bias (V_g) at 0.5 V, resulting in a DC power consumption of 42 mW. The S-parameters and noise figure were measured using an Agilent E8361A PNA with an input power of -30 dBm. A large-signal continuous-wave power sweep was conducted through an E8267D signal generator and an Agilent E4448A spectrum analyzer. All measurements were performed through on-wafer probing.

Fig. 3.52 illustrates the comparison of the measured S-parameters of the LNA. The LNA reaches a peak gain of 21.5 dB at 26 GHz, and the gain trend closely aligns with the simulation results. The 3dB bandwidth spans from 22.9 to 32.9 GHz, covering 10GHz, which represents a 35.8% fractional bandwidth. The input return loss within the 3dB bandwidth ranges from 5 to 12.9dB, and in the design target bandwidth of 25 to 31 GHz, it is within 8.7 to 12.9 dB. The output return loss within the 3 dB bandwidth is from 7 to 30.6dB, and in the design target bandwidth, it is within 11.3 to 30.6 dB. Fig. 3.53 presents the measured noise figure, ranging from 1.8 to 2.9 dB within the 3dB bandwidth and within 1.8 to 2.2 dB in the design target bandwidth, achieving the specified <2.4 dB range. Fig. 3.54 shows the large-signal measurement results at 28GHz, with an OP_{1dB} reaching 11 dBm. This revised CS design reduces the chip size and improves return loss at the expense of some NF performance within the specification target.

doi:10.6342/NTU202402726

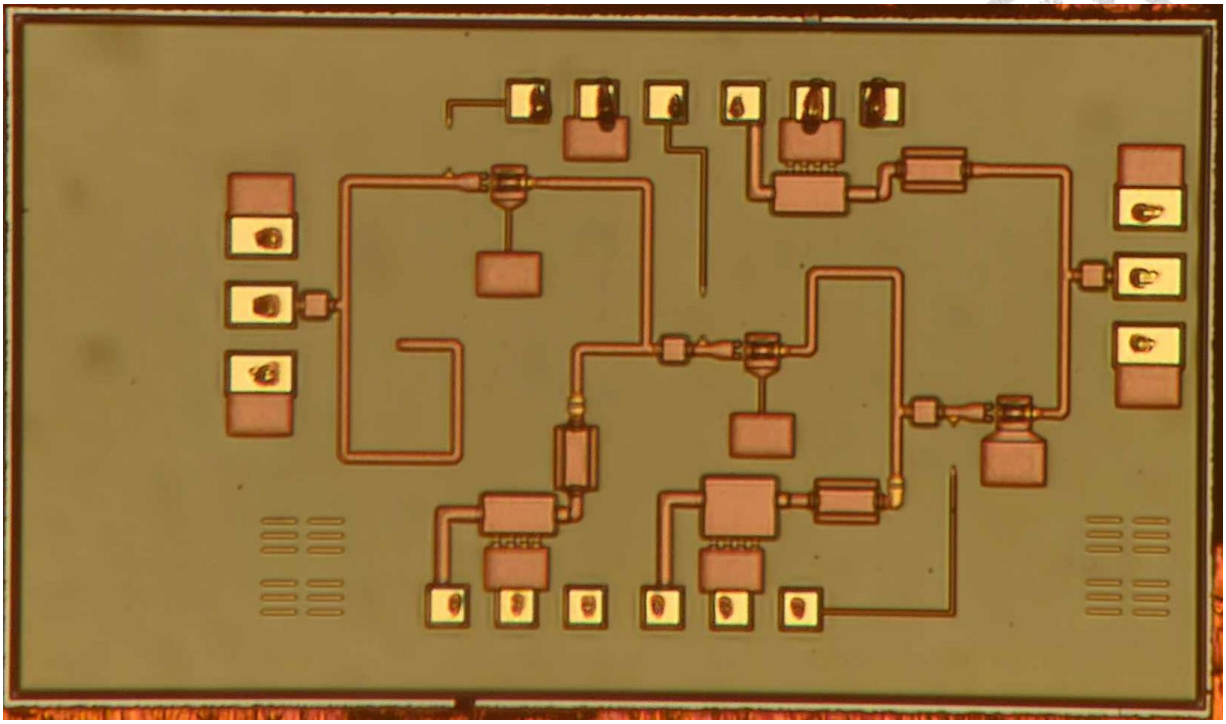

Fig. 3.51. Chip photo of the common source LNA using transmission line matching.

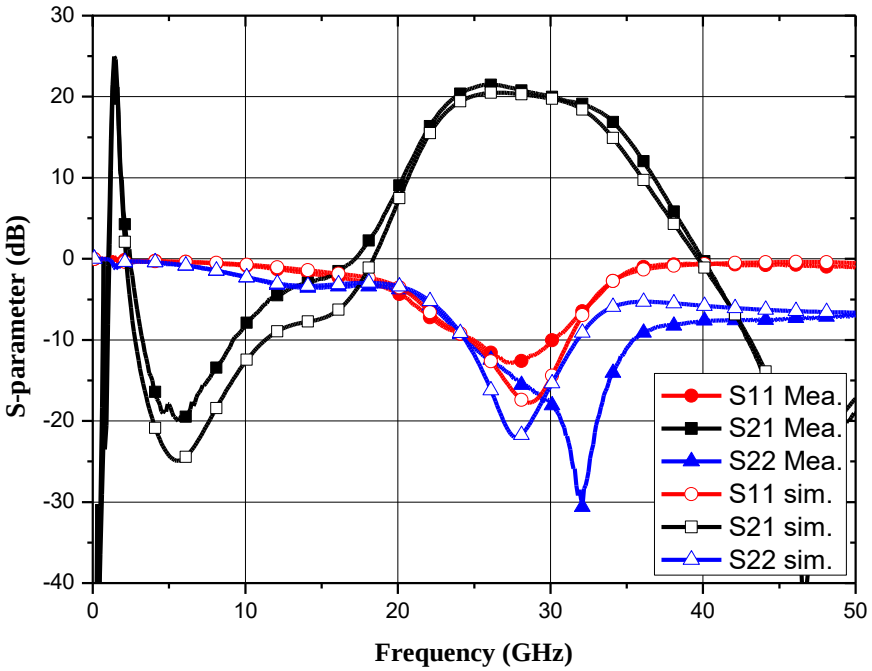

Fig. 3.52. The measured S-parameters of the common source LNA using transmission line matching.

doi:10.6342/NTU202402726

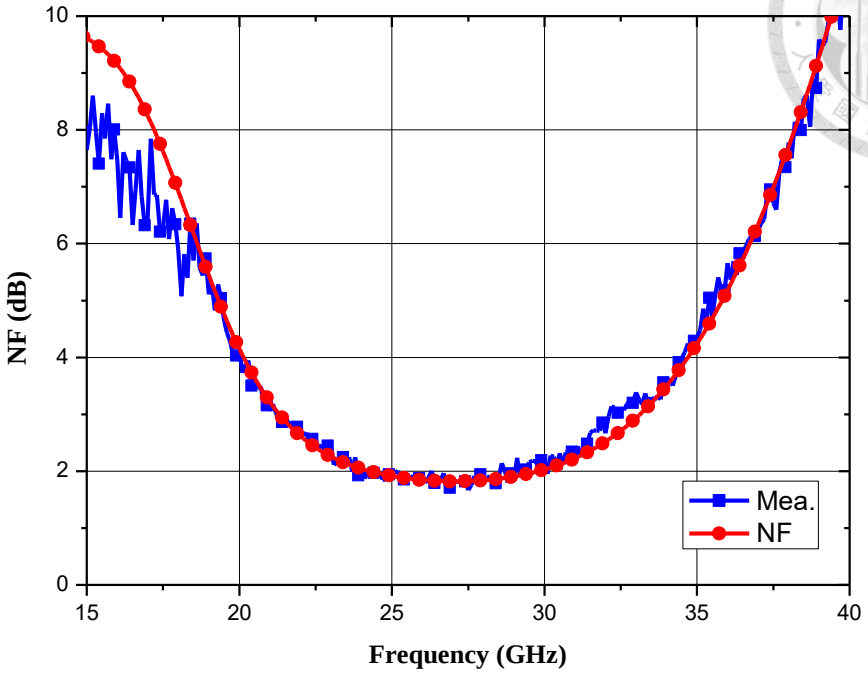

Fig. 3.53. The measured noise figure of the common source LNA using transmission line matching.

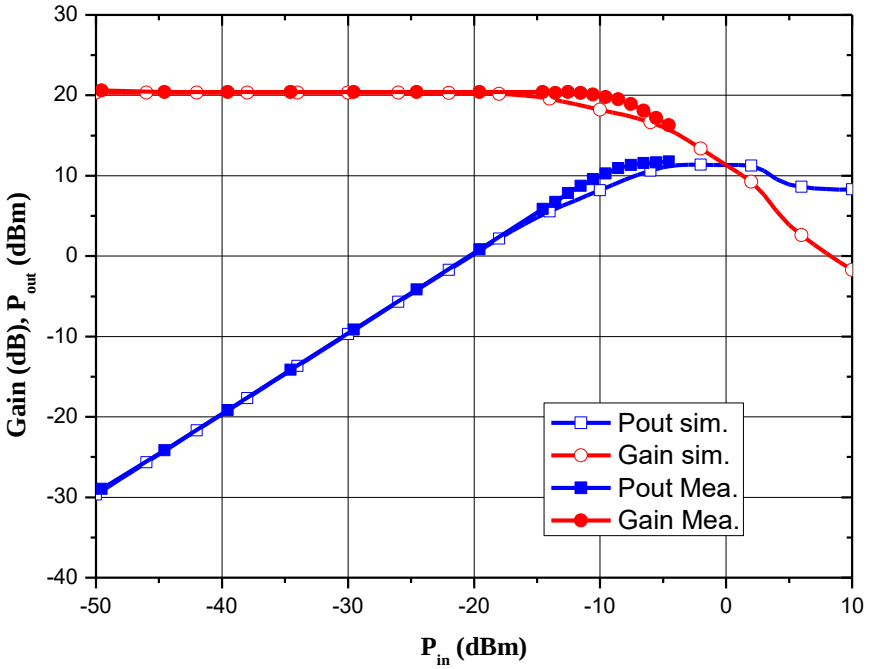

Fig. 3.54. The measured large signal performance at 28 GHz.

doi:10.6342/NTU202402726

3.9.3 Cascode version LNA

This 28 GHz LNA is fabricated using the 0.18 μm GaAs E-Mode pHEMT process (WIN PIH1-10). Fig. 3.55 displays the micrograph of the fabricated chip, with a total area of 1.33 x 0.795 mm², including DC and RF pads. To mitigate the impact of low-frequency oscillations on the circuit, DC bias is supplied via bond wires. The drain bias (V_{ds}) is set to 4 V, and the gate biases (V_{g2} and V_{g1}) are 2.5 V and 0.5 V, respectively. The DC power consumption is 56 mW. The S-parameters and noise figure are measured using an Agilent E8361A PNA with an input power of -30 dBm. The large-signal continuous-wave power sweep is measured using an E8267D signal generator and an Agilent E4448A spectrum analyzer. The measurement results are obtained through on-wafer probing.

Fig. 3.56 illustrates the comparison of the measured S-parameters of the LNA. The LNA achieves a peak gain of 15.9 dB at 28 GHz, showing a 4 dB decrease compared to the simulation results. The 3dB bandwidth extends from 21.3 to 34 GHz, covering 12.7 GHz and representing a fractional bandwidth of 45.9%, exceeding the simulated bandwidth by 2.5 GHz. The input return loss within the 3 dB bandwidth ranges from 6.5 to 15.7 dB, while the output return loss ranges from 6.3 to 26.2 dB. Fig. 3.57 presents the measured noise figure. The measured NF within the 3dB bandwidth is 2.2 to 3.8 dB, with the target bandwidth range being 2.2 to 2.6 dB. Because of the decrease in gain, the ability of the first stage to suppress noise from the subsequent stages diminishes, resulting in a deviation from the simulated results, particularly beyond 30 GHz, where it fails to meet the specified NF < 2.4dB. Fig. 3.58 presents the large-signal measurement results at 28 GHz, where the OP_{1dB} is recorded at -0.5 dBm.

doi:10.6342/NTU202402726

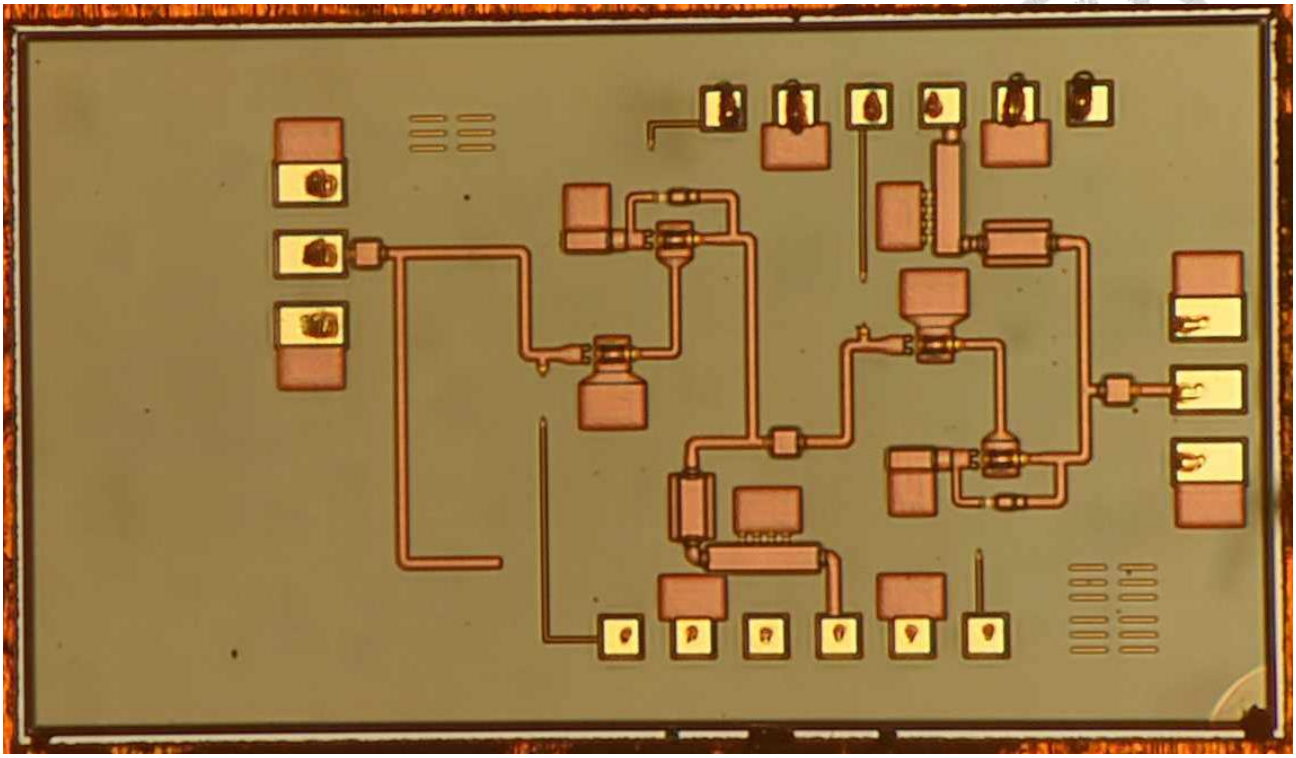

Fig. 3.55. Chip photo of the cascode version LNA.

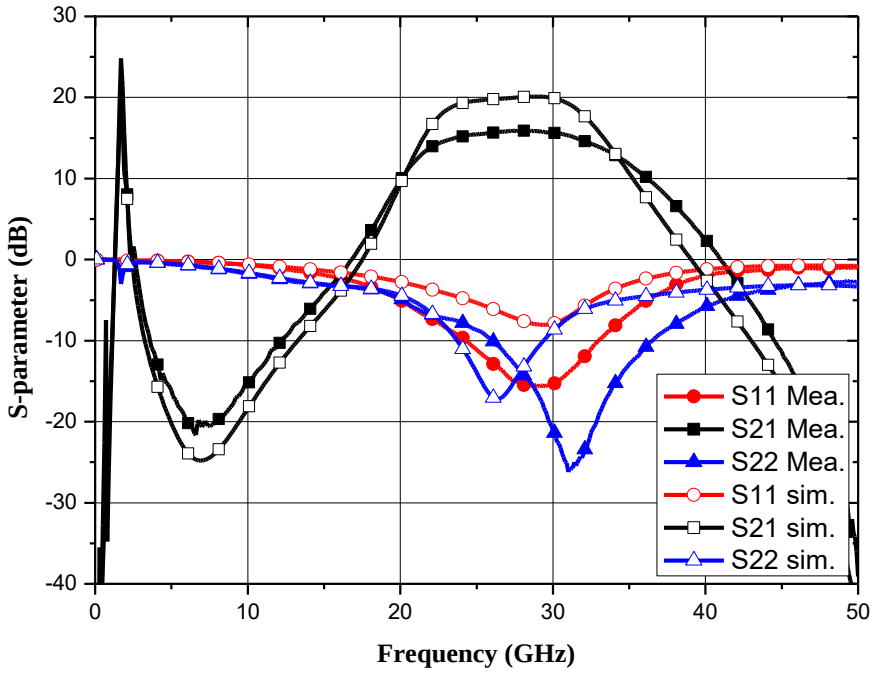

Fig. 3.56. The measured S-parameters of the cascode version LNA.

doi:10.6342/NTU202402726

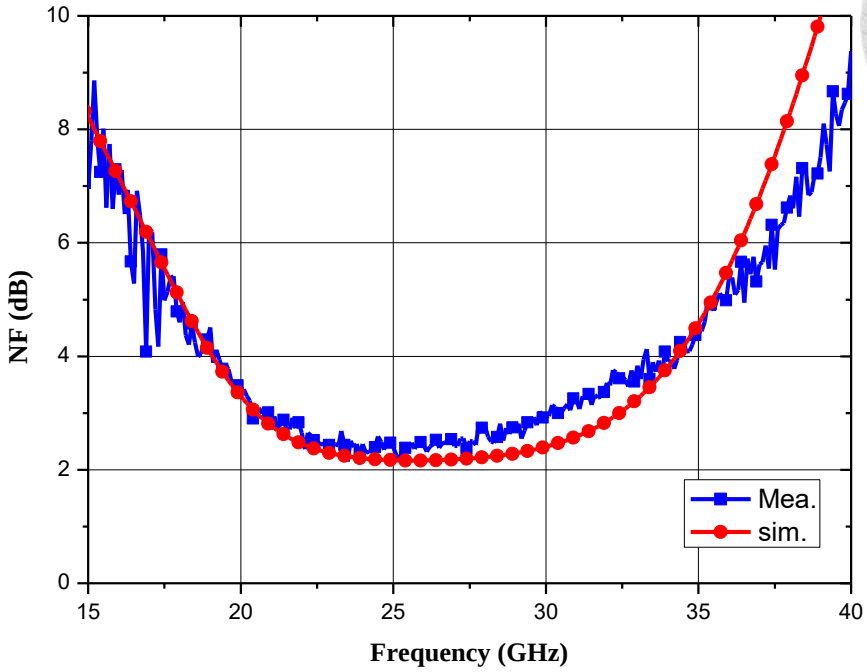

Fig. 3.57. The measured noise figure of the cascode version LNA.

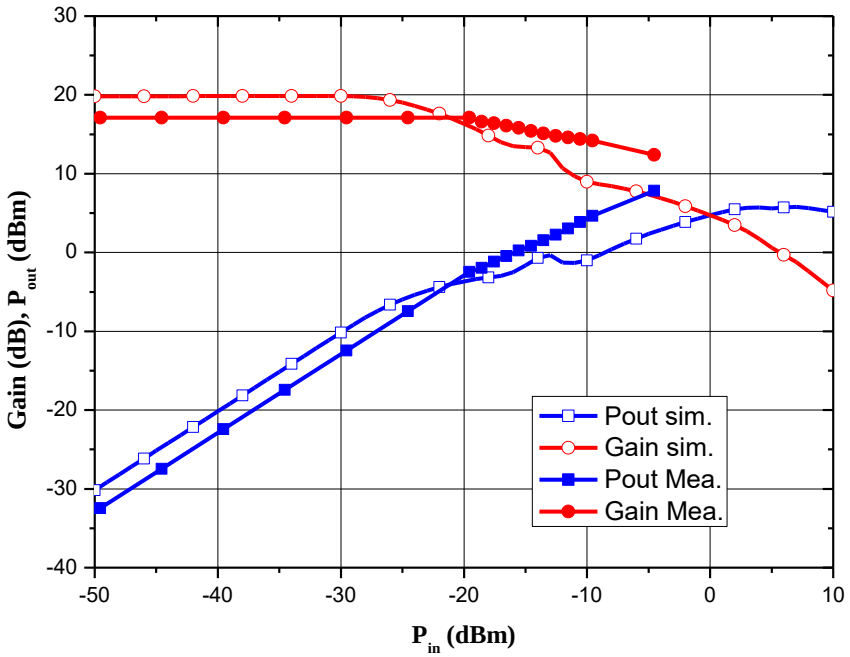

Fig. 3.58. The measured large signal performance at 28 GHz.

doi:10.6342/NTU202402726

3.9.4 Summary

In this chapter, three 28GHz LNAs fabricated using the 0.18 μm GaAs E-Mode pHEMT process (WIN PIH1-10) were designed and measured. The first LNA, employing CS using capacitance matching, utilized source degeneration and appropriate biasing to achieve excellent NF performance while effectively controlling power consumption.

To improve upon the previous version of the CS LNA, the CS using transmission line matching version reduced the use of capacitors on via in the matching circuit, thereby indirectly reducing the use of back vias and minimizing area consumption. To meet the design goal, some bandwidth, and NF characteristics were sacrificed in order to achieve a lower return loss.

Finally, an attempt was made to use a cascode architecture to reduce the number of stages and possibly make the area smaller. However, due to process variations and the asymmetry of the cascode structure, there was a significant disparity between simulation and measurement results, with a 4dB decrease in gain and a 2.5GHz increase in bandwidth. Table 3.5 summarizes recently published GaAs LNAs.

Compared to previously published GaAs LNAs, all three versions exhibited advantages in power consumption and chip area. The CS using capacitance matching version, in particular, demonstrated the best NF performance, offering potential benefits in system applications such as power savings and improved system sensitivity.

The CS using transmission line matching version had the best return loss performance of the three LNA versions and better NF performance than the other circuits in the comparison table. The cascode version, on the other hand, occupies the smallest area among the non-single-stage circuits in the comparison table. Each of the three versions of the LNA demonstrated its own unique characteristics in various aspects.

doi:10.6342/NTU202402726

Table 3.5 Comparison of published LNA in GaAs pHEMT process.

Ref.	Process	BW (GHz)	Gain (dB)	Noise Figure (dB)	OP_{1dB} (dBm)	P_{dc} (mW)	Chip Area (mm^2)
[20]	0.15 μm GaAs pHEMT	22~34	14.3	1.75	N.A.	N.A.	1*0.54
[22]	0.15 μm GaAs pHEMT	10~43	24.6	2.4	12.3	110	1.5*0.7
[18]	0.15 μm GaAs pHEMT	0.1~23	27.4	2.7	8.6	335	1.58*0.86
[21]	0.15 μm GaAs pHEMT	0.1~20	28.6	3.1	12.7	505	1.7*0.9
[27]	0.1 μm GaAs pHEMT	30~50	21.1	3.2	9.5	75.6	2*1
[19]	0.15 μm GaAs pHEMT	28.5~50.5	23	3.8	N.A.	62.6	2*1.5
[17]	0.1 μm GaAs pHEMT	18~43	21.6	1.8	11.5	140	2*1
[16]	0.1 μm GaAs pHEMT	11~39	23	2.1	8.6	80	1.7*1

doi:10.6342/NTU202402726

This work CSC	0.18μm GaAs E-Mode pHEMT	19.4~32.1	23	1.5	8.6	42	1.65*0.7
This work CST	0.18μm GaAs E-Mode pHEMT	22.9~32.9	21.5	1.7	11	42	1.38*0.79
This work cascode	0.18μm GaAs E-Mode pHEMT	21.4~34	16	2.1	-0.5	56	1.33*0.795

doi:10.6342/NTU202402726

Chapter 4 Conclusions

This thesis presents the design and implementation of a switchless bidirectional distributed amplifier in 90-nm CMOS process, and three Ka-band LNAs by using the 0.18 μm GaAs E-Mode pHEMT process for fifth-generation mobile communication (5G).

In Chapter 2, a switchless bidirectional distributed amplifier was designed in a 90-nm CMOS process. To reduce the circuit area of the transceiver, a shared matching network for the bidirectional amplifier was proposed. In order to maintain symmetry while providing sufficient variability for adjustment, a skew-symmetrical design approach for the drain and gate lines was proposed, enhancing the performance of the BDDA. The 3 dB bandwidth was measured to be 1.9 to 33.5 GHz, with a peak gain of 13.8 dB. The noise figure ranged between 2.9 and 3.9 dB, and the DC power consumption was 45.8 mW.

In Chapter 3, three Ka-band LNAs were designed using the 0.18 μm GaAs E-Mode pHEMT process. To optimize the LNA performance, the transistor size and bias were carefully selected, and source degeneration was employed in the design of the common source version to achieve excellent noise performance. Each of the three circuits exhibited distinct characteristics. The common source using capacitance matching version demonstrated the highest gain, NF, and bandwidth. The common source using transmission line matching version exhibited the best return loss. The cascode version featured the smallest chip size.

doi:10.6342/NTU202402726

REFERENCES

[1] M. -K. Cho, J. -G. Kim and D. Baek, "A Switchless CMOS Bi-Directional Distributed Gain Amplifier With Multi-Octave Bandwidth," in *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 11, pp. 611-613, Nov. 2013.

[2] D. -W. Kang, J. -G. Kim, B. -W. Min and G. M. Rebeiz, "Single and Four-Element Ka -Band Transmit/Receive Phased-Array Silicon RFICs With 5-bit Amplitude and Phase Control," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3534-3543, Dec. 2009.

[3] S. Masuda et al., "GaN single-chip transceiver frontend MMIC for X-band applications," *2012 IEEE/MTT-S International Microwave Symposium Digest, Montreal, QC, Canada, 2012*, pp. 1-3.

[4] E. Cohen, C. Jakobson, S. Ravid and D. Ritter, "A Bidirectional TX/RX Four-Element Phased Array at 60 GHz With RF-IF Conversion Block in 90-nm CMOS Process," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1438-1446, May 2010.

[5] Ping Chen, “Design of Si-Based Distributed Amplifiers for Microwave and Millimeter-Wave Applications,” Master dissertation, National Taiwan University, 2010.

[6] A. Alizadeh, M. Meghdadi, M. Yaghoobi, and A. Medi, "Design of a 2–12-GHz Bidirectional Distributed Amplifier in a 0.18- um CMOS Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 2, pp. 754-764, Feb. 2019.

[7] J. -C. Chien and L. -H. Lu, "40-Gb/s High-Gain Distributed Amplifiers With Cascaded Gain Stages in 0.18- μm CMOS," in *IEEE Journal of Solid-State Circuits*,

doi:10.6342/NTU202402726

vol. 42, no. 12, pp. 2715-2725, Dec. 2007

[8] M. Nazari, R. Rezaei Siahrood, J. Yavand Hassani and A. Farahani, "Design of a wideband low noise amplifier using modified cascode structure for 45GHz band applications," *2016 8th International Symposium on Telecommunications (IST)*, Tehran, Iran, 2016, pp. 575-580.

[9] Zuomin blog [Online] https://zuomin.blogspot.com/2009/11/rf.html

[10] Song, M. Cho, J. Kim, and J. D. Cressler, "A SiGe-BiCMOS Wideband (2–22 GHz) Active Power Divider/Combiner Circuit Supporting Bidirectional Operation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4676-4684, Dec. 2016.

[11] M. Cho, I. Song, Z. E. Fleetwood, and J. D. Cressler, "A SiGe-BiCMOS Wideband Active Bidirectional Digital Step Attenuator With Bandwidth Tuning and Equalization," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 8, pp. 3866-3876, Aug. 2018.

[12] C. Çalışkan, M. Yazıcı, M. Kaynak and Y. Gurbuz, "A Switchless SiGe BiCMOS Bidirectional Amplifier for Wideband Radar Applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 10, pp. 1844-1848, Oct. 2020.

[13] S. Sim, L. Jeon and J. -G. Kim, "A Compact X-Band Bi-Directional Phased-Array T/R Chipset in 0.13 μm CMOS Technology," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 1, pp. 562-569, Jan. 2013.

[14] David M. Pozar, Microwave Engineering, Fourth Edition, John Wiley & Sone, Inc., 2012.

[15] Yen-Chih Chen, “Design of the Broadband LNA and Ka-band PA,” Master dissertation, National Taiwan University, 2018.

[16] G. Nikandish and A. Medi, "Transformer-Feedback Interstage Bandwidth

doi:10.6342/NTU202402726

Enhancement for MMIC Multistage Amplifiers," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 2, pp. 441-448, Feb. 2015.

[17] G. Nikandish, A. Yousefi and M. Kalantari, "A Broadband Multistage LNA With Bandwidth and Linearity Enhancement," in *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 10, pp. 834-836, Oct. 2016.

[18] J. Hu, K. Ma, S. Mou and F. Meng, "Analysis and Design of a 0.1–23 GHz LNA MMIC Using Frequency-Dependent Feedback," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 9, pp. 1517-1521, Sept. 2019.

[19] Y. -T. Chou, C. -C. Chiong and H. Wang, "A Q-band LNA with 55.7% bandwidth for radio astronomy applications in 0.15-μm GaAs pHEMT process," *2016 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Taipei, Taiwan, 2016, pp. 1-3.

[20] L. -Y. Lee, Y. Wang and H. Wang, "A 25-31 GHz LNA in GaAs 0.15-μm pHEMT," *2021 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Hualien, Taiwan, 2021, pp. 1-3.

[21] J. Hu, K. Ma, S. Mou and F. Meng, "A Seven-Octave Broadband LNA MMIC Using Bandwidth Extension Techniques and Improved Active Load," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 10, pp. 3150-3161, Oct. 2018.

[22] X. Yan, P. Yu, J. Zhang, S. -P. Gao and Y. Guo, "A Broadband 10–43-GHz High-Gain LNA MMIC Using Coupled-Line Feedback in 0.15-μm GaAs pHEMT Technology," in *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 12, pp. 1459-1462, Dec. 2022.

[23] J. -S. Seo, J. -H. Hwang, K. -J. Kim and G. -H. Ahn, "High Linearity Ka-band GaN Hemt Low Noise Amplifier," *2021 International Conference on Information and Communication Technology Convergence (ICTC)*, Jeju Island, Korea, Republic of,

doi:10.6342/NTU202402726

2021, pp. 383-385.

[24] Shou-Hsien Weng, Chi-Hsien Lin, Hong-Yeh Chang and Chau-Ching Chiong, "Q-band low noise amplifiers using a 0.15μm MHEMT process for broadband communication and radio astronomy applications," *2008 IEEE MTT-S International Microwave Symposium Digest*, Atlanta, GA, USA, 2008, pp. 455-458.

[25] P. -H. Ho, C. -C. Chiong and H. Wang, "An ultra low-power Q-band LNA with 50% bandwidth in WIN GaAs 0.1-μm pHEMT process," *2013 Asia-Pacific Microwave Conference Proceedings (APMC)*, Seoul, Korea (South), 2013, pp. 713-715.

[26] Zuomin blog [Online] https://zuomin.blogspot.com/2017/09/blog-post.html

[27] S. -H. Chang, C. -C. Chiong, K. -Y. Kao and H. Wang, "A Q-band amplifier with low noise figure and medium output power capability for ALMA band-1 receiver," *2017 IEEE Asia Pacific Microwave Conference (APMC)*, Kuala Lumpur, Malaysia, 2017, pp. 755-758.

[28] W. -H. Tsai, Y. Wang and H. Wang, "A Switchless Bidirectional Distributed Amplifier with 2-dB Gain Variation in One Decade Frequency Range in 90-nm CMOS Process," 2022 *IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Busan, Korea, Republic of, 2022, pp. 71-73

[29] Yu-Ting Chou, “Research of Low Noise Amplifier, I/Q Demodulator, and Power Amplifier for Millimeter-wave Application,” Master dissertation, National Taiwan University, 2016.

[30] Bo-Jr Huang, “Design and Analysis of Microwave and Millimeter-wave RF Electrostatic Discharge Protection and Millimeter-wave Multi-Cascode Low Noise Amplifiers ,” Doctor dissertation, National Taiwan University, 2010.

doi:10.6342/NTU202402726