國立臺灣大學電機資訊學院電信工程學研究所

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Master’s Thesis

應用於 D 頻段之倍頻器、5G 通訊之低雜訊放大器及應用於次世代相控陣列雙向放大器之設計

Design of D-band Frequency Doubler, Low-Noise Amplifiers for 5G Communication and Bidirectional Amplifier for Next-Generation Phased-Arrays

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中文摘要

在這本論文由以下三個部分組成，一個 D 頻段低功耗高轉換增益之倍頻器和一個 K_a 頻段低雜訊放大器與 W 頻段雙向功率低雜訊放大器的設計與量測結果。

首先是預計作為 D 頻段訊號源之倍頻器，使用的製程為 28 奈米金氧半場效電晶體，此倍頻器使用馬遜平衡器來產生 180°相位差之訊號，並透過選擇偏壓點在 Class-B 使電路有最多的諧波項，最高的轉換增益可達-4.5 dB，而輸出 3dB 頻寬從 126-146 GHz，達到 15% 的比例頻寬。

第二部分提出應用於 K_a 頻段接收機中之低功耗低雜訊放大器，使用的製程為 90 奈米金氧半場效電晶體。此電路使用雙重變壓器耦合與電流共用技術與在第一級提供足供增益及低雜訊之表現，而在第二級使用本人所提出消除寄生效應之雙重變壓器耦合進而去提高整體電路的表現。量測結果顯示此顆低雜訊放大器具有 18 GHz 之頻寬以及 19.7 dB 的增益，並且在 30 GHz 只有 3.2 dB 的雜訊指數

最後提出的是設計於 W 頻段的雙向功率低雜訊放大器並且比較了有以開關作為切換模態的方式與基於變壓器架構之無開關兩者之間的優劣。無開關功率低雜訊放大器(Switchless bidirectional PA-LNA)，使用選擇電晶體大小與匹配電路使其在 OFF 模態時有開路之效果，此時變壓器耦合的匹配電路就有虛擬開關(Virtual Switch)之效果。以此方式設計電路可以同時保有低雜訊放大器與功率放大器之效果，並且可以省去不少的面積。此無開關之功率低雜訊放大器在低雜訊放大器模式有 18.5 dB 的小訊號增益、21 GHz 的 3-dB 頻寬以及在 81 GHz 有 7 dB 的最小雜訊指數，然而在功率放大器的模式則有 17.2 dB 的小訊號增益和飽和輸出功率則有 10 dBm 和 9.1% 最高功率附加效率的表現。而在有開關的版本中，在輸出與輸入端使用單刀雙擲開關(SPDT switch)去使得訊號在 OFF 模態時能有更開路之效果，相對的則會有 switch 的損耗需要考慮。此有開關之功率低雜訊放大器在低雜訊放大器模式有 18.6 dB 的小訊號增益、25 GHz 的 3-dB 頻寬以及在 81 GHz 有 7.1 dB 的最小雜訊指數，然而在功率放大器的模式則有 18.2 dB 的小訊號增益和則飽和輸出功率有 10 dBm 和 9 %最大附加效率的表現。

關鍵字:互補式金氧半導體、寬頻放大器、變壓器匹配網路、功率放大器、低雜訊放大器、無開關雙向放大器、雙向放大器、K_a 頻段、單刀雙擲開關、W 頻段、

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D 頻段。

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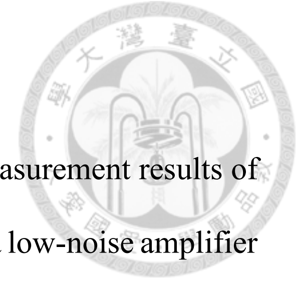
ABSTRACT



This paper comprises three main sections: the design and measurement results of a low-power, high-conversion-gain D-Band frequency multiplier, a low-noise amplifier (LNA) for the K_a-Band, and a bidirectional low-noise amplifier tailored for the W-Band.

The first section focuses on the D-Band frequency multiplier intended to serve as a signal source. It is fabricated using a 28-nanometer CMOS process and utilizes a Marchand-Balun to generate signals with a 180° phase difference. By optimizing the bias point in Class-B, this circuit achieves a peak conversion gain of -4.5 dB. It provides a 3dB output power bandwidth ranging from 126 to 146 GHz, achieving a 15% fractional bandwidth.

The second part introduces a low-power LNA designed for the K_a-Band receiver, fabricated using a 90-nanometer CMOS process. This circuit employs dual transformer coupling and current-sharing techniques in the first stage to deliver ample gain and low-noise performance. In the second stage, a novel dual transformer coupling approach, designed to mitigate parasitic effects, enhances the overall circuit's performance. Measurement results reveal that this LNA offers an 18 GHz 3-dB bandwidth, a gain of 19.7 dB, and a noise figure of only 3.2 dB at 30 GHz.

The final section presents the design of a bidirectional low-noise amplifier for the W-Band and compares two modes: a switchless bidirectional PA-LNA and a switch-based design using transformer configurations. The switchless design achieves an open circuit effect in OFF mode by selecting transistor sizes and matching circuits. This approach emulates a virtual switch within the transformer-coupled matching network. This design enables the circuit to simultaneously function as a low-noise amplifier and a power amplifier while conserving space. In the switchless version, the low-noise amplifier mode provides an 18.5 dB small-signal gain, a 21 GHz 3-dB bandwidth, and

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a minimum noise figure of 7 dB at 81 GHz. In power amplifier mode, it achieves 17.2 dB small-signal gain, a saturated output power (P_{sat}) of 10 dBm, and a 9.1% peak power-added efficiency (PAE_{MAX}).

In the switch version, single-pole double-throw (SPDT) switches at the input and output create open circuits in OFF mode, though there are switch-related losses to consider. In this configuration, the low-noise amplifier mode offers an 18.6 dB small-signal gain, a 25 GHz 3-dB bandwidth, and a minimum noise figure of 7.1 dB at 81 GHz. In power amplifier mode, it provides an 18.2 dB small-signal gain, a saturated output power (P_{sat}) of 10 dBm, a 9% peak power-added efficiency (PAE_{MAX}).

Index Terms – CMOS, wideband amplifier, transformer, power amplifier, low noise amplifier, switchless bidirectional amplifier, K_a band, SPDT, W band, D band.

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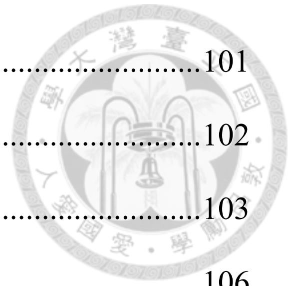

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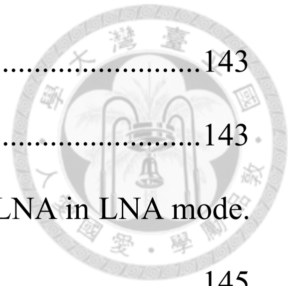

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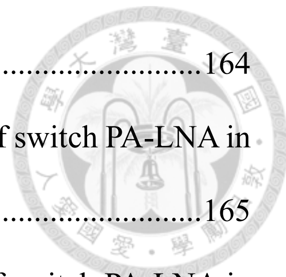

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Chapter 1 Introduction

1.1 Background and Motivation

In recent decades, wireless communication technologies have evolved to higher frequency bands due to the rapid advancement of communication systems. Therefore, it has prompted researchers to explore the potential applications of the D-Band frequency range, spanning from 110 to 170 GHz [1][2]. The D-Band, with its wide bandwidth and unique characteristics, facilitates high-speed data transmission, making it suitable for applications such as wireless communication, data centers, and video streaming. Moreover, the D-Band's advantages extend to radar systems, where it offers finer object discrimination and improved performance, especially in adverse weather conditions. This results in enhanced resolution and accuracy in obstacle detection and target tracking. Beyond wireless communication and radar, the D-Band holds promise for high-resolution imaging, sensing applications, and radio astronomy observations. Its contributions span various fields, such as medical imaging, archaeological research, and the exploration of celestial objects [3].

Designing voltage-controlled oscillators (VCOs) with good phase noise, a wide tuning range, and sufficient output power becomes challenging at high frequencies, as indicated by previous research [4]. Consequently, a common approach involves cascading a frequency doubler with a low-frequency oscillator to create a high-frequency signal source. This technique allows for the generation of signals within the desired D Band frequency range while mitigating the constraints associated with direct VCO designs. By doubling the frequency of a lower frequency oscillator, the resultant signal is adjusted to fall within the D Band range, offering a viable solution for high-frequency applications.

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Therefore, a frequency multiplier design for D Band applications will be introduced.

A high gain broadband low-power consumption monolithic microwave integrated circuit (MMIC) Low-Noise Amplifier (LNA) using a 90-μm complementary metal-oxide-semiconductor field-effect transistor (CMOSFET) process will be presented. This LNA is designed to cover the ka-band frequency range, which spans from 21 to 40.2 GHz. The need for broadband communication systems capable of high-rate data transmission has become increasingly critical due to the rising popularity of smart handsets and the growing demand for multimedia applications. To meet the requirements of wireless communications, the Federal Communications Commission (FCC) has allocated a spectrum range of 3.1 to 10.6 GHz for ultra-wideband (UWB) applications [5]. Furthermore, the FCC has released frequency ranges of 22 to 29 GHz for short-range automotive radar systems [6] and 57 to 71 GHz for wireless personal area networks (WPANs) [7]. These wide unlicensed bands have created opportunities for a wide range of applications, including high-speed links, high-resolution radar, wideband phased-array systems, and wideband commercial radio systems. As a result, the development of an ultrawideband Low-Noise Amplifier (LNA) is of paramount importance to effectively utilize these extensive frequency bands.

The frequency bands from 71 to 76 GHz, 81 to 86 GHz, and 92-95 GHz, collectively known as the W-band and covering the range of 70-110 GHz, are globally authorized for wireless communications [7]. These available 13 GHz bands offer higher data rates compared to lower microwave frequency bands. While these frequency bands demonstrate significant efficacy, they also pose challenges specific to millimeter-wave outdoor communications, including high path loss (a reduction in signal strength with distance) and weak diffraction ability (the ability of waves to bend around obstacles), making them susceptible to obstruction. To address these issues, the phased-array

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technique has been developed [8]-[10], which involves the use of numerous antenna arrays to mitigate the problem of high path loss.

The phased-array transceiver combines both transmitter (TX) and receiver (RX) functions. However, implementing a phased-array system poses challenges due to the requirement for TX and RX circuits, resulting in increased chip area and cost considerations. An efficient solution is to operate the transceiver in time-division duplexing (TDD) mode, where the TX and RX components function in different time slots while utilizing the same antenna [9]. In a TDD phased-array transceiver, the front-end circuit plays a critical role as depicted in Fig. 1.1, as it determines the system's output power, efficiency, and noise figure. Hence, designing a front-end with well-balanced TX/RX performance is crucial.

Traditionally, a T/R switch, such as a single-pole double-throw (SPDT) switch, is employed for bidirectional amplifier selection and isolation. However, SPDT switches typically introduce insertion loss of approximately 2 to 2.5 dB at W-band [11]. This not only compromises the output power (P_{out}) and power-added efficiency (PAE) in the TX path but also directly contributes to the system's noise figure in the RX path. Therefore, for a phased-array transceiver, there is a desire for switchless bidirectional PA-LNAs that eliminate the need for SPDT switches, while preserving the original performance of the power amplifier (PA) and low-noise amplifier (LNA) [12]-[15]. A comprehensive design introduction of both switchless and switch-based bidirectional PA-LNAs will be presented.

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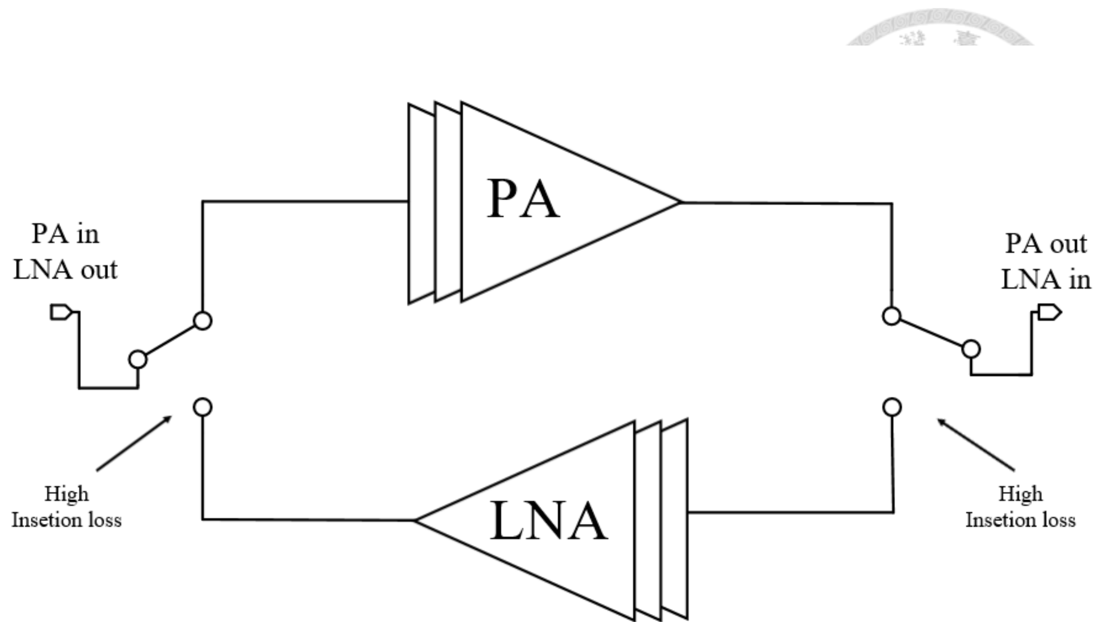

Fig. 1.1 Block diagram of the conventional front-end circuit.

Due to significant advancements in semiconductor technology, the field of monolithic microwave integrated circuits (MMICs) and radio frequency integrated circuits (RFICs) has reached a mature stage. This progress has enabled the development of highly integrated, cost-effective solutions for system-on-a-chip (SOC) implementations. As a result, advanced CMOS processes have emerged as the predominant choice for constructing RF transceivers, offering benefits such as high integration, improved yield, and reduced costs. Against this backdrop, the primary focus of this dissertation will be on conducting research related to Si-based amplifiers for microwave and millimeter-wave applications.

1.2 Literature Survey

The literature surveys include D band Multiplier and Ka-band LNAs and W-Band bidirectional PA-LNAs design in CMOS Process.

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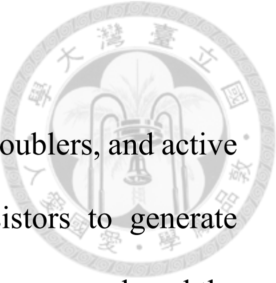
1.2.1 D-Band Frequency Multiplier in CMOS Process



There are multiple topologies available for designing frequency doublers, and active doublers often make use of the nonlinear characteristics of transistors to generate harmonic signals [16]-[19]. In these designs, the fundamental tone is suppressed, and the second harmonic is extracted using differential methods. Table 1.1 provides an overview of previously published frequency doublers in the D-band.

One of the referenced papers, [4], presents a single-end 55-85 GHz doubler implemented using 65-nm CMOS technology and featuring a Marchand balun with compensation line. This design achieves a conversion gain of -10 dB and a 3-dB bandwidth of 50%. Another study [16] describes a high-efficiency D-Band push-push doubler fabricated in 22-nm FDSOI technology. It achieves an output power of 4.1 dBm with an input power of 10 dBm. The peak dc-to-RF efficiency (P_{out}/P_{DC}) is 11.8%, and the total efficiency ($P_{out}/(P_{IN}+P_{DC})$) is 8.2%. In the work presented in [17], a wideband (96–134 GHz) frequency doubler is developed using a distributed amplifier and a nonlinear transmission line. The incorporation of a distributed amplifier structure enables the frequency multiplier to exhibit a wide 33% instantaneous 3-dB bandwidth, spanning from 96 to 134 GHz. The measured peak conversion gain is -6.2 dB, and the conversion efficiency is 8.3% at an output frequency of 118 GHz. Additionally, the study described in [18] focuses on the design of a high-power doubler for F-band frequencies, covering the range of 105-130 GHz. This doubler is implemented using a low voltage process of 1.1 V in 28nm CMOS technology. A novel approach is proposed to reduce the doubler chip size, involving the shorting of the 2nd harmonic in the input network and the balancing of the input balun at the fundamental frequency. The doubler achieves a peak output power of +4 dBm at 120 GHz with an efficiency of 18% at a bias voltage of 0V. It also exhibits a peak gain of -2.2 dB. Thanks to the utilization of a transformer, this doubler

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has a smaller size, measuring only 0.03 mm^2 compared to the Marchand balun. Finally, in the paper referenced as [19], the authors discuss the use of the SOI (Silicon-on-Insulator) process for fabricating frequency doublers. They emphasize the significance of optimizing the transistor dimensions to achieve optimal performance. The doubler presented in this work demonstrates a measured peak power of +3.5 dBm at 150 GHz and surpasses 2 dBm within the frequency range of 140-160 GHz. These results are obtained with a bias voltage of 1 V. To achieve these power levels, an input power of 7-8 dBm at 70-80 GHz is necessary, resulting in a conversion gain of -4 to -5 dBm. Therefore, it is still a challenge to design a D band frequency doubler with high conversion gain, fundamental rejection, and low power consumption.

Table 1.1 Summary of previously published Frequency doubler

Ref.	**Process**	**BW (GHz)**	**CG* (dB)**	**Pout@Pin (dBm)**	**FR** (dB)**	**Pdc (mW)**	**Total Efficiency (%)**
[4]	65-nm CMOS	95-150	-8	3@11	>33	22.8	5.6
[16]	22-nm FDSOI	125-145	-5.5	4.1@9.6	>15	24.7	8.2
[17]	28-nm CMOS	96-134	-6.2	1.8@8	N/A	12	12
[18]	28-nm CMOS	105-130	-2	4@6.2	>16	14	11
[19]	45-nm CMOS SOI	135-160	-4	3.5@6.5	N/A	25	6.2

*: CG: Conventional Gain **FR: Fundamental Rejection
Total Efficiency= $P_{out}/(P_{IN}+P_{DC})$

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1.2.2 K_a-band LNA in CMOS Process

Table 1.2 compiles recent publications focusing on Ka-band CMOS low-power LNAs, which are designed to address thermal considerations and leverage the low-power characteristics of CMOS technology. As CMOS processes advance, reducing the supply voltage has become a prevalent technique to improve power efficiency and accelerate digital data processing. Therefore, CMOS technology is well-suited for low-power LNA design [21].

In addition to advancements in semiconductor processes, various design techniques are employed to reduce power consumption while maintaining satisfactory LNA performance. One such technique is the 'current-reuse topology' [22][23], where two transistors share a common DC path. By introducing an LC tank to cascade two stages in the AC path, it becomes possible to minimize power consumption. However, it's important to note that the cascode topology used in the DC path requires a doubled supply voltage, which can compromise its efficiency in power reduction and may lead to decreased gain. To address this, low-power LNA designs often adopt the 'transformer-feedback technique' to enhance gain performance [24]. Another approach involves the 'forward body-biased technique,' which aims to decrease the threshold voltage (V_{TH}) and subsequently reduce the supply voltage (P_{dc}) [25]. However, it's worth mentioning that this method can result in increased current, limiting its effectiveness in overall power reduction.

For simultaneous noise and input impedance matching, a traditional method involves introducing 'inductive degeneration' at the source terminal of the transistor [26]. Additionally, the 'gate-source transformer-feedback technique' is commonly used in the first stage of an LNA [27].

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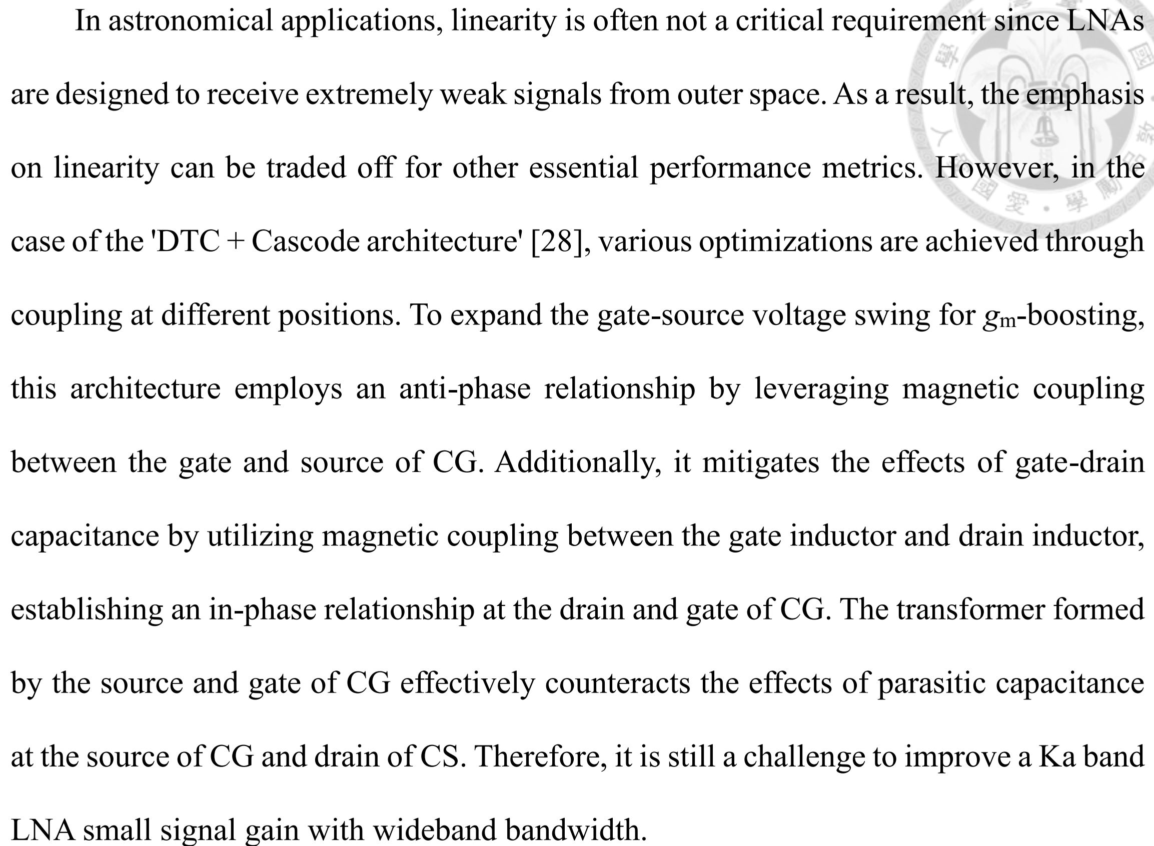

In astronomical applications, linearity is often not a critical requirement since LNAs are designed to receive extremely weak signals from outer space. As a result, the emphasis on linearity can be traded off for other essential performance metrics. However, in the case of the 'DTC + Cascode architecture' [28], various optimizations are achieved through coupling at different positions. To expand the gate-source voltage swing for g_m-boosting, this architecture employs an anti-phase relationship by leveraging magnetic coupling between the gate and source of CG. Additionally, it mitigates the effects of gate-drain capacitance by utilizing magnetic coupling between the gate inductor and drain inductor, establishing an in-phase relationship at the drain and gate of CG. The transformer formed by the source and gate of CG effectively counteracts the effects of parasitic capacitance at the source of CG and drain of CS. Therefore, it is still a challenge to improve a Ka band LNA small signal gain with wideband bandwidth.

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Table 1.2 Summary of previously published Ka-Band LNA.

Ref.	Process	RF freq. (GHz)	3-dB BW	Peak Gain	NF (dB)	P_{dc} (mW)	IP_{1dB} (dBm)	FOM
[22]	0.18-µm CMOS	25	6	10.8	4.6	3.6	N/A	3.07
[25]	0.18-µm CMOS	25	4	11	5.2	4.9	-16	1.25
[28]	65-nm CMOS	24.9-32.5	7.6	18.33	3.2-4.2	20.5	-24	3.08
[29]	90-nm CMOS LP	24-48	24	20	3.1	21.1	N/A	10.9
[30]	65-nm CMOS	15.8-30.3	14.5	10.2	3.3-5.7	12.4	N/A	3.3
[31]	40-nm CMOS	28	7.4	27.1	3.3-4.3	31.4	N/A	4.7
[32]	22-nm FDSOI CMOS	22-32	10	18.6	2.1-2.9	5.6	N/A	22.6
[33]	22-nm SOI CMOS	24-43	19	23	3.1-3.7	20.5	N/A	12.6
[34]	65-nm CMOS	21-41	20	28.5	2.7-3.2	32	N/A	19.3

$$FoM = \frac{Gain[abs.] \times BW[GHz]}{(F-1) \times P_{dc}[mW]}.$$

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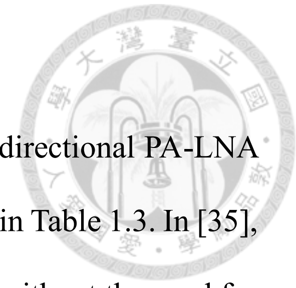
1.2.3 W-Band Bidirectional PA-LNA in CMOS Process



In recent years, there have been significant advancements in bidirectional PA-LNA designs. Previous research on bidirectional PA-LNAs is summarized in Table 1.3. In [35], a novel approach is presented for designing a bidirectional PA-LNA without the need for switches. This is accomplished by optimizing transistor size and employing transformers for impedance matching. By implementing this method, the circuit ensures that the impedance on the alternate path closely resembles an open circuit when operating in LNA or PA mode, thus preserving the desired circuit characteristics. Consequently, this technique eliminates losses caused by switches and leads to a reduction in the overall size of the chip. The DA structure requires multiple gain cells to form artificial transmission lines, leading to high power dissipation and occupying a large chip area [35]. Another reference [36] employed shunt inductors as impedance toggling components to prevent signal leakage and as impedance matching elements for the PA and LNA. This approach demonstrated an effective way to jointly design the core circuits of the PA and LNA. In a 130-nm SiGe BiCMOS process, a dual-band bidirectional PA-LNA was proposed using the shunt switch technique. This method introduced a new approach for shifting between different frequency bands. However, the PA/LNA mode switching in this design still relied on switches. Previous studies have shown that achieving good RF performance in both PA and LNA modes simultaneously requires a higher-level IC process (0.13-um SiGe BiCMOS) or III-V semiconductor technology (0.25-um GaN HEMT). Consequently, the realization of a millimeter-wave (mm-wave) switchless bidirectional PA-LNA, utilizing a 90-nm CMOS process with a low noise figure (<5 dB) in LNA mode and excellent power-added efficiency (>20%) in PA mode, remains a formidable challenge. Therefore, it is still a challenge to design a bidirectional PA-LNA with wideband and operating in high frequency.

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Table 1.3 Summary of previously published mixers with improved linearity.

Ref.	[15]	[35]	[36]	[37]	
Process	90-nm CMOS	65-nm CMOS	0.13-μm SiGe	0.13-μm SiGe	
Topology	Switchless Bi-directional PA-LNA	Switchless Bi-directional PA-LNA	Switchless Bi-directional PA-LNA	Dual-Band Bidirectional PA-LNA	
3-dB Freq.	29.9~39.4 (PA) 34.5~38.7 (LNA)	58~62.5(PA)* 58~67(LNA)*	57~66 (PA&LNA)	28~34(PA)* 25~35(LNA)*	44~65(PA)* 55~65(LNA)*
Tx Peak Gain(dB)	18.1	24.5	16.5	14.1	14.7
Tx OP_{1db} (dBm)	13.3	N/A	11	14.7	7.2
Tx P_{sat} (dBm)	15.2	8.4	12*	16.3	16
Tx PAE_{max} (%)	29	8.7	11	23.6	15.2
Rx Peak Gain(dB)	18.1	21.5	17	13.9	14.1
Rx Min.NF(dB)	4.5	6.7	6.5	4.2	4.6
Rx IP_{1db} (dBm)	-16~-20	N/A	-20	-13	-13.5
Rx P_{dc} (mW)	24.7	39.6	36	10	24

*Estimated from the figured

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1.3 Contributions

This dissertation presents three research contributions. Firstly, a high conversation gain and low power consumption D-band multiplier is introduced, incorporating g_m-boosting technology to improve output power. Secondly, a low power consumption high gain 22 to 40 GHz LNA with new type Double-Transformer-Coupler (DTC) is developed for 5G applications. Lastly, a comparison is conducted between W-band bidirectional PA-LNAs with and without switch for beamformer applications. The method efforts contribute to advancements in enhancing power efficiency, achieving high gain, and evaluating suitable architectures for beamforming applications. The major contribution of these researches is described as follows.

1.3.1 D-band Frequency Multiplier in CMOS process

The design flow and measurement outcomes of a broadband frequency doubler operating within the 126-146 GHz range is presented. This doubler was implemented in 28-nm CMOS process. In previously published works, it is shown that conversion gain often involves a trade-off in fundamental rejection. Therefore, in this frequency doubler, a balanced cascode with g_m-boosting topology is employed to enhance power performance and improve conversion gain. Simultaneously, a built-in low-pass filter has been integrated to enhance the rejection of harmonic frequencies. Additionally, a Marchand balun is utilized to generate wideband balanced differential signals to further improve fundamental rejection. A comprehensive consideration of the frequency doubler design process and the comparison of the g_m-boosting topology will be presented. The measurement results indicate a conversion loss of -4.5 dB at 134 GHz with a 5-dBm input drive, achieving a fundamental rejection greater than 34dbc. This work has been published in 2023 IEEE European Microwave Integrated Circuits Conference (EUMIC).

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1.3.2 K_a-band LNA in CMOS Process

A low-power consumption wideband CMOS LNA, specifically designed for next-generation FPA radio astronomical receivers will be introduced. With consideration for the limited power dissipation constraint (PDC) of the low-power device, we employ a biasing technique to optimize both gain performance and noise figure within this restricted power budget. This approach enables us to achieve optimal performance in terms of gain and noise figure while meeting the limited power dissipation requirements.

In the first stage, we utilize a current-sharing double-transformer-coupler (DTC) to conserve DC power consumption and enhance gain. Subsequently, we employ a new type of DTC technique in the second stage to neutralize the gate-drain and drain-source capacitance. Furthermore, this new DTC technique provides a g_m-boosting effect, enhancing the overall gain. As a result, the proposed Ka-band LNA achieves a small-signal gain of 19.7 dB and a noise figure of 3.4 dB at 29.8 GHz, all while operating with only 7.1 mW of power dissipation. This performance demonstrates the capability of the adopted design topology. Additionally, the LNA achieves a 3 dB bandwidth of 18.3 GHz, spanning from 21.9 to 40.2 GHz. When compared to all published Ka-band CMOS LNAs, the proposed design stands out with its exceptional small-signal performances and low noise figure under low DC power consumption. These results underscore the potential of CMOS LNAs for next-generation FPA radio astronomical applications.

1.3.3 W-Band Bidirectional PA-LNA in CMOS Process

A W-band transformer-based bidirectional PA-LNA using 65-nm CMOS process is presented. To the best of the author's knowledge, this is the first W-band bidirectional PA-LNA to achieves a 3-dB bandwidth of over 20 GHz. In this work, the studies are focused

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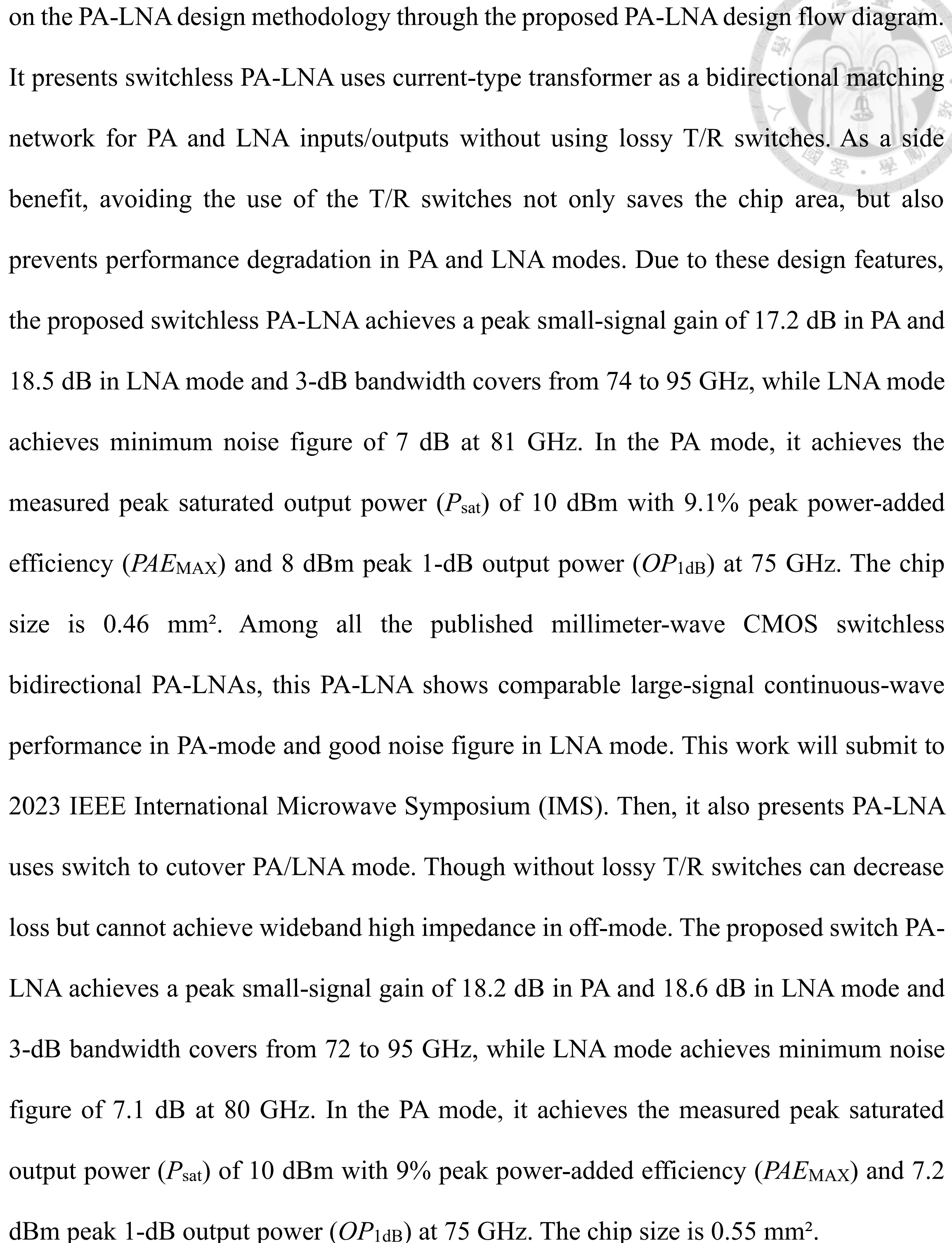

on the PA-LNA design methodology through the proposed PA-LNA design flow diagram. It presents switchless PA-LNA uses current-type transformer as a bidirectional matching network for PA and LNA inputs/outputs without using lossy T/R switches. As a side benefit, avoiding the use of the T/R switches not only saves the chip area, but also prevents performance degradation in PA and LNA modes. Due to these design features, the proposed switchless PA-LNA achieves a peak small-signal gain of 17.2 dB in PA and 18.5 dB in LNA mode and 3-dB bandwidth covers from 74 to 95 GHz, while LNA mode achieves minimum noise figure of 7 dB at 81 GHz. In the PA mode, it achieves the measured peak saturated output power (P_{sat}) of 10 dBm with 9.1% peak power-added efficiency (PAE_{MAX}) and 8 dBm peak 1-dB output power (OP_{1dB}) at 75 GHz. The chip size is 0.46 mm^2. Among all the published millimeter-wave CMOS switchless bidirectional PA-LNAs, this PA-LNA shows comparable large-signal continuous-wave performance in PA-mode and good noise figure in LNA mode. This work will submit to 2023 IEEE International Microwave Symposium (IMS). Then, it also presents PA-LNA uses switch to cutover PA/LNA mode. Though without lossy T/R switches can decrease loss but cannot achieve wideband high impedance in off-mode. The proposed switch PA-LNA achieves a peak small-signal gain of 18.2 dB in PA and 18.6 dB in LNA mode and 3-dB bandwidth covers from 72 to 95 GHz, while LNA mode achieves minimum noise figure of 7.1 dB at 80 GHz. In the PA mode, it achieves the measured peak saturated output power (P_{sat}) of 10 dBm with 9% peak power-added efficiency (PAE_{MAX}) and 7.2 dBm peak 1-dB output power (OP_{1dB}) at 75 GHz. The chip size is 0.55 mm^2.

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1.4 Thesis Organization

The organization of this thesis is shown as follows.

In chapter 2, a high conversion gain D-band multiplier in 28-nm CMOS process is designed and measured. The design procedures including device size selection, g_m-boosting technique, Marchand balun technique and passive lumped LC tank are demonstrating. The simulated, measured results, and comparison table are shown. And a short conclusion is presented at the end of this chapter.

In chapter 3, a compact 22-41 GHz low power LNA with improved small signal gain is proposed by new type DTC technique is designed and measured. The design procedures including size selection, current sharing structure and overall simulation are described. The simulated, measured results, and comparison table are shown. And a short conclusion is presented at the end of this chapter.

Chapter 4 introduces the design of two versions of PA-LNAs: one featuring a switch, and the other without a switch. In the version without a switch, we carefully design the transformer and transistor sizes to ensure that the off-mode impedance remains sufficiently open. In contrast, the version with a switch utilizes the switch to toggle between the Tx and Rx modes. Throughout this chapter, we provide a comprehensive comparison of the advantages and disadvantages of these two versions and offer a detailed description of the design flow. The chapter includes simulated and measured results, as well as a comparison table. A brief conclusion summarizes the key findings presented in this chapter.

Finally, a conclusion of this thesis is given in Chapter 5.

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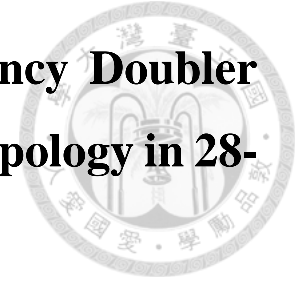

Chapter 2 Design of a D-Band Frequency Doubler with g_m-Boosting Cascode Topology in 28-nm CMOS

D-Band frequency multipliers play a significant role in modern wireless communication systems. The D-Band typically refers to the frequency range between 110 GHz and 170 GHz and finds wide applications in satellite communications, radar systems, and wireless communication. A frequency multiplier increases the frequency of the input signal to its multiples. In the D-Band, frequency multipliers have unique design and operation characteristics. Typically, non-linear devices such as diodes and are employed to generate the multiplied frequency components of the input signal. Through proper design and adjustment, frequency multipliers effectively raise the signal frequency to enable efficient communication in the D-Band, so this chapter will publish a 2-stage low input power doubler using g_m-boosting in 28-nm CMOS technology, with a frequency range of 126-144 GHz. Its maximum conversion gain is -5 dB, and power consumption is relatively low, it consumes 15-mW dc power under only 5-dBm input drive.

2.1 Design Procedure of the D-Band Doubler

2.1.1 Device Size and Bias Selection

The input power, conversion gain, and drain efficiency (P_{OUT}/P_{DC}) of the FET doublers necessitate careful consideration when selecting the bias condition. The simulation setup is shown in Fig. 2.1. The conversion gain, output power, and drain efficiency of the FET doubler under various bias conditions are shown in Fig. 2.2. However, g_{m2} is also a crucial parameter for the frequency doubler to generate a second-harmonic signal, it shows the highest g_{m2} at 0.4-V gate voltage in Fig. 2.3

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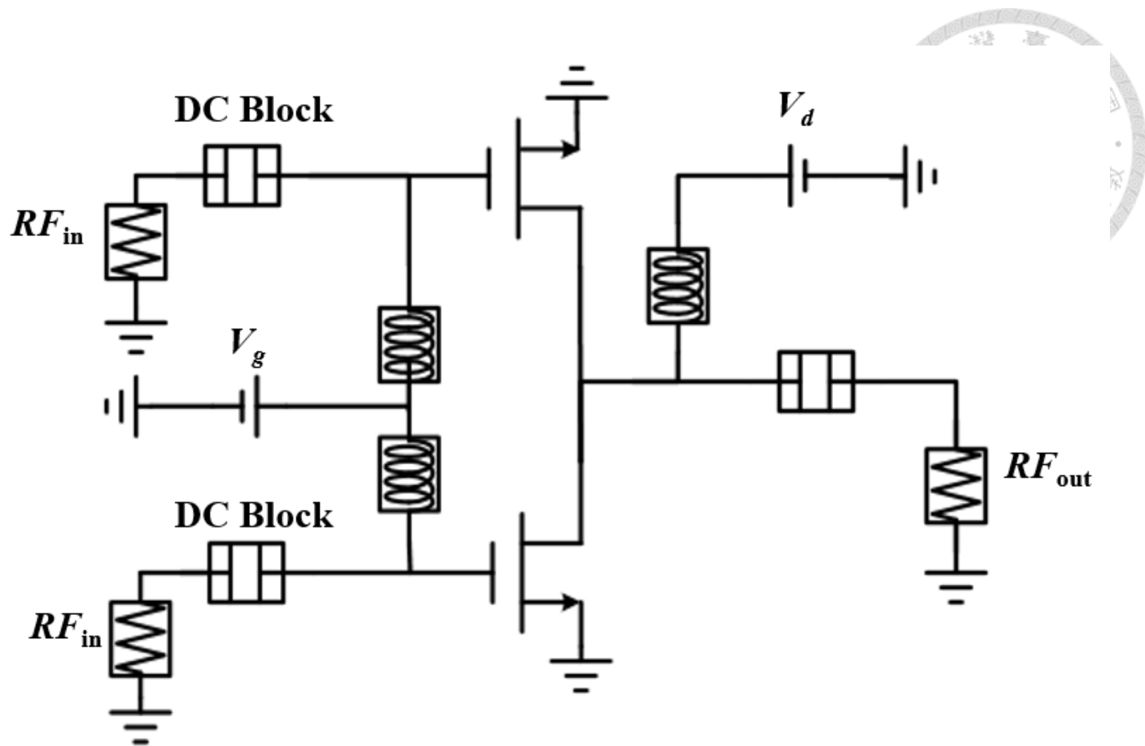

Fig. 2.1. Circuit schematic for the selection of bias condition and device size.

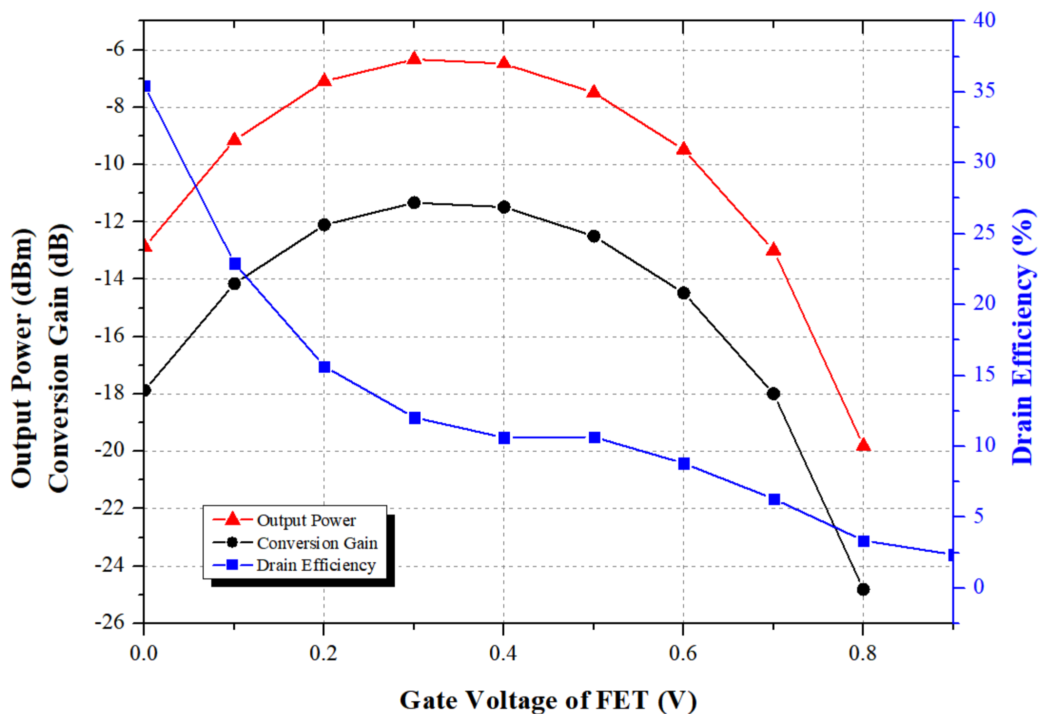

Fig. 2.2. Conversion gain, output power, and drain efficiency with different bias conditions at output frequency of 140 GHz (28-μm width).

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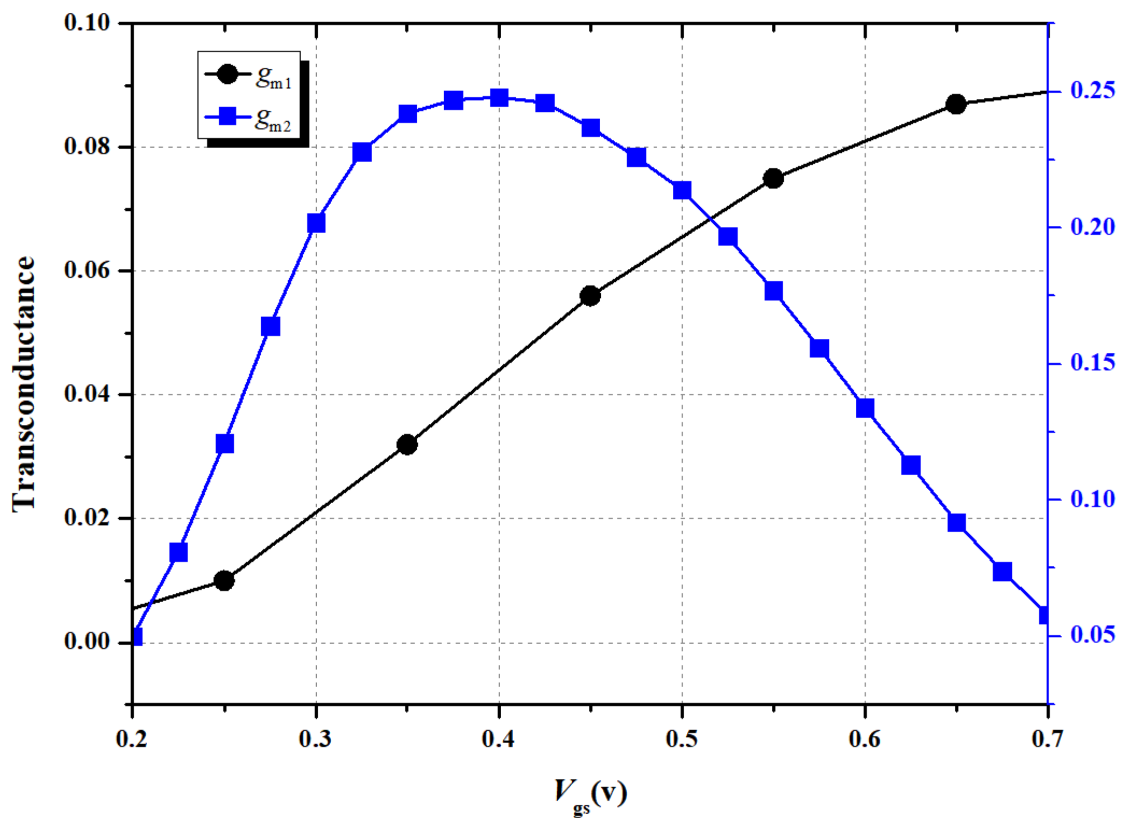

Fig. 2.3. The simulated results of transconductance.

The selection of device size in this doubler circuit considers several factors such as output power, conversion gain, and matching network. A larger-size transistor can produce higher output power, but it also consumes more DC power and experiences degraded conversion gain at higher frequencies due to the parasitic capacitance of C_{gd}. Fig. 2.4 and Fig. 2.5 illustrate the conversion gain and output power of the FETs. The investigation involves three nMOSFETs with total widths of 14-μm, 28-μm, and 56-μm. It is observed that a larger-size device exhibits higher output power but lower peak conversion gain, necessitating a higher input power. Conversely, the small and medium FETs (14 μm and 28 μm) show similar conversion gains, while the large and medium FETs (28 μm and 56 μm) provide similar saturated output power. Hence, a size of 48 μm is found to be suitable as it balances both conversion gain and output power Fig. 2.6 and

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Fig. 2.7 depict the input impedance and optimal load impedance with different sizes. For smaller FETs, the input impedance is close to the open circuit point in the Smith chart. On the other hand, the optimal output impedance is relatively low for larger FETs. Based on these impedance characteristics, the FET with a total width of 28 um is selected for the doubler design.

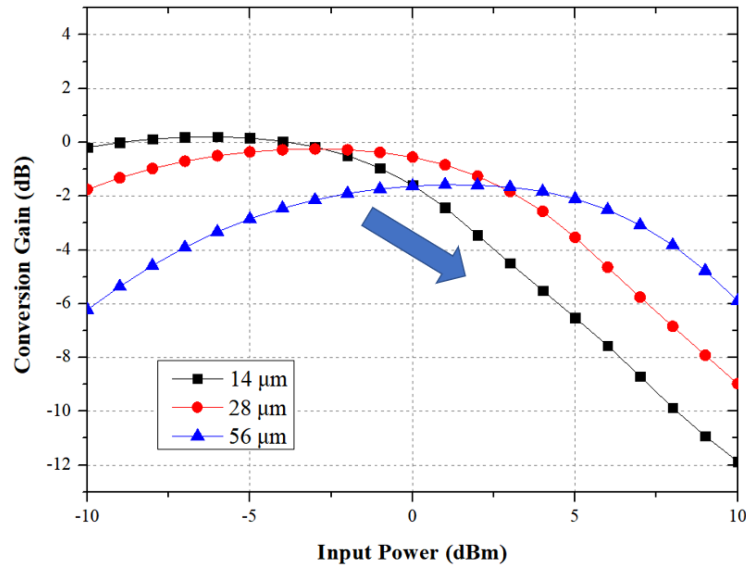

Fig. 2.4. Conversion gain with different sizes versus input power at input frequency of 70 GHz ($V_g = 0.4$ V)

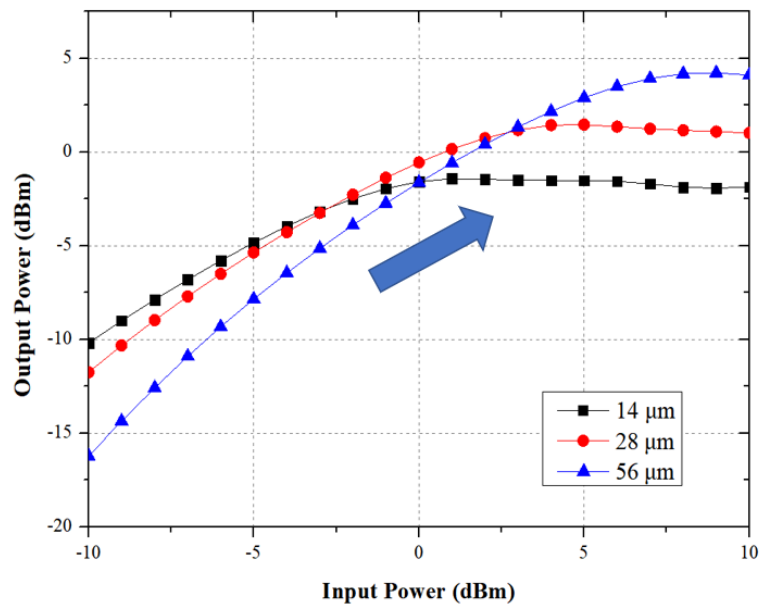

Fig. 2.5. Output Power with different sizes versus input power at input frequency of 70 GHz ($V_g = 0.4$ V)

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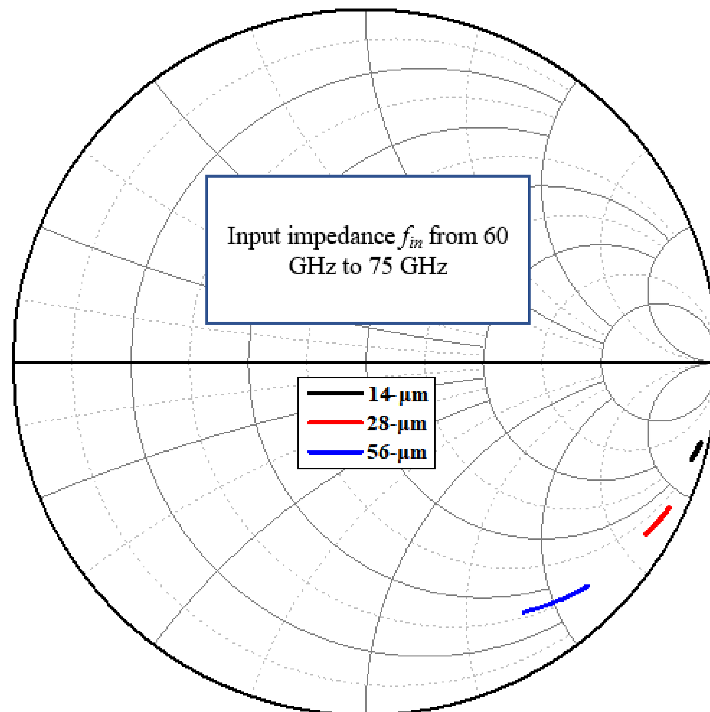

Fig. 2.6. Input impedance with different sizes at frequency of 60-75 GHz (V_g = 0.4 V).

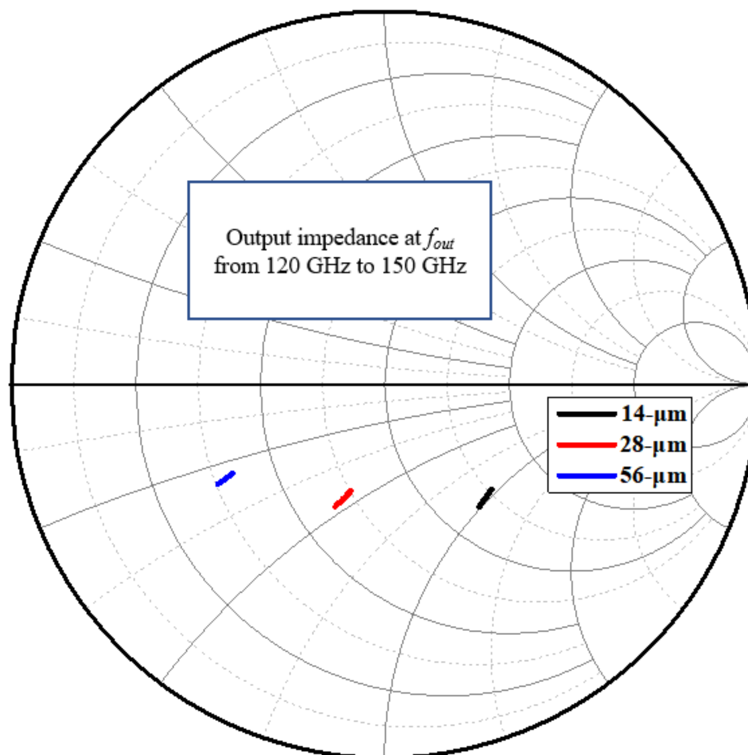

Fig. 2.7. Output impedance with different sizes at frequency of 60-75 GHz (V_g = 0.4 V).

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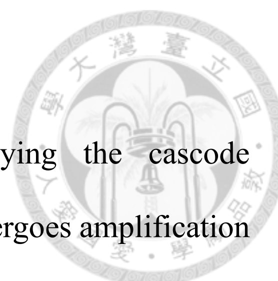
2.1.2 Cascode Configuration Design



For achieving higher output power performance, employing the cascode configuration is a favorable approach. This is because the signal undergoes amplification through the common-gate [58]. However, the selection of transistor size for the common-gate necessitates careful consideration of both the signal output power from the common-source. The output power from the common-source is around -3 dBm; therefore, the IP_{1dB} must exceed 0 dBm. Fig. 2.8 shows the simulated large-signal results of the common-gate configuration with a total transistor width of 52-µm at 140 GHz. The results indicate that the IP_{1dB} is greater than -3 dBm. Therefore, total transistor width of 52-µm is enough. When the fixed total gate width is 52-um, various combinations of devices can be selected. The utilization of multi-way combining techniques and multi-finger devices is commonly employed to mitigate parasitic resistance originating from the gate terminal, while maintaining uniform device sizes. In Table 2.1 a comparison is presented of load-pull simulations for a CG operating at 140 GHz.

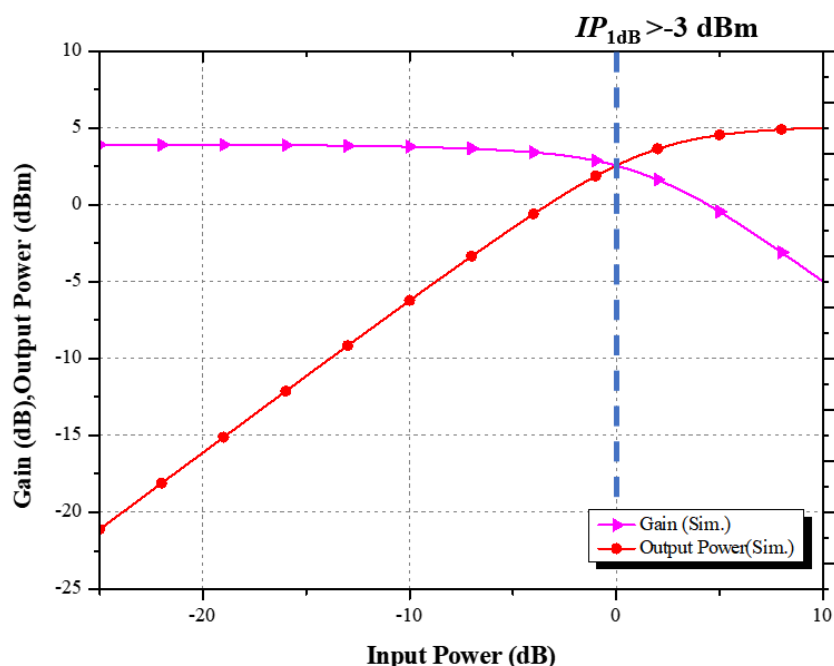


Fig. 2.8. The simulated large-signal results of the common-gate with transistor total width of 52-µm at 140 GHz.

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Table 2.1. Load-pull simulation result comparison with the same device size

V_g(V)	Size W(μm)*Finger* Combine	Z_{opt} (Ω)	Z_s (Ω)	Gain (dB)	P_{out} (dBm)	PAE (%)
0.65	0.8*32*2	8.1+j*43	45.34+j38	3.3	1	8
0.65	1.6*16*2	10.1+j*34	40+j*31	2.8	-0.8	5
0.65	1.6*8*4	8.7+j*45	40+j*34	3.5	-1	4.3

Table 2.1 summarizes the load-pull results, indicating that the configuration with a size of 0.8 μm x 32 fingers and the combination of two transistors exhibits the highest output power, PAE, and favorable gain. Therefore, selecting the transistor size of 0.8 μm x 32 fingers and the combination of two transistors proves to be optimal in this work.

2.1.3 g_m-Boosting Technique

In amplifier circuits, the conventional approach involves using a cascode stage that incorporates a common-gate MOSFET in the signal path[39]. By grounding the gate terminal, as depicted in Fig. 2.9(a), the Miller effect is effectively eliminated, resulting in improved reverse isolation and circuit stability. This cascode configuration also enhances the amplifier gain at multi-gigahertz frequencies by boosting the output resistance. However, when amplifier circuits operate at millimeter-wave frequencies, the gain of the cascode stage experiences a significant decrease due to limitations stemming from carrier mobility and device parasitic effects. To address this gain roll-off at higher frequency bands, a compensating technique can be employed. For instance, an inductor L_g can be added to the common-gate stage, as illustrated in Fig. 2.9(b).

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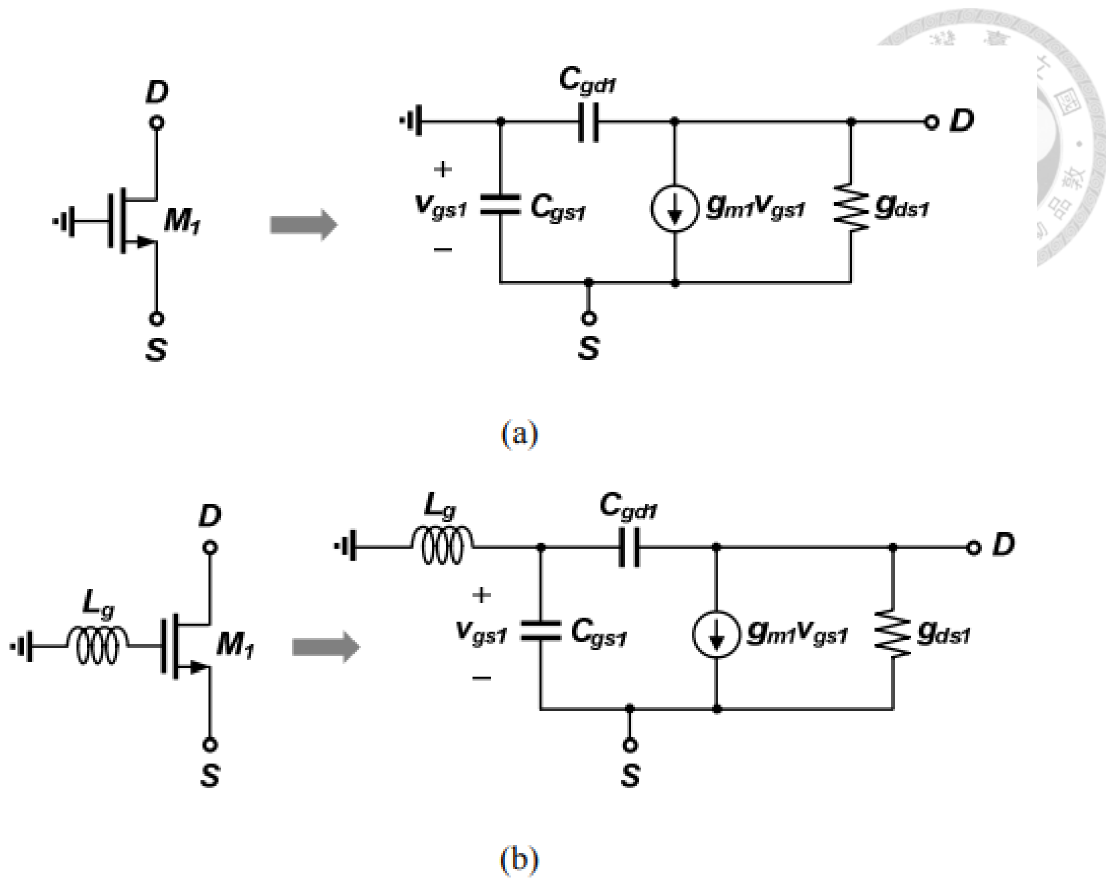

Fig. 2.9. The common-gate transistor (a) without and (b) with the gate inductor.

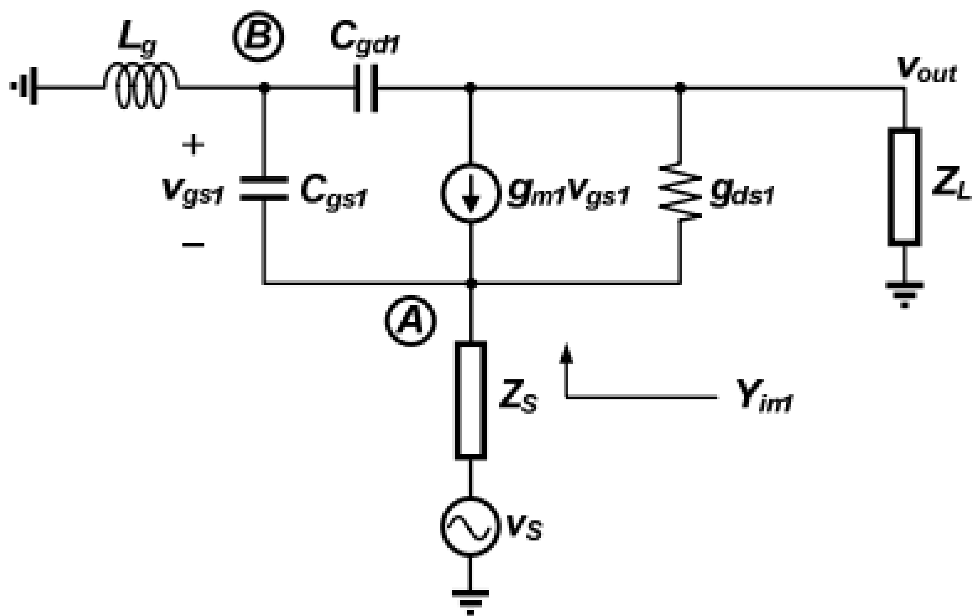

Fig. 2.10. The small-signal equivalent circuit of the common-gate transistor with the gate inductor.

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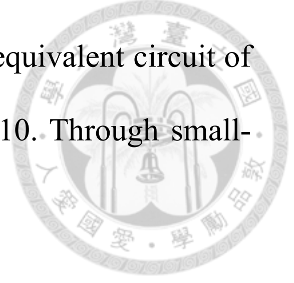

To delve deeper into the proposed gain-boosting technique, an equivalent circuit of the common-gate stage shown in Fig. 2.9(b) is provided in Fig. 2.10. Through small-signal analysis, the voltages at points A and B can be expressed as

$$v_A = \frac{1-(\omega_0/\omega_t)^2}{[1-(\omega_0/\omega_t)^2]+(g_{m1}+j\omega C_{gs1})Z_S} v_S \tag{2.1}$$

$$v_B = \frac{-(\omega_0/\omega_t)^2}{1-(\omega_0/\omega_t)^2} v_A \tag{2.2}$$

where ω_0 is the operating frequency and ω_t is given by

$$\omega_t = \frac{1}{\sqrt{L_g C_{gs1}}}. \tag{2.3}$$

It is observed that the gate-to-drain capacitance (C_{gd1}) have relatively small values. As a result, we can simplify the analysis by neglecting these factors. By considering equation (2.1) and (2.2), we can express the voltage difference across the gate-to-source capacitance as follows:

$$v_{gs1} = \frac{-1}{[1-(\omega_0/\omega_t)^2]+(g_{m1}+j\omega C_{gs1})Z_S} v_S \tag{2.4}$$

Based on equation (2.2), when the angular frequency (ω_0) is smaller than the threshold frequency (ω_t), the voltages v_A and v_B are out of phase. As a result, the amplitude of v_{gs1} increases, which in turn enhances the effective transconductance and boosts the gain of the cascode stage. Observations have indicated that the presence of gate inductance in the common-gate transistor can lead to an increase in device instability [40]. As a result, circuit stability becomes a critical concern and necessitates careful

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examination. However, in frequency multipliers, stability is often better than in amplifiers due to the lower gain of frequency doubler. Therefore, the g_m-boosting technique in frequency multipliers is suitable for implementation. In this work added a gate inductance to the second stage CG transistor for g_m-boosting, as shown in Fig. 2.11. To investigate the impact of TL7 (gate transmission line) on the output power, it conducted simulations with different TL7 lengths and compared the results, as depicted in Fig. 2.12. Notably, the output power increases with an increase in TL7 length. As the length of the gate transmission line increases, the gate inductance also rises, resulting in improved g_m and output power. However, it is crucial to consider that as the TL7 length increases, the stability factor decreases, and bandwidth becomes narrow. Therefore, the selection of an optimal gate transmission line length is crucial for achieving a trade-off among output power, bandwidth, and circuit stability. While a 40-μm (30pH) length offers the highest conversion gain, it results in a significantly narrowed bandwidth. For comprehensive consideration between gain and bandwidth, a 20-μm transmission line length is appropriate to enhance output power by 2 dB and achieve broad wideband performance.

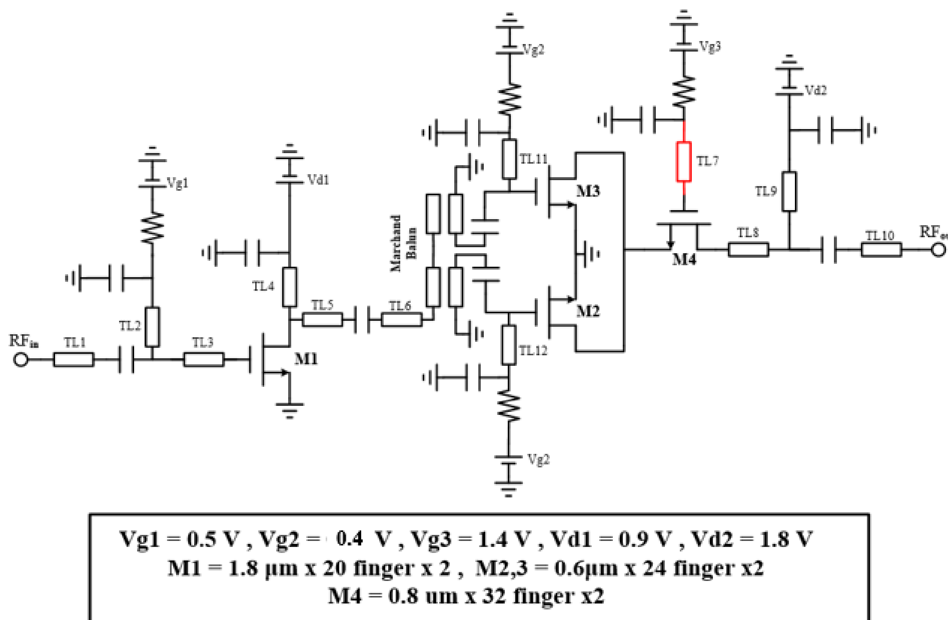

Fig. 2.11. Schematic of the proposed D-Band frequency doubler

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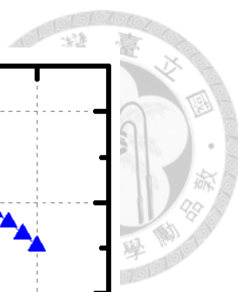
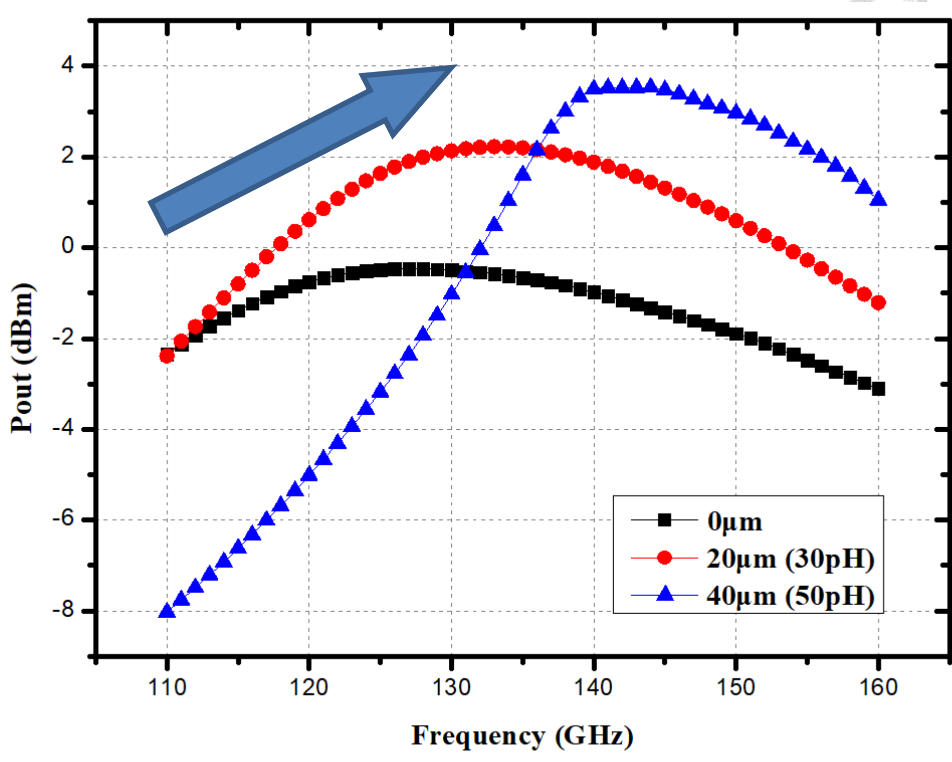
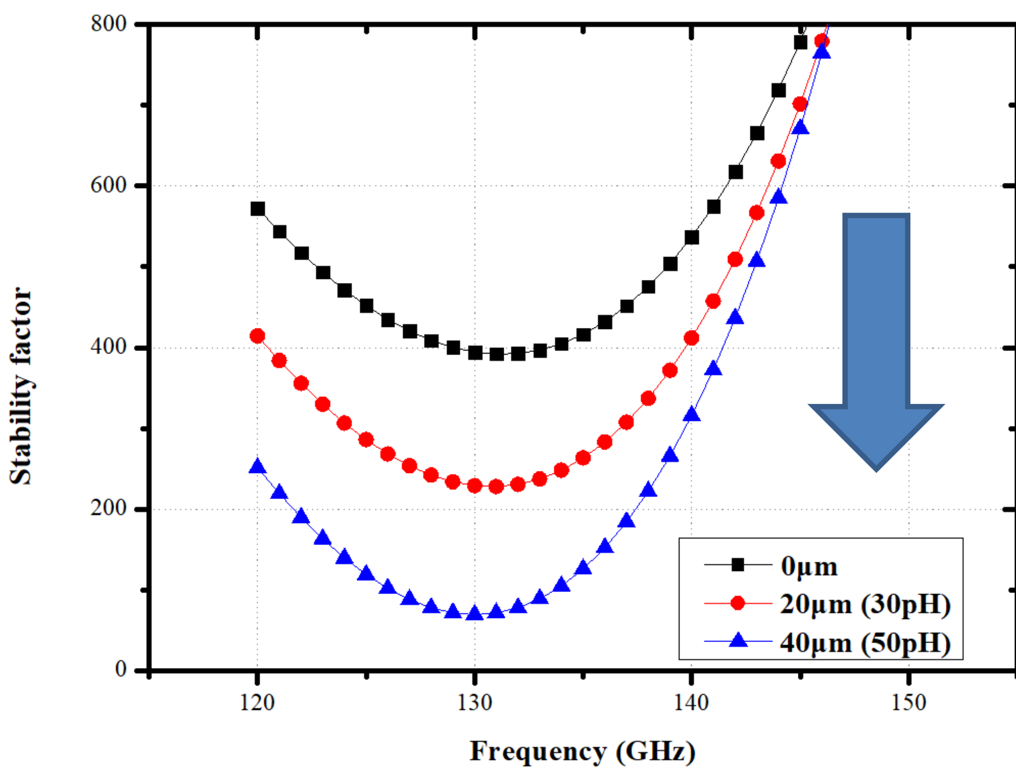




(a)



(b)

Fig. 2.12. The output power and stable factor with different g_m-boosting transmission line lengths (a) output power; (b) stability factor.

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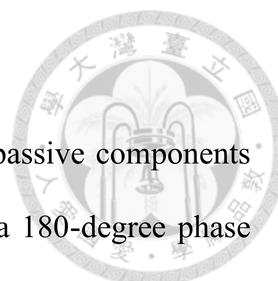
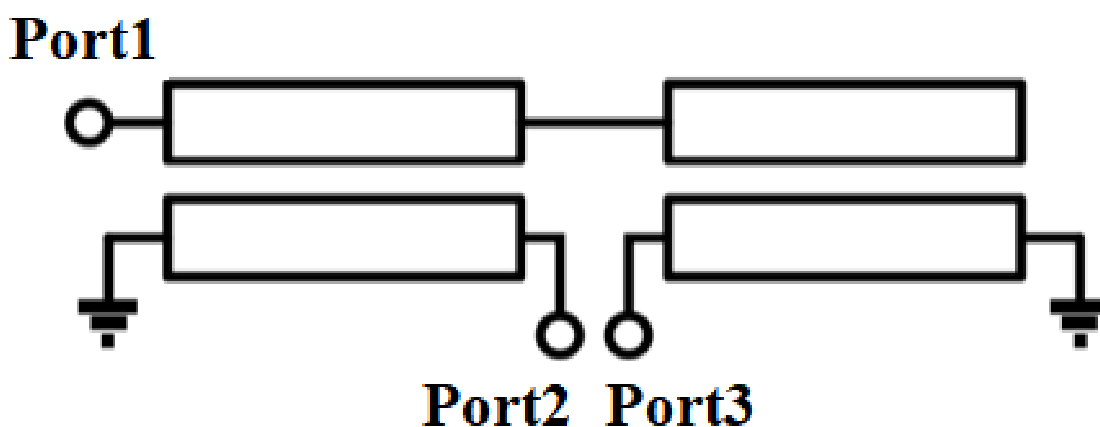
2.1.4 Marchand Balun Design



To realize the doubler, we employ a technique of introducing passive components between the drive-stage and the second stage, effectively creating a 180-degree phase difference. While a transformer coupler can provide a differential signal, achieving a high impedance transformation ratio at high frequencies can be quite challenging. At these elevated frequencies, the operating frequency often surpasses the self-resonance frequency, leading to a low-quality factor. Given the aforementioned considerations, employing a Marchand balun to generate a differential signal emerges as an effective solution, especially suited for the D-Band frequency range. The 3D structure and schematic of the Marchand balun used in this design are displayed in Fig. 2.13. The simulation results indicate that the phase imbalance between port 2 and port 3 is approximately 180 ± 2°, as shown in Fig. 2.14. Additionally, the amplitude imbalance is around 0.2 dB. It shows that the insertion loss of Marchand balun is 3 dB in Fig. 2.15. Based on these promising simulation results, it can assert that the Marchand balun is well-suited for the proposed D-band doubler. Its ability to provide the required 180-degree phase difference and maintain a desirable amplitude balance makes it a reliable component in achieving the desired frequency doubling functionality.



(a)

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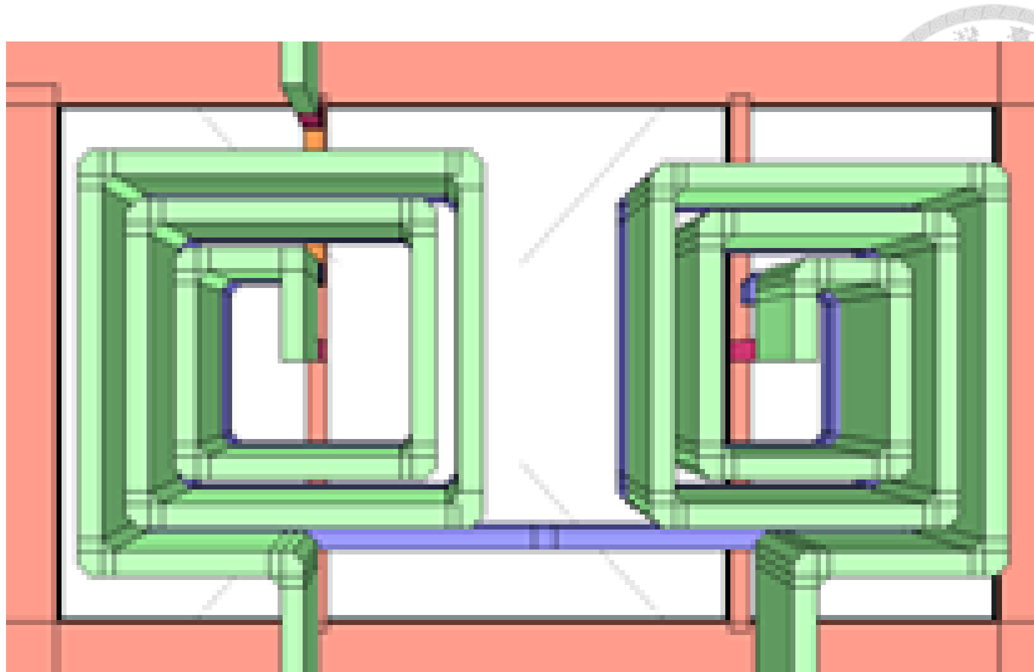

(b)

Fig. 2.13. Marchand balun 3D-structure and schematic (a) Schematic (b) Top view of the Marchand balun.

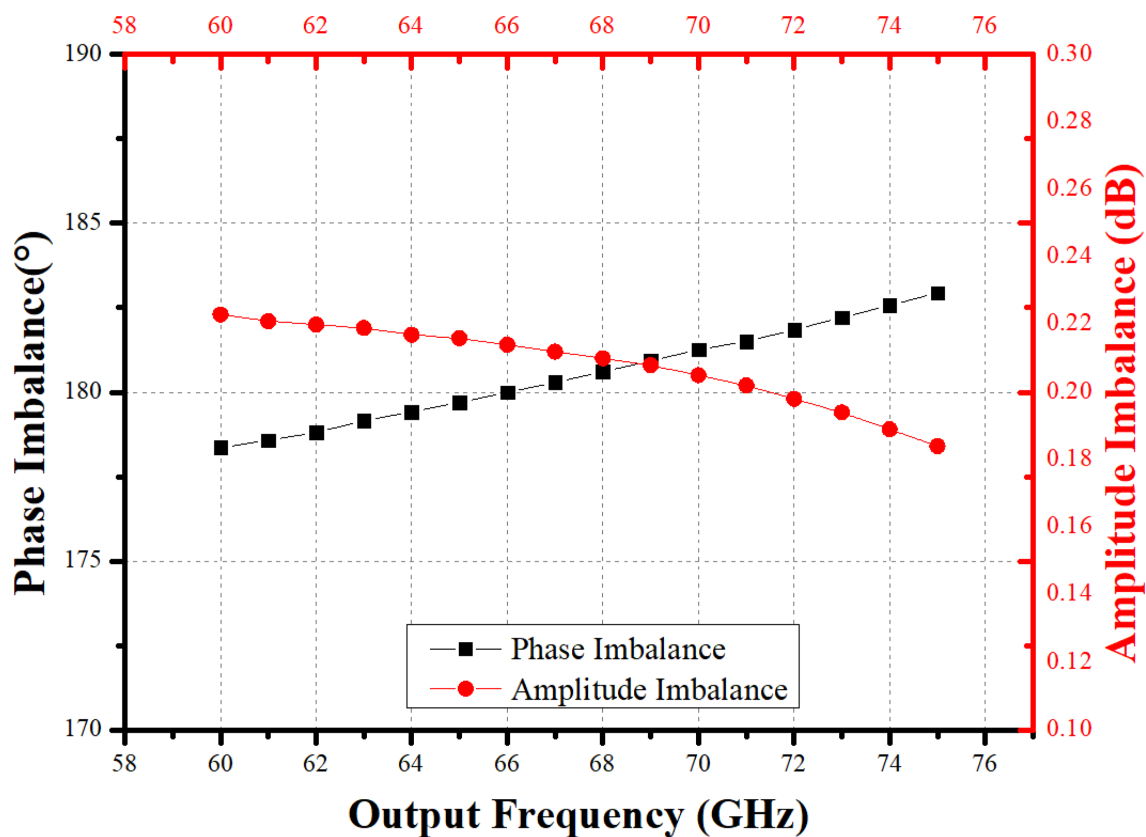

Fig. 2.14. The performance of the 60-75 Marchand balun

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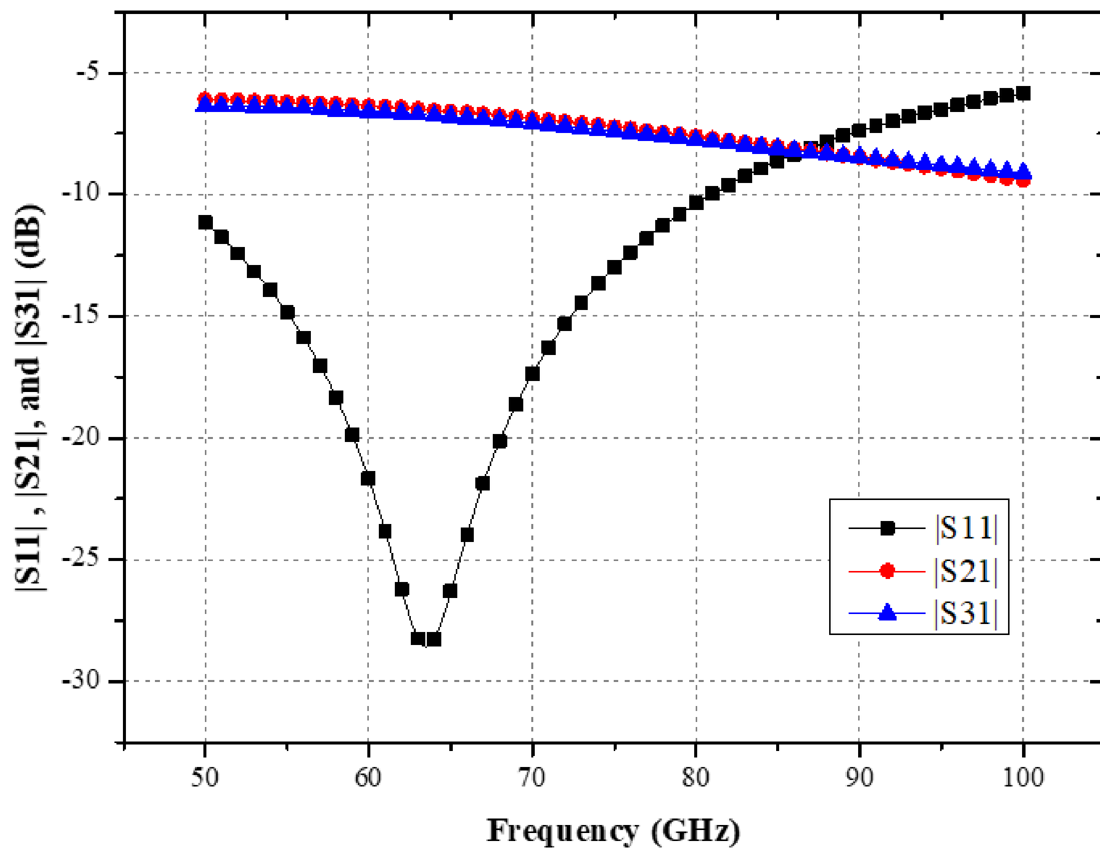

Fig. 2.15. |S11|, |S21|, and |S31| of the Marchand balun

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2.1.5 Overall Circuit Schematic

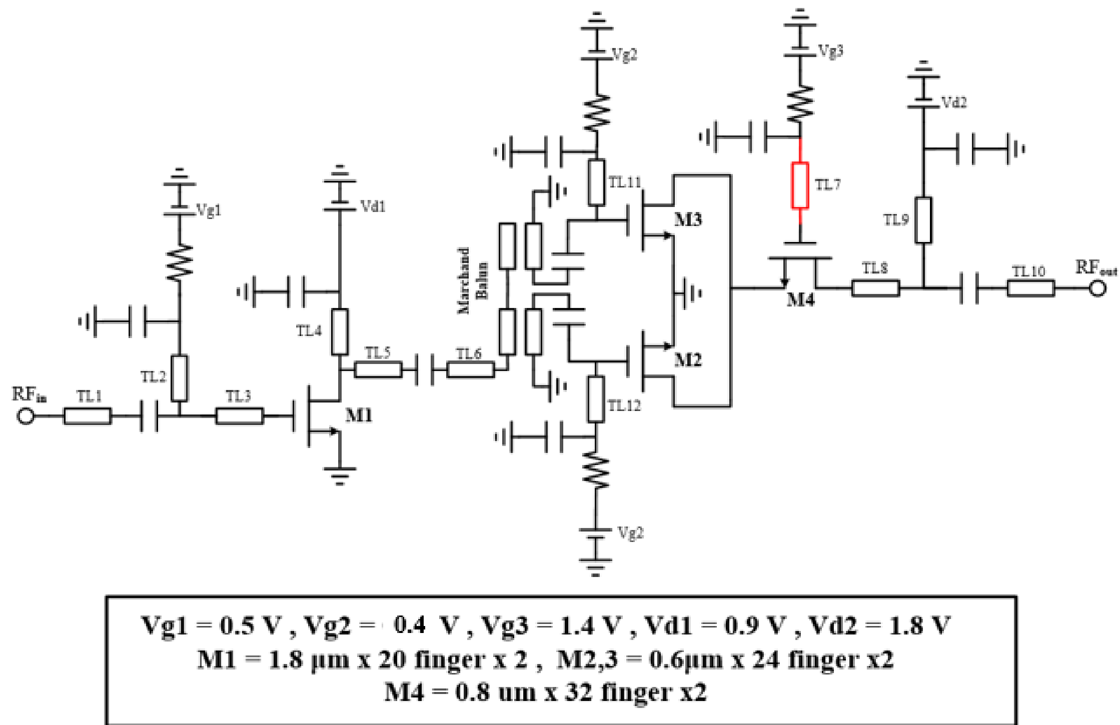

Fig. 2.16. Overall circuit architecture of the frequency doubler.

The circuit is designed by 28-nm CMOS general purpose one-poly nine metal (1P9M) RF process provided by Taiwan Semiconductor Manufacturing Company (TSMC). In this work, balanced cascode architecture and one stage driver is chosen to realize a high conversion gain, low-power consumption frequency doubler, and low input power. The schematic of the proposed D-band frequency doubler is shown in Fig. 2.16. This doubler is composed of 2 stages. The first stage is the drive stage to reduce required input power using CS structure, and it operate in Class-A for high linearity and output power delivered to the next stage. The second stage is designed using cascode structure which operates in Class-B in order to generate higher 2nd harmonic signal. The g_m-boosting technique is utilized in the cascode stage to improve conversion gain and output power. Marchand balun is used between the two stages to generate broadband differential signals.

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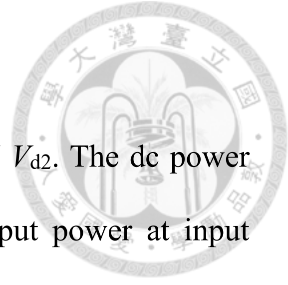
2.2 Simulation Result and Post-layout



The simulation results are obtained under 0.9-V V_{d1} and 1.8-V V_{d2}. The dc power consumption is 15 mW. The simulated conversion gain versus input power at input frequency of 65 GHz is shown in Fig. 2.17 The simulated conversion gain is optimal when input power is 5 dBm Fig. 2.18. shows the simulated conversion gain versus output frequency with input power of 5 dBm. The doubler. The simulated peak conversion gain is -4.5 dB at 130 GHz, and achieves 7.4% efficiency when input power is 5 dBm. As shown in Fig. 2.19, the proposed work demonstrates an output power of 0.5 dBm at 130 GHz. The fundamental rejection is higher than 34 dB at all simulated frequencies in D-band, as shown in Fig. 2.20. Fig. 2.21 show the frequency doubler chip layout.

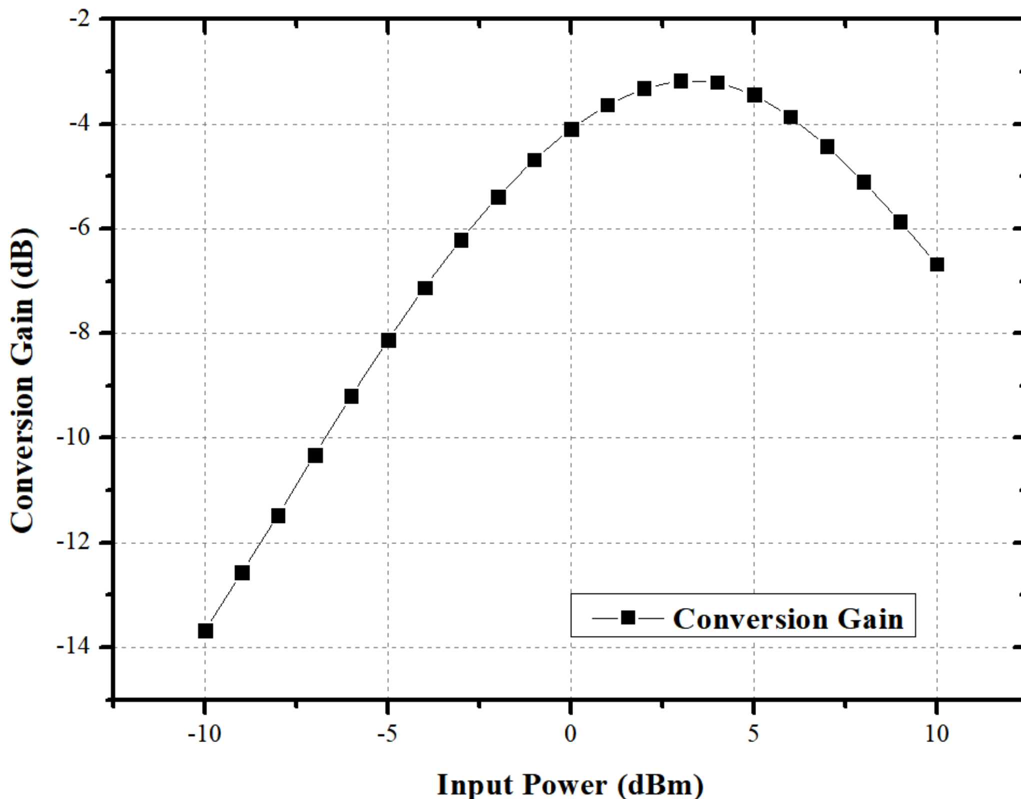


Fig. 2.17. Simulated conversion gain versus input power at input frequency of 65 GHz.

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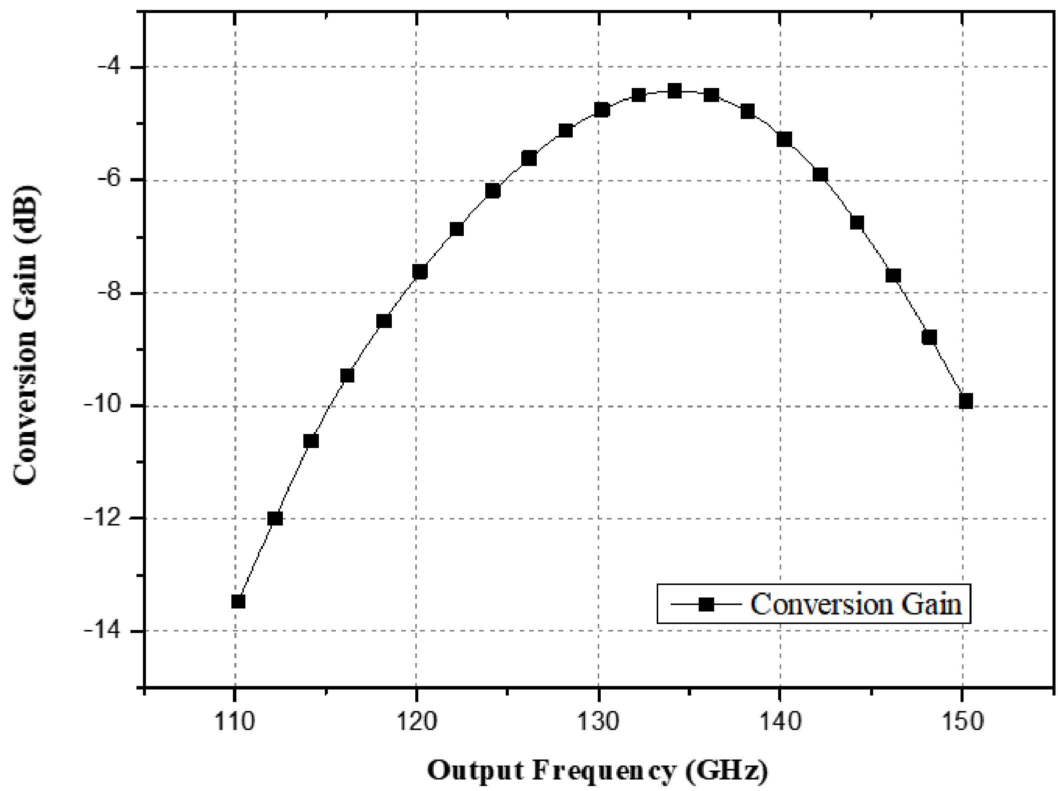

Fig. 2.18. Simulated conversion gain versus input frequency with input power of 5 dBm.

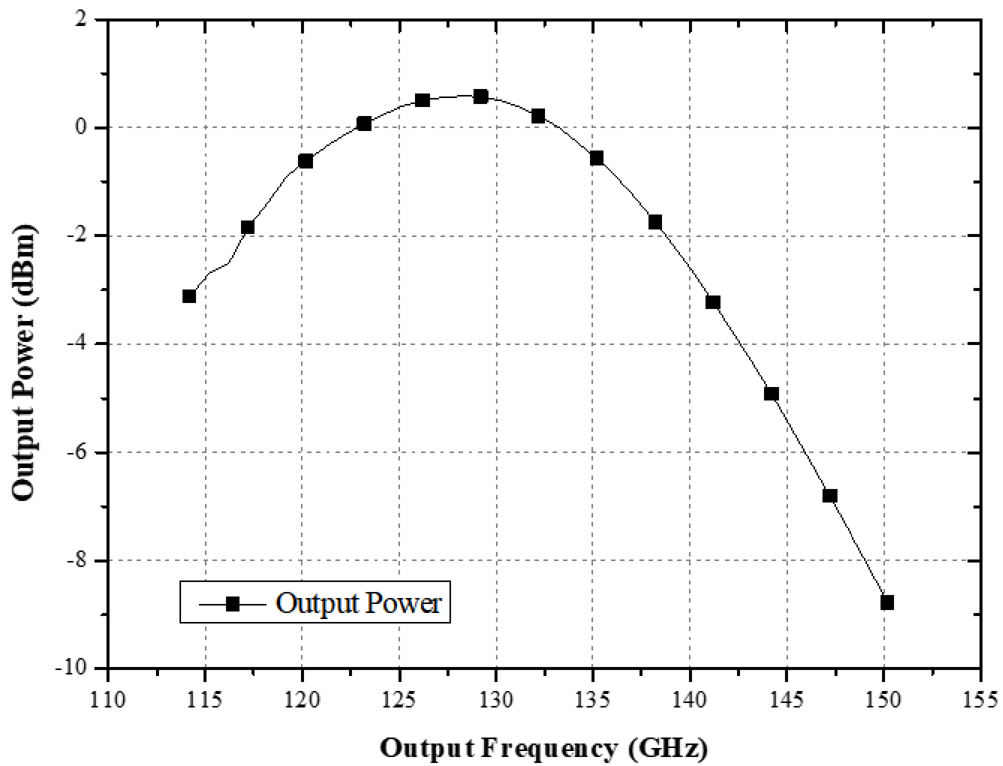

Fig. 2.19. Simulated Output Power versus input frequency with input power of 5

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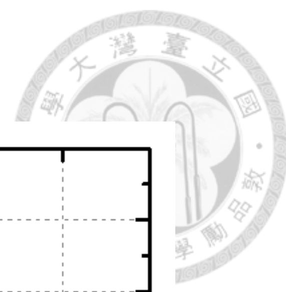
dBm.



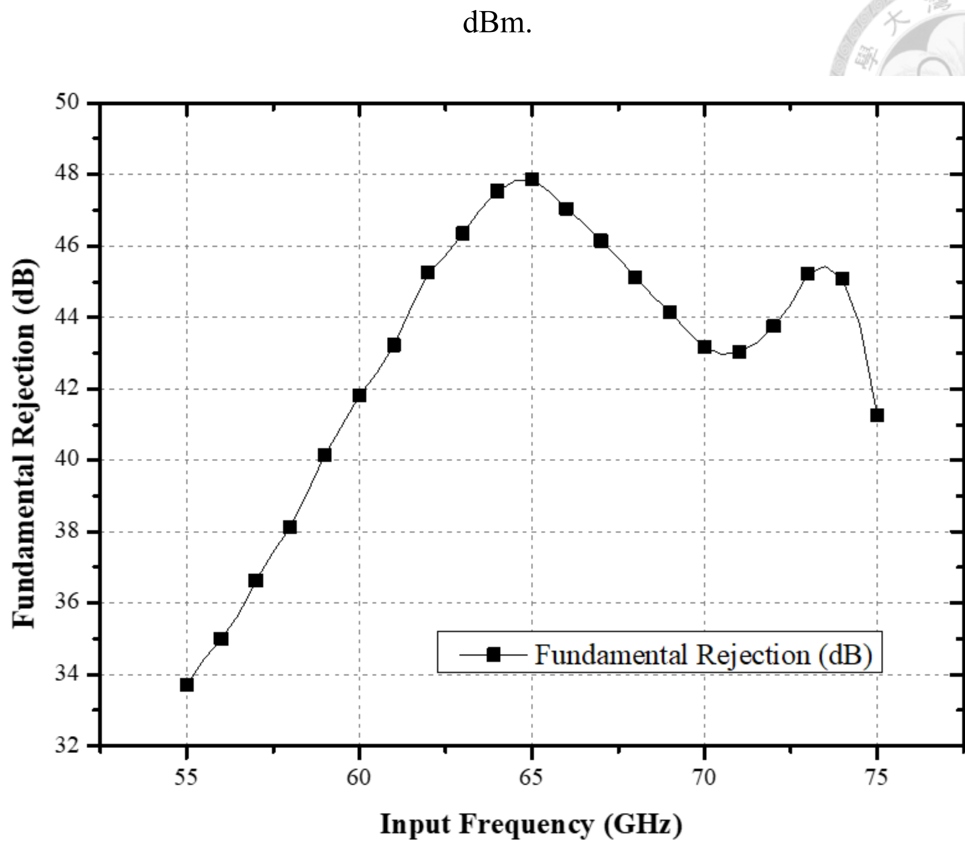


Fig. 2.20 Simulated fundamental rejection versus input frequency with input power of 5 dBm.

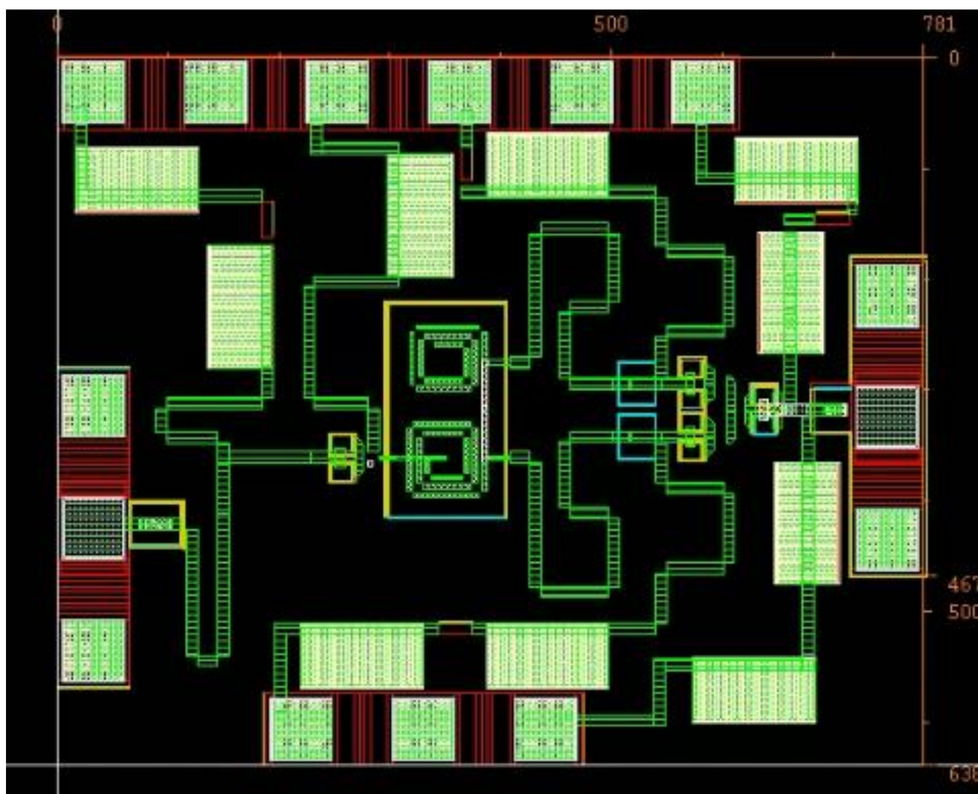


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Fig. 2.21 Layout of the D-band frequency doubler with chip size 0.63 × 0.78 mm^2

2.3 Measurement Result

The D-Band frequency doubler has been produced using a 28-nm CMOS process. The total chip area, inclusive of all pads, amounts to 0.49 mm^2. The chip photo can be seen in Figure 2.18. For testing purposes, the doubler is subjected to on-wafer probing. The measurements are carried out with V_{d1} set at 0.9 V and V_{d2} at 1.8 V. The direct current power consumption registers at 15 mW. The testing protocol utilizes Agilent E8257D and Agilent E8267D signal generators, and the output power is gauged with power meters. Further analysis involves down-conversion of the output signal via a mixer, followed by examination using the Agilent E4448A spectrum analyzer. The necessary DC bias is supplied by the Agilent E3631A power supply. As depicted in Fig. 2.23, the findings of this study showcase an output power of 0.5 dBm at 134 GHz. The conversion gain 3-dB bandwidth spans from 126 GHz to 146 GHz. Specifically, the peak conversion gain at 134 GHz is measured at -4.5 dB. Notably, an efficiency of 7.4% is achieved when the input power is set at 5 dBm, as illustrated in Fig. 2.24. Discontinuity between 134-140 GHz was caused by the frequency limitation of the signal generator in our lab. The frequency doubler fundamental rejection surpasses 34 dB across all measured frequencies in the D-band, as shown in Fig. 2.25.

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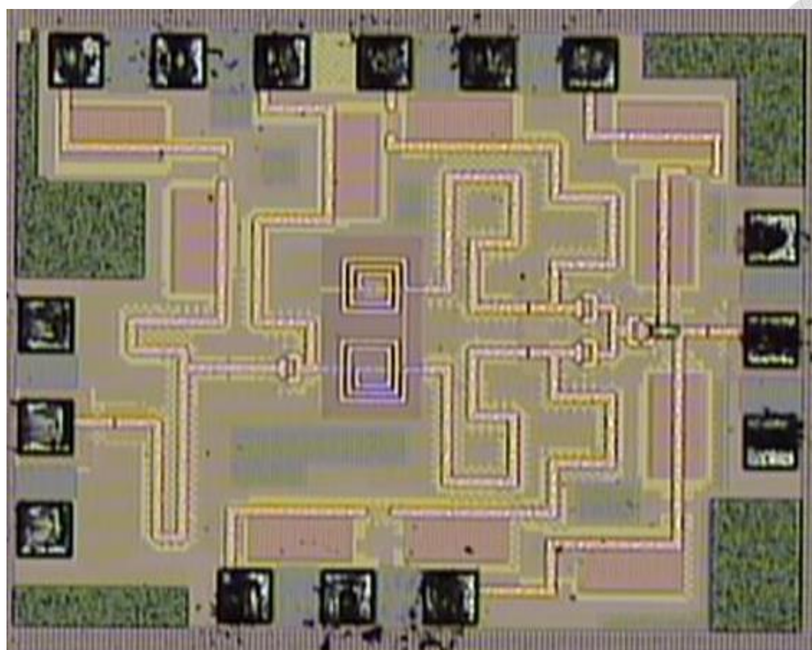

Fig. 2.22. The chip photo of the D-band frequency doubler with chip size 0.63 × 0.78 mm^2

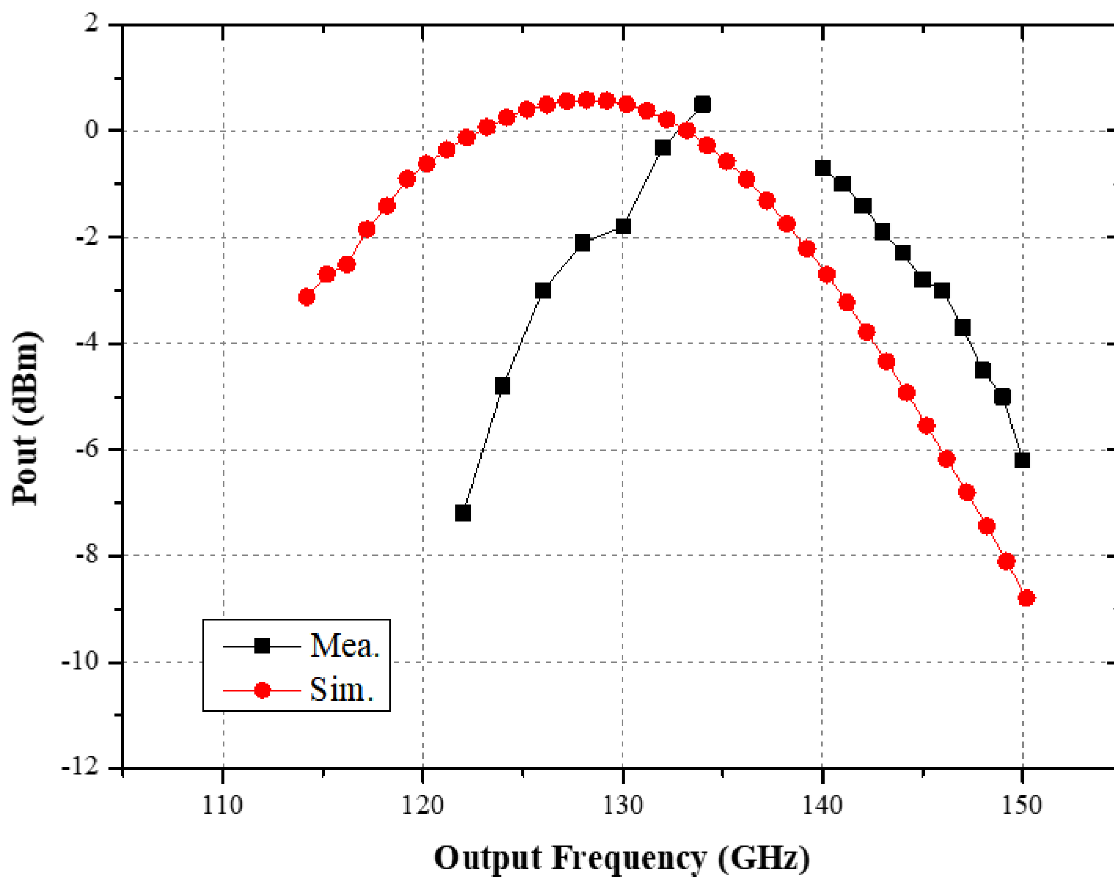

Fig. 2.23. Measured Output Power versus input frequency with input power of 5 dBm.

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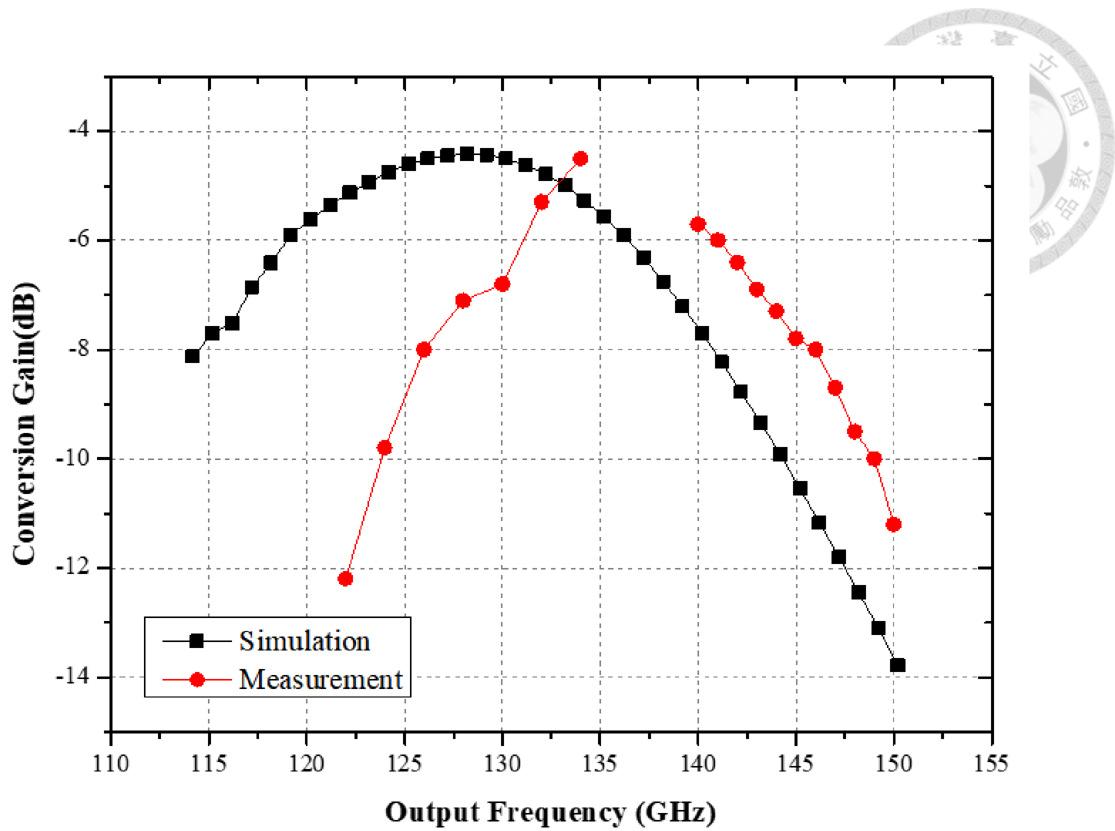

Fig. 2.24. Measured Conversion Gain versus input frequency with input power of 5 dBm.

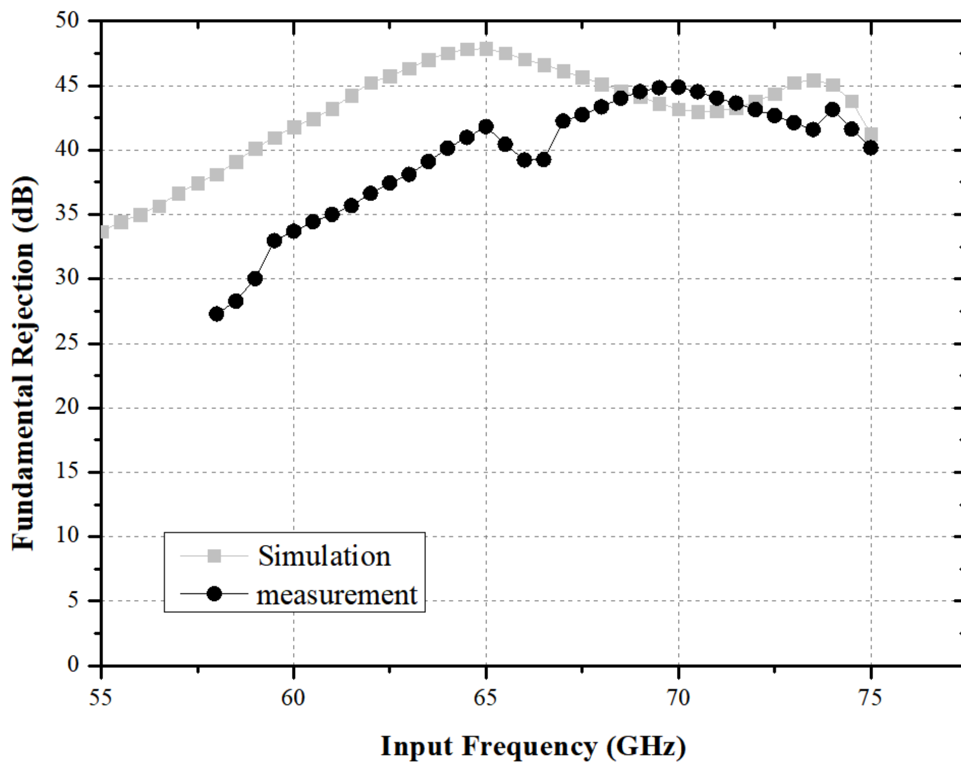

Fig. 2.25. Simulated fundamental rejection versus input frequency.

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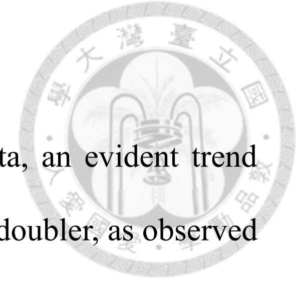

2.4 Trouble Shooting and Discussions

When comparing the measured results with the simulated data, an evident trend emerges: the frequency response of the proposed D-band frequency doubler, as observed in the measured results, exhibits a significant shift of approximately 10 GHz towards higher frequencies. To gain a deeper understanding of this discrepancy, an extensive analysis of the RF and NCH models was conducted. The initial simulation approach involved using HFSS, a well-known electromagnetic simulation software package with a comprehensive 3D modelling environment, in place of Sonnet. Within HFSS, the 3-D architecture of the RF model was constructed, as depicted in Fig. 2.26. An important observation here is the inclusion of additional metal sheets for the lumped ports during the simulation process, a feature conspicuously absent in the real transistor layout. Unfortunately, this introduced an undesirable side effect in the form of extra parasitic capacitance between these added metal sheets. In light of this development, it becomes apparent that addressing the influence of this supplementary parasitic capacitance is necessary. To do so, the NCH+EM model was augmented with small-value capacitors (C_{gs}, C_{gd}, and C_{ds}) [55]. These capacitors were strategically integrated to correct for the impact of the extra parasitic capacitance mentioned earlier. It is worth noting that the capacitance value for each individual lumped port can be computed using the capacitance formula[54].

$$C = \frac{\varepsilon A}{d} \qquad (2,5)$$

where ε represents the dielectric permittivity, which may vary depending on the manufacturing process. A signifies the surface area of the capacitor plates, while d represents the separation distance between these plates. To calculate the overall capacitance, you can simply multiply the capacitance of an individual finger by the total

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number of fingers. The derived capacitance values closely align with those presented in Table 2.2, providing solid support for the validity of the revised model.

Furthermore, it needs to address certain structural details located under the M1 layer, which were not provided in the information. Specifically, the via-holes in the CO layer and the ohmic contacts to the transistor fingers, as depicted in Fig. 2.26(d), introduce additional resistance between the electromagnetic (EM) model and the reference plane of the NCH model. To account for this, a resistor labelled as R_{gco} has been incorporated to represent this resistance. Fig. 2.27 provides an illustration of the transistor trace, where the NCH model, sourced from TSMC, is connected to the simulation outcomes obtained from HFSS software.

Moving on to Fig. 2.28 through Fig. 2.30, a comparative analysis of the S-parameters between the RF and NCH models employing electromagnetic simulations be conducted. The results clearly indicate a noticeable discrepancy. Consequently, in the simulations including additional components such as R_{gco}, C_{gs}, C_{gd}, and C_{ds} to account for the supplementary parasitic effects inherent in the transistor structure.

Fig. 2.31 presents the complete design flow. Table 2.2 lists the values of R_{gco}, C_{gs}, C_{gd}, and C_{ds} for two different transistor sizes that were added in the design. With these modifications, the simulation of conversion gain, output power, and fundamental rejection aligned well with the measurement, as shown in Fig. 2.32 to Fig. 2.33. From Table 2.2, it is observed that the value of R_{gco} is around 40 ohms, consistent with that in the previous report [59].

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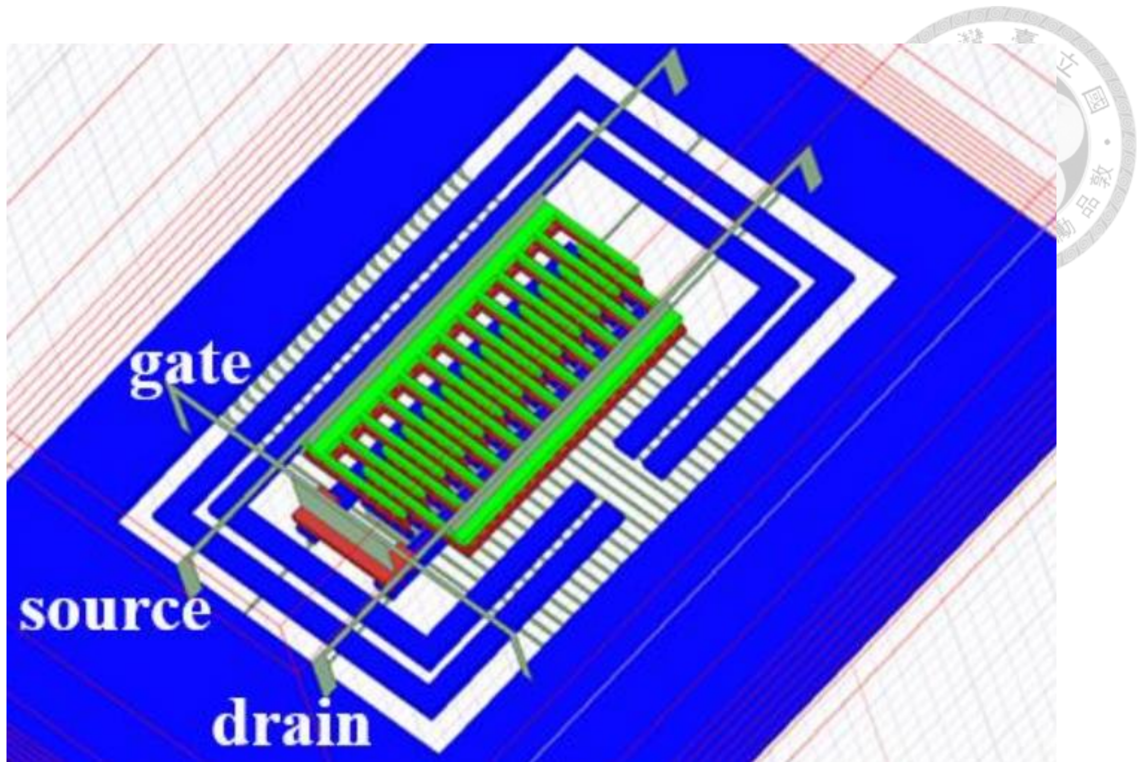
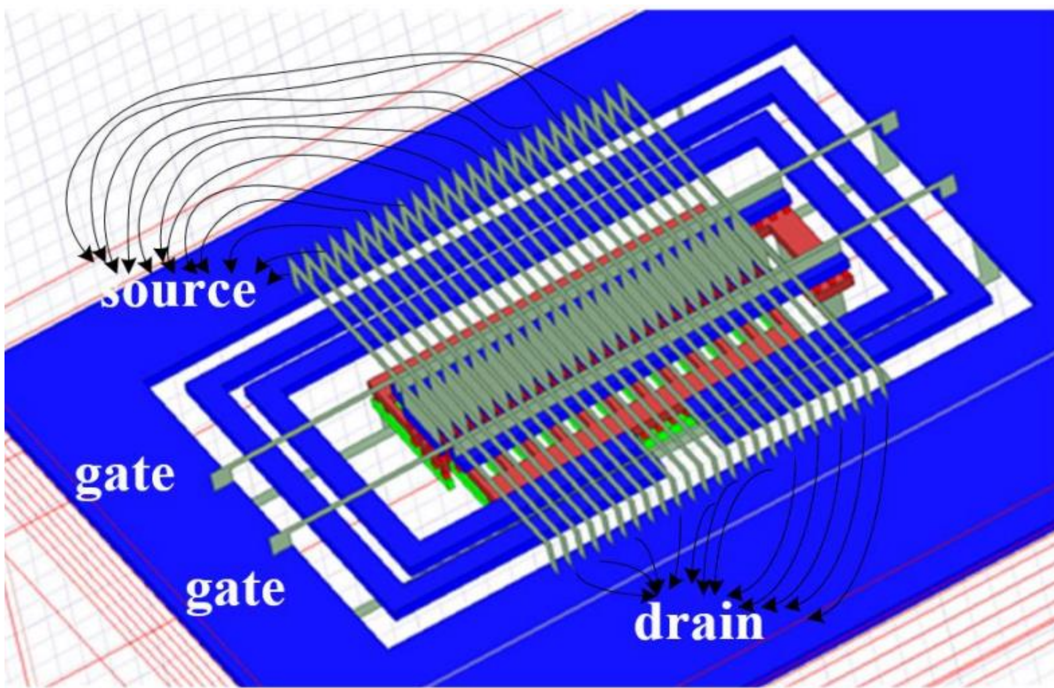


(a)



(b)

(c)

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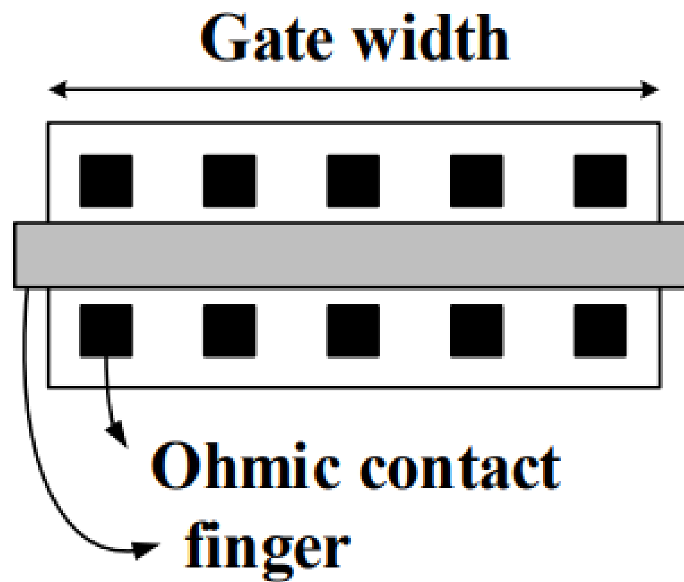

Fig. 2.26 3-D layout of the transistor with 24f ×0.6μm in HFSS. (a) The top view of transistor layout. (b) The back view of transistor layout. (c) The side view of transistor layout(d) The floor plan of a single finger [56].

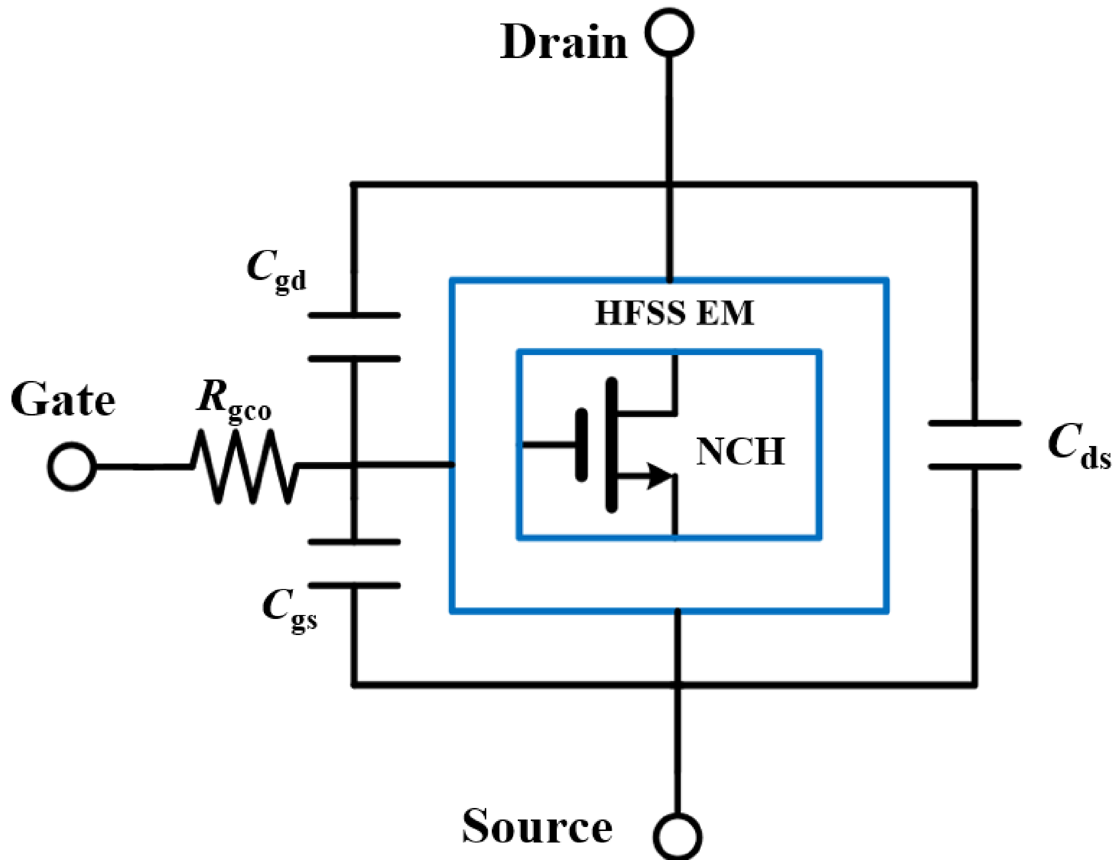

Fig. 2.27. The schematic diagram of NCH model transistor with parasitic parameter.

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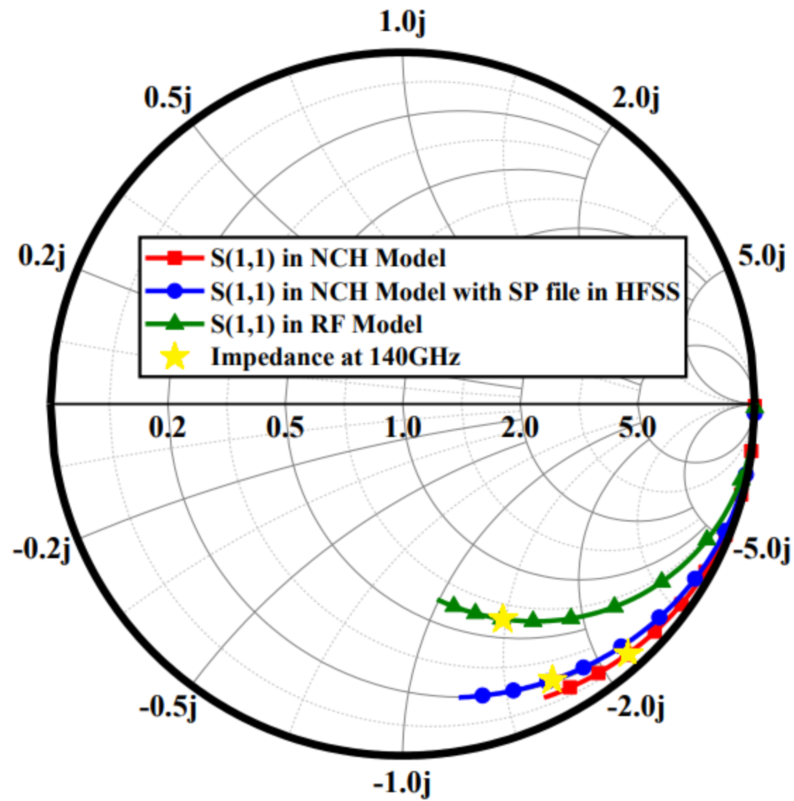

Fig. 2.28. The comparison of different S (1,1) models from 1 to 200 GHz.

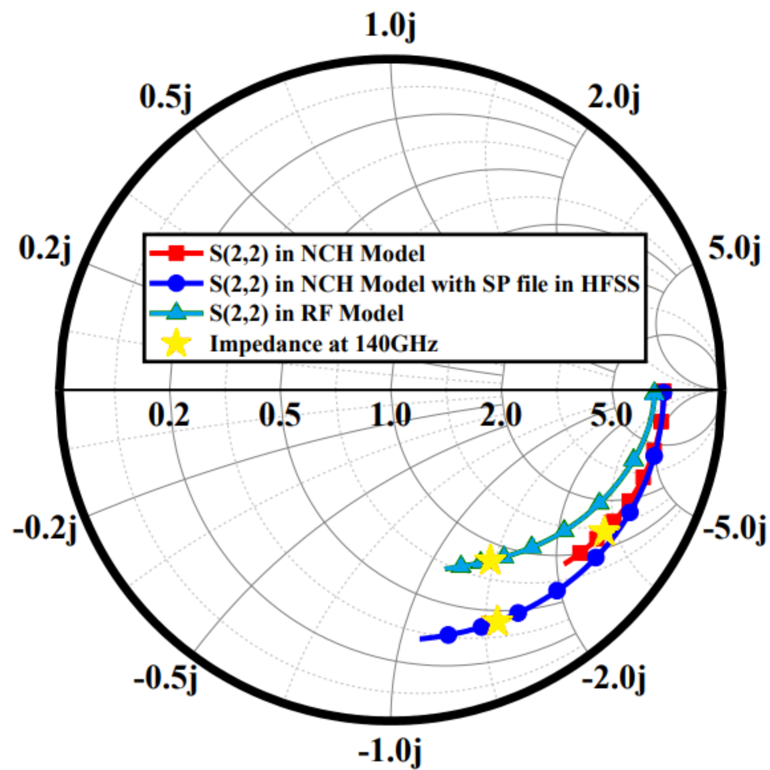

Fig. 2.29. The comparison of different S (2,2) models from 1 to 200 GHz

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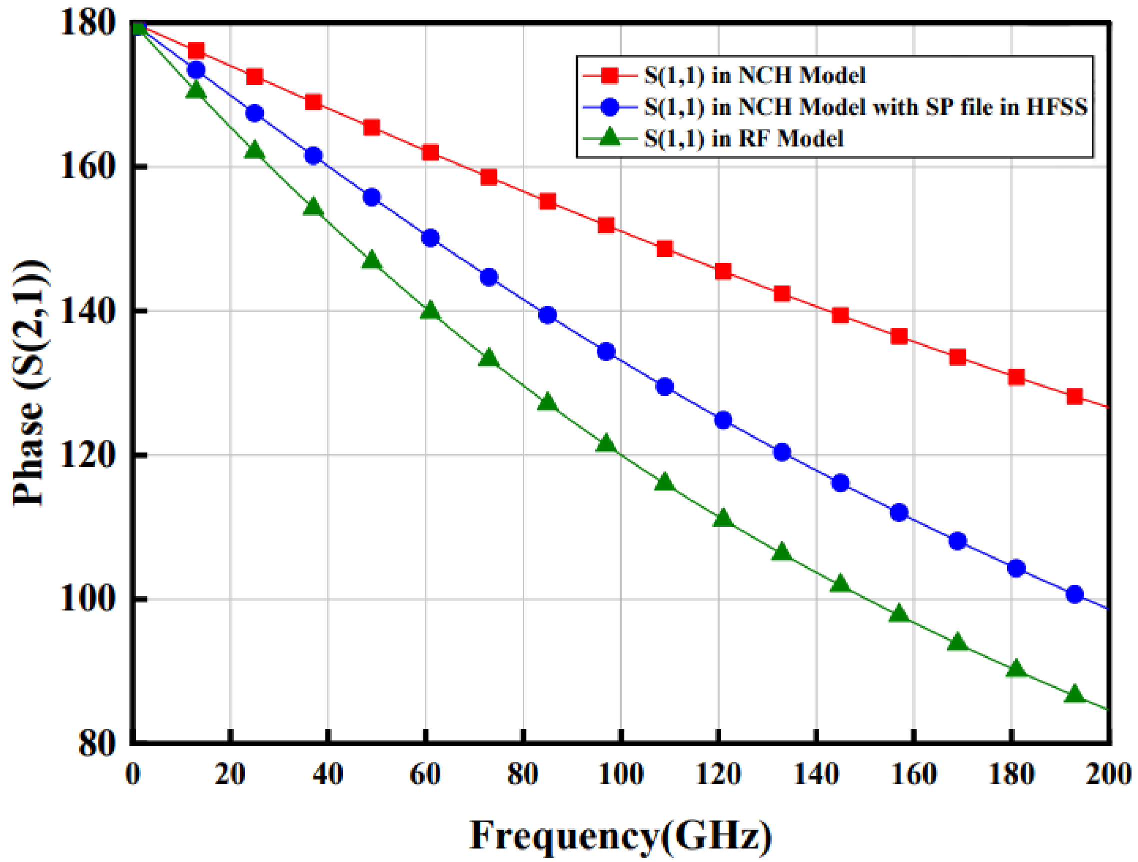

Fig. 2.30. The phase comparison of different models.

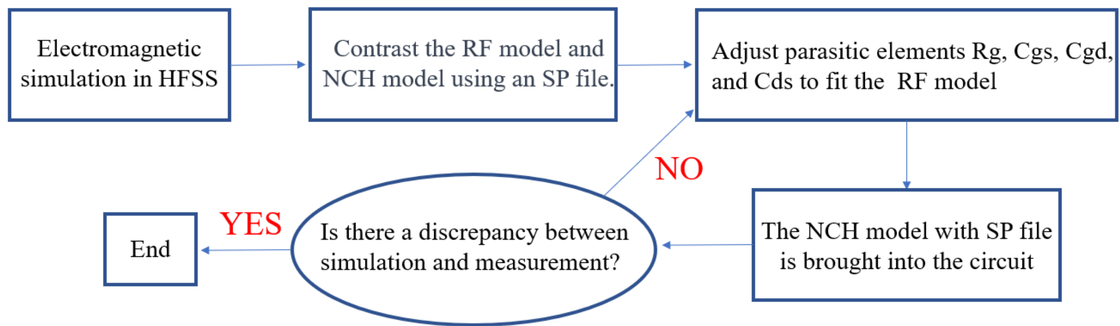

Fig. 2.31. The design flow of the debug [55]

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Table 2.2 The values of R_{gco}, C_{gs}, C_{gd}, and C_{ds} with different transistor size.

	R_{gco}	C_{gs}	C_{gd}	C_{ds}
12 fingers ×0.6 μm	43Ω	5.3 fF	-1.7 fF	-8 fF
16 fingers ×0.8 μm	38 Ω	7.6 fF	-2.3 fF	-10.3 fF
20 fingers ×1.8 μm	44 Ω	8.8 fF	-3.3 fF	-12.6 fF

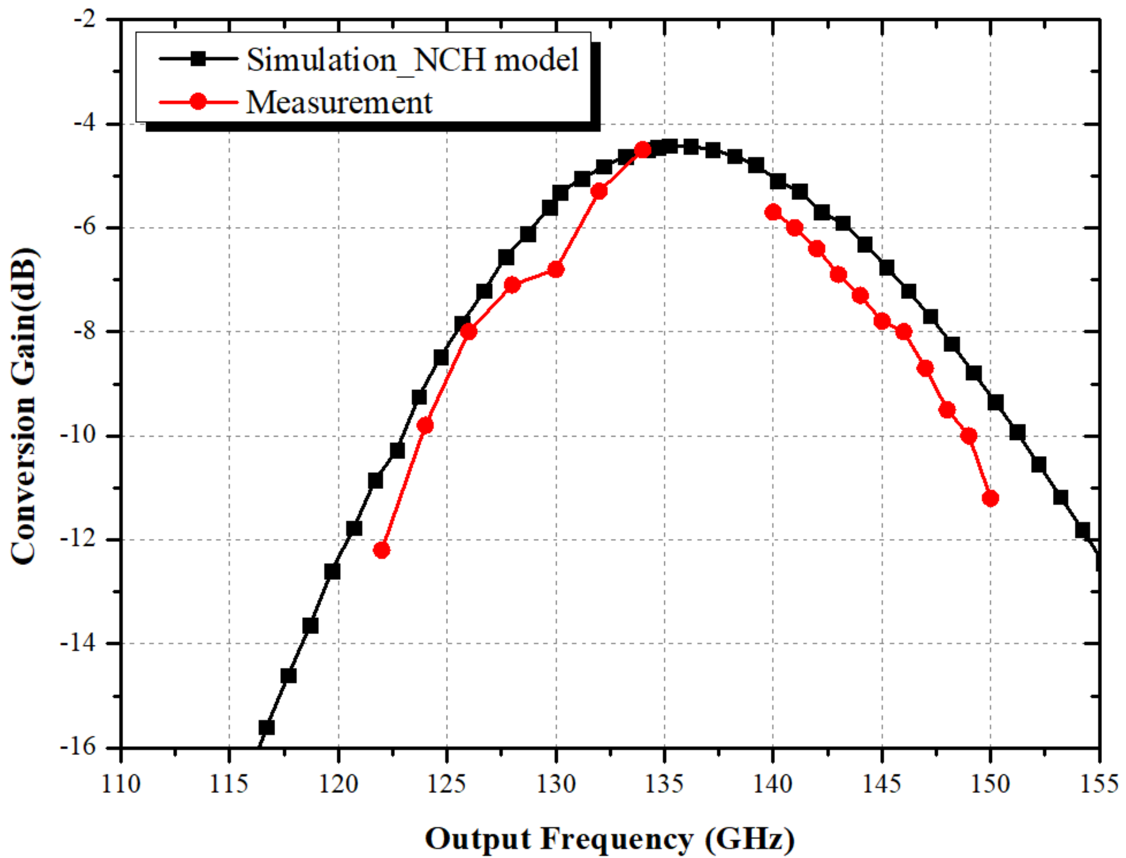

Fig. 2.32. The measured and re-simulated results of conversion gain after considering parasitic effects in transistors.

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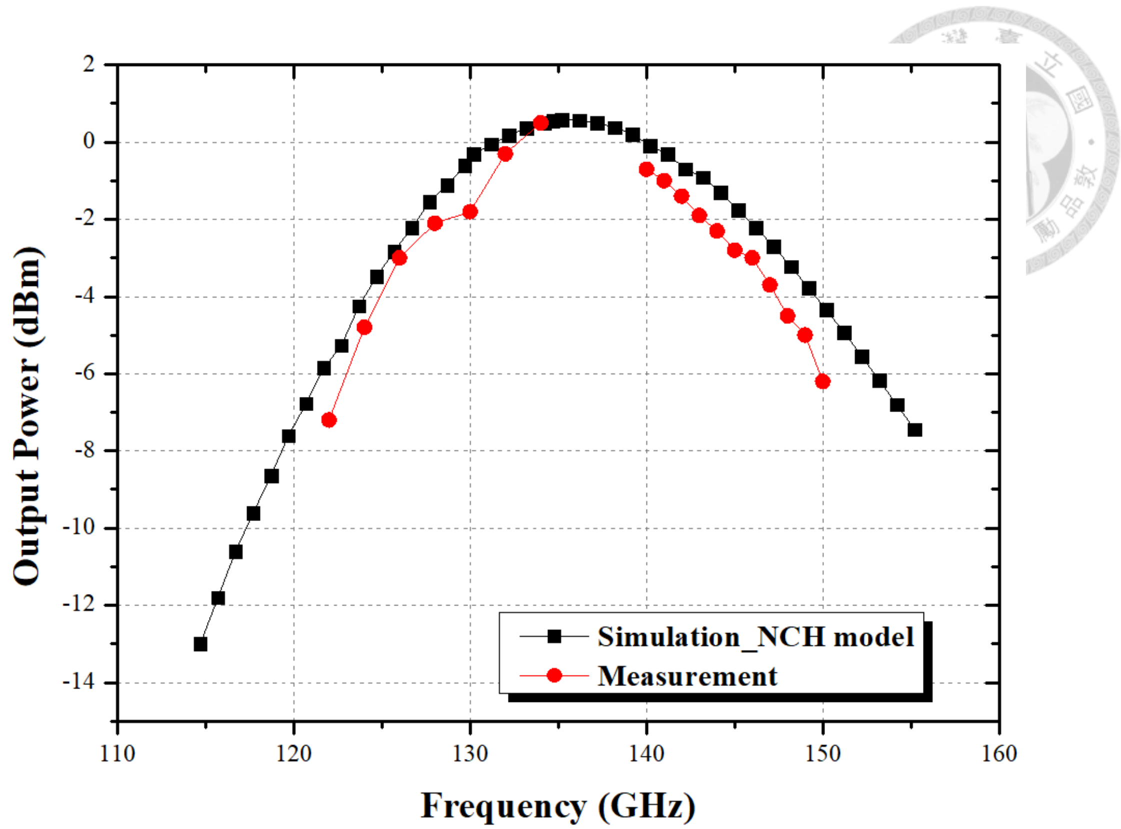

Fig. 2.33. The measured and re-simulated results of output power after considering parasitic effects in transistors.

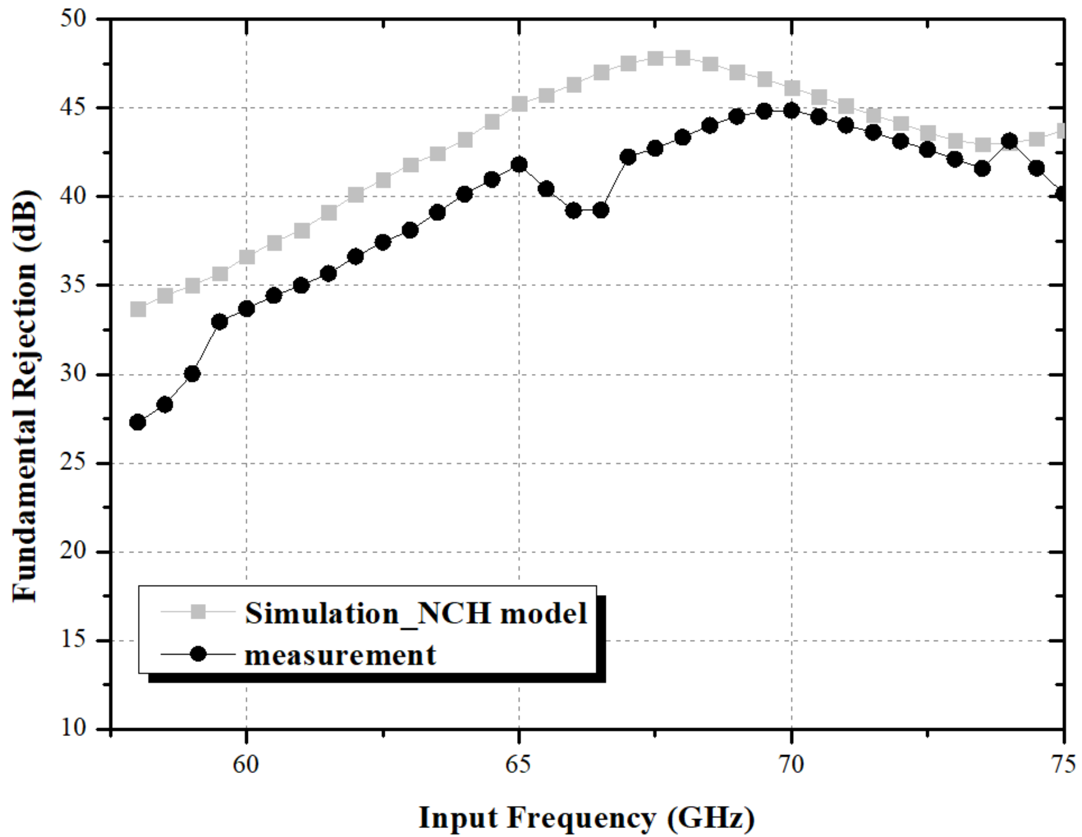

Fig. 2.34. The measured and re-simulated results of output power after considering parasitic effects in transistors.

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2.5 Summary

This chapter introduces a novel D-Band frequency doubler designed for low power consumption, utilizing the g_m-Boosting technique within a 28-nm CMOS process. The first stage of the design involves a drive amplifier, strategically employed to reduce the necessary input power. Subsequently, the second stage employs a cascode topology featuring g_m-boosting. This g_m-boosting technique, when applied to the doubler, emerges as a highly effective approach to achieve elevated output power. The integration of g_m-boosting not only enhances the efficiency of the proposed doubler but also leads to an increase in its output power. This is well illustrated in Table 2.3, where the performance metrics of various published CMOS active frequency doublers from recent years are summarized. In comparison with the published CMOS D-band frequency doubler, it's notable that despite its position as the most efficient option within Table 2.3, the doubler presented in [18] exhibits a notably inferior fundamental rejection. This distinction arises because the differential signal in the referenced work is generated using a transformer, rather than the Marchand Balun topology. While the transformer technique can mitigate insertion loss, it compromises fundamental rejection. However, choosing smaller transistors results in lower power consumption, which in turn leads to lower output power compared to other works. In contrast, the proposed doubler manages to deliver competitive efficiency at a comparable fundamental rejection level. Except for works using advanced CMOS silicon on insulator processes, the proposed doubler shows the competitively efficiency in same fundamental rejection level, lowest power consumption with good conversion gain.

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Table 2.3 Performance Comparison of Recently Published Active Frequency Doubler

Ref.	**Process**	**BW (GHz)**	**CG* (dB)**	**Pout@Pin (dBm)**	**FR** (dB)**	**Pdc (mW)**	**Total Efficiency (%)**
[4]	65-nm CMOS	95-150	-8	3@11	>33	22.8	5.6
[16]	22-nm FDSOI	125-145	-5.5	4.1@9.6	>15	24.7	8.2
[17]	28-nm CMOS	96-134	-6.2	1.8@8	N/A	12	12
[18]	28-nm CMOS	105-130	-2	4@6.2	>16	14	11
[19]	45-nm CMOS SOI	135-160	-3	3.5@6.5	N/A	25	6.2
This work	28-nm CMOS	126-146	-4.5	0.5@5	>34	12	7.4

CG*: Conversion Gain, FR**: Fundamental rejection.

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Chapter 3 K_a-Band Low Power Wideband LNA in 90-nm CMOS Process

A low-power Ka-band low noise amplifier (LNA) for next generation radio astronomical receivers fabricated in 90-nm CMOS technology is presented in this chapter. A new type of doubler-transformer-coupler technique is utilized for higher gain. In order to achieve high gain with limited dc power consumption (PDC), a current-reused technique is applied to the circuit. According to measurement, the proposed Ka-band LNA achieves a 19.1-dB small signal gain with 18.3-GHz 3-dB bandwidth (21.9-40.2 GHz) and limit noise figure of 3.4 dB with only 7.1-mW PDC. To the author's knowledge, among the published Ka-band low-power CMOS LNAs, the LNA has a high figure of merit (FOM) of 19.1 GHz/mW.

3.1 Introduction

In the upcoming generation of radio astronomical heterodyne array receiving systems, the focal plane array (FPA) configuration stands out as an appealing option. This configuration offers a significant enhancement in wide-field mapping speed and system sensitivity without necessitating major antenna redesign[41]. To maximize the number of pixels achievable within the focal plane, it becomes imperative to minimize the power consumption of active devices. This is due to the fact that the FPA needs to be cooled to temperatures between 15-20 K for low-noise amplifier-based systems and 4 K for superconductor-based front-ends. The cooling power available is limited, thereby necessitating efficient power management for optimal performance. As a result, the maximum pixel count of an FPA is constrained not only by the physical dimensions of the antenna focal plane but also by the consumption of DC power.

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Taking into account thermal concerns, multiple approaches are employed to restrict power usage while upholding adequate gain and a minimal noise figure. One such technique involves the implementation of the forward body-bias method. This technique works by diminishing the threshold voltage, thereby enabling the application of a lower supply voltage to reduce the power dissipation (P_{DC}) [42], as illustrated in equation (3.1).

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2|\emptyset_F| - V_{BS}} - \sqrt{2|\emptyset_F|} \tag{3.1}$$

where V_{TH0} is the threshold voltage for VBS=0, γ is a process parameter, and φF is a physical parameter. However, according to the lower V_{TH}, drain current is also increased by this method, which can be expressed as [43]

$$I_{D,sat} = \frac{1}{2}\mu_0 C_{ox}\left(\frac{W}{L}\right) * (V_{GS} - V_{TH})^2 * (1 + \lambda V_{GS}). \tag{3.2}$$

Also, the quantitative analysis of the device performances by using forward body-bias technique can be discussed. Table 2.1 lists the MSG and $NF_{\min}$ of the transistor with 28-µm total gate width under a constant P_{DC} at 30 GHz with and without the forward body-bias technique. The results show that the performances are almost identical under a constant P_{DC}. However, if the forward body-bias technique is used, the circuit needs a bias circuit and a pad to bias the body terminal of the transistor, which will occupy additional layout area. Therefore, this technique does not seem to save the dc power.

Table 3.1 Performances summary by using the forward body-bias technique

V_{DS} = 0.6 V	Gate voltage	Drain current	G_{max}	NF_{min}
V_{BS} =0V	0.5 V	3.1 mA	10.65 dB	1.93 dB
V_{BS} =0.1V	0.487 V	3.1 mA	10.64 dB	1.93 dB
V_{BS} =0.2V	0.473 V	3.1 mA	10.63 dB	1.944 dB

Another technique is the current-reused technique, which is commonly adopted in

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ultra-low-power amplifiers [44]. Given the shared RF path in cascode technology, it draws upon the power consumption of CS+CG from a DC perspective. However, from an RF standpoint, due to the presence of a RF ground between CS and CG, a two-stage CS configuration emerges. This results in elevated gain due to the formation of this two-stage CS setup.

In this chapter, a low-power K_a-band LNA for next generation radio astronomical receivers is proposed. A current-reuse double-transformer-coupling (DTC) technique is utilized in first stage to save power consumption. Besides, a new type of double-transformer-coupling (DTC) technique is employed for enhancing the gain performance of the LNA. Compared with others low-power wideband CMOS LNAs in this band, this LNA offers high gain and low noise performance with 7.1-mW PDC.

Table 3.2 Specifications of the K_a-band CMOS LNA.

	LNA Specifications
Process	90-nm CMOS Process
Frequency	20-40 GHz (k_a-band)
Gain	20 dB
Noise Figure	As low as possible
IP_{1db}	> -23 dBm
Power Consumption	< 9 mW

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3.2 The Design of K_a-band LNA

3.2.1 Biasing Selection and Device Selection

Conventional LNA design revolves around three pivotal aspects: gain performance, noise performance, and stability. Diverse bias conditions and device sizes yield distinct characteristics in relation to these three factors. Consequently, the initial focus should be on establishing the appropriate bias conditions and device sizes to optimize the overall performance of the LNA.

Regarding bias selection, the transconductance (g_m) and drain current (I_{DS}) for this device, maintained at a V_D of 0.6 V and various V_G levels, are depicted in Fig. 3.1. and Fig. 3.2. respectively. Simulations reveal that the peak g_m is achieved at V_G around 0.75 V, corresponding to Class-A operation. However, for LNAs, operation typically occurs within the small-signal region, implying that high linearity in the large-signal region isn't a primary concern. As such, the LNA's bias voltage can be set within the range of 50-70% I_D of the peak g_m, occurring at V_G approximately between 0.5 V and 0.6 V. These bias conditions allow for satisfactory gain performance without significant degradation while substantially reducing DC power consumption. Fig. 3.3. displays dc-IV characteristic curve of the 14-finger device with a total gate width of 28-μm.

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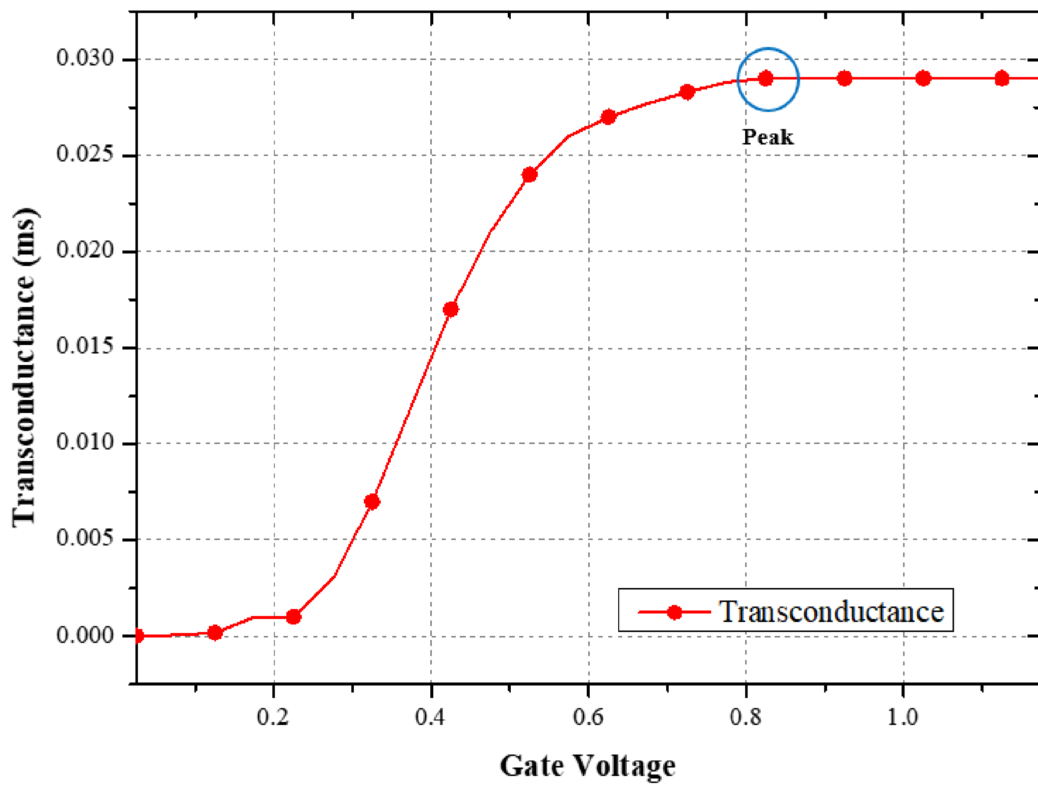

Fig. 3.1. g_m of the transistor with 28-μm total gate width in different V_G

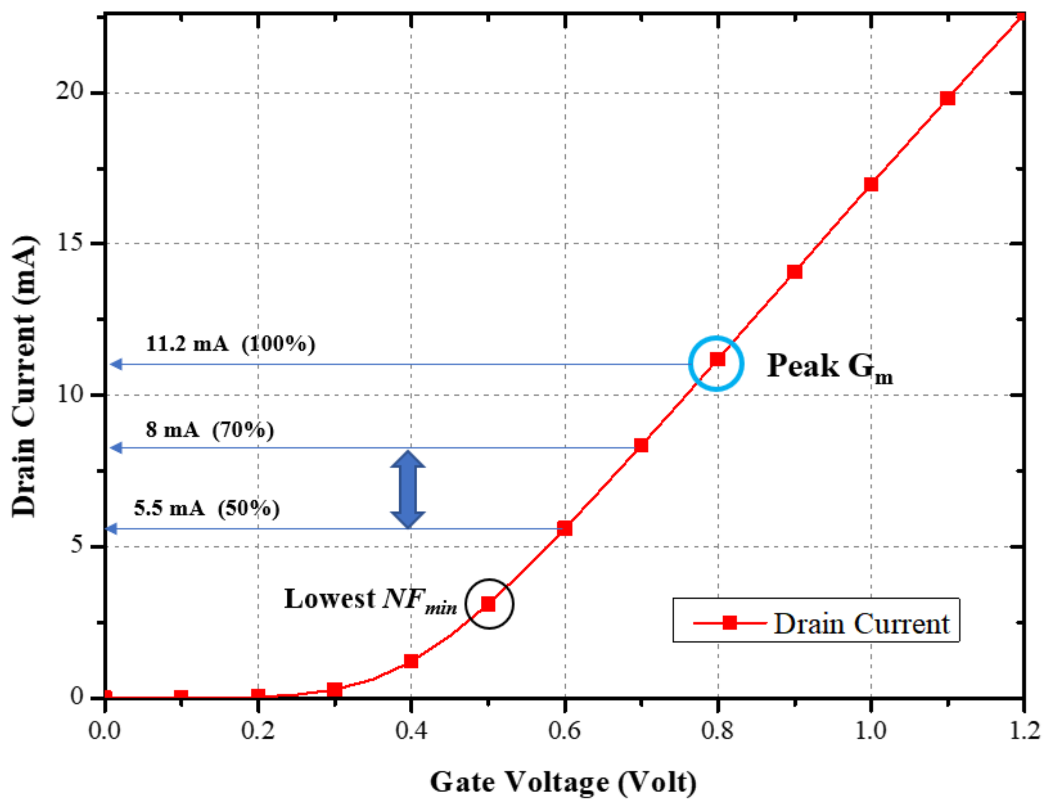

Fig. 3.2. Drain Current of the transistor with 28-μm total gate width in different V_G.

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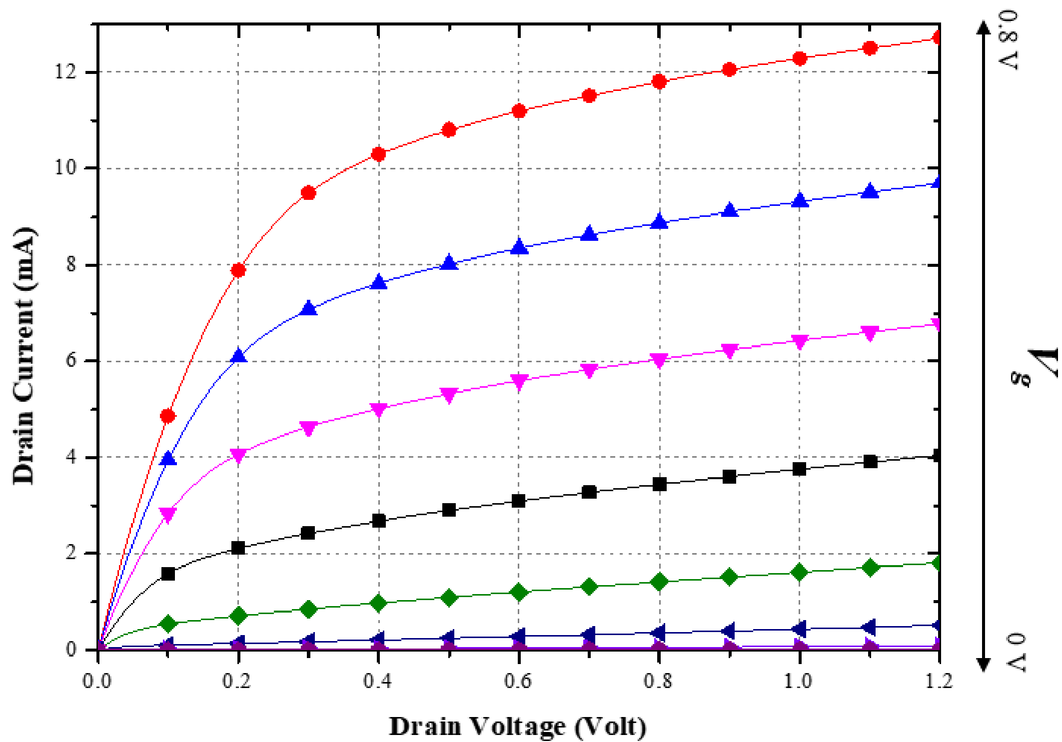

Fig. 3.3. dc-IV curves of the transistor with 28-μm total gate width.

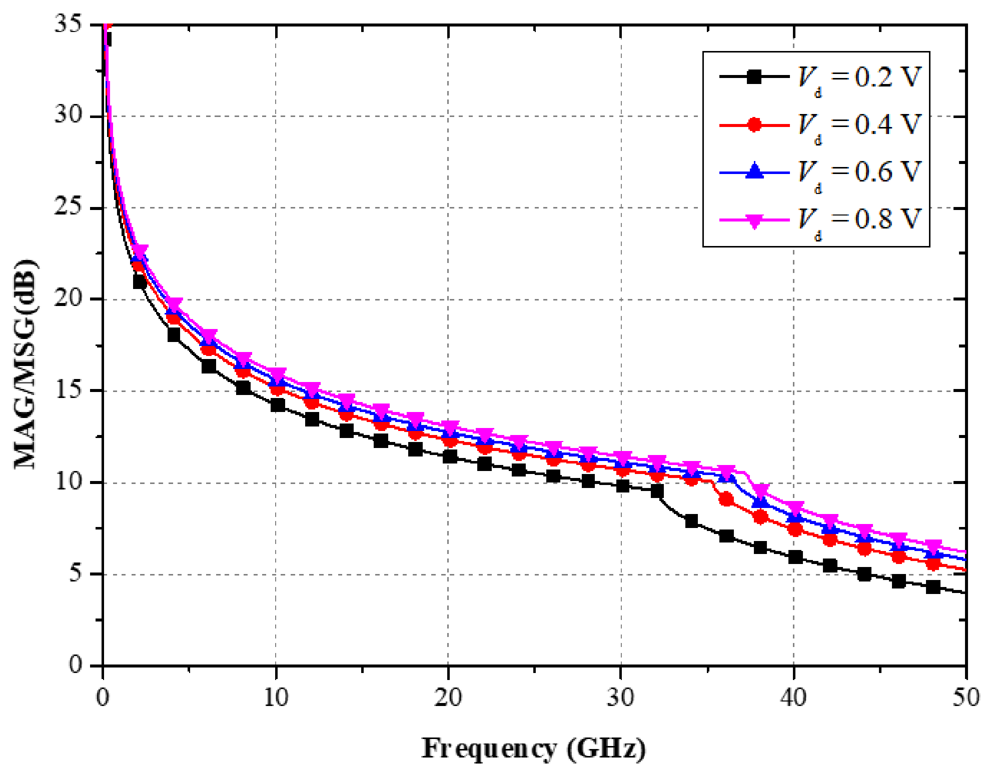

Fig. 3.4. MSG/MAG simulation with 28-μm total gate width in different V_d.

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Fig. 3.5 illustrates the characteristics of MSG/MAG and the minimum noise figure (NF_{min}) for the device operating with a V_d of 1.2 V across different V_g levels. The lowest NF_{min} occurs at V_g around 0.5 V, enabling a reduction in the DC drain current (around 30% of the peak g_m). Notably, the MSG experiences a minor 1 dB degradation in comparison to the Class-A operation. Consequently, when planning to design the LNA with a multi-stage topology, and when achieving an overall gain of greater than 20 dB while operating under low power consumption is feasible, selecting the bias voltage at V_g of 0.5 V becomes advantageous. Fig. 3.3 and Fig. 3.4 illustrate the result that choosing V_d at 0.6 V achieves high gain and low power consumption. This choice aids in conserving DC power and attaining the lowest noise figure possible. Despite the decrease in gain performance, it remains sufficiently effective in suppressing the noise contribution from subsequent components within the system.

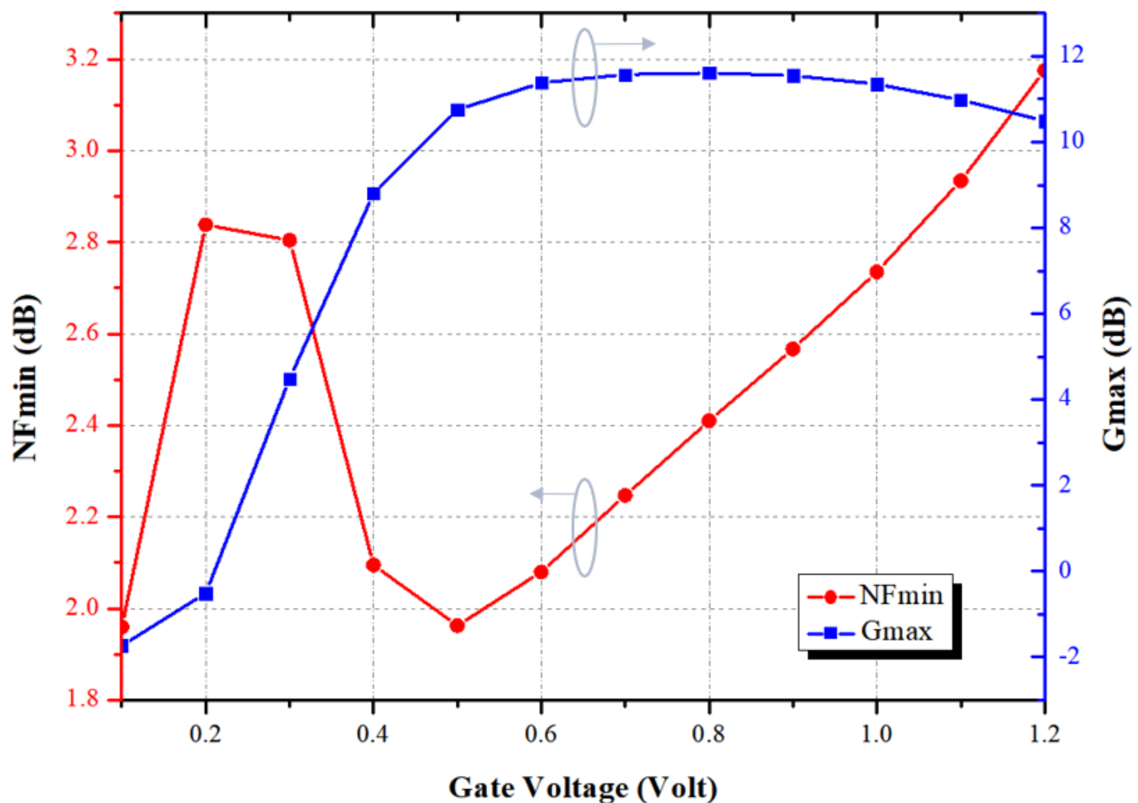

Fig. 3.5. G_{max}, NF_{min} of the transistor with 28-μm total gate width in different V_g.

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For the purpose of selecting device size, Fig. 3.6, Fig. 3.7, Fig. 3.8, and Fig. 3.9 illustrate the variations of MSG/MAG, NF_{min}, and stability factor across different device sizes while maintaining the same bias conditions (V_D = 0.6 V, V_G = 0.5 V) and utilizing 80 pH inductive degeneration at the source terminal. The findings reveal that smaller transistors exhibit improved MSG and lower NF_{min}; however, their stability is compromised. Additionally, smaller devices tend to yield notably high impedance, posing a challenge to match them to a 50 Ω impedance. A summary of the correlation between device size and gain, noise, and stability is presented in Table 3.3.

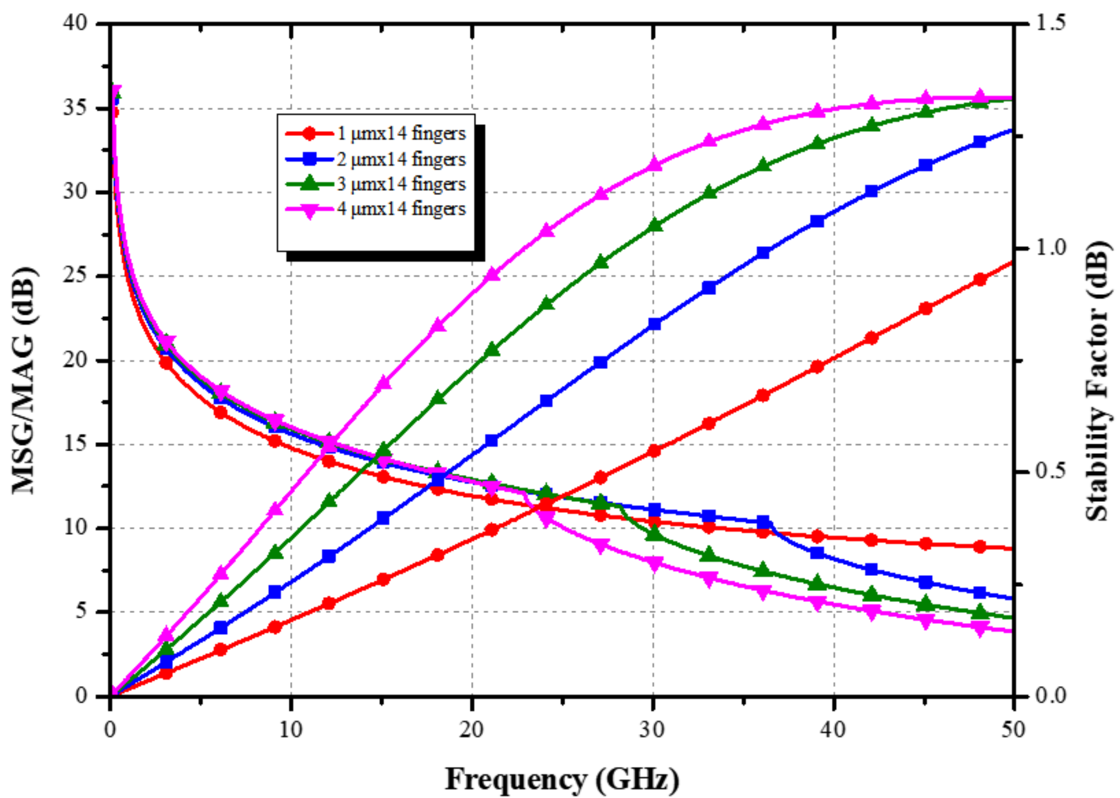

Fig. 3.6. MSG/MAG and stability factor in versus device sizes.

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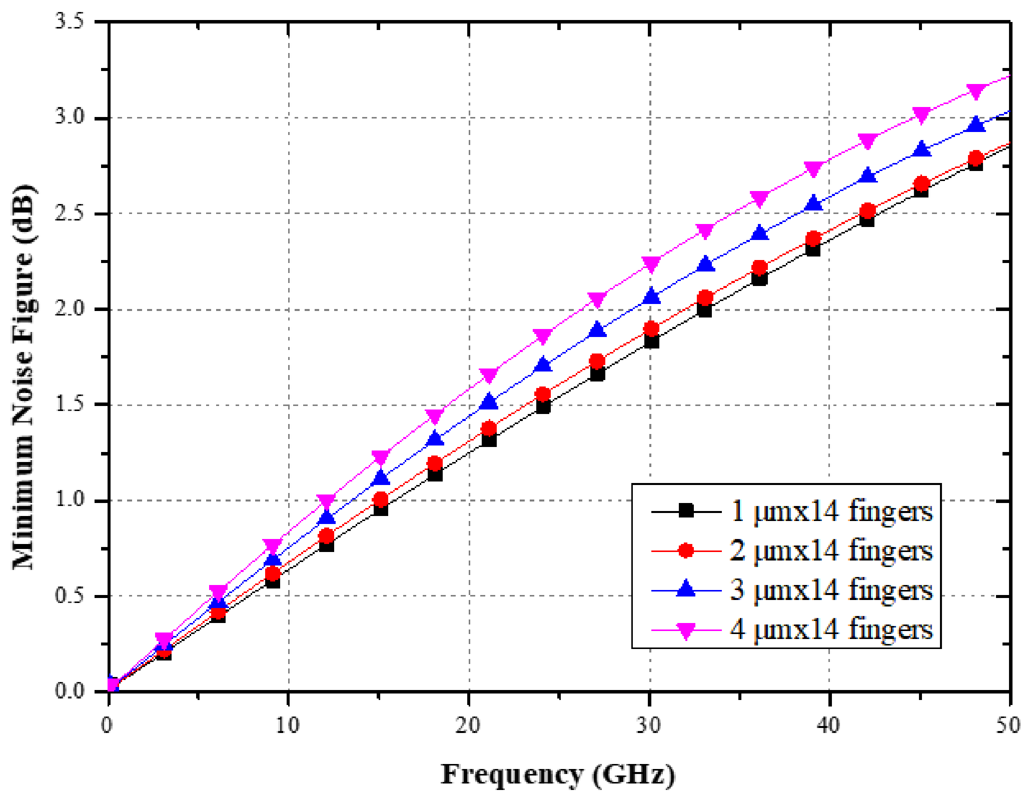

Fig. 3.7. Minimum noise figure in versus device sizes.

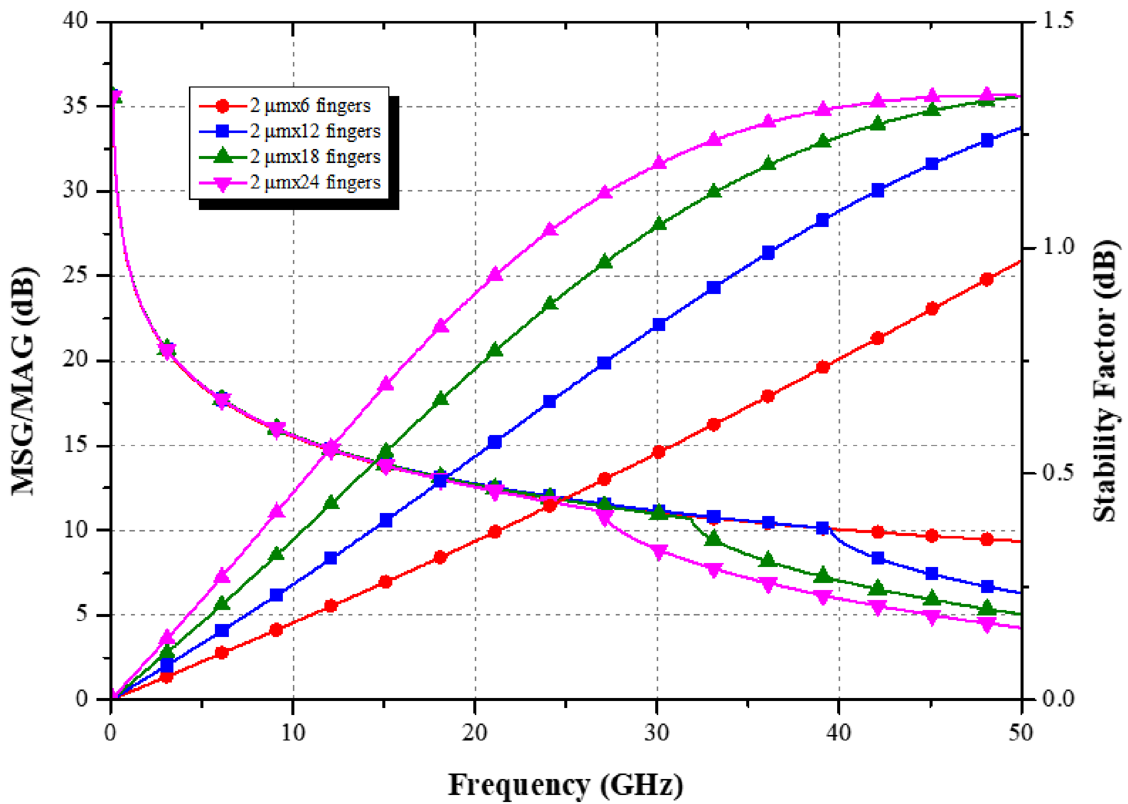

Fig. 3.8. MSG/MAG and stability factor in versus device sizes.

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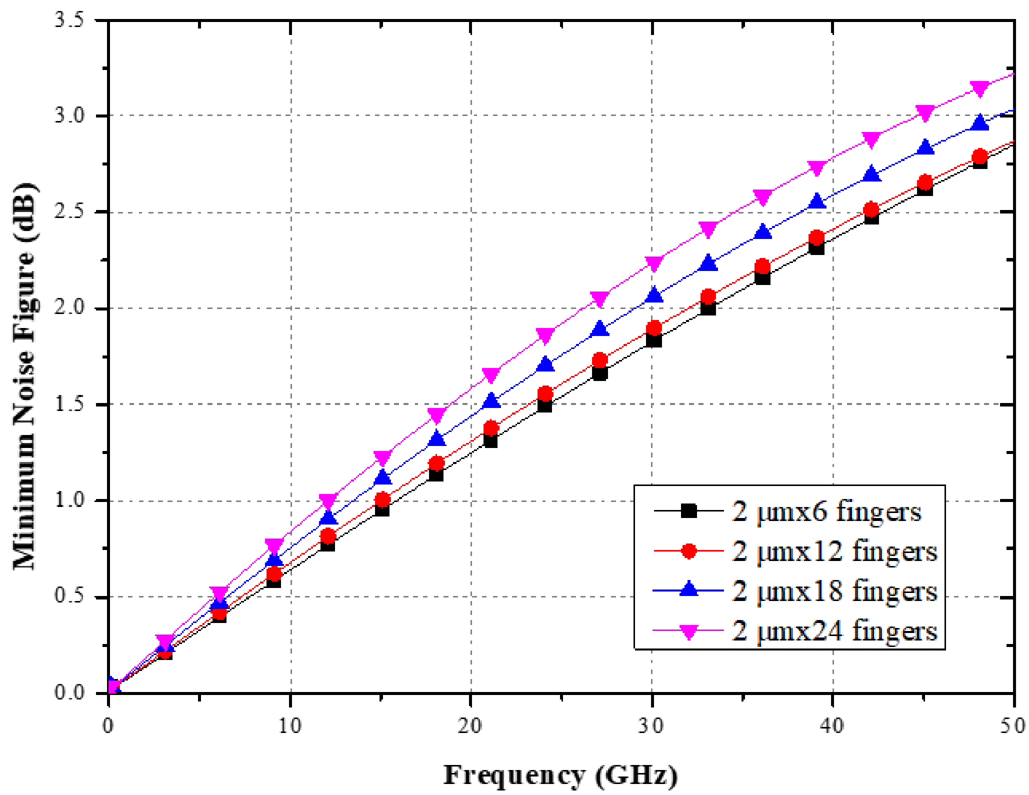

Fig. 3.9. Minimum noise figure in versus device sizes.

Table 3.3. Trade-off study of the device size selection for LNA.

Device Size	Dc Current	MSG/MAG	Noise Figure	Stability
↑	↑	↓	↑	↑
↓	↓	↑	↓	↓

Based on the above simulations, choosing 2 x 14-finger transistor size for the first stage design Additionally, for optimal performance, set the gate voltage bias to 0.5 V and the drain voltage to 0.6 V.

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3.2.2 Current-Reused Double-Transformer-Coupler [44][45].

Fig. 3.10. illustrates the current-reused double-transformer-coupling architecture. In this setup, MOSFETs M1 and M2 are organized in a common-source (CS) configuration, incorporating capacitor C_{c1} to function as an AC ground. The RF signal emanating from M1 is conveyed to M2 through transformer TF_1, which is formed by the combination of two transformers, TF_{1A} and TF_{1B}. This transfer is facilitated by employing inductors L_g, L_d, and L_s. Inductive coupling proves effective for transmitting signals from the lower common-source (CS) stage to the upper common-gate (CG) stage. By using the turns ratio between primary and secondary windings, the transformers can augment voltage gain. Moreover, the arrangement of the double transformers can be leveraged to further enhance gain. Notably, the secondary windings at the gate and source of the upper CS stage are configured in opposing directions, thereby expanding the effective gate-source voltage swing. This double-transformer-coupling configuration contributes positively to both gain and stability, with the inductance L_s playing a stabilizing role. current-reused double-transformer-coupling architecture.

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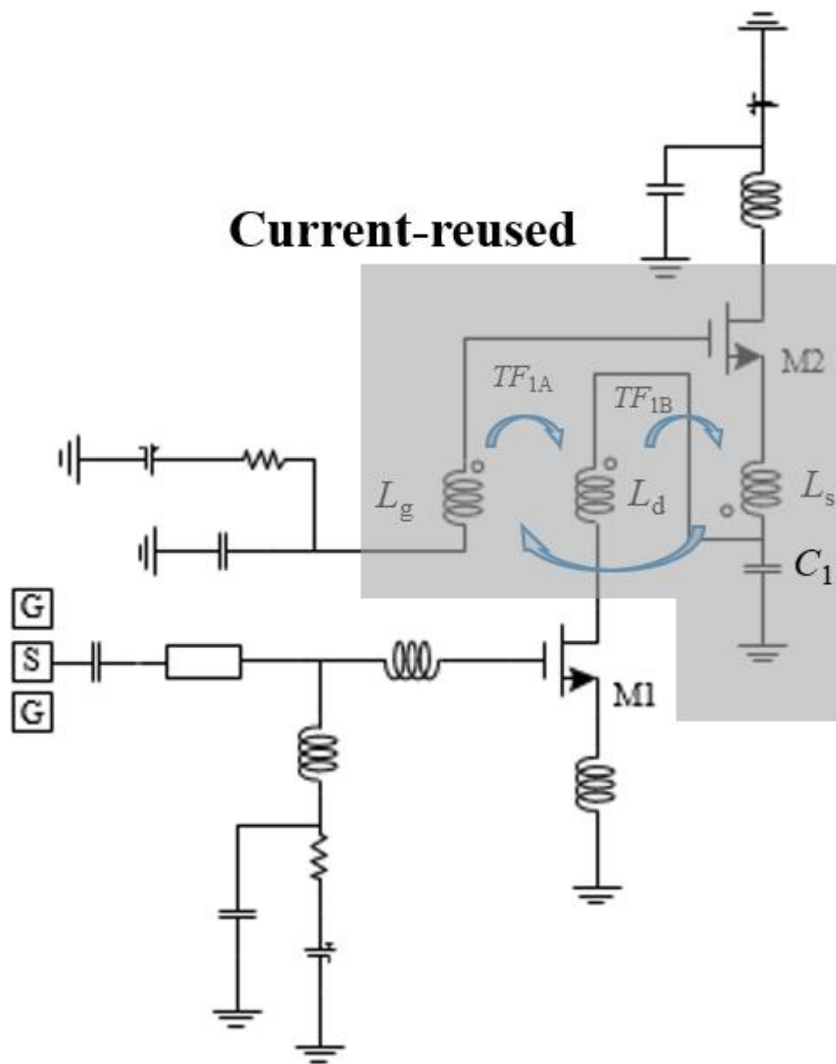

Fig. 3.10. The structure of current-reused double-transformer-coupling.

Fig. 3.11. contrasts the simulation outcomes of the current-reused LNA with three other types of LNA. To ensure a fair evaluation, all four LNAs employ the same two NMOS devices. The current-reused LNA capitalizes on the effects of the double transformers TF_{1A} and TF_{1B}. In contrast, the other two current-reused LNAs employ the effect of a single transformer TF_{1A}, with and without Ls. The cascode LNA features a common-source (CS) to common-gate (CG) structure, devoid of transformers. According Fig. 3.12, the current-reused technique outperforms in terms of minimum noise figure (NF_{min}), and maximum gain.

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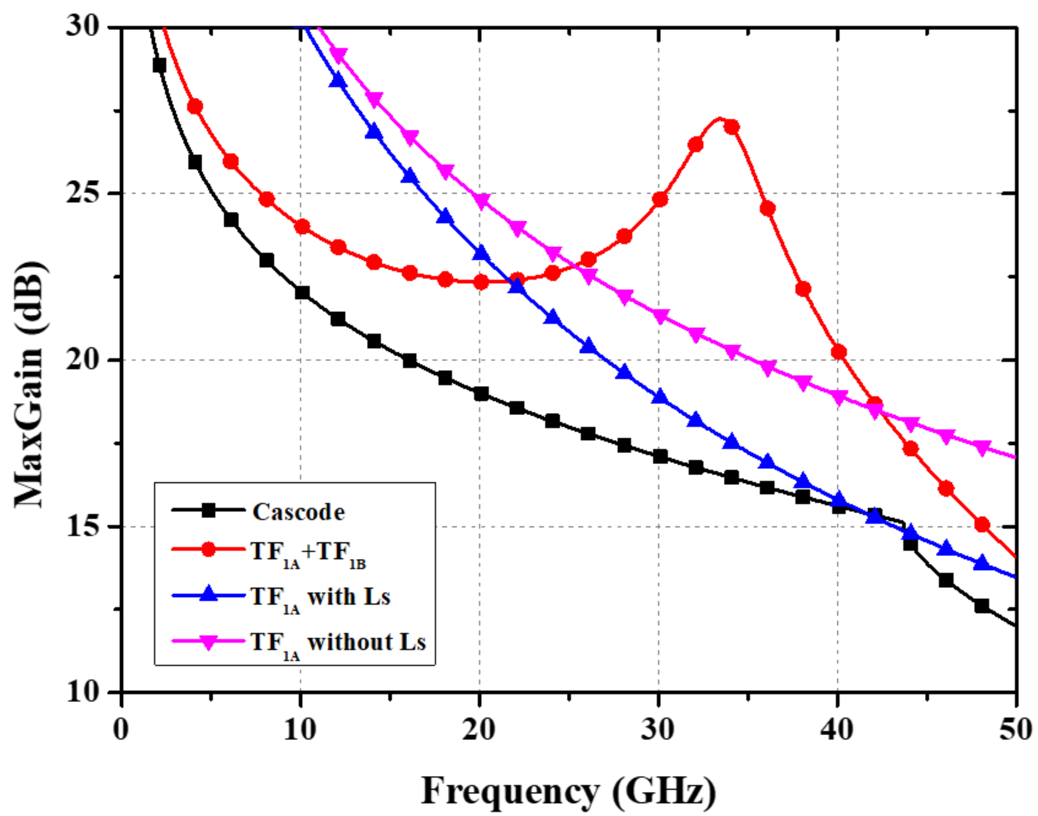

Fig. 3.11. G_{max} comparison of different type of LNA.

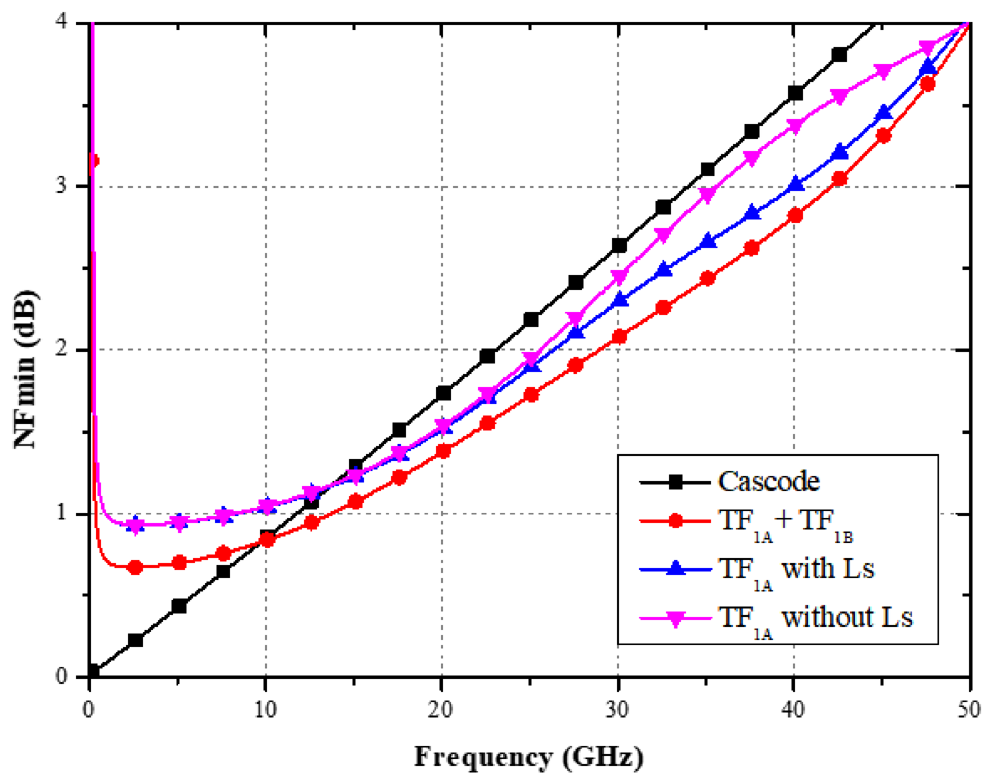

Fig. 3.12. NF_{min} comparison of different type LNA

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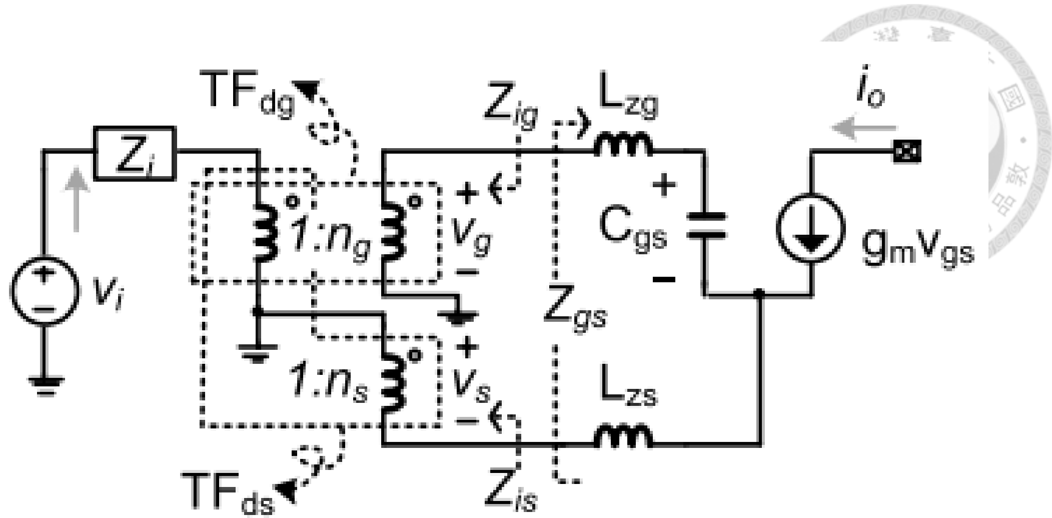

Fig. 3.13. Small-signal model of the CS-CS topology with the double transformers.

Fig. 3.13. illustrates the small-signal model of the CS-CS structure found within the shaded region of Fig. 3.10. At the drain of M1, the voltage v_i is observed. A simplified equivalent circuit model of DTC includes two ideal transformers, TF_{dg} and TF_{ds}, accompanied by associated lumped elements: L_{zg} and L_{zs}. Notably, the effects of lossy factors in these elements are disregarded for simplicity. The equivalent impedance perceived at the primary side of the transformer is then transformed into Z_{ig} and Z_{is}, evident at the secondary side of both the gate and the source. This cumulative impedance is expressed as

$$Z_{igs} = Z_{ig} + Z_{is} \tag{3.3}$$

Z_{gs} stands as the input impedance of M2, incorporating Lzg and Lzs. Within this context, C_{gs} represents the input capacitor of M2, while g_m signifies the transconductance of M2.

$$Z_{gs} = \frac{1}{j\omega C_{gs}} + j\omega\left(L_{zg} + L_{zs}\right) + \frac{g_m L_{zs}}{C_{gs}} \tag{3.4}$$

For clarity, the mutual inductance between L_g and L_s is excluded from consideration. Forming a transformer of turns ratio 1:ng, L_d and L_g comprise transformer TF_{dg}, whereas L_d and L_s constitute transformer TF_{ds} at a turns ratio of 1: n_s. Induced voltages V_g and V_s

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emerge at the secondary windings of TF_{dg} and TF_{ds}, respectively. The overall transconductance $g_m = i_o/v_i$ can be mathematically represented as[45]:

$$G_m = \frac{g_m(n_g + n_s)}{1 + g_m Z_{is} - \omega^2 C_{gs}(L_{zg} + L_{zs}) + j\omega(g_m L_{zs} + Z_{igs} C_{gs})} \tag{3.5}$$

$$= \frac{(n_g + n_s)}{j\omega_0 (L_{zs} + \frac{Z_{igs} C_{gs}}{g_m})} \tag{3.6}$$

where $\omega_0 \approx 1/\sqrt{C_{gs}(L_{zg} + L_{zs})}$ when $g_m Z_{is} << 1$. The g_m is boosted by $(n_g + n_s)$ without additional power consumption compared to the overall transconductance, which does not contain the mutual inductance of the transformer. The L_{zs} would reduce g_m, because

$$G_m = \frac{(n_g + n_s)}{2j\omega_0 L_{zs}} \tag{3.7}$$

where $Z_{igs} \approx Z_{gs}(\omega_0)$. The L_{zs} makes a trade-off relation between the stability and overall transconductance[46]. In conclusion, high transconductance needed a large $n_g + n_s$ and an optimum L_{zs}. The most significant source of noise stems from the channel current noise of M1. When designing a source-degeneration LNA, employing a low transconductance for M1 proves advantageous in achieving a low noise figure (NF). However, this approach also leads to reduced gain for the LNA due to the smaller transconductance. To counterbalance this trade-off, the current-reused structure is introduced, which enhances the overall gain while maintaining a modest transconductance. Furthermore, the introduction of the double-transformer-coupling technique aids in mitigating the additional noise originating from M2. In the illustrated network of M2 within Figure 3(a), the noise figure (NF) can be expressed as follows[45]:

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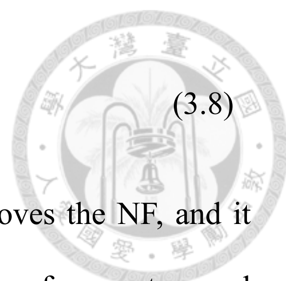

$$NF_{\mathrm{M2}} = 1 + \frac{({n_{\mathrm{g}}}^2 + {n_{\mathrm{s}}}^2) g_{\mathrm{m}} Z_{i\gamma} (\frac{\omega_0}{\omega_{\mathrm{T}}})^2}{(n_{\mathrm{g}} + n_{\mathrm{s}})^2} \tag{3.8}$$

where γ is a bias-dependent factor. Here, $(n_g^2 + n_s^2)/ (n_g + n_s)^2$ improves the NF, and it shows the lowest $NF_{\min}$ in Fig. 3.12. Fig. 3.14 show the structure of current-reused double-transformer-coupler, and Fig. 3.15 show the impedance off S11 and Sopt.

Fig. 3.14. The structure of current-reused double-transformer-coupler

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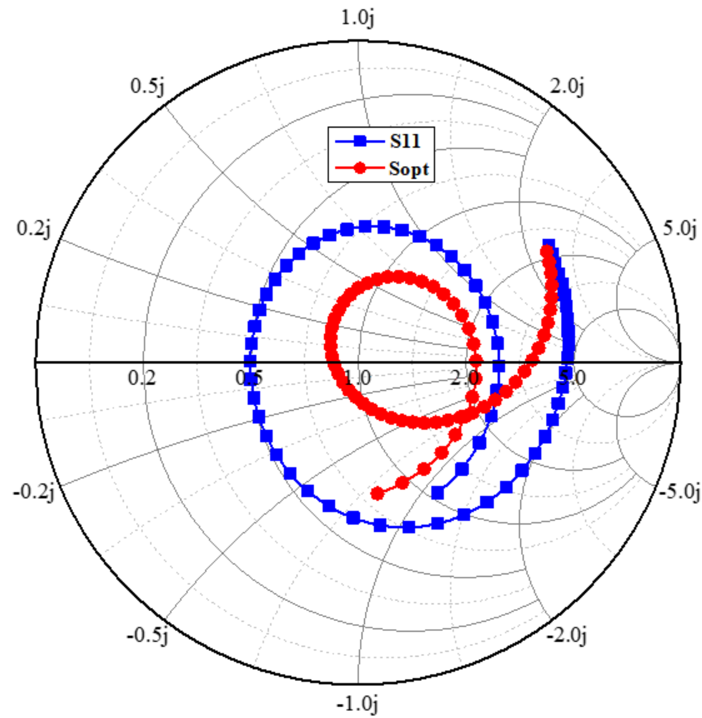

Fig. 3.15. The impedance off S11 and Sopt.

3.2.3 Concept of New Type Double-Transformer-Coupling

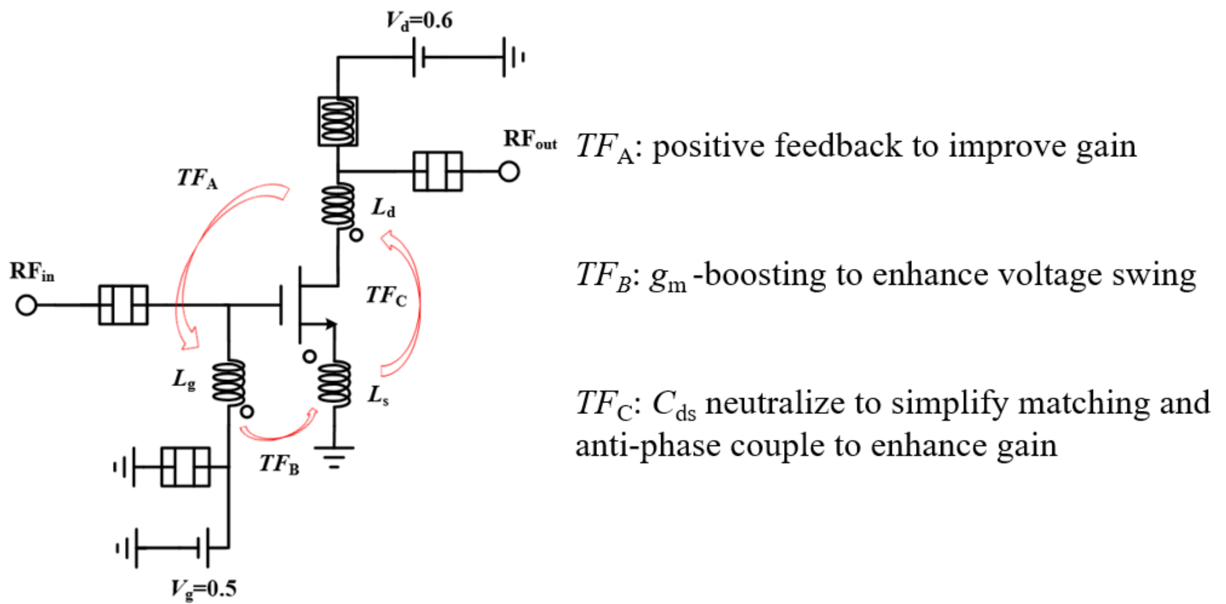

Fig. 3.16. The structure of new type DTC.

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The new type of double-transformer-coupling integrates three key technologies, as illustrated in Fig. 3.16. These technologies include g_m-boosting, positive feedback neutralization, and C_{ds} neutralization, each of which plays a crucial role in optimizing the performance of the system. g_m-boosting, which was previously introduced in Section 2.1.2 [39], is a technique employed to enhance the gate-source voltage swing. This enhancement is achieved using an anti-phase couple facilitated by the magnetic coupling between L_g and L_s. By doing so, the system can effectively increase the g_m (transconductance) and, consequently, improve its overall performance. Fig. 3.17 show the circuit schematic and simulation result as shown in Fig. 3.18.

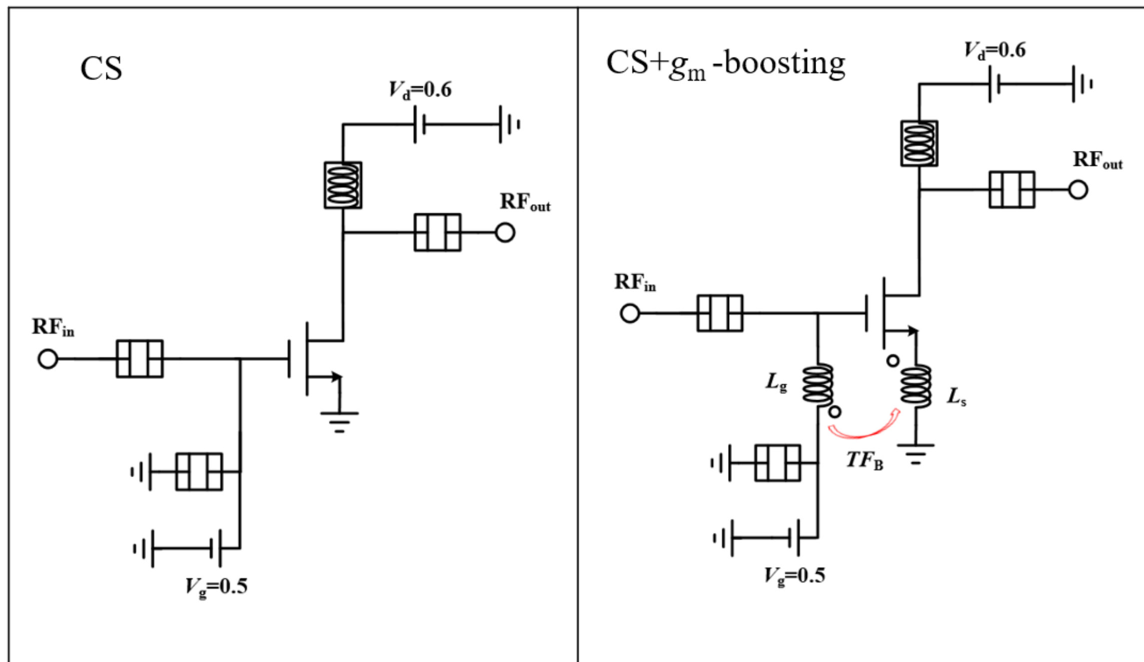

Fig. 3.17. Circuit schematic of CS with and without g_m-boosting.

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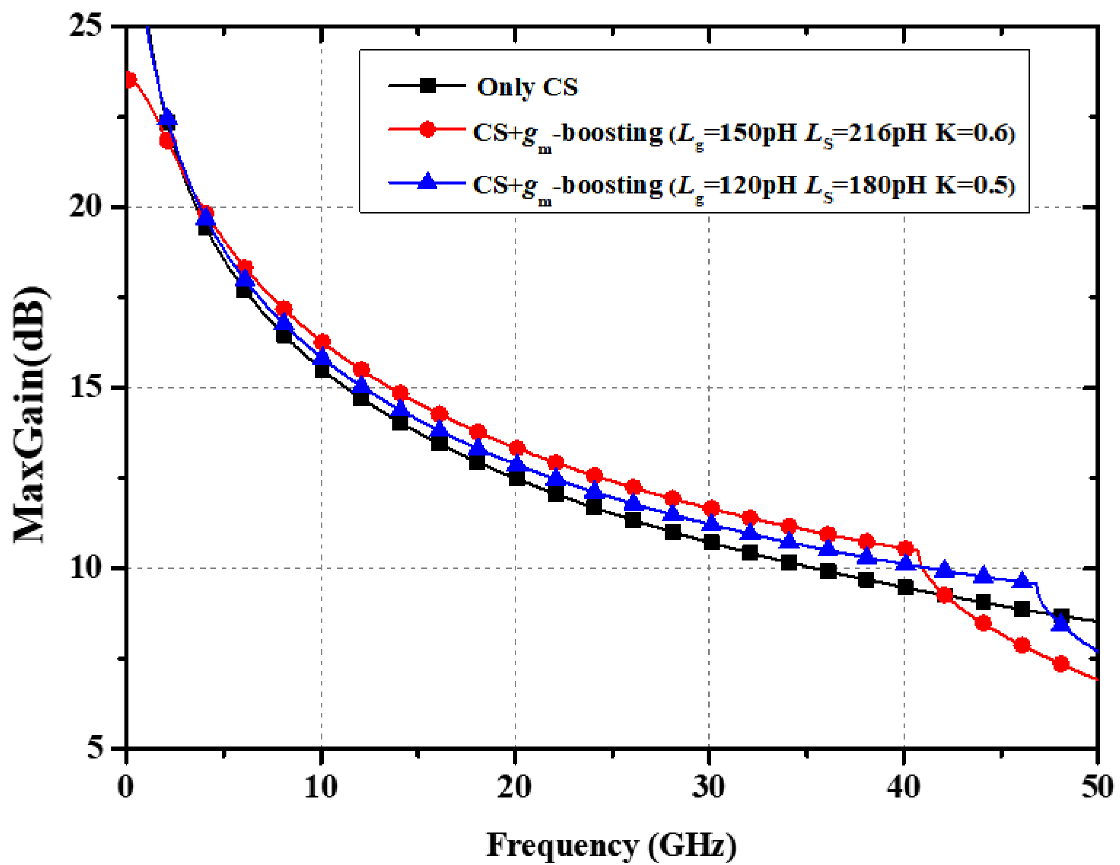

Fig. 3.18. The simulated results of CS and CS with different L_g, L_s, and K.

Positive feedback neutralization serves to eliminate the adverse effects of gate-drain capacitance. This is achieved by establishing an in-phase couple using the magnetic coupling between L_g and L_d, as discussed in [28]. This neutralization technique effectively mitigates any negative impact on the system's performance caused by gate-drain capacitance and positive feedback can improve gain. Fig. 3.20 show the simulation result.

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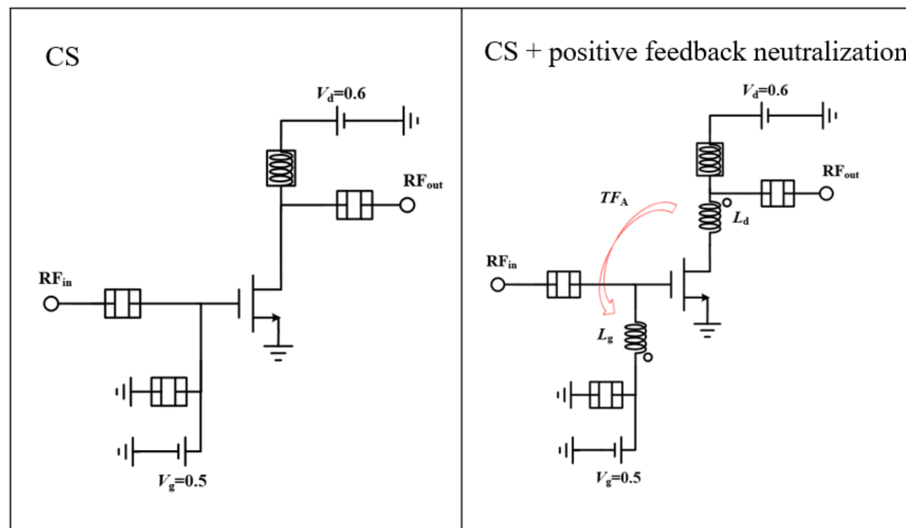

Fig. 3.19.. Circuit schematic of CS with and without positive feedback neutralization.

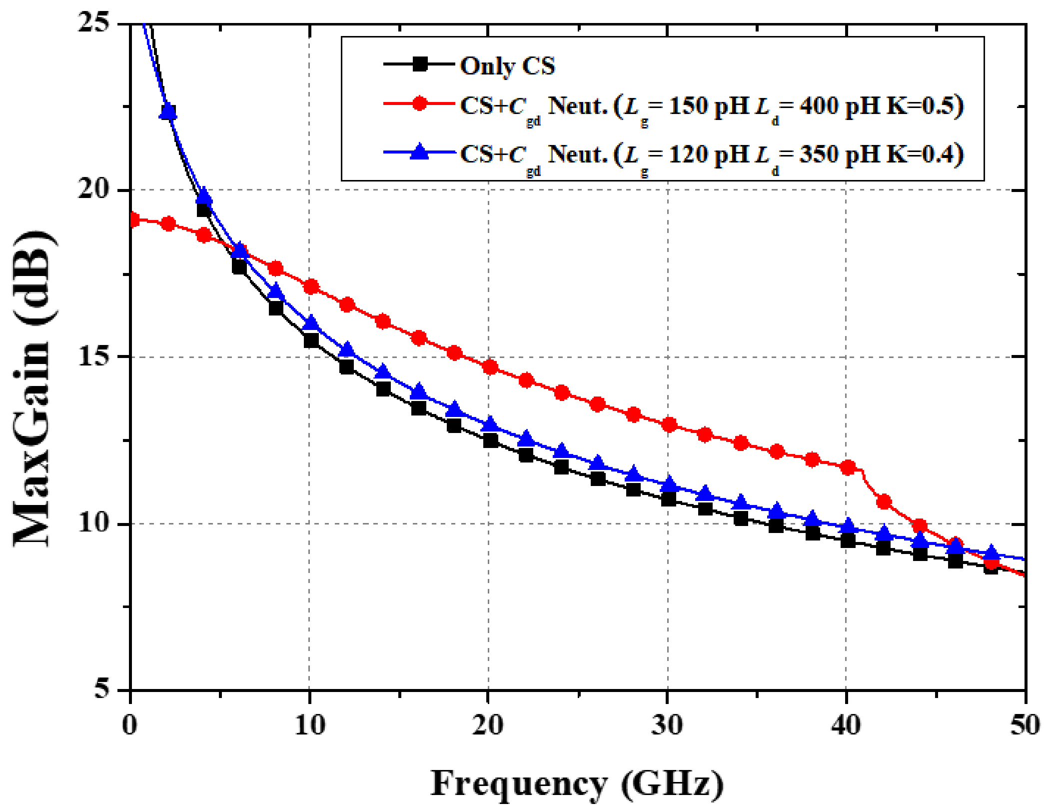

Fig. 3.20. The simulated results of CS and CS with different L_g, L_d, and K.

Neutralization using C_{ds}, on the other hand, focuses on addressing the effects of drain-source capacitance. To achieve this, an anti-phase couple is created through the

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magnetic coupling between L_d and L_s. This neutralization process effectively simplify the matching difficulty by eliminating the conjugate part of impedance. Fig. 3.21 shows the circuit schematic, while Fig. 3.22 illustrates the simulated results where the impedance tends to approach 50Ω.

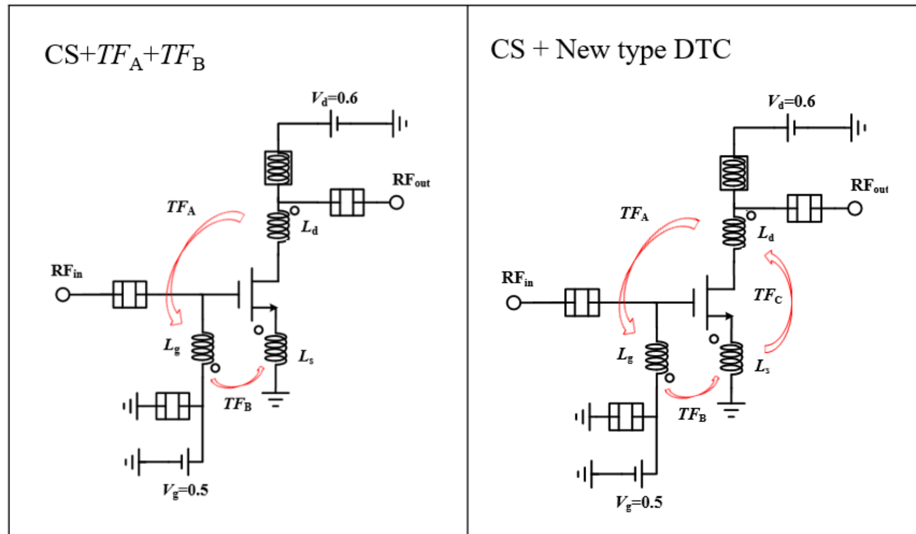

Fig. 3.21. Circuit schematic of new type DTC with and without TF_C.

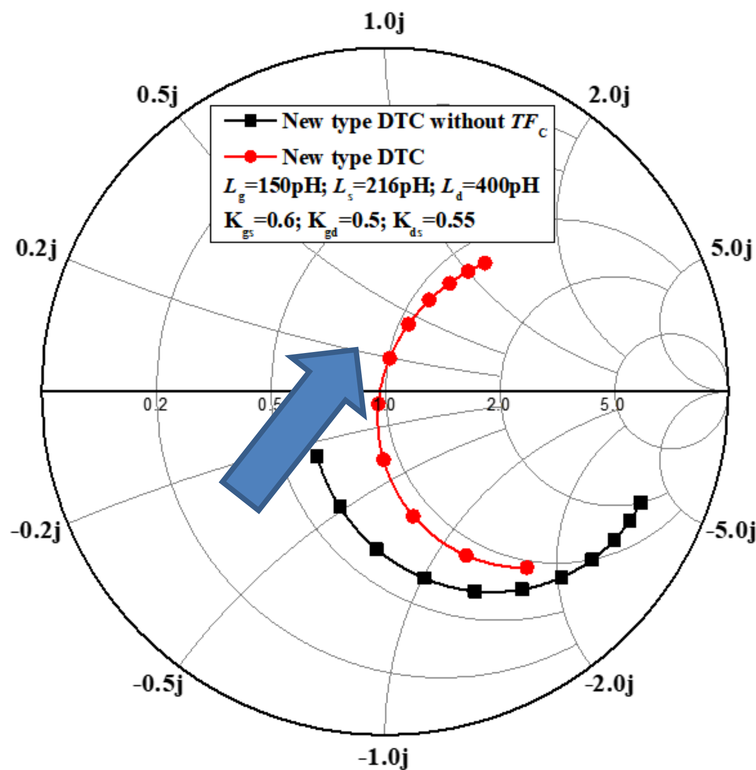

Fig. 3.22. The simulation results of new type DTC with and without TF_C.

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Furthermore, TF_C coupling facilitates the combination of the source signal with the drain signal, as the signal at the source node is in anti-phase with the signal at the drain node, as shown in Fig. 3.23. Inverting the phase of the source signal by 180° allows for the source and drain signals to be in-phase, facilitating superposition [61]. However, due to TF_C employing reverse coupling, the signals on both sides become in-phase, allowing for signal superposition before output. Therefore, the TF_C also improve the circuit gain. Fig. 3.24 shows the G_{max} simulation results of new type DTC with and without TF_C. It shows the G_{max} improved by the signal superposition. Fig. 3.35 compares the G_{max} of new type DTC with others circuit structure.

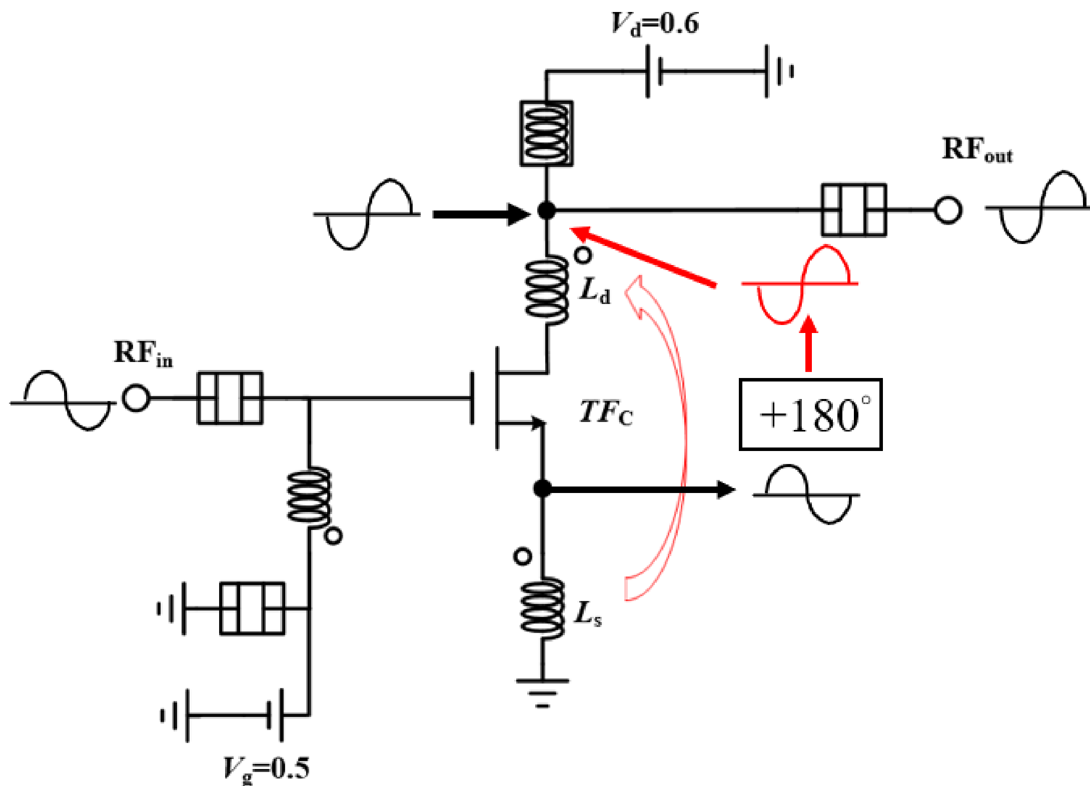

Fig. 3.23. The signal path analysis of the TF_C couple.

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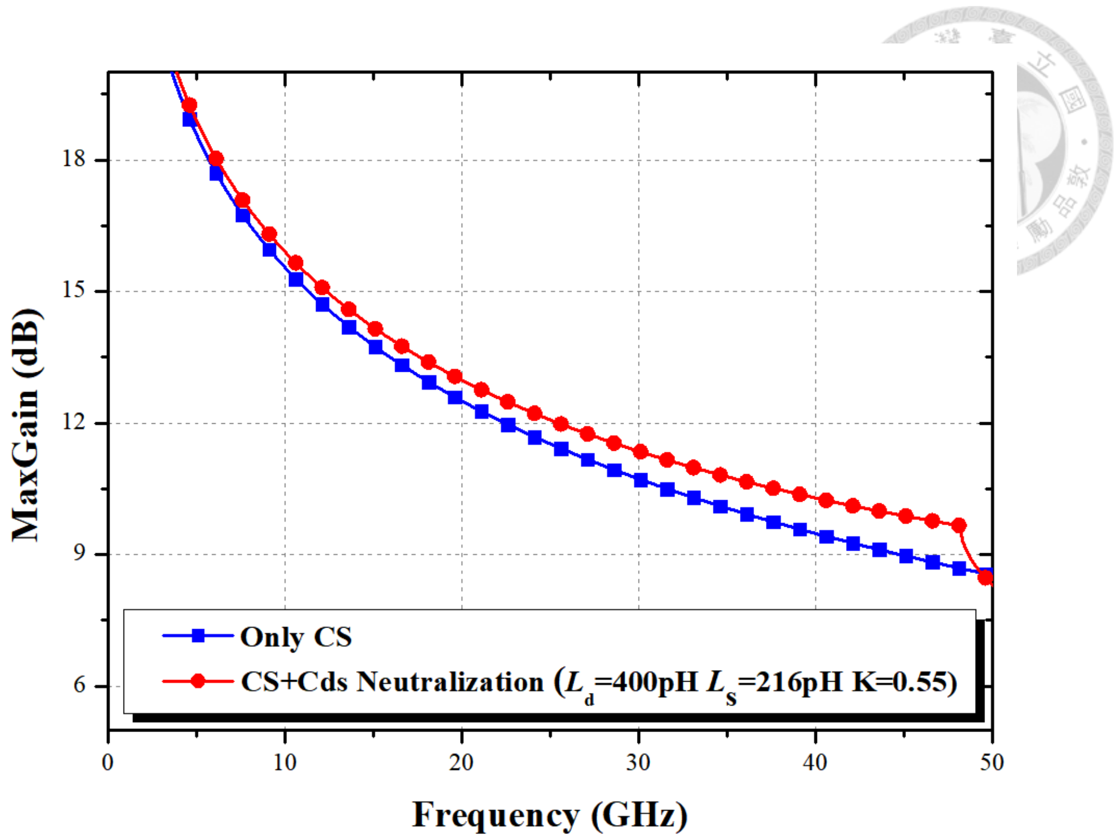

Fig. 3.24. The simulation results of new type DTC with and without TF_C.

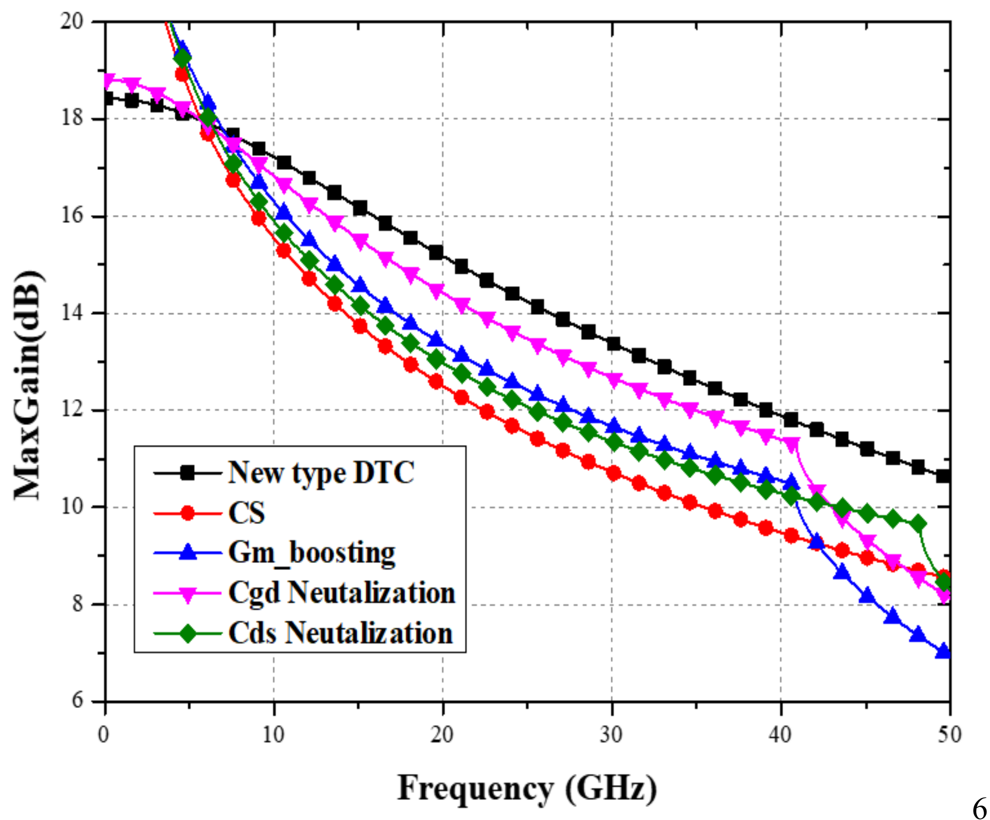

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Fig. 3.25. The simulated result of different topology.

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3.2.4 Complete K_a-band LNA Schematic

The proposed LNA is implemented in TSMC 90-nm CMOS process with ultra-thick metal (UTM), eight metal layers (M1 to M8) and metal-insulator-metal (MIM) capacitor. Fig. 3.26. shows the circuit schematic of the proposed K-band LNA which is composed of one cascode stage with current-reused technique and one common-source stages with new type of double-transformer-coupling. Source degeneration utilize in first-stage to let impedance of noise and input matching close. Moreover, LC tank is used for matching network. All capacitors are realized by using metals M5 to M9 as interdigital capacitors and MIM capacitors. The small-signal models and large-signal models of the 90-nm CMOS transistors are provided by TSMC. All of the passive components are simulated with Sonnet Software. Then, the post-layout simulations are simulated through Advanced Design Software (ADS).

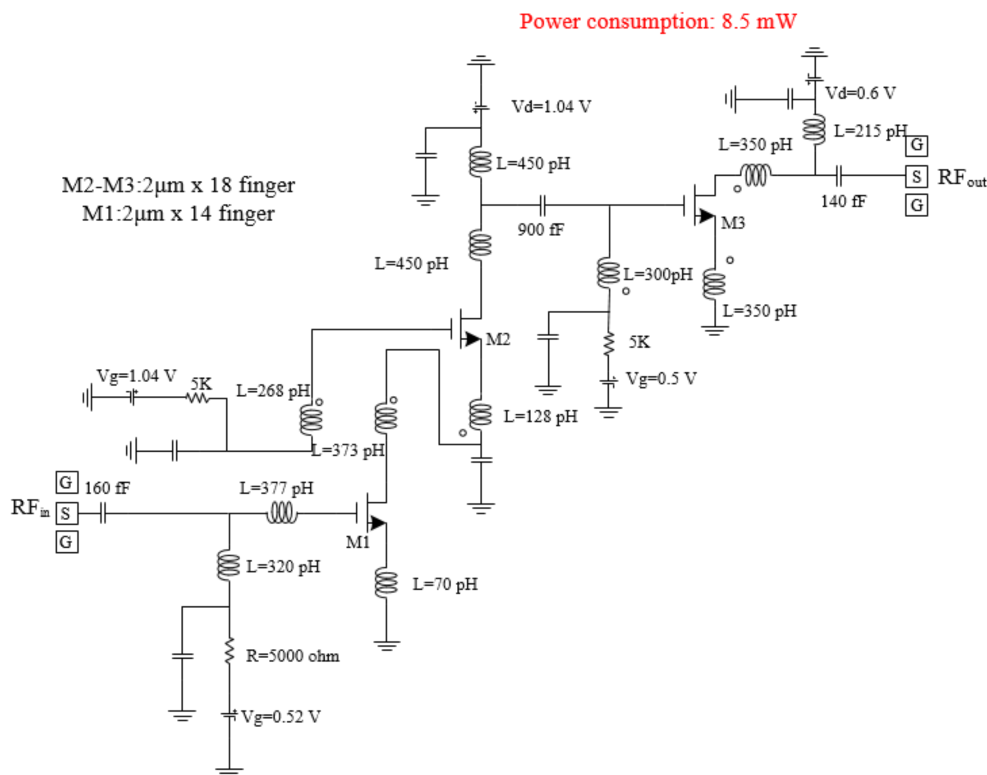

Fig. 3.26. Overall K_a-band LNA Schematic.

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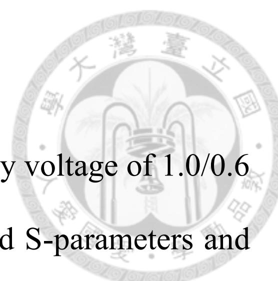
3.3 Simulation Result and Post-layout



The simulation is conducted under a bias condition with a supply voltage of 1.0/0.6 V, resulting in drain current of 4.4 mA for each stage. The simulated S-parameters and noise figure characteristics are presented in Fig. 3.27. and Fig. 3.28., respectively. The simulations reveal several key performance metrics. The peak gain reaches 19.7 dB at 28.3 GHz, while the noise figure achieves a minimum of 3.4 dB at 30 GHz, with an average noise figure of 3.8 dB. The LNA also demonstrates an 18.5-GHz 3-dB bandwidth spanning from 21.5 to 40 GHz. Additionally, both the input and output return losses exceed 5 dB across the entire 3-dB bandwidth.

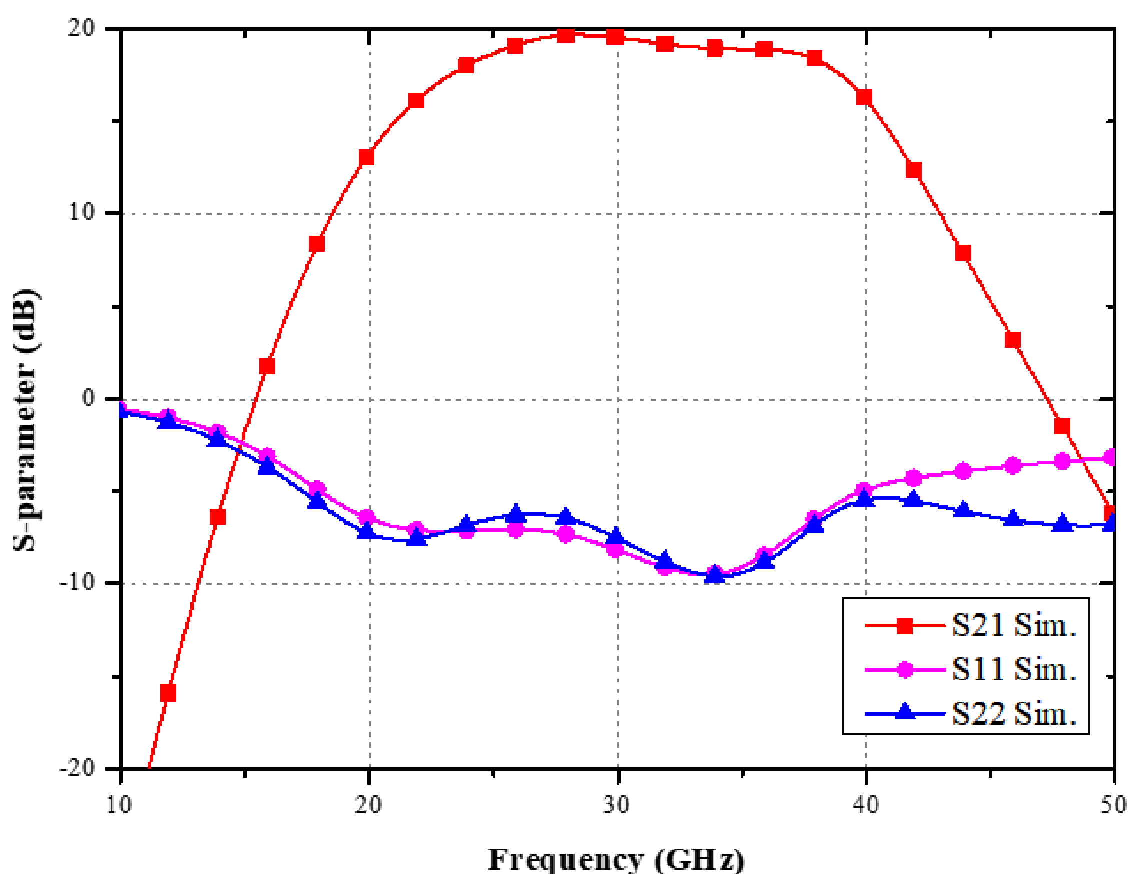


Fig. 3.27. Simulated *S*-parameters of the proposed K_a-band LNA.

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Fig. 3.29. delves into the loss distribution analysis of the proposed LNA. The cascode configuration in the first stage showcases approximately 20.4 dB for the maximum stable gain (MSG), whereas the output stage structure yields about 12.6 dB MSG. However, upon integrating the matching networks, the transistors tend to become stable. This leads to a degradation of about 4 dB in the MSG for the first stage and a 3 dB decrease for the second stage, excluding matching losses. The interstage matching loss is quantified at 2.5 dB, while the input matching loss and output matching loss are both 1.5 dB. Therefore, the simulation results show a peak gain of 20 dB at 30 GHz, which is within reason.

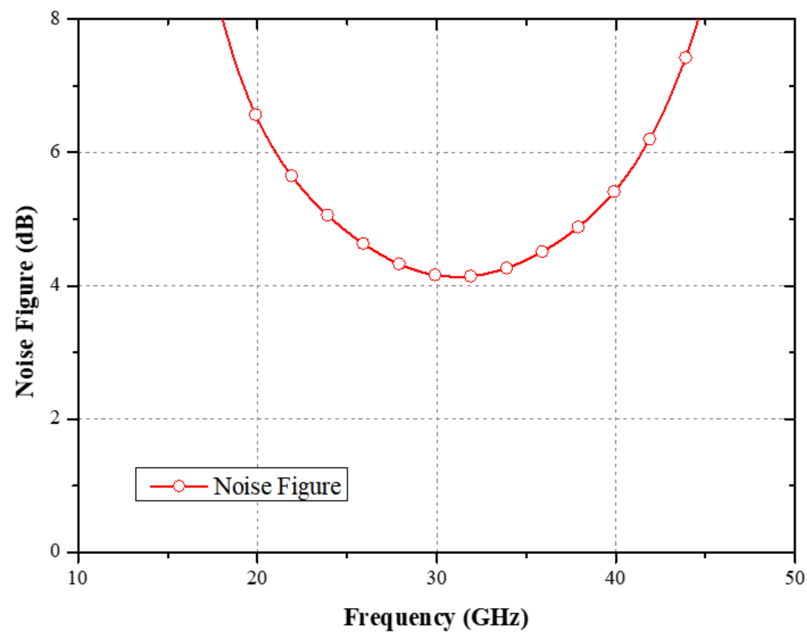

Fig. 3.28. Simulated noise figure of the proposed K_a-band LNA.

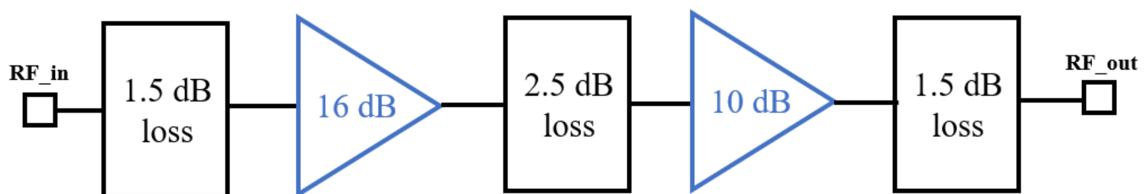

Fig. 3.29. Loss distribution of the proposed LNA.

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Fig. 3.30. shows the simulated results of large signal performances at 30 GHz including gain and output power. Seen from the simulations, the IP_{1dB} is -19 dBm, and OP_{1dB} is -0.6 dBm at 30 GHz. Fig. 3.31 shows the simulated result of drain current in versus input power. It shows the DC current tends to increase with higher input power levels. At an input power of -19 dBm (IP_{1dB}), the corresponding drain current is 11 mA, and total circuit power consumption is 11 mW.

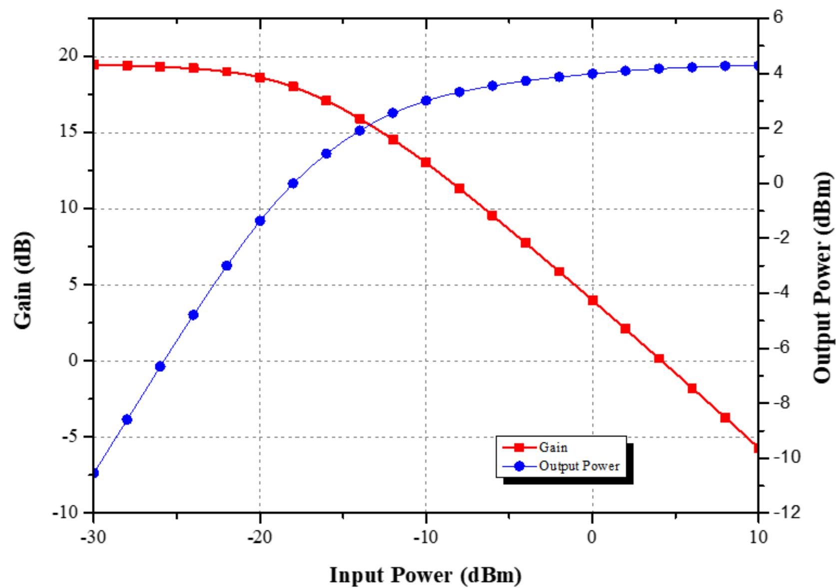

Fig. 3.30. Simulated large-signal performances of the proposed K_a-band LNA.

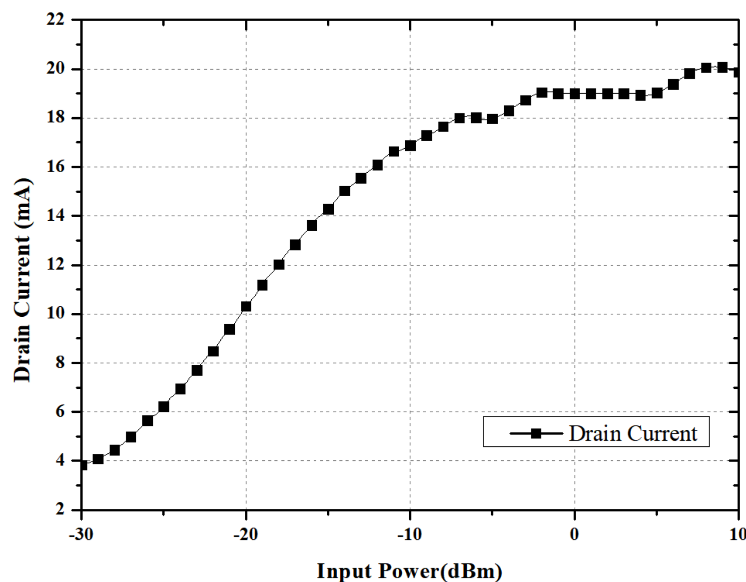

Fig. 3.31. The simulated result of drain current in versus input power.

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The layout of the K_a-band LNA is shown in Fig. 3.32. This LNA occupies a chip size of 0.595×0.87 mm^2 including all pads.

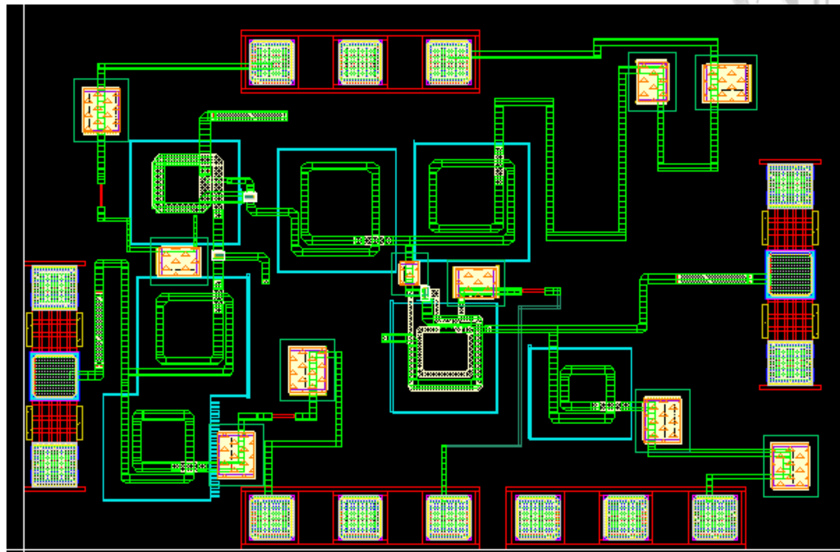

Fig. 3.32. Chip layout of the proposed K_a-band PA.

To prevent the occurrence of unwanted oscillations within the circuit, it is imperative to conduct stability assessments through simulations. Ensuring overall stability necessitates that the stability factor (K) remain greater than 1 for a two-port network. Fig. 3.33. shows the stability factor of the proposed LNA, demonstrating that this factor maintains a value greater than 1 across all frequencies. Moreover, attention is given to potential instability between stages. If the loop gain of the feedback path surpasses unity, the risk of oscillation arises. Fig. 3.34. depict stability mapping circles that illustrate potential interactions between stages. The results distinctly reveal the absence of intersections between these mapping circles. Consequently, the conducted stability tests can be deemed successful, and the design is verified as stable.

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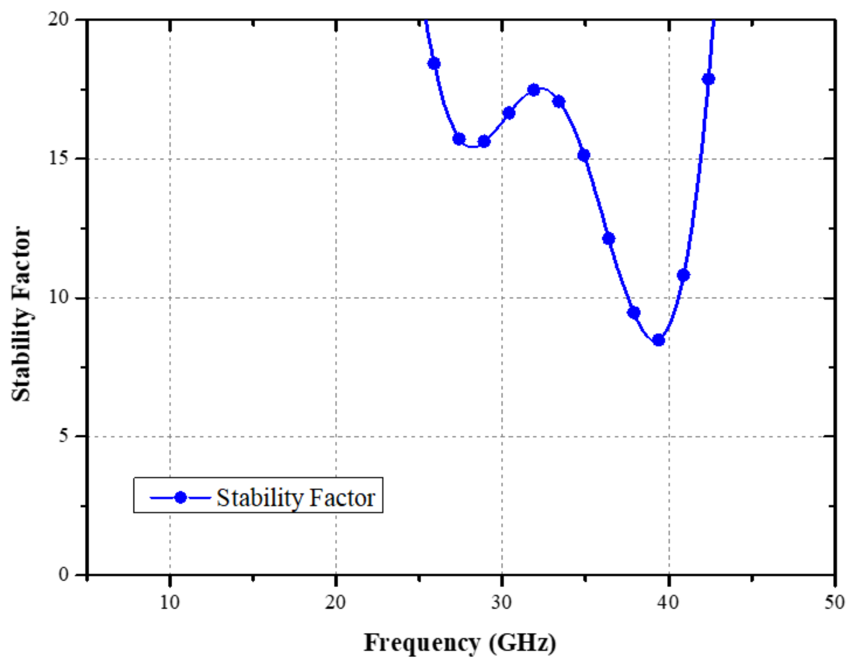

Fig. 3.33. Stability factor of the proposed LNA.

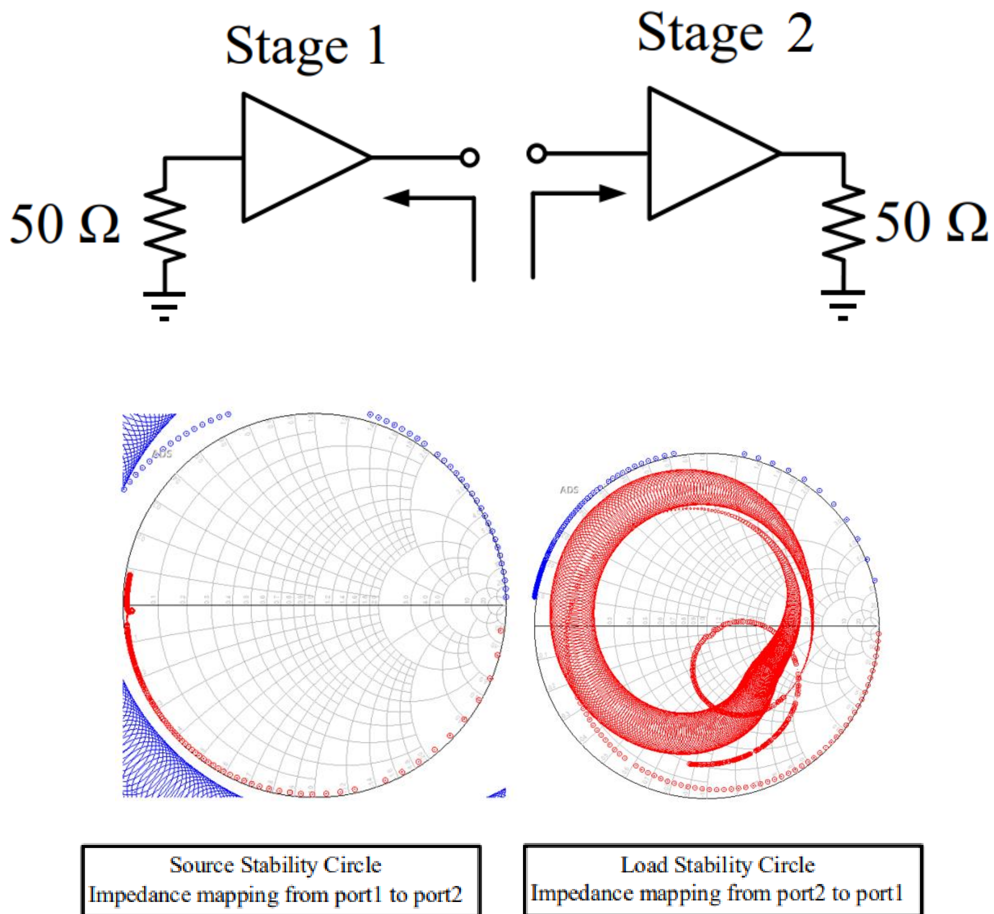

Fig. 3.34. The simulation of inter-stage stability mapping circles.

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3.4 Experimental Results

The chip size is 0.595 × 0.87 mm^2, including all pads. The chip photo of the proposed LNA is shown in Fig. 3.35. The circuit was measured via on-wafer probing. The S-parameters and noise figure are measured by Agilent E8361A PNA with input power of -25 dBm. The large-signal continuous-wave power sweep is measured through an E8267D signal generator and an Agilent E4448A spectrum analyzer.

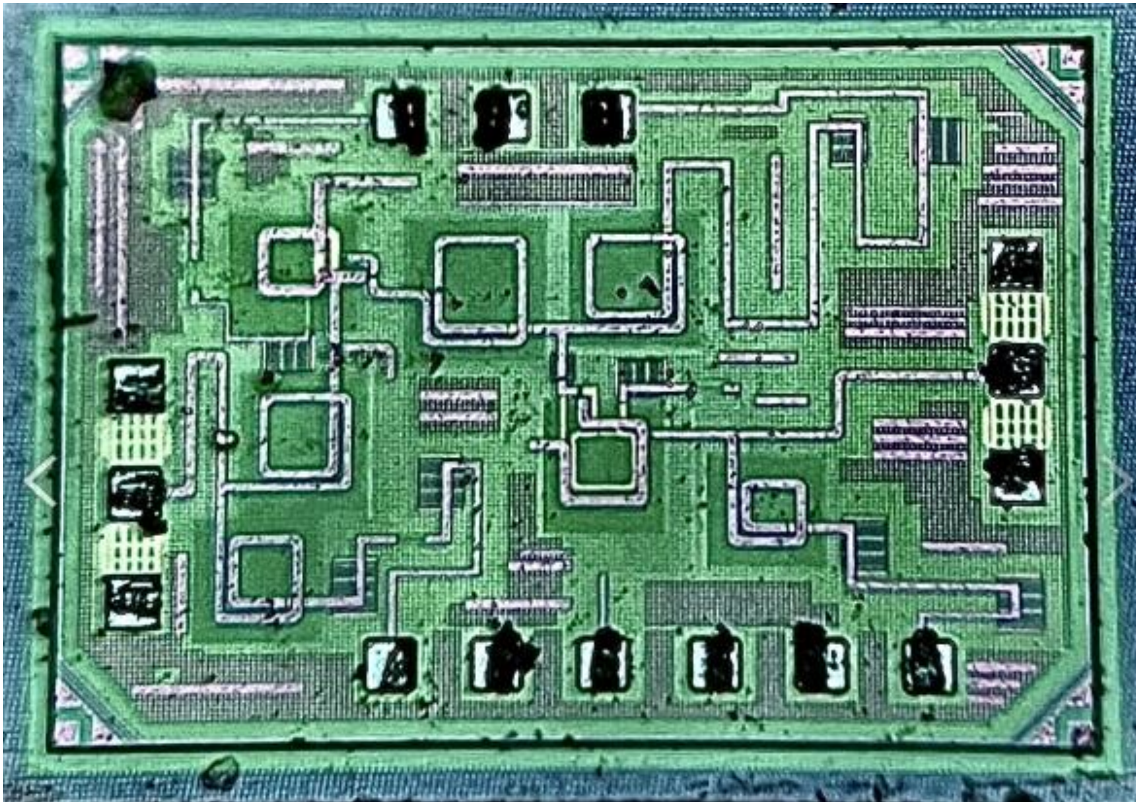

Fig. 3.35. The chip photo in 90-nm bulk CMOS process.

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Fig. 3.36 shows the measured and simulated S-parameters. The LNA achieves a 19.4-dB small signal gain at 24.6 GHz with 18.2-GHz 3-dB bandwidth (21.8-40 GHz), and the input/output return losses are both greater than 6.5 dB from 21.8-40 GHz. The simulated and measured noise figures are exhibited in Fig. 3.37. The lowest noise figure is 3.4 dB at 31 GHz and the average noise figure within the 3-dB bandwidth is 3.85 dB. The large-signal continuous-wave power sweep measurement is tested with the signal of 30 GHz. Fig. 3.38 exhibits the large-signal performances of the proposed LNA. The LNA achieves an IP_{1dB} of -19 dBm and an OP_{1dB} of 0.6 dBm at 30 GHz.

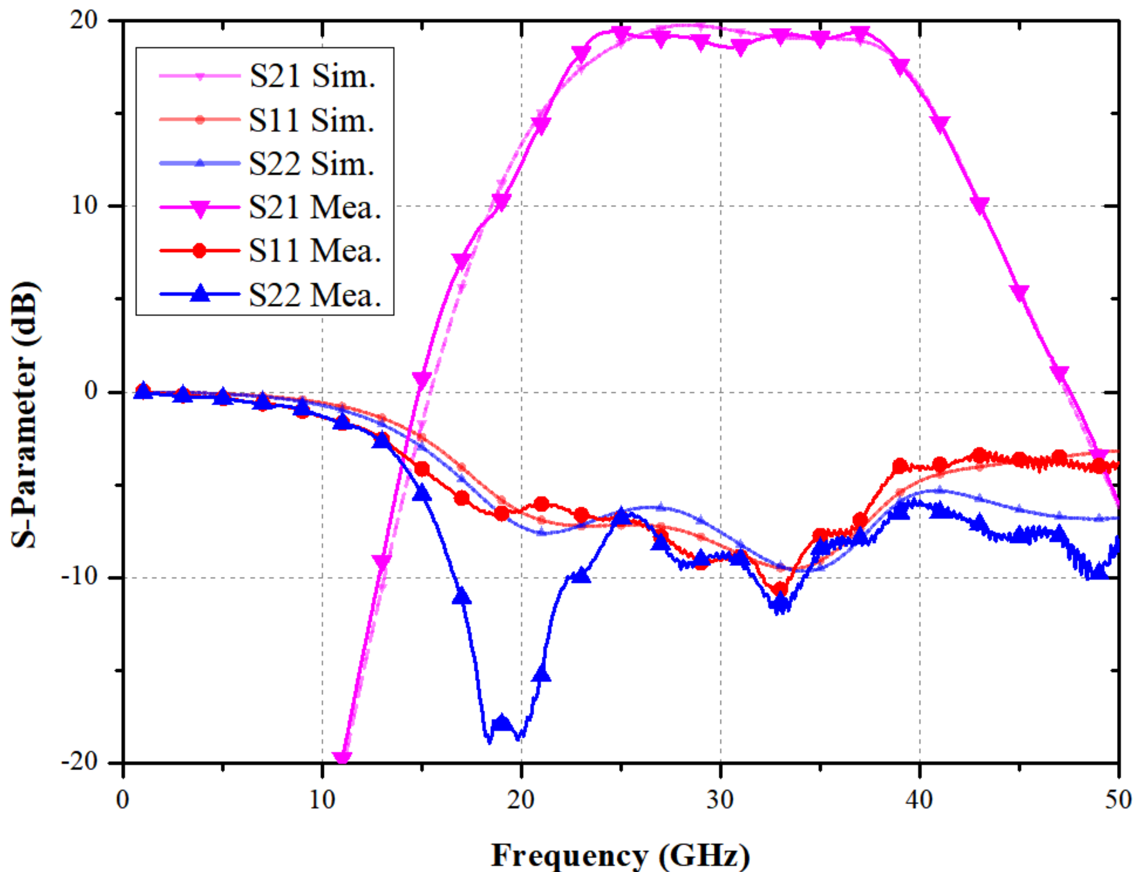

Fig. 3.36. Measured and simulated S-parameters of the proposed K_a-band LNA.

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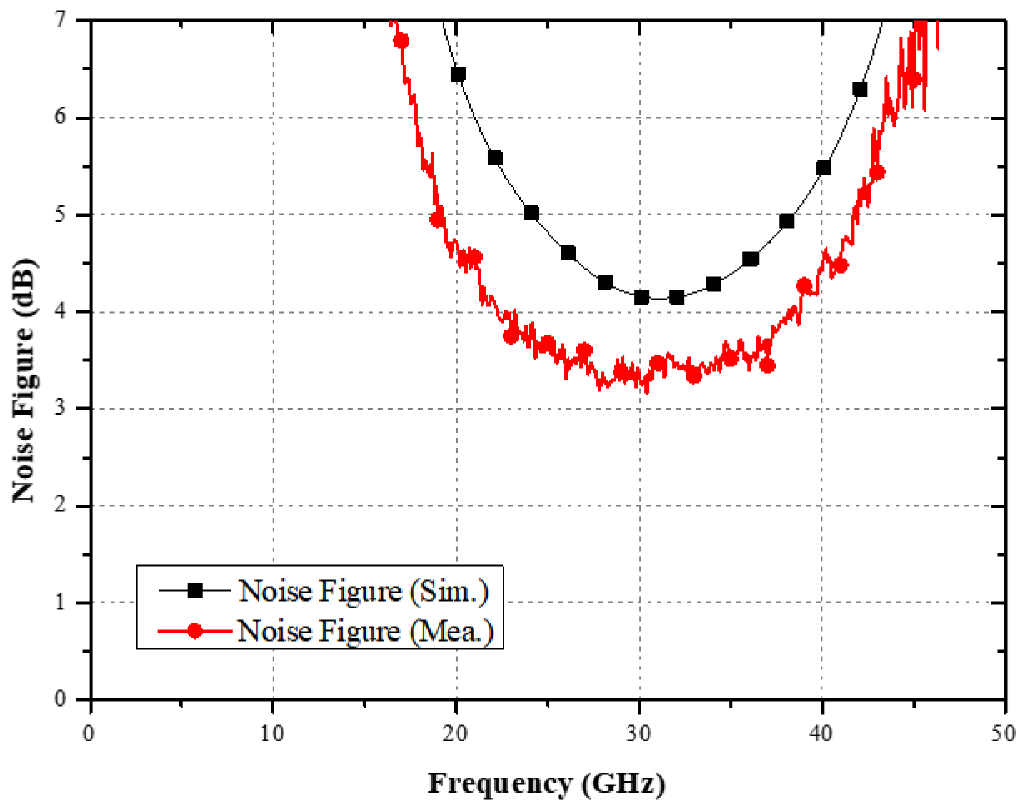

Fig. 3.37. Measured and simulated noise figure of the proposed K_a-band LNA.

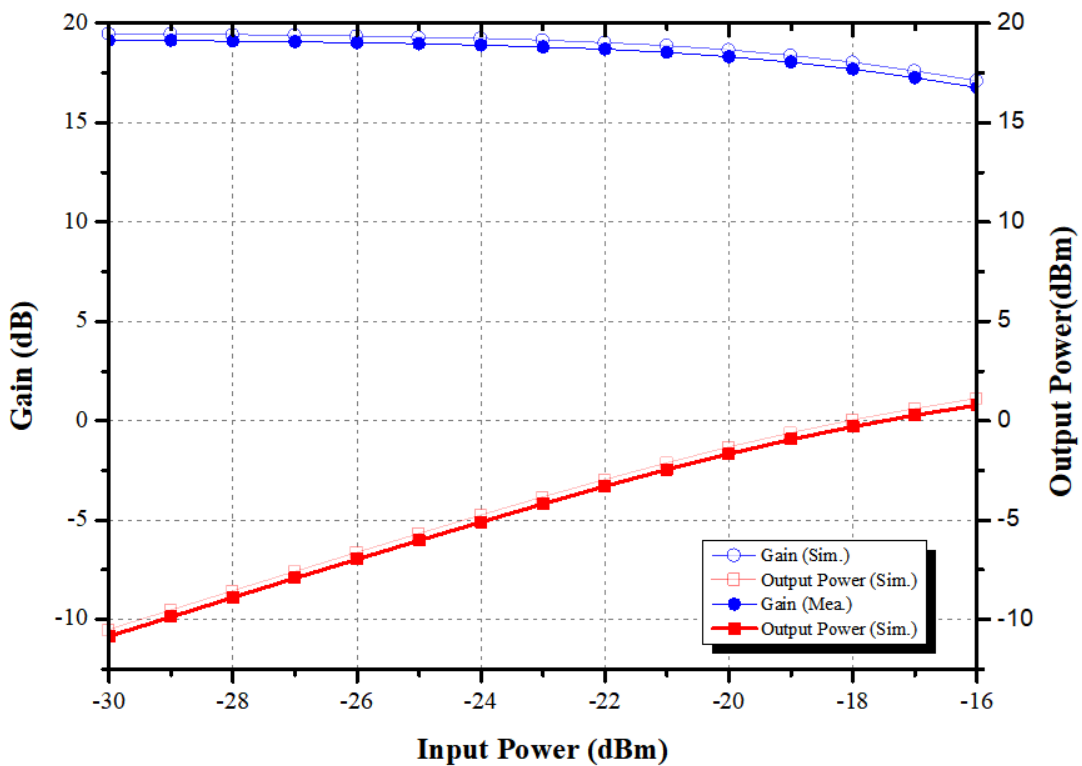

Fig. 3.38. Measured and simulated large signal performances of the proposed K_a-band LNA.

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When comparing the measured noise figure results with the simulated data, a clear trend emerges: the observed noise figure of the proposed K_a-band LNA in the measured results is notably approximately 1 dB lower than in the simulation. Therefore, try to use other simulation software to verify the accuracy of simulation. There are simulation results of single transistor (2-μm*14 fingers) *S*-parameter as shown in Fig. 3.39 to Fig. 3.42. The results demonstrate consistent outcomes in the *S*-parameter. However, there is a discrepancy in the noise figure simulation. The EDA (spectre) noise figure simulation has superior results compared to the ADS simulation, as depicted in Fig. 3.43. This is observed despite having the same $G_{\max}$ as in the ADS simulation, as shown in Fig. 3.41. Additionally, the other important parameters impact noise are noise resistance (Rn) and optimum complex reflection coefficient (Γ_{opt}). Fig. 3.45 shows the simulated Rn result of transistor size with 2-μm*14 finger. Fig. 3.46 shows the simulated Γ_{opt} result of transistor size with 2-μm*14 finger. According to the noise formula [61],

$$\mathrm{F} = \mathrm{F}_{min} + \frac{4r_n|}{Z_0}.\frac{|\Gamma_\mathrm{s} - \Gamma_\mathrm{opt}|^2}{\left|1+\Gamma_\mathrm{opt}\right|^2(1-|\Gamma_\mathrm{s}|^2)} \tag{3.9}$$

it is evident that the significantly higher Rn value in ADS will lead to a noticeable degradation in the simulated noise compared to simulations conducted on EDA.

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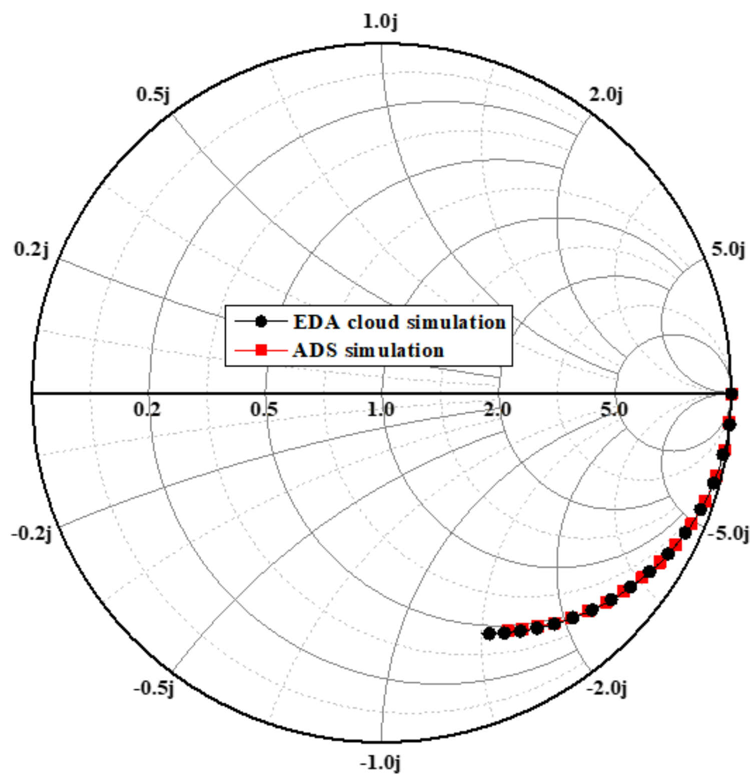

Fig. 3.39. The simulated S11 result of transistor size with 2-μm*14 finger.

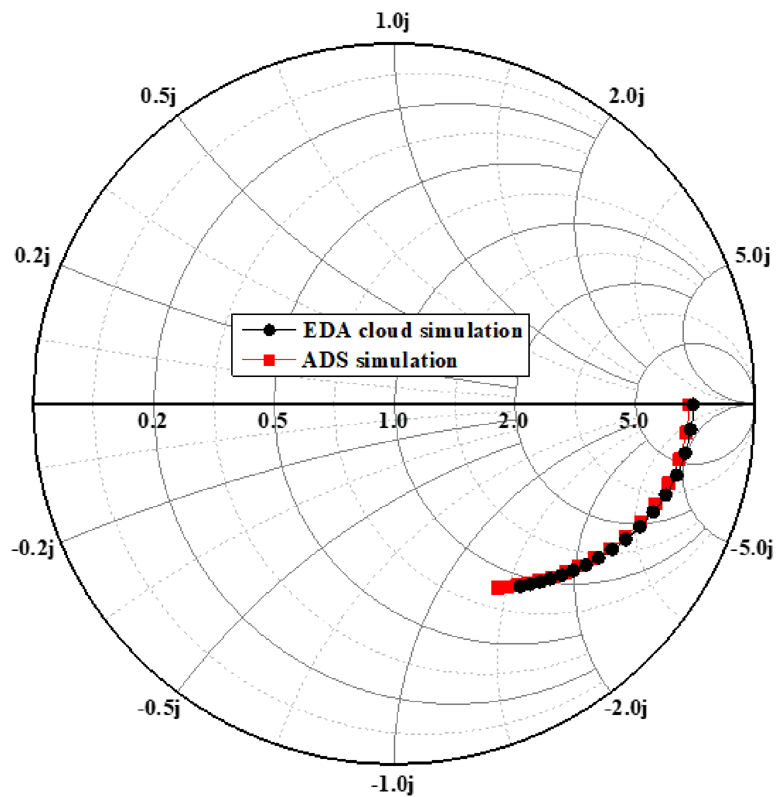

Fig. 3.40. The simulated S22 result of transistor size with 2-μm*14 finger.

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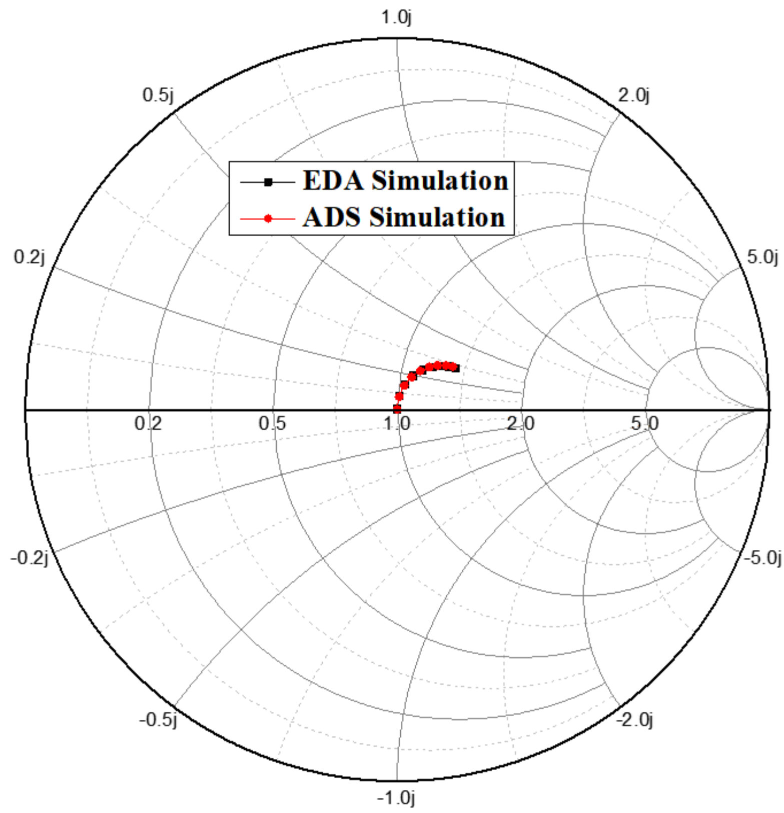

Fig. 3.41. The simulated S12 result of transistor size with 2-μm*14 finger.

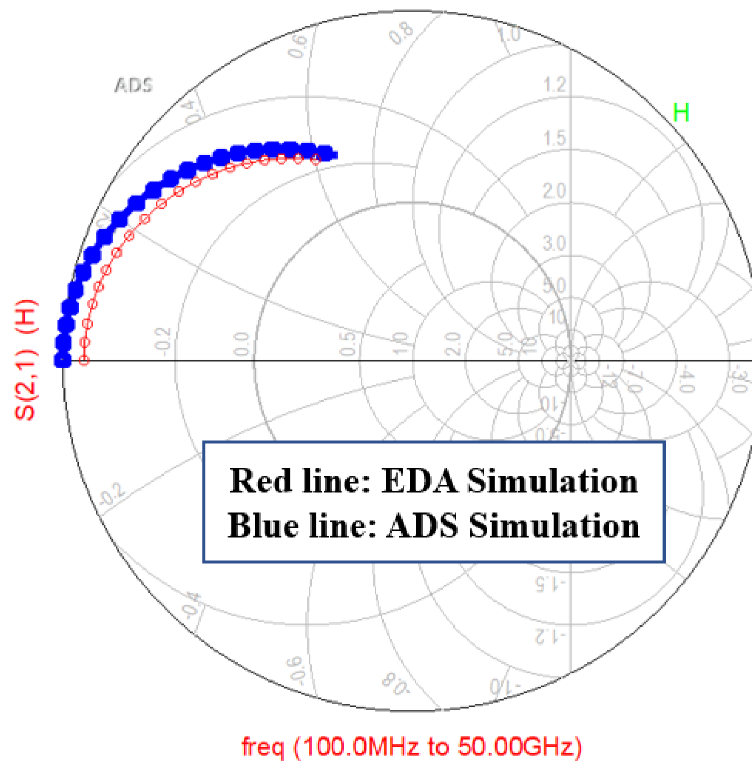

Fig. 3.42. The simulated S21 result of transistor size with 2-μm*14 finger.

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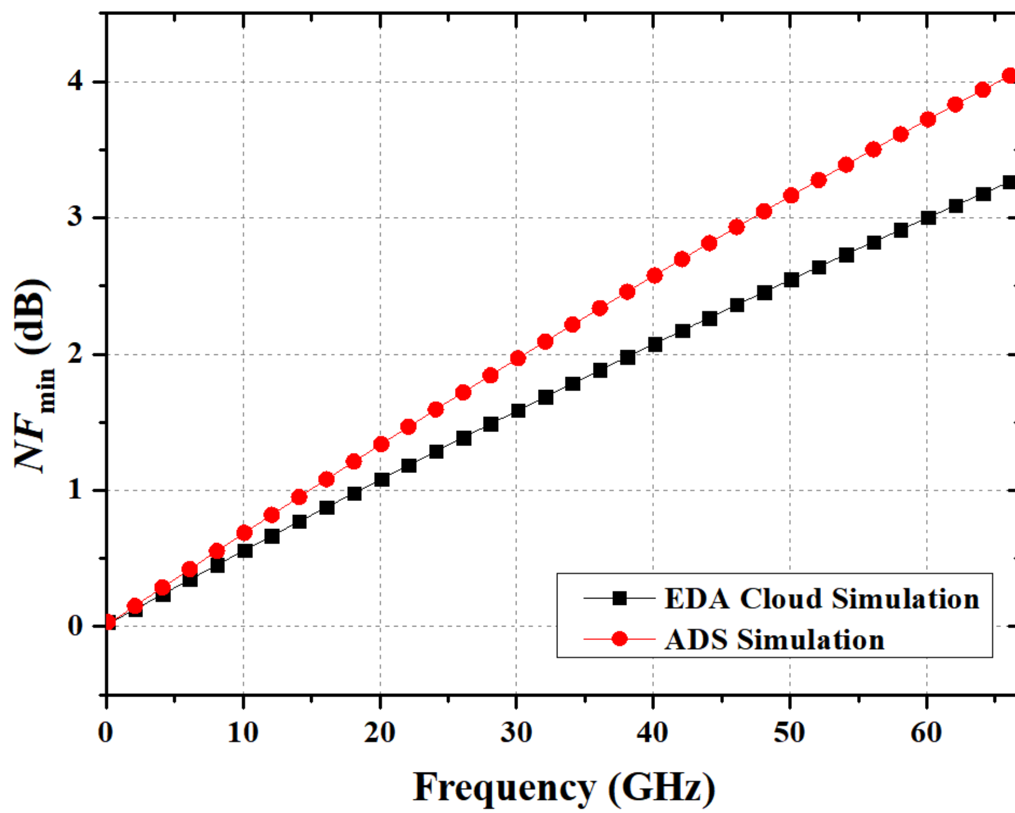

Fig. 3.43. The simulated noise figure results of transistor size with 2-μm*14 finger.

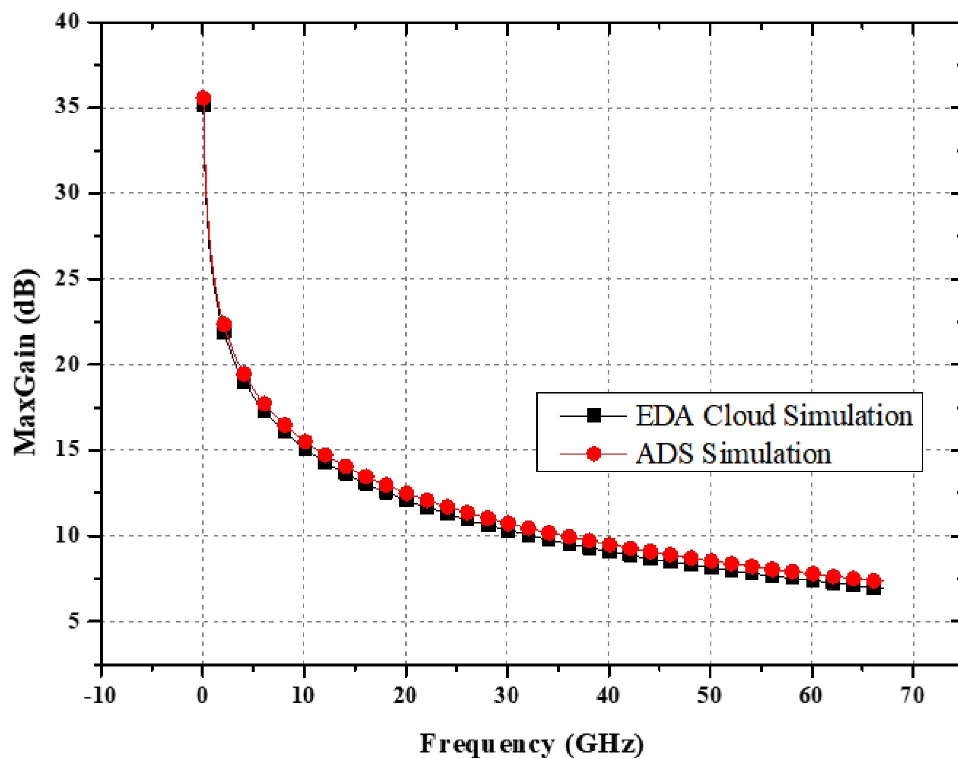

Fig. 3.44. The simulated G_{max} result of transistor size with 2-μm*14 finger.

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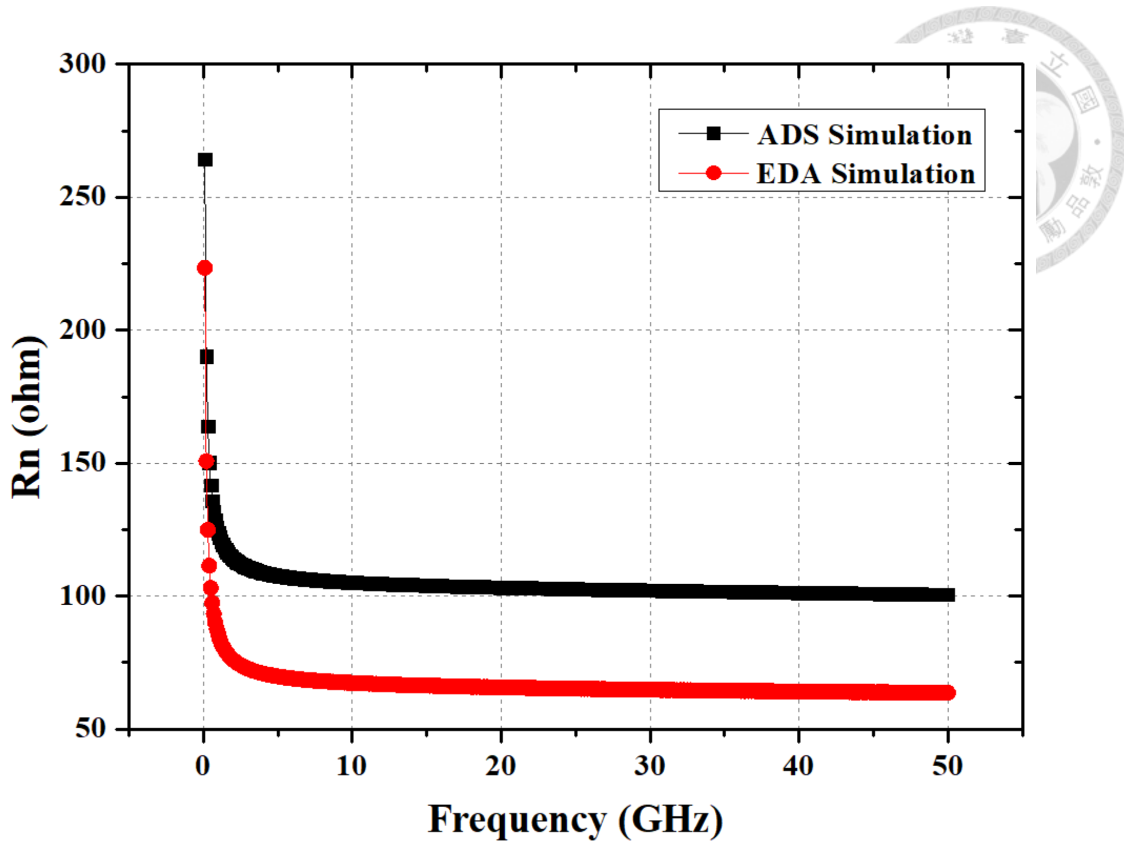

Fig. 3.45.. The simulated Rn result of transistor size with 2-µm*14 finger.

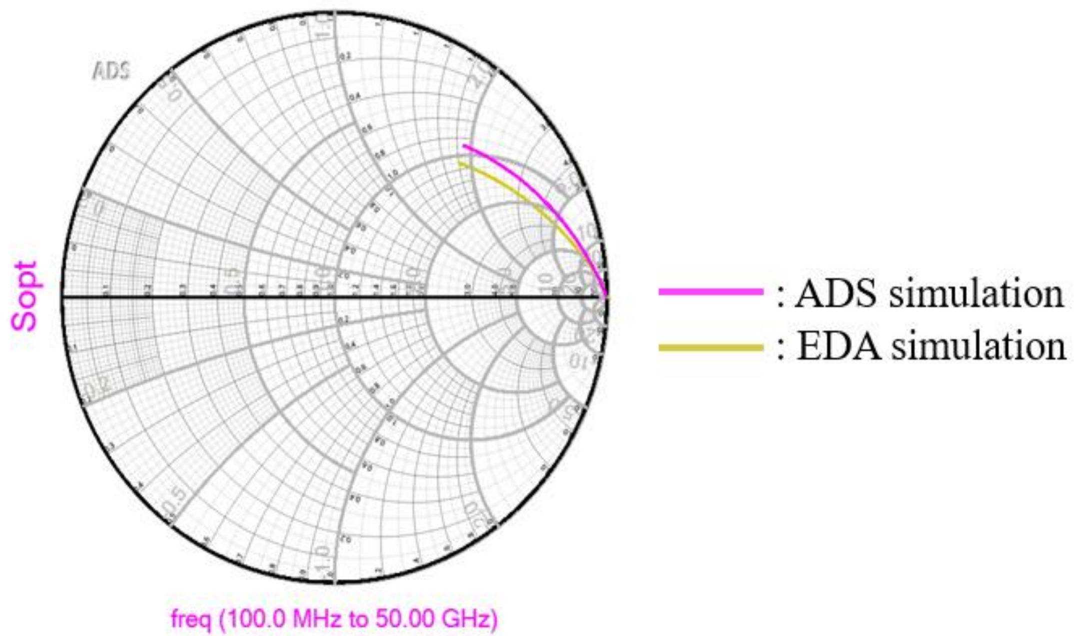

Fig. 3.46. The simulated Γ_{opt} result of transistor size with 2-µm*14 finger.

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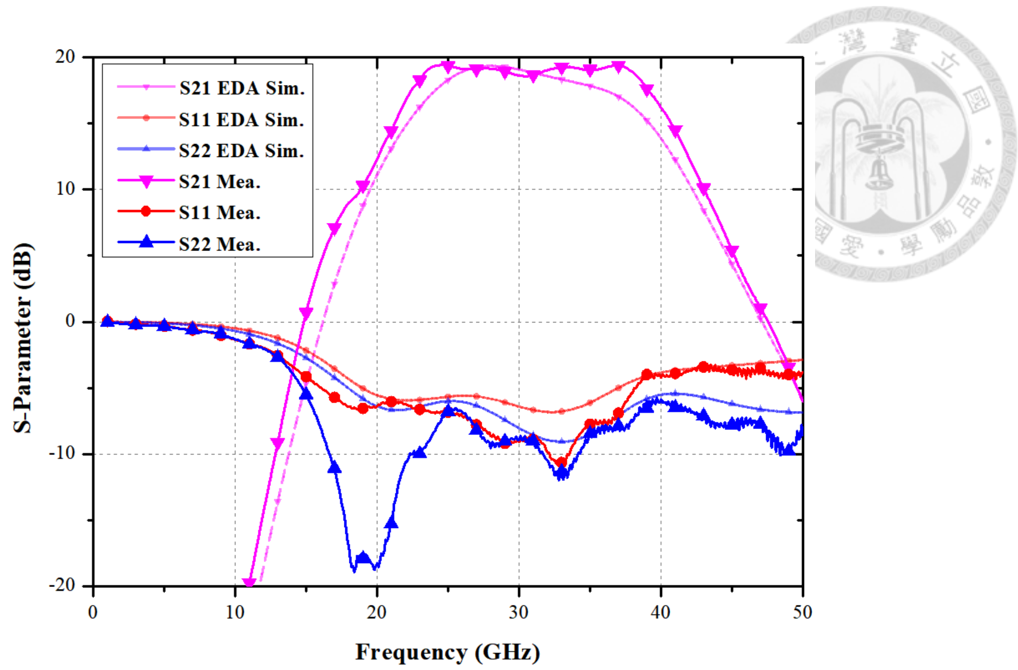

Fig. 3.47. Comparison of simulated in EDA and measured S-parameters for the Ka-band LNA.

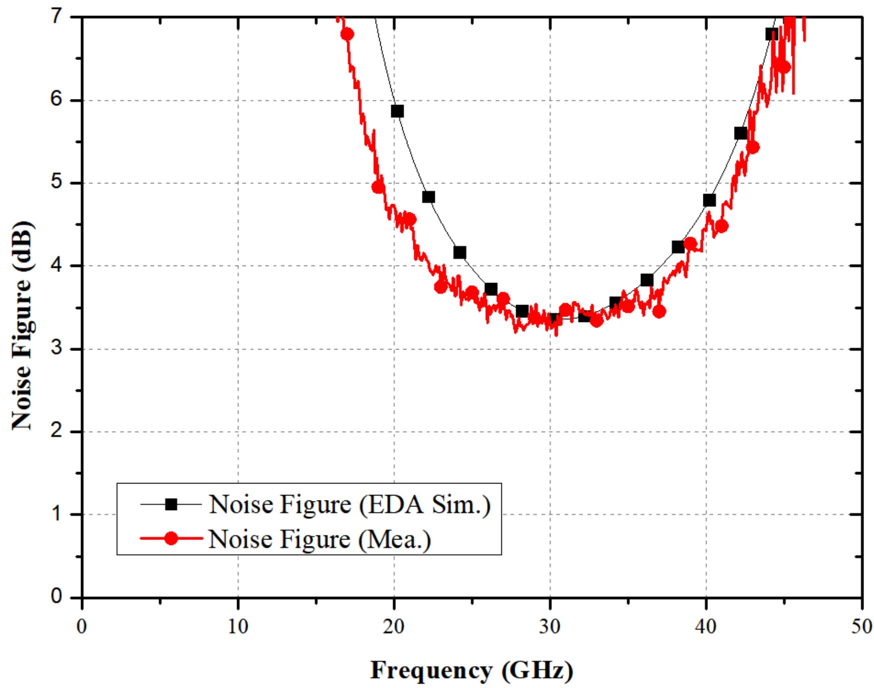

Fig. 3.48. Comparison of simulated in EDA and measured noise figure for the Ka-band LNA.

Fig. 3.47 and Fig. 3.48 show the simulation and measurement results of total circuit. In the S-parameter results, both simulations and measurement exhibit similarity, and the noise figure results also align between EDA simulations and measurement.

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3.5 Summary

A low-power wideband K_a-band LNA using 90-nm CMOS is presented. The current-reused double-transformer-coupling technique is employed at the first stage to achieve high gain and lower power consumption. The new type double-transformer-coupling structure is applied to enhance gain performance and neutralize the parasitic capacitance of transistor in second stage. The measured results agree well with the simulation. This LNA demonstrates high gain and low noise performance with low dc-power consumption and therefore shows the potential of CMOS LNAs for next generation radio astronomical applications. Table 3.4 summarizes the performance of published low-power Ka-band CMOS LNAs in recent years. The FOM_1 and FOM_2 are used to evaluate the performance of the low-power LNA, which are expressed as[47]

$$\mathrm{FOM}_1 = \frac{S_{21} \times Bandwidth\,[GHz]}{(NF_{\min} - 1) \times P_{\mathrm{DC}}\,[mW]} \tag{3.10}$$

and

$$\mathrm{FOM}_2 = \frac{S_{21} \times Bandwidth\,[GHz]}{(NF_{avg.} - 1) \times P_{\mathrm{DC}}\,[mW]} \tag{3.11}$$

where S21 is the peak small signal gain in magnitude, $NF_{\min}$ is the lowest noise figure in magnitude, and $NF_{avg.}$ is the average noise figure in magnitude. Compared with all the published LNAs, the proposed LNA shows the competitive FOM_1, which is 20.1 GHz/mW. The results of [32] exhibit the highest FOM1 of 22.6 GHz/mW due to their advanced CMOS technologies. With the FOM2 based on equation (3.9), the proposed Ka-band LNA features the high FOM_2, among all the previously reported low-power K_a-band CMOS LNAs, excluding these works using advanced CMOS SOI technologies.

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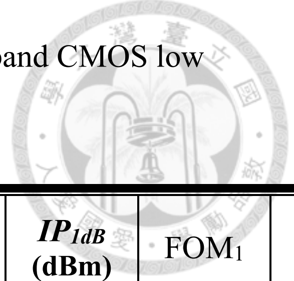

Table 3.4 Comparison of published state-of-the-art low-power K_a-band CMOS low noise amplifiers

Ref.	Process	RF freq. (GHz)	3-dB BW (GHz)	Peak Gain (dB)	NF (dB)	P_{dc} (mW)	IP_{1dB} (dBm)	FOM_1	FOM_2
[22]	0.18-μm CMOS	25	6	10.8	4.6	3.6	-12.5	3.1	N/A
[25]	0.18-μm CMOS	25	4	11	5.2	4.9	-16	1.3	N/A
[28]	65-nm CMOS	24.9-32.5	7.6	18.33	3.2-4.2	20.5	-24	2.8	2.3
[29]	90-nm CMOS LP	24-48	24	20	3.1	21.1	-26	10.9	N/A
[30]	65-nm CMOS	15.8-30.3	14.5	10.2	3.3-5.7	12.4	-16	3.3	2.1
[31]	40-nm CMOS	28	7.4	27.1	3.3-4.3	31.4	-21.6	4.7	3.8
[32]	22-nm FDSOI CMOS	22-32	10	18.6	2.1-2.9	5.6	-23	24.4	19.5
[33]	22-nm SOI CMOS	24-43	19	23	3.1-3.7	20.5	N/A	12.6	11
[34]	65-nm CMOS	21-41	20	28.5	2.7-3.2	32	-20	19.3	17.1
This work	90-nm CMOS	21.8-40	18.2	19.7	3.4-4.6	7.1*(11)	-19	20.1 *(13.5)	16.8 *(11.9)

*() :In condition of input power at IP_{1dB} (-19dBm)

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Chapter 4 W-Band Bidirectional PA-LNA in 65-nm CMOS Process for Beamformer Application

This chapter presents two bidirectional power amplifier-low noise amplifier (PA-LNA) in 65-nm CMOS process for millimeter-wave (mm-wave) multi-element phased-array front-end chip. Among the two PA-LNAs, one uses a switch to cutover PA/LNA mode, and the other PA-LAN uses a current-type transformer as a bidirectional matching network for PA and LNA input/output, without lossy T/R switch. As a switchless benefit, avoiding the use of the T/R switches not only saves the chip area but also alleviates performance degradation in PA and LNA modes. However, in the switchless version, since one channel in off-mode cannot provide an open impedance with sufficient bandwidth for another channel, the overall performance cannot reach a very wide frequency range. In the version with switch, because of the reason of using switch, it can achieve broadband performance. But with the loss of the switch, it also makes its output power lower, and has the disadvantage of larger noise. According to the experimental results, the proposed switchless PA-LNA achieves a peak small-signal gain of 18.6 dB in LNA mode and 17.2 dB in PA mode. In the PA mode, it achieves > 6.6-dBm saturated output power (P_{sat}), and > 3.2-dBm 1-dB output power (OP_{1dB}) in the range of 75 GHz to 90 GHz. While the LNA mode achieves a minimum noise figure (NF) of 7 dB at 81GHz and an average noise figure of 7.8 dB in a 3-dB bandwidth. In version with switch, it achieves a peak small-signal gain of 18.6 dB in LNA mode and 18.6 dB in PA mode. In the PA mode, it achieves > 7-dBm saturated output power (P_{sat}), and > 3.3-dBm 1-dB output power (OP_{1dB}) in the range of 32 GHz to 38 GHz. While the LNA mode achieves

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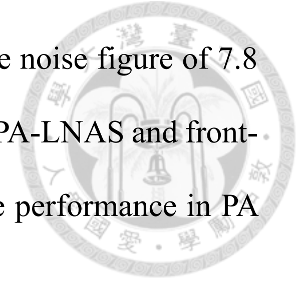

a minimum noise figure (NF_{min}) of 7.1 dB at 80 GHz and an average noise figure of 7.8 dB in a 3-dB bandwidth. Among all the published mm-wave CMOS PA-LNAS and front-ends, this PA-LNA shows comparable large-signal continuous-wave performance in PA mode and exceptional noise figure in LNA mode.

4.1 Phased-Array System[15]

Millimeter-wave phased-array systems find extensive application in satellite communications, close-range radars, and emerging next-generation (B5G/6G) technologies. Despite the advantage of the small mm-wave wavelength in minimizing antenna dimensions, the incorporation of distinct transmitting and receiving antennas on a single chip or board remains a costly endeavor, particularly when dealing with sizable phased-array setups. To address this challenge, a practical approach illustrated in Fig. 4.1 involves the utilization of a bidirectional transceiver. This innovative solution facilitates antenna sharing between transmitter and receiver, effectively halving the required number of antennas, and thereby offering a straightforward means to curtail overall system expenses. However, the chip size also needs to be considered as it shares the same antenna. The height of the chip cannot exceed λ/4. The wavelength at 80 GHz is approximately 3.74 mm. Hence, the height of the chip should not exceed 935 μm.

In the bidirectional phased-array system, the most critical part is the T/R front-end, which usually consists of a low-noise amplifier (LNA), power amplifier (PA) and using T/R switches with high isolation to prevent leakage signal problem in PA or LNA modes. However, the T/R front-end usually suffers from the insertion loss of switches, which deteriorates the noise performance in LNA mode and degrades the output power in PA mode. Besides, insufficient linearity of the switches will also compress the large-signal

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performance in PA mode. To resolve these issues, the switchless bidirectional amplifiers by directly connecting the PA and LNA inputs/outputs (as shown in Fig. 4.2.) have been proposed without adopting lossy T/R switches[15][35][36]. Nevertheless, switchless structure can reduce the loss causing by switch, but there is some defect in switchless version, it would present the design of PA-LNA with switch in Section 4.3 to discuss advantages and disadvantages of each version.

In this chapter, two W-band bidirectional PA-LNA fabricated in 65-nm bulk CMOS process are presented. The decision of the amplifier structure of the switchless PA-LNA circuit and the adoption of gain enhancement technique discussed. Besides, the description and flow chart for how the design trades were made for this PA-LNA are proposed. Finally, the comparison of with/without switch PA-LNA will presented in Section 4.4.

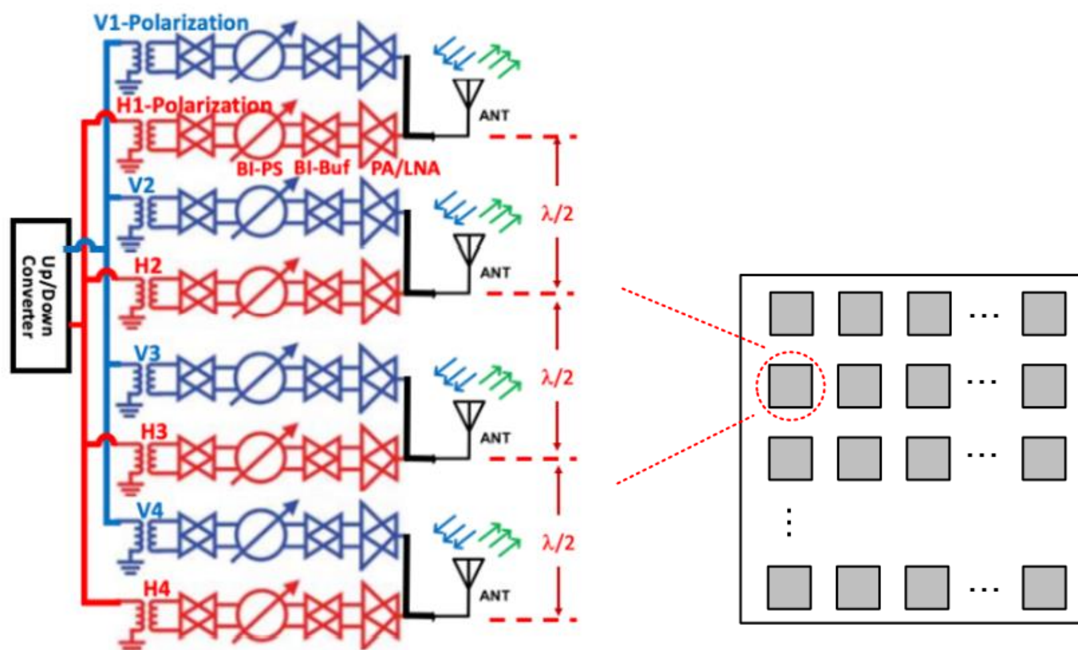

Fig. 4.1. Block diagram of a large-scaled bidirectional phased-array system.

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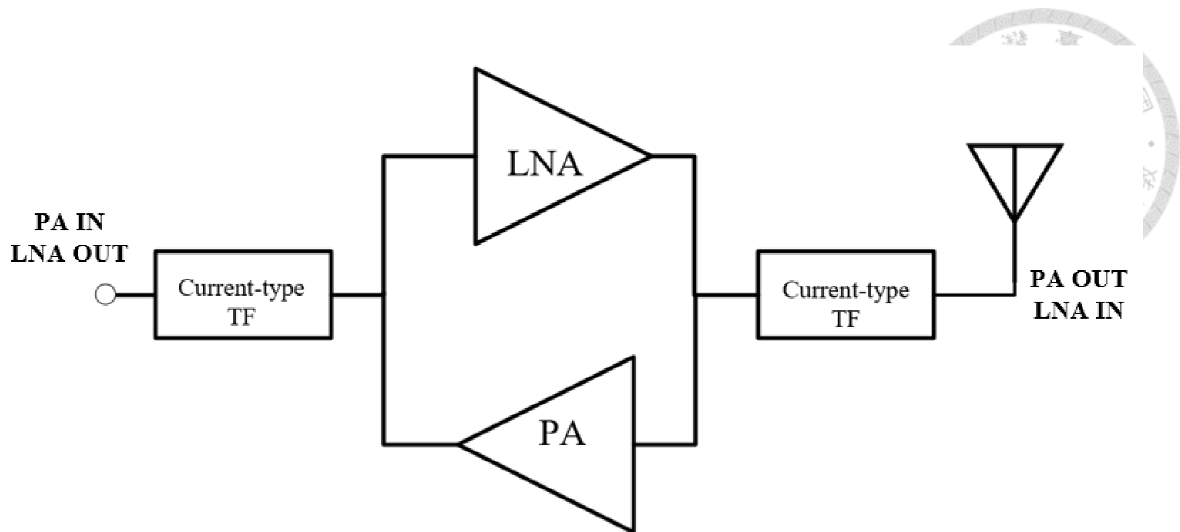

Fig. 4.2. Block diagram of a switchless bidirectional PA-LNA.

4.2 Design Concepts of PA-LNA

4.2.1 Amplifier Structure of PA-LNA cores

First and foremost, the blueprint of the amplifier architecture requires verification before embarking on the determination of suitable components for the matching network. The distributed amplifier (as depicted in Fig. 4.3.) stands as a widely favored configuration for devising broadband amplifiers endowed with bidirectional capabilities [12]. However, owing to the inherent structure of the distributed amplifier, it employs numerous gain cells to construct artificial transmission lines. While this approach facilitates its functionality, it comes at the cost of consuming substantial chip area and a notable power budget. Fig. 4.4 illustrates the application of a single-ended cascode amplifier topology in PA-LNA designs. In comparison to differential amplifiers, single-ended configurations typically grapple with issues concerning stability and linearity. Furthermore, the single-ended amplifier structure often necessitates the incorporation of multiple amplifier stages to achieve adequate gain while maintaining an acceptable 3-dB bandwidth in the mm-wave frequency band.

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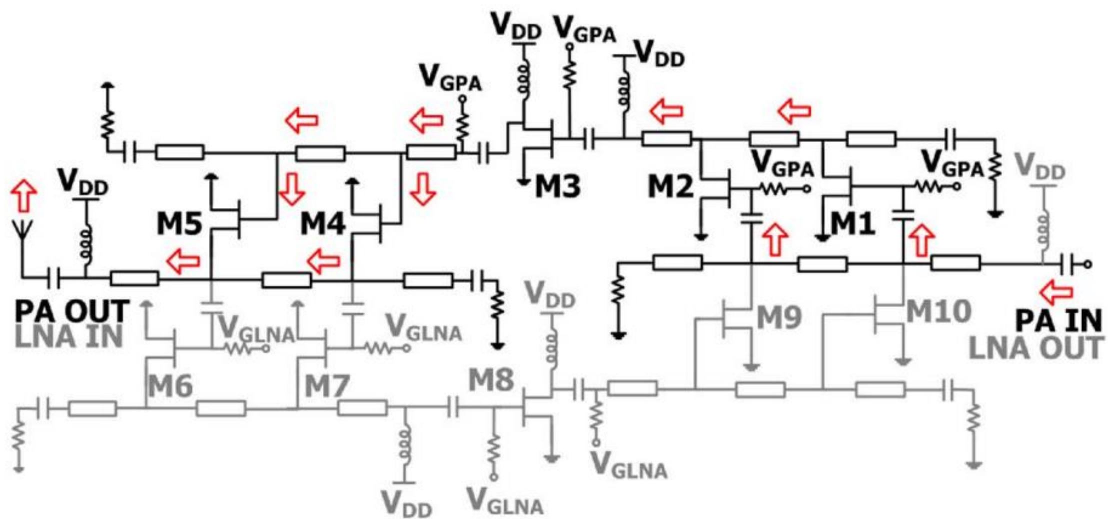

Fig. 4.3. The switchless bidirectional PA-LNA using distributed amplifier topology[12]

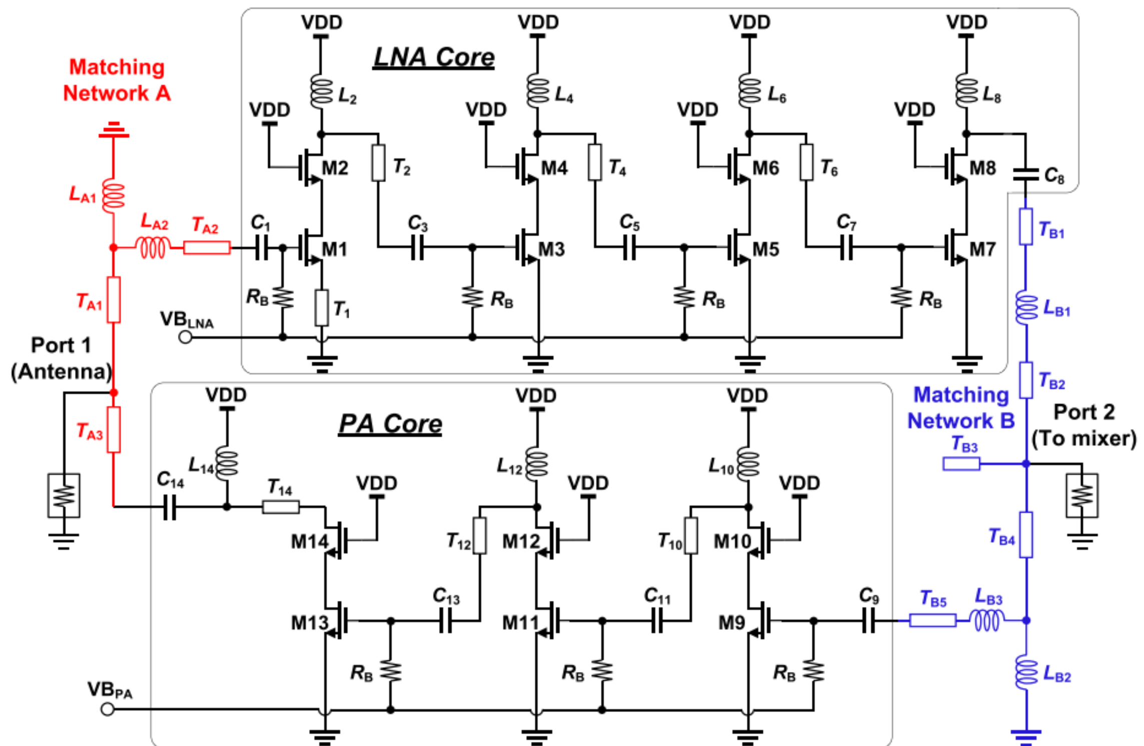

Fig. 4.4. The switchless bidirectional PA-LNA using single-ended cascode amplifier topology[13]

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This implies that a larger chip area is necessary for the matching network, and greater DC power dissipation is required for the proper operation of the transistor. Although utilizing the cascode topology in a single-ended amplifier can enhance gain and isolation, it becomes challenging to achieve impedance matching between circuits of different stages due to the elevated output impedance inherent in the cascode configuration. Given these factors, it can be deduced that the architectures of both the distributed amplifier and single-ended amplifier are unsuitable for PA-LNA designs intended for multi-element phased-array systems.

In light of these considerations, a three-stage differential common-source (CS) amplifier is employed for the PA-LNA design, as illustrated in Figure 3.5. This amplifier offers several advantages: 1) A three-stage differential amplifier can provide ample small-signal gain within the mm-wave frequency range.2) The common-mode rejection property of the differential CS stage ensures ideal direct conduction and AC isolation between the two stages. 3)Implementing capacitive neutralization techniques can be easily accomplished to enhance gain and improve circuit stability. 4)A transformer matching network can be employed to achieve a compact chip area. 5)The differential circuit exhibits suppression of even-order harmonics.[15]

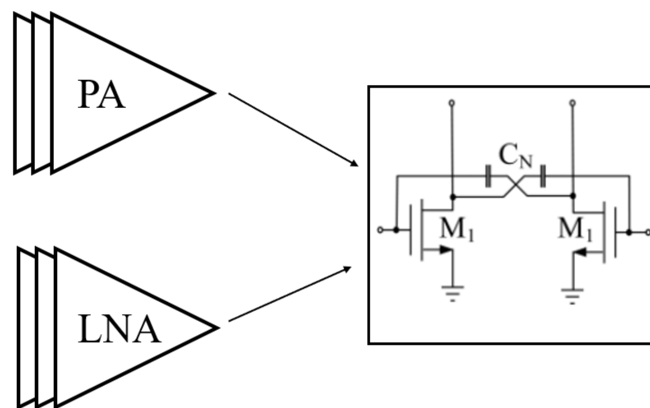

Fig. 4.5. The PA/LNA structure for the proposed PA-LNA

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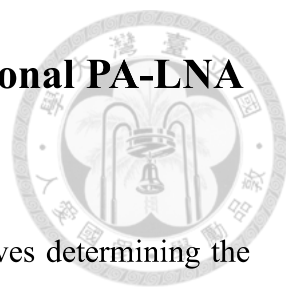

4.3 Design Procedure of the W-Band Bidirectional PA-LNA

4.3.1 Bidirectional Matching Network

Once the amplifier structure is established, the next step involves determining the appropriate matching network. In this work, considering that both the PA and LNA cores consist of three-stage differential common-source amplifiers, the transformer-based matching network depicted in Figure 3.6 can be employed. This choice enables phase conversion, efficient impedance matching, and exceptional DC isolation within the design.

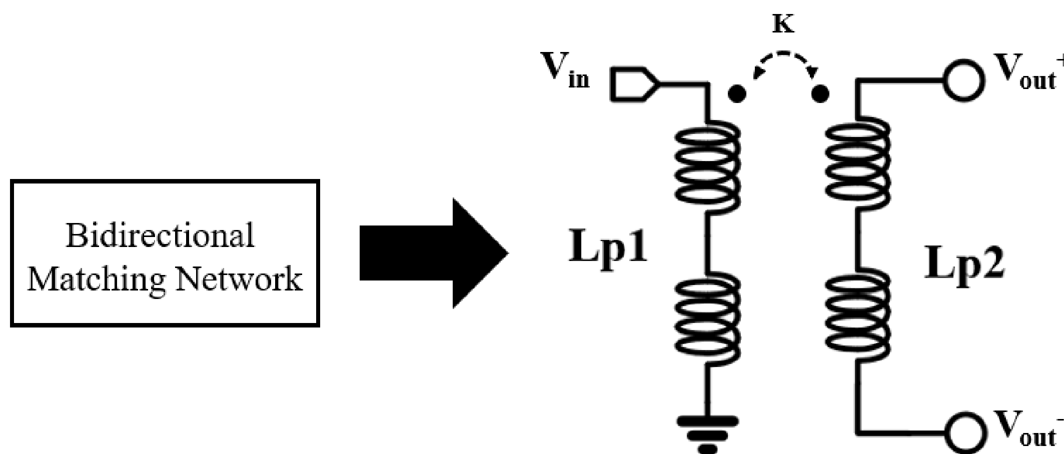

Fig. 4.6. The ideal single to differential transformer model in the proposed PA-LNA design

In addition, the transformer can provide high impedance transformer ratio with low insertion loss. The transformer has two coupling methods which are edge coupling and broadside coupling. The edge coupling places the primary and secondary inductors in the same metal layer, while the broadside coupling places them in two different metal layers. The coupling method effects the maximum coupling coefficient based on the limitation of the DRC rules.

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4.3.2 PA-LNA Design Flows

Fig. 4.7 depicts the circuit concept employed in the design of this bidirectional PA-LNA circuit. Here, a transformer-based topology serves as a compact matching network, and a three-stage differential common-source amplifier with neutralization capacitors, is embraced for both the PA and LNA cores. In PA mode, the PA core is activated by configuring the gate and drain bias voltages according to the designed value. Conversely, the LNA core is deactivated through the adjustment of gate and drain bias voltages, effectively preventing the potential risk of positive feedback and subsequent oscillation issues. Similarly, in LNA mode, the working principle is reversed. The LNA core is engaged, while the PA core is closed by turning off the gate and drain bias voltages.

The important specifications in this switchless bidirectional PA-LNA design center around the PA's output power and the LNA's noise performance. Consequently, carefully design is given to the PA output network and the LNA input network.

In the millimeter-wave frequencies, the off-state input and output impedances of both the PA and LNA are not ideally open due to inherent parasitic capacitances. This phenomenon can result in signal leakage issues, where signals inadvertently traverse from the PA to LNA path or LNA to PA, as illustrated in Fig. 4.8. Hence, preventing such signal leakage in a switchless bidirectional PA-LNA configuration poses a challenge. Moreover, a further challenge arises when the PA output port and the LNA input port are interconnected. This connection complicates the task of achieving optimal power matching in PA mode and desirable noise matching in LNA mode.

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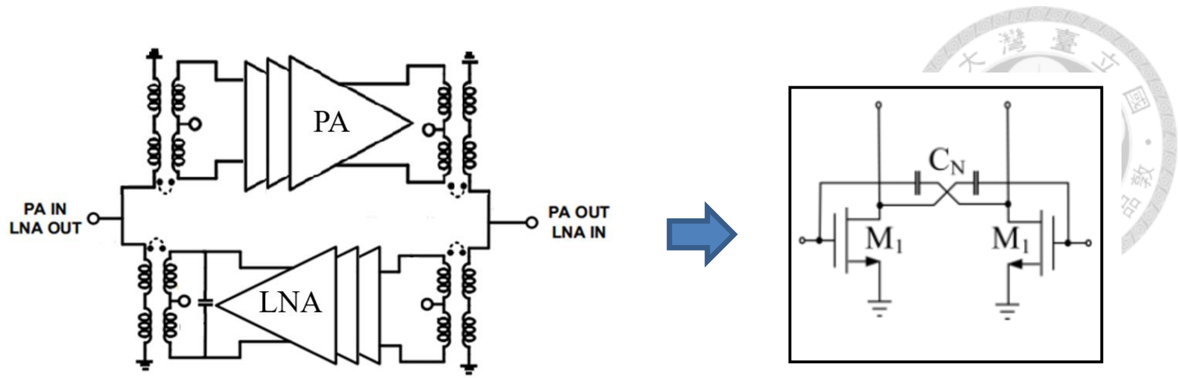

Fig. 4.7. The circuit concept of the proposed PA-LNA.

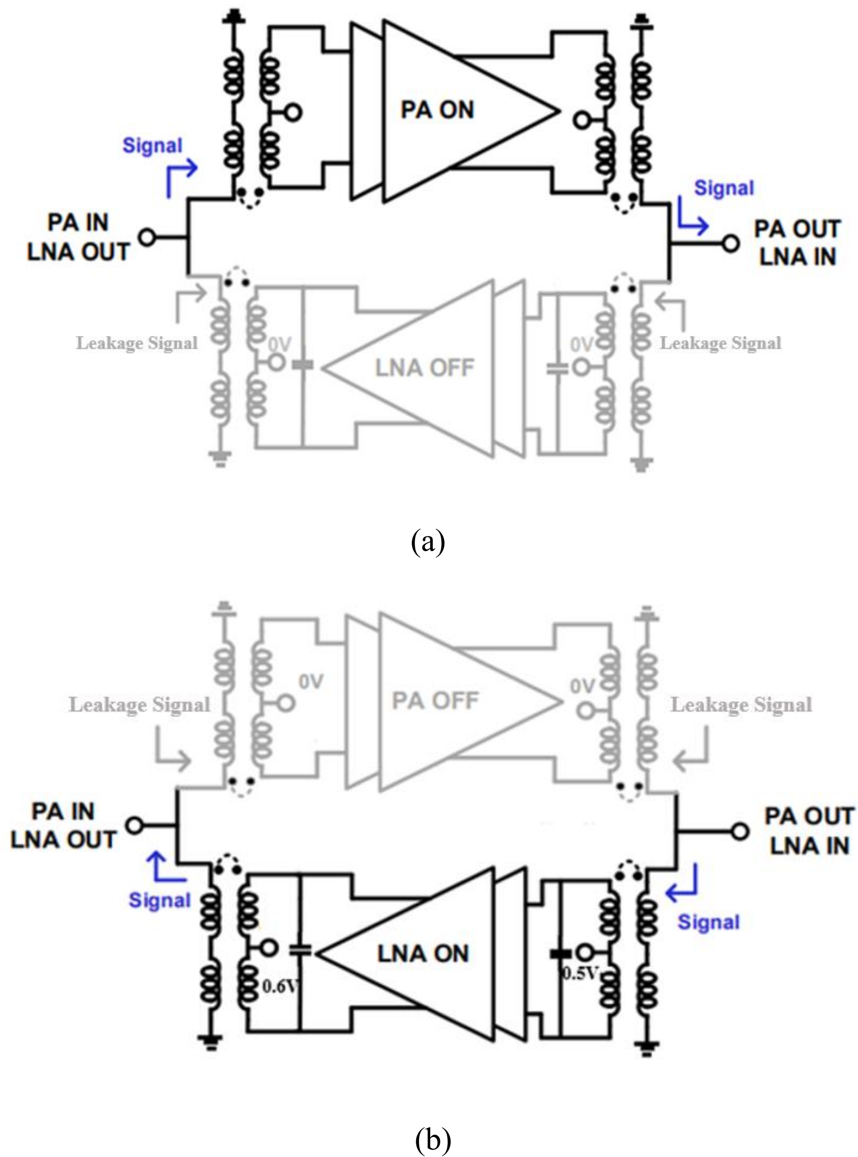

Fig. 4.8. The signal leakage problem in switchless bidirectional PA-LNA. (a) PA mode (b) LNA mode

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To face the challenges inherent in PA-LNA design, a systematic approach is proposed as illustrated in Fig. 4.9. The process commences by ensuring the simultaneous achievement of power matching in PA mode and noise matching in LNA mode. In essence, the initial phase involves optimizing the design of individual PA and LNA units.

Subsequently, attention is directed toward addressing signal leakage and mitigating loading effect concerns. This entails verifying whether the off-state impedance of both the PA and LNA sufficiently meets requirements. To effectuate the conversion from low impedance to high impedance, a transformer is employed. If the impedance fails to reach the desired level, it becomes imperative to re-select transistor size and re-optimize the amplifier transformer design. Finally, the PA input and output, as well as the LNA output and input, are interconnected, necessitating the optimization of the matching network. By using this comprehensive design process, the complexities inherent in PA-LNA design can be effectively reduced.

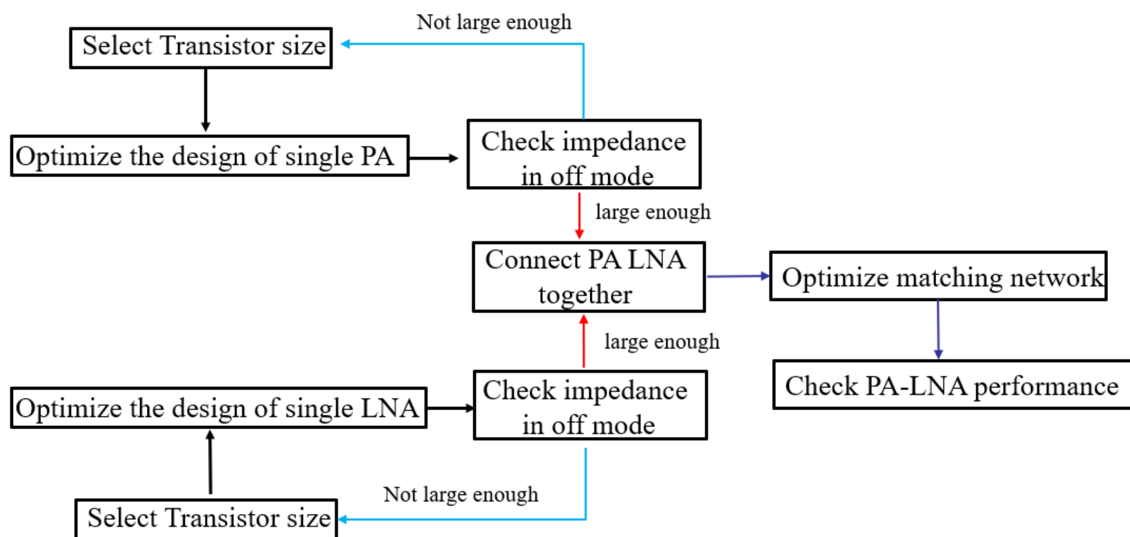

Fig. 4.9. The design flow for switchless bidirectional PA-LNA

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4.3.3 Block Diagram of PA

Before designing the PA part of PA-LNA, the design goals should be decided first. Due to the high antenna gain of mm-wave multi-element phased-array communication systems, each element does not need high output power to deliver the signal. The block diagram and initial power budget of this PA are shown in Fig. 4.10. Considering the feasibility of the circuit, the loss caused by the PA-LNA loading effect, and the published literature[48]-[50], a saturated output power of 10 dBm and a PAE of 10% were determined as targets.

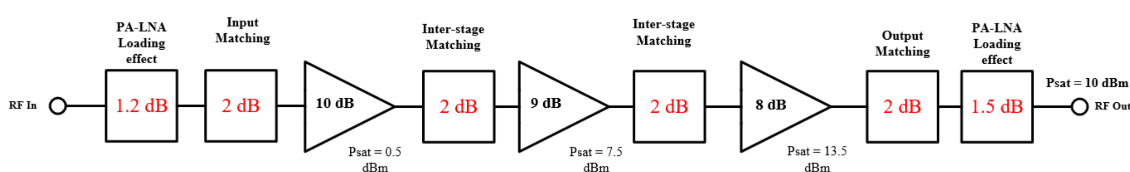

Fig. 4.10. The power budge of the PA

4.3.4 Device and Bias Selection

After establishing the design objectives and circuit architecture, the determination of device size becomes feasible. In a conventional power amplifier (PA) design, the off-state impedance is not important. However, in PA-LNA design, this aspect necessitates proactive consideration. The saturated output power (P_{sat}) of the PA is determined at 10 dBm. Accounting for a 2-dB attenuation due to output matching and a 1.5-dB loss attributed to the PA-LNA loading effect, the output power requirement for the power stage must be more than 13.5 dBm (equivalent to 22 mW). Drawing on the principles of load-line theory [51], an estimation for the P_{sat} of the PA can be derived from:

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$$P_{sat} = \frac{1}{2} \times \frac{V_{max} - V_{min}}{2} \times \frac{I_{max}}{2} \quad (4.1)$$

$$I_{dc} = \frac{I_{max}}{2} = \frac{4P_{sat}}{V_{max} - V_{min}} \quad (4.2)$$

In 65-nm bulk CMOS process, where V_{max} represents the maximum achievable voltage swing at drain of the transistors, and V_{min} stands for the minimum voltage level. For this process, the transistor's supply voltage is 1.2 volts, and the recommended maximum output voltage swing (V_{max}) is twice the direct current (dc) supply voltage. Additionally, V_{min} corresponds to the threshold voltage, approximately 0.3 volts in the 65-nm CMOS process. To achieve a desired saturated output power (P_{sat}) of 13.5 dBm (equivalent to 22 mW), the total current amounts to 45 mA. High class AB operation (with V_{GS} = 0.65 V) in this power stage design is advantageous due to its favorable compromise between gain, linearity, and power efficiency. Given a transistor current density of 0.35 milliamperes per micron (um) with a biasing of 0.65 V for V_G, the total gate width is determined to be 176-µm for this specific power stage configuration. This information is visualized in Fig. 4.12., showcasing the direct current to drain current (DC-IV) curves for a total gate width of 176 um. Furthermore, in Fig. 4.13., the relationship between drain current (I_D) and transconductance (g_m) under various gate biases is illustrated using the same device size.

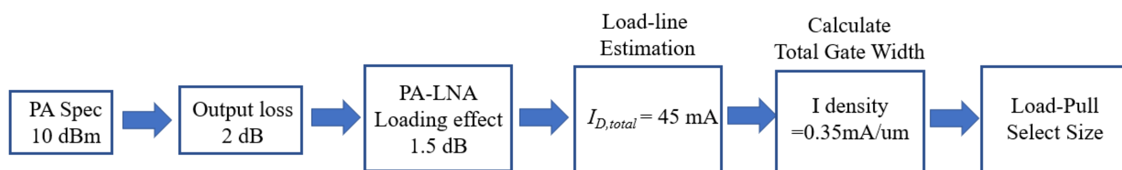

Fig. 4.11. The design flow for transistor size selection

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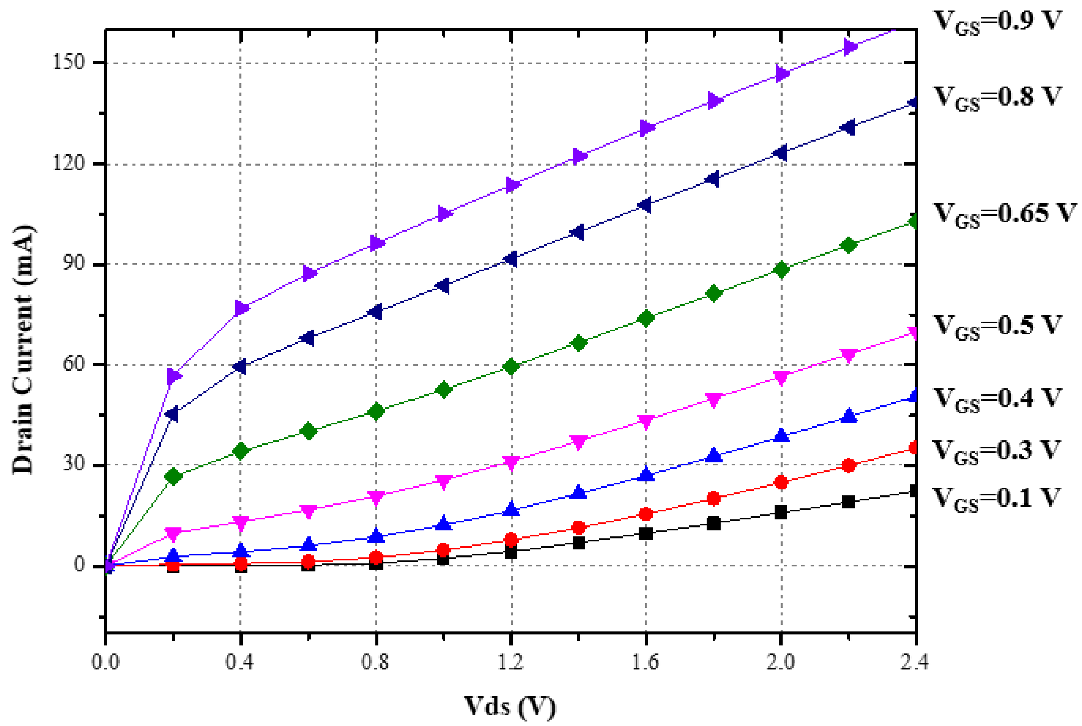

Fig. 4.12. DC-IV curves with a total gate width of 176 μm.

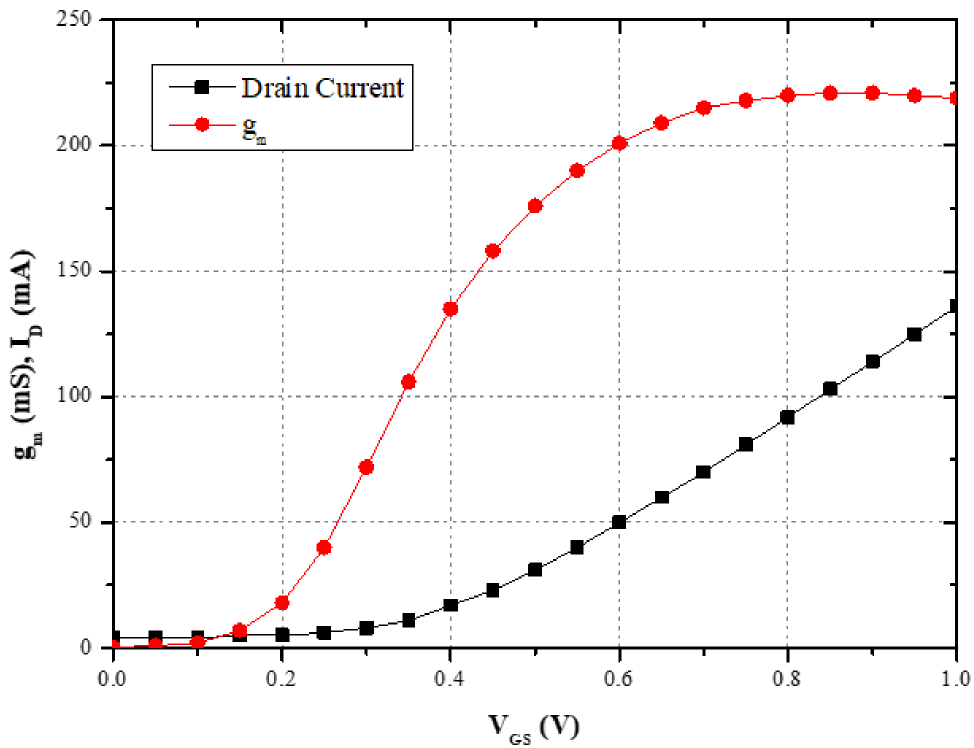

Fig. 4.13. Transconductance and drain current versus gate bias with a total gate width of 176 μm.

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When the fixed total gate width is 176 um, various combinations of devices can be selected. The utilization of multi-way combining techniques and multi-finger devices is commonly employed to mitigate parasitic resistance originating from the gate terminal, while maintaining uniform device sizes. In Table 4.1, a comparison is presented of load-pull simulations for a CS differential pair operating at 85 GHz, with the constraint of a constant total gate width. The neutralized capacitor is set to its maximum K factor value.

The outcomes reveal that opting for a higher number of transistor fingers or combining multiple transistors leads to improved performance in P_{sat}, intrinsic PAE_{MAX}, and near-identical optimal load impedance (Z_{opt}). Nonetheless, it's worth noting that a greater combination of devices results in reduced inherent input resistance. This might render certain extreme input impedance values unsuitable for circuit matching. Moreover, attention must also be given to losses stemming from the combined structure of the transistors. Ultimately, the chosen configuration involves a differential cell comprising two CS units, with four transistors integrated into one unit. Each transistor boasts a size of 2-μm x 11 fingers.

Table 4.1 Load-pull simulation result comparison with the same device size

Vg(V)	0.65	0.65	0.65
W(um)*Finger*Combine	2*11*4	1*22*4	4*11*2
Zopt(Ω)	10.46+j*12.114	10.45+j*12.11	12.25+j*16.1
Zin(Ω)	2.3-j*15.2	3.4-j*12.63	7.82-j*23.46
C_n (fF)	40	44	38.5
Gain(dB)	13.6	13.3	10
Pout (dBm)	14.36	14.01	13.56
PAE (%)	27.6	27.73	20

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4.3.5 Driver Stage Design

Once the performance of power stage has been decided, the appropriate bias conditions and device for the driver stage can be determined. The driver stage is biased within the high Class-AB region, specifically at a V_{GS} of 0.65 V, which be advantageous due to its favorable compromise between gain, linearity, and power efficiency. Given that the power stage demands an input power of approximately 7.5 dBm, and accounting for an estimated loss of 2 dB due to inter-stage matching networks, the P_{sat} of the driver stage needs to be at least 9.5 dBm.

In accordance with load-line theory [51], the overall device size can be established at 88 μm. To attain enhanced power gain, power-added efficiency (PAE), and a compact layout, a configuration involving four CS transistors combined as the driver stage is implemented. Each chosen transistor has dimensions of 2 um x 12 fingers, collectively satisfying the 96-um total size. Based on the load-pull simulation as shown in Fig. 4.14. of the driver stage operating at 85 GHz, the obtained P_{sat} and PAE_{MAX} values stand at 11.72 dBm and 30.3% respectively. Additionally, the optimal load impedance is determined as 16.45 + j33.266 ohm.

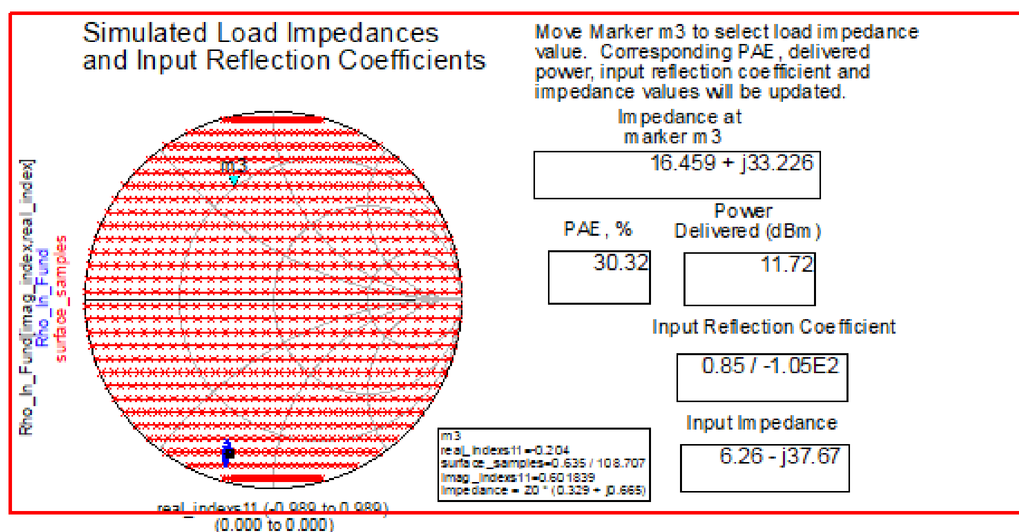

Fig. 4.14. Load-pull simulation of the driver stage at 85 GHz

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4.3.6 Input Stage Design

After the performance of power stage has been decided, the appropriate bias conditions and device for the driver stage can be determined. The driver stage is biased within the high Class-AB region. Given that the power stage demands an input power of approximately -2.5 dBm, and accounting for an estimated loss of 2 dB due to inter-stage matching networks, the P_{sat} of the driver stage needs to be at least 0.5 dBm. According to load-line theory [51], the overall device size can be established at 48 μm. To attain enhanced power gain, power-added efficiency (PAE), and a compact layout, a configuration involving four CS transistors combined as the driver stage is implemented. Each chosen transistor has dimensions of 1 um x 12 fingers, collectively satisfying the 48-um total size. Based on the load-pull simulation (illustrated in Fig. 4.15) of the driver stage operating at 85 GHz, the obtained P_{sat} and PAE_{MAX} values stand at 8 dBm and 28 % respectively. Additionally, the optimal load impedance is determined as 20.8 + j51.8 ohm.

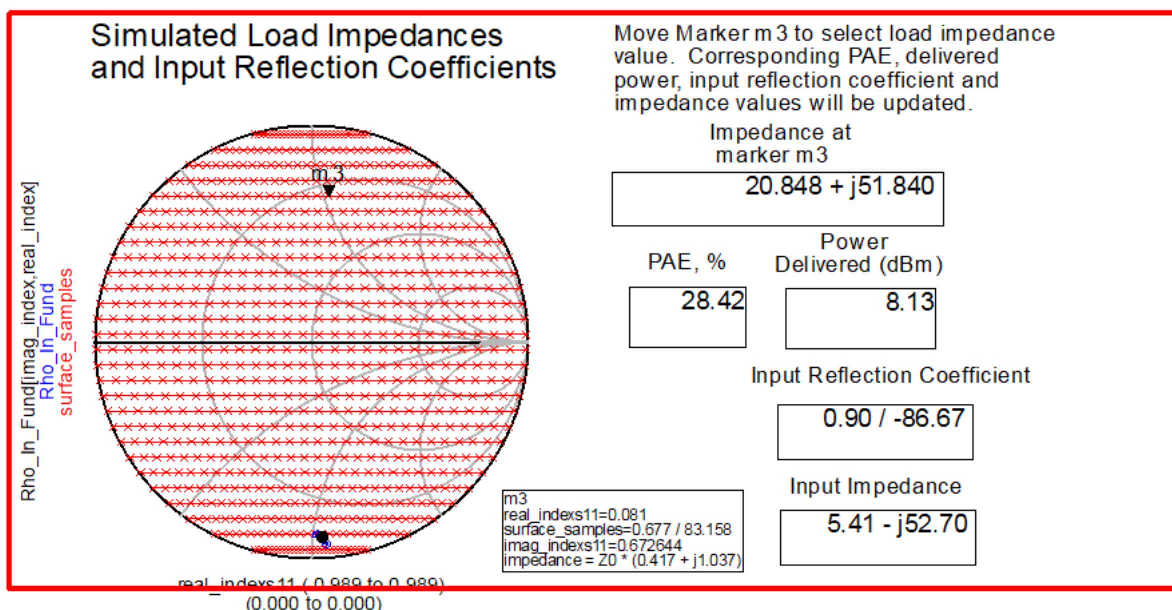

Fig. 4.15. Load-pull simulation of the input stage at 85 GHz

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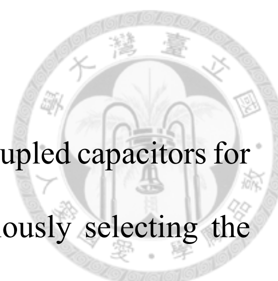
4.3.7 Neutralization Capacitive Technique[52]



The technique of capacitive neutralization employing cross-coupled capacitors for differential CS transistors has a well-established history. By judiciously selecting the neutralization capacitance (Cn), the feedback pathway within the CS transistors can be theoretically entirely nullified. Consequently, both the K factor and reverse isolation experience a remarkable augmentation, all the while maintaining gains and output power performance. In the arrangement of a differential CS transistor circuit depicted in Fig. 4.16.(a), the reverse isolation exhibits a direct correlation with S12. An escalation in S12 exacerbates the degradation of both the Maximum Available Gain (MAG) and Maximum Stable Gain (MSG) of the CS transistor, potentially rendering the transistor unstable. The inherent gate-to-drain capacitance, C_{gd}, engenders a feedback route, compromising the reverse isolation of the CS transistor. This effect becomes more pronounced particularly at Ka-band frequencies. Capacitive neutralization involves the utilization of equivalent negative capacitance (-Cn) to counteract C_{gd}. This negative capacitance is generated by the introduction of cross-coupled capacitors (C_n) between the drain and gate of the two CS transistors operating in a differential configuration.

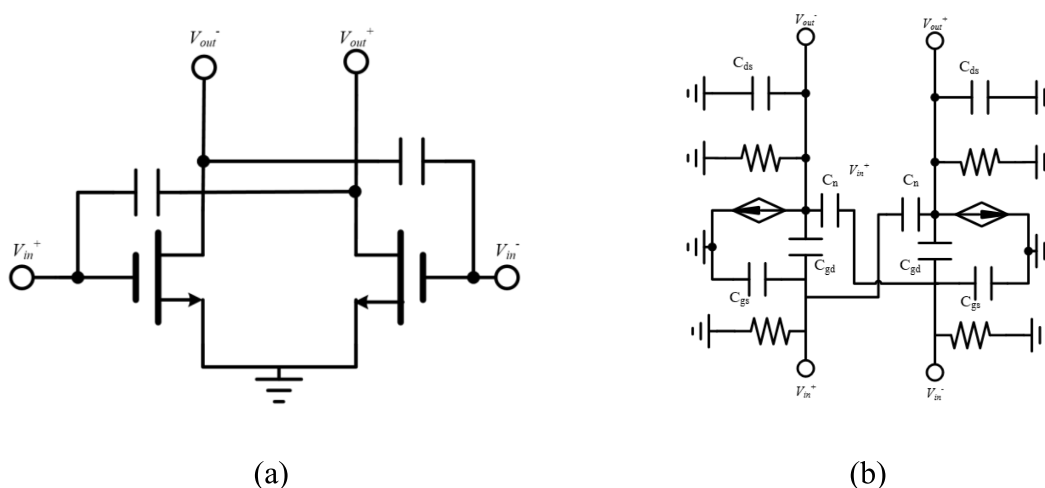


Fig. 4.16. Differential CS cell with neutralization capacitators (C_n) in cross-coupled connection and its small-signal model

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Fig. 4.16.(b) shows the equivalent small-signal model of differential CS cell with capacitive neutralization technique in differential mode. To verify the concept, the Y-parameters and K factor of the differential circuit can be expressed as[53]

$$\begin{aligned} Y_{11} &= g_g + s * Cgs + s * (C_{gd} + C_n) \\ Y_{12} &= -s * (C_{gd} - C_n) \\ Y_{21} &= g_m - s*(C_{gd} - C_n) \\ Y_{22} &= g_{ds} + s*C_{ds} + s*(C_{gd} + C_n) \end{aligned} \tag{3.2}$$

and

$$K = \frac{2 \cdot \Re\{y_{11}\} \cdot \Re\{y_{22}\} - \Re\{y_{12} \cdot y_{21}\}}{|y_{12} \cdot y_{21}|} \tag{3.3}$$

where g_g is the parasitic gate conductance of the NMOS transistor, gas is the parasitic drain-to-source conductance of the NMOS transistor C_{gs}, C_{ds}, C_{gd} are gate-source capacitance, drain-source capacitance, gate-drain capacitance, respectively, as shown in Fig. 4.16. Differential CS cell with neutralization capacitators (Cn) in cross-coupled connection and its small-signal model. As can be seen, when C, is equal to C_{gd}, the K factor is close to infinity and Y21 is cancelled out, which means that the amplifier is unconditionally stable and the reverse isolation is increased. Based on the definition of the MSG/MAG, the MSG/MAG of the differential CS amplifier with cross-coupled neutralization capacitors can be expressed as[53]

$$\begin{aligned} MSG &= \frac{|y_{21}|}{|y_{12}|} \\ &= \frac{|gm - s \cdot c_{gd}|}{|-s \cdot c_{gd}|} \\ MAG &= MSG \cdot \left(K - \sqrt{K^2 - 1}\right). \end{aligned} \tag{3.4}$$

Where K composed of the Y-parameters can be found in Eqn. (3.3). when Cn is equal to C_{gd}, MSG/MAG can achieve its maximum value.

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Fig. 4.17. results present simulation outcomes showcasing the Maximum Stable Gain to Maximum Available Gain ratio (MSG/MAG) and the stability factor (K) of a differential CS pair, varying in device size at 176-um as influenced by Cn. These simulations distinctly illustrate that the application of the capacitive neutralization technique contributes to the stabilization of the differential CS pair. Furthermore, the adoption of this technique yields a noteworthy enhancement in the Maximum Available Gain (MAG) of the differential CS pair, with an increase of approximately 5 dB compared to instances where the capacitive neutralization technique is not employed. Fig. 4.18 show the 3-D structure of power stage with neutralization capacitive technique.

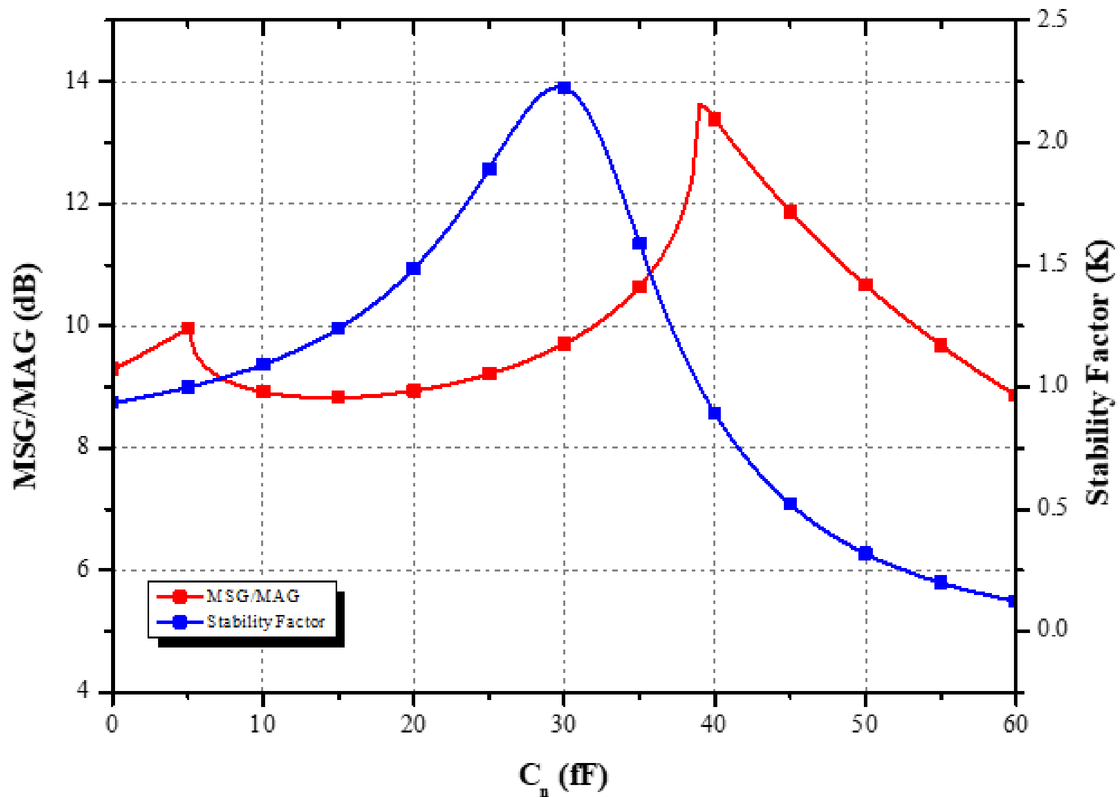

Fig. 4.17. The simulation results of MSG/MAG and stability factor (K) of a differential CS pair with the device size of 176-um versus C_n

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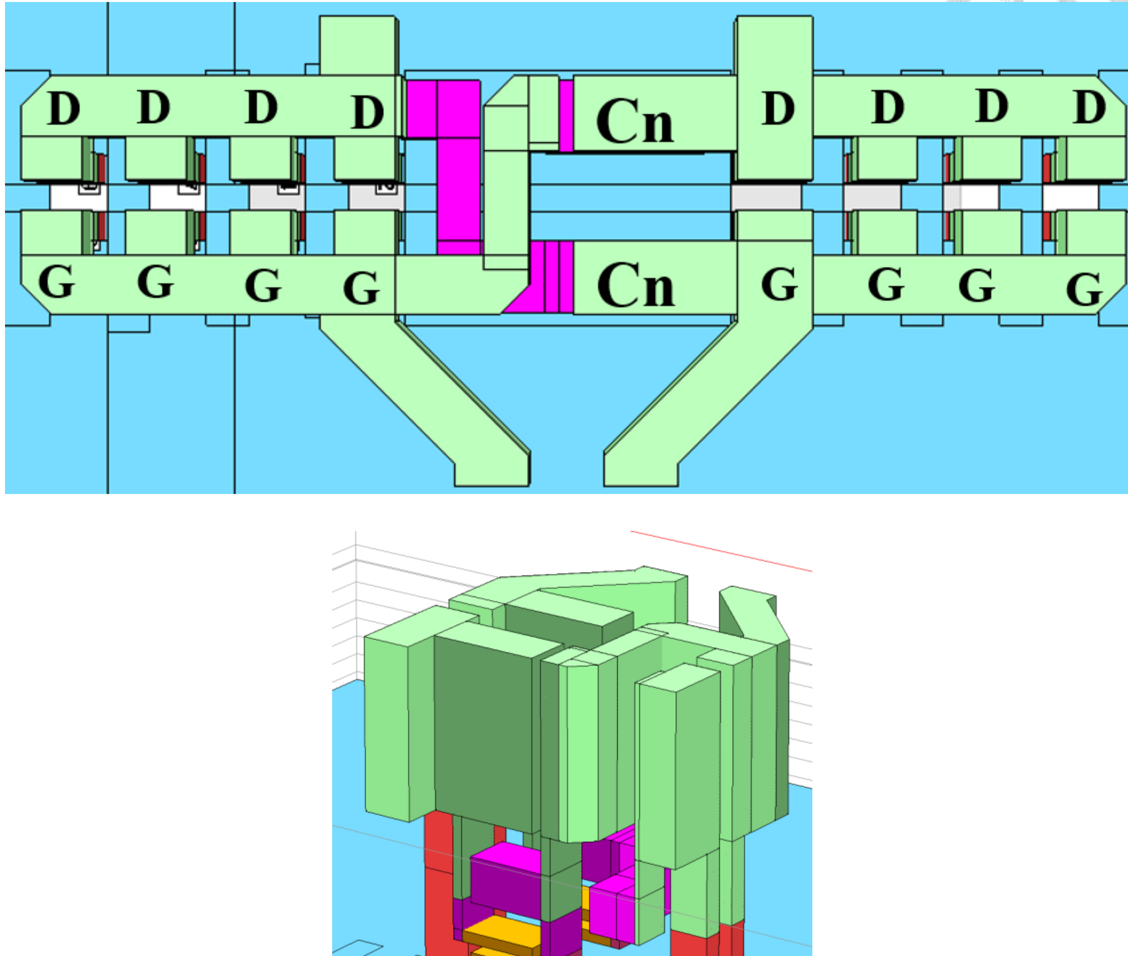

Fig. 4.18. 3-D structure of the differential CS pair and neutralization capacitance in power stage.

4.3.8 Matching Network

For the purpose of achieving output power matching, it becomes imperative to transform the load impedance into its corresponding optimal value, denoted as Z_{opt}, which equates to 10.45 + j*12.11Ω at 85 GHz. Addressing this, a broadside coupling transformer has been meticulously designed to facilitate power matching. Its three-dimensional layout has been realized within the Sonnet EM simulator, as depicted in Fig. 4.19. Within the transformer design, the primary winding (L_p) has been conceived with an ultra-thick top metal (M9), a measure taken to mitigate the impact of ohmic loss during the coupling of signals. Meanwhile, the secondary winding has been implemented using M8. Notably, the

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center-tap capacitor integrated into the primary winding serves a dual role: it contributes to the balanced performance of the output transformer, and simultaneously functions as a means to provide the drain supply voltage for the power stage. Fig. 4.20 provides a visualization of the S-parameters as derived from electromagnetic (EM) simulations, spanning a range of frequencies for this output matching network. The results unveiled therein indicate that the output transformer-based matching network renders an insertion loss of 1.8 dB at 85 GHz, while also ensuring that the input-output return losses exceed the threshold of 8 dB.

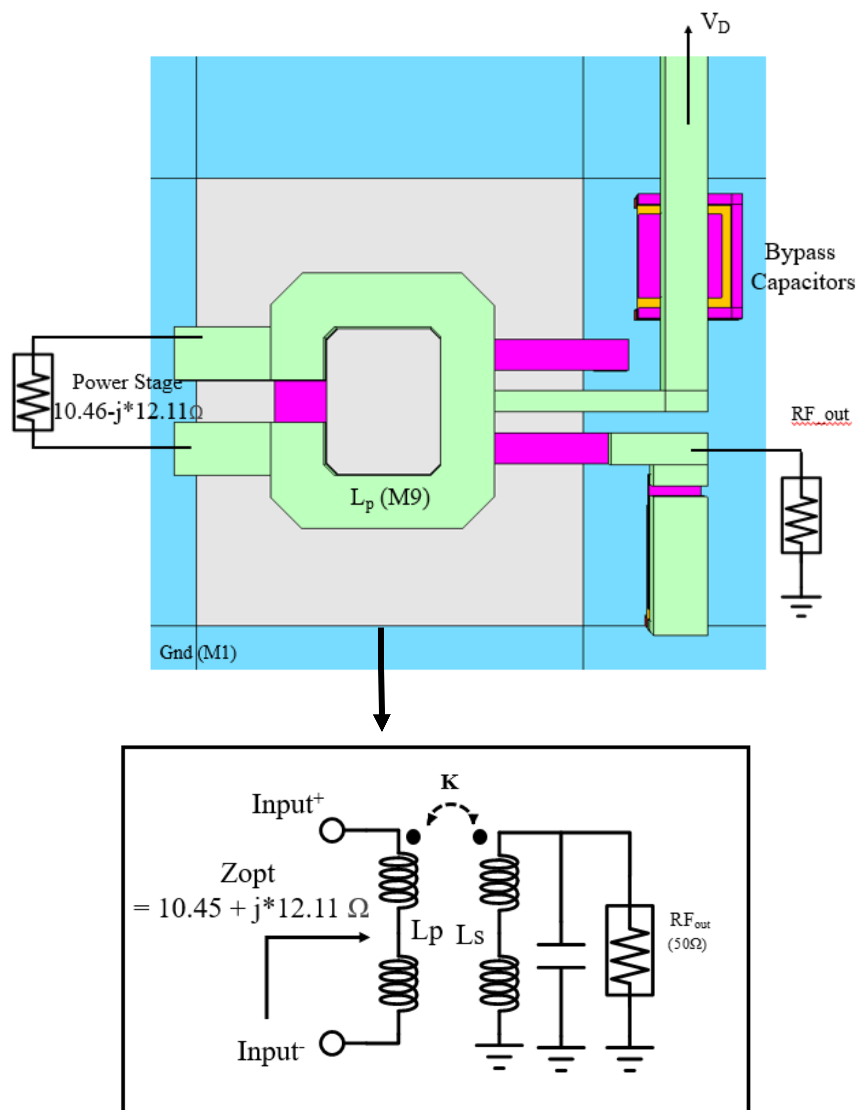

Fig. 4.19. Transformer structure of Output matching.

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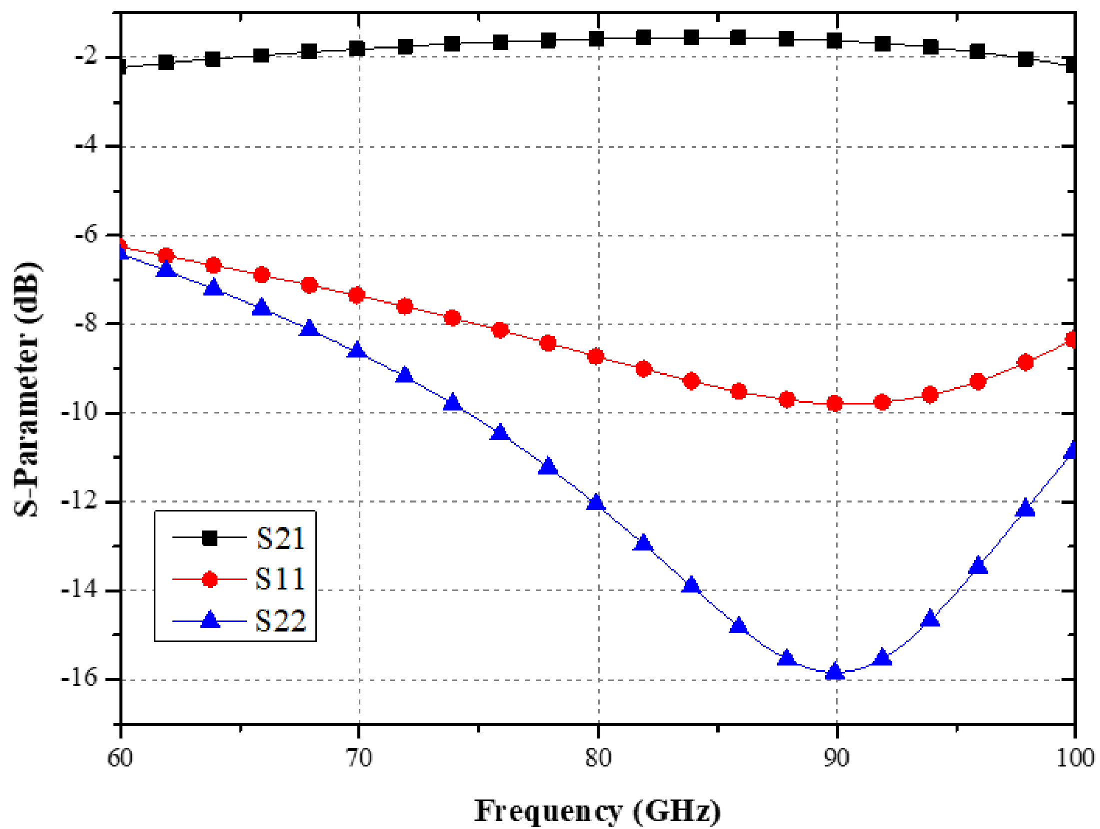

Fig. 4.20. S-parameter simulation result of the EM output matching network

The 3-D layout in Sonnet EM simulator of inter-stage matching network between driver stage and power stage is shown in Fig. 4.21. This matching network used to transform impedance from input impedance of power stage (3.4-j12.63) Ω to Z_{opt} of driver stage (16.45+j33.26) Ω. The drain supply voltage of driver stage is fed by the center-tap capacitors of the primary winding, and the gate supply voltage of the power stage is fed by the center-tap 5-k resistor to suppress common mode signal. The 3-D layout in Sonnet EM simulator of matching network between input stage and driver stage is shown in Fig. 4.21. This matching network used to transform impedance from input impedance of driver stage (6.26-j37.67) Ω to Z_{opt} of input (20.8 + j51.8) Ω. The drain supply voltage of driver stage is fed by the center-tap capacitors of the primary winding, and the gate supply

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voltage of the power stage is fed by the center-tap 5-k resistor to suppress common mode signal. The 3-D layout in Sonnet EM simulator of input matching is shown in Fig. 4.22. This matching network used to transform impedance from 50 Ω to conjugate input impedance of input stage (5-j52.7) Ω. The gate supply voltage of drive stage is fed by the center-tap 5-k Ω resistor of the secondary winding.

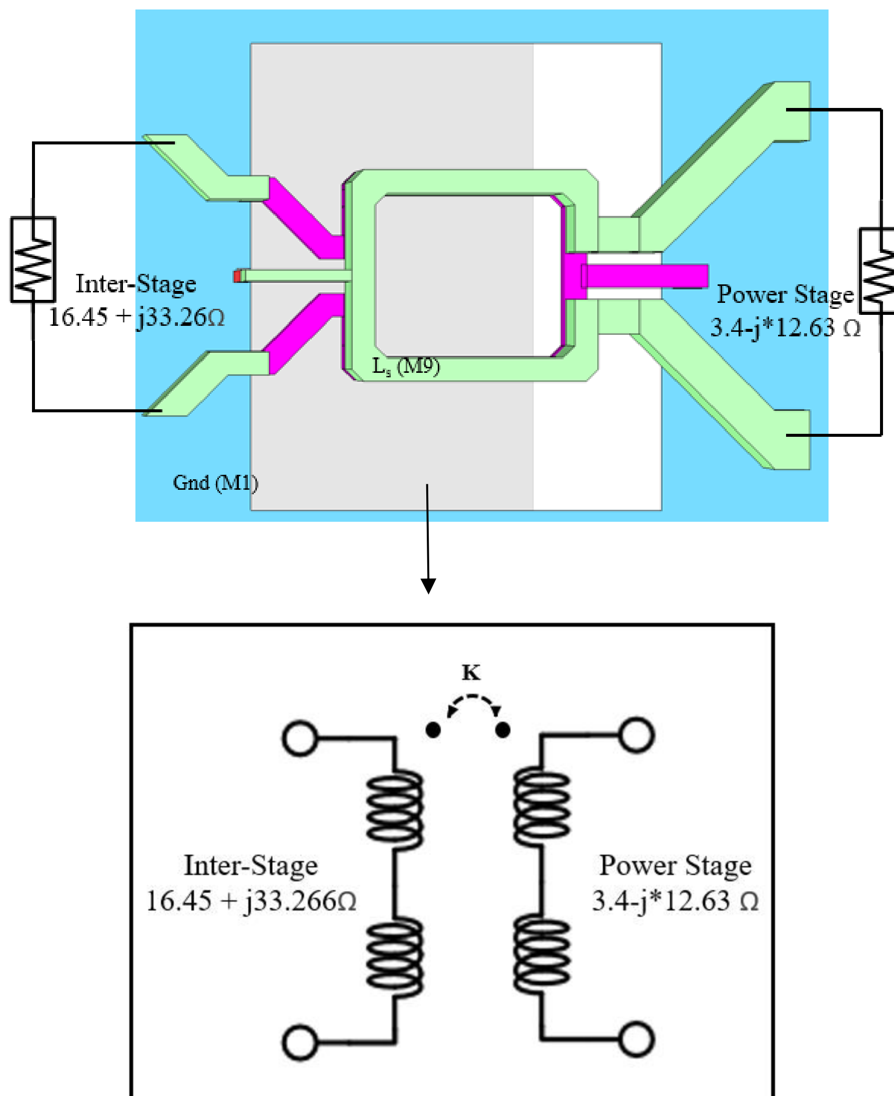

Fig. 4.21. Transformer structure of inter-stage matching network between driver stage and power stage.

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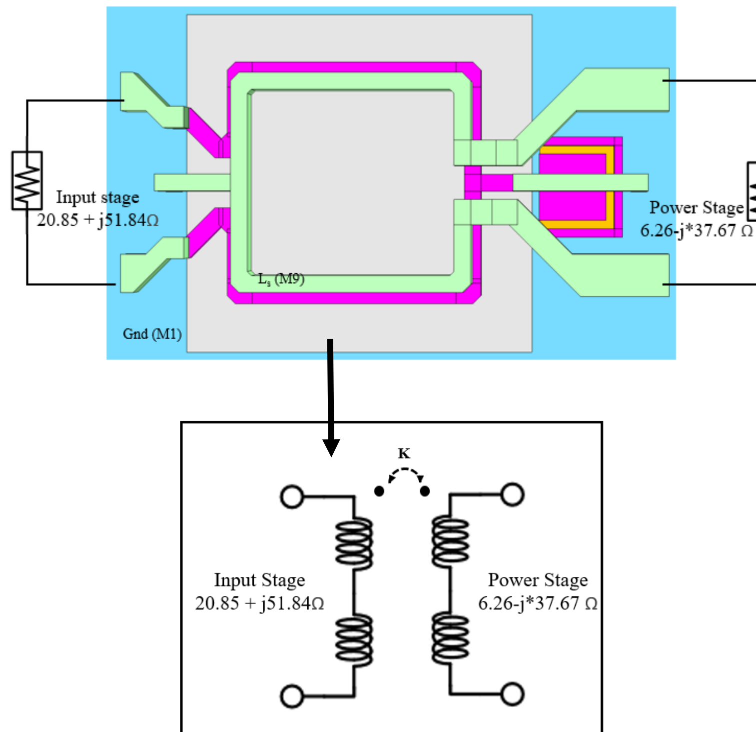

Fig. 4.22. Transformer structure of inter-stage matching network between input stage and driver stage.

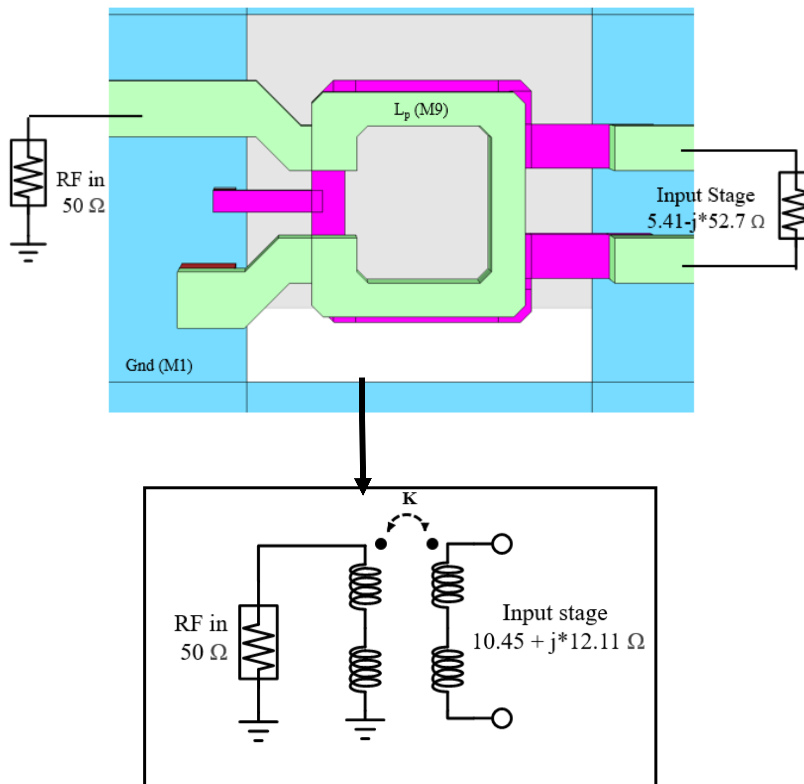

Fig. 4.23. Transformer structure of input matching network.

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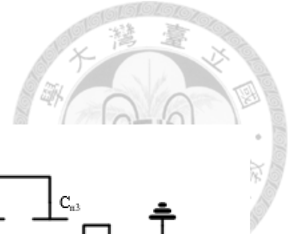
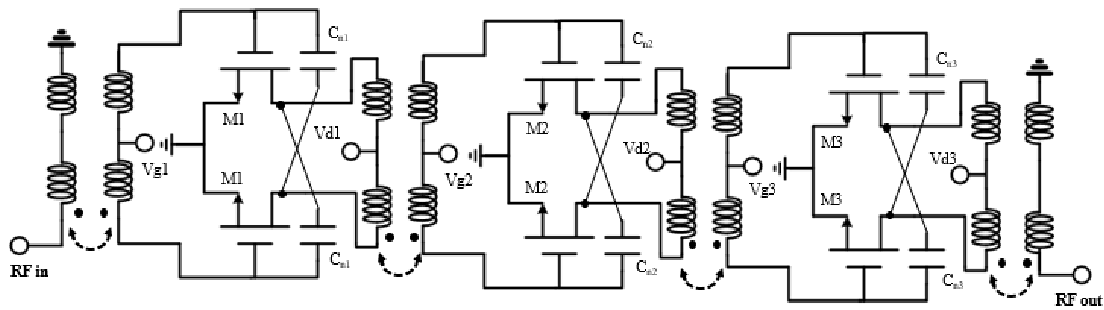
4.3.9 Circuit Schematic and OFF-state Impedance Check





M1 = 2 x (1 μm x 12 fingers)	C_{n1} = 10 fF
M2 = 2 x (2 μm x 12 fingers)	C_{n2} = 24 fF
M3 = 4 x (2 μm x 11 fingers)	C_{n3} = 40 fF

Fig. 4.24. Total schematic of PA part.

The PA part schematic is shown in Fig. 4.24. All of three stages are implemented in a differential CS pair with neutralized capacitors. The device size of transistor M1 is 4 x (2 μm x 11), M2 is chosen for 2 x (2 μm x 12 fingers), and M3 is 4 x (2 μm x 11 fingers), respectively, the neutralized capacitors C_{n1}, C_{n2}, and C_{n3} are 10fF, 24fF, and 40fF.

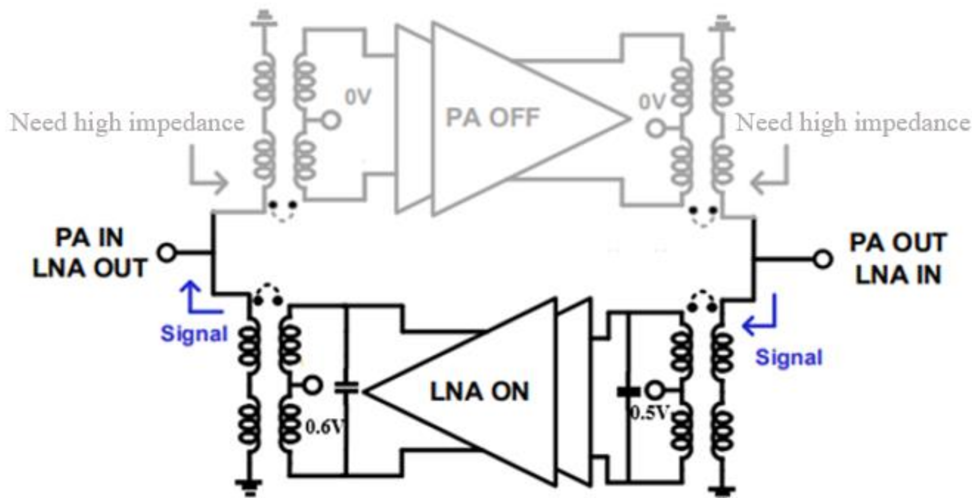


Fig. 4.25. The simplified schematic of the PA in off-state.

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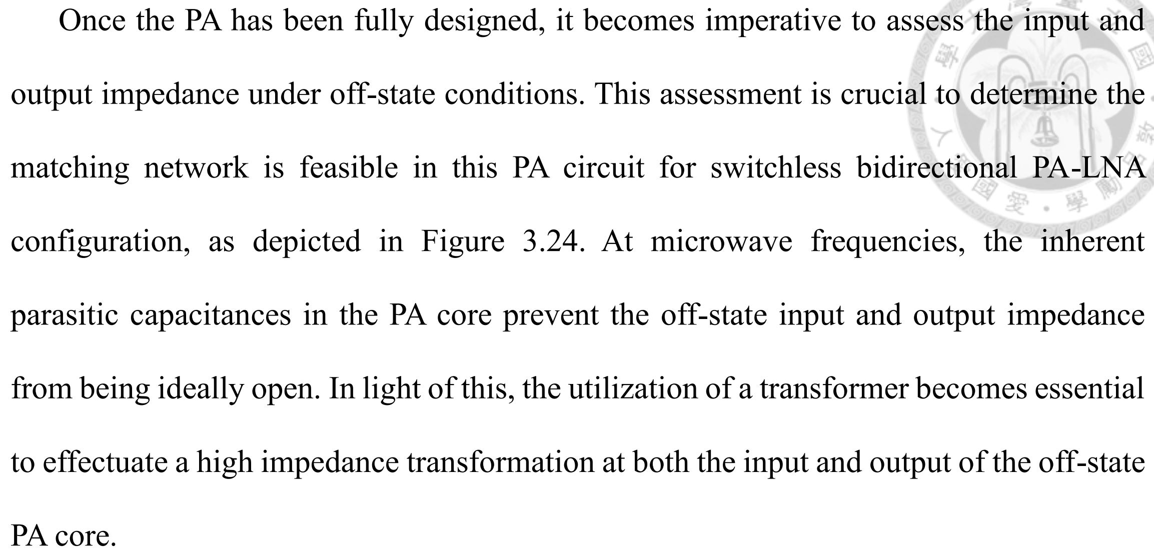

Once the PA has been fully designed, it becomes imperative to assess the input and output impedance under off-state conditions. This assessment is crucial to determine the matching network is feasible in this PA circuit for switchless bidirectional PA-LNA configuration, as depicted in Figure 3.24. At microwave frequencies, the inherent parasitic capacitances in the PA core prevent the off-state input and output impedance from being ideally open. In light of this, the utilization of a transformer becomes essential to effectuate a high impedance transformation at both the input and output of the off-state PA core.

Fig. 4.26. shows the off-state impedance characteristics of the PA across the frequency range of 70 GHz to 95 GHz. Evidently, the original input/output impedance of the off-state PA core fails to attain the desired level of impedance, thus resulting in issues of signal leakage and reduce loading effects. However, through the implementation of a transformer, the off-state impedance of the PA core can be systematically adjusted to reside within the high-impedance domain. Consequently, this modified PA circuit emerges as a suitable candidate for integration into a switchless bidirectional PA-LNA setup. Such integration not only mitigates the challenges posed by loading effects and signal leakage, but also serves to enhance overall performance.

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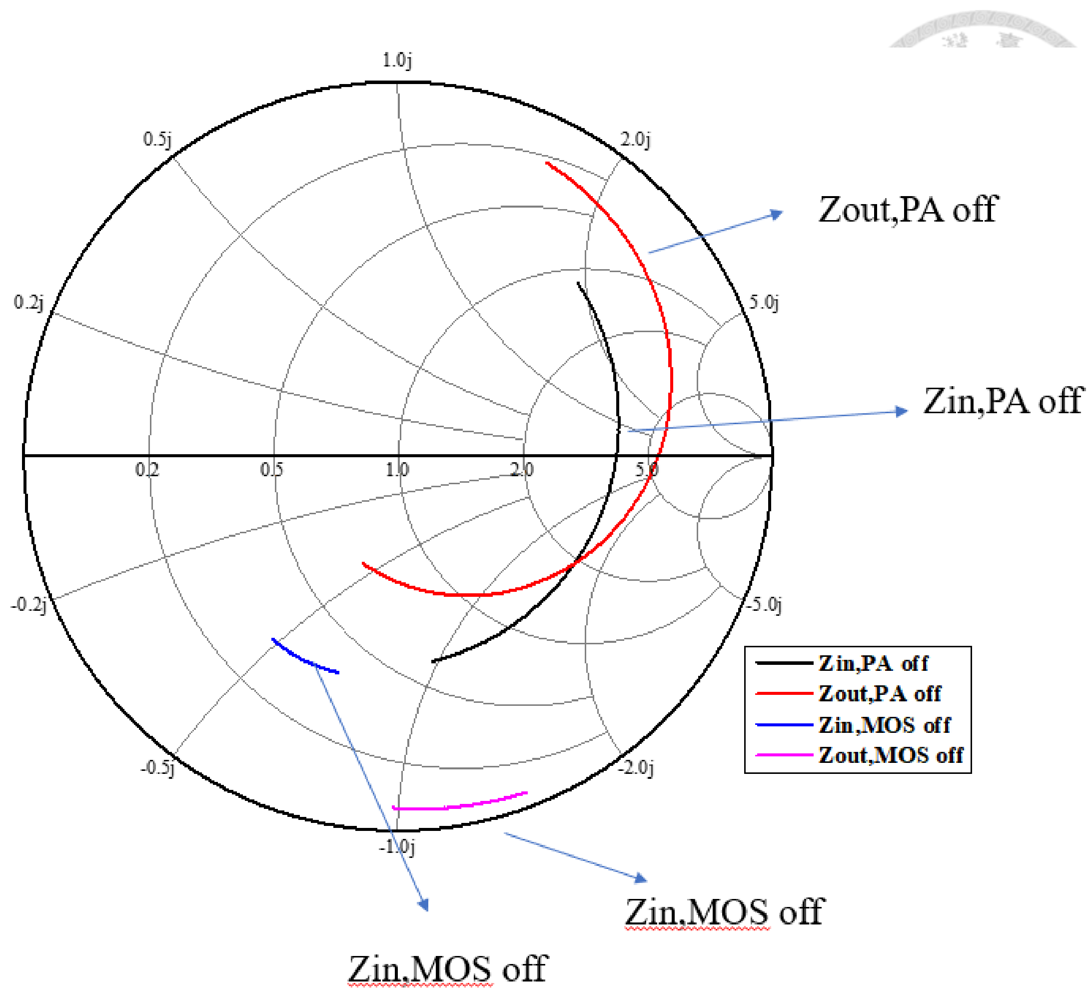

Fig. 4.26. The off-state impedance of PA from 70-95 GHz.

To specify the impact of off-mode impedance on performance, the simulation is as shown in Fig. 4.27. The simulation sweeps the load impedance from 50 to 150 Ω, including open circuit conditions, as shown in Fig. 4.28 . Based on the simulation results, a lower off-mode impedance is found to degrade the gain by approximately 10 dB compared to the open condition, resulting in an unfavorable noise figure.

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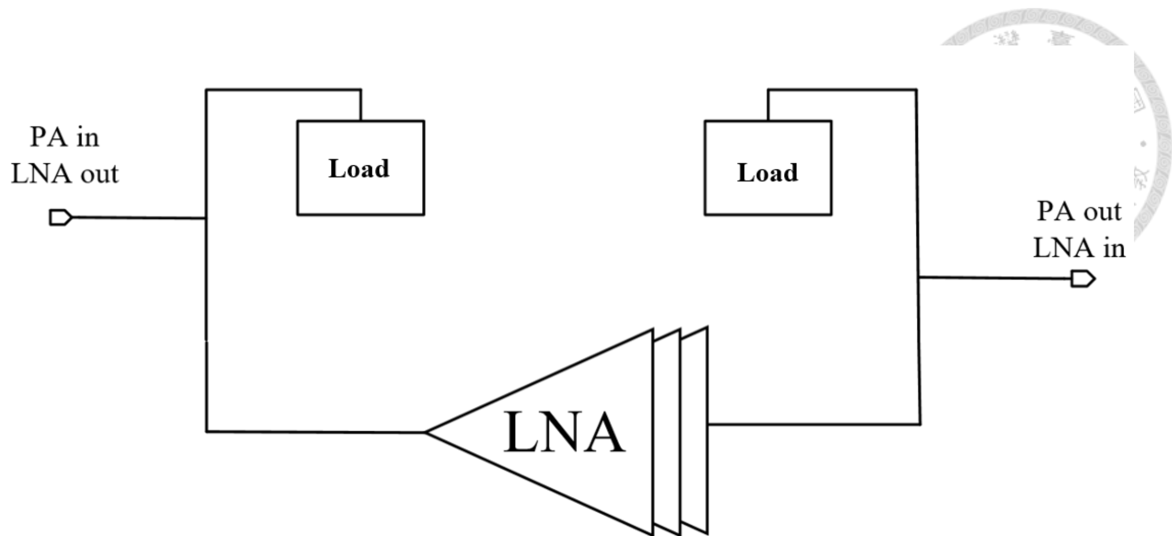

Fig. 4.27. The setup of off-mode load impedance simulation in LNA mode.

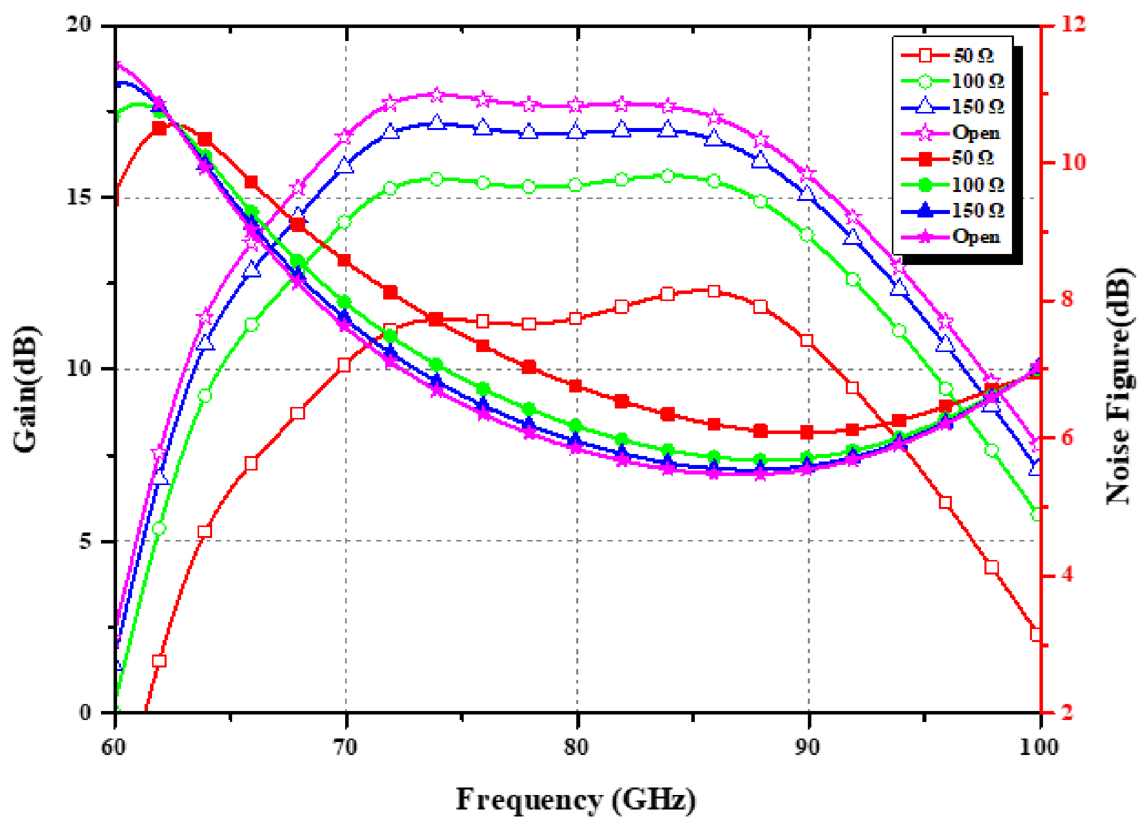

Fig. 4.28. The simulated result of off-mode load impedance simulation in LNA mode.

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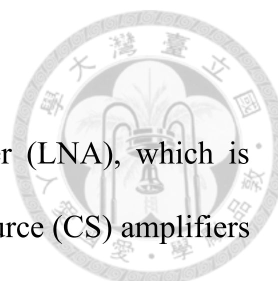

4.3.10 Design of LNA

Fig. 4.26 depicts the schematic of the Low Noise Amplifier (LNA), which is constructed using a topology of three-stage differential Common-Source (CS) amplifiers featuring cross-coupled neutralized capacitors. Although utilizing smaller transistors can yield improved Maximum Stable Gain (MSG) and reduced minimum Noise Figure (NF_{min}), such an approach often leads to compromised stability. Moreover, smaller transistors tend to result in exceedingly high impedance, particularly within a differential amplifier framework, where impedance is effectively doubled. Hence, in the design of this LNA, the sizing of transistors M4, M5, and M6 has been determined as 2× (2-um x 10 fingers) and 2× (2-μm x 8 fingers) respectively. This selection of device dimensions strikes a balance between achieving satisfactory noise performance and facilitating favorable impedance matching conditions. In terms of biasing, the gate voltages of the set at 0.55 voltage when subjected to a drain voltage set 1.0 voltage. This biasing strategy has been employed to optimize noise performance and gain for the LNA configuration.

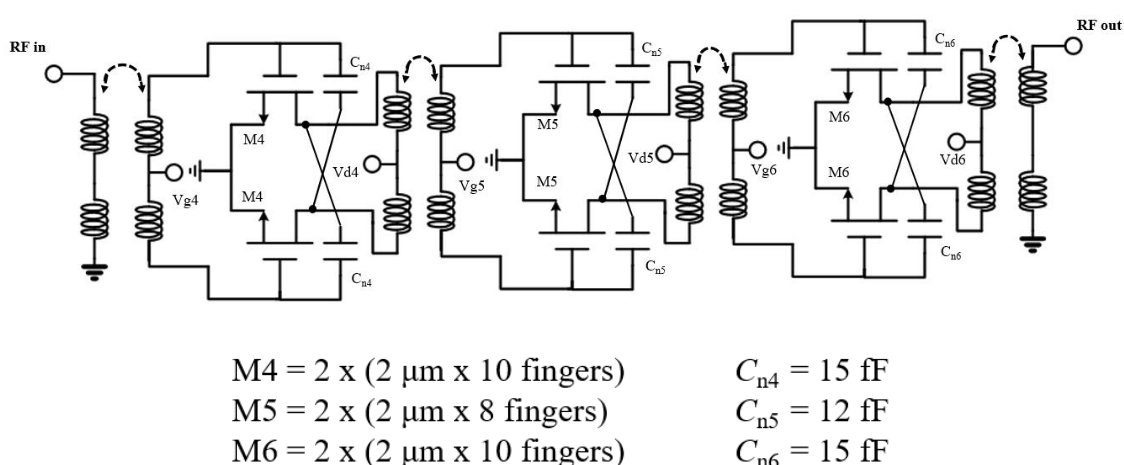

Fig. 4.29. Total schematic of LNA part.

After roughly deciding the required parameters of the single-to-differential transformer by using ideal transformer model, the realistic single-to-differential

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transformer can be designed by EM simulation. In the input noise matching, the load impedance needs to be converted to optimal noise impedance which is equal to 9.97-j20.71 Ω at 85 GHz. The broadside coupling transformer is designed for noise matching and its 3-D layout in Sonnet EM simulator is shown in Fig. 4.30 The center-tap resistor and capacitors are included and applied for the gate bias. Fig. 4.31 shows the EM simulated S-parameters versus different frequencies of this input matching network. The results reveal that the input transformer matching network provides 1.8 dB of the insertion loss at 80 GHz and the I/O return loss are better than 10 dB.

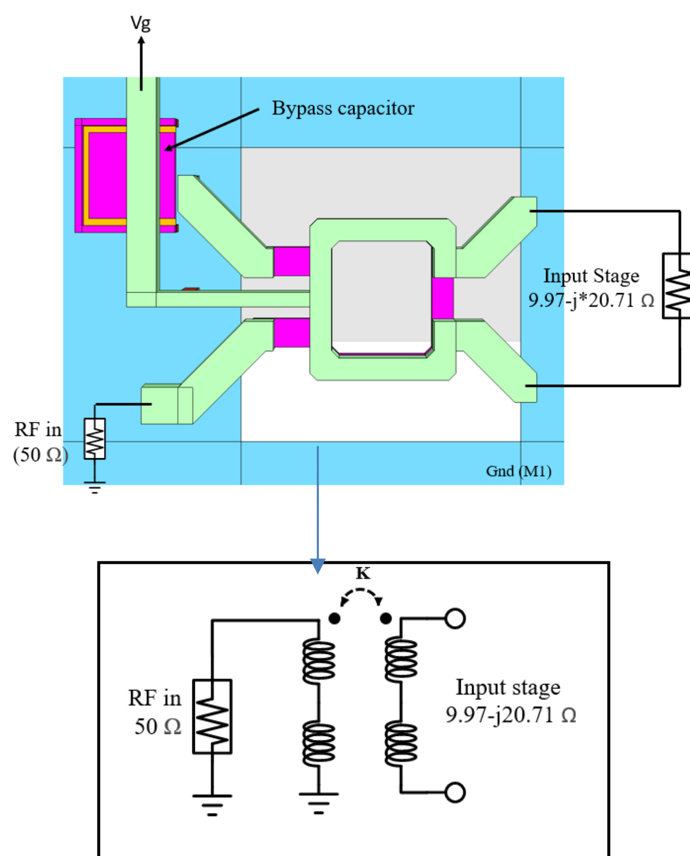

Fig. 4.30. 3-D structure of input matching transformer.

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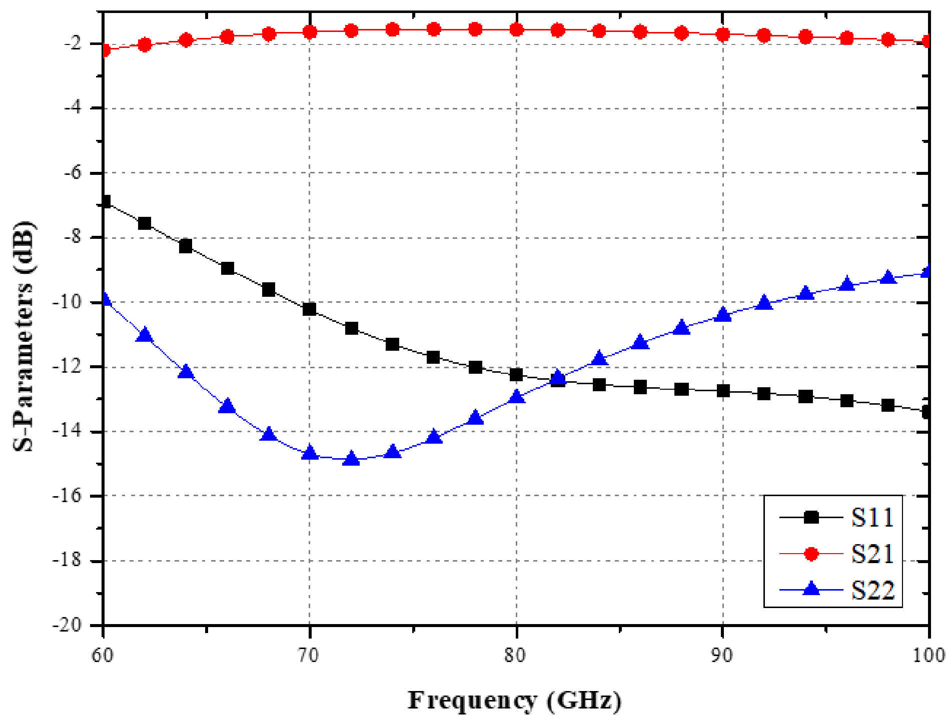

Fig. 4.31. Simulation result of the EM input matching network.

The 3-D layout in Sonnet EM simulator of inter-stage matching network between input stage and second stage is shown in Fig. 4.32. This matching network used to transform impedance from input impedance of inter-stage (5-j48.9) Ω to conjugate matching of input stage (12-j42.2) Ω. The drain supply voltage of driver stage is fed by the center-tap capacitors of the primary winding, and the gate supply voltage of the input stage is fed by the center-tap 5-k resistor to suppress common mode signal. The 3-D layout in Sonnet EM simulator of matching network between inter-stage and output stage is shown in Fig. 4.33. This matching network used to transform impedance from input impedance (4.3-j42.2) Ω of output stage to conjugate matching of inter-stage (12.5- j50) Ω. The drain supply voltage of driver stage is fed by the center-tap capacitors of the primary winding, and the gate supply voltage of the power stage is fed by the center-tap 5-k resistor to suppress common mode signal. The 3-D layout in Sonnet EM simulator of input matching is shown in Fig. 4.34 This matching network used to transform impedance

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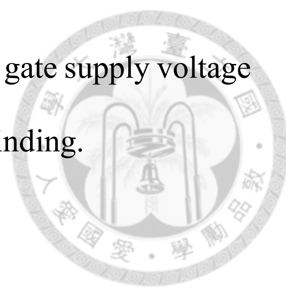
from 50 to conjugate input impedance of output stage (12-j45) Ω. The gate supply voltage of drive stage is fed by the center-tap 5-k resistor of the secondary winding.



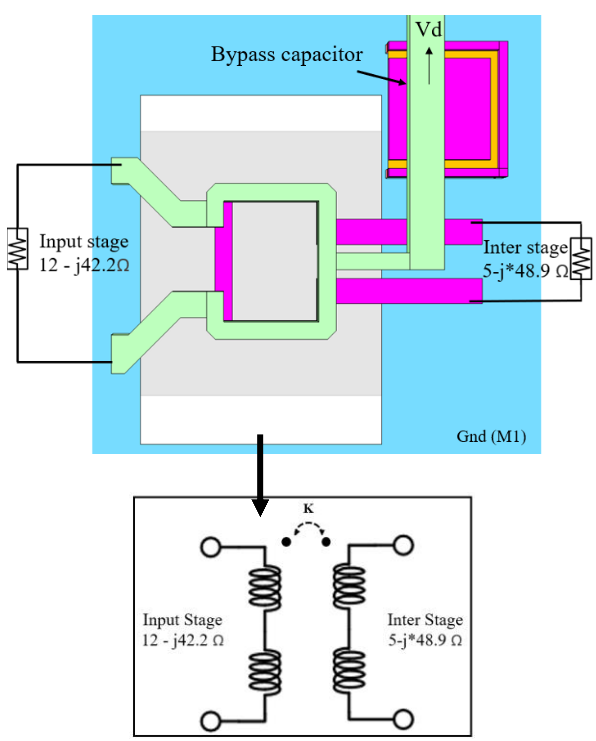


Fig. 4.32. Transformer structure of inter-stage matching network between input stage and inter stage.

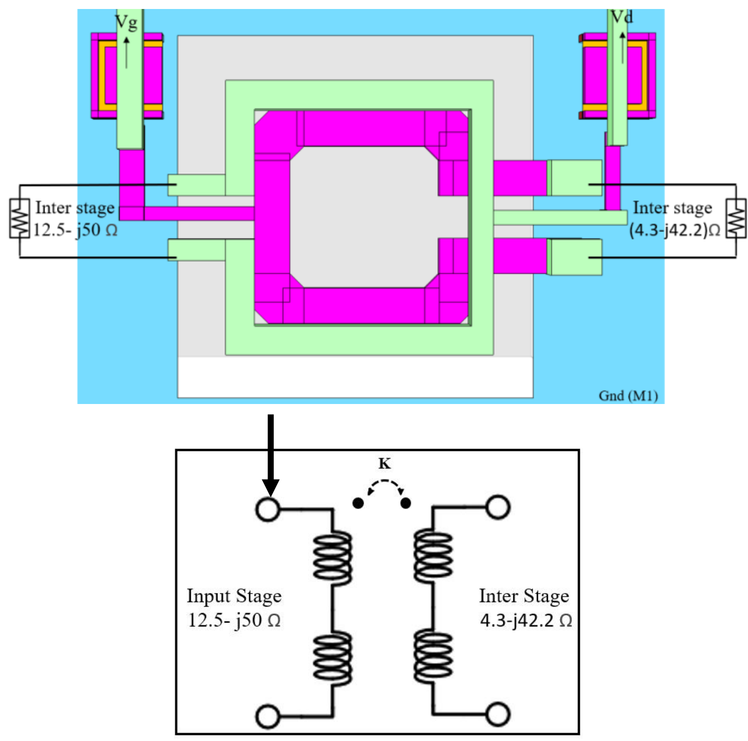


Fig. 4.33. Transformer structure of inter-stage matching network between input stage and second stage.

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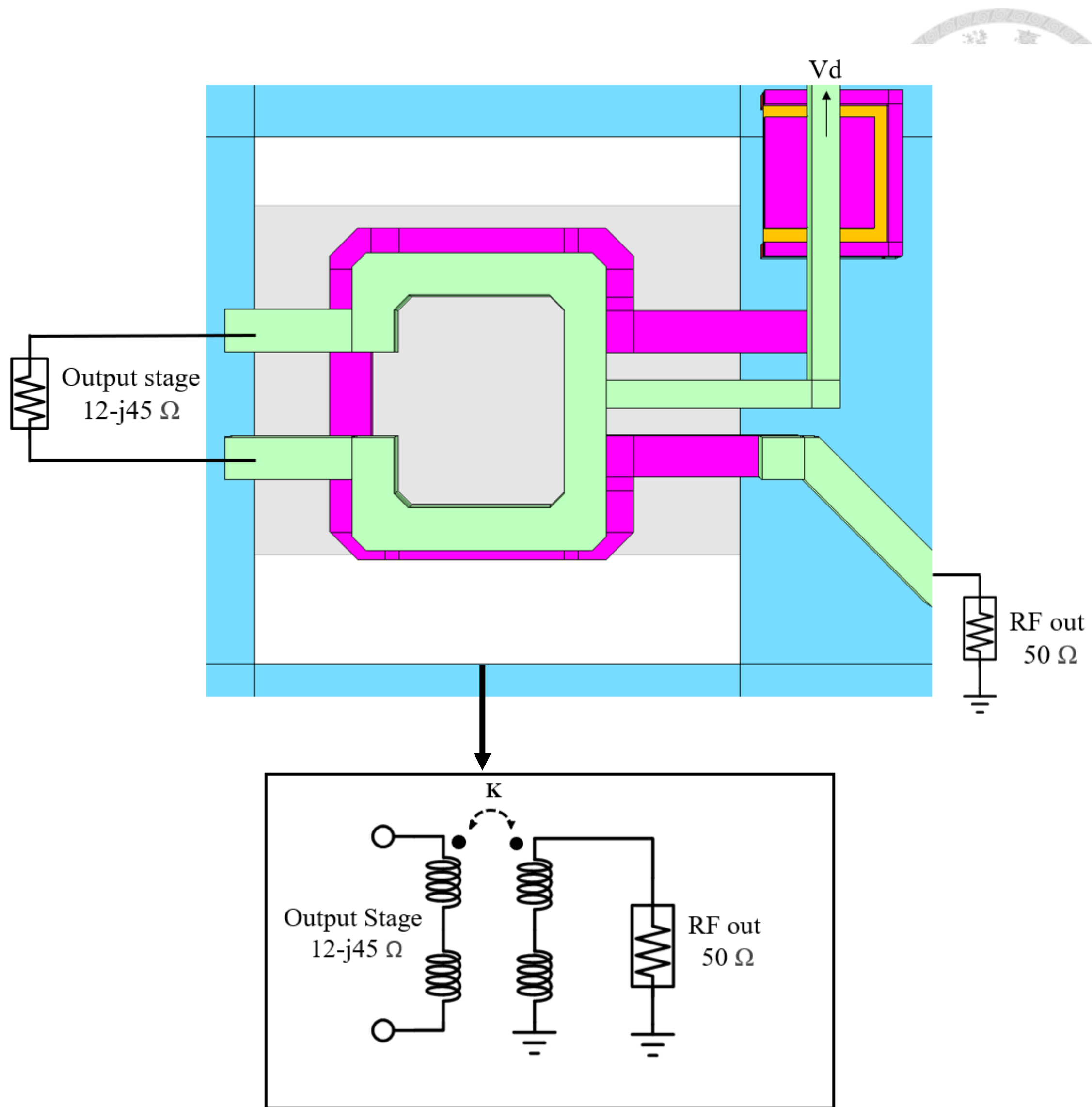

Fig. 4.34. Transformer structure of output stage matching network.

4.3.11 OFF-state Impedance Check

Once the Low Noise Amplifier (LNA) design is finalized, it becomes crucial to assess the input and output impedance under off-state conditions. This assessment serves to determine the viability of integrating this LNA circuit into a switchless bidirectional PA-LNA setup, as depicted in Fig. 4.35. As previously discussed, the off-state input and output impedance of the LNA core do not attain ideal openness due to inherent parasitic capacitances. In lights of this, the utilization of a transformer is necessary to effectuate a high impedance transformation at both the input and output terminals of the off-state LNA

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core. Fig. 4.36 illustrates the off-state impedance characteristics of the LNA across the frequency range of 70 GHz to 95 GHz. Evidently, the original input/output impedance of the off-state LNA core falls short of the desired high impedance level, leading to issues of signal leakage and substantial loading effects. By incorporating a broadside coupling transformer, the low impedance inherent to the off-state LNA core can be systematically converted into the high-impedance region. As a result of this transformation, the adapted LNA circuit emerges as a suitable candidate for inclusion within a switchless bidirectional PA-LNA configuration. This integration not only alleviates the challenges posed by loading effects and signal leakage, but also enhances the overall performance of the system.

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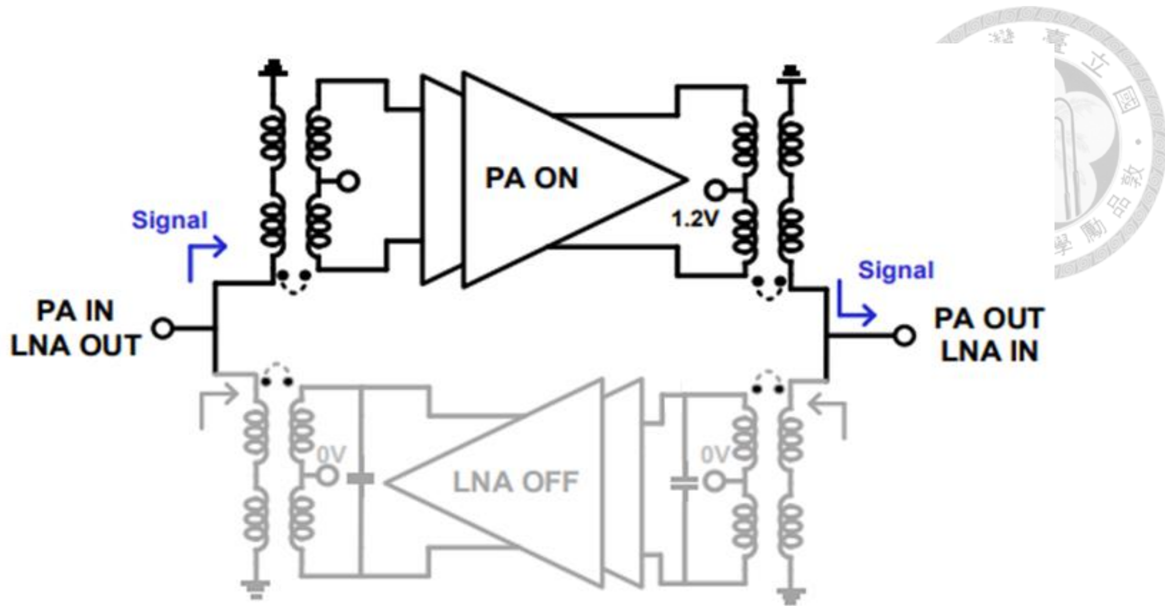

Fig. 4.35. The simplified schematic of the LNA in off-state.

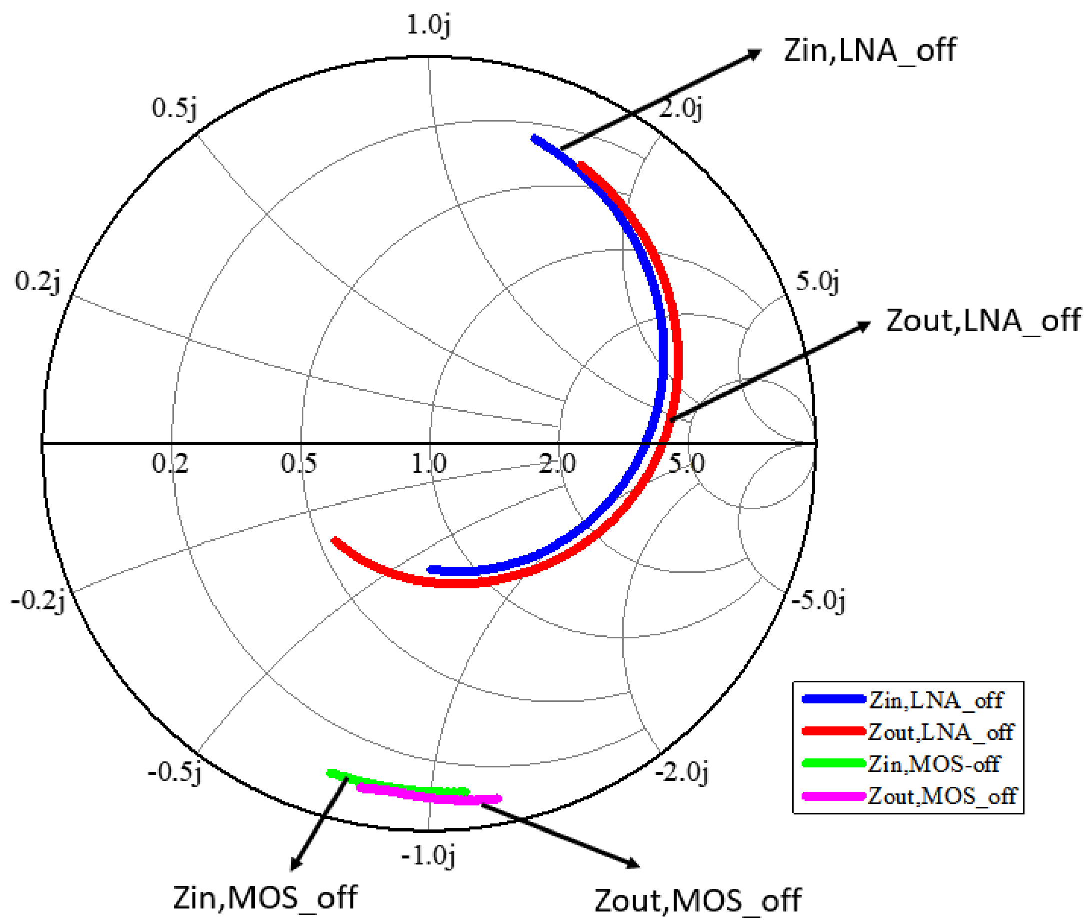

Fig. 4.36. The off-state impedance of LNA from 70GHz to 95 GHz.

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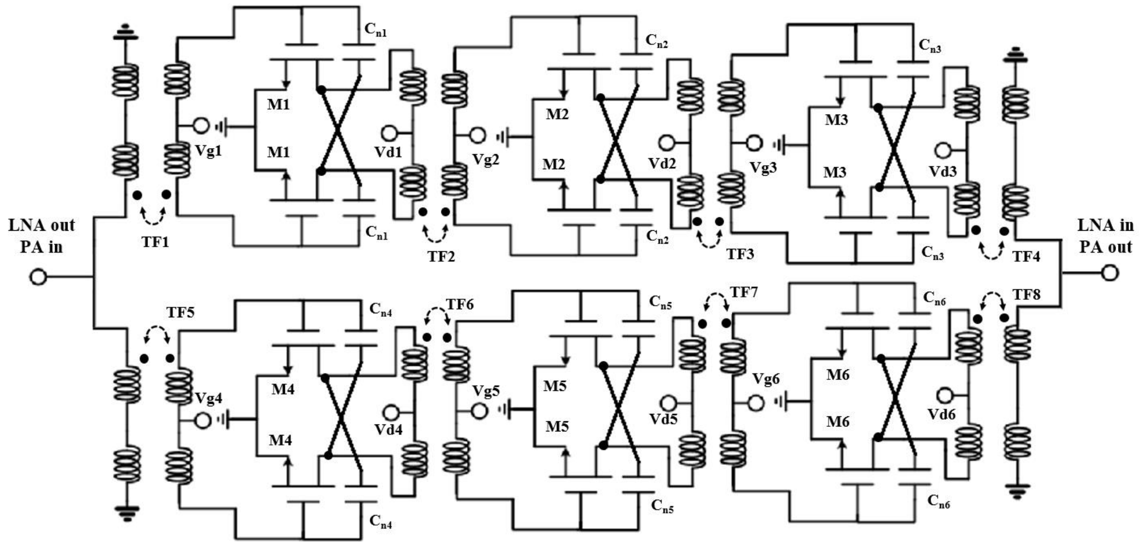
4.3.12 Complete Schematic of Switchless Bidirectional PA-LNA



M1 = 2 x (1 μm x 12 fingers)	C_{n1} = 10 fF
M2 = 2 x (2 μm x 12 fingers)	C_{n2} = 24 fF
M3 = 4 x (2 μm x 12 fingers)	C_{n3} = 48 fF
M4 = 2 x (2 μm x 10 fingers)	C_{n4} = 15 fF
M5 = 2 x (2 μm x 8 fingers)	C_{n5} = 12 fF
M6 = 2 x (2 μm x 10 fingers)	C_{n6} = 15 fF

Mode		
PA-Mode	Vg1=Vg2=Vg3=0.65 V Vd1=Vd2=Vd3=1.2 V	Vg4=Vg5=Vg6=0 V Vd4=Vd5=Vd6=0 V
LNA-Mode	Vg1=Vg2=Vg3=0 V Vd1=Vd2=Vd3=0 V	Vg4=Vg5=Vg6=0.5 V Vd4=Vd5=Vd6=1.0 V

Fig. 4.37. Total Schematic of the propose W-band switchless bidirectional PA-LNA.

After the PA and LNA are fully designed, the PA input/output and LNA output/input can connect together and then make some fine adjustments to the transformer matching network. Fig. 4.37 shows the complete circuit schematic of the proposed PA-

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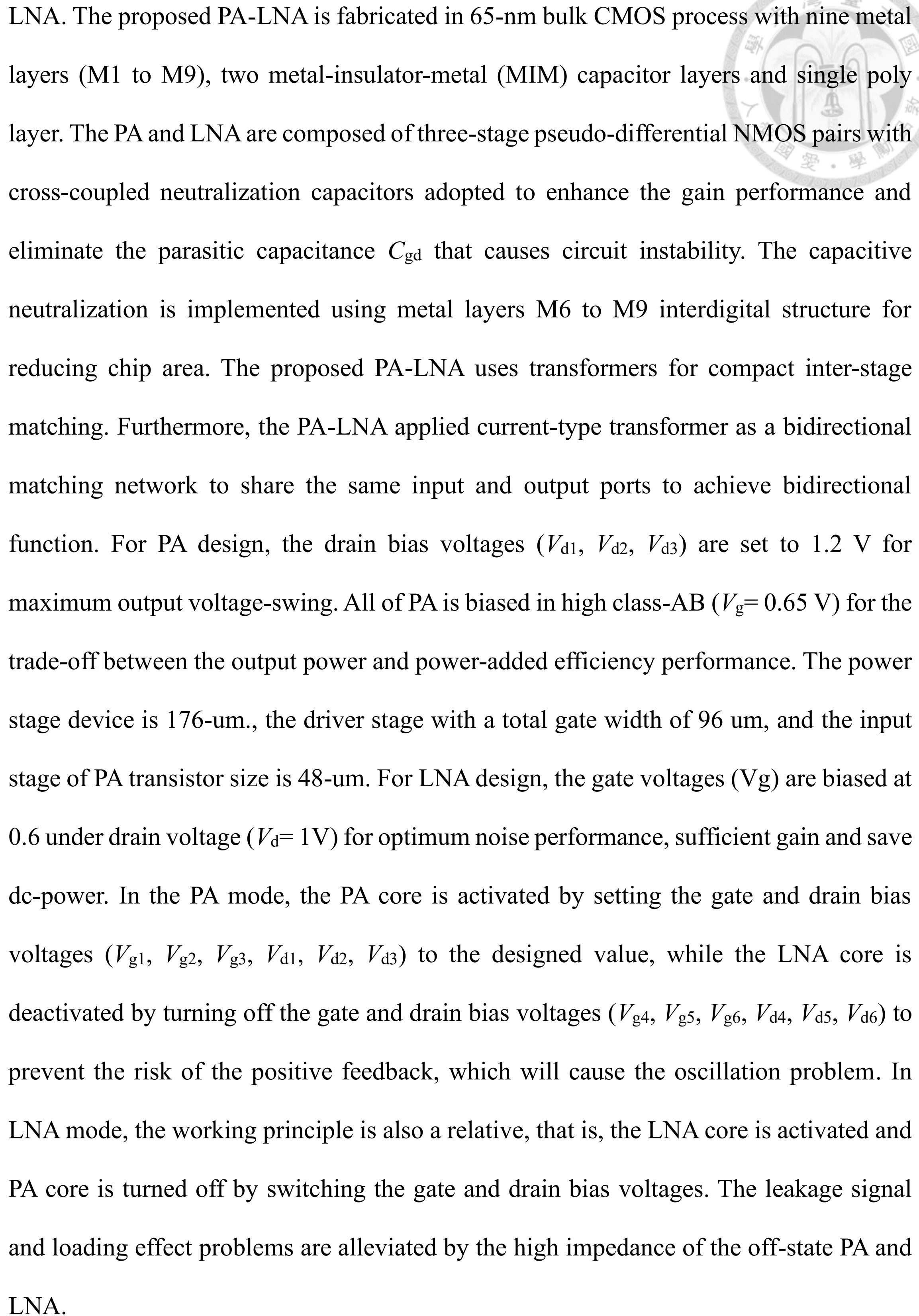

LNA. The proposed PA-LNA is fabricated in 65-nm bulk CMOS process with nine metal layers (M1 to M9), two metal-insulator-metal (MIM) capacitor layers and single poly layer. The PA and LNA are composed of three-stage pseudo-differential NMOS pairs with cross-coupled neutralization capacitors adopted to enhance the gain performance and eliminate the parasitic capacitance C_{gd} that causes circuit instability. The capacitive neutralization is implemented using metal layers M6 to M9 interdigital structure for reducing chip area. The proposed PA-LNA uses transformers for compact inter-stage matching. Furthermore, the PA-LNA applied current-type transformer as a bidirectional matching network to share the same input and output ports to achieve bidirectional function. For PA design, the drain bias voltages (V_{d1}, V_{d2}, V_{d3}) are set to 1.2 V for maximum output voltage-swing. All of PA is biased in high class-AB (V_g= 0.65 V) for the trade-off between the output power and power-added efficiency performance. The power stage device is 176-um., the driver stage with a total gate width of 96 um, and the input stage of PA transistor size is 48-um. For LNA design, the gate voltages (Vg) are biased at 0.6 under drain voltage (V_d= 1V) for optimum noise performance, sufficient gain and save dc-power. In the PA mode, the PA core is activated by setting the gate and drain bias voltages (V_{g1}, V_{g2}, V_{g3}, V_{d1}, V_{d2}, V_{d3}) to the designed value, while the LNA core is deactivated by turning off the gate and drain bias voltages (V_{g4}, V_{g5}, V_{g6}, V_{d4}, V_{d5}, V_{d6}) to prevent the risk of the positive feedback, which will cause the oscillation problem. In LNA mode, the working principle is also a relative, that is, the LNA core is activated and PA core is turned off by switching the gate and drain bias voltages. The leakage signal and loading effect problems are alleviated by the high impedance of the off-state PA and LNA.

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4.3.13 Simulation Result and Post-layout

All of the passive components are simulated in Sonnet EM simulator and the post-layout simulation is done using Advanced Design System (ADS). The total quiescent dc power in LNA mode is 53 mW and in PA mode is 134 mW. The post-simulated S-parameters and noise figure of the PA-LNA in LNA mode are exhibited in Fig. 4.38 and Fig. 4.39. The simulations show the peak gain of 17 dB at 80 GHz, noise figure of 7 dB at 80 GHz, and the 22 GHz 3-dB bandwidth (70-90 GHz). The post-simulated S-parameters of the proposed PA-LNA in PA mode is shown in Fig. 4.40. The peak small-signal is 16 dB at 80 GHz and the 3-dB bandwidth is from 67 to 90 GHz. The post-simulated large signal continuous-wave (CW) results are demonstrated from Fig. 4.41 to Fig. 4.45, which cover 70 GHz to 95 GHz. Besides, Fig. 4.46 depicts the post-simulated power summary versus carrier frequency. As can be seen, the P_{sat} is greater than 8 dBm from 70 to 90 GHz while $OP1dB$ is over 7 dBm from 70 to 90 GHz. Fig. 4.47 shows the chip layout of the proposed W-band switchless bidirectional PA-LNA. The chip size of this PA-LNA is 0.795 × 0.58 mm².

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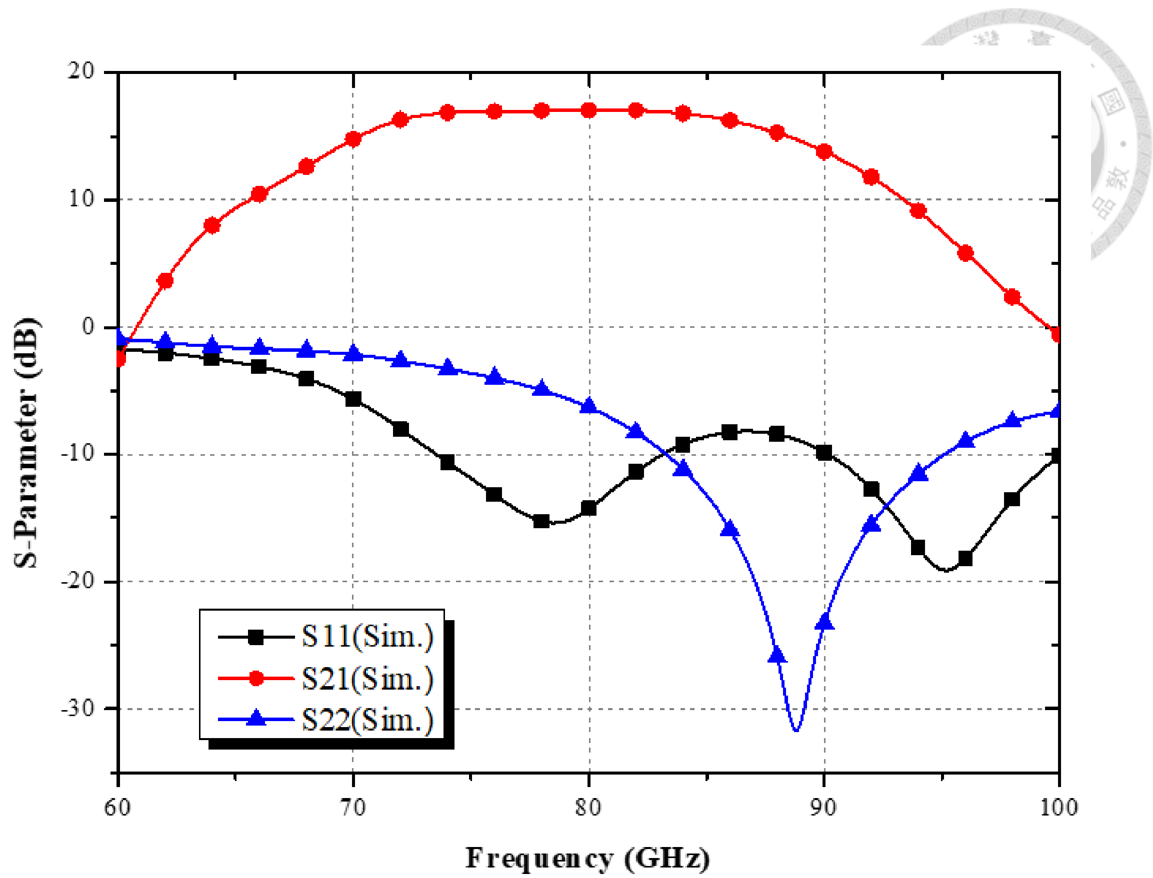

Fig. 4.38. The simulated S-parameters of the proposed PA-LNA in LNA mode.

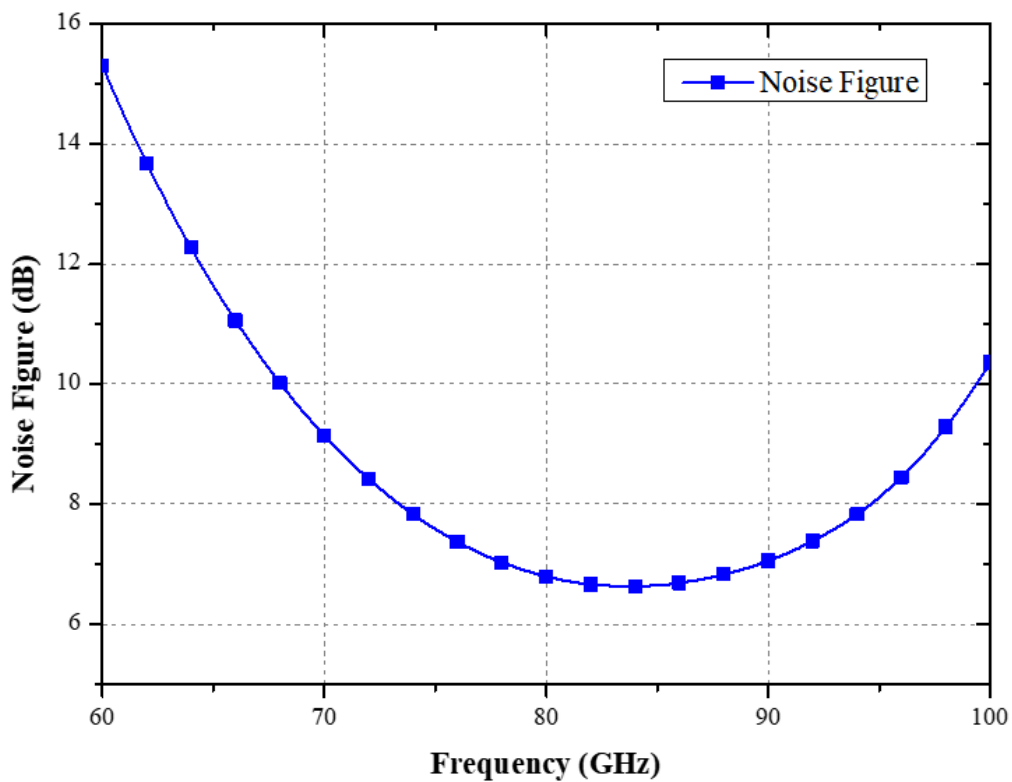

Fig. 4.39. The simulated noise figure of the proposed PA-LNA in LNA mode.

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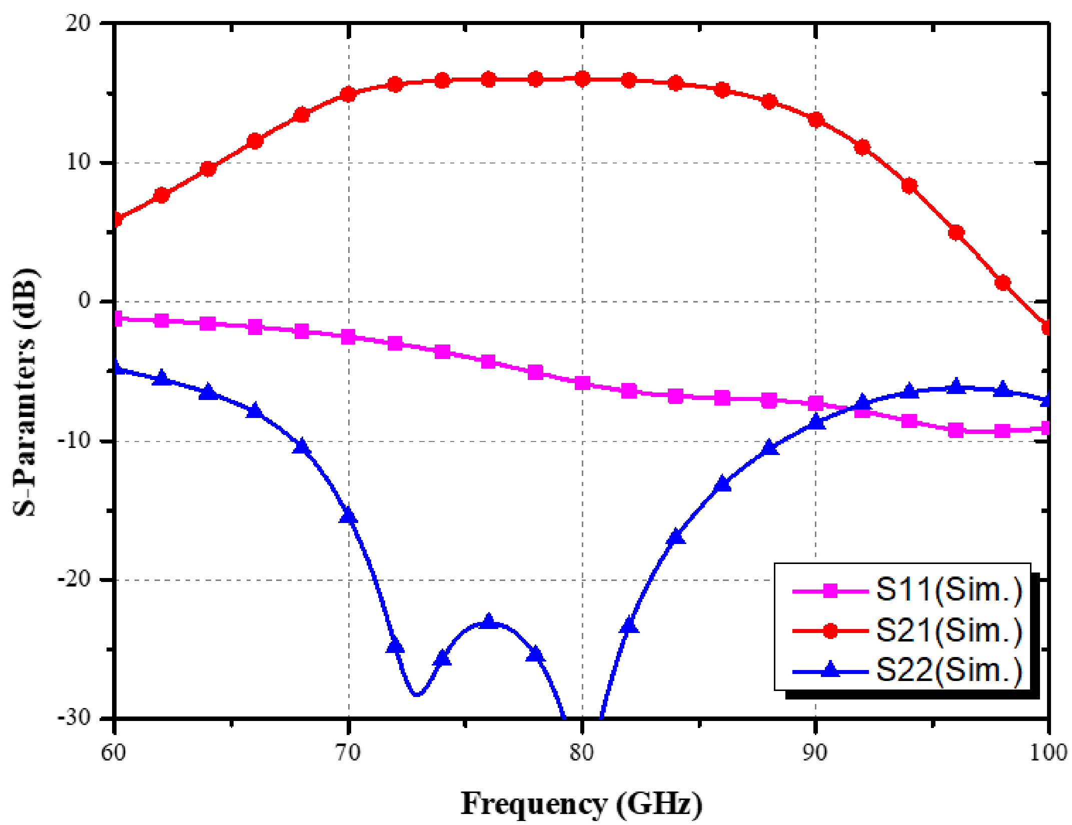

Fig. 4.40. The simulated S-parameters of the proposed PA-LNA in PA mode.

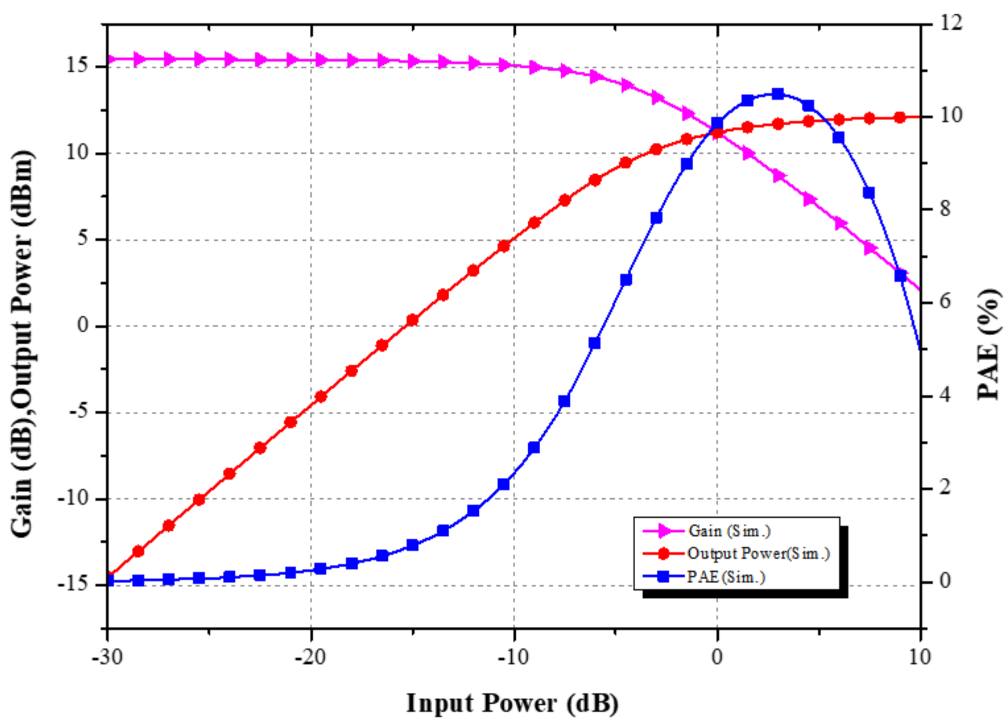

Fig. 4.41. The simulated large-signal results of the proposed PA-LNA in PA mode at 70 GHz.

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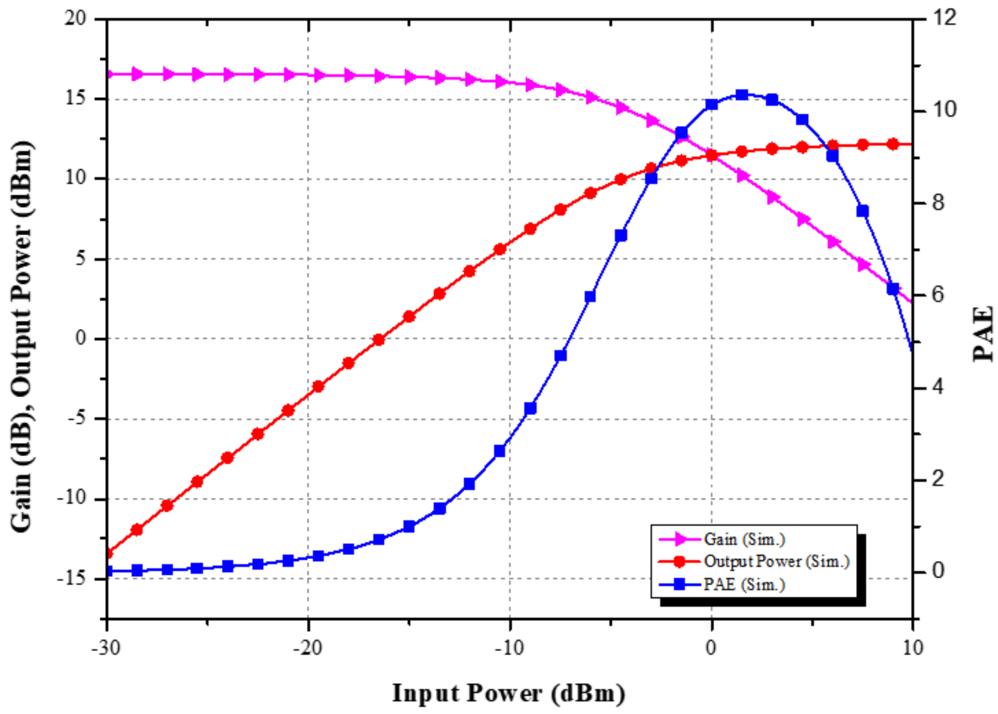

Fig. 4.42. The simulated large-signal results of the proposed PA-LNA in PA mode at 75 GHz.

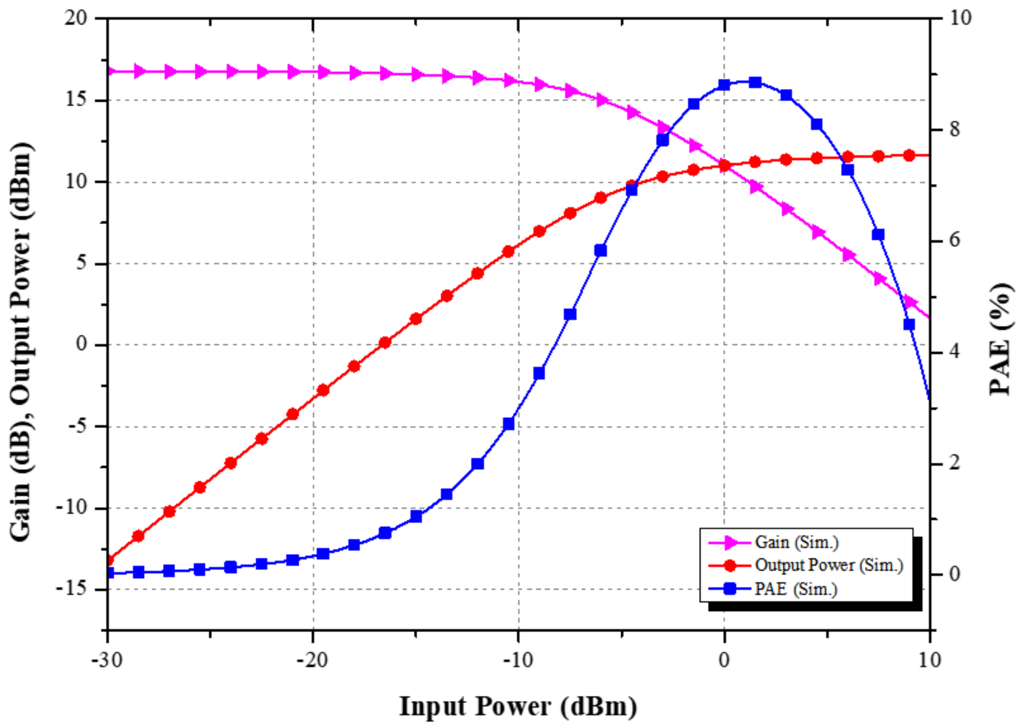

Fig. 4.43. The simulated large-signal results of the proposed PA-LNA in PA mode at 80 GHz.

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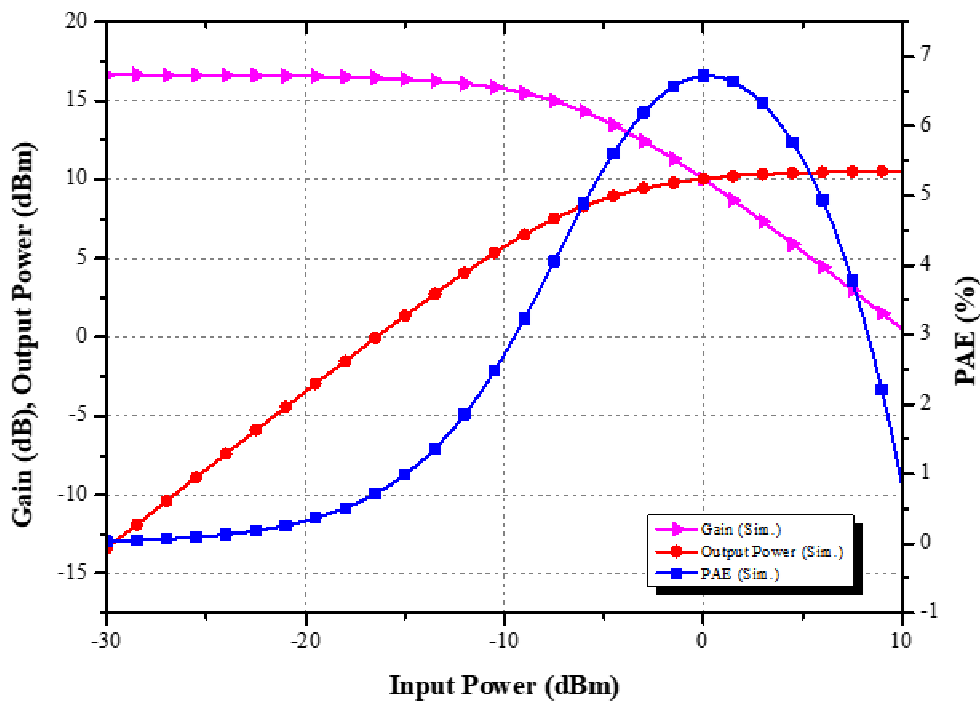

Fig. 4.44. The simulated large-signal results of the proposed PA-LNA in PA mode at 85 GHz.

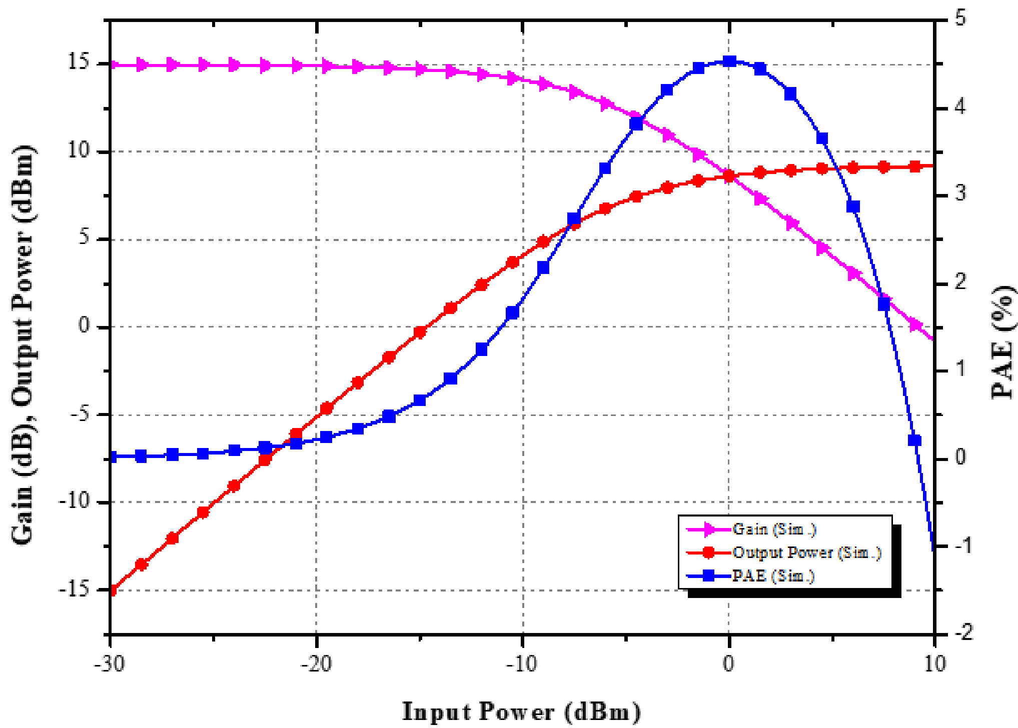

Fig. 4.45. The simulated large-signal results of the proposed PA-LNA in PA mode at 95 GHz.

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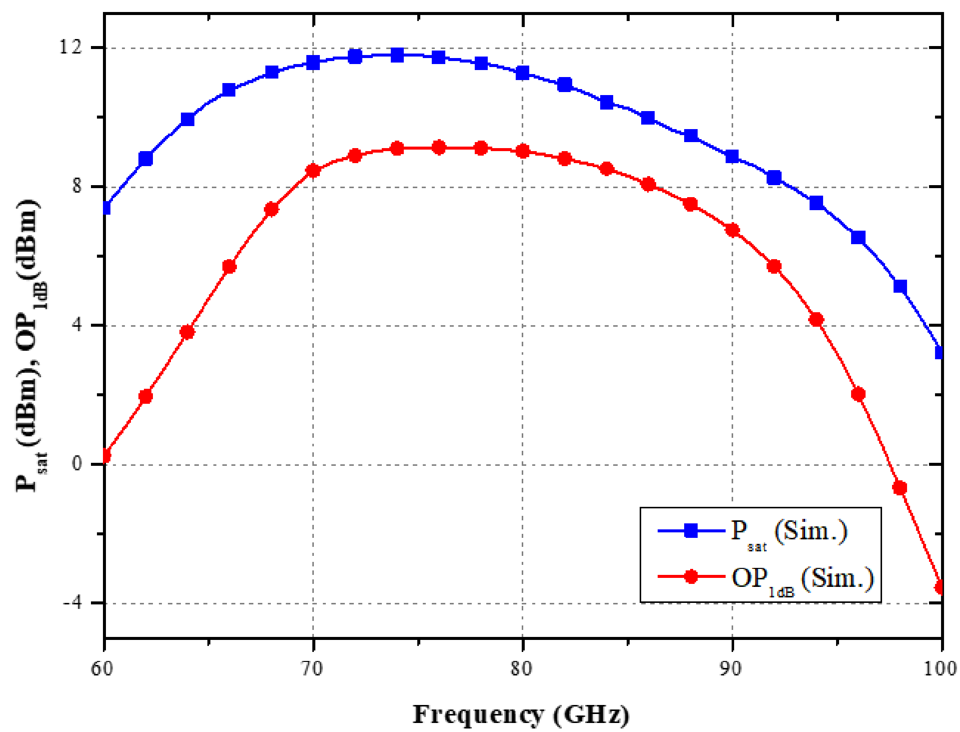

Fig. 4.46. The simulated large-signal CW performance of the proposed PA-LNA from 60 GHz to 100 GHz.

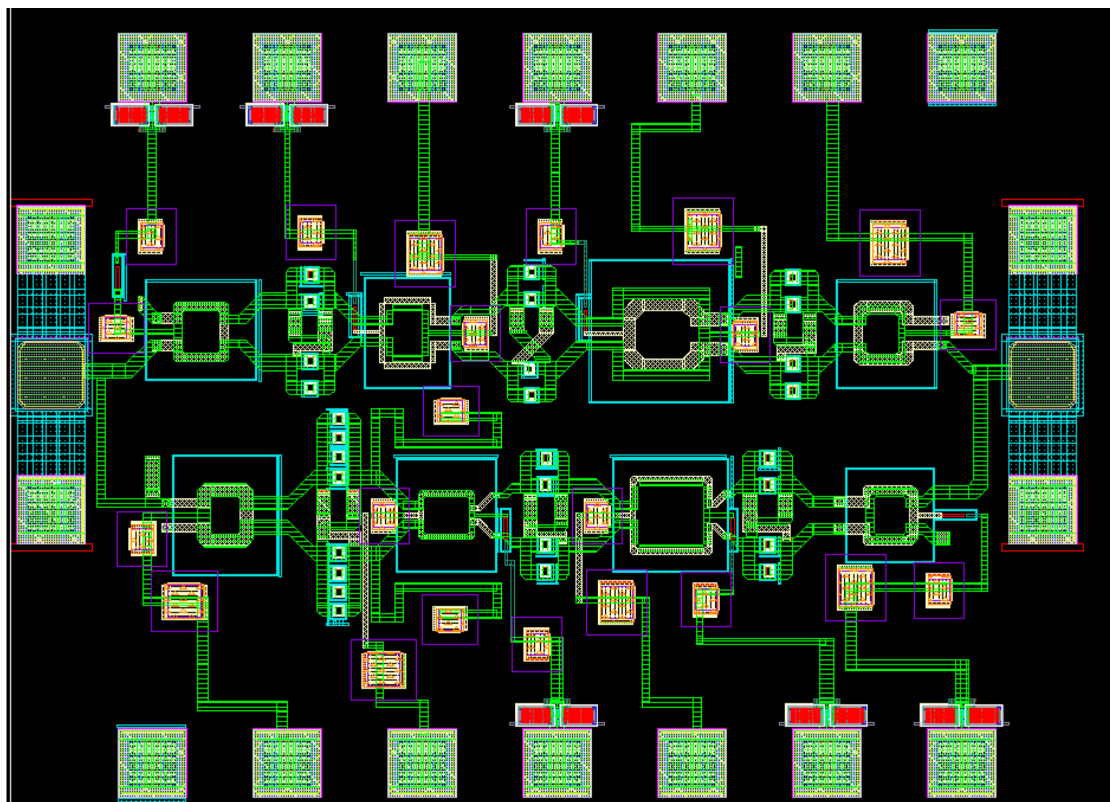

Fig. 4.47. The layout of the proposed W-band switchless bidirectional PA-LNA.

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4.3.14 Experimental Result of the Bidirectional PA-LNA

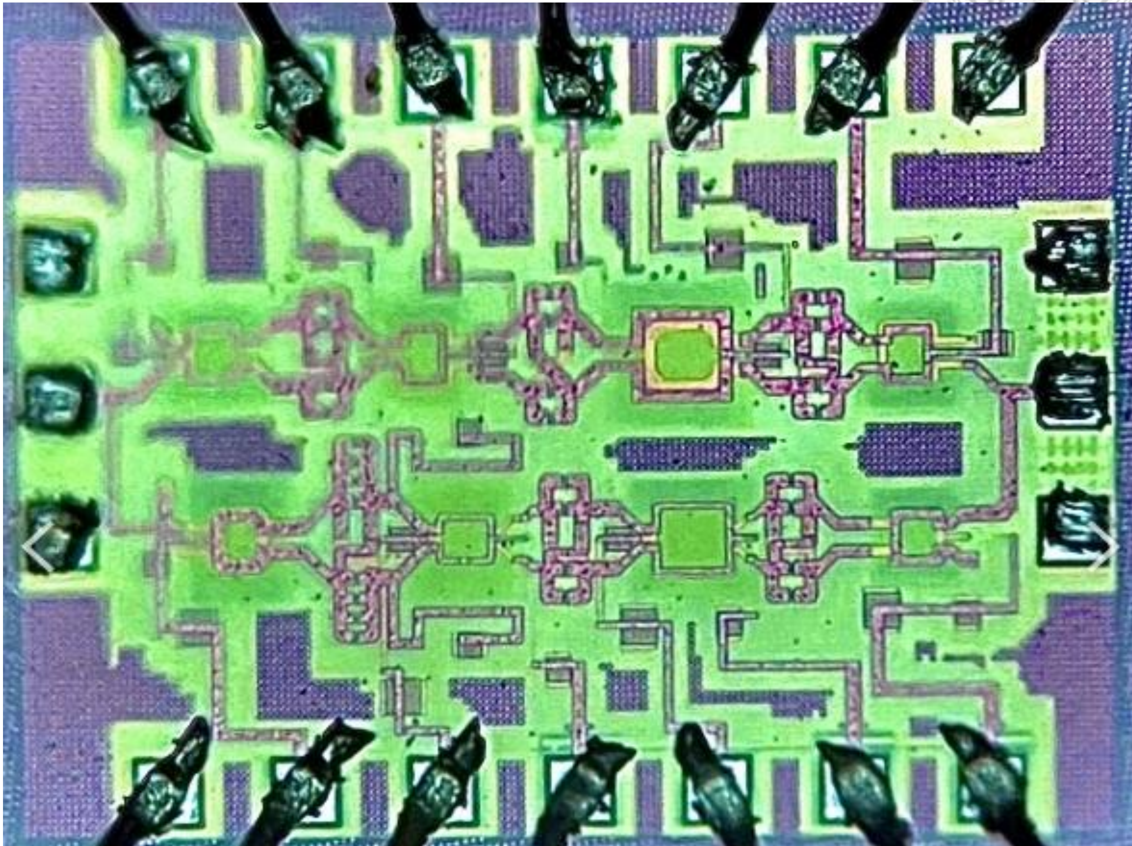

Fig. 4.48. Microphotograph of the proposed PA-LNA.

The proposed PA-LNA is fabricated in 1P9M 65-nm bulk CMOS process with ultra-thick top metal (UTM), and the chip micrograph is shown in Fig. 4.48. The chip size of this circuit is 0.46 mm^2 (0.795 mm × 0.58 mm) including bypass capacitors, dc- and RF-pads. All measurement results were performed on-wafer using GSG RF probes and use bonding-wire to provide dc. The S-parameters are measured with an Anritsu MS46522B VNA. The noise figure is measured by Y-Factor measurement to transfer noise figure. Fig. 4.49. shows the measured and simulated S-parameters of the proposed PA-LNA in LNA mode. The measured peak gain under Pdc of 53 mW is 18.5 dB and the 3-dB bandwidth is 21 GHz covers from 74 to 95 GHz. Fig. 4.50 exhibits the measured and simulated noise

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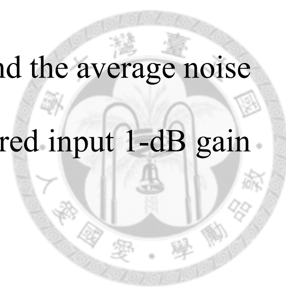
figure in LNA mode. The minimum noise figure is 7 dB at 81 GHz and the average noise figure in the 3-dB bandwidth is 7.8 dB. Fig. 4.51 presents the measured input 1-dB gain compression point (IP1dB) in LNA mode.



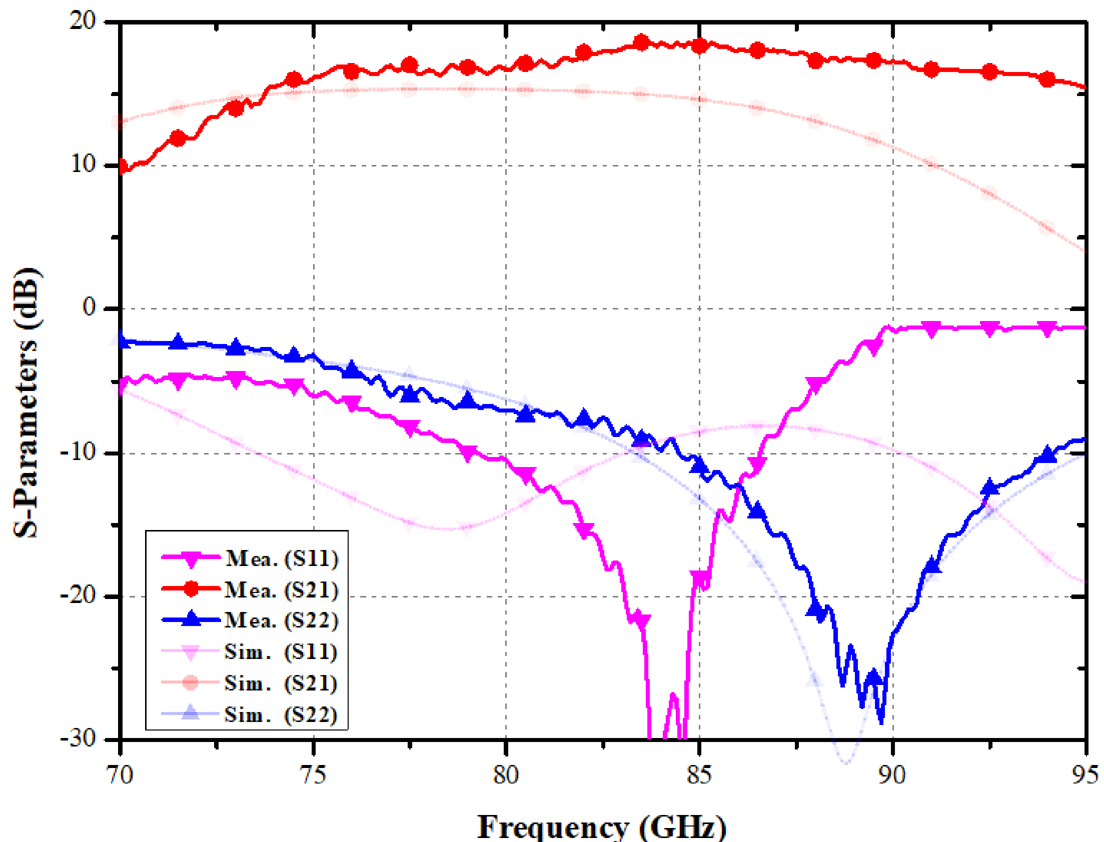


Fig. 4.49. The measured S-parameters of the proposed PA-LNA in LNA mode.

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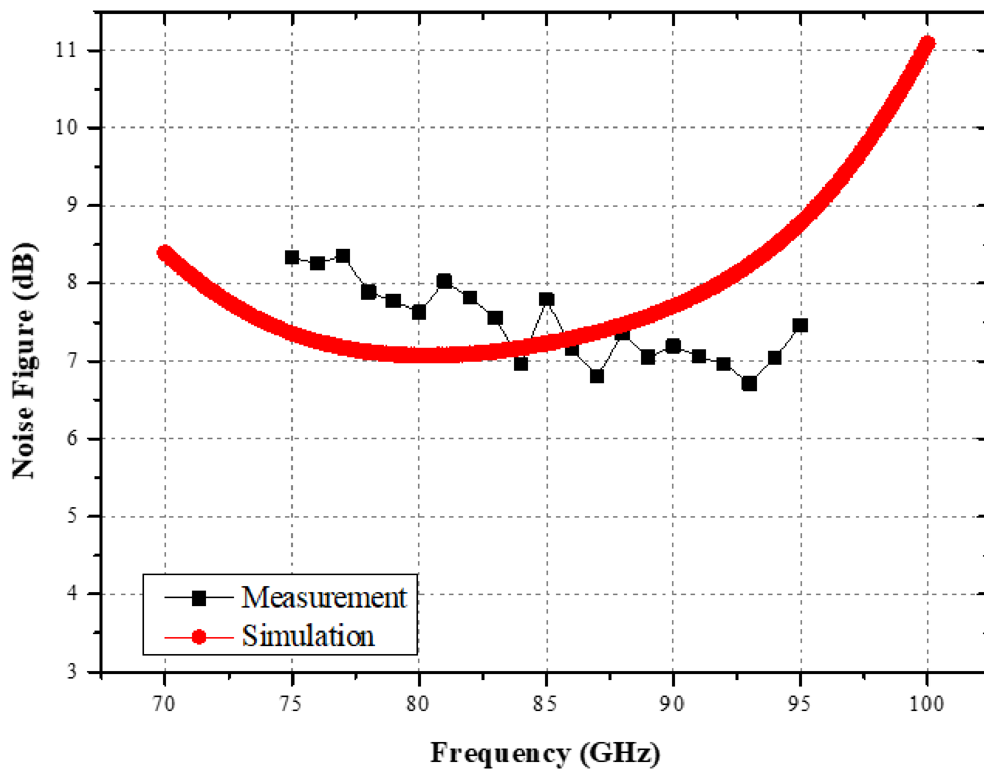

Fig. 4.50. The measured and simulated noise figure of the proposed PA-LNA in LNA mode.

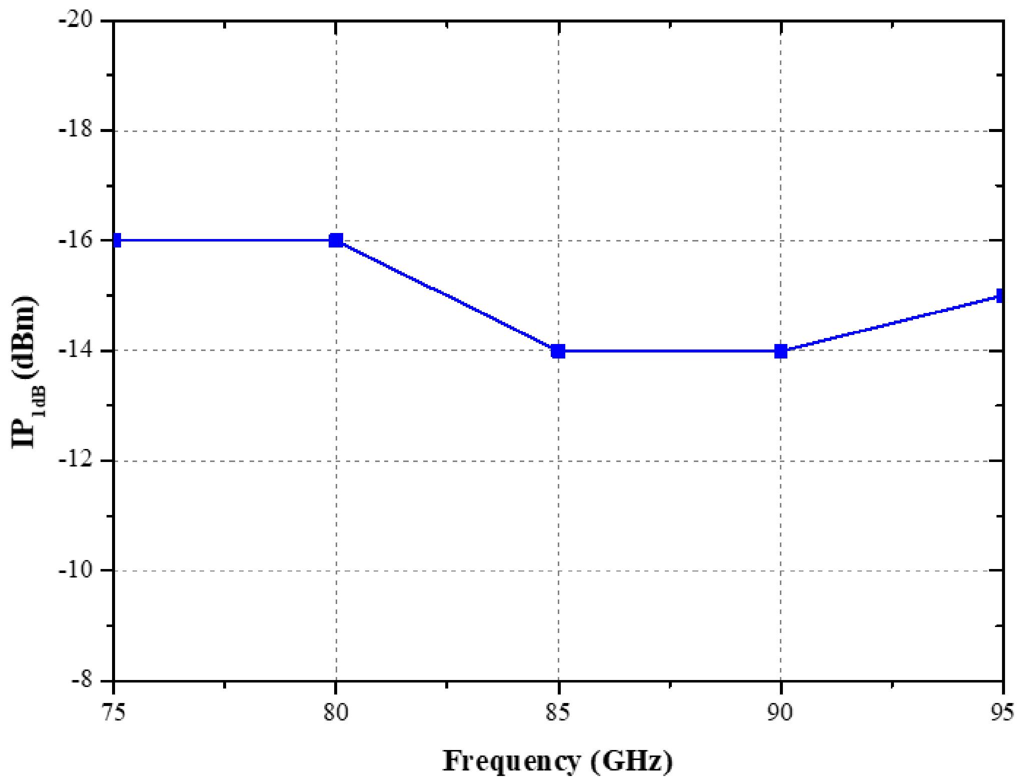

Fig. 4.51. The measured input 1-dB gain compression point (IP_{1dB}) of the proposed PA-LNA in LNA mode

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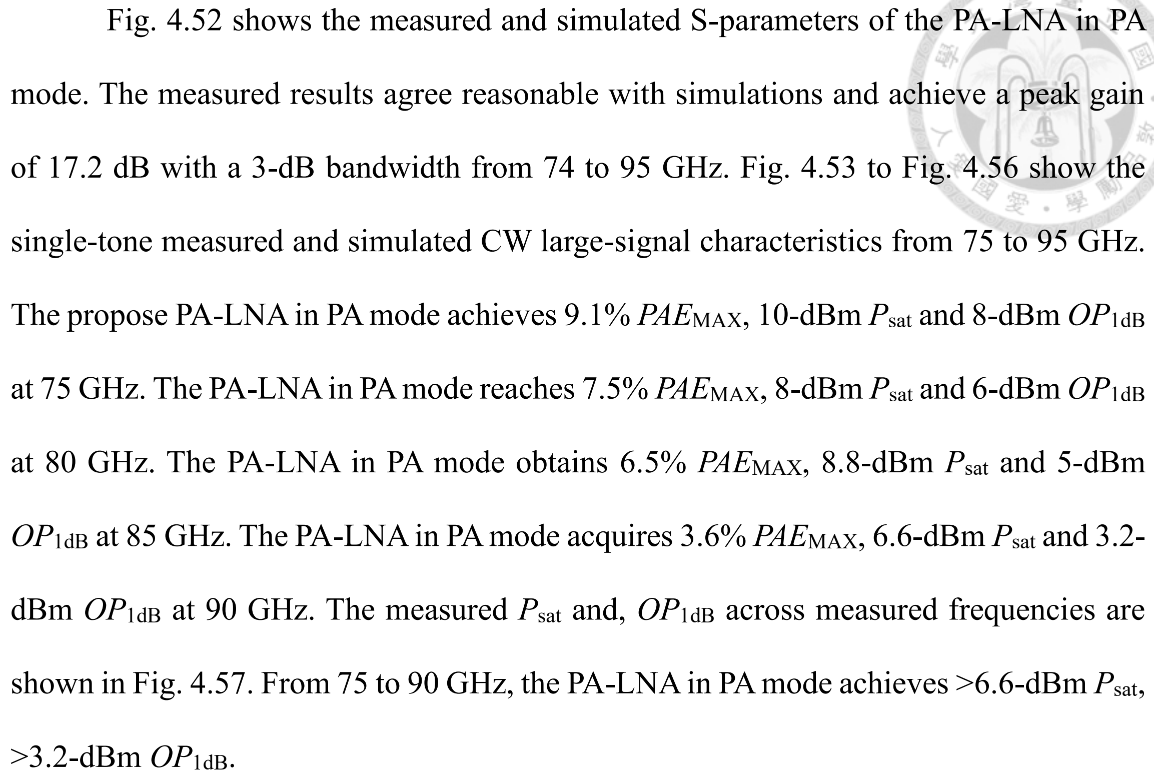

Fig. 4.52 shows the measured and simulated S-parameters of the PA-LNA in PA mode. The measured results agree reasonable with simulations and achieve a peak gain of 17.2 dB with a 3-dB bandwidth from 74 to 95 GHz. Fig. 4.53 to Fig. 4.56 show the single-tone measured and simulated CW large-signal characteristics from 75 to 95 GHz. The propose PA-LNA in PA mode achieves 9.1% PAE_{MAX}, 10-dBm P_{sat} and 8-dBm OP_{1dB} at 75 GHz. The PA-LNA in PA mode reaches 7.5% PAE_{MAX}, 8-dBm P_{sat} and 6-dBm OP_{1dB} at 80 GHz. The PA-LNA in PA mode obtains 6.5% PAE_{MAX}, 8.8-dBm P_{sat} and 5-dBm OP_{1dB} at 85 GHz. The PA-LNA in PA mode acquires 3.6% PAE_{MAX}, 6.6-dBm P_{sat} and 3.2-dBm OP_{1dB} at 90 GHz. The measured P_{sat} and, OP_{1dB} across measured frequencies are shown in Fig. 4.57. From 75 to 90 GHz, the PA-LNA in PA mode achieves $>$6.6-dBm P_{sat}, $>$3.2-dBm OP_{1dB}.

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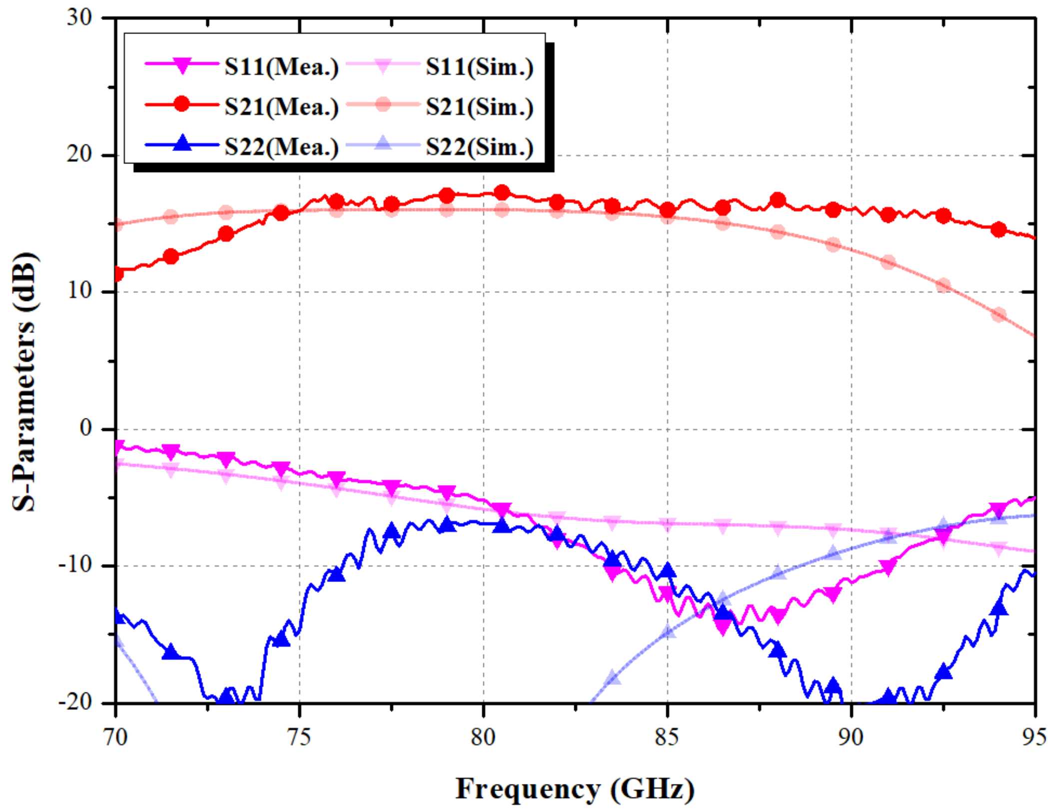

Fig. 4.52. The measured and simulated *S*-parameters of the proposed PA-LNA in PA mode.

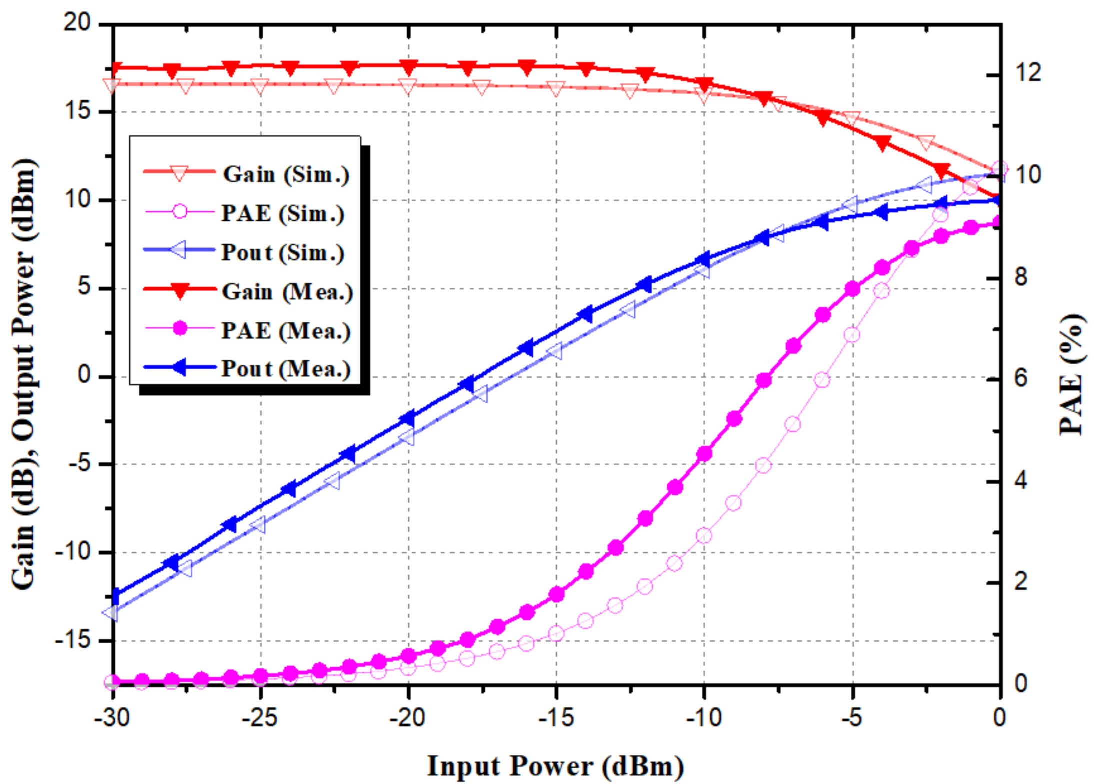

Fig. 4.53. The measured and simulated power performance at 75 GHz in PA mode.

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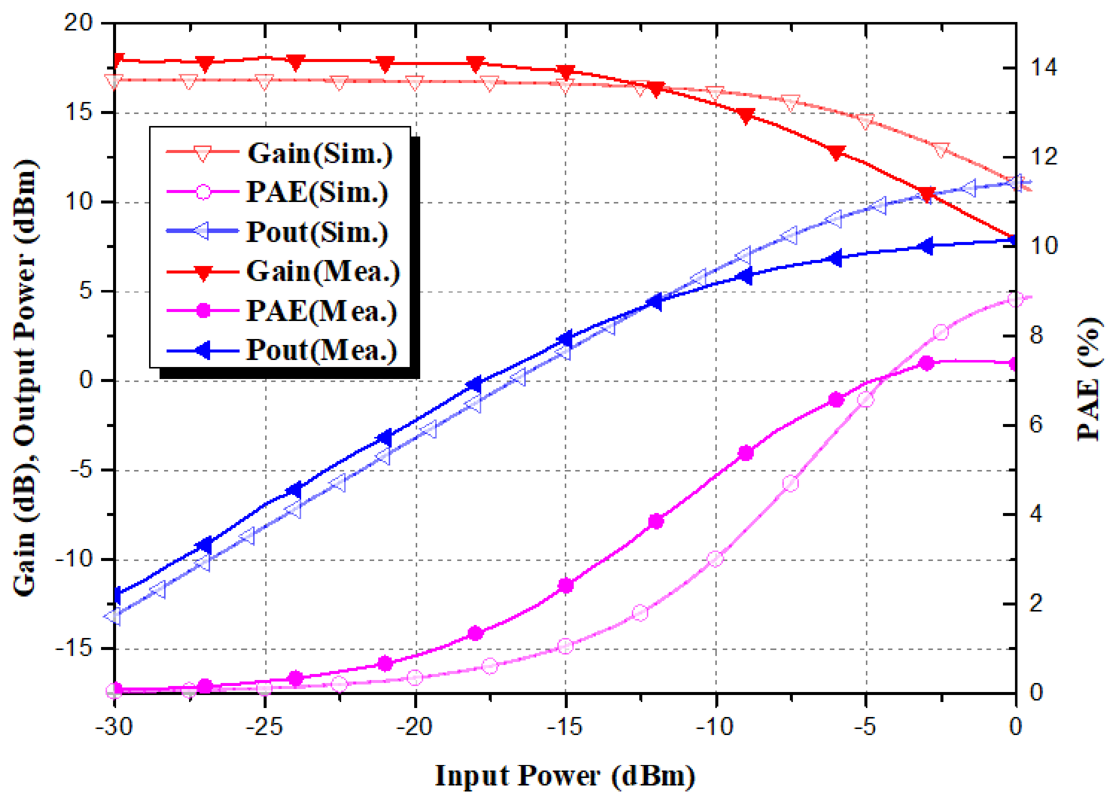

Fig. 4.54. The measured and simulated power performance at 80 GHz in PA mode.

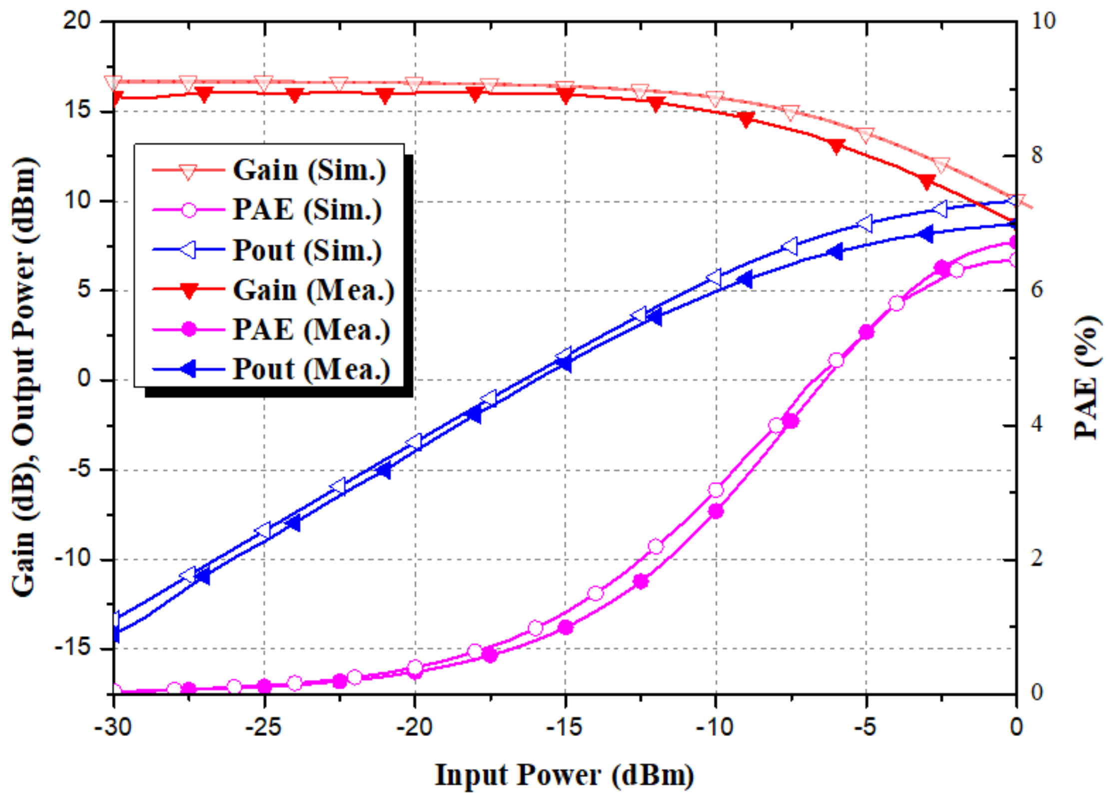

Fig. 4.55. The measured and simulated power performance at 85 GHz in PA mode.

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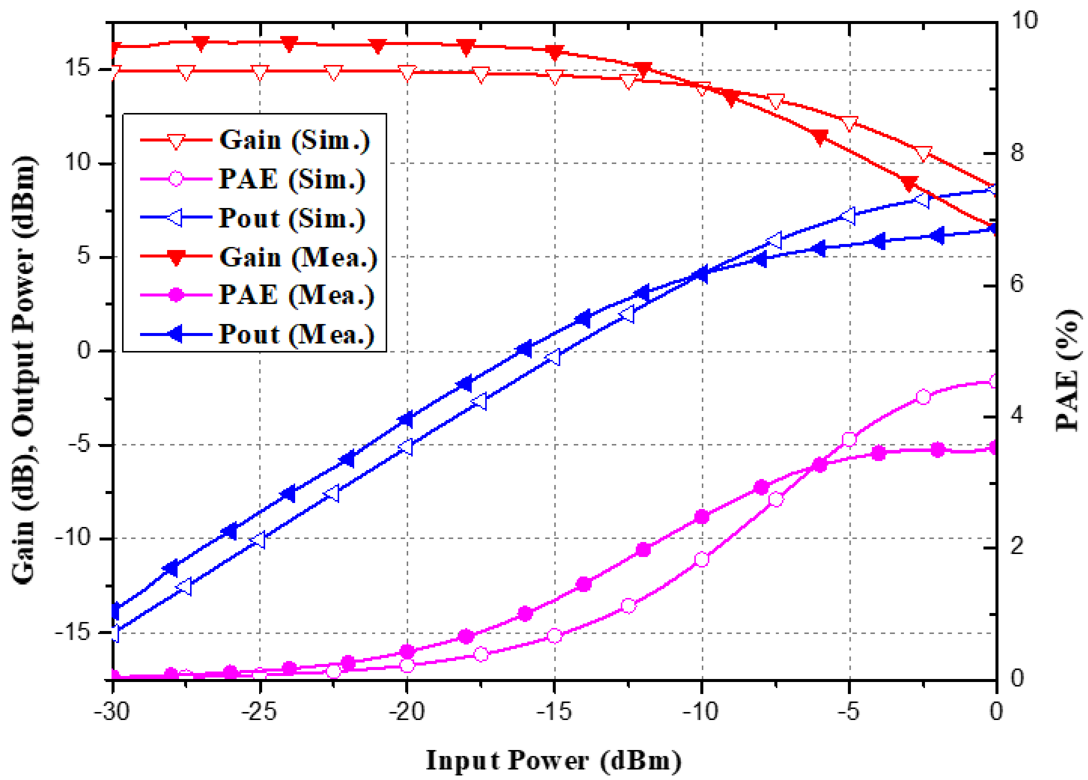

Fig. 4.56. The measured and simulated power performance at 90 GHz in PA mode.

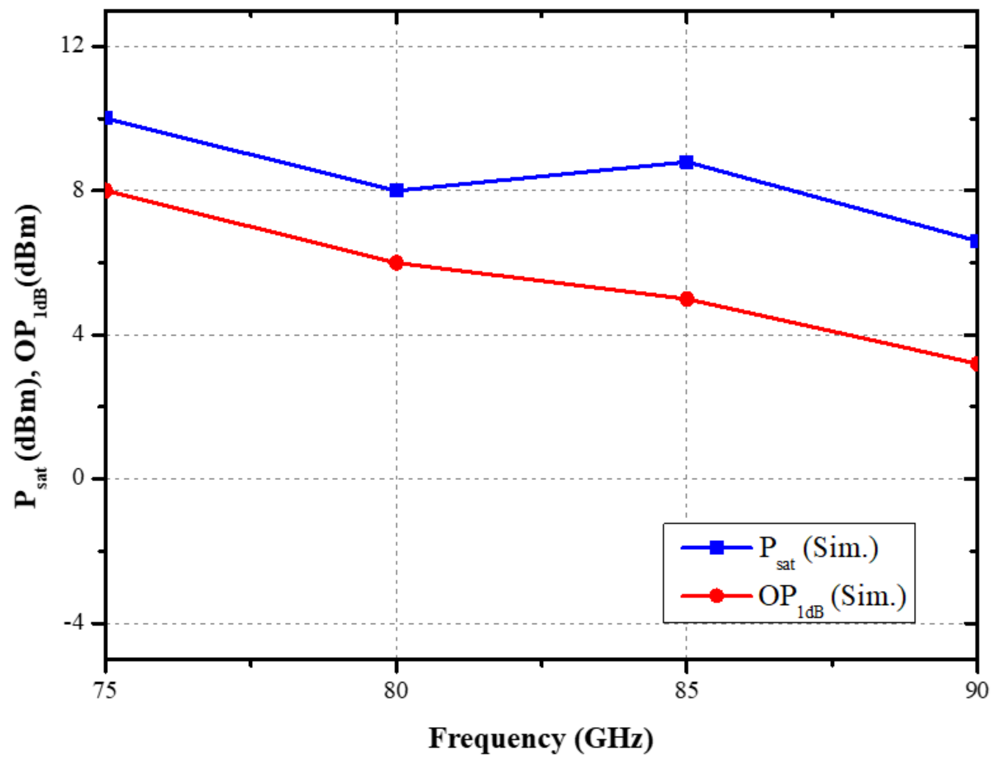

Fig. 4.57. The measured power performance versus RF frequency in PA mode.

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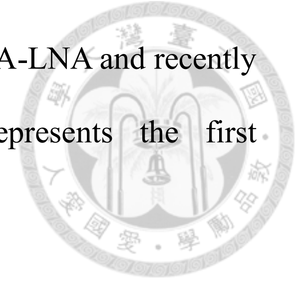

Table 4.2 provides a summary of the performance of both the PA-LNA and recently published bidirectional PA-LNAs. The proposed PA-LNA represents the first implementation of a broadband design operating within the W-band.

Table 4.2 Performance comparison with published PA-LNAs and front-end

Ref.	**[15]**	**[35]**	**[36]**	**[37]**		**This work**
Process	90-nm CMOS	65-nm CMOS	0.13-µm SiGe	0.13-µm SiGe		65-nm CMOS
Topology	Switchless Bi-directional PA-LNA	Switchless Bi-directional PA-LNA	Switchless Bi-directional PA-LNA	Dual-Band Bi-directional PA-LNA		Switchless Bi-directional PA-LNA
3-dB Freq.	29.9~39.4 (PA) 34.5~38.7 (LNA)	58~62.5(PA) 58~67(LNA)	57~66 (PA&LNA)	28~34(PA) 25~35(LNA)	44~65(PA) 55~65(LNA)	73~95(PA) 74~95(LNA)
Tx Peak Gain(dB)	18.1	24.5	16.5	14.1	14.7	17.2
Tx OP_{1db} (dBm)	13.3	N/A	11	14.7	7.2	6 @80 GHz
Tx P_{sat} (dBm)	15.2	8.4	12*	16.3	16	8 @80GHz
Tx PAE_{max} (%)	29	8.7	11	23.6	15.2	7.5 @80 GHz
Rx Peak Gain(dB)	18.1	21.5	17	13.9	14.1	18.6
Rx Min.NF(dB)	4.5	6.7	6.5	4.2	4.6	7
Rx IP_{1db} (dBm)	-16~-20	N/A	-20	-13	-13.5	-11
Rx P_{dc} (mW)	24.7	39.6	36	10	24	53

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4.4 Design of the W-Band bidirectional PA-LNA with switch

In this session, the PA-LNA aims to enhance gain and the three-dB frequency by utilizing a switch to increase the impedance in the off-mode, making it more open. The design goals of this bidirectional PA-LNA are shown in Table 4.3.

Table 4.3 Design goals of the W-Band bidirectional PA-LNA with switch

Bandwidth (GHz)	70-95	Tx Peak Gain	16 dB
Rx Peak Gain	17 dB	Tx P_{sat}	8 dBm
Rx Noise @Min	7 dB	Tx OP_{1dB}	5 dBm
Rx P_{dc}	50 mW	Tx PAE_{MAX} @85 GHz	10%

4.4.1 Circuit Design

The schematic of this bidirectional PA-LNA is shown in Fig. 4.58. It is similar to the schematic of the switchless bidirectional PA-LNA except input matching and output matching. Instead of using transformer to let impedance open, it using switch to let impedance open in off-mode. This bidirectional PA-LNA also uses three stages differential-pair and transformer to compose circuit. Different form switchless version, in this switch version, a single-pole double-throw (SPDT) switch has been incorporated at both the input and output to facilitate the switching of PA/LNA modes. This design modification also guarantees that the impedance remains at a sufficiently high level, preventing any interference with the circuit in another mode.

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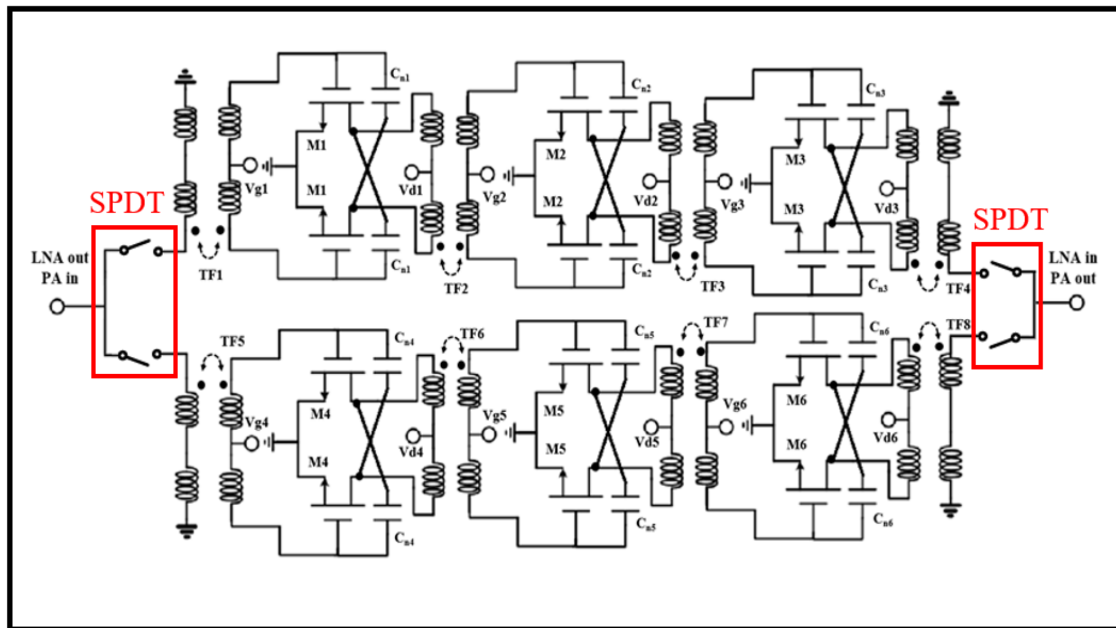

Fig. 4.58. Total Schematic of the propose W-band bidirectional PA-LNA.

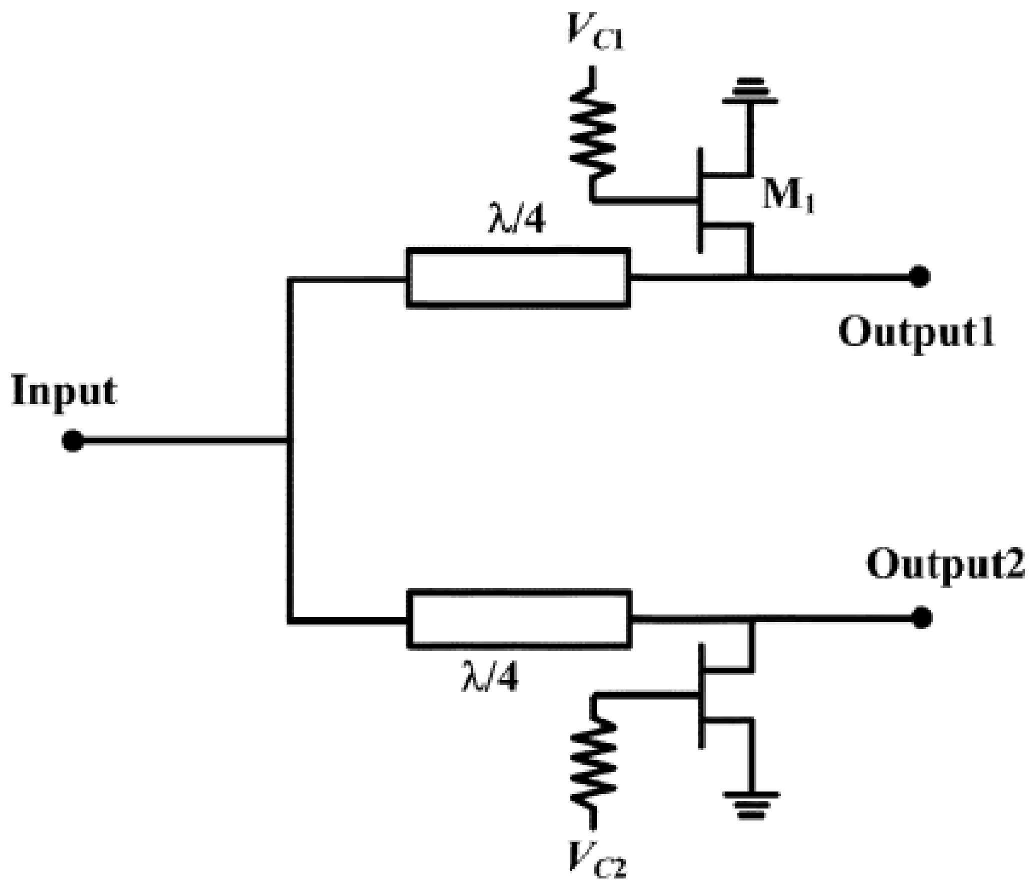

Fig. 4.59. Schematic of the SPDT traveling-wave switch in conjunction with a quarter-wavelength impedance transformer.

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Fig. 4.59 illustrates the complete schematic diagram of the Single-Pole Double-Throw (SPDT) traveling-wave switch. The selection of a 4-finger configuration with an 8-μm device size for the switch design was influenced by its superior insertion loss performance, as evidenced in Fig. 4.60. Moreover, this size configuration achieves isolation levels exceeding 10 dB, as demonstrated in Fig. 4.61. However, the isolation of the SPDT is not large; nevertheless, its purpose is to ensure that the off-mode achieves high impedance. Therefore, 10 dB isolation is sufficient for this work. To create the SPDT switch, two identical Single-Pole Single-Throw (SPST) traveling-wave switch cells and two 50-ohm impedance transformers are employed.

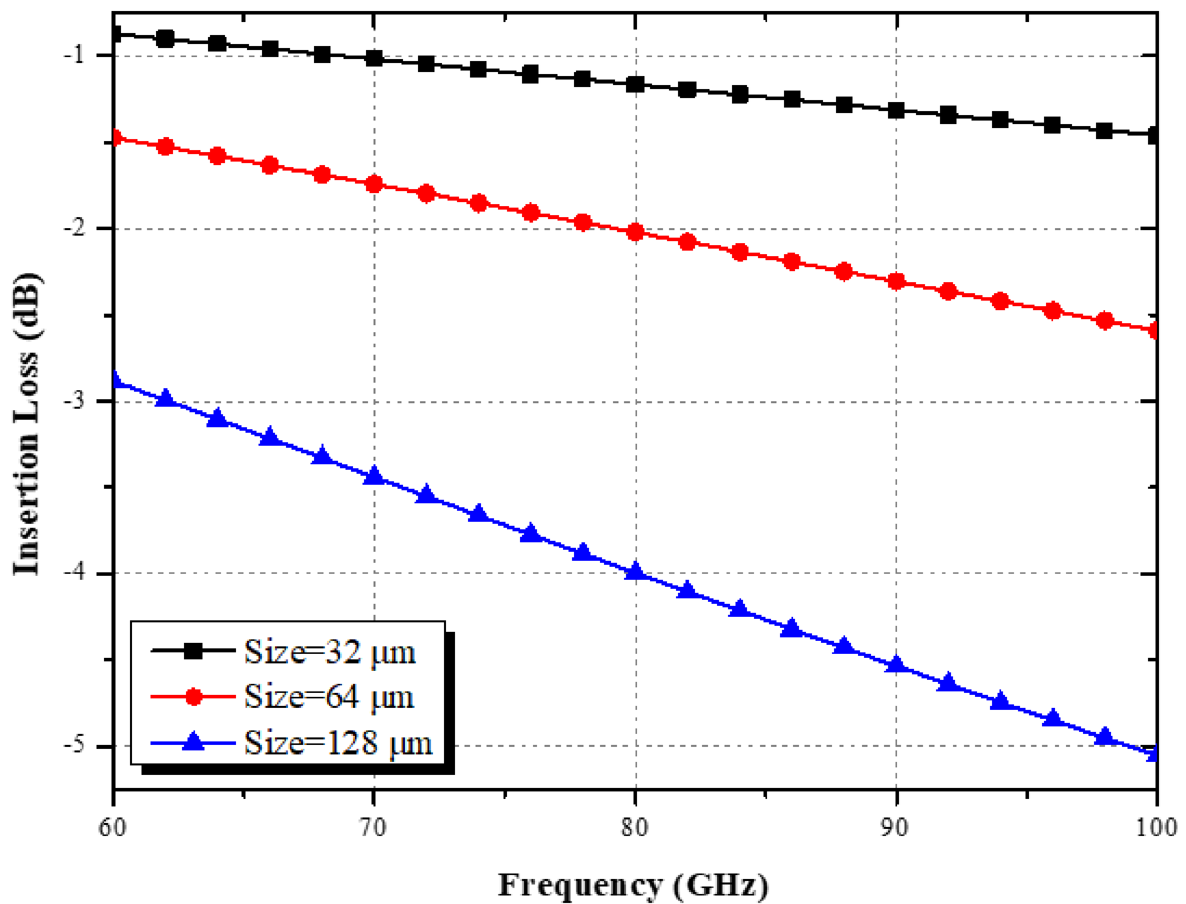

Fig. 4.60. Simulated insertion loss of three-transistor SPST traveling-wave switch with various device sizes.

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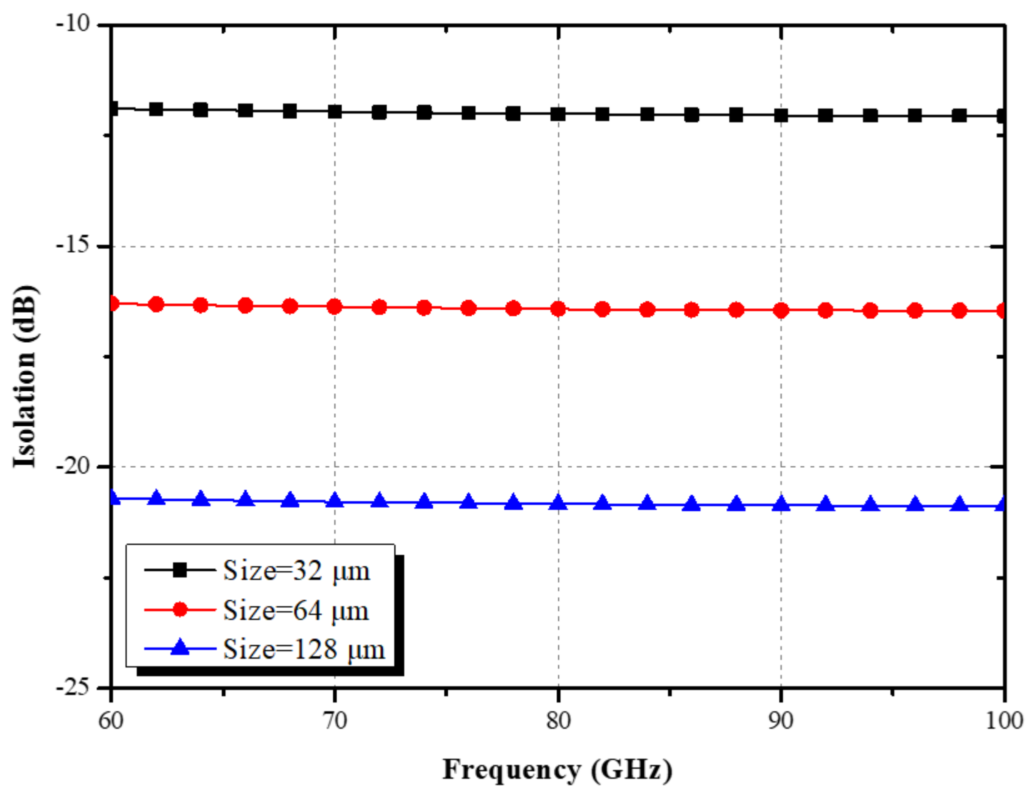

Fig. 4.61. Simulated isolation of three-transistor SPST traveling-wave switch with various device sizes.

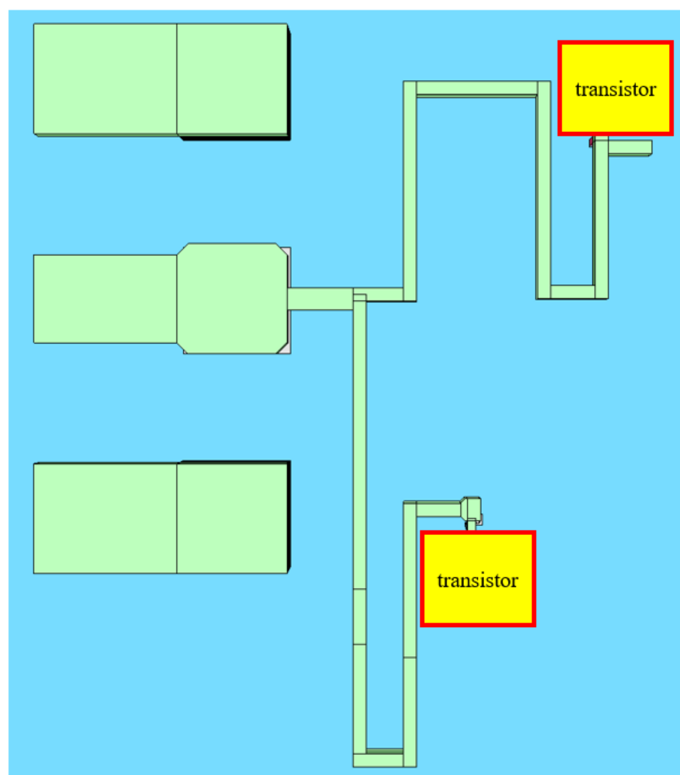

Fig. 4.62. Top view of the SPDT traveling-wave switch in conjunction with a quarter-wavelength impedance transformer.

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Since SPDT is designed in front of input and output matching, we can have more freedom in the design of size and TF. Instead of a switchless version, we need to focus on the impedance of off-mode, which can improve the overall performance of the circuit. As shown in Fig. 4.63, the loss caused by the output matching of PA mode in the version with switch is about 0.5 dB better than the version without switch. However, in Fig. 4.64, the LNA input matching also shows similar results. Because there is no need to consider the impedance of off mode, the matching loss of the switch version is smaller than switchless. Since the SPDT is integrated into both input and output matching, it is crucial to consider its linearity. Fig. 4.65 presents simulated large-signal results for the SPDT, indicating an OP_{1dB} of 10 dBm, larger than the PA's OP_{1dB}. Consequently, the SPDT does not impact the performance of the PA.

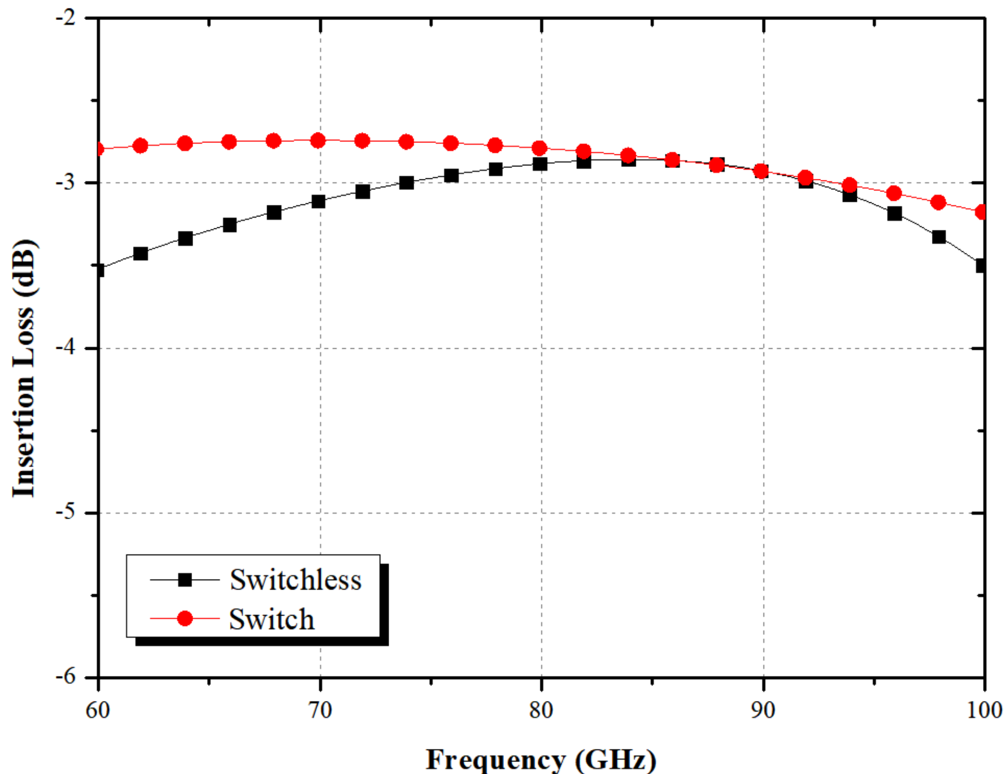

Fig. 4.63. The insertion loss of PA output matching for with/without switch version.

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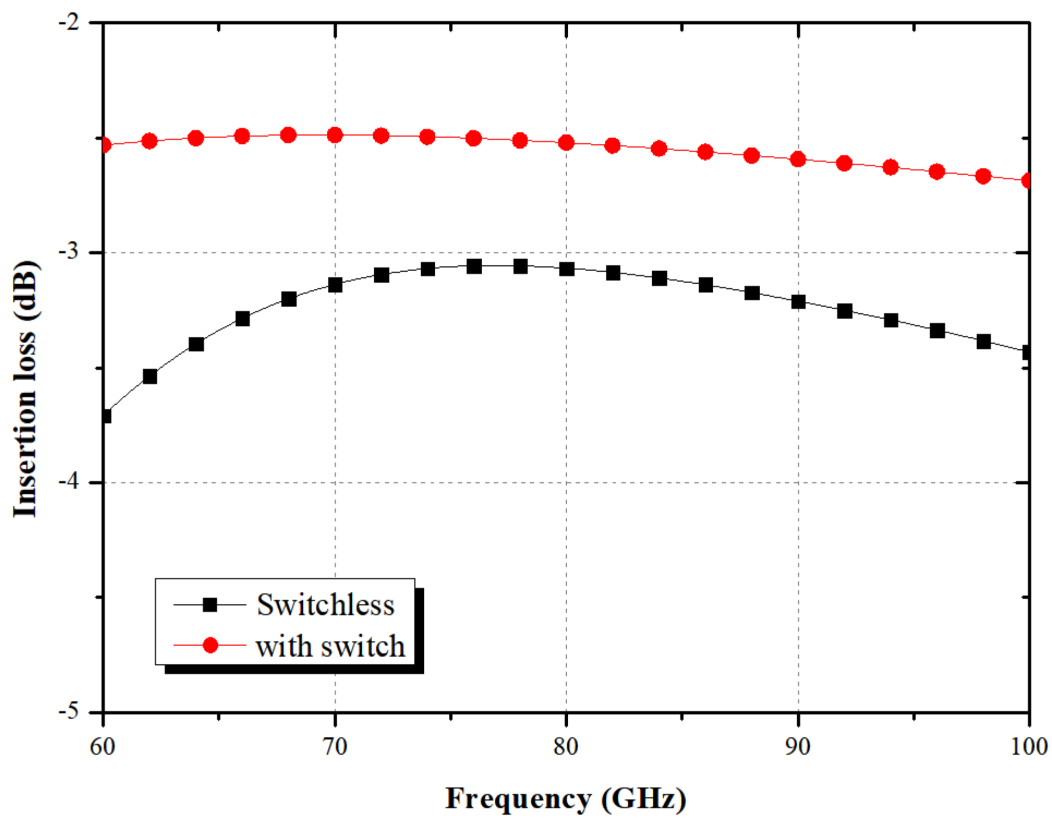

Fig. 4.64. The insertion loss of LNA input matching for with/without switch version.

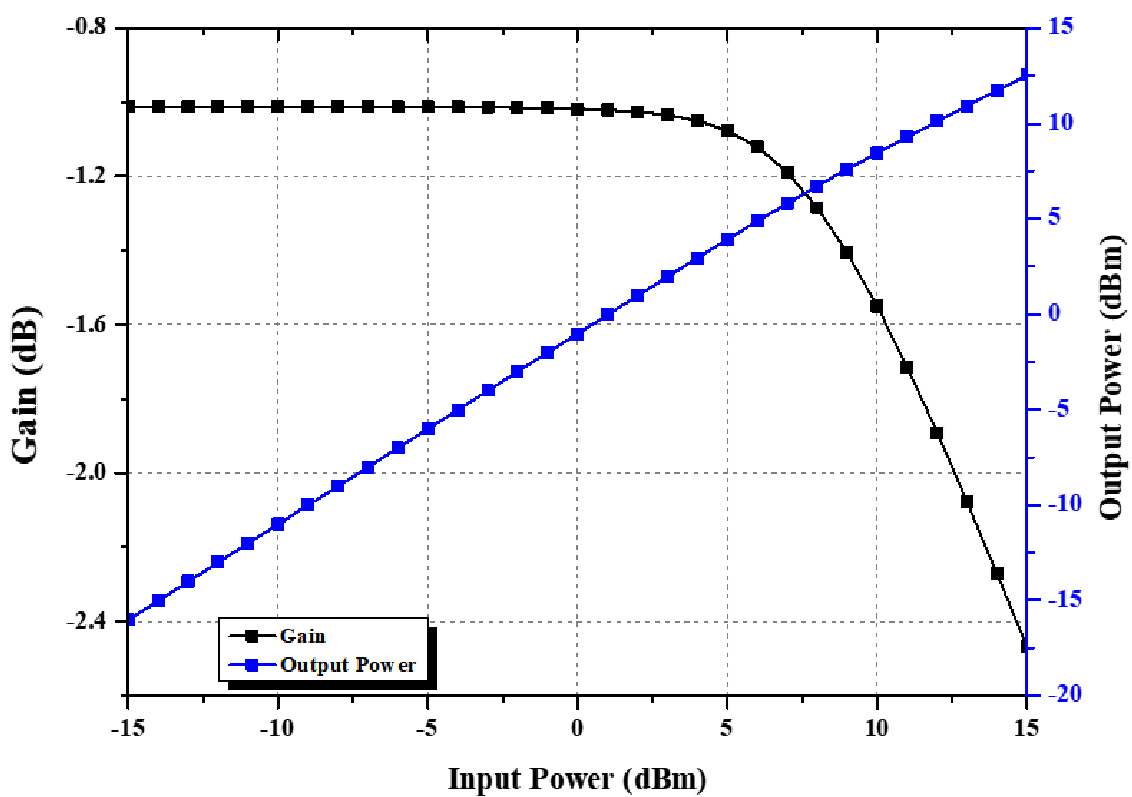

Fig. 4.65 The simulated large-signal results of the SPDT.

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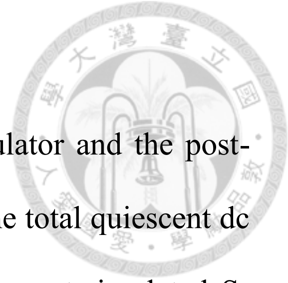
4.4.2 Switch Bidirectional PA-LNA Simulated Result



All the passive components are simulated in Sonnet EM simulator and the post-layout simulation is done using Advanced Design System (ADS). The total quiescent dc power in LNA mode is 52 mW and in PA mode is 134 mW. The post-simulated S-parameters and noise figure of the PA-LNA in LNA mode are exhibited in Fig. 4.66 and Fig. 4.67. The simulations show the peak gain of 17.4 dB at 73 GHz, noise figure of 6.8 dB at 77 GHz, and the 28 GHz 3-dB bandwidth (67-95 GHz). The post-simulated S-parameters of the proposed PA-LNA in PA mode is shown in Fig. 4.68. The peak small-signal is 16.4 dB at 72 GHz and the 3-dB bandwidth is from 66.5 to 95 GHz. The post-simulated large signal continuous-wave (CW) results are demonstrated from Fig. 4.69 to Fig. 4.73, which cover 70 GHz to 90 GHz. Besides, Fig. 4.74 depicts the post-simulated power summary versus carrier frequency. As can be seen, the P_{sat} is greater than 7.5 dBm from 70 to 95 GHz while OP_{1dB} is over 4 dBm from 70 to 95 GHz. Fig. 4.75 shows the chip layout of the proposed W-band switchless bidirectional PA-LNA. The chip size of this PA-LNA is 0.93 × 0.6 mm².

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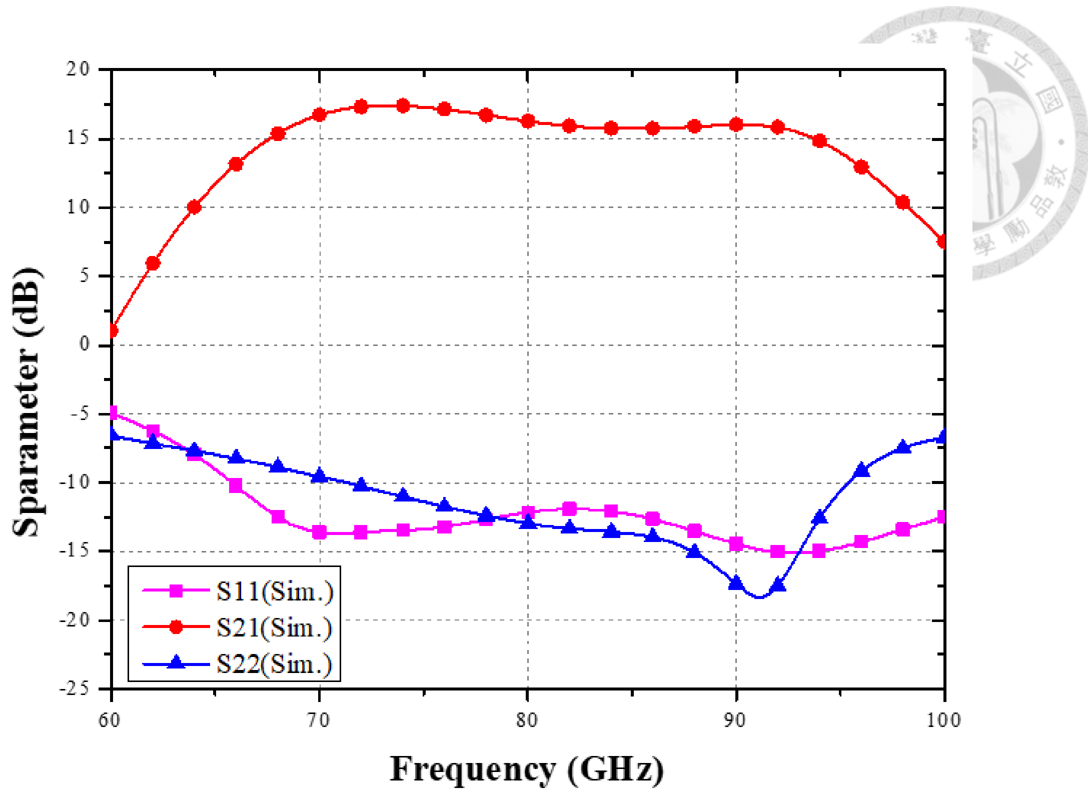

Fig. 4.66. The simulated S-parameters of the proposed switch PA-LNA in LNA mode.

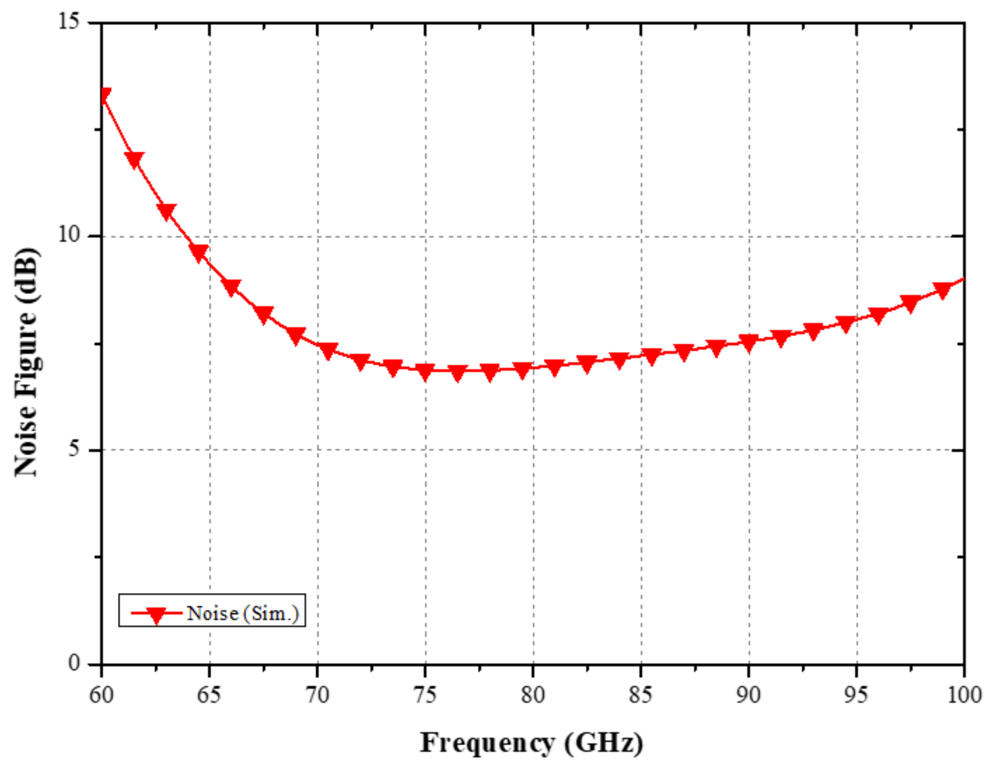

Fig. 4.67. The simulated noise figure of the proposed switch PA-LNA in LNA mode.

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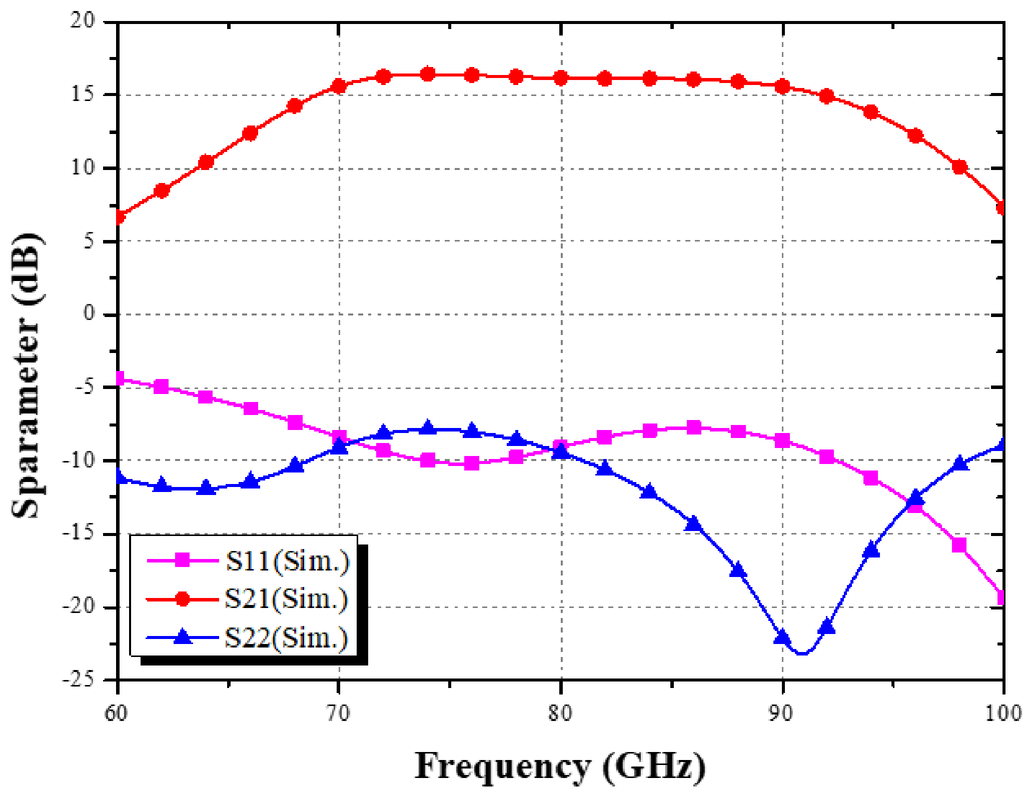

Fig. 4.68. The simulated S-parameters of the proposed switch PA-LNA in PA mode.

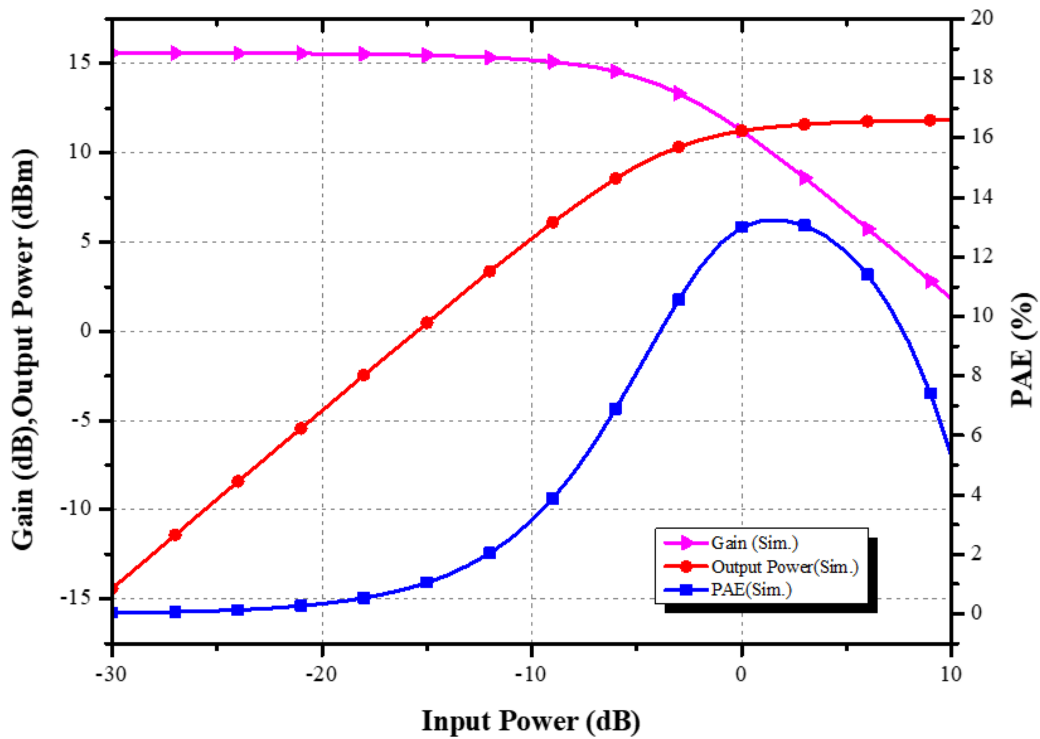

Fig. 4.69. The simulated large-signal results of the proposed switch PA-LNA in PA mode at 70 GHz.

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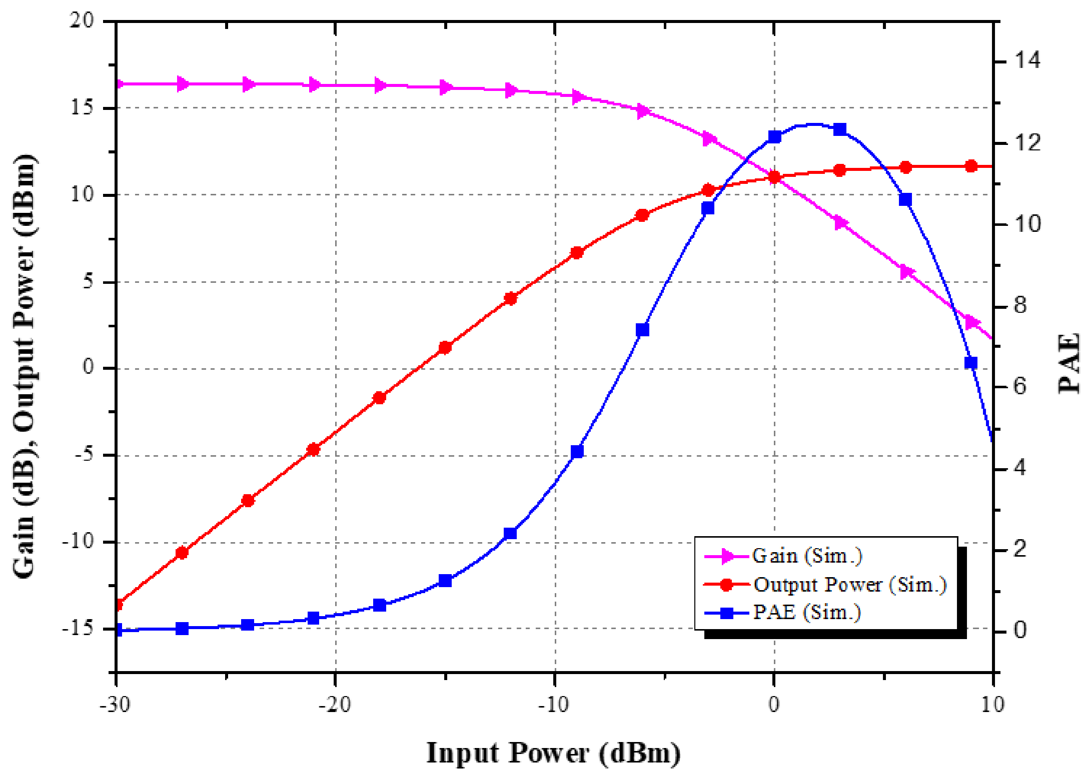

Fig. 4.70. The simulated large-signal results of the proposed switch PA-LNA in PA mode at 75 GHz.

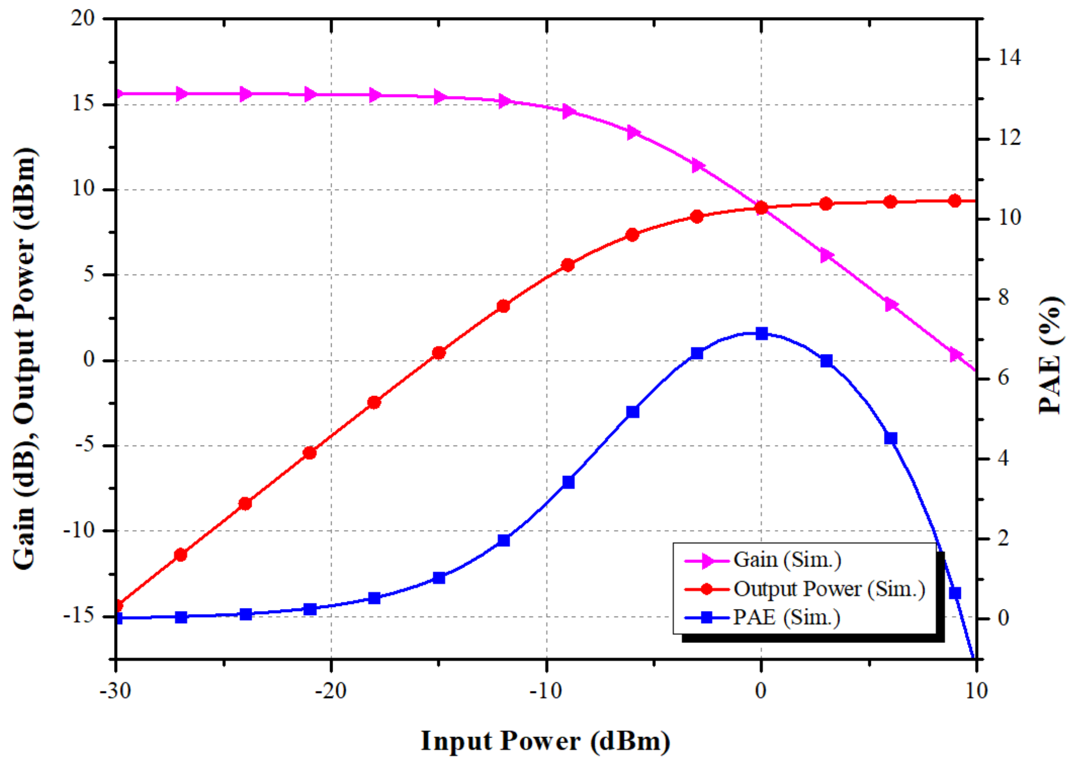

Fig. 4.71.. The simulated large-signal results of the proposed switch PA-LNA in PA mode at 80 GHz.

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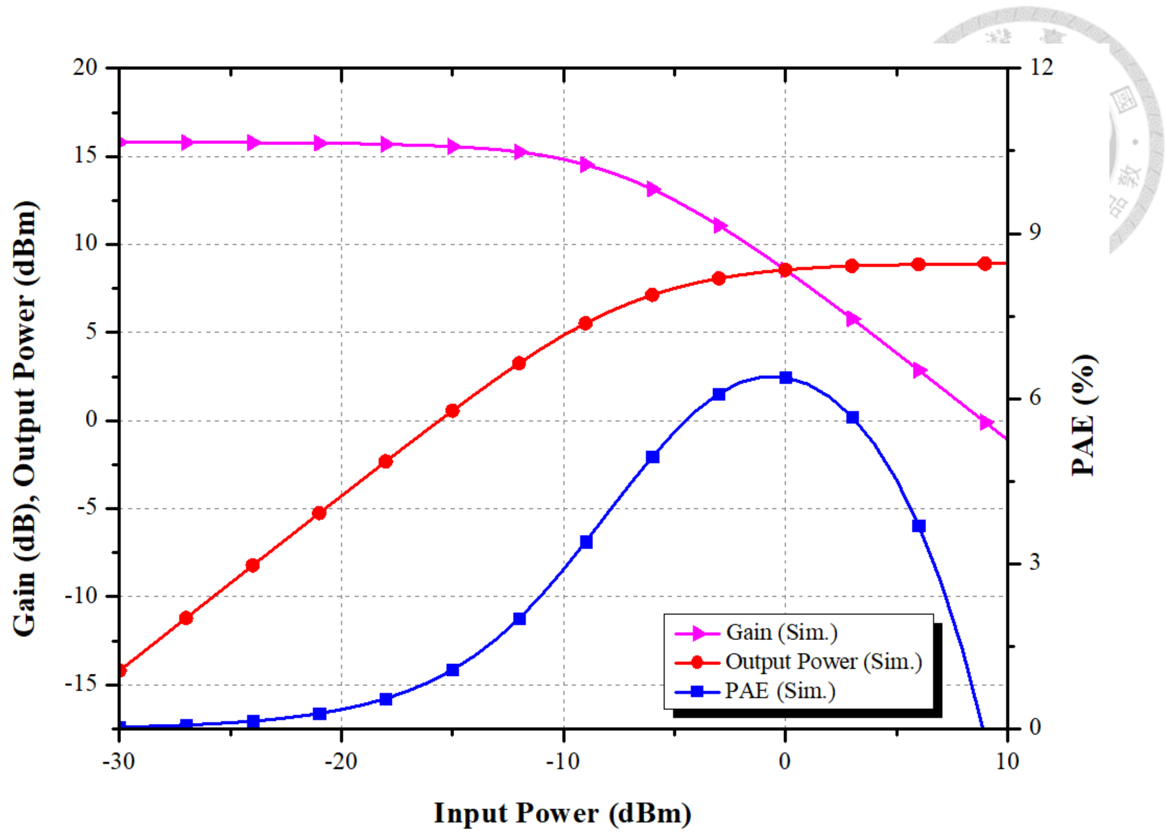

Fig. 4.72. The simulated large-signal results of the proposed switch PA-LNA in PA mode at 85 GHz.

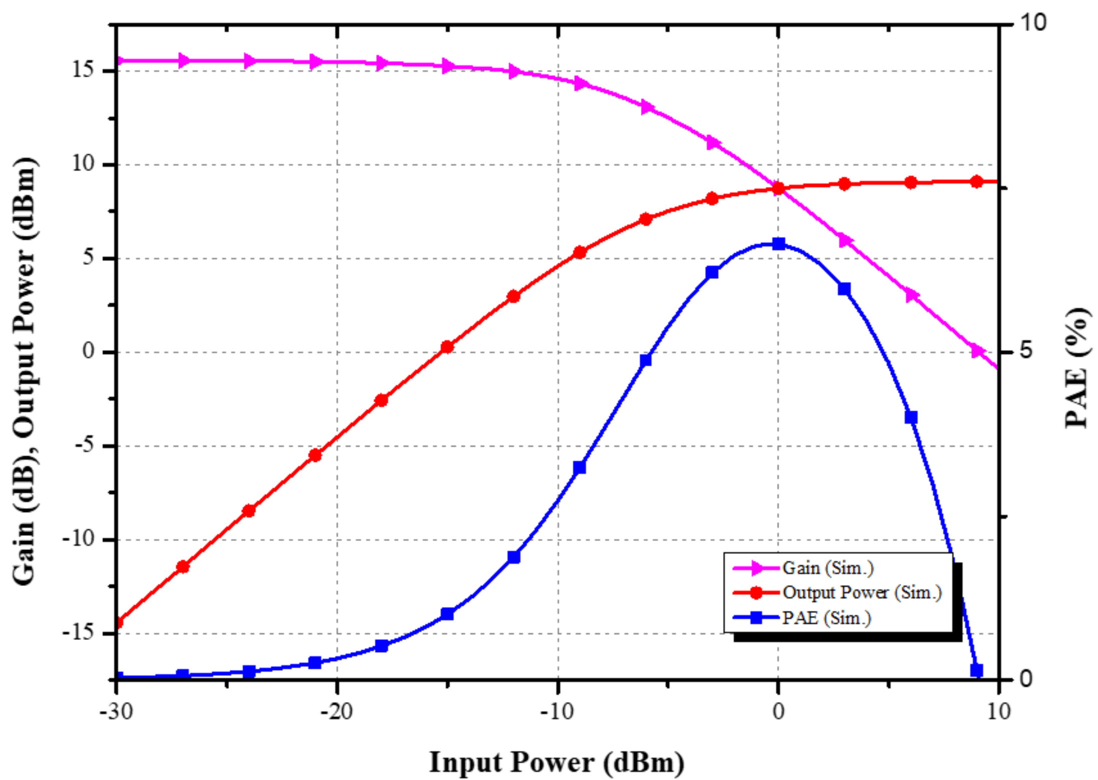

Fig. 4.73. The simulated large-signal results of the proposed switch PA-LNA in PA mode at 90 GHz.

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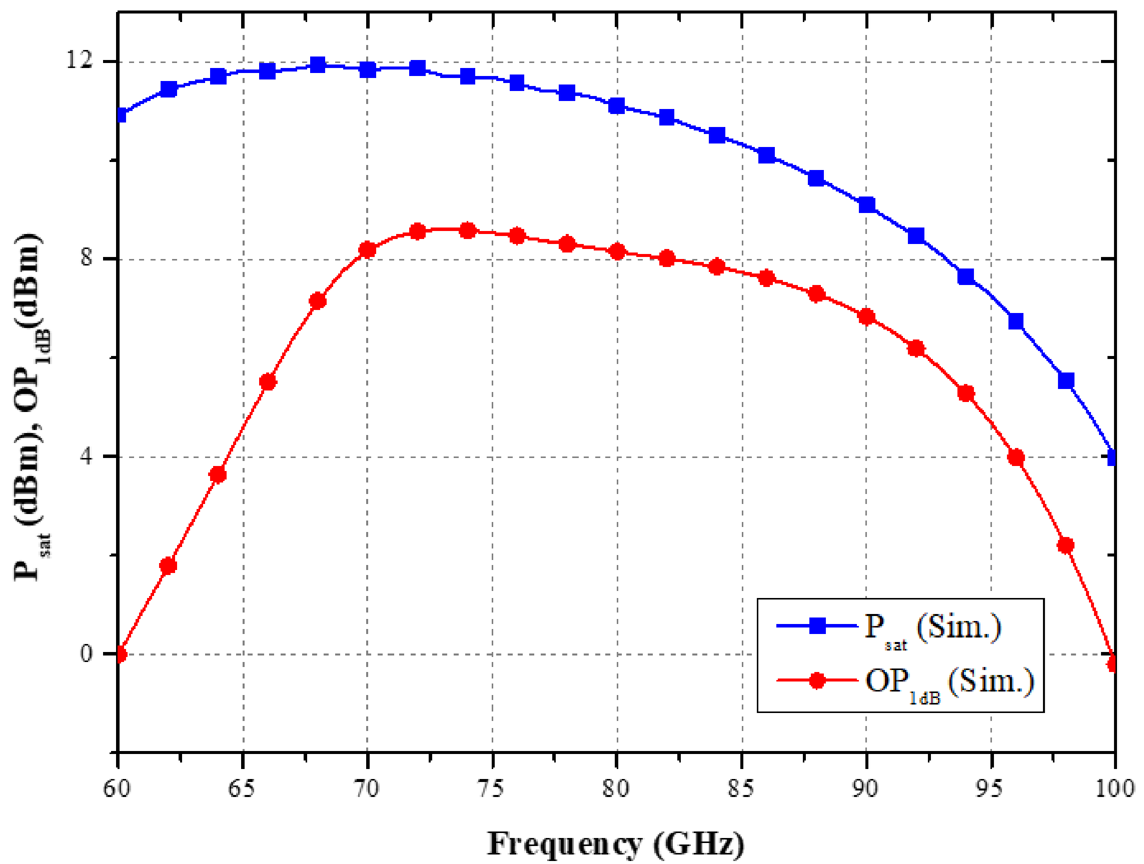

Fig. 4.74. The simulated large-signal CW performance of the proposed PA-LNA in PA mode from 60 GHz to 100 GHz.

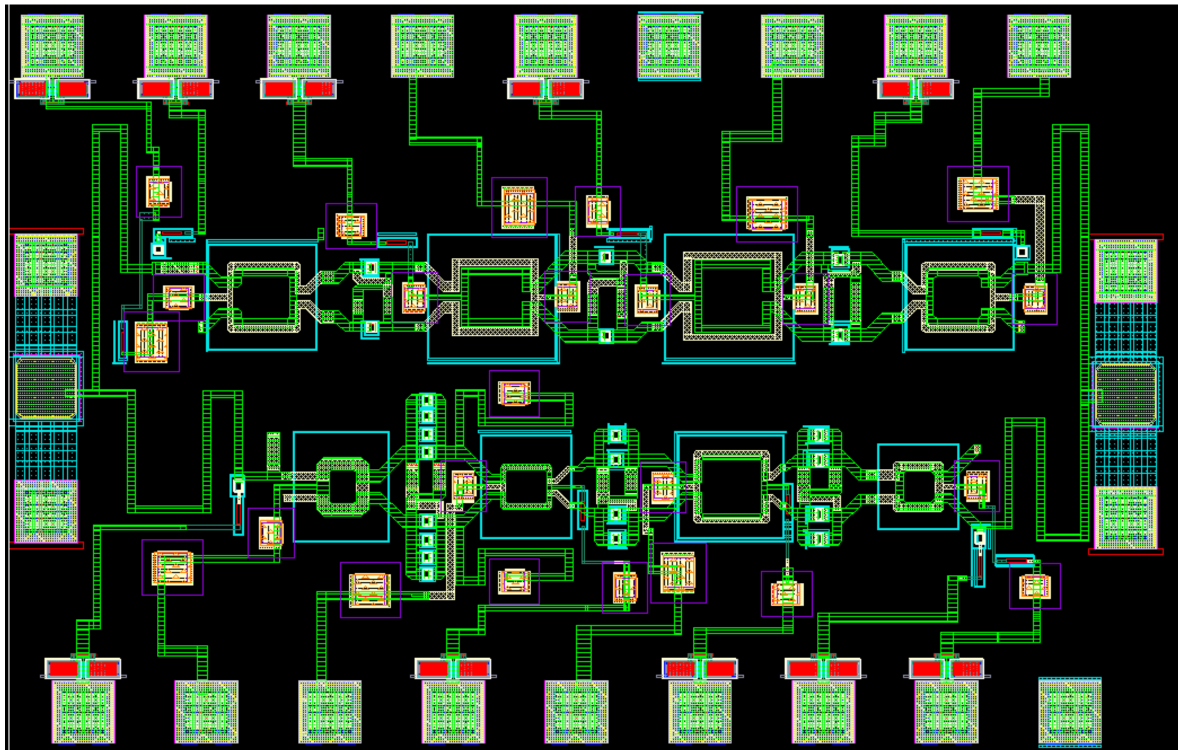

Fig. 4.75. The layout of the proposed W-band switch bidirectional PA-LNA.

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4.4.3 Experimental Result of the Switch Bidirectional PA-LNA

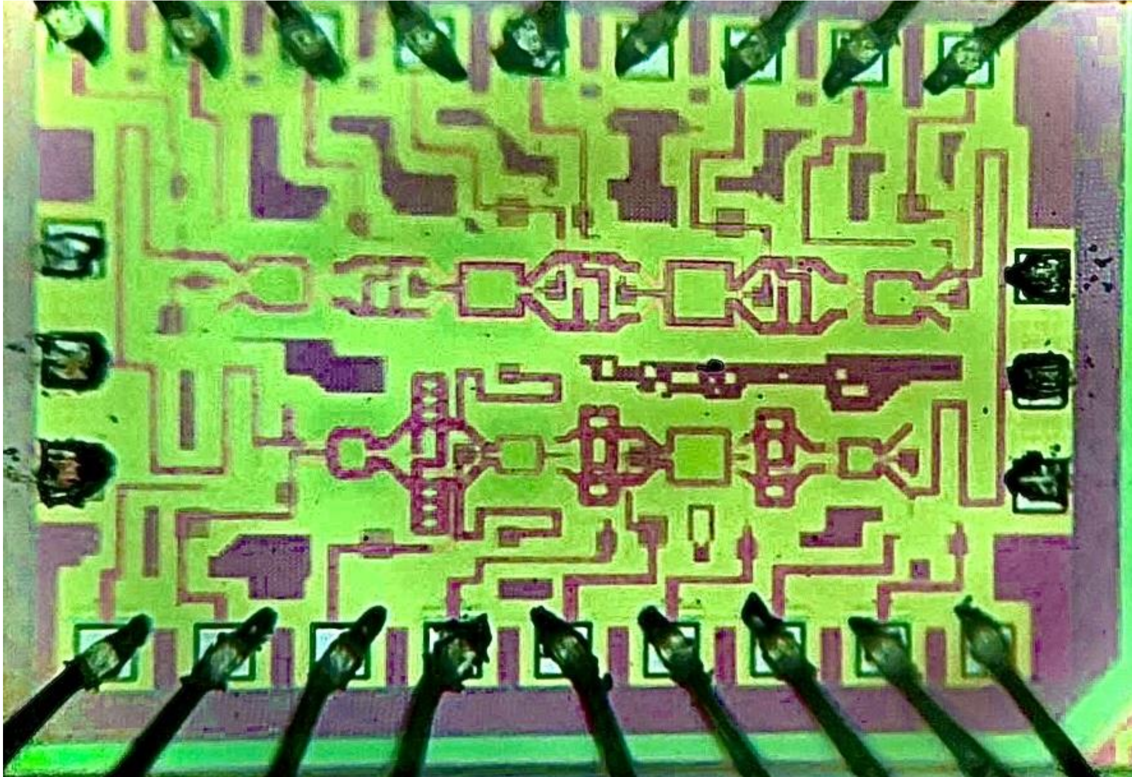

Fig. 4.76. Microphotograph of the proposed switch PA-LNA.

The proposed PA-LNA is fabricated in 1P9M 65-nm bulk CMOS process with ultra-thick top metal (UTM), and the chip micrograph is shown in Fig. 4.76. The chip size of this circuit is 0.55 mm² (0.93 mm × 0.6 mm) including bypass capacitors, dc- and RF-pads. All measurement results were performed on-wafer using GSG RF probes and use bonding-wire to provide dc. The S-parameters are measured by an Anritsu MS46522B VNA. The noise figure is measured by Y-Factor measurement to transfer noise figure. Fig. 4.77 shows the measured and simulated S-parameters of the proposed PA-LNA in LNA mode. The measured peak gain under P_{dc} of 52 mW is 18.6 dB and the 3-dB bandwidth is 21 GHz covers from 74 to 95 GHz. Fig. 4.78 exhibits the measured and simulated noise figure in LNA mode. The minimum noise figure is 7.1 dB at 81 GHz and the average

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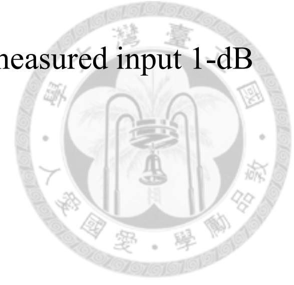
noise figure in the 3-dB bandwidth is 7.8 dB. Fig. 4.79 presents the measured input 1-dB gain compression point (IP_{1dB}) in LNA mode.



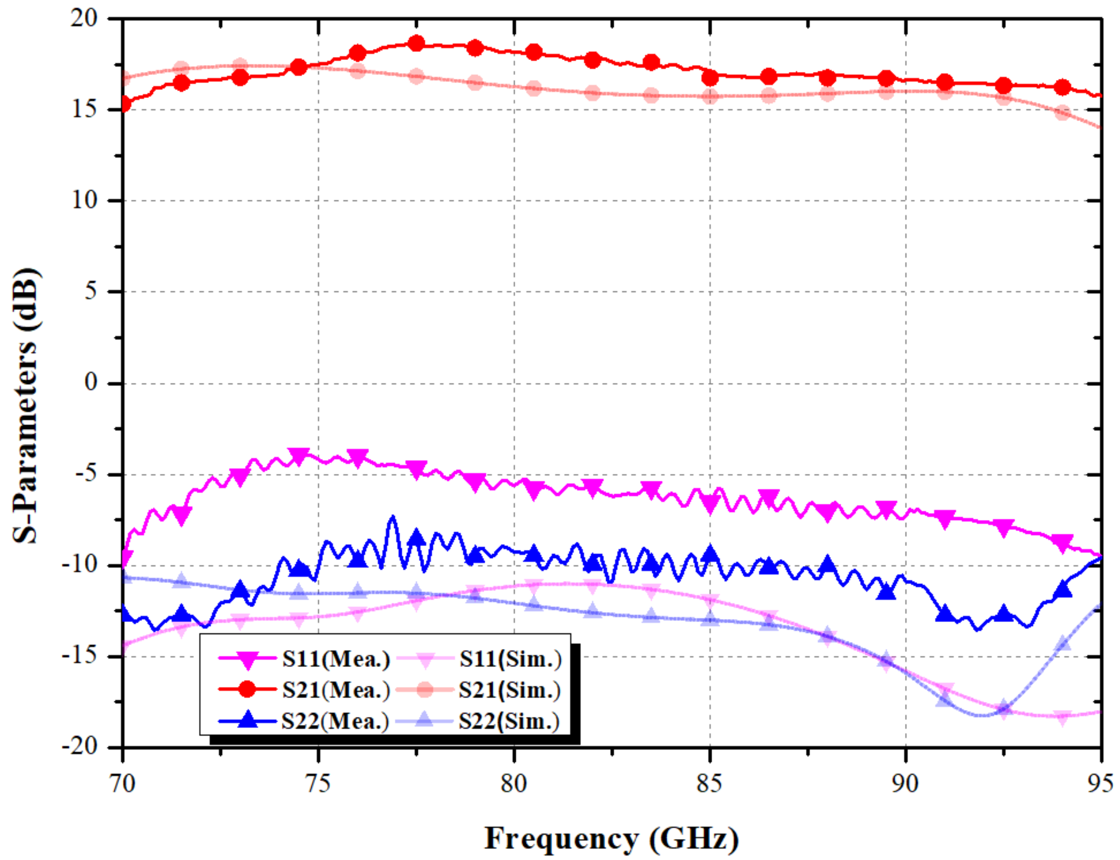


Fig. 4.77. The measured S-parameters of the proposed switch PA-LNA in LNA mode.

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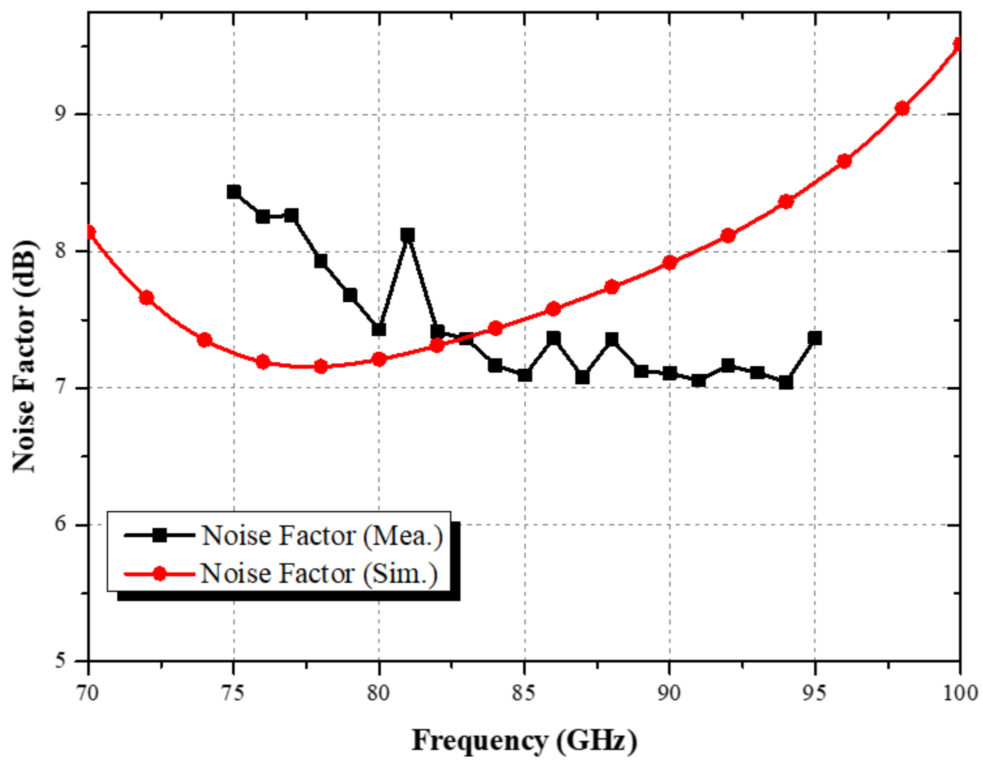

Fig. 4.78. The measured and simulated noise figure of the proposed switch PA-LNA in LNA mode.

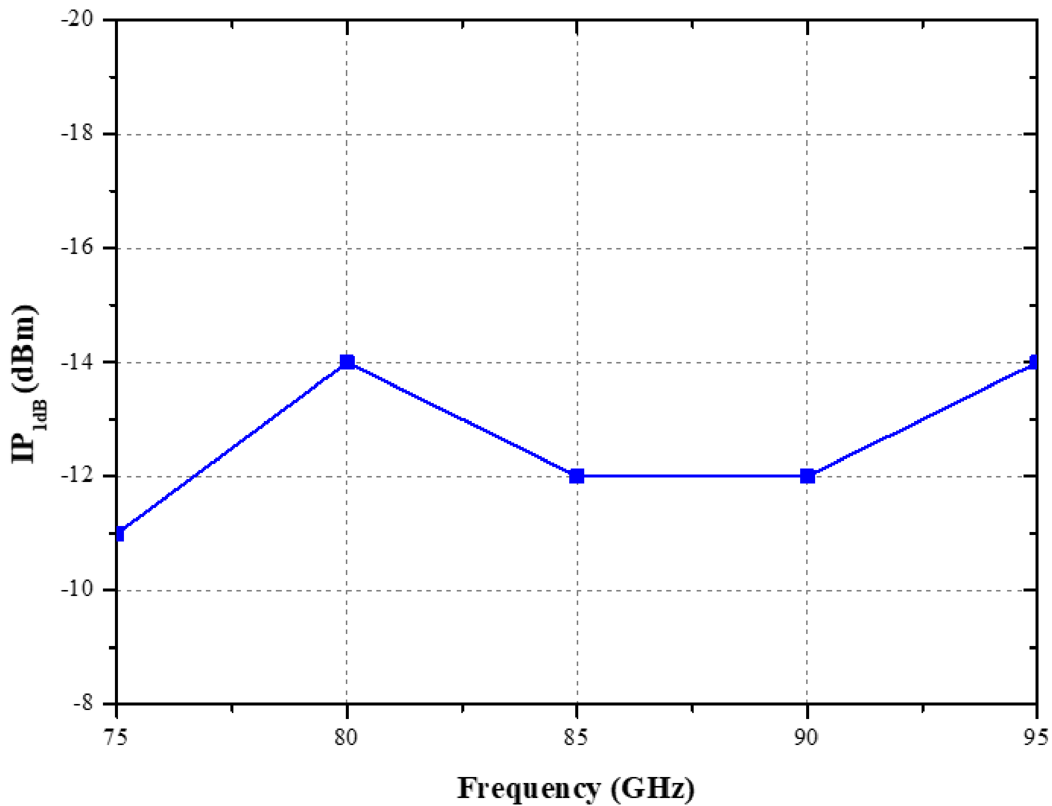

Fig. 4.79. The measured input 1-dB gain compression point (IP_{1dB}) of the proposed PA-LNA in LNA mode

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Fig. 4.80 shows the measured and simulated S-parameters of the PA-LNA in PA mode. The measured results agree reasonable with simulations and achieve a peak gain of 18.2 dB with a 3-dB bandwidth from 72.5 to 95 GHz. Fig. 4.81 to Fig. 4.84 show the single-tone measured and simulated CW large-signal characteristics from 75 to 90 GHz. The propose PA-LNA in PA mode achieves 9% PAE_{MAX}, 10-dBm P_{sat} and 7.3-dBm OP_{1dB} at 75 GHz. The PA-LNA in PA mode reaches 9% PAE_{MAX}, 9.2-dBm Psat and 5.5-dBm OP_{1dB} at 80 GHz. The PA-LNA in PA mode obtains 5% PAE_{MAX}, 7.5 dBm P_{sat} and 3.3-dBm OP_{1dB} at 85 GHz. The PA-LNA in PA mode obtains 4.57% PAE_{MAX}, 7.5 dBm P_{sat} and 4.5-dBm OP_{1dB} at 90 GHz. The measured P_{sat} and, OP_{1dB} across measured frequencies are shown in Fig. 4.85. From 75 to 90 GHz, the PA-LNA in PA mode achieves >7-dBm P_{sat}, >3.3-dBm OP_{1dB}.

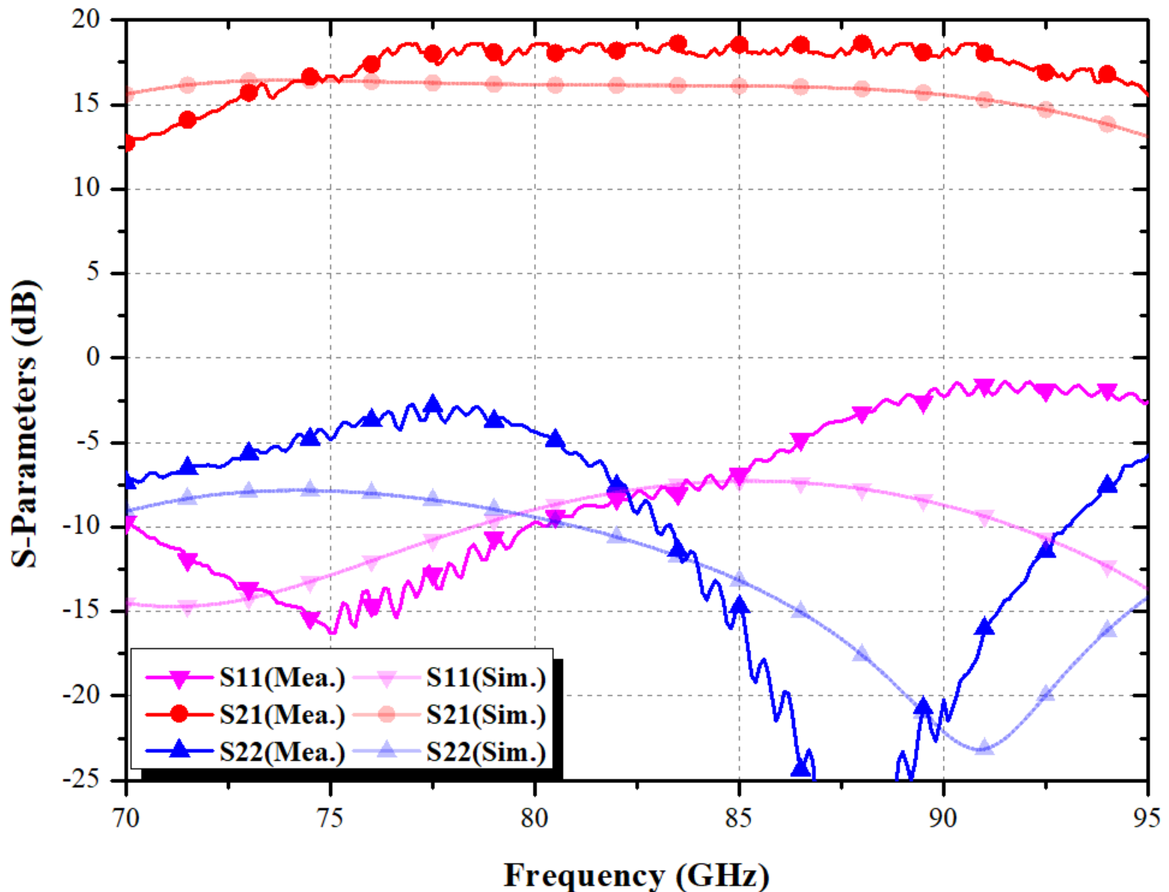

Fig. 4.80. The measured and simulated *S*-parameters of the switch proposed PA-LNA in PA mode.

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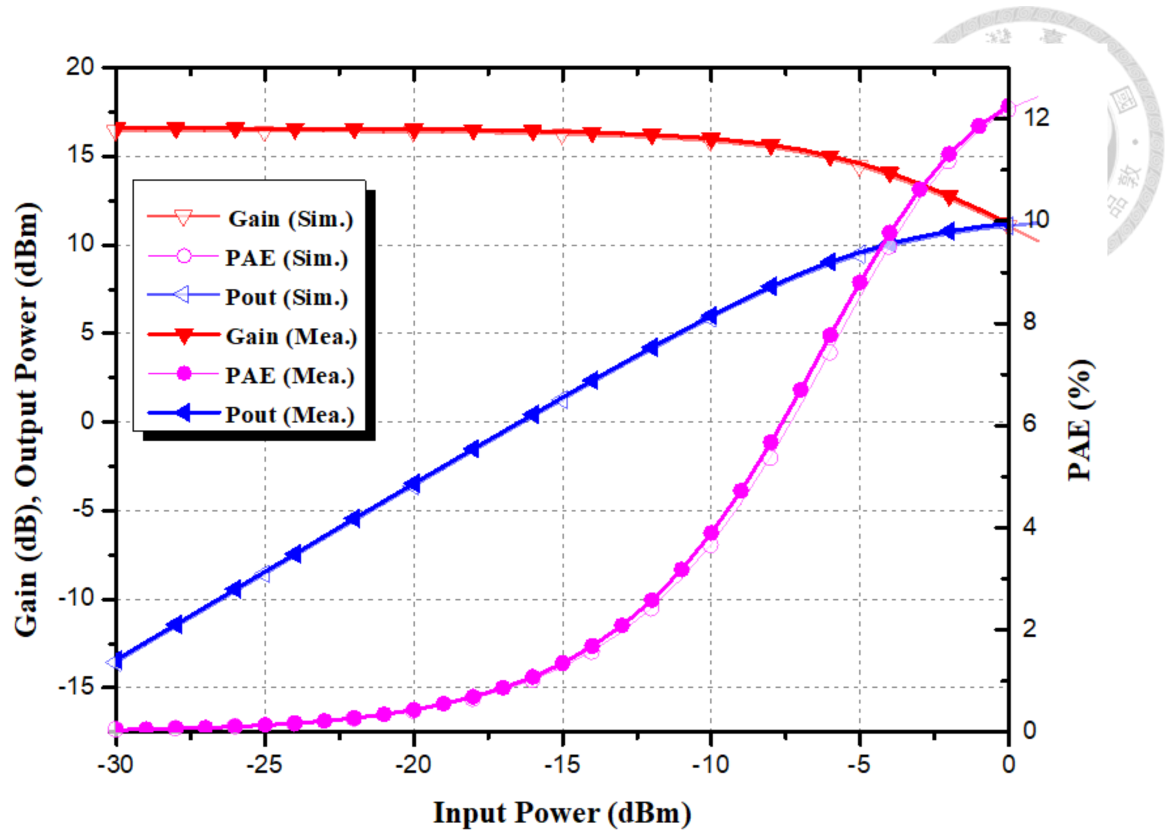

Fig. 4.81. The measured and simulated power performance at 75 GHz in PA mode.

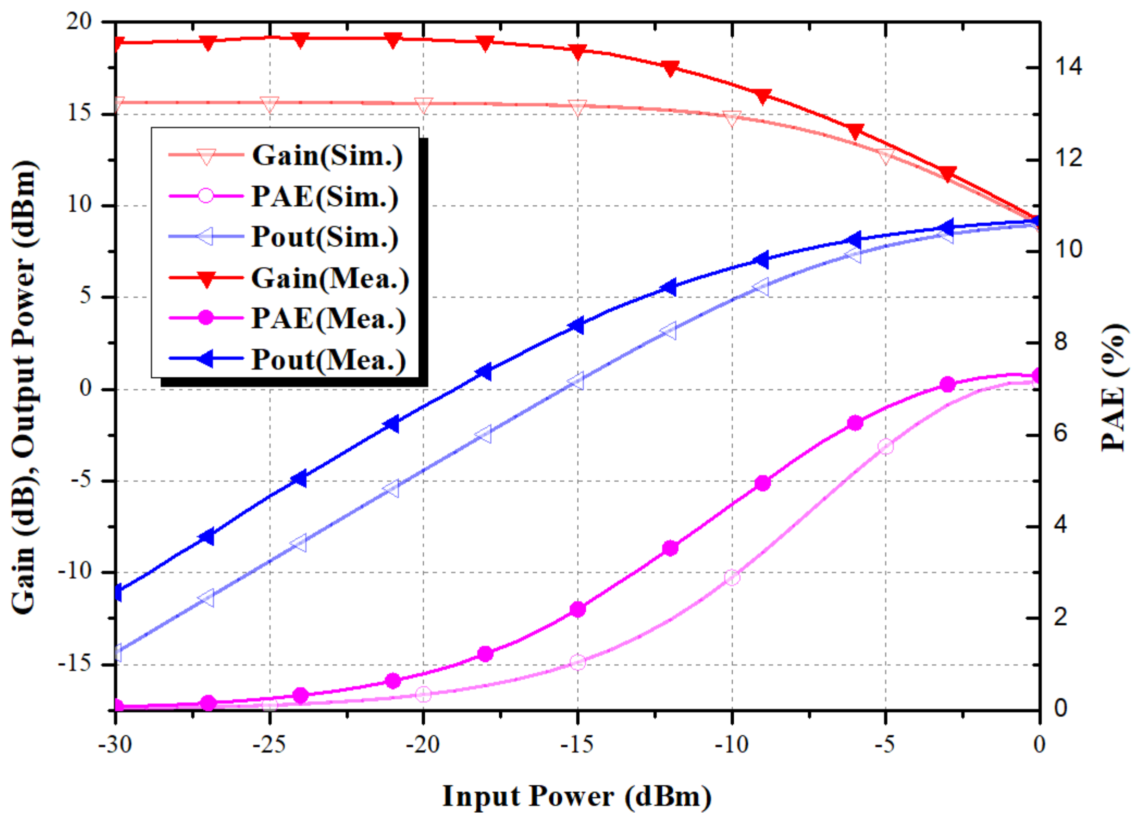

Fig. 4.82. The measured and simulated power performance at 80 GHz in PA mode.

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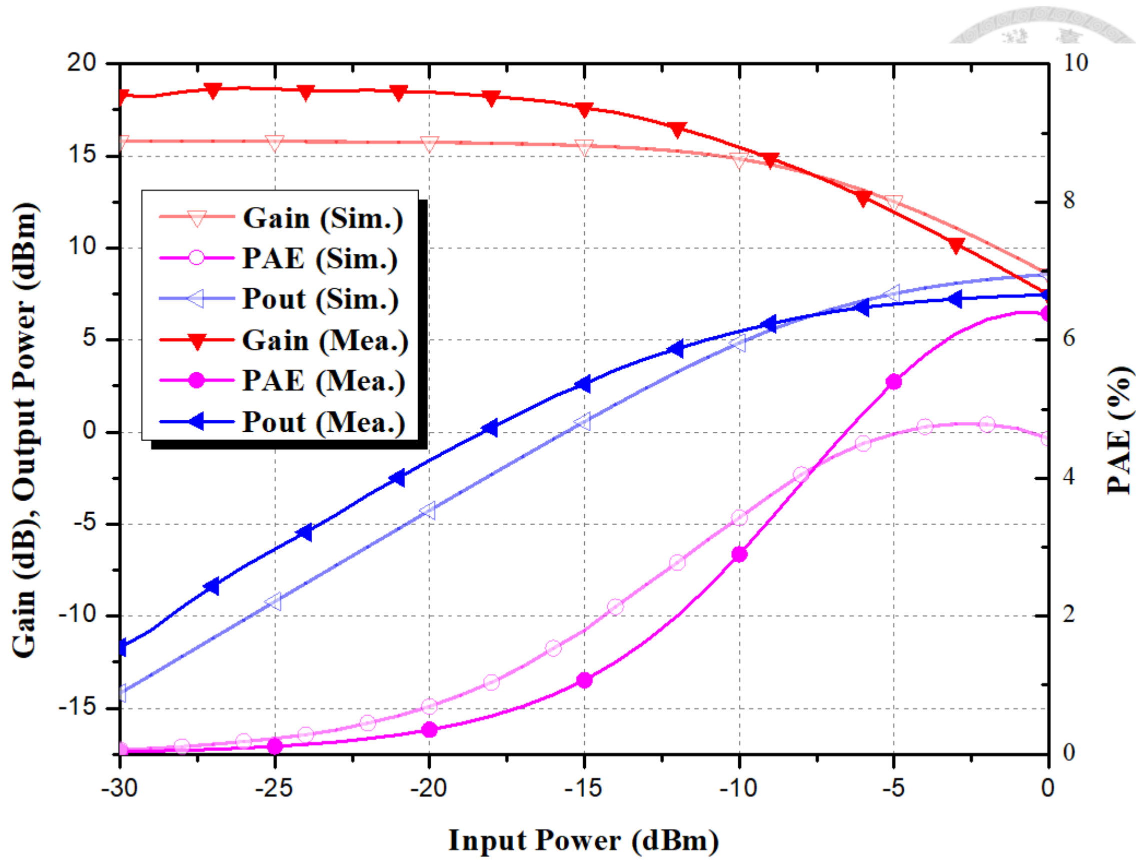

Fig. 4.83. The measured and simulated power performance at 85 GHz in PA mode.

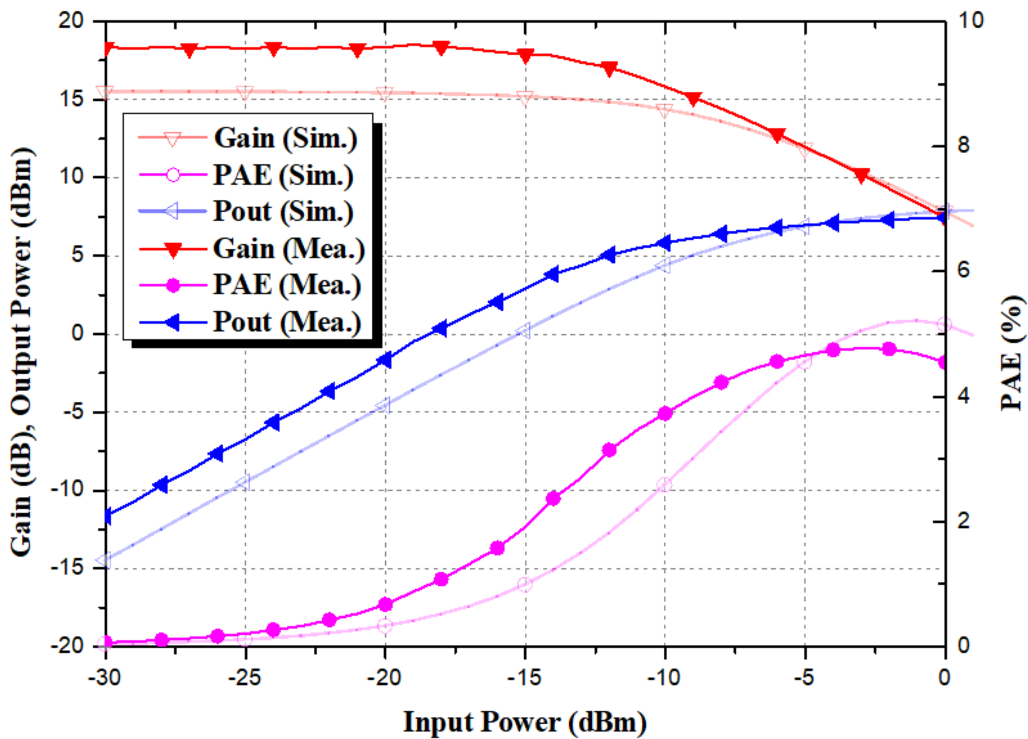

Fig. 4.84. The measured and simulated power performance at 90 GHz in PA mode.

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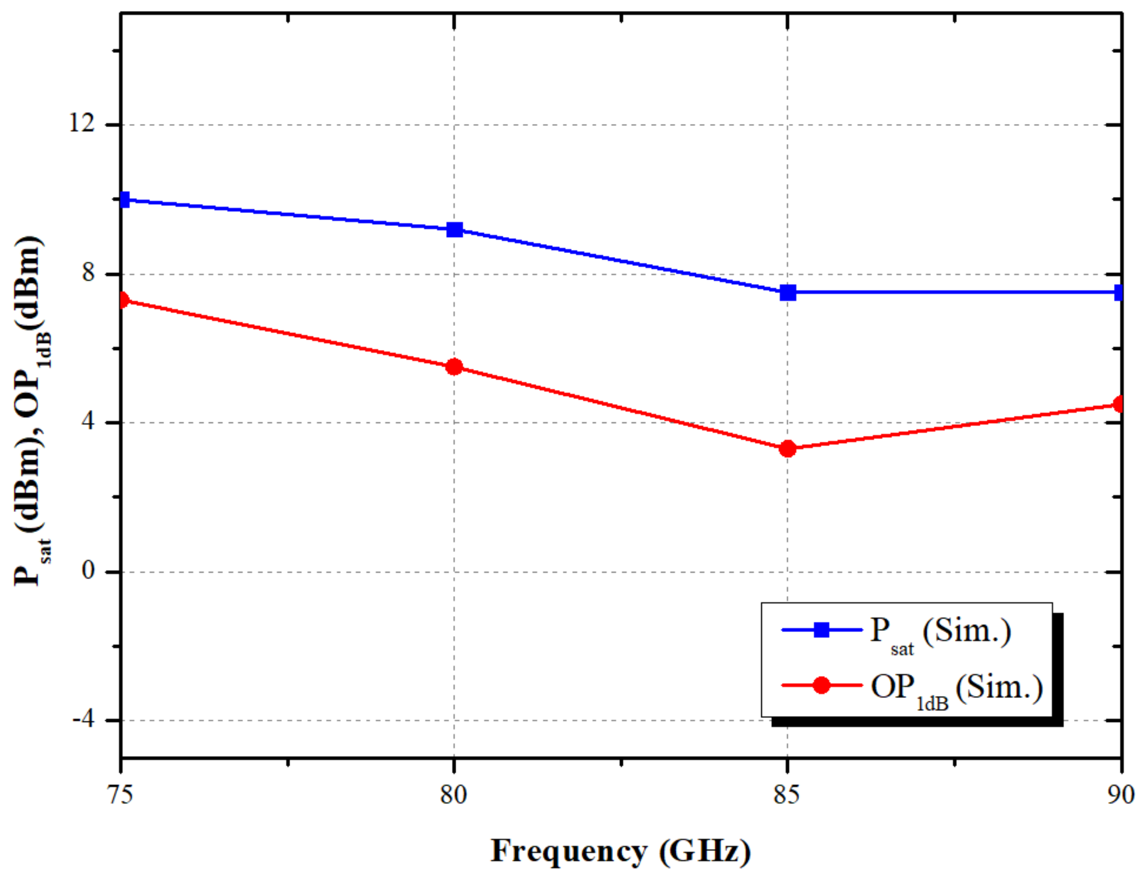

Fig. 4.85. The simulated large-signal CW performance of the proposed PA-LNA in PA mode from 75 GHz to 90 GHz.

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4.5 Trouble Shooting and Discussions

When compare the measured results with the simulated data, a noticeable trend emerges: the frequency response of the proposed w-band bidirectional PA-LNAs, as observed in the measured results, exhibits a significant shift of approximately 5 GHz towards higher frequencies. To gain a deeper understanding of this discrepancy, an extensive analysis of the RF and NCH models was conducted. The initial simulation approach involved using HFSS, a well-known electromagnetic simulation software package with a comprehensive 3D modelling environment, in place of Sonnet. Within HFSS, the 3-D architecture of the RF model is constructed, a depiction of which can be found in Fig. 4.86. A key observation here is the inclusion of additional metal sheets for the lumped ports during the simulation process, a feature conspicuously absent in the real transistor layout. Unfortunately, this introduced an undesirable side effect in the form of extra parasitic capacitance between these added metal sheets. In light of this development, it becomes apparent that addressing the influence of this supplementary parasitic capacitance is necessary. To do so, the NCH+EM model was augmented with small-value capacitors (C_{gs}, C_{gd}, and C_{ds}) [55]. These capacitors were strategically integrated to correct for the impact of the extra parasitic capacitance mentioned earlier. It is worth noting that the capacitance value for each individual lumped port can be computed using the capacitance formula[54],

$$C = \frac{\varepsilon A}{d} \qquad (4,3)$$

where ε represents the dielectric permittivity, which may vary depending on the manufacturing process. A signifies the surface area of the capacitor plates, while d represents the separation distance between these plates. To calculate the overall capacitance, you can simply multiply the capacitance of an individual finger by the total

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number of fingers. The derived capacitance values closely align with those presented in Table 4.4, providing solid support for the validity of the revised model.

Fig. 4.87 provides an illustration of the transistor trace, where the NCH model, sourced from TSMC, is connected to the simulation outcomes obtained from HFSS software. Moving on Fig. 4.88 to Fig. 4.90, a comparative analysis of the S-parameters between the RF and NCH models employing electromagnetic simulations be conducted. The results clearly indicate a noticeable discrepancy. Consequently, in the simulations including additional components such as R_{gco}, C_{gs}, C_{gd}, and C_{ds} to account for the supplementary parasitic effects inherent in the transistor structure. Fig. 4.91 presents the complete design flow. Table 4.4 lists the values of R_{gco}, C_{gs}, C_{gd}, and C_{ds} for four different transistor sizes that incorporated into the design, and it lists the parasitic variations compared to those parameters in TSMC RF model. With these modifications, the simulation of switchless PA-LNA S-parameters and noise figure aligned well with the measurement, as shown in Fig. 4.92 to Fig. 4.94. Additionally, the simulation of switch PA-LNA S-parameters and noise figure aligned well with the measurement, as shown in Fig. 4.95 to Fig. 4.97.

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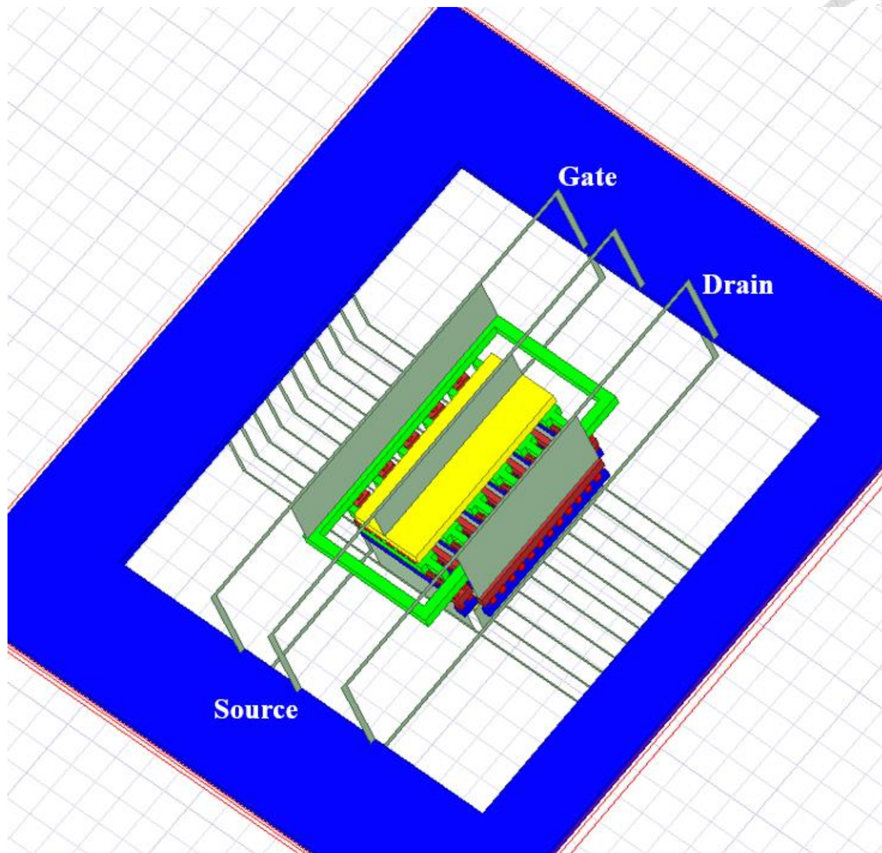
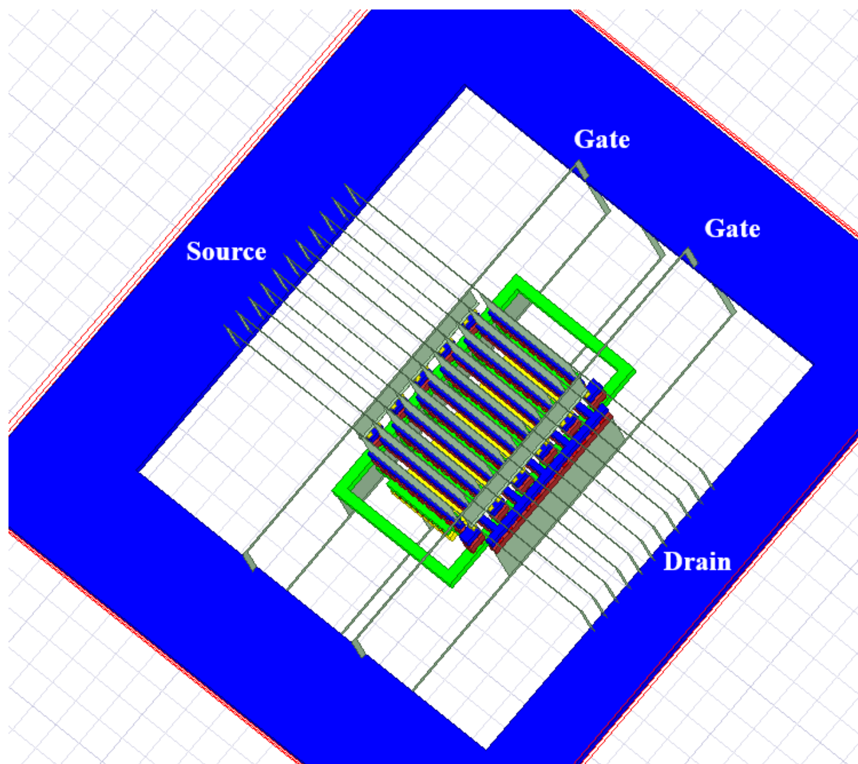


(a)



(b)

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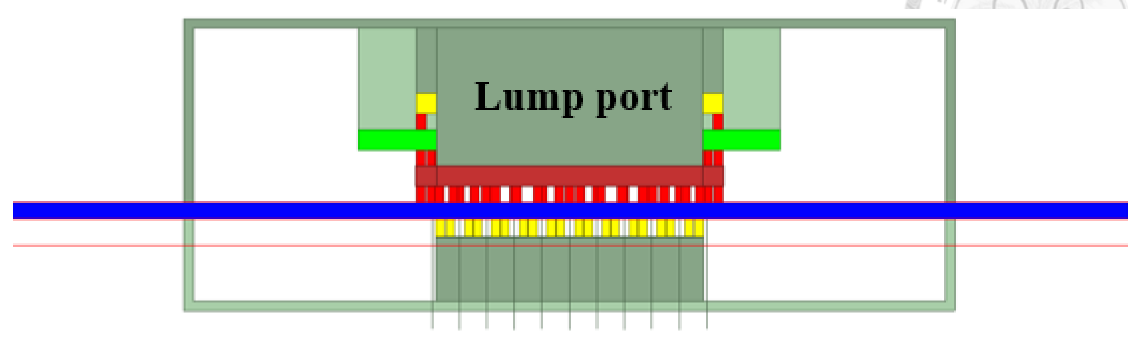

(c)

Fig. 4.86. 3-D layout of the transistor with 10f ×2μm in HFSS. (a) The top view of transistor layout. (b) The back view of transistor layout. (c) The side view of transistor layout.

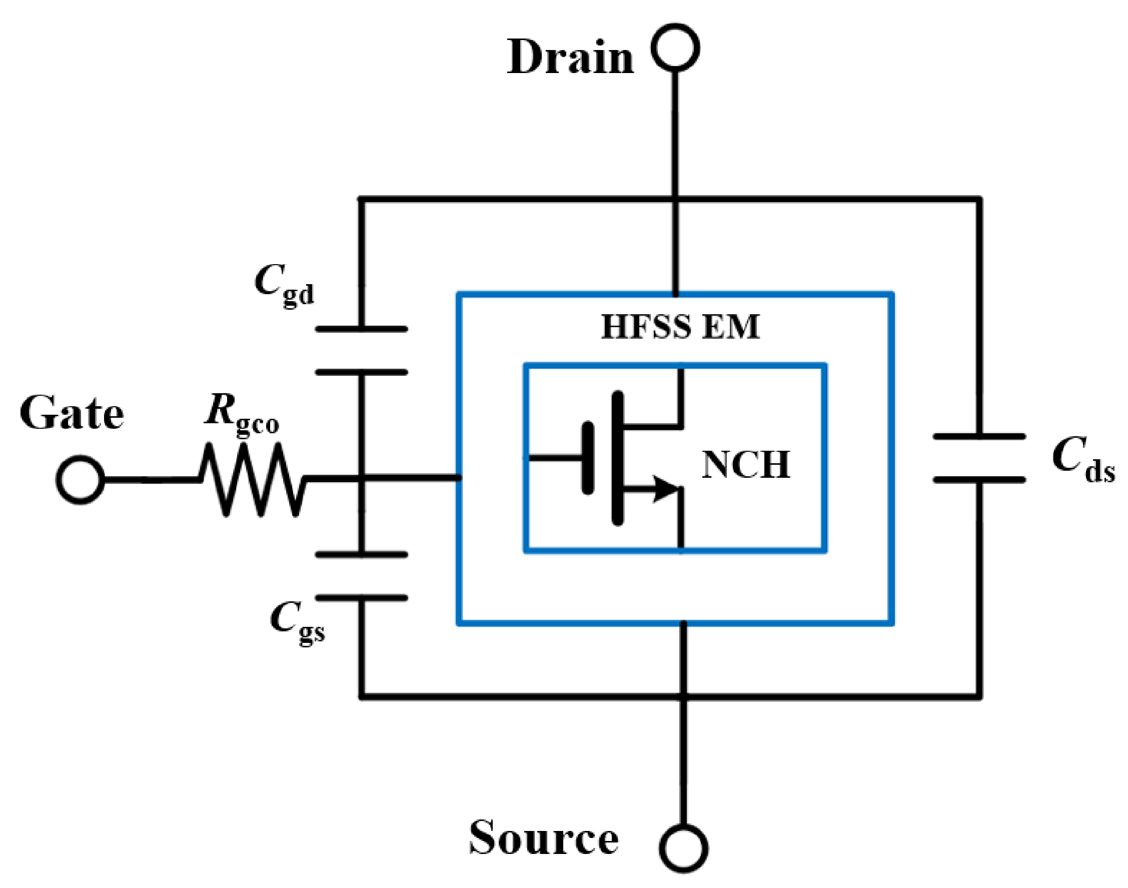

Fig. 4.87. The schematic diagram of NCH model transistor with parasitic parameter.

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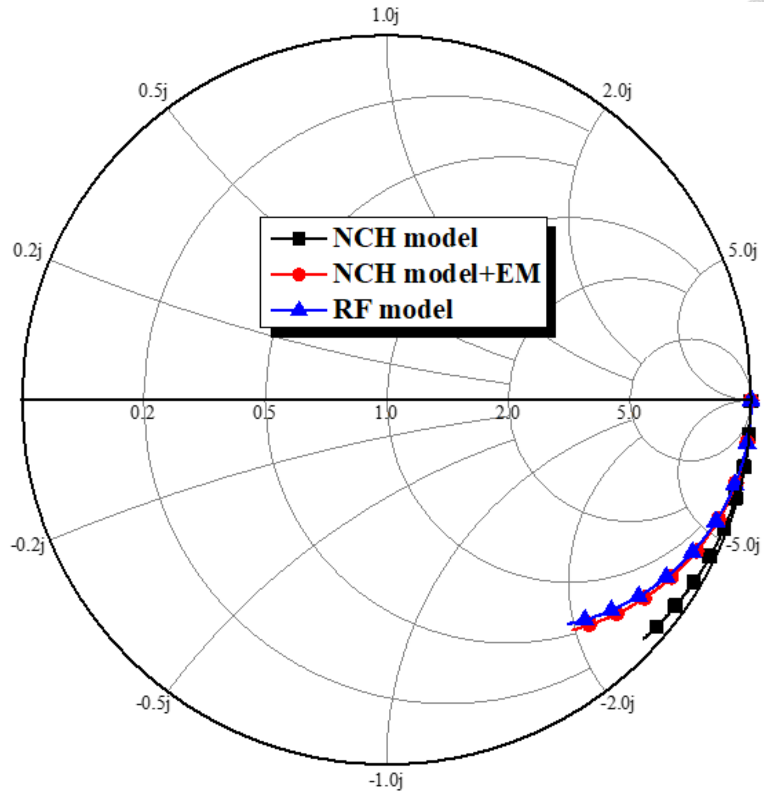

Fig. 4.88. The comparison of different models S (1,1) from 1 to 130 GHz.

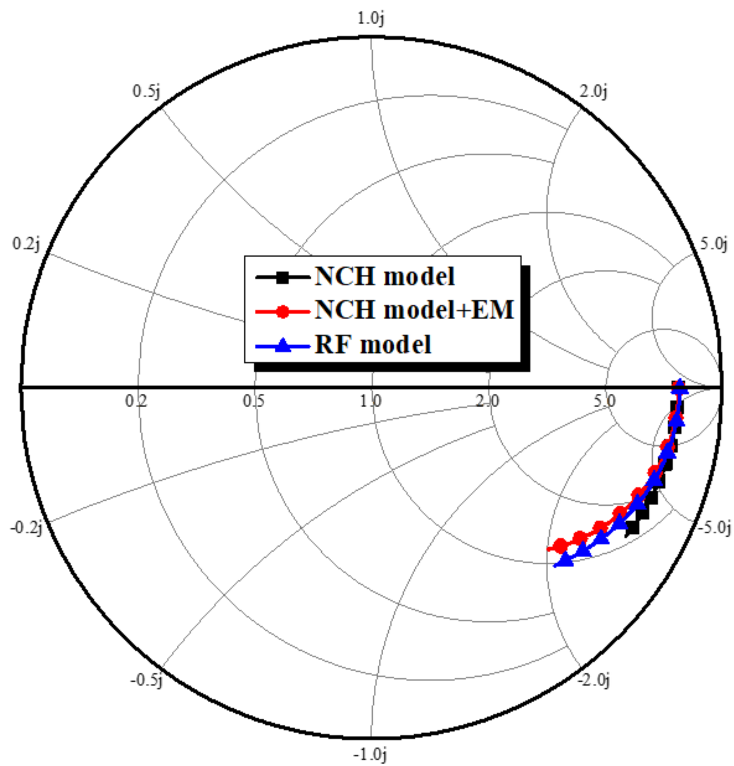

Fig. 4.89. The comparison of different models S (2,2) from 1 to 130 GHz

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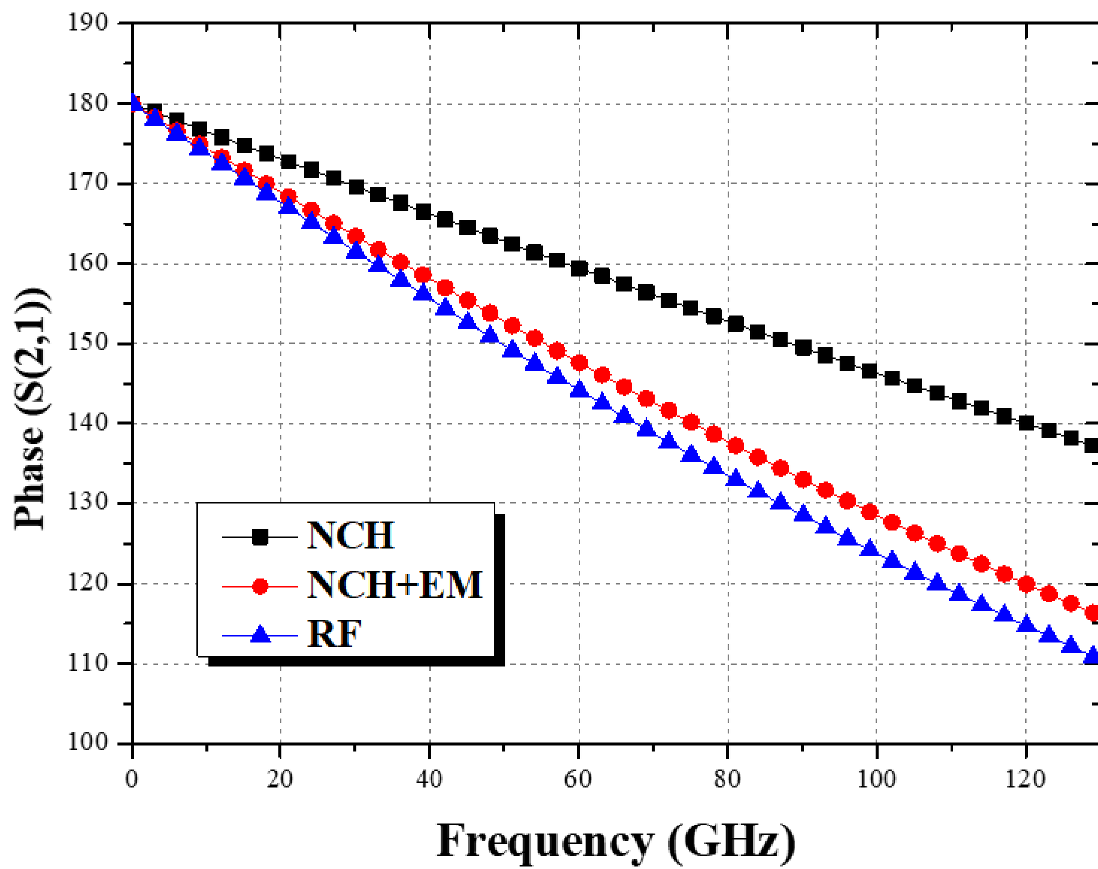

Fig. 4.90. The phase comparison of different models.

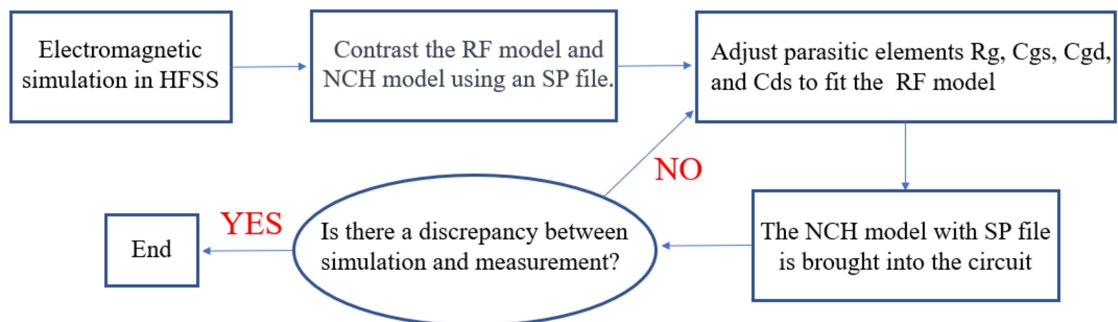

Fig. 4.91. The design flow of the debug.

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Table 4.4 The values of R_{gco}, C_{gs}, C_{gd}, and C_{ds} with different transistor size.

	R_{gco}	C_{gs}	C_{gd}	C_{ds}
12 fingers ×1 μm	20 Ω	-2.8 fF *(15%)	0.6 fF *(18%)	-6 fF *(13%)
8 fingers ×2 μm	24 Ω	-3 fF *(18%)	0.26 fF *(15%)	-5.54 fF *(10%)
10 fingers ×2 μm	20 Ω	-2.7 fF *(15%)	0.45 fF *(16%)	-4.86 fF *(13%)
12 fingers ×2 μm	18 Ω	-2.5 fF *(8.4%)	0.64 fF *(5.3%)	-4.17 fF *(11%)

*(): Compared to TSMC model parasitic parameter

Table 4.4 lists the values of R_{gco}, C_{gs}, C_{gd}, and C_{ds} for four different transistor sizes that incorporated into the design, and it lists the parasitic variations compared to those parameters in TSMC RF model. The results indicate a margin of error of approximately 10% compared to the TSMC RF model.

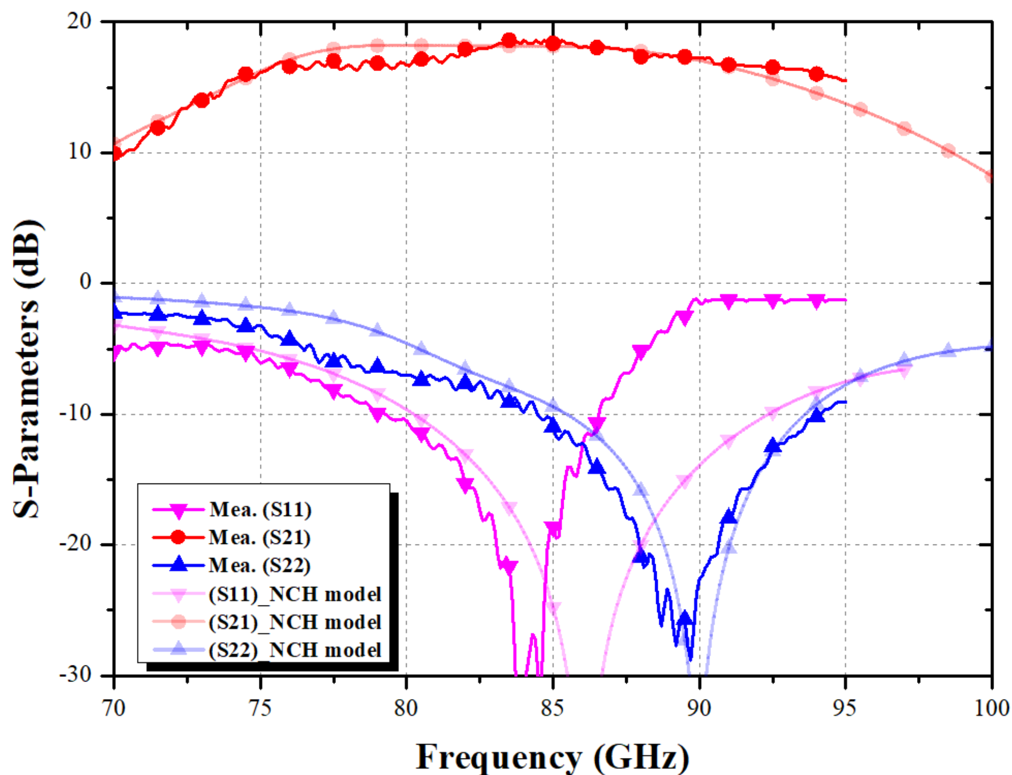

Fig. 4.92. The measured and re-simulated results of S-parameters of switchless PA-LNA in LNA mode.

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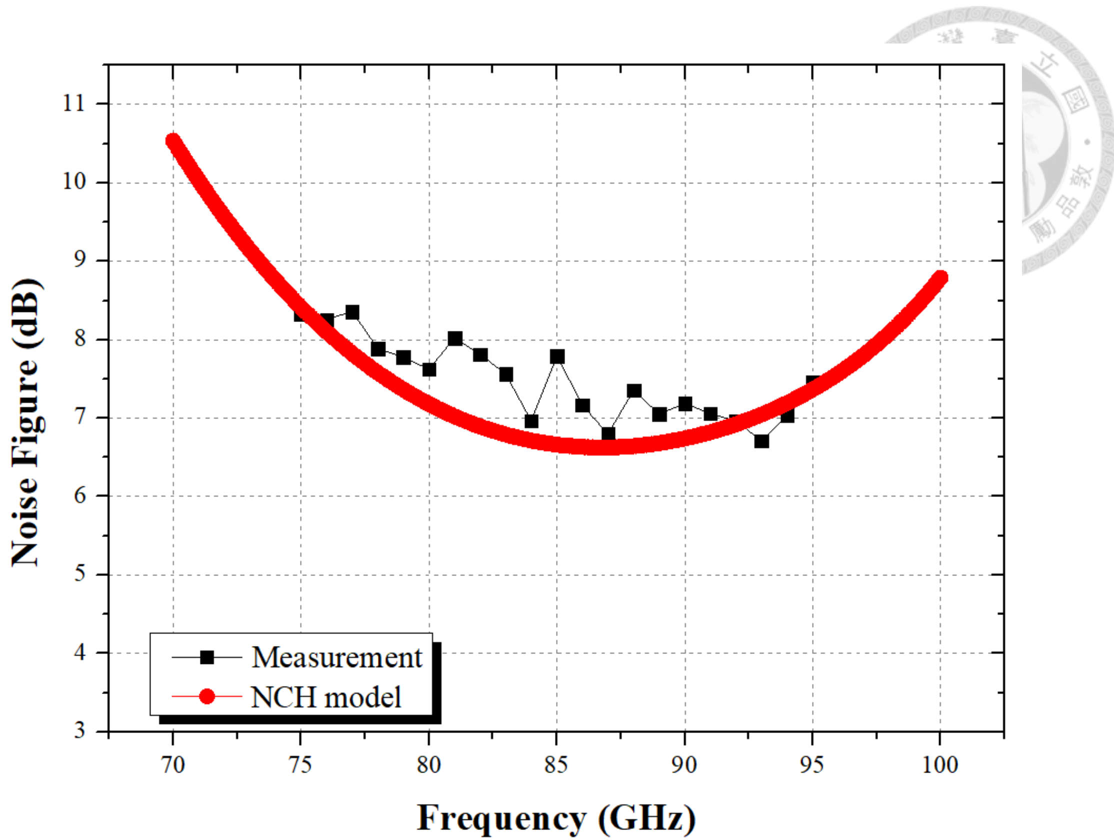

Fig. 4.93. The measured and re-simulated results of noise figure of switchless PA-LNA in LNA mode.

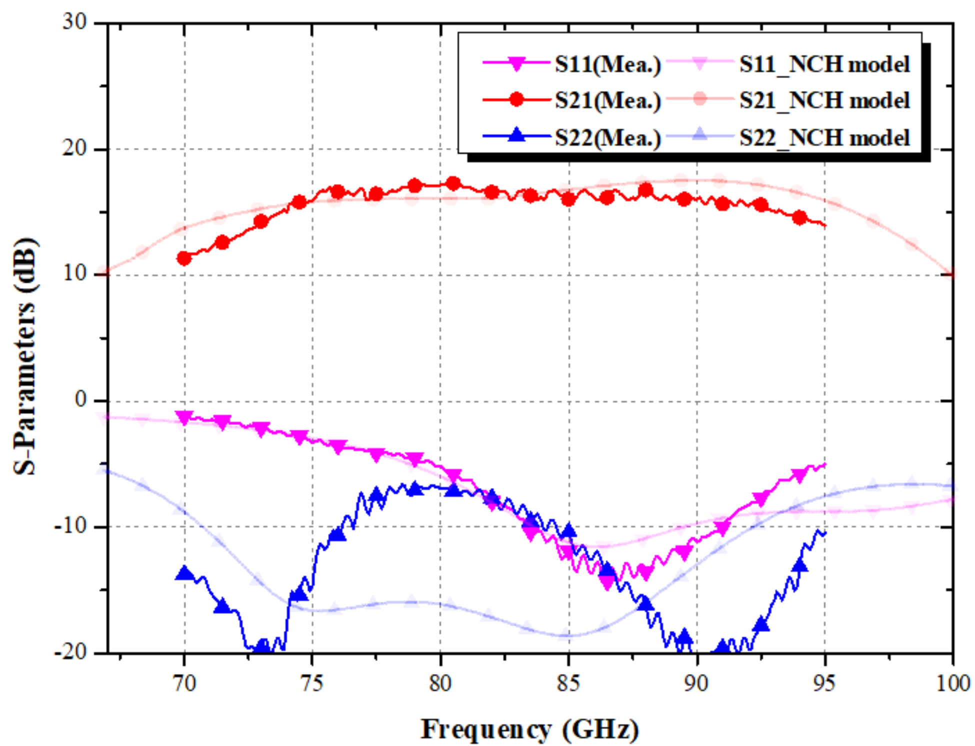

Fig. 4.94. The measured and re-simulated results of S-parameters of switchless PA-LNA in PA mode.

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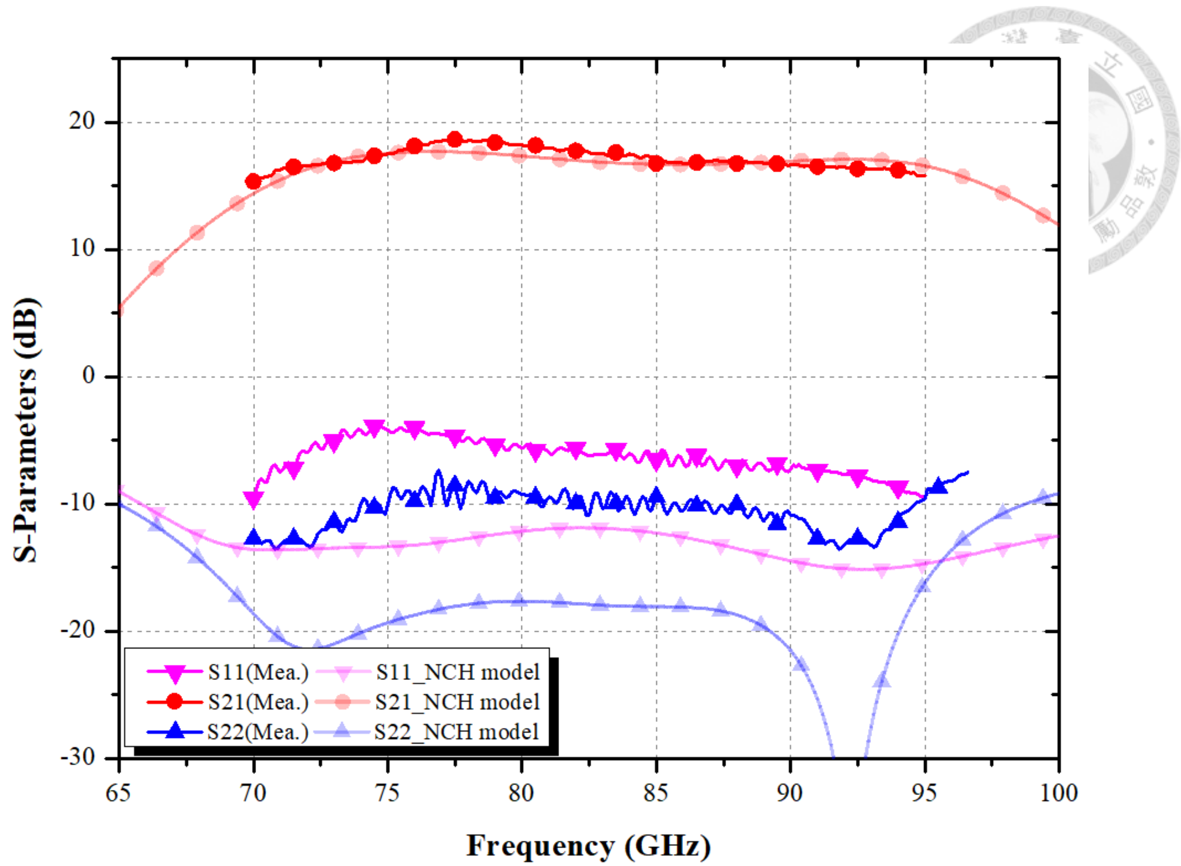

Fig. 4.95. The measured and re-simulated results of S-parameters of switch PA-LNA in LNA mode.

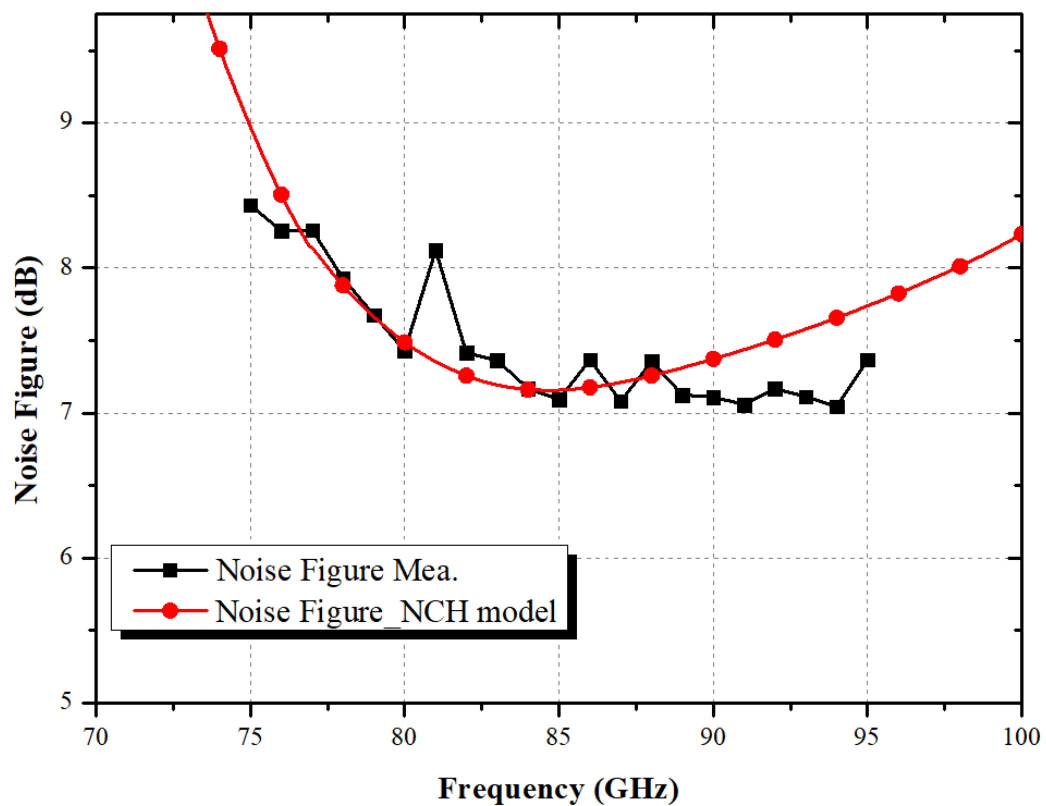

Fig. 4.96. The measured and re-simulated results of noise figure of switch PA-LNA in LNA mode.

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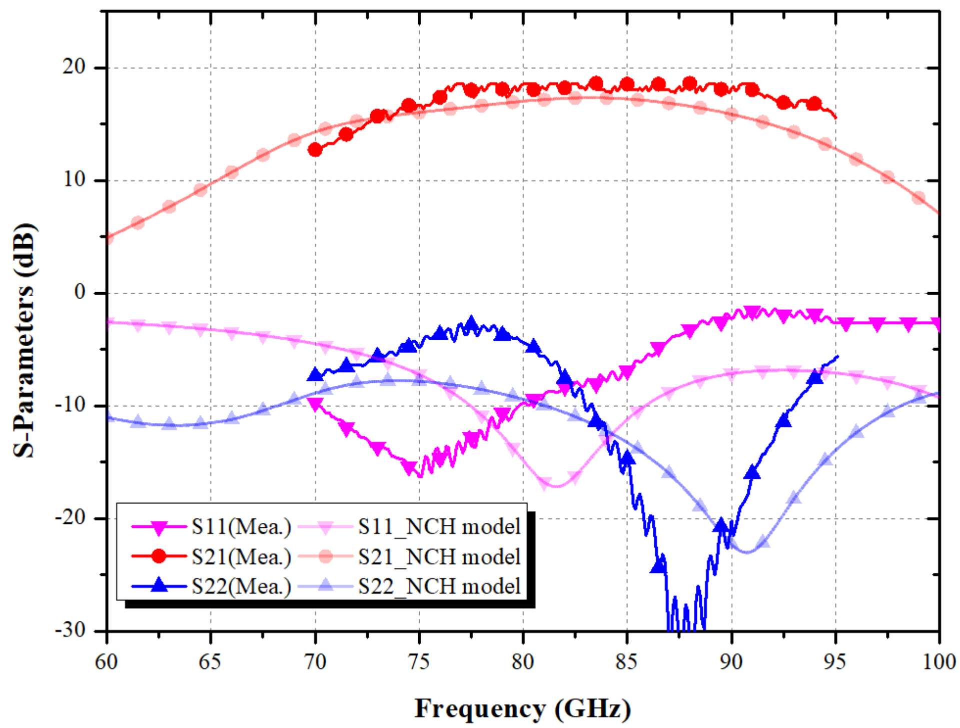

Fig. 4.97. The measured and re-simulated results of S-parameters of switch PA-LNA in PA mode.

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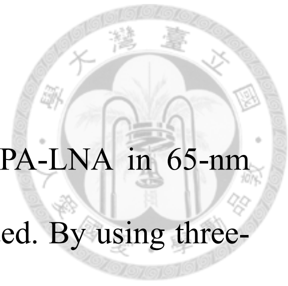
4.6 Summary



In this chapter, two W-band transformer-based bidirectional PA-LNA in 65-nm CMOS process for mm-wave phased-array front-end chip is presented. By using three-stage differential CS amplifier with capacitive neutralization technique for PA core and LNA core, the power gain and stability can be improved. In addition, the first proposed PA-LNA version uses the broadside coupling transformer as a bidirectional matching network for PA and LNA input/output without adopting lossy T/R switches. Thus, as a side benefit, the chip area can be minimized. However, achieving a high impedance for broadband operation using a Transformer rather than a switch proved to be highly challenging. Therefore, in the second version opted for a design that utilized a switch. However, the results indicated that when designing a broadband bidirectional PA-LNA, using a switch for mode switching proved to be more effective. Table 4.5 provides a summary of the performance of both the PA-LNA and recently published bidirectional PA-LNAs. The proposed PA-LNA represents the first implementation of a broadband design operating within the W-band.

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Table 4.5 Performance comparison with published PA-LNAs and front-end

Ref.	**[35]**	**[36]**	**[37]**		**This work**	
Process	65-nm CMOS	0.13-µm SiGe	0.13-µm SiGe		65-nm CMOS	
Topology	Switchless Bidirectional PA-LNA	Switchless Bidirectional PA-LNA	Dual-Band Bidirectional PA-LNA		Switchless Bidirectional PA-LNA	Switch Bidirectional PA-LNA
3-dB Freq.	58~62.5(PA) 58~67(LNA)	57~66 (PA&LNA)	28~34(PA) 25~35(LNA)	44~65(PA) 55~65(LNA)	73~95(PA) 74~95(LNA)	72.5-95(PA) 70~95(LNA)
Tx Peak Gain(dB)	24.5	16.5	14.1	14.7	17.2	18.2
Tx OP_{1db} (dBm)	N/A	11	14.7	7.2	6@80 GHz	5.5@80 GHz
Tx P_{sat} (dBm)	8.4	12*	16.3	16	8@80 GHz	9.2@80 GHz
Tx PAE_{max} (%)	8.7	11	23.6	15.2	7.5@80 GHz	9@80 GHz
Rx Peak Gain(dB)	21.5	17	13.9	14.1	18.5	18.6
Rx Min.NF(dB)	6.7	6.5	4.2	4.6	7	7.1
Rx IP_{1db} (dBm)	N/A	-20	-13	-13.5	-11	-14
Rx P_{dc} (mW)	39.6	36	10	24	53	52

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Chapter 5 Conclusions

This thesis presents the design and implementation of a high conversion gain and high efficiency D band frequency doubler using 28-nm CMOS for Astronomical application, a K_a-band Low noise amplifier by using 90-nm CMOS technology for fifth generation mobile communication (5G), and two version bidirectional PA-LNA for W band phased-array.

In Chapter 2, introduced a high conversion gain and high efficiency D band frequency doubler using 28-nm CMOS. This frequency doubler enables a wider bandwidth and high fundamental rejection by using Marchand balun. The 3-dB bandwidth of the proposed frequency doubler covers from 126 to 146 GHz. The measurement results demonstrate -4.5-dB conversion gain with dc power consumption of 12 mW.

In Chapter 3, a compact 21-40 GHz LNA with improved gain double-transformer-coupler is presented by using 90-nm CMOS process. To reduce the power consumption, the current-reused technique is used. The proposed LNA provides about 19.7 dB gain and 3.4 dB noise figure at 29.8 GHz with dc power consumption of 7.1 mW.

In Chapter 4, a W-band transformer-based switchless bidirectional PA-LNA and W-band bidirectional PA-LNA for mm-wave phased-array front-end chip is presented. The decision of the amplifier structure of the switchless PA-LNA circuit and the adoption of gain enhancement technique are discussed. Besides, the description and flow chart for how the design trades were made for the switchless PA-LNA are proposed. By using three-stage differential CS amplifier with capacitive neutralization technique for PA core and LNA core, the power gain and stability can be improved. In addition, the proposed PA-LNA uses the broadside coupling transformer as a bidirectional matching network for

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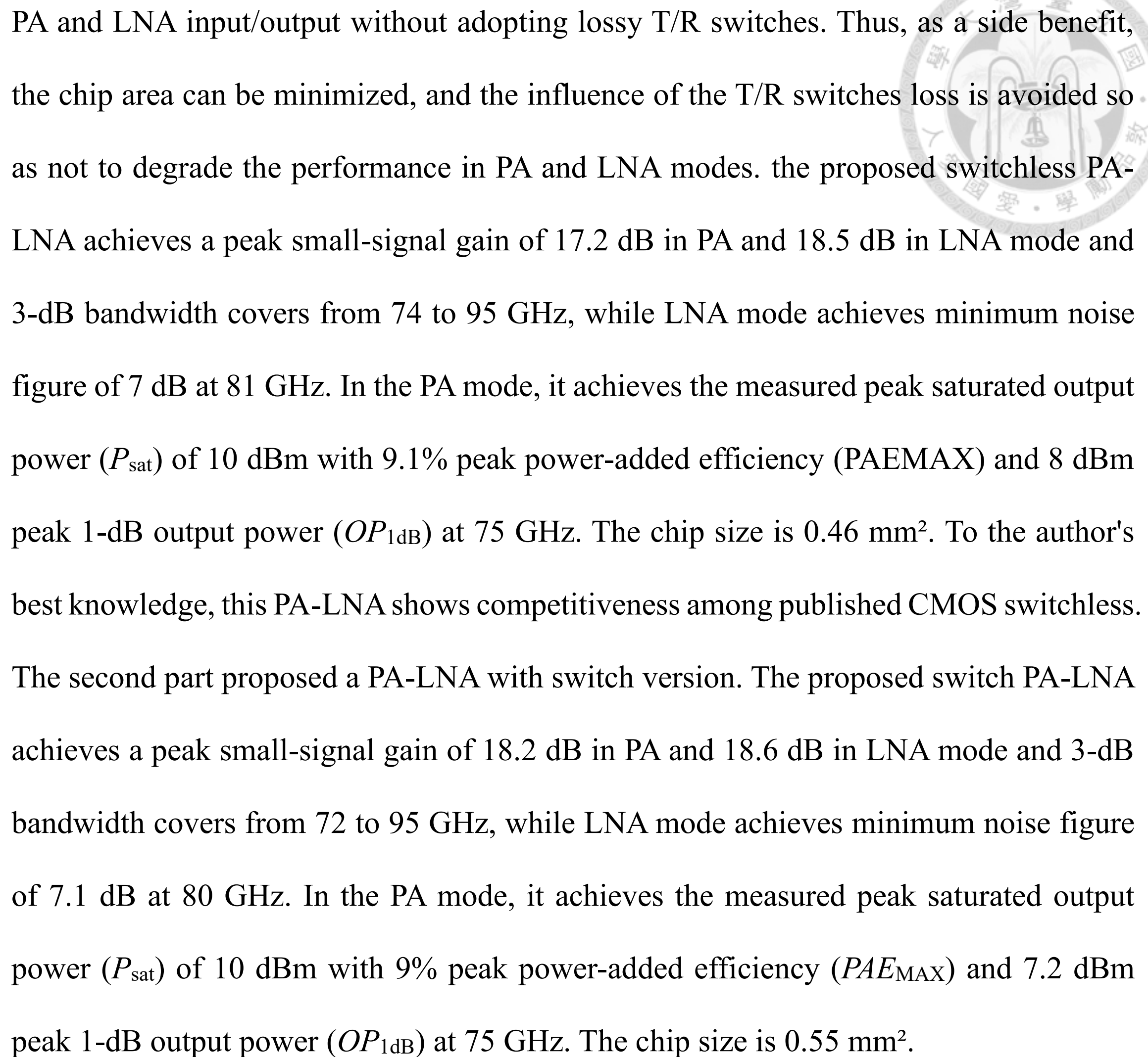

PA and LNA input/output without adopting lossy T/R switches. Thus, as a side benefit, the chip area can be minimized, and the influence of the T/R switches loss is avoided so as not to degrade the performance in PA and LNA modes. the proposed switchless PA-LNA achieves a peak small-signal gain of 17.2 dB in PA and 18.5 dB in LNA mode and 3-dB bandwidth covers from 74 to 95 GHz, while LNA mode achieves minimum noise figure of 7 dB at 81 GHz. In the PA mode, it achieves the measured peak saturated output power (P_{sat}) of 10 dBm with 9.1% peak power-added efficiency (PAEMAX) and 8 dBm peak 1-dB output power (OP_{1dB}) at 75 GHz. The chip size is 0.46 mm^2. To the author's best knowledge, this PA-LNA shows competitiveness among published CMOS switchless. The second part proposed a PA-LNA with switch version. The proposed switch PA-LNA achieves a peak small-signal gain of 18.2 dB in PA and 18.6 dB in LNA mode and 3-dB bandwidth covers from 72 to 95 GHz, while LNA mode achieves minimum noise figure of 7.1 dB at 80 GHz. In the PA mode, it achieves the measured peak saturated output power (P_{sat}) of 10 dBm with 9% peak power-added efficiency (PAE_{MAX}) and 7.2 dBm peak 1-dB output power (OP_{1dB}) at 75 GHz. The chip size is 0.55 mm^2.

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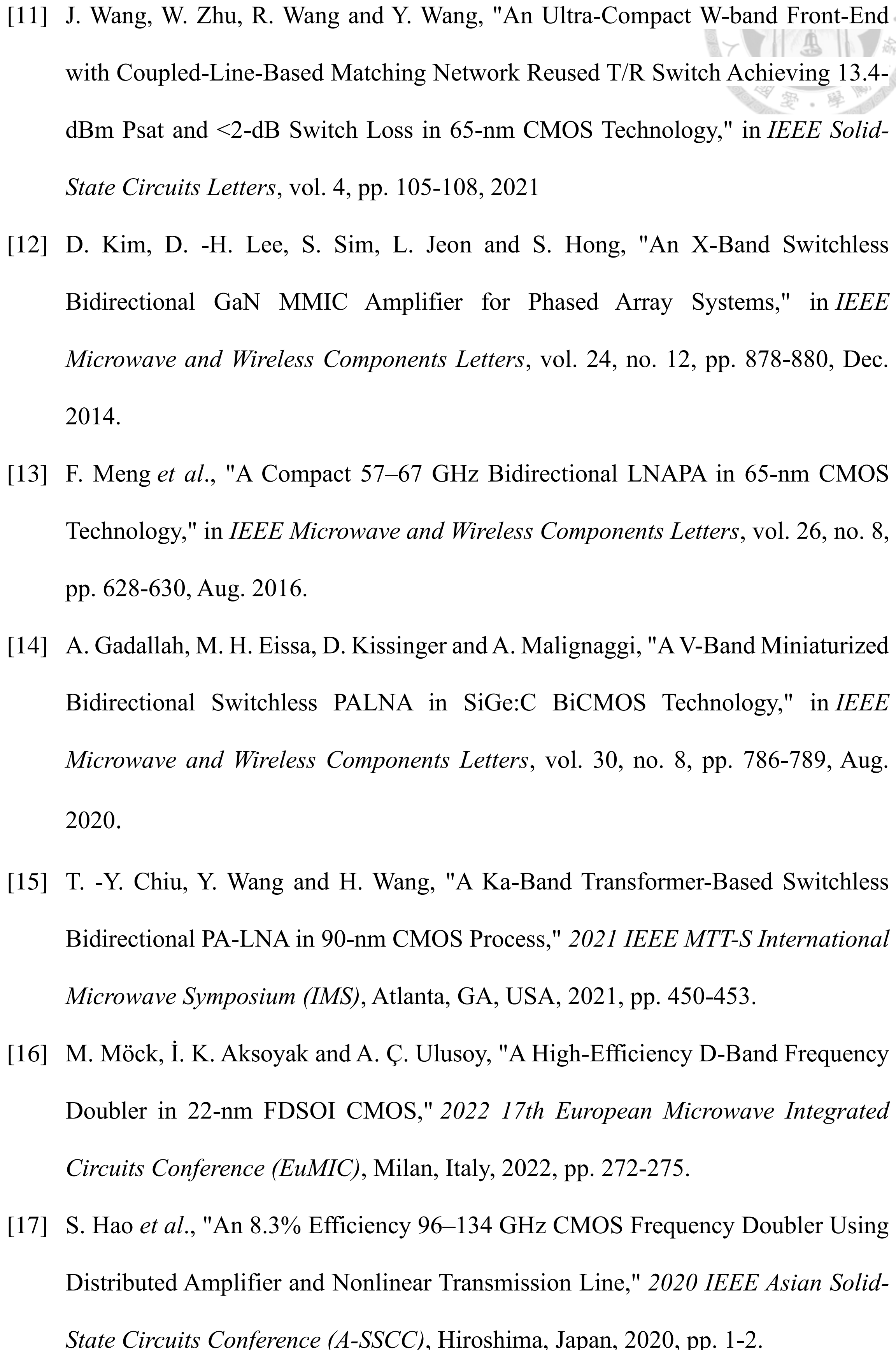

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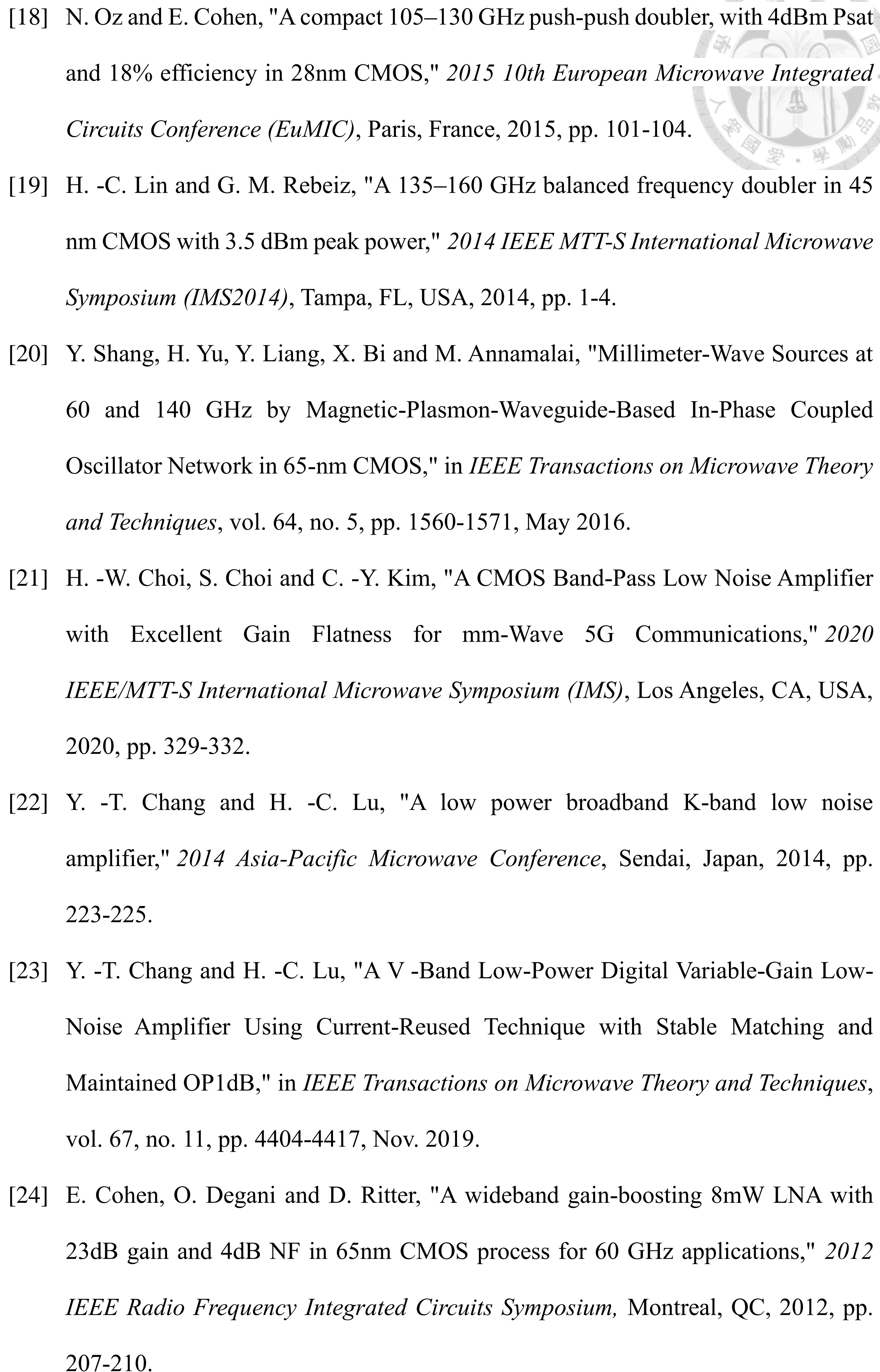

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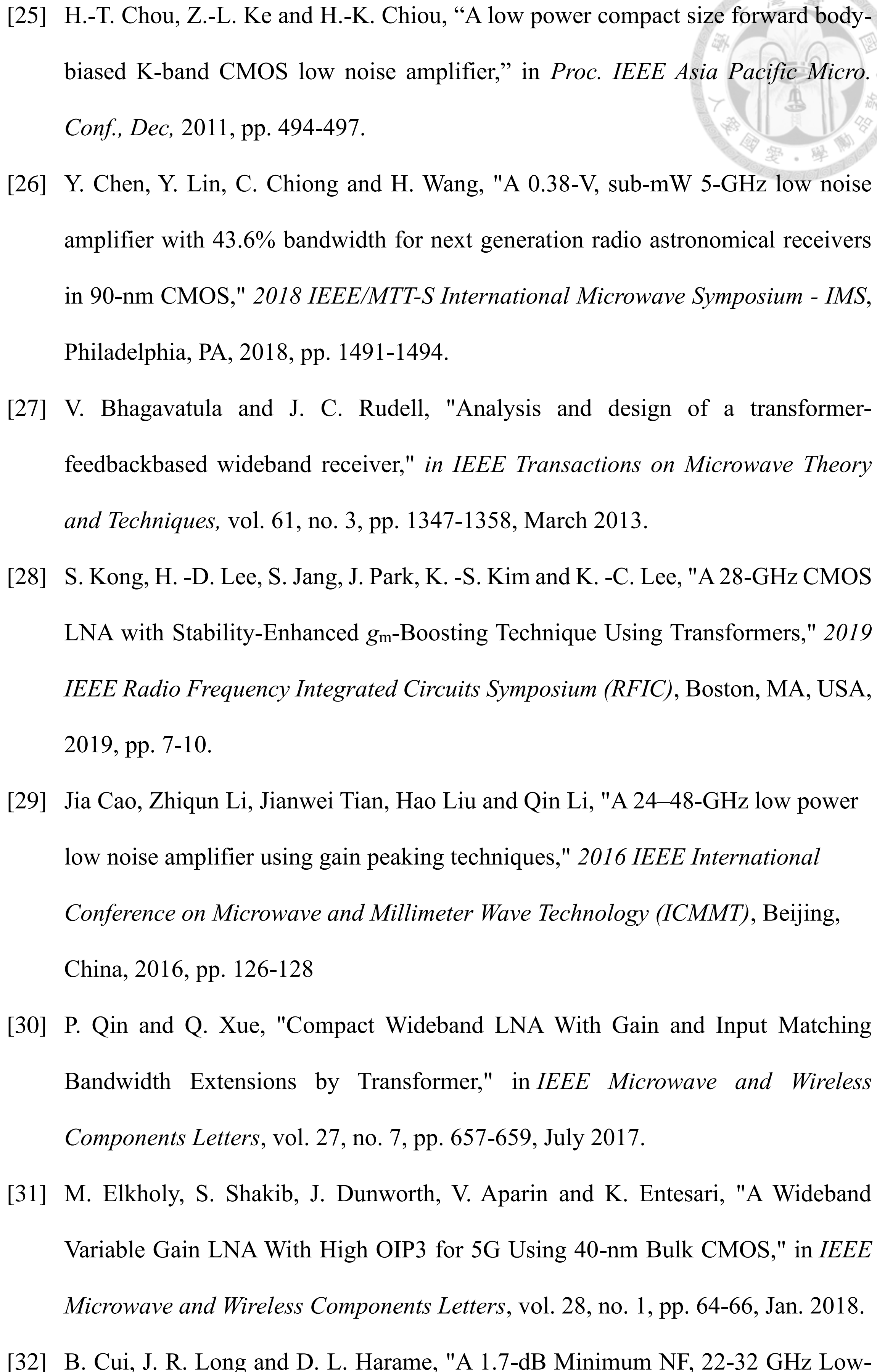

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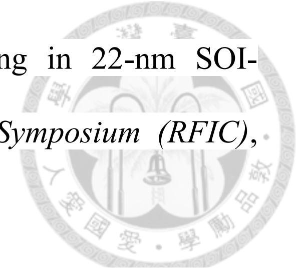

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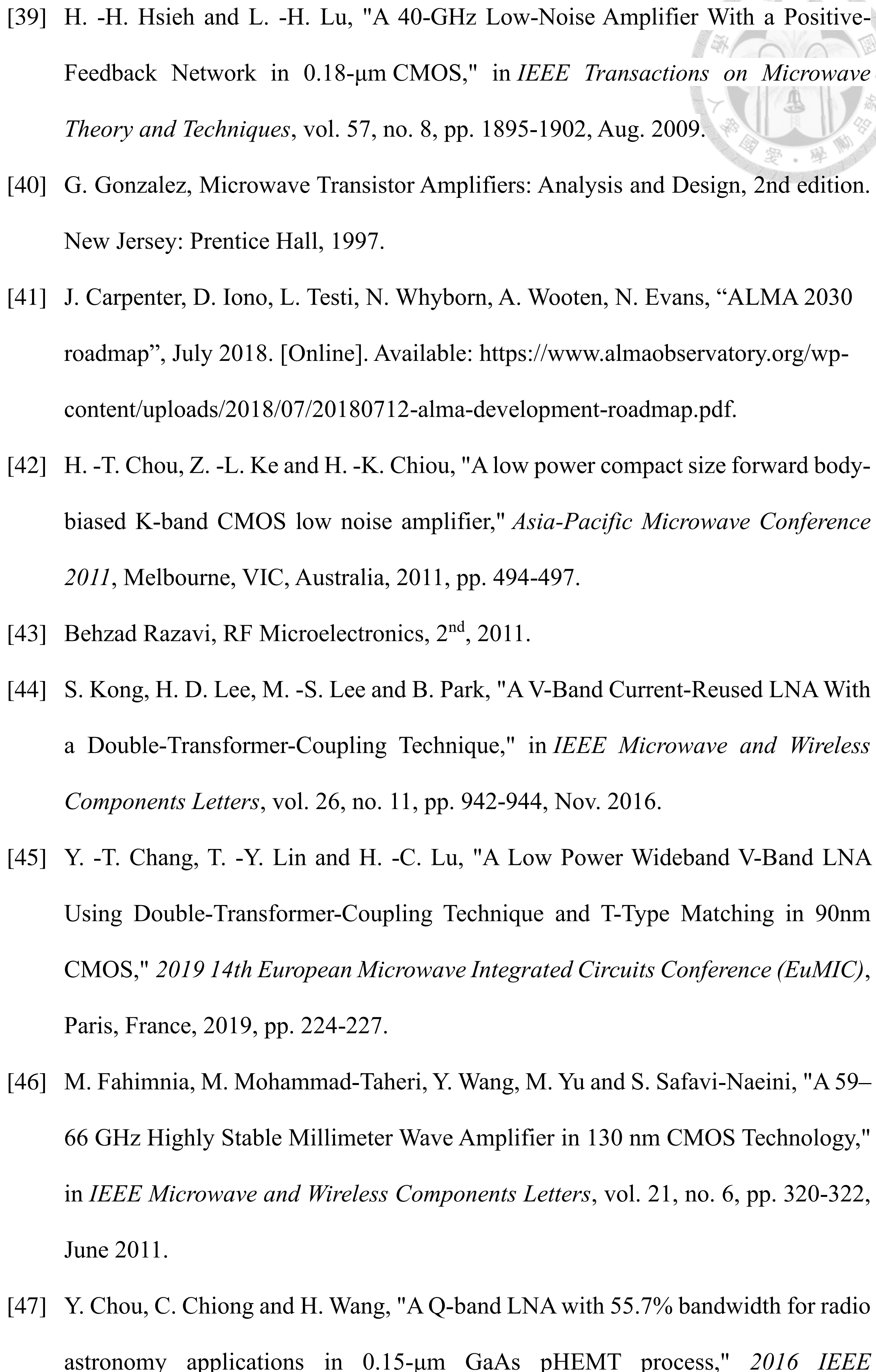

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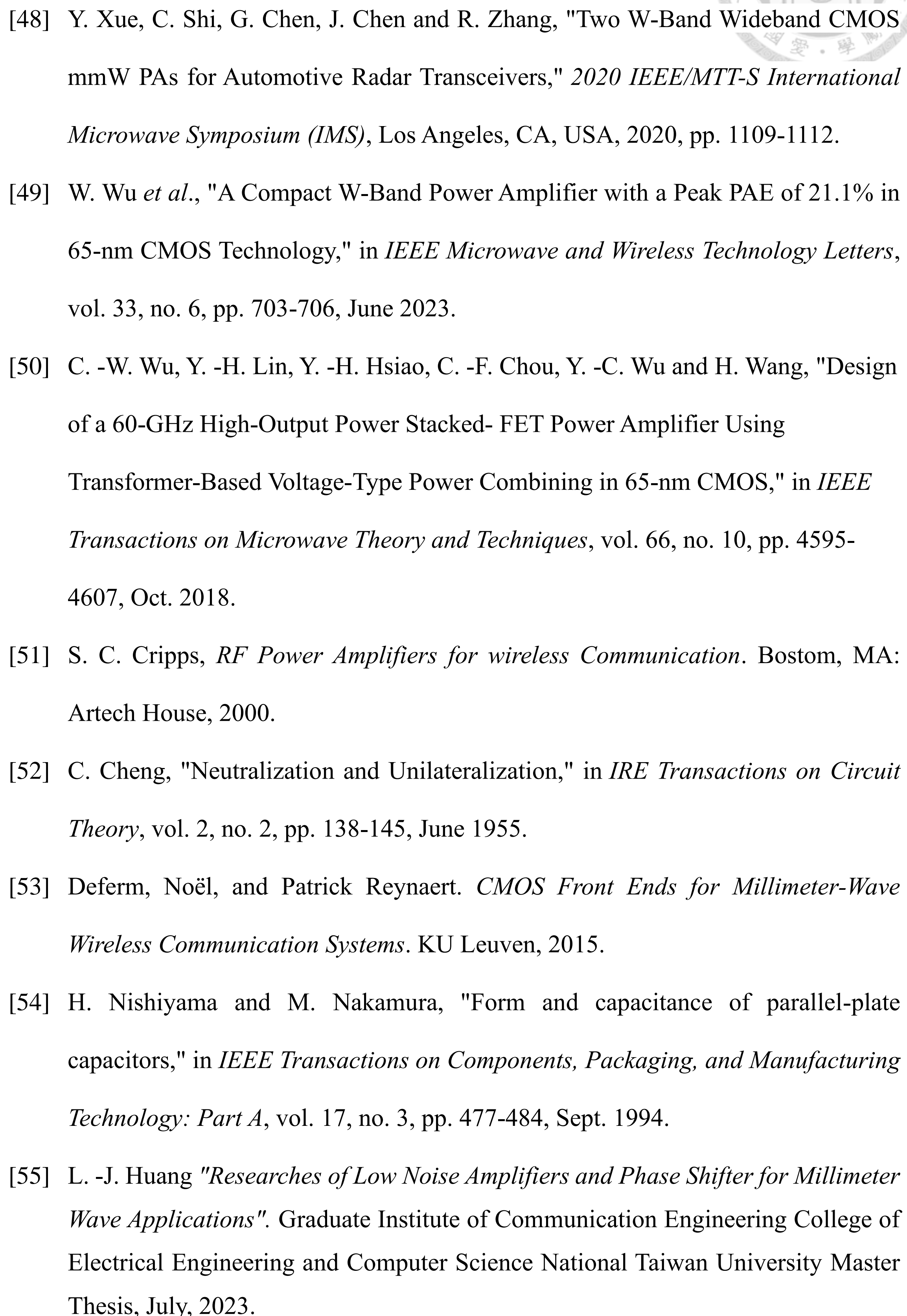

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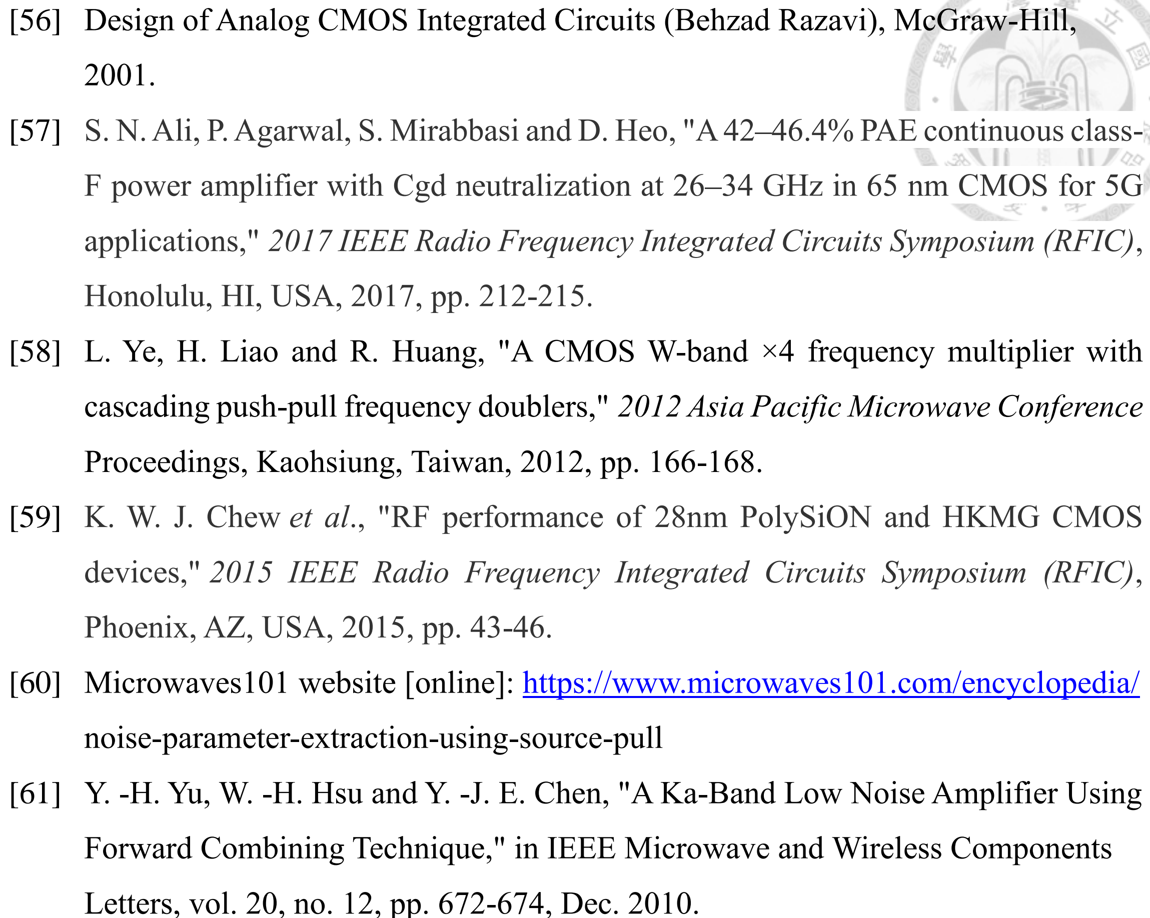

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