國立臺灣大學電機資訊學院電信工程學研究所

碩士論文

Graduate Institute of Communication Engineering
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Master's Thesis

應用於無線通訊與天文接收系統之 D 頻段與 Q 頻段 CMOS 低雜訊放大器設計

Design and Implementation of D-band and Q-band CMOS Low-Noise Amplifiers for Wireless Communication and Astronomical Receiver Applications

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致謝

在這份論文劃下句點之時，我必須首先提到王暉教授。回顧整個研究歷程，老師始終是幕後推手。在資源上大方支持晶片下線，在學術選題上更賦予我們充分自由，對投稿或發表的壓力，老師也憑藉豐富經驗化解我的不安。老師那份堅持與熱情，已成為我未來行路的座標。

回首這段研究歷程，剛進入實驗室時，面對複雜繁瑣的模擬參數與難以到達的設計目標感到不安與徬徨。那份挫敗感幾乎讓我懷疑自己的能力。然而，也正因如此，我學會了不斷地檢視問題、向學長姐請益，並在一次次討論與修正之間逐漸成長。這段歷程不僅讓我獲得知識與技能，更讓我學會如何在壓力下調整心態、在困境中尋找出路。

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中文摘要

本論文分為兩部分，分別針對 D 頻段及 Q 頻段低雜訊放大器（LNA）之設計與實測，應用於 6G 無線通訊與天文接收系統。

第一部分提出一款採用 65 奈米 CMOS 製程之 D 頻段 LNA，採用三級 Gmax-core 架構以兼顧高增益與低雜訊。第一級同步進行雜訊與輸入匹配最佳化，並提出改良之電晶體模擬方法，以提升高頻模擬與量測結果一致性。量測結果顯示，電路於 140 GHz 具 22 dB 峰值增益、8.2 dB 最低雜訊指數，於 130–145 GHz 頻帶內維持逾 15 dB 增益，直流功耗僅 17.3 mW，驗證 CMOS 技術於 6G 高頻前端應用之可行性。

第二部分則提出一款以 90 奈米 CMOS 製程實現之 Q 頻段 LNA。電路首級採用變壓器耦合共源共閘架構以抑制後級雜訊，並於次級導入電流再利用技術提升增益與功率效率。量測結果顯示，該 LNA 於 46.6 GHz 具 15.7 dB 最大增益，3 dB 頻寬覆蓋 36.6–46.6 GHz，最低及平均雜訊指數分別為 3.3 dB 與 3.8 dB，總直流功耗僅 7.8 mW，展現優異性能及良好權衡。

關鍵詞—低雜訊放大器（LNA）、D 頻段、Q 頻段、CMOS、Gmax-core、電流再利用、變壓器耦合共源共閘、6G 通訊、天文接收機。

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ABSTRACT

This thesis presents the design and measurement of low-noise amplifiers (LNAs) in the D-band and Q-band, targeting next-generation wireless communication systems and radio astronomy receivers.

The first part describes a D-band LNA fabricated using a 65-nm CMOS process, employing a three-stage Gmax-core architecture to achieve high gain and low noise. The first stage is optimized for noise and input matching, while an improved transistor modeling approach is introduced to enhance the agreement between simulation and measurement at high frequencies. The LNA demonstrates a peak gain of 22 dB at 140 GHz, a minimum noise figure of 8.2 dB, and maintains over 15 dB gain from 130 to 145 GHz. With a power consumption of 17.3 mW, the results confirm the feasibility of CMOS technology for high-frequency 6G front-end circuits.

The second part presents a Q-band LNA implemented in a 90-nm CMOS process. A transformer-coupled cascode is used in the first stage to suppress noise from subsequent stages, and a current-reuse technique is adopted in the second stage to boost gain with limited power. Measurement results show a maximum gain of 15.7 dB at 46.6 GHz and a 3-dB bandwidth of 36.6–46.6 GHz. The minimum and average noise figures are 3.3 dB and 3.8 dB, respectively. Total DC power consumption is only 7.8 mW, demonstrating an effective trade-off between gain, noise figure, and power efficiency.

Index Terms – Low-noise amplifier (LNA), D-band, Q-band, CMOS, Gmax-core, current-reuse, transformer-coupled cascode, 6G, radio astronomy.

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Chapter 1 Introduction

1.1 Background and Motivation

1.1.1 D-Band LNA for 6G Wireless Communication Systems

With the continuous advancement of wireless communication technologies, the sixth-generation (6G) wireless communication systems are expected to support higher data rates, lower latency, and massive device connectivity[1, 2]. To meet these requirements, the D-band (110 to 170 GHz) millimeter-wave spectrum has been identified as a promising candidate for future high-speed wireless communication systems due to its abundant spectral resources[3]. Potential applications include next-generation 6G systems and short-range, high-speed point-to-point communications.

As illustrated in Fig. 1.1, 6G wireless systems will be required to achieve extreme data rates (>100 Gbps), ultra-low latency (<1 ms), high reliability[4], massive connectivity (up to 10 million devices per km²), extensive coverage, and ultra-low power consumption[2]. These new combinations of requirements significantly exceed the capabilities of existing 5G systems and drive the demand for advanced RF front-end components, such as D-band low noise amplifiers, to enable practical implementations of 6G transceiver architectures.

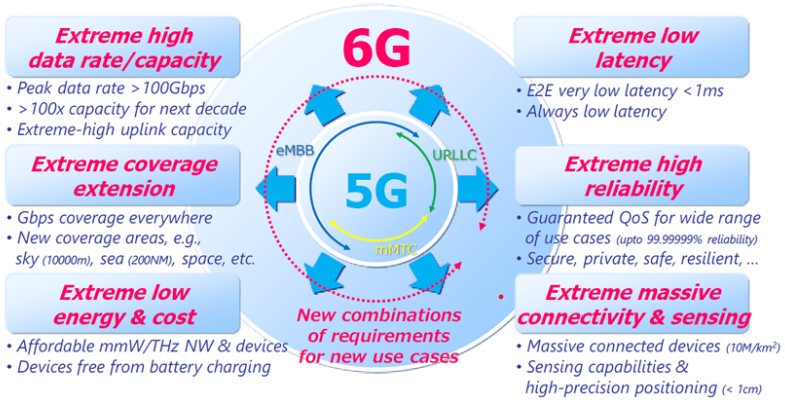

Fig. 1.1 Overview of 6G system scenarios.

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In D-band transceiver architectures, the low noise amplifier is typically implemented at the front-end of the receiver chain, where its gain and noise figure directly affect the overall receiver sensitivity and signal quality. As the operating frequency increases, device transconductance, noise parameters, parasitic effects, and process variations have been proven to degrade LNA performance at high frequencies, resulting in insufficient gain, elevated noise figure, and increased power consumption, thereby posing significant design challenges.

Currently, the main design challenges for D-band LNAs include gain and noise optimization, power consumption suppression, broadband operation, impedance matching, and stability control. In summary, to realize high speed, high capacity, and low latency in wireless communication systems, the key technologies for D-band LNAs are of critical importance.

1.1.2 Next-generation Radio Astronomical Receiving System

With the rapid advancement of large-scale radio telescope array projects, modern astronomy has continuously expanded both the depth and breadth of research on topics such as cosmic structure, star formation, and protoplanetary disk evolution. The Atacama Large Millimeter/submillimeter Array (ALMA) [5], recognized as the world's largest and most sensitive radio array, covers multiple observation bands from 30 GHz to 950 GHz and supports multi-band coordinated observations[6]. ALMA has made significant contributions to key scientific goals, including studies of protostellar disks, astrochemistry, and the early universe [5, 7].

In the realm of millimeter-wave and submillimeter-wave observations, the Q-band (33–50 GHz) has emerged as a critical frequency range due to its low atmospheric water vapor absorption and the availability of high-altitude, arid observational sites[8]. The Q-band plays a pivotal role in the observation of interstellar molecular clouds, star-forming

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regions, and molecular spectral lines in the universe. Its value extends to investigations of galactic evolution, disk structures, and the distribution of cosmic matter, making it an indispensable resource in contemporary radio astronomy[9, 10].

On the receiver front-end, Q-band receiver modules typically employ cryogenic low-noise amplifiers at the beginning of the signal chain to maximize system sensitivity and minimize the noise floor. Cryogenic LNAs are required to achieve high gain and ultra-low noise figures, ensuring that weak cosmic RF signals are faithfully delivered to subsequent processing modules. Room-temperature LNAs, on the other hand, are designed to compensate for waveguide and module losses, thereby further preserving signal integrity. The design and optimization of high-performance Q-band LNAs are therefore fundamental not only to data fidelity and the attainability of scientific outcomes, but also to the detection of rare or extremely faint astronomical phenomena, which pushes the boundaries of astronomical observation[11, 12].

In summary, enhancing the performance of Q-band LNAs in astronomical receiver systems is of critical importance for improving receiver sensitivity, broadening observational capabilities, and deepening our understanding of astronomical theories. Consequently, Q-band LNAs have become a focal point of research in both radio-frequency electronics and astronomical instrumentation.

1.2 Literature Surveys

1.2.1 D-Band Low Noise Amplifier in CMOS Process

In recent years, with the rapid development of high-frequency applications such as millimeter-wave (mmWave) communications and radar systems, D-band (110–170 GHz) low noise amplifiers have emerged as a significant research focus in the field of integrated

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circuits worldwide. Table 1.1 summarizes the key performance metrics of state-of-the-art D-band MMIC amplifiers implemented in various processes, including the employed process, circuit topology, operating frequency range, gain, noise figure, linearity, power consumption, and core area.

To achieve higher gain and broader bandwidth, current D-band LNA designs extensively adopt multi-stage cascade, differential circuit architectures, or gain-boosting techniques. In Table 1.1, the designs [13-19] represent notable CMOS implementations, while [20-22] summarize related results based on SiGe BiCMOS technology. At D-band frequencies, SiGe BiCMOS processes, benefiting from a higher transition frequency (F_t) and maximum oscillation frequency (F_{max}), offer superior gain and noise performance compared to CMOS, and have thus long been regarded as the ideal choice for high-frequency amplifier realization. Most SiGe BiCMOS LNAs can simultaneously achieve extremely low NF and high linearity over a wide bandwidth, making them suitable for high-end communication and radar systems with stringent requirements.

However, CMOS technology exhibits distinct advantages in terms of high integration, low cost, and low power consumption. With the continuous advancement of process technology, many recent works have demonstrated aggressive D-band LNA designs in advanced CMOS, whose gain, noise figure, and power consumption metrics are approaching those of SiGe BiCMOS. For instance, in [13], a 28-nm CMOS implementation employs a single common-source stage followed by four cascoded stages; the first stage is optimized for NF, while the subsequent stages enhance the overall gain, resulting in competitive performance. In [19], a 45-nm SOI process is utilized to realize a multi-stage differential architecture with neutralization capacitor design, albeit at the expense of higher cost and increased power consumption due to the SOI process and multi-stage differential structure. In [14], a 65-nm CMOS design introduces the Gmax-

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core technique, achieving a minimum noise figure of 4.7 dB at D-band. In fact, when gain is insufficient, many NF-optimization techniques, such as source degeneration, become limited, forcing the designer to trade off between gain and NF. Therefore, Gmax-core architectures that simultaneously address high gain and low NF have recently attracted increasing attention.

In summary, while SiGe BiCMOS technology continues to exhibit inherent advantages in terms of gain and noise performance at D-band frequencies, recent advances in CMOS processes have enabled the realization of LNAs with progressively improved metrics. By leveraging innovative circuit topologies and advanced matching techniques, state-of-the-art CMOS designs have begun to approach the performance levels traditionally associated with SiGe BiCMOS implementations. Therefore, this work seeks to further bridge the performance gap by demonstrating a competitive D-band LNA realized in a cost-effective CMOS process, addressing the requirements of next-generation high-speed communication and sensing systems for efficient and affordable solutions.

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Table 1.1 Summary of previously published D-band LNA

Ref.	Process	Architecture	Freq. (GHz)	Gain (dB)	NF (dB)	IP_{1dB} (dBm)	P_{dc} (mW)	Core Area (mm2)	FoM
[20]	130-nm SiGe BiCMOS	7×CS	140-220	15.8	6.1	-16.7	46.0	0.48	21.5
[21]	90-nm SiGe BiCMOS	3×cascode+1×CS	122-150	30.0	6.2	N/A	45.0	0.11	196.4
[22]	130-nm SiGe BiCMOS	2×cascode	119-135*	27.5	6.5	-33	12.0	0.4	216*
[13]	28 nm	4×cascode+1×CS	129-157.5	16.3	9.6	-19	38.8	0.4*	3.6
[14]	65 nm	2×CS(Gmax-core)	145-155	17.9	4.7	-23	13.7	0.193	23.1*
[15]	45 nm SOI	4×Differential CS	125.5-157	16.0	8.0	-14.5	75	0.07	3.1
[16]	28 nm	4×Differential CS	104-132*	21.7	8.4	N/A	18	0.12	14.4*
[17]	65 nm	6×Differential CS	116*	13.8	10.8	-26.8	40	0.605	1.2*
[18]	28 nm SOI	4×CS	143-166	15.7	8.5	N/A	32	0.34	4.4
[19]	45 nm SOI	3×CS	125-155*	9.9	N/A	N/A	38.25	0.347*	N/A

*estimate from graph

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1.2.2 Q-band Low Noise Amplifier in CMOS Process

As the first stage in the receiver chain, the noise figure of a low noise amplifier directly determines the overall system sensitivity. In recent years, regardless of whether Q-band LNAs are implemented in CMOS [23-26] or III-V processes [27, 28], minimizing the NF has remained the primary design objective. In addition to achieving low noise performance, sufficiently high gain is crucial to suppress the noise contribution from subsequent stages. Moreover, as communication system modulation schemes become increasingly complex, higher requirements for linearity parameters, such as the 1-dB compression point (P_{1dB}), have also been imposed to prevent signal distortion and to ensure overall system performance.

With respect to design trends, recent Q-band LNAs have increasingly focused on achieving wider bandwidth, smaller chip area, and lower power consumption. Representative studies in the literature have proposed broadband LNA designs covering the entire Q-band, as well as designs targeting ultra-low power consumption and ultra-compact chip area to address diverse application requirements. Table 1.2 summarizes the key performance metrics of recent representative Q-band LNA designs, including process technology, circuit topology, operating bandwidth, gain, noise figure, linearity, and power consumption.

In terms of circuit topology, the first stage of most designs still adopts the common-source (CS) configuration[23, 25, 29], combined with source degeneration inductors, which enables simultaneous input impedance and noise matching. While source degeneration is beneficial for improving stability and noise matching, it inevitably reduces gain, thereby limiting the noise suppression capability for subsequent stages. For ultra-low power applications, some designs have adopted current-reuse architectures[30] [23], achieving satisfactory gain performance under lower power consumption and thereby enhancing

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overall system efficiency. In recent years, numerous studies have focused on cascode architectures [24, 26, 31-33], aiming to broaden bandwidth and reduce noise, thereby addressing the inherent drawbacks of conventional cascode designs.

In summary, current research and development of Q-band LNAs focus on reducing noise, enhancing gain and linearity, while simultaneously achieving broadband operation, low power consumption, and compact chip area. Therefore, this work aims to implement a competitive Q-band LNA based on mature process technology and optimized circuit architecture to meet the requirements of high-performance and cost-effective receiver applications.

Table 1.2 Summary of previously published Q-band LNA

REF.	**Process**	**BW (GHz)**	**Gain (dB)**	**NF (dB)**	**P_{dc} (mW)**	**IP_{1dB} (dBm)**	**Area (mm^2)**	**FoM_1**	**FoM_2**
IMS'2012[26]	90-nm CMOS	29-44	13.8	3.8	18	-12.1	0.48	2.9	0.5
IMS'2012[30]	90-nm CMOS	38.6-41.7	10.6	5.4	0.92	N/A	0.19	4.6	N/A
TMTT'2011[24]	90-nm CMOS	34-46	20.3	4.6	15	-17.8	0.21	6	0.6
MWTL'2023[23]	90-nm CMOS	25.5-51.5	20.5	4.2	10.1	-25	0.6	16.7	0.9
APMC'2018[34]	90-nm CMOS	34.7-39.2	18.9	6.7	15.6	-20	0.2	0.95	0.1
RFIC' 2023[25]	65-nm CMOS	32-46	21.5	2.2	22	-17.6	0.16	9.7	2.2
RFIC' 2021[31]	28-nm CMOS	22.2-43	21.1	3.5	22.3	N/A	0.22	8.5	N/A
MWCL'2017[32]	65-nm CMOS	15.8-30.3	10.2	3.3	12.4	N/A	0.18	3.3	N/A
APMC' 2023[29]	180nm CMOS	36-42	15.3	7.3	73	-12.3	0.56	0.1	0.02
T-CASII'2018[33]	28-nm CMOS	30.6-35.3	18.6	4.9	9.7	N/A	0.23	2.0	N/A

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1.3 Contributions

This thesis presents the design of a D-band low noise amplifier implemented in a 65-nm CMOS process, as well as a Q-band low noise amplifier realized in a 90-nm CMOS process. The main contributions of these works are summarized in the following sections, and their potential impact is discussed.

1.3.1 Design of a D-band LNA with Gmax core in CMOS process

The proposed D-band LNA adopts a three-stage cascaded Gmax-core architecture. In contrast to conventional Gmax-core designs, where the gate and drain of the input transistor are directly connected and share the same bias voltage [14, 35, 36], this work introduces a DC blocking capacitor to separate the gate and drain DC bias voltages. This modification allows the transistor to be biased at a higher transconductance region, thereby improving gain performance and providing greater flexibility in biasing. Furthermore, a high-frequency circuit simulation methodology is developed. Unlike previous approaches that require manually adding correctional parasitic resistances and capacitances to the transistor model to improve simulation accuracy[37, 38], the proposed method incorporates electromagnetic (EM) simulation results of passive structures directly into the circuit-level simulation. This approach eliminates the need for manual parameter adjustment, providing more accurate and reliable high-frequency predictions while streamlining the simulation process.

The proposed LNA demonstrates a measured peak small-signal gain of 22 dB at the primary operating frequency of 140 GHz, and the gain above 15 dB across the 130–145 GHz frequency range. The minimum measured noise figure is 8.2 dB, and the circuit consumes 17.3 mW of DC power under a gate voltage of 0.7 V and a drain voltage of 1.2 V. Compared to most previously published D-band CMOS LNA designs, the proposed

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LNA exhibits superior overall performance. Implemented in a mature CMOS process, this work experimentally verifies the feasibility of CMOS RF circuits for high-frequency communication systems, demonstrating competitive performance at low cost. This design has been accepted for presentation at the 2024 Asia-Pacific Microwave Conference (APMC) [39].

1.3.2 Design of a Q-band LNA in CMOS Process

This work presents a Q-band low noise amplifier (LNA) implemented in a 90-nm CMOS process. To achieve high gain, low power consumption, and low noise performance, the first stage employs a transformer-coupled cascode architecture, enabling noise matching while suppressing the noise contribution of subsequent stages, while the second stage adopts a current-reuse technique to increase gain under constrained power. Compared with prior Q-band LNAs that mainly use single-ended common-source with source degeneration[23, 29], common-gate[40], or cascode topologies [31, 33, 34, 41], the proposed transformer-coupled cascode provides both noise matching and gain enhancement. In addition, unlike conventional multi-stage amplifiers with separate bias currents, the current-reuse design reduces total DC power to 7.8 mW, lower than many reported works with similar gain and noise figures. The measured 3-dB bandwidth of 36.6–46.6 GHz and minimum noise figure of 3.3 dB (average 3.8 dB) outperform several reported CMOS LNAs with narrower bandwidths or higher noise. These results confirm that the proposed LNA achieves a superior balance of gain, noise, bandwidth, and power efficiency compared with recent CMOS Q-band LNAs.

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1.4 Thesis Organization

The organization of this thesis is as follows:

Chapter 2 discusses the design and implementation of a D-band low noise amplifier based on a 65-nm CMOS process. The design procedure is described step by step, followed by a detailed analysis of the proposed LNA. The LNA adopts a three-stage Gmax core architecture to enhance the maximum stable gain in the D-band and simultaneously achieve noise and conjugate matching. This chapter also presents measurement results, a discussion of encountered issues, and a comparative summary with previously published works.

Chapter 3 presents a Q-band low noise amplifier designed in a 90-nm CMOS process. The design features of the proposed LNA are described in detail, including the use of a transformer-coupled cascode to suppress subsequent-stage noise and the implementation of a current-reuse technique to realize broadband and flat performance. Experimental results, design characteristics, and comparison tables are also provided in this chapter.

Finally, Chapter 4 summarizes the main content of the thesis and highlights the key findings of the preceding chapters.

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Chapter 2 Design of a 140 GHz Low-Noise Amplifier in 65-nm CMOS

2.1 Introduction

The D-band (110–170 GHz), with its extremely wide spectrum and high-speed transmission capability, has become a key technology for advanced applications such as 6G wireless communications, sensing, and imaging. In particular, D-band transceivers leverage high frequency and large bandwidth to support high data rates and multi-band operation, making them widely used in 6G base stations, radar systems, and high-resolution imaging fields. Compared with lower frequency bands, the D-band not only offers higher data rates and lower latency, but is also suitable for diverse scenarios such as security surveillance, automotive radar, and non-destructive testing. With the advent of the 6G era, there is an increasing demand for high-frequency, large-bandwidth, and low-noise front-end circuits. However, high-frequency technology also brings design challenges, including signal loss, component noise, and antenna integration. Thus, how to design D-band transceivers with both a wide bandwidth and low noise has become a critical factor for the development of 6G and related applications.

The D-band covers a wide range of applications, including wireless communications, imaging, sensing, and astronomical observations. For example, the 135 GHz ASK transceiver [42], the 160 GHz transceiver [43], the D-band transceiver front-end[44], the D-band power amplifier[45], the D-band gain-boosted current-bleeding mixer [46], and the D-band imaging-specific LNA[21] all demonstrate its potential and value in various fields.

At such a high frequency as the D-band (110–170 GHz), circuit design faces numerous technical challenges. First, high-frequency signals are susceptible to

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atmospheric absorption and blockage during propagation, leading to significant signal attenuation and limited communication distance. Second, parasitic capacitance and parasitic inductance of circuit components become more prominent at high frequencies, resulting in reduced gain, increased noise, and narrowed bandwidth, which further increase the design difficulty. In addition, when operating near the F_t and F_{max} of the CMOS process, the gain of active devices is limited, and passive losses increase substantially, raising the complexity of circuit integration. Achieving both high gain and low noise in LNA design within the D-band is extremely challenging and requires overcoming multiple issues such as process variation, power consumption, and noise matching.

The Low Noise Amplifier plays a crucial role in the wireless receiver chain, being the first stage at the receiver front-end. Its main function is to amplify weak RF signals while suppressing additional noise, directly determining the overall system sensitivity and noise performance. Especially in high-frequency applications such as the D-band, low-noise design is even more critical. Receiver sensitivity is defined as the minimum input signal power that the system can effectively detect, which is limited by the system noise figure (NF_{sys}), and is expressed as follows[47]:

$$Sensitivity = kT_0 \cdot BW \cdot (S/N)_{min} \cdot NF_{sys} \tag{2.1}$$

k is Boltzmann's constant, T_0 is absolute temperature, BW is receiver bandwidth, $(S/N)_{min}$ is the minimum detectable signal-to-noise ratio, and NF_{sys} is the overall system noise figure. According to Friis' formula for cascade noise figure analysis, the noise figure of the first-stage LNA has a decisive influence on the total system NF. The formula is as follows[48]:

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \ \ldots \tag{2.2}$$

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Therefore, the lower the LNA's NF, the higher the system sensitivity, and the impact of noise from subsequent stages is diminished as the front-end gain increases. Thus, a low-NF design is the key to improving system sensitivity.

Fig. 2.1 illustrates the overall architecture of the 140 GHz receiver system discussed in this thesis. The signal from the antenna is first amplified by a low-noise amplifier to strengthen the weak 140 GHz RF signal. The amplified signal is then sent to an I/Q sub-harmonic mixer, where it is down-converted from RF to intermediate frequency (IF). The local oscillator (LO) signal required by the mixer is generated by a frequency sextupler (X6), amplified by a driver amplifier, and then delivered to the mixer to provide stable LO drive. After frequency conversion, the I/Q IF signals are buffered and amplified, and finally sent to the data acquisition circuit for further processing.

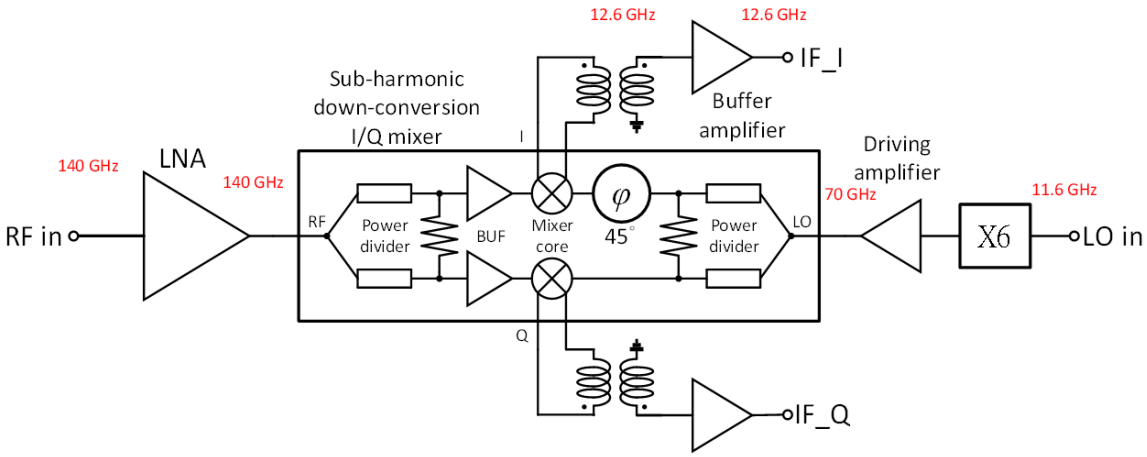

Fig. 2.1 Block diagram of 140-GHz receiver system.

Under this system architecture, the LNA's performance directly affects the receiver's ability to process weak signals and the quality of subsequent data processing. In consideration of the cost of fabricating a 140 GHz receiver system, and to ensure good gain and low noise at very high frequencies, a 65-nm CMOS process is selected. This ensures the LNA can effectively amplify weak RF signals at the front end, enhance overall

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system sensitivity, and reduce the burden on downstream mixers and data acquisition circuits. The noise figure is set to be less than 8 dB, and the gain is set to be greater than 15 dB, with the aim of minimizing the total system noise figure and significantly improving reception quality. The power consumption is limited to below 30 mW, focusing on stable long-term operation and portability, avoiding excessive power dissipation that could cause thermal or reliability issues. The input 1-dB compression point (IP_{1dB}, -20 dBm) reflects the linearity requirement of the LNA under large signal input, ensuring the system does not experience distortion or performance degradation in high dynamic range operations.

This thesis targets 6G wireless communication applications, designing and implementing a 140 GHz LNA to meet the needs of low-cost, high-sensitivity, and highly integrated receiver front-ends. The target specifications for this LNA include:

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Table 2.1 The design goals of the D-band LNA in the 140-GHz receiver system.

	Specification
Process	65-nm CMOS process
Frequency (GHz)	127-153
Gain (dB)	15
Noise Figure(dB)	8
IP_{1dB} **(dBm)**	-20
Power consumption (mW)	30

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2.2 The Design of D-band LNA

2.2.1 Transistor Size and Biasing Selection

The key performance of a low-noise amplifier includes gain, noise figure, and stability, which are critical in high-frequency applications such as at 140 GHz. The gain and noise performance of an LNA are highly dependent on device bias conditions and transistor size. Fig. 2.2 and Fig. 2.3 show the transconductance and drain current of the transistor versus V_g with V_d = 1.2V, and the transistor size is 1μm×12fingers. The maximum g_m is achieved at V_g=0.9; however, based on experience in LNA design, achieving the highest transconductance does not lead to the best noise performance. Considering gain, noise figure, and dc power consumption, V_g is set to 0.7V at first, corresponding to 60% of the g_m peak current, as shown in Fig. 2.2. After setting the bias conditions, the device's size should be determined. To select device size, the MSG/MAG, NFmin, and stability factors at the target frequency are the primary concerns. Fig. 2.4 illustrates MSG/MAG, NFmin, and stability factor with different gate widths. Though smaller devices have better MSG and lower NFmin, their stability is also weak. With the bias condition, the transistor gate width is selected as 1μm with 12fingers, which allows a high gain and appropriate stability below 150 GHz, as shown in Fig. 2.4 to Fig. 2.6. In Fig. 2.7 and Fig. 2.8, various size combinations with the same DC power were compared. The 1 μm × 12 fingers demonstrate the best performance at the target frequency. The previous work also indicates that around the size is appropriate[14]. Fig. 2.10 depicts the MSG/MAG and NFmin versus V_g of the 1 μm × 12 fingers device. As shown in Fig. 2.10, the minimum NFmin occurs at V_g = 0.6V while the maximum MSG/MAG occurs at V_g = 0.9V. Considering the balance between gain and NF, V_g = 0.7V is determined, which is consistent with the result from DC simulations.

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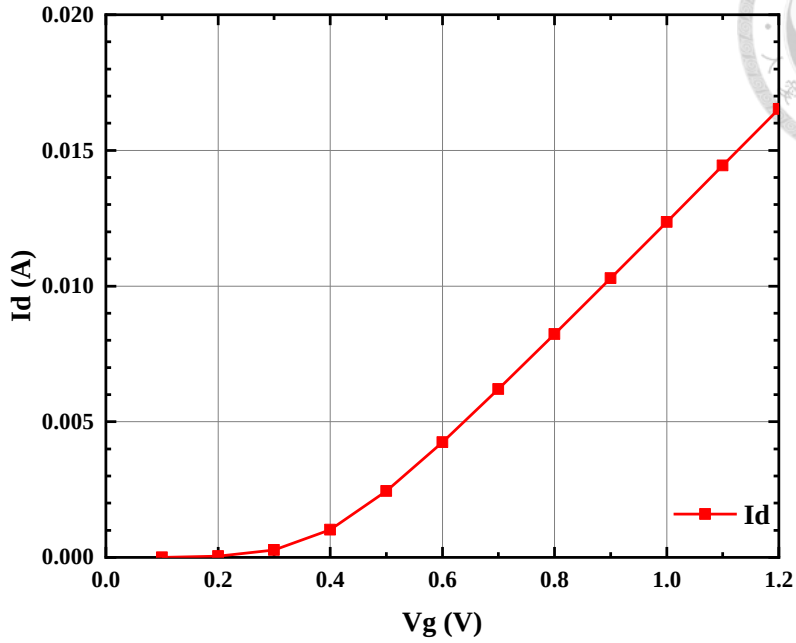

Fig. 2.2 Drain current of the transistor versus V_g. (V_d=1.2 V, w=12fingers×1.2μm)

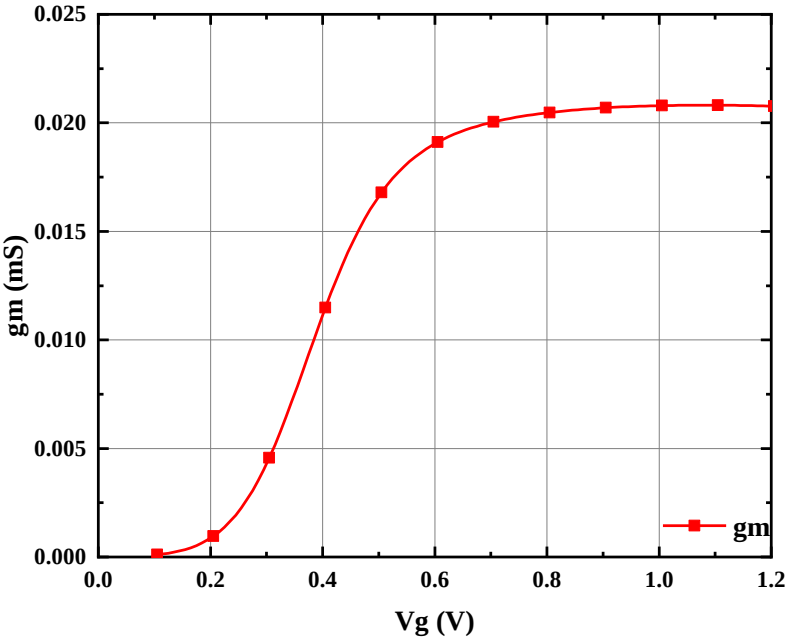

Fig. 2.3 transconductance of the transistor versus V_g.(V_d=1.2 V, w=12fingers×1.2μm)

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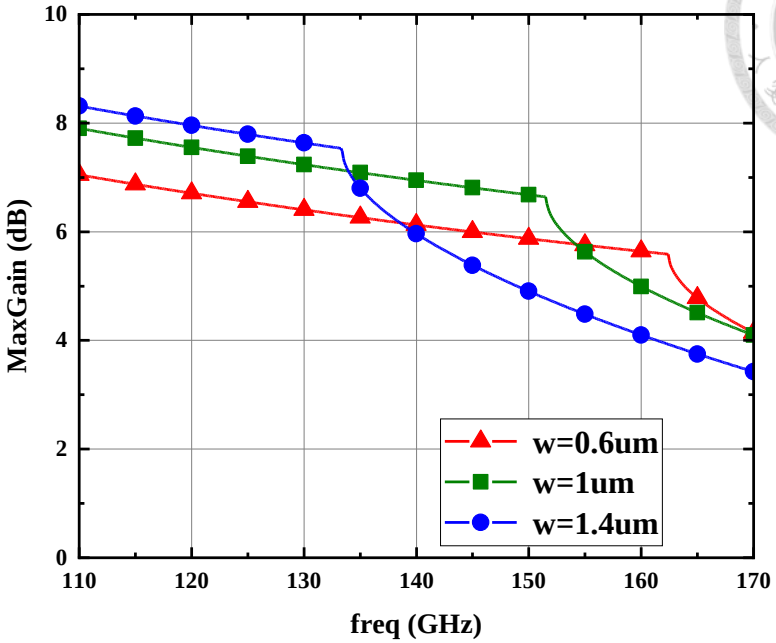

Fig. 2.4 MSG/MAG with different gate widths. (V_g=0.7 V, V_d=1.2 V, finger=12)

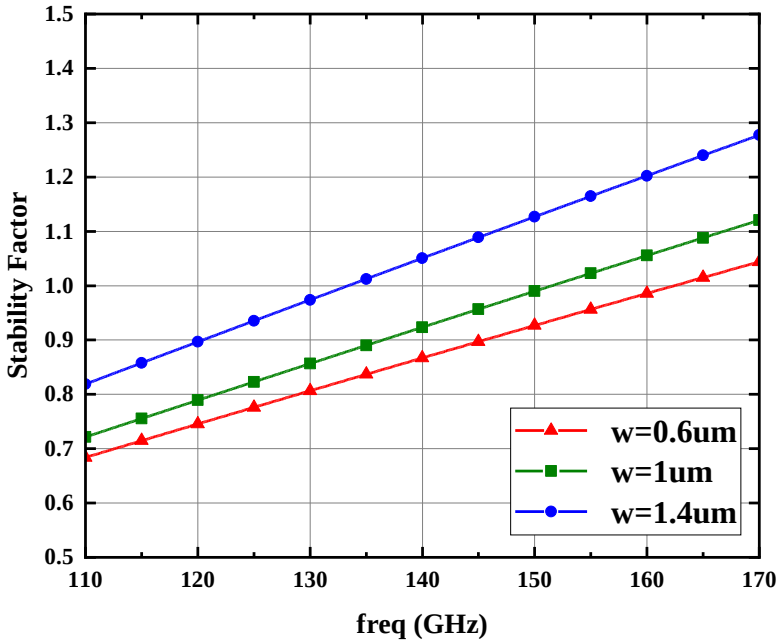

Fig. 2.5 stability factors with different gate widths. (V_g=0.7 V, V_d=1.2 V, finger=12)

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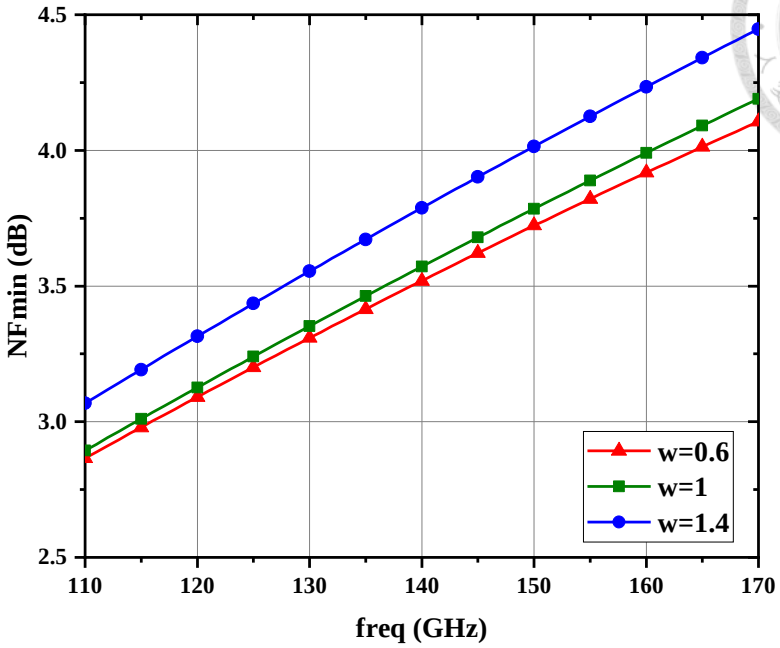

Fig. 2.6 NF_{min} with different gate widths (V_g=0.7 V, V_d=1.2 V, finger=12)

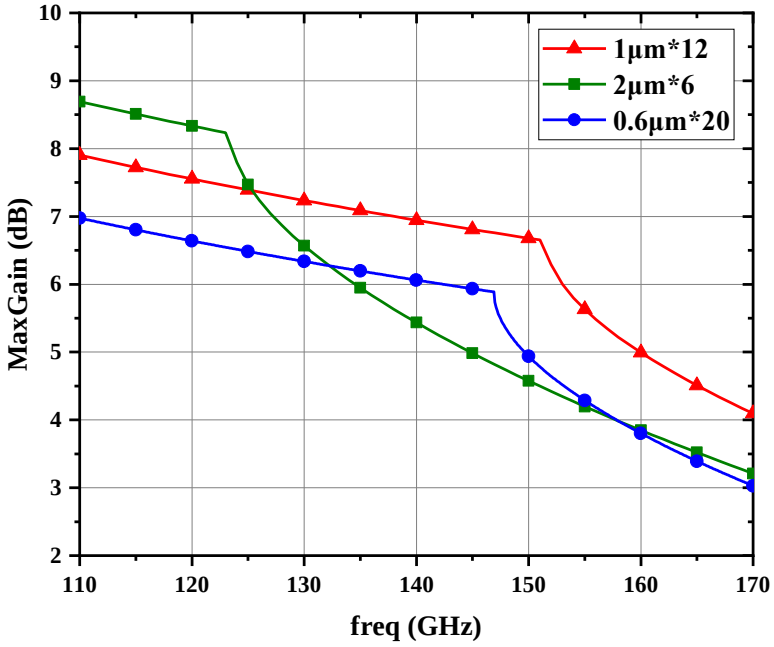

Fig. 2.7 MSG/MAG with different finger combinations. (V_g=0.7 V, V_d=1.2 V)

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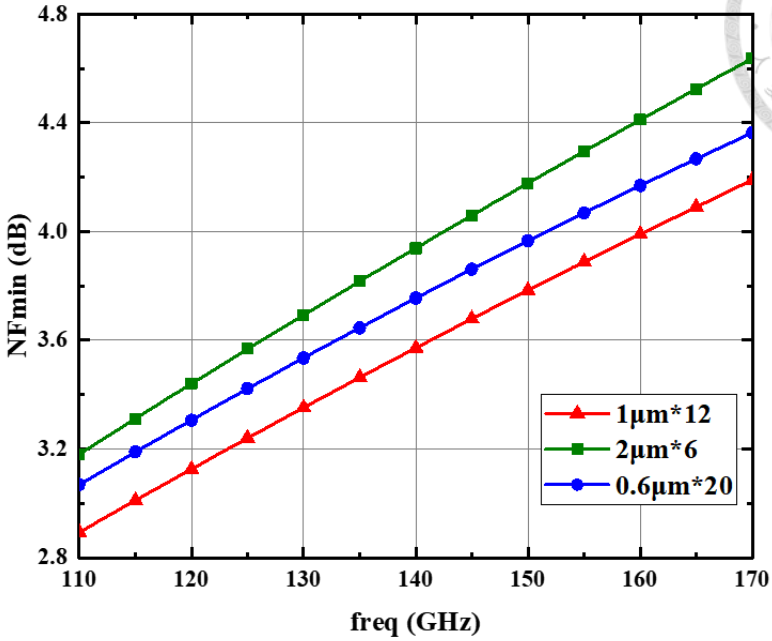

Fig. 2.8 NF_{min} with different finger combinations. (V_g=0.7 V, V_d=1.2 V)

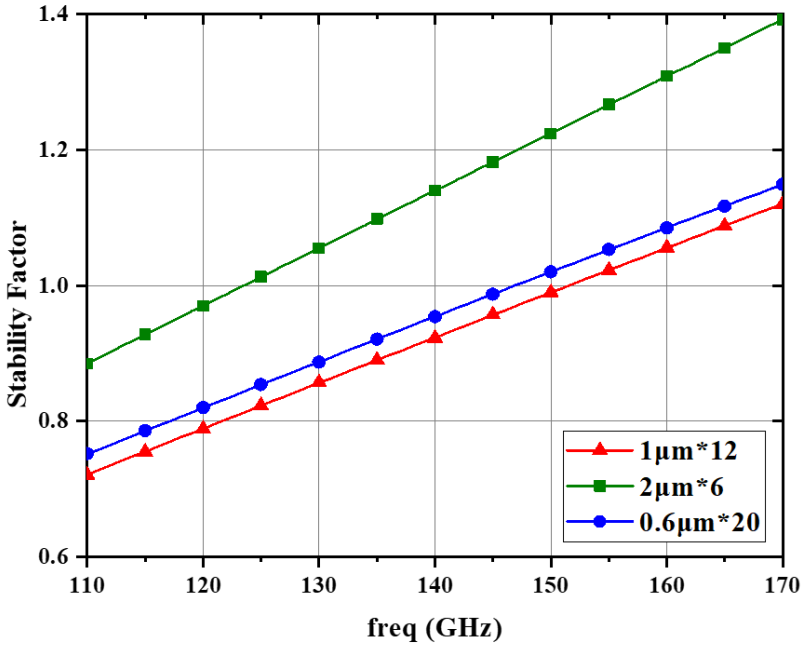

Fig. 2.9 stability factors with different finger combinations. (V_g=0.7 V, V_d=1.2 V)

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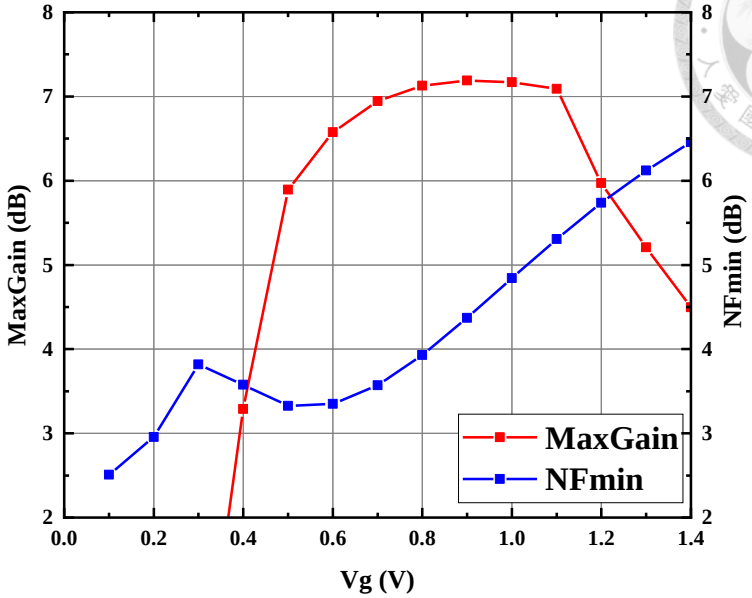

Fig. 2.10 MSG and NF_{min} of the transistor (V_d=1.2 V, w=1×12 μm)

2.2.2 Gmax-Core Architecture Design

This section discusses in detail the design basis of the Gmax core. This design is based on an embedded network consisting of three transmission lines shown in Fig. 2.11. The gain characteristics of the transistor are optimized by adjusting the embedded network parameters.

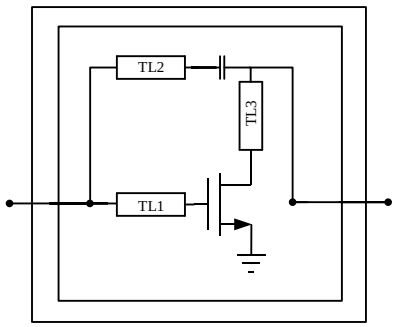

Fig. 2.11 Schematic diagram of the Gmax core

In millimeter-wave LNA design, Maximum Available Gain is an important indicator for evaluating the intrinsic gain capability of transistors. For a two-port network, MAG can be expressed as[49]:

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$$G_{ma} = \left|\frac{S_{21}}{S_{12}}\right| \times \left(k - \sqrt{k^2 - 1}\right) = |A| \times a \tag{2.3}$$

where A is the ratio of forward to reverse transmission coefficients and θ is the angle of $\angle A$, defined as:

$$A = \frac{S_{21}}{S_{12}} = |A| \times e^{j\theta} \tag{2.4}$$

Where θ is and a is a function of the stability factor k, given by:

$$a = k - \sqrt{k^2 - 1} \tag{2.5}$$

Through the above formula, we can clearly see the relationship between the maximum available gain G_{ma}, the stability factor k, and the phase difference θ.

In Gmax core design, another important parameter is the unilateral power gain (U), which can be expressed by S parameters as:

$$\mathrm{U} = \frac{|S_{21}/S_{12} - 1|^2}{2k|S_{21}/S_{12}| - 2\mathrm{Re}(S_{21}/S_{12})} \tag{2.6}$$

Using the relationship A=$S21/S12$, the above expression can be rewritten as:

$$\mathrm{U} = \frac{|A - 1|^2}{2k|A| - 2\mathrm{Re}(A)} \tag{2.7}$$

Further derivation, the relationship between U and G_{ma} can be obtained:

$$\mathrm{U} = \frac{{G_{ma}}^2/a^2 - 2\,G_{ma}/a^2 \cdot cos\theta + 1}{(a^2 + 1)/a \cdot G_{ma}/a - 2\,G_{ma}/a \cdot cos\theta} \tag{2.8}$$

After mathematical organization, the following quadratic equation is satisfied between G_{ma} and U:

$${G_{ma}}^2 - G_{ma}[Ua^2 - 2acos\theta(U - 1) + U] + a^2 = 0 \tag{2.9}$$

To solve this equation:

$$G_{ma} = \frac{1}{2}\left[Ua^2 - 2a\cos\theta\,(U - 1) + U + \sqrt{(Ua^2 - 2a\cos\theta\,(U - 1) + U)^2 - 4a^2}\right] \tag{2.10}$$

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According to the derivation, when the embedded network operates within the unconditional stability region $(1 \leq k \leq \infty)$ and $(-1 \leq \cos\theta \leq 1)$, G_{ma} reaches its maximum value when $k = 1$ and $\cos\theta = -1$,i.e. $(\theta = \pm\pi)$. Under this condition, G_{ma} is solely determined by the unilateral power gain U, and the expression simplifies to:

$$G_{ma} = 2\mathrm{U} - 1 + 2\sqrt{U(U-1)} \tag{2.11}$$

2.2.3 Transmission Line-Based Matching Network

In this embedded matching network design shown in Fig. 2.12, three transmission lines with reactances of jX_1 to jX_3 and a DC-blocking capacitor are required to satisfy the conditions K = 1 and θ = ±π. Since there are three unknowns and only two equations, there exist infinitely many solutions for the embedded network that fulfill these criteria. Once the required reactances are obtained, the actual physical lengths can be determined using the transmission line equation. Typically, low noise amplifiers employ a source degeneration inductor to achieve optimal noise and gain matching simultaneously. However, at the D-band frequency range, the implementation of additional inductors is not only challenging but also significantly reduces the achievable gain. Therefore, the proposed design adopts a Gmax-core architecture, in which the optimal noise and gain matching points are made coincident by properly selecting the parameters of the embedded transmission lines, thereby enabling high gain and low noise performance simultaneously.

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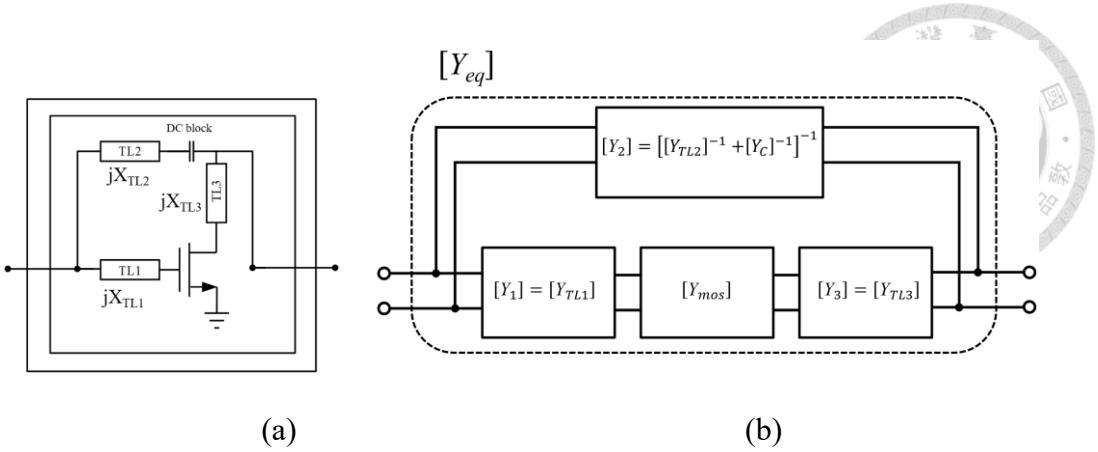

(a) (b)

Fig. 2.12 (a) Gmax-core Architecture (b) Equivalent Y-parameter model

As illustrated in Fig. 2.12, a single-stage Gmax core consists of three transmission lines, including a DC-blocking capacitor for bias isolation. The DC-block was considered first. The capacitance is chosen at 200 fF, which provides an insertion loss of less than 0.7 dB at the target frequency, as shown in Fig. 2.14. By applying the derived conditions for $K = 1$ and $\theta = \pm\pi$, the required reactances jX_1 to jX_3 are determined, and the corresponding physical lengths are calculated according to the impedance transformation formula. The characteristic impedances are then selected based on the calculated reactances and required lengths.

$$X = Z_0 \tan(\frac{2\pi}{\lambda} L_s) \tag{2.12}$$

$$L_s = \frac{\lambda}{2\pi} \tan^{-1}\left(\frac{X}{Z_0}\right) \tag{2.13}$$

In the Advanced Design System (ADS), the matching network can be directly implemented using transmission lines. As long as the core conditions are satisfied, the Gmax core can be formed. For LNA design, it is also essential that the optimal noise and gain matching points are sufficiently close to achieve low noise while maintaining high gain.

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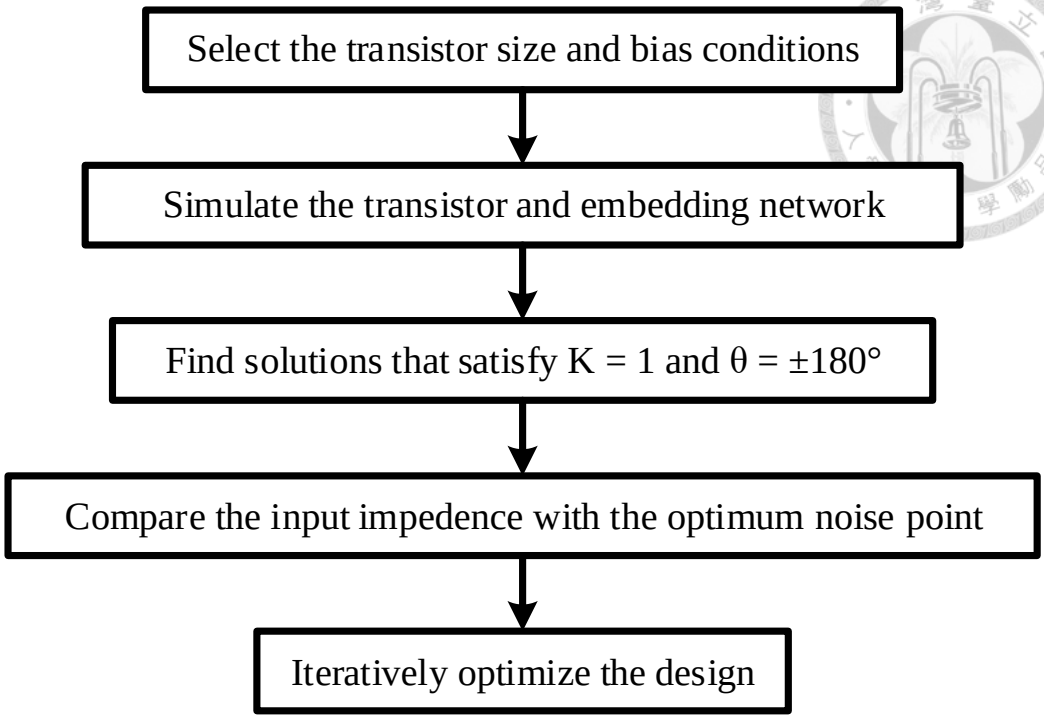

Fig. 2.13 Design flowchart of the Gmax-core.

Fig. 2.13 shows the design flow of the Gmax-core-based LNA, which involves device sizing and bias selection, transistor parameter simulation, determination of solutions satisfying K=1 and θ=±180°, comparison with the optimal noise point, and iterative optimization to simultaneously achieve maximum gain and minimum noise figure. Taking a single-stage amplifier as an example, experience results show that jX_2 is generally larger than jX_1, and thus the third transmission line requires a higher characteristic impedance to provide the necessary reactance. In this work, considering the minimum line width of 2 μm in the 65-nm process corresponds to a characteristic impedance of approximately 74 Ω, the values are set as $Z_1 = Z_2 = 50$ Ω and $Z_3 = 74$ Ω. A higher Z_3 enables a larger jX_3 with the same physical length, reducing the inter-stage matching line length, minimizing loss, and saving chip area. The values of X_1 to X_3 can be converted to physical lengths L_1 to L_3 by the aforementioned equations. With L_3 fixed at 90 μm, L_1 and L_2 are swept in the simulation. The optimal condition is achieved when

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$L2$ = 204 μm and $L3$ = 85 μm, simultaneously satisfying $K = 1$ and $\angle A = \angle (S_{21}/S_{12}) = \pm\pi$, as illustrated in Fig. 2.15 and Fig. 2.16. Under these conditions, Fig. 2.17 shows that the optimal noise matching and conjugate matching points are closely aligned, resulting in both high gain and low noise. This configuration achieves excellent gain and competitive noise performance near the target frequency of 140 GHz. As shown in Fig. 2.18 and Fig. 2.19, the maximum available gain increases from 7 dB to 8.5 dB at approximately 140 GHz.

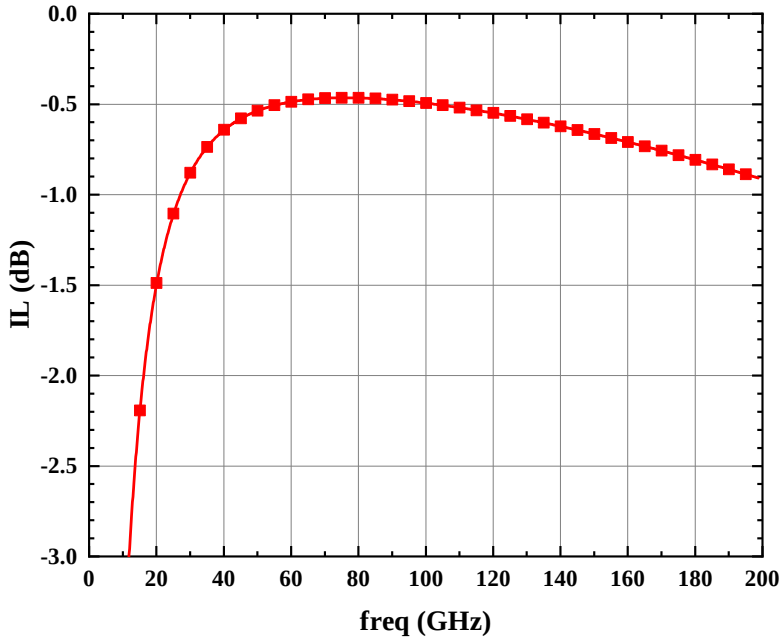

Fig. 2.14 Simulated isolation of the DC block.

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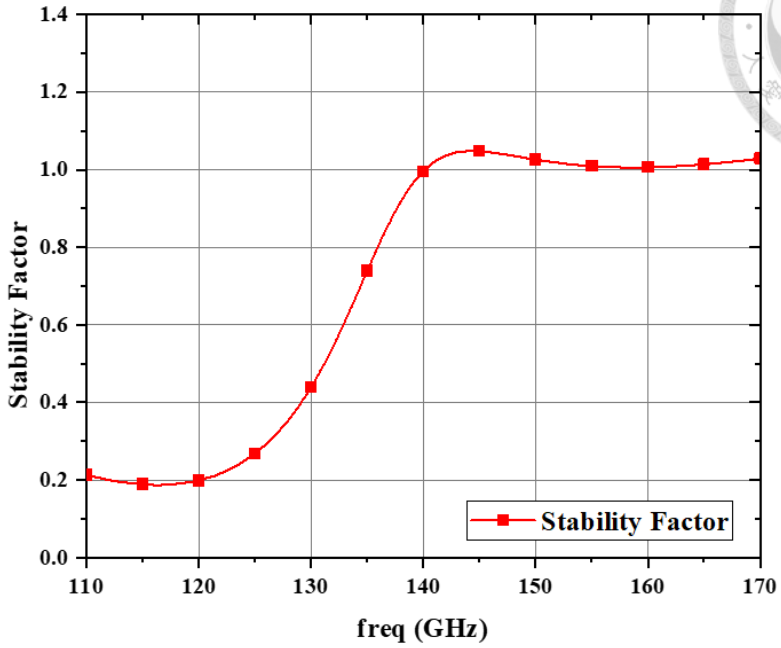

Fig. 2.15 Stability factor of Gmax core.

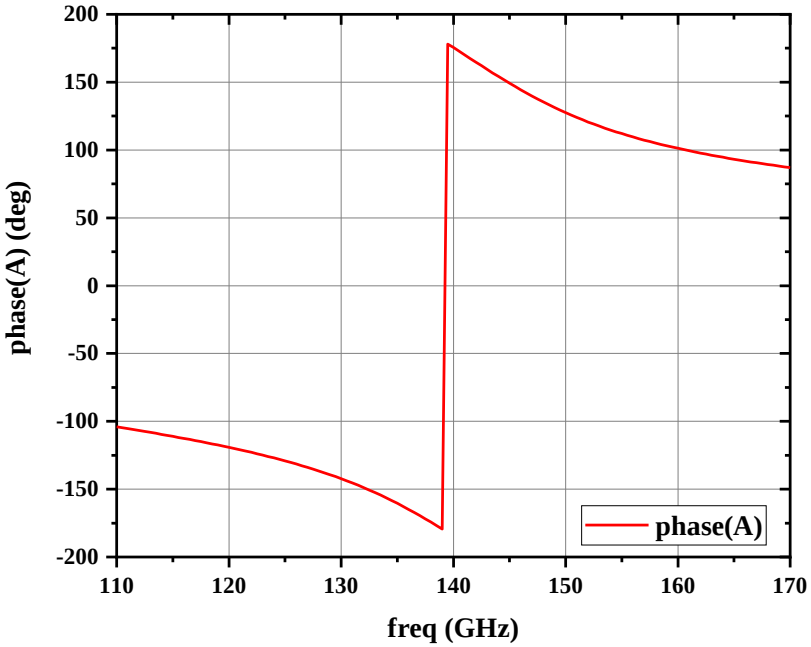

Fig. 2.16 The phase of S_{21}/S_{12} (A).

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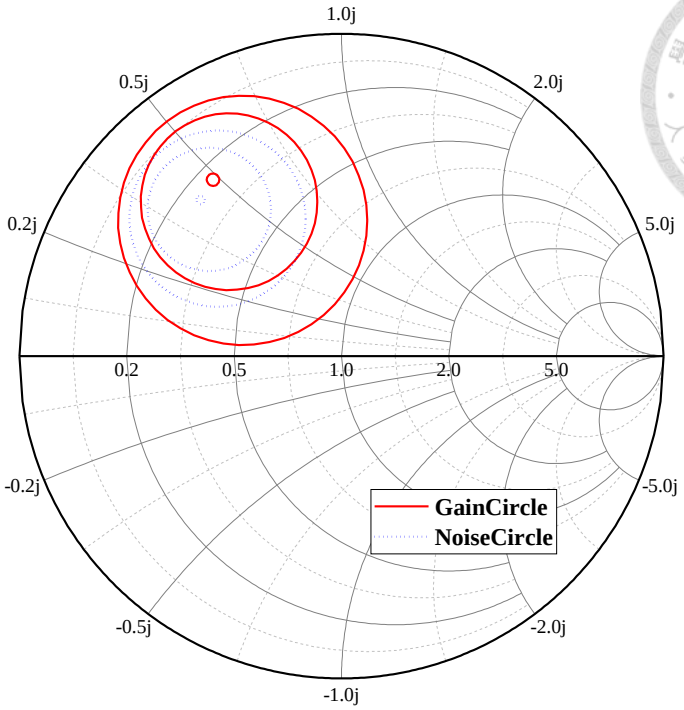

Fig. 2.17 The constant circle of noise and available gain.
Maximum available gain is 8.4 dB with a step size of 0.4 dB.
Minimum noise figure is 5.9 dB with a step size of 0.4 dB.

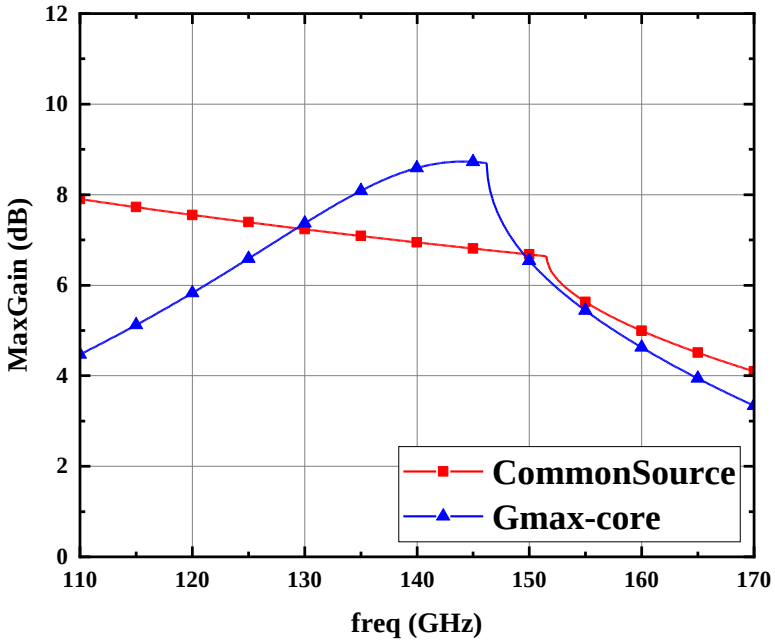

Fig. 2.18 Comparison of Gmax-core and common source of simulated maximum gain.

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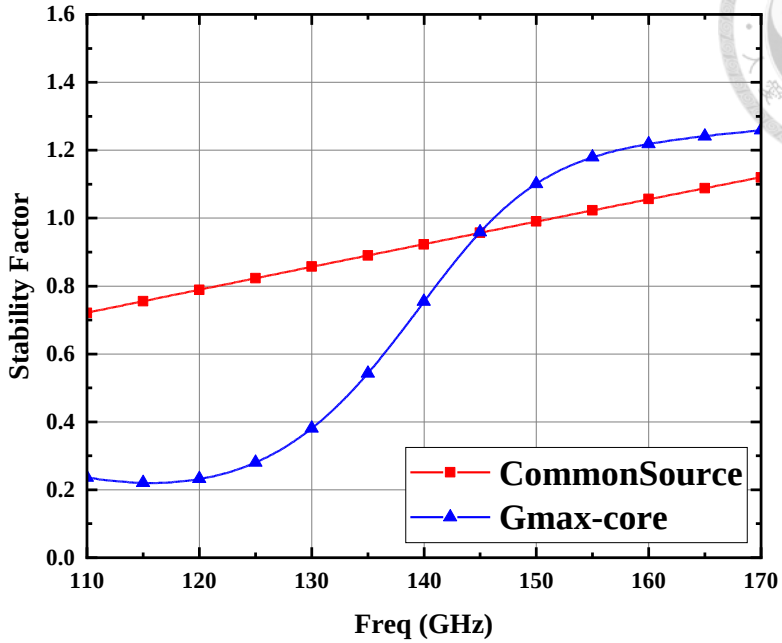

Fig. 2.19 Comparison of Gmax-core and the CS of simulated and stability factor.

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2.3 Complete Circuit Architecture

The proposed low noise amplifier is implemented using a 65-nm complementary metal-oxide-semiconductor (CMOS) process, which features an ultra-thick top metal layer, eight metal layers (M1 to M8), and metal-insulator-metal (MIM) capacitors. The matching networks are realized using microstrip lines and MIM capacitors. The complete circuit structure is thoroughly simulated using the EMX electromagnetic solver.

2.3.1 A single-stage amplifier

A single-stage Gmax core circuit, which serves as a test circuit, is illustrated in Fig. 2.20. The bias conditions are set as V_g = 0.7 V and V_d = 1.2 V. The transmission line characteristic impedances are chosen as $Z_1 = Z_2 = 50\ \Omega$ and $Z_3 = 74\ \Omega$, with transmission line lengths of L_1 = 94 μm, L_2 = 92 μm, and L_3 = 219 μm. Unlike the first stage of the main circuit, this test circuit is designed for maximum gain by employing conjugate matching instead of optimum noise matching. The simulated S-parameters are presented in Fig. 2.21. A maximum gain of 6 dB at 144 GHz is achieved under conjugate matching conditions, which is significantly higher than the simulated gain of a typical common-source amplifier shown in Fig. 2.22, which only achieves 3.8 dB. The simulated output power versus input power characteristics are shown in Fig. 2.23, and the input 1-dB compression point is −7 dBm. The layout of the single-stage Gmax core circuit is depicted in Fig. 2.24, occupying an area of 430 μm × 250 μm, including the RF pads. DC pads are not implemented in this circuit; instead, the DC bias is applied through the RF port using a bias-T.

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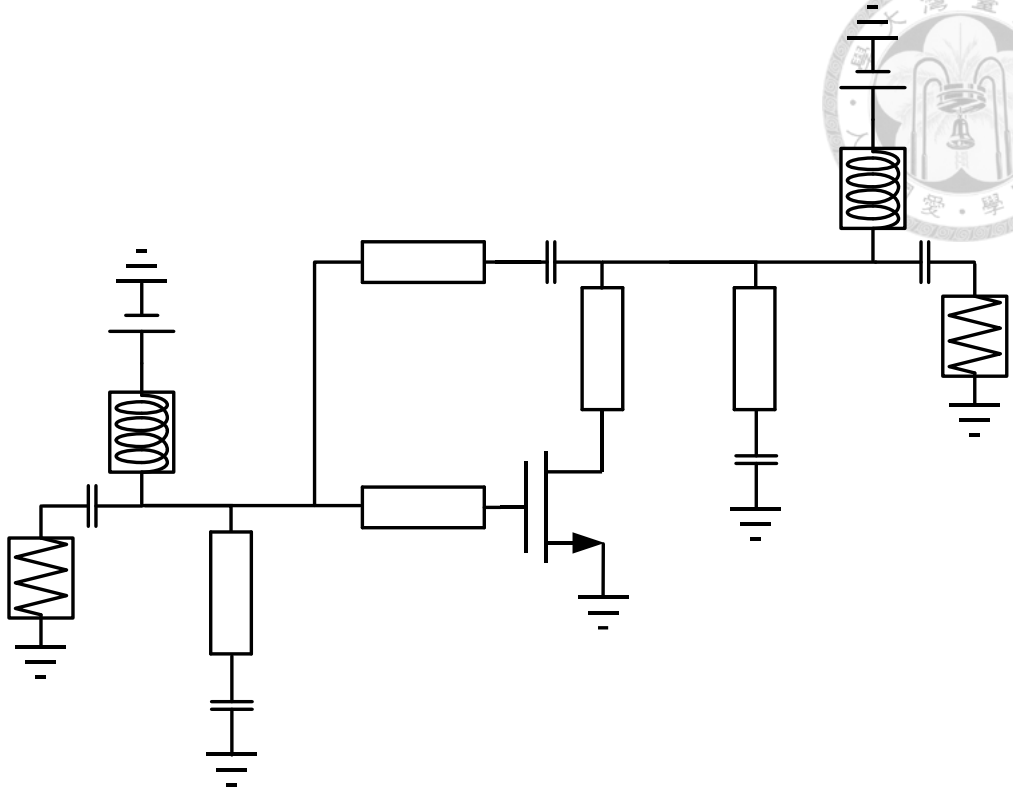

Fig. 2.20 A single-stage Gmax core circuit

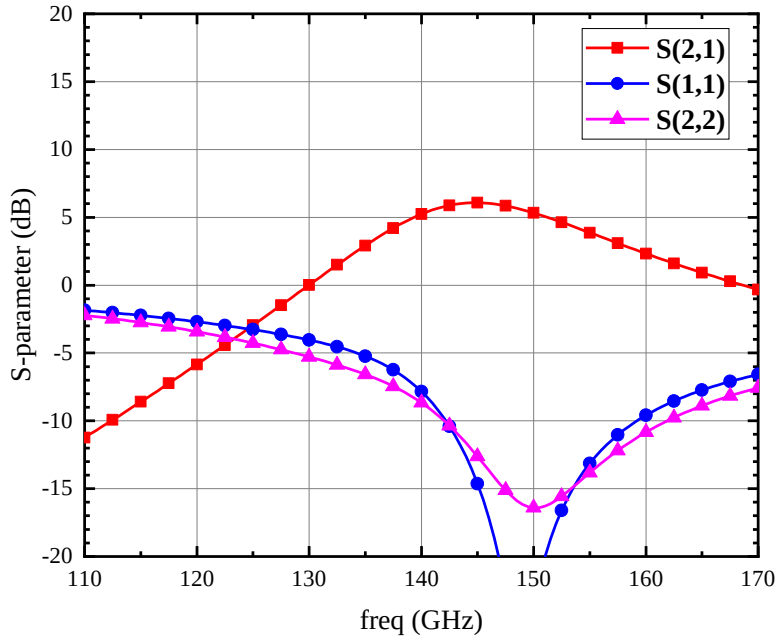

Fig. 2.21 The simulated S-parameters of a single-stage Gmax core amplifier

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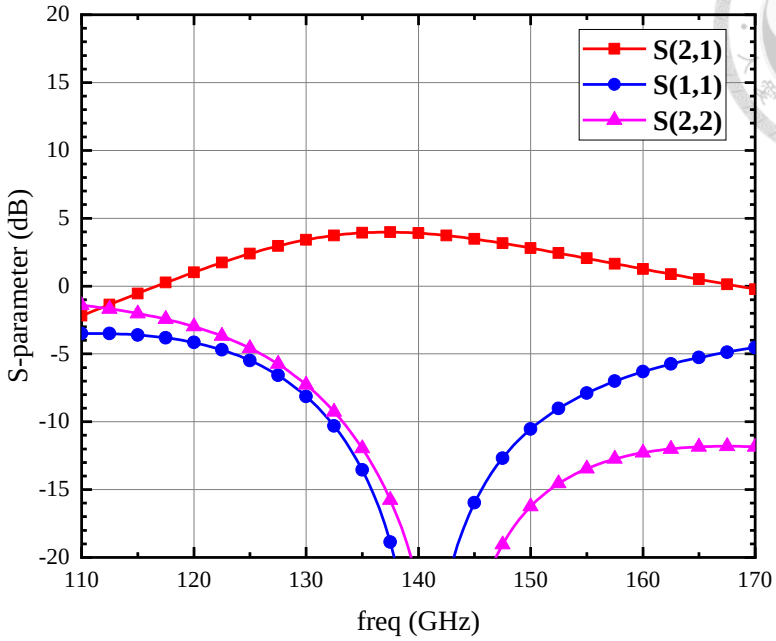

Fig. 2.22 The simulated S-parameters of a CS LNA

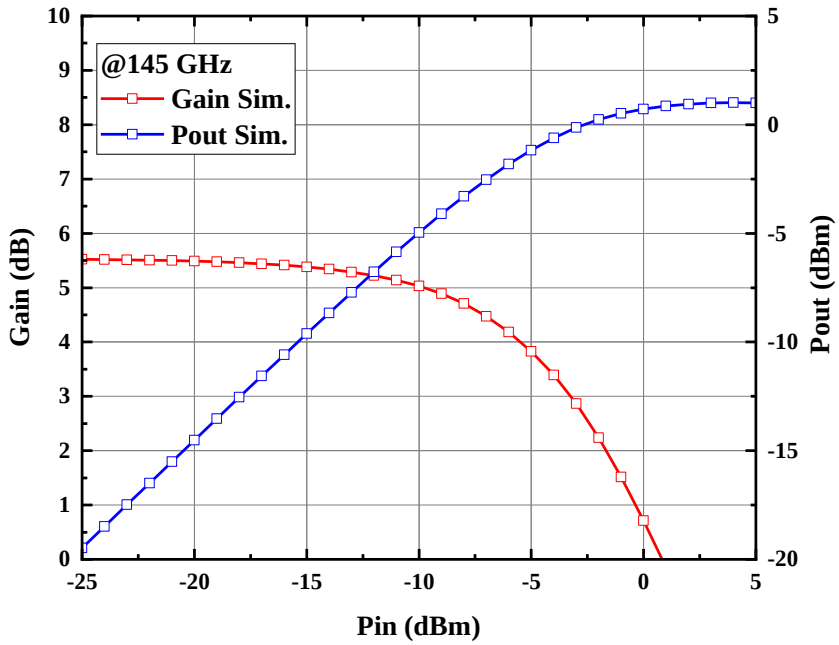

Fig. 2.23 Simulation of IP_{1dB} @ 145 GHz versus input power

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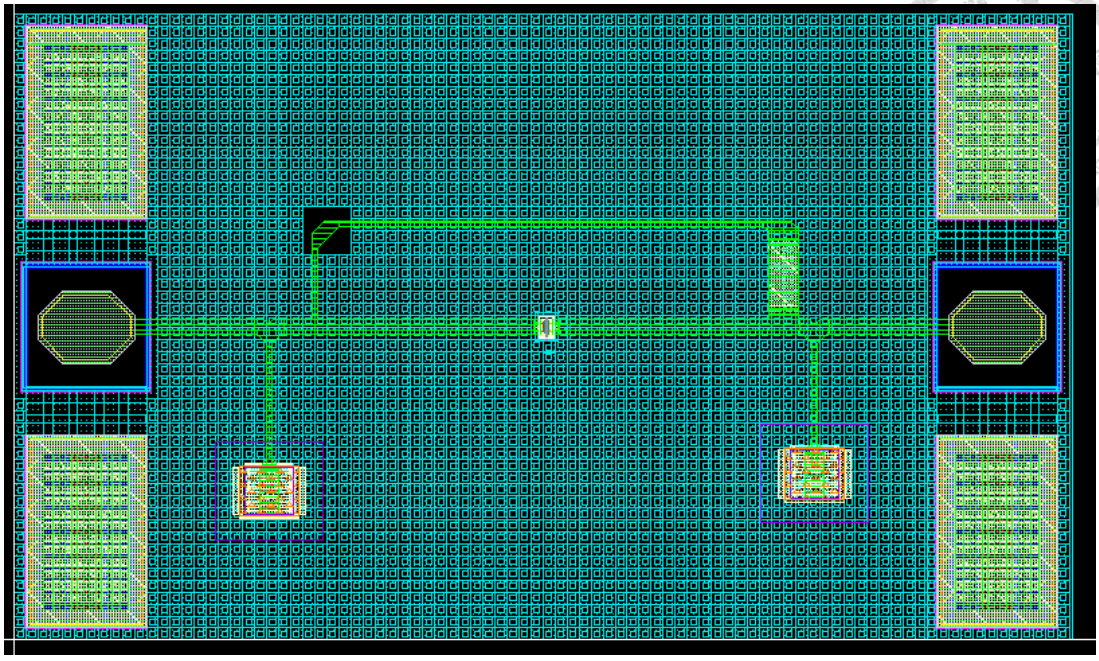

Fig. 2.24 Chip layout for the single-stage amplifier

2.3.2 A three-staged Gmax core LNA

The complete circuit schematic of the proposed D-band low noise amplifier is illustrated in Fig. 2.25. The amplifier consists of three cascaded Gmax core stages. The active device in each stage is designed with a gate width of 1 μm and 12 fingers. The bias conditions are set to a gate voltage of 0.7 V and a drain voltage of 1.2 V, with a drain current of 4.8 mA per stage. To optimize noise impedance close to the conjugate matching impedance, the lengths of the three transmission lines in the first stage are 85 μm, 204 μm, and 90 μm, respectively. Both conjugate and optimum noise matching are achieved at the target frequency by appropriately selecting the transmission line parameters.

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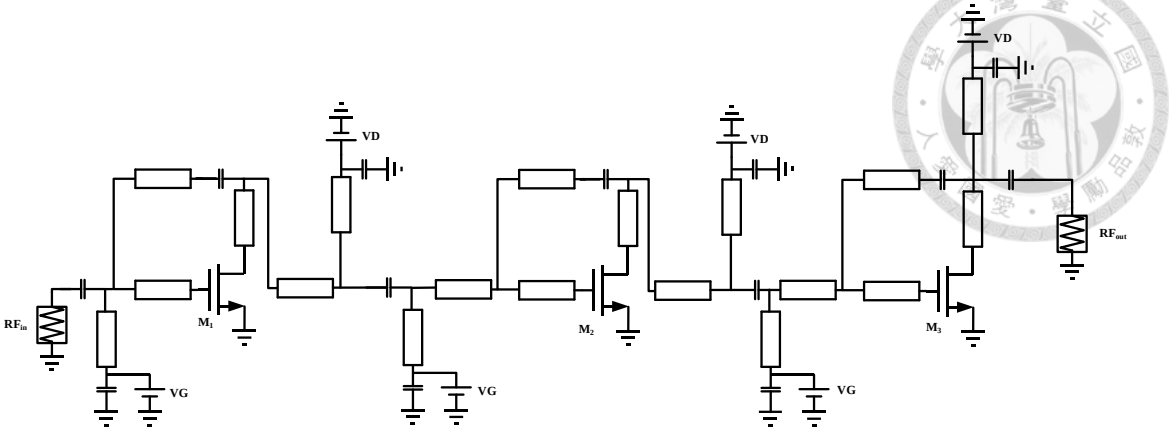

Fig. 2.25 The schematic of a three-staged Gmax core LNA.

The simulated S-parameters are shown in Fig. 2.26. The 3-dB bandwidth extends from 128 GHz to 145 GHz, and a peak gain of 15 dB is achieved at 139 GHz. As shown in Fig. 2.27, the minimum simulated noise figure is 7.9 dB. Fig. 2.28, Fig. 2.29, and Fig. 2.30 present the large-signal simulation results, where the input 1-dB compression point is greater than −17 dBm across the operating band. The final layout of the proposed LNA is depicted in Fig. 2.31, occupying an area of 760 × 625 μm^2.

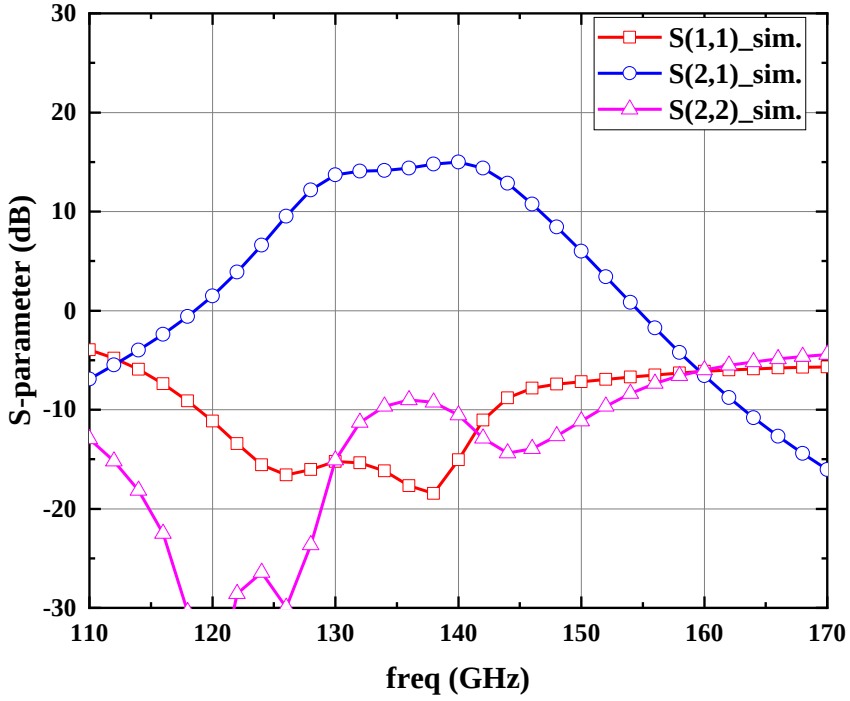

Fig. 2.26 6Simulated S-parameters.

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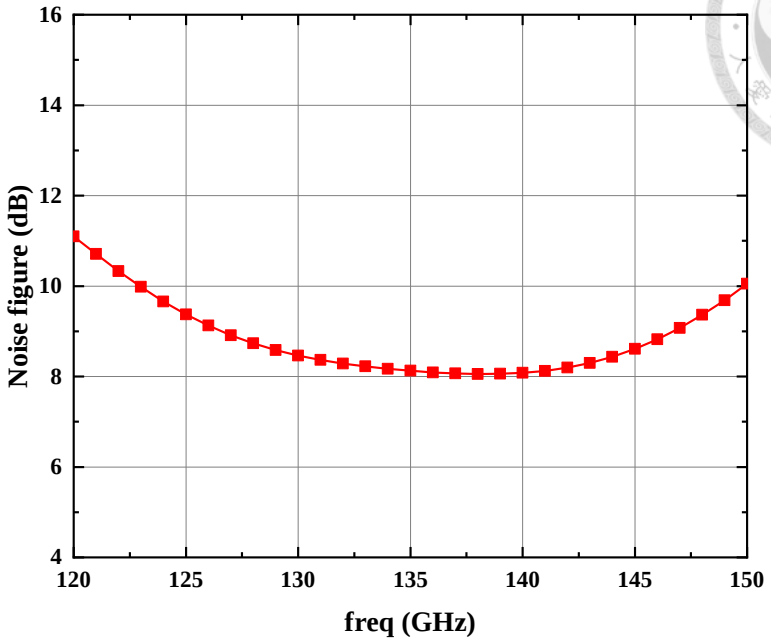

Fig. 2.27 Simulated noise figure.

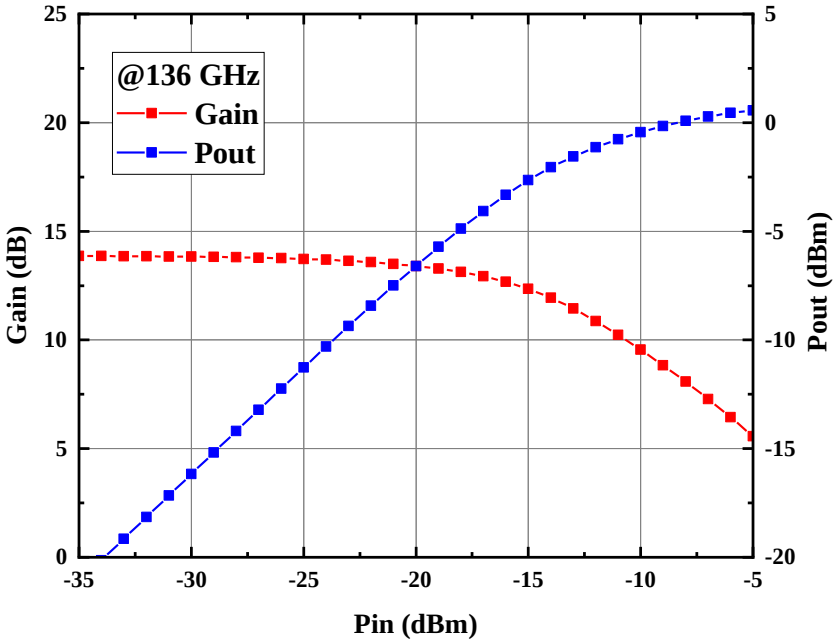

Fig. 2.28 Simulation of IP_{1dB} @ 136 GHz versus input power.

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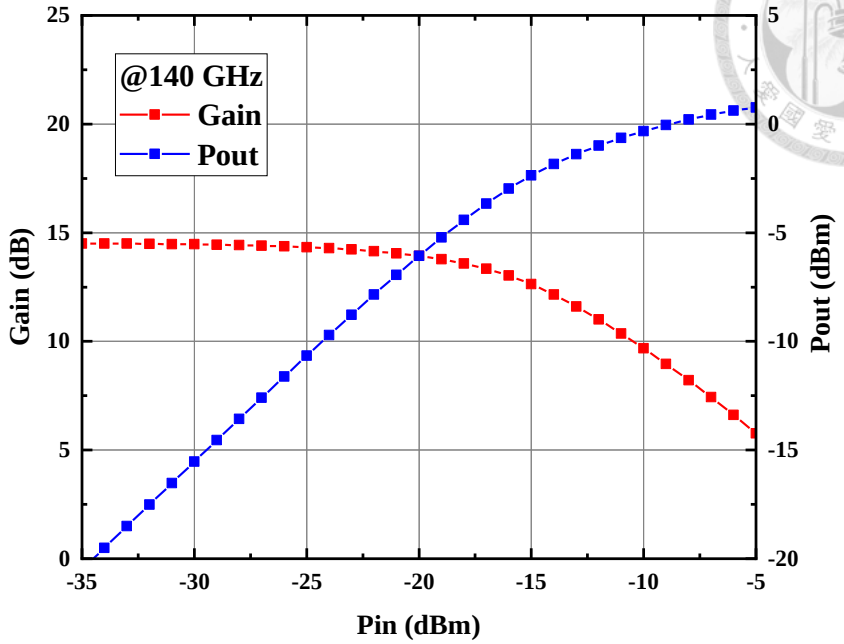

Fig. 2.29 Simulation of IP_{1dB} @ 140 GHz versus input power.

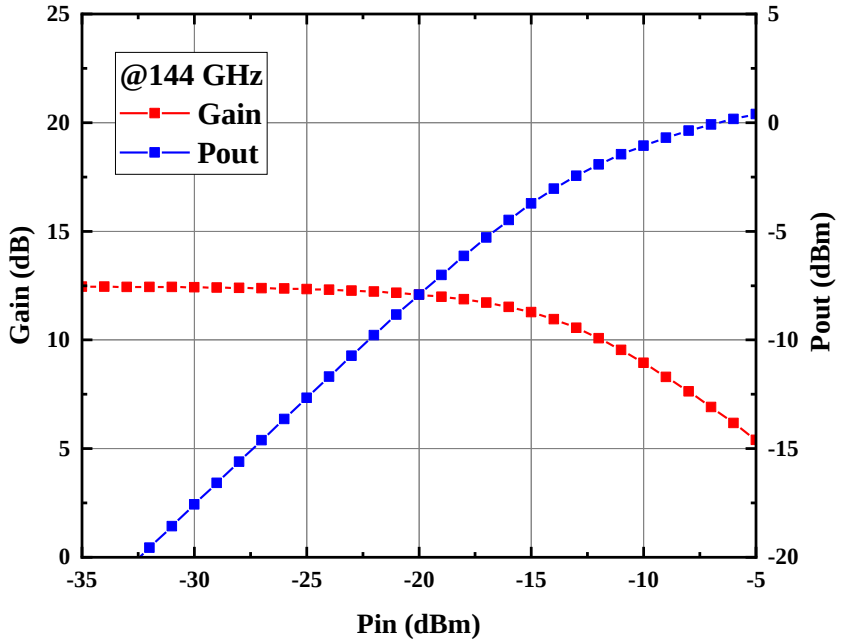

Fig. 2.30 Simulation of IP_{1dB} @ 144 GHz versus input power

doi:10.6342/NTU202504604

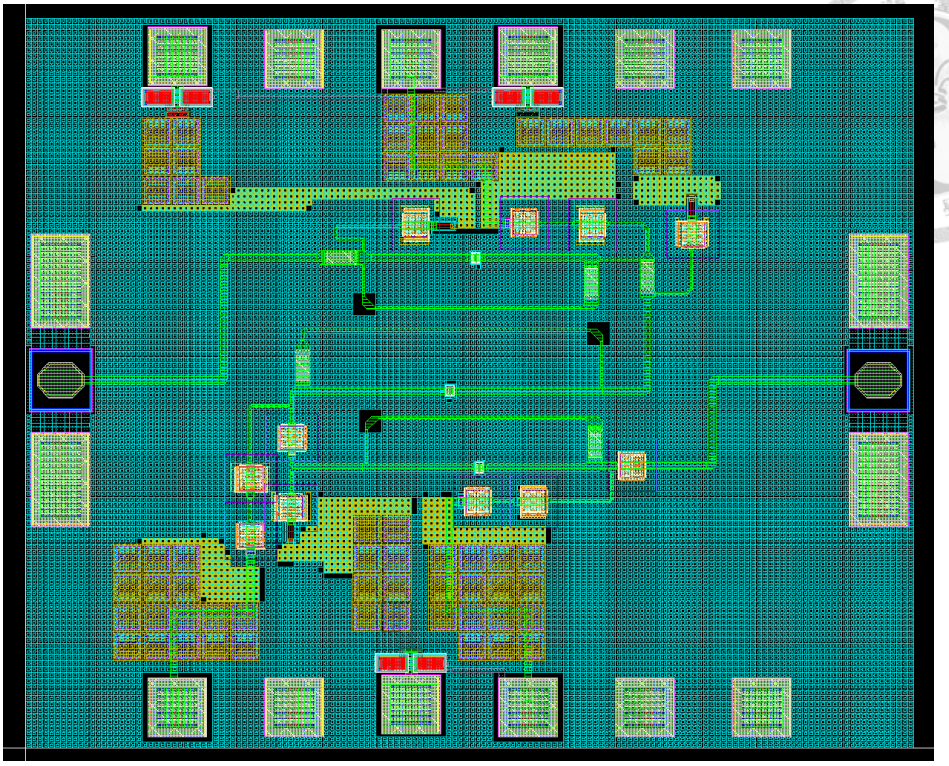

Fig. 2.31 Chip layout for the three-stage LNA

In multi-stage amplifier design, evaluating the stability of each stage individually using the stability factor (k-factor) or μ-factor is insufficient to guarantee global stability of the entire system. After the inter-stage matching network, the output impedance of the preceding stage may fall into the instability region of the subsequent stage, potentially leading to undesired oscillations. Therefore, it is essential to examine the inter-stage impedance to mitigate this risk. If there is an overlap between the stable and unstable regions of the adjacent stages, oscillation may occur under certain conditions. As a result, ensuring that the mapped impedance region from the preceding stage does not overlap with the instability region of the following stage is a critical step in achieving robust stability in high-frequency multi-stage amplifier design. The overall stability simulation results are shown in Fig. 2.32 and Fig. 2.33, where the stability factors are all greater than unity and the inter-stage stability mapping circles do not intersect, indicating that the risk of potential oscillation is effectively avoided.

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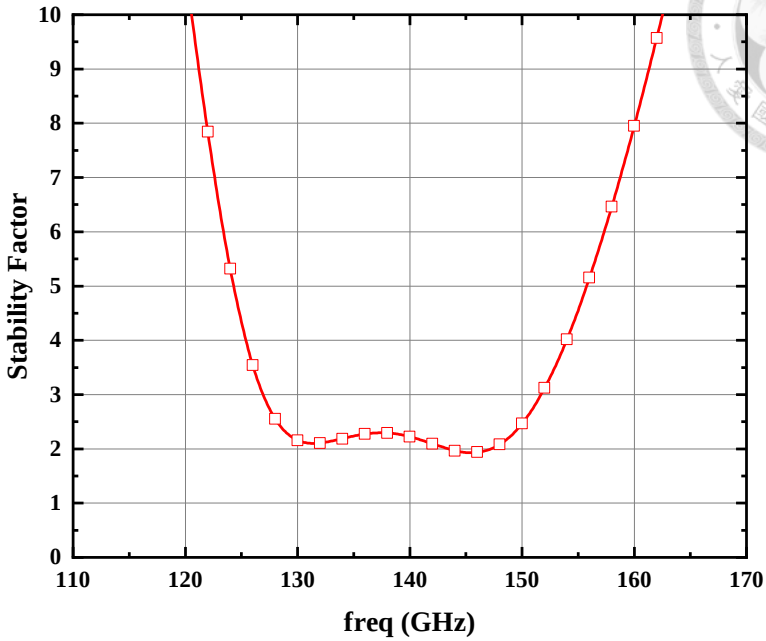

Fig. 2.32 Simulated stability factor of the proposed LNA.

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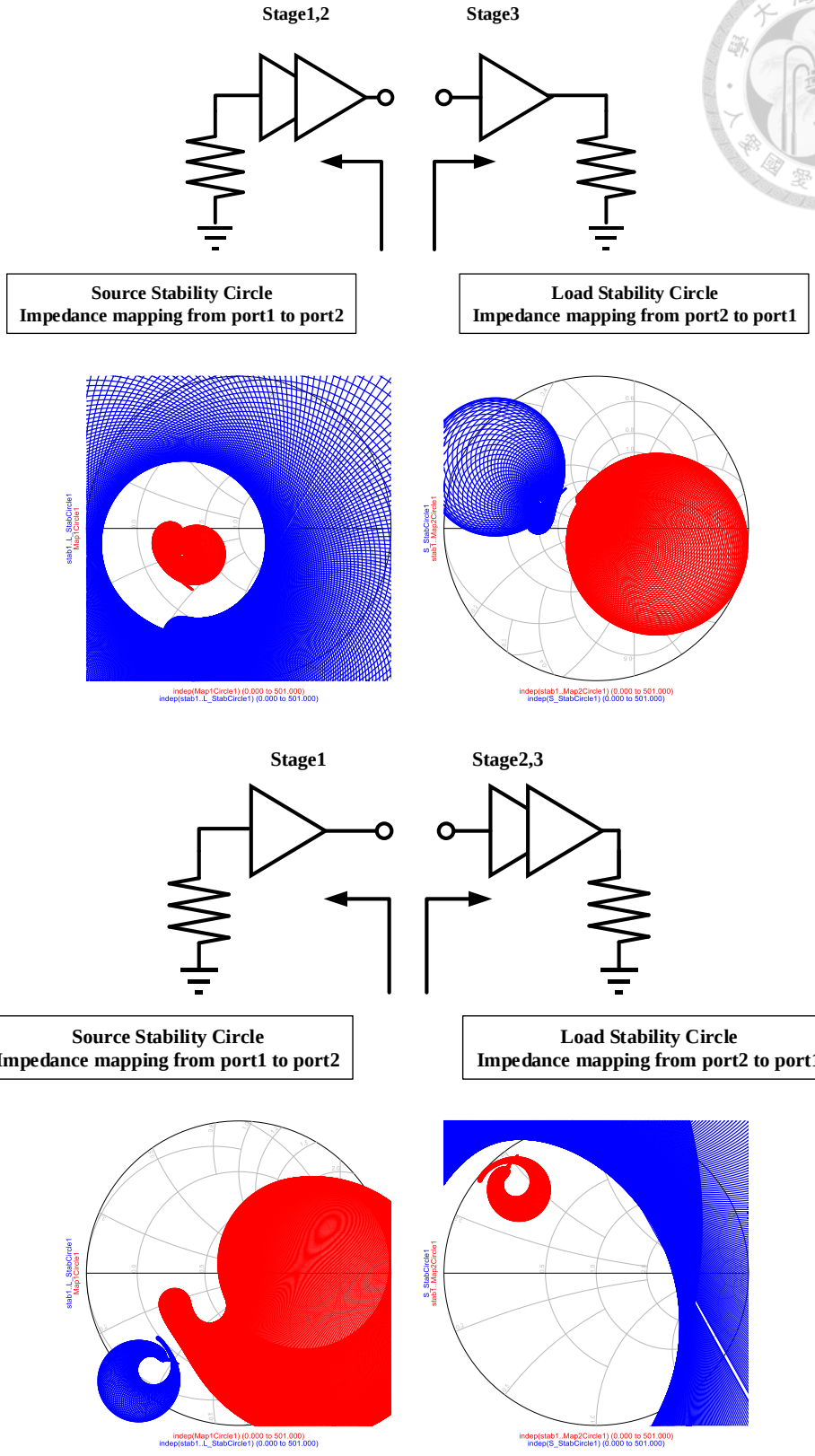

Fig. 2.33 Simulation of inter-stage stability

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2.4 Measurement Result

The proposed chip was fabricated using TSMC's 65-nm CMOS process. As shown in Fig. 2.34, a die micrograph of the fabricated chip is presented. The overall chip area, including both RF and DC pads, is 760 × 625 μm², while the active core occupies 0.12 μm². The circuit operates under a drain supply voltage of 1.2 V and a gate bias of 0.7 V, resulting in a total DC power consumption of 17.3 mW.

All measurements were performed using on-wafer probing, with no off-chip capacitors or resistors incorporated during the measurement. S-parameter characterization was carried out over the frequency range of 110–170 GHz using an Agilent E8361C vector network analyzer (VNA) equipped with OML V06VNA2-T/R D-band frequency extenders.

For noise figure measurement, the setup adopted WR6.5 waveguide and a VDI WR6.5NS noise source. An attenuator was inserted to prevent excessive power at the spectrum analyzer's mixer extension module. The noise measurement configuration is illustrated in Fig. 2.35, and the noise figure was extracted via the Y-factor method[37].

The measured and simulated S-parameters are shown in Fig. 2.36, where measured transistor data were adopted in the simulation. The measured peak small-signal gain achieves 22 dB at 140 GHz, with noise figure results depicted in Fig. 2.37. The minimum measured noise figure is 8.2 dB at 132 GHz. The single-stage amplifier achieves 11.4 dB at 144 GHz with a 3-dB bandwidth.138.8~149.6 GHz, as shown in Fig. 2.40.Though the return loss degrades at 143 GHz, no oscillation was observed.

Large-signal measurement results are summarized in Fig. 2.38. Due to instrument limitations, the frequency range for large-signal characterization starts from 140 GHz. The measured IP_{1dB} is -27 dBm at 140 GHz and -18 dBm at 144 GHz, respectively.

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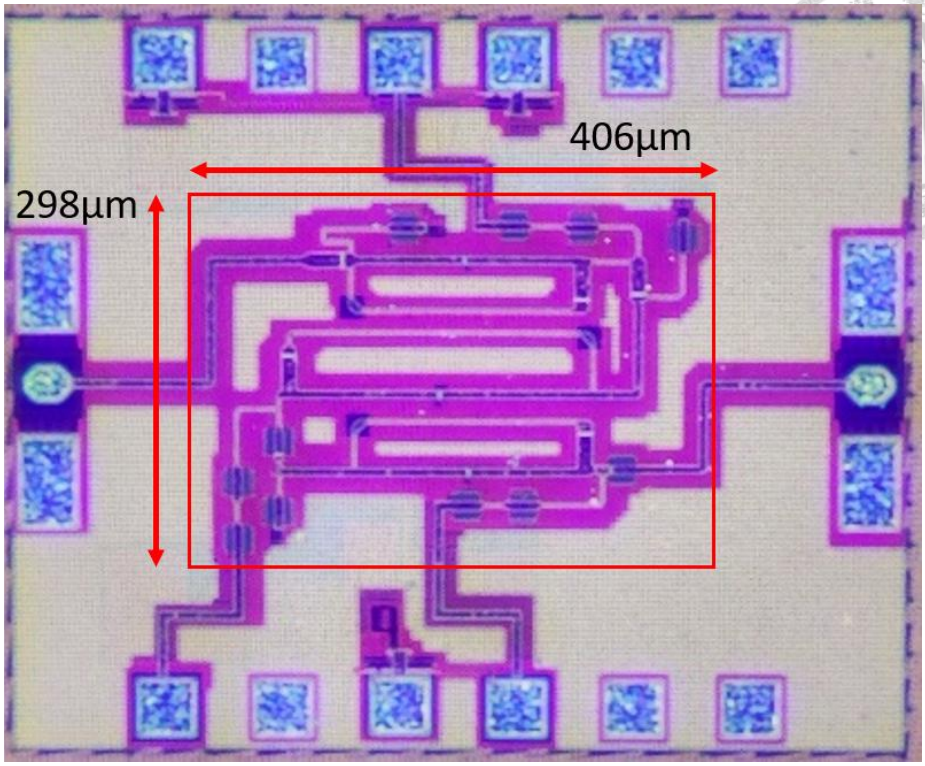

Fig. 2.34 Chip photo. The total size is 0.76×0.625 mm^2, and the core area is 0.12 mm^2.

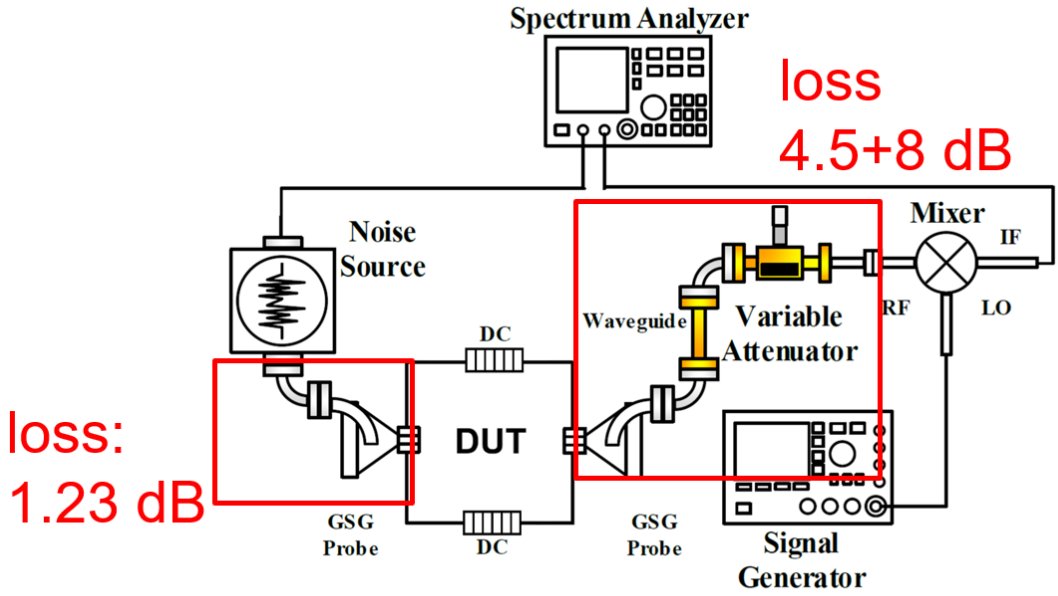

Fig. 2.35 Noise figure measurement setup.

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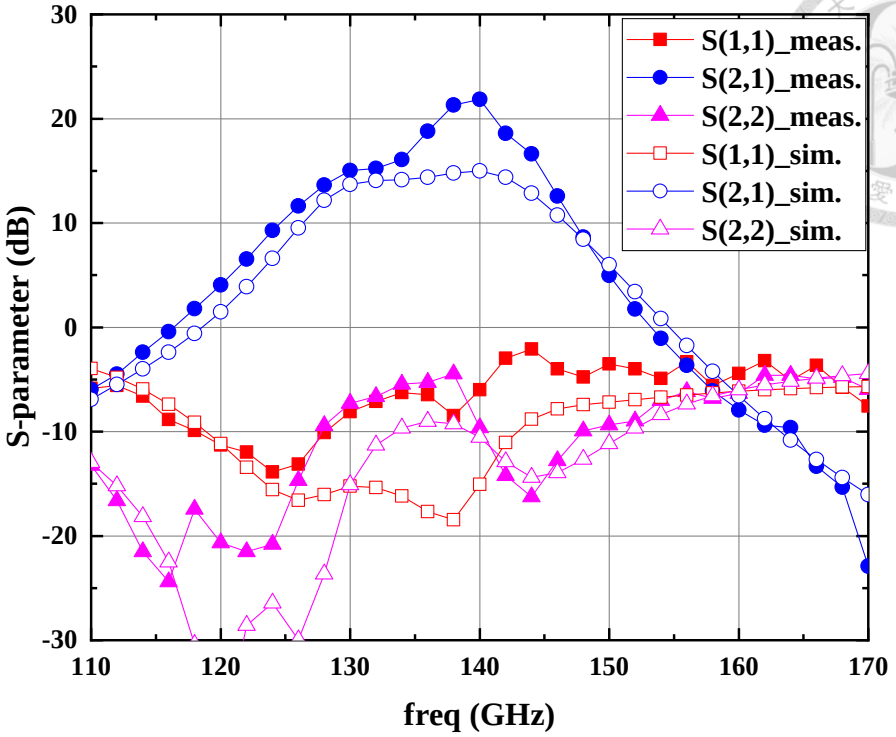

Fig. 2.36 Measured and simulated s-parameters.

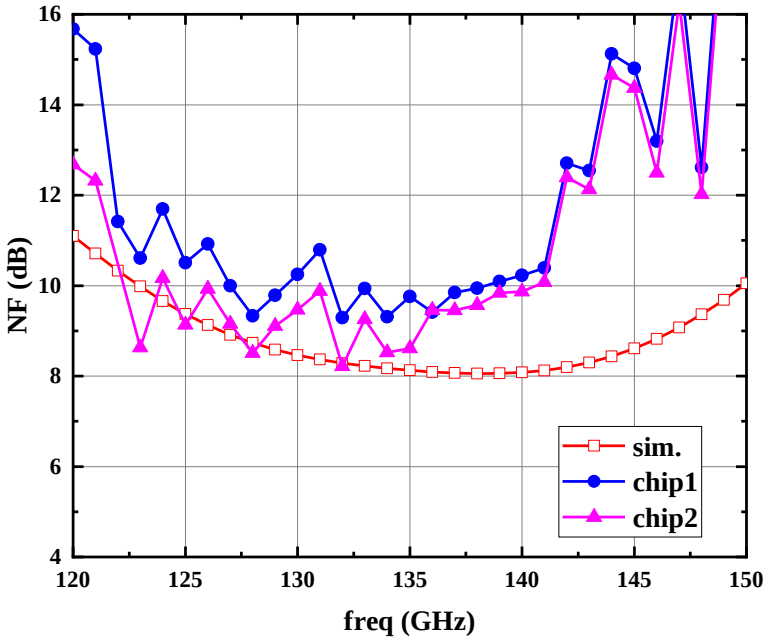

Fig. 2.37 Measured and simulated noise figure

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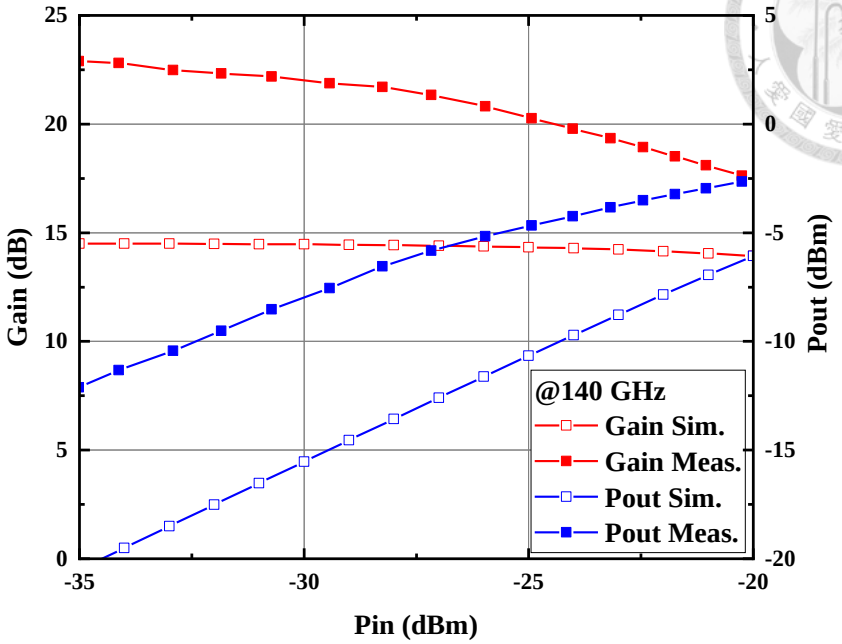

Fig. 2.38 Measured and simulated IP_{1dB} @ 140 GHz versus input power.

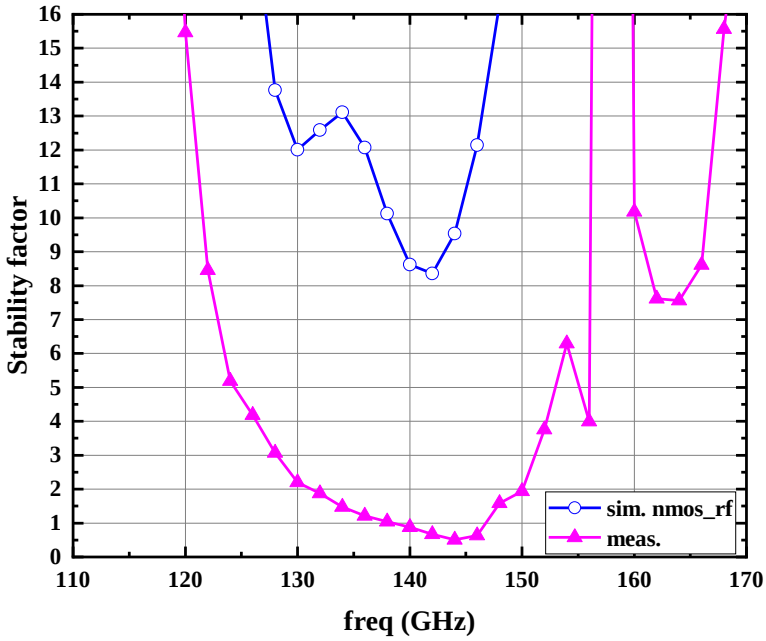

Fig. 2.39 Measured and simulated stability factor.

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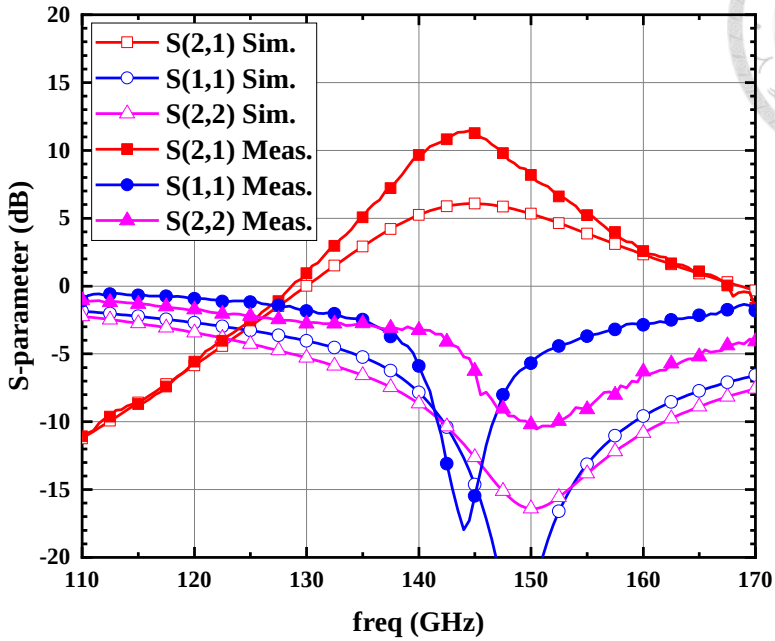

Fig. 2.40 Measured and simulated s-parameters of single-stage amplifier.

2.5 Discussions

Compared with the initial simulation results, the measured frequency response gain of the proposed D-band CMOS amplifier is significantly higher than expected. Although the RF transistor model provided by TSMC is only guaranteed to be accurate below 30 GHz, previous experience has shown that it can still be used at higher frequencies such as the W-band. However, as the operating frequency approaches the D-band, the discrepancy between measurement and simulation increases due to the limited accuracy of the transistor model at higher frequencies. Such inconsistencies between simulation and measurement results caused by inaccurate transistor models have been reported in previous studies [37]. In light of the critical importance of model accuracy, test transistors with identical dimensions as those used in the main circuit were fabricated concurrently during tape-out. Subsequently, the transistor model extracted from actual measurements

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was utilized to replace the foundry-provided PDK model in circuit simulations, thereby improving the consistency between simulated and measured results.

2.5.1 TRL Calibration

A custom Thru-Reflect-Line (TRL) calibration was implemented for transistor measurements in this study. Compared to the Short-Open-Load-Thru (SOLT) calibration, TRL calibration is more suitable for high-frequency measurements. The primary advantage of TRL lies in the fact that it does not require precisely defined short, open, or matched loads; instead, accurate transmission line characteristics are utilized for calibration. As a result, TRL can effectively reduce errors caused by imprecise standards at high frequencies and is commonly realized using coplanar waveguide (CPW) or microstrip lines. The TRL calibration comprises three standards: Thru, Reflect, and Line. The Thru standard is used to define the calibration reference plane, while the Reflect standard can be either an open or a short. The Line standard provides sufficient phase shift to achieve reliable data accuracy. The accuracy of TRL calibration is highly dependent on the design of the Line standard. The Line should be designed such that its electrical length is approximately 90 degrees at the center frequency of interest, with the applicable calibration range extending from approximately 20° to 160°. The overall structure of the TRL calibration is illustrated in Fig. 2.41 to Fig. 2.44. In this work, the Line standard was designed to be 282 μm in length. As shown in Fig. 2.45, simulation results indicate that the 282-μm transmission line corresponds to 90 degrees at 140 GHz, enabling a calibration range from approximately 30 GHz to 250 GHz. The proposed TRL calibration structure has been successfully employed for high-frequency S-parameter measurements of transistors in this study.

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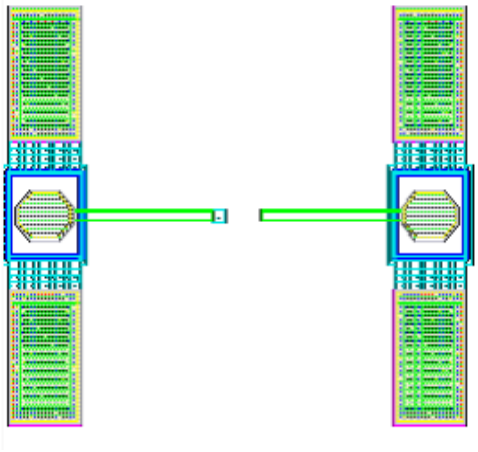
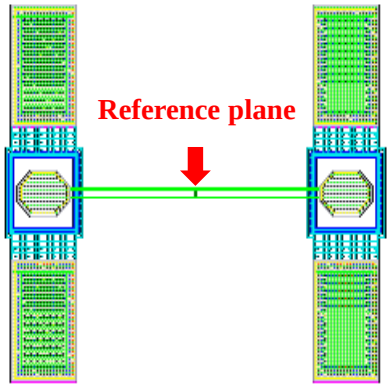
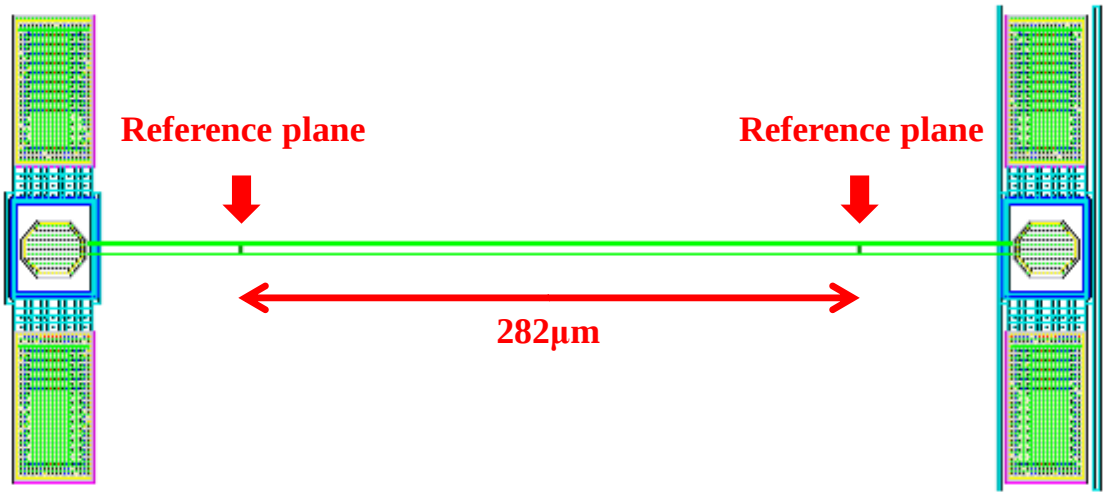


(a) Reflect(short,open)



(b) Through



(c) Line

Fig. 2.41 layout of TRL Calibration

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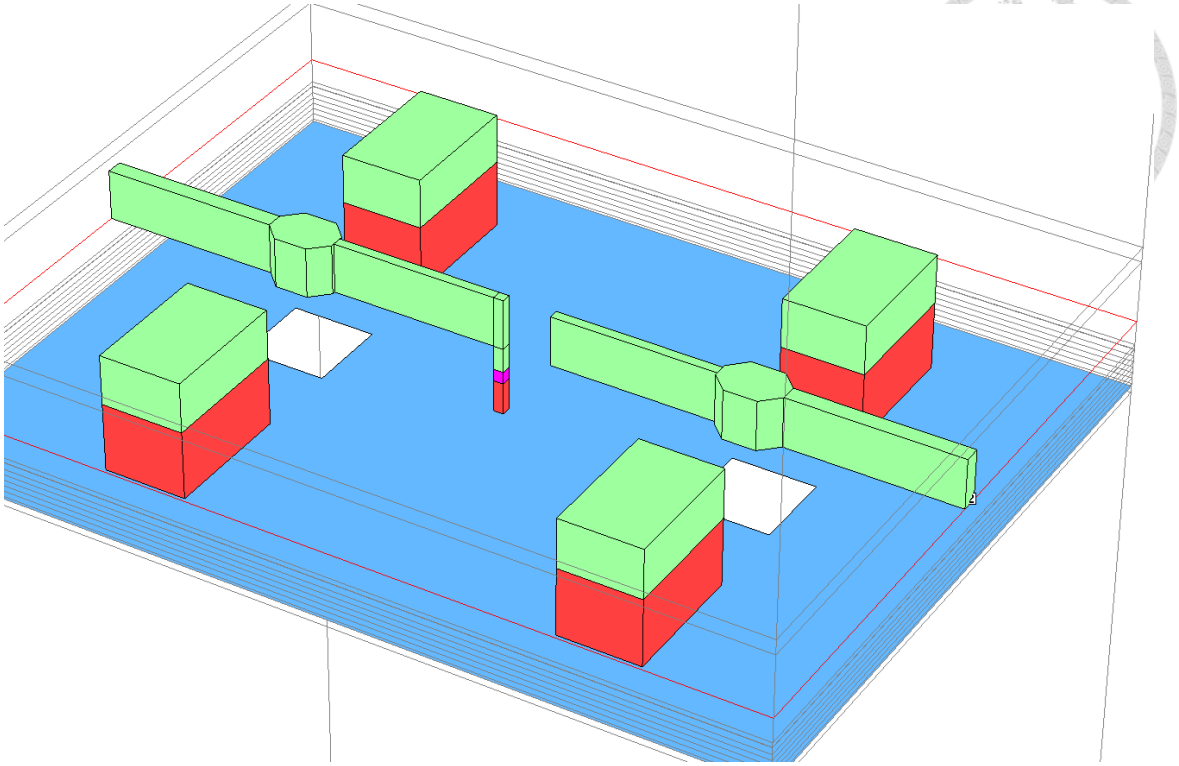

Fig. 2.42 Reflect(short,open)

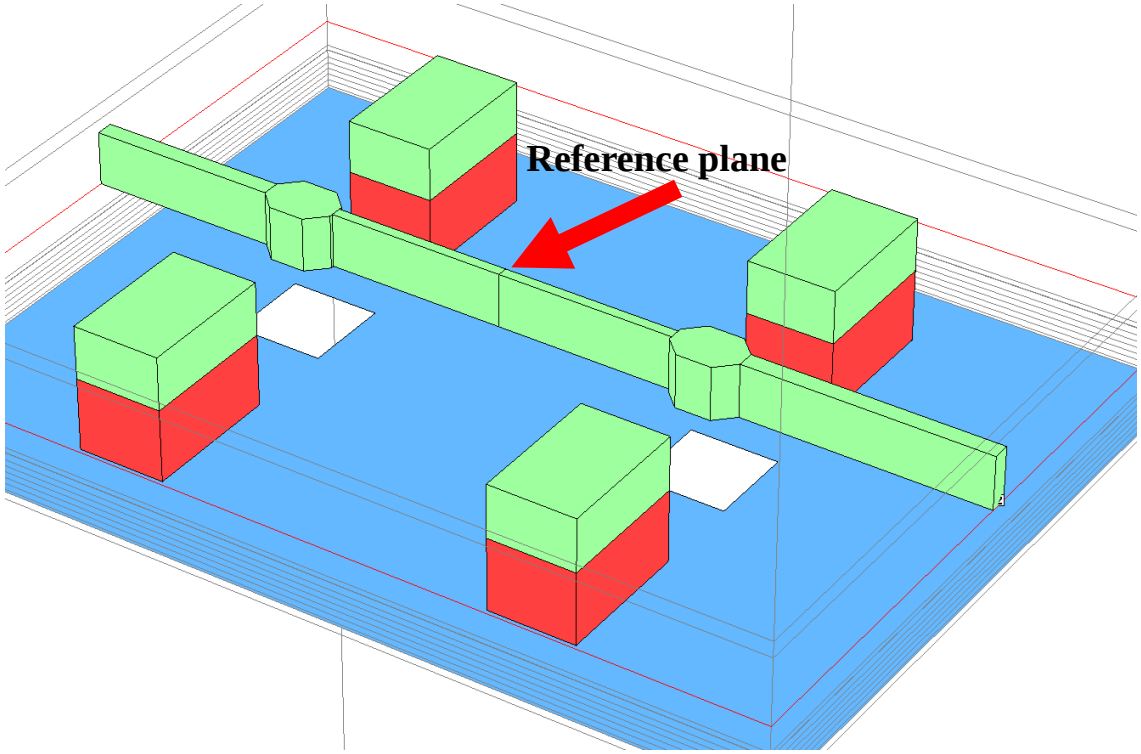

Fig. 2.43 Through

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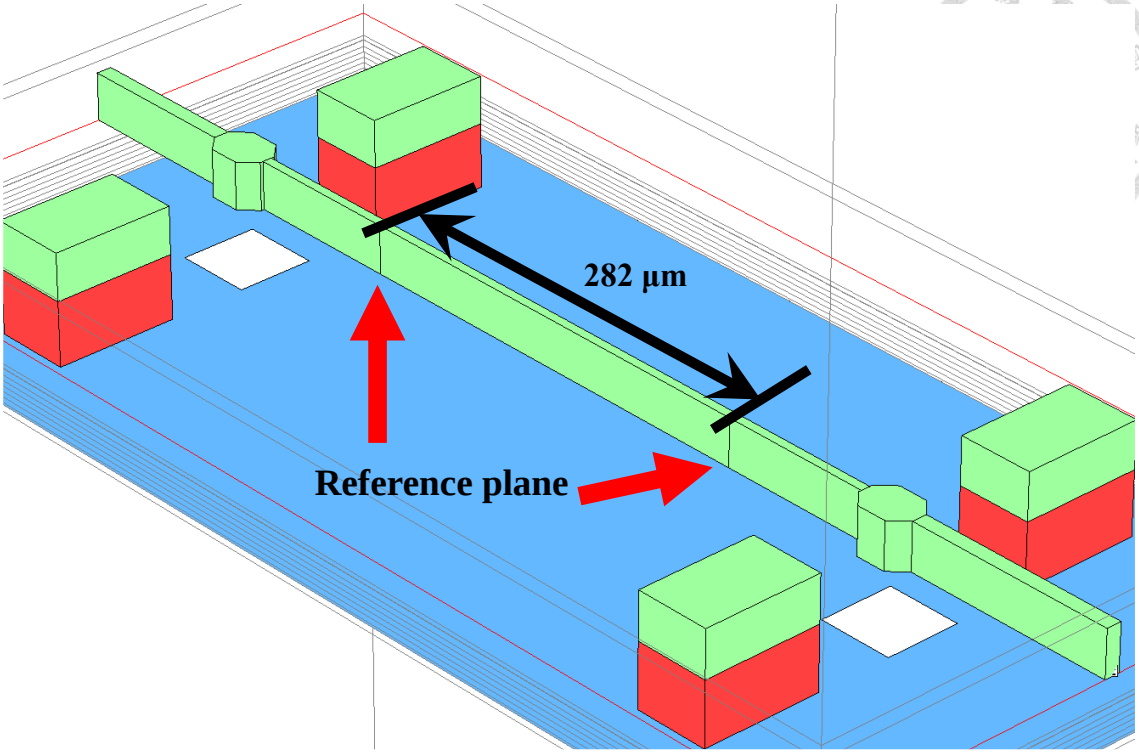

Fig. 2.44 Line

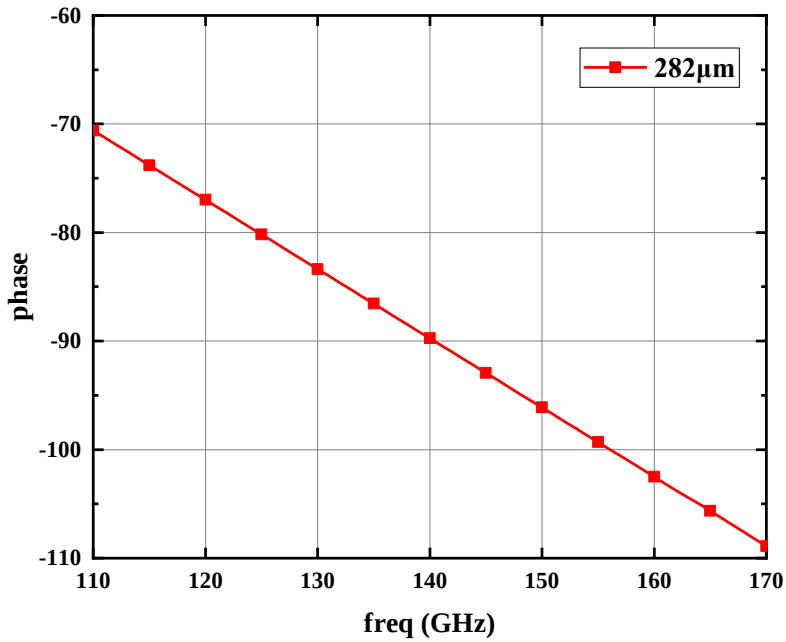

Fig. 2.45 Simulated phase of 282-µm transmission line

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2.5.2 Device measurement and modeling

After obtaining the S-parameter measurement results of the transistor, these data were incorporated into the circuit simulation. As shown in Fig. 2.46, Fig. 2.47, and Fig. 2.48, the simulated S-parameters of the circuit exhibit good agreement with the measured results. This outcome confirms that the previous discrepancies between simulation and measurement were primarily caused by inaccuracies in the original transistor model.

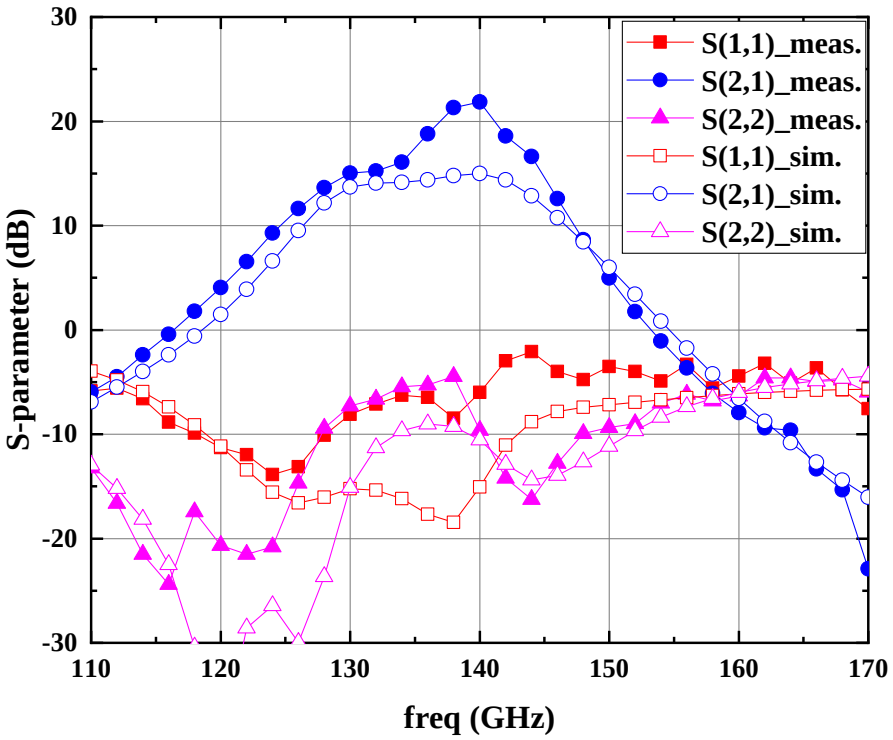

Fig. 2.46 Simulated and measured S-parameters of the proposed D-band LNA.

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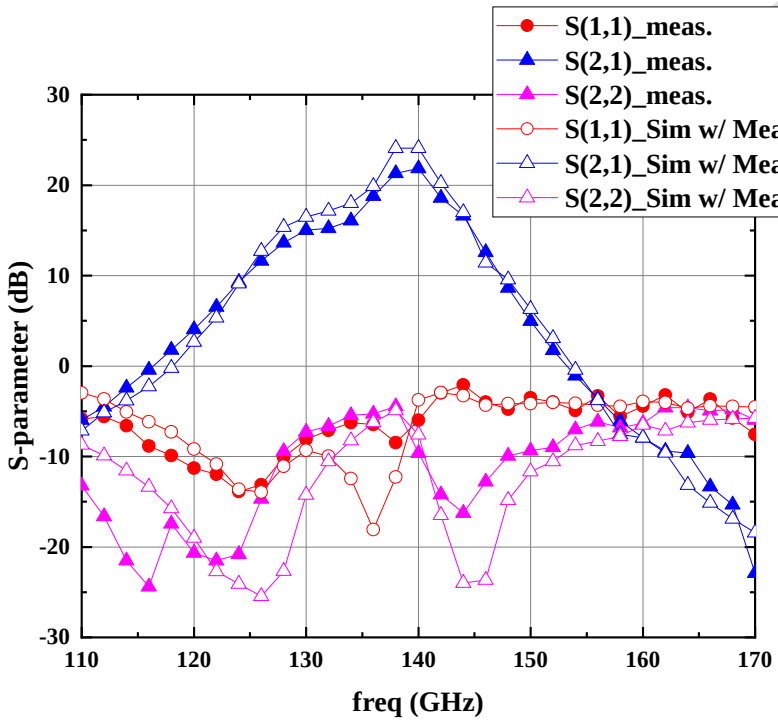

Fig. 2.47 S-parameters of the proposed D-band LNA of measurement and simulation with the measured device.

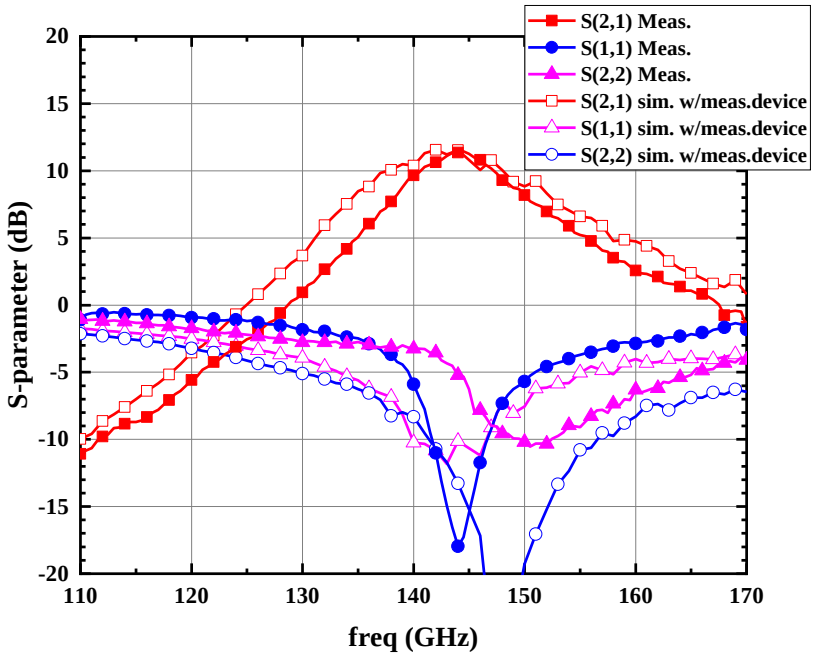

Fig. 2.48 S-parameters of the single-stage amplifier of measurement and simulation with the measured device.

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Previous studies have indicated that the extraction of parasitic parameters in transistors is particularly critical at high frequencies, and it is sometimes necessary to re-simulate the RF models accordingly. Prior work [37, 38]investigated the differences between the RF model and the NCH model. High-frequency structure simulator (HFSS) was employed to perform electromagnetic simulations, which revealed significant discrepancies in the S-parameters between the RF and NCH models and the EM simulation results. To address these issues, additional parasitic elements, such as gate resistance (R_g), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), and drain-to-source capacitance (C_{ds}), were incorporated into the simulation, as illustrated in Fig. 2.49, in order to account for the extra parasitic effects, present in the transistor.

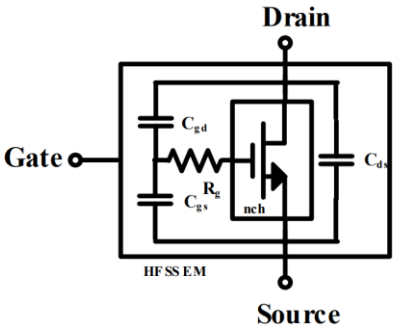

Fig. 2.49 The schematic diagram of previous transistor modeling. [37]

In this work, the transistor was re-simulated as shown in Fig. 2.50, where the NCH model was adopted as the core and the surrounding parasitic effects were carefully modeled. In the TSMC model shown in Fig. 2.50, the parasitics were characterized by lump elements by their measurement data from 0.1 MHz to 30.1GHz. In this work, the electromagnetic simulations were performed using EMX, which offers efficient computation. Compared to SONNET, EMX enables faster simulation under the same physical dimensions and edge mesh settings. Additionally, unlike HFSS, EMX does not require complicated port assignments and ground definitions. Therefore, EMX was selected as the simulation tool in this study.

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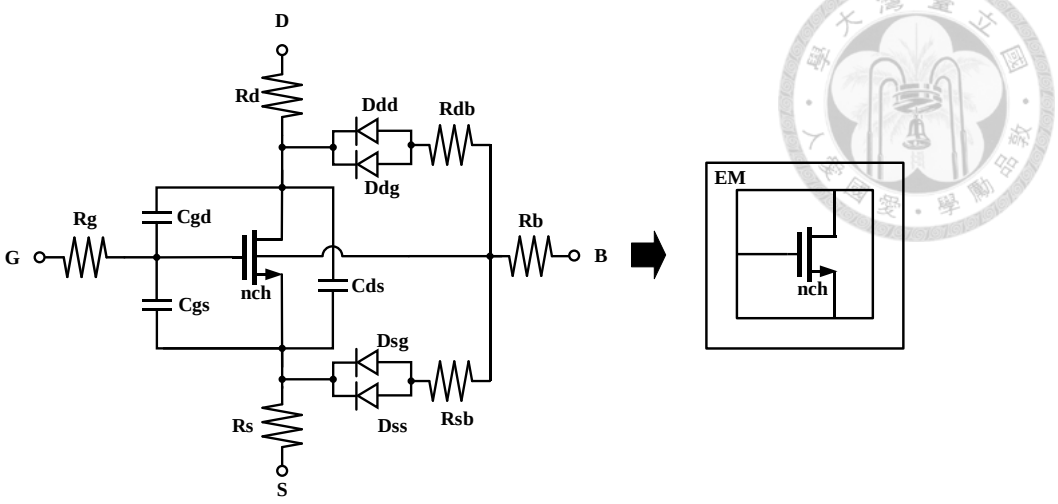

Fig. 2.50 The schematic diagram of the TSMC RF model and nch+EM model.

The EM simulation layout is shown in Fig. 2.51. The external drain and gate ports are excited through the edge of metal2 (M2) and metal3 (M3), respectively. The external source is connected to the bulk and ground directly, while the ground is defined by the surrounding M1 metal. On Fig. 2.52, for the intrinsic device, the internal source and drain are excited from M1, while the internal gate is excited from the middle PO layer to simulate the distributed resistance of the gate.

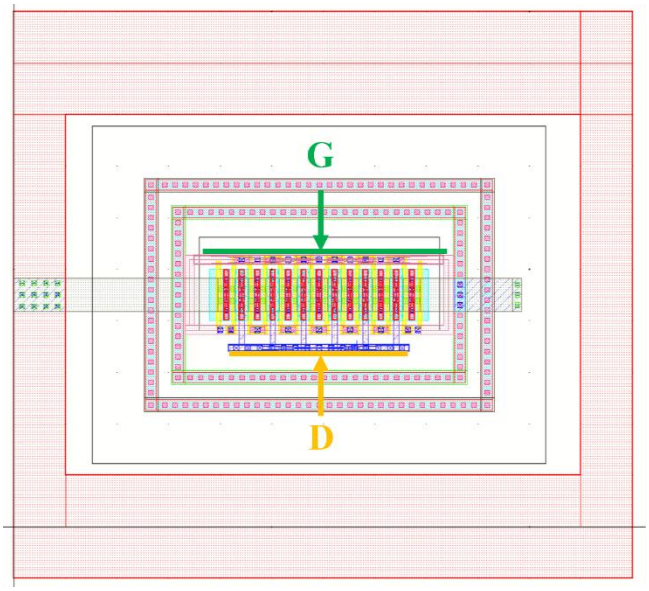

Fig. 2.51 The transistor layout of the proposed EM Model.

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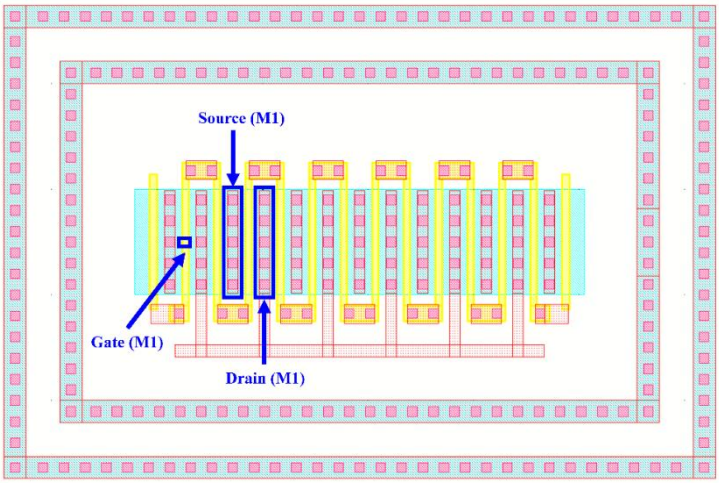

Fig. 2.52 The bottom view of nmos_rf

Fig. 2.53 to Fig. 2.59 present the measured and simulated S-parameters, phase, stability factor, and maximum gain of the transistor, including results obtained from measurement, the foundry model, and the NCH+EM approach. The measurement was conducted in two frequency ranges: 110 to 140 GHz at National Taiwan University (NTU) and 140 to 220 GHz at Taiwan Semiconductor Research Institute (TSRI). The measurement is performed as a two-port network measurement, where the gate and drain are defined as the input and output ports, respectively. The source and bulk terminals are connected to ground in a common-source configuration. The input power level is calibrated to -30 dBm. Although most S-parameters show similar trends, the NCH+EM model exhibits much closer agreement with the measured results, particularly in stability and maximum gain. The simulated minimum noise figure of NCH+EM is 0.5 dB less than the foundry model, as shown in Fig. 2.60. The slight deviation observed in S_{21} and S_{12} of the foundry model significantly affects the phase condition of the Gmax core, leading to discrepancies that further extend to the maximum gain and NF_{min}. In contrast, the NCH+EM model accurately reflects the gate-to-drain coupling capacitance (C_{gd}) and related parasitic effects, thereby improving the prediction of high-frequency behavior.

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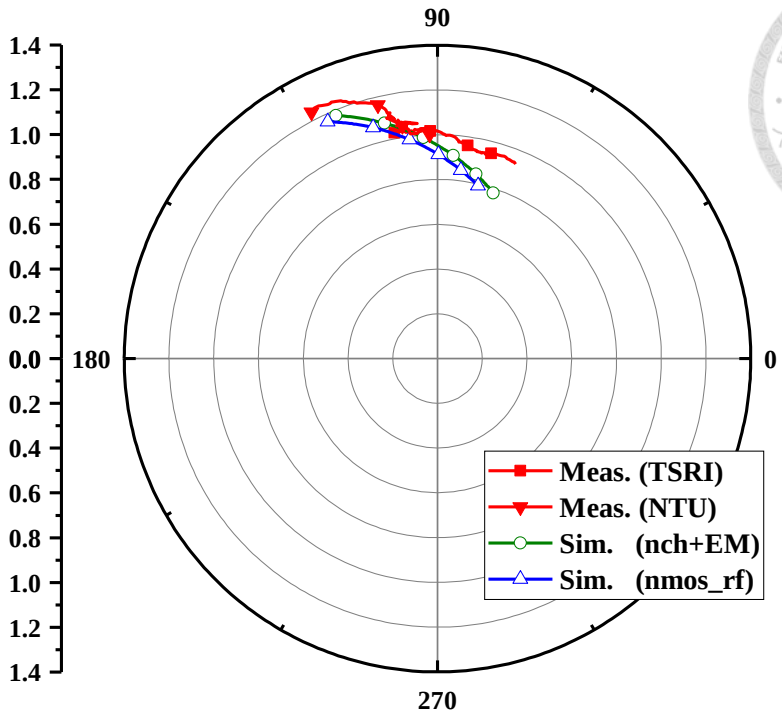

Fig. 2.53 The comparison of S_{21}. (110GHz to 220G)

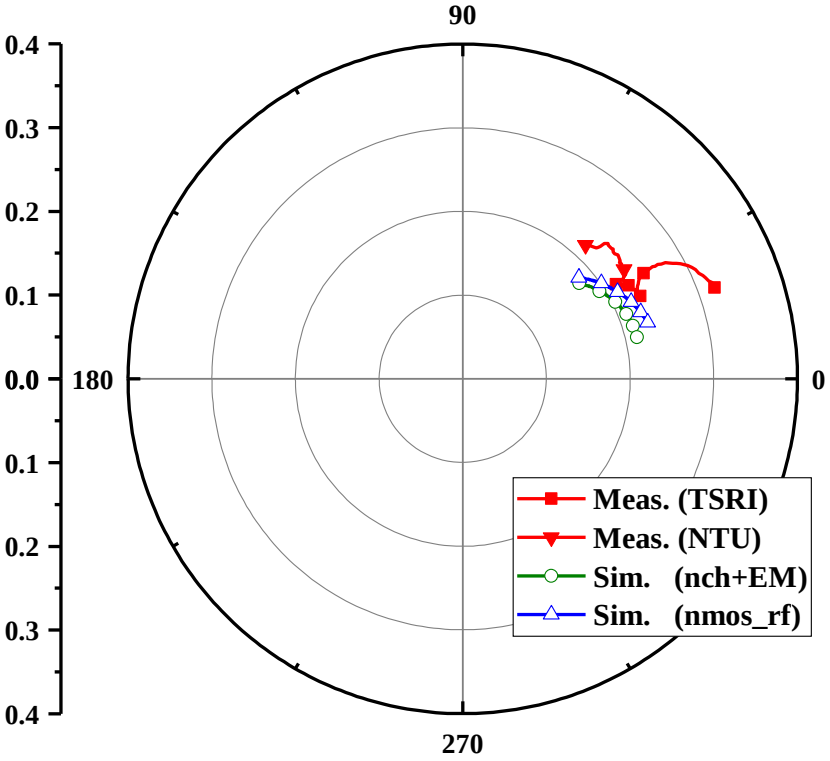

Fig. 2.54 The comparison of S_{12}. (110GHz to 220G)

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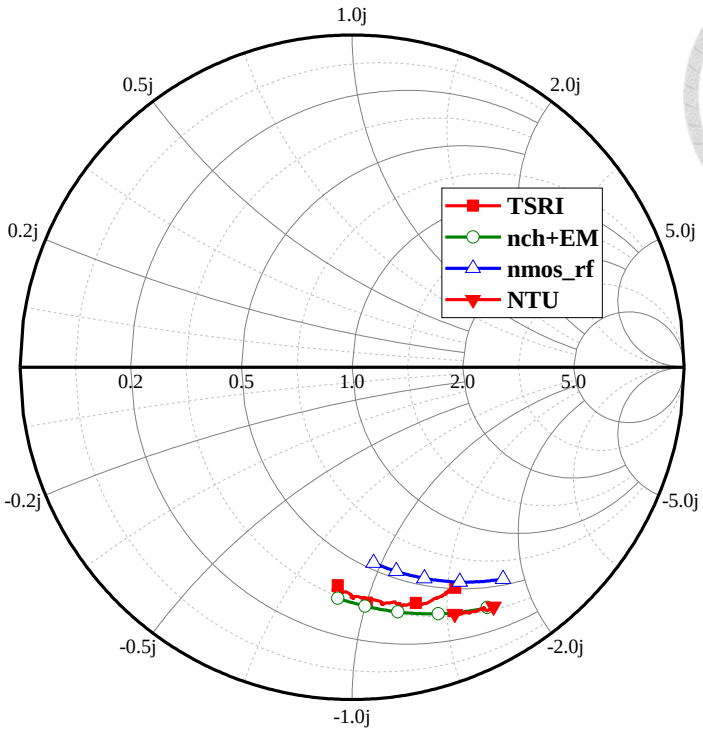

Fig. 2.55 The comparison of S_{11}. (110GHz to 220G)

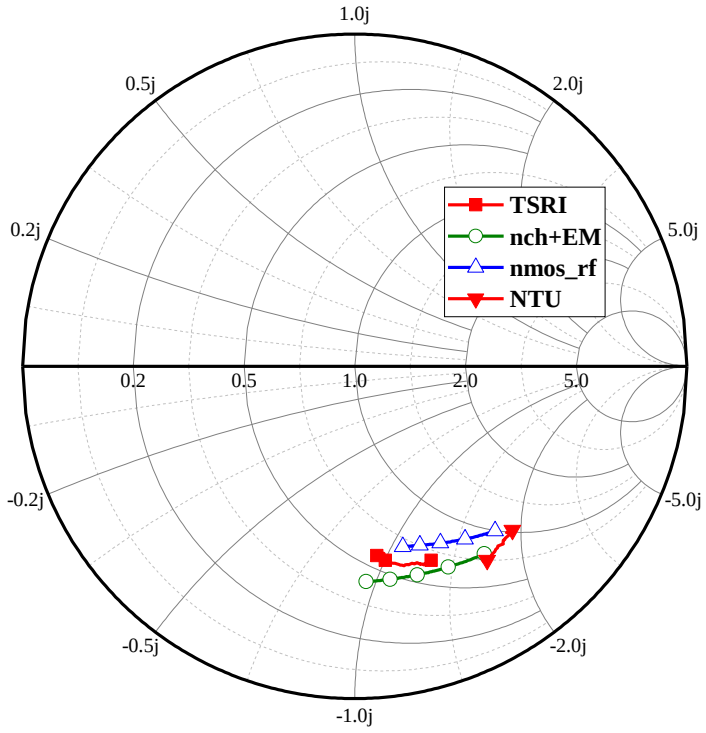

Fig. 2.56 The comparison of S_{22}. (110GHz to 220G)

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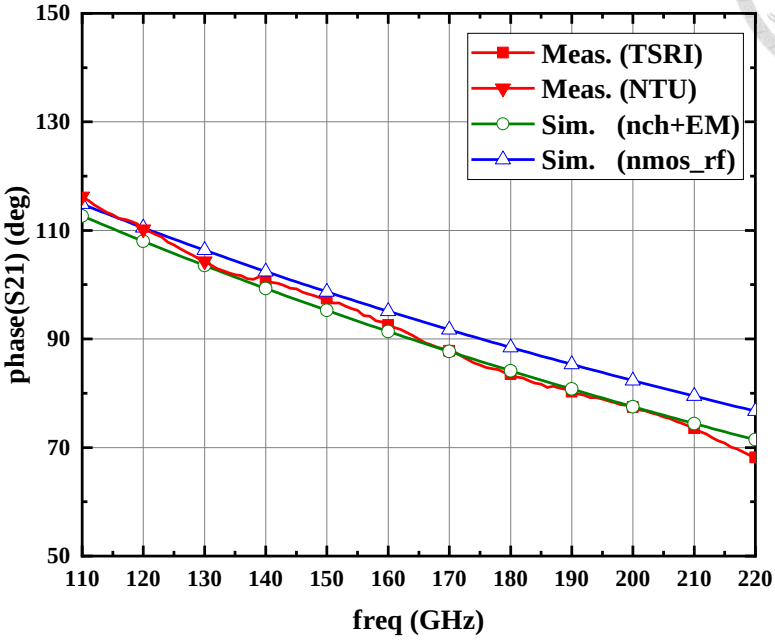

Fig. 2.57 The comparison of the S_{21} phase.

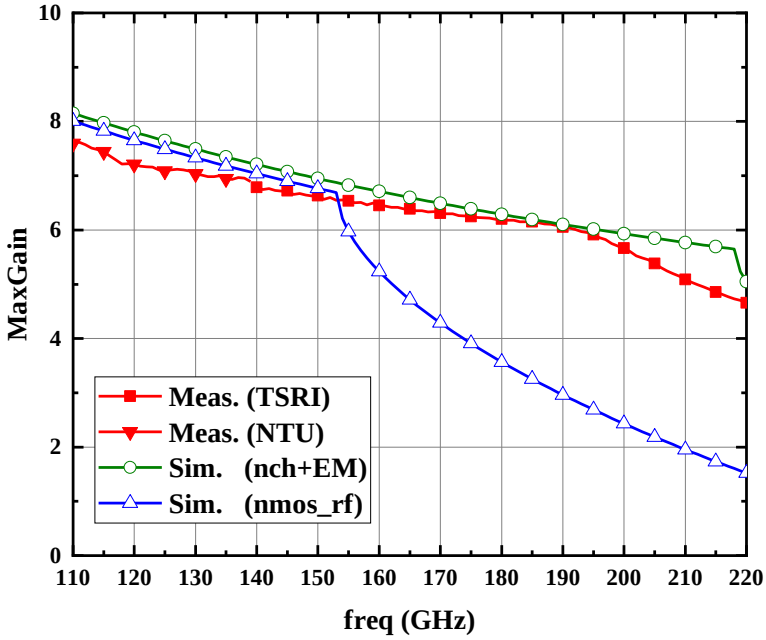

Fig. 2.58 The comparison of the maximum gain.

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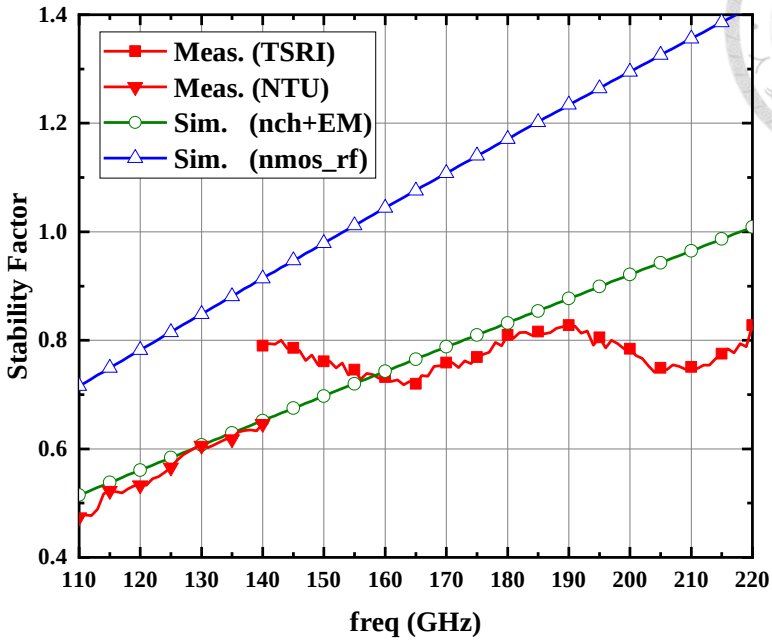

Fig. 2.59 The comparison of the stability factor.

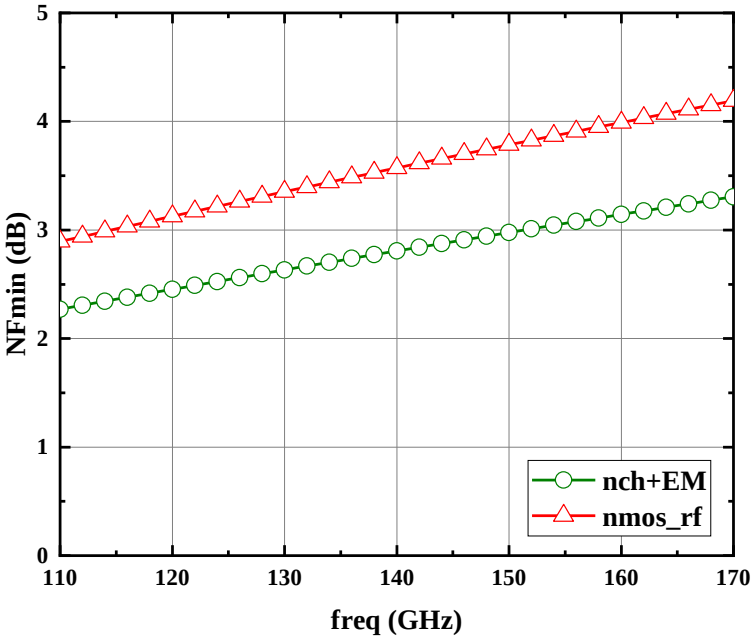

Fig. 2.60 The comparison of the NF_{min}.

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2.5.3 Comparison with measurement results

The improved transistor model was further applied to the overall circuit simulation. As shown in Fig. 2.61 to Fig. 2.66, the simulation results using the NCH+EM model exhibit excellent agreement with the measured results in both S-parameters, noise figure, stability factor, and large-signal behavior shown in Fig. 2.63 to Fig. 2.64. In summary, this chapter proposes a novel methodology for simulating the characteristics of high-frequency transistors. The proposed flow enhances the consistency between simulation and measurement results in high-frequency circuit design.

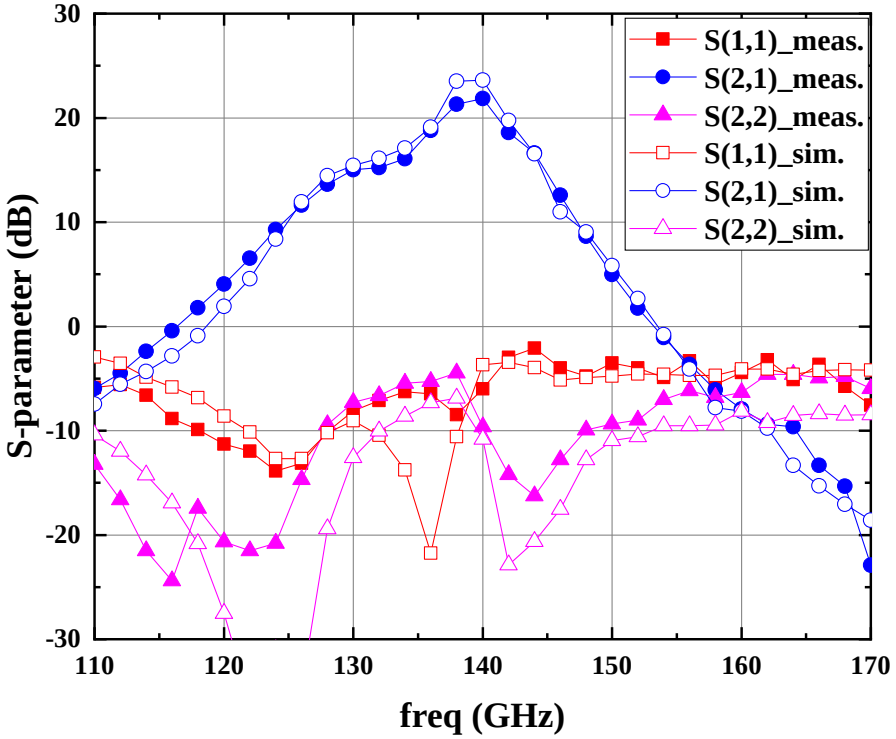

Fig. 2.61 The measured and re-simulated (assigning nch+EM device model) results of S-parameters.

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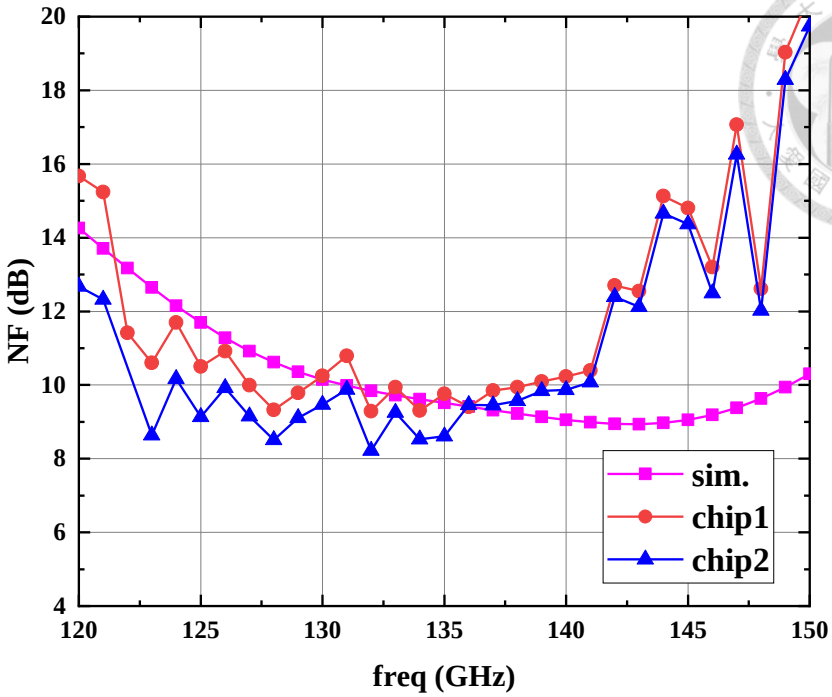

Fig. 2.62 The measured and re-simulated (assigning nch+EM device model) results of the noise figure

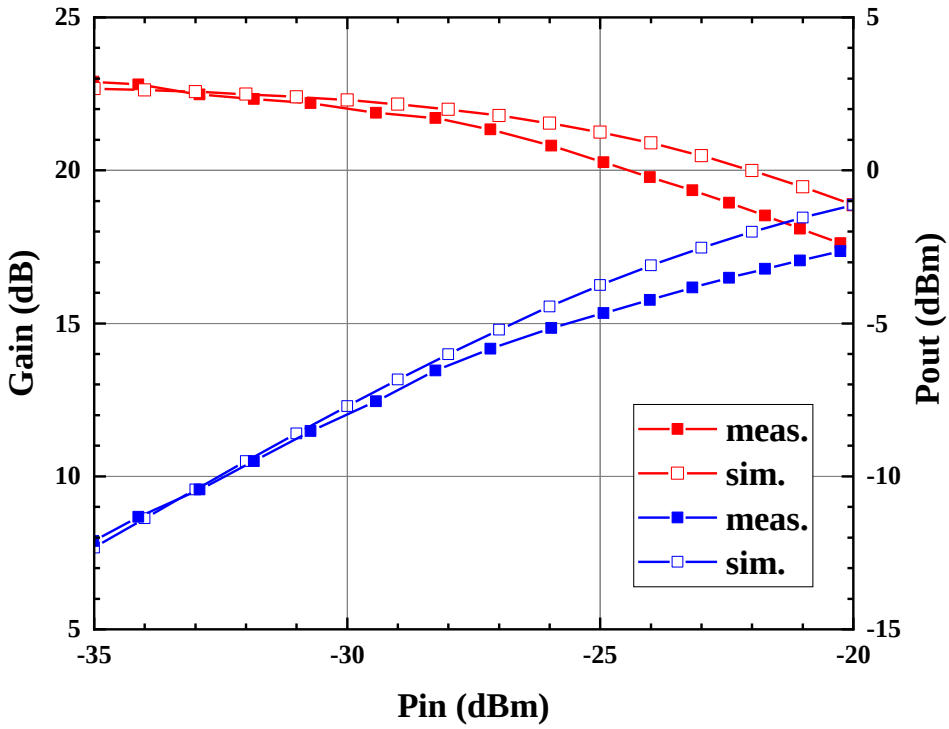

Fig. 2.63 The measured and re-simulated (assigning nch+EM device model) results of the large signal at 140GHz.

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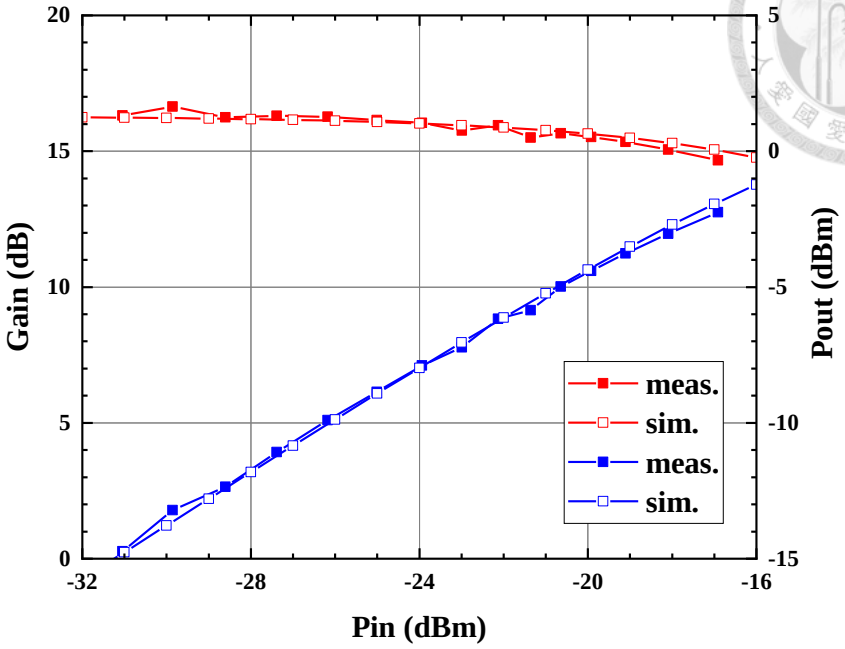

Fig. 2.64 The measured and re-simulated (assigning nch+EM device model) results of the large signal at 144GHz.

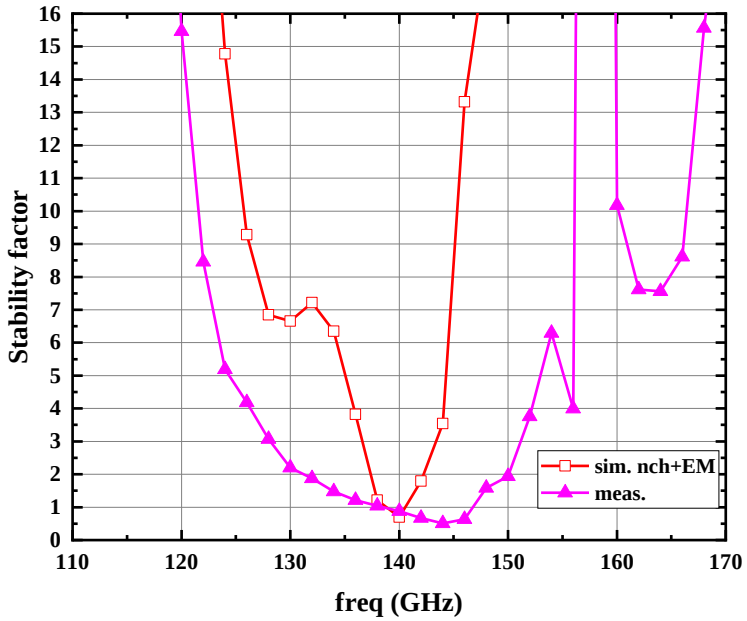

Fig. 2.65 The measured and re-simulated (assigning nch+EM device model) results of the stability factor.

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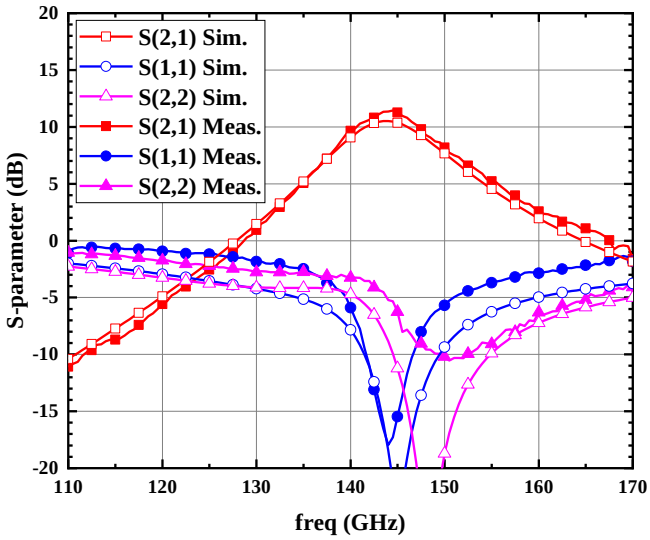

Fig. 2.66 The measured and re-simulated (assigning nch+EM device model) S-parameter of the single-stage amplifier.

2.5.4 Re-design and Verification

To validate the proposed modeling approach, instead of drawing conclusions retrospectively from measured circuit performance, the circuit design was directly implemented using the nch+EM approach instead of the TSMC-provided RF model. This demonstrates the accuracy of the high-frequency transistor modeling method. Since the Gmax core is highly sensitive to transistor characteristics, especially phase deviation may lead to results that deviate from expectations. Therefore, impedance matching and transmission line sections were redesigned under the same architecture to have better noise performance. The design methodology and bias conditions remain unchanged and are not repeated here. At the first stage, the transmission line lengths are set to 101 μm, 97 μm, and 234 μm, respectively. In previous work, the simulation based on the foundry RF model exhibited inaccurate S_{12} magnitude and phase due to inadequate modeling of the gate–drain capacitance (C_{gd}). This inaccuracy causes phase deviation in the Gmax-core and shifts its conjugate and noise matching conditions. After the parasitic extracted, the S_{12} and the effect of C_{gd} were properly simulated with a more accurate prediction of

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phase and reverse gain. As shown in Fig. 2.67, Gmax-core achieves a higher gain, while the noise contribution of the subsequent stages is further suppressed, ultimately resulting in a reduced overall noise figure of about 1.5dB NF compared to the previous design.

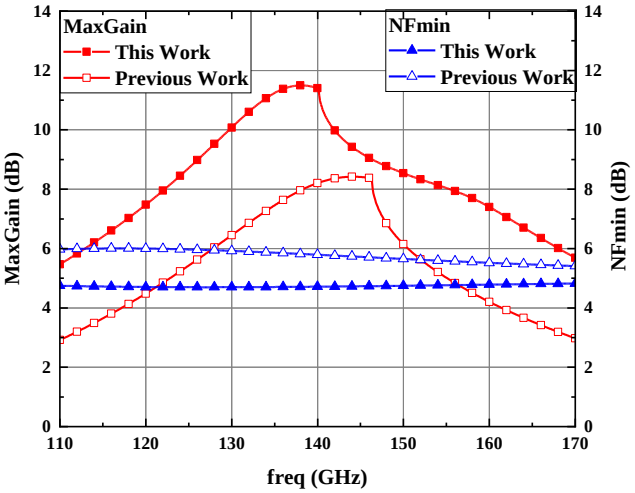

Fig. 2.67 The comparison of two versions of Gmax core.

The chip micrograph is shown in Fig. 2.68, with a total area of 0.42 mm². After excluding bypass capacitors and pads, the core circuit area is 0.113 mm².

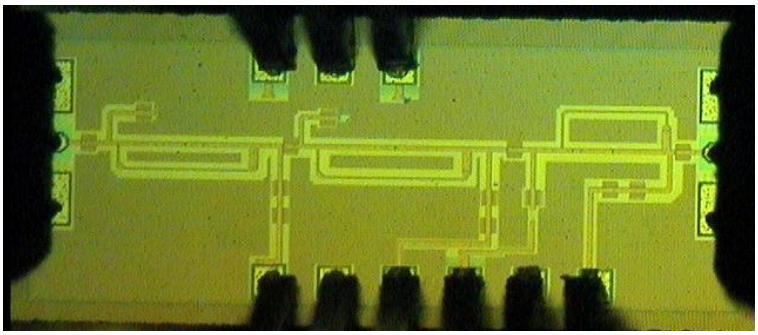

Fig. 2.68 The chip micrograph

Due to equipment limitations, S-parameters were measured in segmented frequency ranges of 110-145 GHz at NTU and 145-220 GHz at TSRI, while the large signal and noise measurements were all conducted at TSRI. As shown in Fig. 2.69, the small-signal gain achieved a peak of 18.7 dB at 138 GHz, with a 3-dB bandwidth of 27 GHz, ranging from 128 to 155 GHz.

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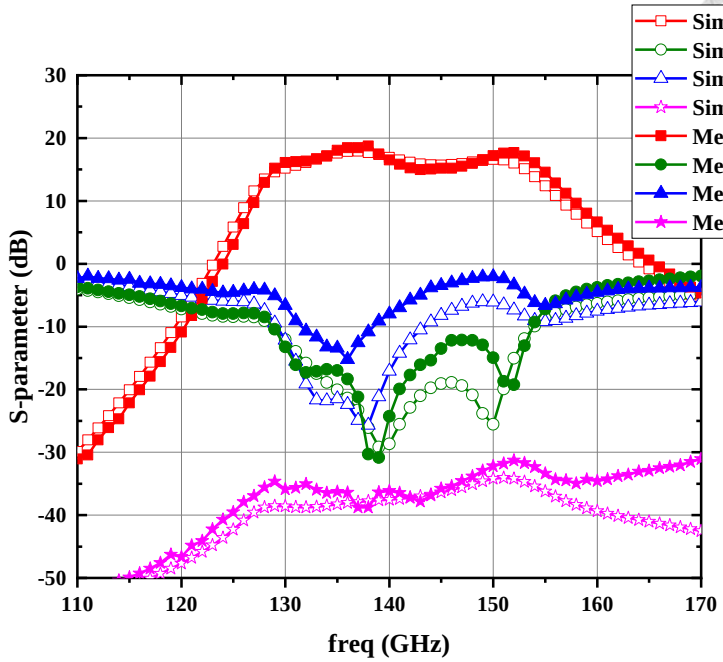

Fig. 2.69 The measured and simulated (assigning nch+EM device model) S-parameter of the re-designed LNA

Noise figure was measured using a frequency extension module (SAX) that down-converted the signal to 0.5 GHz for receiver detection. The measured results are shown in Fig. 2.70. The NF curve exhibits significant fluctuations because no high-gain LNA was connected after the DUT, leaving the output noise uncompressed and increasing calibration uncertainty. The minimum measured NF was 4.8 dB, while the average NF across the 128-155 GHz band was 5.8 dB.

Large-signal characteristics were also examined. A nearly constant 1-dB offset between the simulated and measured large-signal gain and output power was observed. This type of deviation is commonly attributed to absolute power calibration accuracy or load impedance sensitivity at high frequencies. As shown in Fig. 2.71 to Fig. 2.73, the simulated IP_{1dB} values were approximately -20 to -21 dBm. The measured IP_{1dB} values were slightly lower, in the range of -22 to -24 dBm.

The simulated and measured stability factors are shown in Fig. 2.74. The circuit is operating in an unconditional stable state.

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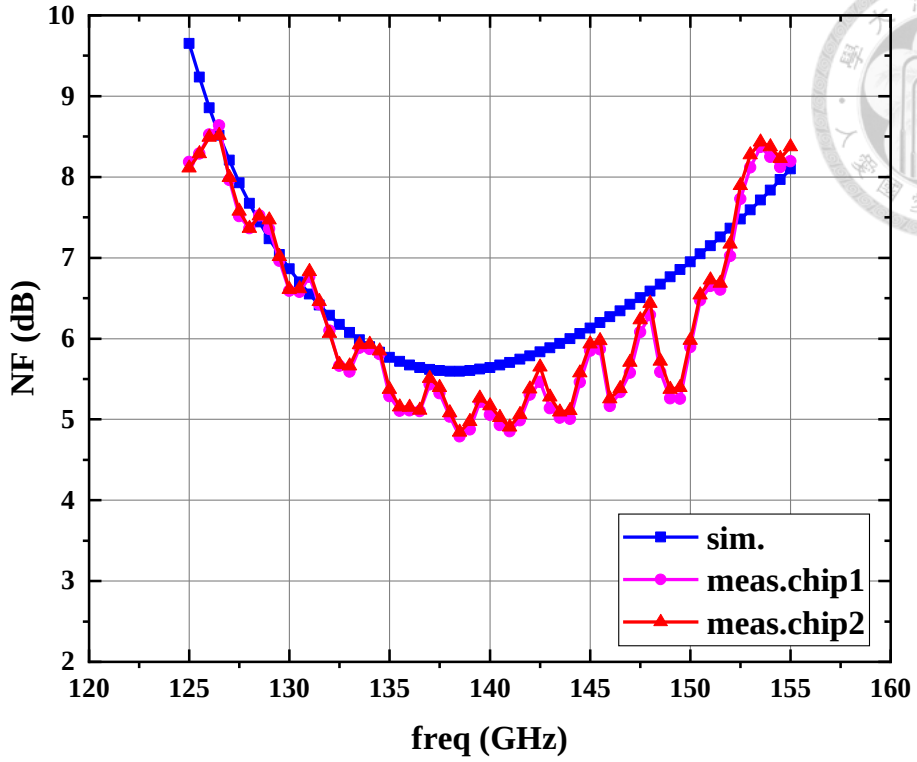

Fig. 2.70 Measured and simulated (assigning nch+EM device model) noise figure

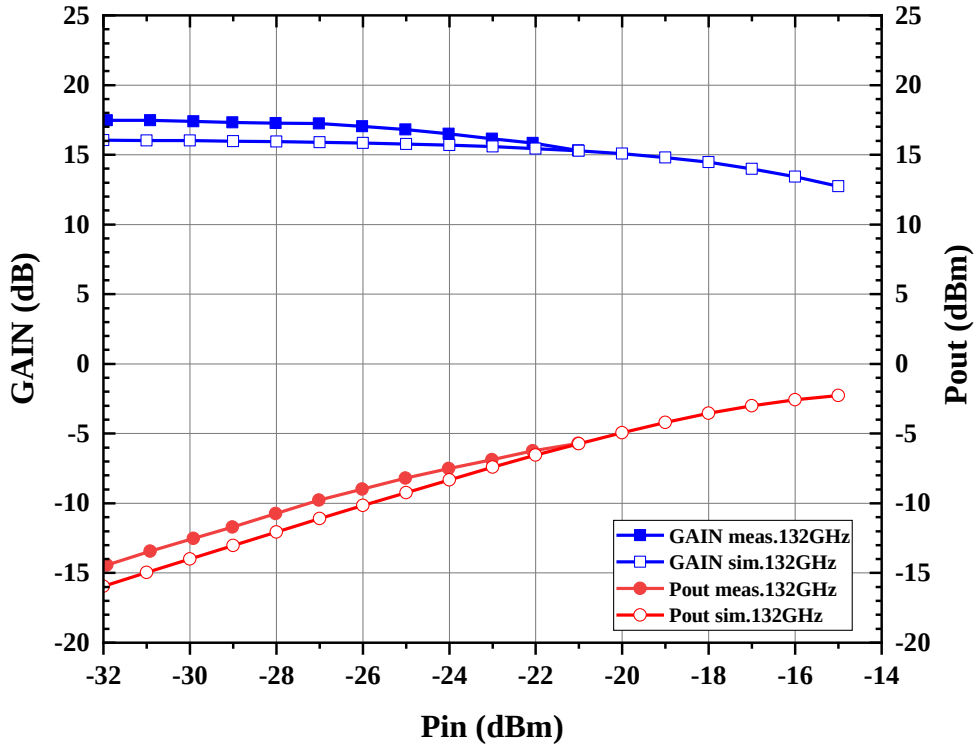

Fig. 2.71 The measured and simulated (assigning nch+EM device model) results of the large signal at 132 GHz.

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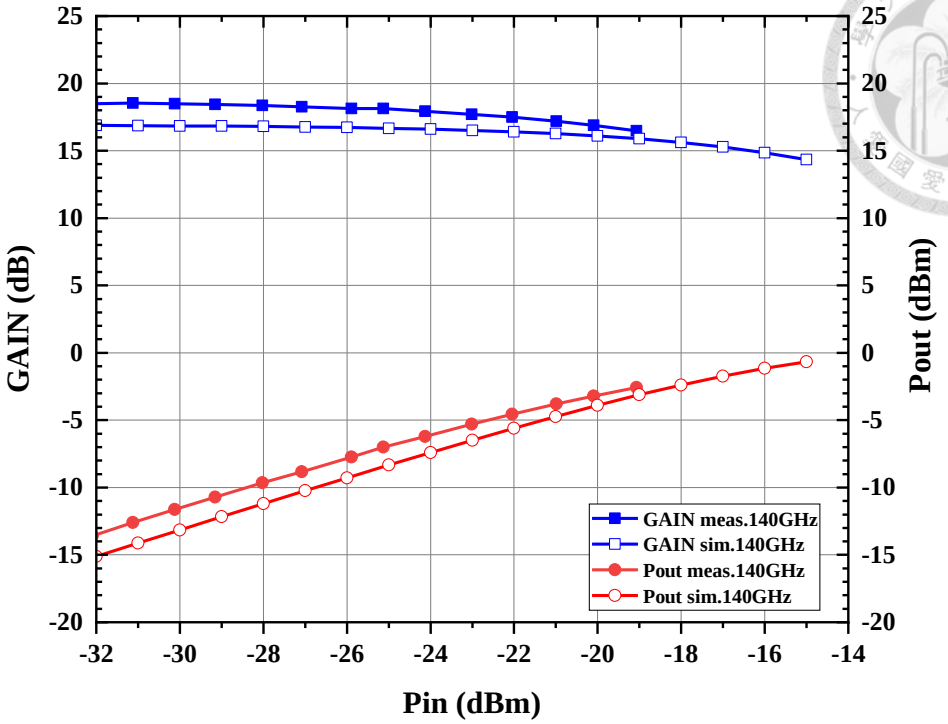

Fig. 2.72 The measured and simulated (assigning nch+EM device model) results of the large signal at 140 GHz.

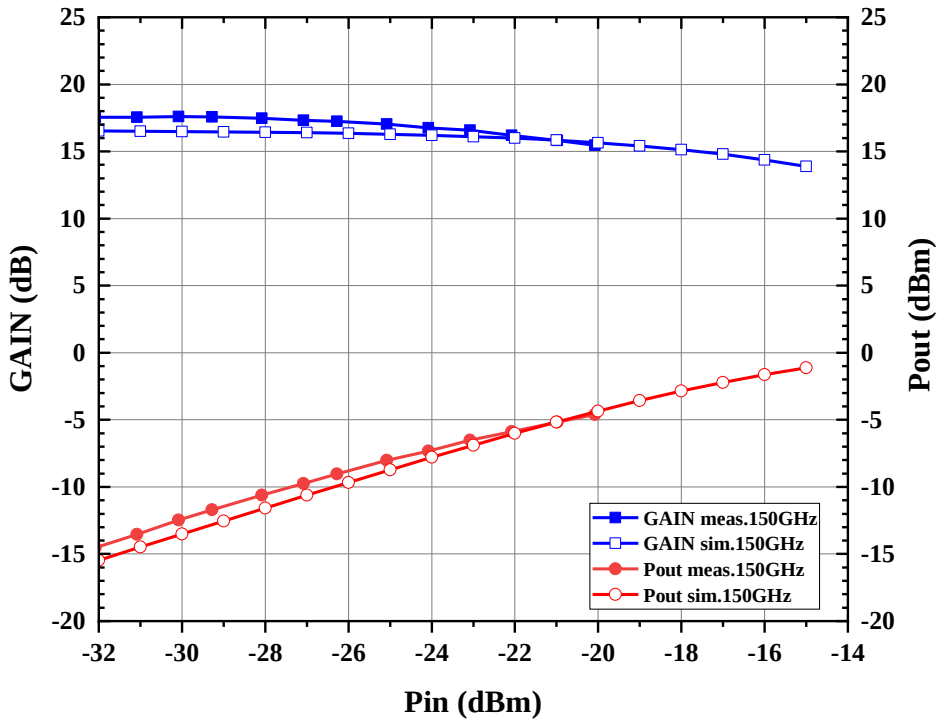

Fig. 2.73 The measured and simulated (assigning nch+EM device model) results of the large signal at 150 GHz.

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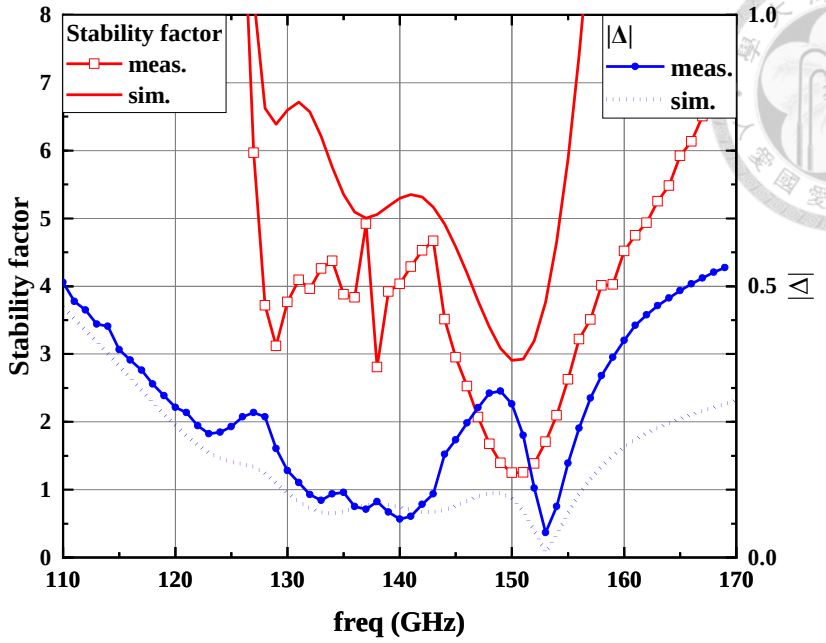

Fig. 2.74 The measured and simulated (assigning nch+EM device model) stability factor

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2.6 Summary

This chapter presents two versions of D-band low noise amplifiers fabricated using a 65-nm CMOS process. The first circuit adopts a three-stage Gmax-core architecture, achieving a small-signal gain of 22 dB, a minimum noise figure of 8.2 dB, and more than 15 dB gain over the 130–145 GHz frequency range, while consuming only 17.3 mW of DC power. The second circuit, the redesigned circuit, also employing a three-stage Gmax-core topology, achieves a peak gain of 18.7 dB with a 27-GHz 3-dB bandwidth from 128 to 155 GHz, a minimum noise figure of 4.8 dB with 5.8 dB average under the same power consumption. To achieve low noise performance, simultaneous noise and input matching is performed at the first stage, and the Gmax-core topology ensures sufficient gain. In addition, a detailed high-frequency circuit simulation methodology is proposed in this chapter to address the challenges arising from the unpredictable characteristics of transistors under high-frequency operation.

Table 2.2 summarizes the performance of recently published D-band CMOS LNAs, where the figure-of-merit (FoM) [50] is employed to evaluate LNA performance in terms of gain-bandwidth product, noise figure, and DC power consumption.

$$FoM = \frac{S_{21,\mathrm{Mag}} \times Bandwidth\,[GHz]}{\left(NF_{\mathrm{Mag}} - 1\right) \times P_{\mathrm{DC}}[mW]} \tag{2.14}$$

Compared with all previously published LNAs, the proposed design exhibits a highly competitive FoM, demonstrating competitive performance characteristics within a mature CMOS process.

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Table 2.2 Summary of previously published D-band LNA

Ref.	Process	Architecture	Freq. (GHz)	Gain (dB)	NF (dB)	IP_{1dB} (dBm)	P_{dc} (mW)	Core Area (mm2)	FoM
[20]	130-nm SiGe BiCMOS	7×CS	140-220	15.8	6.1	-16.7	46.0	0.48	21.5
[13]	28 nm	4×cascode+1×CS	129-157.5	16.3	9.6	-19	38.8	0.4*	3.6
[14]	65 nm	2×CS(Gmax-core)	145-155	17.9	4.7	-23	13.7	0.193	23.1*
[16]	28 nm	4×Differential CS	104-132*	21.7	8.4	N/A	18	0.12	14.4*
[18]	28 nm SOI	4×CS	143-166	15.7	8.5	N/A	32	0.34	4.4
[51]	40 nm	2×cascode+1×CS	139.9-166.7	18.4	5.7	-17	17.3	0.062	38.3
[52]	28 nm	4×Differential CS	135-150	25.4	4.5(min) 5.1(avg)	-24	30.6	0.325	93.5
[53]	40 nm	1×CS+ 4×Differential CS (Gmax-core)	140.6-159.4	20	4.9(min) 6.5(avg)	-22.4	19.3	0.22	45.9
[54]	40 nm	4×CS(Gmax-core)	140-147	27.7	9	-26.2	27.1	0.348	21.9
This work	65nm	3×CS(Gmax-core)	140 (136~144)	22	8.2	-27@140GHz -18@144GHz	17.3	0.12	13.1
This work 2	65nm	3×CS(Gmax-core)	128-155	18.7	4.8(min) 5.8(avg)	-22 ~ -24	17.3	0.113	57.3

*Estimated from the figure

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Chapter 3 Design of a Q-Band Low-Noise Amplifier

3.1 Introduction

With the continuous advancement of astronomical observation technologies, the demand for detecting extremely weak cosmic radio-frequency (RF) signals has been steadily increasing. Particularly in the millimeter-wave and sub-millimeter-wave frequency ranges, these RF signals are subject to significant attenuation as they traverse the atmosphere and propagate over long distances, ultimately arriving at ground-based receiving systems with extremely low power.

Taking the Atacama Large Millimeter/submillimeter Array (ALMA) as an example, the system consists of 66 antennas covering a frequency range from 30 GHz to 950 GHz, partitioned into ten sub-bands. Each frequency band is equipped with dedicated receivers and frontend amplifier modules to effectively process and amplify weak RF signals across different bands[11].

To ensure the reliability of astronomical observation data, the receiver must possess sufficiently high sensitivity to effectively detect extremely low-intensity signals originating from outer space. In general, the sensitivity of a receiving system can be described by the following equation[47]:

$$Sensitivity = kT_0 \cdot BW \cdot (S/N)_{min} \cdot NF_{sys} \tag{3.1}$$

where k is Boltzmann's constant, T_0 is the absolute temperature at the receiver input, BW is the receiver bandwidth, SNR_{min} denotes the minimum acceptable signal-to-noise ratio, and NF represents the noise figure of the system. It is evident from this equation that the noise figure has a direct impact on the overall system sensitivity. If the noise figure is excessively high, the minimum detectable signal strength will be elevated, thereby compromising the ability to detect weak signals, even under otherwise ideal conditions.

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Moreover, practical RF receiver systems typically comprise multiple stages of amplifiers, filters, and other components. The overall system noise figure is determined not by a single component, but rather by the collective contributions of all stages. According to Friis' noise equation, the total noise figure of a multi-stage system can be expressed as follows[48]:

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \ \ldots \tag{3.2}$$

where NF_1 is the noise figure of the first stage, typically the LNA, NF_2 and NF_3 are the noise figures of subsequent stages, and G_1 and G_2 denote the gain of the first and second stages, respectively. It can thus be concluded that both the noise figure and gain of the first-stage LNA have a decisive influence on the overall noise performance of the system. A lower noise figure and higher gain in the first-stage LNA can effectively suppress the noise contributions from subsequent stages.

In the overall receiver chain, the low-noise amplifier serves as the key component for enhancing system sensitivity. The LNA is typically implemented as the first stage at the receiver front-end, and its noise figure and gain directly determine the overall system signal-to-noise ratio. If the LNA exhibits a high noise figure, any signal amplification by subsequent stages can only partially compensate for the noise penalty, making the performance of the first-stage LNA critical to the system.

In practical implementations, the first-stage LNA is often operated at cryogenic temperatures to further reduce noise. However, subsequent components such as waveguides, filters, and isolators inevitably introduce additional signal loss, necessitating the use of room-temperature LNAs to provide further signal amplification and to maintain overall signal strength while controlling the total system noise figure. According to the ALMA system design, the room-temperature LNA must provide at least 15 dB of gain

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without significantly increasing the overall system noise figure to meet the requirements of backend signal processing.

In previous LNA designs, two widely adopted architectures are the distributed amplifier (DA) and multi-stage cascade structures. Distributed amplifiers exhibit excellent broadband characteristics, making them suitable for ultra-wideband applications. However, the accumulation of intrinsic noise sources across multiple stages, combined with the distributed architecture's inherent gain sacrifice, typically results in higher power consumption and larger chip area, making it challenging to simultaneously achieve high sensitivity and low power. On the other hand, the multi-stage cascade architecture allows for a division of functionality, wherein the preceding stage primarily minimizes noise while the subsequent stage provides additional gain. This approach facilitates the realization of low noise figure and high gain, yet an increased number of stages introduces challenges such as higher power consumption, stability concerns, and larger chip area. Therefore, the selection of circuit topology must be carefully balanced according to specific application requirements[11, 12].

In this work, a two-stage amplifier architecture is implemented using a 90-nm CMOS process. As shown in Table 3.1, the design targets a frequency range of 33–50 GHz, a gain of 15 dB, a noise figure of 4 dB, an input 1-dB compression point (IP1dB) of –20 dBm, and a power consumption of 10 mW. The first stage adopts a cascode configuration with a noise-reduction transformer introduced between stages to provide inductive coupling. This design not only effectively isolates noise sources and reduces feedback from the common-gate stage to the input but also enhances inter-stage impedance matching and improves overall circuit stability. The first stage is primarily optimized for noise suppression at the front-end while maintaining input impedance matching and stability, as illustrated Fig. 3.1. The second stage employs a current-reuse

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technique, as shown in Fig. 3.2, which increases the overall gain and enables effective power consumption control, thereby allowing the amplifier to achieve both high gain and low noise figure across the target frequency band. Given the susceptibility of high-frequency amplifiers to parasitic capacitance and impedance mismatch, stability design is of particular importance. In this design, inductive coupling and a second-order LC output matching network are utilized to further enhance broadband stability.

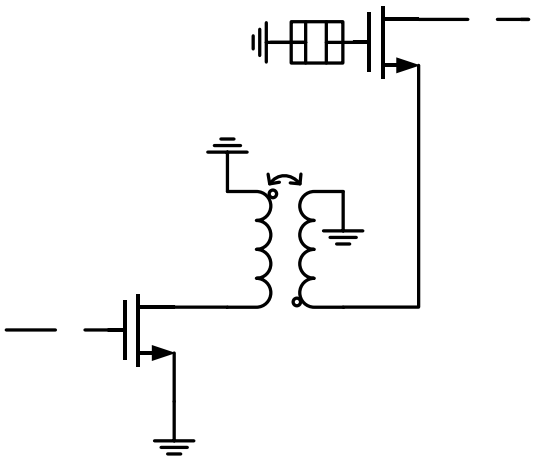

Fig. 3.1 Architecture of noise reduction transformer

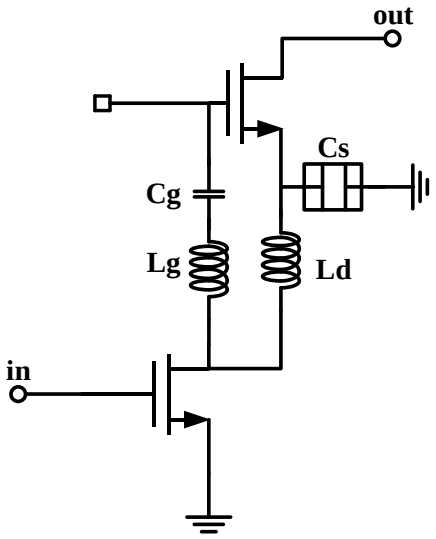

Fig. 3.2 Architecture of current reuse

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Table 3.1 The design goals of Q-band LNA.

	Specification
Process	90-nm CMOS process
Frequency (GHz)	33-50
Gain (dB)	15
Noise Figure(dB)	4
***IP*$_{1dB}$ (dBm)**	-20
Power consumption (mW)	10

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3.2 The Design of Q-band LNA

The low-noise amplifier plays a critical role in wireless receiver systems by enhancing signal strength and reducing the overall system noise. The key performance metrics of an LNA, including gain, noise figure, bandwidth, DC power consumption, and stability, are predominantly influenced by the circuit topology, bias conditions, and transistor sizing.

The proposed design adopts a two-stage amplifier architecture. The first stage utilizes a cascode configuration in conjunction with a noise-reduction transformer to achieve input matching and noise suppression, thereby maintaining high gain while ensuring both stability and optimal noise matching. The second stage employs a current-reuse cascode technique to deliver broadband high-gain performance with low power consumption.

In the first stage, the noise-reduction transformer facilitates impedance transformation between the common-source and common-gate nodes, enabling the simultaneous realization of high gain and minimum noise figure, while suppressing the noise contribution of subsequent stages and enhancing the overall noise and stability performance. The second stage leverages the current-reuse cascode architecture to achieve low power consumption and high gain, while a second-order LC output matching network is employed to further extend the bandwidth.

3.2.1 Transistor Size and Biasing Selection

To determine the optimal device parameters for the first-stage amplifier, the physical characteristics of the transistor were analyzed. Simulations of the DC-IV curve, transconductance, and drain current under different gate bias conditions were performed for a device with gate width w = 1.6 μm and finger number nr = 12, as shown in Fig. 3.3.

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Although the peak transconductance is achieved at V_g = 0.9 V, as shown in Fig. 3.4, the LNA is typically operated in the small-signal region for practical applications. Therefore, it is unnecessary to bias the device at the point of maximum g_m, which corresponds to a high drain current region. As shown in Fig. 3.5, the LNA is usually biased at 50 to 70 percent of the maximum drain current; however, this work chooses approximately 25% I_D of peak g_m for best noise performance.

Further analysis of Fig. 3.7, which shows the minimum noise figure and maximum gain as functions of gate bias V_d, indicates that a bias condition of V_g = 0.5 V and V_d = 0.9 V can achieve a favorable trade-off between low noise figure and high gain, while effectively reducing DC power consumption. Accordingly, the first-stage amplifier in this design adopts this bias setting to achieve an optimal balance among gain, noise performance, and power consumption.

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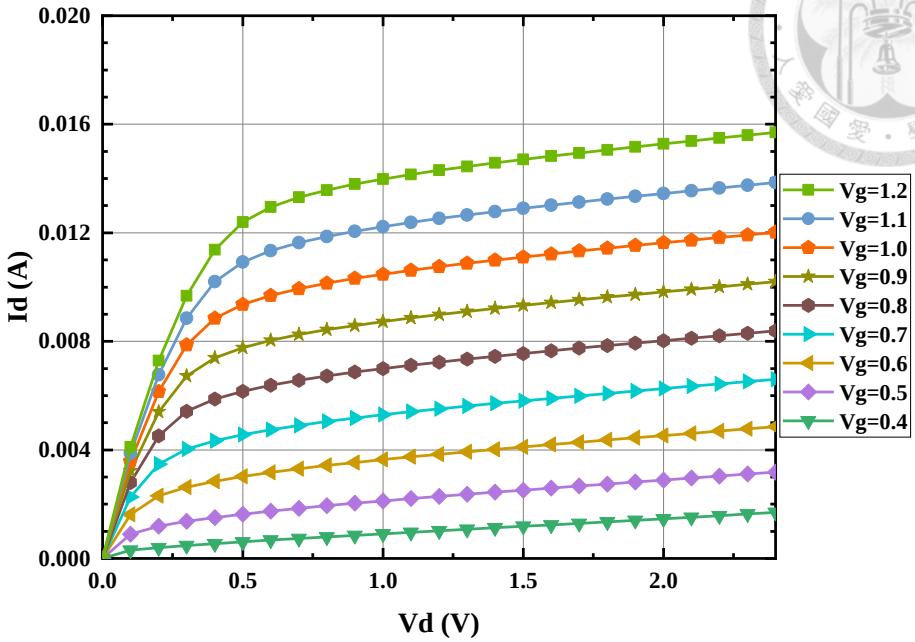

Fig. 3.3 DC-IV curve of the transistor with 12f ×1.6μm.

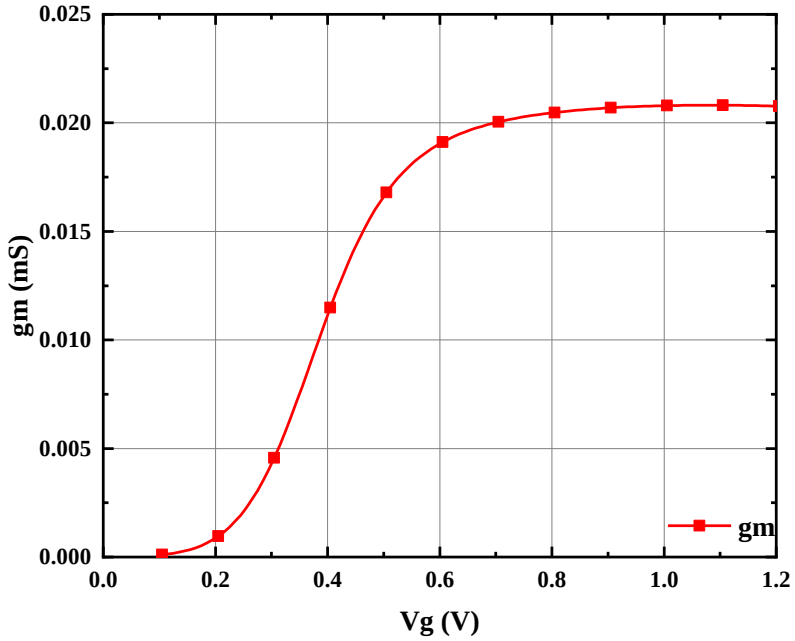

Fig. 3.4 Transconductance versus gate bias of the transistor with 12f ×1.6μm.

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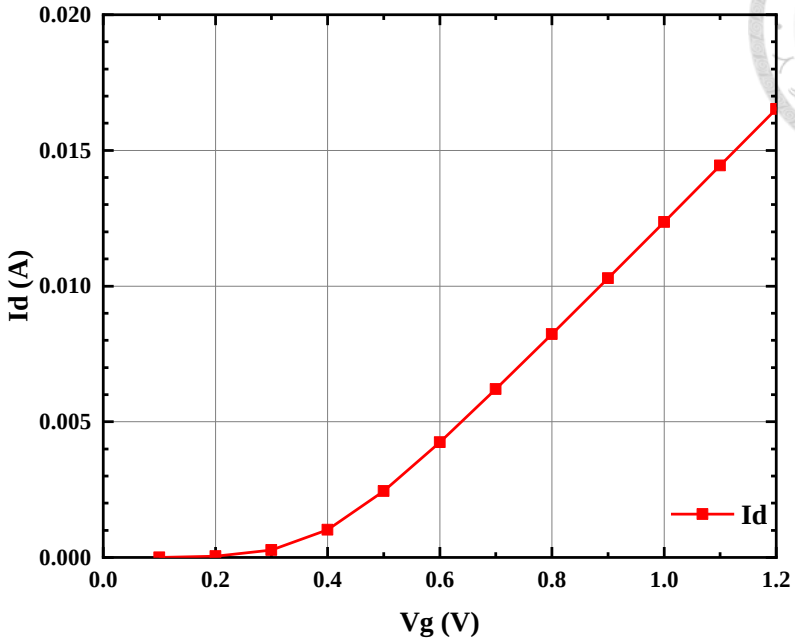

Fig. 3.5 Drain current of the transistor with 12f ×1.6μm.

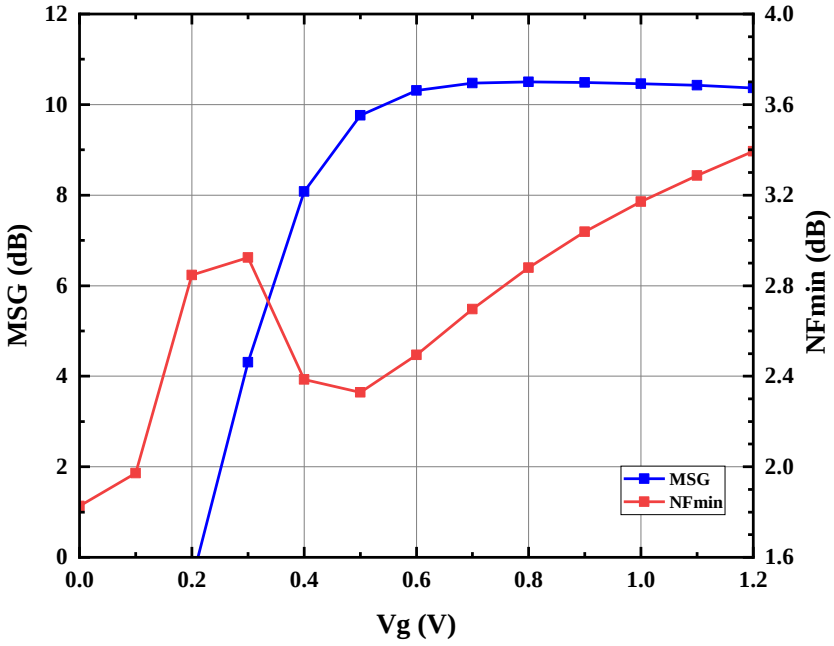

Fig. 3.6 Maximum gain and NF_{min} versus gate bias with 12f ×1.6μm at 40GHz.

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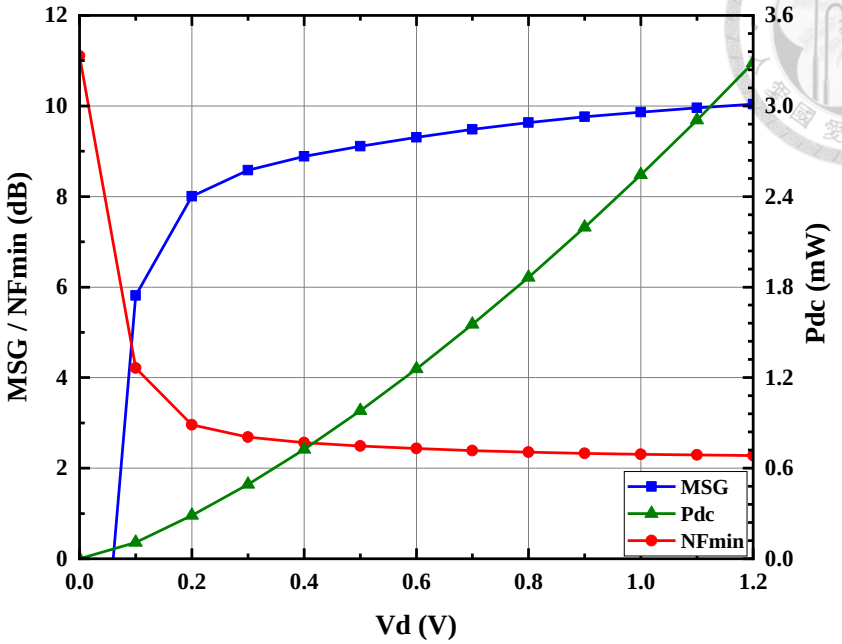

Fig. 3.7 Maximum gain, $NF_{min,}$ and P_{dc} versus V_d with 12f ×1.6μm at 40GHz.

In contrast to the first stage, which is primarily optimized for noise reduction, the main objective of the second-stage current-reuse cascode architecture is to enhance the overall gain. Although the same device dimensions are adopted, the bias settings are slightly adjusted to manage the overall power consumption. As shown in Fig. 3.8, which shows the dependence on DC power and drain bias V_d with current-reused condition, when VDD is reduced from the maximum allowable value of 2 V to 1.4 V, the DC power consumption of each transistor in the cascode stage decreases by approximately 1.7 mW. Consequently, the total power consumption of the second stage is reduced from 8.8 mW to 5.4 mW, resulting in an overall power saving of 3.4 mW, which corresponds to a 40 percent reduction. During this process, the maximum gain decreases by only about 0.5 dB, indicating that significant power savings can be achieved without sacrificing gain performance.

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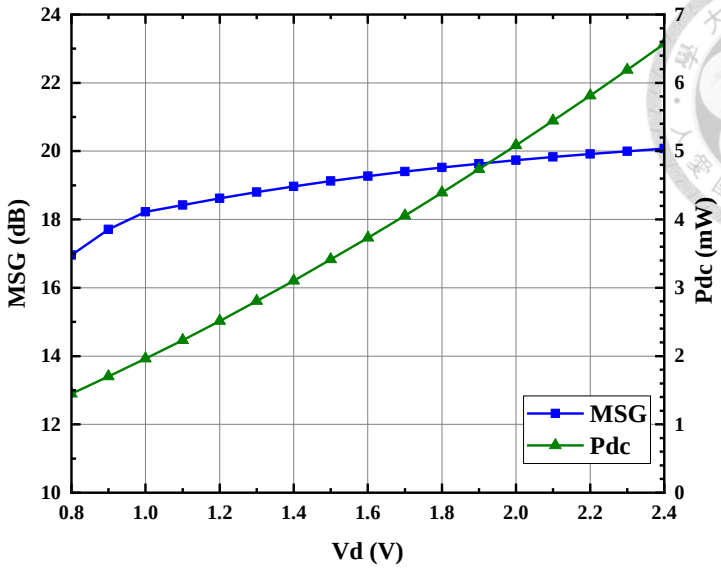

Fig. 3.8 Maximum gain and P_{dc} versus V_d with 12f ×1.6μm at 40GHz.

In terms of device sizing, smaller transistor dimensions typically result in a lower minimum noise figure (NF_{min}). However, excessively small devices lead to higher input impedance, making impedance matching more challenging and reducing stability. As shown in Fig. 3.10 and Fig. 3.11, using overly large device dimensions results in degraded gain and noise performance. Furthermore, as illustrated in the Smith chart, Fig. 3.9, when the device width is less than 1.5 μm, the impedance approaches the edge of the Smith chart, which significantly complicates impedance matching and leads to lower stability.

According to Fig. 3.11, which shows the relationship between NF_{min}, maximum gain, gate width, and finger number at 40 GHz, NF_{min} increases significantly when the gate width exceeds 1.8 μm. Regarding the number of fingers, as observed in Fig. 3.10, a smaller finger count provides better gain and noise performance, but again results in poorer stability, with the impedance moving even closer to the edge of the Smith chart.

Based on a comprehensive evaluation of gain, noise figure, and stability, the device dimensions were selected as 1.6 μm × 12 fingers. This choice ensures low noise and high gain while maintaining adequate stability.

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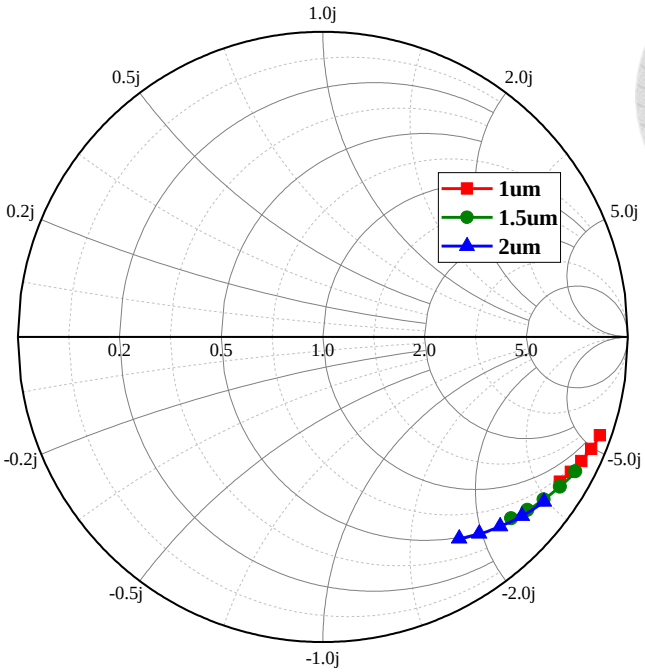

Fig. 3.9 Input impedance with different gate widths at frequency from 30 to 50 GHz

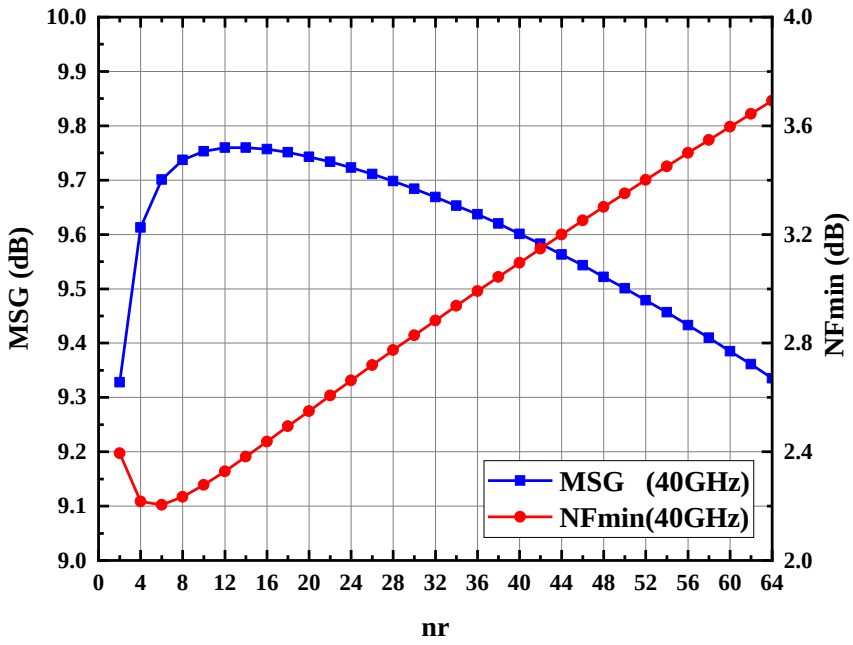

Fig. 3.10 Simulated MSG and NF_{min} versus numbers of fingers with 1.6μm gate width.

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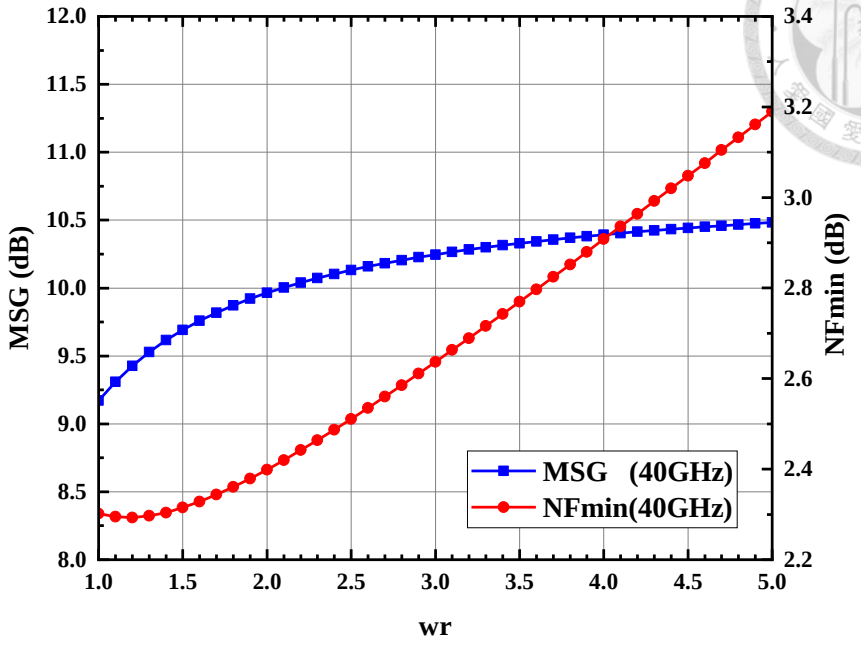

Fig. 3.11 Simulated MSG and NF_{min} versus gate width with 12 fingers.

In summary, through comprehensive parameter simulations and analysis of the data presented in Fig. 3.3 to Fig. 3.11, an optimal trade-off among gain, noise figure, stability, and power consumption was achieved. The device size was determined to be 1.6 μm × 12 fingers, with the first stage biased at V_d = 0.9 V and V_g = 0.5 V, and the second stage biased at V_d = 1.4 V and V_g = 0.5 V.

3.2.2 Noise-reduction Transformer

In millimeter-wave high-frequency LNA design, the cascode architecture often encounters difficulties in simultaneously achieving optimal noise performance and high gain. As a result, traditional designs may employ a single-stage common-source amplifier, which typically exhibits limited gain. To effectively suppress inter-stage parasitic and achieve wide bandwidth, low noise, and high stability, transformer coupling is adopted in this work for inter-stage matching between the CS and CG stages.

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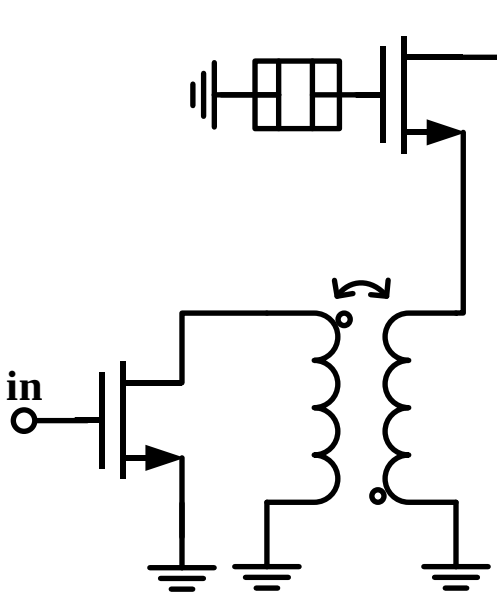

Fig. 3.12 Architecture of noise reduction transformer

As shown in Fig. 3.12, the first stage employs a common-source common-gate configuration, with a noise-reduction transformer used for impedance matching between the two stages. This transformer plays a critical role in the overall design and must be considered from the initial stage of the design process. To facilitate analysis, the mutual inductance model illustrated in Fig. 3.13 is first used to simplify the transformer characteristics, where

$$L_{eq,1} = L_1 \pm M \text{ , } L_{eq,2} = L_2 \pm M \tag{3.3}$$

$$M = K\sqrt{L_1 L_2} \tag{3.4}$$

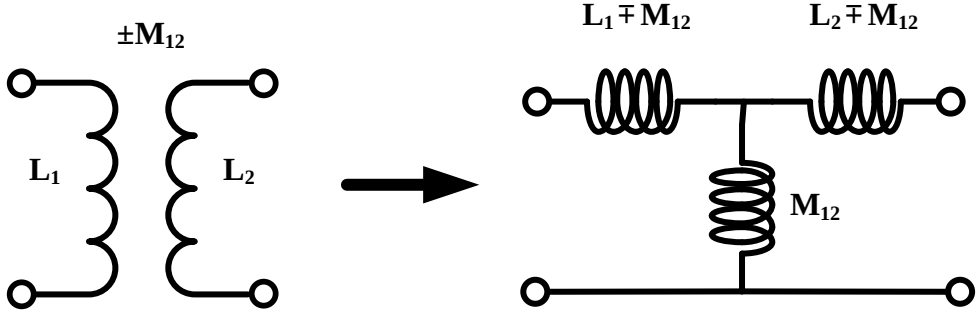

Fig. 3.13 Equivalent Inductive Coupling Diagram

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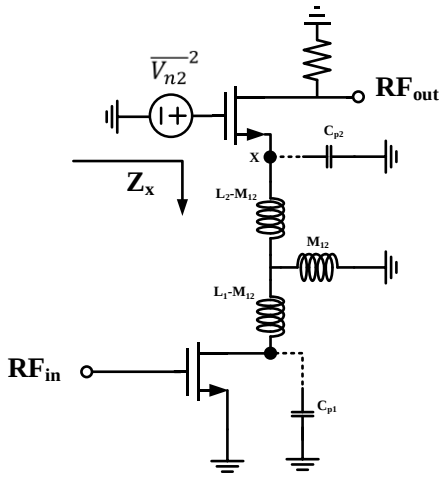

Fig. 3.14 Noise-reduced transformer with equivalent schematic.

The Fig. 3.14 shows the simplified schematic of the cascode amplifier. In the transformer design, it is also necessary to consider the parasitic capacitances C_{p1} and C_{p2} introduced by the transistors at the M_1 drain and M_2 source nodes, respectively. Under these conditions, the impedance seen from node X can be expressed as:

$$Z_x(\mathrm{s}) = \frac{s^3 C_{p1}\left(L_1 L_2 - M^2{}_{1,2}\right) + sL_2}{s^4\left[C_{p1}C_{p2}\left(L_1 L_2 - M^2{}_{1,2}\right)\right] + s^2\left(C_{p1}L_1 + C_{p2}L_2\right) + 1} \tag{3.5}$$

The noise contribution from V_{n2} can be expressed as

$$\frac{V_{n,out}}{V_{n2}} = \frac{-\mathrm{Z}_L}{\mathrm{gm}_2{}^{-1} + Z_x} \tag{3.6}$$

where it is desirable for Z_x to approach infinity. By utilizing the resonance between the equivalent inductance L_{eq} and the parasitic capacitances, the noise contributed by M_2 can be effectively suppressed at the target frequency W. The resonance condition can be described as

$$\omega^2 = \frac{(1 + \frac{C_{p2}}{C_{p1}}\frac{L_2}{L_1}) \pm \sqrt{(1 + \frac{C_{p2}}{C_{p1}}\frac{L_2}{L_1})^2 - 4(\frac{C_{p2}}{C_{p1}})(\frac{L_2}{L_1})(1 - k^2{}_{1,2})}}{2C_{p1}L_2(1 - k^2{}_{1,2})} \tag{3.7}$$

where C_{p1}, C_{p2}, and ω are constants. Therefore, by properly designing L_1, L_2, and the

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coupling coefficient K, the minimum noise figure can be brought closer to that of a common-source amplifier[24].

In the design of this transformer, L_1, L_2, and the coupling coefficient K are the critical parameters. For the purpose of achieving symmetry in the transformer layout, L_1 and L_2 are set equal, that is, $L_1 = L_2 = L$. Therefore, the design focuses on optimizing the values of the inductance L and the coupling coefficient K. As shown in Fig. 3.15 to Fig. 3.18, under ideal conditions, when K is relatively small, the minimum noise figure increases significantly, indicating ineffective suppression of the noise contributed by M_2. On the other hand, excessively large values of K present practical challenges in transformer implementation and insufficient stability. If the inductance L is chosen too small, stability may become insufficient, while overly large values of L result in increased chip area and implementation difficulties. Based on these considerations, $L_1 = L_2 = 520$ pH and K = 0.7 are selected as the final design parameters.

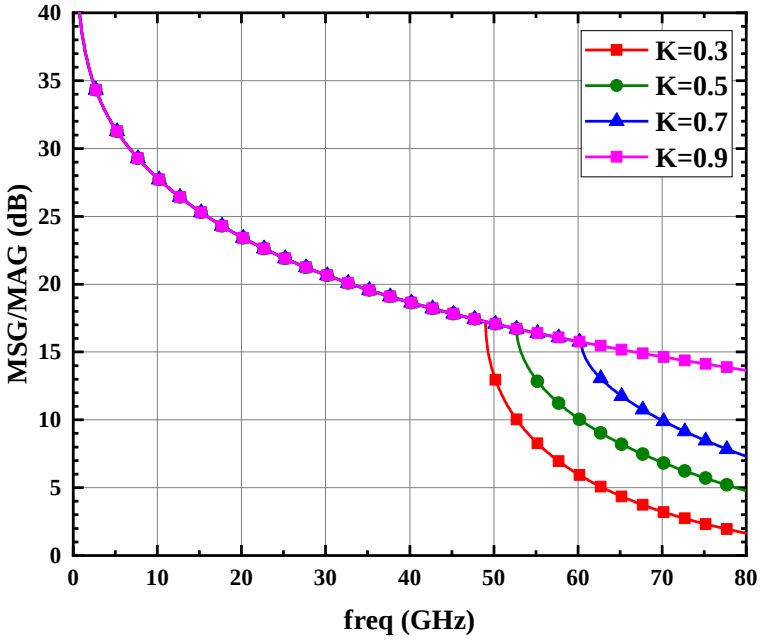

Fig. 3.15 Maximum gain in different coupling coefficients.

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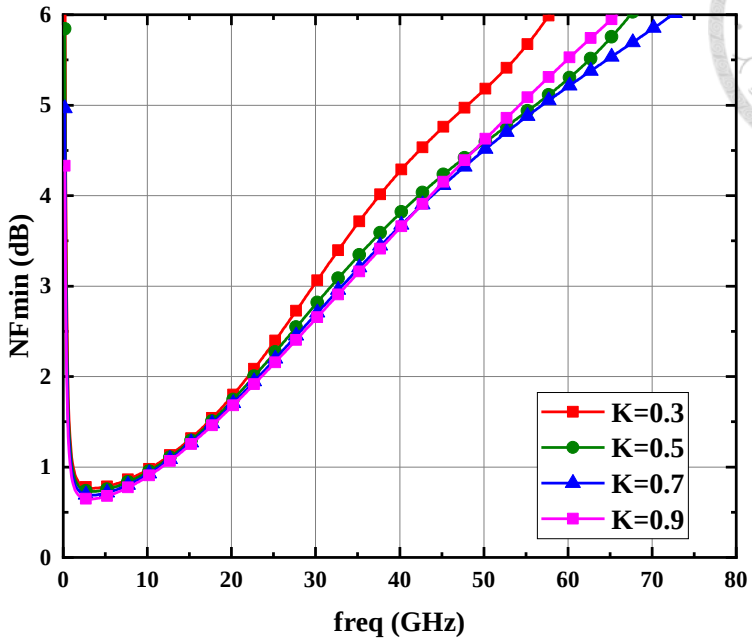

Fig. 3.16 NF_{min} in different coupling coefficient.

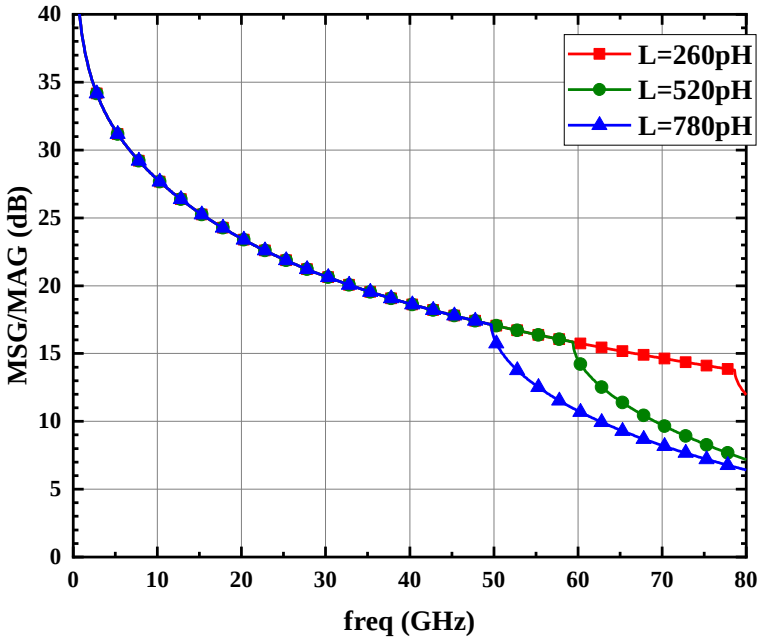

Fig. 3.17 Maximum gain in different inductances.

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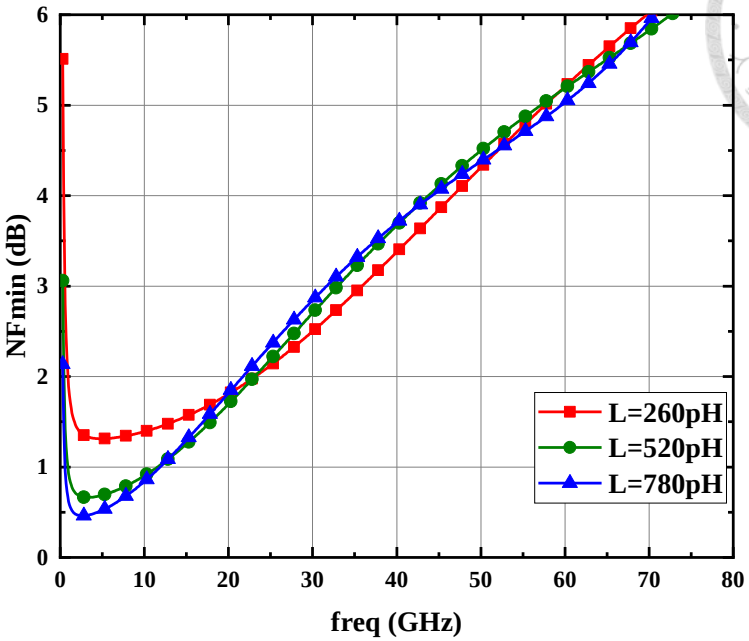

Fig. 3.18 NF_{min} in different inductances.

The 3-D structure of the transformer utilized in this design is shown in Fig. 3.19, where edge coupling on the M_9 layer enhances the coupling coefficient K. As shown in Fig. 3.20, the first stage achieves higher gain and improved noise suppression compared to conventional common-source amplifiers with source degeneration, albeit with a slight NF_{min} increase of approximately 0.5 dB. As to the comparison of the normal cascode and the inductor matching between CS and CG, the NF_{min} of the noise-reduction transformer is 0.3 dB less than the cascode topology, and the stability of these two architectures is insufficient with the same device size. Thus, the noise-reduction transformer in the first stage provides an optimal balance between low noise and high gain, maximizing the overall amplifier performance.

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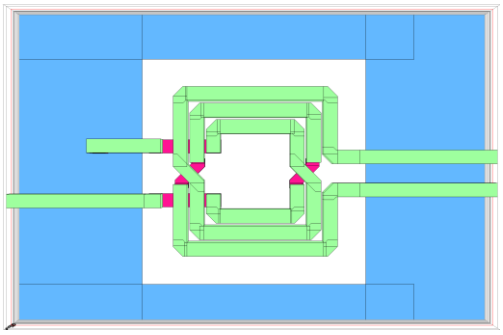

Fig. 3.19 3D structure of the proposed noise-reduced transformer.

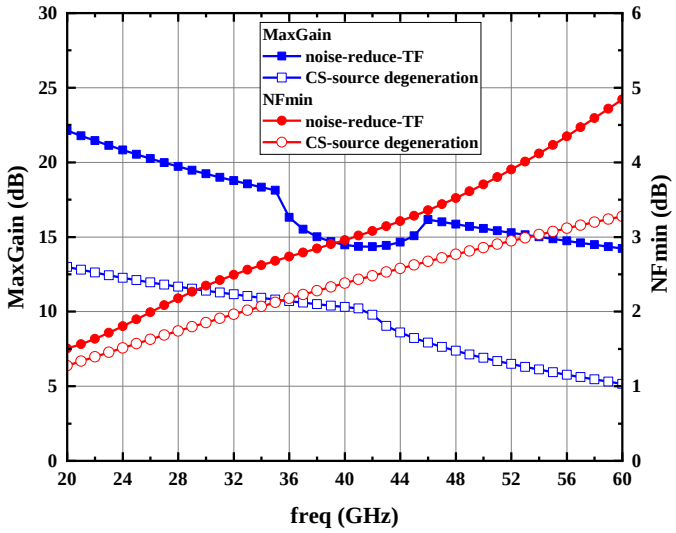

Fig. 3.20 Comparison of noise reduction transformer and CS topology of maximum gain and $NF_{\min}$.

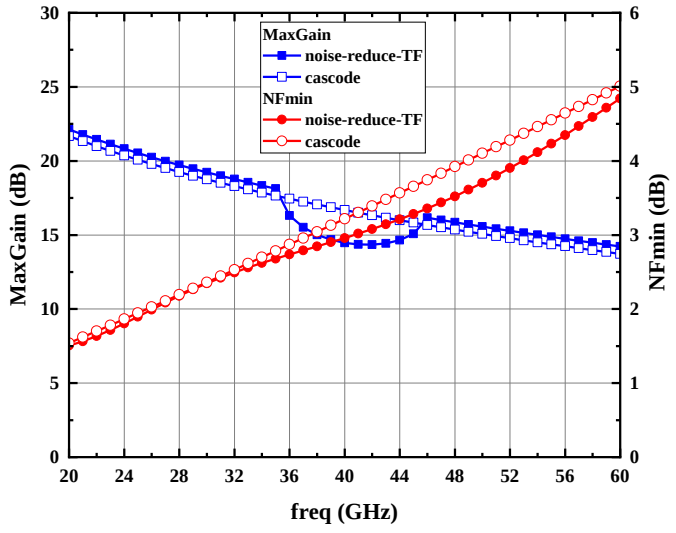

Fig. 3.21 Comparison of noise reduction transformer and cascode topology of maximum gain and $NF_{\min}$.

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3.2.3 Current reuse technique

To achieve high gain, the current-reuse architecture offers the advantage of enhanced high-frequency performance within a limited power budget. Therefore, the current-reuse technique is adopted in this design. As illustrated in Fig. 3.22, the upper and lower amplifier stages share the same DC current path. The DC current flows from the source of the second-stage amplifier (M_2) into the drain of the first-stage amplifier (M_1). From a small-signal perspective, this configuration is equivalent to two common-source stages connected in series, which significantly increases the overall transconductance and gain.[23]

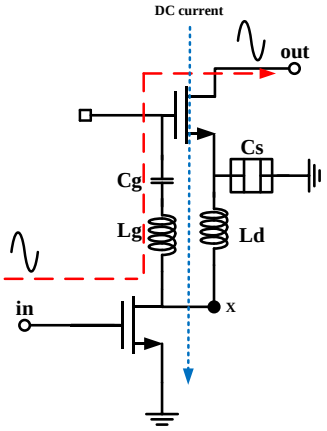

Fig. 3.22 Current reuse topology.

Fig. 3.23 presents the small-signal equivalent model of this architecture. The bypass capacitor at the source of the second-stage transistor M_2 provides an AC ground path, enabling M_2 to operate in the common-source configuration under small-signal conditions instead of the common-gate configuration. This AC isolation effectively suppresses inter-stage interaction and improves overall system stability.

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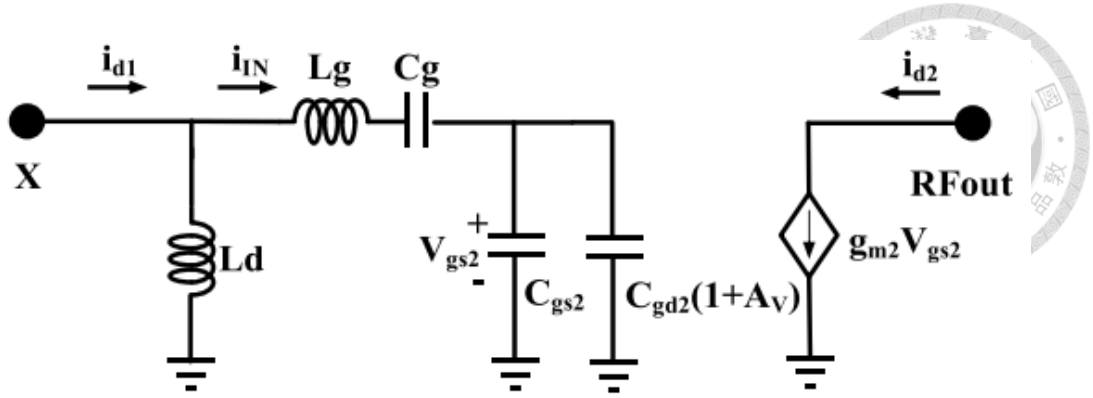

Fig. 3.23 Small signal model of current reuse topology.

In the current-reuse technique, the key components include the inductors L_d and L_g, as well as the bypass capacitor. The selection of the inductors begins with idealized conditions, where all other components are assumed to be ideal large capacitors and inductors. The value of L_d is swept as shown in Fig. 3.24. If L_d is too small, the stability is insufficient, whereas if L_d is too large, the circuit becomes excessively stable. Therefore, L_d is set to 200 pH.

Fig. 3.25 further simulates the impact of different L_g values on both stability and maximum gain. It can be observed that L_g, together with the parasitic capacitance at that node, forms a resonance that affects the high-frequency bandwidth. As a result, L_g = 240 pH is chosen to achieve an appropriate gain.

Fig. 3.27 shows the insertion loss of L_g = 240 pH when C_s is chosen to 200 fF. The insertion loss is below 0.5 dB, ranging from 20 to 50 GHz.

Fig. 3.26 shows the isolation between the 2pF bypass capacitor and L_d. For M_2, the isolation is at least -21 dB from 30 to 50 GHz, indicating that the transistor M_2 operates in the common-source configuration.

Under these conditions, the current-reuse technique further helps reduce overall DC power consumption while maintaining comparable gain performance, leading to a moderate improvement in the circuit figure of merit (FoM).

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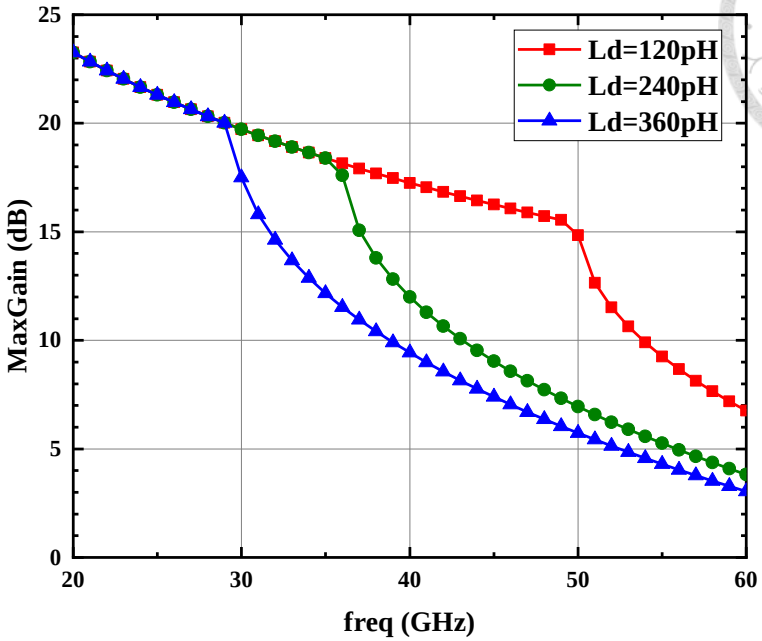

Fig. 3.24 Maximum gain in different L_d with C_g as a DC block and L_g shorted.

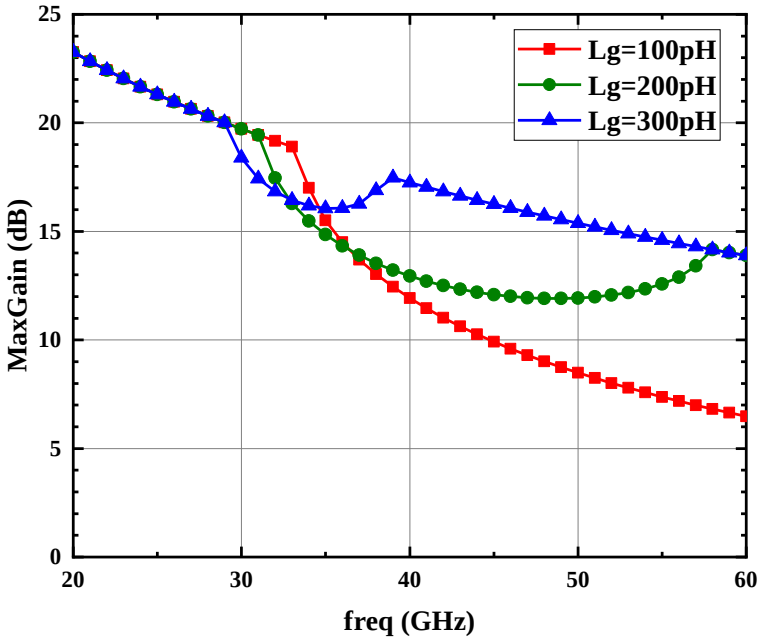

Fig. 3.25 Maximum gain in different L_g with fixed L_d=240pH

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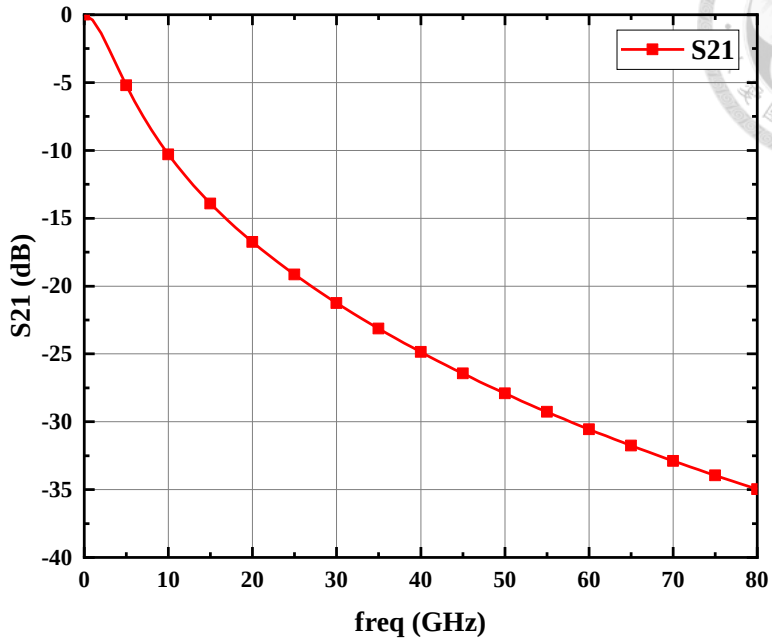

Fig. 3.26 Simulated isolation of L_d and C_s as a bypass element.

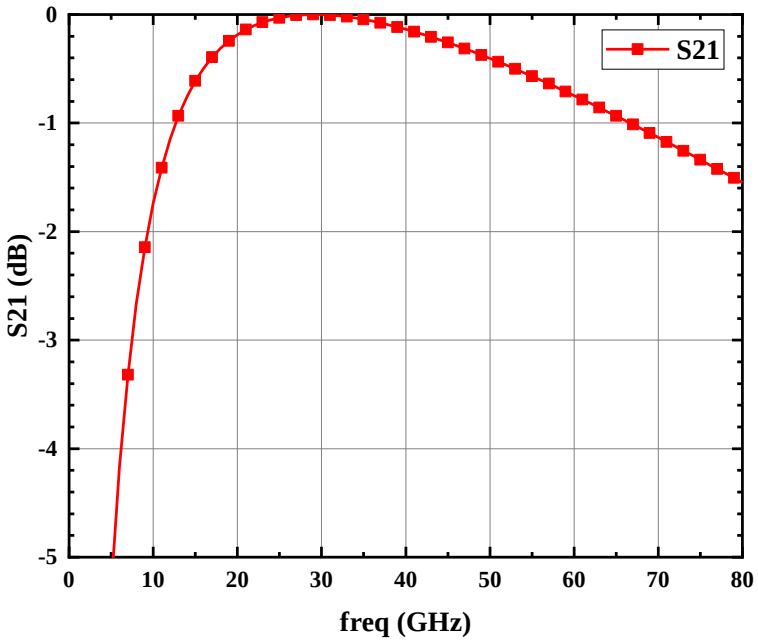

Fig. 3.27 Simulated insertion loss of L_g and C_g

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3.3 Circuit Schematic and Simulation Results

3.3.1 Circuit Schematic

The proposed low-noise amplifier is implemented using the TSMC 90 nm GUTM CMOS process, utilizing an ultra-thick metal (UTM) structure that includes nine metal layers (M_1 to M_9), two metal-insulator-metal (MIM) capacitor layers, and one polysilicon layer. All active devices are based on the 90 nm CMOS small-signal and large-signal transistor models provided by TSMC. Full-wave electromagnetic simulations and post-layout simulations of the passive components are performed using Sonnet and ADS.

The amplifier adopts a two-stage architecture: the first stage employs a cascode configuration with a transformer-based noise-reduction matching network to enhance performance, and input matching adopts coupled inductance to reduce the area; the second stage incorporates a current-reuse cascode design to achieve both high gain and low power consumption.

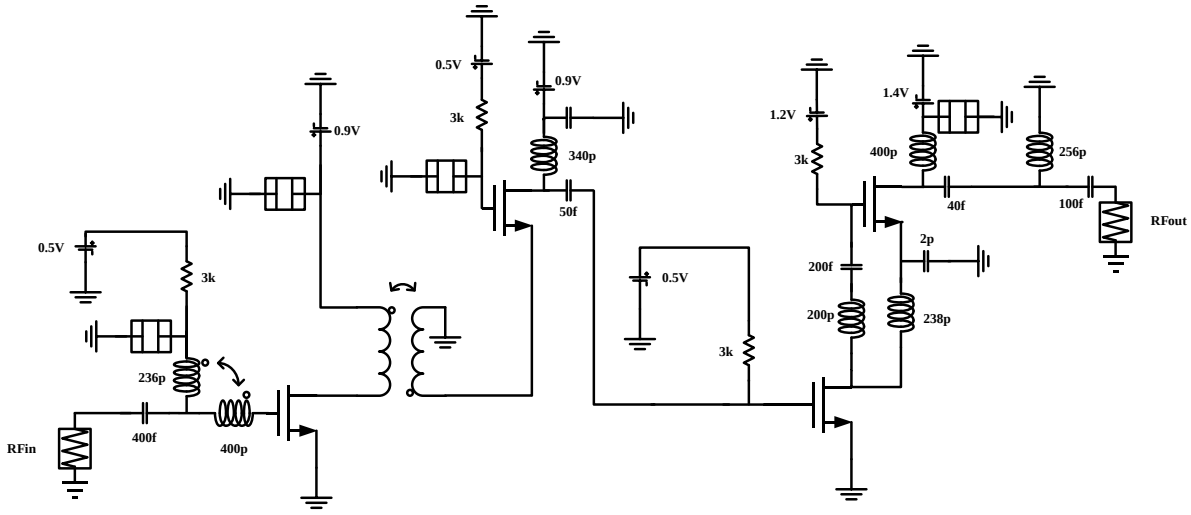

Fig. 3.28 Schematic of proposed LNA

All active device models in the entire circuit are based on the 90 nm small-signal and large-signal models provided by TSMC. The passive components, such as inductors, transformers, and matching networks at each stage, are optimized using Sonnet

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electromagnetic simulation software, and post-layout simulations are performed in ADS and Specter RF to ensure the accuracy of simulation results.

3.3.2 Simulation Results

Fig. 3.29 presents the simulated S-parameters, showing that the maximum small-signal gain reaches 15.7 dB at 43 GHz, with a 3-dB bandwidth spanning from 27.3 to 46.6 GHz. The simulated noise figure is shown in Fig. 3.30, with a minimum value of 4.1 dB at 42 GHz.

Fig. 3.31, Fig. 3.32, and Fig. 3.31 illustrate the relationship between gain, output power, and input power at 30, 37, and 44 GHz, respectively. The simulated input 1-dB compression point is -19 dBm.

The input third-order intercept points performance of the proposed LNA was evaluated at 30, 37, and 44 GHz, as illustrated in Fig. 3.34, Fig. 3.35, and Fig. 3.36, respectively. The simulated IIP_3 are -8 dBm at 30 GHz, -4 dBm at 37 GHz, and -8 dBm at 44 GHz, indicating a consistent linearity response across the operational bandwidth.

Stability analysis is crucial for preventing circuit oscillations. As shown in Fig. 3.37, when the stability factor K is greater than 1, the two-port network meets the necessary and sufficient condition for unconditional stability. Additionally, inter-stage coupling effects may lead to potential instability issues. Therefore, the inter-stage stability mapping loops are examined, as shown in Fig. 3.38. The simulation results indicate that there is no overlap between the mapped circles, ensuring that the circuit is stable.

Finally, the total chip layout area is 0.51 mm^2, as shown in Fig. 3.39, including DC pads, RF pads, and the frame.

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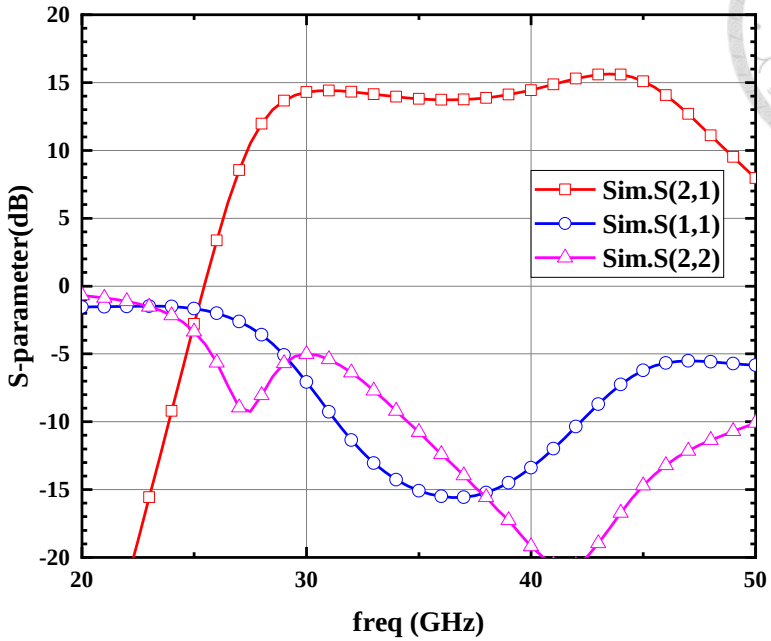

Fig. 3.29 The simulated S-parameters of the proposed LNA

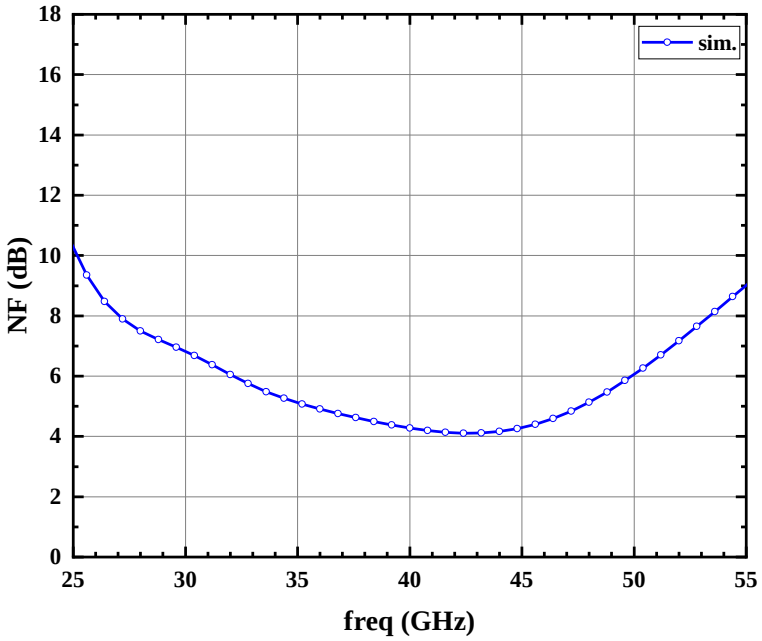

Fig. 3.30 The simulated noise figure of the proposed LNA

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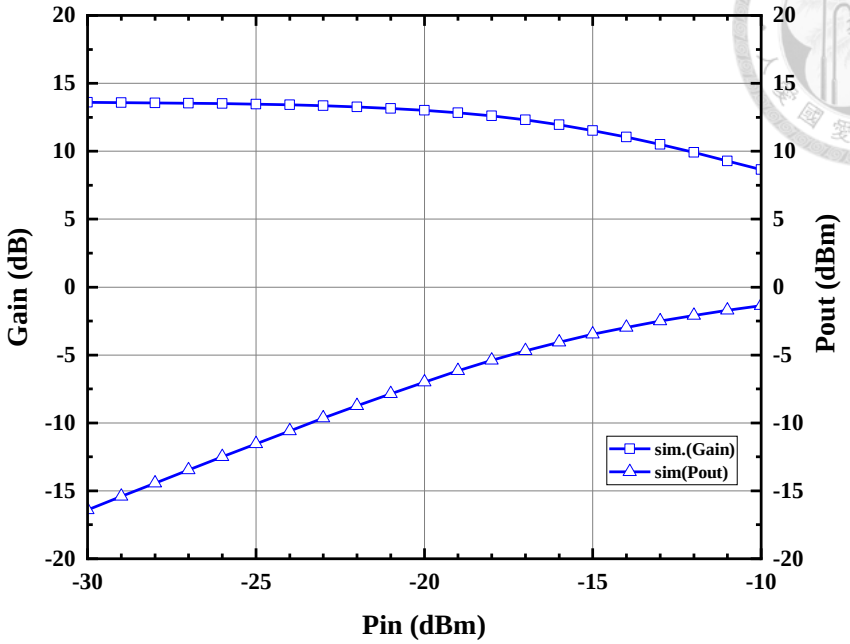

Fig. 3.31 Simulation of IP_{1dB} @ 30 GHz versus input power.

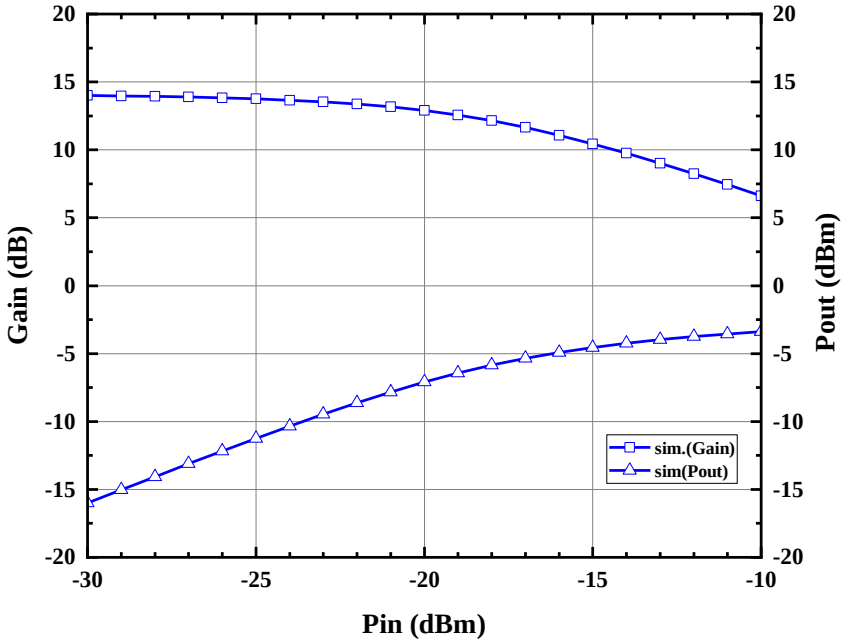

Fig. 3.32 Simulation of IP_{1dB} @ 37 GHz versus input power.

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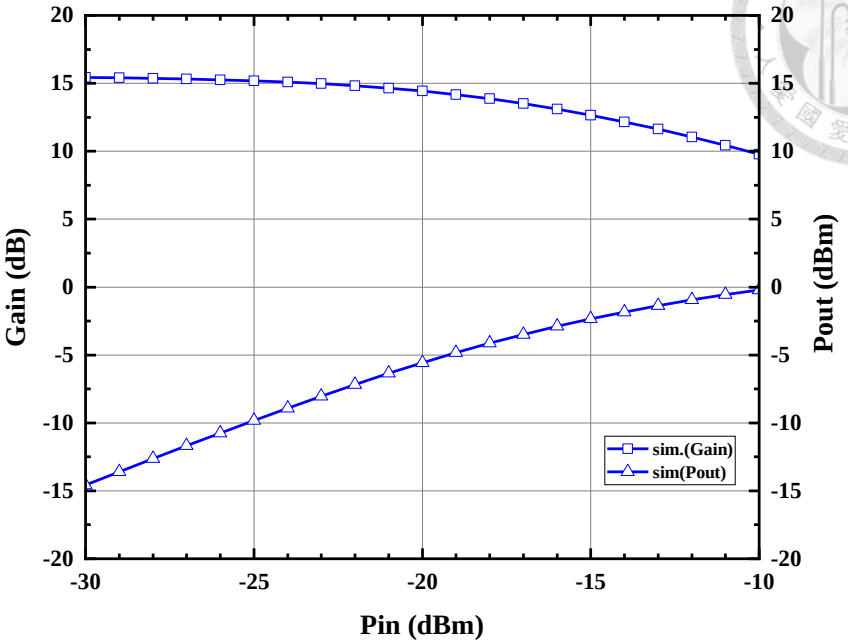

Fig. 3.33 Simulation of IP_{1dB} @ 44 GHz versus input power.

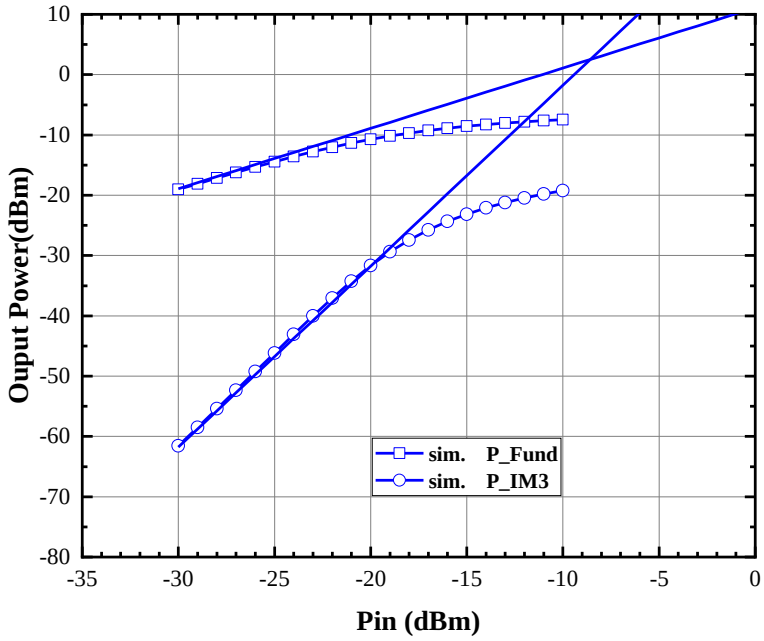

Fig. 3.34 The simulated IM_3 versus input power at 30 GHz.

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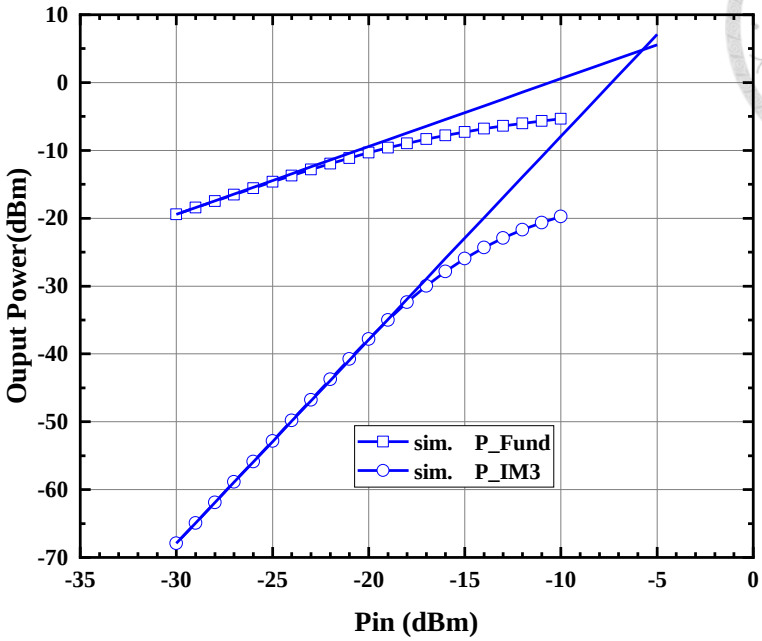

Fig. 3.35 The simulated IM_3 versus input power at 37 GHz.

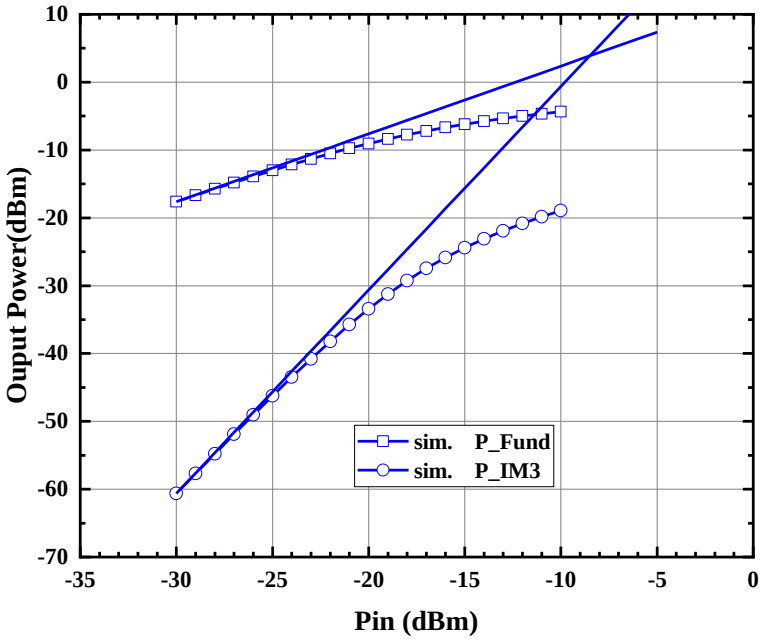

Fig. 3.36 The simulated IM_3 versus input power at 44 GHz.

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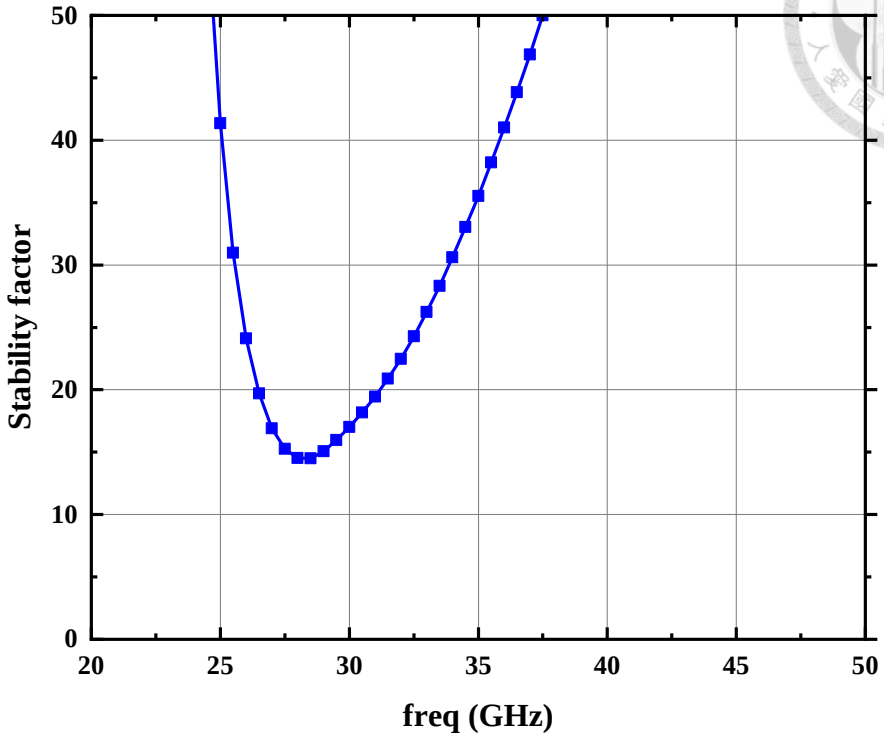

Fig. 3.37 Simulated stability factor

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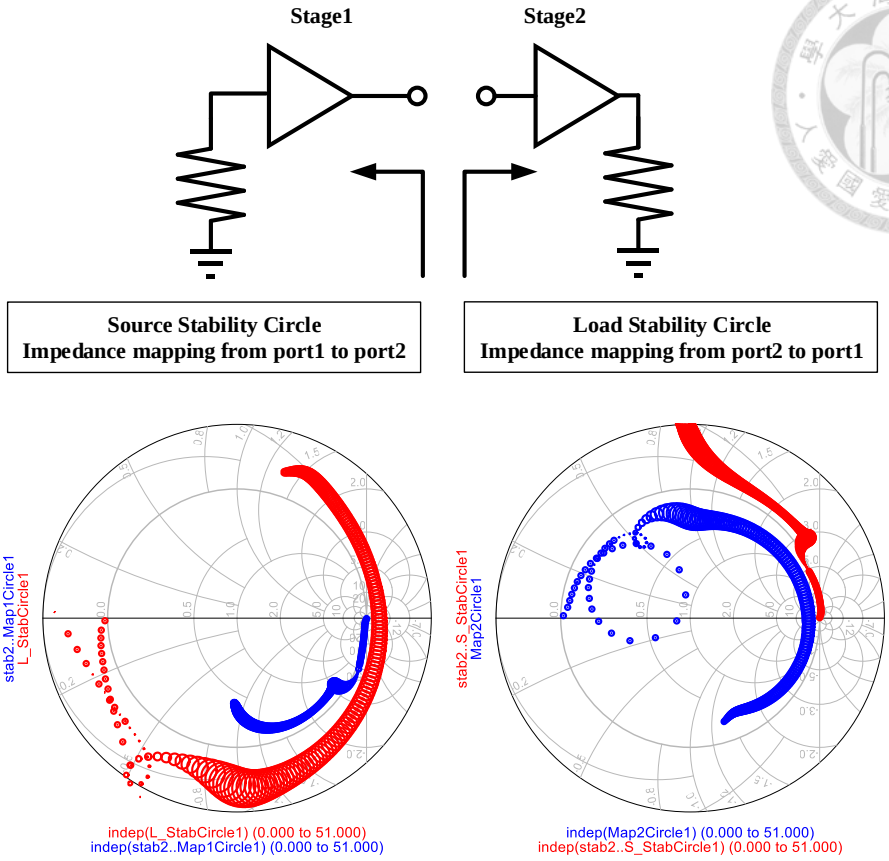

Fig. 3.38 Simulation of inter-stage stability

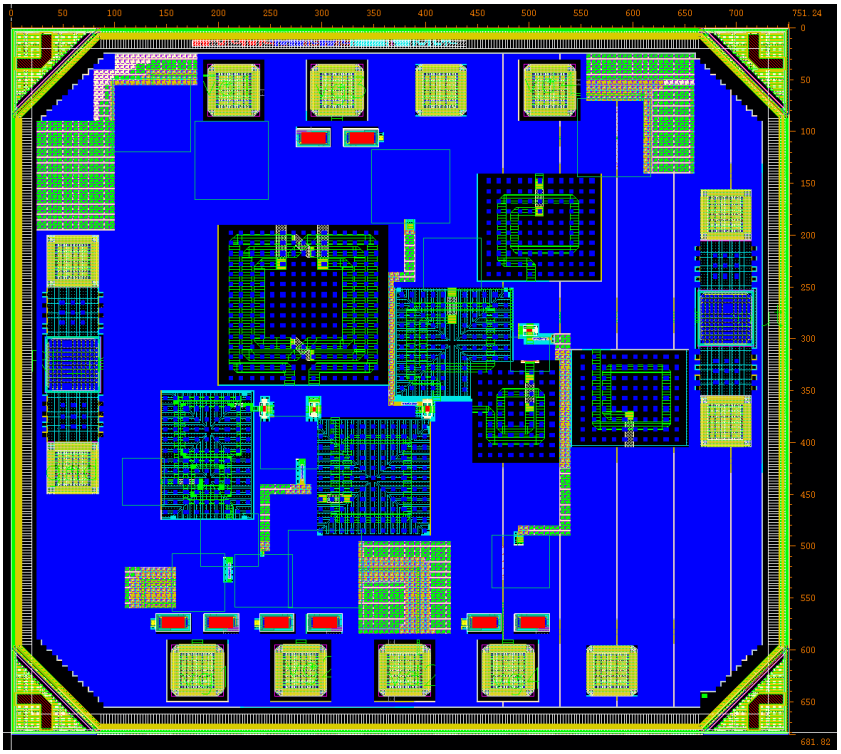

Fig. 3.39 Chip layout for the proposed LNA

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3.4 Measurement Result and Discussion

3.4.1 Measurement Result

The target Q-band low noise amplifier was fabricated using a 90-nm CMOS process. The chip microphotograph is shown in Fig. 3.40, and the total chip area, including the pads, is 0.51 mm². Measurements were conducted under drain bias voltages of 0.9 V and 1.4 V. The circuit exhibits a total DC power consumption of 7.8 mW, with the DC bias supplied to the chip through wire-bonding from the PCB. For enhanced supply stability, off-chip 2-μF bypass capacitors were soldered to each V_d line. RF characteristics were directly measured using GSG probes connected to the RF pads.

The S-parameters were measured using a Keysight E8361A vector network analyzer (VNA), with an output power level of approximately −30 dBm. Fig. 3.41 presents both the measured and simulated S-parameters, demonstrating a 3-dB bandwidth from 36 to 47 GHz and a maximum gain of 15.7 dB at 46.6 GHz.

The noise figure was measured using an Agilent N9041B UXA signal analyzer. Fig. 3.42 shows the simulated and measured noise figure results, where the minimum noise figure of 3.3 dB is achieved at 42 GHz. Within the 3-dB bandwidth, the noise figure remains below 5 dB.

Large-signal continuous-wave power measurements were performed using an E8257D signal generator and an Agilent E4448A spectrum analyzer. Fig. 3.44 and Fig. 3.45 illustrate the measured large-signal performance, indicating that IP_{1dB} is higher than −20 dBm. Fig. 3.46 and Fig. 3.47 show the IM_3 measurement results, demonstrating that the third-order intermodulation products are all greater than −10 dBm.

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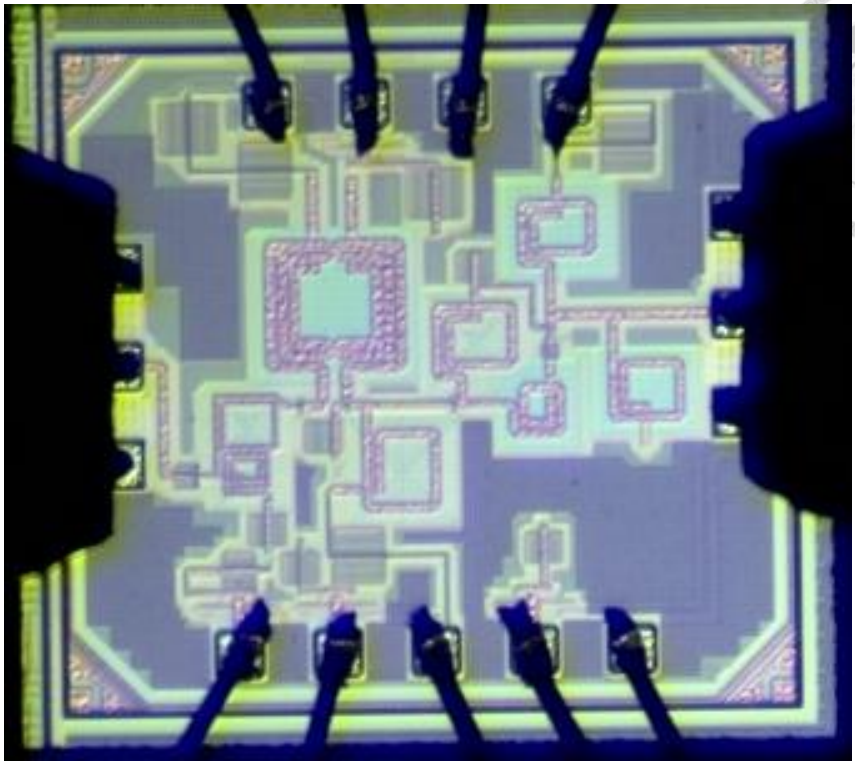

Fig. 3.40 Chip photo. The total size is 0.51 mm².

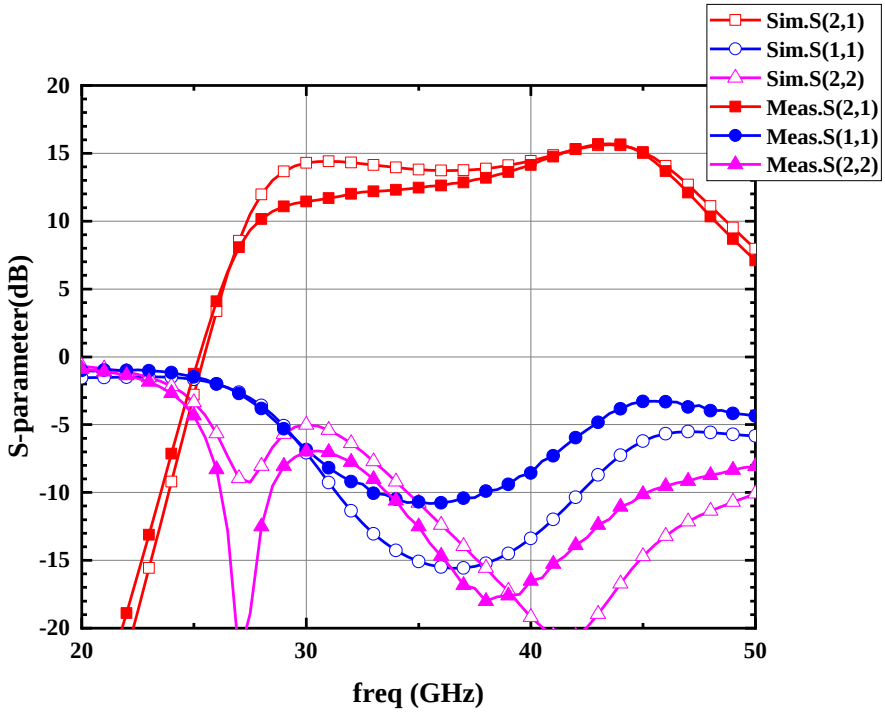

Fig. 3.41 Measured and simulated S-parameters.

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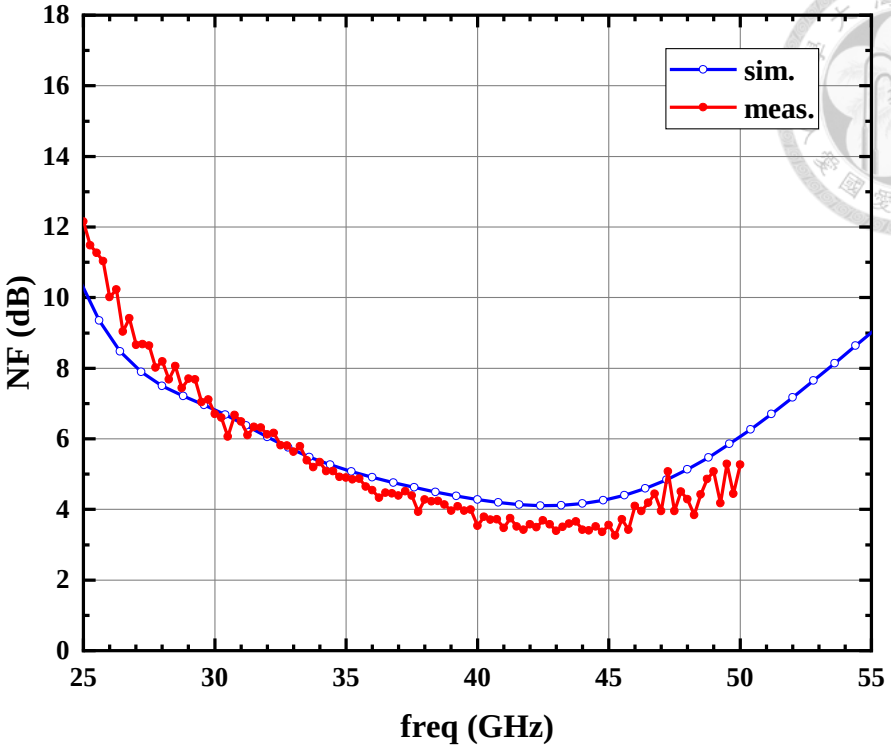

Fig. 3.42 Measured and simulated noise figure.

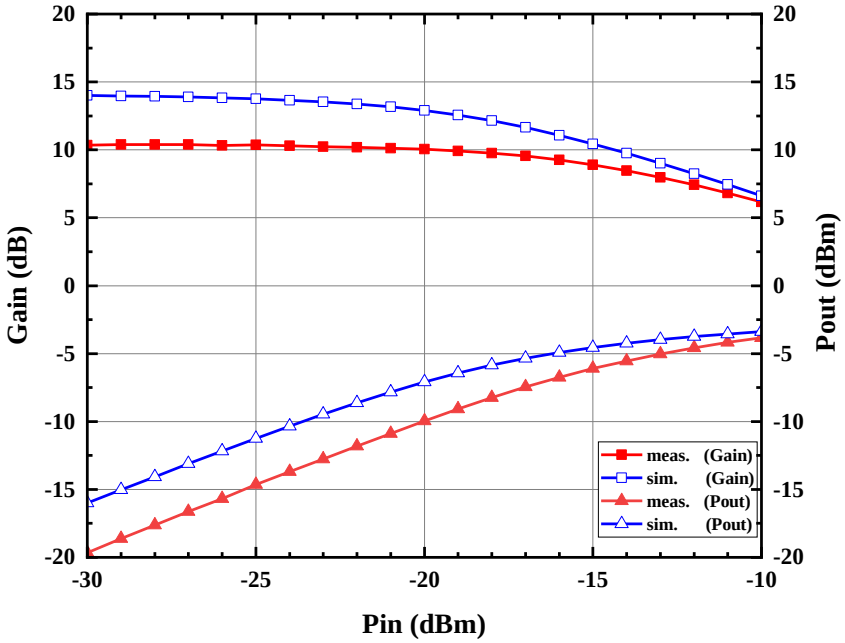

Fig. 3.43 Measured and simulated IP_{1dB} versus input power at 30 GHz.

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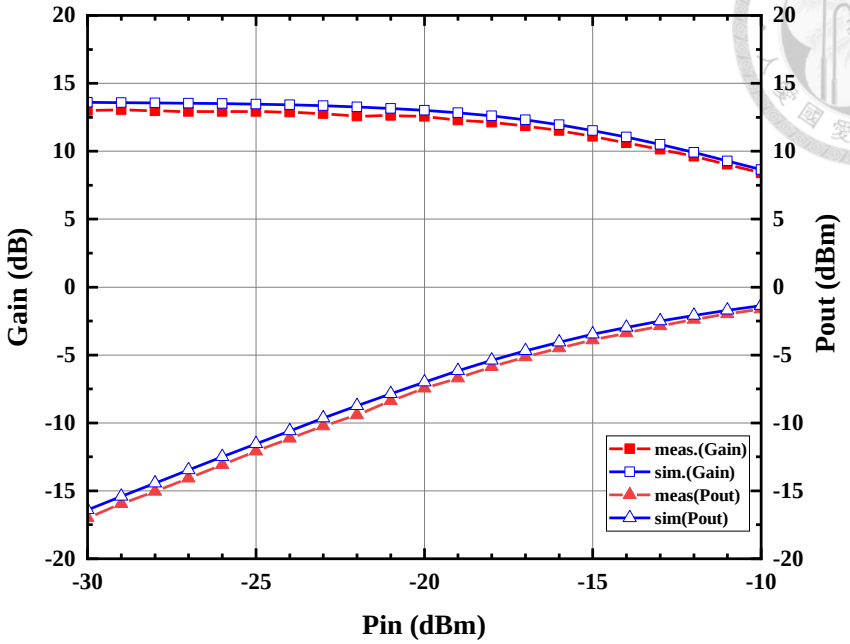

Fig. 3.44 Measured and simulated IP_{1dB} versus input power at 37 GHz.

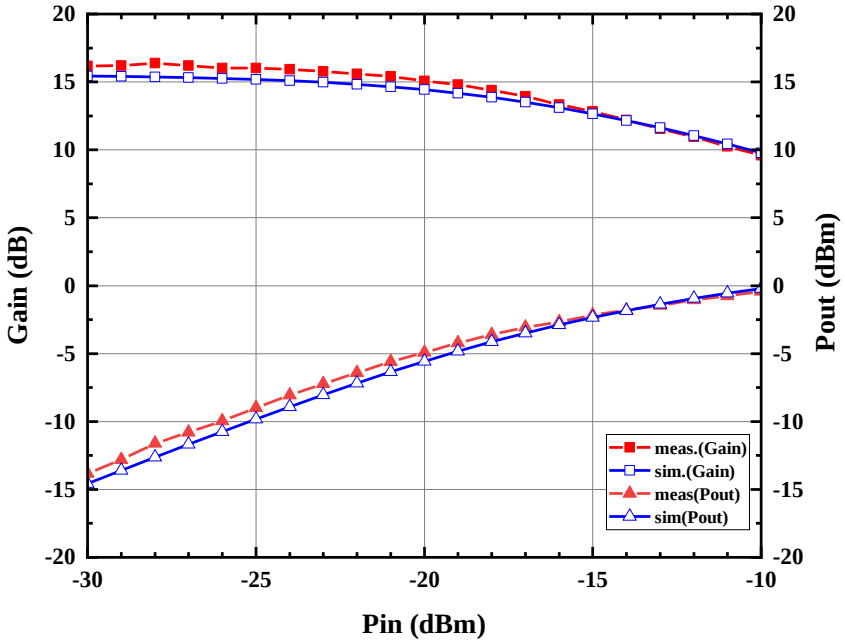

Fig. 3.45 Measured and simulated IP_{1dB} versus input power at 44 GHz.

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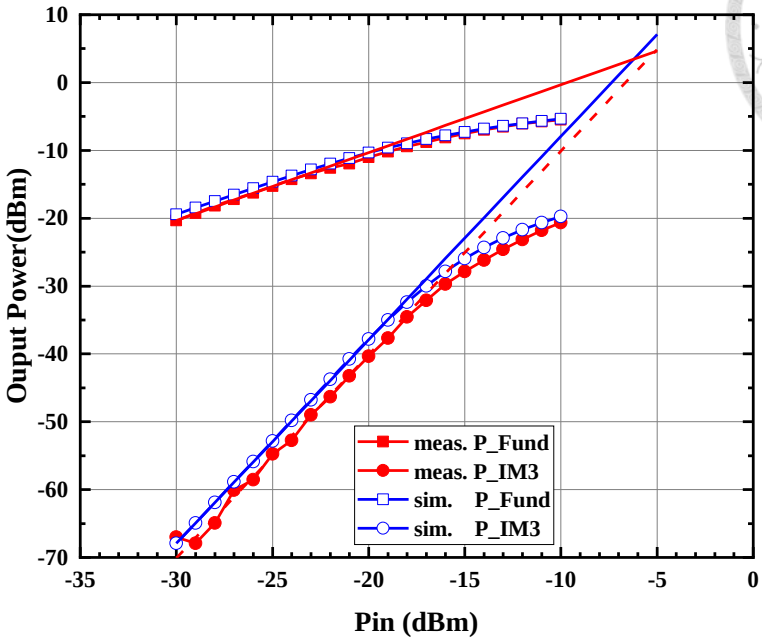

Fig. 3.46 Measured and simulated IM_3 versus input power at 37 GHz

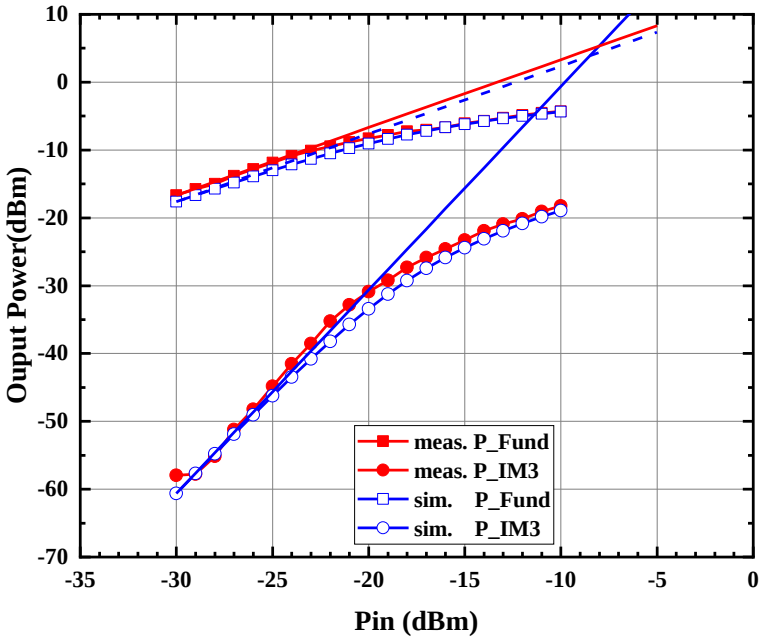

Fig. 3.47 Measured and simulated IM_3 versus input power at 44 GHz

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3.4.2 Discussion

The experimental results reveal an inconsistency between the measurement and simulation, where the measured small-signal gain is about 3 dB lower than the simulated value at 30 GHz. The primary cause is attributed to process variation in the capacitors used in the output matching network. The output matching capacitors are implemented using a metal–oxide–metal (MOM) structure between the M_9 and M_7 metal layers, where M_9 is an ultra-thick metal and M_8 is a thick metal. The capacitance value of MOM capacitors is dependent on the metal linewidth, spacing, and surrounding metal environment like dummy metal, which makes their process variation typically greater than that of metal–insulator–metal (MIM) capacitors.

In this design, the output matching network adopts a second-order LC topology, with all capacitors realized in MOM structures, with the transmission line and MOM width of 10 μm. Insufficient dummy metal filling in the surrounding layout may lead to capacitance deviations, causing the impedance matching to differ from the intended design. The original 40 fF and 70 fF capacitors were re-simulated with a −10% capacitance deviation. As shown in Fig. 3.48, the modified simulation results exhibit a frequency response more consistent with the measured S-parameters. Similarly, the large-signal simulation at 30 GHz in Fig. 3.49 shows that the adjusted response aligns more closely with the measurements. In contrast, the difference in the noise figure depicted in Fig. 3.50 between the re-simulation and the original is not significant, confirming that the first stage effectively suppresses the noise contribution from subsequent stages.

In summary, when capacitors are employed in critical matching networks, the layout should ensure adequate and uniform dummy metal filling and follow metal density rules. To avoid the use of small capacitance, transformer-based matching can be considered for the impedance transformation.

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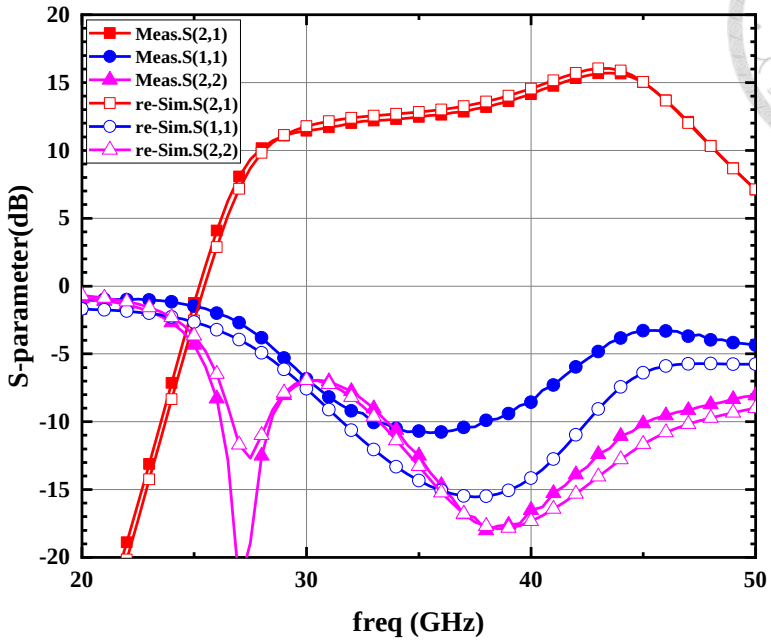

Fig. 3.48 Measured and re-simulated results of S-parameters

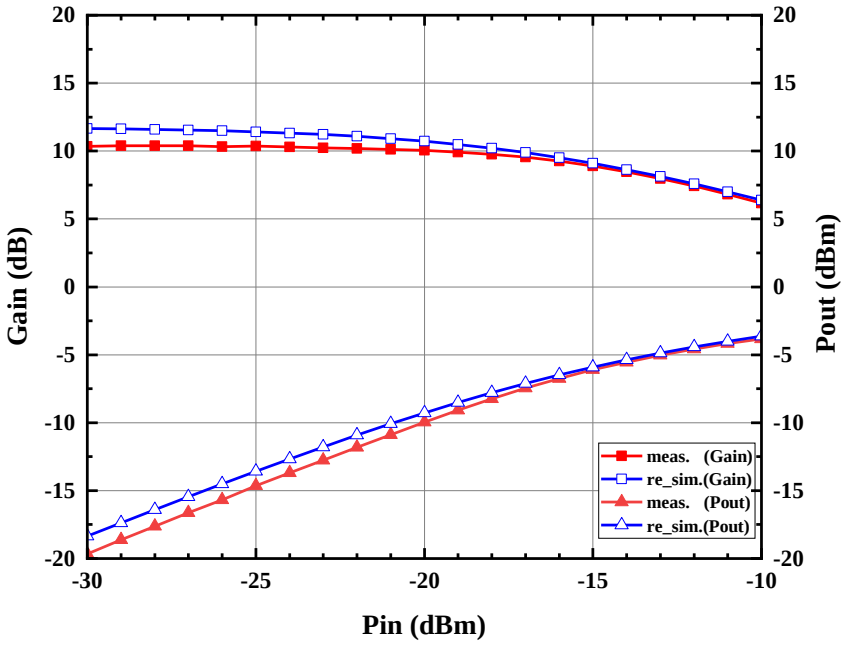

Fig. 3.49 Measured and re-simulated IP_{1dB} versus input power at 30 GHz

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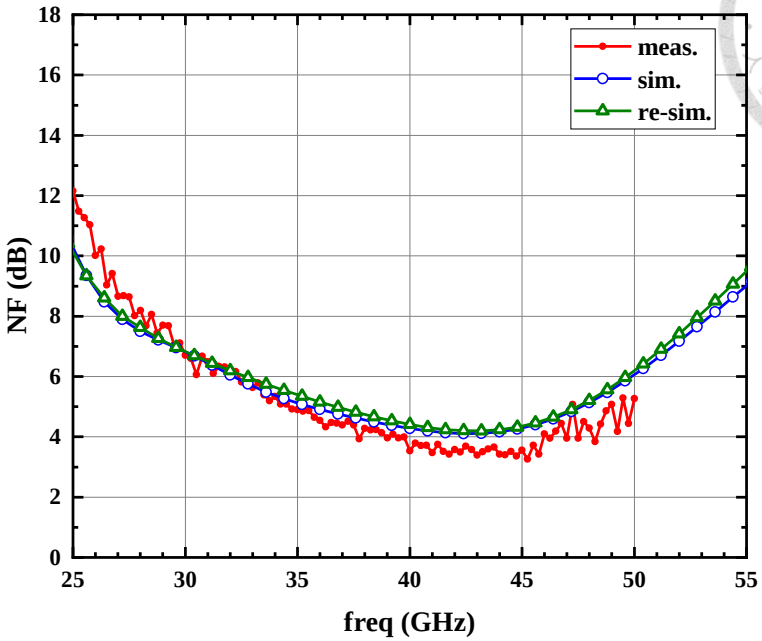

Fig. 3.50 Measured and re-simulated noise figure.

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3.5 Summary

A two-stage low noise amplifier operating from 36.6 to 46.6 GHz was designed and implemented using TSMC 90-nm CMOS technology. The proposed LNA employs a transformer-coupled cascode topology in the first stage to suppress noise contribution from subsequent stages, while the second stage utilizes a current-reused architecture to enhance gain, thus achieving high gain and low noise performance across a wide frequency range. The LNA exhibits a DC power consumption of 7.8 mW, a peak small-signal gain of 15.7 dB, and a 3-dB bandwidth spanning from 36.6 to 46.6 GHz. Furthermore, a minimum noise figure of 3.3 dB and an average NF of 3.8 dB are achieved. Table 2.6 summarizes the performance of recently published Q-band CMOS LNAs, where the figure-of-merit (FoM) [46] is adopted for performance evaluation, which is based on gain-bandwidth product, noise figure, and DC power consumption. The FoM [50] is expressed as follows:

$$FOM_1 = \frac{S_{21,\mathrm{Mag}} \times Bandwidth\ [GHz]}{(NF_{\mathrm{Mag}}-1)\times P_{\mathrm{dc}}[mW]} \tag{3.8}$$

$$FOM_2 = \frac{S_{21,\mathrm{Mag}} \times Bandwidth\ [GHz]\times IP_{1dB}}{(NF_{\mathrm{Mag}}-1)\times P_{\mathrm{dc}}[mW]} \tag{3.9}$$

Here, S_{21} denotes the peak small-signal gain, and NF_{min} represents the minimum noise figure. Compared to previously reported LNAs, the proposed LNA achieves a competitive FoM, demonstrating that the selected architecture provides an excellent trade-off among gain, noise, and power efficiency. These results indicate that this design achieves a competitive balance and outstanding performance under the adopted topology.

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Table 3.2 Summary of previously published Q-band LNA

REF.	Process	BW (GHz)	Gain (dB)	NF (dB)	P_{dc} (mW)	IP_{1dB} (dBm)	Area (mm^2)	FoM_1	FoM_2
IMS'2012[26]	90-nm CMOS	29-44	13.8	3.8	18	-12.1	0.48	2.9	0.5
IMS'2012[30]	90-nm CMOS	38.6-41.7	10.6	5.4	0.92	N/A	0.19	4.6	N/A
TMTT'2011[24]	90-nm CMOS	34-46	20.3	4.6	15	-17.8	0.21	6	0.6
MWTL'2023[23]	90-nm CMOS	25.5-51.5	20.5	4.2	10.1	-25	0.6	16.7	0.9
APMC'2018[34]	90-nm CMOS	34.7-39.2	18.9	6.7	15.6	-20	0.2	0.95	0.1
RFIC' 2023[25]	65-nm CMOS	32-46	21.5	2.2	22	-17.6	0.16	9.7	2.2
RFIC' 2021[31]	28-nm CMOS	22.2-43	21.1	3.5	22.3	N/A	0.22	8.5	N/A
MWCL'2017[32]	65-nm CMOS	15.8-30.3	10.2	3.3	12.4	N/A	0.18	3.3	N/A
APMC' 2023[29]	180nm CMOS	36-42	15.3	7.3	73	-12.3	0.56	0.1	0.02
T-CASII'2018[33]	28-nm CMOS	30.6-35.3	18.6	4.9	9.7	N/A	0.23	2.0	N/A
This work	90-nm CMOS	36.6-46.6	15.7	3.3	7.8	-19	0.51 (core 0.15)	6.9	0.77

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Chapter 4 Conclusions

This thesis presents the design and implementation of two millimeter-wave circuit components. The first component is a D-band low-noise amplifier fabricated using a 65-nm CMOS process. By employing the Gmax core technique, this LNA achieves a high gain and low noise performance, with a small-signal gain of 22 dB and a gain exceeding 15 dB across the 130–145 GHz frequency range. The minimum noise figure is 8.2 dB, and the DC power consumption is 17.8 mW. The redesigned circuit, also employing a three-stage Gmax-core topology, achieves a peak gain of 18.7 dB with a 27-GHz 3-dB bandwidth from 128 to 155 GHz, a minimum noise figure of 4.8 dB with 5.8 dB average under the same power consumption. This LNA is suitable for 140-GHz transceiver systems, astronomical applications, and terahertz imaging.

The second component is a Q-band low-noise amplifier designed in a 90-nm CMOS process. To fulfill the requirements of low noise figure and wide bandwidth, a transformer-coupled cascode topology is adopted in the first stage, while a current-reused architecture is employed in the second stage. The proposed LNA exhibits a DC power consumption of 7.8 mW, a peak small-signal gain of 15.7 dB, and a 3-dB bandwidth from 36 GHz to 46 GHz. The minimum noise figure is 3.3 dB, with an average noise figure of 3.8 dB across the entire bandwidth. The results demonstrate the competitiveness of CMOS technology, indicating its suitability for 5G mobile communication and radio astronomy applications.

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