國立臺灣大學電機資訊學院光電工程學研究所

博士論文

Graduate Institute of Photonics and Optoelectronics

College of Electrical Engineering and Computer Science

National Taiwan University

Doctoral Dissertation

超高靈敏度熱感測元件之設計與製造：基於發光電晶體於智慧科技應用

Design and Fabrication of Ultra-High Sensitivity Thermal Sensing Devices Using Light-Emitting Transistors for Smart Technologies

薩莫古

Mukul Kumar

指導教授：吳肇欣 博士

Advisor: Prof. Chao-Hsin Wu, Ph.D.

中華民國 114 年 1 月

January, 2025

doi:10.6342/NTU202500212

Certificate of Thesis/Dissertation Approval from the

Oral Defense Committee

國立臺灣大學博士學位論文

口試委員會審定書

DOCTORAL DISSERTATION ACCEPTANCE CERTIFICATE
NATIONAL TAIWAN UNIVERSITY

超高靈敏度熱感測元件之設計與製造：基於發光電晶體於智慧科技應用

Design and Fabrication of Ultra-High Sensitivity Thermal Sensing Devices Using Light-Emitting Transistors for Smart Technologies

本論文係薩莫古君（學號 D09941011）在國立臺灣大學光電工程學研究所完成之博士學位論文，於民國 114 年 1 月 6 日承下列考試委員審查通過及口試及格，特此證明

The undersigned, appointed by the Graduate Institute of Photonics and Optoelectronics, on 6 January 2025 have examined a Doctoral Dissertation entitled above presented by MUKUL KUMAR (student ID: D09941011) candidate and hereby certify that it is worthy of acceptance.

口試委員 Oral examination committee:

（指導教授 Advisor）

吳肇欣　林浩雄　陳雯惠

林泰源　黃建璋　吳育任

張書維

所長 Director: 吳育任

doi:10.6342/NTU202500212

Acknowledgements

This Ph.D. dissertation was completed under the guidance of **Prof. Chao-Hsin Wu (吳肇欣)** at the Integrated Optoelectronics Device Lab (IOED), Graduate Institute of Photonics and Optoelectronics (GIPO), National Taiwan University (NTU), Taipei, Taiwan. My time at NTU was an exceptional academic experience, and I feel fortunate to have worked under Prof. Wu's research mentorship. It has been a matter of great pride and privilege to be a part of his research environment. I believe I must have earned some good karma to have Prof. Wu with me always and support me not only academically but also personally. His unwavering support, motivation, and advice have been instrumental in shaping my professional and personal growth during my Ph.D. journey. I always respect Prof. Chao-Hsin Wu from the bottom of my heart and I am trying to be like him. I hope during my Ph.D. work, I earn his trust.

I would like to extend my sincere gratitude to **Prof. Chu-Hsuan Lin**, Department of Opto-Electronics Engineering, National Dong Hwa University (NDHU), Taiwan. Heartfelt thanks to Prof. Lin, encourage me to come to Taiwan for higher study through the TEEP. Prof. Lin's guidance and support played a pivotal role in helping me gain admission to NTU and begin this incredible journey.

doi:10.6342/NTU202500212

I am deeply thankful to the esteemed members of my Ph.D. dissertation committee: **Prof. Yuh-Renn Wu** (Director of GIPO, NTU), **Prof. I-Chun Cheng** (Deputy Director of GIPO, NTU), **Prof. Jian-Jang Huang** (GIPO, NTU), **Prof. Hao-Hsiung Lin** (Department of Electrical Engineering, NTU), **Prof. Tsung-Hsien Lin** (Department of Electrical Engineering, NTU), and **Prof. Shu-Wei Chang** (Research Center for Applied Sciences, Academia Sinica, Taiwan). I am honored to have their esteemed presence at my Ph.D. dissertation, scheduled on January 6, 2025. Their valuable feedback and insights have greatly enriched this research and contributed to its refinement.

A special thanks to **Prof. Shu-Wei Chang**, who provided continuous guidance, even during the challenges of the COVID-19 pandemic. His feedback on my analytical modeling work significantly deepened my understanding of device physics. I am also grateful to **Prof. Yuh-Renn Wu** for his impactful course on “Semiconductor Optics” and his expertise in device simulations, which motivated me to examine every parameter meticulously. My heartfelt thanks go to **Prof. Lon A. Wang** (GIPO, NTU) for encouraging me to apply for a summer internship at TSMC, Taiwan. The industrial experience was invaluable in helping me shape my career goals and understand the differences between academic and industrial research.

doi:10.6342/NTU202500212

I extend my gratitude to the **OIA**, the **International Admissions Department**, the **Finance Section**, **GIPO**, and the **College of Electrical Engineering and Computer Science** at NTU for their unwavering support and scholarships. Their assistance ensured that I could pursue my studies in Taipei, despite its high cost of living.

Special thanks to the cleanroom staff and team members who maintained an excellent fabrication environment. I am especially grateful to **Mr. Po-Yen Tseng** and **Mr. Lu-Ching Hsueh** for their help in device fabrication, and to **Ms. Yun-Hsuan Chang**, **Dr. Hao-Tien Cheng**, **Dr. Lucas Yang**, **Mr. Yun-Cheng Yang**, **Mr. Te-Hua Liu**, **Mr. Chee Keong Yee**, and **Ms. Yu-Han Huang** for their assistance with device characterization and insightful discussions. Thanks to the entire IOED lab family and **Ms. Jessie Chen** for supporting me with official documentation and administrative processes.

A heartfelt acknowledgment to **Mr. Hou-Ju Chen** and his wife, **Ms. Jing-Yi Huang**, whose kindness and support made me feel like part of their family. I am truly grateful and wish them happiness and success. I am also deeply indebted to my senior and friend, **Dr. Kuntal Barman**, for motivating and guiding me during my Ph.D. journey. Thanks to the **National Science and Technology Council (NSTC)**, Taiwan, for funding my research and travel grants, which allowed me to present my work at international conferences such as DRC 2024 in the USA and CSW 2023 in South Korea.

doi:10.6342/NTU202500212

My gratitude extends to countless individuals who supported me throughout my Ph.D. journey, both professionally and personally. While I cannot name everyone, their contributions are etched in my heart.

I owe everything to my family. My grandfather, the **late Shri Uma Shankar Prasad**, my grandmother, **Mrs. Nirmala Devi**, my parents, **Mr. Saroj Kumar** and **Mrs. Munni Devi**, my younger brother **Mr. Rajat Kumar**, and my sister **Mrs. Pooja Kumari,** have always stood by me, supporting me emotionally and financially. Coming from a middle-class background, sending me abroad for my studies was a monumental sacrifice, and I sincerely hope I have made them proud.

Lastly, a special thanks to my beautiful wife, **Mrs. Jyoti Priya**, who married me during the third year of my Ph.D. Her unwavering faith in me, even without a secure job at the time, is a testament to her love and trust. She has been my pillar of strength, sacrificing her comfort to support me in every possible way. Her encouragement pushed me to write more research papers and stay focused on my goals. I am forever grateful for her care.

Finally, I extend my heartfelt thanks to the **Taiwan Government** for their support, which made it possible for me to study and fulfill my dreams at NTU. **Taiwan** will always hold a special place in my heart as a country of innovation and kindness.

doi:10.6342/NTU202500212

Dedicated to the Universe: A Source of Infinite Inspiration

doi:10.6342/NTU202500212

Abstract (Chinese)

本論文全面研究了光發射晶體管 (Light-Emitting Transistors, LETs) 的設計、製造、開發與優化, 作為下一代智慧熱感測技術的先進裝置。基於 III-V 族化合物半導體的 LETs 作為創新且高速的三端口裝置, 集光學與電子功能於單一元件內。透過先進的量子阱 (Quantum-Well, QW) 結構, LETs 展現出在高速光通訊、光電整合電路（Optoelectronic Integrated Circuits, OEICs）以及先進熱感測應用方面的卓越潛力, 特別是由於其量子阱的熱電子發射特性。通過系統性研究與創新的元件架構, 本論文證明了基於 LETs 的裝置在超高熱敏感度與下一代熱感測解決方案中的非凡潛力, 超越了傳統熱感測技術的熱敏感度限制。

本論文首先探討了使用 LETs 於智慧熱感測技術中的動機, 介紹了針對熱感測應用所設計與製造的單量子阱異質結雙極性電晶體(Single Quantum Well-Based Heterojunction Bipolar Transistors, SQW-HBTs)。初步研究強調了在 HBTs 基區內整合階梯式單量子阱 (SQW) 結構, 實現了在 25℃到 85℃溫度範圍內集電極電流提升 72.23%的顯著進步。此提升歸因於增強的熱電子發射動力學, 促進了電子從量子阱中的快速逃逸。與傳統 HBTs 的熱行為相反, 該進展得到基於熱電子發射理論的修正電荷控制模型的支持, 不僅解釋了觀察到的現象, 還促進了 QW-HBT 結構在熱感測應用中的優化設計。

doi:10.6342/NTU202500212

在這些研究基礎上,研究擴展至多量子阱（MQW）及三量子阱（TQW）HBTs,展示了熱敏感度的進一步提升。一種修正電荷控制模型被開發以考量量子阱參數（如數量與位置）對電流增益的影響。該模型經實驗結果驗證後，用於設計 TQW-HBTs, 其在相同溫度範圍內實現了集電極電流 200%的顯著增加, 以及每℃ 7 μA 的電流敏感度。這些見解建立了一個優化 MQW-HBT 及 TQW-HBT 配置以提升裝置熱性能的穩健框架, 用於下一代熱感測器。

儘管 MQWs 實現了顯著的熱敏感度增強, 但由於電子捕獲多重量子阱導致的電流減少, 提出了一個突破性的設計, 即將光發射晶體管級聯於達靈頓電晶體中。該創新達靈頓電晶體配置利用 LET 的熱電子發射機制實現了卓越的熱敏感度。LET 在操作溫度從 25℃上升到 85℃ 時集電極電流增加了 153%, 而達靈頓電晶體在相同偏壓和溫度條件下增加了 210%。此外， LET 的集電極電流對溫度信號比為 8.53 μA/℃, 而在達靈頓配置中此比率提升至 26.2 μA/℃, 展示了熱敏感度的顯著改善。此外, 輸出電壓的電壓對溫度信號敏感度達到 9.12 mV/℃, 超越了傳統熱感測器。

儘管取得了這些進步，本研究探討了解決實現線性電壓對溫度響應的挑戰，並提供了優化 QW 結構以平衡敏感度與線性的建議。本論文進一步詳細研究了 QW 寬度對熱性能的影響, 突顯了敏感度與線性之間的權衡。實驗與模擬研究揭示, 較窄的量子阱顯示出更高的熱敏感度, 而較寬的量子阱則確保了更好的線性度。最佳的量

doi:10.6342/NTU202500212

子阱寬度為 90 Å, 其在 100℃ 時實現了每 ℃ 1.34 mA 的熱敏感度與優異的線性度。這些發現為開發高性能熱感測器提供了關鍵見解。

最後, 本論文強調了包括 SQW-HBTs, MQW-HBTs 和 TQW-HBTs 在內的基於 LET 裝置在智慧熱感測應用中的變革潛力。本研究中報導的新穎配置, 例如與光發射晶體管級聯的達靈頓電晶體, 展現了超高的熱敏感度。這些進步為下一代智慧熱感測技術奠定了堅實的基礎, 提供了超高熱性能的前端元件。

關鍵字 – 光發射晶體管(LET), 量子阱(QW), 多量子阱(MQW), 三量子阱(TQW), 單量子阱異質結雙極性電晶體（SQW-HBT）, MQW-HBT、TQW-HBT, HBLET, 達靈頓電晶體, 修正電荷控制模型, 溫度相關電流增益, 熱電子發射, 高溫, 智慧熱感測器, 超高熱敏感度與線性度

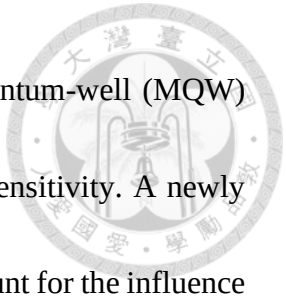
doi:10.6342/NTU202500212

Abstract (English)

This dissertation presents a comprehensive study on the design, fabrication, and optimization of Light-Emitting Transistors (LETs) as advanced devices for next-generation smart thermal sensing technologies. LETs, based on III-V compound semiconductors, emerge as innovative, high-speed three-port devices integrating optical and electronic functionalities. Leveraging state-of-the-art quantum-well (QW) structures, LETs demonstrate exceptional potential for high-speed optical communication, enhanced performance in optoelectronic integrated circuits (OEICs), and advanced thermal sensing applications, particularly due to their thermionic emission properties. These findings position LETs as strong candidates for next-generation smart thermal sensing technologies, surpassing traditional thermal sensor technologies in thermal sensitivity.

The study begins with the design and fabrication of single-quantum-well heterojunction bipolar transistors (SQW-HBTs), designed to enhance thermal sensitivity. The innovative incorporation of a staircase QW into the base region of HBTs achieved a 72.23% increase in collector current across a temperature range of 25℃ to 85℃, attributed to faster electron escape dynamics from the QW. A modified charge-control model incorporating thermionic emission theory effectively explains this behavior and provides a foundation for optimizing SQW-HBT structures for thermal sensing applications.

doi:10.6342/NTU202500212



Building on these initial results, the research advances to multi-quantum-well (MQW) and triple-quantum-well (TQW) HBTs to further improve thermal sensitivity. A newly modified charge-control model for MQW-HBTs is developed to account for the influence of quantum-well parameters, such as number and position, on the current gain. This model, validated against experimental results, guides the design of TQW-HBTs, which exhibit a remarkable 200% increase in collector current over the same temperature range and achieving a current sensitivity of 7 μA/℃. These findings highlight the potential of MQW-HBTs such as TQW-HBTs for applications requiring ultra-high thermal sensitivity.

To address the challenges of reduced current due to electron trapping in MQWs, the dissertation introduces a groundbreaking idea developed in the optoelectronics thermal technology by successful design and fabrication of the world's first Darlington transistor configuration cascaded with LETs. This innovative approach combines the thermionic emission properties of LETs with the amplification benefits of the Darlington design, achieving a 153% increase in LET collector current from 25℃ to 85℃ and a further enhancement to 210% in the Darlington configuration. The collector current-to-temperature sensitivity improves from 8.53 μA/℃ in LETs to 26.2 μA/℃ in the Darlington configuration, with a voltage-to-temperature sensitivity reaching 9.12 mV/℃ surpassing conventional thermal sensor. Despite these advancements, challenges in

doi:10.6342/NTU202500212

achieving linear voltage-to-temperature responses are addressed, with recommendations for optimizing QW structures to balance sensitivity and linearity.

Further investigations into the effect of QW width reveal critical trade-offs between thermal sensitivity and linearity. Narrower QWs exhibit higher sensitivity, while wider QWs improve linearity. An optimal QW width of 90 Å achieves a thermal sensitivity of 1.34 mA/℃ at 100℃ while maintaining excellent linearity, providing essential insights for designing high-performance thermal sensors. Finally, this dissertation work highlights the transformative potential of LET-based devices, including SQW-HBTs, MQW-HBTs, and TQW-HBTs, for smart thermal sensing applications. The novel configurations, such as the Darlington transistor cascaded with Light-emitting transistor, reported ultra-high thermal sensitivity in this studied. These advancements lay strong ultra-high-thermal performance front-end components for next-generation for smart thermal sensing technologies.

Key words – Light-emitting transistor (LET), quantum-well (QW), multiple-QW (MQW), triple-QW (TQW), single-QW-based heterojunction bipolar transistor (SQW-HBT), MQW-HBT, TQW-HBT, HBLET, Darlington transistor, modified charge-control model, temperature dependent current gain, thermionic emission, high temperature, smart thermal sensor, smart sensing technologies, ultra-high thermal sensitivity, and linearity

doi:10.6342/NTU202500212

Table of Contents

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

List of Figures

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

doi:10.6342/NTU202500212

List of Tables

doi:10.6342/NTU202500212

Chapter 1

Introduction to Light-Emitting Transistor for Smart Thermal Sensing Technology

1.1 Introduction

The rapid evolution of semiconductor technology has significantly influenced modern electronics, enabling the development of increasingly sophisticated devices that power industries ranging from computing and communications to healthcare. The invention of the transistor in 1947 marked a pivotal turning point, driving the miniaturization of electronic devices and laying the foundation for solid-state electronics. Over the decades, transistors have evolved from traditional bipolar junction transistors (BJTs) to heterojunction bipolar transistors (HBTs), culminating in the breakthrough development of light-emitting transistors (LETs), which integrate optical and electrical functions within a single device.

As the demand for more efficient, accurate, and compact temperature sensors grows, particularly in optoelectronic integrated circuits (OEICs), innovative thermal sensing technologies have become essential. LETs, with their unique characteristics, have emerged as a promising solution for next-generation smart thermal sensors, offering

doi:10.6342/NTU202500212

exceptional sensitivity, integration capabilities, and performance in optical communication systems and sensor technologies.

This chapter introduces LETs as advanced devices for smart thermal sensing applications, setting the stage for a deeper exploration of their potential in future optoelectronic systems. This chapter begins with Subchapter 1.2, “Era of Transistor to Light-Emitting Transistors,” provides a historical perspective on the evolution of transistor technologies, outlining the transition from traditional transistors to the emergence of LETs. This background establishes the technological foundation necessary to understand how LETs have evolved to meet the demands of modern thermal sensing systems.

Following this, Subchapter 1.3, “Applications of Light-Emitting Transistors,” discusses the diverse and expanding range of applications for LETs, highlighting their role in optical communication, integrated circuits, and, notably, their key position in next-generation thermal sensing technologies. The insights from this subchapter naturally lead to Subchapter 1.4, “Traditional Temperature Sensor Devices,” where we analyze the limitations of conventional temperature sensing technologies. By comparing traditional sensors to LET-based sensors, we highlight the need for innovative solutions, positioning LETs as superior alternatives.

doi:10.6342/NTU202500212

Subchapter 1.5, “Thermal Sensing Mechanism of QW-Based HBTs,” builds on the insights from Subchapter 1.4 by exploring the advanced thermal sensing mechanisms of quantum-well-based heterojunction bipolar transistors (QW-HBTs). These devices, which leverage quantum well (QW) structures to enhance temperature sensitivity, represent a significant advancement in smart thermal sensor technology. This subchapter connects directly to the design and operation of LETs, demonstrating how QW-HBTs are essential components in the development of high-performance thermal sensors.

Finally, Subchapter 1.6, “Thesis Organization,” outlines the structure of this thesis, presenting the research objectives and the flow of the chapters. Each chapter builds upon the previous one, providing a comprehensive understanding of the design, fabrication, and application of LET-based thermal sensing technologies. The thesis concludes by presenting the potential of LETs in shaping the future of smart thermal sensing and optoelectronic systems.

Lastly, this chapter provides an overview of the historical development of transistors, the emergence of LETs, and their applications in OEICs and thermal sensing, laying the groundwork for a detailed discussion on LET-based smart thermal sensor design in the chapters that follow.

doi:10.6342/NTU202500212

1.2 Era of Transistor to Light-Emitting Transistors

The advent of the electronic age began when semiconductor (or "solid-state") devices started replacing bulky and unreliable vacuum tubes. This era was marked by the invention of the first point-contact triode transistor by John Bardeen and Walter H. Brattain in 1947, a significant breakthrough in the development of the original bipolar triode devices [1]. Since then, semiconductors have become the foundation of modern technology, playing a critical role in computing, communication, transportation, entertainment, and medicine. The invention of the transistor in 1947 laid the groundwork for the electronic technologies that enhance our smart lives today.

Following this revolutionary development, William Shockley introduced the concept of minority carrier injection in 1949 [2], and in 1951, the first BJT was demonstrated [3]. In his 1948 patent application, Shockley proposed the use of materials with a wider energy bandgap for the emitter of a BJT to enhance transistor performance through improved minority carrier injection efficiency [4]. This idea was further advanced by Herbert Kroemer in 1957 when he proposed the HBT, utilizing a wider bandgap material for the emitter to suppress hole injection from the base to the emitter in an n-p-n transistor [5]. This marked the transition from homojunction to heterojunction devices, significantly enhancing performance by allowing higher current gains while maintaining low base resistivity.

doi:10.6342/NTU202500212

The HBT structure offered several advantages over traditional BJTs. In a BJT, the n-p-n junction is formed using different dopant concentrations, with the emitter heavily doped to increase electron concentration and improve emitter injection efficiency, while the base is lightly doped to minimize hole back-injection. However, this also leads to increased base-emitter junction capacitance, increased base resistance, and then need for a thicker base, potentially causing bandgap shrinkage and performance degradation. In contrast, the HBT's lightly doped emitter reduces junction capacitance, while its heavily doped base lowers resistivity, allowing for a thinner base and faster transit times. These improvements enable HBT to operate at frequencies in the hundreds of gigahertz range. Advancements in material growth technologies, such as Metal Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE), have enabled the development of modern high-speed HBTs with extremely thin base layers, only tens of nanometers thick. These devices exhibit ultrafast transit times, with carriers crossing the base within femtoseconds, significantly improving their speed and performance [6], [7].

Carrier recombination in semiconductor devices, particularly in the base of HBTs, is a key process that influences transistor operation. Traditionally, base recombination is viewed as an undesirable effect, dissipating energy as heat. However, when applied to light-emitting devices, radiative recombination becomes a crucial mechanism for photon generation. The first observation of coherent light emission from a semiconductor was

doi:10.6342/NTU202500212

achieved in 1962, when diode lasers (DLs) were demonstrated by Robert N. Hall and Holonyak, marking a milestone in optoelectronics [8], [9].

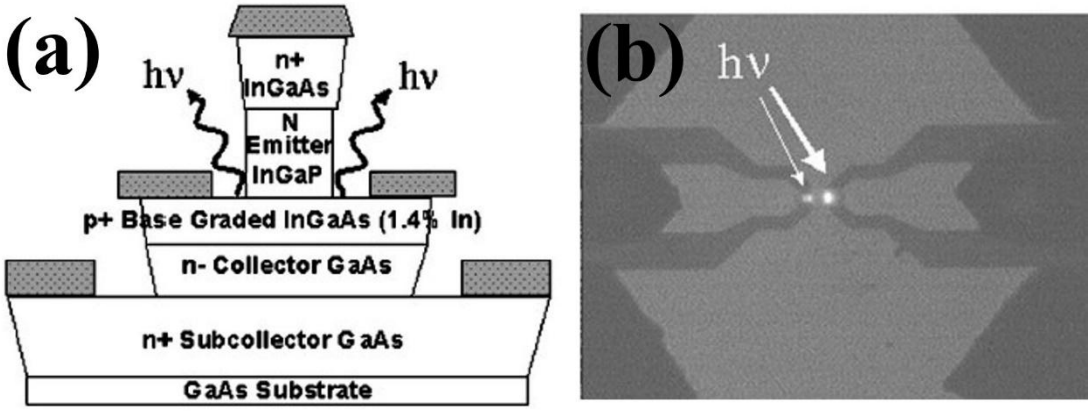


Fig. 1.1: (a) Epitaxial layer structure of the III-V InGaP/GaAs HBT; (b) Top view of light emission from the base of the first light-emitting transistor (LET) based on the HBT layer structure under forward active operation, captured by a silicon CCD [10].

In 2004, a groundbreaking development occurred when Milton Feng and Nick Holonyak, Jr. observed radiative recombination in the base of III-V InGaP/GaAs HBTs, marking the first instance of light emission from a transistor (see **Fig. 1.1(a)** for the epitaxial layer structure) [10]. This observation suggested that HBTs could function as light-emitting sources. This discovery marked the birth of the LETs, a new class of device of both electrical and optical output (see **Fig. 1.1(b)** for the observed light emission from the HBT). Building on this breakthrough, Feng and his team introduced a new class of device by incorporating QWs into the base region of HBTs to enhance radiative recombination, leading to the development of QW-HBTs, or quantum-well heterojunction bipolar light-emitting transistors (QW-HBLETs), or more commonly, the LET [11]. This innovation

doi:10.6342/NTU202500212

introduced a novel class of devices capable of functioning as both high-speed transistors and light sources, offering simultaneous electrical and optical outputs, enabling high-speed optical modulation and opening new possibilities for OEICs [12]. The energy band diagram of this QW-based HBT is shown in **Fig. 1.2(a)**, with **Fig. 1.2(b)** illustrating light emission from the QW-HBT under forward active bias.

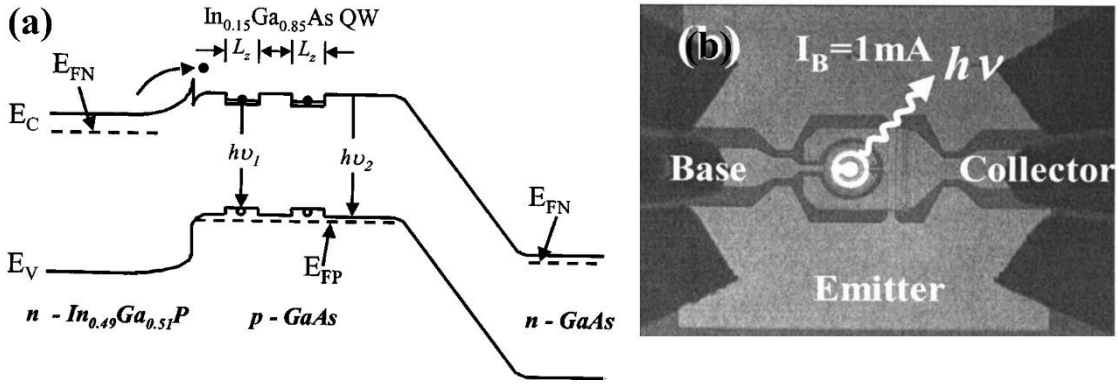
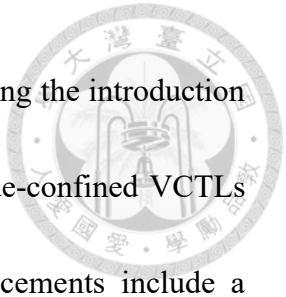


Fig. 1.2: (a) Energy band diagram of the first QW-based HBT with two InGaAs QWs inserted into the base to enhance radiative recombination by capturing more electrons; (b) Top view of light emission from the first QW-HBT in the common emitter configuration, with the device biased in forward active mode and a base current, I_b, of 1 mA [11].

Unlike traditional DLs, where carriers are confined within the QW active region, LETs benefit from the tilted charge distribution in the base and the electric field sweeping carriers from the base to the collector, significantly reducing recombination lifetimes compared to DLs [13]. This results in ultrafast modulation speeds, enabling LETs to achieve modulation frequencies as high as 4.3 GHz [14]. By integrating optical cavities and confining layers, these devices can also be transformed into transistor lasers (TLs), further enhancing their performance as light-emitting sources [15].

doi:10.6342/NTU202500212



The development of TLs has achieved significant milestones, including the introduction of vertical cavity transistor lasers (VCTLs) in 2012 [16], with oxide-confined VCTLs demonstrating bandwidths exceeding 11 GHz [17]. Recent advancements include a tunneling junction LET achieving 12 GHz bandwidth [18]. These innovations position LETs and TLs as promising candidates for OEICs and next-generation high-speed optical communication systems, offering a combination of high speed, low power consumption, and dual electrical-optical outputs.

Today, III-V compound semiconductors, with their superior radiative recombination efficiencies, have paved the way for efficient TLs and LETs, which hold great potential for the future of optoelectronic technologies.

1.3 Applications of Light-Emitting Transistors

Over the last decade, society has become increasingly dependent on internet connectivity and electronic devices for a smart, interconnected lifestyle. The demand for data bandwidth has grown exponentially, driven by applications like high-performance computing, video streaming, cloud computing, and social media. According to CISCO's predictions, nearly two-thirds of the global population will have Internet access by 2023 [19]. The total number of internet users is expected to rise to 5.3 billion (66% of the global population) by 2023, up from 3.9 billion (51%) in 2018. This marks a compound annual growth rate (CAGR) of 6%. **Fig. 1.3** illustrates this projected growth from CISCO’s

doi:10.6342/NTU202500212

Annual Internet Report for 2018-2023.

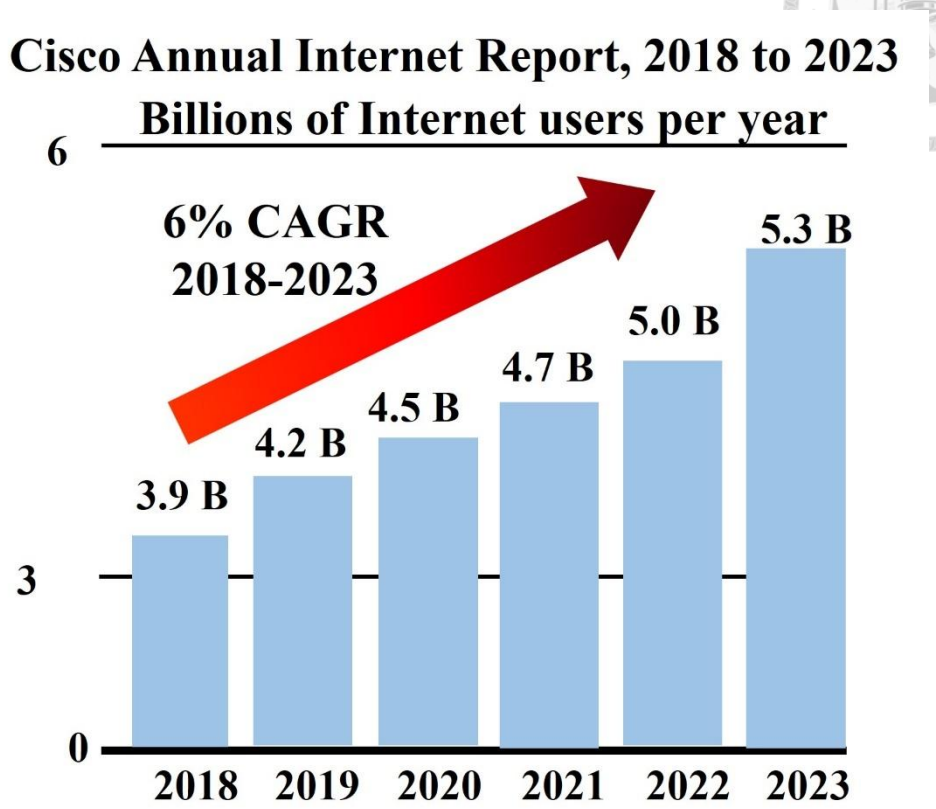


Fig. 1.3: Global internet user growth prediction according to the Cisco Annual Internet Report (2018-2013) white paper [19].

By 2024, the total volume of global data is projected to reach around 147 zettabytes, rising from 120 zettabytes in 2023. This increase is being fueled by rising internet usage, social media, and the proliferation of the Internet of Things (IoT). By 2025, this number is anticipated to soar to 181 zettabytes. The rapid expansion of unstructured data, such as videos and social media content, has contributed significantly to this growth. The challenge now is no longer about generating data but ensuring fast and reliable delivery of such vast quantities.

The development of optical transceiver and receiver systems is key to addressing this

doi:10.6342/NTU202500212

challenge. Optical communication, particularly through fiber optics, has replaced traditional wired connections over long distances and within data centers. It is even on the brink of reaching residential use, providing the necessary speed and reliability for data transmission. Optical interconnects (OIs), which use photons instead of electrons, offer several advantages, particularly for long-distance and high-bandwidth transmission.

In this era of optical communication, LETs and TLs present themselves as promising light transmitters, modulators, and photodetectors due to their dual outputs—both electrical and optical. They facilitate electrical-to-optical (E-to-O) and optical-to-electrical (O-to-E) conversions, making them strong candidates for the development of OEICs and high-speed optical communication systems.

At our Integrated Optoelectronic Device (IOED) Lab at NTU, under the guidance of Prof. Chao-Hsin Wu and in collaboration with Prof. Milton Feng's team at UIUC, we have consistently explored the potential of LETs and TLs for optical logic gate designs [20], [21], [22], [23], [24], [25], [26] and high optical modulation bandwidth [14], [18]. Although LETs and TLs have shown great promise, further modifications to the layer structure are required to fully compete with advanced semiconductor DLs, especially the oxide-confined VCSELs.

Currently, LETs and TLs demonstrate three main applications: 1) optical logic gate designs, 2) high optical modulation bandwidth, and 3) thermal sensor technology for

doi:10.6342/NTU202500212

OEIC development, as shown in **Fig. 1.4**.

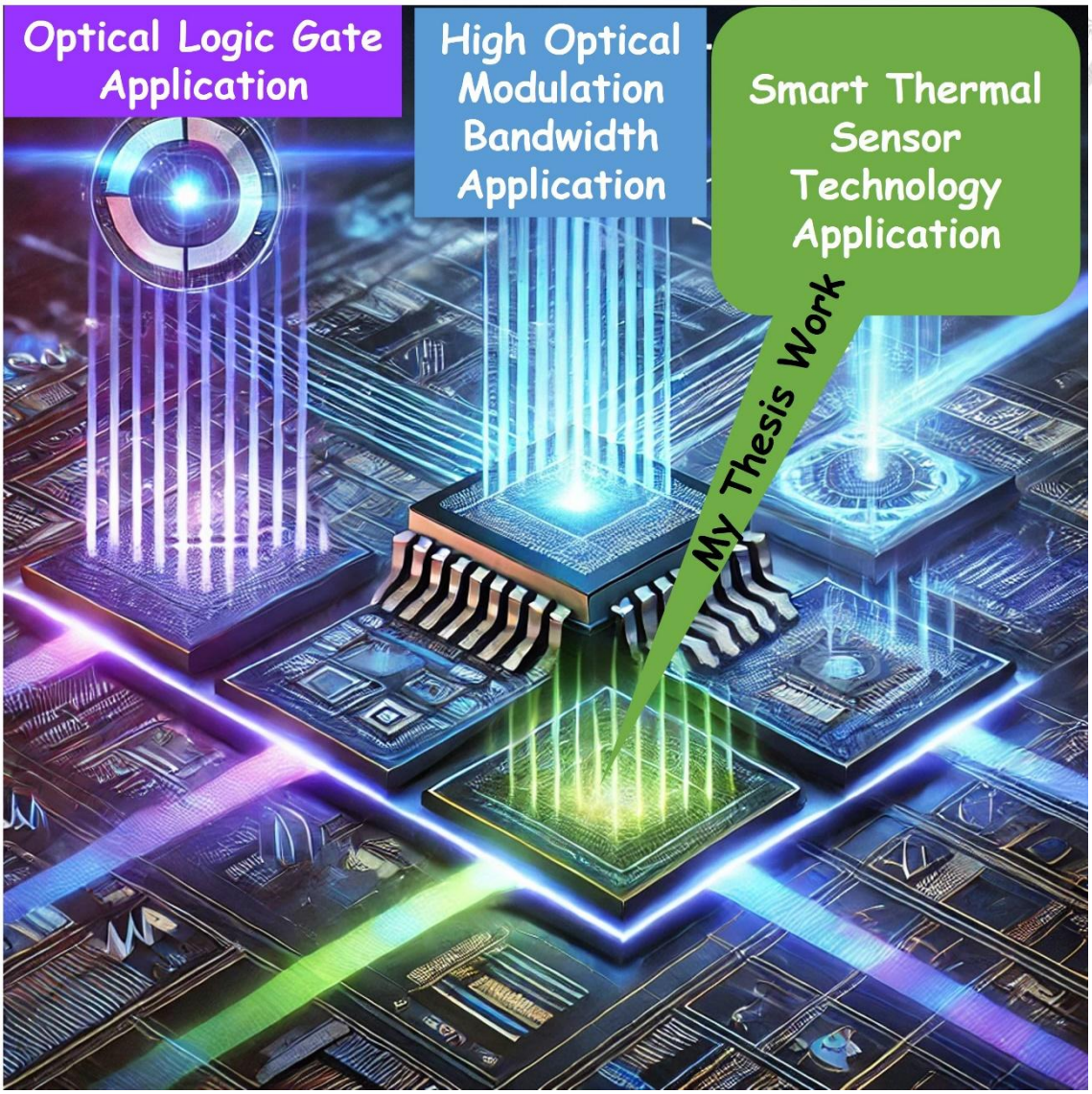


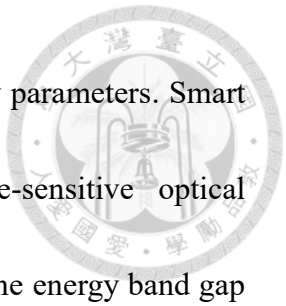
Fig. 1.4: Current applications of LETs and TLs include 1) optical logic gates, 2) high optical modulation bandwidth, and 3) smart thermal sensor applications (my thesis work). LETs and TLs are potential candidates for the development of OEICs.

In my current research, I focus on the application of LETs for next-generation smart thermal sensing technology, utilizing the thermionic emission effects in the QWs.

1.4 Traditional Temperature Sensor Devices

Accurate temperature measurement is essential for the reliable operation of OEICs,

doi:10.6342/NTU202500212



where thermal sensing enables control of both operational and safety parameters. Smart thermal sensing systems achieve this by utilizing temperature-sensitive optical parameters (TSOPs), which depend on the temperature variation of the energy band gap [27], or through temperature-dependent electrical characteristics [28]. Temperature sensors are commonly applied in instrumentation, measurement, and control systems. Traditional temperature sensors, such as platinum resistance thermometers, are renowned for their precision but are often bulky and costly [29]. In contrast, semiconductor-based temperature sensors developed using modern complementary metal-oxide semiconductor (CMOS) technology offer cost-effectiveness and easier to integrate with control units [30], [31], [32], [33].

With the increasing integration density and power demands of modern very-large-scale integration (VLSI) circuits, temperature sensors play a critical role in on-chip thermal and power management to prevent performance limitations and potential functional failures. On-chip sensors enable real-time temperature monitoring, facilitating effective thermal management. Typically, a smart on-chip temperature sensor includes a sensor front-end that generates temperature-dependent signals (e.g., voltage, current, time, or frequency) and a signal-to-digital converter (SDC) that converts these signals into digital output. **Figure 1.5** illustrates the basic block diagram of a smart thermal sensor. **Table 1.1** provides a overview of different temperature sensor types, including their sensing

doi:10.6342/NTU202500212

principle, advantages, and disadvantages.

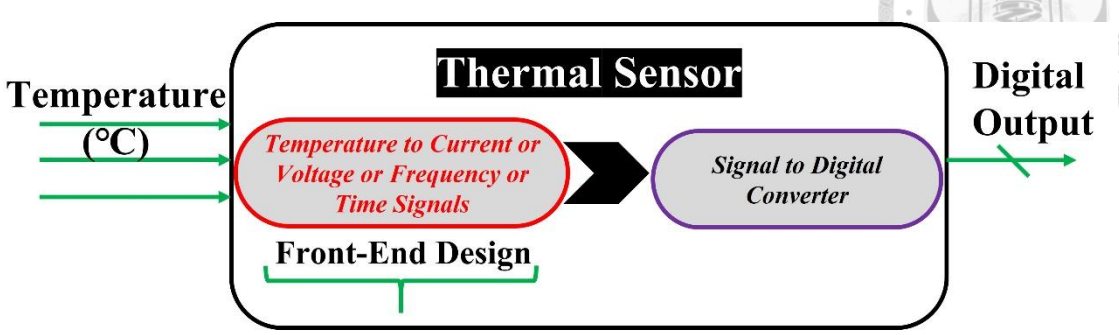


Fig. 1.5: Block diagram of typical integrated thermal sensor.

Bandgap-based sensors are among the most precise and reliable on-chip temperature sensor technologies due to their high linearity and minimal process variation sensitivity [34], [35], [36], [37], [38]. These sensors use BJTs, Schottky diodes, or metal-oxide-semiconductor field-effect transistors (MOSFETs) to produce well-defined voltage or current outputs proportional to temperature [39]. The architecture typically includes a sensor front-end generating PTAT (proportional to absolute temperature) voltage and a reference voltage, coupled with an analog-to-digital converter (ADC) to digitize these outputs, as illustrated in **Fig. 1.6.** Most contemporary designs favor the bandgap configuration due to its high-resolution ADCs and reliable digital outputs. The bandgap circuit, which supplies both PTAT and reference signals, has been a staple design for decades.

Figure 1.7 (a) depicts a traditional bandgap reference circuit utilizing PNP BJTs, where the current mirror transistors M_1 and M_2 are identical, and BJTs T_1 and T_2 have a size

doi:10.6342/NTU202500212

ratio of N. This configuration ensures a consistent current density ratio between the BJTs, with the base-to-emitter voltage difference (ΔV_{BE}) producing a PTAT voltage that is highly linear and relatively insensitive to process variations.

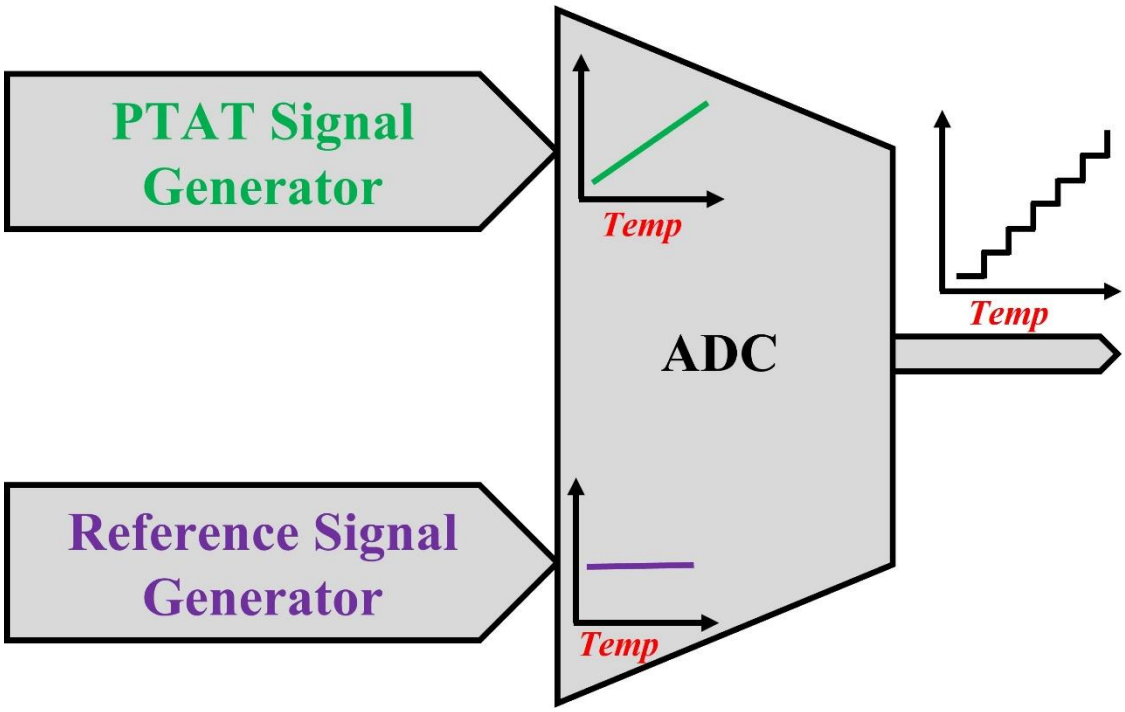


Fig. 1.6: Block diagram of a typical bandgap-based thermal sensor.

When BJT-based designs are used, achieving consistent operation across temperature ranges requires careful calibration due to process variations that affect the reference voltage. The V_{BE}, or base-emitter voltage, of a BJT diode is known to be Complementary to Absolute Temperature (CTAT) and can be combined with the PTAT signal to produce a stable reference voltage. While a reference voltage of approximately 1.25 V, known as the "bandgap reference," is effective, it is not ideally constant over a broad temperature range, often requiring one-or two-point curvature correction techniques to reduce sensing

doi:10.6342/NTU202500212

errors.

Table 1.1: Comparison of Traditional Existing Temperature Sensors.

Temperature Sensor Type	Sensing Principle	Advantage	Disadvantage	Ref.
Pulse-to-Digital Sensors	Utilizes a temperature-to-pulse generator (special inverter) to create a pulse width proportional to absolute temperature (PTAT), with pulse fed into a cyclic time-to-digital converter (TDC) for digital output.	Simple implementation using pure digital circuits, occupying less area.	High-cost calibration due to wide digital circuitry spread; sensitive to supply fluctuations and clock frequency variations.	[40]
Oscillator-Based Sensors	Measures the oscillation frequency of a ring oscillator, which is temperature-dependent. Oscillator output is buffered, and clock edges are counted digitally.	Operates at low supply voltage.	Highly sensitive to supply voltage and process variations, resulting in poor supply sensitivity and accuracy; requires linearity correction.	[41]
Thermal-Diffusivity-Based Sensors	Utilizes the IC substrate's thermal diffusivity with an electrothermal filter (ETF) that converts phase shift to digital.	High accuracy, minimal process sensitivity	Large front-end size, prone to self-heating and thermal noise, high power consumption.	[42]
Bandgap-Based Sensors	Generates PTAT and reference voltage, digitized by an ADC for temperature reading.	High linearity, low process sensitivity, commonly used	Requires one- or two-point calibration to minimize process spread errors; limited supply voltage scaling with modern CMOS technology.	[43]

doi:10.6342/NTU202500212

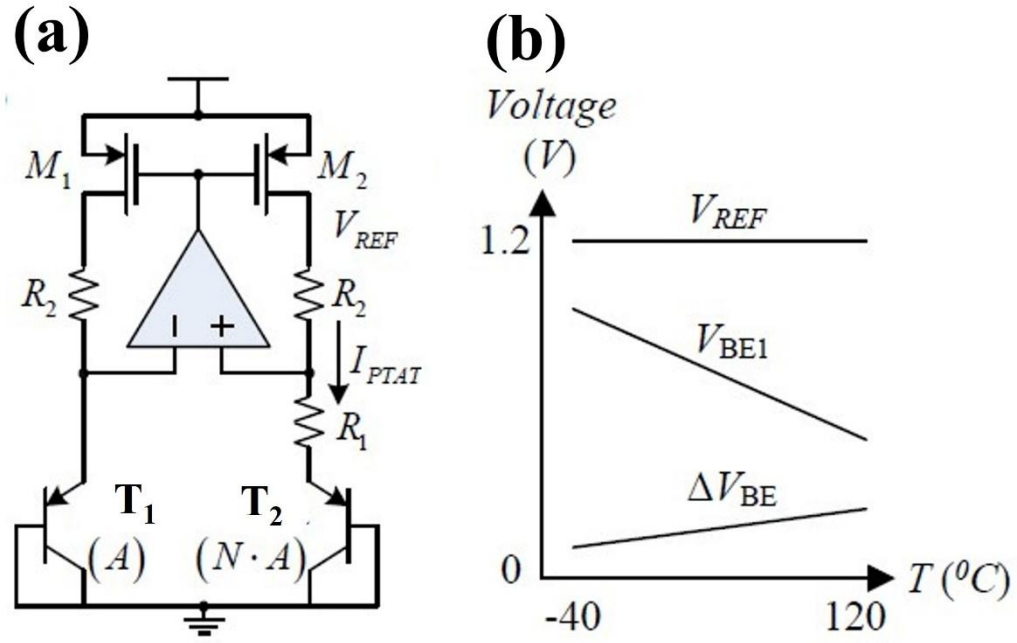


Fig. 1.7: (a) Schematic of a bandgap reference circuit. (b) Illustration of how the reference voltage is derived by combining PTAT and CTCT signals [43].

For accurate temperature sensor applications, where the V_{BE} exceeds tens of microvolts, the current-voltage (I-V) relationship of the BJT diodes can be expressed as:

$$I_{C_1} = A_1 I_S \exp\left(\frac{V_{BE_1}}{\eta V_T}\right) \tag{1.1}$$

$$I_{C_2} = A_2 I_S \exp\left(\frac{V_{BE_2}}{\eta V_T}\right) \tag{1.2}$$

Where I_{C_1} and I_{C_2} are the collector currents, A_1 and A_2 are the BJT areas, I_S is the saturation current (process-dependent), η is the non-ideality factor (typically around 1), and V_T is thermal voltage (kT/q), where k s Boltzmann's constant, T is the absolute temperature, and q is the electron charge.

The operational amplifier within the feedback loop equalizes voltages at points A and B,

doi:10.6342/NTU202500212

ensuring that the voltage across resistor R_1, defined as the difference the two base-emitter voltages (V_{BE_1} and V_{BE_2}), can be expressed as:

$$\Delta V_{BE} = V_{BE_1} - V_{BE_2} \tag{1.3}$$

With Eqs. (1.1) and (1.2), ΔV_{BE} can be written as:

$$\Delta V_{BE} = \eta V_T ln\left(\frac{I_{C_1}}{I_{C_2}}\frac{A_2}{A_1}\right) = \eta\frac{kT}{q}ln(N) \tag{1.4}$$

With further derivations, the bandgap-based temperature sensor front-end can be designed with flexibility, allowing adaptation for specific applications.

However, traditional BJT-based sensors require higher supply voltages, which may not be compatible with low-voltage applications and scaled CMOS processes. To achieve a lower, scalable supply voltage, MOSFETs operating in the subthreshold region are increasingly replacing BJTs in bandgap circuits [44], [45]. This enables integration in low-power systems and supports the trend toward battery-operated and compact devices. In light of the increased demand of the high-speed, thermally sensitive optoelectronic devices, this dissertation explores the development of thermally responsive devices based on QW-HBTs. These devices, with their inherent thermal sensitivity, offer promising front-end components for the next-generation smart thermal sensors. The detailed physics and design motivations behind such devices will be discussed in the following constitutive chapter.

doi:10.6342/NTU202500212

1.5 Thermal Sensing Mechanism of QW-Based HBTs

This section highlights the motivation behind this dissertation, emphasizing the potential of QW-HBTs as promising candidates for the front-end design of next-generation smart thermal sensing applications. Over the past two decades, GaAs-based HBTs have gained substantial recognition for high-temperature applications due to the significant energy band discontinuity, ΔE_V, present in the valence band of III-V emitter-base heterojunctions, such as AlGaAs/GaAs [46], [47], [48], [49], [50], [51]. This feature effectively suppresses hole current back injection, resulting in a high current gain, β_{HBT}. The current gain dependency can be better understood as $\beta_{HBT} \propto \left(1 - \alpha_t \delta_\gamma\right)^{-1}$, where α_t is the base transport factor, δ represents the recombination factor at the emitter-base junction determined by surface recombination at the heterojunction, and γ denotes the emitter injection efficiency. When the energy difference between the Fermi level $E_{F,E}$ and the valence band $E_{V,E}$ in the emitter increases, the equilibrium hole density $P_{E,0} \propto -\left(E_{F,E} - E_{V,E}\right)/k_B T$ decreases. Consequently, the addition of ΔE_V between the emitter and base reduces $P_{E,0}$ and $E_{V,E}$, enhancing thermal stability for sensor applications.

Conventional HBTs typically exhibit a slight decrease or stability in current gain as temperature rises due to the diminishing valence band discontinuity, ΔE_V [52]. In contrast, QW-HBTs show a distinct operational trend under increasing temperatures. This difference can be elucidated using the energy band diagrams shown in **Fig. 1.8**. **Figure.**

doi:10.6342/NTU202500212

1.8(a) presents the energy band diagram of a conventional HBT, while **Fig. 1.8(b)** illustrates a QW-HBT, highlighting the insertion of a QW into the active base layer. By incorporating a QW into the base, QW-HBTs create a novel structure. Unlike conventional HBTs, QW-HBTs feature a QW that traps a portion of the electrons moving from the emitter to the collector, undergoing recombination.

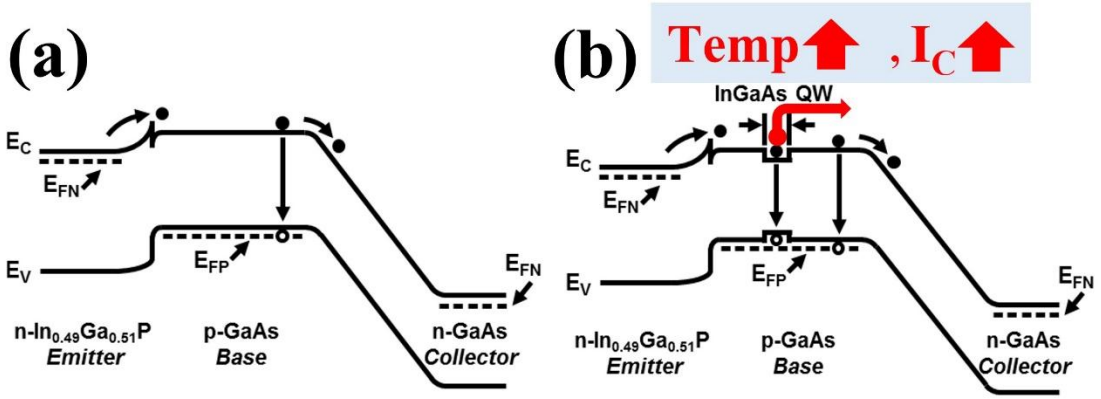


Fig. 1.8: (a) Energy band diagram of a typical InGaP/GaAs HBT, (b) Energy band diagram of a QW-HBT with an inserted InGaAs QW in the InGaP/GaAs HBT structure.

As the temperature rises, the thermal energy of electrons in the QW becomes sufficient to overcome the QW barrier, allowing these electrons to rejoin the diffusion flow towards the collector. This contributes to the collector current, I_C due to the high electric field at the base-to-collector (B-C) junction during forward active operation. This phenomenon results from the rapid escape of electrons from the QW at elevated temperatures, implying that the shorter escape time at higher temperatures enhances electron flow. Consequently, with an increase in temperature, the base current, I_B adjusts to maintain charge neutrality, leading to a larger fraction of electrons reaching the collector. This results in an increased

doi:10.6342/NTU202500212

collector current, I_C and current gain, $\beta \equiv \Delta I_C / \Delta I_B$, defined by the ratio of the increment in collector current ΔI_C to the increment in base current ΔI_B.

The thermionic emission advantage provided by the QW renders the QW-HBT highly sensitive to temperature. To benchmark against existing thermal sensing technologies, the QW-HBT layer structure is significantly optimized to improve current sensitivity, and a cascaded QW-HBT-based thermal sensor circuit is constructed to convert current sensitivity to voltage sensitivity, providing a comparison with current existing technologies. Further details are discussed in the subsequent chapters of this dissertation. In conclusion, the temperature-dependent current gain and collector current of QW-HBTs position them as promising candidates for next-generation front-end temperature sensors.

1.6 Thesis Organization

This thesis is structured to comprehensively explore the development, design, and application of LETs as highly sensitive devices for next-generation smart thermal sensing technology. The content is organized into six chapters, each contributing to a cohesive narrative of the research objectives, methodologies, and findings. The chapter are organized as follows:

- **Chapter 1: Introduction to Light-Emitting Transistor for Smart Thermal Sensing Technology**

This chapter provides an overview of the evolution of semiconductor technology,

doi:10.6342/NTU202500212

focusing on the development of LETs and their potential as advanced smart thermal sensing devices. It introduces the motivation, research objectives, and scope of this study, emphasizing the need for innovative thermal sensing technologies in OEICs.

- **Chapter 2: Design and Fabrication of Single QW-HBTs for Thermal Sensing Technology**

This chapter discusses the design principles and fabrication processes for SQW-HBTs, unveiling their distinct temperature-dependent current gain behavior. It includes the theoretical framework, material considerations, and step-by-step methodologies for constructing these devices, along with challenges and optimizations. The thermal characterization of QW-HBTs is detailed, covering experimental setups, measurement techniques, and result analysis. A modified charge-control model incorporating thermionic emission theory is developed to explain the observed thermal characteristics. The findings establish SQW-HBTs as promising candidates for high-precision smart thermal sensors.

- **Chapter 3: From Analytical Modeling of MQW-HBTs to Design and Fabrication of TQW-HBTs for Thermal Sensing Applications**

This chapter transitions from analytical modeling of multiple-quantum-well (MQW) HBTs to the design and fabrication of triple-quantum-well (TQW) HBTs for thermal sensor applications. The analytical modeling demonstrated how the number and

doi:10.6342/NTU202500212

positioning of QWs impact current gain, providing an efficient epi-layer design. A modified charge-control model for TQW-HBTs is developed to explain the thermal behavior of current-voltage characteristics at high temperature. This chapter also presents the thermal characterization of TQW-HBTs, highlighting experimental setups, measurement techniques, and data analysis methods. TQW-HBTs showcase significant thermal sensitivity and current gain enhancement, solidifying their potential as advanced smart thermal sensors.

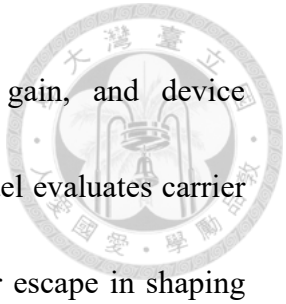
- **Chapter 4: Design and Fabrication of Novel Darlington Transistor Using LET for Smart Thermal Sensor Technology**

This chapter explores the integration of LETs into Darlington transistor configurations to develop a novel device for smart thermal sensor technology. It outlines the design principles, fabrication process, and performance evaluation of the Darlington transistor. This innovative approach enhances current amplification and thermal sensitivity, enabling the LET-based Darlington transistor to serve as a front-end component in advanced smart thermal sensing circuits.

- **Chapter 5: Thermal Sensitivity and Linearity Analysis of Quantum Well HBTs**

This chapter examines the effects of temperature and QW width variations on the electrical performance of QW-HBTs, focusing on their thermal sensitivity and linearity. A combination of simulations and experimental investigations is used to analyze the

doi:10.6342/NTU202500212



intricate relationships among temperature, QW width, current gain, and device performance. A modified temperature-dependent charge-control model evaluates carrier dynamics, emphasizing the roles of thermionic emission and carrier escape in shaping thermal sensitivity. Comparative analyses of different QW widths provide insights into achieving an optimal balance between sensitivity and linearity. The findings offer guidance of designing QW-HBTs suitable for integration into next-generation optoelectronic systems.

- **Chapter 6: Conclusion**

The final chapter summarizes the key findings and contributions of the thesis, emphasizing the advancements in LET for smart thermal sensing applications. Recommendations for future research are presented, including further modification of charge-control models, development of novel device structures, and exploration of industrial-scale fabrication processes. The chapter concludes by envisioning the potential of LET-based thermal sensors in next-generation optoelectronic and thermal sensing technologies.

By following this structure, the thesis systematically addresses the research goals and lays the groundwork for future innovations in LET-based smart thermal sensing technologies.

doi:10.6342/NTU202500212

Chapter 2

Design and Fabrication of Single QW-HBTs for Thermal Sensing Technology

2.1 Introduction

This chapter presents a comprehensive study on the design and fabrication of HBTs incorporating QWs and their potential applications in high-performance OEICs and advanced smart thermal sensing technologies. The focus is on the development of single quantum well-based HBTs (SQW-HBTs), specifically designed for thermal sensing applications, with an emphasis on integrating staircase QWs into the base region. These innovations aim to enhance temperature sensitivity and improve device performance under varying thermal conditions.

The chapter addresses the limitations of conventional front-end thermal sensing devices such as HBTs, BJTs, Schottky diodes, and MOSFETs in achieving high thermal sensitivity. To overcome these challenges, staircase InGaAs QWs are integrated into the base region of LETs. This approach leverages the unique thermionic emission properties of QWs, resulting in improved carrier dynamics, particularly by reducing electron escape time at higher temperatures.

doi:10.6342/NTU202500212

The chapter begins with Subchapter 2.2, “Motivation Behind SQW-HBTs for Thermal Sensing Application,” which highlights the need for devices with enhanced temperature sensitivity and explains the rationale for incorporating staircase QWs into the base region of LETs. The integration of SQWs offers distinctive carrier dynamics, enabling superior thermal performance compared to traditional HBTs.

In Subchapter 2.3, “Device Design and Fabrication of SQW-HBTs,” the structural design of SQW-HBTs is detailed, including material choices, layer compositions, and the specific role of the staircase InGaAs QWs in achieving the desired thermal behavior. It also includes a step-by-step process for fabricating SQW-HBTs, emphasizing the precision required to achieve high-quality layer structures and interfaces.

The chapter proceeds with Subchapter 2.4, “Device Characterization at Different Substrate Temperatures,” presents the experimental evaluations of SQW-HBTs under varying thermal conditions, revealing an unprecedented increase in current gain with temperature. This behavior, distinct from the conventional HBTs, providing the foundation for subsequent theoretical modeling.

The Subchapter 2.5 continues with “Development of Charge Control Models in LETs and TLs,” revisiting traditional charge-control models for LETs and TLs and preparing for

doi:10.6342/NTU202500212

the modifications needed to explain the unique thermal behavior of SQW-HBTs. Subchapter 2.6, “Necessity to Modify the Charge-Control Model for the Design of Highly Efficient SQW-HBTs Layer Structure” justifies these modifications, focusing on thermionic emission effects and temperature-dependent carrier dynamics specific to SQWs.

Following the subchapter 2.7, “Modified Thermionic Emission Model”, a calculation of highly sensitive escape time is introduced to explain the enhanced current gain observed in SQW-HBTs, accounting for phenomena such as reduced electron escape time and thermionic emission from the QW. This modified charge-control model is validated with the thermionic emission model in subchapter 2.8, “Validation of Experimental Results Using Modified Charge-Control Model for SQW-HBTs,” where experimental results align closely with theoretical predictions, confirming the model’s reliability.

In subchapter 2.9, “Carrier Dynamics and Charge Analysis in QW and Base regions,” offers a detailed analysis of carrier behavior in the QW and base regions, emphasizing the impact of these mechanisms on device performance. It further examines the distribution and dynamics of charge carriers in regions with and without QWs to underscore the advantages of SQWs.

doi:10.6342/NTU202500212

Finally, the subchapter 2.10, “Conclusion” summarizes the key findings of the chapter, highlighting the innovative contributions of SQW-HBTs to thermal sensing technology. The experimental and theoretical insights presented in this chapter pave the way for designing advanced smart thermal sensors with unprecedented accuracy and efficiency.

The findings of this study have been published in the IEEE Transactions on Electron Devices: Mukul Kumar et al., “Current gain enhancement of heterojunction bipolar light-emitting transistors using staircase InGaAs quantum well,” *IEEE Transactions on Electron Devices*, vol. 70, no. 10, pp. 5177–5183, Oct. 2023, doi: 10.1109/TED.2023.3305355.

This chapter lays the groundwork for leveraging SQW-HBTs in next-generation smart thermal sensing applications, demonstrating the potential of staircase SQW-HBTs for achieving high thermal performance and provides insights into their fabrication and operational principles.

2.2 Motivation Behind SQW-HBTs for Thermal Sensing Application

Incorporating a QW into the base region of a HBT offers unique advantages for thermal sensing. Instead of generating waste heat through recombination in the base, the

doi:10.6342/NTU202500212

QW-HBT provides dual outputs: an electrical output in the form of collector current and an optical output as trapped electrons recombine within the QW. Initially, the QW-HBT device was developed as a light-emitting device. However, when measured at different temperatures, QW-HBTs exhibited distinct temperature-dependent current gain characteristics that contrast with the typical HBT's behavior.

As outlined in Subchapter 1.5, the thermal mechanism in QW-HBTs is influenced by temperature-dependent thermionic emission within the QW, where an increase in temperature enhances carrier escape from the QW to contribute to the collector current. This thermal sensitivity in current makes QW-HBTs highly responsive to temperature changes. A larger temperature-to-current signal converts into an amplified temperature-to-voltage output signal, an attribute desirable for high-resolution thermal sensors.

Previous research by our lab group, led by Prof. Chao-Hsin Wu, demonstrated the thermally enhanced current gain of QW-HBTs [53]. However, for developing QW-HBTs with enhanced thermal sensitivity tailored for thermal sensor applications, further optimization of the QW-HBT layer structure is essential. Key factors to consider include QW design elements such as the number of QWs, their size, material composition, barrier height, and position within the HBT structure. In this dissertation, I report various QW-HBT layer structures aimed at improving current sensitivity and outline the development of a QW-HBT-based temperature sensing circuit in subsequent chapters.

doi:10.6342/NTU202500212

As this device was initially developed for light emission, its optical output can be enhanced by increasing the rate of radiative recombination within the QW or by incorporating multiple QWs. Optimizing the QW structure to minimize piezoelectric polarization field effects, such as through a staircase QW design, has been shown to improve this rate [54]. In this work, I investigate the temperature-dependent current gain of HBTs incorporating QWs, specifically comparing the performance of square QWs versus staircase QWs. This design also demonstrates an additional advantage of the enhanced current gain in QW-HBTs compared to previously fabricated devices. This work presents the temperature-dependent behavior of current gain in InGaP/GaAs QW-HBT, providing further insights into the thermionic emission mechanisms in staircase QWs. The temperature-sensitive collector current, or current gain, of QW-HBTs is promising as a potential candidate for front-end temperature sensor components in future applications [28], [55].

2.3 Device Design and Fabrication of SQW-HBTs

To investigate the temperature-dependent current-voltage behavior of n-p-n QW-HBTs, the epitaxial layer structure was grown using MOCVD on a semi-insulating (S.I.) GaAs substrate, with carbon (C) and silicon (Si) serving as dopants for the p-type and n-type layers, respectively. The growth process began with a 5000 Å n^+-type GaAs buffer layer on the (100) S.I. GaAs substrate. This was followed by deposition of the bottom n-

doi:10.6342/NTU202500212

type cladding layers, comprising a 634 Å $Al_{0.40}Ga_{0.60}As$ layer, a 5000 Å $Al_{0.95}Ga_{0.05}As$ oxidizable layer, and a 150 Å $Al_{0.40}Ga_{0.60}As$ oxide buffer layer. Subsequently, the heavily doped sub-collector layer was added, consisting of a 200 Å GaAs (n-type) layer, a 120 Å $In_{0.49}Ga_{0.51}P$ (n-type) etch-stop layer, and an undoped 600 Å GaAs collector layer on top of the bottom cladding layer.

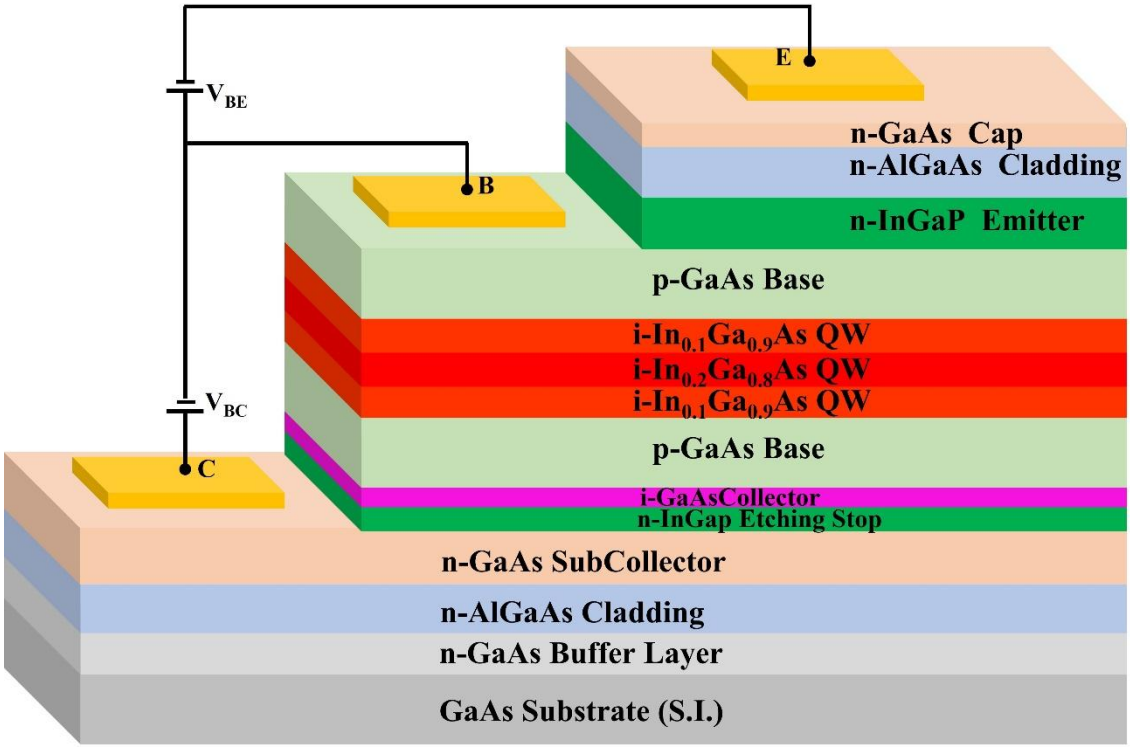


Fig. 2.1: Schematic epitaxial structures of the fabricated n-p-n QW-HBT device.

The base layer, a heavily doped p^+-GaAs with an approximate doping concentration of 3×10^{19} cm^{-3} and a thickness of 980 Å, includes a series of quantum wells (QWs) forming a staircase QW structure to enhance temperature sensitivity. Specifically, the base contains undoped 20 Å $In_{0.1}Ga_{0.9}As$, 120 Å $In_{0.2}Ga_{0.8}As$, and another 20 Å $In_{0.1}Ga_{0.9}As$ QWs, positioned 590 Å away from the emitter. This is followed by a 250 Å n-type

doi:10.6342/NTU202500212

$In_{0.49}Ga_{0.51}P$ wide-gap emitter layer and an upper cladding structure composed of several layers: a 150 Å $Al_{0.35}Ga_{0.65}As$ oxide buffer layer, a 150 Å $Al_{0.8}Ga_{0.2}As$ oxidizable layer, a

Table 2.1: The epitaxial layer structure design of n-p-n QW-HBT.

Layer Name	Material	Mole Fraction (x)	Thickness (Å)	Type	Doping Level (Cm^{-3})	Dopant
Contact	GaAs		1000	N^+	3e18	Si
Confining	$Al_xGa_{1-x}As$	0.35	500	N	2e18	Si
Oxidizable	$Al_xGa_{1-x}As$	0.8	300	N	1.5e18	Si
Oxide Buffer	$Al_xGa_{1-x}As$	0.95~0.99	4000	N	1.5e18	Si
Oxidizable	$Al_xGa_{1-x}As$	0.8	150	N	8e17	Si
Oxide Buffer	$Al_xGa_{1-x}As$	0.35	150	N	5e17	Si
Emitter	$In_xGa_{1-x}P$	0.49	250	N^-	5e17	Si
Base	GaAs		100	P	4e19	C
Base	GaAs		100	P	2e19	C
Base	GaAs		300	P	1e19	C
Buffer	GaAs		10	i		UID
QW	$In_xGa_{1-x}As$	0.1	20	i		UID
QW	$In_xGa_{1-x}As$	0.2	120	i		UID
QW	$In_xGa_{1-x}As$	0.1	20	i		UID
Buffer	GaAs		10	i		UID
Base	GaAs		200	P	1e19	C
Base	$Al_xGa_{1-x}As$	0.05	100	P	3e19	C
Collector	GaAs		600	i	5e16	UID
Order	$In_xGa_{1-x}P$	0.49	120	N^-	3e18	Si
Sub-Collector	GaAs		200	N	3e18	Si
Oxide Buffer	$Al_xGa_{1-x}As$	0.4	150	N	2e18	Si
Oxidizable	$Al_xGa_{1-x}As$	0.95	5000	N	1.50e18	Si
Oxide Buffer	$Al_xGa_{1-x}As$	0.4	634	N	2e18	Si
Buffer Layer	GaAs		5000		3e18	
Substrate 4" GaAs S.I.						

doi:10.6342/NTU202500212

4000 Å $Al_xGa_{1-x}As$ (where x varies from 0.95 to 0.99) acting as an oxide buffer layer, a 300 Å $Al_{0.8}Ga_{0.2}As$ oxidizable layer, and a 500 Å $Al_{0.35}Ga_{0.65}As$ confining layer. Finally, the epitaxial structure is capped with a 1000 Å n^+-GaAs contact layer to ensure low-resistance ohmic contact at the emitter. The epitaxial structure of the QW-HBT is illustrated in **Fig. 2.1**, and **Table 2.1** provides a detailed breakdown of each layer's composition and specifications.

The fabrication of the SQW-HBT device was conducted in the cleanroom facilities at NTU, under the guidance of Prof. Chao-Hsin Wu. The device fabrication process involved a series of standard semiconductor techniques, including photolithography, chemical wet etching, reactive ion etching (RIE), e-beam evaporation, thermal evaporation, plasma-enhanced chemical vapor deposition (PECVD), lift-off, and annealing. The device fabrication was completed in ten sequential steps, as outlined below:

1. Wafer Cleaning

To ensure a contaminant-free surface for photoresist application, the wafer was initially soaked in 95℃ acetone for 5 minutes, followed by 95℃ methanol for an additional 5 minutes. After rinsing with isopropyl alcohol (IPA) and drying with nitrogen, the wafer was baked at 110℃ for 5 minutes on a hot plate. This cleaning step, as shown in **Fig. 2.2**, ensures the cleanliness of the emitter layer's surface.

doi:10.6342/NTU202500212

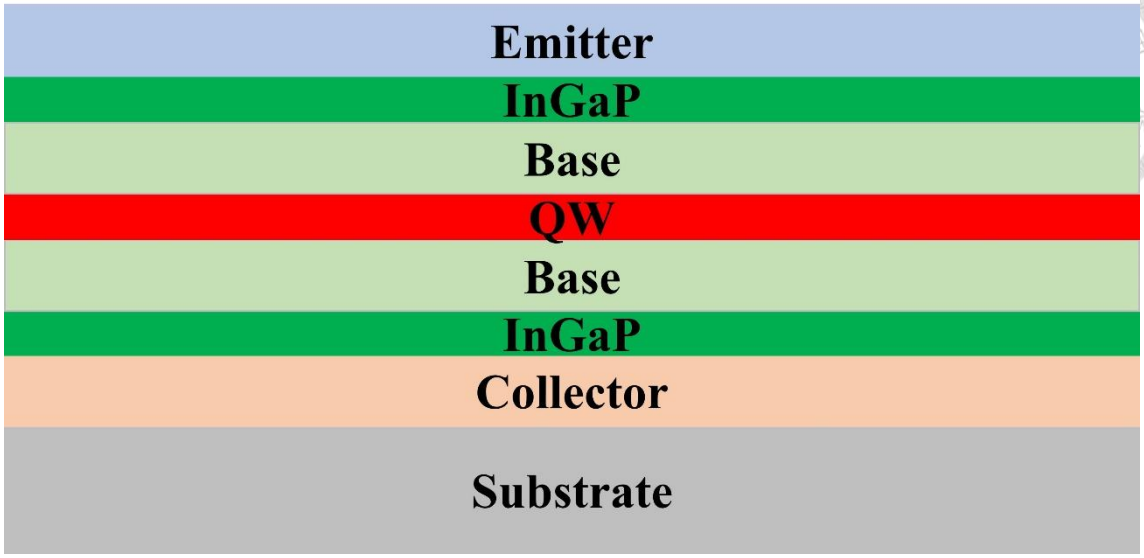


Fig. 2.2: Cross-sectional view of the wafer showing the initial layer structure of the n-p-n SQW-HBT.

2. Emitter Etch

The process begins with spin-coating the wafer using S1813 photoresist, applied at 1000 rpm for 10 seconds and then at 4000 rpm for 30 seconds, followed by baking on a hot plate at 110℃ for 1 minute to enhance adhesion. This is followed by a soft bake for photoresist planarization. After baking, the photoresist is removed at the wafer edges to ensure uniform thickness. Using a light-field photomask, the emitter region is defined, and the wafer is exposed on an MJB4 Mask Aligner in hard contact mode. The photoresist is developed by immersing and gently agitating the wafer in MF319 developer for a few seconds, followed by two rinses in deionized (DI) water. To further harden the photoresist before wet etching, the wafer undergoes a hard bake at 110℃ for 5 minutes.

Selective etching of the emitter mesa is carried out by soaking the wafer in a dilute sulfuric

doi:10.6342/NTU202500212

acid solution (H_2SO_4: H_2O_2: H_2O = 1:8:120). The etching process stops at the InGaP layer beneath the emitter. Finally, the S1813 photoresist is removed by soaking the wafer in acetone, followed by methanol, a rinse in IPA, and drying with nitrogen. The cross-sectional view of the device after emitter etching is shown in **Fig. 2.3**.

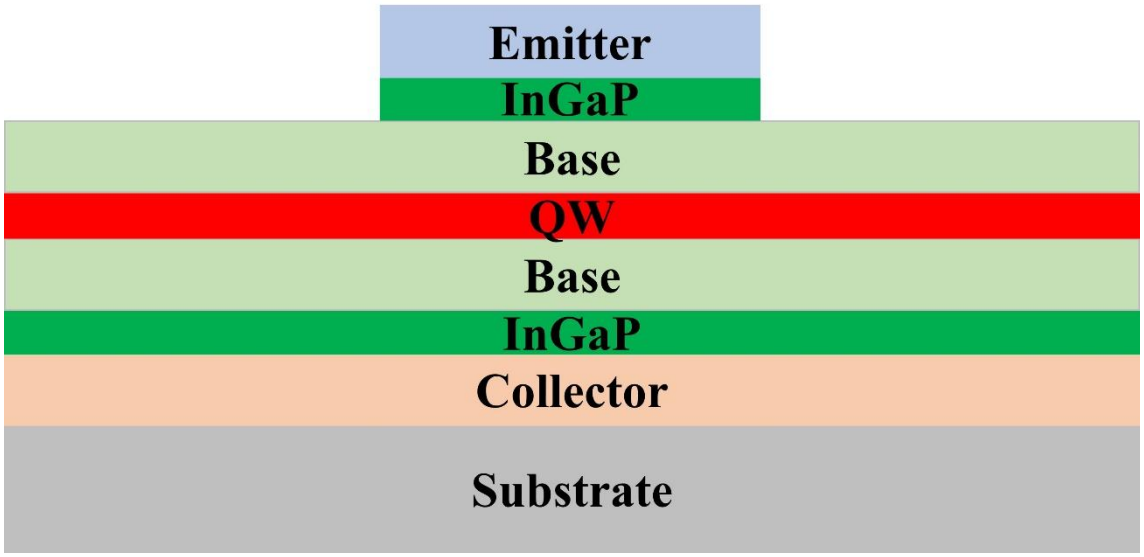


Fig. 2.3: Cross-sectional view of the device following the emitter etching process.

3. Base Metal Contact Deposition

The deposition process begins with wafer cleaning, followed by spin-coating with PMGI photoresist at 1000 rpm for 10 seconds and 4000 rpm for 60 seconds. This is succeeded by a 5-minute bake on a hot plate at 270℃. Next, the wafer is spin-coated with S1813 photoresist at 1000 rpm for 10 seconds and 4000 rpm for 30 seconds, and then baked on a hot plate at 110℃ for 1 minute. To ensure photoresist planarization, edge bead removal is performed. A dark-field photomask is used to define the base region, and the wafer is exposed using an MJB4 Mask Aligner in hard contact mode. The S1813 photoresist is

doi:10.6342/NTU202500212

developed by immersing the wafer in MF319 developer with gentle agitation for a few seconds, followed by two rinses in DI water. Next, the wafer undergoes deep ultraviolet (DUV) exposure for 150 seconds, followed by PMGI photoresist development in 101A developer for 50 seconds, with double rinsing in DI water. This DUV exposure and 101A development sequence is repeated to achieve an undercut photoresist structure. To eliminate any native oxide on the base layer surface, the wafer is immersed in buffered oxide etchant (BOE) for 10 seconds and rinsed twice in DI water. Ti/Pt/Au metal layers (thicknesses of 150 Å, 150 Å, and 2000 Å, respectively) are then deposited as p-type base contacts via E-gun evaporation.

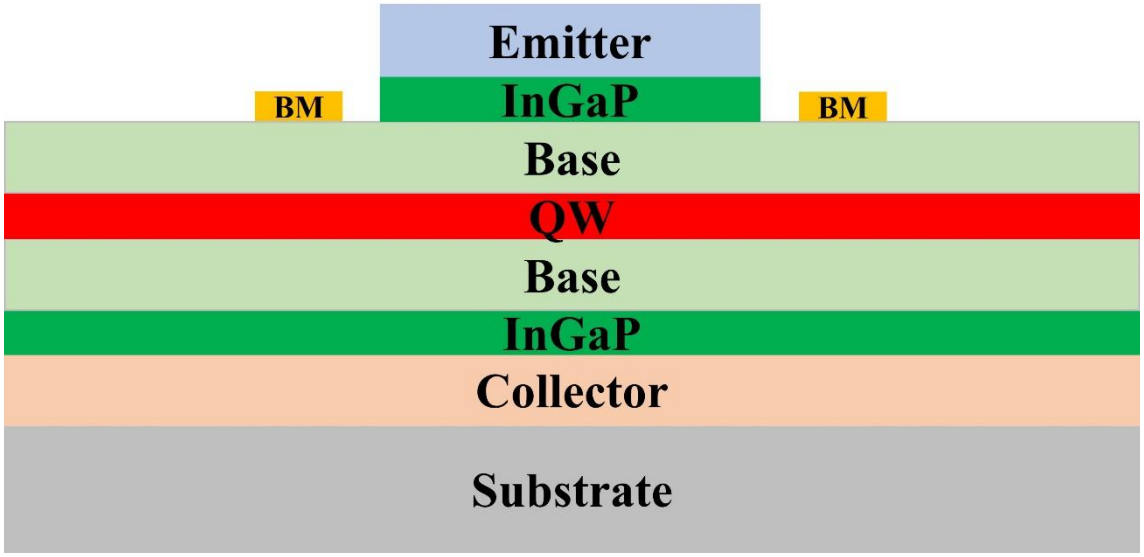


Fig. 2.4: Cross-sectional view of the device after base metal deposition.

The lift-off process begins with stripping the S1813 photoresist by soaking the wafer in acetone at 25℃ for 20 minutes, then in acetone at 65℃ for 10 minutes, followed by acetone at 95℃ for an additional 10 minutes. This is followed by soaking in methanol,

doi:10.6342/NTU202500212

rinsing with IPA, and drying with nitrogen. Finally, the PMGI photoresist is removed by soaking in N-Methyl-2-pyrrolidone (NMP) at 90℃ for 15 minutes, followed by rinsing with IPA, two DI water rinses, and drying with nitrogen. The cross-sectional view of the device following base metal evaporation is illustrated in **Fig. 2.4**.

4. Base-Collector Etch

This process follows similar cleaning, photoresist spin-coating, photolithography, development, and oxide removal steps as those used in emitter etching. However, after the wafer is soaked in dilute sulfuric acid for wet etching, an additional step involves immersing the wafer in HCl for 3 seconds to selectively remove the InGaP layer above the collector layer. Once the InGaP etch-stop layer is removed, the S1813 photoresist is stripped by soaking the wafer in acetone, followed by soaking in methanol, rinsing with IPA, and drying with nitrogen.

5. Emitter and Collector Metal Contacts Disposition

The cleaning, photoresist spin-coating, photolithography, and development procedures follow the same steps as in the base metal deposition process. Au/Ge/Ni/Au metal layers with thicknesses of 250/500/150/2000 Å are deposited as emitter contacts on the emitter contact layer and as collector contacts on the heavily doped sub-collector layer. For the lift-off process, the S1813 photoresist is removed by sequentially soaking the wafer in acetone at 25℃ for 20 minutes, at 65℃ for 10 minutes, and at 95℃ for 10 minutes. This

doi:10.6342/NTU202500212

is followed by a methanol soak, rinsing with IPA, and drying with nitrogen. The PMGI photoresist is then stripped by soaking the wafer in NMP at 90°C for 15 minutes, followed by rinsing with IPA, two rinses in DI water, and nitrogen drying. The cross-section of the device after emitter/collector metal deposition is illustrated in **Fig. 2.5**.

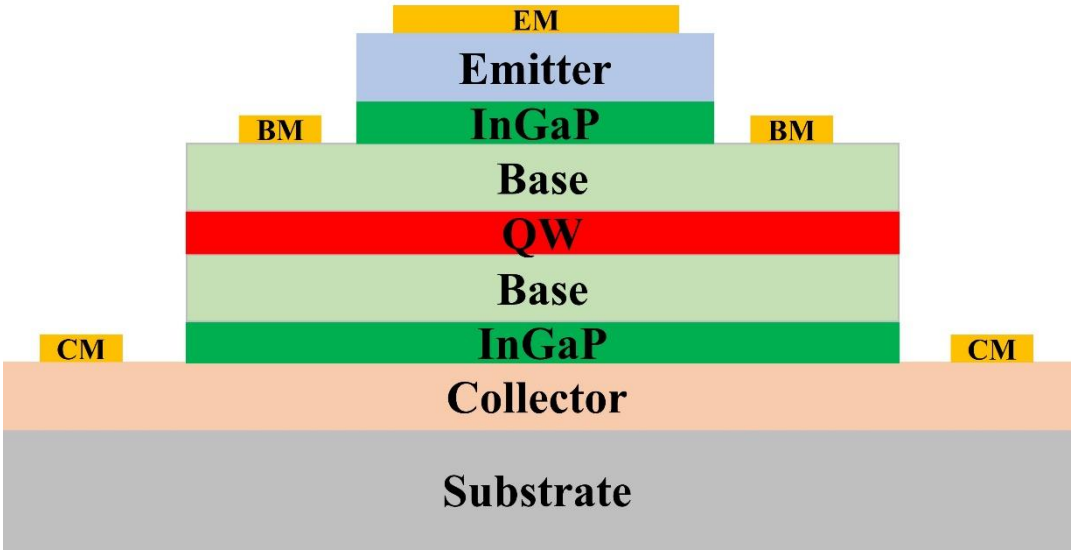


Fig. 2.5: Cross-sectional view of the device post emitter and collector metal deposition.

6. Device Isolation

In this design, the SQW-HBTs are interconnected, necessitating electrical isolation to prevent leakage current. The cleaning, photoresist spin-coating, photolithography, and development procedures are performed as described in the emitter etching process. To achieve selective etching down to the undoped substrate, the wafer is soaked in a dilute sulfuric acid solution (H_2SO_4: H_2O_2: H_2O = 1:8:120), which etches the bottom cladding layer. Finally, the S1813 photoresist is removed by sequentially soaking the wafer in acetone, then methanol, rinsing with IPA, and drying with nitrogen. The cross-section of

doi:10.6342/NTU202500212

the device after isolation is illustrated in **Fig. 2.6**.

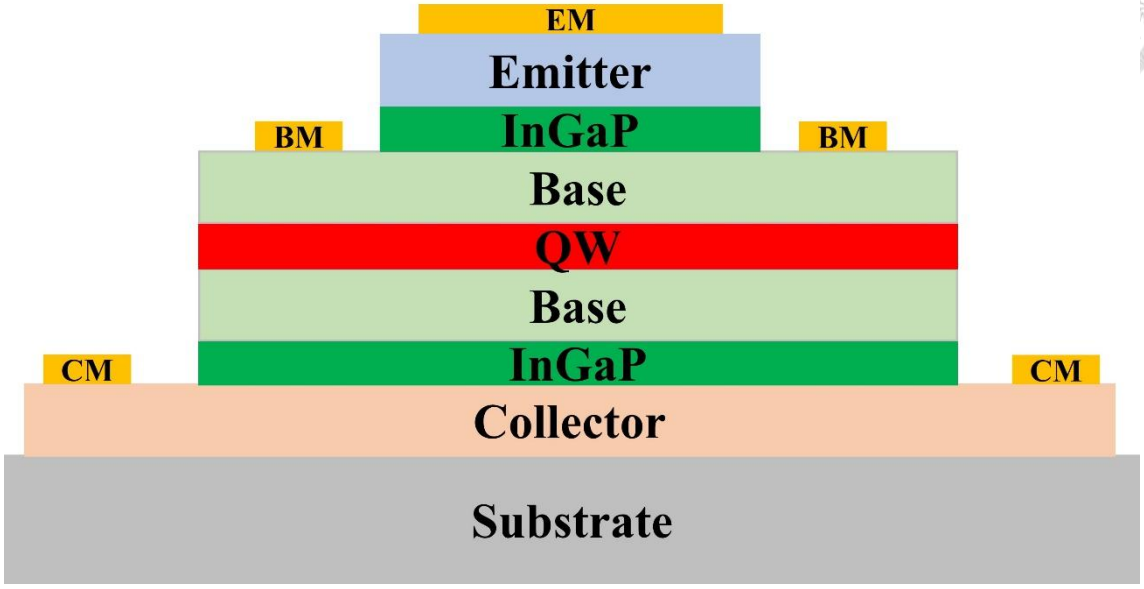


Fig. 2.6: Cross-sectional view of the device after the isolation process.

7. SiN_X Planarization

Following the initial cleaning steps, silicon nitride (SiN_X) is applied as a passivation layer to protect the devices and ensure sufficient space for probing and metal evaporation. SiN_X is deposited using PECVD at a rate of 3 Å/s for approximately 30 minutes, achieving a final thickness of 4000 Å. The cross-section of the device after SiN_X planarization is illustrated in **Fig. 2.7**.

8. Resistor Evaporation

The cleaning, photoresist spin-coating, photolithography, and development, process steps are the same as those used in the base metal deposition process. Nickel-chromium (NiCr) metal is deposited onto the SiN_X passivation layer via thermal evaporation to form a

doi:10.6342/NTU202500212

resistor connecting the collectors of two SQW-HBTs. For the lift-off process, the S1813 photoresist is removed by sequentially soaking the wafer in acetone at 25℃ for 20 minutes, at 65℃ for 10 minutes, and at 95℃ for another 10 minutes, followed by soaking in methanol, rinsing with IPA, and drying with nitrogen. The PMGI photoresist is subsequently removed by soaking the wafer in NMP at 90℃ for 15 minutes, then rinsing with IPA, rinsing twice in DI water, and drying with nitrogen. The cross-section of the device post-resistor evaporation is shown in **Fig. 2.7**.

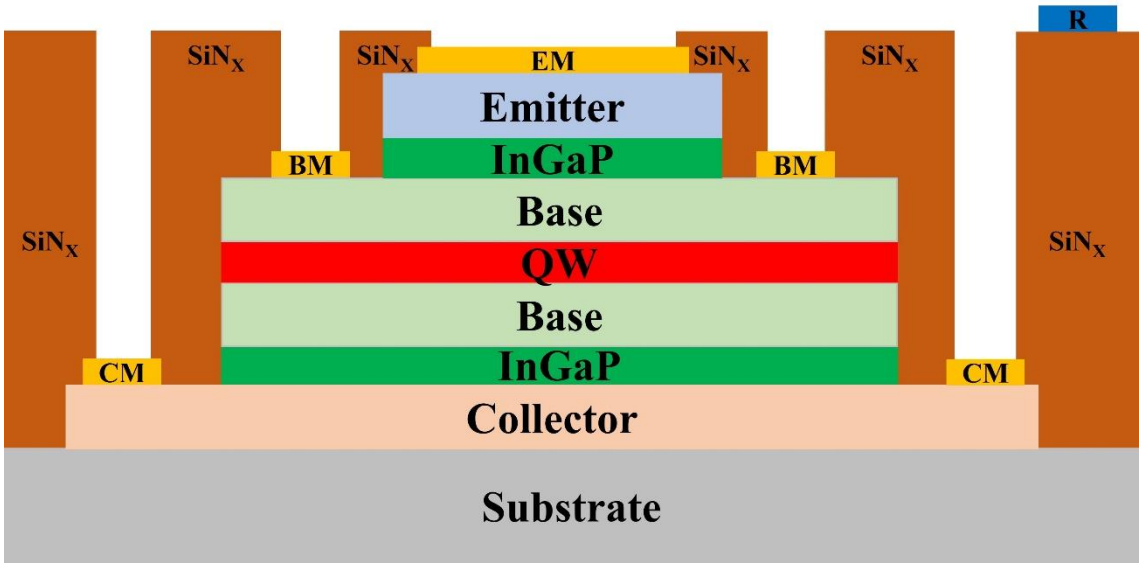


Fig. 2.7: Cross-sectional view of the device following resistor deposition.

9. Via Hole Formation

The cleaning, photoresist spin-coating, photolithography, and development processes follow the same step as in the emitter etching step. The via holes are created by dry etching the SiN_X layer using RIE. Following this, the S1813 photoresist is removed by soaking the wafer in acetone, followed by immersion in methanol, rinsing with IPA, and drying

doi:10.6342/NTU202500212

with nitrogen. The cross-section of the device after the via hole formation is shown in **Fig. 2.7.**

10. Metal Pad and Interconnect Deposition (Metal 1):

The cleaning, photoresist spin-coating, photolithography, and development steps follow the same procedure as in the base metal process. Titanium/gold (Ti/Au) metal contacts, with thicknesses of 500/6000 Å, are deposited to form the Metal 1 pads and establish interconnects between the two SQW-HBTs, completing the device. For liftoff, the S1813 photoresist is removed by soaking the wafer in acetone at 25°C for 20 minutes, followed by immersion in acetone at 65°C for 10 minutes, and acetone at 95°C for 10 minutes. The wafer is then soaked in methanol, rinsed with IPA, and dried with nitrogen. The PMGI photoresist is removed by soaking the wafer in NMP at 90°C for 15 minutes, followed by

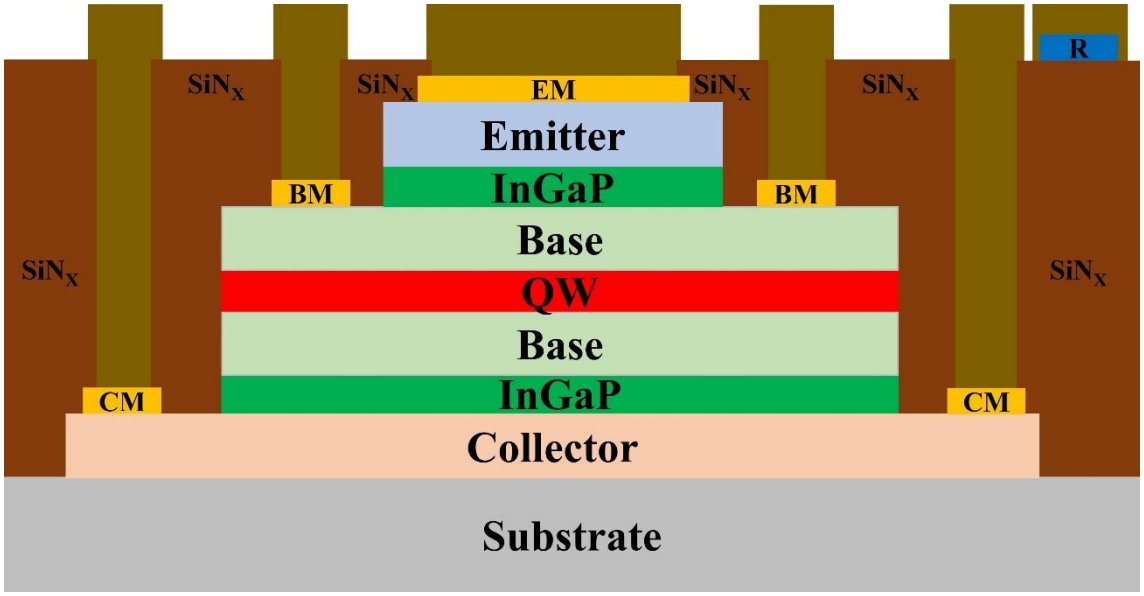


Fig. 2.8: Cross-sectional view of the final fabricated device structure.

doi:10.6342/NTU202500212

rinsing with IPA, two rinses in DI water, and drying with nitrogen. The cross-section of the device after the Metal 1 evaporation process is shown in **Fig. 2.8**. The final successfully fabricated device is shown in inset of **Fig. 2.9**.

2.4 Device Characterization at Different Substrate Temperature

After the successful fabrication of the SQW-HBT device, it was subjected to a temperature-dependent study of its current-voltage (I-V) characteristics. To investigate the temperature-dependent behavior, we used four-probe DC measurements, allowing an in-depth analysis of device physics under elevated temperature conditions. Device characterization was conducted by placing the device on a Peltier temperature-controlled stage, which facilitated examination of the thermally enhanced collector current.

The device achieves thermal equilibrium within two minutes, but a stabilization period of approximately 15 to 20 minutes was allowed to ensure the Peltier stage reached a steady-state temperature for accurate and precise measurements. The characterization setup, including the four-probe method and Peltier stage, is illustrated in **Fig. 2.9**. The inset of **Fig. 2.9** shows the final fabricated device used for this study. A temperature range of 25°C to 85°C was selected, as this range is relevant for real-world applications where precise temperature sensing is crucial. This range also provides insights into the device's

doi:10.6342/NTU202500212

performance under standard operating conditions.

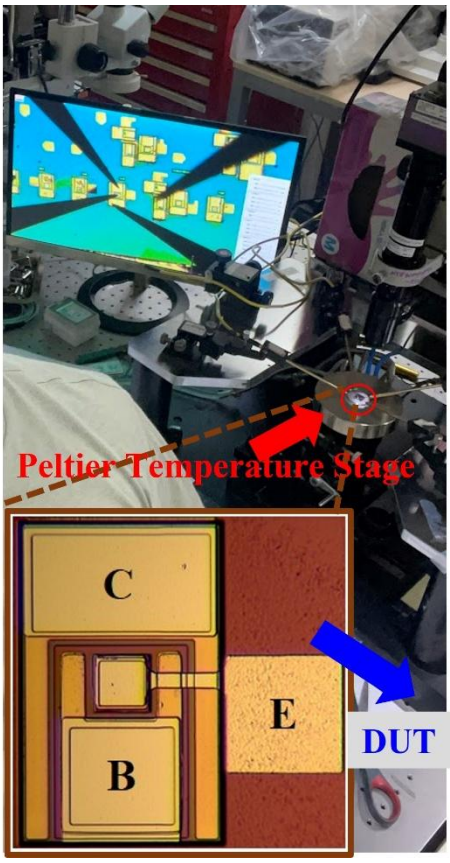


Fig. 2.9: The experimental setup for device characterization. The inset shows the top-view layout of the fully fabricated SQW-HBT, with an emitter cross-sectional area of 40 μm x 40 μm.

For the experiment, an Agilent E5270B was used to supply the DC bias and current. The base current, I_B was varied from 0.2 mA to 1 mA in 0.2 mA increments, while the collector-to-emitter voltage, V_{CE} was swept from 0 to 2 volts. **Figure 2.10** illustrates the collector current, I_C as a function of V_{CE} for different base currents, I_B at substrate temperatures, T_{ext} = 25°C and 85°C. Under forward-active conditions, the collector current increased from 0.394 mA to 0.683 mA at I_B of 0.2 mA and V_{CE} of 2 V. To further understand the underlying device physics, an energy band diagram of the SQW-HBT is

doi:10.6342/NTU202500212

shown in **Fig. 2.11**. When electrons travel from the emitter to the collector, a portion of them are captured by the QW. At higher temperatures, electrons acquire enough energy to overcome the quantum-well energy barrier, leading to an increase in the collector current, I_C and current gain, $\beta = \Delta I_C / \Delta I_B$ with base-to-collector voltage, V_{BC} = 0 V.

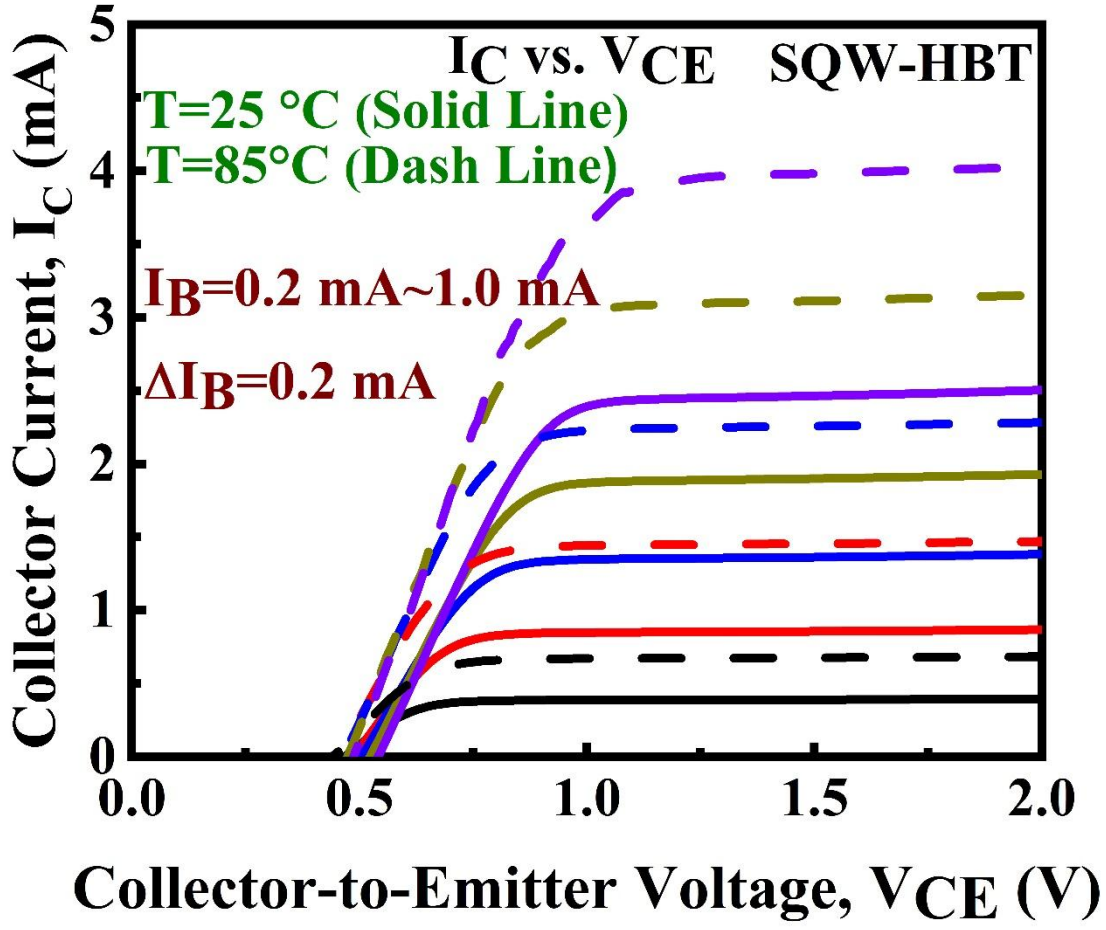


Fig. 2.10: Measured collector current, I_C versus collector-to-voltage, V_{CE} of n-p-n InGaP/GaAs SQW-HBT at different substrate temperatures.

Fig. 2.12 also shows the experimental variation of current gain, β with substrate temperatures, T_{ext} from 25℃ to 85℃. This observed enhancement in current gain is attributed to both higher substrate temperature, T_{ext} and base current, I_B, with a possibility

doi:10.6342/NTU202500212

of enhanced internal heating at higher I_B contributing to further current gain increments.

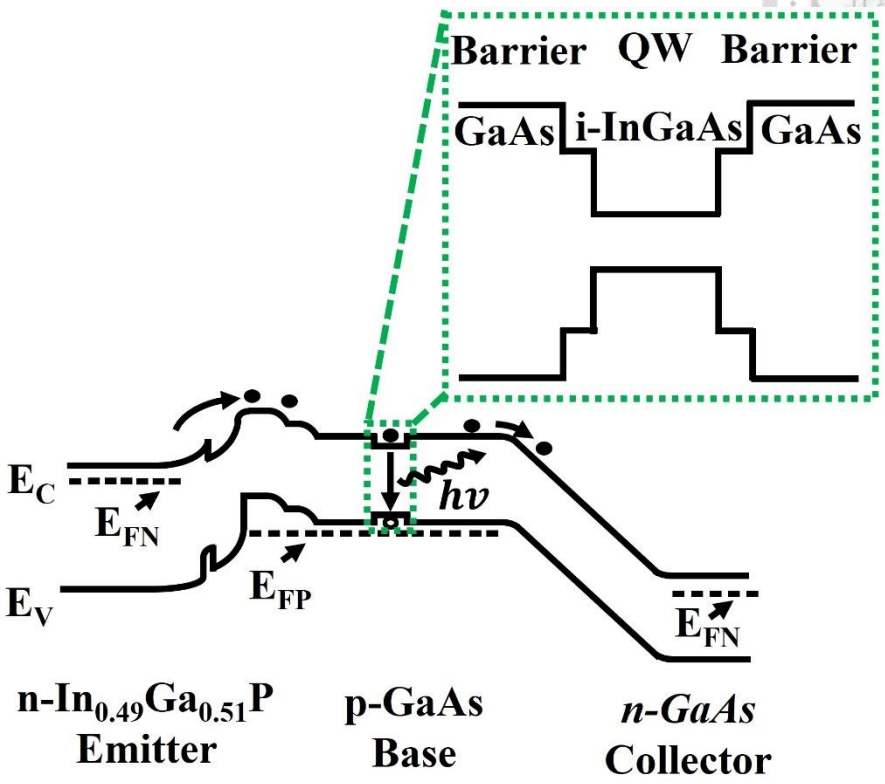


Fig. 2.11: Energy band diagram of an n-type InGaP/p^+-type GaAs/ n-type GaAs SQW-HBT. The inset shows the staircase QW design in the GaAs (p^+-type) base.

This experimental study highlights a unique and significant increase in collector current, approximately 73.23%, at I_B of 0.2 mA and V_{CE} of 2 V, as the SQW-HBT temperature was raised from 25℃ to 85℃. This behavior contrasts with conventional HBTs and is primarily due to the rapid escape of electrons from the InGaAs QW at higher temperatures. Given the novel characteristics of this device, further exploration is required to fully understand its SQW at higher-temperature operation. A temperature-sensitive model will be developed in the next subchapter to provide a deeper investigation into the device physics and provide a means to validate experimental results.

doi:10.6342/NTU202500212

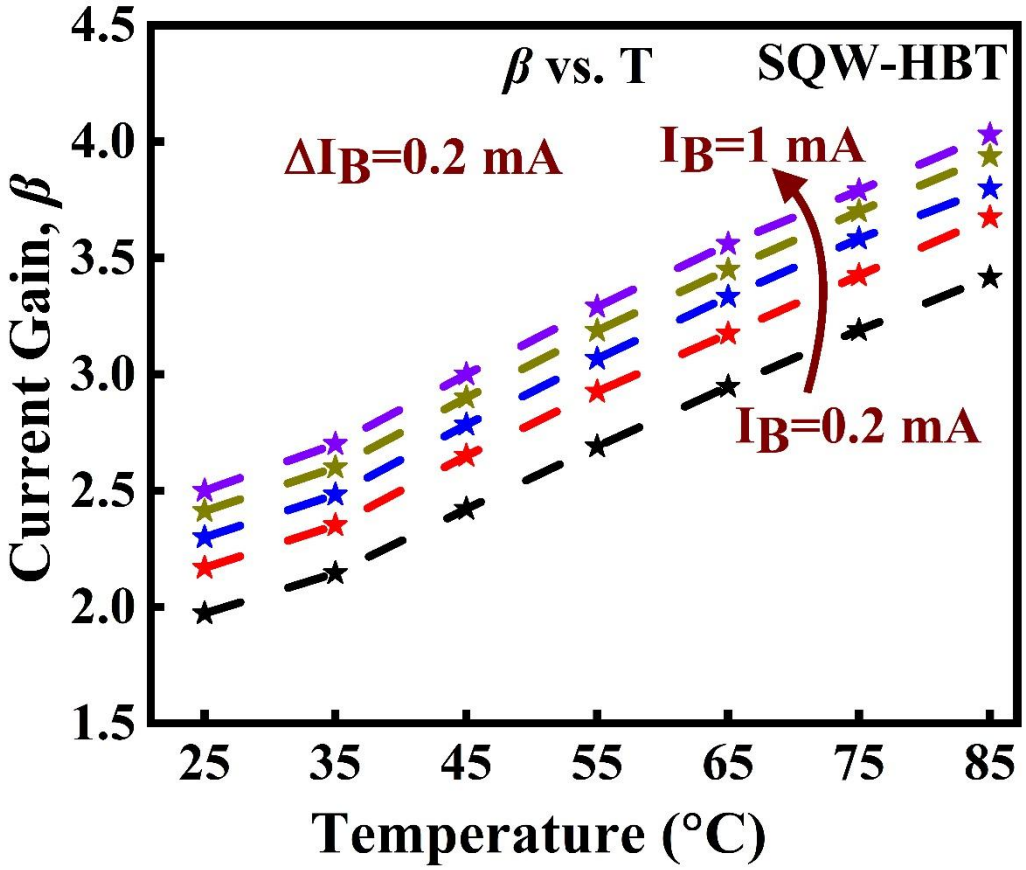


Fig. 2.12: Experimental temperature-dependent current gain as a function of various substrate temperatures, T_{ext} at the different base current, I_B from 0.2 mA to 1 mA.

2.5 Development of Charge-Control Models in LETs and TLs

The evaluation of charge-control models in QW-based optoelectronics devices, such as LETs and TLs, has progressed significantly since 2007, and has played a crucial role in enhancing their design and performance. These models serve to describe the intricate dynamics of carrier injection, recombination, and transport within the QWs embedded in the transistor's base. Since the early conceptualization of LETs and TLs, numerous studies have contributed to refining the charge-control model, incorporating factors like spontaneous and stimulated recombination, high-frequency modulation, and thermionic

doi:10.6342/NTU202500212

emission. These refinements are critical for tailoring LETs and TLs to specific applications, including high-speed communication and thermal sensing.

In 2007, the foundational work on charge-control model in LETs and TLs emphasized the role of QWs in enhancing recombination dynamics [56], [57]. The basic charge-control model of heterojunction bipolar light-emitting transistor (HBLET) was developed by H. W. Then et al. [56]. This model demonstrated how the base minority carrier electron lifetime in n-p-n QW-HBLETs varies with base doping density and the width of the QWs. Their study showed how the minority carrier lifetime could be experimentally determined in HBLETs. The findings showed that inserting QWs into the base region significantly reduced carrier lifetimes, enhanced recombination rates, and enabled faster modulation. The carrier lifetime was reduced from 134 ps in structures without QWs to 10 ps with double QWs and increased doping concentrations, highlighting the impact of QW design on charge-control model. In the same year, 2007, M. Feng et al. [57] developed the basic charge-control model of TLs accounting for the short recombination lifetime in the QW base. This dual-purpose model, which was based on the charge-control technique and laser equations due to their electrical signal amplification with coherent light generation, demonstrates the absence of carrier-photon resonance in TLs, estimating a 3 dB bandwidth up to 70 GHz. This charge-control model was introduced to explain the interaction between carrier injection and recombination in the QW, particularly under

doi:10.6342/NTU202500212

high-frequency conditions. This study highlighted the significance of carrier lifetime in dictating the modulation response, laying the groundwork for TL modeling.

In 2009, B. Faraji et al. [58] developed an analytical charge-control model of TLs, detailing how the small-signal modulation response could be improved by reducing relaxation oscillations and stabilizing the frequency response. Zhang and Leburton (2009) further developed a transient model to describe electron-photon interactions in QWs and carrier dynamics in TLs, predicting a modulation bandwidth of up to 55 GHz under optimal conditions [59]. This work provides insights into electron transit times and recombination dynamics for high-frequency operation.

Research by Iman Taghavi et al. [60] in 2012 advanced charge-control model by exploring the effects of multiple QWs in the base of TLs. Their work demonstrated that multi-QW designs enhance the differential gain and reduce recombination lifetimes, achieving modulation bandwidths of up to 60 GHz. This study emphasized how multi-QW structures could optimize both optical and electrical properties, offering new possibilities for TL applications in high-speed telecommunications applications. Furthermore, Basu et al. [61] (2012) extended the charge control-model for TLs in a common-emitter configuration, examining the effects of stimulated recombination on current gain compression above the lasing threshold. This study was essential for understanding TL behavior in high-injection regimes and ensuring stable gain under demanding operational

doi:10.6342/NTU202500212

conditions.

Unlike TLs, LETs prioritize spontaneous radiative recombination rather than stimulated emission, requiring a different charge-control approach. Li and Leburton extended charge-control models for LETs in (2018) and developed a modified charge-control model for LETs focusing on QW capture times and base carrier lifetime, key factors influencing frequency response and modulation speed [62]. This study highlights that QW structures effectively reduce base carrier lifetime, enhancing high-speed performance. Their model, adapted from the standard charge-control model of BJTs, accounts for the impact of heavy base doping on base transport and its dependence on base current. This approach provides insights into device parameters such as capture time, base lifetime, and transit time, as well as design factors like doping concentration, base width, QW width, number, and location, aligning closely with experimental optical frequency responses. Chang et al. [53] introduced a thermally sensitive charge-control model for QW-HBTs in 2019. This model incorporated thermionic emission to explain the unusual enhancement of current gain with increasing temperature. By modeling the temperature-dependent escape rates of carriers from the QW, this work supported the development of LETs for thermal sensing technologies.

Yang et al. [63] extended the charge-control model by developing a four-port SPICE-compatible model for LETs in 2020, enabling circuit-level simulations of their optical and

doi:10.6342/NTU202500212

electrical characteristics. This model incorporated advanced charge-control mechanisms, including carrier transport and tunneling effects, and the Franz-Keldysh (F-K) effect, facilitating the integration of LETs, into complex circuits for real-world applications. This work bridged the gap between theoretical modeling and practical deployment, particularly in optoelectronic circuits.

The most recent advancements were achieved by Tung et al. [64] in 2022, who developed charge-control models for tunnel-junction TLs (TJTLs). Their work introduced both current and voltage modulation capabilities into the charge control framework, accounting for factors such as electric fields, QW positioning, and collector doping concentrations. By integrating the F-K effect and intra-cavity photon-assisted tunneling (ICPAT), this work laid the foundation for further enhancements in TL and LET performance for complex applications.

The development of advanced charge-control models for LETs and TLs has progressed continually through theoretical advancements and experimental validations. To develop a highly thermal-sensitive QW-based HBT device, an advanced charge-control model is required for designing an efficient epi-layer. In the following sections, the mathematical foundation and experimental validation of our developed modified charge-control model are explored, emphasizing their application in staircase SQW-HBTs for smart thermal sensor technologies.

doi:10.6342/NTU202500212

2.6 Necessity to Modified the Charge-Control Model for the Design of Highly Efficient SQW-HBTs Layer Structure

In a SQW-HBT, the QW plays a crucial role in modifying the minority carrier distribution by capturing electrons. This behavior differs from a separate confinement heterojunction (SCH), particularly due to the forward-active mode in which the transistor operates. The minority charge distribution within the base of SQW-HBT is tilted by the reverse-biased base-collector junction, where the high electric field at the junction sweeps electrons from the base toward the collector, leading to a nearly zero electron density at the collector.

A previous report presented a simple charge-control model for LETs [56], and another charge-control model is discussed in subchapter 2.5. In this chapter 2, we focus on exploring the thermal characteristics of current gain, β and the behavior of minority carriers near the staircase SQW. To achieve this, we utilize analytical expressions that are explicitly related to various time-dependent parameters. **Figure 2.13** illustrates the base minority charge distribution (ρ) of the modified charge-control model for SQW-HBT. The total base minority charge distribution of the SQW-HBT can be approximated as a superposition of two triangular charge populations: Q_0 and Q_1. The charge Q_0 represents electrons diffusing from the emitter to the collector, forming the collector current, I_C in

doi:10.6342/NTU202500212

the absence of the QW, while Q_1 represents the electrons trapped by the QW after diffusing from the emitter. The charge Q_{QW} represents the electrons trapped within the quantum well. Notably, the distribution of Q_0 approaches zero at the base-collector (B-C) junction, whereas the distribution of Q_1 vanishes at the location of the staircase QW.

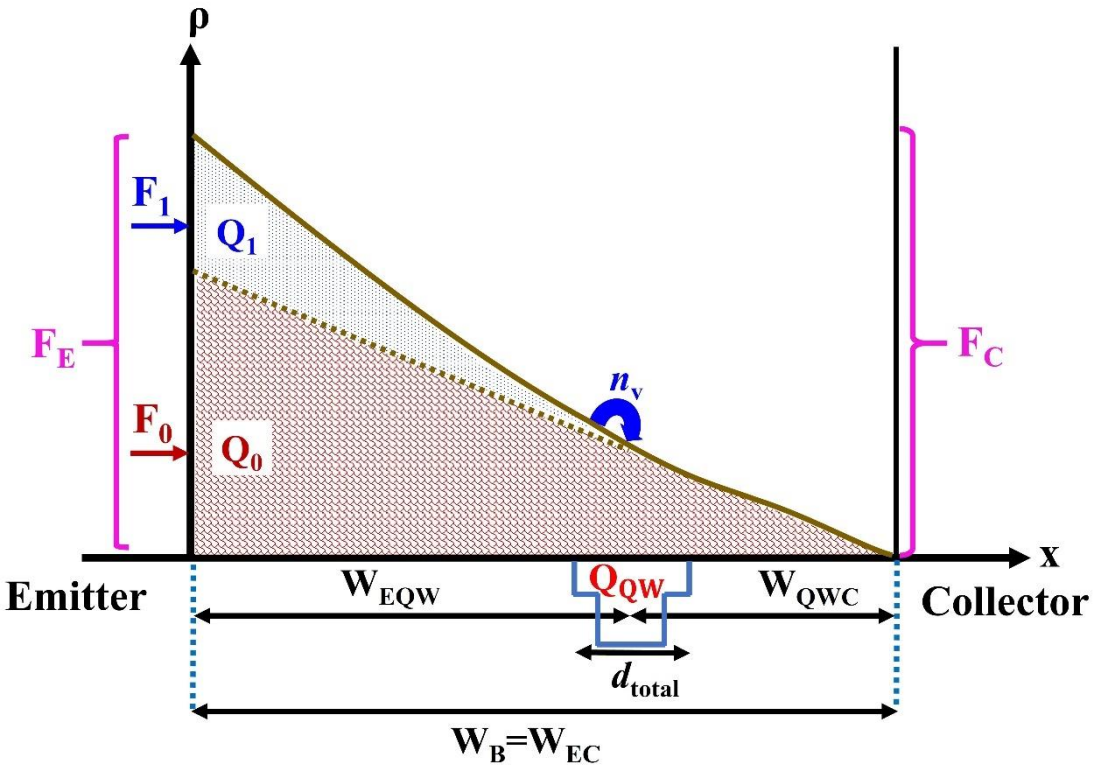


Fig. 2.13: A schematic diagram of the minority charge distribution (ρ) in the SQW-HBT.

The injection of minority electrons from the emitter to the QW region (denoted as the EQW region) can be described by integrating a one-dimensional diffusion equation. The rate equation for the surface charge density is given by the equations

$$\frac{\partial Q_1}{\partial t} = F_1 - \frac{Q_1}{\tau_b} - \frac{Q_1}{\tau_{t,EQW}} \tag{2.1a}$$

doi:10.6342/NTU202500212

$$\tau_{t,EQW} \approx \frac{W_{EQW}^2}{2D_n} \tag{2.1b}$$

Here, F_1 is the charge flux of electrons associated with Q_1 injected into the base from the emitter, τ_b is the bulk recombination lifetime of minority carriers in the heavily doped GaAs of the base, and $\tau_{t,EQW}$ is the transit time of minority carriers crossing the emitter to the QW region, which has a width W_{EQW}. D_n is the electron diffusion constant, assumed to be constant throughout the bulk GaAs material of the base. It is assumed that the electron diffusion length ($L_n \equiv (D_n\tau_b)^{1/2}$) is much longer than both the width of the base ($W_B = W_{EC}$) and the width of the emitter to QW region (W_{EQW}).

In the QW, the rate equation for charge Q_{QW} van be expressed as follows:

$$\frac{\partial Q_{QW}}{\partial t} = -\frac{Q_{QW}}{\tau_{QW}} + \frac{Q_1}{\tau_{t,EQW}} \tag{2.2a}$$

$$\frac{\mathrm{Q_1}}{\tau_{t,EQW}} = \frac{d_{total} q n_{\mathrm{v}}}{\tau_{cap}} - \frac{\mathrm{Q_{QW}}}{\tau_{esc}} \tag{2.2b}$$

Here, τ_{QW} refers to the recombination lifetime of electrons in the QW, d_{total} is the total thickness of the staircase QW, and τ_{cap} and τ_{esc} are the capture time of minority carriers in the QW from the virtual continuum state to the bound ones and escape time of minority carriers from the QW to the bulk GaAs base, respectively. n_{v} is the electron density in the virtual continuum conduction state, and q is the electron charge. Equation (2.2b) indicates that the injection rate into the QW can be calculated by considering the difference between the electron capture and escape rates, which are determined by the

doi:10.6342/NTU202500212

rate at which electrons leave the EQW region. As shown in Eqs. (2.2a) and (2.2b), Q_1 is responsible for supplying the minority carriers into the QW reservoir.

Now, we can now use the triangle similarity theorem, as shown in **Fig. 2.13**, to approximate qn_V by simplifying this expression $\left(1/2 \times qn_{\mathrm{v}} \times \mathrm{W_{QWC}}\right)/\mathrm{Q_0} = \left(\mathrm{W_{QWC}}/\mathrm{W_{EC}}\right)^2$, and we can express it more compactly as

$$qn_{\mathrm{v}} = \frac{2Q_0}{W_{QWC}}\left(\frac{W_{QWC}}{W_{EC}}\right)^2 \tag{2.3}$$

From Eqs. (2.1a) and (2.2a), under steady-state conditions where $\partial/\partial t \to 0$, we can express Q_1 as

$$Q_1 = \frac{\tau_{t,EQW}}{\tau_{QW}} Q_{QW} = \frac{F_1}{\frac{1}{\tau_b} + \frac{1}{\tau_{t,EQW}}} \tag{2.4}$$

Using Eqs. (2.2a) and (2.2b) in the steady-state condition, the surface charge density in the QW can be expressed in terms of n_{v} as

$$Q_{QW} = d_{total} qn_{\mathrm{v}} \left(\frac{\frac{1}{\tau_{cap}}}{\frac{1}{\tau_{esc}} + \frac{1}{\tau_{QW}}} \right) \tag{2.5}$$

With Eqs. (2.3) and (2.4), Q_1 can be written in terms of Q_0 as

$$Q_1 = \left[\frac{\tau_{t,EQW}}{\tau_{QW}} \frac{\frac{1}{\tau_{cap}}}{\frac{1}{\tau_{esc}} + \frac{1}{\tau_{QW}}} \left(\frac{W_{QWC}}{W_{EC}}\right)^2 \frac{d_{total}}{\left(\frac{W_{QWC}}{2}\right)} \right] Q_0 \tag{2.6}$$

Next, we substitute the Q_1 from Eq. (2.4) in the function of F_1 into Eq. (2.6) and evaluate the term F_1/F_0 as

doi:10.6342/NTU202500212

$$\frac{F_1}{F_0}=\frac{\tau_{t,EQW}}{\tau_{QW}}\frac{\frac{1}{\tau_{cap}}}{\frac{1}{\tau_{esc}}+\frac{1}{\tau_{QW}}}\frac{1+\frac{\tau_b}{\tau_{t,EQW}}}{1+\frac{\tau_b}{\tau_{EC}}}\left(\frac{W_{QWC}}{W_{EC}}\right)^2\frac{d_{total}}{\left(\frac{W_{QWC}}{2}\right)} \tag{2.7}$$

We can further express Eq. (2.7) in terms of current gains β_{EC}, β_{EQW}, and β_{QWC} of fictitious HBTs with respective base widths of W_{EC}, W_{EQW}, and W_{QWC}, as follows:

$$\beta_{EC}=\frac{\tau_b}{\tau_{t,EC}},\qquad \beta_{EQW}=\frac{\tau_b}{\tau_{t,EQW}},\qquad \beta_{QWC}=\frac{\tau_b}{\tau_{t,QWC}} \tag{2.8}$$

Using Eq. (2.8), we rewrite Eq. (2.7) as

$$\frac{F_1}{F_0}=\frac{\tau_b}{\tau_{QW}}\frac{\frac{1}{\tau_{cap}}}{\frac{1}{\tau_{esc}}+\frac{1}{\tau_{QW}}}\frac{d_{total}}{\left(\frac{W_{QWC}}{2}\right)}\frac{1}{\beta_{QWC}}\frac{1+\frac{1}{\beta_{EQW}}}{1+\frac{1}{\beta_{EC}}} \tag{2.9}$$

The emitter current, I_E, is given by the relation $I_E=AF_E$, where A is the device cross-section area, and the collector current, I_C, is expressed as $I_C=AF_C$. These can be written in terms of F_0 as

$$I_E=AF_E=A(F_1+F_0)=A\left(\frac{F_1}{F_0}+1\right)F_0 \tag{2.10a}$$

$$I_C=AF_C=A\frac{Q_0}{\tau_{t,EC}}=\frac{A}{\tau_{t,EC}}\frac{F_0}{\frac{1}{\tau_b}+\frac{1}{\tau_{t,EC}}}=\frac{AF_0}{1+\frac{1}{\beta_{EC}}} \tag{2.10b}$$

Using Eqs. (2.10a) and (2.10b), the base current $I_B=I_E-I_C$ can be derived as

$$\mathrm{I_B}=\mathrm{AF_0}\left[\left(1+\frac{\mathrm{F_1}}{\mathrm{F_0}}\right)-\frac{1}{1+\frac{1}{\beta_{\mathrm{EC}}}}\right] \tag{2.11}$$

By utilizing Eqs. (2.10b) and (2.11), we can determine the current gain $\beta\equiv I_C/I_B$. After cancelling the common factor, A and F_0, the expression of current gain β becomes:

doi:10.6342/NTU202500212

$$\beta = \frac{\beta_{EC}}{1 + (1 + \beta_{EC})\frac{F_1}{F_0}} \tag{2.12}$$

With Eq. (2.9), and considering $1/\beta_{EQW}$ has to be dropped, which is usually smaller than unity. The current gain β be reformulated as

$$\beta \approx \frac{\beta_{EC}}{1 + \frac{\beta_{EC}}{\beta_{QWC}}\frac{\tau_b}{\tau_{QW}}\frac{\frac{1}{\tau_{cap}}}{\frac{1}{\tau_{esc}} + \frac{1}{\tau_{QW}}}\frac{d_{total}}{\left(\frac{W_{QWC}}{2}\right)}} \tag{2.13}$$

The temperature-dependent behavior of the SQW-HBT is then analyzed using either Eq. (2.12) or (2.13). Using Eqs. (2.4) and (2.6), the ratio of surface charge density in the QW Q_{QW} to Q_0 is

$$\frac{Q_{QW}}{Q_0} = \frac{\frac{1}{\tau_{cap}}}{\frac{1}{\tau_{esc}} + \frac{1}{\tau_{QW}}}\left(\frac{W_{QWC}}{W_{EC}}\right)^2 \frac{d_{total}}{\left(\frac{W_{QWC}}{2}\right)} \tag{2.14}$$

Substituting Eq. (2.14) into the expression of current gain β in Eq. (2.13), we obtain a more physically insightful formulation:

$$\beta \approx \frac{\beta_{EC}}{1 + \frac{\beta_{EQW}}{\beta_{QWC}}\left(\frac{W_{EQW}}{W_{QWC}}\right)^2 \left(\frac{Q_{QW}/\tau_{QW}}{Q_0/\tau_b}\right)} \tag{2.15}$$

Examining Eq. (2.15), it is evident that if the QW is absent, i.e., Q_{QW}=0 in the base of the SQW-HBT, the current gain β simplifies to β_{EC}, which corresponds to that of a current gain value of the conventional HBT with a base width of W_{EC}. The value of β is diminished by a factor proportional to the ratio of minority carrier recombination rates in the QW (Q_{QW}/τ_{QW}) and the base region without a QW region (Q_0/τ_b). This implies that

doi:10.6342/NTU202500212

recombination of carriers in the QW occurs at a faster rate, leading to a reduction in the current gain (β).

This modified charge-control model facilitates the design of highly efficient epi-layers for LETs by allowing for adjustments to the QW design and the overall epitaxial layer structure. The final expression for the current gain can be employed to verify experimental results with acceptable temperature-dependent carrier transit times. This modified charge-control model for SQW-HBTs provides a deeper understanding of the device physics, particularly under high-temperature conditions, making it valuable for the development of smart thermal sensing technologies.

2.7 Modified Thermionic Emission Model

The classical thermionic emission theory, as initially developed by Schneider and Klitzing [65] and Nagarajan [66], serves as a foundation for understanding carrier behavior in QWs. In this model, carrier distribution within the QW is assumed to follow Boltzmann-like statistics, and the "tail" of this distribution above the QW barrier is identified as the escape current. Consequently, this classical approach only effectively estimates escape times for QW widths on the order of a few hundred Å. However, for our QWs structure in this dissertation, a modification to the escape time formula is required for accurate analysis. We need to modified the escape time, τ_{esc} formula as per

doi:10.6342/NTU202500212

Schneider and Klitzing's work [65]:

$$\tau_{esc} = \left(\frac{2\pi m^{*}_{e} d^2}{k_B T}\right)^{1/2} exp\left(\frac{E_B}{k_B T}\right) \quad (2.16)$$

where k_B is the Boltzmann constant, T is the temperature, m^{*}_{e} is the effective electron mass, *d* is the QW width, and E_B represents the band offset from the first sub-band to the conduction band.

Further studies [67] highlight that escape time in QWs has a competitive relationship with recombination lifetimes, involving a combination of direct tunneling, thermionic emission, and thermally assisted tunneling. This comprehensive model was refined using thermionic emission principles explored by Nelson et al. [67]. To begin, the injection current density, (J_e), is expressed as

$$J_e = e \int_0^{\infty} n(E) \times T(E) \times v(E)\ dE \quad (2.17)$$

where *n*(E) represents the carrier concentration at energy E, T(E) denotes the transmission probability, and *v*(E) is the escape velocity of the carriers. All these parameters depend on direction. The QW's one-dimensional basic electron band structure, illustrated in **Fig. 2.14**. Next, we integrate over all carrier populations in both the confined and unconfined states above the QW. Here, *n*(E) equals the product of the density of states g(E) and the distribution function f(E).

Finally, the carrier escape time, τ_e is determined by dividing the total carrier

doi:10.6342/NTU202500212

concentration in the QW $n_{QW} = n_e \times d$ (in cm^{-2}) by the injection current density:

$$\tau_e = \frac{n_{QW}}{J_e} = \frac{n_e d}{J_e} \tag{2.18}$$

The derived thermionic emission equation is as follows:

Since the QW is within a neutral region, the flux of J_e, emission from the QW in both directions, can be estimated by thermionic emission. The escape current density, *Je,* can be further simplified by assuming high transmission $T(E) \approx 1$, and $\{\hbar^2(k_t^2 + k_z^2)\}/2m^* + (E_{c,w} - E_F) \gg k_B T$ is as follows:

$$J_e$$

$$= 2\frac{2}{d}\frac{1}{A_W}\frac{dA_W}{(2\pi)^3}\int_{k_{z,min}}^{\infty} dk_Z \left(\frac{\hbar k_z}{m^*}\right)\int d\bar{k}_z \frac{1}{exp\{[\frac{\hbar^2({k_t}^2 + {k_z}^2)}{2m^*} + E_{c,w} - E_F]/k_B T\} + 1}$$

$$= \frac{1}{4\pi^2}\frac{\hbar}{m^*}\left(\frac{2m^* k_B T}{\hbar^2}\right)^2 e^{-(E_{c,w}-E_F)/k_B T} \tag{2.19}$$

In this Eq., *v* represents the carrier velocity $\hbar k_z/m^*$, *d* is the QW width, A_W is the area of QW, m* is the effective mass, k_z and k_t denote the wave numbers in the z-direction and continuum state, respectively, and $E_{c,w}$ and E_F are the QW's lowest conduction band and the Fermi level.

The carrier density n_w within the QW, inclusive of carriers in both bound sub-bands and continuum states, is given by:

doi:10.6342/NTU202500212

$$
\begin{aligned}
& n_w \\
& = \frac{2}{d}\frac{1}{A_w}\sum_{l=1}^{N_b}\frac{A_w}{(2\pi)^2}\int_0^{\infty} d\bar{k}_t \frac{1}{exp\{\frac{[(\hbar^2 {k_t}^2/2m^*)+E_l-E_F]}{k_BT}\}+1} \\
& + \frac{2}{d}\frac{1}{A_w}\frac{dA_W}{(2\pi)^3}\int_{k_{z,min}}^{\infty} d\bar{k}_z(z)\int d\bar{k}_t \frac{1}{exp\{\frac{[(\hbar^2 {k_t}^2/2m^*)+E_{c,w}-E_F]}{k_BT}\}+1}
\end{aligned}
\tag{2.20}
$$

where $\hbar^2 k_{z,min}^2/2m^* = \Delta E_b$, and N_b denotes the number of bound sub-bands. Assuming conduction band energy is significantly far away from the Fermi level; i.e.,$(E_{c,w}-E_F)/k_BT \gg 1$, the following approximation applies:

$$
\begin{aligned}
& n_w \\
& = \frac{1}{d}\frac{2}{2\pi}\sum_{l=1}^{N_b}\int_0^{\infty} dx\left(\frac{m^* k_B T}{\hbar^2}\right)\frac{1}{exp[x+\{(E_l-E_F)/K_BT\}]+1} \\
& + \frac{4}{(2\pi)^2}\int_{k_{z,min}}^{\infty} dk_Z(z)\int_0^{\infty} dk_t\, k_t exp\left\{\frac{-(E_{c,w}-E_F)}{k_BT}\right\}exp\left\{\frac{-\hbar^2(k_t^2+k_z^2)}{k_BT}\right\} \\
& = \frac{1}{d}\frac{1}{2\pi}\left(\frac{2m^* k_B T}{\hbar^2}\right)\sum_{l=1}^{N_b}\ln\left[1+exp\left\{\frac{-(E_l-E_F)}{k_BT}\right\}\right] \\
& + \frac{1}{4\pi^{2/3}}\left(\frac{2m^* k_B T}{\hbar^2}\right)^{3/2} exp\left\{\frac{-(E_{c,w}-E_F)}{k_BT}\right\} erfc\left(\sqrt{\frac{\Delta E_B}{k_BT}}\right)
\end{aligned}
\tag{2.21}
$$

where *erfc(x)* is the complementary error function, and $x = \hbar^2 k_t^2/2m^* k_B T$. Using the relation $erfx(x) = \int_x^{\infty} e^{-t^2}\, dt$, a reasonable approximation for $\sqrt{\Delta E_B/k_BT} \gg 1$ results in $erfc\left(\sqrt{\Delta E_B/k_BT}\right) \approx exp(-\Delta E_B/k_BT)/\left(\sqrt{\pi}\sqrt{\Delta E_B/k_BT}\right)$.

With the help of above assumption, n_w can be written as

doi:10.6342/NTU202500212

$$n_w \approx \frac{1}{d}\frac{1}{2\pi}\left(\frac{2m^* k_B T}{\hbar^2}\right)\sum_{l=1}^{N_B} ln\left[1+exp\left\{\frac{-(E_l-E_F)}{k_B T}\right\}\right] + \frac{1}{4\pi^2}\left(\frac{2m^* k_B T}{\hbar^2}\right)^{3/2}\sqrt{\frac{k_B T}{\Delta E_B}}\,exp\left\{\frac{-(E_{c,b}-E_F)}{k_B T}\right\} \tag{2.22}$$

Furthermore, if $(E_l - E_F)/k_B T \gg 1$ which implies that $exp\{-(E_l - E_F)/k_B T\} \ll 1$, we can express the total current density n_w as

$$n_w \approx \frac{1}{d}\frac{1}{2\pi}\left(\frac{2m^* k_B T}{\hbar^2}\right)\sum_{l=1}^{N_B} exp\left\{\frac{-(E_l-E_F)}{k_B T}\right\} + \frac{1}{4\pi^2}\left(\frac{2m^* k_B T}{\hbar^2}\right)^{3/2}\sqrt{\frac{k_B T}{\Delta E_B}}\,exp\left\{\frac{-(E_{c,b}-E_F)}{k_B T}\right\} \tag{2.23}$$

The escape time, τ_{esc} due to thermionic emission, modified by Eq. (2.18), becomes:

$$\tau_{esc} = d\left[\frac{1}{d}\frac{1}{2\pi}\left(\frac{2m^* k_B T}{\hbar^2}\right)\sum_{l=1}^{N_B} ln\left[1+exp\left\{\frac{-(E_l-E_F)}{k_B T}\right\}\right] + \frac{1}{4\pi^2}\left(\frac{2m^* k_B T}{\hbar^2}\right)^{3/2}\sqrt{\frac{k_B T}{\Delta E_B}}\,exp\left\{\frac{-(E_{c,w}-E_F)}{k_B T}\right\}\right] \times 4\pi^2\frac{m^*}{\hbar}\left(\frac{2m^* k_B T}{\hbar^2}\right)^{-2} exp\left\{\frac{-(E_{c,w}-E_F)}{k_B T}\right\} \tag{2.24}$$

If $(E_l - E_F)/k_B T \gg 1$, the escape time simplifies to:

$$\tau_{esc} \approx \frac{2\pi m^*}{\hbar}\left(\frac{2m^* k_B T}{\hbar^2}\right)^{-1} e^{\frac{(E_{c,b}-E_F)}{k_B T}}\sum_{l=1}^{N_b} e^{\frac{-(E_i-E_F)}{k_B T}} + \frac{m^* d}{\hbar}\left(\frac{2m^*\Delta E_B}{\hbar^2}\right)^{-1/2}$$

$$= \frac{2\pi m^*}{\hbar}\left(\frac{2m^* k_B T}{\hbar^2}\right)^{-1}\sum_{l=1}^{N_b} e^{\frac{(E_{c,w}-E_l)}{k_B T}} + \frac{m^* d}{\hbar}\left(\frac{2m^*\Delta E_B}{\hbar^2}\right)^{-1/2} \tag{2.25}$$

doi:10.6342/NTU202500212

We can also write as

$$\frac{1}{\tau_{esc}} \approx \frac{\frac{1}{\pi}\frac{k_B T}{\hbar}}{\frac{1}{2\pi}\left(\frac{k_B T}{\Delta E_B}\right) \times \frac{d}{\sqrt{\frac{\hbar^2}{2m^* \Delta E_B}}} + \sum_{l=1}^{N_b} e^{\frac{(E_{c,b}-E_l)}{k_B T}}} \tag{2.26}$$

where $\sqrt{\hbar^2/(2m^*\Delta E_B)}$ represents the length scale determined by ΔE_b.

Finally, to account for interactions between carriers and longitudinal optical (LO) phonons, we incorporate an additional term. This term acknowledges that LO phonons enhance the likehood of carrier escape from the QW by increasing escape rate. Thus, the modified escape time τ_{esc} becomes

$$\frac{1}{\tau_{esc}} \approx \frac{\frac{1}{\pi}\frac{k_B T}{\hbar}}{\frac{1}{2\pi}\left(\frac{k_B T}{\Delta E_B}\right) \times \frac{d}{\sqrt{\frac{\hbar^2}{2m^* \Delta E_B}}} + \sum_{l=1}^{N_b} e^{\frac{(E_{c,b}-E_l)}{k_B T}}} + \frac{1}{\tau_{LO}} \frac{1}{e^{\hbar\omega_{LO}/k_B T} - 1} \tag{2.27}$$

where $\hbar\omega_{\mathrm{LO}}$ is the LO phonon energy and τ_{LO} is the escape time due to phonon interactions.

Figure 2.14 presents the one-dimensional electron band diagram of the QW, clarifying the energy levels and carrier distribution across the confined and unconfined states. This modified thermionic emission model allows us to better understand carrier dynamics in QWs and offers insights into temperature-dependent behavior, essential for designing high-performance SQW-HBTs in thermal sensing applications.

doi:10.6342/NTU202500212

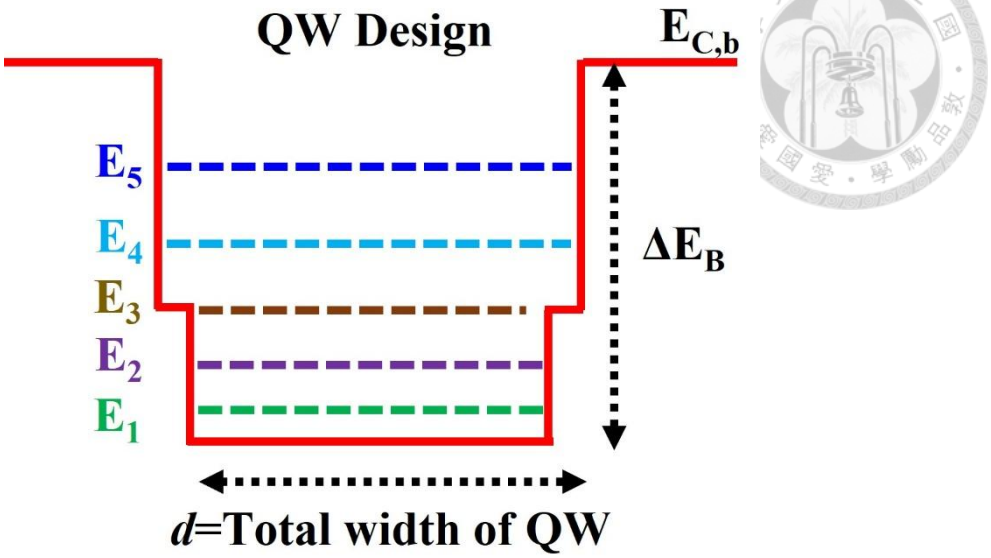


Fig. 2.14: Electron sub-band energy levels in a 1D Quantum-Well structure.

2.8 Validation of Experimental Results Using Modified Charge-Control Model for SQW-HBTs

The modified charge-control model for the SQW-HBTs has been validated through a comprehensive study of thermally enhanced current gain, comparing both experimental and simulation results. The device's performance was carefully measured over a temperature range from 25℃ to 85℃. The experimental I-V characteristics, shown in **Fig. 2.10**, and the observed current gain enhancement, illustrated in **Fig. 2.12**, confirm the model's predictions.

Simulation results further validate the unique temperature-dependent enhancement of current gain. **Figure 2.15** presents the experimental and simulation validation, demonstrating a strong agreement between the temperature-dependent current gain trends

doi:10.6342/NTU202500212

observed in both experiment and simulation. At a base current I_B of 0.2 mA, the simulated current gain trends match the experimental results closely across various temperatures.

Table 2.2 provides the parameter values used in the simulation at a base current I_B of 0.2 mA and a temperature, T =300 K.

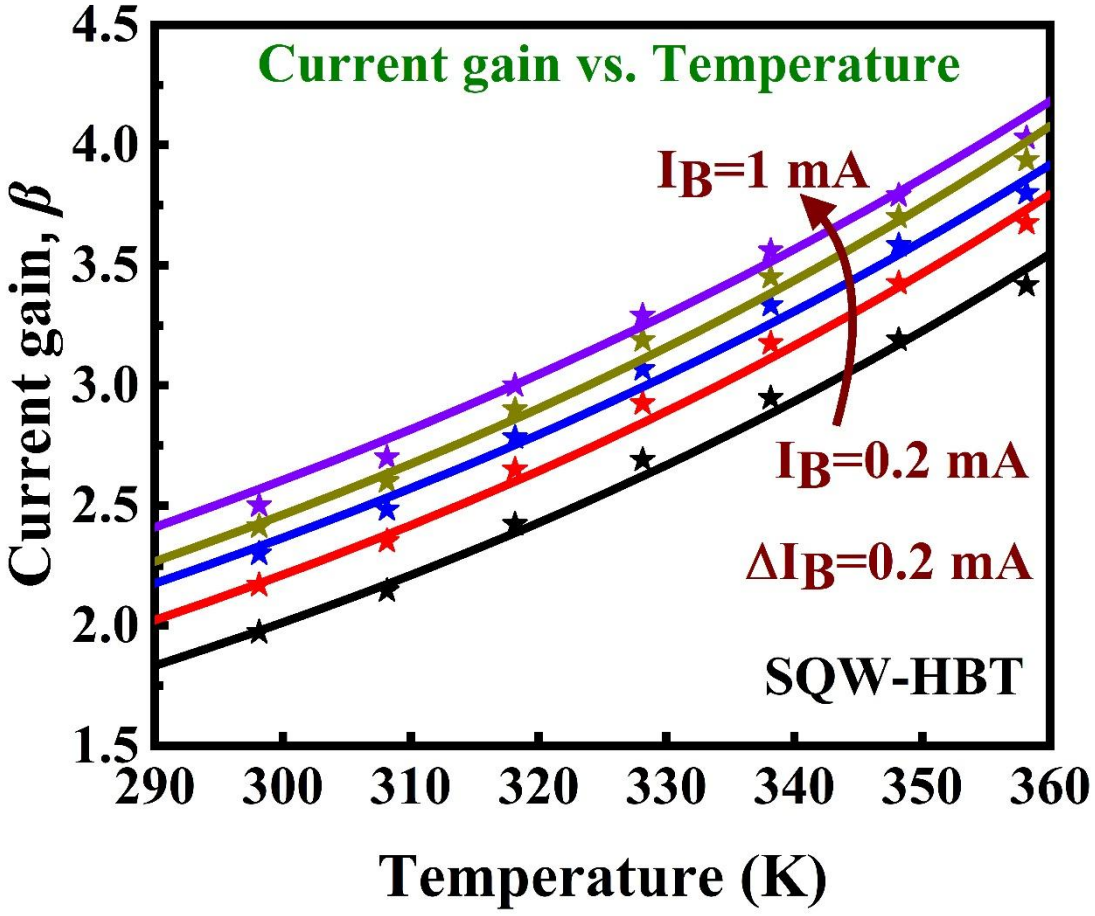


Fig. 2.15: Experimental measured current gain (stars) and simulated current gain (solid line) for the InGaP/GaAs SQW-HBT as a function of substrate temperature, T, measured at various base current, I_B ranging from 0. 2 mA to 1 mA.

Additionally, to further validate the model, we compared the simulation results with experimental data across various base currents, not limited to I_B of 0.2 mA, by linearly adjusting parameters dependent on temperature and base current. At higher temperatures,

doi:10.6342/NTU202500212

the internal heat generated by the device required more precise experimental calibration to accurately match experimental results with theoretical predictions. Despite this, the simulation results remain in good agreement with the experimental results, and the validation of the modified charge-control model is deemed successful. Finally, the agreement between experimental and simulation results demonstrates the reliability of the modified charge-control model for SQW-HBTs in predicting thermally enhanced current gain.

Table 2.2: Analysis of current gain at temperature, T=300 K with the following parameters

Parameter	**W_B**	**W_{EQW}**	***d_{total}***	**W_{QWC}**
Value (Å)	980	590	160	390
Parameter	$\tau_{t,EC}$	$\tau_{t,EQW}$	τ_b	$\tau_{t,QWC}$
Value (ps)	3.16	1.14	75.31	0.50
		QW		
Parameter	ΔE_B	$E_{c,b} - E_1$	$E_{c,b} - E_2$	$E_{c,b} - E_3$
Value (eV)	0.2876	0.2588	0.1859	0.0881
Parameter	τ_{cap}	τ_{QW}	τ_{esc}	
Value (ps)	0.65	108.9	278.68	

doi:10.6342/NTU202500212

2.9 Carrier Dynamics and Charge Analysis in QW and Base Regions

To investigate the temperature-dependent characteristics of current gain, understanding the carrier dynamics is very important, especially the capture, escape, and recombination times in the QW. Among these carrier times, thermionic emission plays a crucial role in distinguishing the unique temperature behavior of this device. The effect of thermionic emission on the escape time is highly sensitive to temperature, which is a key feature of this study.

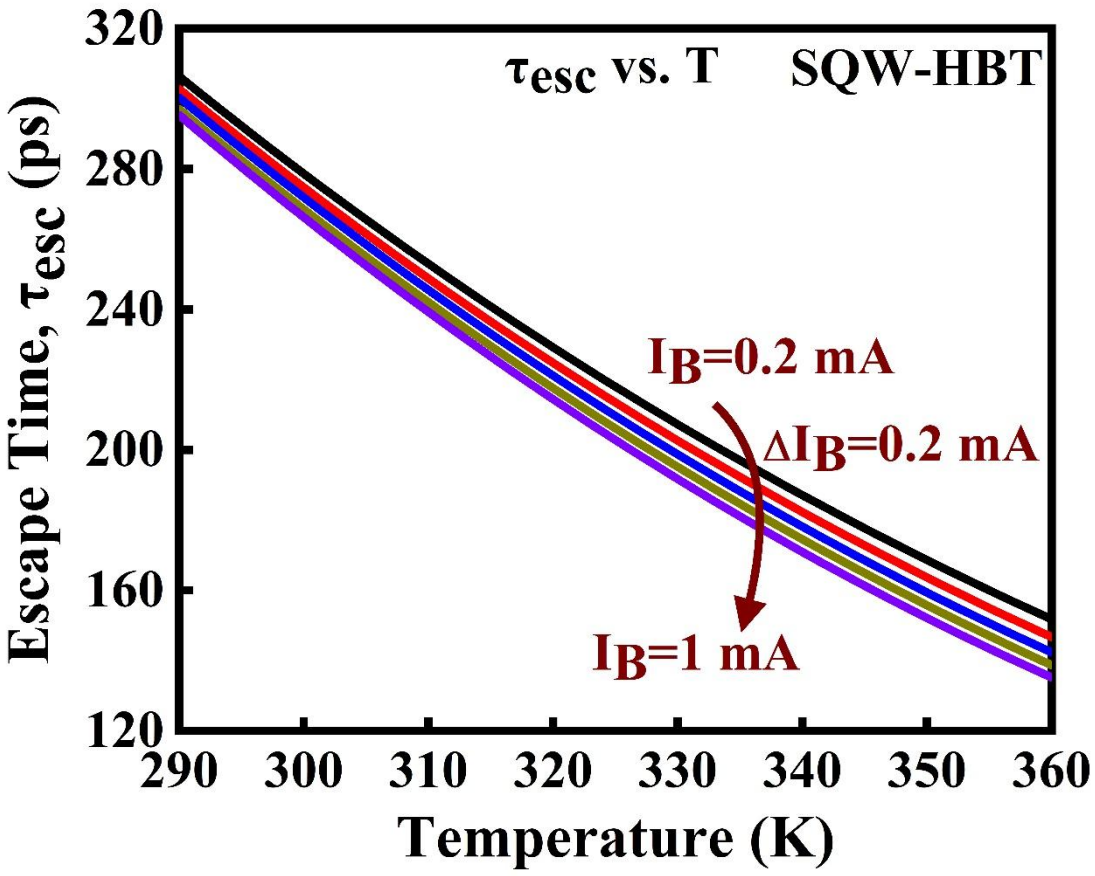


Fig. 2.16: Escape time, τ_{esc} in the QW as a function of temperature, T at various base current, I_B ranging from 0.2 mA to 1 mA.

doi:10.6342/NTU202500212

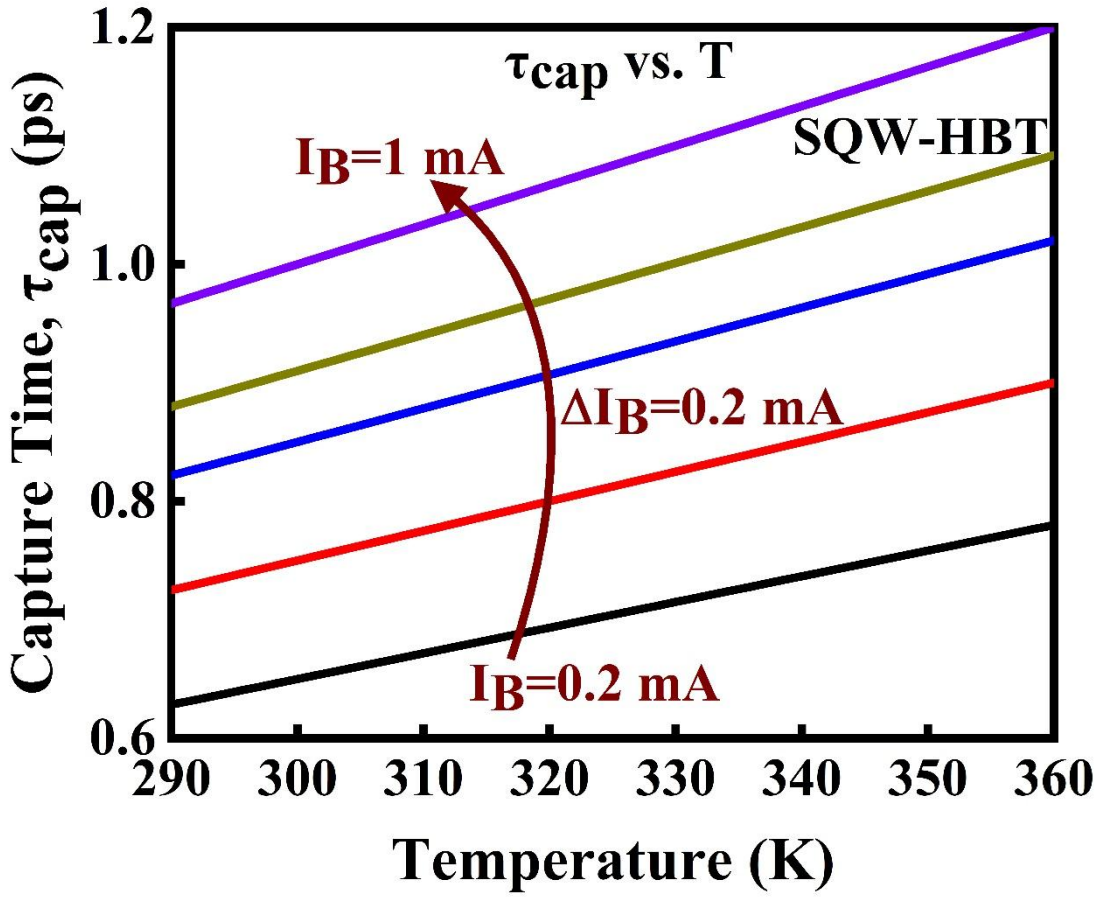


Fig. 2.17: Capture time, τ_{cap} in the QW as a function of temperature, T at various base current, I_B ranging from 0.2 mA to 1 mA.

As discussed in Subchapter 2.7, the modified thermionic emission model provides a more accurate framework for understanding the escape time characteristics within the QWs, highlighting the role of phonon interactions. This model enables better predictions of the thermal sensing behavior in SQW-HBTs at elevated temperatures. In this study, we employ Eq. (2.27), which incorporates Boltzmann statistics, to reformulate the analytical expression for the thermionic emission lifetime and estimate the escape time, τ_{esc} as a function of temperature at different base currents, I_B. The results are illustrated in **Fig.**

doi:10.6342/NTU202500212

2.16. As the electron temperature in the device increases, the band-filling effect causes the tail of the carrier distribution over the QW, leading to an exponential decrease in the escape time with both temperature and base current, I_B.

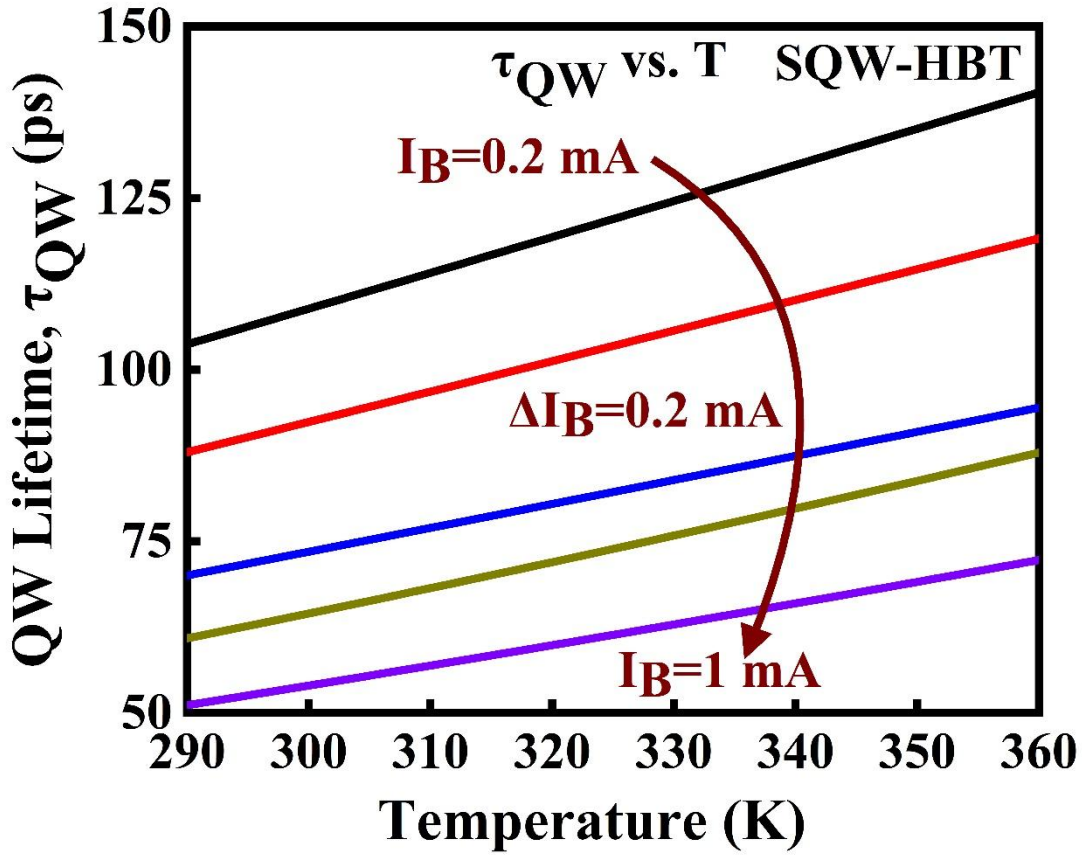


Fig. 2.18: Recombination lifetime, τ_{QW} in the QW as a function of temperature, T at various base current, I_B ranging from 0.2 mA to 1 mA.

To further analyze this behavior, we fit the experimental current gain to the theoretical current gain from Eq. (2.15), in order to extract the capture, τ_{cap} and recombination, τ_{QW} times as a function of temperature at different base current, I_B, as shown in **Figs. 2.17 and 2.18**, respectively. As both temperature and base current increase, carriers that

doi:10.6342/NTU202500212

transition from the bulk states to the quantum well states become increasingly blocked at accessible states, thereby increasing the time required to capture them. The capture time is also influenced by the operating current and voltage, as the Fermi wave vector increases with the base current, I_B, leading to a decreased scattering rate and, consequently, an increase capture time. Compared to the other timescales, the QW recombination and capture times are less sensitive to temperature than the escape time in the QW [68].

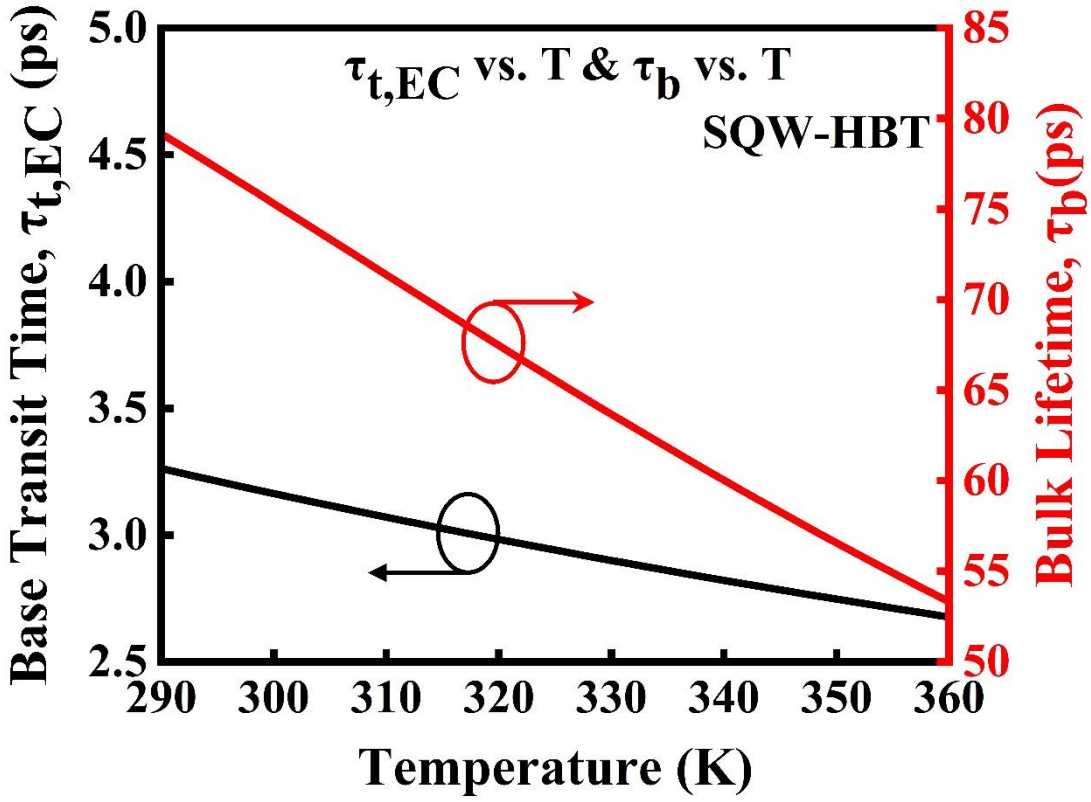


Fig. 2.19: Base transit time, $\tau_{t,EC}$ and bulk recombination time, τ_b as a function of temperature, T of SQW-HBT.

Figure 2.19 (solid black line) presents the variation of the base transit time, $\tau_{t,EC}$ as a function of temperature, T across the heavily p-doped $\left(\sim 3\times 10^{19}\ \text{cm}^{-3}\right)$ GaAs base. The

doi:10.6342/NTU202500212

base transit time is estimated using Einstein's relation $\left(D_n \equiv \mu_p^e k_B T/q\right)$, considering that the mobility of minority carriers has a weak dependence on higher temperatures [69], [70] . As shown in **Fig. 2.19**, as the temperature increases from 290 K to 360 K, the base transit time decreases by approximately 17.95%, indicating that the minority carrier mobility is less sensitive to temperature variations at higher temperatures.

Additionally, in **Fig. 2.19** (solid red line), we show the variation of the bulk recombination time, τ_b with temperature, T in heavily doped (p-type) bulk GaAs. The bulk recombination time is modeled using Shockley-Read-Hall (SRH) recombination, radiative recombination, and Auger recombination, as described by the following equation as

$$\tau_b = \left(\tau_{SRH}^{-1} + \tau_{rad}^{-1} + \tau_{Auger}^{-1}\right)^{-1} = (A_0 + B_0 P + C_0 P^2)^{-1} \quad (2.28)$$

where A_0 is the SRH coefficient, B_0 is the spontaneous emission coefficient, C_0 is the Auger recombination coefficient, and P is the doping concentration in the GaAs base. The recombination times τ_{SRH}, τ_{rad}, and τ_{Auger} represent the SRH, radiative, and Auger recombination times, respectively. In our temperature-dependent charge control model, we assume that the SRH recombination time, τ_{SRH} remains constant due to its typically longer value compared to the other recombination times. The radiative recombination lifetime, τ_{rad} depends on the spontaneous emission coefficient, B_0, which is

doi:10.6342/NTU202500212

proportional to T^{-1} in the QW and $T^{-3/2}$ in the bulk GaAs base [71], [72]. Auger recombination becomes dominant in heavily doped semiconductors due to both high impurity concentration and carrier density. The impact ionization is inversely related to this process. In non-degenerate semiconductors, the threshold kinetic energy, E_{th} for energetic holes is strongly temperature-dependent during the band-to-band Auger recombination process. As the bandgap, E_g narrows at higher temperatures, the threshold energy, E_{th} is lowered, which increases the Auger recombination coefficient, C_0 [73]. **Figure 2.19** (solid red line) illustrates that the total recombination in the heavily doped base, characterized by the recombination lifetime, τ_b changes by approximately 32.66% as the temperature, T increases from 290 K to 360 K. This indicates that Auger recombination becomes dominant over the bulk recombination time at higher temperatures.

To understanding the charge analysis in the QW, it is important to understand the role of the QW in the fabricated SQW-HBT device. The incorporated QW in the base region of the transistor functions as a reservoir for capturing electrons transmitted from the emitter to the collector. The escape time of electrons from the QW is strongly influenced by temperature. As the temperature increases, the escape time decreases exponentially with $(K_B T)^{-1}$, enabling electrons in the QW to acquire sufficient energy and escape more rapidly to rejoin the base region of the transistor. At elevated temperatures, this process

doi:10.6342/NTU202500212

becomes even more pronounced, with additional electrons contributing to the base charge, Q_0 region which are subsequently swept to the collector through the reverse base-to-collector (B-C) process. This increase in electron flow enhances the collector current, $I_C = AQ_0/\tau_{t,EC}$, and the current gain, $\beta = I_C/I_B$. As a result, both the collector current and the current gain of the SQW-HBT exhibit significant sensitivity to temperature variations.

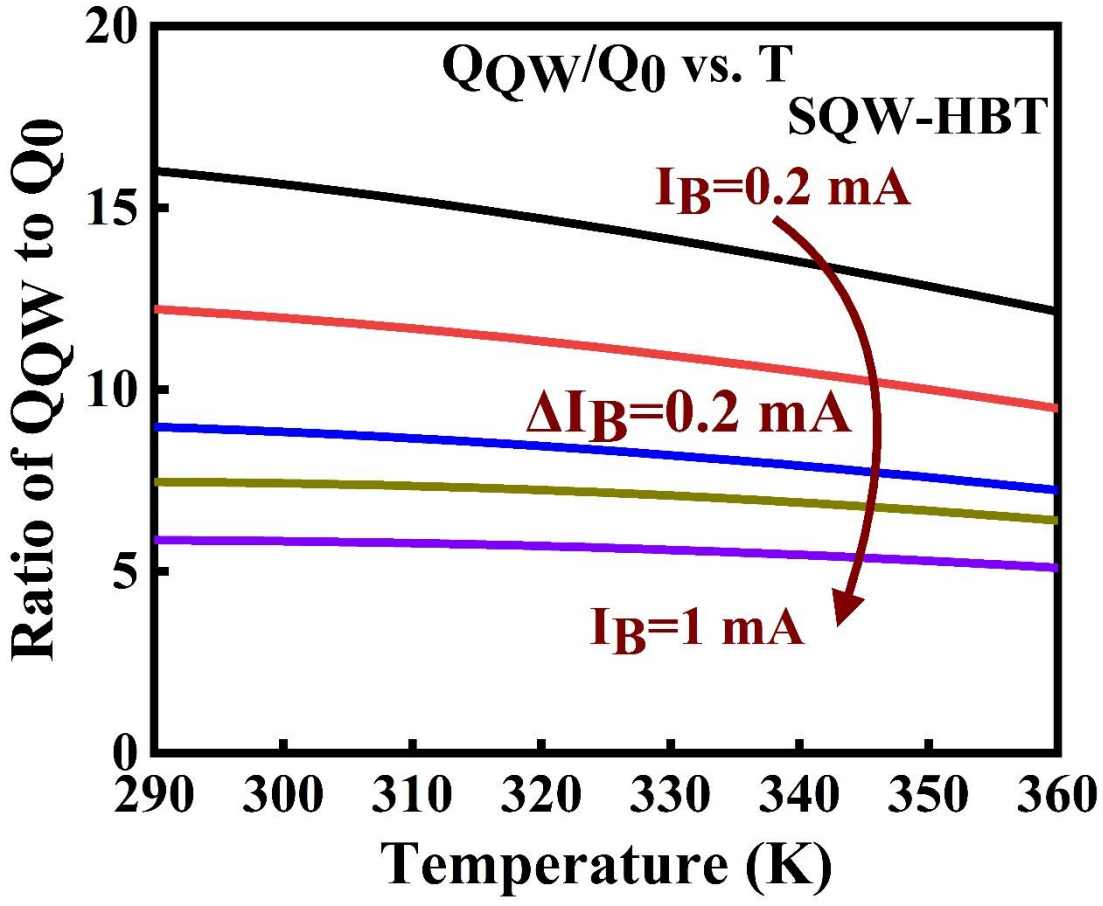


Fig. 2.20: Theoretical calculation from Eq. (2.14) showing the temperature-dependent ratio between Q_{QW} and Q_0 at different base currents, I_B ranging from 0.2 mA to 1 mA.

The theoretical framework presented in Eq. (2.14) for calculating the temperature-

doi:10.6342/NTU202500212

dependent charge ratio tends to underestimate the charge analysis in the QW relative to the base region without the QW. The theoretical results derived from this equation indicate that the ratio between Q_{QW} (charge in the QW) and Q_0 (charge in the base) decreases with increasing temperature, T and base current, I_B, as shown in **Fig. 2.20**. This analysis employs the same parameter values as those used in **Fig. 2.15**. This unique temperature-dependent enhancement of current gain presents a promising candidate for the development of the front-end designs of advanced smart temperature sensors. Furthermore, it facilitates the potential integration of these devices into OEICs, paving the way for innovative applications in next-generation thermal sensing technologies.

2.10 Conclusion

This chapter successfully introduced LETs incorporating staircase SQWs in the base region and investigated their temperature-dependent current gain behavior under varying substrate temperatures. Experimental measurement demonstrated a significant increase in collector current by approximately 73.23%, at a base current of I_B of 0.2 mA and a collector-to-emitter voltage, V_{CE} of 2 V, as the substrate temperature increased from 25°C to 85°C. This trend, opposite to the behavior observed in conventional HBTs, is attributed to the repaid escape of electrons from the InGaAs QW at elevated temperatures.

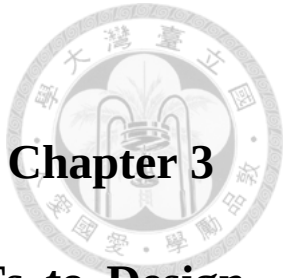
To understand this unique behavior, a modified charge-control model incorporating QW

doi:10.6342/NTU202500212

thermionic emission theory was proposed to account for temperature-dependent carrier dynamics. The experimental data closely aligned with simulation results, validating the accuracy of the proposed model. This study highlights the distinct thermal behavior of SQW-HBTs compared to traditional HBTs, wherein the current gain increases with temperature in the 25 ℃ to 85 ℃ range due to the reduced electron escape time in the QW.

This distinctive characteristic sets SQW-HBTs apart from conventional HBTs and positions them as promising candidates for the designing novel smart front-end thermal sensors. The modified charge-control model aids in designing efficient layer structures for staircase SQW-HBTs, enabling optimization of QW position, shape, size, and width within the transistor base. These advancements pave the way for future innovation in thermal sensor technology, offering new opportunities for high-precision smart thermal sensing applications.

doi:10.6342/NTU202500212



Chapter 3

From Analytical Modeling of MQW-HBTs to Design and Fabrication of TQW-HBTs for Thermal Sensing Applications

3.1 Introduction

The incorporation of MQWs within the base of HBTs has revolutionized the development of highly thermally sensitive LETs, offering a unique platform for thermal sensing applications.

This chapter delves into the analytical modeling, design, fabrication, and experimental validation of triple-quantum-well heterojunction bipolar transistors (TQW-HBTs), focusing on their enhanced thermal sensitivity and current gain characteristics. The primary objective is to enhance the understanding of MQW-HBTs and develop a thermally sensitive TQW-HBT device by leveraging advanced modified charge-control models and innovative fabrication processes. The chapter begins by establishing the motivation behind analytical modeling for MQW-HBTs and the development of highly thermal-sensitive TQW-HBTs (Subchapter 3.2). It then provides a comprehensive account of the development of charge-control models in MQW-based LETs and TLs

doi:10.6342/NTU202500212

(Subchapter 3.3), culminating in the necessity for a modified charge-control model tailored to MQW-HBTs (Subchapter 3.4). The analysis extends to the impact of MQWs on current gain, with a detailed examination of the effect of QW position and number on charge dynamics and gain performance (Subchapter 3.5). The insights gained from this study guide the design and fabrication of the TQW-HBT device, with specific emphasis on optimizing the device layer structure and fabrication processes (Subchapter 3.6). Subsequent sections highlight the characterization of the fabricated TQW-HBT at varying substrate temperatures (Subchapter 3.7), validating the proposed modified charge-control model (Subchapter 3.8) and thermionic emission model for TQW-HBT including with parameter extraction related to carrier dynamics such as carrier recombination and transit times (Subchapter 3.9). It also discussed the charge dynamics within the TQWs and the base region, followed by a comparison of simulated and experimental results to validate the current gain in TQW-HBTs (Subchapter 3.10). Finally, the chapter concludes by summarizing the key findings and their implications for advancing the design of thermal-sensitive devices (Subchapter 3.11). The outcomes of this research, including the development of modified charge-control models and their experimental validation, underscore the importance of TQW-HBTs in next-generation thermal sensing technologies. Notably, the findings have been published in two high-impact journals *IEEE Transactions on Electron Devices* in the following papers:

doi:10.6342/NTU202500212

1) Mukul Kumar et al., “Analytical modeling of current gain in multiple-quantum-well heterojunction bipolar light-emitting transistors,” *IEEE Trans. Electron Devices*, vol. 71, no. 1, pp. 343–349, Jan. 2024, doi:10.1109/TED.2023.3289930.
2) Mukul Kumar et al., “Current gain enhancement at high-temperature operation of triple-quantum-well heterojunction bipolar light-emitting transistor for smart thermal sensor application,” *IEEE Trans. Electron Devices*, vol. 71, no. 1, pp. 896–903, Jan. 2024, doi:10.1109/TED.2023.3339084.

This chapter lays the groundwork for understanding the thermal and electrical properties of TQW-HBTs, demonstrating their potential in OEICs and high-resolution smart thermal sensing applications.

3.2 Motivation Behind Analytical Modeling for MQW-HBTs and Development of Highly Thermal Sensitive TQW-HBTs

Chapter 2 examined the thermal behavior of SQW-HBTs for thermal sensing applications, emphasizing the significant role of thermionic emission properties in QWs. Achieving high sensitivity and accuracy is critical to advancing the field of smart thermal sensing technologies. To enhance thermal sensitivity, optimizing QW design is essential to developing an efficient epi-layer structure for LETs. LETs, with their dual electrical

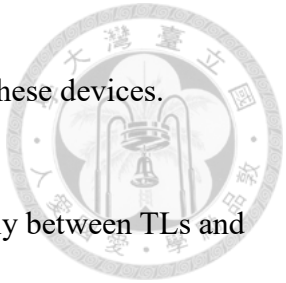
doi:10.6342/NTU202500212

and optical outputs, exhibit great potential for high-amplification and high-frequency operation. Incorporating QWs into the transistor base facilitates radiative output, while integrating multiple QWs further enhances radiative performance, culminating in the development of multiple-quantum-well heterojunction bipolar transistors (MQW-HBTs), novel class of high-speed, three-port light-emitting devices.

Initial research into MQW-HBTs revealed challenges, particularly a reduction in current gain. This reduction is attributed to high spontaneous recombination due to the incorporation of MQWs in the transistor base and modifications in charge carrier distribution within the base region. These factors negatively impacted the device's I-V characteristics and current gain, resulting in a performance hierarchy: $\beta_{MQW\text{-}HBT} < \beta_{SQW\text{-}HBT} < \beta_{HBT}$. Such limitations hindered the practical application of MQW-HBT due to their lower current gain compared to SQW-HBTs and conventional HBTs.

Recent studies have addressed these limitations, revitalizing interest in MQW-HBTs by demonstrating an improved trade-off between differential optical gain and collector current gain. These developments position MQW-HBTs as a promising candidate for high-optical-bandwidth applications. While optical characterization in MQW-based TLs has been extensively studied, the electrical current gain of MQW-HBTs has not been thoroughly investigated, presenting an opportunity for further investigation. Subchapter

doi:10.6342/NTU202500212

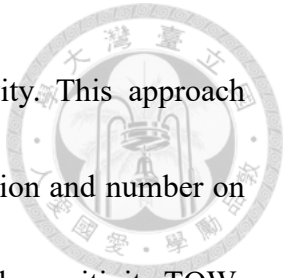


3.3 provides a detailed examination of existing analytical models of these devices.

The current gain modeling of MQW-based devices differs significantly between TLs and LETs due to their distinct operational principles. In TLs, the current gain equation incorporates factors such as carrier injection, recombination, and optical gain, reflecting their dual purpose of signal amplification and coherent light generation. Parameters such as population inversion and stimulated emission dominate in TL modeling. Conversely, for MQW-HBTs, the current gain equation primarily focuses on carrier injection and recombination, as these devices are optimized for light emission rather than signal amplification. Analytical modeling of current gain for MQW-HBTs focuses on parameters such as radiative recombination, light extraction, and carrier transport within MQWs, which distinguishes them from MQW-based TLs. To date, limited research has been reported on the electrical current gain of MQW-HBTs, with most studies focusing on optical characterization in MQW-based TLs, such as optical modulation. This gap highlights the need for a comprehensive analytical model that addresses both electrical and thermal performance parameters for MQW-HBTs.

This chapter presents an analytical model to calculate the current gain ($\beta_{MQW\text{-}HBT}$) of MQW-HBTs, employing one-dimensional diffusion equations and a modified charge-control model. The proposed model incorporates thermionic emission and optimized

doi:10.6342/NTU202500212



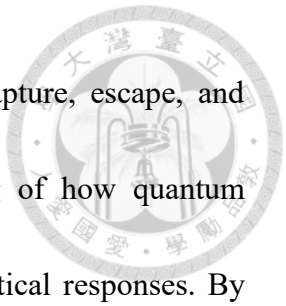
MQW positioning to maximize current gain and thermal sensitivity. This approach provides a systematic method for evaluating the effects of QW position and number on current gain. Additionally, the model forms the basis for designing high-sensitivity TQW-HBTs. Analytical modeling of MQW-HBTs offers insights into thermal characteristics and carrier transport dynamics under high-temperature operations. The motivation behind this work is to guide the development of LETs with thermally enhanced current gain and collector current, contributing to next-generation smart thermal sensor technology. By addressing existing knowledge gaps, this study contributes to the development of next-generation high-precision, smart thermal sensing devices.

3.3 Development of Charge-Control Models in MQW-Based LETs and TLs

The development of charge-control models for MQW-based LETs and TLs has evolved significantly over the years, reflecting the continuous advancements in theoretical frameworks, experimental techniques, and material innovations. This section systematically outlines the progress made in MQW-based device modeling.

In 1995, McDonald and O'Dowd laid the groundwork for advanced carrier dynamics modeling by introducing a three-level rate equation framework for QW-based lasers [74]. This model incorporated gateway or virtual states, bridging the gap between bulk carrier

doi:10.6342/NTU202500212



regions and QWs, and accounted for processes such as carrier capture, escape, and diffusion. This framework provided a fundamental understanding of how quantum confinement and localized states influence charge transport and optical responses. By treating carriers in QWs, barriers, and gateway states as distinct carrier populations, McDonald and O'Dowd established a basis for comprehending complex charge-control mechanisms in MQW devices.

Recent research highlights the potential of MQWs integrated into transistor base for high-optical bandwidth modulation. MQWs improves the trade-off between differential optical gain and collector current gain, making them attractive for advanced modulation applications. Several models have been proposed to explain phenomena such as fast carrier recombination in these devices.

In 2007, M. Feng et al. [57] and H. W. et al. [56] developed the basic charge-control models for TLs and LETs, respectively. Feng et al. modified these models using a two-level rate equation framework for QW-based TLs. They addressed the shortcomings of earlier models by emphasizing the differences between bulk and QW carriers in their carrier rate equations. Their work demonstrated that spontaneous recombination and carrier trapping significantly affect the current gain and modulation response of QW-TLs, laying the groundwork for small-signal and large-signal modulation analysis.

Subsequent advancements introduced more complex models, incorporating diffusion

doi:10.6342/NTU202500212

effects, QW capture and escape lifetimes, virtual states localized within QWs, and laser rate equations. These models enabled the development of small-signal modulation bandwidth frameworks [58], [75], [76]. Detailed studies on SQW-based LETs and TLs, including modulation characteristics, are discussed in Subchapter 2.5.

Research into MQWs has explored their impact on optical bandwidth [60], [77], [78], [79]; resonance-free modulation [80]; threshold-base current [81], [82]; imbalanced carrier and photon density distribution [83]; distortion characteristics [84]; modal gain [85]; and nonlinear gain models [86] in TLs. Additionally, the role of tunnel injection layers in MQW-TLs has been examined [87], [38].

S. Piramasubramanian et al. [88] studied the effect of QW position on distortion and modulation bandwidth. However, these studies primarily focused on TLs and their current gain characteristics. TLs and LETs differ in device structures, operational principles, and performance requirements, leading to distinct current gain equations for each.

To date, no research has comprehensively reported the electrical current gain of MQW-HBTs, as most studies emphasize the optical characterization of MQW-TLs, such as optical modulation. This knowledge gap underscores the need for a charge-control model that integrates MQWs into base of transistor. Such a model would support the design of

doi:10.6342/NTU202500212

optimized epitaxial layer structures for LETs, enhancing their applicability in thermal sensor technologies and other QW-based applications.

3.4 Modified Charge-Control Model and Current Gain Analysis for MQW-HBTs

To investigate thermally enhanced current gain in MQW-HBTs-based structure, it is essential to develop a modified charge-control model based on the thermionic emission of charge carriers in MQWs. The unique structural difference between QW-based devices with SCH and MQW-HBTs lies in the charge profile of the minority carrier distribution within the transistor's active base region. In MQW-HBTs, the incorporation of MQWs in the base leads to a triangular minority carrier charge distribution, with a steep incline near the collector end of the base. This is in contrast to the stored-charge distribution in SCH-based structures, which arises as a result of transistor operation. When an MQW-HBT operates in active forward mode, the high electric field at the base-collector (B-C) junction rapidly sweeps minority charge carriers from the active base region into the collector, resulting in an approximately zero minority carrier density at this B-C interface.

The basic charge-control models for LETs and TLs were initially reported by Then et al. [56] and Feng et al. [57] in 2007. Building on this work, subsequently in 2019, our research team reported a modified charge-control model for square SQW-HBTs [53].

doi:10.6342/NTU202500212

This dissertation also discusses the modified charge-control model of staircase SQW-HBTs [89] in Subchapter 2.6 which was reported in 2023. These models analyzed the thermal characteristics of the current gain (β) and the behavior of minority carriers surrounding the SQW. Detailed derivations and discussions of this modified staircase SQW-HBT charge-control model is presented in Subchapter 2.6. Building on this foundation, this study focuses on understanding the effect of MQWs in the transistor base on the current gain (β).

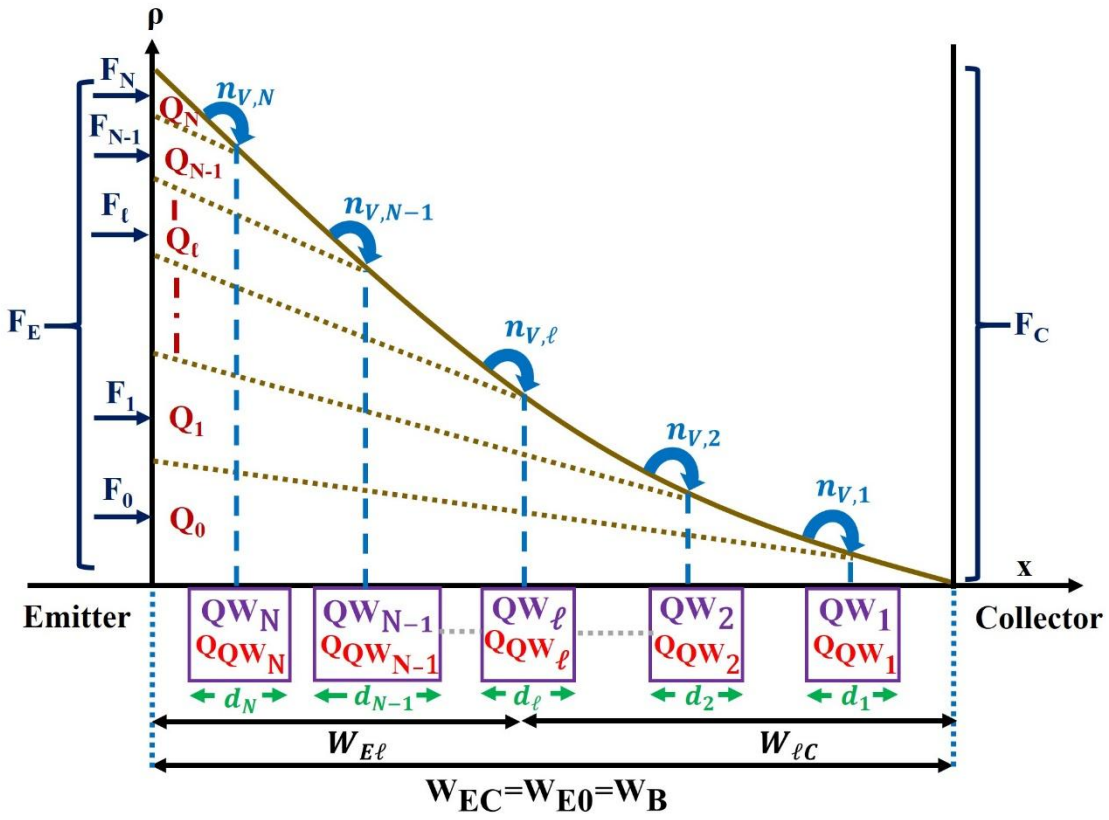


Fig. 3.1: Schematic representation of the minority carrier distribution (ρ) in the base region of an MQW-HBT.

doi:10.6342/NTU202500212

In this chapter, we propose a modified charge-control model for calculating the current gain (β) of MQW-HBTs. **Figure 3.1** illustrates the modified charge-control model for an N-number of QWs integrated into the transistor base, showing the volume charge density of the minority carrier distribution (ρ) in the base region of MQW-HBT. Additionally, **Fig. 3.2** presents an example of a real band diagram for MQW-HBTs, specifically for an InGaP/GaAs MQW-HBT structure.

The total charge of minority carriers in the transistor base is divided into three distinct sections:

I. Without QWs in the base: When no QWs are present, minority carriers diffuse directly from the emitter to the collector through the active base region. This diffusion contributes to the collector current, I_C, and is represented as Q_0. The distribution of Q_0 diminishes to zero at the B-C junction.

II. With N-number of QWs in the base: When N-number of QWs are incorporated into the base, portions of the minority charge carriers are captured by these QWs. The carriers diffusing from the emitter to successive QWs are represented by Q_1, Q_2, ….., Q_{N-1}, Q_N, corresponding to carriers captured at QW_1, QW_2, ……, QW_{N-1}, QW_N, respectively. Here, QW_1 is the first QW closest to the collector, and

doi:10.6342/NTU202500212

QW_N is n^{th} QW nearest to the emitter. The minority charge carrier distribution (Q_i: i: 1 to N) becomes zero at each QW location.

III. Charge stored in the N-number of QWs: A portion of the minority carriers is stored within the N-number of QWs. These stored charges are denoted as Q_{QW_1}, Q_{QW_2}, ……, $Q_{QW_{N-1}}$, Q_{QW_N}. For instance, Q_{QW_1} represents carriers stored in QW_1, Q_{QW_2} represents carriers stored in QW_2, and so on. Similarly, Q_{QW_N} accounts for the carriers stored in Q_{QW_N}.

This modified charge-control model incorporates the presence of MQWs in the transistor base, provides a comprehensive framework for understanding the interaction of minority charge carriers with MQWs in the base region, and influences the current gain by designing QWs such as position, shape, width, and barrier height, offering a foundation for designing efficient, optimized epitaxial structures for MQW-HBTs for thermal sensing applications.

To study the current gain analysis in the presence of MQW in the base region of HBTs, this modified charge-control model is useful for developing the analytical derivation of the current gain for MQW-HBTs. The analytical framework developed herein is validated against previously reported experimental data by Chang et al. [53] and Yang et al. [90],

doi:10.6342/NTU202500212

obtained from two different epi-layer wafers. Furthermore, we investigate the influence of QW positioning on both the current gain and QW charge distribution.

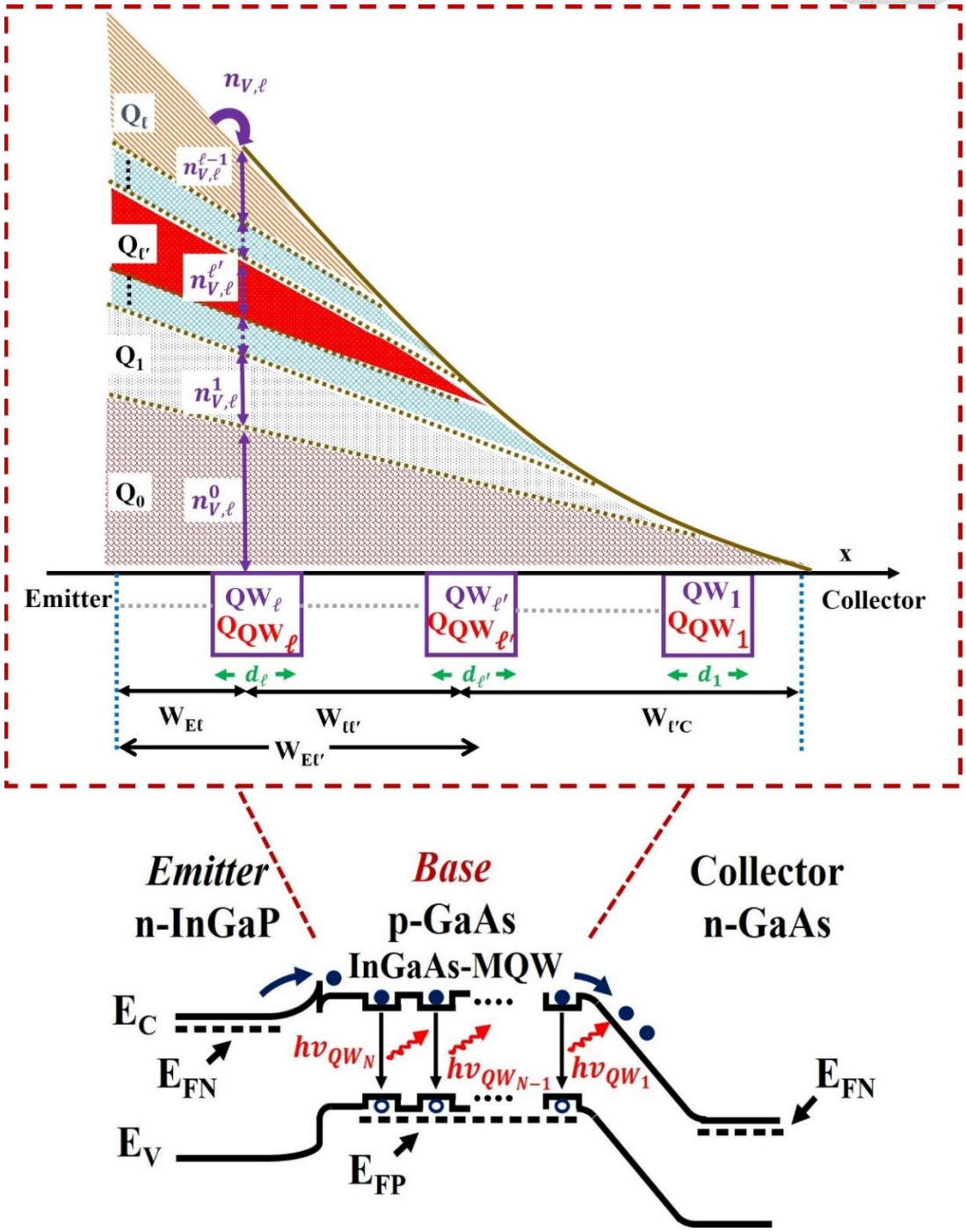


Fig. 3.2: Energy band diagram of the InGaP/GaAs MQW-HBT. The inset illustrates the calculation of the virtual state density ($n_{v,\ell}$) of the QW_ℓ in the base region of the MQW-HBT.

doi:10.6342/NTU202500212

The rate equation governing the charge, Q_ℓ, within a specific emitter to QW region is derived by integrating the one-dimension diffusion equation for minority carrier electrons injected from emitter to the QW_ℓ region. The resulting expression is as follows:

$$\frac{\partial Q_\ell}{\partial t} = F_\ell - \frac{Q_\ell}{\tau_b} - \frac{Q_\ell}{\tau_{t,E\ell}}, \tag{3.1a}$$

$$\tau_{t,E\ell} \approx \frac{W_{E\ell}^2}{2D_n}, \tag{3.1b}$$

where F_ℓ represents the electron flux injected from the emitter to the base and associated with Q_ℓ; τ_b and $\tau_{t,E\ell}$ are the recombination lifetime of minority carriers in bulk GaAs and transit time of electrons across the emitter-to-QW_ℓ region of width $W_{E\ell}$, respectively. $W_{E\ell}$ represents the width between the emitter-to-QW_ℓ. Here, D_n denotes the diffusion constant of electrons, which is assumed to remain constant within bulk GaAs. Equation (3.1a) describes the dynamic behavior of Q_ℓ, while Eq. (3.1b) provides an approximation of the electron transit time under the assumption that the minority carrier diffusion length ($L_n \equiv \sqrt{D_n \tau_b}$) exceeds both the base width (W_B) and the emitter-to-QW separation.

The rate equation of the charge within QW_ℓ, Q_{QW_ℓ}, is described as

$$\frac{\partial Q_{QW_\ell}}{\partial t} = -\frac{Q_{QW,\ell}}{\tau_{QW,\ell}} + \frac{Q_\ell}{\tau_{t,E\ell}}, \tag{3.2a}$$

doi:10.6342/NTU202500212

$$\frac{Q_\ell}{\tau_{t,E\ell}} = \frac{d_\ell q n_{V,\ell}}{\tau_{cap,\ell}} - \frac{\mathrm{Q_{QW_\ell}}}{\tau_{esc,\ell}}, \tag{3.2b}$$

In these Eqs. (3.2a) and (3.2b), $\tau_{\mathrm{QW},\ell}$ represents the recombination lifetime of minority carriers within the QW_ℓ and d_ℓ denotes the thickness of QW_ℓ. The term q refers to the electronic charge, while $n_{\mathrm{v},\ell}$ indicates the minority carrier density of virtual conduction states in QW_ℓ. Additionally, $\tau_{\mathrm{cap},\ell}$ denotes the capture time of minority carriers transitioning from virtual conduction states ($n_{\mathrm{v},\ell}$) to bound states within QW_ℓ and $\tau_{\mathrm{esc},\ell}$ denotes the escape time of minority carriers leaving the intrinsic QW_ℓ into the doped base. The net injection rate of minority carriers into the QW_ℓ is determined by the difference between the rates of minority carrier capture and escape. Equation (3.2b) quantifies the net injection rate of the electrons into the QW_ℓ, derived from the rate of electrons transitioning from the emitter region to QW_ℓ. Both Eqs. (3.2a) and (3.2b) demonstrate that the role of Q_ℓ to facilitate the injection of minority carriers into the reservoir of QW_ℓ.

At steady-state ($\partial/\partial \mathrm{t} \rightarrow 0$), the Eqs. (3.1a) and (3.2b) simplify, leading to the expression for Q_ℓ as

$$Q_\ell = \frac{F_\ell}{\frac{1}{\tau_b} + \frac{1}{\tau_{t,E\ell}}} = \mathrm{Q_{QW_\ell}} \frac{\tau_{t,E\ell}}{\tau_{QW,\ell}}. \tag{3.3}$$

At steady-state condition with Eq. (3.2b), the surface charge density within the QW_ℓ is further related to the volume density of QW_ℓ ($\mathrm{n_{v,\ell}}$) as

doi:10.6342/NTU202500212

$$Q_{QW_\ell} = \frac{\frac{1}{\tau_{cap,\ell}}}{\frac{1}{\tau_{QW,\ell}} + \frac{1}{\tau_{esc,\ell}}} d_\ell q n_{V,\ell}. \quad (3.4)$$

Using geometric considerations and the similarity of charge distributions within the QWs, the carrier density

In **Fig. 3.2**, the term $n_{\mathrm{v},\ell}$ can be expressed as

$$n_{\mathrm{v},\ell} = \sum_{\ell'=0}^{\ell-1} n_{\mathrm{v},\ell}^{\ell'}, \qquad \text{where} \quad \ell = 1,2,3,\cdots\cdots, N \quad (3.5)$$

Here, $n_{\mathrm{V},\ell}^{\ell'}$ represents the contribution of charge distribution of $\mathrm{Q}_{\ell'}$ to $n_{\mathrm{v},\ell}$, as depicted by the shaded red triangle (dotted) in the inset of **Fig. 3.2**. This contribution can be compared to that of $\mathrm{Q}_{\ell'}$ using geometric considerations and the similarity of charge distributions within the QWs. Since the two triangles are similar, their areas satisfy the following relation

$$\frac{\frac{1}{2} \times q n_{\mathrm{v},\ell}^{\ell'} \times W_{\ell\ell'}}{Q_{\ell'}} = \left(\frac{W_{\ell\ell'}}{W_{E\ell'}}\right)^2, \quad (3.6)$$

where $\mathrm{W}_{\ell\ell'} = \mathrm{W}_{\mathrm{E}\ell'} - \mathrm{W}_{\mathrm{E}\ell}$ represents the distance between QW_ℓ and $\mathrm{QW}_{\ell'}$. Using Eqs. (3.5) and (3.6), $qn_{\mathrm{v},\ell}$ can be expressed as a function of $\mathrm{Q}_{\ell'}$ as follows:

$$qn_{\mathrm{v},\ell} = \sum_{\ell'=0}^{\ell-1} 2\left(\frac{W_{\ell\ell'}}{W_{E\ell'}}\right)^2 \frac{Q_{\ell'}}{W_{\ell\ell'}}, \qquad \text{where } \ell = 1,2,,\cdot\cdot, N. \quad (3.7)$$

Using Eqs. (3.4) and (3.7), Q_ℓ can be expressed in terms of $\mathrm{Q}_{\ell'}$ as

doi:10.6342/NTU202500212

$$Q_\ell = \sum_{\ell'=0}^{\ell-1} \left[\frac{\tau_{t,E\ell}}{\tau_{QW,\ell}} \frac{\dfrac{1}{\tau_{cap,\ell}}}{\dfrac{1}{\tau_{QW,\ell}} + \dfrac{1}{\tau_{esc,\ell}}} \left(\frac{W_{\ell\ell'}}{W_{E\ell'}}\right)^2 \frac{d_\ell}{\left(\dfrac{W_{\ell\ell'}}{2}\right)} \right] Q_{\ell'}, \tag{3.8}$$

where $\ell = 1,2,3,\cdots\cdots, N.$

Substituting Q_ℓ from Eq. (3.3) in the function of F_ℓ into Eq. (3.8), the DC flux F_ℓ can be expressed in terms of $F_{\ell'}$ as

$$F_\ell = \sum_{\ell'=0}^{\ell-1} \left[\frac{\tau_{t,E\ell}}{\tau_{QW,\ell}} \frac{\dfrac{1}{\tau_{cap,\ell}}}{\dfrac{1}{\tau_{QW,\ell}} + \dfrac{1}{\tau_{esc,\ell}}} \frac{W_{\ell\ell'}^2}{W_{E\ell'}^2} \frac{2d_\ell}{W_{\ell\ell'}} \frac{\dfrac{1}{\tau_b} + \dfrac{1}{\tau_{t,E\ell}}}{\dfrac{1}{\tau_b} + \dfrac{1}{\tau_{t,E\ell'}}} \right] F_{\ell'}, \tag{3.9}$$

where $\ell = 1,2,3,\cdots\cdots, N.$

The current gains $\beta_{E\ell}$ and $\beta_{E\ell'}$ can be defined in terms of fictitious HBTs with base widths $W_{E\ell}$ and $W_{E\ell'}$, and $(W_{\ell\ell'}/W_{E\ell'})^2$, as follows:

$$\beta_{E\ell} = \frac{\tau_b}{\tau_{t,E\ell}}, \qquad \beta_{E\ell'} = \frac{\tau_b}{\tau_{t,E\ell'}}, \qquad \left(\frac{W_{\ell\ell'}}{W_{E\ell'}}\right)^2 \approx \frac{\tau_{t,\ell\ell'}}{\tau_{t,E\ell'}}, \tag{3.10}$$

Using Eq. (3.10), the expression for F_ℓ from Eq. (3.9) can be rewritten as

$$\begin{aligned} F_\ell &\cong \sum_{\ell'=0}^{\ell-1} \left[\frac{\tau_{t,E\ell}}{\tau_{QW,\ell}} \frac{\dfrac{1}{\tau_{cap,\ell}}}{\dfrac{1}{\tau_{QW,\ell}} + \dfrac{1}{\tau_{esc,\ell}}} \frac{\tau_{t,\ell\ell'}}{\tau_{t,E\ell'}} \frac{d_\ell}{\left(\dfrac{W_{\ell\ell'}}{2}\right)} \frac{1+\beta_{E\ell}}{1+\beta_{E\ell'}} \right] F_{\ell'} \\ &\cong \sum_{\ell'=0}^{\ell-1} \left[\frac{\tau_b}{\tau_{QW,\ell}} \frac{\dfrac{1}{\tau_{cap,\ell}}}{\dfrac{1}{\tau_{QW,\ell}} + \dfrac{1}{\tau_{esc,\ell}}} \frac{1+\dfrac{1}{\beta_{E\ell}}}{1+\dfrac{1}{\beta_{E\ell'}}} \frac{1}{\beta_{\ell\ell'}} \frac{d_\ell}{\left(\dfrac{W_{\ell\ell'}}{2}\right)} \right] F_{\ell'}, \end{aligned} \tag{3.11}$$

where $\ell = 1,2,3,\cdots\cdots, N.$

The term $U_{\ell\ell'}$ is additionally defined as

doi:10.6342/NTU202500212

$$U_{\ell\ell'} = \frac{\tau_b}{\tau_{QW,\ell}} \frac{\frac{1}{\tau_{cap,\ell}}}{\frac{1}{\tau_{QW,\ell}} + \frac{1}{\tau_{esc,\ell}}} \frac{1 + \frac{1}{\beta_{E\ell}}}{1 + \frac{1}{\beta_{E\ell'}}} \frac{1}{\beta_{\ell\ell'}} \frac{d_\ell}{\left(\frac{W_{\ell\ell'}}{2}\right)}. \quad (3.12)$$

Using Eq. (3.12), the flux F_ℓ can be expressed in terms of $U_{\ell\ell'}$ as

$$F_\ell \cong \sum_{\ell'=0}^{\ell-1} U_{\ell\ell'} F_{\ell'}, \qquad \text{where} \quad \ell = 1,2,3,\cdots\cdots,N \quad (3.13)$$

In **Fig. 3.1**, the total direct current (DC) flux at the emitter terminal F_E and the collector terminal F_C is defines as follows:

$$F_E = \sum_{\ell=0}^{N} F_\ell\,, \qquad \text{where} \quad \ell = 1,2,3,\cdots\cdots,N. \quad (3.14a)$$

$$F_C = \frac{Q_0}{\tau_{t,EC}} = \frac{Q_0}{\tau_{t,E0}}. \quad (3.14b)$$

Using Eq. (3.14a), the emitter current I_E is given by $I_E=AF_E$, where A represents the cross-section area of the device. Expanding F_E, the emitter current becomes

$$I_E = AF_E = A\sum_{\ell=0}^{N} F_\ell = A\left[1 + \sum_{\ell=1}^{N} V_\ell\right] F_0, \qquad \text{where} \quad \ell = 1,2,3,\cdot\cdot,N. \quad (3.15)$$

Here, V_ℓ is defined as the ratio F_ℓ/F_0.

Similarly, from Eq. (3.14b), the collector current $I_C=AF_C$ can be related to F_0 as

$$I_C = AF_C = A\frac{Q_0}{\tau_{t,E0}} = A\frac{\beta_{EC}}{1+\beta_{EC}} F_0, \quad (3.16a)$$

where

$$Q_0 = \frac{F_0}{\frac{1}{\tau_b} + \frac{1}{\tau_{t,E0}}}, \qquad \beta_{EC} = \frac{\tau_B}{\tau_{t,EC}}, \quad (3.16b)$$

doi:10.6342/NTU202500212

Using Eqs. (3.15) and (3.16a), the base current I_B is derived as $I_B = I_E - I_C$, can be derived as follows:

$$I_B = A\left[1 + \sum_{\ell=1}^{N} V_\ell - \frac{\beta_{EC}}{1+\beta_{EC}}\right]F_0, \qquad \text{Where} \quad \ell = 1,2,3,\cdot\cdot,N. \tag{3.17}$$

The current gain, denoted as $\beta \equiv \Delta I_C/\Delta I_B = I_C/I_B$, is evaluated by utilizing Eqs. (3.16a) and (3.17) after canceling the common factor A and F_0. This results in the following expression for the current gain:

$$\beta = \frac{\beta_{EC}}{1 + (1+\beta_{EC})\sum_{\ell=1}^{N} V_\ell}, \qquad \text{where} \quad \ell = 1,2,3,\cdots\cdots,N\cdot \tag{3.18}$$

To determine the current gain behavior of the MQW-HBT, the expression for the current gain (β) from Eq. (3.18) is employed. When compared to the current gain of a conventional HBT (β_{EC}), the current gain of MQW-HBT is primarily reduced by a factor $\sum_{\ell=1}^{N} V_\ell$, which represents a mathematical relationship between recombination rates of electron charge densities in each QW and the QW-to-collector region.

For the case where $N = 1$, the current gain of a Single QW in the base region of the transistor ($\beta_{1QW\text{-}HBT}$) is determined using Eq. (3.18), resulting in the following expression:

$$\beta_{1QW-HBT} \approx \left[\frac{1}{\beta_{EC}} + \left(1 + \frac{1}{\beta_{EC}}\right)V_1\right]^{-1} \tag{3.19}$$

Here, V_1 is equivalent to $U_{1,0}$, as obtained from Eq. (3.12). It is assumed that $\tau_{QW,1} = \tau_{QW}$, $\tau_{cap,1} = \tau_{cap}$, and $\tau_{esc,1} = \tau_{esc}$. Additionally, $\beta_{E1} = \beta_{EQW}$, $\beta_{E0} = \beta_{EC}$, $\beta_{10} = \beta_{QWC}$, and $W_{10} = W_{1C}$, which is equal to the width of the QW-to-collector (W_{QWC}). The

doi:10.6342/NTU202500212

expression of $\beta_{1QW\text{-}HBT}$ is further refined as

$$\beta_{1QW-HBLET} \approx \left[\frac{1}{\beta_{EC}} + \left(1+\frac{1}{\beta_{EC}}\right)\frac{\tau_b}{\tau_{QW}}\frac{\frac{1}{\tau_{cap}}}{\frac{1}{\tau_{QW}}+\frac{1}{\tau_{esc}}} \times \frac{1}{\beta_{QWC}}\frac{d}{\left(\frac{W_{QWC}}{2}\right)}\frac{1+\frac{1}{\beta_{EQW}}}{1+\frac{1}{\beta_{EC}}}\right]^{-1}$$

$$\approx \left[\frac{1}{\beta_{EC}} + \frac{\tau_b}{\tau_{QW}}\frac{\frac{1}{\tau_{cap}}}{\frac{1}{\tau_{QW}}+\frac{1}{\tau_{esc}}}\frac{1}{\beta_{QWC}}\frac{d}{\left(\frac{W_{QWC}}{2}\right)}\right]^{-1}. \quad (3.20)$$

In this Eq. (3.20), the term $1/\beta_{EQW}$, which is typically smaller than one, has been omitted for simplification. The expression for the current gain ($\beta_{1QW\text{-}HBT}$) for a single QW (SQW) in the HBT case, as derived from Eq. (3.18), is identical to the Eq. (12) presented by Chang *et al*. [53]. This analytical modeling of the current gain using a modified charge-control model provides insights for enhancing thermally dependent current gain by optimizing the design of MQWs and the positioning of QWs. Consequently, this analytical model for MQW-based HBT can be employed to optimize transistor current gain and enhancing the capture-escape process.

3.5 Effect of QW Position and Number on Current Gain and Charge Analysis in MQW-HBTs

The expression for current gain from Eq. (3.18) of the MQW-HBT is utilized to investigate the impact of number of QWs and their positioning on the current gain. This study considers two types of epi-layer designs: a single quantum-well heterojunction bipolar transistor (single QW-based HBT or 1QW-HBT) as reported by Change et al. [53],

doi:10.6342/NTU202500212

and a double quantum-well heterojunction bipolar transistor (double QW-based HBT or 2QW-HBT), as reported by Yang et al. [90]. Previous studies [53], [90] have provided an in-depth detailed of the fabrication process for n-p-n QW-HBTs incorporation 1QW and 2QW in the base region of transistor. Additionally, a comprehensive description of the fabrication and structure of both 1QW-HBT and 2QW-HBT has also been provided in [53], [90], [91], [92], [93].

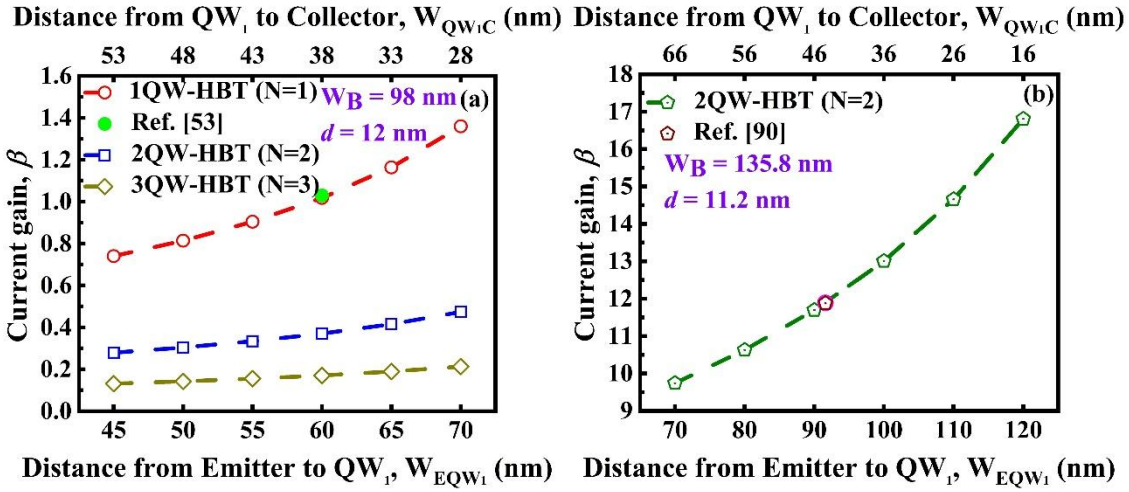


Fig. 3.3: (a) The current gain β as a function of the quantum well (QW) position within a 98 nm GaAs base width for a 1QW-HBT, based on the specified epitaxial layer structure [53]. The analysis includes impact of increasing the number of QWs within the same base is also analyzed. (b) The current gain as a function of the QW position within a 135.8 nm GaAs base width for a double QW HBT (2QW-HBT), incorporating the epitaxial layer structure [90].

The 1QW-HBT structure is considered to investigate the impact of QW position and the number of QWs on the current gain of the transistor. It is observed that the current gain increases by approximately 83.65% when the distance from QW-to-collector $\left(W_{QW_1C}\right)$ is reduced from 53 nm to 28 nm as, illustrated in **Fig. (3.3a)**. This unusual trend can be

doi:10.6342/NTU202500212

explained by the reduced capture of electrons by the QW when it is positioned farther from the emitter and closer to the collector in transistor's base. Conversely, the transit time of escaped electrons from the QW-to-collector decreases when the QW is placed nearer to the collector. The simulation results for the current gain (represented by red hollow circles) align well with the experimental current gain (depicted as green solid circles) when the QW is inserted at 60 nm from the emitter $\left(W_{EQW_1}\right)$ in the 98 nm GaAs base of the transistor [53]. **Table 3.1** lists the simulation parameters for the current gain of 1QW-HBT $\beta_{1QW\text{-}HBT}$, at a base current, I_B of 1 mA and a collector-to-emitter voltage, V_{CE} of 2 V at a temperature of $T = 300$ K.

Table 3.1: Model parameters used for evaluation of $\beta_{1QW\text{-}HBT}$ at T=300 K [53]

Parameter	Symbol	Value
Distance from emitter to QW	W_{EQW}	60 nm
Width of QW	d	12 nm
Width of base	W_B	98 nm
Transit time of electron across base width	$\tau_{t,EC}$	3 ps
Transit time of electron across QW to collector	$\tau_{t,QWC}$	0.45 ps
Base recombination time	τ_b	93 ps
Capture time	τ_{cap}	0.25 ps
QW recombination time	τ_{QW}	20 ps
Escape time	τ_{esc}	93.45 ps

When the number of QWs is increased in the base of transistor, the current gain decreases significantly due to the increased electron capture via the MQW. For instance, when the number of QWs with the same equal widths increased from 1 to 3 in the same 98 nm GaAs base width of the transistor, the current gain of the 2QW-HBT $\beta_{2QW-HBT}$ and

doi:10.6342/NTU202500212

3QW-HBT (triple-quantum-well heterojunction bipolar transistor) $\beta_{3QW-HBT}$ decreases by 63.6% and 83.22%, respectively, when the QW is inserted 60 nm from the emitter ($W_{EQW_1} = 60$ nm) in the same 98 nm base width. The separation between two consecutive QWs in the 2QW-HBT and 3QW-HBT is 40 nm. For simplicity, we assume that the value of τ_{cap}, τ_{esc}, and τ_{QW} are the same for each QW with equal width in the case of 2QW-HBT and 3QW-HBT due to limited experimental data available on MQW-HBT. The current gain for the 2QW-HBT and 3QW-HBT increases by approximately 69.70% and 62%, respectively, when the distance from QW-to-collector $\left(W_{QW_1C}\right)$ is reduced from 53 nm to 28 nm, as shown in **Fig. 3.3(a).**

We also aim to validate our charge-control model for the experimental 2QW-HBT structure. The simulation results for the current gain of 2QW-HBT ($\beta_{2QW\text{-}HBT}$, magenta solid circle) align well with the experimental results ($\beta_{2QW\text{-}HBT}$, wine dot pentagon) when the transistor has a GaAs base width of 135.8 nm, with double QW widths of a 11.2 nm (separation by 56 nm) inserted at $W_{QW_1C} = 44.2$ nm. Additionally, the current gain of the 2QW-HBT increases by approximately 72.48% as the distance from the emitter-to-QW $\left(W_{EQW_1}\right)$ increases from 70 nm to 120 nm in the 135.8 nm GaAs base width, as shown in **Fig. (3.3b)**. **Table 3.2** lists the simulation parameters for the current gain of 2QW-HBT at I_B of 3 mA and V_{CE} of 2.5 V for the 135.8 nm base width at temperature of T = 28°C.

doi:10.6342/NTU202500212

Table 3.2: Model parameters used for evaluation of $\beta_{1QW\text{-}HBT}$ at T= 28 °C

Parameter	Symbol	Value	Source Ref.
Distance from emitter to QW_1	W_{EQW_1}	91.6 nm	[90], [91], [92], [93]
Width of QW	d	11.2 nm	[90], [91], [92], [93]
Width of base	W_B	135.8 nm	[90], [91], [92], [93]
Transit time of electron across base	$\tau_{t,EC}$	3.55 ps	[90]
Base recombination time	τ_b	93 ps	[53]
Capture time	τ_{cap}	6.27 ps	[90]
QW recombination time	τ_{QW}	89 ps	[94], [95]
Escape time	τ_{esc}	149 ps	[90]

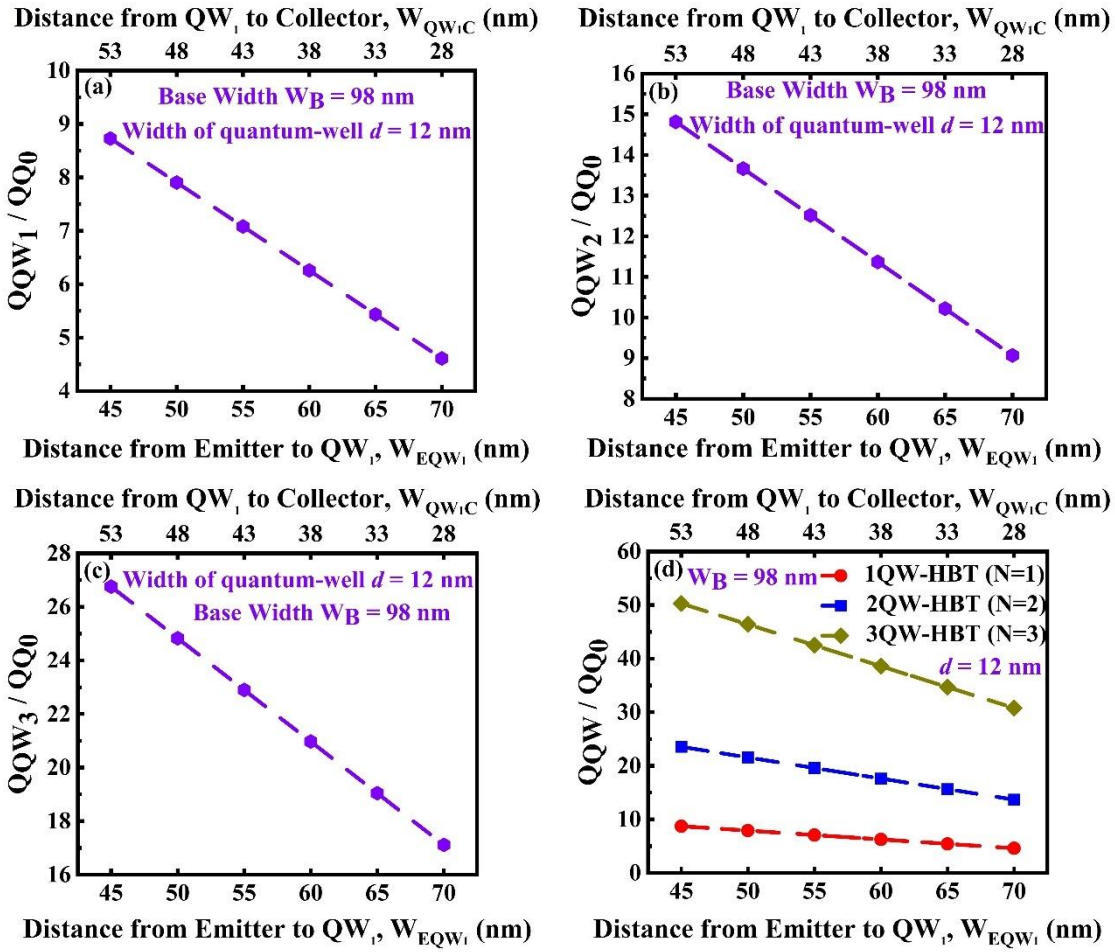


Fig. 3.4: (a) The ratio of Q_{QW_1}/Q_0, (b) Q_{QW_2}/Q_0, and (c) Q_{QW_3}/Q_0 as a function of the position of QW in 1QW-HBT, 2QW-HBT, and 3QW-HBT, respectively. (d) The total charge captured by the QWs as a function of the position of the QW.

doi:10.6342/NTU202500212

Now, for the study the charge distribution of the base minority carrier density in MQW-HBTs and demonstrate the application of the continuity condition to the population of minority carriers in the active region of the MQW into the base of transistor, the expression of Q_ℓ is defined with using Eqs. (3.3) and (3.4) as:

$$Q_\ell = \frac{\tau_{t,E\ell}}{\tau_{QW,\ell}} \frac{\frac{1}{\tau_{cap,\ell}}}{\frac{1}{\tau_{QW,\ell}} + \frac{1}{\tau_{esc,\ell}}} d_\ell q n_{\mathrm{V},\ell}. \tag{3.21}$$

Using Eq. (3.3), the ratio of $\mathrm{Q_{QW_\ell}}$ to $\mathrm{Q_0}$ is expressed as follows:

$$\frac{Q_{QW_\ell}}{Q_0} = \frac{Q_\ell}{Q_0} \frac{\tau_{QW,\ell}}{\tau_{t,E\ell}}, \tag{3.22}$$

The recursive relationship of $\mathrm{Q_\ell/Q_0}$ is defined using the Eqs. (3.8) and (3.12) as follow:

$$\frac{Q_\ell}{Q_0} = \sum_{\ell'=0}^{\ell-1} U_{\ell\ell'} \frac{1+\beta_{E\ell'}}{1+\beta_{E\ell}} \frac{Q_{\ell'}}{Q_0}, \qquad \text{where } \ell = 1,2,\cdots,N \cdot \tag{3.23}$$

However, the theoretical calculation of the charge ratio using Eqs. (3.22) and (3.23) tends to underestimate the charge analysis in $\mathrm{QW_\ell/Q_0}$. The electrons injected from the emitter diffuse through the base and are more readily absorbed by the QW when it is positioned closer to the emitter. Thus, $\mathrm{Q_{QW_\ell}/Q_0}$ depends on the position of the QW, which ultimately affects the current gain of MQW-HBT. The current gain of 1QW-HBLT, 2QW-HBT, and 3QW-HBT can be alternatively be expressed in terms of $\mathrm{Q_{QW_\ell}/Q_0}$ as

$$\beta_{1QW-HBT} = \frac{\beta_{EC}}{1 + \frac{\tau_b}{\tau_{QW,1}}\left(1 + \frac{1}{\beta_{E1}}\right)\frac{Q_{QW_1}}{Q_0}}, \tag{3.24a}$$

doi:10.6342/NTU202500212

$$\beta_{2QW-HBT} = \frac{\beta_{EC}}{1 + \frac{\tau_b}{\tau_{QW,1}}\left(1 + \frac{1}{\beta_{E1}}\right)\frac{Q_{QW_1}}{Q_0} + \frac{\tau_b}{\tau_{QW,2}}\left(1 + \frac{1}{\beta_{E2}}\right)\frac{Q_{QW_2}}{Q_0}}, \quad (3.24b)$$

$$\beta_{3QW-HBT} = \beta_{EC} \times \left[1 + \frac{\tau_b}{\tau_{QW,1}}\left(1 + \frac{1}{\beta_{E1}}\right)\frac{Q_{QW_1}}{Q_0} + \frac{\tau_b}{\tau_{QW,1}}\left(1 + \frac{1}{\beta_{E1}}\right)\frac{Q_{QW_1}}{Q_0} + \frac{\tau_b}{\tau_{QW,3}}\left(1 + \frac{1}{\beta_{E3}}\right)\frac{Q_{QW_3}}{Q_0}\right]^{-1}, \quad (3.24c)$$

where β_{E1}, β_{E2}, and β_{E3} are evaluated through Eq. (3.10). The values of Q_{QW_1}/Q_0, Q_{QW_2}/Q_0, and Q_{QW_3}/Q_0 are calculated using Eqs. (3.22) and (3.23), as shown in **Figs. (3.4a)**, **(3.4b)**, and **(3.4c)**, respectively. These calculations are based on the function of W_{EQW_1} and W_{QW_1C} for a 98 nm GaAs base of the transistor. Since the position of QW_3 is closer to the emitter than QW_2 and QW_1, QW_3 captures more electrons compared to the other QWs (QW_2 and QW_1). When the number QWs increases from 1 to 3 in the same 98 nm GaAs base, the total number of electrons captured by the 2QW and 3QW in 2QW-HBT and 3QW-HBT, respectively, is affected by the position of QWs $\left(W_{QW_1C}$ or $W_{EQW_1}\right)$ in the same 98 nm GaAs base of the transistor are shown in **Fig. (3.4d)**. When the width of W_{QW_1C} decreases from 53 nm to 28 nm, or when W_{EQW_1} increases from 45 nm to 70 nm, the total charge captured by 1QW, 2QW, and 3QW in 1QW-HBT, 2QW-HBT, and 3QW-HBT decreases by 47.17%, 41.90%, and 38.80%, respectively. This

doi:10.6342/NTU202500212

decrease in charge capture results in an increase in current gain of 83.65%, 69.70%, and 62% for the respective configurations. The current gain can also be enhanced through thermionic emission techniques [53], [90].

Our modified charge-control method can improve current gain by optimizing MQW design and QW positioning. This analytical model of MQW-HBTs serves as a foundation for enhancing transistor current gain and refining the capture-escape process. Furthermore, this modified charge-control model aids in designing efficient epi-layers for MQW-based HBTs for smart thermal sensing applications. We utilized this modified charge-control model to TQW-HBT. The detailed study for high-temperature applications is discussed in the subsequent subchapter.

3.6 Device Layer Structure Design and Fabrication Process for TQW-HBTs

The chapter 2 discussed how SQW-HBTs exhibit high sensitivity to temperature variations due to leveraging the thermionic emission properties of QWs. The sensitivity of QW-HBTs to ambient temperature can be significantly enhanced by employing specific layer structure designs that induce strong thermionic emission within the QWs or MQWs in the base region of HBTs. While previous studies have predominantly focused on the optical properties of MQW-based devices, such as optical modulation and laser thermal characteristics, limited attention has been paid to their electrical

doi:10.6342/NTU202500212

characteristics, as discussed in detail in Subchapter 3.3. The modified charge-control model for MQW-HBTs provides a valuable framework for designing efficient epitaxial layers for thermal sensing applications by enhancing thermal sensitivity through the introduction of additional QWs.

This section introduces a novel TQW-HBT, also referred to as a triple-quantum-well heterojunction bipolar light-emitting transistor (TQW-HBLET or TQW-LET). This device is designed to investigate the temperature-dependent current-voltage (I-V) characteristics of InGaP/GaAs TQW-HBTs. The epitaxial structures of n-p-n TQW-HBTs were fabricated on a semi-insulating (S.I.) GaAs substrate using the MOCVD process. The epitaxial layer stack consisted of several layers, starting with a heavily doped n-type GaAs buffer layer with a thickness of 5000 Å. This was followed by bottom cladding layers comprising a 634 Å thick n-type $Al_{0.40}Ga_{0.60}As$ layer, a 5000 Å thick oxidizable $Al_{0.95}Ga_{0.05}As$ layer, and a 150 Å thick oxide buffer layer of $Al_{0.40}Ga_{0.60}As$. The sequence continued with a 200 Å thin sub-collector layer of heavily doped n-type GaAs, followed by a 120 Å etching stop layer of $In_{0.49}Ga_{0.51}P$, and a 600 Å collector layer of undoped GaAs. The active layer design included a 1120 Å thick GaAs base layer with an average p-type doping concentration of $3 \times 10^{19} cm^{-3}$. Three undoped InGaAs QWs, each 70 Å thick and tailored for a wavelength (λ) of approximately 980 nm, were positioned side by side with a separation of 35Å. The emitter layer consisted of a 250 Å

doi:10.6342/NTU202500212

wide-bandgap n-type $In_{0.49}Ga_{0.51}P$ layer. The upper cladding structure comprised multiple layers: a 150 Å $Al_{0.35}Ga_{0.65}As$ oxide buffer layer, a 150 Å $Al_{0.8}Ga_{0.2}As$ oxidizable layer, a 4000 Å thick $Al_xGa_{1-x}As$ layer (where x varies from 0.95 to 0.99) serving as an oxide buffer layer, a 300 Å $Al_{0.8}Ga_{0.2}As$ oxidizable layer, and a 500 Å $Al_{0.35}Ga_{0.65}As$ confining layer. Finally, the epitaxial structure of TQW-HBTs was capped with a 1000 Å thick heavily doped n-type GaAs contact layer. The complete epitaxial layer structure of the TQW-HBTs is illustrated in **Fig. 3.5**, which also includes an inset showing the top views of the fabricated device. Detailed specifications and compositions for each layer of the TQW-HBT are provided in **Table 3.3.**

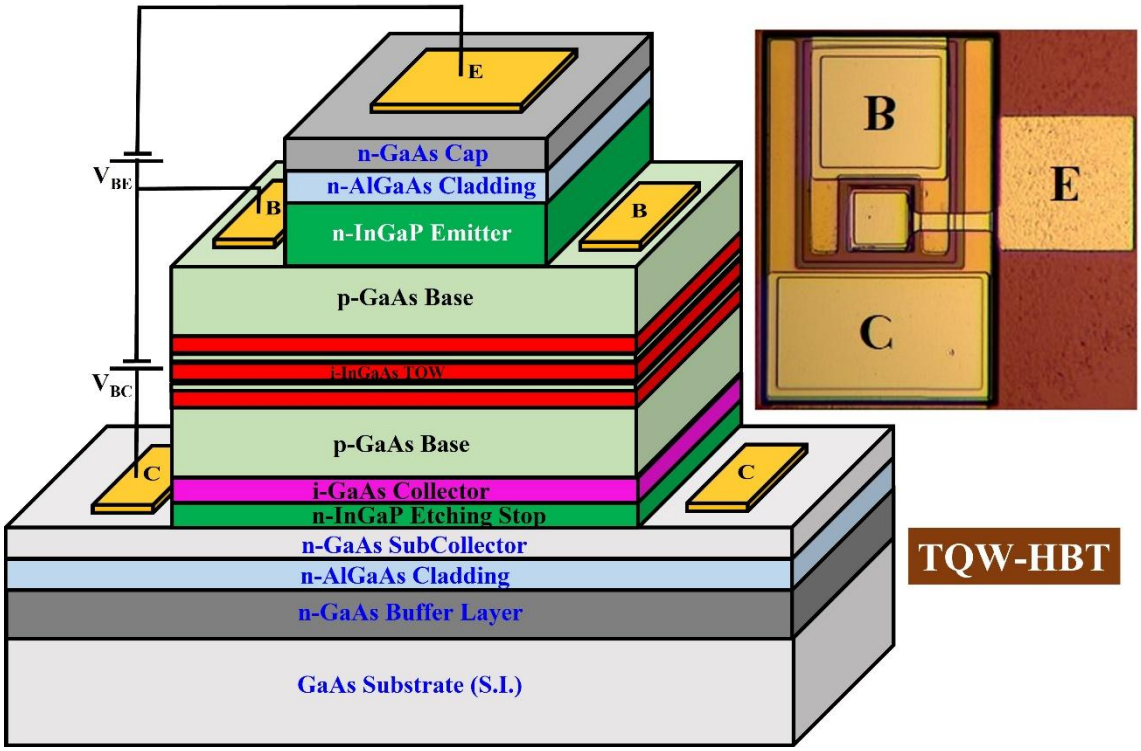


Fig. 3.5: Schematic of the epitaxial structure of the triple-quantum-well heterojunction bipolar transistor (TQW-HBT). The inset shows the top-view layout of the TQW-HBT device, with an emitter cross-section area of 40 μm x 40 μm.

doi:10.6342/NTU202500212

Table 3.3: The epitaxial layer structure design of n-p-n TQW-HBT.

Layer Name	Material	Mole Fraction (x)	Thickness (Å)	Type	Doping Level (Cm^{-3})	Dopant
Contact	GaAs		1000	N^+	3e18	Si
Confining	$Al_xGa_{1-x}As$	0.35	500	N	2e18	Si
Oxidizable	$Al_xGa_{1-x}As$	0.8	300	N	1.5e18	Si
Oxide Buffer	$Al_xGa_{1-x}As$	0.95~0.99	4000	N	1.5e18	Si
Oxidizable	$Al_xGa_{1-x}As$	0.8	150	N	8e17	Si
Oxide Buffer	$Al_xGa_{1-x}As$	0.35	150	N	5e17	Si
Emitter	$In_xGa_{1-x}P$	0.49	250	N^-	5e17	Si
Base	GaAs		100	P	4e19	C
Base	GaAs		100	P	2e19	C
Base	GaAs		300	P	1e19	C
Buffer	GaAs		20	i		UID
QW	$In_xGa_{1-x}As$	0.2	70	i		UID
Barrier	GaAs		35	i		UID
QW	$In_xGa_{1-x}As$	0.2	70	i		UID
Barrier	GaAs		35	i		UID
QW	$In_xGa_{1-x}As$	0.2	70	i		UID
Buffer	GaAs		20	i		UID
Base	GaAs		200	P	1e19	C
Base	$Al_xGa_{1-x}As$	0.05	100	P	3e19	C
Collector	GaAs		600	i	5e16	UID
Order	$In_xGa_{1-x}P$	0.49	120	N^-	1e17	Si
Sub-Collector	GaAs		200	N	3e18	Si
Oxide Buffer	$Al_xGa_{1-x}As$	0.4	150	N	2e18	Si
Oxidizable	$Al_xGa_{1-x}As$	0.95	5000	N	1.50e18	Si
Oxide Buffer	$Al_xGa_{1-x}As$	0.4	634	N	2e18	Si
Buffer Layer	GaAs		5000	N	3e18	Si
Substrate 4" GaAs S.I.						

doi:10.6342/NTU202500212

The fabrication process of TQW-HBTs follows a similar methodology to that of SQW-HBTs, as outlined in subchapter 2.3**.** Initially, the emitter and base mesas were defined using wet etching, followed by isolation etching down to the semi-insulating GaAs substrate. Following that, standard lithographic techniques and metallization processes were employed to deposit the emitter (E), base (B), and collector (C) contacts. The process completed with planarization, via hole etching, and pad metallization. The advanced epitaxial design and fabrication process enable TQW-HBTs to achieve enhanced thermal sensitivity, making them highly suitable candidate based on III-V compound semiconductor device for next-generation temperature sensing applications.

3.7 Device Characterization at Different Substrate Temperatures

Following the successful fabrication of TQW-HBT devices, their current-voltage (I-V) behavior was studied across a temperature range of 25℃ to 85℃ to evaluate high-temperature operation. For characterization, the devices were placed on a Peltier temperature-controlled stage. Thermal equilibrium was achieved within two minutes, but for precise measurements, an additional twenty minutes were allowed to ensure the Peltier stage reached a steady-state temperature before measurement result data collection. Electrical DC bias and current were supplied using an Agilent E5270B source. During the device characterization process, the base current, I_B was varied systematically from 0.2

doi:10.6342/NTU202500212

mA to 1 mA in increments of 0.2 mA, while the collector-to-emitter voltage, V_{CE} was increased from 0 to 2 volts. The collector current, I_C versus collector-to-emitter voltage, V_{CE} characteristics were measured at substrate temperature, T_{ext} of 25℃ and 85℃ for different base current, as shown in **Fig. 3.6**. The insertion of three QWs into the base of the transistor resulted in enhanced electron capture, causing a reduction in the collector current and current gain.

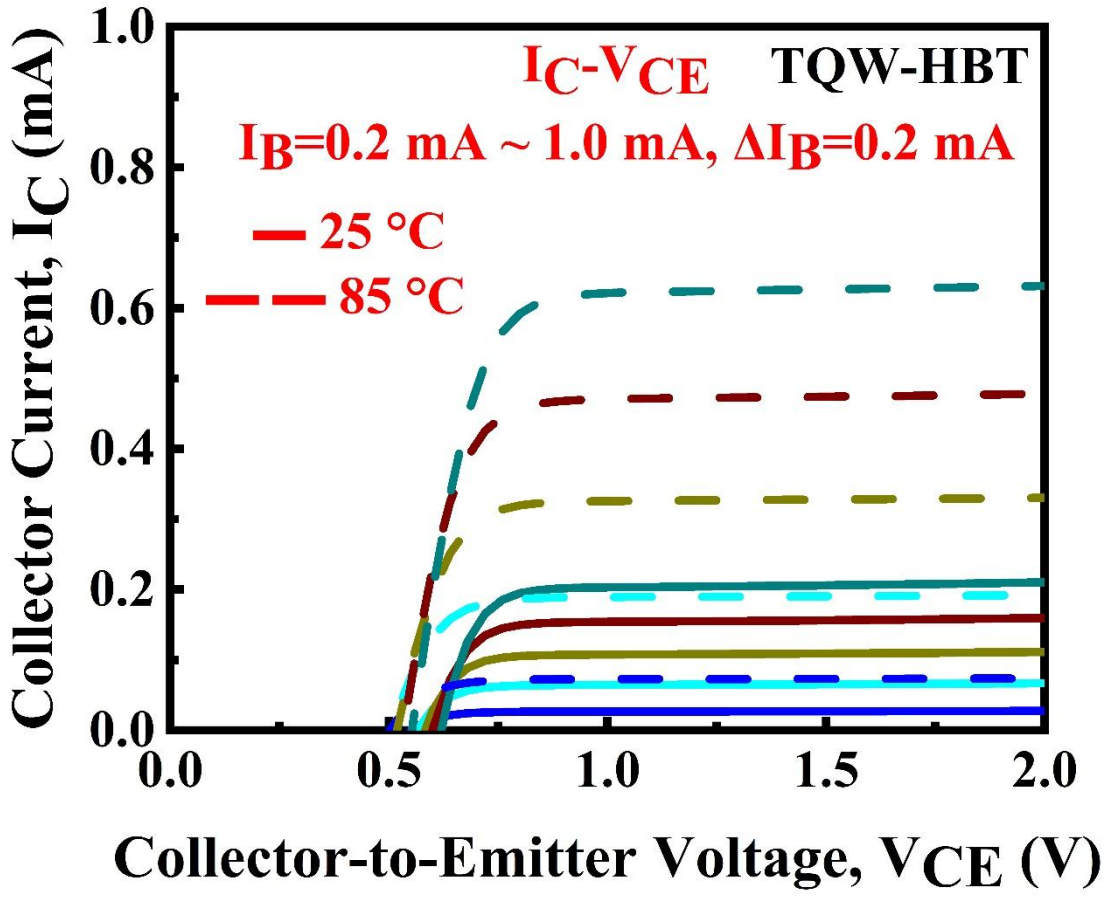


Fig. 3.6: Experimental characteristics: collector current I_C vs. collector-to-voltage V_{CE} of n-p-n TQW-HBT at varied base currents I_B from 0.2 mA to 1 mA, characterized at T_{ext}=25 ºC (solid line) and T_{ext}=85ºC (dashed line).

This phenomenon can be explained using the energy band diagram of TQW-HBTs,

doi:10.6342/NTU202500212

depicted in **Fig. 3.7**, which illustrates a device configuration with n-type $In_{0.49}Ga_{0.51}P/p^+$-type GaAs/ n-type GaAs configuration. Under forward-active region operation with I_B of 1 mA and V_{CE} of 2 V, the collector current, I_C increased from 0.210 mA at T_{ext}=25℃ to 0.631 mA at T_{ext}=85℃. This temperature-dependent collector current is a critical parameter for designing smart thermal sensor based on the $I_C(T)$ characteristics. Additionally, at the same bias conditions (I_B and V_{CE}), the collector-to-emitter offset voltage decreased from 0.64 V at T_{ext}=25℃ to 0.56 V at T_{ext}=85℃, indicating the presence of intrinsic carrier surges with increasing temperature.

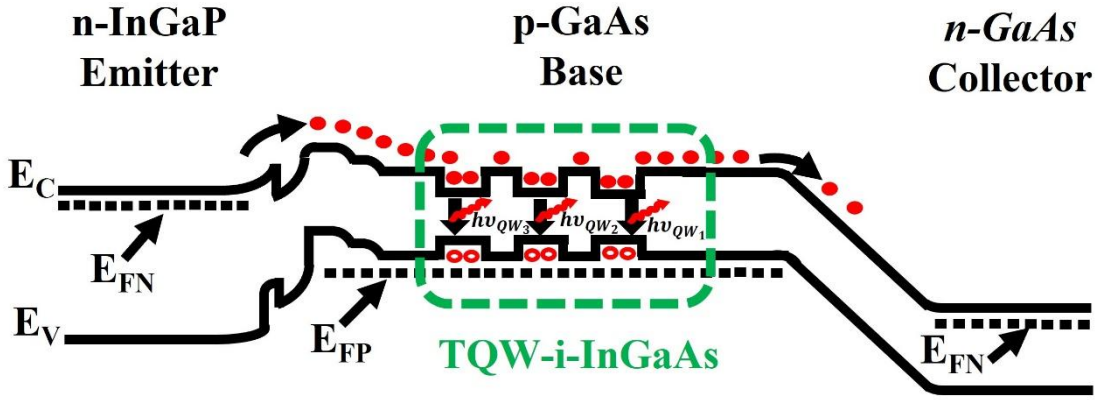


Fig. 3.7: A energy band diagram of n-p-n InGaP/GaAs TQW-HBT.

Figure 3.8 illustrates the thermally enhanced current gain, β_{TQW} of the TQW-HBT, demonstrating its variation with controlled temperature, T_{ext} for different base currents, I_B ranging from 25ºC to 85ºC. The current gain increased with both higher substrate temperature, T_{ext} and base current, I_B. The conduction band offset of the QW played a pivotal role in confining electrons within the QW of the base region, effectively localizing

doi:10.6342/NTU202500212

them around the QWs. As the temperature increased, thermal energy enabled electrons

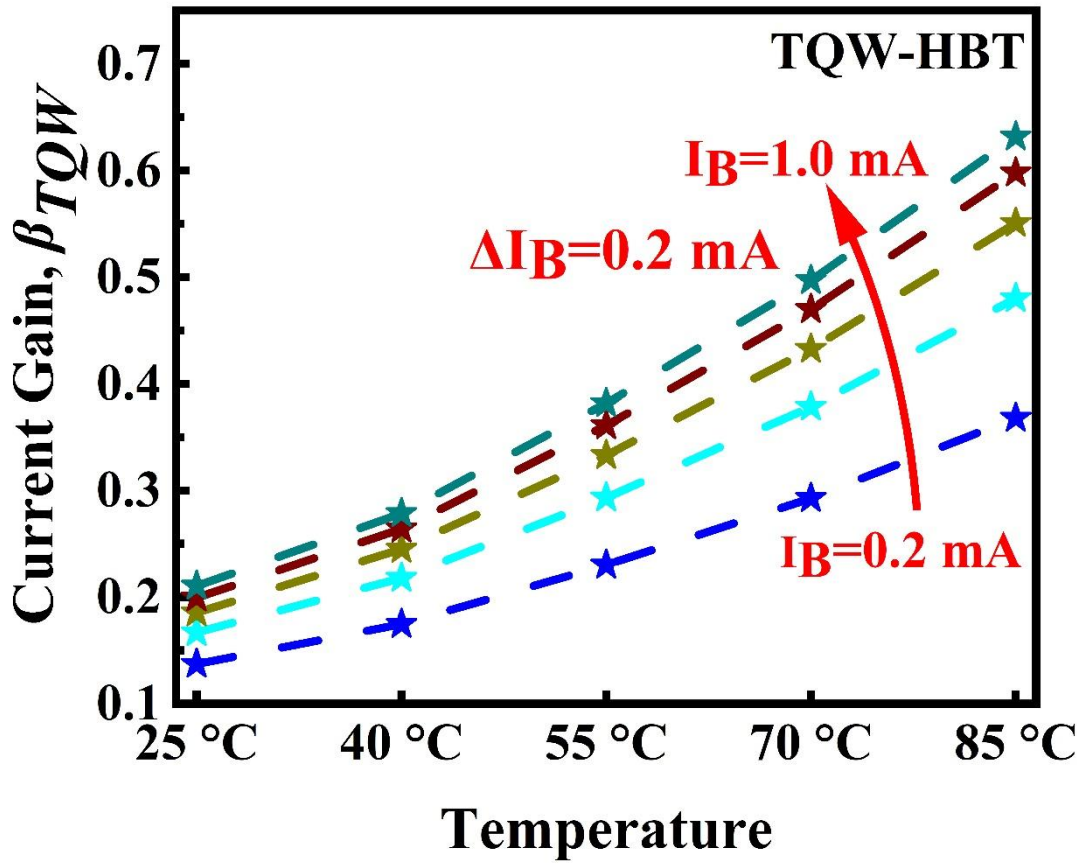


Fig. 3.8: Experimental analysis of current gain, β_{TQW} of TQW-HBT as a function of externally controlled substrate temperature, T_{ext} for different base currents.

within the QW reservoir to overcome the quantum-well-barrier (QWB), allowing them to rejoin the diffusion flow toward the collector. This reduced the electron capture effect of the TQW at elevated temperatures, resulting in an enhanced current gain under reverse bias as more electrons reached the base-collector (B-C) junction. Furthermore, the higher current gain, β_{TQW} observed at increased base current, I_B may be attributed to thermal effects caused by the injection of current, which could elevate the device's internal temperature. These experimental results highlight the modulation of current gain with

doi:10.6342/NTU202500212

ambient temperature variations, demonstrating the potential of TQW-HBTs for temperature-sensitive applications.

In addition to experimental characterization, to further investigate device physics at higher temperatures, theoretical analysis using a modified charge-control model is presented in the next subsection. These findings highlight the potential of TQW-HBTs for developing highly sensitive, temperature-dependent I-V characteristics, making them promising candidates for next-generation smart thermal sensor front-end components.

3.8 Modified Charge-Control Model for TQW-HBTs

TQW-based HBTs demonstrate unique characteristics compared to SCH structures due to the tilting of the minority carrier distribution during forward-active operation. Applying a reverse bias to the B-C junction induces a high electric field that drives electrons into the collector, resulting in a near-zero electron density at the collector boundary. The basic charge-control model for LET and TL was initially introduced by Then et al. [56] and Feng et al. [57] in 2007. Subsequently, our research team modified the charge-control model framework for LETs and investigated its thermal characteristics in 2019 for square SQW-HBTs [53]. Furthermore, we expanded on this by reporting the modified charge-control model for staircase SQW-HBTs in 2023 [89]. Detailed analyses of SQW- and MQW-based modeling for LETs and TLs are presented in Subchapter 2.6

doi:10.6342/NTU202500212

and 3.3 of this dissertation.

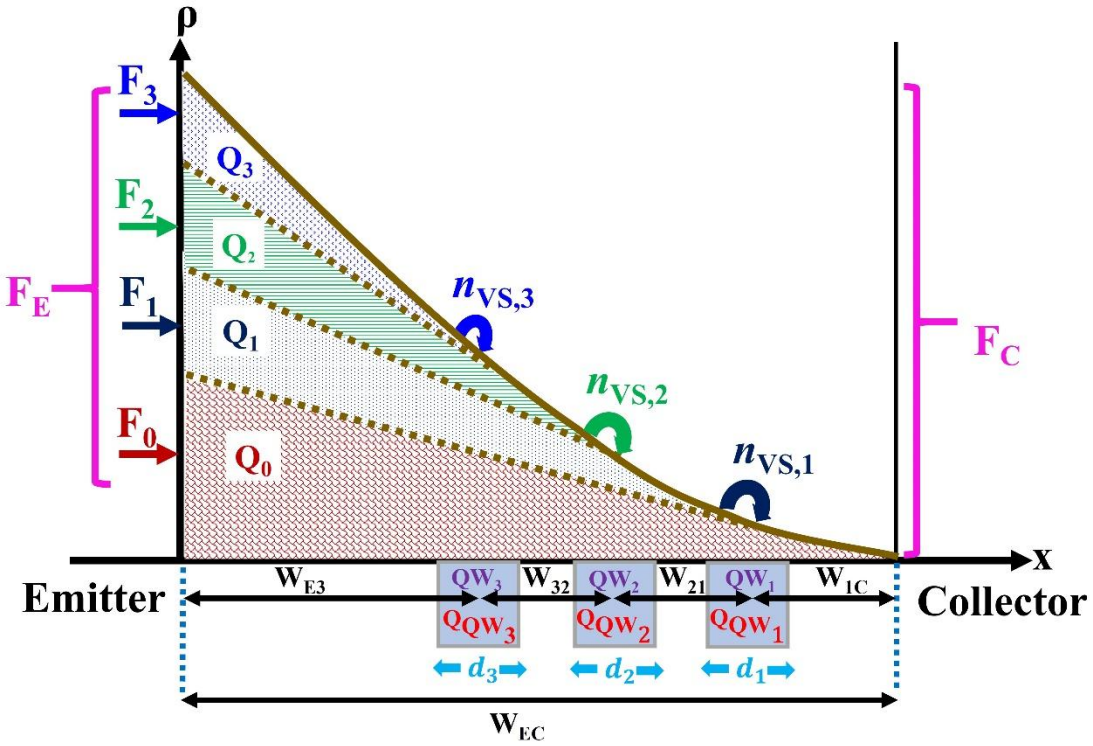


Fig. 3.9: Schematic representation of minority charge distribution (ρ) in the base region of the TQW-HBT.

This section focuses on investigating the electron distribution around the TQWs and the temperature-dependent behavior of current gain in TQW-HBTs. The research prioritizes analytical formulations that explicitly incorporate time-dependent parameters to enhance understanding of device behavior. **Figure 3.9** illustrates the modified charge-control model, depicting the distribution of minority charges (ρ) within the base region of TQW-HBTs. The base charge distribution in TQW-HBTs can be represented as a combination of four triangular charge populations, designated as Q_0, Q_1, Q_2, and Q_3. The total volume charge density of minority carriers in the base consists of seven components: Q_0,

doi:10.6342/NTU202500212

Q_1, Q_2, Q_3, Q_{QW_1}, Q_{QW_2}, and Q_{QW_3}. Here, Q_1, Q_2, and Q_3 represents electrons diffusing from the emitter to QW_1, QW_2, and QW_3, respectively, contributing to spontaneous or stimulated recombination. Q_0 governs the diffusion of electrons towards the B-C junction, contributing to the collector current, I_C. Q_{QW_1}, Q_{QW_2}, and Q_{QW_3} are associated with minority carrier capture by QW_1, QW_2, and QW_3, respectively.

Expanding upon the previously derived current gain expression for MQW-HBTs, this study investigates the temperature impact on the current gain of TQW-HBTs, represented as $\beta_{TQW\text{-}HBT}$, using Eq. (3.18). In this analysis, quantum-well coupling and quantum-tunneling currents are omitted due to their relatively minor influence compared to the dominant thermionic emission process. The current gain of TQW-HBTs, β_{TQW} is derived using Eq. (3.18), with N = 3 as follows:

$$\beta_{TQW} \approx \frac{\beta_{EC}}{1+(1+\beta_{EC})(V_1+V_2+V_3)} \tag{3.25}$$

where $\beta_{EC} = \tau_b/\tau_{t,EC}$ denotes the current gain of an HBT with base width W_B, τ_b is the bulk recombination lifetime of electrons in the base, and $\tau_{t,EC}$ represents the electron transit time through the GaAs base region of the transistor. Increasing the number of QWs in the base region reduces the current gain due to enhanced carrier recombination in the TQWs. Conversely, in the absence of TQWs $(V_1 + V_2 + V_3 = 0)$, the current gain equals β_{EC} of the HBT with the same base width W_B. The terms V_1, V_2, and V_3 are defined

doi:10.6342/NTU202500212

using $V_\ell = F_\ell/F_0$ from Eq. (3.15) as F_1/F_0, F_2/F_0, and F_3/F_0, respectively, with F_ℓ derived from Eq. (3.13). **Figure 3.9** highlights the charge flux of minority carriers corresponding to Q_0, Q_1,Q_2, and Q_3, represented by F_0, F_1,F_2, and F_3, respectively. With Eq. (3.13), the terms F_1, F_2, and F_3 can be represented as

$$F_1 \cong U_{1C}F_0 \tag{3.26a}$$

$$F_2 \cong U_{2C}F_0 + U_{21}F_1 \tag{3.26b}$$

$$F_3 \cong U_{3C}F_0 + U_{31}F_1 + U_{32}F_2 \tag{3.26c}$$

Using Eq. (3.12), the terms U_{1C}, U_{2C}, U_{3C}, U_{21}, U_{31}, and U_{32} are defined as

$$U_{1C} = \frac{\tau_b}{\tau_{QW,1}} \frac{\frac{1}{\tau_{cap,1}}}{\frac{1}{\tau_{QW,1}} + \frac{1}{\tau_{esc,1}}} \left(\frac{1 + \frac{1}{\beta_{E1}}}{1 + \frac{1}{\beta_{EC}}} \right) \frac{1}{\beta_{1C}} \frac{d_1}{\left(\frac{W_{1C}}{2}\right)} \tag{17a}$$

$$U_{2C} = \frac{\tau_b}{\tau_{QW,2}} \frac{\frac{1}{\tau_{cap,2}}}{\frac{1}{\tau_{QW,2}} + \frac{1}{\tau_{esc,2}}} \left(\frac{1 + \frac{1}{\beta_{E2}}}{1 + \frac{1}{\beta_{EC}}} \right) \frac{1}{\beta_{2C}} \frac{d_2}{\left(\frac{W_{2C}}{2}\right)} \tag{3.27b}$$

$$U_{3C} = \frac{\tau_b}{\tau_{QW,3}} \frac{\frac{1}{\tau_{cap,3}}}{\frac{1}{\tau_{QW,3}} + \frac{1}{\tau_{esc,3}}} \left(\frac{1 + \frac{1}{\beta_{E3}}}{1 + \frac{1}{\beta_{EC}}} \right) \frac{1}{\beta_{3C}} \frac{d_3}{\left(\frac{W_{3C}}{2}\right)} \tag{3.27c}$$

doi:10.6342/NTU202500212

$$U_{21} = \frac{\tau_b}{\tau_{QW,2}} \frac{\frac{1}{\tau_{cap,2}}}{\frac{1}{\tau_{QW,2}} + \frac{1}{\tau_{esc,2}}} \left(\frac{1 + \frac{1}{\beta_{E2}}}{1 + \frac{1}{\beta_{E1}}} \right) \frac{1}{\beta_{21}} \frac{d_2}{\left(\frac{W_{21}}{2}\right)} \tag{3.27d}$$

$$U_{31} = \frac{\tau_b}{\tau_{QW,3}} \frac{\frac{1}{\tau_{cap,3}}}{\frac{1}{\tau_{QW,3}} + \frac{1}{\tau_{esc,3}}} \left(\frac{1 + \frac{1}{\beta_{E3}}}{1 + \frac{1}{\beta_{E1}}} \right) \frac{1}{\beta_{31}} \frac{d_3}{\left(\frac{W_{31}}{2}\right)} \tag{3.27e}$$

$$U_{32} = \frac{\tau_b}{\tau_{QW,3}} \frac{\frac{1}{\tau_{cap,3}}}{\frac{1}{\tau_{QW,3}} + \frac{1}{\tau_{esc,3}}} \left(\frac{1 + \frac{1}{\beta_{E3}}}{1 + \frac{1}{\beta_{E2}}} \right) \frac{1}{\beta_{32}} \frac{d_3}{\left(\frac{W_{32}}{2}\right)} \tag{3.27f}$$

Here, the recombination lifetime of electrons in each QW is represented by $\tau_{QW,1}$, τ_{QW2}, and τ_{QW3} for QW_1, QW_2, and QW_3, respectively. The densities of minority carrier in the virtual conduction states of the QWs are $n_{VS,1}$, $n_{VS,2}$, and $n_{VS,3}$ for QW_1, QW_2, and QW_3, respectively. The capture times of minority carriers transitioning to bound states from their respective virtual states in the QW_1, QW_2, and QW_3 are $\tau_{cap,1}$, τ_{cap2}, and $\tau_{cap,3}$, respectively. The escape times of electrons from QW_1, QW_2, and QW_3 into the doped base region are $\tau_{esc,1}$, $\tau_{esc,2}$, and $\tau_{esc,3}$. The QW widths in the fabricated TQW-HBTs device are uniform, with $d_1 = d_2 = d_3 = d$. Other terms, including β_{E3}, β_{E2}, β_{E1}, β_{32}, β_{31}, β_{3C}, β_{2C}, β_{1C}, and β_{21}, are calculated using the formulation

doi:10.6342/NTU202500212

detailed in Eq. (3.10).

3.9 Modified Thermionic Emission Model, Carrier Dynamics and Charge Analysis in TQW Structures

The escape time of electrons from QWs was analyzed using the classical thermionic emission model developed by Schneider and Klitzing [65] and Nagarajan [66]. This model assumes that the carrier distribution in the QW follows a Boltzmann-like statistics, where the escape currents are directly related associated with the carrier distribution tail at the top of the energy barrier. However, this approach is effective only for QW widths on the order of several hundred Angstroms, limiting its application for narrow QWs. In the fabricated TQW-HBTs, each QW has a width of 70 Å. To address this limitation, a modified expression for the thermionic emission lifetime proposed by Nelson et al. was employed. This method accounts for thermionic emission, thermally assisted tunneling, and direct tunneling within the QW [67].

The estimation of electron escape time began with calculating the injection current density J_e. This was achieved by integrating the product of the carrier concentration in the QW, the transmission probability, and the carrier escape velocity across the energy range. Subsequently, the carrier population in confined sub-band states and unconfined states above the QW was integrated. The thermionic emission lifetime was then evaluated

doi:10.6342/NTU202500212

using the equation:

$$\tau_{esc}^{te}=\frac{n_e d}{J_e} \tag{3.28}$$

In this calculation, the classical Maxwell-Boltzmann distribution was utilized for simplicity, making it suitable for analyzing macroscopic systems at elevated temperatures. While its accuracy diminishes as quantum effects become significant, the model provides an effective approximation. Alternatively, the Boltzmann distribution, instead of the Fermi-Dirac distribution, was employed to reformulate the thermionic emission lifetime, leading to the following analytical expression:

$$\begin{aligned}\tau_{esc}^{te} &= \frac{2\pi m^*}{\hbar}\left(\frac{2m^* k_B T}{\hbar^2}\right)^{-1}\sum_{i=1}^{N_b} e^{\frac{(E_{c,b}-E_i)}{k_B T}} + \frac{m^* d}{\hbar}\left(\frac{2m^*\Delta E_B}{\hbar^2}\right)^{-1/2} \\ &\approx \frac{\pi\hbar}{k_B T}\sum_{i=1}^{N_b}\exp\left(\frac{E_{c,b}-E_i}{k_B T}\right) + \frac{\pi\hbar d}{2\pi\Delta E_B}\left(\frac{2m^*\Delta E_B}{\hbar^2}\right)^{1/2}\end{aligned} \tag{3.29}$$

Here, the effective barrier height E_B is the energy difference between the conduction band edge in the GaAs barrier ($E_{c,b}$) and the first sub-band of the InGaAs QW (E_1). The QW width is denoted by d, and m^* represents the electron effective mass. k_B is the Boltzmann constant, T is the temperature in kelvins, and $[\hbar^2/2m^*\Delta E_B]^{1/2}$ determines the characteristic length scale associated with ΔE_B. The term N_b indicates the number of bound sub-bands, and E_i denotes the energy of the i^{th} bound sub-band. A detailed derivation of this equation is presented in chapter 2, subchapter 2.7.

This modified thermionic emission model also incorporates the effects of carrier LO

doi:10.6342/NTU202500212

phonon interaction, which play a significant role in the escape rate due to polar scattering. At elevated temperatures, electrons can absorb LO phonons and escape from the QW. To account for this, a temperature-dependent term $[\exp(\hbar\omega_{LO}/k_B T) - 1]^{-1}$, derived from the Bose-Einstein distribution function, was included in the escape rate [96], [97]. Consequently, the escape time due to thermionic emission can be expressed as

$$\tau_{esc} \approx \left[\frac{1}{\tau_{esc}^{te}} + \frac{1}{\tau_{LO}} \frac{1}{\exp\left(\frac{\hbar\omega_{LO}}{k_B T}\right) - 1} \right]^{-1} \tag{3.30}$$

Here, τ_{LO} represents the electron escape time from the bound states to unconfined states due to the absorption of LO phonons, and $\hbar\omega_{LO}$ is the LO phonon energy.

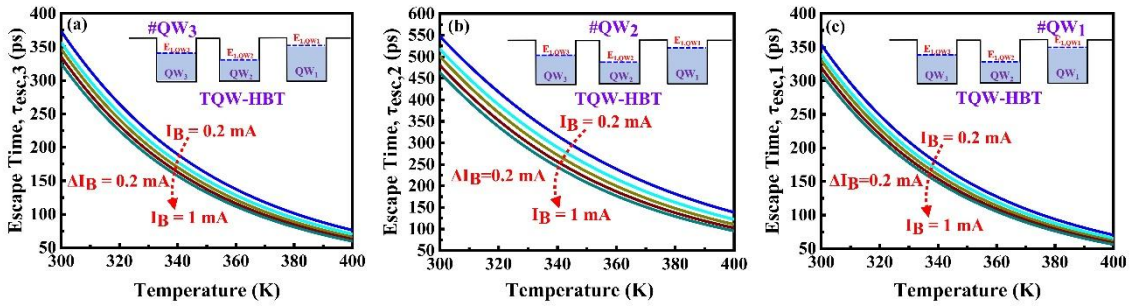


Fig. 3.10: Temperature-dependent escape times for different base currents in the QW of TQW-HBT. (a) Escape time from QW_3 ($\tau_{esc,3}$), (b) escape time from QW_2 ($\tau_{esc,2}$), and (c) escape time from QW_1 ($\tau_{esc,1}$). The insets illustrate the sub-band energy level positions in the TQW.

We extracted the capture time (τ_{cap}), escape time (τ_{esc}), and recombination time (τ_{QW}) as functions of temperature at different base currents I_B by fitting the experimental current gain to the theoretical current gain (β_{TQW}) derived in Eq. (3.25) for TQW-HBTs. These results are illustrated in **Fig. 3.10**, **Fig. 3.11**, and **Fig. 3.12**, respectively. With increasing

doi:10.6342/NTU202500212

electron temperature, the extensive carrier distribution within the QW is significantly influenced by the band filling effect. Consequently, the escape time decreases exponentially with increasing temperature and base current, as depicted in **Fig. 3.10**. The escape times for QW_1, QW_2, and QW_3, shown in **Fig. 3.10 (a), (b), (c)**, respectively, differ due to variations in their first sub-band energy levels in the QWs, which are determined by the unique layer structure of the TQW-HBT.

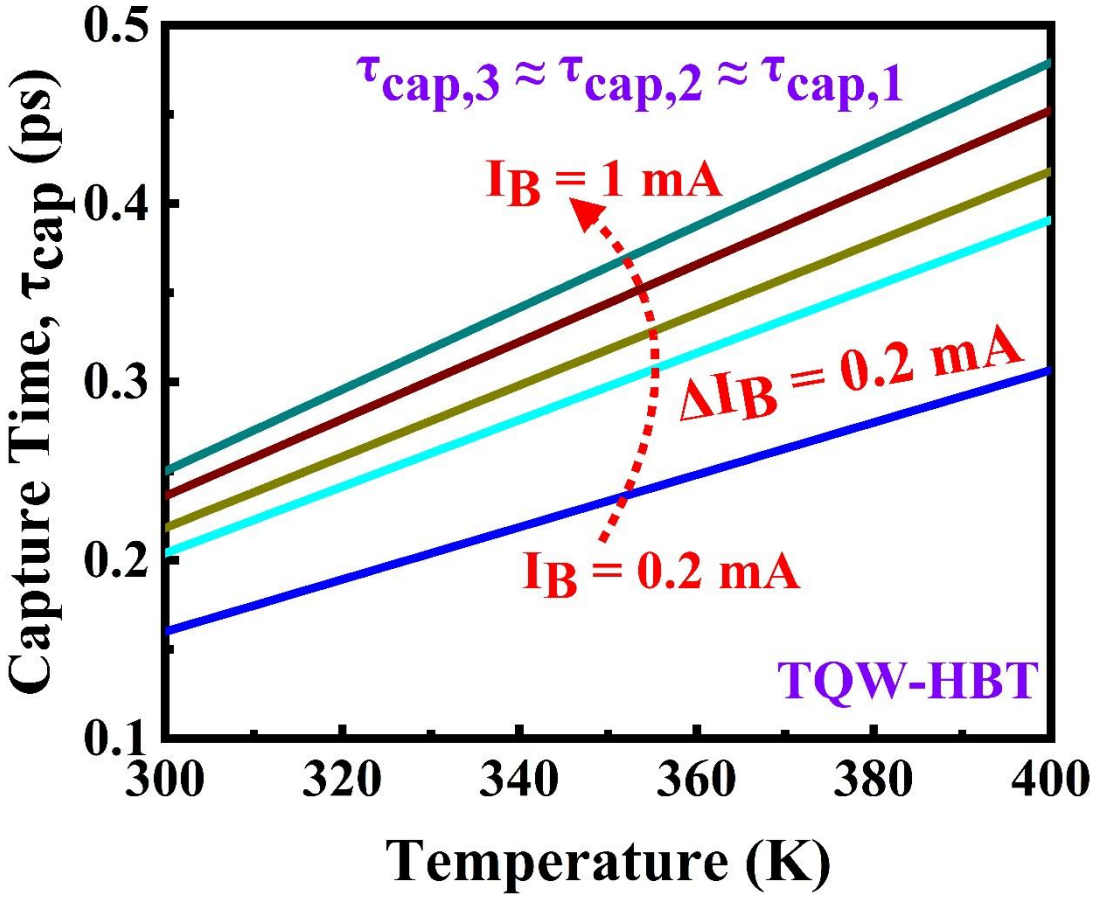


Fig. 3.11: Capture time τ_{cap} as a function of temperature T for various base currents ranging from 0.2 mA to 1 mA. Assume nearly equal captures times $\tau_{cap,3} \approx \tau_{cap,2} \approx \tau_{cap,1}$ in all the QWs.

We also incorporated self-heating effects in our analysis, which demonstrate that the

doi:10.6342/NTU202500212

junction temperature in our TQW-HBTs is lower than that in conventional HBT. However, as the base current and temperature increase, the capture time increase significantly. This phenomenon occurs because carriers transitioning from bulk states to the QW states face restrictions at available states, leading to prolonged captures times. Additionally, the capture time is also influenced by the device's operating current-voltage conditions. With increasing base current, the scattering rate decreases, resulting in increased capture time due to the increased Fermi wavevector, as shown in **Fig. 3.11**.

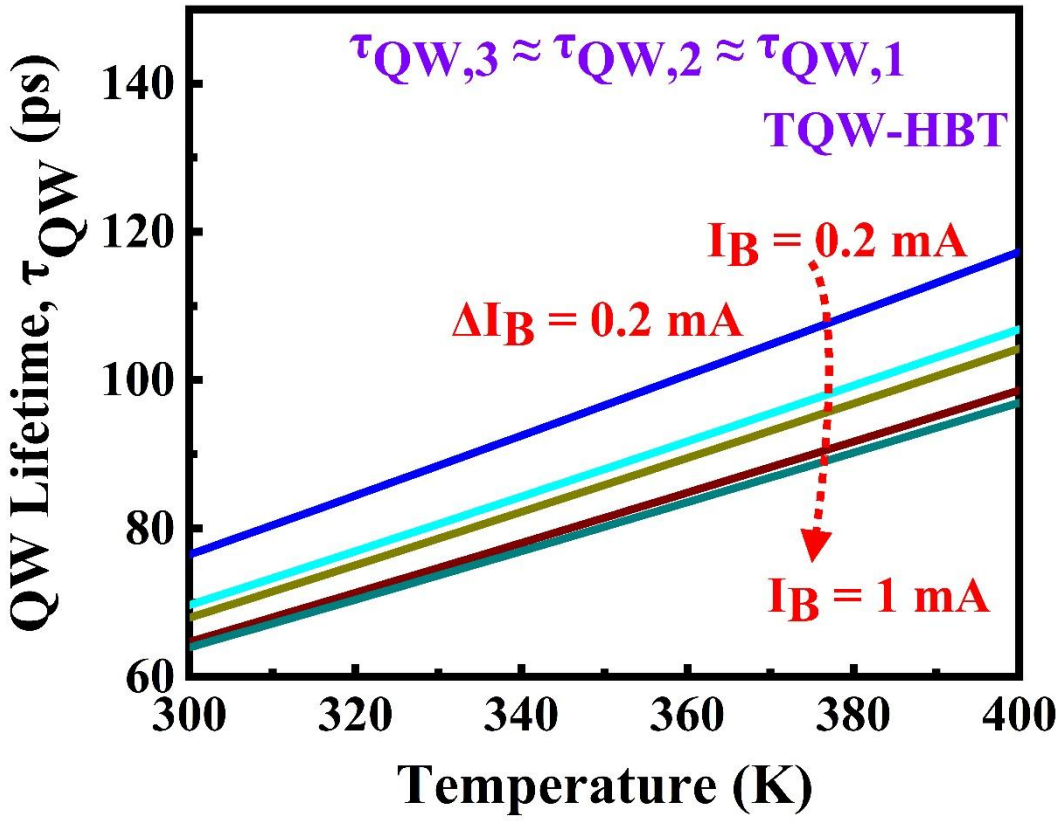


Fig. 3.12: Recombination lifetime τ_{QW} as a function of temperature T for different base currents ranging from 0.2 mA to 1 mA. Note: Assume nearly equal recombination times $\tau_{QW,3} \approx \tau_{QW,2} \approx \tau_{QW,1}$ in all the QWs.

doi:10.6342/NTU202500212

The QW recombination time (τ_{QW}) was also extracted as a function of temperature and base currents, as shown in **Fig. 3.12**. Among these three timescales, the QW recombination time and capture time exhibit less sensitivity to temperature variations compared to the escape time in the QW. Furthermore, τ_{esc} shows a more pronounced variation with temperature than a bulk recombination time τ_b and transit time $\tau_{t,EC}$.

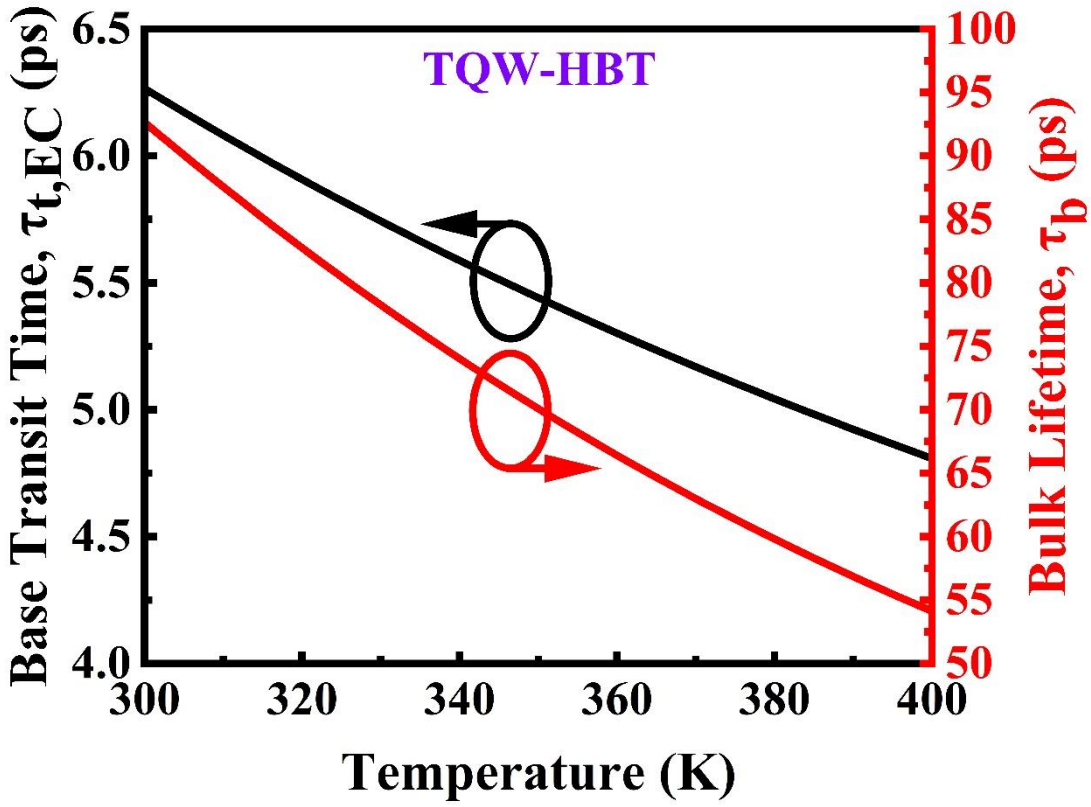


Fig. 3.13: Base transit time $\tau_{t,EC}$ (solid black line) and bulk recombination lifetime τ_b (solid red line) as a function of temperature T.

Carrier recombination and transit time are critical factors influencing the performance of TQW-HBTs. The base region of TQW-HBTs is heavily doped with a p-type dopant concentration of approximately 3×10^{19} cm^{-3}. This high doping level primarily impacts

doi:10.6342/NTU202500212

the minority carrier mobility μ_e^p through ionized impurity scattering, although its influence diminishes at elevated temperatures due to phonon scattering. Phonon scattering, proportional to temperature, reduces minority carrier mobility with increasing temperatures, albeit with a lesser impact at higher temperatures [69], [70]. The base transit time $\tau_{t,EC}$ was analyzed as a function of temperature using Einstein's relationship, $D_n = \mu_e^p k_B T/q$, considering the temperature dependency of minority carrier mobility μ_e^p. As shown in **Fig. 3.13** (solid black line), the transit time decreases by approximately 23.25% when the temperature rises from 300 to 400 K, suggesting a moderate dependency of minority carrier mobility μ_e^p on temperatures.

Next, we examined the bulk recombination time in the heavily p-doped base as a function of temperature T, as illustrated in **Fig. 3.13** (solid red line). The bulk lifetime was modeled using the Shockley-Read-Hall (SRH) recombination, radiative recombination, and Auger recombination mechanisms same as Eq. (2.28):

$$\tau_{rec} = \left(\frac{1}{\tau_{SRH}} + \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}}\right)^{-1} = (A_0 + B_0 P + C_0 P^2)^{-1} \quad (3.31)$$

Here, P represents the doping concentration in the base region; and A_0, B_0, and C_0 corresponds to the SRH, radiative, and Auger recombination coefficients, respectively. This SRH, radiative, and Auger recombination times are denoted as τ_{SRH}, τ_{rad}, and τ_{Auger}, respectively. In heavily doped GaAs semiconductors, Auger recombination becomes dominant due to the high impurity and carrier densities. At higher temperatures,

doi:10.6342/NTU202500212

the energy bandgap E_g shrinks, reducing the threshold kinetic energy E_{th} for high-energy electrons and potentially increasing the Auger recombination coefficient C_0 [73]. Conversely, at room temperature, the recombination process is predominantly governed by band-to-band radiative recombination in the direct band gap GaAs. The radiative recombination lifetime τ_{rad} is related to the spontaneous emission coefficient B_0, which varies with $T^{-3/2}$ for the bulk materials with parabolic bands and T^{-1} for quantum wells with separated bands [71], [72]. In our temperature-dependent charge-control model, the SRH recombination time τ_{SRH} is substantially longer than the radiative and Auger recombination times. As B_0 is treated as constant in this model, the bulk lifetime τ_b decreases by approximately 41.55% as the temperature T increases from 300 to 400 K, as shown in **Fig. 3.13** (solid red line). These findings indicate that Auger recombination dominates the bulk recombination process at higher temperatures.

This comprehensive analysis highlights the intricate dependencies of recombination and transit times on temperatures and doping concentration, emphasizing their critical role in determining the performance of TQW-HBTs under varying operating conditions. The modified thermionic emission model provides a robust framework, particularly in the context of narrow QWs, enabling enhanced understanding and optimization of TQW-HBT devices.

To understand the charge distribution in the TQW and base regions at high temperatures,

doi:10.6342/NTU202500212

the theoretical framework for temperature-dependent charge analysis, as expressed in Eqs. (3.22) and (3.23), underestimates the charge distribution within the TQWs and base region. The ratio of total charge stored in the TQWs to the base charge Q_0 is represented as

$$\frac{Q_{(QW_3+QW_2+QW_1)}}{Q_0} = \frac{Q_{QW3}}{Q_0} + \frac{Q_{QW2}}{Q_0} + \frac{Q_{QW1}}{Q_0} \tag{3.32}$$

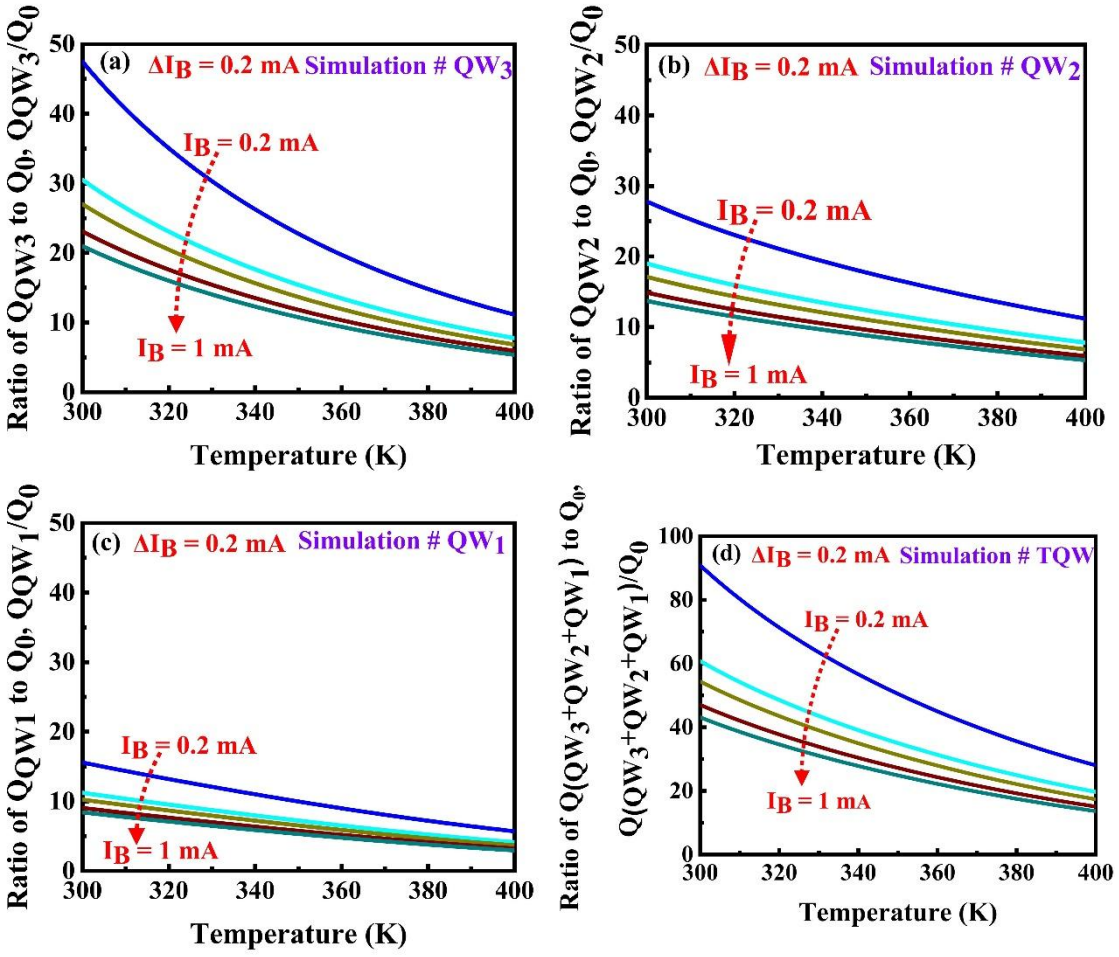


Fig. 3.14: Theoretical simulation of the temperature-dependent ratios based on Eqs. (3.22) and (3.23). (a) Ratio of Q_{QW_3} to Q_0, (b) ratio of Q_{QW_2} to Q_0, (c) ratio of Q_{QW_1} to Q_0 and (d) ratio of $Q_{(QW_3+QW_2+QW_1)}$ to Q_0. The total electrons stored in the TQWs are denoted by $Q_{(QW_3+QW_2+QW_1)}$.

In the fabricated TQW-HBT, it is observed that QW_3 captures a higher number of

doi:10.6342/NTU202500212

electrons compared to QW_2 and QW_1, mainly because of its closer to the emitter. As the temperature increases, electrons gain sufficient thermal energy to escape more readily from the QW. These escaping electrons contribute to the base charge Q_0, altering the charge distribution. The results of our theoretical simulations, using the same parameters as those in **Fig. 3.15**, are illustrated in **Fig. 3.14(a)-(d)**. These simulations demonstrate a decreasing trend in the ratios Q_{QW_3}/Q_0, Q_{QW_2}/Q_0, Q_{QW_1}/Q_0, and $Q_{(QW_3+QW_2+QW_1)}/Q_0$ with increasing temperature and base current. At elevated temperatures, a larger proportion of carriers escape from the QWs and migrate towards the collector. This increased carrier escape rate contributes to a notable amplification in the current gain. The enhanced current gain is directly linked to the redistribution of charges and the increase in Q_0 cause by the elevated electron escape rate, emphasizing the significant thermal dependence of charge dynamics in TQW-HBTs.

3.10 Experimental Validation of Simulated Current Gain in TQW-HBT: Results and Discussion

In the fabricated TQW-HBT device, the three QWs act as electron capture regions, analogous to buckets, that trap electrons traveling from the emitter to the collector. As the temperatures rises, the electron escape time, τ_{esc} decreases exponentially with $1/k_BT$, allowing electrons stored in the TQWs to acquire sufficient energy to escape. At elevated

doi:10.6342/NTU202500212

temperatures, these escaping electrons contribute to the base charge Q_0. Under the influence of base-collector (B-C) reverse bias, the escaped electrons are swept into the collector, thereby increasing both the collector current $I_C = AQ_0/\tau_{t,EC}$ and the current gain β_{TQW}. This leads to significant temperature-dependent variations in both the collector current I_C and the current gain.

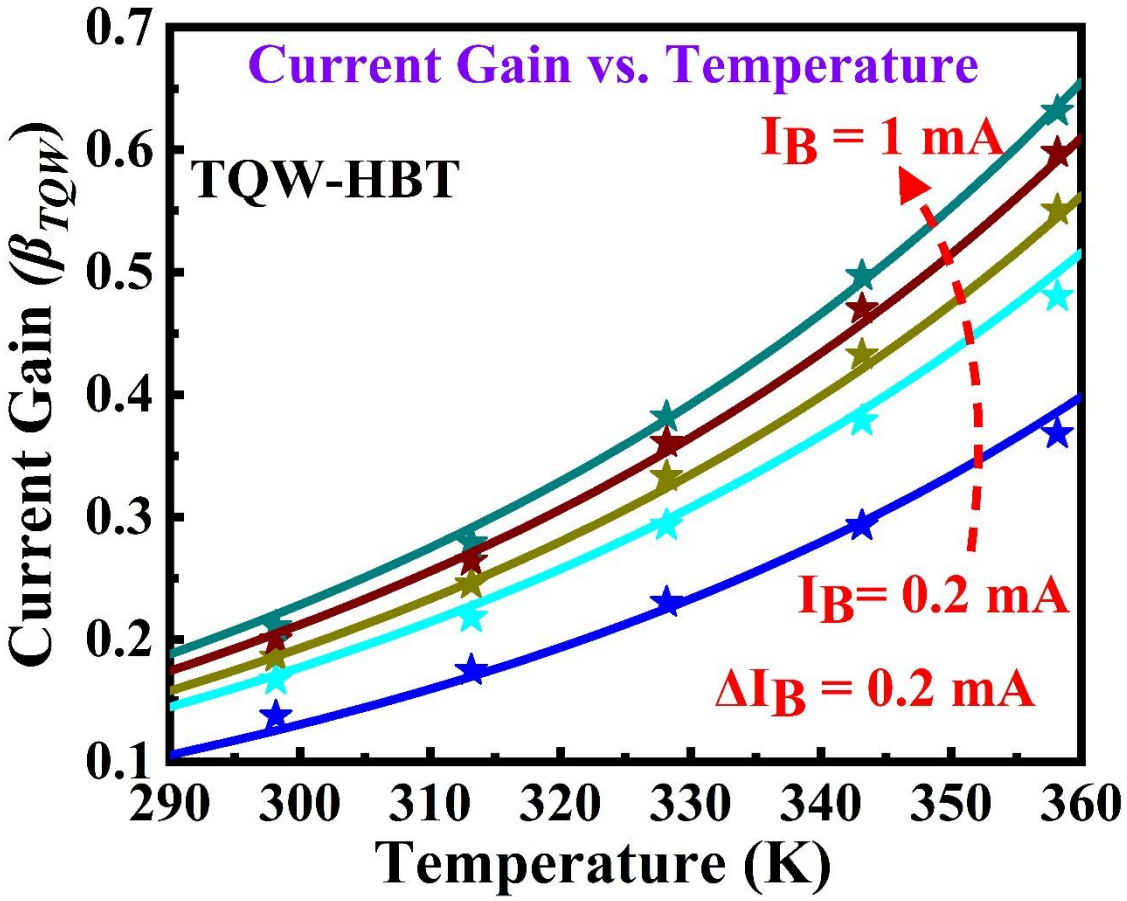


Fig. 3.15: Temperature dependence of current gain β_{TQW} in TQW-HBT for varied base currents (0.2 mA to 1 mA): experimental results (solid stars) and simulation results (solid line).

Figure 3.15 illustrates the experimentally measured current gain as a function of temperature T under different base currents, represented by family curves at $V_{BC} = 0$.

doi:10.6342/NTU202500212

These experimental results are compared with the simulated current gain trends at varying base currents. The simulation results, particularly at a base current of I_B of 0.2 mA, closely align with the experimental data. The parameters used for the simulation at a temperature of 300 K are summarized in **Table 3.4**.

Table 3.4: Analysis of current gain β_{TQW} at 300 K using the following parameters

Parameter	W_B	W_{3C}	W_{2C}	W_{1C}	W_{31}	W_{32}
Value (Å)	1120	565	460	355	210	105
Parameter	W_{21}	W_{E1}	W_{E2}	W_{E3}	d	τ_{EC}
Value	105 Å	765 Å	660 Å	555 Å	70 Å	6.26 ps
Parameter	τ_{b}	τ_{cap}	τ_{QW}	$\tau_{\mathrm{esc},3}$	$\tau_{\mathrm{esc},2}$	$\tau_{\mathrm{esc},1}$
Value (ps)	92.63	0.16	76.50	373.34	547.83	353.73
Parameter	QW_3		QW_2		QW_1	
	ΔE_B	$E_{\mathrm{c,b}}-E_1$	ΔE_B	$E_{\mathrm{c,b}}-E_1$	ΔE_B	$E_{\mathrm{c,b}}-E_1$
Value(meV)	308.7	234.17	319.45	256.98	307.38	231.66

Efforts were made to fit the experimental measurements data across various base currents, beyond 0.2 mA, by adjusting parameters that linearly depends on both base current and temperature. However, at higher base currents, internal heating within the device required more precise experimental calibration to achieve a theoretical fit with the measured current gain. Despite these challenges, the simulation results were largely consistent with the experimental results, which was satisfactory. Notably, as thermionic emission causes

doi:10.6342/NTU202500212

electrons to escape from the QWs, the collector current at I_B of 1 mA increases by approximately 200% when the temperature rises from 25ºC to 85ºC. This indicates that at higher temperature T, a larger number of carriers escape from the QWs and are collected at the collector, resulting in a higher current gain.

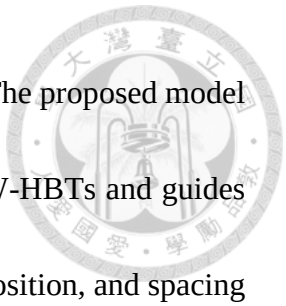
The sensitivity of the TQW-HBTs is defined as the change in the collector current with respect to temperature $(\Delta I_C/\Delta T)$, which distinguishes it from the sensitivity (change in voltage with respect to temperature, $\Delta V/\Delta T$) commonly defined in conventional BJT or PIN diode-based thermal sensors. The average current-to-temperature signal of the TQW-HBT is 7 μA/℃, demonstrating significant promise for high-resolution temperature sensing.

In future work, more complex circuit designs incorporating passive components will be explored, allowing for sensitivity to be redefined as $\Delta V/\Delta T$. This will facilitate more meaningful comparisons with existing technologies. The substantial current-to-temperature signal of the TQW-HBT highlights its potential for integration into OEICs, paving the way for advanced smart temperature-sensing applications.

3.11 Conclusion

This chapter presents the development of a modified charge-control model for MQW-HBTs, which accurately predicts the current gain of transistors using continuity

doi:10.6342/NTU202500212



equations tailored for LETs incorporating MQWs within their base. The proposed model provides valuable insights into the operational behavior of the MQW-HBTs and guides the design of efficient epi-layer structures by optimizing the width, position, and spacing of each QW in the base. Our findings reveal a trade-off between the collector current gain and optical modulation gain, as the addition of more QWs in the transistor base reduces the current gain. Analytical results demonstrate that the position of the MQWs within the base significantly influences the current gain, with the highest gain achieved when the MQWs are placed closer to the collector. This study also highlights the role of QW positioning and the number of QWs in capturing charges, which in turn impacts the transistor's overall current gain. To validate the modified charge-control model, we utilized experimental data from prior work on 1QW-HBTs and 2QW-HBTs. The model demonstrates its potential for designing efficient epitaxial layers in MQW-HBTs, specifically for the front-end components of smart thermal sensors and OEICs.

Using this modified model, the TQW-HBT epi-layer was designed and successfully fabricated specifically for thermal sensor applications. Experimental and simulation results demonstrate that the current gain of TQW-HBTs increases significantly with rising substrate temperatures. The model integrates thermionic emission theory, highlighting that minority carriers in the TQWs gain sufficient energy at elevated temperatures to

doi:10.6342/NTU202500212

escape more readily due to reduced escape times. This phenomenon, contrary to conventional HBT behavior, leads to a significant enhancement in current gain. Notably, the collector current increased by approximately 200% as the operating temperature rose from 25℃ to 85℃, with experimental findings closely aligning with simulation results. The modified charge-control model successfully explains the thermo-electric enhancement of current gain in TQW-HBTs, validating its effectiveness in designing efficient epitaxial layers. The theoretical predictions align closely with experimental trends, further confirming the model's accuracy.

The TQW-HBT demonstrated a current sensitivity of 7 μA/℃ under the bias conditions I_B of 1 mA and V_{CE} of 2 V, showcasing its potential as a high-resolution temperature sensor. This high current-to-temperature signal establishes the TQW-HBT as a strong and promising candidate for front-end components in advanced smart thermal sensing technologies.

In conclusion, this work highlights the potential of TQW-HBTs as thermally enhanced devices with significant applications in next-generation temperature sensing technologies and OEICs. The insights gained and methodologies developed pave the way for further advancements in this promising field.

doi:10.6342/NTU202500212

Chapter 4

Design and Fabrication of Novel Darlington Transistor Using LET for Smart Thermal Sensor Technology

4.1 Introduction

This chapter introduces a groundbreaking invention in thermal sensing technology, highlighting the unique thermally induced current gain enhancement achieved through a first-of-its-kind Darlington pair circuit based on a cascaded three-port high-speed LET. The integration of LETs with Darlington transistor configurations represents a significant advancement in the development of smart thermal sensor technologies, offering unprecedented improvements in thermal sensitivity and current gain. This chapter explores the motivation, design, fabrication, and characterization of a novel Darlington transistor employing LETs, aiming to address the limitations of conventional thermal sensors and establish a new benchmark in thermal sensing applications.

The chapter begins by discussing the "Motivation Behind the Novel Darlington Transistor Design by Cascading of SQW-HBTs" (Subchapter 4.2). This section highlights the need for innovative designs to improve the temperature sensitivity of LETs and the rationale behind adopting a cascading configuration of SQW-HBTs. By leveraging thermionic emission and quantum well effects, this design achieves significant improvements in

doi:10.6342/NTU202500212

current amplification and thermal responsiveness.

The insights gained from Subchapter 4.2 lead to the detailed “Device Design and Layer Structure of the Darlington Transistor” (Subchapter 4.3). Here, the epi-layer structural framework and functional aspects of the Darlington transistor are presented, focusing on the incorporation of quantum wells to facilitate thermionic emission and enhance thermal sensing performance. This section also explains how the choice of materials and device structure ensures superior linearity and sensitivity across a range of temperatures.

Building on the design principles established in Subchapter 4.3, the “Device Fabrication Process for the Darlington Transistor” is elaborated in Subchapter 4.4. This section outlines the step-by-step fabrication methodology, including material deposition, etching, and integration processes, while addressing the challenges encountered during fabrication. Special attention is given to optimizing the quantum well properties and ensuring consistency in device performance.

The fabricated device is then characterized at varying substrate temperatures in Subchapter 4.5, “Device Characterization at Different Substrate Temperatures.” This section presents experimental data validating the temperature-dependent performance of the Darlington transistor, including its current gain, collector current, and thermal

doi:10.6342/NTU202500212

sensitivity. The characterization underscores the device's capability as a robust thermal sensor under practical operating conditions.

To enable meaningful comparisons with existing thermal sensor technologies, Subchapter 4.6 focuses on the “ADS Modeling of the Darlington Transistor: Converting Current Sensitivity to Voltage Sensitivity for Comparison with Existing Technologies.” Advanced Design System (ADS) modeling tools are employed to convert current-to-temperature signals into voltage-to-temperature signals, highlighting the superior performance of the Darlington transistor over traditional thermal sensors in terms of sensitivity and linearity.

Notably, the findings of this study have been published in the reputed high-impact journal *IEEE Electron Device Letters*: Mukul Kumar et al., “Design and fabrication of novel Darlington transistor using light-emitting transistors for smart thermal sensor technology,” *IEEE Electron Device Letters*, vol. 45, no. 7, pp. 1365–1368, July 2024, doi:10.1109/LED.2024.3401084.

Finally, this chapter provides a comprehensive overview of the design and development process for the novel Darlington transistor. It not only demonstrates the potential of LET-based Darlington configurations in advancing thermal sensor technology but also lays a

doi:10.6342/NTU202500212

strong foundation for future research in OEICs and high-precision smart thermal sensing technology application.

4.2 Motivation Behind Novel Darlington Transistor Design by Cascading of SQW-HBTs

The unique properties of QWs, particularly their thermionic emission dominance, make QW-based HBTs promising candidates for thermal sensor applications. As demonstrated in Chapters 2 and 3, single-QW (SQW)-HBTs and triple-QW (TQW)-HBTs exhibit high thermal sensitivity, making them suitable candidates for temperature sensing. However, the incorporation of QWs in the base region of HBTs significantly reduces the current gain compared to conventional HBTs. Despite this drawback, the temperature-dependent sensitivity of these devices makes them valuable for thermal sensing purposes.

For the design of a smart thermal sensor, achieving both high sensitivity and accuracy is of paramount importance. This chapter introduces a novel approach to enhance thermal sensitivity by increasing both the temperature-induced current and the current gain of the device. This proposed design involves a Darlington transistor pair configuration, utilizing cascaded n-p-n LETs. The temperature-sensitive characteristics of this configuration are analyzed under varying substrate temperatures.

doi:10.6342/NTU202500212

The proposed novel Darlington transistor demonstrates ultra-high thermal sensitivity, surpassing that of existing thermal sensors used in sensing devices. This enhanced sensitivity is attributed to thermionic emission phenomena within the QWs, which enable the Darlington transistor to operate effectively as a smart thermal sensor for both electrical and optical sensing. With LETs offering dual outputs, the design holds potential for multifunctional sensing applications.

This study highlights the distinctive thermal properties of III-V-based transistors and underscores their potential to advance next-generation sensor technologies. By leveraging the strengths of QW-based HBTs and the Darlington transistor configuration, this work paves the way for the development of high-performance, smart thermal sensor technologies.

4.3 Device Design and Layer Structure of Darlington Transistor

The epitaxial structure of the n-p-n LETs, designed to study current-voltage (I-V) characteristics for high-temperature applications, is depicted in **Fig. 4.1**. These devices are fabricated using MOCVD on (100)-oriented semi-insulating (S.I.) GaAs substrates. Silicon (Si) and carbon (C) are utilized as n-type and p-type dopants, respectively, to achieve precise doping levels across the device structure.

The epitaxial growth begins with a heavily n-type doped GaAs buffer layer, 8500 Å thick,

doi:10.6342/NTU202500212

deposited on the S.I. GaAs substrate to mitigate lattice mismatch issues. Following this, the n-type bottom confinement layer, acting as a distributed Bragg reflector (DBR) to enhance vertical recombination radiation escape, consists of a sequence of layers: 634 Å of $Al_{0.4}Ga_{0.6}As$, 500 Å of $Al_{0.95}Ga_{0.05}As$, and 150 Å of $Al_{0.4}Ga_{0.6}As$. Above the DBR, the structure incorporates a heavily n-type doped GaAs subcollector layer (200 Å), an n-type $In_{0.49}Ga_{0.51}As$ etching stop layer (120 Å), and an n-type $Al_{0.05}Ga_{0.95}As$ collector layer (800 Å). The active region includes a heavily graded p-type doped GaAs base layer (890 Å), with a doping concentration ranging from $1x\ 10^{19}\ cm^{-3}$ to $4\ x\ 10^{19}\ cm^{-3}$. Incorporated within this base layer is an undoped 70-Å $In_{0.2}Ga_{0.8}As$ quantum well, designed for $\lambda \approx 980\ nm$, sandwiched by undoped 10-Å-thin GaAs buffer layers and a 100-Å $Al_{0.025}Ga_{0.975}As$ layer positioned just above the collector layer. The structure is completed with a 250-Å n-type $In_{0.49}Ga_{0.51}P$ wide-bandgap emitter layer, followed by a 4300-Å n-type $Al_{0.35}Ga_{0.65}As$ confinement layer. Finally, a heavily n-type doped 1000-Å GaAs emitter cap layer is added to ensure low-resistance ohmic contact for the emitter.

The fabrication process begins with wet etching to form the emitter and collector mesas, followed by isolation etching down to the S.I. GaAs substrate. Standard photolithography techniques are employed to define contact regions, and metallization is carried out to deposit the contacts for the emitter (E), base (B), and collector (C). The process is finalized with planarization, via hole etching, and pad metallization to ensure the precise

doi:10.6342/NTU202500212

electrical connectivity. This meticulous fabrication approach ensures the realization of both the n-p-n LET and the Darlington transistor structure with high precision and functionality. A detailed fabrication process flow is presented in the subsequent Subchapter of chapter 4. **Table 4.1** summarizes the composition and specifications of each layer in the epitaxial structure. The described design and fabrication process enable the realization of high-performance Darlington transistors with enhanced functionality for smart thermal sensor technology.

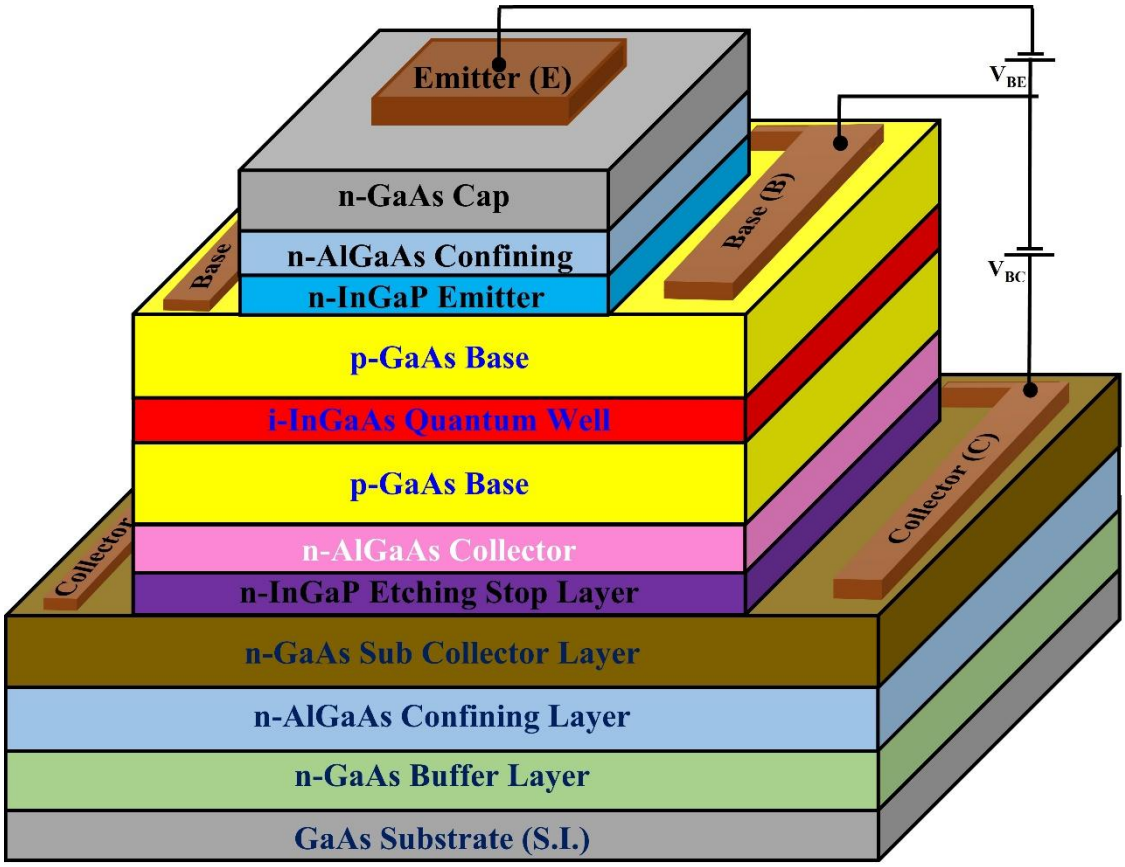


Fig. 4.1: Schematic of the epitaxial layer structure of the n-p-n QW-HBT (LET).

doi:10.6342/NTU202500212

Table 4.1: The epitaxial layer structure design of n-p-n LET

Layer Name	Material	Mole Fraction (x)	Thickness (Å)	Type	Doping Level (Cm^{-3})	Dopant
Contact	GaAs		1000	N^+	5e18	Si
Confining	$Al_xGa_{1-x}As$	0.35	4000	N	3e18	Si
Oxidizable	$Al_xGa_{1-x}As$	0.35	150	N	8e17	Si
Oxide Buffer	$Al_xGa_{1-x}As$	0.35	150	N	5e17	Si
Emitter	$In_xGa_{1-x}P$	0.49	250	N^-	5e17	Si
Base	GaAs		100	P	4e19	C
Base	GaAs		100	P	2e19	C
Base	GaAs		200	P	1e19	C
Buffer	GaAs		10	i		UID
QW	$In_xGa_{1-x}As$	0.2	70	i		UID
Buffer	GaAs		10	i		UID
Base	GaAs		300	P	1e19	C
Base	$Al_xGa_{1-x}As$	0.025	100	P	3e19	C
Collector	$Al_xGa_{1-x}As$	0.05	800	i	2e16	UID
Order	$In_xGa_{1-x}P$	0.49	120	N^-	3e16	Si
Sub-Collector	GaAs		200	N	5e18	Si
Oxide Buffer	$Al_xGa_{1-x}As$	0.4	150	N	3e18	Si
Oxidizable	$Al_xGa_{1-x}As$	0.95	500	N	3e18	Si
Oxide Buffer	$Al_xGa_{1-x}As$	0.4	634	N	3e18	Si
Buffer Layer	GaAs		8500	N	5e18	
Substrate 4" GaAs S.I.						

4.4 Device Fabrication Process for Darlington Transistor

This Subchapter provides a comprehensive description of the fabrication process for the devices this chapter, including SQW-HBT and Darlington transistor, which consists

doi:10.6342/NTU202500212

of two cascaded SQW-HBTs. The fabrication was carried out using a range of standard semiconductor processing techniques. The fabrication methods and equipment employed include photolithography, wet etching, metal lift-off, thermal annealing, RIE, electron-beam evaporation, thermal evaporation, PECVD. The detailed step-by-step explanation of the device fabrication process are given below:

1) Sample Cleaning

Before starting each fabrication step, the substrate is cleaned to remove any contaminants and prepare it for spin-coating the photoresist. The cleaning process includes soaking the substrate in acetone at 95℃ for 5 minutes, followed by soaking it in methanol at 95℃ for another 5 minutes. Afterward, the substrate is rinsed with IPA and dried with a nitrogen gun. Finally, it is baked at 110℃ for 5 minutes to remove any remaining organic substances. **Figure 4.2** shows the substrate's epitaxial cross-section after cleaning.

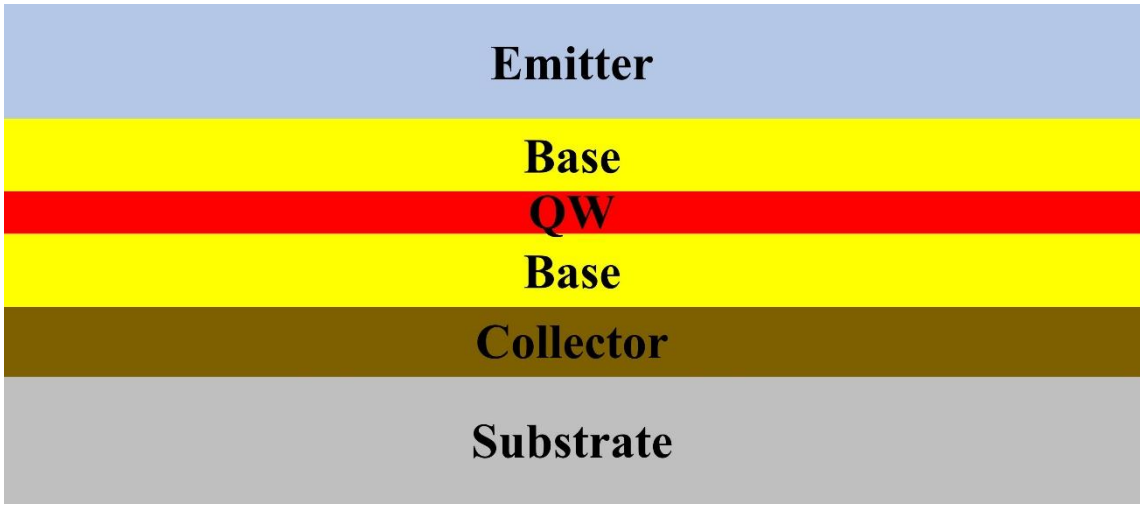


Fig. 4.2: Epitaxial cross-sectional view after cleaning

doi:10.6342/NTU202500212

2) Emitting Mesa Etching

The emitter mesa etching process begins by spin-coating the substrate with S1813 photoresist at 1000 rpm for 10 seconds, followed by 4000 rpm for 60 seconds to achieve a uniform coating. The substrate is then soft-baked at 110℃ for 1 minute to stabilize the photoresist. After soft baking, the photoresist around the edges of the substrate is removed to ensure a flat photoresist layer. Next, a light-field photomask is used with an MA6 mask aligner to define the emitter pattern. The photoresist is developed by immersing the substrate in MF319 developer with gentle agitation, followed by rinsing with deionized water and drying with a nitrogen gun.

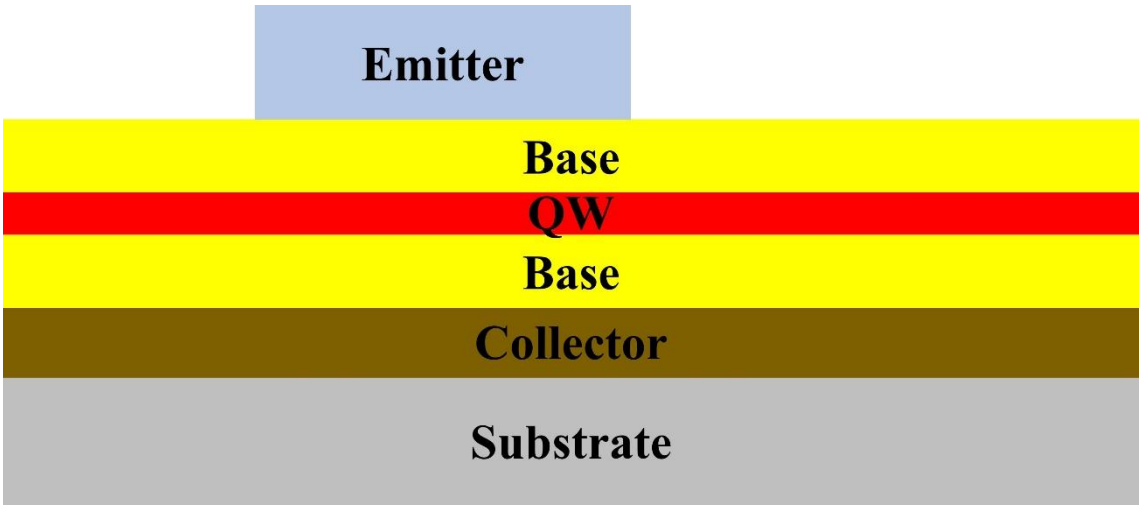


Fig. 4.3: Epitaxial cross-sectional view after emitter mesa etching

To harden the photoresist for wet etching, the substrate is hard-baked at 115℃ for 5 minutes. A diluted sulfuric acid solution (H_2SO_4: H_2O_2: H_2O in a ratio of 1:8:120) is then

doi:10.6342/NTU202500212

prepared, and the substrate is immersed to selectively etch the emitter platform. After etching, the substrate is sequentially cleaned by immersing it in acetone and methanol, rinsing with IPA, and drying with a nitrogen gun to ensure the complete removal of the S1813 photoresist. **Figure 4.3** shows the epitaxial cross-section after emitter platform etching.

3) Base Mesa Etching

The steps for cleaning, photoresist spin-coating, exposure, development, and oxide removal in the base mesa etching process are the same as those used for the emitter platform etching. However, before immersing the substrate in the diluted sulfuric acid solution, it is first dipped in HCl for 3 seconds to remove the InGaP etch stop layer.

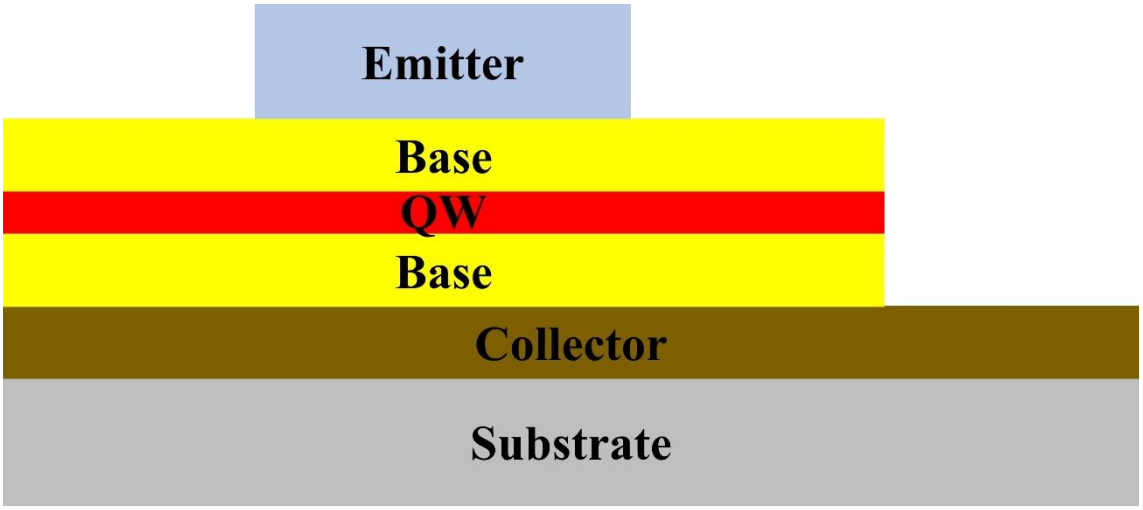


Fig. 4.4: Epitaxial cross-sectional view after base mesa etching.

After the InGaP layer is removed, the substrate is immersed in the diluted sulfuric acid solution for the selective etching of the base platform. Following this, the substrate is

doi:10.6342/NTU202500212

cleaned by sequentially immersing it in acetone and methanol, rinsing with IPA, and drying with a nitrogen gun to ensure the complete removal of the S1813 photoresist. **Figure 4.4** shows the epitaxial cross-section after base platform etching.

4) Emitter and Collector Metal Deposition

After cleaning the substrate, PMGI photoresist is spin-coated onto the wafer at 1000 RPM for 10 seconds, then at 4000 RPM for 60 seconds, and baked at 270℃ for 5 minutes. Next, S1813 photoresist is spin-coated onto the wafer at 1000 RPM for 10 seconds, followed by 4000 RPM for 60 seconds, and baked at 110℃ for 1 minute. After soft baking, the photoresist around the edge of the wafer is removed to ensure a flat photoresist layer. The substrate is then exposed using the MA6 exposure system with a dark-field mask to define the areas for emitter/collector metal deposition. The photoresist is developed by immersing the substrate in MF319 developer with gentle agitation, followed by rinsing with deionized water and drying.

Next, the substrate is exposed to DUV light for 150 seconds and immersed in 101A developer for 50 seconds, followed by rinsing with deionized water to develop the PMGI photoresist. These DUV exposure and 101A development steps are repeated several times to create an undercut photoresist structure. To remove the oxide layer, the substrate is immersed in BOE, followed by rinsing with DI water. The wafer is then placed into an

doi:10.6342/NTU202500212

electron beam evaporator to deposit the metal layers in the following sequence: 500 Å of Au, 250 Å of Ge, 150 Å of Ni, and 1500 Å of Au. After deposition, the substrate is immersed in acetone at 25℃ for 5 minutes, followed by immersion in acetone at 95℃ for 5 minutes to lift off the S1813 photoresist. To remove the PMGI photoresist, the substrate is heated in 90℃ NMP for 10 minutes, then rinsed sequentially with IPA and DI water, and dried with a nitrogen gun. **Figure 4.5** shows the epitaxial cross-section after emitter/collector metal deposition.

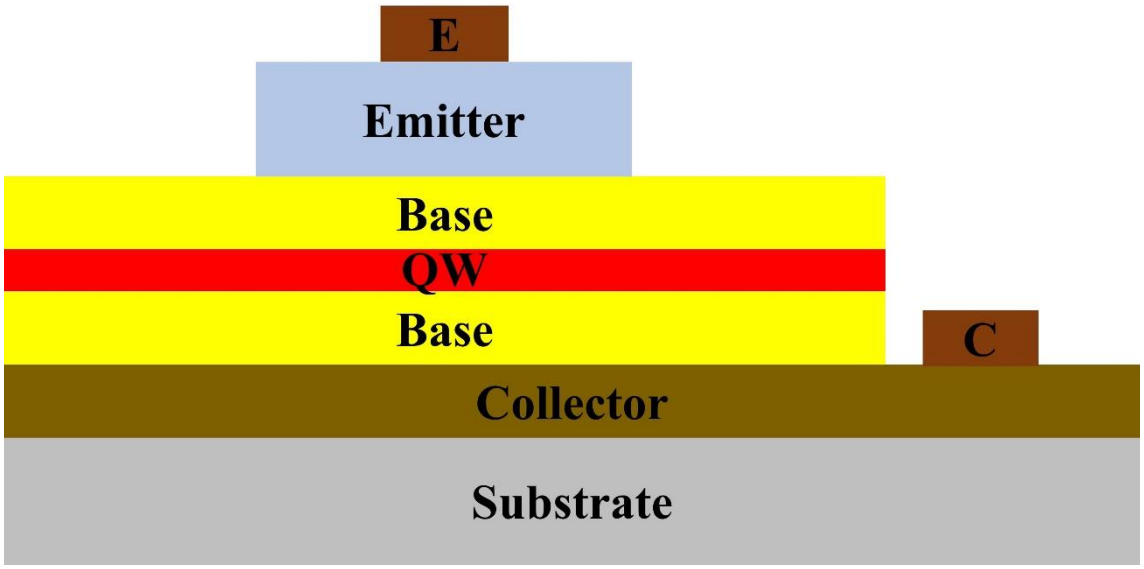


Fig. 4.5: Epitaxial cross-sectional view after E/C metal deposition

5) Thermal Annealing Process

The wafer is subjected to rapid thermal processing (RTP) in a nitrogen environment at 360℃ for 1 minute. This treatment enhances the contact quality of the N-type metal, facilitates atomic rearrangement, and relieves internal stress, ensuring a good ohmic

doi:10.6342/NTU202500212

contact for the N-type metal. The emitter and collector initially show Schottky contact, but after annealing, they exhibit ohmic contact. This behavior can be observed through their current-voltage (I-V) characteristics.

6) Base Metal Deposition

The steps for cleaning the wafer, spin-coating the photoresist, exposure, development, oxide removal, and metal deposition for the base metal deposition process is same as the emitter/collector deposition process. Next, the base contact layer is deposited sequentially with 200 Å of Ti, 200 Å of Pt, and 1500 Å of Au.

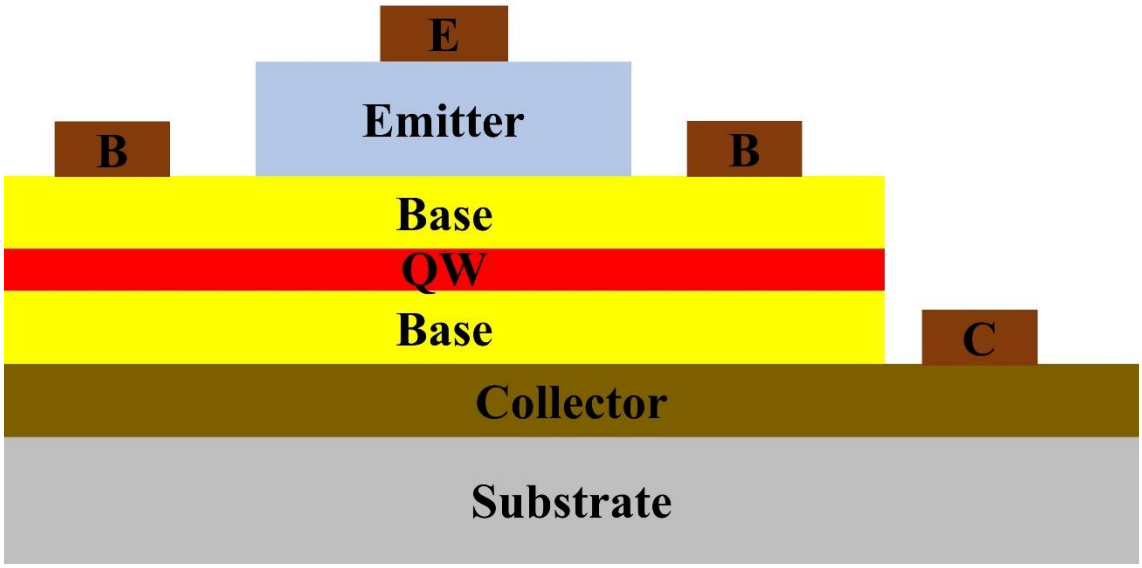


Fig. 4.6: Epitaxial cross-sectional view after base metal deposition

After deposition, the wafer is immersed in acetone at 25℃ for 5 minutes, followed by immersion in acetone at 95℃ for 5 minutes to remove the S1813 photoresist, completing the metal lift-off process. To remove the PMGI photoresist, the wafer is boiled in NMP at 90℃ for 10 minutes, then rinsed with IPA and DI water, and finally dried with nitrogen

doi:10.6342/NTU202500212

gas. **Figure 4.6** shows the epitaxial cross-section after the base metal deposition.

7) Device Isolation

At this stage, the LETs are interconnected. To prevent interference between devices and leakage currents, isolation of the devices is required. The steps for cleaning the wafer, spin-coating the photoresist, exposure, development, oxide removal, and emitter platform etching are the same as described above. The only difference is that before immersing the wafer in diluted sulfuric acid, the wafer needs to be immersed in HCL for 3 seconds to remove the InGaP etching stop layer. After removing the InGaP etching stop layer, the wafer is immersed in a selective etchant to etch down to the undoped GaAs substrate.

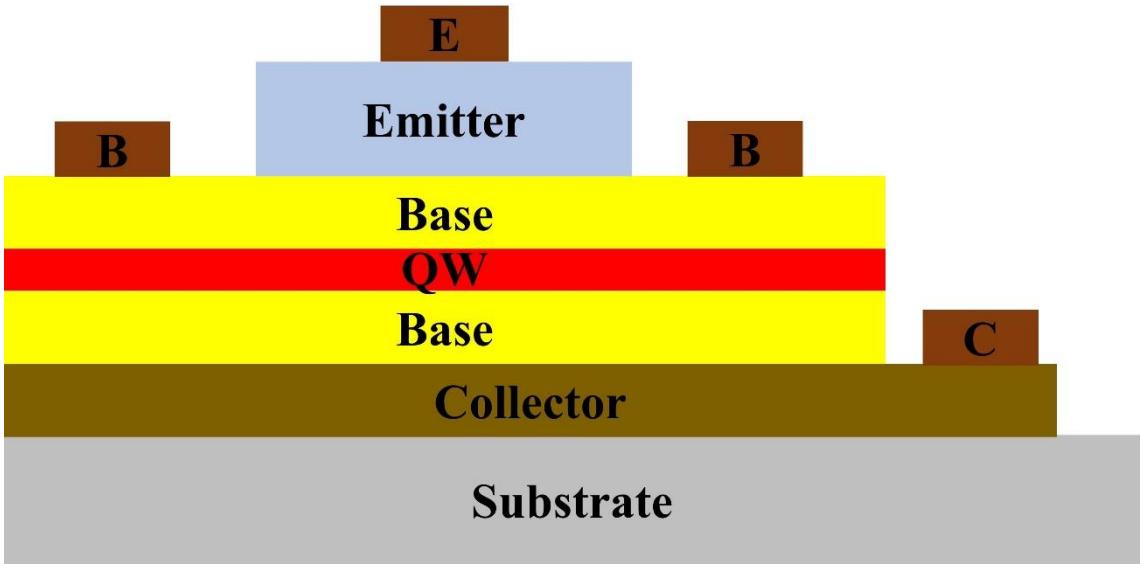


Fig. 4.7: Epitaxial cross-sectional view after isolation device process

Finally, the wafer is sequentially immersed in acetone and methanol, rinsed with IPA, and dried with a nitrogen gun to ensure complete removal of the S1813 photoresist. **Figure 4.7** shows the epitaxial cross-sectional view after the isolation island process.

doi:10.6342/NTU202500212

8) Silicon Nitride Surface Passivation Process and Contact Hole Etching Process

After cleaning the wafer, a silicon nitride layer is deposited as a passivation layer to protect the device and ensure surface planarization. A 3000 Å thick silicon nitride film is deposited using PECVD. The steps for wafer cleaning, spin-coating the photoresist, exposure, development, oxide removal, and emitter platform etching are the same for the contact hole etching process.

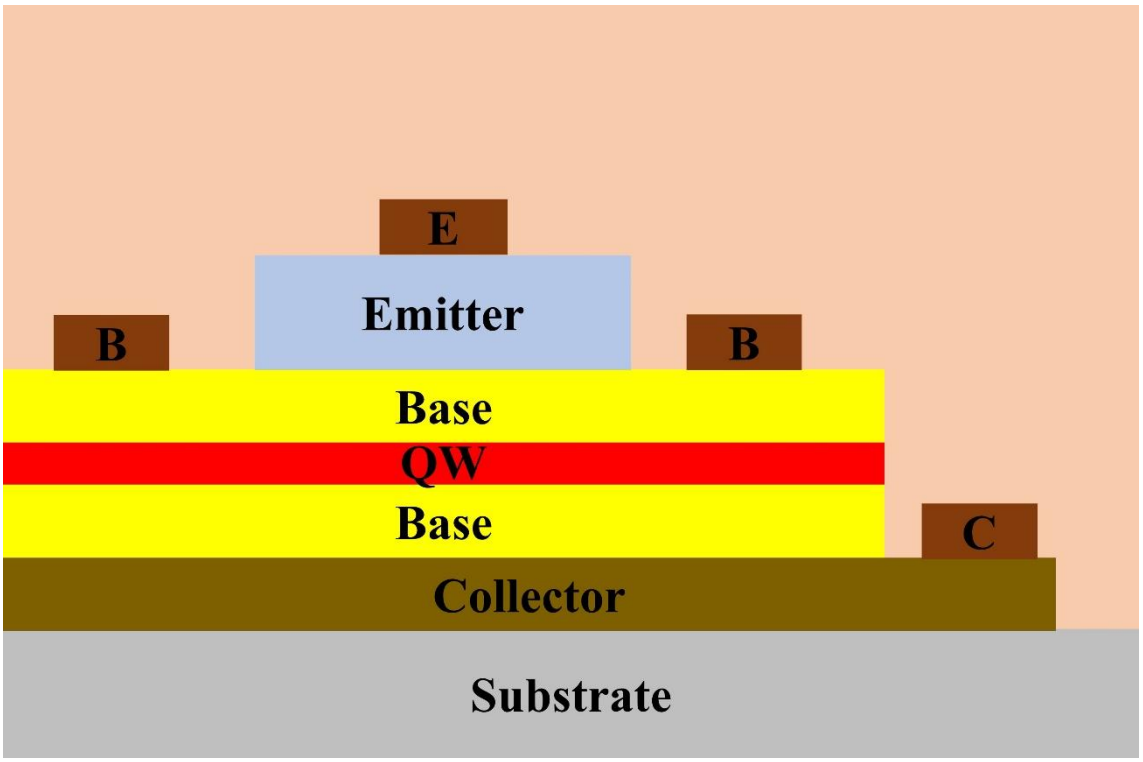


Fig. 4.8: Epitaxial cross-sectional view after silicon nitride surface passivation and contact hole etching processes.

RIE is then used to etch the contact holes. After etching, the wafer is sequentially immersed in acetone and methanol, rinsed with IPA, and dried with a nitrogen gun to

doi:10.6342/NTU202500212

ensure the S1813 photoresist is completely removed. **Figure 4.8** shows the epitaxial cross-sectional view after the silicon nitride surface passivation and contact hole etching processes.

9) Metal Pad and Interconnection (Metal 1)

The process steps for wafer cleaning, spin-coating the photoresist, exposure, development, oxide removal, and emitter/collector metal deposition remain the same. Afterward, a sequential deposition of 500 Å of titanium (Ti) and 15000 Å of gold (Au) is performed to form the metal pad and interconnections between the two LETs. To complete the metal lift-off process, the wafer is immersed in acetone at 25℃ for 5 minutes, followed by acetone at 95℃ for another 5 minutes, to remove the S1813 photoresist.

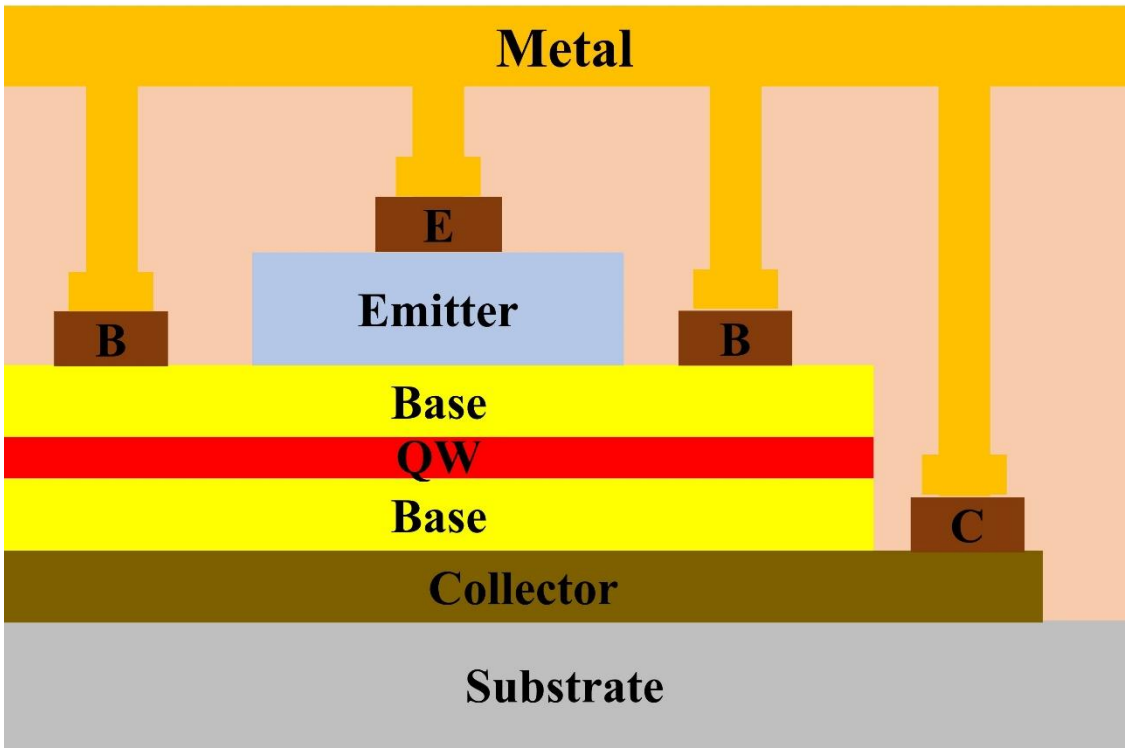


Fig. 4.9: Epitaxial cross-sectional view after interconnection metal and metal pad.

doi:10.6342/NTU202500212

The PMGI photoresist is then removed by boiling the wafer in NMP at 90℃ for 10 minutes. The wafer is subsequently rinsed with IPA and DI water and dried using a nitrogen gun. **Figure 4.9** presents the epitaxial cross-sectional view after completing the interconnection metal and metal pad processes. The final top view images of the LET and Darlington transistor are shown in **Fig. 4.10** (a) and (b), respectively.

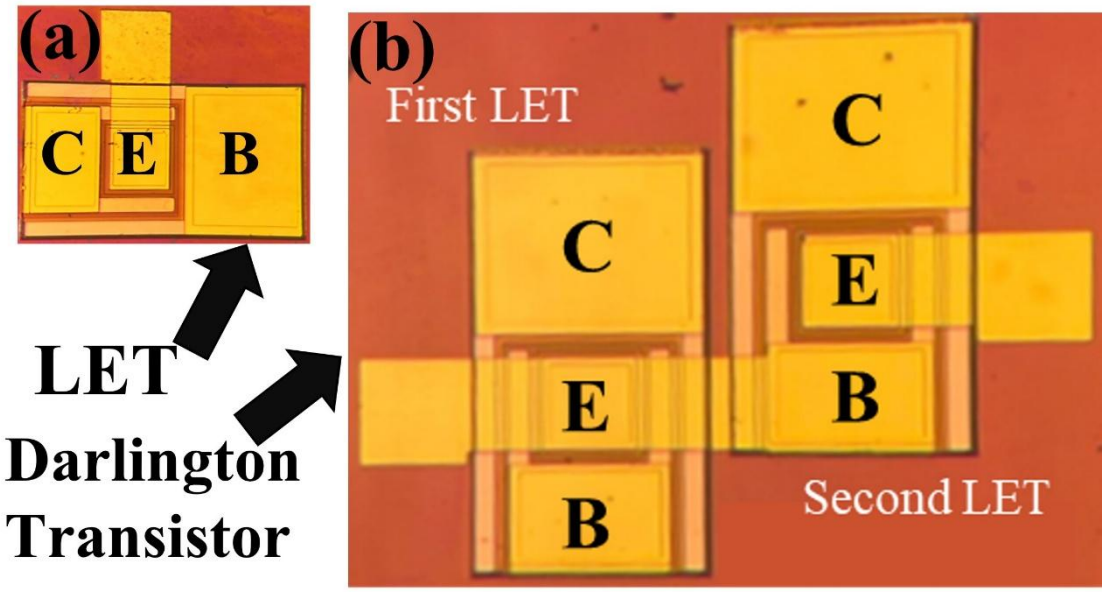


Fig. 4.10: The top view of fabricated device (a) LET, (b) Darlington transistor. The emitter area is 80 μm × 80 μm.

4.5 Device Characterization at Different Substrate Temperature

Following the successful fabrication of both devices, a high-temperature performance evaluation was conducted. Each LET and Darlington transistor were placed on a Peltier temperature-controlled stage for 20 minutes to allow the temperature control

doi:10.6342/NTU202500212

stage to stabilize. However, the circuit itself reached equilibrium within 2 minutes. Electrical biasing and current were supplied using an Agilent E5270B instrument, with the base current varied from 0.25 mA to 1 mA and the collector-to-emitter voltage increased from 0 V to 4 V. The collector current versus collector-to-emitter voltage characteristics for both the LET and Darlington transistor were carefully measured at substrate temperatures ranging from 25℃ to 85℃, as shown in **Fig. 4.11** and **Fig. 4.12**, respectively.

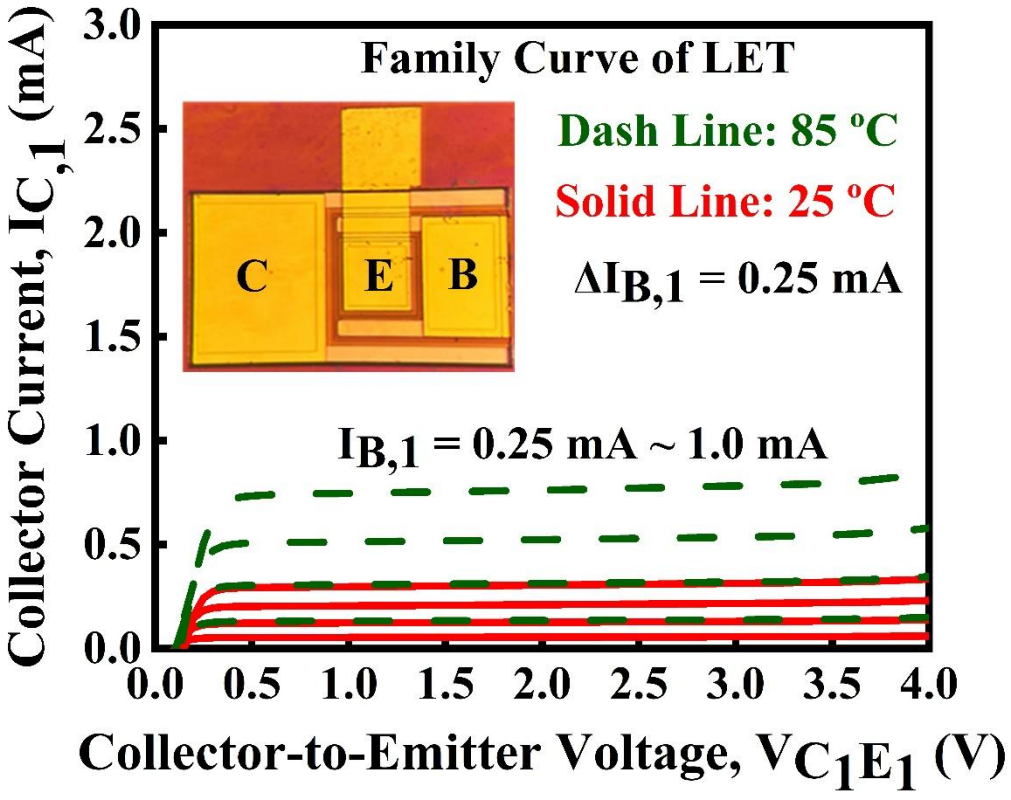


Fig. 4.11: Experimental collector current, $I_{C,1}$ versus collector-to-emitter voltage, $V_{C_1E_1}$ at different base currents, $I_{B,1}$ ranging from 0.25 mA to 1 mA, measured at various substrate temperatures. The inset shows the LET device contacts and applied bias configuration used for the measurements.

doi:10.6342/NTU202500212

Notably, under a base current of 1 mA and a collector-to-emitter voltage of 4 V, the collector current of the LET increased from 0.335 mA to 0.847 mA, while the collector current of the Darlington transistor surged from 0.75 mA to 2.32 mA when the temperature increased from 25℃ to 85℃.

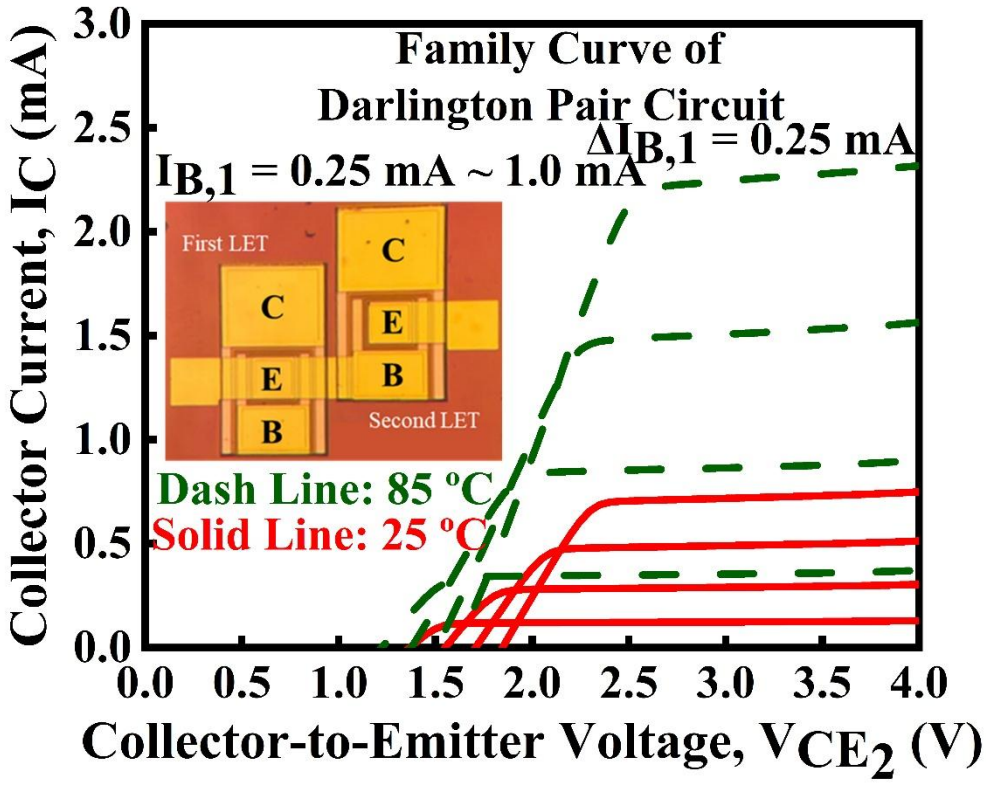


Fig. 4.12: Experimental collector current, I_C versus collector-to-emitter voltage, V_{CE_2} at different base currents, $I_{B,1}$ ranging from 0.25 mA to 1 mA, measured at various substrate temperatures. The inset shows the Darlington transistor device contacts and applied bias configuration used for the measurements. A 500 Ω resistance (R) is used as an external resistance to connect C_2 (collector of second LET) to V_{DD}.

Additionally, the collector-to-emitter offset voltage decreased from 0.15 V to 0.14 V for

doi:10.6342/NTU202500212

the LET and from 1.85 V to 1.65 V for the Darlington transistor as the substrate temperature increased from 25℃ to 85℃. These changes indicate the occurrence of intrinsic carrier surges as the temperature rises. The offset voltage of the Darlington transistor is larger due to the series configuration of two LETs, which results in potentially higher power consumption.

A significant enhancement in current gain, which can be attributed to the increase in both temperature and base current, was observed. The current gain ($\beta_{Darlington}$) of the Darlington transistor as a function of temperature can be expressed as follows:

$$\beta_{Darlington}(T) = \beta_{LET_1}(T) + \beta_{LET_2}(T) + \beta_{LET_1}(T) * \beta_{LET_2}(T) \quad (4.1)$$

Here, $\beta_{LET_1}(T)$ and $\beta_{LET_2}(T)$ represent the current gain of the first and second LETs, respectively, as a function of temperature. As temperature increase, electrons gain sufficient energy to overcome the QW energy barrier, and may escape form the QW, increasing the collector current, I_C and current gain, defined as $\beta=I_C/I_B$ with base-to collector voltage $V_{B_1C} = 0\,\text{V}$. **Fig. 4.13** (solid star symbol) shows the variation of experimental current gains, β_{LET}, as a function of different substrate temperature T_{ext} from 25℃ to 85℃ for LET and **Fig. 4.13** (solid sphere symbol) shows the variation of experimental current gains, $\beta_{Darlington}$, as a function of different substrate temperature T_{ext}

doi:10.6342/NTU202500212

from 25℃ to 85℃ for Darlington transistor. The unique enhancement in current gain is attributed to the increasing temperature T_{ext} and base current I_B. However, it is possible that the current gain increased at a higher base current I_B due to the thermal effect, as the injection of current into the base could heat the device internally.

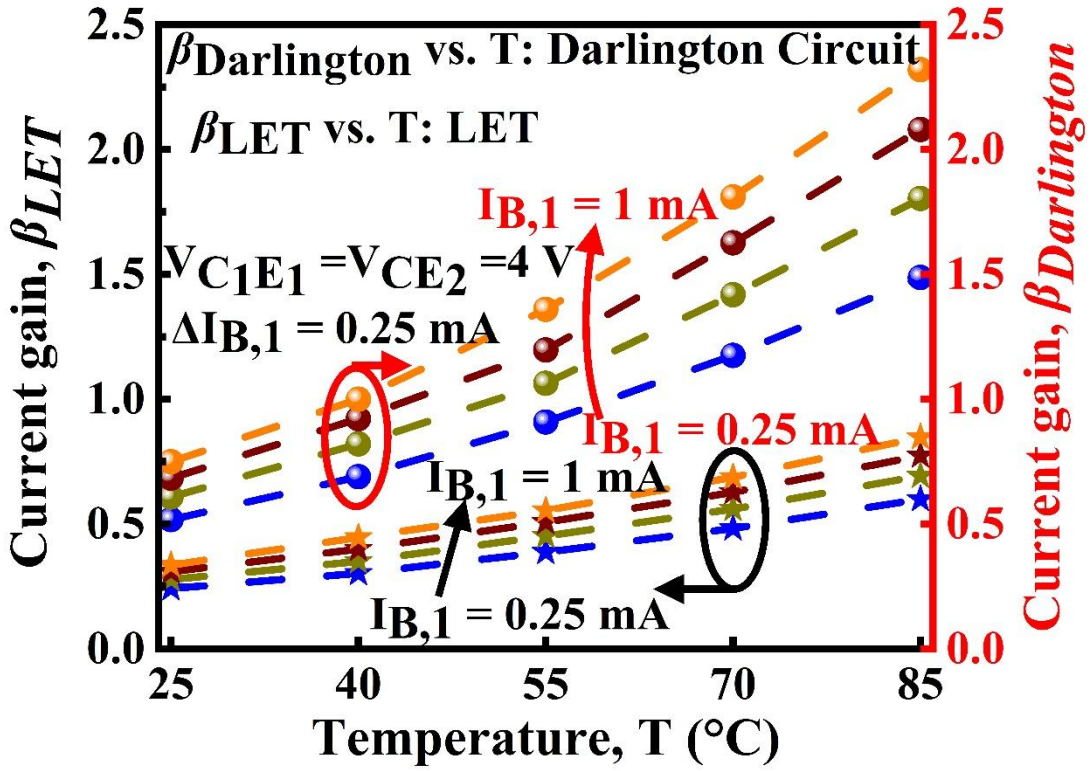


Fig. 4.13: Current gain of the LET (solid star symbols) and Darlington transistor (solid sphere symbols) as a function of substrate temperature, with base current, $I_{B,1}$ ranging from 0.25 mA to 1 mA.

In the tradition HBT, the variation of the base-to-emitter voltage, V_{BE} with the temperature is crucial parameter for designing BJT-based thermal sensors. Typically, as temperature increases, V_{BE} decreases, leading to a decrease in collector current, I_C with

doi:10.6342/NTU202500212

temperature [98]. However, notably observed that in the novel high-speed three-port LET and Darlington transistors based on LETs, $V_{B_1E_1}$ decreased with temperature, yet the collector current increased with the temperature. This unique temperature-dependent behavior is attributed to thermionic emission dominance with increasing temperature compared to change in collector current due to variations in $V_{B_1E_1}$.

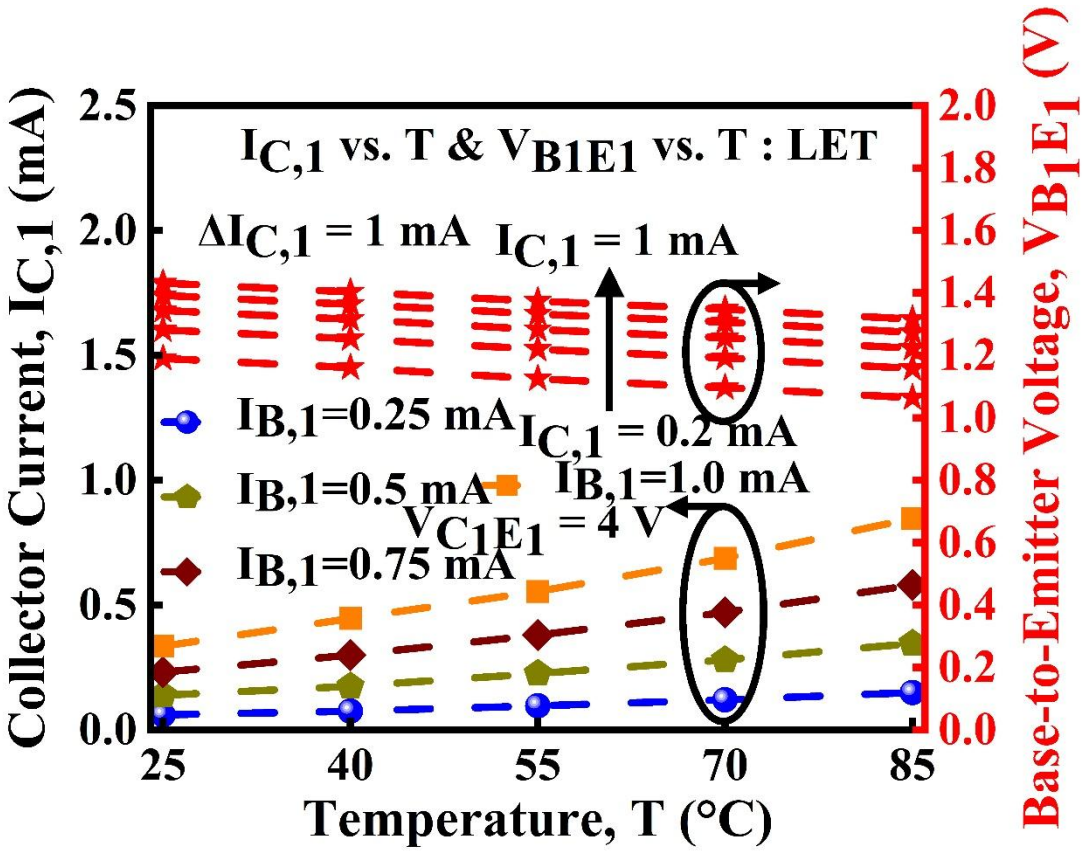


Fig. 4.14: Varication of collector current, $I_{C,1}$ and base-to-emitter voltage, $V_{B_1E_1}$ with substrate temperature for the LET, measured at constant base current, $I_{B,1}$ and constant collector current, $I_{C,1}$, respectively.

Figures 4.14 and 4.15 depict the linear response of $V_{B_1E_1}$ & $V_{B_1E_2}$ to substrate

doi:10.6342/NTU202500212

temperature as a function of $I_{C,1}$ & I_C for LETs and Darlington transistors, respectively. Moreover, these figures illustrate the variation in I_C with substrate temperature (25℃ to 85℃) for both devices. The collector current exhibits an ultra-high sensitivity to temperature, with the sensitivity parameter (defined as the ratio of change in collector current, ΔI_C to the change in temperature, ΔT) provided in **Table 4.2**. These values are tabulated for varying base currents (I_B) across the temperature range for LETs and Darlington transistors.

Table 4.2: Current sensitivity ($\Delta I_C/\Delta T$, μA/℃) for LET and Darlington transistor for different base current I_B

Base Current (I_B)	Transistor Type	Current Sensitivity ($\Delta I_C/\Delta T$)	Unit
0.25 mA	LET	1.49	μA/℃
	Darlington	4.04	μA/℃
0.50 mA	LET	3.45	μA/℃
	Darlington	9.96	μA/℃
0.75 mA	LET	5.81	μA/℃
	Darlington	17.45	μA/℃
1 mA	LET	8.53	μA/℃
	Darlington	26.2	μA/℃

At collector-to-emitter voltage of 4 V and base current of 1 mA, the collector current-to-temperature sensitivity was measured to be 8.53 μA/℃ for LETs and significantly higher at 26.2 μA/℃ for the Darlington transistor. This ultra-high temperature dependence of I_C underscores its potential for the development of next generation of smart thermal sensors based current sensitivity characteristics.

doi:10.6342/NTU202500212

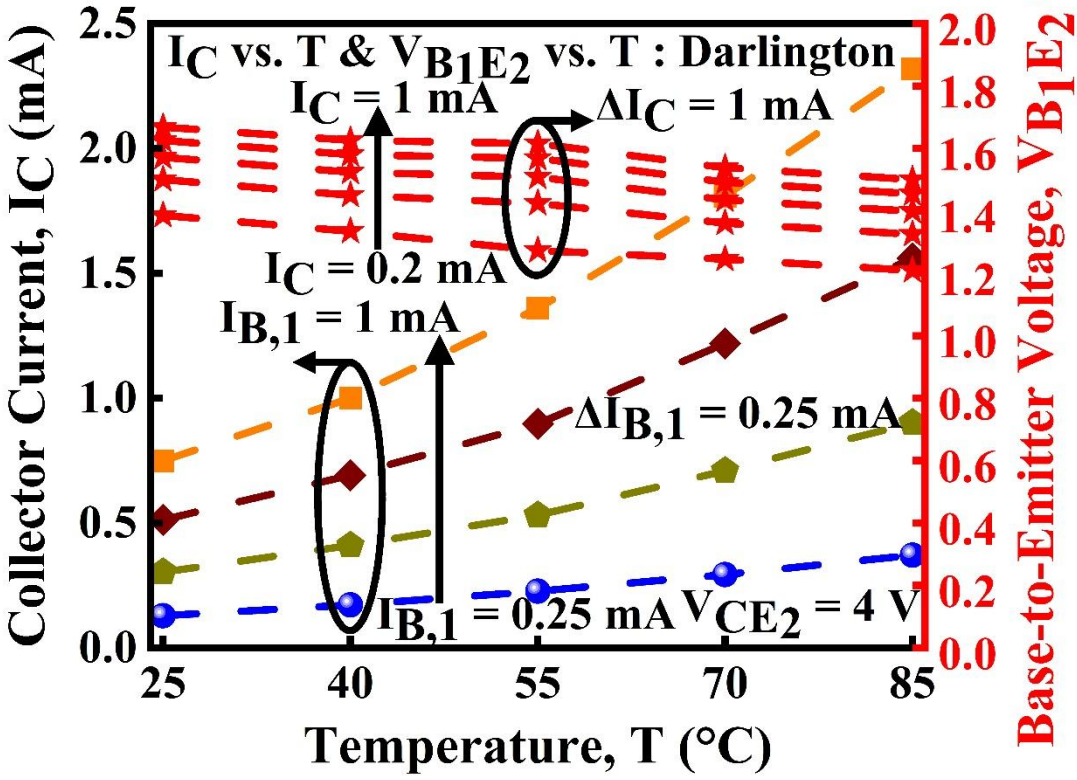


Fig. 4.15: Varication of collector current, I_C and base-to-emitter voltage, $V_{B_1E_2}$ with substrate temperature for the Darlington transistor, measured at constant base current, $I_{B,1}$ and constant collector current, I_C, respectively.

4.6 ADS Modeling of Darlington Transistor: Converting Current Sensitivity to Voltage Sensitivity for Comparison with Existing Technologies

This section outlines the design of a Darlington pair circuit utilizing two LETs. The innovative Darlington transistor is simulated using ADS software, incorporating experimental results from individual LET components. In the ADS model, the emitter of the first LET (LET_1), denoted as E_1, is connected to the base of the second LET (LET_2),

doi:10.6342/NTU202500212

denoted as B_2. The collector of LET_1 (C_1) is directly connected to the supply voltage V_{DD}, while the collector of LET_2 (C_2) is connected to V_{DD} through a 500 Ω external resistance. The ADS model of Darlington transistor is illustrated in **Fig. 4.16**.

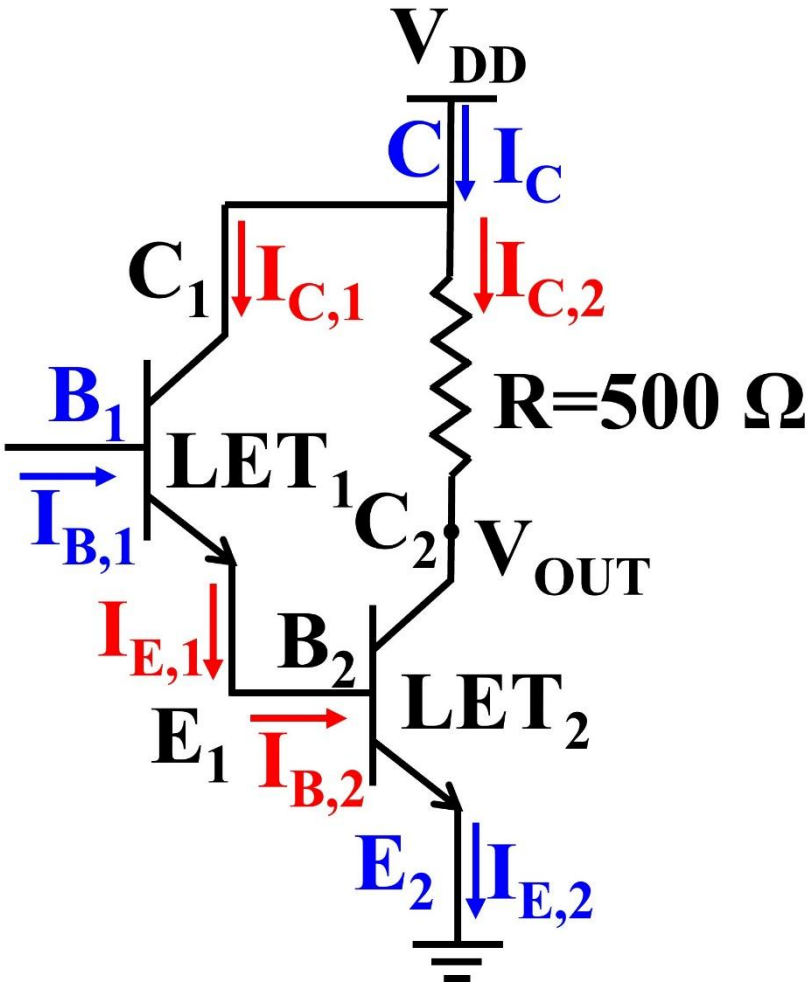


Fig. 4.16: Darlington pair circuit design utilizing two n-p-n LETs (LET_1 and LET_2). B_1 and E_2 represent the base and emitter nodes of Darlington transistor, respectively.

Experimental collector current, I_C of Darlington transistor closely aligns with the simulated collector current obtained from the ADS model, as illustrated in **Fig. 4.17**. The simulation is conducted for varying base current, $I_{B,1}$ ranging from 0.25 mA to 1 mA, with

doi:10.6342/NTU202500212

a step-size of 0.25 mA, across different substrate temperatures ranging from 25°C to 85°C. **Fig. 4.18** shows the collector current of LET_1 ($I_{C,1}$) and LET_2 ($I_{C,2}$) for different $I_{B,1}$ values and substrate temperatures. The overall collector current of Darlington transistor (I_C) is the sum of $I_{C,1}$ and $I_{C,2}$.

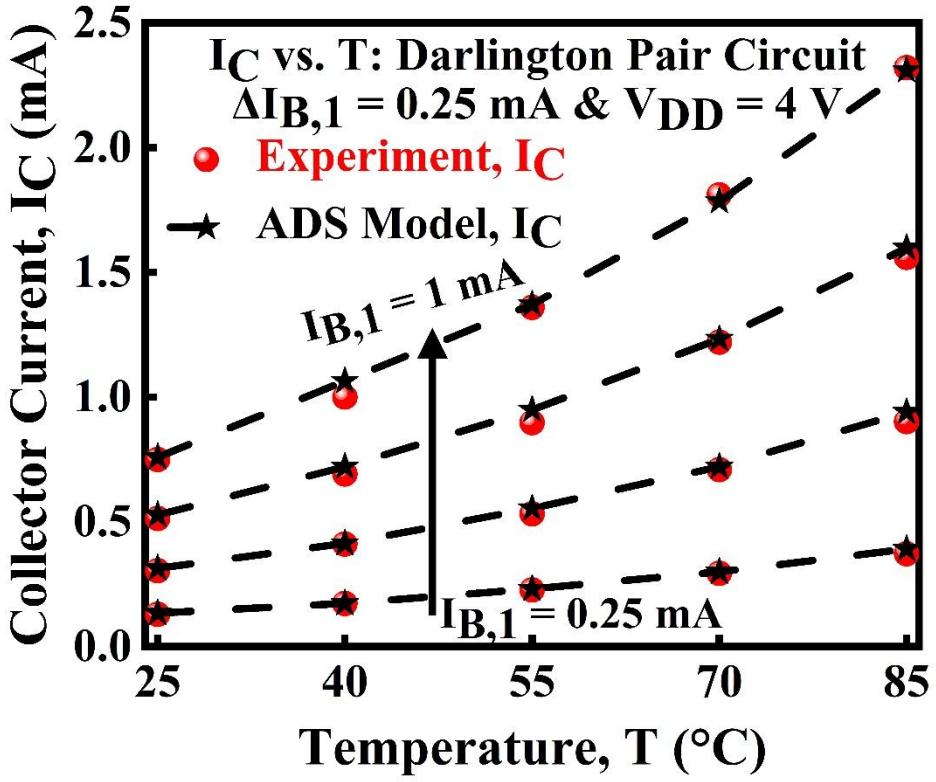


Fig. 4.17: Temperature-dependent collector current, I_C of the Darlington transistor for different base currents, $I_{B,1}$ ranging from 0.25 mA to 1 mA.

In contrast to conventional BJT or PIN diode-based thermal sensors, where the sensitivity is defined as the change in the voltage with respect to change in temperature (voltage-to-temperature signal, $\Delta V/\Delta T$), our approach involves converting the current-to-temperature

doi:10.6342/NTU202500212

signal into a voltage-to-temperature signal using passive components like resistors.

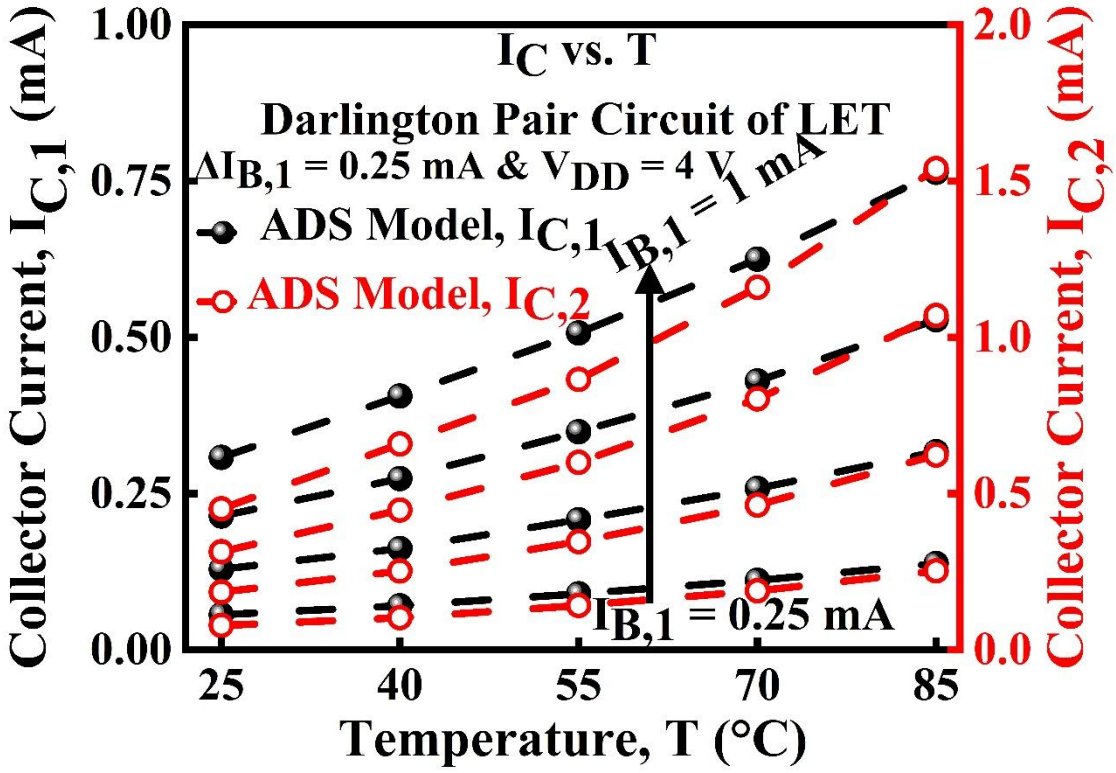


Fig. 4.18: Collector current of individual LETs in the Darlington pair circuit for different base currents at various substate temperatures. (I_C=$I_{C,1}$+$I_{C,2}$).

In this circuit design, a 500 Ω resistor aims to convert the current-to-temperature signal into a voltage-to-temperature signal and this allows for a more meaningful comparison with existing conventional technology [99], [100], [101], [102]. This resistor value was chosen to ensure a measurable output voltage, given the low collector current ($I_{C,2}$) of the second LET. It reflects considerations based on the Darlington transistor and epi-layer design, aligning with desired output voltage requirements for effective comparison. The experimental collector current of the Darlington transistor (I_C) is measured over a

doi:10.6342/NTU202500212

temperature range of 25 ℃ to 85 ℃, considering a fixed external resistance (R=500 Ω). Under these conditions, the output voltage of the Darlington circuit, $V_{out}=V_{DD}-I_{C,2}*R$ is calculated for I_B values ranging from 0.25 mA to 1 mA at different substrate temperature, as depicted in **Fig. 4.19** (black sphere symbol). V_{out} decreases with increasing the base current of Darlington transistor, $I_B=I_{B,1}$ and substate temperature due to the rise in collector current of LET_2, $I_{C,2}$ with increasing $I_{B,1}$ and temperature.

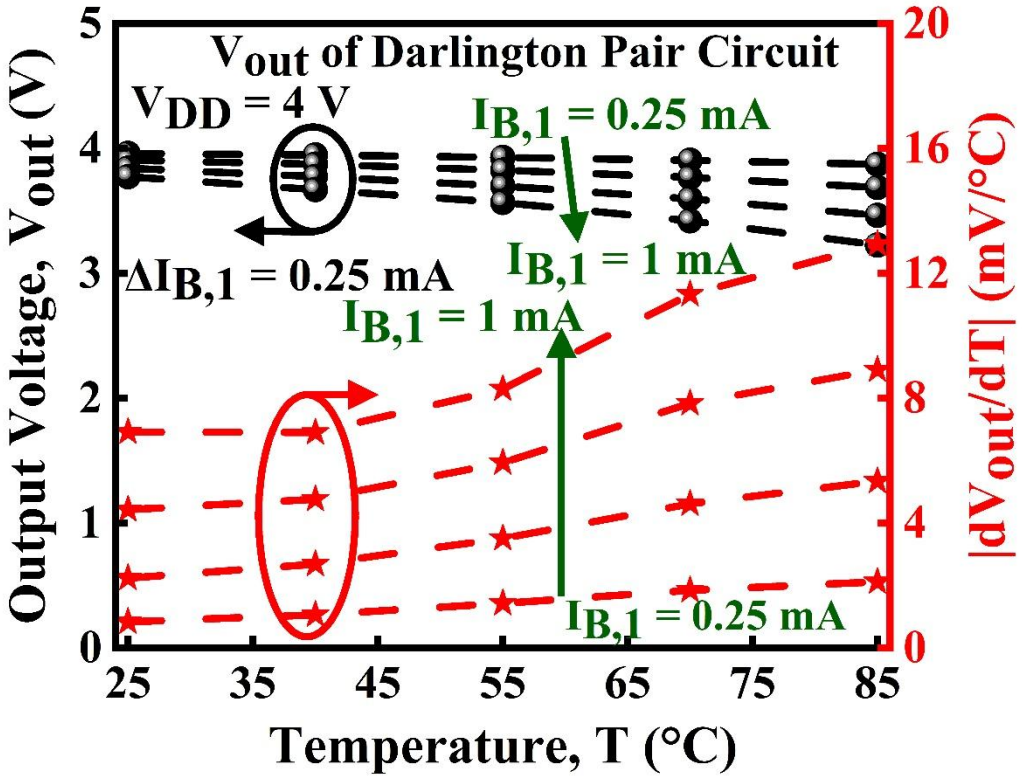


Fig. 4.19: Output voltage of Darlington transistor, V_{out} and derivative of output voltage with respect to temperature as a function of temperature at different base currents.

The absolute value of the derivative of V_{out} with respect to temperature, $|dv_{out}/dt|$, is a

doi:10.6342/NTU202500212

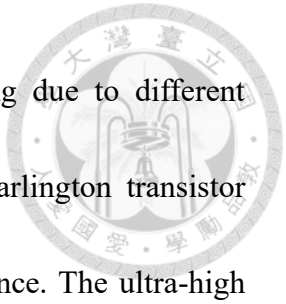
function of substrate temperature and is illustrated in **Fig. 4.19** (red star symbol). This indicates that the output voltage of the Darlington transistor is highly temperature-dependent, with a term expected to be linear for thermal sensor design, although a slight deviation may occur due to non-linear electron escape from the quantum well within this temperature range or necessitate more precise measurements at higher temperature.

Table 4.3: Thermal sensitivity of Darlington transistor comparison with other technology

Thermal Sensor Technology	Temperate Range	Thermal Sensitivity	Ref.
Thermistor	-40 to 85 ℃	1.04 mV/℃	[99]
Diode	16 to 60 ℃	2.1 mV/K	[100]
BJT	-55 to 125 ℃	3 mV/℃	[101]
BJT	-40 to 125 ℃	230 μV/℃	[102]
BJT	-40 to 85 ℃	180 μV/℃	[99]
MOS	-20 to 80 ℃	120 μV/℃	[103]
LET-Based Darlington Transistor	25 to 85 ℃	9.12 mV/℃	This work

The voltage-to-temperature signal (voltage sensitivity, defined as $\Delta V_{out}/\Delta T$) of the Darlington transistor is calculated as 1.46, 3.65, 6.30, and 9.12 mV/℃ for I_B values 0.25, 0.50, 0.75, and 1 mA, respectively, as the temperature increases from 25 ℃ to 85℃. **Table 4.2** presents the thermal sensitivity of this fabricated device with reported conventional technologies, showing the significantly higher signal output of the Darlington transistor.

doi:10.6342/NTU202500212



Although direct comparison with traditional sensors is challenging due to different operational principles, the superior signal characteristics of the Darlington transistor underscore its potential for enhanced temperature-sensing performance. The ultra-high thermal sensitivity of this novel device demonstrates that LET-based Darlington transistors show strong promise as front-end components for high-resolution, smart thermal sensors.

4.7 Conclusion

This chapter presented the design and development of a novel Darlington transistor employing LETs for advanced smart high-temperature sensing applications. The study introduced the groundbreaking concept of leveraging thermionic emission within QWs to enhance temperature sensing capabilities, marking a significant innovation in this domain. At elevated temperatures, the increased thermionic emission within the QW led to notable enhancements in both collector current and current gain. Under bias conditions of collector-to emitter voltage of 4 V and base current of 1 mA, the LET demonstrated a 153% increase in collector current as the operating temperature increased from 25℃ to 85℃. The Darlington transistor, leveraging its unique configuration, achieved an even more pronounced improvement, with a 210% increase in collector current under same bias and temperature conditions.

To further enhance thermal sensitivity, a Darlington pair configuration was designed by

doi:10.6342/NTU202500212

interconnecting two LETs. Under bias conditions of collector-to-emitter voltage of 4 V and base current of 1 mA, the individual LETs exhibited a collector current-to-temperature signal ratio of 8.53 μA/℃. Remarkably, this ratio escalated to 26.2 μA/℃ in the Darlington configuration, demonstrating a significant improvement in thermal sensitivity. Moreover, the voltage-to-temperature signal of the output voltage reached 9.12 mV/℃ at I_B of 1 mA and V_{DD} of 4 V, surpassing conventional thermal sensors.

Despite these achievements, achieving a highly linear voltage-to-temperature response remains a challenge. Further optimization of the quantum well structure is essential to improve linearity, thermal sensitivity, and temperature-dependent current gain. This includes refining parameters such as barrier height, well thickness, and the number and geometry of the QWs to reduce the thermionic emission lifetime within the QW.

The observed positive relationship between temperature and current gain underscores the potential of the Darlington transistor as a excellent candidate for designing front-end smart temperature sensors. These findings not only demonstrate the remarkable thermal performance of the Darlington transistor but also highlight its advantages over conventional bipolar-based temperature sensors.

doi:10.6342/NTU202500212

In summary, this work establishes the Darlington transistor, leveraging LETs, as a promising candidate for next-generation thermal sensing applications. It provides a groundwork foundation for future advancements in OEICs and smart thermal sensor technologies, setting a new benchmark for performance and innovation in this field.

doi:10.6342/NTU202500212

Chapter 5

Thermal Sensitivity and Linearity Analysis of Quantum Well HBTs

5.1 Introduction

This chapter presents an in-depth study of the thermal sensitivity and linearity of QW-based HBTs, a critical area for advancing next-generation thermal sensing technologies. The investigation emphasizes the influence of QW parameters such as QW width and temperature variations on the electrical performance of QW-HBTs, laying the groundwork for their application in high-precision smart temperature sensors for OEICs. By systematically analyzing the thermal behavior of QW-HBTs, this chapter contributes to the development of devices with optimized sensitivity, linearity, and temperature-dependent performance.

The chapter begins with Subchapter 5.2, “Motivation Behind Thermal Sensitivity and Linearity Study for QW-Based HBTs,” which highlights the significance of achieving an optimal balance between thermal sensitivity and linearity. This Subchapter explores the need for advanced device designs to overcome the limitations of existing temperature sensing technologies based on QW-based HBT, particularly in terms of thermal sensitivity in varying temperature application range.

doi:10.6342/NTU202500212

Building upon this motivation, Subchapter 5.3, “Device Design, Fabrication, and Characterization at Different Substrate Temperatures” provides a detailed overview of the design and fabrication processes for QW-HBTs. This section elaborates on the material selection, layer structures, and experimental characterization performed under varying substrate temperatures, enabling a comprehensive understanding of their thermal behavior.

To enhance the theoretical understanding of QW-HBT performance, Subchapter 5.4, “Thermionic Modified Charge-Control Model” introduces a temperature-dependent charge-control model. This model elucidates the impact of thermionic emission on carrier transport, charge storage, and current gain, offering a robust framework for interpreting temperature-induced changes in QW-HBTs.

Subsequently, Subchapter 5.5, “Effect of QW Width on Escape Time, Charge Storage, and Temperature-Dependent Current Characteristics” investigates the role of QW width in shaping the thermal sensitivity and linearity of QW-HBTs. By analyzing the interplay between QW dimensions, carrier dynamics, and temperature effects, this section identifies the design parameters necessary to achieve high-performance thermal sensors. Finally, the chapter conclude with Subchapter 5.6, “Conclusion,” summarizing the findings of the study and identifying the optimal QW-HBT design parameters. The

doi:10.6342/NTU202500212

conclusion emphasizes the critical balance thermal sensitivity and linearity and underscores the importance of these findings for developing advanced smart thermal sensors integrated into OEICs.

The findings of this research have been published in the prestigious journal *IEEE Transactions on Electron Devices* as:

Mukul Kumar et al., "Investigation of thermal sensitivity and linearity of quantum well-based heterojunction bipolar transistor," *IEEE Transactions on Electron Devices*, vol. 72, no.1, pp. 111-118, Jan. 2025, doi: 10.1109/TED.2024.3492153.

This chapter provides a comprehensive exploration of QW-HBTs' electrical thermal properties, offering critical insights into their design and development for advanced temperature sensing applications in OEICs. These findings establish a strong foundation for future research in high-precision smart thermal sensing technology.

5.2 Motivation Behind Thermal Sensitivity and Linearity Study for QW-Based HBTs

In the preceding chapters, significant advancements in the development of thermally sensitive QW-HBTs have been demonstrated. Chapter 3 highlighted that the current gain of TQW-HBTs exhibits a temperature-dependent increase, predominantly

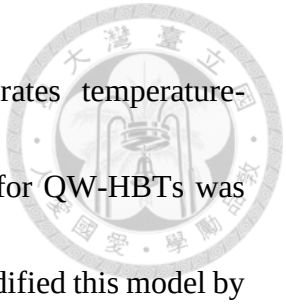
doi:10.6342/NTU202500212

driven by thermionic electron emission from the QWs. This phenomenon enhances the collector current's sensitivity to temperature, achieving a current sensitivity ($\Delta I_C/\Delta T$) of 7 μA/℃ in TQW-HBTs. Building upon this foundation, Chapter 4 introduced a novel Darlington transistor design by cascading two QW-HBTs, further elevating current sensitivity to 26.2 μA/℃. This design also reported a voltage-to-temperature sensitivity ($\Delta V_{out}/\Delta T$) of 9.12 mV/℃, outperforming conventional technologies such as thermistors [99], diodes [100], BJTs [99], [101], [102], MOS devices [103], and FET [104]-based temperature sensors.

Despite these advancements, direct comparisons with traditional sensors remain challenging due to differing operational principles and design parameters. The non-linear electron escape from QWs, which influences the temperature-to-voltage signal's linearity and thermal sensitivity, is a critical parameter for designing effective thermal sensors. Therefore, it becomes imperative to optimize QW parameters, including the number, barrier height, thickness, shape, and size, to improve the thermal sensitivity and linearity of QW-HBT devices. The size of the QW plays a dual role in maximizing optical and carrier confinement and optimizing carrier transport times, which directly impact device performance.

Previous studies by Li and Leburton [62] and Wu et al. [105] have highlighted the dependency of quantum well width on carrier capture and recombination times,

doi:10.6342/NTU202500212



emphasizing the need for a charge-control model that incorporates temperature-dependent time parameters. While the initial charge-control model for QW-HBTs was introduced by UIUC in 2007 [56], subsequent developments have modified this model by integrating diffusion, QW capture and escape lifetimes, and two-level rate equations. These models also incorporate QW dynamics, virtual states, and laser rate equations, paving the way for small-signal modulation bandwidth frameworks. Additionally, studies have explored the impact of MQWs [60], [77], [78] on optical bandwidth and nonlinear gain [86] in TLs. However, the current gain equations for QW-HBTs and TLs differ significantly due to their distinct structures and functional requirements, as detailed in Subchapters 2.5 and 3.3.

Building on these insights, this dissertation proposes a modified temperature-dependent charge-control model for single, multiple, and triple QW-HBTs, discussed in Chapters 2.6, 3.4, and 3.8. This model has been validated through experimental results reported in prior works. The current study extends this approach, modifying the charge-control model to predict the observed trends in temperature-dependent current gain. As temperature increases, carriers within the QWs gain sufficient energy to escape, diffusing to the collector and enhancing current gain. The unique and nearly linear characteristics of the QW-HBT's temperature-dependent current gain form the basis for optimizing the device's layer structure using the modified charge-control model. This chapter investigates the

doi:10.6342/NTU202500212

effects of varying QW sizes on thermal sensitivity and linearity, aiming to enhance the collector current and current gain's temperature responsiveness. Detailed discussions on epi-layer design, optimization, fabrication, characterization at different temperatures, and experimental validations using the modified charge-control model are presented in the following Subchapters.

This work significantly contributes to the advancement of QW-HBTs for temperature sensing applications, particularly in developing high-performance sensors for OEICs. It highlights the potential of QW-HBTs in next-generation thermal sensor technologies, offering a comprehensive framework for their optimization and application.

5.3 Device Design, Fabrication, and Characterization at Different Substrate Temperatures

The epitaxial structure of the QW-HBT used in this study is depicted in **Fig. 5.1**. The epitaxial layers were grown using MOCVD on a semi-insulating (S.I.) GaAs substrate, following a meticulously engineered sequence to optimize device performance. The structure begins with an n-type doped GaAs buffer layer to minimize lattice mismatch with the substrate. This is followed by a bottom cladding layer, comprising a 634-Å thick $Al_{0.4}Ga_{0.6}As$ layer, a 5000-Å thick $Al_{0.90}Ga_{0.10}As$ layer, and a 150-Å thick $Al_{0.4}Ga_{0.6}As$ layer. This cladding layer functions as a DBR, aiding the vertical escape of recombination radiation. Next, a heavily doped n-type GaAs sub-collector layer, 200-Å thick, is

doi:10.6342/NTU202500212

incorporated to enable collector ohmic contact, followed by a 120-Å thick $In_{0.49}Ga_{0.51}P$ layer serving as an etch stop. The collector region is finalized with a 600-Å thick intrinsic GaAs layer.

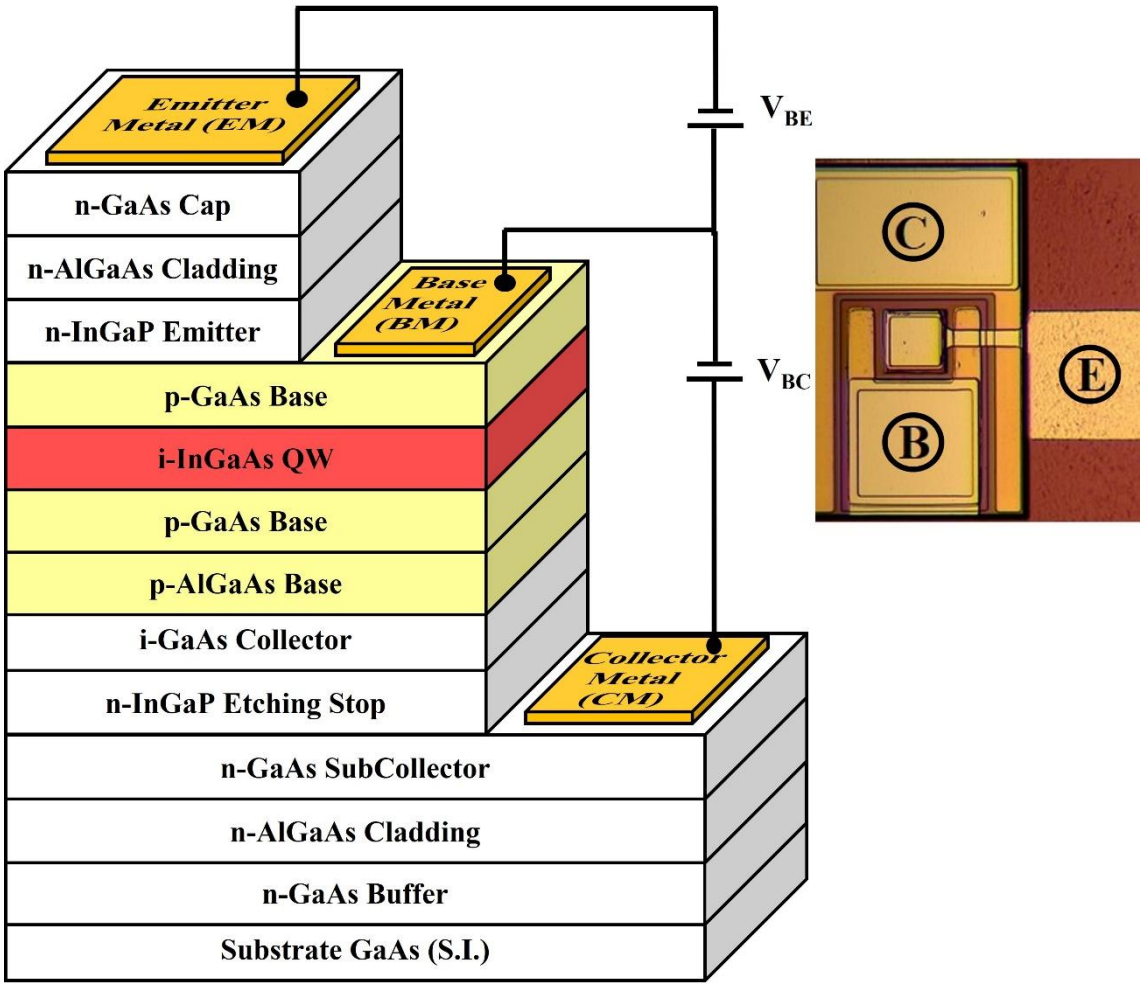


Fig. 5.1: Schematic representation of the epitaxial structure of the n-p-n QW-HBT. The emitter area is 40 μm x 40 μm. The inset provides the top view of the QW-HBT device.

The base region incorporates a meticulously designed structure, starting with a 100-Å thick, heavily p-doped $Al_{0.05}Ga_{0.95}As$ layer, followed by an 880-Å thick, heavily p-doped (~10^{19} cm^{-3}) GaAs base. Embedded within this base is an undoped 120-Å thick $In_{0.2}Ga_{0.8}As$ quantum well, sandwiched by 10-Å thin, undoped GaAs buffer layers.

doi:10.6342/NTU202500212

The emitter region features a 250-Å thick n-type $In_{0.49}Ga_{0.51}P$ layer with a wide bandgap, followed by a sequence of layers: a 150-Å thick n-type $Al_{0.35}Ga_{0.65}As$ layer, a 150-Å thick n-type $Al_{0.8}Ga_{0.2}As$ layer, a 4000-Å thick n-type $Al_{0.98}Ga_{0.02}As$ layer, a 300-Å thick n-type $Al_{0.8}Ga_{0.2}As$ layer, and a 500-Å thick $Al_{0.35}Ga_{0.65}As$ layer. The structure is capped with a 1000-Å thick, heavily doped n-type GaAs layer to provide emitter ohmic contact. The fabrication process begins with wet etching to form the emitter and base mesas. Isolation etching is performed until the semi-insulating (S.I.) GaAs substrate is reached. Contacts for the emitter (E), base (B), and collector (C) are deposited using standard lithography and metallization techniques. The process concludes with planarization, via hole etching, and pad metallization. The detailed fabrication steps are consistent with those outlined in Subchapter 2.3. The final fabricated device, including its top view, is shown in the inset of **Fig. 5.1**.

For characterization, the QW-HBT was placed on a Peltier temperature-controlled stage. Approximately 20 minutes were required for the stage to reach a stable temperature, ensuring accurate and reliable measurements. Electrical DC bias and current were applied using an Agilent E5270B instrument. The current gain, defined as $\beta=I_C/I_B$, was measured under a collector-to-emitter voltage, V_{CE} of 2 V at various temperatures. The base current, I_B was varied from 1 mA to 5 mA in increments of 0.4 mA, and the results are shown in **Fig. 5.2.**

doi:10.6342/NTU202500212

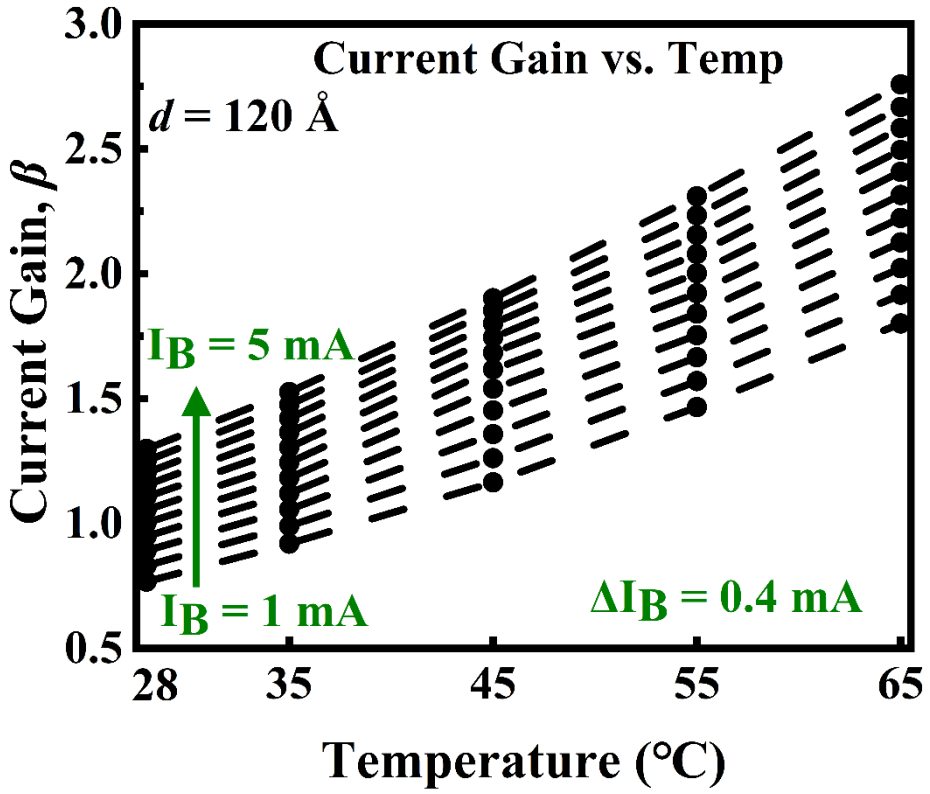


Fig. 5.2: Experimental current gain, β of QW-HBT as a function of substrate temperature, T for various base current, I_B ranging from 1 mA to 5 mA. The quantum-well width, *d* in the fabricated device is 120 Å.

The unique enhancement of the current gain in the QW-HBT at elevated temperatures can be understood through the energy band diagram of the fabricated device, as shown in **Fig. 5.3**. During electron transport from the emitter to the collector, a portion of the electrons is captured by the QW incorporated in the transistor's base region. At higher temperatures, the energy trapped within the QW increases. When electrons gain sufficient energy to overcome the QW barrier, they escape the QW and reach the collector terminal. Due to the high electric field at the B-C junction, these electrons are swept into the

doi:10.6342/NTU202500212

collector, contributing to the collector current. This phenomenon results in an increase in the current gain, β of the device, making it suitable for high-temperature applications.

5.4 Thermionic Modified Charge-Control Model

In this section, the temperature-dependent current gain $\beta(T)$ of the QW-HBT is analyzed using an analytical framework that incorporates various time constant governing carrier dynamics. The modified charge-control model for electron concentration distribution in the base region of the QW-HBT is illustrated in **Fig. 5.3.** The total base minority carrier concentration comprises three components: Q_1, Q_2, and Q_{QW}.

Component Q_1: Represents electrons in region (I) that diffuse through the base, interact with the QW. These carriers may be captured by the QW or escape back into the base.

Component Q_2: Denotes electrons in region (II) that directly diffuse towards the collector, contributing with the collector current.

Component Q_{QW}: Corresponds to the bound electrons stored within the QW, which can recombine with holes present in the QW.

For region I, the rate of change of carrier concentration is described by the following coupled rate equation in the frequency domain:

$$-i\omega\widetilde{Q}_1 = \tilde{F}_{n,1}(I) - \frac{\widetilde{Q}_1}{\tau_b} - \frac{\widetilde{Q}_1}{\tau_{t,EQW}} \tag{5.1}$$

where $F_{n,1}(I)$ represents the carrier flux injected from emitter into region I, τ_b is the minority carrier recombination lifetime in the base bulk, and $\tau_{t,EQW}$ is the transit time from

doi:10.6342/NTU202500212

emitter to the QW.

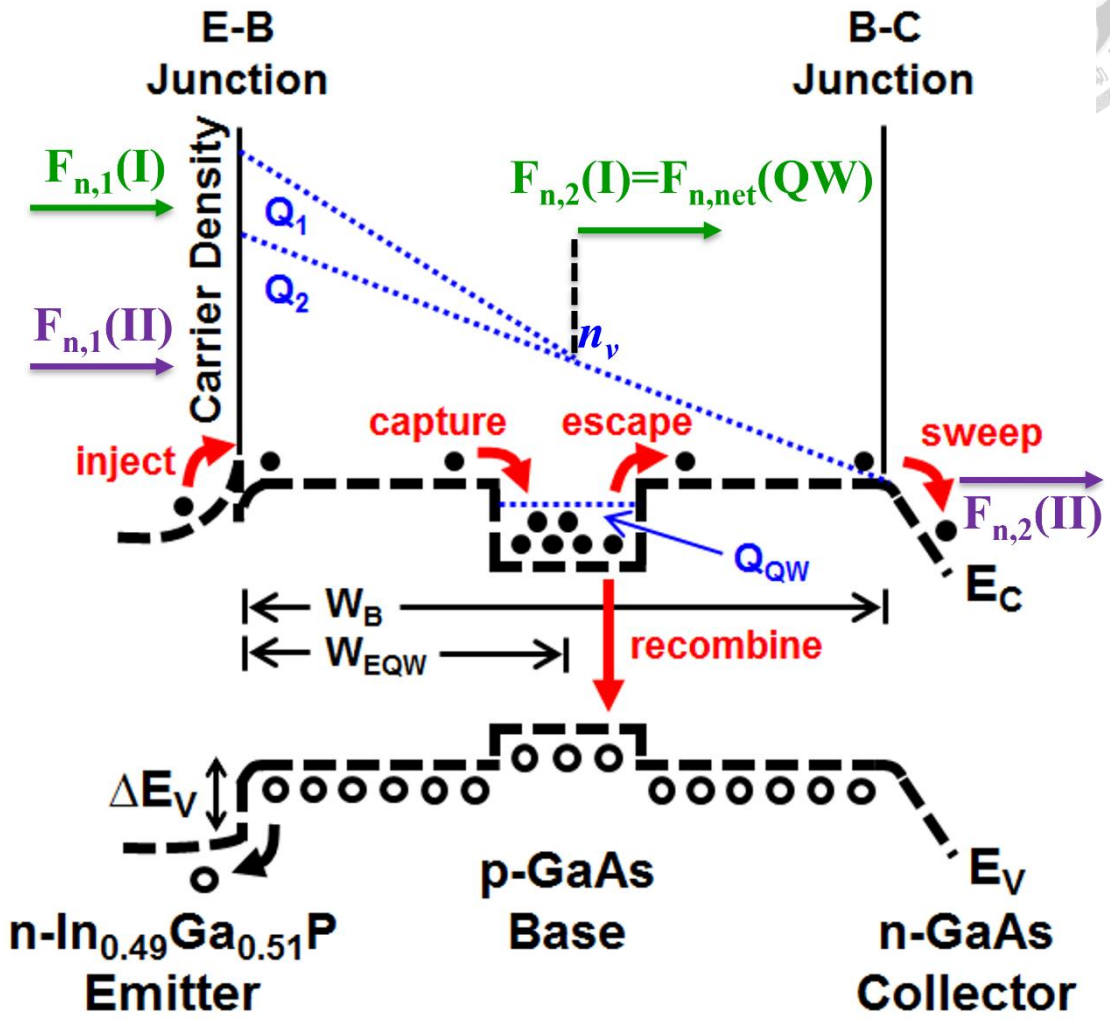


Fig. 5.3: Schematic energy band diagram and the electron distribution concentration of the QW-HBT.

For region (II), the coupled rate equation is expressed as

$$-i\omega\tilde{Q}_2 = \tilde{F}_{n,1}(II) - \frac{\tilde{Q}_2}{\tau_b} - \frac{\tilde{Q}_2}{\tau_{t,EC}} \tag{5.2}$$

where $F_{n,1}(II)$ denotes the electron flux injected from the emitter to region II, and $\tau_{t,EC}$ is the transit time from emitter to collector.

doi:10.6342/NTU202500212

Within the QW region, the coupled rate equation is:

$$-\mathrm{i}\omega\widetilde{\mathrm{Q}}_{\mathrm{QW}} = \frac{\tilde{n}_{\mathrm{v}}d}{\tau_{\mathrm{cap}}} - \frac{\widetilde{\mathrm{Q}}_{\mathrm{QW}}}{\tau_{\mathrm{QW}}} - \frac{\widetilde{\mathrm{Q}}_{\mathrm{QW}}}{\tau_{\mathrm{esc}}} \tag{5.3}$$

where τ_{QW} denotes the recombination lifetime in the QW, τ_{cap} represents capture time from the virtual state to the QW, τ_{esc} represents escape time from the QW to the base, d represents width of the QW, and n_v represent the current density (cm^{-3}) in the virtual state. To balance carrier conservation principles, a dynamic equilibrium is established between region (I) and the QW. This equilibrium facilitates the derivation of a relationship the carrier density in the QW, expressed as $n_{QW} = Q_{QW}/d$, and the carrier density in the virtual state, n_v as presented in Eq. (5.3). This relationship can be represented as follows:

$$\tilde{n}_{QW} = \frac{\frac{1}{\tau_{cap}}}{-\mathrm{i}\omega + \frac{1}{\tau_{QW}} + \frac{1}{\tau_{esc}}}\tilde{n}_{\mathrm{v}} \tag{5.4}$$

The total carrier flow $F_{n,2}(I)$, representing the carriers leaving region (I) and being captured by the QW, is balanced with $F_{n,net}(QW)$, which denotes the total carrier flow captured by the QW and subsequently escaping it. To drive this relationship, n_{QW} is substituted with n_v, establishing a relationship between $F_{n,1}(I)$ and $F_{n,2}(I)$, Here, W_{EQW} represents the distance between the emitter to the QW. The carrier equilibrium between region (I) and the QW can be expressed as:

doi:10.6342/NTU202500212

$$\tilde{F}_{n,2}(I) = \tilde{F}_{n,net}(QW) = d\left(\frac{\tilde{n}_v}{\tau_{cap}} - \frac{\tilde{n}_{QW}}{\tau_{esc}}\right) = \frac{d\tilde{n}_v}{\tau_{cap}}\left(\frac{-i\omega + \frac{1}{\tau_{QW}}}{-i\omega + \frac{1}{\tau_{QW}} + \frac{1}{\tau_{esc}}}\right) \quad (5.5)$$

The carrier flow $\tilde{F}_{n,2}(I) = \tilde{F}_{n,1}(I)\,\mathrm{sech}\left(W_{EQW}/\tilde{L}_n\right)$ can be expressed in an alternate form. Using Eq. (5.5), the injected flux $F_{n,1}(I)$ can be rewritten as

$$\tilde{F}_{n,1}(I) = \frac{d}{\tau_{cap}}\left(\frac{-i\omega + \frac{1}{\tau_{QW}}}{-i\omega + \frac{1}{\tau_{QW}} + \frac{1}{\tau_{esc}}}\right)\cosh\left(\frac{W_{EQW}}{\tilde{L}_n}\right)\tilde{n}_v \quad (5.6)$$

The carrier flow $F_{n,2}(II)$ represents the carriers leaving region II, which correspond to those diffusing directly to the collector. This outflow of carriers $F_{n,2}(II)$ from region (II) can be expressed as

$$\tilde{F}_{n,2}(II) = \frac{D_n}{\tilde{L}_n}\frac{1}{\sinh\left(\frac{W_{QWC}}{\tilde{L}_n}\right)}\tilde{n}_v = \frac{1}{\tau_{t,QWC}}\frac{\frac{W_{QWC}}{\tilde{L}_n}}{\sinh\left(\frac{W_{QWC}}{\tilde{L}_n}\right)}\frac{W_{QWC}}{2}\tilde{n}_v \quad (5.7)$$

Using Eq. (5.7) and the relationship $\tilde{F}_{n,2}(II) = \tilde{F}_{n,1}(II)\,\mathrm{sech}\left(W_{EC}/\tilde{L}_n\right)$, the expression of $F_{n,1}(II)$ can be formulated as

$$\tilde{F}_{n,1}(II) = \cosh\left(\frac{W_{EC}}{\tilde{L}_n}\right)\frac{\frac{W_{QWC}}{\tilde{L}_n}}{\sinh\left(\frac{W_{QWC}}{\tilde{L}_n}\right)}\frac{W_{QWC}}{2 * \tau_{t,QWC}}\tilde{n}_v \quad (5.8)$$

Using Eqs. (5.6) and (5.8), the total flux injected by the emitter, $\tilde{F}_{n,1}$, which is the sum of the fluxes in region (i) and (ii), can be expressed as

$$\tilde{F}_{n,1} = \tilde{F}_{n,1}(I) + \tilde{F}_{n,1}(II) \quad (5.9)$$

doi:10.6342/NTU202500212

$$= \frac{d}{\tau_{cap}}\left(\frac{-i\omega + \frac{1}{\tau_{QW}}}{-i\omega + \frac{1}{\tau_{QW}} + \frac{1}{\tau_{esc}}}\right)\cosh\left(\frac{W_{EQW}}{\tilde{L}_n}\right)\tilde{n}_v$$

$$+ \cosh\left(\frac{W_{EC}}{\tilde{L}_n}\right)\frac{1}{\tau_{t,QWC}}\frac{\frac{W_{QWC}}{\tilde{L}_n}}{\sinh\left(\frac{W_{QWC}}{\tilde{L}_n}\right)}\frac{W_{QWC}}{2}\tilde{n}_v$$

Under DC operation conditions $(\omega = 0)$, the current gain (β), defined as $\beta = I_C/I_B$, can be expressed as

$$\beta = \frac{\tilde{F}_{n,2}(II)}{\tilde{F}_{n,1} - \tilde{F}_{n,2}(II)} \tag{5.10}$$

By substituting the relevant term in Eq. (5.10), this can be expanded to

$$\beta = \frac{\frac{W_{QWC}}{\tilde{L}_n}}{\sinh\left(\frac{W_{QWC}}{\tilde{L}_n}\right)}\frac{W_{QWC}}{2\tau_{t,QWC}}\left[\frac{d}{\tau_{cap}}\left(\frac{\frac{1}{\tau_{QW}}}{\frac{1}{\tau_{QW}} + \frac{1}{\tau_{esc}}}\right)\cosh\left(\frac{W_{EQW}}{\tilde{L}_n}\right)\right.$$

$$\left. + \left\{\cosh\left(\frac{W_{EC}}{\tilde{L}_n}\right) - 1\right\}\frac{\frac{W_{QWC}}{\tilde{L}_n}}{\sinh\left(\frac{W_{QWC}}{\tilde{L}_n}\right)}\frac{W_{QWC}}{2\tau_{t,QWC}}\right]^{-1} \tag{5.11}$$

If the diffusion length of electrons L_n significantly exceeds the dimensions of W_B=W_{EC}, W_{EQW}, and W_{QWC}, the current gain (β) can be approximated as

$$\beta = \frac{\frac{W_{QWC}}{2\tau_{t,QWC}}}{\frac{d}{\tau_{cap}}\left(\frac{\frac{1}{\tau_{QW}}}{\frac{1}{\tau_{QW}} + \frac{1}{\tau_{esc}}}\right) + \frac{W_{QWC}}{4\tau_{t,QWC}}\left(\frac{W_{EC}}{\tilde{L}_n}\right)^2} \tag{5.12}$$

To represent β in Eq. (5.12) in terms of more conventional parameters, we define β_β and β_{QWC}, representing the current gains for the EC region without QW and QWC region,

doi:10.6342/NTU202500212

respectively:

$$\beta_\beta = \frac{\tau_b}{\tau_{t,EC}}, \qquad \beta_{QWC} = \frac{\tau_b}{\tau_{t,QWC}} \tag{5.13}$$

Using Eq. (5.4), the ratio of current density (n_{QW}/n_v, in cm^{-3}) in the QW and virtual state can be expressed as

$$\frac{n_{QW}}{n_v} = \frac{\frac{1}{\tau_{cap}}}{\frac{1}{\tau_{QW}} + \frac{1}{\tau_{esc}}} \tag{5.14}$$

With Eq. (5.14) and $Q_{QWC} = n_v W_{QWC}/2$, the surface density ratio between the QW region and the QW-to-collector base bulk region is given as

$$\frac{Q_{QW}}{Q_{QWC}} = \left(\frac{\frac{1}{\tau_{cap}}}{\frac{1}{\tau_{QW}} + \frac{1}{\tau_{esc}}} \right) \frac{2d}{W_{QWC}} \tag{5.15}$$

Finally, substituting Eqs. (5.13), (5.14), and (5.15), the current gain (β) is simplified as

$$\beta = \frac{1}{\frac{1}{\beta_\beta} + \frac{1}{\beta_{QWC}} \frac{Q_{QW}/\tau_{QW}}{Q_{QWC}/\tau_b}} \tag{5.16}$$

This expression for current gain β is critical for analyzing the temperature-dependence characteristics of the QW-HBT. By employing the modified charge-control model, the temperature-dependent carrier concentration in the base segment of each transistor region is independently assessed. **Figure 5.4** illustrated simulated carrier concentrations in the QW's base region, specifically for a width of 120 Å, over a temperature range of 300 K

doi:10.6342/NTU202500212

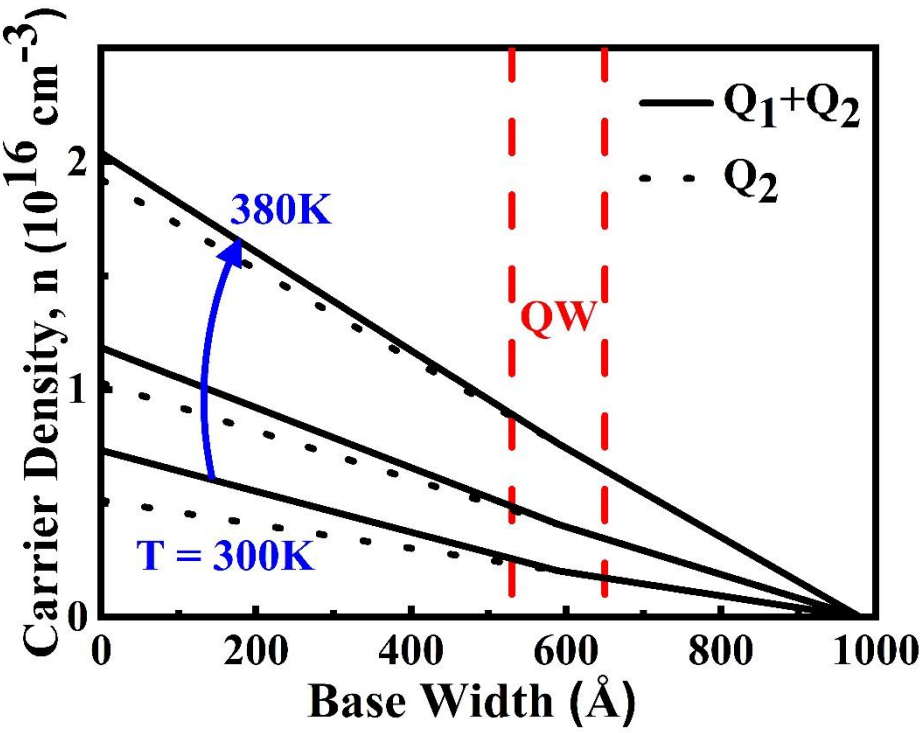


Fig. 5.4: Schematic representation of minority carrier distribution in a QW-HBT with a 120 Å QW width at temperatures of 300 K, 340 K, and 380 K. Regions below the solid line include Q_1 and Q_2, while regions below the dotted line refer to Q_2.

to 380 K. In this figure, regions below the dotted line correspond to Q_2, while regions below the solid line represent Q_1 and Q_2 collectively. As temperature increases, reduced escape time enables electrons in the QW to gain sufficient energy to escape. Consequently, Q_1, representing bound-state carrier density, decreases while Q_2 increases due to carrier escape. This shift results in a decreasing Q_1 to Q_2 ratio and an eventual overlap of solid and dotted lines at higher temperatures.

doi:10.6342/NTU202500212

5.5 Effect of QW Width on Escape Time, Charge Storage, and Temperature-Dependent Current Characteristics

To achieve a high-sensitivity of QW-HBT for temperature sensor applications, we systematically optimized the layer structure of QWs with varying widths. QW-based HBT exhibit high temperature sensitivity due to the dominance of thermionic emission in the QW region. However, the nonlinear escape of electrons from the QW presents challenges in comprehending device physics and improving sensitivity while maintaining acceptable linearity across different temperature ranges.

This study explores the impact of QW width on escape time, employing a modified thermionic theory. Detailed derivations of escape time are presented in Subchapter 2.7, and Eq. (2.27) is utilized for calculating escape time across various QW widths, with a minimum width of 50 Å considered for analysis. **Figure 5.5** depicts the variation of electron escape time with temperature for QW widths of 50 Å, 60 Å, 70 Å, 90 Å, and 120 Å. As temperature increases, carrier density in the base region rises due to the band-filling effect, extending the tail of the carrier distribution beyond the QW. This leads to an exponential decrease in escape time. For example, when the temperature increases from 300 K to 400 K, the escape time decreases by 83.24% for a QW width of 120 Å and 74% for a QW width of 50 Å. This observation suggests that narrower QWs require less energy for carrier escape, reducing sensitivity to temperature-dependent current gain. This

doi:10.6342/NTU202500212

phenomenon arises because escape time exhibits greater temperature dependence compared to other recombination and capture times.

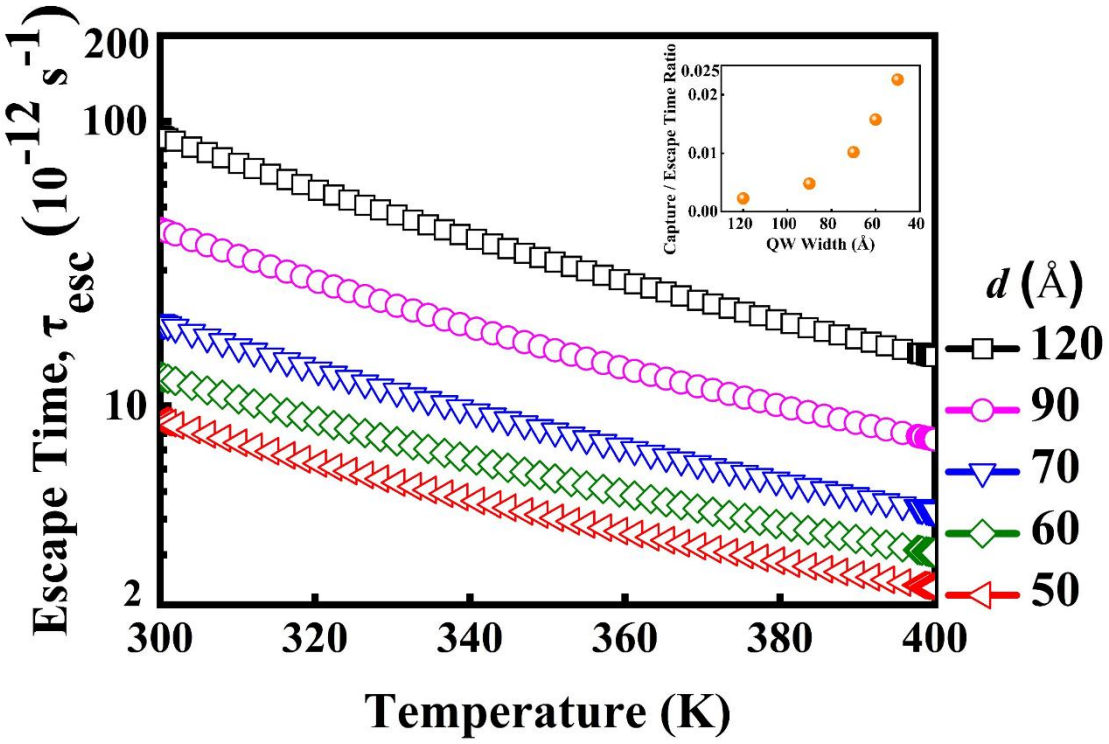


Fig. 5.5: Calculated electron escape time as a function of temperature for varying QW-widths (50 Å, 60 Å, 70 Å, 90 Å, and 120 Å) and the electron capture-to-escape time ratio at 300 K as a function of QW-widths.

The inset of **Fig. 5.5** presents the electron capture-to-escape time ratio at 300 K for different QW widths, revealing that narrower QWs increase this ratio, indicating a higher likelihood of carrier escape rather than to be captured. If the escape time is significantly shorter than the capture time, carriers may escape more easily due to temperature fluctuations, which can impact the device's thermal sensitivity. Additionally, it is observed that when the QW width decreases below 90 Å, this ratio increases sharply,

doi:10.6342/NTU202500212

meaning the escape time becomes less sensitive to temperature. As a result, the device's thermal sensitivity decreases, limiting its performance across a broader temperature range.

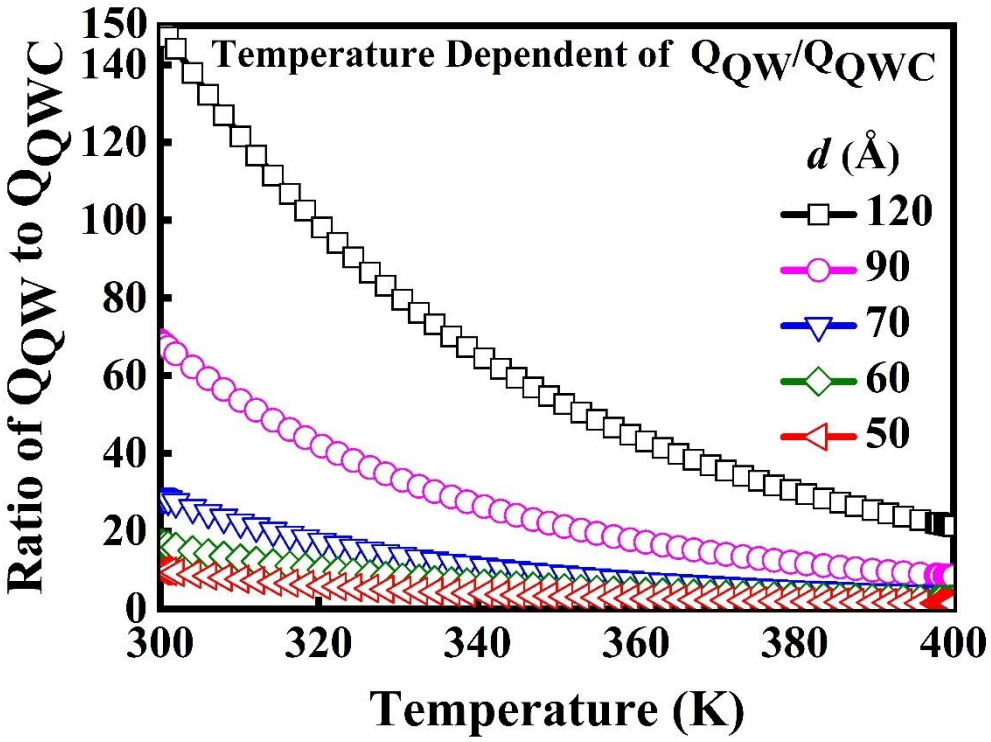


Fig. 5.6: Extracted current density ratio, Q_{QW}/Q_{QWC} as a function of temperature for varying QW widths (50 Å, 60 Å, 70 Å, 90 Å, 120 Å).

The TCAD software is initially used to simulate various QW structures, allowing for the determination of bound-state carrier density values. These values are then integrated into the charge-control model to calculate the virtual state for different QW widths at various temperatures. By substituting the virtual state into Eqs. (5.6) and (5.8), the fluxes $F_{n,1}$(I) and $F_{n,1}$(II) are obtained, respectively. The diffusion equations governing the base region of the QW-HBT are solved, and the rate equation for the QW is applied to derive Eq.

doi:10.6342/NTU202500212

(5.12) for current gain. This equation includes the impact of various carrier lifetimes, with escape time playing a dominant role over capture time and QW recombination time. As the escape time decreases exponentially with rising temperature, the current gain becomes primarily governed by escape time in relation to temperature.

Equation (5.12) expresses the relationship between carrier lifetime and current gain, and is reformulated in a more conventional format for clarity. Specifically, the term Q_{QW}/Q_{QWC} is highly sensitive to temperature. This ratio represents the carrier density between the QW region and the QW-to-collector bulk region. **Figure 5.6** shows this carrier density ratio as a function of temperature for various QW widths. As the temperature increases, the ratio decreases, primarily due to the thermionic effects. With higher temperatures, the escape time decreases exponentially with $1/K_BT$, allowing electrons within the QW to rapidly gain energy and escape, returning to the transistor base. At elevated temperatures, electrons gain even more energy, resulting in faster escapes. These additional electrons contribute to the accumulation of charge in the base, Q_0 and QWC regions, which is then directed toward the collector through the B-C reverse process. Additionally, larger QW widths exhibit a more significant decrease in Q_{QW}/Q_{QWC} compared to smaller QW widths.

doi:10.6342/NTU202500212

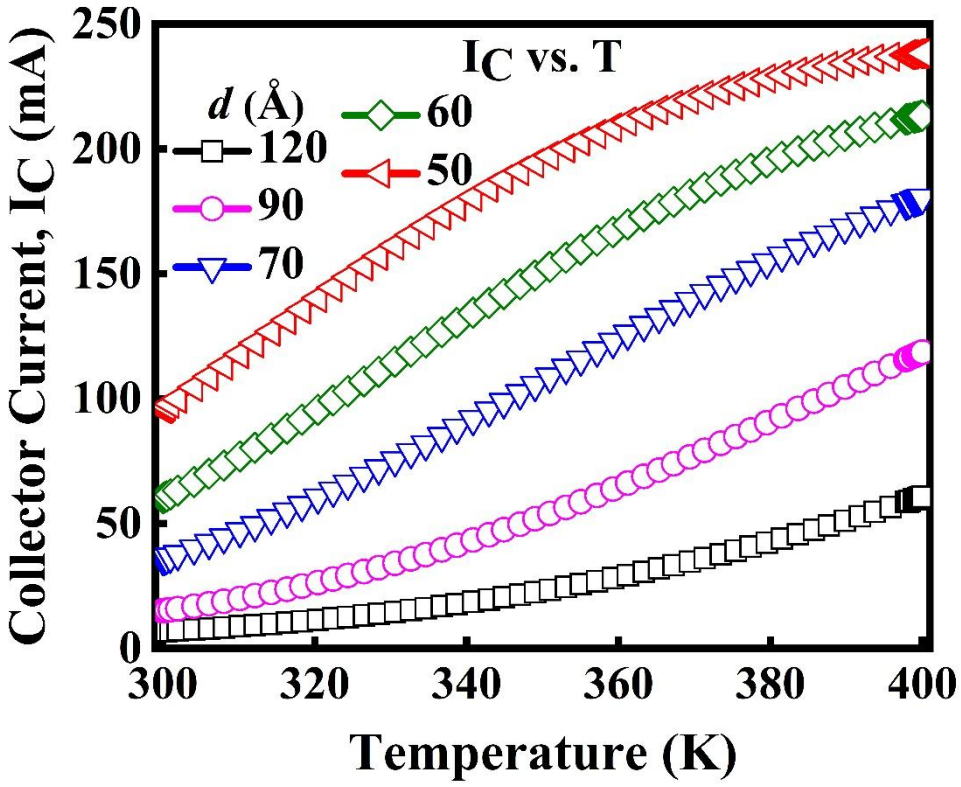


Fig. 5.7: Simulated collector current as a function of temperature for epitaxial designs with varying QW widths (50 Å, 60 Å, 70 Å, 90 Å, 120 Å).

Figures 5.7 and 5.8 shows the collector current and current gain of the QW-HBT as functions of temperature for various QW widths. Notably, the experimental current gain for a QW width, *d*, of 120 Å aligns well with the simulation results for the same width. Conceptually, the QW can be considered an "electron reservoir" that provides electrons for thermionic emission as the temperature increases. As the QW width increases, the number of electrons captured in the QW reservoir also increases, which leads to a decrease in both the collector current and current gain with larger QW widths. Electrons in narrower QWs require less time to escape, resulting in lower rates of change in the

doi:10.6342/NTU202500212

sensitivity of current gain and collector current to temperature changes at higher temperatures. For a QW width of 50 Å, the current gain initially increases with temperature but eventually saturates at higher temperatures. In contrast, narrower QWs deplete quickly due to their smaller electron reservoir capacity.

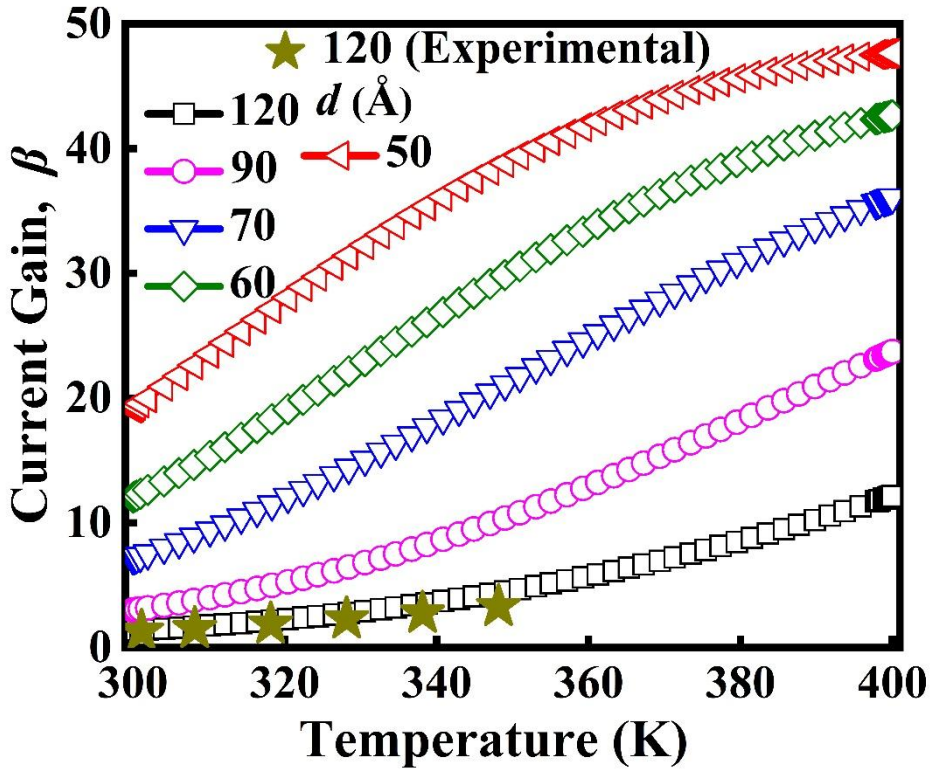


Fig. 5.8: Simulated current gain as a function of temperature for epitaxial designs with varying QW-widths (50 Å, 60 Å, 70 Å, 90 Å, and 120 Å). The gray solid star symbol represents the experimental observed current gain for a QW-width, d, of 120 Å at a base current, I_B of 5 mA and collector-to-emitter voltage, V_{CE} of 2 V.

To predict high thermal sensitivity and good linearity, we systematically varied the QW width within the same base width for simulation purposes. Sensitivity and linearity are

doi:10.6342/NTU202500212

crucial factors for the design of smart thermal sensors, as they determine the temperature range of application and are heavily influenced by design specifications, especially the QW width. The nonlinearity in collector current with respect to temperature results from the nonlinear electron escape from the QW. For the analysis of thermal sensitivity and linearity over the temperature range from 25℃ to 100℃, we plotted δI_C versus temperature T. These curves were then fitted using the Allometric1 Equation as follows:

$$\delta I_C = \mathrm{A} \times \mathrm{T}^{\mathrm{B}} \tag{5.17}$$

Here, A is the thermal sensitivity fitting parameter, which needs a larger value for higher sensitivity, and B is the linearity fitting parameter, which ideally should be closer to 1 for good linearity. **Figure 5.9** shows the derivative of collector current (δI_C, defined as thermal sensitivity in mA/℃) versus temperature for different QW widths. Using Eq. (5.17), the fitting parameters A and B were calculated for each QW width, as shown in **Table 5.1.**

Table 5.1: Parameter setting A and B for different QW-widths

QW-Width (*d*)	**Thermal Sensitivity Fitting Parameter (A)**	**Linearity Fitting Parameter (B)**
120 Å	0.00253	1.22999
90 Å	0.0538	0.67748
70 Å	1.24943	0.01116
60 Å	7.42333	-0.40507
50 Å	38.76601	-0.8237

doi:10.6342/NTU202500212

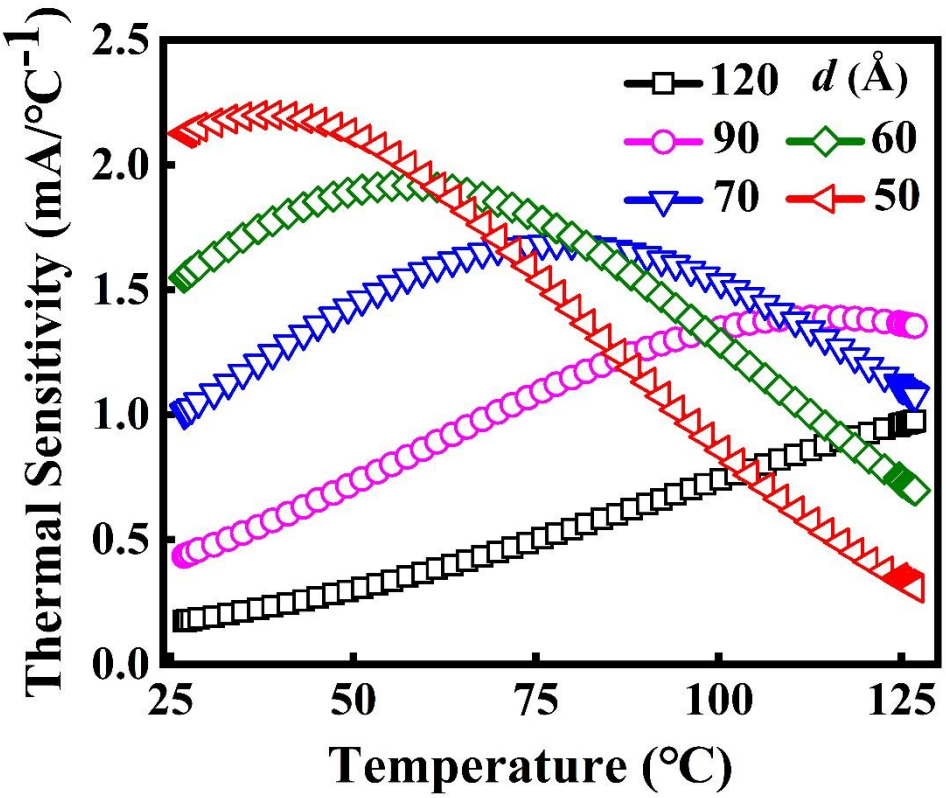


Fig. 5.9: Collector current derivation as a function of temperature for varying QW-widths (50 Å, 60 Å, 70 Å, 90 Å, and 120 Å).

For this specific epi-layer design of QW-HBT, the 50 Å QW width exhibits high sensitivity to temperature primarily within the near-room temperature range. However, the 90 Å QW width demonstrates optimal performance in terms of both thermal sensitivity and linearity within the 25℃ to 100℃ temperature range. At 100℃, the thermal sensitivity of the QW-HBT with a QW width of 90 Å is 1.34 mA/℃, with the fitting linearity parameter B equal to 0.67748. This outstanding result indicates that the QW-HBT is a promising device suitable for applications in smart thermal sensor

doi:10.6342/NTU202500212

technology.

5.6 Conclusion

This chapter presents a comprehensive analysis of the effects of temperature and QW width variations on the electrical performance of QW-HBTs. Through a combination of simulations and experimental investigations, the intricate relationships among temperature, QW width, current gain, thermal sensitivity, and linearity have been systematically explored. Utilizing a modified temperature-dependent charge-control model, the study reveals a significant increase in the current gain of QW-HBTs with rising temperatures, primarily due to enhanced thermionic emission from the QW. As temperature rises, carriers stored in the QW acquire sufficient energy to escape, resulting in a decrease in escape time and the carrier ratio Q_1/Q_2, which, in turn, leads to an increase in current gain.

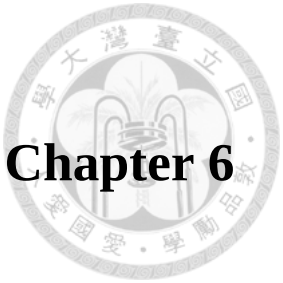
However, narrower QWs exhibit limitations at elevated temperatures, as they cannot supply sufficient carriers, leading to saturation in current gain. Additionally, the study underscores the critical role of QW width in determining the thermal sensitivity and linearity of QW-HBTs with respect to temperature variations. Narrower QWs exhibit higher thermal sensitivity due to shorter carrier escape times, while wider QWs ensure improved linearity over a broader temperature range.

The findings indicate that a QW width of 90 Å achieves an optimal balance between

doi:10.6342/NTU202500212

thermal sensitivity and linearity, particularly within the temperature range of 25℃ to 100℃. At 100℃, a QW width of 90 Å demonstrates a thermal sensitivity of 1.34 mA/℃ and a linearity fitting parameter B of 0.67748. These results identify a best design approach for high-performance temperature sensors, facilitating their integration into OEICs. This study provides valuable insights for advancing temperature sensing technologies, paving the way for next-generation applications in smart thermal sensor systems.

doi:10.6342/NTU202500212



Chapter 6

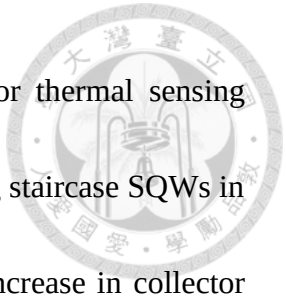
Conclusion

6.1 Summary and Key Contributions of the Thesis

This thesis presents a comprehensive study on the design, development, and optimization of LETs for advanced smart thermal sensing technology. The research explores the evolution of semiconductor devices, from traditional transistors to III-V compound semiconductor based LETs, highlighting their significant potential in high-performance thermal sensing applications. The key findings and innovations from each chapter are summarized below.

The first chapter sets the foundation by outing the evolution of transistors, from the advent of the BJT to the modern LET structure. It discusses the unique features of LETs, which integrate both electrical and optical functions into a single device. These attributes make LETs particularly suited for applications in high-speed optical communication and OEICs. Furthermore, the chapter introduces the motivation behind employing LETs for thermal sensing, showcasing their potential to revolutionize temperature sensor technology by offering both high sensitivity and efficient thermal response.

doi:10.6342/NTU202500212



The second chapter focuses on the development of QW-HBTs for thermal sensing applications. The study introduces the novel concept of incorporating staircase SQWs in the base region of HBTs. Experimental results show a significant increase in collector current by approximately 73.23% as the substrate temperature increases from 25℃ to 85℃. This increase in current gain with temperature is distinct from conventional HBTs and is attributed to enhanced electron escape dynamics within the QWs. The modified charge-control model that incorporates thermionic emission theory effectively explains this behavior, supporting the design of optimized QW-HBT structures for smart thermal sensing devices.

Building upon the insights from Chapter 2, Chapter 3 extends the design to MQW and TQW HBTs. A modified charge-control model was developed for MQW-HBTs, which demonstrates the impact of QW positioning and number on the current gain. The model successfully predicts the behavior of TQW-HBTs, with experimental results showing an impressive 200% increase in collector current as the substrate temperature rises from 25℃ to 85℃. The TQW-HBTs demonstrated a current sensitivity of 7 μA/℃ under operating conditions of I_B of 1 mA and V_{CE} of 2 V. This significant thermal response positions TQW-HBTs as highly promising candidates for advanced thermal sensing applications in OEICs.

doi:10.6342/NTU202500212

In the chapter 4, a novel Darlington transistor configuration using LETs is introduced, leveraging their thermionic emission properties for enhanced thermal sensing performance. The LET device showed a 153% increase in collector current as the temperature increased from 25℃ to 85℃, while the Darlington configuration achieved a remarkable 210% increase under the same bias conditions. Thermal sensitivity analysis revealed a collector current-to-temperature ratio of 26.2 μA/℃ in the Darlington configuration, significantly higher than conventional thermal sensors. Despite these promising results, the chapter highlights challenges related to achieving a highly linear voltage-to-temperature response. Further optimizations are necessary to improve the quantum well structure to enhance linearity, thermal sensitivity, and current gain.

The chapter 5 provides a detailed analysis of the thermal sensitivity and linearity of QW-HBTs, focusing on the effect of QW width on thermal performance. Both experimental and simulation results demonstrate that narrower QWs exhibit higher thermal sensitivity but suffer from limitations in current gain at elevated temperatures. Conversely, wider QWs ensure better linearity but with reduced thermal sensitivity. The study identifies a QW width of 90 Å as optimal, achieving a thermal sensitivity of 1.34 mA/℃ and a linearity fitting parameter B of 0.67748 at 100℃, balancing thermal sensitivity and

doi:10.6342/NTU202500212

linearity. These findings provide essential insights for the design of next-generation temperature sensors in OEICs.

In conclusion, this thesis demonstrates the significant potential of LET-based devices, including SQW-HBTs, MQW-HBTs, and TQW-HBTs, in the development of advanced thermal sensors for smart sensing applications. By incorporating novel design approaches such as the Darlington transistor configuration, this work highlights a new direction for III-V based thermal sensor design for next generation for thermal sensing and OEICs with enhanced temperature sensitivity and performance. The result presented, including increases in collector current ranging from 73.23% to 210% as a function of temperature, underpins the viability of these devices as high-performance thermal sensing components. Furthermore, the thesis emphasizes the critical role of quantum well structures, design optimizations, and charge-control models in achieving efficient and accurate thermal sensing, laying the groundwork for the next generation of smart sensor technologies in the field of optoelectronics.

6.2 Recommendations and Future Research Directions

This thesis has demonstrated the outstanding performance of III-V compound semiconductor QW-based HBTs for thermal sensing applications. As a relatively new research topic, there remains significant potential for exploring the device physics of these

doi:10.6342/NTU202500212

transistors at elevated temperatures. This exploration could enable the design of highly efficient epitaxial layer structures with ultra-high thermal sensitivity and improved linearity for next-generation thermal sensing technologies. Below are some recommended directions for future research:

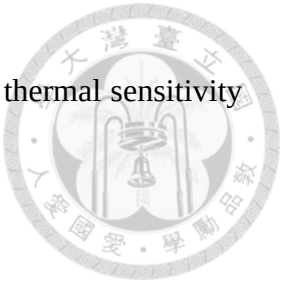
1) Advanced Charge-Control Model for QW-HBTs

The thesis introduced a modified charge-control model to predict the thermally enhanced current gain in QW-based HBTs. However, for MQW and TQW-based HBTs, effects such as tunneling current or quantum well coupling—neglected in this study due to the dominance of thermionic emission at high temperatures—need to be addressed. At lower temperatures or with narrower barriers between quantum wells, tunneling effects may become significant. Future work should focus on further modifying the charge-control model to account for such phenomena, enabling more accurate predictions of thermal behavior across a wider temperature range.

2) Optimization for Linearity and Sensitivity

Despite achieving ultra-high thermal sensitivity, nonlinearity persists due to non-linear electron escape from the quantum wells. Further optimization of the epitaxial layer design—by adjusting quantum well width, material composition, barrier height,

doi:10.6342/NTU202500212



and the number of quantum wells—is essential to enhance both thermal sensitivity and linearity.

3) Integration with Thermal Circuits

The ultra-high thermal sensitivity of LETs presents opportunities for designing thermal circuits, such as Darlington transistors, current mirrors, and ring oscillators, to serve as front-end components in smart thermal sensor applications. These circuits, combined with ADC designs, could be evaluated based on parameters such as resolution, error rate, accuracy, temperature sensitivity, and stability, compared to existing thermal sensing technologies.

4) Optical Sensing at Elevated Temperatures

The dual electrical and optical outputs of LETs can be leveraged for optical sensing applications at high temperatures. This dual functionality provides a versatile platform for exploring advanced sensing applications where traditional electrical-only sensors may face limitations.

5) Heterogeneous Integration with Si

By Combing the strength of Si and compound semiconductor, heterogenous integration techniques such as wafer bonding techniques, Epitaxial Lift-Off (ELO), 3D integration and Packing using TSVs and microbumps opens new possibilities for advanced, compact and cost-efficient technologies for mass production.

doi:10.6342/NTU202500212

By addressing these areas, researchers can further advance the performance, applicability, and commercialization of QW-HBT-based thermal sensing devices, paving the way for their adoption in next-generation smart thermal sensor technologies.

doi:10.6342/NTU202500212

References

[1] J. Bardeen and W. H. Brattain, “The transistor, a semi-conductor triode,” *Phys. Rev.*, vol. 74, no. 2, pp. 230–231, Jul. 1948, doi: 10.1103/PhysRev.74.230.

[2] W. Shockley, “The theory of p-n junctions in semiconductors and p-n junction transistors,” *Bell System Technical Journal*, vol. 28, no. 3, pp. 435–489, Jul. 1949, doi: 10.1002/j.1538-7305.1949.tb03645.x.

[3] W. Shockley, M. Sparks, and G. K. Teal, “p-n junction transistors,” *Phys. Rev.*, vol. 83, no. 1, pp. 151–162, Jul. 1951, doi: 10.1103/PhysRev.83.151.

[4] W. Shockley, “Circuit element utilizing semiconductive material.” United States of America Patent 2,569,347, 26 June 1948.

[5] H. Kroemer, “Theory of a wide-gap emitter for transistors,” *Proc. of the IRE*, vol. 45, no. 11, pp. 1535–1537, 1957, doi: 10.1109/JRPROC.1957.278348.

[6] W. Snodgrass, W. Hafez, N. Harff, and M. Feng, “Pseudomorphic InP/InGaAs heterojunction bipolar transistors (PHBTs) experimentally demonstrating f_T = 765 GHz at 25°C increasing to f_T = 845 GHz at -55°C,” in *Intern. Electron Devices Meeting*, 2006, pp. 1–4. doi: 10.1109/IEDM.2006.346853.

[7] Y. Shiratori, T. Hoshi, and H. Matsuzaki, “InGaP/GaAsSb/InGaAsSb/InP double heterojunction bipolar transistors with record f_t of 813 GHz,” *IEEE*

doi:10.6342/NTU202500212

Electron Device Lett., vol. 41, no. 5, pp. 697–700, May 2020, doi: 10.1109/LED.2020.2982497.

[8] R. N. Hall, G. E. Fenner, J. D. Kingsley, T. J. Soltys, and R. O. Carlson, "Coherent light emission from GaAs junctions," *Phys. Rev. Lett.*, vol. 9, no. 9, pp. 366–368, Nov. 1962, doi: 10.1103/PhysRevLett.9.366.

[9] N. Holonyak and S. F. Bevacqua, "Coherent (visible) light emission from $Ga(As_{1-x}P_x)$ junctions," *Appl. Phys. Lett.*, vol. 1, no. 4, pp. 82–83, Dec. 1962, doi: 10.1063/1.1753706.

[10] M. Feng, N. Holonyak, and W. Hafez, "Light-emitting transistor: Light emission from InGaP/GaAs heterojunction bipolar transistors," *Appl. Phys. Lett.*, vol. 84, no. 1, pp. 151–153, Jan. 2004, doi: 10.1063/1.1637950.

[11] M. Feng, N. Holonyak, and R. Chan, "Quantum-well-base heterojunction bipolar light-emitting transistor," *Appl. Phys. Lett.*, vol. 84, no. 11, pp. 1952–1954, Mar. 2004, doi: 10.1063/1.1669071.

[12] C. H. Wu, G. Walter, H. W. Then, M. Feng, and N. Holonyak, "Scaling of light emitting transistor for multigigahertz optical bandwidth," *Appl. Phys. Lett.*, vol. 94, no. 17, Apr. 2009, Art. no. 171101, doi: 10.1063/1.3126642.

[13] M. Feng, N. Holonyak, A. James, K. Cimino, G. Walter, and R. Chan, "Carrier lifetime and modulation bandwidth of a quantum well

doi:10.6342/NTU202500212

AlGaAs/InGaP/GaAs/InGaAs transistor laser," *Appl. Phys. Lett.*, vol. 89, no. 11, Sep. 2006, Art. no. 113504, doi: 10.1063/1.2346369.

[14] G. Walter, C. H. Wu, H. W. Then, M. Feng, and N. Holonyak, "4.3 GHz optical bandwidth light emitting transistor," *Appl. Phys. Lett.*, vol. 94, no. 24, Jun. 2009, Art. no. 241101, doi: 10.1063/1.3153146.

[15] M. Feng, N. Holonyak, G. Walter, and R. Chan, "Room temperature continuous wave operation of a heterojunction bipolar transistor laser," *Appl. Phys. Lett.*, vol. 87, no. 13, Sep. 2005, Art no. 131103, doi: 10.1063/1.2058213.

[16] M.-K. Wu, M. Feng, and N. Holonyak, "Surface emission vertical cavity transistor laser," *IEEE Photonics Technology Lett.*, vol. 24, no. 15, pp. 1346–1348, Aug. 2012, doi: 10.1109/LPT.2012.2203356.

[17] M. Feng, C.-H. Wu, M. K. Wu, C.-H. Wu, and N. Holonyak, "Resonance-free optical response of a vertical cavity transistor laser," *Appl. Phys. Lett.*, vol. 111, no. 12, Sep. 2017, Art. no. 121106, doi: 10.1063/1.5004133.

[18] C.-H. Wu and C.-H. Wu, "12 GHz spontaneous optical bandwidth tunnel junction light-emitting transistor," *Appl. Phys. Lett.*, vol. 115, no. 18, Oct. 2019, Art. no. 181102, doi: 10.1063/1.5124959.

[19] U. Cisco, "Cisco annual internet report (2018–2023) white paper," San Jose,

doi:10.6342/NTU202500212

CA, USA, Mar. 2020.

[20] H.-T. Cheng, Y.-T. Liang, Y.-T. Huang, S.-J. Hsu, W.-H. Lin, M. Feng, and C. H. Wu, "Electro-optical logics by three-terminal quantum-well-light-emitting transistors integration," *Photon. Res.*, vol. 12, no. 8, p. A51-A62, Aug. 2024, doi: 10.1364/PRJ.516274.

[21] H.-H. Chen, C.-W. Wang, and C.-H. Wu, "Monolithically integrated optical NAND gate using light-emitting transistors," in *23rd Opto-Electronics and Commun. Conf.*, Jul. 2018, pp. 1–2. doi: 10.1109/OECC.2018.8729956.

[22] A. Winoto, J. Qiu, D. Wu, Y.-T. Peng, and M. Feng, "Integrated photonics of transistor laser, detector and active load for all optical NOR gate," in *Inter. Symp. on VLSI Techn. Syst. and Appl.*, Apr. 2019, pp. 1–5. doi: 10.1109/VLSI-TSA.2019.8804656.

[23] A. Winoto, J. Qiu, D. Wu, and M. Feng, "Transistor laser-integrated photonics for optical logic: Unlocking unique electro-optical integration potential to open up new possibilities for logic processors," *IEEE Nanotech. Mag.*, vol. 13, no. 2, pp. 27–34, Apr. 2019, doi: 10.1109/MNANO.2019.2891978.

[24] Y.-T. Liang, Y.-T. Huang, C.-H. Wu, and H.-Y. Lin, "Monolithically integrated opto-electrical NOR gate using light emitting transistors," in *Opto-Electronics and Commun. Conf. (OECC)*, Oct. 2020, pp. 1–3. doi:

doi:10.6342/NTU202500212

10.1109/OECC48412.2020.9273560.

[25] Y.-T. Chen, Y.-T. Liang, and C.-H. Wu, “Monolithically integrated optoelectronic multiplexer circuit using light emitting transistors,” in *Proc. Opto-Electron. Commun. Conf. (OECC)*, Jul. 2021, pp. 1-3, doi: 10.1364/OECC.2021.T3E.2.

[26] M. Feng, A. Winoto, J. Qiu, Y.-T. Peng, and N. Holonyak, “All optical NOR gate via tunnel-junction transistor lasers for high speed optical logic processors,” in *Intern. Symp. on VLSI Techn., Syst. and Appl. (VLSI-TSA)*, Apr. 2018, pp. 1–2. doi: 10.1109/VLSI-TSA.2018.8403847.

[27] Y. Xiao Y. Xiao, T.-Z. Wu, S.-J. Dang, Y.-L. Gao, Y. Lin, L.-H. Zhu, Z.-Q. Guo, Y.-J. Lu, and Z. Chen, “Determining junction temperature of LEDs by the relative reflected intensity of the incident exciting light,” *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2257–2260, May 2017, doi: 10.1109/TED.2017.2678513.

[28] G. C. M. Meijer, “Thermal sensors based on transistors,” *Sens. and Actuat.*, vol. 10, pp. 103–125, Sep. 1986, doi: 10.1016/0250-6874(86)80037-3.

[29] J. P. Bentley, “Temperature sensor characteristics and measurement system design,” *J. Phys. E*, vol. 17, no. 6, pp. 430–439, Jun. 1984, doi: 10.1088/0022-3735/17/6/002.

doi:10.6342/NTU202500212

[30] A. Bakker, “CMOS smart temperature sensors-An overview,” in *Proc. SENSORS,* Vol. 2, Jun. 2002, pp. 1423–1427, doi: 10.1109/ICSENS.2002.1037330.

[31] K. A. A. Makinwa, “Smart temperature sensors in standard CMOS,” *Proc. Eng.*, vol. 5, pp. 930–939, 2010, doi: 10.1016/j.proeng.2010.09.262.

[32] I. M. Dmitrenko, S. P. Logvinenko, N. I. Ivanov, and Z. M. Kolot, “Thermometric characteristics of semiconductor diodes,” *Cryogenics*, vol. 6, no. 6, pp. 357–358, Dec. 1966, doi: 10.1016/0011-2275(66)90137-8.

[33] K. Souri, Y. Chae, Y. Ponomarev, and K. A. A. Makinwa, “A precision DTMOST-based temperature sensor,” in *Proc. ESSCIRC,* Sep. 2011, pp. 279–282. doi: 10.1109/ESSCIRC.2011.6044961.

[34] M. A. P. Pertijs, A. Niederkorn, Xu Ma, B. McKillop, A. Bakker, and J. H. Huijsing, “A CMOS smart temperature sensor with a 3 sigma inaccuracy of +/-0.5 degrees C to 120 degrees C,” *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 454–461, Feb. 2005, doi: 10.1109/JSSC.2004.841013.

[35] F. Sebastiano, L. J. Breems, K. A. A. Makinwa, S. Drago, D. M. W. Leenaerts, and B. Nauta, “A 1.2-V 10-μ W NPN-based temperature sensor in 65-nm CMOS with an inaccuracy of 0.2℃ (3σ) from -70℃ to 125℃,” *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2591–2601, Dec. 2010, doi:

doi:10.6342/NTU202500212

10.1109/JSSC.2010.2076610.

[36] Z. Shenghua and W. Nanjian, “A novel ultra low power temperature sensor for UHF RFID tag chip,” in *IEEE Asian Solid-State Circuits Conf.*, Nov. 2007, pp. 464–467. doi: 10.1109/ASSCC.2007.4425731.

[37] A. L. Aita, M. Pertijs, K. Makinwa, and J. H. Huijsing, “A CMOS smart temperature sensor with a batch-calibrated inaccuracy of ±0.25°C (3σ) from -70°C to 130°C,” in *IEEE Inter. Solid-State Circuits Conf.*, Feb. 2009, pp. 342-343,343a. doi: 10.1109/ISSCC.2009.4977448.

[38] M. A. P. Pertijs and J. H. Huijsing, *Precision temperature sensors in CMOS technology*. Doedrecht, Netherlands: Springer, 2006.

[39] C. Cahoon and R. J. Baker, “Low-voltage CMOS temperature sensor design using schottky diode-based references,” in *IEEE Workshop on Microelectronics and Electron Devices.*, Apr. 2008, pp. 16–19. doi: 10.1109/WMED.2008.4510657.

[40] P. Chen, C.-C. Chen, C.-C. Tsai, and W.-F. Lu, “A time-to-digital-converter-based CMOS smart temperature sensor,” *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1642–1648, Aug. 2005, doi: 10.1109/JSSC.2005.852041.

[41] S. Park, C. Min, and S. Cho, “A 95nW ring oscillator-based temperature sensor for RFID tags in 0.13 μm CMOS,” in *IEEE Intern. Symp. on Circuits*

doi:10.6342/NTU202500212

and Systems, May 2009, pp. 1153–1156. doi: 10.1109/ISCAS.2009.5117965.

[42] C. P. L. van Vroonhoven, D. d'Aquino, and K. A. A. Makinwa, "A thermal-diffusivity-based temperature sensor with an untrimmed inaccuracy of ±0.2°C (3s) from -55°C to 125°C," in *IEEE Inter. Solid-State Circuits Conf.-(ISSCC)*, Feb. 2010, pp. 314–315. doi: 10.1109/ISSCC.2010.5433900.

[43] B. Razavi, *Design of analog CMOS integrated circuits*. New York, NY, USA: McGraw-Hill, 2005.

[44] L. Lu, B. Vosooghi, J. Chen, and C. Li, "A subthreshold-MOSFETs-based scattered relative temperature sensor front-end with a non-calibrated ±2.5°C 3σ relative inaccuracy from -40°C to 100°C," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1104–1112, May 2013, doi: 10.1109/TCSI.2013.2249131.

[45] G. Giustolisi, G. Palumbo, M. Criscione, and F. Cutri, "A low-voltage low-power voltage reference based on subthreshold MOSFETs," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 151–154, Jan. 2003, doi: 10.1109/JSSC.2002.806266.

[46] N. Chand, R. Fischer, T. Henderson, J. Klem, W. Kopp, and H. Morkoç, "Temperature dependence of current gain in AlGaAs/GaAs heterojunction bipolar transistors," *Appl. Phys. Lett.*, vol. 45, no. 10, pp. 1086–1088, Nov.

doi:10.6342/NTU202500212

1984, doi: 10.1063/1.95024.

[47] H. Ito, T. Ishibashi, and T. Sugeta, “Current gain enhancement in graded base AlGaAs/GaAs HBTs associated with electron drift motion,” *Jpn. J. Appl. Phys.*, vol. 24, no. 4A, p. L241, Apr. 1985, doi: 10.1143/JJAP.24.L241.

[48] K. Ikossi-Anastasiou, A. Ezis, K. R. Evans, and C. E. Stutz, “Low-temperature characterization of high-current-gain graded-emitter AlGaAs/GaAs narrow-base heterojunction bipolar transistor,” *IEEE Electron Device Lett.*, vol. 13, no. 8, pp. 414–417, Aug. 1992, doi: 10.1109/55.192776.

[49] W. Liu, S.-K. Fan, T. Henderson, and D. Davito, “Temperature dependences of current gains in GaInP/GaAs and AlGaAs/GaAs heterojunction bipolar transistors,” *IEEE Trans. Electron Devices*, vol. 40, no. 7, pp. 1351–1353, Jul. 1993, doi: 10.1109/16.216446.

[50] L. L. Liou and B. Bayraktaroglu, “Thermal stability analysis of AlGaAs/GaAs heterojunction bipolar transistors with multiple emitter fingers,” *IEEE Trans. Electron Devices*, vol. 41, no. 5, pp. 629–636, May 1994, doi: 10.1109/16.285008.

[51] Y.-S. Lin and J.-J. Jiang, “Temperature dependence of current gain, ideality factor, and offset voltage of AlGaAs/GaAs and InGaP/GaAs HBTs,” *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2945–2951, Dec. 2009, doi:

doi:10.6342/NTU202500212

10.1109/TED.2009.2033325.

[52] E. S. Yang, C. C. Hsu, H. B. Lo, and Y.-F. Yang, “Modeling of current gain’s temperature dependence in heterostructure-emitter bipolar transistors,” *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1315–1319, Jul. 2000, doi: 10.1109/16.848270.

[53] Y.-H. Chang, Y.-L. Chou, S.-W. Chang, and C.-H. Wu, “Thermally-enhanced current gain of quantum-well heterojunction bipolar transistor,” *J. Appl. Phys.*, vol. 126, no. 1, Jul. 2019, Art. no. 014503, doi: 10.1063/1.5091050.

[54] H. Karan and A. Biswas, “Improving performance of light-emitting diodes using InGaN/GaN MQWs with varying trapezoidal bottom well width,” *Otik*, vol. 247, Dec. 2021, Art. no. 167888, doi: 10.1016/j.ijleo.2021.167888.

[55] K. Souri and K. A. Makinwa, “Readout methods for BJT-based temperature sensors,” in Energy-Efficient Smart Temperature Sensors in CMOS Technology (Analog Circuit and Signal Processing), 1st ed. Cham, The Netherland: Springer, Oct. 2017, pp. 19–36, doi: 10.1007/978-3- 319-62307-8_2.

[56] H. W. Then, M. Feng, N. Holonyak, and C. H. Wu, “Experimental determination of the effective minority carrier lifetime in the operation of a quantum-well n-p-n heterojunction bipolar light-emitting transistor of

doi:10.6342/NTU202500212

varying base quantum-well design and doping," *Appl. Phys. Lett.*, vol. 91, no. 3, Jul. 2007, Art. no. 033505, doi: 10.1063/1.2759263.

[57] M. Feng, N. Holonyak, H. W. Then, and G. Walter, "Charge control analysis of transistor laser operation," *Appl. Phys. Lett.*, vol. 91, no. 5, Jul. 2007, Art. no. 053501, doi: 10.1063/1.2767172.

[58] B. Faraji, W. Shi, D. L. Pulfrey, and L. Chrostowski, "Analytical modeling of the transistor laser," *IEEE J. of Sel. Topics Quantum Electron.*, vol. 15, no. 3, pp. 594–603, May/Jun. 2009, doi: 10.1109/JSTQE.2009.2013178.

[59] L. Zhang and J.-P. Leburton, "Modeling of the transient characteristics of heterojunction bipolar transistor lasers," *IEEE J. Quantum Electron.*, vol. 45, no. 4, pp. 359–366, Apr. 2009, doi: 10.1109/JQE.2009.2013215.

[60] I. Taghavi, H. Kaatuzian, and J.-P. Leburton, "Bandwidth enhancement and optical performances of multiple quantum well transistor lasers," *Appl. Phys. Lett.*, vol. 100, no. 23, Jun. 2012, Art. no. 231114, doi: 10.1063/1.4727898.

[61] R. Basu, B. Mukhopadhyay, and P. K. Basu, "Modeling of current gain compression in common emitter mode of a transistor laser above threshold base current," *J. Appl. Phys.*, vol. 111, no. 8, Apr. 2012, Art no. 083103, doi: 10.1063/1.4703926.

[62] Y. Li and J.-P. Leburton, "Quantum well capture and base carrier lifetime in

doi:10.6342/NTU202500212

light emitting transistor," *Appl. Phys. Lett.*, vol. 113, no. 17, Oct. 2018, Art. no. 171110, doi: 10.1063/1.5044758.

[63] L. Yang, S.-W. Chang, and C.-H. Wu, "A four-port model of light-emitting transistors for circuit simulation and application," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5572–5580, Dec. 2020, doi: 10.1109/TED.2020.3028326.

[64] C.-T. Tung, H.-Y. Lin, S.-W. Chang, and C.-H. Wu, "Analytical modeling of tunnel-junction transistor lasers," *IEEE J. of Sel. Topics Quantum Electron.*, vol. 28, no. 1: semiconductor lasers, pp. 1–8, Jan.-Feb. 2022, Art no. 1501008, doi: 10.1109/JSTQE.2021.3090527.

[65] H. Schneider and K. V. Klitzing, "Thermionic emission and Gaussian transport of holes in a GaAs/ $Al_xGa_{1-x}As$ multiple-quantum-well structure," *Phys. Rev. B*, *Condens. Matter*, vol. 38, no. 9, pp. 6160–6165, Sep. 1988, doi: 10.1103/PhysRevB.38.6160.

[66] R. Nagarajan, "Carrier transport effects in quantum well lasers: An overview," *Opt. Quantum Electron.*, vol. 26, no. 7, pp. S647–S666, Jul. 1994, doi: 10.1007/BF00326653.

[67] J. Nelson, M. Paxman, K. W. J. Barnham, J. S. Roberts, and C. Button, "Steady-state carrier escape from single quantum wells," *IEEE J. Quantum*

doi:10.6342/NTU202500212

Electron., vol. 29, no. 6, pp. 1460–1468, Jun. 1993, doi: 10.1109/3.234396.

[68] M. Mosko and K. Kálna, "Carrier capture into a GaAs quantum well with a separate confinement region: comment on quantum and classical aspects," *Semicond Sci. Technol.*, vol. 14, no. 9, pp. 790–796, Sep. 1999, doi: 10.1088/0268-1242/14/9/308.

[69] S. Tiwari and S. L. Wright, "Material properties of *p*-type GaAs at large dopings," *Appl. Phys. Lett.*, vol. 56, no. 6, pp. 563–565, Feb. 1990, doi: 10.1063/1.102745.

[70] M. L. Lovejoy, M. R. Melloch, and M. S. Lundstrom, "Temperature dependence of minority and majority carrier mobilities in degenerately doped GaAs," *Appl. Phys. Lett.*, vol. 67, no. 8, pp. 1101–1103, Aug. 1995, doi: 10.1063/1.114974.

[71] G. W.'t Hooft, M. R. Leys, and H. J. Talen-v.d. Mheen, "Temperature dependence of the radiative recombination coefficient in GaAs(Al, Ga)As quantum wells," *Superlattices Microstructures*, vol. 1, no. 4, pp. 307–310, Jan. 1985, doi: 10.1016/0749-6036(85)90092-8.

[72] Y. Arakawa, H. Sakaki, M. Nishioka, J. Yoshino, and T. Kamiya, "Recombination lifetime of carriers in GaAs-GaAlAs quantum wells near room temperature," *Appl. Phys. Lett.*, vol. 46, no. 5, pp. 519–521, Mar. 1985,

doi:10.6342/NTU202500212

doi: 10.1063/1.95578.

[73] P. T. Landsberg, “The band-band Auger effect in semiconductors,” *Solid State Electron*, vol. 30, no. 11, pp. 1107–1115, Nov. 1987, doi: 10.1016/0038-1101(87)90074-8.

[74] D. McDonald and R. F. O’Dowd, “Comparison of two- and three-level rate equations in the modeling of quantum-well lasers,” *IEEE J. Quantum Electron.*, vol. 31, no. 11, pp. 1927–1934, Nov. 1995, doi: 10.1109/3.469272.

[75] B. Faraji, W. Shi, D. L. Pulfrey, and L. Chrostowski, “Common-emitter and common-base small-signal operation of the transistor laser,” *Appl. Phys. Lett.*, vol. 93, no. 14, Oct. 2008, Art. no. 143503, doi: 10.1063/1.2998267.

[76] B. Faraji, D. L. Pulfrey, and L. Chrostowski, “Small-signal modeling of the transistor laser including the quantum capture and escape lifetimes,” *Appl. Phys. Lett.*, vol. 93, no. 10, Sep. 2008, Art. no. 103509, doi: 10.1063/1.2981799.

[77] I. Taghavi, H. Kaatuzian, and J.-P. Leburton, “Multiple versus single quantum well transistor laser performances,” in *Proc. Integer. Photon. Res., Silicon Nanophoton.*, Washington, DC, USA, Jun. 2012, pp. 1-3, doi: 10.1364/IPRSN.2012.IM4B.5.

[78] I. Taghavi, H. Kaatuzian, and J.-P. Leburton, “Performance optimization of

doi:10.6342/NTU202500212

multiple quantum well transistor laser," *IEEE J. Quantum Electron.*, vol. 49, no. 4, pp. 426–435, Apr. 2013, doi: 10.1109/JQE.2013.2250488.

[79] R. Ranjan, P. Pareek, S. S. Anwer Askari, and M. K. Das, "Small signal analysis of tin-incorporated group-IV alloys based multiple quantum well transistor laser," in Proc. *Int. Conf. Numer. Simulation Optoelectron. Devices (NUSOD)*, Nov. 2018, pp. 73–74. doi: 10.1109/NUSOD.2018.8570273.

[80] R. Basu, B. Mukhopadhyay, and P. K. Basu, "Modeling resonance-free modulation response in transistor lasers with single and multiple quantum wells in the base," *IEEE Photon. J.*, vol. 4, no. 5, pp. 1572–1581, Oct. 2012, doi: 10.1109/JPHOT.2012.2211075.

[81] R. Basu, B. Mukhopadhyay, and P. K. Basu, "Analytical model for threshold-base current of a transistor laser with multiple quantum wells in the base," *IET Optoelectron.*, vol. 7, no. 3, pp. 71–76, Jun. 2013, doi: 10.1049/iet-opt.2012.0039.

[82] R. Ranjan, P. Pareek, S. S. A. Askari, and M. K. Das, "Performance analysis of GeSn-alloy-based multiple quantum well transistor laser," in *Proc. Phys. Simulation Optoelectron. Devices XXVI*, Feb. 2018, p. 85. doi: 10.1117/12.2290570.

[83] I. Taghavi, B. Namvar, M. Hosseini, and H. Kaatuzian, "Large signal analysis

doi:10.6342/NTU202500212

of multiple quantum well transistor laser: Investigation of imbalanced carrier and photon density distribution," *J. Appl. Phys.*, vol. 127, no. 13, Apr. 2020, Art. no. 133102, doi: 10.1063/5.0003290.

[84] R. Ranjith, S. Piramasubramanian, and M. Ganesh Madhan, "Effect of number of quantum wells on modulation and distortion characteristics of transistor laser," *Opt. Laser Technol.*, vol. 147, Mar. 2022, Art. no. 107655, doi: 10.1016/j.optlastec.2021.107655.

[85] R. Ranjan, M. K. Das, and S. Kumar, "Performance analysis of tin-incorporated group-IV alloy based transistor laser," *Opt. Laser Technol.*, vol. 106, pp. 228–233, Oct. 2018, doi: 10.1016/j.optlastec.2018.04.010.

[86] I. Taghavi, H. Kaatuzian, and J.-P. Leburton, "A nonlinear gain model for multiple quantum well transistor lasers," *Semicond. Sci. Technol.*, vol. 28, no. 2, Feb. 2013, Art. no. 025022, doi: 10.1088/0268-1242/28/2/025022.

[87] R. Basu, B. Mukhopadhyay, and P. K. Basu, "Performance study of a tunnel injection transistor laser with multiple quantum-wells in the base," in *Proc. 12th Int. Conf. Fiber Opt. Photon.*, Dec. 2014, p. 1-3, doi: 10.1364/PHOTONICS.2014.M4A.4.

[88] S. Piramasubramanian, M. Ganesh Madhan, V. Radha, S. M. S. Shajithaparveen, and G. Nivetha, "Effect of quantum well position on the

doi:10.6342/NTU202500212

distortion characteristics of transistor laser," *Opt. Commun.*, vol. 414, pp. 22–28, May 2018, doi: 10.1016/j.optcom.2017.12.055.

[89] M. Kumar, S.-J. Hsu, S.-Y. Ho, S.-W. Chang, and C.-H. Wu, "Current gain enhancement of heterojunction bipolar light-emitting transistors using staircase InGaAs quantum well," *IEEE Trans. Electron Devices*, vol. 70, no. 10. Pp. 5177-5183, Oct 2023, doi: 10.1109/TED.2023.3305355.

[90] H.-H. Yang, W.-C. Tu, H.-L. Wang, and C.-H. Wu, "Investigation of effective base transit time and current gain modulation of light-emitting transistors under different ambient temperatures," *Appl. Phys. Lett.*, vol. 105, no. 18, Nov. 2014, Art., no. 181119, doi: 10.1063/1.4901338.

[91] H.-L. Wang, P.-H. Chou, and C.-H. Wu, "Microwave determination of quantum-well capture and escape time in light-emitting transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1088–1091, Mar. 2013, doi: 10.1109/TED.2013.2242330.

[92] H.-L. Wang, Y.-J. Huang, and C.-H. Wu, "Optical frequency response analysis of light-emitting transistors under different microwave configurations," *Appl. Phys. Lett.*, vol. 103, no. 5, Jul. 2013, Art. no. 051110, doi: 10.1063/1.4817545.

[93] H.-L. Wang, H.-H. Yang, and C.-H. W. Wu, "Quantum well saturation effect on the reduction of base transit time in light-emitting transistors," *IEEE Trans.*

doi:10.6342/NTU202500212

Electron Devices, vol. 61, no. 10, pp. 3472–3476, Oct. 2014, doi: 10.1109/TED.2014.2349922.

[94] H. R. Mojaver and H. Kaatuzian, "Analysis and improvement of optical frequency response in a long wavelength transistor laser," *Opt. Quantum Electron.*, vol. 44, nos. 1–2, pp. 45–54, May 2012, doi: 10.1007/s11082-011-9531-2.

[95] L. Zhang and J.-P. Leburton, "Modeling of the transient characteristics of heterojunction bipolar transistor lasers," *IEEE J. Quantum Electron.*, vol. 45, no. 4, pp. 359–366, Apr. 2009, doi: 10.1109/JQE.2009.2013215.

[96] C.-Y. Tsai, L. F. Eastman, Y.-H. Lo, and C.-Y. Tsai, "Breakdown of thermionic emission theory for quantum wells," *Appl. Phys. Lett.*, vol. 65, no. 4, pp. 469–471, Jul. 1994, doi: 10.1063/1.112339.

[97] C.-Y. Tsai, C.-Y. Tsai, Y.-H. Lo, R. M. Spencer, and L. F. Eastman, "Nonlinear gain coefficients in semiconductor quantum-well lasers: Effects of carrier diffusion, capture, and escape," *IEEE J. Sel. Topics in Quantum Electron.*, vol. 1, no. 2, pp. 316–330, Jun. 1995, doi: 10.1109/2944.401211.

[98] M. S. Frost, M. Riches, and T. Kerr, "A p-n-p AlGaAs heterojunction bipolar transistor for high-temperature operation," *J. Appl. Phys.*, vol. 60, no. 6, pp. 2149–2153, Sep. 1986, doi: 10.1063/1.337168.

doi:10.6342/NTU202500212

[99] M. H. Perrott M. H. Perrott, J. C. Salvia, F. S. Lee, A. Partridge, S. Mukherjee, C. Arft, J. Kim, N. Arumugam, P. Gupta, S. Tabatabaei, S. Pamarti, H. Lee, and F. Assaderaghi, "A temperature-to-digital converter for a MEMS-based programmable oscillator with < ±0.5-ppm frequency stability and < 1-ps integrated jitter," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 276–291, Jan. 2013, doi: 10.1109/JSSC.2012.2218711.

[100] W. Tian, B. Bas, D. Harmsen, K. Williams, and X. Leijtens, "Temperature sensing diode in InP-based photonic integration technology," *IEEE Photon. J.*, vol. 16, no. 2, pp. 1–8, Apr. 2024, doi: 10.1109/JPHOT.2024.3374266.

[101] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of 0.1°C from -55°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005, doi: 10.1109/JSSC.2005.858476.

[102] Z. Huang, Z. Tang, X.-P. Yu, Z. Shi, L. Lin, and N. N. Tan, "A BJT-based CMOS temperature sensor with duty-cycle-modulated output and ±0.5°C (3s) inaccuracy from −40 °C to 125 °C," *IEEE Trans. on Circuits Syst. II: Exp. Briefs*, vol. 68, no. 8, pp. 2780–2784, Aug. 2021, doi: 10.1109/TCSII.2021.3068283.

[103] S. Xie and A. J. P. Theuwissen, "On-chip smart temperature sensors for dark

doi:10.6342/NTU202500212

current compensation in CMOS image sensors," *IEEE Sensors J.*, vol. 19, no. 18, pp. 7849–7860, Sep. 2019, doi: 10.1109/JSEN.2019.2919655.

[104] I. Vikulin, V. Gorbachev, A. Gorbacheva, V. Krasova, and V. Litvinenko, "Radiation resistant FET-based temperature sensor for end devices of IoT," in Proc. 3rd Int. *Conf. Adv. Inf. and Commu. Technol. (AICT)*, Jul. 2019, pp. 272–277. doi: 10.1109/AIACT.2019.8847905.

[105] B. Wu, J. M. Dallesasse, and J.-P. Leburton, "Design and novel turn-off mechanism in transistor lasers," *J. Phys., Photon.*, vol. 3, no. 3, Jul. 2021, Art. no. 034018, doi: 10.1088/2515-7647/ac0b4d.

doi:10.6342/NTU202500212

APPENDIX A

List of Publications

Journals:

1) **Mukul Kumar**, S.-W. Chang, and C.-H. Wu, "Investigation of thermal sensitivity and linearity of quantum well-based heterojunction bipolar transistor," *IEEE Transactions on Electron Devices*, Early Access, Nov 2024, doi: 10.1109/TED.2024.3492153.

2) **Mukul Kumar**, K.-Y. Hsueh, S.-J. Hsu, and C.-H. Wu, "Design and fabrication of novel Darlington transistor using light-emitting transistors for smart thermal sensor technology," *IEEE Electron Device Letters*, vol. 45, no. 7, pp. 1365-1368, July, 2024, doi:10.1109/LED.2024.3401084.

3) **Mukul Kumar**, S.-Y. Ho, S.-J. Hsu, P.-C. Li, S.-W. Chang, and C.-H. Wu, "Current gain enhancement at high-temperature operation of triple-quantum-well heterojunction bipolar light-emitting transistor for smart thermal sensor application," *IEEE Trans. Electron Devices*, vol. 71, no.1, pp. 896-903, Jan. 2024, doi: 10.1109/TED.2023.3339084.

4) **Mukul Kumar**, S.-J. Hsu, S.-Y. Ho, S.-W. Chang, and C.-H. Wu, "Current gain enhancement of heterojunction bipolar light-emitting transistor using staircase

doi:10.6342/NTU202500212

InGaAs quantum well," *IEEE Trans. Electron Devices*, vol. 70, no. 10, pp. 5177-5183, Oct, 2023, doi:10.1109/TED.2023.3305355.

5) **Mukul Kumar**, L.-C. Hsueh, S.-W. Cheng, S.-W. Chang, and C.-H. Wu, "Analytical modeling of current gain in multiple-quantum-well heterojunction bipolar light-emitting transistors," *IEEE Trans. Electron Devices*, vol. 71, no. 1, pp. 343-349, Jan 2024, doi:10.1109/TED.2023.3289930.

Journals Under Review:

i. **Mukul Kumar**, and C.-H. Wu, "Ultra-high thermal sensitivity using Darlington-cascaded triple-quantum-well heterojunction bipolar light-emitting transistor," *IEEE Trans Electron Devices*.

ii. **Mukul Kumar**, and C.-H. Wu, "TCAD based modeling and simulation for current gain enhancement of InGaP/GaAs light-emitting transistor for wide range of temperature applications," *Physica Status Solidi: Application and Materials Science*.

Journals Preparing for Submission:

I. Thermally Enhanced Current Gain of W-Shaped Quantum-Well Heterojunction Bipolar Transistor for Smart Thermal Sensor Application (IEEE-TED).

II. Investigate the effect of square emitter size on electrical and optical characteristics of heterojunction bipolar light-emitting transistor (IEEE-EDL)

doi:10.6342/NTU202500212

III. Emitter Size Effect on the Electrical and Optical characteristics of ultra-high thermal sensitivity Darlington transistor (IEEE-EDL)

Conferences:

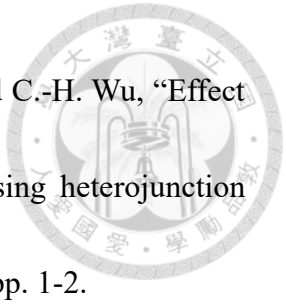
1) **Mukul Kumar**, K.-Y. Hsueh, Y.-J. Huang, G.-J. Lai, and C.-H. Wu, "Enhancing thermal sensing with cascaded quantum-well heterojunction bipolar transistors in Darlington transistor Configuration," *in Proc. CLEO-PR*, Aug. 2024, pp. 1-2, doi: 10.1109/CLEO-PR60912.2024.10676668.

2) **Mukul Kumar**, K.-Y. Hsueh, Y.-J. Huang, and C.-H. Wu, "A Darlington transistor using cascaded n-p-n light-emitting transistors for temperature sensor applications," in *Proc. DRC*, June, 2024, pp. 1-2, doi: 10.1109/DRC61706.2024.10605405.

3) S.-J. Hsu, S.-W. Cheng, S.-Y. Ho, P.-C. Li, **Mukul Kumar**, and C.-H. Wu, "The impact of mesa size scaling on heterojunction bipolar light emitting transistor in optoelectronic logic gate applications", *in Proc. Optics & Photonics Taiwan International Conference (OPTIC)*, Dec., 2023, pp. 1-2.

4) **Mukul Kumar**, S.-Y. Ho, S.-J. Hsu, P.-C. Li, S.-W. Cheng, and C.-H. Wu, "High temperature operation of triple-quantum well light emitting transistor for smart thermal sensor application", *in Proc. International Electron Devices & Materials Symposium (IEDMS)*, Oct., 2023, pp. 1-2.

doi:10.6342/NTU202500212



5) S.-J. Hsu, S.-W. Cheng, S.-Y. Ho, P.-C. Li, **Mukul Kumar**, and C.-H. Wu, "Effect of mesa scaling on optoelectronics logic gate performance using heterojunction bipolar light emitting transistors", *in Proc. IEDMS*, Oct., 2023, pp. 1-2.

6) **Mukul Kumar**, L.-C. Hsueh, S.-W. Cheng, S.-Y. Ho, S.-J. Hsu, C.-H. Wu, "Effect of quantum-well number of on the current gain of heterojunction bipolar light-emitting transistors" *in Proc. CLEO*, May 2023, pp. 1-2, doi: 10.1364/cleo_at.2023.jw2a.43.

7) **Mukul Kumar**, S.-W. Cheng, P.-C. Li, S.-J. Hsu, S.-J. Hsu, and C.-H. Wu, "Simulation study of temperature effect on current gain of heterojunction bipolar light-emitting transistors", *in Proc. CSW*, May 2023, pp. 1-2.

8) S.-W. Cheng, Y.-T. Chen, **Mukul Kumar**, and C.-H. Wu, "The development and performance of InGaP/GaAs single-quantum-well heterojunction phototransistors," *in Proc. Asia Commun. and Photon. Conf. (ACP)*, Nov. 2022, pp. 1472–1474. doi:10.1109/ACP55869.2022.10088778.

9) S.-W. Cheng, L.-C. Hsueh, S.-J. Hsu, **Mukul Kumar**, C.-H. Wu, "The development of integrated optoelectronic amplifiers and thermal sensors using light-emitting transistors circuits," *in proc. OPTIC*, Dec, 2022, pp. 1-2.

doi:10.6342/NTU202500212

10) **Mukul Kumar**, Y.-T. Chen, L.-C. Hsueh and C.-H. Wu, "Simulation study of quantum-well heterojunction bipolar transistor structure to thermally-enhanced current gain for thermal sensor application," *in proc. OPTIC*, Dec. 2021, pp. 1-2.

11) L.-C. Hsueh, S.-W. Cheng, H.-Y. Lin, **Mukul Kumar** and C.-H. Wu, "Development of integrated optoelectrical amplifier and high resolution smart thermal sensor with light-emitting transistors," *in proc. OPTIC*, Dec. 2021. pp. 1-2.

12) L.-C. Hsueh, S.-W. Cheng, H.-Y. Lin, **Mukul Kumar** and C.-H. Wu, "The first demonstration of the optoelectrical amplifier and high resolution thermal sensor with light-emitting transistors," *in Proc. IEDMS*, Nov. 2021, pp. 1-2.

13) **Mukul Kumar**, L.-C. Hsueh, Y.-T. Chen and C.-H. Wu, "Thermally-enhanced current gain of light-emitting transistors: A simulation-based analysis," *in IEDMS*, Nov. 2021, pp. 1-2.

14) L.-C. Hsueh, H.-Y. Lin, **Mukul Kumar**, and C.-H. Wu, "Thermal dynamic performance and integrated optoelectronic system with InGaP / GaAs quantum well light-emitting transistors (LETs)," *in Proc. Asia Commun. and Photon. Conf. (ACP),* Oct 2021, pp. 1-3, doi: M5D.2. doi: 10.1364/ACPC.2021.M5D.2.

doi:10.6342/NTU202500212

APPENDIX B

List of Abbreviations

Abbreviation	Detail
1QW-HBT	Single Quantum-Well Heterojunction Bipolar Transistor
2QW-HBT	Double Quantum-Well Heterojunction Bipolar Transistor
ADC	Analog-to-Digital Converter
ADS	Advanced Design System
B-C junction	Base-to-Collector Junction
BJT	Bipolar Junction Transistor
BOE	Buffered Oxide Etchant
CAGR	Compound Annual Growth Rate
CCD	Charge-Coupled Device
CISCO	Cisco Systems, Inc.
CMOS	Complementary Metal-Oxide Semiconductor
CTAT	Complementary to Absolute Temperature
DBR	Distributed Bragg Reflector
DC	Direct Current
DI	Deionized

doi:10.6342/NTU202500212

DL	Diode Laser
DUV	Deep Ultraviolet
EQW	Emitter to the QW Region
ETF	Electrothermal Filter
E-to-O	Electrical-to-Optical
F-K	Franz-Keldysh
GHz	Gigahertz
HBLET	Heterojunction Bipolar Light-Emitting Transistor
HBT	Heterojunction Bipolar Transistor
ICPAT	Intra-Cavity Photon-Assisted Tunneling
IOED Lab	Integrated Optoelectronic Device Lab
IoT	Internet of Things
IPA	Isopropyl Alcohol
I-V	Current-Voltage
LET	Light-Emitting Transistor
LO Photons	Longitudinal Optical Photons
MBE	Molecular Beam Epitaxy
MOCVD	Metal Organic Chemical Vapor Deposition

doi:10.6342/NTU202500212

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MQW	Multiple-Quantum-Well
MQW-HBT	Multiple-Quantum-Well Heterojunction Bipolar Transistor
MQW-TL	Multiple-Quantum-Well Transistor Laser
NiCr	Nickel-Chromium
NMP	N-Methyl-2-Pyrrolidone
OEIC	Optoelectronic Integrated Circuit
OI	Optical Interconnect
O-to-E	Optical-to-Electrical
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PTAT	Proportional to Absolute Temperature
QW	Quantum Well
QWB	Quantum-Well-Barrier
QW-HBLET	Quantum-Well Heterojunction Bipolar Light-Emitting Transistor
QW-HBT	Quantum-Well Heterojunction Bipolar Transistors
RIE	Reactive Ion Etching
RTP	Rapid Thermal Processing
S.I.	Semi-Insulating

doi:10.6342/NTU202500212

SCH	Separate Confinement Heterojunction
SDC	Signal-to-Digital Converter
SiN_X	Silicon Nitride
SQW-HBT	Single Quantum Well-Based HBT
SRH	Shockley-Read-Hall
TDC	Time-to-Digital Converter
TJTL	Tunnel-Junction Transistor Laser
TL	Transistor Laser
TQW	Triple-Quantum-Well
TQW-HBLET	Triple-Quantum-Well Heterojunction Bipolar Light-Emitting Transistor
TQW-HBT	Triple-Quantum-Well Heterojunction Bipolar Transistor
TQW-LET	Triple-Quantum-Well Light-Emitting Transistor
TSOP	Temperature-Sensitive Optical Parameter
UIUC	University of Illinois Urbana-Champaign
VCTL	Vertical Cavity Transistor Laser
VLSI	Very-Large-Scale Integration

doi:10.6342/NTU202500212

List of Symbols

Symbol	Detail
d_ℓ	Thickness of QW_ℓ
E_B	Energy Difference Between the Conduction Band Edge in the GaAs Barrier ($E_{c,b}$) and the First Sub-Band of the InGaAs QW (E_1)
E_i	Energy of the i^{th} Bound Sub-Band in the QW
F_ℓ	Electron Flux Injected from the Emitter to the Base and Associated With Q_ℓ
I_{C_1}	Collector Current of T_1 (Refer to Fig. 1.7)
I_{C_2}	Collector Current of T_2 (Refer to Fig. 1.7)
N_b	Number of Bound Sub-Bands in the QW
$n_{v,\ell}$	Virtual State Density of the QW_ℓ in the Base Region of the MQW-HBT.
$n_{v,\ell}$	Minority Carrier Density of Virtual Conduction States in QW_ℓ
Q_{QW_1}	Minority Carrier Capture by QW_1 (Refer to Fig. 3.9)
Q_{QW_2}	Minority Carrier Capture by QW_2 (Refer to Fig. 3.9)
Q_{QW_3}	Minority Carrier Capture by QW_3 (Refer to Fig. 3.9)
Q_1	Electrons Diffusing from the Emitter to QW_1 (Refer to Fig. 3.9)
Q_2	Electrons Diffusing from the Emitter to QW_2 (Refer to Fig. 3.9)

doi:10.6342/NTU202500212

Q_3	Electrons Diffusing from the Emitter to QW_3 (Refer to Fig. 3.9)
$W_{E\ell}$	Width Between the Emitter-to-QW_ℓ
$W_{\ell\ell'}$	Distance Between QW_ℓ and $QW_{\ell'}$
$\beta_{2QW-HBT}$	Current Gain of the 2QW-HBT
$\beta_{3QW-HBT}$	Current Gain of the 3QW-HBT
$\beta_{E\ell'}$	Current Gain of Fictitious HBTs with Base Width of $W_{E\ell'}$
β_{EC}	Current Gain of an HBT with Base Width W_B
$\beta_{E\ell}$	Current Gain of Fictitious HBTs with Base Width of $W_{E\ell}$
μ_e^p	Minority Carrier Mobility
$\tau_{cap,1}$	Capture Time Minority Carriers in the QW_1 (Refer to Fig. 3.9)
$\tau_{cap,3}$	Capture Time Minority Carriers in the QW_1 (Refer to Fig. 3.9)
$\tau_{cap,\ell}$	Capture Time of Minority Carriers Transitioning from Virtual Conduction States ($n_{v,\ell}$) to Bound States Within QW_ℓ
τ_{cap2}	Capture Time Minority Carriers in the QW_2 (Refer to Fig. 3.9)
$\tau_{esc,1}$	Escape Times of Electrons from QW_1 (Refer to Fig. 3.9)
$\tau_{esc,2}$	Escape Times of Electrons from QW_2 (Refer to Fig. 3.9)
$\tau_{esc,3}$	Escape Times of Electrons from QW_3 (Refer to Fig. 3.9)

doi:10.6342/NTU202500212

$\tau_{esc,\ell}$	Escape Time of Minority Carriers Leaving the Intrinsic QW_ℓ into the Doped Base
$\tau_{QW,1}$	Recombination Lifetime of Electrons in QW_1 (Refer to Fig. 3.9)
$\tau_{QW,2}$	Recombination Lifetime of Electrons in QW_2 (Refer to Fig. 3.9)
$\tau_{QW,3}$	Recombination Lifetime of Electrons in QW_3 (Refer to Fig. 3.9)
$\tau_{QW,\ell}$	Recombination Lifetime of Minority Carriers Within the QW_ℓ
$\tau_{t,E\ell}$	Transit Time of Electrons Across the Emitter-to-QW_ℓ Region of Width $W_{E\ell}$
D_n	Electron Diffusion Constant
m_e^*	Effective Electron Mass
n_v	Electron Density in the Virtual Continuum Conduction State
$n_{VS,1}$	Densities of Minority Carrier in the Virtual Conduction States of QW_1 (Refer to Fig. 3.9)
$n_{VS,2}$	Densities of Minority Carrier in the Virtual Conduction States of QW_2 (Refer to Fig. 3.9)
$n_{VS,3}$	Densities of Minority Carrier in the Virtual Conduction States of QW_3 (Refer to Fig. 3.9)
n_{QW}	Total Carrier Concentration in the QW

doi:10.6342/NTU202500212

α_t	Base Transport Factor
$\beta_{LET_1}(T)$	Current Gain of the First LET (Refer to Fig. 4.12)
$\beta_{LET_2}(T)$	Current Gain of the Second LET (Refer to Fig. 4.12)
τ_{LO}	Escape Time due to Phonon Interactions
τ_{QW}	Recombination Lifetime of Electrons in the QW
τ_b	Bulk Recombination Lifetime of Minority Carrier
τ_{cap}	Capture Time
τ_{esc}	Escape Time
$\tau_{t,EC}$	Base Transit Time
$\tau_{t,EQW}$	Transit Time of Minority Carriers Crossing the EQW Region
ΔE_V	Energy Band Discontinuity in Valence Band
A	Thermal Sensitivity Fitting Parameter
A	Device Cross-Section Area
A_0	SRH Coefficient
A_1	Area of T_1 (Refer to Fig. 1.7)
A_2	Area of T_2 (Refer to Fig. 1.7)
Au	Gold
B	Base

doi:10.6342/NTU202500212

B	linearity fitting parameter (Refer to Eq. 5.17)
B_0	Spontaneous Emission Coefficient
B_1	Base of the First LET (Refer to Fig. 4.16)
B_2	Base of the Second LET (Refer to Fig. 4.16)
C	Carbon as a Doping
C	Collector (Refer to Device Figs.)
℃	Degree Celsius
C_0	Auger Recombination Coefficient
C_1	Collector of the First LET (Refer to Fig. 4.16)
C_2	Collector of the Second LET (Refer to Fig. 4.16)
d_{total}	Total Thickness of the Staircase QW
E	Emitter
E_1	Emitter of the First LET (Refer to Fig. 4.16)
E_2	Emitter of the Second LET (Refer to Fig. 4.16)
$E_{c,w}$	QW's Lowest Conduction Band
E_F	Fermi Energy Level
$E_{F,E}$	Fermi Level Energy
$E_{V,E}$	Valence Band Energy

doi:10.6342/NTU202500212

f(E)	Distribution Function
$F_{n,1}(I)$	Carrier Flux Injected from Emitter into Region (Refer to Fig. 5.3)
$F_{n,1}(II)$	Electron Flux Injected from the Emitter to Region II (Refer to Fig. 5.3)
$F_{n,net}(QW)$	Total Carrier Flow Captured by the QW and Subsequently Escaping it
g(E)	Density of States
Ge	Germanium.
$\hbar\omega_{LO}$	LO Phonon Energy
I_B	Base Current
I_C	Collector Current
$I_{C,1}$	Collector Current of LET_1 (Refer to Fig. 4.16)
$I_{C,2}$	Collector Current of LET_2 (Refer to Fig. 4.16)
I_E	Emitter Current
I_S	Saturation Current
J_e	Injection Current Density
K	Temperature Unit in Kelvin
k or k_B	Boltzmann's Constant
L_n	Electron Diffusion Length
M_1	First Current Mirror Transistors (Refer to Fig. 1.7)

doi:10.6342/NTU202500212

M_2	Second Current Mirror Transistors (Refer to Fig. 1.7)
mA	Milli Ampere
n(E)	Carrier Concentration at Energy E
Ni	Nickel
P	Doping Concentration in the GaAs Base
$P_{E,0}$	Equilibrium Hole Density
Pt	Platinum
q	Electron Charge
Q_0	Charge in the Base (Refer to Fig. 2.1)
Q_{QW}	Charge in the QW in Fig.
Si	Silicon
T	Absolute Temperature
T(E)	Transmission Probability
T_1	First BJT (Refer to Fig. 1.7)
T_2	Second BJT (Refer to Fig. 1.7)
T_{ext}	Exact Temperature
Ti	Titanium
V	Voltage

doi:10.6342/NTU202500212

v(E)	Escape Velocity of the Carriers
V_{BC}	Base-to-Collector Voltage
V_{BE}	Base-Emitter Voltage
V_{BE}	Base-to-Emitter Voltage
V_{CE}	Collector-to-Emitter Voltage
V_{DD}	Supply Voltage
V_T	Thermal Voltage
W_B or W_{EC}	Width of the Base
β_{EC}	Current Gain of HBT with Base Width of W_{EC}
β_{EQW}	Current Gain of HBT with Base Width of W_{EQW}
β_{HBT}	Current Gain of Typical HBT
$\beta_{MQW\text{-}HBT}$	Current Gain of Typical MQW-HBT
β_{QWC}	Current Gain of HBT with Base Width of W_{QWC}
β_{QWC}	Current Gain for QWC Region
$\beta_{QW\text{-}HBT}$	Current Gain of Typical QW-HBT
$\beta_{SQW\text{-}HBT}$	Current Gain of Typical SQW-HBT
$\beta_{TQW\text{-}HBT}$	Current Gain of Typical TQW-HBT
β_{β}	Current Gain for the EC Region Without QW

doi:10.6342/NTU202500212

ΔI_B	Increment in Base Current
ΔI_C	Increment in Collector Current
ΔV_{BE}	Base-to-Emitter Voltage Difference
η	Non-Ideality Factor
ρ	Base Minority Charge Distribution
$\tau_{t,EC}$	Transit Time from Emitter to Collector
$\tau_{t,EQW}$	Transit Time from Emitter to the QW
γ	Emitter Injection Efficiency
δ	Recombination Factor at the Emitter-Base Junction
δI_C	Derivative of Collector Current

doi:10.6342/NTU202500212

APPENDIX C

Summary of Oral Defense Discussion

The oral defense of this dissertation, conducted on January 6, 2025, provided valuable feedback and insightful recommendations from the esteemed committee members. In this section, I have included the question raised, along with corresponding answers and committee suggestions. The discussion is detailed below:

i. Are any potential difficulties in growing a triple quantum well (TQW) structure compared to a single quantum well (SQW) structure in the light-emitting transistor (LET) design.

Response: Growing a TQW structure in the LET design is more challenging than a SQW structure due to the increased precision required for the narrower and more complex QW dimensions. Each layer's thickness and material composition must be meticulously controlled to achieve the desired optical and electronic properties, as even minor deviations can significantly affect the LET's performance.

In this research, the layer structures were designed at the IOED Lab at NTU and grown with the support of a collaborating industrial partner. The industry demonstrated high proficiency in achieving precise layer thickness and material

doi:10.6342/NTU202500212

composition, ensuring high-quality TQW structures. However, if the TQW structure were grown in-house at NTU, additional effort and expertise would be necessary to achieve the same level of precision. The facilities and expertise available in the collaborating industry play a critical role in maintaining the required accuracy for TQW growth.

Committee Suggestions:

The committee suggested consulting with NTU professors or experts specializing in QW growth and epitaxial techniques to ensure high-quality TQW structures. Such collaboration would address potential challenges and improve the efficiency of the growth process. Incorporating these recommendations could enhance future efforts to grow TQW structures in-house, leading to further advancements in LET development for smart thermal sensing technologies.

ii. The nonlinearity in the Darlington transistor arises from which factor?

Response: The electron escape from the QW exhibits a nonlinear behavior with temperature, and this contributes to the nonlinearity in the Darlington transistor. Additionally, the nonlinearity may arise from the circuit design or the epitaxial layer (epi-layer) structure. In the future, efforts should focus on minimizing the

doi:10.6342/NTU202500212

nonlinearity through optimized epi-layer design, circuit design, or by adjusting QW parameters, such as the width.

Committee Suggestions: The committee noted that the nonlinearity primarily arises from the circuit design of the Darlington transistor and not solely from the nonlinear electron escape from the QW. This is evident in Fig. 4.13, where the current gain of the LET is linear, while the current gain of the Darlington transistor is nonlinear. The nonlinearity may be attributed to the $\beta_{LET_1} * \beta_{LET_2}$ term in Eq. 4.1. The committee recommended further optimization of the Darlington pair circuit and epi-layer design to address this issue.

iii. Do you have any experimental data that varies the QW position in the base?

Response: In this dissertation, the experimental results are for a fixed position of the QW in the base of the transistor. For varying the QW position in the base, only simulation data are discussed in Chapter 3. In the future, experimental studies on the effect of QW position on the device characteristics will also be conducted.

iv. What happens if the QW is not present in the base of the transistor at high temperatures?

doi:10.6342/NTU202500212

Response: In this case, the transistor simply becomes a typical HBT structure. For such a structure, the current gain remains almost constant or slightly decreases with temperature in the HBT-based layer structure.

v. Is constant current or increasing current with temperature required for thermal sensor design?

Response: In traditional BJT-based front-end designs, the current gain is almost constant with temperature. However, BJT-based bandgap circuits provide a voltage-to-temperature signal based on changes in the base-to-emitter voltage (ΔV_{BE}). In the case of LETs, the design is current-sensitive. By using passive elements like resistors, the current sensitivity can be converted into voltage sensitivity. Therefore, LETs have the potential to use as a promising front-end design component for future temperature sensing applications.

vi. How QW recombination time is depends on the base current?

Response: The QW recombination time is influenced by the base current because the base current determines the injection of carriers into the QW region, which governs the recombination processes. As the base current increases, more carriers are injected into the QW, resulting in a higher carrier density. The recombination time, τ_{QW} is

doi:10.6342/NTU202500212

inversely proportional to the carrier density, meaning that a higher base current leads to a shorter recombination time. Radiative recombination in the QW follows the relationship $R_{rad}=B.n^2$, where B is the radiative recombination coefficient and n is the carrier density. Therefore, an increased base current enhances the radiative recombination rate, reducing τ_{QW}.

vii. Is there any benchmark or figure of merit (FOM) for current thermal sensors, and why do we use this device for thermal sensing?

Response: The LET was initially developed as a light-emitting device. However, when measured at different temperatures, it exhibited a unique thermal response in its current gain, which is opposite to the typical behavior of HBT devices. This device shows ultra-high current sensitivity. However, traditional front-end components of thermal sensors are defined based on voltage sensitivity for thermal sensing applications. To make a comparison, we designed a Darlington transistor using passive elements, such as resistors, to convert the current sensitivity of the LET into voltage sensitivity. We then compared this with existing technologies (Table 4.3). Despite this effort, it is still challenging to make direct comparisons due to differences in circuit design and operational conditions. The LET is a novel device, and in the future, it can be integrated with ADC circuits to study key FOM

doi:10.6342/NTU202500212

parameters, including resolution, error rate, accuracy, temperature sensitivity, and stability.

viii. For transistor-based thermal sensors, the device is always on, resulting in constant power consumption. Have you considered the self-heating problem?

Response: Yes, the issue of self-heating and its impact on junction temperature has been considered. In the context of our ambient temperature measurement setups, we have focused on the influence of substrate temperature on the device. Since our measurements are conducted under ambient conditions, the junction temperature is naturally elevated.

Additionally, in our TCAD simulations, we have incorporated a comprehensive thermal model to account for the effects of self-heating. By setting various substrate temperatures and applying different bias conditions, we have been able to calculate the heat effects that impact the junction temperature and, in turn, influence quantum-well thermionic emission. Our research is specifically tailored to studying how substrate temperature changes affect electron behavior in the quantum well and its impact on thermionic emission.

doi:10.6342/NTU202500212

ix. Noise in the Darlington transistor is also amplified, and it ultimately affects the thermal sensor. How can this problem be solved?

Response: The issue of noise amplification in the Darlington transistor is indeed a challenge, as it can adversely impact the performance of the thermal sensor. One approach to address this problem is to carefully optimize the circuit design to minimize noise contribution. For example, choosing appropriate passive components, such as low-noise resistors, and ensuring proper impedance matching can reduce noise levels.

Additionally, the use of feedback mechanisms in the bandgap circuit front-end design can help suppress noise amplification. Implementing low-pass filters or active filtering techniques can further attenuate high-frequency noise components.

On the device side, reducing thermal noise by carefully engineering the epitaxial layer structure, such as minimizing defects in the quantum wells or using materials with lower noise characteristics, can also contribute to noise reduction.

Finally, integrating advanced signal processing techniques, such as digital noise cancellation or averaging multiple measurements, can enhance the overall signal-to-noise ratio (SNR) in the thermal sensor system. In the future study, combining these

doi:10.6342/NTU202500212

approaches can significantly mitigate the noise amplification issue in the Darlington transistor and improve the thermal sensor's performance.

Committee Suggestions: Study the noise in LETs, as it is necessary for designing an efficient thermal sensor.

x. What is the conversion time? You mentioned that the device takes 2 minutes to give the response, which is too long for a thermal sensor. You should study the conversion time.

Response: Regarding the conversion time, our current laboratory setup does not allow for the precise estimation of conversion or response time for our device. However, we acknowledge the importance of such measurements and plan to explore methodologies for assessing response time in future studies. While it currently takes 2 minutes to complete these measurements, we believe the device itself has a fast response time due to the thermionic emission mechanism. We are confident that the conversion time is likely to be fast, but further studies are needed to confirm this.

doi:10.6342/NTU202500212

xi. Why should your device be measured at 25 ℃? If your device heats up, for example, to 40℃ and you suddenly measure it at 0℃, would there be any issues caused by self-heating?

Response: We selected the temperature range from 25℃ to 85℃ based on its relevance to real-world applications where temperature sensing is critical. This range enables us to evaluate the device's performance under typical operating conditions. While we acknowledge the importance of exploring performance at lower and higher temperatures, we appreciate the committee's suggestion to extend the temperature range in future studies.

If the device heats up to, for example, 40℃ and is then suddenly measured at 0℃, self-heating could present challenges. A rapid temperature shift may cause transient thermal effects, where the junction temperature does not immediately stabilize, potentially affecting the accuracy of the measurement.

Self-heating could also affect device, and the thermal dynamics during such a sudden change could temporarily impact quantum-well thermionic emission and other temperature-dependent properties. To mitigate these issues, it is essential to account

doi:10.6342/NTU202500212

for thermal time constants and allow the device sufficient time to stabilize at the new temperature before conducting measurements.

In future studies, we plan to thoroughly investigate transient thermal behavior and self-heating effects. This will enable us to better understand how rapid temperature changes influence device performance and ensure reliable operation under diverse conditions.

xii. How many devices have you fabricated? Do you observe consistent results from the same devices?

Response: For each SQW- and TQW-HBT, we have fabricated 12 devices with different emitter mesa sizes, including: 80 μm x 80 μm, 60 μm x 60 μm, 50 μm x 50 μm, 40 μm x 40 μm, 30 μm x 30 μm, 20 μm x 20 μm, and 10 μm x 10 μm. Yes, we have characterized all the devices, and they exhibit almost identical device characteristics.

xiii. You need to perform 1-point or 2-point calibration because, for instance, if your device is fabricated and measured on another day in a different environment, variations might occur.

doi:10.6342/NTU202500212

Response: Thank you for the committee's suggestion. We will include such studies in future research. However, we have measured this device over an extended period with repeated measurements conducted on different days. The results consistently show similar characteristics, indicating reliable performance under varying conditions.

xiv. How can you integrate with an ADC circuit that is based on CMOS technology?

Response: We can apply the same QW technique and design a new layer structure for a Si-Ge substrate. Ultimately, we plan to use the results from this new device as a component to integrate with the ADC circuit in future work.

xv. What are the bias conditions for voltage sensitivity in the Darlington transistor?

Response: The bias conditions for this thermal sensitivity, as mentioned in this dissertation, are a V_{DD} of 4 V and a I_B of 1 mA.

xvi. Will your device perform well for a higher temperature range, or only within the 25℃ to 85℃ range? At higher temperatures, self-heating problems may occur, affecting the thermal sensor.

doi:10.6342/NTU202500212

Response: We have measured the device under ambient temperature conditions, and it performs well in terms of thermal sensitivity within this temperature range. Thank you to the committee for suggesting the study of the device's behavior at higher and lower temperature ranges in the future. While self-heating could be a potential issue at higher temperatures, we have conducted measurements at ambient conditions, and we can address the self-heating problem in the front-end design before sending the signal to the ADC in the future study.

xvii. Are the quantum wells (QWs) in the TQW structure the same width or different? How do you decide the width of the QW?

Response: The QW widths in the TQW structure are the same. The width size is 70 Å. TCAD was used to design the TQW-HBT layer structure.

xviii. If your QWs are equal, and you consider the width of the SQW to be the same as the total width of the TQW, how would this affect the linearity and sensitivity of your device?

Response: If the SQW is designed with a width equal to the total width of the TQW, it would be more difficult for electrons to escape quickly due to the larger QW width. Electrons would accumulate at the bottom of the QW. Additionally, the sub-band

doi:10.6342/NTU202500212

energy levels of each QW in the TQW structure differ due to the unique design of the TQW-HBT layer. This difference could be influenced by strain in the TQW from the surrounding layers or barriers, which may affect the current sensitivity of the device. The sensitivity of the TQW structure is higher compared to a single QW with the same total width as the TQW. Thank you to the committee for the suggestion to study linearity and sensitivity further in future research.

xix. Can you provide a final comparison of the sensitivity for all your devices?

Response: The sensitivity of our devices is summarized below:

Device	Temperature	Biased Condition	Current Sensitivity	Voltage Sensitivity
SQW-HBT (Chapter-2)	25℃ to 85℃	V_{CE}= 2 V & I_B=0.2 mA	4.82 μA/℃	X
TQW-HBT (Chapter-3)	25℃ to 85℃	V_{CE}= 2 V & I_B=1 mA	7 μA/℃	X
LET in Darlington (Chapter-4)	25℃ to 85℃	V_{CE}= 4 V & I_B=1 mA	8.53 μA/℃	X
Darlington (Chapter-4)	25℃ to 85℃	V_{DD}= 4 V & I_B=1 mA	26.2 μA/℃	9.12 mV/℃
QW-HBT (d=90 Å) (Chapter-5)	100℃	V_{CE}= 2 V & I_B=5 mA	1.35 mA/℃	X

doi:10.6342/NTU202500212

xx. In Fig. 5.9, why does the sensitivity increase and then decrease?

Response: This behavior is due to the width of the QW. For a particular QW width, energy is stored at the sub-band energy levels. As the temperature increases, the electron energy reaches a certain level where it can either saturate or cause electrons to be depleted more quickly. This results in a decrease in sensitivity at higher temperatures.

xxi. Escape time, capture time, and QW recombination time — which time is fitted and which one is calculated? What are the values of $\hbar\omega_{\mathrm{LO}}$ and τ_{LO}? In Eq. 2.27, when comparing the two terms, which one dominates?

Response: In Eq. 2.27, the first term of RSH is calculated with the help of TCAD, while the second term of RSH is calculated using the values $\hbar\omega_{\mathrm{LO}}=34\times10^{-3}$ eV and $\tau_{\mathrm{LO}}=120\times10^{-12}$ s. The capture time and QW recombination time are determined by fitting the experimental data. When comparing the two terms of RSH in Eq. 2.27 at T=300K for the I_B = 0.2 mA, the first term is 1.88423 ns, and the second term is 0.32705 ns. This indicates that the thermionic emission term is dominates.

xxii. In Fig. 2.14, can you change the squared QW figure to a staircase-QW?

doi:10.6342/NTU202500212

Response: As per the committee's suggestion, Fig. 2.14 has been updated to a staircase-QW in the final dissertation.

xxiii. What happens if the barrier width is low in the TQW-HBT layer structure? Have you studied the wave function and QW levels of the TQW structure?

Response: If the QW barrier width is low, there is a possibility that the TQWs may couple and behave like a single QW. In future studies, we plan to calculate the wave function using TCAD simulations. For the sub-band energy levels, this dissertation utilized TCAD to calculate the sub-band energy for each QW in the TQW layer. Using these sub-band energy levels, we subsequently calculated the electron escape time at different base currents and temperatures.

xxiv. Can you clearly define the collector-emitter voltage for the LET and the Darlington transistor in Fig. 4.11, Fig. 4.12, and Fig. 4.16?

Response: After carefully considering the committee's suggestion, the collector-emitter voltage for the LET is defined as $V_{C_1E_1}$, and the collector-emitter voltage for the Darlington transistor is defined as V_{CE_2}. These have been clearly indicated in Fig. 4.16.

In addition, the following changes were made:

doi:10.6342/NTU202500212

- In Fig. 4.13, V_{CE}=4 V has been updated to $V_{C_1E_1}$=V_{CE_2}=4 V.
- In Fig. 4.14, V_{CE}=4 V has been updated to $V_{C_1E_1}$=4 V.
- In Fig. 4.15, V_{CE}=4 V has been updated to V_{CE_2}=4 V.

These changes ensure consistency and clarity in the representation of the collector-emitter voltage for the LET and Darlington transistor.

I would like to express my heartfelt gratitude to the members of my Ph.D. defense committee for their invaluable suggestions and insightful feedback. Their guidance has been instrumental in improving my research and enhancing the quality of my oral defense. I deeply appreciate their time, effort, and unwavering support throughout this process.

doi:10.6342/NTU202500212

APPENDIX D

學位論文學術倫理暨原創性聲明書

turnitin

Digital Receipt

This receipt acknowledges that Turnitin received your paper. Below you will find the receipt information regarding your submission.

The first page of your submissions is displayed below.

Submission author:	薩莫古 薩莫古
Assignment title:	學位論文原創性檢查01
Submission title:	PhD Thesis_Mukul Kumar_D09941011_Design and Fabricatio...
File name:	Thesis_Mukul_Kumar_D09941011.pdf
File size:	9.71M
Page count:	278
Word count:	49,434
Character count:	269,589
Submission date:	20-Jan-2025 11:37AM (UTC+0800)
Submission ID:	2567367755

國立臺灣大學電機資訊學院光電工程學研究所

博士論文

Graduate Institute of Photonics and Optoelectronics

College of Electrical Engineering and Computer Science

National Taiwan University

Doctoral Dissertation

超高靈敏度熱感測光伴之設計與製造：基於發光電晶體於智慧科技應用

Design and Fabrication of Ultra-High Sensitivity Thermal Sensing Devices Using Light-Emitting Transistors for Smart Technologies

薩莫古

Mukul Kumar

指導教授：吳肇欣 博士

Advisor: Prof. Chao-Hsin Wu, Ph.D.

中華民國 114 年 1 月

January, 2025

doi:10.6342/NTU202500212

PhD Thesis_Mukul Kumar_D09941011_Design and Fabrication of Ultra-High Sensitivity Thermal Sensing Devices Using Light-Emitting Transistors for Smart Technologies.pdf

ORIGINALITY REPORT

16%	1%	16%	0%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	Mukul Kumar, Shu-Jui Hsu, Shu-Yun Ho, Shu-Wei Chang, Chao-Hsin Wu. "Current Gain Enhancement of Heterojunction Bipolar Light-Emitting Transistors Using Staircase InGaAs Quantum Well", IEEE Transactions on Electron Devices, 2023 Publication	6%
2	Mukul Kumar, Shu-Yun Ho, Shu-Jui Hsu, Pin-Chia Li, Shu-Wei Chang, Chao-Hsin Wu. "Current Gain Enhancement at High-Temperature Operation of Triple-Quantum-Well Heterojunction Bipolar Light-Emitting Transistor for Smart Thermal Sensor Application", IEEE Transactions on Electron Devices, 2023 Publication	5%
3	Mukul Kumar, Lu-Ching Hsueh, Sheng-Wen Cheng, Shu-Wei Chang, Chao-Hsin Wu. "Analytical Modeling of Current Gain in Multiple-Quantum-Well Heterojunction	4%

doi:10.6342/NTU202500212

Bipolar Light-Emitting Transistors", IEEE Transactions on Electron Devices, 2024
Publication

4	Yun-Hsuan Chang, Yung-Lin Chou, Shu-Wei Chang, Chao-Hsin Wu. "Thermally-enhanced current gain of quantum-well heterojunction bipolar transistor", Journal of Applied Physics, 2019 Publication	1%

Exclude quotes	On	Exclude matches	< 1%
Exclude bibliography	On		

doi:10.6342/NTU202500212

國立臺灣大學光電工程學研究所
學位論文學術倫理暨原創性聲明書

1. 本人已經自我檢核，確認無違反學術倫理情事，論文倘有造假、變造、抄襲、由他人代寫，或涉其他一切有違著作權及學術倫理之情事，及衍生相關民、刑事責任，概由本人負責，概無異議。
2. 本人之學位論文已確實經本校論文內容相似度比對系統檢核，內容比對相似度為 16 %。

附比對分析結果，並確認如下：

☐ 比對相似度<10%。

☐ 比對相似度≧10%：

☐ 單項≦2%。

☑ 單項≧3%，共有 3 筆。均為本人參與之研究計畫或列名參與之報告、投稿之論文，於比對報告後另檢附單頁說明，並由本人及指導教授簽名確認。

☐ 單項≧3%，共有___筆。於比對報告上被標示處逐項說明，並由本人及指導教授簽名確認。

聲明人：Mukul Kumar Mukul Kumar

學號：D09941011

中華民國 114 年 01 月 20 日

指導教授簽章：

共同指導教授簽章（無免）：

系所（學位學程）主管簽章：

備註：110 學年度第 2 學期起研究生應於繳交學位論文前完成論文相似度比對作業，並將本聲明書送交指導教授及系、所、學位學程主管簽章，本聲明書正本由各系、所、學位學程留存備查。

(113.01)

doi:10.6342/NTU202500212

APPENDIX E

About the Author

Mukul Kumar was born in Muzaffarpur, Bihar, India, and is a flexible dedicated researcher, continually devoted to exploring semiconductor device physics and utilizing for future innovations.

Mr. Kumar has a strong academic background; he earned a Master of Technology in Electronics and Communication Engineering from the Indian Institute of Technology (IIT) Dhanbad, India, in 2019, and a Bachelor of Technology in Electronics and Communication Engineering from Jaypee University of Engineering & Technology (JUET), Guna, India, in 2015. Currently, Mr. Kumar is working towards a Ph.D. degree at the Graduate Institute of Photonics and Optoelectronics, National Taiwan University (NTU), Taipei, Taiwan.

His current research interests include light-emitting transistors (LETs), transistor lasers (TLs), heterojunction bipolar transistors (HBTs), high-speed integrated circuits, and semiconductor device characterization and simulation. Mr. Kumar is developing a smart thermal sensor circuit using LETs. His research focuses on the unique properties

doi:10.6342/NTU202500212

of LETs, which exhibit increased current gain with temperature—a characteristic that could revolutionize thermal sensor technology. Recently, Mr. Kumar achieved a groundbreaking milestone in optoelectronics semiconductor technology: the successful design and fabrication of the world's first Darlington transistor using LETs. This pioneering research was recently published in the esteemed IEEE Electron Device Letters (IEEE-EDL).

An active member of professional societies such as IEEE, IEEE Electron Device Society, and OPTICA, Mukul has published extensively in high-impact journals and presented his research at international conferences such as DRC, CSW, CLEO, and CLEO-Pacific Rim. Mr. Kumar is the first author of 6 peer-reviewed journals and author and co-author of 14 conference papers. His work has been recognized with numerous awards, including the EECS College International Scholarship 2024, NTU Outstanding International Graduate Student Scholarship 2023-2024, the Best Poster Award at the 2023 International Electron Devices and Materials Symposium in Taiwan, the National Taiwan University International Graduate Student Scholarship 2020-2023, and multiple academic scholarships for his exceptional performance. Mr. Kumar also actively participates in Taiwan's National Science and Technology Council research projects and received grants that facilitated his presentation of research at the

doi:10.6342/NTU202500212

prestigious international conference “Compound Semiconductor Week (CSW) 2023” in South Korea and “82nd Device Research Conference (DRC) 2024” in the USA .

Driven by a passion for semiconductor technology and III-V compound semiconductors, Mr. Kumar is committed to contributing to the advancement of smart civilizations through his research. His dedication to academic excellence and his relentless pursuit of innovation in semiconductor technology make him a prominent figure in his field, motivating and inspiring the next generation of engineers and scientists.

doi:10.6342/NTU202500212