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Master's Thesis

應用於控制量子位元之低溫 CMOS 類比前端電路

Design of Cryo-CMOS Analog Front-End Circuits for Qubit Control

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本論文係 賴耀承 R10943126 在國立臺灣大學電子工程學研究所完成之碩士學位論文，於民國 114 年 3 月 3 日承下列考試委員審查通過及口試及格，特此證明。

The undersigned, appointed by the Graduate Institute of Electronics Engineering on 3 March 2025 have examined a Master's Thesis entitled above presented by Yao-Chen Lai (R10943126) candidate and hereby certify that it is worthy of acceptance.

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To My Dear Family

謹獻給我的家人

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摘要

本論文提出一個應用於控制量子位元的類比前端控制電路之設計與實現，該電路採用台積電 40 奈米 CMOS 製程進行製作。此前端電路包含超源極跟隨器架構濾波器與可變增益放大器，目標為在低溫環境下達成高保真度、低功耗及寬頻操作的性能要求。

基於超源極跟隨器架構之濾波器實現一個二階低通轉換函數，其-3 dB 頻寬達到 400 MHz，同時在 1 V 電源下保持 42.8 dB 的信噪比與-50.4 dB 的總諧波失真，同時功耗僅為 0.057 毫瓦特。該濾波器的擬差動架構消除了對共模回授電路的需求，提升了功率效率與線性度。

可變增益放大器採用自補償電晶體與主動電感進行頻寬延展，實現了 35.4 dB 的增益調變範圍，並可操作至 1 GHz。設計展現出精確的 dB 線性特性，同時功耗僅為 0.438 毫瓦特。

實驗驗證部分，晶片透過鍵合線連接至自行設計的印刷電路板進行量測，所使用的儀器包括示波器、信號產生器與頻譜分析儀等。晶片實拍顯示，總面積為 1.109 × 1.011 mm²，核心電路面積為 0.046 mm²。量測結果證實，所提出之設計達到了量子信號控制所需的嚴格性能要求，具備高保真度、寬頻操作及低功耗等特性。

關鍵字：控制量子位元、基於超源極跟隨器的濾波器、可變增益放大器、自補償電晶體、主動式電感

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Abstract

This thesis presents the design and implementation of an analog front-end control circuit for qubit control, fabricated using TSMC 40-nm CMOS technology. The front-end includes a Super-Source-Follower (SSF)-based filter and a Variable Gain Amplifier (VGA), targeting high fidelity, low power, and wide bandwidth operation in cryogenic environments.

The SSF-based filter achieves a second-order low-pass transfer function , achieving a -3 dB bandwidth of 400 MHz. Under a 1 V power supply, it maintains a signal-to-noise ratio (SNR) of 42.8 dB and a total harmonic distortion (THD) of -50.4 dB, while power consuming only 0.057 mW. Its pseudo-differential architecture eliminates the need for a common-mode feedback circuit, improving power efficiency and linearity.

The VGA, designed with self-compensated transistors and active inductors for bandwidth extension, provides a gain variation range of 35.4 dB and operates up to 1 GHz. The design demonstrates precise dB-linear characteristics while consuming 0.438 mW.

Experimental validation was performed with the chip bonded to a custom-designed PCB, using measurement instruments such as oscilloscopes, signal generators, and spectrum analyzers. The die photo shows a total area of 1.109 × 1.011 mm², with a core circuit area of 0.046 mm². Measurement results confirm that the proposed design meets the stringent requirements for quantum signal control, achieving high fidelity, wide bandwidth, and low power consumption.

Keywords: Qubit Control, Super-Source-Follower (SSF)-Based Filter, Variable Gain Amplifier (VGA), Self-Compensated Transistors, Active Inductors

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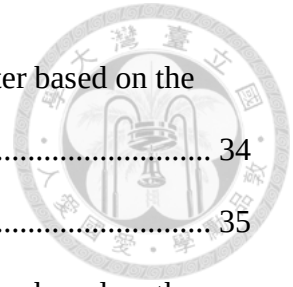

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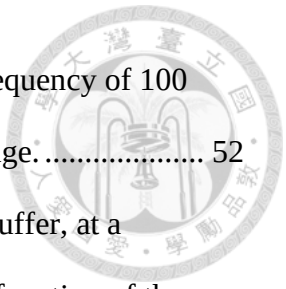

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Chapter 1 Introduction

1.1 Background and Motivation

In recent years, research on quantum signal control circuits has been progressing rapidly, particularly in the field of quantum computers. As the performance and number of qubits increase, the demand for precise and high-performance quantum signal control circuits is becoming increasingly significant.

Quantum computers demonstrate significant advantages over classical computers in addressing a wide range of computational problems. Quantum computing holds the potential to revolutionize various fields by providing exponential speedups for problems that are classically intractable. As depicted in Fig. 1-1, quantum computing presents broad application prospects in key fields such as quantum chemistry, optimization problems, and cryptography. In quantum chemistry, quantum computers can simulate molecular interactions that are beyond the capability of traditional computers. Optimization problems, critical in logistics and operations, benefit from quantum computing speedups by finding optimal solutions in complex systems. In the field of cryptography, quantum algorithms have the potential to break traditional encryption methods, which drives the demand for quantum resistant encryption standards.

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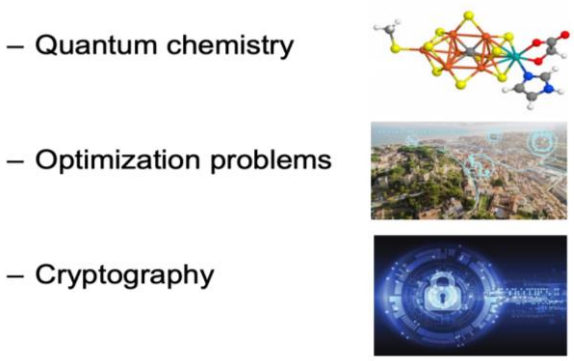

Fig. 1-1 Exponential speed up for classically intractable problem [1].

Fig. 1-2 illustrates a key challenge in scaling quantum computers beyond 100 qubits—the complexity of cabling. As controllers potentially scale to millions of qubits, the current approaches to cabling and signal control become impractical. The dense interconnections between qubits and control systems lead to increased thermal load and space constraints, significantly hindering system scalability. To overcome these challenges, new architectures and technologies must be developed, such as integrated control systems or advanced multiplexing techniques, to reduce the physical space requirement and maintain operational efficiency in larger-scale qubit control systems.

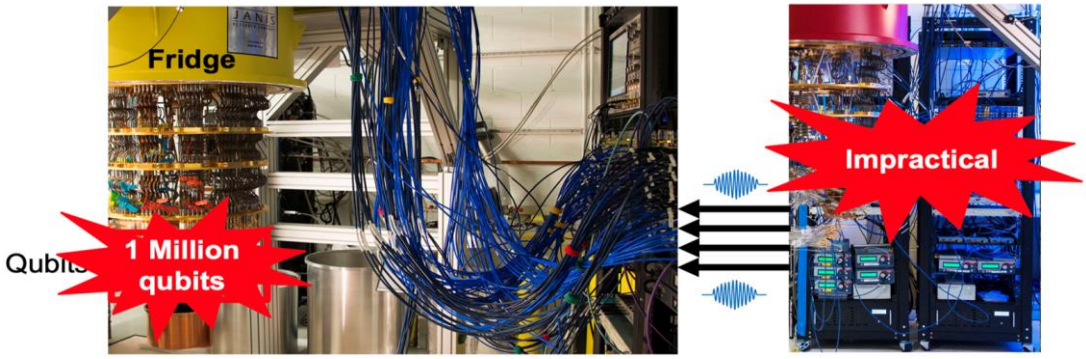

Fig. 1-2 Scalability: cabling becoming impractical [2].

As depicted in Fig. 1-3, the diagram compares state-of-the-art, proposed, and future quantum computing architectures between temperature stages: 300 K, 3 K, and 20 mK. The existing architecture requires extensive cabling across temperature levels, leading to

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inefficiencies. The proposed design of the architecture reduces complexity by optimizing components, placing control electronics at the 3 K stage. The future architecture aims to integrate all controllers and digital-to-analog converters (DACs) into a single die or package at cryogenic temperatures, minimizing wiring and enhancing the scalability of large-scale quantum controllers. This technological evolution is crucial for improving the efficiency and scalability of quantum control systems.

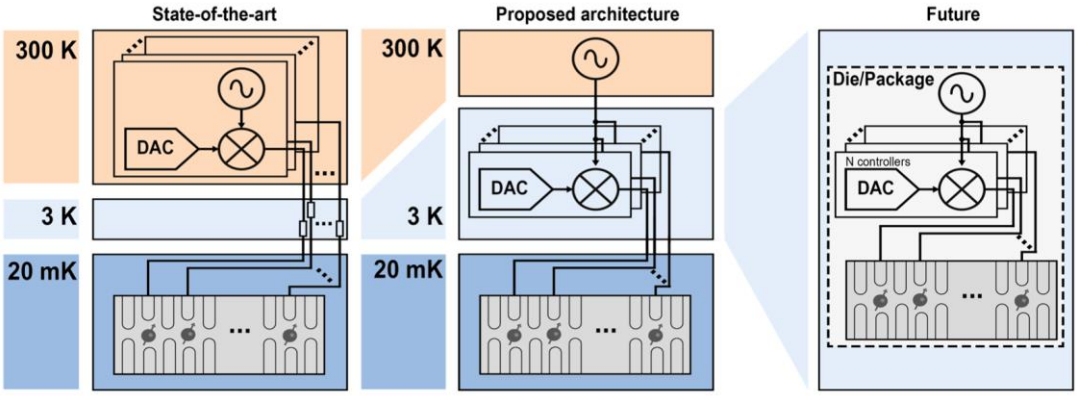

Fig. 1-3 Towards a scalable quantum computer [1].

1.2 Thesis Overview

This thesis is composed of five chapters, and the following text presents the structure of this work. Chapter 2 provides a brief introduction to the analog front-end control circuits, including traditional filters and variable gain amplifiers, discussing their performance in terms of bandwidth, power consumption, gain and noise. Additionally, various related state-of-the-art techniques are also thoroughly discussed.

Moving on to Chapter 3, a detailed analysis of the analog front-end circuit design, including filters and variable gain amplifiers, is presented, covering their operational principles, design considerations, layout techniques, and simulation results. Chapter 4 discusses the measurement results of the analog front-end circuits, including the die photo,

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measurement environment setup, Printed Circuit Board (PCB), and a discussion of the measurement results.

Finally, Chapter 5 provides a summary of the main findings of this thesis and outlines potential avenues for future research.

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Chapter 2 Fundamental of the Analog Front-End Control Circuit

This chapter primarily introduces the basic architecture of the qubit control signal generation system and the functions of its constituent modules. The system comprises digital-to-analog converters (DACs), filters, variable gain amplifiers (VGAs), a local oscillator driver (LO driver), a mixer, and a demultiplexer (DEMUX), which work together to generate precise control signals suitable for quantum computing operations. This chapter provides a detailed examination of the existing circuit architectures for the filter and VGA block diagrams, focusing on their operational principles and design considerations. The filter is used to eliminate unwanted frequency components, ensuring signal purity and stability, while the VGA adjusts signal amplitude to provide flexible gain control, further enhancing the precision of qubit operations, thereby supporting efficient quantum computation.

2.1 Basic Cryo-CMOS System of Qubits Control

Fig. 2-1 illustrates a typical qubit control signal generation system, primarily designed to provide precise control signals for quantum computer operations. The operation of quantum computers demands exceptionally high signal fidelity to guarantee precise qubit state transitions and accurate logic operations. The architecture depicted in the figure comprises digital-to-analog converters (DACs), filters, variable gain amplifiers (VGAs), a local oscillator (LO) driver, mixers, a demultiplexer (DEMUX), and output filtering and amplification modules.

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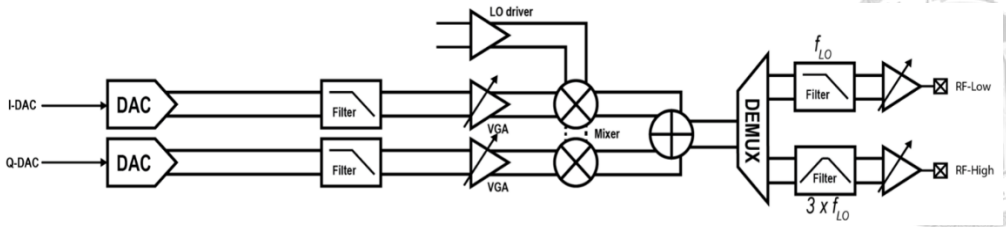

Fig. 2-1 Architecture of a circuit system for controlling qubits [1].

Initially, the system employs I-DAC and Q-DAC to generate the I and Q signal channels, respectively, which are combined to form a complex signal of the form I + jQ, where j represents the imaginary unit. This is a commonly used digital-to-analog conversion technique in quantum computing for in-phase (I) and quadrature-phase (Q) signals. These two signal channels convey the amplitude and phase information of the quantum signal, and their combination is used to precisely control the state of the qubits. The role of the DACs is to convert digital signals into continuous analog signals, facilitating subsequent control of the qubits.

Following the digital-to-analog conversion, the signal passes through a filtering module to remove unwanted frequency components, thereby ensuring signal quality and enhancing system stability. The selection and design of the filter are crucial, as improper filtering can introduce additional noise or distortion, which may propagate into subsequent amplification and mixing stages. The filter used here effectively eliminates high-frequency noise and harmonic distortion, ensuring high-quality signal transmission throughout each stage of the system.

After filtering, the signal is fed into a variable gain amplifier (VGA) to further adjust the signal amplitude. The variable gain characteristic of the VGA provides the system with flexibility, allowing fine-tuning of the sampled signal according to different operational conditions to ensure system stability and precision. In a qubit control system, different qubits may require varying control signals, and the VGA allows for precise

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adjustment of the signal amplitude to meet the specific needs of each qubit, achieving optimal control. Consequently, the performance and adjustment capabilities of the VGA directly impact the precision of the entire quantum control system.

The signal amplified by the VGA is then fed into the mixer block, where it is combined with the signal from the local oscillator (LO). The LO driver provides a stable LO signal, which serves as the foundation for frequency conversion. The mixer achieves frequency conversion by multiplying the amplified signal with the LO signal. The primary purpose of this frequency conversion is to up-convert the signal to the specific frequency required for qubit operations, ensuring compatibility with qubit control requirements. This step is crucial for the precise manipulation of qubit states, as qubit operations require microwave signals at specific frequencies. On the other hand, frequency conversion is also used to down-convert signals to a desired frequency, enabling easier decoding and analysis of qubit state readout.

Following the mixing stage, the signal passes through a demultiplexer (DEMUX) to separate different frequency bands, resulting in low-frequency (RF-Low) and high-frequency (RF-High) outputs. The DEMUX effectively separates signals of different frequencies, enabling the system to provide appropriate output signals for various application scenarios. This design significantly enhances the flexibility of the overall control system, allowing it to accommodate the synchronous control requirements of multiple qubits while helping to minimize interference and noise.

The final output signal undergoes additional filtering to ensure frequency purity. These filters are specifically designed to eliminate higher-order harmonics generated during the mixing process, thereby maintaining the frequency purity of the low-frequency (RF-Low) and high-frequency (RF-High) outputs. After filtering, the signal is passed

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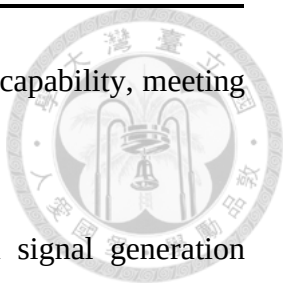

through a final power amplification block to provide sufficient drive capability, meeting the operational requirements for qubit manipulation.

In conclusion, this system represents a typical qubit control signal generation architecture, with its primary advantage being the coordinated operation among multiple blocks. The system generates control signals suitable for quantum computing through a sequence of steps including digital-to-analog conversion, filtering, amplification, mixing, and multi-band selection. These control signals require exceptionally high frequency and phase stability to ensure precise qubit manipulation, thereby enabling efficient quantum computation. In future large-scale quantum computing applications, the optimization and advancement of such signal control systems will be crucial for improving the scalability and performance of quantum computers.

2.2 Fundamentals of the Filter

Analog filters are fundamental components in various systems, including communication systems, sensor interfaces, automotive electronics, security systems, data acquisition systems, and high-energy physics experiments. Their primary functions include adjusting the bandwidth of input signals and suppressing out-of-band noise and interference during signal processing. Moreover, in mixed-signal systems, where analog-to-digital converters (ADCs) are inherently necessary, analog filters are essential for anti-aliasing and signal conditioning. These filters are placed ahead of the ADC to maintain signal integrity and ensure high-quality signal conversion.

Research in microelectronics is increasingly steering toward solutions centered on digital integrated circuits and systems, wherein the power resources assigned to the analog front-end is continually decreasing [3]. However, the specifications for the analog front-end regarding the Signal-to-Noise Ratio (SNR) remain quite stringent. This

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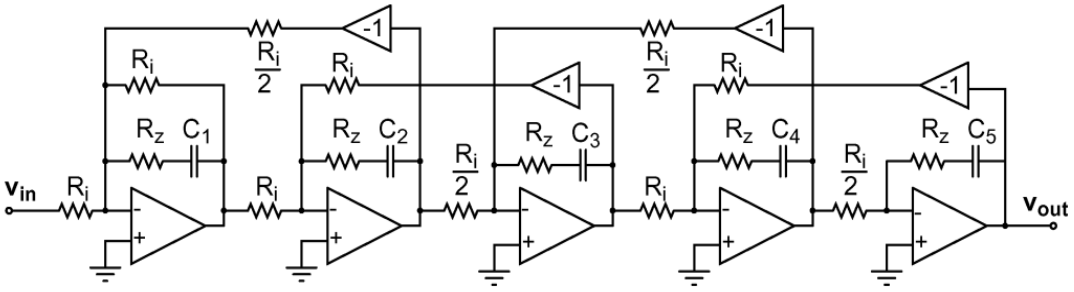
necessitates achieving a larger dynamic range in environments with minimal in-band noise [4].

Active-RC closed-loop architectures (as depicted in Fig. 2-2) are extensively applied in many telecommunications and sensor systems due to their ability to provide high linearity and ensure the reliability of circuit designs [5]. However, these circuits require the incorporation of resistors and high-bandwidth operational amplifiers, which leads to elevated in-band noise and higher power consumption.



R_i=1666.67 Ω, R_z=145 Ω, C_1=339.76 fF, C_2=919.3 fF, C_3=634.51 fF, C_4=1012.5 fF, C_5=530.05 fF

Fig. 2-2 The single-ended schematic of the active-RC filter, with component values set for the highest bandwidth condition [5].

As depicted in Fig. 2-3, the gm-RC filter is an important fundamental component in analog filter design [6]. Owing to its intrinsic open-loop configuration, this type of filter requires a lower power budget and demonstrates a low power spectral density for in-band noise. However, it also faces challenges such as inaccuracies in the transfer function and distortion within the in-band signal. An increased overdrive voltage is commonly utilized to enhance linearity; however, this approach limits the available voltage headroom for accommodating signal swing, thereby diminishing the signal-to-noise ratio (SNR).

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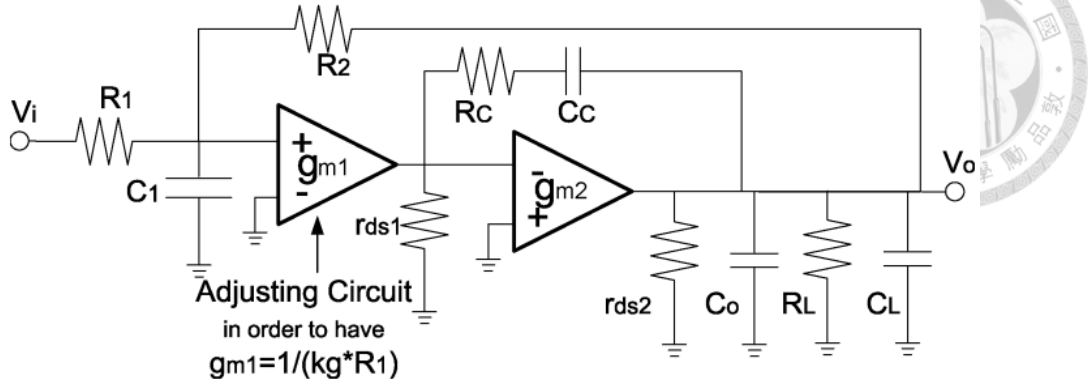

Fig. 2-3 Architecture of the Gm-RC cell [6].

As a result, research activities have focused on developing innovative analog filter circuit architectures to enhance signal processing quality within defined limitations of supply voltage and power consumption. Typically, a Figure-of-Merit (FoM) is employed to evaluate and contrast various filter circuit architectures. Nonetheless, there is currently no FoM that fully integrates all key performance parameters of filters, including frequency response accuracy, noise, linearity and power supply, which are essential for a fair evaluation.

Among various innovative filter circuit architectures, the Active-RC biquadratic cell provides a balanced trade-off between the advantages of Active-RC and gm-RC approaches [6]. However, careful consideration must be given to the thermal noise of resistors and the input stage noise of operational amplifiers.

On the other hand, as illustrated in Fig. 2-4, configurations based on Source-Follower circuits have undergone thorough examination. As mentioned in reference [7], a "composite" Source-Follower biquadratic cell employs positive feedback to synthesize complex poles through a single branch. Furthermore, in reference [8], as shown in Fig. 2-5, examined the cascading of compact single-pole cells, where the alternation of positive and negative cells facilitated the synthesis of complex poles.

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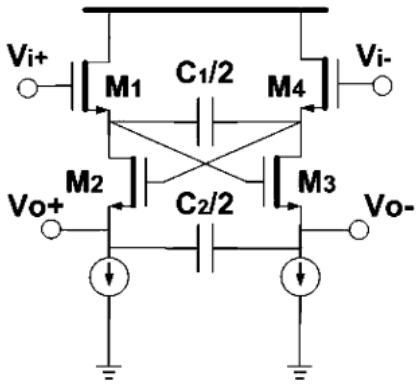

Fig. 2-4 Continuous-time filter implemented with a source-follower topology [7].

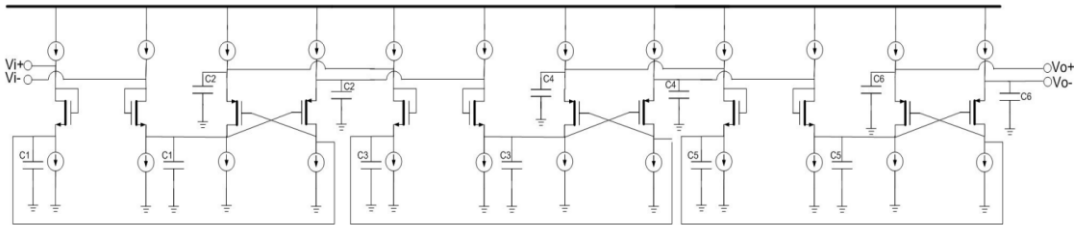

Fig. 2-5 Overall architecture of the cascaded continuous-time filter implemented with a source-follower topology [8].

Recently, as shown in Fig. 2-6, the Super-Source-Follower (SSF) topology has been recently utilized for the efficient realization of a fully differential Sallen-Key filter [9], offering exceptionally wide bandwidth and minimal in-band noise. Nevertheless, an additional power budget is needed to effectively reject out-of-band zeros in the Sallen-Key configuration.

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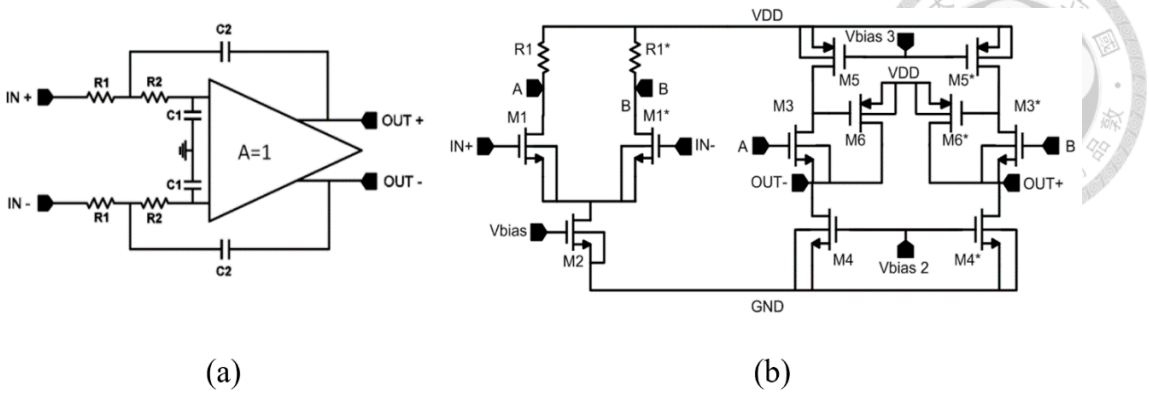

(a) (b)

Fig. 2-6 (a) Topology of the sallen-key biquadratic filter. (b)Schematic of the active element in the second sallen-key stage (nMOS implementation) [9].

In the process of developing this approach, an optimized circuit architecture for analog filters has been proposed. This architecture employs the Super-Source-Follower (SSF) circuit as the fundamental building block of the filter, needing just two active transistors and two supplementary capacitors, this design enables the implementation of an efficient and robust biquadratic filter cell [10]. The filter architecture is well-suited for implementation in a pseudo-differential topology, removing the necessity for a common-mode feedback circuit, as the output voltage is determined by the gate-source voltage of the SSF configuration.

The overall schematic of the 4th-order filter is depicted in Fig. 2-7. This filter is composed of two biquadratic cells arranged in a cascade within a pseudo-differential topology. The initial cell incorporates an NMOS-SSF, whereas the subsequent one utilizes a PMOS-SSF. This configuration ensures consistent input and output common-mode voltages, effectively mitigating for the level-shifting effects introduced by each cell.

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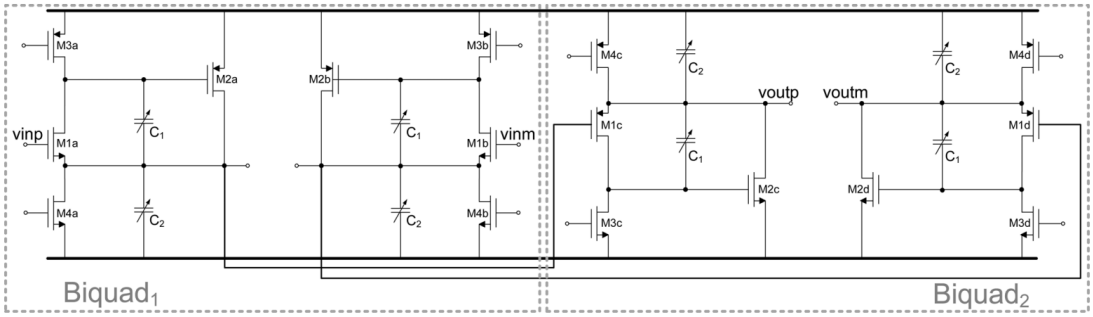

Fig. 2-7 SSF-based filter [10]

In summary, considering all the aforementioned circuit architectures and based on the performance metrics outlined in Table 2-1, the SSF-based architecture demonstrates the lowest power and lower in band integrated noise. Therefore, the SSF-based design was selected as the filter architecture for this system.

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Table 2-1 Performance comparison of filter architectures

	TCASI'09 [5]	**JSSC'06 [6]**	**JSSC'06 [7]**	**ISSCC'08 [8]**	**ESSCIRC'10 [9]**	**JSSC'15 [10]**
Technology [nm]	180	130	180	130	40	180
Topology	Active-RC	Gm-C	SF-C	SF-C	Active-RC	SSF-C
Order	5	4	4	6	5	4
DC Gain [dB]	0	4	-3.5	0	0	-2
Bandwidth [MHz]	300	11	10	280	880	33
SNR [dB]	56.6	81	79	-	-	70
THD [dB]	-40	-40	-40	-	-	-40
In band integrated noise [μVrms]	860	36	23.7	368	320	45
Power [mW]	54	14.2	4.1	0.12	27.5	1.38
Area [mm^2]	0.63	0.9	0.43	0.06	0.039	0.14

To validate the SSF concept, a prototype circuit was implemented using 40nm CMOS technology. The circuit consists of a single SSF biquadratic filter cell, realizing a second-order low-pass transfer function with a -3 dB bandwidth of 400 MHz. The filter operates under a 1 V power supply, consuming 57 μA of current. Owing to the inherent linearity provided by the local feedback mechanism of the SSF, the filter demonstrates a P_{1dB} of 450 mV_{PP}.

2.3 Fundamentals of the Variable Gain Amplifier

The Variable-Gain Amplifier (VGA) plays a crucial role in analog front-end control circuits due to its capability of providing adjustable gain, thereby enhancing the overall

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system dynamic range. Over the past few decades, significant research efforts have been dedicated to addressing key design challenges, including the achieving of precise dB-linear gain control, wide bandwidth and low power consumption. With the rapid growth in rising need for data-driven analytics and machine learning technologies, the need for efficient signal processing has increased exponentially. To meet these requirements, the data rate of several hundreds of megabits per second is highly anticipated at the analog baseband stage, necessitating VGAs that deliver precise gain control with excellent energy efficiency, while achieving wide bandwidth and preserving a compact form factor.

While designing a VGA using SiGe technology is relatively straightforward due to its ultra-high cut-off frequency and the inherent exponential current-voltage characteristics of BJTs [11], which facilitates dB-linear gain control, there are several considerations compared to MOSFETs. First, in terms of manufacturing cost, BJTs are less commonly integrated than MOSFETs in modern CMOS technology. Implementing a BJT-based VGA typically requires specialized BiCMOS or SiGe processes, which increases the manufacturing cost. Given the widespread use of CMOS technology in integrated circuits, a MOSFET-based VGA provides advantages in production cost and leverages a more established technology. Moreover, MOSFETs implemented with CMOS technology can achieve wideband performance using advanced processes, making standard CMOS technology a more favorable choice for VGA design.

Secondly, BJTs tend to have higher power consumption due to their operational principles, which require a base current to control the collector current. This means that BJT-based VGA designs always involve a continuous base current flow, resulting in higher static power dissipation. Additionally, BJTs require a relatively higher base-emitter voltage (VBE), typically around 0.7V, for conduction, whereas MOSFETs can operate with a lower gate-source voltage, making MOSFETs more suitable for low-

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voltage operation. Consequently, a MOSFET-based VGA typically consumes less power compared to a BJT-based design.

Thirdly, BJT-based VGA designs require more complex biasing circuits due to their high temperature sensitivity. This temperature dependence means that the current in BJTs can vary significantly with changes in temperature. To stabilize the operating point, BJT-based VGAs usually need more sophisticated biasing circuits to compensate for temperature fluctuations, which adds complexity to the circuit design, especially in applications that demand high stability and reliability.

Finally, there is the issue of integration. BJTs are more challenging to integrate into standard CMOS processes, whereas MOSFETs can be easily integrated into standard CMOS technology, providing advantages in large-scale integration. This also effectively reduces the required circuit area in design. In summary, although BJT-based designs have their advantages in achieving dB-linear gain characteristics and are suitable for high-speed and wideband applications, their disadvantages include higher power consumption, increased manufacturing costs, complex biasing circuitry, and difficulty integrating into standard CMOS processes. Therefore, MOSFET-based designs are generally more suitable for VGA circuit implementation.

However, for a MOSFET-based VGA design, compared to a BJT-based design, there are two primary challenges that need to be addressed. First is the accuracy of the gain characteristic with a linear response in decibels (dB). Owing to the square-law behavior of MOSFETs, additional circuitry is required in CMOS technology designs to generate an exponential characteristic, thereby ensuring dB-linear accuracy. The quasi-exponential generator is a essential circuit component that serves to transform the mapping of the control voltage to the gain of the VGA, converting it from a linear scale to a decibel (dB) scale. Therefore, optimizing the pseudo-exponential generator is an

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indispensable element in achieving a MOSFET-based VGA with precise dB-linear characteristics.

Secondly, the issue of operating frequency and bandwidth must be addressed. This challenge is associated with the lower carrier mobility, larger parasitic capacitance, and transconductance characteristics of MOSFETs, which often necessitate higher power consumption or result in a more complex circuit architecture when implementing wideband designs. This complexity makes it difficult to integrate additional exponential generation circuits to achieve accurate dB-linear gain control. For designs targeting precise dB-linear performance and minimal power consumption, a larger chip area is typically required to achieve better matching. Moreover, due to the adoption of closed-loop topologies, these designs are typically suitable only for narrowband applications.

Due to the considerable power consumption of the exponential function generator, it is desirable in low-power designs to develop a VGA incorporating an intrinsic dB-linear compensation mechanism, thereby eliminating the need for additional control circuitry. Furthermore, it is essential to investigate the fundamentals of exponential generation and broadband design methodologies further. Subsequently, the following sections summarize several state-of-the-art techniques and approaches. As shown in Fig. 2-8, a pair of transistors with different oxide thicknesses are employed as source-degenerated resistors in combination with a differential amplifier to generate a linear response [12]. By arranging three circuit cells in a cascade, a pseudo-exponential function is naturally generated and seamlessly integrated into the core of the VGA. Consequently, the proposed VGA attains 50 dB gain range with a gain accuracy maintained within ±0.5 dB, without the need for any additional pseudo-exponential generation circuit.

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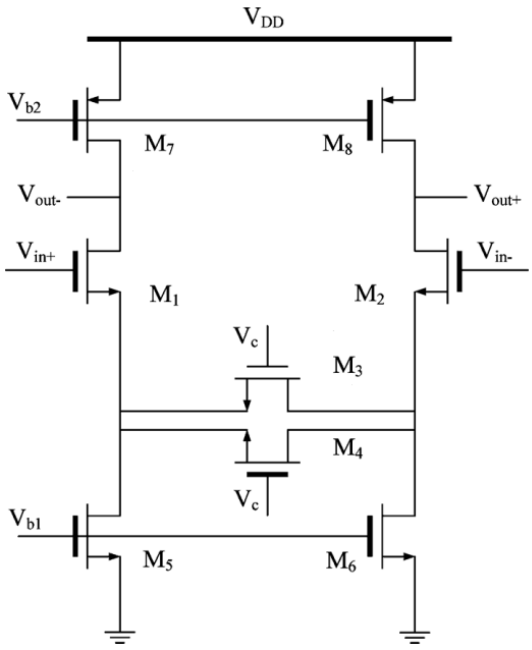

Fig. 2-8 A VGA architecture employing source degeneration for transconductance adjustment [12].

Another design example, as shown in Fig. 2-9, adopts a different approach. Rather than relying on source-degenerated transistors for gain control, incorporating a pair of transistors operating in distinct regions can also facilitate the design of a dB-linear VGA, as illustrated in [13]. By precisely tuning the bias conditions of these two transistors, the current flowing through each load transistor can be efficiently regulated. Through this approach, accurate dB-linear characteristics can be attained. However, the limitation of this approach lies in the restricted bandwidth caused by the parasitic capacitance accumulated at the output node, which constrains its suitability for high-frequency VGA applications.

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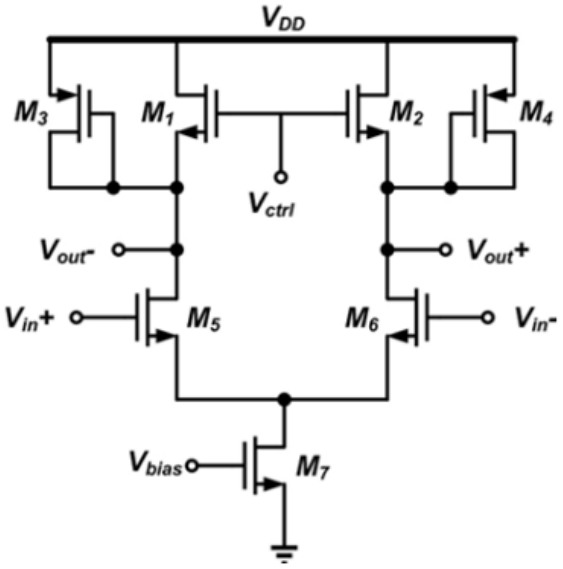

Fig. 2-9 A VGA architecture designed to control the load current [13].

To achieve higher operating frequencies, bandwidth enhancement techniques can be employed. A widely recognized approach is inductive peaking, which is considered one of the most effective approaches to implementing high-performance wideband amplifiers. Nevertheless, spiral inductors are quite bulky and occupy a significant amount of chip area. As a result, inductor-less designs have garnered more attention in recent years. In Fig. 2-10, a pair of cross-coupled capacitors is employed to introduce a transmission zero at higher frequencies through the use of positive feedback, thereby boosting the total bandwidth of the amplifier [14]. Nonetheless, the capacitance needed within the negative feedback loop is relatively minimal, generally ranging from several tens of femtofarads (fF). These minimal capacitance values are extremely susceptible, and their implementation can be challenging as a result of parasitic capacitance effects, which can negatively affect the flatness of in-band gain, degrading performance.

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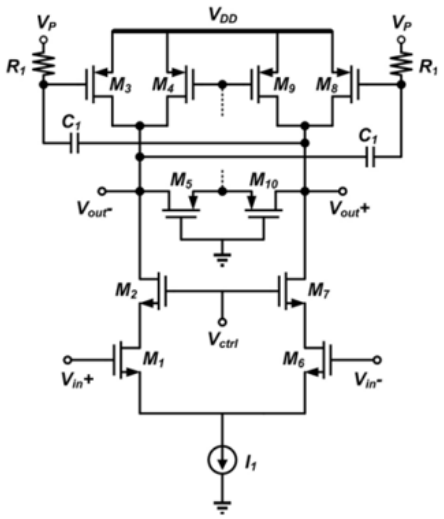

Fig. 2-10 A VGA architecture utilizing cross-coupled capacitors to achieve gain peaking [14].

Fig. 2-11 presents a gate peaking technique [15], which utilizes a similar concept to that in Fig. 2-9 to achieve dB-linear gain control. In this approach, gain peaking is accomplished near the cut-off frequency aided by the use of transistors M8 and M9. As the "peaking" resistor is realized using a MOSFET operating in the triode region, the position of the transmission zero can be precisely adjusted. Consequently, the magnitude of gain peaking can be effectively regulated by adjusting the bias voltage.

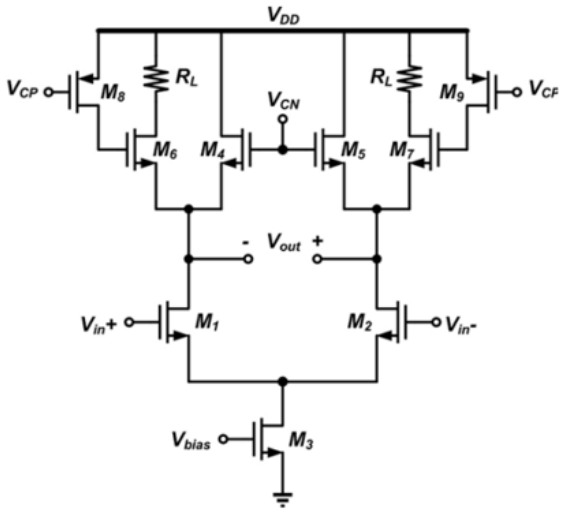

Fig. 2-11 A VGA architecture employing gate bias control for gain peaking [15].

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It is important to highlight that these designs can be classified into two categories according to their gain-control mechanisms. The configurations shown in Fig. 2-8 and Fig. 2-10 regulate the overall gain by varying their transconductance, whereas the other two topologies in Fig. 2-9 and Fig. 2-11 manipulate the load impedance of the amplifiers to control gain. Thus, it is clear that by simultaneously tuning both the transconductance and load impedance in the same direction whether increasing or decreasing, a broader gain variation range can be realized. This principle is demonstrated in Fig. 2-12, which illustrates a four-stage wideband variable-gain amplifier without inductors [16]. The first and third stages operate as fixed-gain units delivering higher gain, whereas the second and fourth stages function as variable-gain units. These stages leverage self-compensated transistors are utilized to achieve precise dB-linear gain control, eliminating the need for a pseudo-exponential generator.

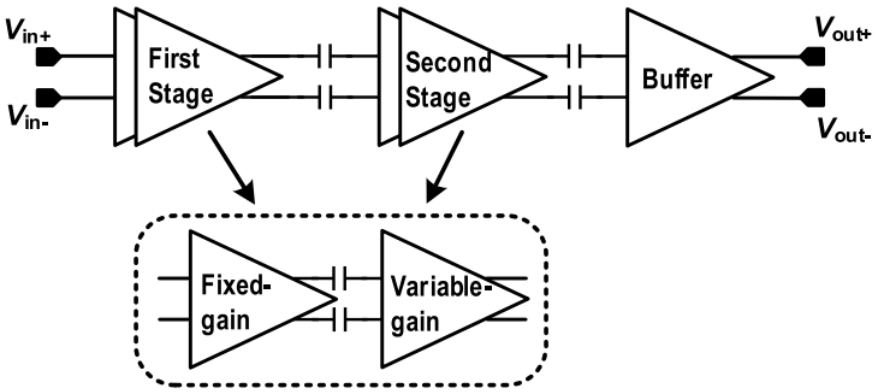

Fig. 2-12 A wideband VGA featuring self-compensated transistors for precise dB-linear characteristics [16].

Fig. 2-12 illustrates a wideband variable-gain amplifier featuring self-compensated transistors for precise dB-linear characteristics. Based on the analysis of all the circuit architectures discussed above and the performance comparison in Table 2-2, the wideband variable-gain amplifier with self-compensated transistors demonstrates the best performance metrics.

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Therefore, this architecture is selected as the foundation for designing the filter in this system.

Table 2-2 Performance comparison of VGA architectures

	JSSC'13 [12]	**JSSC'15 [13]**	**TCAS-I'06 [14]**	**TMTT'16 [15]**	**TCAS-I'20 [16]**
Technology [nm]	65	180	180	65	65
Type	Tune g_m	Manipulate R_L	Tune g_m	Manipulate R_L	Tune g_m
Gain Range [dB]	76 (-13~63)	38.6 (1.6~40.2)	95 (-52~43)	22 (2~24)	40 (-19~21)
Bandwidth [GHz]	0.0148	0.149	1.05	2.2	4
Power [mW]	3.84	0.74	6.5	3.48	3.5
Area $[mm^2]$	0.01	0.034	0.4	0.01	0.012
FoM	29.3	228.6	38.4	1390.8	3809.5

$$FOM = \frac{Bandwidth\ [GHz] * dB - linear\ Gain\ Range\ [dB]}{Power\ [mW] * Active\ Area\ [mm^2]}$$

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Chapter 3 Design of the Analog Front-End Control Circuit

This chapter provides an overview of the analog front-end control circuit and describes the design of each component in detail, beginning with a baquadratic filter based on the Super-Source-Follower (SSF) architecture, which is used to suppress unwanted signals while maintaining low power consumption. The variable gain amplifier (VGA) is then discussed, focusing on achieving accurate dB-linear characteristics and extending bandwidth through the use of active inductors. The fixed gain unit works in conjunction with the VGA to ensure sufficient gain for maintaining the precision required in qubit operations. In brief, the analog front-end control circuit is designed to meet the stringent requirements of qubit control, including cryogenic operation, power efficiency, high fidelity, and wide bandwidth.

3.1 The Block Diagram and Architecture of the Proposed System

Fig. 3-1 illustrates a complex signal processing chain designed for quantum qubit control, which is crucial for ensuring the precise manipulation of quantum states. The system initially receives differential input signals, VINP and VINN, which pass through a filtering stage to eliminate unwanted frequency components, thereby enhancing signal integrity. The filtered signals are then fed into a combination of fixed-gain and variable-gain amplifiers, allowing for precise control over signal amplification. This flexibility is essential to accommodate the varying signal strengths required for different qubit operations. Following the amplification stages, multiple output buffers are employed to

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ensure adequate signal driving capability while isolating the outputs from the core circuitry. This system architecture is pivotal for scalable quantum computing, where precise and reliable qubit control is key to the successful execution of quantum algorithms.

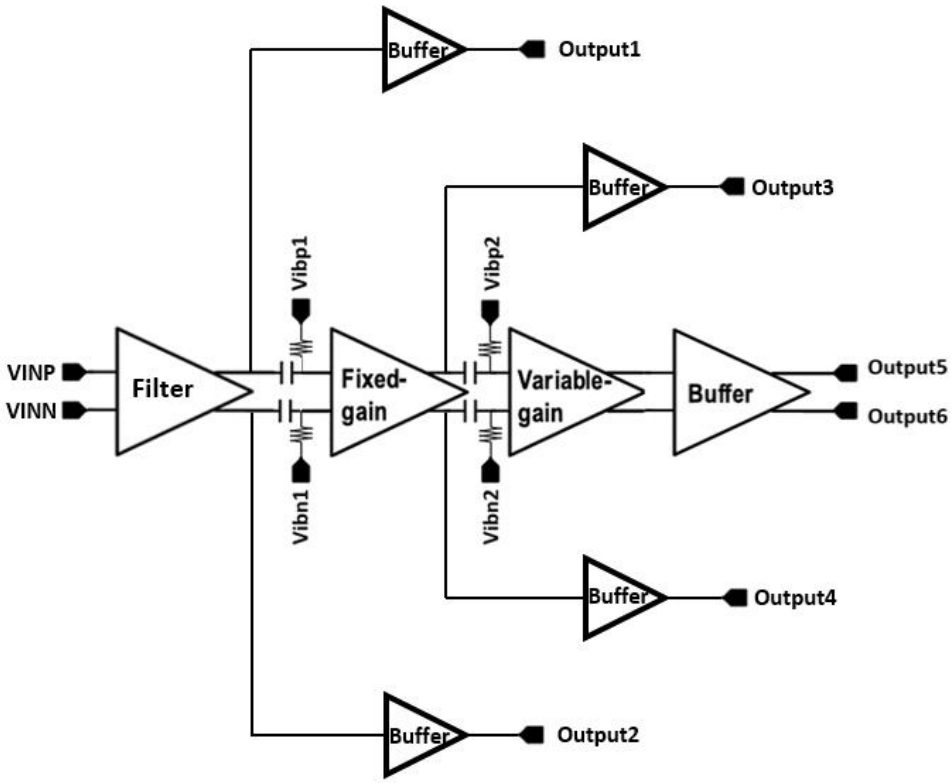

Fig. 3-1 Architecture of the overall system.

The system is applied to control qubits and is required to operate in a cryogenic environment at 3K, leading to several challenges that define the implementation and verification of the circuit design, and subsequently define the specifications for the entire circuit.

First, the circuit must operate at an extremely low temperature of 3K. As a result, the power consumption cannot be too high, as excessive power consumption during operation may alter the environmental temperature. Therefore, the target power consumption of the overall circuit is less than 1mW.

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Secondly, qubits are fragile, requiring control by high-fidelity circuits to precisely manipulate the solid-state qubits. The target fidelity is 99.99%, hence the signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) of the circuit should achieve 40 dB.

Thirdly, since the circuit needs to control multiple solid-state qubits, the operational frequency range must be sufficiently wide, with a target bandwidth of 300 MHz.

Finally, for controlling multiple qubits, the signals for different qubits must be modulated to different levels for identification, requiring the VGA to provide a gain variation range of at least 20 dB. In summary, specifications were defined for the two modules in this design. Table 3-1 presents the specification sheet for the filter, while Table 3-2 outlines the specifications for the variable gain amplifier.

Table 3-1 Specification sheet for the filter

	Specification
Technology	40 nm CMOS
Operating Frequency [MHz]	100
Supply Voltage [V]	1
Gain (in 100MHz) [dB]	-5
Bandwidth [GHz]	0.3
SNR [dB]	40
SFDR [dB]	40
THD [dB]	-40
Power [mW]	<0.08

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Table 3-2 Specification sheet for the VGA

	Specification
Technology	40 nm CMOS
Operating Frequency [MHz]	100
Supply Voltage [V]	1
Gain Range [dB]	20
Bandwidth [GHz]	0.3
Power [mW]	<0.55

This design primarily consists of two modules: the filter and the variable gain amplifier, each serving the purposes outlined below. The circuit architecture for controlling qubits is illustrated in Fig. 3-1. The filter is mainly used for filtering the output signal when the signal generated by the DAC is converted to an analog signal. The fundamental frequency of the output signal is f_0, and during the frequency conversion process, replicas of the signal may appear at $n \times f_0$ (where n is an integer). The filter is thus required to filter out all signal replicas except for the fundamental frequency. A second-order filter is designed to ensure cleaner suppression of unwanted signal components. Since the circuit needs to control multiple solid-state qubits, the qubit signals need to be modulated to different levels for identification, which is achieved by the VGA adjusting the gain. This gain adjustment process must be linear in dB.

3.2 Circuit Implementation of the Filter

3.2.1 Design of the SSF-Based Baquadratic Cell

As shown in Fig. 3-2, the fundamental architecture of the proposed single-ended version of the baquadratic cell is presented. Resistors R1, R2, R3 indicated by the dashed lines , signify the limited output resistance of the MOS transistors, which will be taken into account during the later analysis of the transfer function. This biquadratic cell

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leverages the Super-Source-Follower (SSF) circuit, with two additional capacitors to synthesize complex poles.

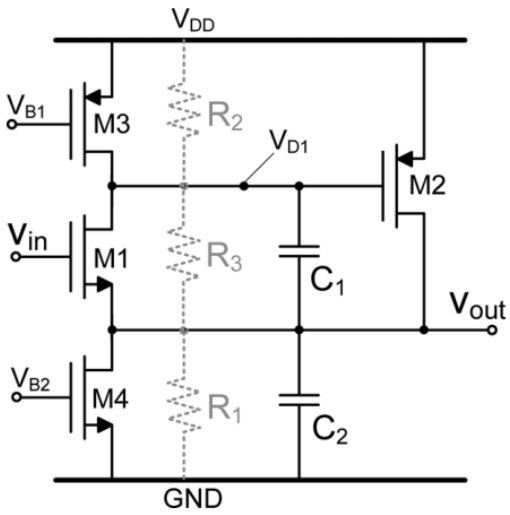

Fig. 3-2 SSF-Based biquadratic filter [10].

The input signal is fed to the gate of transistor M1, which operates in the subthreshold region, exhibiting an extremely high input impedance. The output signal is obtained from the source of transistor M1, resulting in an output voltage that is reduced by a value of V_{GS} compared to the gate input signal. The voltage discrepancy between the input and output is a characteristic feature of source followers, which can limit their effectiveness in large-signal processing and necessitates thorough consideration during system design. Simultaneously, this configuration enables the output common-mode voltage to remain independent of the input common-mode voltage, meaning that no additional common-mode feedback circuit is required, which reduces signal distortion, saves area and power. Regarding the power supply, to ensure proper operation, the minimum required V_{DD} can be expressed as $V_{SW} + 2V_{OV} + V_{GS}$, where V_{SW} corresponds to the output signal swing and $V_{OV} = V_{GS} - V_{TH}$.

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The transfer function associated with the biquadratic cell utilizing the Super-Source-Follower (SSF) architecture is given by Equation (3.1), where g_{m1} and g_{m2} represent the transconductance values of transistor M1 and M2, respectively:

$$T(s) \cong \frac{A_0}{1+s\frac{C_1}{g_{m1}}+S^2\frac{C_1C_2}{g_{m1}g_{m2}}} \tag{3.1}$$

The DC gain can be expressed by Equation (3.2), which is related to resistors R1, R2**,** and R3 (as shown in Fig. 3-2):

$$A_0 = \frac{g_{m1}R_1R_3+g_{m1}g_{m2}R_1R_2R_3}{R_1+R_2+R_3+g_{m1}R_1R_3+g_{m2}R_1R_2+g_{m1}g_{m2}R_1R_2R_3} \cong 1 \tag{3.2}$$

Specifically, resistor R1 is the parallel combination of the drain-source resistances of transistors M4 and M2 ($r_{ds4}//r_{ds2}$), while resistor R2 represents the output resistance of M3 transistor (r_{ds3}), and resistor R3 models the drain-source resistance of M1 transistor (r_{ds1}). When resistor R3 is significantly larger than resistors R1 and R2, the DC gain of the second-order cell can be approximated by Equation (3.3):

$$A_{0_{noR3}} \cong \frac{g_{m1}g_{m2}R_1R_2}{1+g_{m1}g_{m2}R_1R_2} \tag{3.3}$$

In comparison to a single-transistor source follower implementation [9], this design demonstrates a substantial enhancement in voltage buffering performance. It is worth mentioning that if resistor R3 approaches the values of resistors R1 and R2, a minor decrease in DC gain may occur, which can be interpreted as a second-order effect in small-signal analysis.

The frequency and quality factor of the specific complex pole pair synthesized by the SSF biquadratic filter are given in Equation (3.4):

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}\ ;\ Q = \frac{C_2}{C_1}\frac{g_{m1}}{g_{m2}} \tag{3.4}$$

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In general, achieving high-frequency poles necessitates either increasing the transconductance (gm) or reducing the capacitance. Nonetheless, the capacitance cannot be excessively reduced, as it must remain substantially greater than the parasitic capacitance present at each node (to ensure industrial reliability, the parasitic capacitance should constitute less than 20% of the overall capacitance). This reliability requirement constrains the extent to which the capacitance can be minimized, thereby necessitating higher transconductance to facilitate the synthesis of high-frequency poles. This presents a common trade-off, as larger transconductance competes with the need for linearity optimization, which requires a higher overdrive voltage (V_{OV}).

As will be explained, unlike many conventional topologies, the linearity improves when the overdrive voltage is lower. Therefore, filters designed with minimal overdrive voltage can efficiently synthesize high-frequency poles while minimizing power consumption. Furthermore, the proposed SSF-based biquadratic cell only uses two transistors M1 and M2 for analog filtering, with just three nodes (VIN, VOUT, and VD1). As a consequence, the quality factor exhibits lower sensitivity to parasitic effects, including high-frequency poles, when compared to alternative continuous-time filter architectures. As indicated in Equation (3.4), As shown in Equation (3.4), the pole frequency can be adjusted by digitally configuring the capacitor array, enabling programmable bandwidth and supporting the implementation of a reconfigurable filter. Moreover, the capacitor array can also be employed to compensate for process variations.

The primary distinction between the SSF cell architecture and the single transistor source follower lies in the incorporation of a supplementary local feedback loop implemented via transistor M2. Compared to a standalone transistor configured as a source follower, this represents a significant advantage of the SSF cell, as the feedback loop between transistors M1 and M2 further reduces the variation in voltage between the

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gate and source terminals of transistor M1 and decreases the total output impedance of the SSF cell. Consequently, the smaller variation in voltage between the gate and source terminals of transistor M1, the better the in-band linearity performance. Moreover, the decreased output impedance results in reduced in-band noise, as the noise currents generated by transistors M2, M3, and M4 (shown in Fig. 3-2) will pass through a smaller output impedance.

First, we will examine the loop gain, and the approximate value of the low-frequency loop gain, G_{loop0}, is given by Equation (3.5):

$$G_{loop_0} = -g_{m2} * \left(\frac{1}{g_{m1}} // R_1\right) * g_{m1} * R_2 \cong -g_{m2}R_2 \tag{3.5}$$

Because G_{loop0} is determined by the transconductance of M2 transistor (g_{m2}) and the output resistance of transistor M3 (R_2), the SSF-based cell architecture allows for the optimization of DC gain and linearity is achieved without altering the characteristics of transistor M1. In practice, to improve in-band linearity can be achieved by biasing transistor M1 in the moderate or weak inversion region, which corresponds to a low overdrive voltage, thereby reducing the current I_{DS}. As a result, the output resistance of transistor M1 decreases without impacting the loop gain of the SSF cell. Equation (3.6) presents the transfer function of the loop gain:

$$G_{loop}(s) \cong \frac{-g_{m2}R_2 \cdot \left(1 - s\frac{C_1}{g_{m2}}\right)}{1 + sR_2C_1\left(1 + \frac{g_{m2}}{g_{m1}}\right) + s^2\frac{C_1C_2R_2}{g_{m1}}} \tag{3.6}$$

At low frequencies, the system is characterized by a dominant pole p1, a right-half-plane zero z1, and an additional pole p2, with their respective values given in Equation (3.7).

$$p_1 \cong \frac{g_{m1}}{R_2C_1(g_{m1}+g_{m2})} \; ; \; z_1 \cong \frac{g_{m2}}{C_1} \; ; \; p_2 \cong \frac{g_{m1}+g_{m2}}{C_2} \tag{3.7}$$

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As expected, the higher loop gain at low frequencies reduces the gate-source voltage swing of the transistor M1, hence enhancing linearity characteristics. Conversely, the dominant pole p1 leads to a gradual decrease in the magnitude of G_{loop} as the frequency rises. Consequently, a decline in linearity is expected at higher frequencies, similar to other closed-loop analog circuits.

Next, regarding the output impedance, the equivalent output impedance R_{out} of the SSF architecture at low frequencies is given by Equation (3.8), which corresponds to the low-frequency transfer function, assuming R3 is greater than R1 and R2:

$$R_{out} = \frac{R_1(R_2+R_3)}{R_1+R_2+R_3+g_{m1}R_1R_3+g_{m2}R_1R_2+g_{m1}g_{m2}R_1R_2R_3} \cong \frac{1}{g_{m1}} \cdot \frac{1}{g_{m2}R_2} \tag{3.8}$$

The feedback loop between transistor M1 and transistor M2 further reduces the standard output impedance associated with a single-transistor source follower, typically estimated as $1/g_{m1}$. The reduction is roughly equal to G_{loop0}, which is approximately $g_{m2}R_2$, thereby improving noise performance. However, it should be noted that the output impedance may experience a slight increase due to the influence of R_3.

Lastly, regarding output noise, the in-band output-referred noise remains relatively consistent in value, with its expression given in Equation (3.9). Here, Rout represents the output impedance of the SSF architecture. It is important to note that v_{n1} to v_{n4} correspond to the equivalent voltage noise sources of transistors M1 through M4, respectively:

$$ON^2 \cong v_{n1}^2 + v_{n2}^2 + v_{n3}^2 + v_{n4}^2 \cong v_{n1}^2$$

$$= \frac{4kT\gamma}{g_{m1}} \cdot \left(\frac{R_1}{R_1+\frac{1}{g_{m1}}}\right)^2 + \frac{4kT\gamma}{g_{m1}} \cdot (g_{m1}R_2 \cdot g_{m2}R_{out})^2 \tag{3.9}$$

Where

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$$v_{n1}^2 = \frac{4kT\gamma}{g_{m1}} \cdot \left(\frac{R_1}{R_1 + \frac{1}{g_{m1}}}\right)^2 + \frac{4kT\gamma}{g_{m1}} \cdot (g_{m1}R_2 \cdot g_{m2}R_{out})^2 \quad (3.10)$$

$$v_{n2}^2 = 4kT\gamma g_{m2} \cdot R_{out}^2 \quad (3.11)$$

$$v_{n3}^2 = 4kT\gamma g_{m3} \cdot (g_{m2}R_2R_{out})^2 \quad (3.12)$$

$$v_{n4}^2 = 4kT\gamma g_{m4}R_{out}^2 \quad (3.13)$$

In the overall output noise power spectral density, measured as the spot noise at the center of the filter passband, the transistor M1 is the primary noise contributor. The noise contributions from the other transistors (M2, M3, and M4) are lower due to the output impedance characteristics of the SSF architecture. The influence of flicker noise has been excluded from this analysis.

The validity of Equation (3.9) has been verified in the low-frequency range, where transistor M1 serves as the dominant source of noise. Conversely, a marginal rise in noise levels can be attributed to the impact of transistor M4. In proximity to the pole frequency, the increasing output impedance of the SSF architecture results in noticeable noise peaks originating from transistors M2, M3, and M4.

3.2.2 Design of the SSF-Based Filter

The complete schematic of the biquadratic filter is presented in Fig. 3-3. This filter consists of cascaded second-order cells, utilizing a fully differential circuit architecture. Table 3-3 outlines the key design parameters.

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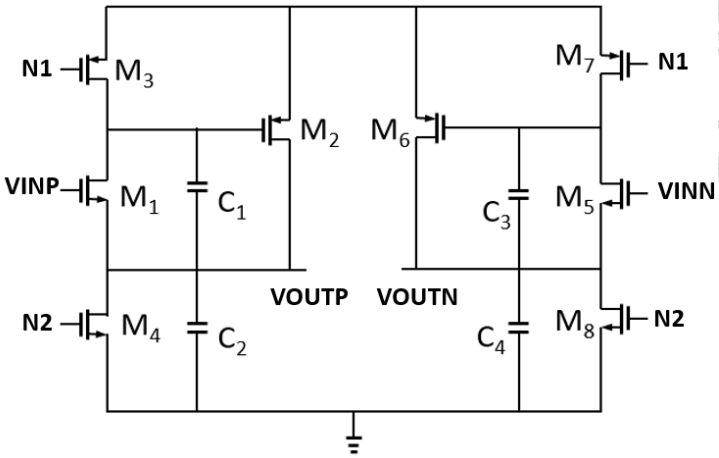

Fig. 3-3 Schematic of the differential implementation of the SSF-based filter.

Table 3-3 Parameter values of the SSF-based filter

Parameter	Value
Pole Frequency	561 MHz
g_{m1} / g_{m5}	196.4 μS
g_{m2} / g_{m6}	305.4 μS
C_1	28.7 fF
C_2	61.6 fF

A low-Q cell is positioned at the initial stage of the cascade to improve linearity characteristics in proximity to the cutoff frequency. This second-order fully differential circuit implements a biquadratic butterworth low-pass response characterized with a DC gain of approximately -2 dB. At a sampling frequency of 100 MHz, the gain remains around -2 dB, and the pole frequency is 561 MHz (-3 dB), as illustrated in Fig. 3-4, where the red line represents the pre-simulation results, and the blue line represents the post-simulation results. The total capacitance in the pseudo-differential implementation is 180.6 fF.

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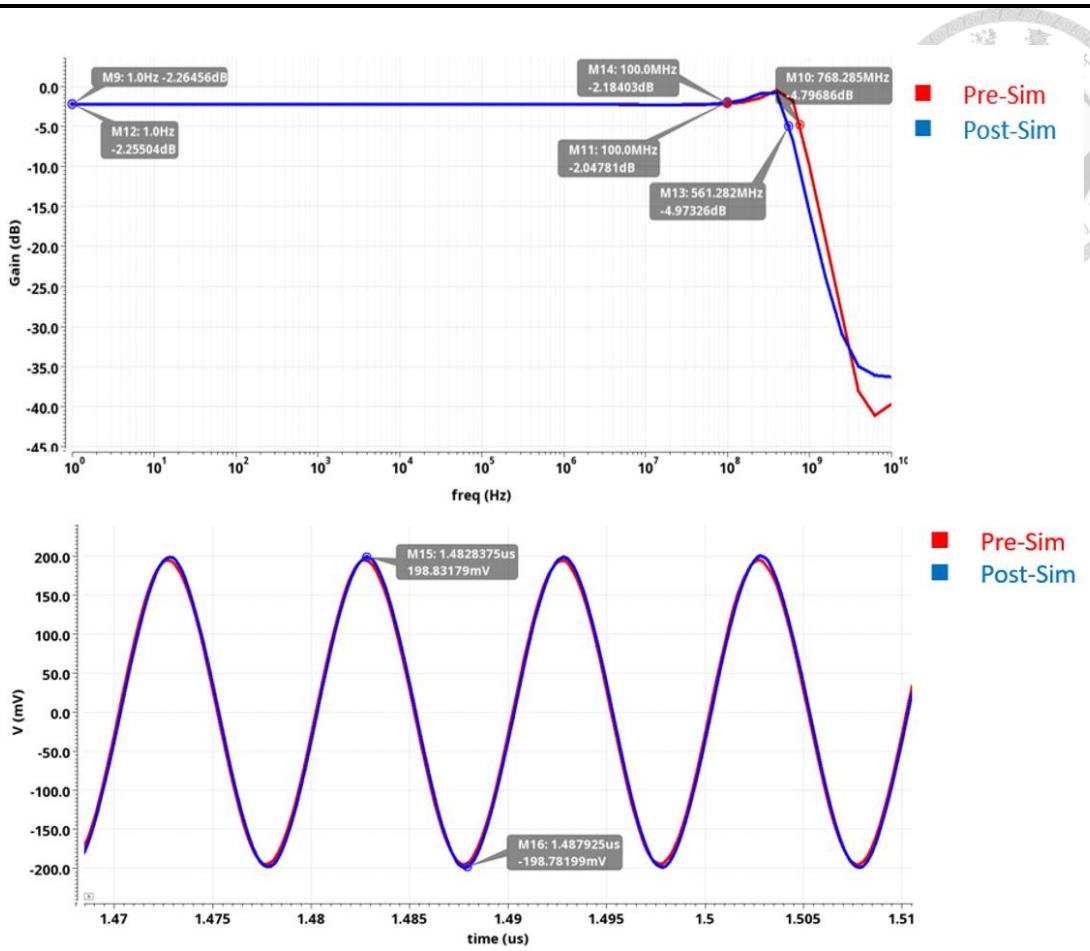

Fig. 3-4 AC Response (top) and Transient Response (bottom) of the filter based on the SSF architecture (The red line represents the pre-sim, while the blue line corresponds to the post-sim.)

The output stage of the filter circuit based on the SSF architecture requires a broadband output buffer. The design of the output buffer is illustrated in Fig. 3-5. Following the output stage, a bias-Tee is connected before interfacing with the 50Ω standard input impedance of the high-frequency measurement equipment.

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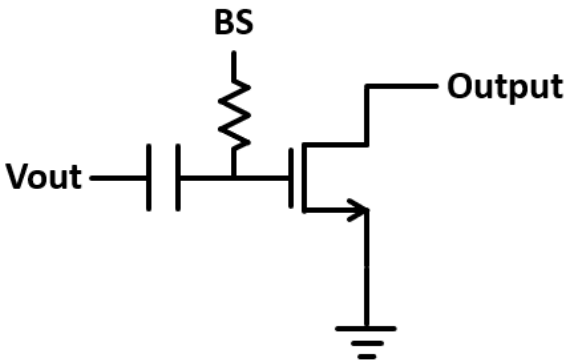

Fig. 3-5 Schematic of the output buffer.

Given that high-frequency testing equipment commonly operates with a standardized 50Ω input impedance, incorporating an output buffer is essential for achieving appropriate output matching and mitigating the impact of significant capacitive loading. In most cases, the output buffer is configured to operate with a gain of unity to maintain a sufficiently wide bandwidth, ensuring that it does not affect the overall high-frequency cutoff. Additionally, the input capacitance of the buffer should be minimized to avoid surpassing the driving capability of the preceding circuit stage.

Next, the discussion focuses on the simulation results, as shown in Fig. 3-6, the red line represents the pre-simulation results, while the blue line represents the post-simulation results. The biquadratic filter based on the SSF architecture, after passing through the buffer, exhibits a gain of -4.8 dB at a sampling frequency of 100 MHz. Subsequently, as seen in Fig. 3-7, the spectrum analysis shows Signal-to-Noise Ratio (SNR) of 42.8 dB, Spurious-Free Dynamic Range (SFDR) of 48.2 dB, and Total Harmonic Distortion (THD) of -50.4 dB. Lastly, the contributions to thermal noise can be analyzed as shown in Table 3-4. The simulation outcomes reveal that the in-band integrated output noise associated with the SSF architecture, excluding flicker noise, is

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104 nV^2. The corresponding output noise (ON) within a bandwidth of 400 MHz is 1.85*10^{-16} nV/ Hz.

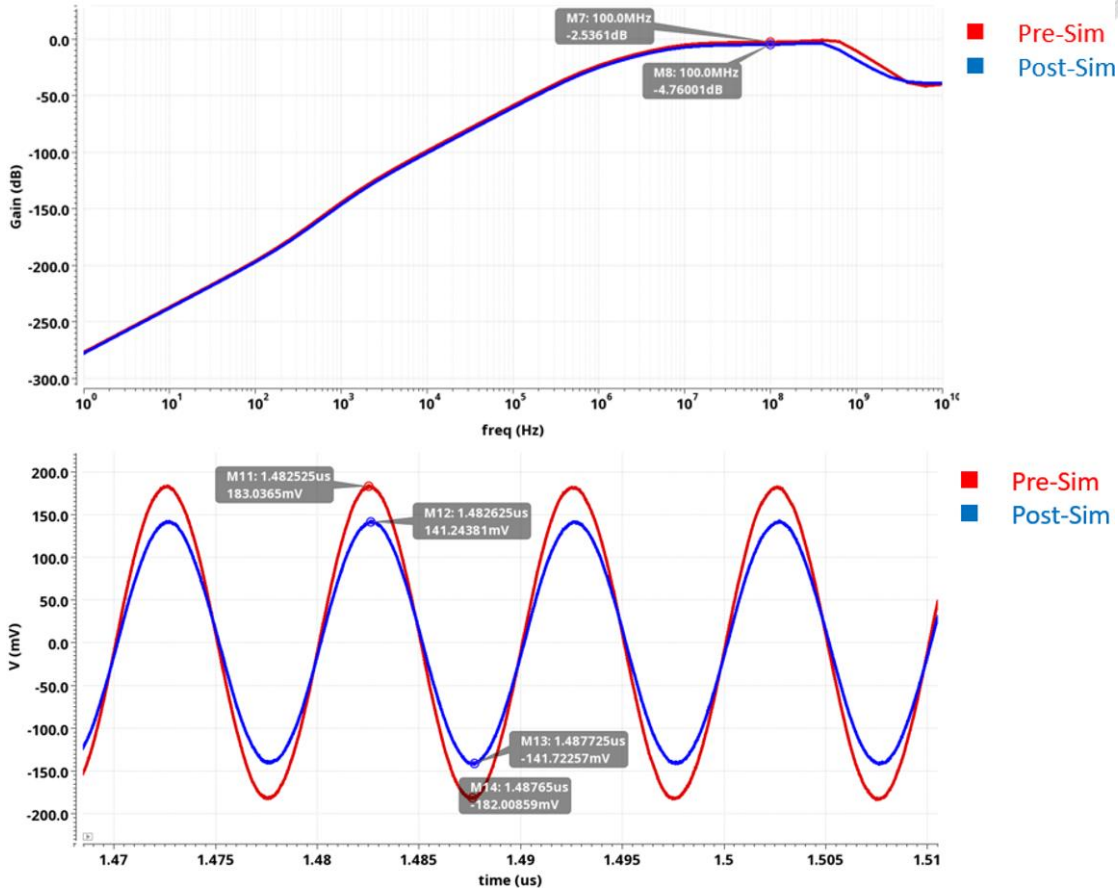

Fig. 3-6 AC response (top) and transient response (bottom) of the filter based on the SSF architecture after passing through the buffer (The red line represents the pre-simulation, while the blue line corresponds to the post-simulation.)

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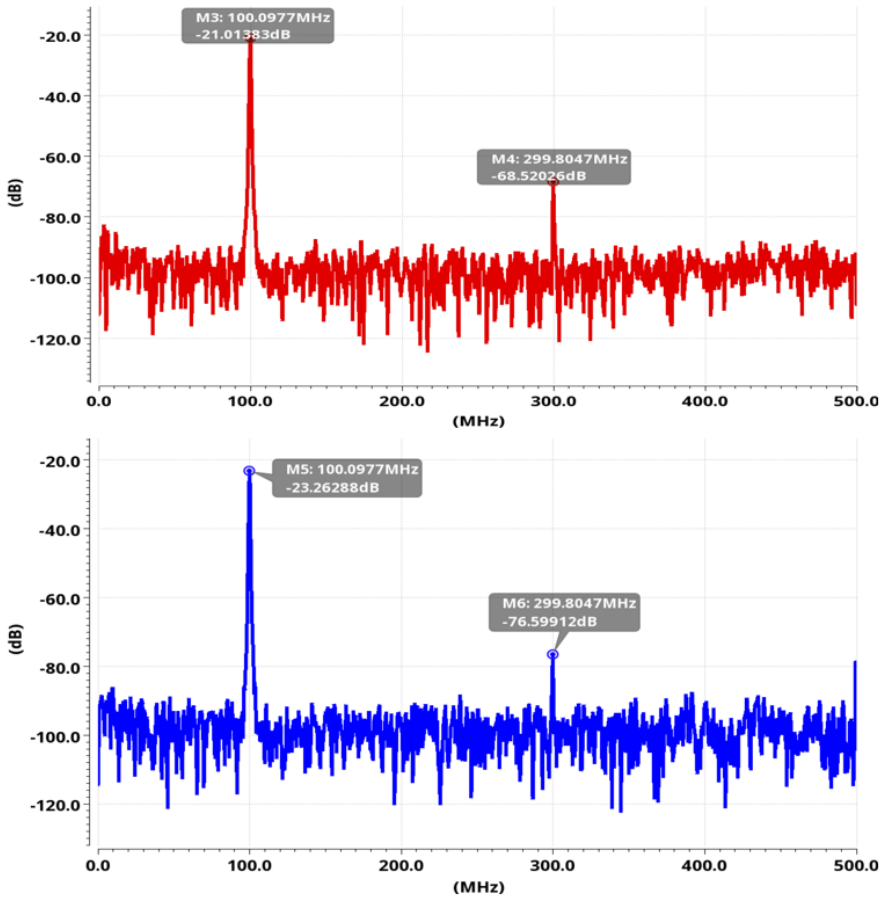

Fig. 3-7 Spectrum analysis of the filter Based on the SSF architecture after passing through the buffer (Red line represents pre-simulation, blue line represents post-simulation)

Table 3-4 Thermal noise analyze of the SSF-based filter

Device	Noise Contribution [V^2]	% of Total
M_1/ M_5	$2.2 * 10^{-8}$	43%
M_2/ M_6	$2 * 10^{-8}$	38.5%
M_3/ M_7	$3 * 10^{-9}$	6%
M_4/ M_8	$1.9 * 10^{-9}$	3.6%

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Finally, the comparison between the specifications defined in Table 3-1 and the simulation results is summarized in Table 3-5. At an operating frequency of 100 MHz, the results indicate that the gain, bandwidth, SNR, SFDR, THD, power consumption, and area all meet the expected design standards.

Table 3-5 Comparison of filter specifications and simulation results

	Specification	**Pre-sim (TT 40°C)**	**Post-sim (TT 40°C)**
Technology	40 nm CMOS		
Operating Frequency [MHz]	100		
Supply Voltage [V]	1		
Gain (in 100MHz) [dB]	-5	-2.5	-4.8
Bandwidth [GHz]	0.3	0.6	0.4
SNR [dB]	40	43.6	42.8
SFDR [dB]	40	47.5	48.2
THD [dB]	-40	-46.8	-50.4
Power [mW]	<0.08	0.062	0.057

3.2.3 Conclusions

This paper presents and analyzes a low-pass second-order filter cell based on the SSF architecture, exploring its performance with respect to DC characteristics, inearity, transfer function and noise. Additionally, a fully realized second-order filter prototype is described and tested, consisting of a single cell in a fully differential circuit configuration to demonstrate the feasibility of the concept. The developed prototype is implemented using 40 nm CMOS technology, featuring a -3 dB bandwidth of 400 MHz. Operating

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with a single 1 V power supply, the filter consumes 62 µA of current. The achieved signal-to-noise ratio (SNR) is 42.8 dB, with a total harmonic distortion (THD) of -50.4 dB for the output signal, and a P1dB of -4 dBm.

3.3 Circuit Implementation of the Variable Gain Amplifier

3.3.1 Theory of Self-Compensated Transistor

The principle of self-compensated transistors is based on the fact that both the transconductance and the output resistance of the transistor can simultaneously adjust gain modulation. Under appropriate bias conditions, these two factors can produce an exponential gain characteristic over a wide range. In the circuit depicted in Fig. 3-8(a), the transistor M_1 operates in the triode region, where I_0 represents an ideal current source, and R_L serves as the load resistor. The following analysis will explore how the transconductance of the transistor and the gain of the amplifier vary with different gate bias voltages.

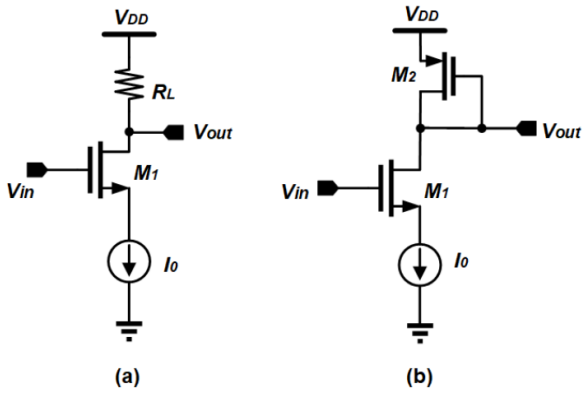

Fig. 3-8 Amplifier configurations based on triode-region operation: (a) using a resistor as the load, and (b) employing a diode-connected PMOS transistor as the load.

For a MOS device operating in the triode region, its drain current can be expressed by Equation (3.14).

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$$I_D = K\left[(V_{GS} - V_{TH})\,V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{3.14}$$

Where $K=\mu C_{ox}W/L$, with μ representing the effective carrier mobility, C_{ox} denoting the gate oxide capacitance per unit area, W being the gate of width, and L being the gate of length. V_{TH} is the threshold voltage. Given that the current source operates under ideal conditions, V_D remains unaffected by changes in gate voltage V_G. To maintain the same drain current as V_G varies, V_S must be appropriately adjusted. Therefore, V_S can be represented as a function of V_G, as shown in Equation (3.15).

$$V_S = (V_G - V_{TH}) \pm \sqrt{(V_G - V_D - V_{TH})^2 + \frac{2I_D}{K}} \tag{3.15}$$

When the overdrive voltage $V_{OV} = (V_G - V_S - V_{TH}) > 0$, the following Equation (3.16) can be obtained:

$$V_{DS} = -(V_G - V_D - V_{TH}) + \sqrt{(V_G - V_D - V_{TH})^2 + \frac{2I_D}{K}} \tag{3.16}$$

The transconductance g_m is defined as the partial derivative of the drain current I_D with respect to the gate-source voltage V_{GS}, as given in Equation (3.17).

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = KV_{DS} \tag{3.17}$$

Substituting equation (3.16) into equation (3.17), we obtain Equation (3.18).

$$g_m = K\left[-(V_G - V_D - V_{TH}) + \sqrt{(V_G - V_D - V_{TH})^2 + \frac{2I_D}{K}}\right] \tag{3.18}$$

Equation (3.18) can be simplified to yield Equation (3.19).

$$g_m = K'\left(-x + \sqrt{x^2 + 1}\right) \tag{3.19}$$

Where

$$K' = \frac{K}{\sqrt{2I_D/K}} \tag{3.20}$$

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$$x = \frac{(V_G - V_D - V_{TH})}{\sqrt{2I_D/K}} \tag{3.21}$$

Based on the Taylor series expansion, Equation (3.22) can be derived.

$$\sqrt{x^2 + 1} \approx 1 + \frac{x^2}{2} \tag{3.22}$$

Therefore,

$$g_m \approx K' e^{-x} \tag{3.23}$$

Additionally, the output resistance of a transistor functioning within the triode region represents a significant aspect that warrants consideration. This differs from a transistor operating in the saturation region, where the output resistance is relatively high and remains nearly constant. In the triode region, the output resistance of the transistor is on the same order as the load resistance and changes based on the biasing conditions. The drain-source conductance of a transistor in the triode region can be calculated using equation (3.14)

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = K(V_{GS} - V_{TH} - V_{DS}) = \sqrt{2I_D K} \cdot x \tag{3.24}$$

When the load resistor is substituted with a diode-connected transistor, as shown in Fig. 3-5(b), the output resistance can be expressed by equation (3.25):

$$R_{total} = \frac{1}{g_{ds} + g_{m2}} = \frac{1}{\sqrt{2I_D K_1} \cdot (c + x)} \tag{3.25}$$

Where

$$c = \sqrt{\frac{K_2}{K_1}} \tag{3.26}$$

Despite the fact that the drain-source conductance g_{ds} is linearly proportional to the variable x, when paralleled with another transistor and an appropriate value for c is chosen,

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the discrepancy between the resulting output resistance and the exponential function e^{-x} is substantially minimized. In consequence, by tuning the size ratio between PMOS and NMOS, it becomes feasible to achieve a variable load resistance with minimal dB-linear error.

The total gain of the amplifier is determined by both the transconductance and output resistance. Transforming this relationship to a dB scale yields Equation (3.27).

$$\text{Gain range (dB)} = \text{change in } g_m \text{ (dB)} + \text{change in } R_{total} \text{ (dB)} \quad (3.27)$$

Thus, we can take advantage of the characteristics of triode-region transistors, where both the transconductance and output resistance vary concurrently in the design of a variable gain amplifier (VGA), enabling a broader range of gain adjustment. By carefully optimizing the biasing conditions, it is possible to attain a gain variation exceeding 20 dB without compromising dB-linear accuracy.

3.3.2 Design of the dB-Linear Variable Gain Amplifier Unit

Fig. 3-9 illustrates the circuit diagram of the proposed variable gain unit. The design utilizes a source coupled differential pair operating in the linear region, with active inductors serving as the load to enhance the bandwidth. This circuit architecture employs two key techniques: first, gain error compensation, and second, bandwidth extension through the use of active inductors.

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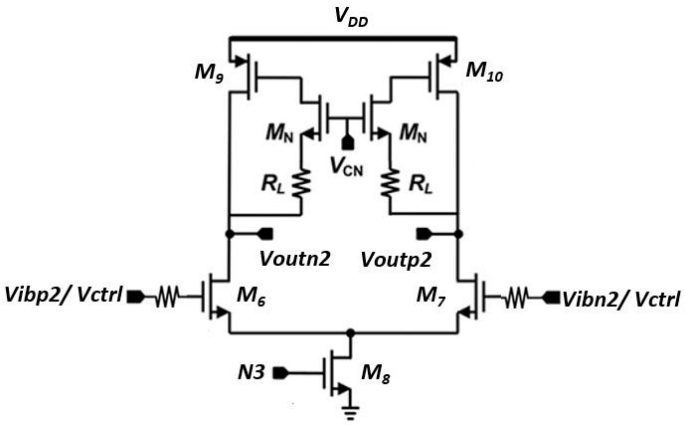

Fig. 3-9 Schematic of the variable gain amplifier unit

In the gain error compensation process, an increase in the control voltage leads to a corresponding rise in the overdrive voltage. Nevertheless, as the load transistor operates under consistent conditions, the voltage at the output node remains stable. At the same time, it is essential to ensure that the current through the input transistors remains stable. This necessitates an increase in the source potential of the input differential pair to reduce the drain-source voltage V_{DS} of the transistors. As the overdrive voltage continues to increase, the input differential pair shifts from operating in the moderate triode region to the deep triode region, while maintaining a steady current flow.

The analytical formulation presented in Section 3.3.1 relies on the conventional characteristic equation, which neglects all second-order effects and non-ideal factors. To achieve a more accurate analysis that aligns with the simulation outcomes, these influencing factors must be incorporated into the modified equation. As device dimensions continue to shrink to sub-micron scales, short-channel effects such as threshold voltage variation, mobility reduction due to vertical electric fields, and velocity saturation effects can no longer be ignored [15]. In evaluating the proposed circuit, mobility degradation becomes particularly prominent due to the high overdrive voltage.

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Hence, a more precise equation for representing short-channel devices is presented in Equation (3.28).

$$I_D = \frac{\alpha K[(V_{GS}-V_{TH})V_{DS}]}{1+\theta(V_{GS}-V_{TH})} \tag{3.28}$$

Here, θ is an empirical parameter utilized to characterize the influence of the vertical electric field on mobility degradation, while α is an additional parameter introduced to improve the alignment between the calculated results and the simulation data. Consequently, the transconductance can be expressed by Equation (3.29).

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\alpha K V_{DS}}{[1+\theta(V_{GS}-V_{TH})]^2} \tag{3.29}$$

Since I_D is consistently equal to half of the tail current and the bias conditions of the load transistor remain constant, keeping V_D unchanged, the value of V_S can be determined by applying the updated current-voltage relationship presented in Equation (3.14), as shown in Equation (3.30).

$$V_S = \frac{1}{2}\left[\left(V_G - V_{TH} + V_D - \frac{\theta I_D}{\alpha K}\right)\right] - \sqrt{\left(\left(V_G - V_D - V_{TH} + \frac{\theta I_D}{\alpha K}\right)^2 + \frac{4I_D}{\alpha K}\right)} \tag{3.30}$$

As a result, the drain-source voltage V_{DS} and the overdrive voltage V_{OV} can be expressed by Equation (3.31) and Equation (3.32), respectively.

$$V_{DS} = \frac{1}{2}\left[-(V_G - V_{TH} - V_D) + \frac{\theta I_D}{\alpha K} + \sqrt{\left(\left(V_G - V_D - V_{TH} + \frac{\theta I_D}{\alpha K}\right)^2 + \frac{4I_D}{\alpha K}\right)}\right] \tag{3.31}$$

$$V_{OV} = \frac{1}{2}\left[V_G - V_{TH} - V_D + \frac{\theta I_D}{\alpha K} + \sqrt{\left(\left(V_G - V_D - V_{TH} + \frac{\theta I_D}{\alpha K}\right)^2 + \frac{4I_D}{\alpha K}\right)}\right] \tag{3.32}$$

Hence, transconductance g_m is expressed as shown in Equation (3.33):

$$g_m = \left(\frac{\alpha K}{2} - \theta^2 I_D\right) \cdot \sqrt{\left(\left(V_G - V_D - V_{TH} + \frac{\theta I_D}{\alpha K}\right)^2 + \frac{4I_D}{\alpha K}\right)}$$

$$- \left(\frac{\alpha K}{2} + \theta^2 I_D\right) \cdot (V_G - V_{TH} - V_D) - \frac{3\theta I_D}{2} - \frac{\theta^3 I_D^2}{\alpha K} \tag{3.33}$$

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When active inductors are utilized as the load, the load resistance at low frequencies mirrors the characteristics of a diode-connected transistor. Based on the required gain range and dB-linear error, the sizes of transistors M4 and M5 can be established.

It is worth highlighting that the transconductance and output resistance exhibit complementary behaviors when represented on a dB scale, with the transconductance forming a concave curve and the output resistance forming a convex curve. As illustrated in Fig. X, when the dB-linear error of transconductance g_m is positive, the corresponding error in the total output resistance R_{total} becomes negative, and vice versa. Overall, by simultaneously adjusting the transconductance and output resistance, it is expected that the gain error can be reduced.

Next, we discuss the use of active inductors to extend the bandwidth. The high-frequency cutoff of the amplifier is typically constrained by the parasitic capacitance at the output node. As noted earlier, an on-chip inductor can be placed in series with the load resistor, creating resonance with the parasitic capacitance to achieve bandwidth extension. However, passive inductors require a considerable amount of chip area. To mitigate this problem, active inductors are introduced into the design, allowing for both area efficiency and bandwidth enhancement.

Fig. 3-10 (a) illustrates a basic active inductor implemented using a source follower, where the gate of transistor M1 is connected to a series resistor Rs. Considering the gate-source parasitic capacitance, the output impedance observed from the source node can be described by Equation (3.34) [26].

$$Z_{out} = \frac{R_S C_{gs} S + 1}{g_m + C_{gs} S} \tag{3.34}$$

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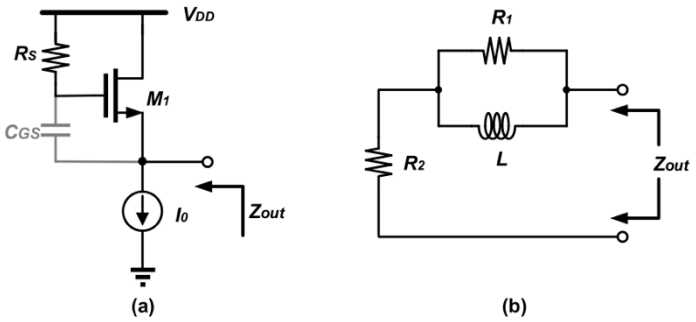

Fig. 3-10 (a) Show the inductive output generated by the source follower, while (b) presents the corresponding equivalent circuit network of (a).

When s=0, the output impedance corresponds to that of a diode-connected transistor, and as sss approaches infinity, the output impedance becomes $Z_{out}=R_S$. If $R_S \gg 1/g_m$, the circuit exhibits inductive characteristics. The output impedance can be represented as a dissipative inductor in series with a resistor, as depicted in Fig. 3-10 (b).

Where

$$R_1 = R_s - \frac{1}{g_m} \tag{3.35}$$

$$R_2 = \frac{1}{g_m} \tag{3.36}$$

$$L = \frac{C_{GS}}{g_m}\left(R_S - \frac{1}{g_m}\right) \tag{3.37}$$

A significant limitation of active inductors is their high voltage headroom requirement, which restricts their applicability in low-supply voltage environments. However, in our design, the input transistors are biased to function within the triode region rather than the conventional saturation region. Consequently, this limitation is leveraged as a benefit in our design. Moreover, to incorporate the adaptability of passive resistors, the finalized design is illustrated in Fig. 3-9. The gate voltage of transistor MN

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can be adjusted to fine-tune the series gate resistance, thereby enabling the modification of the inductance generated by the active load.

3.3.3 Design of the Fixed Gain Unit

Given that the variable gain unit exhibits wideband characteristics and utilizes transistors biased in the triode region, where the overall gain of a individual unit is relatively limited, with a significant portion of the gain range being negative. Thus, a fixed gain unit is required to enhance the total gain. The circuit architecture of the fixed gain unit is similar to that of the variable gain unit, but with the key difference being that the input differential pair is operating in the saturation region, as depicted in Fig. 3-11.

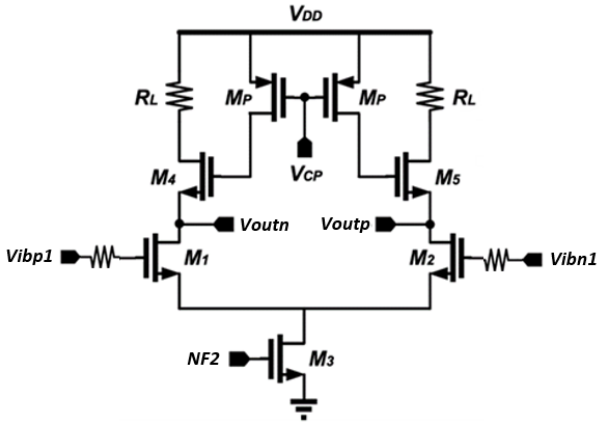

Fig. 3-11 Schematic of the fixed-gain unit

The main purpose of this circuit unit is to deliver adequate gain, thereby ensuring that the overall VGA achieves a practical gain range. To enhance low frequency gain, a passive resistor R_L is connected in series with the diode-configured load [17]. Furthermore, active inductors are employed once more to counteract the effects of parasitic capacitance. A PMOS transistor operating in the triode region functions as the peaking resistor, with its peaking level adjustable by tuning the gate voltage of the PMOS transistor.

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Fig. 3-12 illustrates the simulation results of the fixed-gain unit, demonstrating a low-frequency gain of around 15 dB and bandwidth extension achieved under acceptable peaking conditions. The active inductor is sensitive to the control voltage V_{CP} applied to the series resistor. As V_{CP} increases, the Q-factor also increases, leading to a corresponding expansion in bandwidth. This enables the circuit to adapt effectively to PVT variations.

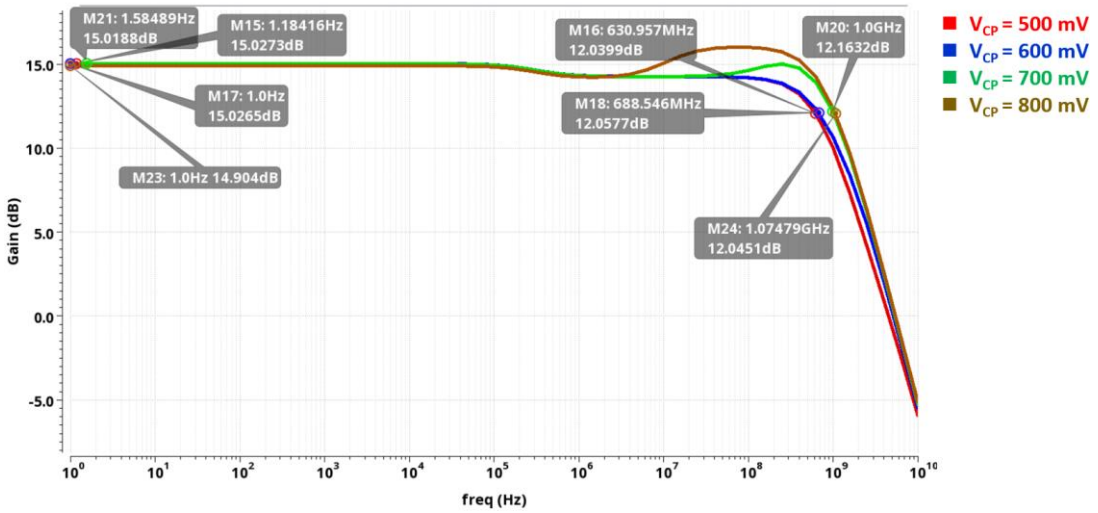

Fig. 3-12 AC response of the fixed gain unit circuit as a function of variations in V_{CP}.

3.3.4 Design of the Variable Gain Amplifier Stage

To realize a practical gain variation range, both a variable gain unit and a fixed gain unit are necessary to achieve a gain range spanning from -22.2 dB to 13.2 dB, yielding an overall gain variation of 35.4 dB. The complete circuit configuration is shown in Fig. 3-13 and is divided into two parts for discussion. The first part consists of a cascaded circuit, formed by connecting a variable gain unit with a fixed gain unit. The second part introduces a wideband output buffer, added to meet the measurement requirements.

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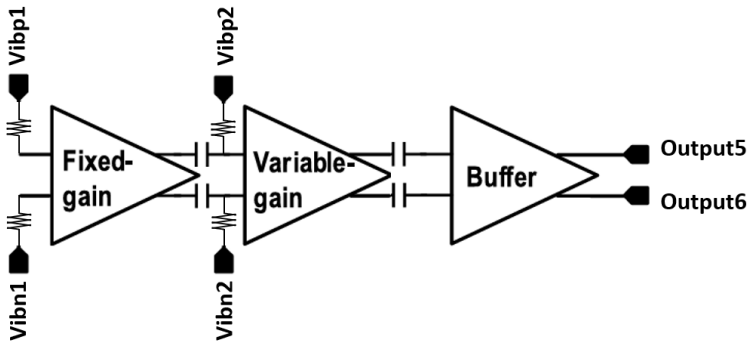

Fig. 3-13 Architecture of the overall VGA system

To begin with, we focus on the first part, which involves the design of a single-stage configuration comprising a fixed-gain unit and a variable-gain unit. Given that the input DC voltage of the variable-gain unit governs the overall gain, AC coupling through capacitors is required for these units. Although this occupies more area, it effectively addresses the DC offset issue. When comparing the variable-gain unit to the fixed-gain unit, the fixed-gain unit exhibits superior noise performance owing to its higher gain. In contrast, the variable-gain unit provides improved linearity by adjusting the gain settings to accommodate varying input power levels. Considering that the overall system noise performance is predominantly influenced by the initial stage, while linearity is determined by the final stage, the fixed gain unit is positioned ahead of the variable gain unit to optimize both the noise figure and linearity.

The differential pair M_1/ M_2 in the fixed gain unit (depicted in Fig. 3-11) operates consistently in the saturation region, with a fixed input common-mode DC voltage. In contrast, the differential pair M_6/ M_7 in the variable gain unit (shown in Fig. 3-9) is designed to operate in the triode region. Fig. 3-14 presents the simulation results under TT corner conditions, showing that M_6/ M_7 operate in the triode region when 694 mV ≤ Vctrl ≤1 V. Similarly, Fig. 3-15 depicts the simulation results for the FF corner, where M_6/ M_7 remain in the triode region for 799 mV ≤ Vctrl ≤ 1 V. Lastly, Fig. 3-16 shows the

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SS corner results, indicating that M_6/ M_7 operate in the triode region when 614 mV ≤ Vctrl ≤ 1 V. These simulations confirm that across different PVT variations, the Vctrl range required for M_6/ M_7 to operate in the triode region aligns with the Vctrl adjustment range needed to achieve the VGA's modulated gain range.

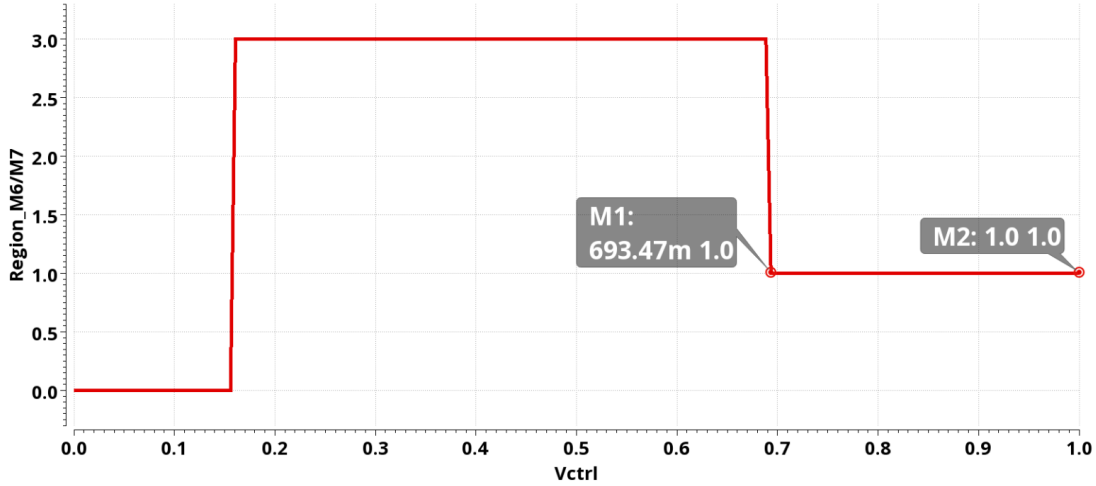

Fig. 3-14 Under the TT corner at 40°C with a supply voltage of 1 V, the DC voltage variation of Vctrl for M_6/ M_7 is analyzed.

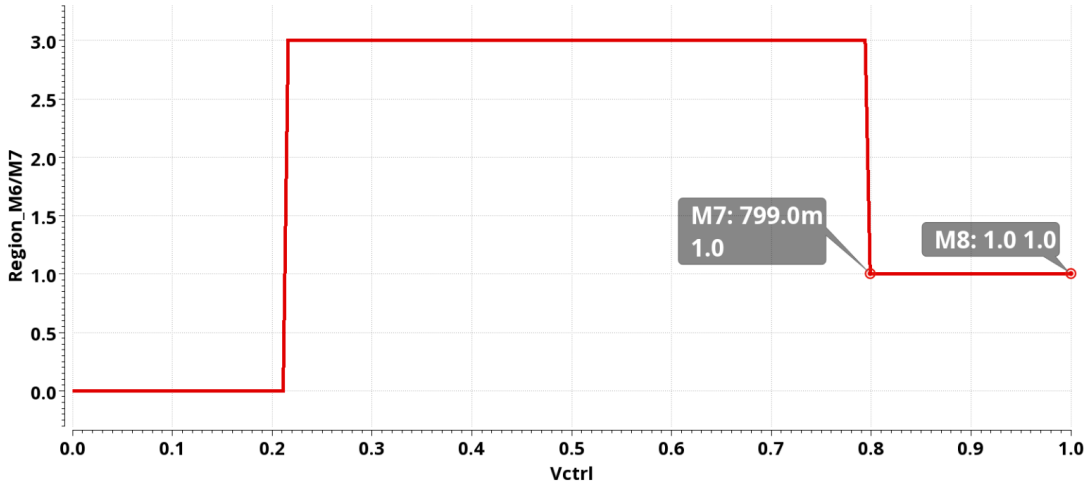

Fig. 3-15 Under the FF corner at -40°C with a supply voltage of 1.1 V, the DC voltage variation of Vctrl for M_6/ M_7 is analyzed.

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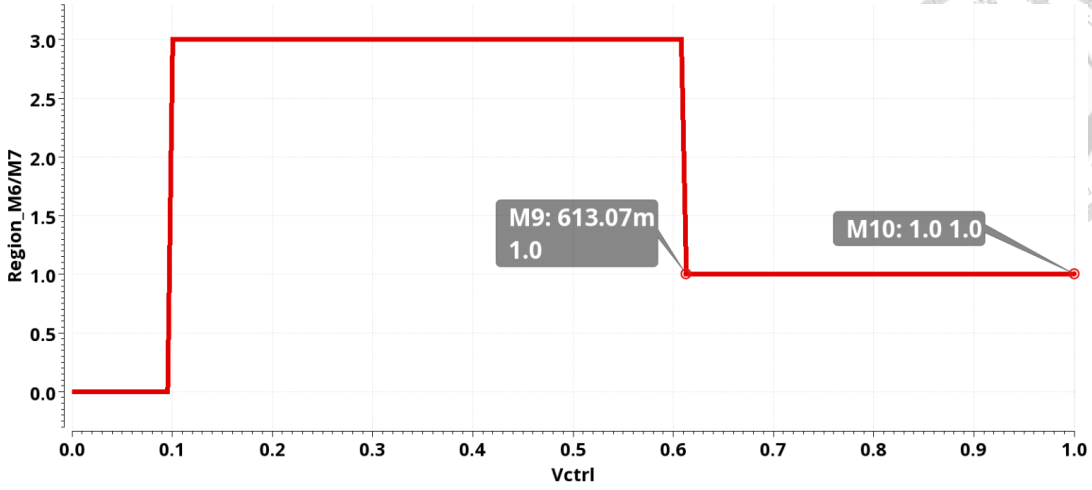

Fig. 3-16 Under the SS corner at -125°C with a supply voltage of 0.9 V, the DC voltage variation of Vctrl for M_6/ M_7 is analyzed.

When 700 mV ≤ Vctrl ≤ 1 V, the differential pair M_6/ M_7 in the variable gain unit (as shown in Fig. 3-9) consistently operates in the triode region, as illustrated in Fig 3-14. Under these conditions, the bandwidth remains approximately 1 GHz, as depicted in Fig. 3-17.

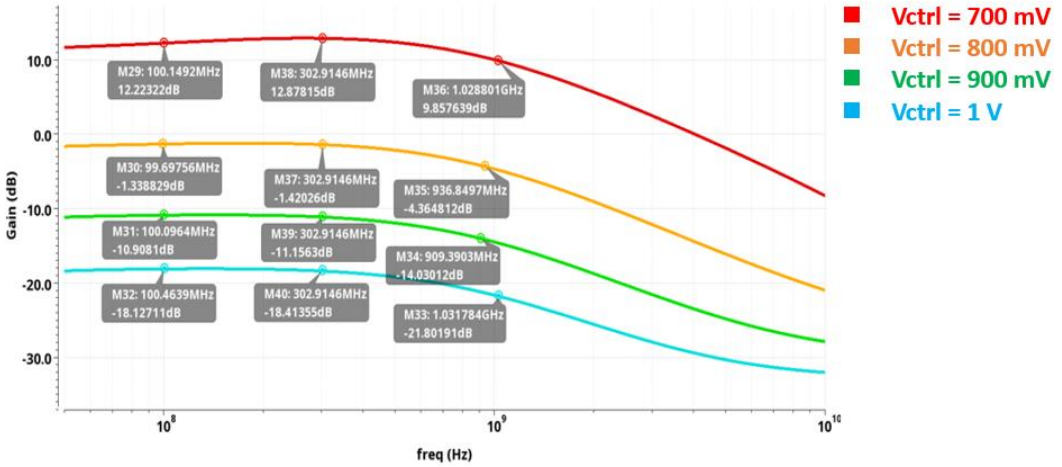

Fig. 3-17 AC response of the overall VGA architecture (as shown in Fig. 3-13) under TT corner conditions at 40°C with a supply voltage of 1V are analyzed based on variations in Vctrl.

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The simulation results, as illustrated in Fig. 3-18, demonstrate the gain variation of the variable gain amplifier as a function of the control voltage at a sampling frequency of 100 MHz. When the control voltage is 700 mV, the gain is 15.8 dB; at 800 mV, the gain decreases to 0.9 dB; at 900 mV, the gain further reduces to -10.9 dB; and at 1 V, the gain reaches -19.6 dB.

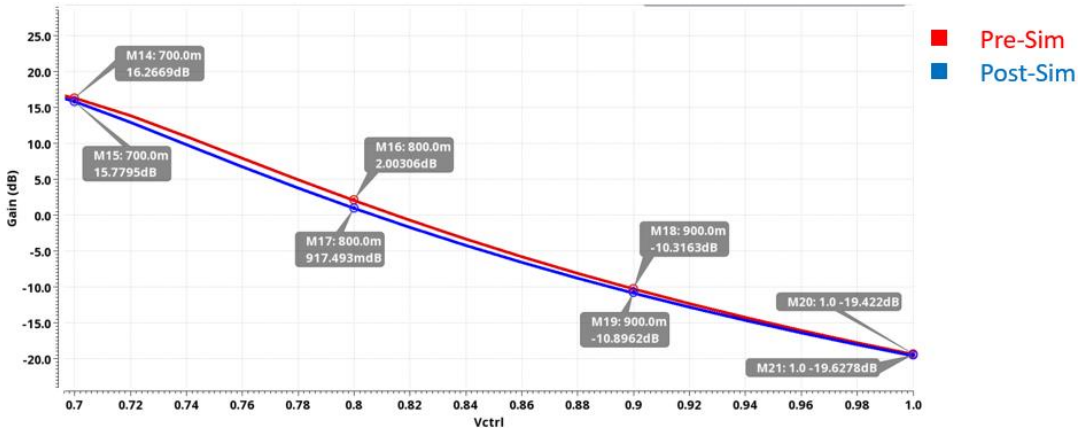

Fig. 3-18 AC response of the variable gain amplifier at a sampling frequency of 100 MHz, with the gain varying as a function of the control voltage. (Red line represents pre-simulation, blue line represents post-simulation)

The second part involves the wideband output buffer. The output buffer circuit architecture is depicted in Fig. 3-5, where the output stage is connected to a bias-Tee before being linked to the high-frequency measurement equipment, which utilizes a standard 50Ω input impedance.

Given that high-frequency testing equipment commonly operates with a standardized 50Ω input impedance, incorporating an output buffer is essential for achieving appropriate output matching and mitigating the impact of significant capacitive loading. Typically, the output buffer is configured with unity gain to guarantee a sufficiently wide bandwidth, thereby preserving the overall high-frequency cutoff.

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Additionally, the input capacitance of the buffer should be kept minimal to avoid exceeding the ability of the preceding stage to deliver sufficient drive.

The subsequent section focuses on the simulation results. As shown in Fig. 3-18, the gain of the variable gain amplifier, after passing through the buffer, varies with the control voltage at a sampling frequency of 100 MHz. When the control voltage is 700 mV, the gain is 13.2 dB; at 800 mV, the gain is -1.7 dB; at 900 mV, the gain decreases to -13.5 dB; and at 1 V, the gain further reduces to -22.2 dB.

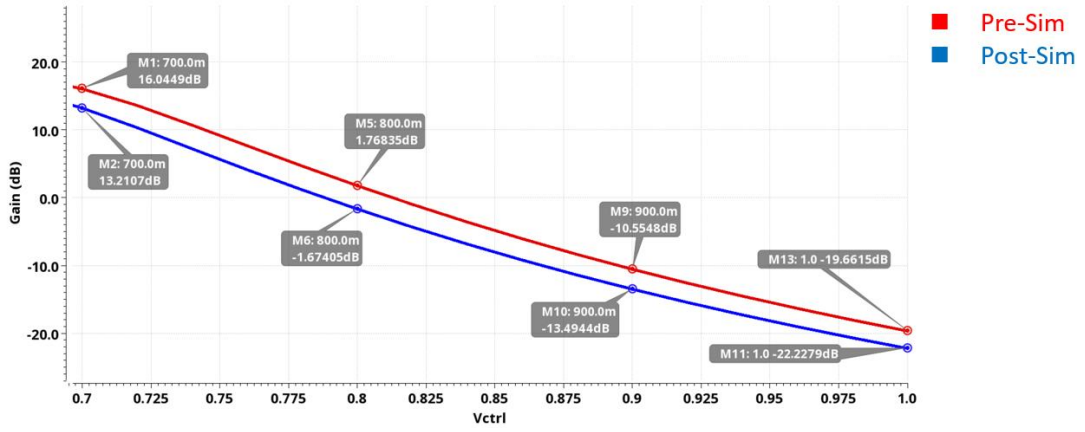

Fig. 3-19 AC response of the variable gain amplifier, followed by a buffer, at a sampling frequency of 100 MHz, with the gain varying as a function of the control voltage. (Red line represents pre-simulation, blue line represents post-simulation)

Finally, the comparison between the specifications defined in Table 3-2 and the simulation results is summarized in Table 3-6. At an operating frequency of 100 MHz, the results demonstrate that the gain variation range with respect to the control voltage, as well as the bandwidth, power consumption, and area, all meet the expected design standards.

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Table 3-6 Comparison of VGA specifications and simulation results

	Specification	**Pre-sim (TT 40°C)**	**Post-sim (TT 40°C)**
Technology	40 nm CMOS		
Operating Frequency [MHz]	100		
Supply Voltage (V)	1		
Gain Range [dB]	20	35.7	35.4
Bandwidth [GHz]	0.3	1.2	1
Power [mW]	<0.55	0.468	0.438

3.3.5 Conclusions

This paper presents the design of a wideband variable gain amplifier (VGA) featuring accurate dB-linear performance. To achieve a bandwidth of up to 1 GHz, an inductor-less approach is employed, utilizing non-saturated transistors to realize a variable gain range greater than 40 dB. This approach addresses dB-linear gain inaccuracies while streamlining the overall design. To validate the design concept, the proposed VGA was implemented using a standard 40 nm CMOS process and evaluated via on-wafer probing. The simulation results align well with the measurement results. Thus, the proposed design methodology is both straightforward and efficient, making it well-suited for VGA implementations targeting high-speed analog signal processing applications

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Chapter 4 Experimental Result of Proposed Analog Front-End Control Circuit

This chapter discusses the measurement results of the analog front-end circuits, including the die photo, measurement environment setup, Printed Circuit Board (PCB), and a discussion of the measurement results.

4.1 Die Photo

This work is fabricated in TSMC 40-nm process technology. The total chip area, including PAD regions, measures 1.109 mm² × 1.011 mm². The core circuit area, which encompasses the output buffer, occupies 0.046 mm², as illustrated in Figure 4-1.

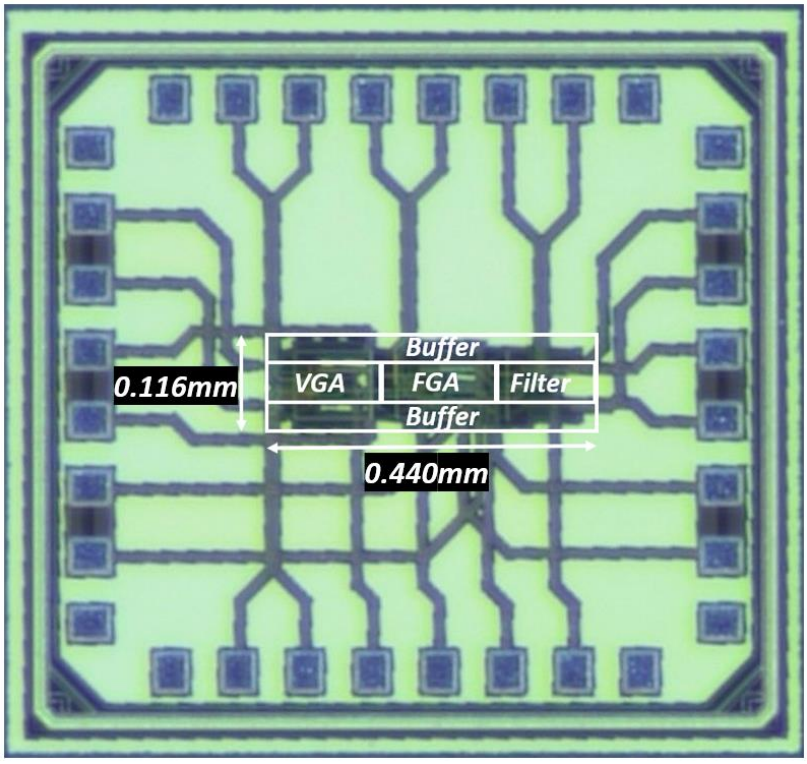

Fig. 4-1 Die photos of the analog front-end control circuit.

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4.2 Measurement Environment Setup

The chip was bonded to a custom-designed PCB using bonding wires for measurement purposes, with additional external components integrated to evaluate steady-state and transient responses as well as spectrum analysis. The measurement setup involved the use of instruments including a power supply, oscilloscope, signal generator, digital multimeter, and spectrum analyzer.

The measurement setup is illustrated in Fig. 4-2. First, for the DC bias voltage is supplied by the Agilent E3646A power supply and is further regulated and adjusted using a Low Dropout Regulator (LDO). A variable resistor is used to fine-tune the regulator's output voltage, ensuring a stable and precise voltage supply to the chip. The Keysight 34470A digital multimeter is employed to verify the bias voltage at each PAD of the chip. For the AC input signal, The Agilent E4438C signal generator produces the required operating frequency for the circuit. This single-ended signal is AC-coupled through a balun transformer, with additional DC bias applied to ensure that VIN and VIP share the same DC voltage. This configuration guarantees that VIN and VIP are perfectly out of phase.

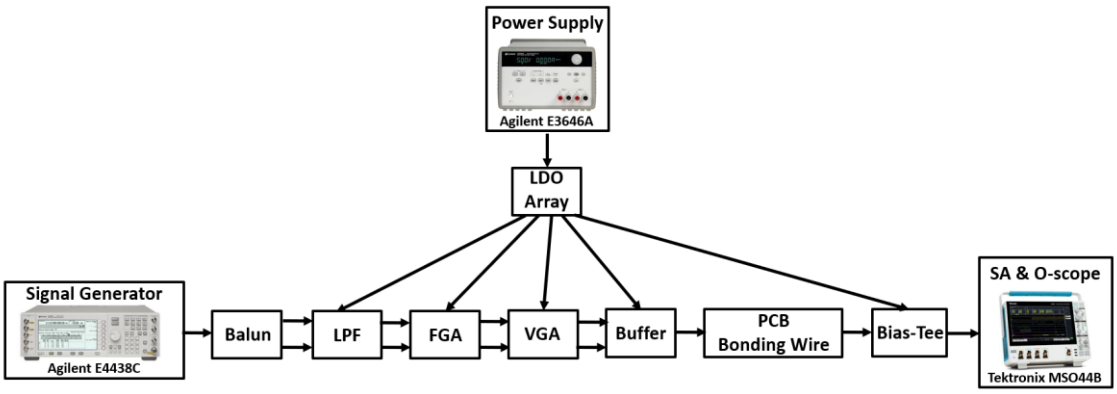

Fig. 4-2 Measurement setup.

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Next, for the output measurement, the output of the chip is first connected to a Bias-Tee, ensuring proper transmission of the RF signal. The Bias-Tee effectively separates the DC and RF components, allowing accurate signal delivery to the Tektronix MSO44B oscilloscope and spectrum analyzer. The output signals are then analyzed using both instruments to evaluate their time-domain and frequency-domain characteristics.

4.3 PCB Board

As shown in Fig. 4-3, a printed circuit board (PCB) was developed to test and verify the functionality of the proposed SSF-based filter and VGA. The PCB features a single power domain, supplying 1 V to the analog circuits. The signal generated by the signal generator is converted into a fully differential sine wave through a balun and fed into the chip via an SMA connector. Fig. 4-4 illustrates the actual measurement setup employed in this work.

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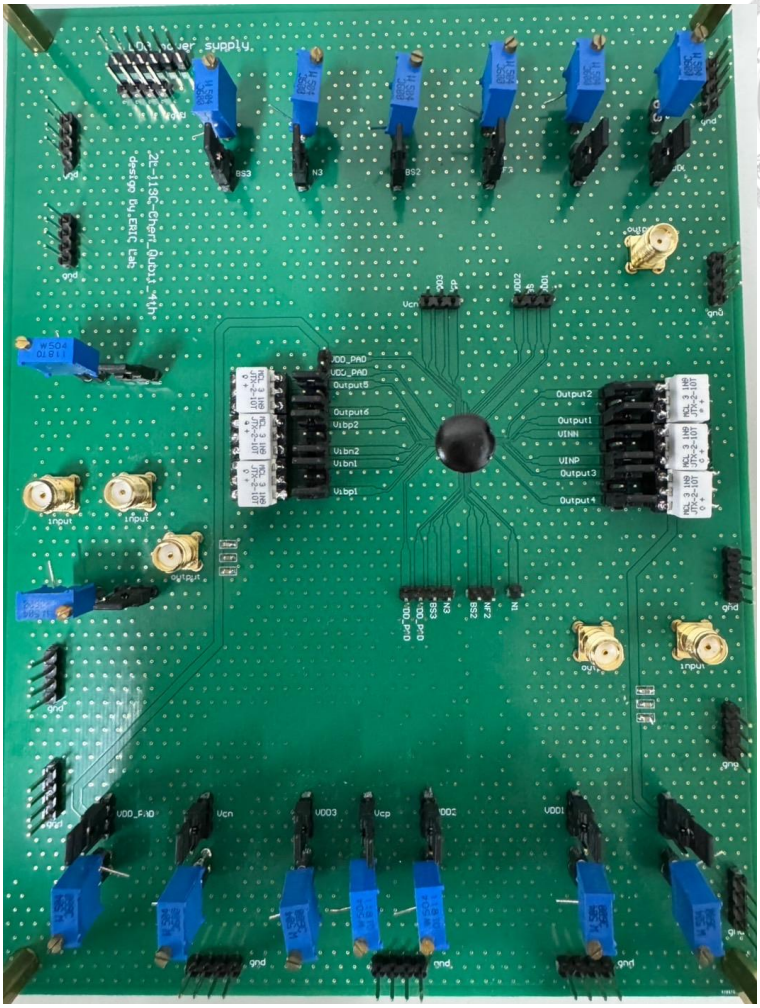

Fig. 4-3 PCB board.

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Fig. 4-4 Measurement environment.

4.4 Measurement Results

4.4.1 Measurement Results of the SSF-Based Filter

Fig. 4-5 illustrates the relationship between gain and frequency under an input voltage of 200 mV_{PP}, comparing the post-simulation results (black line) with the measured data (red line). The horizontal axis represents frequency (Hz), ranging from 100 MHz to 1 GHz, while the vertical axis denotes gain (dB), spanning from approximately -5 dB to -25 dB.

Several key data points are highlighted in the figure: At 100 MHz, the post-simulation gain is -4.9 dB, whereas the measured gain is slightly higher at -4.4 dB. At 360 MHz, which represents the measured bandwidth, the gain decreases to -7.4 dB, exhibiting a more rapid attenuation trend compared to the post-simulation results. At 400 MHz, which corresponds to the post-simulated bandwidth, the gain reaches -7.5 dB.

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Beyond 400 MHz, the measured gain (red line) declines at a steeper rate than the post-simulation results and exhibits noticeable deviations and fluctuations.

The results suggest that while the simulated and measured responses match closely at lower frequencies, discrepancies arise as frequency increases, likely due to parasitic effects, process variations, or unmodeled losses in the physical implementation.

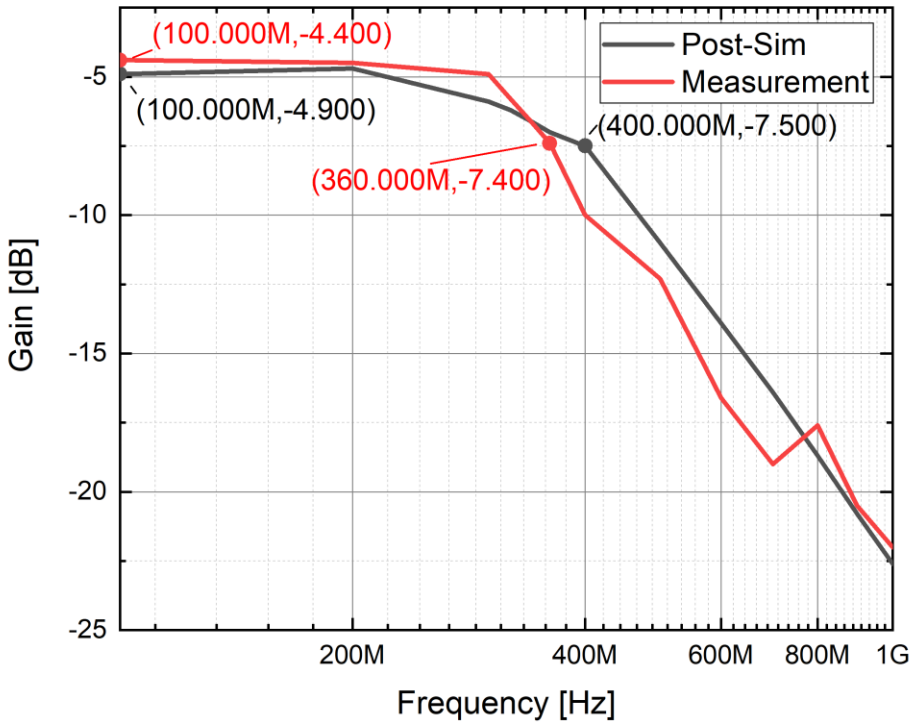

Fig. 4-5 Frequency response of the SSF-Based filter

Fig. 4-6 presents the measured results of the 1 dB compression point (P1dB) under a 100 MHz input signal condition. This figure illustrates the relationship between gain (dB) and input voltage (mVpp), comparing the post-simulation results (black line) with the measured data (red line).

At an input voltage of 100 mVpp, the post-simulation gain is -4.8 dB, whereas the measured gain is -4.6 dB, indicating a slight deviation. As input voltage increases, both

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curves exhibit gain compression. When the input voltage reaches 424 mVpp, the measured gain drops to -5.5 dB, marking its 1 dB compression point (P_{1dB}). Conversely, in the post-simulation results, the gain decreases to -5.8 dB at 450 mVpp, corresponding to its P_{1dB}.

The discrepancy in P_{1dB} between the measured and simulated data indicates that the measured circuit reaches gain compression at a lower input voltage compared to the post-simulation results. These variations may stem from process deviations, device mismatches, or unmodeled parasitic effects in the actual circuit implementation.

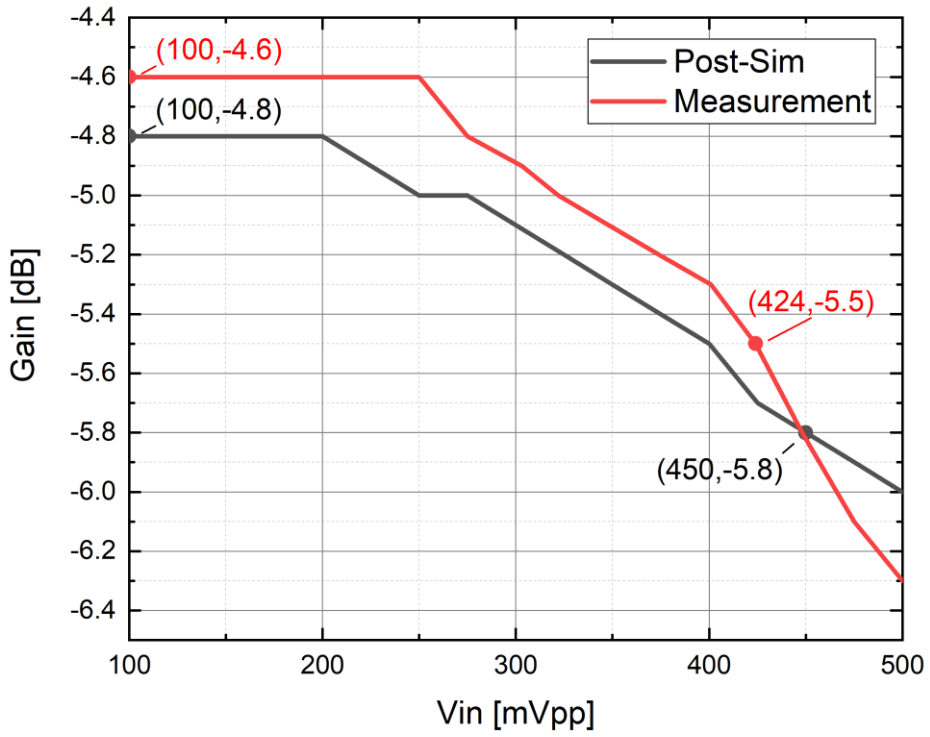

Fig. 4-6 1 dB compression point－input signal @100 MHz

Fig . 4-7 presents the spectrum analysis of output noise, comparing post-simulation results (black line), measured results (red line), and instrument noise floor (blue line) across a frequency range from 1 MHz to 1 GHz. At low frequencies (1M - 10M Hz), the

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measured noise is significantly higher than both post-simulation and instrument noise, indicating the presence of flicker noise (1/f noise). At mid frequencies (1 – 10 MHz), the measured noise gradually converges with the post-simulation results. At higher frequencies (>100 MHz), both the measured and simulated noise exhibit a relatively stable trend with some fluctuations.

Measured noise is higher than post-simulated noise, particularly at low frequencies, likely due to additional flicker noise effects in the actual circuit. The post-simulated noise curve is lower than the measured noise curve but follows a similar trend, suggesting that the simulation model accurately predicts noise behavior at higher frequencies. Instrument noise is significantly lower than both measured and simulated noise, confirming that the observed noise is from the circuit itself rather than from spectrum analyzer limitations.

In summary, the flicker noise effect in the low-frequency range (1 – 10 MHz) is more pronounced than predicted by post-simulation, suggesting the potential influence of process variations, layout effects, or device mismatches in the actual circuit. In the high-frequency range (>100 MHz), the measured and post-simulation results exhibit a similar trend, indicating that thermal noise is the dominant noise source in this region, and the simulation results demonstrate higher accuracy.

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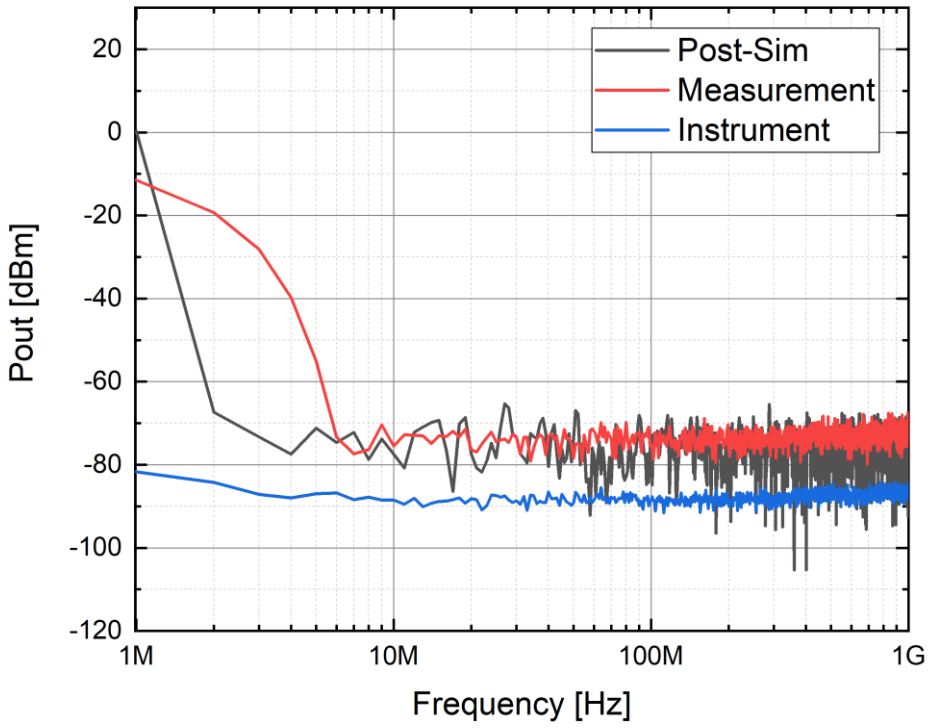

Fig. 4-7 Spectral Analysis of Noise

Table 4-1 presents a comparison of key parameters between post-simulation and measurement results for the SSF-based filter, including gain, bandwidth, the 1 dB compression point (P_{1dB}), and power consumption.

Overall, the measured results for gain and power consumption closely align with the post-simulation results, indicating a certain degree of accuracy in the design model. However, bandwidth and P_{1dB} are lower than the simulated values, which may be attributed to process variations, device mismatch errors, or unmodeled parasitic effects.

In general, the measured results exhibit a consistent trend with the simulation data; however, discrepancies remain in high-frequency performance and nonlinear regions (P_{1dB}). This suggests that further model refinement or design adjustments could improve prediction accuracy.

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Table 4-1 SSF-based filter parameters measurement

	Post-sim	Measurement
Gain (in 100 MHz) [dB]	-4.9	-4.4
Bandwidth [MHz]	400	360
P_{1dB} [mVpp]	450	424
Power [mW]	0.057	0.052
Total Ouput Noise [dBm] (1M to 1GHz)	-67.5	-57.7

4.4.2 Measurement Results of the VGA

Fig. 4-8 presents the measured frequency response of the Variable Gain Amplifier (VGA) at an input frequency of 100 MHz, comparing the experimental results with the simulated data. The simulation results indicate that when $V_{ctrl} = 0.7$ V, the VGA achieves a gain of approximately 13.2 dB, which decreases to -22.2 dB when $V_{ctrl} = 1$ V, demonstrating a wide gain tuning range. However, the measured results reveal that the gain varies only within the range of -4.4 dB to -6.9 dB, indicating that the VGA fails to achieve the expected gain modulation effect.

This indicates that the actual implementation of the VGA does not achieve gain modulation as intended in the design, which may be attributed to the influence of the testing environment, process variations, or circuit design limitations. First, the testing environment could be a contributing factor, where biasing conditions or instrument calibration errors may impact the proper operation of the VGA. Additionally, external parasitic effects or poor load matching could introduce unintended signal attenuation.

Second, process variations may also play a role, particularly fluctuations in the threshold voltage, which can affect transistor operating conditions and consequently alter gain control behavior. Furthermore, device mismatch errors could impair the internal gain adjustment mechanism of the VGA, leading to a reduced modulation range.

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Finally, circuit design constraints may limit gain control effectiveness. Specifically, the gain control mechanism might fail to efficiently regulate the transconductance of the VGA, preventing a significant change in gain. Additionally, parasitic capacitance effects could weaken the influence of control signals on the circuit, thereby restricting the VGA's ability to achieve proper gain modulation. Further analysis and circuit optimization are required to enhance the accuracy of gain control and improve the overall performance of the VGA.

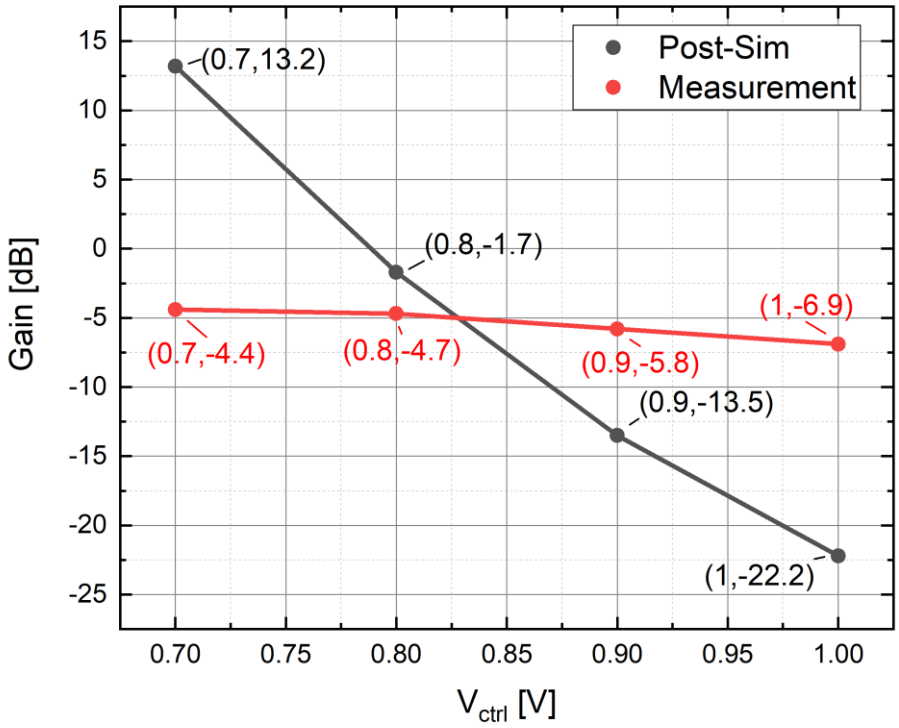

Fig. 4-8 Frequency response of the VGA—input signal @100 MHz

4.4.3 Comparison Table

Tables 4-2 and 4-3 present comparisons between the proposed SSF-based filter and VGA with state-of-the-art circuits, respectively. Since the measurement results represent only a partial outcome of the study, the comparisons are based on post-simulation results.

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Table 4-2 Comparison table of proposed SSF-based filter (post-simulation)

	TCASI'09 [5]	**JSSC'06 [6]**	**JSSC'06 [7]**	**ISSCC'08 [8]**	**ESSCIRC'10 [9]**	**JSSC'15 [10]**	**This Work**
Technology [nm]	180	130	180	130	40	180	40
Topology	Active-RC	Gm-C	SF-C	SF-C	Active-RC	SSF-C	SSF-C
Order	5	4	4	6	5	4	2
DC Gain [dB]	0	4	-3.5	0	0	-2	-4.8
Bandwidth [MHz]	300	11	10	280	880	33	400
SNR [dB]	56.6	81	79	-	-	70	42.8
THD [dB]	-40	-40	-40	-	-	-40	-50.4
Power [mW]	54	14.2	4.1	0.12	27.5	1.38	0.057
Area [mm^2]	0.63	0.9	0.43	0.06	0.039	0.14	0.012

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Table 4-3 Comparison table of proposed VGA (post-simulation)

	JSSC'13 [12]	**JSSC'15 [13]**	**TCAS-I'06 [14]**	**TMTT'16 [15]**	**TCAS-I'20 [16]**	**This Work**
Technology [nm]	65	180	180	65	65	40
Type	Tune g_m	Manipulate R_L	Tune g_m	Manipulate R_L	Tune g_m	Tune g_m
Gain Range [dB]	76 (-13~63)	38.6 (1.6~40.2)	95 (-52~43)	22 (2~24)	40 (-19~21)	35.4 (-22.2~13.2)
Bandwidth [GHz]	0.0148	0.149	1.05	2.2	4	1
Power [mW]	3.84	0.74	6.5	3.48	3.5	0.438
Area [mm^2]	0.01	0.034	0.4	0.01	0.012	0.034
FoM	29.3	228.6	38.4	1390.8	3809.5	2377.1

$$FOM = \frac{Bandwidth\ [GHz] * dB - linear\ Gain\ Range\ [dB]}{Power\ [mW] * Active\ Area\ [mm^2]}$$

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4.4.4 Discussion and Summary

This study evaluates the performance of the SSF-based filter and the VGA with self-compensated transistors and active inductors, comparing measurement results with simulations.

The SSF-based filter exhibits measured gain and power consumption close to simulations, validating the accuracy of the design model. However, bandwidth and P_{1dB} are lower than expected, likely due to process variations, component mismatches, or unmodeled parasitic effects.

The VGA demonstrates a significantly reduced gain tuning range compared to simulations, with measured gain varying only between -4.4 dB and -6.9 dB. This discrepancy may be attributed to biasing conditions, process variations, or circuit design limitations, preventing effective gain modulation.

While the proposed circuits show advantages in power efficiency and area, further optimization is required to improve gain control. Future work should focus on model refinements and circuit enhancements to improve accuracy and ensure suitability for high-performance applications.

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Chapter 5 Conclusions and Future Works

5.1 Conclusions

This thesis presents the design and implementation of an analog front-end control circuit for qubit control, fabricated using TSMC 40-nm CMOS technology. The proposed system incorporates a Super-Source-Follower SSF-based filter and a Variable Gain Amplifier, both optimized for high-fidelity signal processing, low power consumption, and wide bandwidth operation in cryogenic environments.

The SSF-based filter was designed to achieve a second-order low-pass transfer function with a -3 dB bandwidth of 400 MHz. The pseudo-differential architecture effectively eliminates the need for a common-mode feedback circuit, leading to improved power efficiency and enhanced linearity. Measurement results indicate that the implemented filter maintains a SNR of 42.8 dB and a THD of -50.4 dB under a 1 V power supply, confirming the effectiveness of the SSF topology in meeting stringent performance requirements for quantum applications.

The VGA utilizes self-compensated transistors and active inductors to extend bandwidth and maintain precise dB-linear gain characteristics. The amplifier demonstrates a gain variation range of 35.4 dB, with operation extending up to 1 GHz. The power consumption remains as low as 0.438 mW, making it well-suited for low-power cryogenic applications. Experimental verification was conducted using a custom-designed PCB, with the chip bonded via wire bonding. Measured performance closely aligns with post-simulation results, validating the proposed circuit methodologies.

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Overall, the results confirm that the designed analog front-end meets the demanding specifications for qubit control. The combination of an SSF-based filter and a dB-linear VGA successfully achieves high fidelity, wide bandwidth, and low power consumption, demonstrating the viability of the proposed architecture for scalable quantum computing applications.

5.2 Future Works

Further research improvements for this chip are listed below:

1. Extended Cryogenic Characterization: Although the design is optimized for cryogenic operation, more extensive measurements at temperatures below 4 K are required to fully understand the impact of cryogenic effects on transistor behavior and overall circuit performance.

2. Integration with Quantum Control Systems: Future research can explore direct integration with quantum processor architectures, enabling a more seamless interface between the control electronics and qubit arrays. The development of custom packaging and interconnect solutions will be essential to minimize parasitic effects at cryogenic temperatures.

3. Technology Scaling and Advanced Process Nodes: The circuit was fabricated using a 40-nm CMOS process. Future designs may leverage more advanced process nodes (e.g., 22 nm or FinFET technologies) to achieve further reductions in power consumption and area while maintaining or improving performance.

4. Exploration of Alternative Topologies: Beyond SSF-based filters and self-compensated VGAs, alternative topologies such as gm-C filters and digital-intensive VGA implementations could be explored to optimize energy efficiency and scalability for large-scale quantum computing systems.

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