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金氧半穿隧二極體之暫態電流行爲

Transient Current Behavior in MIS Tunnel Diodes

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金氧半穿隧二極體之暫態電流行為

Transient Current Behavior in MIS Tunnel Diodes

本論文係黃崧瑋(F09943059)在國立臺灣大學電子工程學研究所完成之博士學位論文，於民國 113 年 5 月 10 日承下列考試委員審查通過及口試及格，特此證明。

The undersigned, appointed by the Graduate Institute of Electronics Engineering on 10 May 2024 have examined a Doctoral Dissertation entitled above presented by Sung-Wei Huang (F09943059) candidate and hereby certify that it is worthy of acceptance.

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故事的開始多半只是個不經意的瞬間，然而總要過後才看的明白。大學畢業之後原本沒有念博的打算，而研究所第一年某天隨竹哥到卓越拿光罩，閒談間問起研究目標，你說要將元件翹翹板電流現象和邊緣場效應用數學模型加以解釋，而彼時甚至都還無法在模擬當中重現這一現象。當時我心中有些嗤笑，卻又不禁被這遠大抱負所震懾。自此我便時常重新審思自己該如何度過研究所這段時光，是得過且過抑或是濃墨重彩；或許可以說，我後續簽博、埋首研究，都是這件小事的漣漪。

往事如煙，有些卻清晰地難忘。2021 年 5 月 14 日，對準完厚薄氧後踏出無塵室已過了 8 時，同林俊諭驅車初訪校門口的金牛座平價牛排，餐後又返回實驗室鍍鋁至深更。彼時疫情四起，人心惶惶，我們也惴惴地做著沒有明天的製程。隔日一早又回黃光室對準時，卻收到新增 180 人確診、雙北升三級警戒的消息，我和林俊諭決定暫罷製程盡快返鄉。而 JC 則是要繼續留在台北，你說，逃竄的人群好像電影裡才有的情節，此刻在亂流中你覺得自己才眞正的活著。等我 7 月中重新返校時，一切安好如初，想再回味金牛座的酥皮濃湯，卻

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發現其已然歇業。滄海桑田，不勝唏噓。而那批元件後來終究也沒有做完，甚至不知所蹤，顯得先前的辛苦有些徒勞，但他卻承載了超越研究意義的感觸。若後來者在我的盒中找到幾片曝光完卻沒鍍背面鋁的 wafer，請不要過分奇怪，於我，那是劃分疫情時代前後的象徵和並不如煙的一段往事。

雖說這四年在研究上可謂順風順水，心中卻總是暗潮洶湧。由衷感謝冠竹、軒毅、綺憶、俊億先後消化了我研究的負能量，興許你們從不理解我的憂心和抱怨，但或許就是這種不在意的態度才使我漸漸放下心中的執念。尤其特別感謝我師父引我領悟了研究更普世的定義，往後還有更多要向你取經。

感謝實驗室諸位學長姐和學弟妹。謝謝帶我第一學期專題的劉宇恆學長、教會我模擬的陳昱諠學姐。謝謝帶我第二學期專題的陳柏均學長、不厭其煩教我製程的楊詠竣學長、研究模範江子豪學長、陪我打球的許庭昊學長，以及在研究方方面面幫襯著我的林冠文學長，未來還要繼續仰仗你了。謝謝大學同屆竹哥、建宇、人豪、琛云，大家夥兒在白板上爭辯著研究的往日還歷歷在目，那是我第一次感受到研究的快樂可以那麼簡單又純粹。謝謝研究所同屆林俊諭、JC、林彥瑜，你們陪我走過了研究路上最辛苦難熬的時光，一起在無塵室奮戰的日子永遠難忘。謝謝高博分攤了許多實驗室雜事，你是很可靠的大學姐，謝謝軒毅、舜啓、祐德、郁芹的兩年相伴。謝謝牢不可破的聯盟：機台之神賢哥和暫態大師俊億學長，以及 IEDM 的其他成員：威騏、Joan 姐、老龔、老蔡，很開心博班最後一年有你們在。也謝謝曾一同共事的藍柏皓、王文彥、陳羿融、黃冠霖、林暐城、施惠馨，祝你們前程似錦。

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再回首，四年匆匆，向著不知爲何的未來前進，有所執著、有所收穫；有時像在空無一人的黑暗中吶喊，有時也綻放出煙花般的絢爛。或許這有如人之一生：在虛無當中尋找著意義。而路漫漫其修遠兮，吾將上下而求索。

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摘要

本篇博士論文深入探討了鋁/二氧化矽/p 型矽組成的金屬-氧化層-半導體穿隧二極體（金氧半穿隧二極體）中的暫態電流行爲。透過施加不同極性的寫入電壓並以相同電壓讀取，我們發現金氧半穿隧二極體之閘極可讀取到不同極性的暫態電流，可作爲動態記憶體之雙態使用。論文前段主要聚焦於平面金氧半穿隧二極體的研究，通過大量實驗數據，我們評估了寫入電壓程式的極性、大小、持續時間及元件氧化層厚度對毫秒時間尺度下暫態電流的影響。實驗中發現，正向寫入電壓增加時，暫態電流會出現飽和現象，這可歸因於在從寫入電壓切換到讀取電壓的瞬間有大量多數載子電洞流入半導體中與儲存的少數載子電子做快速復合。我們透過 TCAD 模擬深入分析了在整個暫態過程中、包括了毫秒尺度之前的載子運動，並根據電洞流動方向將其分爲三個時期：介電層弛豫期、電洞排出期和漂移復合期。我們進一步將漂移復合期這一過程建模，所得模型成功預測暫態電流之飽和電壓，模型分析與 TCAD 模擬結果的偏差僅爲 0.01 伏。

爲提高暫態電流性能，我們探索了薄金屬環繞閘極與氧化層局部薄化等特殊結構。薄金屬環繞閘極金氧半穿隧二極體實現了相較於最佳平面金氧半穿隧二極體 4.5 倍的暫態電流提升，歸因於薄金屬橫向電阻所造成環繞閘極底下儲存之電子產生的延遲效應。而通過在深空乏條件下施加電應力下引發介電層軟崩潰，可創造出氧化層局部薄化之金氧半穿隧二極體，其暫態電流性能比最佳平面結構提高了 20 倍，這是由於氧化層局部薄化區域的高穿隧機率會使半導體側在寫入時大量缺少電子，在讀取時將有極強的電子電流流經此一氧化層局部薄化區來補足這一缺額，使得暫態電流大幅提升。

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在本論文的附錄中，我們藉助模擬深入探討了氧化層電荷對於平面金氧半穿隧二極體之暫態電流的影響。氧化層電荷會在元件外形成空乏區，加快儲存電子的復合速率，顯著降低毫秒時間尺度的暫態電流。此外，當氧化層電荷較多時會在元件外吸引電子，若施加較大的閘極寫入電壓，將導致元件外部電子匱乏，讀取時需透過載子生成來補充電子，從而產生反向暫態電流。

關鍵字： 金氧半穿隧二極體；金氧半電容；動態記憶體；暫態電流；暫態行爲；介電層軟崩潰；解析模型。

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Abstract

This dissertation investigates the transient current behavior in Al/SiO_2/Si(p) metal-insulator-semiconductor tunnel diodes (MIS tunnel diode, MISTD). By applying write voltages of different polarities and reading at a constant voltage, we discovered that the gate of the MISTD can detect transient currents of varying polarities, which can serve as the two states for dynamic memory applications.

The initial part of the dissertation focuses on the Planar MISTD. Using extensive experimental data, we discussed the impact of write voltage polarity, write voltage magnitude, write time, and the oxide layer thickness on the transient current at the millisecond time scale. We observed that with an increase in positive write voltage, the transient current reaches a saturation point. This saturation is attributable to the rapid recombination of holes flooding into the semiconductor with the stored minority carrier electrons upon switching to the read voltage. Through TCAD simulations, we analyzed the movement of carriers during the transient process in the sub-millisecond regime, classifying the motion of holes into three periods: dielectric relaxation period, hole depletion period, and diffusion and recombination period. We further modeled the transient current during the diffusion and recombination period, finding that the modeling results aligned closely with the TCAD simulation results. Additionally, our model successfully predicted the saturation voltage of the transient current, deviating from the TCAD simulation results by only

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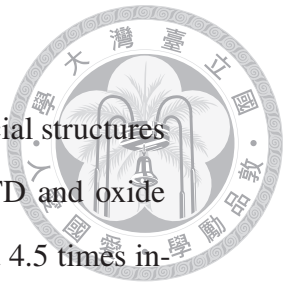

0.01 volts.

To enhance transient current performance, we explored special structures such as the ultra-thin metal surrounded gate (UTMSG) MISTD and oxide local thinning (OLT) MISTD. The UTMSG MISTD achieved a 4.5 times increase in transient current compared to the best Planar device, due to the edge late response effect of the electrons under the surrounding gate caused by the lateral resistance of the thin metal. On the other hand, inducing dielectric soft breakdown under deep depletion stress created an OLT MISTD, which improved transient current performance by 20 times compared to the best Planar device. This improvement is due to the high tunneling probability in the locally thinned oxide region, leading to a significant electron deficiency on the semiconductor side during the write procedure. During reading, a strong electron current flows through this thinned oxide area to compensate for the deficiency, significantly boosting the transient current.

In the appendix, we further explore the impact of oxide charges on the transient current of Planar MISTD through simulations. The presence of oxide charges forms a depletion region outside the gate area, accelerating the recombination of stored electrons and significantly reducing the transient current at the millisecond scale. Moreover, an abundance of oxide charges will induce inversion electrons outside the device, leading to an electron deficiency when a larger gate write voltage is applied. During reading, this deficiency necessitates electron supply through carrier generation, thus forming a reverse transient current.

Keywords: MIS tunnel diode; MIS capacitor; Dynamic memory; Transient current; Transient behavior; Dielectric soft breakdown; Analytical model.

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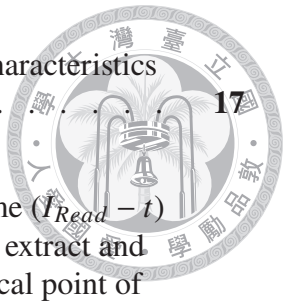

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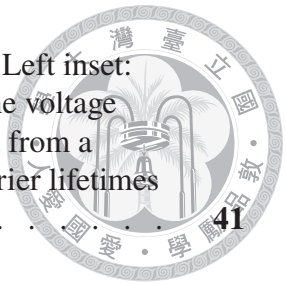

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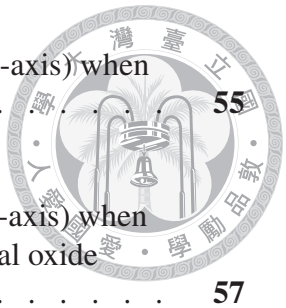

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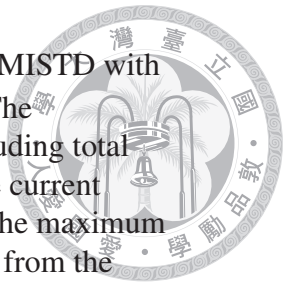

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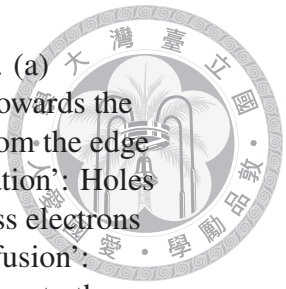

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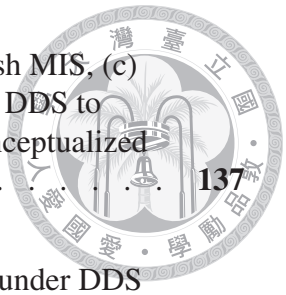

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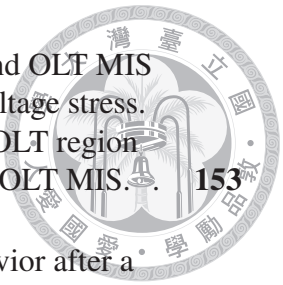

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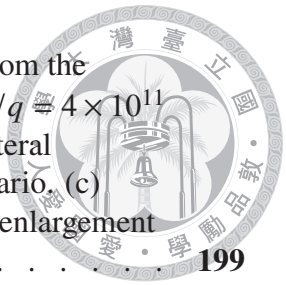

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1

Introduction

1.1 Motivation

The 21st century stands as the era of technology, with electronic technology taking a prominent role. Various electronic devices in our daily lives rely on integrated circuit chips for control, underscoring their undeniable significance. Beyond the perspective of commerce that, the incessant demand for chips is poised to propel the continued flourishing of the semiconductor industry, Miller's "Chip war: the fight for the world's most critical technology," published in 2022 [1], posits that a nation's prowess in the realm of

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chips significantly influences its international standing, as chip capabilities have fundamentally become a crucial component of national defense.

Within the intricate web of relationships in the semiconductor industry's upstream and downstream sectors, chip manufacturing stands as an indispensable link. The production of nanoscale devices necessitates the use of exceedingly costly precision instruments, elevating the barriers to entry and consolidating the market share of advanced chip manufacturing. However, this does not imply stagnation in semiconductor manufacturing technology; on the contrary, the competition in advanced chip manufacturing is only intensifying.

Due to the rapid development of artificial intelligence and the Internet of Things, the demand for computational power has far surpassed previous levels. According to the renowned Moore's Law proposed by Intel' s co-founder Gordon Moore [2,3], the computational power of a unit area of a chip doubles approximately every 18 months. This relies heavily on continually shrinking the size of devices to accommodate more devices per unit area. As the core component in integrated circuits, the metal-oxide-semiconductor field-effect transistor (MOSFET) inevitably undergoes a reduction in size, accompanied by a decrease in the thickness of the gate oxide layer.

When the physical thickness of the gate oxide layer is reduced to less than 4 nanometers, an unavoidable quantum tunneling phenomenon occurs [4–8]. This results in an additional leakage current passing through the originally insulating oxide layer, leading to a decline in the performance of the device and an increase in power consumption.

Simultaneously, harnessing the quantum tunneling effect could prove beneficial in designing emerging electronic devices for specialized applications beyond the scope of

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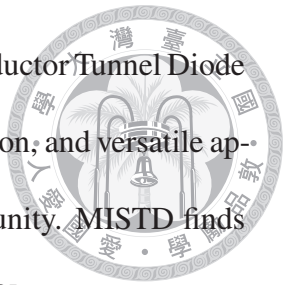

Moore's Law [2,3]. One such example is the Metal-Insulator-Semiconductor Tunnel Diode (MISTD), known for its simple structure, cost-effectiveness in fabrication, and versatile applications, capturing significant attention within the academic community. MISTD finds application in a wide array of devices, including photodetectors [9–19], temperature sensors [20–26], strain sensors [27–29], gas sensors [30–36], solar cells [37–44], transistors [45–50], logic gates [51], negative differential resistance and transconductance [52–55], non-volatile memories [56–61], and more.

However, past literature has predominantly focused on the steady-state electrical characteristics of these devices, with limited research on the transient behavior of MISTD. A comprehensive understanding of transient properties is particularly crucial in practical applications, especially in today's context where high-speed response is a major requirement for electronic devices [62–68]. Furthermore, the transient characteristics of MIS devices can be utilized for extracting bulk semiconductor minority carrier lifetimes [69–71], understanding interface trap properties [72–74], and assessing the extent of copper contamination [75–77]. The capacitor properties of MISTD can also be exploited by reading its transient current to function as an embedded dynamic memory [78–88].

In this work, we delve into an in-depth exploration of the transient current characteristics of MISTD. We propose methods to enhance the magnitude of its transient current by optimizing parameters and designing special structures, aiming to elevate its performance as a dynamic memory for future application.

1.2 Basic Electrical Characteristics of MISTD

We will focus our investigation on the Al/SiO_2/Si(p) tunnel diode within the scope of this study. The p-type boron doping concentration is approximately 10^{16} cm^{-3}, and the silicon

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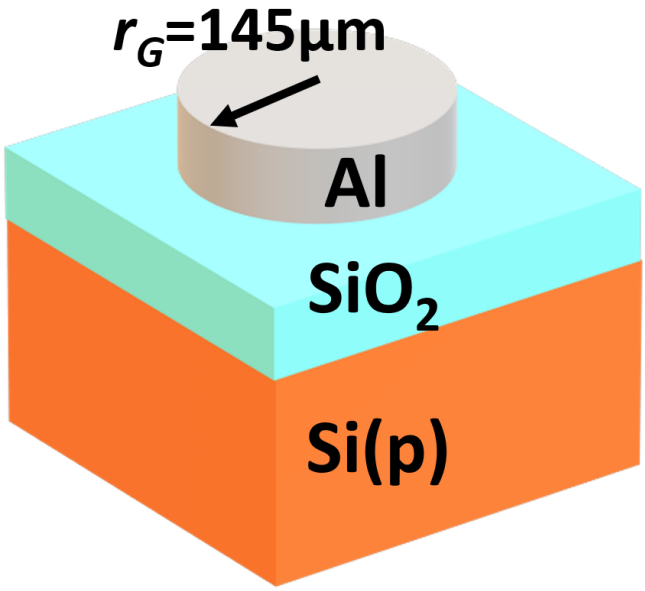

Figure 1–1. Illustration of the MISTD device studied in this work.

dioxide layer has a thickness ranging from 2 to 4 nm. The top aluminum layer is circular, with a radius of 145 μm, and serves as the gate in this configuration. The device structure is visually depicted in **Figure 1–1** , while **Figure 1–2** illustrates the band diagram of the Al/SiO_2/Si(p) system at room temperature, specifically at the flat-band voltage, showcasing detailed information on electron affinity, work function, and bandgap [89–91].

The flat-band voltage, denoted as V_{Fb}, is defined as the gate voltage that results in a flat energy band in the silicon. It can be expressed as follows:

$$V_{Fb} = \phi_m - (\chi_s + E_g/2q + \phi_F) \tag{1.1}$$

Here, ϕ_m is the metal work function, χ_s is the silicon electron affinity, E_g is the silicon band gap, q is the elementary charge, and ϕ_F is the Fermi potential of the silicon. The Fermi potential is defined as the potential difference between the intrinsic Fermi level (E_i)

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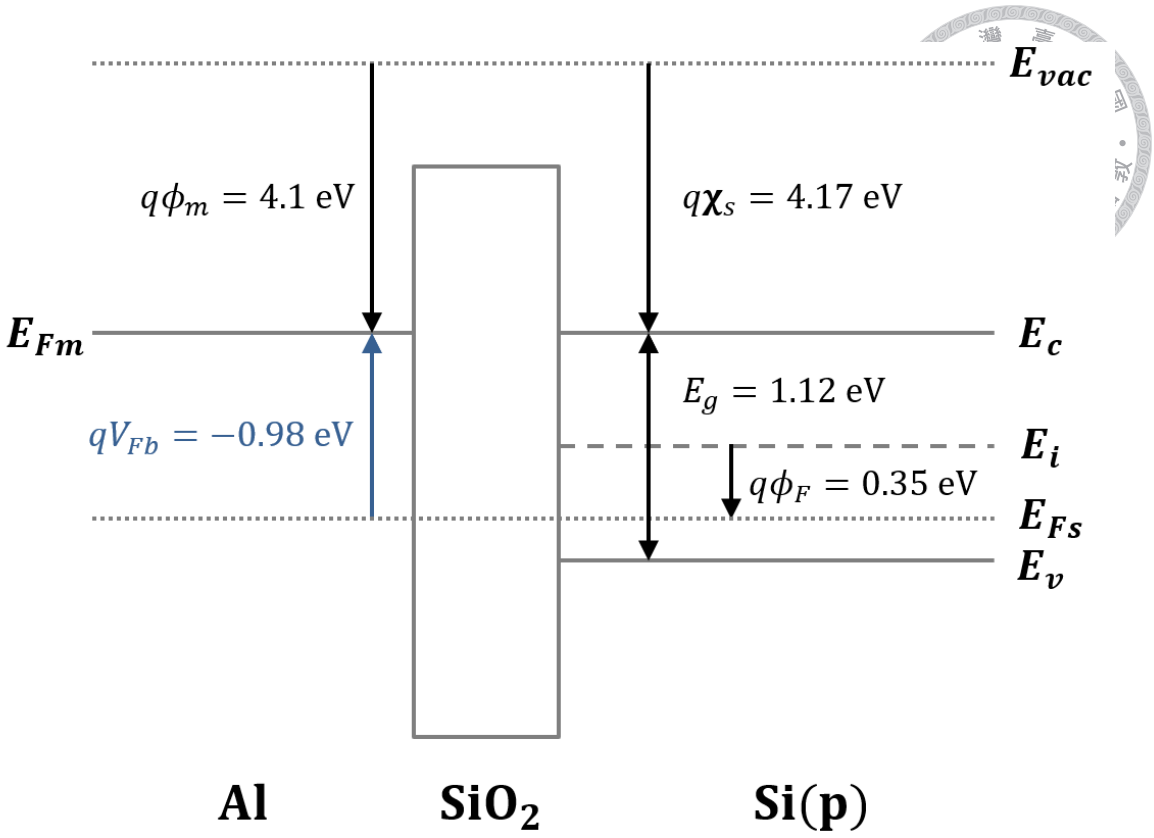

Figure 1–2. Band diagram of the MISTD device at the flat-band voltage at room temperature.

and the bulk Fermi level (E_{Fs}). ϕ_F can be expressed as

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{1.2}$$

where k is the Boltzmann's constant, T is the temperature, N_A is the p-type doping concentration, and n_i is the intrinsic carrier concentration in the silicon. For the MISTD studied in this work, V_{Fb} = -0.98 V.

The steady-state electrical characteristics of the MISTD with varying oxide thicknesses have been thoroughly investigated in existing literature [92–96]. In this work, we utilize the findings from [97] to introduce the current-voltage ($I - V$) and capacitance-voltage ($C - V$) characteristics. The devices studied in [97] were identical to those employed in our

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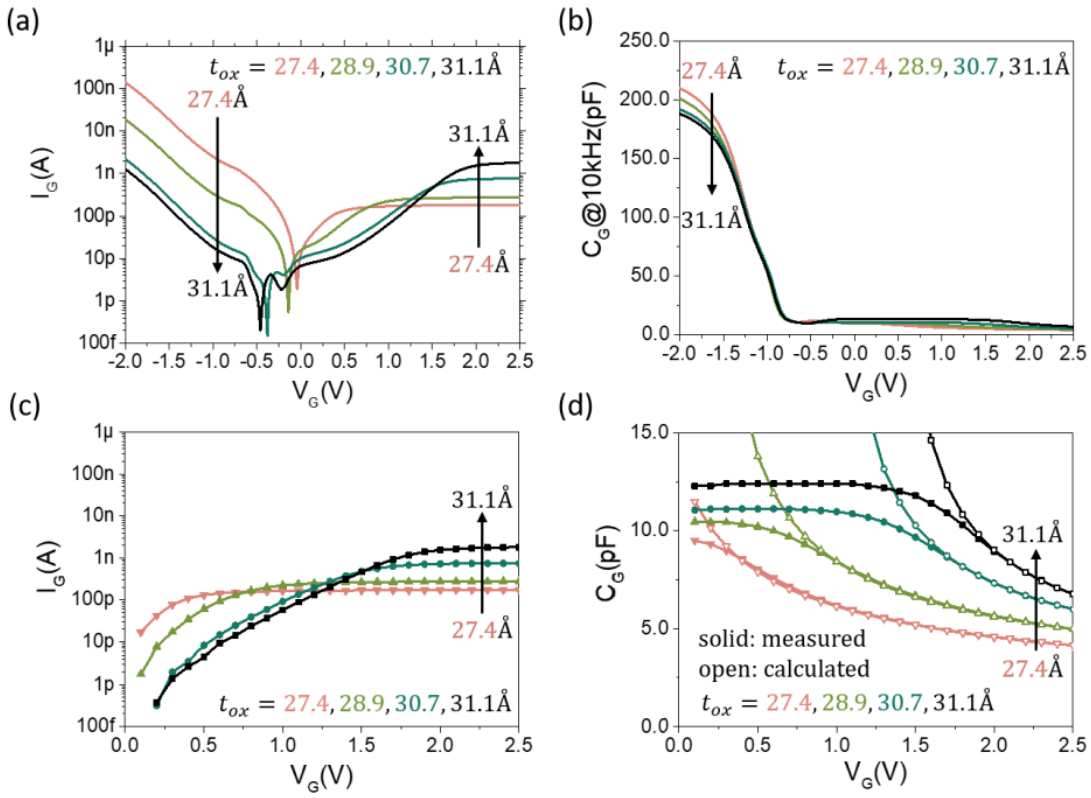

Figure 1–3. (a) $I-V$ and (b) $C-V$ characteristics of the MISTD with varying oxide thicknesses, utilizing a voltage sweep ranging from -2 to 3 V. (c) $I-V$ and (d) $C-V$ characteristics at the steady state investigated by biasing the device at the measuring voltage for a duration of 10 seconds. The gate radius is 85 μm here [97].

research, with the only difference being the gate area. The $I-V$ and $C-V$ characteristics will provide insights into the electrostatic behavior of the MISTD, including parameters such as the oxide voltage drop (V_{ox}) and silicon surface band bending (ψ_s) under different gate voltages.

Figure 1–3 (a) and (b) depict the $I-V$ and $C-V$ characteristics, respectively, of the MISTD with varying oxide thicknesses by sweeping up the voltage. **Figure 1–3** (c) and (d) present the $I-V$ and $C-V$ characteristics when the devices are in the steady state, biased at the measuring voltage for 10 seconds, for positive gate voltages (V_G).

The $I-V$ curve resembles that of a diode. For a negative V_G, the MISTD operates in

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the forward-bias regime, where the current is dominated by the electron tunneling current and electrons tunnel from the metal gate to the silicon. When $V_G > 0$, the device enters the reverse-bias regime, and the positive current saturates. In this case, the current comes from electrons tunneling from the silicon to the gate. The gate current I_G for $V_G > 0$ can be divided into two regimes. When V_G is not large and I_G has not saturated, the current's magnitude is limited by the tunneling rate of electrons, termed the 'tunneling-limited regime'. If V_G is sufficiently large for I_G to saturate, the magnitude of the gate current is limited by the generation current in the silicon, known as the 'generation-limited regime'.

The $C - V$ characteristics of the MISTD are analogous to the traditional metal-oxide-semiconductor (MOS) capacitor. The voltage balance of the MISTD is expressed as follows:

$$V_G - V_{Fb} = V_{ox} + \psi_s \tag{1.3}$$

$$= -\frac{Q_s(\psi_s)}{C_{ox}} + \psi_s \tag{1.4}$$

Here, $Q_s(\psi_s)$ is the charges in the silicon for a specific ψ_s, and C_{ox} is the oxide capacitance. For $V_G < V_{Fb}$ (which is -0.98 V in this work), the MISTD is in the accumulation regime, where holes accumulate near the silicon surface. When $V_{Fb} < V_G < V_{th}$, the MISTD is in the depletion regime. V_{th} is the gate voltage when $\psi_s = 2\phi_F$, signifying the onset of silicon entering the inversion regime. V_{th} can be explicitly expressed as follows:

$$V_{th} = V_{Fb} - \frac{Q_s(2\phi_F)}{C_{ox}} + 2\phi_F \tag{1.5}$$

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For the MISTD devices studied here, V_{th} is approximately -0.2 V. Without considering quantum tunneling, as in a traditional MOS capacitor, the device is in the inversion regime for $V_G > V_{th}$. However, for the MISTD, inversion electrons in the silicon tunnel through the oxide to the gate. When V_G is sufficiently large for the tunneling rate to surpass the capability of electron generation in the silicon, the number of inversion charges does not increase with V_G. As a result, V_{ox} is fixed according to (1.3), and the increase in V_G falls on the silicon. This leads to the deep depletion phenomenon, where the depletion region expands, and the capacitance value drops. The gate voltage at which deep depletion begins is defined as the critical voltage V_c according to the literature [96]. Therefore, the MISTD is in the inversion regime for $V_{th} < V_G < V_c$ and is in the deep depletion regime for $V_G > V_c$.

V_c also marks the separation point between the tunneling-limited and generation-limited regime. In the tunneling-limited regime, where $0 < V_G < V_c$, the tunneling rate of electrons is lower than the maximum total generation rate of electrons inside the silicon. Consequently, the oxide can hold the inversion charges despite the leakage current. The number of inversion charges is close to that derived in the classical MOS capacitor without considering quantum tunneling. This means the increase in V_G in this regime mostly reflects on the increase in V_{ox}, while ψ_s almost remains the same, as shown in **Figure 1–4** (a)(b) and (c). In the generation-limited regime, where $V_G > V_c$, the tunneling rate of electrons surpasses the maximum total generation rate inside the silicon. The oxide is unable to hold as many inversion charges due to the large leakage current. Therefore, the inversion charges do not increase with V_G. V_{ox} remains constant as V_G increases, resulting in the saturation of I_G. Meanwhile, the increase in V_G almost entirely falls onto the silicon, leading to the

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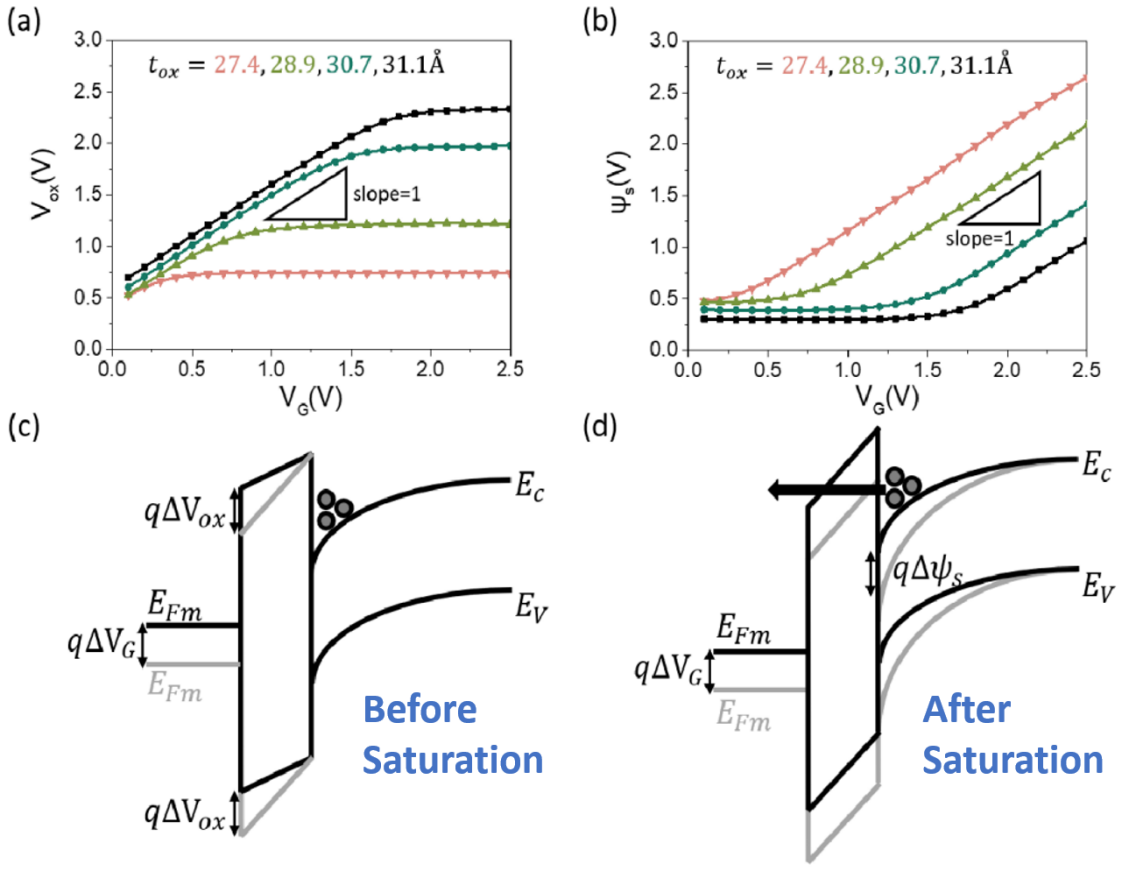

Figure 1–4. (a) The oxide voltage (V_{ox}) and (b) the silicon surface band bending (ψ_s) extracted from the $C-V$ characteristics in **Figure 1–3**. (c) The band diagram under a low positive gate voltage (V_G), where the oxide can hold the inversion charges. The gate current is in the tunneling-limited regime. The voltage drop mainly occurs across the oxide layer. Consequently, V_{ox} increases as V_G increases, while ψ_s remains almost constant. (d) The band diagram under a large positive gate voltage, where the oxide cannot hold the inversion charges. The gate current is in the generation-limited regime. The voltage drop primarily occurs across the silicon. Consequently, ψ_s increases as V_G increases while V_{ox} remains almost constant [97].

deep depletion phenomenon, as shown in **Figure 1–4** (a)(b) and (d).

The preceding discussion is succinctly encapsulated in **Figure 1–5**, presenting the $I-V$ and $C-V$ characteristics of an MISTD with a 3 nm oxide layer. This visualization underscores the various regimes and the specific voltages (V_{Fb}, V_{th}, V_c) as defined earlier.

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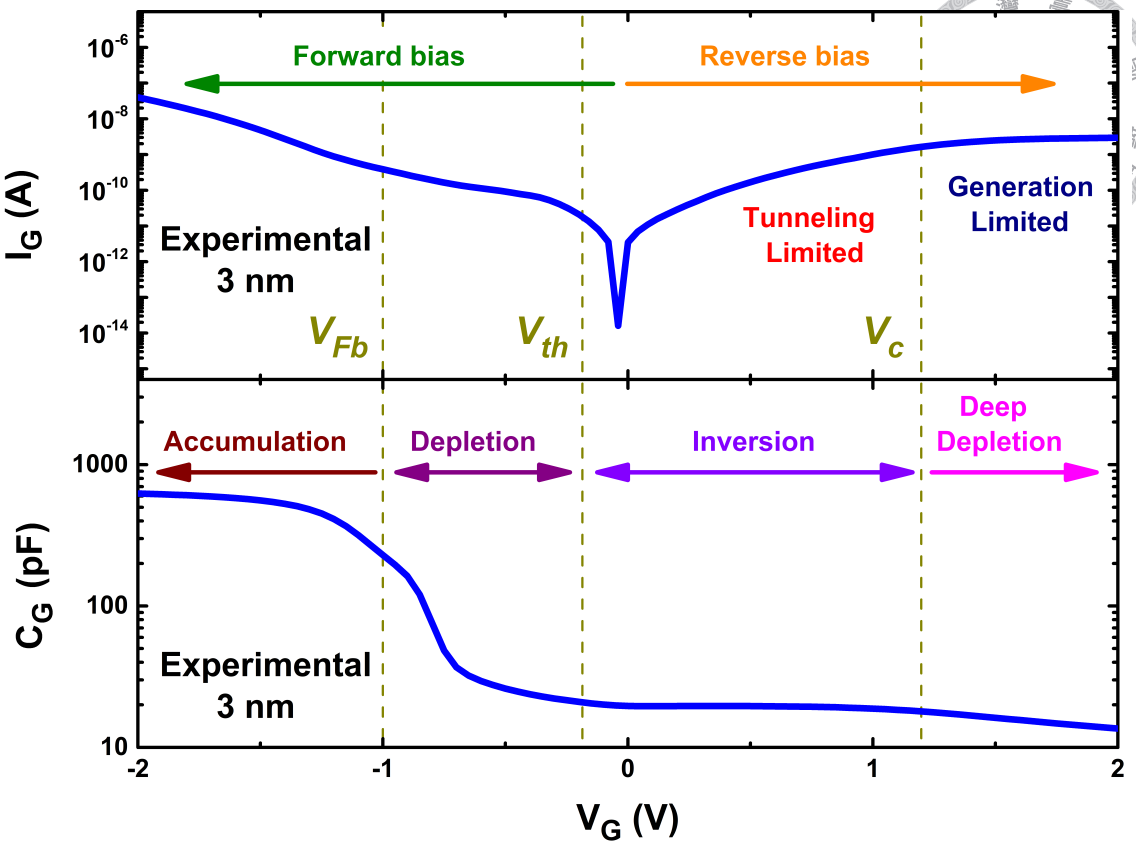

Figure 1–5. $I - V$ and $C - V$ characteristics of an MISTD with a 3 nm oxide layer, emphasizing the various regimes discussed in the text.

1.3 Transient Behavior in MISTD

In this study, our focus centers on the transient current behavior of the MISTD. Previous research [78–83] has established that applying voltage pulses with different polarities to the gate yields gate currents with opposite directions, a characteristic that can be harnessed for dynamic memory applications. The voltage program employed to test the transient response of the device is depicted in **Figure 1–6**. The read procedure consistently takes places at 0 V. A positive voltage pulse with a write voltage V_{Write} and a write time T_{Write} is applied to the gate for 'Write 1' (W1). Subsequently, the gate voltage is switched to 0 V, resulting in a negative transient read current at the gate, denoted as the current of 'Read

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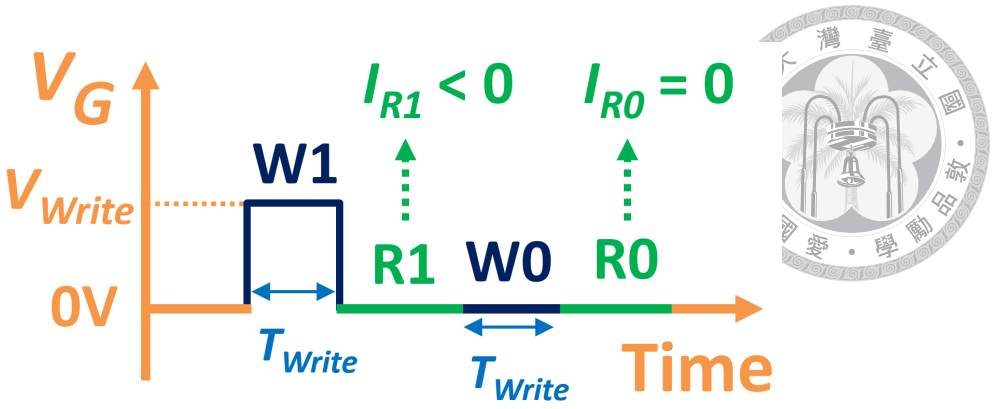

Figure 1–6. The voltage program used for the dynamic memory operation.

1' ($I_{R1} < 0$). Conversely, a voltage pulse with a 0 V write voltage is employed for 'Write 0' (W0), leading to a zero read current ($I_{R0} = 0$) when the gate voltage is switched to 0 V. The opposite polarities of the two transient currents (negative for I_{R1} and 0 for I_{R0}) can store one-bit information, serving as a dynamic memory.

It is evident that a 0 V write pulse results in a zero transient current read at 0 V since no charges are stored in the devices during W0. No charges need to flow in or out to respond to the change in gate voltage, as the gate voltage remains constant. On the contrary, it might be perplexing why a positive write pulse leads to a negative transient read current. This can be succinctly explained by referring to **Figure 1–7**. **Figure 1–7** (a) and (b) schematically illustrate the charges and currents in the MISTD during 'R1' and at 0 V steady state, respectively. During 'W1', a positive bias is applied to the gate, resulting in positive charges stored at the gate and negative charges stored in the silicon. At the beginning of 'R1', where the gate voltage is switched to 0 V, the stored negative charges in the silicon cannot flow out immediately. Despite carriers in the metal usually having a much faster response time than in the semiconductor [98, 99], discharging the positive charges stored at the gate is constrained by the discharging of negative charges in the silicon due

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to charge neutrality. Consequently, there will be excess positive charges at the gate and excess negative charges in the silicon at the beginning of the transient, compared to those at the 0 V steady state. The positive charges at the gate will gradually discharge in response to the change in negative charges in the silicon. Discharging can occur through the external circuit or by quantum tunneling. The former results in a negative gate transient current ($I_d < 0$) due to the discharge of positive charges, while the latter results in a positive gate transient current ($I_t < 0$) due to the tunneling of negative charges from the silicon to the metal gate. Thus, the transient current during R1 can be expressed as

$$I_{Read,1} = I_d + I_t \tag{1.6}$$

where I_d is positive while I_t is negative. However, in the time interval of interest for this study, specifically the read time before 100 ms, it is observed that I_t is significantly lower than I_d based on simulation results, which will be discussed further later in this dissertation. Therefore, $I_{Read,1}$ is dominated by I_d and is negative.

Special design considerations were implemented in the structure of the MISTD to enhance the transient read current, aiming to provide a larger current window for easier identification of distinct states [78–83]. However, limited attention has been given to the fundamental transient current behavior of the simplest structure, the **Planar** MISTD. We believe that a thorough investigation into the transient behavior of the Planar MISTD will establish a robust foundation for the future design of MISTD for dynamic memory applications. Therefore, we will primarily focus on the research of the transient behavior of the Planar MISTD.

At the same time, owing to the voltage program we have adopted, the current window

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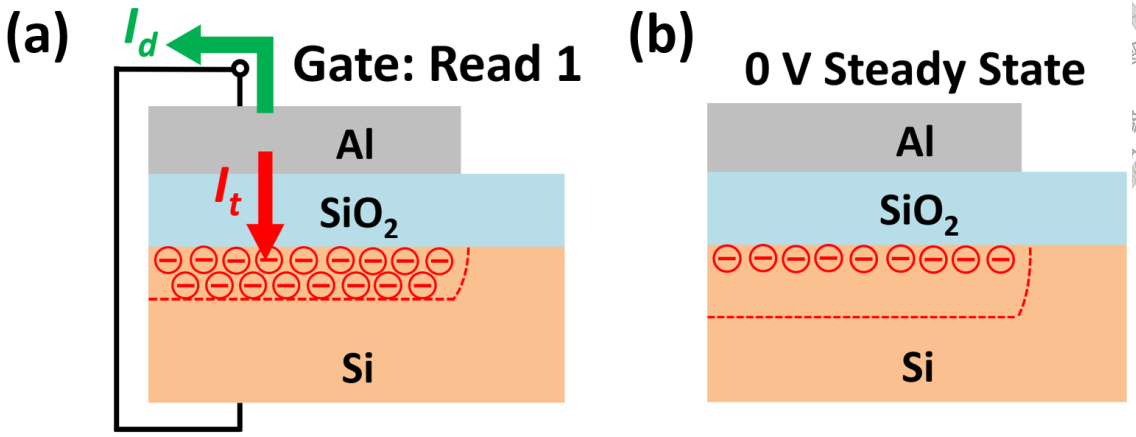

Figure 1–7. (a) Schematics of the transient currents during 'Read 1'. The total gate current (I_G) is a composite of a negative displacement current (I_d) and a positive tunneling current (I_t). (b) Schematics of the MISTD at 0 V steady state. No current will be measured at the gate.

is determined by the magnitude of the transient read current of 'R1'. Consequently, our research emphasis is placed on the transient behavior of R1. For the specific Al/SiO_2/Si(p) system employed, the MISTD device is in the inversion regime at 0 V during 'R1'. Meanwhile, the MISTD device during 'W1' is subjected to a gate voltage more positive than 0 V. Accordingly, the MISTD is considered to be in a 'deeper' inversion during 'W1', compared to the 0 V steady state. Therefore, the particular scenario of interest in this work is ***the transient current behavior of the MISTD switching from a 'deeper' inversion to a 'shallower' inversion***. To the best of our knowledge, this aspect has not been extensively studied in the academic literature. Although some work had discussed the transient behavior of the MOS capacitor, they primarily focused on the transient capacitance when transitioning from the flat-band condition to the inversion regime [65, 66, 70, 100–104].

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1.4 Fabrication Process

A p-type boron-doped (100)-oriented 3-inch silicon wafer with a resistivity of 1-10 Ω-cm (doping concentration around 10^{16} cm^{-3}) was utilized as the substrate. Initial wafer cleaning was performed using the Radio Corporation of America (RCA) process to eliminate impurities and native oxide, as outlined in [105]. Subsequently, an ultra-thin silicon dioxide layer with an oxide thickness ranging from 2 to 4 nm was grown through the anodic oxidation (ANO) process. The anodic oxidation apparatus, identical to the one employed in this study, is depicted in **Figure 1–8** (a) in [55]. Further details on the mechanism of anodic oxidation of SiO_2 can be found in [106].

In the ANO process, the silicon wafer and the platinum plate are immersed in deionized (D.I.) water and connected to a 15 V DC voltage source, serving as the anode and the cathode, respectively. The electric field between the silicon and the platinum induces dissociation of the D.I. water, and the hydroxide ions (OH^-) react with the Si wafer to grow the SiO_2 thin film. The chemical reaction at the anode side is given by:

$$Si + 4\,OH^- \rightarrow SiO_2 + 4\,e^- + 2\,H_2O. \tag{1.7}$$

The ANO process exhibits a relatively slow oxide growth rate, allowing precise control over the oxide thickness. An essential advantage of anodic oxidation for SiO_2 growth in studying MIS tunnel diodes is the ability to achieve a gradual change in oxide thicknesses on a single wafer by tilting the silicon wafer in D.I. water during anodic oxidation. This gradual change results from the electric field's gradual variation, enabling the fabrication of MIS tunnel diodes with multiple oxide thicknesses on a single wafer. In this work, for

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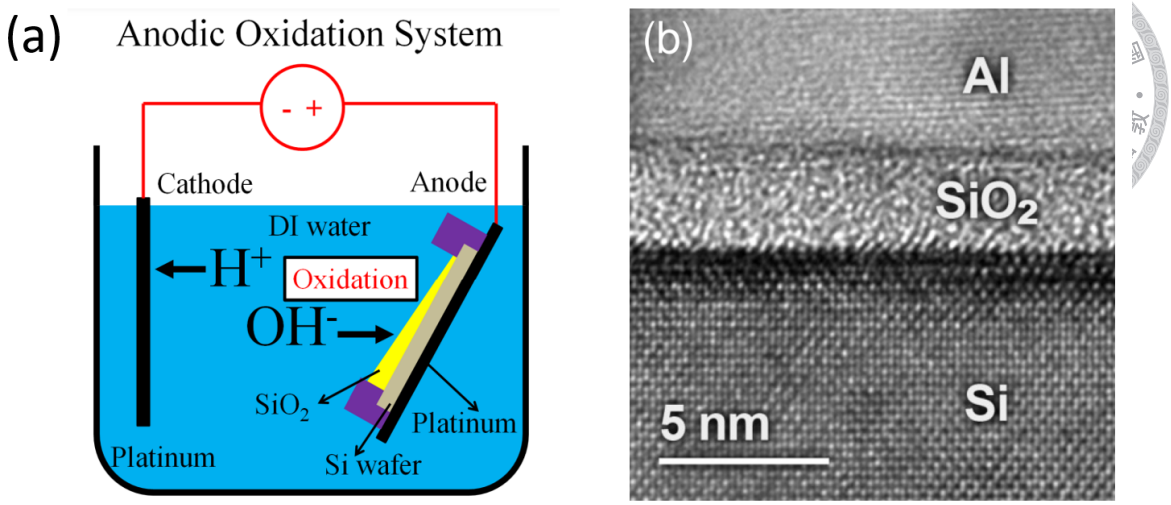

Figure 1–8. (a) Illustration of the anodic oxidation apparatus [55]. (b) HRTEM image of an MISTD device [96].

instance, MIS tunnel diodes on the same wafer have oxide thicknesses ranging from 2.5 to 3.3 nm.

Despite anodic oxidation not being a conventional method for SiO_2 formation, prior studies have demonstrated that anodic growth SiO_2 exhibits quality comparable to thermally grown SiO_2. **Figure 1–8** (b) from [96] presents a cross-sectional high-resolution Transmission Electron Microscopy (HRTEM) image of an MIS tunnel diode with anodic growth SiO_2, showcasing a dense and defect-free oxide layer. In [107], the evolution of X-ray Photoelectron Spectroscopy (XPS) Si 2p spectra from the oxide surface to the Si substrate for oxides with a 40 Å thickness of anodic SiO_2 showed a similar trend to RTO SiO_2. [107] further demonstrated that MIS tunnel diodes with anodic SiO_2 exhibited lower leakage current and higher breakdown voltage than those with RTO SiO_2. Thus, anodic growth of SiO_2 is believed to possess comparable quality to traditionally grown dry-oxidation SiO_2.

Following oxide growth, the wafers underwent rapid thermal annealing (RTA) to rec-

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tify oxide defects and interface imperfections, conducted in an ambient environment of 15 torr N_2 under 900 ℃ for 45 seconds. A 150 nm aluminum layer was thermally evaporated onto the top of the wafer, subsequently patterned as the top gate with a radius of 145 μm using photolithography. Subsequently, buffered oxide etchant (BOE) was employed to eliminate the native oxide on the wafer's backside, and a 150 nm aluminum layer was evaporated onto the backside to serve as the back contact.

1.5 Measurement Details

The DC, AC, and transient electrical characteristics were measured using the Agilent B1500A. During the $I-V$ and $C-V$ measurements, the gate voltage was ramped from negative to positive (forward direction) or vice versa (reverse direction), following the conventional measurement method. The voltage program for measuring transient characteristics, including current-time ($I-t$) and capacitance-time ($C-t$) characteristics, is illustrated in **Figure 1–9**. The device is biased at a voltage V_{Base} for a 'Base Hold Time' before the measurement. When the gate voltage is switched to V_{Source}, the measurement starts, and the time point of the switching is marked as the beginning of the transient time, i.e., $t = 0$. To test the transient behavior of the MISTD, this voltage program will be executed with

$$V_{Base} = V_{Write}, \tag{1.8}$$

$$V_{Source} = V_{Read}, \tag{1.9}$$

$$Base\ Hold\ Time = T_{Write}, \tag{1.10}$$

where V_{Read} is the gate voltage during the read procedure, typically set to 0 V in this dissertation.

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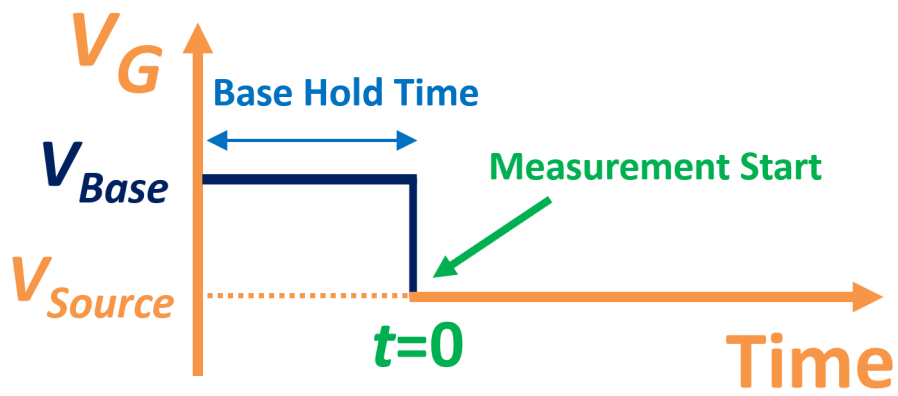

Figure 1–9. The voltage program utilized for measuring transient characteristics set on the Agilent B1500A measuring instrument.

Figure 1–10 illustrates examples of the measured transient read current I_{Read} for an MISTD with the oxide thickness d = 29.7 Å, T_{Write} = 1 s, and V_{Write} = 0.3 V (black curve) and 1 V (red curve). The transient current decays with time. To facilitate uniform comparisons, we opt to extract the value of the transient current at 50 ms for discussion, which is close to the refresh time of the dynamic memory (64 ms). However, it is noteworthy that the measured transient current might not include data at 50 ms. In such cases, we perform interpolation using the neighboring measured data, assuming an exponentially decaying trend. Although the transient current at millisecond time scales does not precisely follow an exponential decay, the interpolation provides a good fit, as depicted in **Figure 1–10**, and is more accurate than linear interpolation (not shown here). Therefore, we will employ the interpolation method mentioned above to extract the data at 50 ms if it is not measured.

It is crucial to note that the oxide thickness d of the MISTD serves as the electrical equivalent oxide thickness (EOT) and is determined through electrical measurements. Given that the tunneling current of the MISTD under a forward bias is highly dependent on the oxide thickness, it can be effectively employed for fitting the oxide thickness. The database utilized for this purpose is the collection of $I-V$ curves in [108], where the oxide

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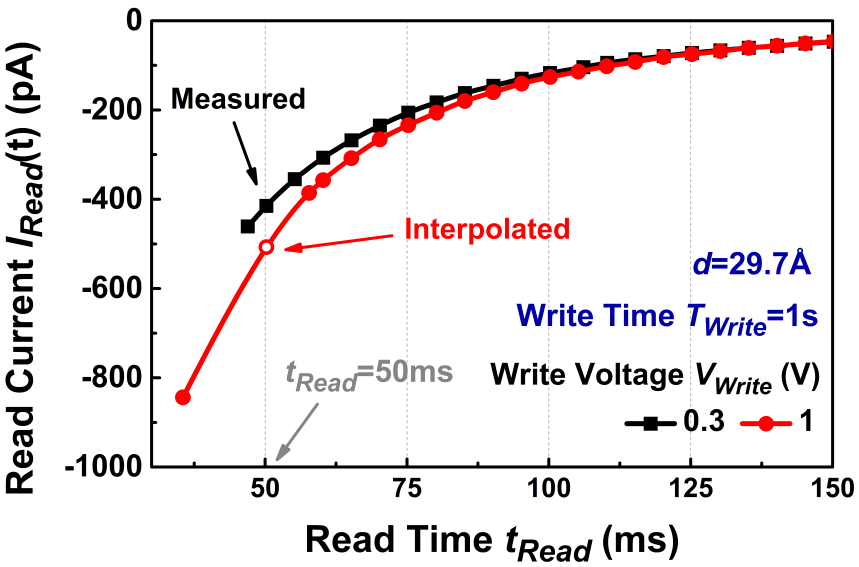

Figure 1–10. An example of the measured transient read current-time ($I_{Read} - t$) characteristics. In many sections of this work, we will extract and discuss the transient current at 50 milliseconds as a focal point of analysis. If the measured transient current data does not encompass information at the 50-millisecond time point, we will assume an exponential decay of the transient current and interpolate accordingly, as illustrated by the red curve in the figure.

thicknesses of the various MISTD were characterized by HRTEM images. The DC current density J of the MISTD device in the accumulation regime (V_G < - 1 V) is employed to fit the oxide thickness d, with the assumption that $ln\, J \propto -d$. The validity of this assumption is briefly elucidated as follows.

The tunneling current can be expressed as [4],

$$J = \frac{qm^* k^2 T^2}{2\pi^2 \hbar^3} P_t S \propto P_t \tag{1.11}$$

where m^* is the longitudinal electron effective mass of silicon, P_t is the tunneling probability, and S is the supply function in the Tsu-Esaki model [109, 110], which remains almost constant for a fixed V_G in accumulation regime. For direct tunneling, P_t can be expressed

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as

$$P_t = exp\left(-\frac{B[1-(1-V_{ox}/\psi_b)^{3/2}]}{E_{ox}}\right) \tag{1.12}$$

where B is a constant in the FN tunneling model [111], ψ_b is the conduction band offset between Si and SiO_2, and E_{ox} is the electric field in the oxide. If there is no charges within the oxide layer,

$$E_{ox} = \frac{V_{ox}}{d} \tag{1.13}$$

For an MISTD in the accumulation regime, most of the gate voltage offset to the flat-band voltage ($V_G - V_{Fb}$) will drop on the oxide layer. Therefore, V_{ox} will be the same for MISTD with different oxide thicknesses. As a result, the logarithm of the tunneling current in the accumulation regime will be linearly correlated to the oxide thickness d with a slope of -1,

$$ln\, J \propto ln\, P_t \propto -1/E_{ox} \propto -d \tag{1.14}$$

In this work, d is fitted using the current density at -1.8 V.

1.6 TCAD Simulation

We employed Silvaco Atlas TCAD for device simulation in this dissertation [112]. The simulation was performed in a 2-D cylindrical coordinate system to better align with the circular shape of the device used in the experiment. **Figure 1–11** schematically illustrates the device structure used in the simulation. Silicon was p-type doped with a doping con-

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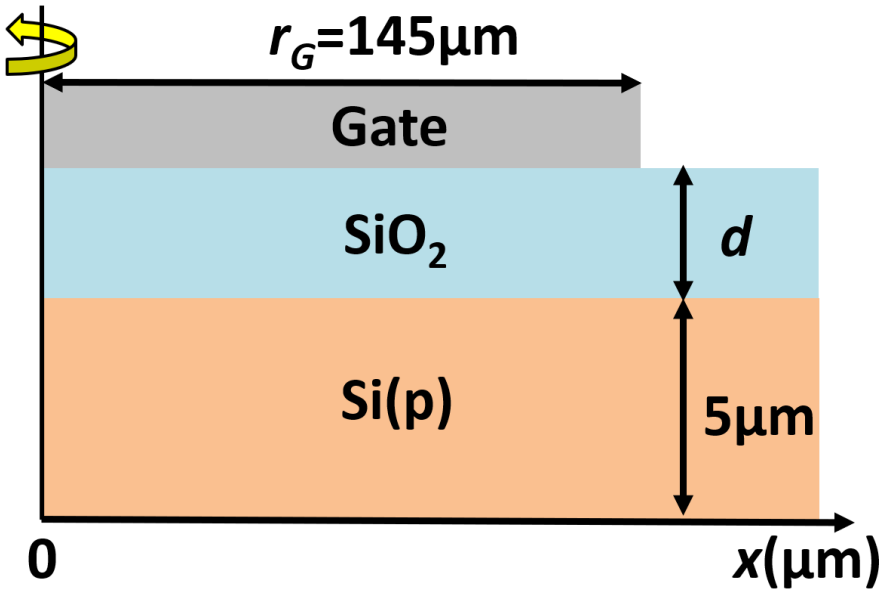

Figure 1–11. Schematic cross section of the device used for 2-D cylindrical TCAD simulation.

centration of 10^{16} cm^{-3}. The silicon substrate thickness was set to 5 μm. The SiO_2 layer was uniform with a thickness d. The gate metal was aluminum, with a work function of 4.1 eV. The gate radius was 145 μm, identical to the one in the experiment.

In addition to the drift-diffusion model, which accounts for carriers' transport in the semiconductor, the following models were also included in the TCAD simulation: quantum effect in Bohm quantum potential form [113], Schockley-Read-Hall (SRH) recombination [114, 115]. The tunneling current was modeled using self-consistent direct tunneling in all its forms [110]. The lifetime (τ) for both electrons and holes was set to 100 ns by default. The trap energy level was at the intrinsic Fermi level E_i. The model of the lifetime dependency on the impurity concentration was not considered. Interface traps were not included for the simplicity of discussion. Auger recombination was also ignored due to its negligible contribution to the recombination compared to SRH recombination under the interested conditions [116].

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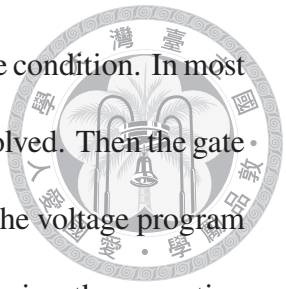

The $I-V$ and $C-V$ characteristics were simulated in the steady-state condition. In most transient simulations, the steady-state of the device at V_{Write} was first solved. Then the gate voltage switched to 0 V, and the transient started. This was similar to the voltage program in **Figure 1–9** with an infinitely long base hold time, aimed at reducing the execution time of the simulation. This voltage program was intended to simulate the case when the MISTD almost reached the steady-state during 'W1' in the experiment. Generally, this was the case when $T_{Write} \geq 1$ s. Further details will be addressed in the subsequent chapter.

1.7 Chapter Organization

We initiated our exploration into the transient current behavior of the Planar MISTD, aiming to establish a robust foundation for comprehending the MISTD's transient behavior. In **Chapter 2**, we examined the transient currents of the Planar MISTD at the 50-millisecond mark, drawing insights from both experimental observations and simulation results. We assessed the impact of voltage program polarity, write voltage, write time, and oxide thickness on the transient current. A noteworthy observation was the saturation of the transient current as the positive write voltage increased, marking the first instance of such a phenomenon. We proposed a mechanism to elucidate this behavior. We also discussed the influence of oxide charges on the transient current behavior, explaining discrepancies between experimental and simulation results, where 'ideal' MISTD devices were considered without accounting for oxide charges. Delving deeper into the current saturation phenomenon, **Chapter 3** presented an analytical model of transient currents in the sub-millisecond regime, with results aligning closely with TCAD simulations.

Subsequently, we introduced two specialized designs for the MISTD's structure to enhance the transient current window for dynamic memory applications. **Chapter 4** show-

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cased the enhanced transient current and capacitance window of the ultra-thin metal surrounded gate (UTMSG) MISTD. In **Chapter 5** we introduced the oxide local thinning (OLT) MISTD, presenting an enhanced transient current window. **Chapter 6** concluded our research by benchmarking the transient current window of MISTD with various designs and offering suggestions for future work.

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2

Transient Currents of Planar MISTD at Millisecond Time Scales

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2.1 Introduction

In **Chapter 1**, we introduce the steady-state electrical characteristics of the MISTD, resembling a MOS capacitor with an ultra-thin oxide layer. We also present the fabrication process and the simulation setup for the MISTD. The fundamental transient current behavior and the measuring voltage program are also discussed. In this chapter, we delve further into the transient current behavior of the Planar MISTD to establish a foundation for employing MISTD in dynamic memory applications.

Our exploration commence with the examination of experimental results in **Section 2.2**. Transient currents were examined under various write programs, considering voltage polarities, write voltages (V_{Write}), write times (T_{Write}), and oxide thicknesses (d) as parameters. It is revealed that there exists an optimal oxide thickness for achieving the maximum transient current. Notably, when employing a positive write pulse, the transient current exhibits saturation as the write voltage increased, a phenomenon termed the 'Saturation Phenomenon'. In **Section 2.3**, TCAD simulations were conducted to investigate the transient current behavior of the Planar MISTD, yielding results consistent with the experimental findings. Building on the simulation outcomes, we propose a detailed mechanism to elucidate the peculiar 'Saturation Phenomenon' in **Section 2.4**, reinforcing the proposed mechanism with additional supporting evidence.

Subsequently, contour plots are introduced in **Section 2.5** to identify optimal parameters that can yield the largest transient currents in the MISTD. This serves as an illustrative example guiding the optimization of the Planar MISTD design. Further clarification of uncertainties in the simulation results presented in **Section 2.3**, including the impact of Auger recombination, tunneling current, and the value of carriers' lifetime, is provided

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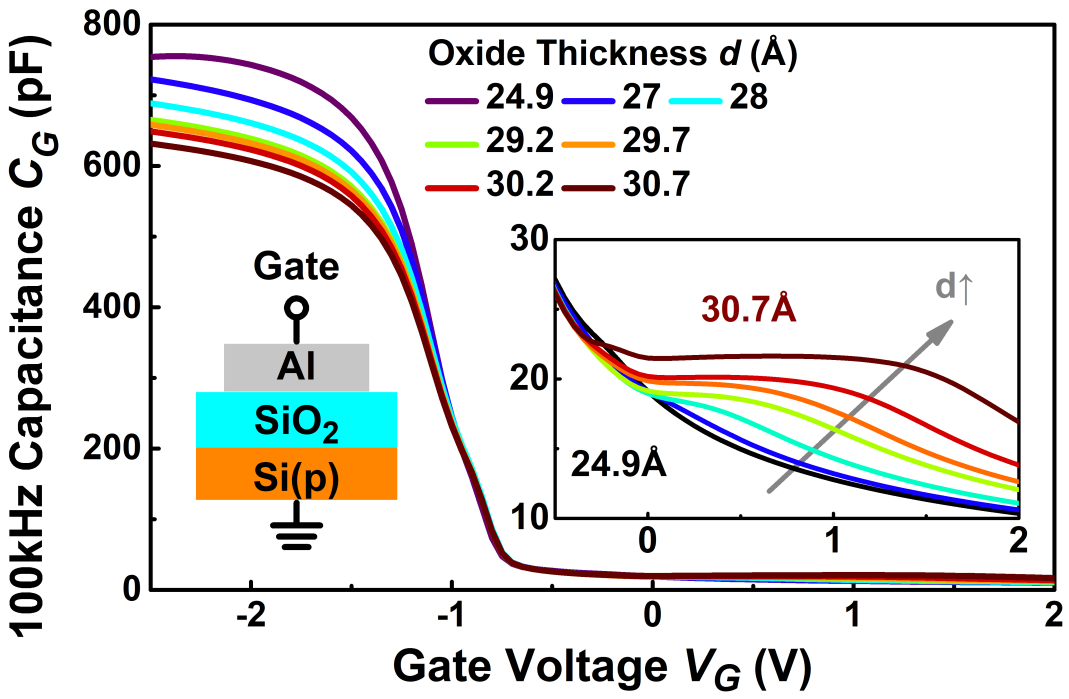

Figure 2–1. 100k Hz $C_G - V_G$ characteristics of the Planar MISTD with the oxide thickness ranging from 24.9 Å to 30.7 Å. Left inset: Device cross section. Right inset: Enlargement of the $C_G - V_G$ curves in the inversion and deep depletion regime.

in **Section 2.6**. Finally, **Section 2.7** discuss the influence of existing oxide charges on transient current behavior, effectively explaining discrepancies between experimental and simulation results.

The $C_G - V_G$ characteristics at a frequency of 100 kHz of the MISTD investigated in this section are depicted in **Figure 2–1**. The devices exhibit varying oxide thicknesses ranging from 24.9 Å to 30.7 Å. In the accumulation regime (V_G < -1 V), the capacitance, C_G, as determined by the oxide capacitance, is expressed as:

$$C_{ox} = \frac{\epsilon_{ox}}{d} \tag{2.1}$$

where C_{ox} represents the oxide capacitance per unit area, ϵ_{ox} is the permittivity of silicon

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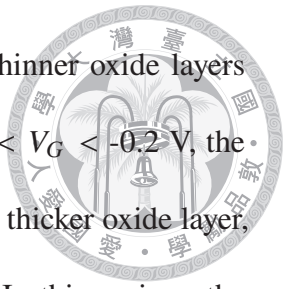

dioxide, and d is the oxide thickness. Consequently, devices with thinner oxide layers demonstrate larger C_G values in the accumulation regime. For -1 V < V_G < -0.2 V, the devices are in the depletion regime. Afterwards, for the device with a thicker oxide layer, e.g., d = 30.7 Å, the device transitions into the inversion regime. In this regime, the device stores more inversion charges under positive bias ($V_G > 0$) compared to zero voltage ($V_G = 0$). Consequently, when the gate voltage switches from positive to zero volts, transient current is anticipated. Conversely, for the device with a thinner oxide layer, e.g., d = 24.9 Å, the device enters the deep depletion regime immediately after V_G = -0.2 V. In this case, the device can not store any inversion charges due to the large tunneling rate of the thin oxide layer. Therefore, no transient current is expected when the device switched from positive gate voltage to zero voltage. It is noteworthy that when the electron tunneling rate exceeds the electron generation rate, the device enters the deep depletion regime. Consequently, the device with a thicker oxide layer, characterized by a lower tunneling rate, will enter the deep depletion regime at a larger gate voltage, leading to a 'wider' inversion regime compared to the device with a thinner oxide layer. The detailed results of the transient currents for these devices will be presented and discussed in the subsequent sections.

2.2 Transient Currents at Millisecond Time Scales

2.2.1 Overview

In this section, we will discuss the experimental results of the transient currents read at 50 ms (I_{Read}) under different voltage programs. We will examine the impact of the voltage polarity, V_{Write}, T_{Write}, and d on I_{Read}. First of all, we want to mention that the write pro-

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grams with the opposite polarities will result in I_{Read} with the opposite polarities. More specifically, $V_{Write} > 0$ results in $I_{Read} < 0$ and $V_{Write} < 0$ results in $I_{Read} > 0$. The different polarities of I_{Read} can serve as the two states for memory application. Alternatively, we can also select either $V_{Write} > 0$ or $V_{Write} < 0$, combined with $V_{Write} = 0$, which results in $I_{Read} = 0$, to serve as the memory two states as discussed in **Section 1.3**. Basically, we consider that it will be better to select $V_{Write} > 0$ and $V_{Write} = 0$ as the voltage programs for memory two states, since the reverse-bias current is usually much lower than the forward-bias current, conserving power [10, 20, 51]. Besides, there will be more electron trapping in the oxide layer under forward-bias for $V_{Write} < 0$, resulting in reliability issues [57]. However, we still demonstrate I_{Read} under negative write programs as a comparison to the results with positive write programs, to gain more insights into the characteristics and the mechanism of the transient currents with $V_{Write} > 0$.

In **Figure 2−2** (a) and (b), the experimental results depict the magnitude of the transient read currents at 50 ms, denoted as I_{Read} hereafter, for MISTD with various oxide thicknesses (d). The data is presented against V_{Write}, spanning from -2 V to +3 V, with T_{Write} set at 10 ms and 1 s, respectively. Each data point is extracted from a decaying transient current ($I_{Read} - t$ characteristics) as illustrated in **Figure 1−10** . Several observations can be highlighted:

- I_{Read} exhibits dependence on V_{Write}, T_{Write}, and d.
- Under positive write programs, the magnitude of I_{Read} increases with an increase in T_{Write} from 10 ms to 1 s, while it remains relatively constant under negative write programs.
- The device with d = 24.9 Å shows almost no transient currents under both negative

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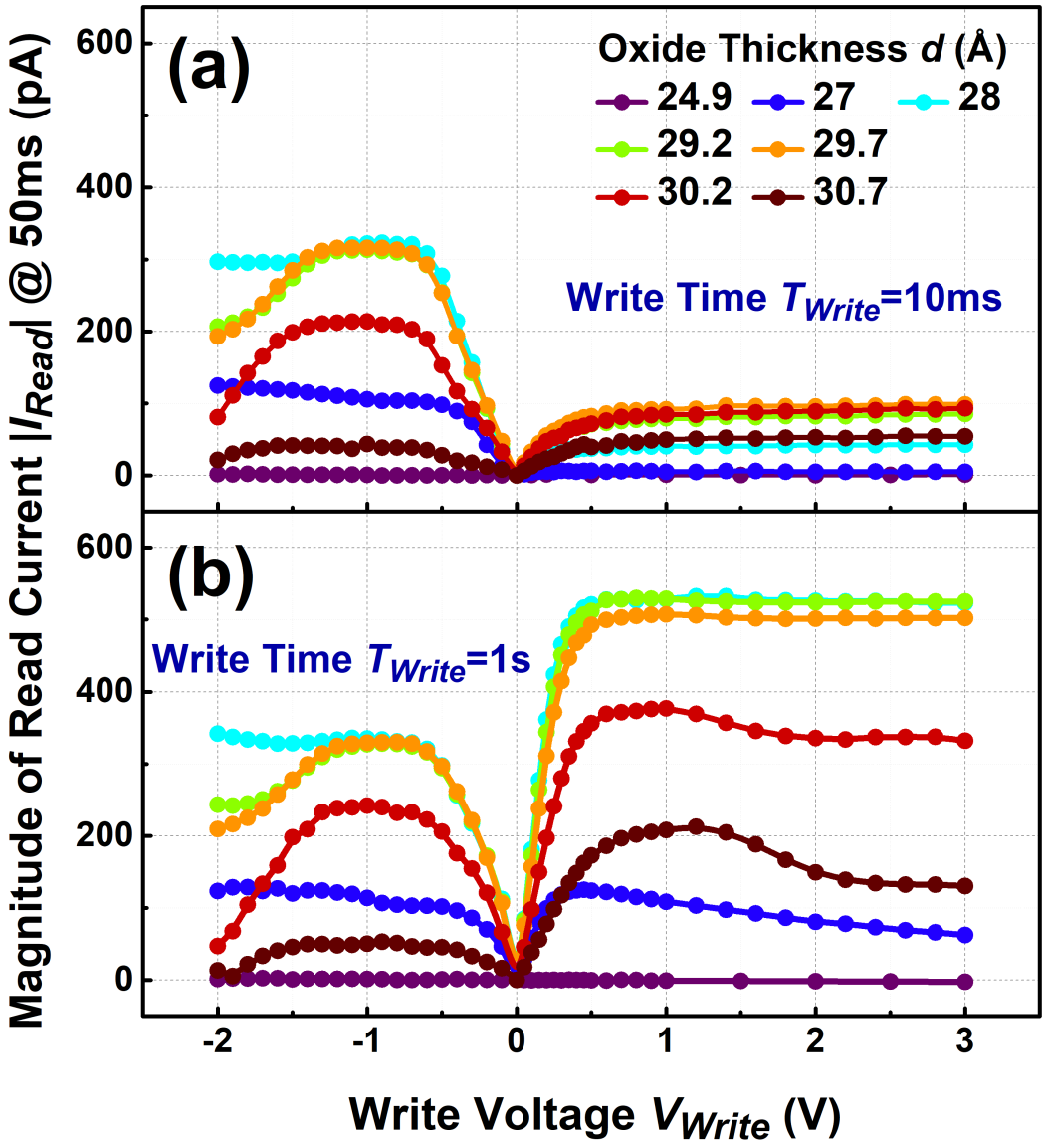

Figure 2–2. $I_{Read} - V_{Write}$ characteristics of the MISTD under write time T_{Write} = (a) 10 ms and (b) 1 s.

and positive write programs.

- MISTD demonstrates the largest magnitude of transient currents for d ranging from 28 to 30 Å under both negative and positive write programs.

- The magnitude of I_{Read} saturates (or even decreases) for V_{Write} < -0.5 V.

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These observations will be discussed further in this section. Additionally, it is observed that:

- Under positive write programs, the magnitude of I_{Read} saturates as V_{Write} increases, and the gate voltage at which I_{Read} saturates, denoted as $V_{Write,sat}$, is almost constant for devices with different d.

This phenomenon is referred to as the 'Saturation Phenomenon' of transient read currents under positive write programs. It requires further explanation, and a proposed mechanism will be discussed in **Section 2.4**.

Nevertheless, it is important to note that other phenomena have been observed in the experimental results, including:

- When V_{Write} < -0.5 V, the magnitude of I_{Read} decreases as V_{Write} becomes more negative for the device with a thicker oxide (d > 28 Å).

- Under positive write programs, $V_{Write,sat}$ increases for devices with a thicker oxide layer, e.g., d = 30.2 and 30.7 Å.

- When $V_{Write} > V_{Write,sat}$, the magnitude of I_{Read} decreases as V_{Write} becomes more positive for the device with a thicker oxide (d > 30 Å).

These effects are considered non-ideal and attributed to the presence of oxide charges. These complexities will be briefly discussed in **Section 2.7**, where these results will be reproduced by TCAD simulation with the inclusion of oxide charges. Detailed information on the transient current behavior when oxide charges are considered will be provided in the appendix for conciseness in the main dissertation.

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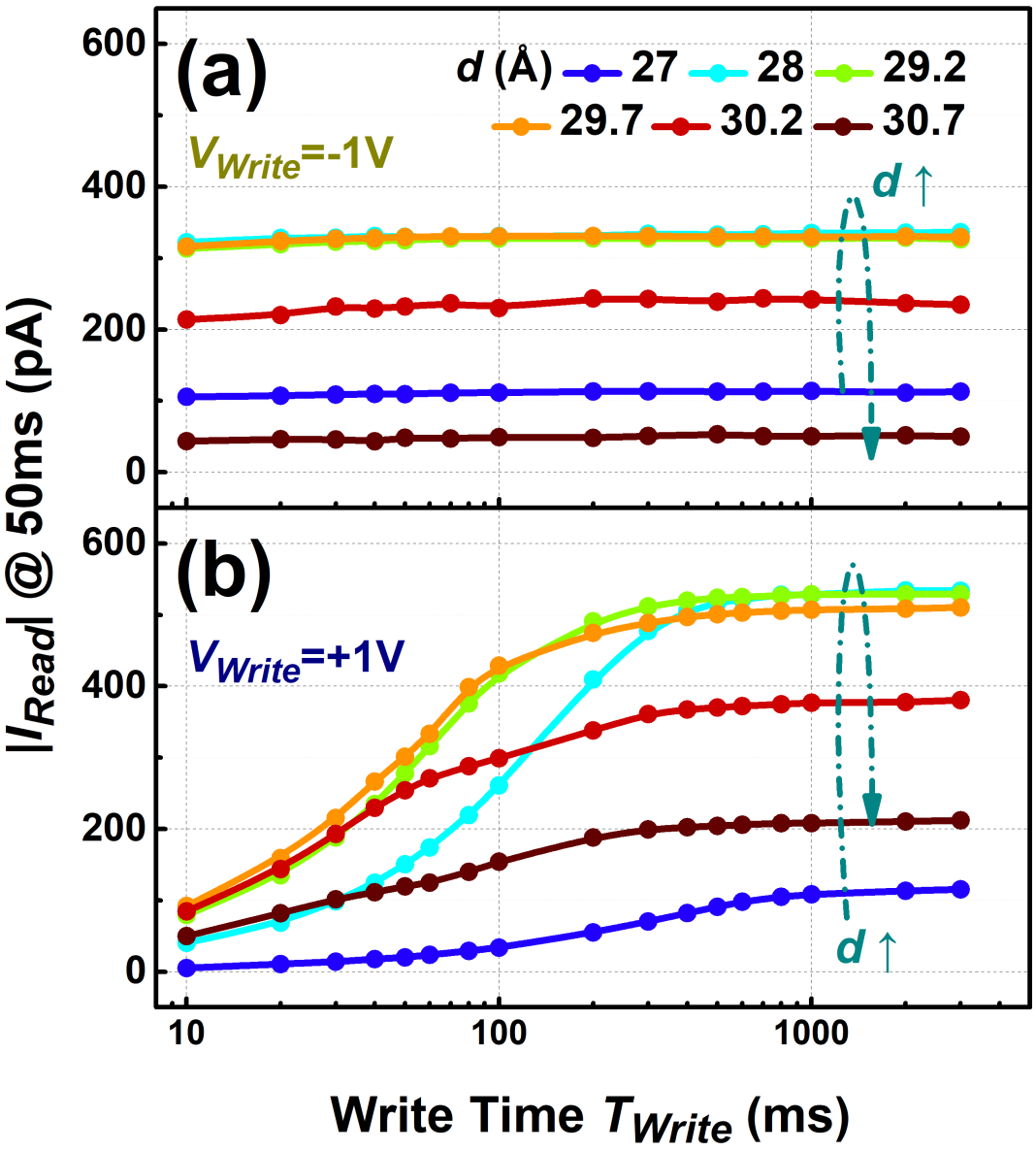

Figure 2–3. $I_{Read} - T_{Write}$ characteristics of the MISTD under write voltage V_{Write} = (a) -1 V and (b) + 1 V.

In **Figure 2–3** (a) and (b), the magnitude of I_{Read} is depicted against T_{Write} ranging from 10 ms to 3000 ms for V_{Write} = -1 V and +1 V, respectively. Notably, results for the device with d = 24.9 Å are excluded as it exhibits no transient currents. The following observations are noted:

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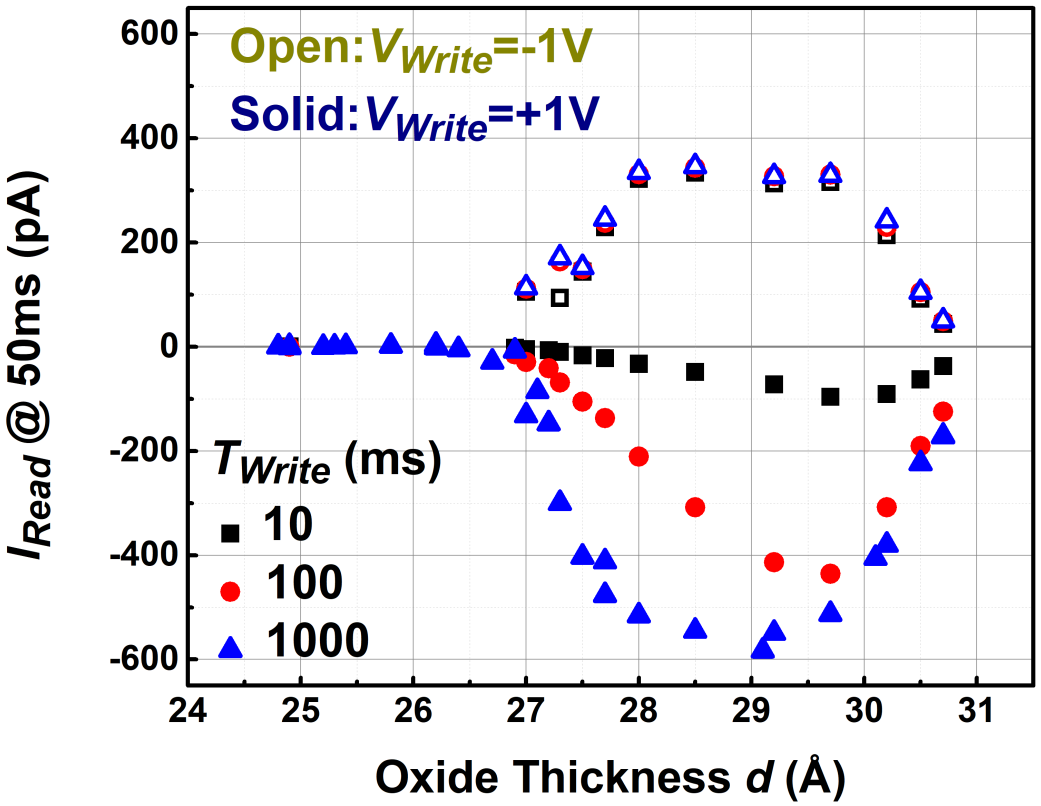

Figure 2–4. $I_{Read} - d$ characteristics of the MISTD under $V_{Write} = \pm 1$ V and T_{Write} = 10, 100 and 1000 ms.

- For all devices under a negative write program, I_{Read} remains constant for T_{Write} ranging from 10 ms to 3000 ms. Alternatively, it can be stated that I_{Read} saturates after $T_{Write} > 10$ ms for V_{Write} = -1 V.

- For all devices under a positive write program, the magnitude of I_{Read} increases as T_{Write} increases from 10 ms to around 1000 ms. Subsequently, I_{Read} saturates.

- Under both negative and positive write programs, the magnitude of I_{Read} initially increases and then decreases with d. The optimal d exhibiting the largest magnitude of I_{Read} is around 28-30 Å.

Figure 2–3 illustrates the $I_{Read} - d$ relationship under different voltage programs,

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including T_{Write} = 10, 100, and 1000 ms, and V_{Write} = ±1 V. The following observations are made:

- Devices with d < 27 Å exhibit almost no transient currents regardless of the write program.
- I_{Read} is independent of T_{Write} under negative write programs, while this is not the case under positive write programs.
- There is an optimal d to achieve the largest magnitude of the transient current, which is around 28-30 Å.

The observations from this three figures are consistent with each other, and the reasons behind these observations will be discussed shortly in this section. Additionally, it is noted that the peak value of I_{Read} under positive write programs may vary with T_{Write}. Further optimization is required to determine the optimal d in **Section 2.5**.

2.2.2 Negative Write Program

In this subsection, we delve into the transient current behavior under negative write programs, providing a comparison to the transient current behavior under positive write programs, which is our primary focus. The band diagrams for the MISTD under various conditions are illustrated in **Figure 2–5**. Subfigure (a) depicts the situation at the 0 V steady-state. The band diagram during the write procedure of a negative write program (V_{Write} < 0) is presented in subfigure (b), while the subsequent read procedure at 0 V is depicted in subfigure (c). It is essential to note that the time slice of the band diagrams is chosen at the millisecond time-scale. The sub-millisecond regime introduces additional complexities, which will be further discussed in **Chapter 3**.

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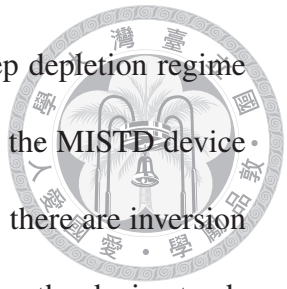

Apart from the devices with $d < 27$Å, that directly enter the deep depletion regime without an inversion regime, exhibiting no transient current behavior, the MISTD device resides in the inversion regime at the 0 V steady-state. In this regime, there are inversion electrons near the silicon surface. During the negative write program, the device tends to transition into the depletion or even the accumulation regime, indicating an excess of electrons during writing. The electrons near the silicon surface discharge through two mechanisms. Firstly, they diffuse into the silicon substrate. Secondly, they recombine with incoming holes. After the negative write programs, V_G is switched to 0 V to read the transient currents. As electrons diffuse away or recombine with holes, an electron deficiency near the silicon surface arises, resulting in a negative electron quasi-Fermi level (E_{Fn}). The device aims to restore to the 0 V steady-state, leading to either the diffusion of electrons from the silicon substrate or their generation in the depletion region. However, the former term is considerably lower than the latter term [92, 96, 97, 117] since the silicon substrate has p-type doping. Consequently, during the read procedure after a negative write program, the device essentially restores to the 0 V steady-state through the generation process in the depletion region, where electrons flow to the surface while holes flow to the substrate. This results in a negative hole current flowing from the silicon substrate to the back contact. Due to charge neutrality, the charges stored at the metal respond to the charges at the silicon side, leading to a positive gate transient current ($I_{Read} > 0$).

In accordance with the provided explanation, the magnitude of I_{Read} is dependent on the number of electrons that need to be generated during the read procedure. Larger electron deficiency results in a larger I_{Read}. The electron deficiency is influenced by the number of electrons discharged during the write procedure. For a negative write program

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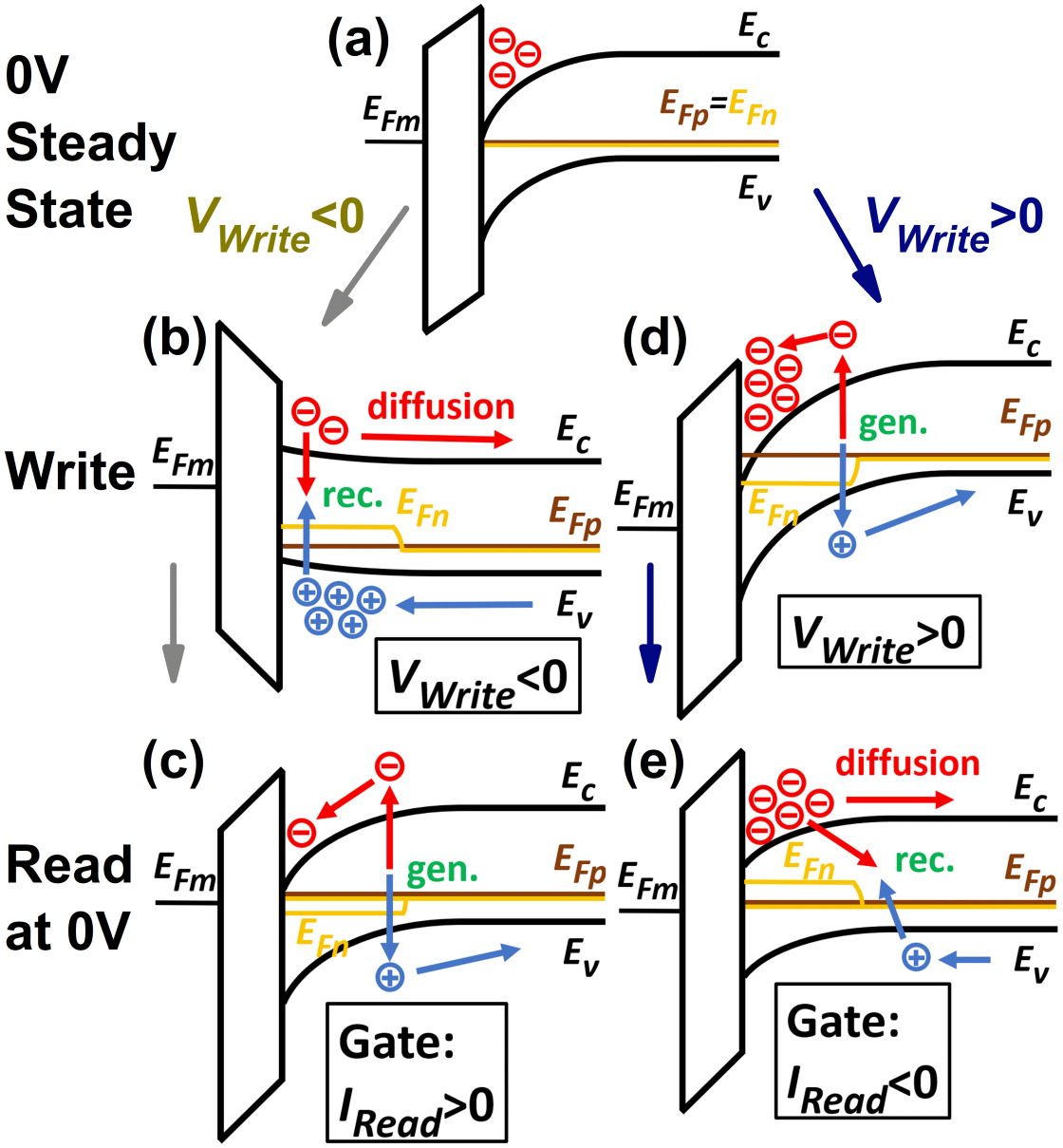

Figure 2–5. Schematic band diagrams of the MISTD (a) at 0 V steady state, during the (b) write procedure with $V_{Write} < 0$ and (c) subsequent (c) read procedure at 0 V, and during the (d) write procedure with $V_{Write} > 0$ and (e) subsequent read procedure at 0 V. (b)(c)(d) and (e) illustrate the band diagrams at millisecond time scales. The conduction band minimum (E_c), valence band maximum (E_v), and Fermi-level of the metal (E_{Fm}), hole quasi-Fermi level (E_{Fp}) and electron quasi-Fermi level are illustrated. The motions of electrons and holes are depicted as well.

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V_{Write} that biases the device into the depletion or accumulation regime during writing, numerous holes enter the silicon surface, leading to significant recombination with electrons. Consequently, the device swiftly transitions into the $V_G = V_{Write}$ steady-state during writing, rendering any further increase in T_{Write} ineffective in enhancing I_{Read}. Our experimental results indicate that it takes less than 10 ms to bias the device into the $V_G = V_{Write}$ steady-state during writing, as I_{Read} remains unchanged for T_{Write} ranging from 10 ms to 3 s.

Similarly, I_{Read} does not exhibit further increases as V_{Write} becomes more negative. The inversion charges in the silicon decrease nearly exponentially with the gate voltage from the inversion regime to the depletion and accumulation regimes [89, 91]. Given that the device is in the inversion regime at the 0 V steady-state, the electron deficiency remains nearly the same for V_{Write} biasing the device into the depletion and accumulation regimes. In other words, the electron deficiency becomes almost constant once V_{Write} is negative enough to repel all the inversion electrons in the silicon. Therefore, I_{Read} saturates with negative V_{Write}.

The peak in the $I_{Read} - d$ relation around 28-30 Å is attributed to the following reasons. For $V_G > V_{th}$, where V_{th} denotes the threshold voltage at which the device enters the strong inversion regime, as defined in **Chapter 1**, the device operates in the inversion regime, and the inversion charges Q_{inv} at V_G can be expressed as [118, 119]

$$|Q_{inv}| = C_{ox}(V_G - V_{th}) \tag{2.2}$$

For the devices examined in this study, $V_{th} \approx$ -0.2 V, irrespective of the oxide thickness d. When the device is in the strong inversion regime at the 0 V steady-state, $|Q_{inv}|$ is

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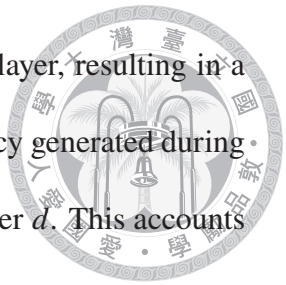

proportional to C_{ox}. Consequently, the MISTD with a thicker oxide layer, resulting in a lower C_{ox}, will have less $|Q_{inv}|$. Thus, the maximum electron deficiency generated during the negative write program will be smaller for the device with a smaller d. This accounts for the decreasing trend in the $I_{Read} - d$ for devices with $d > 30$ Å.

However, it is important to note that (2.2) is valid only if the device has not yet entered the deep depletion regime. In the deep depletion regime, $|Q_{inv}|$ does not increase with V_G. Therefore, for the device with a very thin oxide layer that directly enters the deep depletion regime, exhibiting almost no inversion regime, there is virtually no Q_{inv} in the silicon at the 0 V steady-state compared to the steady-state at a negative V_{Write}. Consequently, the negative write program cannot generate any electron deficiency, resulting in no transient current in the device. This explains the decreasing trend in the $I_{Read} - d$ for devices with $d < 28$ Å. As a result, MISTD with d = 28-30 Å will exhibit the largest I_{Read}.

2.2.3 Positive Write Program

The preceding subsection addressed the transient current behavior under negative write programs, serving as a comparison to the transient current behavior under positive write programs discussed in this subsection. **Figure 2−5** (d) and (e) illustrate the band diagrams during the write voltage programs ($V_{Write} > 0$) and the subsequent read procedure at 0 V, respectively, with **Figure 2−5** (a) showing the band diagram at the 0 V steady state for comparison. When a positive voltage pulse is abruptly applied to the gate for writing, the silicon tends to accumulate more inversion electrons. Electrons will be supplied by two means: diffusion from the silicon substrate and generation in the depletion region. Since the latter is much more significant than the former, as discussed in the previous subsection, the number of electrons supplied to the silicon surface during the write procedure

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is primarily determined by the generation process in the depletion region. Subsequently, the gate voltage is switched to 0 V for reading. Excess inversion electrons are stored at the silicon surface compared to the 0 V steady-state, resulting in a risen E_{Fn}. As the device gradually restores to the 0 V steady-state, the excess electrons will discharge in two ways. One way is direct diffusing backward to the substrate, resulting in a positive electron current at the silicon substrate. The other is recombined with incoming holes from the substrate, leading to a positive hole current at the silicon substrate. It is noticed that the polarity of current at the silicon substrate is defined positive when current flows from back contact into silicon substrate. Although the ratio between the electron and hole currents depends on E_{Fn}, which will be further discussed in **Chapter 3**, both components of these two currents are positive at the silicon substrate. Consequently, due to charge neutrality, positive charges at the gate flow out through the external circuit, resulting in a negative transient current $I_{Read} < 0$.

The magnitude of I_{Read} depends on how many inversion electrons can be stored during the write procedure. Since the excess inversion electrons stored during writing rely on the generation process in the depletion region, which is a relatively slow process and may take several hundred milliseconds or even several seconds to charge the device to the steady-state at a positive V_{Write}, the magnitude of I_{Read} increases with T_{Write} increasing from 10 ms to 1 s. For $T_{Write} \geq 1$ s, I_{Read} remains the same, and we consider that the device has almost charged to the steady-state at V_{Write} at the end of the write procedure. In short, under the positive write program, I_{Read} depends on T_{Write} due to the relatively slow charging process dominated by the generation.

The peak of the $I_{Read} - d$ relation under the positive write program is similar to the one

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under the negative write program, and the reason is also similar. The detailed discussion is as follows. For simplicity, let us focus on the case for $T_{Write} \geq 1$ s, where I_{Read} remains the same, and we can consider that the device is switched from the steady-state at V_{Write}. During the read process at 0 V, the device is turning from a deeper inversion to a shallower inversion, and the magnitude of I_{Read} depends on the excess inversion charges stored in the silicon. The excess inversion charges that can be produced by the write procedure at the beginning of the read procedure can be expressed as:

$$|Q_{inv,excess}(t = 0^+)| = |Q_{inv}(V_{Write})| - |Q_{inv}(V_{Read} = 0)| \tag{2.3}$$

where $Q_{inv,excess}$ represents the excess inversion charges, $t = 0^+$ represents the time point at the beginning of the read procedure, $Q_{inv}(V_G)$ represents the inversion charges in the device in the steady-state under a gate voltage V_G, and V_{Read} represents the gate voltage during the read procedure, which is 0 V here. According (2.2), $Q_{inv,excess}$ can be further expressed as:

$$|Q_{inv,excess}(t = 0^+)| = C_{ox}(V_{Write} - V_{Read}) \tag{2.4}$$

which is proportional to C_{ox}. As a result, the magnitude of I_{Read} decreases for the device with a larger d, explaining the decreasing trend for $d > 30$ Å. At the same time, (2.3) and (2.4) hold only if the device is still in the inversion regime at V_{Write}. When the oxide is very thin and the electrons leak easily, the device enters the deep depletion regime directly and can hardly store any inversion charges. As a result, the magnitude of I_{Read} decreases for $d < 28$ Å. The $I_{Read} - d$ characteristics under positive write programs were tested again

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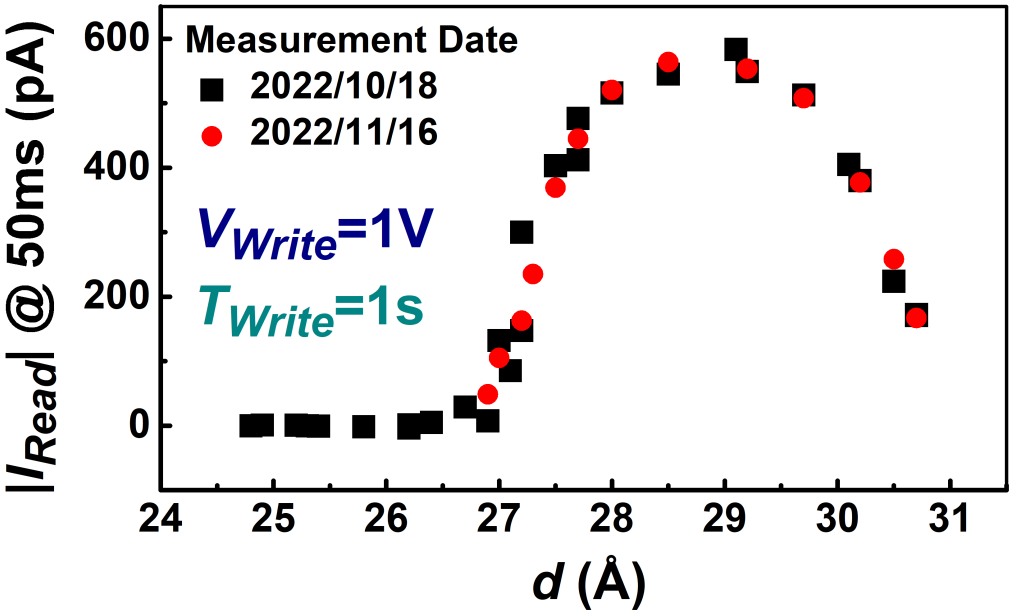

Figure 2–6. Reliability test of the $I_{Read}-d$ characteristics of the MISTD under V_{Write} = 1 V and T_{Write} = 1 s. The two measurement dates were separated by one month.

about one month later, with the devices unencapsulated and exposed to atmospheric conditions. The magnitude of I_{Read} only deviates slightly, as shown in **Figure 2–6**. Therefore, we believe that the transient current behavior of the MISTD devices is stable, reliable, reproducible, and can be used for dynamic memory applications.

While we have successfully explained the characteristics of I_{Read} concerning T_{Write} and d, the 'Saturation Phenomenon' remains elusive. This phenomenon refers to the saturation of I_{Read} as V_{Write} increases. In our previous discussions, we assumed that the magnitude of I_{Read} is directly proportional to the amount of inversion electrons stored in the silicon at the beginning of the read procedure, denoted as $Q_{inv,excess}(t = 0^+)$. This assumption appears reasonable, at the same time suggesting that, under this premise, the magnitude of I_{Read} should continuously increase with V_{Write} as long as the device at V_{Write} steady-state remains in the inversion regime, where (2.4) holds. However, as evident in

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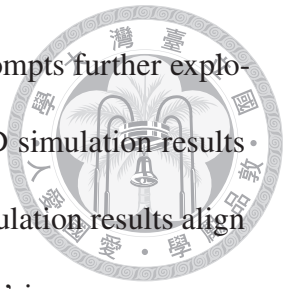

Figure 2–2 , this is NOT the case. The 'Saturation Phenomenon' prompts further exploration. In the subsequent section, **Section 2.3**, we will present TCAD simulation results detailing the transient current behavior of MISTD devices. These simulation results align well with the experimental findings, and the 'Saturation Phenomenon' is even more pronounced in the simulation. To unravel this phenomenon, we will leverage physical quantities obtained from the simulation, including silicon band bending, electron and hole densities in the sub-millisecond regime to study the saturation of transient read current at 50 ms. A detailed analysis of the mechanism will be provided in **Section 2.4**.

2.3 Simulation Results

In this section, we delve into the primary results obtained through TCAD simulations. The simulation setup and device cross-section were introduced in **Section 1.6**. In the simulation process, we initially solved the steady-state condition of the device under V_{Write}. Subsequently, the gate voltage was abruptly switched to 0 V, initiating the transient phase. This voltage program aims to reproduce scenarios where $T_{Write} \geq 1$ s, given that the MISTD has already reached a steady-state, as discussed in the preceding section. Although the voltage program used in the simulation is not an exact match to the experimental one, it significantly reduces simulation time while yielding results that align closely with the experimental findings. **Figure 2–7** and **Figure 2–8** present the TCAD simulation results for the $I_{Read} - V_{Write}$ and $I_{Read} - d$ characteristics, respectively, with the voltage program illustrated in the inset of **Figure 2–7** . Noted again that I_{Read} represents the gate transient current at 50 ms as previous defined. Key observations from the experimental results that are reproducible in the simulation include:

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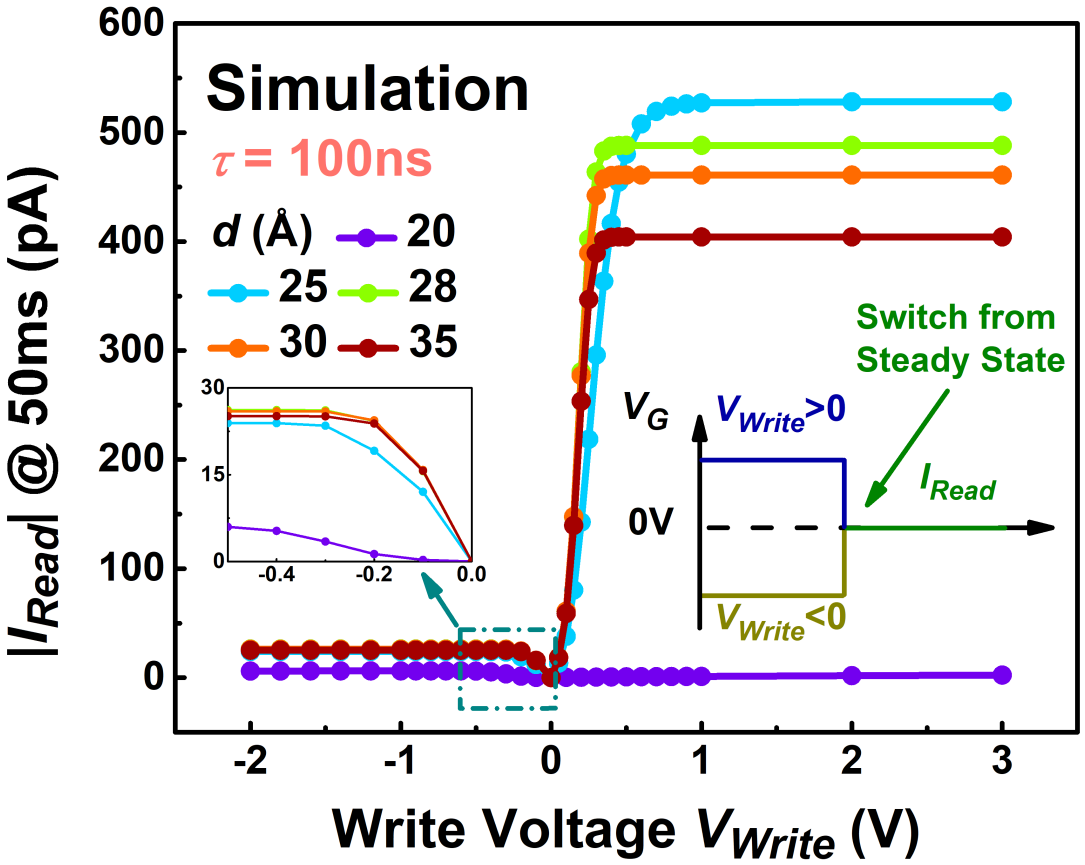

Figure 2–7. Simulation results of the $I_{Read}-V_{Write}$ characteristics. Left inset: Enlargement under low negative V_{Write}. Right inset: The voltage program used in the simulation. The device is switched from a steady-state at V_{Write} to 0 V. Both electron and hole carrier lifetimes are set as 100 ns.

- Devices with extremely thin oxide layers show minimal transient current behavior.
- There exists an optimal oxide thickness that maximizes I_{Read}.
- The magnitude of I_{Read} saturates with increasing V_{Write} under positive write programs, and $V_{Write,sat}$ remains consistent across devices with different d.

While there are some discrepancies from the experimental results, such as

- the magnitude of I_{Read}, especially under negative write programs,
- the saturation voltage value under positive write programs,

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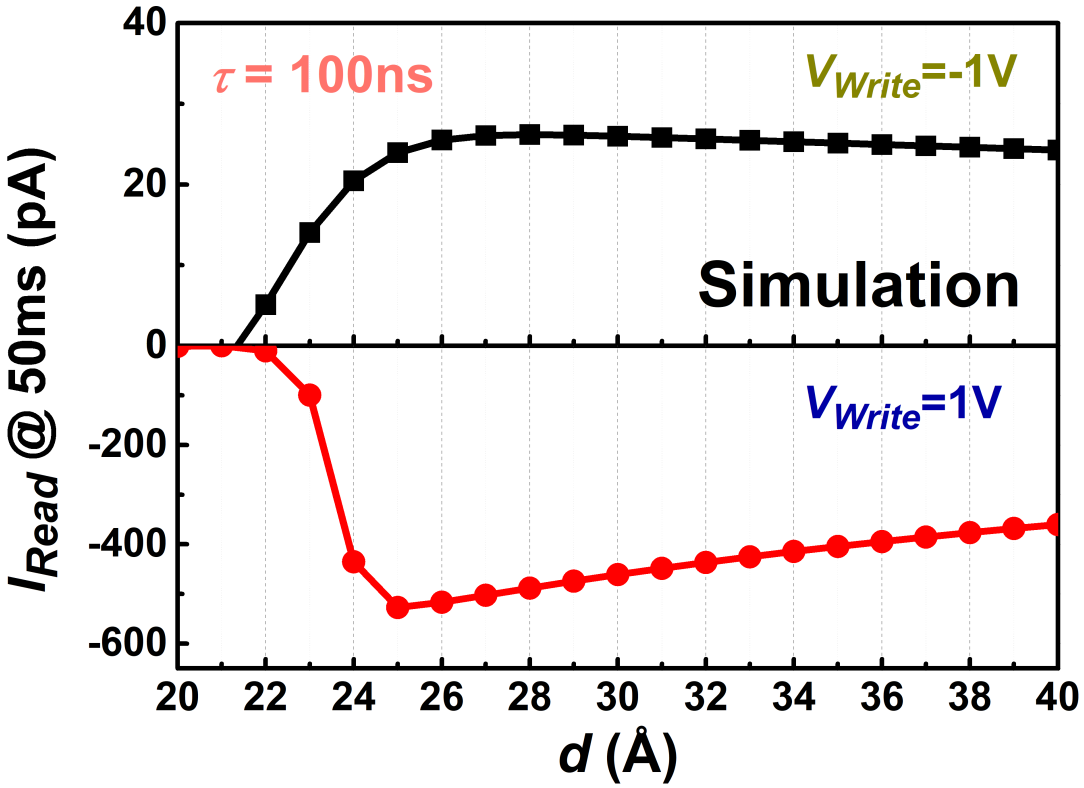

Figure 2–8. Simulation results of the $I_{Read} - d$ characteristics.

- the peak position and decreasing trend of the $I_{Read} - d$ relation,

these variations can be accounted for or reproduced by adjusting the carriers' lifetime τ and incorporating the inevitable oxide charges Q_{ox}. The simulations in **Figure 2–7** and **Figure 2–8** employed $\tau_n = \tau_p = \tau = 10^{-7}$ s as the default setting, where τ_n and τ_p represent the lifetimes of electrons and holes, respectively. To maintain a more organized dissertation structure and prioritize the discussion of the crucial 'Saturation Behavior', we will address the impact of lifetime and oxide charges later in **Section 2.6** and **Section 2.7**. These sections will demonstrate that by adjusting τ and Q_{ox}, the observed deviations can be reproduced and explained.

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2.4 Mechanism of The Saturation Phenomenon

2.4.1 Mechanism Details

In this section, we will propose a detailed mechanism to explain the 'Saturation Phenomenon' under the positive write programs with the assistance of the simulation. First and foremost, we maintain the assumption that the magnitude of the transient current during the transient ($I_{Read}(t)$) is proportional to the excess inversion charges at the specific time point ($Q_{inv,excess}(t)$). This assumption is based on the fact that the excess inversion charges stored at the silicon surface will induce a risen E_{Fn} at the surface, which correlates logarithmically to the excess inversion charges. The silicon side of the device will then resemble a one-sided diode in the forward-bias regime. In this regime, the currents, whether the diffusion term or the recombination term, depend exponentially on E_{Fn}. Therefore, we find the following assumption to be reasonable:

$$|I_{Read}(t)| \propto |Q_{inv,excess}(t)| = |Q_{inv}(t) - Q_{inv}(V_{Read} = 0)| \tag{2.5}$$

where $Q_{inv}(t)$ is the inversion charges at the specific time point, and $Q_{inv}(V_{Read} = 0)$ is the inversion charges at the 0 V steady-state as previously defined. The fundamental voltage balance equation during the transient necessitates the following:

$$V_{Read} - V_{Fb} = -\frac{Q_s(t)}{C_{ox}} + \psi_s(t) \tag{2.6}$$

$$\cong -\frac{Q_{inv}(t)}{C_{ox}} + \psi_s(t) \tag{2.7}$$

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Here, $Q_s(t)$ can be approximated by $Q_{inv}(t)$, since the device is now in the strong inversion regime, and the inversion charges dominate the total charges in the silicon. Now, consider the scenario where $V_{Write} > V_{Write,sat}$, where $V_{Write,sat}$ is the write voltage where current saturation occurs. According to (2.7), when too many inversion charges accumulate in the silicon, ψ_s will decrease significantly, potentially reaching very small or even negative values. Consequently, electrons will diffuse easily due to the low ψ_s. Of greater significance, holes will swiftly flow in, engaging in rapid recombination with the excess inversion charges. This rapid recombination process leads to a substantial reduction in the number of inversion charges in a very short time, ultimately allowing ψ_s to become sufficiently large.

Figure 2–9 illustrates the temporal evolution of ψ_s when switching from V_{Write} = 0.3, 1, and 2 V to 0 V, where $V_{Write} > V_{Write,sat}$ in the latter two cases. In the case of V_{Write} = 2 V, $\psi_s(t)$ is initially negative due to the presence of a large $Q_{inv}(t)$. However, $\psi_s(t)$ undergoes a rapid increase over time and converges to the value observed with V_{Write} = 1 V at approximately 150 ns. Noted that the inversion charge can be expressed as follows:

$$|Q_{inv}(t)| = C_{ox}[V_{Read} - V_{Fb} - \psi_s(t)] \tag{2.8}$$

The two curves of ψ_s with V_{Write} = 1 and 2 V merged after 150 ns. In essence, this signifies a minimum threshold of ψ_s after 150 ns, signifying the presence of a saturated stored inversion charge and a consequent saturated transient read current. The saturated stored inversion charge can be expressed as:

$$|Q_{inv,sat}(t)| = C_{ox}[V_{Read} - V_{Fb} - \psi_{s,min}(t)] \tag{2.9}$$

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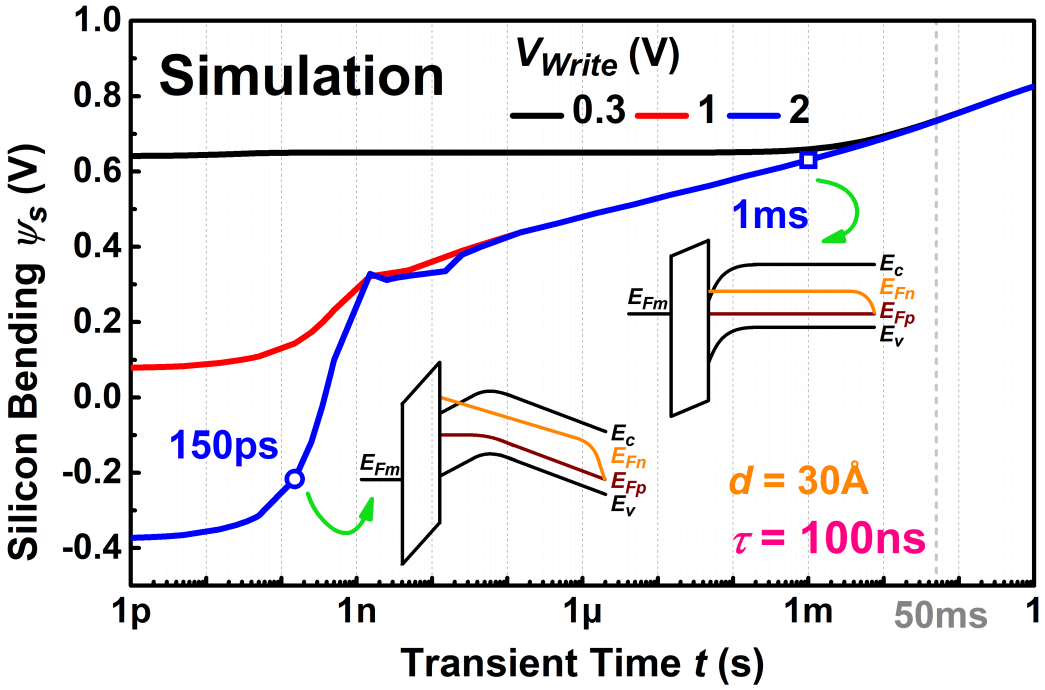

Figure 2–9. Simulation results of $\psi_s - t$ relation for the device with $d = 30$ Å when switching from $V_{Write} = 0.3$, 1 and 2 V to 0 V. Insets: Schematics band diagrams at $t = 150$ ps and 1 ms.

for $t \geq 150$ ns, where $\psi_{s,min}(t)$ represents the minimum requirement for silicon band bending depending on the transient time. The investigation into the minimum requirement of ψ_s is depicted in **Figure 2–10**, illustrating the correlation between ψ_s and V_{Write} at various time points. The graph clearly shows the existence of a $\psi_{s,min}(t)$ for $t \geq 150$ ns. This implies that, even though a substantial $Q_{inv}(t = 0^+)$ may be stored for a significantly high V_{Write}, $Q_{inv}(t)$ will decrease to the saturation value within the initial 150 ns, ensuring that $\psi_s(t)$ meets the minimum requirement.

The significant drop in Q_{inv} can be attributed to the atypical band diagram resulting from the very small (or even negative) value of ψ_s in the first 150 ns. The insets in **Figure 2–9** present a comparison of the band diagrams at 150 ps and 1 ms for $V_{Write} = 2$ V, where the one at 1 ms is similar to **Figure 2–5**. Excess electrons either diffuse out

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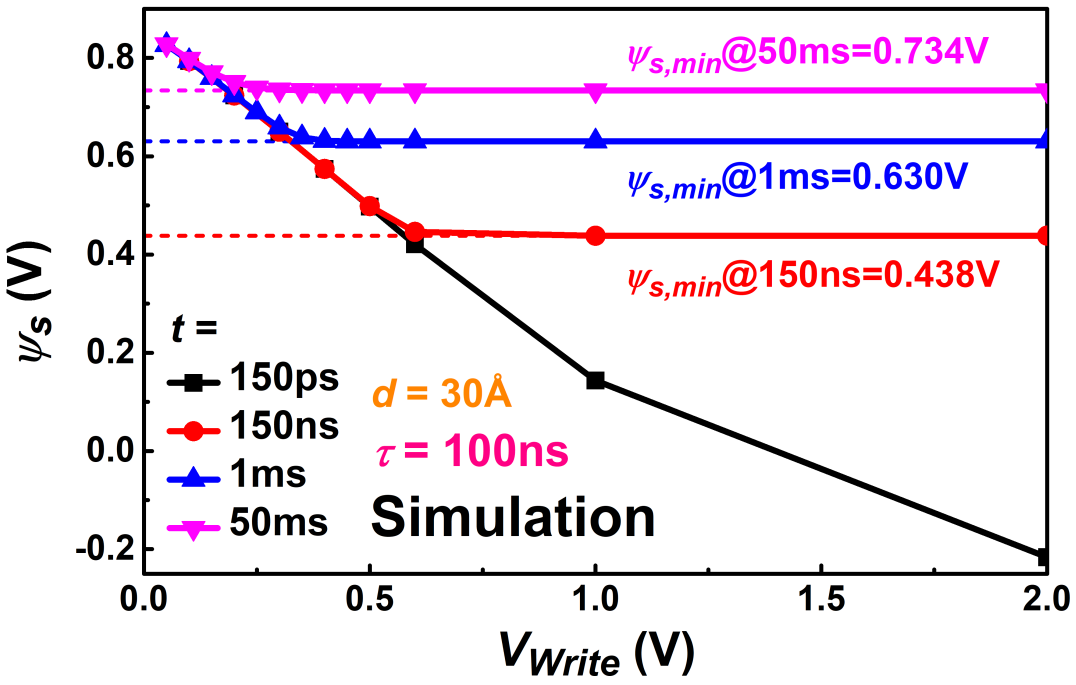

Figure 2–10. Simulation results of $\psi_s - V_{Write}$ relation for the device with $d = 30$ Å at time points $t = 150$ ps, 150 ns, 1 ms and 50 ms. There will be a minimum requirement for ψ_s, denoted as $\psi_{s,min}$, for transient time $t \geq 150$ ns.

or get recombined at a relatively slow rate. However, the band diagram at 150 ps is highly unusual, as depicted in **Figure 2–11** along with the carrier density. Despite the local downward band bending caused by the large number of inversion charges, the overall effect is upward bending, as indicated by $\psi_s < 0$. In this scenario, a substantial number of holes enter, and both the electron and hole densities are very high, leading to a large recombination rate over a wide range inside the silicon. The intense recombination significantly reduces $Q_{inv}(t)$ in the first 150 ns, until it is sufficiently low for $\psi_s(t)$ to meet the minimum requirement. **Figure 2–12** illustrates the time evolution of the maximum electron density in the silicon and the hole density at the silicon surface. It is evident that for $V_{Write} = 2$ V, there is a substantial increase in the hole density, accompanied by a significant decrease in the electron density, occurring within the range of hundreds of picoseconds to hundreds

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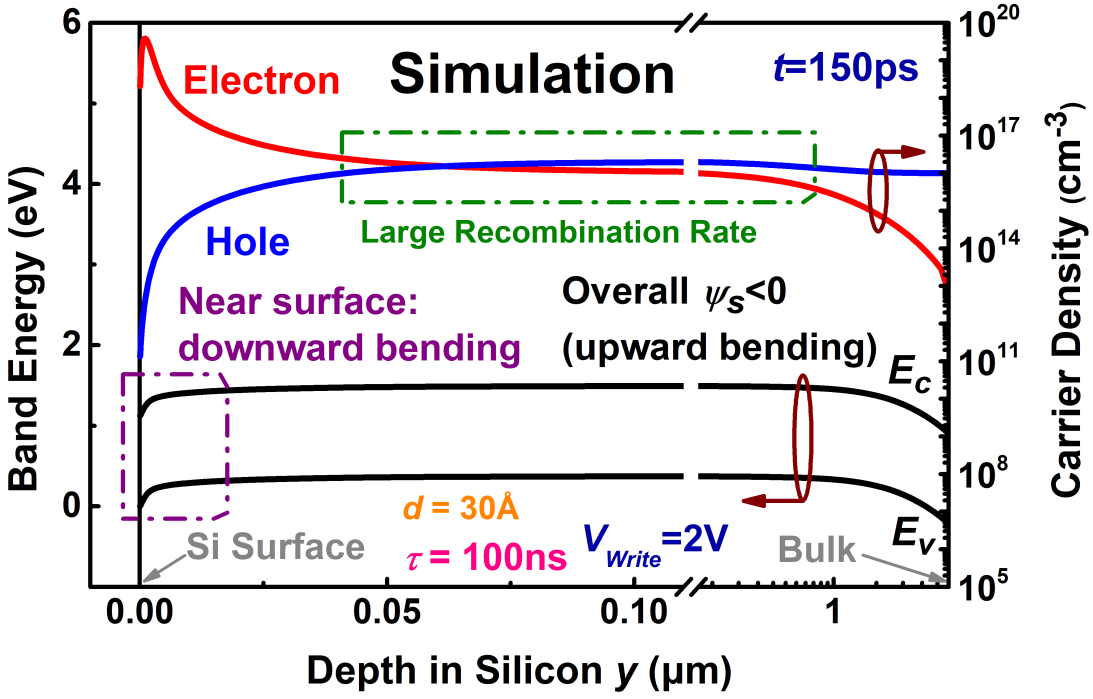

Figure 2–11. Simulation results of the band diagram for the device with $d = 30$ Å at 150 ps after a write program with $V_{Write} = 2$ V. The origin is set at the Si/SiO_2 surface, and y represents the depth inside the silicon from the surface. The electron and hole densities are also shown in the figure.

of nanoseconds. The electron density then follow the one for $V_{Write} = 1$ V afterwards, supporting this mechanism. Moreover, this mechanism also suggests that when the inversion charges stored in the silicon exceed $Q_{inv,sat}(t = 150\text{ ns})$, the read current will reach the saturation level. When switched from the steady-state at V_{Write} in the inversion regime, the inversion charges stored in the silicon at the beginning of the transient is

$$|Q_{inv}(t = 0^+)| \cong Q_{inv}(V_{Write}) \cong C_{ox}(V_{Write} - V_{th}) \tag{2.10}$$

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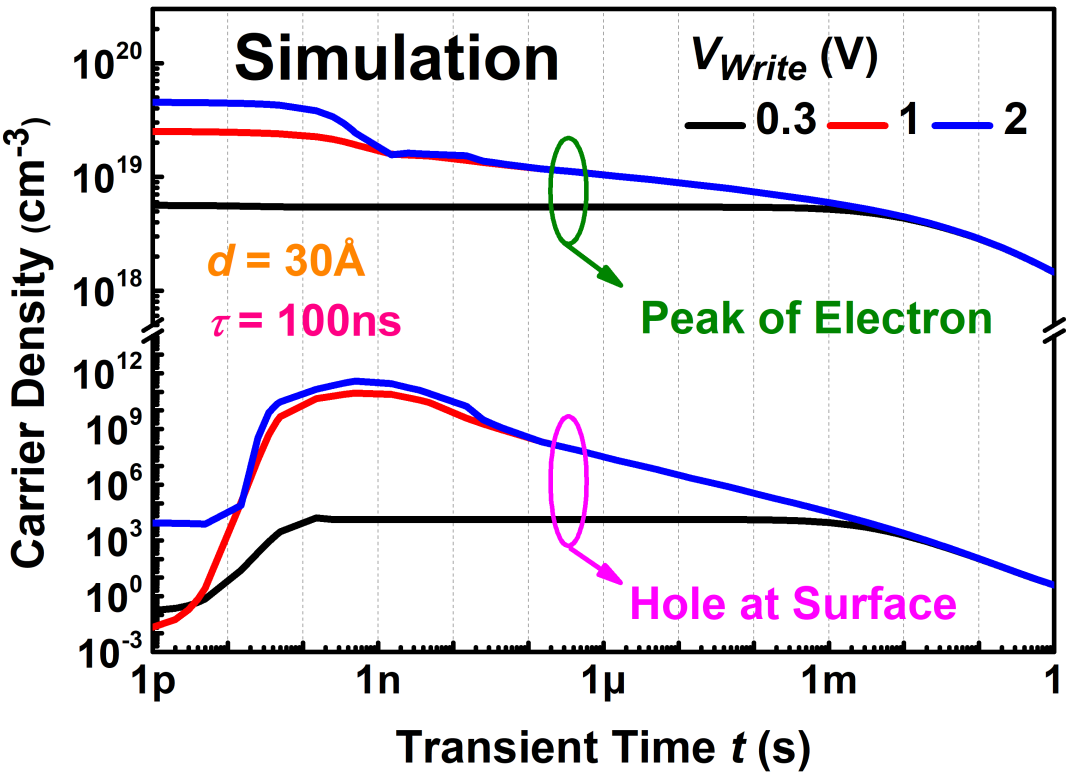

Figure 2–12. Simulation results of the time evolution of the maximum electron density in the silicon and the hole density at the silicon surface for the device with $d = 30$ Å under positive write programs with $V_{Write} =$ 0.3, 1 and 2 V.

Saturation happens for $V_{Write} \geq V_{Write,sat}$, where the requirement for $V_{Write,sat}$ is

$$|Q_{inv}(V_{Write,sat})| \geq |Q_{inv,sat}(t = 150 \text{ ns})| \tag{2.11}$$

and this will finally result in

$$V_{Write,sat} \cong V_{th} + V_{Read} - V_{Fb} - \psi_{s,min}(t = 150 \text{ ns}) \tag{2.12}$$

For the simulation, $V_{Write,sat} \cong -0.2 + 0 + 0.98 - 0.438 \cong 0.34$.

However, another criterion must be met for saturation to occur. Specifically, the write

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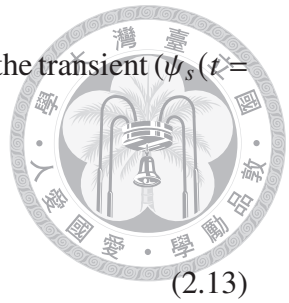

voltage should be sufficiently high to ensure that ψ_s at the beginning of the transient ($\psi_s(t = 0^+)$) is lower than $\psi_{s,min}(t = 150\text{ ns})$. This necessitates

$$\psi_s(t = 0^+) < \psi_{s,min}(t = 150\text{ ns}) \tag{2.13}$$

Since Q_{inv} hardly changes at the onset of the transient, (2.7) at the moment just before and after the onset of the transient implies

$$V_{Read} - V_{Write} = \psi_s(t = 0^+) - \psi_s(t = 0^-) \tag{2.14}$$

Therefore, the representation for $V_{Write,sat}$ becomes

$$V_{Write,sat} = V_{Read} + \psi_s(t = 0^-) - \psi_{s,min}(t = 150\text{ ns}) \tag{2.15}$$

The simulation data at steady-state indicates that the value of $\psi_s(t = 0^-)$ varies from 0.94 to 0.99 V when V_{Write} ranges from 0.3 to 0.6 V. Consequently, the predicted $V_{Write,sat}$ is approximately 0.5 V, which is larger than the one predicted by (2.12). Since both criteria must be satisfied to achieve saturation, we consider $V_{Write,sat}$ to be around 0.5 V, which closely aligns with the value observed in **Figure 2–7** .

In summary, (2.5) and (2.9) successfully explain the saturation of the read current. Additionally, the model predicts a decreasing trend in the magnitude of saturated I_{Read} as d increases, except for cases where the oxide is too thin to accumulate inversion charges to the saturated value due to severe tunneling. This trend arises because C_{ox} is lower for a larger d. (2.12) or (2.15) provides an approximate expression for $V_{Write,sat}$, which is

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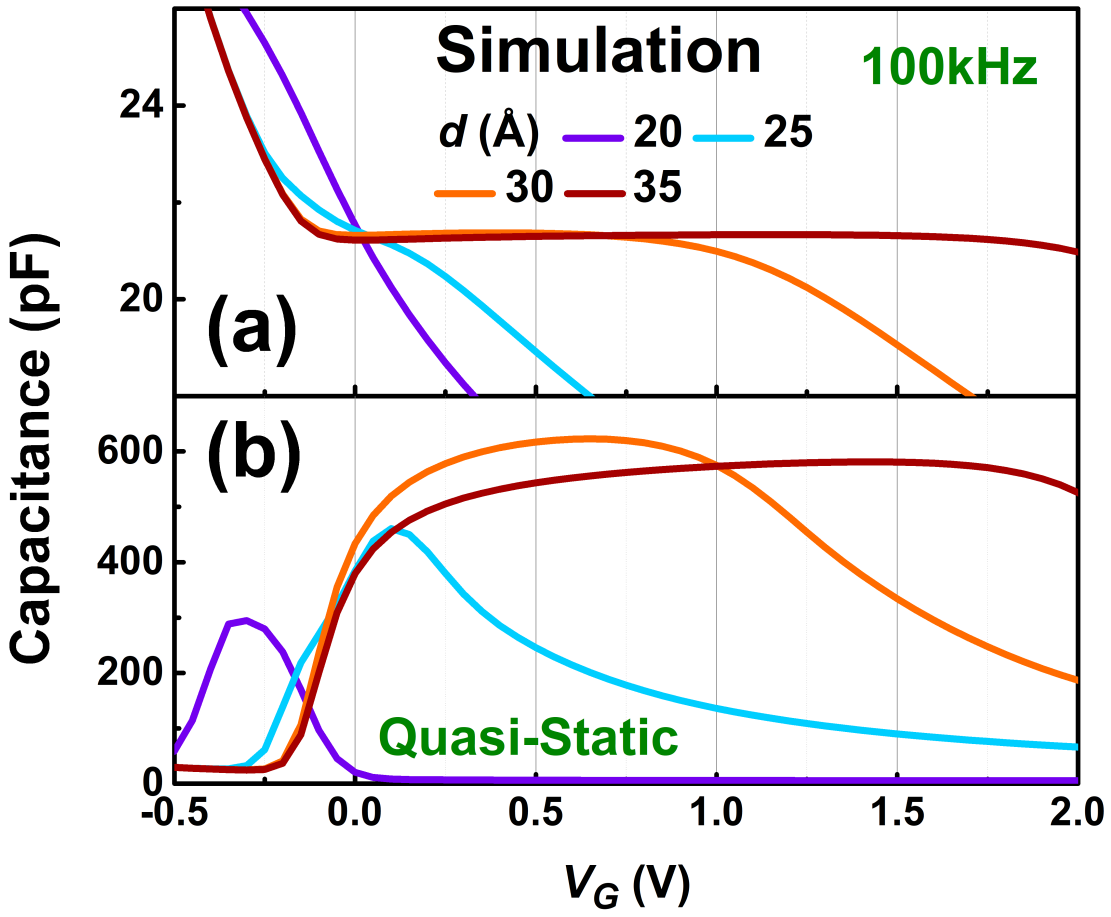

Figure 2–13. Simulation results of the (a) 100 kHz and (b) quasi-static $C-V$ characteristics in the inversion and deep depletion regime for the devices with various oxide thickness.

independent of the oxide thickness. The predicted value is also in close agreement with the simulation result.

It is important to note that the model can also aid in understanding the saturation of read current under negative write programs. In this scenario, I_{Read} will be proportional to the deficiency of Q_{inv} and will follow the same relationship as described by (2.5). Consequently, I_{Read} saturates for a sufficiently negative V_{Write} that can expel all the inversion charges.

However, for the device with a relatively thin oxide, the proposed mechanism requires

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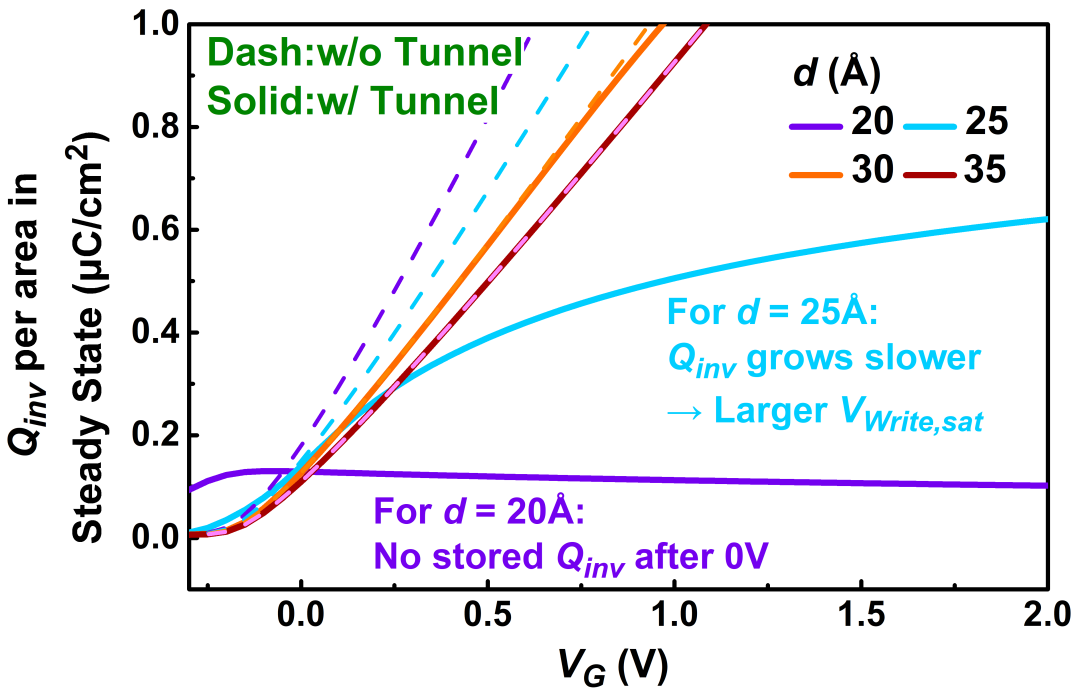

Figure 2–14. Inversion charges Q_{inv} in the steady-state condition for devices with various oxide thickness, calculated utilizing the simulated 100 kHz and quasi-static $C - V$ curves. The results not considering quantum tunneling effect are also presented for comparison.

modification due to the inability of inversion charges to accumulate as in a traditional MIS capacitor, given the tunneling nature of an MISTD. The simulation results of high-frequency (100 kHz) and quasi-static $C - V$ characteristics for devices with various oxide thicknesses, shown in **Figure 2–13** (a) and (b), respectively, can be utilized to calculate the depletion charges and total charges in the silicon [91]. Subsequently, subtracting the depletion charges from the total charges yields the inversion charges Q_{inv}. The corresponding Q_{inv} under different gate voltages is presented in **Figure 2–14** . Results with the quantum tunneling model disabled in the simulation are also included for comparison. In the case of an oxide layer thicker than 30 Å, the device operates in the inversion regime after 0 V, where the classic relation (2.2) is applicable. However, for a thinner oxide layer, a deviation from this relationship occurs. For $d = 20$ Å, no inversion charge is stored after

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0 V, indicating an absence of transient current in a device with d = 20 Å. For d = 25 Å, although the increase is slower compared to the classic relationship, Q_{inv} can still be stored, reaching the level of $Q_{inv,sat}$ only at a larger $V_{Write,sat}$. This observation explains the later saturation of I_{Read} as observed in **Figure 2–7**.

2.4.2 Other Evidences

Combined with the revision when tunneling effects are considered, the simple mechanism proposed in the previous subsection successfully explains the phenomenon of the 'Saturation Phenomenon' under positive write programs. In this subsection, we provide additional evidence supporting this mechanism.

Firstly, we vary the read voltage (V_{Read}) under positive write programs. The resulting I_{Read} is plotted against $V_{Write} - V_{Read}$ in **Figure 2–15** (a) and (b) for the experimental and simulation results. Noted again I_{Read} is extracted from the gate transient current at 50 ms. According to (2.5) and (2.9), the magnitude of $I_{Read,sat}$ is larger for a larger V_{Read}, consistent with the results presented in **Figure 2–15**. At the same time, according to (2.12) and (2.15), $V_{Write,sat} - V_{Read}$ remains constant when V_{Read} changes, as observed in **Figure 2–15**.

Next, we alter the work function (ϕ_m) in the TCAD simulation to examine the proposed mechanism. The resulting $C - V$ curves are shown in **Figure 2–16** (a). According to the flat-band voltage equation (1.1), V_{Fb} decreases as ϕ_m decreases, resulting in the left shift of the $C - V$ curves. At the same time, according to (2.5) and (2.9), the increase of V_{Fb}, resulting from the increase of ϕ_m, leads to the decrease in the magnitude of $I_{Read,sat}$. Furthermore, since the expression for V_{th} (1.5) also contains V_{Fb}, the influence of V_{Fb} from the varying of ϕ_m is canceled out in (2.12), resulting in an unchanged $V_{Write,sat}$ for different

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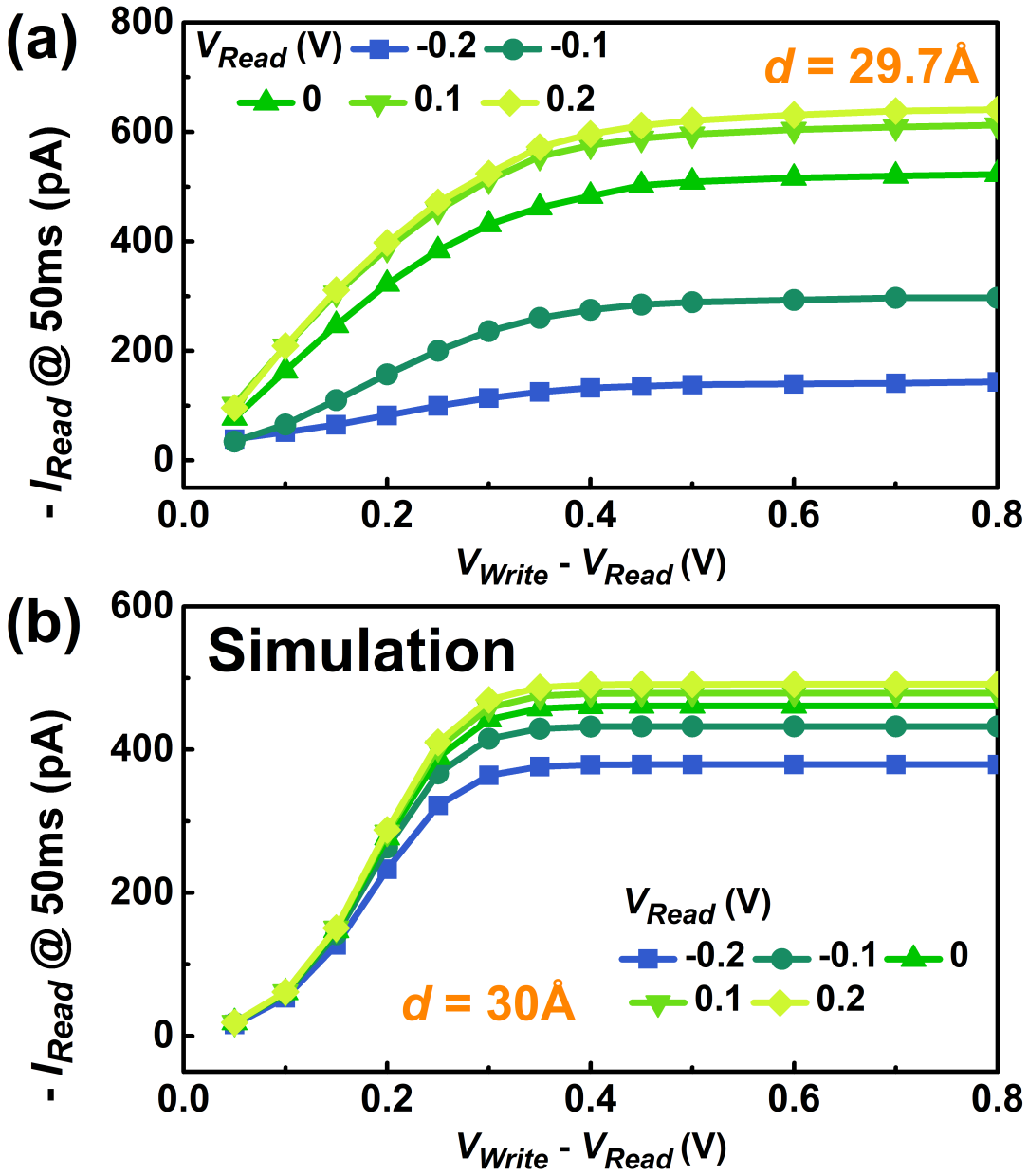

Figure 2–15. (a) Experimental and (b) simulation results of the $I_{Read} - (V_{Write} - V_{Read})$ characteristics for various V_{Read}. The oxide thicknesses are 29.7 Å and 30 Å for the experiment and simulation, respectively.

ϕ_m. These predictions are observable in **Figure 2–16** (b), displaying the $I_{Read} - V_{Write}$ relation for various work functions. The experimental and simulation results align well with the predictions, serving as evidence for the proposed mechanism.

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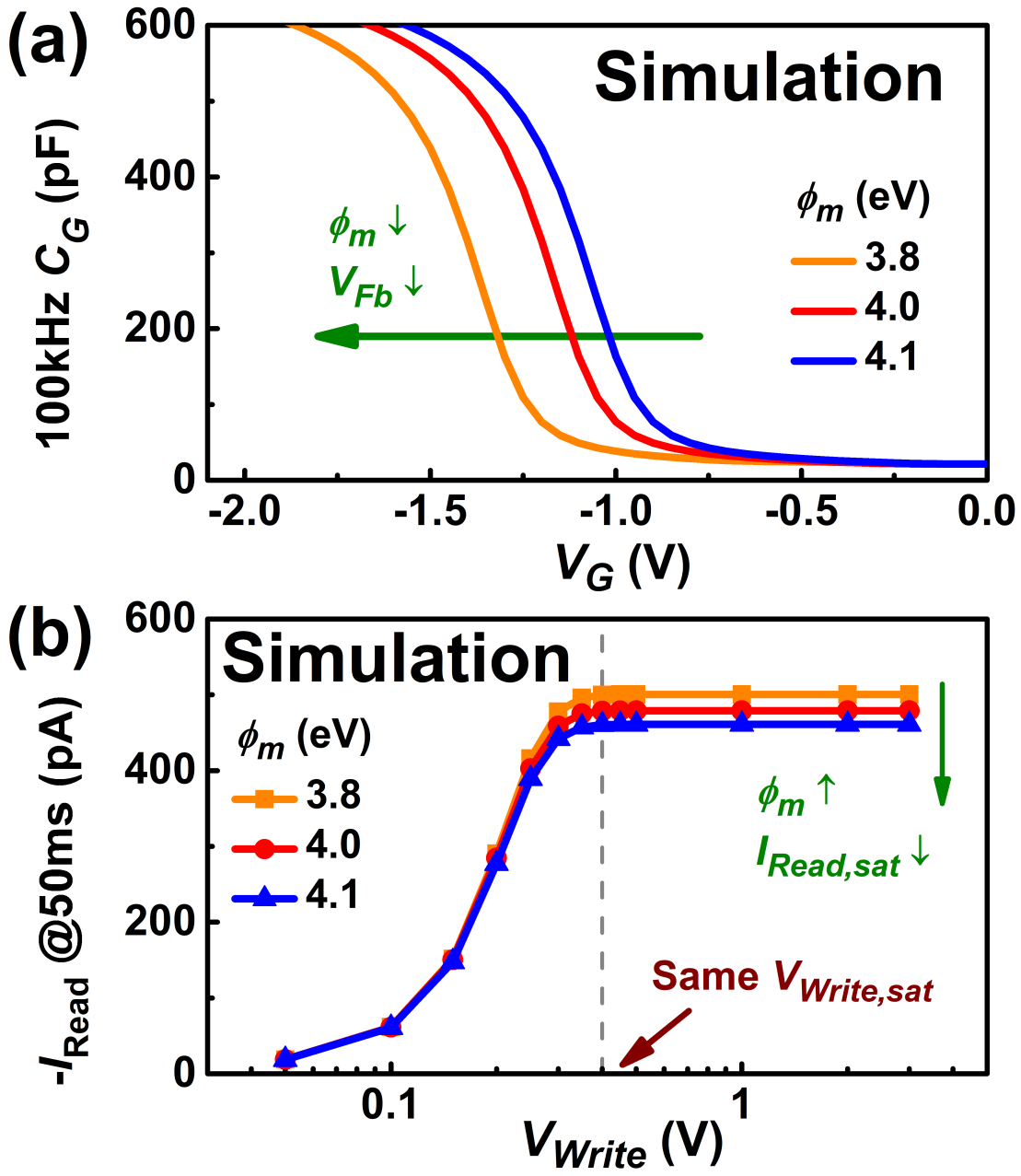

Figure 2–16. (a) The simulation $C-V$ and (b) $I_{Read}-V_{Write}$ characteristics for devices with various work functions.

2.5 Optimal Parameters for The Planar MISTD

We have presented the experimental and simulation results of I_{Read} and explained the mechanism of the 'Saturation Phenomenon' in the previous sections. In this section, we

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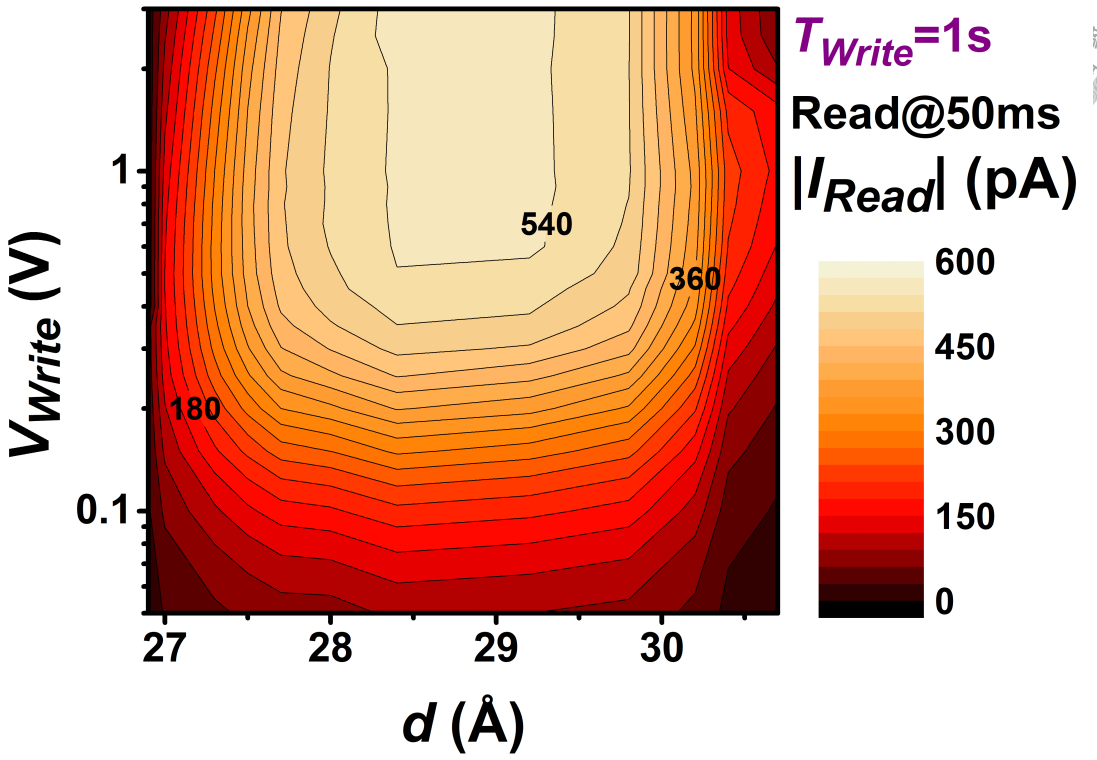

Figure 2–17. Contour map of $|I_{Read}|$ versus d (x-axis) and V_{Write} (y-axis) when T_{Write} = 1 s.

will discuss the optimization of the design of the Planar MISTD when used for dynamic memory applications. We will employ a positive voltage program to 'Write 1', resulting in a negative transient current serving as 'Read 1', and a zero voltage program to 'Write 0', resulting in a zero transient current serving as 'Read 0'. Since the memory window is determined by the magnitude of the transient current after the positive write program, on the one hand, we want I_{Read} to be as large as possible. However, on the other hand, we do not want V_{Write} and T_{Write} to be too high for power-conserving considerations. Therefore, we need to carefully choose the write voltage and write time for the write program and the oxide thickness for the MISTD to have a large I_{Read} and low write power simultaneously.

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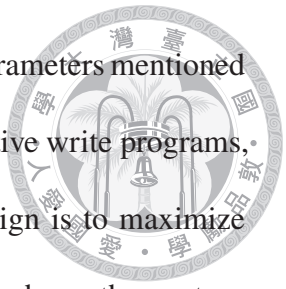

We propose that by utilizing the contour map regarding the three parameters mentioned above, we can better design the optimal parameters. Since under positive write programs, I_{Read} increases with T_{Write} until $T_{Write} \geq 1$ s, if the goal of the design is to maximize the magnitude of I_{Read}, $T_{Read} = 1$ s should be chosen. **Figure 2–17** shows the contour map of I_{Read} versus V_{Write} and d when $T_{Write} = 1$ s. Noted again that I_{Read} represents the gate transient current at 50 ms. The shallower color indicates a larger magnitude of I_{Read}. According to the contour map, the device with $d = 29.2$ Å has the largest $|I_{Read}|$. At the same time, $|I_{Read}|$ saturates when $V_{Write} \geq 0.5$ V. Therefore, to achieve the maximum magnitude of I_{Read}, we suggest using $V_{Write} = 0.5$ V and $T_{Write} = 1$ s for the device with $d = 29.2$ Å.

However, in some cases, T_{Write} is set as a fixed value to meet the required operation frequency. In such scenarios, a contour map of I_{Read} versus T_{Write} and d needs to be generated to determine the optimal parameters. The contour map with $V_{Write} = 1$ V is depicted in **Figure 2–18**. We choose 1 V since, when $T_{Write} \leq 1$ s, I_{Read} often continues to increase with V_{Write}; thus, an intermediate value of V_{Write} is selected. The blue dashed line in the contour map represents the oxide thickness that yields the largest $|I_{Read}|$ for a given T_{Write}. For instance, for $T_{Write} \geq 100$ ms, the device with d ranging from 28.5 to 29.5 Å is the optimal choice. For $T_{Write} \leq 100$ ms, it is preferable to grow the oxide within the 29.5 to 30.5 Å range. Consequently, if operational speed is the top priority, we recommend using $V_{Write} = 1$ V and $T_{Write} = 10$ ms for the device with $d = 29.7$ Å.

In practical applications, the device is fabricated with a fixed oxide thickness that cannot be altered. Therefore, it would be beneficial to have a contour map of $|I_{Read}|$ against V_{Write} and T_{Write}. An example is presented in **Figure 2–19**, with $d = 29.7$ Å. From

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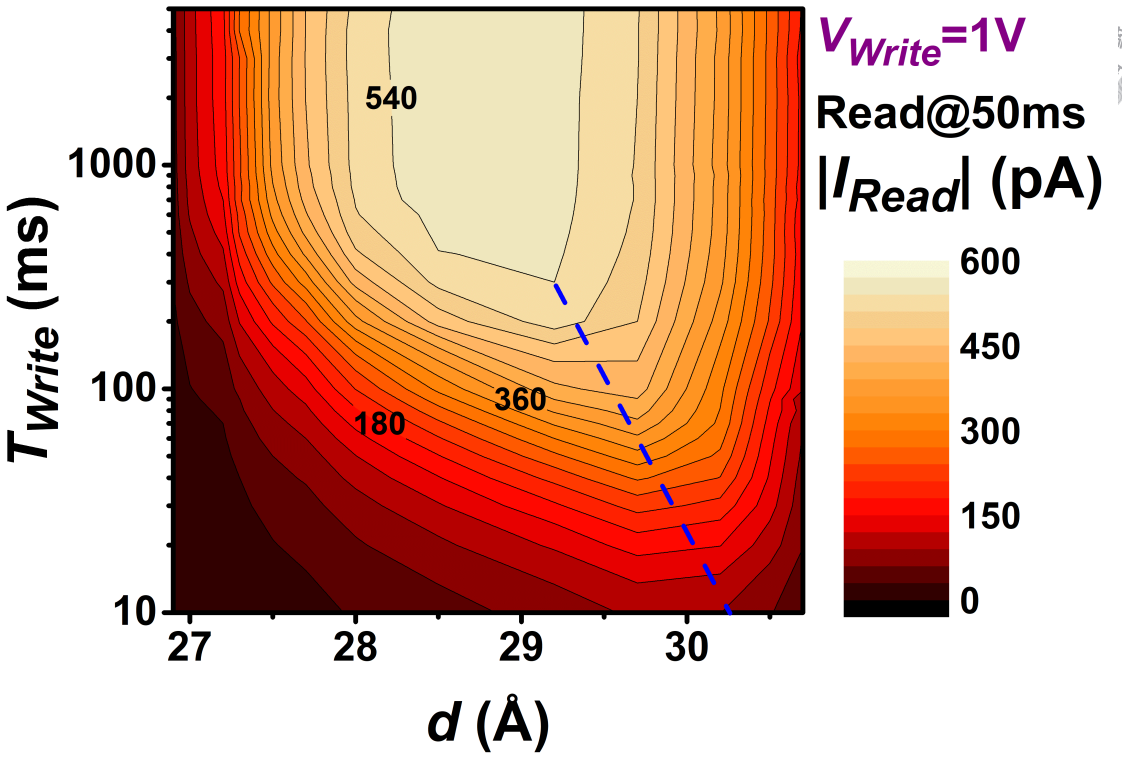

Figure 2–18. Contour map of $|I_{Read}|$ versus d (x-axis) and T_{Write} (y-axis) when V_{Write} = 1 V. The blue dashed line indicates the optimal oxide thickness under a certain write time.

this contour map, we can observe that if the magnitude of the read current is the primary concern, we may opt for V_{Write} = 0.7 V and T_{Write} = 600 ms for power-conserving considerations, as further increases in these two parameters do not significantly enhance $|I_{Read}|$. Alternatively, if the goal is to operate at the highest frequency, we might choose V_{Write} = 0.5 V and T_{Write} = 10 ms.

2.6 More About The Simulation

We have examined the fundamental transient current behavior of the Planar MISTD under different write programs and discussed the optimization of parameters for dynamic

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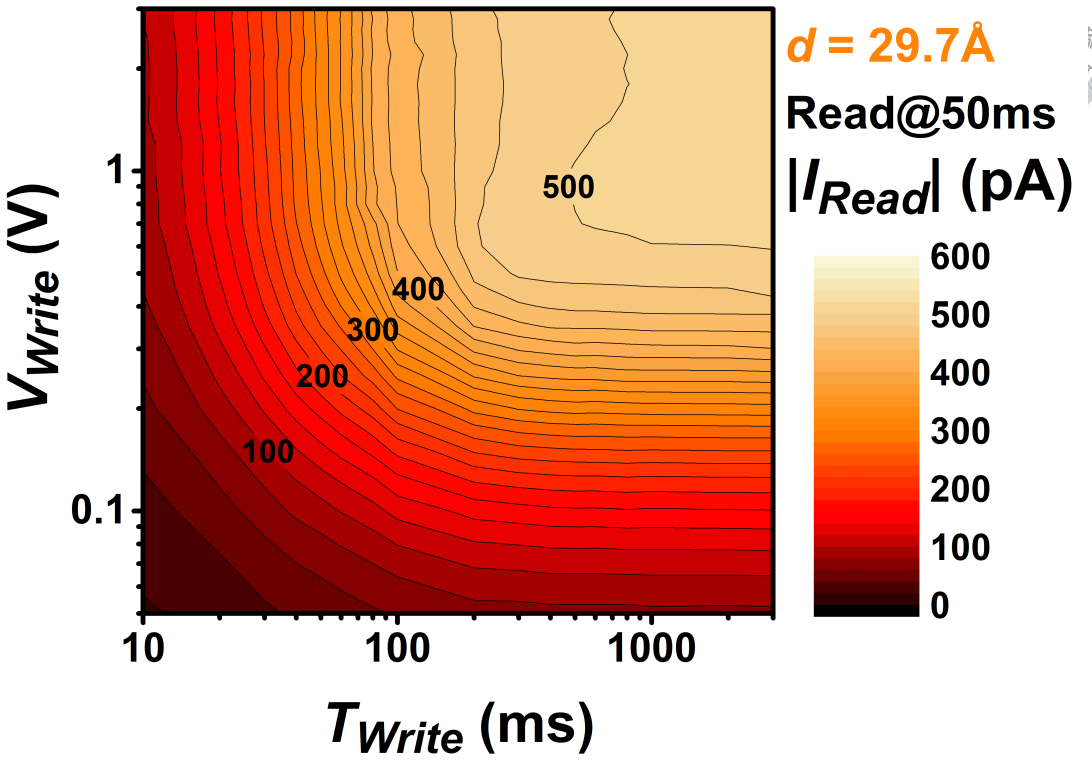

Figure 2–19. Contour map of $|I_{Read}|$ versus T_{Write} (x-axis) and V_{Write} (y-axis) for the device with d = 29.7 Å.

memory applications. In **Section 2.3**, we effectively reproduced the $I_{Read} - V_{Write}$ characteristics. Nevertheless, discrepancies persist between the simulation and experimental results, prompting a closer examination of the assumptions made during the TCAD simulation and the proposed mechanism. This section delves into more intricate details of the TCAD simulation, aiming to address the aforementioned issues.

We have omitted the consideration of Auger recombination in the simulation due to its significantly slower rate compared to the SRH recombination process. In **Figure 2–20**, the results depict the magnitude of the transient current $|I_{Read}|$ plotted against the transient time t, with and without the inclusion of the Auger recombination model in the simulation

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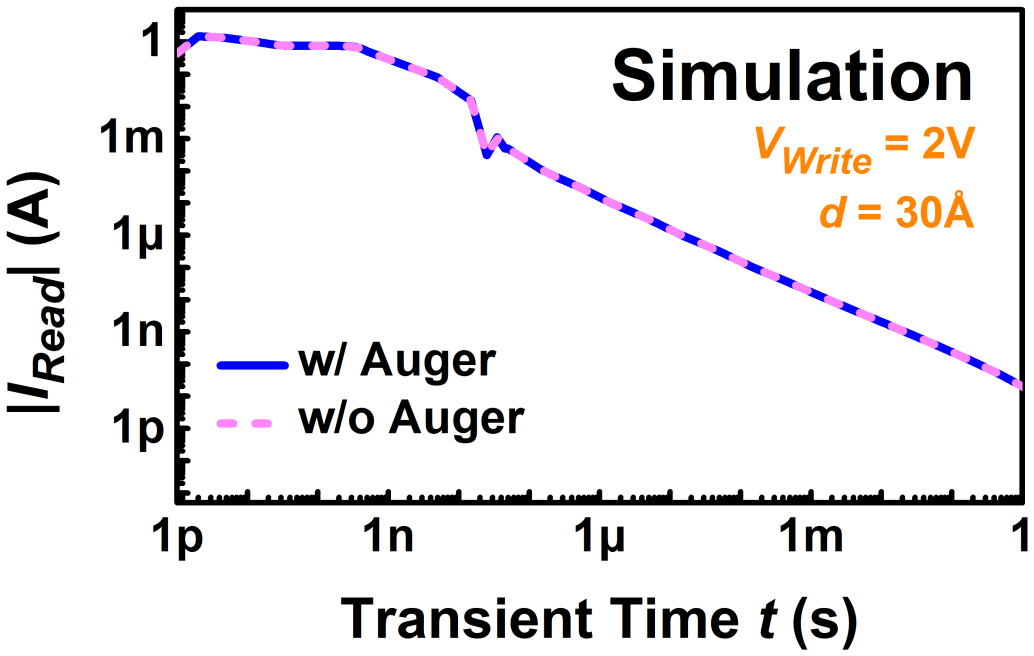

Figure 2–20. Comparison of transient current characteristics of the device with $d = 30$ Å under $V_{Write} = 2$ V, with or without the Auger recombination model included in the simulation.

for the device with $d = 30$ Å and $V_{Write} = 2$ V. The choice of 2 V for the write voltage aims to enhance the initial storage of electrons in the silicon, making Auger recombination more pronounced given its faster recombination rate for larger carriers' densities. However, even under these conditions, I_{Read} remains identical to the scenario without considering Auger recombination.

Furthermore, based on calculations using the models and equations employed in Silvaco TCAD [112], the ratio of Auger recombination to SRH recombination is expected to be larger than 1 % only when both electron and hole densities surpass 10^{18} cm^{-3} simultaneously. Such a scenario is unlikely to occur during the transient. Therefore, we find it reasonable to neglect Auger recombination in the simulation and the proposed mechanism in this dissertation for the sake of simplicity.

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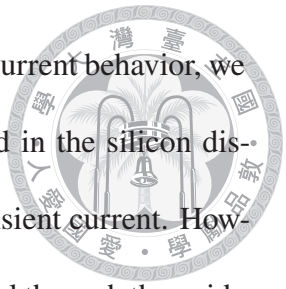

In the preceding discussion in this chapter regarding the transient current behavior, we have operated under the assumption that the inversion charges stored in the silicon discharge solely through the silicon substrate, resulting in a negative transient current. However, it is important to note that excess inversion charges may also tunnel through the oxide to the gate, leading to a positive transient current. The former is characterized as the displacement current term I_d, while the latter is the tunneling current term I_t, and the total gate current is expressed as:

$$I_g = I_d + I_t \tag{2.16}$$

In **Section 1.3**, we indicated that during the transient of the Planar device, I_t is significantly lower than I_d, and our focus is primarily on the displacement current. To substantiate this assertion, we examine the results of the TCAD simulation. As illustrated in **Figure 2−21** , the figure displays the different components of the transient current at the gate for the device with $d = 30$ Å under $V_{Write} = 1$ V. Notably, I_d totally determines I_g and is at least four orders of magnitude larger than I_t. Hence, we assert that the discharge of excess inversion electrons through tunneling within the device through the thin oxide, is minor compared to the discharge through the external circuit via displacement. Consequently, we have omitted consideration of the tunneling current during the transient in this chapter and the subsequent one.

It has come to our attention that there are deviations in the simulation results presented in **Section 2.3** when compared to the experimental results. One notable discrepancy is the mismatch in the magnitude of the transient read current, particularly under negative write programs. In this discussion, we aim to illustrate that the choice of carriers' lifetime in

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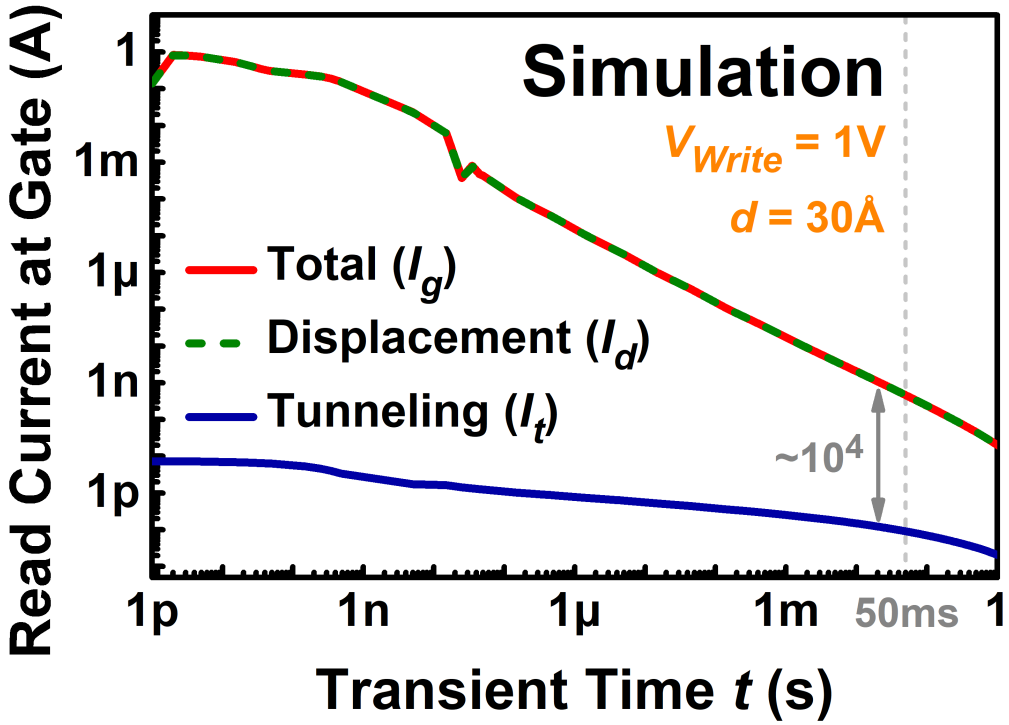

Figure 2–21. Simulation results of total current, displacement current, and tunneling current at gate during the transient for the device with d = 30 Å under V_{Write} = 1 V.

the simulation significantly influences the magnitude of I_{Read}. As mentioned earlier, we initially set $\tau_n = \tau_p = \tau = 10^{-7}$ s = 100 ns as the default in the simulation. However, this value is adjustable. **Figure 2–22** depicts the results of $|I_{Read}|$ for various τ values, considering the device with d = 30 Å under V_{Write} = ± 1 V, with the experimental results represented by the dashed lines. Noted again that I_{Read} represents the gate transient current at 50 ms. Notably, $|I_{Read}|$ generally follows a $1/\tau$ relation under V_{Write} = -1 V, while there is no clear trend for V_{Write} = +1 V. The rationale behind this observation is as follows.

After the negative write program, there is an electron deficiency in the silicon. During the transient, electrons need to be generated from the depletion region to replenish the deficiency. Consequently, the transient current is determined by the generation current,

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which can be expressed as [89, 96]:

$$J_{gen} \approx \frac{qn_iW}{2\tau}\left(1 - e^{\Delta\phi_n/\phi_t}\right) \tag{2.17}$$

Here, J_{gen} represents the generation current density, W is the depletion width, $\Delta\phi_n$ is the quasi-Fermi level splitting defined as the difference between the electron and hole quasi-Fermi level energies ($\Delta\phi_n \equiv \left(E_{Fn} - E_{Fp}\right)/q$), and $\phi_t = kT/q$ is the thermal voltage. Consequently, I_{Read} under negative write programs follows a $1/\tau$ relationship.

Under positive write programs, I_{Read} comprises recombination and diffusion current components [89, 117]. The recombination current component is τ-dependent, while the diffusion current component is τ-independent. Consequently, there is no monotonic trend for the $I_{Read} - \tau$ relation. For lower τ, the recombination current increases roughly in proportion to $1/\tau$. However, stronger recombination causes faster discharge of excess inversion charges, leading to a decrease in the electron quasi-Fermi level. Consequently, at a specific time point, such as 50 ms, $\Delta\phi_n$ becomes lower, and the diffusion current, which exponentially depends on $\Delta\phi_n/\phi_t$, also decreases. Therefore, predicting the overall effect on the total current I_{Read} is challenging.

Fortunately, the variation of I_{Read} with τ under positive write programs is not as significant compared to that under negative write programs. The magnitude of the former remains in the same order for τ ranging from 5 to 1000 ns, with a peak-to-valley ratio of less than 2. In contrast, the latter may exhibit differences of two orders of magnitude in the same range of τ.

One might question why we did not calibrate the value of τ using I_{Read} under negative write programs first and then used this τ for the simulation. The reason is that there are

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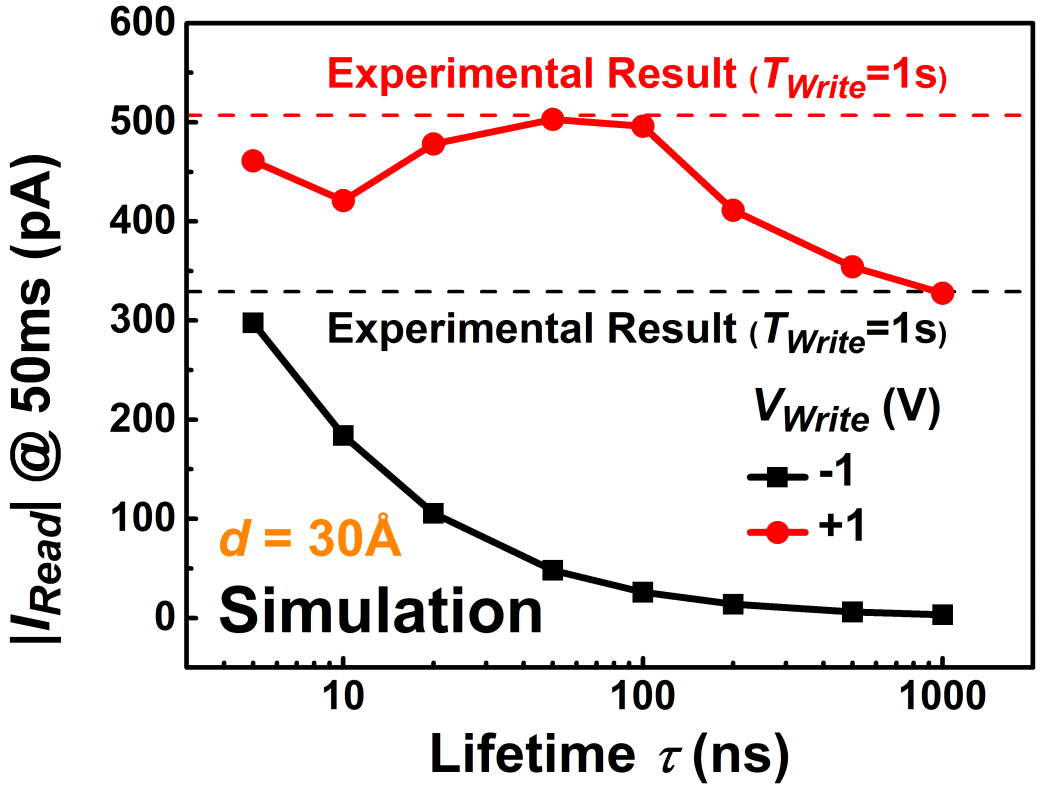

Figure 2–22. Simulation results of $I_{Read} - \tau$ characteristics for the device with $d = 30$ Å under $V_{Write} = \pm 1$ V. The dashed lines show the experimental result as a comparison.

other factors that significantly impact I_{Read} under negative write programs. For instance, we neglected interface traps in the simulation, which are unavoidable in experimental devices. Additionally, the consideration of oxide charges Q_{ox} has been omitted so far. As we will explore in **Section 2.7**, both positive and negative write programs have a strong dependence on Q_{ox}, and by incorporating Q_{ox} into the simulation, we can address many discrepancies outlined in **Section 2.3**. Consequently, we believe that selecting $\tau = 100$ ns in the simulation is adequate to reproduce the transient currents under positive write programs and reveal the mechanism behind the unusual 'Saturation Phenomenon.'

Nevertheless, fine-tuning the value of τ allows us to bring the simulation results closer to the experimental ones, especially under negative write programs. The following exam-

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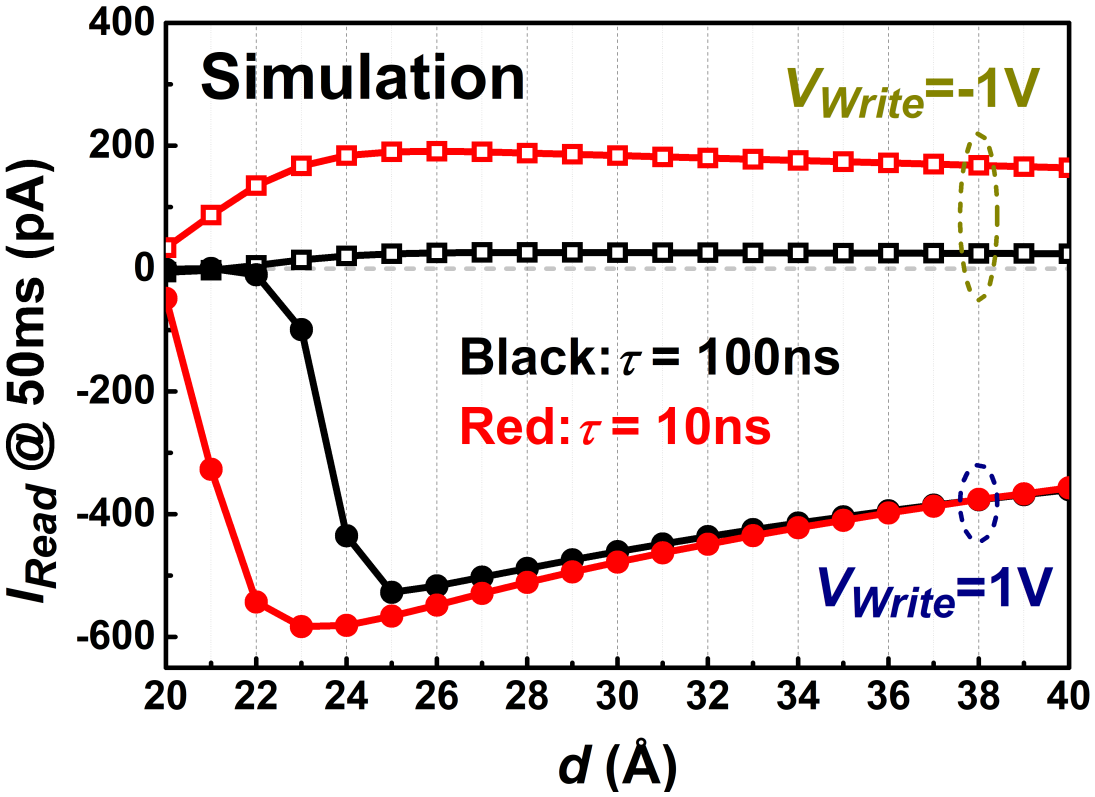

Figure 2–23. Simulation results of $I_{Read} - d$ characteristics under $V_{Write} = \pm$ 1 V with τ = 10 and 100 ns.

ples illustrate the adjustment of τ for the calibration of the TCAD simulation. **Figure 2–23** presents the $I_{Read} - d$ characteristics under $V_{Write} = \pm$ 1 V, with τ = 10 and 100 ns. For V_{Write} = -1 V, the magnitude of I_{Read} is significantly larger for τ = 10 ns, approaching the experimental results more closely than with τ = 100 ns. For V_{Write} = +1 V, the magnitude of I_{Read} changes only slightly. However, the peak position of the $I_{Read} - d$ relation shifts to a lower d for a lower τ. This shift is due to a lower τ indicating a faster generation rate under a positive gate voltage during the write procedure. Consequently, it becomes possible for the device with a thinner oxide to overcome the large tunneling probability and store the inversion charges, resulting in a larger magnitude of I_{Read} compared to the device with a thicker oxide, as predicted by (2.9).

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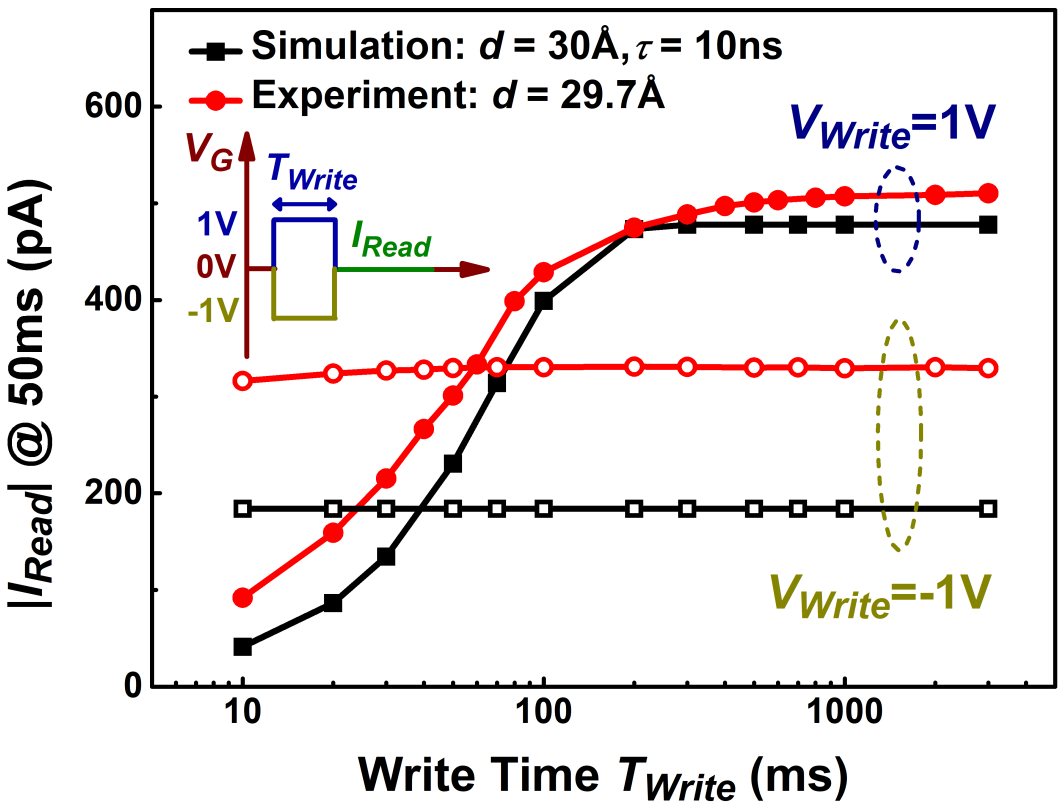

Figure 2–24. Comparison of the experimental and simulation $I_{Read} - T_{Write}$ characteristics under $V_{Write} = \pm 1$ V pulsed write programs. For the experimental device, $d = 29.7$ Å. For the simulation device, $d = 30$ Å and $\tau = 10$ ns.

Finally, we conducted the simulation with $\tau = 10$ ns to reproduce the $I_{Read} - T_{Write}$ characteristics under positive and negative write programs, and the results are illustrated in **Figure 2–24**. The experimental results are also shown for comparison. For the experimental device, the oxide thickness is 29.7 Å, while it is 30 Å for the simulation device. As seen, the simulation results of the $I_{Read} - T_{Write}$ relation under positive write programs closely resemble the experimental results, not only in the magnitude of I_{Read} but also in the saturation after $T_{Write} \geq 1$ s. Despite the mismatch in the magnitude of the I_{Read}, which can be further improved by fine-tuning the value of τ, the simulation $I_{Read} - T_{Write}$ behavior is also close to the experimental one under negative write programs. These re-

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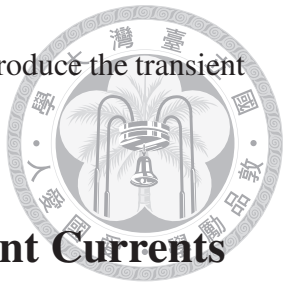
sults indicate that it is possible to utilize TCAD simulation to fully reproduce the transient behavior of the MISTD by tuning the parameters.



2.7 Impact of Oxide Charges on The Transient Currents

In this section, we present simulation results of I_{Read} considering the presence of oxide charges. There will be inevitably effective positive oxide charges within the SiO_2 layer with a number density between 10^{10} and 10^{12} cm^{-2}, originating from oxygen vacancies resulting from bonding imperfections and positive ions such as H^+ and Na^+ [39, 120]. These positive oxide charges will induce a depletion region and possibly an inversion layer outside the gate area for the p-type silicon substrate used in this work. The excess inversion electrons stored under the gate during the transient will interact laterally with the carriers outside, influencing the transient behavior.

The simulation results in **Figure 2–25** illustrate the $|I_{Read}| - V_{Write}$ characteristics with oxide charges presented, addressing deviations observed between the simulation and experimental results. Noted again that I_{Read} represents the gate transient current at 50 ms. The device has a 30 Å oxide layer, and the lifetime is set to 100 ns. Oxide charge densities (Q_{ox}/q) are set as 0, 3, and 4×10^{11} cm^{-2}. With the inclusion of oxide charges, $|I_{Read}|$ decreases for a positive V_{Write} and increases for a negative V_{Write}. Additionally, $|I_{Read}|$ shows a decreasing trend as V_{Write} continues to increase after saturation, which can also be observed in the experimental results **Figure 2–2**, but not in the simulation results without the oxide charges. Furthermore, the presence of oxide charges raises $V_{Write,sat}$, the write voltage where I_{Read} starts to saturate, under positive write programs. This finding can explain the slight variations in $V_{Write,sat}$ for devices with different oxide thicknesses, as the ultra-thin oxide layers grown by anodic oxidation followed by rapid thermal annealing,

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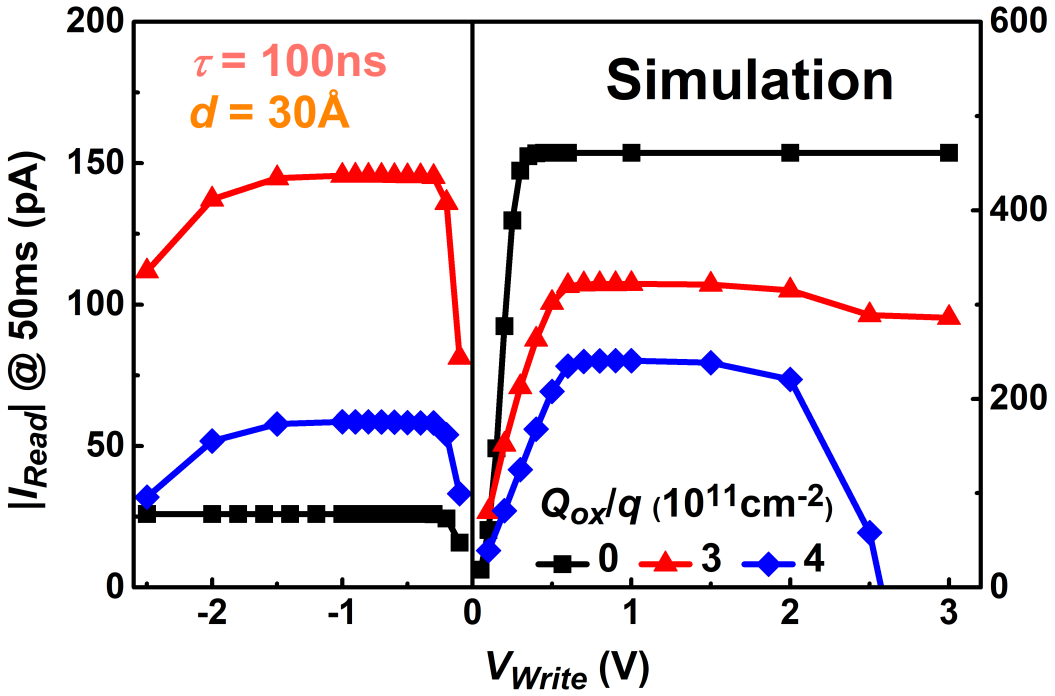

Figure 2–25. Simulation results of $I_{Read} - V_{Write}$ characteristics with oxide charges presented. Q_{ox}: The area density of positive oxide charges. Q_{ox}/q: Number density of oxide charges.

identical to the fabrication process in this dissertation, exhibit increased oxide charges with the oxide thickness [107]. Besides, we can also observe that I_{Read} will decrease as $|V_{Write}|$ increases after the saturation under both positive and negative write programs, consistent with the experimental results.

The results in **Figure 2–2** emphasize that oxide charges impact the magnitude of I_{Read} under both positive and negative write programs, highlighting their importance in accurate simulation to reproduce experimental results. The intricate reasons behind the decrease in I_{Read} and the increase in $V_{Write,sat}$ under positive write programs due to the presence of oxide charges are omitted here and will be thoroughly discussed in the appendix for conciseness in the dissertation.

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2.8 Summary

In this chapter, we explored the transient currents of the Planar MISTD at millisecond timescales, specifically at 50 ms. We presented experimental results for the $I_{Read} - V_{Write}$, $I_{Read} - T_{Write}$, and $I_{Read} - d$ characteristics under positive write programs, with a comparison to results under negative write programs. Regarding the $I_{Read} - T_{Write}$ relation, we observed saturation in the magnitude of I_{Read} for $T_{Write} \geq 1$ s, indicating that the device approaches a steady state during this write time. The $I_{Read} - d$ relation exhibited a peak, suggesting an optimal oxide thickness to maximize transient current magnitude. When the oxide is thick, the oxide capacitance decreases, limiting its ability to store inversion charges. Conversely, when the oxide is too thin, it loses its capacity to store charges due to severe tunneling effects. This results in the optimum thickness falls within the range of 28-30 Å.

In the $I_{Read} - V_{Write}$ relation, we noted that under positive write programs, $|I_{Write}|$ saturates with increasing V_{Write}, a phenomenon not previously observed in the literature. Interestingly, the saturation voltage $V_{Write,sat}$ is almost consistent across devices with different oxide thicknesses. This 'Saturation Phenomenon' challenges the assumption that the magnitude of I_{Read} is solely proportional to excess inversion charges at the start of the transient.

To unravel the underlying mechanism, we conducted TCAD simulations. Despite minor discrepancies, the simulation results aligned with the experimental findings. Notably, the 'Saturation Phenomenon' persisted in the simulations. Based on the simulation results in the sub-millisecond regime, we proposed a mechanism to understand the phenomenon. When V_{Write} exceeds $V_{Write,sat}$, the silicon band bending diminishes according to the volt-

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age balance across the MIS system, resulting in a rapid influx of holes to recombine with excess inversion electrons. This process raises silicon band bending, meeting the time-dependent minimum band bending requirement $\psi_{s,min}(t)$ for transient times $t \geq 100$ ns, leading to the saturation of the read current at 50 ms. The proposed mechanism accurately predicted $V_{Write,sat}$, and the transient currents behaved as anticipated when varying the read voltage and the work function of the metal gate.

We introduced a methodology employing contour maps to optimize parameters for operating the MISTD as a dynamic memory cell, utilizing negative and zero I_{Read} after positive and zero voltage write programs, respectively. Different optimal parameters for oxide thickness, write voltage, and write time were derived based on various considerations. For instance, to maximize the transient current window with minimal power consumption, we recommended using $V_{Write} = 0.5$ V and $T_{Write} = 1$ s for a device with $d = 29.2$ Å.

At the end of this chapter, we presented additional simulation results, supporting the validity of our assumption in neglecting the influence of Auger recombination and tunneling current in the discussion of transient current behavior. We also highlighted the impact of the selected value of carriers' lifetime in the simulation and the presence of oxide charges on transient current behavior, indicating that fine-tuning these parameters would be able to eliminate many discrepancies between the presented simulation and experimental results.

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3

Simulation and Modeling of Transient Currents of Planar MISTD in The Sub-Millisecond Regime

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3.1 Introduction

In the preceding chapter, we investigated the transient currents of the gate at 50 ms. Analyzing the experimental data, we gained insights into the influence of write voltage, write time, and oxide thickness on read currents, with consistent alignment observed in TCAD simulation results. It was also noted that the read current at 50 ms tends to saturate with an increase in positive write voltage. The selection of the 50 ms time point for our study was motivated by two factors. Firstly, this value closely approximates the refresh time of the dynamic memory cell, highlighting its potential suitability for such applications. Secondly, owing to constraints imposed by our measuring instrument, a time point of several tens of milliseconds represents the fastest achievable data acquisition time for us.

To gain a comprehensive understanding of the read current at 50 ms and the peculiar 'Saturation Phenomenon' observed in **Chapter 2**, we find it imperative to delve into the transient behavior of the device within the sub-millisecond regime. Due to the unavailability of experimental data in this regime, our focus in this chapter shifts towards TCAD simulation and analytical modeling.

In **Section 3.2**, we examine the simulation results depicting the transient behavior of a Planar MISTD with a 30 Å oxide layer, switching from 1 V to 0 V. Detailed examination will be given to the temporal response of electron and hole currents in the substrate, electron and hole density distribution in the silicon, maximum recombination rate, and band diagrams covering a time span from 1 ps to 1 s. Our observations provide a comprehensive insight into carrier motions within the semiconductor, as well as the discharge mechanism of excess inversion electrons. Additionally, we note that the total gate transient current

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exhibits an inverse decay with time, at least within the transient time range of 100 ns to 1 ms, for a write voltage of 1 V.

Moving on to **Section 3.3**, we introduce an analytical model to elucidate this phenomenon. The modeling results demonstrate a good alignment with the simulation results for the transient gate current in the sub-millisecond regime. Moreover, our proposed model is capable of deriving the transient current 'Saturation Phenomenon' at the millisecond time scale, as observed in both experimental and simulation results, with the predicted saturation voltage deviating by only 0.01 V.

3.2 Simulation Results

3.2.1 Overview

In this section, we delve into the transient behavior of the Planar MISTD with a 30 Å oxide layer, transitioning from 1 V to 0 V, based on simulation results spanning from 1 ps to 1 s. **Figure 3–1** (a) illustrates the schematic device cross section. The silicon has a thickness of 5 μm, and the silicon oxide is 30 Å thick. In the following discussion in this chapter, we will examine some physics quantities along the depth in the silicon, with the origin set at the Si/SiO_2 interface and the silicon substrate at a depth of 5 μm. It is crucial to emphasize that, according to the definition used in this dissertation, the current density within the silicon at the depth of 5 μm has an opposite sign to the substrate current. In other words, a negative current within the silicon indicates that the current flows from the silicon substrate to the silicon surface. Consequently, the substrate current is considered positive. The definition of the direction of the current flow is visually illustrated in **Figure 3–1** (b).

It is crucial to reiterate the direction and the sign of the gate and substrate currents. Dur-

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ing the transition from 1 V to 0 V, positive charges stored at the gate discharge, specifically flowing out of the gate through the external circuit, leading to a **negative** gate transient current. On the other hand, the substrate current is considered positive when it flows from the substrate to the silicon surface. Consequently, the discharge of excess inversion charges from the silicon surface to the substrate results in a **positive** substrate current. It is evident that the gate and substrate currents have the same magnitude but opposite signs, given that the MISTD is a two-terminal device.

In **Chapter 2**, experimental results provide insights into gate and substrate currents only at the millisecond time-scale. However, TCAD simulation enables us to explore transient currents in the sub-millisecond regime. Additionally, crucial physical quantities within the silicon at various time points become visually accessible through the simulation, including carrier densities, current densities, and band diagrams. It should be noted that the quantum tunneling model was enabled in the simulation. However, the magnitude of the tunneling current is low compared to the displacement current as demonstrated in the previous chapter. Therefore, we will neglect the tunneling current in the discussion in this chapter.

Figure 3–2 illustrates the temporal responses of several physical quantities over a transient time (t) range from 1 ps to 1 s. Subfigure (a) depicts the magnitude of substrate current densities, presenting the substrate total current density ($I_{Total,sub}$) along with substrate electron and hole current density components ($I_{e,sub}$ and $I_{h,sub}$, respectively) separately. Subfigure (b) showcases the maximum electron density (Max. n_e) inside the silicon, approximately 2 nm from the silicon interface, in linear scale. Subfigure (c) reveals the hole density at the silicon surface (surface n_h). Subfigure (d) illustrates the maximum recom-

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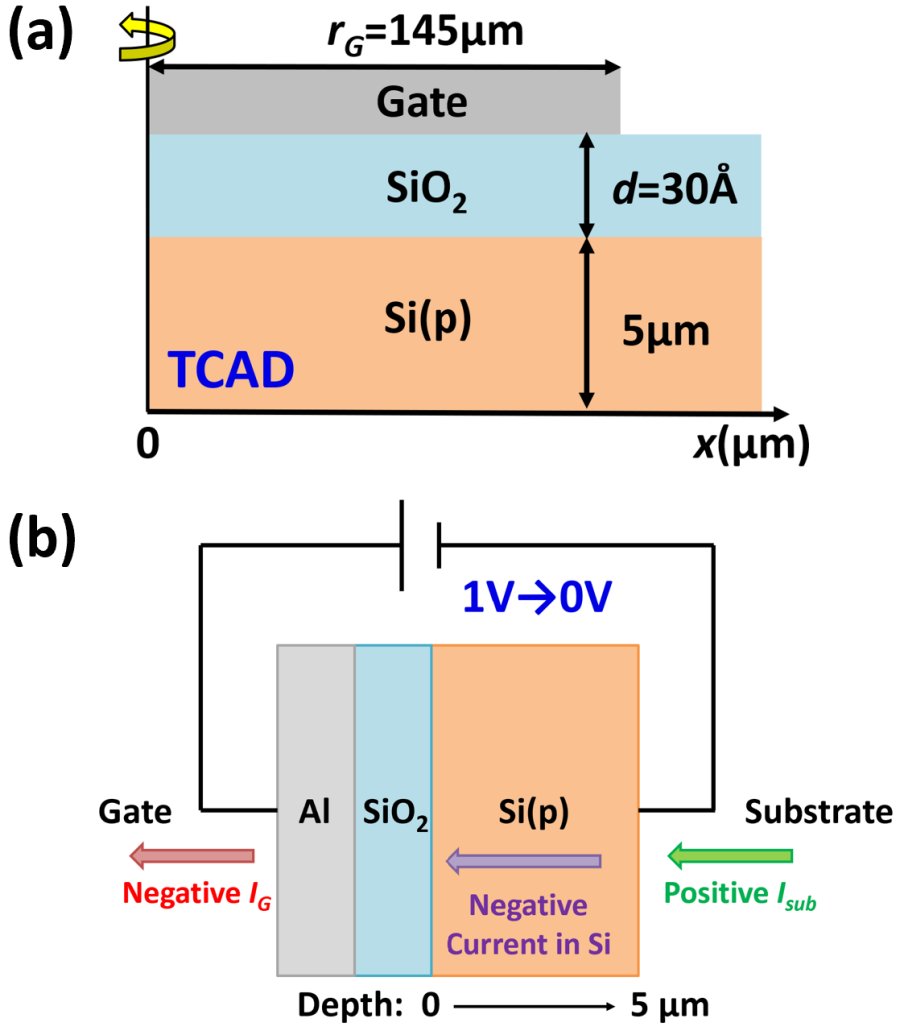

Figure 3–1. (a) Schematic cross section of the device studied in the TCAD simulation in this chapter. (b)Schematic illustrating the definition of the sign and direction of the current flow at the gate and substrate electrode, and inside the silicon.

bination rate inside the silicon (Max. Recom. Rate). Subfigure (e) exhibits the silicon surface band bending (ψ_s). Subfigure (f) displays the electron and hole quasi-Fermi levels (E_{Fn} and E_{Fp}, respectively), with the inset providing an enlarged view of E_{Fp} for t ranging from 1 ns to 100 ns. Subfigure (g) demonstrates the depletion region width W of the silicon. First of all, we highlight some observations about the substrate current density displaying in **Figure 3–2** (a):

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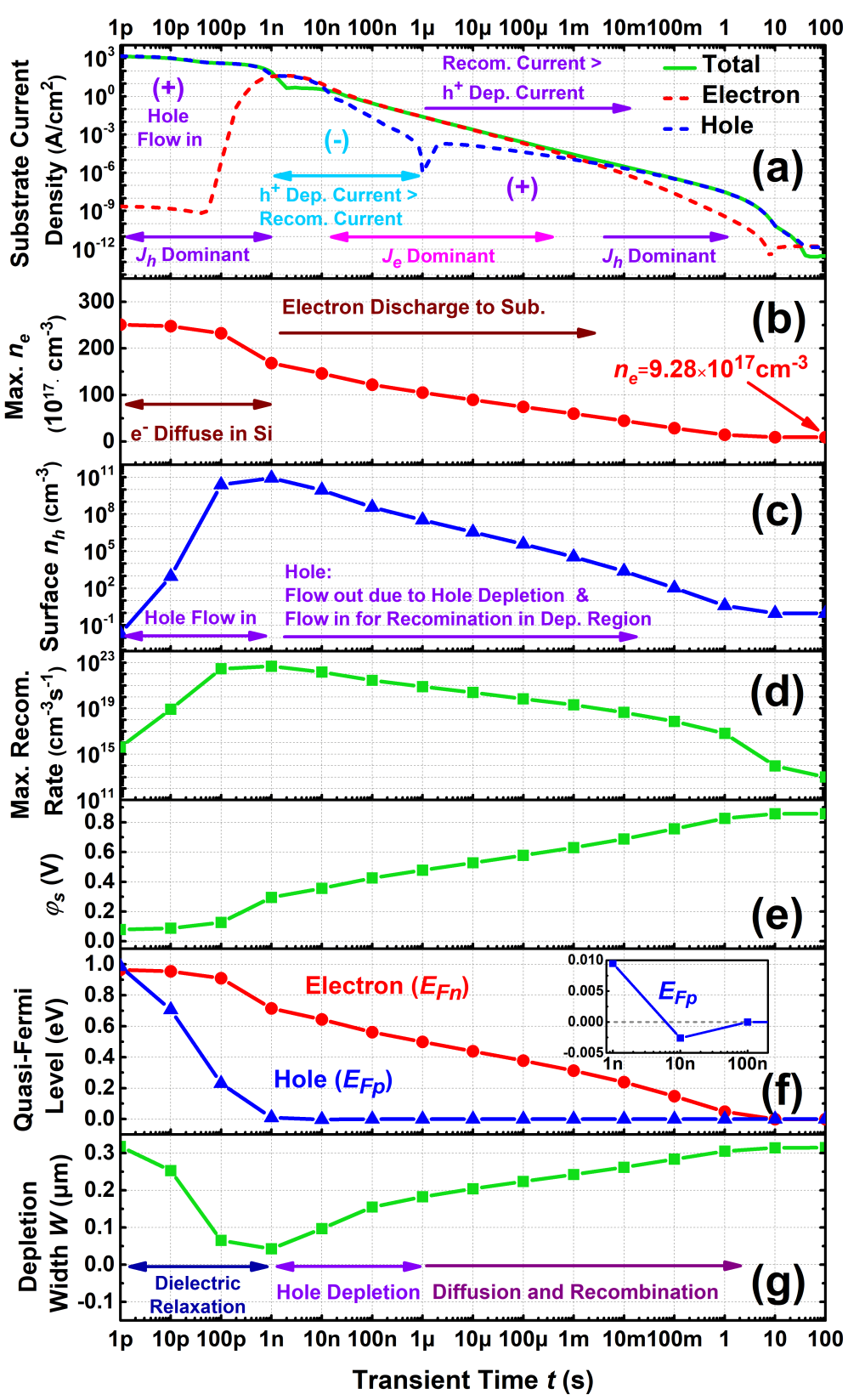

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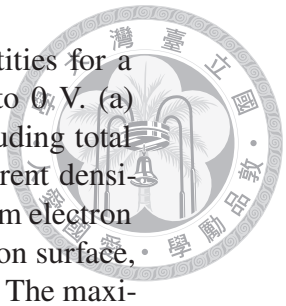

Figure 3–2. Temporal responses of several physical quantities for a MISTD with an oxide layer of 30 Å switching from 1 V to 0 V. (a) The magnitude of the current densities at the substrate, including total current density (green solid line), and electron and hole current densities (red and blue dashed lines, respectively).(b) The maximum electron density inside the silicon, which is about 2 nm from the silicon surface, in linear scale. (c) The hole density at the silicon surface. (d) The maximum recombination rate inside the silicon. (e) The silicon surface band bending. (f) Electron and hole quasi-Fermi levels. Inset: Enlargement of hole quasi-Fermi level for transient time within 1 ns to 100 ns. (g) The depletion width.

Substrate Total Current Density:

- The substrate total current density is consistently positive throughout the transient, with the magnitude generally decaying over time.

- Between 100 ns and 1 ms, the curve of substrate total current density against t appears close to a straight line in log-log scale, suggesting an inverse decay with time, i.e., $I_{Total,sub} \propto 1/t$.

- For t less than 1 ns, the substrate total current is primarily influenced by hole current. Between 10 ns and 1 ms, the substrate total current is dominated by electron current. Beyond 10 ms, the substrate total current is predominantly influenced by hole current. In other time periods, both electron and hole currents contribute to the substrate total current.

Substrate Hole Current Density:

- The magnitude of substrate hole current density generally decays with transient time t.

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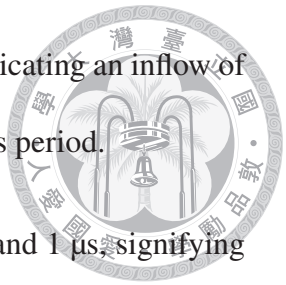

- Substrate hole current density is positive for t less than 1 ns, indicating an inflow of holes from the silicon substrate to the silicon surface during this period.
- Substrate hole current density becomes negative between 1 ns and 1 µs, signifying an outflow of holes from the silicon surface to the silicon substrate in this interval.
- Substrate hole current density turns positive again for t larger than 1 µs, indicating an inflow of holes from the silicon substrate to the silicon surface.

Substrate Electron Current Density:

- Substrate electron current density is consistently positive, representing an outflow of electrons from the silicon surface to the silicon substrate throughout the entire transient.
- For t less than 100 ps, the substrate electron current density is minimal. It experiences a rapid increase between 100 ps and 1 ns, followed by a decay with time thereafter.

The behavior of the substrate hole current is considerably intricate. Conversely, the behavior of the substrate electron current is more straightforward. Throughout the entire transient, the substrate electron current density remains positive, signifying the discharge of electrons from the silicon surface to the substrate. This aligns with the decreasing trend observed in the maximum electron density as depicted in **Figure 3–2** .

However, it is noteworthy that, although the magnitude of the substrate electron current density decays with time after 1 ns, following the discharge pattern, the substrate electron density is minimal in the first 100 ps. The reason behind this lies in the fact that excess inversion electrons are initially stored at the silicon surface at the beginning of transient,

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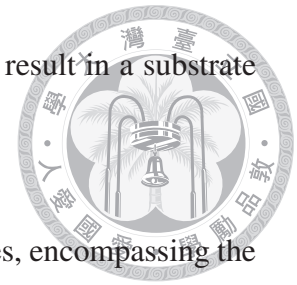
and it takes some time for these electrons to flow to the substrate to result in a substrate electron current.



For a deeper understanding, **Figure 3–3** presents current densities, encompassing the total current density as well as the electron and hole components, within the silicon at various time points ranging from 1 ps to 100 ms. The horizontal axis represents the depth in the silicon, with the origin set at the silicon surface. It is emphasized again that, the current density at the depth of 5 μm has an opposite sign to the substrate current. A negative current indicates that the current flows from the silicon substrate to the silicon surface, so the substrate current is considered positive according to **Figure 3–1** (b).

From **Figure 3–3** , we can deduce that, although there is electron current flowing from the silicon surface to the substrate for t within 1 ps and 100 ps, it diminishes to almost zero within the silicon. Consequently, the substrate current is minimal. Two primary reasons contribute to this observation. Firstly, as the substrate is p-type doped, excess inversion electrons undergo strong recombination when flowing within the silicon. Secondly, given that electron transport is diffusion-dominated, the magnitude of the electron current density is proportional to the electron density. It takes approximately 1 ns for electrons to diffuse to the substrate, thus increasing the electron density there. Consequently, the substrate electron current density is minimal until that point. The carrier densities, along with the recombination rate inside the silicon at different time points, are illustrated in **Figure 3–4** . It is evident that the electron density is still lower than 10^{10} cm^{-3} when t = 100 ps but exceeds 10^{13} cm^{-3} at t = 1 ns, indicating that electrons take about 1 ns to flow from the silicon surface to the substrate. Therefore, the substrate electron density is minimal in the first 1 ns.

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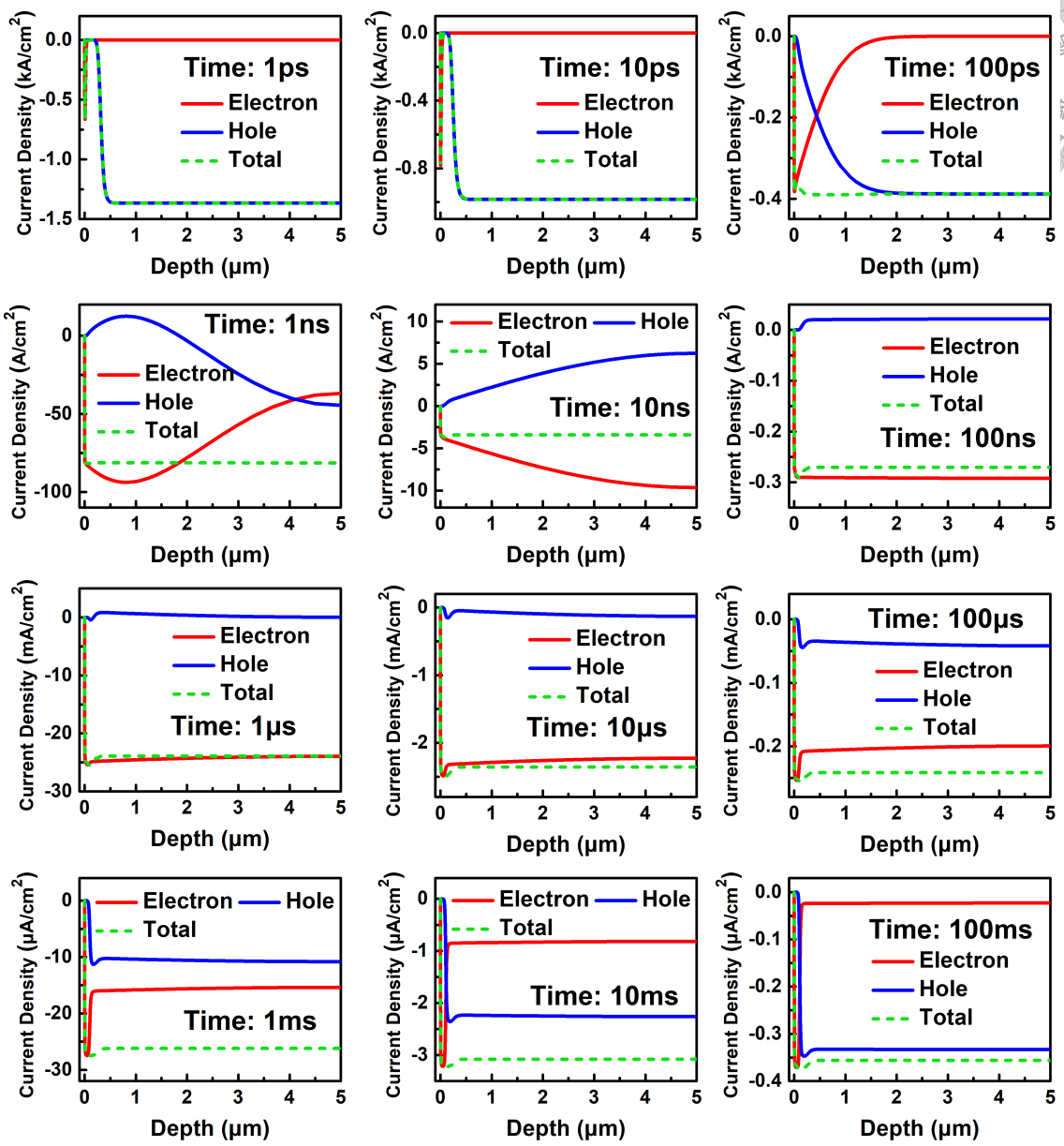

Figure 3–3. Current densities inside the silicon, including the total current densities and the electron and hole current components, at different time points ranging from 1 ps to 100 ms during the transient for the device switching from 1 V to 0 V. The horizontal axis represents the depth in the silicon from the surface. The silicon substrate is at the depth of 5 μm. The current density here is defined positive when it flows from the silicon surface to the silicon substrate. Therefore, a negative current density at the depth of 5 μm indicates the current flows from the substrate to the surface, which represents a positive substrate current.

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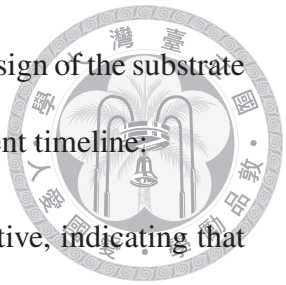

However, the behavior of holes is relatively intricate. Based on the sign of the substrate hole current density, we have defined three time periods on the transient timeline:

- Dielectric Relaxation (t < 1 ns): Substrate hole current is positive, indicating that holes flow in to the silicon surface.
- Hole Depletion (1 ns < t < 1 μs): Substrate hole current is negative, indicating that holes flow out to the silicon substrate.
- Diffusion and Recombination (t > 1 μs): Substrate hole current is positive, indicating that holes flow in to the silicon surface.

In the upcoming subsection, we will provide a detailed discussion on the distinct motions of holes within these three periods.

3.2.2 Hole Motions: Dielectric Relaxation, Hole Depletion, and Diffusion and Recombination

Dielectric Relaxation

For transient time t less than 1 ns, the device is in the 'Dielectric Relaxation' period. In this period, the substrate hole current is positive, indicating the influx of holes from the silicon substrate to the surface.

The voltage balance equation for an MIS device is expressed as:

$$V_G - V_{Fb} = -\frac{Q_s}{C_{ox}} + \psi_s \tag{3.1}$$

Consider the scenario where the device switches from 1 V to 0 V. At the onset of the transient, when neither carriers have had time to respond to the voltage change, Q_s will be close to its value at the 0 V steady-state. Since the left-hand side of the equation decreases

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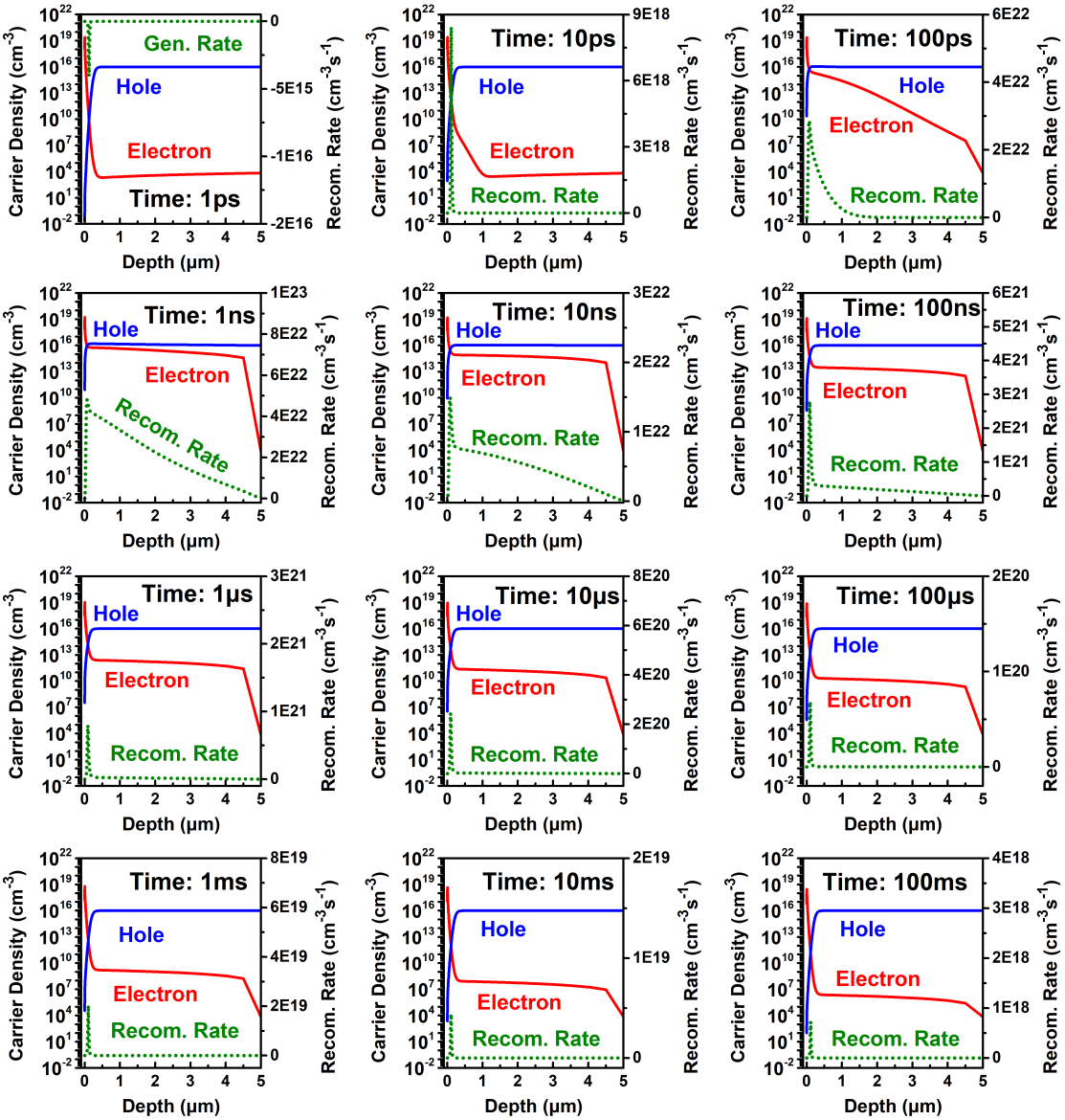

Figure 3–4. Electron and hole densities inside the silicon, with the generation rate also presented, at different time points ranging from 1 ps to 100 ms during the transient for the device switching from 1 V to 0 V. The horizontal axis represents the depth in the silicon from the surface. The silicon substrate is at the depth of 5 µm.

by 1 V before and after the switching, ψ_s must also decrease by 1 V immediately to maintain equation balance. Consequently, ψ_s will be very low at the beginning of the transient, as illustrated in **Figure 3–2** (e). The low value of ψ_s indicates that there should be more holes at the silicon surface compared to the moment before the transient. Hence, holes

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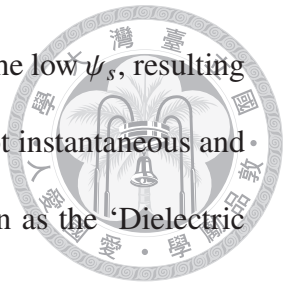

tend to flow in from the silicon substrate to the surface to respond to the low ψ_s, resulting in a positive substrate hole current. However, this influx of holes is not instantaneous and takes approximately 1 ns, and the this transient time period is known as the 'Dielectric Relaxation'.

In most cases familiar to us in semiconductor devices, we assume that the majority carrier's quasi-Fermi level, which is the hole quasi-Fermi level (E_{Fp}) in this context, is flat throughout the semiconductor. However, this assumption does not hold true during the transient, especially within the first 1 ns. This is because the motion of holes cannot keep pace with the rapid change of ψ_s. Consequently, the uneven distribution of E_{Fp} in the silicon requires some time to return to a flat condition. To gain a better understanding of this phenomenon, the band diagrams at different transient times are depicted in **Figure 3–5**. It is evident that E_{Fp} is notably uneven for $t < 1$ ns, contrasting with the typically flat E_{Fp} observed for $t > 1$ ns. It is important to note that the zero energy in these band diagrams is defined at the Fermi level of the silicon substrate. Therefore, the fact that E_{Fp} exceeds 0 within the silicon and get farther from the valence band energy (E_v), particularly at the surface, indicates a deficit of holes compared to what would be expected if holes could instantaneously respond to the voltage change and thus maintain a flat E_{Fp}. The surface hole density, as depicted in **Figure 3–2** (c), is exceedingly low at the onset of the transient (1 ps), gradually increasing until 1 ns, which implies that the inflow of holes requires approximately 1 ns to reach its peak before following a decreasing trend thereafter. If holes could indeed keep pace with ψ_s, the surface hole density should exhibit a consistent decrease throughout the transient, mirroring the rise of ψ_s throughout the entire transient (**Figure 3–2** (e)). However, this contradicts the observed behavior of surface hole density.

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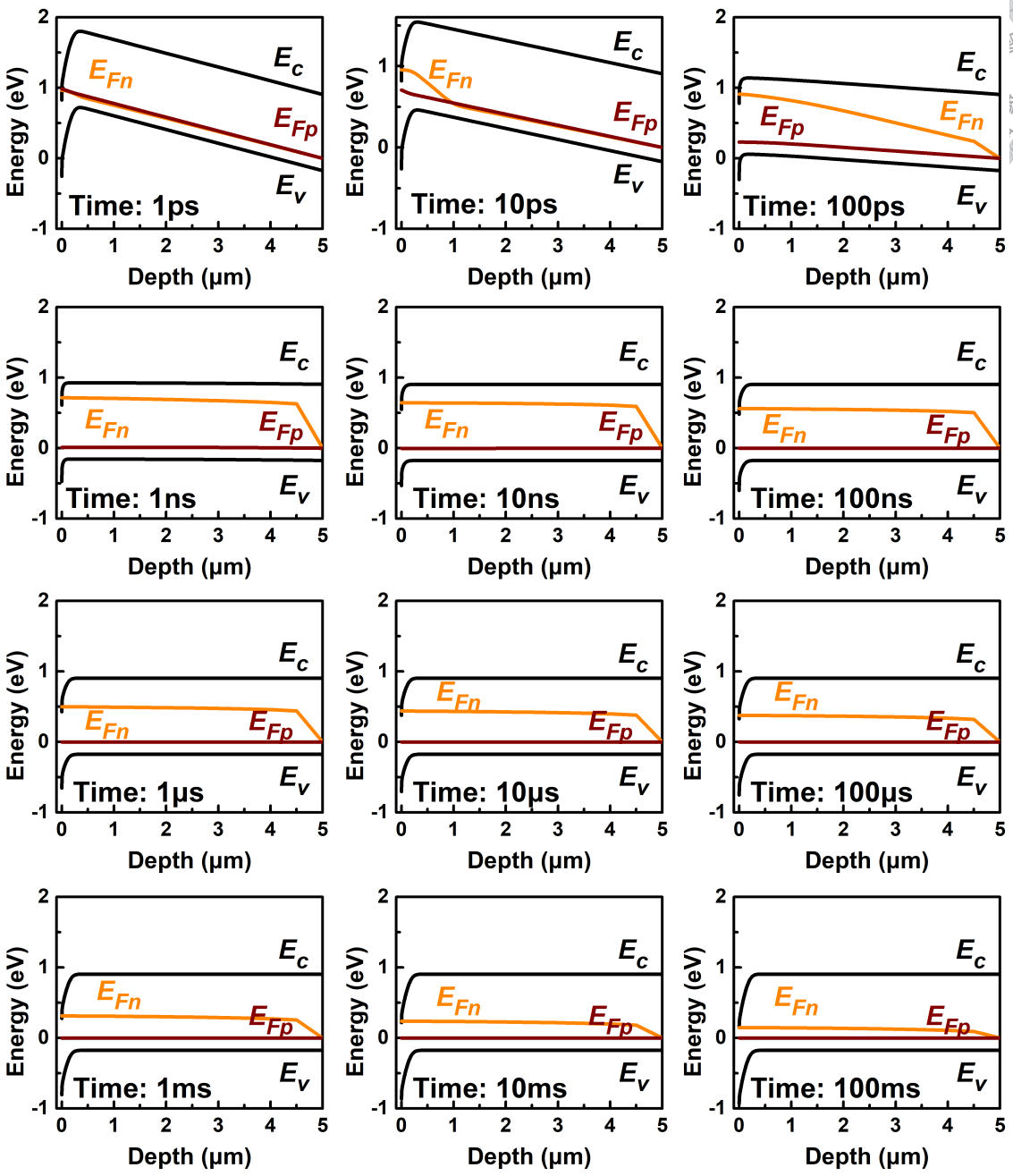

Figure 3–5. Band diagrams of the silicon, including conduction band and valence band energies (E_c and E_v, respectively), electron and hole quasi-Fermi level (E_{Fn} and E_{Fp}, respectively), at different time points ranging from 1 ps to 100 ms during the transient for the device switching from 1 V to 0 V. The horizontal axis represents the depth in the silicon from the surface. The silicon substrate is at the depth of 5 μm.

Therefore, we can conclude that holes are unable to immediately respond to changes in voltage, and approximately 1 ns is required to flatten the hole quasi-Fermi level. This time

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period is defined as the 'Dielectric Relaxation' period.

We have also observed that the band diagrams (**Figure 3–5**) for t = 1, 10, and 100 ps appear unusual: Each band diagram exhibits an uncommon local peak near the surface. The reason behind this anomaly is that, during this period, ψ_s remains very small, resulting in minimal overall downward band bending. At the same time, as holes have not yet migrated to the surface, the excess inversion electrons dominate and accumulate a large number of negative charges near the surface. This accumulation leads to a significant downward band bending near the silicon surface. To reconcile the fact that the overall downward band bending is not substantial, the energy bands will bend upward in the bulk silicon, for instance, from 1 to 5 μm in this context, resulting in bulge-shaped band diagrams. The upward band bending near the silicon substrate also indicates a strong flow of hole current from the substrate towards the surface. Given that electrons are still diffusing solely within the silicon and have not reached the substrate yet, the substrate total current is predominantly governed by the positive substrate hole current during the 'Dielectric Relaxation' period.

Additionally, it is important to note again that during this period, holes recombine with excess electrons over a broad spatial region inside the silicon. This phenomenon contributes to the saturation of the read current observed at millisecond time scales, as extensively discussed in **Chapter 2**.

In a short summary, during the 'Dielectric Relaxation' period for transient time less than 1 ns, holes will flow in from the substrate to follow up the rapid change of ψ_s, and the substrate current is dominated by the positive hole current.

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Hole Depletion

During the time period between 1 ns and 1 μs (1 ns < t < 1 μs), the device enters the 'Hole Depletion' period. In this phase, the substrate hole current is negative, signifying the net outflow of holes from the silicon surface to the substrate. We identify three primary mechanisms governing hole current conduction during this period, as elaborated in the following:

Hole Outflow: Overreaction of Hole

The first mechanism involves a negative substrate hole current caused by the overreaction of holes, occurring predominantly around $t \approx 10$ ns. As discussed previously, during the 'Dielectric Relaxation' period, a significant number of holes flow in rapidly in response to the low ψ_s. However, at the same time, ψ_s is time-dependent and increases with t, as illustrated in **Figure 3–2** (e). Consequently, the number of holes arriving at the surface may exceed what is required for the ψ_s at that time, leading to an 'Overreaction of Hole'. The temporal response of the hole quasi-Fermi level E_{Fp} in **Figure 3–2** (f) supports this observation. For t < 1 ns, E_{Fp} is positive, as discussed earlier, indicating a deficit of holes and an expected inflow of holes. However, around $t \approx 10$ ns, E_{Fp} becomes negative (closer to the valence band edge (E_v) compared to $E_{Fp} = 0$), suggesting an overabundance of holes at the silicon surface during this period. Consequently, holes at the surface flow out to the silicon substrate, resulting in a negative substrate hole current.

To gain a clearer understanding, we examine the spatial distributions of hole density in linear scale near the silicon surface at various transient time points in **Figure 3–6** . Once again, the origin of the horizontal axis is defined at the silicon surface. We observe peaks in the hole distributions at several time points, indicating an overabundance of holes at the

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surface, which tend to diffuse backward toward the silicon substrate. This phenomenon initiates at $t = 100$ ps. However, at this moment, the predominant behavior remains the influx of holes, aimed at smoothing out the elevated E_{Fp}. Moreover, this peak does not extend significantly into the bulk silicon, implying that the outflow of holes due to diffusion is easily overshadowed by the strong inflow of holes. Consequently, the substrate hole current remains positive (holes flow in from the substrate to the surface) at $t = 100$ ps. Afterwards, at $t = 1$ and 10 ns, the peak of the hole distribution becomes prominent and broad, extending deep into the bulk silicon. Besides, E_{Fp} now stabilizes and even becomes negative. Therefore, holes flow out from the silicon surface to the substrate, resulting in a negative substrate hole current.

In summary, the overreaction of holes results in a negative substrate hole current around $t \approx 10$ ns. This current component is unique to the $t \approx 10$ ns period and represents an additional term compared to the two components discussed subsequently, which occur throughout the $t > 1$ ns period. This distinction is apparent from the bulge observed in the substrate hole current near $t = 10$ ns in **Figure 3–2** (a).

Hole Outflow: Expansion of Depletion Region

The second mechanism involves another negative substrate hole current caused by the expansion of the depletion region for $t > 1$ ns. Following the 'Dielectric Relaxation' period, E_{Fp} stabilizes, indicating that holes can respond to the change in ψ_s after 1 ns. Consequently, as ψ_s increases with transient time, in accordance with (3.1) and the decrease in the number of inversion charges during the transient, the depletion width W in the silicon also increases over time. This can be observed in **Figure 3–2** (g) for $t > 1$ ns. It is noteworthy that the decreasing trend of W during the 'Dielectric Relaxation' period

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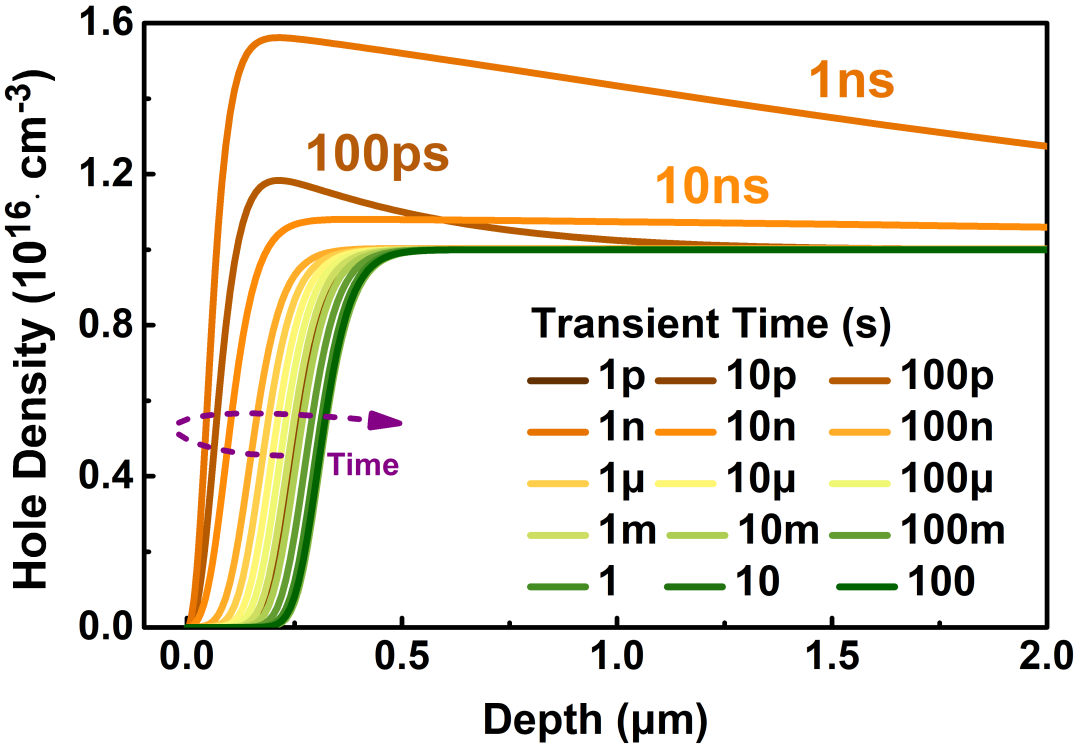

Figure 3–6. Spatial distributions of hole density near the silicon surface at several time points. The origin of the horizontal axis is defined at the silicon surface.

occurs because holes are still in the process of responding to the rapid change in ψ_s. After 1 ns, W progressively increases with time, as indicated by ψ_s. The expansion of the depletion region signifies a depletion of holes, which migrate from the edge of the depletion region to the silicon substrate, resulting in a negative substrate hole current.

Clear evidence is observed in **Figure 3–3** for $t = 100$ ns. The hole current density is positive, indicating that holes are flowing out toward the substrate, resulting a negative substrate hole current. However, this positive hole current density in the silicon does not originate at the silicon surface; rather, it begins at the edge of the depletion region. This implies that the outflow of holes results from the expansion of the depletion region.

It should be noted that as W continues to increase for $t > 1$ ns, this outflow of holes also

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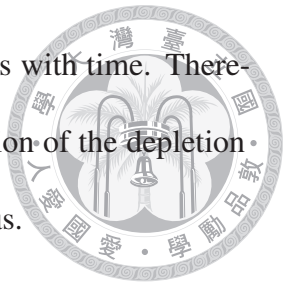

persists. However, the magnitude of this component rapidly decreases with time. Therefore, this negative hole current component, attributable to the expansion of the depletion region, only predominates for transient time ranging from 10 ns to 1 μs.

Hole Inflow: Recombination with Electrons

The third mechanism involves a positive substrate hole current caused by recombination with electrons for $t > 1$ ns. Excess inversion electrons will undergo recombination with holes in the depletion region, with the source of these holes being the silicon substrate. In other words, holes flow in from the substrate to recombine with electrons flowing out from the surface within the depletion region. Consequently, this results in a positive substrate hole current component. However, for the period between 1 ns and 1 μs, the two negative substrate hole current terms dominate, resulting in an overall negative substrate hole current.

In a short summary, during the 'Hole Depletion' period spanning from 1 ns to 1 μs, the depletion of holes flowing from the silicon to the substrate, resulting from the overreaction of holes and the expansion of the depletion region, outweighs the inflow of holes for recombination with electrons. Consequently, the substrate hole current is predominantly characterized as negative.

Diffusion and Recombination

Finally, for transient times greater than 1 μs ($t > 1$ μs), the device enters the 'Diffusion and Recombination' period. This period is named after the main electron motions. In this phase, the motion of holes is primarily dictated by their recombination with the excess inversion electrons within the depletion region. Consequently, holes flow in from the silicon substrate into the device, resulting in a positive substrate hole current.

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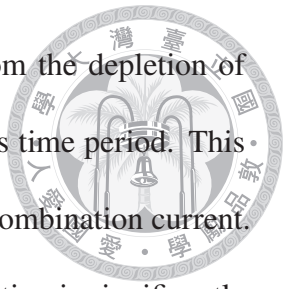

It is noteworthy that the outflowing hole current, originating from the depletion of holes near the edge of the depletion region, is also present during this time period. This hole current component exhibits the opposite direction to the hole recombination current. However, during this period, the current component due to hole depletion is significantly lower than that due to recombination. Thus, the substrate hole current is predominantly governed by the positive hole recombination current.

Furthermore, these two current components can be discerned by examining the current density within the silicon in **Figure 3–3** . For instance, consider the situation at $t = 100$ μs, falling within the 'Diffusion and Recombination' period. The hole current density at the substrate (at a depth of 5 μm) is negative, indicating that holes are flowing into the device from the substrate, resulting in a positive substrate hole current. The negative current density remains relatively constant throughout the bulk silicon, until there is a notable increase in magnitude around 0.3 μm, followed by a decrease near the silicon surface. This behavior of the hole current density can be explained as follows:

In the bulk silicon spanning from 0.3 μm to the substrate at 5 μm, there exist two opposing hole current flows. One comprises holes flowing in from the substrate for recombination, resulting in a negative hole current density within the silicon. The other involves the depletion of holes flowing out toward the substrate, yielding a positive hole current density within the silicon. As the magnitude of the former is greater than that of the latter, the overall hole current density in the bulk silicon is negative. Additionally, the component of hole depletion diminishes around 0.3 μm, as it originates from the edge of the depletion region, which is approximately at this depth. Consequently, the counteracting term to the negative hole recombination current within the silicon disappears, leading to an increase in

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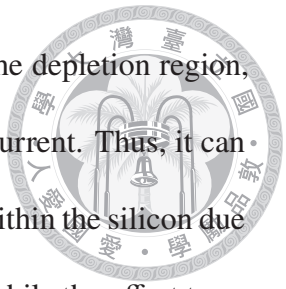

the magnitude of overall hole current density. Subsequently, within the depletion region, holes recombine with excess electrons, resulting in a vanishing hole current. Thus, it can be concluded that the magnitude of the negative hole current density within the silicon due to recombination is approximately equal to the peak value at 0.3 μm, while the offset term between this value and the substrate hole current represents the magnitude of the positive hole current density within the silicon due to hole depletion.

In summary, during the transient, hole motions are characterized as follows with the aid of **Figure 3–7**. In the 'Dielectric Relaxation' period (t < 1 ns), holes flow in in response to band bending, resulting in a positive substrate hole current (subfigure (a)). In the 'Hole Depletion' (1 ns < t < 1μs) and 'Diffusion and Recombination' (t > 1μs) periods, two major hole current components exist. The first arises from hole depletion due to depletion region expansion, leading to a negative substrate hole current (subfigure (b)). The second stems from influx of holes for recombination with excess electrons, leading to a positive substrate hole current (subfigure (c)). In the 'Hole Depletion' period, the first term dominates, resulting in a negative total substrate hole current. Conversely, in the 'Diffusion and Recombination' period, the second term dominates, leading to a positive total substrate hole current.

3.2.3 Discharge of Excess Inversion Electrons

In the preceding subsection, we delved into the intricate dynamics of hole motion. Regarding the motions of electrons, we have previously discussed how strong recombination spreading over the entire silicon within the first 100 ns leads to the saturation of transient current read at millisecond time scales, a phenomenon termed the 'Saturation Phenomenon' in **Chapter 2**. Additionally, we established in **Section 3.2.1** electron diffusion

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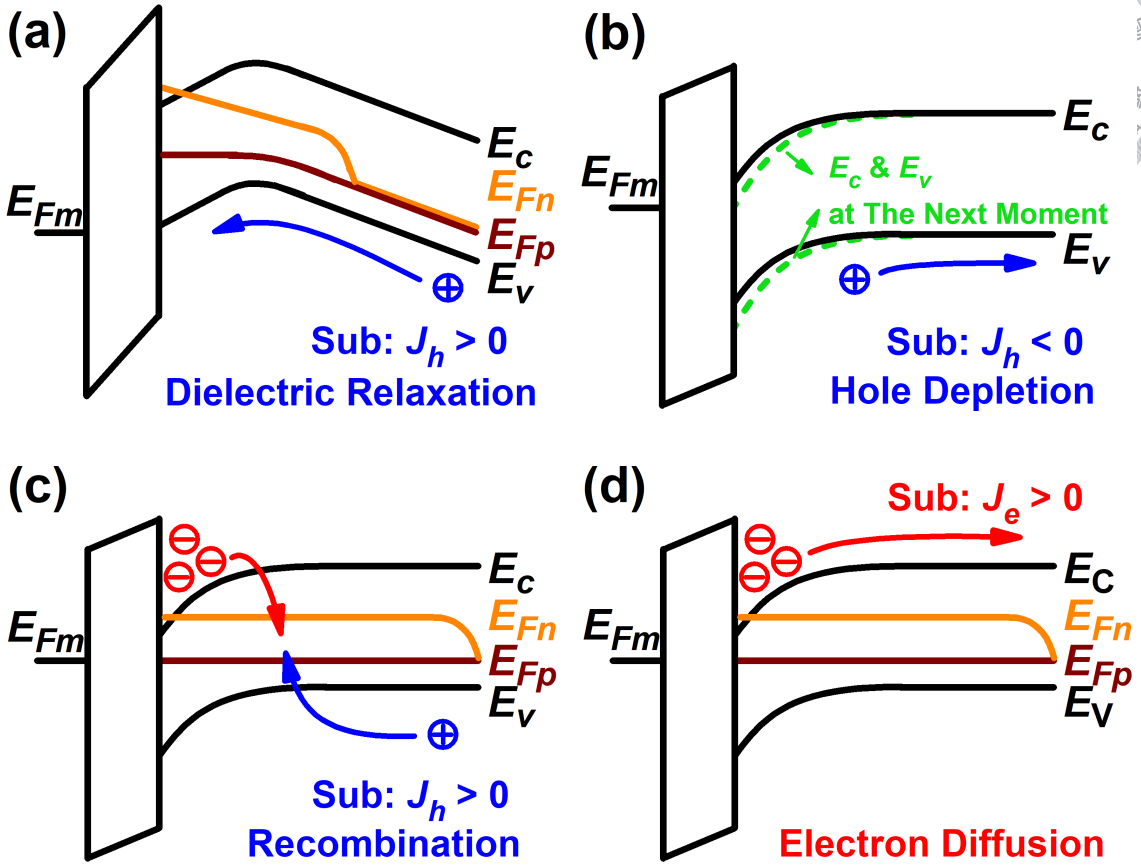

Figure 3–7. Schematics of several mechanisms of carriers' motions. (a) 'Dielectric Relaxation': Holes flow from the substrate towards the silicon surface. (b) 'Hole Depletion': Holes flow out from the edge of the depletion region to the substrate. (c) 'Recombination': Holes flow in from the substrate and recombine with the excess electrons flowing out from the silicon surface. (d): 'Electron Diffusion': Excess inversion electrons diffuse from the silicon surface to the silicon substrate.

reaches the substrate after about 1 ns. Now, we turn our attention to the discharge of excess inversion electrons afterwards in the 'Diffusion and Recombination' period. We identify three primary discharge mechanisms for transient time over 100 ns ($t > 100$ ns): *tunneling*, *diffusion*, and *recombination*. The detailed discussion about these mechanisms are as follows.

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Tunneling

The MISTD device under investigation in this chapter features an oxide layer with a thickness of 30 Å, making quantum tunneling through the oxide a factor that should be considered. This phenomenon affects the transient behavior of the device in three major ways. Firstly, during the write procedure, when the device is biased into the deep depletion regime, quantum tunneling may lead to fewer stored inversion charges compared to a scenario without the tunneling effect. This has been explored in detail in **Section 2.4.1**. Secondly, excess electrons near the silicon surface may tunnel through the oxide to the metal gate during the read procedure. This results in a positive gate current, partially counteracting the overall negative transient gate current. Finally, the number of excess inversion electrons decreases as they discharge through quantum tunneling. However, we will demonstrate below that the current and discharge attributable to quantum tunneling are negligible when compared to other mechanisms.

During the transient, inversion electrons tunnel from the silicon surface to the metal gate, allowing for direct measurement of the tunneling current at the gate. In **Figure 2−21** , we present the transient gate tunneling current alongside the gate displacement current and the gate total current for comparison. It is evident that the tunneling current is at least four orders of magnitude lower than the displacement current throughout the transient period. Thus, we can confidently conclude that the transient current resulting from quantum tunneling is negligible.

Next, we aim to demonstrate that quantum tunneling is not a significant discharge mechanism for excess inversion electrons. As depicted in **Figure 2−21** , the tunneling current remains below 10 pA for $t < 1$ μs and further decreases to below 1 pA for $t > 1$

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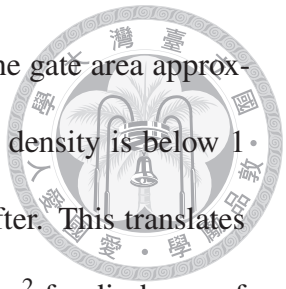

μs. With a device featuring a circular gate with a radius of 145 μm, the gate area approximately equals 6.6×10^{-4} cm^2. Consequently, the tunneling current density is below 1 nA/cm^2 for transient times before 1 μs and below 0.1 nA/cm^2 thereafter. This translates to approximately 1×10^{-9} nC/cm^2 within the first 100 μs and 1 nC/cm^2 for discharge of inversion charges up to 1 s due to quantum tunneling.

However, analysis from **Figure 2–14** reveals that the magnitude of the inversion charge approaches 1 $\mu C/cm^2$ (several hundreds of nC/cm^2), a significantly larger value than that resulting from quantum tunneling. Hence, we confidently conclude that the discharge of excess inversion electrons through quantum tunneling is negligible compared to other mechanisms, as discussed subsequently.

Diffusion and Recombination

For transient times after 100 ns, the device enters the 'Diffusion and Recombination' period. Excess inversion electrons near the silicon surface migrate towards the substrate. As these electrons traverse the depletion region, some undergo recombination with holes flowing in from the substrate. The remainder of the electrons that do not recombine continue their flow towards the substrate. This description illustrates that the total current density remains continuous. When electrons that should have flowed towards the substrate but recombine instead, an equivalent flow of holes, with the same magnitude, enters from the substrate.

For example, consider the current density inside the silicon at 100 μs in **Figure 3–3**. The electron current density is high near the surface, while the hole density is nearly zero. The negative electron current density indicates flow towards the surface, signifying electron movement towards the substrate. As this electron flow traverses the depletion region,

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a portion of the electron current transforms into hole current, maintaining the same direction. This implies that some outflowing electrons recombine with inflowing holes. Subsequently, these two current densities remain constant throughout the bulk silicon region until reaching the surface.

It is noteworthy that the total current density within the silicon remains almost constant, except for a slight decrease in magnitude around a depth of approximately 0.3 μm, which is near the edge of the depletion region. This decrease is attributed to hole depletion resulting from the expansion of the depletion region, as discussed earlier in **Section 3.2.2**.

Given the minor impact of the decrease in hole current compared to the total current density, we can temporarily disregard it to simplify the discussion and analytical modeling in the next section. Under this condition, we can infer that *the substrate electron and hole currents represent the diffusion and recombination currents, respectively,* in the 'Diffusion and Recombination' period. Therefore, we can analyze the composition of the substrate current during this period, as illustrated in **Figure 3–8**. For time periods between 1 μs and 1 ms, electron current dominates, indicating that the diffusion current is stronger than the recombination current. Conversely, for transient time after 1 ms, hole current dominates, suggesting that the recombination current is stronger than the diffusion current. This phenomenon can be attributed to reason as follows.

In the 'Diffusion and Recombination' period, both E_{Fn} and E_{Fp} are nearly constant within the silicon, as depicted in **Figure 3–5**. However, E_{Fn} at the substrate, being the final mesh node, is constrained to 0. The quasi-Fermi level splitting, denoted as $\Delta\phi_n$, is

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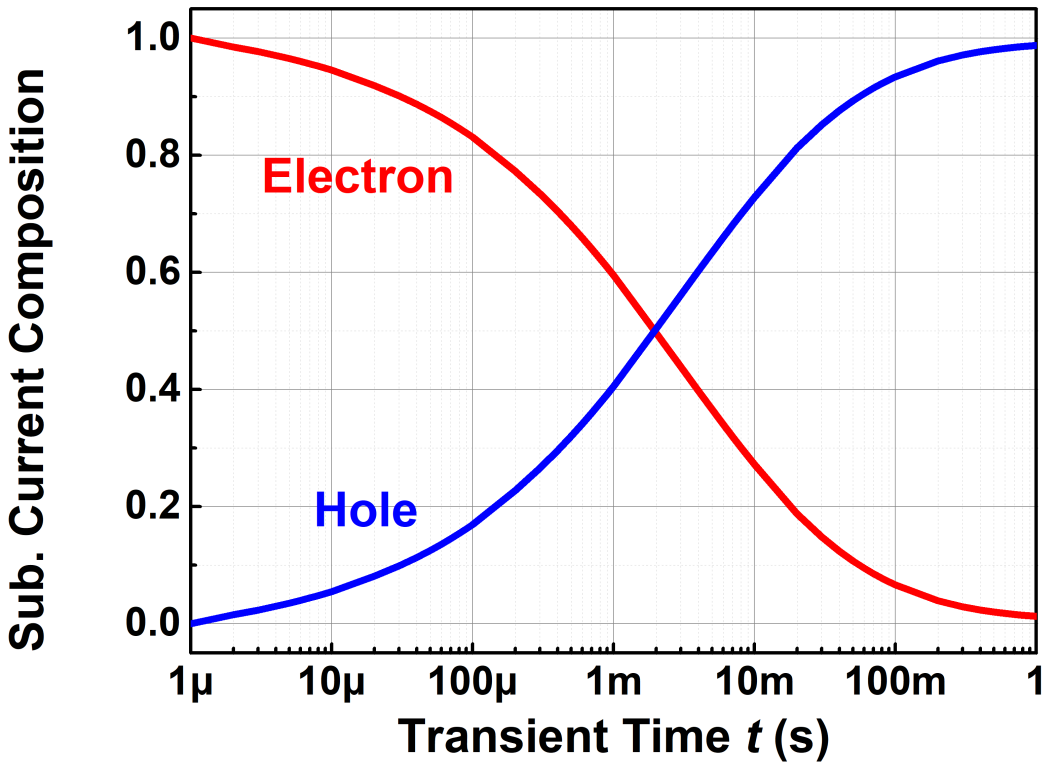

Figure 3–8. The substrate current composition during the transient time from 1 μs to 1 s. The electron current component represents the diffusion current. The hole current component represents the recombination current.

defined as the difference between E_{Fn} and E_{Fp}, given by:

$$\Delta\phi_n \equiv (E_{Fn} - E_{Fp})/q \tag{3.2}$$

When E_{Fn} exceeds E_{Fp} within the p-type silicon substrate, indicating a positive ϕ_m, the device exhibits a substrate current akin to a one-sided p-n diode with a short substrate under forward bias [89, 96, 117]. Consequently, the diffusion current J_n, can be expressed

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as:

$$J_n = J_{n0} \cdot \exp\left(\frac{\Delta\phi_n}{\phi_t}\right) \tag{3.3}$$

where $\phi_t \equiv kT/q$ is the thermal voltage, and

$$J_{n0} = \frac{qD_n n_i^2}{W_p N_A} \tag{3.4}$$

where D_n represents the diffusion coefficient for electrons in the p-type silicon, and W_p denotes the thickness of the silicon substrate. It is important to note that we utilize the short-base limit approximation here to streamline the calculation, considering that the electron diffusion length L_n surpasses the substrate thickness W_p [90]. For a more accurate expression, W_p in (3.4) should be substituted with $L_n \tanh(W_p/L_n)$.

On the contrary, describing the recombination current J_r is more intricate. The forward regime of the diode lacks an analytical expression for the recombination current, often necessitating numerical computation [121]. However, for simplification purposes, the recombination current can be approximated by the product of the maximum recombination rate within the silicon, denoted as R_{max}, and a fraction of the space charge region δW where significant recombination occurs [89], [90]. Furthermore, $R_{max} = n_i/2\tau \cdot \exp(\Delta\phi_n/2\phi_t)$, where τ denotes the carrier lifetime of both electrons and holes for simplicity. Thus, the recombination can be expressed as:

$$J_r = qR_{max}\delta W = J_{r0} \cdot \exp\left(\frac{\Delta\phi_n}{2\phi_t}\right) \tag{3.5}$$

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where

$$J_{r0} = \frac{qn_i\delta W}{2\tau} \tag{3.6}$$

Given that J_{r0} typically exceeds J_{n0}, J_n surpasses J_r only for a high ϕ_n, primarily due to the exponential factor being $1/\phi_t$ in the former and $1/2\phi_t$ in the latter. Conversely, as ϕ_n diminishes to a low value, J_n falls below J_r. At the same time, ϕ_n decreases from a positive value to 0 during the transient. Consequently, initially, J_n, or the electron current, dominates, followed by J_r, or the hole current, taking precedence thereafter. This trend elucidates the observations depicted in **Figure 3–8**.

Now that we have the analytical expression for the dominant current component at the silicon substrate, we can proceed to analytically investigate the transient current behavior of the Planar MIS device. The comprehensive derivation and calculations will be presented in the following section.

3.3 The Analytical Model

In this section, we will develop an analytical model to describe the transient current behavior of a Planar MISTD with a 30 Å oxide layer transitioning from a positive bias to 0 V. For the p-type silicon substrate under study, the device experiences deeper inversion under positive bias compared to the steady-state condition at 0 V. Consequently, excess inversion electrons will initially accumulate in the silicon and then gradually discharge. The resulting gate transient current densities J_g under different write voltages V_{Write} are illustrated in **Figure 3–9** (a). It is important to understand the decaying trend of the transient current in order to predict the retention time of J_g. Subfigure (b) depicts J_g at 1 ms

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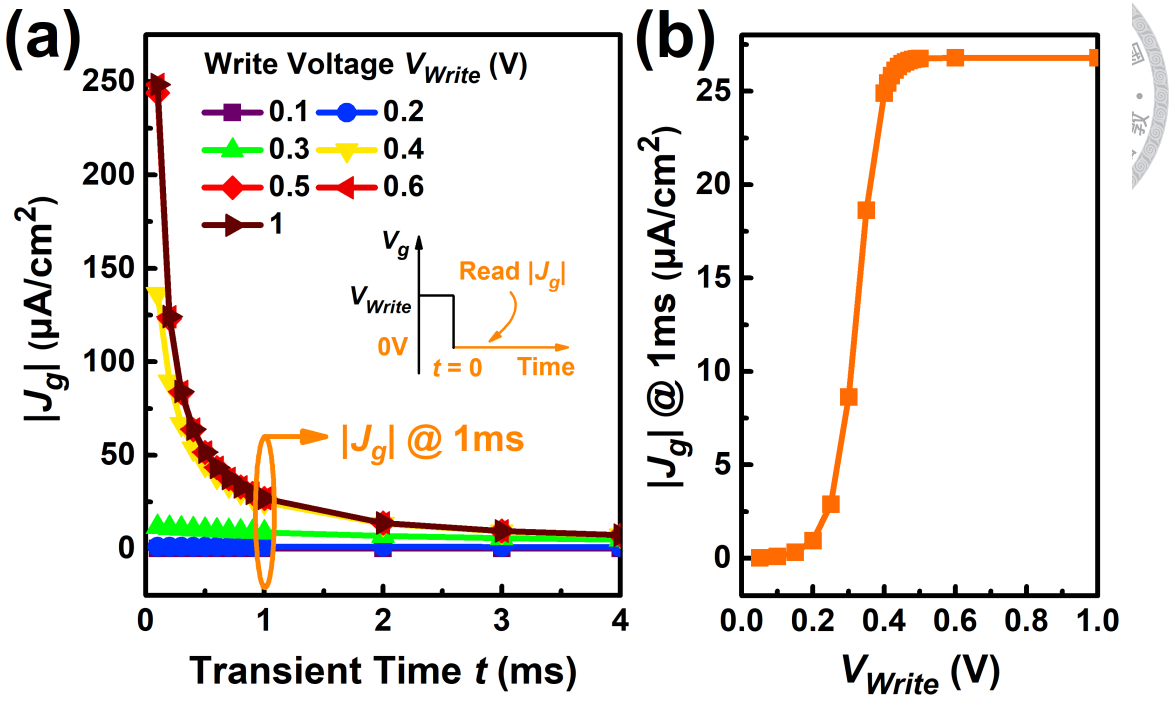

Figure 3–9. (a)Simulation results of the gate transient currents in the MISTD with different write voltages. Inset: Voltage program. (b) J_g at 1 ms against V_{Write}.

versus V_{Write}, where a clear saturation behavior is evident, as discussed in **Chapter 2**. It is also crucial to figure out the minimum required V_{Write} to achieve saturation, which is beneficial for the operation and design of the device for dynamic memory applications.

There were some previous research on the modeling of the transient behavior of MIS capacitors [65, 66]. However, most of these studies examined devices transitioning from flat-band conditions to the inversion regime, with discussions centered on the generation of minority carriers. Few investigations have addressed transient currents resulting from the discharge of inversion charges stored in the silicon.

Observations from **Figure 3–2** indicate that, for a 1 V write voltage, the total current, especially between 100 ns and 1 ms, exhibits a linear decay with time, evident from the slope of -1 in the log-log plot. This suggests an inverse relationship between the to-

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tal current and time ($J \sim 1/t$). This transient current behavior contradicts the typical exponential decay observed in R-C circuits with metal-insulator-metal (MIM) capacitors. While some academic papers have noted and discussed the $1/t$-decay transient current phenomenon [103, 122, 123], attributing it to the tunneling detrapping of pre-charged oxide traps, our TCAD simulation assumed an ideal oxide without any traps. Therefore, the $1/t$-decay transient current observed in our simulation is clearly not due to detrapping but rather an intrinsic aspect of discharging excess inversion charges. To the best of our knowledge, this is the first observation of an MIS device with an ideal oxide exhibiting transient current decay inversely with time.

We will then quantitatively model the transient currents to elucidate this phenomenon. The proposed analytical model will capture the temporal response of transient currents and electron quasi-Fermi level splitting, spanning the range from 100 ns to 1 ms. The modeling outcomes under low-voltage operation ($\leq$ 1 V), considering diffusion and recombination currents in the silicon, closely align with simulation results. Additionally, the proposed model can accurately predict the saturation write voltages, deviating by only 0.01 V from actual values without relying on simulation data.

3.3.1 1/*t* Decaying Transient Current

In this subsection, we will derive an analytical model to elucidate the $1/t$-decay gate transient current J_g for t ranging from 100 ns to 1 ms for the device transitioning from +1 V to 0 V. We focus on this aspect as it aligns with our primary concern, given that our discussion of the measurement results in **Chapter 2** primarily revolves around J_g. The investigation into substrate current J_s previously in this chapter serves to enhance our understanding of J_g behavior. However, it is essential to recognize that J_g and J_s are two sides of the same

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coin, as they possess identical magnitudes with opposite signs due to current continuity principles.

Figure 3–10 (a) and (b) illustrate the simulation results depicting the temporal response of the gate transient current J_g and the quasi-Fermi level splitting $\Delta\phi_n$, respectively, with trend lines included. The $J_g - t$ relationship in the log-log plot exhibits linearity, with a slope very close to -1, suggesting that J_g follows a $1/t$ dependence. Additionally, $\Delta\phi_n$ also decays linearly with ln$t$, with the slope magnitude approaching the thermal voltage ϕ_t. (Note: In the simulation, temperature $T = 293$ K, $\phi_t = 0.0253$ V, intrinsic carrier density $n_i = 8.2 \times 10^9$ cm^{-3}.)

The modeling procedure starts with the basic voltage balance equation across the MIS system, which has been written down at (3.1), but is emphasized here again:

$$V_G - V_{Fb} = -\frac{Q_s}{C_{ox}} + \psi_s \tag{3.7}$$

Since the device operates in the inversion regime under both 0 V and 1 V steady-state conditions, the number of depletion charges is negligible compared to the number of inversion charges. Therefore, Q_s can be approximated as [91]:

$$\begin{aligned} Q_s &= -\sqrt{2q\epsilon_s N_A}\sqrt{\psi_s + \phi_t \cdot \exp\left[\frac{\psi_s - 2\phi_F + \Delta\phi_n}{\phi_t}\right]} \\ &\approx -\sqrt{2\epsilon_s N_A k_B T} \cdot \exp\left[\frac{\psi_s - 2\phi_F + \Delta\phi_n}{2\phi_t}\right] \end{aligned} \tag{3.8}$$

By subtracting ψ_s from both sides of (3.7), taking the logarithm, and then differentiating

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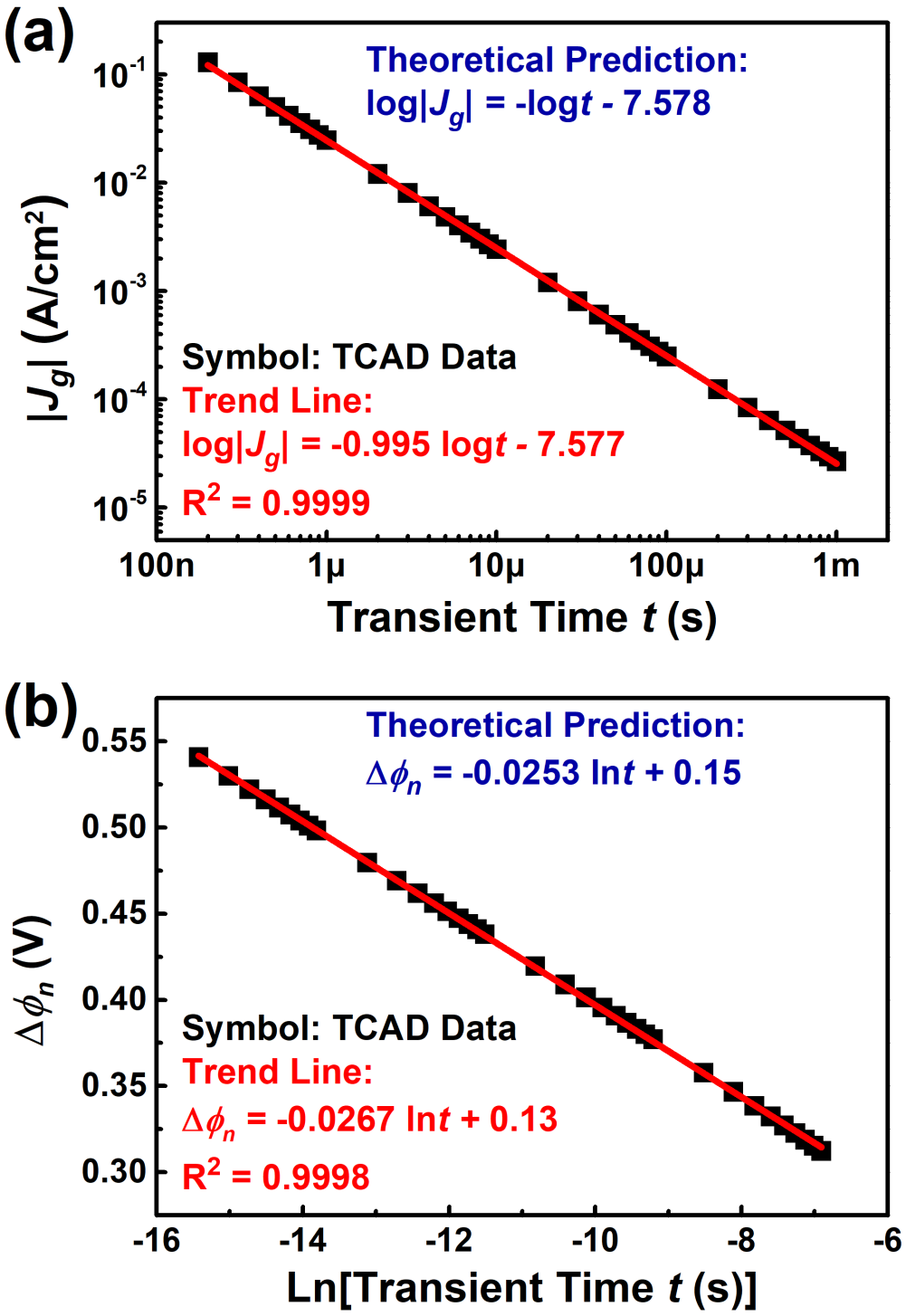

Figure 3–10. Temporal response of the (a) gate transient current density and (b) quasi-Fermi level splitting with transient time spanning from 100 ns to 1 ms. Symbols: Simulation results. Lines: Trend lines.

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with respect to time, we obtain the relation,

$$\frac{d\Delta\phi_n}{dt} = -\left(\frac{2\phi_t}{V_G - V_{Fb} - \psi_s} + 1\right)\frac{d\psi_s}{dt} = -\alpha\frac{d\psi_s}{dt} \tag{3.9}$$

with α defined as

$$\alpha \equiv \frac{2\phi_t}{V_G - V_{Fb} - \psi_s} + 1 \tag{3.10}$$

Based on the parameters used in the simulation, $V_G - V_{Fb} = 0.98$ V during the read procedure, and $2\phi_t = 0.0506$ V ($T = 293$ K). Over the transient period spanning from 100 ns to 1 ms, ψ_s varies between 0.45 V and 0.65 V. Consequently, α ranges from 1.095 to 1.153. For simplification purposes in subsequent discussions, we will assume that α can be treated as a constant with a value of 1.1.

The time differentiation of the total charges in the substrate (3.8) results in

$$\frac{dQ_s}{dt} = C_{ox}\frac{d\psi_s}{dt} = -\frac{C_{ox}}{\alpha}\frac{d\Delta\phi_n}{dt} \tag{3.11}$$

Therefore, the gate current density J_g can be related with $\Delta\phi_n$ due to the current continuity,

$$J_g = -J_s = -\frac{dQ_s}{dt} = \frac{C_{ox}}{\alpha}\frac{d\Delta\phi_n}{dt} \tag{3.12}$$

Given that the discharge of excess inversion electrons in the silicon is primarily governed by the diffusion process as discussed in the previous subsection, J_s can also be represented by the diffusion current J_n in (3.3). Connecting (3.3) and (3.12) yields a differential equa-

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tion for $\Delta\phi_n$,

$$\frac{d\Delta\phi_n}{dt} = -\frac{\alpha J_{n0}}{C_{ox}} \cdot \exp\left(\frac{\Delta\phi_n}{\phi_t}\right) \tag{3.13}$$

The general solution is given as:

$$\Delta\phi_n = -\phi_t \cdot \ln(t + t_0) - \phi_t \cdot \ln\left(\frac{\alpha J_{n0}}{C_{ox}\phi_t}\right) \tag{3.14}$$

$$J_g = -\frac{C_{ox}\phi_t}{\alpha(t + t_0)} \tag{3.15}$$

Here, t_0 represents an initial time constant, which can be determined with one data point or through theoretical calculation. We will adress the determination of t_0 later. When $t \ll t_0$, J_g remains nearly constant, while when $t \gg t_0$, J_g decays inversely with time. For a write voltage of 1 V, exceeding the saturation voltage discussed in **Chapter 2**, t_0 becomes negligible compared to the range of interest for t here (from 100 ns to 1 ms). Consequently, the gate transient current is given by:

$$J_g = -\frac{C_{ox}\phi_t}{\alpha t} \tag{3.16}$$

This elucidates the $1/t$-decay trend observed in the gate transient current. Additionally, when t_0 can be disregarded, it allows for the computation of the specific parameters' numerical values in (3.14) and (3.15) for the device utilized in the simulation,

$$\log|J_g| = -\log t - 7.578 \tag{3.17}$$

$$\Delta\phi_n = -0.0253 \cdot \ln t + 0.15 \tag{3.18}$$

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The calculation results presented above are juxtaposed with the trend lines in simulation outcomes, as illustrated in **Figure 3–10**. It is evident that the results generated by the model closely align with the simulation results, especially concerning the gate transient current. This correspondence suggests that the proposed model effectively elucidates the phenomenon of $1/t$ decaying transient currents.

3.3.2 Recombination-Dominant Regime

The derivation above has assumed that the substrate current is dominated by the diffusion current J_n. However, this assumption holds true only for large values of $\Delta\phi_n$. When $\Delta\phi_n$ is low, the substrate current is dominated by recombination. Consequently, the substrate current should now be expressed by the recombination current J_r in (3.5). Following a similar derivation as above, we can derive expressions for J_g and $\Delta\phi_n$ in the recombination-dominant regime as follows:

$$\Delta\phi_n = -2\phi_t \cdot \ln(t + t_0) - 2\phi_t \cdot \ln\left(\frac{\alpha J_{r0}}{2C_{ox}\phi_t}\right) \tag{3.19}$$

$$J_g = -\frac{2C_{ox}\phi_t}{\alpha(t + t_0)} \tag{3.20}$$

Therefore, we have derived the expression for the gate transient current J_g for t from 100 ns to 1 ms. However, before using (3.15) and (3.20) to model the current, it is crucial to know when the device is in the diffusion-dominant and recombination-dominant regimes. Therefore, we need to first study the the ratio between the diffusion and recombination currents.

Note that J_{r0} is expressed in (3.6). The parameter δW within, representing the fraction of the space charge region where the recombination is significant, can only be estimated

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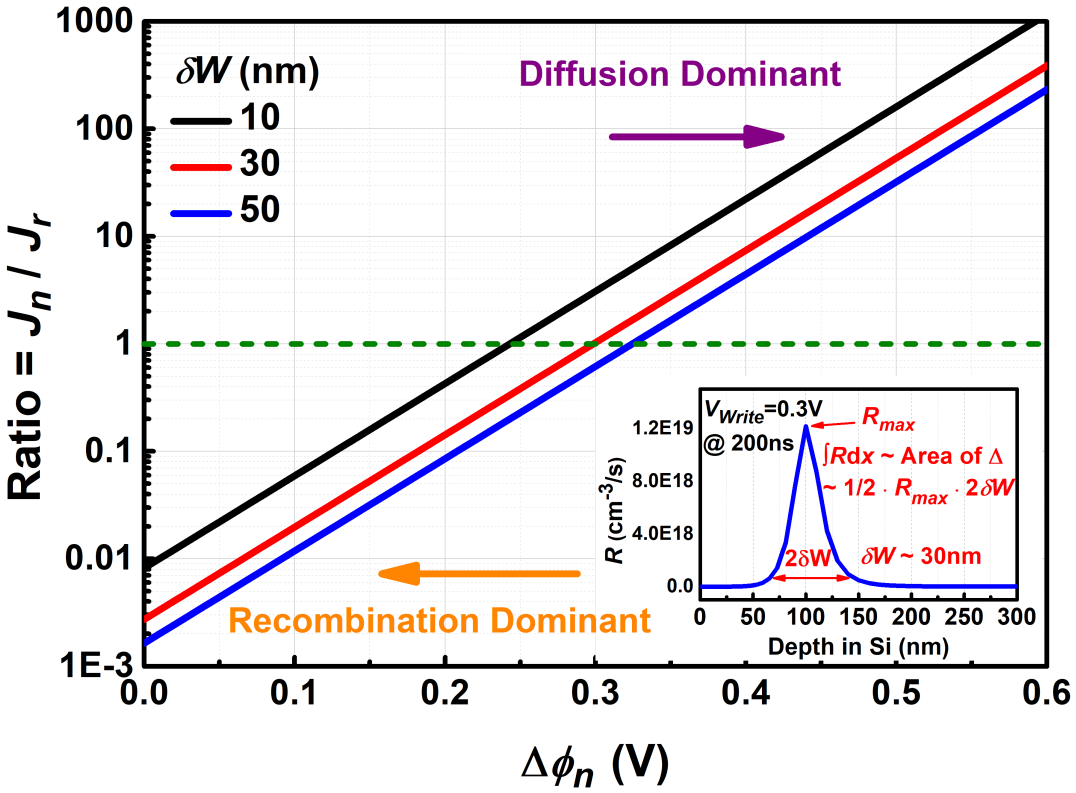

Figure 3–11. Ratio of the diffusion current and the recombination current under different $\Delta\phi_n$. The device is in the recombination-dominant and the diffusion-dominant regime for $\Delta\phi_n$ lower and larger than 0.3 V, respectively. Inset: The recombination rate R along the depth in the silicon, for V_{Write} = 0.3 V at t = 200 ns. Accordingly, δW is determined as 30 nm.

by examining the spatial distribution of the recombination rate, where detailed information on the physical quantities in the silicon is needed. It may depend on the value of $\Delta\phi_n$, increasing the complexity for the modeling δW [89, 90]. Therefore, to simplify the discussion, we can only roughly estimate a constant value for δW.

This value of δW is determined according to the simulation results of write voltage V_{Write} = 0.3 V at 200 ns. The inset of **Figure 3–11** displays the spatial distribution of the recombination rate R inside the silicon. The overall recombination $R_{max}\delta W$ equals the integral of R with respect to the depth in the silicon and can be approximated by the area

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of the triangle under the curve. According to the triangle area formula, δW is half of the base of the triangle, which is about 30 nm in this case. As a result, we adopt 30 nm to be the value for δW in the following for simplification.

Figure 3–11 shows the ratio of the diffusion current and the recombination current against $\Delta\phi_n$. When the ratio is greater than 1, the substrate current is diffusion-dominant; when the ratio is lower than 1, it becomes recombination-dominant. Accordingly, we consider that $\Delta\phi_n \leq 0.3$ V to be recombination-dominant, while $\Delta\phi_n > 0.3$ V to be diffusion-dominant for simplicity in the subsequent modeling procedure.

3.3.3 Modeling Results

Figure 3–12 illustrates the simulation outcomes depicting the temporal response of $\Delta\phi_n$ for V_{Write} varying from 0.1 to 1 V, with t spanning from 200 ns to 1 ms. When $V_{Write} \leq 0.3$ V, the magnitude of $\Delta\phi_n$ remains below 0.3 V within this time span, indicating recombination-dominant. Conversely, for $V_{Write} \geq 0.4$ V, $\Delta\phi_{\mathrm{n}}$ exceeds 0.3 V, signifying diffusion-dominant. Accordingly, we employed (3.15) to model J_g in the diffusion-dominant regime and (3.20) in the recombination-dominant regimes, for $V_{Write} \leq 0.3$ V and $V_{\mathrm{w}} \geq 0.4$ V, respectively.

The results of the modeling are showcased in **Figure 3–13** , juxtaposed with the TCAD simulation outcomes. Here, the parameter t_0 for each curve is calibrated using the initial data point of the simulation result, specifically J_g at 200 ns. The modeling results exhibit a strong alignment with the simulation findings. Nonetheless, it is vital to acquire at least one data point for each write voltage to accurately determine the value of t_0 and effectively model the transient current. In the subsequent subsection, we propose a method to theoretically compute the values of t_0, streamlining the modeling of transient currents without relying on simulation results.

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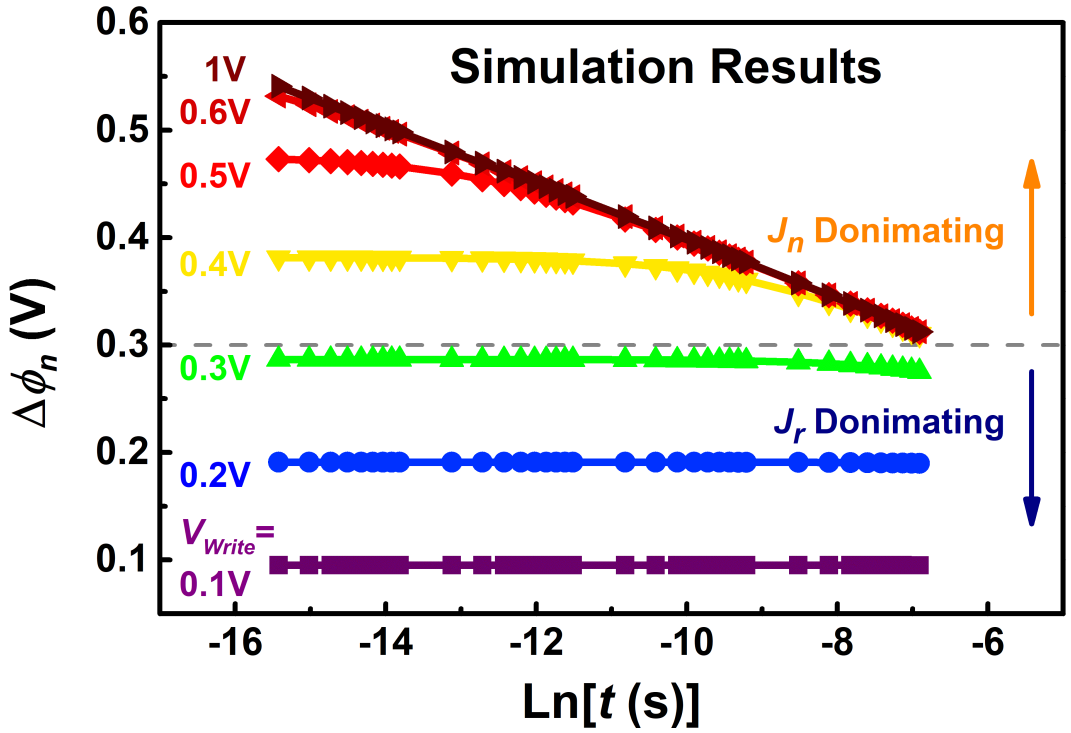

Figure 3–12. Simulation results of $\Delta\phi_n - \ln t$ relation from 100 ns to 1 ms for V_{Write} varying from 0.1 to 1 V.

3.3.4 Discussion on Initial Time Constant t_0

In this subsection, we aim to demonstrate that t_0 can be theoretically determined by V_{Write}.

Initially, it is noted that t_0 can be determined by $\Delta\phi_n$ at the onset of the transient. The instants immediately before and after the onset of the transient are defined as infinitesimal $t = 0^-$ and $t = 0^+$, respectively. Given that $t_0 \gg t$ at $t = 0^+$, by establishing a relationship between (3.3) and (3.15), we can derive the expression for t_0 in the diffusion-dominant regime:

$$t_0 = \frac{C_{ox}\phi_t}{\alpha J_{n0}} \exp\left(-\frac{\Delta\phi_n(t = 0^+)}{\phi_t}\right) \tag{3.21}$$

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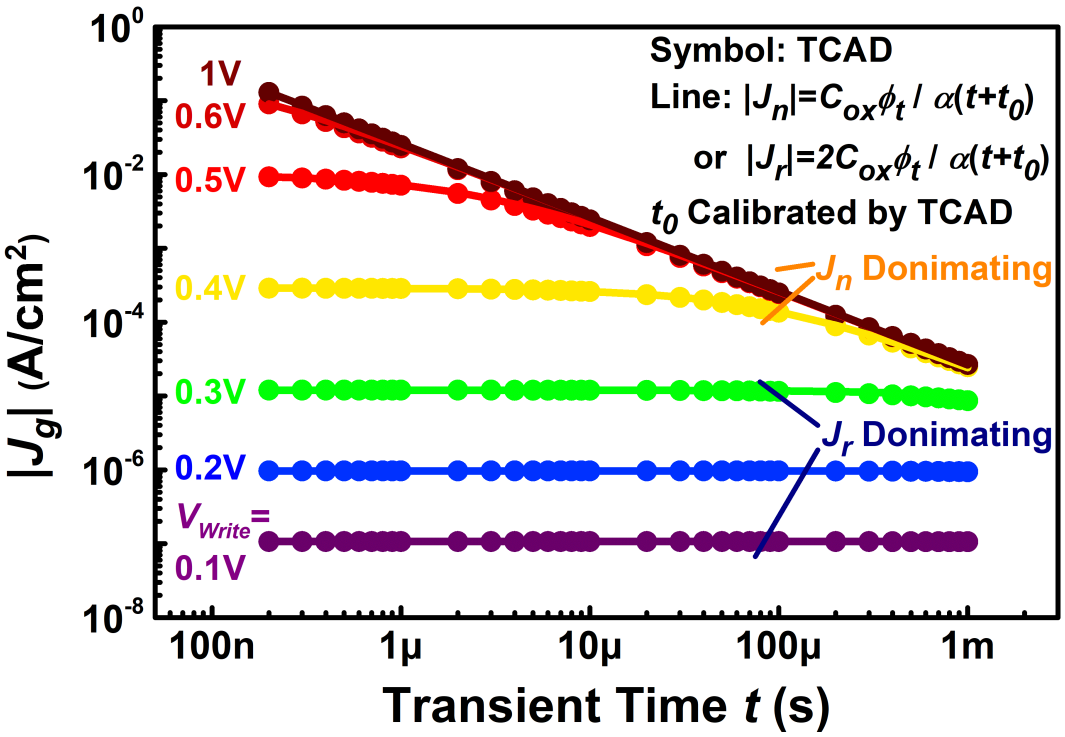

Figure 3–13. Temporal response of the gate transient current for V_{Write} varying from 0.1 to 1 V. Symbols: TACD simulation results. Lines: Modeling results. t_0 is calibrated by the initial simulation data point.

Similarly, t_0 in the recombination-dominant regime can be determined by (3.5) and (3.20):

$$t_0 = \frac{2C_{ox}\phi_t}{\alpha J_{r0}} \exp\left(-\frac{\Delta\phi_n(t=0^+)}{2\phi_t}\right) \tag{3.22}$$

Next, we will show that $\Delta\phi_n(t = 0^+)$ is close to V_{Write} if the device has not entered into the deep depletion regime yet under the steady-state at V_{Write}.

The voltage balance equation (3.7) during the write procedure is expressed as

$$V_{Write} - V_{Fb} = -\frac{Q_s(t=0^-)}{C_{ox}} + \psi_s(t=0^-) \tag{3.23}$$

At the moment when the gate voltage switches to $V_{Read} = 0$ V, Q_s remains unchanged,

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implying that $Q_s(t = 0^+) = Q_s(t = 0^-)$. Consequently, the entire drop in gate voltage is absorbed by ψ_s, resulting in

$$\psi_s(t = 0^+) - \psi_s(t = 0^-) = V_{Read} - V_{Write} = -V_{Write} \tag{3.24}$$

Based on the expression of Q_s (3.8), $Q_s(t = 0^+) = Q_s(t = 0^-)$ implies that

$$\Delta\phi_n(t = 0^+) - \Delta\phi_n(t = 0^-) = -[\psi_s(t = 0^+) - \psi_s(t = 0^-)] = V_{Write} \tag{3.25}$$

For a low V_{Write}, the device remains in the inversion regime during the writing procedure, with a negligible splitting between E_{Fn} and E_{Fp}. Consequently, $\Delta\phi_n(t = 0^-) = 0$. Conversely, under a large V_{Write}, there might be an electron deficiency at the silicon surface, resulting in $\Delta\phi_n(t = 0^-) < 0$. Fortunately, within the range of V_{Write} under discussion here (0.1 ~ 1 V), $\Delta\phi_n(t = 0^-)$ is negligible compared to $\Delta\phi_n(t = 0^+)$. Hence, a simple yet crucial relation can be established as follows:

$$\Delta\phi_n(t = 0^+) \approx V_{Write} \tag{3.26}$$

Figure 3–14 examines the relationships (3.25) and (3.26) through simulation results. It is evident that $\Delta\phi_n(t = 0^+)$ is very close to V_{Write} for the considered conditions. Hence, we can theoretically calculate t_0 for each V_{Write} ranging from 0.1 to 1 V using (3.21), (3.22), and (3.26), and model the transient currents without relying on simulation results. The modeling results, depicted as lines in **Figure 3–15**, with theoretically calculated t_0, closely align with the simulation results (represented by symbols), indicating the reason-

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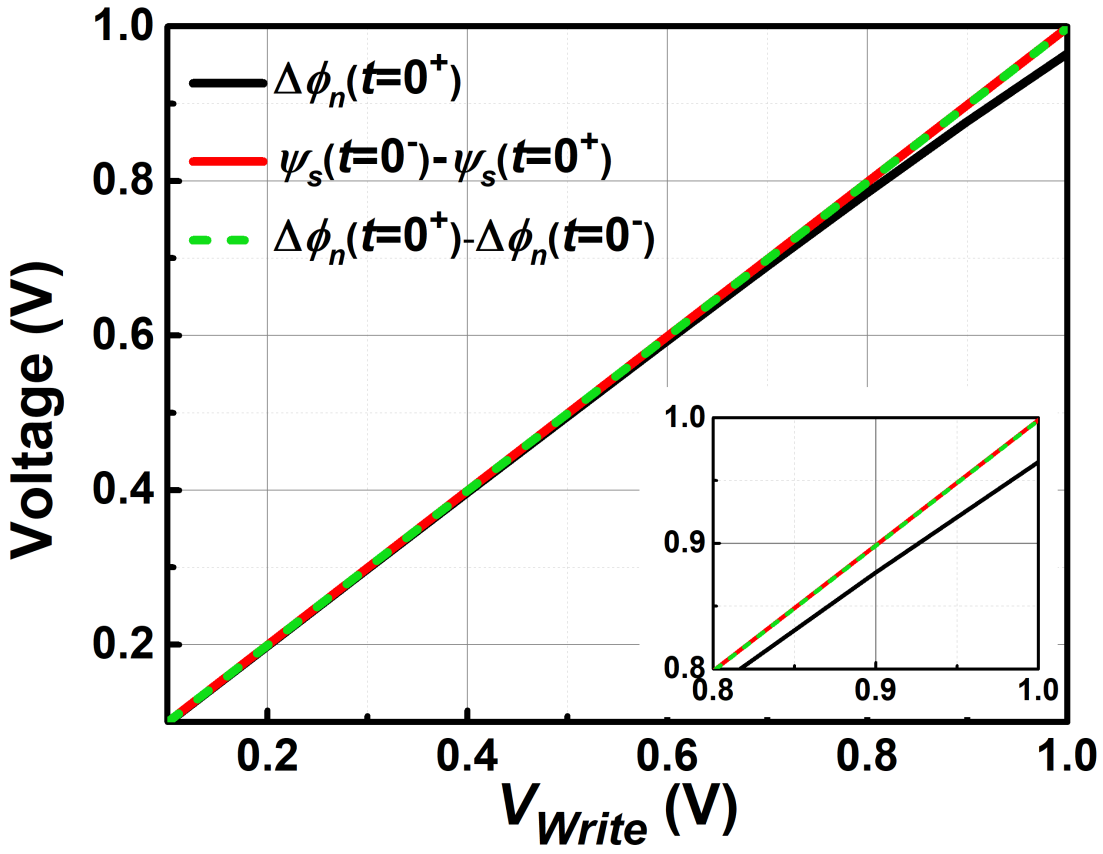

Figure 3–14. $\Delta\phi_n$ before the onset of transient ($\Delta\phi_n(t = 0^+)$), the difference between ψ_s before and after the onset of transient ($\psi_s(t = 0^-) - (\psi_s(t = 0^+)$), and the difference between $\Delta\phi_n$ right after and before the onset of transient ($\Delta\phi_n(t = 0^+) - \Delta\phi_n(t = 0^-)$) against V_{Write}. Inset: Enlargement for V_{Write} from 0.8 to 1 V.

ableness of the t_0 estimation above.

3.3.5 Saturation Voltage

In **Figure 3–9** , we observe that J_g saturates for large V_{Write} at 1 ms. The saturation write voltage $V_{Write,sat}$ can be predicted now that J_g can be modeled. It is noteworthy that this saturation write voltage has been discussed in **Chapter 2**, and we have derived expressions for it in (2.12) and (2.15). In the derivation of these two equations, we assumed that saturation would occur when the stored inversion charges surpass the saturated value

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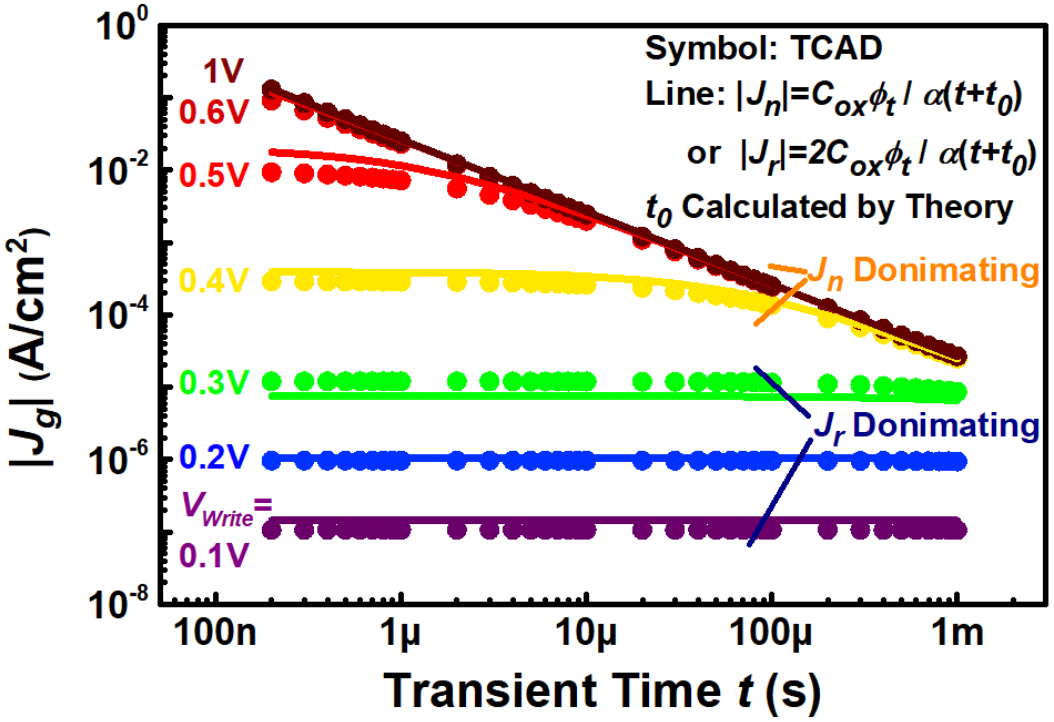

Figure 3–15. Temporal response of the gate transient current for V_{Write} varying from 0.1 to 1 V. Symbols: TACD simulation results. Lines: Modeling results. t_0 is calibrated theoretically without any input from the simulation data.

$Q_{inv,sat}$ or when the silicon band bending is suppressed below $\psi_{s,min}$ at the hundreds of nanoseconds time-scale. However, this approach may overestimate $V_{Write,sat}$, as although the aforementioned criteria may not be met at the hundreds of nanoseconds time-scale, the subsequent discharge of inversion electrons, dominated by the diffusion or recombination process, may still lead to the saturation of the transient current. With the analytical model proposed above, we can derive a more accurate value for $V_{Write,sat}$, incorporating the mechanisms related to the discharge of excess inversion electrons.

First, we carefully define $V_{Write,sat}$ as the write voltage where the magnitude of J_g at

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t_{Read} reaches 99% of that for a 1 V write voltage, that is,

$$\frac{J_g(V_{Write,sat}, t_{Read})}{J_g(V_{Write} = 1\text{V}, t_{Read})} = 0.99 \tag{3.27}$$

Since t_0 is negligible for V_{Write} = 1 V, according to (3.15), the requirement above becomes

$$\frac{t_{Read}}{t_{Read} + t_{0,sat}} = 0.99 \tag{3.28}$$

where $t_{0,sat}$ is the t_0 when saturation happens. Accordingly, it can be expressed as,

$$t_{0,sat} = 0.01 t_{Read} \tag{3.29}$$

For t_{Read} = 1 ms, $t_{0,sat} = 10^{-5}$ s. By utilizing (3.21) and (3.26), we can forecast the saturation write voltage in the following manner:

$$V_{Write,sat} = -\phi_t \cdot \ln\left(\frac{\alpha J_{n0} t_{0,sat}}{C_{ox}\phi_t}\right) \tag{3.30}$$

In this case, $V_{Write,sat}$ = 0.45 V.

Figure 3–16 (a) depicts the magnification of J_g at 1 ms to determine the value of $V_{Write,sat}$, which is approximately 0.46 V, closely resembling the predicted value mentioned above. Additionally, we can plot t_0 against V_{Write}, where $t_{0,sat}$ can be identified when the curve intersects the line of $t_0 = 10^{-5}$ s. **Figure 3–16** (b) presents the values of t_0 obtained through calibration of simulation data and theoretical calculations exclusively. The prediction is remarkably accurate for the TCAD-calibrated data, as the modeling results of J_g closely align with the simulation results. Moreover, the deviation between $t_{0,sat}$

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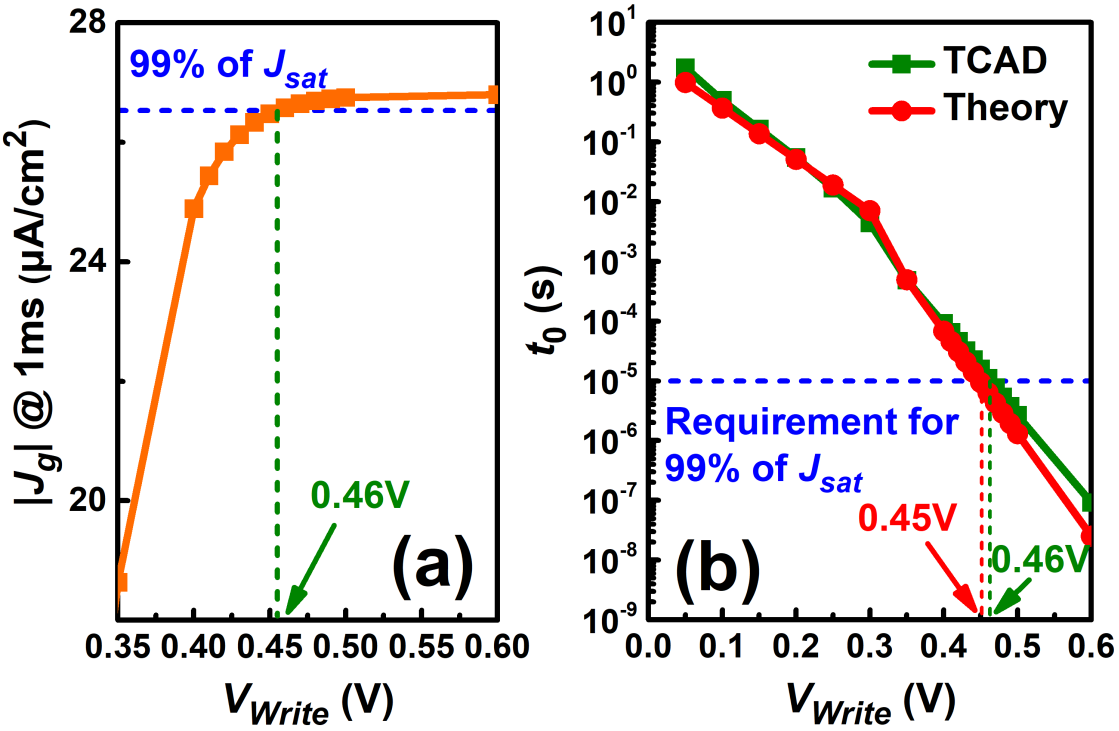

Figure 3–16. (a) J_g at 1 ms against the V_{Write}, with $V_{Write,sat}$ highlighted. (b) TCAD-calibrated and theoretic-calculated t_0 under different V_{Write}.

obtained from simulation results and theoretical calculations is merely about 0.01 V. Additionally, transient simulations are also conducted at T = 350 K, yielding a $V_{w,sat}$ = 0.29 V. Concurrently, according to (3.30), a predicted $V_{Write,sat}$ = 0.30 V is estimated at that temperature, deviating from the simulation value by only 0.01 V. This suggests that the model has the potential to be applied effectively at high temperatures.

3.4 Summary

In this chapter, we investigated the transient behavior in the Planar MISTD in the sub-millisecond regime through TCAD simulation and analytical modeling. In **Section 3.2**, initially, we conducted a detailed examination of the temporal response of electron and hole current densities within the silicon and at the substrate, alongside the distribution of

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carrier concentrations, band diagrams with electron and hole quasi-Fermi levels included, the recombination rate, and the depletion width. This analysis was performed when the device, featuring a 30 Å oxide layer, transitioned from +1 V to 0 V. Based on the motion of holes, we delineated the entire transient into three distinct periods: 'Dielectric Relaxation', 'Hole Depletion', and 'Diffusion and Recombination'.

During the 'Dielectric Relaxation' period, encompassing transient times less than 1 ns ($t < 1$ ns), holes migrated from the substrate into the silicon surface in response to the instantaneous decrease in ψ_s. This results in a significant positive substrate hole current. Concurrently, the diffusion of excess electrons had not yet reached the substrate, thus, the substrate current was predominantly governed by the positive hole current. Notably, substantial recombination occurred within the silicon during this phase, resulting in the 'Saturation Phenomenon' discussed in **Chapter 2**.

In the 'Hole Depletion' (1 ns $< t <$ 1μs) and 'Diffusion and Recombination' ($t >$ 1μs) periods, two primary hole current components were identified. The first stemmed from hole depletion induced by the expansion of the depletion region, leading to a negative substrate hole current. The second originated from the influx of holes for recombination with excess electrons, resulting in a positive substrate hole current. During the 'Hole Depletion' period, the dominance of the first term yielded a negative total substrate hole current. Additionally, with the diffusion of electrons reaching the substrate during this phase, the overall substrate current was dominated by the positive substrate electron current.

In contrast, during the 'Diffusion and Recombination' period, the second term took precedence, resulting in a positive total substrate hole current. As the excess inversion electrons were discharged from the silicon surface, some directly flowed to the substrate,

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generating a positive substrate electron current, while others underwent recombination with holes originating from the substrate, thereby contributing to a positive substrate hole current. Consequently, the substrate electron and hole currents were characterized as the diffusion and recombination currents, respectively.

We observed that for the device transitioning from +1 V to 0 V, the substrate current was diffusion-dominant within a transient time ranging from 100 ns to 1 ms (100 ns $< t <$ 1 ms). Additionally, we noted that the gate transient current decayed inversely with transient time $J_g \sim 1/t$ during this time period.

Subsequently, we introduced an analytical model in **Section 3.3** for the temporal response of the gate current and quasi-Fermi level splitting. The derivation also demonstrated that $J_g \sim 1/t$. Furthermore, by considering the recombination current, we successfully modeled the transient current for write voltages ranging from 0.1 to 1 V, with the modeling results exhibiting strong agreement with the simulation results. The analytical model accurately predicted the saturation write voltage, with a deviation of only 0.01 V.

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4

Improvement of Transient Behavior in The Designed Ultra-Thin Metal Surrounded Gate MISTD

4.1 Introduction

In In the introductory chapter, we explored the potential of leveraging the transient behavior of MISTD devices for dynamic memory applications. The subsequent chapters have been dedicated to examining the transient current characteristics of Planar MISTD devices, with a focus on variations in oxide thickness and their response to dif-

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ferent voltage programming schemes. A key area of interest has been the gate transient current, denoted as I_{Read}, measured 50 ms following the transient's initiation. This specific measurement interval was chosen because it approximates the refresh cycle timing of contemporary dynamic memory systems. A higher I_{Read} magnitude simplifies the process of memory state discrimination. The experiments detailed in **Chapter 2** reveal that, under conditions of positive voltage application, the Planar MISTD devices exhibit a maximum I_{Read} in the realm of hundreds of picoamperes. To illustrate, with write time T_{Write} of 10 ms and 1000 ms, the peak observed values of $|I_{Read}|$ at 50 ms were approximately 100 pA and 600 pA, respectively.

In the current and forthcoming chapters, our aim is to engineer novel structures within MISTD devices to improve the magnitude of I_{Read} into the nanoampere range. This chapter delves into the transient behavior of MISTD devices featuring an ultra-thin metal surrounded gate (UTMSG), a topic for which the foundational electrical properties, such as current-voltage ($I-V$) and capacitance-voltage ($C-V$) characteristics, alongside primary transient phenomena including transient current ($I-t$) and transient capacitance ($C-t$), have been preliminarily investigated in the preceding studies [79, 80, 124]. Despite these initial investigations, several facets of UTMSG behavior remain unexplored and warrant further examination. In this discourse, we identify and elaborate on various dimensions where our investigation extends beyond the scope of earlier research:

- The write and read voltage programs utilized in preceding studies lacked a uniform standard. In contrast, this chapter employs the identical write voltage programs as delineated in **Chapter 2** to investigate the transient current characteristics of UTMSG devices.

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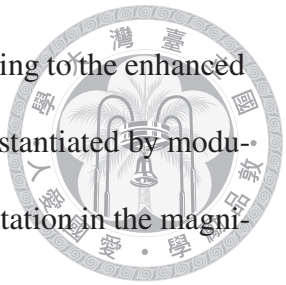

- A more comprehensive elucidation of the mechanisms contributing to the enhanced I_{Read} in UTMSG devices is provided. This enhancement is substantiated by modulating the read voltage V_{Read}, which yields a significant augmentation in the magnitude of I_{Read}.

- The discovery of atypical $C-V$ characteristics in UTMSG devices is reported, which could be harnessed to achieve an enhanced transient capacitance window.

- The effect of the area proportion of the surrounding gate on both the $C-V$ characteristics and transient behavior of UTMSG devices is thoroughly examined.

The structural design of the UTMSG device is depicted in **Figure 4–1** (a), juxtaposed with the Planar device configuration shown in subfigure (b) for comparison. The Planar device has an aluminum top gate with a thickness of 150 nm. In contrast, the UTMSG device's top gate is ingeniously constructed from a dual-gate system: a center gate featuring thick aluminum with a thickness of 150 nm, encircled by a surrounding gate composed of ultra-thin aluminum, approximately 10 nm thick. The entire gate's radius, denoted as r_o, is set at 145 μm, mirroring the gate radius of the Planar configuration. The radius of the central gate, referred to as r_i, is experimentally varied between 85 μm and 115 μm within this study. A noteworthy design aspect is the inclusion of a thin insulating layer of aluminum oxide around the center gate's sidewall, acting as a high-resistance barrier. This layer is instrumental in inducing an R-C time delay for carriers beneath the surrounding gate, thereby enhancing the transient response of the UTMSG device.

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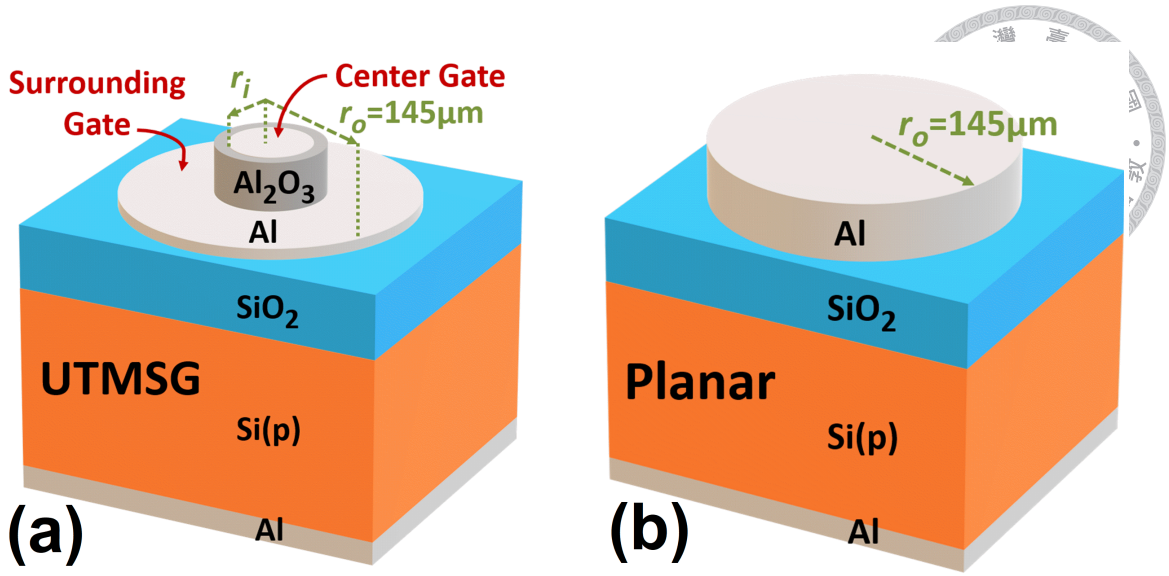

Figure 4–1. Schematics of the (a) UTMSG and (b) Planar devices, respectively. r_o denotes the radius of the whole gate in both UTMSG and Planar devices, and is set as 145 μm. r_i denotes the radius of the center gate in the UTMSG device, varying from 85 to 115 μm in this study.

4.2 Experimental

Figure 4–2 elaborates on the fabrication process flow. The initial substrate, a 3-inch p-type boron-doped silicon wafer with a resistivity spanning 1-10 Ω-cm, undergoes a thorough cleansing via the standard Radio Corporation of America (RCA) protocol. Subsequent to this, the silicon wafer, accompanied by a Pt electrode, is submerged in deionized (D.I.) water, with an applied voltage of +15 V facilitating the growth of a SiO_2 layer roughly 3 nm thick through anodic oxidation. A post-oxidation annealing step then follows, utilizing a rapid thermal process (RTP) in a 20 torr N_2 atmosphere at 950 °C for 15 seconds.

For the Planar device, photolithography post thermal evaporation of 150 nm aluminum defines the top electrode with a radius of 145 μm. Conversely, for the UTMSG device, center gates with radii of 85, 100, and 115 μm are initially outlined subsequent to the

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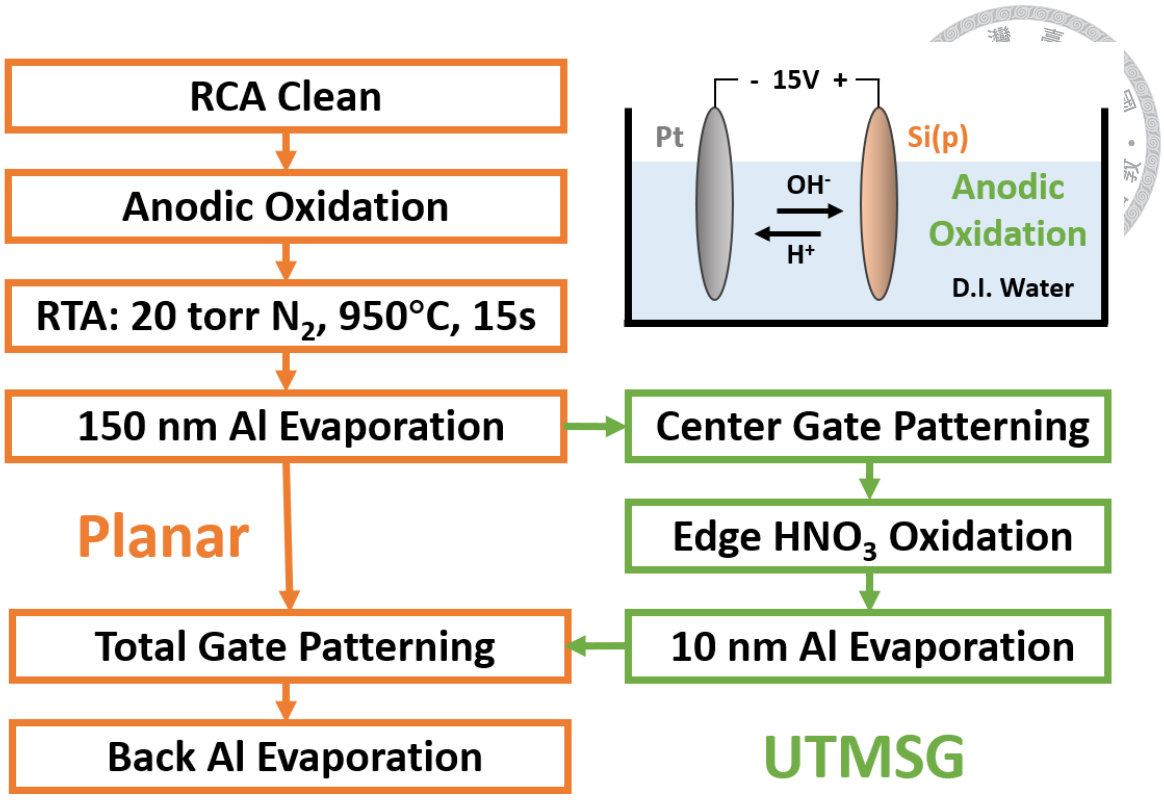

Figure 4–2. The experimental process flow chart of Planar and UTMSG devices.

evaporation of 150 nm aluminum. The application of dilute nitric acid serves to passivate the sidewall of the center gate, engendering a thin insulating layer of aluminum oxide. Thereafter, an ultra-thin aluminum film, 10 nm in thickness, is evaporated and patterned to form the total gate with a radius of 145 μm. It is noteworthy that within UTMSG devices, the center gate comprises thick metal of 150 nm thickness, whereas the surrounding gate is fashioned from a resistive, ultra-thin metal merely 10 nm thick. Culminating the process for both Planar and UTMSG devices, the back oxide is removed via buffer oxide etchant, followed by the evaporation of 150 nm aluminum to establish the back contact.

TABLE 4–I catalogs the parameters of the fabricated Planar and UTMSG devices, with particular emphasis on the proportion of surrounding gate, denoted as *S*. This parameter is underscored as it represents a focal point of discussion within this study.

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TABLE 4–I
Proportion of surrounding gate, S, of the UTMSG devices used in this work.

Device	r_o	r_i	Proportion of Surrounding Gate, S
Planar	145	NA	0
UTMSG		85	0.66
		100	0.52
		115	0.37

4.3 Improved Transient Current of The UTMSG MISTD

The improved transient current performance of UTMSG devices was highlighted in [79]. Nonetheless, the study in [79] presented a singular value for the proportion of the surrounding gate, denoted as S, fixed at 0.36. In **Figure 4–3**, we conduct a comparative analysis of the read currents (I_{Read}) for UTMSG devices featuring varying S values against that of the Planar device. The transient current was measured at -0.2 V following a 2 V write pulse applied for 1 s (V_{Write} = 2 V, T_{Write} = 1 s). It is evident from the comparison that UTMSG devices exhibit a higher I_{Read} magnitude, which further increases with a larger S. Notably, the UTMSG device with S = 0.66 can achieve a maximum current improvement factor of 9 times relative to the Planar device.

Subsequently, we extracted the magnitude of I_{Read} at 50 ms for different read voltages V_{Read}, maintaining a constant voltage program with V_{Write} = 2 V and T_{Write} = 1 s, as illustrated in **Figure 4–4**. It is apparent that the magnitude of I_{Read} increases with the proportion of the surrounding gate S, across all V_{Read} values. In particular, for the UTMSG device with S = 0.66, the I_{Read} magnitude at 50 ms under a V_{Read} of 0 V, employing the same voltage program as examined in **Chapter 2**, achieves 2.7 nA. This is approximately 4.5 times greater than the outcome for the Planar MISTD device discussed in **Chapter 2**. Additionally, it is noteworthy that the UTMSG devices demonstrate their highest I_{Read}

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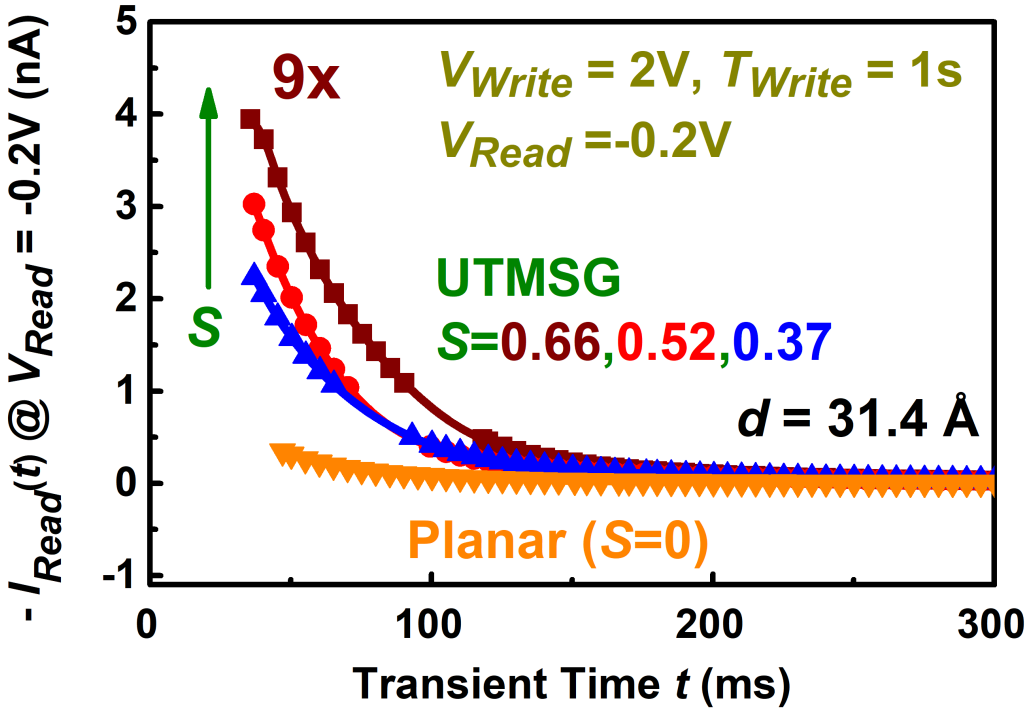

Figure 4–3. Transient currents of the UTMSG devices with varying S, compared to that of the Planar device, read at -0.2 V under V_{Write} = 2 V and T_{Write} = 1 s.

magnitude at a V_{Read} of -0.2 V.

The phenomenon observed can be elucidated through the edge late response effect, as illustrated in **Figure 4–5**. In the Planar device scenario, the gate voltage transition from 2 V to -0.2 V initiates the diffusion of electrons, the minority carriers, from the inversion layer towards the substrate back contact. This action triggers the discharge of positive charges accumulated at the top gate through the external circuit, generating a positive displacement current, I_d. Conversely, in the UTMSG device, the voltage switch at the top center gate does not occur simultaneously at the surrounding gate due to an R-C time delay. This delay is induced by the resistive ultra-thin metal layer and the insulating aluminum oxide layer that links the center gate with the surrounding gate [125, 126]. Consequently, the potential at the surrounding gate in the UTMSG device decreases to -0.2 V more slowly

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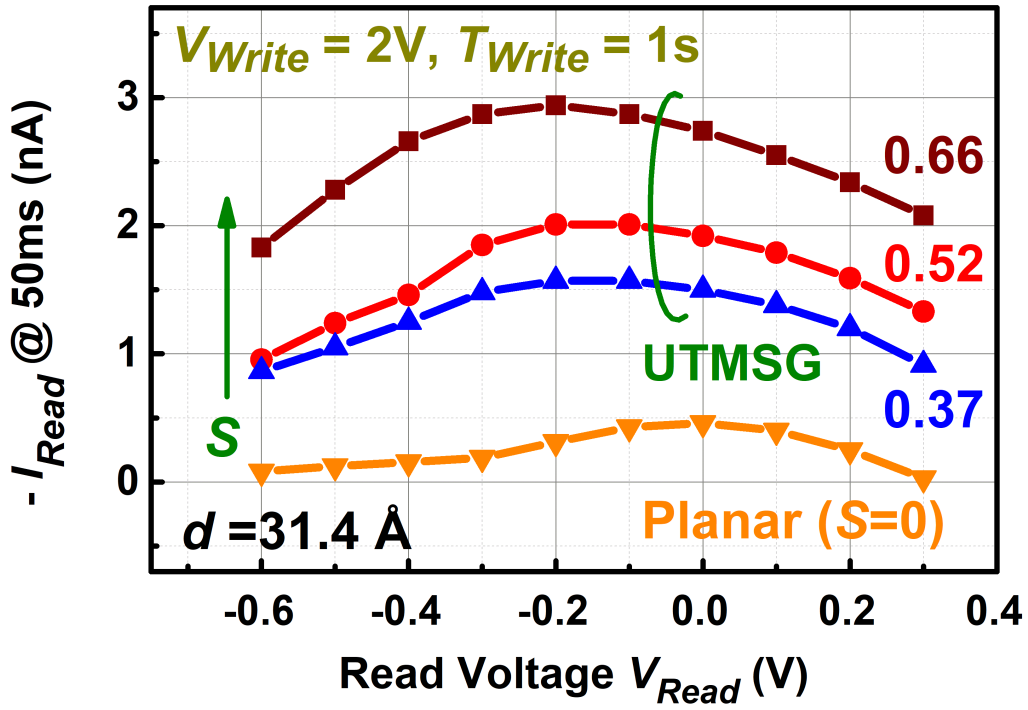

Figure 4–4. The magnitude of I_{Read} at 50 ms under different read voltage V_{Read}, showing a peak at V_{Read} = -0.2 V for the UTMSG devices.

compared to both the center gate and the top gate of the Planar device under the identical voltage program. This slower potential change prolongs the time required for the excess electrons under the surrounding gate to discharge, manifesting the edge late response effect. Hence, the magnitude of I_{Read} for the UTMSG device is enhanced.

Moreover, the larger S in UTMSG devices means more excess electrons are delayed in discharging, naturally leading to a higher I_{Read} magnitude for devices with a larger S. The optimal V_{Read} of -0.2 V is also consistent with this mechanism. At -0.2 V, the MIS system studied in this dissertation starts to enter into the weak inversion regime, whereby the discharge of excess electrons during the transient state is maximized upon switching the gate voltage to -0.2 V.

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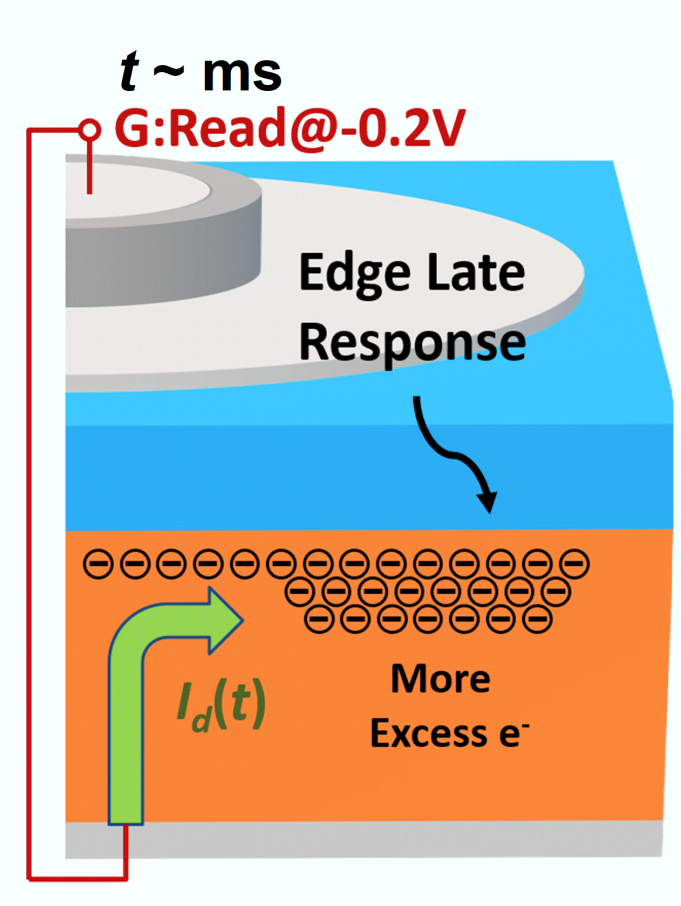

Figure 4–5. Schematic illustrating the edge late response effect which corresponds to the enhancement of the transient current for the UTMSG device.

4.4 Improved Transient Capacitance of The UTMSG MISTD

Beyond the enhanced transient current performance of the UTMSG device, we have also identified an improvement in its transient capacitance behavior, making it a promising candidate for dynamic memory applications. This improvement is rooted in the device's unconventional capacitance-voltage ($C-V$) characteristics, which are elucidated through a small-signal model proposed in **Section 4.4.1**. The subsequent analysis, detailed in **Section 4.4.2**, will explore the enlarged transient capacitance window and the influence

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of proportion of the surrounding gate S on this phenomenon.

4.4.1 Capacitance-Voltage Characteristics

The UTMSG device demonstrates unconventional capacitance-voltage ($C-V$) characteristics, distinguished by a $C-V$ curve that adopts a reverse-bell shape, which has never been discovered before. **Figure 4–6** (a) presents the $C-V$ behavior of UTMSG devices with varying S values in comparison to the Planar device, with **Figure 4–6** (b) providing a detailed view of these curves in the depletion and inversion regimes. Despite the identical total gate area of both UTMSG and Planar devices, their capacitance significantly diverges in the accumulation regime. A thorough investigation, as discussed in [85], reveals that in the accumulation regime (V_G < -1 V), the capacitance ratio between UTMSG and Planar devices closely mirrors the area proportion of the center gate, which, based on the earlier definition, equals 1 - S. This indicates that during the accumulation regime, only the carriers beneath the center gate are reactive to the AC signal. This observation extends into the depletion regime (-1 V < V_G < -0.2 V), as highlighted in **Figure 4–6** (b). Nevertheless, as V_G rises above -0.2 V and until 0 V, the capacitance of the UTMSG device experiences an increase, culminating in the convergence of all $C-V$ curves in the strong inversion regime (V_G > 0 V). This observation suggests that the carriers located beneath the entire gate structure, encompassing both the center and the surrounding gates, are responsive to the AC signal in this specific regime. Such dynamics result in the distinctive reverse-bell shaped $C-V$ characteristics of the UTMSG device.

To elucidate the atypical capacitance-voltage ($C-V$) behavior observed, we introduce an AC small-signal model. This model is depicted in **Figure 4–7** , where R_{Al} represents the series resistance between the inner center gate and the outer surrounding gate, while R_{Si}

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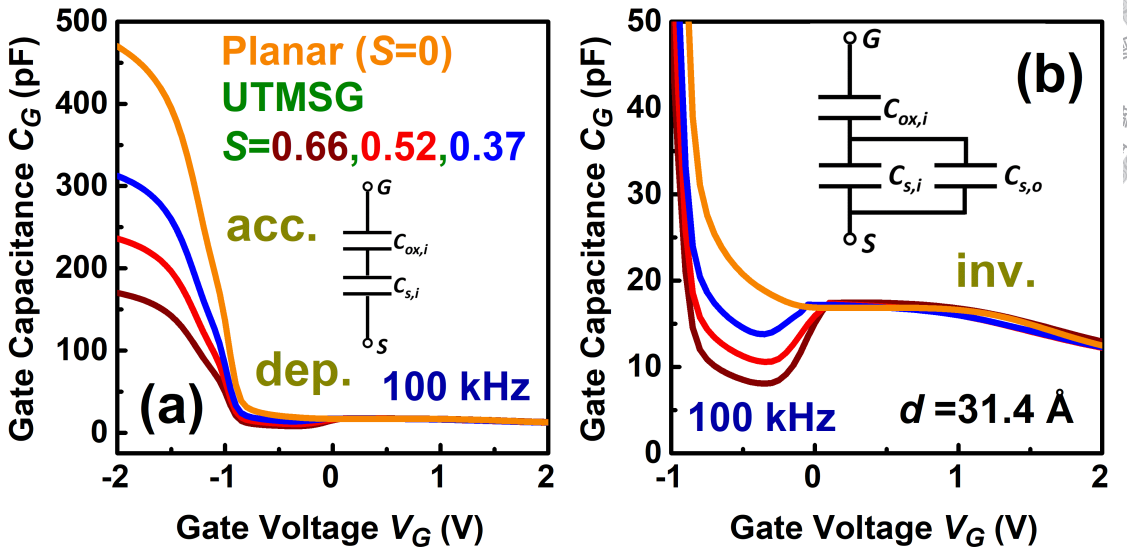

Figure 4–6. (a) 100 kHz capacitance-voltage ($C-V$) characteristics of the UTMSG devices with varying S compared with the Planar device. (b) Enlargement of (a) in the depletion and inversion regimes. Inset of (a): Simplified AC model in the accumulation and the depletion regimes. Inset of (b): Simplified AC model in the inversion regime.

represents the series resistance of the inversion channel near the silicon surface connecting the inversion layers beneath the center and surrounding gates. The terms $C_{ox/s,i/o}$ represent the capacitance of the oxide/semiconductor under the inner/outer gate. It is posited that R_{Al} exhibits such a high resistance that it effectively impedes the AC small signal from traversing this branch of the circuit. Consequently, during the accumulation and depletion regimes, only carriers beneath the center gate are reactive to the AC signal. This is attributable to the absence of an inversion layer near the silicon surface, rendering R_{Si} too large for the AC signal to pass through. This simplifies the small-signal circuit to resemble the inset shown in **Figure 4–6** (a). Hence, the capacitance value closely aligns with 1 - S, decreasing as S increases. Nonetheless, in the strong inversion regime, an inversion channel forms near the silicon surface, drastically reducing R_{Si} to the point where it can be considered a short circuit. This alteration simplifies the small-signal circuit to

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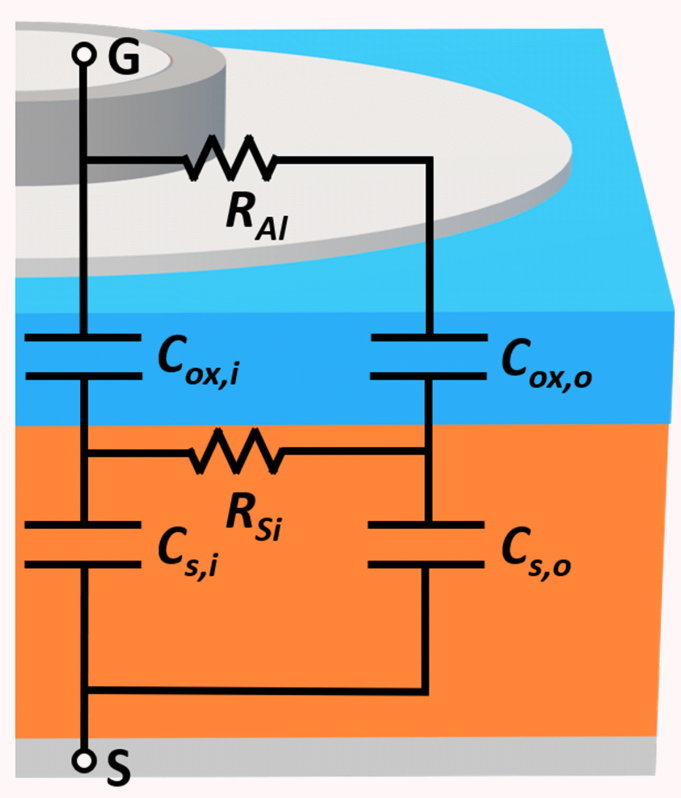

Figure 4–7. The detailed small-signal AC model proposed to explain the atypical $C-V$ characteristics for the UTMSG device.

that illustrated in the inset of **Figure 4–6** (b). Therefore, the capacitance in the inversion regime, primarily influenced by the silicon capacitance across the entire gate due to the ultra-thin oxide layer, aligns for both Planar and UTMSG devices and remains unaffected by variations in S.

The validity of the proposed AC small-signal model is further substantiated by examining the capacitance-voltage ($C-V$) curves at varying frequencies, as illustrated in **Figure 4–8**. Notably, the gate voltage at which the capacitance begins to increase, marking the transition from the depletion to the inversion regimes, typically spanning from -0.5 to 0 V, shifts towards more negative values at lower AC frequencies. This increase in capacitance occurs when R_{Si} decreases sufficiently, allowing the AC signal to pass through.

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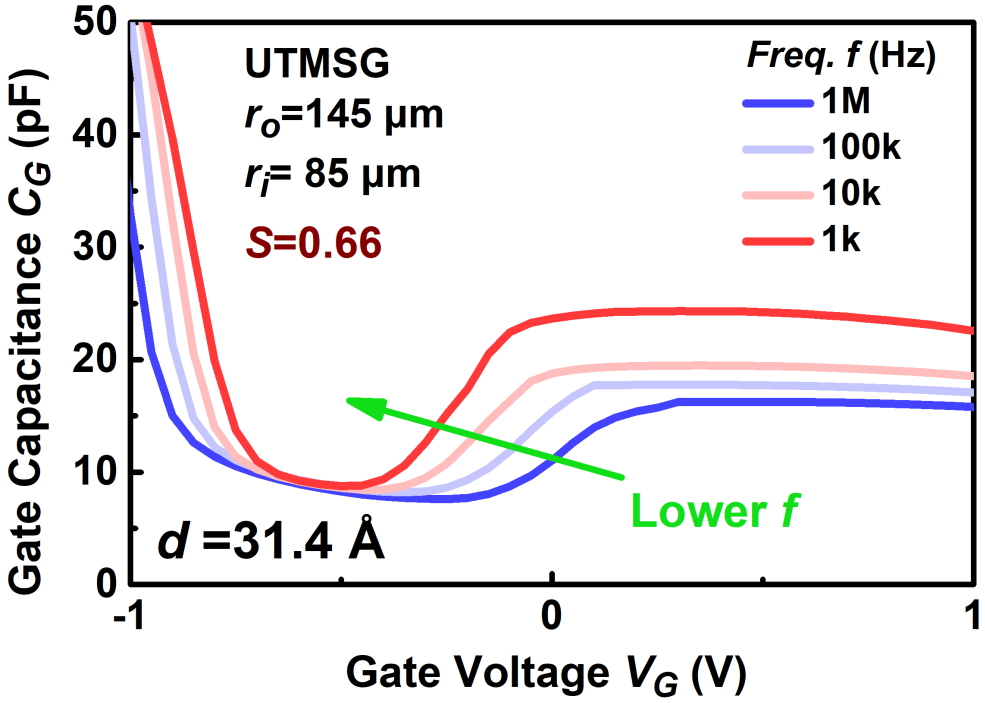

Figure 4–8. The $C - V$ characteristics in the depletion and inversion regimes for the UTMSG device with $S = 0.66$ with various frequencies. The $C - V$ curve with a lower frequency turns up at a lower gate voltage.

Given that the $R_{Si} - C_{s,o}$ branch effectively acts as a low-pass R-C filter, its cutoff frequency is inversely proportional to the product $R_{Si}C_{s,o}$. Consequently, under identical gate voltage conditions, where the inversion channel remains constant and thus R_{Si} retains a fixed value, the AC signal with a lower frequency more readily traverses this circuit branch. In essence, this suggests that the inversion channel requires fewer carriers to facilitate the passage of a lower-frequency AC signal. As a direct outcome, the corresponding $C - V$ curve exhibits an upward turn at an earlier gate voltage, or at a more negative gate voltage.

4.4.2 Transient Capacitance

The distinctive capacitance behavior depicted in **Figure 4–6** showcases that exploiting the reverse-bell shape of the $C - V$ curve enables the attainment of a broader transient

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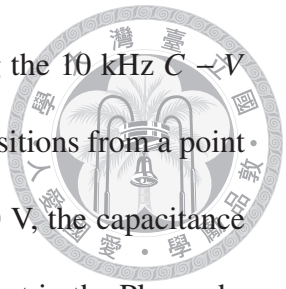

capacitance window [124]. This concept is exemplified by analyzing the 10 kHz $C-V$ characteristics featured in **Figure 4–9** (a). When the gate voltage transitions from a point within the valley of the depletion regime to the inversion regime at 0 V, the capacitance change observed in the UTMSG device is significantly greater than that in the Planar device. This variation amplifies with an increase in the surrounding gate proportion, S.

For applications in dynamic memory, pulses of +0.5 V and -0.5 V with a duration of 1 s are applied to the gate, followed by the measurement of transient capacitance at a constant read voltage V_{Read} = 0 V. The observed transient capacitance is presented in **Figure 4–9** (b), where open and solid symbols represent the transient capacitance values when the gate voltage is switched to 0 V from +0.5 V and -0.5 V, respectively. It is evident from these results that all UTMSG devices feature larger capacitance windows in comparison to the Planar device, highlighting the potential of UTMSG structures in enhancing dynamic memory performance through optimized capacitance behavior.

The mechanisms underlying the enhanced transient capacitance are elucidated as follows. Upon transitioning the gate voltage from -0.5 V to 0 V, the inversion charges are initially unable to get fully generated. To compensate for the gate bias, the voltage consequently drops across the silicon, inducing deep depletion and resulting in a decreased capacitance. Given that the steady-state capacitance at -0.5 V is inherently lower for the UTMSG device with a higher S, a more pronounced change in capacitance is observed during this transition.

Conversely, when the gate voltage shifts from +0.5 V to 0 V, the electrons accumulated beneath the gate cannot be instantaneously discharged. This delay limits the potential drop across the silicon, leading to a reduction in the depletion region and, hence, an increase in

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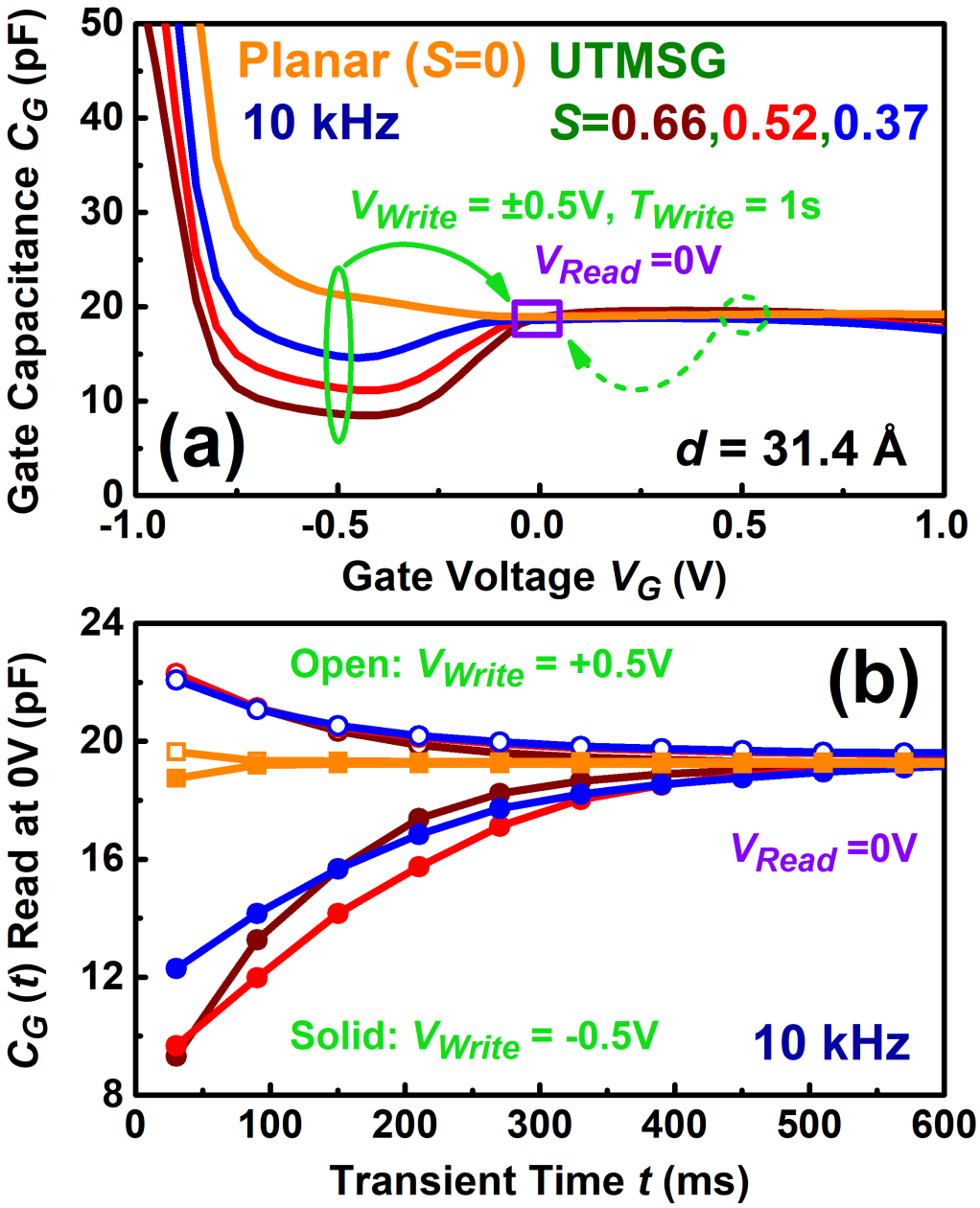

Figure 4–9. (a) 10 kHz $C - V$ characteristics of the UTMSG devices with various S along with the Planar device. (b) Transient capacitance behavior for the UTMSG and Planar devices, with the write voltage of +0.5 V (open symbol) and -0.5 V (solid symbol).

capacitance. For the UTMSG devices, this reduction in the depletion region is significantly more pronounced due to the prolonged discharge time of excess electrons, attributable to the edge late response effect. Consequently, UTMSG devices exhibit a more substantial

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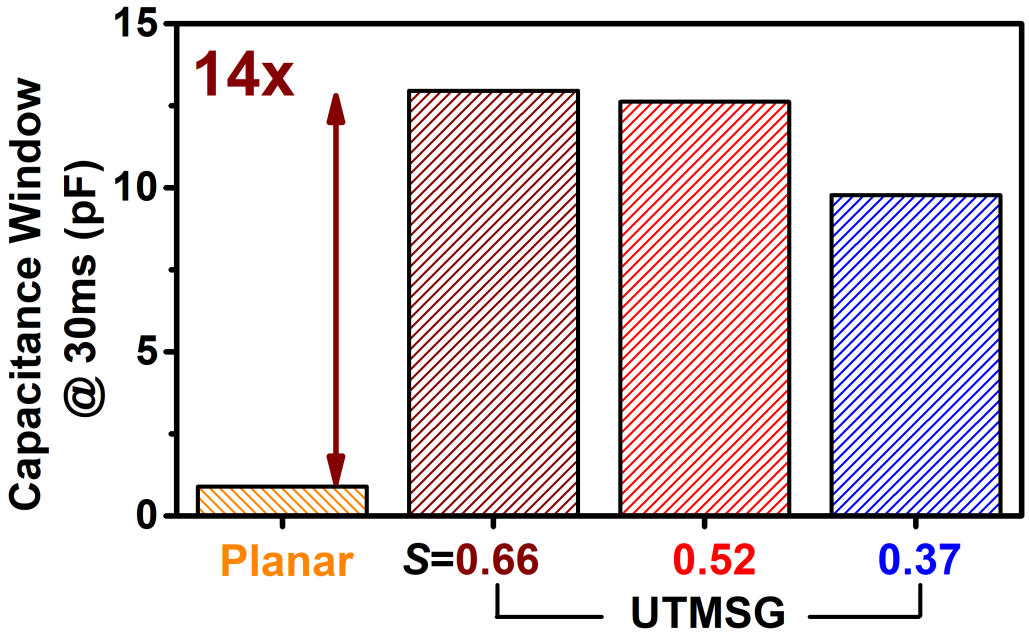

Figure 4–10. The capacitance window extracted at 30 ms for the UTMSG and Planar devices. 14 times improvement can be achieved for the UTMSG device with S = 0.66 compared with the Planar one.

change in capacitance under these voltage transitions of opposite polarities. This effect is particularly notable when switching from -0.5 V to 0 V, leveraging the unique reverse-bell-shaped $C - V$ characteristics for enhanced performance.

Consequently, the capacitance windows corresponding to the two states, measured at 30 ms, are delineated in **Figure 4–10**. There is a clear correlation between the size of the capacitance window and the proportion of the surrounding gate, S; a larger S yields a larger capacitance window. This trend mirrors that observed in the transient current behavior. Notably, for the UTMSG device with an S value of 0.66, the enhancement in the transient capacitance window is substantial, reaching up to 14 times that of the Planar device.

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4.5 Summary

In summary, this chapter has rigorously examined the enhanced transient behavior of the Ultra-Thin Metal Surround Gate (UTMSG) MISTD, highlighting significant advancements in both transient current and capacitance characteristics that hold promising implications for dynamic memory applications. Through meticulous experimentation and analysis, we have delineated the superior performance of UTMSG devices over conventional Planar structures, attributing these improvements to the unique design and operational mechanisms of the UTMSG architecture.

The investigations commenced with an exploration of the transient current behavior, where UTMSG devices demonstrated a remarkable increase in the magnitude of read current (I_{Read}) at 50 ms post a 2 V write pulse for 1 s. This enhanced performance was attributed to the edge late response effect, facilitated by the resistive ultra-thin metal layer and the insulating aluminum oxide layer that introduce an R-C time delay, thereby extending the discharge time for excess electrons. Notably, the magnitude of I_{Read} was observed to increase with the proportion of the surrounding gate (S), with an S value of 0.66 enabling a 9 times improvement in I_{Read} at the read voltage V_{Read} of -0.2 V compared to the Planar device. The magnitude of I_{Read} measured at 50 ms with V_{Read} set to 0 V reaches 2.7 nA, marking a substantial improvement, approximately 4.5 times greater than the best performance observed in the Planar device.

Furthermore, the chapter explored the unconventional capacitance-voltage ($C-V$) characteristics of UTMSG devices, characterized by a reverse-bell shape that has not been previously reported. This atypical behavior was leveraged to achieve a larger transient capacitance window, essential for the efficacy of dynamic memory systems. The capacitance

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window's expansion was directly correlated with S, underscoring the pivotal role of the surrounding gate's proportion in enhancing device performance. In particular, a UTMSG device with an S of 0.66 exhibited a 14 times increase in the transient capacitance window relative to its Planar counterpart.

The unconventional $C-V$ behavior and the enhanced transient capacitance behaviors were further elucidated through a proposed AC small-signal model, which accounted for the observed phenomena by considering the impact of the resistive ultra-thin metal layer on the device's response to the AC small signal. This model provided a robust theoretical framework for understanding the UTMSG device's operational dynamics, particularly in the accumulation, depletion, and inversion regimes.

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5

Enhancement of Transient Current Window in The Oxide Local Thinning MISTD via Dielectric Soft Breakdown

5.1 Introduction

In the realm of contemporary integrated circuit design, the phenomenon of dielectric breakdown takes on critical importance, a situation exacerbated by the ongoing trend of minimizing the dimensions of components, particularly the gate oxide layer. This reduction in thickness subjects the gate oxide to enhanced electric fields and elevates tunnel-

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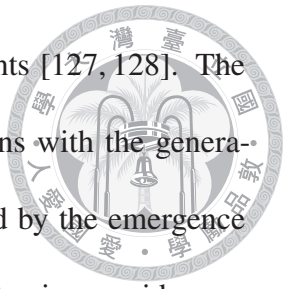

ing currents, significantly raising the potential for breakdown incidents [127, 128]. The process of oxide breakdown unfolds in three distinct stages: it begins with the generation of traps within the oxide due to electrical stress; this is followed by the emergence of a conductive pathway within the dielectric material; and culminates in a rapid surge in current through this pathway, which can lead to additional thermal damage [129, 130]. Oxide breakdown is classified into two major categories according to the severity of the oxide damage: hard breakdown (HBD) is characterized by a significant increase in leakage current, effectively breaking the oxide's dielectric capabilities; on the other hand, soft breakdown (SBD) results in a comparatively modest rise in leakage current, allowing the affected device to remain operational across a wide range of circuits [131]. The discourse surrounding SBD at the dawn of the 21st century largely revolved around understanding its underlying physical mechanisms [132, 133], developing models for the post-breakdown current flow [134, 135], and analyzing breakdown statistics [136, 137]. While initially framed as a matter of reliability, subsequent research has illuminated potential applications for oxide SBD in various domains, including as a component in random number generators [138, 139], as a basis for physically unclonable functions (PUF) [140, 141], and in memory cell technology [142].

This study deliberately triggers SBD in MISTD devices to significantly extend the transient current window, a crucial attribute for dynamic memory applications. Post-SBD, the enhancement of the current window can span up to two magnitudes. The specific MIS structure engaged in this research is illustrated in **Figure 5–1** (a). Initially, this structure exhibits a uniform oxide layer with sparse traps, denoted as a 'Fresh' MIS in **Figure 5–1** (b). The application of constant voltage deep depletion stress (DDS) pro-

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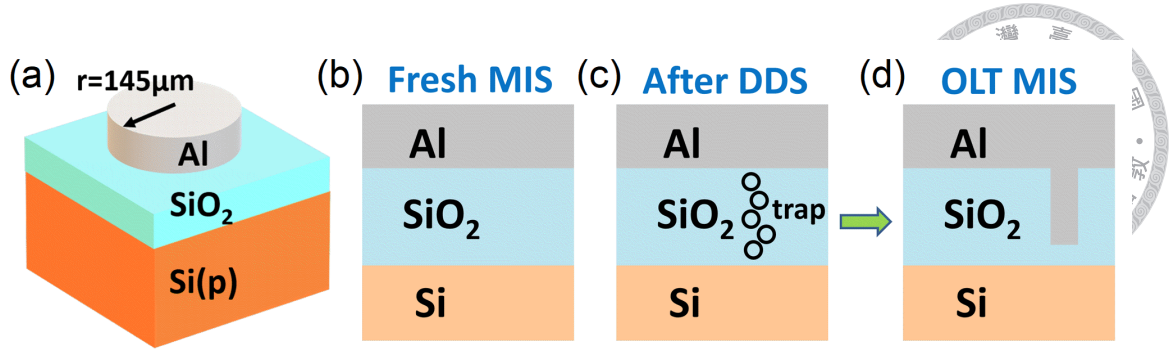

Figure 5–1. Schematics of (a) the MISTD, cross sections of (b) Fresh MIS, (c) MIS with traps generated inside oxide after performing DDS to induce dielectric soft breakdown (SBD) and (d) the conceptualized OLT MISTD.

vokes the generation of bulk traps, pushing the silicon into the deep depletion regime under voltage stress and leading to the establishment of a percolation pathway, as detailed in **Figure 5–1** (c). The potential for damage induced by leakage current through this pathway under DDS is minimized due to the light doping of the silicon (1-10 Ω-cm) and the limitation of current by the substrate in the deep depletion regime [143–145]. The occurrence of SBD in DDS under these conditions of low current compliance is documented [146, 147]. Following SBD, for the sake of simplicity, the MIS can be conceptualized as having undergone oxide local thinning (OLT), as depicted in **Figure 5–1** (d). This simplification is due to the highly localized nature of the main tunneling current post-SBD [148–152]. OLT MIS showcases an enhanced transient current window when subjected to pulsed voltage write programs, as demonstrated in the following sections.

5.2 Enhanced Transient Current of The OLT MISTD

5.2.1 Experimental Results

The manufacturing methodology for the Fresh MMISTD mirrored that of the Planar MISTD outlined in **Chapter 2**, with a particular emphasis on maintaining the oxide thickness of

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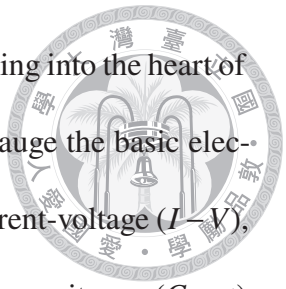

the Fresh MIS devices at approximately 30 Å in this study. Before delving into the heart of the experimental procedure, initial measurement were conducted to gauge the basic electrical characteristics of these devices. This included evaluations of current-voltage ($I-V$), capacitance-voltage ($C-V$), transient current ($I-t$), and transient capacitance ($C-t$) profiles. Following this foundational analysis, the devices were subjected to DDS under a constant voltage of 5 V. This stress was sustained until breakdown was reached.

A pivotal outcome of the DDS was the establishment of a conducting percolation path through the oxide layer. This path facilitated a significant surge in the tunneling current, which became highly concentrated along this newly formed percolation path. Consequently, for the sake of analytical simplicity, the post-DDS device could be effectively conceptualized as an OLT MIS, as depicted in **Figure 5–1** (d). It is imperative to underscore the role of deep depletion as a pivotal stress condition in this context. This specification is crucial as it biases the silicon into the deep depletion regime during the application of stress, thereby precluding the occurrence of HBD and paving the way exclusively for SBD. For the p-type silicon substrate we used in this work, it required a large positive stress. In contrast, it was demonstrated in [50] that for the same MIS system, HBD instead of SBD would happen under a large negative voltage stress.

The formation of OLT in the MIS structure, featuring a fresh oxide layer with a thickness of d = 31.1 Å and subjected to a 5 V DDS, is detailed in **Figure 5–2** (a). This procedure notably leads to a sudden decrease in the current level, serving as a hallmark of SBD. Comparative analyses of the $I-V$ and $C-V$ properties for both the Fresh and the OLT MIS devices are illustrated in **Figure 5–2** (b) and (c). It is noticed that the electrical characteristics of the Fresh and OLT device correspond to the same device before and after

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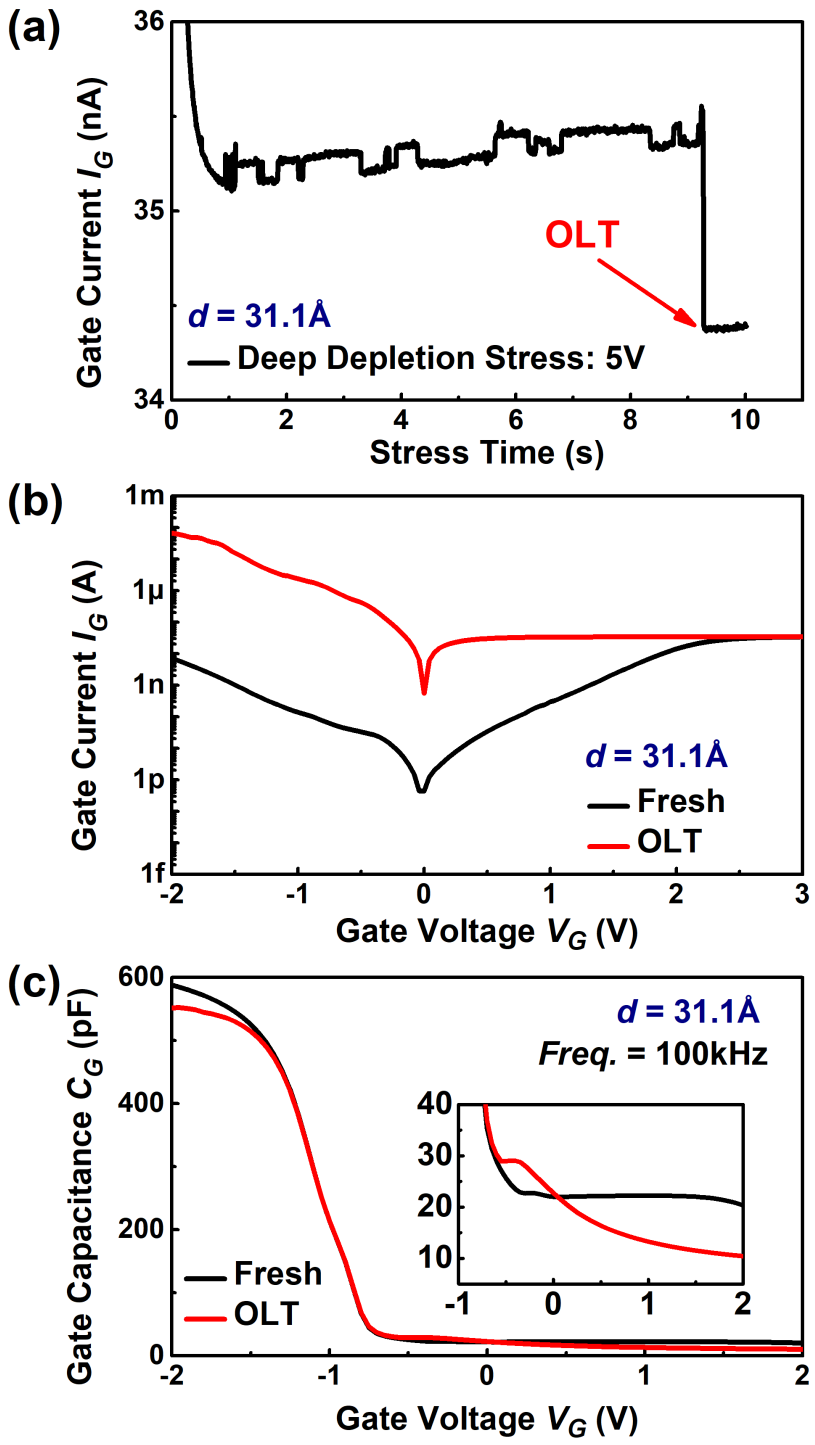

Figure 5–2. (a) The current-time characteristics for the MIS device under DDS with a constant voltage of 5 V. The forming of OLT is marked as the sudden drop in the current. (b) $I-V$ and (c) $C-V$ characteristics of the Fresh and OLT MIS device. Inset of (c): Enlargement of the $C-V$ curves in the deep depletion regime.

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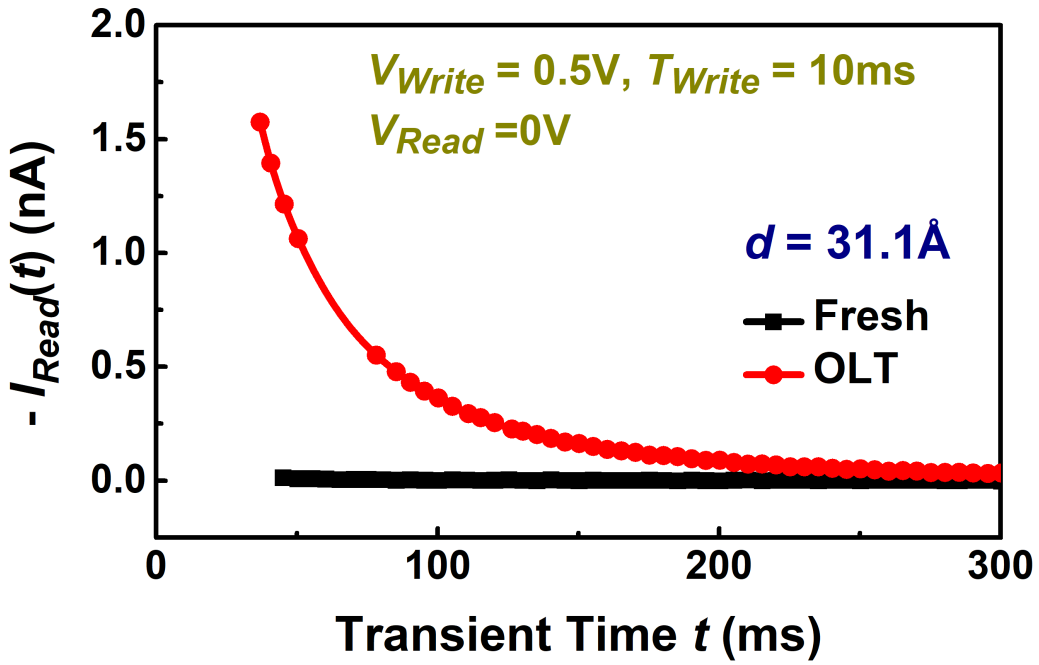

Figure 5–3. Transient current behavior of the Fresh and OLT MIS with V_{Write} = 0.5 V, T_{Write} = 10 ms, and V_{Read} = 0 V.

SBD, respectively. Specifically, in the forward bias regime under a negative bias, there is a significant elevation in the tunneling current over several orders of magnitude. On the other hand, the saturation current in the reverse bias regime under a positive bias remains almost the same, indicating that the breakdown under DDS is self-protective and the damage of oxide is not catastrophic [18, 50]. Additionally, the onset of current saturation occurs at a considerably lower voltage in OLT MIS device compared to the Fresh device. This can be attributed to the facilitated tunneling of inversion electrons through the OLT regions, a behavior that can be further evidenced by the deep depletion phenomenon observed in the $C - V$ curves of OLT MIS [96, 153]. Consequently, the introduction of an OLT spot is shown to have a profound impact on the overall performance and electrical characteristics of the MIS device. It is also noted that a hump can be observed in the $C - V$ curve of the OLT device for V_G between -0.5 to 0 V. This is attributed to the strong tun-

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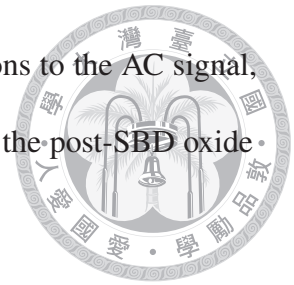
neling through the oxide, leading to the response of inversion electrons to the AC signal, which was discussed in detail in [154–157], which also suggests that the post-SBD oxide becomes much more leaky.



To examine the transient response, a voltage pulsed program with V_{Write} = 0.5 V and T_{Write} = 10 ms, followed by a V_{Read} = 0 V to read the current, is executed. The observed transient current behavior is depicted in **Figure 5–3**. The magnitude of I_{Read} at 50 ms are 8 pA and 1.07 nA for Fresh and OLT MIS, respectively, marking an enhancement exceeding two orders of magnitude. Notably, the magnitude of I_{Read} of 1.07 nA for the OLT MIS also represents a 10 times improvement over the highest recorded I_{Read} of approximately 100 pA for the best Planar device with T_{Write} of 10 ms. This substantial increase underscores the potential of OLT MIS to broaden the current window, making it a viable option for dynamic memory applications.

In practice, applying a 0 V and a 0.5 V pulse to write on the OLT MIS results in the readout of zero current and a negative current of enhanced magnitude, respectively, as showcased in **Figure 5–4** (a). These outcomes correspond to the binary states '0' and '1' in dynamic memory. Following this, an endurance test is carried out, with the results presented in **Figure 5–4** (b). The binary current states demonstrate stability over 10^5 cycles, with observed degradation beyond this point likely linked to the inherent instability associated with SBD [158–160]. As such, it is recommended that future efforts focus on developing a targeted pattern for OLT region formation to further augment the endurance of the system [49].

To address concerns related to power consumption and operational speed, the transient current behavior and endurance of the devices are initially tested using a relatively

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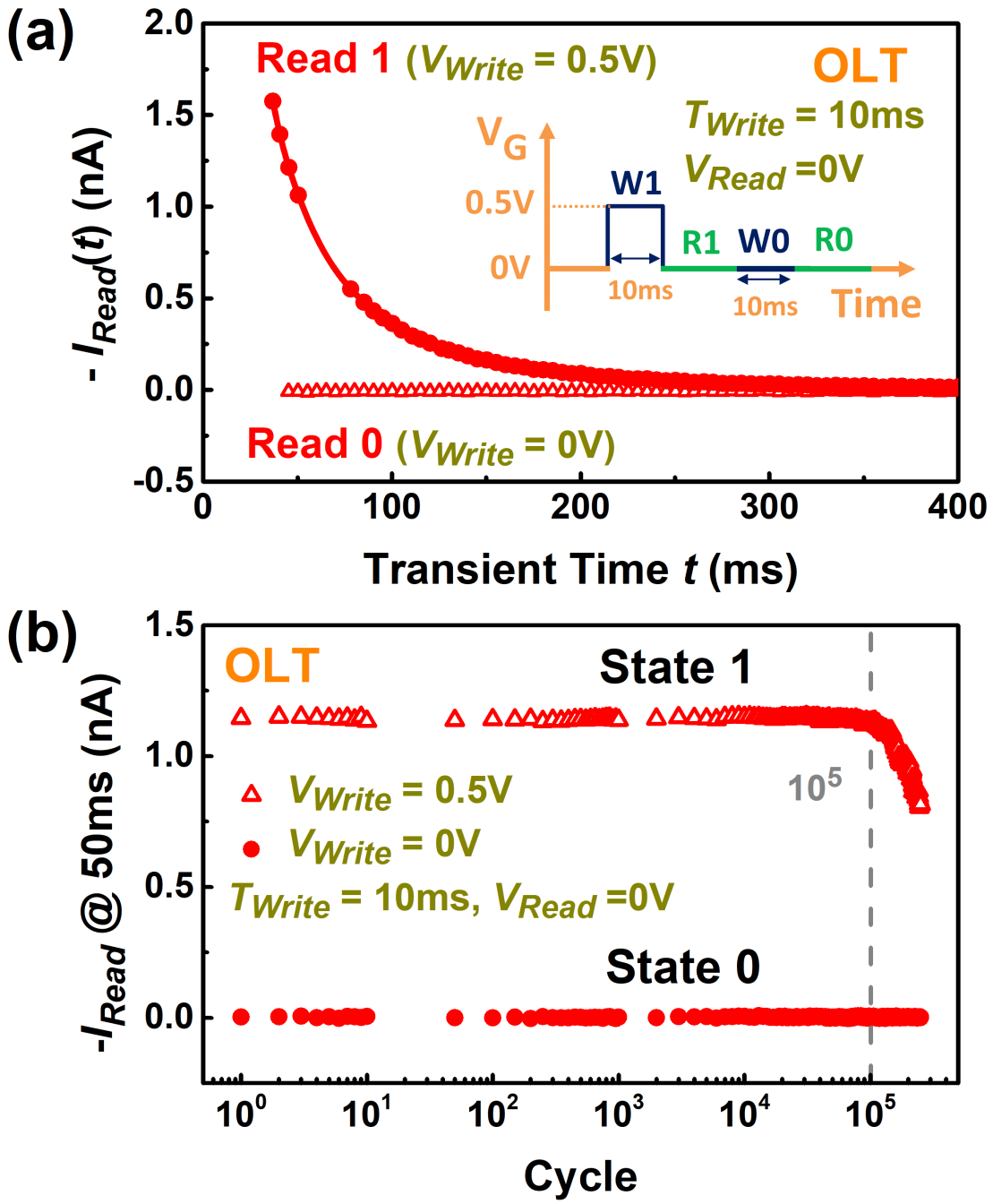

Figure 5–4. (a) Transient current behavior of the OLT MIS for State '0' and '1' with V_{Write} of 0 and 0.5 V, respectively. Inset: Illustration of the voltage program. (b) Endurance test of the two current states of the OLT MIS.

low write voltage of 0.5 V and a short write time of 10 ms. To further explore the capabilities of the OLT MIS devices, we increase both V_{Write} and T_{Write} to ascertain the maximum

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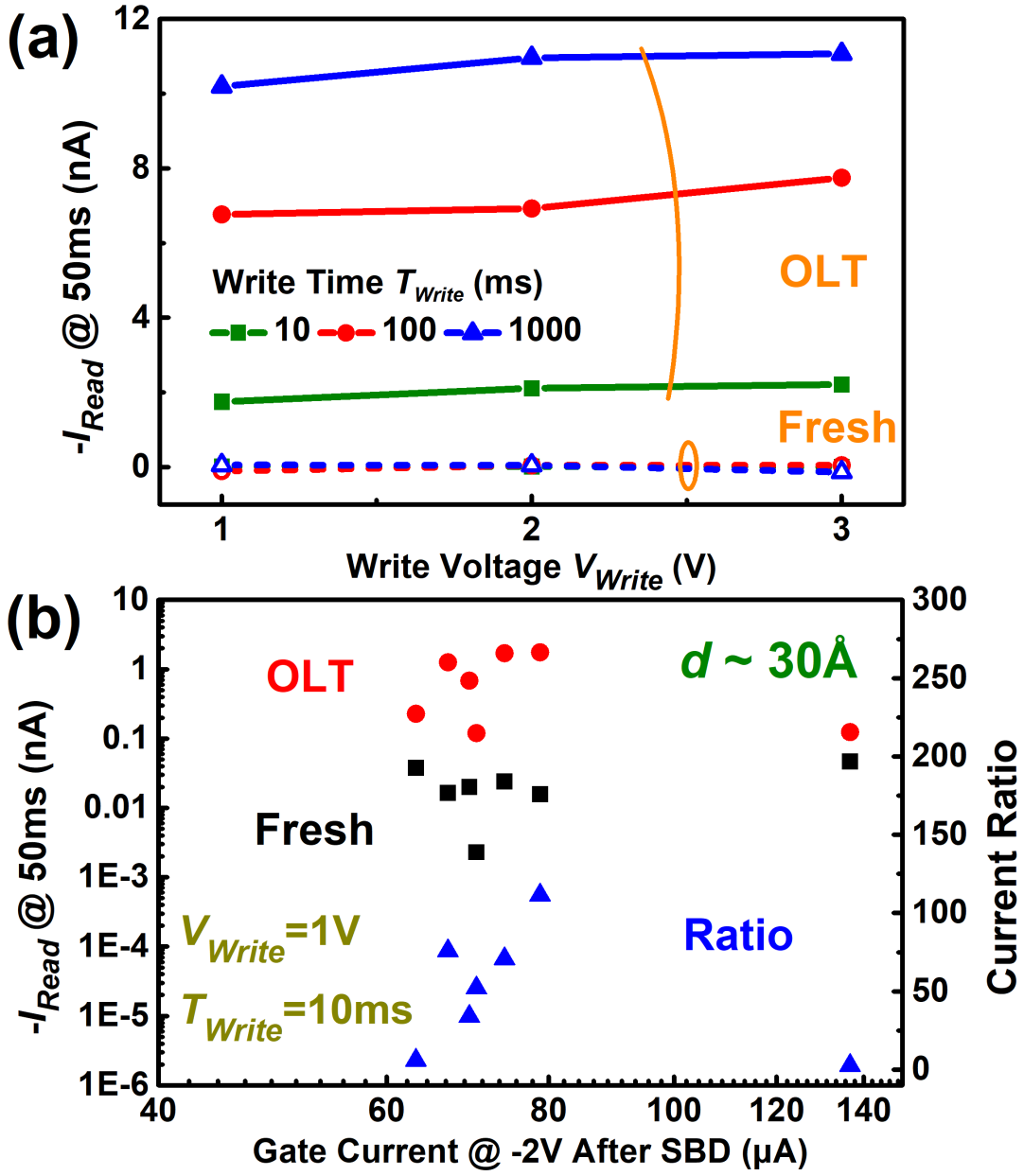

Figure 5–5. (a) The magnitude of I_{Read} at 50 ms for the Fresh and OLT device under various V_{Write} and T_{Write}. The peak I_{Read} exceeds 10 nA for T_{Write} of 1000 ms. (b) The magnitude of I_{Read} at 50 ms with V_{Write} = 1 V and T_{Write} = 10 ms for several MIS devices before and after SBD, marked as Fresh and OLT, respectively, with the current ratio also displayed.

achievable I_{Read} magnitude. The outcomes of these tests are illustrated in **Figure 5–5** (a), showcasing V_{Write} values extending from 1 to 3 V and T_{Write} durations spanning from 10

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to 1000 ms. It was observed that the magnitude of I_{Read} begins to saturate once V_{Write} surpasses 1 V, registering only marginal increases beyond this point. Conversely, the magnitude of I_{Read} exhibits substantial growth as T_{Write} is extended. Specifically, the peak $|I_{Read}|$ at 50 ms reaches beyond 2 nA for a T_{Write} of 10 ms, achieving a 20 times enhancement over the best planar device under identical conditions (100 pA). Furthermore, $|I_{Read}|$ surpasses 10 nA for T_{Write} of 1000 ms, marking a 16 times increase compared to the best planar scenario (600 pA) under identical test parameters.

5.2.2 Discussions

In the preceding section, we highlight the enhanced transient current window of the OLT MIS device. Now, we aim to delve into the underlying mechanism through the lens of transient capacitance analysis. **Figure 5−6** illustrates the change of capacitance relative to the steady-state capacitance at 0 V, specifically, $C_{Read}(t) - C_{Read}(t = \infty)$, with the original measured data presented in the inset. Notably, the capacitance change in the OLT MIS device is not just quantitatively larger but also exhibits an opposite sign when compared to that of the Fresh MIS device. This suggests a fundamental difference in carrier movement within the device.

Revisiting the transient capacitance behavior of Fresh MIS, paralleling the discussion on the UTMSG device in **Chapter 4**, adds depth to our understanding. The observed decrease in transient capacitance for the Fresh MIS, upon shifting from a positive gate voltage to 0 V, can be elucidated as follows: During the application of a positive write pulse, electrons accumulate at the silicon surface. Once the gate voltage reverts to 0 V, the excess of electrons remains, exceeding the equilibrium quantity for the 0 V steady state.

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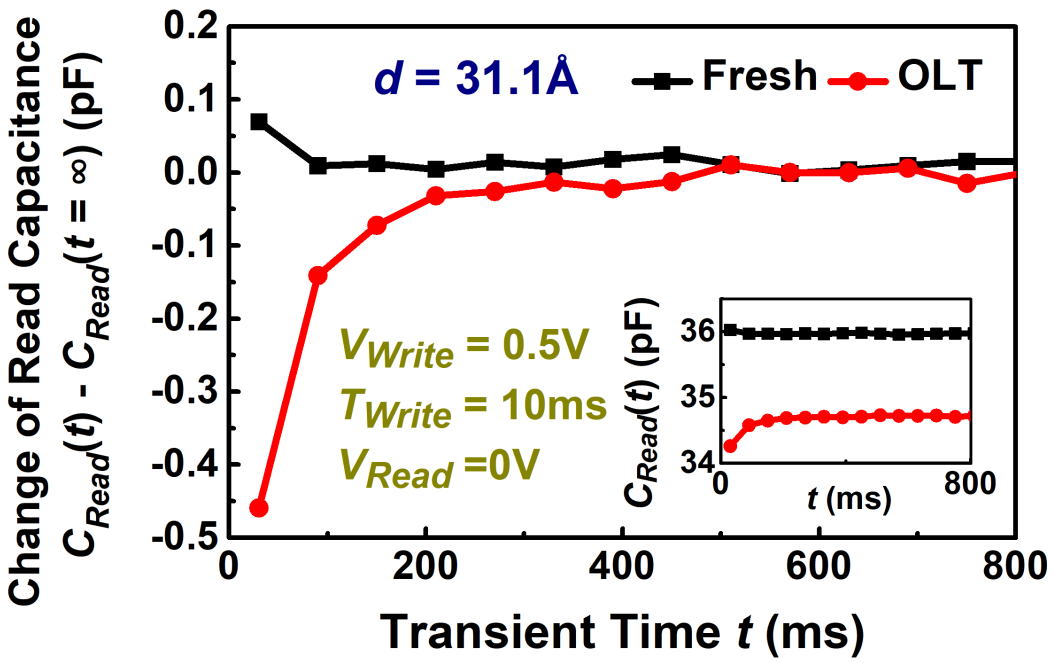

Figure 5–6. The change of transient capacitance with respect to the steady state condition. Inset: Measured transient capacitance characteristics.

Following the voltage balance equation,

$$V_G - V_{Fb} = -\frac{Q_s}{C_{ox}} + \psi_s \tag{5.1}$$

the surface potential (ψ_s) decreases after the dielectric relaxation time, leading to a shrinkage of the depletion region. As these excess electrons progressively discharge, ψ_s increases, and the depletion region expands accordingly, leading to a decreasing transient capacitance trend for the Fresh MIS.

Contrary to the Fresh MIS, the OLT MIS exhibits an increasing transient capacitance during the read procedure, implying a decrease of the depletion width on millisecond timescales. This suggests a higher ψ_s compared to the steady-state scenario. According to the voltage balance equation (5.1), this condition indicates a reduced presence of inversion

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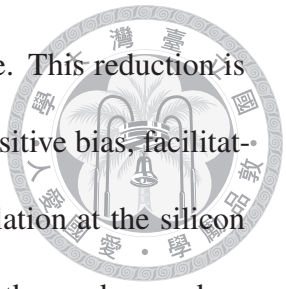

electrons in the silicon during the transient relative to the steady state. This reduction is attributed to the high tunneling rate through the OLT region under positive bias, facilitating electron passage through the OLT spot rather than their accumulation at the silicon surface during the write process. Consequently, the transient during the read procedure starts with fewer electrons than in the steady state.

Additionally, for an MIS device with an oxide thickness of 30 Å, positive oxide charges outside the gate induce inversion charges underneath, maintaining charge neutrality at the steady state, as depicted in **Figure 5–7** (a). However, these inversion charges are also drained to the gate due to the significant tunneling rate through the OLT spot, as shown in subfigure (b). This leads to an electron deficiency both under and outside the gate area, contrasting sharply with the Fresh MIS scenario. During the read process, electrons tunnel from the gate through the OLT spot into the silicon, compensating for the deficiency and resulting in a significant negative gate transient current, illustrated in subfigure (c).

This mechanism can also be interpreted from an alternative perspective. The band diagrams along the OLT spot at 0 V steady state, and during the write and read processes, are schematically illustrated in **Figure 5–7** (d)-(f). The notable electron deficiency at the silicon surface lowers the electron quasi Fermi level (E_{Fn}) below the gate Fermi level (E_{Fm}). Hence, during the read transient, electrons naturally flow from the gate to the silicon via the OLT spot, aiding the device's return to steady state. However, the electron supply through the OLT spot during the read procedure is limited by an extreme funneling effect within a highly localized area of tens of nm^2 [160], [150], prolonging the recovery of the OLT MIS to steady state compared to the Fresh MIS. Moreover, as electrons must laterally flow within the inversion layer to address the deficiency under and outside the

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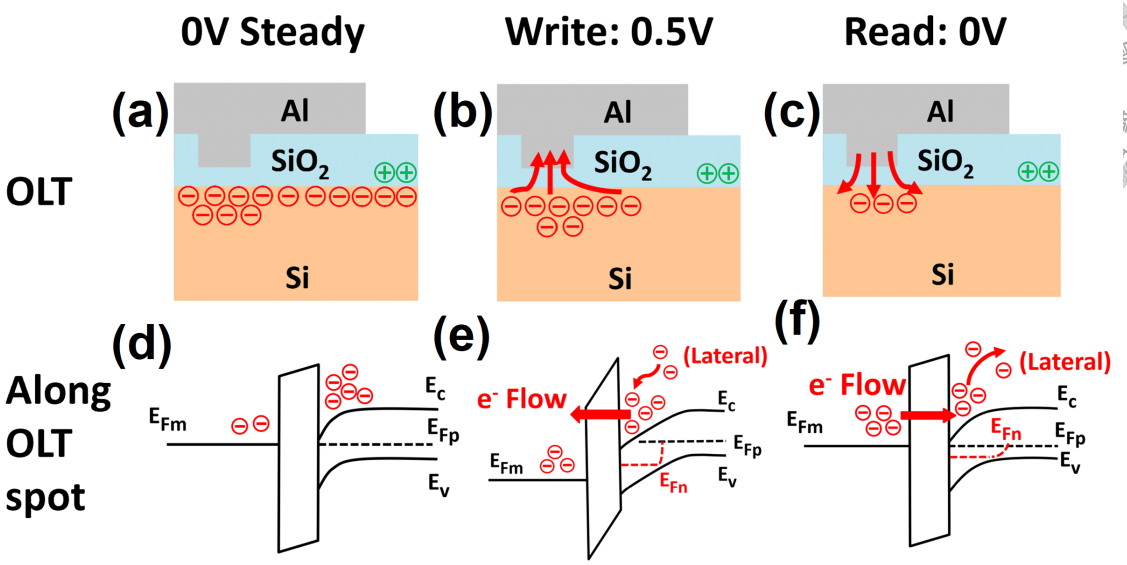

Figure 5–7. (a)-(c) Schematics cross sections of the OLT MIS device and (d)-(f) band diagrams across the OLT spot at 0 V steady state, during the write and read procedure, respectively.

gate, the OLT MIS experiences a delayed return to the steady state, further enhancing its transient behavior.

In summary, the contrast in the sign of the transient capacitance change observed in the OLT MIS device, compared to the Fresh device, highlights a fundamental shift in the nature of the transient current. This shift underscores that the transient current in OLT MIS is primarily driven by the tunneling current through the OLT spot, rather than the displacement current in the Fresh device. Furthermore, the significant electron deficiency both under and outside the gate in OLT MIS necessitates a substantial influx of tunneling electrons, leading to the enhanced transient current behavior of the OLT MIS.

5.2.3 Simulation Results

To further study the enhanced transient current behavior of the OLT MIS device and validate the previously suggested mechanism, a 2-D cylindrical TCAD simulation was exe-

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cuted. The cross-sectional view of the OLT MIS device is depicted in **Figure 5−8** (a). In this setup, the oxide layer has a thickness of 3 nm, featuring an OLT spot centrally positioned, where the oxide thins down to 1 nm with a radius of 100 nm. The device maintains a gate radius of 145 μm, consistent with standard configurations, while the silicon substrate extends to a radius of 2000 nm. The Fresh MIS, serving as a comparative model, mirrors the structure of the OLT MIS but lacks the OLT spot. The simulation incorporates two distinct values of the number of oxide charges: 0 and 3.2×10^{11} cm^{-2}, to explore the impact of charge density on the transient electrical characteristics.

The simulation outcomes showcasing the $I-V$ characteristics are presented in **Figure 5−8** (b). For the Fresh devices, an increase in the oxide charges Q_{ox} results in a higher saturation current in the reverse bias regime, attributable to an additional supply of generation current outside the gate [39,95]. On the other hand, with the same Q_{ox} levels, both Fresh and OLT devices exhibit nearly equivalent saturation currents. Meanwhile, the current of the OLT device reaches saturation at a significantly reduced voltage, almost nearing 0 V. Additionally, in the forward bias regime, the current for the OLT MIS markedly surpasses that of the Fresh MIS. These findings align with experimental results in **Figure 5−2** , suggesting that the simplified OLT MIS structure model can successfully mimic the steady-state electrical behavior of the post-BD MIS device.

Following the steady-state simulations, transient currents transitioning from a V_{Write} = 0.5 V steady state to 0 V are also simulated, with results for millisecond time scales highlighted in **Figure 5−8** . For the Fresh MIS, an increase in the oxide charge Q_{ox} leads to a diminished magnitude of I_{Read}, which has been discussed in the end of **Chapter 2**. In the case of the OLT MIS without any oxide charges, the magnitude of I_{Read} is negligible,

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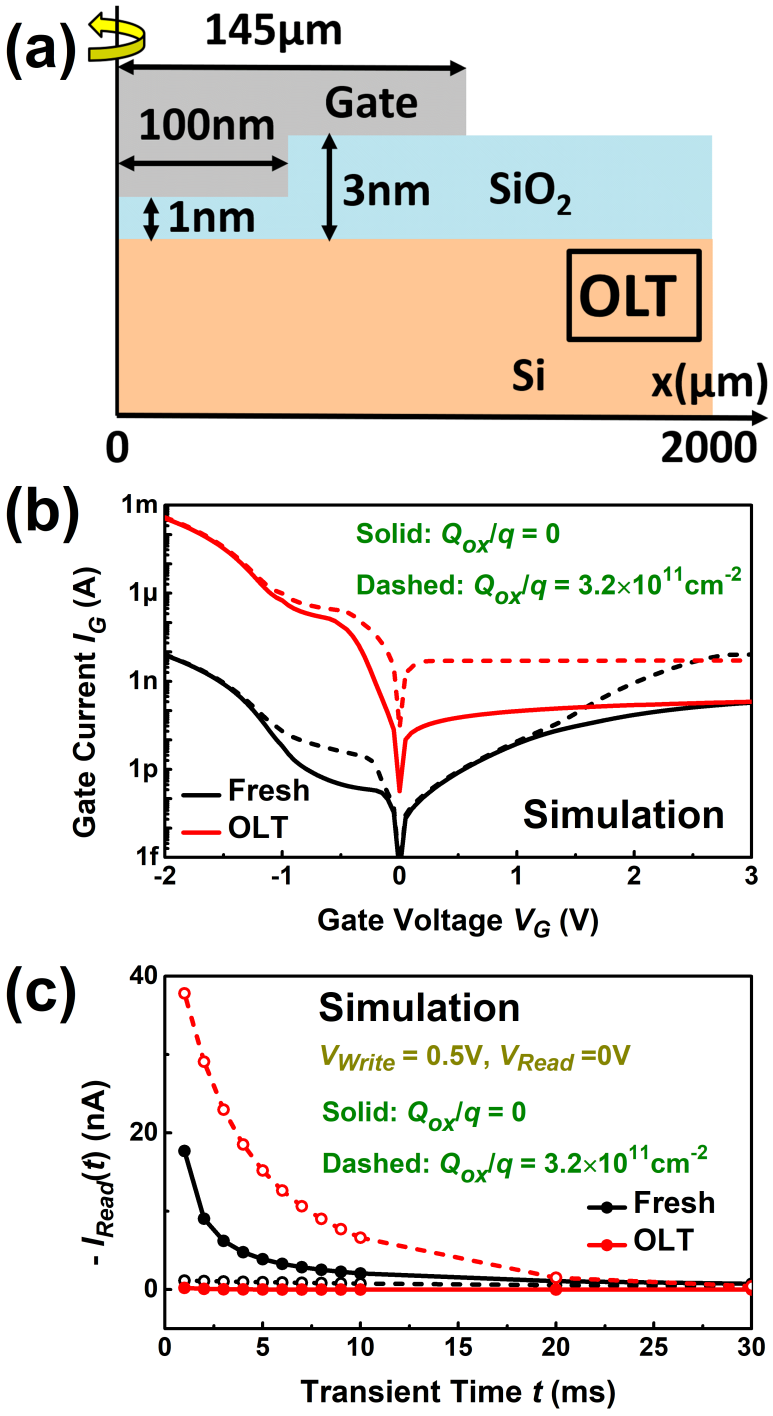

Figure 5–8. (a) Schematics cross section of the OLT MIS device used in the 2-D cylindrical TCAD simulation. (b) $I-V$ characteristics and (c) $I-t$ characteristics when transitioning from 0.5 V steady state to 0 V of the Fresh and OLT MIS devices with Q_{ox} of 0 and 3.2 $\times 10^{11}$ cm^{-2}.

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markedly lower than that observed for the Fresh MIS. However, elevating the number of oxide charge Q_{ox}/q to 3.2×10^{11} cm^{-2} results in a significant increase in $|I_{Read}|$, surpassing that of the Fresh MIS in the absence of oxide charges. Therefore, these simulations not only replicate the enhanced transient current behavior of the OLT MIS device but also underline the pivotal role of oxide charges in this enhancement.

This discovery posits that only the electron deficiency beneath the gate might not sufficiently account superior enhancement in the transient current behavior for the OLT MIS compared to the Fresh MIS. Instead, the enhanced transient current behavior of the OLT MIS also owes to the electron shortage outside the gate. This shortage is caused by inversion electrons, induced by oxide charges, being drained through the OLT spot under a positive write voltage. Therefore, both the electron deficiencies under and outside the gate, facilitated by oxide charges, contribute crucially to the enhanced transient current of the OLT MIS device, as illustrated previously in **Figure 5–7**.

For futher understanding, we isolate and examine the components of the transient currents for the Fresh MIS without oxide charge and the OLT MIS with Q_{ox} of 3.2×10^{11} cm^{-2}. These findings are presented in **Figure 5–9**. For the Fresh MIS, the transient current is primarily comprised of the displacement current, with the tunneling current playing a negligible role, as comprehensively discussed in **Chapter 2**. Conversely, for the OLT MIS, the transient current is overwhelmingly attributed to the tunneling current. The occurrence of a negative sign for the gate tunneling current further signifies that electrons are tunneling from the gate to the silicon. This observation is in alignment with the mechanism outlined in **Figure 5–7**.

Additionally, it is noteworthy that the gate displacement current in the OLT MIS ex-

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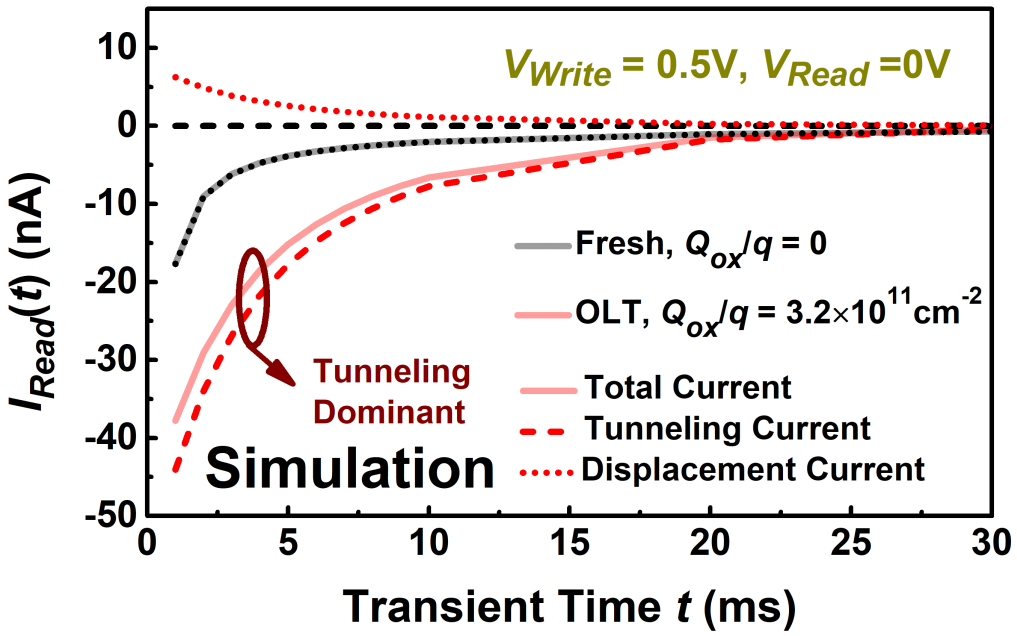

Figure 5–9. Transient behavior of the total current, tunneling current, and displacement current for the Fresh MIS without oxide charge and OLT MIS with Q_{ox} of 3.2 $\times 10^{11}$ cm^{-2}, transitioning from 0.5 V steady state to 0 V.

hibits a positive value, indicative of a negative displacement current at the substrate side, which stands in contrast to the behavior observed in Planar devices as explored in **Chapter 3**. This distinct behavior suggests that carrier dynamics within the silicon of OLT MIS are governed by generation rather than recombination, reinforcing the hypothesis of an electron deficiency in the silicon. This understanding of transient current components further corroborates the unique operational mechanisms at play in OLT MIS devices, differentiating them from their Fresh and Planar counterparts.

5.3 Self-Protective Soft Breakdown

Finally in this chapter, we want to highlight the importance of the SBD induced by DDS on the enhanced transient behavior of the MIS device. Breakdown occurring under DDS

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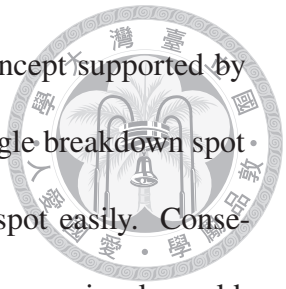

conditions is characterized as a self-protective soft breakdown, a concept supported by findings in [50]. In the DDS environment, the formation of even a single breakdown spot enables inversion electrons beneath the gate to tunnel through this spot easily. Consequently, electrons can no longer accumulate underneath the gate as they previously could, leading to a substantial decrease in the quantity of inversion charges.

Accordingly, the magnitude of the electric field across the oxide, which is

$$|E_{ox}| = \frac{|Q_s|}{d}, \tag{5.2}$$

also reduces significantly. As the probability of the generation of the breakdown spot is positively correlated to the strength of the electric field, further breakdown event will hardly take place. This means that once a breakdown has formed under DDS, no further breakdown will happen. Therefore, this is considered as the self-protective soft breakdown. This phenomenon describes the notion of self-protective soft breakdown, where the system essentially safeguards itself from additional breakdowns following the initial occurrence. Therefore, performing DDS to induce breakdown is considered as the self-protective soft breakdown.

In contrast, for the MIS device with a p-type substrate, the scenario changes notably under the application of a large negative voltage stress (NVS) on the gate. This stress biases the silicon into the accumulation regime, a condition under which no self-protective mechanism is activated, and breakdown events can continue to happen. In the accumulation regime, holes, acting as the majority carriers, tend to gather near the silicon surface. Given the ample supply of holes from the silicon substrate, their density beneath the oxide layer does not diminish, even in the face of significant tunneling rates through any

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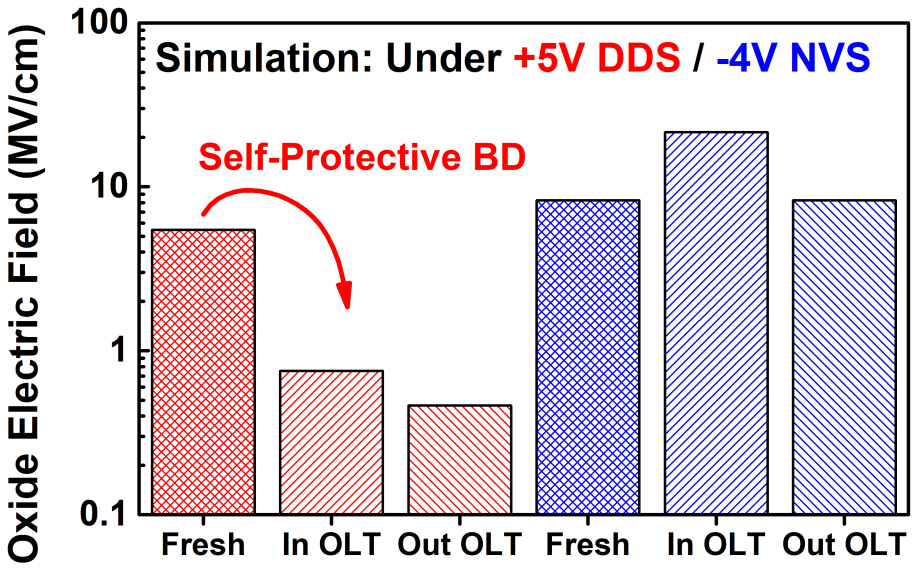

Figure 5–10. Magnitudes of the oxide electric fields for the Fresh and OLT MIS under +5 V deep depletion stress and -4 V negative voltage stress. 'Fresh': Fresh MIS without any OLT spot. 'In OLT': OLT region in the OLT MIS. 'Out OLT': Undamaged oxide in the OLT MIS.

breakdown spot.

In essence, the induction of a breakdown spot does not lead to a reduction in the surface charge density, $|Q_s|$, beneath the oxide. Consequently, the electric field across the oxide, essential in determining the probability of further breakdown events, remains elevated. This persistent high electric field ensures that subsequent oxide breakdown events are more likely to occur, underscoring the difference in the behavior under NVS compared to those undergoing DDS.

To validate the theoretical insights, a TCAD simulation was conducted using the same structure outlined in **Figure 5–8** (a), with the OLT spot serving as the breakdown spot, alongside the structure for the Fresh MIS. The objective is to ascertain the magnitude of the oxide electric field under a +5 V DDS and a -4 V NVS. The results are illustrated in

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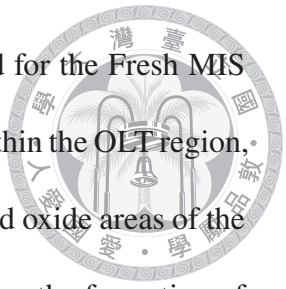

Figure 5–10. In this context, 'Fresh' denotes the oxide electric field for the Fresh MIS devoid of any OLT spot. 'In OLT' represents the oxide electric field within the OLT region, whereas 'Out OLT' represents the oxide electric field in the undamaged oxide areas of the OLT MIS device. The simulation findings reveal that under DDS, upon the formation of an OLT spot, there is a notable reduction in the oxide electric field magnitude, particularly for 'Out OLT'. This contrasts starkly with the NVS scenario, where the oxide electric field remains elevated even in the presence of an OLT spot. Such results underscore the self-protective nature of breakdown under DDS, affirming the theory that the electrical environment induced by DDS inherently mitigates further breakdown occurrences, a protective mechanism absent under NVS conditions.

Based on the discussions presented, it becomes evident that only through DDS can a breakdown transition into a self-protective state. This phenomenon plays a vital role in enhancing the transient behavior observed in OLT MIS devices. For comparative purposes, a -5 V Negative Voltage Stress (NVS) was applied to another Fresh MIS to examine its transient current behavior. **Figure 5–11** (a) illustrates the $I-V$ characteristics before and after NVS, revealing a significant increase in current under forward bias conditions, similar to the DDS-induced scenario depicted in **Figure 5–2** (a). However, distinct from the DDS scenario, post-NVS, the current in the reverse bias regime does not exhibit saturation and even exceeds the original levels observed in the Fresh MIS. This indicates that breakdown induced by a long-time NVS is not self-protective but rather destructive, transforming the device's operation from diode-like to resistor-like, with ohmic current conduction patterns emerging [142].

Further investigation into the transient current behavior was conducted using a write

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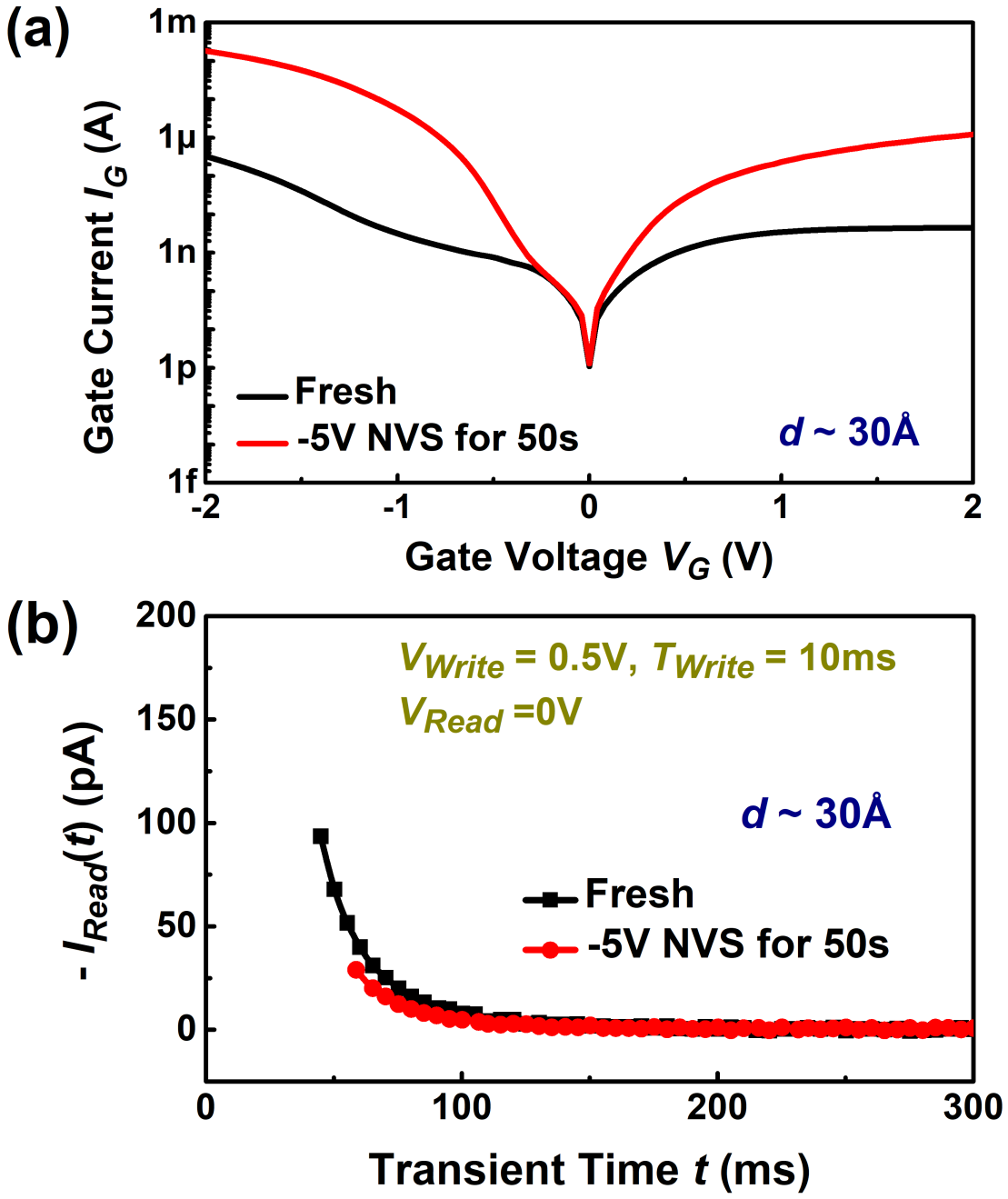

Figure 5–11. (a) $I-V$ characteristics and (b) transient current behavior after a V_{Write} = 0.5 V and T_{Write} = 10 ms voltage pulse, for the same MIS device before and after a -5 V NVS lasting for 50 s.

program with V_{Write} = 0.5 V and T_{Write} = 10 ms. Contrary to the outcomes following DDS, the magnitude of I_{Read} decreases instead of increasing after NVS. This reduction can be linked to the complete loss of tunnel-diode functionality, a consequence of exten-

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sive oxide layer damage. Therefore, to attain an enhanced transient current window, it is imperative that the forming process of the device be conducted via DDS, highlighting the critical importance of the stress methodology in determining the operational and functional integrity of MIS devices.

5.4 Summary

In this chapter, we have detailed the significant advancements in transient current performance achieved with the Oxide Local Thinning (OLT) MIS device. This enhanced capability is primarily a result of employing Deep Depletion Stress (DDS) on a conventional Planar or Fresh MIS device, thereby triggering a self-protective dielectric soft breakdown (SBD). This specific approach ensures that only a single percolation path or breakdown spot emerges under DDS conditions. For ease of understanding, the device post-SBD is conceptualized as an OLT MIS, characterized by a tunneling current that is predominantly focused within this designated OLT region or breakdown spot. Remarkably, this self-protective SBD enables the device to retain tunnel-diode-like electrical characteristics, distinguishing it from outcomes associated with Negative Voltage Stress (NVS) where the oxide undergoes catastrophic damage, rendering the device resistor-like in behavior.

The OLT MIS showcases superior transient current behavior not only when compared to the pre-SBD Fresh MIS but also against the best performing Planar MIS as discussed in **Chapter 2**. When subjected to a voltage program of $V_{Write} = 1$ V and $V_{Read} = 0$ V for $T_{Write} = 10$ ms, the OLT MIS impressively demonstrates an $|I_{Read}|$ of 2 nA. This performance is 20 times greater than that of the optimum Planar configuration (100 pA) under analogous conditions. Moreover, with $T_{Write} = 1000$ ms, the OLT MIS achieves an $|I_{Read}|$ exceeding 10 nA, outstripping the best Planar (600 pA) by 16 times and over 4

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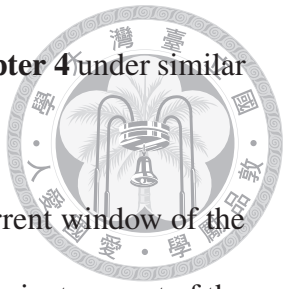

times the performance of the best UTMSG (2.7 nA) discussed in **Chapter 4** under similar program.

We also delve into the rationale behind the enhanced transient current window of the OLT MIS device. Contrary to the displacement current-dominated transient current of the Fresh or Planar MIS, the transient current during the read procedure in the OLT MIS is predominantly driven by the tunneling current from the gate into the silicon. This scenario introduces a significant electron deficiency during the write procedure. TCAD simulations further illuminate that positive oxide charges outside the gate substantially contribute to the transient current enhancement in the OLT MIS. These charges induce inversion electrons in the silicon outside the gate, which are subsequently drained to the gate during the write procedure, leading to an appreciable electron deficiency. Coupled with the under-the-gate electron shortfall, the dominant tunneling current significantly elevates the transient current magnitude in the OLT MIS compared to the Fresh MIS, illustrating the profound impact of OLT on the transient electrical behavior in the MIS device.

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6

Conclusion

6.1 Conclusions

In this dissertation, we delve into the basics of transient current behavior in MISTDs, offering an in-depth exploration of its implications and mechanisms. **Chapter 1** lays the groundwork by presenting the basic electrical characteristics of MISTDs, with a focus on the significance of transient current behavior for dynamic memory applications. Moving on to **Chapter 2**, we undertake a thorough examination of transient current phenomena at millisecond time scales in Planar MISTDs, supported by extensive experimental data. This investigation covers the effects of various factors on transient current magnitude, including write program polarity, write time, write voltage, and the oxide thickness of the device. Based on empirical observations, we propose optimal parameters tailored for dynamic memory applications.

Additionally, we identify and analyze a 'Saturation Phenomenon', where the transient current magnitude reaches a saturation with increasing write voltage during positive write programs. Through TCAD simulations, this phenomenon is attributed to a rapid decrease in silicon band bending at the initiation of the transient. This change facilitates a significant influx of holes that recombine with previously stored inversion electrons within the silicon,

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culminating in the saturation of the transient current. This aspect of our research highlights the intricate interplay between device parameters and transient current behavior, offering valuable insights for optimizing MISTD performance in memory and other semiconductor applications.

In **Chapter 3**, our exploration shifts towards the simulation and modeling of transient current behavior in Planar MISTDs, focusing particularly on the dynamics within the silicon when transitioning from a positive bias to 0 V. Unlike the motion of excess inversion electrons which flow out from the silicon surface to the silicon substrate, leading to a positive substrate electron current, the motion of holes is complicated and can be divided into three periods: 'Dielectric Relaxation', 'Hole Depletion', and 'Diffusion and Recombination'.

During the 'Dielectric Relaxation' period, holes swiftly migrate into the silicon from the substrate, a response to the immediate decrease in silicon band bending, thus inducing a positive substrate hole current. The 'Hole Depletion' period sees an outflow of holes to the substrate, attributed to an overreaction of hole accumulation in the previous period and subsequent expansion of the depletion region, which yields a negative substrate hole current. In the 'Diffusion and Recombination' period, holes from the substrate flow in to recombine with the outgoing excess inversion electrons, leading to a positive substrate hole current.

We also notice that in the 'Diffusion and Recombination' period, the MISTD device is akin to a p-n junction in the forward regime. This understanding allows us to mathematically describe both the electron diffusion current and the hole recombination current, paving the way for an analytical model of the transient current specific in this period.

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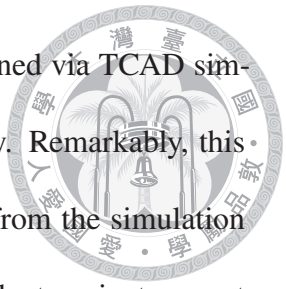

The results derived from this modeling align closely with those obtained via TCAD simulations, underscoring the model's accuracy and predictive capability. Remarkably, this model predicts a saturation voltage with only a 0.01 V discrepancy from the simulation value, demonstrating its precision and offering valuable insights into the transient current phenomena within Planar MISTDs.

The second and third chapters of this dissertation are dedicated to analyzing the transient current behavior in MISTDs with the simplest structural configuration, namely, the Planar MISTDs. These chapters establish that the peak magnitudes of transient currents achievable by Planar MISTDs are 100 pA and 600 pA for write times of 10 ms and 1000 ms, respectively. Building on this foundational knowledge, the subsequent two chapters introduce and explore two specialized designs aimed at augmenting the transient current magnitude. The enhancements proposed through these designs are targeted to improve the utility of MISTDs in applications requiring dynamic memory, potentially offering significant advancements over the baseline performance identified in Planar MISTDs.

In **Chapter 4**, we explore the enhanced transient behavior of the ultra-thin metal surrounded gate (UTMSG) MISTD, which showcases a significant increase in the transient current magnitude. For a write time of 1000 ms, the UTMSG MISTD achieves a transient current of 2.7 nA, which is 4.5 times larger compared to the peak performance observed in the best Planar device. This remarkable enhancement is largely due to the edge late response of excess electrons underneath the surrounding gate, a phenomenon driven by the RC time delay. This delay itself is a consequence of the insulating layer positioned between the central and surrounding gates, along with the resistive properties of the thin metal utilized in the gate's construction.

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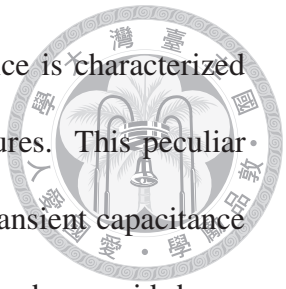

Additionally, the capacitance-voltage curve of the UTMSG device is characterized by a unique reverse-bell shape, distinct from traditional MIS structures. This peculiar capacitance-voltage profile can be leveraged to further amplify the transient capacitance window, offering potential advantages in dynamic memory applications where rapid charge and discharge cycles are critical. Thus, the UTMSG design not only represents a significant leap in transient current performance but also opens new avenues for optimizing the dynamic behavior of MISTDs through innovative structural modifications.

In **Chapter 5**, we introduce the concept of achieving a post-soft-breakdown MISTD through the application of constant positive voltage stress. This stress biases the device into a deep depletion regime, resulting in what can be effectively modeled as an oxide local thinning (OLT) MIS device, where the tunneling current through the oxide layer is significantly concentrated. The OLT device showcases an outstanding transient current performance, with magnitudes reaching approximately 2 nA and over 10 nA for write times of 10 ms and 1000 ms, respectively. This represents a 20 times and 16 times improvement over the best Planar devices. In contrast to the Planar device, where the transient current is primarily comprised of displacement current, the transient current in the OLT device is dominated by tunneling current. This is due to the high tunneling rate through the OLT spot, leading to an electron deficiency within the silicon during the positive write pulse. It is important to note that the presence of oxide charges induces inversion electrons near the Si/SiO_2 interface outside the gate, suggesting that the positive write program induces electron deficiencies not only under the gate but also in regions outside it. When the gate voltage is switched back to 0 V for reading, a significant electron tunneling current flows through the OLT spot to offset these deficiencies, thereby enhancing the transient current

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behavior of the OLT MISTD.

Furthermore, we demonstrate that undergoing dielectric soft breakdown under deep depletion stress is crucial for the self-protective nature of the breakdown to manifest. A breakdown in the deep depletion regime prevents further breakdown events from occurring, as the leakage of inversion electrons through the breakdown spot substantially lowers the magnitude of electric field across the oxide layer. In stark contrast, applying negative voltage stress leads to ongoing breakdown events and catastrophic damage, resulting in a decrease, rather than an increase, in transient current magnitude. This distinction underscores the necessity of specific stress conditions to achieve the desired enhancement in transient current behavior.

In conclusion, this dissertation provides an in-depth exploration of transient current behavior in Planar MISTDs and introduces two innovative designs, UTMSG and OLT, that significantly enhance transient current performance. These proposed structures represent a leap forward in optimizing MISTD technology for dynamic memory applications and other semiconductor uses, highlighting the potential of specialized design strategies to elevate device functionality and efficiency.

6.2 Benchmark

In the concluding chapter of this dissertation, after synthesizing the overarching findings, we aim to benchmark the transient current magnitude across various MISTDs, encompassing Planar, UTMSG, and OLT devices, alongside those documented in the literature. This comparison leverages the read current magnitude at 50 ms following a positive write program, employing write voltage of 1 and 2 V as a measure of performance. The outcomes for write time of 10 and 1000 ms are demonstrated in **Figure 6–1** (a) and (b), respectively.

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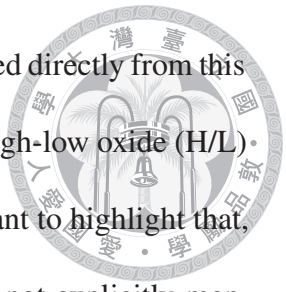

The data pertaining to the Planar, UTMSG, and OLT devices are sourced directly from this dissertation. The results related to edge-removed (ER), Trench, and high-low oxide (H/L) MISTDs are cited from [83], [82], and [84], respectively. It is important to highlight that, for certain studies, the specific transient current values at 50 ms are not explicitly mentioned, necessitating an approximate interpolation from the data provided. This approach ensures a comprehensive and comparative analysis of the transient current performance across a spectrum of MISTD configurations, thereby contextualizing the advancements and contributions of this dissertation within the broader field of semiconductor research.

From **Figure 6–1** , we observe that the special designs of ER, Trench, and H/L MISTD do not appear to offer superior transient current performance compared to the best Planar devices. This observation raises questions regarding the reported enhancements in transient current windows in previous studies [82–84], suggesting that these improvements may be due in part to the suboptimal performance of the Planar devices used as control groups in those works. In the referenced studies, the transient current performance of these specially designed MISTDs is benchmarked against Planar devices with equivalent effective oxide thicknesses, noted to exceed 30 Å. However, our investigations, as detailed in **Chapter 2**, identify the optimal oxide thickness for Planar MISTDs to be approximately 28 to 30 Å. Beyond this thickness, the transient current magnitude decreases significantly, a phenomenon attributed to reduced oxide capacitance and increased oxide charges [107]. Therefore, while ER, Trench, and H/L MISTDs demonstrate enhanced transient currents relative to the Planar devices with the same oxide thicknesses, they fail to surpass the peak performance of the best Planar devices showcased in this dissertation.

Conversely, the OLT and UTMSG MISTDs indeed show a remarkable improvement in

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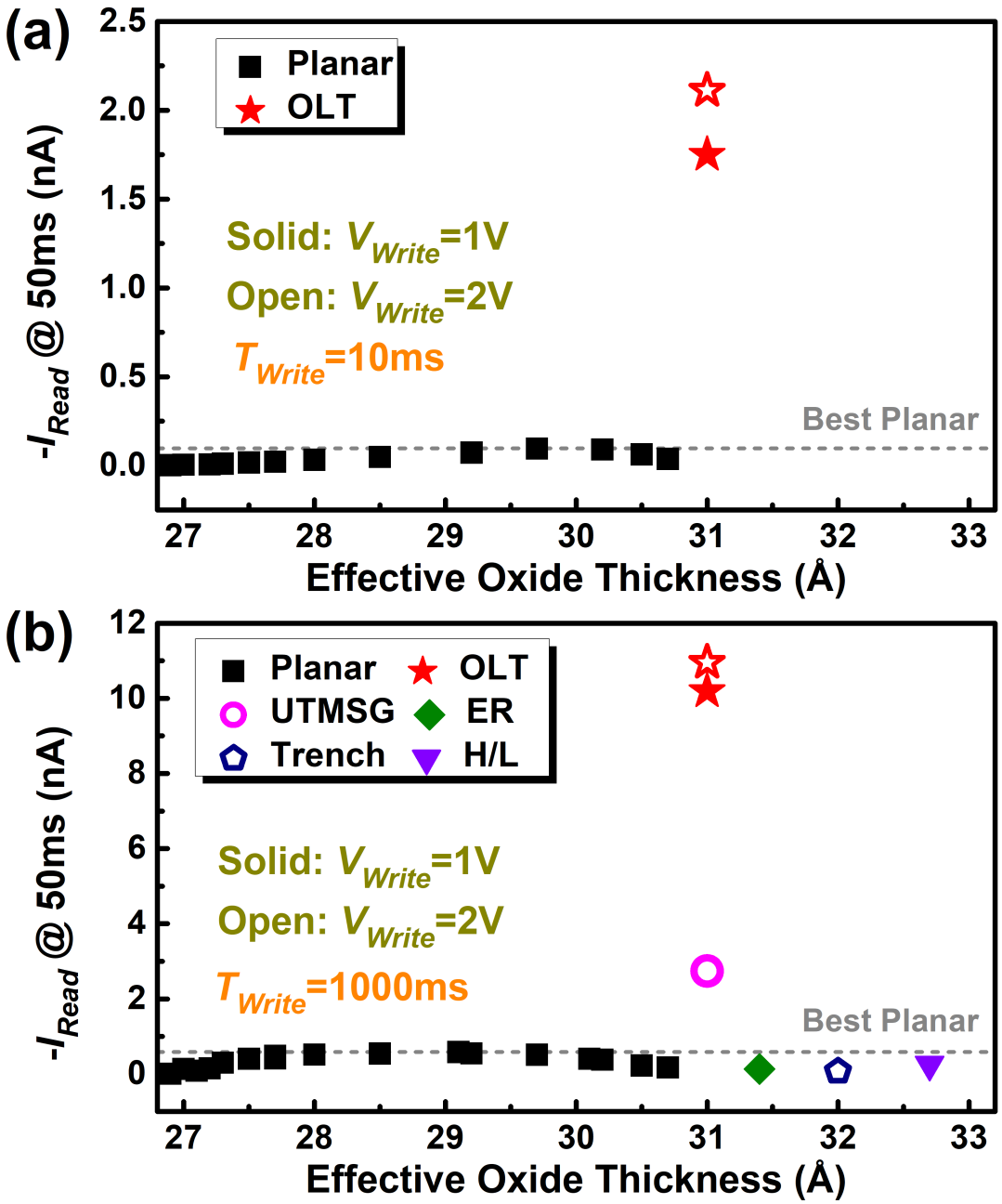

Figure 6–1. Benchmark of the magnitude of the transient current for the MISTDs with several designed structures, with the write time of (a) 10 ms and (b) 1000 ms. Gate radius of each device is summarized as follows. Planar: 145 μm. OLT: 145 μm. UTMSG: 145 μm. ER: 85 μm. Trench: 170 μm. H/L: 145 μm.

transient current behavior, even when compared with the best Planar devices. Specifically, for a write time of 10 ms, the magnitude of the transient current for the OLT MISTD reach

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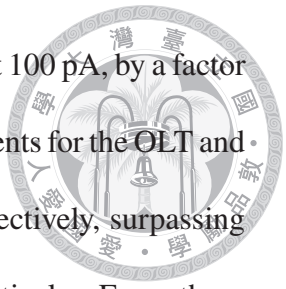

approximately 2 nA, outperform the best Planar device, which stands at 100 pA, by a factor of 20. For a write time of 1000 ms, the magnitudes of the transient currents for the OLT and UTMSG MISTDs are recorded at over 10 nA and about 2.7 nA, respectively, surpassing that of the best Planar device, 600 pA, by 16 and 4.5 times, respectively. From these observations, we deduce that the innovative design approaches employed in the UTMSG and OLT MISTDs effectively yield a superior transient current window compared to that of the Planar MISTD under optimal conditions.

Given that the devices might possess varying gate dimensions, we ensure a fair comparison of the transient current window by calculating the transient current density, with the outcomes presented in **Figure 6−2** . Observations confirm that the designs of ER, Trench, and H/L MISTDs do not surpass the performance of the best Planar devices. Conversely, OLT and UTMSG MISTDs indeed demonstrate superior transient current density relative to the best Planar devices, showcasing the potential advantages of these advanced structural designs of MISTD in enhancing device performance.

6.3 Future Works

In this dissertation, we have identified several areas that merit further investigation, highlighting both the achievements and limitations encountered. Future studies should ideally focus on three primary avenues to build upon the foundational work established here. There is a compelling need to expand the discussion and refine the analytical model concerning the transient current behavior in Planar MISTDs. A deeper exploration into this aspect could yield more precise predictions and insights into the underlying mechanisms governing transient current dynamics.

At the same time, the transient behavior of MISTDs with specialized designs warrants

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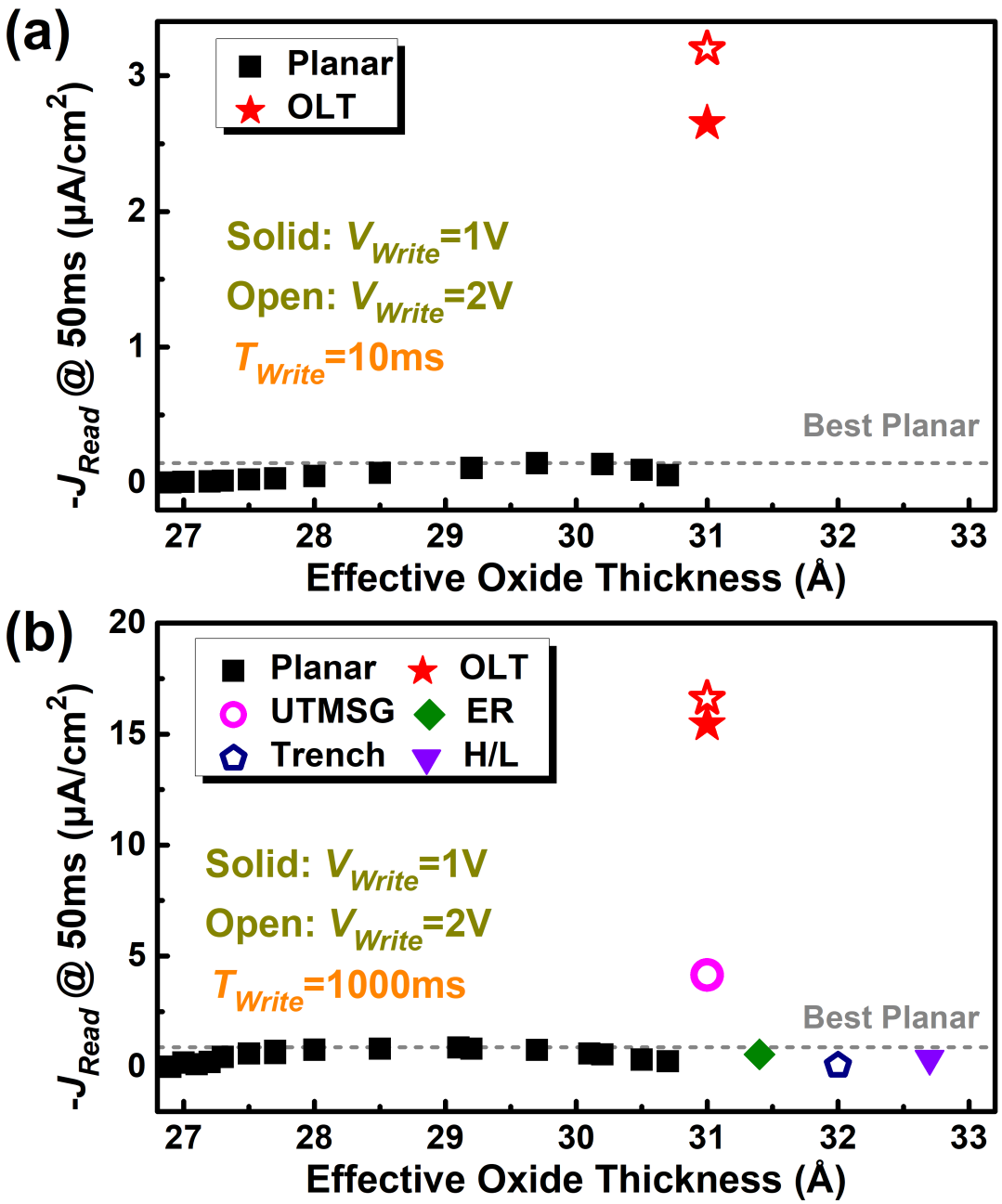

Figure 6–2. Benchmark of the transient current density for the MISTDs with several designed structures, with the write time of (a) 10 ms and (b) 1000 ms.

more comprehensive detailing. While this dissertation introduces innovative structures like UTMSG and OLT MISTDs, a thorough examination of their transient behaviors, under varying operational conditions, could illuminate new paths for optimization and appli-

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cation.

What's more, the pursuit of novel device architectures that harness the advantageous features of the OLT design, while simultaneously enhancing reliability, is imperative. This entails the conceptualization, development, and empirical validation of MISTD structures that not only replicate the superior transient current performance of OLT devices but also address potential vulnerabilities to ensure robust, long-term functionality.

The specific pathways for these explorations are outlined below, offering a roadmap for advancing MISTD technology to new heights of performance and application versatility.

Firstly, **Chapter 2** and **Chapter 3** predominantly explore the transient current behaviors in Planar MISTDs under positive voltage programs, leaving the dynamics following a negative write voltage program somewhat less understood. The investigation into whether hole flow direction changes multiple times post-negative write program, similar to observations after positive write programs, presents an intriguing area for future research. Moreover, the current analytical model presupposes a switch from a steady-state condition akin to scenarios depicted in TCAD simulations. Nevertheless, our experimental setups span a wide range of write times from 10 to 3000 ms, suggesting the necessity for an advanced analytical model that accounts for transient phenomena during the write process itself. For example, during a positive write program pushing the device into deep depletion, a negative electron quasi-Fermi level splitting occurs. This results in electron generation within the depletion region, contributing to excess inversion charges upon switching to 0 V for reading. The future model should, therefore, adeptly incorporate the impact of write time on transient behavior. Further refinement could enable the model to also accurately predict transient currents following negative write programs. Ultimately, the most sophisticated

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model would analytically capture transient current responses for any combination of write and read voltages, offering a comprehensive tool for predicting and understanding MISTD behaviors across a broad spectrum of operational scenarios.

Secondly, while **Chapter 4** and **Chapter 5** concentrate on the transient current behavior during the transition from a positive bias to 0 V in the UTSMG and OLT MISTDs, it is proposed that future studies should explore scenarios involving switches from negative biases as well. The current scope of simulation and modeling for these innovative structures is somewhat restricted. Given that both UTMSG and OLT devices have demonstrated superior transient current capabilities compared to the best Planar MISTD, a thorough investigation combining experimental validation, simulations, and analytical modeling is anticipated to yield deeper insights. Such a comprehensive approach could significantly enhance the design and application of MISTDs in dynamic memory and beyond, especially as these devices venture into the realms of sub-micrometer scaling. Additionally, the enriched understanding from these studies may offer valuable design considerations for optimizing device performance at these reduced scales, promising advancements in the utility and efficiency of semiconductor technologies.

Lastly, we introduce an innovative MISTD structure, the ultra-edge-thickened (UET) MISTD, which shows promise for further enhancements in transient current behavior for dynamic memory applications. As depicted in **Figure 6–3** , this design draws inspiration from the OLT MISTD, leveraging a thick oxide region outside the gate that harbors an abundance of positive oxide charges. These charges, in turn, induce inversion electrons beneath the oxide, maintaining charge neutrality. At the same time, the thin oxide region offers an efficient tunneling pathway for electrons, allowing a positive write pulse to ef-

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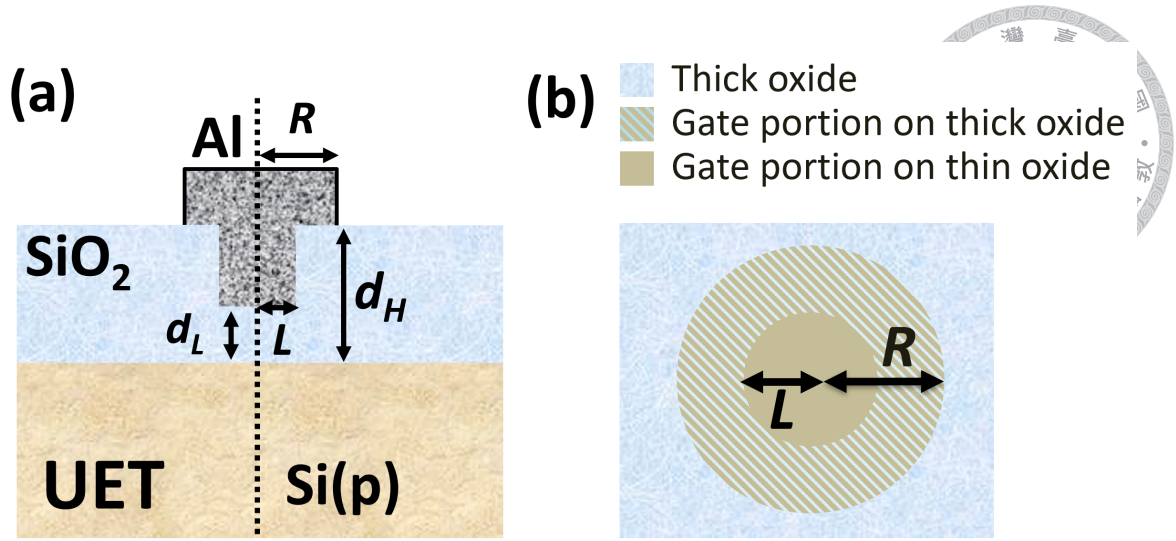

Figure 6–3. (a) Schematic cross section and (b) top view of the ultra-edge-thickened (UET) MISTD. R: Gate radius. L: Radius of the thin oxide region. d_H and d_L: Oxide thickness of the thick and thin oxide region, respectively.

fectively drain out electrons from the silicon both under and outside the gate area. During the read procedure, a substantial electron current tunnels through the thin oxide region, addressing the resultant electron deficiency, mirroring the operational mechanism of the OLT MISTD. However, distinct from the OLT approach, the UET device's thin and thick oxide regions are precisely delineated during the fabrication process through photolithography, not by soft breakdown induced by deep depletion stress. This methodological distinction suggests enhanced device endurance and reliability for the UET MISTD.

Preliminary investigations into the UET device have already shown it to surpass the best Planar MISTD in terms of transient current behavior, using current density as a measure of performance. Thus, we posit that the UET MISTD stands as a strong contender for the optimal design in dynamic memory applications. The UET device's structure, defined through patterning, allows for the deliberate design and optimization of parameters such as gate radius (R), radius of the thin oxide region (L), and the oxide thicknesses of

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the thick (d_H) and thin (d_L) oxide regions, offering a versatile framework for advancing MISTD technology.

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Appendix A

Transient Current Behavior in Planar MIS Tunnel Diodes with Oxide Charges

A.1 Overview

In the end of **Chapter 2**, we demonstrated how oxide charges influence the transient current magnitude at 50 ms in Planar MISTDs. Specifically, it was observed that for positive write programs, the transient current magnitude decreases in devices with oxide charges compared to those devoid of any oxide charges. This observation, mentioned in the main body of the dissertation, indicates a complex underlying mechanism responsible for the reduction in transient current magnitude, necessitating a detailed exposition. Thus, we reserve a comprehensive explanation for this phenomenon to the appendix of this dis-

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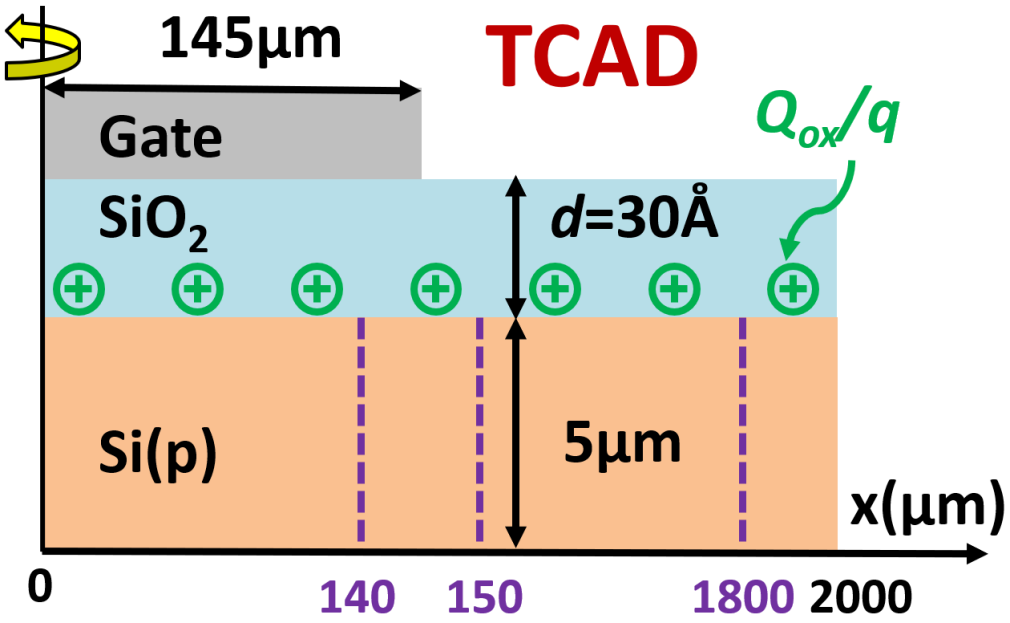

Figure A–1. Schematic cross section of the MISTD device used in the 2-D cylindrical simulation. Q_{ox}/q stands for the number density of the oxide charges. x represents the horizontal axis of the device. Several positions which are chosen to present the electron density are highlighted: 140 μm (under the gate, near the gate edge), 150 μm (outside the gate, near the gate edge), and 1800 μm (outside the gate, faraway from the gate edge).

sertation, where we can delve into the intricacies of how oxide charges impact transient current behavior without the constraints of space.

In this appendix, we delve into the simulation results pertaining to transient currents measured at 50 ms, echoing the discussions from the main text of the dissertation, within a Planar MISTD featuring an oxide layer thickness of 30 Å. The device cross section used for the TCAD simulation is illustrated in **Figure A–1** . These simulations explore a range of oxide charge number densities (Q_{ox}/q), from 0 to 5×10^{11} cm^{-2}. The simulated device maintains a standard gate radius of 145 μm, yet it incorporates an expanded total substrate area with a radius of 2000 μm. This modification aims to highlight the effect of oxide charges located outside the gate area on the device's transient current behavior. Six spe-

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cific values for the oxide charge number density are examined: 0, 2.8, 3, 3.2, 4, and 5 $\times 10^{11}$ cm^{-2}. The $-I_{Read}$ versus V_{Write} characteristics derived from these simulations are presented in **Figure A–2** (a), with subfigure (b) providing a detailed view of the segment where $-I_{Read} > 0$. The main observation can be summarized as follows:

- Devices devoid of any oxide charges display the largest $-I_{Read}$ across all write voltages.
- The introduction of oxide charges leads to a reduction in $-I_{Read}$, though not in a monotonic fashion. The extent of this reduction also varies with the applied write voltage.
- Oxide charges cause an increase in V_{Write} at which $-I_{Read}$ reaches the peak value, referred to as the saturation voltage.
- Contrary to the constant $-I_{Read}$ after saturation observed in devices without oxide charges, $-I_{Read}$ may decline for write voltages exceeding the saturation voltage in devices with oxide charges, particularly when Q_{ox}/q surpasses 3×10^{11} cm^{-2}.
- Remarkably, $-I_{Read}$ turns negative under a high write voltage of 3 V for substantial oxide charge densities ($Q_{ox}/q \geq 4 \times 10^{11}$ cm^{-2}), indicating a significant shift in transient current behavior with the increase in oxide charge density.

The results can also be interpreted by using the number density of oxide charges, Q_{ox}/q, as a parameter of interest. **Figure A–3** depicts the relationship between $-I_{Read}$ and Q_{ox}/q under write voltages of 2 V and 3 V. It is noteworthy that for the p-type silicon substrate with a doping concentration of 10^{16} cm^{-3} used in the simulations, number densities of oxide charges below 2.6×10^{11} cm^{-2} induce merely a depletion region outside the gate due to

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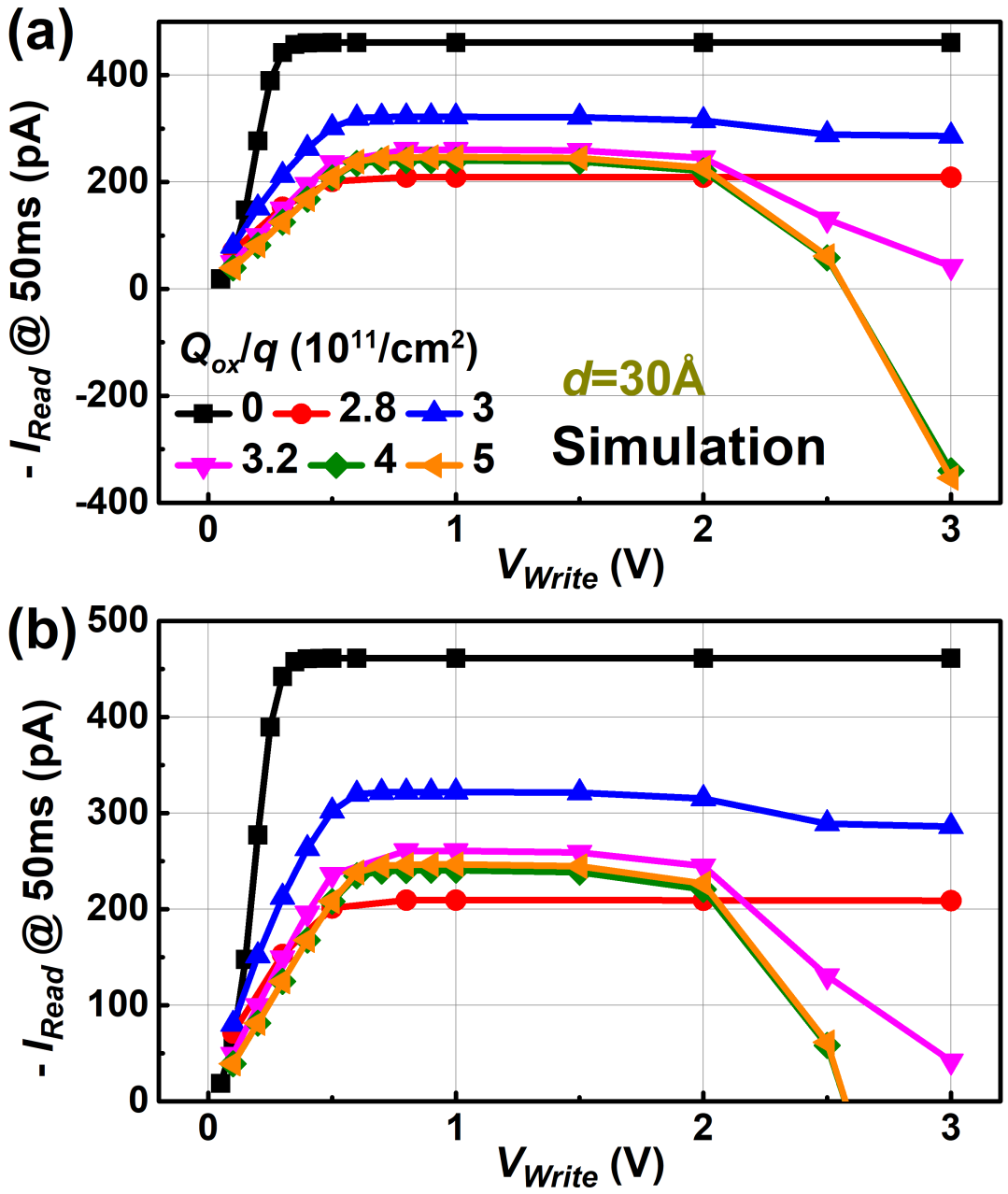

Figure A–2. (a) Simulation results of the transient read current at 50 ms versus write voltage ($-I_{Read}$ versus V_{Write}) characteristics for a Planar MISTD with an oxide layer of 30 Å and varying number densities of oxide charges, ranging from 0 to 5×10^{11} cm^{-2}. (b) Enlargement of (a) for $-I_{Read} > 0$.

charge neutrality, with negligible inversion electrons. Conversely, when Q_{ox}/q surpasses 2.6×10^{11} cm^{-2}, both a depletion region and inversion charges emerge outside the gate area.

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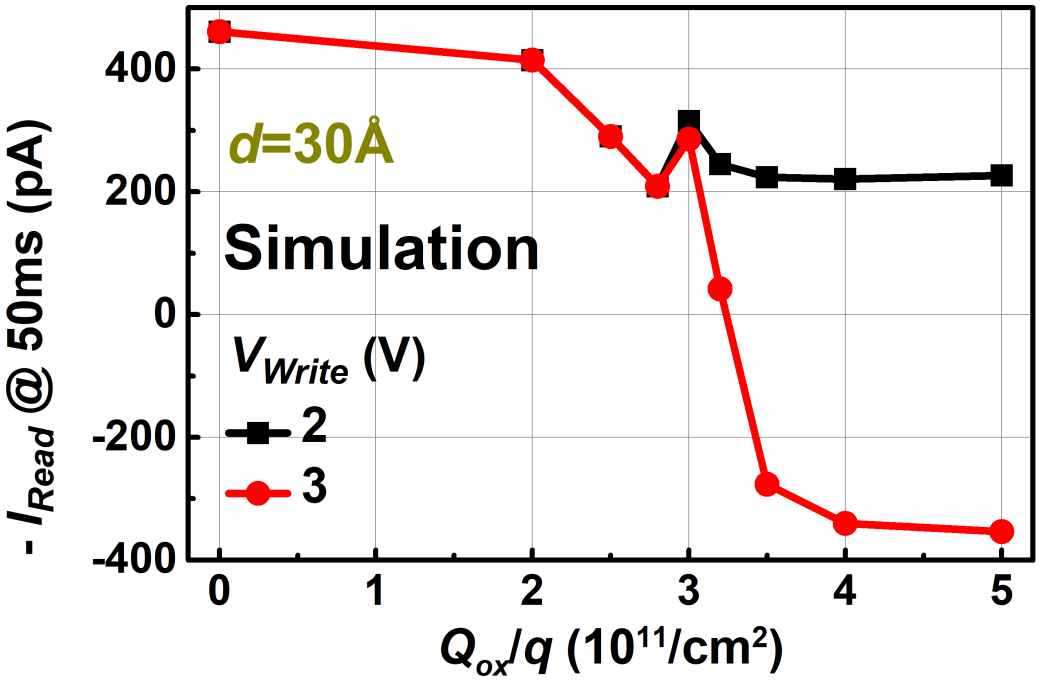

Figure A–3. Simulation results of the transient read current at 50 ms versus the number density of oxide charges ($-I_{Read}$ versus Q_{ox}/q) characteristics for a Planar MISTD with an oxide layer of 30 Å and the write voltages of 2 and 3 V.

Observations from **Figure A–3** indicate that for $Q_{ox}/q \leq 2 \times 10^{11}$ cm^{-2}, $-I_{Read}$ slightly decreases. When Q_{ox}/q lies between 2 and 3 $\times 10^{11}$ cm^{-2}, $-I_{Read}$ initially falls but subsequently rises. At $Q_{ox}/q = 3 \times 10^{11}$ cm^{-2}, $-I_{Read}$ reaches a local peak. For values of $Q_{ox}/q \geq 3 \times 10^{11}$ cm^{-2}, $-I_{Read}$ once again declines. Notably, at a V_{Write} of 3 V, $-I_{Read}$ significantly drops and can even turn negative. This phenomenon underscores that with a substantial presence of oxide charges under high write voltages, the direction of the transient current can indeed reverse, offering further insight into the complex interplay between oxide charges and transient current behaviors in Planar MISTDs.

To address the observations noted above, we selectively focus on Q_{ox}/q equal to 0, 3, and 4 $\times 10^{11}$ cm^{-2}, under V_{Write} of 1 V and 3 V, to thoroughly investigate the transient

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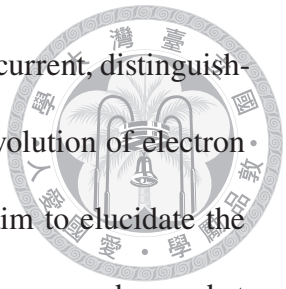

behavior. This detailed examination includes analyses of the substrate current, distinguishing between electron and hole components, as well as tracking the evolution of electron density within the silicon. By adopting this focused approach, we aim to elucidate the underlying mechanisms contributing to the varied transient current responses observed at different oxide charge densities and write voltages. This in-depth exploration will provide valuable insights into the interplay between oxide charges, substrate currents, and electron dynamics, shedding light on the factors influencing transient current behavior in Planar MISTDs.

A.2 Decreased Transient Current Magnitude Due to Accelerated Recombination in The Extended Depletion Region

In this section, we address the reduction in transient current magnitude arising from increased oxide charges by delving into simulation results for oxide charge densities (Q_{ox}/q) of 0, 3, and 4 $\times 10^{11}$ cm^{-2} under the V_{Write} of 1 V. The phenomenon of the reversal of direction of I_{Read} will be explored in the subsequent section.

We present the substrate transient currents, encompassing the total, electron, and hole currents, in **Figure A–4**, categorizing them according to the respective Q_{ox}/q values. This approach mirrors the analytical method introduced in **Chapter 3**. It is reiterated that I_{Read} signifies the gate transient current, whereas **Figure A–4** and following figures focus on the substrate current. Due to the principle of charge neutrality, the gate transient current I_{Gate} and the substrate transient current $I_{Substrate}$ share the same magnitude but opposite

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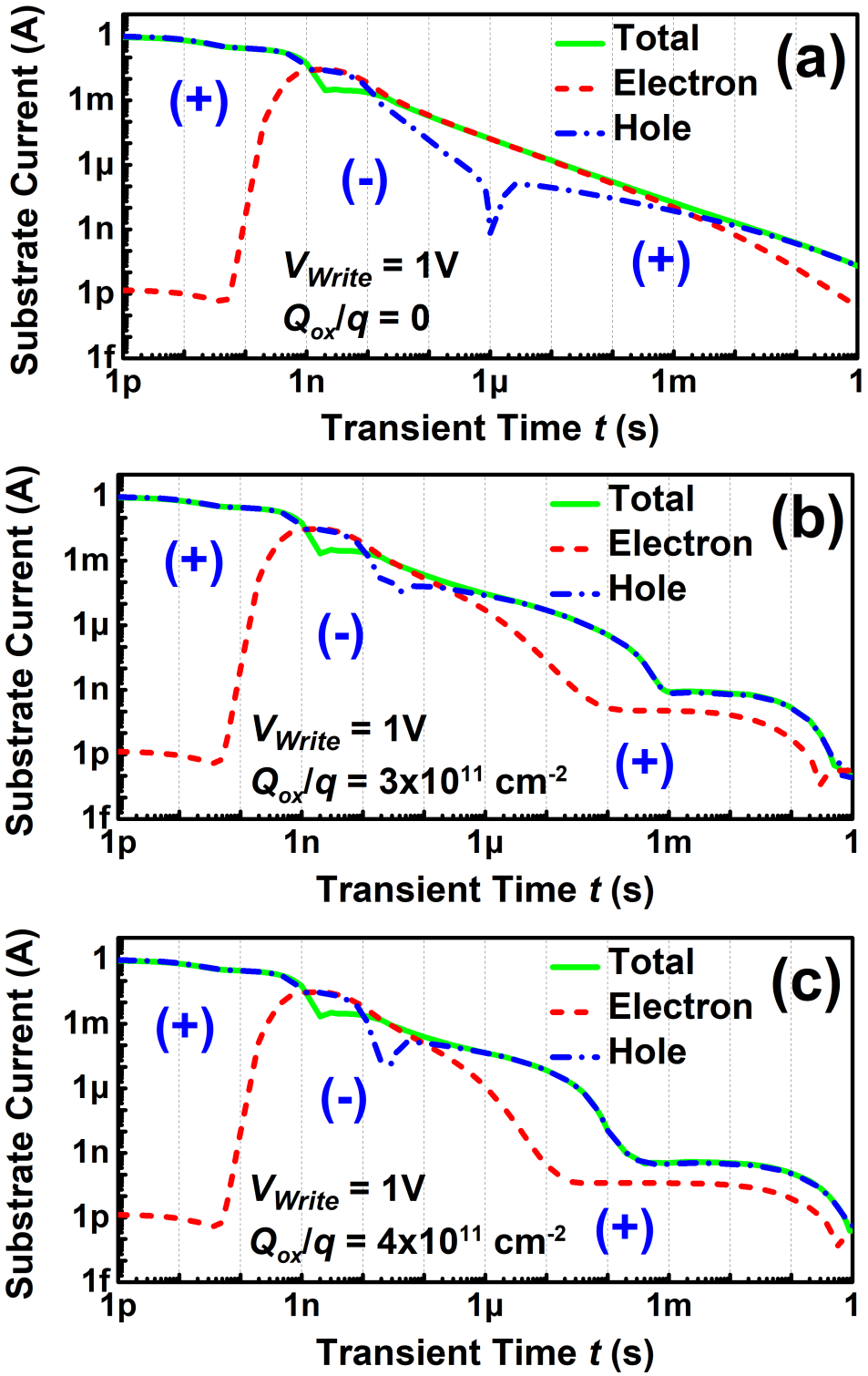

Figure A–4. Substrate transient currents, including the total current, electron current and hole current, for the device with Q_{ox}/q = (a) 0, (b) 3, and (c) 4 $\times 10^{11}$ cm^{-2} under V_{Write} = 1 V.

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signs, expressed as:

$$I_{Substrate}(t) = -I_{Gate}(t). \tag{A.1}$$

where t represents the transient time. Consequently, a positive $-I_{Read}$ at 50 ms, indicating a negative I_{Read} at the gate, translates to a positive substrate current, providing insight into the interplay between oxide charge densities and transient current behaviors.

The behavior of substrate transient current for $Q_{ox}/q = 0$ in **Figure A–4** (a) has been extensively analyzed in **Chapter 3**. Key findings from this analysis are summarized as follows:

- The substrate total and electron currents maintain positive values throughout the transient phase.
- For times $t < 1$ ns and $t > 10$ ms, the total current is predominantly influenced by the hole current, whereas between 10 ns and 1 ms, the electron current predominates.
- Initially, within the first 100 ps, the electron current magnitude remains low due to the diffusion of excess electrons still within the silicon and not yet reaching the substrate.
- The behavior of the substrate hole current enables segmentation of the transient phase into three distinct periods: dielectric relaxation, hole depletion, and diffusion and recombination.
- During the dielectric relaxation period ($t < 1$ ns), a positive substrate hole current arises as holes rapidly influx from the substrate, reacting to the sudden decrease in

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silicon band bending ψ_s.

- In the hole depletion period (1 ns < t < 1 μs), the hole current turns negative as holes are drawn away to the substrate, a consequence of the overreaction in the previous period and the expansion of the depletion region.

- Lastly, the diffusion and recombination period (t > 1 μs) is characterized by a positive substrate hole current, where holes from the substrate flow in to recombine with outgoing electrons.

The segmentation into three distinct periods, initially described for $Q_{ox}/q = 0$, persists even when oxide charge densities are present, as evidenced in **Figure A–4** (b) and (c). Despite the introduction of oxide charges, the substrate hole current continues to exhibit a transition from positive to negative and ultimately back to positive. Besides, the first turning point, for the substrate hole current from positive to negative, remains almost the same at around 100 ps. However, the second turning point, for the substrate hole current from negative to positive, becomes earlier for the device with more oxide charges. It moves from 1 μs for $Q_{ox}/q = 0$, to about 10 ns for $Q_{ox}/q = 3$ and 4 $\times 10^{11}$ cm^{-2}. This turning point is determined by the competition between opposing hole current flows during the hole depletion period. On one side, hole outflow to the substrate occurs due to the overreaction in the preceding period and the expansion of the depletion region. On the other side, hole inflow from the substrate aims to recombine with excess electrons, manifesting as the recombination current. The direction of the substrate hole current hinges on which of these components is more substantial. Therefore, the earlier turning of positive substrate hole current in devices with oxide charges suggests a significantly enhanced recombination process. Furthermore, it is noted that in the diffusion and recombination period, the

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dominance of the hole current starts only after $t > 10$ ms for $Q_{ox}/q = 0$. Conversely, for $Q_{ox}/q = 3$ and 4×10^{11} cm^{-2}, the substrate hole current begins to prevail earlier, before 1 μs, also indicating a stronger recombination process.

Additionally, the decay of substrate electron and hole current does not follow a linear trend on a log-log scale, unlike the scenario with $Q_{ox}/q = 0$. This linear decay pattern for $Q_{ox}/q = 0$ has been thoroughly elucidated and modeled in **Chapter 3**, with the assumption that electron current density (J_e) and hole current density (J_h) correspond to diffusion current density (J_{diff}) and recombination current density (J_{rec}), respectively. With $Q_{ox}/q = 0$, the absence of a depletion region and inversion charges outside the gate area simplifies the device to a laterally uniform system, justifying a 1-D model MIS system approximation. However, the presence of oxide charges introduces depletion regions and potentially inversion charges outside the gate area, necessitating consideration of lateral carrier interactions within the silicon during transient conditions. Consequently, the system cannot be reduced to a simplistic 1-D model, requiring a more complex two-dimensional approach to accurately capture carrier movements.

The insights derived from **Figure A−4** can be viewed from another perspective, as illustrated in **Figure A−5**. This figure delineates the transient current curves by juxtaposing identical current components across varying oxide charge densities within the same subfigure. Specifically, subfigures (a), (b), and (c) display the substrate total current, electron current, and hole current, respectively. As previously observed, it is more clear here that **Figure A−5** (c) elucidates that the second turning point of the hole current, where it transitions from negative to positive, occurs earlier for higher Q_{ox}/q values. Beyond the previously discussed findings, it is notable that the total substrate currents for devices

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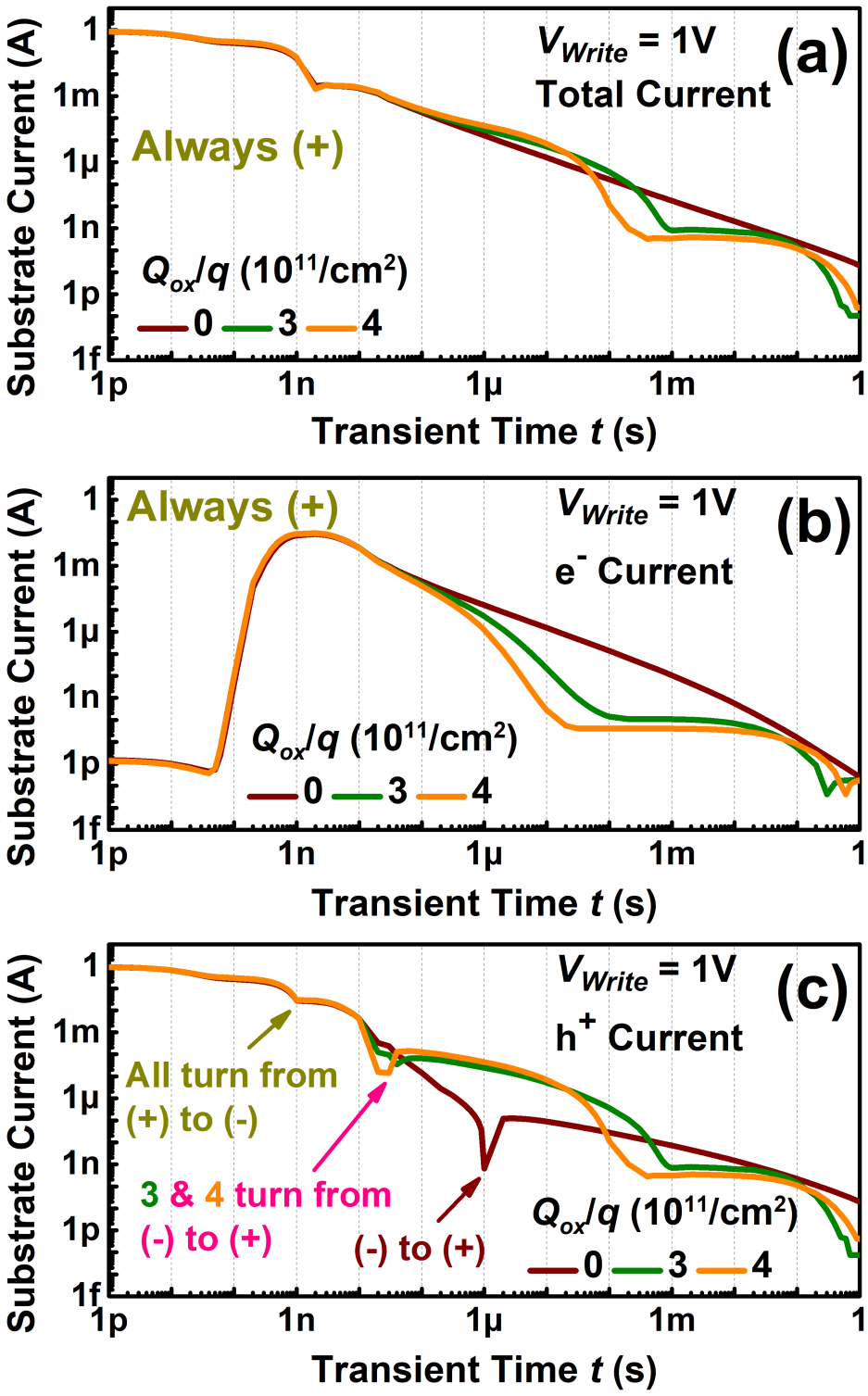

Figure A–5. Substrate transient (a) total currents, (b) electron currents, and (c) hole currents for the device with $Q_{ox}/q = 0$, 3, and 4×10^{11} cm^{-2} under $V_{Write} = 1$ V.

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with oxide charges initially exceed those without any oxide charges during microsecond time scales. However, as the focus shifts to millisecond time scales, which is our primary interest, the current magnitudes decrease and fall below those observed in devices devoid of oxide charges. The phenomenon whereby devices with oxide charges show a temporary advantage at microsecond scales, only to be surpassed by devices without oxide charges at a longer transient time, emphasizes the complex interplay of oxide charges in influencing transient current responses in MISTDs.

Thus far, the reduction in $-I_{Read}$ at millisecond time scales for devices with oxide charges has been linked to a more pronounced recombination process within the silicon at microsecond time scales, as evidenced by the increase in substrate hole current during this period. To delve deeper, we investigate the time evolution of electron density near the silicon surface (at a 2 nm depth) at various specific positions x, with findings illustrated in **Figure A−6**. The electron density, n_e, at positions x = 140 μm (under the gate, near the gate edge), 150 μm (outside the gate, close to the gate edge), and 1800 μm (far from the gate edge), are depicted in subfigures (a), (b), and (c), respectively. **Figure A−6** (a) reveals that the initial excess inversion electrons stored under the gate are comparable across devices with varying Q_{ox}/q. Yet, post $t > 1$ μs, n_e under the gate substantially decreases. Given that, as indicated in **Figure A−5**, the substrate electron current is considerably lower at microsecond time scales, this decrease in excess electrons is not attributed to diffusion to the substrate. Concurrently, since the recombination rate predominantly relies on the electron quasi-Fermi level at the surface, which in turn is influenced by the surface electron density, a diminished n_e would not suggest enhanced recombination in the depletion region beneath the gate. Consequently, we infer that the swift decline in n_e at microsecond time

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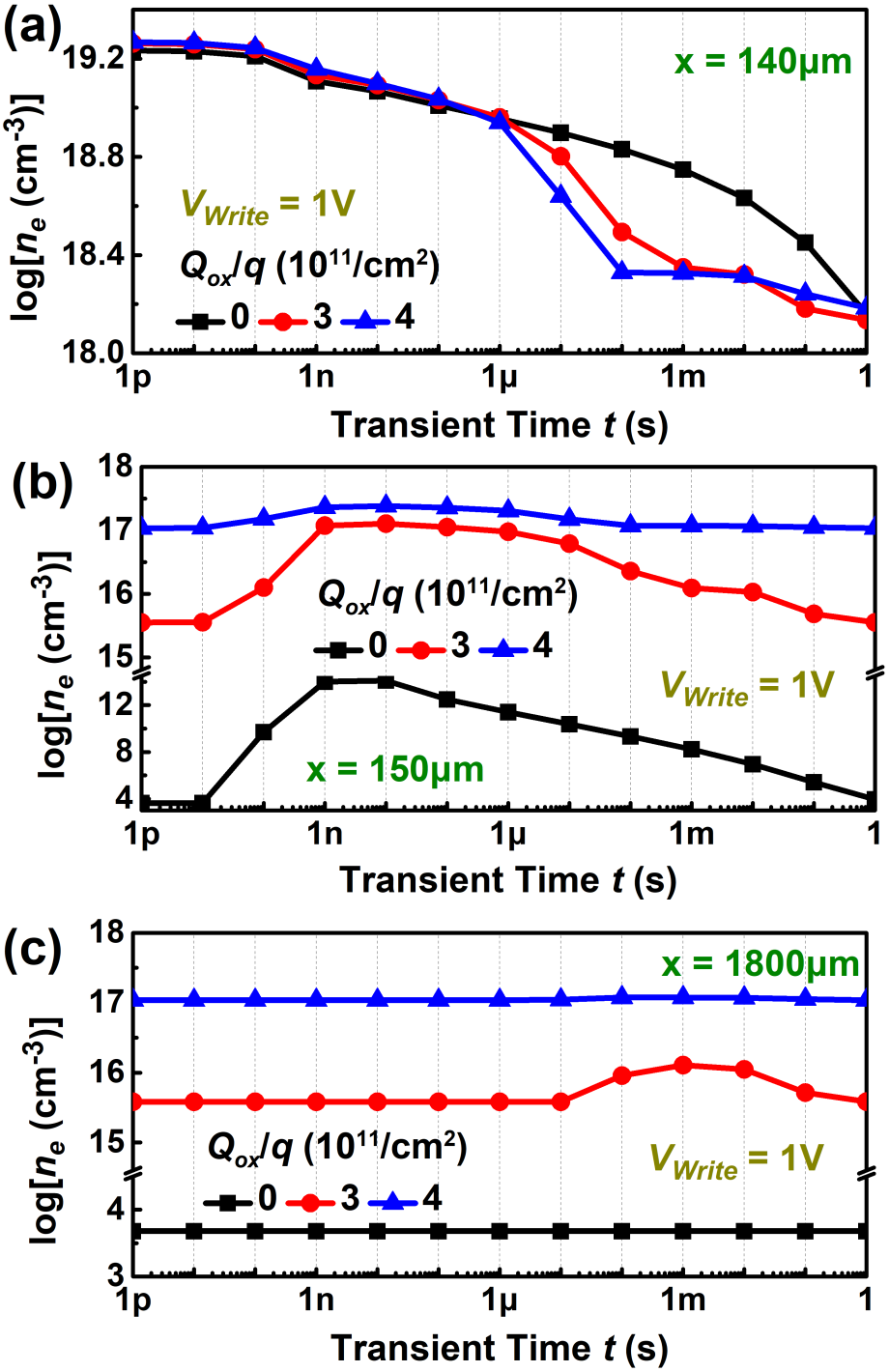

Figure A–6. Time evolution of the electron densities at 2 nm depth near the silicon surface for Q_{ox}/q = 0, 3, and 4 $\times 10^{11}$ cm^{-2} under V_{Write} = 1 V, at x = (a) 140 μm (under the gate, near the gate edge), (b) 150 μm (outside the gate, near the gate edge), and (c) 1800 μm (outside the gate, faraway from the gate edge).

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scales is not a result of intensified diffusion or recombination under the gate.

Therefore, the significant reduction in electron density under the gate in devices with oxide charges is attributed to the lateral outward diffusion of excess electrons from the gate area. This mechanism is clearly supported by the data in **Figure A–6** (b) and (c), where n_e, the electron density outside the device, rises during the transient. For example, at $x = 150$ µm, although n_e for $Q_{ox}/q = 3 \times 10^{11}$ cm^{-2} remains relatively constant at the beginning and end of the transient phase, it experiences a surge of more than an order of magnitude between 1 ns to 100 µs. This increase in n_e serves as definitive proof that excess inversion electrons beneath the gate are diffusing laterally outward, thereby elevating the electron density in these areas. Similarly, at $x = 1800$ µm, n_e for $Q_{ox}/q = 3 \times 10^{11}$ cm^{-2} also sees an increase from 100 µs to 10 ms, indicating a delayed augmentation due to the time required for excess electrons to diffuse further outside the gate. This late increase highlights the spatial dynamics of electron movement and the significant impact of oxide charges on electron distribution during the transient state.

It may be observed that the timing of the increase in n_e outside the gate does not precisely coincide with the decrease in n_e beneath the gate. The primary reason for this discrepancy lies in the behavior of the transporting electrons, which is governed by the lateral diffusion current, $J_{diffuse,lateral}$. This lateral diffusion current is distinct from the previously defined vertical diffusion current, J_{diff}, that flows vertically towards the substrate. The lateral diffusion current can be mathematically expressed as [89]:

$$J_{diffuse,lateral} = qD_n \frac{dn_e}{dx}, \tag{A.2}$$

where q is the charge of an electron, D_n is the electron diffusion coefficient, and $\frac{dn_e}{dx}$ rep-

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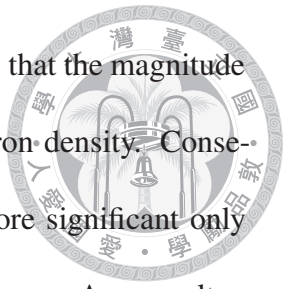

resents the gradient of the electron density. This relationship indicates that the magnitude of $J_{diffuse,lateral}$ is directly proportional to the gradient of the electron density. Consequently, the lateral diffusion of electrons intensifies and becomes more significant only after n_e outside the gate reaches a high level and extends over a broad area. As a result, a substantial reduction in n_e under the gate is observed only when these conditions are met.

To further substantiate our findings, we directly visualize the temporal evolution of the lateral spatial distribution of electron density, as shown in **Figure A–7**. Subfigures (a), (b), and (c) correspond to oxide charge densities (Q_{ox}/q) of 0, 3, and 4×10^{11} cm^{-2}, respectively, all under a write voltage (V_{Write}) of 1 V. It is important to note that the scales across these subfigures are adjusted for clearer illustration.

In **Figure A–7** (a), for $Q_{ox}/q = 0$, n_e outside the gate remains low, resulting in minimal lateral diffusion. In contrast, when oxide charges are present, the diffusion of excess electrons intensifies, reaching areas far outside the gate. This electron movement is akin to a spreading sea wave: the electron density near the gate edge disperses outwards and diminishes over time, consequently elevating the electron density in regions far from the gate after a certain propagation duration. A closer look at **Figure A–7** (b) reveals that the electron 'wave' expands significantly by the time the transient reaches 10 μs, becoming more pronounced at 100 μs. This observation mirrors the notable decrease in n_e under the gate for $t > 1$ μs, as highlighted in **Figure A–6** (a).

Thus, it can be concluded that the reduction in n_e under the gate in devices with oxide charges is attributable to the outward lateral diffusion of electrons from the gate area. Moreover, as Q_{ox}/q rises, the presence of induced inversion electrons outside the gate also increases, which in turn enhances the lateral diffusion of electrons as described by

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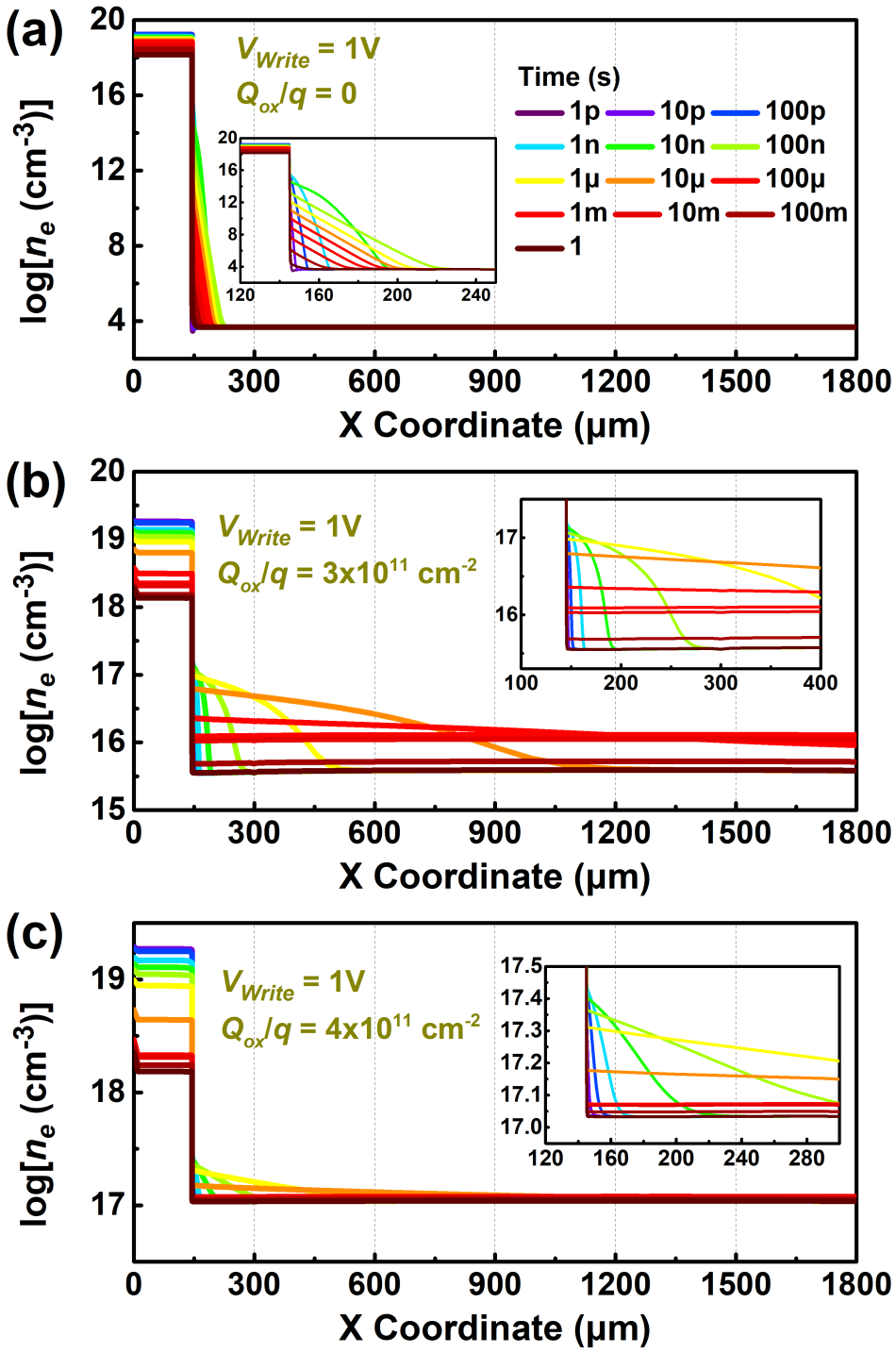

Figure A–7. Time evolution of the lateral distribution of the electron densities at 2 nm depth near the silicon surface for Q_{ox}/q = (a) 0, (b) 3, and (c) 4 $\times 10^{11}$ cm^{-2} under V_{Write} = 1 V. Insets: Enlargement near the gate edge.

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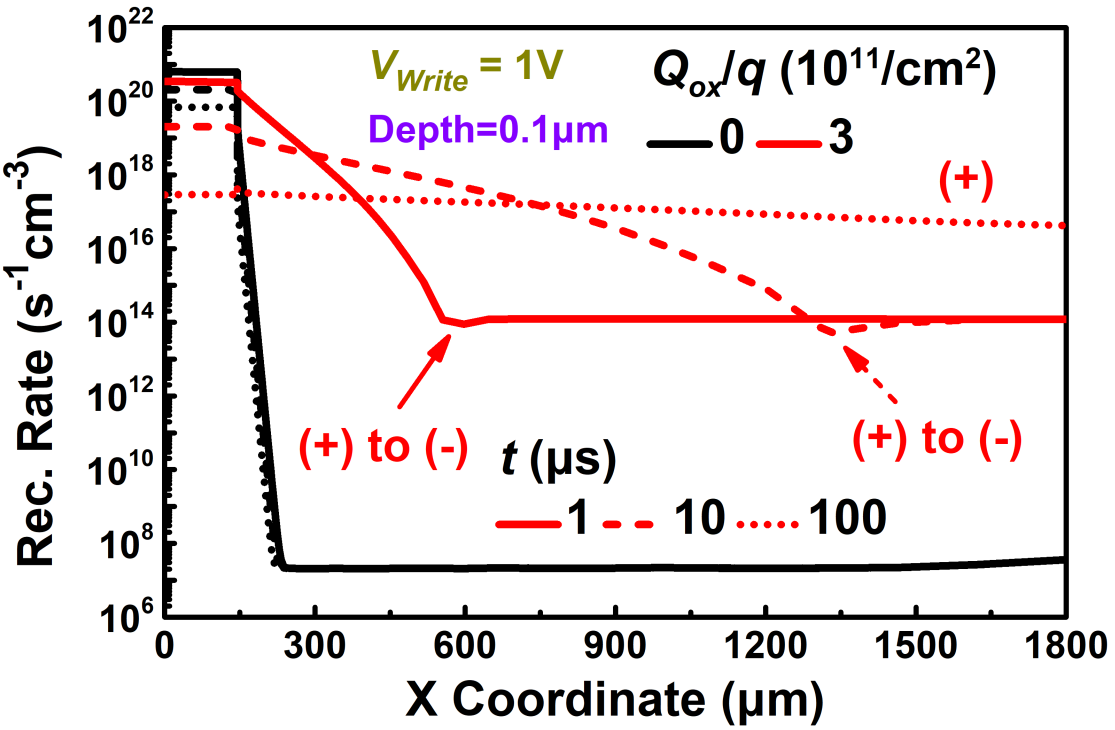

Figure A–8. Lateral spatial distribution of the recombination rate inside the silicon at the depth of 0.1 μm from the surface for Q_{ox}/q of 0 and 3 $\times 10^{11}$ cm^{-2} under V_{Write} = 1 V, for transient time t at 1, 10, and 100 μs.

(A.2). This mechanism leads to a more rapid decline in n_e under the gate, consistent with observations in **Figure A–6** (a).

Therefore, the ensuing query revolves around the mechanism through which excess electrons diffusing outside the gate are discharged in devices with oxide charges. Given the extremely low substrate electron current, as evidenced in **Figure A–5** , it is implausible for these excess electrons to be discharged via diffusion to the substrate. Consequently, the most reasonable explanation is that these electrons undergo recombination with incoming holes within the depletion region located outside the gate. This is supported by the fact that the area of the depletion region outside the gate is considerably larger than that underneath it, fostering a much more significant recombination process. This hypothesis aligns with the observed enhancement in the magnitude of the substrate hole current, which becomes

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the predominant contributor to the substrate total current. This alignment of observations underscores the critical role of recombination outside the gate area in mediating electron discharge in devices with oxide charges.

To validate these observations further, we analyze the lateral spatial distribution of the recombination rate inside the silicon at a depth of 0.1 μm from the surface for Q_{ox}/q values of 0 and 3 $\times 10^{11}$ cm^{-2} under V_{Write} of 1 V, at transient times t of 1, 10, and 100 μs. The findings are presented in **Figure A–8**. For $Q_{ox}/q = 0$, the decline in recombination rate outside the gate is minimal when compared to that beneath the gate. Conversely, for $Q_{ox}/q = 3 \times 10^{11}$ cm^{-2}, the recombination rate outside the gate is on par with that underneath it. Given that the area outside the gate significantly exceeds that of the area under the gate, the total recombination process is markedly intensified.

Moreover, we note a transition in the recombination rate from positive to negative at $t = 1$ and 10 μs. It is noted that the recombination process occurs predominantly in areas with carrier concentrations exceeding steady-state levels. Consequently, regions yet to be reached by the lateral diffusion of electrons lack excess carriers. As the electron waves continue to propagate outwards at $t = 1$ and 10 μs, as depicted in **Figure A–7**, areas not yet impacted by these waves will not experience significant recombination.

In summary, the reduction in transient current magnitude, $-I_{Read}$, in devices with oxide charges can be attributed to the outward lateral diffusion of excess electrons, followed by the accelerated recombination in the extended depletion region outside the gate.

Finally, the discussion above can be summarized schematically in **Figure A–9** and **Figure A–10**, corresponding to the discharge mechanism of excess when switching from 1 V for the device with $Q_{ox}/q = 0$ and 3 $\times 10^{11}$ cm^{-2}, respectively.

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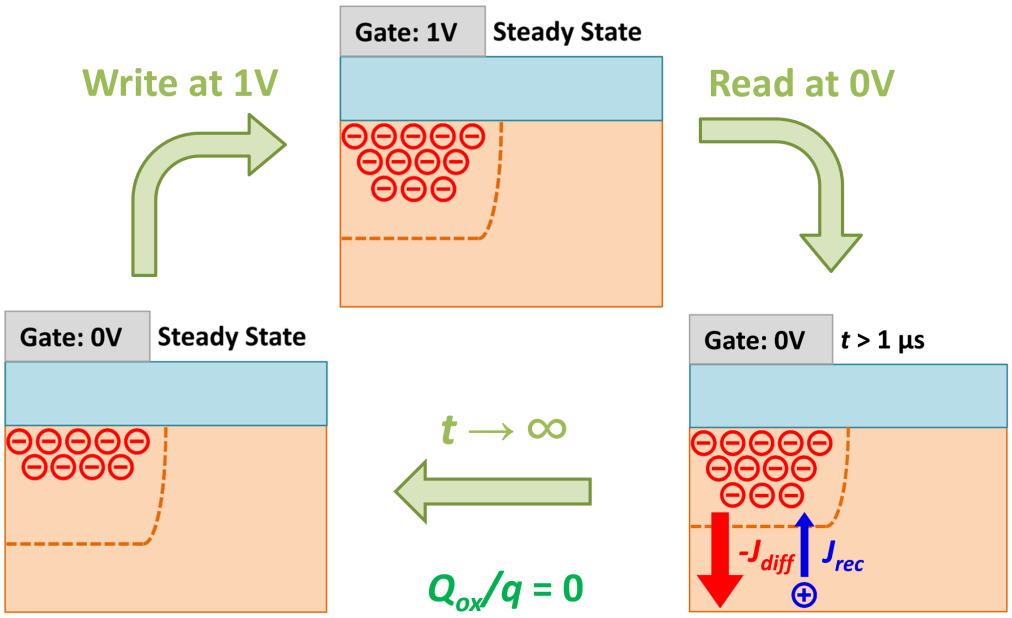

Figure A–9. Schematics illustrating the discharge mechanism of the excess electrons for the device without oxide charges, switching from 1 V.

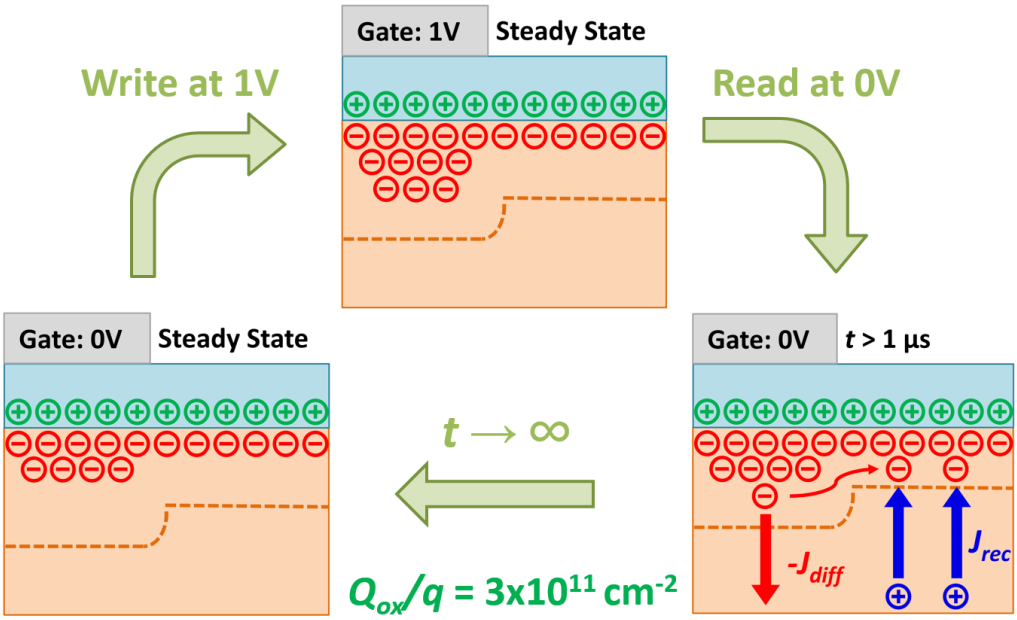

Figure A–10. Schematics illustrating the discharge mechanism of the excess electrons for the device with $Q_{ox}/q = 3 \times 10^{11}$ cm^{-2}, switching from 1 V.

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A.3 Reversed Transient Current Direction For Substantial Oxide Charges Under Large Write Voltage

The previously discussed sections have elucidated the mechanisms behind the decreased magnitude of transient current at millisecond time scales in devices with oxide charges. Nonetheless, observations from **Figure A−2** and **Figure A−3** indicate that when Q_{ox}/q surpasses 3.5 $\times 10^{11}$ cm^{-2}, the sign of $-I_{Read}$ becomes negative under a substantial V_{Write} of 3 V. This phenomenon of reversed transient current direction presents a distinct behavior that cannot be accounted for solely by the mechanisms outlined in the prior section.

In this section, our goal is to explore the underlying mechanisms that lead to the observed phenomena in simulations conducted under V_{Write} of 3 V, particularly for Q_{ox}/q of 0, 3, and 4 $\times 10^{11}$ cm^{-2}, with a special emphasis on the latter scenario. The substrate transient currents, including total, electron, and hole currents, are depicted in **Figure A−11** and **Figure A−12**, categorized by both the value of Q_{ox}/q and the type of current component, respectively.

Fundamentally, the behavior of transient current in devices devoid of oxide charges remains consistent between write voltages of 1 V and 3 V. Similarly, the transient current response in devices with Q_{ox}/q of 3×10^{11} cm^{-2} under a V_{Write} of 1 V largely mirrors that observed under a V_{Write} of 3 V. However, an essential divergence is noted for devices with Q_{ox}/q of 4×10^{11} cm^{-2}, highlighting an essential difference in transient current behavior under large write voltage conditions for substantial oxide charges.

For the device with an oxide charge density (Q_{ox}/q) of 4×10^{11} cm^{-2} under V_{Write} of 3 V, the transient current behavior up to 100 μs mirrors the behavior observed under

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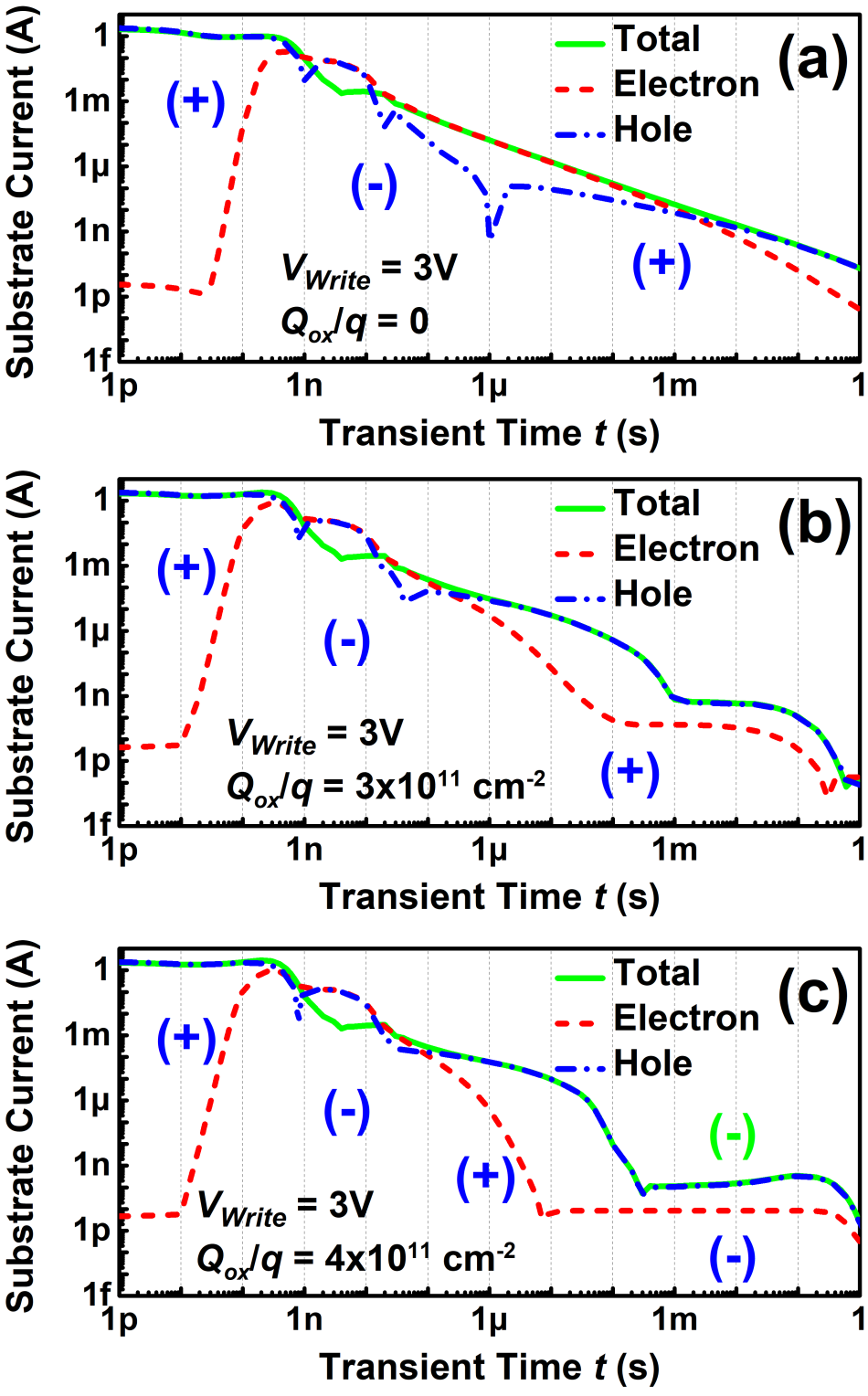

Figure A–11. Substrate transient currents, including the total current, electron current and hole current, for the device with Q_{ox}/q = (a) 0, (b) 3, and (c) 4 $\times 10^{11}$ cm^{-2} under V_{Write} = 3 V.

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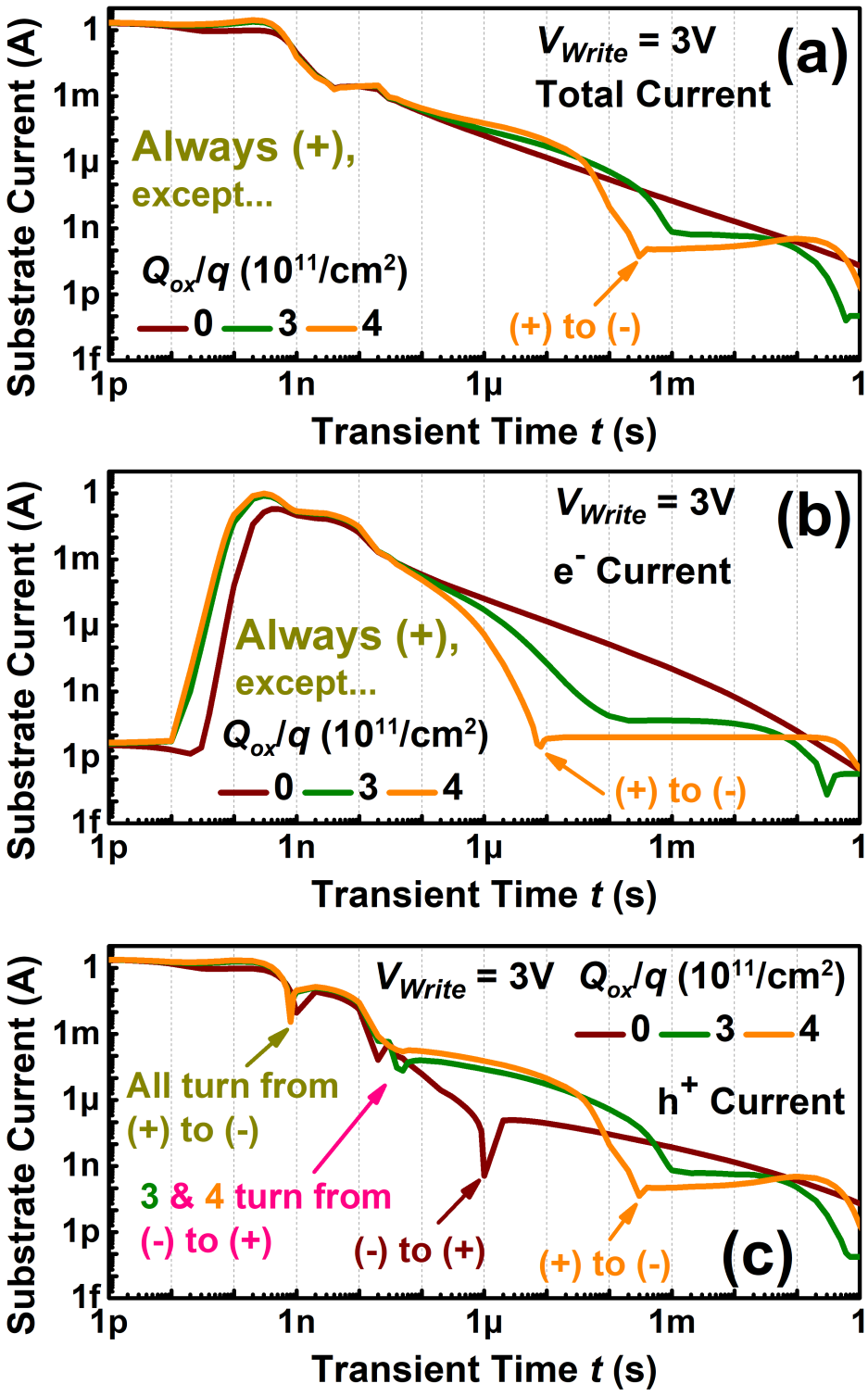

Figure A–12. Substrate transient (a) total currents, (b) electron currents, and (c) hole currents for the device with Q_{ox}/q = 0, 3m and 4 $\times 10^{11}$ cm^{-2} under V_{Write} = 3 V.

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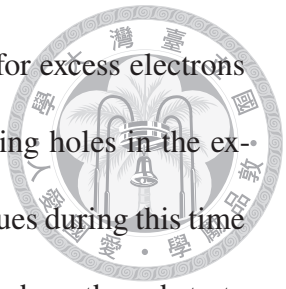

V_{Write} of 1 V. This similarity suggests that the discharge mechanism for excess electrons beneath the gate, via lateral diffusion and recombination with incoming holes in the expanded depletion region, remains consistent across different V_{Write} values during this time period. However, a distinct phenomenon is observed around 300 µs, where the substrate total current, and predominantly its hole current component, abruptly shifts to a negative value. This behavior, not previously noted in our discussions, persists into millisecond time scales. Consequently, this results in a positive transient current at the gate, thereby producing a negative $-I_{Read}$, marking a significant departure from earlier observed transient current dynamics.

To understand the underlying cause of the transient current's reversed direction at millisecond time scales, we examine the evolution of electron density 2 nm beneath the silicon surface at specific locations: x = 140 µm (directly under the gate, near the gate edge), 150 µm (just outside the gate, near the gate edge), and 1800 µm (significantly outside the gate), for a device with Q_{ox}/q of 4×10^{11} cm^{-2} under write voltages of 1 V and 3 V. The findings are documented in **Figure A–13**, yielding several key observations:

- In subfigure (a), differing from scenarios with V_{Write} = 1 V, where n_e beneath the gate decreases monotonically over time, for V_{Write} = 3 V, n_e beneath the gate falls below the 0 V steady state level within 100 µs to 10 ms, followed by an increase towards recovery.

- In subfigures (b) and (c), at the beginning and the end of the transient for V_{Write} = 1 V, n_e outside the gate remains nearly the same. However, under V_{Write} = 3 V, the scenario alters significantly. By the end of the transient, corresponding to the 0 V steady state, n_e exceeds its initial value, which corresponds to the 1 V steady state.

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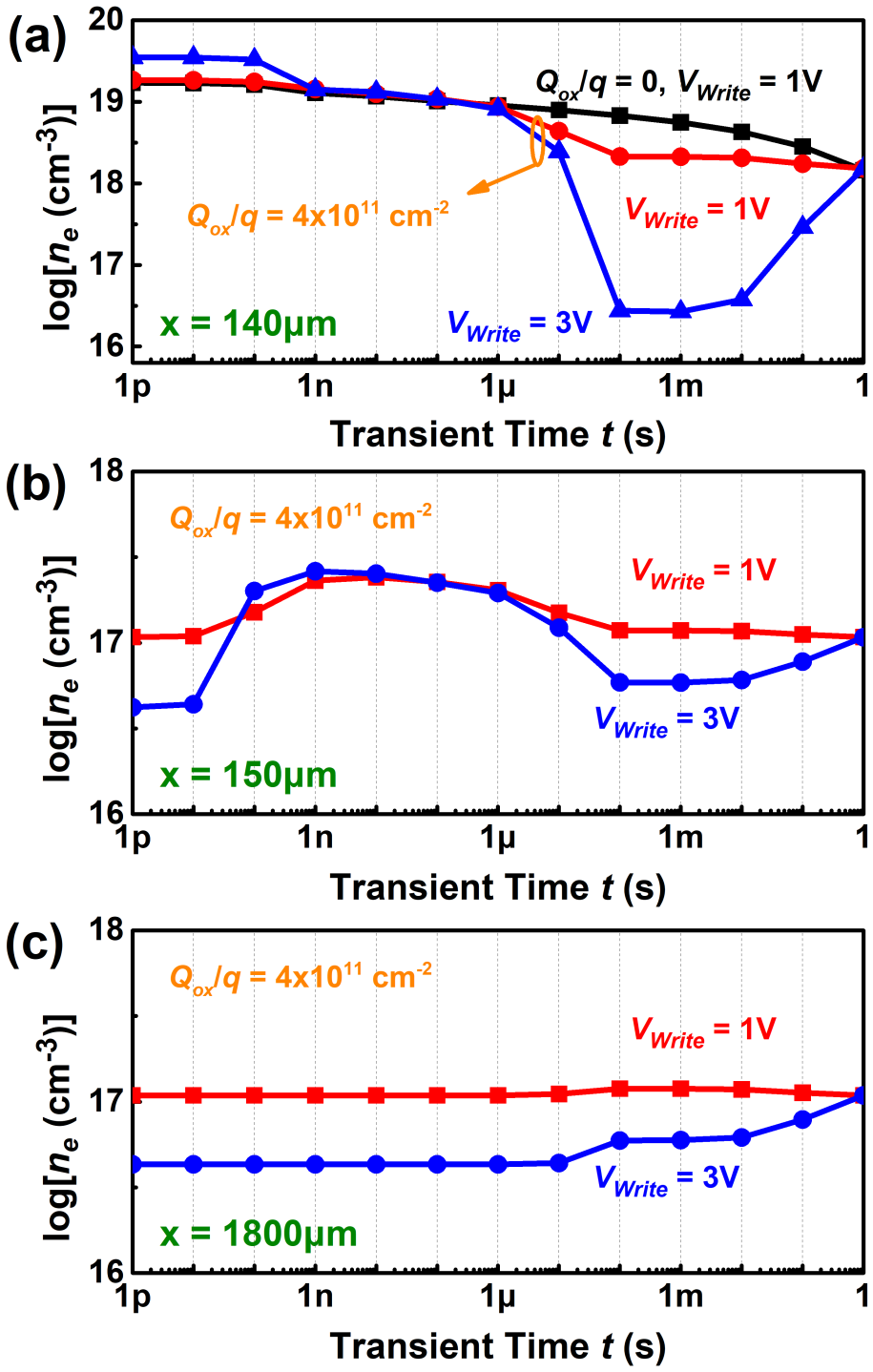

Figure A–13. Time evolution of the electron densities at 2 nm depth near the silicon surface for $Q_{ox}/q = 4 \times 10^{11}$ cm^{-2} under $V_{Write} = 1$ and 3 V, at x = (a) 140 μm (under the gate, near the gate edge), (b) 150 μm (outside the gate, near the gate edge), and (c) 1800 μm (outside the gate, faraway from the gate edge). The results without oxide charges under $V_{Write} = 1$ V are also displayed in (a) for comparison.

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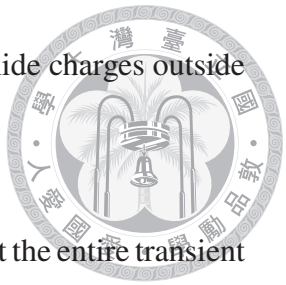

This suggests that inversion electrons, induced by significant oxide charges outside the gate, are drained out during the write process.

- For $V_{Write} = 3$ V, at $x = 1800$ μm, n_e consistently rises throughout the entire transient phase. Conversely, at $x = 150$ μm, n_e escalates beyond the 0 V steady state level early in the transient (between 1 ns and 10 μs), but later drops below the 0 V steady state level for t ranging from 100 μs to 10 ms, before ultimately rising again to reach the steady state.

Based on the observations outlined, the mechanism behind the reversed direction of the transient current for devices with substantial oxide charges can be hypothesized as follows. In devices with an oxide charge density significantly exceeding the threshold necessary for inducing strong inversion outside the gate, a large population of inversion electrons is present in the 0 V steady state due to charge neutrality. When subjected to a sufficiently high write voltage, pushing the device into deep depletion, inversion electrons outside the gate are drawn towards and beneath the gate, causing a corresponding decrease in electron density in outside the gate areas. Upon switching back to 0 V, an excess of electrons accumulates under the gate while an electron deficiency arises outside the gate.

In the initial 10 μs, these excess electrons under the gate diffuse laterally outwards, akin to the electron waves discussed previously. This lateral diffusion through the weak inversion layer outside the gate presents the most efficient discharge route for excess electrons, compared to vertical diffusion into the substrate or recombination with incoming holes. Despite the initial electron deficiency outside the gate, the lateral diffusion process temporarily creates regions of electron excess at certain locations and times (e.g., $x = 150$ μm between 1 ns and 1 μs) relative to the 0 V steady state. Consequently, during these in-

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tervals, enhanced recombination occurs in the extended depletion region outside the gate, mirroring the dynamics observed in the prior section.

However, the electron deficiency outside the gate proves to be so significant that the electron supply from beneath the gate is insufficient for compensation. Moreover, the inversion electrons beneath the gate become less than those in the 0 V steady state in an effort to offset the electron deficiency outside. This leads to an electron deficiency under the gate as well. Consequently, after 100 μs, both regions under and outside the gate experience electron deficiencies simultaneously. This scenario resembles the dynamics observed in the oxide local thinning (OLT) MISTD discussed in **Chapter 5**, as schematically depicted in **Figure 5–7** . In the OLT MISTD, these electron deficiencies are offset by electrons tunneling from the gate through the OLT region into the silicon, maintaining a positive gate transient current at the millisecond time scale, corresponding to a negative $-I_{Read}$.

Meanwhile, in this planar MISTD with substantial oxide charges, the absence of OLT regions means that the tunneling rate through the 30 Å oxide layer during the read process at zero bias is minimal. Consequently, the electron deficiency cannot be addressed through electron tunneling. Instead, it is mitigated by the electron generation process within the extended depletion region, both under and outside the gate. Generated electrons migrate towards the surface, while generated holes move to the substrate, resulting in a negative substrate hole current that dominates the total current. Therefore, due to current conservation, a positive gate transient current manifests at the millisecond time scale, resulting in a negative $-I_{Read}$.

The observation regarding the dynamics of electron deficiency and its compensation mechanisms, as described, is also supported by the visual data presented in **Figure A–14** (a).

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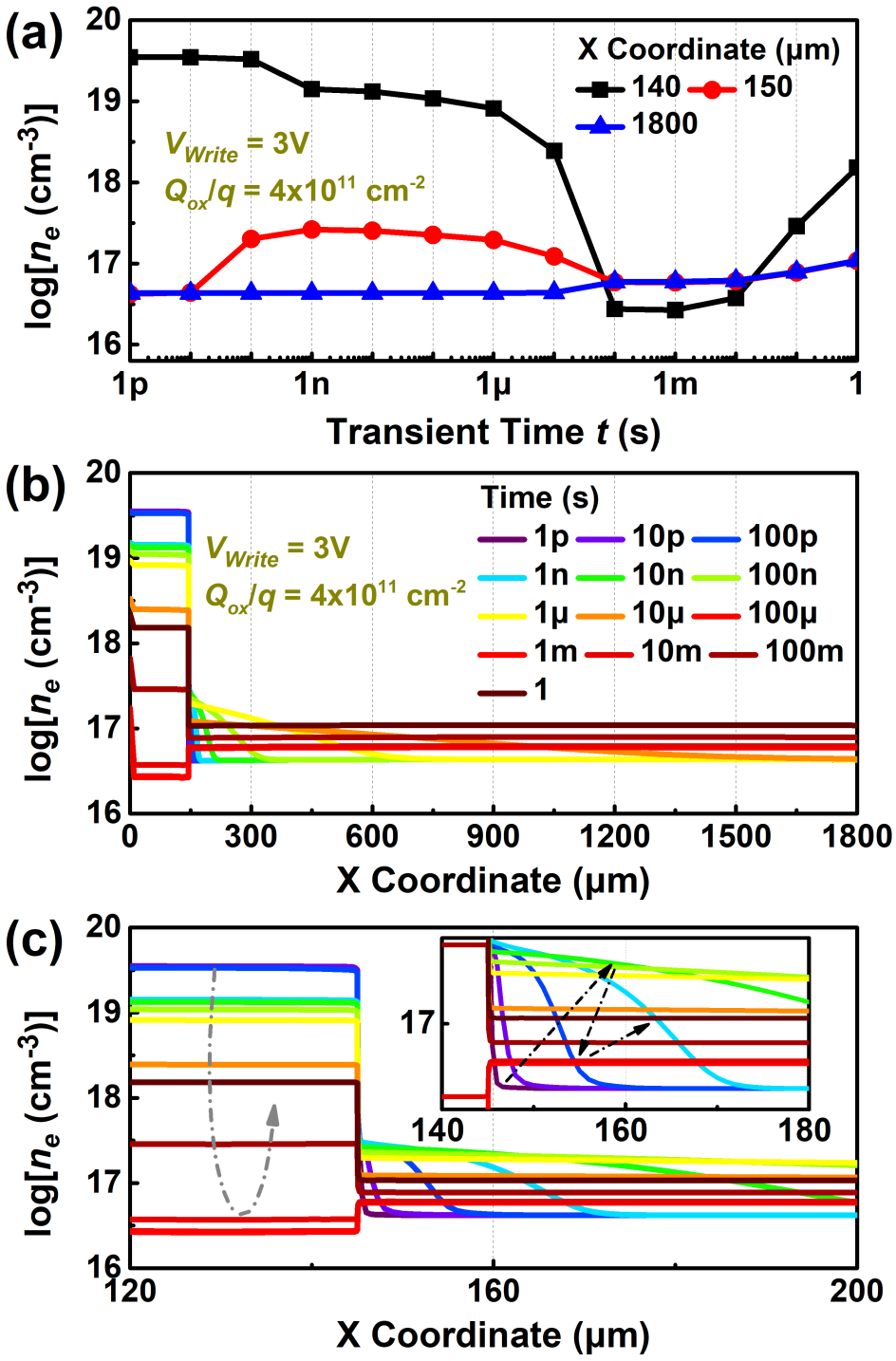

Figure A–14. (a) Time evolution of the electron densities at 2 nm from the silicon surface at x = 140, 150, and 1800 μm, for $Q_{ox}/q = 4 \times 10^{11}$ cm^{-2} under V_{Write} = 3 V. (b) Time evolution of the lateral distribution of the electron densities of the same scenario. (c) Enlargement of (b) near the gate edge. Inset: Further enlargement of (c).

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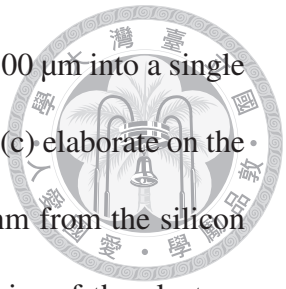

This figure amalgamates the electron densities at x = 140, 150, and 1800 μm into a single panel for comprehensive analysis. Additionally, **Figure A–14** (b) and (c) elaborate on the lateral spatial distribution of the electron density n_e at a depth of 2 nm from the silicon surface. These figures conspicuously illustrate the turnaround behavior of the electron density across different spatial locations.

The clear observation of electron density's turnaround behavior in these figures not only corroborates the discussed mechanisms of electron deficiency and its compensation but also visually represents the complex interplay between electron generation, lateral diffusion, and recombination processes within the device. Such detailed visualization aids in understanding the nuanced electron dynamics contributing to the unusual phenomenon of a negative $-I_{Read}$ at millisecond time scales in devices with substantial oxide charges, under high write voltages.

Direct evidence of the generation process occurring within the silicon is captured in **Figure A–15**, which illustrates the lateral spatial distribution of the recombination rate at a depth of 0.1 μm from the silicon surface. It is important to note that a negative recombination rate in this context actually indicates the generation rate. Observations from this figure reveal that for $t < 100$ μs, significant recombination takes place both under the gate and outside the gate near the gate edge. This is attributed to the presence of excess electrons in these areas, which overcomes the generation process occurring farther outside the gate, where there is an electron deficiency, ultimately leading to an overall influx of holes and thus positive hole currents.

However, for $t > 100$ μs, the scenario shifts to a predominant generation process across the entire observed area, exhibiting almost uniform strength. This uniform generation pro-

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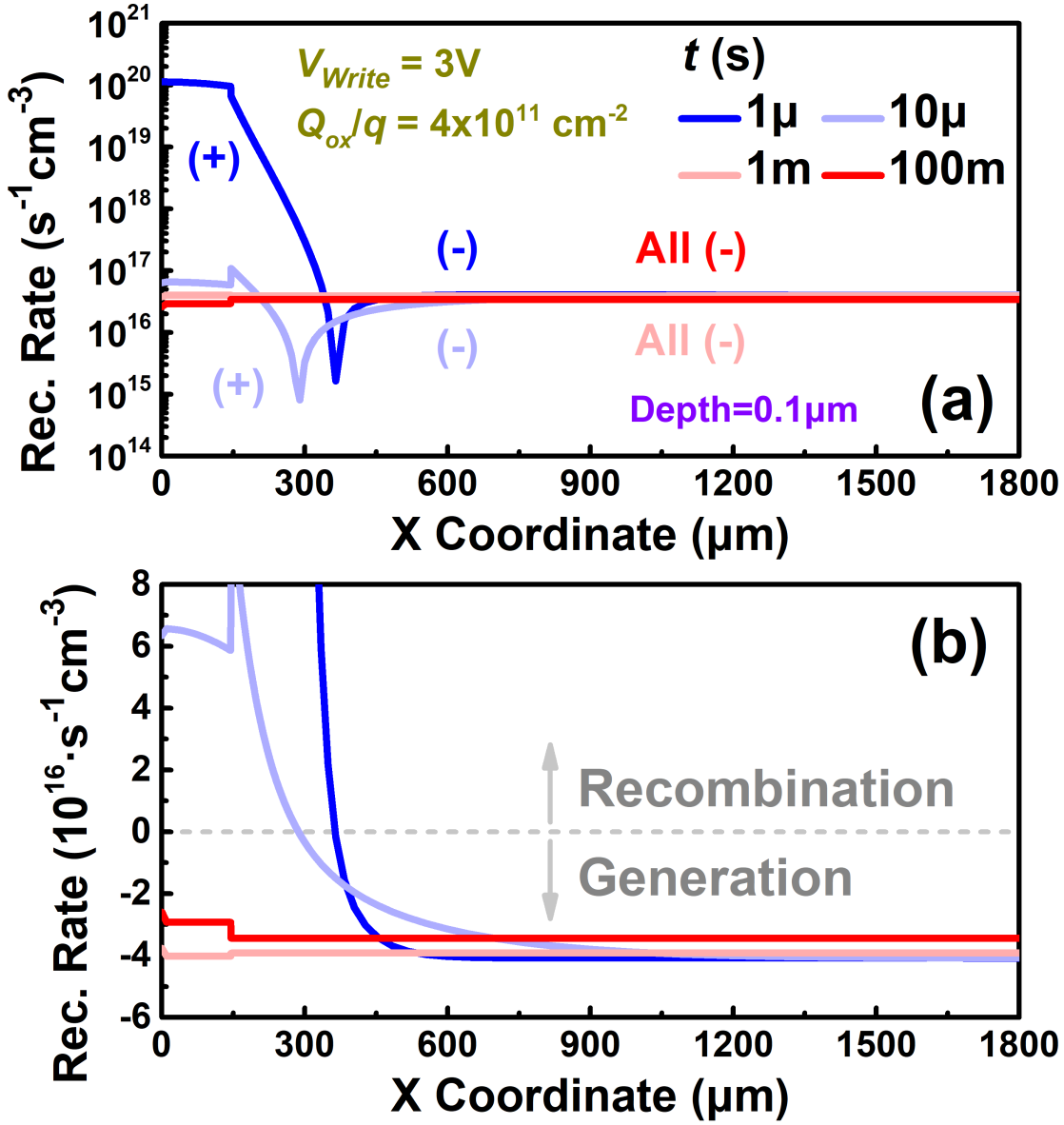

Figure A–15. Lateral spatial distribution of the recombination rate inside the silicon at the depth of 0.1 μm from the surface in the (a) log scale and (b) linear scale for $Q_{ox}/q = 4 \times 10^{11}$ cm^{-2} under $V_{Write} = 3$ V, for transient time t at 1 μs, 10 μs, 1 ms, and 100 ms.

cess signifies that the observed negative substrate hole current arises from a pronounced generation process within the extended depletion region. This generation process contributes to the unique phenomenon observed in devices with substantial oxide charges under higher write voltages, where a reversed transient current direction, manifesting as

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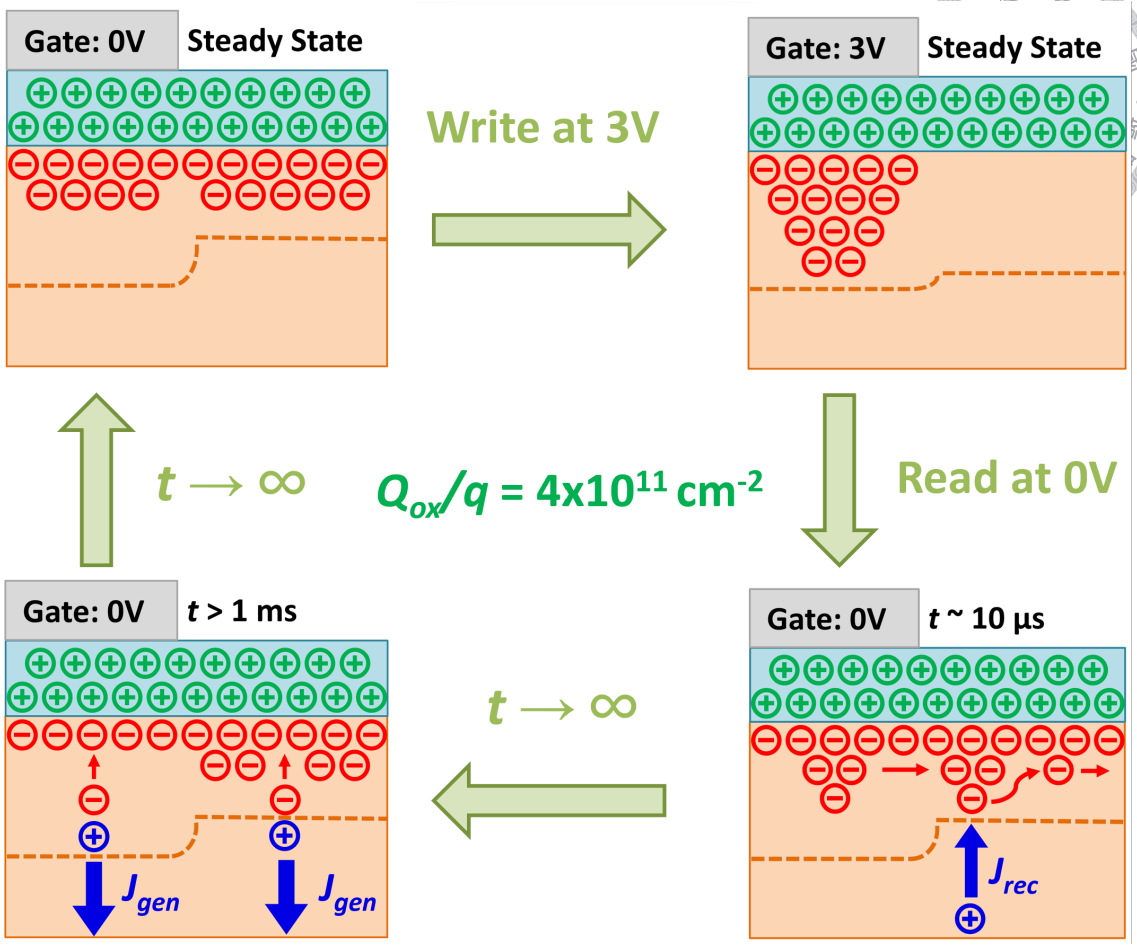

Figure A–16. Schematics illustrating the discharge mechanism of the excess electrons for the device with $Q_{ox}/q = 4 \times 10^{11}$ cm^{-2} switching from 3 V.

negative $-I_{Read}$, emerges at millisecond time scales due to the dominance of electron generation over recombination in the extended depletion regions.

The mechanism behind the reversed transient current direction in devices with substantial oxide charges under a high write voltage is concisely depicted in **Figure A–16**. Here is a brief overview of this mechanism:

- During the write process, inversion electrons induced by oxide charges outside the gate are drawn towards and accumulate beneath the gate.

- Upon switching the gate voltage to 0 V, excess electrons initially stored beneath the

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gate begin to diffuse laterally outwards at the microseconds time scale, aiming to compensate for the electron deficiency outside the gate.

- Regions experiencing an excess of electrons also undergo a temporary recombination process. However, the quantity of stored excess electrons proves insufficient to counterbalance the electron deficiency outside the gate. Furthermore, the excessive outward diffusion of electrons results in an additional electron deficiency beneath the gate.

- Consequently, at the milliseconds time scales, a generation process is initiated to address the electron deficiencies both under and outside the gate, resulting in a negative substrate hole current. This current becomes the dominant component of the substrate total current, leading to a negative $-I_{Read}$.

This summarized mechanism elucidates how the interplay between oxide charges-induced behaviors, lateral electron diffusion, and the generation process contributes to the unconventional transient current response observed in these devices under specific conditions.

The discussions thus far have primarily focused on the analytical results. To complement these discussions, we now present experimental evidence of transient current with a reversed direction. The experimental results are illustrated in **Figure A–17** (a), showcasing a Planar device with an oxide layer with thickness of 31.3 Å, indicative of a high concentration of oxide charges as referenced in [107]. This device was subjected to a write program with a write voltage of 3 V and a write time of 10 ms. Notably, a clear reversal in the direction of the transient current is observed, with $-I_{Read}(t)$ transitioning from positive to negative within tens of milliseconds.

For comparison, simulation results for a device with an oxide layer of 30 Å and $Q_{ox}/q =$

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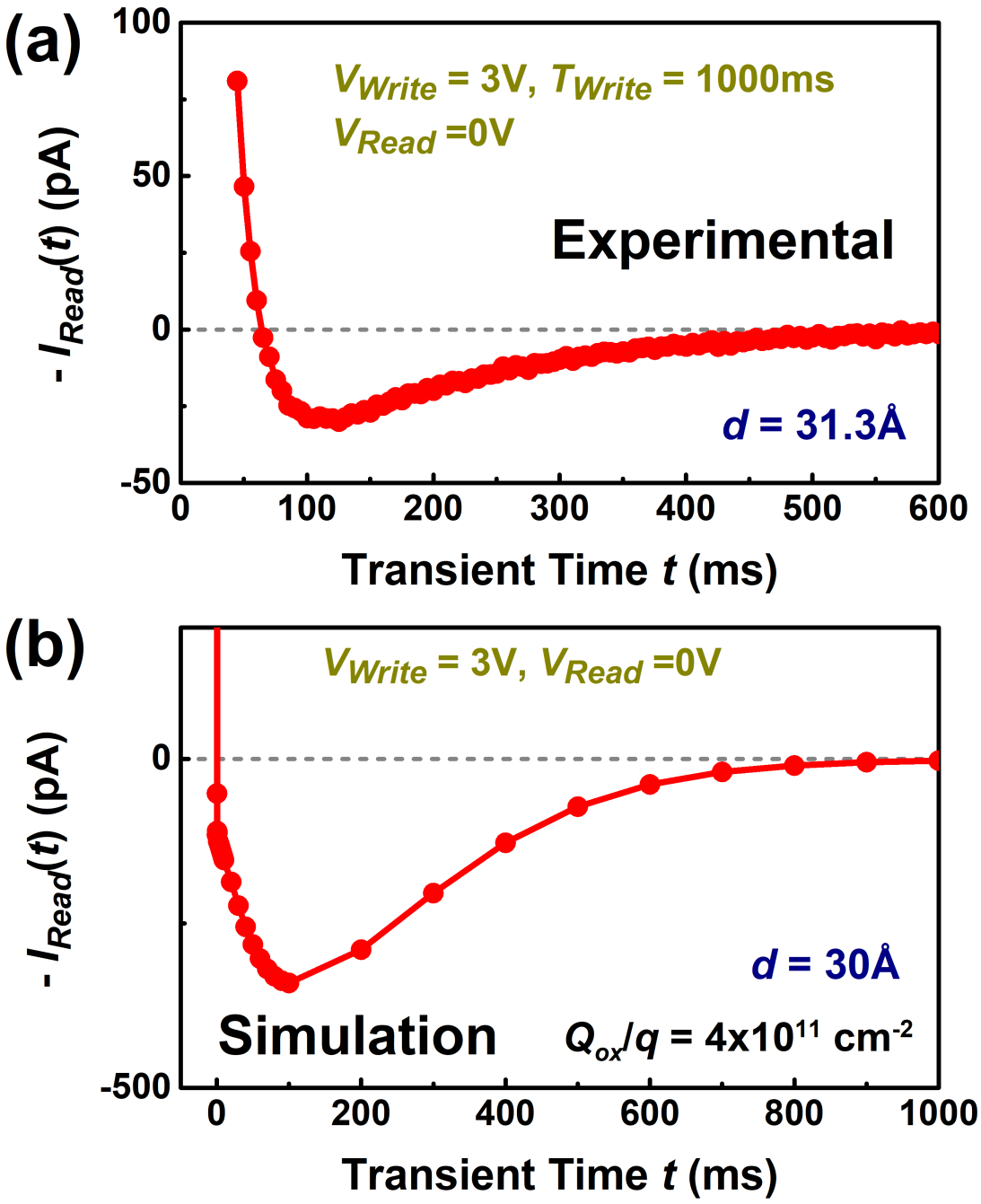

Figure A–17. (a) Experimental results of the transient current ($-I_{Read}(t)$) for the MISTD device with an oxide thickness of 31.3 Å, after a write program with V_{Write} of 3 V and T_{Write} of 1000 ms. (b) Simulation results of $-I_{Read}(t)$ for the device with a 30Å oxide layer and $Q_{ox}/q = 4 \times 10^{11}$ cm^{-2}, switching from a 3 V steady state.

4×10^{11} cm^{-2}, transitioning from a 3 V steady state, are shown in **Figure A–17** (b). Although the exact moment of transient current direction reversal, occurring at several hun-

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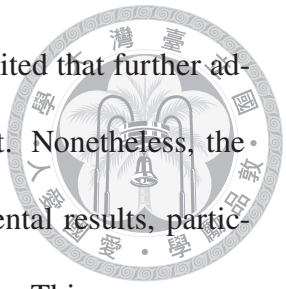

dred microseconds, differs from the experimental timeframe, it is posited that further adjustments to carriers' lifetime parameters could refine this alignment. Nonetheless, the simulated transient current exhibits a similar pattern to the experimental results, particularly regarding the occurrence of reversed transient current direction. This congruence between experimental and simulated data reinforces the understanding of the mechanisms leading to this unique behavior and suggests avenues for further refinement of the simulation model to achieve closer correspondence with empirical observations.

A.4 Summary

In this appendix, we have delved into the transient current behavior in Planar MISTDs with oxide charges. Our discussion centered on elucidating two principal observations:

- **Decrease in Transient Current Magnitude with Increased Oxide Charges (Q_{ox}/q):** We observed that a rise in the number density of oxide charges leads to a diminished magnitude of transient current at millisecond time scales ($-I_{Read}$). This phenomenon is ascribed to the lateral diffusion of excess electrons outward from the gate area. These electrons then undergo substantial recombination during the microsecond time scales within the extended depletion region, explaining the reduction in transient current magnitude.

- **Reversed Transient Current Direction for Devices with Substantial Oxide Charges Under High Write Voltage:** In devices with a high concentration of oxide charges and subjected to a high write voltage, we noted a reversal in the transient current direction. This reversal stems from a pronounced electron deficiency outside the gate, caused as the inversion electrons, induced by oxide charges, are drawn beneath the

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gate. The inability of the excess electrons stored beneath the gate to compensate for this deficiency during the microsecond time scales necessitates electron generation at the millisecond time scales. This process ultimately results in the observed reversal of the transient current direction.

Through detailed analysis and comparison of simulation and experimental data, these insights underscore the complex interplay between oxide charges, lateral electron diffusion, and electron generation/recombination processes in influencing the transient current characteristics of Planar MISTDs under varying conditions.

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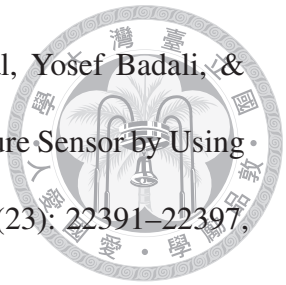

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