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Doctoral Dissertation

二維材料堆疊結構在電晶體及記憶體之應用研究

Stacked Structures of 2D Materials for Transistor and Memory Applications

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本論文係 蔡柏政君（D07943004）在國立臺灣大學電子工程學研究所完成之博士學位論文，於民國111年8月25日承下列考試委員審查通過及口試及格，特此證明。

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博士班的畢業不是結束而是真正的開始，進入職場沒有容錯的空間，在學期間遇到困難亦或犯錯都可以重新來過審視錯誤並在錯誤中學習，已經畢業的學長學弟們都在各自的領域有所發展，接著換我要邁向人生另一個階段，期許自己能在未來有所展現，祝福所有人一切順心。

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摘要

本論文研究目標著重在二維材料的成長及元件製作分析、異質結構 (Hetero-structure) 與平面式閘極電晶體 (In-plane Gate Transistor, IPGT) 應用，主要研究材料為石墨烯 (Graphene) 、過渡金屬二硫化物的二硫化鉬(MoS_2) 以及二硫化鎢(WS_2)。傳統化學氣相沉積法成長二維材料，需將過渡金屬和硫族元素的兩種前驅物同時放置於高溫爐管中反應，化學反應極其複雜，此外由於二維材料成長溫度相當高，異質結構薄膜製備不易，我們利用原子層沉積、熱蒸鍍、射頻濺鍍等方式提供過渡金屬氧化物薄膜，結合高溫爐管的硫化過程，我們成功製備出大面積石墨烯和二硫化鉬、二硫化鎢薄膜。我們在研究過程中發現由於缺乏斷鍵，二維材料表面不利於原子層沉積之前驅物分布，藉由調整前驅物靜置時間在二維材料表面形成成核點有利於原子層沉積，利用此方式在二硫化鉬表面成長 5 nm 氧化鋁做為間隔層並轉印同質材料 MoS_2 以增強螢光光譜發光強度或是異質材料 WS_2 形成雙波段螢光發光結構。我們並將石墨烯直接成長於藍寶石基板上，再使用熱蒸鍍取代射頻濺鍍提供過渡金屬氧化物薄膜來成長過渡金屬二硫化物，避免濺鍍時氬離子轟擊底層材料造成破壞，使用此成長方式製備成二硫化鉬/石墨烯電晶體元件。以二硫化鉬做為表面鈍化層則可提升石墨烯電晶體之電流和載子遷移率。若使用原子層蝕刻技術將上層二硫化鉬孤立做為電荷儲存層，此異質結構之元件便會出現遲滯現象可做為記憶體元件應用。為了探討電荷儲存於二硫化鉬之現象，我們以三層二硫化鉬並使用原子層蝕刻技術將電極下方二硫化鉬蝕刻使通道中的二硫化鉬孤立做為電荷儲存層，我們發現隨著孤立層數增加其遲滯曲線亦會增加。此外為了避免氧化物與通道接觸會使得石墨稀上閘極電晶體的特性下降，我們藉由電子束微影製作出石墨烯平面式閘極電晶體，此元件無須使用氧化物介電層便可對石墨烯通道的電流進行調制並大幅提升石墨烯電晶體的元件特性。

關鍵字：二維材料、平面式閘極電晶體、場效電晶體、記憶體、原子層蝕刻

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Abstract

The thesis is focused on the fabrication of 2-D materials, and their hetero-structures for device applications. The main research materials are graphene and transition metal disulfides, such as MoS_2 and WS_2. By using the conventional chemical vapor deposition, the growth of 2-D materials requires two precursors of transition metals and chalcogenides. Considering the thin-body nature of 2-D materials, it is difficult to achieve precise control over the growth parameters. On the other hand, high growth temperatures are usually required for 2-D material growth, which will make it difficult to establish epitaxially grown 2-D material hetero-structures. Therefore, we have adopted atomic layer deposition (ALD), thermal evaporation, and radio frequency sputtering (RF sputtering) to provide transition metal oxide films. Combined with the sulfurization procedure in a hot furnace, we have successfully demonstrated large-area graphene, molybdenum disulfide and tungsten disulfide growth. Since there are no dangling bonds, direct oxide growth by using ALD is difficult on 2-D material surfaces. We have demonstrated that a thin 5 nm Al_2O_3 dielectric layer can be grown on the MoS_2 surface by using ALD with an additional precursor soaking time. With the thin oxide separation layer between two mono-layer 2-D materials, luminescence enhancement is observed by transferring a mono-layer MoS_2 film onto the sample, while dual color emission can be

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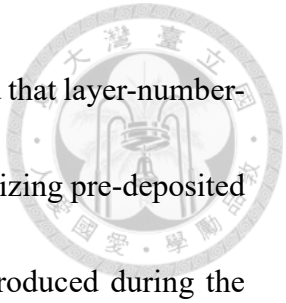

observed by transferring mono-layer WS_2. We have also demonstrated that layer-number-controllable MoS_2 films can be grown on graphene surfaces by sulfurizing pre-deposited MoO_3 films by using the thermal evaporator. With no damages introduced during the growth procedure, significant device performance enhancement is observed for the top-gate graphene transistors with the MoS_2 passivation layer. By using the atomic layer etching (ALE) procedure to isolate the topmost MoS_2 layer from the graphene channel, a memory architecture based on the MoS_2/graphene hetero-structure is proposed. With the semiconducting 2-D material (MoS_2) as the charge separation layer and the conductive counterpart (graphene) as the channel layer, a top-gate transistor can be operated as a memory device. The long retention times and increasing current ratios between "1" and "0" states with increasing isolated MoS_2 layer numbers have revealed the potential of 2-D materials for memory device applications. The same concept is also applied to multi-layer MoS_2 with the isolated MoS_2 layers as the charge storage layer and the underneath MoS2 layers as the channel. On the other hand, by using the electron beam lithography, the in-plane gate transistor architecture provides an alternate approach for the fabrication of 2-D transistors with reduced interfaces with other materials and the channel is modulated by electric field laterally.

Key words – 2-D material, In-plane gate transistor, Field effect transistor, Memory, Atomic layer etching,

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Chapter 1 Introduction

1.1 The Challenge of CMOS Scaling

The semiconductor industry has been rapidly developed over the past few decades. In 1958, the first integrated circuit (IC) was invented by Jack Kilby, which was fabricated by using germanium. At the same time, the integrated circuit was demonstrated via a planar technology in silicon by Robert Noyce. The first metal-oxide-semiconductor field-effect transistor (MOSFET) came out at 1960, which used SiO_2 as the gate insulator for transistors. In nowadays semiconductor industry, it is important to further improve the performances of ICs by reducing the linewidths of transistors. The International Technology Roadmap for Semiconductor (ITRS) provides a roadmap for future device architecture with reduced line widths. For example, it is predicted that 2.5 nm MOSFET is needed at 2023 [1]. Their main projection in the frontend process and the MOSFET is high performance when keeping the low power consumption in the logic circuit. The aim of this Roadmap is to identify key technical requirements to support the historical scaling of CMOS technology, which is known as the “Moore’s law”. It predicts that the number of transistors on an IC increases exponentially, doubling over 18 months in period [2]. The physical gate length scaled down to ~20 nm as the technology node reached 22 nm [3]. The developmental progress leads to today’s electronic devices that present advanced

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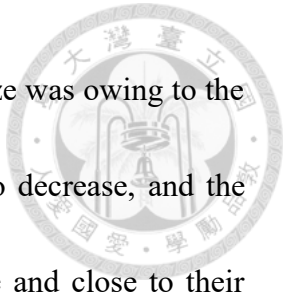

performance with reduced cost per function, and reduced physical size was owing to the device miniaturization. The size of the electron device continues to decrease, and the obstacles of traditional silicon-based processes continue to increase and close to their physical limit. Si CMOS scaling need to overcome two fundamental problems: (1) The decreasing charge mobilities in ultra-thin channels like, nano-sheets, nano-wires or fins introduced to maximize electrostatic control at scaled dimensions and (2) a slow V_{dd} downscaling dictated by the 60mV/dec thermal limit. The limitations can be overcome by replacing the channel materials and device design. It is an urgent issue that we need to find a new material to replace silicon and let Moore's Law continue [4,5]. Due to the atomic thickness of 2-D materials, they are considered as a possible candidate to replace silicon in advanced technology nodes. The 2-D material can offer high device performances at nm dimensions. Such as transition metal dichalcogenides (TMDs) family, molybdenum disulfide (MoS_2), is an explosion in research activities due to its potential applications in various electronic and optoelectronic devices. Although the conventional bulk semiconductors, such as germanium and silicon, can also be made very thin, 2-D semiconductors own extra advantages, such as atomically smooth surfaces without dangling bonds [6]. The consistent and fixed thicknesses in numbers of atomic layers, as schematically shown in Figure 1-1 (a) and (b). The advantages can suppress the trap generation, carrier scattering, and thickness variation which can guarantee devices with

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high performance. On the other hand, as shown in Figure 1-1 (c), mobility degradation will be observed for silicon with thickness scaling, while the trend is much slower for MoS_2, which will lead to a high mobility value at the extremely thin thickness down to mono-layers of MoS_2. Several theoretical works [7-10] have also been carried out to evaluate the scalability of monolayer/multilayer 2-D FETs on semiconductor-on-insulator (SOI) and double-gate (DG) FET, as schematically shown in Figure 1-1 (d). It has recently been reported that MoS_2 suffers from remote phonon scattering in high-k dielectric environment and has an intrinsic phonon limited room-temperature mobility of ~60 $cm^2/V \cdot s$ [11]. The study suggested that 2-D materials, with TMDs as the best candidate for transistor applications. In Figure 1-2, the MoS_2 and WS_2 could meet N3 performance requirements with an improved energy consumption compared to Si-FinFETs [5]. These results have demonstrated that 2-D materials are promising candidates to replace Si in the advanced technology nodes.

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Year of Production	2013	2015	2017	2019	2021	2023	2025	2028
Logic Industry "Node Name" Label	"16/14"	"10"	"7"	"5"	"3.5"	"2.5"	"1.8"	
Logic ½ Pitch (nm)	40	32	25	20	16	13	10	7
Flash ½ Pitch [2D] (nm)	18	15	13	11	9	8	8	8
DRAM ½ Pitch (nm)	28	24	20	17	14	12	10	7.7
FinFET Fin Half-pitch (new) (nm)	30	24	19	15	12	9.5	7.5	5.3
FinFET Fin Width (new) (nm)	7.6	7.2	6.8	6.4	6.1	5.7	5.4	5.0
6-t SRAM Cell Size(um2) [@60f2]	0.096	0.061	0.038	0.024	0.015	0.010	0.0060	0.0030
MPU/ASIC HighPerf 4t NAND Gate Size(um2)	0.248	0.157	0.099	0.062	0.039	0.025	0.018	0.009
4-input NAND Gate Density (Kgates/mm) [@155f2]	4.03E+03	6.37E+03	1.01E+04	1.61E+04	2.55E+04	4.05E+04	6.42E+04	1.28E+05
Flash Generations Label (bits per chip) (SLC/MLC)	64G /128G	128G /256G	256G / 512G	512G / 1T	512G / 1T	1T / 2T	2T / 4T	4T / 8T
Flash 3D Number of Layer targets (at relaxed Poly half pitch)	16-32	16-32	16-32	32-64	48-96	64-128	96-192	192-384
Flash 3D Layer half-pitch targets (nm)	64nm	54nm	45nm	30nm	28nm	27nm	25nm	22nm
DRAM Generations Label (bits per chip)	4G	8G	8G	16G	32G	32G	32G	32G
450mm Production High Volume Manufacturing Begins (100Kwspm)				2018				
Vdd (High Performance, high Vdd transistors)[**]	0.86	0.83	0.80	0.77	0.74	0.71	0.68	0.64
1/(CVI) (1/psec) [**]	1.13	1.53	1.75	1.97	2.10	2.29	2.52	3.17
On-chip local clock MPU HP [at 4% CAGR]	5.50	5.95	6.44	6.96	7.53	8.14	8.8	9.9
Maximum number wiring levels [unchanged	13	13	14	14	15	15	16	17
MPU High-Performance (HP) Printed Gate Length (GLpr) (nm) [**]	28	22	18	14	11	9	7	5
MPU High-Performance Physical Gate Length (GLph) (nm) [**]	20	17	14	12	10	8	7	5
ASIC/Low Standby Power (LP) Physical Gate Length (nm) (GLph)[**]	23	19	16	13	11	9	8	6

Table 1-1 Summary Table of 2013 ITRS Technology Trend Targets (Table taken from International Technology Roadmap for Semiconductors 2013 [1])

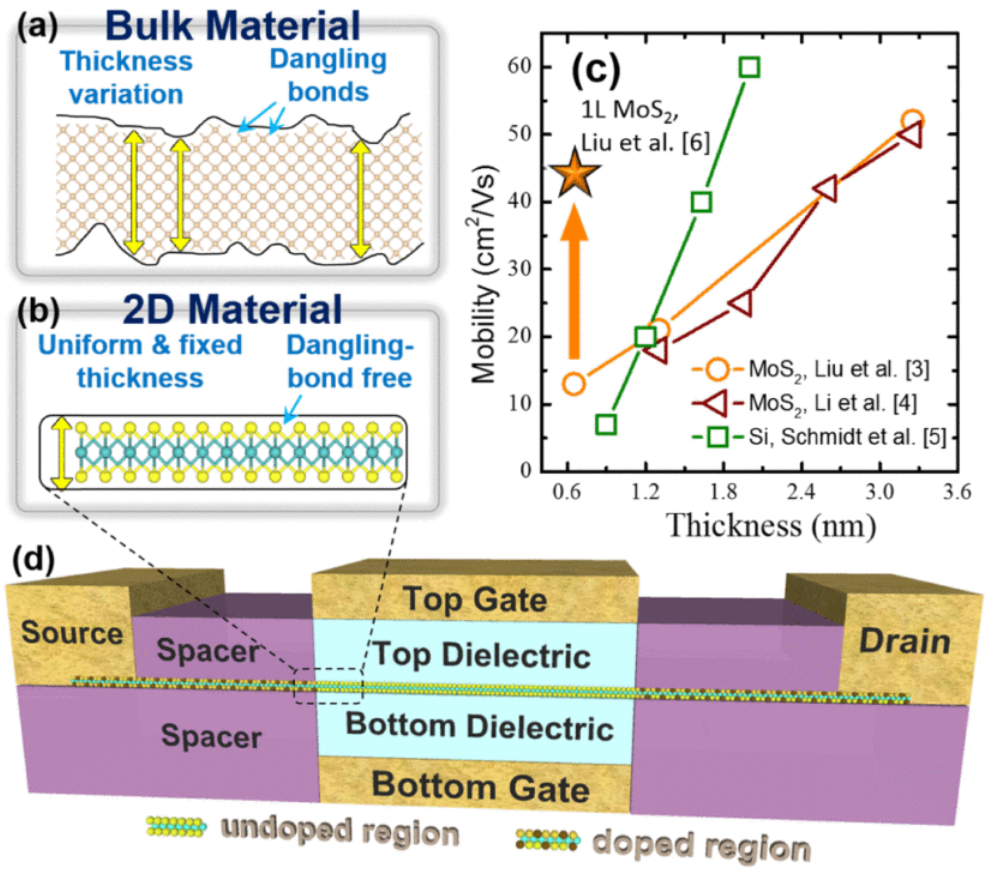

Figure 1-1 (a) Issues of bulk material during thickness scaling for FET application. (b) Advantages of 2-D materials. (c) Carrier mobility degradation with reduced material thickness for MoS_2 and Silicon. (d) Schematic of a Dual Gate 2-D FET. [6]

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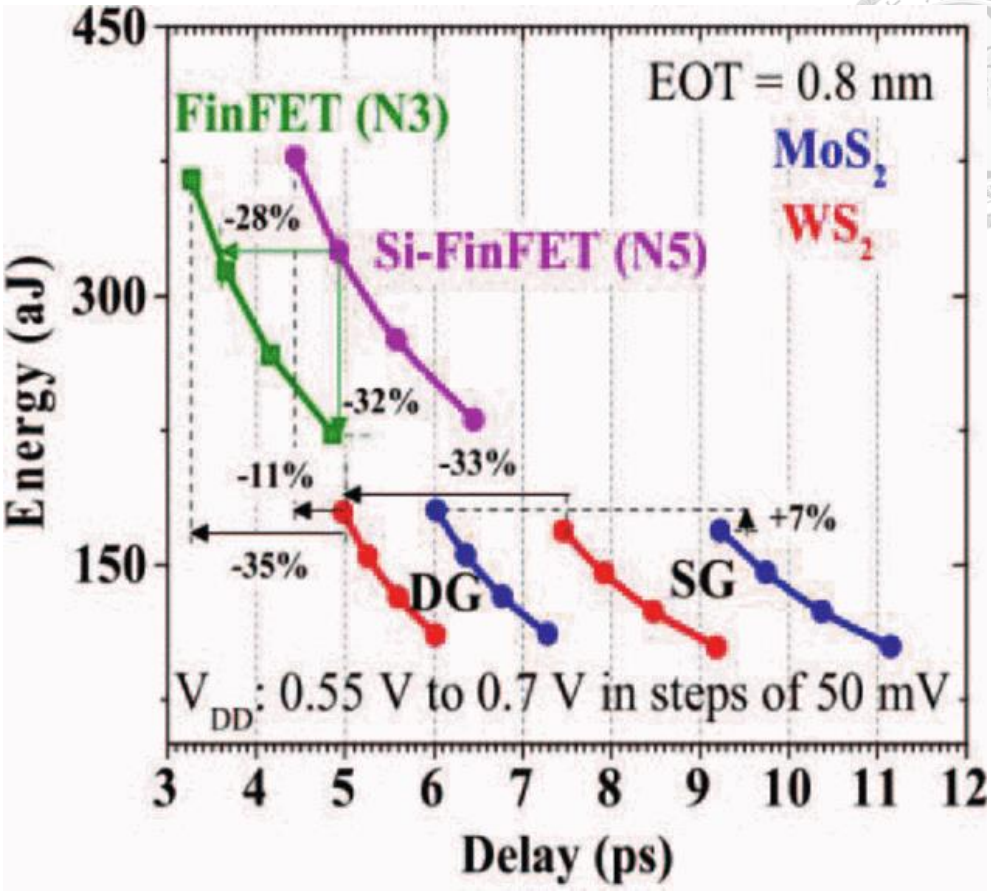

Figure 1-2 Energy delay comparison of Single Gate, Double Gate MX_2 FETs and Si FinFET for fixed wire load with N5 technology assumptions, computed using effective capacitance and ON current [5].

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1.2 The evolution of 2-D material researches

Graphene is a sheet of a monolayer carbon atoms, bounded in a hexagonal honeycomb lattice structure. It is an allotrope of carbon atoms in sp^2-bonded. Graphene can be wrapped up into fullerene (zero-dimensional (0D)). The carbon atom is rolled up into carbon nanotube (one-dimensional (1D)) and stacked on top of each other to form graphite (three-dimensional (3D)), with an interplanar spacing of 0.335nm [12, 13]. The 2-D crystal graphene was discovered in 2004. With a covalently-bonded hexagonal lattice of carbon atoms and one atom thickness (~0.14 nm), the Dirac-cone band structure of graphene indicates that carriers can move through the material at very high speeds, giving it fascinating properties such as unparalleled thermal conductivity and high carrier mobility(~23000 $cm^2/V \cdot s$) [14]. Graphene has many outstanding properties in terms of optical transparency. Benefiting from one atomic thickness, graphene has very high transparency of 97.7% in visible light. It only absorbs 2.3% of visible light in single layer graphene. The absorption, as well as a single layer and bilayer graphene, are both 2.3%, and the transparency of graphene becomes effective indication of the numbers of the graphene layer, which is confirmed by simulations using Dirac fermions with Fermi's golden rule [15]. The theoretical and experimental results both suggest that graphene has excellent optical properties. Combined with its high conductivity, graphene becomes a

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very competitive transparent conductive thin film that could potentially replace many traditional transparent films, such as indium tin oxide (ITO), and fluorine-doped tin oxide (FTO). Another application for graphene high conductive, graphene for interconnects within a 7-nm FinFET technology. The resistivity dependence on line width < 40 nm for copper (Cu) and doped graphene, where the graphene resistivity is lower than Cu [16]. Due to its wide absorption spectral, short carrier lifetime, and high conductivity, graphene has promising for optical devices. These unique properties and potential of graphene have attracted huge research efforts around the world.

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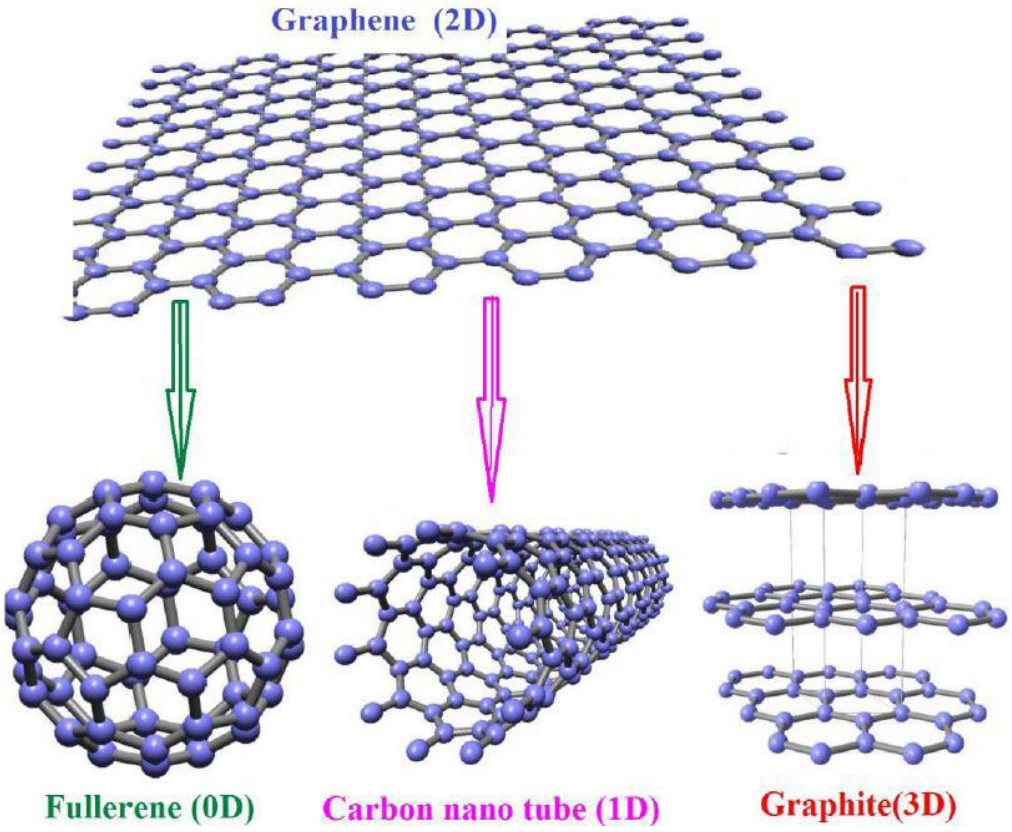

Figure 1-4 The Graphene and related structures [12].

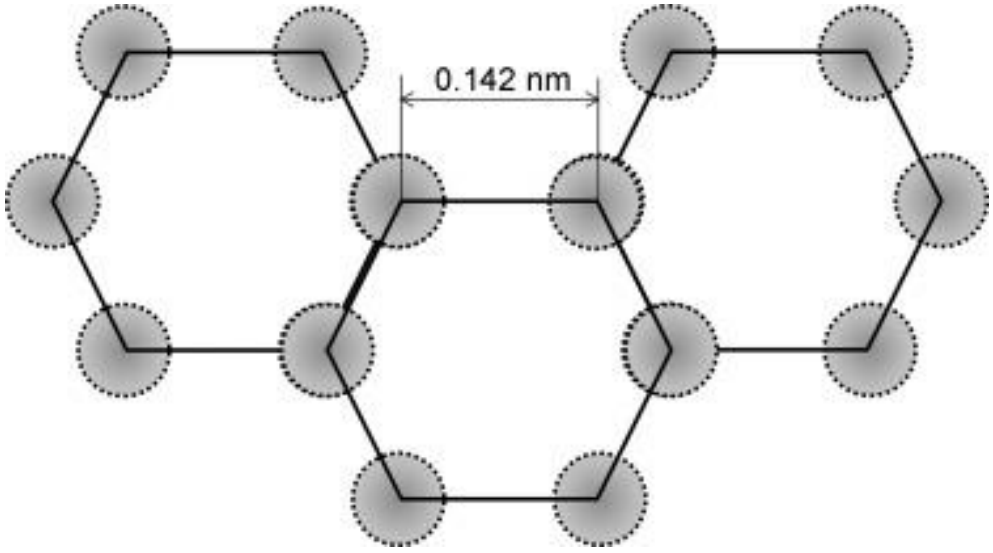

Figure 1-3 The hexagonal lattice of graphene [13].

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As the first discovered 2-D material, graphene is believed to be of potential application for high-speed electronics in the < 10 nm technology node with the advantage of theoretically predicated ultra-high carrier mobility values [17]. However, graphene is of zero bandgap in its nature. Therefore, there is no OFF state for graphene transistors, which would lead to low ON/OFF ratios for the device. To overcome this disadvantage of graphene, people have turned their focus on other 2-D materials with bandgaps such as transition metal dichalcogenides (TMDs) for the transistor application in recent years. TMDs is well-known in the 2-D material family. TMDs has the general chemical formula MX_2, where M is a transition metal (M = W, Mo, etc.) and X is a group VI atom (X = Te, S, or Se). Compared with graphene, TMDs are with visible bandgap values changing with their layer numbers [18,19]. The band gap values for monolayer MoS_2, $MoSe_2$, WS_2,and WSe_2, direct band gaps are 1.88 eV, 1.57 eV, 2.03 eV, 1.67 eV respectively, and for bulk TMDs, indirect band gaps of 1.23 eV (MoS_2), 1.09 eV ($MoSe_2$), 1.32 eV (WS_2), 1.21 eV (WSe_2) are predicted [20]. Among all the candidates in the TMDs family, one of the most promising materials for device applications is MoS_2. The crystal lattice is a sandwich structure, where the transition metal atoms are surrounded by the group VI atoms. TMDs has three main type phases: Octahedral (1T), Trigonal prismatic (2H), and Trigonal prismatic (3R) as shown in Figure 1-5 [21]. The first mono-layer molybdenum disulfide (MoS_2) transistor was fabricated by Radisavlievic et al. at 2011 [22]. Since mono-layer

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MoS_2 is of direct bandgap value 1.88 eV, the 2-D material transistor can be turned off by using MoS_2 as the channel. On the other hand, the MoS_2 transistors with a 1-nm physical gate length was also demonstrated by using a single-walled carbon nanotube as the gate electrode. The ultrashort devices has demonstrated excellent switching characteristics with the subthreshold swing ~65 millivolts per decade and an On/Off current ratio ~10^6 [23].

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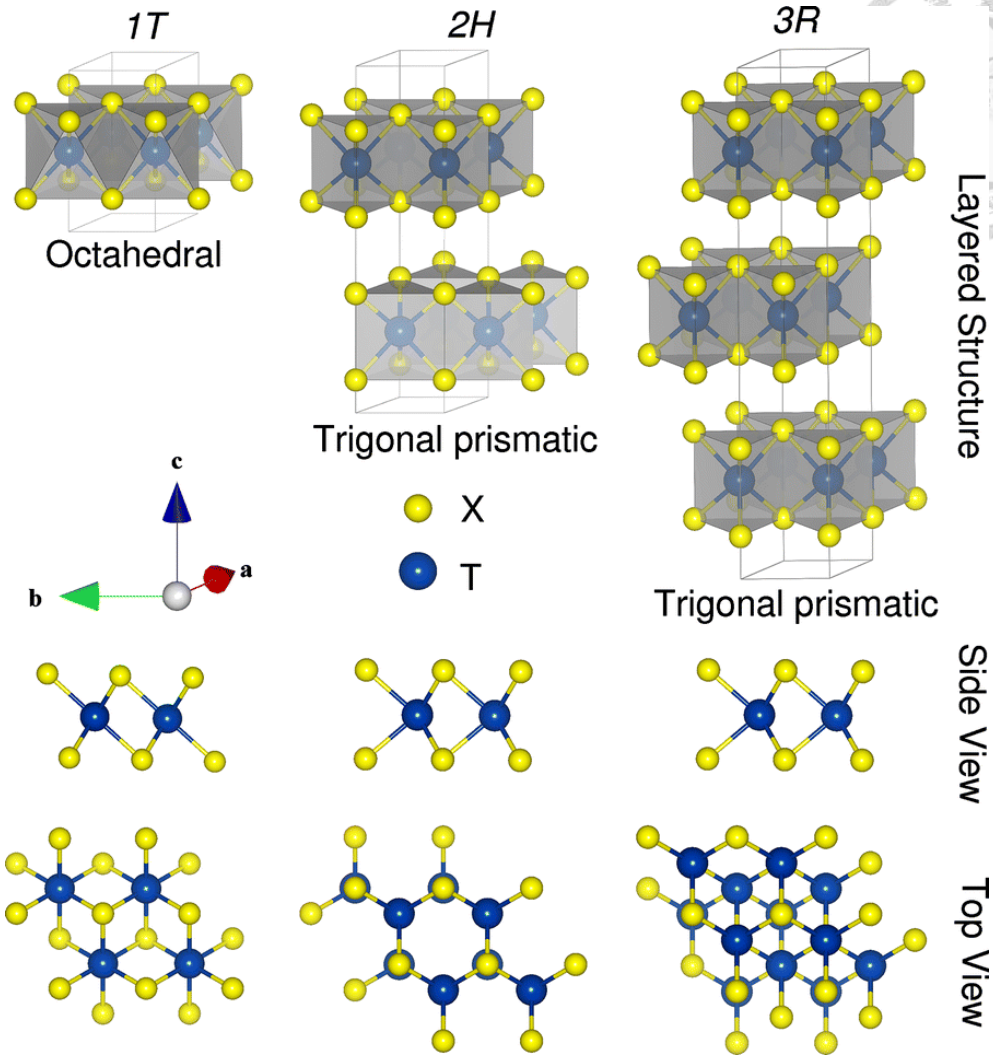

Figure 1-5 Structural of 1T, 2H, and 3R TMDs and their corresponding metal atoms coordination. The top and side views of layered forms are shown [21].

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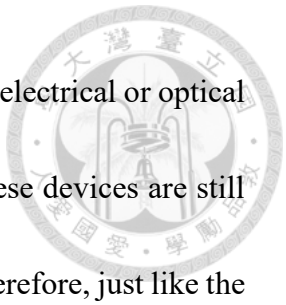

Although 2-D materials have already exhibited their potential in electrical or optical device applications in the nanometer regime, the performances of these devices are still limited by the material characteristics of individual 2-D materials. Therefore, just like the evolution of compound semiconductors, the research trend of 2-D materials has gradually moved from homo- to hetero- junctions of 2-D materials. In most publications, sequential attachment of mechanically exfoliated 2-D materials is often adopted for the establishment of vertical 2-D material hetero-structures [24,25]. The hetero-structure is established by sequentially reattach the films onto each other on a given substrate, such as SiO_2/Si substrates. Although this method has been proved to be an easy and functional approach, the possible chemical contamination between layers and undefined film area would limit the practical applications of the 2-D material hetero-structures. Furthermore, the voids and wrinkles introduced during the transferring procedure might also influence the device performance. Therefore, epitaxially grown 2-D materials onto other 2-D material layers has strong potential for fabricating such hetero-structures. In one previous publication, it has been demonstrated that homo-junctions of MoS_2 can be grown directly on sapphire substrates through repeating the same CVD cycles. 2-, 4- and 6- layer MoS_2 can be prepared after 1-, 2- and 3- CVD growth cycles [26]. The epitaxially grown multi-layer MoS_2 films actually marks the beginning of van der Waals epitaxy on 2-D material surfaces show in Figure 1-6.

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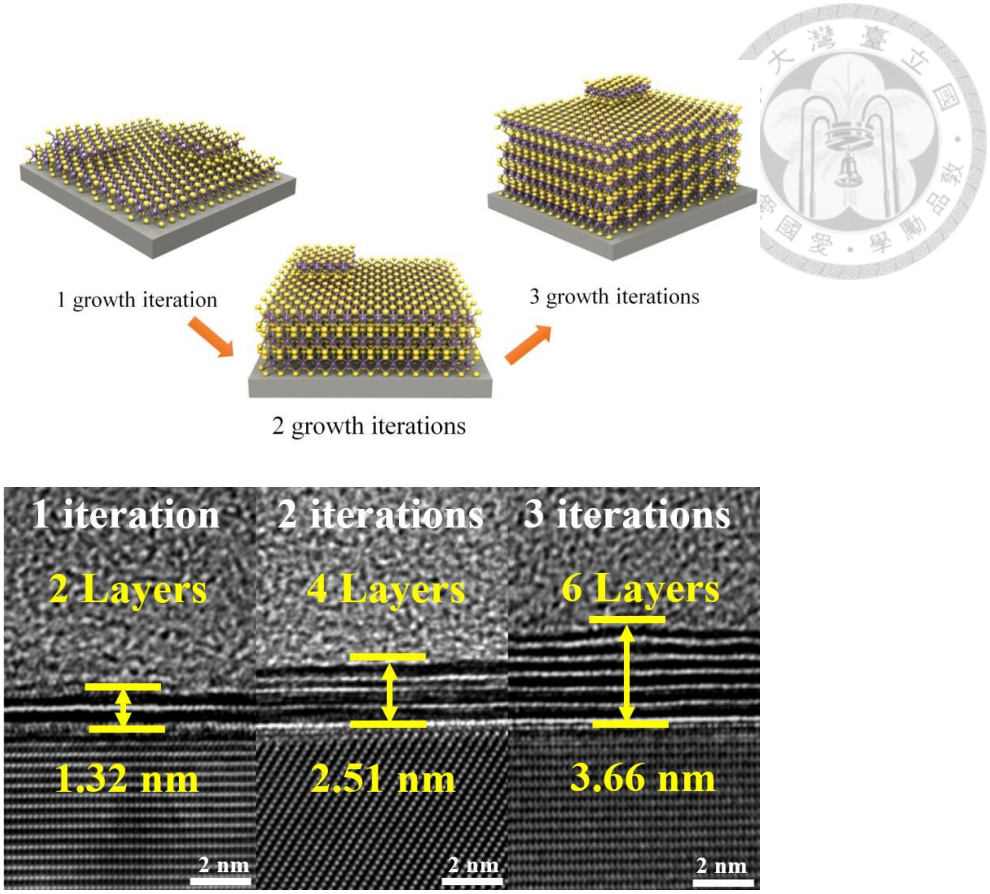

Figure 1-6 The growth procedures of repeated CVD growth cycles with one, two and three separate growth iterations (left) and the cross-sectional HRTEM images of the three samples (right) [26].

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For the preparation of vertical 2-D material hetero-structures, chemical vapor deposition (CVD) can be a ready access for this purpose. However, for the preparation of different 2-D materials for hetero-structure establishment, different precursors have to be adopted. Growth optimization is required for each 2-D material. The more complicated growth procedures are disadvantageous for the establishment of multiple 2-D material hetero-structures. Therefore, if a standard growth procedure can be applied to different 2-D material growth, the establishment of 2-D material hetero-structures would become much easier and promising for practical applications. In another previous publication, it has been demonstrated that both scalable WS_2 and MoS_2 films with good layer number controllability can be prepared by sulfurizing pre-deposited W and Mo films show in Figure 1-7 [27]. With the same sulfurization procedure, scalable WS_2/MoS_2 hetero-structures can be prepared. Compared with MoS_2 transistors, the enhanced field-effect mobility values of the WS_2/MoS_2 hetero-structure transistor have demonstrated that improved device performances can be obtained with well-designed 2-D material hetero-structures. The results have also demonstrated by stacking different 2-Dmaterials, the performances of devices based on these hetero-structures may exceed those with individual 2-D materials. The complexity in wafer structures such as 2-D material hetero-structures will bring additional advantage over the construction of the device architechure. In another publication, it has also been proposed that there are two growth mechanisms

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involved in the sulfurization of pre-deposited MoO_3 films, which are (a) planar TMDs growth and (b) Mo oxide segregation occurred during the sulfurization procedure show in Figure 1-8 [28]. The balance between the planar MoS_2 growth and the Mo oxide segregation is an important issue to obtain a uniform 2-D material films by using this approach.

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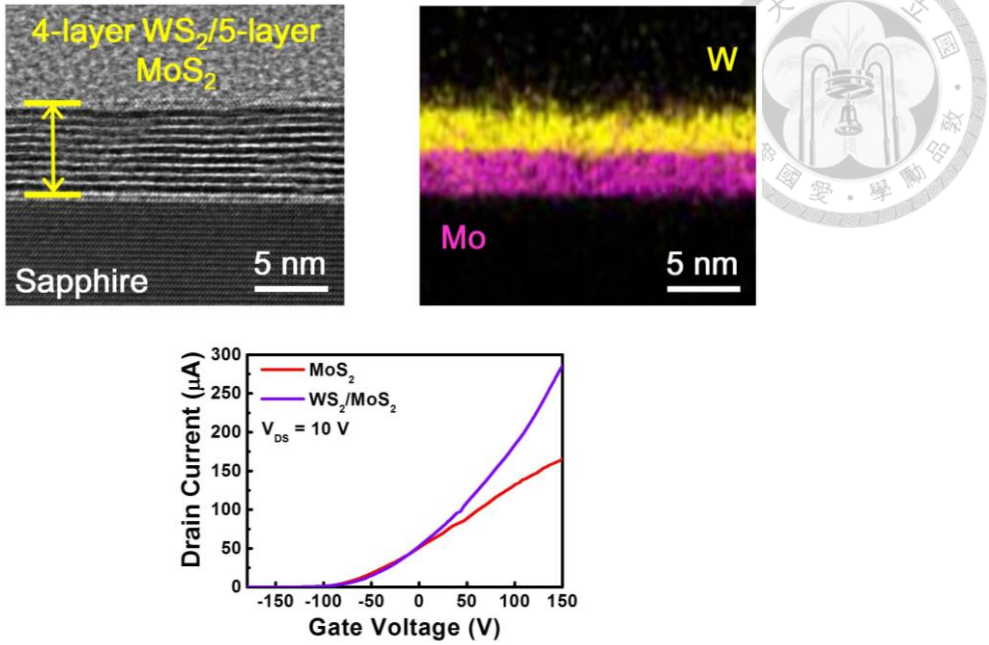

Figure 1-7 The cross-sectional HRTEM image (left) and the HAADF mappings (middle) of Mo and W elements of the MoS_2/WS_2 hetero-structure sample. The I_D-V_{GS} curves of MoS_2 and WS_2/MoS_2 hetero-structure transistors operated at V_{DS} = 10 V [27].

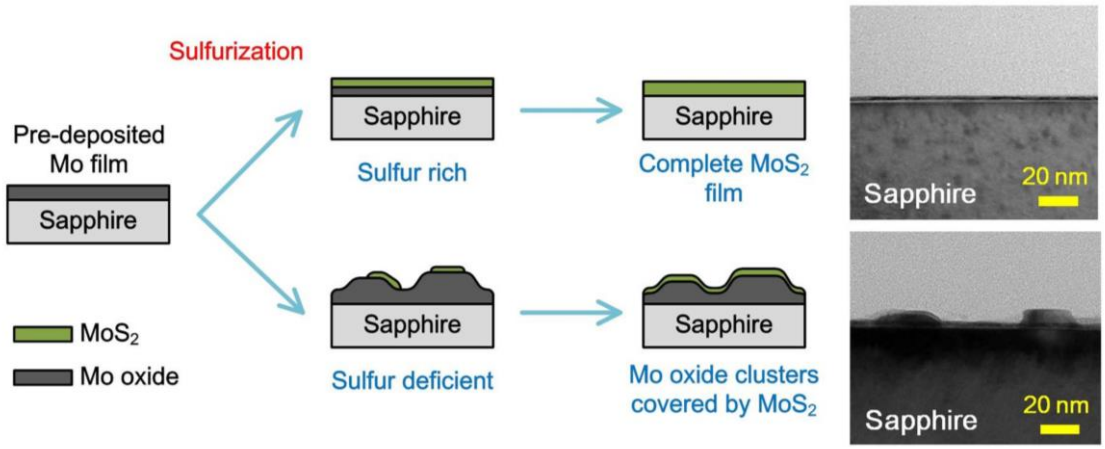

Figure 1-8 The growth mechanisms of the sulfurization of pre-deposited MoO_3 films [28].

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Besides the growth of TMDs hetero-structures, it has been proposed in one publication that MoS_2 can be grown on graphene/Cu via CVD methods [29]. However, only small MoS_2 flakes were observed due to the un-avoidable chemical reactions between the precursors and the metal substrates. For this purpose, we have demonstrated that by using CVD, graphene films can be grown directly on sapphire substrates [30]. Compared with the graphene films grown on copper foils, inferior crystallinity is observed for the graphene films grown directly on sapphire substrates. However, since sapphire is an inert substrate, it is possible to do following 2-D material growth directly on the graphene/sapphire samples. Therefore, it has been demonstrated that layer-number-controllable MoS_2 films can be grown on the graphene surfaces by sulfurizing the pre-deposited Mo films by using a RF sputtering system. Although the Ar plasma adopted during the sputtering deposition procedure may bring potential damage to the underlying graphene films, this method does provide a ready access to establish epitaxially grown 2-D material hetero-structures with different lattice structures and chemical compositions.

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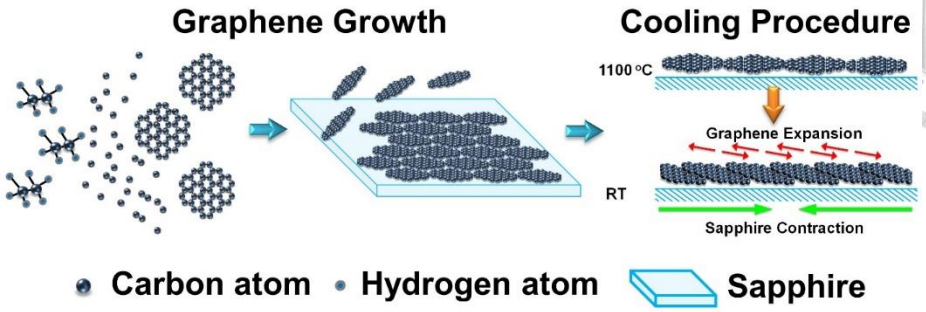
(a)



(b)

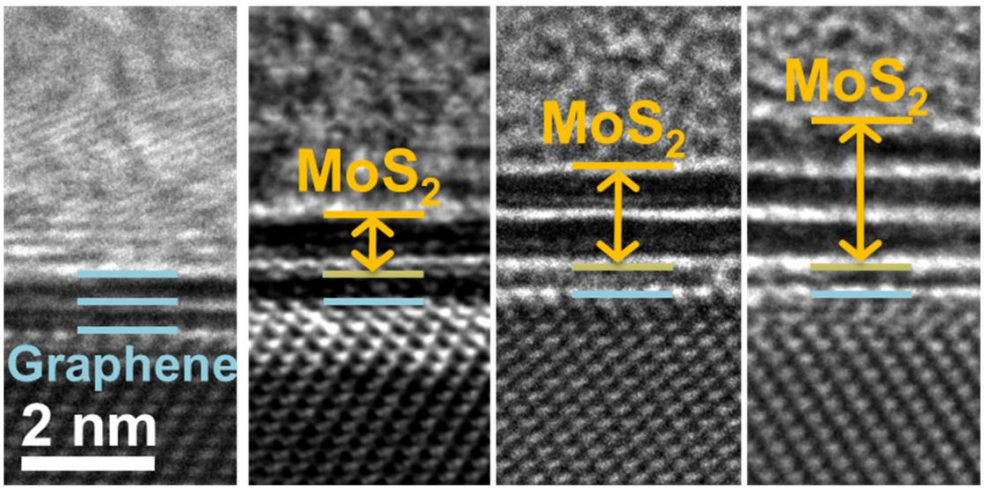


Figure 1-9 (a) A schematic diagram showing the mechanisms of graphene grown directly on sapphire substrates and (b) the cross-sectional high-resolution transmission electron microscope (HRTEM) images of MoS_2/graphene hetero-structures with different MoS_2 layer numbers [30].

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1.3 Outline of the thesis

In this thesis, we have demonstrated that by sulfurizing pre-deposited Mo or MoO_3 films through different approaches, wader-scale and uniform MoS_2 with good layer number controllability can be obtained on different substrate surfaces. Since top-gate transistor is the most common adopted device architecture in semiconductor industry, the stacked structures of 2-D materials with dielectric layers is the first research topic in this thesis. Since in theory, there is no dangling bonds on 2-D material surfaces. It is difficult to achieve uniform precursor distribution on 2-D material surfaces by using the atomic layer deposition technique (ALD) commonly adopted for uniform oxide growth. With an additional precursor soaking, we have demonstrated that a thin Al_2O_3 dielectric layer can be well grown on monolayer MoS_2 by using ALD. We have demonstrated that thin Al_2O_3 layers can be grown on MoS_2 surfaces without influencing their optical characteristics. Low leakage is also observed for the top-gate MoS_2 transistor with the thin Al_2O_3 layer as the gate dielectric. With the 5 nm thin separation layer between mono-layer 2-D materials, luminescence enhancement is observed by stacking the same 2-D materials (MoS_2 with MoS_2). Dual color emission can be observed by stacking different 2-D materials (MoS_2 with WS_2). We have demonstrated that with careful treatment of the

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interfaces of 2-D crystals with other materials, different stacked structures can be established.

Although dielectric layers can be grown directly on 2-D material surfaces, the oxide/2-D material interface may still influence the device performances considering the thin body of 2-D material channels. In this case, it is possible to use a less conductive 2-D material as the passivation layer to the conductive 2-D material channel. It is also important to develop a non-destructive growth procedure of the 2-D material passivation to the under 2-D material channel. In the second topic of this thesis, we have demonstrated that by using the thermal evaporator, bilayer MoS_2 can be grown on graphene surfaces without damage to the underlying graphene channel. The significant field-effect mobility value enhancement suggests that the MoS_2 layer can be a passivation layer on the graphene channel. Similar field-effect mobility values obtained for the device with a monolayer MoS_2 passivation layer suggest that 2-D material channel and passivation layers can be achieved in a few atomic layers. The results have demonstrated that a less conductive 2-D material can act as an efficient passivation layer for conductive 2-D material channels when to-gate device architecture is adopted. Beside 2-D material passivation layers, an alternate approach to avoid the influence of dielectric layers to the 2-D material channels is the adoption of in-plane gates. By using the same MoS_2/graphene hetero-structure and e-beam lithography, we have fabricated and characterized in-plane

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gate transistors. In-plane gate transistors with a 300 nm gate-channel separation were fabricated on the MoS_2/graphene film using the e-beam lithography. We utilized atomic layer etching (ALE) to remove the MoS_2 beneath the source/drain electrodes. In this way, the electrode metal would contact the graphene channel directly. The MoS_2 passivation can effectively isolate the graphene channel from the environment. A field-effect mobility of the device similar to that from Hall measurements indicates that the device performance is well maintained using in-plane gates.

Besides the transistor application, the 2-D material layers may also act as charge storage layers to memory devices. The key issue would be the creation of isolated charge storage layers on the channel layer. For this purpose, epitaxially grown bilayer MoS_2 is grown on monolayer graphene by sulfurizing MoO_3 films deposited by using thermal evaporation. The similar Hall mobility values of the monolayer graphene obtained before and after the MoS_2 growth indicate that there is no additional to the underlying 2-D material layer during the deposition/sulfurization procedure. By using the atomic-layer etching (ALE) technique, the topmost mono-layer MoS_2 layer is isolated from the source/drain electrodes. With the isolated mono-layer MoS_2 on top of the graphene channel, a hysteresis loop is observed for the top-gate graphene transistor. The long retention time for the “0” and “1” states of the device suggests an effective electron storage in the isolated MoS_2 layer. The van der Waals interface between MoS_2 and

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graphene will prevent charge transfer when no external electrical fields are applied to the charge storage layer. The 1T0C memory module fabricated by using thin 2-D material layers can be advantageous for the application of dynamic random access memories (DRAMs) with reduced line widths.

To further simply the fabrication procedure of 2-D material memories, it is possible to further expand the concept of isolated charge storage layers from MoS_2/graphene hetero-structures to multi-layer 2-D materials. For this purpose, tri-layer MoS_2 is fabricated into top-gate transistors with zero, one and two isolated MoS_2 layers on top of the three, two and one layers of MoS_2 channels by using the ALE technique before the source/drain formation. Long retention times and increasing current ratios between "1" and "0" states with increasing isolated MoS_2 layer numbers have revealed the potential of 2-D materials for memory device applications. Due to the van der Waals attachment instead of chemical bonds between MoS_2 layers, a long retention time of electrons stored at the isolated MoS_2 layers are observed for the devices. The results have confirmed that the isolated 2-D material layers can act as the charge storage layers for memory device application.

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Chapter 2 Growth Approaches and Characterizations of 2-D Materials

In this chapter, we will introduce the growth approaches, the film transferring procedure and characterization systems for 2-D materials discussed in this thesis.

2.1 The Preparations of 2-D Materials

The graphene files adopted in this thesis is grown directly on sapphire substrates by using a chemical vapor deposition system (CVD). The CVD system is shown in Figure 2-1. Sapphire substrates have very high melting point up to 2072 °C and is chemically stable at high temperatures, which makes it suitable for 2-D material growth at high temperatures. Its flat surface is also advantageous for possible adatom migration during the van der Waals epitaxy of 2-D materials. For the growth of graphene, the Ar, H_2 and C_2H_6 mixture gas is introduced into the CVD system. By controlling the gas ratio of C_2H_6/H_2 as well as the injecting Ar gas, the temperature is then raised to 1050 °C and stay for 30 mins for graphene growth. By using this method, we can achieve wafer-size and high-quality graphene films for device applications [31].

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Figure 2-1 The graphene CVD system.

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For the preparation of transition metal dichalcogenides (TMDs) samples discussed in this thesis, a two-step procedure of transition metal oxide deposition followed by the sulfurization procedure is adopted. There are three approaches for the deposition of transition metal oxide depositions. The first one is the sulfurization of pre-deposited Mo and W films by using a radio-frequency (RF) sputtering system. The sputtering system is shown in Figure 2-2 (a). The purities of the Mo and W targets are 99.99 % and are supplied by the company Summit-Tech at Taiwan. During the metal deposition procedure, the sputtering power is kept at 30 W, and the background pressure is kept at 5×10^{-3} torr with 30 sccm Ar gas flow. The sputtering times are 15 and 30 sec. for the growth of mono-layer MoS_2 and WS_2, respectively. After the metal deposition, the samples are moved out of the chamber and oxidized naturally in the atmospheric condition. The second approach is the deposition of MoO_3 films by using a thermal evaporator. The thermal evaporation system is shown in Figure 2-2 (b). With the graphene/sapphire sample as the new substrate, 1.0 nm thick molybdenum trioxide (MoO_3) was deposited on the graphene/sapphire substrate using the thermal evaporation. The deposition rate is kept at 0.1 nm/ sec. with the MoO_3 deposition thickness 1 nm for bi-layer MoS_2 and 0.5 nm for mono-layer MoS_2 growth. The third approach for MoO_3 growth is by using an atomic layer deposition system (ALD). The ALD system is shown in Figure 2-2 (c). For the deposition of the MoO_3 films, two precursors molybdenum hexacarbonyl ($Mo(Co)_6$) and ozone (O_3) are

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adopted to deposit the MoO_3 film on sapphire substrates. The growth temperature is kept at 180 ℃. 15 growth cycles are adopted for the deposition of the MoO_3 film ~ 1 nm. Compared with the approach by using the RF sputtering, the major advantage of the MoO_3 deposition by using the thermal evaporator is that a minimum damage to underlying 2-D materials can be achieved without the introduction of plasma during the deposition procedure.

After metal deposition, a similar sulfurization procedure is adopted for TMDs growth. The sulfurization system is shown in Figure 2-2 (d). The samples are placed in the center of a furnace for sulfurization. Before sulfurization, the tube is pumped down to 5×10^{-3} torr to evacuate gas molecules such as oxygen from the environment. During the sulfurization procedure, 160 sccm Ar gas is used as the carrier gas, while the furnace pressure is kept at 0.7 torr. The growth temperature for the samples is kept at 800 °C with the S powder placed upstream of the gas flow. During the sulfurization procedure, the samples are kept at 800 °C for 20 mins. The evaporation temperature for the S powder is kept at 160 °C. Samples with 1.5 g of S powder are prepared. After the sulfurization procedure, the transition metal oxide films will transformed into wafer-scale TMDs films.

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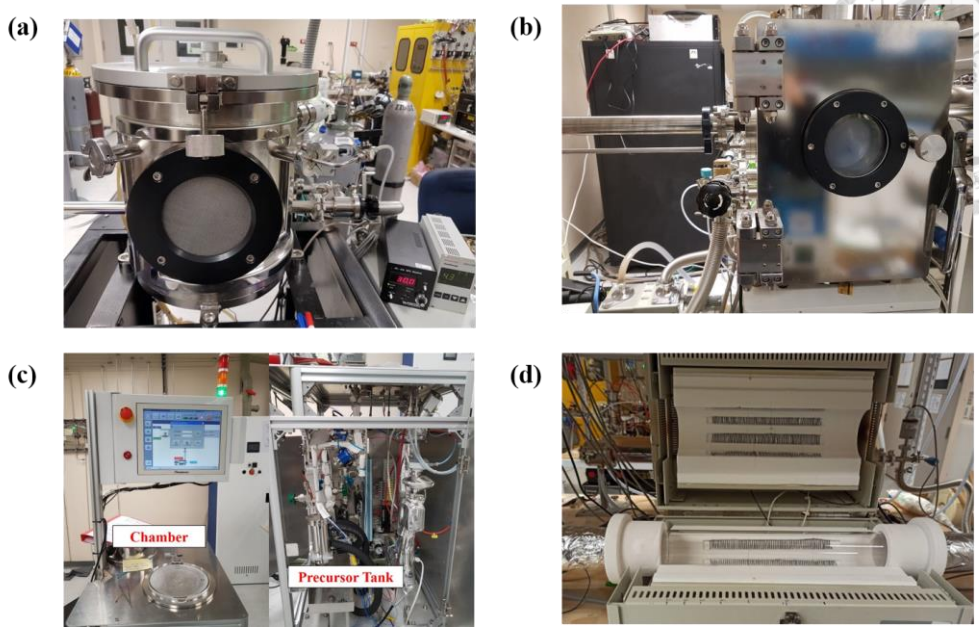

Figure 2-2 (a) The RF sputtering system for Mo and W film depositions, (b) the thermal evaporation system and (c) the ALD system for deposition for the MoO_3. (d) The MoS_2 and WS_2 CVD system.

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2.2 The Transferring Procedures of Grown 2-D Materials

Although epitaxially grown 2-D materials on semiconductor substrates are discussed in this thesis, it is still required to transfer the grown 2-D material films to other substrates for material characterizations and different device applications. For this purpose, we have adopted two different approaches in this thesis for 2-D material film transferring.

2.2.1 PDMS Stamp Transferring

The first transferring procedure is the polydimethylsiloxane (PDMS) stamp transferring. The detailed transferring procedure is shown below. After stamping the as-grown 2-D material/sapphire sample to PDMS substrates, we can de-attach the 2-D material from the sapphire substrates with the assist of DI water. The water has the tendency to penetrate into the interface between the 2-D material film and the sapphire substrate due to different surface energies, which will help the de-attachment of the 2-D material films from sapphire substrates [32]. After that, the PDMS/2-D material film is attached to other substrates such as the SiO_2/Si substrate. In the case of MoS_2, because it is more adhesive to SiO_2 than PDMS, we can just lift the PDMS film and leave the MoS_2 films on SiO_2 surfaces for device fabrication. As we have discussed in one our previous publication, the van der Waals forces of MoS_2 with different materials are different [33].

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In this case, we may de-attach the MoS_2 films from the sapphire substrates as long as the supporting template substrate is more adhesive to MoS_2 than MoS_2 to the sapphire substrate. In this case, there is no need to etch off the underneath substrate for film transferring as the case of MoS_2 grown on SiO_2 surfaces. The successful MoS_2 transferring to SiO_2/Si substrates indicates that MoS_2 is more adhesive to PDMS than the sapphire substrates. On the other hand, MoS_2 is more adhesive to SiO_2 than PDMS.

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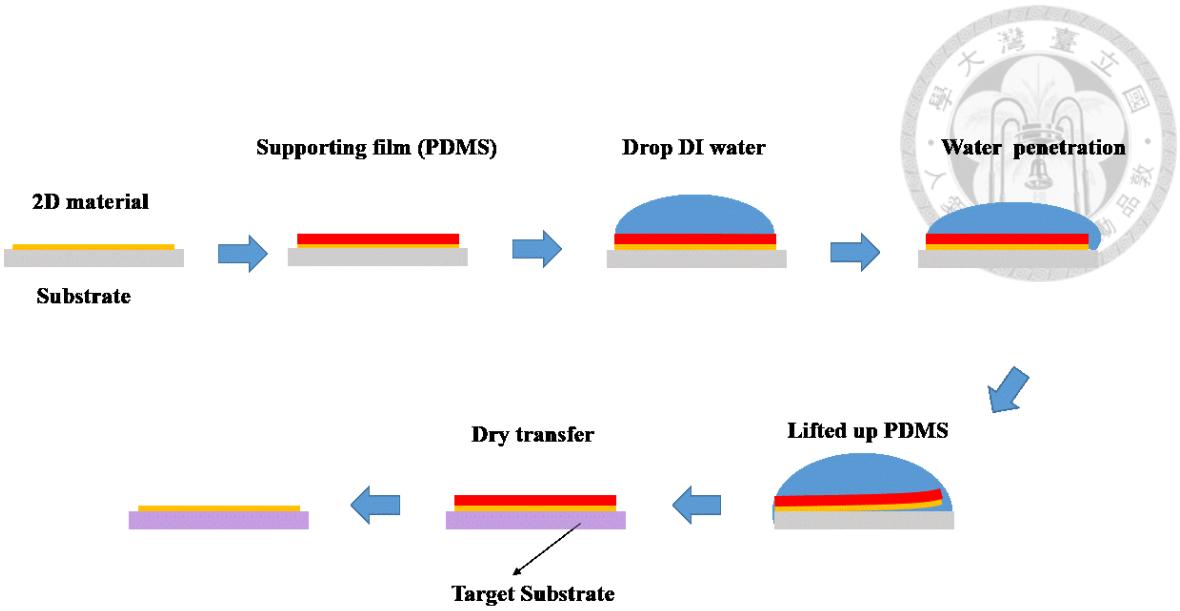

Figure 2-3 Schematic of the dry transfer process of 2-D material using PDMS as a transfer film.

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2.2.2 PMMA Assisted Transferring

Compared with the PDMS stamp transferring, the PMMA assisted transferring technique is a more common transferring technique in the 2-D material research community. The transferring procedure is shown in Figure 2-5. We coat PMMA A4 on the 2-D material films as a supporting template by using a spin coating system. There are two steps of rotation speeds. The spin speed for step one is 500 rpm for 10 s and step two is 800 rpm for 10 s. After the spin coating, we put the sample on a hot plate at 120 °C and bake for 5 mins to curd the PMMA film. Then we lift up the film from one corner of the sample by using a blade and sink the sample into 1 M KOH solution. After this procedure, the PMMA/2-D material film and the sapphire substrate will separate. After that, we transfer the PMMA/2-D material film to a beaker filled with DI water for rinsing. The cleaning procedure would repeat at least three times. After that, we scoop up the PMMA/2-D material film by using a giving substrate (i.e. SiO_2/Si substrates). Then, the sample is put on a hot plate to remove the residue water at 100 °C. Then, we will coat a thicker PMMA to ensure that the 2-D material film adheres better to the substrate. We will leave the sample dry for few hours and then put the sample into Acetone for 1 hour to remove the PMMA layer on 2-D materials. After the transferring procedure, the grown 2-D material films can be transferred to different substrates.

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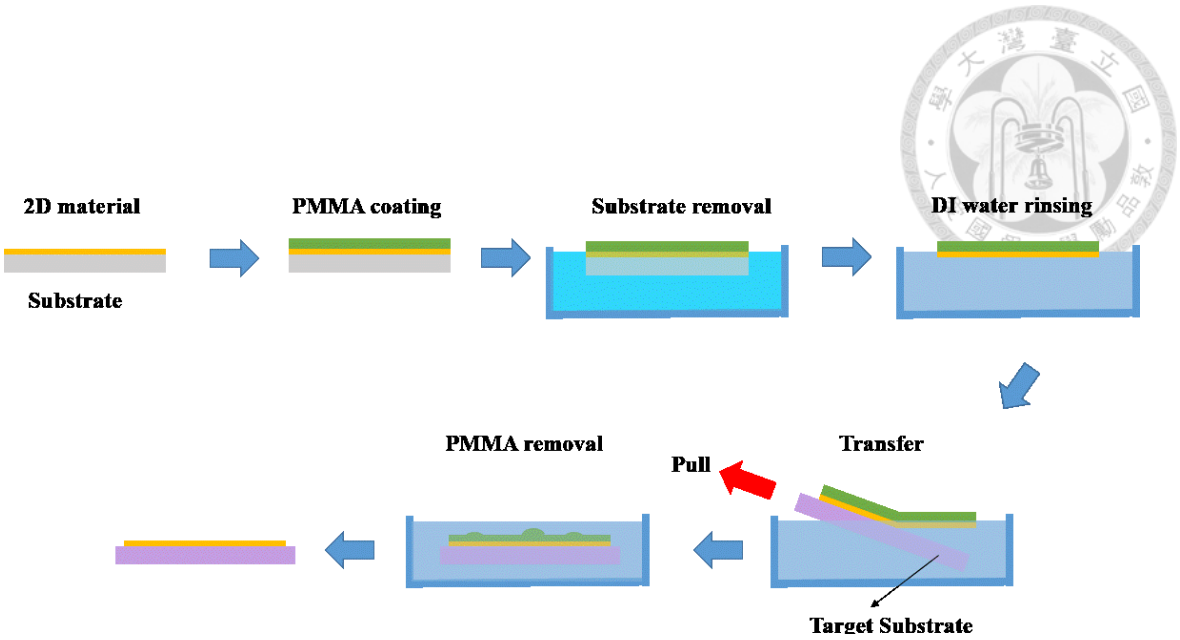

Figure 2-4 Schematic of the wet transfer process of 2-D material using PMMA as a transfer film.

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2.2 The Raman and Photoluminescence Measurement System

Raman and photoluminescence (PL) measurements are two important non-destructive techniques to provide the initial characterizations to the grown 2-D material films. We will introduce these two characterization techniques for 2-D materials in this section.

2.2.1 The Raman spectrum of 2-D materials

The Raman measurement is widely used for 2-D material researches in recent year. The advantages of Raman measurement are non-destructive, simple, and capable of measuring signals in solid, liquid or gas samples. In this thesis, the Raman measurement for the 2-D material samples discussed in this thesis is performed on a HORIBA JobinYvon HR800UV system, which is shown in Figure 2-5. The external laser path setting and optical microscope of the system system are shown in Figure 2-6. The light sources equipped in this system are 488 nm, 532 nm and 632.8 nm lasers. We use 488 nm and 532 nm as our main light sources for Raman measurements of 2-D materials.

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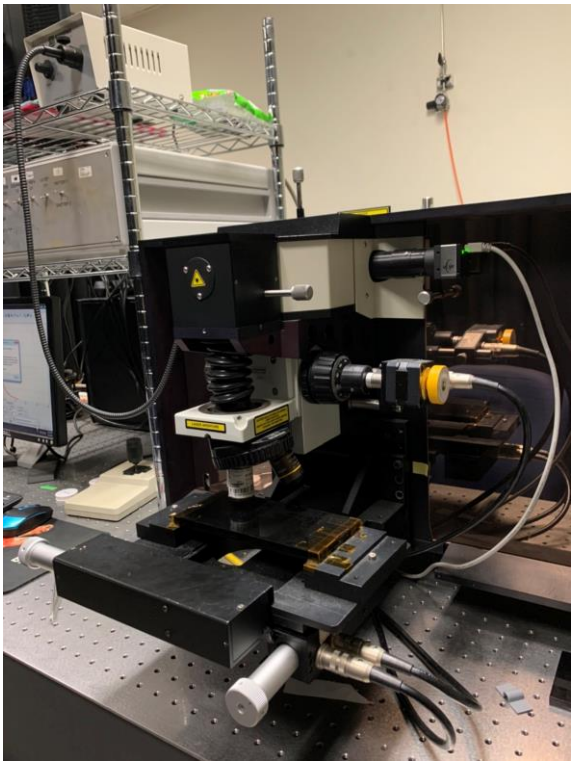

Figure 2-5 The HORIBA Jobin Yvon HR800UV Raman system.

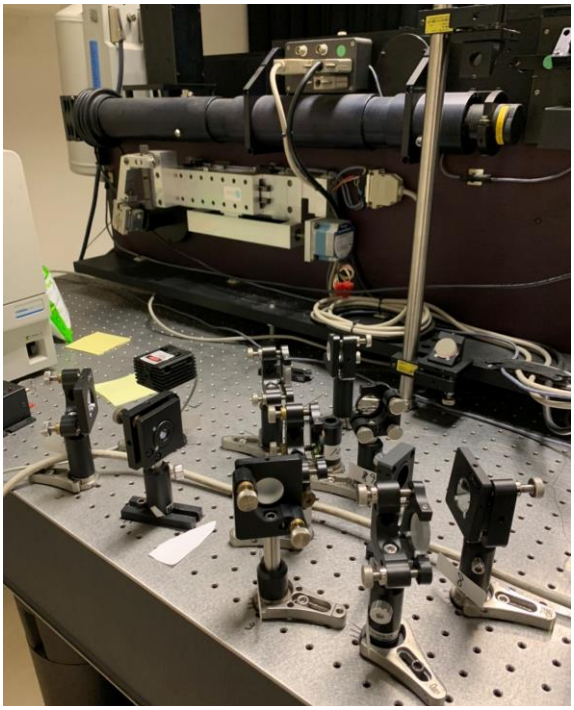

Figure 2-6 The external optical light path setting for HORIBA JobinYvon HR800UV system.

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For graphene, since the carbon-carbon bondings are sp^2 bonds, the irradiated light will resonate with π electron. Several characteristic Raman peaks will be observed on the Raman spectra of graphene. The Raman spectra of a mono-layer graphene is shown in Figure. 2-7. As shown in the figure, three characteristic Raman peaks located at ~ 1350 cm^{-1} (D peak), ~1580 cm^{-1} (G peak) and ~2700 cm^{-1} (2D peak) are usually observed for the grown graphene films [34]. Since the D peak corresponds to the inelastic scattering of photons in the graphene crystal, the intensity of the D peak usually correlated with the defect density of the grown graphene film. On the other hand, the 2D peak intensity is related to the layer numbers of the grown films. For a mono-layer graphene with low a defect density, depending on the laser wavelengths, the peak ratio between 2D and G peaks would usually larger than 2. Therefore, the Raman spectrum of graphene will usually provide a first sight on the crystallinity and layer numbers of the grown graphene films.

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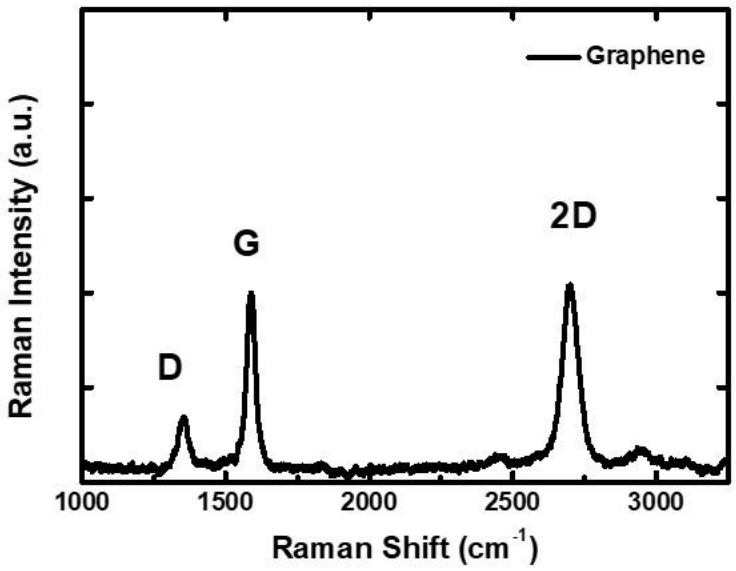

Figure 2-7 The Raman spectra of a mono-layer graphene.

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The Raman spectra of a mono-layer MoS_2 is shown in Figure 2-8 (a). As shown in the figure, two characteristics Raman peaks E^1_{2g} and A_{1g} are observed in the Raman spectra. The E^1_{2g} peak is of the lateral vibration mode, which is located at ~384 cm^{-1}. With increasing MoS_2 layer numbers, the peak will undergo red shift and the peak intensity will also increase in Figure 2-8 (b) [35]. When the MoS_2 layer number reaches a certain value, the peak intensity will start to decrease. The A_{1g} peak is of the vertical vibration mode, which is located at ~402 cm^{-1}. With increasing MoS_2 layer numbers, the peak will undergo blue. The evolution of A_{1g} peak intensities is similar to E^1_{2g}. The full width at the half maximum (FWHM) of the E^1_{2g} peak can also provide a qualitative investigation over the crystallinity of the grown MoS_2 film. Although we can obtain a qualitative investigation over the MoS_2 layer numbers through the Raman peak difference Δk, it is difficult to obtain the exact MoS_2 layer numbers directly through their Raman spectra. Nevertheless, the Raman measurement still provide the first glance on the layer numbers and crystallinity of the grown MoS_2.

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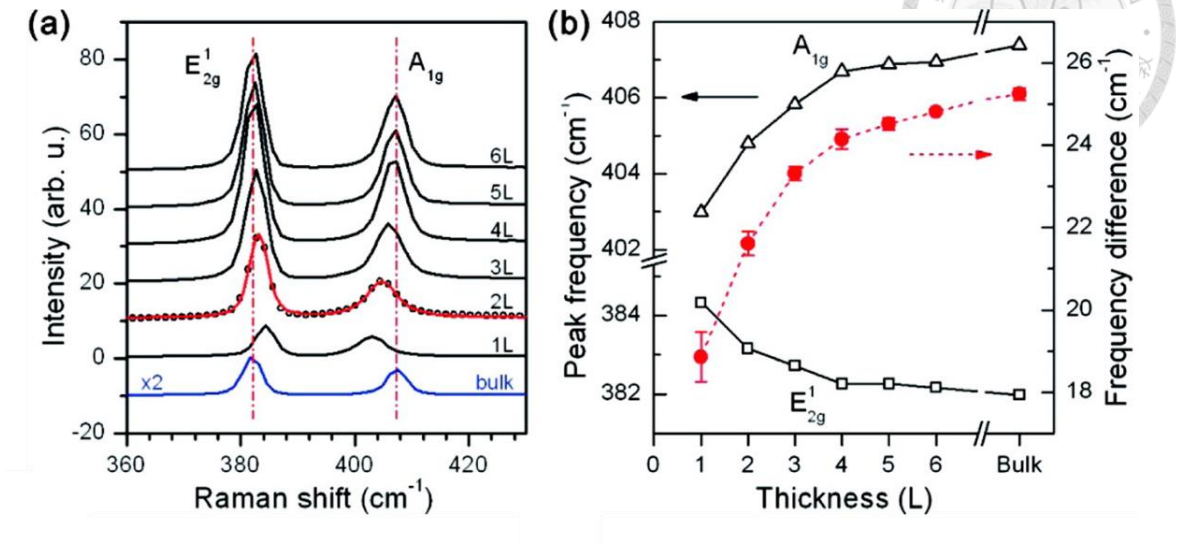

Figure 2-8 (a) Raman spectra of thin and bulk MoS_2 films. (b) Frequencies of E^1_{2g} and A_{1g} Raman difference of layer thickness [35].

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Similar to MoS_2, characteristic Raman peaks can also be observed for WS_2 films for qualitative investigation. The Raman spectra of a mono-layer WS_2 is shown in Figure 2-9 [36]. As shown in the figure, two characteristics Raman peaks E^1_{2g} and A_{1g} are observed in the Raman spectra. Similar to MoS_2, the E^1_{2g} peak is of the lateral vibration mode, which is located at ~356 cm^{-1}. With increasing WS_2 layer numbers, the peak will undergo red shift and the peak intensity will also increase in Figure. The A_{1g} peak is of the vertical vibration mode, which is located at ~417 cm^{-1}. Although in principle, The Raman measurement of WS_2 may also provide a qualitative insight of the grown WS_2 films. However, due to the much larger Raman peak difference value and its small variation with increasing layer numbers, it is difficult to acquire the information of layer numbers of the grown WS_2 films directly from the Raman spectrum. The direct observation by using the cross-sectional high-resolution transmission electron microscope (HRTEM) will be a better approach to tell the actual layer numbers of the grown WS_2 samples.

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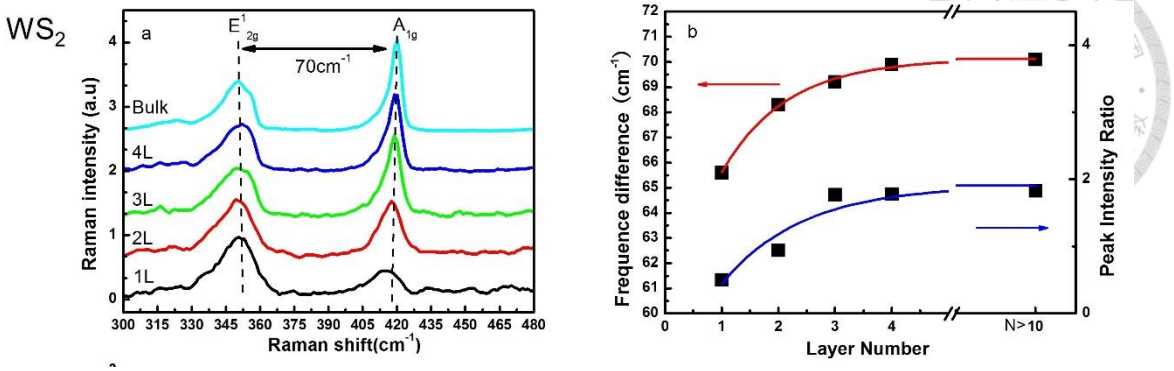

Figure 2-9 Raman spectra of thin and bulk WS_2 films and frequencies of E^1_{2g} and A_{1g} Raman difference of layer thickness [36].

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2.2.2 The Photoluminescence spectrum of 2-D materials

The PL measurement is a very useful and non-destructive technique for semiconductor inspection. We can know the band gap of material, impurity type, and activation energy from the PL spectrum. The PL spectra of a mono-layer MoS_2 is shown in Figure. 2-10 [37]. Since mono-layer MoS_2 is of direct bandgap material, strong luminescence is observed for the sample. The two PL peaks 627 and 667 nm observed in the figure is attributed to the spin-orbit coupling induced valence band splitting at the K point of the MoS_2 band structure. With increasing layer numbers, MoS_2 will gradually transform from direct-bandgap to indirect-bandgap material. In this case, the PL peak intensity of multi-layer MoS_2 will gradually decrease. No significant luminescence peak will be observed for bulk MoS_2.

The PL spectra of a mono-layer WS_2 is shown in Figure. 2-11 [38]. The PL spectra display an indirect to direct bandgap from multilayer WS_2 to monolayer WS_2. With the decreasing of thickness, the intensity of PL peaks gradually increases. The PL intensity is extremely weak for multi-layer WS_2, consistent with an indirect bandgap semiconductor. The peak blue shift to shorter wavelength with decreasing WS_2 layer numbers indicates an increase in the bandgap value of the 2-D material films. The PL peak energy would reach its maximum for monolayer WS_2, which is about 2.0 eV.

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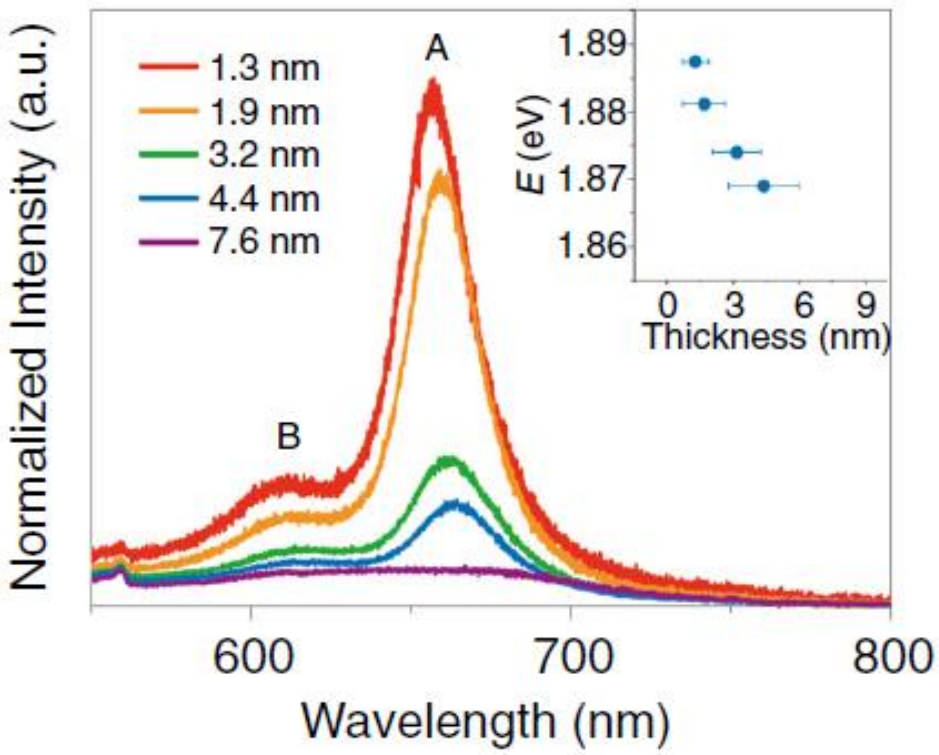

Figure 2-10 Photoluminescence spectra of MoS2 with different thickness [37].

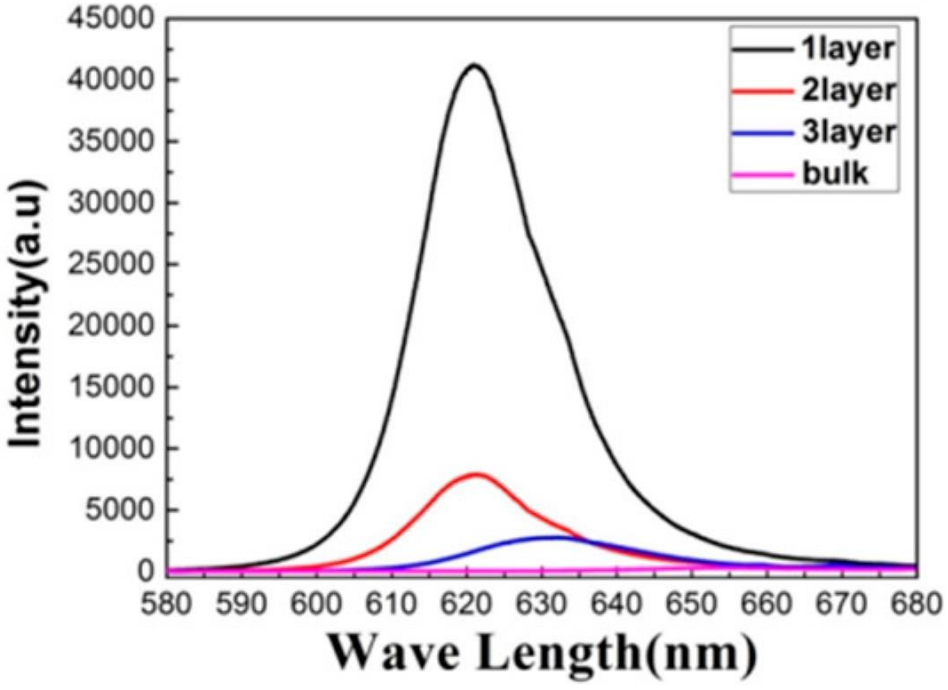

Figure 2-11 Photoluminescence spectra of WS2 with different thickness [38].

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2.3 Device Fabrications Systems

The systems adopted for device fabrication in this thesis will be introduced in this section.

2.3.1 The atomic layer deposition system (ALD)

A lot of techniques such as sputtering, pulsed laser deposition (PLD), chemical vapor deposition (CVD), and atomic layer deposition (ALD) have been applied to the deposition of dielectric layers [39]. Due to the thin body nature of 2-D materials, we need for thin film deposition techniques with excellent conformality and atomic thickness control becomes important. Compared to other deposition techniques, ALD has near-perfect conformality on structures with high aspect ratios with precise thickness control [40]. Therefore, the favorable technique for the oxide deposition of nanoscale devices is ALD.

One of the advantages of ALD technology over other thin film deposition methods is its "self-limiting" nature. Self-limiting means that once a monolayer molecule reacts and bonds to the material surface, it is unlikely that any other reactant molecule will bond to the molecule that makes up the monolayer of the surface, and eventually only one layer of the reactant [41]. Owing to its self-limiting growth characteristics, ALD has many advantages including precise composition and thickness control, large area uniformity,

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excellent conformality, and good reproducibility. Figure 2-12 shows the ALD cycle, a four-step for ALD cycle include:

- Step 1: The precursor (i.e. precursor A) enters the chamber through a carrier gas to chemically react with the substrate and then produce by-products.
- Step 2: The excess precursor and by-products are purged from the chamber by the vacuum pump and N_2 carrier gas.
- Step 3: After both the precursor and the by-products are purged from the chamber, the reactant (i.e. precursor B) is sprayed into the chamber to react with the precursor and then produce by-products.
- Step 4: After the reaction is completed, the excess reactants and by-products are purged from the chamber by a vacuum pump to complete an ALD cycle.

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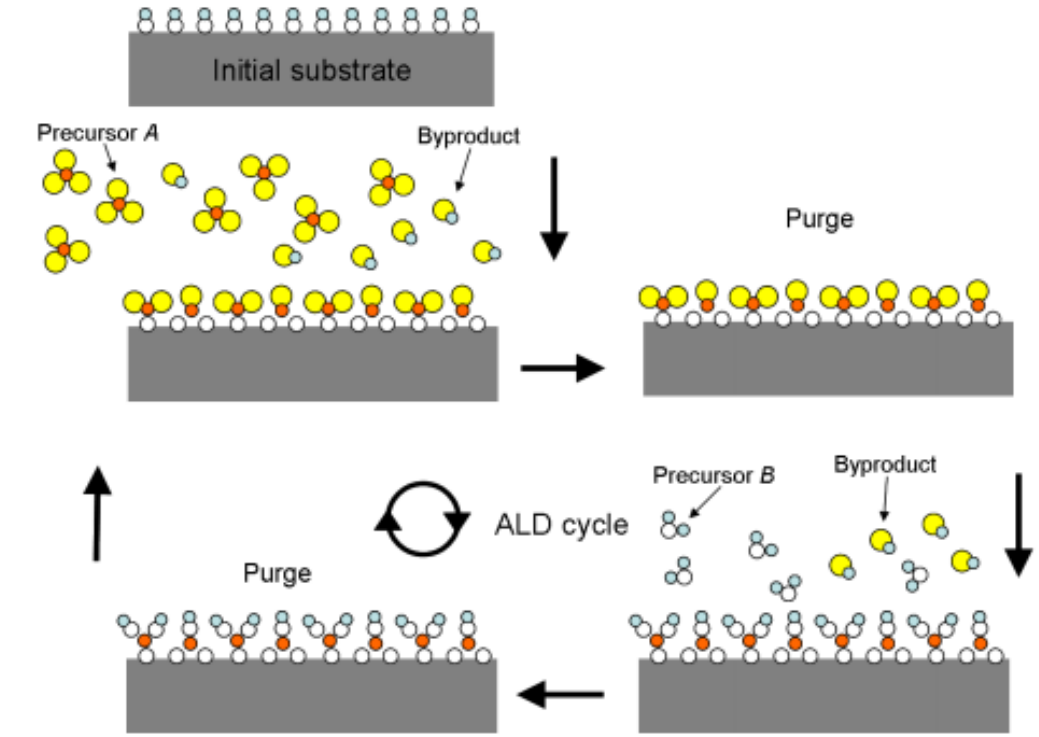

Figure 2-12 Schematic diagram of ALD cycle [42].

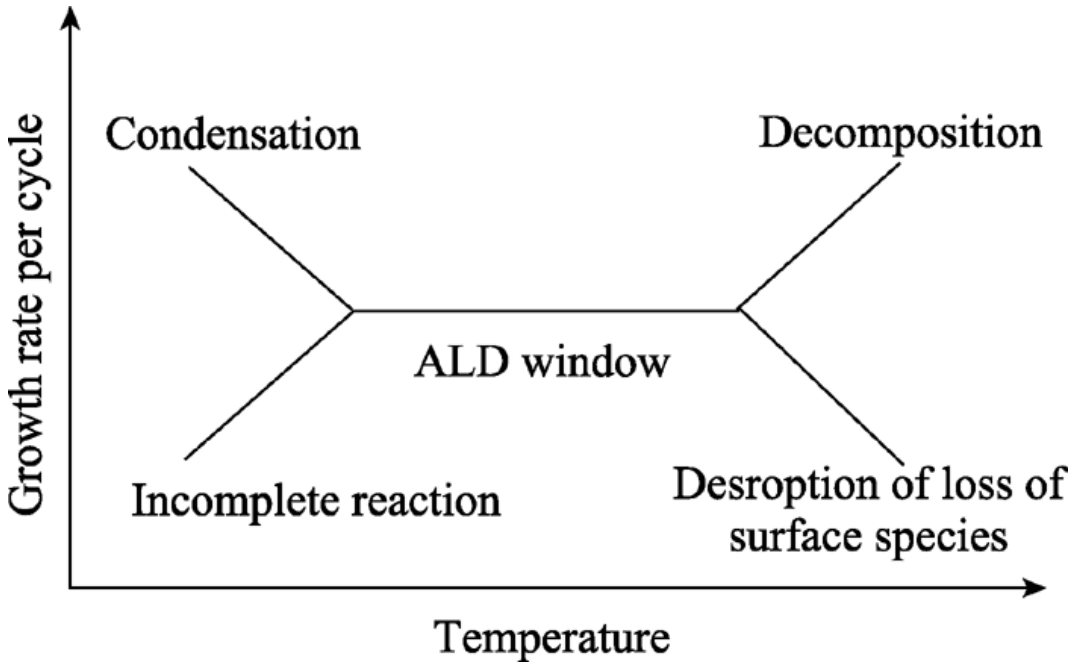

Figure 2-13 Schematic diagram of ALD process window [43].

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The activation energy is required to remove the ligand of the adsorbed molecule by interaction with the reactant molecules during ALD process. The activation energy is provided from the applied heat substrate. Therefore, the deposition temperature in the ALD process is a key parameter for self-limiting growth. The growth rate is usually kept constant while the ALD process is carried out over a range of temperatures to provide sufficient energy for the reaction. This temperature range is so-called the "ALD process window" as shown in Figure 2-13.

At the lower temperatures, the growth rate generally decreases with decreasing temperature due to insufficient thermal energy of the reaction. However, due to the condensation of the precursors, the opposite trend may sometimes be observed. At the higher temperatures, the first chemical reactant can decompose on the surface before it reacts with the second reactant. In this case, the growth rate will be higher than expected from the ALD process. However, if the first precursor is stable, it can still desorb from the surface before it has a chance to react with the second reactant.

In the ALD process for Al_2O_3, (1) The TMA pulse is injected into the chamber and reacts to the substrate surface. (2) After the adsorption of precursor on the surface, the excess precursor is removed by purging the chamber. (3) The H_2O is pulse injected into the chamber and reacts with TMA to form the Al_2O_3. (4) Excess H_2O is cleaned by

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purging the chamber. After the above 4-step cycle is done, a new cycle begins until the desired thickness is reached. The overall reaction equation is as follows.

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 3CH_4$$

In the ALD process for MoO_3, (1) The $Mo(CO)_6$ pulse is injected into the chamreactsnd react to the substrate surface. (2) After the adsorption of precursor on the surface, the excess precursor is removed by purging the chamber. (3) The O_3 pulse is injected into the chamber and reacts with $Mo(CO)_6$ to form the MoO_3. (4) Excess O_3 is cleaned by purging the chamber. After the above 4-step cycle is done, a new cycle begins until the desired thickness is reached. The overall reaction equation is as follows [44].

$Mo(CO)_6$ pulse $\quad Mo(CO)_6(g) + |\text{-}O \rightarrow |\text{-}O\text{-}Mo(CO)_{0.5} + 5.5\ CO(g)$

O_3 pulse $\quad |\text{-}O\text{-}Mo(CO)_{0.5} + O_3(g) \rightarrow |\text{-}O\text{-}Mo\text{-}O_3 + 0.5\ CO(g)$

The ALD system used in this thesis is a customized thermal ALD system manufactured by SYSKEY technology. The system is composed of a chamber, vacuum pump system and precursor module. The chamber substrate is a heater that can heat up to 300 ºC. A mechanical pump pumps down the chamber to 1×10^{-2} torr. The precursor module consists of two precursor tanks and two high-speed pulse valves controlling the injection of precursors. The temperature of the precursor tank for TMA is controlled by a circulation refrigerator system. N_2 is the carrier gas used during the ALD process.

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2.3.2 The electron-beam lithography system (EBL)

In order to examine our fabricated devices, we utilize scanning electron microscope (SEM) to confirm the sizes of the devices. Compared with the conventional optical microscopes, SEM can observe a structure down to nanometer and offer higher resolution images because the wavelength of electron beam is much shorter than visible light. Moreover, we can use SEM to check the size of the device structure, which is not possible with optical microscopes. Besides inspection over the fabricated devices, we also use the SEM system equipped with a pattern generator for device fabrication in the nanometer regime. As shown in Figure 2-14, the SEM system is Inspect F from FEI Company, which is equipped with a pattern generator system and can be used for electron beam lithography in the nanometer regime. With a high voltage range from 1 keV to 30 keV, the scattering electron will be detected and the intensity of the secondary electrons varies depending on the angle of the incident electrons onto the sample. According to the signal intensity, the roughness of the surface will be expressed. For the fabrication process, SEM play an important role in examining the devices in each processing steps. More importantly, the fabrication of nanoscale devices relies on the precision of SEM system. In this thesis, we use this system for the fabrication of in-plane gate transistors.

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Figure 2-14 FEI inspect F scanning electron microscope (SEM) system with a pattern generator system for electron beam lithography.

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2.3.3 The atom layer etching (ALE) of 2-D materials

In our previous publications, we have demonstrated that by using a low-power oxygen plasma to oxidize multi-layer TMDs, the topmost fully oxidized TMDs layer will detach from the underlying TMDs layers due to the weakened adhesion in between [33]. In this case, atomic layer etching of TMDs can be achieved by using this technique. It is also possible to tell the actual layer numbers of the grown TMDs by repeating the same ALE procedures. The oxygen plasma etching system used in this thesis is shown in Figure 2-15 The ALE system. The system is a dry etching system that uses Transformer Coupled Plasma (TCP). It generates plasma by using the electromagnetic field that generated by electromagnetic induction. For a single ALE procedure, the oxygen plasma power was kept at 20 W in the etching chamber. The background pressure was maintained at 0.4 Torr with a 30 sccm oxygen gas flow during the removal process. The treatment time is 10 sec. After the oxidization, the sample was dipped in deionized water for 10 s to detach the topmost oxidized MoS_2 layer. Through repeating the same procedure, layer-by-layer TMDs etchings can be achieved by using this system [33]. Besides ALEs, the oxygen plasma system is also used for the channel definition of the 2-D material transistors.

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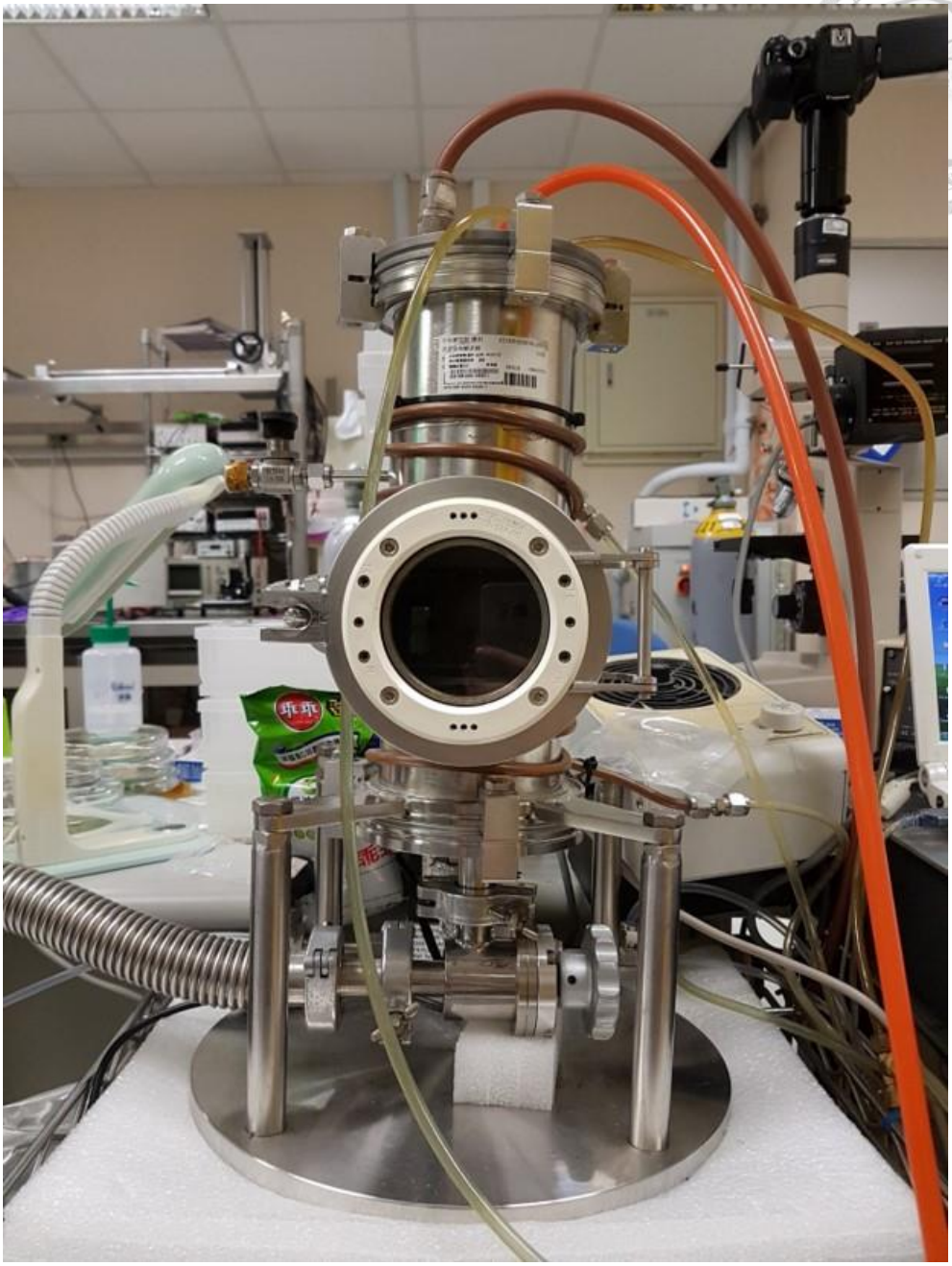

Figure 2-15 The ALE system

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Chapter 3 Stacked Structures of 2-D Materials for Transistor Applications

3.1 Luminescence Enhancement and Dual-Color Emission of Stacked Mono-layer 2-D Materials

Different TMDs have been investigated for over ten years. They are MoS_2, WS_2 and WSe_2. Among of them, MoS_2 is the most studied material due to its easy formation by using different growth techniques and the possibility of material stacking either of homo- or hetero-structures [27,45]. However, since only a few atomic layers of 2-D materials are usually adopted for investigation, the influence of the environment and the interface issues play an important role in the application of these materials. For electronic device application such as top-gate MoS_2 transistors, the oxide/ MoS_2 interface will significantly influence the device performances, which will result in low drain currents and low mobility values for the device. It is also difficult to form Ohmic contact between the metal/MoS_2 interface such that high contact resistance is another issue for 2-D devices. The results have demonstrated that the interfaces with other materials will significantly influence the characteristics of 2-D materials. The mono-layer TMDs are of direct bandgap, their applications not only optical devices but also widely investigated in electronic devices. However, since multi-layer TMDs or their hetero-structures stacking

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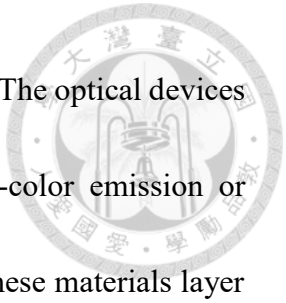

are usually of indirect bandgap materials, most of the optical devices. The optical devices only exist single-color emission/detection in literature. The Multi-color emission or enhanced luminescence intensities can not be achieved by stacking these materials layer by layer. In this chapter, we have demonstrated that by using ALD deposit a 10 nm Al_2O_3 dielectric layer with an additional precursor soaking time, two mono-layer MoS_2 layers can be well separated by the thin dielectric layer. Similar optical characteristics of the monolayer MoS_2 film before and after the ALD growth indicates that minor damages are introduced to the thin 2-D material film during the growth procedure. With the thin separation layer between mono-layer 2-D materials, luminescence enhancement is observed by transferring a mono-layer MoS_2 film to a 5 nm Al_2O_3/mono-layer MoS_2 sample. Dual color emission can be observed by transferring mono-layer WS_2 to the other $Al2O_3/MoS_2$ sample. With careful treatment on the interfaces of 2-D crystals with other materials, different stacked structures can be established, which will be advantageous for further device applications of 2-D materials.

3.1.1 The deposition of thin dielectric layers on MoS_2 surfaces

To investigate the growth of dielectric layers on 2-D material surfaces, one sample with sequentially grown mono-layer MoS_2/5 nm Al_2O_3/mono-layer MoS_2/10 nm Al_2O_3 on a sapphire substrate is prepared. The cross-sectional HRTEM image of the sample is

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shown in Figure 3-1. While the first MoS_2 layer is well grown on the first 10 nm Al_2O_3 layer, incomplete second MoS_2 layer is observed in the figure. The magnified HRTEM image is shown as an inset in Figure 3-1. It is clearly seen from the figure that although part of the second MoS_2 layer is still separated from the first MoS_2 layer, the rest of the second MoS_2 layer is actually grown directly on the first MoS_2 layer. The partial desorption of the 5 nm Al_2O_3 layer during the 800 ^oC sulfurization procedure of the second MoS_2 layer may be the main reason responsible for this phenomenon. The weak adhesion between the Al_2O_3 and MoS_2 interface is attributed to the lack of dangling bonds on MoS_2 surfaces such that non-uniform precursor distributions and the lack of nucleation sites would lead to an inferior Al_2O_3 layer growth by using ALD.

To solve this problem, the other sample with thicker Al_2O_3 separation layer (10 nm) and an additional 30 s stay time after the TMA pulse during ALD growth is prepared. The cross-sectional HRTEM image of the sample is shown in Figure 3-2 (a). As shown in the figure, the two MoS_2 layers are well separated from each other. The corresponding high-angle annular dark-field scanning (HAADF) image showing the distinct sulfur distributions (Figure 3-2 (b)) also confirms this point.

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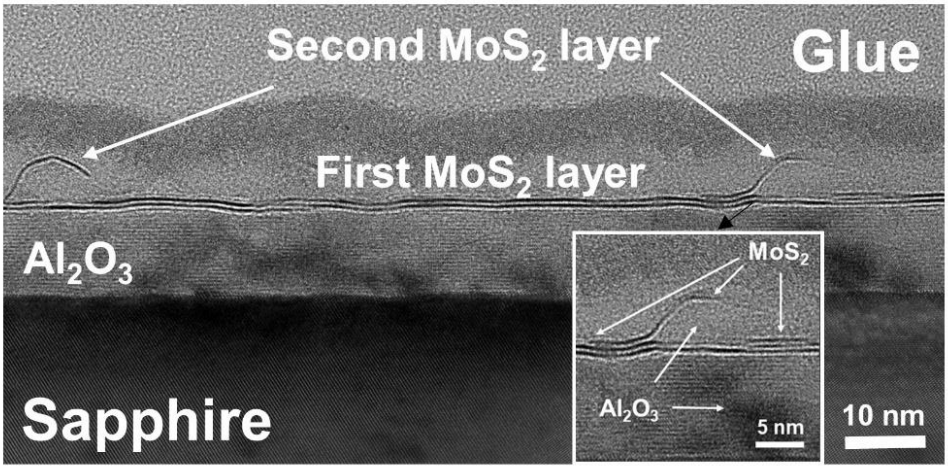

Figure 3-1 The cross-sectional HRTEM image of the sample with sequentially grown mono-layer MoS_2/5 nm Al_2O_3/mono-layer MoS_2/10 nm Al_2O_3 on a sapphire substrate.

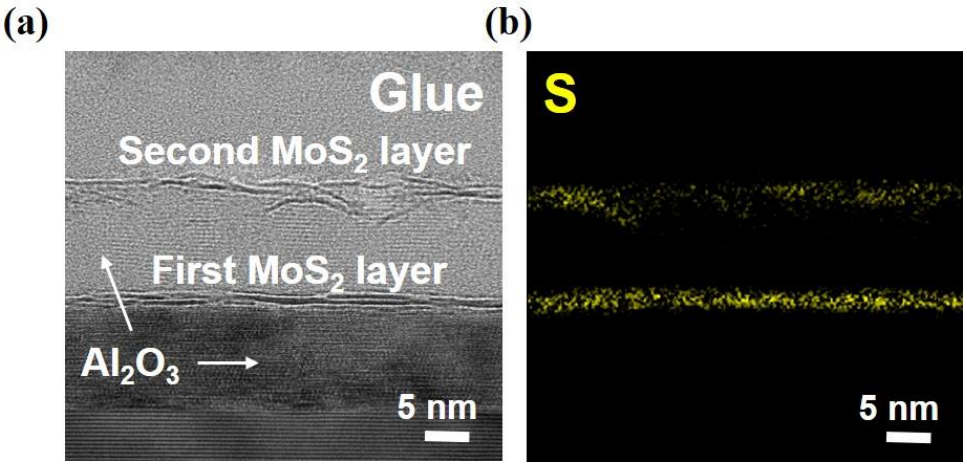

Figure 3-2 The cross-sectional HRTEM image and (b) The corresponding HAADF image showing the sulfur (S) distributions of the sample with sequentially grown mono-layer MoS_2/10 nm Al_2O_3/mono-layer MoS_2/10 nm Al_2O_3 on a sapphire substrate.

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3.1.2 Luminescence enhancement of stacked mono-layer MoS_2

Since TMDs usually exhibits an evolution of direct bandgap to indirect bandgap with increasing layer numbers, it is impossible to enhance their luminescence intensities simply by increasing their film thicknesses. Therefore, one possible application of such a thin dielectric layer is to separate two mono-layer 2-D material layers for luminescence enhancement. To achieve this goal, a 5 nm Al_2O_3 separation layer is gown on mono-layer MoS_2 surfaces following similar ALD growth procedures discussed above. The Raman spectra of the mono-layer MoS_2 sample before and after the 5 nm Al_2O_3 separation layer growth are shown in Figure 3-3 (a). As shown in the figure, similar Raman spectrum with characteristic Raman peaks E^1_{2g} and A_{1g} of MoS_2 are observed before and after the oxide growth. The results demonstrate that the oxide growth did not bring major damage to the thin 2-D material film. The same phenomenon also results in similar photoluminescence (PL) intensities before and after the oxide growth (Fig. 3-3 (b)). On the other hand, Δk difference from 19.3 to 18.3 cm^{-1} and PL peak position shift from 665 to 671 nm are still observed after the Al_2O_3 growth. One possible mechanism responsible for the decreasing Δk value may be the n-doping of the Al_2O_3 layer to the mono-layer MoS_2 such that the red shift of the A_{1g} peak would results in a decreasing Δk value [46]. The same phenomenon also results in the broadening of the A_{1g} Raman peak after the Al_2O_3 growth as shown in Figure 3-3 (b). As for the PL peak shift, it is possible that the growth of the

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thin Al_2O_3 separation layer would induce tensile strain to the MoS_2 film, which would result in the PL peak red shift [47]. Further investigations are still required in the future to clarify these points. The PL spectra of the sample with and without the other mono-layer MoS_2 transferred to the Al_2O_3 surface is shown in Figure 3-3 (c). Two times PL intensity enhancement is observed for the sample, which demonstrates that the thin oxide layer can effectively separate the same mono-layer 2-D materials for intense luminescence.

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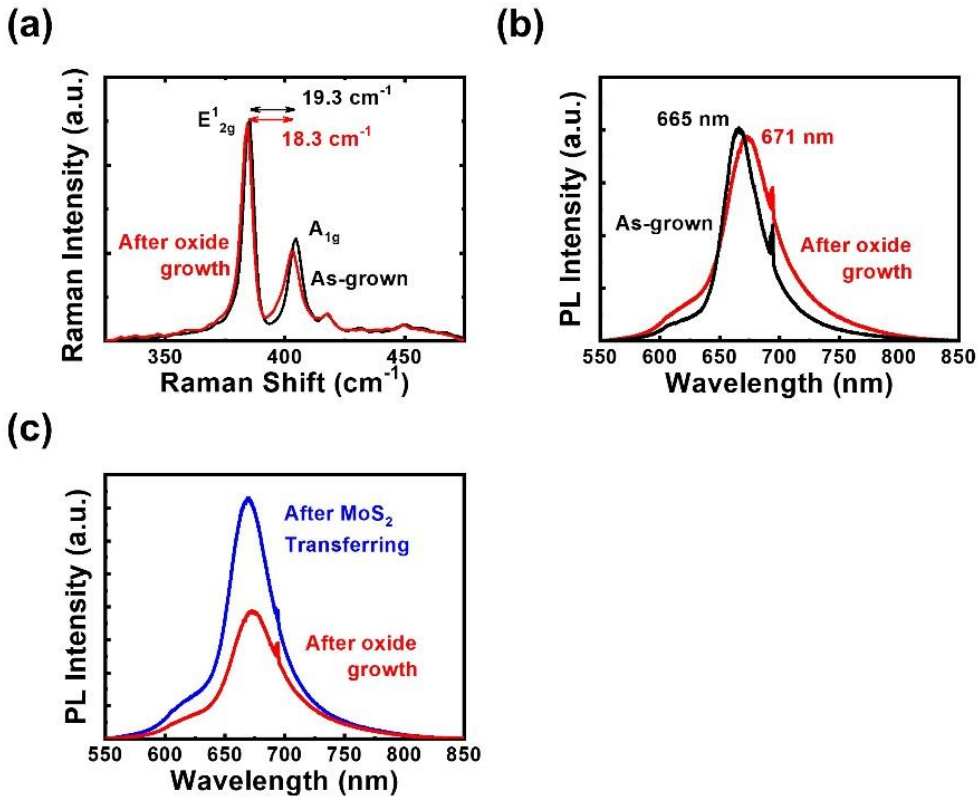

Figure 3-3 (a) The Raman and (b) the PL spectra of the mono-layer MoS_2 sample before and after the 5 nm Al_2O_3 separation layer growth. (c) The PL spectra of the sample with and without the other mono-layer MoS_2 transferred to the Al_2O_3 surface.

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3.1.3 Dual-color emission of stacked mono-layer MoS_2 and WS_2

Following the similar procedure, different 2-D materials may also be stacked for multi-color emission. To prevent the absorption to the MoS_2 luminescence, the bandgap value of the upper 2-D material should be larger than MoS_2. Since he bandgap value of mono-layer WS_2 (1.98eV) is larger than MoS_2 (1.89 eV), therefore, multi-color emission may be achieved by stacking WS_2 with MoS_2 with the thin separation layer. For this purpose, WS_2 films are transferred to a 5 nm Al_2O_3/mono-layer MoS_2 sample. The Raman spectrum of the sample is shown in Figure 3-4 (a). Characteristic Raman peaks corresponding to MoS_2 and WS_2, respectively, are observed in the figure. The PL spectrum of the sample is shown in Figure 3-4 (b). The PL spectra of the sample before film transferring and standalone WS_2 are also shown in the figure for comparison. Since WS_2/MoS_2 is of type-II band alignment, direct attachment of WS_2 with MoS_2 will weaken the PL intensities of the two materials [27]. With a 5 nm Al_2O_3 inserted in between, dual-color emission from both mono-layer MoS_2 and WS_2 can be observed. No luminescence decreasing is observed for the sample.

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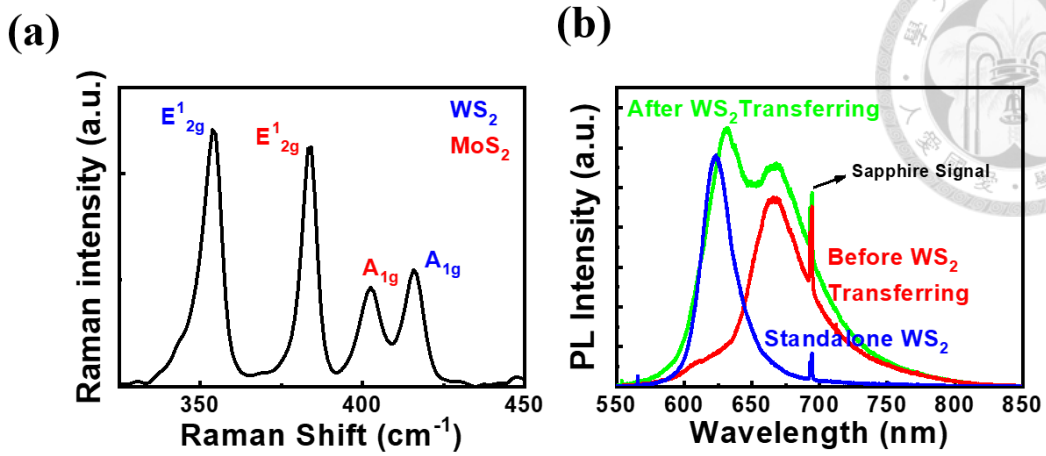

Figure 3-4 (a) The Raman and (b) the PL spectrum of the sample with mono-layer WS_2 transferred to a 5 nm Al_2O_3/mono-layer MoS_2 substrate. The PL spectra of the sample before the WS_2 transferring and the standalone WS_2 are also shown in (b)

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3.1.4 Conclusion

In conclusion, we have demonstrated that thin Al_2O_3 layers can be grown on MoS_2 surfaces without influence its optical characteristics. Low leakage is also observed for the top-gate MoS_2 transistor with the thin Al_2O_3 layer as the gate dielectric. With the thin separation layer between mono-layer 2-D materials, luminescence enhancement is observed by stacking the same 2-D materials (MoS_2 with MoS_2). Dual color emission can be observed by stacking different 2-D materials (MoS_2 with WS_2). We have demonstrated that with careful treatment on the interfaces of 2-D crystals with other materials, difference stacked structures can be established. The stacking of 2-D materials with other materials will bring wide applications of 2-D materials in practical devices.

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3.2 Top-gate Graphene Transistors with MoS_2 Passivation Layers

The most possible application of 2-D materials is in electronic devices. With the thin channels down to a few atomic layers, the influence of the dielectric layers is un-avoidable when top-gate device architecture is adopted. In this chapter, we have demonstrated that by using the thermal evaporator, bi-layer MoS_2 can be grown on graphene surfaces without introducing additional damages to the graphene channel. The significant field-effect mobility value enhancement suggest that the MoS_2 layer can act as an efficient passivation layer to the graphene channel. Similar field-effect mobility values obtained for the device with a mono-layer MoS_2 passivation layer suggest that 2-D material channel and passivation layers can be achieved in a few atomic layers, which will be advantageous for electronic devices with reduced line widths.

3.2.1 MoS_2 growth on graphene surfaces using the RF sputtering

In one previous publication, we have demonstrated that scalable graphene films can be grown directly on sapphire substrates without the assistance of metal templates [48]. Layer-number-controllable MoS_2 films can also be grown on the graphene surfaces by sulfurizing the pre-deposited Mo films prepared by the RF sputtering [30]. However,

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damages to the underlying graphene films may be introduced due to the Ar plasma adopted by the RF sputtering system. To demonstrate this point, a sample with a graphene film grown directly on a sapphire substrate is prepared. By using the graphene/sapphire sample as the new substrate, a bi-layer MoS_2 film is grown on the graphene surface through the sulfurization of the pre-deposited Mo film prepared by the RF sputtering.

The Raman spectra of the graphene films before and after the MoS_2 growth are shown in figure 3-5. As shown in the figure, the D/G peak ratios increase from 0.3 to 1.0 after the sputtering growth MoS_2. The increasing D/G peak ratio suggests that additional defects are introduced to the graphene channel after the MoS_2 growth procedure [49]. The Hall mobility values of the graphene films would therefore, reduce from 274 to 30 $cm^2/V{\cdot}s$. In this case, although the grown MoS_2 film may separate the graphene channel to the top dielectric layer, the defects introduced during the MoS_2 growth procedure would degrade the device performances.

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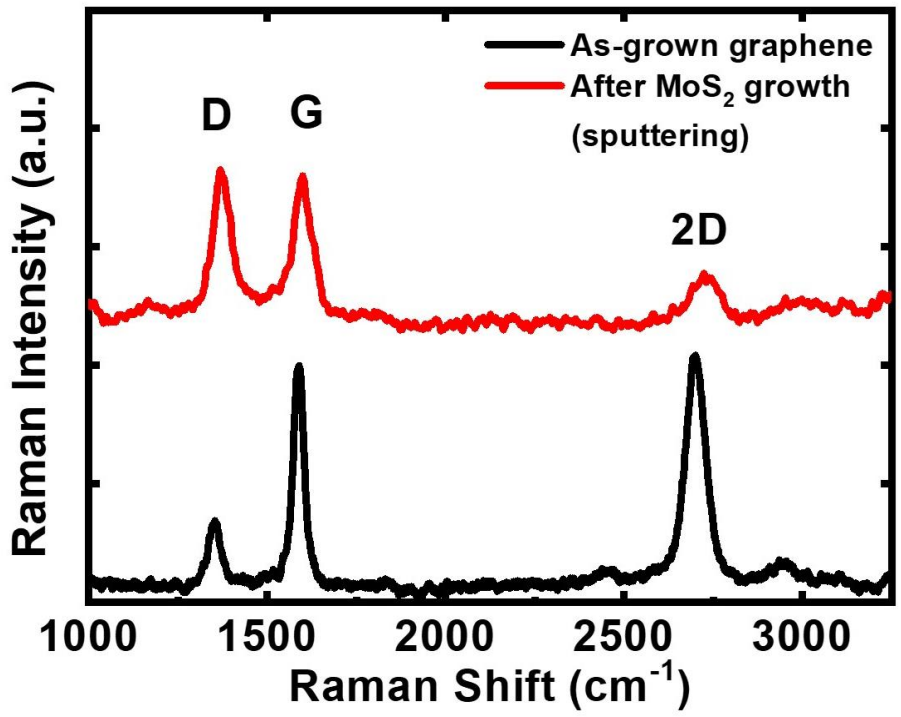

Figure 3-5 The Raman spectra of the graphene films before and after the MoS_2 growth by using the RF sputtering.

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3.2.2 Non-destructive MoS_2 growth on graphene surfaces and the passivated top-gate graphene transistor

To prevent the damage to the graphene films, the thermal evaporation is adopted for the MoO_3 deposition. The cross-sectional HRTEM image of sample after the MoS_2 growth prepared by using the thermal evaporator is shown in Figure 3-6 (a). Bi-layer MoS_2 is observed on mono-layer graphene for this sample, which demonstrates that besides the RF sputtering of Mo films, large-area MoS_2 film can also be prepared through the sulfurization of the MoO_3 films deposited by using the thermal evaporator. The Raman spectrum of the sample showing the characteristic Raman peaks of graphene is shown in Figure 3-6 (b). As shown in the figure, similar D/G peak ratio ~0.3 with the as-grown graphene film is observed for this sample. Similar Hall mobility value 280 $cm^2/V{\cdot}s$ with the as-grown graphene sample is also observed for the bi-layer MoS_2/graphene sample. With the similar D/G peak ratios and Hall mobility values before and after the MoS_2 growth, the results reveal that compared with RF sputtering, limited defects are introduced during the MoS_2 growth procedure. The MoS_2 films prepared by using the thermal evaporator may act as a passivation layer to the graphene channel.

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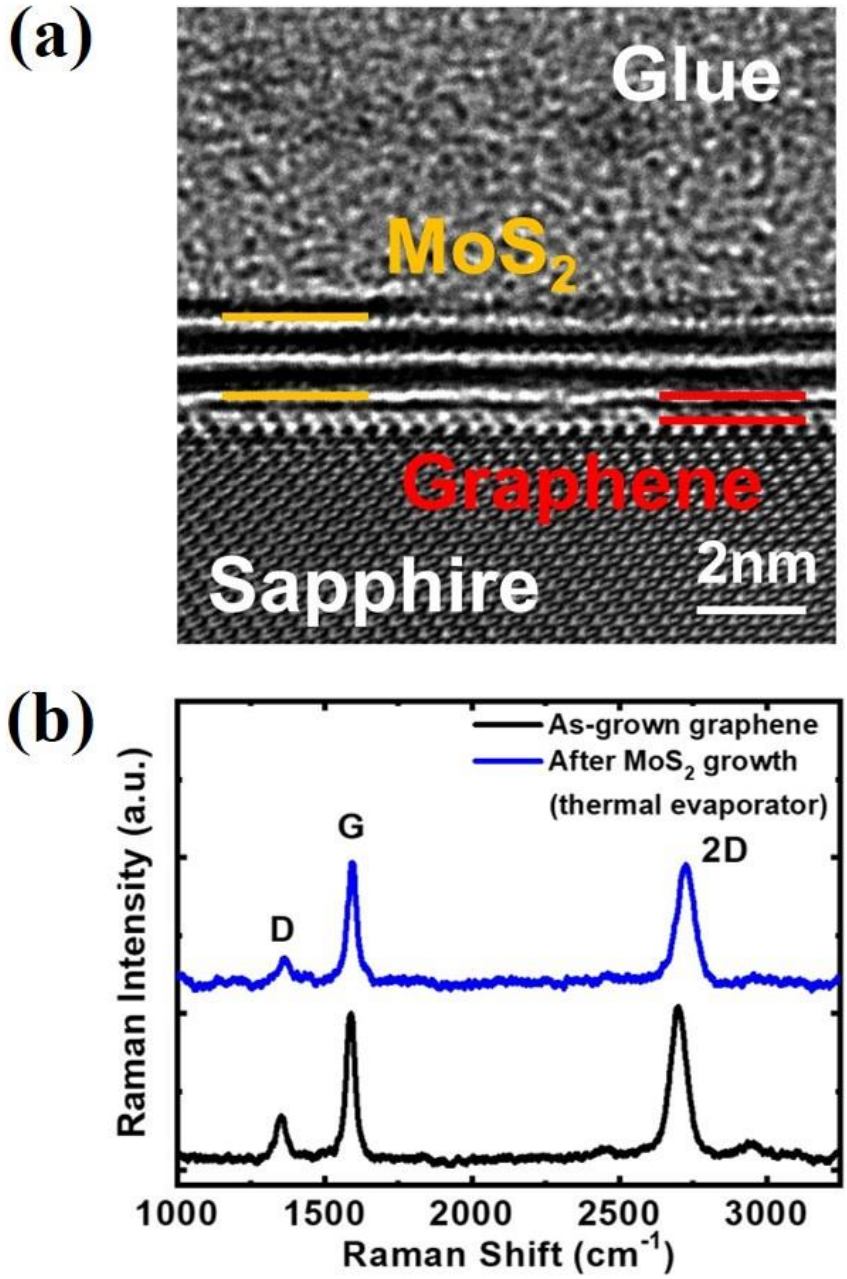

Figure 3-6 (a) The cross-sectional HRTEM image and (b) the Raman spectrum of the sample showing the characteristic Raman peaks of graphene of sample after the MoS_2 growth prepared by using the thermal evaporator. The Raman spectrum of the as-grown graphene film is also shown in (b) for comparison.

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The fabrication procedure for the top-gate graphene transistors with and without the MoS_2 passivation layers is shown in figure 3-7 (a). To prevent the non-uniform precursor distribution of the top dielectric layer on 2-D material surfaces, a thin 5 nm Al_2O_3 layer is deposited by using a e-beam deposition system before the ALD growth procedure [50]. Devices with 30 nm Al_2O_3 dielectric layer in total and channel length/width 5/40 μm are fabricated. The I_D-V_{GS} curves of the two devices with and without the MoS_2 passivation layers at V_{DS} = 1.0 V are shown in figure 3-7 (b). By using the equation $\mu_{FET} = \frac{1}{V_{DS}}\frac{t}{\varepsilon}\frac{L}{W}\frac{dI_{DS}}{dV_{GS}}$, where t is the oxide thickness, ε is the dielectric constant of Al_2O_3, L is the channel length, W is the channel width and $\frac{dI_{DS}}{dV_{GS}}$ is the slope of transfer characteristic of the device at V_{DS} = 1V. The derived hole and electron mobility values of the device without the MoS_2 passivation layer are 9.3 and 3.8 $cm^2/V{\cdot}s$, respectively. Compared with the bottom-gate transistors fabricated by using the graphene films prepared through the same approach, much lower mobility values are observed of the top-gate graphene transistor with no passivation layers. The results reveal that although thin body can be achieved for 2-D material top-gate transistors, significant influence from the top dielectric layer will be brought to the thin channel with few atomic layers. Compared with the device with no passivation layers, the derived field-effect hole and electron mobility values of the device with the bi-layer MoS_2 passivation layer are 35.0 and 8.2 $cm^2/V{\cdot}s$, respectively.

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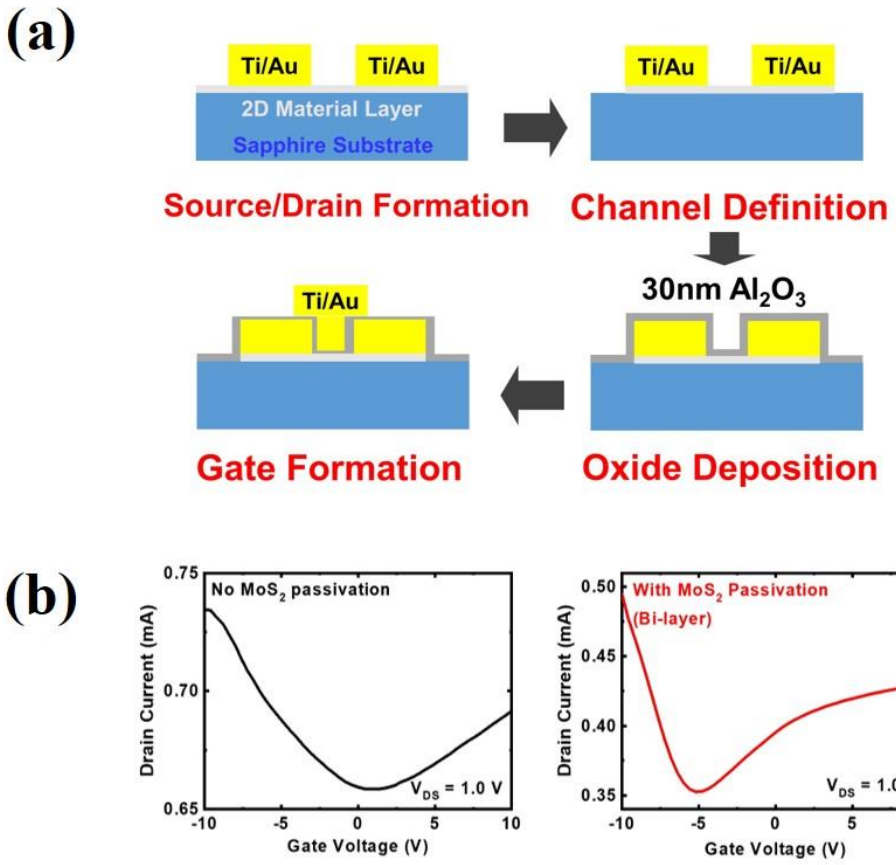

Figure 3-7 (a) The fabrication procedure and (b) the I_D-V_{GS} curves of the top-gate graphene transistors with and without the MoS_2 passivation layer.

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Compared with the Hall mobility value, lower field-effect mobility values are observed for the device. Since the growth mechanisms of the MoO_3 sulfurization at high temperatures include the planar MoS_2 growth and the MoO_3 segregation . The in-complete MoS_2 coverage across the graphene surface may be obtained for the sample [28]. Part of the graphene channel may still contact directly with the top dielectric layer. In this case, a lower field-effect mobility value will be obtained for the device. To solve this problem, a low-temperature sulfurization procedure should be developed in the future to prevent the MoO_3 segregation. Nevertheless, significant increase of field-effect mobility of the device with passivated channels suggests that the MoS_2 layer can effectively act as a passivation layer to the graphene channel.

Since one major advantage of 2-D materials for device applications is the thickness controllability down to one 2-D material layer, the other sample with mono-layer MoS_2 grown on the graphene film is prepared. The Raman spectra of the samples with bi-layer and mono-layer MoS_2 films grown on graphene surfaces are shown in Figure 3-8 (a). The two characteristic Raman peaks E^1_{2g} and A_{1g} of MoS_2 is shown in the figure. As shown in the figure, the energy difference (Δk) between the two MoS_2 characteristic Raman peaks drops from 22.4 to 20.4 cm^{-1}. Since bi-layer MoS_2 is observed from the HRTEM image (Figure 3-6 (a)) for the sample with Δk value 22.4 cm^{-1} and the Δk value would decrease with decreasing MoS_2 layer numbers, the results suggest that a mono-layer MoS_2

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is obtained for the sample with Δk value 20.4 cm^{-1}. Following similar procedure, the sample with a mono-layer MoS_2 passivation layer is also fabricated into top-gate transistors, the I_D-V_{GS} curve of the device at V_{DS} = 1.0 V is shown in Figure 3-8 (b). The derived hole and electron mobility values of the device are 30.0 and 9.5 $cm^2/V{\cdot}s$, respectively, which are close to the value of the device with a bi-layer MoS_2 passivation layer. The results reveal that by using 2-D materials as the passivation layer, thinnest thickness down to one 2-D material layer can be achieved.

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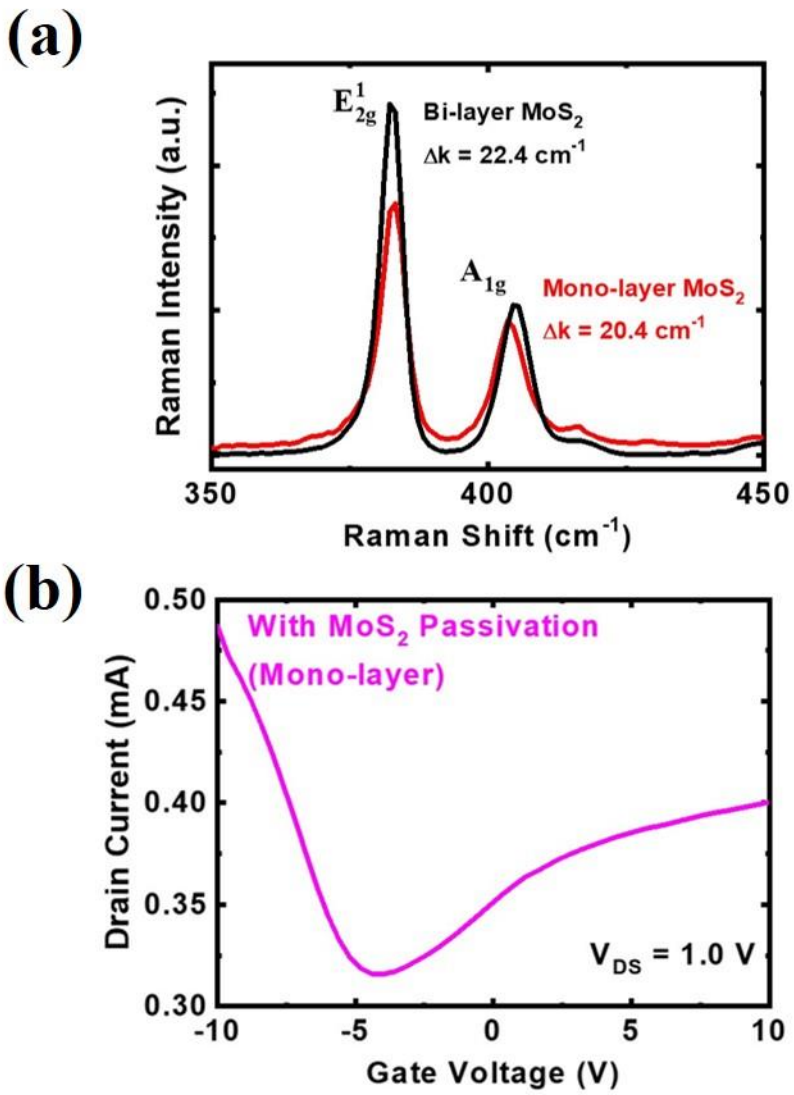

Figure 3-8 (a) The Raman spectra of the samples with bi-layer and mono-layer MoS_2 films grown on graphene surfaces. (b) The I_D-V_{GS} curve of the top-gate graphene transistor at V_{DS} = 1.0 V with a mono-layer MoS_2 passivation layer.

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3.2.3 Conclusion

In conclusion, we have demonstrated that layer-number-controllable MoS_2 films can be grown on graphene surfaces by sulfurizing pre-deposited MoO_3 films by using the thermal evaporator. With no additional damages introduced during the growth procedure, significant device performance enhancement is observed for the top-gate graphene transistors with the MoS_2 passivation layer. The results have demonstrated that a less conductive 2-D material can act as an efficient passivation layer for conductive 2-D material channels when top-gate device architecture is adopted. The possibility of further reducing the passivation layer thickness to one 2-D material layer is advantageous for fabrication of electronic devices with reduced line widths.

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3.3 In-plane Gate Graphene Transistors (IPGTs) with MoS_2 Passivation Layers

We demonstrate in-plane gate transistors based on the molybdenum disulfide (MoS_2)/graphene hetero-structure. The graphene works as channels while MoS_2 functions as passivation layers. The weak hysteresis of the device suggests that the MoS_2 layer can effectively passivate the graphene channel. The characteristics of devices with and without removal of MoS_2 between electrodes and graphene are also compared. The device with direct electrode/graphene contact shows a reduced contact resistance, increased drain current, and enhanced field-effect mobility. The higher field-effect mobility than that obtained through Hall measurement indicates that more carriers are present in the channel, rendering it more conductive.

3.3.1 Device fabrications of IPGTs

The graphene films were grown by using the chemical vapor deposition (CVD) in a hot furnace at 1050 ºC with the ethane precursor and Ar/H_2 carrier gas directly on sapphire substrates. With the graphene/sapphire sample as the new substrate, 1.0 nm thick molybdenum trioxide (MoO_3) was deposited on the graphene/sapphire substrate by using the thermal evaporation. The sample was then sulfurized in a furnace at 850 °C to convert

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MoO_3 into MoS_2. After the definition of large-area contact electrodes through typical photolithography, in-plane gate transistors were fabricated with the aid of e-beam lithography. The electrodes composed of 50 nm Au/10 nm Ti were deposited with the e-beam evaporator. For the removal of MoS_2 beneath the electrodes, we used a customer-designed low-pressure RF oxygen plasma system to perform ALE. The plasma power was kept at 20 W, and the background pressure was maintained at 0.4 Torr with a 30 sccm oxygen gas flow during the removal process. The etching time was 10 s. After this, the sample was dipped into deionized water for 10 s to detach the topmost oxidized MoS_2 layer.

3.3.2 The influence of gate-channel separations of IPGTs

For demonstrating the feasibility of 2-D materials on the architecture of in-plane gate transistors, a graphene film grown directly on sapphire substrates is prepared. The Raman spectrum of the sample is shown in Figure 3-9 (a). The ratio of D/G peak is around 0.4, indicating that while a continuous graphene film could be grown directly on sapphire substrates using CVD, a limited graphene grain size and non-negligible defect density featured by the D peak were still present in the graphene film. The detailed discussions on the growth and formation mechanisms of the graphene films grown directly on sapphire substrates are demonstrated elsewhere [30]. Nevertheless, compared with the

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counterparts grown on copper foils, the graphene films grown on sapphire substrates require no transferring processes and can further simplify the device fabrication. Therefore, this growth scheme is suitable for the architecture of in-plane gate transistors. The fabrication steps of the in-plane gate graphene transistor are illustrated in Figure 3-9 (b). The large-area electrodes were fabricated using photolithography. After that, the e-beam lithography was utilized to fabricate the in-plane gate transistor. The scanning electron microscope (SEM) image of the device near the channel is also shown in Figure 1(b). After the device fabrication procedure, an in-plane gate graphene transistor with channel width/length 500 /500 nm and the gate-channel separation 300 nm can be fabricated. The voltage-current transfer curves of the device under forward and reverse biases at $V_{\mathrm{DS}} =$ 0.5 V are shown in Figure 3-9 (c). Standard characteristics of graphene transistor with the Dirac point located at about 30 V gate biases are observed for the device. Since we could not observe current modulation with gate biases for the device with larger gate separation 1000 nm, the transistor performances of the device should be attributed to the smaller gate separation 300 nm and therefore, higher electric fields between gate and source electrodes. Further investigation is still required in the future to clarify the operation mechanisms of the device. We use the following formula to estimate the field-effect mobility μ_{FET} at $V_{\mathrm{DS}} =$ 0.5 V (linear regime):

$$\mu_{\mathrm{FET}} = \frac{1}{g}\frac{1}{V_{\mathrm{DS}}}\frac{d}{\varepsilon}\frac{L}{W}\frac{\mathrm{d}I_{\mathrm{DS}}}{\mathrm{d}V_{\mathrm{GS}}},$$

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where d is the gate-to-channel separation; ε is the dielectric constant of air; L and W are the channel length and width, respectively; and the factor $g = 2$ accounts for the number of in-plane gates at two sides of the channel. The derived hole and electron mobilities of the device are 90.0 and 77.0 $cm^2/V{\cdot}s$, respectively. The hole mobility is close to that commonly observed for the directly grown graphene films via the Hall measurement (p-type, 100-200 $cm^2/V{\cdot}s$). This supports the architecture of in-plane gate transistors for 2-D materials and shows the potential for abandoning gate dielectrics. However, the Dirac point shifts to -4.0 V under reverse gate bias, indicating that the water and gas molecules may significantly influence the device performance under the ambient condition [51].

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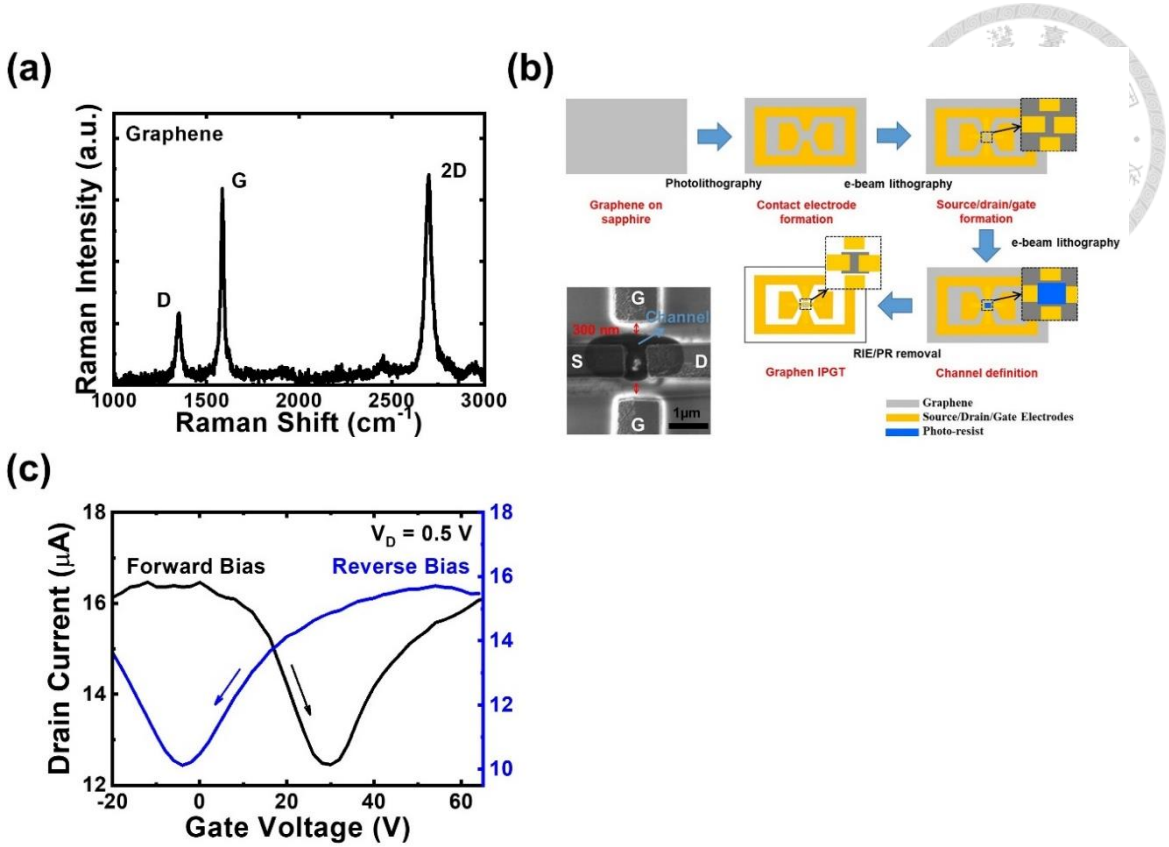

Figure 3-9 (a) The Raman spectra of the graphene film grown directly on sapphire substrates. (b) The fabrication steps of the in-plane gate transistors. The SEM image of the device is also shown in (b). (c) The transfer curve of the in-plane gate transistors measured under forward and reverse gate biases at V_{DS} = 0.5 V.

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3.3.3 IPGTs with MoS_2 passivation layers

The passivation layer is a possible solution to prevent the attachment of water or gas molecules to the graphene channel [51]. Since dielectric materials for gates may bring additional influence to the graphene channel and do not conform to the concept behind in-plane gate transistors, the most promising candidate for passivation layers should be other 2-D material layers. In previous publication, we have demonstrated that by sulfurizing pre-deposited Mo films, MoS_2 layers could be grown on graphene surfaces [30]. However, since the Ar plasma in the radio-frequency sputtering system may bring additional damage to graphene films, we formed the MoS_2/graphene hetero-structure by sulfurizing the MoO_3 film deposited with the thermal evaporator. The Raman spectra of the MoS_2/graphene hetero-structure corresponding to the characteristic peaks of graphene and MoS_2, respectively, are shown in Figure 3-10 (a). The observation of both the graphene and MoS_2 Raman peaks indicates that the MoS_2/ graphene hetero-structure is formed after the sequential growth of graphene and MoS_2. The difference Δk between the two Raman peaks of MoS_2 is 21.3 cm^{-1}, indicating the presence of bi-layer MoS_2 after the sulfurization procedure [52]. On the other hand, the similar D/G peak ratios of graphene before and after the MoS_2 growth (around 0.4) suggest that by using the thermal evaporator, only a limited amount of damage was introduced to the graphene film during the deposition of MoO_3. Following the similar device fabrication of standalone graphene

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in-plane gate transistors (Figure 3-9 (b)), MoS_2/graphene in-plane gate transistors with gate separations of 300 nm were fabricated. The transfer curves of the device under forward and reverse biases at $V_{DS} = 1.0$ V are shown in Figure 3-10 (b). Similar with the graphene in-plane gate transistors, the device behaves as a typical graphene transistor. The Dirac point at a positive $V_{GS} = 10.0$ V indicates a p-type graphene channel under forward biases. The weak hysteresis on the transfer curves suggests that the MoS_2 layer can effectively protect the channel from contaminants in environments. By using Eq. (1), the derived hole and electron mobilities of the device are 61.0 and 31.0 $cm^2/V{\cdot}s$, respectively. Compared with the hole mobility 100-200 $cm^2/V{\cdot}s$ of the graphene film on sapphire from Hall measurements, the field-effect mobility is lower. The derived field-effect mobility values are also lower than the standalone graphene in-plane gate transistors discussed in the last section. The results may be attributed to the high contact resistance at the electrode/MoS_2 interfaces which hinder the supply of carriers as the gate voltage is changed [53].

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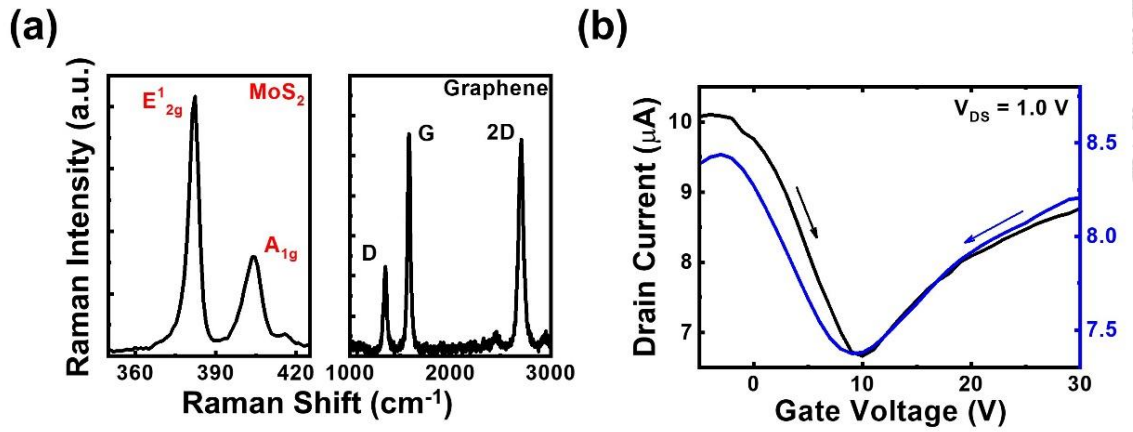

Figure 3-10 (a) The Raman spectra of MoS_2/graphene hetero-structure and (b) the transfer curve of the in-plane gate transistor at V_{DS}= 1.0 V.

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3.3.4 Conclusion

With the graphene on sapphire as the new substrate, we grew MoS_2/graphene hetero-structures by sulfurizing the MoO_3 film deposited on graphene. In-plane gate transistors were fabricated on the MoS_2/graphene hetero-structure. By using MoS_2 as the passivation layer, a weak hysteresis on the transfer curves is observed for the in-plane gate transistor, which suggests that the MoS_2 layer can effectively protect the graphene channel from contaminants in environments. After the removal of MoS_2 beneath electrodes, the direct contact between electrodes and graphene shows reduced contact resistance. This increases the field-effect mobility and drain current of the device. The architecture of in-plane gate transistor provides an alternate approach for the fabrication of 2-D transistors with the less non-ideal interface effect.

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Chapter 4 2-D Memories

4.1 Charge Storage of Isolated Mono-layer MoS_2 in Top-gate MoS_2/graphene Transistors

Epitaxially grown bi-layer molybdenum disulfide (MoS_2) is grown on mono-layer graphene by sulfurizing MoO_3 films deposited by using the thermal evaporation. The similar Hall mobility values of the mono-layer graphene obtained before and after the MoS_2 growth indicate that there is no additional to the underlying 2-D material layer during the deposition/sulfurization procedure. By using the atomic-layer etching (ALE) technique, the topmost mono-layer MoS_2 is isolated from the source/drain electrodes. With the isolated mono-layer MoS_2 on top of the graphene channel, a hysteresis loop is observed for the top-gate graphene transistor. The long retention time for the "0" and "1" states of the device suggests an effective electron storage in the isolated MoS_2 layer. The van der Waals interface between MoS_2 and graphene will prevent charge transfer when no external electrical fields are applied to the charge storage layer. The 1T0C memory module fabricated by using thin 2-D material layers can be advantageous for the application of dynamic random access memories (DRAMs) with reduced line widths.

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4.1.1 Device fabrications of top-gate graphene transistors with isolated MoS_2 layers

To demonstrate the charge storage effect of the MoS_2 layer in the bi-layer MoS_2/mono-layer graphene hetero-structure, a top-gate transistor is fabricated by using photo-lithography open source and drain electrodes. The fabrication procedure is shown in Figure 4-1. To isolate the topmost MoS_2 layer from the source/drain electrodes, one-time ALE is performed before the source/drain metal deposition. The left partial oxidized mono-layer MoS_2 would protect the graphene film from the damage of the oxygen plasma during the ALE procedure. After the channel definition by using photo-lithography, a 5 nm Al_2O_3 dielectric layer is deposited on the sample by using the atomic layer deposition. Before the ALD growth, The 5 nm Al_2O_3 dielectric layer is deposited on the sample by using the e-beam evaporation to deposition for better precursor distribution during the ALD growth procedure. The total dielectric layer thickness would therefore reach 10 nm. The source, drain and gate electrodes are deposited by using a e-beam evaporation system with 10 nm Ti and 100 nm Au. After the memory devide fabrication procedure, The devices with 10 nm $Al2O_3$ dielectric layer in total and channel length/width 5/40 μm are fabricated. The optical microscope of is shown in Figure 4-2.

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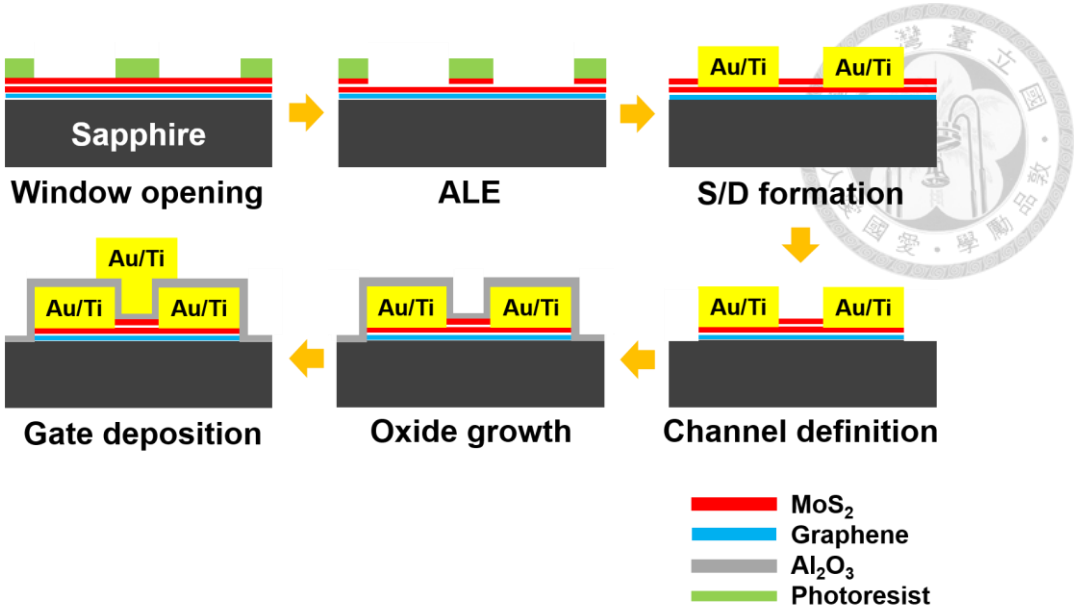

Figure 4-1 The fabrication steps of the top-gate graphene transistor with an isolated MoS_2 layer on top of the graphene channel.

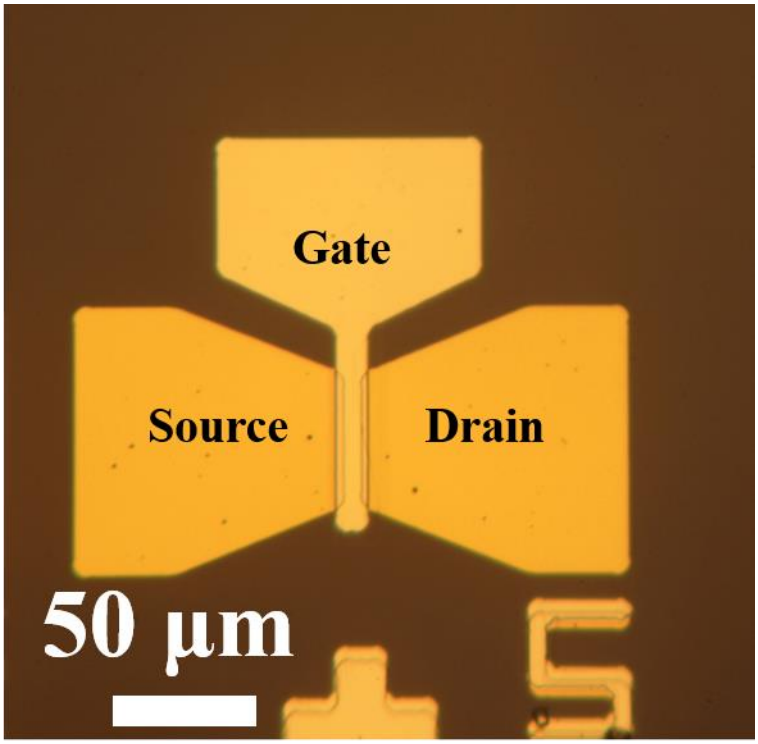

Figure 4-2 The optical microscope picture of memory device.

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4.1.2 The transfer curves of top-gate graphene transistors with isolated MoS_2 layers

As a result, after the growth of bilayer MoS_2 on graphene, electrons transfer from the former to latter, and the graphene channel remains p-type. In this condition, the drain current would first decrease as V_{GS} increases, as can be told from Figure 4-3. Still, compared with the V-shaped transfer curve of typical graphene transistors, no modulation of electron gas is observed as V_{GS} further increases. A possible reason for this phenomenon is that at a sufficiently large V_{GS}, a considerable amount of negative (defect) charge trapped around the bilayer MoS_2 and oxide may begin to screen the electric field applied by the gate. As a result, the increment of the effective field asserted on the graphene becomes small and can no longer lower the energy of Dirac cones for further accommodation of mobile electrons.

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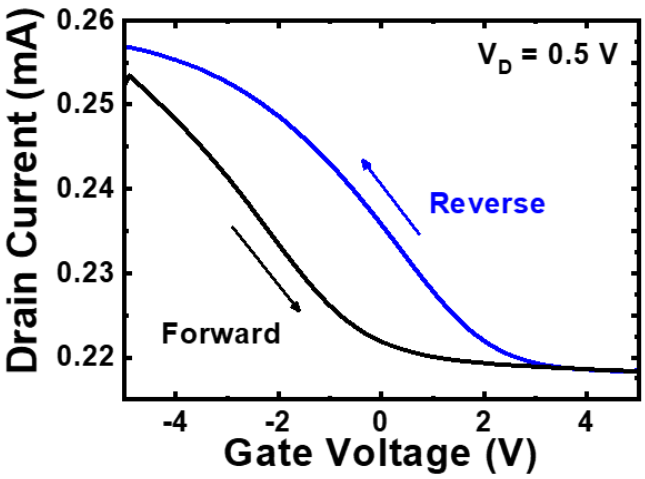

Figure 4-3 The forward and reverse transfer curves of the top-gate transistor at V_{DS} = 0.5 V.

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On the possible origin of current bistability, we look into four regimes marked on the simplified transfer curves shown on the left side of Figure 4-4. Regimes I and III correspond to bistable states of drain current, and regimes II and IV represent the states at very positive and negative gate bias voltage V_{GS}, respectively. Let us consider device configurations on the hysteresis loop (I→II→III→IV) and begin from the low-current state (regime I). As shown in Figure 4-4, at the low-current state under forward operation (increasing V_{GS}), both the Dirac cones and conduction band in MoS_2 are lowered. The empty valence band of graphene is gradually filled while the conduction band in MoS_2 remains mostly empty. The defect states near the interface of topmost layer of MoS_2 and oxide are not replenished easily because the electron density in the conduction band of MoS_2 is still too low to supply the trap states. The direct tunneling of electrons from the graphene through the bilayer MoS_2 is yet to be turned on to fill defect states. In consequence, the Fermi level of defect states E_{FD} is lower than that $E_{F,G}$ of the graphene. As V_{GS} enters regime II, the number of holes in the lower branch of Dirac cones becomes fewer, and the conduction band of the bilayer MoS_2 is further lowered. Electrons in the lower branch of graphene may enter the conduction band of bilayer MoS_2 via thermionic emissions and replenish the defect states through trapping. Also beyond a level of V_{GS}, the direct tunneling of electrons in the graphene into defect states becomes possible, and the unoccupied defect states below $E_{F,G}$ would be soon filled. The tunneling marks the

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onset of significant charge accumulation near the topmost layer of MoS_2 and oxide. Beyond this level of V_{GS}, the gate field would be screened and cannot initiate the accommodation of electrons in the upper branch of Dirac cones. This impedes the modulation of electron gas as V_{GS} further increases.

As the gate voltage V_{GS} decreases from regime II, the tunneling process from the graphene to defect states is turned off. The elevated conduction band of bilayer MoS_2 also hinders the escape of electrons trapped in defect states. Under such circumstances, the negative charge corresponding to the defect states in regime III cannot be evacuated and would attract mobile holes into the graphene channel. In terms of band diagrams, the Dirac cone in regime III would be higher than that in regime I, enabling the accommodation of relatively more holes than those in the latter. The bistability on drain current reflects the distinct hole densities in these two regimes. If the gate bias V_{GS} turns more negative from the high-current state in regime III into regime IV, the tunneling from defect states to the graphene is switched on. The negative charge that attracts the holes in graphene is swept into the graphene channel and gets evacuated. After then, if the gate bias voltage V_{GS} increases from regime IV, the absence of negative charge near the topmost layer of MoS_2 and oxide would direct the device configuration into regime I rather than III. This would complete one cycle of current bistability. From the discussion above, we see that the key to current bistability in our extremely thin top-gate transistor

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is the capability of bilayer MoS_2 to separate defect charge near its topmost layer and oxide from the graphene channel. In other words, in the same range of tunneling voltage, a few layers of semiconducting 2-D materials can be as robust as ten-nanometer thick conventional semiconductors in charge isolation. The van der Wall interaction which results in weak interlayer coupling of atomic orbitals may be the reason why it requires higher fields or fewer atomic layers for the direct tunneling to take place in 2-D materials. This, nevertheless, makes 2-D materials a promising candidate in memory devices based on the 1T0C architecture.

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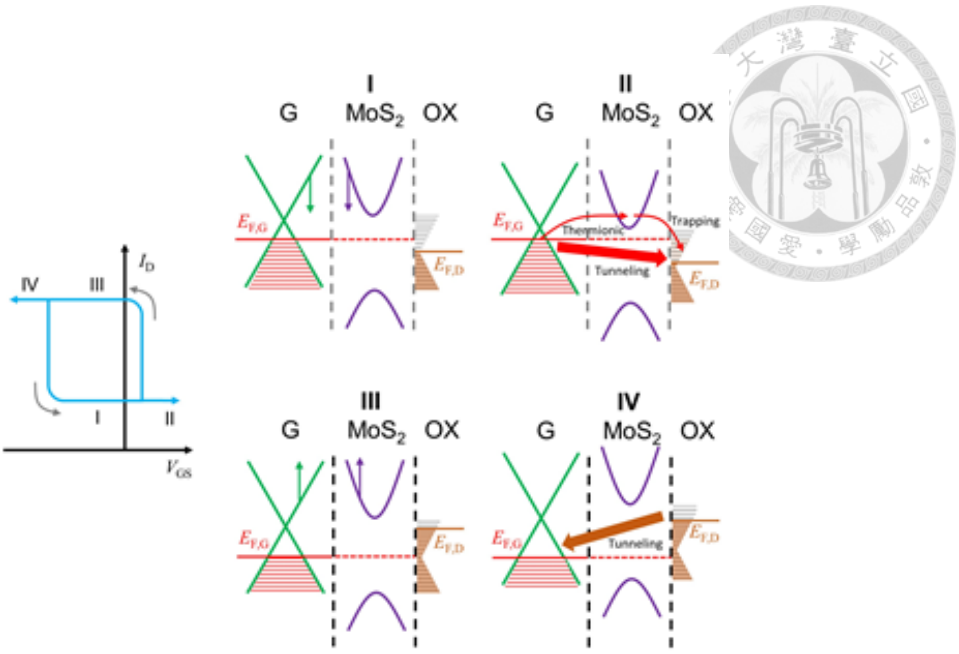

Figure 4-4 Simplified transfer curves under the forward and reverse operations (left). Four regimes are marked on them, and the corresponding band diagrams are depicted on the right.

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4.1.3 Read-write operations of MoS_2/graphene memories

The transient behaviors of the top-gate transistor are shown in Figure 4-5a. If we apply a gate voltage V_{GS} of +5 V to the device for 10 s and then switch V_{GS} to 0 V, the drain current jumps to the high-current state of about 0.27 mA. On the other hand, if V_{GS} is initially set to −5 V for 10 s and switched to 0 V, the low-current state of around 0.24 mA is observed. A current difference of about 30 μA is maintained up to tens of seconds or even longer. The results are consistent with the bistable states on transfer curves. When a positive gate bias voltage V_{GS} is applied (MoS_2 layer is charged with electrons; write) and then switched to 0 V, the "1" state is set. On the other hand, as a negative gate bias voltage V_{GS} is applied (electrons are depleted from the MoS_2 layer; erase) and then brought back to 0 V, the device returns to "0" state. The long retention times of the "0" and "1" states feature the robust charge storage around the isolated MoS_2 layer. One complete write-read-erase-read cycle of the device versus time are shown in Figure 5b. As shown in the figure, clear "0" and "1" states are observed after the "erase" and "write" steps. Although the difference between "0" and "1" states of this memory device is not as large compared with the conventional Si-based transistors. The actual current difference between "0" and "1" states of this device is about several tens of μA as shown in Figure 5b, which is still large considering the mono-layer thin charge storage layer MoS_2. Therefore, it is possible to further enlarge the difference between "0" and "1" states

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simply by increasing the MoS_2 layer numbers. Based on the similar concept, it is also possible to integrate the 2-D material storage layer into the Si devices for memory applications. Further investigation is still required in the future. The consistent current levels of both the “0” and “1” states in various cycles are signs of the stable operation. The repeatability also indicates the potential of the device for memory applications.

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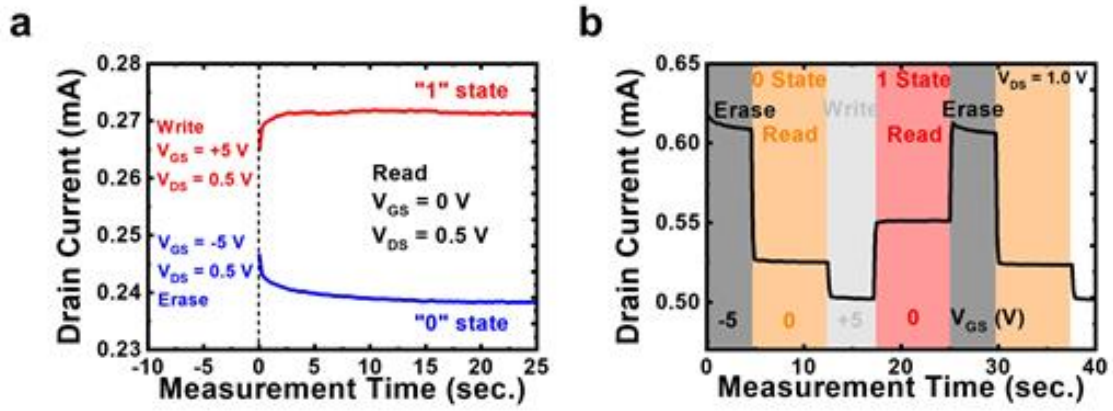

Figure 4-5 (a) The transient responses of drain current of the top-gate transistor at V_{DS} = 0.5 V. The gate bias voltage V_{GS} is first set to $\pm$ 5 V for 10 s, respectively, before turned to 0 V. (b) A complete write-read-erase-read cycle versus time of the device.

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4.1.4 Conclusion

In conclusion, we have demonstrated that by using thermal evaporator, uniform and wafer-scale MoS_2 can be grown non-destructively onto directly CVD-grown graphene on sapphire substrates. By using the ALE procedure to isolate the topmost MoS_2 layer of the bi-layer MoS_2 film from the source/drain electrodes, a possible memory architecture based on 2-D materials is proposed. With the semiconducting 2-D material (MoS_2) as the charge separation layer and the conductive counterpart (graphene) as the charge-detection channel, a top-gate transistor can function as a memory device. The long retention times of the "0" and "1" states indicate that robust charge storage can be realized with isolated bilayer MoS_2. A 1T0C memory module may be implemented with the thin hetero-structure of 2-D materials. Since 2-D materials can be transferred to different substrates, it is possible to integrate the thin and flexible memory devices into organic electronics and wearable circuits in addition to the memories with reduced thickness.

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4.2 Multi-layer MoS_2 for Memory Applications

In the previous section, it has been demonstrated that with an isolated MoS_2 layer on top of the graphene channel, memory devices based on the 2-D material hetero-structure can be fabricated. The actual thickness of the device is reduced to < 2.0 nm with bi-layer MoS_2 grown on top of mono-layer graphene. This is also an all-2-D material memory device. However, since MoS_2 can act both as the charge storage and the channel layers, it is possible to further simplify the fabrication procedure of 2-D memories based on multi-layer MoS_2 instead of the MoS_2/graphene hetero-structure. In this section, we have demonstrated that by using the atomic-layer etching technique (ALE), one and two layers of isolated MoS_2 layers are fabricated on two and one layers of MoS_2 channels. Memory operations with long retention times are observed for the devices with the isolated MoS_2 layers. The program and erase voltages are reduced to < 5.0 V. The higher drain current ratios for the device with two isolated MoS_2 layers at “one” and “zero” states suggest that more electrons can be stored in MoS_2 with increasing layer numbers.

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4.2.1 Device fabrications of top-gate MoS_2 transistors with isolated MoS_2 layers

To demonstrate the possible memory operations of the multi-layer MoS_2 sample. A top-gate transistor architecture is adopted. The fabrication procedure of the top-gate MoS_2 transistor is shown in Figure 4-6. To form isolated MoS_2 layers on top of the transistor channels, we have performed ALEs before the source/drain electrode formation. For source/drain electrodes, 20 nm titanium (Ti) is deposited on the MoS_2 surface followed by the other 100 nm gold (Au) deposition using a e-beam evaporator. After the 30 nm Al_2O_3 growth, the gate electrode with the same composition as the source/drain electrodes is deposited. Two devices with one- and two- times ALE procedures are fabricated. For comparison, another device with no ALE procedure is also fabricated. The channel length/width are 5 and 40 μm, respectively.

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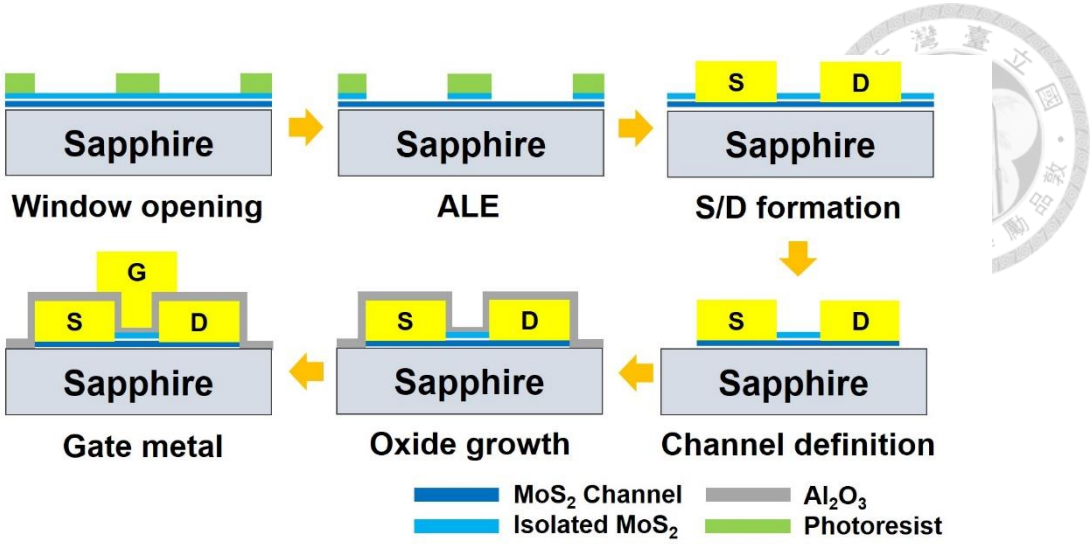

Figure 4-6 The fabrication flow of the multi-layer MoS_2 transistors.

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4.2.2 The transfer curves of top-gate MoS_2 transistors with isolated MoS_2 layers

The transfer curves of the three devices under forward and reverse gate biases at V_{DS} = 1.0 V are shown in Figure 4-7. As shown in the figure, no hysteresis loop is observed for the device with no ALE procedure before the source/drain metal deposition. For the device with one-time ALE procedure, since there is one isolated MoS_2 layer on top of the two-layer MoS_2 channel, a small hysteresis loop is observed for the device. Different from the p-type characteristics of the graphene channel, n-type MoS_2 channels are observed for the device. In this case, higher drain currents are observed for the device under forward gate biases due to the electron depletion at the isolated MoS_2 layer under negative gate biases. For the device with two-time ALE procedures, a larger hysteresis is observed. Since there are two MoS_2 isolation layers on top of the one-layer MoS_2 channel, more electrons can be stored in the MoS_2 isolation layers. The other phenomenon observed in Figure 4-7 is the reducing drain current levels with increasing ALE times. Compared with the three-layer MoS_2 channel for the device without any ALE procedure, two- and one-layer MoS_2 channels are obtained after one and two ALE procedures. In this case, lower drain current levels will be observed with increasing ALE times due to the fewer MoS_2 layers left as the transistor channel for current flow.

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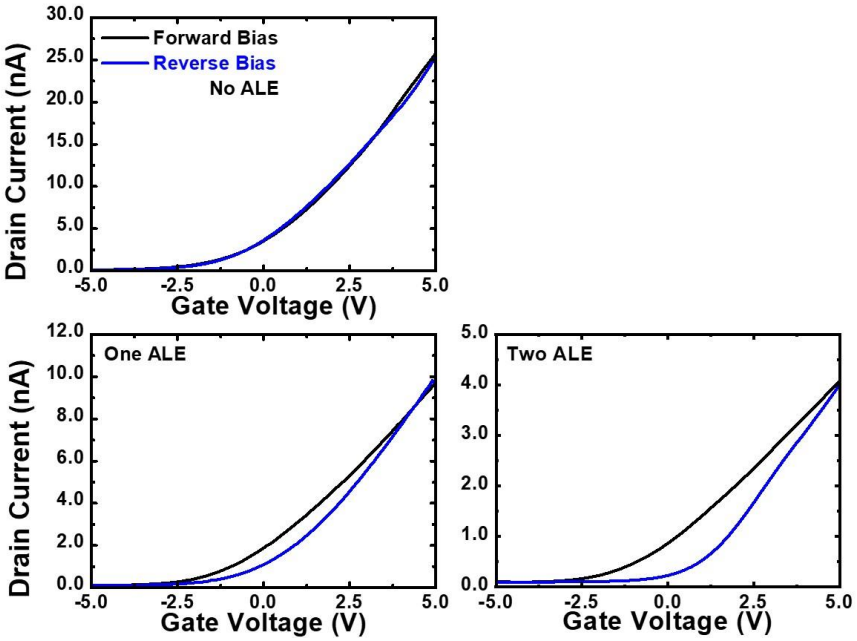

Figure 4-7 the transfer curves of the three devices with zero, one and two ALE procedures at V_{DS} = 1.0 V.

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4.2.3 Read-write operations, operation speed and charge storage of MoS_2 memories

The program/read/erase/read cycles of the device with two ALE procedures are shown in Figure 4-8 (a). The “program/erase” gate voltages are set as -5.0 and 5.0 V, respectively. The program/erase time is below 1.0 seconds. The “read” gate voltage is set as 0.0 V. As discussed in the last section, n-type channels are observed for the MoS_2 transistor. In this case, when negative gate biases are applied, electrons in the isolated MoS_2 layers will be depleted such that a higher electron density in the MoS_2 channel and therefore, a higher drain current will be observed at zero gate bias. This is the “1” state of the MoS_2 memory. On the contrary, when positive gate biases are applied to the device, electrons will accumulate and store in the isolated MoS_2 layer, which will result in a lower drain current under the zero gate bias. This will be the “0” state of the device. The program/read/erase/read cycles shown in Figure 4-8 (a) precisely follow the descriptions discussed above. Clear “1” and “0” states are observed for the device. The drain currents at V_{DS} = 1.0 V measured with time at zero gate biases after the -5.0 and 5.0 V gate voltage stresses, respectively, for 10 sec. are shown in Figure 4-8 (b). The slow varying in the drain current levels with time over 30 minutes. Suggests that a long retention time is observed for electrons stored in the isolated MoS_2 layers, which will make this device a non-volatile memory. The results also indicate that it is difficult for electron diffusion at

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the interface of the isolated MoS_2 and MoS_2 channel layers without the external electric field applied vertically to the MoS_2 layers.

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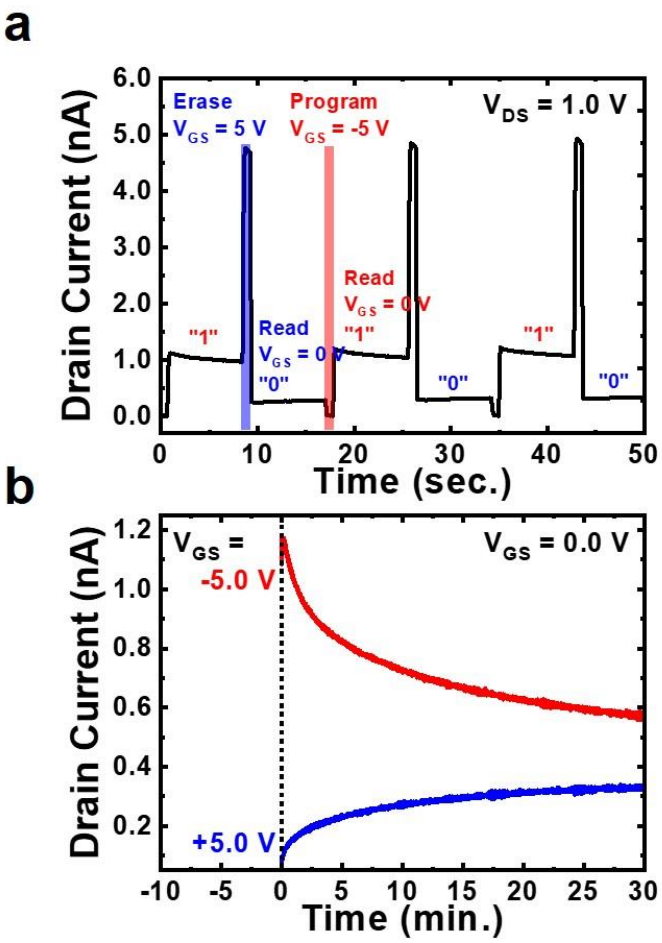

Figure 4-8 (a) The program/read/erase/read cycles and (b) The drain currents measured with time at zero gate biases after the -5.0 and 5.0 V gate voltage stresses of the device with two ALE procedures at V_{DS} = 1.0 V.

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The drain current ratios at “1” and “0” states of the two devices with one and two ALE procedures after different program/erase gate biases are shown in Figure 4-9. The read voltage is set as 0.0 V. The program/erase gate biases at each data point is of the same value but different polarities. The program/erase time is 5 seconds. As shown in the figure, the drain current ratio will remain at 1.0 for program/erase gate voltages < 2.0 V. After that, the drain current ratios will increase until a saturation is reached at program/erase gate voltage ~ 7.0 V. A minimum program/erase gate voltage 2.0 V required to observe the memory operations of the device suggests that although the MoS_2 layers are close to each other, the attachment through van der Waals forces will still limit the carrier transport in between the 2-D material layers. The drain current ratios of the device with two ALE procedures at program/erase gate voltage 7.25 V is ~8.8, while the value for the device with one ALE procedure is ~2.8. The saturation current ratio is not proportional to the isolated MoS_2 layer numbers as expected. A possible mechanism responsible for this phenomenon may be the influence of the dielectric layer to the topmost MoS_2 layer. Fewer electrons can be stored at the topmost MoS_2 layer than the second MoS_2 layer underneath. On the other hand, the minimum program/erase voltage ~ 2.0 V required for the device operation also provides a possibility to slightly change the read voltage to enlarge the “1” and “0” state current ratios. The program/read/erase/read

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cycles of the device with two ALE procedures are shown in Figure 4b. The "program/erase" gate voltages are set as -5.0 and 5.0 V, respectively.

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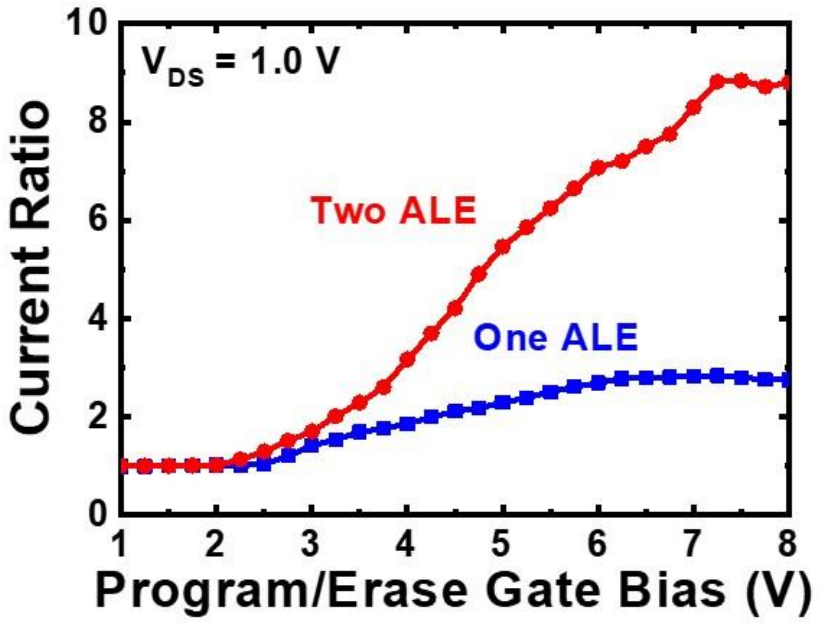

Figure 4-9 The drain current ratios at “1” and “0” states of the two devices with one and two ALE procedures after different program/erase gate biases. The read voltage is set as 0.0 V and V_{DS} = 1.0 V.

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4.3 Conclusion

In conclusion, we have demonstrated that by using the ALE technique, isolated MoS_2 layers can be fabricated on the MoS_2 channels by using tri-layer MoS_2 samples grown on sapphire substrates. Long retention times and increasing current ratios between “1” and “0” states with increasing isolated MoS_2 layer numbers have revealed the potential of 2-D materials for memory device applications. The low program/erase voltages also indicate a low power consumption of the device. It is possible to further decrease the program/erase voltages by decreasing the oxide thicknesses.

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Chapter 5 Conclusion

In conclusion, we have demonstrated that thin Al_2O_3 layers can be grown on MoS_2 surfaces without influence its Raman and PL characteristics. With the thin separation layer between mono-layer 2-D materials, luminescence enhancement is observed by stacking the same 2-D materials (MoS_2 with MoS_2). The Dual color emission can be observed by stacking different 2-D materials (MoS_2 with WS_2). We have demonstrated that with ALD precursor soaking time treatment on the interfaces of 2-D crystals with other materials, difference stacked structures can be established. The stacking of 2-D materials with other materials will bring wide applications of 2-D materials in practical devices.

For the establishment of TMD/graphene hetero-structures, we have demonstrated that layer-number-controllable MoS_2 films can be grown on graphene surfaces by sulfurizing pre-deposited MoO_3 films which deposited by the thermal evaporator. Thermal evaporation can prevent the RF sputtering Ar plasma damage. With no additional damages introduced during the growth procedure, significant device performance enhancement is observed for the top-gate graphene transistors with the MoS_2 passivation layer. The results have demonstrated that a less conductive 2-D material can act as an efficient passivation layer for conductive 2-D material channels when top-gate device architecture is adopted. The possibility of further reducing the passivation layer thickness

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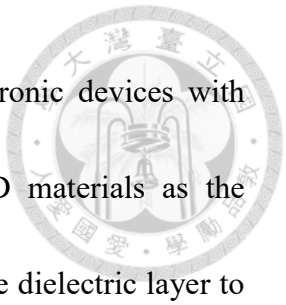

to one 2-D material layer is advantageous for fabrication of electronic devices with reduced line widths. Besides the adoption of less conductive 2D materials as the passivation layers, an alternate approach to avoid the influence of the dielectric layer to the transistor channel would be the in-plane gate transistor architecture. By using the same MoS_2/graphene hetero-structures, in-plane gate transistors were fabricated. Although there is no oxide/2D material interface in this device architecture, the water and oxygen molecular from the atmospheric environment will still influence the device performances. Therefore, by using MoS_2 as the passivation layer, we can observe a weak hysteresis by the transfer curves for the in-plane gate transistor, which suggests that the MoS_2 layer can effectively protect the graphene channel from contaminants in environments. After the removal of MoS_2 beneath electrodes, the direct contact between electrodes and graphene shows reduced contact resistance. This increases the field-effect mobility and drain current of the device. The architecture of in-plane gate transistor provides an alternate approach for the fabrication of 2-D transistors with the less non-ideal interface effect.

Besides the application of passivation layers of MoS_2 in the MoS_2/graphene hetero-structure, MoS2 layers can also act as charge storage layers for memory applications. By using the ALE procedure to isolate the topmost MoS_2 layer of the bi-layer MoS_2 film from the source/drain electrodes, a possible memory architecture based on 2-D materials is proposed. With the semiconducting 2-D material (MoS_2) as the charge storage layer and

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the conductive counterpart (graphene) as the charge-detection channel, a top-gate transistor can function as a memory device. The long retention times of the “0” and “1” states indicate that robust charge storage can be realized with isolated bilayer MoS_2. A 1T0C memory module may be implemented with the thin hetero-structure of 2-D materials. Since 2-D materials can be transferred to different substrates, it is possible to integrate the thin and flexible memory devices into organic electronics and wearable circuits in addition to the memories with reduced thickness.

To simplify the fabrication procedure, the concept of 2D material hetero-structure memories can be further expanded to individual 2D materials such as multi-layer MoS_2. We have demonstrated that by using the ALE technique, isolated MoS_2 layers can be fabricated on the MoS_2 channels by using tri-layer MoS_2 samples grown on sapphire substrates. The retention times is longer then MoS_2/graphene hetero-structure and increasing current ratios between “1” and “0” states with increasing isolated MoS_2 layer numbers have revealed the potential of 2-D materials for memory device applications. The low program/erase voltages also indicate a low power consumption of the device. It is possible to further decrease the program/erase voltages by decreasing the oxide thicknesses.

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Future work

In this thesis, 2-D memory devices were successfully demonstrated by using the MoS_2/graphene hetero- and multi-layer MoS_2 homo- structures. Although good device performances with high endurance are observed for these devices. There is still a need to further extend the concept to other 2D materials for even better device performances. On possible candidate is WSe_2. WSe_2 is another typical semiconducting TMDs, with a bandgap 1.3 eV (indirect, bulk) and 1.8 eV (direct, monolayer). Due to its low effective mass, it has been reported that single-layer WSe_2 has high room temperature phonon-limited electron mobility (exceeds 700 $cm^2V^{-1}s^{-1}$) [54]. Therefore, WSe_2 is being considered as potential candidates for channel materials for memory device applications in the future. In this thesis, we have observed that the device performances such as higher drain currents can be observed after removal the MoS_2 on MoS_2/graphene hetero-structures in chapter 3. The results have demonstrated that the high contact resistance at the metal/2-D material interfaces will be another issue influencing the device performances. In one pervious publication, it has been demonstrated that higher drain currents can be obtained by using 2-D material antimonene on the MoS_2 surface as the contact metal [53]. With the assist of van der Waals epitaxy on 2-D material surfaces, less dependence on the lattice structures of the epi-layers to the substrates will help the formation of elemental 2-D materials on semiconductor 2-D material surfaces. Since most

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elemental 2-D materials are of semi-metals, the reduced contact resistance at the elemental 2D material/semiconductor 2-D material interfaces will be significantly reduced. Therefore, the replacement of contact metals with lower contact resistance for the memory device should be the other important topic to be studied in the future. On the other hand, further investigation on the operation speed of the memory device should also be conducted in the future. In chapter 4, with the semiconducting 2-D material (MoS_2) as the charge separation layer and the conductive counterpart (graphene) as the charge-detection channel. An easy carrier transportation at the 2-D material interface is observed. A detailed investigation on the carrier transport at the 2-D material interfaces would bring more different device applications to 2-D materials in the future.

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[1] **Po-Cheng Tsai**, Hon-Chin Huang, Chun-Wei Huang, Shoou-Jinn Chang, and Shih-Yen Lin, “Luminescence Enhancement and Dual-Color Emission of Stacked Mono-layer 2D Materials”, Nanotechnology, vol. 31, no. 36, pp. 365702 June 2020.

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