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應用於第六代通訊系統之 D 頻段放大器、二倍頻器與單刀單擲切換器之研究

Research of D-band Amplifier, Frequency Doubler and SPST Switch for 6th-Generation Communication

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承翰

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中文摘要

本論文包含三個部分。第一部分是應用於 6G 通訊系統發射端的 D 頻段寬頻驅動放大器設計與量測結果，使用 65 奈米金氧半場效電晶體製程。第二部分是應用於 6G 通訊系統本地震盪源之 D 頻段倍頻器設計與量測結果，使用 65 奈米金氧半場效電晶體製程。第三部分為應用於涵蓋 6G 多頻段之超寬頻單刀單擲開關設計與量測結果，使用 90 奈米金氧半場效電晶體製程。

首先是預計應用於 300 GHz 相位陣列收發系統之驅動放大器，為了增強混頻器產生的訊號，所提出的放大器不僅需要寬頻寬，還必須提供足夠的增益和輸出功率性能。因此，針對 65 奈米金氧半場效電晶體製程在 D 頻段的增益性能較差的問題，採用增益提昇技術來提高增益。此外，本設計也採用了補償匹配技術來獲得更寬的頻寬。量測結果表明，所提出的驅動放大器在大於 10 dB 小訊號增益下表現出 128 至 170 GHz 的頻寬。輸出 1dB 壓縮點功率在 140、150 和 160 GHz 時分別為-7.4、-3.7 和-7.3 dBm。此外，整體晶片包總面積為 0.38 平方毫米，其中核心電路面積僅為 0.1 平方毫米。

第二部分提出應用在 140 GHz 收發系統之本地震盪源組件之低功號 D 頻段二倍頻器。採用補償馬遜平衡不平衡轉換器來最小化幅度和相位差，以獲得更好的轉換增益和基頻抑制性能。為了增強轉換和輸出功率性能，採用了共源共柵拓樸架構。並採用增益提昇技術進一步提升轉換增益效能。量測結果表明，此二倍頻器的工作頻率範圍為 143 GHz 至 170 GHz，在 158 GHz 達到-3.5 dB 的峰值轉換增益。輸入功率為 4.3 dBm 時，在 158 GHz 處輸出峰值功率為 0.76 dBm。在整個頻帶內，基頻抑制大於 41.3 dBc。此外，此二倍頻器的直流功耗為 16.3 mW，含 pad 面積為 0.262 平方毫米。

最後一部分介紹了專為跨多頻段發射機系統設計的超寬頻超緊湊單刀單擲 (SPST) 開關。所提出的開關僅由四個電晶體和幾個電阻器組成，沒有任何大型被動元件，如電感器、變壓器或傳輸線，以最小化晶片尺寸。量測結果顯示，所提出的單刀單擲開關在 DC 至 140 GHz 與 170 GHz 頻寬內，分別實現小於 3.3 dB 與 3.6 dB 的插入損耗，具有覆蓋多個超寬頻收發系統的潛力。回波損耗 140 GHz 與 170 GHz 內分別優於 14 dB 與 9 dB；隔離度在相同頻段則分別優於 22 dB 與 18.5 dB，展現良好的關斷狀態性能。此開關的核心面積為 980 μm^2，比先前報告的毫米

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波寬頻單刀單擲開關面積小兩個數量級或更多。

關鍵字: 互補式金氧半導體、寬頻放大器、二倍頻器、單刀單擲開關、馬遜平衡不平衡轉換器、D 頻段、300 GHz 相位陣列收發系統、140 GHz 相位陣列收發系統。

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ABSTRACT

This thesis consists of three main parts. The first chapter presents the design and measurement results of a D-band broadband driving amplifier for a 6th-generation wireless system (6G) transmitter fabricated in a 65-nm CMOS process. The second chapter describes the design and measurement results of a D-band doubler for a local oscillation chain in a 140 GHz transceiver system fabricated in a 65-nm CMOS process. The last chapter discusses the design and measurement of an ultra-wideband and compact switch for multi-band coverage in a 6G transceiver system fabricated in a 90-nm CMOS process.

The first part focuses on a driving amplifier designed for the potential network in a 300 GHz phased-array transceiver system. To boost the signal generated by the mixer, the proposed amplifier not only demands a wide bandwidth but also has to provide sufficient gain and output power performance. Therefore, the gain-boosting technique was adopted to boost gain due to the poor gain performance of CMOS in the D-band. Additionally, the compensated matching technique is also utilized in this design to obtain a broader bandwidth. The measurement results show that the proposed driving amplifier exhibits a bandwidth of 128 to 170 GHz over a 10 dB small signal gain. The output 1-dB compression point power levels are -7.4, -3.7, and -7.3 dBm at 140, 150, and 160 GHz, respectively. Furthermore, the total area with pads is 0.38 mm^2 (0.42 mm×0.9mm), and the core area of the proposed amplifier is 0.1 mm^2 (0.15 mm×0.665mm).

The second part presents a D-band doubler designed for 140 GHz transceivers. The compensated Marchand balun is adopted to minimize the amplitude and phase difference to obtain better conversion gain and rejection performance. In order to enhance the conversion and output power performance, a cascode topology is adopted.

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The gain-boosting technique is utilized to further increase the conversion gain performance. The measurement results show that the proposed frequency doubler covers from 143 GHz to 170 GHz, and the peak conversion gain is -3.5 dB occurs at 158 GHz. The peak output power exhibits 0.76 dBm at 158 GHz with 4.3 dBm input power. The fundamental rejection is greater than 41.3 dBc in the entire frequency bandwidth. Furthermore, the proposed frequency doubler consumes 16.3 mW DC power, and occupies 0.262 mm^2 (0.4 mm × 0.655 mm) with all pads.

The last part introduces an ultra-wideband and ultra-compact single-pole-single-through (SPST) switch designed for a multi-band transceiver system. The proposed switch is composed of only four transistors and several resistors, and without any large passive components such as an inductor, transformer, or transmission lines to minimize the chip size. The proposed switch achieves less than 3.3 dB and 3.6 dB insertion loss from DC to 140 GHz and 170 GHz, which has the potential to cover multiple ultra-wideband transceiver systems. The return loss is greater than 14 dB and 9 dB within 140 GHz and 170 GHz, respectively. The off-state performance of isolation is better than 22 dB and 18.5 dB within 140 GHz and 170 GHz, respectively. The proposed switch achieves an IP_{1dB} of 10.6 dBm at 75 GHz and an IP_{1dB} of 10 dBm at 110 GHz. The core area of the switch is 980 μm^2, which is two or more orders of magnitude smaller than the previously reported mm-Wave broadband SPST switch.

Index Terms – CMOS, broadband amplifier, frequency doubler, SPST switch, Marchand balun, D-band, 300 GHz phased-arrays transceiver system, 140 GHz phased-arrays transceiver system.

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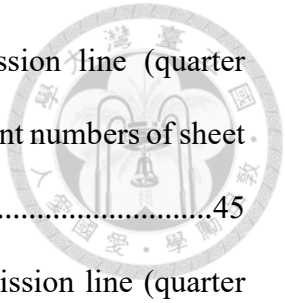

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Chapter 1 Introduction

1.1 Background and Motivation

1.1.1 300-GHz Phase-Array Transceiver System

Wireless communication has flourished in recent years, with the high demand for high data transmission rates, low latency, and the ability to support the connection of numerous devices. The millimeter-wave (mm-Wave) transceiver systems have become more and more popular due to their advantages of providing ultra-wide bandwidth and high data transmission rate. The Fifth-Generation (5G) has been implemented in recent years, with the advantage of up to one hundred times faster data transmission rates, tens of times lower latency, and the capability to connect millions of devices simultaneously. As 5G has begun to commercialize, the research on 6G has also begun [1]. While 5G focuses on the mm-Wave frequency bands, with a maximum of up to 28-38 GHz, 6G extends the operation frequency to terahertz (THz), including the low-band of below 1 GHz, the mid-band of 1-7 GHz and 7-24 GHz, the high bands of mm-Wave band 24-92 GHz and sub-THz band 92-300 GHz [2].

Fig. 1.1 shows the expected evolution from 5G to 6G, including achieving hundreds of times faster data transmission rate, tens of times lower latency, and supporting more connected devices to enhance the Internet of Things (IoT) [3-9]. With the support of 6G, an abundance of applications such as artificial intelligence (AI), immersive experience, low latency, and reliable communication can be realized.

Nevertheless, as shown in Fig. 1.2, one of the greatest challenges of using higher frequencies is signal attenuation over distance, which is particularly severe in THz systems. To address these issues, techniques such as phased-array beamforming and

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multiple-input multiple-output (MIMO) are used. The phased-array system with beamforming can control the phase of different antenna units to enhance the signal. The MIMO system can increase the channel capacity, transmission rate, and connection stability. Both techniques have been adopted to generate a more powerful signal to cope with the massive transmission loss in high frequencies.

In such a broadband transceiver system, the wideband driving amplifier plays a crucial role. Signal attenuation is severe in the millimeter wave and sub-terahertz frequency bands, and nonlinear effects can easily affect signal quality. The driving amplifier can provide good linearity, reduce signal distortion, and ensure that the modulated signal will not be deformed due to nonlinear effects. In addition, it is necessary for D-band amplifiers to have high linearity and broadband performance to accommodate the ultra-wide bandwidth needed by 6G applications. Their high-efficiency performance at these high frequencies is vital to the success of phased-array systems and multi-beam operations to deliver the next generation of wireless services that are high-performance and high-reliability.

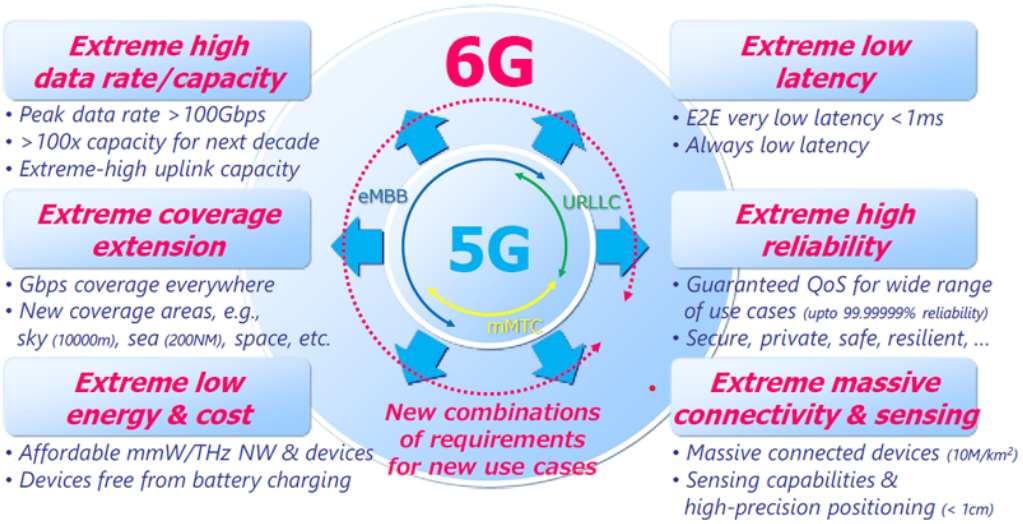

Fig. 1.1 Demands for 6G Wireless Communication Technology.

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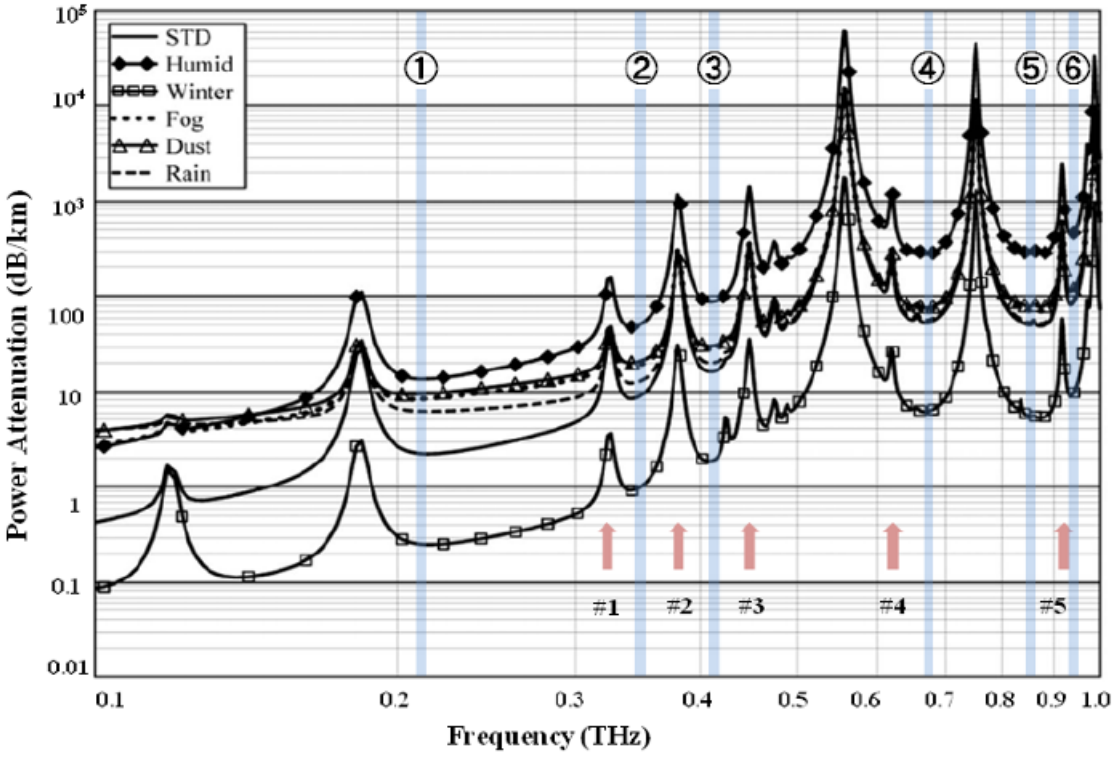

Fig. 1.2 The atmospheric attenuation of electromagnetic waves at sea level.

1.1.2 D-band Local Oscillation (LO) Chain [10-14]

With the advancement of wireless transmission, the millimeter-wave and sub-terahertz wireless systems are becoming more and more significant. Another issue, except for the high transmission loss, is the demand for a high-frequency local oscillator. It is indispensable in the transceiver system, especially near D-band and sub-THz, to maintain the functionality of signal processing. However, it is very challenging to directly generate the high-frequency signal source due to inherent device and material limitations, which result in poor performance, limited tuning range, and so on.

To deal with these challenges, frequency multiplication techniques have been proposed. The concept starts from a low-frequency, low-phase-noise signal source, and frequency multipliers sequentially upconvert the signal to the desired frequency. Power amplifiers are added in the path to compensate for the loss introduced by the frequency

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multiplier to ensure adequate LO power is provided to the transceiver system. Different from direct generation, the frequency multiplication technique enables the oscillator to operate at a relatively lower frequency, which has superior performance than those at high frequencies. Furthermore, the design of frequency multiplication is more flexible and lower cost, which makes it widely recognized as the most practical and scalable solution.

In this technique, the frequency doubler plays a vital role by efficiently generating the second harmonics while simultaneously suppressing the undesired harmonics. The overall LO chain characteristics are highly dependent on the performance of the frequency multiplier, including bandwidth, conversion gain, output power, harmonic suppression, and DC power consumption. Among the designs of frequency doublers, the push-push architecture and Marchand balun design have a decisive influence on the characteristics of the frequency doublers.

In summary, the successful development of high-performance D-band local oscillator chains is primarily dependent on effective frequency multiplication, especially through the careful design of the frequency doublers. These components are crucial for meeting the strict requirements for phase noise performance, output power level, and spectral purity needed by advanced wireless communication and sensing systems that function in the D-band.

1.1.3 An Ultra-Wideband Switch [15, 16]

The ultra-wide bandwidth benefits the 6th generation(6G) communication, allowing high data transmission rates and low latency. Moreover, various applications such as holographic imaging, augmented reality, and perception fusion are built on high-bandwidth characteristics. Nevertheless, it is also one of the most challenging specifications of the 6G transceiver system design. The transceiver system that can cover

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from low frequency to the THz frequency requires extremely wideband RF front-end design capabilities. Traditional solutions for a multi-band application are usually achieved by multiple switch elements or sub-modules to form a complex band switching architecture. Despite its ability to optimize the performance in particular frequency bands, it has the disadvantages of complex control logic, diverse paths, and has accumulated considerable losses.

As a result, an ultra-wideband switch can serve as an effective solution. This type of switch offers exceptional bandwidth performance, capable of covering the desired frequency bands, thereby significantly reducing the number of components required in control circuits. Furthermore, its simple structure makes it suitable for integration into advanced processes, particularly in applications that do not necessitate frequency band switching. Examples include high-bandwidth scanning modules, continuous spectrum detectors, and single-channel broadband transceiver systems. Achieving multi-frequency band coverage with a single switch component not only minimizes signal paths and connection interfaces but also reduces losses and stray effects associated with packaging and wiring, ultimately enhancing the reliability and performance of the overall system.

In conclusion, the introduction of an ultra-wideband switch represents not only a simplified circuit design solution but also a strategic component choice that addresses the fundamental requirements of 6G technology. It has demonstrated significant advantages in enhancing performance, reducing power consumption, streamlining structure, and adapting to the trends of multi-mode and multi-frequency operation. Consequently, it is poised to become an indispensable component of future ultra-wideband RF systems.

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1.2 Literature Surveys

The literature surveys include D-band broadband amplifier, D-band frequency doubler, and DC to D-band SPST switch design in the CMOS Process.

1.2.1 D-Band Broadband Amplifier in CMOS Process

Driving amplifiers play a crucial role in transceiver systems. As signals pass through lossy components such as frequency multipliers, power dividers, and mixers, they weaken or attenuate. This attenuation can lead to saturation in the subsequent components. Therefore, it is essential to have a well-designed driving amplifier that can magnify the signals while meeting the required frequency range and power specifications of the system. Table 1.1 summarizes the previously published D-band amplifiers

Due to the high loss of passive components at high frequencies and the limitation of f_{max} and f_T in the CMOS process, it is challenging to design CMOS circuits above 100 GHz. As a result, various techniques to further increase gain performance have been adopted by previous works. The simplest approach involves cascading multiple stages to achieve higher gain and wider bandwidth [17-19]. Additionally, employing a differential topology can also enhance output power [18]. However, too many stages cascading not only consume large DC power but are also potentially vulnerable to inter-stage instability. The gain-boosting technique is a widely used method for enhancing gain performance in the D-band [20-22]; however, the addition of a transmission line has to be carefully chosen to avoid causing oscillation due to its positive feedback. Another method to obtain higher gain is the Gmax-core topology [23]; properly choosing three passive elements around a common source transistor can significantly increase the gain in the desired frequency, while the bandwidth may be limited and vulnerable to process variation of

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passive elements. The compensated matching technology is also commonly used in millimeter-wave amplifier design, which broadens the bandwidth of the entire circuit by matching each stage to different frequencies [24].

The proposed D-band driving amplifier is based on a cascode topology. Adopting a gain-boosting technique to further enhance gain performance and a compensated matching technique to broaden the bandwidth.

Table 1.1 Summary of previously published D-band amplifiers.

Ref.	**Process**	**Topology**	**Freq. (GHz)**	**Peak Gain (dB)**	OP_{1dB} **(dBm)**	P_{dc} **(mW)**	**Area (mm^2)**
[17]	40-nm CMOS	8 x CS	101.5~142.1	20.6	-3.1@120GHz	45	0.225
[18]	65-nm CMOS	Differential 6 x CS	110.6~121.8	13.8	-14@116GHz	40	0.605
[19]	65-nm CMOS	4 x cascode + 1 x CS	110~180*	19	N/A	66	0.37
[21]	28-nm CMOS	2 x CS + 3 x cascode	129~157.5	16.3	-3.7@150GHz	38.8	0.62
[22]	65-nm CMOS	3 x cascode	188~192	16.3	N/A	33.4	0.46
[23]	65-nm CMOS	2 x G_{max}-core	147~158	17.9	-6.9@152.2GHz	13.7	0.193

*Gain > 10 dB

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1.2.2 D-Band Frequency Doubler in CMOS Process

Table 1.2 summarizes recent publications on D-band CMOS frequency doublers. There are several topologies for implementing frequency multiplication; the most widely used are the injection-locked frequency doubler (ILFD) [25, 26] and the push-push frequency doubler [27-31]. However, due to the limitation of the locking range and high-quality factor of the LC resonator, the bandwidth of the injection-locked frequency doubler is restricted. Thus, for wideband purposes, push-push topology would be more favorable. In this architecture, harmonic signals can be obtained by operating the transistors nonlinearly. Additionally, by separating the input signal into out-of-phase signals and combining them after transistors, odd harmonic tones were canceled while even harmonics remained. Therefore, the push-push doubler exhibits excellent suppression of fundamental and third-order harmonics even without additional filtering designs.

The study [26] presented the D-band injection-locked doubler fabricated in 65-nm CMOS. The circuit consists of a Pierce oscillator injection locked by a push-push pair. The frequency doubler exhibits an operating bandwidth of 106 GHz to 128 GHz, with a core power dissipation of 6 mW. With an approximate 3 dB loss in the output buffer, the doubler achieves a -2.6 dBm output power, given a 0 dBm input power.

With the advantage of a wide bandwidth, the Marchand balun is commonly used to generate the out-of-phase signal. The amplitude and phase difference of the two ports will significantly influence the harmonic rejection and conversion efficiency of the doubler. [27] demonstrates the novel method for tuning the amplitude and phase difference by adding a compensation transmission line. With the compensated Marchand balun, this frequency doubler, fabricated in 65-nm CMOS, achieves a bandwidth of 95 to 150 GHz and over 30 dB rejection, along with a conversion gain of -8 dB and a peak output power

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of 3 dBm. To further increase higher-order harmonic rejection, the Chebyshev filter was implemented in [28]. This push-push doubler fabricated in 90-nm CMOS achieves 158 to 204 GHz bandwidth along with -7.8 dB conversion gain and 2.2 dBm peak output power. With the filter design, the 3rd and 4th harmonic rejection is greater than 20 dBc and 23 dBc, respectively. For the purpose of having a higher conversion gain performance, [29] added a common gate transistor after the push-push doubler stage, which makes the full circuit a cascode topology, allowing the circuit to have higher conversion gain and output power. Adding a transmission line at the gate of the common gate transistor can further boost the gain performance. The paper [30] presents a high-efficiency push-push frequency doubler fabricated in 22-nm FDSOI CMOS. It achieves a peak conversion gain of -5.5 dB and an output power of 4.1 dBm, spanning a bandwidth of 125 to 145 GHz. The peak drain efficiency (P_{out}/P_{dc}) is 11.8%. In the work presented in [31], another push-push D-band doubler fabricated in 45-nm SOI CMOS achieves a bandwidth of 135 to 160 GHz, along with a -3 dB peak conversion gain and a peak output power of 3.5 dBm.

In the proposed D-band frequency doubler, a push-push topology and a compensated Marchand balun structure were adopted to achieve a broader bandwidth. A common source transistor is cascading after the push-push doubler to increase the conversion gain. Furthermore, the gain-boosting technique was implemented to maximize the conversion gain. Meanwhile, the low DC power consumption and specific input and output power must also be satisfied to match the system requirement.

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Table 1.2 Summary of previously published D-Band Frequency Doubler.

Ref.	Process	3-dB Bandwidth (GHz)	Peak CG (dB)	P_{out}@P_{in} (dBm)	FR (dBc)	P_{dc} (mW)	Area (mm^2)
[26]	65-nm CMOS	106-128	0	-2.6@0	N/A	23	0.27
[27]	65-nm CMOS	95-150	-8	3@11	> 30	19.2~22.8	0.24
[28]	90-nm CMOS	158-204	-7.8	2.2@10	N/A	88.8	0.41
[29]	28-nm CMOS	126-146	-4.5	0.5@5	> 34	12	0.49
[30]	22-nm FDSOI CMOS	125-145	-5.5	4.1@11.7	N/A	24.7	0.326
[31]	45-nm SOI CMOS	135-160	-3	3.5@7	N/A	25	0.44

1.2.3 DC to D-band SPST switch in CMOS Process

The design of the switch focuses on several performances, including covering bandwidth, insertion loss, and return loss at the on-state, the isolation at the off-state, and the power handling capability. From the viewpoint of the transceiver system, the area of the switch is also a very crucial characteristic. Table 1.3 summarizes the previously published broadband SPST switches.

[32] demonstrates a G-band SPST switch used in an on-off-key (OOK) module. The body of the transistor is floating through a large transistor to improve the insertion loss performance. Moreover, a grounded co-planar wave guide (GCPW) folded coupled line topology is developed to improve the switch isolation and lower its insertion loss simultaneously. It demonstrates a minimum of 2.38 dB insertion loss, larger than 8 dB

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return loss, and more than 30 dB isolation in the frequency range of 140 to 183 GHz. In the study [33], with a combination of front-gate and back-gate biasing, unique to fully depleted silicon-on-insulator (FDSOI) MOSFETs, the threshold voltage of the MOSFET can be decreased. This results in lower ON-state resistance (R_{ON}), and thus, the insertion loss of the switch can be improved. The switch achieves an insertion loss of 3.1 dB and an isolation of 37 dB at 220 GHz, as well as a peak isolation of 58 dB at 200 GHz. [34] shows a switch based on PIN-diode topology fabricated in a 90-nm SiGe BiCMOS process. The switch achieves a bandwidth of over 125 GHz with an insertion loss of less than 3.6 dB and an isolation of more than 22 dB up to 160 GHz, while maintaining an OP1dB of 23 dBm. [35] illustrates a digitally tunable SPST switch based on the traveling-wave concept, fabricated in 22-nm FDSOI CMOS. Compared to a standard CMOS, silicon-on-insulator (SOI) technologies offer the advantage of a lower parasitic capacitance, since the transistor is isolated from the silicon substrate. The switch achieves an insertion loss of 1.2 dB at 60 GHz and a 24-dB isolation at 60 GHz with a bandwidth of 10-110 GHz, while having an IP_{1dB} of 7 dBm at 24 GHz.

Finally, [36] demonstrates an ultra-compact SPST switch by non use of large-area passive components, such as inductors, transformers, and transmission lines. With the advantages of a special device option (BFMOAT) and the SOI process, the substrate parasitic effects and parasitic capacitance are reduced. The measured results reported a DC to 110 GHz bandwidth with an insertion loss of less than 3.1 dB, an isolation of better than 22 dB, and a return loss of better than 12 dB. The core area occupied only 160 μm^2, which is up to two or more orders of magnitude smaller than prior wideband mm-wave SPST switches.

In the proposed DC to D-band SPST switch, the main structure would only contain four transistors to minimize the area. However, the 90-nm CMOS process does not have

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special device options or SOI advantages to enhance the performance. As a result, the trade-off between the number of series and shunt transistors and the device size selection would be more critical. Moreover, the body floating technique is also adopted in this work to further decrease the insertion loss of the switch.

Table 1.3 Summary of previously published switched.

Ref.	Process	Type	Freq. (GHz)	IL (GHz)	RL (dB)	ISO (mW)	P_{1dB} (dBm)	Core Area (mm^2)
[32]	65-nm CMOS	SPST	140-183	Min. 2.38	> 8	> 30	N/A	0.0067
[33]	22-mm FDSOI CMOS	SPST	DC~220	< 3.1	> 12	> 37	N/A	0.026
[34]	90-nm SiGe BiCMOS	SPST	DC~125	< 3.6	> 10.9	> 22	20@2GHz	0.106*
[35]	22-mm FDSOI CMOS	SPST	10~110	< 1.8	N/A	> 17	7@24GHz	0.18
[36]	22-mm FDSOI CMOS	SPST	DC~110	< 3.1	> 12	> 22.8	10.8@50GHz	0.00016

*Chip Area

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1.3 Contributions

This thesis presents three research contributions. Firstly, a D-band broadband driving amplifier is introduced, adopting a gain-boosting technique and a compensating matching technique to realize high gain and broad bandwidth performance. Secondly, a D-band doubler with push-push topology and gain-boosting technique is developed for the 140 GHz transceiver system. Lastly, a DC to D-band single-pole-single-through (SPST) switch is presented, without using any large area passive element; the switch only occupies 980 μm^2. The major contributions of these circuits are described as follows.

1.3.1 D-band Broadband Amplifier in CMOS process

The proposed D-band broadband amplifier fabricated in a 65-nm CMOS process for a 300-GHz phase-array transceiver system is demonstrated. The D-band broadband amplifier is composed of a three-stage cascode topology along with a gain-boosting technique to further enhance the gain performance. Also, the compensating matching technique is implemented during the circuit design. The proposed amplifier exhibits a wideband performance with a very compact core area.

Experimental results demonstrated that the proposed amplifier achieves 128 to 170 GHz bandwidth with 10 dB signal gain and 21.3 dB peak gain at 165 GHz. The output 1-dB compression point power levels are -7.4, -3.7, and -7.3 dBm at 140, 150, and 160 GHz, respectively. The total power consumption of this work is 39.3 mW, with the core area only 0.1 mm^2. This research was published in the 2024 APMC [37].

1.3.2 D-band Frequency Doubler in CMOS Process

The proposed frequency doubler, fabricated in a 65-nm CMOS process designed for

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the D-band local oscillation chain, is presented. The conversion gain and output power performance are enhanced by cascode topology and gain-boosting technique. With the compensated Marchand balun, the gain and phase difference are minimized, and the doubler exhibits an excellent rejection performance.

The experiment results showed that the 3-dB frequency bandwidth covers from 143 GHz to 170 GHz with a peak conversion gain of -3.5 dB at 158 GHz. The peak output power level is 0.76 dBm at 158 GHz with 4.3 dBm input power. The measured fundamental rejection is greater than 41.3 dBc in the entire frequency bandwidth. With 16.3 mW DC power consumption, the total chip area, including all pads, is 0.262 mm^2.

1.3.3 SPST switch in CMOS Process

An ultra-wideband and ultra-compact SPST switch designed for a multi-band 6G transceiver system fabricated in 90-nm CMOS is showcased. With no large-area occupied passive components, such as inductors or transmission lines, utilized in the design, the proposed switch is able to minimize chip size with a very simple structure.

From the measurement results, the proposed switch achieves less than 3.3 dB and 3.6 dB insertion loss from DC to 140 GHz and 170 GHz, which has the potential to cover multiple ultra-wideband transceiver systems. The return loss is greater than 14 dB and 9 dB within 140 GHz and 170 GHz, respectively. The off-state performance of isolation is better than 22 dB and 18.5 dB within 140 GHz and 170 GHz, respectively. The proposed switch achieves an IP_{1dB} of 10.6 dBm at 75 GHz and an IP_{1dB} of 10 dBm at 110 GHz. The core area of the switch is 980 μm^2, which is two or more orders of magnitude smaller than the previously reported mm-Wave broadband SPST switch.

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1.4 Thesis Organization

The organization of this thesis is shown as follows.

In Chapter 2, a D-band broadband amplifier in a 65-nm CMOS process for a 300-GHz phase-array transceiver system is designed. The design procedures are presented, including device selection and gain-boosting techniques. The chapter also includes simulation results, measurement results, and a comparison table. Additionally, troubleshooting of the design and discussion of the transistor device measurement results will be presented. Finally, a brief conclusion is provided at the end of this chapter.

In Chapter 3, a D-band frequency doubler in a 65-nm CMOS process for a 140 GHz transceiver is demonstrated. The design procedures are described, including biasing and device size selection, compensated Marchand balun design, and gain-boosting technique design. The chapter also includes simulation results, measurement results, and a comparison table. Additionally, a brief conclusion is provided at the end of this chapter.

In Chapter 4, a DC to D-band single-pole-single-through switch in a 90-nm CMOS process for an on-off keying transmitter is presented. The design procedures include device size selection and body floating technique. The chapter also includes simulation results, measurement results, and a comparison table.

Finally, Chapter 5 concludes the conclusion of this thesis.

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Chapter 2 Design of a 128 to 170 GHz Broadband Amplifier with Gain-Boosting Technique in 65-nm CMOS Process

2.1 Introduction

Wireless communication has advanced rapidly due to its wide bandwidth, low latency, and high data rates. However, higher frequencies suffer from severe signal attenuation. The mm-Wave systems leverage phased array beamforming and spatial MIMO to enhance directionality and reduce interference. 5G offers up to 100× faster speeds and much lower latency than 4G, supporting massive device connectivity. Looking ahead, 6G, expected around 2030, will bring even faster speeds, near-zero latency, AI-driven networks, and terahertz communication. As frequencies rise, path loss increases, making high-gain amplifiers critical. Proper gain and power budget planning are essential to maintain signal integrity and system performance.

Fig. 2.1 presents the block diagram of the 300-GHz transmitter system. The driving amplifier is used to amplify the RF signal output from the I/Q sub-harmonic mixer to ensure that its strength is sufficient to drive the subsequent square wave mixer and 300 GHz power amplifier (PA), ultimately increasing the overall transmission power. Also, signal attenuation is severe in the millimeter wave and sub-terahertz frequency bands, and nonlinear effects can easily affect signal quality. The driving amplifier can provide good linearity, reduce signal distortion, and ensure that the modulated signal will not be deformed due to nonlinear effects, affecting the final transmission quality. Table 2.1 shows the design goals of a D-band driving amplifier.

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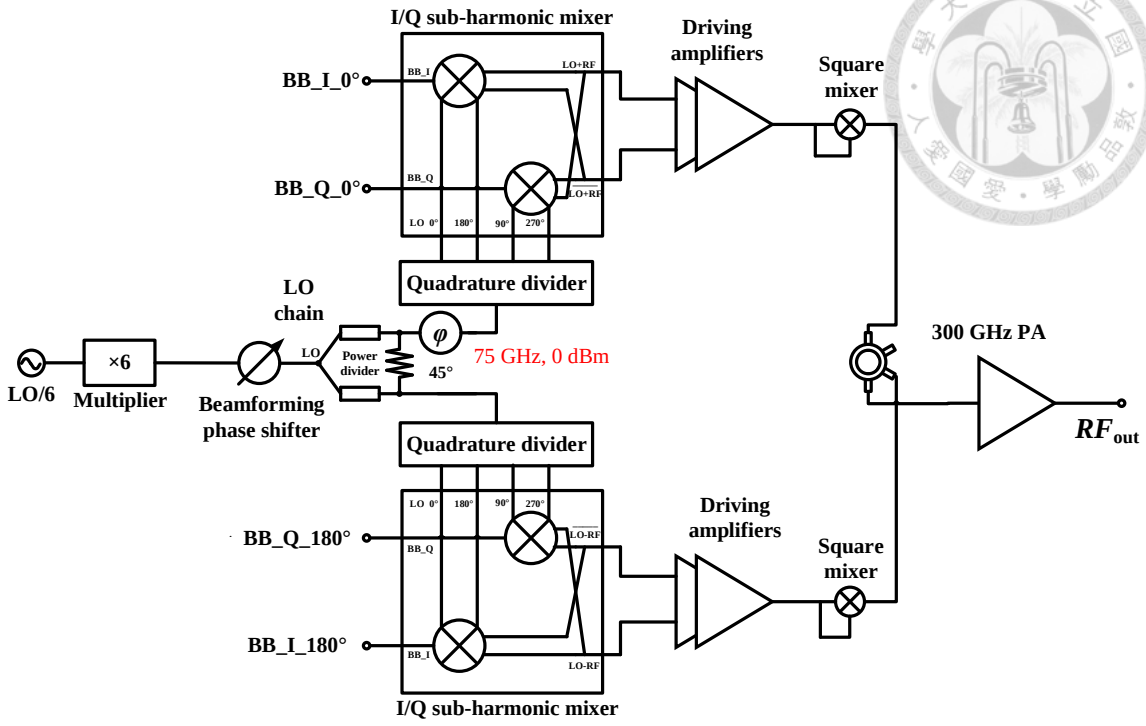

Fig. 2.1 Block diagram of 300-GHz transmitter system.

In this work, based on experimental results, the peak gain is 21.3 dB at 165 GHz, with 128 to 170 GHz bandwidth of a minimum 10.6 dB small signal gain and an output-referred 1-dB compression point of -7.4, -3.7, and -7.3 dBm at 140, 150, and 160 GHz, respectively. The total DC power consumption of this work is 39.3 mW, with the core area only 0.1 mm^2.

Chapter 2 will demonstrate the proposed D-band broadband driving amplifier for the 300 GHz phase-array transceiver. Chapter 2.2 introduces the design of the proposed amplifier, which is based on a three-stage cascode topology. Due to the poor gain performance of CMOS at the D-band, a gain-boosting technique is adopted. Adding a transmission line at the gate of the common gate transistor of the cascade can increase the gain performance. The compensated matching technique is also adopted while designing the inter-stage matching, which can broaden the bandwidth. Chapter 2.3 shows the

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measured results of the proposed amplifier. Chapter 2.4 discusses the unmatched results from simulations and measurements. Troubleshooting and device measurement results are also introduced in this section. At last, Chapter 2.5 summarizes this work.

Table 2.1 The design goals of the D-band driving amplifier in the 300 GHz transceiver system.

	Specification
Process	65-nm CMOS process
Frequency (GHz)	126.8-160
Gain (dB)	> 10
$\boldsymbol{OP_{1dB}}$ **(dBm)**	> -10 dBm
Chip area (mm^2)	As small as possible

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2.2 Design of D-band Driving Amplifier

2.2.1 DC Bias and Device Size Selection

The three key factors in designing an amplifier are gain performance, bandwidth performance, and stability. The bias point of the device and device size significantly determine these characteristics. Therefore, selecting the appropriate bias point and device size will be crucial at the outset of amplifier design.

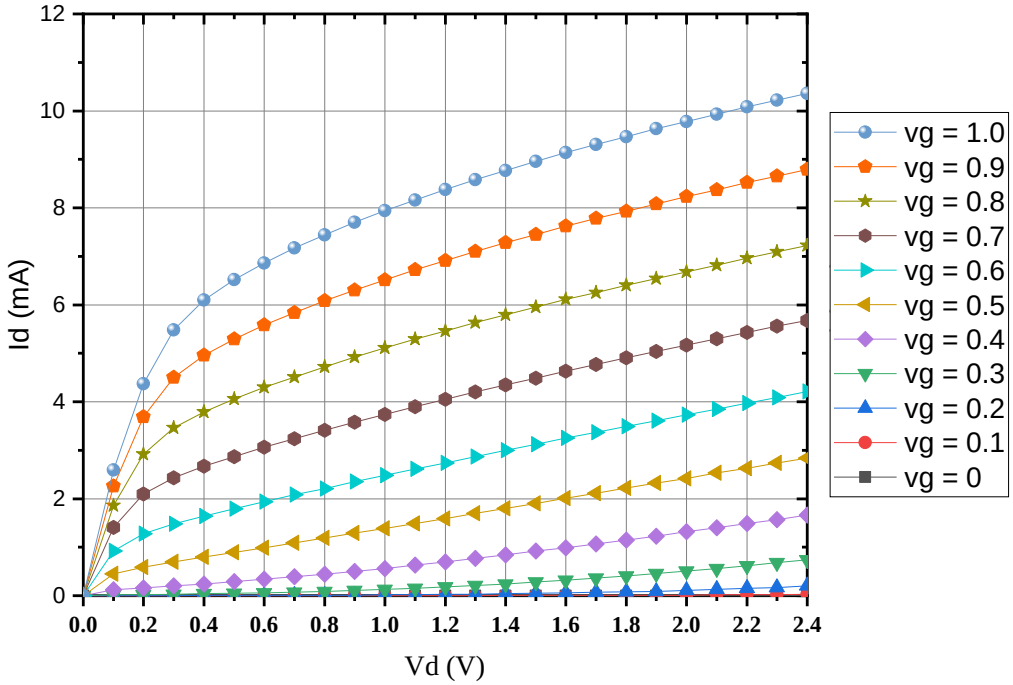

Fig. 2.2 DC-IV curve of the transistor size of 1 μm x 10-fingers.

The circuit design starts with device bias selection, the DC-IV curve of the 1 μm x 10-fingers device size demonstrated in Fig. 2.2. For the purpose of enough output power performance, the drain voltage (V_D) of the device is selected at 1.2 V. And, the transconductance (g_m) and drain current (I_D) versus different gate voltage (V_G) with the device size of 1 μm x 10-fingers and drain voltage of 1.2 V are depicted in Fig. 2.3 and

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Fig. 2.4. Based on simulation results, the peak transconductance (g_m) occurs at a gate voltage of 0.94 V. In the design, to achieve the highest gain performance due to the poor gain in the D-band, the gate voltage will be selected to 0.8 V, which is 98% of the gm peak, but only 72% of the DC power consumption.

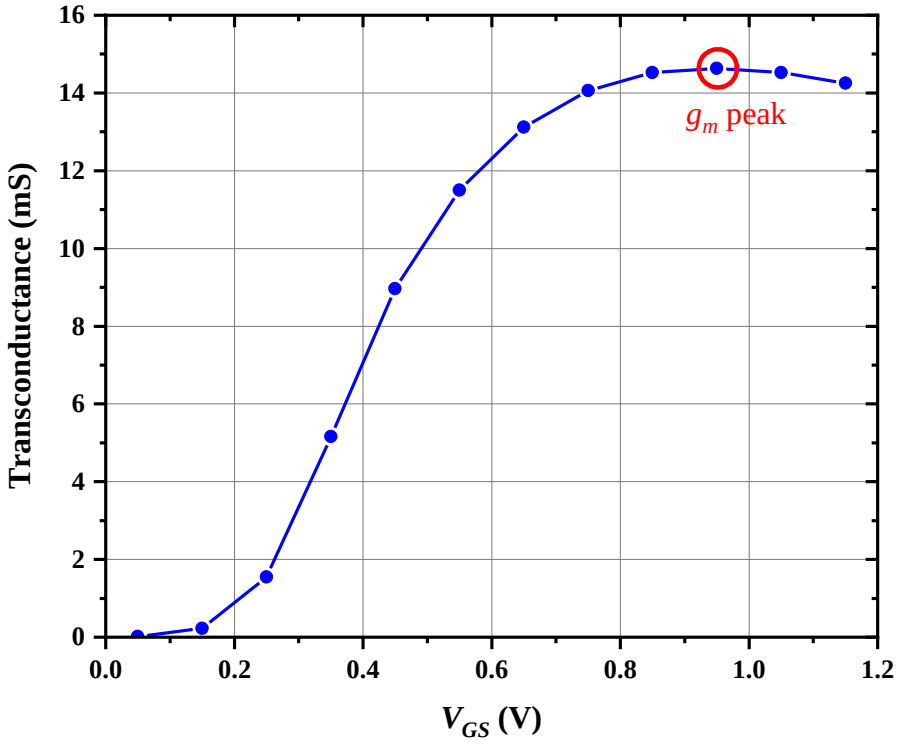

Fig. 2.3 Transconductance versus gate bias of the transistor size of 1 μm x 10-fingers.

Fig. 2.5, Fig. 2.6, Fig. 2.7, and Fig. 2.8 demonstrate the simulation results of the MSG/MAG and stability factor with different transistor sizes under the same bias condition of V_{GS} of 0.8 V and V_{DS} of 1.2 V. The results show that the smaller transistor size exhibits higher maximum gain, while the stability is compromised. Furthermore, smaller transistor device sizes often have higher impedance, which makes it challenging to match to 50 Ω impedance and results in higher matching loss. Table 2.2 summarizes the large signal simulation results at 140 GHz with different transistor sizes. It shows that the 1 μm x 10 fingers size has enough output power while having adequate gain

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performance; meanwhile, a moderate DC power consumption is also a critical concern. Table 2.3 summarizes the relationship between device size, stability factor, and gain performance. From the simulation results, the transistor size is chosen to be 1 μm x 10 fingers.

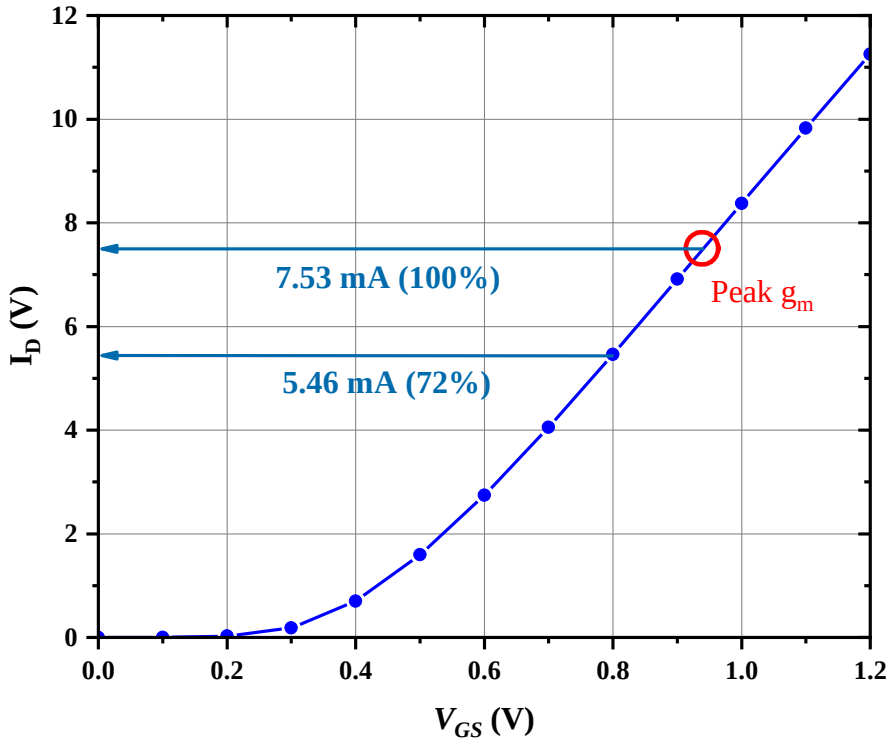

Fig. 2.4 Drain current versus gate bias of the transistor size of 1 μm x 10-fingers.

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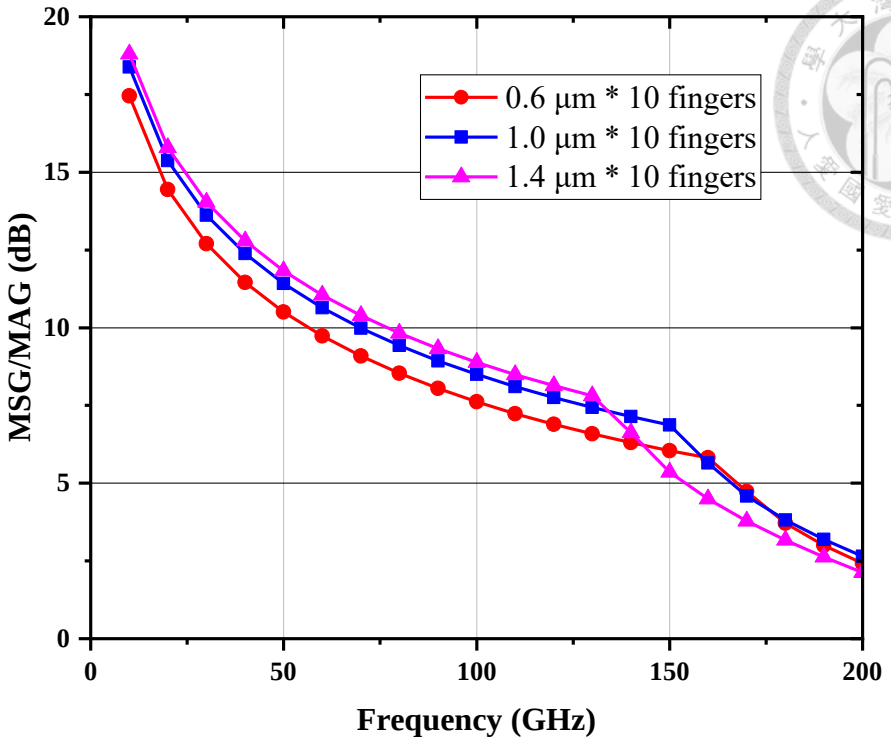

Fig. 2.5 MSG/MAG versus frequency with different gate widths under bias conditions of V_{GS} = 0.8 V, V_{DS} = 1.2 V.

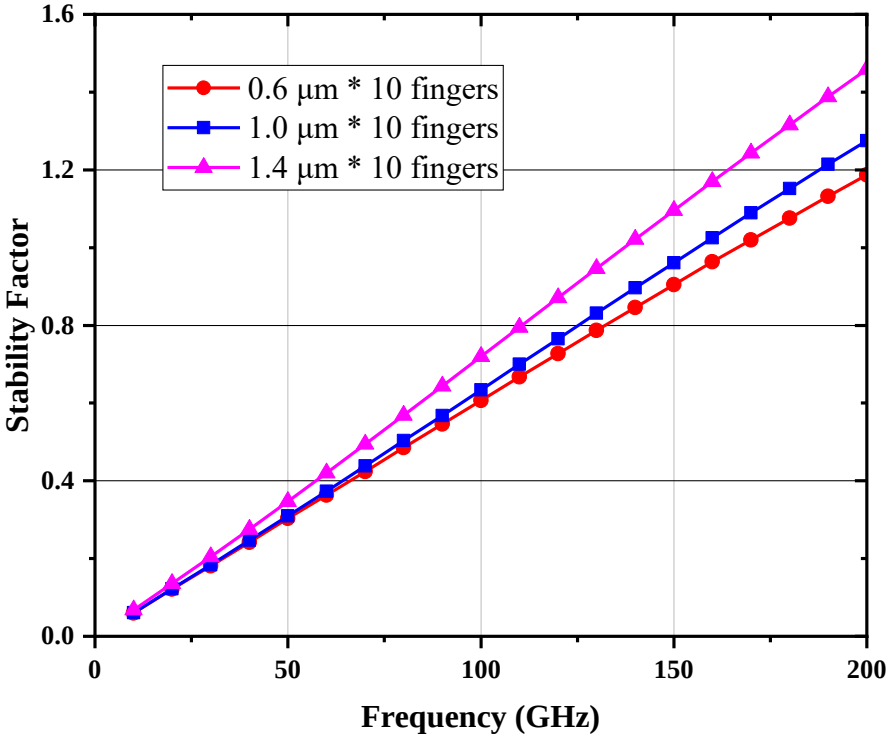

Fig. 2.6 Stability Factor versus frequency with different gate widths under bias conditions of V_{GS} = 0.8 V, V_{DS} = 1.2 V.

doi:10.6342/NTU202504602

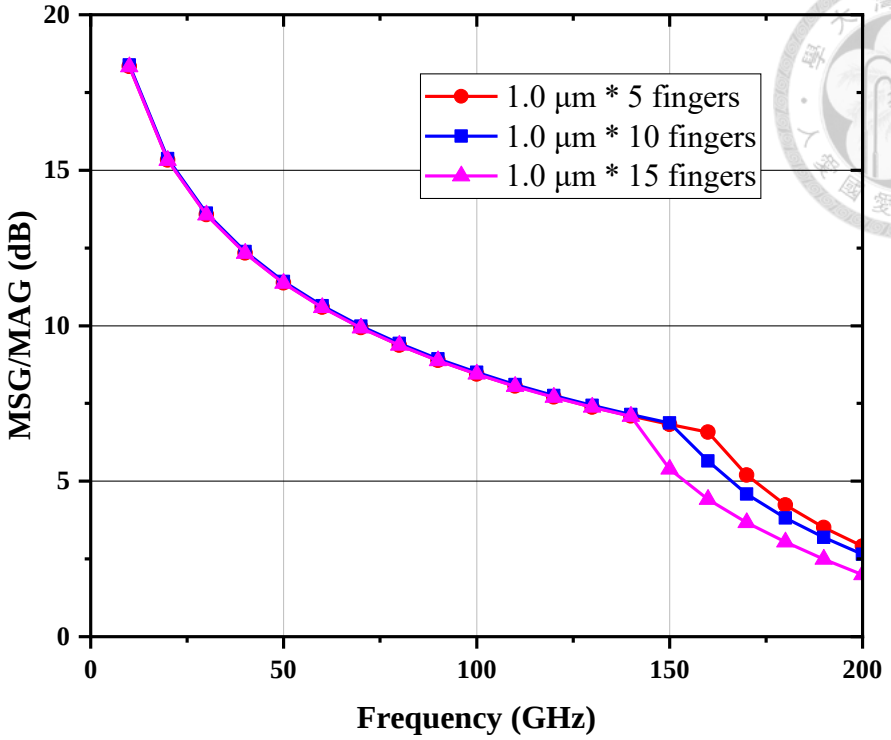

Fig. 2.7 MSG/MAG versus frequency with different numbers of fingers under bias conditions of V_{GS} = 0.8 V, V_{DS} = 1.2 V.

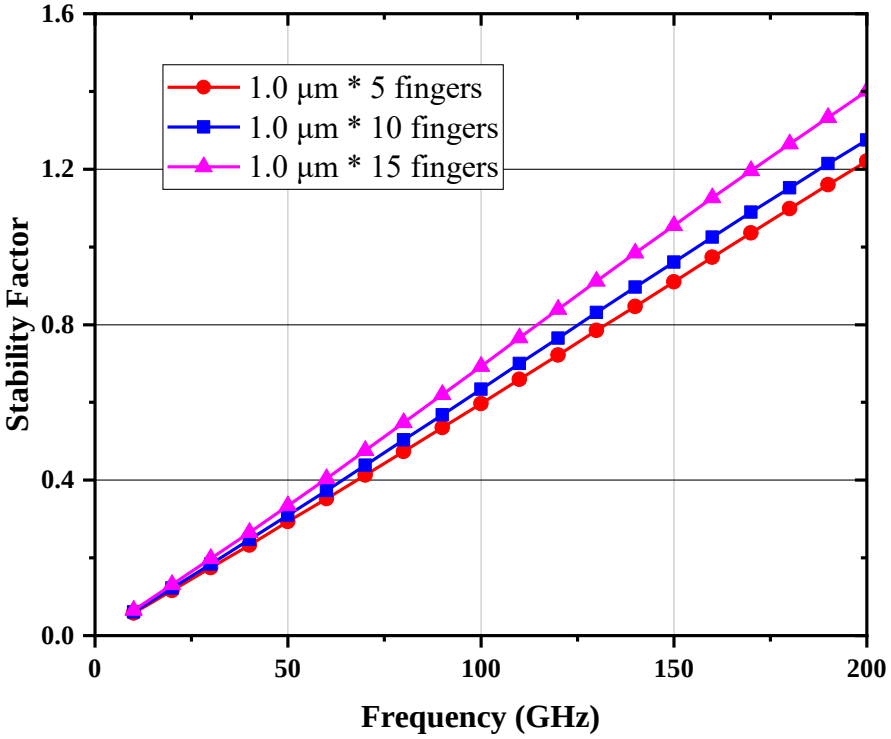

Fig. 2.8 Stability Factor versus frequency with different numbers of fingers under bias conditions of V_{GS} = 0.8 V, V_{DS} = 1.2 V.

doi:10.6342/NTU202504602

Table 2.2 The large signal simulation results with different transistor sizes.

Size	Gain (dB)	P_{sat} (dBm)	OP_{1dB} (dBm)	Z_{opt} (Ohm)	I_d (mA)
1 μm x 5 fingers	**5.3**	1.25	-0.4	113+j*166	2.76
1 μm x 10 fingers	**5.4**	4.3	2.5	58+j*80	5.46
1 μm x 15 fingers	**4.7**	5.7	4.1	39+j*57	8.07

Table 2.3 Trade-off study of the device size selection for D-band amplifier.

Device Size	MSG/MAG	Stability Factor	Power consumption
↑	↓	↑	↑
↓	↑	↓	↓

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2.2.2 Cascode Configuration Design

Fig. 2.9 shows the transistor size and bias condition of the common source (CS) and cascode configuration. Fig. 2.10 illustrates the simulated MSG/MAG of common source (CS) and cascode configuration under the condition shown in Fig. 2.9. Although the dc consumption of the cascode cell is twice that of the common source topology, the gain performance is also almost two times that of the common source configuration around the desired frequency band. Moreover, the output voltage swing of the cascode configuration is much higher than the common source structure, which can enhance output power performance to meet the design requirement of OP_{1dB}.

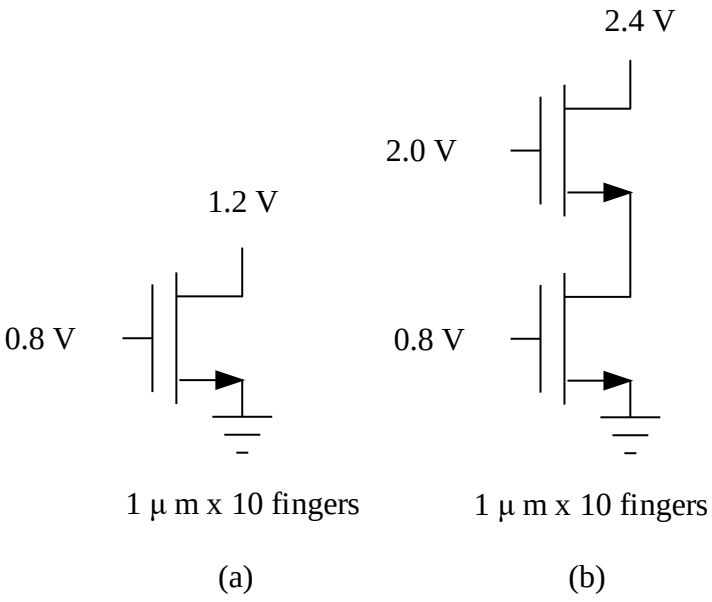

Fig. 2.9 The transistor size and bias condition of (a) the common source (CS) and (b) the cascode configuration.

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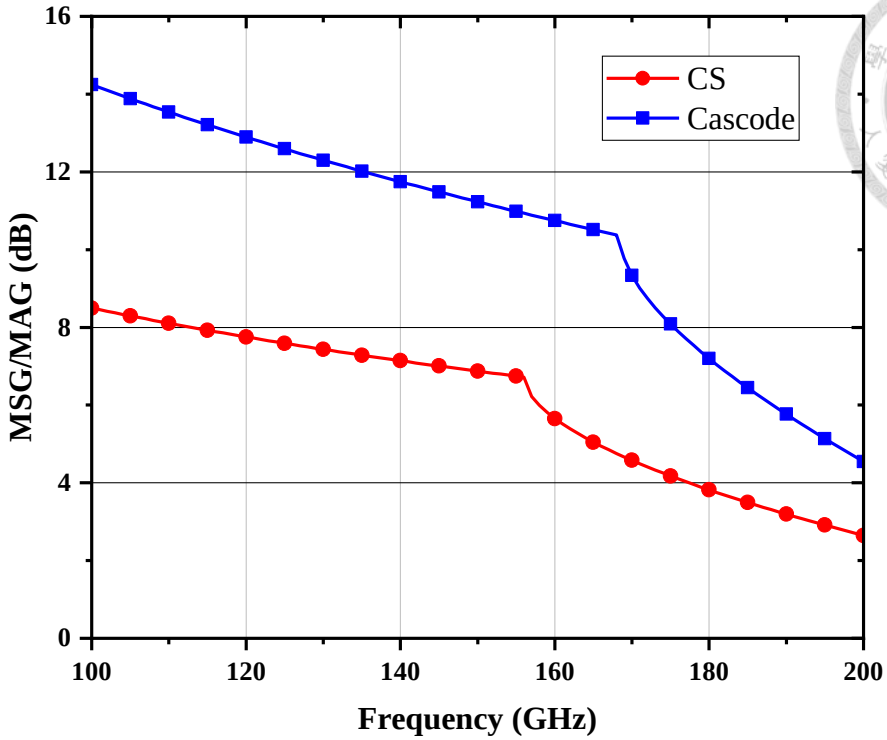

Fig. 2.10 MSG/MAG of common source (CS) and cascode configuration under the condition shown in Fig. 2.9.

2.2.3 Gain-Boosting Technique [20, 38-40]

By grounding the gate terminal of a common gate transistor in cascode topology can alleviate the Miller effect on gate-to-drain capacitance in the common source. This results in enhanced reverse isolation, improved circuit stability, and better gain and bandwidth performance in the cascode structure. However, when the transistor is operating in sub-terahertz, the gain of the cascode cell drops dramatically due to the limitation of carrier mobility and large device parasitic effects. By introducing a gate inductance in the common gate transistor shown in Fig. 2.11, positive feedback is formed to compensate for the gain degradation at elevated frequencies.

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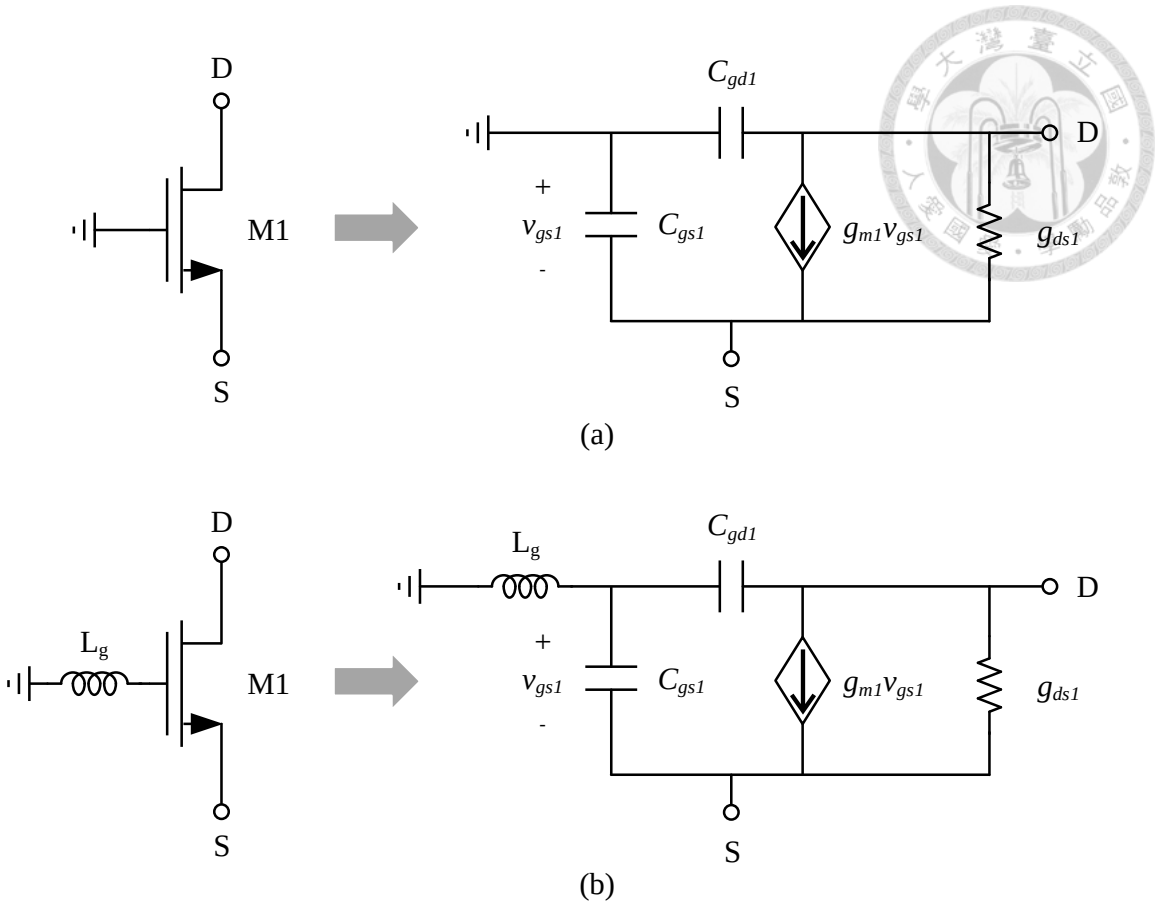

Fig. 2.11 The common gate transistor (a) without and (b) with the gate inductance.

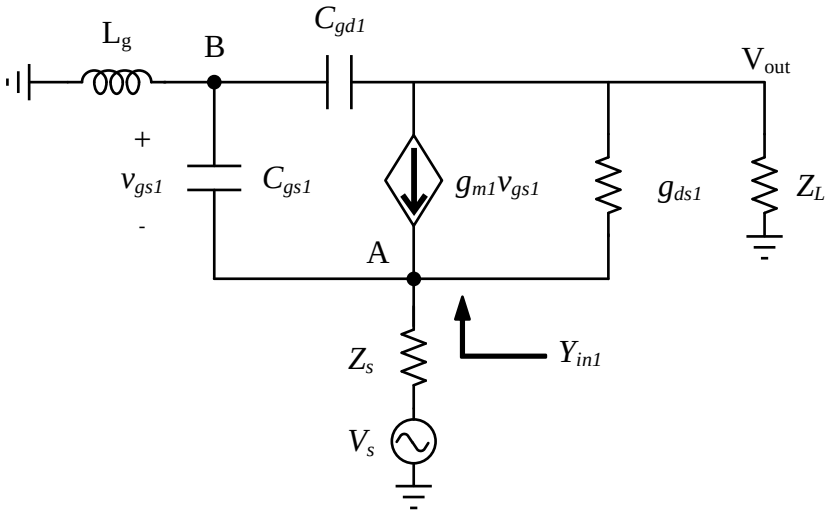

Fig. 2.12 Small-signal equivalent circuit of the common gate transistor with the gate inductance.

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To further study the effect caused by the gate inductance shown in Fig. 2.11(b), an equivalent circuit of the common gate stage along with gate inductance is shown in Fig. 2.12. Based on the small signal analysis, the voltages at nodes A and B can be presented by

$$v_A = \frac{1-(\omega_0/\omega_t)^2}{\left[1-(\omega_0/\omega_t)^2\right]+\left(g_{m1}+j\omega_0 C_{gs1}\right)Z_s} v_s \tag{2.1}$$

$$v_B = \frac{-(\omega_0/\omega_t)^2}{1-(\omega_0/\omega_t)^2} v_A \tag{2.2}$$

where ω_0 is the operating frequency and ω_t is given by

$$\omega_t = \frac{1}{\sqrt{L_g C_{gs1}}} \tag{2.3}$$

Since the gate-to-drain capacitance C_{gd1} and the channel conductance g_{ds1} are relatively small, we can neglect these factors to simplify the analysis. By considering the equation (2.1) and (2.2), the voltage difference across gate-to-source capacitance can be derived as

$$v_{gs1} = \frac{-1}{\left[1-(\omega_0/\omega_t)^2\right]+\left(g_{m1}+j\omega_0 C_{gs1}\right)Z_s} v_s \tag{2.4}$$

From equation (2.2), when the angular frequency (ω_0) is smaller than the threshold frequency (ω_t), the voltages of nodes A and B are out of phase. Therefore, the amplitude of v_{gs1} increases, resulting in enhanced effective transconductance and boosting the gain of the cascode stage.

Due to the self-resonant frequency limitation of inductance, the microstrip line is more favorable for implementing in the mm-wave design. Fig. 2.13 shows the simulated V_{gs} waveform in time domain simulation with (V_{gs}') and without (V_{gs}) the gate inductance

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of the common gate transistor. It is obvious that the amplitude of V_{gs} increases when a transmission line is added at the gate of the common gate transistor. Fig. 2.14 demonstrates the simulated MSG/MAG of the cascode structure versus frequency with different lengths of gate inductance. The simulation condition is based on the topology and bias shown in Fig. 2.9(b), and adding a different length of transmission line at the gate terminal of the common gate transistor of the cascode structure. Adding a transmission line can push the turning point of the cascode stage toward a higher frequency and increase the MSG at high frequency. Fig. 2.15 illustrates the simulated stability factor of the cascode structure versus frequency with different lengths of gate inductance. As the length of the gate transmission line increases, the stability factor worsens. Therefore, it is cautious to choose the proper length of the gate transmission line to prevent the circuit from being instability.

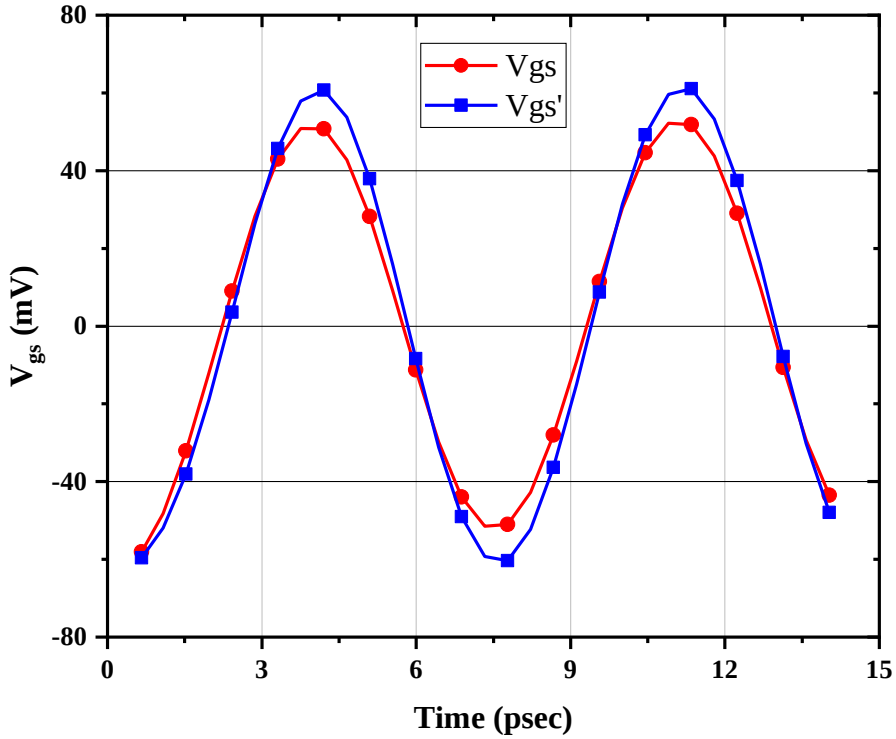

Fig. 2.13 The V_{gs} waveform in time domain simulation with (V_{gs}') and without (V_{gs}) the gate inductance of the common gate transistor.

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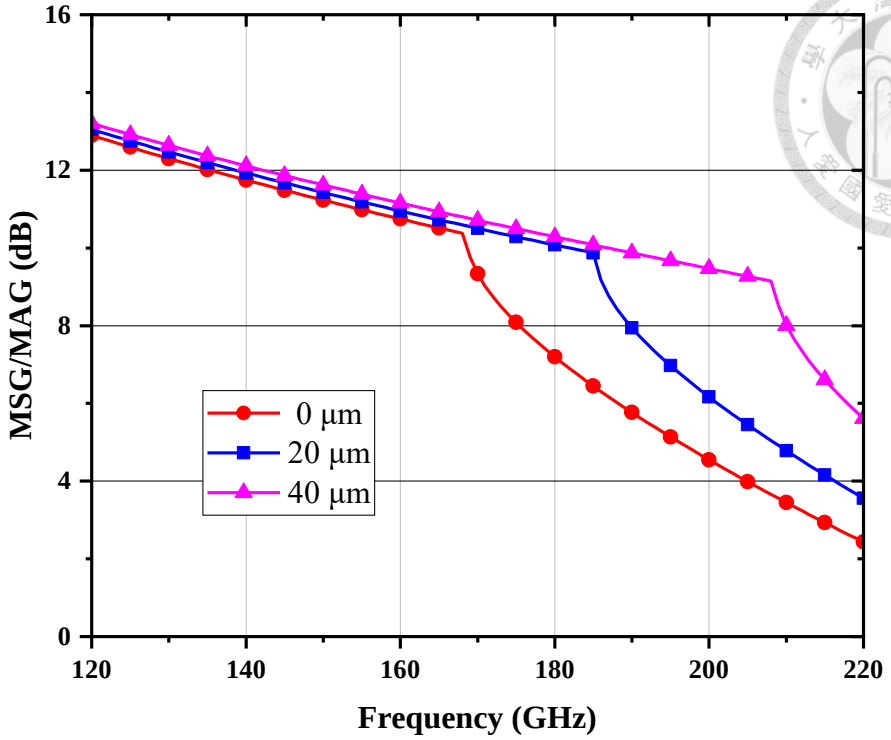

Fig. 2.14 Simulated MSG/MAG of cascode structure versus frequency with different lengths of gate inductance.

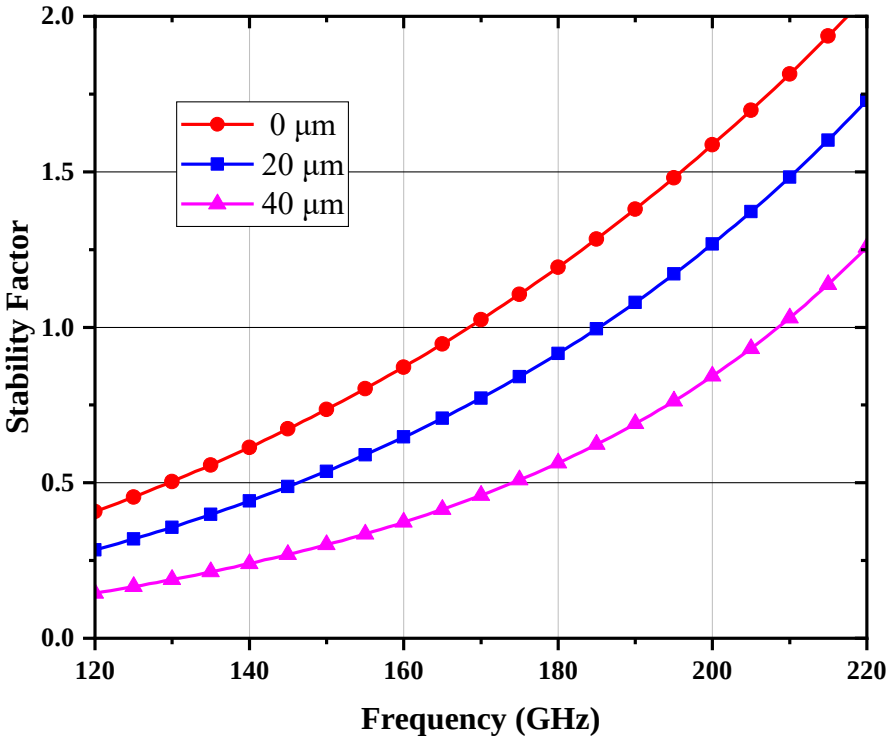

Fig. 2.15 Simulated stability factor of cascode structure versus frequency with different lengths of gate inductance.

doi:10.6342/NTU202504602

From the previous simulation, it is obvious that the gate inductance can significantly improve the MSG/MAG of the cascode stage at the expense of potentially unstable causes by positive feedback. Based on the small-signal equivalent model shown in Fig. 2.12, the input admittance Y_{in1} can expressed as

$$Y_{in1} = \frac{g_{m1}}{1-(\omega_0/\omega_t)^2} + \frac{j\omega_0 C_{gs1}}{1-(\omega_0/\omega_t)^2} \tag{2.5}$$

If the value of common gate inductance L is too large, the ω_t will be smaller than ω_0, causing the input admittance Y_{in1} to have a negative conductance, and may cause the circuit oscillation. As a result, the value of the common gate inductance should be carefully chosen to avoid circuit instability, that is, under the condition of

$$\omega_0 < \omega_t \tag{2.6}$$

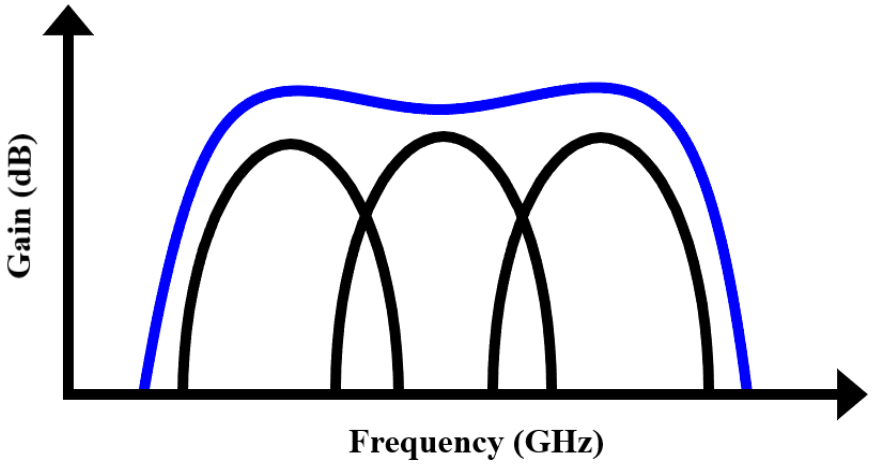

Fig. 2.16 Schematic diagram of compensated matching.

By adding different lengths of gain-boosting transmission and matching at different frequencies at each stage, the proposed amplifier can exhibit a broad band performance by compensated matching concept, as shown in Fig. 2.16.

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2.2.4 Circuit Architecture and Post-layout Simulation Results

The proposed driving amplifier is implemented in TSMC 65-nm CMOS process with ultra-thick metal (UTM), eight metal layers (M_1 to M_8), and a metal-insulator-metal (MIM) capacitor. Advanced Design Software (ADS) and Sonnet Software are used throughout the design for circuit and post-layout simulation. Fig. 2.17 depicts a schematic of the proposed D-band driving amplifier based on a three-stage cascode topology. To further enhance the gain performance, the gain-boosting technique (red, thick transmission line) is adopted in the design. Furthermore, for the purpose of broadening the bandwidth, the compensated matching technique is adopted in the inter-stage matching networks [2][9]. By designing the two inter-stage matching networks that match at different frequencies, broadband performance is achieved. LC components are used for input, inter-stage, and output matching networks. The microstrip line is more favorable than the inductor to implement in the mm-wave design due to the self-resonant frequency limitation of inductance. Bypass capacitors are implemented as MIM capacitors, while DC blocks involved in matching networks are realized using metal-oxide-metal capacitors, which are interdigital of metal 5 to metal 9. Fig. 2.18 shows the layout of the proposed driving amplifier with a total area of 0.37 mm^2 (0.9 mm × 0.42 mm) with all pads and only 0.1 mm^2 (0.725 mm × 0.15 mm) core area. The total DC power consumption of the proposed amplifier is 39.3 mW.

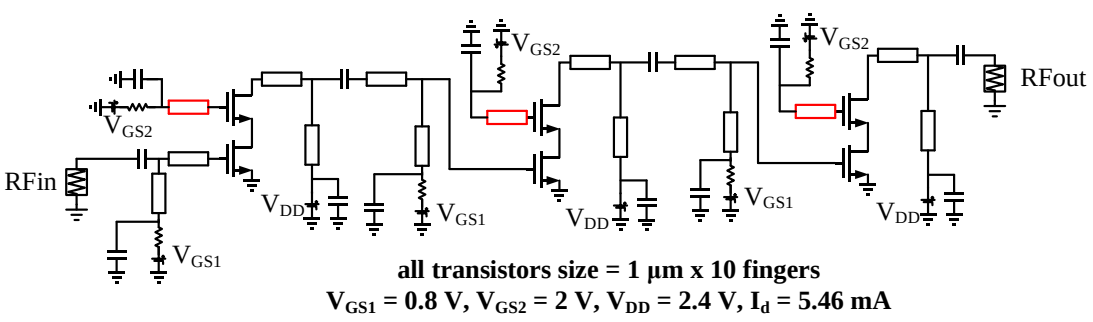

Fig. 2.17 Complete schematic of the proposed driving amplifier.

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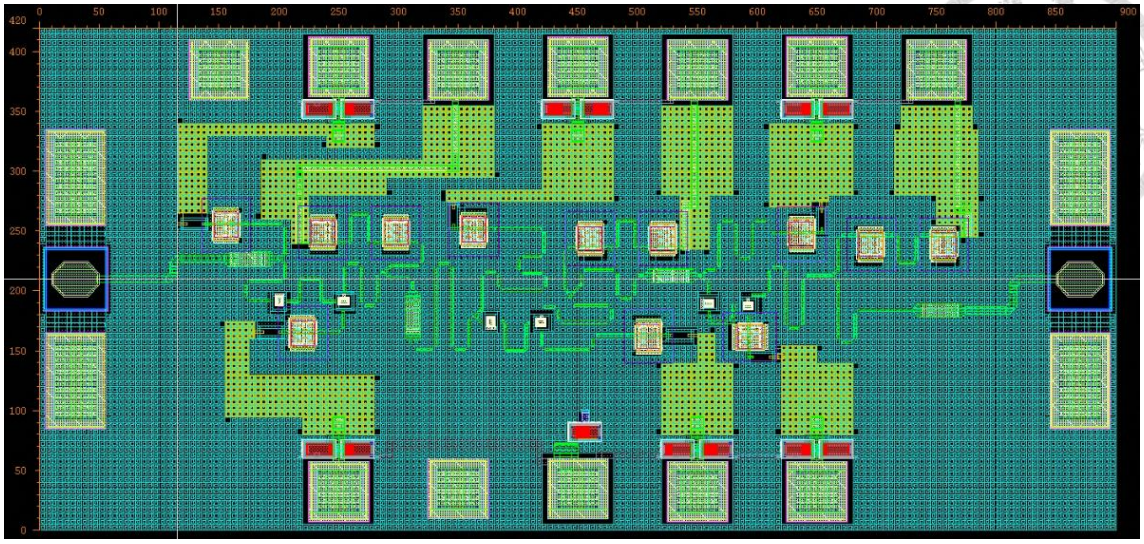

Fig. 2.18 Layout of the proposed D-band driving amplifier.

Fig. 2.19 illustrates the simulated s-parameter of the proposed driving amplifier; based on simulation results, the peak gain is 17.8 dB, a 3-dB bandwidth of 124 to 138 GHz, and the bandwidth of gain exceeding 10 dB is 123 to 154 GHz. Fig. 2.20, Fig. 2.21, and Fig. 2.22 demonstrate the simulated output 1-dB compression point (OP_{1dB}) power levels and power gain performance at 130, 140, and 150 GHz. The OP_{1dB} achieves -1.6, -2.7, and -5.2 dBm at 130, 140, and 150 GHz, respectively.

It is essential to check the stability of the proposed driving amplifier to avoid oscillation. In this work, two methods were introduced. First of all, if the Rollett stability factor (K) is greater than one, representing the two-port network is unconditionally stable. Fig. 2.23 depicts the overall simulated stability factor of the proposed amplifier under different corner conditions and shows that it is greater than one at all frequencies. The K factor for stability is adequate for a single-stage amplifier. However, it is insufficient for a multi-stage amplifier, such as in the case of stages 1 and 2. Stages 1 and 2 can still oscillate with each other, and the K factor does not account for internal oscillations that may occur between stages. Therefore, stability circles are required for a more in-depth

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analysis. We need to ensure that the load stability circle at the front end does not intersect any impedance that may be seen at the rear end. Fig. 2.24 demonstrates the inter-stage stability circle between stage 1 and stage 2; the simulation results show no overlap between the mapping circles, meaning this inter-stage is stable. Fig. 2.25(a) demonstrates the inter-stage stability circle between stage 2 and stage 3. However, this result shows an overlap between the mapping circles. Therefore, we need to further examine the situation at different frequencies. Fig. 2.25(b), (c), and (d) show no overlap between mapping circles after dividing frequency in a smaller range, which means that the crossovers occur at different frequencies, and there is no stability issue in this inter-stage. Fig. 2.26 shows the simulation results under different device corners.

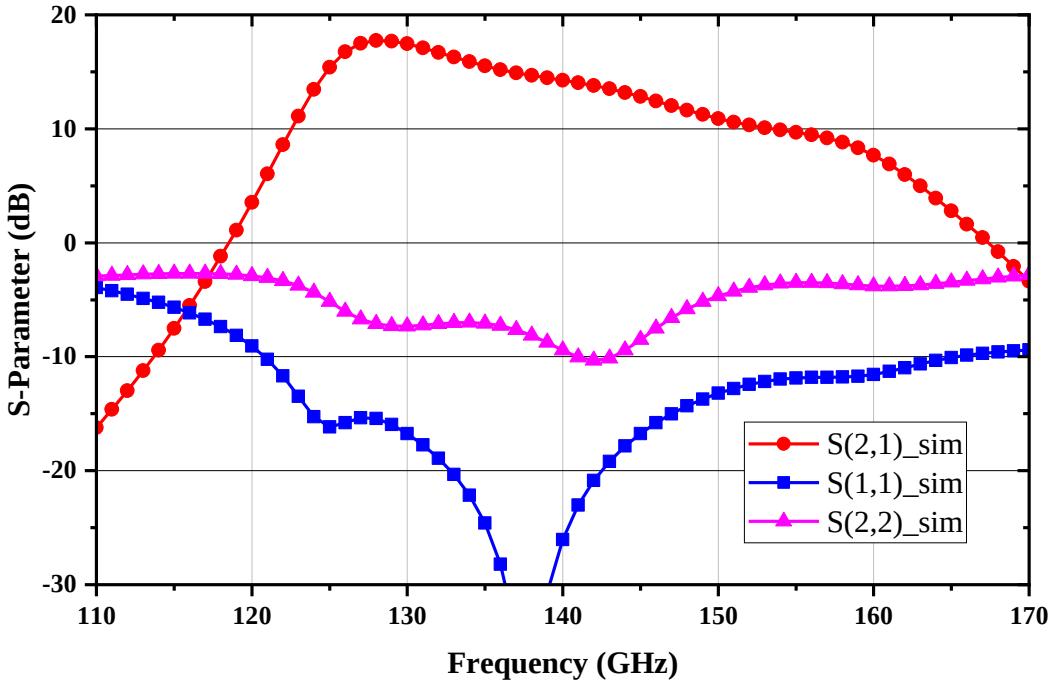

Fig. 2.19 Simulated S-parameter of the proposed D-band driving amplifier.

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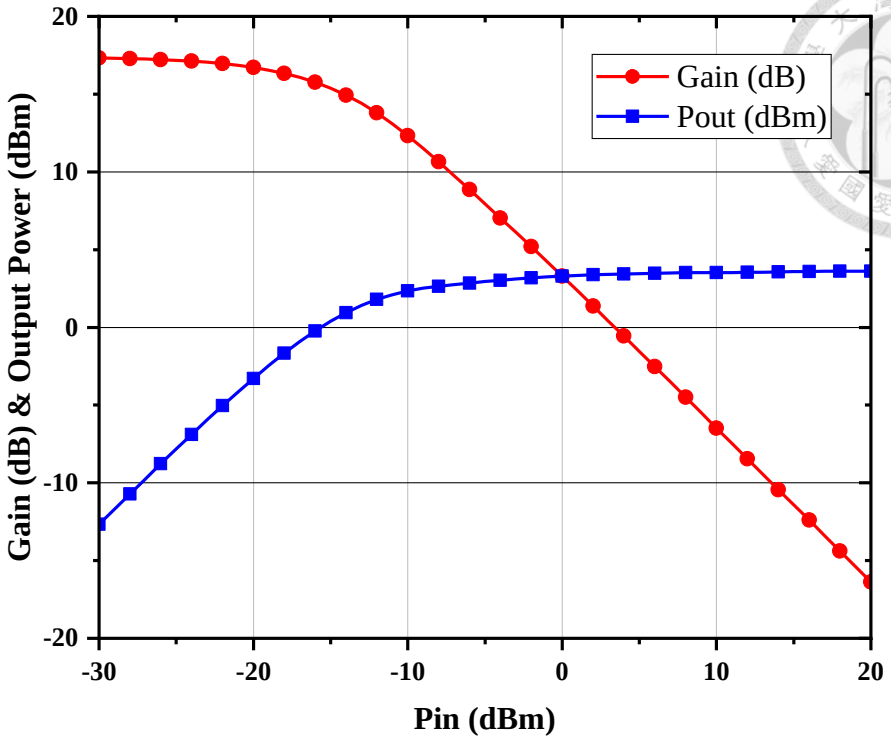

Fig. 2.20 Simulated large-signal performance of 130 GHz.

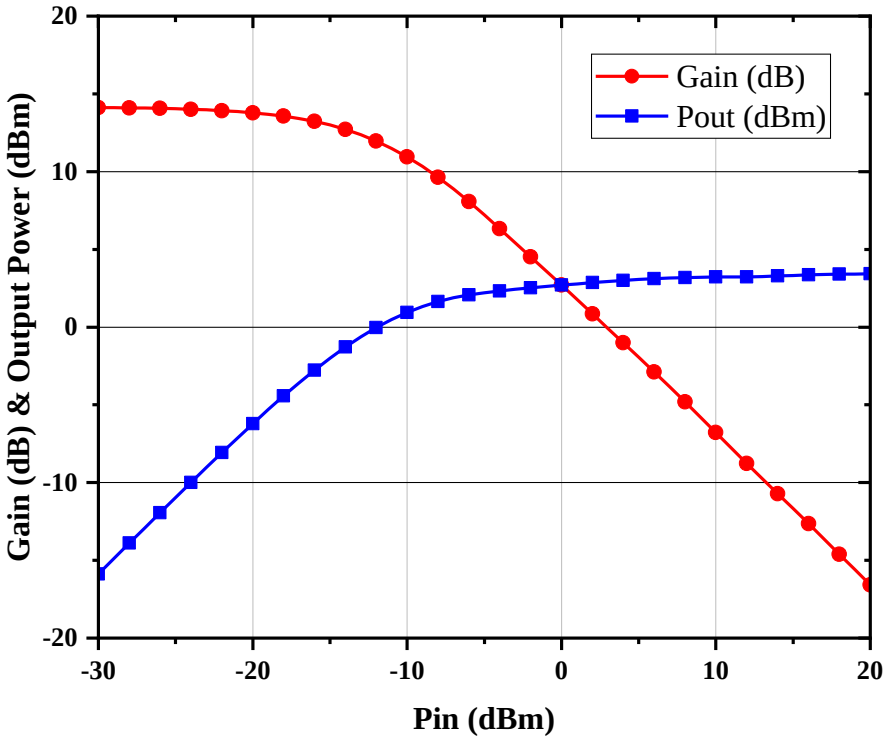

Fig. 2.21 Simulated large-signal performance of 140 GHz.

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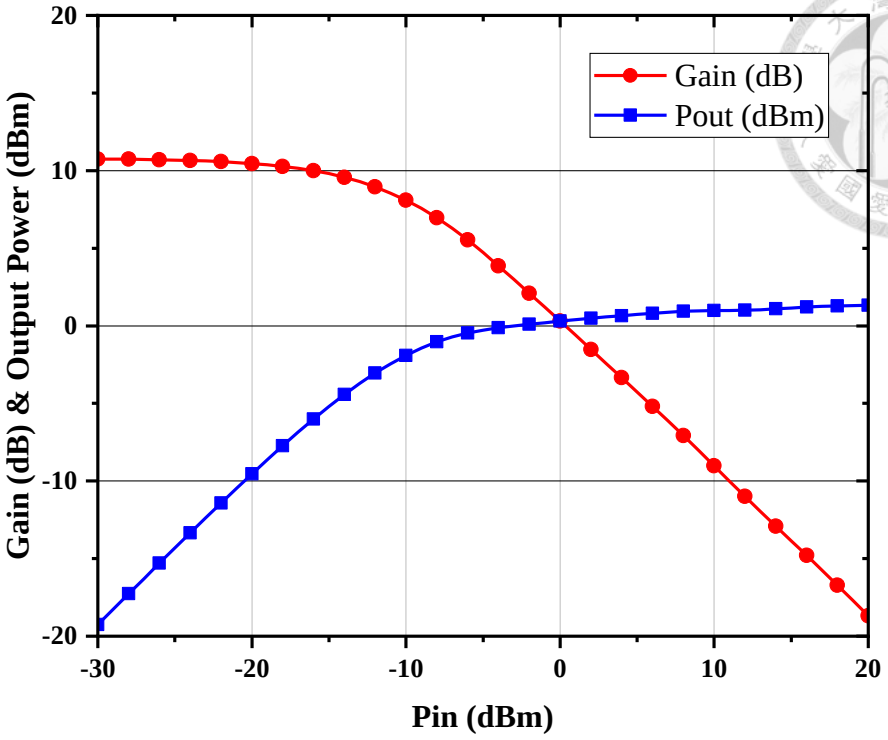

Fig. 2.22 Simulated large-signal performance of 150 GHz.

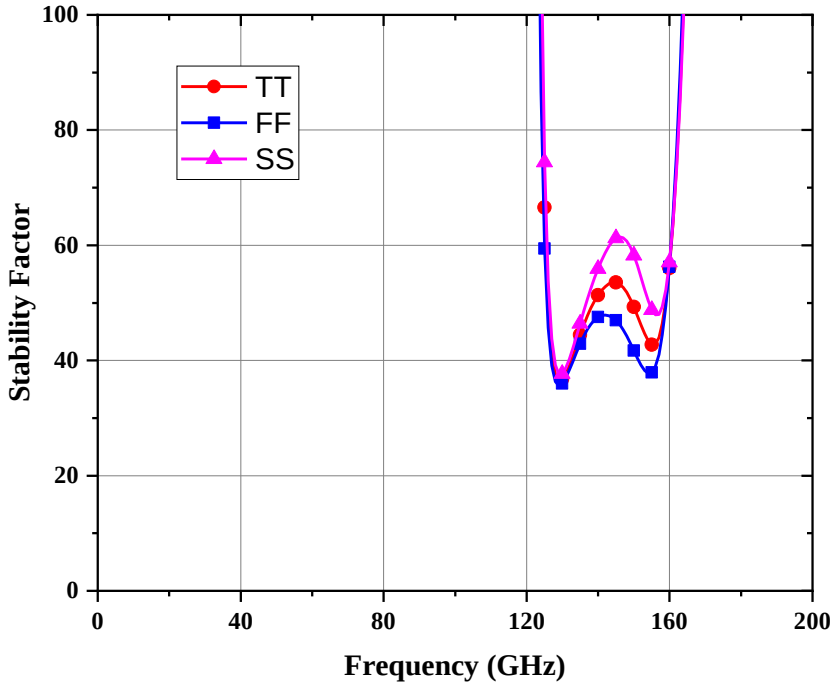

Fig. 2.23 Simulated stability factor of the proposed driving amplifier.

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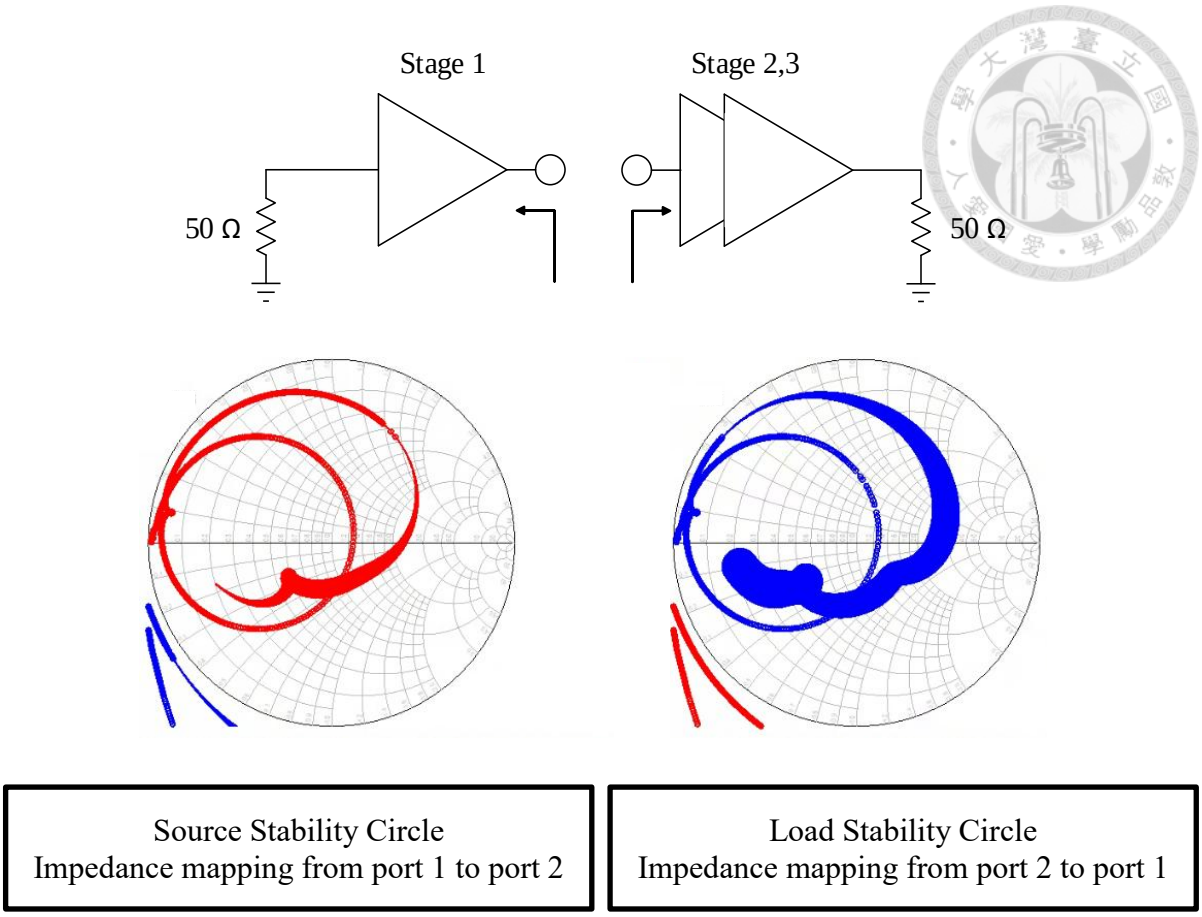
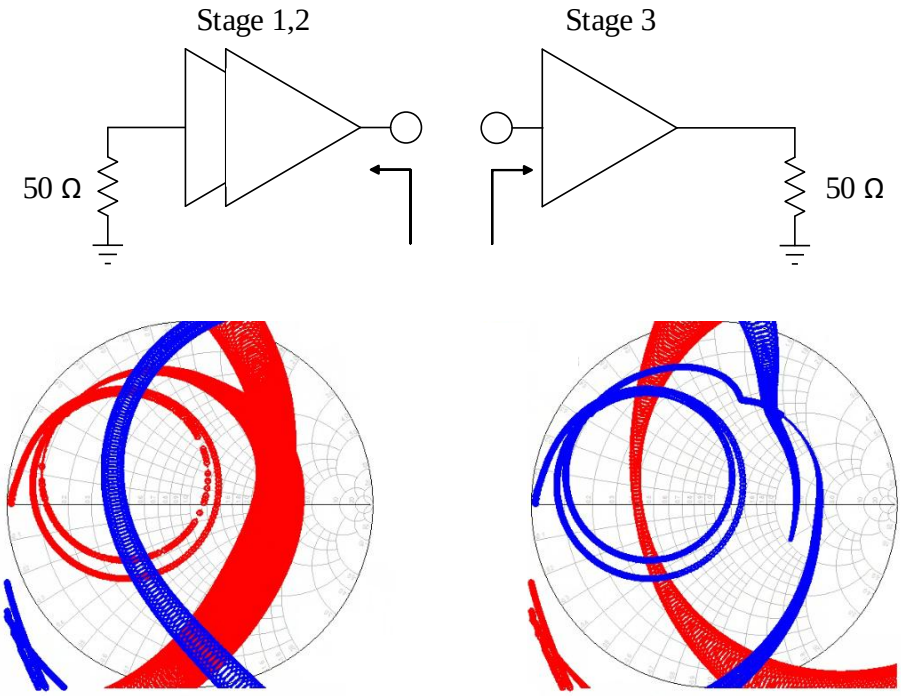


Fig. 2.24 Simulated inter-stage stability mapping circle of stages 1&2.



(a) 0.1~170 GHz

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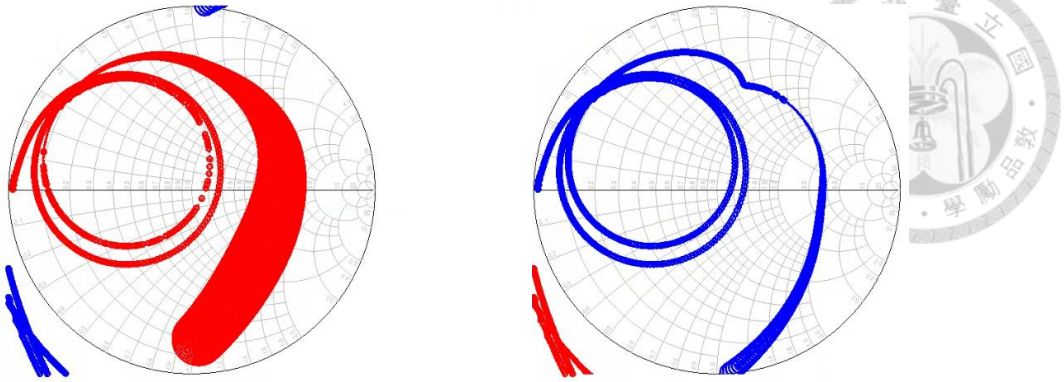
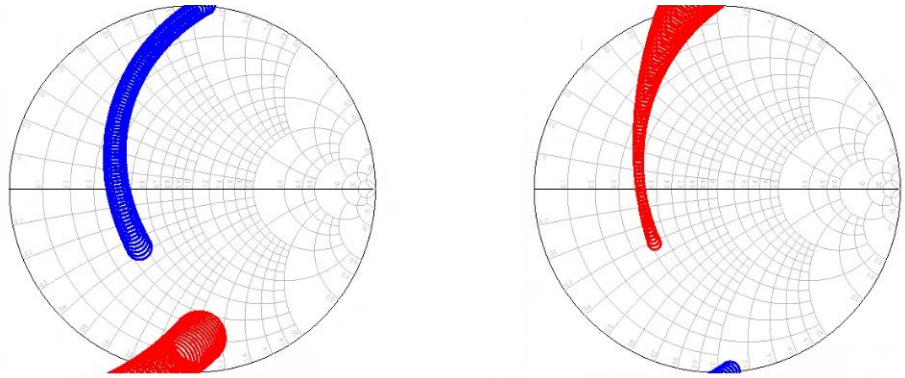
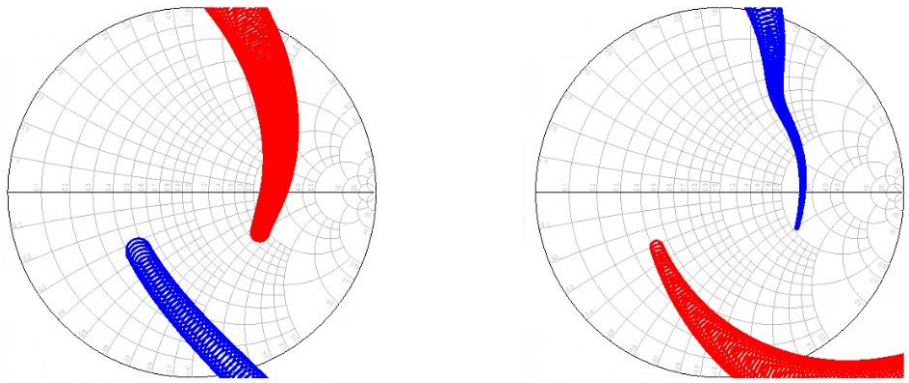


(b) 0.1 ~ 140 GHz



(c) 140 ~ 148 GHz



(d) 148 ~ 170 GHz

Source Stability Circle Impedance mapping from port 1 to port 2	Load Stability Circle Impedance mapping from port 2 to port 1

Fig. 2.25 Simulated inter-stage stability mapping circle of stages 2&3.

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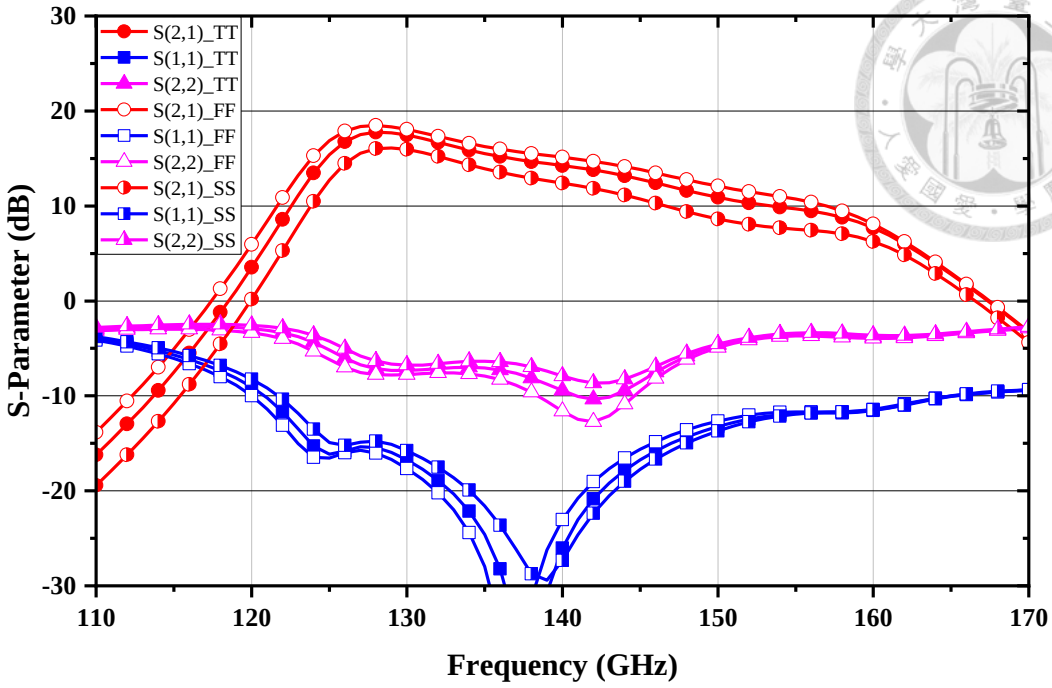

Fig. 2.26 Simulated S-parameter of the proposed driving amplifier under different device corners.

2.3 Measurement Results

The proposed D-band driving amplifier is fabricated in a 65-nm CMOS process. Fig. 2.27 shows the chip micrograph of the proposed work, the total area with pads is 0.37 mm^2 (0.9 mm × 0.42mm), and the core area of the proposed amplifier is 0.1 mm^2 (0.725 mm × 0.15 mm). The S-parameters of the proposed broadband amplifier are measured from 110 GHz to 170 GHz using an Agilent E8361C VNA with V06VNA2-TR frequency extenders. All measurement results were performed by on-wafer probing using GSG RF probes, and a bonding wire was used for DC feeding.

Fig. 2.28 shows the simulation and measurement S-parameters of the proposed driving amplifier. The measured peak gain is 21.3 dB at 165 GHz, and the small-signal gain is higher than 10 dB from 128 to 170 GHz. It is evident that the measured small-signal gain shifted about 10 GHz toward the higher frequency band and increased at 155 to 170 GHz. To investigate this unpredictable phenomenon further, Section 2.4 will

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provide a deeper discussion and address the problem.

The output power of the proposed amplifier is measured by a signal generator (E8257D), a frequency multiplier, WR-10 waveguides, and a power meter (PM5B). Fig. 2.29, Fig. 2.30, and Fig. 2.31 illustrate the measured and simulated large-signal performance, which includes power gain and output power at 140, 150, and 160 GHz. Since there are variations in small-signal gain performance among the desired frequency bands, the measured and simulated OP_{1dB} also exhibit significant differences. At 140 GHz, the measured and simulated power gains are 13.9 and 14.2 dB, respectively, and the OP_{1dB} values are -7.4 and -2.7 dBm. At 150 GHz, the measured and simulated power gains are 10.7 and 10.9 dB, respectively, and the OP_{1dB} values are -3.7 and -5.2 dBm. At 160 GHz, the measured and simulated power gain is 15 and 7.6 dB, and the OP_{1dB} is -7.3 and -7.4 dBm.

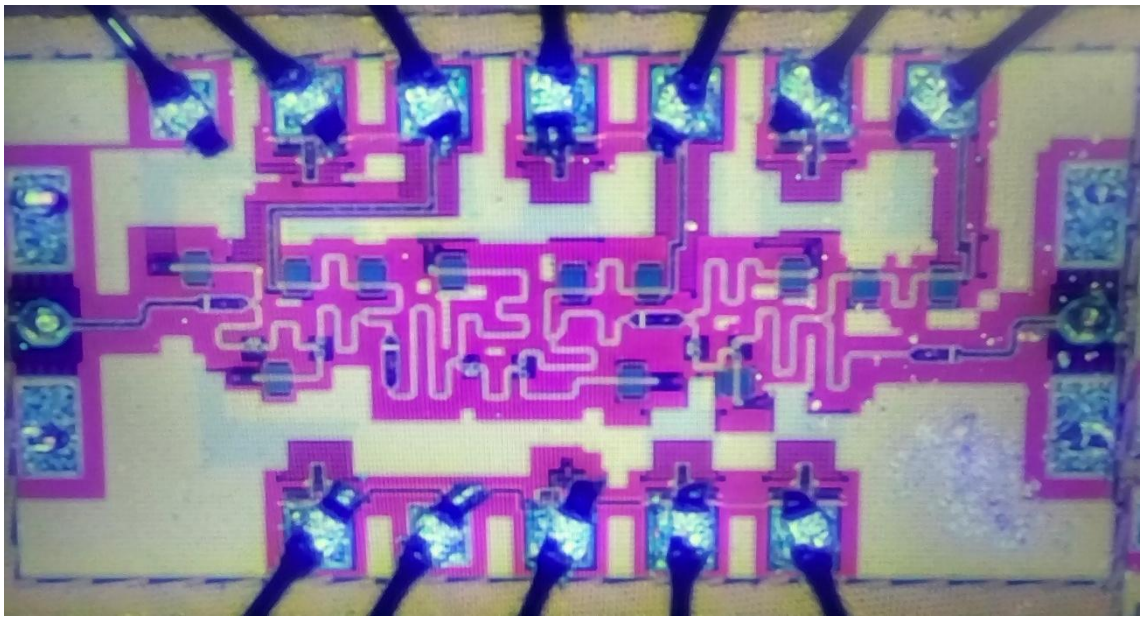

Fig. 2.27 The chip micrograph of the proposed driving amplifier.

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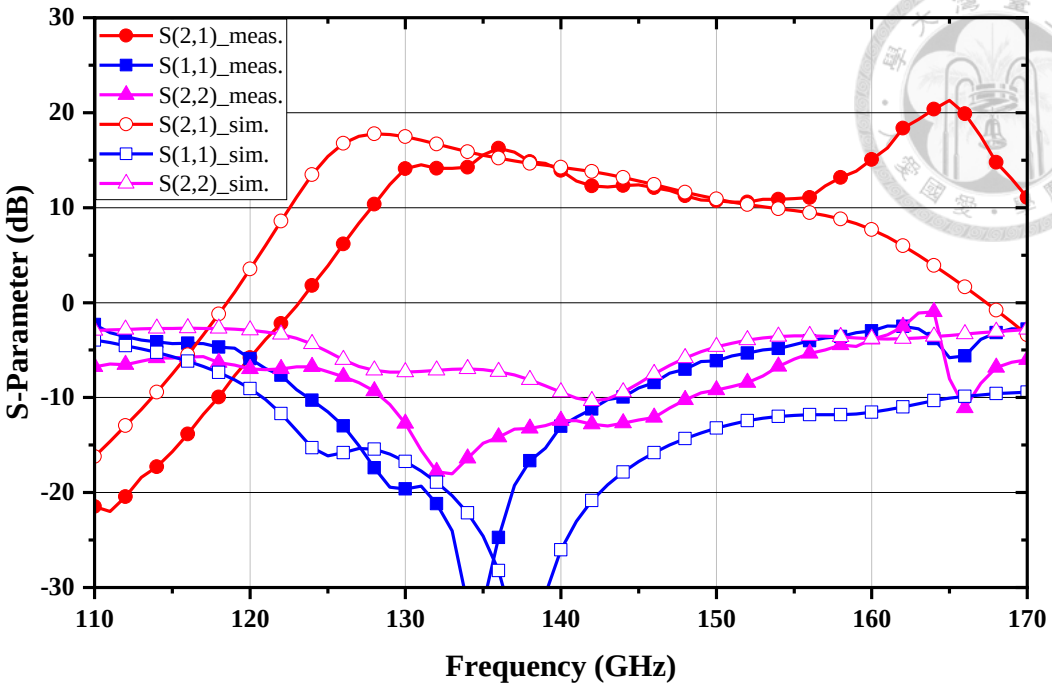

Fig. 2.28 The measurement and simulation S-parameter of the proposed driving amplifier.

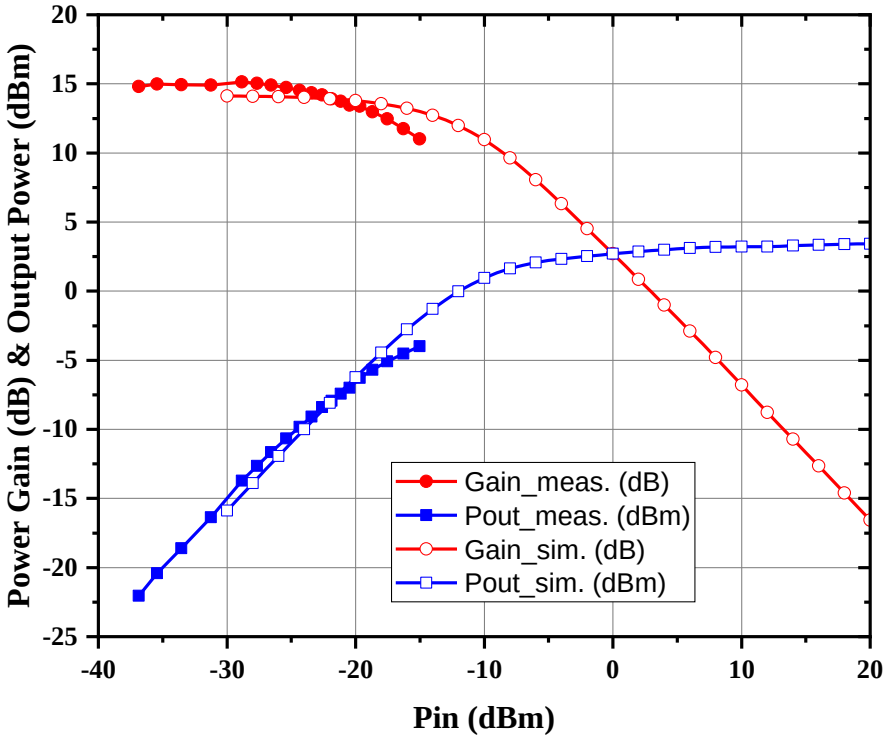

Fig. 2.29 The measured power gain and output power at 140 GHz.

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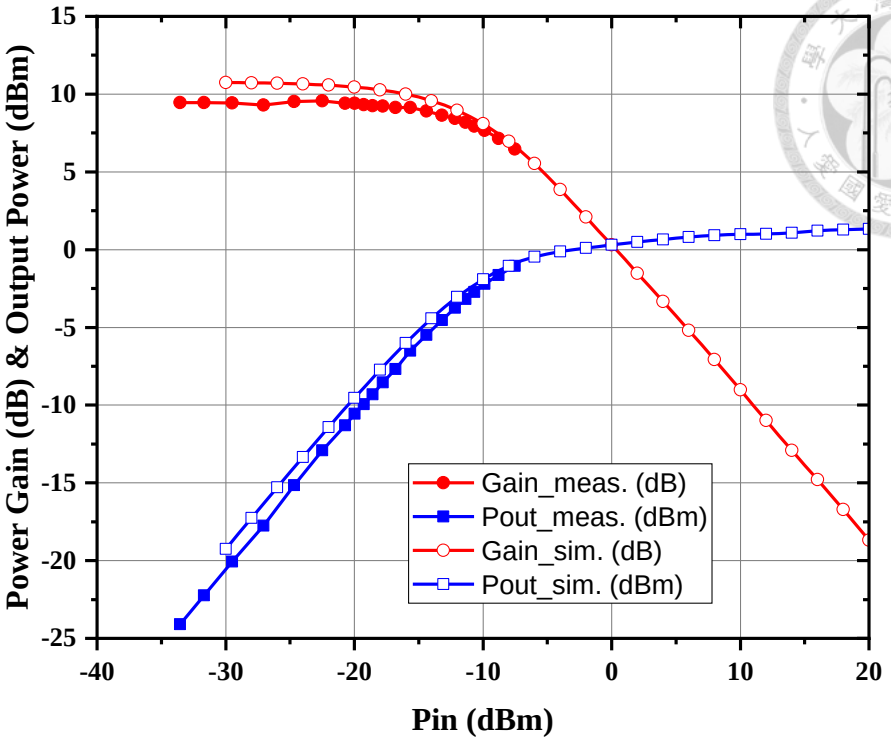

Fig. 2.30 The measured power gain and output power at 150 GHz.

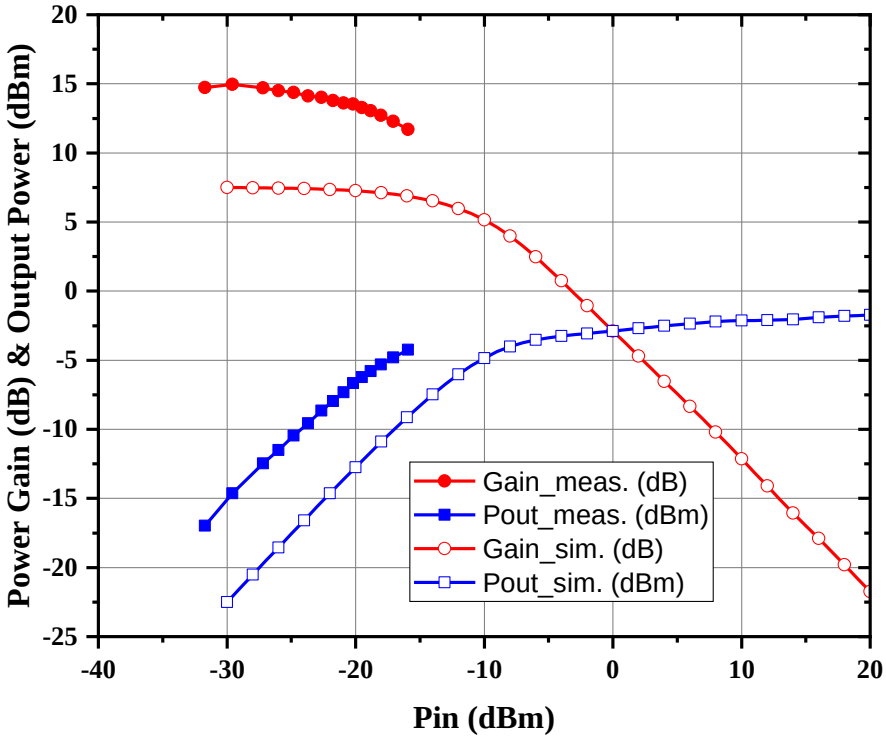

Fig. 2.31 The measured power gain and output power at 160 GHz.

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2.4 Troubleshooting and Discussion

2.4.1 EM Simulation Setup

The skin effect is a phenomenon where high-frequency alternating current (AC) tends to flow near the surface of a conductor rather than be uniformly distributed across its cross-section. This effect becomes more pronounced as frequency increases, leading to increased effective resistance and power loss. The formula for skin depth is shown as follows [41]

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \tag{2.7}$$

Where ρ is resistive of the conductor (Ω/m), ω = 2πf is the angular frequency (rad/s), and $\mu = \mu_0\mu_r$ is permeability (H/m). In the case of the metal material of copper at 140 GHz, the skin depth is less than 0.2 μm, meaning most current flows within a very thin surface layer. As a result, the mesh setting in electromagnetic (EM) simulation is very important. In Sonnet software, two key settings influence the mesh fineness: the number of metal sheets and the cell sizes.

When using thick metal, the structure is approximated by two or more infinitely thin sheets of metal. The number of sheets (NoS) defines the number of cross-sections used to simulate the thick metal. For the typical two-sheet model, one sheet represents the top surface of the structure, and a second sheet represents the bottom surface of the structure. Vias are placed automatically around the perimeter to allow current to flow between the sheets. Increasing the number of sheets adds more layers of infinitely thin metal between the top and bottom metal sheets. Fig. 2.32 shows the simulation result of the insertion loss for a 275 μm transmission line (quarter wavelength of 140 GHz under this process) and a width of 2 μm, under different sheet setups. The results reveal that two-sheet and four-

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sheet setups significantly differ from the eight-sheet and sixteen-sheet setups. Fig. 2.33 shows the simulation result of the phase of the length of a 275 μm transmission line (quarter wavelength of 140 GHz under this process) and a width of 2 μm under different numbers of sheet setups. Also, two-sheet and four-sheet setups differ from those divided into more sheets. As a result, we recognized that the EM simulation should be carried out at least under the eight-sheet setup at this frequency. Of course, it would be better and more accurate if it could be divided into more sheets, but it will also lead to some problems and implementation difficulties in Sonnet.

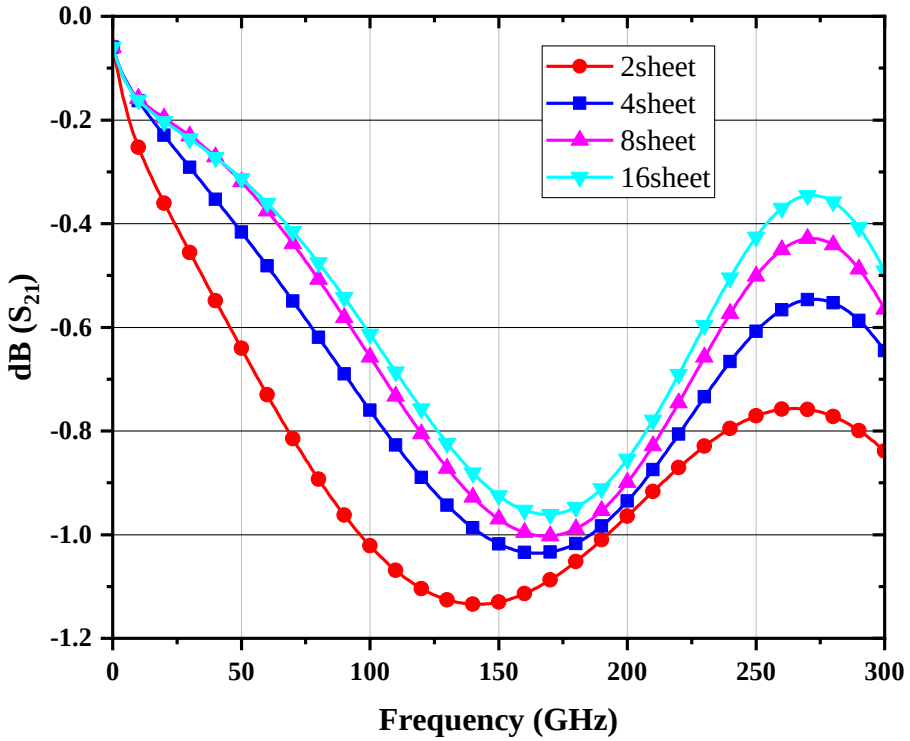

Fig. 2.32 Simulated insertion loss of the length of 275 μm transmission line (quarter wavelength of 140 GHz) and width of 2 μm under different numbers of sheets setups.

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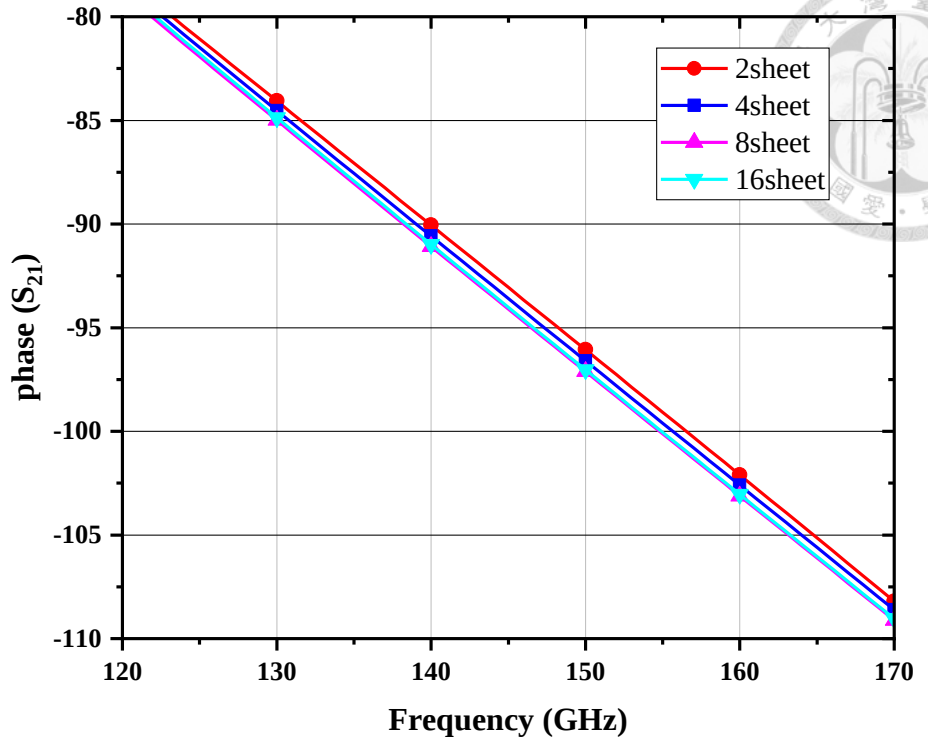

Fig. 2.33 Simulated phase of the length of a 275 μm transmission line (quarter wavelength of 140 GHz) and a width of 2 μm under different numbers of sheet setups.

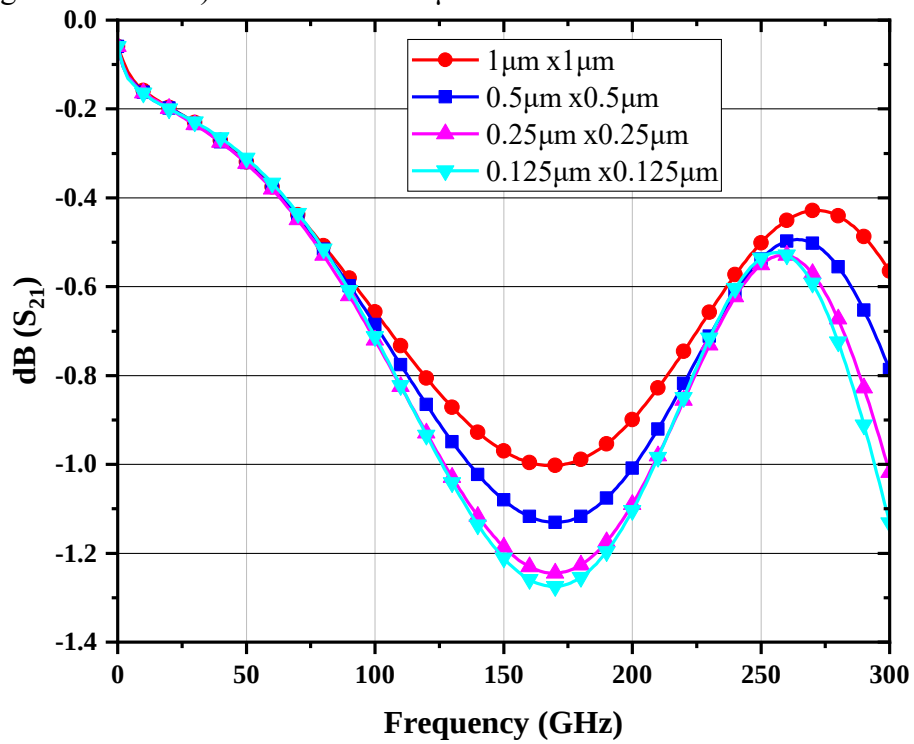

Fig. 2.34 Simulated insertion loss of the length of 275 μm transmission line (quarter wavelength of 140 GHz) and width of 2 μm under different cell sizes.

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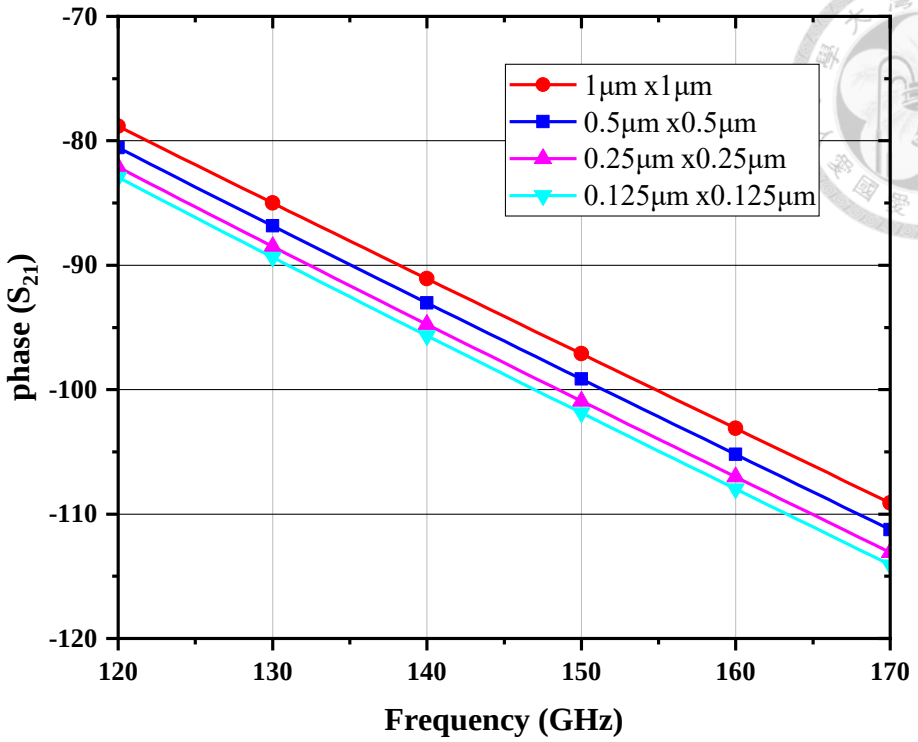

Fig. 2.35 Simulated phase of the length of a 275 μm transmission line (quarter wavelength of 140 GHz) and a width of 2 μm under different cell sizes.

Another influencing factor is cell size, which represents the smallest size that the EM simulation subdivides the circuit into subsections. Fig. 2.34 shows the simulation result of the phase of the length of a 275 μm transmission line (quarter wavelength of 140 GHz under this process) and a width of 2 μm under different cell sizes. It is obvious that the insertion loss of the transmission line of cell sizes of 1 μm x 1 μm and 0.5 μm x 0.5 μm has a much different value from the cell sizes of 0.25 μm x 0.25 μm and 0.125 μm x 0.125 μm. Fig. 2.35 shows the simulation result of the phase of the length of a 275 μm transmission line (quarter wavelength of 140 GHz under this process) and a width of 2 μm under different cell sizes. A similar result shows that the phase of cell sizes of 1 μm x 1 μm and 0.5 μm x 0.5 μm differ from those divided into smaller cell sizes. Therefore, the cell size of 0.25 μm x 0.25 μm would be considered as the maximum acceptable dimension in a two μm width transmission line simulation.

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However, these two setups of the EM simulation would increase the processing time and memory requirements. In this case, the processing time of increasing the number of sheets became three times from a two-sheet setup to an eight-sheet setup and even seven times to a sixteen-sheet setup; simultaneously, the memory also required approximately three and seven times, respectively. As for the smaller cell size, the processing time increased eleven times from 1 μm x 1 μm cell size to 0.25 μm x 0.25 μm cell size and terrifying 47 times to 0.125 μm x 0.125 μm cell size; at the same time, the memory required also became four and eleven times. Overall, the processing time and required memory from the two sheets and 1 μm x 1 μm cell size to the appropriate 8 sheets and 0.25 μm x 0.25 μm cell size roughly need 33 and 12 times in Sonnet. Therefore, the EMX Planar 3D Solver High-Frequency EM Simulator has been introduced to tackle this dilemma. The significant advantage of EMX is the adaptive mesh technique. It can mesh the edge of the metal layer very meticulously and merge the homogeneous plane mesh into a larger one to decrease computation loading.

In this work, the transmission line used in the matching network is mostly two microns in width, and the initial EM simulation is based on two sheets and a 1 μm x 1 μm cell size. Accordingly, the re-simulation was done in EMX with more than 8 sheets and a 0.25 μm x 0.25 μm cell size.

2.4.2 Device Model Measurement Result

From the foundry document, we can recognize that the RF model of 65-nm CMOS is only reliable under 30 GHz. The estimated parasitic capacitance and inductance caused by routing around the transistor would be different at higher frequencies. As a result, we have taped out the transistor used in this design and measured it using the TRL calibration method. TRL (Thru-Reflect-Line) [42] is a popular calibration technique used in vector

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network analyzers (VNAs) to remove systematic errors and improve measurement accuracy. It is widely used in RF and microwave applications, especially when other calibration methods (like SOLT - Short-Open-Load-Thru) are impractical. There are three key components in TRL calibration: Thru, Reflect, and Line. “Thru” represents a direct connection between the two measurement ports. This standard helps characterize port match and tracking errors. “Reflect” needs a high-reflection standard (e.g., open or short) that is identical at both ports. This helps determine port match and reflection tracking. “Line” consists of a transmission line of known length and impedance. This standard helps determine frequency response and delay.

TRL calibration offers high accuracy, whereas traditional SOLT (Short-Open-Load-Thru) methods may be impractical. Unlike SOLT, TRL does not require precision loads, as it relies on a known transmission line rather than perfectly characterized impedance standards. Additionally, TRL provides flexibility in non-50Ω environments as long as the line impedance is well-defined, making it suitable for customized test setups. One key constraint is the frequency range limitation, where the Line standard must have an electrical length between 20° and 160° to ensure accurate results, often requiring multiple line lengths for wideband measurements. This means that multiple calibrations may be needed to cover a broad frequency range.

Fig. 2.36 shows the layout of TRL calibration. The calibration length is 100 μm, which means the reference plane of calibration is 100 μm from the port. In (a), the Thru is composed of two 100 μm transmission lines connected to each other. In (b), the Reflect consists of port one shorted to the ground and port two open after a 100 μm transmission line. Another group is reversed to the first one, port one open and port two short after a 100 μm transmission line. In (c), the Line contains a quarter-wavelength transmission line between two ports and a 100 μm reference line. The quarter-wavelength transmission line

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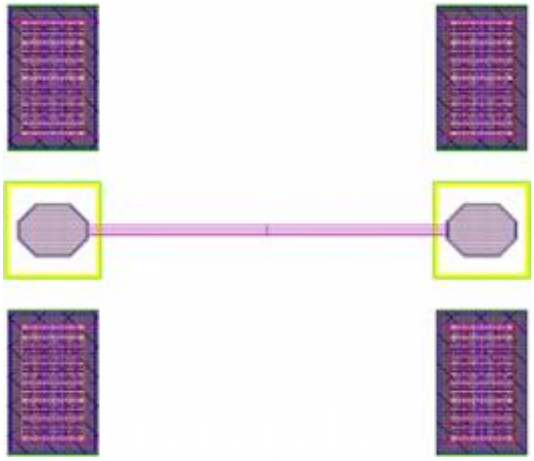
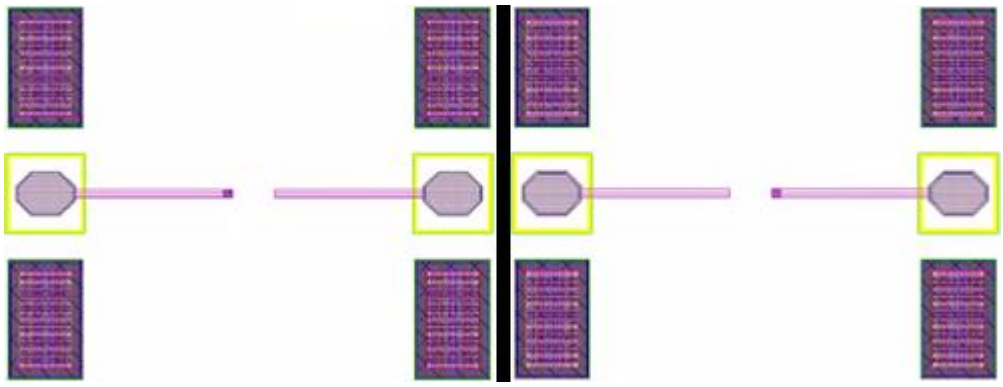
is set at 140 GHz, which means the valid calibration frequency band is 31 to 248 GHz. Fig. 2.37 demonstrates the layout of the proposed test device with a size of 1 μm x 10 fingers. Similar to the calibration design, the desired test device is connected to a 100 μm reference transmission line before the port. Fig. 2.38 illustrates the core layout of a common-source transistor, which replaces the common-source transistor in the proposed cascode configuration. Fig. 2.39 depicts another layout type of a common source transistor, which replaces the common-gate transistor in the proposed cascode configuration.



(a)



(b)

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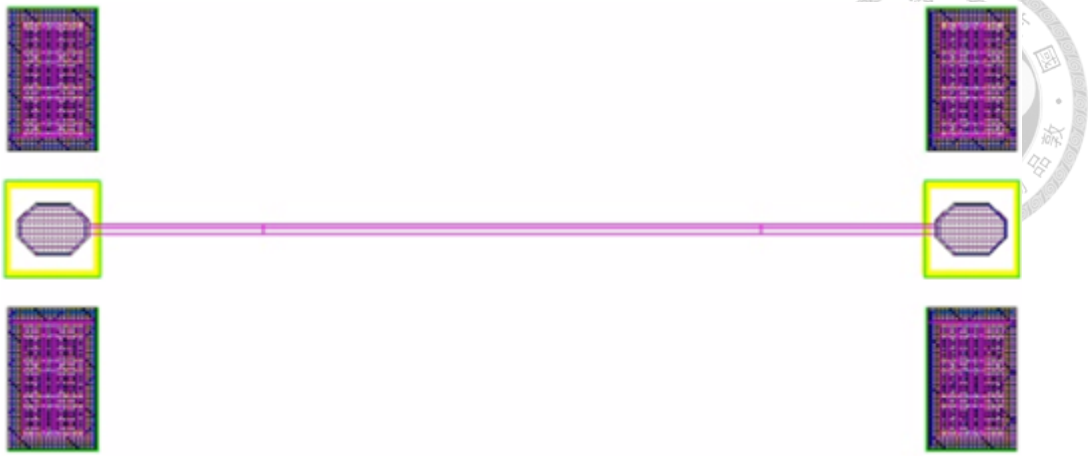

(c)

Fig. 2.36 Layout of TRL calibration, (a) Thru, (b) Reflect, (c) Line.

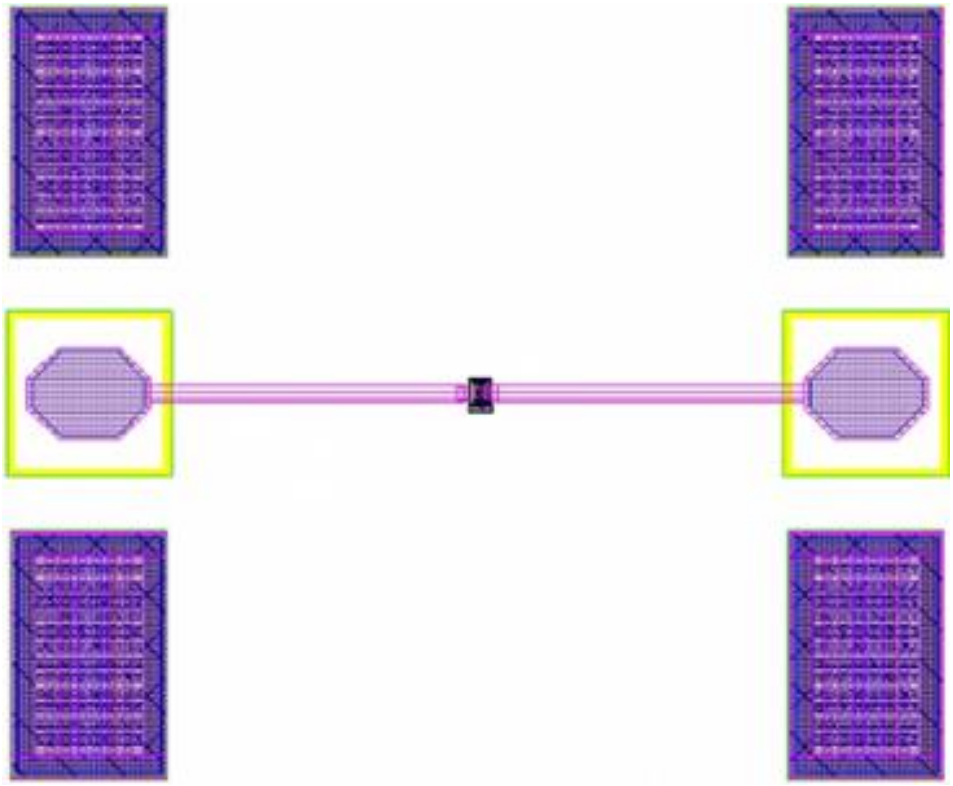

Fig. 2.37 Layout of test device with size of 1 μm x 10 fingers.

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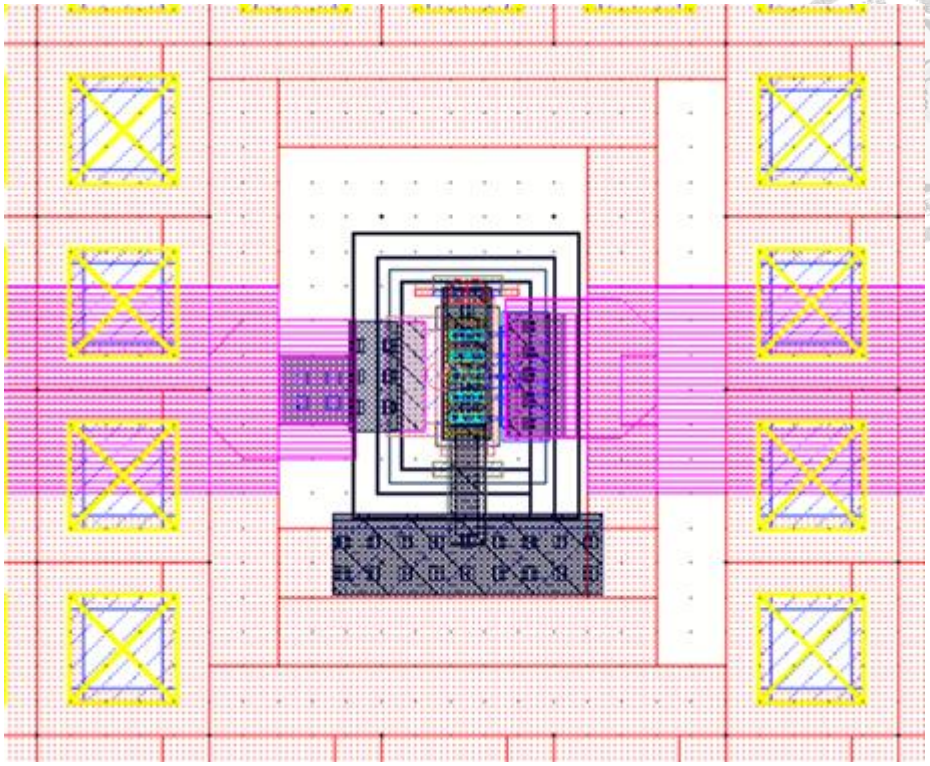

Fig. 2.38 The core layout of the CS device.

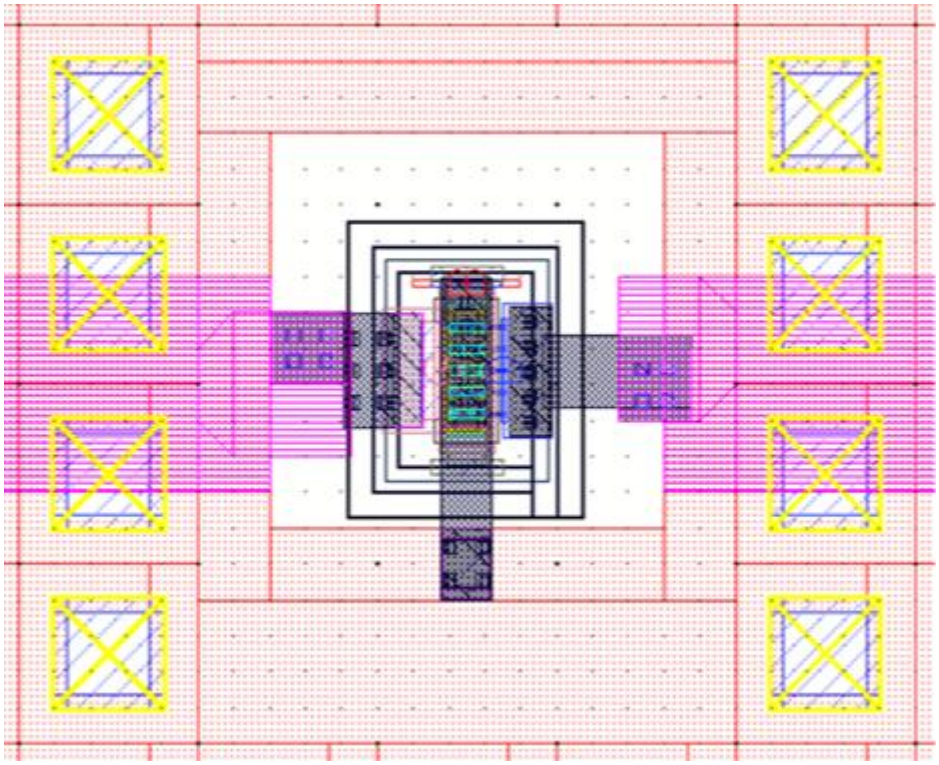

Fig. 2.39 The core Layout of the common-gate (CG) transistor in cascode (measured under common-source).

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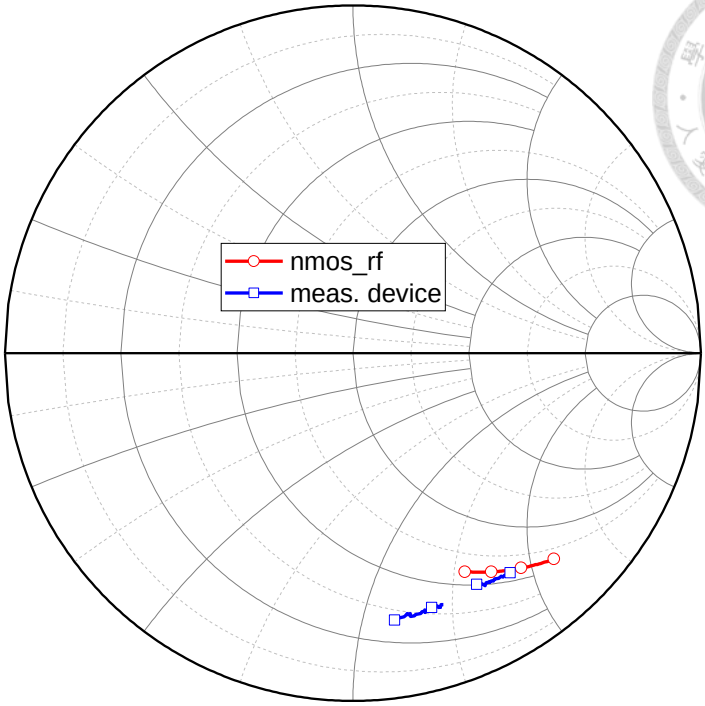

Fig. 2.40 S_{11} of the nmos_rf device and the measured device on the Smith chart.

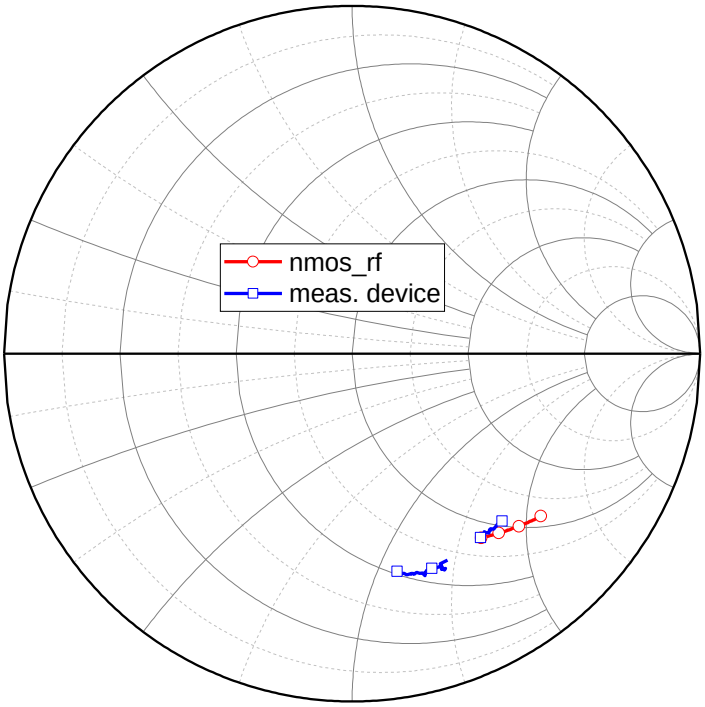

Fig. 2.41 S_{22} of the nmos_rf device and the measured device on the Smith chart.

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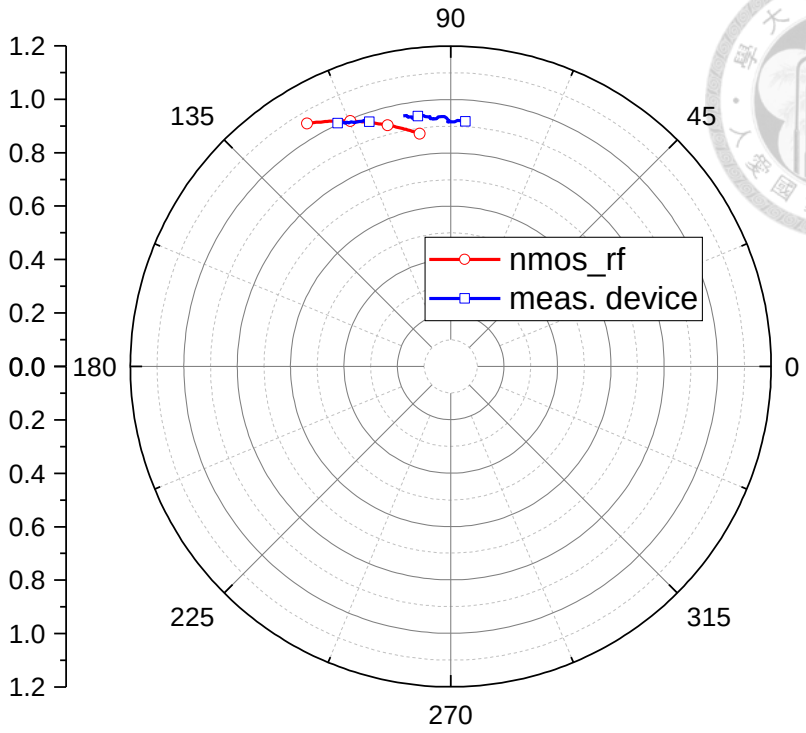

Fig. 2.42 S_{21} of the nmos_rf device and the measured device on the polar graph.

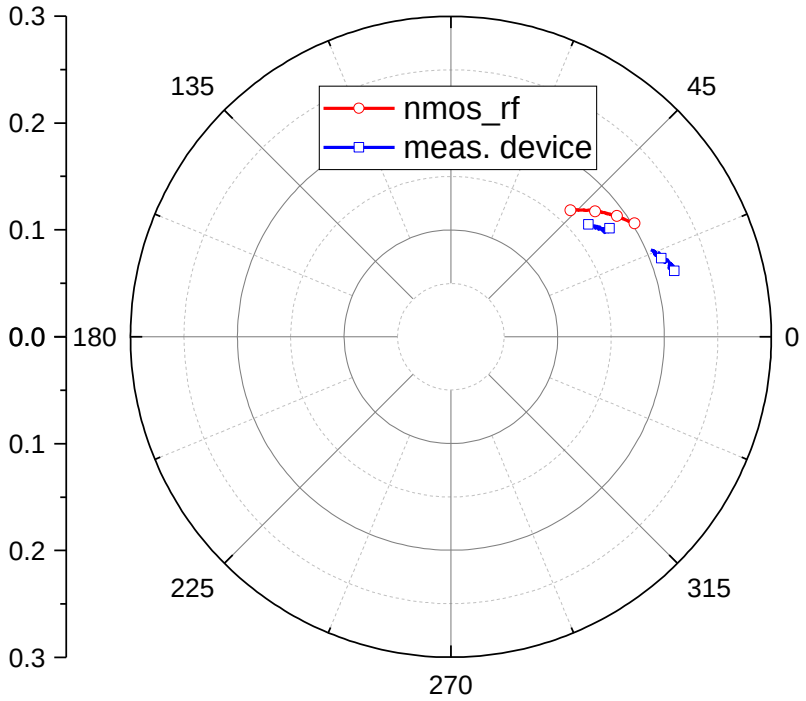

Fig. 2.43 S_{12} of the nmos_rf device and the measured device on the polar graph.

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The following measurement results are calibrated based on the previous TRL calibration design. Fig. 2.40 and Fig. 2.41 illustrate the S_{11} and S_{22} of the nmos_rf device and the measured device on the Smith chart. Due to the limitations of measurement instruments, the measured results, pink and green lines, show the results of 110 to 130 GHz and 140 to 170 GHz. The red and blue lines show the simulated results of nmos_rf at 110 to 170 GHz. It is clear that both S_{11} and S_{22} of the simulation and measurement results have huge differences. Fig. 2.42 and Fig. 2.43 depict the S_{21} and S_{12} of the nmos_rf device and the measured device on the polar graph. The graph shows that the results have the same trend as the previous two figures.

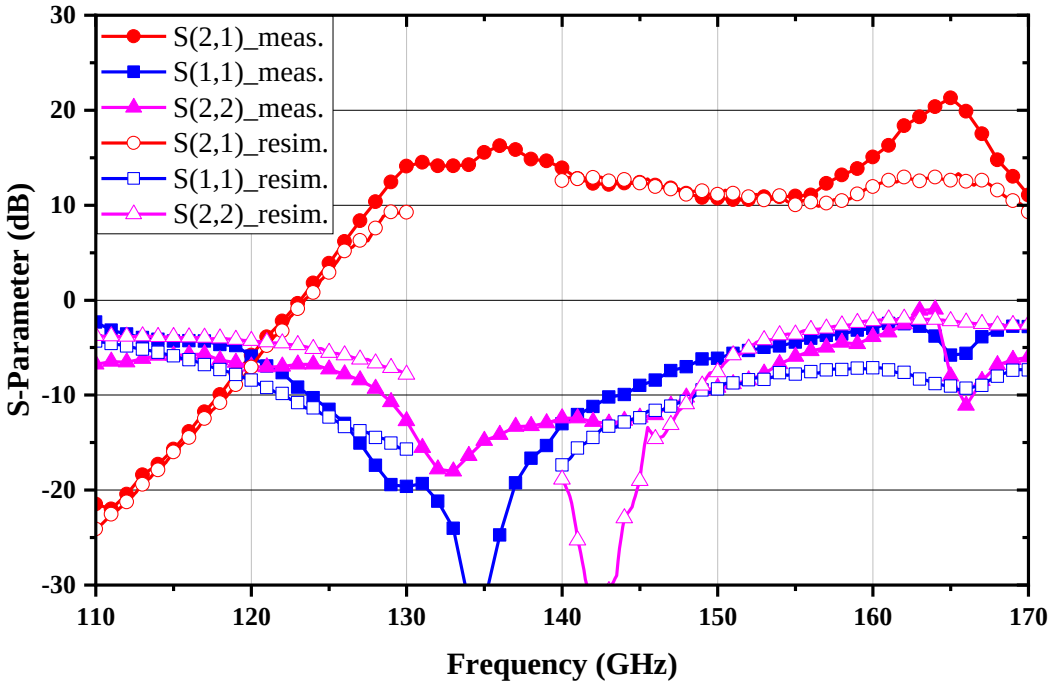

Fig. 2.44 The measured and re-simulated s-parameter with the measured device.

Fig. 2.44 shows the measured and re-simulated s-parameter. The re-simulation results contain EMX simulation results with more than 8 sheets and a 0.25 μm x 0.25 μm cell size, and the measured test device calibrated by TRL calibration. The results show that

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the significant problem in Fig. 2.28, frequency shifting about 10 GHz, has been resolved. The S-parameters of the measured and simulation results are well aligned at the desired frequency bands, except that the peak occurs at 160-170 GHz. One of the reasons may be that the common gate transistor substitute in is measured in a common source topology, which may be unable to accurately predict the realistic results. As a result, a specially designed common gate transistor in a test device is necessary.

2.4.3 NCH+EM Model

Due to the unmatched measurement and simulation performance in the high-frequency range of the proposed amplifier. The research on the RF model and the NCH model is conducted [39, 40]. As mentioned in Section 2.4.2, the reliable range provided by the foundry is to 30 GHz, although, with the previous works' experience, the model is still dependable around V-band. However, the results are getting unaligned while the frequency increases to W-band, and become more mismatched within D-band. As shown in Fig. 2.45, the estimated parasitic capacitance and inductance introduced by routing around the transistor would be different at higher frequencies. As a result, the re-simulation of the routing is conducted, and the simulation results are combined with the NCH model, forming the new RF device model, as shown in Fig. 2.46. Fig. 2.47 and Fig. 2.48 depict the top view and bottom view of the NCH + EM simulation setting. The port is excitation at the circled red area. The three ports in top view are regarded as the source, gate, and drain of the new device. The three output ports of the bottom view are connected to the NCH transistor, respectively, forming a new NCH + EM device. Fig. 2.49 shows the re-simulation results with the new NCH + EM device compared to the original simulation and measurement results. It is obvious that the overall performance of the entire band aligned well. Especially, the peak at the frequency of 160 to 170 GHz predicts

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much better than the simulation done in the measured device shown in Fig. 2.44.

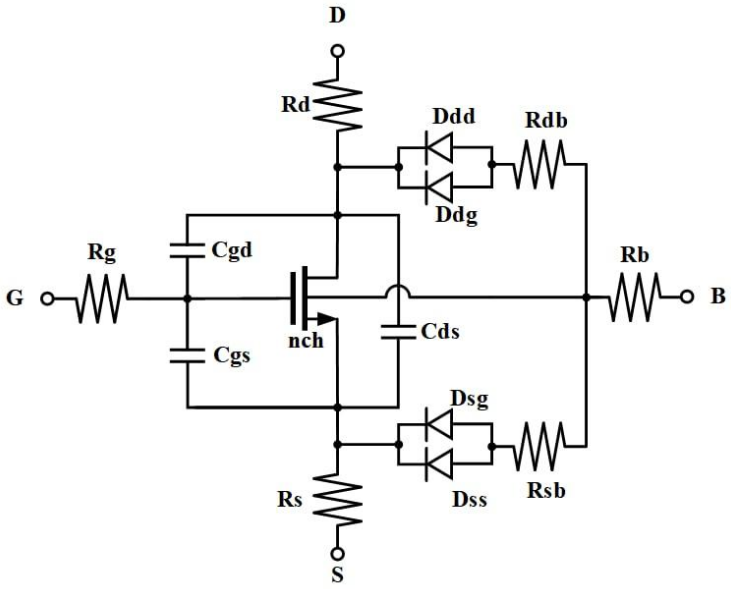

Fig. 2.45 The schematic diagram of the NMOS_RF model.

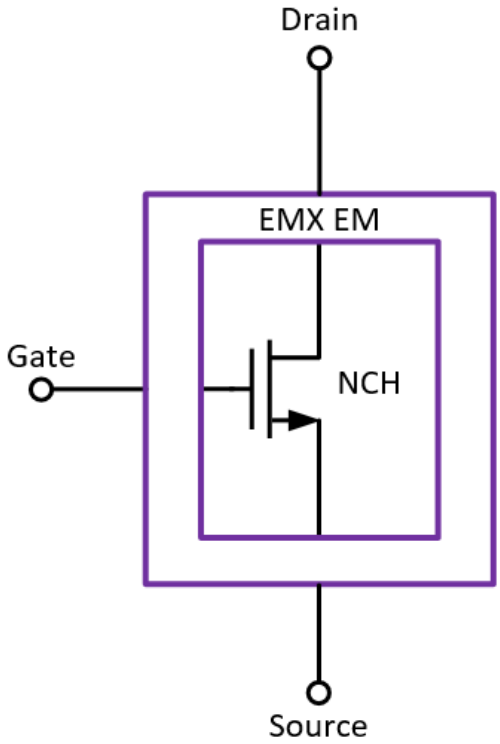

Fig. 2.46 The schematic diagram of the NCH + EM model.

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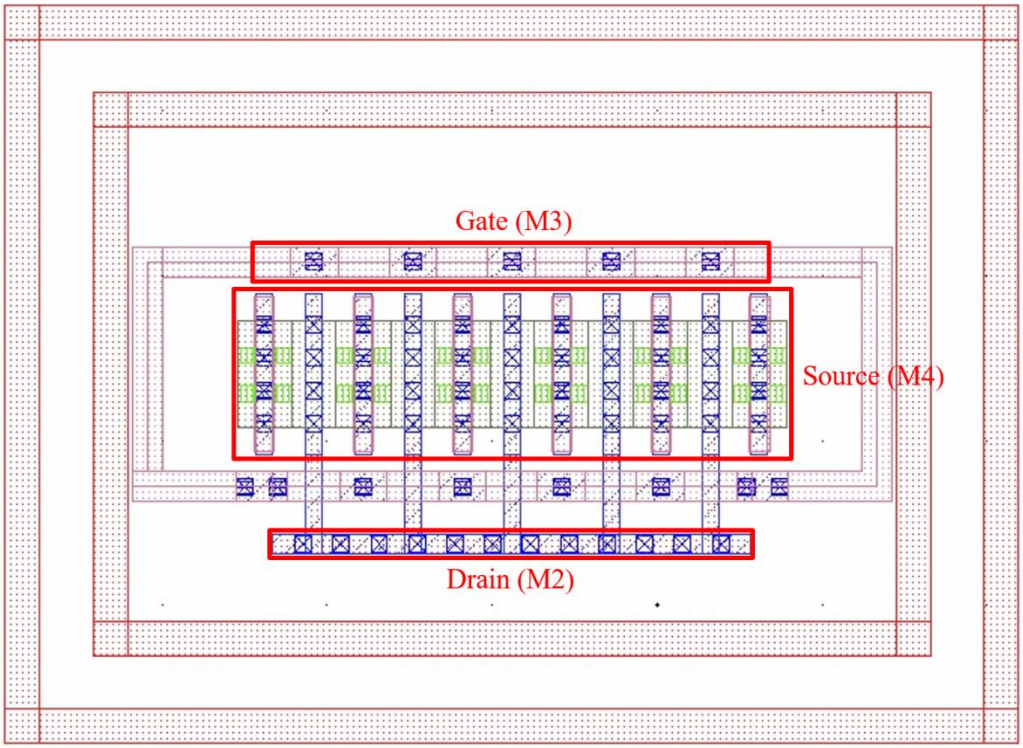

Fig. 2.47 Top view of NCH + EM simulation setting.

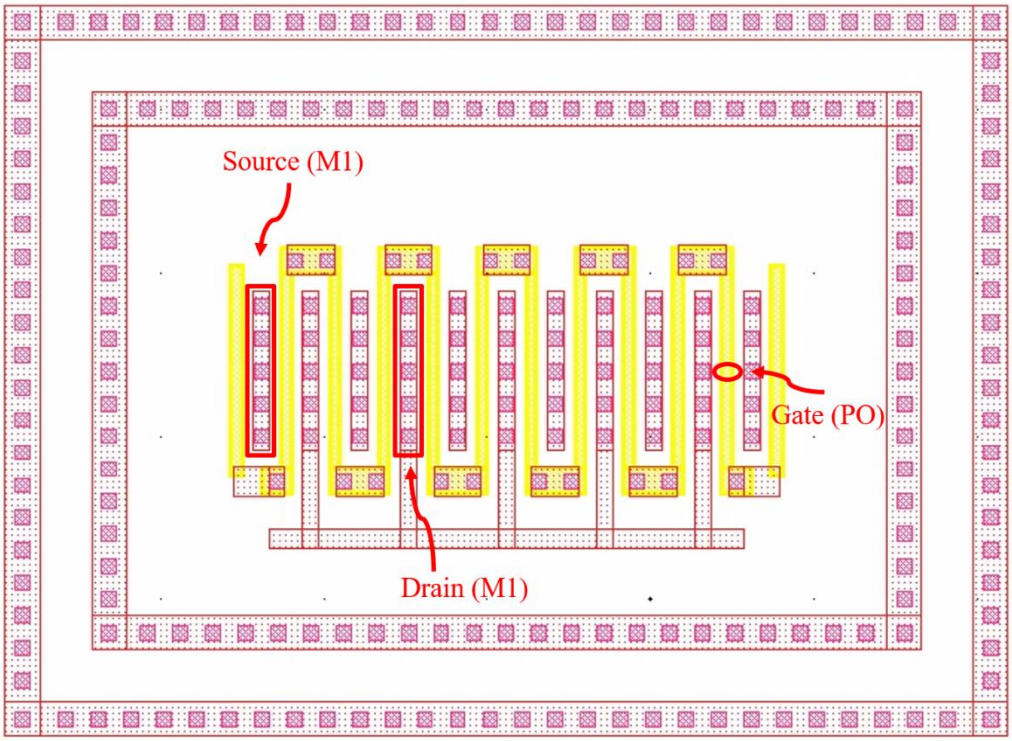

Fig. 2.48 Bottom view of NCH + EM simulation setting.

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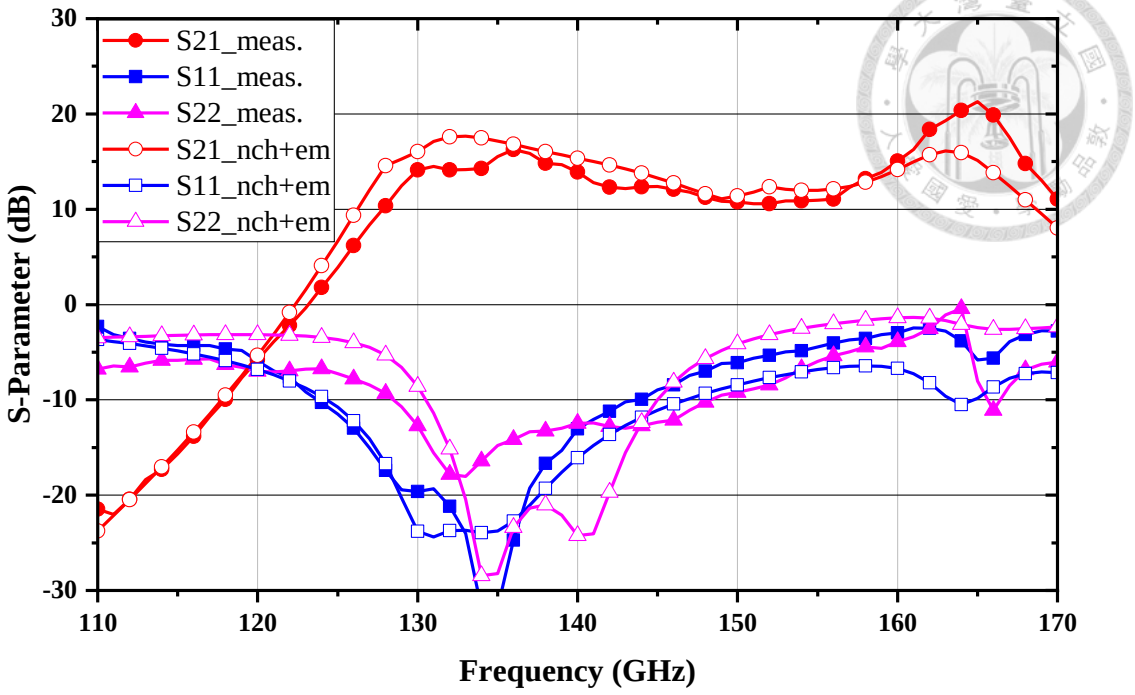

Fig. 2.49 The measured and re-simulated s-parameter with Nch+em device.

2.5 Summary

This chapter focuses on a D-band broadband amplifier design in a 300 GHz phased-array transceiver system fabricated in a 65-nm CMOS process. To achieve enough gain and bandwidth performance, a three-stage cascode structure with a gain-boosting technique is adopted, and a compensated matching technique is utilized in the design to broaden the bandwidth. With 39.3 mW DC power consumption, the measurement results showed that the bandwidth with a small-signal gain larger than 10 dB is 128 to 170 GHz. The peak gain is 21.3 dB at 165 GHz. The measured output-referred 1-dB compression point power levels are -7.4, -3.7, and -7.3 dBm at 140, 150, and 160 GHz, respectively. Furthermore, the core area of this work is highly compact, nearly half the size of other similar structures shown in Table 2.4. Furthermore, the EM simulation setup, the device measurement, and the Nch+em model have also been discussed in this work, which makes

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the simulation and measurement results of the proposed amplifier show good alignment in the desired frequency bands.

Table 2.4 Performance comparison of recently published CMOS D-band amplifiers and proposed driving amplifier.

Ref.	Process	Topology	Freq. (GHz)	Peak Gain (dB)	OP_{1dB} (dBm)	P_{dc} (mW)	Core Area (mm^2)
[17]	65-nm CMOS	8 x CS	101.5~142.1	20.6	-3.1@120GHz	45	0.182
[18]	65-nm CMOS	Differential 6 x CS	110.6~121.8	13.8	-14@116GHz	40	0.6
[19]	65-nm CMOS	4 x cascode + 1 x CS	110~180*	19	N/A	66	0.21***
[43]	28-nm FDSOI CMOS	4 x CS	143~166	15.7	> -3 @155~165GHz	32	0.34
[44]	65-nm CMOS	1 x CS	126~136**	5.1	N/A	8.625	0.112***
[45]	45-nm SOI CMOS	3 x CS	125~155**	9.9	N/A	38.25	0.347***
This Work	65-nm CMOS	3 x cascode	128~170*	21.3	-7.4@140GHz -3.7@150GHz -7.3@160GHz	39.3	0.1

*Gain > 10 dB, **Estimated from the figure, ***Estimated from the chip photograph.

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Chapter 3 Design of D-Band Frequency Doubler with Gain-Boosting Technique in 65-nm CMOS Process

3.1 Introduction

The advancement of millimeter-wave and sub-terahertz wireless systems has underscored the critical need for generating stable, low-phase-noise local oscillator (LO) signals, especially near the D-band (110–170 GHz), to support high-speed communication and sensing applications. However, direct generation of such high-frequency signals faces significant challenges, including degraded phase noise, limited tuning range, and increased circuit complexity. Frequency multiplication techniques are widely employed to address these issues by sequentially upconverting a low-phase-noise reference signal. Frequency doublers play a vital role by efficiently generating second harmonics while suppressing undesired components, thus maintaining high spectral purity. Compared to direct generation, frequency multiplication allows circuits to operate at lower intermediate frequencies where device performance is better, enabling improved phase noise, greater design flexibility, and enhanced system scalability, making it the preferred method for D-band LO signal generation.

Fig. 3.1 shows the architecture of the proposed D-band LO chain. This work presents the design and implementation of a compact, low-power D-band frequency generation system using a six-times frequency multiplier (sextepler) followed by a frequency doubler stage and a D-band power amplifier (PA), which collectively generate a high-frequency LO signal in the 132–162 GHz range. This signal drives a subharmonic mixer for up-conversion with differential I/Q intermediate frequency (IF) inputs. Table 3.1 shows the design goals of a D-band driving amplifier.

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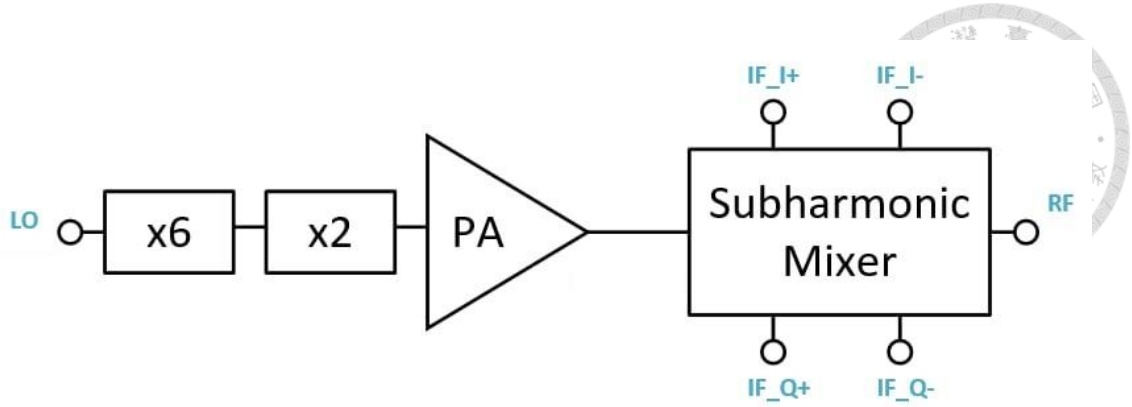

Fig. 3.1 The architecture of the D-band LO chain.

Table 3.1 The design goals of the D-band frequency doubler.

	Specification
Process	65-nm CMOS process
Output Frequency (GHz)	138-160
Conversion Gain (dB)	> -5
Input Power (dBm)	> -2
Harmonic Suppression (dBc)	> 20

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In this work, based on the measurement results, the proposed frequency doubler exhibits a 3-dB bandwidth of 143 GHz to 170 GHz. The peak conversion gain of -3.5 dB occurs at 158 GHz, and the peak output power is 0.76 dBm at 158 GHz with 4.3 dBm input power. The fundamental rejection is greater than 41.3 dBc within the frequency bandwidth. The total DC power consumption is 16.3 mW under 3 dBm input power, and the total chip size is 0.262 mm^2.

Chapter 3 will demonstrate the proposed D-band frequency doubler for the 140 GHz LO chain. Chapter 3.2 introduces the design of the proposed frequency doubler, which is based on a push-push topology. For the purpose of enhancing the output power and conversion gain performance, a common gate transistor is connected after the push-push structure, forming the cascode configuration. To further improve the conversion gain performance of the frequency doubler at the D-band, a gain-boosting technique is adopted. Adding a transmission line at the gate of the common gate transistor of the cascade can increase the gain performance. Chapter 3.3 shows the measured results of the proposed frequency doubler. Chapter 3.5 discusses the unmatched results and re-simulation of the RF model. Chapter 3.5summarizes this work.

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3.2 The Design of D-band Frequency Doubler

3.2.1 Biasing Selection and Device Size Selection

There are several key factors in selecting the device size of a frequency doubler, including conversion gain, output power, and matching difficulty. The following simulations are based on the setup shown in Fig. 3.2. Generally, the biasing point of the frequency doubler is at Class-B to make sure the transistor is operating in the linear region and delivers maximum second harmonics to optimize the conversion gain. Fig. 3.3 shows the simulated drain current under different input power. Fig. 3.4 demonstrates the simulated second-order transconductance (gm_2) versus gate voltage (V_g) under small signal. The maximum point occurs at 0.34 V. Nevertheless, the frequency doubler often operates at higher input power, which makes the peak gm_2 occur at a lower gate voltage. Fig. 3.5 illustrates the simulated conversion gain and output power versus different V_g under a total gate width of 12 μm and 3 dBm input power. The final selection of bias conditions is 0.35 V of V_g and 1.2 V of V_d.

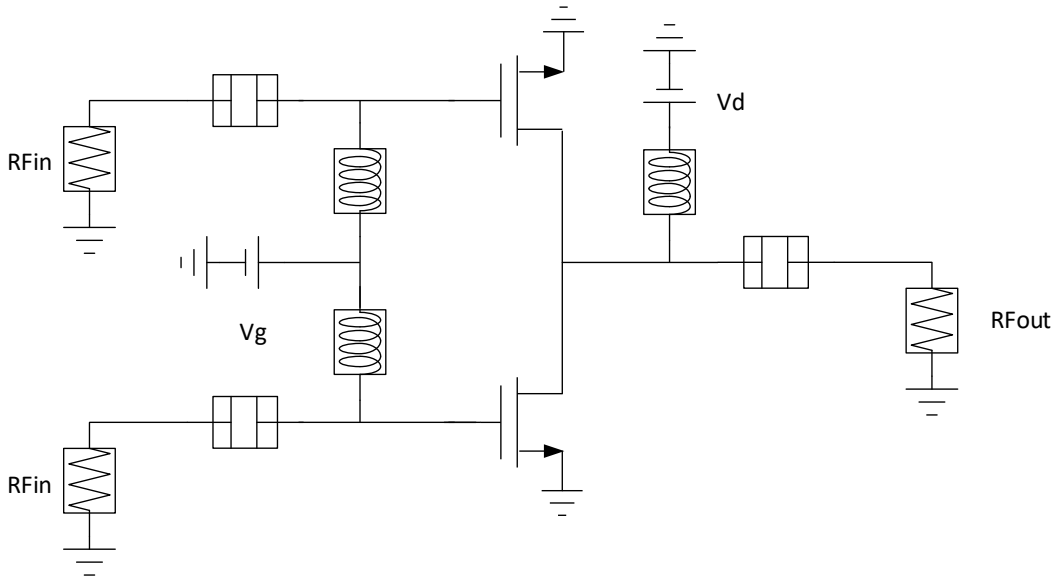

Fig. 3.2 The schematic of the simulation circuit for selecting DC bias and device size.

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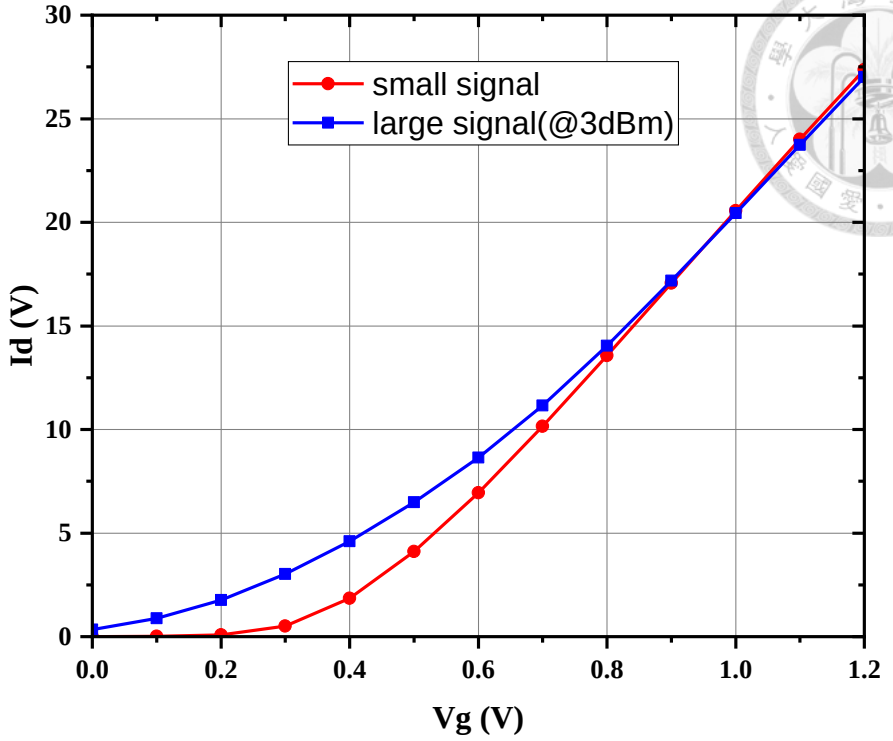

Fig. 3.3 The simulated drain current under different input power versus V_g.

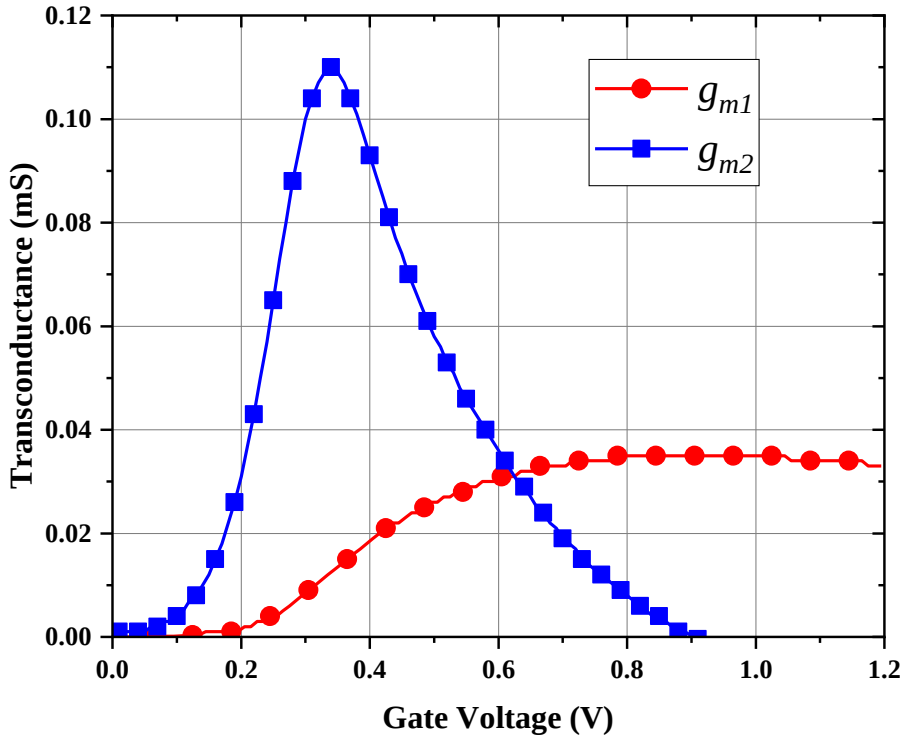

Fig. 3.4 The simulated first- and second-order transconductance versus V_g.

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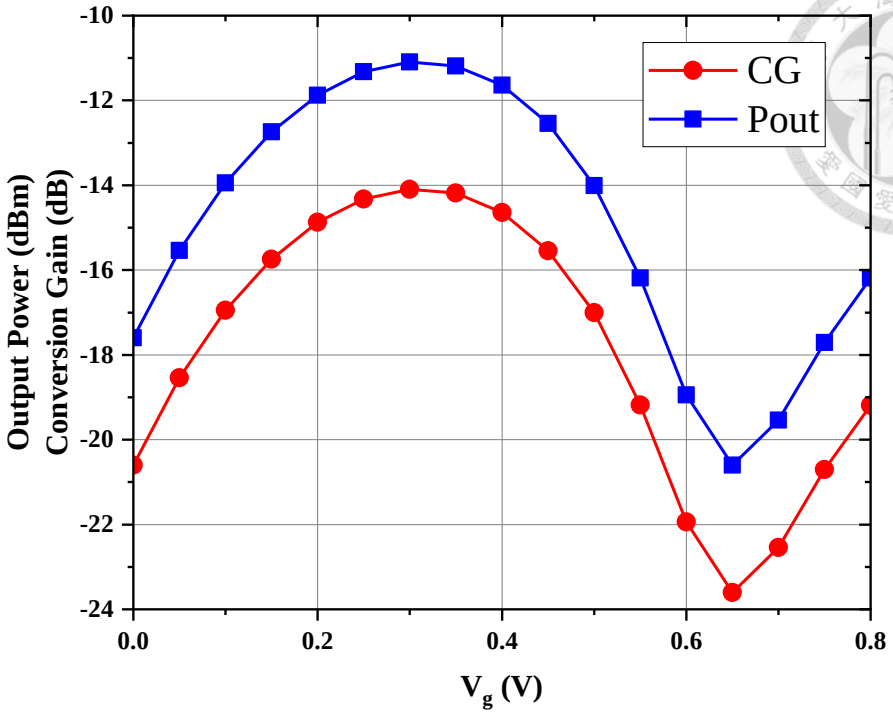

Fig. 3.5 The simulated conversion gain and output power versus V_g.

The larger transistor delivers higher output power while consuming higher DC power and degrading the conversion gain due to high parasitic capacitors. Moreover, the larger device also saturates at higher input power. In this work, the doubler must deliver maximum output power at an input of only 3 dBm due to specification limitations. Consequently, the device size selected for this work is relatively small, allowing for earlier saturation. Fig. 3.6 and Fig. 3.7 show the simulated conversion gain and output power with different device sizes versus input power. The bias conditions in these two graphs are 0.35 V and 1.2 V for V_g and V_d. This figure confirms the previous inference that the larger the size, the higher the saturation power. However, the conversion gain performance is poor, and the output power is inadequate at moderate input power. The total gate width of 12 μm and 18 μm shows the best performance at the desired 3 dBm input power. Fig. 3.8 and Fig. 3.9 illustrate the input and output impedance with different transistor sizes. Fig. 3.10 depicts the input impedance of the common gate transistor,

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which is the following stage of the push-push structure. Since there's no extra interstage matching design between the push-push structure and the common gate transistor. The output impedance of the chosen size shown in Fig. 3.9 should also be considered to be close to the input impedance shown in Fig. 3.10. As a result, based on previous simulations, the transistor size of the push-push stage is chosen to be a total gate width of 12 μm, which demonstrates not only a closer impedance to following stage but also a lower dc power consumption compared to 18 μm.

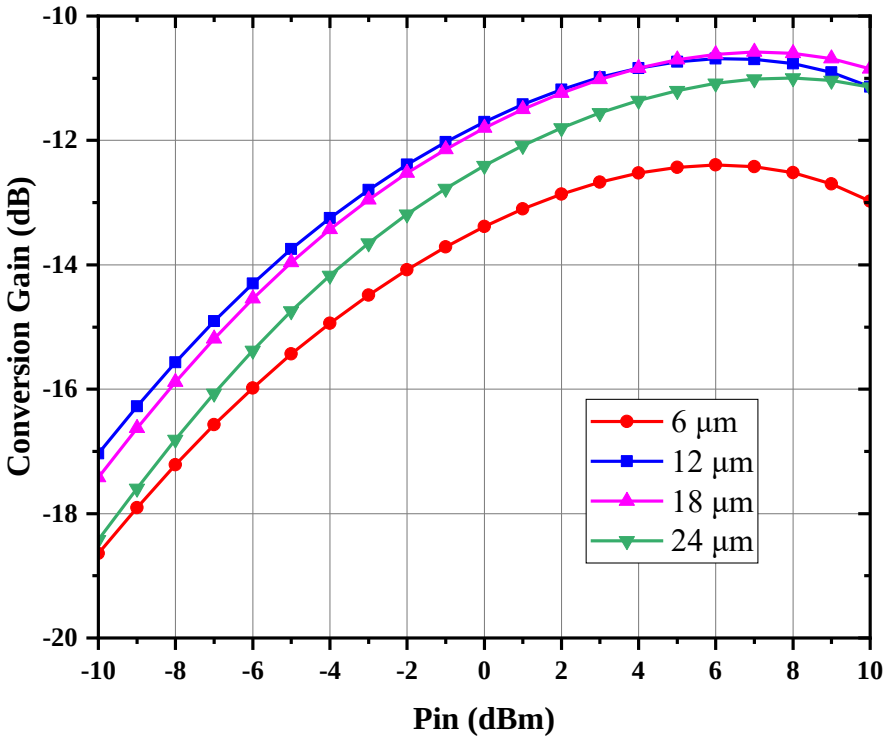

Fig. 3.6 Simulated conversion gain with different total gate widths versus input power.

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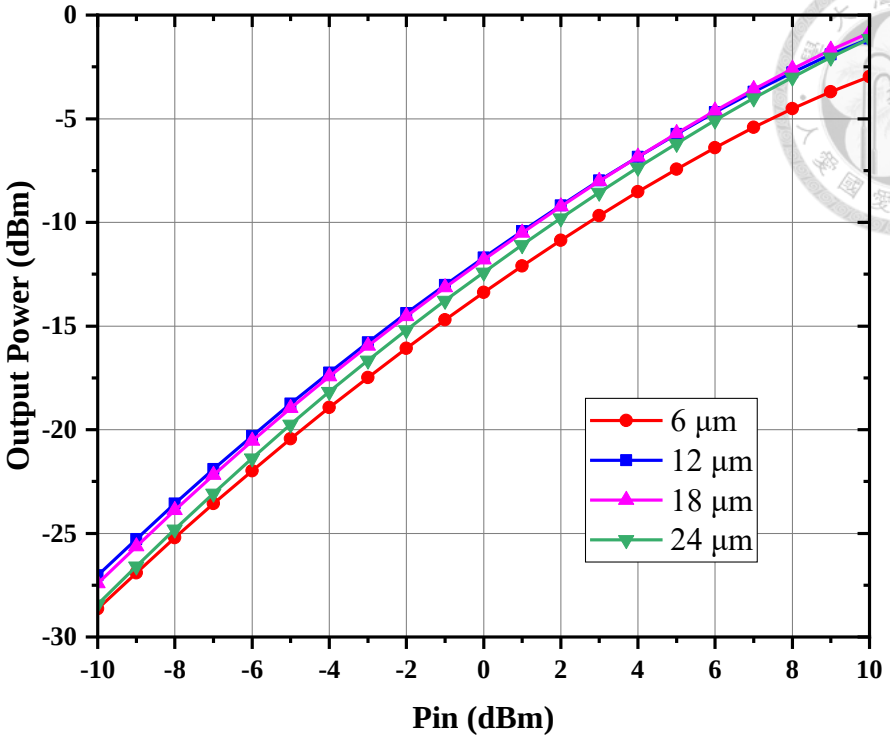

Fig. 3.7 Simulated output power with different total gate widths versus input power.

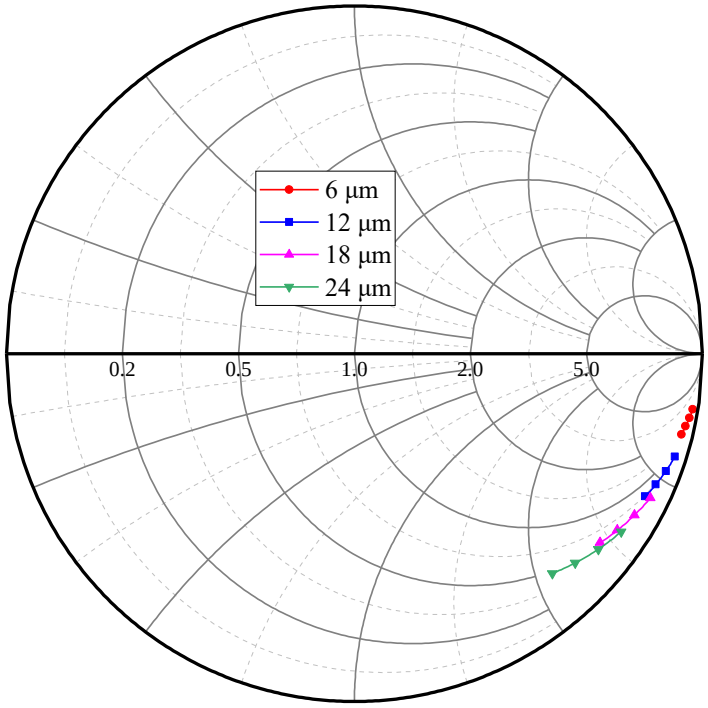

Fig. 3.8 Simulated input impedance of the push-push structure with different transistor sizes at the frequency of 60-90 GHz.

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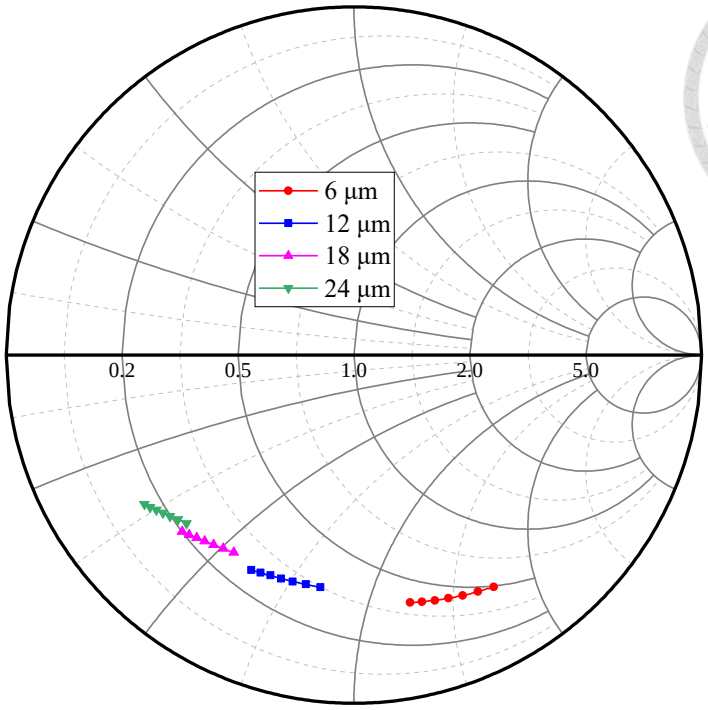

Fig. 3.9 Simulated output impedance of the push-push structure with different transistor sizes at the frequency of 120-180 GHz.

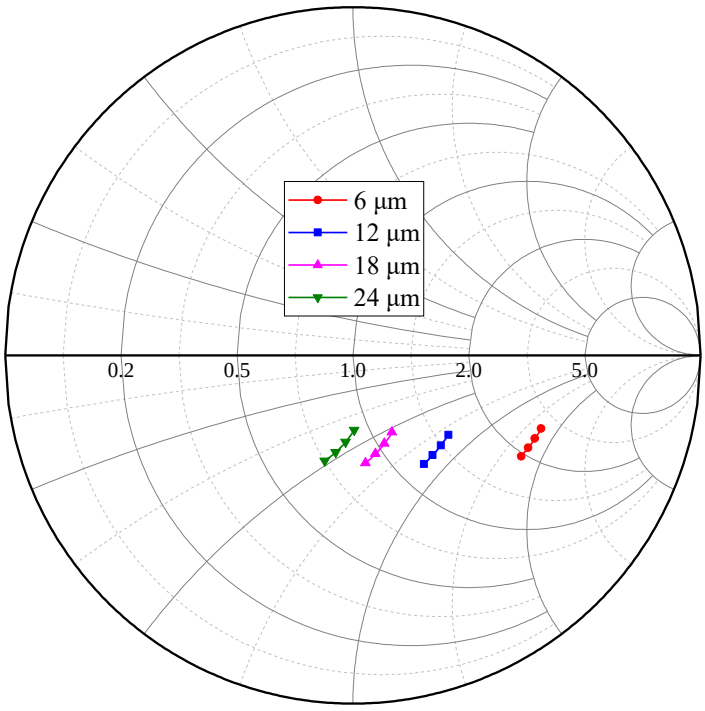

Fig. 3.10 Simulated input impedance of the common gate transistor with different transistor sizes at the frequency of 120 to 180 GHz.

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3.2.2 Cascode configuration and Gain-Boosting technique

The cascode configuration is adopted in this work to achieve higher conversion gain and output power performance. By connecting a common gate transistor after the push-push structure, not only can it enlarge the signal, but the gain-boosting technique can also be applied to this topology. As mentioned and derived in Section 2.2.3, adding the transmission line at the gate of the common gate transistor can push the turning point of the cascode stage toward a higher frequency and increase the MSG at high frequency. Nevertheless, the gain-boosting technique will degrade the stability of the circuit due to the positive feedback. Fortunately, the stability of the frequency doubler is usually better than that of the amplifier due to lower gain performance. As a result, the gain-boosting technique is appropriate to carry out in the frequency multiplier design.

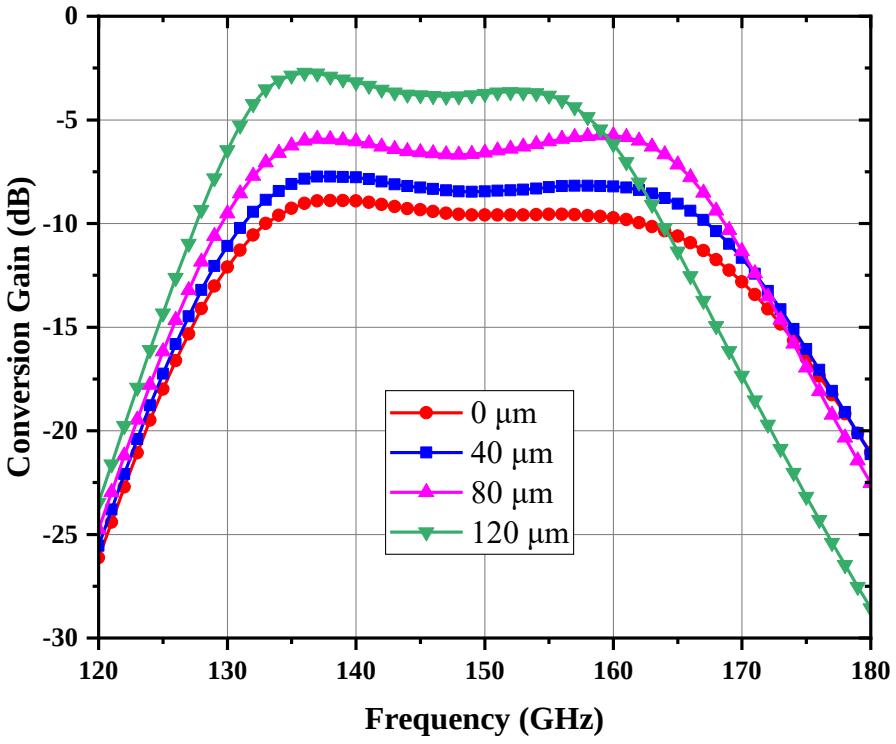

Fig. 3.11 The simulated output power versus frequency under different lengths of gain-boosting transmission line is added.

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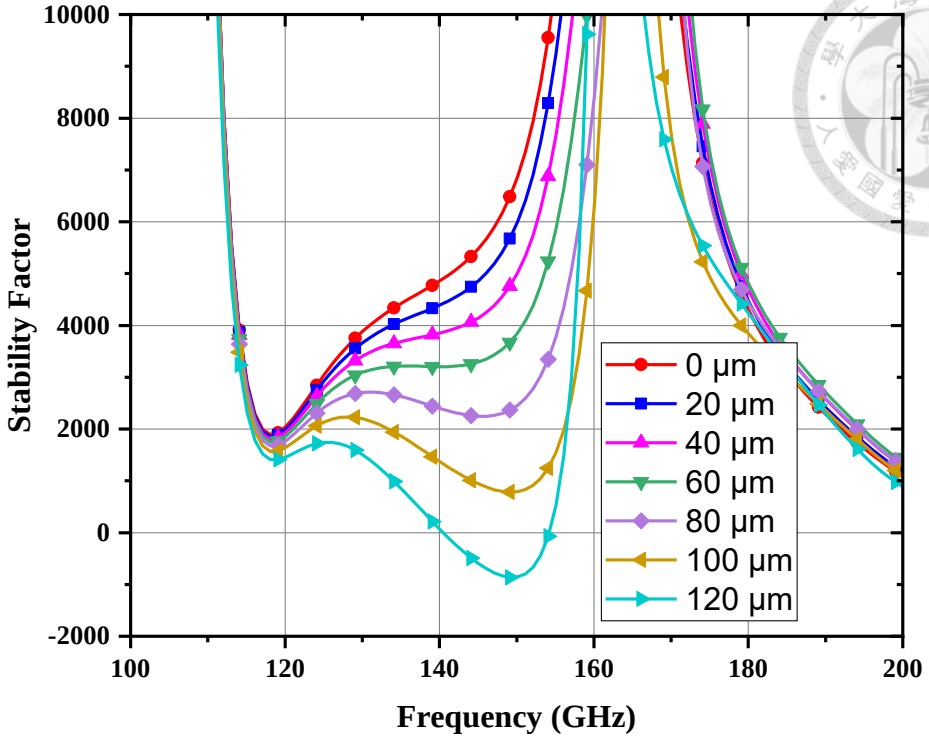

Fig. 3.12 The simulated stability factor versus frequency under different lengths of gain-boosting transmission line is added.

As shown in Fig. 3.18, the gain-boosting transmission (red TL) is added at the gate of the common gate transistor of the cascode configuration. Fig. 3.11 shows the simulated conversion gain versus output frequency while adding different lengths of transmission line. The results reveal that the conversion gain improved as the length of the line increased. However, as shown in Fig. 3.12, the simulated stability factor under different lengths of transmission line illustrates that the stability factor is degraded as the length of the line increases. Based on these simulation results, the length of transmission is selected to be 80 μm. Fig. 3.13 shows the output matching performance. It is obvious that the output matching can play the role of a high-pass filter, which can greatly increase the fundamental rejection performance of the frequency doubler. In this design, the fundamental rejection improved by 20 –30 dB in the desired frequency band.

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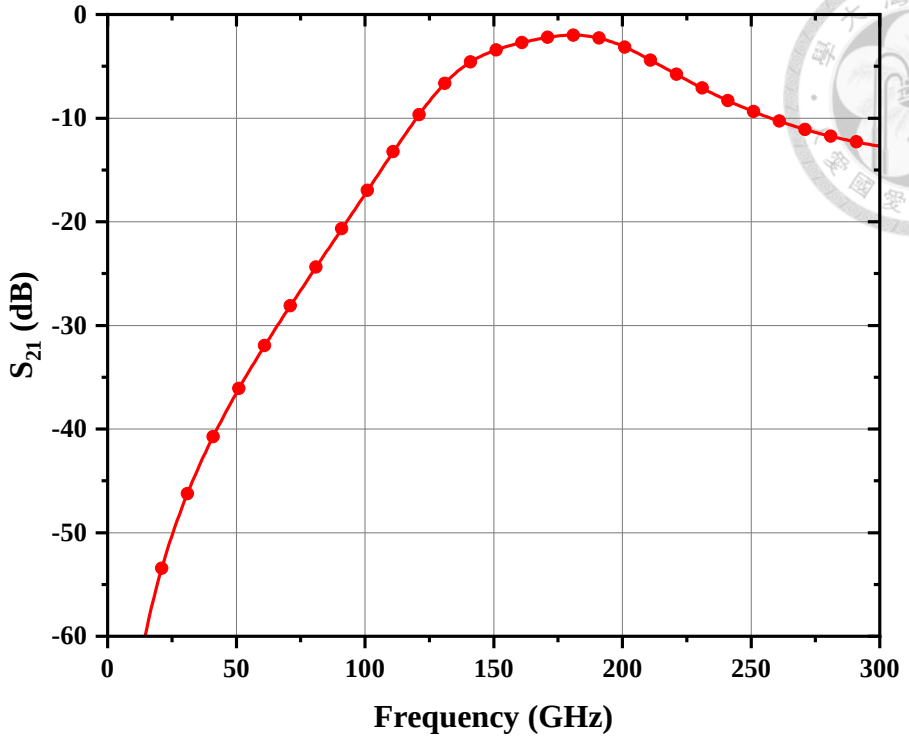

Fig. 3.13 The output matching performance.

3.2.3 Marchand Balun Design

To realize the fundamental cancelling and frequency-doubling function in push-push configuration, the 180-degree phase difference is indispensable. Two commonly used passive elements that can achieve this are the transformer and the Marchand balun. Nevertheless, the transformer is challenging to realize in such high-frequency bands due to the limitation of the self-resonance frequency of coupling inductors. As a result, the Marchand balun structure is more favorable in this design. Fig. 3.14 shows the schematic and top-view of the EM structure of the Marchand balun. Amplitude and phase imbalance between the two ports of the Marchand balun significantly affect the fundamental rejection performance of the frequency doubler. [27] introduces a novel compensated Marchand balun, which can improve the balance of two ports and can effectively improve the fundamental rejection.

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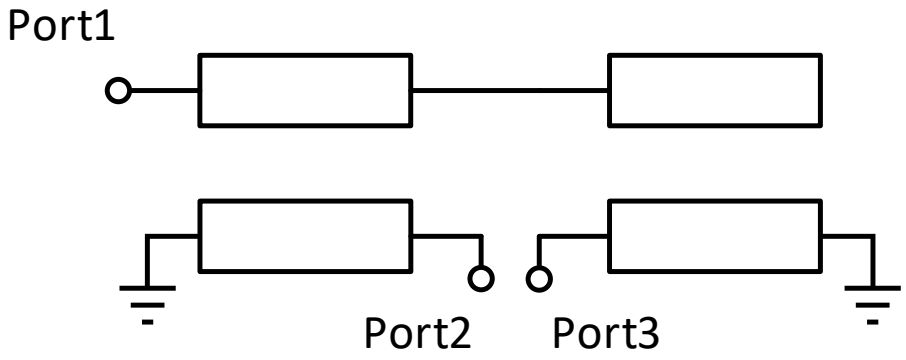
Fig. 3.15 demonstrates the simulated S-parameters of the Marchand balun proposed in this work. The minimum insertion loss of the Marchand balun is -1.5 dB, and less than 2.2 dB in the proposed frequency bands. Fig. 3.16 indicates the simulated amplitude imbalance between ports 2 and 3 of the Marchand balun with only 0.05 dB in 65 to 84 GHz. Fig. 3.17 shows the simulated phase imbalance of the Marchand balun, with an approximate 178.5 ± 0.2° phase shift in the 65 to 84 GHz range. The three-port common-mode rejection ratio (CMRR) proposed by Bockelman and Eisenstadt is adopted in this work [46]. The figure-of-merit (FOM) of the CMRR is shown as

$$\mathrm{CMRR} = \sqrt{\frac{(2+\Delta)^2 + \theta^2(1+\Delta)^2}{\Delta^2 + \theta^2(1+\Delta)^2}} \approx \frac{2+\Delta}{\sqrt{\Delta^2+\theta^2}} \tag{3.1}$$

where Δ and θ are the amplitude and phase imbalance of a balun. According to the simulation results mentioned above, the proposed compensated Marchand balun exhibits the essential 180-degree phase difference between the two ports. Simultaneously, it demonstrates excellent performance in terms of amplitude and phase imbalance, making it a reliable component in achieving the proposed frequency doubler functionally.



(a)

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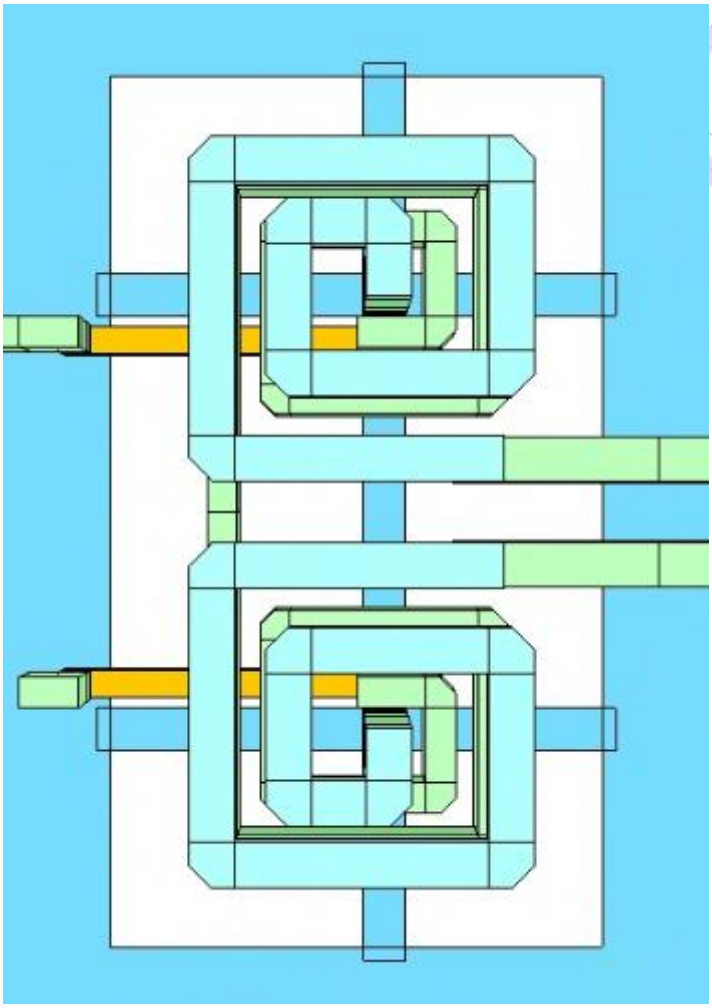

(b)

Fig. 3.14 The (a) Schematic and (b) Top view of the Marchand balun.

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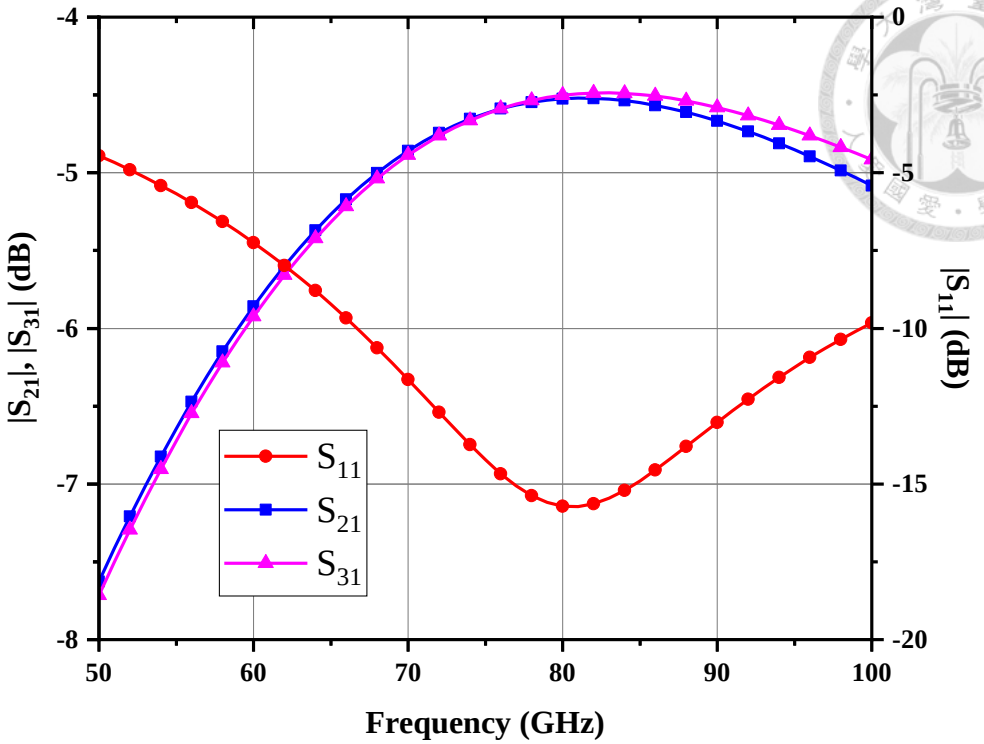

Fig. 3.15 The simulated s-parameter of the Marchand balun.

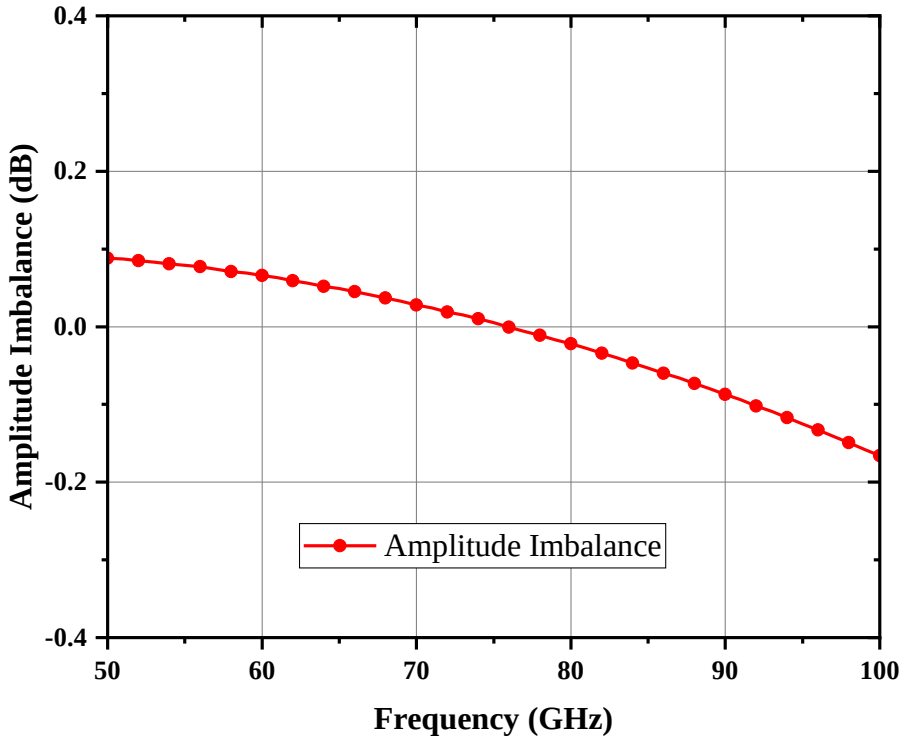

Fig. 3.16 The simulated amplitude imbalance of the Marchand balun.

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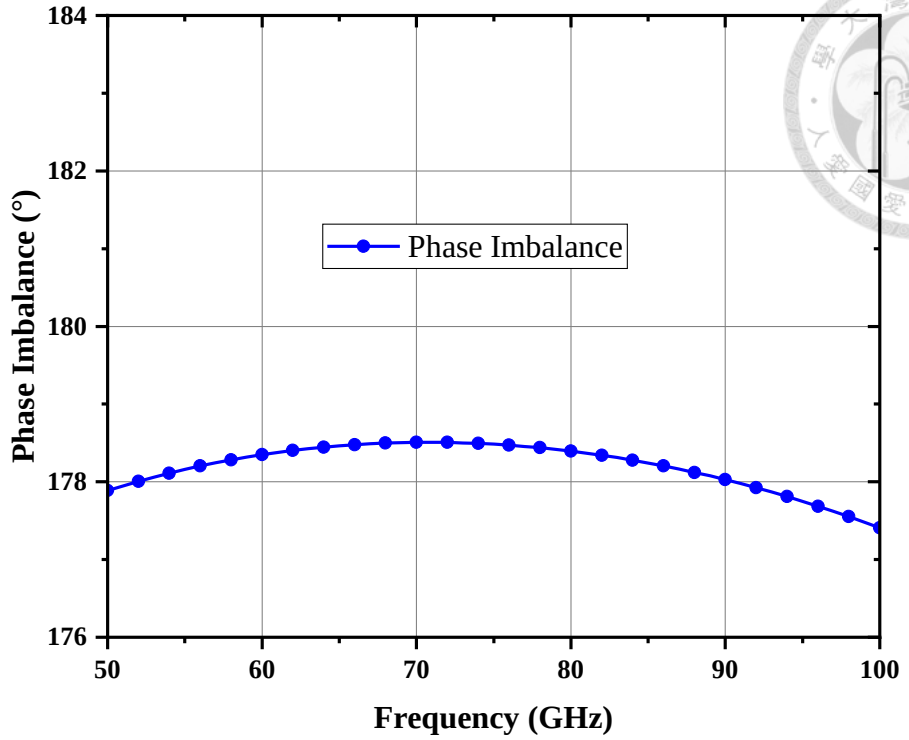

Fig. 3.17 The simulated phase imbalance of the Marchand balun.

3.2.4 Circuit Architecture and Post-layout Simulation Results

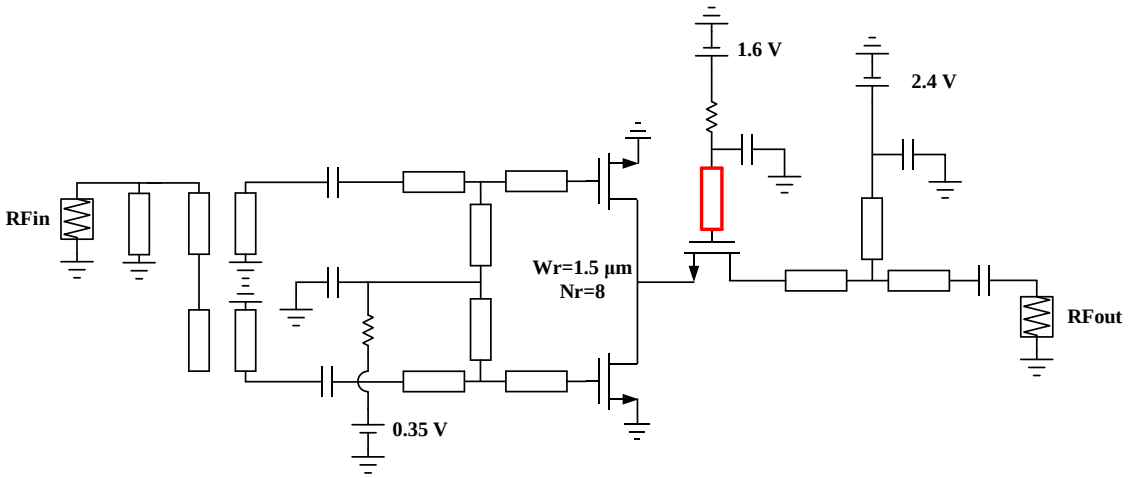

Fig. 3.18 The circuit schematic of the proposed D-band frequency doubler.

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The proposed frequency doubler is implemented in TSMC 65-nm CMOS process with ultra-thick metal (UTM), eight metal layers (M_1 to M_8), and a metal-insulator-metal (MIM) capacitor. Advanced Design Software (ADS) and Sonnet Software are used throughout the design for circuit and post-layout simulation. Fig. 3.18 depicts a schematic of the proposed D-band frequency doubler based on a one-stage push-push cascode topology. The bias point of the push-push structure is at Class-B to maximize the second-order transconductance. To further enhance the gain performance, the gain-boosting technique (red, thick transmission line) is adopted in the design. Furthermore, for maintaining the push-push structure well-functioned, the 180-degree phase difference generator is indispensable. The compensated Marchand balun is adopted in this design to realize broadband, low loss, and low amplitude and phase imbalance. The transmission lines and capacitors are used in input matching between the transistor and the Marchand balun, and output matching. The microstrip line is more favorable than the inductor to implement in the mm-wave design due to the self-resonant frequency limitation of inductance. Bypass capacitors and large capacitance capacitors are implemented as MIM capacitors, while the small ones involved in matching networks are realized using metal-oxide-metal capacitors, which are interdigital of metal 7 to metal 9. Fig. 3.19 shows the layout of the proposed frequency doubler with a total area of 0.262 mm^2 (0.4 mm × 0.655 mm) with all pads. The total DC power consumption of the proposed frequency doubler is 16.3 mW under 3 dBm input power.

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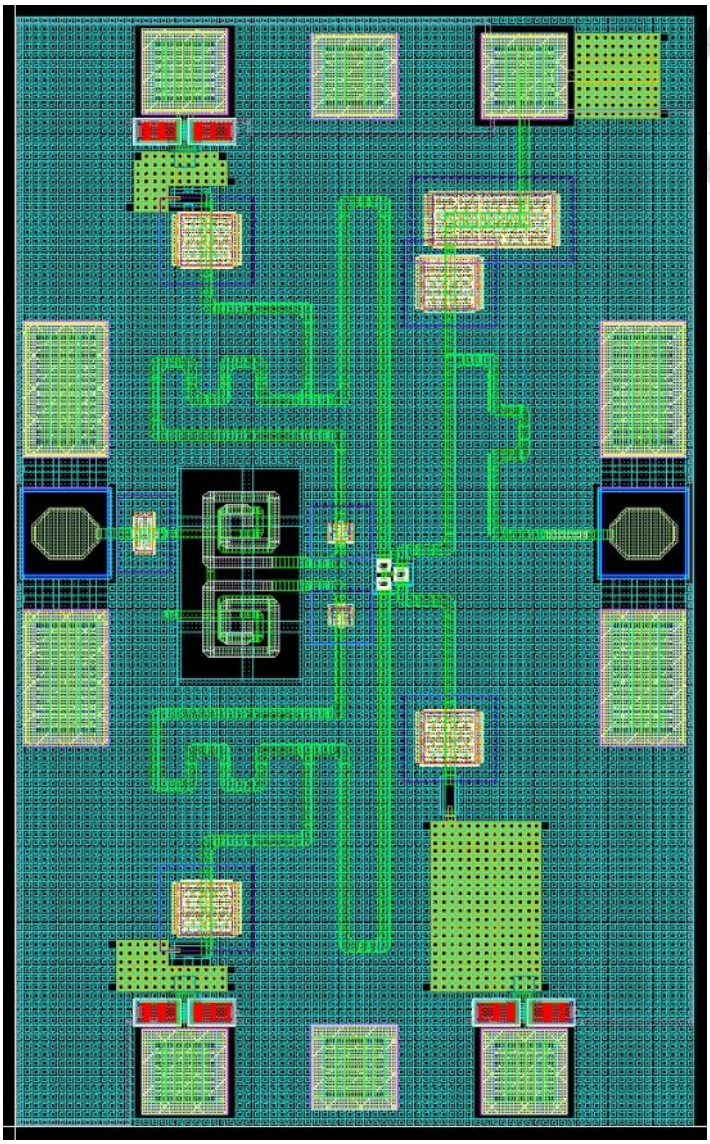

Fig. 3.19 Layout of the proposed D-band frequency doubler.

Fig. 3.20 illustrates the simulated conversion gain and output power versus frequency at an input power of 3 dBm; based on simulation results, the peak gain is -5.6 dB at 159 GHz, with a 3-dB bandwidth of 131 to 167 GHz, covering a total bandwidth of 36 GHz. Fig. 3.21 and Fig. 3.22 illustrate the simulated conversion gain and output power as a function of input power at the center input frequency of 74.5 GHz and the peak conversion gain input frequency of 79.5 GHz.

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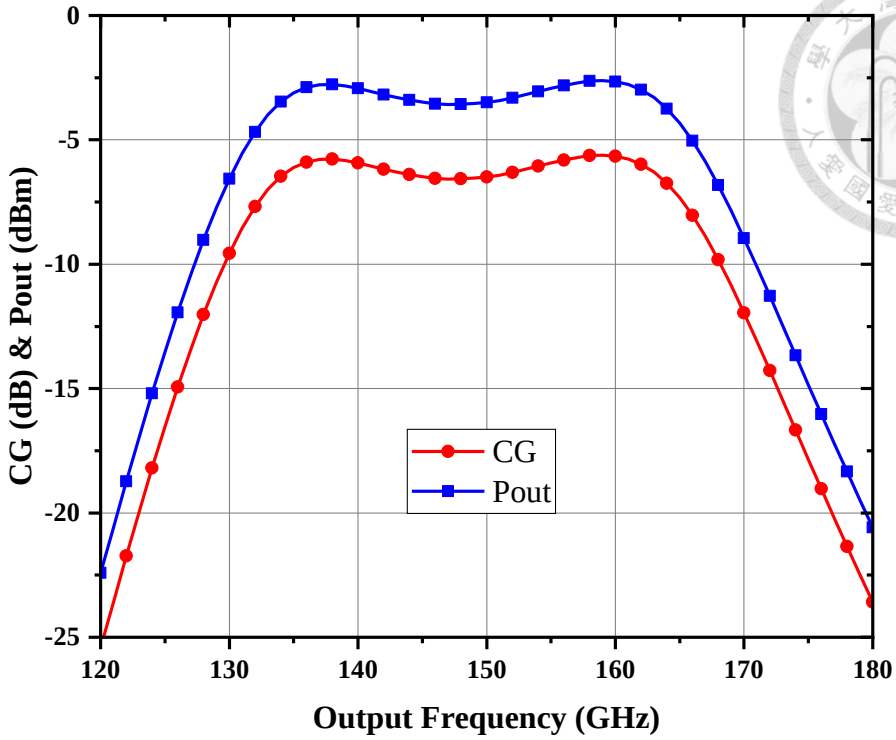

Fig. 3.20 The simulated conversion gain and output power versus output frequency at 3 dBm input power.

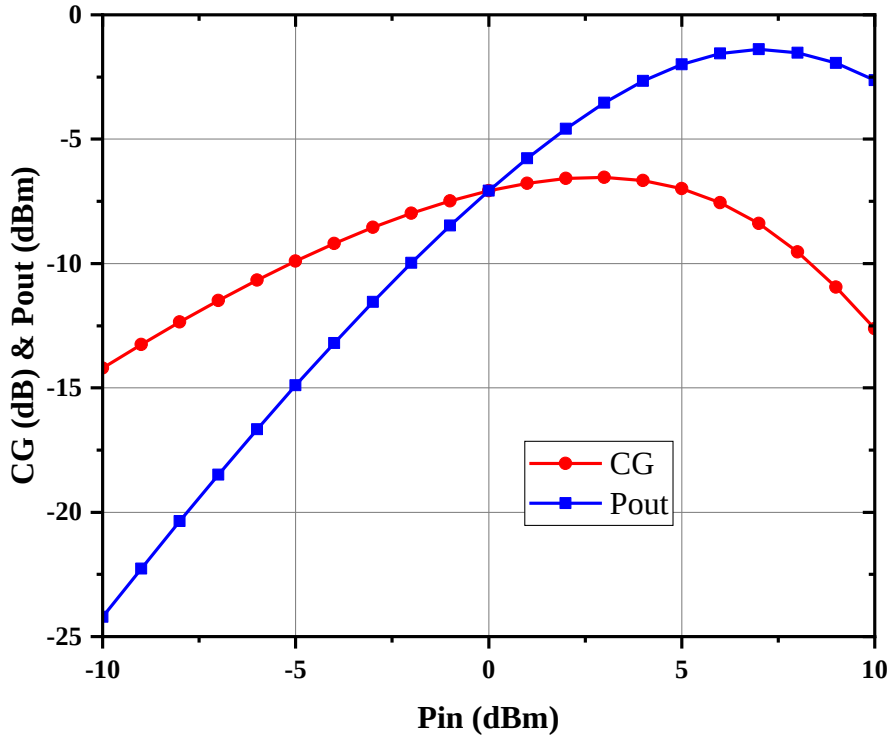

Fig. 3.21 The simulated conversion gain and output power versus input power at 74.5 GHz input frequency.

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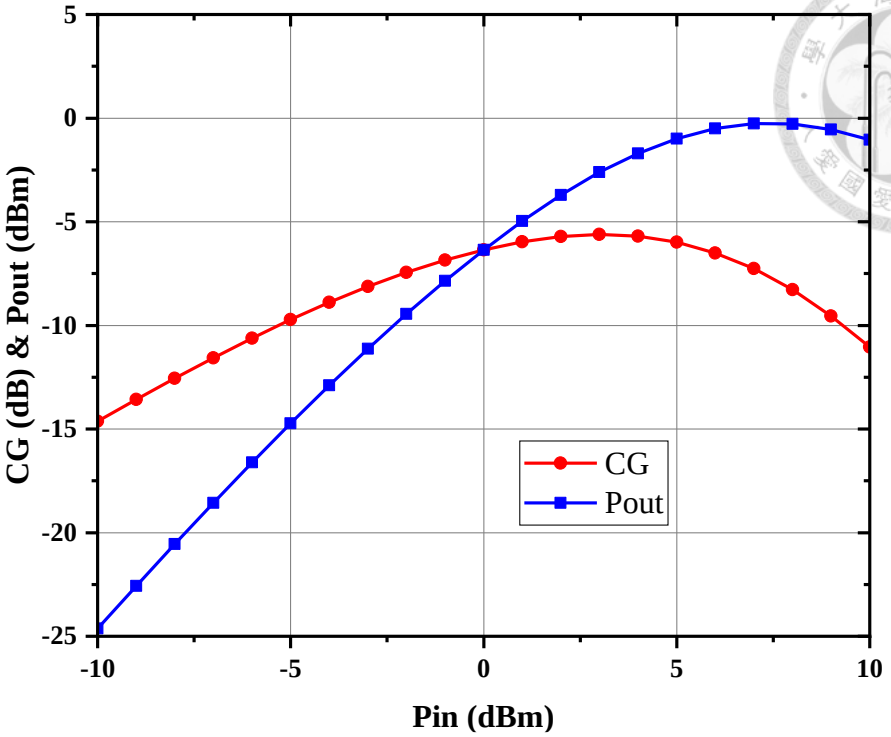

Fig. 3.22 The simulated conversion gain and output power versus input power at 79.5 GHz input frequency.

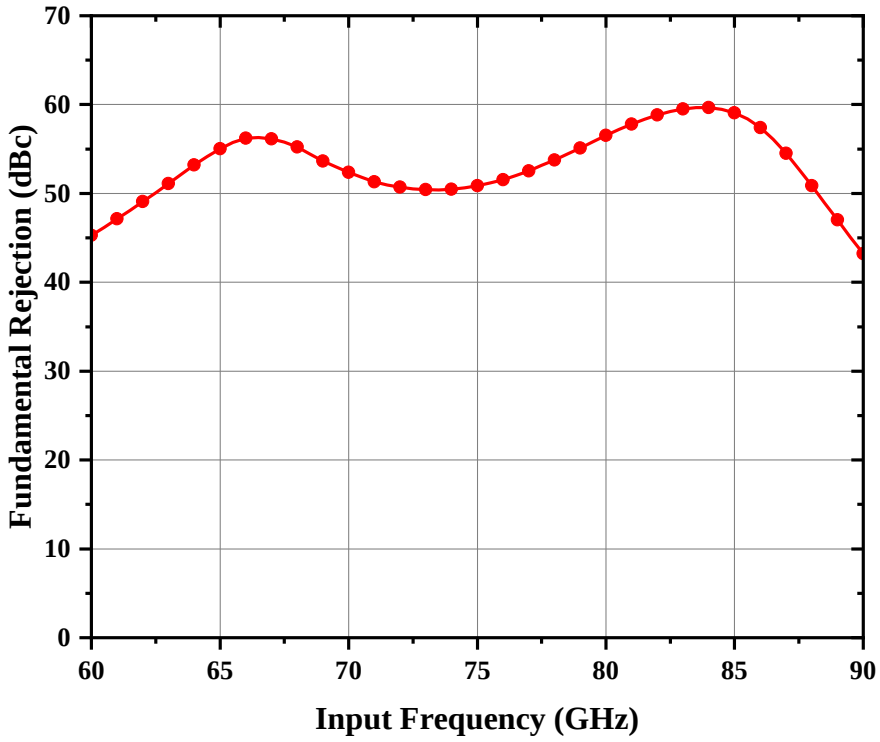

Fig. 3.23 The simulated fundamental rejection to input frequency at 3 dBm input power.

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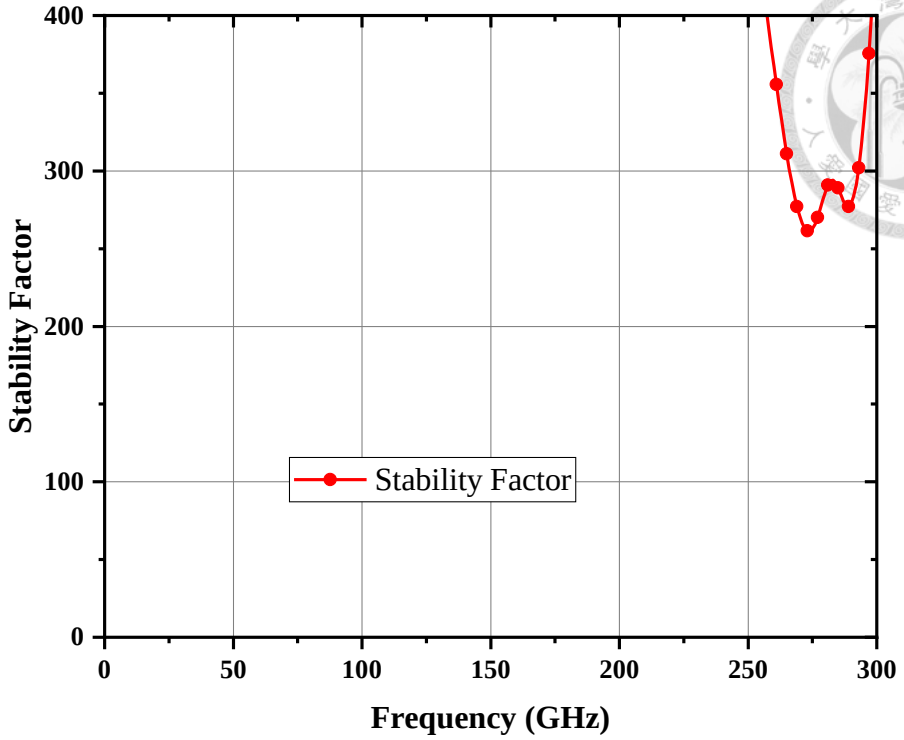

Fig. 3.24 The simulated stability factor of the proposed frequency doubler.

Fig. 3.23 shows the simulated fundamental rejection to input frequency at 3 dBm input power, which is greater than 50 dBc in the desired frequency bands. Fig. 3.24 depicts the overall simulated stability factor of the proposed frequency doubler and shows that it is greater than one at all frequencies.

3.3 Measurement Results

The proposed D-band frequency doubler is fabricated in the 65-nm CMOS process. Fig. 3.25 shows the chip micrograph of the proposed frequency doubler; the total area with pads is 0.262 mm^2 (0.4 mm × 0.655 mm). The input power is given from the N5260-60003 67 GHz to 110 GHz waveguide T/R module with attenuator, through the WR-10 waveguide, and an RF probe injected into the circuit. The output signal is transmitted through the WR-6 waveguide to the PM5 power meter. All measurement results were

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performed by on-wafer probing using GSG RF probe and GGB DC probe.

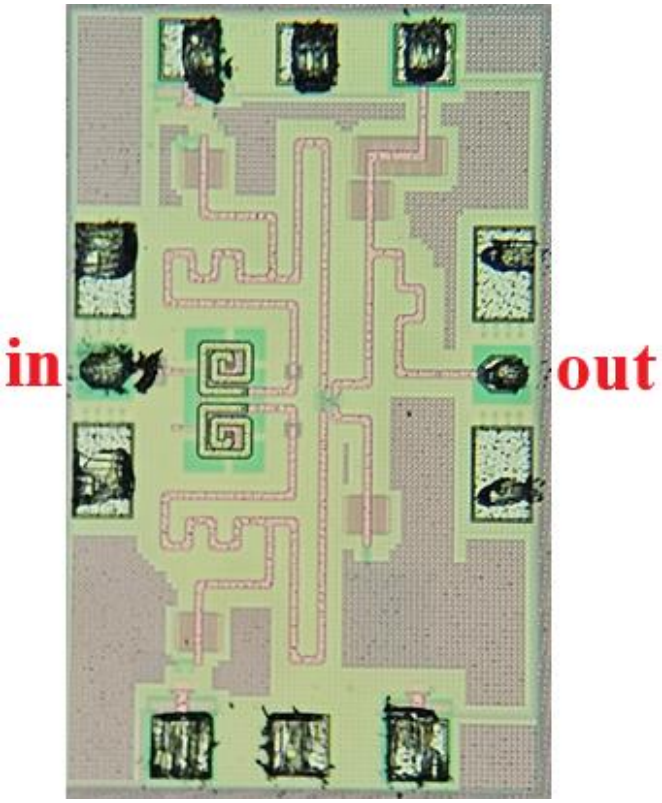

Fig. 3.25 The chip micrograph of the doubler with a chip size of 0.262 mm^2.

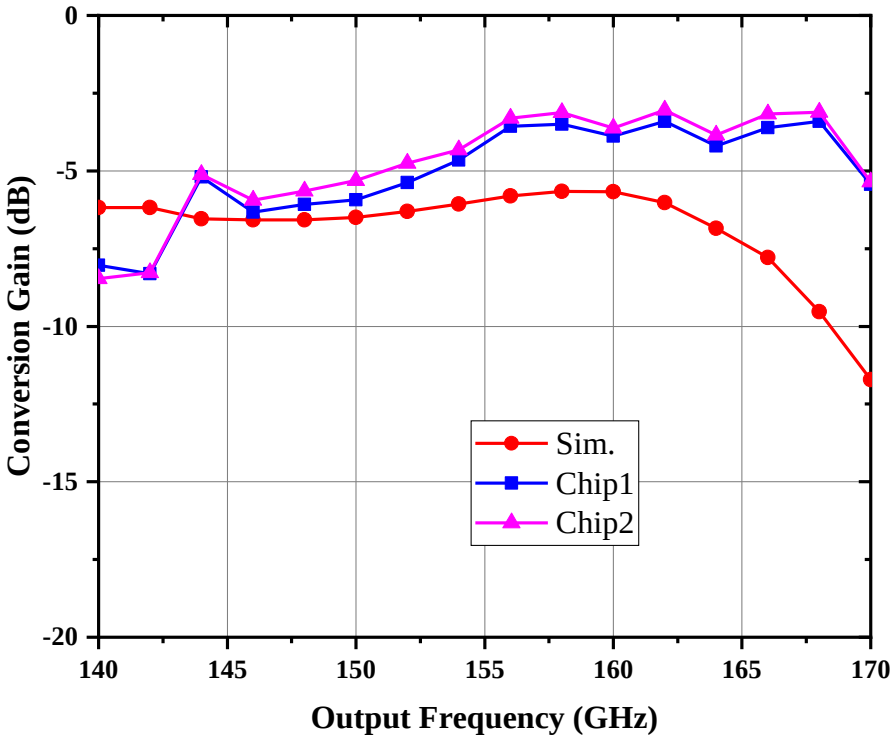

Fig. 3.26 The measured and simulated conversion gain.

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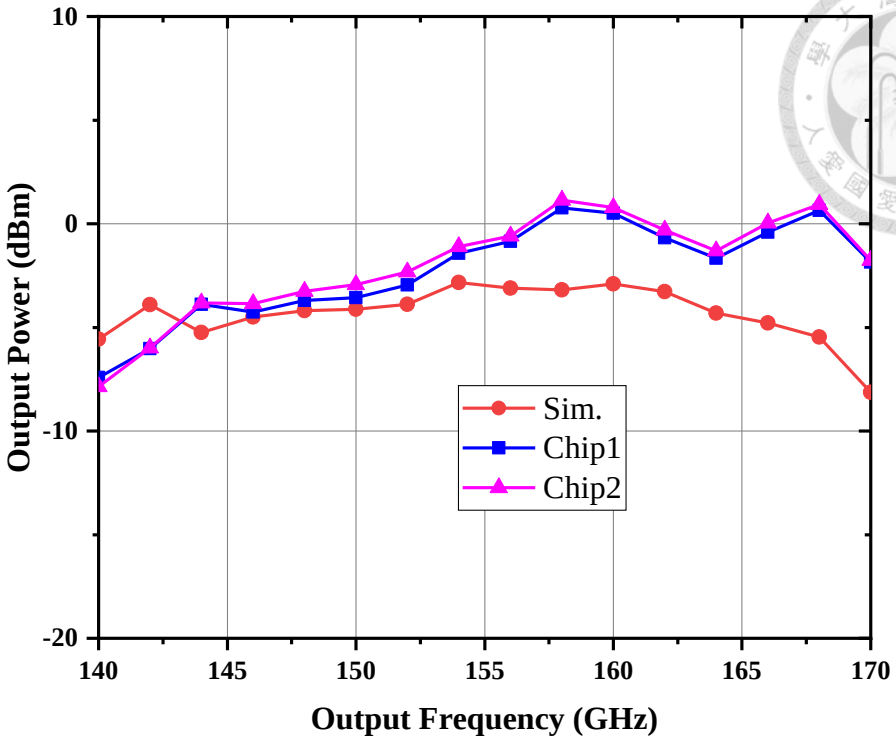

Fig. 3.27 The measured and simulated output power.

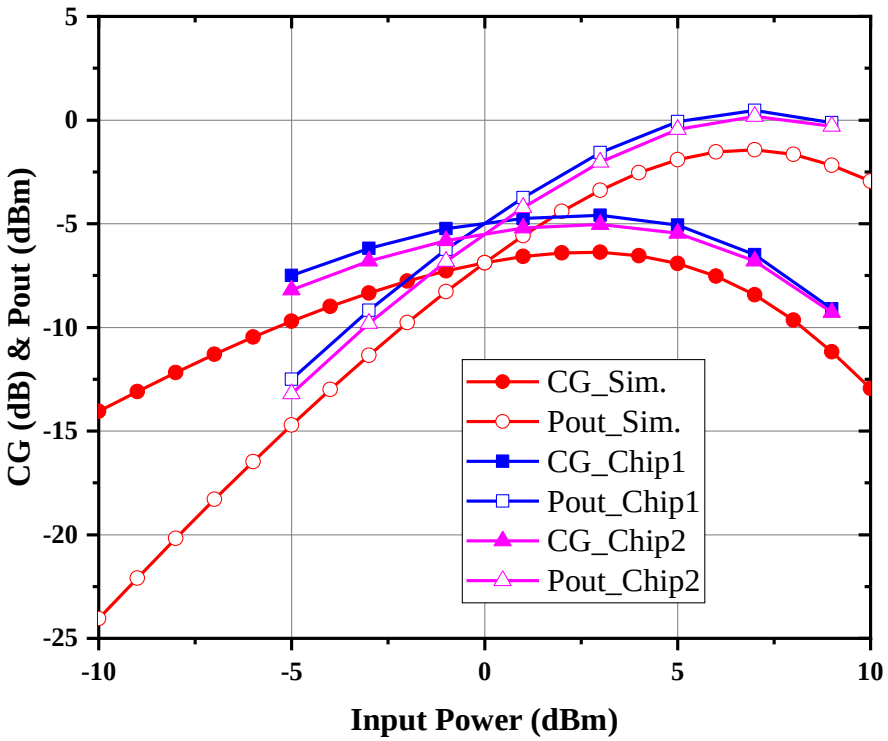

Fig. 3.28 The measured and simulated conversion gain and output power versus input power at 75 GHz

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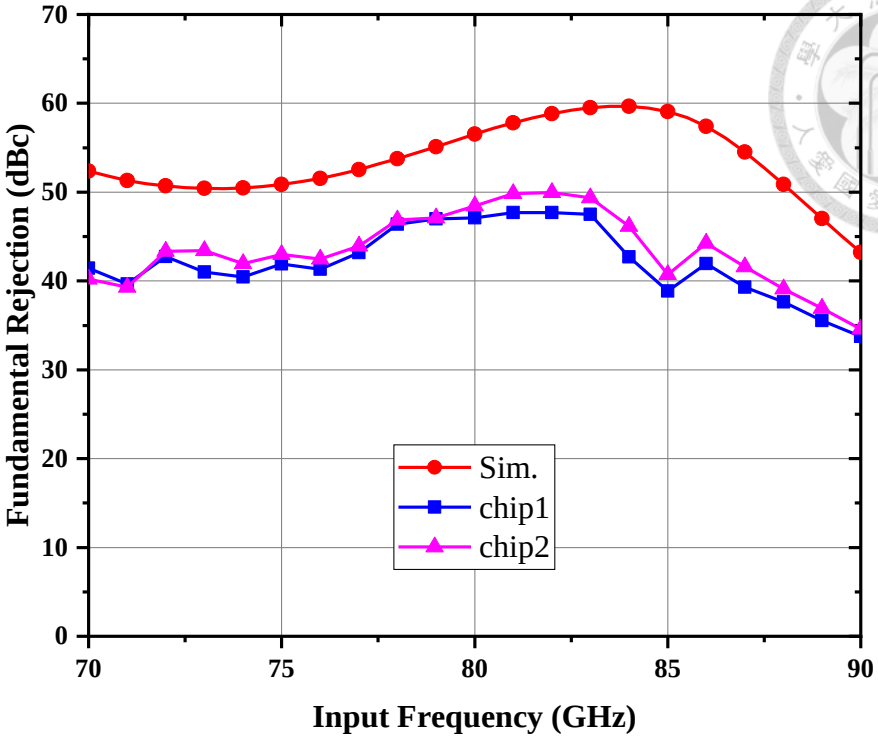

Fig. 3.29 The measured and simulated fundamental rejection.

Fig. 3.26 demonstrates the measured and simulated conversion gain of the proposed D-band frequency doubler. The peak conversion is -3.5 dB, which occurs at 158 GHz, and the 3-dB bandwidth covers from 143 GHz to 170 GHz. Fig. 3.27 depicts the measured and simulated output power of the proposed frequency doubler. The peak output power is 0.76 dBm at 158 GHz with 4.3 dBm input power. The overall trend of the measurement results is similar to the simulation; however, the high-frequency parts are not aligned well with the measurement results. To further investigate the phenomenon, the troubleshooting is discussed in Section 3.4. Fig. 3.28 demonstrates the measured and simulated conversion gain and output power versus input power at 75 GHz. The peak conversion gain and output power occur at 3 dBm and 7 dBm input power, respectively. As observed in the previous two figures, the measured conversion gain and output power performance are slightly higher than the simulation results. Fig. 3.29 shows the measured and simulated

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fundamental rejection performance, which is greater than 41.3 dBc within the desired frequency bandwidth.

3.4 Troubleshooting and Discussion

As discussed in Section 2.4.3, the Nch+EM model is an effective way to figure out the unmatched simulation and measured results. Fig. 3.30 and Fig. 3.31 depict the top view and bottom view of the NCH + EM simulation setting. The port is excitation at the circled red area. The three ports in top view are regarded as the source, gate, and drain of the new device. The three output ports of the bottom view are connected to the NCH transistor, respectively, forming a new NCH+EM device. Fig. 3.32 and Fig. 3.33 show the re-simulation results with the new NCH+EM device compared to the original simulation and measurement results. It is obvious that the results at the frequency of 150 GHz to 170 GHz become aligned very well after changing the device model. Similar results are depicted in Fig. 3.34 and Fig. 3.35, the conversion gain and output power versus input power at 75 GHz show good agreement after changing the transistor model. As demonstrated in Fig. 3.36, the trend in the fundamental rejection performance remains unchanged.

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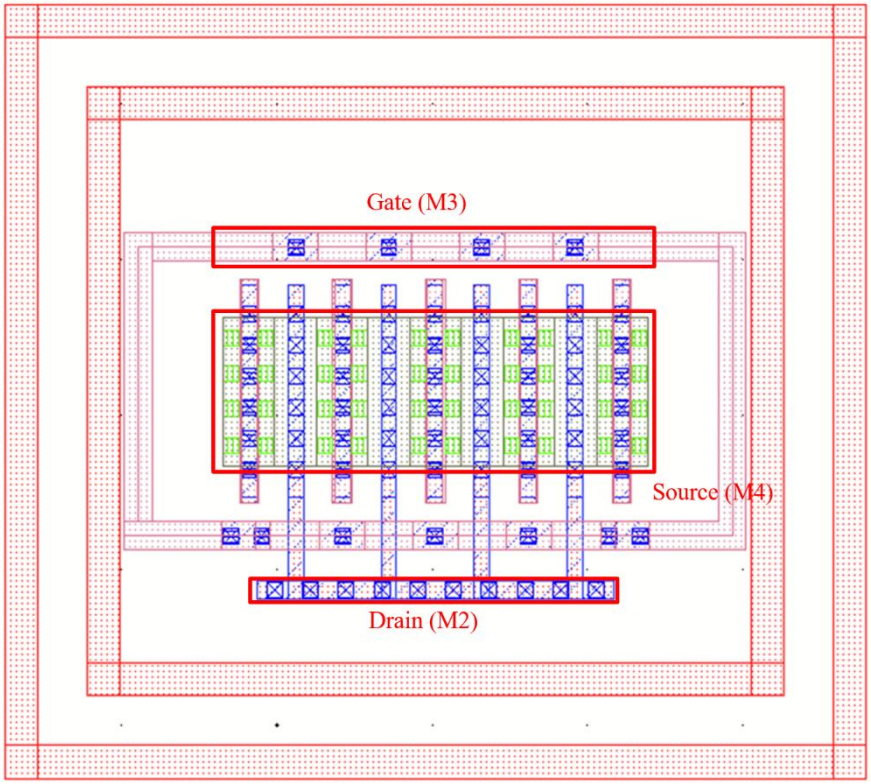

Fig. 3.30 Top view of NCH+EM simulation setting.

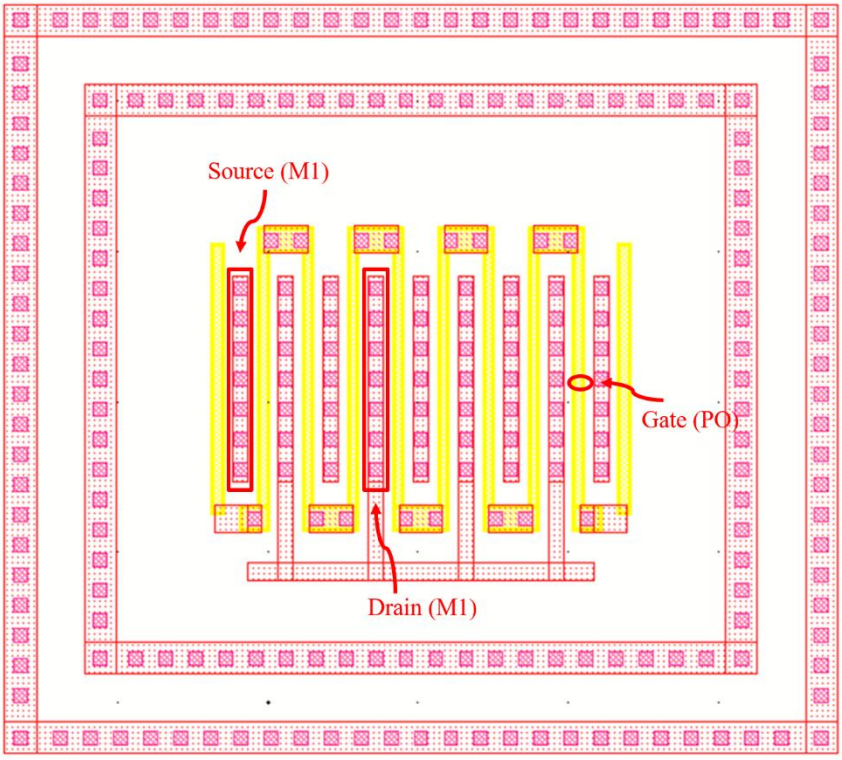

Fig. 3.31 Bottom view of NCH+EM simulation setting.

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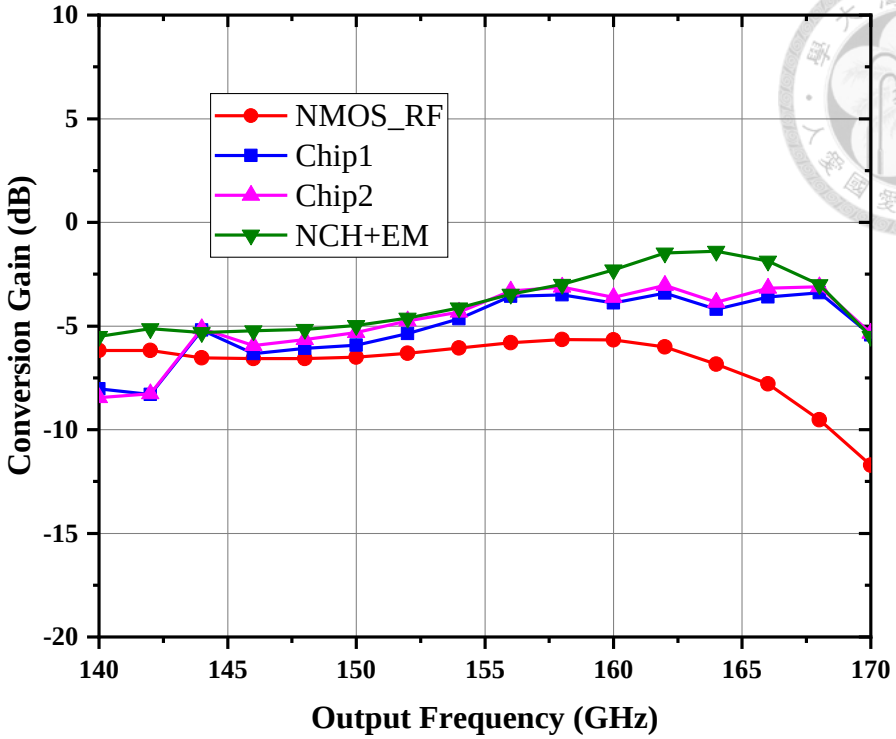

Fig. 3.32 The conversion gain of measurement results and simulation under different transistor models.

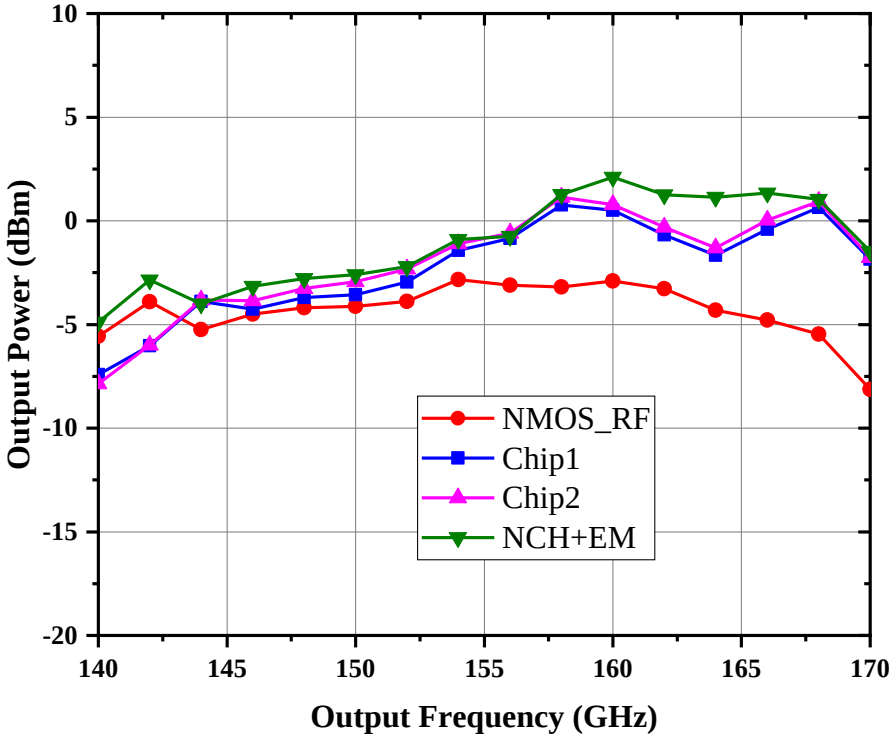

Fig. 3.33 The output power of measurement results and simulation under different transistor models.

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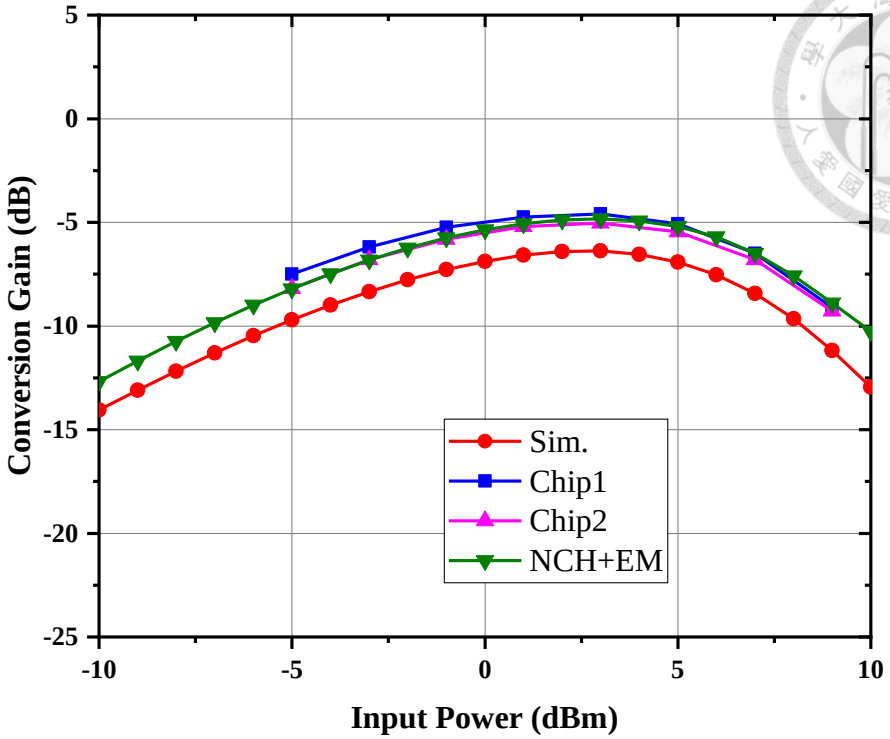

Fig. 3.34 The conversion gain of measurement results and simulation under different transistor models at 75 GHz.

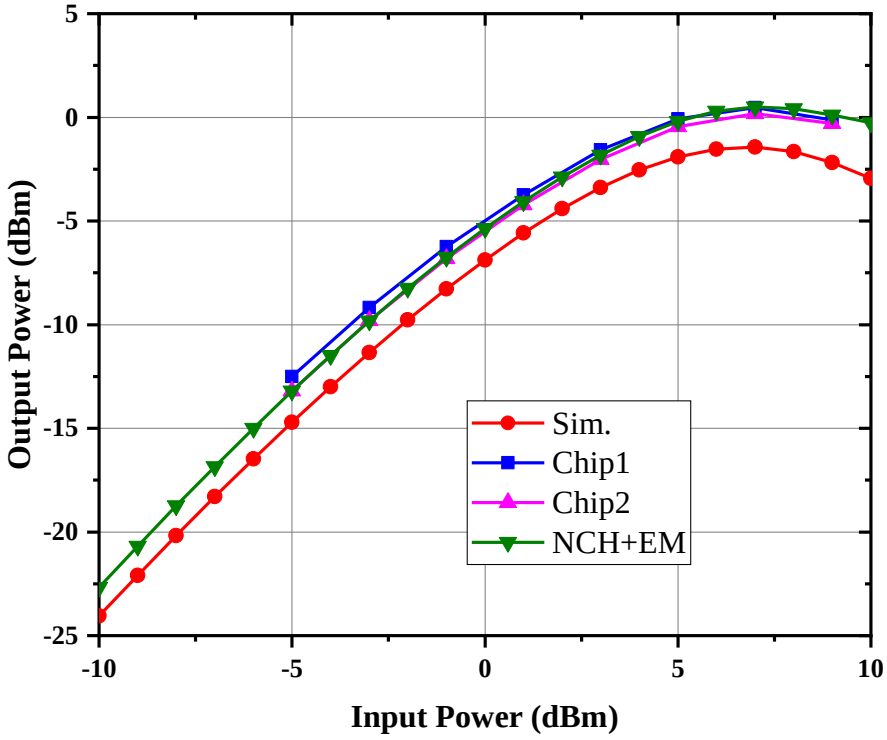

Fig. 3.35 The output power of measurement results and simulation under different transistor models at 75 GHz.

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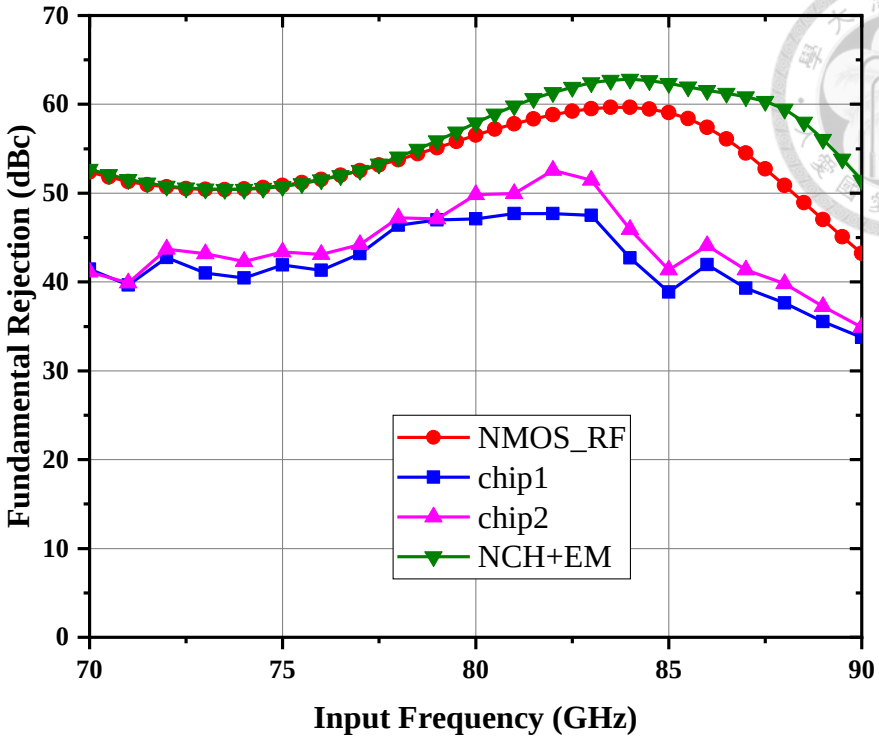

Fig. 3.36 The fundamental rejection of measurement results and simulation under different transistor models.

3.5 Summary

In this chapter, a D-band frequency doubler designed for a D-band local oscillation chain, which is fabricated in the 65-nm CMOS process, is presented. To achieve a better conversion gain and rejection performance, a well-designed low-amplitude and low-phased difference compensated Marchand balun is designed. For the sake of increasing output power and conversion gain, a common gate transistor is connected after the push-push structure, forming a cascode topology. Moreover, a gain-boosting technique, which is realized in the transmission line, is adopted in this design to further enhance the conversion gain performance. With 16.3 mW of DC power consumption under 3 dBm input power, the measurement results showed that the 3-dB bandwidth covers from 143 GHz to 170 GHz, and with a peak conversion gain of -3.5 dB at 158 GHz. Also, the peak output power is 0.76 dBm at 158 GHz with 4.3 dBm input power. The fundamental

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rejection is better than 41.3 dBc in the entire frequency bandwidth. The total chip size, including all pads, is 0.262 mm2 (0.4 mm x 0.655 mm). Table 3.2 summarizes the recently published D-band frequency doubler. Furthermore, re-simulation of the RF device has also been done in this work, which makes the simulation and measurement results of the proposed doubler show good alignment in the desired frequency bands.

Table 3.2 Performance comparison of recently published frequency doubler.

Ref.	**Process**	**3-dB Bandwidth (GHz)**	**Peak CG (dB)**	**P_{out}@P_{in} (dBm)**	**FR (dBc)**	**P_{dc} (mW)**	**Area (mm^2)**
[26]	65-nm CMOS	106-128	0	-2.6@0	N/A	23	0.27
[27]	65-nm CMOS	95-150	-8	3@11	> 30	19.2~22.8	0.24
[28]	90-nm CMOS	158-204	-7.8	2.2@10	N/A	88.8	0.41
[29]	28-nm CMOS	126-146	-4.5	0.5@5	> 34	12	0.49
[30]	22-nm FDSOI CMOS	125-145	-5.5	4.1@11.7	N/A	24.7	0.326
[31]	45-nm SOI CMOS	135-160	-3	3.5@7	N/A	25	0.44
[47]	90-nm CMOS	156-196	-11.9	-1.9@10	> 10.9	18	0.315
[48]	40-nm CMOS	154-206	-17.1	-9.7@8	N/A	38.7	0.32
[49]	45-nm SOI CMOS	170-190	-6.4	0@4	N/A	39	0.34
This Work	65-nm CMOS	143~170	-3.5	0.76@4.3	> 41.3	16.3	0.262

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Chapter 4 Design of a DC to D-band Single-Pole Single-Throw Switch in 90-nm CMOS Process

4.1 Introduction

In recent years, due to the progress of wireless communication, the demand for mm-Wave transceivers has increased. With the advantages of high-frequency bandwidth, the 6G enables a high data transmission rate and nearly zero latency, which can support many applications such as artificial intelligence and immersive experiences. However, it is also the most challenging specification of the 6G transceiver system to cover from the low frequency bands to sub-THz. Traditional multi-band solutions frequently require intricate band switching involving multiple switches or sub-modules. While these systems can enhance performance, they also present challenges such as complex control logic, varied signal paths, and considerable losses. As a result, an ultra-wideband switch is an effective solution due to its exceptional bandwidth performance, which covers multiple frequency bands and reduces the number of components required in control circuits. Its simple structure allows for integration into advanced processes, particularly in applications that do not necessitate frequency band switching, such as high-bandwidth scanning modules, continuous spectrum detectors, and single-channel broadband transceivers. By achieving multi-frequency band coverage with a single switch, it minimizes signal paths and reduces losses, thereby enhancing the reliability and performance of the overall system. Table 4.1 depicts the design goals of the proposed DC to D-band SPST switch.

Chapter 4 will demonstrate the proposed DC to D-band SPST switch. Chapter 4.2 introduces the design of the proposed switch, which is based on several series and shunt transistors, which can minimize the area of the switch. For the purpose of enhancing the

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insertion loss, a body-floating technique is adopted. Chapter 4.3 shows the measured results of the proposed SPST switch. Chapter 4.4 summarizes this work.

In this work, based on experimental results, the bandwidth covering from DC to 140 GHz has the insertion loss lower than 3.3 dB, the return loss is greater than 14 dB, and the isolation is better than 22 dB. Further extend the covering bands to 170 GHz, with the insertion loss lower than 3.6 dB, the return loss is greater than 9 dB, and the isolation is better than 18.5 dB. An output-referred 1-dB compression point is located at 10 to 11 dBm at 75 to 110 GHz. The core area is only 980 μm^2.

Table 4.1 The design goals of the proposed DC to D-band SPST switch.

	Specification
Process	90-nm CMOS process
Frequency (GHz)	DC-140
Insertion Loss (dB)	< 3.5
Return Loss (dB)	> 10
Isolation (dB)	> 20
$\boldsymbol{IP_{1dB}}$ **(dBm)**	> 10

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4.2 The Design of SPST Switch

4.2.1 DC Biasing and Device Size Selection

The basic operating principles of the RF MOSFET switch are based on the on-resistance (R_{on}) and C_{off} characteristics of the transistors, which significantly influence the performance of the switch in terms of insertion loss, return loss, and isolation. Meanwhile, the R_{on} and C_{off} are mainly determined by following several factors, including the size of the transistor, the gate-to-source bias, and the threshold voltage. Among these factors, unlike other advanced processes that offer a super-low-VT option (SLVT), the threshold voltage in this process is typically fixed. As a result, this section will focus on selecting the device size and DC biasing point. Fig. 4.1 shows the schematic of a series transistor and a shunt transistor, which is the most basic topology in the millimeter-wave switch design.

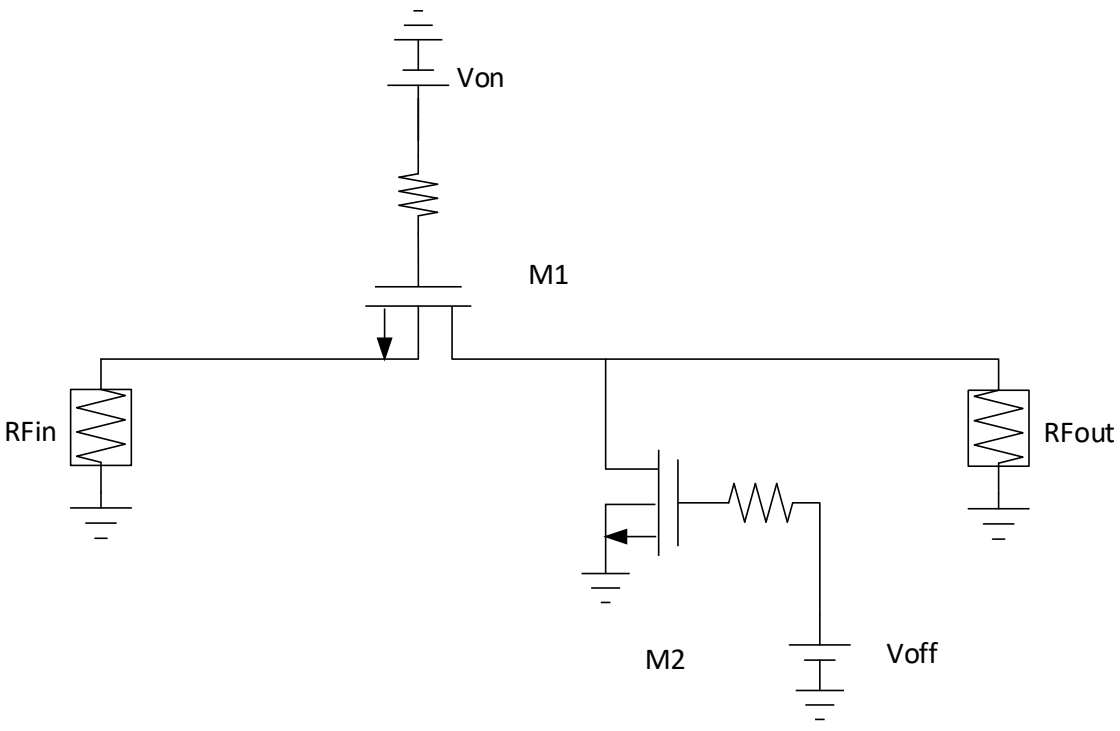

Fig. 4.1 The schematic of a series and a shunt transistor.

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Based on the schematic shown in Fig. 4.1, assuming the nMOSFET transistors can be simplified to R_{on} and C_{off} when in active and cut-off regions. The insertion loss in the ON-mode (V_{on} = 1.2 V, V_{off} = 0 V) can be expressed as [36, 50]:

$$\begin{aligned}\begin{bmatrix} A & B \\ C & D \end{bmatrix} &= \begin{bmatrix} 1 & R_{on} \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ C_{off} & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1 + R_{on} j\omega C_{off} & R_{on} \\ C_{off} & 1 \end{bmatrix}\end{aligned} \tag{4.1}$$

The insertion loss of the switch can be given by:

$$\begin{aligned} IL &= -20 \log |S_{21}| \\ &= -20 \log \left| \frac{2}{A + B/Z_0 + CZ_0 + D} \right| \end{aligned} \tag{4.2}$$

Therefore, the insertion loss can be derived as:

$$IL = 10 \log \left\{ \left(1 + \frac{R_{on}}{2Z_0} \right)^2 + \left[\pi f C_{off} (R_{on} + Z_0) \right]^2 \right\} \tag{4.3}$$

where R_{on} is the channel resistance of a series transistor M_1, and C_{off} represents the capacitance of the parallel transistor M_2. Also, the channel resistance, $R_{on,}$ can be expressed as:

$$R_{on} = \frac{1}{\mu C_{ox} (W/L)(V_{GS} - V_{th})} \tag{4.4}$$

where μ is the carrier mobility in the channel; C_{ox} is the unit capacitance of the gate oxide layer; W and L represent the channel width and length; V_{GS} and V_{th} are the gate-to-source bias and threshold voltage. As a result, the control voltage is set to 1.2 V, which is the maximum tolerable of the transistor, to decrease the R_{on}, and thus, minimize the

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insertion loss.

There are two cases of topology type in discussion, the series-type and the shunt-type. For a series-type transistor, M_1 in Fig. 4.1, a smaller transistor size having a small C_{off}, and thus achieving better isolation, while the larger R_{on} results in higher insertion loss. As the size of the device increases, the smaller R_{on} can contribute to a smaller insertion loss, while a larger C_{off} leads to worse isolation performance. As for the shunt-type transistor, M_2 in Fig. 4.1, the increase of the transistor size can improve the isolation of the overall switch circuit due to a smaller R_{on}, while deteriorating the insertion loss performance caused by a larger parasitic capacitance C_{off}. Table 4.2 summarizes the trade-off study between device size and overall switch performance. As a result, the goal of device selection is to find a device size to achieve balanced performance in both on- and off-states of the switch.

Fig. 4.2 shows the simulated R_{on} and C_{off} under different total gate widths. After the trade-off between two key factors, the final series-type transistor size is selected as 2 μm x 8 fingers, and the shunt-type transistor size is selected as 1 μm x 12 fingers, which is slightly smaller than the series-type for a better insertion loss performance. Fig. 4.3shows the performance comparison of one and two shunt transistors; it is obvious that adding one more shunt transistor can greatly improve the isolation performance while slightly sacrificing the insertion loss performance at high frequency. Fig. 4.4 demonstrates the overall schematic of the proposed SPST switch. The transistor M_4, which is parallel with resistor R_1, can further improve the isolation of the switch during the off-state. When the switch is off, the transistor M_4 is active, bypassing the signal to the ground and thus improving the isolation of the switch. As shown in Fig. 4.5, the simulated isolation is approximately 3-dB better in the entire frequency band with the parallel transistor M_4. However, the on-state performance would have slightly degraded due to the M_4. Fig. 4.6

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illustrates the simulated insertion loss and return loss with and without the parallel transistor M_4. It is observed that the insertion loss increases by 0.2 dB, and the return loss worsens by 2 dB.

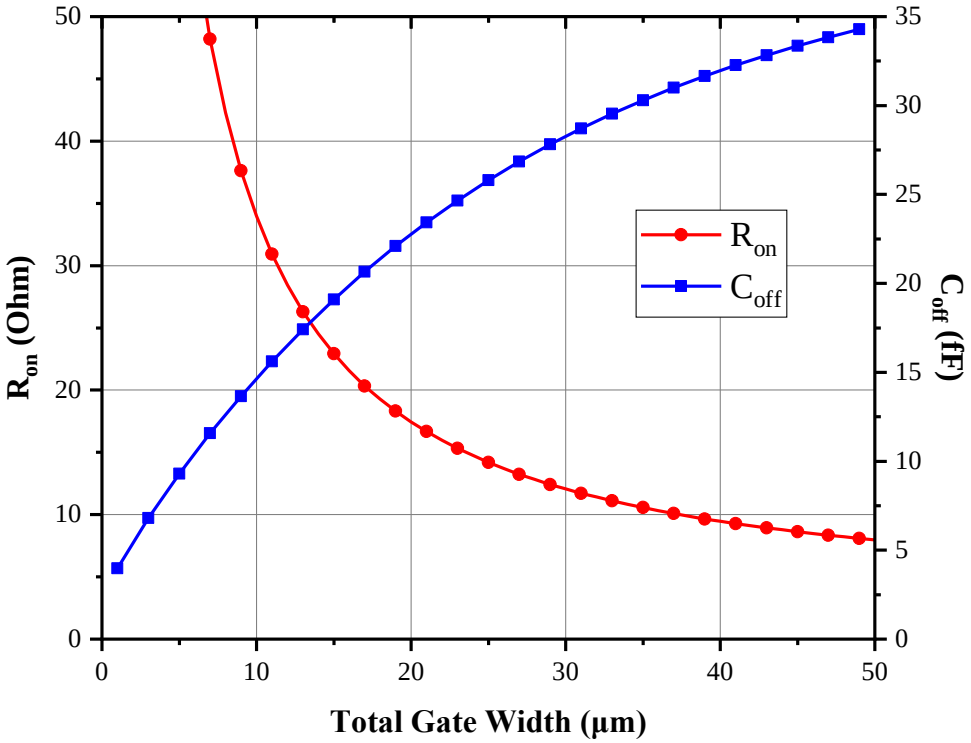

Fig. 4.2 The simulated R_{on} and C_{off} under different transistor sizes.

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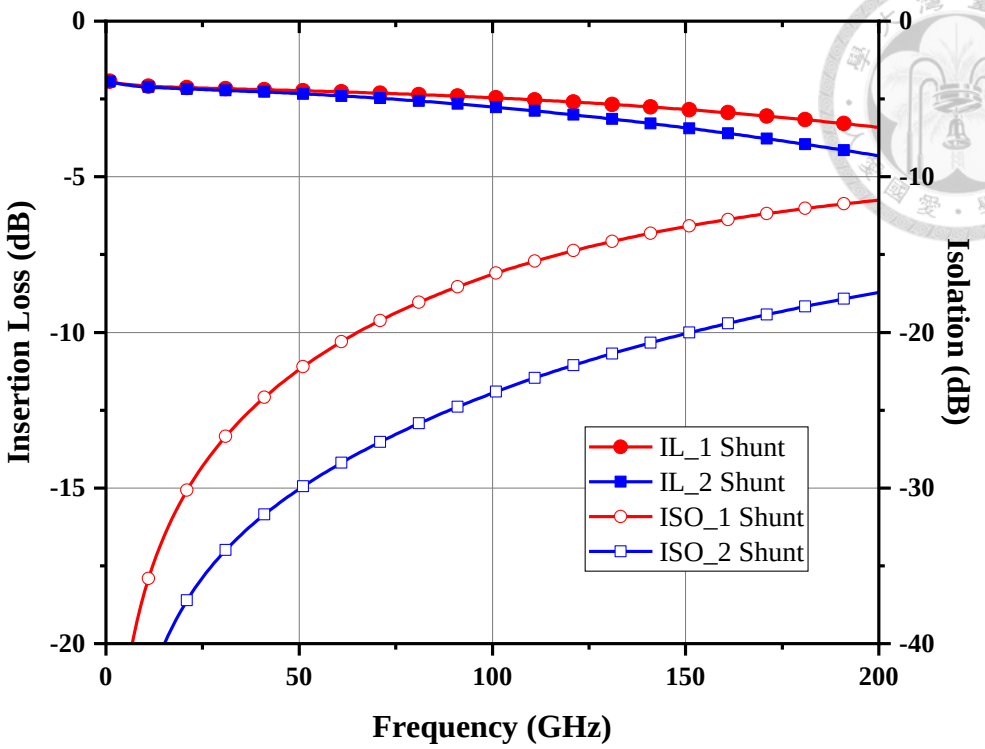

Fig. 4.3 The performance comparison of one and two shunt transistors.

Table 4.2 Trade-off study of the device size to the overall switch performance.

Type	Device Size	Insertion Loss	Isolation
Series	↑	☺	☹
	↓	☹	☺
Shunt	↑	☹	☺
	↓	☺	☹

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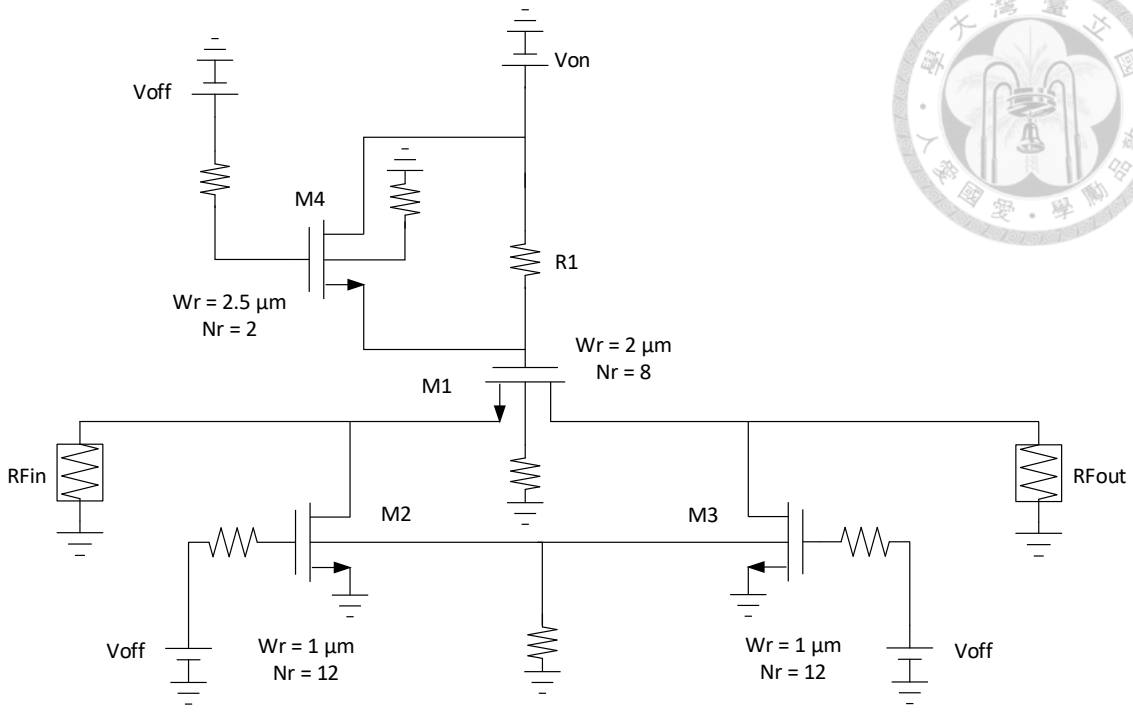

Fig. 4.4 The schematic of the proposed SPST switch.

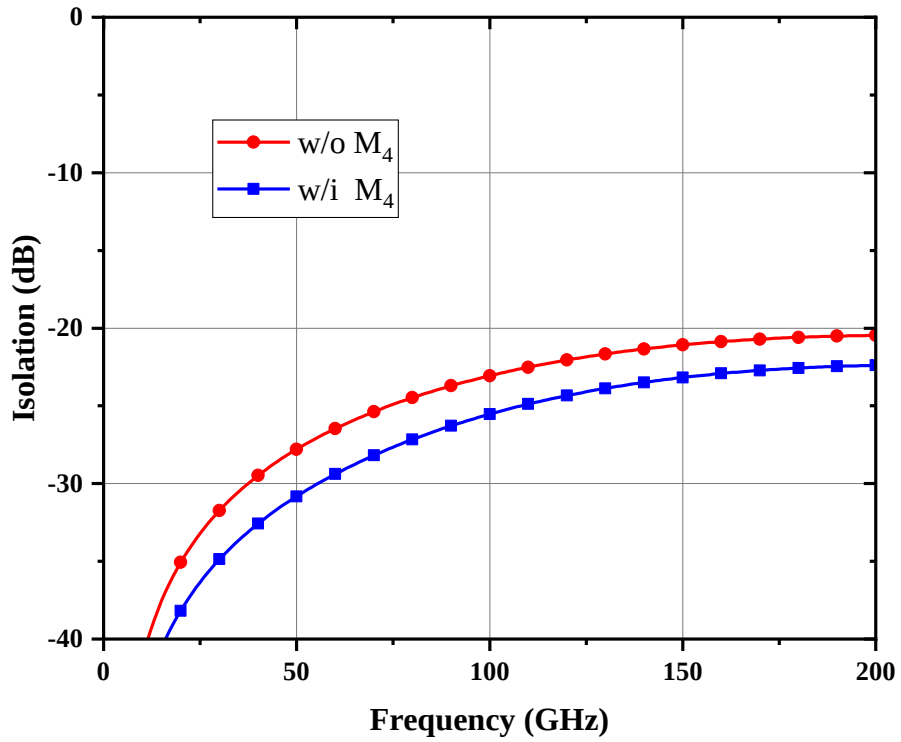

Fig. 4.5 The simulated isolation with and without the M_4 transistor shown in Fig. 4.4.

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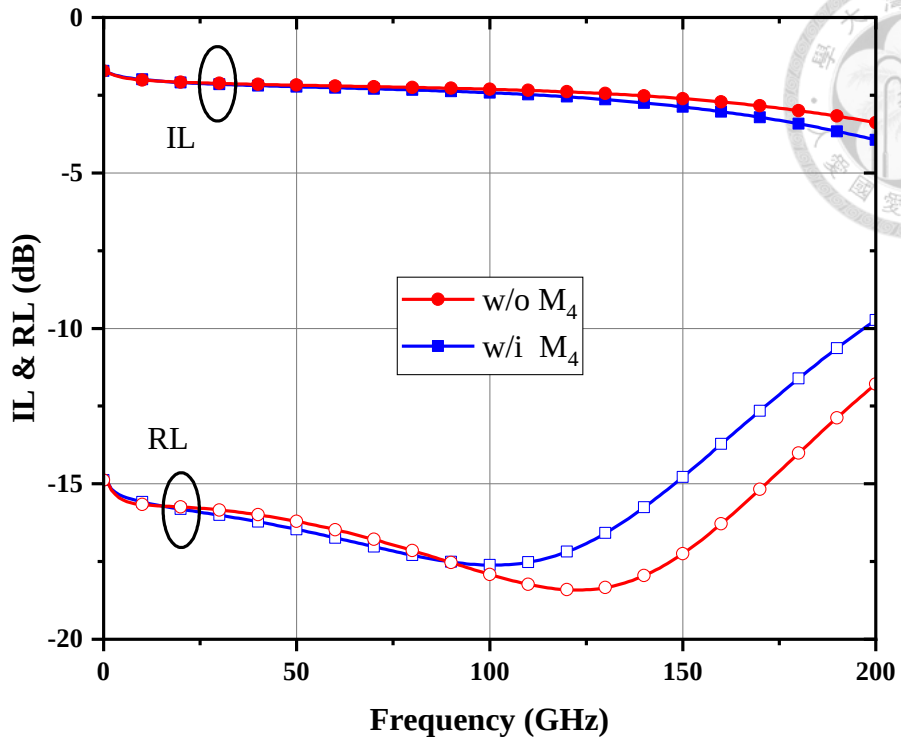

Fig. 4.6 The simulated IL and RL with and without the M_4 transistor shown in Fig. 4.4.

4.2.2 Body-Floating Technique

The body-floating is commonly used in millimeter-wave mixers, frequency doublers, and switches to improve the insertion loss and conversion gain performance. The cross-section of the NMOS transistor with the body-floating technique is shown in Fig. 4.7. In order to further investigate the mechanism of this technique, the schematic and equivalent small-signal model of an NMOS transistor is demonstrated in Fig. 4.8, where C_{gb}, C_{db}, and C_{sb} represent the gate-to-body, drain-to-body, and source-to-body capacitances. Fig. 4.9 and Fig. 4.10 compare the situation of the body directly connected to the ground and the situation of the body connected to the ground via a resistor, which is the body-floating technique. In Fig. 4.10, the influence of C_{gb}, C_{db}, and C_{sb} can be neglected if the value of the resistor is large enough. And thus, the parasitic effect can be reduced, which has a significant impact on high-frequency performance. Fig. 4.11 illustrates the simulated

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insertion loss and return loss of the proposed switch with and without the body-floating technique. Based on the simulation results, it is obvious that the insertion loss became better with the body-floating resistor, and as the frequency increases, the effect becomes more significant. It improves 0.3 dB at 75 GHz, 0.5 dB at 140 GHz, and even 0.7 dB at 170 GHz. Simultaneously, the performance of return loss remains well after adding a body-floating transistor. Fig. 4.12 shows the simulated isolation with and without a body-floating resistor, which also barely degrades after applying the body-floating technique. In Fig. 4.13, the large-signal simulation results of the proposed switch at 140 GHz with and without the body-floating technique are demonstrated. It can be observed that although the IP_{1dB} remains at the same level, when the input signal increases, the unlinearity phenomenon is much better than that without applying the body-floating technique [51, 52].

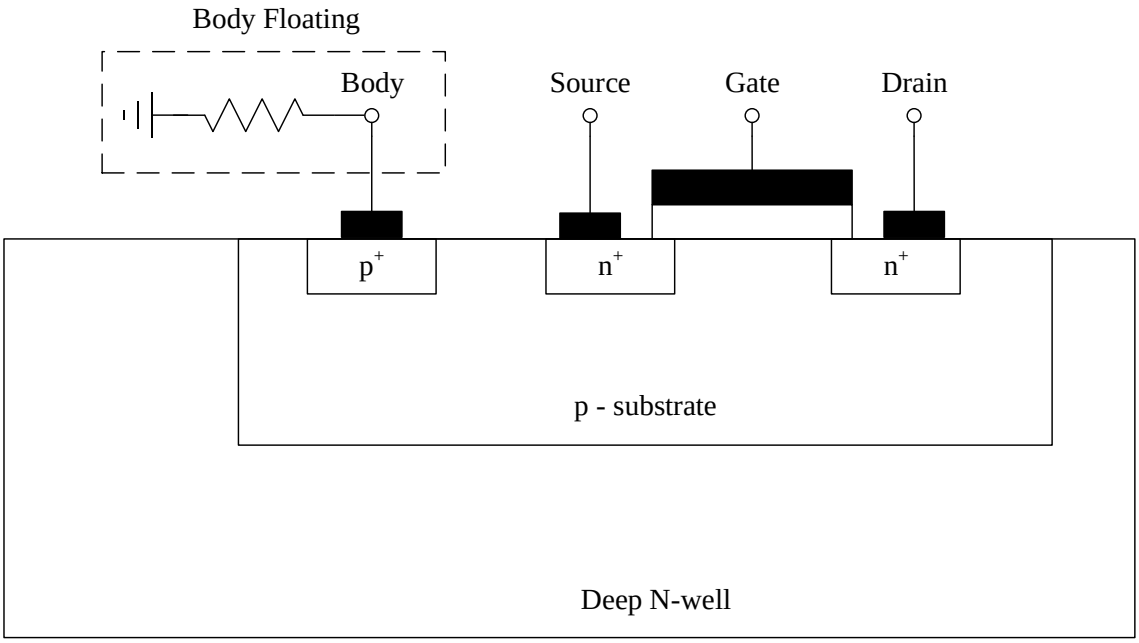

Fig. 4.7 The cross-section of an NMOS transistor with body-floating.

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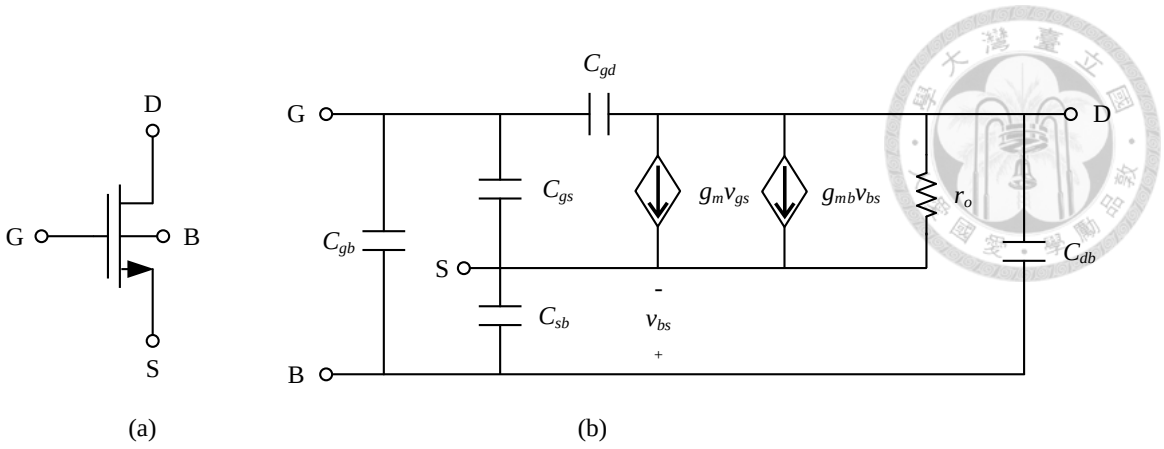

Fig. 4.8 NMOS transistor (a) schematic and (b) equivalent small-signal circuit model.

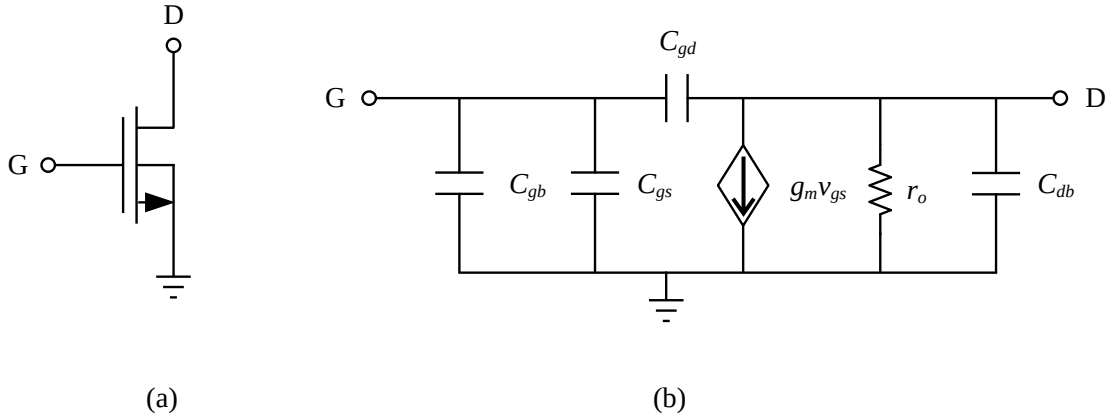

Fig. 4.9 The (a) schematic and (b) equivalent small-signal model of body grounding.

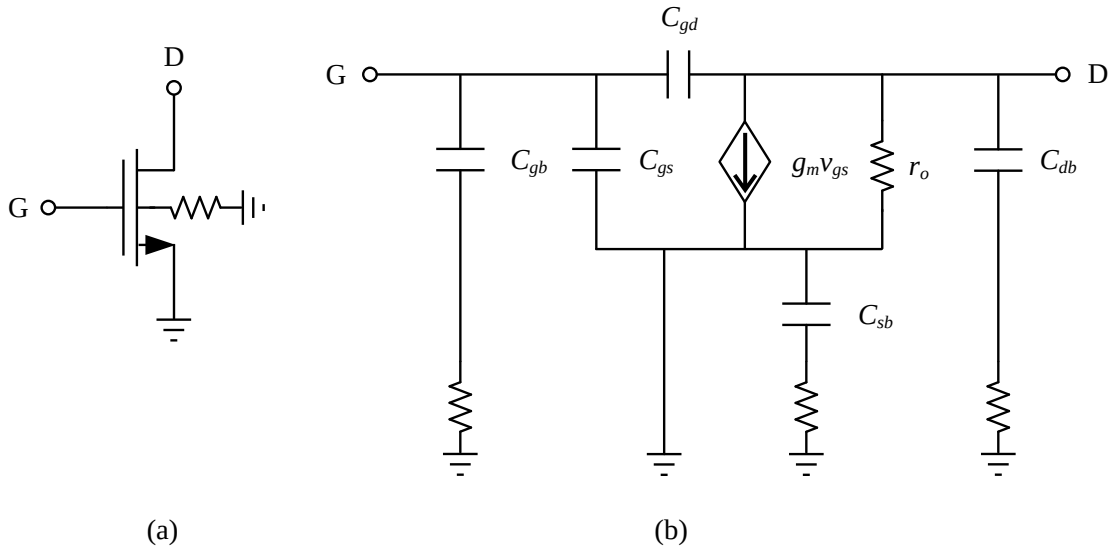

Fig. 4.10 The (a) schematic and (b) equivalent small-signal model of the body-floating.

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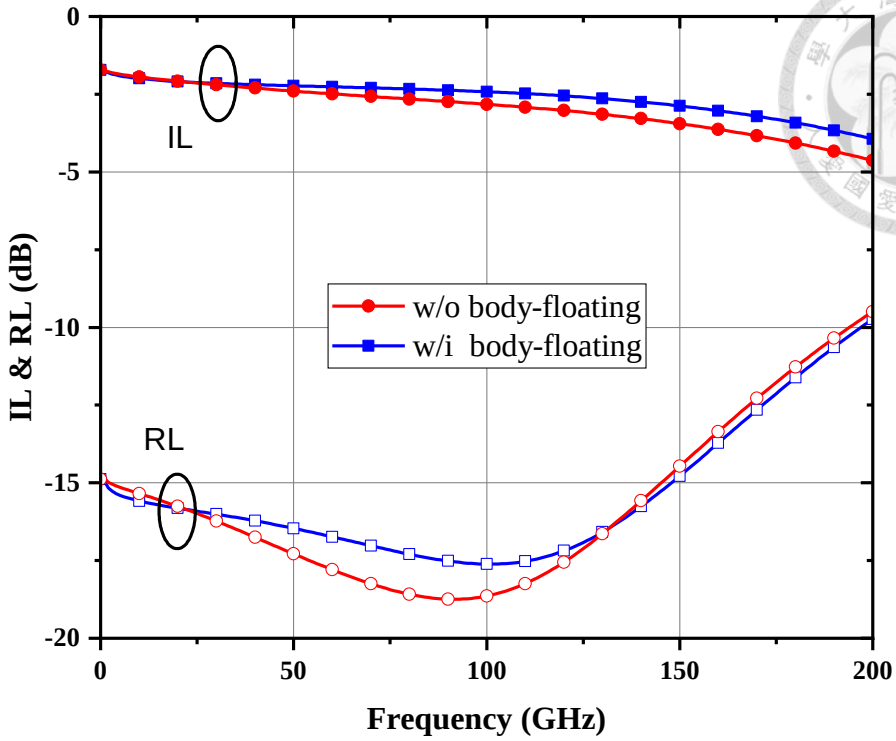

Fig. 4.11 The simulated IL and RL with and without the body-floating technique.

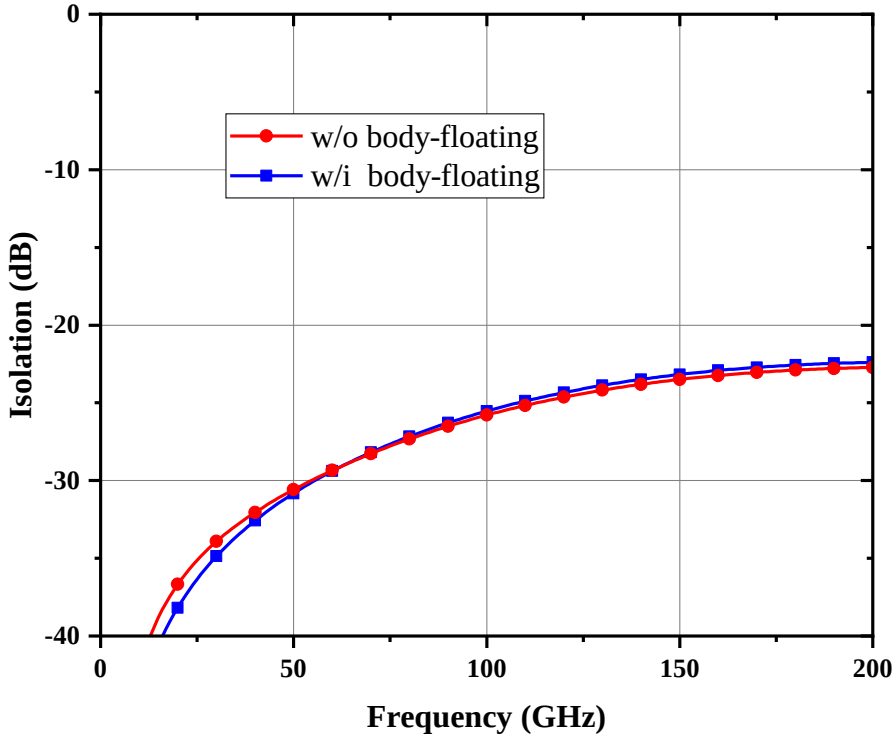

Fig. 4.12 The simulated isolation with and without the body-floating technique.

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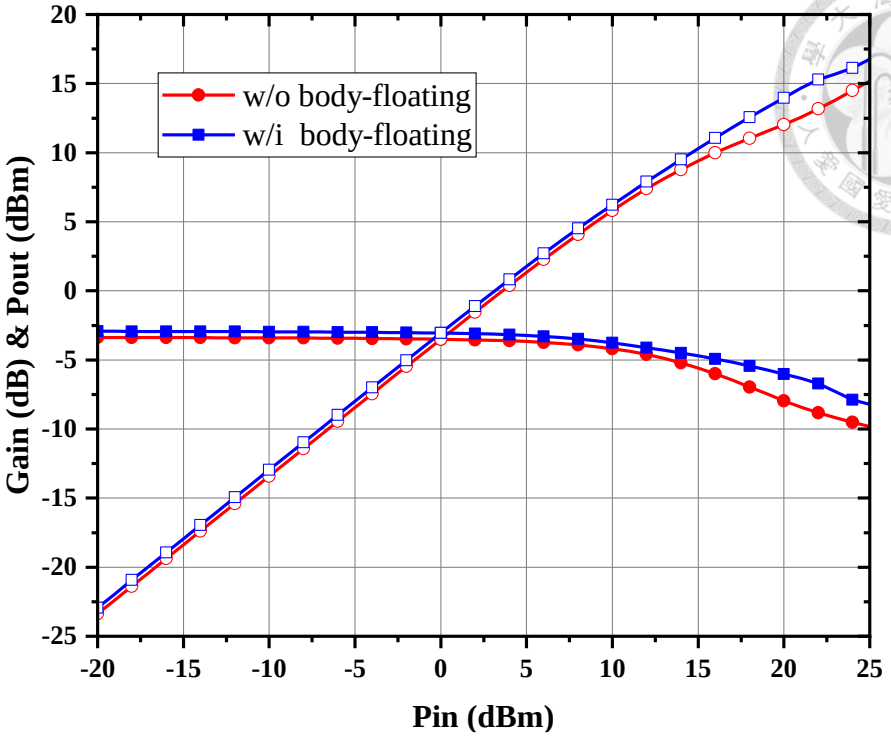

Fig. 4.13 The simulation large signal results at 140 GHz with and without the body-floating technique.

4.2.3 Circuit Architecture and Post-layout Simulation Results

The proposed SPST switch is implemented in TSMC 90-nm CMOS process with ultra-thick metal (UTM), eight metal layers (M_1 to M_8), and a metal-insulator-metal (MIM) capacitor. Advanced Design Software (ADS) and Sonnet Software are used throughout the design for circuit and post-layout simulation. Fig. 4.14 depicts a schematic of the proposed DC to D-band SPST switch based on a one-series and three-shunt nMOSFET transistors. The control voltage of the switch is set to 1.2 V, which is the maximum available voltage of the transistor. A transistor M_4 is shunted to R_1 to further improve the isolation of the switch. To further enhance the insertion loss performance, the body-floating technique is adopted in the design. Fig. 4.15 shows the layout of the proposed switch with a core area of 980 μm^2 (29 μm x 34 μm), and a total area of 0.195 mm^2 (0.3 mm x 0.65 mm) with all pads.

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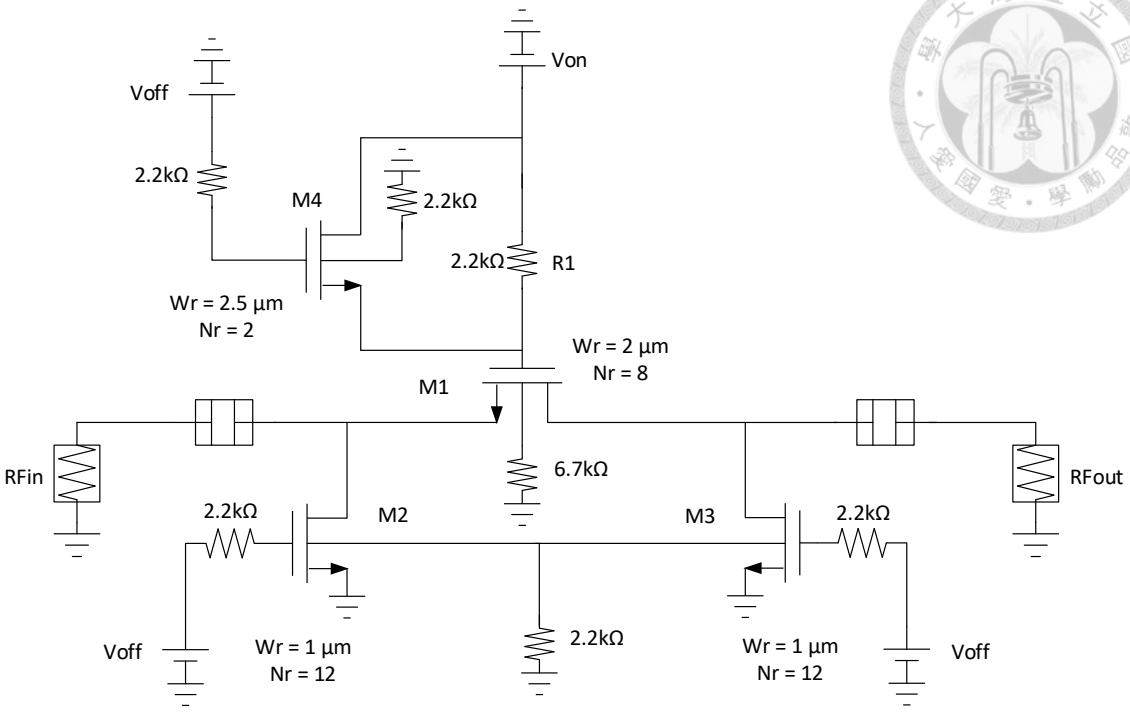

Fig. 4.14 The schematic of the proposed SPST switch.

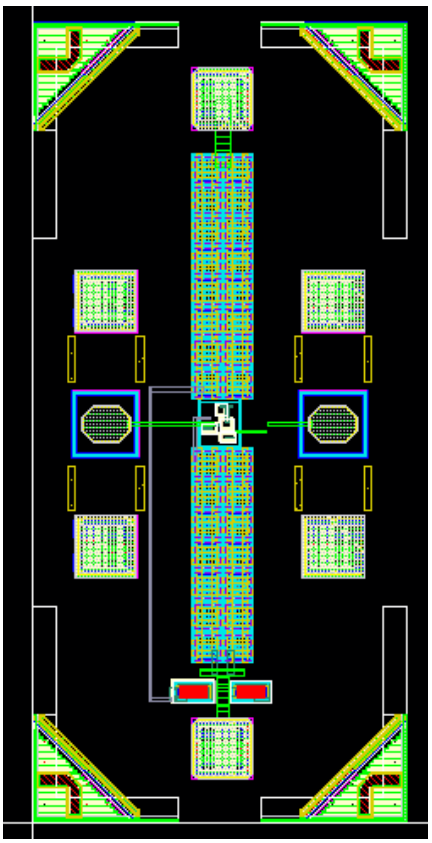

Fig. 4.15 The chip layout of the proposed SPST switch.

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Fig. 4.16 shows the simulated insertion loss of the proposed DC to D-band SPST switch. The insertion loss is less than 3.3 dB within 140 GHz, and under 3.6 dB within 170 GHz. Fig. 4.17 depicts the simulated return loss, which is larger than 14.6 dB and 10 dB within 140 GHz and 170 GHz, respectively. Fig. 4.18 demonstrates the off-state performance of the switch; the isolation is better than 19.2 dB and 17.7 dB within 140 GHz and 170 GHz, respectively. Fig. 4.19, Fig. 4.20, Fig. 4.21, and Fig. 4.22 illustrate the simulated power gain and output power under 75, 110, 140, and 170 GHz. The simulated results show that the IP_{1dB} are 9.7, 9.5, 9.7, and 10.3 dBm. Fig. 4.23 shows the two-tone simulation results at 140 GHz, where the IIP_3 of the proposed switch is 19.4 dBm.

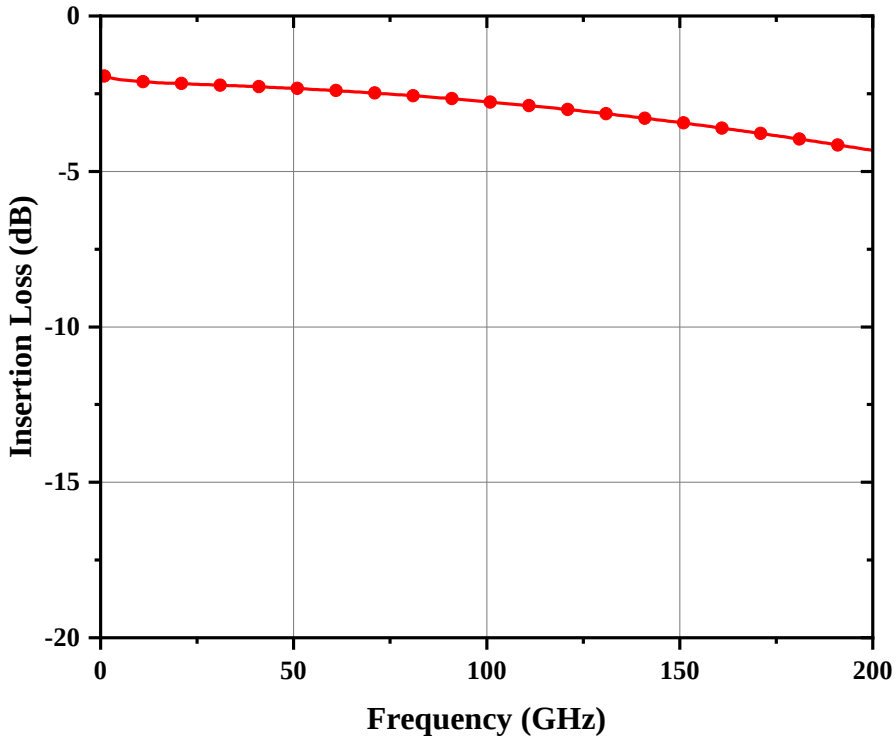

Fig. 4.16 The simulated insertion loss.

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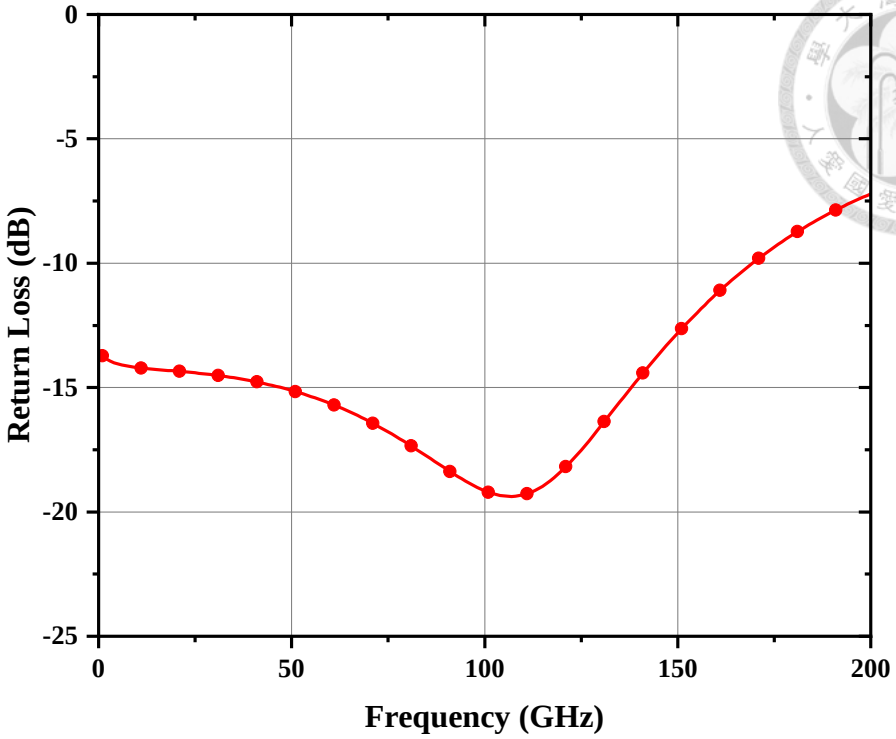

Fig. 4.17 The simulated return loss.

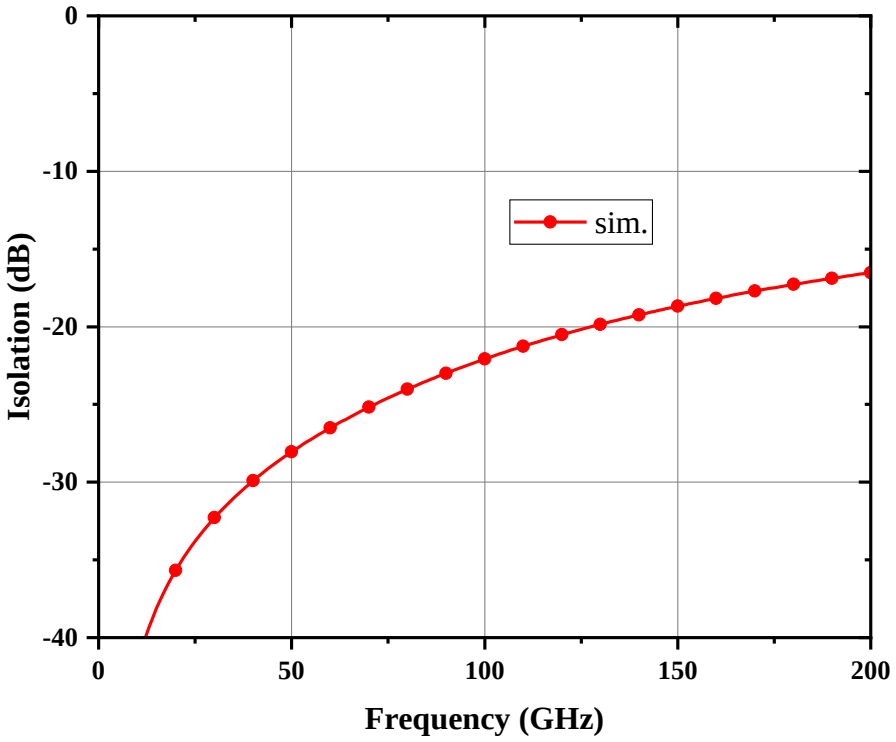

Fig. 4.18 The simulated isolation.

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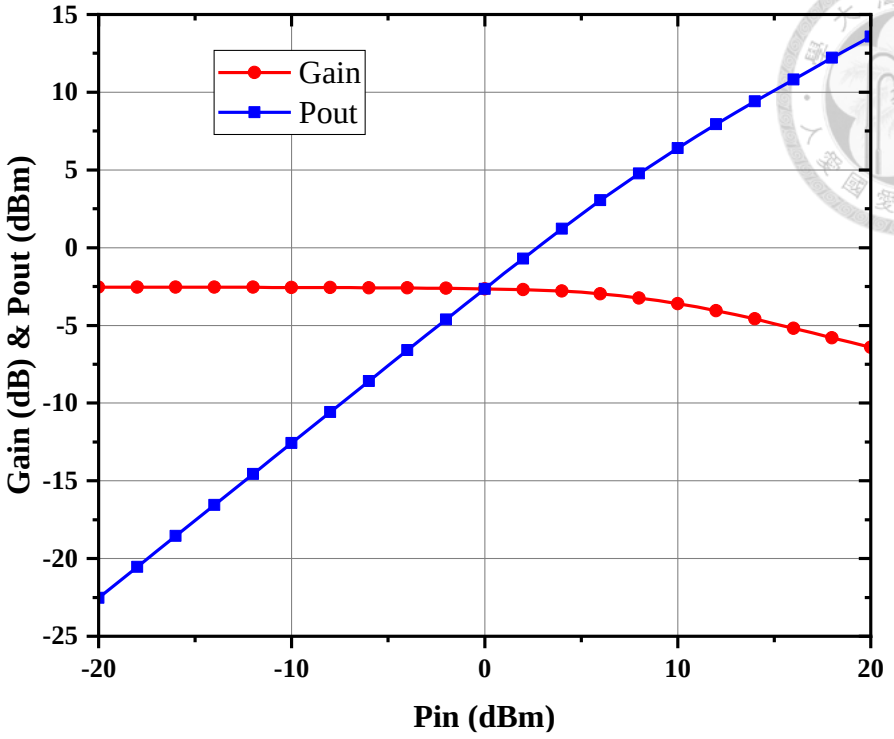

Fig. 4.19 The simulated large signal at 70 GHz.

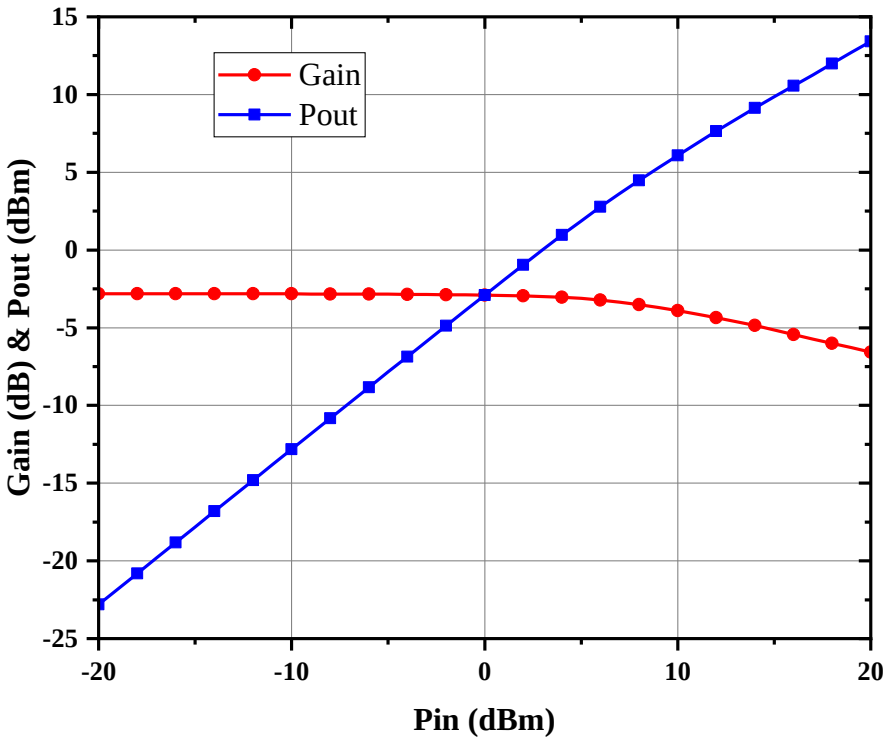

Fig. 4.20 The simulated large signal at 110 GHz.

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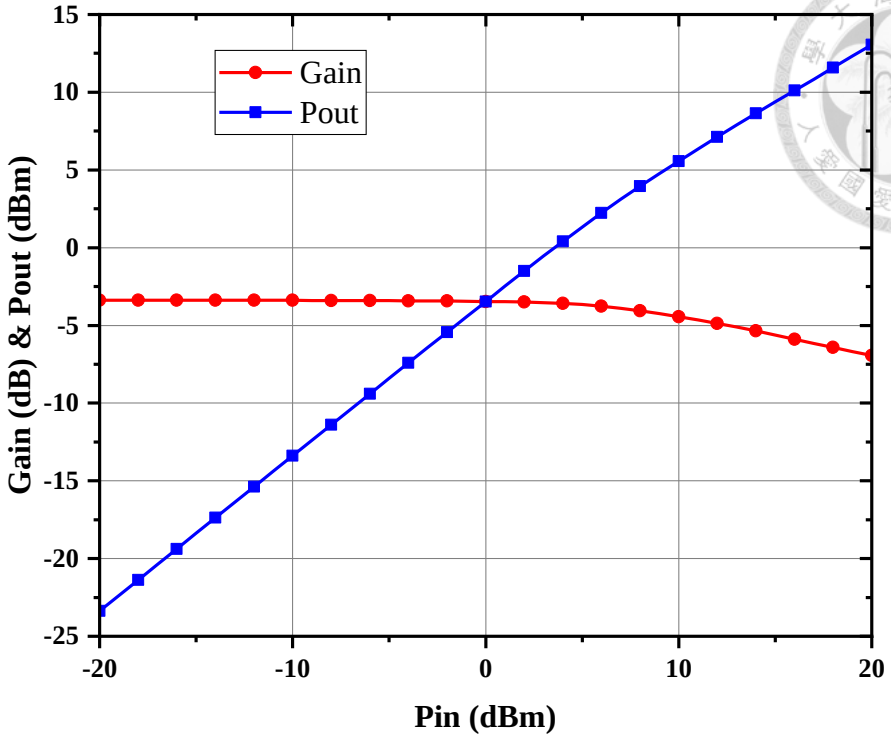

Fig. 4.21 The simulated large signal at 140 GHz.

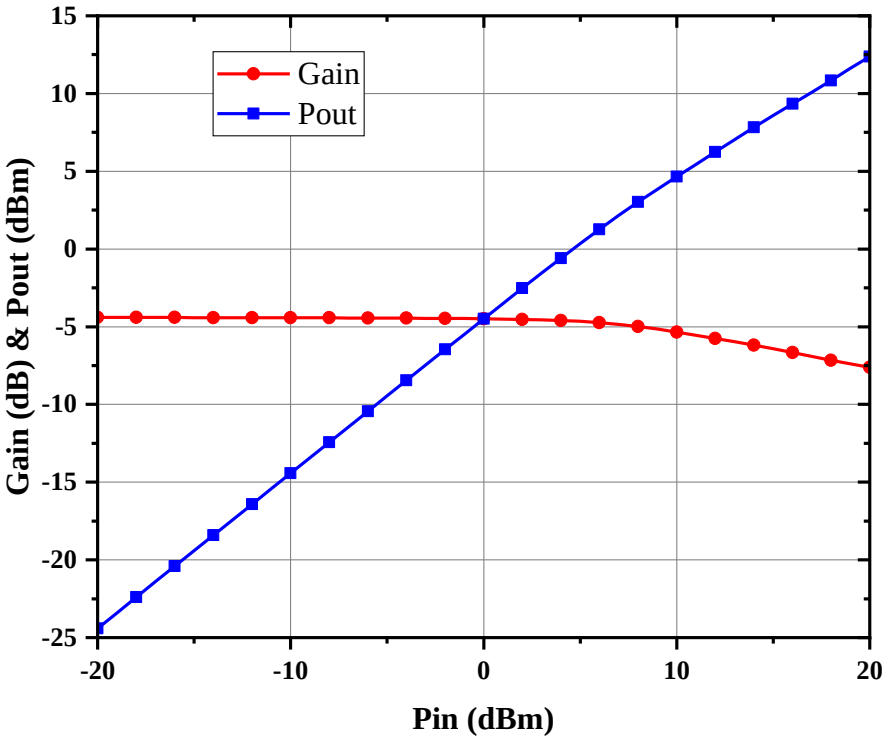

Fig. 4.22 The simulated large signal at 170 GHz.

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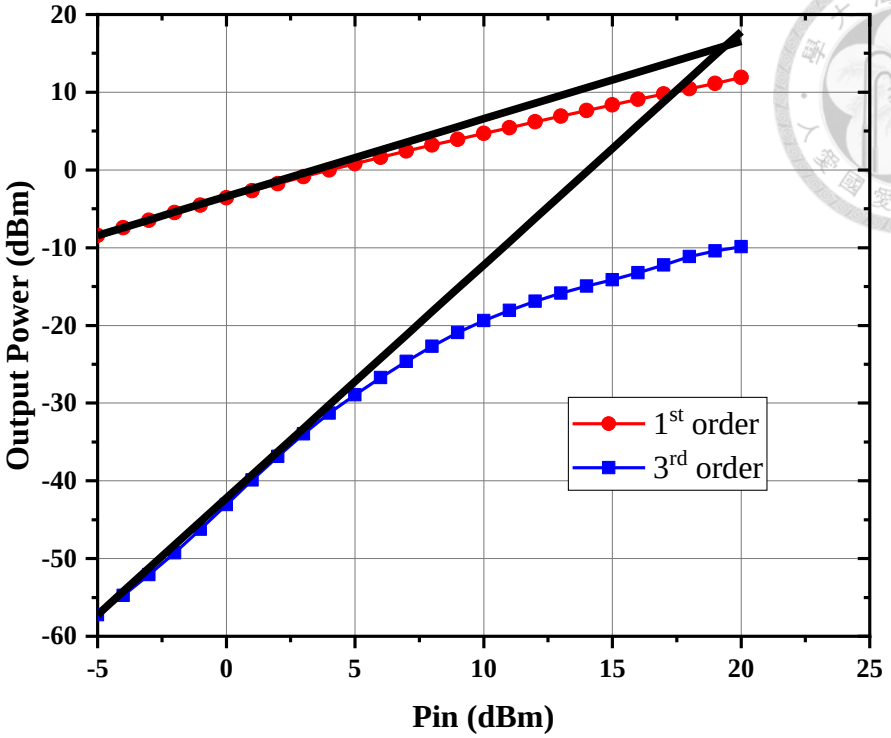

Fig. 4.23 Simulation of IIP_3.

4.3 Measurement Results

The chip micrograph of the proposed SPST switch, fabricated in a 90-nm CMOS process, is depicted in Fig. 4.24. The total area without pads is 980 μm^2. The circuit is measured on-wafer probing with GSG RF probes and DC bonding wiring on the PCB. The control voltage is set to 1.2 V, which is the maximum tolerable voltage level of the MOSFET. The S-parameters are measured by the Keysight N5291A vector network analyzer (VNA), which has an output power level of roughly -20 dBm. The large-signal continuous-wave power sweep is measured through an E8267D signal generator and an Agilent E4440A spectrum analyzer.

The simulated and measured insertion loss, return loss, and isolation at input power level of -20 dBm are shown in Fig. 4.25, Fig. 4.26, and Fig. 4.27, respectively. Based on the measured results, the proposed switch achieves a bandwidth of DC to 140 GHz with

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an insertion loss of less than 3.3 dB, a return loss of greater than 14 dB, and an isolation of greater than 22 dB. Further extending the cover frequency to 170 GHz, the proposed switch exhibits an insertion loss of less than 3.6 dB, a return loss of more than 9 dB, and an isolation of greater than 18.5 dB. Fig. 4.28 and Fig. 4.29 show the simulated and measured large-signal power results of the proposed switch at 75 and 110 GHz, achieving 10.6 and 10 dBm IP_{1dB}, respectively.

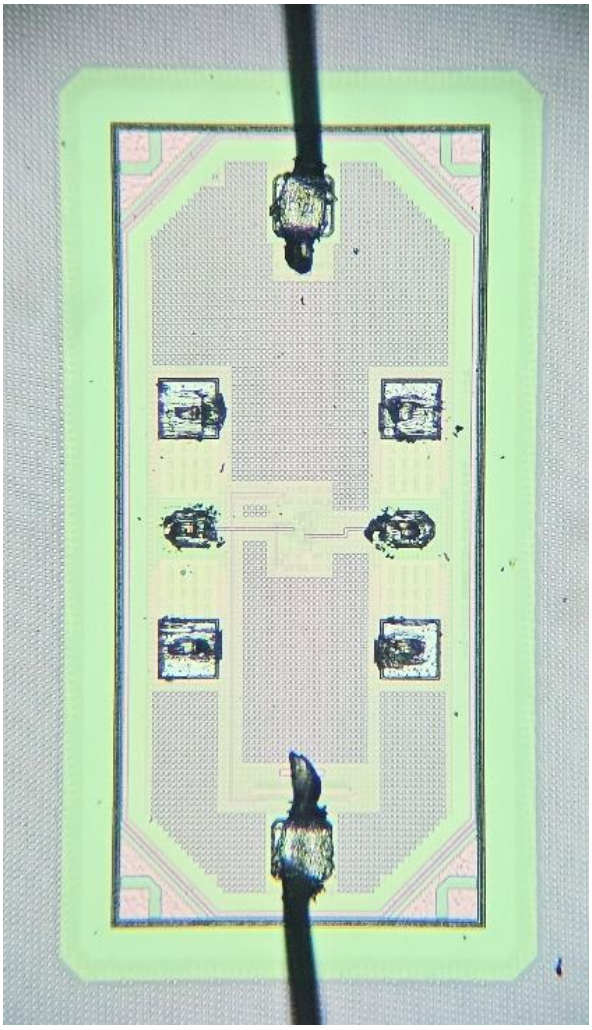

Fig. 4.24 The chip micrograph of the proposed SPST switch with a chip size of 0.195 mm^2 and a core area of 980 μm^2.

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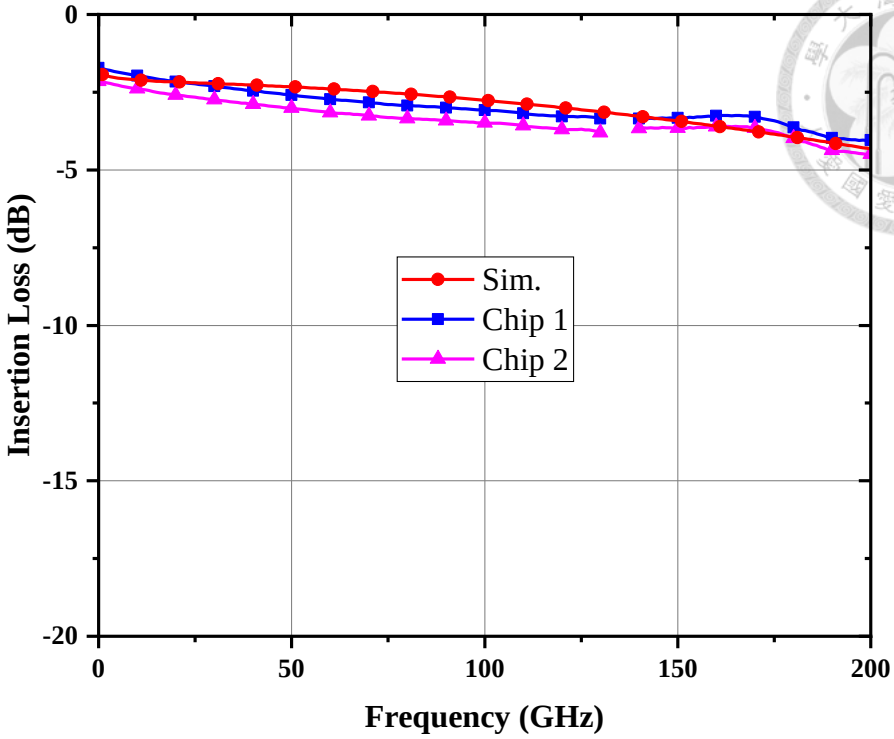

Fig. 4.25 The simulated and measured insertion loss.

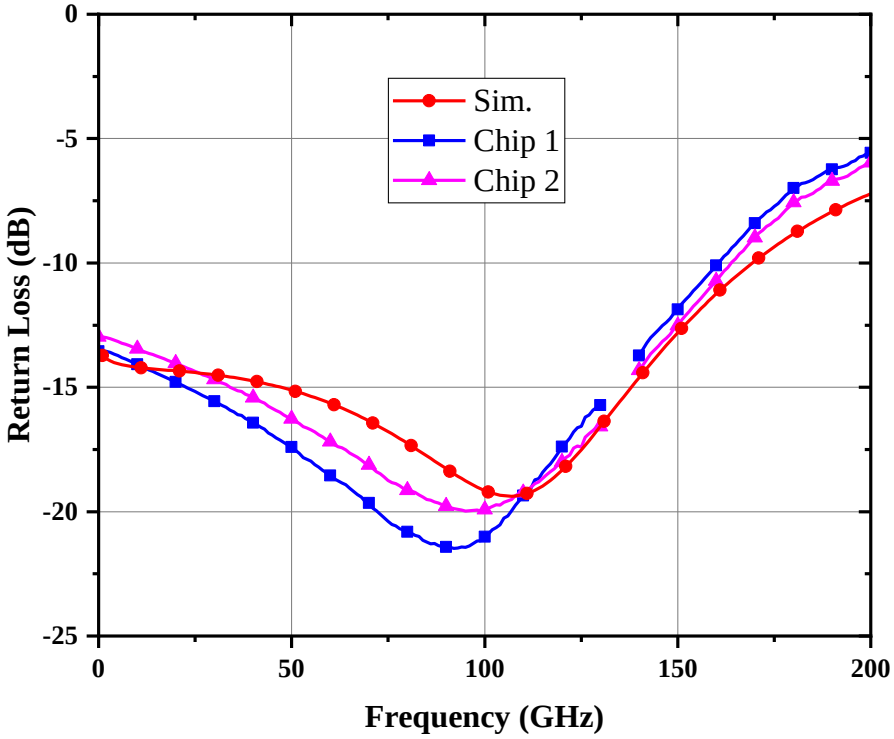

Fig. 4.26 The simulated and measured return loss.

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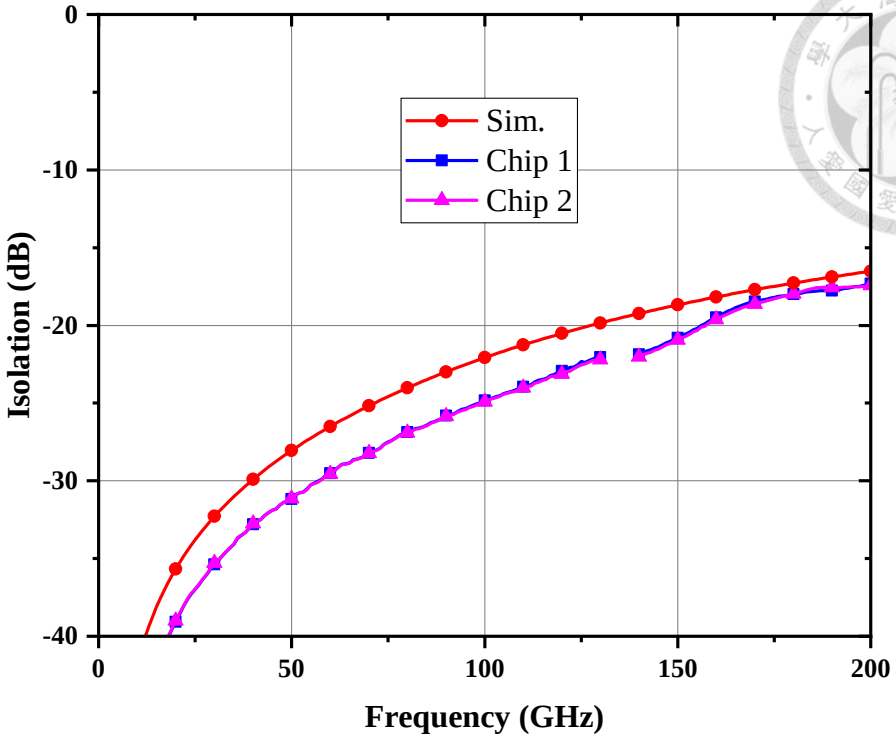

Fig. 4.27 The simulated and measured isolation.

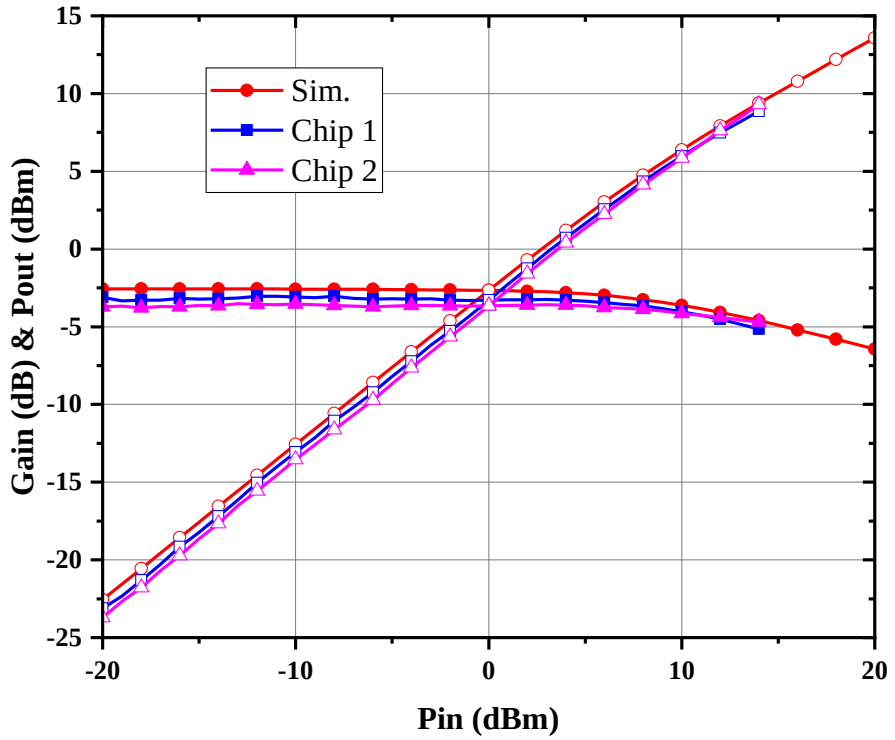

Fig. 4.28 The simulated and measured large signal at 75 GHz.

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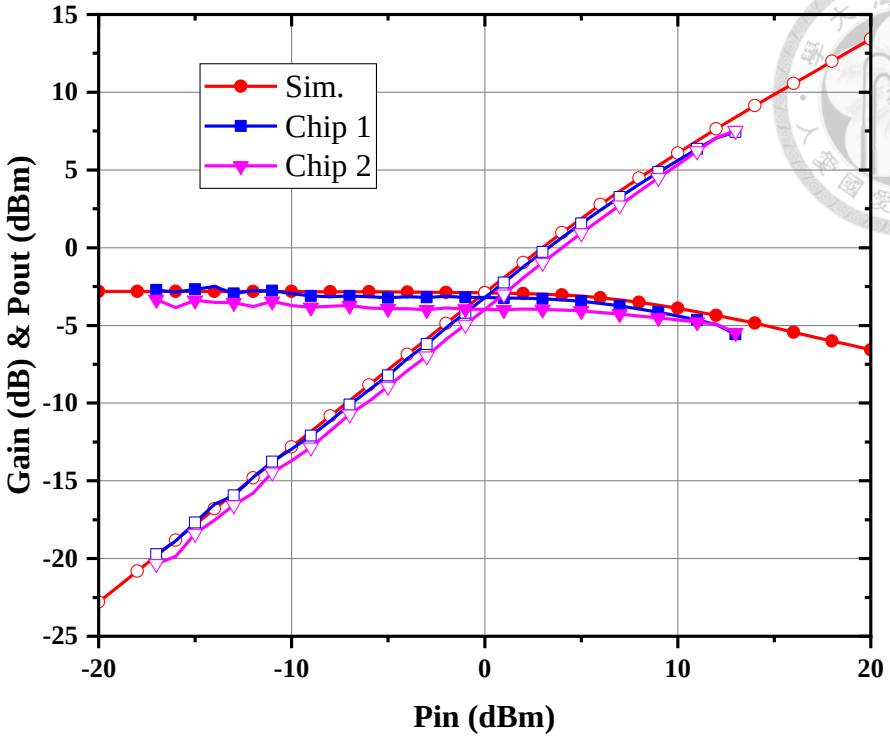

Fig. 4.29 The simulated and measured large signal at 110 GHz.

4.4 Summary

In this chapter, a DC to D-band SPST switch with ultra-compact area fabricated in the 90-nm CMOS process is presented. The proposed switch is composed of only four transistors and resistors, without utilizing large-area passive components such as inductors, transformers, and transmission lines. The body-floating technique is adopted in the design to further improve the insertion loss performance. The proposed switch achieves an insertion loss of less than 3.3 dB and 3.6 dB from DC to 140 GHz and 170 GHz, respectively, which has the potential to cover multiple ultra-wideband transceiver systems. The return loss is greater than 14 dB and 9 dB within the frequency ranges of 140 GHz and 170 GHz, respectively. The off-state performance of isolation is better than 22 dB and 18.5 dB within the 140 GHz and 170 GHz frequency ranges, respectively. The proposed switch achieves an IP_{1dB} of 10.6 dBm at 75 GHz and an IP_{1dB} of 10 dBm at 110

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GHz. The core area of the switch is 980 μm^2.

The performance of published millimeter-wave wideband SPST switches over the past few years is summarized in Table 4.3. The proposed SPST switch has an ultra-wide bandwidth with an ultra-compact core area, which is two or more orders of magnitude smaller than the previously reported mm-Wave broadband SPST switch. The insertion loss performance is also comparable to that of other more advanced processes. Meanwhile, the IP_{1dB} of the proposed switch is also the most remarkable among the MOSFET-based designs. Compared to the similar structure in reference [36], this work demonstrates improved performance based on i) adding one more shunt transistor to greatly improve the isolation performance while slightly sacrificing the insertion loss performance at high frequencies, and ii) a body-floating technique to improve the insertion loss performance with no cost.

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Table 4.3 Comparison of recently published switches and proposed switches.

Ref.	Process	Topology	Freq. (GHz)	IL (GHz)	RL (dB)	ISO (dB)	IP_{1dB} (dBm)	Core Area (mm^2)
[53]	250 nm InP HBT	Independent Reflective Load SPST	110-140	0.77-2.7	> 12	> 22.5	N/A	0.048
[54]	65-nm CMOS	transmission-line type SPST	110-170	< 3.6	N/A	> 19.5	N/A	0.013
[32]	65-nm CMOS	transmission-line type SPST	140-183	Min. 2.38	> 8	> 30	N/A	0.0067
[33]	22-mm FDSOI CMOS	Distributed SPST	DC~220	< 3.1	> 12	> 37	N/A	0.026
[34]	90-nm SiGe BiCMOS	PIN-diode SPST	DC~125	< 3.6	> 10.9	> 22	20@2GHz	0.106*
[35]	22-mm FDSOI CMOS	transmission-line type SPST	10~110	< 3.1	> 12	> 37	7@24GHz	0.018
[36]	22-mm FDSOI CMOS	Transistor- and resistor-based SPST	DC~110	< 3.1	> 12	> 22.8	10.8@50GHz	0.00016
This Work	90-nm CMOS	Transistor- and resistor-based SPST	DC~140 DC~170	< 3.3 < 3.6	> 14 > 9	> 22 > 18.5	10.8@75GHz 10@ 110GHz	0.00098

*Chip Area

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Chapter 5 Conclusions

This thesis presents the design and implementation of a broadband D-band driving amplifier using a 65-nm CMOS process for a 300 GHz phased-array transceiver system, a D-band frequency doubler using a 65-nm CMOS process for the 140 GHz local oscillation chain, and an ultra-wideband single-pole-single-throw (SPST) switch using a 90-nm CMOS process for the multi-band transceiver.

In Chapter 2, the D-band amplifier fabricated by a 65-nm CMOS process is presented. To achieve enough gain and bandwidth performance, a three-stage cascode structure with a gain-boosting technique is adopted, and a compensated matching technique is utilized in the design to broaden the bandwidth. With 39.3 mW DC power consumption, the measurement results showed that the bandwidth with a small-signal gain larger than 10 dB is 128 to 170 GHz. The peak gain is 21.3 dB at 165 GHz. The measured output-referred 1-dB compression point power levels are -7.4, -3.7, and -7.3 dBm at 140, 150, and 160 GHz, respectively. Furthermore, the core area of this work is highly compact, which occupies a total area with pads of 0.37 mm^2, and the core area of the proposed amplifier is 0.1 mm^2, nearly half the size of other similar structures. Furthermore, device measurement has also been done in this work, which shows good alignment in the desired frequency bands.

In Chapter 2, the D-band frequency doubler fabricated by a 65-nm CMOS process is demonstrated. To increase the conversion gain and output power performance, the cascode topology is adopted. The gain-boosting technique is also utilized in this design to further enhance the above performance. With the well-designed compensated Marchand balun, the amplitude and phase difference of the differential signal are minimized, which makes the doubler present an excellent fundamental rejection

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performance. With 16.3 mW DC power consumption under 3 dBm input power, the proposed frequency doubler exhibits a 3-dB bandwidth of 143 GHz to 170 GHz. The peak conversion gain is -3.5 dB at 158 GHz, and the peak output power is 0.76 dBm at 158 GHz with 4.3 dBm input power. The fundamental rejection is better than 41.3 dBc in the entire frequency bandwidth. The total chip area with all pads is 0.262 mm^2.

In Chapter 4, an ultra-wideband and ultra-compact SPST switch is designed for a multi-band transceiver system. The proposed switch is composed of only four transistors and several resistors, and without any large passive components such as an inductor, transformer, or transmission lines to minimize the chip size. The proposed switch achieves less than 3.3 dB and 3.6 dB insertion loss from DC to 140 GHz and 170 GHz, which has the potential to cover multiple ultra-wideband transceiver systems. The return loss is greater than 14 dB and 9 dB within 140 GHz and 170 GHz, respectively. The off-state performance of isolation is better than 22 dB and 18.5 dB within 140 GHz and 170 GHz, respectively. The proposed switch achieves an IP_{1dB} of 10.6 dBm at 75 GHz and an IP_{1dB} of 10 dBm at 110 GHz. The core area of the switch is 980 μm^2, which is two or more orders of magnitude smaller than the previously reported mm-Wave broadband SPST switch.

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