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鍺（錫）金氧半場效電晶體的低溫電子傳輸特性

Electron Transport in Ge(Sn) Metal-Oxide-Semiconductor Field-Effect Transistors at Cryogenic Temperatures

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本論文係陳彥洋 (R11943087) 在國立臺灣大學電子工程學研究所完成之碩士學位論文，於民國 114 年 06 月 27 日承下列考試委員審查通過及口試及格，特此證明。

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謝誌

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中文摘要

鍺錫 (GeSn) 合金因其具備直接能隙、高載子遷移率，以及與矽積體電路技術的相容性，在光電與電子應用領域中引起廣泛關注。儘管已有諸多研究展示出高性能的鍺錫元件，關於鍺錫由間接能隙轉變為直接能隙之機制，仍未獲得完整的理解。過往相關的實驗研究多半聚焦於光學特性，對於電性方面的探究則相對稀少。因此，本論文旨在探討鍺錫由間接能隙轉變為直接能隙對於電子傳輸特性造成的影響。

本研究使用化學氣相沉積 (CVD) 技術，成長高品質且應變鬆弛的鍺磊晶結構及錫原子比例分別為 4.5% 與 10.5% 的鍺錫磊晶結構。隨後製備鍺（錫） n 型金氧半場效電晶體 (n-MOSFETs)，並於 300 K 至 4 K 的溫度範圍內進行電性特性分析。在 300 K 時，隨著錫原子比例增加，元件的關閉電流上升而開態電流下降，推測原因分別為接面漏電流的增加與合金散射效應的加劇。在所有元件中，於積累區與空乏區皆觀察到異常高的閘極–通道電容，其成因為接面在交流訊號的驅動下提供了大量的多數載子（電洞）。本文提出一種方法，未來可用於校正關閉電流對閘極電容和等效遷移率的影響，適合應用於能隙小、遷移率高的電晶體，如鍺錫、砷化銦 (InAs) 及銻化銦 (InSb) n 型金氧半場效電晶體。當溫度自 300 K 降低至 4 K 時，隨著接面漏電流受到抑制，所有元件的關閉電流皆呈現單調遞減。然而，開態電流隨溫度的變化則呈現出較為複雜的行為。為便於分析，本研究採用分裂電容–電壓方法，以分離開態電流對電子濃度與遷移率的依賴性。在強反轉區中，閘極–通道電容對溫度的微幅變化，可歸因於反轉層電子在交流訊號驅動下的供應對溫度的變化。最後，本研究探討了電子的等效遷移率。隨著錫原子比例提升至 10.5%，遷移率隨溫度變化的趨勢由原先的單調遞減，轉變為在 100 K 至 20 K 之間出現異常上升的行為。此現象可歸因於直接能隙 $Ge_{0.895}Sn_{0.105}$ 元件中的遷移率提升，此提升係由隨著溫度降低，Γ 谷中電子數量的增加所致。根據傳輸特性的結果可推論，鍺錫材料中由間接能隙轉變為直接能隙的轉換範圍，發生於錫原子比例介於 4.5% 與 10.5% 之間。

關鍵字：鍺錫、金氧半場效電晶體、間接能隙至直接能隙的轉變、電子遷移率、小訊號模型

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ABSTRACT

Germanium-tin (GeSn) alloys have attracted great attention for both optoelectronic and electronic applications due to their direct-bandgap characteristics, high carrier mobility, and compatibility with Si VLSI technology. While numerous studies have demonstrated high-performance GeSn devices, the understanding of indirect-to-direct bandgap transition in GeSn remains incomplete. Previous experimental studies have predominantly focused on optical aspects, with limited electrical data available. This thesis investigates the impact of the indirect-to-direct bandgap transition on electron transport properties in GeSn.

High-quality, strain-relaxed Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ epitaxial structures are grown using chemical vapor deposition. Ge(Sn) n-type metal-oxide-semiconductor field-effect transistors (n-MOSFETs) are fabricated and characterized at temperatures of 300 K to 4 K. At 300 K, the off-state current increases and the on-state current decreases with the Sn fraction due to enhanced junction leakage and alloy scattering, respectively. Abnormally high gate-to-channel capacitance is observed in the accumulation and depletion regimes across all devices due to a large supply of majority carriers (holes) through the junctions in response to the AC signals. A method is proposed for future calibration of the off-state leakage effect on C_{GC}, and consequently, mobility extraction, which can be applied to small-bandgap, high-mobility transistors such as GeSn, InAs, and InSb n-MOSFETs. As the temperature decreases from 300 K to 4 K, the off-state current decreases monotonically across all devices due to the suppressed junction leakage. The on-state current, however, exhibits a complex trend with temperature. To facilitate analysis, the dependence of on-state current on both electron density and mobility is decoupled using a split C-V method. The slight temperature dependence of gate-to-

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channel capacitance in the strong inversion regime is a result of the temperature-dependent supply of inverted electrons in response to the AC signals. Lastly, the electron effective mobility is investigated. As the Sn fraction increases up to 10.5 at%, the trend of mobility over temperature transitioned from a monotonic decrease to one exhibiting an anomalous upturn between 100 K and 20 K. This is attributed to the mobility enhancement in the direct-bandgap $Ge_{0.895}Sn_{0.105}$ device due to an increased electron population in the Γ-valley as the temperature decreases. Based on the transport results, the indirect-to-direct bandgap transition in GeSn is identified to occur between Sn fractions of 4.5 at% and 10.5 at%.

Keywords: germanium-tin (GeSn), metal-oxide-semiconductor field-effect transistor (MOSFET), indirect-to-direct bandgap transition, electron mobility, small-signal model

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Chapter 1 Introduction

1.1 Motivation

Germanium-tin (GeSn) alloys hold great promise for optical and electrical device applications owing to their direct-bandgap characteristics [2] and small carrier effective masses [3]. In addition, the compatibility with Si VLSI technologies makes GeSn alloys a competitive platform for the monolithic integration of optoelectronics and nanoelectronics, offering a cost-effective alternative to III-V compound semiconductors [4]. Among the group-IV semiconductors, bandgap transitions between indirect valleys (X and L) as well as between indirect and direct valleys (L and Γ) have been predicted in the SiGe and GeSn alloy systems, respectively [1] (Fig. 1-1). When the Sn fraction exceeds 10 at%, GeSn undergoes an indirect-to-direct bandgap transition [1]. Due to their small bandgap energy, direct-bandgap GeSn alloys span the mid-wave infrared (3 – 8 μm) and far-wave infrared (8 – 14 μm) spectrums [1]. The combination of both properties enable high-performance infrared photonic applications, such as GeSn-based lasers [2] and

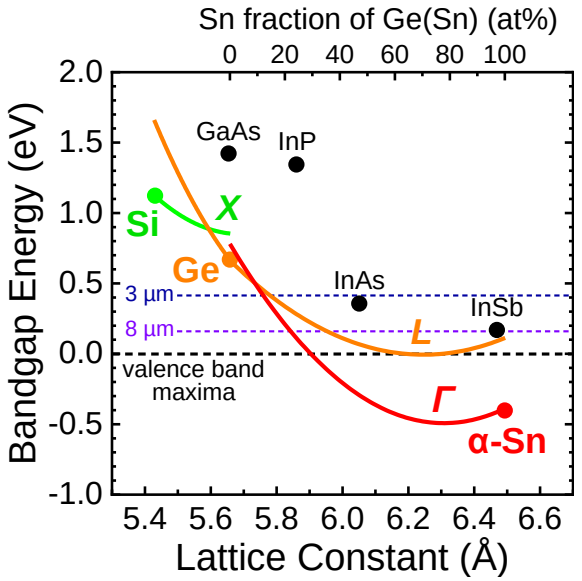

Fig. 1-1 Bandgap energy vs. lattice constant of the SiGe and GeSn alloy systems as well as direct-bandgap III-V compound semiconductors [1].

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photodetectors [5].

GeSn alloys also exhibit high carrier mobility. Traditionally, III-V compound semiconductors offer significantly higher electron mobility (~ 70,000 cm^2/Vs [6]) compared to that of Si and Ge (~ 1,400 and 3,900 cm^2/Vs, respectively [6]) (Fig. 1-2). However, the hole mobility in III-V materials is merely comparable to that in Si and significantly lower than that in Ge. Therefore, a heterogeneous group III-V/Ge complementary metal-oxide-semiconductor (CMOS) was proposed as a new transistor architecture to leverage their respective carrier mobility advantages [6]. Nevertheless, the integration of III-V materials with Ge remains a challenge, and GeSn alloys emerge as one of the alternative material platforms that offers a monolithic solution [4]. By incorporating Sn atoms into Ge, the hole mobility is greatly enhanced (~ 4,500 cm^2/Vs) [7]. On the other hand, in direct-bandgap GeSn, electron mobility comparable to that of III-V materials (~ 100,000 cm^2/Vs [8]) have been predicted thanks to a large electron population in the Γ-valley, where the electron effective mass is very small [9]. The superior carrier mobilities and direct-bandgap characteristics in GeSn enable high-performance GeSn-based electronic devices, such as metal-oxide-semiconductor field-effect transistors (MOSFETs) [10, 11], tunneling diodes [12], and tunneling FETs (TFETs) [13, 14].

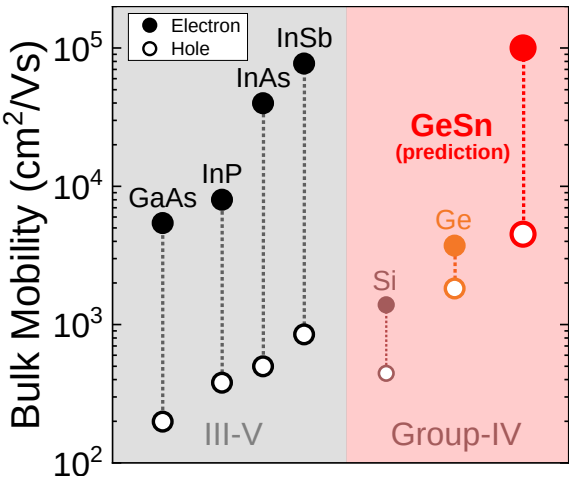

Fig. 1-2 Bulk mobility of electron and hole in group-IV and III-V compound semiconductors [6].

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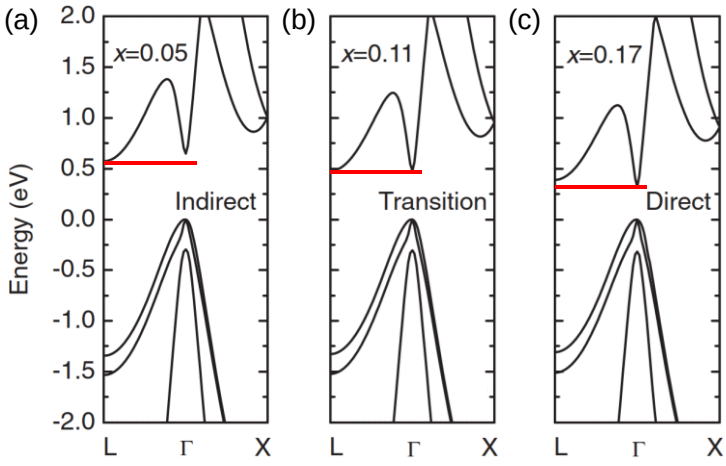
Despite extensive works of direct-bandgap GeSn in optoelectronic and electronic applications, the indirect-to-direct bandgap transition in GeSn is not yet fully understood. Previous experimental investigations have primarily focused on optical aspects [2, 15, 16], with very few electrical studies reported [9]. Therefore, in this work, the transport properties in Ge(Sn) n-type metal-oxide-semiconductor field-effect transistors (n-MOSFETs) were investigated. The temperature dependence of mobility changes substantially as the Sn fraction increases up to 10.5 at%, which is attributed to enhanced Γ-valley electron transport resulting from an indirect-to-direct bandgap transition in GeSn.

1.2 Tunable Band Structure of GeSn

By incorporating Sn atoms into Ge crystals, the bandgap energies of both the indirect valleys (e.g., X and L) and the direct valley (e.g., Γ) in GeSn decrease due to the increased lattice constant [7]. In addition to the reduction in bandgap energy, the strong spin-orbit coupling in Sn atoms raises the energy of the entire conduction band except for that at the Γ-point [7]. The combined effect of Sn incorporation is a more pronounced reduction in the bandgap energy of the direct Γ-valley compared to the other indirect valleys. There-



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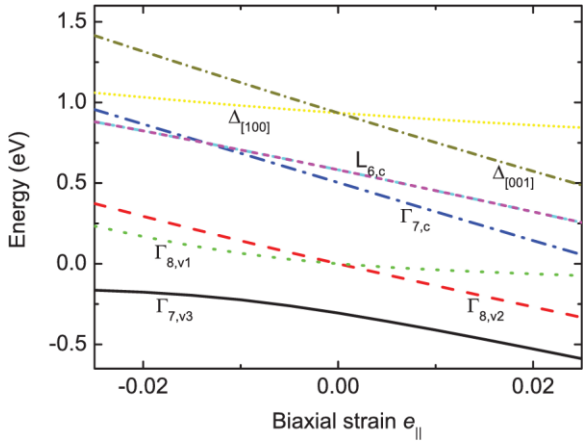
fore, by increasing the Sn fraction, an indirect-to-direct bandgap transition in GeSn can be achieved (Fig. 1-3). Another way to achieve the indirect-to-direct bandgap transition in GeSn is to apply in-plane biaxial strain. As the tensile (positive) strain increases, the energy of the conduction band edge at the Γ-point ($\Gamma_{7,c}$) decreases faster than that at the L-point ($L_{6,c}$), thereby resulting in a less energetic Γ-valley compared to the L-valley [18] (Fig. 1-4). The effect of Sn incorporation and strain on the "directness" of GeSn alloys are summarized in the contour maps showing the energy separation between the two valleys, where an indirect-to-direct transition in unstrained GeSn alloys occurs at a Sn frac-



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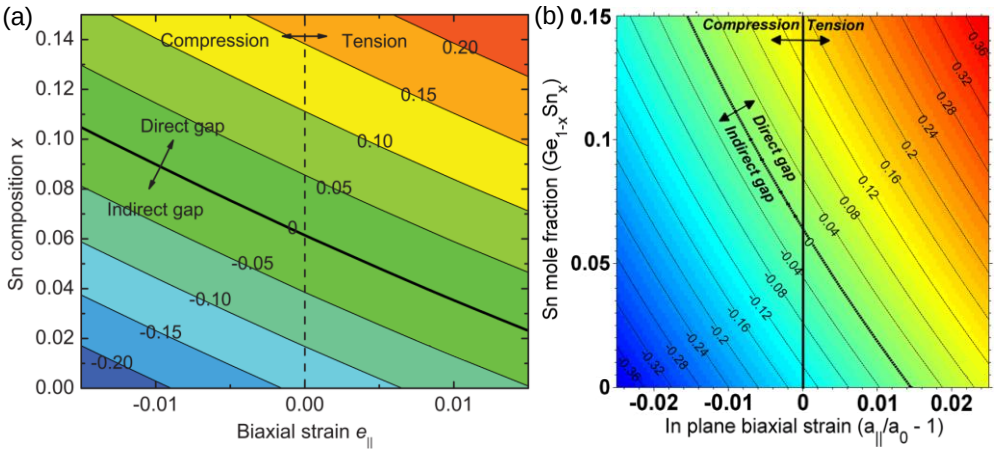

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tion of around 6 – 7 at% (Fig. 1-5).

The transition of GeSn alloys from an indirect-bandgap to a direct-bandgap material is clearly observed in the temperature-dependent photoluminescence (PL) spectra (Fig. 1-6). At room temperature, the PL spectrum of $Ge_{0.96}Sn_{0.04}$ exhibits only one peak, which is attributed to stronger radiative recombination from the direct Γ-valley compared to the indirect L-valley [15] (Fig. 1-6 (a)). As the temperature decreases, the single peak splits into two distinct peaks. This is attributed to the indirect bandgap nature of $Ge_{0.96}Sn_{0.04}$, which suppresses the thermal excitation of electrons to the direct Γ-valley at low temperatures and enhances radiative recombination from the indirect L-valley [20]. However, as the Sn fraction increases to 8 at% or 10 at%, only one peak is observed in the PL spectra, irrespective of temperature (Fig. 1-6 (b) and (c)). This is attributed to the indirect-to-direct

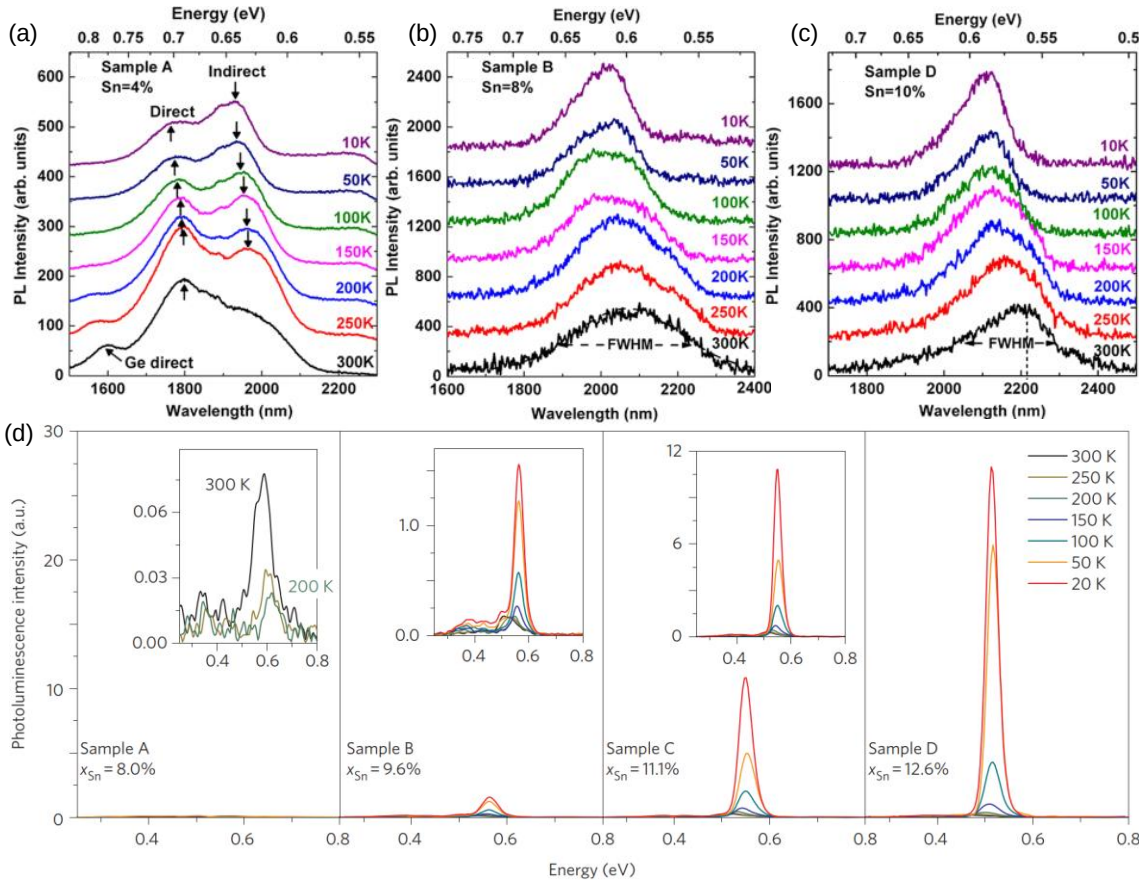

Fig. 1-6 Temperature dependent photoluminescence (PL) spectra of the GeSn alloys with Sn fractions of (a)-(c) 4 – 10 at% [15] and (d) 8.0% – 12.6% [2]. The insets in (d) show zoomed portions of the spectra.

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bandgap transition in GeSn, bringing the energy of the Γ-valley closer to or lower than that of the L-valley [15]. As a result, radiative recombination is dominated by that from the direct Γ-valley at all temperatures.

The indirect-to-direct bandgap transition in GeSn is also observed from the temperature-dependent PL intensity (Fig. 1-6 (d)). As the temperature decreases, the PL intensity of $Ge_{0.92}Sn_{0.08}$ decreases monotonically, implying that $Ge_{0.92}Sn_{0.08}$ is an indirect-bandgap material. This is because at low temperatures, electrons in $Ge_{0.92}Sn_{0.08}$ condense to the L-valley, where radiative recombination is significantly less efficient in comparison to that in the direct Γ-valley [2]. With Sn fractions of 9.6 at% and above, the PL intensity increases as the temperature decreases, and this enhancement becomes more pronounced with increasing Sn content. This is attributed to the indirect-to-direct transition in GeSn alloys, which brings the energy of the direct Γ-valley closer to or lower than that of the L-valley and results in an increased electron population in the Γ-valley, where radiative recombination is significantly more efficient than that in the indirect L-valley [2].

By applying in-plane biaxial compressive strain to GeSn alloys, the hole mobility is enhanced (Fig. 1-7 (a)). This is because the compressive strain breaks the symmetry of the group-IV diamond structure, thereby lifting the degeneracy of the heavy-hole (HH) and light-hole (LH) bands and splitting them into higher valence (HV) and lower valence (LV) bands [18]. As a result, more holes occupy the HV band, which is deformed and has a much-reduced effective mass compared to the degenerate HH band (Fig. 1-7 (b)). Furthermore, interband scattering is reduced due to the lifting of the Γ-point degeneracy, which further contributes to the enhancement of hole mobility in compressively strained GeSn [7]. In contrast, by increasing the Sn fraction and/or applying in-plane biaxial tensile strain to GeSn alloys, the electron mobility is enhanced (Fig. 1-8 (a)). This is because both Sn alloying and tensile strain increase the cell volume, which results in a faster

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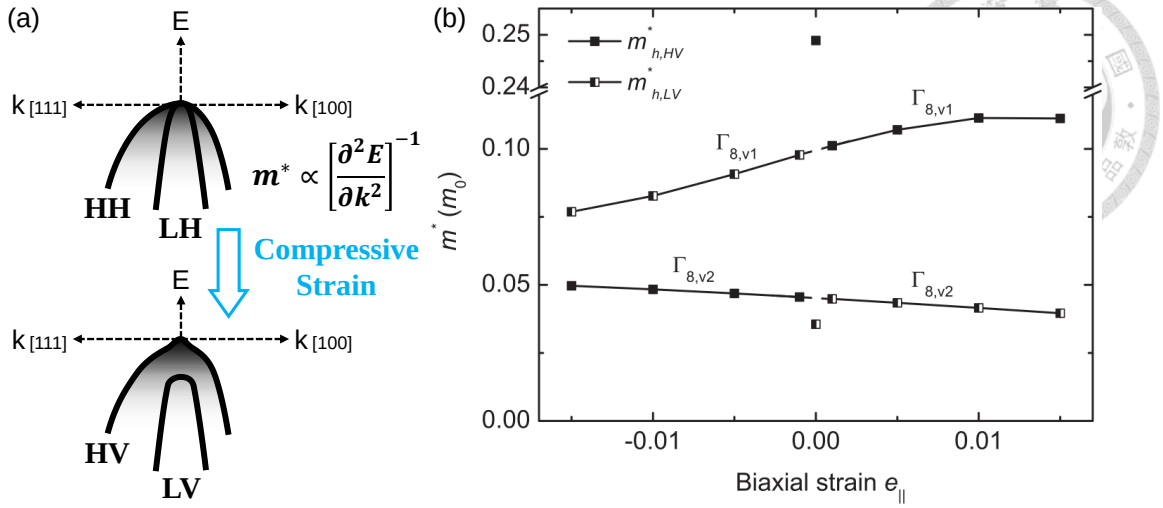

Fig. 1-7 (a) Schematics of the band structure showing the hole mobility enhancement in GeSn alloys. (b) Simulated hole effective masses of the higher valence ($m^*_{h,HV}$) and lower valence ($m^*_{h,LV}$) bands of $Ge_{0.9}Sn_{0.1}$ vs. in-plane biaxial strain along [100] direction [18].

reduction in the direct Γ-gap compared to the indirect L-gap [7]. As a result, more electrons occupy the Γ-valley, where the effective mass is much smaller than that of the L-valley (Fig. 1-8 (b)). Besides, the conductivity effective masses in both the L-valley and Γ-valley decrease with increasing Sn fraction, which might possibly lead to the enhancement of electron mobility in GeSn alloys with high Sn contents [17] (Fig. 1-8 (b)).

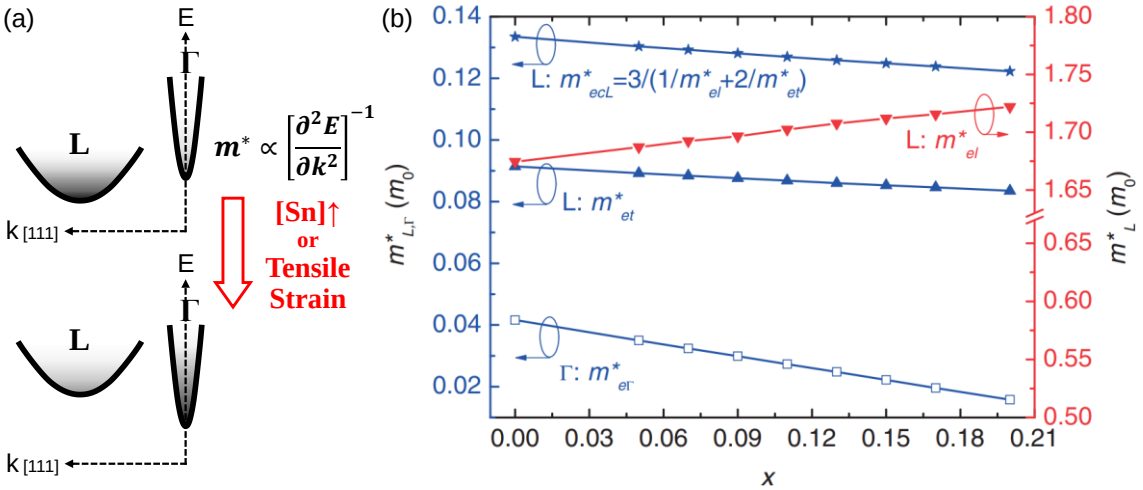

Fig. 1-8 (a) Schematics of the band structure showing the electron mobility enhancement in GeSn alloys. (b) Simulated conductivity effective masses of electron in the L-valley (m^*_{ecL}) and Γ-valley ($m^*_{e\Gamma}$) of strain-relaxed $Ge_{1-x}Sn_x$ alloys vs. Sn content x [17].

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The variation of electron mobility with the Sn fraction and tensile strain has been investigated in GeSn n-MOSFETs. Unexpectedly, the electron effective mobility does not increase as the Sn fraction increases from 6 at% to 8.5 at% (Fig. 1-9 (a)). This could be attributed to an enhanced alloy scattering with increasing Sn fraction [21]. By contrast, a significant enhancement in electron mobility is achieved by applying tensile strain while keeping the Sn fraction constant (Fig. 1-9 (b)). This is because the tensile strain increases the electron population in the Γ-valley, while the fixed Sn content ensures a constant alloy scattering intensity [11].

To investigate the effect of indirect-to-direct bandgap transition on the electrical transport properties in GeSn, a temperature-dependent mobility characterization is required. This is because the room-temperature data in Fig. 1-9 (b) only indicate that the Γ-valley lies lower in tensile-strained GeSn compared to compressively strained GeSn, but

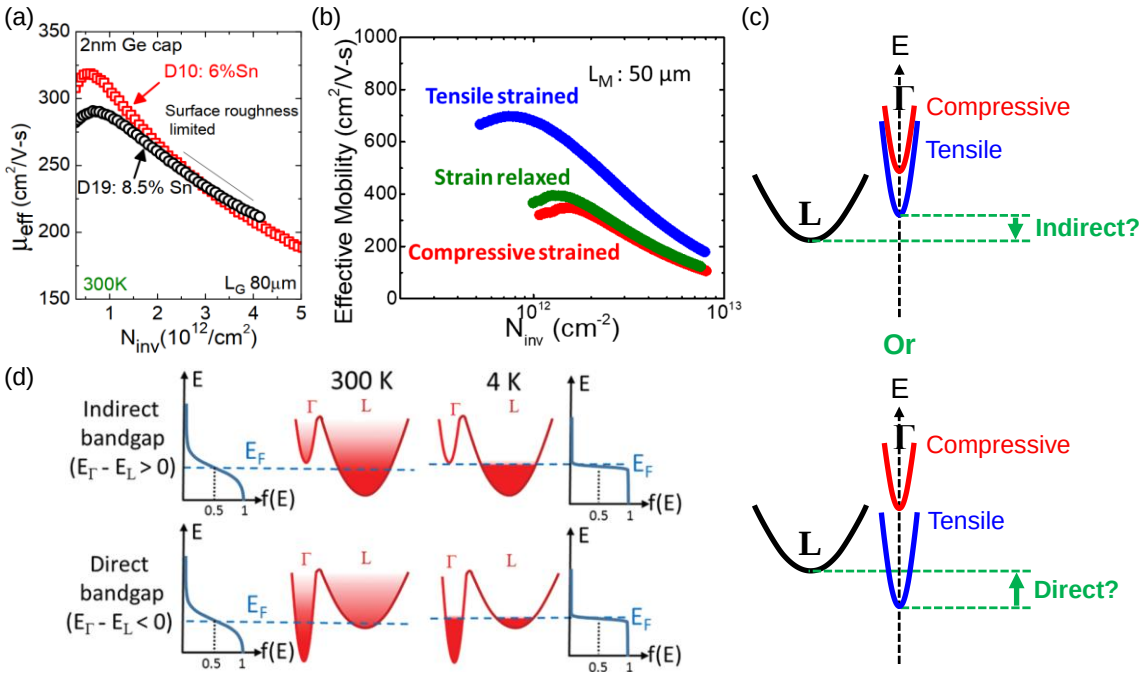

Fig. 1-9 Electron effective mobility (μ_{eff}) vs. inversion carrier density (N_{inv}) of GeSn n-MOSFETs (a) with different Sn fractions (compressive-strained) [21] and (b) different strain conditions ([Sn] = 4%) [11]. (c) Schematics of band structures of compressive and tensile-strained GeSn in (b). (d) Schematics of electron population in the L- and Γ-valleys of indirect-bandgap and direct-bandgap GeSn at 300 K and 4 K [12].

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do not confirm a transition to a direct bandgap GeSn (Fig. 1-9 (c)). Thanks to the suppressed Fermi-tail at low temperatures, electrons condense to different valleys depending on the indirect-bandgap or direct-bandgap nature of GeSn (Fig. 1-9 (d)). Due to the big difference in the electron effective masses between the Γ-valley and L-valley (Fig. 1-8 (b)), a distinct characteristic in the temperature-dependent of the effective mobility is expected when an indirect-to-direct bandgap transition in GeSn occurs. These will be explored in this work.

1.3 Thesis Outline

In this thesis, transport properties in GeSn n-MOSFET with a Sn fraction up to 10.5 at% are investigated from 300 K to 4 K. In Chapter 2, GeSn epitaxial growth, n-MOSFET fabrication, and the measurement methodology are introduced. Then, room-temperature device characteristics are investigated. Equivalent small-signal circuit models are proposed to explain the anomalous I-V and C-V results due to high off-state leakages. In Chapter 3, cryogenic device characteristics are investigated. Then, electron mobility and density are extracted using the split C-V method. As the Sn fraction increases, a drastic change in the temperature-dependence of mobility is observed. This is explained by the *dual-valley electron transport* and is attributed to the effect of indirect-to-direct bandgap transition in GeSn. Finally, the conclusions and future works of this thesis are given in Chapter 4.

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Chapter 2 Fabrication and Characterization of Ge(Sn) n-MOSFETs

GeSn alloys are promising for electronic applications due to their small carrier effective masses [3]. When compressive strain is applied on GeSn, the valence band is deformed, which reduces the effective mass of the heavy-hole band [18]. Furthermore, the compressive strain lifts the degeneracy at the Γ-point, which increases hole occupancy in the deformed heavy-hole band and further enhances hole mobility [18]. On the other hand, when tensile strain is applied on GeSn or the Sn fraction is increased, the Γ-valley is lowered relative to the L-valley [19]. This increases the electron population in the Γ-valley and enhances electron mobility, because the effective mass in the Γ-valley is much smaller than that in the L-valley [9]. The high carrier mobilities enable high-performance GeSn-based CMOS applications, making it a promising candidate for next-generation channel materials for transistors [4].

2.1 Introduction

Ge(Sn) n-type metal-oxide-semiconductor field-effect transistors (n-MOSFETs) with various architectures, such as planar [22], mesa [11], tri-gate (FinFET) [23], and gate-all-around (GAAFET) [24], have been reported. Ge(Sn) n-FinFETs and n-GAAFETs excel in device performance due to their excellent capability for gate control [23, 24], making them ideal candidates to further extend Moore's Law. To investigate electron transport in Ge(Sn) n-MOSFETs, it is necessary to characterize the dependence of electron mobility on electron density, which is commonly practiced using a split C-V method [25]. This method, however, cannot be applied to the FinFET or GAAFET since the gate capacitance is too small for a C-V meter to detect reliably. Ge(Sn) planar and mesa n-

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MOSFETs are preferred for the split C-V method due to their large gate-to-channel areas [11, 22], with examples of successful mobility extraction summarized below.

2.1.1 Planar GeSn n-MOSFETs

Prior to the deposition of GeSn layers, a Ge epitaxial layer is grown on a Si substrate and subjected to in-situ hydrogen annealing to form a strain-relaxed, defect-free virtual substrate [26, 27]. This facilitates the subsequent growth of a fully strained GeSn active layer and preserves the film quality by reducing the defect formation associated with strain relaxation [28]. The device structure is shown in Fig. 2-1 (a). In transfer I-V curves, clear transistor characteristics with an on-off current ratio (I_{ON}/I_{OFF}) of approximately 10^2 is observed (Fig. 2-1 (b)). In the microwave-annealed (MWA) device, the off-state current (I_{OFF}) is lower and the gate-induced drain leakage is less pronounced than in the rapid thermal annealed (RTA) devices (Fig. 2-1 (b)) thanks to the much suppressed dopant diffusion during the MWA process [22]. In addition, the on-state gate-to-channel capacitance

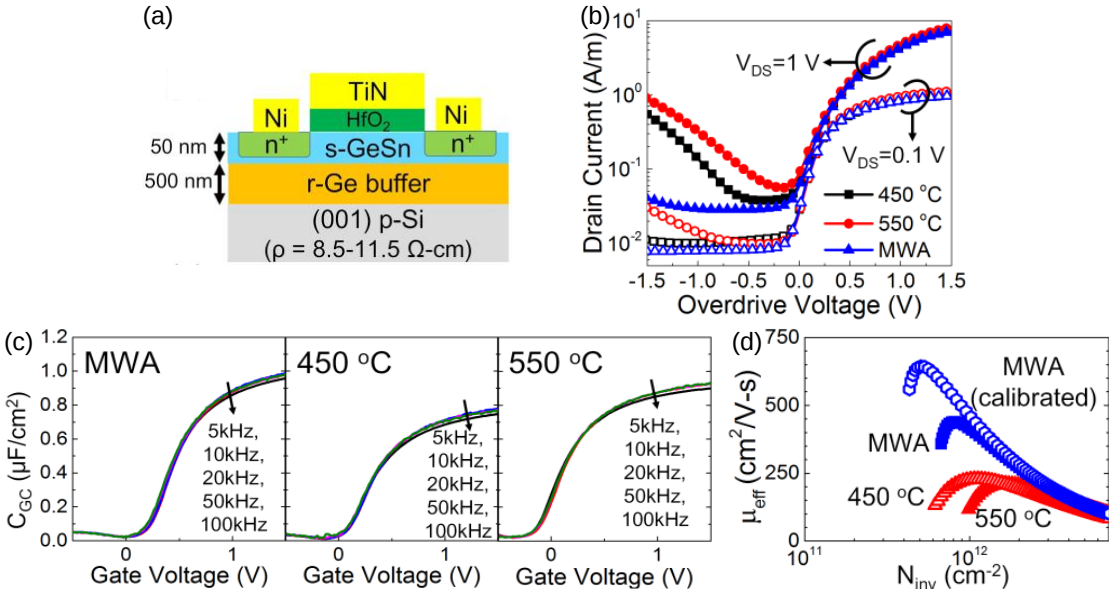

Fig. 2-1 (a) Device structure, (b) transfer I-V characteristics, (c) normalized gate-to-channel capacitance (C_{GC}) vs. gate voltage, and (d) effective mobility (μ_{eff}) vs. inversion carrier density (N_{inv}) of the planar $Ge_{0.955}Sn_{0.045}$ n-MOSFET [22].

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(C_{GC} at gate voltage = 1.5 V) is higher for the MWA device (Fig. 2-1 (c)), indicating that the quality of gate stack and oxide/semiconductor interface are better preserved by MWA [22], as evidenced by the higher effective mobility (μ_{eff}) of the MWA device (Fig. 2-1 (d)). These results show that MWA is a better dopant activation method compared to RTA for GeSn n-MOSFETs. It's worth noting that the electron transport occurs exclusively within the $Ge_{0.955}Sn_{0.045}$ layer, because the inversion channel only spans a few nanometers near the surface (Fig. 2-1 (a)) [29, 30]. Consequently, the μ_{eff} reflects only the transport properties in $Ge_{0.955}Sn_{0.045}$ channel, which is very different from the cases discussed below.

2.1.2 Mesa GeSn n-MOSFETs

Mesa GeSn n-MOSFETs are identical to the planar devices (Fig. 2-1 (a)), except that the source and drain are "recessed", i.e., formed in a wider-bandgap layer (Ge) beneath the channel ($Ge_{0.96}Sn_{0.04}$) (Fig. 2-2 (a)), to reduce off-state current (I_{OFF}) [11]. In transfer I-V characteristics, an on-off current ratio (I_{ON}/I_{OFF}) of approximately 200 is observed for the mesa structure, which is larger than those for the planar structures (~ 10 for Si substrates and ~ 5 for SOI substrates) (Fig. 2-2 (b)). Given that the on-state current (I_{ON}, drain current at gate voltage = 3 V) is similar for both structures (Fig. 2-2 (b)), the higher I_{ON}/I_{OFF} is attributed to a lower I_{OFF} in the mesa structure thanks to its "recessed" source and drain (formed on a wider-bandgap Ge layer) [11]. The I_{OFF} is higher in the planar structures because their junctions are formed on a narrower-bandgap $Ge_{0.96}Sn_{0.04}$ layer [11]. These results show that the mesa structure is excellent for suppressing I_{OFF} while taking advantage of the high channel mobility in the $Ge_{0.96}Sn_{0.04}$ layer.

As the mesa length (L_M) increases, the effective mobility increases accordingly (Fig. 2-2 (c)). This is attributed to an increasing contribution from the high-mobility, tensile-strained $Ge_{0.96}Sn_{0.04}$ layer, because the total mobility (μ_{eff}) is consisted of contributions

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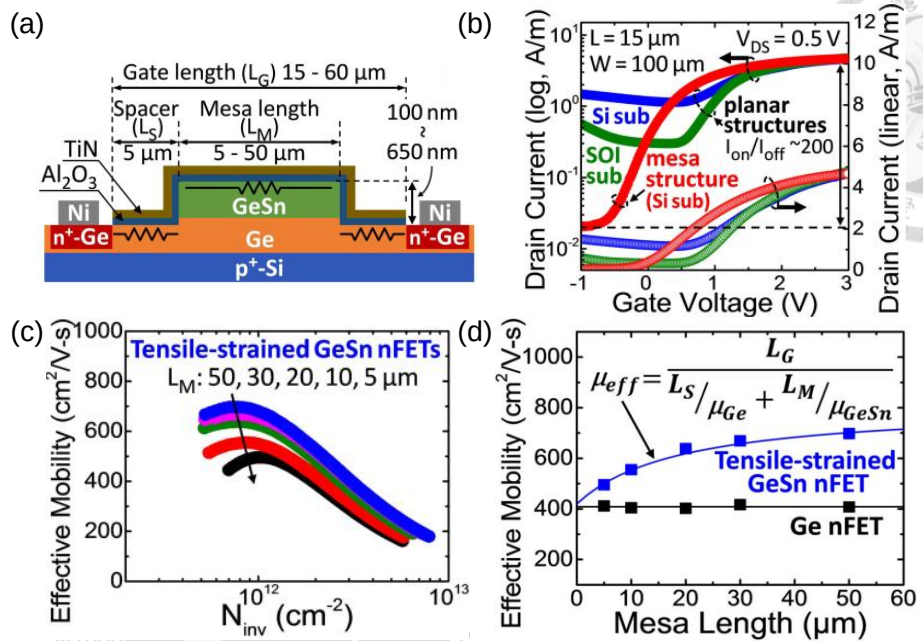

Fig. 2-2 (a) Device structure of the mesa GeSn n-MOSFETs [11]. (b) Transfer I-V characteristics of the planar (on Si and SOI substrates) and mesa $Ge_{0.96}Sn_{0.04}$ n-MOSFETs [11]. (c) Effective mobility (μ_{eff}) vs. inversion carrier density (N_{inv}) of the tensile-strained $Ge_{0.96}Sn_{0.04}$ n-MOSFETs with various mesa lengths (L_M) [11]. (d) μ_{eff} vs. L_M of the Ge n-MOSFETs and tensile-strained $Ge_{0.96}Sn_{0.04}$ n-MOSFETs [11].

from both the recessed source and drain regions (μ_{Ge}) and the mesa region (μ_{GeSn}) (Fig. 2-2 (a)) [11], as evidenced by the well-fitted curves to the data extracted from Fig. 2-2 (c) (Fig. 2-2 (d)). Consequently, the effective mobility does not reflect the "pure" electron transport in the $Ge_{0.96}Sn_{0.04}$ layer. Instead, it reflects a combination of transport in both the "recessed" Ge channel and the $Ge_{0.96}Sn_{0.04}$ channel. The "pure" electron mobility in the $Ge_{0.96}Sn_{0.04}$ channel can only be approximated by either making L_M much larger than the spacer length (L_S) or extracting the parameter μ_{GeSn} from the equation in Fig. 2-2 (d) via parametric fitting [11]. As a result, the planar structure is preferred over the mesa structure for extracting the "pure" GeSn mobility.

2.1.3 Surface-Capped GeSn n-MOSFETs

Surface-capped GeSn n-MOSFETs are identical to the planar ones (Fig. 2-1 (a)),

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except that the GeSn channel is capped with Ge (Fig. 2-3 (a)) [21]. Lower interface trap density (D_{it}) is observed for samples capped with a thicker Ge layer (Fig. 2-3 (b)), which translates into a steeper subthreshold-swing (SS) (Fig. 2-3 (c)) and a higher effective mobility (μ_{eff}) (Fig. 2-3 (d)) due to a lower interface trap capacitance [31] and fewer Coulomb scatterers at the oxide/semiconductor interface [10, 32, 33], respectively. These results indicate that the surface-capped structure is excellent for improving SS and μ_{eff}. Nevertheless, it's worth noting that a significant portion of electron transport occurs in the Ge capping layer, even if it is as thin as 2 nm. This is because the conduction band offset between Ge and GeSn (either with a Sn fraction of 6 at% or 8.5 at%) is negligible compared to the thermal energy at room temperature (~25 meV) [34], and the electron distribution in the inversion channel only spans a few nanometers near the surface [29, 30]. Consequently, the μ_{eff} does not reflect the "pure" electron transport in the $Ge_{0.94}Sn_{0.06}$ or

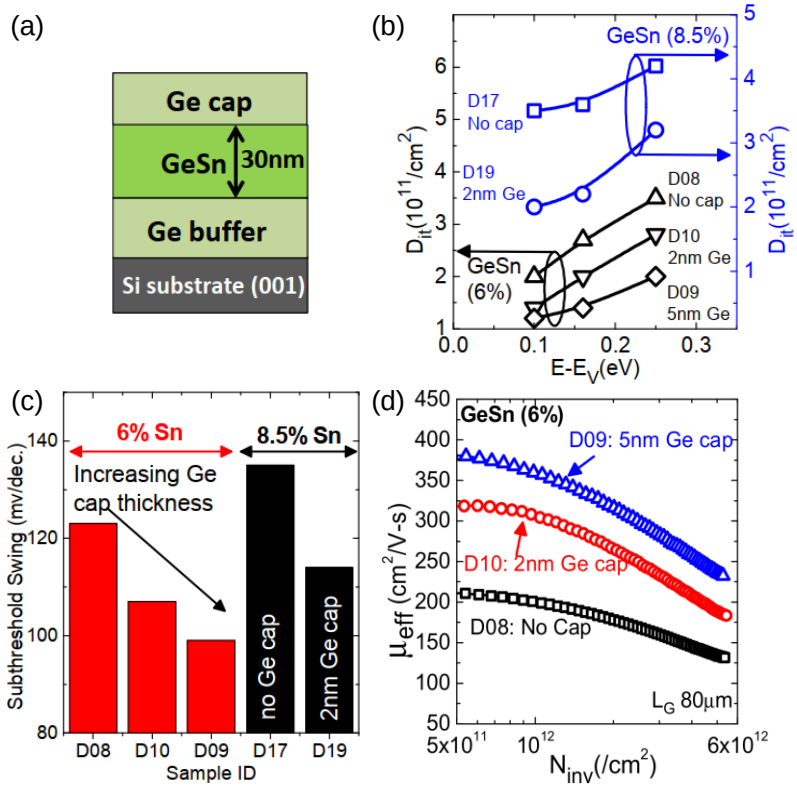

Fig. 2-3 (a) Epitaxial structure, (b) interface trap density (D_{it}) vs. energy ($E-E_V$), (c) subthreshold swing, and (d) μ_{eff} vs. N_{inv} of the planar $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.915}Sn_{0.085}$ n-MOSFETs with or without a Ge cap [21].

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$Ge_{0.915}Sn_{0.085}$ layer. Instead, it reflects a combination of transport in both the Ge layer and the GeSn layer. Since it is difficult to eliminate the contribution of the Ge layer to the μ_{eff}, the planar structure is preferred over the surface-capped structure for extracting the "pure" GeSn mobility.

2.2 Experiment

2.2.1 Material Growth and Analysis

The indirect- to direct-bandgap transition in strain-relaxed Ge(Sn) occurs at a Sn fraction of 6 – 7 at% [18, 19, 35]. Therefore, direct-bandgap Ge(Sn) is metastable and has to be prepared using a non-equilibrium, low-temperature growth method, because the solubility of Sn in Ge is much lower than 6 – 7 at% (< 1.1 at%) [36]. Since CVD allows low-temperature growth of Ge(Sn) with wafer-scale uniformity [37, 38], a commercially available reduced-pressure chemical vapor deposition (RPCVD) system (ASM Epsilon 2000) was used in this study for Ge(Sn) epitaxial growth. Digermane (Ge_2H_6) and tin-tetrachloride ($SnCl_4$) were used as precursors, with ultra-pure hydrogen (H_2, 99.9999 %) serving as the carrier gas.

The deposition process is outlined as follows (Fig. 2-4). First, the chamber was heated to 1,170 ℃ and etched by hydrogen chloride (HCl) to remove residues left from the previous process. Then, the chamber was cooled to 600 ℃, and a bare p^+-Si (100) wafer, pre-cleaned with diluted hydrofluoric acid (HF, 1:50), was loaded. Following that, an in-situ H_2 baking at 1,100 ℃ was performed to remove native oxides. Subsequently, the chamber was cooled to 325 ℃ and then heated up to 375 ℃, during which a layer of 500-nm or 700-nm Ge was deposited (Fig. 2-5 (a)). Then, another in-situ H_2 annealing at 800 ℃ was performed for 10 min. to reduce the threading dislocations and to relax the strain of the Ge film [27, 39]. This makes the Ge surface defect-free [26], effectively

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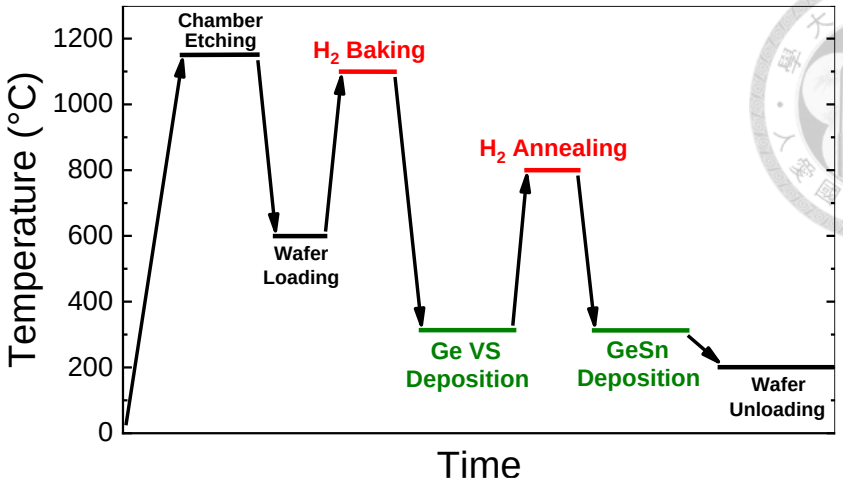

Fig. 2-4 A schematic of the deposition process of Ge(Sn) epitaxial structures.

creating a new substrate, i.e., a virtual substrate (VS), with a smaller lattice mismatch with GeSn compared to that between Si and GeSn [40], thereby facilitating the subsequent growth of high-quality GeSn films. The chamber was then cooled to 320 °C, and a layer of 550-nm GeSn with either a lower or higher $SnCl_4$ flow rate was deposited (Fig. 2-5 (a)). Note that the GeSn films were grown thick in an effort to exceed their critical thicknesses, thereby relaxing the default compressive-strain when grown on Ge [41], making the GeSn film more direct-bandgap-like [18, 19, 35]. The dopant gas is not introduced during the growth of the Ge and GeSn films to minimize the influence of Coulomb scattering on electron transport caused by the charged impurities. Nevertheless, unintentional doping (UID) is still detected in the Ge and GeSn films, with p-type carrier concentrations of approximately 10^{16} to 10^{17} cm^{-3} [9]. This is possibly due to acceptor-like defect states near the valence band generated by crystal imperfections [42], which acts as Coulomb scatterers due to the their charged nature.

Strains and Sn fractions of the Ge(Sn) epitaxial structures were characterized by high-resolution reciprocal space mapping (HRRSM) [11] (Fig. 2-5 (b)). The Ge VSs remain slightly tensile-strained ($\varepsilon = +0.26\%$) even after thermal annealing at 800 °C, which is attributed to the difference in the thermal expansion coefficients between Ge and Si [39,

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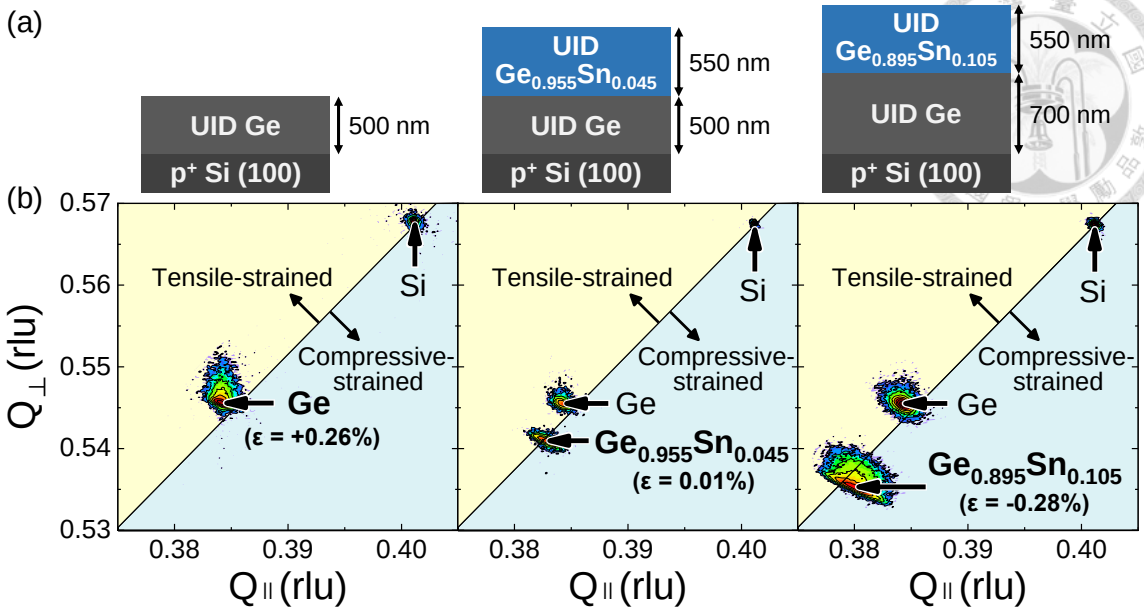

Fig. 2-5 (a) Epitaxial structures of the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ films and (b) the corresponding (224) high-resolution reciprocal space mapping (HRRSM) contours.

43]. The strains (Sn fractions) of the GeSn films were extracted as +0.01% (4.48 at%) and –0.28% (10.53 at%), respectively. The residual compressive strain in the GeSn layer increases with increasing Sn fraction, which is consistent with the results from other studies: relaxation rate of GeSn films decreases as the Sn fraction increases, even when the film thickness far exceeds its critical thickness [44, 45].

Compositions of the Ge(Sn) epitaxial structures were studied using scanning electron microscope (SEM) imaging by backscattered electrons (BSEs) and energy-dispersive X-ray spectroscopy (EDXS) (Fig. 2-6). Clear boundaries between the Si, Ge, and GeSn layers were identified from the difference in brightness of the SEM images (Fig. 2-6 (a) and (e)), because atoms with higher atomic numbers, i.e., Ge or Sn, appear brighter when BSEs are used for imaging [46]. The EDXS mapping results coincide with the SEM results: the regions with strong X-ray signals corresponding to the Si K-series (Fig. 2-6 (b) and (f)), Ge K-series (Fig. 2-6 (c) and (g)), and Sn L-series (Fig. 2-6 (d) and (h)) overlap with the darkest region, the second darkest region, and the brightest region in the SEM

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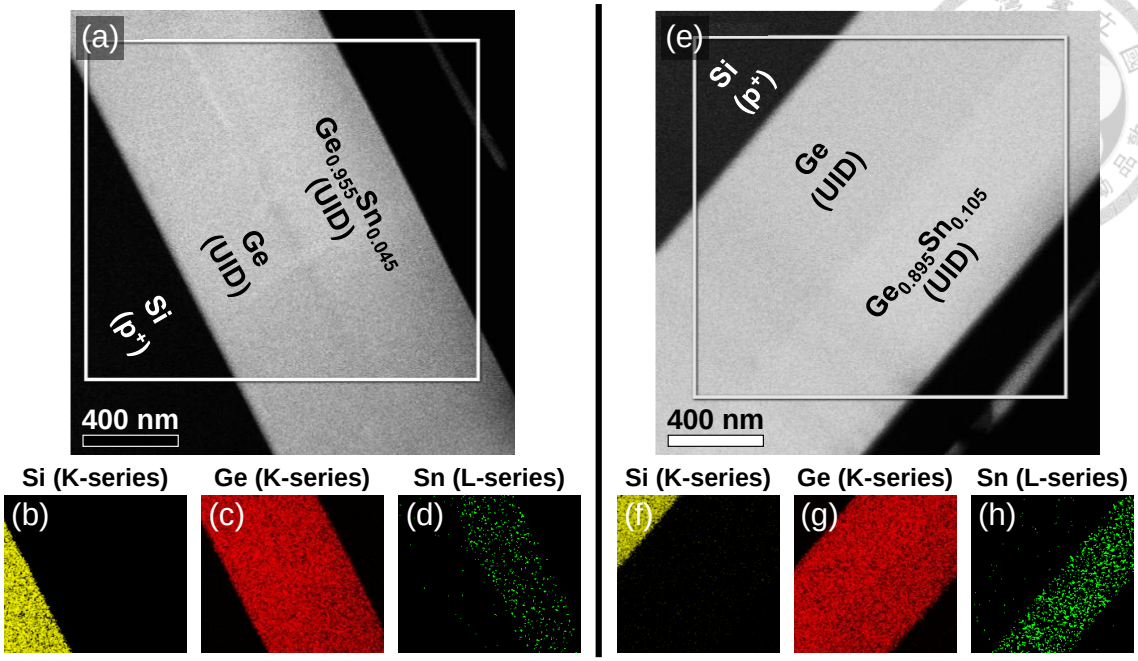

Fig. 2-6 Scanning electron microscope (SEM) images by backscattered electrons (BSEs) of the (a) $Ge_{0.955}Sn_{0.045}$ and (e) $Ge_{0.895}Sn_{0.105}$ epitaxial structures. Energy-dispersive X-ray spectroscopy (EDXS) mapping of the white squares in (a) and (e) showing (b)(f) Si, (c)(g) Ge, and (d)(h) Sn atom distributions.

images, respectively.

Crystallinity of the GeSn epitaxial structures were studied under transmission electron microscope (TEM) (Fig. 2-7). The defective regions are confined to the bottom of the Ge and GeSn layers (Fig. 2-7 (a) and (d)) thanks to the H_2-annealing after Ge deposition [27, 39] as well as the large thicknesses of the GeSn layers to keep the surface regions away from the misfit and threading dislocations near the Ge/GeSn interfaces [45]. Clear atomic structures were observed near the surface of the GeSn layers (Fig. 2-7 (b) and (e)), and thus high crystallinity is expected in the MOSFET inversion layers. Moreover, regular patterns of distinct bright spots were observed from the diffraction patterns near the surface of the GeSn layers (Fig. 2-7 (c) and (f)). This indicates that the films near the surface are single crystalline [47].

Lastly, surface morphology of the GeSn epitaxial structures were characterized using atomic force microscope (AFM). Randomly oriented hills and valleys were observed on

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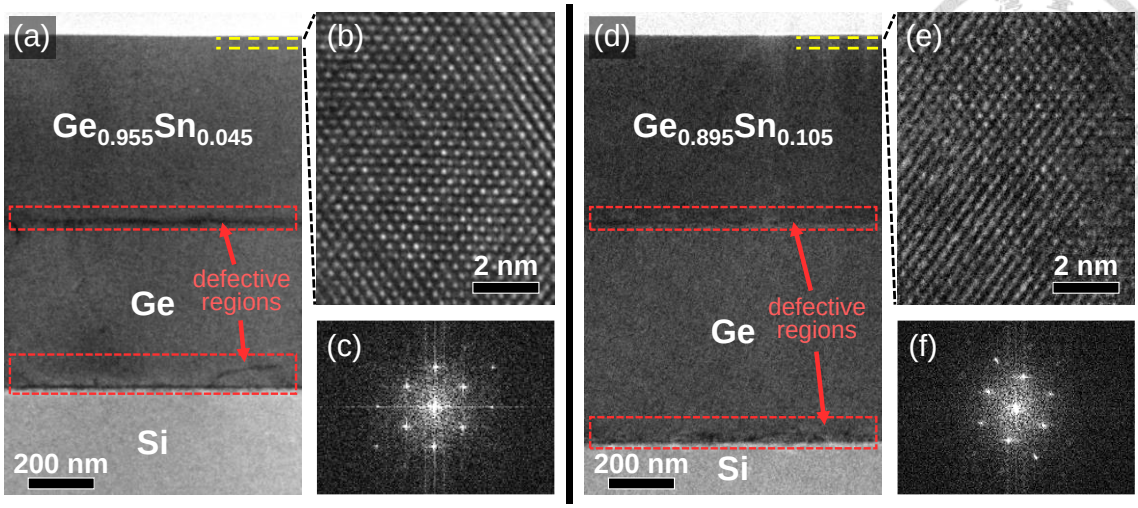

Fig. 2-7 (a)(d) Cross-sectional high-resolution transmission electron microscope (HRTEM) images, (b)(e) the near-surface cross-sectional HRTEM images, and (c)(f) the near-surface spot diffraction pattern of the $Ge_{0.955}Sn_{0.045}$ and $Ge_{0.895}Sn_{0.105}$ epitaxial structures.

the surface of the Ge epitaxial structure (Fig. 2-8 (a)), which is a feature associated with the threading dislocations near the Ge/Si interface [45]. A crosshatch pattern with two orthogonal sets of ridges and trenches were observed on the surface of the $Ge_{0.955}Sn_{0.045}$ epitaxial structure (Fig. 2-8 (b)), which is attributed to the nucleation of misfit dislocations at the Ge/GeSn interface as a result of strain-relaxation [45, 48]. The root-mean-square (RMS) surface roughness of the Ge and $Ge_{0.955}Sn_{0.045}$ epitaxial structures is 2.94 nm and 2.85 nm, respectively (Fig. 2-8 (a) and (b)). The RMS value of the $Ge_{0.895}Sn_{0.105}$ epitaxial

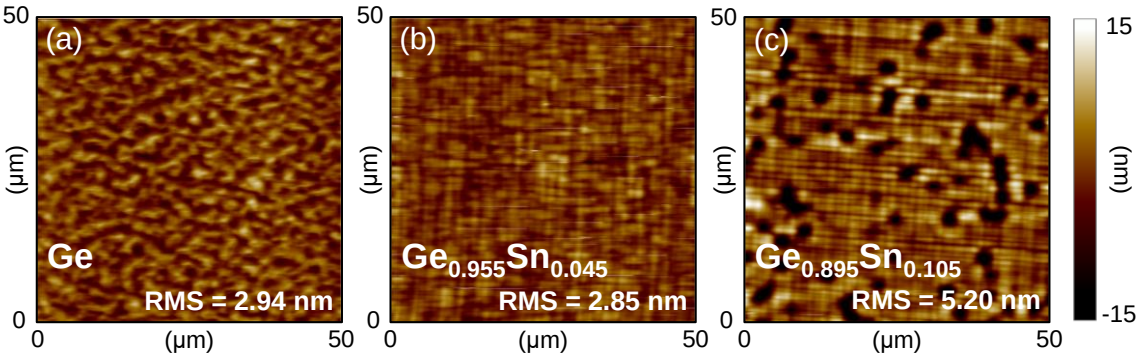

Fig. 2-8 Atomic force microscope (AFM) images of the surface of the (a) Ge, (b) $Ge_{0.955}Sn_{0.045}$, and (c) $Ge_{0.895}Sn_{0.105}$ epitaxial structures.

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structure increases to 5.20 nm due to a more pronounced crosshatch pattern and the formation of circular pits on the surface (Fig. 2-8 (c)). This may be due to an increased misfit dislocation density at the Ge/GeSn interface and the generation of half-loops in the GeSn film [45] due to a larger lattice mismatch between the Ge VS and the GeSn film compared to the Ge and $Ge_{0.955}Sn_{0.045}$ epitaxial structures.

2.2.2 Device Fabrication

The gate-first fabrication process of Ge(Sn) n-MOSFETs is outlined as follows (Fig. 2-9 (a)). After the Ge(Sn) epitaxial growth, square coupons were diced from the wafers and subjected to a degreasing process by immersing in acetone, methanol, and isopropanol alcohol with sonication [49]. Then, the coupons were dipped in diluted hydrofluoric acid (HF, 1:25) and diluted hydrochloric acid (HCl, 1:10) to remove native oxides and organic residuals, respectively [11, 22, 49]. 15-nm aluminum oxide (Al_2O_3) and 100-nm of titanium nitride (TiN) were subsequently deposited as the gate stacks using plasma-enhanced atomic layer deposition (PEALD) and sputtering, respectively. After that, alignment marks and gate stacks were defined using Cl_2-based anisotropic reactive-ion etching

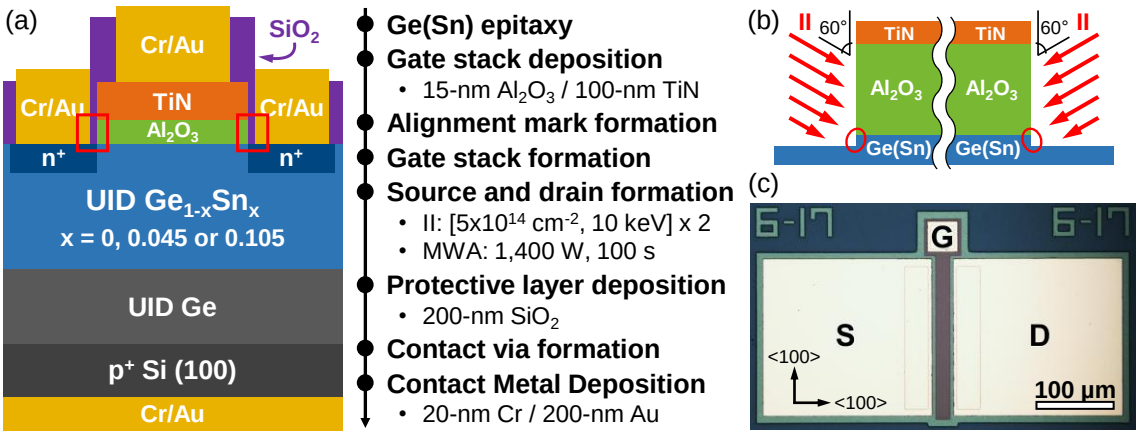

Fig. 2-9 (a) A schematic of the device structure and the process flow of Ge(Sn) n-MOSFETs. (b) Enlarged portions of the red squares in (a) showing the angle of the 2-steps ion implantation (II). (c) An optical microscope (OM) image of a Ge(Sn) n-MOSFET. Crystallography directions <100> are labeled.

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(RIE), where the gate stacks were slightly over-etched (a thin layer of the Ge(Sn) layer is removed) to ensure a complete removal of the Al_2O_3 layers, thereby preventing dopants from being blocked during ion implantation.

Then, phosphorous (^{31}P) ion implantation (II) and microwave annealing (MWA) were carried out to form the source and drain region. Note that MWA, rather than rapid thermal annealing (RTA), was selected for dopant activation to better preserve crystal quality and the oxide/Ge(Sn) interface quality [11, 22]. The II process was done in two steps, each with an azimuth angle (rotation) differing by 180° and a zenith angle (tilt) set to 60° (Fig. 2-9 (b)) to eliminate the potential underlapping between the source/drain and the gate stacks (encircled in Fig. 2-9 (b)) due to the shadowing effect [50] and the "neck" formed due to the over-etching of the gate stacks. The underlapped regions, which were not implanted and not controlled by the gate, create high-energy barriers between the source and the channel. This results in large series resistances in the device and should therefore be avoided.

Finally, a layer of 200-nm silicon dioxide (SiO_2) was deposited as a protective layer, with contact vias formed by wet etching using buffer oxide etchant (BOE). The devices were finished by depositing 20-nm of Chromium (Cr) and 200-nm of Gold (Au) followed by a lift-off process. The optical microscope (OM) image of the Ge(Sn) n-MOSFET is shown in Fig. 2-9 (c), where the channel direction (transport direction) is <100>. A deviation from a transport direction of <100> could result in a change in electron mobility due to the anisotropy of the constant energy surface centered at the L symmetry point. Devices fabricated on (110) substrates could exhibit a more pronounced direction-dependent electron mobility due to a lower symmetry in valley configuration [51]. However, due to the isotropy of the constant energy surface centered at the Γ-point, electron mobility in direct-bandgap Ge(Sn) devices is expected to show much weaker dependence on

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channel direction. This opens up a new way to probe the indirect-to-direct bandgap transition in GeSn alloys (Chapter 4.2).

2.2.3 Device Characterization

Using the split C-V method, inversion carrier density (N_{inv}) and effective mobility (μ_{eff}) of the n-MOSFETs can be obtained [25]. The N_{inv} is derived from the normalized gate-to-channel capacitance (C_{GC}), obtained through split C-V measurements using a C-V meter configured as follows: the high-voltage terminal (which forces a bias superimposed by a sinusoidal signal) is connected to the gate, while the low-voltage terminal (which senses current) is connected to the source and drain [25] (Fig. 2-10 (b) and (c)). The substrate of the n-MOSFETs must be grounded and isolated from the low terminal of the C-V meter. In this configuration, the C-V meter only detects the capacitive response from minority (inversion) carriers (electrons in n-MOSFETs) supplied through both the

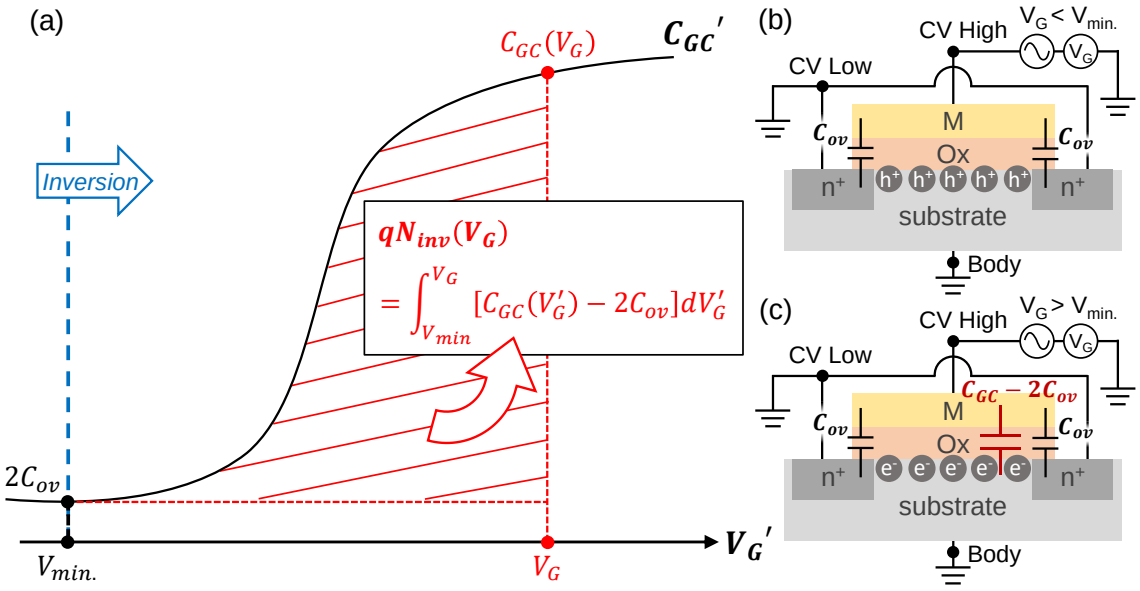

Fig. 2-10 (a) A schematic of the normalized gate-to-channel capacitance (C_{GC}) vs. gate voltage (V_G) of an n-MOSFET as well as the derivation of inversion carrier density (N_{inv}) and effective mobility (μ_{eff}). Schematics of the biasing configuration and capacitance components measured in (b) the accumulation or depletion regime ($V_G < V_{min}$) and (c) the inversion regime ($V_G > V_{min}$).

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source and drain terminals thanks to the rectifying characteristics of the source-to-substrate and drain-to-substrate n^+/p junctions.

When the device is biased in the accumulation or depletion regime ($V_G < V_{min.}$), the channel is disconnected from the source and drain due to high energy barriers between them (Fig. 2-10 (b)). Therefore, the C-V meter reads only twice the overlap capacitance ($2C_{ov}$) [25], with a slight V_G dependence due to the presence of gate-induced drain leakage (GIDL) [52] (Fig. 2-10 (a)). As V_G increases, the device is gradually biased into the inversion regime ($V_G > V_{min.}$), where the energy barrier between the channel and the source/drain is progressively lowered, allowing more carriers to be injected from the source/drain into the channel (Fig. 2-10 (c)). As a result, the capacitance increases with V_G and eventually saturates to a value close to the oxide capacitance (Fig. 2-10 (a)) [25]. Since the increase in C_{GC} beyond $2C_{OV}$ is contributed by electrons in the inversion layer, the inversion charge density (qN_{inv}) is obtained by integrating C_{GC} offset by $2C_{OV}$ ($C_{GC} - 2C_{OV}$) with respect to V_G [10, 22] (Fig. 2-10 (a)).

The drain current (I_D) in a long-channel n-MOSFET is expressed as the sum of drift and diffusion currents [25]:

$$I_D = qN_{inv}\mu_{eff}V_{DS}\frac{W}{L} - WkT\mu_{eff}\frac{dN_{inv}}{dx}, \tag{2-1}$$

where V_{DS}, W, L, and x are drain-to-source bias, device width, device length, and the coordinate along the channel direction, respectively. The diffusive term (second term) can be dropped from Equation (2-1) when the gradient of N_{inv} along the channel direction is small, i.e., when the applied V_{DS} is small and the device is biased in the strong inversion regime ($V_G > V_{th}$ (threshold voltage)) [25], allowing μ_{eff} to be obtained as [30]

$$\mu_{eff}(\psi_s) = \frac{L}{W}\frac{I_D(\psi_s)}{V_{DS}\cdot qN_{inv}(\psi_s)}, \tag{2-2}$$

where ψ_s is the surface band-bending at the oxide/semiconductor surface. Given that ψ_s

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is the change in surface potential beyond that at flat-band condition, ψ_s can be expressed as a function of $V_G - V_{FB}$ (flat-band voltage) [30]. Moreover, ψ_s can also be expressed as a function of $V_G - V_{th}$ using the relation between V_{th} and V_{FB} [30]:

$$V_{th} = V_{FB} + 2\psi_B + \frac{\sqrt{4\epsilon_s q N_a \psi_B}}{C_{ox}}, \tag{2-3}$$

where ψ_B, ϵ_s, and N_a are bulk Fermi potential, bulk dielectric constant, and bulk doping concentration, respectively. As a result, μ_{eff} (Equation (2-2)) can be recast into a function of an experimentally measurable quantity $V_G - V_{th}$, i.e., the overdrive voltage (V_{OV}):

$$\mu_{eff}(V_{OV}) = \frac{L}{W}\frac{I_D(V_{OV})}{V_{DS} \cdot qN_{inv}(V_{OV})}. \tag{2-4}$$

The necessity to account for the V_{th} in Equation (2-4), i.e., to express μ_{eff} as a function of V_{OV} (or $V_G - V_{th}$) instead of V_G alone, arises because I_D and N_{inv} are obtained from two independent measurements (transfer I-V and split C-V measurements), which may involve a V_{th} shift between them.

In fact, V_{th} shifts between measurements, similar to the negative/positive bias temperature instability (NBTI/PBTI) in Si MOSFETs [53, 54], were constantly observed. This is attributed to the poorer Al_2O_3/Ge(Sn) interface quality [55] compared to the SiO_2/Si interface [31], resulting in prominent generation or charging of interface traps during a gate bias stress [53, 54], and consequently, a non-negligible V_{th} shift. To reliably extract μ_{eff}, it is necessary to exclude the effect of V_{th} shift by offsetting V_G with V_{th} (Equation (2-4)). However, V_{th} cannot be extracted from the C_{GC}-V_G curve. The only way to obtain N_{inv} as a function of V_{OV} is to eliminate the V_{th} shift between the transfer I-V measurement and the split C-V measurement, ensuring that the V_{th} extracted from the transfer I-V curves can be used as the V_{th} for the C_{GC}-V_G curves.

To eliminate the V_{th} shift between measurements, it is necessary to fix the maximum gate bias ($V_{G,\,max.}$) and the V_G sweep durations, because V_{th} increases with $V_{G,\,max.}$ and the

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sweep duration of the gate bias [54] (Fig. 2-11 (a)). In addition, when measuring a new device or measuring at a new temperature, V_{th} will shift in the first few rounds of measurement even if $V_{G,\,max.}$ and V_G sweep durations are held constant (Fig. 2-11 (b)). This is possibly due to the interface trap generation [53, 54] or the variation of charged interface trap density with temperature [31]. It usually takes several rounds of V_G sweeps before the V_{th} is stabilized. Note that the V_{th} in this study was extracted using the transconductance change method, where V_{th} is derived as the gate voltage corresponding to the maximum of the second derivative of the transfer I-V curves [56]. This approach ensures that the extracted V_{th} corresponds to a surface band-bending of $2\psi_B$ [56], which is consistent with the definition in Equation (2-3).

A standardized measurement procedure was established accordingly (Fig. 2-11 (c)). Before starting the "main" measurement, several rounds of calibration V_G sweeps were performed with a fixed $V_{G,\,max.}$ and a fixed V_G sweep duration until the V_{th} shift between successive transfer I-V measurements became negligible. After that, the "main" transfer

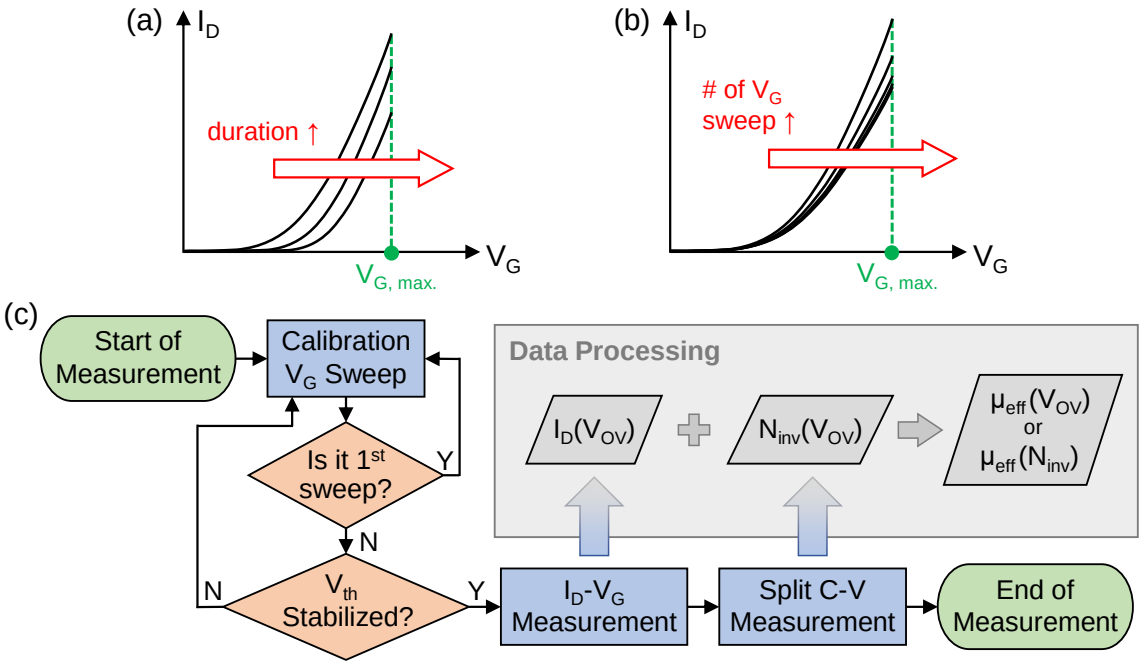

Fig. 2-11 Schematics of V_{th} shift caused by the increase of (a) V_G sweep durations and (b) the number of V_G sweeps. (c) A schematic of the standard measurement procedure.

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I-V and split C-V measurements were performed with $V_{G,\,max.}$ and V_G sweep durations set to values identical to those used in the calibration V_G sweeps. This ensures that the V_{th} of both the I-V and C-V measurements remain the same. Finally, μ_{eff} was extracted by plugging the acquired data into Equation (2-4).

While fixing $V_{G,\,max.}$ between measurements is easy, maintaining consistency in the V_G sweep durations is more challenging. To achieve the latter, the time spent at each V_G step within the entire V_G sweep must be kept identical across measurements, because the V_G sweep duration is the sum of all individual V_G step times (Fig. 2-12). To ensure that each V_G step time is identical across every 4-terminal (to monitor source, drain, body, and gate current/voltage) transfer I-V measurement, three Keysight B1500A high-resolution source measure units (SMUs) and an independent Keysight B2901A SMU were synchronized using a customized MATLAB® program for precise V_G step timing (Fig. 2-13 (a)). This program also enabled precise V_G step timing across every split C-V measurement, which require controlling a Keysight E4980A LCR meter that lacks a built-in timing function for each V_G step (Fig. 2-13 (b)). The timing-sensitive parts of the code were executed on parallel CPU cores to avoid irregular system interruptions and delays in the timing function. These approaches ensure precise timing across measurements, and consequently, the reliability of the extracted μ_{eff}.

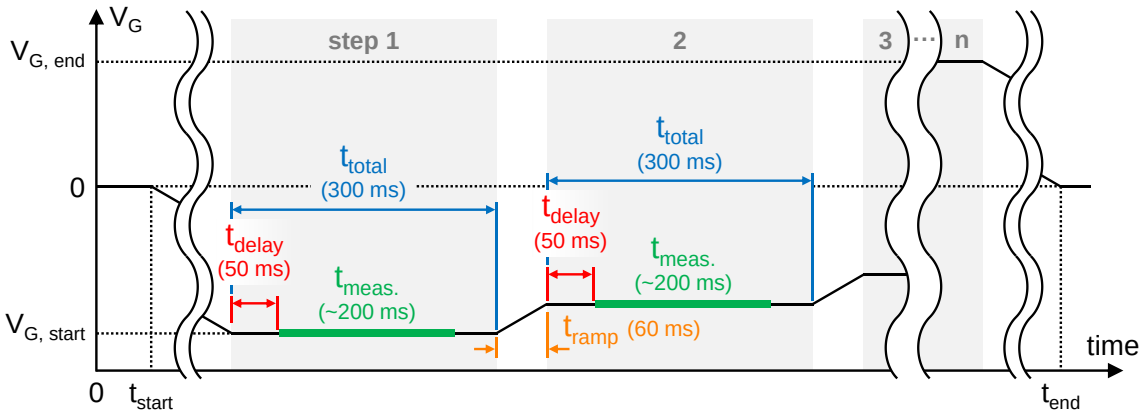

Fig. 2-12 A schematic of the timing of each V_G step during a single measurement.

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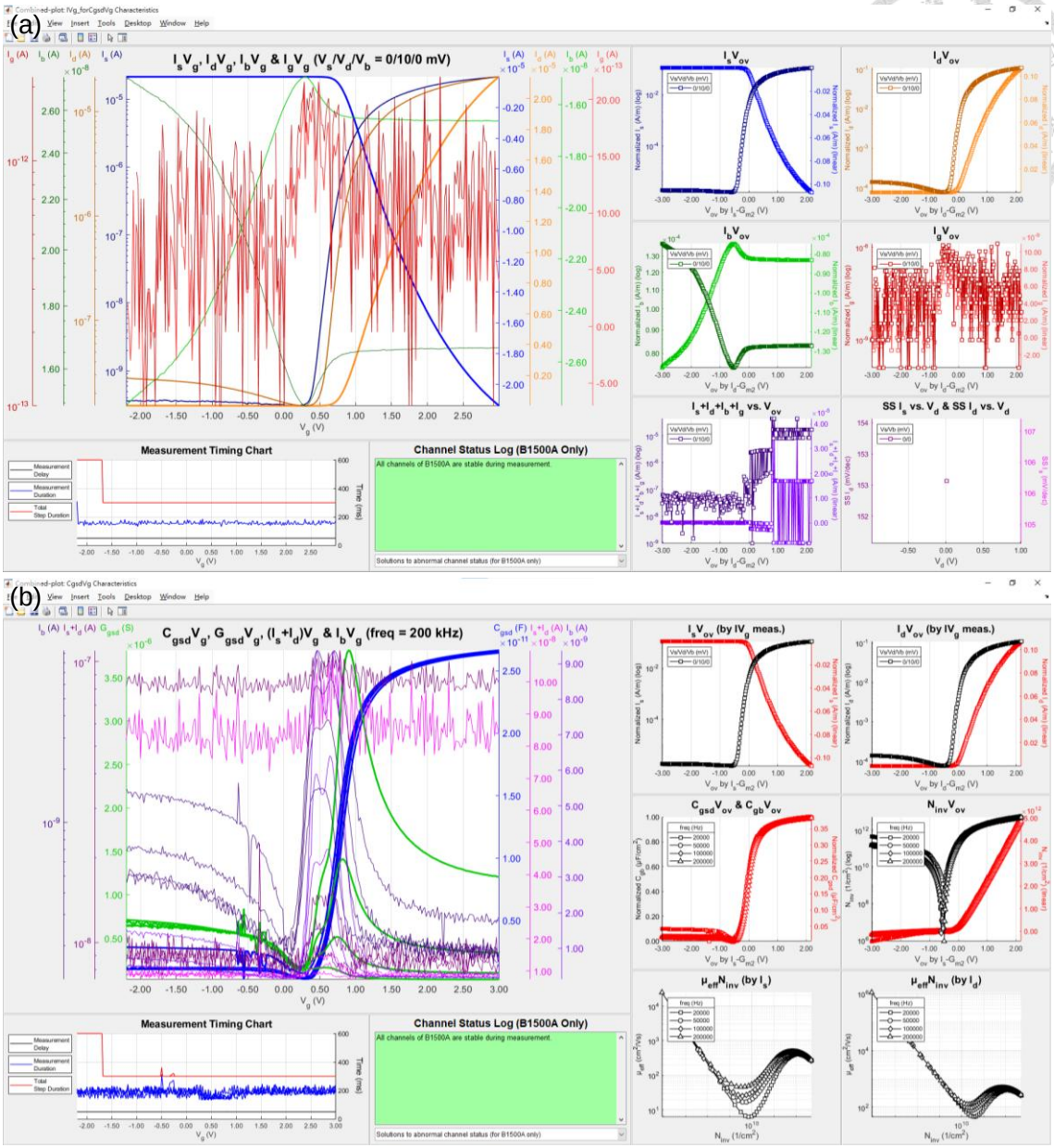

Fig. 2-13 Screenshots of the monitoring panel of the MATLAB® program during the (a) transfer I-V and (b) split C-V measurement of the Ge n-MOSFET at 250 K.

2.3 Room-Temperature Device Characteristics

The channel dimensions of the Ge(Sn) n-MOSFETs are chosen to minimize the influence of parasitic effects on the extracted μ_{eff}. When the surface is depleted or weakly inverted, the electron supply from the source/drain is very limited. The electrons supplied through the generation-recombination (GR) processes near the surface, which are not de-

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tected by the CV meter (Fig. 2-10 (b)), may outnumber those supplied from the source/drain [57]. This leads to deviation in the measured C_{GC} and, consequently, in the extracted μ_{eff} [57]. To minimize the error in the extracted μ_{eff}, the channel length (L) should be chosen as small as possible to minimize the total number of traps in the surface depletion region [58] and at the oxide/semiconductor interface [57] that assist the near-surface GR processes.

Moreover, L should be at least 10 – 20 times the depletion width of the source-to-substrate and drain-to-substrate n^+/p junctions to mitigate the channel area reduction when the surface is weakly inverted (Fig. 2-14), because such reduction introduces errors in the measured C_{GC}, and consequently, the extracted μ_{eff} [57]. To a first-order approximation, the depletion width of the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs can be estimated using that of the abrupt, one-sided n^+/p junction at zero bias [30] as 299, 282, and 250 nm, respectively. By choosing L to be 20 μm, the error in the extracted μ_{eff} can be reduced to ~ 5 % [59]. Lastly, the channel width (W) is chosen as 200 μm (W/L = 10), ensuring that the non-uniform electron flow induced by fringing gate fields is negligible.

2.3.1 Transfer I-V Characteristics

The normalized drain current (I_D), source current (I_S), and body current (I_B) of the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs are plotted against overdrive voltage

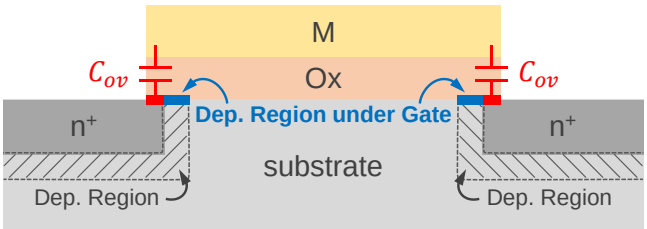

Fig. 2-14 A schematic showing the reduction of channel area due to the junction depletion regions under the gate region.

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(V_{OV}) to rule out the effect of threshold voltage (V_{th}) variation across devices (Fig. 2-15). The effect of gate leakage (I_G) is neglected since it is much lower (< 10^{-8} A/m) than I_D, I_S, and I_B (Fig. 2-13 (a)). The drain-to-source bias (V_{DS}) is maintained at a low value of 10 mV with the source and body grounded to meet the prerequisites of the split C-V method (Chapter 2.2.3).

For all devices, as V_{OV} increases above –0.5 V, both I_D and I_S increase due to the formation of the inversion channel [30], while I_B remains relatively constant with V_{OV}, indicating that I_B originates from parasitic leakages that are not modulated by the gate potential (Fig. 2-15). Since $I_D \approx I_B$ when $V_{OV} < –0.5$ V and $I_D = I_S + I_B$ (Fig. 2-16), I_B is approximately the off-state leakage on the drain side. As V_{OV} decreases from –0.5 V to –2 V, a very slight increase in I_D was observed across all devices, which is attributed to gate-induced drain leakage (GIDL) [22]. With the aid of MWA, dopant diffusion was suppressed, resulting in small gate-to-drain overlaps and small GIDL [22]. Consequently, the effect of GIDL on I_D is barely visible since it is obscured by the larger drain-to-substrate junction leakage, because I_D at $V_{OV} < –0.5$ V comprises both junction leakage and GIDL in long-channel n-MOSFETs [60]. The effect of gate-induced source leakage (GISL) on I_S is negligible, too. Therefore, the off-state leakage, either on the source or drain side, consists primarily of the junction leakage. Moreover, the orders-of-magnitude

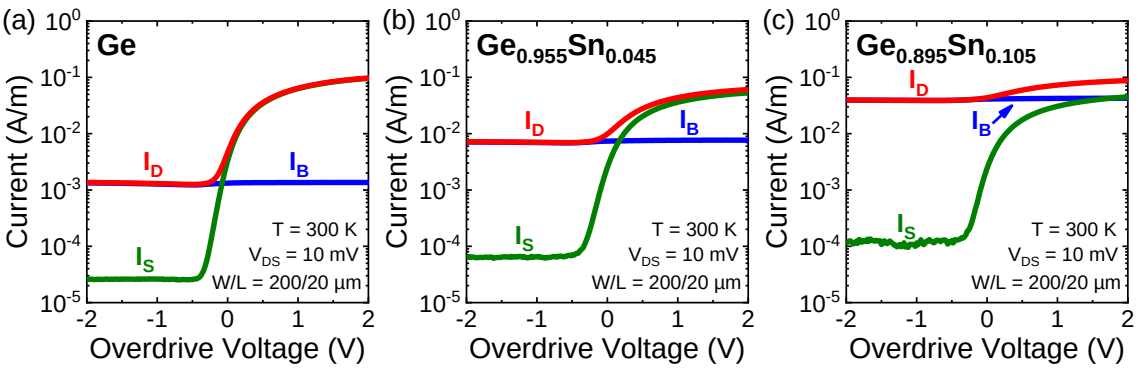

Fig. 2-15 Normalized drain current (I_D), source current (I_S), and body current (I_B) vs. overdrive voltage (V_{OV}) of the (a) Ge, (b) $Ge_{0.955}Sn_{0.045}$, and (c) $Ge_{0.895}Sn_{0.105}$ n-MOSFETs at 300 K.

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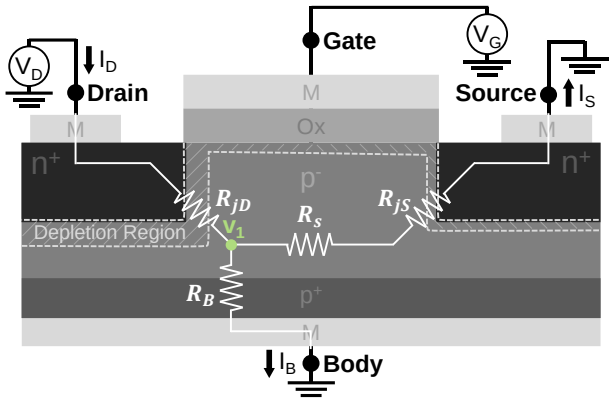

Fig. 2-16 Schematics showing the polarity of current at each terminal and the internal resistances.

difference in off-state leakage between the source and drain sides can be attributed to the larger bias across the drain-to-substrate junction. This likely due to the heavily-doped p^+-Si substrate, which significantly reduces the resistance from the drain to the body (R_B) compared to that from the drain to the source ($R_s + R_{jS}$), thereby pulling the node v_1 close to ground (Fig. 2-16).

The off-state leakage at $V_{OV} = -2$ V (I_{OFF*}), off-state current (I_{OFF}, I_S or I_D at $V_{OV} \sim -0.5$ V) and on-state current (I_{ON}, I_S or I_D at $V_{OV} = 2$ V) are extracted from Fig. 2-15 and plotted against Sn fraction (Fig. 2-17). On both the source and drain sides, the I_{OFF*} and I_{OFF} increase with Sn fraction (Fig. 2-17 (a) and (b)), which is primarily attributed to the increase in junction leakage with increasing Sn fraction due to a decreasing bandgap en-

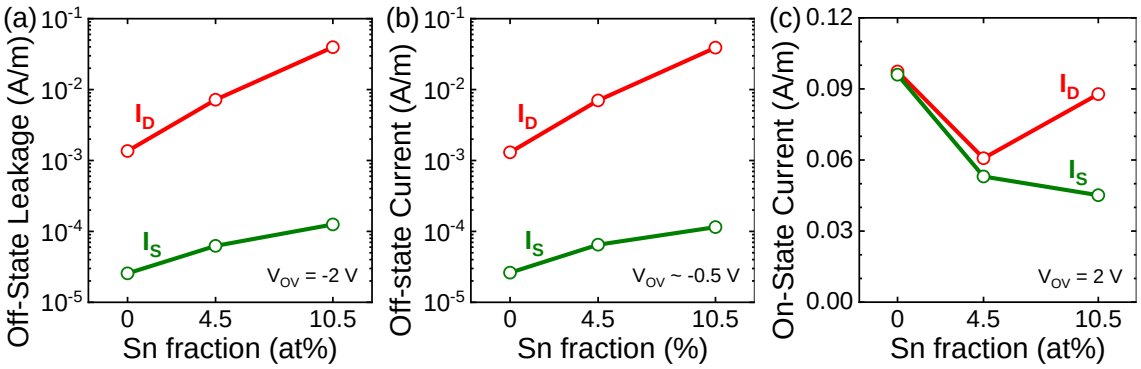

Fig. 2-17 (a) The off-state leakage at $V_{OV} = -2$ V (I_{OFF*}), (b) off-state current (I_{OFF}, I_S or I_D at $V_{OV} \sim -0.5$ V), and (c) on-state current (I_{ON}, I_S or I_D at $V_{OV} = 2$ V) vs. Sn fraction of the Ge(Sn) n-MOSFETs at 300 K.

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ergy [61, 62]. The Sn-fraction dependence of I_{ON} on the source and drain sides is, however, different (Fig. 2-17 (c)). On the source side, I_{ON} decreases with increasing Sn fraction, which could be attributed to an enhanced alloy scattering [21, 63], because carrier scattering degrades mobility, and consequently, I_{ON}. On the drain side, I_{ON} exhibits a V-shape dependence on Sn fraction, where the upturn at [Sn] = 10.5 at% is attributed to the much higher I_{OFF} on the drain side compared to that on the source side (Fig. 2-17 (b)). This is because the I_{OFF} on the drain side in the $Ge_{0.895}Sn_{0.105}$ device contributes approximately 40% to its I_{ON}, thereby obscuring its "true" Sn-fraction dependence of I_{ON}.

The higher I_{OFF} on the drain side also results in orders-of-magnitude differences in on-off current ratio (I_{ON}/I_{OFF}) and minimum subthreshold swing (SS_{min}) between the source and drain sides (Fig. 2-18 (a) and (b)). The former difference occurs since I_{OFF} on the two sides differ by orders of magnitude (Fig. 2-17 (b)), whereas I_{ON} on the two sides are of the same order (Fig. 2-17 (c)); the latter difference occurs since the high I_{OFF} obscures the subthreshold characteristics of I_D, making the subthreshold slope much smaller than the "true" one (Fig. 2-15). Note that the SS_{min} of all devices are above the Boltzmann limit (Fig. 2-18 (b)), possibly due to the finite depletion capacitance and interface trap capacitance [30, 31].

In Si n-MOSFETs, I_{OFF} is negligibly small. Therefore, the only transport mechanism

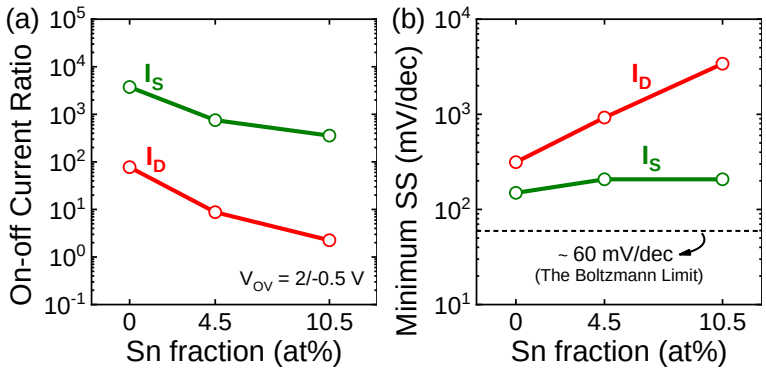

Fig. 2-18 The (a) on-off current ratio (I_{ON}/I_{OFF}) and (b) minimum subthreshold swing (SS_{min}) vs. Sn fraction of the Ge(Sn) n-MOSFETs at 300 K.

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is the drift of electrons along the inversion channel [25]. However, for the Ge(Sn) n-MOSFETs, I_{OFF} is too large to be neglected. Parasitic transports, such as GIDL and junction leakage, should be investigated, because they substantially distort the C_{GC}-V_{OV} characteristics (Chapter 2.3.2). To do so, models of the DC carrier transport mechanisms in the Ge(Sn) n-MOSFETs in the transfer I-V configuration are proposed (Fig. 2-19 to Fig. 2-21) based on the experimental results and analyses (Fig. 2-15 to Fig. 2-18).

In the accumulation regime (V_{OV} = –2 V), the drain-to-substrate n^+/p junction is reverse-biased since the drain is applied with a higher bias (10 mV) compared to the substrate (grounded) (Fig. 2-19). Due to the small bandgap energy and high trap density in Ge(Sn), Shockley-Read-Hall (SRH) and trap-assisted tunneling (TAT) GR processes are highly active in junction depletion regions [64], making GR current the dominant transport mechanism in a Ge(Sn) p-n junction under a small bias [61, 65]. Therefore, electron-hole pairs are generated within the depletion region of the drain-to-substrate n^+/p junction and are subsequently swept toward the n^+-side and p-side by the electric field [30, 66], establishing a reversed-biased current (I_R) (①). The current path is completed

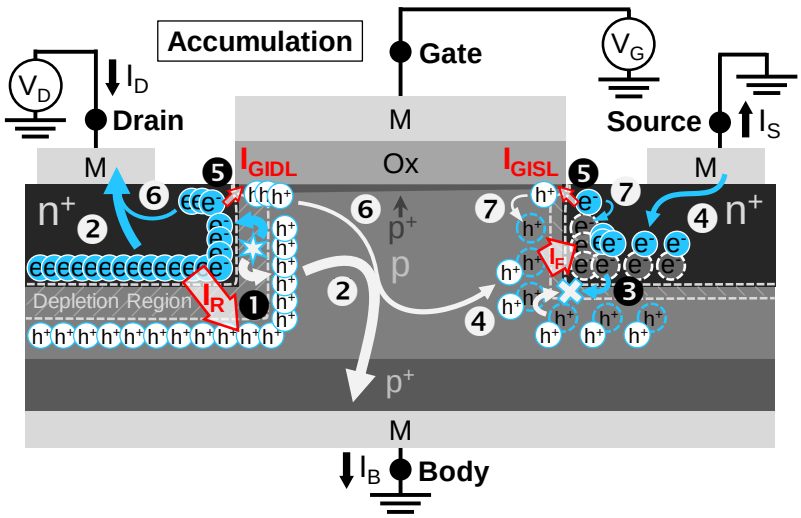

Fig. 2-19 Schematics of the DC carrier transport mechanisms in the Ge(Sn) n-MOSFETs during the transfer I-V measurements in the accumulation regime (V_{OV} = –2 V). Excess/Deficient carriers are represented by solid/hollow circles; electron/hole/total currents are represented by blue/white/red arrows.

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by discharging the excess electrons and holes via the n^+ drain contact (ohmic for electrons) and the p^+ body contact (ohmic for holes), respectively (②).

In contrast, the source-to-substrate junction should be forward-biased to support the experimentally observed off-state source leakage (I_{OFF*}), which flows out of the source terminal (Fig. 2-17 (a)). Consequently, electrons and holes diffuse across the junction and recombine within the depletion region [30, 66], establishing a forward-biased current (I_F) and resulting in electron and hole deficiency on the n^+-side and p-side, respectively (③). Since the source and body terminals are held at the same potential, no net current flows between them. Therefore, the current path is completed by replenishing the electron and hole deficiency through electron inflow from the n^+ source contact and excess hole current originating from the drain-to-substrate junction, respectively (④).

Lastly, the large negative gate voltage in the accumulation regime and the small bandgap energy of Ge(Sn) leads to gate-induced drain leakage (I_{GIDL}) and, possibly, gate-induced source leakage (I_{GISL}), where the transport mechanism is band-to-band tunneling [67] or trap-assisted tunneling [68]. In these processes, electrons tunnel to the n^+-side and generate holes on the p-side (⑤). The current paths are completed by either discharging excess electrons and holes via the n^+ drain and p^+ body contacts, respectively (⑥), or replenishing the carrier deficiency induced by ③ (⑦).

The DC carrier transport mechanisms and internal current paths in the depletion regime ($V_{OV} \sim -0.5$ V) and the strong inversion regime ($V_{OV} = 2$ V) are identical to those in the accumulation regime, except for some difference. Specifically, in the depletion regime, GIDL and GISL are absent (Fig. 2-20), because the electric field at the gate-to-drain and gate-to-source overlaps are much smaller compared to those in the accumulation regime, respectively; in the strong inversion regime ($V_{OV} = 2$ V), GIDL and GISL are also absent for the same reason, but there exists an additional electron transport along the in-

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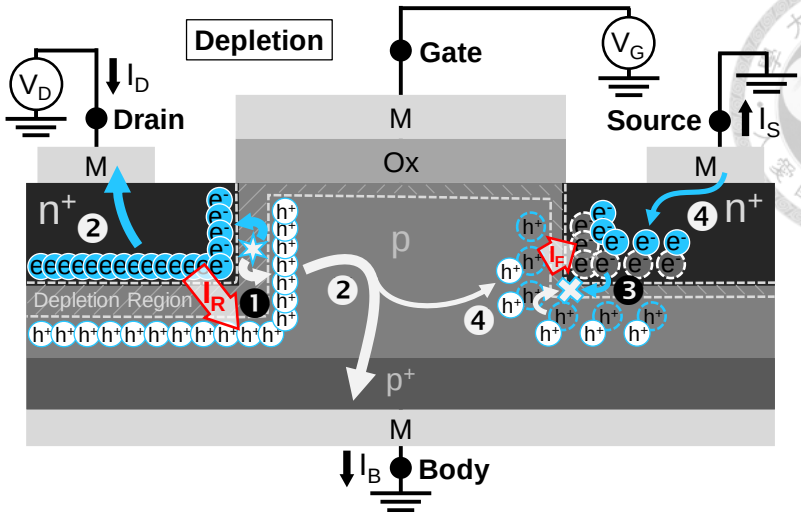

Fig. 2-20 Schematics of the DC carrier transport mechanisms in the Ge(Sn) n-MOSFETs during the transfer I-V measurements in the depletion regime (V_{OV} ~ –0.5 V).

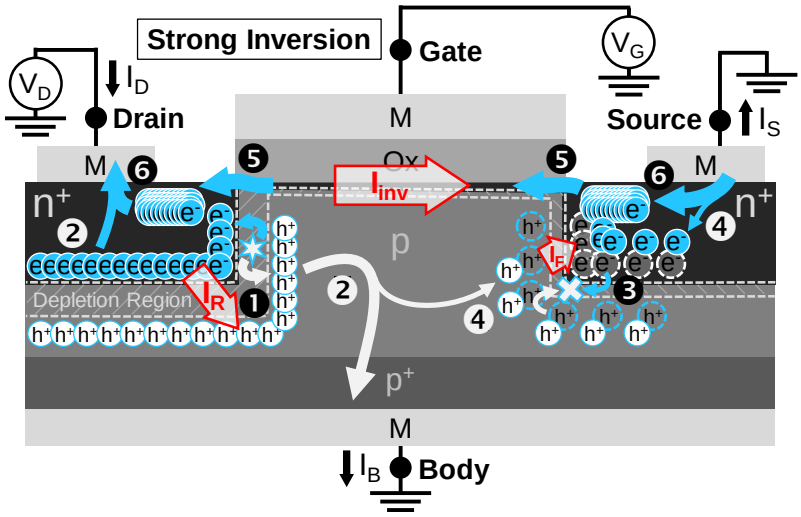

Fig. 2-21 Schematics of the DC carrier transport mechanisms in the Ge(Sn) n-MOSFETs during the transfer I-V measurements in the strong inversion regime (V_{OV} = 2 V).

version channel (⑤ and ⑥) due to the heavily inverted surface (Fig. 2-21).

2.3.2 Split C-V Characteristics

The normalized gate-to-channel capacitance (C_{GC}) of the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs is plotted against V_{OV} to rule out the effect of V_{th} variation

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across devices (Fig. 2-22). The C_{GC}-V_{OV} curves exhibit asymmetric V-shapes with different heights at both positive (inversion) and negative (accumulation) gate biases. In the strong inversion regime (V_{OV} = 2 V), all C_{GC}-V_{OV} curves reach their maxima due to the presence of inversion channel [25]. During the transition into the depletion regime (V_{OV} ~ –0.5 V), a drastic reduction in C_{GC} with decreasing V_{OV} is observed across all C_{GC}-V_{OV} curves, which is attributed to the depletion of the inversion channel [25]. As the device is further biased into the accumulation regime (V_{OV} = –2 V), a pronounced increase in C_{GC} with a decreasing V_{OV} is observed across all C_{GC}-V_{OV} curves, deviating significantly from the conventional split C-V characteristics [25]. The potential causes are elaborated as follows.

The C_{GC} measured in the accumulation, depletion, and strong inversion regimes are extracted from Fig. 2-22 and plotted against the Sn fraction (Fig. 2-23). Because the Ge(Sn) n-MOSFETs are fabricated using a gate-first process, both gate-to-source and gate-to-drain overlaps are negligible. Thus, for conventional C_{GC}-V_{OV} curves, C_{GC} in the accumulation and depletion regimes are vanishingly small thanks to the current-rectifying characteristics of the source-to-substrate and drain-to-substrate n^+/p junctions (Chapter 2.2.3). This is, however, against the experimental results (Fig. 2-23 (a) and (b)), possibly due to the leaky junctions (Fig. 2-17 (a) and (b)) resulting from the smaller bandgap of

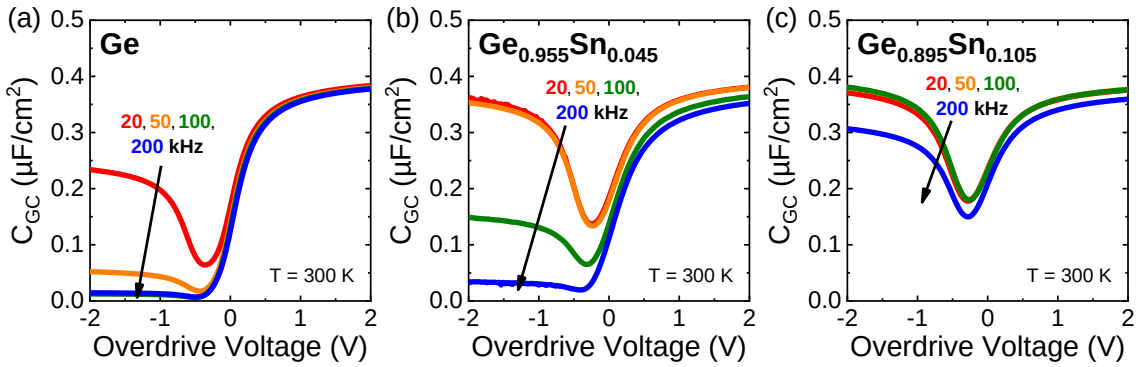

Fig. 2-22 Normalized gate-to-channel capacitance (C_{GC}) of the (a) Ge, (b) $Ge_{0.955}Sn_{0.045}$, and (c) $Ge_{0.895}Sn_{0.105}$ n-MOSFETs vs. V_{OV} measured with frequencies of 20, 50, 100, and 200 kHz at 300 K.

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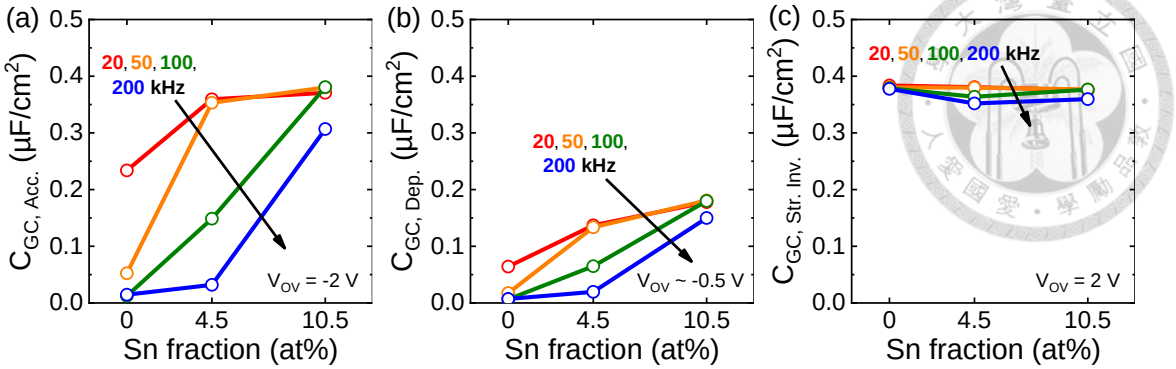

Fig. 2-23 C_{GC} vs. Sn fraction in the (a) accumulation, (b) depletion, and (c) strong inversion regimes of the Ge(Sn) n-MOSFETs measured with frequencies of 20, 50, 100, and 200 kHz at 300 K.

Ge(Sn) compared to Si [61]. The leaky junctions may lead to a non-negligible carrier transport between the source/drain and the substrate via the leaky junctions [66], allowing the source/drain to supply majority carriers (holes) to the surface and resulting in the non-vanishing C_{GC} in the accumulation and depletion regimes (Fig. 2-23 (a) and (b)). As the Sn fraction increases, the junctions become increasingly leaky (Fig. 2-17 (a) and (b)), which may lead to the corresponding increase in C_{GC} (Fig. 2-23 (a) and (b)). Besides, the junctions may be treated as resistors in series with the gate stack. As the frequency increases, the reactance X of the gate stack decreases relative to the junction resistance due to its capacitive nature ($X = 1/\omega C$), thereby reducing both the voltage drop V across the gate stack and the energy E stored in it ($E = CV^2/2$) [69]. This weakens the capacitive characteristic of the device, which may contribute to the decrease in C_{GC} with increasing frequency (Fig. 2-23 (a) and (b)).

In the strong inversion regime, C_{GC} reaches approximately 0.37 μF/cm^2 for all devices (Fig. 2-23 (c)). A dielectric constant of ~ 6.3 is extracted accordingly for the gate oxide (Al_2O_3), which is close to the reported value of ~ 6.5 [70]. Here, the minority carriers (electrons) are supplied to the surface through the channel. However, due to the leaky junctions, the minority carriers can also be supplied to the surface via the leaky junctions [57] and GR processes in the surface depletion region [71]. Because capacitance is a result

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of charge variation [52], C_{GC} is dependent on the supply of minority carriers through both the channel and the junction. Thus, the slight variation in C_{GC} with Sn fraction (Fig. 2-23 (c)) may be a result of the variation in both the I_{ON} and the I_{OFF}. Besides, both the channel and junctions may act as resistances in series with the gate stack. Similar to the behavior in the accumulation and depletion regimes, the capacitive behavior of the device is weakened as the frequency increases [69], which may contribute to the corresponding decrease in C_{GC} (Fig. 2-23 (c)). Since the aforementioned anomalies observed in the split C-V characteristics of the Ge(Sn) n-MOSFETs have not been reported elsewhere, the preceding arguments require validation, and the process of which is outlined in Fig. 2-24.

First, AC carrier transport mechanisms in Ge(Sn) n-MOSFETs under the split C-V configuration in the accumulation, depletion, and strong inversion regimes are proposed (①). Then, based on the proposed AC carrier transport mechanisms, equivalent small-signal circuit models are constructed (②). Analytical expressions for circuit capacitance C, which consists of two parameters C_0 and ω_c, are subsequently derived from the circuit models (③). Using a fitting procedure, the two parameters C_0 and ω_c are extracted from experimental data (④). A comparison between the expressions for C_0 and ω_c and the ex-

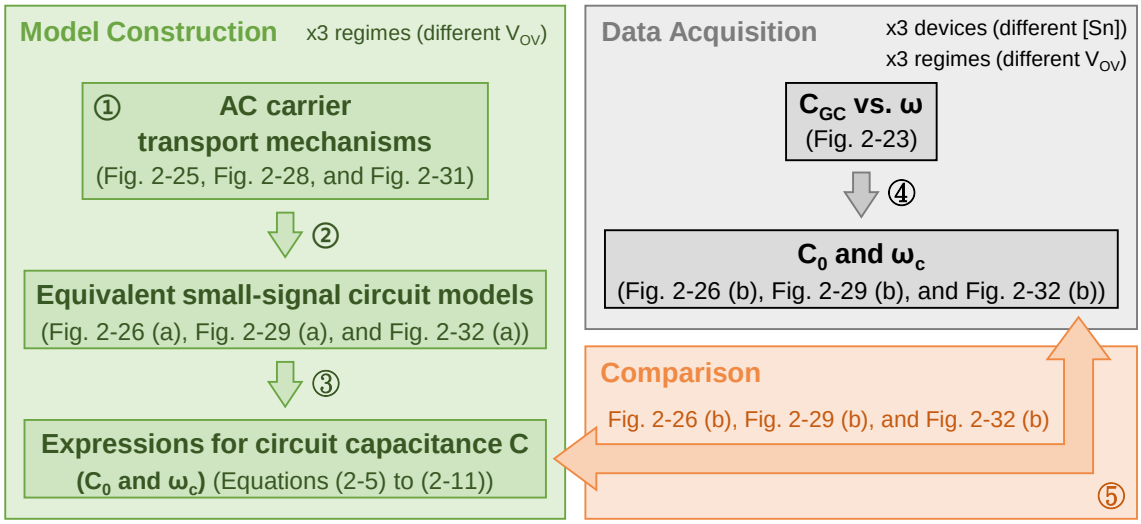

Fig. 2-24 A schematic of the validation process of the split C-V characteristics.

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tracted values are made (⑤), confirming the models' validity and the data interpretation using the models.

Models of the AC carrier transport mechanisms in the Ge(Sn) n-MOSFETs in the split C-V configuration are proposed as follows (Fig. 2-25, Fig. 2-28, and Fig. 2-31). In the accumulation regime, holes are repelled from the surface during the positive half of the AC cycle ($+\Delta V_G$), leading to a decrease in charge ($-\Delta Q$) in the accumulation layer (①) (Fig. 2-25 (a)). The excess holes repelled from the surface can either leave via the p^+ body contact (⑥) or couple to the n^+ source and drain contacts via the junctions (② and ③) and the gate-to-source and gate-to-drain overlaps (④ and ⑤). The former current path (⑥) results from a hole concentration gradient established by the excess holes in the substrate [58], while the remaining current paths are discussed as follows.

On one hand, the excess holes build up its concentration near the p-sides of the junctions. This breaks the equilibrium between the drift and diffusive components of hole current across the junctions, thereby resulting in net hole diffusion from the p-sides to the

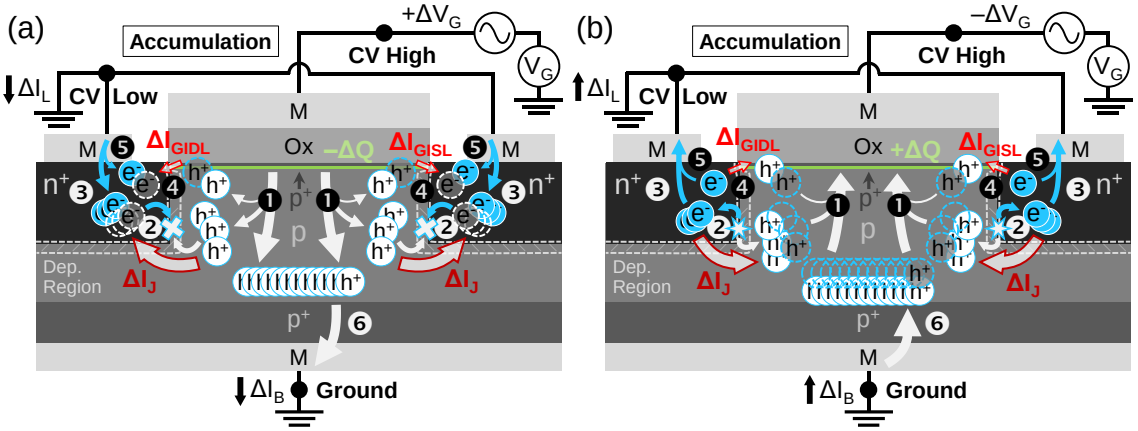

Fig. 2-25 Schematics of the AC carrier transport mechanisms in the Ge(Sn) n-MOSFETs during the (a) positive and (b) negative half of an AC cycle of the split C-V measurements in the accumulation regime. Differential (AC) excess/deficient carriers are represented by the solid/hollow circles, while differential (AC) electron/hole/total currents are represented by blue/white/red arrows.

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n^+-sides [66]. Because diffusion current in a Ge(Sn) p-n junction is dominated by GR current due to a high defect density [61, 65], holes tend to recombine with electrons within the depletion regions before reaching the n^+-sides [66]. The recombination processes result in a decrease in electron concentration within the depletion regions, which breaks the equilibrium between the drift and diffusive components of electron current across the junctions, thereby resulting in net electron diffusion from the n^+-sides to the depletion regions [66]. A differential current ΔI_J is therefore established (②). These current paths are completed by replenishing the electron deficiency through the n^+ source and drain contacts (③).

On the other hand, the positive gate voltage swing ($+\Delta V_G$) reduces the electric fields at the gate-to-source and gate-to-drain overlaps. This leads to a decrease in the number of electrons tunneled from the p-sides to the n^+-sides, or equivalently, a deficiency of electrons and holes on the n^+-sides and p-sides, respectively. As a result, differential currents ΔI_{GIDL} and ΔI_{GISL} are established (④). The current paths are then completed by replenishing the hole and electron deficiency through ① and the inflow of electrons via the n^+ source and drain contacts (⑤), respectively. Because the AC carrier transport mechanisms in the negative half of the AC cycle ($-\Delta V_G$) (Fig. 2-25 (b)) is exactly the reverse of those in the positive half of the AC cycle, detailed descriptions are omitted for brevity as they can be inferred by symmetry.

By extending a concept from [72], a physically based equivalent small-signal circuit model of the Ge(Sn) n-MOSFETs during spilt C-V measurements is constructed (Fig. 2-26 (a)) to explain the anomalous split C-V behaviors. Based on Fig. 2-25, the carrier storage properties at the surface are modeled by oxide capacitance C_{ox} and accumulation capacitance C_A [25], while the dissipative carrier transports corresponding to ②, ④, and ⑥ are modeled by differential junction conductance G_j, differential GIDL conductance

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G_{GIDL}, and differential bulk conductance G_B, respectively. To facilitate analysis, other transport processes are omitted (e.g. oxide leakage) since their effects are negligible (Appendix A.1). In the accumulation regime, the circuit capacitance C of the small-signal model (Fig. 2-26 (a)) is derived from the imaginary part of the ratio i_x/v_x [69] as

$$C = \frac{1}{\omega}\mathrm{Im}\left(\frac{i_x}{v_x}\right) = C_0 \cdot \frac{1}{1+(\omega/\omega_c)^2} + 2C_{ov}\,, \tag{2-5}$$

where

$$C_0 = \frac{C_{ox} \parallel C_A}{1 + \dfrac{G_B}{2G_j + 2G_{GIDL}}} \tag{2-6}$$

and

$$\omega_c = \frac{G_B + 2G_j + 2G_{GIDL}}{C_{ox} \parallel C_A}\,. \tag{2-7}$$

The assumptions and derivations are stated and justified in Appendix A.1.

On one hand, the low-pass form in Equation (2-5) predicts that once the angular frequency ω exceeds the cut-off angular frequency ω_c, the circuit capacitance C will decrease from its constant value C_0 by two orders of magnitude for every decade increment in ω [69], before approaching the lower limit of $2C_{ov}$ (overlap capacitance). This is because the gate stack (C_{ox} || C_A) is in series with the substrates and junctions (G_B and $2G_j$

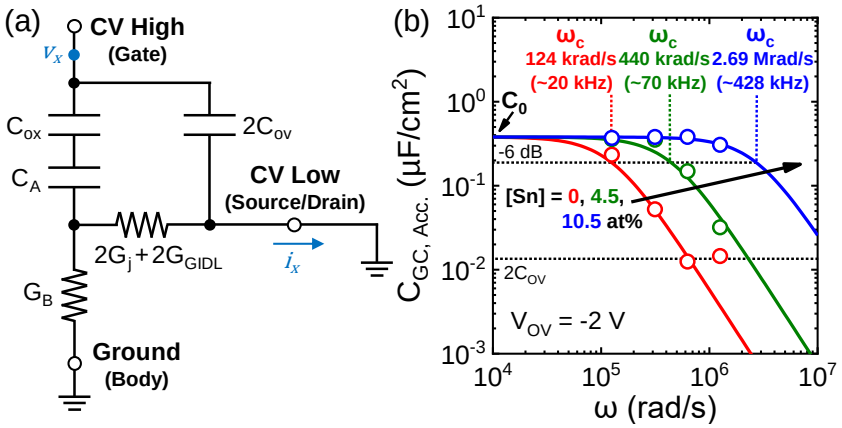

Fig. 2-26 (a) An equivalent small-signal circuit model of the Ge(Sn) n-MOSFETs biased in the accumulation regime. (b) C_{GC} vs. angular frequency ω (replotted from Fig. 2-23 (a)) and the fitted curves.

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+ $2G_{GIDL}$) (Fig. 2-26 (a)). When ω increases above ω_c, the reactance of $C_{ox} \parallel C_A$ drops below the reciprocal of $G_B + 2G_j + 2G_{GIDL}$ (Equations (2-5) and (2-7)). This results in a smaller voltage drop across $C_{ox} \parallel C_A$, and consequently, less energy stored in $C_{ox} \parallel C_A$ than the energy dissipated through $G_B + 2G_j + 2G_{GIDL}$ [69]. This significantly attenuates the reactive behavior of the circuit, leading to a sharp decrease in circuit capacitance C (Equations (2-5)). In the log-log plot of C_{GC} vs. ω (replotted from Fig. 2-23 (a)), the curves fitted by Equation (2-5) using a least-square method closely match the experimental data (Fig. 2-26 (b)). This implies that the frequency response of C_{GC} is satisfactorily captured by the small-signal model (Equation (2-5)).

On the other hand, the ratio $G_B/(2G_j + 2G_{GIDL})$ in the denominator of Equation (2-6) implies a competition between the bulk and the junctions. When most of the carriers are supplied from the bulk ($G_B \gg 2G_j + 2G_{GIDL}$), C_0 is expected to be vanishingly small because the C-V meter detects negligible current across the junctions. This corresponds to the conventional C_{GC}-V_{OV} curve (Fig. 2-10 (a)). However, when most of the carriers are supplied from the junctions ($2G_j + 2G_{GIDL} \gg G_B$), as is the case for the Ge(Sn) n-MOSFETs due to their leaky junctions (Fig. 2-17 (a)), C_0 is expected to be independent of $2G_j + 2G_{GIDL}$ and to reach its maximum value of $C_{ox} \parallel C_A$, because the C-V meter detects significant current across the junctions. A similar competition is also predicted by Equation (2-7), where either the bulk conductance (G_B) or junction conductance ($2G_j + 2G_{GIDL}$) determines the cut-off frequency (ω_c). For leaky junctions ($2G_j + 2G_{GIDL} \gg G_B$), as is the case for the Ge(Sn) n-MOSFETs, ω_c is expected to be proportional to $2G_j + 2G_{GIDL}$. This is because the frequency response of C, which is governed by ω_c (Equation (2-5)), primarily results from the fact that the frequency-dependent element $C_{ox} \parallel C_A$ is in series with $2G_j + 2G_{GIDL}$ (Fig. 2-26 (a)).

The fitting parameters (used in Fig. 2-26 (b)) and $2I_{OFF*}$ (excerpted from Fig. 2-17

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(a)) are shown in Fig. 2-27 (a). By using the Sn fraction as an intermediate parameter, C_0 and ω_c are found to be independent of and proportional to $2I_{OFF*}$, respectively (Fig. 2-27 (b)). Since I_{OFF*} comprises both the junction leakage and GIDL (Chapter 2.3.1), i.e., $2I_{OFF*}$ is proportional to $2G_j + 2G_{GIDL}$, it follows that C_0 and ω_c are independent of and proportional to $2G_j + 2G_{GIDL}$, respectively. These findings validate the predictions made by the small-signal model (Equations (2-6) and (2-7)).

The preceding analyses confirm that in the accumulation regime, the AC behaviors of the Ge(Sn) n-MOSFETs are well-characterized by the small-signal model, thereby enabling interpretation of the anomalous split C-V characteristics based on the model. First, the anomalously high C_{GC} (Fig. 2-23 (a)) relative to the standard one [25] is attributed to a large $2G_j + 2G_{GIDL}$, because this implies a large C_0 and ω_c (Equations (2-6) and (2-7)), and consequently, a large C (Equation (2-5)). Physically, this originates from a large supply of majority carriers across the leaky junctions in response to the AC signal (Fig. 2-25), as evidenced by the high I_{OFF*} (Fig. 2-17 (a)). Second, the increase in C_{GC} with increasing Sn fraction (Fig. 2-23 (a)) is attributed to a corresponding increase in $2G_j + 2G_{GIDL}$, because this a implies a larger C_0 and ω_c (Equations (2-6) and (2-7)), and consequently, a larger C (Equation (2-5)). Physically, this originates from an increase in the supply of

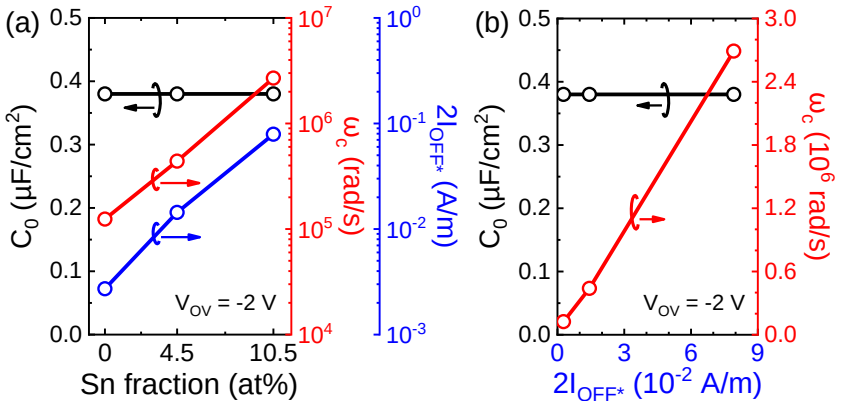

Fig. 2-27 (a) Fitting parameters C_0 and ω_c (used in Fig. 2-26 (b)) as well as $2I_{OFF*}$ (excerpted from Fig. 2-17 (a)) vs. Sn fraction. (b) C_0 and ω_c (from (a)) vs. $2I_{OFF*}$ (from (a)).

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majority carriers across the junctions in response to the AC signal (Fig. 2-25) as the Sn fraction increases, as evidenced by the corresponding increase in I_{OFF*} (Fig. 2-17 (a)). Lastly, the reduction in C_{GC} with increasing frequency (Fig. 2-23 (a)) is attributed to a corresponding decrease in the gate stack reactance ($1/\omega(C_{ox} \parallel C_A)$) relative to $2G_j + 2G_{GIDL}$, because this increases ω/ω_c and reduces the circuit capacitance C (Equations (2-5) and (2-7)), given that the junctions are leaky ($2G_j + 2G_{GIDL} \gg G_B$). From a physical standpoint, this originates from the reduced energy storage in the gate stack relative to that dissipated through carrier transport across the substrate and junctions as the frequency increases (Fig. 2-25) [69].

In the depletion regime, the AC carrier transport mechanisms follow the same models as those in the accumulation regime (Fig. 2-25), except that the charge variation (ΔQ) now occurs at the edge of surface depletion region due to the depleted surface (Fig. 2-28). In addition, any transport process related to GIDL and GISL are absent because the electric field at the gate-to-drain and gate-to-source overlaps are much smaller compared to those in the accumulation regime, respectively. As a result, the physically based equivalent small-signal circuit model is constructed to be identical to that in the accumulation regime, except that C_A is replaced with the depletion capacitance C_D [25] and that $2G_{GIDL}$

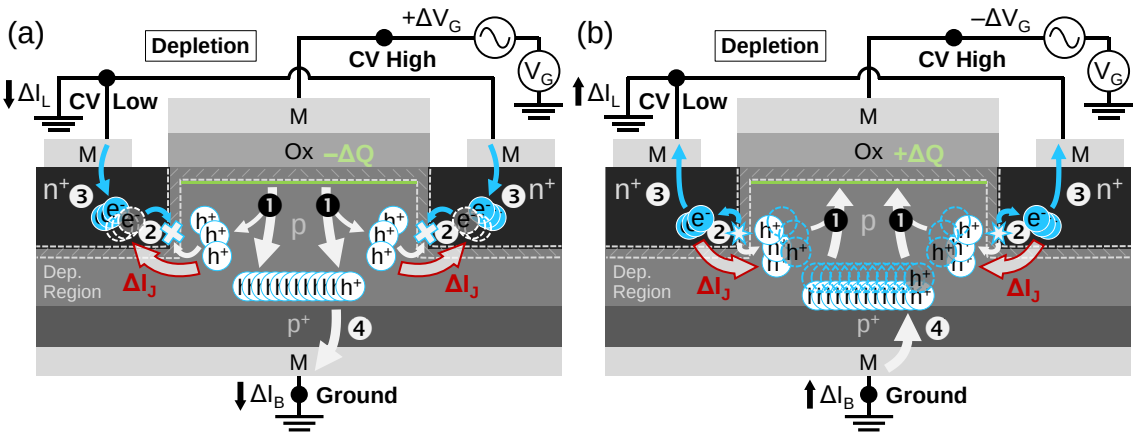

Fig. 2-28 Schematics of the AC carrier transport mechanisms in the Ge(Sn) n-MOSFETs during the (a) positive and (b) negative half of an AC cycle of the split C-V measurements in the depletion regime.

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is set to 0 (Fig. 2-29 (a)). The circuit capacitance C takes on the same form as that in Equation (2-5), except that C_0 and ω_c become

$$C_0 = \frac{C_{ox} \parallel C_D}{1 + \frac{G_B}{2G_j}} \tag{2-8}$$

and

$$\omega_c = \frac{G_B + 2G_j}{C_{ox} \parallel C_D}. \tag{2-9}$$

The assumptions and derivations are stated and justified in Appendix A.2.

The analyses below parallel those in the accumulation regime. First, the fitted curves closely match the experimental data (Fig. 2-29 (b)), implying that the frequency response of C_{GC} is satisfactorily captured by the small-signal model (Equation (2-5)). Moreover, both Equations (2-8) and (2-9) predict a competition between the bulk (G_B) and the junctions ($2G_j$). Given that the junctions of the Ge(Sn) n-MOSFETs are leaky ($2G_j \gg G_B$), i.e., most of the majority carriers are supplied across the junctions rather than from the bulk, C_0 is predicted to be independent of $2G_j$ and to attains its maximum value of $C_{ox} \parallel C_D$ (Equation (2-8)), while ω_c is predicted to be proportional to $2G_j$ (Equation (2-9)). These are validated by the fitting results shown in Fig. 2-30 (b), which is derived from Fig. 2-30

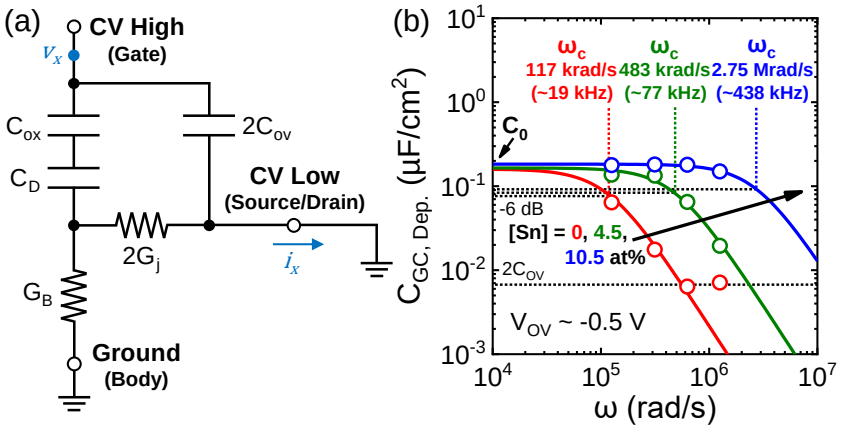

Fig. 2-29 (a) An equivalent small-signal circuit model of the Ge(Sn) n-MOSFETs biased in the depletion regime. (b) C_{GC} vs. angular frequency ω (replotted from Fig. 2-23 (b)) and the fitted curves.

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(a) using the Sn fraction as an intermediate parameter. It's worth noting that due to the leaky nature of the junctions ($2G_j \gg G_B$), C_0 is independent of $2G_j$ (Equation (2-8)). Thus, the slight increase in C_0 with increasing Sn fraction and $2I_{OFF}$ (Fig. 2-30 (a) and (b)) cannot be attributed to the increase in $2G_j$. Instead, it should be attributed to the increase in C_D due to the increase in dielectric constant [30] with increasing Sn fraction [73].

Similar to the case in the accumulation regime, interpretations regarding the anomalous split C-V characteristics in the depletion regime are made based on the small-signal model. First, the anomalously high C_{GC} (Fig. 2-23 (b)) is attributed to a large $2G_j$, because this implies a large C_0 and ω_c (Equations (2-8) and (2-9)), and consequently, a large C (Equation (2-5)). Physically, this originates from a large supply of majority carriers across the leaky junctions in response to the AC signal (Fig. 2-28), as evidenced by the high I_{OFF} (Fig. 2-17 (b)). Second, the increase in C_{GC} with increasing Sn fraction (Fig. 2-23 (b)) is attributed to a corresponding increase in $2G_j$, because this implies an increase in C_0 and ω_c (Equations (2-8) and (2-9)), and consequently, an increase in C (Equation (2-5)). Physically, this originates from an increased supply of majority carriers across the junctions in response to the AC signal (Fig. 2-28) as the Sn fraction increases, as evidenced by the corresponding increase in I_{OFF} (Fig. 2-17 (b)). Lastly, the reduction in C_{GC} with increasing

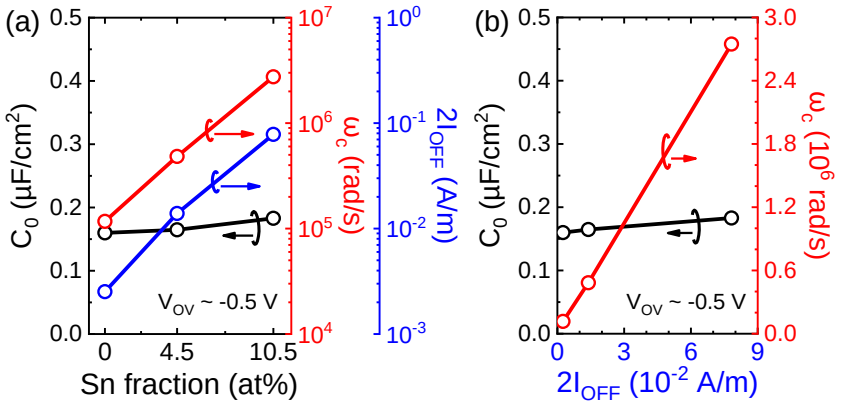

Fig. 2-30 (a) Fitting parameters C_0 and ω_c (used in Fig. 2-29 (b)) as well as $2I_{OFF}$ (excerpted from Fig. 2-17 (b)) vs. Sn fraction. (b) C_0 and ω_c (from (a)) vs. $2I_{OFF}$ (from (a)).

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frequency (Fig. 2-23 (b)) is attributed to a corresponding decrease in the gate stack reactance ($1/\omega(C_{ox} \parallel C_D)$) relative to $2G_j$, because this increases ω/ω_c and reduces the circuit capacitance C (Equations (2-5) and (2-9)), given that the junctions are leaky ($2G_j \gg G_B$). From a physical standpoint, this originates from the reduced energy storage in the gate stack relative to that dissipated through carrier transport across the substrate and junctions as the frequency increases (Fig. 2-28) [69].

In the strong inversion regime, the AC carrier transport mechanisms follow the same models as those in the depletion regime (Fig. 2-28), except that the charge variation (ΔQ) now occurs in the inversion layer due to the heavily inverted surface (Fig. 2-31). Besides, two additional transport mechanisms emerge: surface GR processes (①), due to the presence of surface depletion region, and the drift of electrons along the inversion channel (④ and ⑤). During the positive half of the AC cycle ($+\Delta V_G$), electrons are attracted to the surface, leading to an increase in negative charge ($-\Delta Q$) in the inversion layer (Fig. 2-31 (a)). On one hand, the attracted electrons are supplied from the surface depletion region [71], resulting in electron deficiency, and consequently, generation of electron-hole pairs [58]. These pairs are then separated by the electric field in the surface depletion

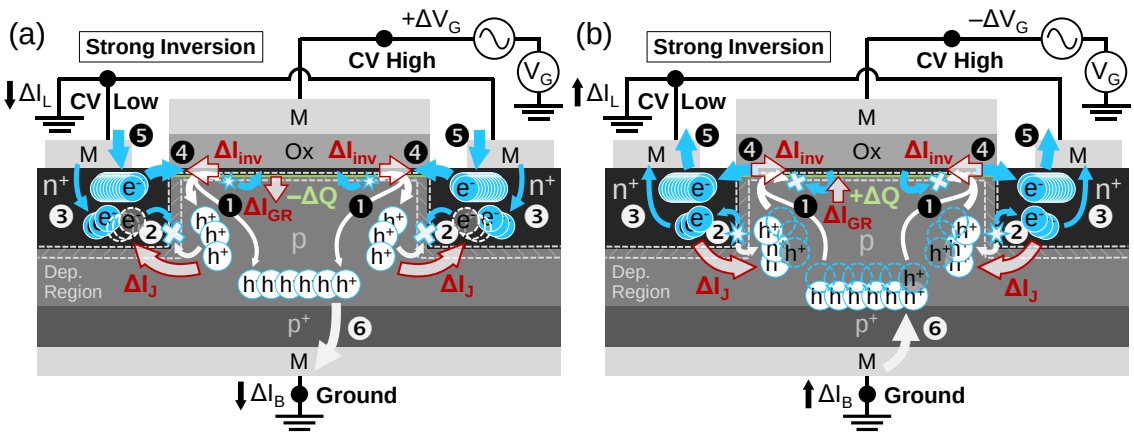

Fig. 2-31 Schematics of the AC carrier transport mechanisms in the Ge(Sn) n-MOSFETs during the (a) positive and (b) negative half of an AC cycle of the split C-V measurements in the strong inversion regime.

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region, where electrons and holes are swept to the inversion layer and the substrate, respectively, establishing a differential current ΔI_{GR} (①). The current paths are then completed through processes (②, ③, and ⑥) identical to those in the depletion regime (Fig. 2-28 (a)). On the other hand, the attracted electrons are supplied directly from the source and drain, establishing differential currents ΔI_{inv} (④). The current paths are then completed by the inflow of electrons from the n^+ source and drain contacts (⑤). Detailed descriptions of the AC carrier transport in the negative half of the AC cycle ($-\Delta V_G$) (Fig. 2-31 (b)) is omitted for brevity because they can be inferred by symmetry.

The physically based equivalent small-signal circuit model is constructed to be identical to that in the depletion regime, except that C_D is replaced with the inversion capacitance C_I [25], and additional differential channel conductance G_{ch} as well as differential surface GR conductance G_{gr} are introduced (Fig. 2-32 (a)). The circuit capacitance C takes on the same form as that in Equation (2-5), expect that C_0 and ω_c become

$$C_0 = \frac{C_{ox} \parallel C_I}{1 + \dfrac{\alpha G_B}{4G_{ch} + 2\alpha G_j}} \tag{2-10}$$

and

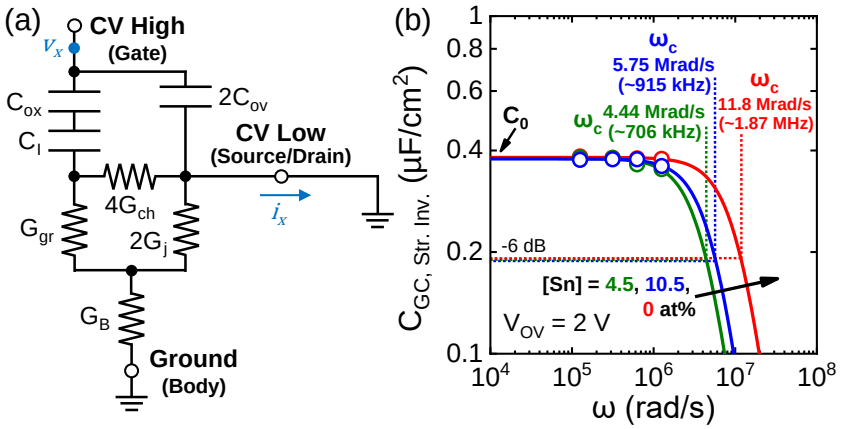

Fig. 2-32 (a) An equivalent small-signal circuit model of the Ge(Sn) n-MOSFETs biased in the strong inversion regime. (b) C_{GC} vs. angular frequency ω (replotted from Fig. 2-23 (c)) and the fitted curves.

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$$\omega_c = \frac{4G_{ch} + \alpha\left(G_B + 2G_j\right)}{C_{ox} \parallel C_I}, \tag{2-11}$$

where

$$\alpha = \left[1 + \left(G_B + 2G_j\right)/G_{gr}\right]^{-1} \tag{2-12}$$

is a dimensionless quantity. The assumptions and derivations are stated and justified in Appendix A.3.

The analyses below parallel those in the depletion regime. First, the fitted curves closely match the experimental data (Fig. 2-32 (b)), implying that the frequency response of C_{GC} is satisfactorily captured by the small-signal model (Equation (2-5)). Because both G_{gr} and G_j account for the same physical process (GR) and the surface area (W x L ~ 200 x 20 μm^2) is much larger than the active junction area (W x junction depth ~ 200 x 0.1 μm^2), a first-order approximation $G_{gr} \gg 2G_j$ can be made. Note that it is the surface area, rather than the volume, of the depletion region that is relevant, because GR processes are primarily contributed by a single cross-sectional surface within the depletion region where the Fermi level aligns with mid-gap [58]. Combining with the fact that the junctions of the Ge(Sn) n-MOSFETs are leaky ($2G_j \gg G_B$), α can be approximated as one. Then, using the fact that the surface is heavily inverted ($4G_{ch} \gg G_B$), Equations (2-10) and (2-11) predict C_0 to be independent of $4G_{ch} + 2G_j$ and ω_c to be linear in $4G_{ch} + 2G_j$, respectively.

The fitting parameters (used in Fig. 2-32 (b)) and $4I_{ON} + 2I_{OFF}$ (excerpted from Fig. 2-17 (b) and (c)) are shown in Fig. 2-33 (a). By using the Sn fraction as an intermediate parameter, C_0 and ω_c are found to be independent of and linear in $4I_{ON} + 2I_{OFF}$, respectively (Fig. 2-33 (b)). Since I_{ON} and I_{OFF} comprises the inversion current and junction leakage, respectively (Chapter 2.3.1), i.e., $4I_{ON} + 2I_{OFF}$ is proportional to $4G_{ch} + 2G_j$, it follows that C_0 and ω_c are independent of and linear in $4G_{ch} + 2G_j$, respectively. These

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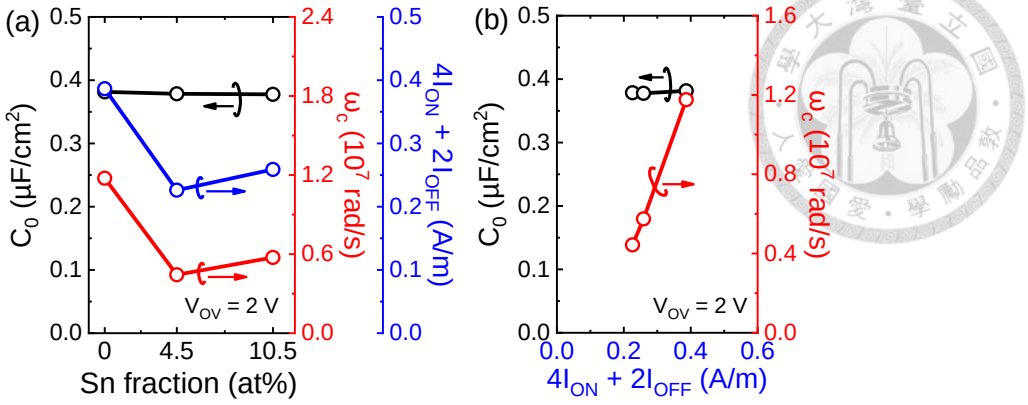

Fig. 2-33 (a) Fitting parameters C_0 and ω_c (used in Fig. 2-32 (b)) as well as $4I_{ON} + 2I_{OFF}$ (excerpted from Fig. 2-17 (b) and (c)) vs. Sn fraction. (b) C_0 and ω_c (from (a)) vs. $4I_{ON} + 2I_{OFF}$ (from (a)).

findings validate the predictions made by the small signal model (Equations (2-10) and (2-11)).

The preceding analyses confirm that in the strong inversion regime, the AC behaviors of the Ge(Sn) n-MOSFETs are well-characterized by the small-signal model, thereby enabling interpretation of the split C-V characteristics based on the model. On one hand, the Sn-fraction dependence of C_{GC} (Fig. 2-23 (c)) is attributed to a variation in $4G_{ch} + 2G_j$. This is because the circuit capacitance C depends on both C_0 and ω_c (Equation (2-5)), and by using the Sn fraction as an intermediate parameter, both C_0 and ω_c (Fig. 2-33 (a)) are linked to a dependence on $4I_{ON} + 2I_{OFF}$ (Fig. 2-33 (b)), and consequently to $4G_{ch} + 2G_j$, through Equations (2-10) and (2-11). Physically, this originates from the Sn-fraction dependent supply of minority carriers by the channel and the junctions in response to the AC signal (Fig. 2-31). On the other hand, the frequency dispersion in C_{GC} (Fig. 2-23 (c)) is attributed to the frequency dependence of the gate stack reactance ($1/\omega(C_{ox} \parallel C_I)$) relative to $4G_{ch} + 2G_j$. This is because ω/ω_c, which governs the frequency response of C (Equation (2-5)), primarily comprises $1/\omega(C_{ox} \parallel C_I)$ and $4G_{ch} + 2G_j$ (Equation (2-11)), given that the junctions are leaky ($2G_j \gg G_B$), the surface is heavily inverted ($4G_{ch} \gg G_B$), and the surface area is large ($G_{gr} \gg 2G_j$). From a physical standpoint, this originates from

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the frequency-dependent energy storage in gate stack relative to that dissipated through carrier transport across the channel and junctions (Fig. 2-31) [69].

To sum up, in both the accumulation and depletion regimes, the abnormally high C_{GC} (Fig. 2-23 (a) and (b)) is attributed to a large supply of majority carriers through the leaky junctions in response to the AC signal (Fig. 2-25 and Fig. 2-28). In addition, the increase in C_{GC} with increasing Sn fraction (Fig. 2-23 (a) and (b)) is attributed to a corresponding increase in the supply of majority carriers through the junctions in response to the AC signal (Fig. 2-25 and Fig. 2-28). Moreover, the reduction in C_{GC} at a higher frequency (Fig. 2-23 (a) and (b)) is attributed to the corresponding reduction in energy stored in the gate stack relative to that dissipated through carrier transport across the substrate and junctions (Fig. 2-25 and Fig. 2-28) [69]. In the strong inversion regime, the Sn-fraction dependence of C_{GC} (Fig. 2-23 (c)) is attributed to the Sn-fraction dependent supply of minority carriers by the channel and the junctions in response to the AC signal (Fig. 2-31). The frequency dispersion in C_{GC} (Fig. 2-23 (c)), however, is attributed to the frequency-dependent energy storage in gate stack relative to that dissipated through carrier transport across the channel and junctions (Fig. 2-31) [69].

2.3.3 Split G-V Characteristics

The normalized gate-to-source-drain conductance (G_{gsd}) of the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs is shown as a function of V_{OV} (Fig. 2-34). In the strong inversion regime (V_{OV} = 2 V), all G_{gsd}-V_{OV} curves level-off since the channel conductance exhibits minimal further increase (Fig. 2-15). As V_{OV} decreases, G_{gsd} is expected to decrease and eventually vanish in the depletion (V_{OV} = –0.5 V) and accumulation regimes (V_{OV} = –2 V) due to the reduction in channel conductance and the rectifying characteristics of the drain-to-substrate and source-to-substrate n^+/p junctions. However, an anoma-

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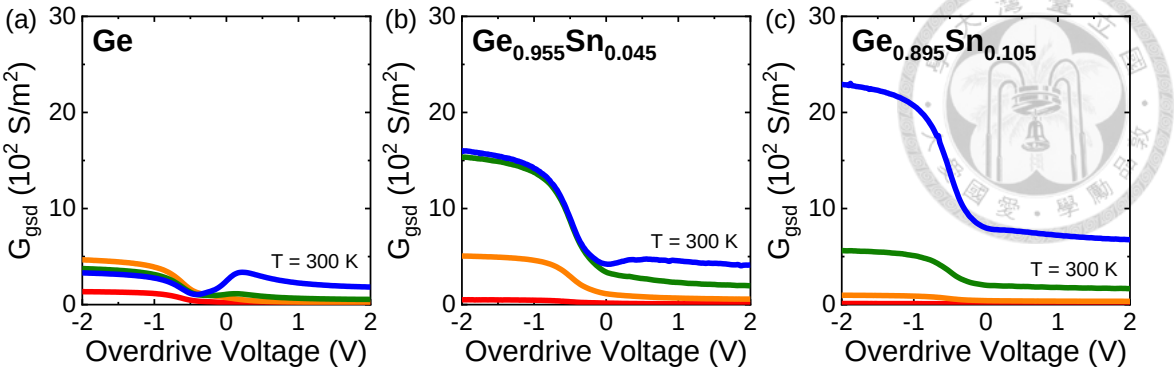

Fig. 2-34 Normalized gate-to-source-drain conductance (G_{gsd}) of the (a) Ge, (b) $Ge_{0.955}Sn_{0.045}$, and (c) $Ge_{0.895}Sn_{0.105}$ n-MOSFETs vs. V_{OV} measured with frequencies of 20, 50, 100, and 200 kHz at 300 K.

lous increase in G_{gsd} is observed across all devices. This could be a result of high off-state leakage (high junction/GIDL conductance), which establishes a signal path between the source/drain and the surface during transistor off-state.

The G_{gsd} measured in the accumulation, depletion, and strong inversion regimes are extracted from Fig. 2-34 and plotted against the Sn fraction (Fig. 2-35). For all devices, G_{gsd} increases with increasing frequency, which is opposite to the trend of C_{GC} vs. frequency (Fig. 2-23). This could be understood as follows. The measured conductance (G_{gsd}) is determined by both the gate stack reactance ($X = 1/\omega C$) and the series resistance R (junction, GIDL, or channel resistance, depending on V_{OV}). An increase in frequency lead to a decrease in X relative to the resistance, thereby increasing both the voltage drop V

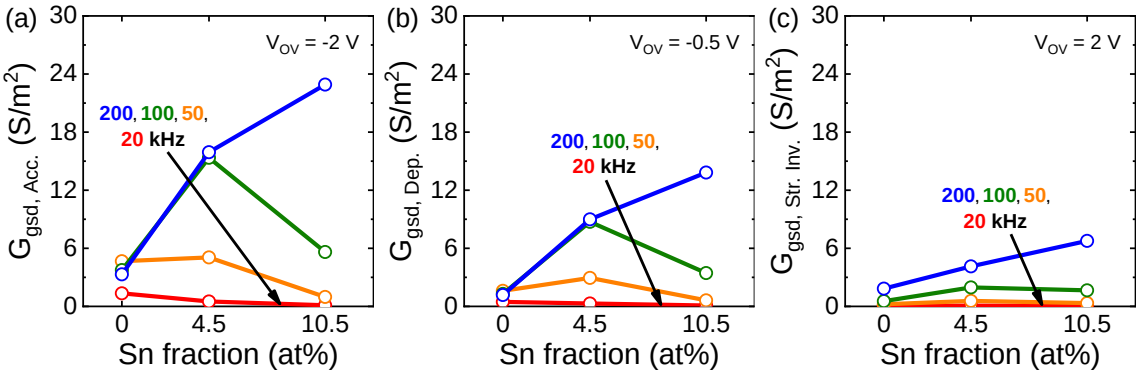

Fig. 2-35 G_{gsd} vs. Sn fraction in the (a) accumulation, (b) depletion, and (c) strong inversion regimes of the Ge(Sn) n-MOSFETs measured with frequencies of 20, 50, 100, and 200 kHz at 300 K.

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Table 2-1 G_0 and ω_c of Equation (2-13). α is defined as $[1 + (G_B + 2G_j)/G_{gr}]^{-1}$.

Biasing Regime	V_{OV}	G_0	ω_c
Accumulation	–2 V	$2G_j + 2G_{GIDL}$	$\frac{G_B + 2G_j + 2G_{GIDL}}{C_{ox} \parallel C_A}$
Depletion	–0.5 V	$2G_j$	$\frac{G_B + 2G_j}{C_{ox} \parallel C_D}$
Strong inversion	2 V	$4G_{ch} + 2\alpha G_j$	$\frac{4G_{ch} + \alpha(G_B + 2G_j)}{C_{ox} \parallel C_I}$

across the resistance and the energy E dissipated in it ($E = V^2/R$) [69]. This enhances the resistive (conductive) behavior of the device, which may contribute to the increase in G_{gsd} with increasing frequency. Besides, in both the accumulation and depletion regimes (Fig. 2-35 (a) and (b)), the high-frequency limit of G_{gsd} increases with Sn fraction, which could be attributed to an enhanced transistor off-state leakage. The validating process is identical to Fig. 2-24, except that C_{GC} and C_0 are replaced with G_{gsd} and G_0.

To elucidate the anomalous split G-V characteristics, models of the AC carrier transport mechanisms in the Ge(Sn) n-MOSFETs in the split C-V configuration are proposed as before (Fig. 2-25, Fig. 2-28, and Fig. 2-31). By extending a concept from [72], physically based small-signal circuit models are also constructed as before (Fig. 2-26 (a), Fig. 2-29 (a), and Fig. 2-32 (a)). The circuit conductance G of the small-signal model is derived from the real part of the ratio i_x/v_x [69] as

$$G = \mathrm{Re}\left(\frac{i_x}{v_x}\right) = G_0 \cdot \frac{1}{1 + (\omega_c/\omega)^2}, \tag{2-13}$$

where G_0 and ω_c are listed in Table 2-1. The assumptions and derivations are detailed in Appendix A.

On one hand, the high-pass form in Equation (2-13) predicts that once the angular frequency ω drops below the cut-off frequency ω_c, the circuit conductance G will decrease from its constant value G_0 by two orders of magnitude for every decade decrease in ω [69]. Note that this is complementary to the low-pass form of the circuit capacitance C

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(Equation (2-5)). In the log-log plot of G_{gsd} vs. ω (replotted from Fig. 2-35), the curves fitted by Equation (2-13) using a least-square method closely match the experimental data (Fig. 2-36), implying that the frequency response of G_{gsd} is successfully captured by the small-signal models (Equation (2-13)).

On the other hand, G_0 is expected to be proportional to $2G_j + 2G_{GIDL}$, $2G_j$, and $4G_{ch} + 2\alpha G_j$ in the accumulation, depletion, and strong inversion regimes, respectively (Table 2-1). This is because in the accumulation and depletion regimes, the signal paths between the source/drain and the surface are connected through the junctions (Fig. 2-25 and Fig. 2-28), whereas in the strong inversion regime, the signal paths are connected through the channel, junction, and surface GR processes (Fig. 2-31). Given that the junctions of the Ge(Sn) n-MOSFETs are leaky ($2G_j + 2G_{GIDL} \gg G_B$ and $2G_j \gg G_B$), ω_c is also expected to be proportional to $2G_j + 2G_{GIDL}$, $2G_j$, and $4G_{ch} + 2\alpha G_j$ in the accumulation, depletion, and strong inversion regimes, respectively (Table 2-1). Note that using the first-order approximation $G_{gr} \gg 2G_j$ (Chapter 2.3.2), α can be approximated as one.

The fitting parameters (used in Fig. 2-36 (a) and (b)) and the off-state current ($2I_{OFF*}$ and $2I_{OFF}$, excerpted respectively from Fig. 2-17 (a) and (b)) are plotted against the Sn fraction (Fig. 2-37). By using the Sn fraction as an intermediate parameter, both G_0 and

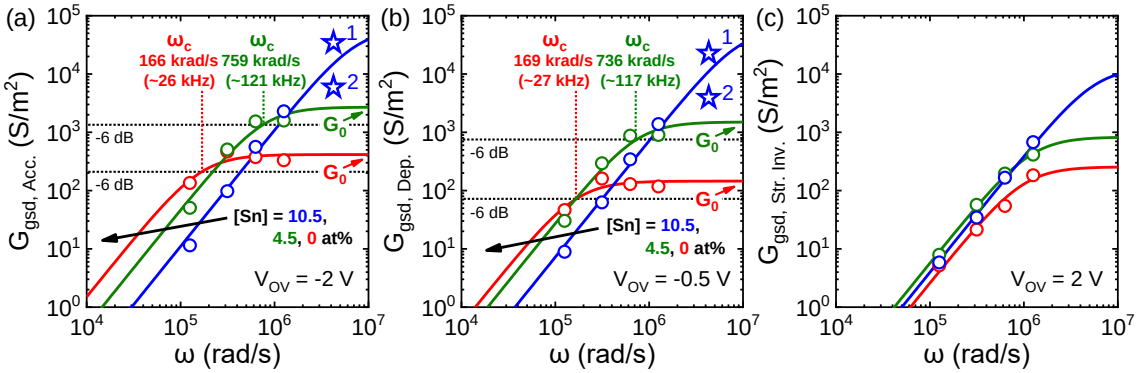

Fig. 2-36 G_{gsd} vs. angular frequency ω in the (a) accumulation (replotted from Fig. 2-35 (a)), (b) depletion (replotted from Fig. 2-35 (b)), and (c) strong inversion regimes (replotted from Fig. 2-35 (c)) along with the fitted curves. The blue stars represent the next possible high-frequency data.

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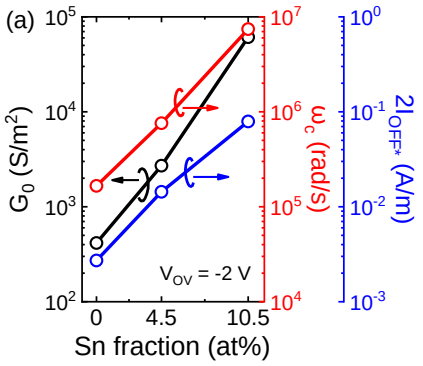

Fig. 2-37 (a) Fitting parameters G_0 and ω_c (used in Fig. 2-36 (a)) as well as $2I_{OFF*}$ (excerpted from Fig. 2-17 (a)) vs. Sn fraction in the accumulation regime. (b) Fitting parameters G_0 and ω_c (used in Fig. 2-36 (b)) as well as $2I_{OFF}$ (excerpted from Fig. 2-17 (b)) vs. Sn fraction in the depletion regime.

ω_c are found to increase with but not proportional to $2I_{OFF*}$ and $2I_{OFF}$ (Fig. 2-38), and consequently, $2G_j + 2G_{GIDL}$ and $2G_j$. These findings are slightly off compared to the predictions made by the small-signal models (Table 2-1), possibly due to the inaccurate extraction of G_0 and ω_c of the $Ge_{0.895}Sn_{0.105}$ n-MOSFET resulted from a lack of data at frequencies higher than 200 kHz. To be specific, the next high-frequency data (blue star 1 or blue star 2) could severely alter the plateau (G_0) and the 6-dB drop point (ω_c) of the fitting curves (Fig. 2-36 (a) and (b)). The lack of high-frequency data also invalidates the extraction process of G_0 and ω_c for all devices in the strong inversion regime (Fig. 2-36 (c)). Therefore, discussions related to G_0 and ω_c in the strong inversion regime are omitted.

Nevertheless, if G_{gsd} can be properly fitted using the model (Equation (2-13) and

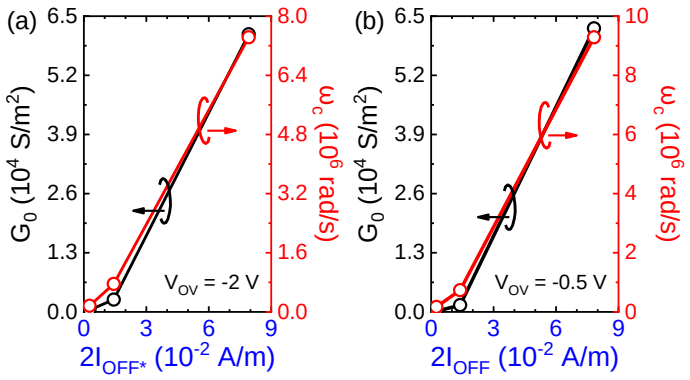

Fig. 2-38 (a) G_0 and ω_c vs. $2I_{OFF*}$ in the accumulation regime. (b) G_0 and ω_c vs. $2I_{OFF}$ in the depletion regime.

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Table 2-1), the effect of high off-state leakage on C_{GC} can be calibrated as follows. First, obtain C_{GC} and G_{gsd} under a wide range of test frequencies (say, from 1 kHz to 1 MHz) using the split C-V and split G-V measurement. Then, extract C_0, G_0, and ω_c of the small-signal models using the fitting procedures (Fig. 2-26 (b), Fig. 2-29 (b), Fig. 2-32 (b), and Fig. 2-36). In the accumulation and depletion regimes, obtain the two pairs of unknown ($C_{ox} \parallel C_A$, G_B) and ($C_{ox} \parallel C_D$, G_B) by solving the coupled equations

$$\begin{cases} C_0 = \dfrac{C_{ox} \parallel C_A}{1 + \dfrac{G_B}{2G_j + 2G_{GIDL}}} \\ \omega_c = \dfrac{G_B + 2G_j + 2G_{GIDL}}{C_{ox} \parallel C_A} \end{cases} \tag{2-14}$$

and

$$\begin{cases} C_0 = \dfrac{C_{ox} \parallel C_A}{1 + \dfrac{G_B}{2G_j}} \\ \omega_c = \dfrac{G_B + 2G_j}{C_{ox} \parallel C_A} \end{cases}, \tag{2-15}$$

respectively, where $2G_j + 2G_{GIDL}$ and $2G_j$ are known as the extracted G_0 (Table 2-1). Finally, recalculate new sets of C_0 and ω_c using the parameters ($C_{ox} \parallel C_A$, G_B) and ($C_{ox} \parallel C_D$, G_B) with $2G_j + 2G_{GIDL}$ and $2G_j$ set to zero (no junction leakage). The calibrated C_{GC} can be reconstructed using Equation (2-5). As for the strong inversion regime, obtain the pair of unknown ($C_{ox} \parallel C_I$, αG_B) by solving the coupled equation

$$\begin{cases} C_0 = \dfrac{C_{ox} \parallel C_I}{1 + \dfrac{\alpha G_B}{4G_{ch} + 2\alpha G_j}} \\ \omega_c = \dfrac{4G_{ch} + \alpha\left(G_B + 2G_j\right)}{C_{ox} \parallel C_I} \end{cases}, \tag{2-16}$$

where $4G_{ch} + 2\alpha G_j$ is known as the extracted G_0 (Table 2-1). Then, recalculate a new set of C_0 and ω_c using the parameters ($C_{ox} \parallel C_I$, αG_B) with $2\alpha G_j$ set to zero (no junction leakage). This can be done by deducting $2\alpha G_j$ from $4G_{ch} + 2\alpha G_j$, where $2G_j$ is the one found in the depletion regime, and α is found by comparing αG_B and the previously ob-

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tained G_B. Finally, the calibrated C_{GC} can be reconstructed using Equation (2-5). This method eliminates the influence of high off-state leakage on C_{GC}, and consequently, on the mobility extraction, which can be applied to small-bandgap, high-mobility transistors such as GeSn, InAs, and InSb n-MOSFETs [1, 6].

2.3.4 μ_{eff}-N_{inv} Characteristics

The effective mobility (μ_{eff}) extracted from I_D or I_S and C_{GC} measured at different frequencies is plotted against inversion carrier density (N_{inv}) for the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs (Fig. 2-39). Only data above the threshold voltage (V_{OV} > 0 V) are displayed, because this is a prerequisite for the split C-V method (Chapter 2.2.3). For all devices, the μ_{eff} extracted from I_D is consistently higher than that extracted from I_S, regardless of N_{inv}. This is attributed to the much larger I_{OFF} on the drain side compared to the source side (Fig. 2-17 (b)). In addition, as the N_{inv} decreases, the discrepancy between the μ_{eff} extracted from I_D and I_S becomes more pronounced. This is attributed to the increased channel resistance, causing both I_D and I_S to become increasingly dominated by their respective I_{OFF}, which is orders of magnitude higher on the drain side than on the source side (Fig. 2-17 (b)). Lastly, as the Sn fraction increases, the discrepancy between

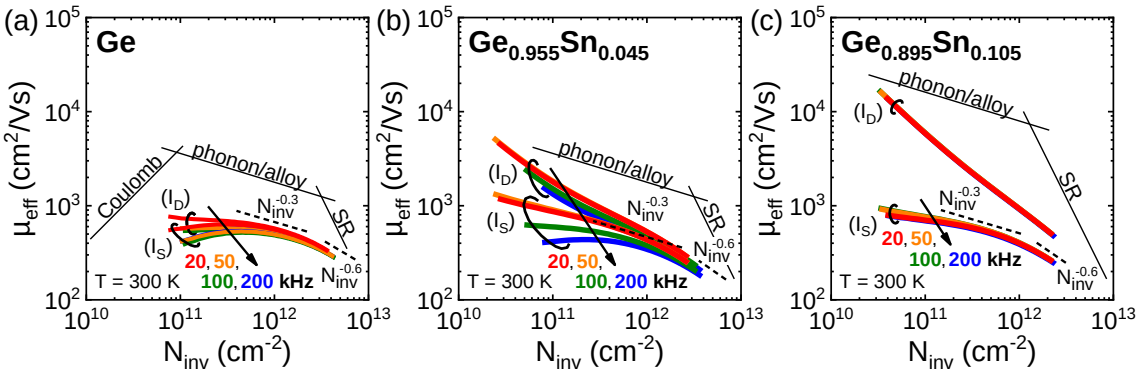

Fig. 2-39 Effective mobility (μ_{eff}) vs. inversion carrier density (N_{inv}) of the (a) Ge, (b) $Ge_{0.955}Sn_{0.045}$, and (c) $Ge_{0.895}Sn_{0.105}$ n-MOSFETs measured at frequencies of 20, 50, 100, and 200 kHz at 300 K.

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the μ_{eff} extracted from I_D and I_S also becomes more pronounced. This is attributed to the increase in I_{OFF} on the drain side relative to the source side with increasing Sn fraction (Fig. 2-17 (b)). As a result, at room temperature, the μ_{eff} extracted from I_S better reflects the "true" mobility, because it is less influenced by I_{OFF}.

The dominant electron scattering mechanisms are inferred from the density dependence of μ_{eff} extracted by I_S (Fig. 2-39). In the intermediate-density regime (N_{inv} = 1 x 10^{12} cm^{-2}), characteristic plateaus with density dependence of $N_{inv}^{-0.3}$ are observed across all devices, which is attributed to either phonon scattering [74, 75] or alloy scattering [76]. In the high-density regime (N_{inv} = 5 x 10^{12} cm^{-2}), the density dependence increases up to $N_{inv}^{-0.6}$ across all devices, which is attributed to the increased influence of surface roughness scattering (SR) [74, 75]. However, in the low-density regime (N_{inv} = 5 x 10^{11} cm^{-2}), positive density dependence, which is attributed to Coulomb scattering [74, 75], are only observed in the Ge device (Fig. 2-39 (a)). The absence of positive density dependencies in the other two devices, except for the $Ge_{0.955}Sn_{0.045}$ n-MOSFET at 200 kHz (Fig. 2-39 (b) and (c)), is attributed to the anomalous split C-V characteristics. In particular, the abnormally high C_{GC} in the depletion regime (Fig. 2-23 (b)) leads to an elevated $2C_{ov}$, and consequently, an abnormally low N_{inv} (Fig. 2-10 (a)), which eventually leads to an excessively high μ_{eff} (Equation (2-4)), thereby obscuring the positive density dependence of μ_{eff}. This is supported by the recovery of a positive density dependence of μ_{eff} in the $Ge_{0.955}Sn_{0.045}$ n-MOSFET as the frequency increases to 200 kHz (Fig. 2-39 (b)), because the abnormally high C_{GC} in the depletion regime is suppressed at high frequencies (Fig. 2-23 (b)). As a result, the μ_{eff} extracted at higher frequencies is less influenced by the anomalous split C-V characteristics (Chapter 2.3.2).

Other two factors determining the optimal frequency for the extraction of μ_{eff} are interface trap response and channel resistance. On one hand, interface trap capacitance

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decreases monotonically with frequency, and thus μ_{eff} should be extracted with the highest possible frequency to minimize its influence [25, 32]. On the other hand, the presence of channel resistance in series with the gate stack results in a reduction in C_{GC} at high frequencies [72, 77]. This occurs because as the frequency increases, the reactance ($X = 1/\omega C$) of the gate stack decreases relative to the channel resistance, thereby reducing both the voltage drop (V) across and the energy ($E = CV^2/2$) stored in the gate stack [69]. Consequently, the overall capacitive behavior of the device is suppressed, leading to a reduction in C_{GC}. If μ_{eff} is extracted with an excessively high frequency, it would be overestimated due to the excessively low C_{GC} [32]. Therefore, according to the split C-V results, the optimal frequency is 50 kHz, because it is the highest frequency before the C_{GC} of any device begins to drop off in the strong inversion regime (Fig. 2-23 (c)).

The μ_{eff} extracted from I_S and C_{GC} at 50 kHz of the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs are extracted from Fig. 2-39 and plotted against Sn fraction (Fig. 2-40). The N_{inv} is fixed at a value of 1 x 10^{12} cm^{-2} to mitigate the overestimation of μ_{eff} at lower densities (Fig. 2-39). Because μ_{eff} is extracted in the intermediate-density regime, the monotonic decrease in μ_{eff} with increasing Sn fraction could be attributed to an enhanced Coulomb scattering due to an increased D_{it} at the oxide/Ge(Sn) interface [21, 55] and an enhanced alloy scattering due an increased Sn fraction [21, 76, 78].

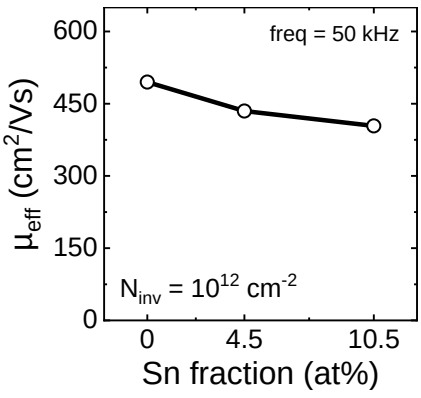

Fig. 2-40 μ_{eff} (extracted from I_S and C_{GC} at 50 kHz) vs. Sn fraction at a fixed N_{inv} of 10^{12} cm^{-2} at 300 K.

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2.4 Summary

In summary, strain-relaxed Ge(Sn) epitaxial structures with Sn fractions up to 10.5 at% were grown using RPCVD, with Sn fractions and strains characterized by HRRSM and high film quality confirmed by HRTEM, EDXS, and AFM. Planar Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs were fabricated using a gate-first process. To ensure the accuracy of the extracted effective mobility (μ_{eff}), a customized MATLAB® program was implemented for measurement. In transfer I-V characteristics, an increase in I_{OFF} and a decrease in I_{ON} with Sn fraction were observed, with the former attributed to an increased junction leakage and the latter to an enhanced alloy scattering. In split C-V characteristics, abnormally high C_{GC} and an increase in C_{GC} with Sn fraction were observed in both the accumulation and depletion regimes. The former is attributed to a large supply of majority carrier through the junctions in response to the AC signal, while the latter is due to an enhanced supply of majority carriers with increasing Sn fraction. In the strong inversion regime, a slight Sn fraction dependence of C_{GC} was observed, which is attributed to the Sn-fraction dependent supply of minority carriers by both the channel and junctions in response to the AC signal. A method is proposed to eliminate the off-state leakage effect on C_{GC}, and consequently, mobility extraction, which can be applied to small-bandgap, high-mobility transistors such as GeSn, InAs, and InSb n-MOSFETs. Among all regimes, frequency dispersion in C_{GC} was observed, which is attributed to the frequency-dependent energy storage in the gate stacks. Lastly, the μ_{eff}-N_{inv} characteristics are less distorted for devices with a lower I_{OFF} and measured at a higher frequency. In the intermediate-density regime, μ_{eff} decreases monotonically with Sn fraction, which is attributed to an enhanced Coulomb scattering and alloy scattering.

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Chapter 3 Electron Transport Properties in Ge(Sn) n-MOSFETs

3.1 Introduction

The electron transport in CVD-grown GeSn epitaxial films has been reported [9]. Hall measurements were performed on GeSn films under different strain conditions and Sn fractions from 300 K to 4 K to characterize the electron transport properties (Fig. 3-1 (a)). Significant mobility enhancement was observed in GeSn films by applying tensile strain (Fig. 3-1 (b)) and increasing Sn fraction (Fig. 3-1 (c)). This is because the energy difference between the indirect and direct valleys in GeSn films is smaller (i.e. more like a direct-bandgap material) under a large tensile strain or with a high Sn fraction [18, 19, 35], leading to an increase in the electron population in the Γ-valley, where the effective mass is very small [9].

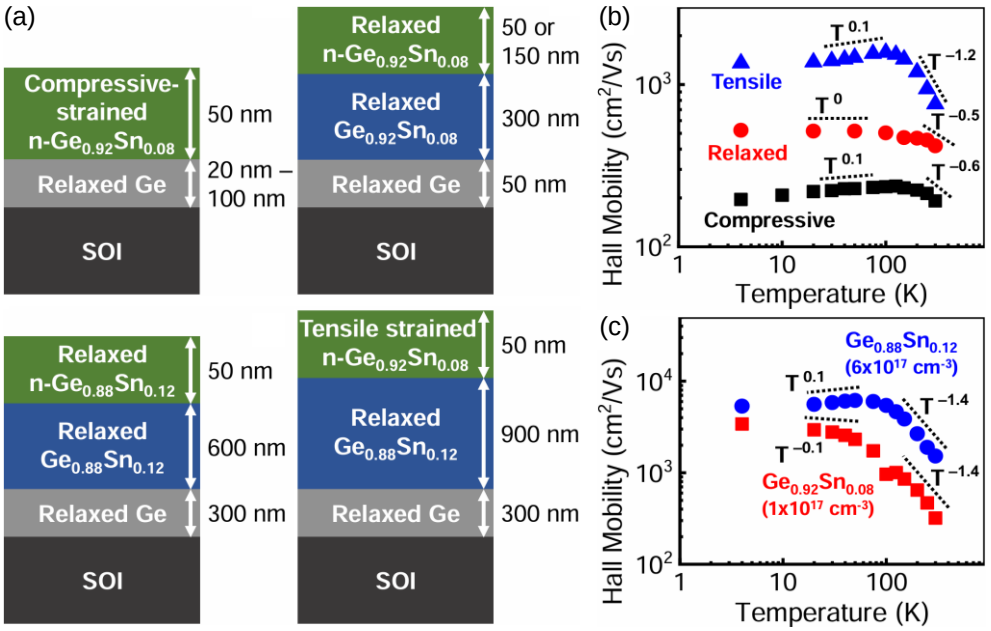

Fig. 3-1 (a) Epitaxial structures of the $Ge_{0.92}Sn_{0.08}$ and $Ge_{0.88}Sn_{0.12}$ films under different strain conditions. Hall mobility vs. temperature of (b) $Ge_{0.92}Sn_{0.08}$ films under different strain conditions as well as (c) strain-relaxed $Ge_{0.92}Sn_{0.08}$ and $Ge_{0.88}Sn_{0.12}$ films [9].

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In the low-temperature regime (T < 100 K), the Hall mobility of all GeSn films remains relatively constant with temperature (~ T^0) (Fig. 3-1 (b) and (c)), indicating that Coulomb scattering is the dominant scattering mechanism [9]. In the high-temperature regime, however, the power dependence of Hall mobility on temperature varies across the GeSn films. For the compressive-strained and strain-relaxed $Ge_{0.92}Sn_{0.08}$ films, the temperature dependence is approximately $T^{0.5}$ (Fig. 3-1 (b)), which is attributed to the alloy scattering [9]. A much higher temperature dependence of $T^{1.2}$ and $T^{1.4}$ is observed for the tensile-strained $Ge_{0.92}Sn_{0.08}$ film (Fig. 3-1 (b)) and strain-relaxed $Ge_{0.88}Sn_{0.12}$ film (Fig. 3-1 (c)), respectively. This is attributed to the mobility enhancement as a result of the direct-bandgap characteristics of tensile-strained $Ge_{0.92}Sn_{0.08}$ film and strain-relaxed $Ge_{0.88}Sn_{0.12}$ film [9]. To sum up, the effect of the indirect- to direct-bandgap transition in GeSn, achieved either by increasing tensile strain or Sn fraction, is manifested in the significant mobility enhancement and the abrupt increase in the power dependence of mobility on temperature.

The electron transport properties have also been reported in Ge(Sn) n-MOSFETs. For Ge n-MOSFETs (Fig. 3-2 (a)), the effective electron mobility exhibits a density dependence of $N_{inv}^{-1/3}$ at 250 K (Fig. 3-2 (b)), indicating that phonon scattering is the main factor that limits the mobility [79]. As the temperature decreases, the $N_{inv}^{-1/3}$ dependence

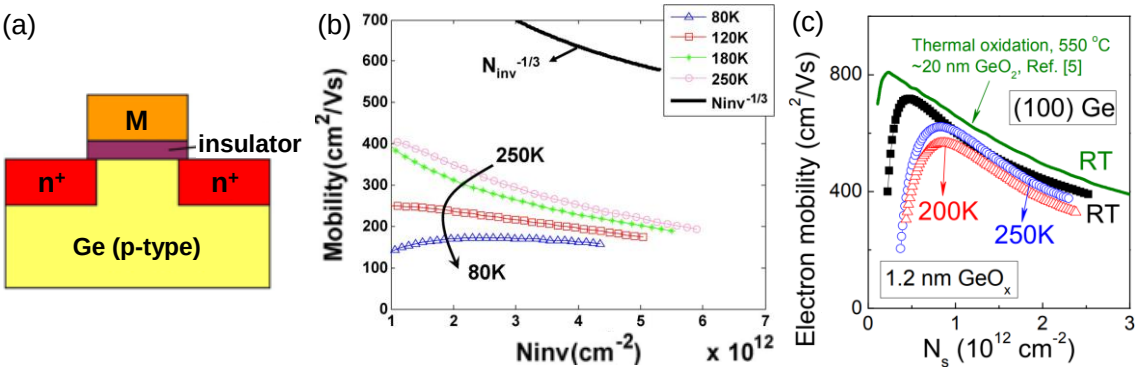

Fig. 3-2 (a) Device structure of a Ge n-MOSFET with its effective electron mobility vs. inversion carrier density (N_{inv} or N_s) at various temperatures reported in (b) [79] and (c) [33].

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vanishes, implying that phonon scattering is no longer the dominant scattering mechanism. However, the effective mobility does not increase despite the reduction in phonon scattering. Instead, a monotonic reduction in mobility with decreasing temperature is observed (Fig. 3-2 (b) and (c)). The reason is that in Ge n-MOSFETs, the oxide/semiconductor interface is worse than that of the pristine SiO_2/Si interface discussed in classical texts, thereby resulting in a higher interface trap charge density (D_{it}). This leads to a stronger Coulomb scattering, and consequently, the reduction in effective mobility with a decreasing temperature [33, 79].

The electron transport properties are also investigated in the compressively strained $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.815}Sn_{0.085}$ n-MOSFETs. Because the oxide/GeSn interface quality is even poorer than its oxide/Ge counterpart, thin layers of Ge are grown on top of the GeSn layers (Fig. 3-3 (a)) to improve the interface quality and reduce D_{it} [21]. Despite the effort, these devices do not benefit from the high electron mobility associated with the GeSn alloys. The effective electron mobility in the GeSn n-MOSFETs (Fig. 3-3 (b) and (c)) is lower than that reported for pure Ge channels (Fig. 3-2 (b) and (c)). This might be attributed to additional alloy scattering in the GeSn channels [78]. In addition, the effective electron mobility exhibits a monotonic decrease with a decreasing temperature (Fig. 3-3

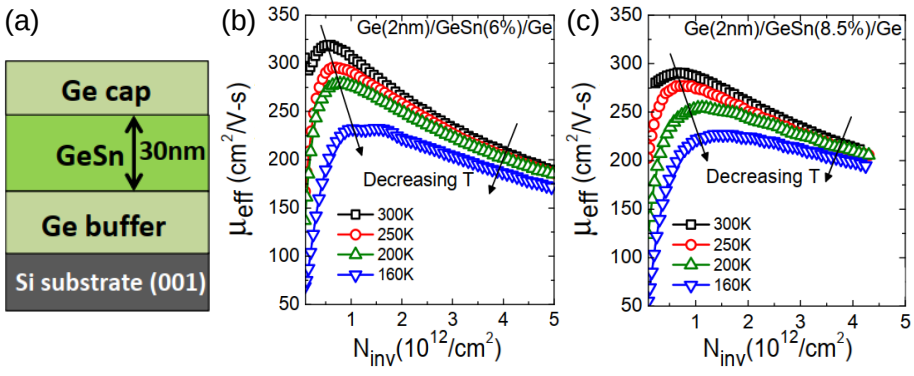

Fig. 3-3 (a) Epitaxial structure of the GeSn capped with a thin Ge layer. Effective electron mobility (μ_{eff}) vs. inversion carrier density (N_{inv}) of the (b) $Ge_{0.94}Sn_{0.06}$ and (c) $Ge_{0.915}Sn_{0.085}$ n-MOSFETs (with a 2-nm Ge capping layer) at various temperatures [21].

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(b) and (c)). This can be attributed to enhanced Coulomb scattering at a lower temperature due to the poor oxide/semiconductor interface [21], similar to that observed in the Ge n-MOSFETs [33, 79]. Unlike the electron transport observed in n-GeSn films (Fig. 3-1 (b) and (c)), no mobility enhancement with a decreasing temperature is observed in the GeSn n-MOSFETs (Fig. 3-3 (b) and (c)). This may stem from the GeSn channels not being sufficiently "direct", resulting in an inadequate population of high-mobility electrons in the Γ-valley at low temperatures, which fails to counteract the increased Coulomb scattering with decreasing temperature and enhance the mobility [9].

A more direct-bandgap-like GeSn channel material, such as the strain-relaxed $Ge_{0.895}Sn_{0.105}$ alloy in this work, is expected to exhibit a more dominant Γ-valley electron transport and enhance the electron mobility at low temperatures. As the temperature decreases, the Fermi-tail becomes sharper. The electron population in different valleys (Γ or L) becomes increasingly dependent on the energy difference between these two valleys [9]. Due to the large difference in electron effective masses between the Γ-valley and L-valley [17], very different temperature-dependent trends of mobility between the indirect-bandgap and direct-bandgap GeSn alloys are expected. Therefore, by investigating the cryogenic transport characteristics in the Ge(Sn) n-MOSFETs, the effects of indirect-to-direct bandgap transition in Ge(Sn) alloys on the electron transport properties can be understood.

3.2 Cryogenic Device Characteristics

3.2.1 Transfer I-V Characteristics

The normalized drain current (I_D) of the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs from 300 K to 4 K are plotted against the overdrive voltage (V_{OV}) (Fig. 3-4). For all devices, the threshold voltage exhibits a two-step increase as the temperature de-

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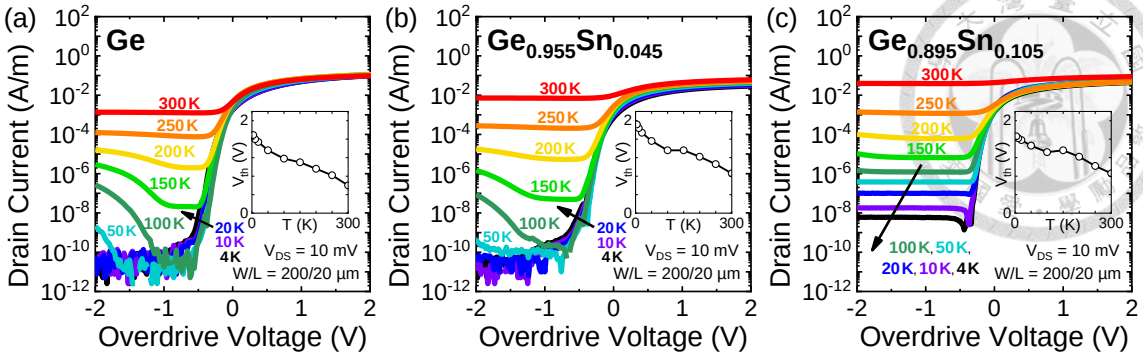

Fig. 3-4 Normalized drain current (I_D) vs. overdrive voltage (V_{OV}) of the (a) Ge, (b) $Ge_{0.955}Sn_{0.045}$, and (c) $Ge_{0.895}Sn_{0.105}$ n-MOSFETs from 300 K to 4 K. Threshold voltage (V_{th}) vs. temperature (T) of the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs are shown in the insets of (a), (b), and (c), respectively.

creases (insets of Fig. 3-4). The initial increase in V_{th} is attributed to the shift in bulk Fermi potential with temperature [80], while the second step of increase in V_{th} is attributed to the presence of interface traps [81]. The latter occurs because, at lower temperatures, MOSFETs require a larger surface band-bending to achieve strong inversion [31]. Due to the high interface trap density near the conduction band edge [82], a larger gate bias, or a larger threshold voltage, is required at lower temperatures to fill these traps before the surface inversion occurs [83].

As the temperature drops, I_D at $V_{OV} \sim -0.5$ V decreases for all devices. This is because I_D at $V_{OV} \sim -0.5$ V is governed by the drain-to-substrate junction leakage [11], which decreases at lower temperatures [66]. As V_{OV} decreases from –0.5 V to –2 V, the change in I_D is different across devices and temperatures. For the Ge and $Ge_{0.955}Sn_{0.045}$ n-MOSFETs (Fig. 3-4 (a) and (b)), increases in I_D are observed above 50 K, which is attributed to gate-induced drain leakage (GIDL) [22] caused by carrier tunneling at the gate-to-drain overlaps [67]. The effect of GIDL on I_D becomes more prominent at lower temperatures. This is because, in long-channel n-MOSFETs, the off-state leakage (I_D at $V_{OV} < -0.5$ V) comprises both junction leakage and GIDL [60], and the reduction in junction leakage at lower temperatures increases the relative contribution of GIDL to I_D. At tem-

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peratures below 50 K, GIDL drops below the current detection limit and is no longer observed [84]. In contrast, for the $Ge_{0.895}Sn_{0.105}$ n-MOSFET, GIDL is not observed at all temperatures (Fig. 3-4 (c)). By extracting the off-state current (I_{OFF}, I_D at V_{OV} ~ –0.5 V) from Fig. 3-4 and plotting it against temperature (Fig. 3-5 (a)), it is observed that the junction leakage in the $Ge_{0.895}Sn_{0.105}$ device is higher than the other low-Sn devices, possibly due to a smaller bandgap [19] and/or a worse junction quality [64]. Given that the off-state leakage comprises both junction leakage and GIDL [60], the high junction leakage in the $Ge_{0.895}Sn_{0.105}$ n-MOSFET may have obscured the relative contribution of GIDL to I_D.

The on-state drain current ($I_{ON,D}$, I_D at V_{OV} = 2 V) is extracted from Fig. 3-4 and plotted against temperature (Fig. 3-5 (b)). The on-state source current ($I_{ON,S}$, I_S at V_{OV} = 2 V) is also extracted from I_S-V_{OV} curves (not shown) for comparison (Fig. 3-5 (c)). A much larger $I_{ON,D}$ compared to $I_{ON,S}$ is observed at 300 K, which is attributed to the significantly higher I_{OFF} on the drain side than on the source side (Chapter 2.3.1). As the temperature drops, a peak in $I_{ON,D}$ ($I_{ON,S}$) with a 15% (16%) current enhancement is observed in the Ge n-MOSFET, while a monotonic decrease in both $I_{ON,D}$ and $I_{ON,S}$ are observed in the $Ge_{0.955}Sn_{0.045}$ n-MOSFET. For the $Ge_{0.895}Sn_{0.105}$ n-MOSFET, however, a peak in $I_{ON,D}$ ($I_{ON,S}$) with a 15% (21%) current enhancement is recovered, except that it

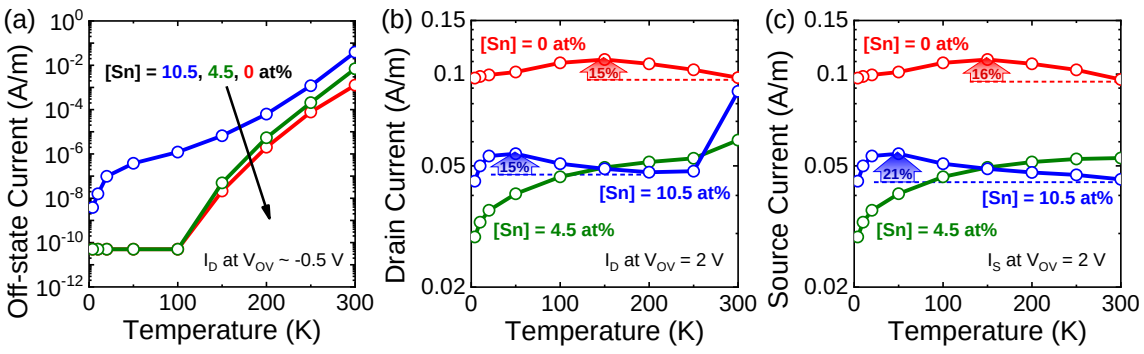

Fig. 3-5 (a) Off-state current (I_{OFF}, I_D at V_{OV} ~ –0.5 V), (b) on-state drain current ($I_{ON,D}$, I_D at V_{OV} = 2 V), and (c) on-state source current ($I_{ON,S}$, I_S at V_{OV} = 2 V) vs. temperature of the Ge(Sn) n-MOSFETs.

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occurs at a much lower temperature (50 K) compared to the Ge n-MOSFET (150 K). Because the on-state current is proportional to both electron density and mobility [30], their combined effects need to be decoupled using the split C-V method (Chapter 3.2.2) before investigating the physical mechanism responsible for the distinct temperature dependencies of the on-state current across devices (Chapter 3.3.2).

Using Fig. 3-5 (a) and (b), the on-off current ratio (I_{ON}/I_{OFF}) is obtained as a function of temperature (Fig. 3-6 (a)). For all devices, the monotonic increase in I_{ON}/I_{OFF} with decreasing temperature and increasing Sn fraction is attributed to the corresponding decrease in I_{OFF} (Fig. 3-5 (a)). This is because, across all devices and temperatures, I_{ON} stays on the same order (Fig. 3-5 (b)), while I_{OFF} differs by several orders of magnitude (Fig. 3-5 (a)). From Fig. 3-4, the minimum subthreshold swing (SS_{min}) is extracted and plotted against temperature (Fig. 3-6 (b)). As the temperature decreases, SS_{min} of all devices decreases monotonically, which is attributed to the suppressed thermal tail in the Fermi-Dirac distribution [85]. Due to the finite depletion capacitance and interface trap capacitance, SS_{min} remains strictly above the Boltzmann limit [86]. In addition, at low temperatures, SS_{min} levels off and deviates significantly from the Boltzmann limit. This can be attributed to the presence of band-tail states, possibly originating from crystalline disorders in the MOSFET channels [86]. SS_{min} vs. temperature is also extracted from I_S-V_{OV}

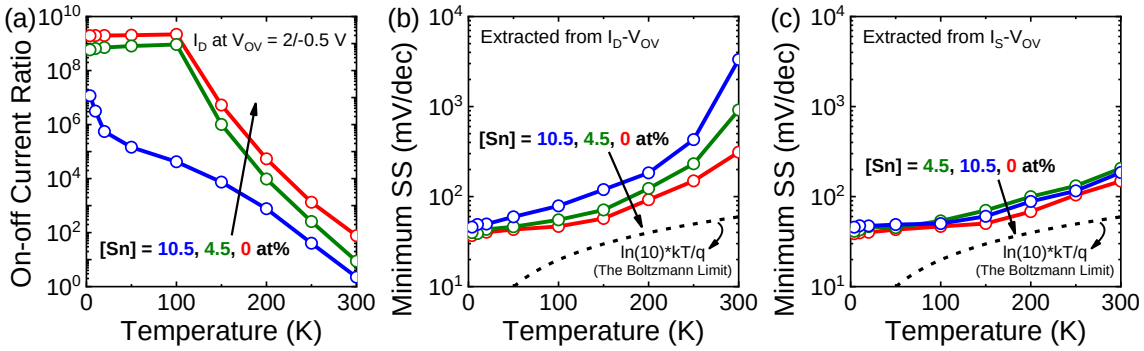

Fig. 3-6 (a) On-off current ratio (I_{ON}/I_{OFF}), minimum subthreshold swing (SS_{min}) extracted from (b) I_D-V_{OV} curves (Fig. 3-4) and (c) I_S-V_{OV} curves (not shown) vs. temperature of the Ge(Sn) n-MOSFETs.

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curves (not shown) for comparison (Fig. 3-6 (c)). Around 300 K, the SS_{min} extracted from the I_S-V_{OV} curves are much smaller than those extracted from the I_D-V_{OV} curves (Fig. 3-6 (b)). This is attributed to the significantly higher I_{OFF} on the drain side than on the source side, obscuring the subthreshold characteristics of I_D (Chapter 2.3.1).

3.2.2 Split C-V Characteristics

The normalized gate-to-channel capacitance (C_{GC}) of the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs from 300 K to 4 K is plotted against V_{OV} to rule out the effect of V_{th} variation (Fig. 3-7). The frequency of measurement is selected to be 50 kHz to reduce the effects of interface traps and channel resistance on C_{GC} (Chapter 2.3.4). The C_{GC}-V_{OV} curves of all devices exhibit asymmetric V-shapes, with the asymmetry becoming more pronounced as the temperature decreases. In the strong inversion regime (V_{OV} = 2 V), all C_{GC}-V_{OV} curves attain their maxima due to the presence of inversion channels [25]. When transitioning into the depletion regime (V_{OV} ~ –0.5 V), a drastic reduction in C_{GC} with decreasing V_{OV} is observed across all curves due to the depletion of the inversion channels [25]. As the temperature decreases, the "subthreshold" slopes of the C_{GC}-V_{OV} curves across all devices steepen due to a sharper MOSFET turn-on characteristics [31] at lower temperatures (Fig. 3-4). When transitioning further into the accumulation

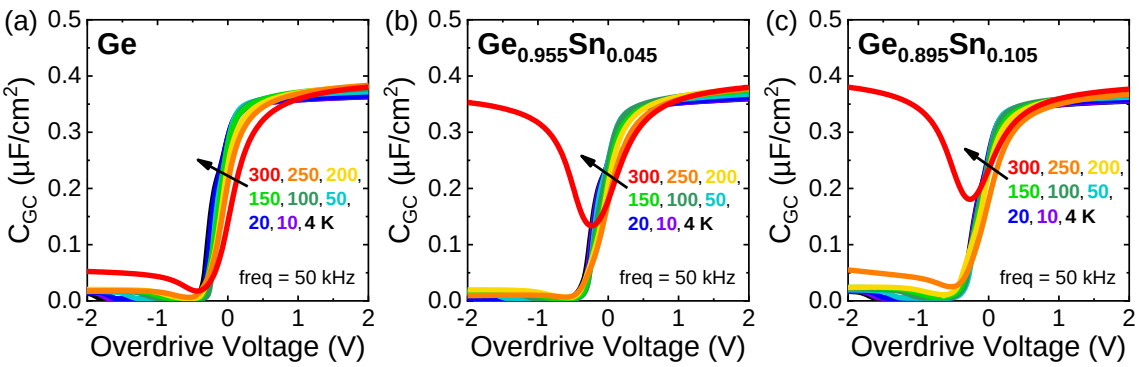

Fig. 3-7 Normalized gate-to-channel capacitance (C_{GC}) vs. V_{OV} of the (a) Ge, (b) $Ge_{0.955}Sn_{0.045}$, and (c) $Ge_{0.895}Sn_{0.105}$ n-MOSFETs measured with frequencies of 50 kHz from 300 K to 4 K.

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regime (V_{OV} = –2 V), an increase in C_{GC} with decreasing V_{OV} is observed across all curves, even at low temperatures. This deviates from the standard split C-V characteristics [25], and the potential causes are elaborated as follows.

The C_{GC} measured in the accumulation, depletion, and strong inversion regimes are extracted from Fig. 3-7 and plotted against temperature (Fig. 3-8). Because the Ge(Sn) n-MOSFETs are fabricated using a gate-first process, both gate-to-source and gate-to-drain overlaps are negligible. Therefore, in both the accumulation and depletion regimes, the abnormally high C_{GC} (Fig. 3-8 (a) and (b)) cannot be attributed to the overlap capacitance (Fig. 2-10 (a)). Instead, at 300 K, it is attributed to the significant junction leakage and GIDL (Chapter 2.3.2). As the temperature decreases to 200 K, a drastic reduction in C_{GC} is observed across all devices; below 200 K, C_{GC} remains low and relatively constant for all devices (Fig. 3-8 (a) and (b)). This, by analogy with the case at 300 K, may be attributed to the suppressed junction leakage at lower temperatures (Fig. 3-5 (a)).

In the strong inversion regime, C_{GC} reaches approximately 0.36 μF/cm^2 across all devices and all temperatures (Fig. 3-8 (c)). A dielectric constant for the gate oxide (Al_2O_3) is extracted as ~ 6.2, which is close to the reported value of ~ 6.5 [70]. At 300 K, the Sn-fraction dependence of C_{GC} is attributed to the variation in $4G_{ch} + 2G_j$ (Chapter 2.3.2). As the temperature decreases, a slight variation in C_{GC} is observed across all devices (Fig.

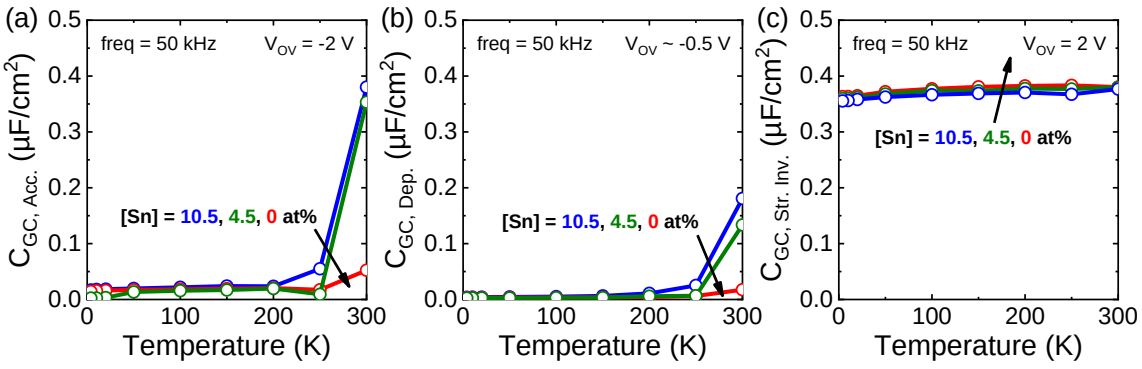

Fig. 3-8 C_{GC} vs. temperature in the (a) accumulation (V_{OV} = –2 V), (b) depletion (V_{OV} ~ –0.5 V), and (c) strong inversion (V_{OV} = 2 V) regimes of the Ge(Sn) n-MOSFETs measured with frequencies of 50 kHz.

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3-8 (c)). This, in analogy to the case at 300 K, may be attributed to the variation of $4G_{ch} + 2G_j$ with temperature. Note that none of the temperature-dependent split C-V behaviors observed in Fig. 3-8 have been reported elsewhere. Therefore, the preceding arguments require validation, which is presented as follows.

To elucidate the temperature-dependent split C-V characteristics, models of the AC carrier transport mechanisms in the Ge(Sn) n-MOSFETs in the split C-V configuration at temperatures ranging from 300 K to 4 K are proposed. The transport mechanisms are identical to those at 300 K (Fig. 2-25, Fig. 2-28, and Fig. 2-31), except that the junction leakages decrease with decreasing temperature. Eventually, at the lowest temperature of 4 K, the junction leakages are effectively suppressed (Fig. 3-9). This is the same as the conventional Si n-MOSFETs [25], where the ammeter connected to the source/drain only picks up AC current either in the accumulation or the strong inversion regime.

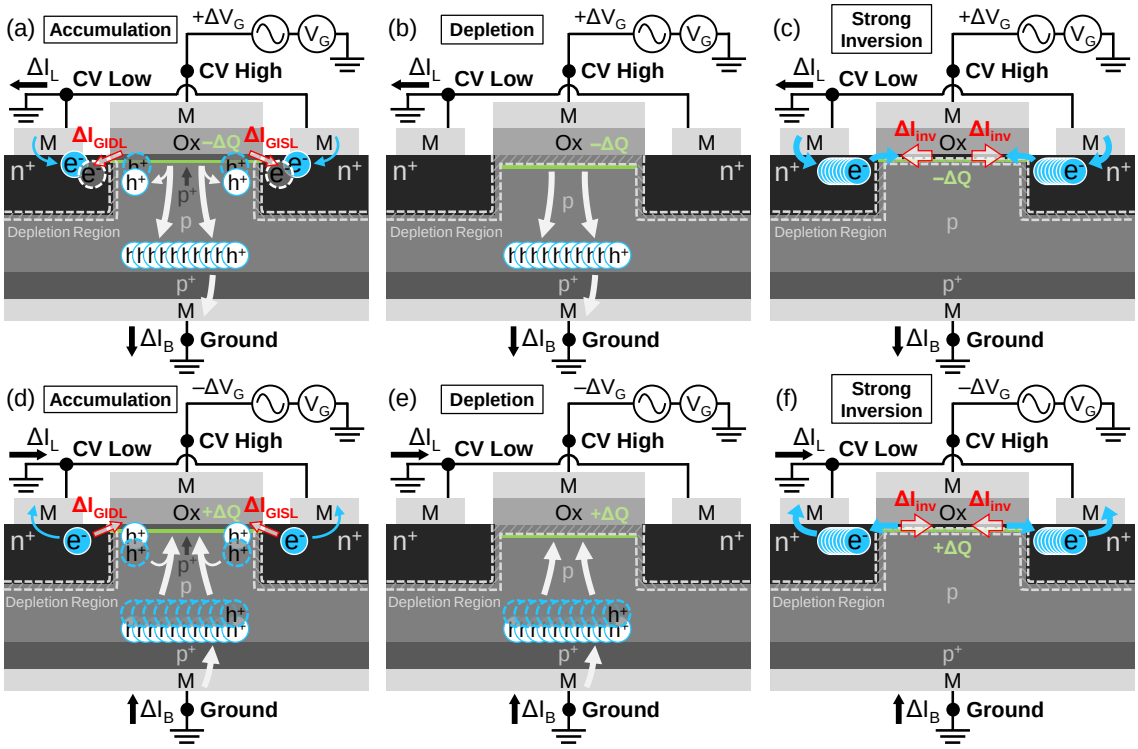

Fig. 3-9 Schematics showing the AC carrier transport mechanisms in the Ge(Sn) n-MOSFETs during the positive/negative half of an AC cycle of the split C-V measurements in the (a/d) accumulation, (b/e) depletion, and (c/f) strong inversion regimes at the lowest temperature of 4 K.

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By extending a concept from [72], physically based equivalent small-signal circuit models of the Ge(Sn) n-MOSFETs during spilt C-V measurements at temperatures ranging from 300 K to 4 K are constructed (Fig. 3-10). Based on the AC carrier transport mechanisms elaborated in the previous paragraph, the circuit models are made identical to those at 300 K (Fig. 2-26 (a), Fig. 2-29 (a), and Fig. 2-32 (a)), except for some differences. The carrier storage properties at the surface are modeled by oxide capacitance (C_{ox}), overlap capacitance (C_{ov}), accumulation capacitance (C_A), depletion capacitance (C_D), and inversion capacitance (C_I) [25], except that C_A, C_D, and C_I are functions of temperature T. The dissipative carrier transports are modeled by bulk conductance (G_B), GIDL conductance (G_{GIDL}), junction conductance (G_j), generation-recombination conductance (G_{gr}), and channel conductance (G_{ch}), except that G_{GIDL}, G_j, G_{gr}, and G_{ch} are functions of temperature T.

In the accumulation regime, the circuit capacitance C of the small-signal model (Fig. 3-10 (a)) is derived from the imaginary part of the ratio i_x/v_x [69] as

$$C = \frac{1}{\omega}\mathrm{Im}\left(\frac{i_x}{v_x}\right) = C_0 \cdot \frac{1}{1+(\omega/\omega_c)^2} + 2C_{ov}\,, \tag{3-1}$$

where

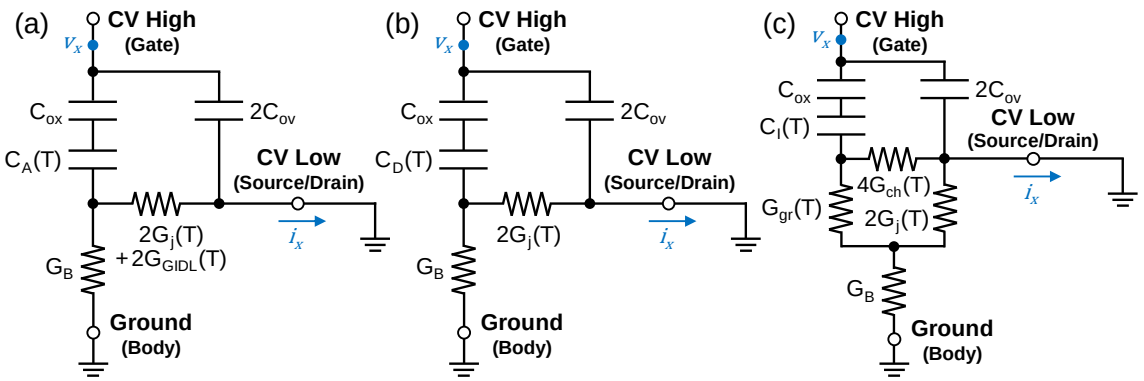

Fig. 3-10 Equivalent small-signal circuit models of the Ge(Sn) n-MOSFETs biased in the (a) accumulation, (b) depletion, and (c) strong inversion regimes at temperatures ranging from 300 K to 4 K.

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$$C_0 = \frac{C_{ox} \parallel C_A(T)}{1 + \dfrac{G_B}{2G_j(T) + 2G_{GIDL}(T)}} \tag{3-2}$$

and

$$\omega_c = \frac{G_B + 2G_j(T) + 2G_{GIDL}(T)}{C_{ox} \parallel C_A(T)}. \tag{3-3}$$

The assumptions and derivations are identical to those stated in Appendix A.1.

The low-pass form in Equation (3-1) predicts that once the angular frequency ω exceeds the cut-off frequency ω_c, a two-orders-of-magnitude reduction in C from its constant value C_0 per decade increase in ω is expected [69], before approaching the lower limit of $2C_{ov}$ (overlap capacitance). Such behavior occurs because as ω increases above ω_c, the reactance of $C_{ox} \parallel C_A(T)$ drops below the reciprocal of $G_B + 2G_j(T) + 2G_{GIDL}(T)$ (Equations (3-1) and (3-3)). Consequently, the energy stored in $C_{ox} \parallel C_A(T)$ becomes less than that dissipated through $G_B + 2G_j(T) + 2G_{GIDL}(T)$ [69], significantly attenuating the capacitive behavior of the circuit (Equations (3-1)). This prediction is validated by the log-log plot of C_{GC} vs. ω (replotted from Fig. 3-8 (a) and data measured at other frequencies, not shown), where the curves fitted by Equation (3-1) closely match the experimental data at 300 K across all devices (Fig. 3-11). The data below 300 K deviate from the char-

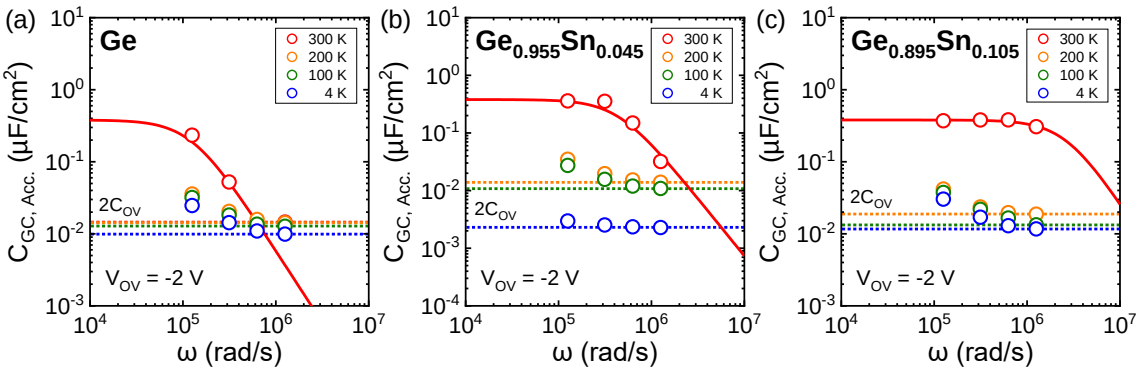

Fig. 3-11 C_{GC} vs. angular frequency ω (replotted from Fig. 3-8 (a) and data measured at other frequencies, not shown) of the (a) Ge, (b) $Ge_{0.955}Sn_{0.045}$, and (c) $Ge_{0.895}Sn_{0.105}$ n-MOSFETs in the accumulation regime at 300 K, 200 K, 100 K and 4 K.

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acteristic reduction in capacitance with increasing frequency predicted by Equation (3-1). Instead, they exhibit saturation in the high-frequency limit. This behavior arises because C_{GC} diminishes significantly at lower temperatures (Fig. 3-11), thereby saturating at its lower bound of $2C_{ov}$ (Equation (3-1)).

In fact, the reduction in C_{GC} with decreasing temperature (Fig. 3-11) is consistent with the prediction by the small-signal model. Specifically, Equation (3-1) anticipates a reduction in the circuit capacitance C as the temperature decreases. This occurs because both C_0 and ω_c decrease as $2G_{GIDL}(T) + 2G_j(T)$ decreases (Equations (3-2) and (3-3)), where the off-state leakage, and consequently $2G_{GIDL}(T) + 2G_j(T)$, diminishes significantly as the temperature drops (Fig. 3-4). Note that $C_A(T)$ has a negligible effect on the temperature dependence of C_0 and ω_c (Equations (3-2) and (3-3)), because $C_A(T)$ is very large in the accumulation regime [25]. This makes the term $C_{ox} \parallel C_A(T) \sim C_{ox}$ (temperature-independent), which effectively suppresses the temperature dependence contributed by $C_A(T)$.

The preceding analyses confirm that the AC behaviors of the Ge(Sn) n-MOSFETs from 300 K to 4 K are qualitatively captured by the small-signal model. Therefore, the temperature-dependent split C-V characteristics can be interpreted based on the model. At 300 K, the anomalously high C_{GC} (Fig. 3-8 (a)) is attributed to a large $2G_j + 2G_{GIDL}$, because this implies a large C_0 and ω_c (Equations (3-2) and (3-3)), and consequently, a large C (Equation (3-1)). As the temperature decreases, the reduction in C_{GC} (Fig. 3-8 (a)) is attributed to the corresponding reduction in $2G_j(T) + 2G_{GIDL}(T)$, because this implies a decrease in C_0 and ω_c (Equations (3-2) and (3-3)), and consequently, a decrease in C (Equation (3-1)). From a physical standpoint, this originates from a diminished supply of majority carriers across the junctions in response to the AC signal as the temperature decreases (Fig. 3-9 (a) and (d)), which is evidenced by the corresponding reduction in off-

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state leakage (Fig. 3-5 (a)).

In the depletion regime, the circuit capacitance C of the physically based small-signal model (Fig. 3-10 (b)) takes on the same form as that in Equation (3-1), except that C_0 and ω_c become

$$C_0 = \frac{C_{ox} \parallel C_D(T)}{1 + \frac{G_B}{2G_j(T)}} \tag{3-4}$$

and

$$\omega_c = \frac{G_B + 2G_j(T)}{C_{ox} \parallel C_D(T)}, \tag{3-5}$$

respectively. The assumptions and derivations are identical to those stated in Appendix A.2. The following analyses parallel those in the accumulation regime. First, the fitted curves closely match the experimental data at 300 K across all devices (Fig. 3-12), which validates the prediction of Equation (3-1). Moreover, Equation (3-1) predicts a reduction in circuit capacitance C as the temperature decreases, because both C_0 and ω_c decrease as $2G_j(T)$ decreases (Equations (3-4) and (3-5)), where I_{OFF}, and consequently $2G_j(T)$, diminishes significantly as the temperature drops (Fig. 3-5 (a)). This is validated by the reduction in C_{GC} with decreasing temperature (Fig. 3-12), which eventually results in the

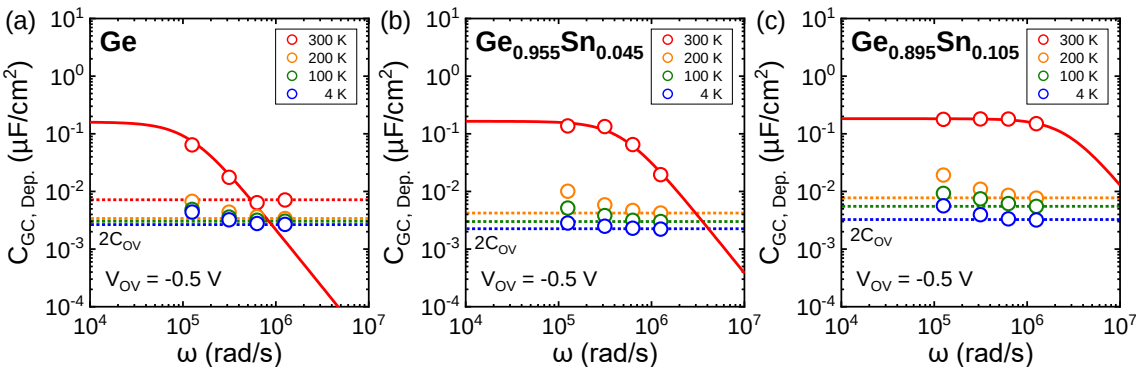

Fig. 3-12 C_{GC} vs. angular frequency ω (replotted from Fig. 3-8 (b) and data measured at other frequencies, not shown) of the (a) Ge, (b) $Ge_{0.955}Sn_{0.045}$, and (c) $Ge_{0.895}Sn_{0.105}$ n-MOSFETs in the depletion regime at 300 K, 200 K, 100 K and 4 K.

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saturation of C_{GC} at its lower bound $2C_{ov}$ (Equation (3-1)).

Similar to the case in the accumulation regime, interpretations regarding the temperature-dependent split C-V characteristics in the depletion regime are made based on the small-signal model. At 300 K, the anomalously high C_{GC} (Fig. 3-8 (b)) is attributed to a large $2G_j$, because this implies a large C_0 and ω_c (Equations (3-4) and (3-5)), and consequently, a large C (Equation (3-1)). As the temperature decreases, the reduction in C_{GC} (Fig. 3-8 (b)) is attributed to the corresponding reduction in $2G_j(T)$, because this implies a decrease in C_0 and ω_c (Equations (3-4) and (3-5)), and consequently, a decrease in C (Equation (3-1)). From a physical standpoint, this originates from a diminished supply of majority carriers across the junctions in response to the AC signal as the temperature decreases (Fig. 3-9 (b) and (e)), which is evidenced by the corresponding reduction in off-state leakage (Fig. 3-5 (a)).

In the strong inversion regime, the circuit capacitance C of the physically based small-signal model (Fig. 3-10 (c)) takes on the same form as that in Equation (3-1), except that C_0 and ω_c become

$$C_0 = \frac{C_{ox} \parallel C_I(T)}{1 + \dfrac{\alpha(T)G_B}{4G_{ch}(T) + 2\alpha(T)G_j(T)}} \tag{3-6}$$

and

$$\omega_c = \frac{4G_{ch}(T) + \alpha(T)\left[G_B + 2G_j(T)\right]}{C_{ox} \parallel C_I(T)}, \tag{3-7}$$

respectively, where

$$\alpha(T) = \left[1 + \left[G_B + 2G_j(T)\right]/G_{gr}(T)\right]^{-1} \tag{3-8}$$

is a dimensionless quantity smaller than unity. The assumptions and derivations are identical to those stated in Appendix A.3. In contrast to the case in both the accumulation and depletion regimes, the curves fitted using Equation (3-1) closely match the experimental

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data at temperatures down to 4 K across all devices (Fig. 3-13). This indicates that the cryogenic frequency response of C_{GC} is satisfactorily captured by the small-signal model (Equation (3-1)).

At 300 K, a first-order approximation $G_{gr} \gg 2G_j$ is made because the surface area is much larger compared to the junction area (Chapter 2.3.2). Combining with the fact that the junctions of the Ge(Sn) n-MOSFETs are leaky ($2G_j \gg G_B$), α can be approximated as one. Using the fact that the surface is heavily inverted ($4G_{ch} \gg G_B$), Equations (3-6) and (3-7) predict C_0 to be independent of $4G_{ch} + 2G_j$ and ω_c to be linear in $4G_{ch} + 2G_j$, respectively. At the lowest temperature of 4 K, G_{gr} and G_j are effectively suppressed ($G_{gr} = G_j \sim 0$) because both conductance account for the GR processes [61, 65]. Therefore, α can be approximated as zero, and thus Equations (3-6) and (3-7) predict C_0 to be independent of

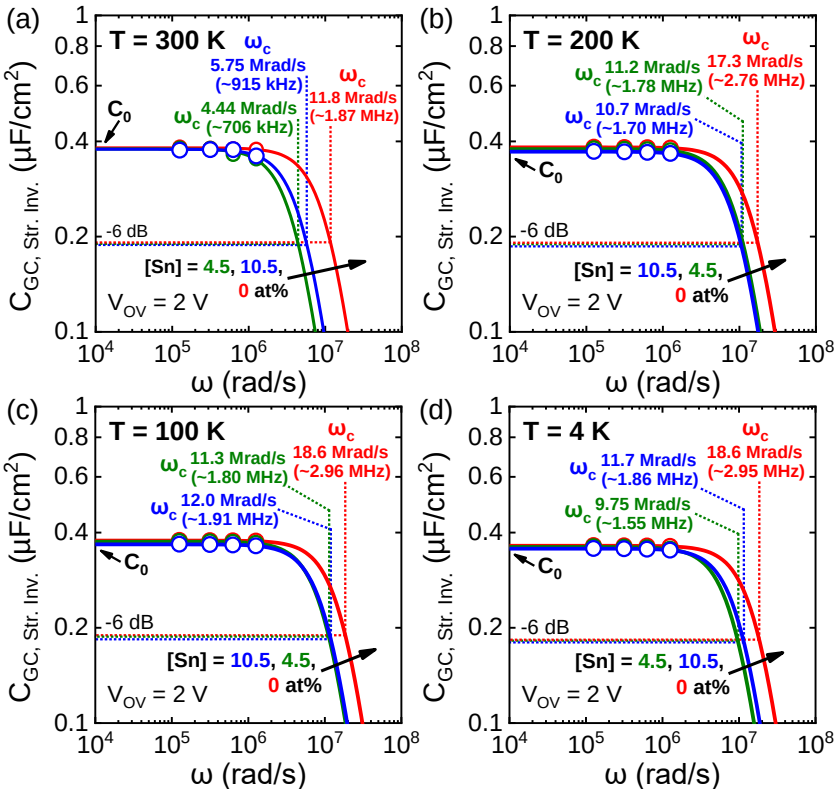

Fig. 3-13 C_{GC} vs. angular frequency ω (replotted from Fig. 3-8 (c) and data measured at other frequencies, not shown) of the Ge(Sn) n-MOSFETs in the strong inversion regime at (a) 300 K, (b) 200 K, (c) 100 K, and (d) 4 K.

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$4G_{ch}$ and ω_c to be linear in $4G_{ch}$, respectively. An intuitive interpolation can be made at temperatures between 300 K and 4 K: C_0 is expected to be independent of $4G_{ch}(T) + 2G_j(T)$, while ω_c is expected to be linear in $4G_{ch}(T) + 2G_j(T)$. This is justified by the fact that, as the temperature decreases, $2G_j(T)$ decreases, thereby causing the term $4G_{ch}(T) + 2G_j(T)$ to transition from the room-temperature limit of $4G_{ch} + 2G_j$ to the low-temperature limit of $4G_{ch}$.

The fitting parameters (used in Fig. 3-13) and $4I_{ON} + 2I_{OFF}$ (excerpted from Fig. 3-5 (a) and (c)) at temperatures down to 4 K are shown in Fig. 3-14. By using the Sn fraction as an intermediate parameter, C_0 and ω_c are found to be weakly dependent on and linear in $4I_{ON} + 2I_{OFF}$ at temperatures down to 4 K, respectively (Fig. 3-15). Because I_{ON} and I_{OFF} comprises the inversion current and junction leakage, respectively (Chapter 3.2.1),

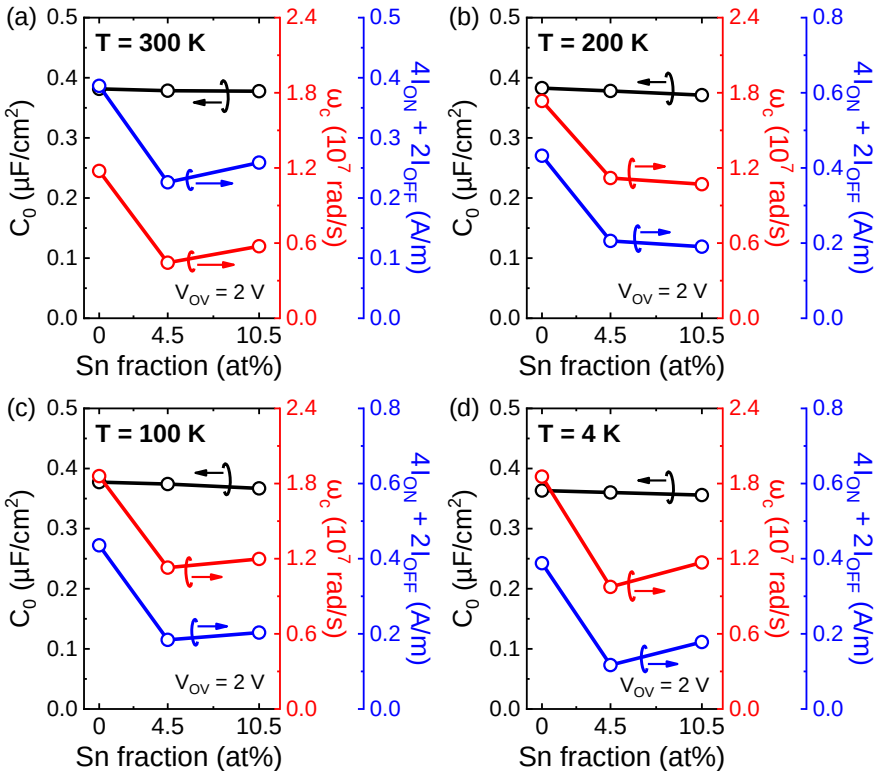

Fig. 3-14 Fitting parameters C_0 and ω_c (used in Fig. 3-13) as well as $4I_{ON} + 2I_{OFF}$ (excerpted from Fig. 3-5 (a) and (c)) vs. Sn fraction at (a) 300 K, (b) 200 K, (c) 100 K, and (d) 4 K. (b) C_0 and ω_c (from (a)) vs. $4I_{ON} + 2I_{OFF}$ (from (a)).

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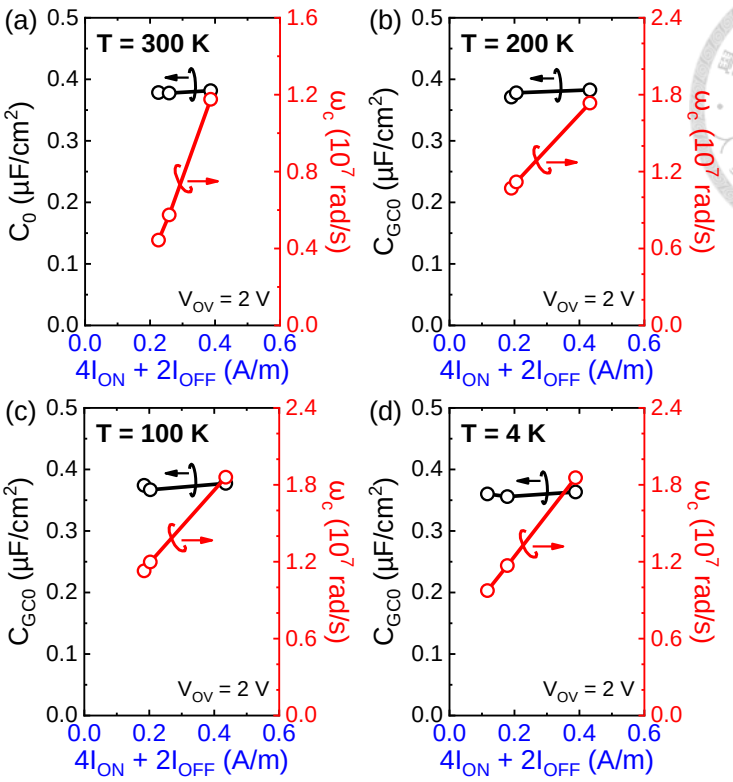

Fig. 3-15 Fitting parameters C_0 and ω_c (used in Fig. 3-13) as well as $4I_{ON} + 2I_{OFF}$ (excerpted from Fig. 3-5 (a) and (c)) vs. Sn fraction at (a) 300 K, (b) 200 K, (c) 100 K, and (d) 4 K. (b) C_0 and ω_c (from (a)) vs. $4I_{ON} + 2I_{OFF}$ (from (a)).

i.e., $4I_{ON} + 2I_{OFF}$ is proportional to $4G_{ch}(T) + 2G_j(T)$, it follows that C_0 and ω_c are weakly dependent on and linear in $4G_{ch}(T) + 2G_j(T)$ at temperatures down to 4 K, respectively. These findings validate the predictions made by the small-signal model (Equations (3-6) and (3-7)).

The preceding analyses confirm that the AC behaviors of the Ge(Sn) n-MOSFETs from 300 K to 4 K are well-characterized by the small-signal model. Therefore, the temperature-dependent split C-V characteristics can be interpreted based on the model. Across all device, the temperature dependence of C_{GC} (Fig. 3-8 (c)) is attributed to the variation in $4G_{ch}(T) + 2G_j(T)$. This is because the circuit capacitance C depends on both C_0 and ω_c (Equation (3-1)), where C_0 and ω_c are linked to a dependence on $4I_{ON} + 2I_{OFF}$ (Fig. 3-15), and consequently to $4G_{ch}(T) + 2G_j(T)$, through Equations (3-6) and (3-7).

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Note that $C_I(T)$ does not contribute to the temperature dependence of either C_0 or ω_c. This is because $C_I(T)$ is very large in the strong inversion regime [25], making the term $C_{ox} \parallel C_I(T) \sim C_{ox}$ (temperature-independent), which effectively suppresses the temperature dependence contributed by $C_I(T)$. From a physical standpoint, this originates from the temperature-dependent supply of minority carriers by both the channel and the junctions in response to the AC signal (Fig. 3-9 (c) and (f)).

To sum up, in both the accumulation and depletion regimes, the reduction in C_{GC} with decreasing temperature (Fig. 3-8 (a) and (b)) is attributed to the corresponding decrease in the supply of majority carriers across the junctions in response to the AC signal (Fig. 3-9 (a), (b), (d), and (e)). Therefore, standard split C-V characteristics are recovered at low temperatures across all device. In the strong inversion regime, the temperature dependence of C_{GC} (Fig. 3-8 (c)) is attributed to the temperature-dependent supply of minority carriers by both the channel and the junctions in response to the AC signal (Fig. 3-9 (c) and (f)). This implies that in Ge(Sn) n-MOSFETs, both inversion carrier transport and junction leakages contribute to the on-state gate-to-channel capacitance.

3.3 Electron Mobility in Ge(Sn) n-MOSFETs

3.3.1 Effective Mobility vs. Inversion Carrier Density

The effective mobility (μ_{eff}) extracted from drain current (I_D) (Fig. 3-4) is plotted against the inversion carrier density (N_{inv}) for the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs (Fig. 3-16). Similar to the case at 300 K, the frequency is chosen as 50 kHz (Fig. 3-7) to reduce the effect of interface trap capacitance [25, 32] and channel resistance [32, 72, 77] (Chapter 2.3.4). Only the data above threshold voltage ($V_{OV} > 0$ V) are displayed, because the split C-V method assumes that the inversion current is predominantly drift current rather than diffusion current (Chapter 2.2.3). Besides, the data with an

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I_{ON}/I_{OFF} ratio smaller than 10^2 are omitted to avoid the overestimation of effective mobility due to the high off-state leakage (Chapter 2.3.4).

In the low-density regime (N_{inv} = 5 x 10^{11} cm^{-2}), the effective mobility increases with the inversion charge density for all Ge(Sn) n-MOSFETs (Fig. 3-16). This is attributed to the screening effect on Coulomb scattering [74, 75, 87]. As the inversion charge density increases, the impurity potential is screened more effectively, because there are more "polarized" electrons to move around and contribute to the screening process. This results in a weaker Coulomb scattering and, consequently, an increase in effective mobility with inversion carrier density. As the temperature decreases, the density dependence of effective mobility increases from $N_{inv}^{0.5}$, $N_{inv}^{0.55}$, and $N_{inv}^{0.75}$ to $N_{inv}^{1.05}$, $N_{inv}^{1.15}$, and $N_{inv}^{1.4}$ for the Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs, respectively (Fig. 3-16). This is attributed to an enhanced screening effect [31, 88], because electrons are more easily "polarized" to contributed to screening at lower temperatures due to a sharper Fermi-Dirac distribution (Appendix B.4.2). Besides, as the Sn fraction increases, the power of the density dependence of effective mobility becomes higher (Fig. 3-16). This can be attributed to the higher interface trap density (D_{it}) [74] at the Al_2O_3/Ge(Sn) interface of devices with a higher Sn fraction [21, 55].

In the intermediate-density regime (N_{inv} = 1 x 10^{12} cm^{-2}), characteristics plateaus

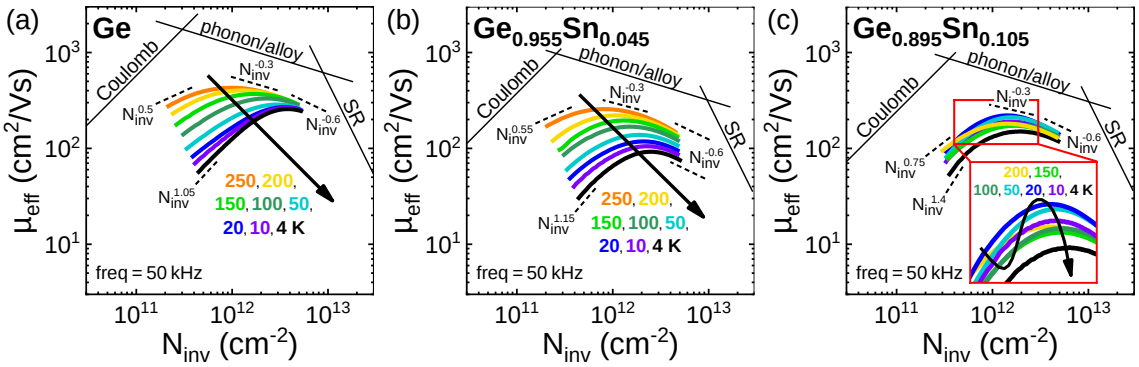

Fig. 3-16 Effective mobility (μ_{eff}) vs. inversion carrier density (N_{inv}) of the (a) Ge, (c) $Ge_{0.955}Sn_{0.045}$, and (e) $Ge_{0.895}Sn_{0.105}$ n-MOSFETs (extracted from I_D (Fig. 3-4) and C_{GC} at 50 kHz (Fig. 3-7)).

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with a density dependence of $N_{inv}^{-0.3}$ is observed across all devices at high temperatures (Fig. 3-16). This is attributed to phonon scattering [31] or alloy scattering [89]. As the temperature decreases, the characteristic plateau in the Ge and $Ge_{0.955}Sn_{0.045}$ n-MOSFETs become less prominent, indicating a weaker phonon and alloy scattering at lower temperatures. The $N_{inv}^{-0.3}$ plateau for the $Ge_{0.895}Sn_{0.105}$ n-MOSFET, however, appears to persist down to cryogenic temperatures. This could be attributed to stronger alloy scattering [78] compared to the other devices with lower Sn fractions. Lastly, in the high-density regime (N_{inv} = 5 x 10^{12} cm^{-2}), the density dependence of effective mobility becomes $N_{inv}^{-0.6}$ for all devices across all temperatures (Fig. 3-16), which is attributed to an increased influence of the surface roughness (SR) scattering [74].

3.3.2 Effective Mobility vs. Temperature

The effective mobility in various density regimes (Fig. 3-16) is extracted and plotted against temperature (Fig. 3-17 and Fig. 3-20). In the low-density regime (N_{inv} = 5 x 10^{11} cm^{-2}), a peak effective mobility is observed in the conventional Si n-MOSFET (Fig. 3-17), which is attributed to the competition between the reduction of phonon scattering and the enhancement of Coulomb scattering as the temperature decreases [31]. For the Ge and $Ge_{0.955}Sn_{0.045}$ n-MOSFETs, however, no peak in effective mobility is observed. Instead, the effective mobility decreases monotonically with a decreasing temperature. This is attributed to stronger Coulomb scattering in the Ge(Sn) n-MOSFETs than that in the Si n-MOSFET as a result of a higher D_{it} at the Al_2O_3/Ge(Sn) interface [21, 55] compared to that at the SiO_2/Si interface [31], considering that the impurity concentration of the Ge(Sn) substrates (Chapter 2.2.1) and the Si substrates [31] are similar (~ 10^{16} cm^{-3}). As the temperature decreases, the temperature dependence of effective mobility is reduced from $T^{0.7}$ to $T^{0.3}$, indicating that the mobility degradation is mitigated at lower temperatures. This

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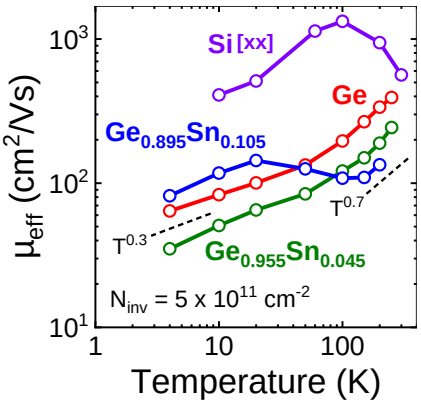

Fig. 3-17 μ_{eff} vs. temperature of the Si [31] and Ge(Sn) n-MOSFETs (extracted from Fig. 3-16) in the low-density regime (N_{inv} = 5 x 10^{11} cm^{-2}).

could be attributed to an enhanced screening effect at lower temperatures, where electrons become more easily "polarized", and consequently, more effective at screening the perturbing potential introduced by the impurities (Appendix B.4.2).

For the $Ge_{0.895}Sn_{0.105}$ n-MOSFET, however, an anomalous mobility upturn is observed between 100 K and 20 K (Fig. 3-17). The decrease in effective mobility as the temperature decreases from 200 K to 150 K and from 20 K to 4 K can be attributed to Coulomb scattering as a result of the high D_{it} at the poor oxide/Ge(Sn) interface [21]. However, the anomalous increase in effective mobility as the temperature drops from 100 K to 20 K cannot be explained by any of the scattering mechanisms in n-MOSFETs. On one hand, phonon scattering is weak at low temperatures [74, 75], and thus it cannot contribute to the increase in effective mobility. On the other hand, Coulomb, alloy, and surface roughness scattering are stronger in the $Ge_{0.895}Sn_{0.105}$ device compared to the other low-Sn devices due to a higher D_{it} [21, 55], a higher Sn fraction, and a larger surface roughness (Fig. 2-8), respectively. Therefore, an even more severe mobility degradation with decreasing temperature would be expected, contradicting the observed increase in effective mobility.

An additional transport mechanism, i.e., the *dual-valley electron transport* [9], can

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explain the anomalous mobility upturn in the $Ge_{0.895}Sn_{0.105}$ n-MOSFET. In Ge(Sn) alloys, two conduction-band valleys (Γ and L) are close in energy. According to Fermi-Dirac statistics, electrons occupy both the Γ- and L-valleys (Fig. 3-18). Thus, even though all electrons are in the same physical space (the inversion channel), they transport with different effective masses and mobilities [9]. The overall electron mobility μ is expressed as a weighted average of the mobility in the Γ-valley (μ_Γ) and the L-valley (μ_L) [17]:

$$\mu = \frac{n_\Gamma \mu_\Gamma + n_L \mu_L}{n_\Gamma + n_L} = \frac{(n_\Gamma / n_L)\mu_\Gamma + \mu_L}{n_\Gamma / n_L + 1}, \tag{3-9}$$

where the n_Γ and n_L represents the electron population in the Γ-valley and L-valley, respectively. When the ratio of electron population in the Γ-valley relative to that in the L-valley, i.e., n_Γ/n_L, is large (small), μ approaches μ_Γ (μ_L). This is straightforward because the overall mobility μ would be dominated by μ_Γ (μ_L) if the majority of electrons reside in the Γ-valley (L-valley).

At low temperatures, the Fermi-tail is suppressed, so electrons condense to the valley with a lower energy [12]. For indirect-bandgap Ge(Sn) alloys, such as Ge and $Ge_{0.955}Sn_{0.045}$, the energy of the L-valley is lower [18, 19, 35]. Therefore, as the tempera-

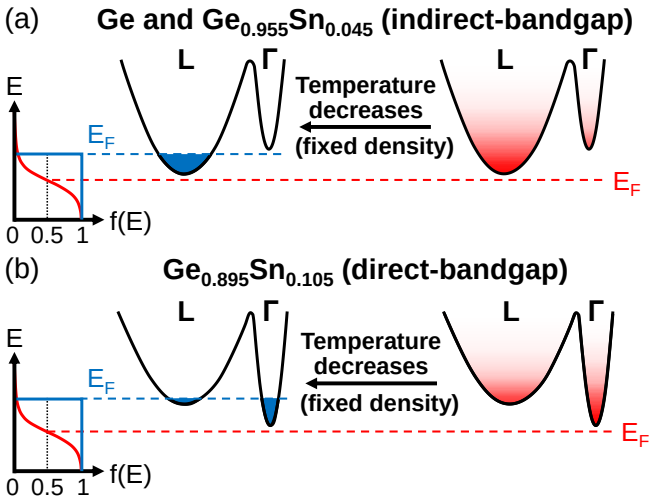

Fig. 3-18 The variation of electron population in the Γ- and L-valley with temperature in (a) indirect-bandgap and (b) direct-bandgap Ge(Sn) alloys under a fixed electron density [12].

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ture drops, electrons condense to the L-valley (Fig. 3-18 (a)). This results in a reduction in n_Γ/n_L under a fixed electron density [9], and thus the L-valley electrons dominate the overall transport, i.e., μ approaches μ_L (Equation (3-9)). Due to the much larger effective mass in the L-valley ($\mu_L \ll \mu_\Gamma$) [17, 19], the overall mobility μ is expected to decrease as the temperature decreases. This agrees with the monotonic reduction in effective mobility observed in the Ge and $Ge_{0.955}Sn_{0.045}$ n-MOSFETs (Fig. 3-17).

On the other hand, for direct-bandgap Ge(Sn) alloys, such as $Ge_{0.895}Sn_{0.105}$, the Γ-valley is lower in energy [18, 19, 35]. Under a fixed electron density, the n_Γ/n_L ratio increases as the temperature decreases (Fig. 3-18 (b)) [9]. Therefore, the Γ-valley electrons dominate the overall transport, i.e., μ approaches μ_Γ (Equation (3-9)). Since the effective mass in the Γ-valley is much smaller ($\mu_\Gamma \gg \mu_L$) [17, 19], an enhancement in overall mobility μ with decreasing temperature is expected. This explains the anomalous mobility upturn observed in the $Ge_{0.895}Sn_{0.105}$ n-MOSFET (Fig. 3-17). At temperatures below 20 K, the mobility of the $Ge_{0.895}Sn_{0.105}$ device even surpasses those of the Ge and $Ge_{0.955}Sn_{0.045}$ devices, despite being subjected to the strongest Coulomb scattering [21, 55] and alloy scattering [78] across all devices.

A calculated result from prior work [9] corroborates the arguments above. As the temperature decreases, n_Γ/n_L of the strain-relaxed n-$Ge_{0.92}Sn_{0.08}$ film decreases, while that of the strain-relaxed n-$Ge_{0.88}Sn_{0.12}$ film increases (Fig. 3-19). This indicates that at some Sn fractions between 8 at% and 12 at%, the n-GeSn film would exhibit a marginal transition in the trend of n_Γ/n_L vs. temperature from decreasing to increasing, which agrees with the observed transition in the trend of mobility vs. temperature in the Ge(Sn) n-MOSFETs as the Sn fraction increases from 4.5 at% to 10.5 at% (Fig. 3-17). Combining with the fact that the mobility of the $Ge_{0.895}Sn_{0.105}$ device remains relatively constant with temperature, a Sn fraction of 10.5 at% can be treated as a threshold of transition from an

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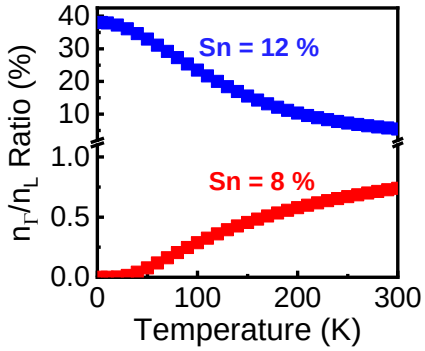

Fig. 3-19 Calculated electron population ratio in the Γ-valley relative to that in the L-valley (n_Γ/n_L) of the strain-relaxed n-$Ge_{0.92}Sn_{0.08}$ and n-$Ge_{0.88}Sn_{0.12}$ films [9].

indirect to direct bandgap GeSn. In addition, the increase in n_Γ/n_L occurs predominantly at temperatures below 200 K (Fig. 3-19), suggesting that the mobility enhancement with decreasing temperature starts around 200 K. Such a "transition point" is also observed in the $Ge_{0.895}Sn_{0.105}$ device around 100 K, where the anomalous mobility upturn with decreasing temperature begins (Fig. 3-17).

In the intermediate-density regime (N_{inv} = 1 x 10^{12} cm^{-2}), the μ_{eff}-T curves of the Ge(Sn) n-MOSFETs (Fig. 3-20 (a)) are similar to those in the low-density regime (Fig. 3-17). As the Sn fraction increases from 0 at% to 10.5 at%, a transition from a monotonic trend of effective mobility over temperature to that with an anomalous mobility upturn

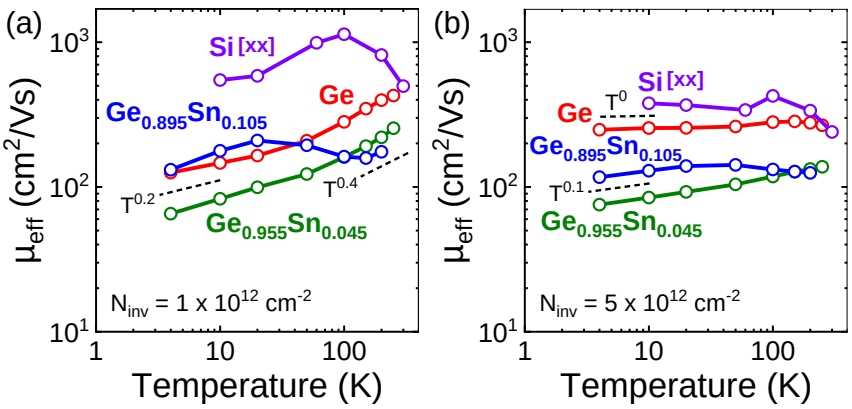

Fig. 3-20 μ_{eff} vs. temperature of the Si [31] and Ge(Sn) n-MOSFETs (extracted from Fig. 3-16) in the (a) intermediate-density (N_{inv} = 1 x 10^{12} cm^{-2}) and (b) high-density regimes (N_{inv} = 5 x 10^{12} cm^{-2}).

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between 150 K and 20 K is also observed. This is attributed to the dual-valley electron transport, where a mobility enhancement arises due to the indirect- to direct-bandgap transition of Ge(Sn) by increasing the Sn fraction (Fig. 3-18). The only difference is the weaker temperature dependence ($T^{0.2} \sim T^{0.4}$) compared to that in the low-density regime ($T^{0.3} \sim T^{0.7}$). This can be attributed to a stronger influence of alloy and surface roughness scattering at higher densities, where both of the scattering mechanisms are temperature-independent (Appendix B.1).

In the high-density regime (N_{inv} = 5 x 10^{12} cm^{-2}), the μ_{eff}-T curves of all the Ge(Sn) n-MOSFETs exhibit an even weaker temperature dependence ($T^{0} \sim T^{0.1}$) (Fig. 3-20 (b)) compared to those in the intermediate-density ($T^{0.2} \sim T^{0.4}$) (Fig. 3-20 (a)) and low-density regimes ($T^{0.3} \sim T^{0.7}$) (Fig. 3-17). This is attributed to an even stronger influence of alloy and surface roughness scattering at higher densities, where both of the scattering mechanisms are temperature-independent (Appendix B.1). Nevertheless, the effect of indirect-to direct-bandgap transition on electron transport remains readily observable. In particular, the μ_{eff}-T curve of the $Ge_{0.955}Sn_{0.045}$ n-MOSFET is below that of the Ge device owing to stronger alloy scattering [78]. However, the μ_{eff}-T curve of the $Ge_{0.895}Sn_{0.105}$ n-MOSFET becomes progressively higher than that of the $Ge_{0.955}Sn_{0.045}$ device as the temperature decreases, despite being subjected to a stronger alloy [78] and surface roughness scattering (Fig. 2-8). This is explained by the dual-valley electron transport, where a mobility enhancement with decreasing temperature occurs exclusively in the $Ge_{0.895}Sn_{0.105}$ n-MOSFET due to an increased electron population in the Γ-valley (Fig. 3-18 (b)). These findings indicate that an indirect-to-direct bandgap transition in Ge(Sn) occurs between a Sn fraction of 4.5 at% and 10.5 at%, which agrees with theoretical predictions [18, 19, 35].

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3.4 Summary

In summary, transfer I-V and split C-V characteristics of the Ge, $Ge_{0.955}Sn_{0.045}$ and $Ge_{0.895}Sn_{0.105}$ n-MOSFETs were investigated from 300 K to 4 K. As the temperature decreases, drastic reduction in I_{OFF} were observed across all devices. This is attributed to a diminished junction leakage and gate-induced drain leakage (GIDL). The temperature dependence of I_{ON}, however, was quite complex across all devices. Before investigating the underlying cause, the combined effects of inversion carrier density (N_{inv}) and effective mobility (μ_{eff}) on I_{ON} were decoupled using the split C-V method. As the temperature decreases, reduction in C_{GC} were observed in the accumulation and depletion regimes, which is attributed to a diminished supply of majority carriers through the junctions in response to the AC signal. In the strong inversion regime, the temperature-dependence of C_{GC} is attributed to the temperature-dependent supply of minority carriers by both the channel and the junctions in response to the AC signal. These were validated using physically based small-signal circuit models derived from the temperature-dependent AC carrier transport mechanisms. Finally, effective mobility in the Ge(Sn) n-MOSFETs were investigated. For the Ge and $Ge_{0.955}Sn_{0.045}$ n-MOSFETs, a monotonic decrease in μ_{eff} with decreasing temperature is observed due to enhanced Coulomb scattering. As the Sn fraction increases up to 10.5 at%, the μ_{eff}-T trend transitions from a monotonic decrease to one with an anomalous mobility upturn (enhancement) even being subjected to stronger Coulomb, alloy, and surface roughness scattering. This can be explained by an increased electron population in the Γ-valley, where the effective mass is much smaller than in the L-valley, strongly suggesting that $Ge_{0.895}Sn_{0.105}$ is a direct-bandgap material and that an indirect-to-direct bandgap transition occurs between Sn fractions of 4.5 at% and 10.5 at%.

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Chapter 4 Conclusion and Future Work

4.1 Conclusion

In this thesis, the transport properties in GeSn n-MOSFETs with Sn fractions up to 10.5 at% were investigated from 300 K to 4 K. In Chapter 2, room-temperature device characteristics were investigated and explained using equivalent small-signal circuit models. Strain-relaxed Ge, $Ge_{0.955}Sn_{0.045}$, and $Ge_{0.895}Sn_{0.105}$ epitaxial structures were grown using RPCVD, where the exact strain and Sn fractions were extracted from the RSM results. The high-quality of the GeSn epitaxy was confirmed through TEM, EDXS, and AFM analysis. To rule out the effect of threshold voltage variation on the extraction of effective mobility, all measurements were conducted with a standardized procedure implemented by a customized MATLAB® program, which performs calibration V_G sweeps and maintains identical V_G step timing throughout the measurement. The off-state current (I_{OFF}) of the Ge(Sn) n-MOSFETs increased with the Sn fraction, which is attributed to the enhanced junction leakage. By contrast, the on-state current (I_{ON}) of the Ge(Sn) n-MOSFETs decreased with the Sn fraction, which is attributed to the enhanced alloy scattering. In both the accumulation (V_{OV} = –2 V) and depletion regimes (V_{OV} = –0.5 V), abnormally high gate-to-channel capacitance (C_{GC}) was observed across all devices, which is attributed to the large supply of majority carrier through the junctions in response to the AC signal. In the strong inversion regime (V_{OV} = 2 V), a slight Sn-fraction dependence of gate-to-channel capacitance (C_{GC}) was observed, which is attributed to the Sn-fraction dependent supply of minority carriers by both the channel and junctions in response to the AC signal. These were validated using physically based small-signal circuit models. A method is proposed for future calibration of the off-state leakage effect on C_{GC}, and consequently, mobility extraction, which can be applied to small-bandgap, high-mobility transistors such as GeSn, InAs, and InSb n-MOSFETs. Finally, a reduction in effec-

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tive mobility is observed with an increasing Sn fraction, which is attributed to enhanced alloy scattering.

In Chapter 3, cryogenic device characteristics and electron transport properties were investigated. A monotonic reduction in off-state current (I_{OFF}) with a decreasing temperature was observed across all Ge(Sn) n-MOSFETs, which is attributed to suppressed junction leakages. The on-state current (I_{ON}), however, exhibited a complex trend with the temperature. To facilitate analysis, its dependence on both electron density and mobility was decoupled using the split C-V method. The abnormally high gate-to-channel capacitance (C_{GC}) in both the accumulation (V_{OV} = –2 V) and depletion regimes (V_{OV} = –0.5 V) observed at room-temperature was effectively suppressed at low temperatures thanks to the diminished supply of majority carriers through the junctions in response to the AC signal. In the strong inversion regime (V_{OV} = 2 V), the temperature-dependence of gate-to-channel capacitance (C_{GC}) was observed, which is attributed to the temperature-dependent supply of minority carriers by both the channel and junctions in response to the AC signal. These were also validated using the physically based small-signal circuit models. Finally, the effective mobility (μ_{eff}) in the Ge(Sn) n-MOSFETs was investigated. A monotonic decrease in μ_{eff} with decreasing temperature is observed in the Ge and $Ge_{0.955}Sn_{0.045}$ n-MOSFETs due to enhanced Coulomb scattering. As the Sn fraction increases up to 10.5 at%, a transition in the μ_{eff}-T trend is observed from a monotonic decrease to one with an anomalous mobility upturn (enhancement) even under a stronger Coulomb, alloy, and surface roughness scattering. This is attributed to an increased electron population in the Γ-valley, where the effective mass is much smaller than in the L-valley. The results suggest that $Ge_{0.895}Sn_{0.105}$ is a direct-bandgap material and an indirect-to-direct bandgap transition between Sn fractions of 4.5 at% and 10.5 at%.

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4.2 Future Work

There are five main directions that could be further explored in the future:

1. Electron transport in Ge(Sn) n-MOSFETs under different strain conditions:

By varying the strain applied to the Ge(Sn) active layer while keeping the Sn fraction constant, the "directness" of Ge(Sn) can be modulated without altering the intensity of alloy scattering [11]. This approach eliminates one interfering factor and enables a clearer observation of the indirect-to-direct bandgap transition in GeSn alloys.

2. Electron transport in Ge(Sn) gated Hall-bar by Hall measurements:

By extracting Hall mobility and Hall carrier density through Hall measurements, the effect of immobile charges (e.g., interface trap charges) on the extracted mobility can be excluded [90, 91]. This approach minimizes the influence of the typically poor oxide/Ge(Sn) quality and enables a more reliable investigation into the nature of the indirect-to-direct bandgap transition in GeSn alloys.

3. Magnetotransport: effective mass extraction:

In previous methods, the observation of the indirect-to-direct bandgap transition in Ge(Sn) relies on carrier mobility, which is complicated by various scattering mechanisms. This issue can be addressed by extracting the effective masses of Ge(Sn) from temperature-dependent Shubnikov-de Haas (SdH) oscillations [92] and compare them to theoretical predictions [3]. Due to the large difference between the electron effective masses in the L-valley and the Γ-valley [3], the indirect or direct bandgap nature of GeSn alloys should be readily identified.

4. Electron transport in Ge(Sn) n-MOSFETs under different channel directions:

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For indirect-bandgap Ge(Sn) n-MOSFETs, the electron mobility could depend on channel direction. When fabricated using (110) substrates, the direction-dependence of electron mobility could become more prominent due to a lower symmetry (2-fold) in valley configuration compared to (100) substrates (4-fold) [51]. Because the constant energy surface centered at the Γ-point is isotropic, the direction-dependence of electron mobility is contributed by electrons in the L-valley and/or the Δ-valley. Therefore, if a transition from an indirect to direct bandgap occurs, the direction-dependence of electron mobility should weaken or vanish because electrons in the isotropic Γ-valley becomes more dominant. This offers a new way to probe the indirect-to-direct bandgap transition in GeSn alloys.

5. Calibration of high off-state leakage effect on C_{GC} and mobility extraction:

Both C_{GC} and the extracted effective mobility are severely affected by the transistor off-state leakage, especially for high-Sn GeSn n-MOSFETs (Chapter 2.3). A method to eliminate the effect of off-state leakage is proposed, but requires data at frequencies higher than 200 kHz (Chapter 2.3.3). Therefore, by obtaining C_{GC} and G_{gsd} under a wider frequency spectrum (say, from 1 kHz to 1 MHz) using the split C-V and split G-V measurement, the off-state leakage effect on C_{GC} can be calibrated, enabling accurate mobility extraction from low-bandgap, high-mobility transistors such as GeSn, InAs, and InSb n-MOSFETs suffering from severe junction leakage.

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Appendix A Derivation of the Circuit Capacitance of Small-Signal Models

A.1 Accumulation Regime (V_{OV} = –2 V)

During the split C-V measurement, the AC signal applied to the Ge(Sn) n-MOSFETs are small relative to the DC bias, and thus the non-linear carrier storage properties and carrier transport properties in the Ge(Sn) n-MOSFETs (Fig. 2-25) can be approximated using linearized circuit elements, i.e., small-signal models [93]. On one hand, in the accumulation regime (V_{OV} = –2 V), the storage of carriers at the surface are modeled by the distributed gate oxide capacitance $c_{ox}WdL$ and the distributed accumulation capacitance c_AWdL, while the storage of carriers at the source-to-substrate and drain-to-substrate junctions are modeled by the junction capacitance C_j and the diffusion capacitance C_d (Fig. A-1 (a)). Besides, the storage of carriers at the gate-to-source and

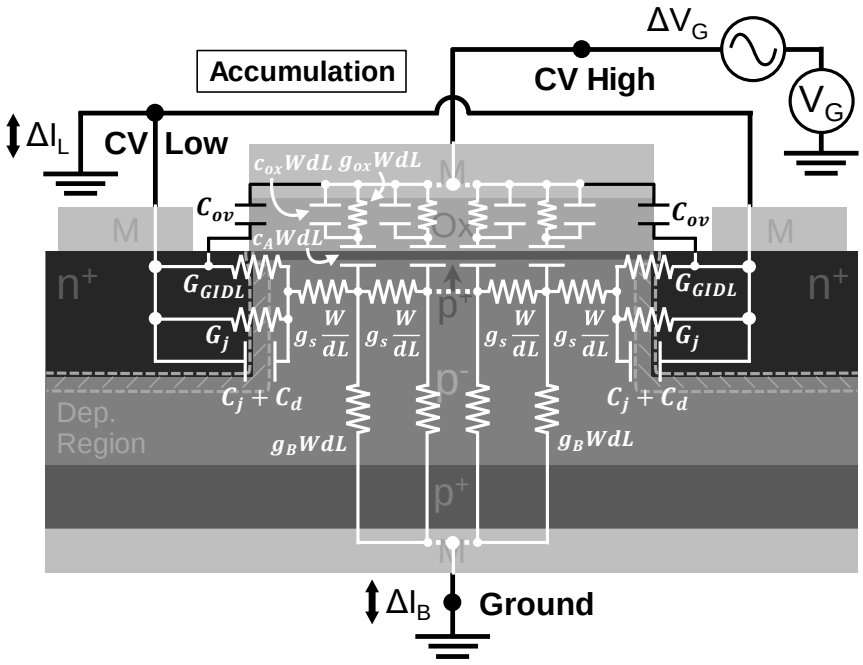

Fig. A-1 The distributed small-signal circuit model of the Ge(Sn) n-MOSFETs biased in the accumulation regime (V_{OV} = –2 V) during split C-V measurement.

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gate-to-drain overlaps are modeled by the overlap capacitance C_{ov}. Note that the effects of interface traps are omitted for simplicity. On the other hand, the vertical transport of carriers across the bulk, the horizontal transport of carriers across the bulk near the surface, the transport of carriers across the source-to-substrate and drain-to-substrate n^+/p junctions, the tunneling of carriers at the gate-to-source and gate-to-drain overlaps, and the leakage through the oxide layer are modeled by the distributed differential bulk conductance g_BWdL, the distributed differential series conductance g_sW/L, the differential junction conductance G_j, the differential GIDL conductance G_{GIDL}, and the distributed differential oxide conductance g_{ox}WdL, respectively (Fig. A-1).

To facilitate analysis, a lumped circuit approximation [72] has been made, where the distributed capacitance (c_{ox}WdL and c_AWdL) and the distributed differential conductance (g_BWdL, g_sW/L, and g_{ox}WdL) are integrated along the channel direction (L) to transform into lumped capacitance (C_{ox} and C_A) and lumped differential conductance (G_B, $2G_s$, and G_{ox}), respectively (Fig. A-2). Note that a factor of two is introduced to $2G_s$ to make sure

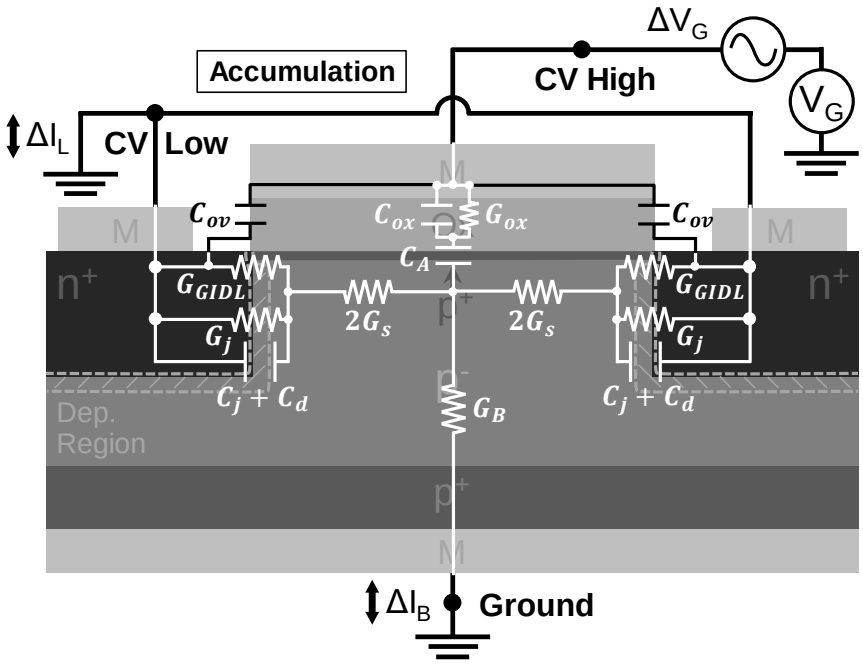

Fig. A-2 The lumped small-signal circuit model derived from Fig. A-1.

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that the total series conductance along the channel is G_s. Due to symmetry, the lumped circuit model is "folded" with respect to the central symmetric axis of the devices, thereby doubling C_j, C_d, C_{ov}, G_j, G_{GIDL}, and $2G_s$ since they are all in parallel with their respective counterparts (Fig. A-3 (a)).

To extract the most important feature from the circuit model, further simplifications are made (Fig. A-3 (b)). Firstly, G_{ox} is omitted since the gate current does not change with gate bias (Fig. 2-13 (a)), i.e., $G_{ox} \sim 0$ S, rendering the oxide layer completely capacitive. Then, $2C_j + 2C_d$ are omitted since G_j is much larger than both the junction susceptance B_j and the diffusion susceptance B_d. Specifically, the ratio G_j/B_j is expressed as [94]

$$\frac{G_j}{B_j} = \frac{G_j}{2\pi f C_j} = \frac{G_j}{\pi f A}\sqrt{\frac{\psi_{bi}}{2q\epsilon_s N_A}}, \tag{A-1}$$

where the lower bound of G_j is approximately 20 μS since $I_{OFF} \sim 0.2$ μA at $V_D = 10$ mV (Fig. 2-17 (a)). Using the parameters in [3, 5, 11, 95] and junction area A ~ 210 μm x 55 μm, it can be obtained from Equation (A-1) that as long as f is much smaller than 1 MHz, G_j/B_j will be much larger than unity. In addition, the ratio G_j/B_d is expressed as [94]

$$\frac{G_j}{B_d} = \frac{g_j}{2\pi f C_d} \approx \frac{1}{\pi f \tau_n}, \tag{A-2}$$

where the lower bound of the minority carrier lifetime τ_n is 90 ns (Ge) [64]. As long as f

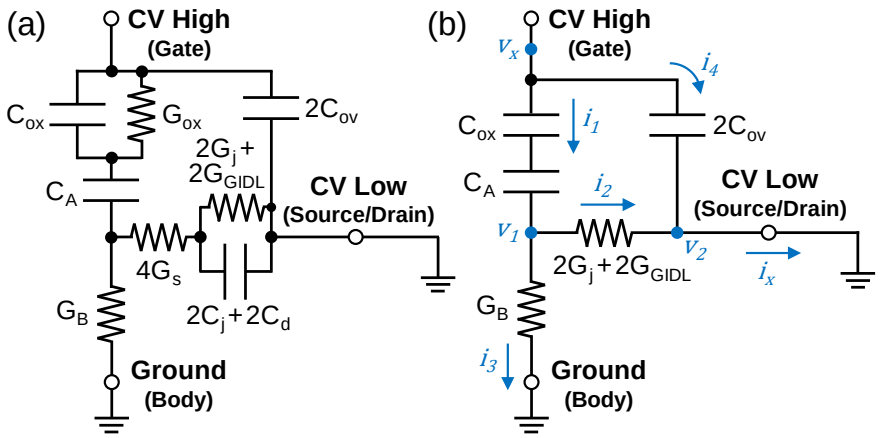

Fig. A-3 The (a) complete and (b) simplified equivalent small-signal circuit model derived from Fig. A-2.

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is much smaller than 4 MHz, G_j/B_d will be much larger than unity. These imply that if the measurement frequency is much smaller than 1 MHz, which is the case in this study (20 – 200 kHz), the electrical behavior of the junctions will be predominantly conductive rather than capacitive. Lastly, $4G_s$ is omitted since G_j is expected to be much smaller than G_s. This is because the transport across the junctions are determined by the transport of minority carriers [30, 66], while the transport across the bulk is determined by the majority carriers. Given that the minority carrier lifetime is significantly longer (~10^6 times) than the majority carrier lifetime (dielectric relaxation time) [58, 66], the rate of carrier transport across the junctions in series with bulk is expected to be limited by that across the junction. As a result, the total conductance ($4G_s \parallel 2G_j$) is expected to be limited by the junction conductance $2G_j$.

The frequency response of the circuit's capacitance is obtained as follows. By performing Nodal Analysis [69] at node v_1 (Fig. A-3 (b)), the relation

$$i_1 = i_2 + i_3 \tag{A-3}$$

is obtained, where i_1, i_2, and i_3 are expressed as

$$i_1 = s(C_{ox} \parallel C_A)(v_x - v_1)\,, \tag{A-4}$$

$$i_2 = \left(2G_j + 2G_{GIDL}\right)v_1\,, \tag{A-5}$$

and

$$i_3 = G_B v_1\,, \tag{A-6}$$

respectively. The parallel operator $\parallel$ is defined as

$$A \parallel B = \frac{AB}{A+B}\,. \tag{A-7}$$

By plugging Equations (A-5) to (A-7) into Equation (A-3) and rearranging the terms, the relation between v_1 and v_x can be obtained as

$$v_1 = \frac{s(C_{ox} \parallel C_A)}{G_B + 2G_j + 2G_{GIDL} + s(C_{ox} \parallel C_A)} v_x\,. \tag{A-8}$$

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Next, by performing Nodal Analysis [69] at node v_2 (Fig. A-3 (b)), the relation

$$i_x = i_2 + i_4 \tag{A-9}$$

is obtained, where i_2 is given by Equation (A-5), and i_4 is expressed as

$$i_4 = 2sC_{ov}v_x\,. \tag{A-10}$$

By plugging Equation (A-8) into Equation (A-5), i_2 can be expressed as a function of v_x. Finally, by plugging i_2 (as a function of v_x) and Equation (A-10) into Equation (A-9), the relation between i_x and v_x can be obtained as

$$i_x = \frac{s(C_{ox} \parallel C_A)\left(2G_j + 2G_{GIDL}\right)}{G_B + 2G_j + 2G_{GIDL} + s(C_{ox} \parallel C_A)}v_x + 2sC_{ov}v_x\,. \tag{A-11}$$

By replacing s with jω in Equation (A-11), the circuit capacitance C is derived as

$$C = \frac{1}{\omega}\mathrm{Im}\left(\frac{i_x}{v_x}\right) = C_0 \cdot \frac{1}{1 + (\omega/\omega_c)^2} + 2C_{ov}\,, \tag{A-12}$$

where

$$C_0 = \frac{C_{ox} \parallel C_A}{1 + \dfrac{G_B}{2G_j + 2G_{GIDL}}} \tag{A-13}$$

and

$$\omega_c = \frac{G_B + 2G_j + 2G_{GIDL}}{C_{ox} \parallel C_A}\,. \tag{A-14}$$

On the other hand, the circuit conductance G is derived as

$$G = \mathrm{Re}\left(\frac{i_x}{v_x}\right) = G_0 \cdot \frac{1}{1 + (\omega_c/\omega)^2}\,, \tag{A-15}$$

where

$$G_0 = 2G_j + 2G_{GIDL} \tag{A-16}$$

and

$$\omega_c = \frac{G_B + 2G_j + 2G_{GIDL}}{C_{ox} \parallel C_A}\,. \tag{A-17}$$

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A.2 Depletion Regime (V_{OV} ~ –0.5 V)

Similarly, the distributed small signal circuit model of the Ge(Sn) n-MOSFETs biased in the depletion regime (V_{OV} ~ –0.5 V) is derived by approximating the non-linear carrier storage and transport properties (Fig. 2-28) using linearized circuit elements (Fig. A-4). The assumptions and circuit element symbols are identical to those in the accumulation regime (Appendix A.1 and Fig. A-1), except that c_AWdL is replaced with the distributed depletion capacitance c_{ox}WdL, and G_{GIDL} is removed since GIDL is absent in the depletion regime. To facilitate analysis, a lumped circuit approximation [72] similar to those in the accumulation regime (Fig. A-2) has also been made (Fig. A-5). Due to symmetry, the lumped circuit model is also "folded" with respect to the central symmetric axis of the devices, thereby doubling C_j, C_d, C_{ov}, G_j, and $2G_s$ since they are all in parallel with their respective counterparts (Fig. A-6 (a)). To extract the most important feature from the circuit model, further simplifications are also made (Fig. A-6 (b)): G_{ox}, $2C_j$ +

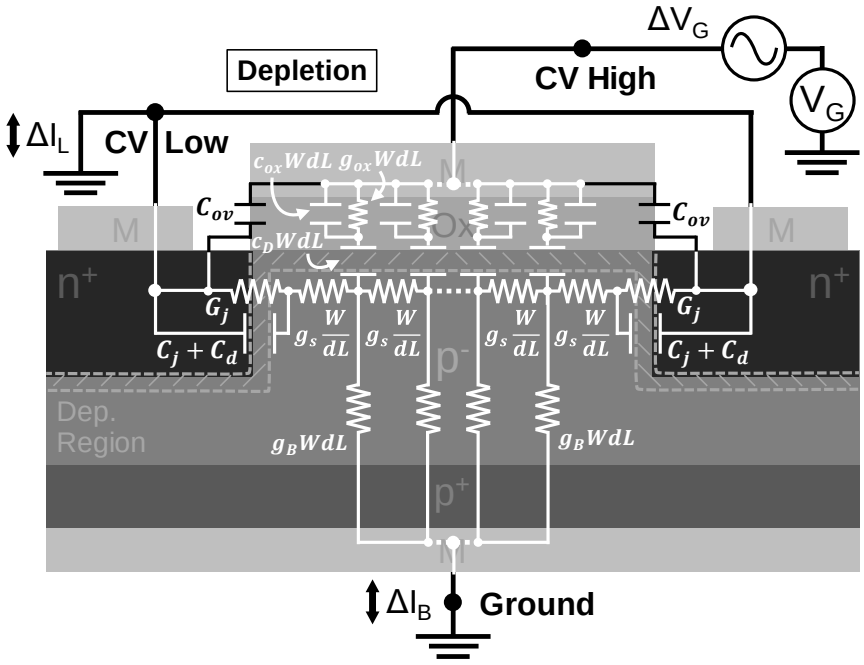

Fig. A-4 The distributed small-signal circuit model of the Ge(Sn) n-MOSFETs biased in the depletion regime (V_{OV} ~ –0.5 V) during split C-V measurement.

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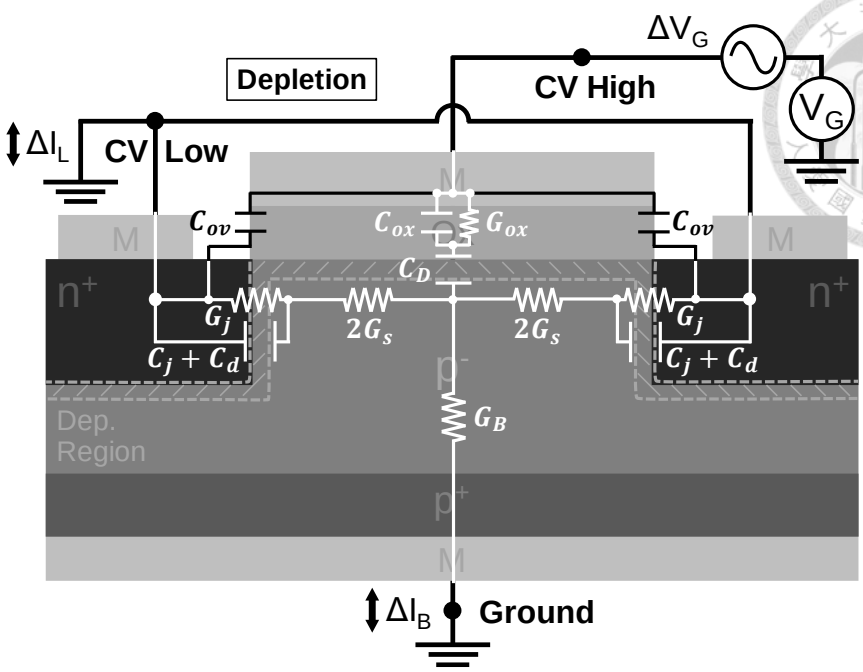

Fig. A-5 The lumped small-signal circuit model derived from Fig. A-4.

$2C_d$, and $4G_s$ are omitted for the same reasons as those stated in Appendix A.1.

The frequency response of the circuit's capacitance is obtained similarly to those stated in Appendix A.1, except that C_A is replaced with C_D and G_{GIDL} is omitted. The circuit capacitance C is derived as

$$C = \frac{1}{\omega}\mathrm{Im}\left(\frac{i_x}{v_x}\right) = C_0 \cdot \frac{1}{1+(\omega/\omega_c)^2} + 2C_{ov}\,, \tag{A-18}$$

where

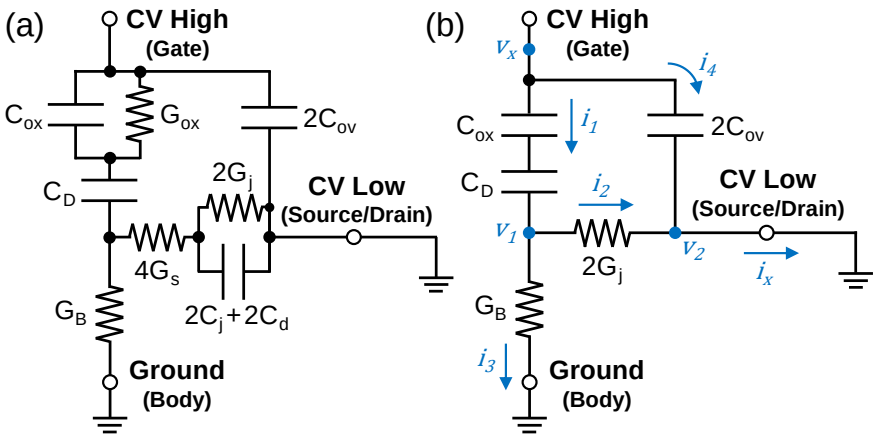

Fig. A-6 The (a) complete and (b) simplified equivalent small-signal circuit model derived from Fig. A-5.

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$$C_0 = \frac{C_{ox} \parallel C_D}{1 + \frac{G_B}{2G_j}} \tag{A-19}$$

and

$$\omega_c = \frac{G_B + 2G_j}{C_{ox} \parallel C_D}. \tag{A-20}$$

On the other hand, the circuit conductance G is derived as

$$G = \mathrm{Re}\left(\frac{i_x}{v_x}\right) = G_0 \cdot \frac{1}{1 + (\omega_c/\omega)^2}, \tag{A-21}$$

where

$$G_0 = 2G_j \tag{A-22}$$

and

$$\omega_c = \frac{G_B + 2G_j}{C_{ox} \parallel C_D}. \tag{A-23}$$

A.3 Strong Inversion Regime (V_{OV} = 2 V)

The distributed small signal circuit model of the Ge(Sn) n-MOSFETs biased in the strong inversion regime (V_{OV} = 2 V) is also derived by approximating the non-linear carrier storage properties and carrier transport properties (Fig. 2-31) using linearized circuit elements (Fig. A-7). The assumptions and circuit element symbols are identical to those in the depletion regime (Appendix A.2 and Fig. A-4), except that c_{ox}WdL is replaced with the distributed inversion capacitance c_IWdL, and additional distributed differential channel conductance g_{ch}W/dL as well as distributed differential surface GR conductance g_{gr}WdL are introduced. In addition, C_D is omitted since, in the strong inversion regime, the electric field from the gate is screened by the charges in the inversion layer, i.e., the charges at the edge of the surface depletion region no longer respond to the AC signal applied to the gate [25]. The distributed bulk trap capacitance c_TWdL associated with

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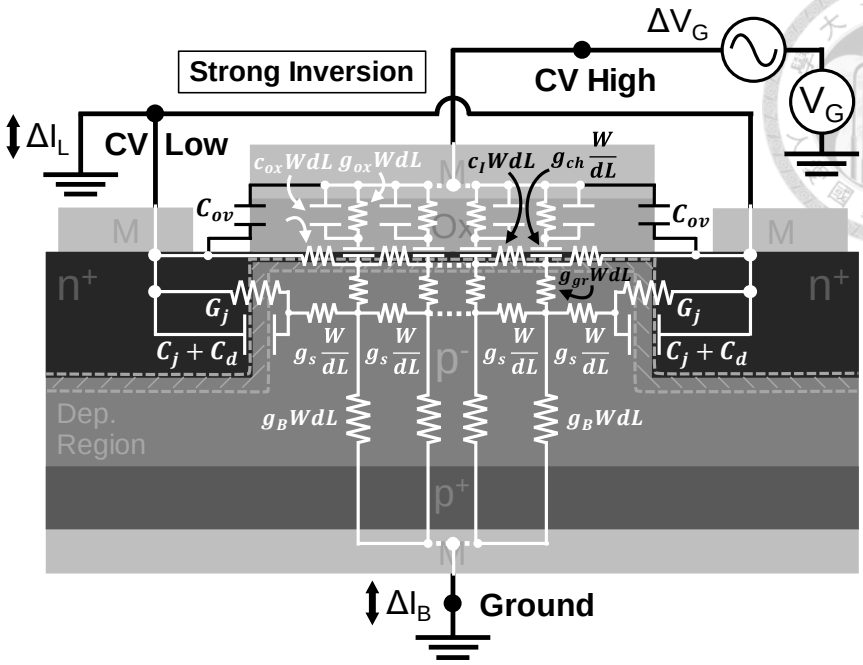

Fig. A-7 The distributed small-signal circuit model of the Ge(Sn) n-MOSFETs biased in the strong inversion regime (V_{OV} = 2 V) during split C-V measurement.

g_{gr}WdL is also omitted since c_TWdL is negligible compared to c_IWdL [58].

To facilitate analysis, a lumped circuit approximation [72] similar to those in the depletion regime (Fig. A-5) has also been made (Fig. A-8). Note that a factor of two is

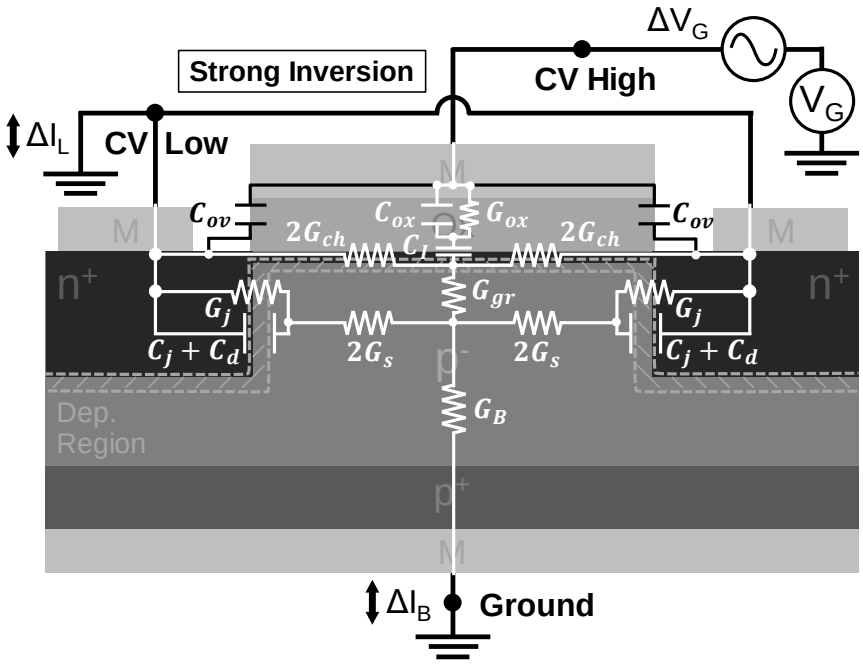

Fig. A-8 The lumped small-signal circuit model derived from Fig. A-7.

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introduced to $2G_{ch}$ to make sure that the total series conductance along the channel is G_{ch}. Due to symmetry, the lumped circuit model is also "folded" with respect to the central symmetric axis of the devices, thereby doubling C_j, C_d, $2C_{ov}$, G_j, $2G_s$, and $2G_{ch}$ since they are all in parallel with their respective counterparts (Fig. A-9 (a)). To extract the most important feature from the circuit model, further simplifications are also made (Fig. A-9 (b)): G_{ox}, $2C_j + 2C_d$, and $4G_s$ are omitted for the same reasons as those stated in Appendix A.1.

The frequency response of the circuit's capacitance is obtained as follows. By performing Nodal Analysis [69] at node v_2 (Fig. A-9 (b)), the relation

$$i_3 = i_4 + i_5 \tag{A-24}$$

is obtained, where i_3, i_4, and i_5 are expressed as

$$i_3 = G_{gr}(v_1 - v_2)\,, \tag{A-25}$$

$$i_4 = 2G_j v_2\,, \tag{A-26}$$

and

$$i_5 = G_B v_2\,, \tag{A-27}$$

respectively. Note that the parallel operator $\|$ is as defined in Equation (A-7). By plugging Equations (A-25) to (A-27) into Equation (A-24) and rearranging the terms, the re-

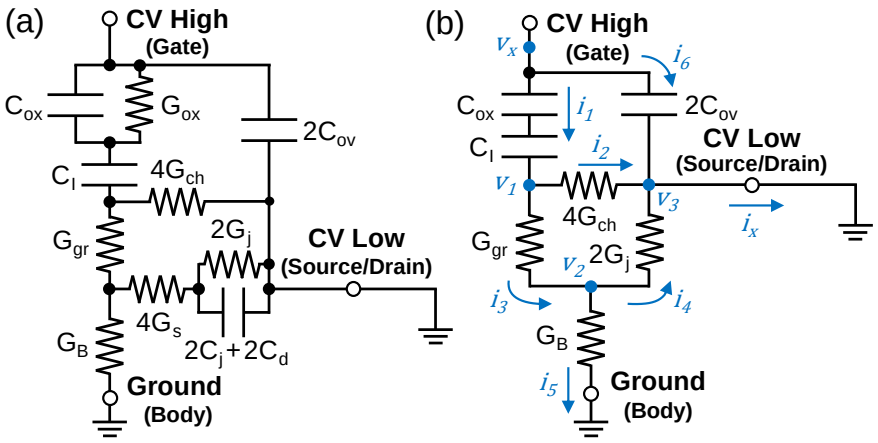

Fig. A-9 The (a) complete and (b) simplified equivalent small-signal circuit model derived from Fig. A-8.

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lation between v_1 and v_2 is obtained as

$$v_2 = \frac{G_{gr}}{G_B + 2G_j + G_{gr}} v_1 . \quad \text{(A-28)}$$

Next, by performing Nodal Analysis [69] at node v_1, the relation

$$i_1 = i_2 + i_3 \quad \text{(A-29)}$$

is obtained, where i_3 is given by Equation (A-25), and i_1 and i_2 are expressed as

$$i_1 = s(C_{ox} \parallel C_I)(v_x - v_1) \quad \text{(A-30)}$$

and

$$i_2 = 4G_{ch} v_1 , \quad \text{(A-31)}$$

respectively. By plugging Equation (A-28) into Equation (A-25), i_3 can be expressed as a function of v_1. Then, by plugging Equations (A-30) and (A-31) into Equation (A-29) and rearranging the terms, the relation between v_1 and v_x is obtained as

$$v_1 = \frac{[s(C_{ox} \parallel C_I) + 4G_{ch}](G_B + 2G_j + G_{gr}) + G_{gr}(G_B + 2G_j)}{s(C_{ox} \parallel C_I)(G_B + 2G_j + G_{gr})} v_x . \quad \text{(A-32)}$$

Finally, by performing Nodal Analysis [69] at node v_3 (Fig. A-3 (b)), the relation

$$i_x = i_2 + i_4 + i_6 \quad \text{(A-33)}$$

is obtained, where i_2, i_4 are given by Equations (A-31) and (A-26), respectively, and i_6 is expressed as

$$i_6 = 2sC_{ov} v_x . \quad \text{(A-34)}$$

By plugging Equations (A-28) and (A-32) into Equation (A-26), i_4 can be expressed as a function of v_x. By plugging Equation (A-32) into Equation (A-31), i_2 can also be expressed as a function of v_x. Finally, by plugging i_2, i_4 (both as a function of v_x), and Equation (A-34) into Equation (A-33), the relation between i_x and v_x can be obtained as

$$i_x = \frac{s(C_{ox} \parallel C_I)[4G_{ch}(G_B + 2G_j + G_{gr}) + 2G_j G_{gr}]}{[s(C_{ox} \parallel C_I) + 4G_{ch}](G_B + 2G_j + G_{gr}) + G_{gr}(G_B + 2G_j)} v_x . \quad \text{(A-35)}$$

By replacing s with jω in Equation (A-35), the circuit capacitance C is derived as

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$$C = \frac{1}{\omega}\mathrm{Im}\left(\frac{i_x}{v_x}\right) = C_0 \cdot \frac{1}{1+(\omega/\omega_c)^2} + 2C_{ov}\,, \tag{A-36}$$

where

$$C_0 = \frac{C_{ox} \parallel C_I}{1+\dfrac{\alpha G_B}{4G_{ch}+2\alpha G_j}} \tag{A-37}$$

and

$$\omega_c = \frac{4G_{ch}+\alpha\left(G_B+2G_j\right)}{C_{ox} \parallel C_I} \tag{A-38}$$

using the definition

$$\alpha = \left[1+\left(G_B+2G_j\right)/G_{gr}\right]^{-1}. \tag{A-39}$$

On the other hand, the circuit conductance G is derived as

$$G = \mathrm{Re}\left(\frac{i_x}{v_x}\right) = G_0 \cdot \frac{1}{1+(\omega_c/\omega)^2}\,, \tag{A-40}$$

where

$$G_0 = 4G_{ch}+2\alpha G_j \tag{A-41}$$

and

$$\omega_c = \frac{4G_{ch}+\alpha\left(G_B+2G_j\right)}{C_{ox} \parallel C_I}. \tag{A-42}$$

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Appendix B Scattering Mechanisms in n-MOSFETs

B.1 Overview

Due to various perturbation to the periodic crystal potentials, the electron transport properties are not only dependent on the electronic band structures but electron scattering processes. In particular, the electron mobility μ is expressed as [96]

$$\mu = \frac{e}{m^*}\langle \tau_{tr} \rangle = \frac{e}{m^*}\frac{\int \tau_{tr}(E) E \frac{\partial f}{\partial E} dE}{\int E \frac{\partial f}{\partial E} dE}, \tag{B-1}$$

where the effective mass m^* and the energy-averaged transport lifetime $<\tau_{tr}>$ are determined by the curvature of band structures and scattering processes, respectively. According to Matthiessen's rule, the energy-dependent transport lifetime $\tau_{tr}(E)$ is the inverse of the sum of all inverse transport lifetime $1/\tau_{tr,n}(E)$ [97]:

$$\tau_{tr}(E) = \left[\sum\nolimits_n \frac{1}{\tau_{tr,n}(E)}\right]^{-1}, \tag{B-2}$$

where each $\tau_{tr,n}(E)$ corresponds to a type of electron scattering mechanism. To facilitate the understanding of electron transport in n-MOSFETs, the electron mobility μ is usually approximated as [98]

$$\mu = \left[\sum\nolimits_n \frac{1}{\mu_n}\right]^{-1}, \tag{B-3}$$

where μ_n corresponds to a type of electron scattering mechanism with transport lifetime $\tau_{tr,n}$, i.e.,

$$\mu_n = \frac{e}{m^*}\langle \tau_{tr,n} \rangle = \frac{e}{m^*}\frac{\int \tau_{tr,n}(E) E \frac{\partial f}{\partial E} dE}{\int E \frac{\partial f}{\partial E} dE}. \tag{B-4}$$

In this case, the summation is done after energy-averaging. Thus, μ can then be understood as being limited by various "branches" μ_n, with the lowest one corresponding to the

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Table B-1 The power of density (α) and temperature (γ) dependence of 2DEG mobility $\mu_{n,2D}$.

	surface roughness scattering	phonon scattering	alloy scattering	Coulomb scattering
α	–2 [74]	–0.3 [31]	–0.3 [89]	0.5 ~ 2 [31, 74, 75]
γ	0 [31]	–1 ~ –1.75 [74, 75]	–0.5* [9, 99] 0† (Appendix B.3.2)	–1 ~ 1 [31, 74]

* Bulk transport; † 2DEG transport (not yet reported)

dominant scattering mechanism (Fig. B-1).

In the Ge(Sn) n-MOSFETs, four types of scattering mechanisms are expected to be observed. The 2DEG mobility limited by each type of them is expressed as

$$\mu_{n,2D} \propto {N_{inv}}^{\alpha} T^{\gamma}, \tag{B-5}$$

where the power dependence of $\mu_{n,2D}$ on the inversion carrier density (α) and temperature (γ) are listed in Table B-1. A positive (negative) α indicates that the corresponding $\mu_{n,2D}$ increases (decreases) with density, making it the mobility-limiting "branch" of the overall mobility μ in the low-density (high-density) regime (Fig. B-1). Therefore, Coulomb scattering dominates in the low-density regime since it is the only scattering mechanism with a positive α [31, 74, 75]. Surface roughness scattering, which exhibits the most negative α, dominates in the high-density regime [74]. As for phonon and alloy scattering, they dominate in the intermediate-density regime because their α is negative but smaller in magnitude compared to that of surface roughness scattering [31, 89]. Analogously, at

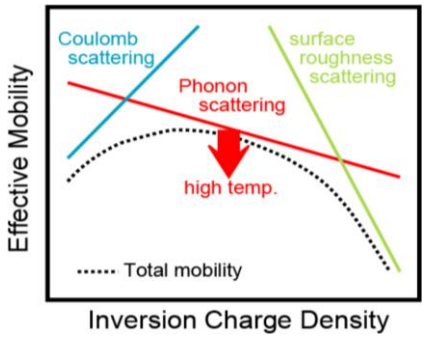

Fig. B-1 A schematic showing the relationships between the total mobility and different mobility branches corresponding to various scattering mechanisms [100].

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room temperature, either phonon or alloy scattering dominates since their γ is negative [9, 74, 75, 99]. However, at low temperatures, Coulomb scattering dominates since its γ is mostly positive, expect at the cryogenic limit [31, 74]. The intensity of surface roughness scattering remains constant with temperature (γ = 0), indicating that it could be observed at all temperatures [31]. Further details are stated below.

B.2 Surface Roughness Scattering

B.2.1 The Physical Mechanism

The change in the position of oxide/semiconductor interface (Δ) leads to a variation in the position of electron wavefunction in the inversion channel, and consequently, a change in the potential energy ($E_{eff}\Delta$) at the centroid of the wavefunction (Fig. B-2), assuming that the energy subbands and the shape of wavefunctions are independent of Δ (since Δ is small) [101]. According to Fermi's Golden Rule, potential energy variation gives rise to a perturbation to carrier transport [102]. Therefore, the surface roughness of an n-MOSFET is a source of electron scattering. The surface-roughness-limited mobility μ_{SR} is expressed as [101]

$$\mu_{SR} \propto {E_{eff}}^{-2}\Delta^{-2}T^{\gamma}, \tag{B-6}$$

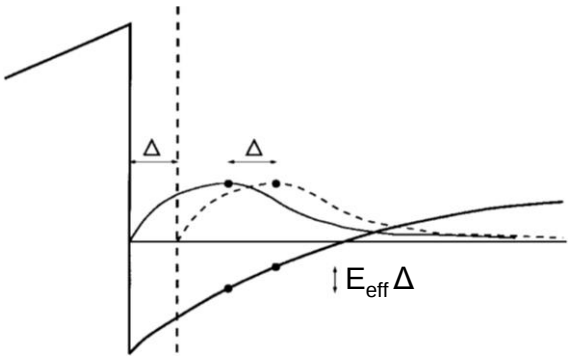

Fig. B-2 A schematic showing the effect of the change in surface position (Δ) on the electron wavefunction, where the potential energy at the centroid is varied by $E_{eff}\Delta$ [101].

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where the term $E_{eff}\Delta$ is raised to a power of two because scattering rate is proportional to the square of the perturbing potential energy [102]. As the surface becomes rougher (larger Δ) and the effective field (E_{eff}) becomes stronger, the change in potential energy at the centroid ($E_{eff}\Delta$) becomes larger (Fig. B-2). This leads to a more severe perturbation to electron transport and, consequently, a lower μ_{SR} (Equation (B-6)).

B.2.2 The Temperature Dependence

The temperature dependence (γ) of μ_{SR} remains inconclusive (Equation (B-6)). Some of the prior works suggest that μ_{SR} is independent of temperature ($\gamma = 0$) [31, 103] since the surface roughness does not change with temperature. However, other works suggests a sublinear ($\gamma = -1/3$) [104] and a linear ($\gamma = -1$) [101] temperature dependence, which is attributed to the variation of screening effect and Fermi-Dirac statistics (Equation (B-4)) with temperature [101].

B.2.3 The Density Dependence

The E_{eff}^{-2} dependence of μ_{SR} (Equation (B-6)) implies that surface roughness scattering is dominant at high field. According to the expression [101]

$$E_{eff} = \frac{qN_{dep} + qN_{inv}/2}{\epsilon_{semi}}, \tag{B-7}$$

it can be observed that E_{eff} is proportional to inversion carrier density N_{inv} in the high-field limit since the depletion carrier density N_{dep} no longer increases after strong inversion [30]. Therefore, μ_{SR} is also expected to exhibit an N_{inv}^{-2} dependence [74], i.e.,

$$\mu_{SR} \propto {N_{inv}}^{-2} T^{\alpha}, \tag{B-8}$$

in the high-field limit.

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B.3 Phonon and Alloy Scattering

B.3.1 The Physical Mechanism

The presence of atomic vibrations, or phonons, in semiconductors at finite temperatures induce time-varying crystal potential energy at the centroid of the electron wavefunction in the inversion channel [102]. Therefore, according to Fermi's Golden Rule, the atomic vibrations, or phonons, give rise to electron scattering since potential energy variation is a perturbation to carrier transport [102]. Similarly, the substitution of one type of atom into a periodic host of atoms of other types, such as that in the $Ge_{1-x}Sn_x$ alloys or III-V compound semiconductors, also induces a perturbing potential energy [78]. This is known as alloy or disorder scattering [99]. The mobility limited by phonon scattering (μ_{ph}) and alloy scattering (μ_{al}) takes on the same form [75, 76]

$$\mu \propto {E_{eff}}^{-0.3} T^{\gamma}, \tag{B-9}$$

where γ varies depending on the type of scattering mechanism involved.

B.3.2 The Temperature Dependence

According to Bose-Einstein distribution, the average energy of phonons decreases with temperature and becomes zero in the low-temperature limit [74]. This implies that the perturbating potential induced by phonons weakens as the temperature decreases. Therefore, γ is reported to be –1 ~ –1.75 [74, 75] for the mobility limited by phonon scattering (μ_{ph}) (Equation (B-9)).

On the other hand, the γ for alloy scattering in bulk semiconductors is reported to be –0.5 [9, 99], while the exponent γ for alloy scattering in n-MOSFETs (2DEG transport) has yet to be reported. When it comes to mobility calculation for alloy scattering, the energy dependence of transport lifetime is completely determined by the energy dependence of the density of states N(E) [105]

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$$\left[\tau_{tr,n}(E)\right]^{-1} \propto N(E), \tag{B-10}$$

where the 3D and 2D density of states are used for the bulk and 2DEG transport, respectively. Since the energy dependence of the 3D and 2D density of states is given by [94]

$$N_{3D}(E) \propto E^{1/2} \tag{B-11}$$

and

$$N_{2D}(E) \propto E^{0}, \tag{B-12}$$

respectively, by noting that the average energy of electrons is proportional to kT [94], the energy averaging process (Equation (B-4)) yields a $T^{-0.5}$ and T^{0} dependence for the mobility limited by alloy scattering (μ_{al}) in bulk semiconductor and n-MOSFETs, respectively. Such a 0.5 power difference between the bulk and 2DEG transport is also observed in the calculation of the mobility limited by phonon scattering [102].

B.3.3 The Density Dependence

In contrast to the surface roughness scattering, both phonon and alloy scattering are dominant in the intermediate-field regime since the E_{eff} dependence of μ_{ph} and μ_{al} (Equations (B-9)) is weaker than that of the μ_{SR} (Equation (B-6)). If the substrates of the n-MOSFETs were lightly-doped, such as the UID Ge(Sn) substrates used in this work (Chapter 2.2.1), N_{dep} would be much smaller than $N_{inv}/2$ since a substantial N_{inv} is expected in the intermediate-field regime (Equation (B-7)). Therefore, both μ_{ph} and μ_{al} are also expected to exhibit an $N_{inv}^{-0.3}$ dependence [31, 89], i.e.,

$$\mu \propto {N_{inv}}^{-0.3} T^{\gamma}, \tag{B-13}$$

in the intermediate-field regime.

B.4 Coulomb Scattering

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B.4.1 The Physical Mechanism

The presence of charged impurities induce a potential energy variation at the centroid of the electron wavefunction in the inversion channel [102]. According to Fermi's Golden Rule, potential energy variation give rise to a perturbation to carrier transport [102]. Therefore, charged impurities are sources of electron scattering. The Coulomb-limiting mobility μ_C is expressed as

$$\mu_C \propto {N_{inv}}^{\alpha} T^{\gamma}, \tag{B-14}$$

where α is reported to be 0.5 ~ 2 [31, 74, 75], and γ is reported to be –1 ~ 1 [31, 74]. The variation in both α and γ is a result of a competition between the intensity of Coulomb scattering and the strength of screening effect [31, 74].

B.4.2 The Temperature Dependence

Due to the anisotropy (dependent on **q**) of the Coulomb perturbing potential, the Coulomb scattering rate $W_{\mathbf{k}}(\mathbf{q})$ derived from Fermi's Golden Rule merely gives the single-particle lifetime $\tau_{i,n}$ [102]

$$\left[\tau_{i,n}(\boldsymbol{k})\right]^{-1} \propto \int W_{\boldsymbol{k}}(\boldsymbol{q}) d\boldsymbol{q}, \tag{B-15}$$

which differs from the transport lifetime $\tau_{tr,n}$ [102]

$$\left[\tau_{tr,n}(\boldsymbol{k})\right]^{-1} \propto \int W_{\boldsymbol{k}}(\boldsymbol{q}) w(|\boldsymbol{k}|, |\boldsymbol{q}|) d\boldsymbol{q} \tag{B-16}$$

by an angular weighting factor [102]

$$w(|\boldsymbol{k}|, |\boldsymbol{q}|) = 1 - \cos\theta = \frac{|\boldsymbol{q}|^2}{2|\boldsymbol{k}|^2}, \tag{B-17}$$

where the electron wavevectors before and after scattering are denoted as **k** and **k'** = **k** + **q**, respectively (Fig. B-3). Note that the angular weighting has little effect on acoustic phonon or alloy scattering since their perturbing potentials are nearly isotropic

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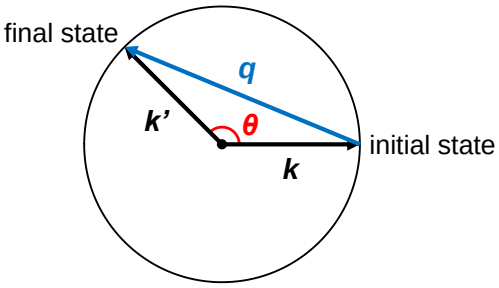

Fig. B-3 A schematic showing the geometrical relationships between the wavevector before scattering (**k**) and after scattering (**k'** = **k** + **q**). The magnitude of **k** and **k'** are identical since Coulomb scattering is an elastic (energy-conserving) scattering process [102].

(independent of **q**) [102, 105].

The purpose of w(|**k**|, |**q**|) (Equation (B-17)) is to account for the "efficacy" of Coulomb scattering since large-angle (large-θ) scattering has a larger impact on current conduction (Fig. B-3), and consequently, electron mobility [102]. Given that μ_C is proportional to the energy-averaged $\tau_{tr,n}$ (Equation (B-4)) and $\tau_{tr,n}$ is inversely correlated to the scattering angle θ (Equations (B-16) and (B-17)), a large θ at the average energy is indicative of a stronger scattering (smaller $\tau_{tr,n}$), and consequently, a lower μ_C. As temperature decreases, due to a suppressed Fermi tail, both the average energy E(**k**) and average wavevector |**k**| of the electron decreases, which leads to an increase in θ at the average wavevector |**k**| (Equation (B-17)) and, consequently, a reduction in μ_C. Therefore, μ_C exhibits a positive temperature dependence (positive γ) (Equation (B-14)) since electrons become increasingly more susceptible to Coulomb scattering at lower temperatures due to a loss of kinetic energy.

The weaker (less positive γ) and the negative temperature dependence (negative γ) (Equation (B-14)) of μ_C is explained by the screening effect. For Coulomb scattering, $W_{\mathbf{k}}(\mathbf{q})$ is expressed as [102]

$$W_{\boldsymbol{k}}(\boldsymbol{q}) \propto |V(|\boldsymbol{q}|)|^2 \delta\big(\varepsilon(\boldsymbol{k}+\boldsymbol{q}) - \varepsilon(\boldsymbol{k})\big), \tag{B-18}$$

where the δ-function is the density of state, and V(|**q**|) is the Fourier transform of the

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Coulomb perturbing potential. Considering a case where a charged impurity (e^+), either a substrate impurity or an interface trap charge, is located at a distance d away from the 2DEG in the inversion channel (Fig. B-4). V(|**q**|) can then be expressed as [102]

$$V(|\boldsymbol{q}|) = \frac{e^2}{2\epsilon_s}\frac{e^{-|\boldsymbol{q}|d}}{|\boldsymbol{q}| + q_{TF}}, \tag{B-19}$$

where q_{TF}, the Thomas-Fermi screening wavevector, accounts for the screening of the impurity potential by the redistribution of free carriers (2DEG) in the inversion channel. A larger q_{TF} is indicative of a stronger 2DEG screening since a larger q_{TF} leads to a smaller V(|**q**|) (Equation (B-19)) and, consequently, a weaker Coulomb scattering (Equation (B-18)).

The 2DEG screening strength is related to the 2DEG polarizability Π_{TF} through the relationship [102]

$$q_{TF} = \frac{e^2}{2\epsilon_s}\Pi_{TF}, \tag{B-20}$$

where Π_{TF} is given by [102]

$$\Pi_{TF} = \frac{dn_{2D}}{dE_F}. \tag{B-21}$$

By expressing the 2DEG density as [66]

$$n_{2D} = g_{2D}\int_{E_i}^{\infty} f(E, E_F)dE, \tag{B-22}$$

where g_{2D} and f(E, E_F) are the 2D density-of-states and Fermi-Dirac distribution function, respectively, Equation (B-21) can be recast into

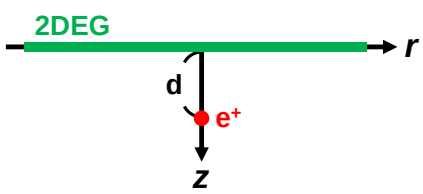

Fig. B-4 A schematic showing the geometrical relationships between the charged impurity (e^+) and 2DEG.

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$$\Pi_{TF} = g_{2D}\int_{E_i}^{\infty}\frac{\partial f(E,E_F)}{\partial E_F}dE$$
$$= \frac{g_{2D}}{kT}\int_{E_i}^{\infty} f(E,E_F)[1-f(E,E_F)]dE. \quad \text{(B-23)}$$

This indicates that Π_{TF} is proportional to the area under the joint Fermi-Dirac distribution $f(E, E_F)[1 – f(E, E_F)]/kT$ above the first subband energy E_i (Fig. B-5). Therefore, the "polarizable" electrons, i.e., the electrons that contribute to 2DEG screening, are those thermally activated near the Fermi level E_F (Fig. B-5). As temperature decreases, the Fermi-tail is suppressed, which results in an increase in E_F if the electron density is held constant. Consequently, Π_{TF} increases, and the number of "polarizable" electrons increases as well (Fig. B-5). This is confirmed by performing a direct integration on Equation (B-23):

$$\Pi_{TF} = \frac{g_{2D}}{1+e^{(E_i-E_F)/kT}}. \quad \text{(B-24)}$$

At room temperature, E_F is far below E_i, and thus Π_{TF} is close to 0 (Equation (B-24)). However, at low temperatures, E_F is above E_i, and thus Π_{TF} approaches g_{2D} (Equation (B-24)). The increase in Π_{TF} with decreasing temperature (Fig. B-5) and the asymptotic behavior of Π_{TF} at low temperatures (saturates to g_{2D}) are corroborated by a numerical

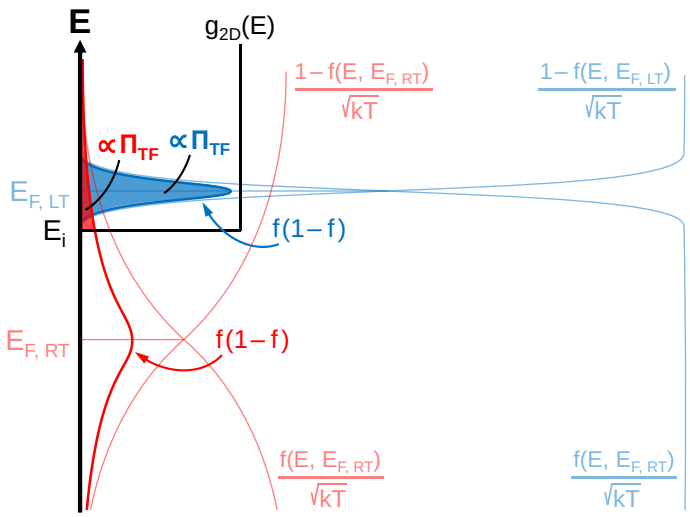

Fig. B-5 A schematic showing the relationship between the polarizability Π_{TF} and the joint Fermi-Dirac distribution $f(E, E_F)[(1 – f(E, E_F))]/kT$ at a fixed electron density at room temperature and low temperature.

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calculation (Fig. B-6 (a)).

As a result, the screening effect gets stronger as temperature decreases (Equation (B-20)), which counteracts the enhancement of Coulomb scattering at lower temperatures. As temperature decreases, the faster the screening effect enhances compared to the intensifying Coulomb scattering, the milder (smaller γ) the reduction in μ_C would be (Equation (B-14)). If the screening effect were very effective compared to Coulomb scattering, which usually occurs at very low temperatures [31, 74], increases in μ_C with decreasing temperature (negative γ) could even be observed (Equation (B-14)). It is worth mentioning that due to the asymptotic behavior of Π_{TF} at low temperatures, γ is expected to exhibit a similar asymptotic behavior in the low-temperature limit.

B.4.3 The Density Dependence

A more detailed investigation reveals that the 2DEG polarizability Π_{TF} (Equation (B-24)) is dependent on the scattering wavevector $|\mathbf{q}|$ through the relationship [88]

$$\Pi_{TF}(|\boldsymbol{q}|) = \frac{g_{2D}}{1+e^{(E_i-E_F)/kT}}\left\{1-\left[1-\left(\frac{2k_F}{|\boldsymbol{q}|}\right)^2\right]^{1/2}\right\}, \qquad \text{(B-25)}$$

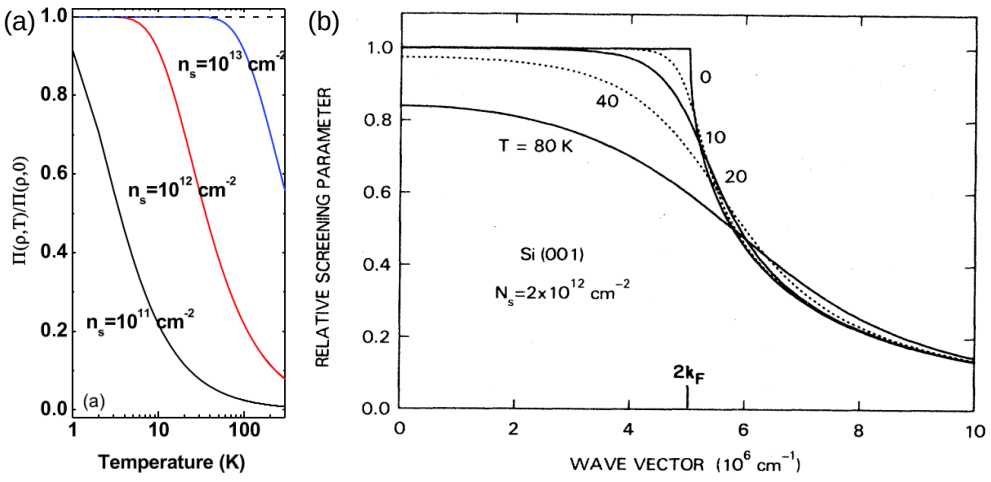

Fig. B-6 Relative screening parameter (polarizability Π_{TF}) vs. (a) temperature at various 2DEG densities [88] and (b) the scattering wavevector $|\mathbf{q}|$ at various temperatures [106].

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where k_F, the Fermi-wavevector, is proportional to the square of 2DEG density [107]:

$$k_F \propto (2\pi n_{2D})^{1/2}. \quad \text{(B-26)}$$

In this case, the screening effect is effective only up to $2k_F$ since $\Pi_{TF}(|\mathbf{q}|)$ decreases dramatically as $|\mathbf{q}|$ increases above $2k_F$ (Fig. B-6 (b)). As n_{2D} increases, $2k_F$ increases, which broadens the effective screening range. Therefore, the screening effect becomes stronger as n_{2D} increases (Fig. B-6 (a)), which leads to an increase in μ_C with density. This explains the positive density dependence of μ_C (positive α) (Equation (B-14)). As temperature decreases, $\Pi_{TF}(|\mathbf{q}|)$ increases at every $|\mathbf{q}| < 2k_F$ (Fig. B-6), indicating an enhancement in screening strength at lower temperatures, irrespective of n_{2D} (Fig. B-6 (a)). This leads to a more drastic increase in μ_C with density as temperature decreases and, consequently, explains the higher density dependence (larger α) of μ_C as the temperature decreases (Equation (B-14)).

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PUBLICATION LIST

Journal

1. **Yen-Yang Chen**, Kai-Ying Tien, Wei-Hsiang Kao, Chia-You Liu, and Jiun-Yun Li, "Electron Transport in Ge(Sn) Metal-Oxide-Semiconductor Field-Effect Transistors at Cryogenic Temperatures," *Applied Physics Letters* (submitted).
2. Kai-Ying Tien*, **Yen-Yang Chen***, Chia-You Liu, Hsiang-Shun Kao, and Jiun-Yun Li, "Extremely High Electron Mobility in GeSn Epitaxial Films by Chemical Vapor Deposition," *Advanced Electronic Materials*, vol. 11, no. 11, p. 2400925, 2025.
3. Nai-Wen Hsu, Wei-Chih Hou, **Yen-Yang Chen**, Yu-Jui Wu, Hsiang-Shun Kao, Charles Thomas Harris, Tzu-Ming Lu, and Jiun-Yun Li, "Temperature Dependence of Charge Distributions and Carrier Mobility in an Undoped Si/SiGe Heterostructure," *IEEE Transactions on Electron Devices*, vol. 69, no. 2, pp. 482-486, 2022.

Conference

1. **Yen-Yang Chen**, Kai-Ying Tien, Chia-You Liu, Wei-Hsiang Kao, and Jiun-Yun Li, "Electron Transport in Ge(Sn) n-type Metal-Oxide-Semiconductor Field-Effect Transistors at Cryogenic Temperatures," *2024 International Conference on Solid State Devices and Materials*, Himeji, Hyogo, Japan, Sep. 1 – 4, 2024 (oral).

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