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基材鰭式場效電晶體與鍺量子井場效電晶體之模擬研究

Simulation Study of Bulk FinFET and Ge Quantum Well pFET

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摘要

基材鰭式場效電晶體具有散熱佳，低製造成本，與傳統場效電晶體製程相容等優點。結合 RCAT 與三面閘極的結構展現非常優異壓制短通道的能力。在模擬結果顯示該結構具有良好的 SS 及 DIBL 的電性特徵。由於載子在完全空乏的鰭式通道流動，臨界電壓會受到鰭式通道的寬度及高度影響，必須重新修正。相較於 RCAT 結構，基材鰭式場效電晶體對於凹槽深度及反向基板偏壓的變化較為不敏感。為了降低漏電流，在通道加上較高的參雜濃度，同時也會有較好控制能力。而汲極輕度參雜(LDD)被用來減低價帶至導帶的穿隧電流。同時，增加閘極-汲極氧化層厚度可以在犧牲少許控制能力的狀態下有效減低漏電流。

應用於未來高速元件的一種 Si-cap/Ge/Si 結構以模擬方式探討它的特性。Si-cap 假設為完全張弛，而鍺通道層假設為完全應變。90-nm 平板矽場效電晶體一搬須要有 HALO 怖植以降低短通道效應。矽鍺異質結構造成的量子井可以將電洞侷限在鍺通道內。模擬結果顯示，相較於矽元件，此舉可以增加閘極的控制能力。Ge 的 BTBT 性質在分析後放入計算中。不同的矽覆蓋層與鍺通道厚度所造成的漏流增減均進行模擬驗證

關鍵字: 場效電晶體、基材鰭式場效電晶體、臨界電壓、量子井

Abstract

Bulk FinFET has advantages of heat dissipation, wafer cost, process compatibility and extendibility of conventional planar MOSFET technologies. The combination of recess channel array transistors (RCAT) technology and triple-gate in bulk silicon prove excellent SCEs control ability. It owns superior subthreshold slope (~70 mV/dec) and DIBL characteristics in simulation works. Due to the fully depleted fin channel, the subthrehold voltage is modified by not only channel doping but also the fin width and fin height. The saddle-like FinFET structure shows good immunity of electric characteristics of recess depth variation and reverse body bias comparing to RCAT structure. To integrate with DRAMs process, the leakage current must be suppressed. With higher channel doping, it reduces the I_{off} current and subthreshold slope. By adopting LDD in S/D region, the band-to-band-tunneling generation is smaller. Also, increasing the thickness of gate-to-drain oxide, can help the leakage suppression a lot but only a slightly control ability sacrifice.

A Si-cap/Ge/Si pFET structure based on 90-nm node for future high-speed transistor application is simulated. The Si-cap is assume to be relax and Ge layer is fully strained. For 90-nm node planar control-Si device, HALO implantation is necessary to reduce the SCEs. The Si-cap/Ge heterostructure results in the holes confinement in the quantum well, which provide better control ability comparing to

control-Si device. The BTBT model for Ge is analyzed and put into simulation. The leakage due to smaller bandgap of Ge is examined by different Si-cap thickness and Ge layer thickness.

Keywords: MOSFET, Bulk FinFET, Threshold Voltage, Quantum Well

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Chapter 1
Introduction

1.1 Advantage of MOSFET Scaling Down

Computing capability has increased dramatically over the decades, enabled by significant advances in silicon integrated circuit technology led by the continued miniaturization of the MOS transistor. The rapid progress in the semiconductor industry has been driven by improved circuit performance and functionality together with reduced manufacturing costs. Since the 1960s, the number of transistors that can be inexpensively placed on an integrated circuit is increasing exponentially, doubling approximately every two years [1], which is depicted in Figure 1.1 [2]. While Moore's law only describes the rate of increase in transistor density, reduction of the physical MOS device dimensions has improved both circuit speed and density in the following ways: a) Circuit delay time decreases with a reduction in gate length as a factor of $\sim 1/\kappa$ ($\kappa > 1$), allowing for faster circuits, b) Chip area decreases with $\sim 1/\kappa^2$ enabling higher transistor density and cheaper ICs. c) Switching power density ~ 1 constant; allows lower power per function or more circuits at the same power. Device scaling has been a relatively straightforward solution thus far, but physical limits are approaching, and new materials and device structures are needed to continue scaling

trends.

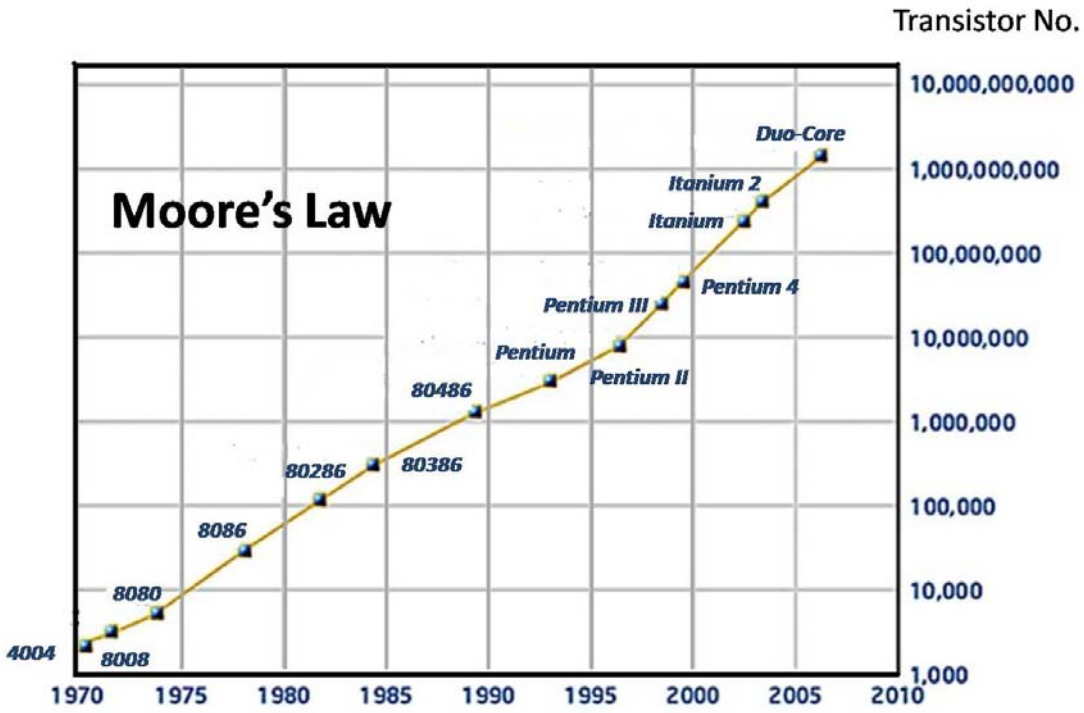

Figure 1-1 Moore' Law

1.2 Planar Bulk-Si MOSFET Scaling Challenges

The planar bulk-silicon MOSFET has been the base of the semiconductor industry over the last 40 years. People keep shrink the gate length to improve the performance and reduce the cost of single device. However, the scaling of bulk MOSFETs becomes increasingly difficult for gate lengths below ~20nm expected by the year 2009. As the gate length is reduced, the channel potential influenced by the source and drain increases relative to the gate, leading to significantly degraded short-channel effects (SCE). This cause some drawbacks, a) increased off-state leakage, b) threshold voltage (V_{th}) roll-off, and c) reduction of V_{th} with increasing

drain bias due to a modulation of the source-channel potential barrier by the drain voltage, also called drain-induced barrier lowering (DIBL). In order to maintain the relatively strong gate control of the channel potential in bulk devices, various technological improvements such as ultra-thin gate dielectrics, ultra-shallow source/drain junctions, halo implants and advance channel dopant profile engineering techniques such as super-steep retrograde wells have been necessary. Each of these technologies is now approaching fundamental physical limitations which may, in turn, limit further scaling of device dimensions. In MOS devices, the gate dielectric thickness is the single most important device dimension to enable device scaling and has also been the most aggressively scaled one. However, gate dielectrics are already so thin that quantum mechanical direct tunneling through them results in significant gate leakage currents below ~20Å. The use of alternative high-κ gate dielectric materials can provide a small effective oxide thickness to maintain adequate gate control needed for L_g scaling while providing a large physical barrier to gate-oxide tunneling, thereby reducing gate leakage. Besides, in order to scale bulk-Si transistors, heavy body doping is also necessary to eliminate leakage paths far from the gate dielectric interface and to increase back-gate (substrate) control of the body. For sub-100nm gate length devices, a strong halo implant is generally used to suppress sub-surface leakage, but this tends to increase the average channel doping in small L_g

devices. High channel doping concentration, however, reduces carrier mobility due to impurity scattering and increased transverse electric field, increases subthreshold slope, enhances band-to-band tunneling leakage, and increases depletion and junction capacitances. These factors may combine to significantly degrade device performance, which is unwanted. In summary, how to increase on-current without those disadvantages is our main goal trying to achieve.

1.3 General Background For Bulk FinFET

From previous section, it mentioned that, to overcome the drawbacks of planar MOSFTE scaling, new device structure is needed. While two-dimension planar devices almost reach it's physical limits, a three-dimensional MOSFET structure is proposed, which is called FinFET. FinFET is one of the promising candidates for device structure in sub-50nm technology node and beyond, because of its good cut-off characteristics due to double gate mode operation. Generally, there are two kinds of FinFET structure proposed, namely a bulk-FinFET fabricated on a bulk Si substrate and SOI-FinFET on an SOI substrate . The bulk-FinFET is superior to the SOI-FinFET in terms of wafer cost, process compatibility and extendibility of conventional planar MOSFET technologies.

DRAMs need good Ioff characteristic to ensure enough data retention time. Hence, a bulk FinFET is a promising candidate for sub-50 nm DRAM technology and some

of the implementations of FinFET for DRAM cell array are already reported [3] [4]. According the DRAMs roadmap [5], in sub-50nm node, FinFET will replace RCAT and DRAMs is viewed as the first one who will adopt FinFET in their products. Thus, in our simulation, the device was designed by the assumption of DRAMs application.

Year		04	06	08	10	12
Node (nm)		80	65	50	40	30
Lithography		ArF	ArF Immersion	F2 Immersion , EUV		
Gate		Wsix+Si	W+Si	W+WN / CoSix		
Metal / IMD		Al		Al or Cu / Low-K		
DRAM	Density	1Gb	2Gb / 4Gb	4Gb / 8Gb	16Gb ~	
	Cell Structure	RCAT		FinFET		
	Capacitor	MIS	MIM (AHO / HfO / TiO2)			

Table 1-1 DRAM roadmap to 2012

1.4 General Background For Ge Quantum Well pFET

As the industry aggressively scale transistors in accordance with Moore's Law to sub-20nm dimensions, it becomes increasingly difficult to maintain the required device performance. Currently, the increase in drive currents for faster switching speeds at lower supply voltages is largely at the expense of an exponentially growing leakage current, which leads to a large standby power dissipation. There is an important need to explore novel channel materials that would provide us with high-performance nanoscale MOSFETs. Due to their significant transport advantage, high-mobility materials are very actively being researched as channel materials for future highly scaled CMOS. Recent progress in epitaxial growth and demonstrations

of device application of Si-based hetero-junctions provide a foundation for the foundation for the investigation of such hetero-structure MOSFETs. The use of Si-based materials also allows one to take advantage of the maturity and world-wide investment in Si processing technology. Modifying the mobility by the use of a different material, as opposed to adjusting doping profiles, geometric design, or vertical field in the channel, is advantageous because the performance gain will be a multiplicative factor to the enhancement obtained by geometric scaling, without compromising other device criteria such as short channel effects. The strained Si, SiGe, and even pure Ge provide the carrier mobility enhancement over bulk Si [6-9]. Recently, using strain in Si-based hetero-structures has been the research and industrial subject in enhancing carrier mobility. A thin Si layer grown on relaxed Silicon-Germanium ($Si_{1-x}Ge_x$) will be strained since relaxed $Si_{1-x}Ge_x$ has a larger lattice constant than bulk Si. This produces enhanced in–plane carrier mobility in the strained-Si, as well as band offsets between the relaxed $Si_{1-x}Ge_x$ and the strained-Si, which can be used for carrier confinement in advanced device structures. For However, although the carrier mobility in strained-Si is enhanced, the enhancement has limits. Tremendous drive current enhancement is impossible if only strained-Si is applied. In addition, for a given doping concentration, hole mobility in Si is significantly lower than electron mobility. The lower mobility is reflected in the

asymmetric design of CMOS logic circuits. Significant enhancement in p-MOSFET performance will allow more symmetric design of CMOS logic circuits. Ge epitaxially grown on a Si substrate is a promising channel material for MOSFETs since bulk Ge exhibits a much higher mobility for both electrons and holes as compared to Si. In addition, a theoretical calculation has shown that compressively strained-Ge layer exhibits a drastic enhancement of hole mobility much higher than that of unstrained Ge [10]. Recently, a hole mobility of 2700cm2/Vs at room temperature has been reported [11] in a strained-Ge channel.

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Chapter 2
Physical Models

2.1 Introduction Of Numerical Simulator

For constructing and analyzing the three-dimensional Bulk FinFET device, the Technology Computer Aid Design (TCAD) software products provided by Synopsys corporation is applied. Sentaurus/ISE-TCAD software[1], which is a sophisticated product, cover the entire range from process simulation over device and circuit and systems simulation to complete package simulation. On the basis of three-dimensional simulation, we adopted the 3-D simulators of Sentaurus/ISE-TCAD tools such as the DEVISE as structure emulator and the DESSIS as device simulator. The DEVISE of Sentaurus /ISE-TCAD helps us to construct the physical FinFET structure, impurity profile, and mesh definition. Then, the DESSIS of Sentaurus/ISE-TCAD can include many device physical models combined with continuity equation and solve it by finite-element method (FEM). The solution can help us to analyze the electric characteristics of FinFET device. This chapter describes physical models used in the DESSIS of Sentaurus/ISE-TCAD for FinFET structure. It is because DESSIS incorporates advanced physical models and robust numeric methods for the simulation of most types of semiconductor device ranging from very deep submicron

Si FinFETs to large bipolar power structures. To make the simulation more convincing, we need to clarify about the model we use in FinFET structure. The physical models of FinFET described in this chapter are transport equations, quantization model, mobility models, and generation-recombination models.

2.2 Transport Equations

The transport equations describe the carriers tranferring phenomena in the interior of semiconductor. The classical semiconductor equations including the Poisson equation, continuity equations, and current densities equations are displayed in section 2.2.1 and 2.2.2. The consideration for device operation at different temperatures is presented in section 2.2.3. Finally, in section 2.2.4, the manipulation of transport equations covering semiconductor and contact metal is presented.

2.2.1 Governing Equations For Device Physics

The three equations governing charge transport in FinFET devices are the Poisson equation, electron continuity equation, and hole continuity equation. The Poisson equation is:

$$\nabla^2\varphi = -\frac{q}{\varepsilon}[p(x) - n(\mathrm{x}) + \mathrm{N_d^+}(\mathrm{x}) - \mathrm{N_a^-}(\mathrm{x})] \quad (2.1)$$

This equation specifies the electrostatic potential and the electric field within the device. Here φ is the electrostatic potential, ε is the electrical permittivity, q is the electronic charge, n is the electron density, p is the hole density, $\mathrm{N_d^+}$ is the number of

ionized donors, and N_a^- is the number of ionized acceptors. The electron and hole continuity equations are:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla J_n - R_n + G_n \tag{2.2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla J_p - R_p + G_p \tag{2.3}$$

Where R_n and R_p are the electron and hole recombination rate, G_n and G_p are the electron and hole generation rate. J_n is the electron current density. J_p is the hole current density.

2.2.2 Drift-Diffusion Equation

The drift-diffusion model of a semiconductor is frequently used to describe semiconductor devices. It provides a powerful description of microscopic particle transport on the phenomenological level where current densities for electrons and holes are given by:

$$J_n = -nq\mu_n\nabla\Phi_n \tag{2.4}$$

$$J_p = -pq\mu_p\nabla\Phi_p \tag{2.5}$$

Where μ_n and μ_p are the electron and hole mobilities, and Φ_n and Φ_p are the electron and hole quasi-Fermi potentials.

2.3 Mobility Models

The carrier mobility in a MOSFET channel is significantly lower than that in bulk silicon, due to additional scattering mechanisms. Section 2.3.1 describe how these

models combine together. And the following sections list the model we use separately. In the simplest case, the mobility is a function of the lattice temperature. The so-called constant mobility model described in section 2.3.2, which is due to phonon scattering, should only be applied for un-doped materials. For doped materials, the carriers are scattered by the impurities. This leads to a degradation of the mobility. Section 2.3.3 introduces the models that describe this effect. Moreover, models that describe the mobility degradation at interfaces, for example, the silicon–oxide interface in the channel region of bulk FinFET are introduced in section 2.3.4. These models account for the scattering with surface phonons and surface roughness. Finally, the models that describe mobility degradation in high electric fields are discussed in section 2.3.5.

2.3.1 Mobility Models Combination

Mobility model is one of the most important physical models in device simulation. If more than one mobility model is activated, the different mobility contributions are combined according to the following scheme – different bulk and surface mobility contributions are combined following Mathiessen' s rule:

$$\frac{1}{\mu} = \frac{1}{\mu_{b1}} + \frac{1}{\mu_{b2}} + \cdots + \frac{1}{\mu_{s1}} + \frac{1}{\mu_{s2}} + \cdots \tag{2.6}$$

If the high field saturation model is activated, the final mobility is computed in two steps. First, the low field mobility is determined according to (2.6). Second, the final mobility is computed from a (model-dependent) formula as a function of a

driving force F :

$$\mu = f(\mu_{low} + F) \tag{2.7}$$

2.3.2 Mobility Due to Lattice Scattering (Constant mobility model)

The constant mobility model assumes that carrier mobility is only affected by phonon scattering and, therefore, dependent only on the lattice temperature:

$$\mu_{const} = \mu_L(\frac{T}{300K})^{-\gamma} \tag{2.8}$$

Where μ_L is the mobility due to bulk phonon scattering, T is the lattice temperature. The γ of electrons and holes are 2.5 and 2.2, respectively.

2.3.3 Doping-Dependent Mobility Degradation (Masetti Model)

In doped semiconductors, scattering of the carriers by charged impurity ions leads to degradation of the carrier mobility. Sentaurus Device supports two models for doping-dependent mobility. The default model used by Sentaurus Device to simulate doping-dependent mobility in silicon was proposed by Masetti *et al*. [1]. The Masetti model is:

$$\mu_{dop} = \mu_{mini1} \exp\left(-\frac{P_c}{N_i}\right) + \frac{\mu_{const} - \mu_{mini2}}{1+(\frac{N_i}{C_r})^{\alpha}} - \frac{\mu_1}{1+(\frac{C_s}{N_i})^{\beta}} \tag{2.9}$$

where $N_i = N_a + N_d$ denotes the total concentration of ionized impurities.

2.3.4 Mobility Degradation At Si-Insulator Interface

The model for carrier mobility in silicon inversion layers and in the bulk of the

semiconductor is the one which mostly affects the accuracy of the results of the terminal current calculation in two- and three-dimensional (2-D, 3-D) MOSFET simulation programs. It is because that in the inversion layer of a bulk FinFET, the high transverse electric field forces carriers to interact strongly with the Si–insulator interface. The carrier scattering is subjected to acoustic surface phonons and surface roughness. The models in this section describe mobility degradation caused by these effects. The surface contribution due to acoustic phonon scattering has the form:

$$\mu_{ac} = \frac{B}{F_{\perp}} + \frac{C(\frac{N_i}{N_0})^{\lambda}}{F_{\perp}^{1/3}(\frac{T}{T_0})^{k}} \quad (2.10)$$

and the contribution attributed to surface roughness scattering is given by:

$$\mu_{sr} = (\frac{(\frac{F_{\perp}}{F_{ref}})^{A}}{\delta} + \frac{F_{\perp}^{3}}{\eta})^{-1} \quad (2.11)$$

where the reference field F_{ref} = 1 V/cm ensures a unit-less numerator and $F_{\perp}$ is the transverse electric field normal to the semiconductor-insulator interface. These models can be combined with this form:

$$\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}} \quad (2.12)$$

where $D = \exp(\frac{-x}{l_{crit}})$ (*x* is the distance from the interface and l_{crit} is a fit parameter) is a damping that switches off the inversion layer terms far away from the interface. In the Lombardi model [2], the exponent A in (2.11) is equal to 2.

2.3.5 High Field Saturation

In high electric fields, the carrier drift velocity is no longer proportional to the

electric field strength, instead, the velocity saturates to a finite speed. In our work, we apply Canali model for the description of this effect [3]. The Canali model originates from the Caughey–Thomas formula [4], but has temperature-dependent parameters, which were fitted up to 430 K by Canali et al. :

$$\mu(F) = \frac{\mu_{low}}{[1+(\frac{\mu_{low}F}{v_{sat}})^{\beta}]^{1/\beta}} \quad (2.13)$$

where μ_{low} denotes the low field mobility. And $F = |\nabla\varphi_c|$, for the gradient of the Fermi potential $\nabla\varphi_c$.

2.4 Quantization Model

With the progress of device scaling, some features of current MOSFETs (oxide thickness, channel width) have reached quantum mechanical length scales. That means the wave nature of electrons and holes can make significant difference from classical charge inversion theory. The most basic quantization effects in MOSFETs are the shift of the threshold voltage and reduction of the gate capacity due to less energy levels in the inversion region. To include quantization effects in a classical device simulation, a simple approach is to introduce an additional potential to the classical density formula:

$$n = N_c \exp\left(\frac{E_{Fn} - E_c - \Lambda}{k_b T}\right) \quad (2.12)$$

where n is the electron density, T is the carrier temperature, k_b is the Boltzmann constant, N_c is the conduction band density of states, E_c is the conduction band

energy, and E_{Fn} is the electron Fermi energy. When using Fermi statistics, the exponential function in is replaced by a Fermi integral of order 1/2. The density gradient model is numerically robust, but still increasing the computation time. It can be applied to MOSFETs, quantum wells, SOI structures, and bulk FinFET, and gives a reasonable description of terminal characteristics and charge distribution inside a device. It can describe both 2-D and 3-D quantization effects. Although for channel width larger 10 nm, the effect of quantum is relative small.[5] In order to obtain more correct density distribution in the channel, we can still apply the density gradient model as our reference in some simple testing.

2.4.1 Physical Model Description

For the density gradient model [6] [7], Λ can be expressed in terms of a partial differential equation:

$$\Lambda = -\frac{\gamma\hbar^2}{12m}\left\{\nabla^2 \log n + \frac{1}{2}(\nabla \log n)^2\right\} = -\frac{\gamma\hbar^2}{6m}\frac{\nabla^2\sqrt{n}}{\sqrt{n}} \quad (2.13)$$

Where $\hbar = h/2\pi$ is the reduced Planck constant, *m* is the DOS mass, and γ is a fit factor. The density gradient model increases the current through the semiconducting potential barriers. However, this effect is not a trustworthy description of tunneling through the barrier. To model tunneling, use one of the dedicated models that Sentaurus/ISE provides. To suppress unwanted tunneling or to fit tunneling currents despite these concerns, consider using the modified mobility model according to:

$$\mu = \frac{\mu_{cl} + \gamma \mu_{tun}}{1+\gamma} \quad (2.14)$$

where μ_{cl} is the classical mobility, μ_{tun} is a fit parameter, and $\gamma = \max(0, {}^{n}/_{n_c} - 1)$. Here, n_c is the 'classical' density.

2.5 Generation and Recombination

The fundamental generation and recombination of Shockley-Read-Hall (SRH) and Band-to-band tunneling(BTBT) model are both applied.

2.5.1 Shockley–Read–Hall recombination (SRH)

To account for excess electrons and holes recombination, one can assume there is an allowed energy state, called a "tarp", within the forbidden bandgap. The trap can capture electrons and holes with almost equal probability. The balance equation for each trap yields a Shockley-Read-Hall (SRH) rate. The individual characteristic properties of generation-recombination centers depend strongly on the technology. Therefore, they are usually lumped together in quantities like the effective electron and hole lifetimes, ending up with one effective single-level SRH rate. In Sentaurus/ISE, the following form is implemented:

$$R^{SRH} = \frac{np - n_i^2}{\tau_p(n+n_1) + \tau_n(p+p_1)} \quad (2.41)$$

with

$$n_1 = n_i \exp\left(\frac{E_t}{kT}\right) \quad (2.42)$$

and:

$$p_1 = n_i \exp\left(\frac{-E_t}{kT}\right) \quad (2.43)$$

where E_t is the difference between the defect level and intrinsic level. The silicon default value is $E_t = 0$. The minority lifetimes τ_n and τ_p are modeled as a product of a doping-dependent, field-dependent, and temperature-dependent.

2.5.2 Band–To–Band Tunneling Model (BTBT)

The reduction of the junction leakage current of MOSFETs transistors becomes a crucial issue in the forth coming generation of devices. Besides the junction current which depends on the drain-to-bulk voltage, an additional leakage current is generated in the Drain in the vincinity of the surface when a high Drain-to-Gate voltage is applied. This Gate Induced Drain Leakage (GIDL), which has become one of the most limiting factor on advanced double-oxide devices, can even be larger than the channel off-current of long devices. It is crucial, especially to DRAM circuit design.

Both GIDL and junction leakage are relate to band-to-band tunneling. To show both of the leakage phenomena, we need to apply band-to-band tunneling model in our simulation. Band-to-Band-Tunneling (BTBT) GIDL has been considerably studied [8]–[14] and is now available in most state-of-art MOSFET public domain models.

In our work, we applied Hurkx model as tunneling model. The Hurkx band-to-band tunneling model [15] is implemented to provide a complete range of commonly used

band-to-band tunneling models in Sentaurus/ISE. The tunneling carriers are modeled by an additional generation–recombination contribution. In the Hurkx model, this contribution is expressed as:

$$G = -A \cdot D \cdot \left(\frac{F}{F_0}\right)^P \cdot \exp\left(-\frac{B \cdot E_g(T)^{1.5}}{E_g(300K)^{1.5} F}\right) \quad (2.2)$$

Where F is the electric field, F_0=1V/m, and:

$$D = \frac{np - n_i^2}{(n+n_i)(p+n_i)}(1 - |\alpha|) + \alpha \quad (2.2)$$

For $\alpha = 0$, it gives the original Hurkx model. $\alpha = -1$ gives only generation, and $\alpha = +1$ gives only recombination. For many other BTBT description model, they describe tunneling by means of a current density, which are only suitable for post-processing calculations and cannot be incorporated into the continuity equations. Hurkx model avoid this drawback. Also, from the equation, we know that Hurkx model will degenerate to normal SRH model under low electric field, which is physics sophisticated.

2.6 Reference

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Chapter 3

Simulation Study Of Bulk FinEFT

3.1 Motivation

For applying in DRAMs, the MOSFET need good Ioff characteristic to ensure enough data retention time. Hence, a bulk FinFET is a promising candidate for sub-50 nm DRAM technology and some of the implementations of FinFET for DRAM cell array are already reported [1] [2]. FinFET structure exhibits excellent subthreshold characteristics. In this chater, we perform the simulation with a saddle-like FinFET structure (S-Fin) [3] on bulk Si substrate for sub-50 nm deep trench DRAMs and compare it with a recess channel array transistor (RCAT) structure. In this chapter, the author will examine and discuss these fundamental characteristics with recess depth, fin width and fin height, and negative body bias variation. Also, the author compare the characteristics between S-Fin and RCAT.

3.2 Device Structure

A saddle-type structure is depicted in Figure 3-1. The U-shape channel and side gate is the combination of RCAT and triple gate FinEFT technology. Gate length (Lg) and width (W) are both 40 nm. The gate oxide thickness (Tox) is 4 nm according ITRS roadmap and the channel fin height is 10 nm. The effective channel length is

Leff = Lg+2H. For trench DRAMs technology, a large junction depth is demanded to reduce the parasitic resistance between the trench capacitance and the 3D transistor (Figure 3-1(b)). Therefore, the access time can be lower. However, GIDL current is considerable due to the large overlap between gate and storage node. To reduce the amount of GIDL current, a lateral decay of the source/drain doping profiles (Figure 3-1(c)) is adopted. The negative substrate bias (-0.5V) is applied to keep a reverse bias between the substrate and the bottom plate of the deep trench capacitor. Although applying p+ poly-gate can adjust the Vth, but it also produces higher GIDL due to the higher band bending near the interface. Thus, a n+ ploy-gate is used that we can benefit from its lower GIDL. In this paper, characteristics of device are simulated by TCAD simulator [4]. We activated band-to-band model (BTBT) [5] to evaluate the GIDL current in the critical regions with high electric field.

It is also important to know that this kind of structure can be realize in fabrication process [1]. First, the groove-like RCAT channel and the fin structure to the channel width direction were formed. While the damascene-FinFET(D-Fin) [6] is constructed by etching only the field oxide and the recess channel array transistor (RCAT) structure is formed by etching only the active silicon, the saddle-like bulk FinFET (S-Fin) is prepared by etching both of the active silicon and the field oxide. The well-rounded corner profile of fin was obtained. The fin height can be controlled to be

40nm. A 70nm DRAM technology was used for the device evaluation. A damascene-FinFET (D-Fin) and an RCAT were also fabricated by controlling the dry-etching condition. In our work, we perform both S-Fin and RCAT structure. The RCAT structure is with the same dimension like S-Fin but just remove the double side-gate.

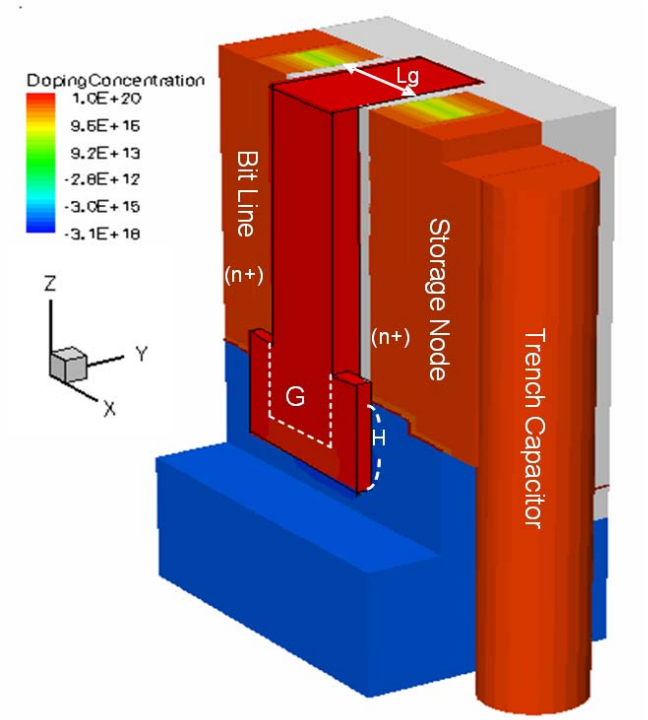

Figure 3-1 (a) FinFET structure and design parameters for device simulation.

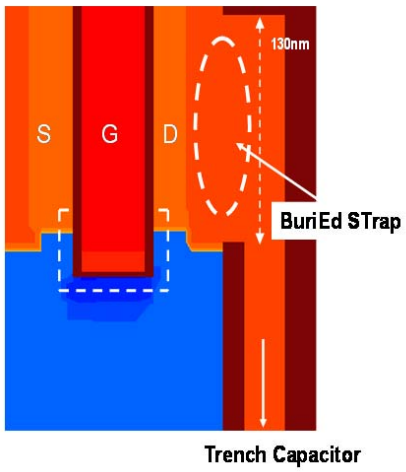

Figure 3-1 (b) Buried strap scheme

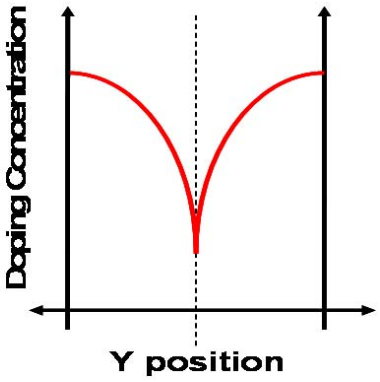

Figure 3-1(c) Gaussian S/D profile

3.3 Threshold Voltage, DIBL Definition

3.3.1 Threshold Voltage Definition

The V_{th} model of the conventional planar MOSFETs with long-channel length and wide channel width is expressed like [7]:

$$V_{th} = V_{FB} + 2\varphi_B + \frac{qN_b x_{dep}}{C_{ox}} \quad (3.1)$$

where V_{FB} and φ_B are the flat-band voltage and Fermi potential, respectively. N_b, x_{dep}, and C_{ox} are the body doping, channel depletion length under the gate, and gate capacitance, respectively. Equation (3.1) is based on the linear operation region. Here, we ignore oxide charge to simplify the modeling form. But for fully-depleted devices, the channel width may be much less than the depletion length. Thus the equation for threshold voltage can be expressed like:

$$V_{th} = V_{FB} + 2\varphi_B + \frac{qN_b W}{2C_{ox}} \quad (3.2)$$

This form doesn't consider QM effect near the Si/Oxide interface, yet. But for consideration of more accuracy, QM effect should not be ignored.

3.3.2 Drain Induced Barrier Lowering Definition

Drain induced barrier lowering or DIBL is a secondary effect in MOSFETs referring originally to a reduction of threshold voltage of the transistor at higher drain voltages. The origin of the threshold decrease can be understood as a consequence of charge neutrality: the Yau charge-sharing mode [8]. The combined charge in

the depletion region of the device and that in the channel of the device is balanced by three electrode charges: the gate, the source and the drain. As drain voltage is increased, the depletion region of the p-n junction between the drain and body increases in size and extends under the gate, so the drain assumes a greater portion of the burden of balancing depletion region charge, leaving a smaller burden for the gate. As a result, the charge present on the gate retains charge balance by attracting more carriers into the channel, an effect equivalent to lowering the threshold voltage of the device.

3.4 Bulk FinFET Recess Depth

3.4.1 Introduction

The depth of recess channel (H) is relative to effective channel length by 2H+Lg. With fixed Lg, the larger H can increase the effective channel length.

3.4.2 Threshold Voltage Variation With Recess Depth

Figure 3-2 shows the RCAT and S-Fin threshold voltage versus the recess etch depth with a Vds=0.05V. The S-Fin shows relative small variation of threshold voltage with the recess depth comparing to RCAT. ΔV_{th} of RCAT is 0.225V with depth varying from 30nm to 60nm. And ΔV_{th} of S-Fin is only 0.015V with the same variation range. It means S-Fin is less sensitivity of recess depth variation and better process margin in the recess depth.

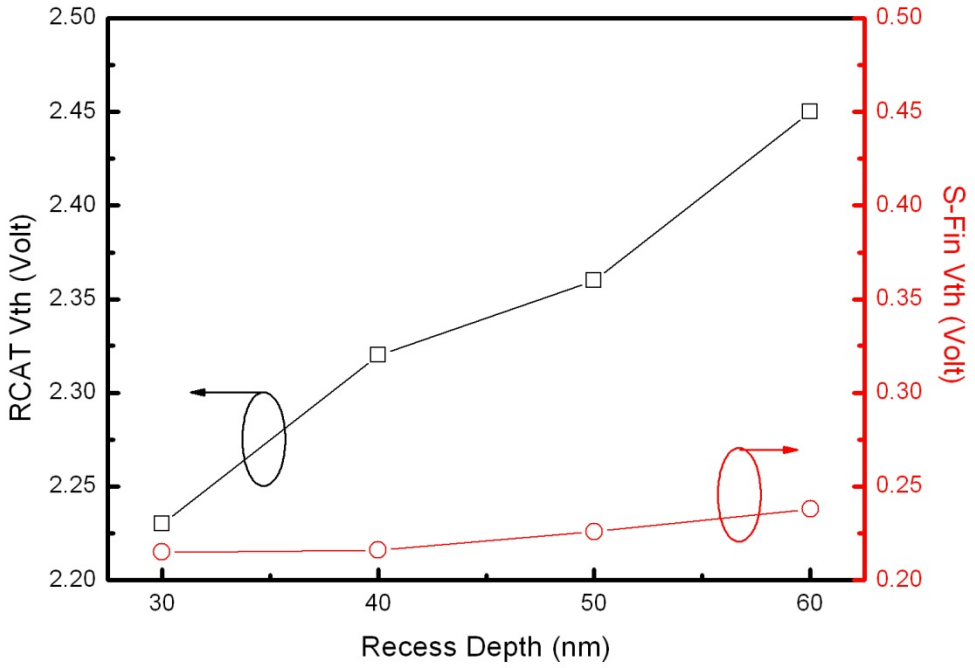

Figure 3-2 V_{th} of RCAT and S-Fin with different recess etch depth

3.5 Fin Width and Fin Height Variaiton

For three-dimension fully-depleted fin structure, the fin width and fin height are important factors for the performance.

Figure 3-4 shows the threshold voltage and drain-induced barrier lowering (DIBL) characteristics versus fin width. Figure 3-5 is threshold voltage and drain-induced barrier lowering (DIBL) characteristics versus fin height. For devices with full-depleted (FD) channel, threshold voltage is mainly adjusted by fin width and fin height. As the fin width increases (Figure 3-4), the control of side-gate decreases, which causes the degradation of DIBL. As the fin height increases (Figure 3-5), the

control of top-gate decreases, which also causes the degradation of DIBL. The saddle fin structure shows a good DIBL behavior even though fin height, fin width, and recess depth change.

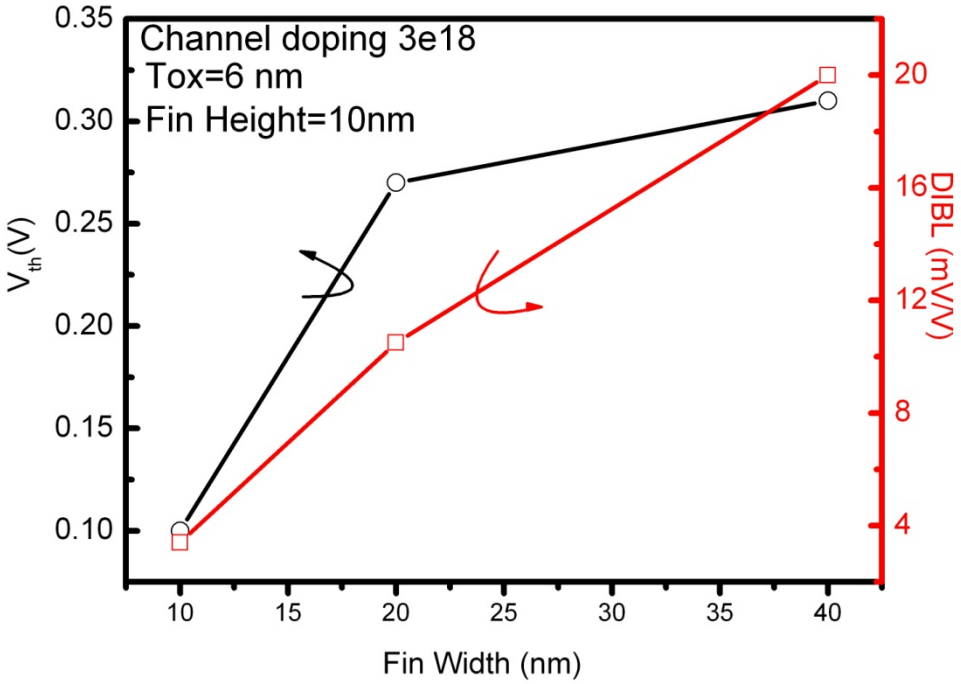

Figure 3-3 V_{th} and DIBL characteristics v.s the fin width.

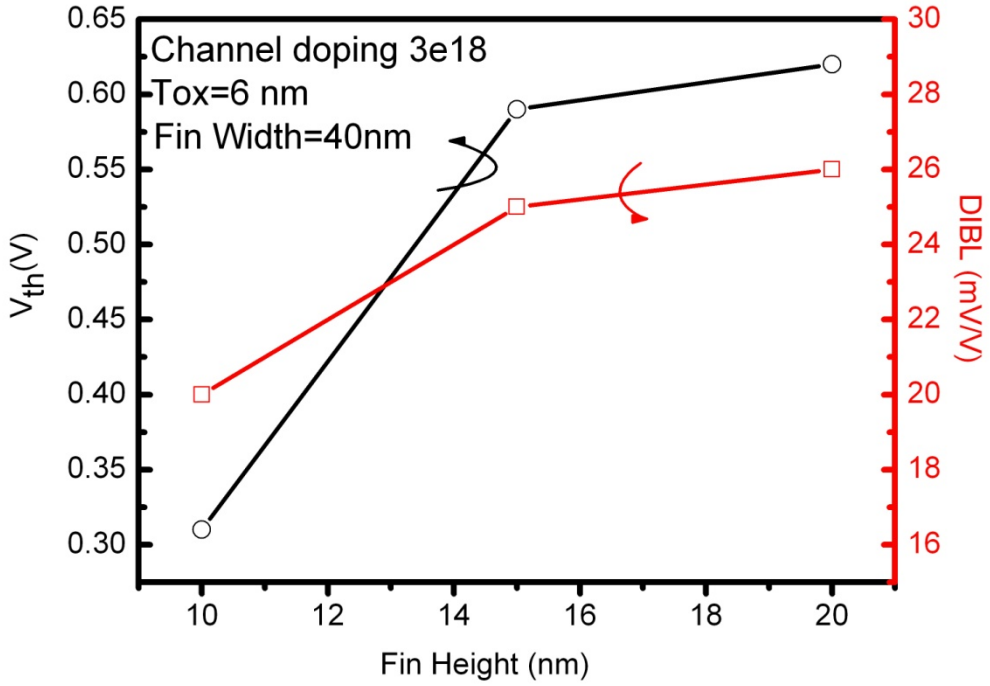

Figure 3-4 V_{th} and DIBL characteristics v.s the fin height.

3.6 Bulk FinFET Reverse Body Bias

3.6.1 Introduction

This reverse body bias is conventionally used to prevent any forward bias of the source-body junction due to circuit noise on the bitline or body, which could cause injected electrons from the source to diffuse to a capacitor node diffusion.

3.6.2 Threshold Voltage Variation With Reverse Body Bias

Figure 3-6 body bias dependency of RCAT and S-Fin cell array transistor. From the figure, the body-tied S-Fin shows negligible body bias dependency compare to RCAT structure. The body bias of DRAM device has been used to increase the off state

performance of the cell transistor. On the contrary, it also increases the junction leakage current of the storage node. Therefore, it is a great advantage that the body bias of S-Fin can be reduced without losing its performance.

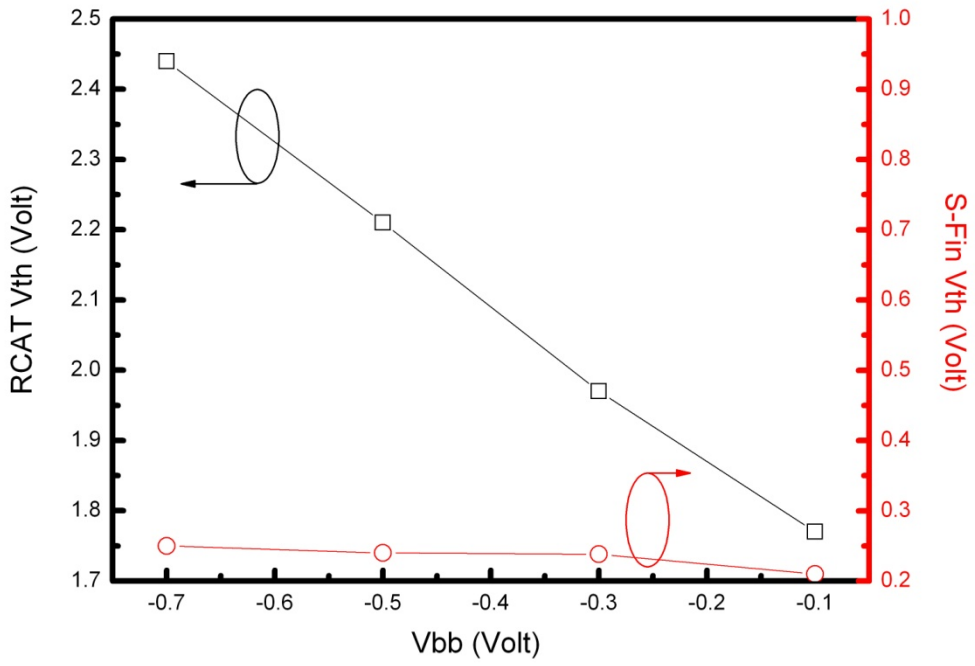

Figure 3-5 V_{th} of RCAT and S-Fin with different body bias.

3.6.3 DIBL Variation With Reverse Body Bias

Comparing to RCAT, DIBL of S-Fin is much less which shows a very good SCEs elimination. Also, from Figure 3-7, we see that the S-Fin is less sensitive in DIBL with body bias variation. To reduce the leakage, the reverse body bias should rise up. But that will also increase the SCEs in RCAT and degrade the DIBL. For S-Fin, the

DIBL is almost constant comparing to RCAT, which means it owns better potential to suppress the leakage without sacrifice too much control ability.

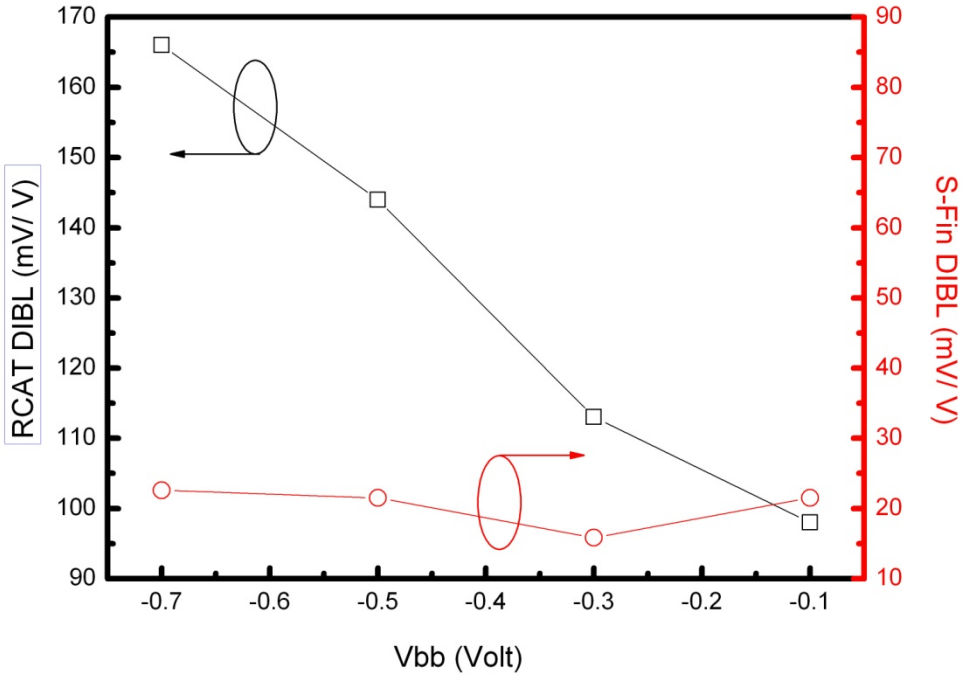

Figure 3-6 DIBL of RCAT and S-Fin with different body bias.

3.7 Reference

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Chapter 4

Leakage Analysis of Bulk FinFET

4.1 Introduction

The reduction of the leakage current of MOSFETs has become a important issue in the forth coming generation of devices. The leakage current will increase the consumption of power in logical circuit. In DRAMs technology, the requirement for leakage current is less than 1 fA/ per cell in order to maintain the charge state in capacity. There are two major leakage paths in the MOSFETs besides subthreshold leakage (Figure 4-1). One is the junction leakage current, which depends on the drain-to-bulk voltage. The other leakage current is generated in the vicinity of the surface of drain region when a high drain-to-gate voltage is applied. This gate induced drain leakage (GIDL), which has become one of the most crucial limitations on advanced devices, can even be larger than the channel off-current of long devices. Band-to-band-tunneling (BTBT) GIDL phenomenon has been considerably studied [1]–[6] and is now available in most state-of- art MOSFET simulation. Usually, the BTBT current become ignorable when the electric field is comparable to 1MV/cm. Under low electric field, it is trap-assisted tunneling (TAT) which dominate and is temperature dependent.

The carriers responsible for GIDL originate in the region of the drain that is overlapped by the gate, and GIDL occurs when the gate is set to zero or negative (nMOSFET) and the drain is at positive voltage. A large electric field then exists

across the oxide, which must be supported by the charge in the drain region. For nMOSFET, the tunneling will create holes in the forming depletion region as shown in Figure 4-2(b). However, as the holes (minority carriers) arrive the surface to form the inversion layer, they will immediately swept laterally to the substrate as shown in Figure 4-2(a). Hence, the depletion region under the oxide in the drain will not form the inversion layer but form a deep depletion layer.

Saddle-like bulk FinFET exhibits a large area of drain-to-gate overlapping region. It is 130-nm for junction depth in order to integrate with trench capacity. It is crucial to reduce the leakage generate in this region.

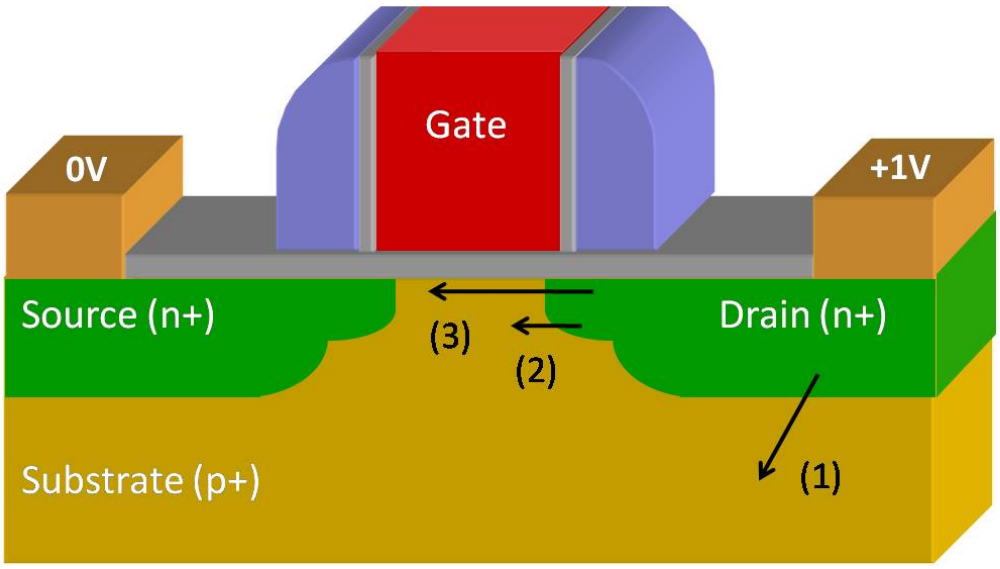

Figure 4-1 Conventional planar MOSFET leakage path (1) PN junction leakage (2) subthreshold leakage (3) GIDL

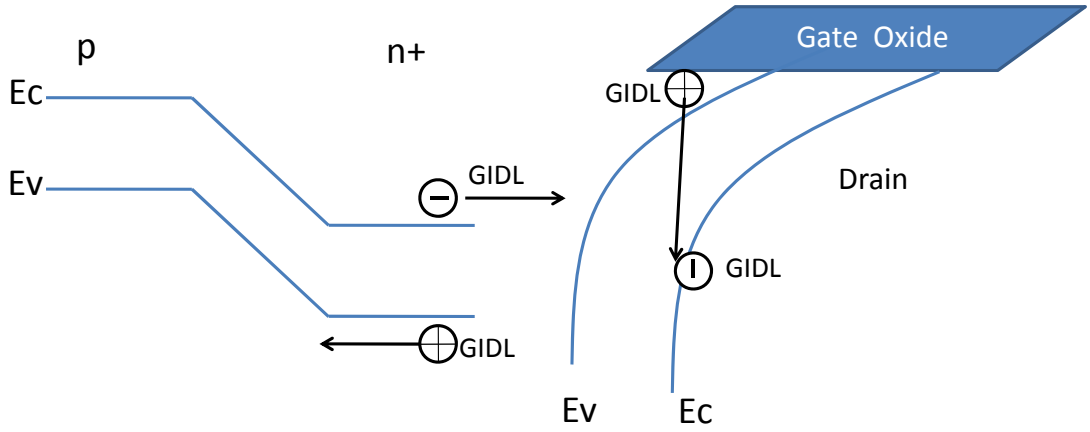

Figure 4-2(a) lateral band diagram Figure 4-2(b) gate-to-drain band diagram

4.2 GIDL and Junction Leakage

We turn on BTBT model in the drain region and the substrate below the drain region. For saddle-fin structure, junction leakage is inevitable when comparing to SOI structure. However, the junction leakage is much smaller than GIDL in our case due to the large overlap between gate and storage node

Figure 4-3 is the electric filed distribution and BTBT generation of saddle-fin structure. Due to the 10nm overlapping of side-gate and drain region, the electric field extends away from the interface of top-gate and drain region. That will also increase the BTBT current. Since the drain region is heavily n^+ doping (1e19 cm^{-3}~1e20 cm^{-3}), and substrate doping is 1e17 cm^{-3}, the depletion region would mostly drop in the substrate region. That means the p-n junction leakage can be induced mostly in the substrate region.

With little subthreshold leakage (by channel doping), we contribute the major leakages p-n junction leakage current and GIDL current. In Figure 4-4, we extract p-n junction leakage current from total BTBT current. In saddle-fin structure, the p-n junction leakage is two-order smaller than total BTBT current. That means, in

off-state, GIDL dominate the leakage current. To reduce the leakage effectively, we need to reduce the GIDL current.

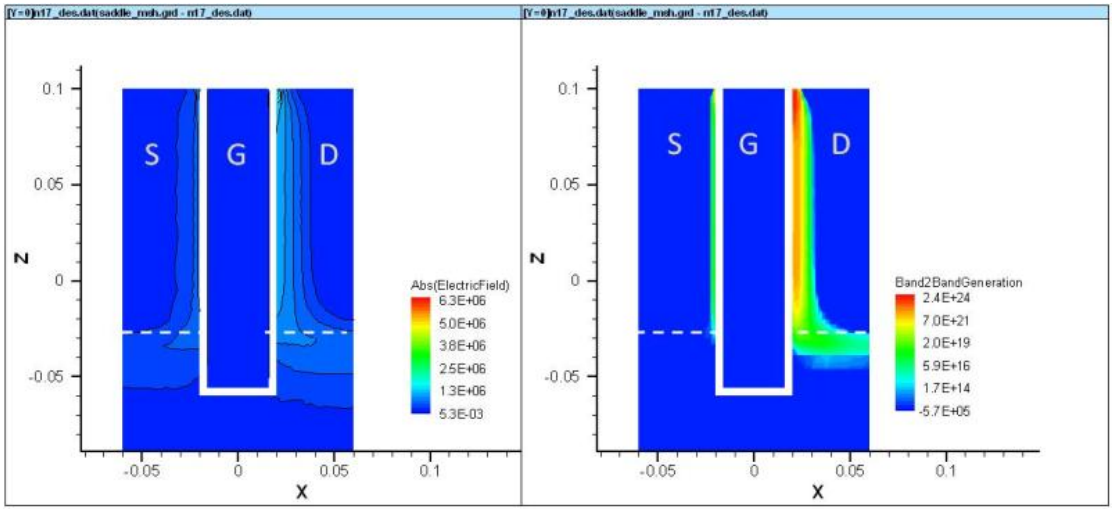

Figure 4-3 Field distribution and BTBT generation rate of saddle-fin structure.

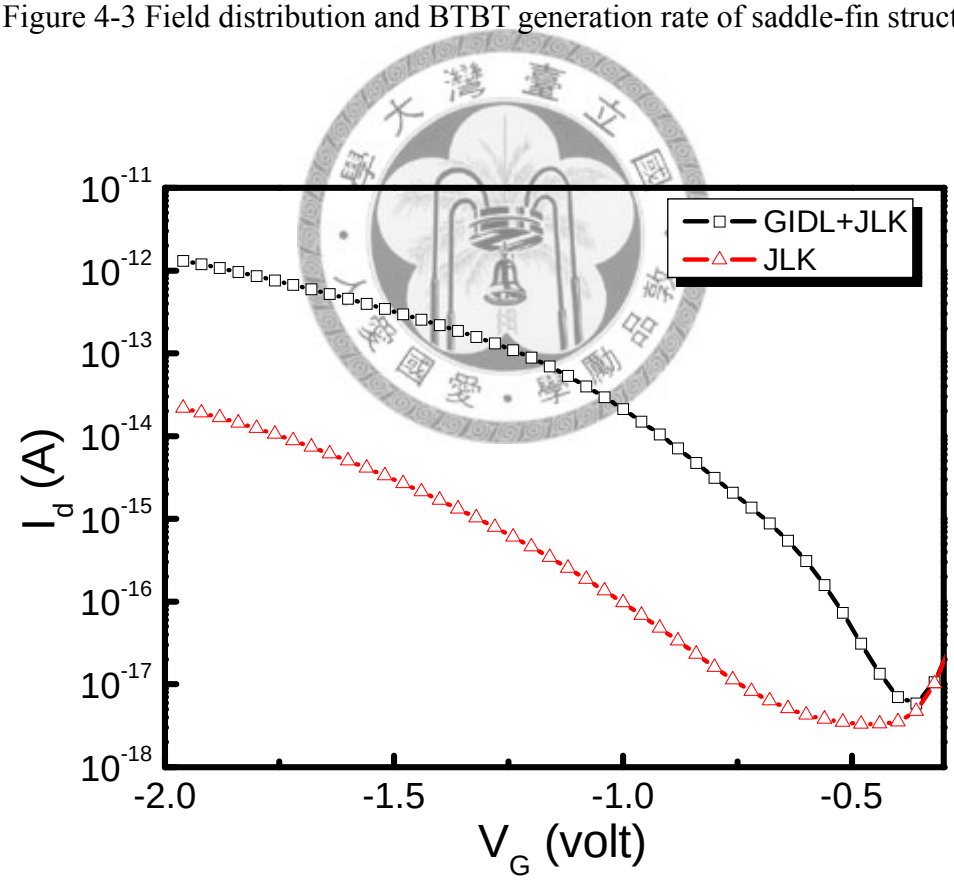

Figure 4-4 BTBT current v.s Vg. Junction leakage current (JLK) is extracted from total BTBT current.

4.3 Channel Doping

For substrate doping concentration 1e-17 cm^{-3}, the depletion length is about 100-nm. If the effective channel length is less than the depletion length, the device may punch-through under zero bias. It will increase the leakage current and degrade the DRAM cell retention time.

Figure 4-5 shows that, with 3e18 cm^{-3} channel doping, the leakage is 4X less than zero extra channel doping case(remaining 1e17 $cm^{-3)}$. The SS will improve due to less punch-through.

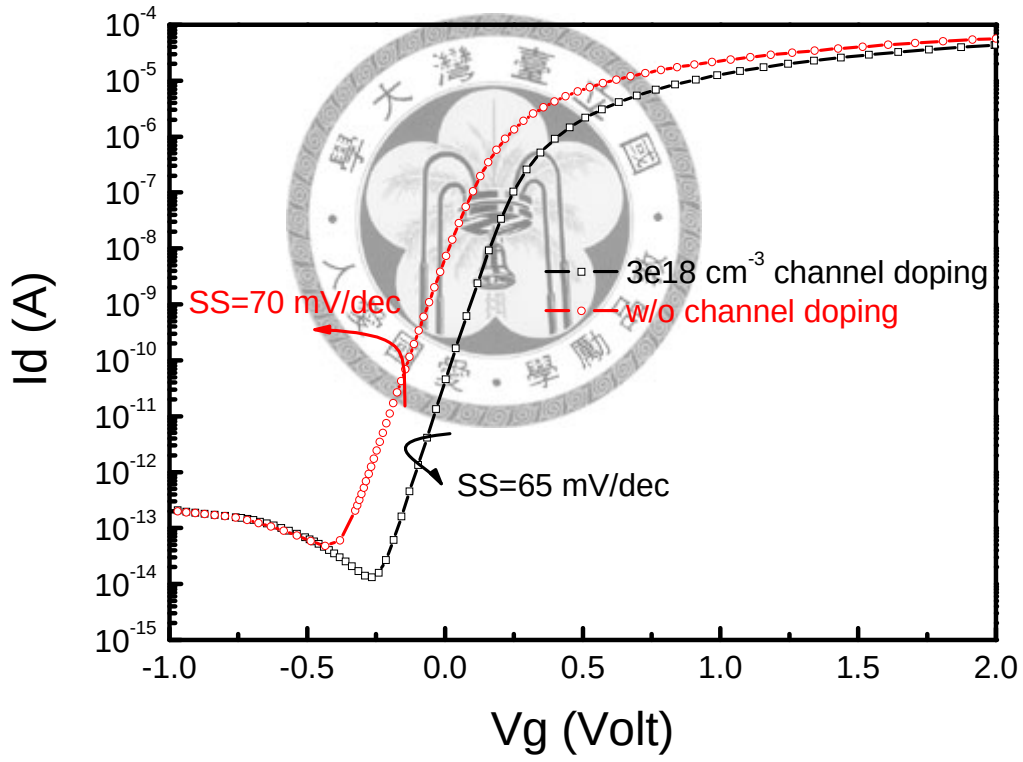

Figure 4-5 Id v.s Vg with and without channel doping

4.4 Lateral and Vertical LDD Doping

Figure 4-6 show 2-D prolife of key transistor region. For Figure 4-6(a), LDD doping profiles with a peak at the top of S/D region and gradually down (Z-direction), which is vertical doping in Z-direction. The doping distribution is from 7e19 cm^{-3} to 1e17 cm^{-3} within 130-nm. For Figure 4-6(b), LDD doping profiles with minimum at the interface of gate oxide and drain (X-direction). The doping distribution is from7e19 cm^{-3} to 7e18 cm^{-3} within 60-nm.For Figure 4-6(c), LDD doping profiles with minimum in the center of S/D region (Y-direction). The doping distribution is from7e19 cm^{-3} to 1e18 cm^{-3} within 20-nm.

From Figure 4-7, with LDD doping, it can reduce 10X leakage current under Vds=1V. For vertical doping in Z-direction, although it can also reduce the leakage, it suffers from smaller I_{on} when the others don't sacrifice too much I_{on}.

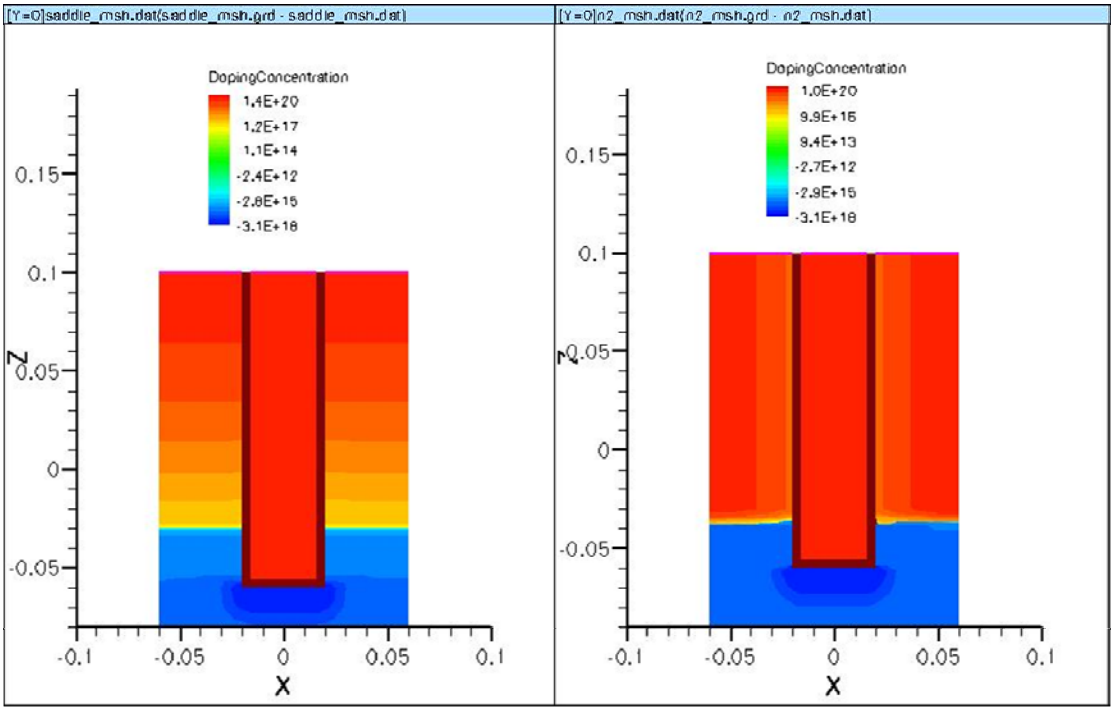

Figure 4-6(a) Vertical doping in Z-direction Figure 4-6(b) Lateral doping in X-direction

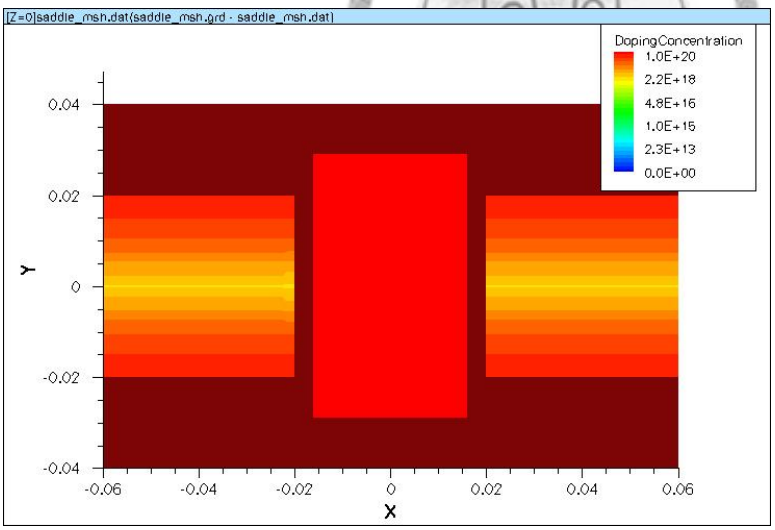

Figure 4-6(c) Lateral doping in Y-direction

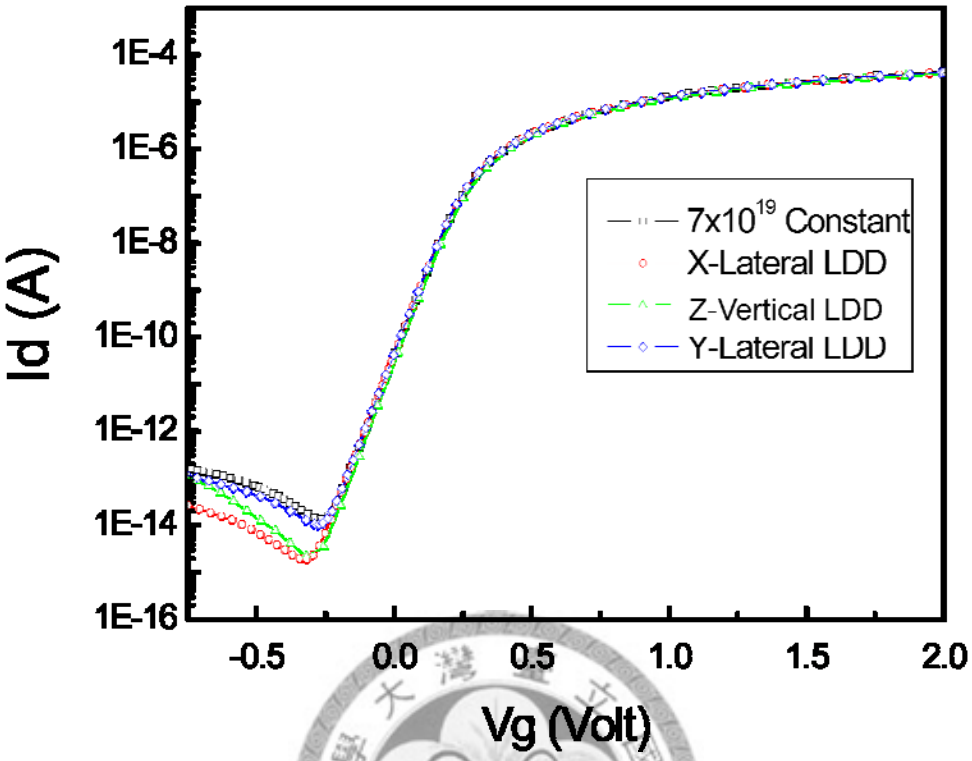

Figure 4-7 Id vs. Vg with different doping profile.

4.5 Tox thickness

To reduce the electric field is the most efficient way to reduce the BTBT current. The oxide thickness between gate and source/drain is set to be 4-nm,6-nm ,and 8-nm while the thickness of side-gate oxide remaining 4-nm. Figure 4-8, the I_{off} of 6-nm is almost 30x lower than I_{off} of 4-nm. For oxide thickness 8-nm, the I_{off} is with the same order of 6-nm. Both of the I_{off} (6-nm,8-nm) are met the requirement of less 1fA/cell for DRAMs. The subthreshold slope slightly degrade with oxide thickness (Figure 4-9).

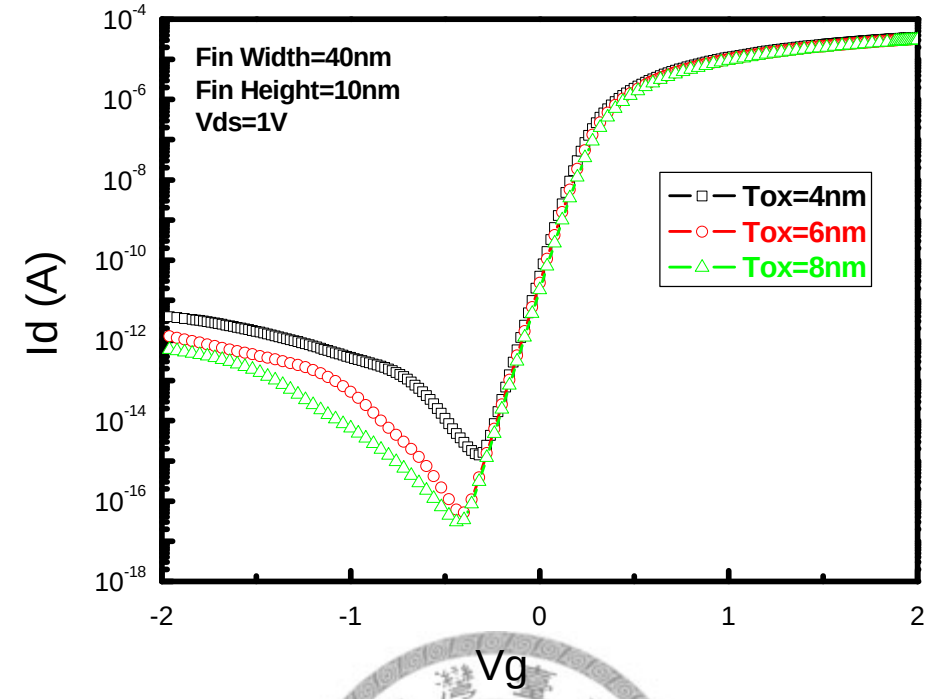

Figure 4-8 Id vs. Vg with different gate-drain oxide thickness.

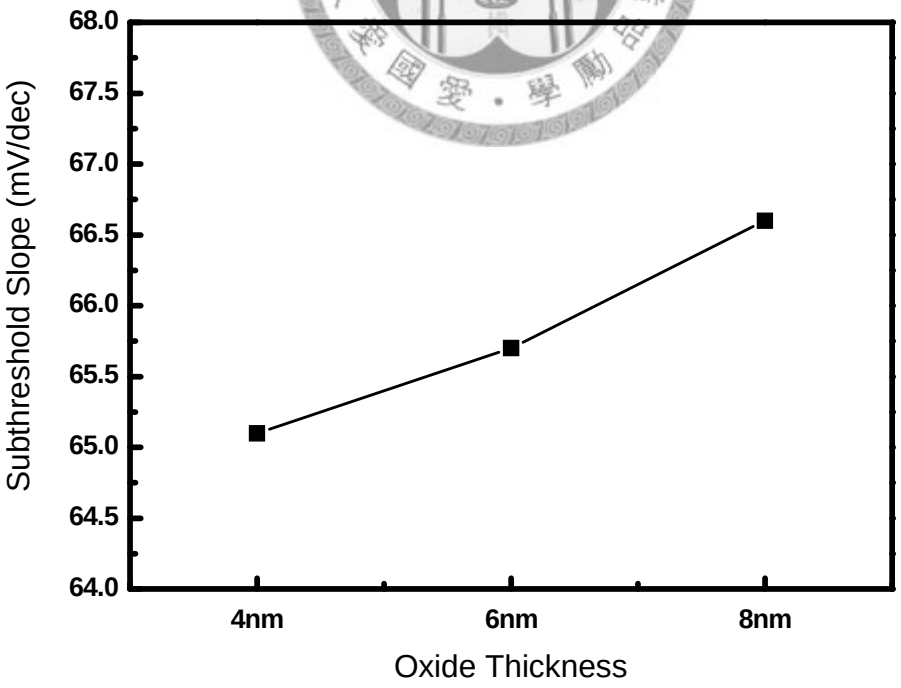

Figure 4-9 Subthreshold slope with different gate-drain oxide thickness.

4.6 Reference

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Chapter 5
Simulation Study of Heterojunction Effect on Ge Quantum Well pFETs

5.1 Introduction

5.1.1 Advantage of Germanium MOSFET

With the demand for higher drive current, the scaling of MOSFET devices keep proceed to get further improved performance. But for conventional Si-based MOSFETs, the scaling dimension is approaching its physical limits. It's time to seek for new materials which can integrate into the FET structure. As depicted in Table1.1, comparing to Si, MOSFETs on bulk germanium (Ge) substrate offer higher mobility for electrons and superior mobility for holes. Additional advantages of germanium include high density of states (DOS) in the conduction band and relatively simple integration with silicon. That all imply Ge MOSFET could be the potential candidate for high performance device application in the future [1].

Semiconductor	Mobility at 300K ($cm^2V^{-1}s^{-1}$)	
	electrons	holes
Si	1500	450
Ge	3900	1900
GaAs	8500	400

Table 5-1 Bulk mobility for Si, Ge, and GaAs at 300K [2]

5.1.2 Issues Of Germanium MOSFET

Although bulk Ge MOSFETs have already shown the potential for high performance MOS technology, its rare containment on earth and relative high cost still make the bulk Ge MOSFET application unreasonable. Moreover, as Table 1.2 shows, The narrow bandgap of germanium results in increased source-drain (S/D) junction leakage while its higher dielectric constant degrades electrostatic integrity. In addition, compared to Si, n-type dopants in germanium have lower solid solubility and diffuse rapidly, which make it difficult to achieve shallow junctions with sufficiently low sheet resistance.

Material	Si	Ge
Bandgap (eV)	1.12	0.66
Dielectric Constant (ε_0)	11.9	16

Table 5-2 Bandgap at 300K and dielectric constant of Si and Ge

Till now, the most practical and economical ways to implement a high mobility Ge layer would be to form an ultra-thin Ge-rich epi-layer on top of a Si substrate. Why?

Recently, the dual channel (strain-Si and strain-Ge) [3] and Ge channel [4] on relaxed SiGe buffer structures have proved significant electron and hole mobility enhancements, but it still suffer from the disadvantages of threading dislocation defect, rough surface, and high cost of the substrate. In contrast, the ultra-thin Ge epitaxially grown directly on Si with compressive strain has the advantages of high mobility, relatively low cost and compatibility with conventional CMOS process.

And, there is a serious problem affecting Ge MOSFET structure: Germanium oxide has long been known as more complex and less stable than silicon oxide. Germanium oxide exists in a number of stoichiometry (GeOx) and crystal structures (amorphous, hexagonal, tetragonal) which depend on oxidation conditions and processing history [5] [6]. And, germanium oxide commonly is a mixture of these various forms and inter-conversion is possible during processing or exposure to ambient conditions [7] [8]. Hexagonal and amorphous germanium oxides are water soluble while the tetragonal form is insoluble. Thus, it says that the Ge native oxide is very unstable and become the main impedance for Ge application. To overcome this issue, an ultra-thin Si-cap is grown on Ge quantum well to passivate the Ge surface. The Si-cap can be served as a passivation layer to facilitate further gate dielectrics growth. The Ge channel MOSFETs were then formed as this Si/epi-Ge/Si structure.

The strained Si, SiGe, and even pure strained Ge layer provide the carrier mobility

enhancement over bulk Si [9-12]. Furthermore, there are several advantages we can observe from the Si/epi-Ge/Si structure:

(1) The pure Ge channel can possess intrinsically high carrier mobilities and avoid alloy scattering (SiGe).

(2) The type-II band alignment between Ge and Si forms a deep quantum well for holes in the Ge channel and the channel is away from the oxide by the Si-cap spacing. Therefore, Coulomb and surface roughness scattering induced by the oxide surface are reduced.

(3) Compressive strain in the Ge channel will split the valence-band degeneracy and reduce the in-plane effective mass.

Those factors will further increase the hole mobility from the intrinsic Ge bulk hole mobility. Besides the advantage of high mobility of Ge pFETs, there is drawback we can't ignore. Germanium has both a narrower bandgap and smaller effective mass than silicon, which may easily induce BTBT current. Large band-to-band tunneling (BTBT) leakage currents can ultimately limit the scalability of Ge pFETs. In our simulation, we applied BTBT model and try to seek a way to reduce the leakage current.

5.2 Device Structure

Fig. 5-1 shows the device structure of the strained-Ge channel pMOSFET. The gate

length is ~90-nm with effective channel length is ~38-nm, the physical gate oxide is 1.2-nm, the Source/Drain depths is ~50-nm with extension depth is~20-nm, and the gate workfunction is set to be 4.15 eV. Due to a large valence band edge offset at the heterojunction between the unstrained Si and the Ge quantum well, the inversion carriers formed in the Ge quantum well. The holes of pFETs are confined in the Ge quantum well layer to form the buried channel, and the characteristics of the Ge quantum well pFETs vary from that of the conventional structure of Si MOSFETs.

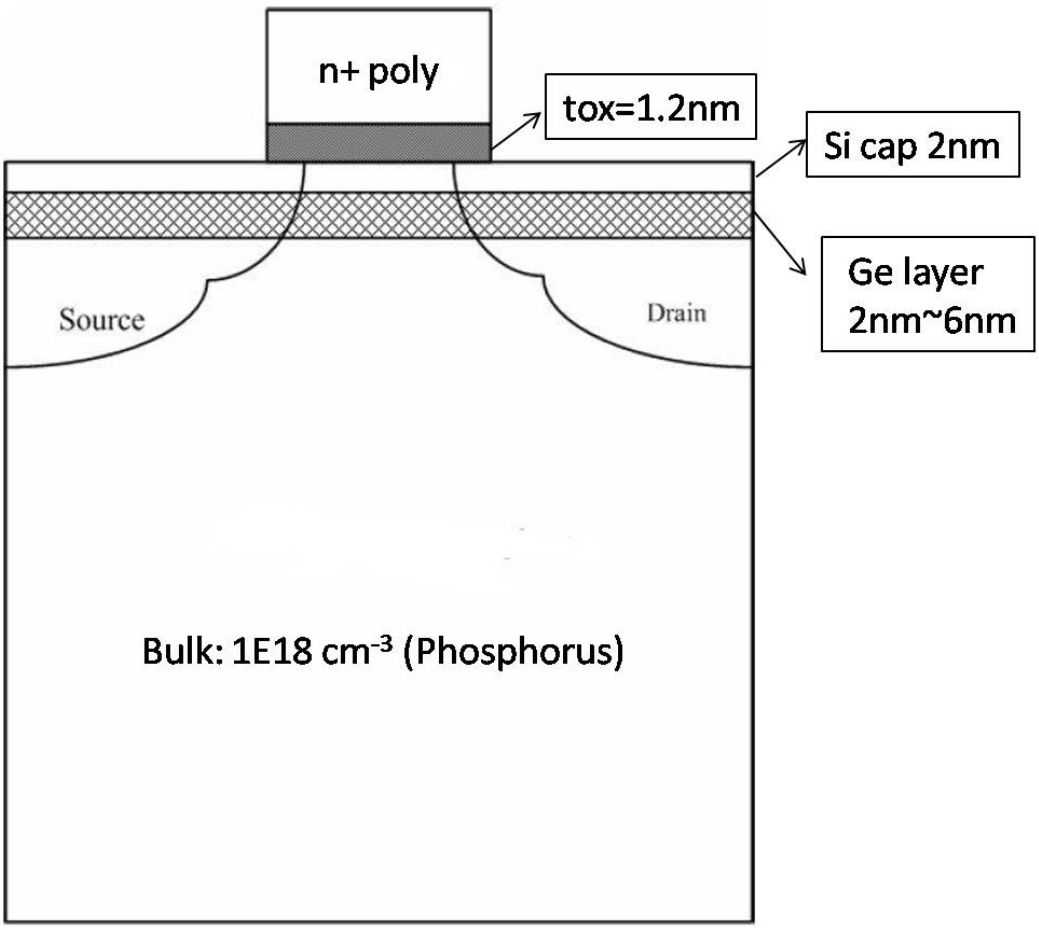


Figure 5-1 Ge pFET structure

For very short-channel MOSFET, more highly impurity doping region near the two ends of the channel are beneficial to the suppression of short-channel effect, since they help compensate charge-sharing effects from source-drain fields. For pMOSFET, this can be implemented by a moderate-dose n-type implant carried out together with the p^+ source-drain implant (Figure 5-2). We compare Si/Ge/Si device with control-Si by different doping profiles (w/ HALO and w/o HALO).

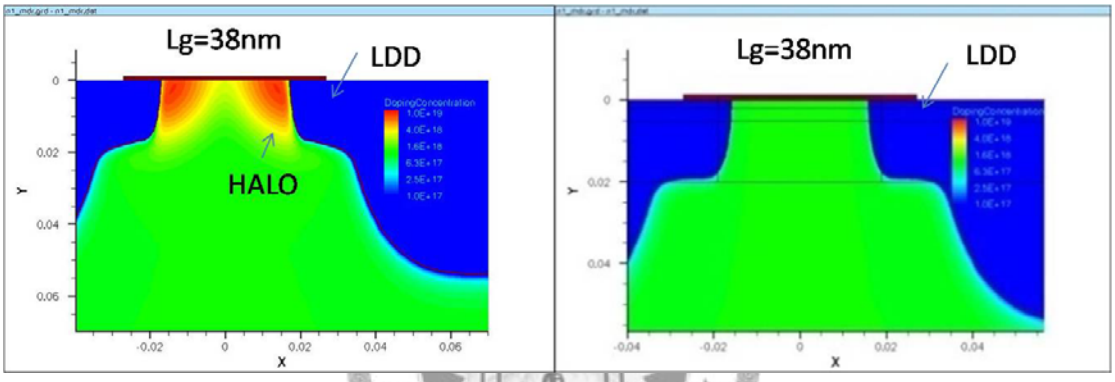


Figure 5-2 Doping profile of pFET with and without HALO profile

5.3 Physical Models and Parameters

All the device simulations for the Ge quantum well pFETs and control Si pFETs are carried out by DESSIS, a two-dimensional (2D) numerical device simulator. Because the lattice constants of the pure Si and Ge are mismatched by 4%, the strain effect has to be considered. The Ge layer is assumed to be fully compressively strained on Si substrate, and the Si-cap is thus unstrained. Due to the band offset between Si-cap/epi-Ge/Si substrate, the quantum Ge well forms, which leads to the Ge buried channel of pFETs. Because the device has a relatively thin oxide and high

level of channel doping, some physical dimensions of the pFETs (oxide thickness, Si-cap thickness and Ge quantum well thickness) have reached the quantum mechanical length scales. Therefore the wave nature of electrons and holes can no longer be neglected. We apply 1D Schroedinger model to simulate the quantum mechanical effect and analyze the impact of Si/Ge heterojunction on pFETs. Both the Si-cap and Ge quantum well thicknesses are critical issues in understanding and analyzing the characteristics of Ge pFETs.

For the pFETs investigated in the study, the Ge channel is assumed to be fully compressively strained on Si substrate, and the Si-cap is thus unstrained. This leads to the type II Si/Ge heterojunction between Si-cap and strained Ge. According the strain calculation, he band offset for △Ec is -0.19 eV and for △Ev is -0.76 eV. That makes the bandgap of Ge 0.55 eV (Figure 5-3).

We also consider the band-to-band-tunneling effect in Ge pFET. Due to smaller bandgap of Ge, it is assumed there is serious BTBT leakage current at off-state. Figure 5-4 shows that the experimental BTBT generation rate of Ge is much higher than Si. For Hurkx BTBT theoretical model:

$$G = -A \cdot D \cdot \left(\frac{F}{F_0}\right)^P \cdot \exp\left(-\frac{B \cdot E_g(T)^{1.5}}{E_g(300K)^{1.5} F}\right)$$

At T=300K, the F_0 is the key factor to determine the magnitude of BTBT generation rate. In Figure 5-5, F_0=6.4 MV/cm can fit the experimental data well. And F_0 of Si

is 22.5MV/cm as default in DESSIS.

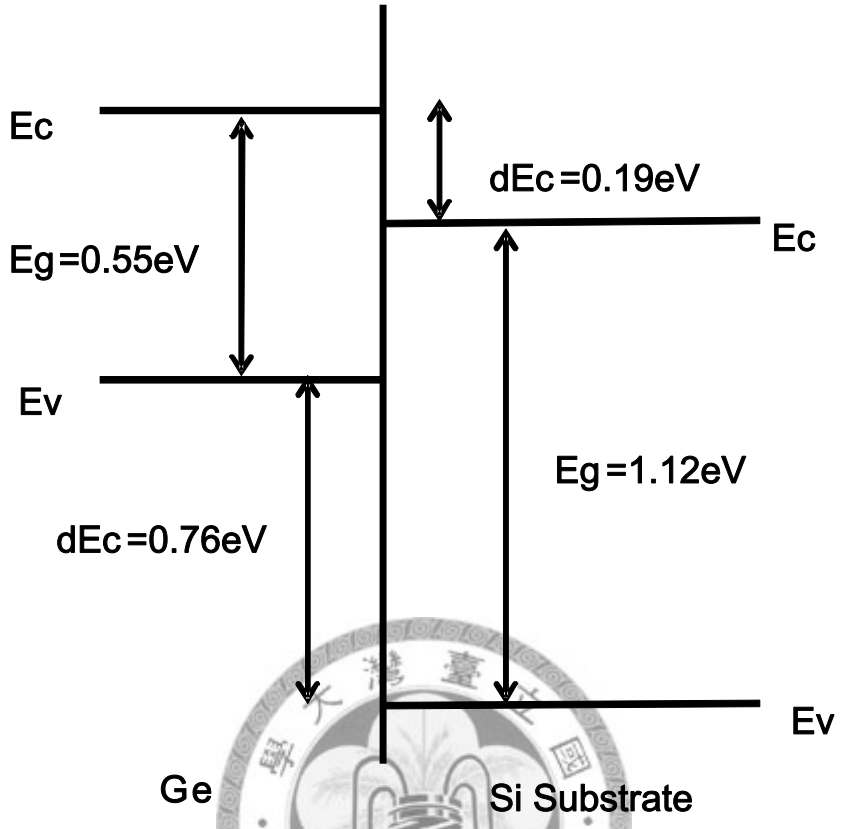


Figure 5-3 The schematic band alignment of Ge/Si substrate

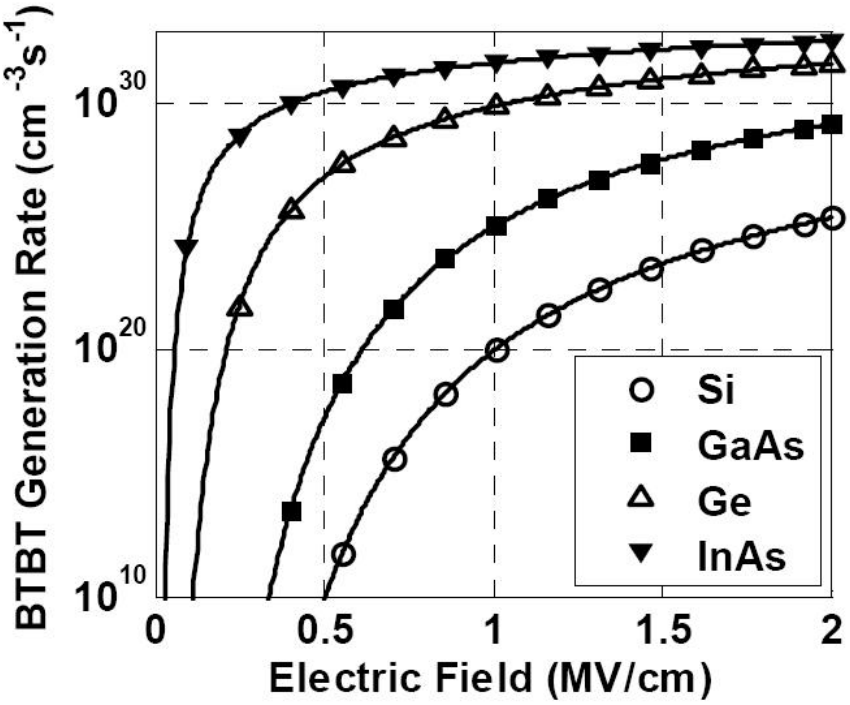


Figure 5-4 BTBT generation rate vs. Electric Field. Si (indirect) has

lowest BTBT rate while Ge (small bandgap & mass) is higher [13].

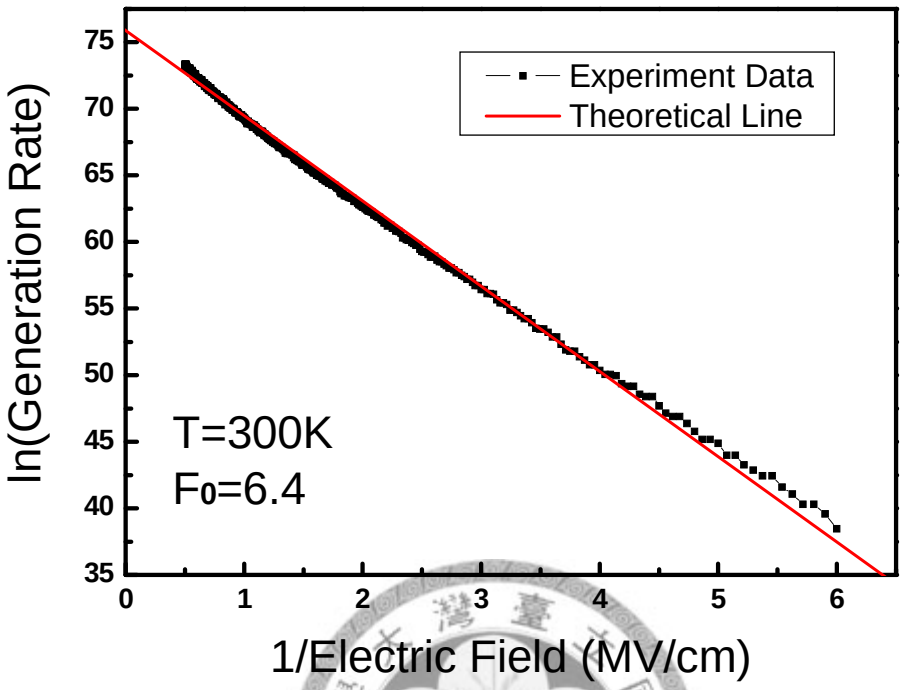


Figure 5-5 BTBT generation rate with inverse of electric field

5.4 Results And Discussion

5.4.1 Substhreshold Slope Modification of pFET

For short-channel device, increasing channel doping can help reduce SCEs. But at the same time, the high channel doping will increase the impurity scattering, which results in mobility degradation. A HALO implantation is applied to suppress the SCEs as mentioned previously. From Table 5-3, for control-Si without HALO will significantly degrade the substhrehold slope since the substrate doping is only 1e18 cm^{-3}. For substrate doping with this magnitude of order, the depletion length is about 33-nm. That means, without HALO implantation, the two ends of channel with 38-nm

gate length may punch through. But in Si/Ge/Si structure, the high hole concentration under 2-nm silicon cap play a role to maintain a good substhrehold slope without HALO implantation.

Lg =38nm pFET			
Device Structure	Doping Profile	w/o QM effect Subthreshold Slope [mV/decade]	w/ QM effect Subthreshold Slope [mV/decade]
Control-Si	w/ HALO	76	84
	w/o HALO	90	98
Si/Ge/Si 2nm Ge layer	w/ HALO	86	84
	w/o HALO	86	83

Table 5-3 Subthreshold slope comparison of control Si and Ge pFET under different doping profile.

The electron and hole concentration peak are at silicon-oxide interface under classical model. But if we apply quantum-mechanism model, the carrier concentration reach its maximum a little distance under silicon-oxide interface. And it goes to nearly zero at the interface due to boundary condition of wave function, as show in Figure 5-4. Thus, the effective gate oxide thickness is slightly larger than the physical thickness. This cause the decrease of Cox. As make the substhreshold-slope degradation for control-Si shown in Table 5-3. For Si/Ge/Si structure, the allowed

density of state in quantum well will reduce under quantum mechanism consideration (Figure 5-5). The lower carrier density confined in quantum well will slightly improve the substhreshold-slope and avoid the shift of peak position. In conclusion, the Ge well will provide higher concentration which can compensate the charge-sharing effect. For small gate length, it can benefit from the Si/Ge/Si structure which can replace the HALO implantment.

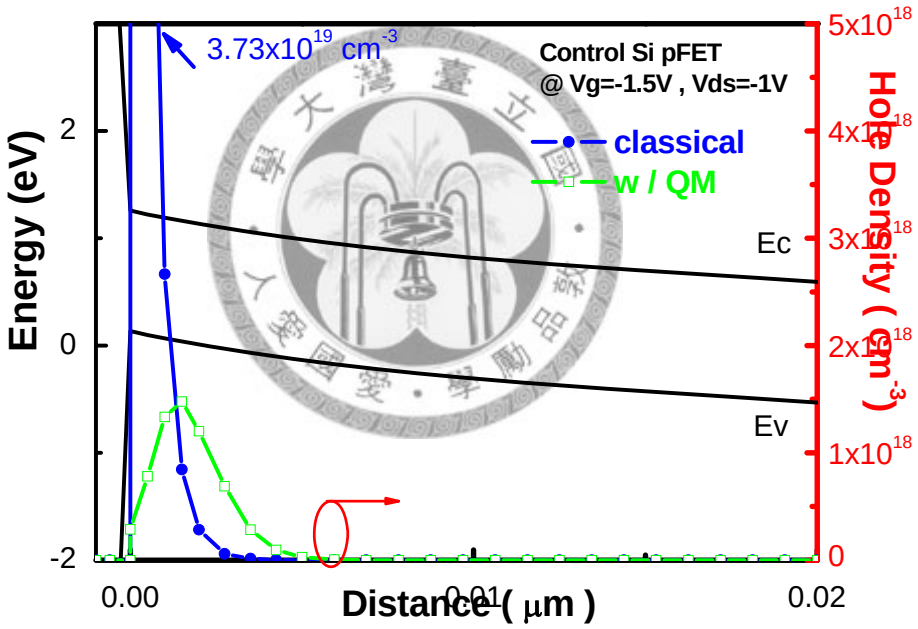


Figure 5-6 Hole density distribution of control-Si device

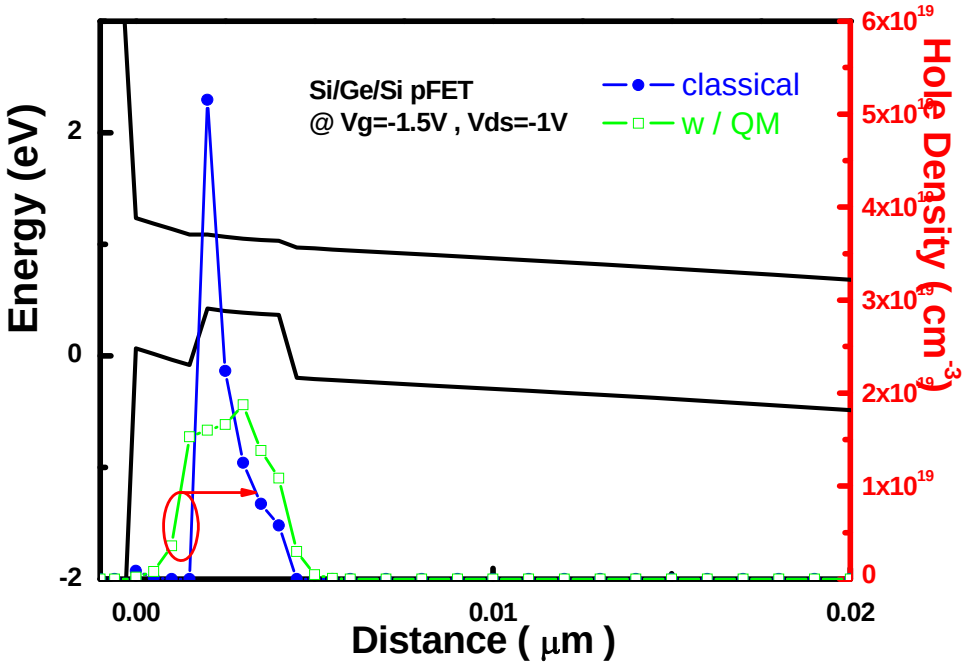


Figure 5-7 Hole density distribution of Ge pFET device

5.4.2 Cap Thickness Variation

Influence of Si-cap layer thickness on Ge pFET are depicted in Figure 5-8. It is observed that the leakage current increases as the Si-cap becomes thicker. The simulation is first assumed there is no BTBT model. Figure 5-9 explains the correlation between the leakage current and the Si-cap layer thickness. At off state , if the Si-cap layer thickness is thicker, the valence band at the heterojunction will be closer to the Fermi level, that is, there are more holes at the Ge channel with thicker Si-cap thickness. On the other side, the thinner Si-cap layer thickness shows that the valence band at the heterojunction is far away from the Fermi level with fewer holes at the Ge channel. As a result, without BTBT model, the thicker Si-cap cause lager off-state current.

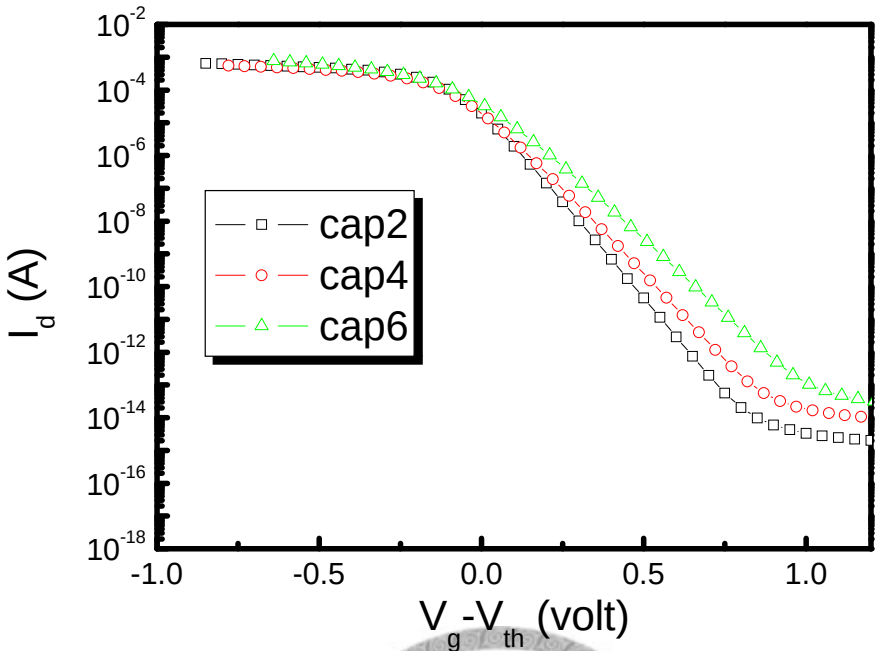
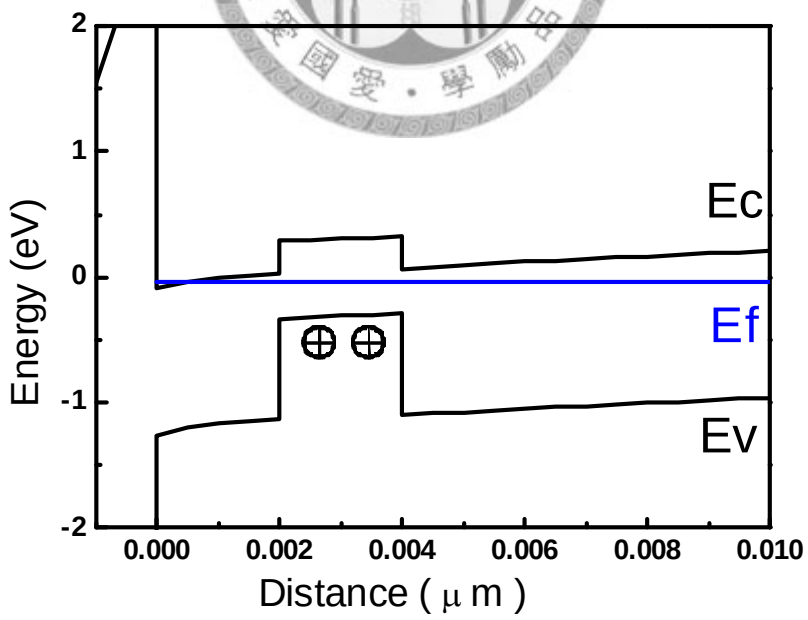
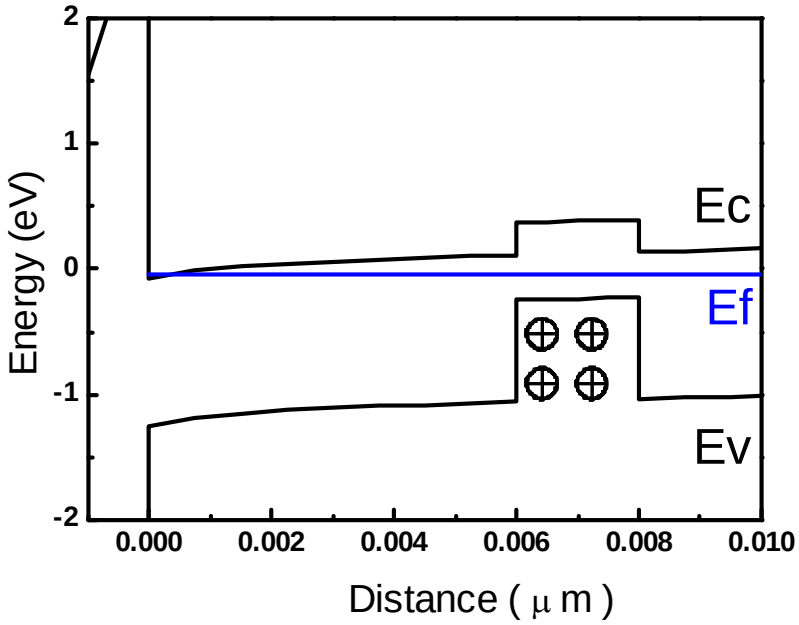


Figure 5-8 The normalized current characteristics of Ge pFET with different cap thickness without BTBT model



(a)



(b)

Figure 5-9 Band diagrams for the heterostructure of (a) thinner Si-cap (b) thicker Si-cap, showing more holes are confined in Ge QW for thicker Si-cap

Moreover, for thicker Si-cap, the Ge quantum well confines less holes and thus the Vth moves toward more negative voltage for 2-nm Ge layer pFET, which is shown in Figure 5-10. But by considering the BTBT model in these device simulations, we find that increasing the thickness of silicon cap will decrease the leakage current. The result is contrast to non-BTBT simulation. For BTBT, it is highly related to the electric field. For thicker Si-cap, the maximum electric field in the Ge channel is smaller than the thinner Si-cap. As a result, the leakage current will be suppressed with the increasing of Si-cap thickness.

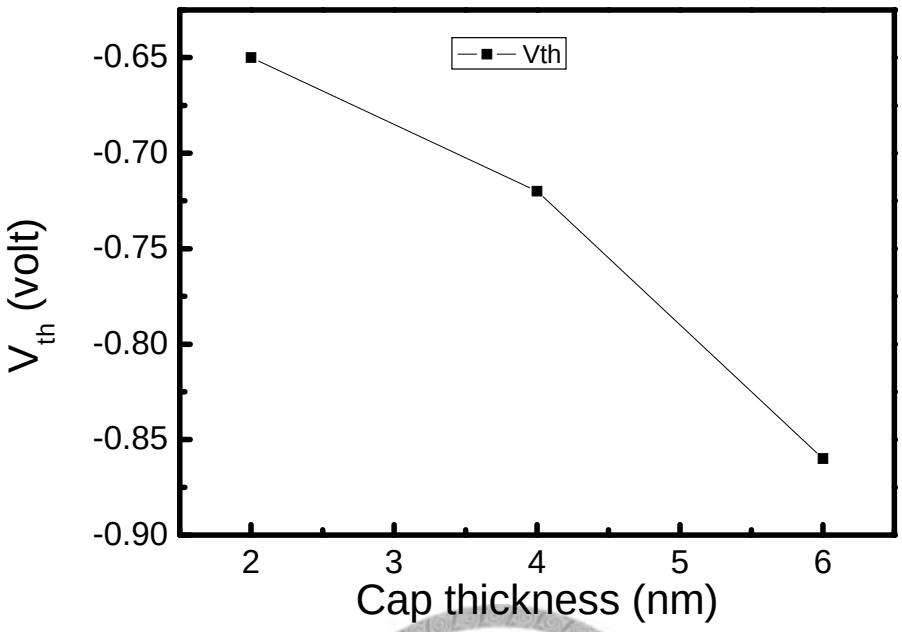


Figure 5-10 Vth variation with silicon cap thickness in Ge pFET at Vds=-0.05V. The thickness of Ge layer is fixed at 2nm.

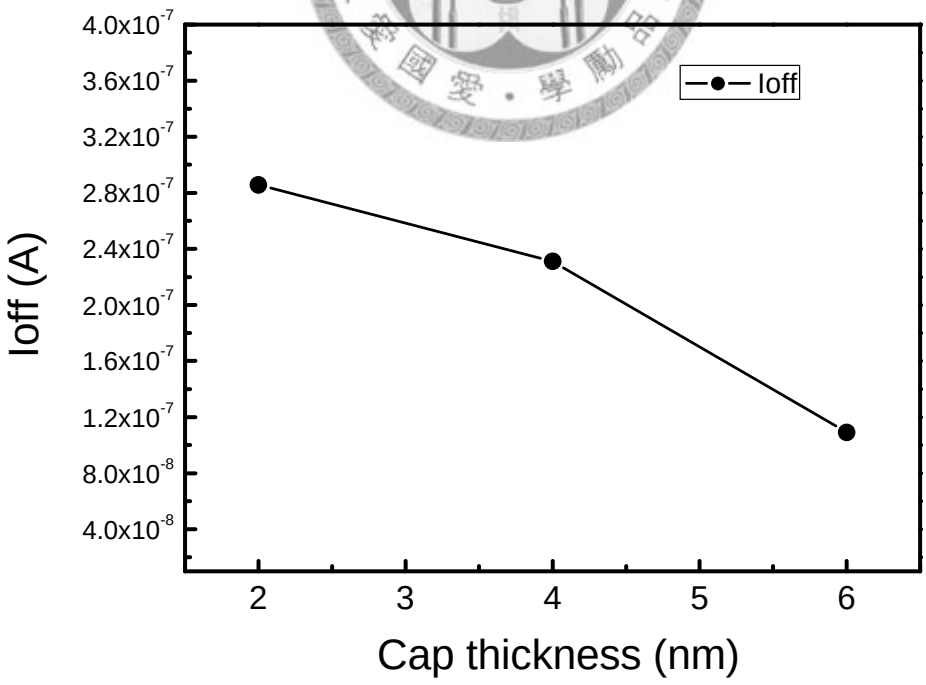


Figure 5-11 I_{off} variation with silicon cap thickness in Ge pFET at Vds=-0.05V.

5.4.3 Ge layer Thickness Variation

Another condition for Ge pFET is the fixed Si-cap with different Ge thickness. The smaller bandgap of Ge forms a quantum well between the Si-cap and the Si substrate. The energy states in the quantum well can be solved by the coupling of Schroedinger equation and Poisson equation through self-consistent process. From Figure 5-12, the narrower quantum well has higher energy level comparing to wider quantum well. The higher energy level increase the bandgap in the channel direction which will decrease the tunneling probability due to the larger forbidden path. Also, the narrower quantum well contains less available states, which means the quantized effect is more significant.

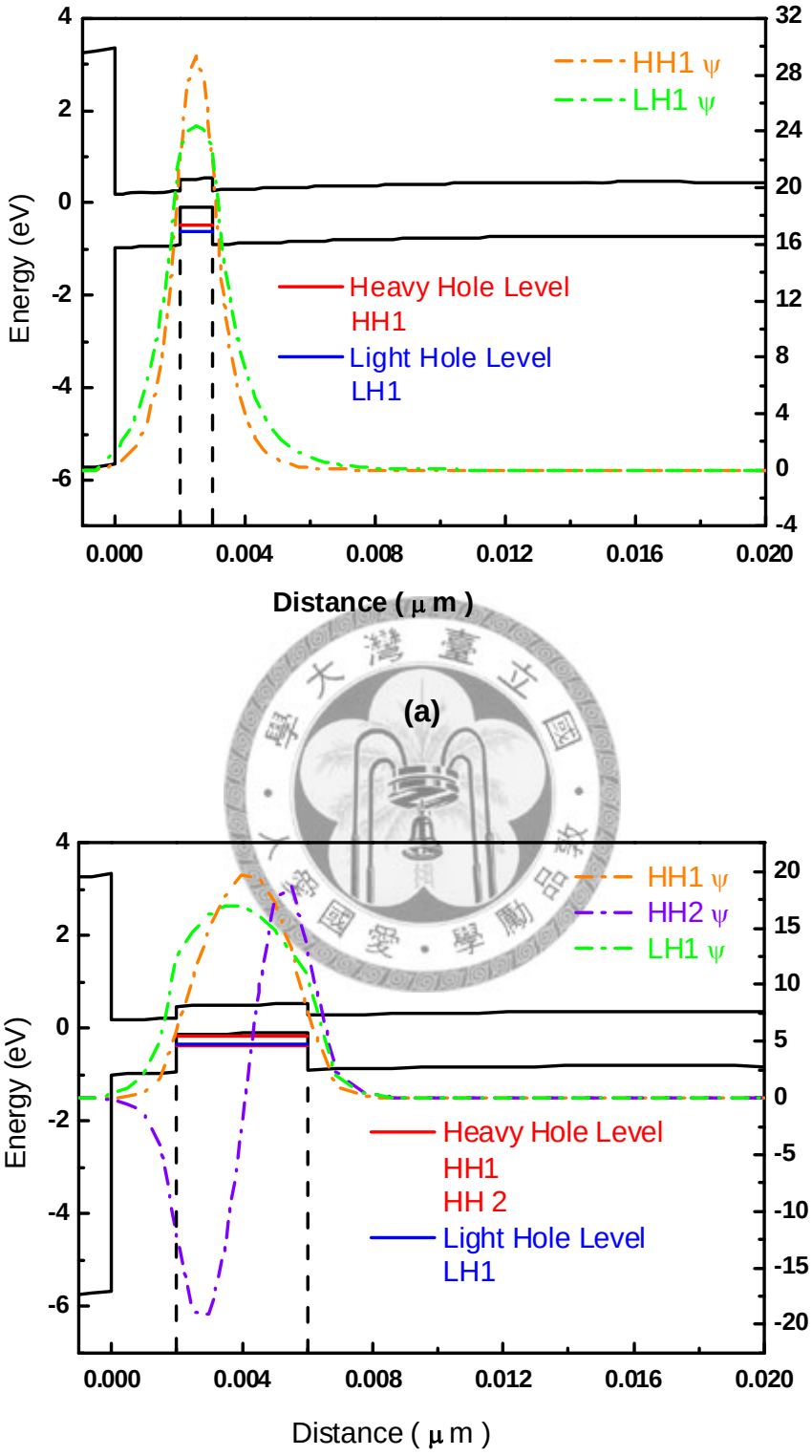


Figure 5-12 Energy level in Ge QW and corresponding wavefuntion for (a) 1nm (b) 4nm Ge thickness

As shown in Figure 5-13, the heterojunction Ge pFET can effectively suppress the BTBT leakage by more than three order of magnitude with small Ge layer thickness (1-nm). For thickness larger than 4-nm, it reveals large leakage but increasing slowly. For thickness smaller than 2-nm, the leakage can be effectively suppressed due to the quantum confinement.

In conclusion, there are three main factors dominate the leakage current under small Ge thickness (1-nm):

1. Smaller channel width
2. Less quantization states
3. Larger bandgap due to stronger quantization

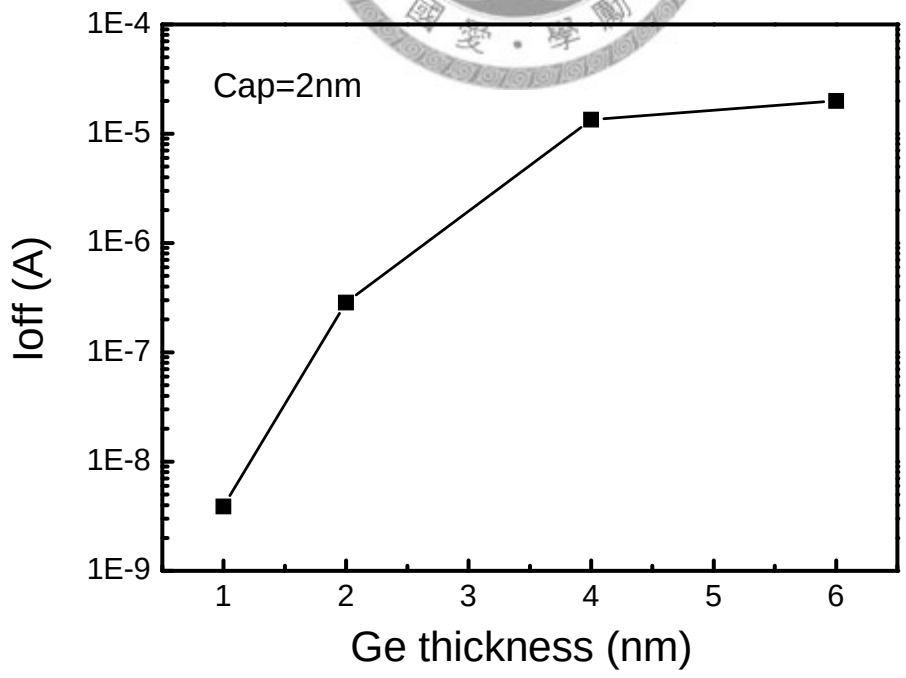


Figure 5-13 I_{off} variation with Ge layer thickness with fixed cap-2nm.

5.5 Reference

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Chapter 6
Conclusions

6.1 Summary

The research studied in the first part of this thesis focuses on the novel 3D bulk(body-tied) FinFET. TCAD tool [Synopsys Sentaurus TCAD Simulator] was used for all simulation works in this thesis. With the aid of TCAD, we show that the saddle-fin posses excellent control ability in sub-50nm region, which greatly reduce the SCEs. Also, comparing to the RCAT structure, the saddle-fin is less sensitive to the recess depth and the reverse body bias. The excellent I_{on}/I_{off} ratio is preferred by DRAMs. In our work, we assume that the bulk FinFET can first be implemented at the trench DRAM technology. To reduce the parasitic resistance of the buried-strap channel, the junction depth is 130-nm. The long junction depth induces a high GIDL current due to the large gate/drain overlapping. With lateral LDD doping profile on source/drain, it is proved that the GIDL can be reduced without too much I_{on} degradation. Morever, the GIDL current can be further suppressed by increasing the thickness of gate-drain oxide.

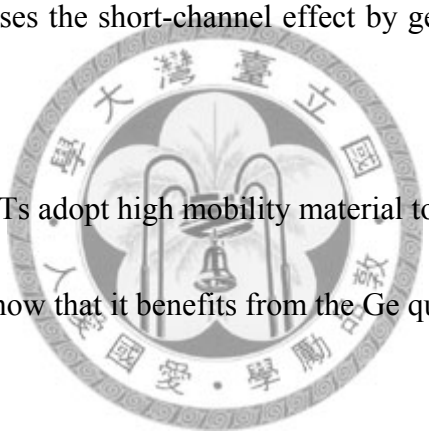
The second part of the thesis is the pFET with Si/Ge/Si structure. The higher hole mobility make it suitable for future high-performance devices. But the smaller

bandgap will induce higher BTBT leakage current in off-state. With shrinking the thickness of Ge layer, substhrehold slope and the leakage current decrease. For the 38-nm device, which corresponds to 90-nm technology node, we show that the Ge layer can substitute for HALO implantation due to the high hole density confined in the Ge quantum well.

For the task to find the suitable design rule of devices, we try to approach it in the following two ways:

(1) The saddle-fin eases the short-channel effect by geometrically extending the channel into trench.

(2) The Si/Ge/Si pFETs adopt high mobility material to increase the performance and we show that it benefits from the Ge quantum well structure.



6.2 Future Work

In the simulation of device structure and material modification, several terms are worth further investigation:

1. Although the saddle-fin exhibits good electrical properties, such as low DIBL and SS, there are some emergent issues need to be solved. One of the main challenges in bringing FinFETs into manufacturing is the difficulty to reduce the series resistance. The use of thin silicon channels in devices and FinFETs needed for control of SCE

implies that these devices suffer from severe series resistance. As the scaling down of effective channel length, it becomes more worse. While the use of raised source/drain technology can reduce the resistance of the extension region, and wrapped-around-contact technology eventually should be developed to enhance the performance of the devices.

2. The strained Ge can be integrated with new device structures such as SOI and double gate MOSFETs. By incorporating strained Ge into SOI or double gate devices, enhanced device performance is expected with better short channel effects and scalability. However, these variations of the device structure and material require more theoretical work in order to understand the carrier transport, such as phonon scattering, surface roughness scattering, Coulomb scattering, etc. Moreover, to identify the position where BTBT happens will help us to scheme a method to suppress the leakage in the future.