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COLLEGE OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

NATIONAL TAIWAN UNIVERSITY

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應用於外差式雷射干涉儀訊號之數位介面設計

A NEW DESIGN OF DIGITAL INTERFACE FOR

HETERODYNE LASER INTERFEROMETER SIGNALS

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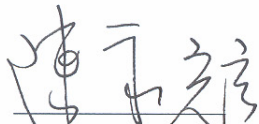
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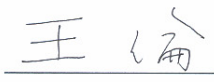
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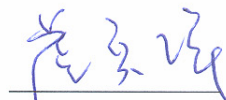
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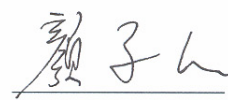
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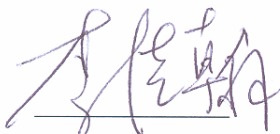

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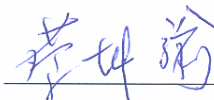

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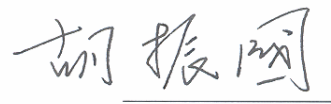
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中文摘要

由於對工具機及半導體步進機台精準度的嚴格要求日以遽增，相對來說對位移感測器的要求日漸增加，雷射干涉儀是普遍用於位移量測的系統，其具有長距離的量測範圍和低於奈米尺度的位移解析度。

在不同形式的雷射干涉儀中，外差式雷射干涉儀將光源等同於一個頻率的載波，並將其用於偵測由移動的平台所產生的都普勒頻率與其對載波產生的頻率調變，這項優點使外差式的雷射干涉儀相對於傳統的干涉儀不管是對外界環境或校正誤差所產生的干擾都會有較好的抵抗力。

在這篇論文中首先會以邁克森雷射干涉儀作為開頭，接著介紹單調光雷射干涉儀與外差式雷射干涉儀。在來介紹過去文獻中提出的幾種外差式雷射干涉儀介面，以及此論文所提出的改良式的數位架構，最後將以邏輯閘的模擬和 FPGA 的驗證作為本篇論文的結束。

關鍵字: 外差式干涉法，相位量測，數位相位計，雷射量測系統，位移量測。

Abstract

Due to the rigorous demand on the precision of the manufacturing tools or the lithography stepper, the request of the position sensor is also rigid. The laser interferometer is the commonly used in the long range positioning system, and with the sub-nanometer resolution.

In the laser interferometers, the heterodyne laser provides the light as frequency carriers and catches the Doppler frequency from the moving stages in FM (frequency modulation) mode. This benefit makes the heterodyne have good endurance to the misalignment or other environment noise.

In this thesis, the first begins with the introduction of Michelson interferometer, the homodyne interferometer, and the heterodyne type. The following are the prior digital interfaces designed for the heterodyne laser interferometer, and the new modified digital interface and architecture is proposed in this thesis. Finally, the gate-level simulation and the FPGA verification are presented in the end of this thesis.

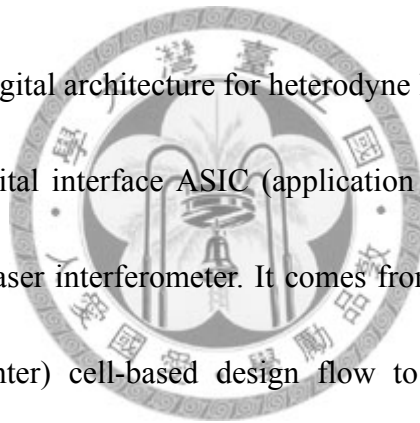
Keywords: heterodyne interferometry, phase measurement, digital phasemeter, laser measurement systems, displacement measurement

Statement of Contributions

General Contributions

The following are substantial achievements although not my original contributions.

1. Deliver a measurement system consisting of a Agilent N1231A interferometer measurement board and a real time operating system implemented with Mathworks xPC Target. It acquires the position data precisely for real-time measurement.
2. Deliver an overall digital architecture for heterodyne laser interferometer.
3. Deliver a initial digital interface ASIC (application specific integrated circuit) design for Agilent laser interferometer. It comes from following the CIC (Chip Implementation Center) cell-based design flow to the gate-level simulation without DFT insertion.
4. The above digital interface guarantees 10 nm displacement resolutions under the pseudo measurement signal testing.



Original Contributions

The original contributions are as follow.

1. A new phase interpolation method for rising timing resolution is proposed. It achieves 0.6 nm under on-chip testing.
2. A counter glitches canceling method is proposed and passes the verification on gate-level simulation and FPGA on-chip testing.



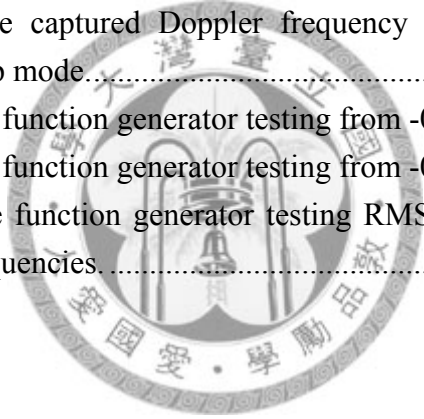
Contents

誌謝.....	I
中文摘要.....	II
<i>Abstract</i>	III
<i>Statement of Contributions</i>	IV
<i>Contents</i>	VI
<i>List of Figures</i>	VII
<i>List of Tables</i>	IX
<i>Chapter 1 Introduction</i>	1
1.1 Servo Control System.....	1
1.2 Michelson Interferometer.....	2
1.3 Homodyne Laser Interferometer.....	4
1.4 Heterodyne Laser Interferometer.....	8
1.5 Homodyne and Heterodyne Comparison.....	11
<i>Chapter 2 Electronics of Heterodyne Laser Interferometer</i>	14
2.1 Basic Operation.....	14
2.2 Delay Line Interpolator.....	16
2.3 Two-way Frequency-Conversion.....	18
2.4 Vernier Scale.....	21
<i>Chapter 3 Architecture</i>	24
3.1 Octonary Phase Interpolation.....	24
3.2 Data path of Integer Part Calculation.....	25
3.3 Multiplexer Determination.....	27
3.4 Minimum Sorter Determination.....	29
3.5 Metastability and Displacement Resolution Discussion.....	31
3.6 Method comparison.....	33
3.7 Gate Level Simulation on TSMC 0.18 μm Design Kits.....	34
<i>Chapter 4 FPGA Verification</i>	42
4.1 Architecture Adapted for Cyclone III.....	42
4.2 Gate-level Simulation and On-chip Testing.....	43
4.3 Optical System and Function Generator Testing.....	52
<i>Chapter 5 Conclusion and Future work</i>	59
<i>References</i>	60

List of Figures

Figure 1.1 Servo Control Diagram.....	1
Figure 1.2 Schematics of Michelson Interferometer.....	2
Figure 1.3 Relationship of Phase Difference and Irradiance.	4
Figure 1.4 Schematics of Homodyne Interferometer (Courtesy of Spindler and Hoyer Inc.)	5
Figure 1.5 A simple signal processing circuit for homodyne interferometer.	8
Figure 1.6 Schematics of Homodyne Interferometer.....	9
Figure 1.7 Schematics of Heterodyne Interferometer (Courtesy of Spindler and Hoyer Inc.)	11
Figure 1.8 Effect on homodyne misalignment.....	13
Figure 2.1 Basic Phase Estimation diagram.	15
Figure 2.2 The block diagram of Zygo delay line interpolator.	16
Figure 2.3 The operation diagram of Zygo delay line interpolator.....	17
Figure 2.4 Frequency conversion diagram.....	18
Figure 2.5 Two-way frequency conversion diagram.	19
Figure 2.6 Phasemeters selection diagram.....	20
Figure 2.7 Mechanical Vernier Scale.....	20
Figure 2.8 The operation of Vernier scale method.....	21
Figure 3.1 The operation of Octonary phase interpolation.	24
Figure 3.2 Fractional Part Determination.	25
Figure 3.3 The control unit of the Integer part calculation.	25
Figure 3.4 The save and reset timing diagram of the control unit.	26
Figure 3.5 The integral parts counts change unstably.....	27
Figure 3.6 A counter module with save-and-reset control unit.....	27
Figure 3.7 count registers' relationship with the fractional part value.....	28
Figure 3.8 Schematic of multiplexer determination.	29
Figure 3.9 Schematic of minimum sorter determination	30
Figure 3.10 Overall Architecture of the circuits.	31
Figure 3.11 The probable determined phase location when the timing violation occurs.....	32
Figure 3.12 Gate-level Simulation in typical model.....	38
Figure 3.13 The details of the gate-level simulation results from 3D.7 to 39.3.....	39
Figure 3.14 The details of the gate-level simulation results from 39.3 to 36.0.	

.....	40
Figure 3.15 (a) The gate-level simulation in fast model. (b) Gate-level simulation in slow model.....	41
Figure 4.1 Architecture adapted for Cyclone III FPGA.....	42
Figure 4.2 Gate-level Simulation on Cyclone III library.....	46
Figure 4.3 Testing diagram in Cyclone III FPGA.....	47
Figure 4.4 Diagram of SignalTap II Analyzer	47
Figure 4.5 Testing the target mirror moves away from the interferometer. .	48
Figure 4.6 Testing the target mirror moves close to the interferometer.	49
Figure 4.7 RMSE comparison of the displacement difference in 11 different Doppler frequencies.....	51
Figure 4.8 The optical setup and the troubles in heterodyne laser source. .	52
Figure 4.9 The measured Doppler frequency when the target is stopped...	53
Figure 4.10 The Doppler frequency result in a moving stage.....	54
Figure 4.11 The diagram of the function generator testing.....	55
Figure 4.12 The captured Doppler frequency in the function generator sweep mode.....	56
Figure 4.13 The function generator testing from -0.32 MHz to 0.8 MHz ...	57
Figure 4.14 The function generator testing from -0.8 MHz to -0.48 MHz..	58
Figure 4.15 The function generator testing RMSE in 11 different Doppler frequencies.....	58



List of Tables

Table 3.1 Comparison of Heterodyne Electronics	34
Table 3.2 Testbench for gate-level simulation on TSMC 0.18 μm design kits.	36
Table 3.3 Signal names for gate-level simulation on TSMC cell library.....	37
Table 4.1 Gate-level Simulation Environment for Cyclone III FPGA	43
Table 4.2 Signal names for reference phasemeter on Cyclone III gate-level simulation.....	44



Chapter 1

Introduction

1.1 Servo Control System

In the past few years, computer numerical control machine has grown up rapidly. The critical request to the information of position and velocity also grows up. Under this framework, a high-precision discrete-time servo-mechanical system needs a sensor to measure both position and velocity of the position stage in a real-time manner. Most of sensors are realized as optical ruler or laser interferometer. The laser interferometer has a benefit on long-range and high-resolution. This thesis chooses the laser interferometer as a basis and develops electronic techniques to deal with the stage position in high resolution and velocity tolerance.

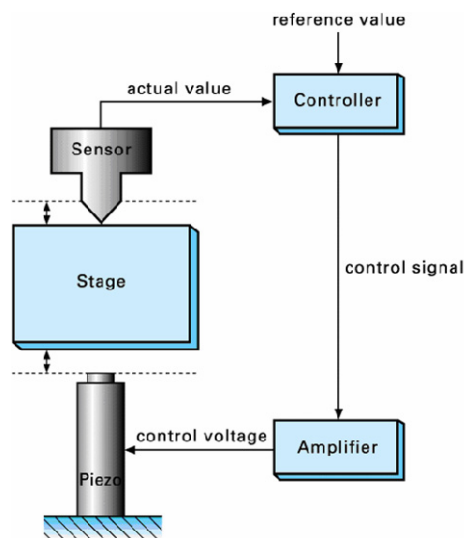


Figure 1.1 Servo Control Diagram [1]

1.2 Michelson Interferometer

The basic and original concept of interferometers comes from Michelson interferometer, which is shown in Figure 1.2. The coherent He-Ne Laser is incident onto the non-polarized beam splitter and split into two light (1) and (2) which have equal intense beam.

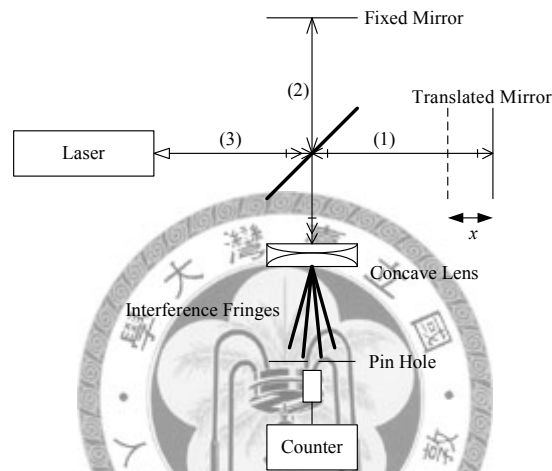


Figure 1.2 Schematics of Michelson Interferometer [2]

The beam (2) hit the mirror which is fixed and the beam (1) hit the mirror which translates with the stage or object under measured. The beam splitter combines the reflection of them and redirects them into a concave lens. If we consider beam (1) and beam (2) in time domain [3]:

$$\begin{aligned} E_1 &= E_0 \cos(\omega t) \\ E_2 &= E_0 \cos(\omega t + \theta(t)) \end{aligned}, \text{ where } E_0 \text{ is the wave amplitude of both beam (1) and beam (2).} \quad (1.1)$$

Then combine them as:

$$\begin{aligned} E &= E_0 \cos(\omega t) + E_0 \cos(\omega t + \theta(t)) \\ &= 2E_0 \cos\left(\frac{1}{2}(2\omega t + \theta(t))\right) \times \cos\left(\frac{1}{2}\theta(t)\right) \end{aligned} \quad (1.2)$$

E has modulated amplitude as:

$$E = 2E_0 \cos\left(\frac{1}{2}\theta(t)\right) \quad (1.3)$$

And the intensity read by photo detector is the square of amplitude:

$$\begin{aligned} E^2 &= 4E_0^2 \cos^2\left(\frac{1}{2}\theta(t)\right) \\ &= 2E_0^2 \cos(\theta(t)) \end{aligned} \quad (1.4)$$

The path lengths x can be represented as:

$$x = \lambda \cdot \frac{\theta}{2\pi}, \text{ where } \lambda \text{ is the wavelength of laser source.} \quad (1.5)$$

The path differences between beam (1) and beam (2) induce the phase change in wave intensity, if the translated mirror continuously moves, the results behind the concave lens is an annular fringe pattern and the sinusoidal intensity variation is read by photo detector through the pinhole. The counter counts the integral multiples in bright and dark fringes for $\lambda/2$ position resolutions. The advanced signal processing technique in comparing relative phase through ADC achieves the resolution to $\lambda/512$ [4].

The thing that must pay attention is that the translated mirror must have a smooth movement to reduce the back and forth vibration. The Michelson interferometer can not afford acute back and forth vibration and will happen double counts of interference fringes. It also needs a fine linear bearing to release this problem. To deal with this issue and make the laser interferometry more unrestricted to environment or equipment, the following improvement by generating quadrature outputs of measurement signal is proposed and called homodyne laser interferometer.

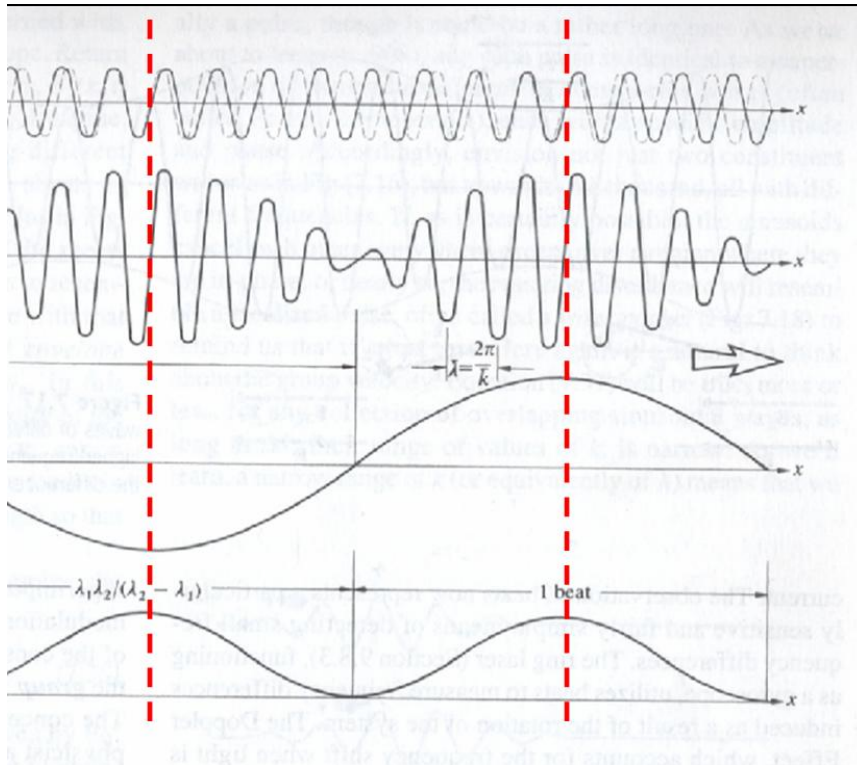


Figure 1.3 Relationship of Phase Difference and Irradiance [3].

The reflection off the both mirrors will be partially incident onto the active volume of laser source, as the beam (3) in Figure 1.2, the reflection may cause the external resonate in the laser source, modulating the laser power and wavelength, to cope with this problem, the corner cube mirror will be used to redirect the beam light and avoid the overlapping in the laser source.

1.3 Homodyne Laser Interferometer

The homodyne interferometer schematic is shown in Figure 1.4. [5] The output of laser source has been modified into the linear polarized beam and incident onto the polarizing beam splitter, as mentioned foregoing, the homodyne interferometer modify and rearrange the corner cube to replace the plane mirror in both fixed and translated mirror.

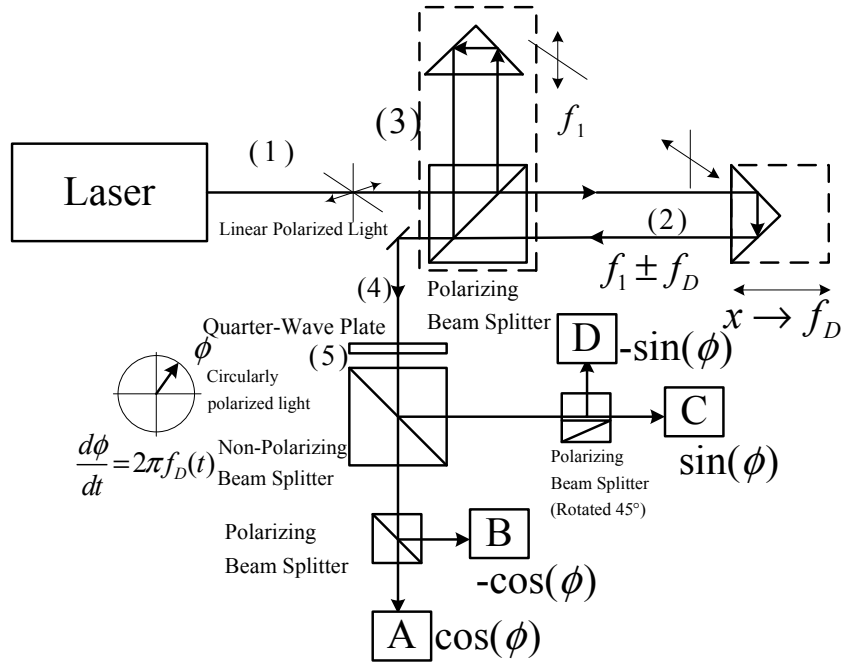


Figure 1.4 Schematics of Homodyne Interferometer (Courtesy of Spindler and Hoyer Inc.)

The beam (1) is 45° with respect to beam (2) and beam (3), the beam (3) is incident onto the fixed corner cube as the Michelson interferometer, and beam (2) is incident onto the translated mirror and carry out the frequency f_D modulated by Doppler effect, which quantity is [5]:

$$f_D = \frac{2}{\lambda_A} v, \quad \text{where } \lambda_A \text{ is the wavelength of laser source.} \quad (1.6)$$

Both beam (2) and beam (3) is recombined as beam (4) in the polarizing beam splitter and then redirected into the quarter-wave plate to transform into the circularly polarized light. This optical setup also avoids the interference light incident onto the laser source.

The optical setup before the beam (4) is very similar to Michelson interferometer, after here, the beam (4) pass through a quarter-wave plate with its 45° linear

polarization, then transform into the circular polarization, and make the beam (5) have 180° phase differences in x and y direction, this phenomenon is used to generate differential wave light for further purpose. The circularly polarized light has a phasor which angular velocity is $2\pi f_D$. The rotating phasor $\phi(t)$ is the main object to be detected. To achieve this goal, the beam (4) is transferred through a polarizing beam splitter and detected by photodetector A, the relationship between the laser intensity and the signal A can be shown as [5]:

$$I_A(t) = I_O(t) \frac{1}{4} [1 + \cos(\phi(t))]; \quad (1.7)$$

$$\phi(t) = \pm \arccos \left[\frac{4I_A(t)}{I_O(t)} - 1 \right]$$

The $I_A(t)$ is the intensity read from photodetector A, and the $I_O(t)$ is the intensity of laser, which should be noticed that can fluctuate with time. By this equation, one arccos value cause two $\phi(t)$ which have opposite sign. This sign ambiguity can be fixed by the quadrature signal generated from rotated 45° polarizing beam splitter.

$$I_C(t) = I_O(t) \frac{1}{4} [1 + \sin(\phi(t))]; \quad (1.8)$$

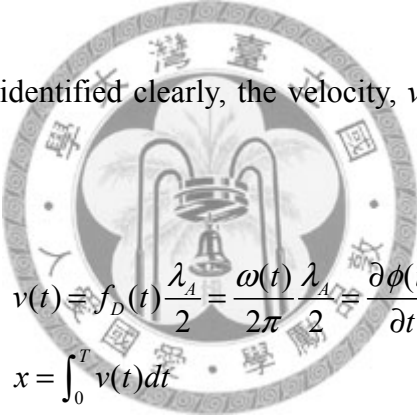
The added sin term of $\phi(t)$ helps classify the region $[-\pi/2, \pi/2]$, accompany the arccos function, which region is $[0, \pi]$, the phasor located within $[0, 2\pi)$ can be determined. For implement issues, the aging laser source and optical components may cause the intensity ambiguity in the zero-crossing of the interference fringes. This setup provides the complement signal of signal A and signal C as below:

$$I_B(t) = I_o(t) \frac{1}{4} [1 - \cos(\phi(t))]; \quad (1.9)$$

$$I_D(t) = I_o(t) \frac{1}{4} [1 - \sin(\phi(t))];$$

The beams which is incident to photodetector B and photodetector D comes from another polarized light which have 180° phase differences to the original light. The complementary signals can be regarded like differential signal pair represented as digital data or as square wave converting in Figure 1.5. No matter the processing of the complementary signals, it reduces the effects of intensity fluctuations on the phase measurement.

Since the $\phi(t)$ can be identified clearly, the velocity, v , and displacement, x , can be calculated as below:



$$v(t) = f_D(t) \frac{\lambda_A}{2} = \frac{\omega(t)}{2\pi} \frac{\lambda_A}{2} = \frac{\partial \phi(t)}{\partial t} \frac{\lambda_A}{4\pi} \quad (1.10)$$

$$x = \int_0^T v(t) dt$$

Note that the displacement x is measured up to time T .

Here shows a simple processing method deal with the homodyne interferometer. In Figure 1.5 [7], the signals B and A are sent to a comparator and results the high/low level voltage, so do signals C and D. The subtracting action reduces the ambiguity of fringe contrast in zero-crossing, this low fringe contrast can appear from vibration, interferometer mis-alignment and unequal in the non-polarizing beam splitter [5]. The signal E and signal F are the outcome of two comparators, the signal E is the clock of

counter accumulate the register every positive edge trigger, and the signal F is the up/down sign bit, when the signal E trigger, the bit F appears low, that means the displacement x is moving forward. Otherwise, if the bit F appears high when the signal E rising trigger, it means the reflector is translating backward. This method is exquisite that combines both the optical phenomenon and digital techniques.

For further resolution, the xor operation can be applied to signals E and F to induce double frequency, in this manner, the up/down sign bit must be attached to E&F signal to occur a correct indicate. The more digital interpolation method is proposed [6].

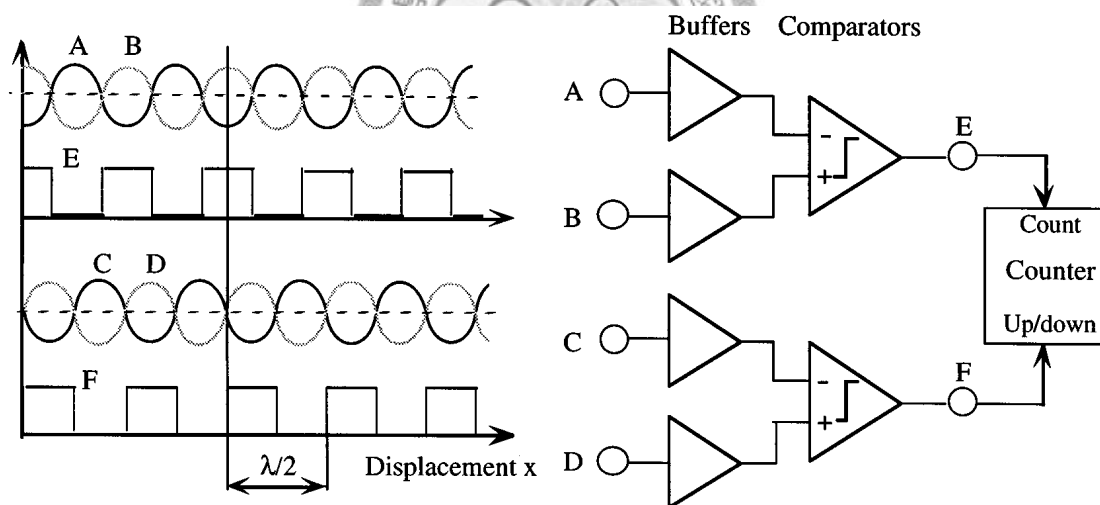


Figure 1.5 A simple signal processing circuit for homodyne interferometer.

1.4 Heterodyne Laser Interferometer

The heterodyne laser source generates the different frequency by several ways, and two well-known manners are longitudinal Zeeman effect or acoustic optical

modulation (AOM) device [9].

As shown in equation (1.4), the photodetector amplitude is a cosine function of phase differences $\theta(t)$ between reference and measurement beam. The heterodyne can be viewed as a frequency shift in $\theta(t)$:

$$\theta(t) = 2\pi \cdot (f_2 - f_1)t + \theta'(t) \quad (1.11)$$

Figure 1.6 [11] elaborates more clearly on heterodyne operation; the $f_2 - f_1$ frequency oscillates in a fixed frequency when the reflector stops ideally.

The react Doppler frequency δf from moving reflector makes the beat frequency shifting. What the digital interface that resolves the heterodyne operation needs to do is detecting every cycle's frequency as precise as it can. To accumulate the detected frequency and substrates the reference one can produce the phase $\theta'(t)$ that the phase difference results from the moving reflector.

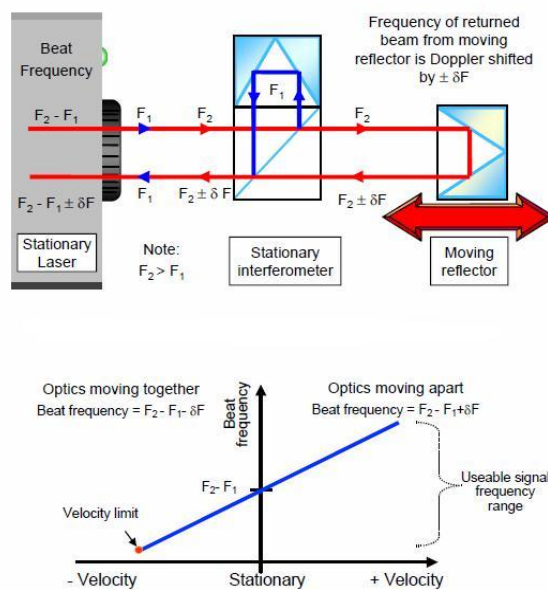
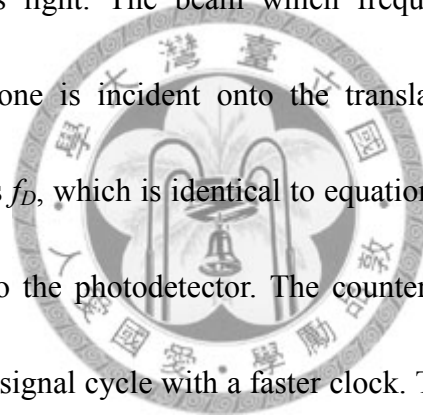


Figure 1.6 Schematics of Homodyne Interferometer

Heterodyne laser source outputs two frequency beams f_1 , f_2 , with circular polarization as shown in Figure 1.7 [5], after passing through quarter-wave plate and transforming into orthogonal polarized mode, the combinational two frequency wave is incident onto a non-polarizing beam splitter for beam (1) and beam (2). Beam (1) is directly incident onto a photodetector and feed through into a digital counter which counts the cycle in one period of reference beam. Beam (2) carry on two frequency with x and y direction polarization respectively. The polarizing beam-splitter separates two different frequencies light. The beam which frequency is f_2 enters a fixed reflector, and the other one is incident onto the translated reflector, the induced Doppler frequency here is f_D , which is identical to equation (1.6). Two beams overlap at beam (4) and feed into the photodetector. The counter counts and calculates the time in one measurement signal cycle with a faster clock. The clock speed determines the minimal timing resolution essentially. After both counters count reference and measurement period respectively, the digital interface subtracts the measurement value from the reference one. The difference can represent the phase variance in this cycle. Accumulating the phase variance continuously, the displacement change can be observed apparently.



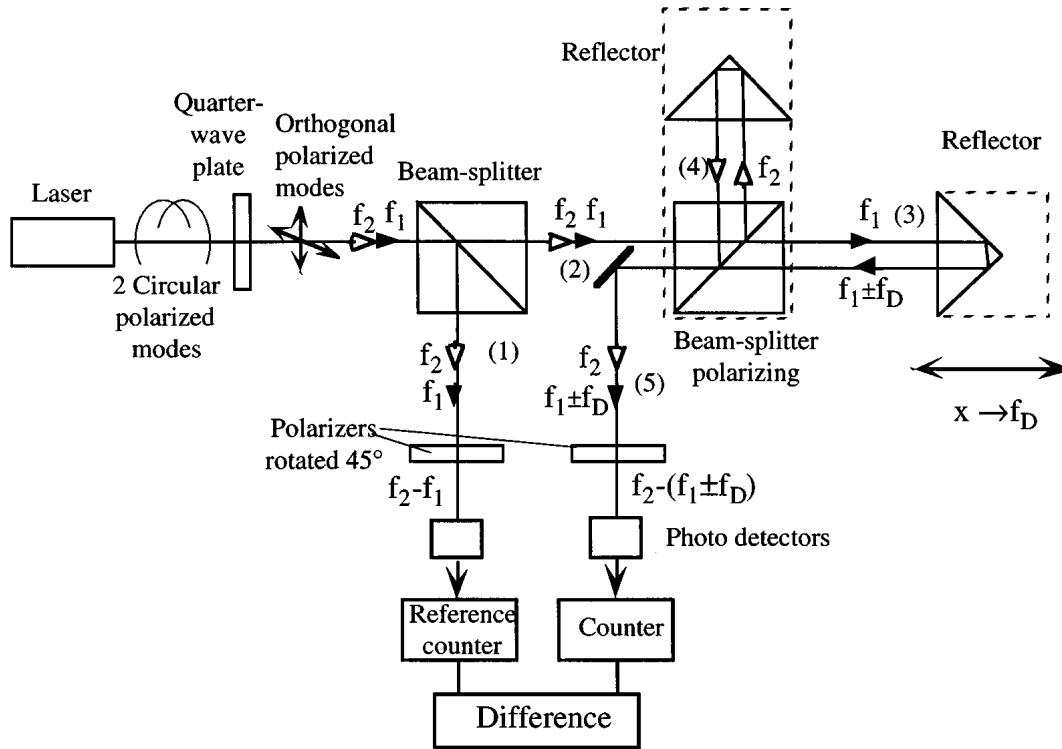


Figure 1.7 Schematics of Heterodyne Interferometer (Courtesy of Spindler and Hoyer Inc.)

1.5 Homodyne and Heterodyne Comparison

After introducing both homodyne and heterodyne systems, here is the reason that the heterodyne system is used for optical operation in this thesis. Essentially, the homodyne system determines the intensity ratio of laser source $I_o(t)$ and interference fringes (For example, $I_A(t)$ in equation (1.7)). The homodyne is a method with a great potential because its resolution depends on ADC output bits [4] and without the physical restriction in Doppler frequency, that means state-of-the-art electronics in ADC or other mixed-signal circuits can help the improving in both position resolution and velocity tolerance. But some realization problems may affect the signal integrity. In realization, the intensity of both $I_o(t)$ and $I_A(t)$ must be in a stable range and the

photodetector must have a good signal to noise ratio to keep the optical intensity transferring to the electronic signal correctly. Besides, to setup a homodyne system must challenge the following problem. (1) The measurement and reference beam overlap changes during motion; this makes the optical alignment facing a critical challenge or scarifies the coherence of interference fringes and loss the integrity in displacement, as shown in Figure 1.8 [12]. (2) Non-ideal characteristics of photodetectors, this may affect the intensity and produce the fault signal [12]. (3) When doing the multi-axes measurement, the laser source intensity $I_o(t)$ must be distributed to each axis equally; this makes the optical setup more complicated or needs to use multiple laser sources to finish the multi-axes setup [12].

The heterodyne systems do not need the careful regard for the beam intensity. Since the Doppler frequency f_D is carried on light central frequency produced by either Zeeman effect or AOM, the heterodyne systems care about the timing accuracy in each measurement cycle. The heterodyne systems also have weakness in resolve the displacement and velocity. To resolve the timing more accurate, the counting clock frequency must be multiple times faster then the reference/central signal. The slow reference frequency can have a better timing resolution intuitively, but the excessively slow reference frequency will limit the target speed away from the photodetector, which produces negative Doppler frequency.

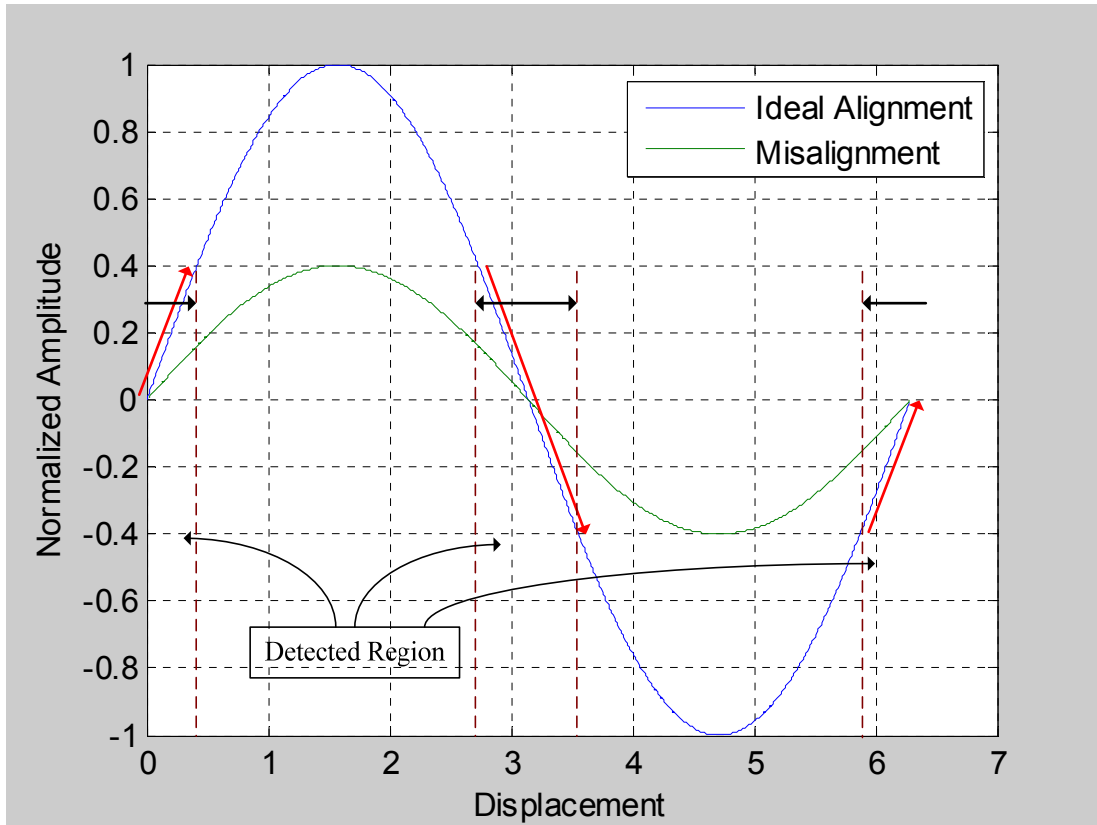


Figure 1.8 Effect on homodyne misalignment

To compromise the benefits and drawbacks of these two optical operations, this thesis chooses the heterodyne systems to assure the information integrity under a critical environment and inexpert optical alignment. Then increase the timing resolution by digital circuits' technique.

Chapter 2

Electronics of

Heterodyne Laser Interferometer

2.1 Basic Operation

The basic phase estimation of heterodyne laser signal is to put on a counter and count the cycle between the rising edges of measurement and reference signal, like the ΔT_1 in Figure 2.1 [14]. The phase change between cycles in Figure 2.1 is $\Delta T_2 - \Delta T_1$, accumulates the phase change continuously, and the total phase displacement can be determined. There still has problem in the determination of ΔT_1 and ΔT_2 , for example, what if the ΔT_1 or ΔT_2 is equal to 0? The control unit of the counter may have the ambiguity whether it should reset the counter or not. The feasible method to estimate the phase change is to place two counters to determine T_M and T_R respectively, and subtract T_R from T_M . Since T_R is almost a constant if the laser source frequency is stable enough, the interface updates the accumulating phase every rising edge of measurement signal. The control unit will feel comfortable in this method and process less error during the estimation of the phase variation.

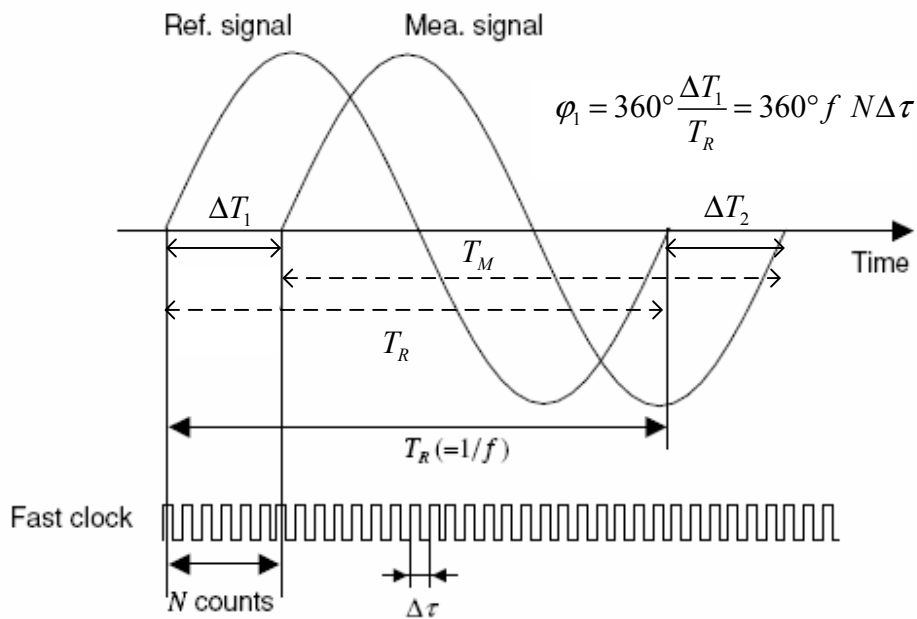


Figure 2.1 Basic Phase Estimation diagram.

Since the prototype of phase calculation is almost finished. There still has challenge between the timing resolution and the limitation on the digital circuits. As discussed before, the faster clock results the higher resolution on resolving every measurement signal, but the digital counter can not afford the fast clock as higher resolution expecting. Even the advanced lithography process progress everyday, the fast clock also produces consideration power consumption and increase the chip temperature. The following are several ways proposed to extend the timing resolution without increasing the clock speed. In the following discussions, the integral part means the multiple counts of the fast clock in Figure 2.1; the fraction part means the time interval in one fast clock period that is determined.

2.2 Delay Line Interpolator

The delay line interpolator method is proposed in 1998 by F.C. Demarest and Zygo Corporation [15]. As shown in Figure 2.2, the fast clock is generated from PLL and 20 MHz reference signal F_R . This PLL generates two clocks; one is 1280 MHz for the counter to evaluate the integral part of the timing register, and the other is 40 MHz for circuits processing. The 1280 MHz counter clock feeds into the delay locked loop which has eight stages delay line. When the DLL lock the period of the 1280 MHz clock, the same control voltage which is exported from the loop filter attaches on the slave delay line and produces the same delay in the delay line interpolator.

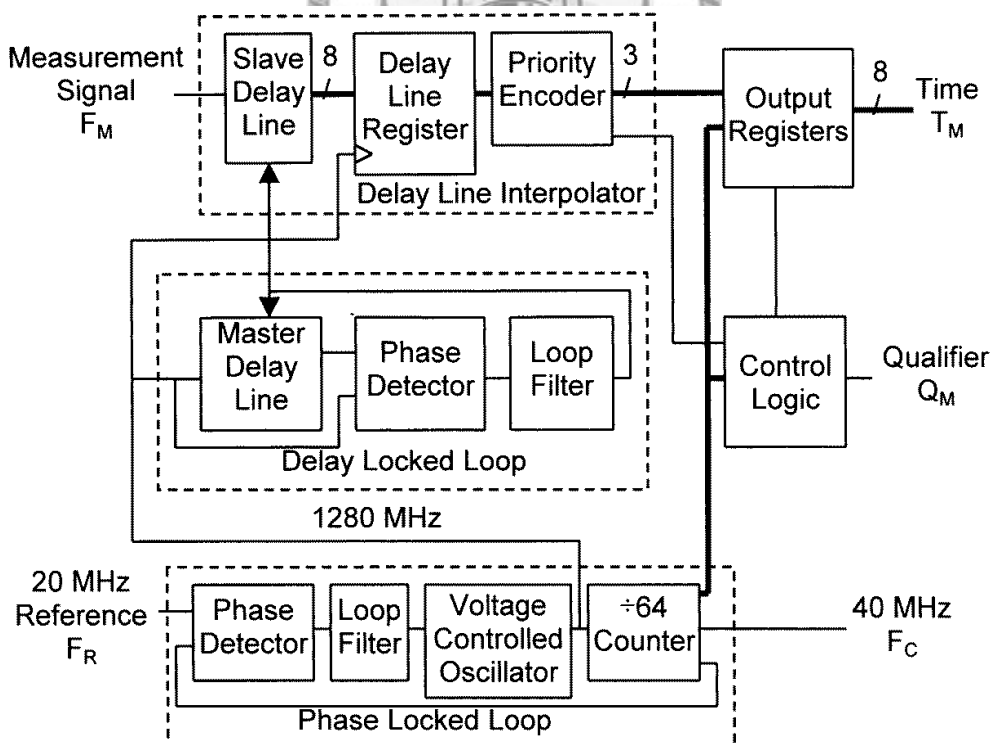


Figure 2.2 The block diagram of Zygo delay line interpolator.

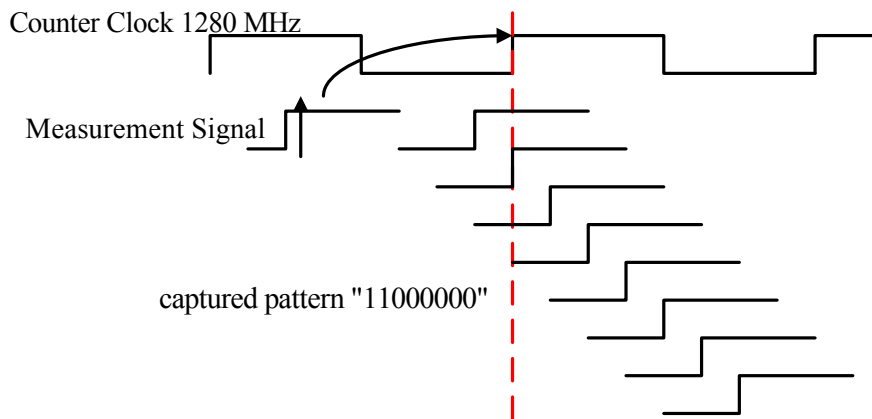


Figure 2.3 The operation diagram of Zygo delay line interpolator.

The slave delay line has the same delay behavior to the master delay line produced by the master delay line. When the measurement signal enters into the delay interpolator, the interpolator generates eight signals which have the delay to each other in one of eight period of the counter clock. As shown in Figure 2.3 [16], when the measurement signal occur a rising edge trigger, the control unit indicates the counter clock to capture the output of delay line interpolator. The captured pattern can represent the location where the measurement signal triggers in the previous counter clock cycle. If the measurement clock is ideally close to the previous clock rising edge trigger, the next clock trigger captures the pattern totally 1. And another situation, if the clock triggers at just half of the clock period in the previous clock, the next clock trigger will capture the pattern '11110000'. After the right code conversion, the captured pattern can represent the fractional part in one clock period. By this skillful method, it can obviously detect the timing under one clock cycle and have the eighth resolution than just use the fast clock from PLL.

2.3 Two-way Frequency-Conversion

The homodyne technique has the problem in intensity and direction ambiguity, and heterodyne technique has the restricted bandwidth by central frequency and resolution specification. For example, the digital phase meter resolves the timing to 1ns; the corresponding angular resolution is 0.36° in 1 MHz reference frequency. But the same 1ns, it only resolves to 3.6° in 10 MHz carrier signal. One way to increase the resolution is to shift the measurement and reference signal in a lower level, as shown in Figure 2.4 [14]. In Figure 2.4, the dropped heterodyne beat frequency f_b causes the narrow bandwidth in negative Doppler frequency.

The solution to this problem is to generate a signal which converts the Doppler frequency to a contrary direction.

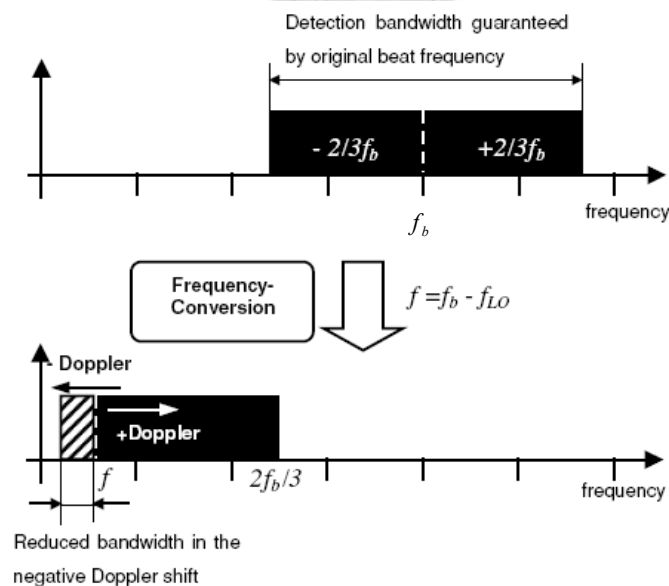


Figure 2.4 Frequency conversion diagram.

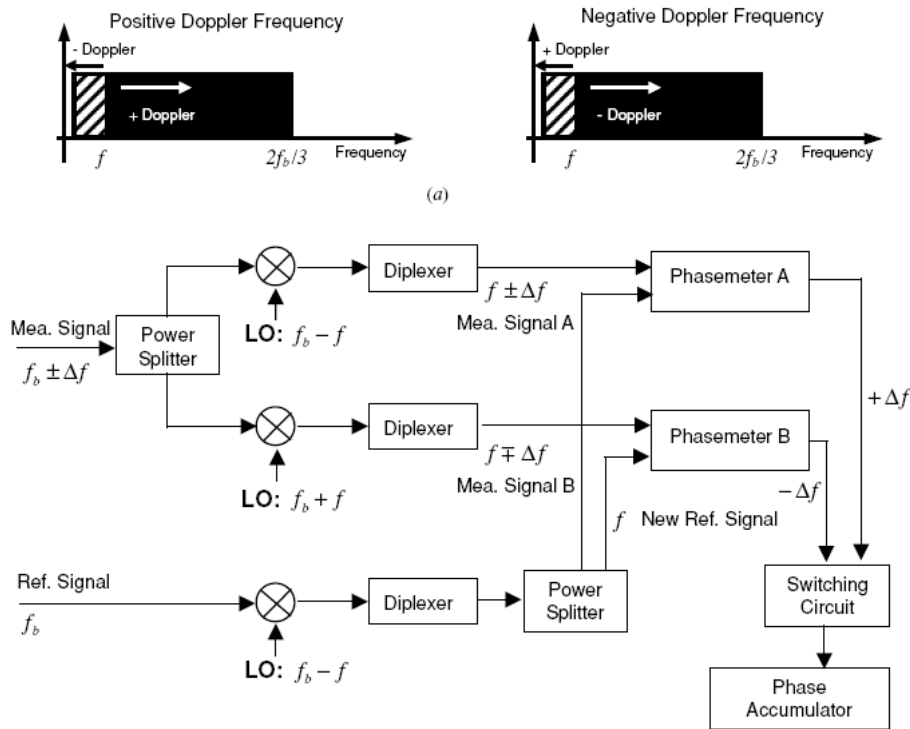


Figure 2.5 Two-way frequency conversion diagram.

As shown in Figure 2.5 [14], the measurement signal which carries the Doppler frequency pass through a power splitter and mixed with two frequencies, $f_b + f$, and $f_b - f$. The mixed signals have the identical carrier frequency f , and the Doppler frequency Δf have the same quantity but the opposite sign. The phasemeters digitalize the Doppler frequency both Δf and $-\Delta f$. Since these dual frequencies can be detected, $|\Delta f|$ is obtained when Δf is quite less than zero.

The converted Doppler frequencies have opposite sign in analog operation. A switching circuit is used to select the right Δf information. Shown in Figure 2.6 [14], when the target has a positive velocity, the phasemeter A continuously unwrap the information from the signal. When the velocity drops the zero, the phasemeter B starts

to read the signal

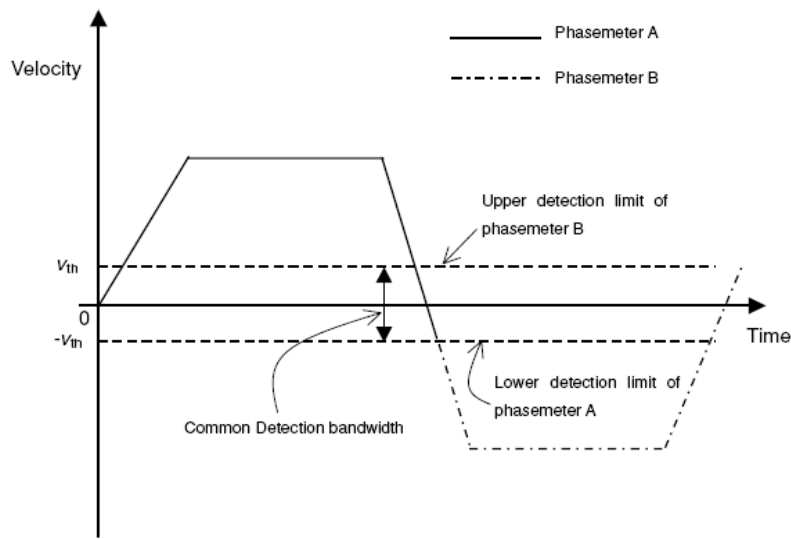


Figure 2.6 Phasemeters selection diagram.

and determines the Δf . When the frequency is lower than $-2/3f$, which is the lowest end that phasemeter A can detect, the switching circuit reads the data from phasemeter B to phase accumulator to continue the unwrapping operation.

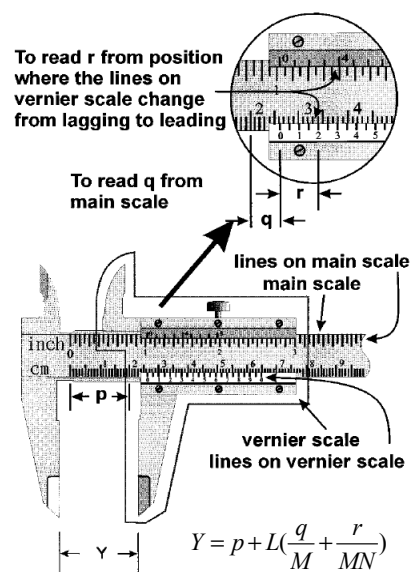
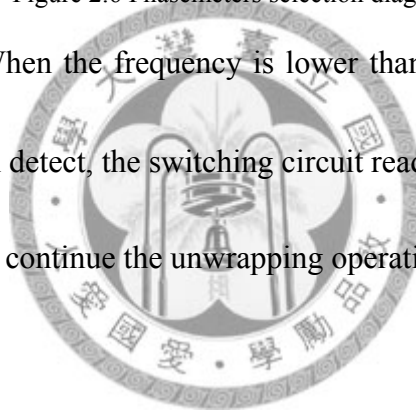


Figure 2.7 Mechanical Vernier Scale.

2.4 Vernier Scale

As its name, the Vernier scale method is developed from the mechanical Vernier caliper [17]. Figure 2.7 shows the operation of the Vernier caliper. The unit length L is divided into the equal segments which number is N and the stripes are inscribed on the Vernier scale. The same length L in the main scale is divided into M divisions (where $M = cN - 1$, c is a positive integer and is equal to 2 here). The resolution in Figure 2.7 is $L/(MN)$, and L in Figure 2.7 is 39 mm, M is 39, N is 20. The measured length Y is:

$$Y = 2 + 39 \text{ mm} \left(\frac{6}{39} + \frac{4}{39 \cdot 20} \right) = 2.62 \text{ cm} \quad (2.1)$$

The Vernier scale method is that assuming the incoming measurement and reference signal has the same or very close period. The common period can be viewed as the unit length L in the previous discussion. Pass the reference signal into a PLL and multiply the frequency by M , so the generated clock has M divisions in one reference

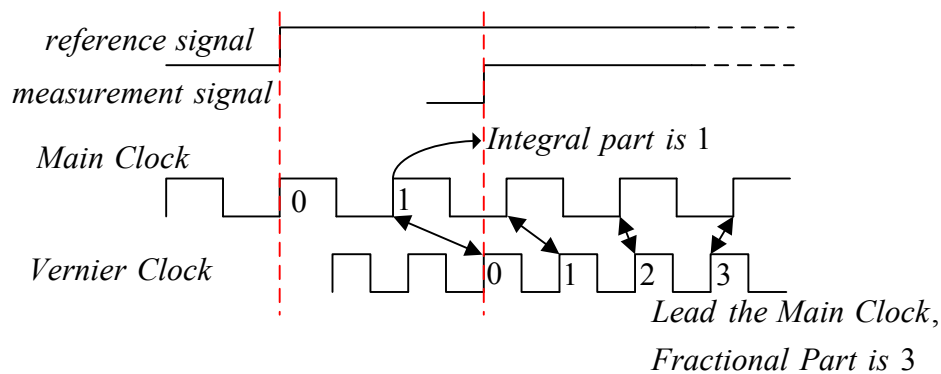


Figure 2.8 The operation of Vernier scale method.

period. The measurement signal is passed through another PLL and generates another clock which has N divisions in one measurement or nearly reference period. The operation diagram is shown on. The main clock determines the integral part of the phase difference. When the Vernier clock triggers, it begins to determine the fractional part. Every Vernier clock period, the Vernier clock chases upon the main clock in $1/MN$ period of the reference signal [17]. The counts that Vernier clock chases is the residual timing between the last main clocks trigger and the measurement signal triggers in $1/MN$ resolution of the reference signal. In Figure 2.8 [17], the main clock has the frequency M times that reference signal, and the Vernier clock has N times than the measurement signal. The main clock begins to count the integral part when the reference signal triggers. The counter counts to 1 when the measurement signal comes up, so the integral part is $1/M$. There still has time interval between the last main clock triggers and the measurement signal rises. The following operation makes the Vernier clock trigger detect the high low level of the main clock. Once the Vernier clock overheads the main clock, it means the undetermined time interval of main clock has been count in $1/MN$ (here the fractional part is $3/MN$).

The Vernier scale method increases the resolution tremendously, but the lack of velocity tolerance makes it difficult to realize on the servo control system. The reason is that the moving target mirror affects both measurement signal and the Vernier clock

which is generated from the measurement signal and PLL. That means the moving target mirror causes the jitter and undetermined timing during the fractional counting.

The previous research specify the restriction of the frequency deviation as the N times of the Vernier clock, the v_{\max} can be derived as below [18]:

$$|v_{\max}| \approx \left(\frac{\lambda}{2}\right) f_{ref} b^2, \text{ where } b = \frac{1}{N} \quad (2.2)$$

The resolution is limited by the t_s which is the settling time of the detecting flip-flop, and the b can be estimated as $b = t_s f_{max}$, where the f_{max} is the maximum reference frequency that the chip or device can work properly. This work is accomplished with

0.6 nm displacement resolution (with $\lambda/2$ linear interferometer), ± 0.3 m/sec target speed.



Chapter 3

Architecture

3.1 Octonary Phase Interpolation

This method is the reverse of the Zygo delay line interpolator which delays the measurement signal in one of eight of fast clock period. The PLL in this operation generates eight phases' signals of the fast clock. When the measurement signals triggers, it outputs the pattern of these eight phase clocks' high-low level, and if the phases is generated precisely, the trigger location below one clock cycle can be located in anyone of eight patterns in one clock period.

As shown in Figure 3.1. The measurement signal export the pattern from the eight phase clocks. The 8-bits number then pass through a code converter and transform to

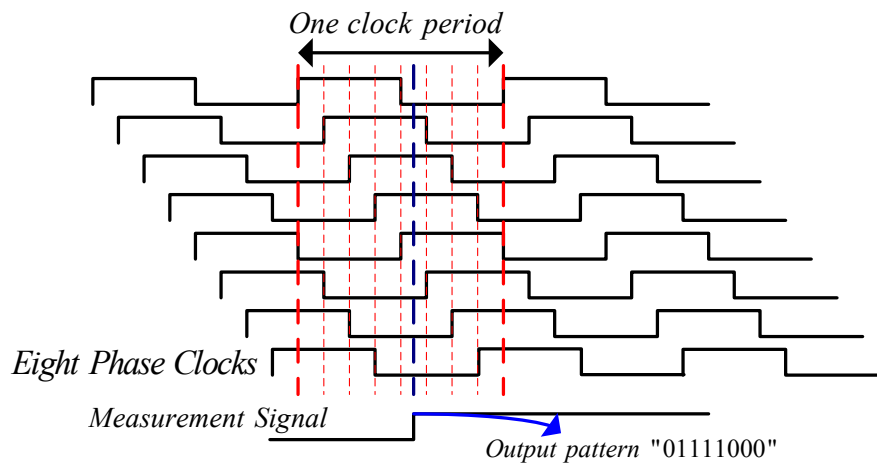


Figure 3.1 The operation of Octonary phase interpolation.

a 3-bits number which represents the read phase location from 0 to 7.

Subtracting the previous measurement cycle's phase location from the new read ones induces the phase difference below one clock period between two measurement cycles. This difference is employed as the fractional part of one measurement counting, and expanding the timing determination sub clock.

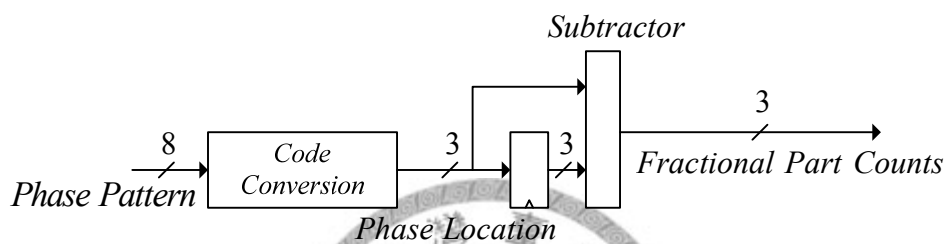


Figure 3.2 Fractional Part Determination.

3.2 Data path of Integer Part Calculation

The integer part time counting is to count the measurement signal period by a faster clock, the counts can represent the time ought to the measurement signal period with

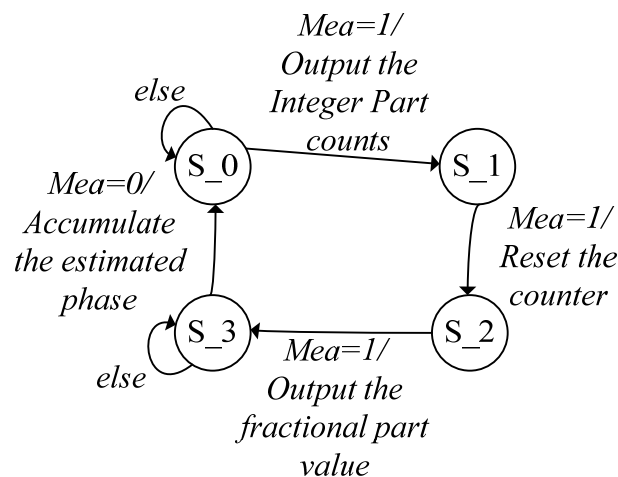


Figure 3.3 The control unit of the Integer part calculation.

the timing resolution in one faster clock period. As shown in Figure 3.3, the idle state is S_0 , and when the measurement comes to 1, the state machine generates three pulses sequentially, which first outputs counter's value in that time, and then reset the counter, finally outputs the fractional part value. When the measurement goes down to 0, the circuits accumulate the counts as the incremental phase difference. During the pass and reset process, the circuits do not count the time even the measurement signal is in high voltage level. Due to this situation, the real integer counts are the counter's counts plus 2.



Figure 3.4 The save and reset timing diagram of the control unit.

In Figure 3.5, a trouble appears when the circuits are implemented on the FPGA. Since the counts' integral and fractional part is calculated separately. The meta-stability problem of the integral part counter induces the value instability even the frequency varies within one clock period. This problem drops the time resolution to one clock period, and the fractional part detect is useless because the integral part varies an extra count and the frequency do not change so. The following sections propose several ideas to solve this problem and guarantee the time resolution under a

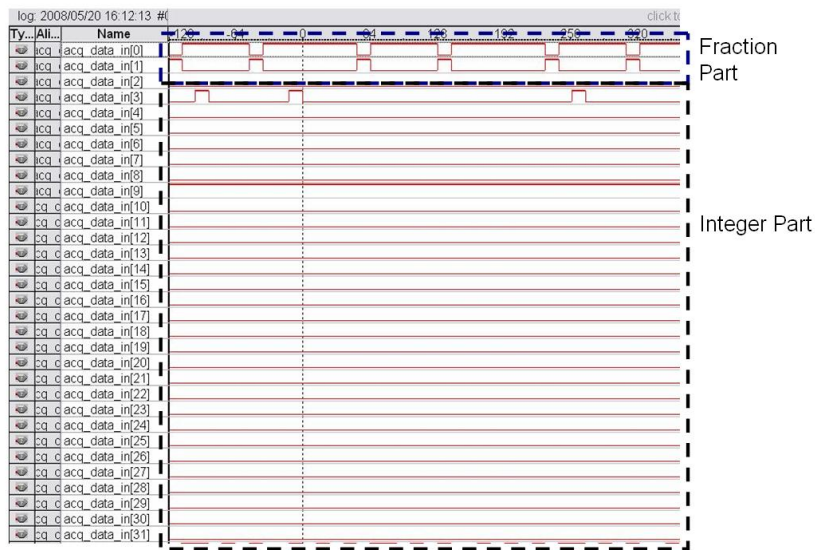


Figure 3.5 The integral parts counts change unstably.

clock period.

3.3 Multiplexer Determination

In previous sections, a counter module with save-and-reset action is represented as an `int_counter` module as in Figure 3.6. Eight `int_counter` modules are employed and connect with eight different phases of clocks, and each of them counts the same measurement signal.

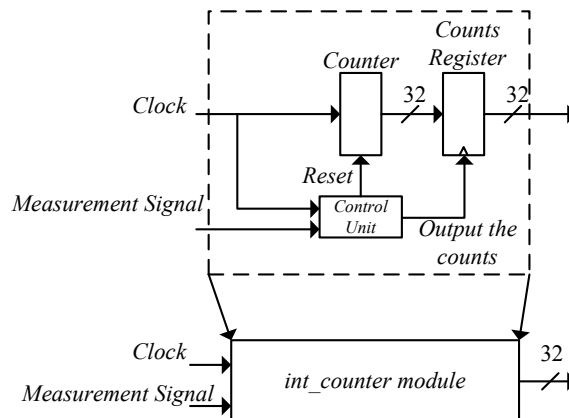


Figure 3.6 A counter module with save-and-reset control unit.

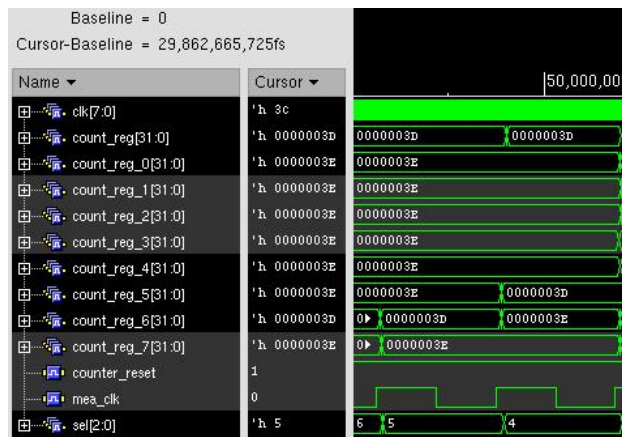


Figure 3.7 count registers' relationship with the fractional part value.

In ideal case, the output counts register has a corresponding relationship with the fractional part value. As depicted in Figure 3.7, the `count_reg_0` to `count_reg_7` are the counts result of eight different phase's clock which count the same measurement signal. The 3-bits `sel` register is the phase location of that cycle's measurement trigger. The `sel` here from 6, 5, to 4 in each measurement cycle, which reveal the fractional part value is 7. In integral part, one of the eight numbers is 3D and others seven are 3E. It means there are 7 clocks has triggered before the measurement signal trigger in the last clock period. This multi-counter calculation helps us to determine the integral part value more accurate. The first developed method is to select the counts register by the multiplexer. As shown in Figure 3.7, the correct register is `count_reg_6` where the `sel` is 5. The less integral number plus the fractional part constitute the correct frequency estimation. The schematic is shown as Figure 3.8.

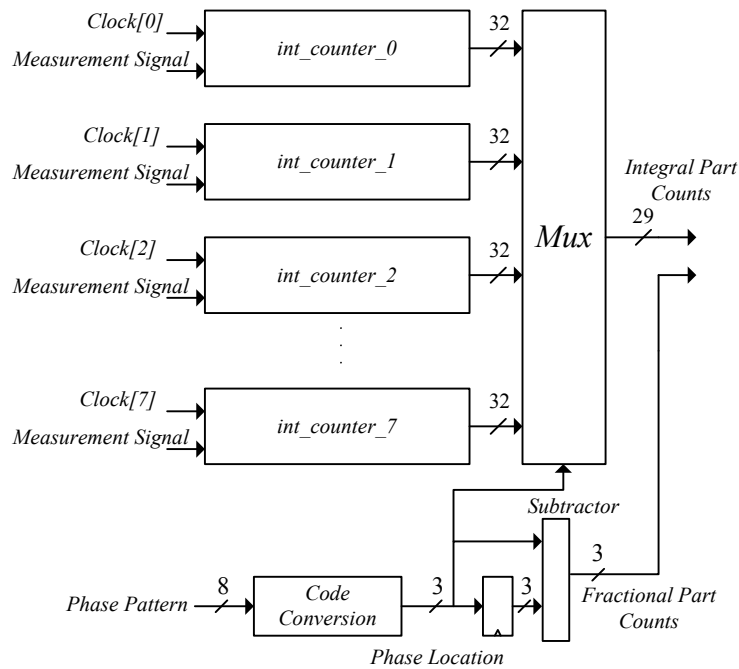


Figure 3.8 Schematic of multiplexer determination.

Although the multiplexer selection looks reasonable, it gets tough to realize on chip. This architecture can not endure different PVT library, and selection between the phase location register sel and the correct integral register is mismatch under different process library. Besides, under the FPGA test, the integral part still vibrates no matter the register is choose. A revised integral part determination is proposed in the following section to deal with this problem.

3.4 Minimum Sorter Determination

The multiplexer determination causes plenty of troubles in implementation; the minimum determination is the improved function to choose the correct integral register. As shown in Figure 3.7, the correct integral part value is 3D no matter the

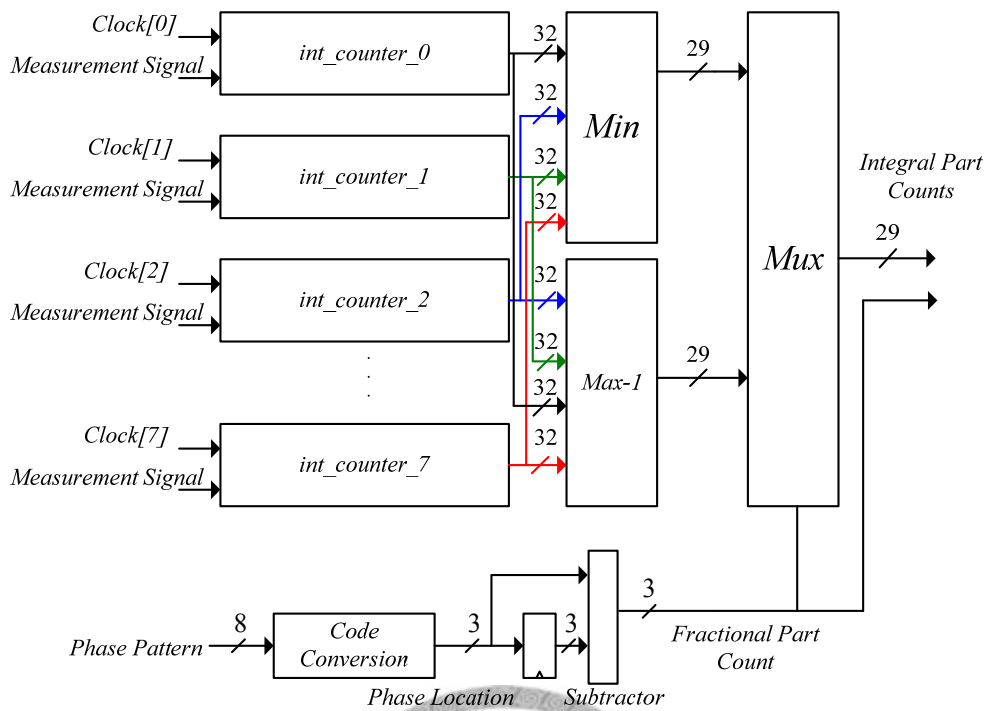


Figure 3.9 Schematic of minimum sorter determination

phase location is 6, 5, or 4, and the minimum of the eight integral part values also can represent the counts from the last beginning clock after the measurement signal trigger. This method endures the different register corner and performs a better result than the foregoing. The further formation is to pass the signal into both minimum and maximum minus 1 block, as shown in Figure 3.9. This arrangement is to prevent the miscounting situation like in Figure 3.7 if the only minimum register is miscounted to 3E. The fractional part is involved again to recognize which register should be employed. The complete block diagram is shown in Figure 3.9.

The overall architecture is shown in Figure 3.10. The multiply 64 PLL generates the eight phases' clocks and synchronizes with the reference signal. The phasemeter

mentioned foregoing calculates the measurement count and outputs the digital words. The adder adds the constant reference count due to the synchronized reference signal. The variance between the measurement count and reference count can represent the velocity output in the moment, and the incremental velocity is the accumulated displacement since the measurement process starts.

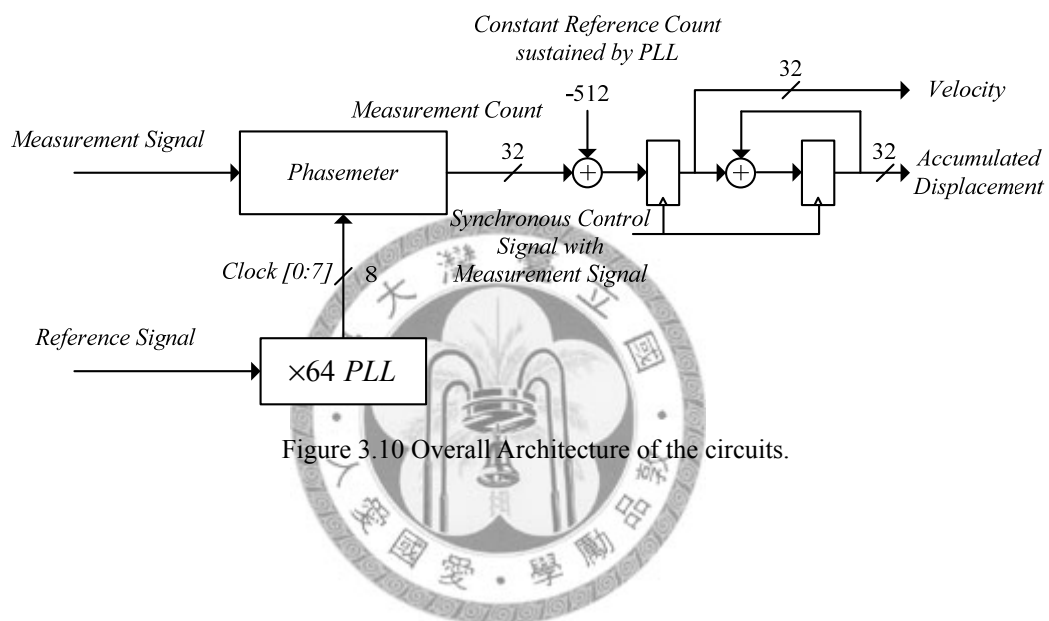


Figure 3.10 Overall Architecture of the circuits.

3.5 Metastability and Displacement Resolution Discussion

In practical realization, it only needs four clocks in Figure 3.1 and is enough to determine eight phase location where the measurement signal triggering. Assume that the flip-flops' setup and hold time region are not over eighth of one clock period. As shown in Figure 3.11, the measurement signal triggers at the rising edge of $clk1$. Since the $clk2$, $clk3$, and $clk4$ are stable in this region, the probable location here is phase location 7 or 0, which is only affected by the metastability in $clk1$. However, no

matter which location is chosen, the displacement error does not exceed the resolution that under eighth of one clock period.

The displacement resolution relies on the timing resolution of the reference signal but not the measurement ones. If the fixed timing resolution is 0.1 ns, the displacement resolution is 0.632 nm if the wavelength is 632 nm and the frequency is 1 MHz. The resolution rises to 63.2 nm if the frequency is up to 10 MHz. In the heterodyne interferometry, the displacement resolution is the phase or timing resolution of the reference signal. The measurement signal's timing results only represent the time portion in the reference one. Although the fixed timing resolution may have the more indistinct resolution in resolving the fast measurement signal's timing, the counted measurement portions under the reference signal phase resolution does not affect or drop the resolution of displacement.

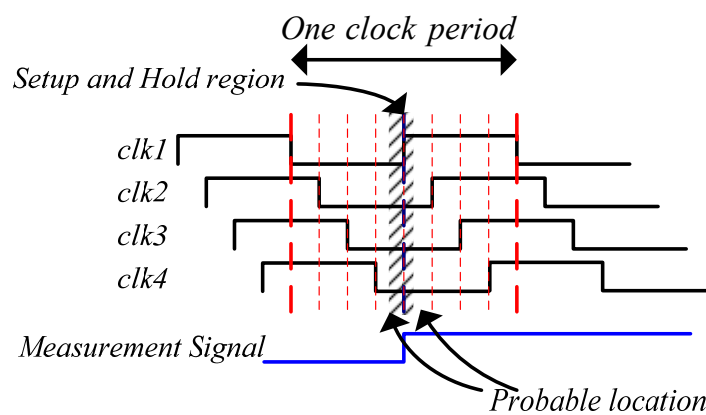


Figure 3.11 The probable determined phase location when the timing violation occurs.

3.6 Method comparison

The Zygo delay line interpolator has a good performance including the high displacement resolution under a clock period and high velocity tolerance of target mirror, but it requires more sophisticated analog components (one PLL, one DLL, and one delay line) to cooperate and finishes the work. The frequency shift method has a great advancement in displacement resolution and hold on the tolerance in mirror translation velocity, but it also needs lots of analog component such as mixers, diplexers, and frequency synthesizers to generate precise frequency in local oscillator parts of Figure 2.5 [14]. The frequency of local oscillator needs the precise adjustment or it makes error in calculating the displacement.

The Vernier scale method needs less analog components (two PLLs) to achieve high displacement resolution. But the measurement signal induces the clock unstable troubles and restricts the mirror translating speed to 0.3 m/s.

The self-developed octonary interpolator provides a digital architecture to solve this problem with less analog components (one eight phase PLL), and make it easy to implement entire measuring system in a FPGA board (Altera Cyclone III FPGA). The following is the comparison of several heterodyne electronics.

Table 3.1 Comparison of Heterodyne Electronics

	<i>Mea. Sci.</i> 1998	<i>Mea. Sci.</i> 2004	<i>Mea. Tech.</i> 2006	<i>Agilent</i> <i>NI231B</i>	This work
<i>Position Resolution</i>	$\lambda/512$	$\lambda/1024$	$\lambda/512$	$\lambda/1024$	Function generator testing: $\lambda/64$ On-chip PLL testing: $\lambda/512$
<i>Speed Tolerance in</i> <i>Target Mirror</i>	2.2 m/s	2.4 m/s	0.3 m/s	2.8 m/s	0.5 m/s
<i>Electronic</i> <i>Implementation</i>	Digital: ECL Asic. Analog: one DLL, one Delay Line one PLL.	Digital: FPGA Analog: Mixers, Diplexers, Frequency Synthesizers	Digital: FPGA Analog: Two PLLs.	Digital: FPGA Analog: Unknown.	Digital: FPGA Analog: one PLL (8 phase output.)

3.7 Gate Level Simulation on TSMC 0.18 μm Design Kits

To simulate and test the interferometer digital circuits, a method is to employ a variable wave to simulate the effect of Doppler frequency. If the circuits can detect the measurement frequency indeed, the variance between it and reference frequency can be detected. Displacement and speed of the target mirror can also obtain.

The testbench sets the reference frequency as 4 MHz for Agilent Laser Head 5517D which frequency ranges from 3 MHz to 4 MHz, and multiply the clock frequency up to 256 MHz. Cooperating with the octonary phase interpolator, the total displacement resolution compromises to $\lambda/512$, λ is the wavelength of laser and comes to 632 nm in vacuum. The measurement frequency is set as a frequency variant signal, which varies around the reference frequency 4 MHz. To avoid the timing violation from uncertain

measurement triggering, the frequency variance is set as a fractional number which denominator is 512.

$$T_{ref} \times \left(\frac{\text{any value}}{512} \right) = \frac{T_{ref}}{64} \times (\text{Integral} + 2) + \frac{T_{ref}}{512} (\text{fractional}) \quad (3.1)$$

The testbench of this simulation and the detailed measurement profile is shown in Table 3.2. As shown in Figure 3.13, the pictures show the circuits work properly during every measurement frequency changes. Equation (3.1) shows the relationship between the measurement period and the detected integral and fractional value. The measurement period is modulated with (any value/512), which means the minimum timing resolution under this architecture is 1/512 of reference period. The integral part is determined by the counter which has clock speed 64 times than reference period. The resolution of the integral part is 1/64 of reference period. The fractional part is the eight phase interpolator of one clock period, which has 8 times timing resolution than the clock speed, also as 1/512 of reference period time resolution.

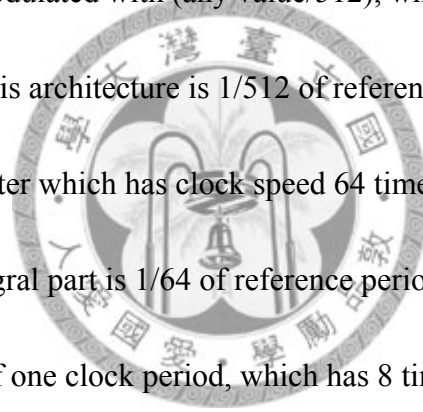


Table 3.2 Testbench for gate-level simulation on TSMC 0.18 μm design kits.

<i>Library</i>	TSMC 0.18 μm	
<i>Area</i>	870938.515625 μm^2	
<i>Clocks</i>	Eight 256 MHz clocks with 45° difference	
<i>Displacement Resolution</i>	$\lambda/512$	
<i>Reference Frequency</i>	4 MHz	
<i>Measurement Frequency</i>		
<i>Period</i>	<i>Corresponding Integral Value</i>	<i>Corresponding Fractional Value</i>
<i>250 ns * (511/512)</i>	0x3D	7
<i>250 ns * (502/512)</i>	0x3C	6
<i>250 ns * (493/512)</i>	0x3B	5
<i>250 ns * (484/512)</i>	0x3A	4
<i>250 ns * (475/512)</i>	0x39	3
<i>250 ns * (466/512)</i>	0x38	2
<i>250 ns * (457/512)</i>	0x37	1
<i>250 ns * (448/512)</i>	0x36	0

The first simulation result is in typical model, as shown in Figure 3.12. Table 3.3 shows the signal index of each signal. The corresponding counts appears clearly with the measurement frequency change even the variance is small. Figure 3.13 and Figure 3.14 are the zoom-in figures from Figure 3.12. The detailed signals like the state machine are shown and the correct integral part can be determined without error. The fractional part is also shown as predicted. Figure 3.15 shows the simulation results in slow and fast model. During the simulation in slow model, most phase location cannot be ascertained due to the timing violation between measurement trigger and the clocks transition. It means the chip cannot work in the difficult environment or the mistakes may occur under this specification. The fast model shows the same results with the

typical model.

Table 3.3 Signal names for gate-level simulation on TSMC cell library

<i>Mea_clk</i>	Measurement Frequency.
<i>Clk[7:0]</i>	Eight different phase clocks.
<i>Count_sub[31:0]</i>	The value the subtract measurement counts from the reference counts.
<i>Count_reg</i>	The selected integral parts by combination logics
<i>Count_reg_0[31:0]</i>	Integral parts of measurement counts synchronized with clk[0].
<i>Count_reg_1[31:0]</i>	Integral parts of measurement counts synchronized with clk[1].
<i>Count_reg_2[31:0]</i>	Integral parts of measurement counts synchronized with clk[2].
<i>Count_reg_3[31:0]</i>	Integral parts of measurement counts synchronized with clk[3].
<i>Count_reg_4[31:0]</i>	Integral parts of measurement counts synchronized with clk[4].
<i>Count_reg_5[31:0]</i>	Integral parts of measurement counts synchronized with clk[5].
<i>Count_reg_6[31:0]</i>	Integral parts of measurement counts synchronized with clk[6].
<i>Count_reg_7[31:0]</i>	Integral parts of measurement counts synchronized with clk[7].
<i>Fraction[2:0]</i>	Fractional parts of measurement counts
<i>Sel[2:0]</i>	Phase Location of measurement trigger
<i>Total_count[31:0]</i>	Accumulated phase variance.
<i>Total_reset</i>	Reset signal to total_count[31:0] register.
<i>Reg_transfer</i>	State 1 of state machine to save the counters' counts.
<i>reset</i>	State 2 of state machine to reset the counters. (Negative trigger.)
<i>Sel_ctrl</i>	State 3 of state machine to shift previous and present phase location. (Negative trigger.)
<i>add</i>	Accumulate the phase difference.

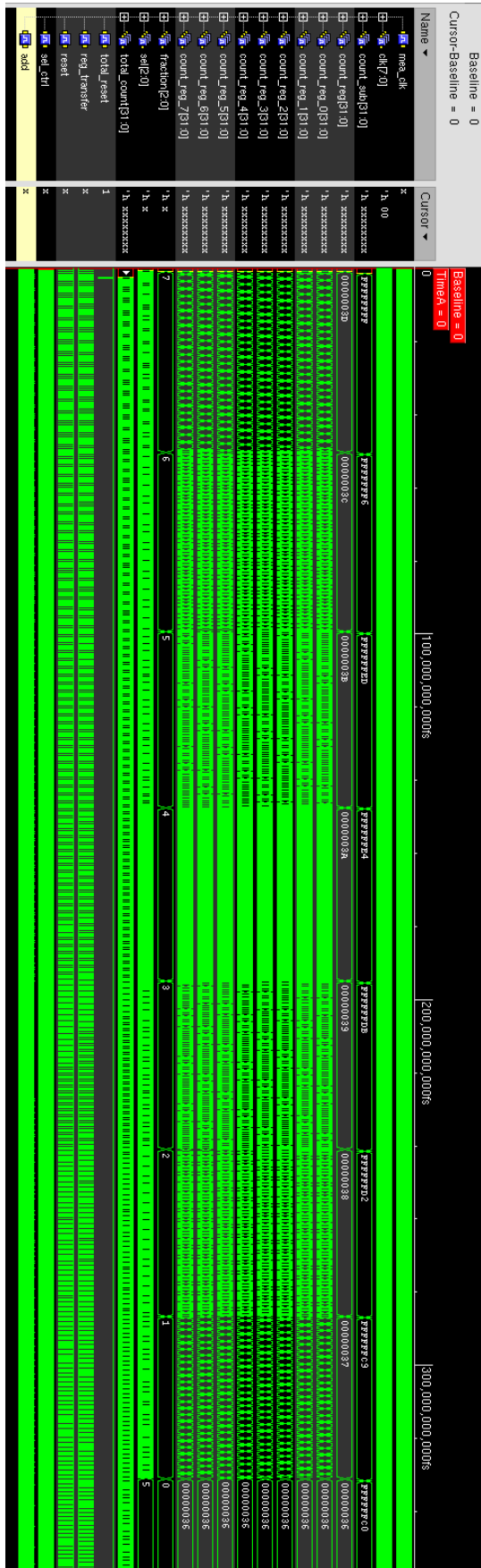
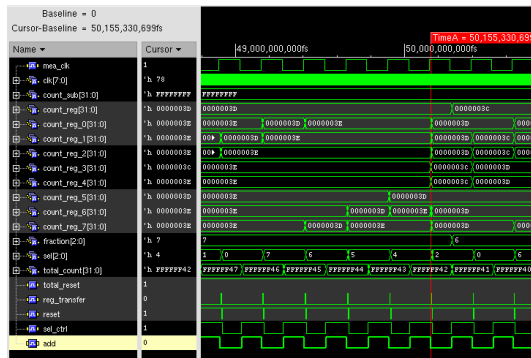
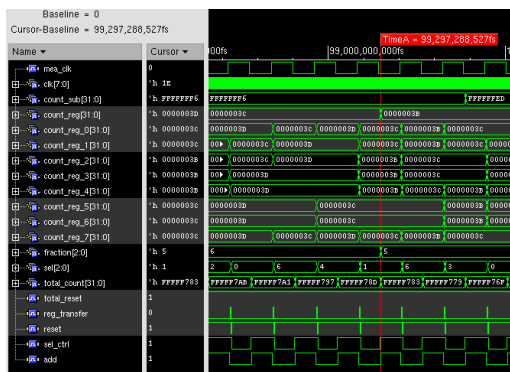


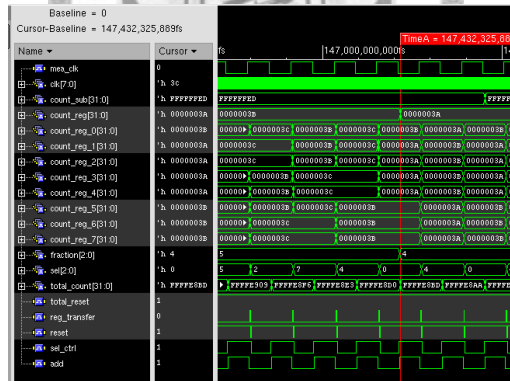
Figure 3.12 Gate-level Simulation in typical model



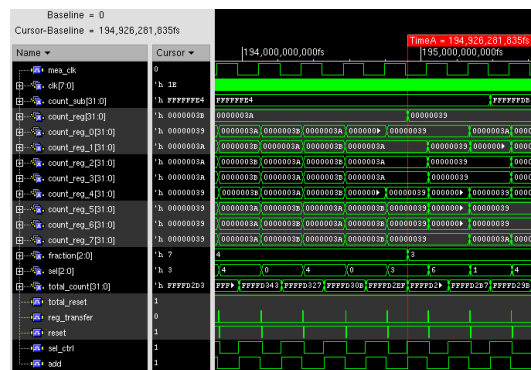
Corresponding Counts From 3D.7 to 3C.6



Corresponding Counts From 3C.6 to 3B.5

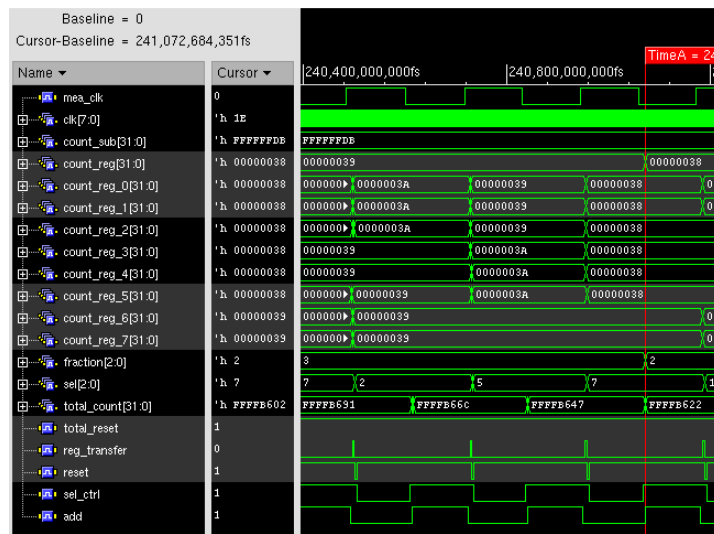


Corresponding Counts From 3B.5 to 3A.4

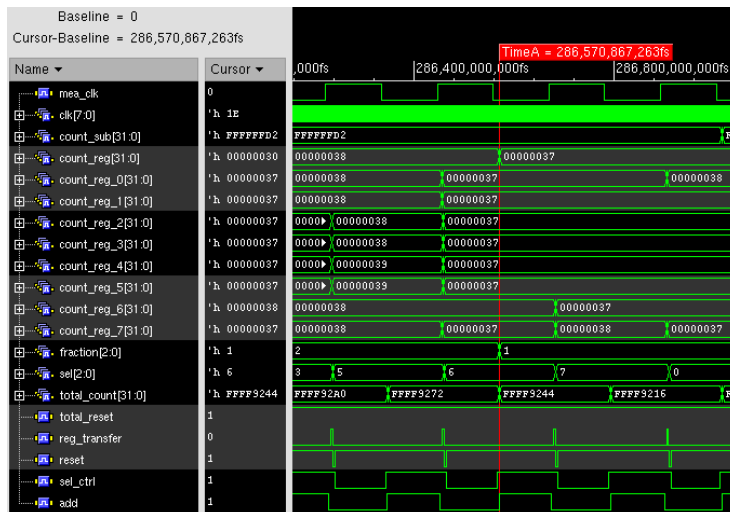


Corresponding Counts From 3A.4 to 39.3

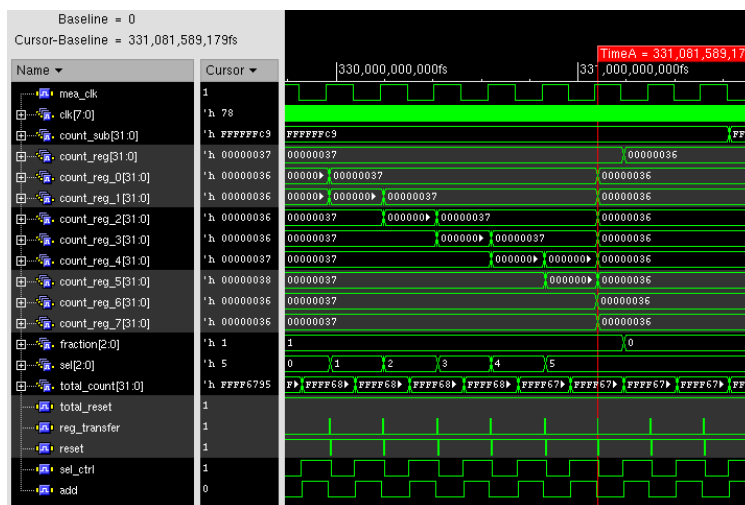
Figure 3.13 The details of the gate-level simulation results from 3D.7 to 39.3.



Corresponding Counts From 39.3 to 38.2

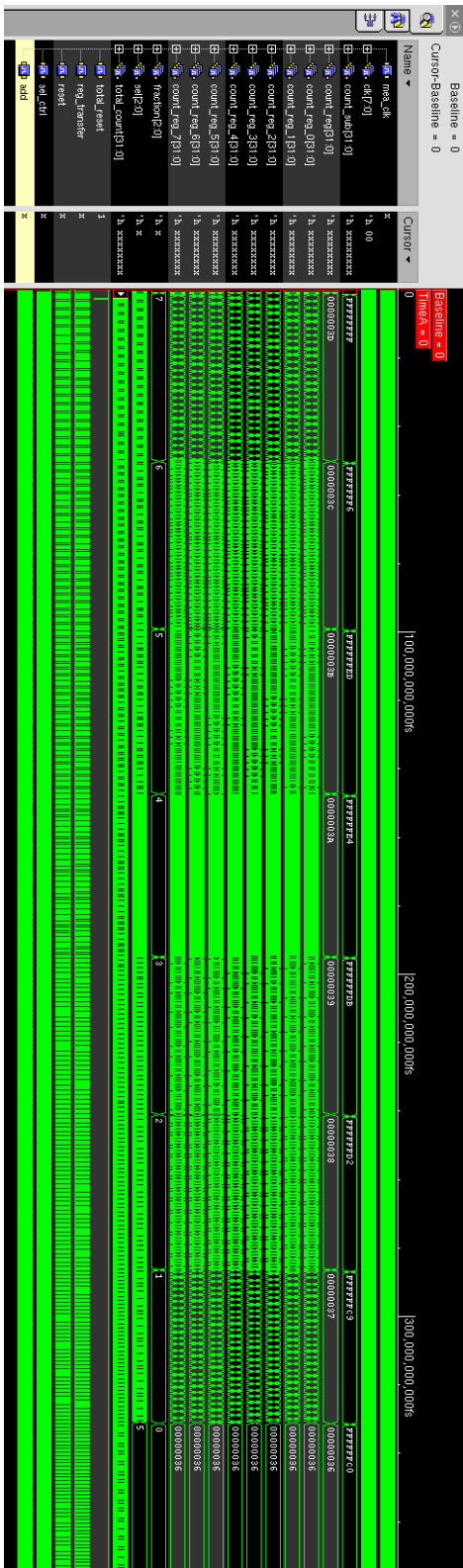


Corresponding Counts From 38.2 to 37.1

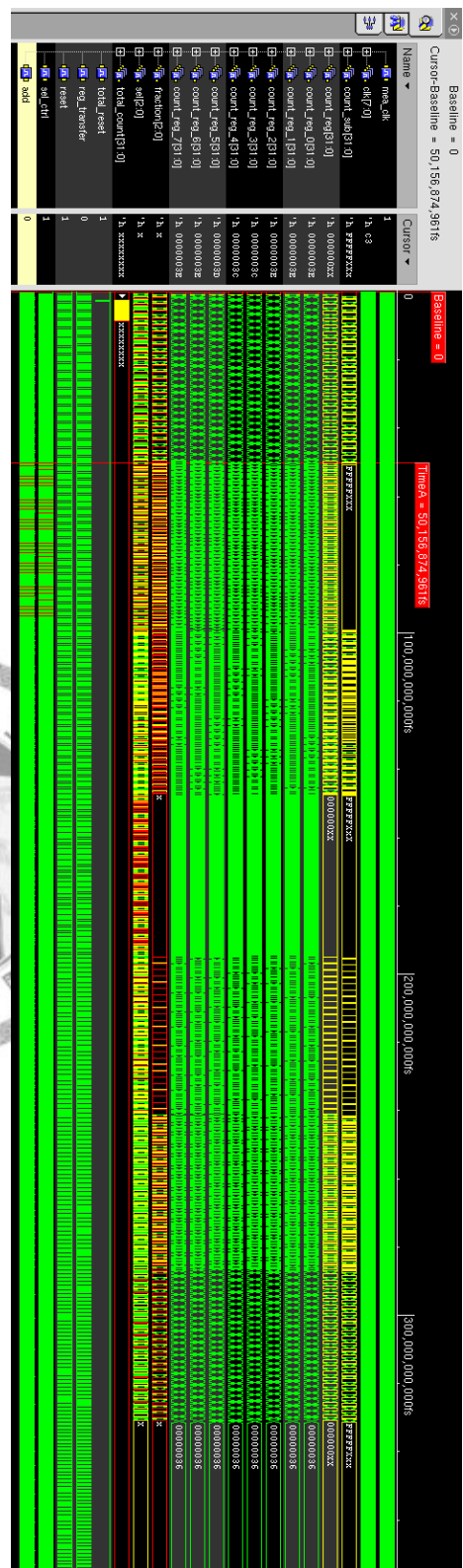


Corresponding Counts From 37.1 to 36.0

Figure 3.14 The details of the gate-level simulation results from 39.3 to 36.0.



(a)



(b)

Figure 3.15 (a) The gate-level simulation in fast model. (b) Gate-level simulation in slow model.

Chapter 4

FPGA Verification

4.1 Architecture Adapted for Cyclone III

The PLL included in Cyclone III can not lock the input frequency under 4 MHz. To compromise this situation, the architecture is modified to two phasemeter and subtracts the measurement count from reference ones. The chip clocks run at 260 MHz and the displacement resolution is around $\lambda/550$. The overall architecture is shown in Figure 4.1. Unlike the other one shown in Figure 3.10, this architecture counts both reference and measurement signal simultaneously, and synchronizes the reference count with the measurement part control signal. This setup synchronizes the reference count which is updated by the reference signal, and avoids the timing violation due to the different updating frequency.

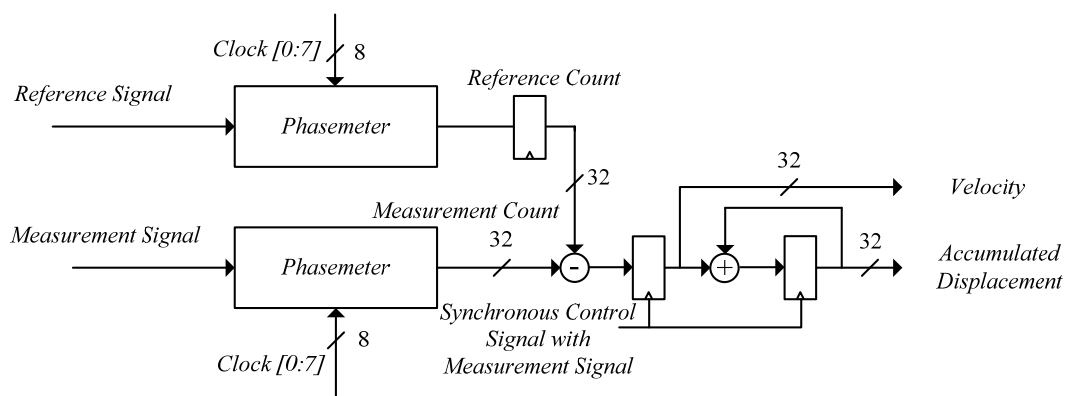


Figure 4.1 Architecture adapted for Cyclone III FPGA

4.2 Gate-level Simulation and On-chip Testing

Before the experiment, the gate-level simulation provides a platform to verify whether the design is workable. Here uses Altera® Cyclone® III library and Synopsys® Design Compiler® for HDL synthesis and delay annotation. The clock speed drops to 32 MHz due to the conservative delay model. The clock speed rises to 260 MHz on the on-chip testing. The actual integral value is 8 here when the measurement frequency is equal to reference frequency, but the calculated value is 6 here. The missed 2 is due to the save and reset process in the state machine.

Table 4.1 Gate-level Simulation Environment for Cyclone III FPGA

<i>Library</i>	Cyclone III	
<i>Area</i>	N/A	
<i>Clocks</i>	Eight 32 MHz clocks with 45° difference	
<i>Displacement Resolution</i>	$\lambda/64$	
<i>Reference Frequency</i>	4 MHz	
<i>Measurement Frequency</i>		
<i>Period</i>	<i>Corresponding Integral Value</i>	<i>Corresponding Fractional Value</i>
<i>250 ns* (127/64)</i>	0xD	7
<i>250 ns* (118/64)</i>	0xC	6
<i>250 ns* (109/64)</i>	0xB	5
<i>250 ns* (100/64)</i>	0xA	4
<i>250 ns* (91/64)</i>	0x9	3
<i>250 ns* (82/64)</i>	0x8	2
<i>250 ns* (73/64)</i>	0x7	1
<i>250 ns* (64/64)</i>	0x6	0

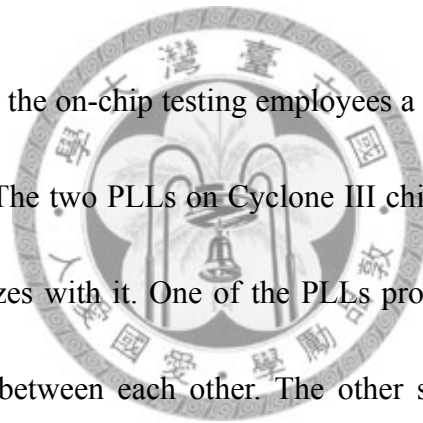
The following chart splits to two to show the signal index of the reference and measurement timing diagram.

Table 4.2 Signal names for reference phasemeter on Cyclone III gate-level simulation.

<i>ref_clk</i>	Reference Frequency.
<i>Clk[7:0]</i>	Eight different phase clocks.
<i>Count_reg_ref[31:0]</i>	The selected integral parts of reference counts
<i>Count_reg_0[31:0]</i>	Integral parts of reference counts synchronized with clk[0].
<i>Count_reg_1[31:0]</i>	Integral parts of reference counts synchronized with clk[1].
<i>Count_reg_2[31:0]</i>	Integral parts of reference counts synchronized with clk[2].
<i>Count_reg_3[31:0]</i>	Integral parts of reference counts synchronized with clk[3].
<i>Count_reg_4[31:0]</i>	Integral parts of reference counts synchronized with clk[4].
<i>Count_reg_5[31:0]</i>	Integral parts of reference counts synchronized with clk[5].
<i>Count_reg_6[31:0]</i>	Integral parts of reference counts synchronized with clk[6].
<i>Count_reg_7[31:0]</i>	Integral parts of reference counts synchronized with clk[7].
<i>Fraction[2:0]</i>	Fractional parts of reference counts
<i>Sel[2:0]</i>	Phase Location of reference signal trigger
<i>Reg_transfer</i>	State 1 of state machine to save the counters' counts.
<i>reset</i>	State 2 of state machine to reset the counters. (Negative trigger.)
<i>Sel_ctrl</i>	State 3 of state machine to shift previous and present phase location. (Negative trigger.)
<i>add</i>	State 0 of state machine to process the integral part counts determination.

The timing diagram shown in Figure 4.2 shows the reaction of the output registers after the measurement signal in Table 4.1 is fed in. The selected integral part value varies depending on the different measurement signal, and the fractional part also responds as expecting. The signal index of the Figure 4.2 (a) is same as the Table 3.3. Although the reference integral part count is less 2 than the actual value which should be detected, the measurement ones suffer the same situation. After the subtraction for the frequency determination, the non-ideal issue is canceled and output the correct frequency information.

As shown in Figure 4.3, the on-chip testing employees a PLL to simulate the variant measurement frequency. The two PLLs on Cyclone III chip connects to two different oscillators and synchronizes with it. One of the PLLs provides the clocks which are 260 MHz and have 45° between each other. The other supplies the programmable measurement signal to check if the circuits work in the right function. The SignalTap® II embedded logic analyzer captures the signal inside the design logic and display on the host PC through the JTAG connection. The operation diagram is shown in Figure 4.4 [19]. The download design includes the SignalTap II instance, and the embedded logic analyzer storage the data in the on-chip memory every clock trigger.



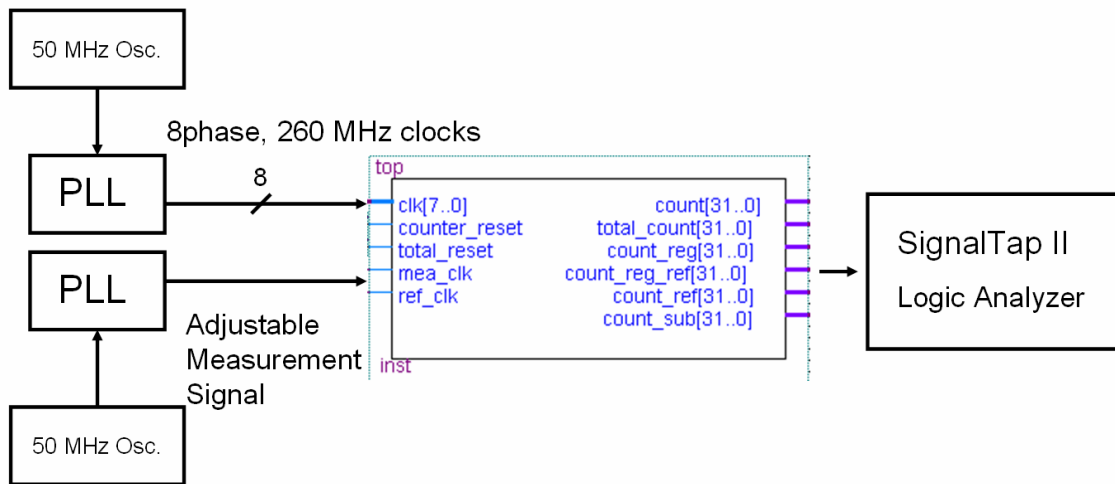


Figure 4.3 Testing diagram in Cyclone III FPGA

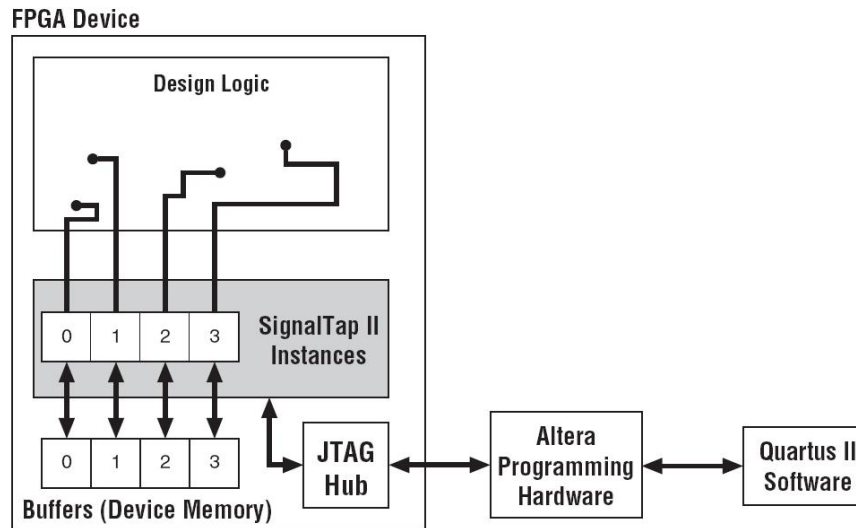
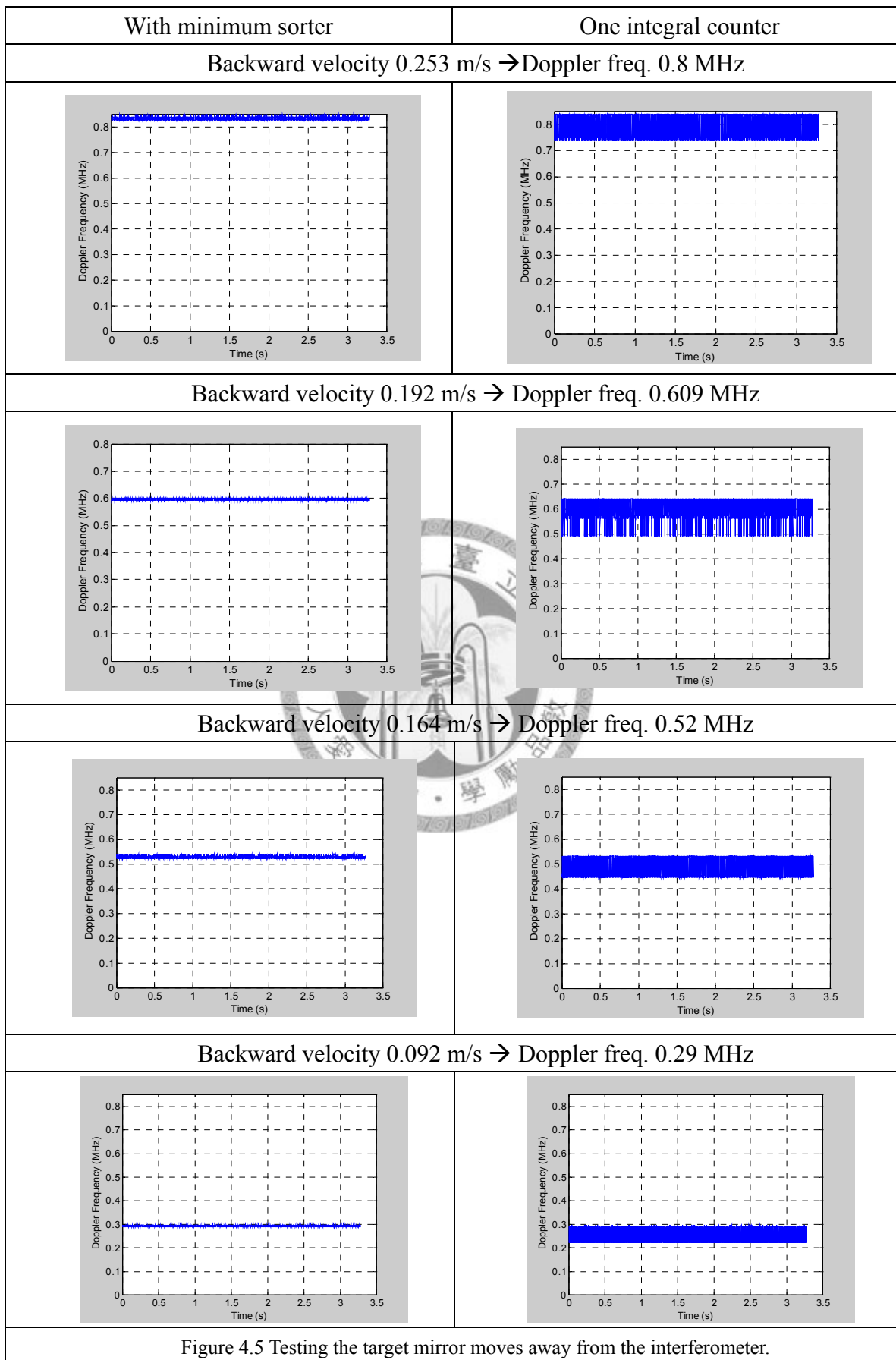
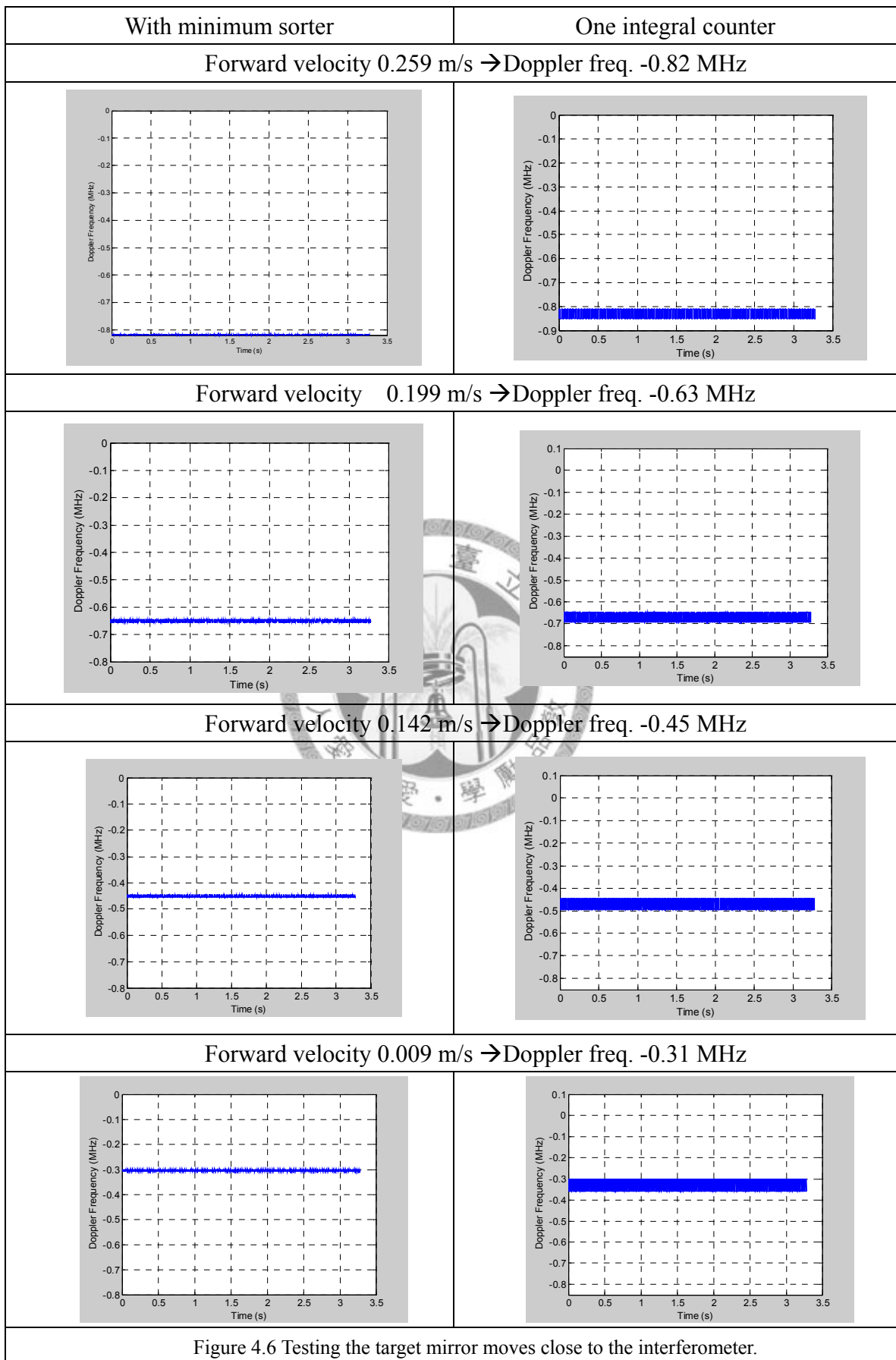


Figure 4.4 Diagram of SignalTap II Analyzer

The testing results are shown on Figure 4.5 and Figure 4.6. The central frequency fed into the reference phasemeter here is 4 MHz. The measurement signal frequency range from 3.18 MHz to 4.8 MHz, which are equivalent to target mirror velocity -0.259 m/s to 0.253 m/s. These two figures also compare the results of the phasemeter with and without the eight integral counters and the minimum sorter. The left side uses the architecture shown in Figure 3.9. The right side uses only one integral





counter and combines with the fractional part directly. The results reveal the minimum sorter method can stabilize and reduce the variation here. The resolution can drop to the time intervals in the octonary phase interpolator and achieve the demanded resolution.

The following is the quantity analysis of above data; the displacement difference means the phase variance compares with the reference signal in every measurement cycle and multiplies the wavelength λ .

About the equation (4.1), considering the relation in Figure 1.3 The detected irradiance amplitude is the proportion of two light wave phase difference. The method for homodyne is detecting the amplitude to acquire the phase difference. And for heterodyne, every period of reference signal represents the heterodyne frequency f_2 chasing upon the heterodyne frequency f_1 , and the reference signal needs $T_{reference}$ to make the f_2 leads the f_1 a full period (λ in displacement). The ΔT and $\Delta\theta$ are caused by the Doppler frequency and the extra phase difference from the moving target mirror. So the $\Delta\theta$ means the proportion of the reference period that f_2 needs to leads the f_1 a full wave. Every time when the measurement frequency and the reference frequency occurs mismatch, the $\Delta\theta$ of the $T_{reference}$ can represents the displacement difference of that cycle by multiplying the wavelength λ [3][12][14].

(4.1)

$$\text{Displacement difference} = \Delta\theta \times \lambda = \frac{\Delta T}{T_{\text{reference}}} \times 631.99 \text{ nm}$$

The displacement difference should be identical in a constant Doppler frequency; however, the difference is limited by the digital circuit's resolution. The RMSE of the displacement difference can represent the average resolution performance of the circuits. Figure 4.7 shows the RMSE in two architectures and under 11 different frequencies. Each frequency has 8192 displacement data, and the result is the RMSE between these displacement data under the same frequency. The result shows the phasemeter with the eight integral counters and the minimum sorter has the average displacement resolution under 1 nm in the on-chip testing. And for the one counter's results, although it connects with the octonary phase interpolator, the average resolution is still around 4 to 5 nm.

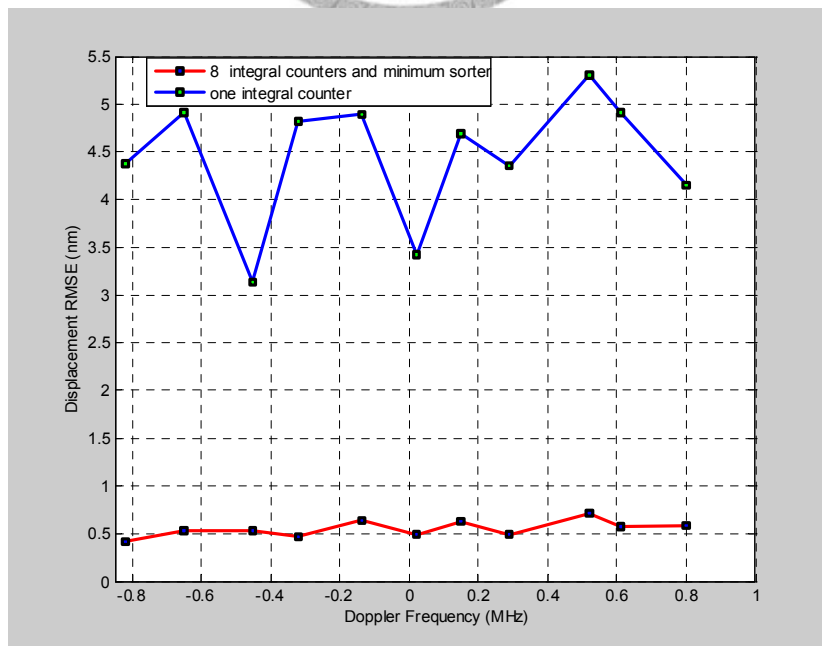


Figure 4.7 RMSE comparison of the displacement difference in 11 different Doppler frequencies.

4.3 Optical System and Function Generator Testing

The optical system setup is shown on the left side of Figure 4.8, the laser light passes through a non-polarizing beam splitter and splits to two lights. The bended light passes through the double passes plane mirror interferometer, which increase an extra resolution in $\lambda/4$. The receiver which picks up the interference light outputs the measurement signal.

The reference signal output from the laser head is shown on the right side of the Figure 4.8. The picture shows the situation of the reference light when light mask of the laser head is closed and open. The laser source and the reference signal here suffer the influence by some indeterminable reasons. One of the suggestions may be the reflection light of the receiver lens re-incident onto the laser head and cause the

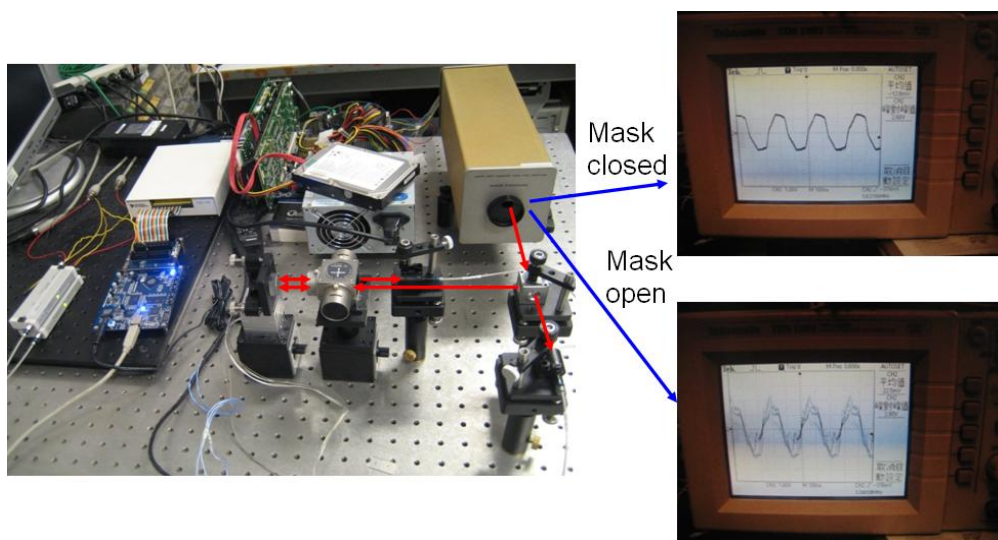


Figure 4.8 The optical setup and the troubles in heterodyne laser source.

influence, but the situation needs to be clarified. Sometimes the laser source can work properly which is not affected by the reflection light. Under this circumstance, the Doppler frequency is taken by the digital interface. The measured Doppler frequency is shown on Figure 4.9 when the stage is stopped. Figure 4.9 also shows that the average of Doppler frequency in this experiment is not 0 exactly. The scope also shows that the frequency comes from reference and measurement signal has a difference about 1 kHz.

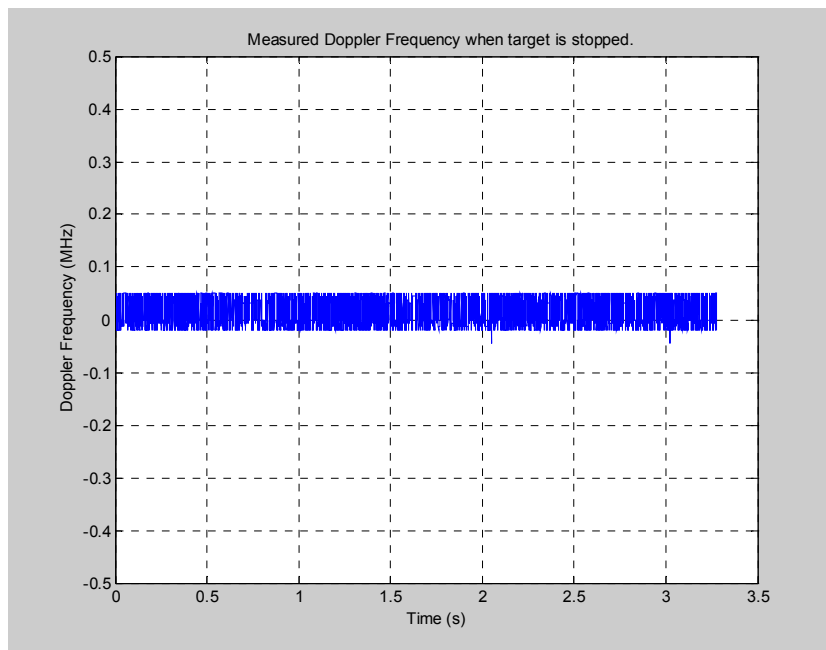


Figure 4.9 The measured Doppler frequency when the target is stopped.

Then the piezo stage below the target mirror is fed on a sine wave with 25 Hz and 10v peak-to-peak signal. The Doppler frequency data is shown on Figure 4.10, it is not sure the velocity information can be acquired by this implicit data directly. The following experiment uses the function generator to pretend the reference and

measurement signal to verify this interface deeply.

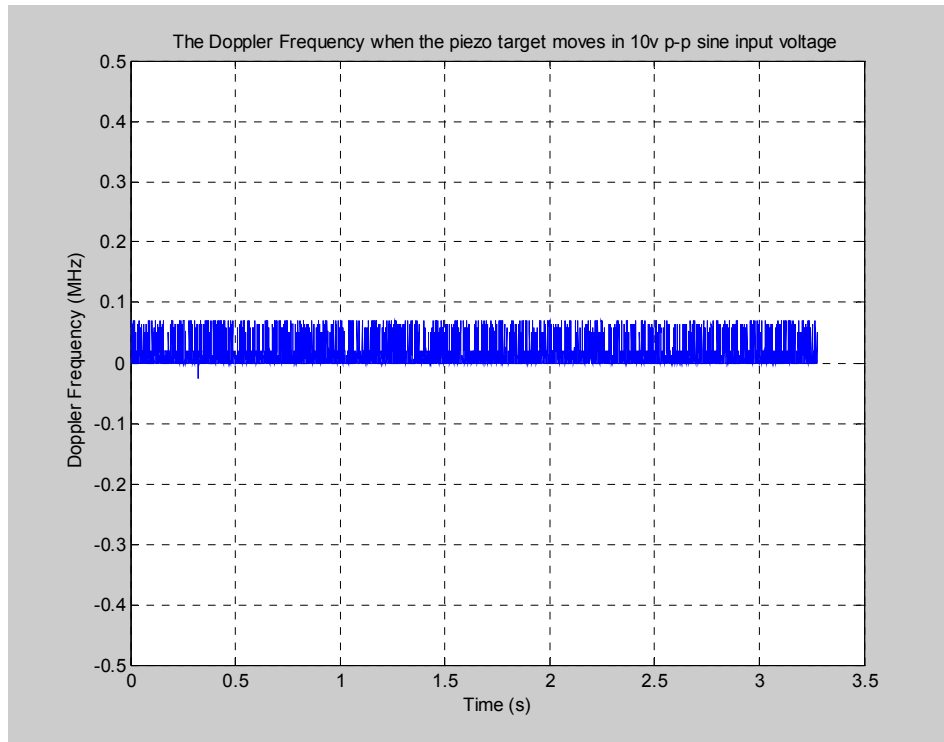


Figure 4.10 The Doppler frequency result in a moving stage

As shown in Figure 4.11, two function generators generate the signals as the pseudo measurement and reference signal. The higher one is Model FG-513 13 MHz Sweep/Function Generator manufactured by American Reliance Inc. This generator provides the square wave in 4 MHz as the reference for the FPGA board. The lower is 33220A 20 MHz Function/Arbitrary Waveform Generator manufactured by Agilent Technology. This one provides the square wave varies from 3.8 MHz to 4.0 MHz with the sweep frequency and 11 different frequencies level testing. The Figure 4.12 shows the frequency data captured by the digital interface. The available frequency range is ± 0.8 MHz, which is equivalent to ± 0.5 m/s target speed without the fold factor. The

interface reacts generally like the setting in the function generator with a little variance. The simulation in previous section is assume as the square wave, but the signal is not perfect signal in MHz frequency, due to the discussion in section 3.5 , the calculated results is not affected by the signal variance if the variance or the timing jitter of the reference of measurement signal is under (reference period/512).

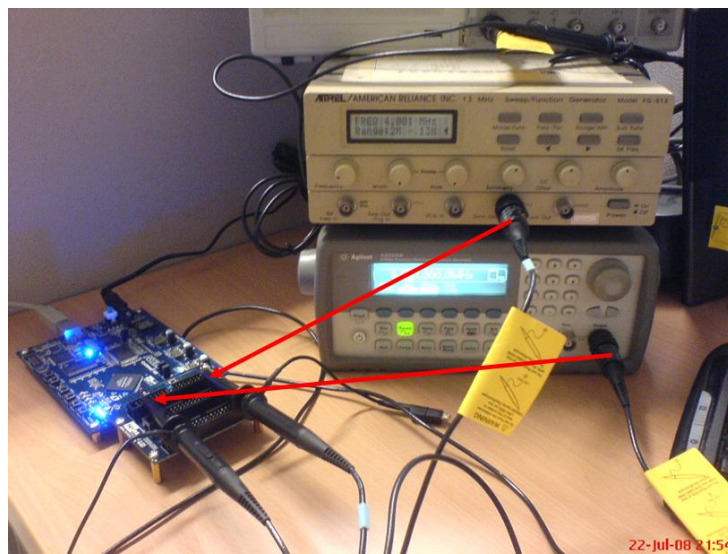


Figure 4.11 The diagram of the function generator testing.

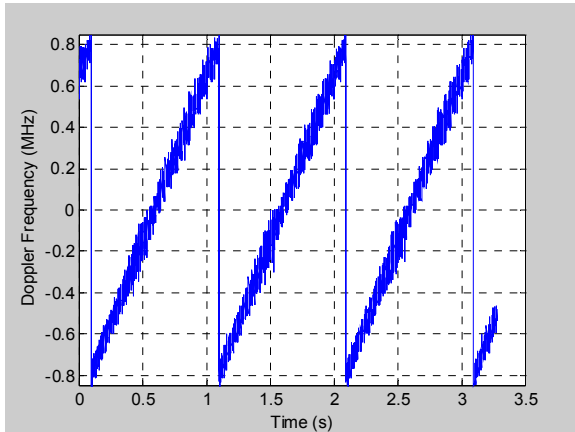
The level testing is shown in Figure 4.13 and Figure 4.14, the different frequencies pretend as the Doppler frequency from the moving target mirror are applied on the digital interface, the results shows the interface capture the frequency indeed but with a big variance. The RMSE is shown in and reveals the resolution here is about 9 nm, the reason that the resolution can't achieve the sub-nanometer scale may come from:

- (1) The glitches from the integral counter can't be canceled clearly through this method.

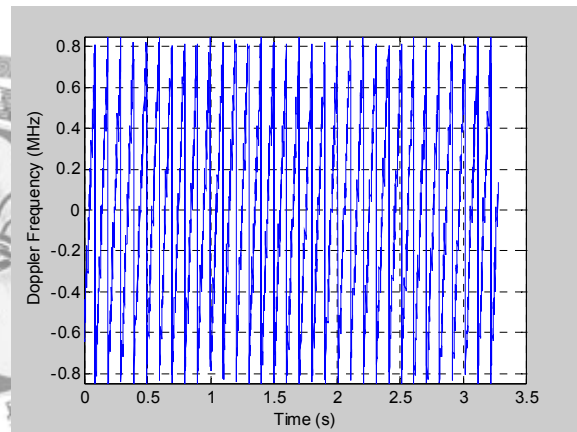
(2) The clock transmission line is not protected well and causes the noise to affect the frequency detection.

Although the testing results are not as expected, this digital interface can also provide $\lambda/64$ resolution under this testing.

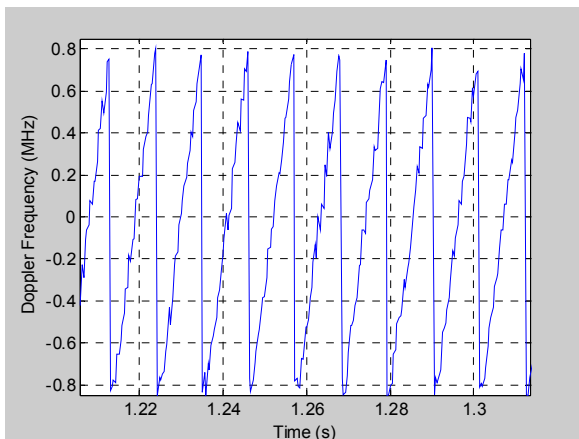
Doppler Frequency varies from 0.8 MHz to -0.8 MHz
sweep in 1 sec.



Doppler Frequency varies from 0.8 MHz to -0.8 MHz
sweep in 100 msec.



Doppler Frequency varies from 0.8 MHz to -0.8 MHz
sweep in 10 msec.



Doppler Frequency varies from 0.8 MHz to -0.8 MHz
sweep in 5 msec.

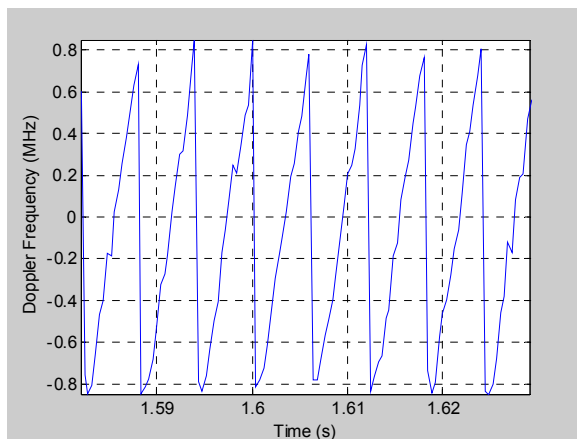
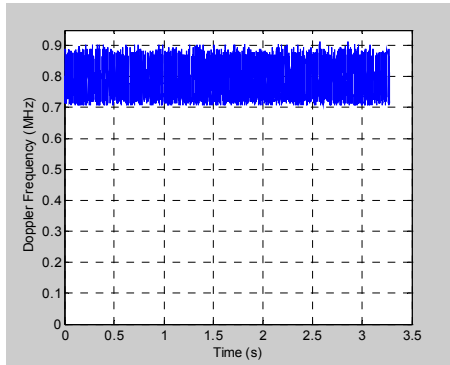
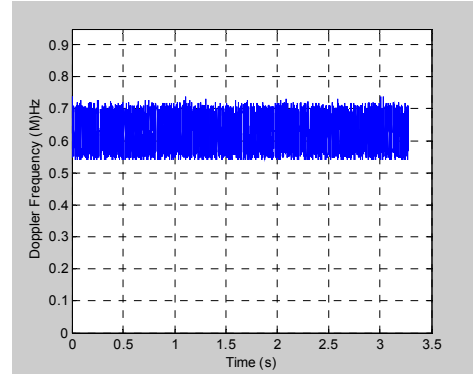


Figure 4.12 The captured Doppler frequency in the function generator sweep mode.

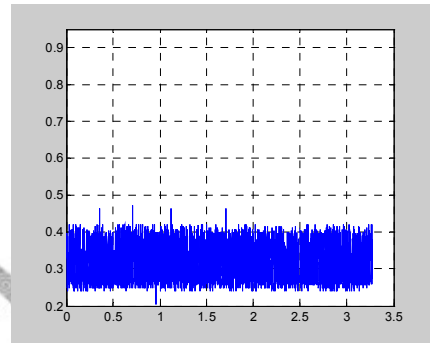
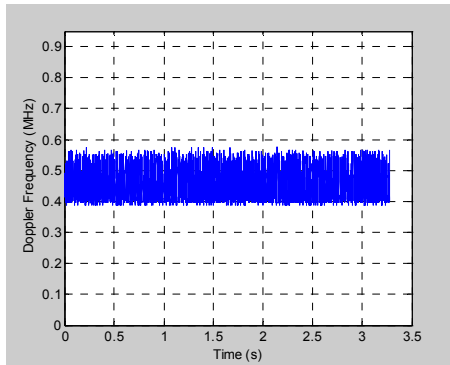
Backward velocity 0.253 m/s, Doppler frequency 0.8 MHz



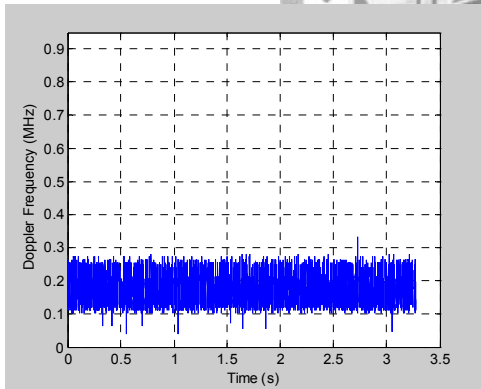
Backward velocity 0.202 m/s, Doppler frequency 0.64 MHz



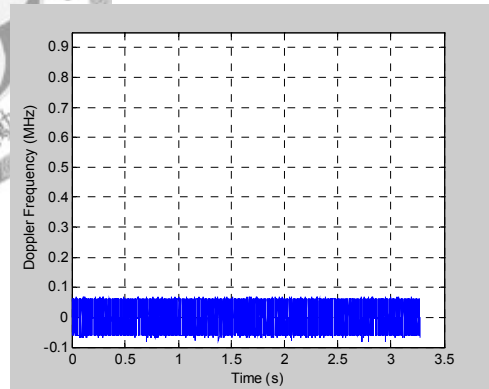
Backward velocity 0.152 m/s, Doppler frequency 0.48 MHz Backward velocity 0.101 m/s, Doppler frequency 0.32 MHz



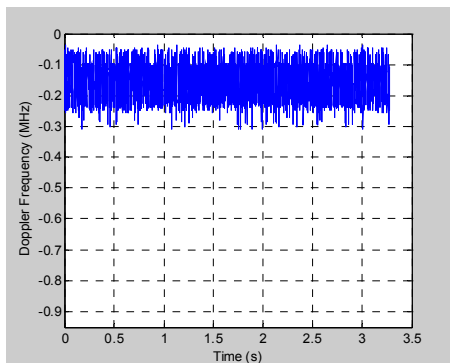
Backward velocity 0.051 m/s, Doppler frequency 0.16 MHz



Target Mirror stops, Doppler frequency around 0 Hz



Forward velocity 0.051 m/s, Doppler frequency -0.16 MHz



Forward velocity 0.101 m/s, Doppler frequency -0.32 MHz

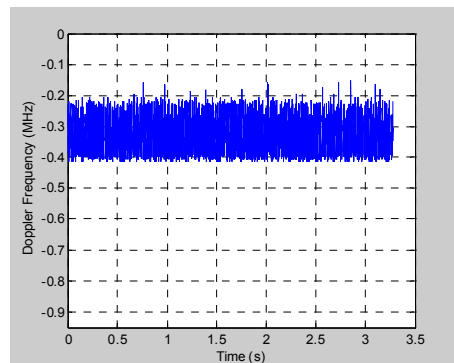
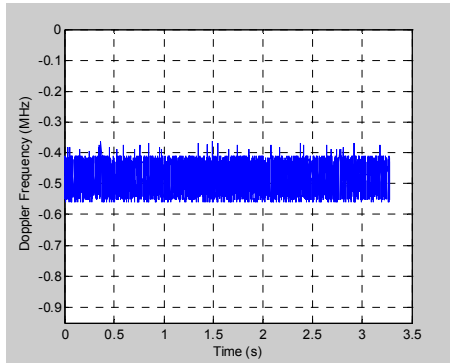
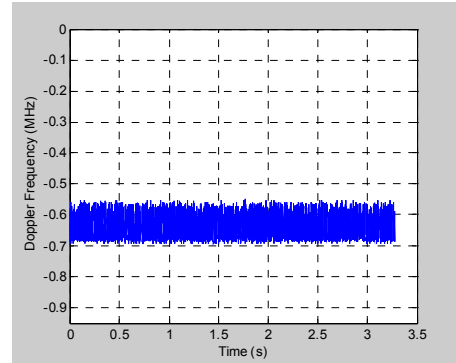


Figure 4.13 The function generator testing from -0.32 MHz to 0.8 MHz

Forward velocity 0.152 m/s, Doppler frequency -0.48 MHz



Forward velocity 0.202 m/s, Doppler frequency -0.64 MHz



Forward velocity 0.253 m/s, Doppler frequency -0.8 MHz

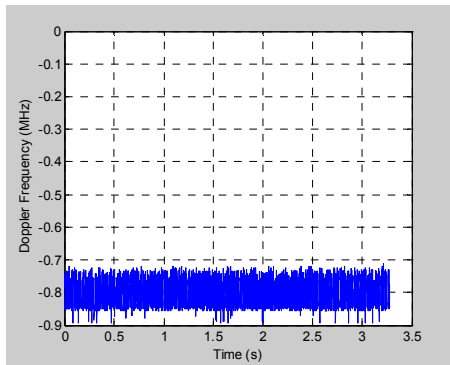


Figure 4.14 The function generator testing from -0.8 MHz to -0.48 MHz

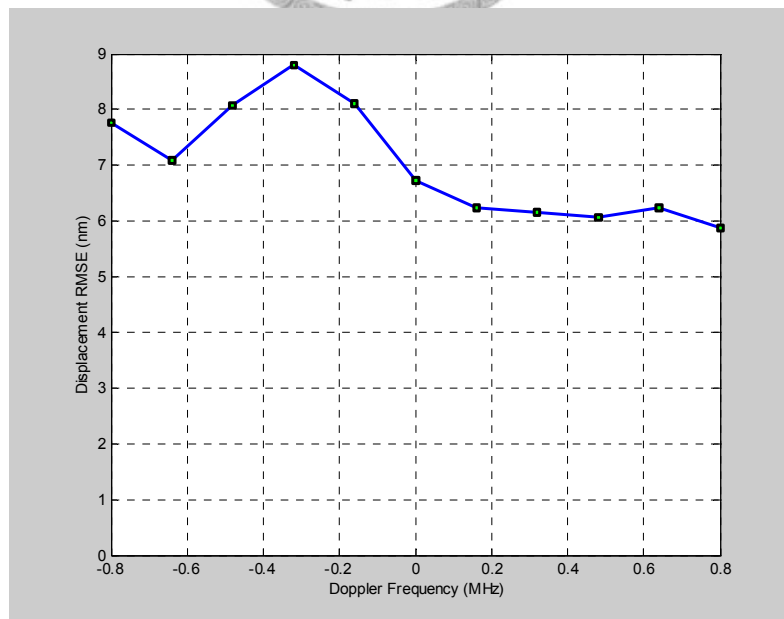


Figure 4.15 The function generator testing RMSE in 11 different Doppler frequencies.

Chapter 5

Conclusion and Future work

In this research, a digital interface designed for heterodyne interferometers is developed. This design implementation passes gate-level simulation and on-chip testing. It provides a good displacement resolution with sufficient measurement velocity. An innovative octonary phase interpolator for Agilent laser interferometer is proposed. In function generator testing, the octonary phase interpolator doesn't react as expectation, but the interface also performs the resolution in $\lambda/64$ due to the 64 times faster clock speed than the reference signal.

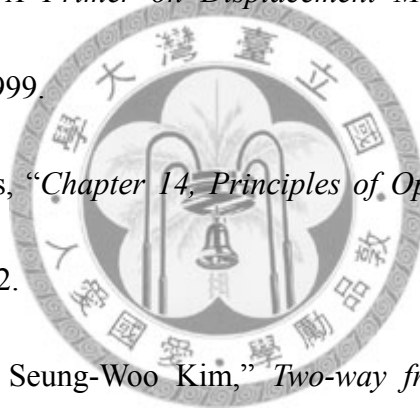
The optical trouble affects the signal purity and makes it hard to detect the stage motion; this trouble may be caused by the reflected light of the receivers lens and induces the resonation in laser source. However, this trouble needs more verification in future works and applied to this interface.

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