國立臺灣大學電機資訊學院電子工程學研究所

博士論文

Graduate Institute of Electronics Engineering
College of Electrical Engineering & Computer Science
National Taiwan University

Doctoral Dissertation

用於植入式生醫用途具高能量效率之 400MHz 射頻收發器設計

Design of 400-MHz Energy-Efficient RF Transceivers for Bio-medical Implantable Applications

劉耀鴻

Yao-Hong Liu

指導教授：林宗賢 博士

Advisor: Tsung-Hsien Lin, Ph.D.

中華民國 98 年 8 月

Aug., 2009

國立臺灣大學博士學位論文
口試委員會審定書

用於植入式生醫用途具高能量效率之 400MHz 射頻收發器設計
Design of 400-MHz Energy-Efficient RF Transceivers for Bio-medical Implantable Applications

本論文係劉耀鴻（D93943017）在國立臺灣大學電子工程研究所完成之博士學位論文，於民國 98 年 7 月 20 日承下列考試委員審查通過及口試及格，特此證明

口試委員：

_____（指導教授）

_____ _____

_____ _____

_____ _____

系主任、所長 _____

Design of 400-MHz Energy-Efficient RF Transceivers for Bio-Medical Implantable Applications

By

Yao-Hong Liu

Dissertation

Submitted in partial fulfillment of the requirement
for the degree of Doctor of Philosophy
in Graduate Institute of Electronics Engineering
at National Taiwan University
Taipei, Taiwan, R.O.C.

Jul. 2009

Approved by :

Jiel Tsorng Wu _____ _____

_____ Jeny Chin Shen-Iuan Liu

_____ Kro-Hig Cheng _____

Advised by : _____

Approved by Director : _____

謝辭

在此感謝在博士班就讀一路上幫助我的人，讓我可以順利的拿到學位。首先是指導教授林宗賢博士，不但在專業上給予我許多寶貴的意見，經由他的指導讓我可以在專業領域上看的更寬廣；也謝謝一起共事多年的部門主管曾英哲博士，由於他在這幾年中的鼓勵和支持，讓我可以不用擔心經濟狀況下半工半讀的完成學位；另外也向背後默默支持我的女友(盈辰)表達心裡的感激，總在我低潮時陪著我，是我這段時間最重要的心靈支柱；最後感謝我的家人給予我的一切及他(她)們無條件的支持。

Acknowledgement

I would like to thank the people who helped me through the way in obtaining my Ph.D. degree. First, I would like to thank my advisor, Dr. Tsung-Hsien Lin, for offering me many valuable opinions and helping me to see the mixed-signal IC design from a broader perspective. Then, I want to thank my supervisor whom I have worked together for many years, Dr. Y.-C. Tseng, for his encouragement and support through out my Ph.D. study. Most important, I appreciate my girl-friend (Ingrid) for always being there for me especially when I was disheartened; she was the most important supporter during this time. Finally I want to thank for my family, for everything and their unconditional supports for me.

中文摘要

在本篇論文中將介紹一個可用於植入式醫療用途之低功率射頻收發器。此收發器操作在 400MHz 的頻段，且在上傳及下傳的路徑上採用不同的調變方式以及傳輸率來達到最佳化。在下傳路徑上使用一個 156kbps 的 ASK 接收器，而在上傳路徑上則使用 6Mbps GFSK、17.5Mbps OQPSK 以及 25Mbps HS-OQPSK 三種發射器架構。**第一章**及**第二章**將先討論我們預定使用的醫療用途及收發器設計考量。**第三章**則介紹了常用的低功率收發器架構，包括超再生式接收器以及鎖相迴路式及混波器式直接調變發射器。

第四章首先會介紹用於下傳接收上，採用一個具有"三角積分脈寬數位器"之超再生式 ASK 接收器。此三角積分脈寬數位器是相當於用於脈寬領域上之三角積分調變器，它可以達到 0.23ns 的脈寬偵測解析度。整體接收器消耗 900 μW，在 156kbps 的接收率時可以達到-78dBm 的接收靈敏度。

然後在**第五章**及**第六章**將會分別介紹用於上傳發射之 FSK/PSK 雙模發射器。首先，**第五章**討論一個可做 G/FSK 上傳調變之"三角積分相位旋轉器"。經由適當的選去鎖相迴路輸出之多項位訊號，此三角積分相位旋轉器可以等效合成具有高頻率解析度之頻率調變器。此 G/FSK 發射器消耗 9mW 且可輸出-11dBm 的功率，在最大 6Mbps 的傳輸率下可達到 1.5nJ/bit 的能量效率。然而在**第六章**則介紹一個 OQPSK 發射器，它可以使用三角積分相位旋轉器中的"相位選擇器"，直接選擇四相位訊號中的其中一相位輸出來達成 OQPSK 調變。此 OQPSK 發射器消耗 3.5mW，在最大 17.5Mbps 的傳輸率時此發射器可以達到 200pJ/bit 的能量效率並可輸出-8dBm 的輸出功率。

為了更進一步的改善 OQPSK 發射器的頻譜效率，**第七章**提出一個將"內嵌 FIR

之相位選擇器”來將 OQPSK 調變做時域半弦濾波，因此可以將 OQPSK 調變之旁帶能量降低。此發射器架構消耗 1.4mW(不含鎖相迴路)且可達到最大 25Mbps 的傳輸率。最後，**第八章**將會提供此論文的總結。

關鍵字: 植入式生醫元件; 低功率射頻收發器; 超再生接收器; 三角積分; 頻率合成器; 鎖相迴路; FSK; PSK; Half-sine shaping OQPSK。

Abstract

A low-power radio transceiver designed for implantable medical applications is presented in this dissertation. These transceivers operate at around 400-MHz band and utilize different modulation schemes and data rate between downlink and uplink. A low-data-rate ASK RX is presented for downlink reception; while high-data-rate GFSK, OQPSK and HS-OQPSK TXs are demonstrated for uplink transmission. **Chapter 1** and **Chapter 2** will firstly discuss the targeted medical applications as well as the design requirements for the medical transceivers.

In **Chapter 3**, several low-power transceiver architectures are introduced, including a super-regenerative receiver, mixer-based and PLL-base direct-modulation transmitters.

Downlink reception adopted a super-regenerative ASK RX with a proposed Delta-Sigma Pulse-Width-Digitizer (ΔΣ-PWD) will be presented in **Chapter 4**. The ΔΣ-PWD can be considered as a pulse-width-domain counterpart of a conventional Delta-Sigma modulator which can suppress quantization jitter by 22 dB and achieve a pulse-width detection resolution of 0.23 ns. The whole receiver consumes 900 μW. With a 156-kbps data rate, the RX achieves -78-dBm sensitivity.

Chapter 5 and **Chapter 6** will then present a MUX-based dual-mode uplink TX. First, a Sigma-Delta Phase Rotator (ΣΔ-PR) designed for G/FSK uplink transmission is discussed in **Chapter 4**. By properly combining the multi-phase signals from the PLL output, the ΣΔ-PR can effectively synthesize frequency modulation signals with fine-resolution frequencies. The proposed G/FSK TX consumes 9 mW and delivers

-11-dBm output power. With a maximum data rate of 6-Mbps, the G/FSK TX achieves 1.5-nJ/bit energy efficiency. **Chapter 6** presents an energy-efficient OQPSK TX which can also be implemented with the ΣΔ-PR proposed in **Chapter 5**, by directly selecting one of the quadrature phases through the Phase MUX. The whole OQPSK TX dissipates 3.5 mW. With a maximum data rate of 17.5 Mbps, the OQPSK TX achieves an energy efficiency of 200 pJ/bit and is capable of delivering an output power up to -8 dBm.

In order to further improve the spectral efficiency of previous MUX-based OQPSK transmitter, **Chapter 7** proposed a FIR-embedded Phase-MUX which allows to half-sine shape the OQPSK modulation; thus reducing the side-lobe energy of OQPSK modulation. The proposed HS-OQPSK TX (without PLL) consumes 1.4 mW and achieves 25-Mbps data rate. Finally, **Chapter 8** will summarize and conclude this dissertation.

Key words: bio-medical implantable devices; low-power RF transceivers; super-regenerative receivers; sigma-delta; frequency synthesizers; phase-locked loop (PLL); FSK; PSK; Half-sine shaping OQPSK.

Contents

List of Figures

List of Tables

Chapter 1
Introduction

1.1 Implantable Bio-Medical Applications

The physical sizes of many bio-medical instruments are scaled down significantly, owing to the advancement in various technology areas. The miniaturization of these devices has brought convenience and efficiency in many medical applications. Coupled with rapid progress of semiconductor and wireless communication technologies, small form factor also opens new opportunities for emerging implantable medical devices. This implanted device demands bi-directional wireless data telemetry for signal transmission as well as command reception.

The transmission bandwidth of general bio-medical signal is typically below several kHz. On the other hand, some real-time medical signal transmissions require very high throughput (e.g. several MHz), such as medical image or multi-channel neural signals. The low transmission data rate and high power consumption of the general consumer low-power radios designed for Bluetooth or Zigbee are not feasible for such applications. This chapter will introduce these implantable applications which requiring wideband transmission.

1.1.1 Wireless Capsule Endoscope

One noticeable example is the capsule endoscope system [1], as shown in Fig. 1-1. IMD denotes the implant device, whereas EXD denotes the external device. The swallowable device captures a human body's internal images and transmits the data via wireless interface. Such devices eliminate the need of a cable attached to the medical sensors, thereby greatly improves patient's comfort level.

One major design challenge associated with these implantable devices is to extend their operation lifetime under limited energy source (e.g. a Li-cell battery). Therefore, low-power realization is a primary design goal. In particular, the wireless communication module often dissipates a significant amount of power.

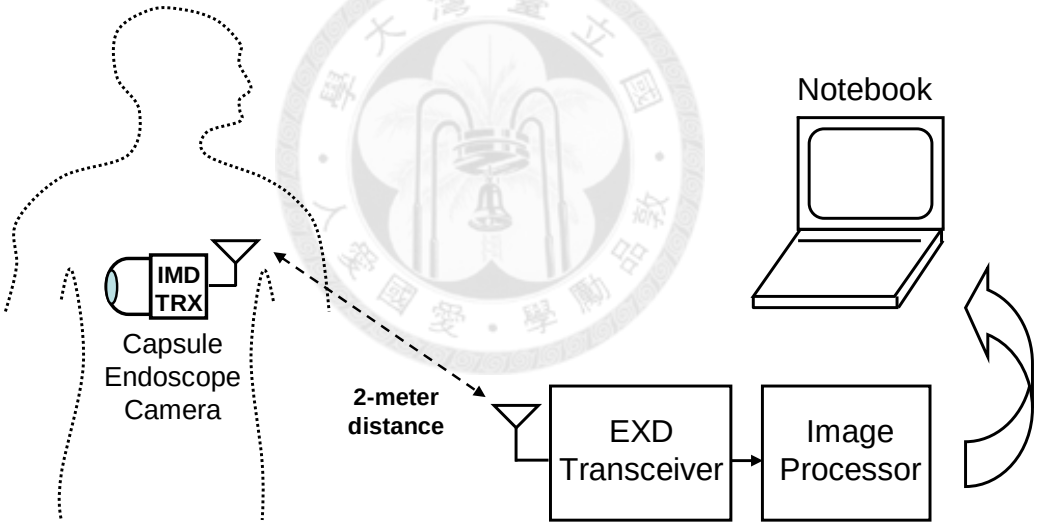


Fig. 1-1: Wireless capsule endoscope system

1.1.2 Multi-Channel Neural Recording

The real-time multi-channel neural recording system incorporates arrays of miniature *in-vivo* Micro-Electrical-Mechanical System (MEMS) electrodes for neural signal detection, as shown in Fig. 1-2, for the implanted electrodes have the advantages of lower infection risk and less signal interference compared with that of the

conventional *ex-vivo* electrodes [2]. However, the large amount of collected raw data posts great challenges on the design of the implanted transmitters. While various compression or sorting techniques [3, 4] can be applied to reduce the amount of neural information, high transmission data rate is still desirable to support simultaneous multi-channel recording. In addition, these transmitters must consume low power and be energy efficient to enable a long operation lifetime.

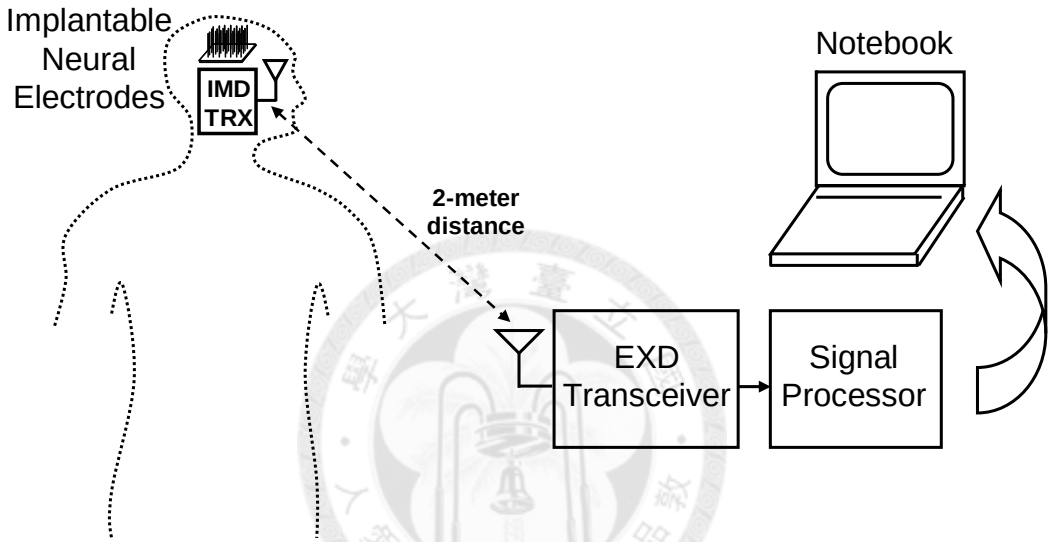


Fig. 1-2: Implantable multi-channel neural recording system

1.2 Dissertation Organization

To address these challenges mentioned above, this dissertation presents a low-power receiver as well as several high-data-rate transmitters designs. This dissertation is organized as follow. Chapter 2 discusses the transceiver design requirements for these implantable applications. Chapter 3 introduces several RF transceiver architectures. Implantable wireless receiver design with proposed pulse-width digitizer is presented in chapter 4. In chapter 5 and 6, the proposed G/FSK and OQPSK transmitter architectures are individually introduced. The Half-sine

shaped O-QPSK transmitter with a FIR-embedded Phase MUX design is proposed to improve spectral efficiency will be discussed in chapter 7. Finally, Chapter 8 is the conclusion.

Chapter 2
Wireless Interface and Design Requirements

2.1 Asymmetrical Transceiver Architecture

For medical applications requiring wideband transmission, the data communication is typically asymmetrical. The implant device needs to turn-on periodically for listing and receiving "simple" commands to control its operation from external device; while the collected data to be transmitted outwards is often much larger. A conventional wireless link employing same uplink and downlink signaling scheme is not energy-efficient in such application scenario. This work incorporates the asymmetrical characteristics into the system design and proposes an asymmetrical wireless link to achieve optimal performance. The proposed wireless interface system is depicted in Fig. 2-1.

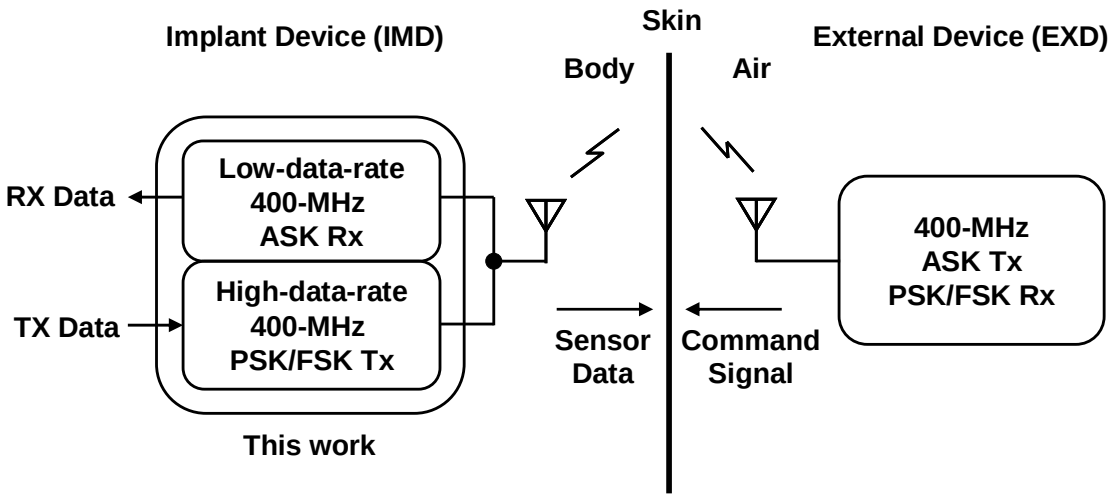


Fig. 2-1: Asymmetrical transceiver architecture

The IMD receiver employs an amplitude modulation method – On-Off Keying (OOK) for its low-power consumption and fast turn-on time. Although amplitude modulation is in general less sophisticated, it is fit for ultra-low-power operation because of the low circuit complexity. In addition, the start-up time of OOK receiver is generally fast since PLL is not required in this system, making it suitable for IMD receivers which are usually highly duty-cycled for periodic sniffing.

On the other hand, low power and supporting large data rate are two major considerations in selecting IMD transmitter signaling approach. In the proposed system, FSK and PSK modulation scheme are adopted. Owing to the constant envelop characteristic and the relatively simple modulator designs, FSK and PSK are well-suited for a low-power transmitter.

On the low-power transceiver design, this work proposes a novel FSK/PSK dual-mode transmitter as well as the OOK receiver realized in a super-regenerative architecture.

2.2 Data Rate Requirements

The IMD receiver data rate requirement is not critical since the implant devices control require fewer bits. In this system, a minimum of 150 kbps is specified in this system.

On the other hand, the transmission data rate, capsule endoscope system for example, depends on the image quality, frame rate, and the image compression ratio, as expressed in (2-1). Assuming 8-bit 256×256-pixel color images with 10 fps (frames/sec), and 5:1 image compression ratio, the required IMD transmitter data rate is calculated to be 3.15 Mbps.

$$Data\_rate = \frac{bits\_num \times pixels \times fps \times 3(RGB)}{compression\_ratio} \quad (2\text{-}1)$$

In a neural recording system, the requirement for uncompressed transmission data rate is mainly determined by the number of simultaneous recording channels, and the resolution and sampling rate of the analog-to-digital converter (ADC) in each channel [2], as expressed below.

$$Data\ rate = channel\ num \times sampling\ rate \times bit\ num \quad (2\text{-}2)$$

In this implementation, assuming the implanted transmitter is designed for a system with a maximum of 64 simultaneous recording channels and each channel is sampled at 8-kSample/s with an 8-bit resolution. Therefore, the transmitter must be capable of delivering a data rate exceeding 4.1 Mbps.

2.3 Operation Frequency Band for Implantable Transceivers

The selection of operation frequency for an implanted transceiver must consider signal propagation characteristics of human body, circuit power consumption, and implantable antenna size. The proposed wireless transceiver is designed to operate at around 400-MHz frequencies [5]. This frequency range is chosen primarily because the signal propagation characteristics in an implanted environment at 400-MHz band are better than other available frequency bands (e.g. 900-MHz or 2.4-GHz ISM bands) [6], and the circuit power consumption is also likely reduced, while transmission range is increasing compared to working at GHz range. On the other hand, compare to the conventional low-frequency magnetic-coupled medical telemetry system [7], operating at higher radio frequency allows smaller antenna size, larger signal bandwidth.

The proposed 400-MHz transceiver is capable of compliance with the frequency band allocated by FCC in 1999, Medical Implant Communications Service (MICS), which operates at the 402 to 405 MHz MICS band. The 3-MHz band is divided into 10 channels; each occupies 300-kHz bandwidth, as shown in Fig. 2-2. The output power is limited to 25 μW to minimize interference with others and to avoid causing heat damage to human body [8].

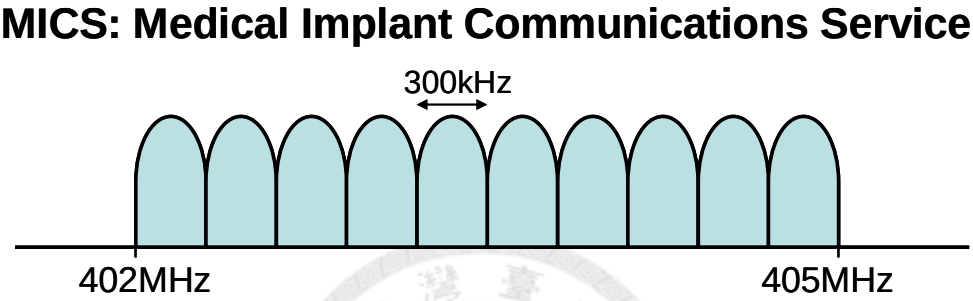


Fig. 2-2: Medical Implant Communications Service (MICS) band

2.4 Modulation Schemes

In many low-power low-data-rate wireless communication systems for bio-medical applications, Amplitude-Shift-Keying (ASK) modulation is often used because of its low-power consumption and fast turn-on time. Therefore, this modulation is implemented in downlink path for its stringent power consumption requirement and duty-cycled operation.

However, ASK signal has a poor immunity to channel noise [9], which makes it impractical for the high-data-rate uplink transmission. In this regard, Frequency-Shift-Keying (FSK) and Phase-Shift-Keying (PSK) signaling schemes are more robust and appropriate even though they require more complicated hardware. Furthermore, the constant-envelope characteristic of the FSK and PSK signals enables the incorporation of a power-efficient non-linear power amplifier (PA) in the transmitter

[10]-[12]. Even with these benefits, limited energy source still poses great challenges on the transmitter design.

Fig. 2-3 compares the simulated signal-to-noise ratio (SNR) requirements for OOK, FSK and PSK demodulators. It shows that the FSK modulators must deliver slightly higher output power than PSK modulation to satisfy a given SNR requirement. For example, to satisfy a 10^{-4} bit-error-rate (BER) requirement, a FSK transmitter needs to provide 3-dB higher output power than a PSK transmitter does. On the other hand, FSK modulation has an advantage of easier demodulation circuit implementation. Therefore, this work presents a dual-mode FSK/PSK transmitter for higher flexibility on modulation.

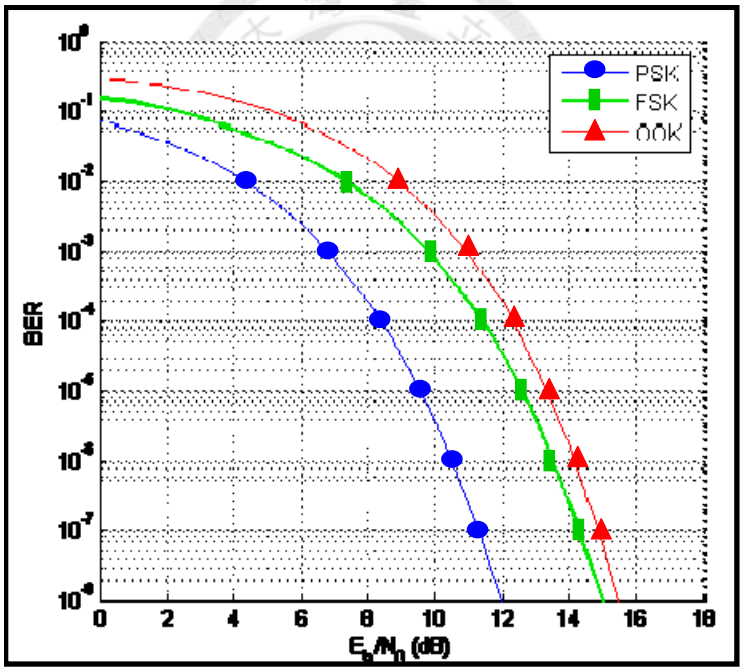
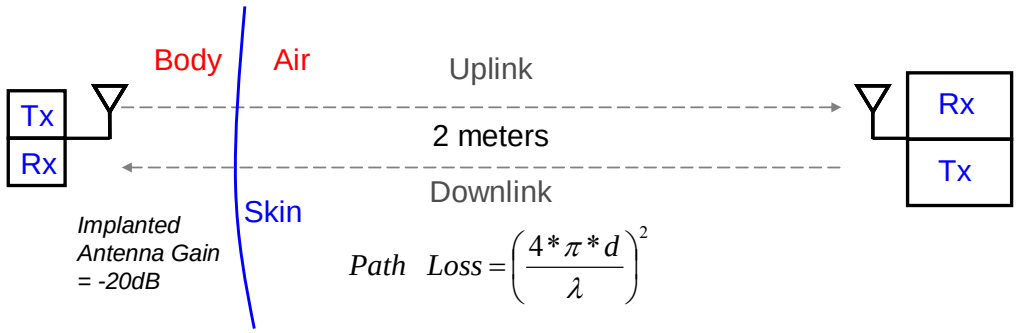


Fig. 2-3: Simulated BER versus E_b/N_0 for PSK and FSK modulations

2.5 Link Budget Analysis

The radio design requirements are derived and estimated through link budget analysis, as depicted in Fig. 2-4. The path loss due to signal propagation can be

estimated by the free-space path loss equation shown in (2-3) [13].



-15 dBm	-20 dB	-20dB	➔ -30 dB	-85 dBm	Uplink
-60 dBm	-20 dB	-20 dB	← -30 dB	10 dBm	Downlink
	Antenna Gain	Skin/air interface	2-meter free-space path loss		

Fig. 2-4: Link budget of the proposed wireless interface

$$Path\ Loss = \left(\frac{4*\pi*d}{\lambda}\right)^2 \qquad (2\text{-}3)$$

In (2-3), λ is the wave-length. d is the distance between transmitter and receiver and is specified at 2 meters in this work. In addition, assuming an excess loss of 40 dB due to fading, skin-air interface and a worst-case antenna loss of 20 dB, the total path loss is estimated to be 70 dB.

For downlink, the EXD transmitter output power is limited to 10 dBm in order to avoid causing heat damage to human body, then the received power at the IMD receiver input calculated to be -60 dBm by equation (2-4) as expressed below (in dB):

$$P_{RX\_Signal} = P_{TX} - Path\ Loss - Ant.\ Loss - Skin\ Loss \qquad (2\text{-}4)$$

In addition, the SNR requirement for ASK modulation to achieve bit-error-rate of 10^{-4} is around 10 dB; then the required sensitivity for IMD receiver is estimated to be around -70 dBm.

On the other hand, for uplink, if the IMD transmitter output power is -15 dBm, then the received power at the external receiver input is calculated to be -85 dBm by using

(2-4). Assuming the EXD receiver NF is 6 dB and the maximum occupied signal bandwidth is 35 MHz at maximum data rate of 17.5 Mbps, the noise floor of the external receiver can be estimated by using (2-5) (where N_0 is the thermal noise power density, -174 dBm/Hz), which is around -92 dBm.

$$P_{RX\_Noise} = N_0 + 10 \times \log(BW) + RX\ \ NF \tag{2-5}$$

Therefore, the SNR at EXD receiver output is around 7 dB. As illustrated in Fig. 2-3, a 7-dB SNR (corresponding to 10-dB E_B/N_0 with bandwidth efficiency of 0.5) is adequate for G/FSK or O-QPSK demodulator to achieve a bit error rate much lower than 10^{-4}.

Chapter 3
Introduction to Low-Power RF Transceiver Architectures

This chapter will introduce several low power transceiver architectures, including super-regenerative receiver, PLL-based and mixer-based direct conversion transmitters. In addition, this chapter will also discuss the design issues and limitations in these architectures.

3.1 Super-Regenerative Receiver Architecture

The super-regenerative receiver architecture was proposed in 1922 by Armstrong [16]. Fig. 3-1(a) shows the simplified block diagram of super-regenerative receiver. The low noise amplifier (LNA) magnifies the input RF power and converts it into a current, which then injects into the periodically quenched oscillator (OSC) to produce input-dependent oscillation envelopes. The envelope of the oscillator is then converted into pulses whose width bears the input information by the following Envelope Detector. The quench clock (V_Q) is generated by Quench Timing Controller, as shown in Fig. 3-1(b). When V_Q is low, the oscillator is turned off; while the oscillator is turned on when V_Q is high. The start-up time ($T_{Start\text{-}up}$) of the quenched oscillator is theoretically proportional to the receiver input power (in dBm), which can be expressed as [17]

$$T_{Start-up} = T_{noise} - K \cdot (P_{RFIN} - P_{noise}) \quad (3\text{-}1)$$

Where the parameter *K* represents the input-power-to-pulse-width conversion gain of a quenched oscillator, T_{noise} is the required start-up time when input RF power (P_{RFIN}) is at the sensitivity level (P_{noise}). Equation (3-1) shows that the start-up time of the quenched oscillator is affected by the input power of super-regenerative receiver, making the pulse width of oscillator proportional to the input power in dBm. Therefore, the ASK modulation signal can be demodulated by detecting the pulse-width information of super-regenerative receivers.

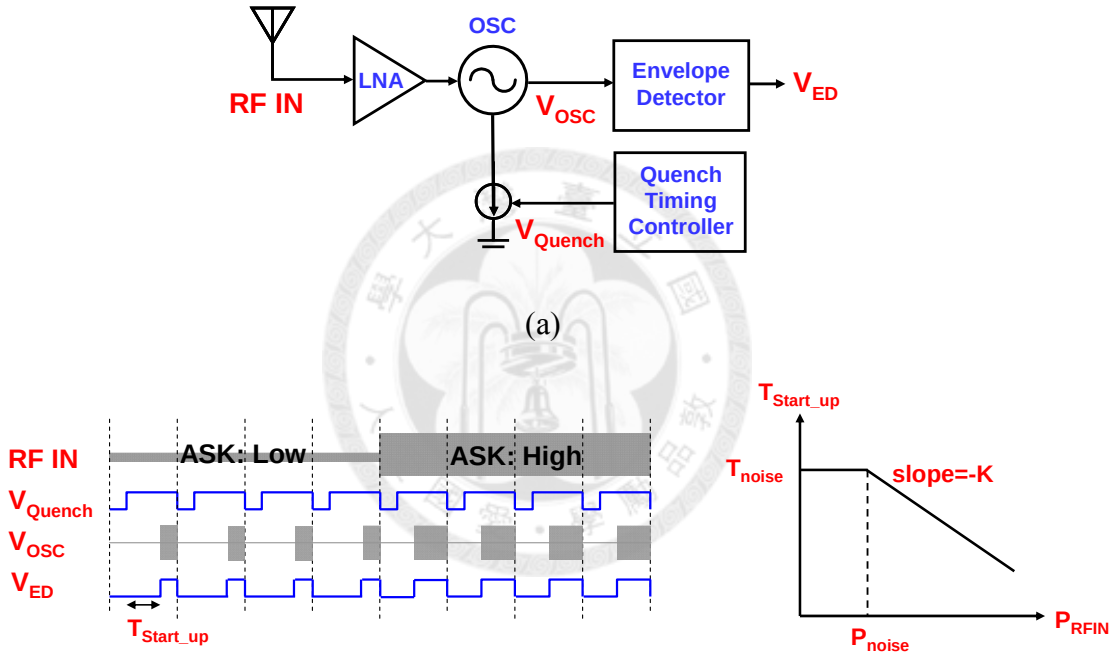
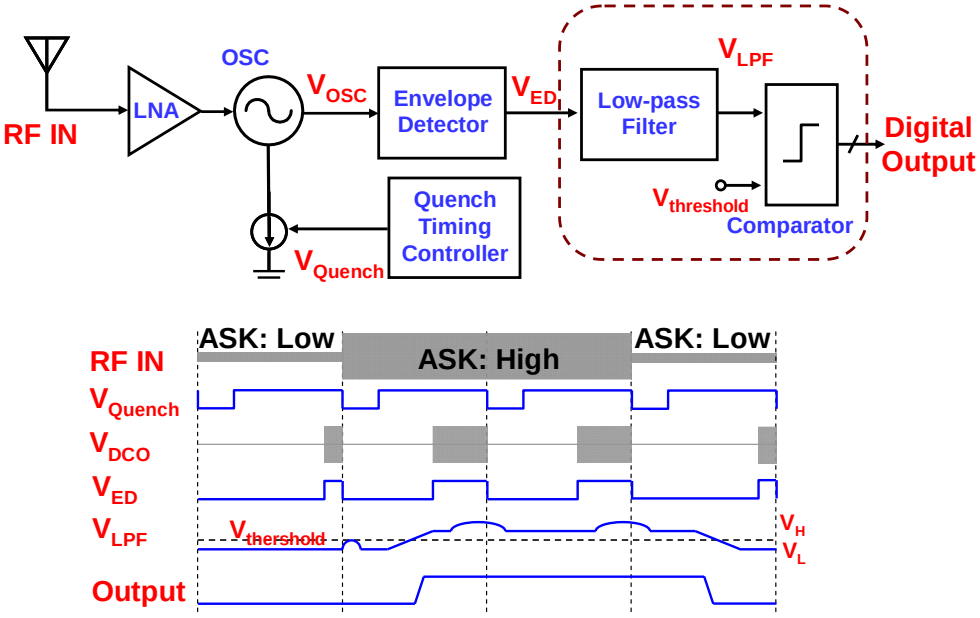


Fig. 3-1: (a) Simplified schematic of a super-regenerative receiver, (b) operation principle of a super-regenerative receiver

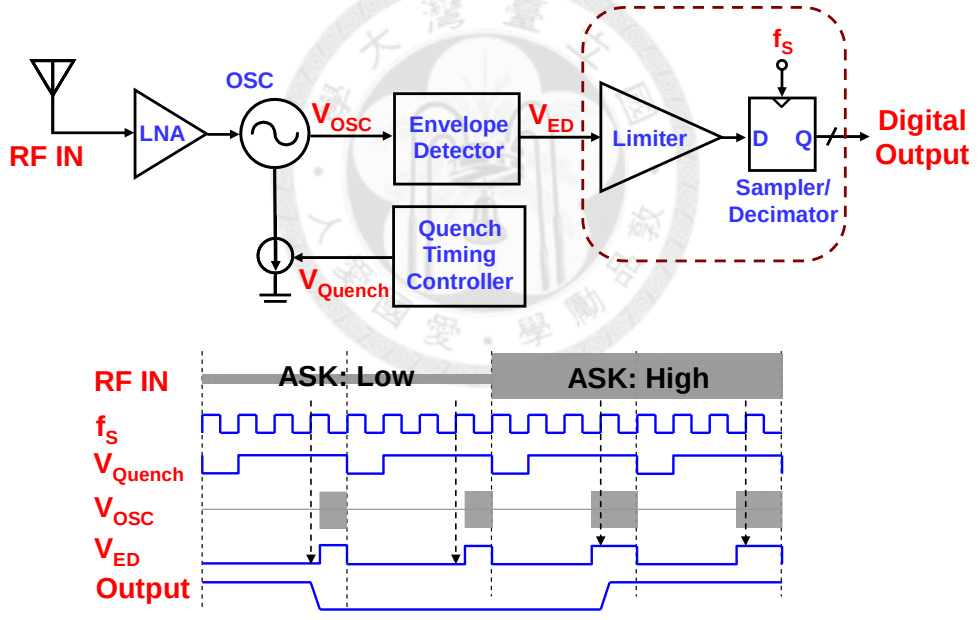
Detecting the pulse width with fine resolution is critical in correctly demodulating the input amplitude modulation signal without degrading the receiver sensitivity. Various methods exist for pulse-width detection. The low-pass filtering method [17, 18], as shown in Fig. 3-2(a), process the pulse-width information in voltage domain. The pulse-width signal is first averaged by a low pass filter to extract the DC voltage (V_{LPF});

then it is compared by a voltage comparator with the threshold voltage ($V_{threshold}$). Assuming the low-pass filtered voltage at ASK high and ASK low value are V_H and V_L, as illustrated in Fig. 3-2(a). An analog AGC loop is implemented as in [17] can be used to regulate the $(V_H+V_L)/2$ to be equal to $V_{threshold}$. However, the mismatch between $V_{threshold}$ and $(V_H+V_L)/2$ will limit the resolution of the pulse-width detection. In addition, the smoothness of low-pass-filtered pulse signal also affects the resolution of pulse-width detection, which can be achieved by extracted over many quench periods, resulting in a trade-off between resolution and conversion speed.

On the other hand, the direct-sampling method [19, 20, 21], as shown in Fig. 3-2(b), is favorable in low-voltage deep-submicron technologies since it process the data in time domain. First, this circuit hard-limits the OSC output envelope; it is then directly sampled by a high frequency sampling clock (f_S). However, the resolution of the pulse-width detection is severely limited by jitter and insufficient sampling frequency. In addition, jitter is introduced by circuit noise of super-regenerative receiver and sampling clock source. Although the resolution degraded by jitter can be relaxed by averaging the results over several quench periods (at the cost of data rate); insufficient sampling frequency is still the dominant resolution limitation in this method. For instance, to achieve a 10-ns pulse-width detection resolution for a typical super-regenerative receiver requires at least 100-MHz sampling clock frequency.



(a)



(b)

Fig. 3-2: Super-regenerative receivers with a conventional pulse-width digitizer; (a) low-pass filtering method, (b) direct-sampling method.

3.2 Low-Power Direct-Conversion RF Transmitter Architectures

Low-power RF transmitters generally adopt constant-envelope modulation, such as FSK or PSK, to reduce linearity-power trade-off. In addition, direct conversion of the baseband information into RF frequency allows efficient hardware implementation. These direct-conversion transmitters can be realized in either mixer-based or PLL-based architecture. This section will individually discuss these two transmitter architectures.

3.2.1 Mixer-Based Direct-Conversion Transmitters

Mixer-based direct-conversion transmitter architecture, which adopts the Gilbert-cell quadrature-mixer as RF modulator, is very popular for its flexibility of supporting all kinds of modulations. Fig. 3-3 illustrates a direct up-conversion design example. It consists of two digital-to-analog converters (DACs), two reconstruction filters, summed-output quadrature mixers, and a linear PA. This architecture is a universal modulator which can modulate all kinds of modulation; however, a higher transmission data rate inevitably leads to higher power consumption of the DACs and filters, presenting a tightly coupled power-bandwidth trade-off. In addition, this transmitter topology is typically sensitive to process, supply voltage, and temperature (PVT) variations, and various analog non-idealities, such as offset, IQ mismatch, and non-linearity effects. Large devices and higher bias currents are required in the analog circuits to overcome these non-ideal effects at the cost of increased silicon area and power consumption.

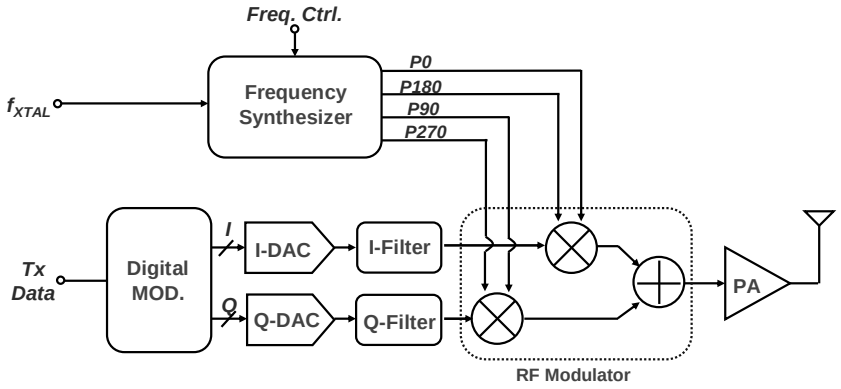
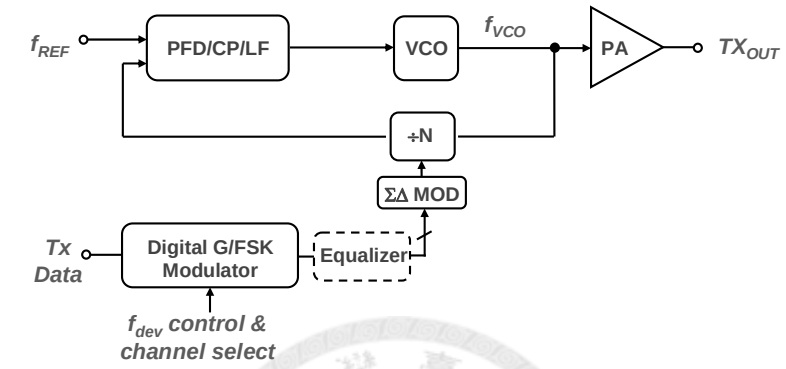


Fig. 3-3: Block diagram of a conventional mixer-based direct-modulation transmitter

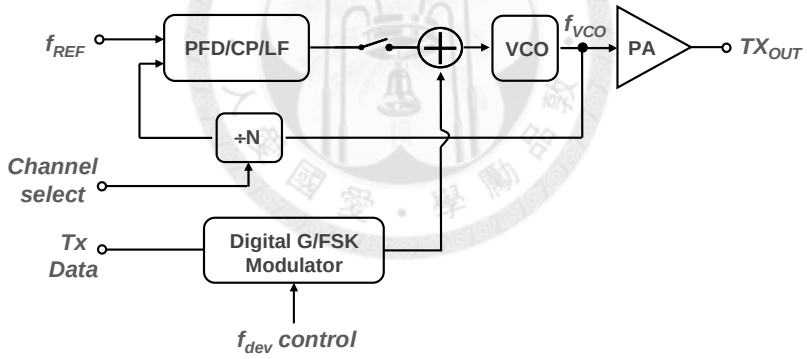
3.2.2 PLL-Based Direct-Conversion Transmitters

The PLL-based solutions are often favored for low-power applications, for they are more hardware-efficient. There are three major types of PLL-based FSK transmitter architectures [10]-[12]. For the closed-loop type, as illustrated in Fig. 3-4(a), the modulation is performed with the PLL closed. The data is applied to modulate the divider or the reference signal. The closed-loop topology is mainly suitable for transmitting narrow-band signals, for the data rate is limited by the loop bandwidth. While an equalizer can be applied to compensate the loop dynamics and extend the data rate beyond the PLL bandwidth, gain error of the equalizer degrades FSK modulation performance [10]. The second type of the PLL-based FSK transmitter is based on the open-loop architecture, as depicted in Fig. 3-4(b). Here, the modulation data is injected to control the VCO directly. Open-loop topology is free from the bandwidth constraint; however, since the loop is open during data transmission, frequency drift of the unlocked VCO is a major drawback. In practice, the open-loop topology requires periodic re-locking of the VCO frequency, thus making continuous operation difficult [11]. In addition, the VCO phase noise is not suppressed by the loop. The third type of the PLL-based FSK transmitter is based on the two-point modulation

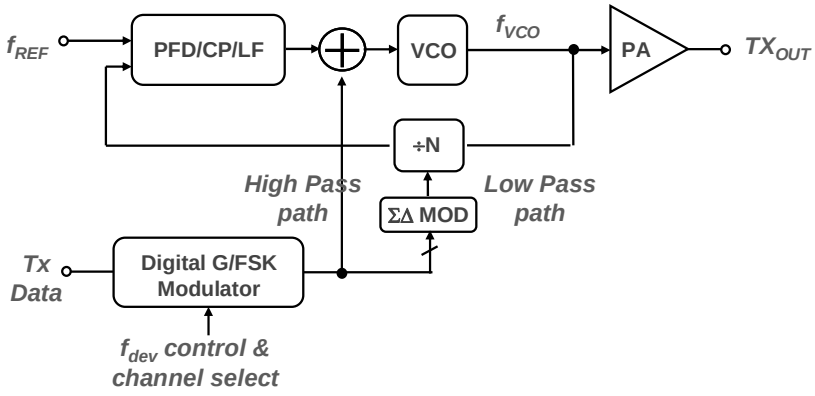
architecture, as shown in Fig. 3-4(c). By combining the two previous topologies, the two-point modulation method can overcome the signal bandwidth limitation and frequency drifting problem occurred in the closed-loop and open-loop topologies. However, this method requires good matching between the high-pass and low-pass paths [12]; hence, posing some design difficulties.



(a)



(b)



(c)

Fig. 3-4: Conventional PLL-based G/FSK transmitter architectures, (a) closed-loop architecture, (b) open-loop architecture, (c) two-point architecture. (f_{dev}: deviation frequency)

Chapter 4
A Super-regenerative ASK Downlink Receiver with A ΔΣ Pulse-Width Digitizer

4.1 Introduction

A 156-kbps ASK receiver is implemented in this work targeting for the implantable bio-medical applications. Due to stringent energy constraint, the receiver for an implanted device must be highly energy efficient. In addition, these implanted receivers are usually highly duty-cycled to save average power consumption [14]. Therefore, a fast turn-on time is also favorable to reduce energy waste during receiver start-up [15]. In this work, a super-regenerative receiver is implemented for its theoretically infinite gain during signal regeneration; thus resulting in good sensitivity, wide power detection range, fast start-up and low-power consumption. [16].

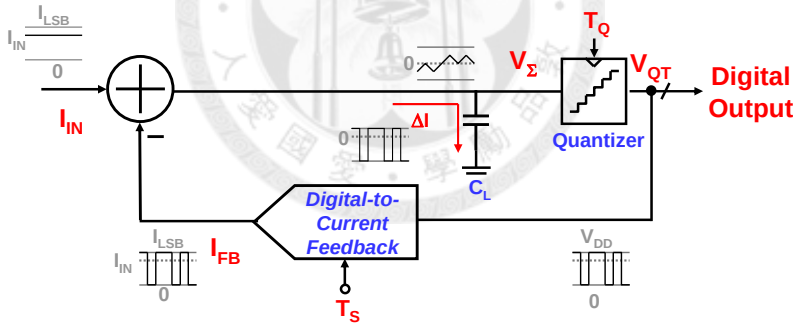
4.2 Proposed ΔΣ Pulse-Width Digitizer Architecture

To overcome the fore-mentioned design issues in the conventional pulse-width detector architectures, this work proposed Delta-Sigma pulse-width digitizer (ΔΣ-PWD) architecture [22]. The proposed architecture basically applies Delta-Sigma noise shaping concept in pulse-width domain to suppress the quantization error due to insufficient sampling frequency [23].

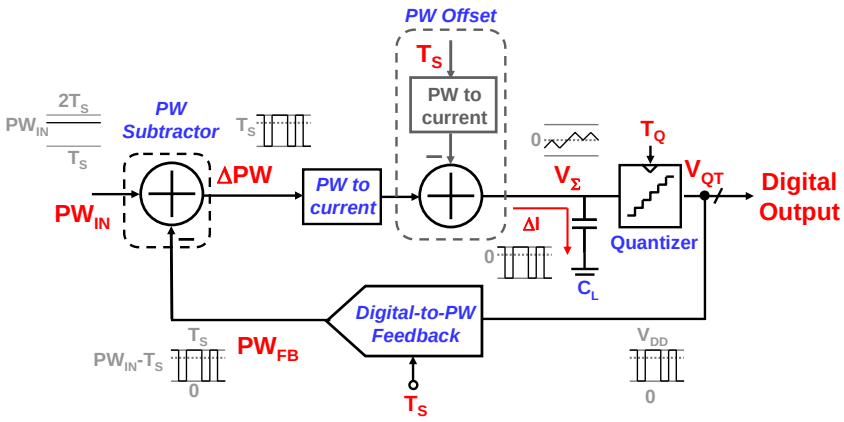
Conventional ΔΣ modulators are widely used in high-resolution analog-to-digital conversion applications, because they can suppress low-frequency quantization noise due to Quantizer by using a feedback loop containing the integrators [24]. Fig. 4-1(a) shows the conventional current domain single-bit 1st-order ΔΣ modulators simplified block diagram. Assuming the I_{IN} is a slow-variant input current. The feedback current (I_{FB}) is rapidly dithered between 0 and I_{LSB}, where I_{LSB} is the unit step of the digital-to-current converter. This feedback loop containing an integrator will force the average of I_{FB} to be equal to input current (I_{IN}), making the average of subtracted current (ΔI) and integrated voltage (V_{Σ}) to be zero. The 1-b digital output is rapidly dithered between 0 and V_{DD}, while its average value is tracking with the input current I_{IN}.

The ΔΣ modulators can also be applied into pulse-width domain, as shown in Fig. 4-1(b), to suppress the quantization error during pulse-width sampling. Similarly, assuming the PW_{IN} is a slow-variant input pulse-width value. The feedback pulse-width value (PW_{FB}) is rapidly dithered between 0 and T_S, where T_S is the sampling period of the sampling clock. This feedback loop containing an integrator will force the average of PW_{FB} to be equal to input pulse-width value (PW_{IN}), making the average of subtracted pulse-width value (ΔPW) to be zero. However, this generates negative pulse-width value at pulse-width subtactor output, which makes the circuit implementation difficult. Hence, a current which is equivalent to the pulse-width value of T_S (i.e. *PW Offset* in Fig, 4-1(b)) is subtracted with original current, up-shifting the input pulse-width detection range by T_S. The 1-b digital output is rapidly dither between 0 and V_{DD}, while its average value is tracking with the input pulse-width value (PW_{IN}) with an offset of T_S.

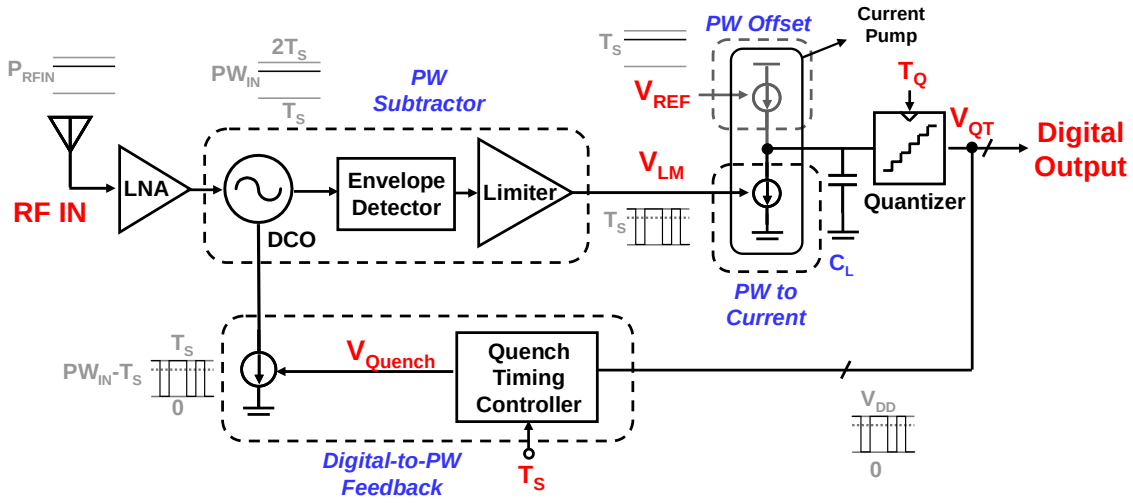
In order to suppress the quantization error during pulse sampling in direct-sampling pulse-width detector architecture, a ΔΣ-PWD embedded in the super-regenerative receiver is proposed in this dissertation, as shown in Fig. 4-1(c), which is basically a pulse-width domain 1st-order ΔΣ modulator. The proposed architecture only requires an additional Charge Pump (CP), a loop capacitor (C_L), and a Quantizer (QT). The DCO, Envelope Detector and Limiter form a *Pulse-Width Subtractor*. The Charge Pump performs *Pulse-Width to-Current* conversion, while a *Pulse-Width Offset* is implemented by injecting a reference current pulse to avoid negative pulse-width operation. In the feedback path, the Quantizer output (V_{QT}) is fed-back and converted to pulse width by a Quench Timing Controller functioned as a *Digital-to-Pulse-Width Feedback*. The 1-b digital output is rapidly dither between 0 and V_{DD}, while its average value is tracking with the input power in dBm (P_{RFIN}).



(a)



(b)

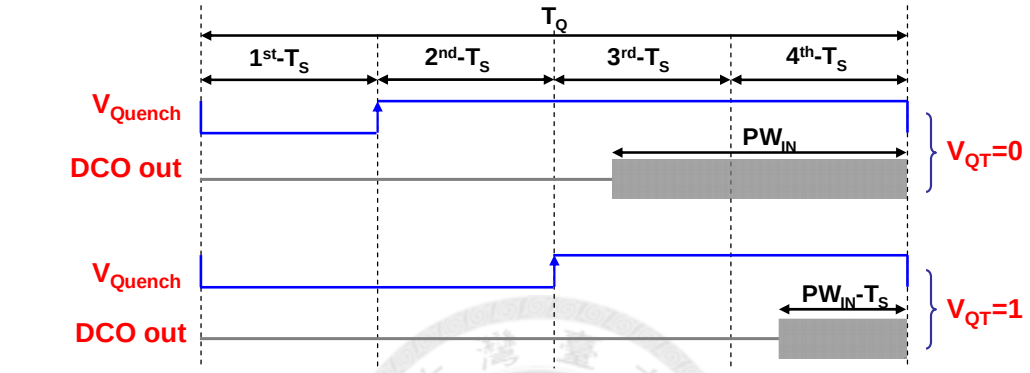


(c)

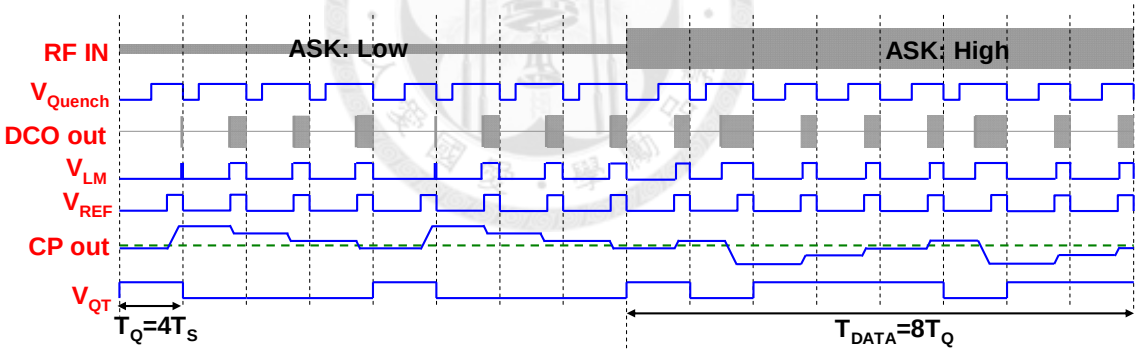
Fig. 4-1: (a) Current domain 1st-order ΔΣ modulator, (b) pulse-width domain 1st-order ΔΣ modulator with offset, (c) proposed Delta-Sigma pulse-width digitizer (ΔΣ-PWD) architecture embedded in a super-regenerative receiver

The ΔΣ-PWD uses time domain feedback to attain pulse-width domain digitization [25]. The time domain digital-to-PW feedback is performed by Quench Timing Controller according to the single-bit digital signal V_{QT} in this design; whereas pulse-width subtraction is performed by DCO, Envelope Detector and Limiter in the super-regenerative receiver. The quench timing is generated by the sampling clock (T_S); while the quantizer clock and quench period, T_Q, is composed to four equal parts, as illustrated in Fig. 4-2(a), with each has duration of T_S. At the 1st-T_S duration, the quench clock (V_{Quench}) is reset and Quantizer input is sampled. If Quantizer output is 0, the quench clock will turn on at 2nd-T_S. This feedback quench clock (V_{Quench}) controls the DCO quench current, hence affects the DCO oscillation envelope. Meanwhile, the DCO envelope also depends on the input ASK signal. The net effect of these two determines the actual DCO envelope, hence the pulse width at Limiter output (V_{LM}) which assumes to be PW_{IN} in this case. On the other hand, if quantizer output is 1, the quench clock

will turn on at 3rd-T_S. Therefore, this effectively subtracts pulse width of DCO envelope by T_S (i.e. PW_{IN}-T_S). Fig. 4-2(b) illustrates the overall operation timing diagram of the single-bit ΔΣ-PWD (for simplicity, 8 times over-sampling of data by quench clock (i.e. $T_{DATA}=8T_Q$) is used in this drawing). The input ASK signal can be easily discriminated in the Digital Baseband (DBB), by processing the oversampled 1-bit V_{QT}.



(a)



(b)

Fig. 4-2: (a) Implementation of digital-to-PW feedback and PW subtraction by Quench Timing Controller and Quenched DCO, (b) the overall operation principle and timing of proposed ΔΣ-PWD (assume $T_{DATA}=8T_Q=32T_S$)

The performance of conventional ΔΣ modulators can be improved by increasing the bit numbers of Quantizer (B) and sampling frequency ($1/T_S$); however, the improvement in proposed ΔΣ-PWD is limited due to the constant production of these

two parameters. Assuming Quantizer bit number (B) is increased to two for instance, as illustrated in Fig. 4-3, the sampling period is also reduced by 2^B-1 in order to maintain the same pulse-width detection range (T_{DR}) for same comparison. The quench period (T_Q) is divided into four durations, but each of them is not necessary equal to T_S. The summed period of 2nd-duration (i.e. Quench ON) and 3rd-duration (ΔΣ-PWD Detection) are assigned to be equal to the DCO start-up time at the noise level (T_{noise}). By adjusting the quench turn on time in 2nd-duration according to the feedback signal V_{QT} (with 2^B codes), the DCO start-up information in 3rd-duration (ΔΣ-PWD Detection, T_{DR}) can be detected and quantized into 2^B-1 intervals with each of T_S time. The pulse-width detection range (T_{DR}) in 3rd-duration is set to half of T_{noise} for easier timing generation. Therefore, it can be expressed as

$$T_{DR} = \frac{T_{noise}}{2} = (2^B - 1)T_S \tag{4-1}$$

As revealed in Equation (4-1), the production of quantization levels (2^B-1) and sampling time (T_S) is a constant under same DCO operation condition. The 4th-duration is employed as a reference pulse for Pulse-Width Offset. In general case, the overall quench period (T_Q) is a function of bit number (B) and T_{noise}, which can be expressed as

$$T_Q(B, T_{noise}) = T_{noise} + 2T_S = T_{noise} \cdot (1 + \frac{1}{(2^B - 1)}) \tag{4-2}$$

Increasing of Quantizer bit number (B) would lead to shorter quench period (T_Q); thus increasing the overall over-sampling-ratio of ΔΣ-PWD (i.e. OSR=T_{DATA}/T_Q). However, the OSR is still limited by the start-up time at noise level T_{noise}. In this dissertation, a lower sampling frequency (T_S=50 ns) and a single-bit Quantizer (B=1) are adopted in order to minimize the circuit complexity and power consumption.

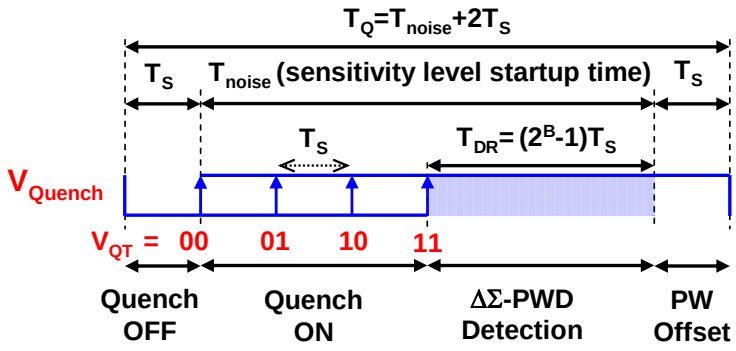


Fig. 4-3: Feedback quench timing of a ΔΣ-PWD (B=2)

This ΔΣ-PWD is inherently a time-domain signal processing, which is suitable for low-voltage operation. In addition, it is insensitive to many analog non-idealities [26] (e.g. Quantizer DC offset). Most important, many calibration or decimation circuits can move into digital domain. For example, conventional analog AGC loop [17] or Data Synchronizer [21] for super-regenerative receiver is required in order to achieve the optimized demodulation performance. In this work, the match filter, threshold detector, the decimator, and the data synchronizer can be implemented in digital domain (DBB) to support ASK demodulation.

4.3 Analysis of the ΔΣ Pulse-Width Digitizer

The proposed ΔΣ-PWD adopts Delta-Sigma noise shaping concept and processes information in pulse-width domain. In order to gain more insights and obtain more quantitative analysis of the ΔΣ-PWD, this section will firstly provide a linear model as well as its related transfer function [24]. The quantization noise calculation and the rejection capability of ΔΣ-PWD will then be revealed. Finally, we will discuss several design considerations from system viewpoint.

4.3.1 Linear Model of the ΔΣ-PWD

In order to analyze the ΔΣ-PWD and its effects on the suppression of quantization error due to sampling clock frequency, a model is devised as illustrated in Fig. 4-4 which corresponds to the architecture in Fig. 4-1(c). The feedback loop ensures that the average of the 1-bit V_{QT} tracks input signal power in dBm (P_{RFIN}). The input signal is converted into pulse width (i.e. PW_{LM}) by the DCO, Envelope Detector and Limiter. The parameter *K* represents the dBm-to-pulse-width conversion gain, whereas the V_{FS} represents the full-scale operation of the quantizer. Parameter α is the up/down current mismatch of Charge Pump (CP). By applying pulse-width feedback at quench clock of DCO has an advantage of eliminating up/down current mismatch of Charge Pump (CP), since this mismatch is absorbed inside the feedback loop. After being subtracted with the quench feedback pulse width (PW_{Quench}, which converted by the Quench Timing Controller (QTC) according to V_{QT}, with gain of T_S/V_{FS}), the input pulse width is then compared with the pulse width ($PW_{REF}=T_S$) of a reference signal (V_{REF}) by the Charge Pump (CP) to remove DC term. The Charge Pump (CP) then converts the pulse width to current domain. Similar to the Charge Pump in a phase-locked loop (PLL), the Charge Pump (CP) only charges the loop capacitor in partial duration of each quench period (i.e. T_Q); therefore, the equivalent average pulse-width-to-current gain of the Charge Pump (CP) is calculated to be I_{CP}/T_Q (where I_{CP} is output current of the Charge Pump) [27]. The comparison result of the Charge Pump (CP) is integrated on the loop capacitor (C_L). The quantization noise voltage of the Quantizer ($V_{n,QT}$) is added at the output of the ΔΣ-PWD, which can be related to the time-domain quantization error due to insufficient sampling frequency; whereas the noise-induced jitter and clock jitter ($PW_{n,jitter}$) are equivalently included at the input of the ΔΣ-PWD.

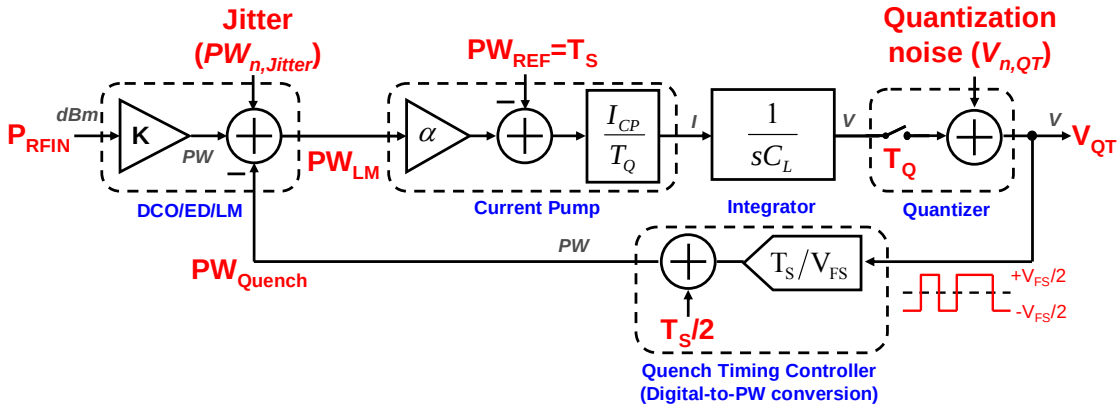


Fig. 4-4: linear model of the proposed ΔΣ-PWD

Noise Transfer Function (NTF) represents the impact of quantization noise ($V_{n,QT}$) to the output (V_{QT}) of ΔΣ-PWD. As illustrated in Fig. 4-4, it can be derived as [24]:

$$NTF(s)=\frac{V_{QT}(s)}{V_{n,QT}(s)}=\frac{s}{s+\omega_L} \tag{4-3}$$

Where the loop bandwidth ω_L is decided by output current of the Charge Pump (I_{CP}), loop capacitance (C_L), sampling period (T_S) and quench period (T_Q).

$$\omega_L=\frac{T_S\alpha I_{CP}}{T_Q C_L V_{FS}} \tag{4-4}$$

Equation (4-3) reveals that the high-pass Noise Transfer Function (NTF) of the ΔΣ-PWD shapes the quantization error of sampling clock.

On the other hands, the feedback loop provides a 1st-order low-pass Signal Transfer Function (STF), suppressing clock and noise-induced jitters while still allows sufficient data rate. It can be defined as following:

$$STF(s)=\frac{V_{QT}(s)}{PW_{n,Jitter}(s)}=\frac{\omega_L(V_{FS}/T_S)}{s+\omega_L} \tag{4-5}$$

Fig. 4-5 shows the filter profile of STF and NTF as derivate in (4-3) and (4-5), the selection of loop bandwidth ω_L is a trade-off between the suppression of quantization noise (i.e. NTF) and jitter (i.e. STF). Lower ω_L allows better jitter suppression, while

higher ω_L has better quantization noise suppression. Since jitter effect can be further suppressed by digital decimation filter following the ΔΣ-PWD, higher ω_L is generally preferred in this system to optimize the capability of quantization noise suppression.

4.3.2 Pulse-Width Quantization Noise of ΔΣ-PWD

The quench turn on time of DCO is dithered by the ΔΣ-PWD loop with a step of T_S. Therefore, the equivalent pulse-width variance due to quantization noise is [24]

$$\sigma^2_{PW\_\Delta\Sigma PWD}(f) = \frac{\Delta_{PW}{}^2}{12} = \frac{T_S{}^2}{12} \tag{4-6}$$

The power spectrum density (PSD) of the pulse-width variance is derivate as the pulse-width variance ($\sigma_{PW\_\Delta\Sigma PWD}{}^2$) divided by the quench frequency, f_Q, (since the Quantizer is sampled by quench clock) and then be multiplied by the noise transfer function (NTF) of the ΔΣ-PWD, as expressed as following (assuming $f<<f_L$):

$$\begin{aligned} S_{PW\_\Delta\Sigma PWD}(f) &= \frac{\sigma^2_{PW\_\Delta\Sigma PWD}}{f_Q} \times |NTF|^2 \\ &\approx \frac{T_S{}^2}{12} \cdot (\frac{1}{f_Q}) \cdot (\frac{f}{f_L})^2 \end{aligned} \tag{4-7}$$

The integrated pulse-width quantization noise ($PW_{n,\Delta\Sigma PWD}{}^2$) can be derivate by integrating the pulse-width noise PSD ($S_{PW\_\Delta\Sigma PWD}$) from DC to single-side signal bandwidth f_C (which is defined by the digital filter), as shown below

$$\begin{aligned} PW_{n,\Delta\Sigma PWD}{}^2 &= 2 \cdot \int_0^{f_C} S_{PW\_\Delta\Sigma PWD}(f) df \\ &= \frac{T_S{}^2 f_C{}^3}{18 f_Q f_L{}^2} \end{aligned} \tag{4-8}$$

Replace (4-2) and (4-4) into (3-8), the pulse-width quantization noise ($PW_{n,\Delta\Sigma PWD}{}^2$) can be calculated as

$$PW_{n,\Delta\Sigma PWD}{}^{2} = \frac{V_{FS}{}^{2} C_{L}{}^{2} f_{C}{}^{3} T_{noise}{}^{3}}{72\pi^{2}\alpha I_{CP}{}^{2}} \cdot (1 + \frac{1}{(2^{B}-1)})^{3} \quad (4\text{-}9)$$

In the conventional ΔΣ-modulator design, the quantization noise can be reduced by increasing the Quantizer bit number (*B*) or sampling frequency ($f_S=1/T_S$), both of which are two independent parameters [24]. However, the sampling period (T_S) and Quantizer bit number (B) in ΔΣ-PWD are two correlated parameters, as revealed in (4-1). Increasing the Quantizer number (B) by one only gains noise improvement less than 6 dB, as estimated by (4-9), but would significantly increase power consumption of Quantizer (at least 4 times) due to roughly doubled Quantizer numbers and sampling frequency (f_S). Nevertheless, the quantization noise can be further improved by increasing the ΔΣ-modulator order.

On the other hand, the PSD of pulse-width quantization noise of direct-sampling type pulse-width digitizer can be derivate as

$$S_{PW\_DirectSample}(f) = \frac{\sigma^{2}_{PW\_DirectSample}}{f_Q} = \frac{T_S{}^{2}}{12} \cdot (\frac{1}{f_Q}) \quad (4\text{-}10)$$

Fig. 4-5 also plots the pulse-width noise PSD of ΔΣ-PWD and direct-sampling type pulse-width digitizer, where $S_{PW.Signal}$ represents the pulse-width PSD of input signal with bandwidth of f_C. In order to show the noise shaping effect of ΔΣ-PWD compared to the direct-sampling method (with same sampling frequency and signal bandwidth), a quantization-noise-suppression-ratio (QNSR) is defined in this dissertation as:

$$QNSR \equiv \frac{PW_{n,DirectSample}{}^{2}}{PW_{n,\Delta\Sigma PWD}{}^{2}} = \frac{2\int_0^{f_C} (\frac{T_S{}^{2}}{12} \cdot \frac{1}{f_Q}) df}{2\int_0^{f_C} (\frac{T_S{}^{2}}{12} \cdot \frac{1}{f_Q}) \cdot (\frac{f}{f_L})^{2} df} = 3(\frac{f_L}{f_C})^{2} \quad (4\text{-}11)$$

Where $PW_{n,DirectSample}{}^{2}$ is the integrated pulse-width quantization noise of the direct-sampling type digitizer. Equation (4-11) also shows that the quantization error suppression can be improved by increasing the loop bandwidth of ΔΣ-PWD (f_L) or by

reducing the signal bandwidth (f_C). Assuming loop bandwidth of $f_L=f_S/16$ and signal bandwidth of $f_C=f_S/128$ are adopted, this ΔΣ-PWD can achieve theoretically 22.8-dB QNSR, which equivalently samples the direct-sampling type pulse-width detector with a 13.8 times higher sampling frequency.

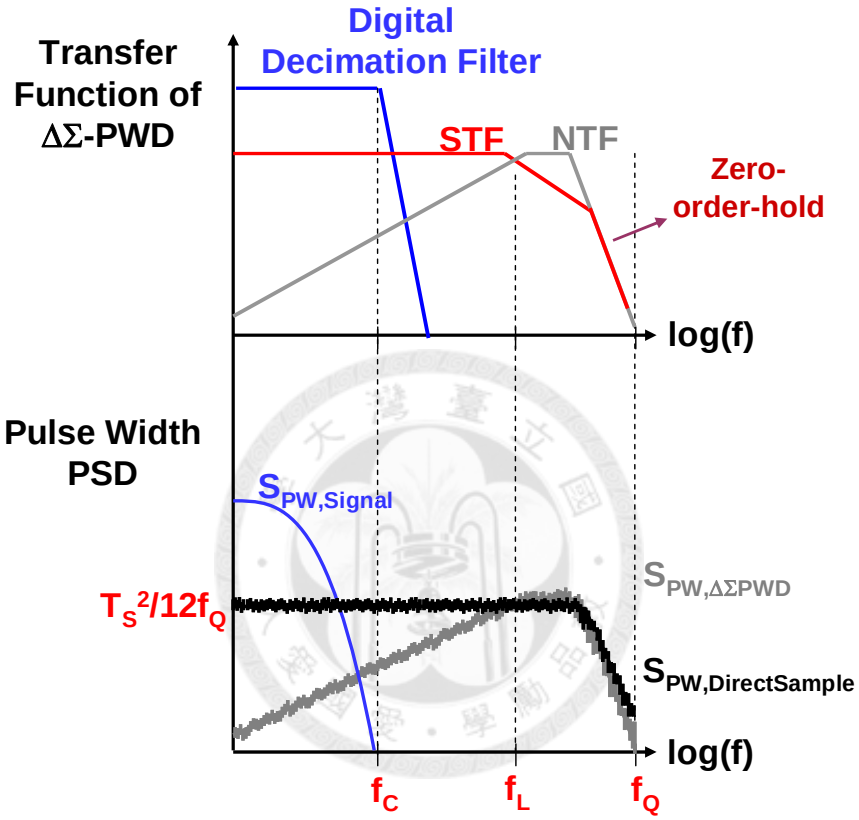


Fig. 4-5: Illustration of transfer functions and pulse-width spectrum density of the ΔΣ-PWD

4.3.3 Non-idealities and Design Considerations in The ΔΣ-PWD

Similar to ΔΣ fractional-N PLL design [10], the Charge Pump circuit would induce several non-idealities, such as noise, mismatch and non-linearity, degrading the close-in noise performance. First, despite the fact that the quantization noise is the dominant noise source which can be suppressed by the feedback loop, the Charge Pump would

still increase low-frequency noise floor. In this system, a pulse width of T_S is offset in order to avoid negative pulse-width operation, increasing the period of current noise pumping into loop capacitor. In addition, although Charge Pump is absorbed inside the loop to reduce the degradation due to mismatch, it would still contribute distortion when mismatch. Furthermore, channel-length modulation effect of Charge Pump current source would also lead to higher even-order distortion, increasing the 2^{nd}-harmonic power level. Therefore, careful optimization of the Charge Pump device size is critical to overcome noise, mismatch and channel-length modulation issues.

Although this ΔΣ-PWD uses continuous-time implementation in this work, its characteristic is similar to the discrete-time ΔΣ-modulator implementation; therefore, many design issues in continuous-time ΔΣ-modulator, such as loop delay [25], do not significantly affect its performance.

4.4 Circuit Implementations

The super-regenerative receiver with proposed ΔΣ-PWD is demonstrated in the 400-MHz MICS band. In this section, key building blocks and design issues are described in details.

4.4.1 Low Noise Amplifier (LNA) and Digital-Controlled-Oscillator (DCO)

Fig. 4-6 shows the schematic of Low-Noise Amplifier (LNA) and Digital-Controlled Oscillator (DCO). Poor isolation between LNA output and the antenna would potentially degrade the super-regenerative receiver sensitivity; hence, the differential-type cascoded LNA is adopted in this work. The LNA uses bond-wires as

its source degeneration inductors for impedance matching and noise optimization. The LNA transforms input RF power into current which then directly injects into the DCO. This LNA consumes around 200 μA.

The 400-MHz DCO adopts NP-core LC-tank oscillator architecture to reduce start-up current, as shown in Fig. 4-6. The bias current of the DCO is periodically quenched, while the DCO outputs periodic pulses signal with various width depending on the input RF power level. In order to increase resonance impedance, this DCO uses large inductance (20 nH) to compensate the low quality factor (i.e. around 5) of on-chip spiral inductor. A 6-bit capacitor array is implemented to cover center frequency variation due to process, supply and temperature. The average DCO current consumption is around 350 μA from 1.3-V supply voltage.

"T_{noise}" is the start-up time when input power is at the receiver noise level (i.e. P_{noise}), which decreases when the bias current of LNA and DCO increase. In order to achieve wide power detection range, an analog AGC loop is implemented in low-pass filtering type super-regenerative receiver to continuous adjusting the bias current of LNA and DCO [17]. On the other hand, the bias current of LNA and DCO in this work is digitally controlled by DBB. When the receiver saturation or below noise level (i.e. V_{QT} is almost all "1" or all "0") are detected by the DBB, the RF gain can be programmed by adjusting the bias current of LNA and DCO (i.e. 2-bit *RF Gain Control<1:0>* in Fig. 4-6) to extend the operation range of the super-regenerative receiver.

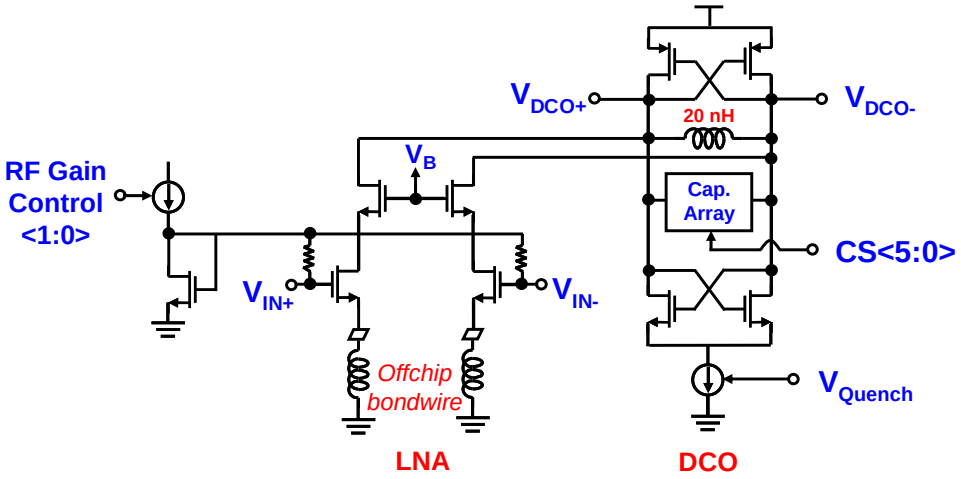


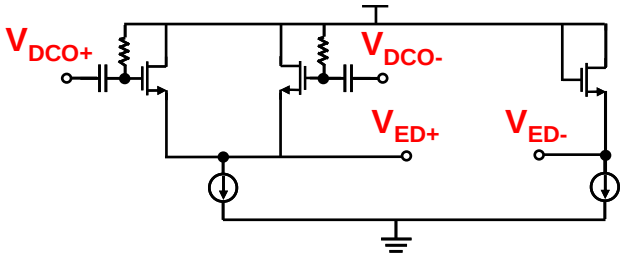
Fig. 4-6: Simplified schematic of LNA and quenched DCO.

4.4.2 Complementary Differential Envelope Detector and Limiter

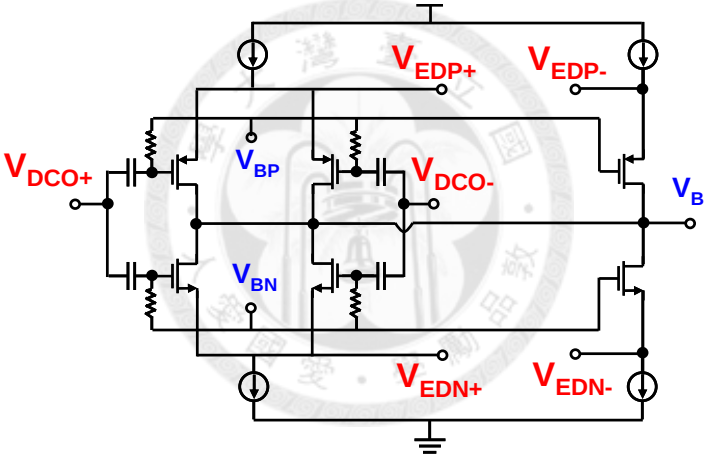
An envelope detector is required in the super-regenerative receiver to rectify the DCO output RF signal (V_{DCO}) and extract the envelope signal (V_{ED}). However, the common-mode voltage of DCO output is significantly fluctuated when DCO is quenching. The conventional single-ended envelope detector architecture [29], as depicted in Fig. 4-7(a), is unable to reject this common-mode fluctuation, resulting in unwanted glitches at super-regenerative receiver output [20]. A modified complementary differential envelope detector is implemented in this work, as shown in Fig. 4-7(b). The simulation results in Fig. 4-7(d) shows that not only the output swing can be doubled by using complimentary structure without consuming extra current, the common-mode fluctuation can also be cancelled by this differential circuit implementation. This envelope detector consumes 30 μA from 1.3-V supply voltage.

A complementary differential limiting amplifier is adopted here to accommodate the previous complementary differential envelope detector stage. In this work, the limiting amplifier is designed with programmable threshold by manually adjusting bias current (I_N) from 6 μA to 9 μA, as shown in Fig. 4-7(c). Since I_P is slightly higher than I_N, the

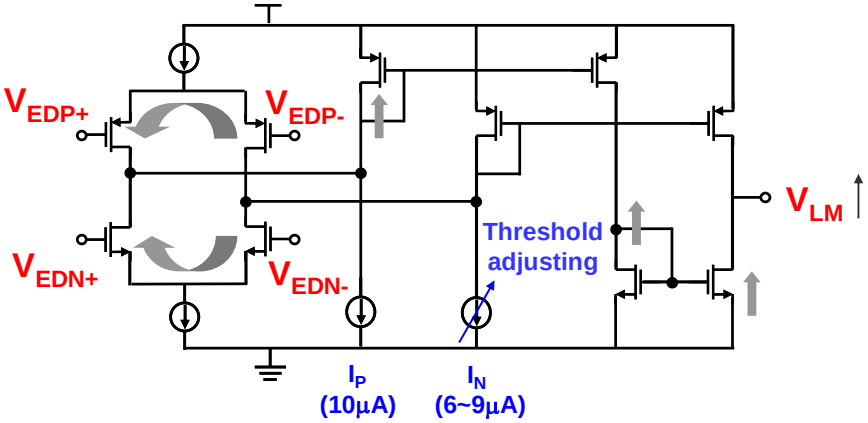
limiting amplifier output (V_{LM}) remains low when no input signal is applied. When input signal is larger than threshold, output voltage turns high. This limiting amplifier consumes 50 μA from 1.3-V supply voltage. Fig. 4-7(d) shows the simulated transient of DCO oscillation envelope detection and limiting waveform.



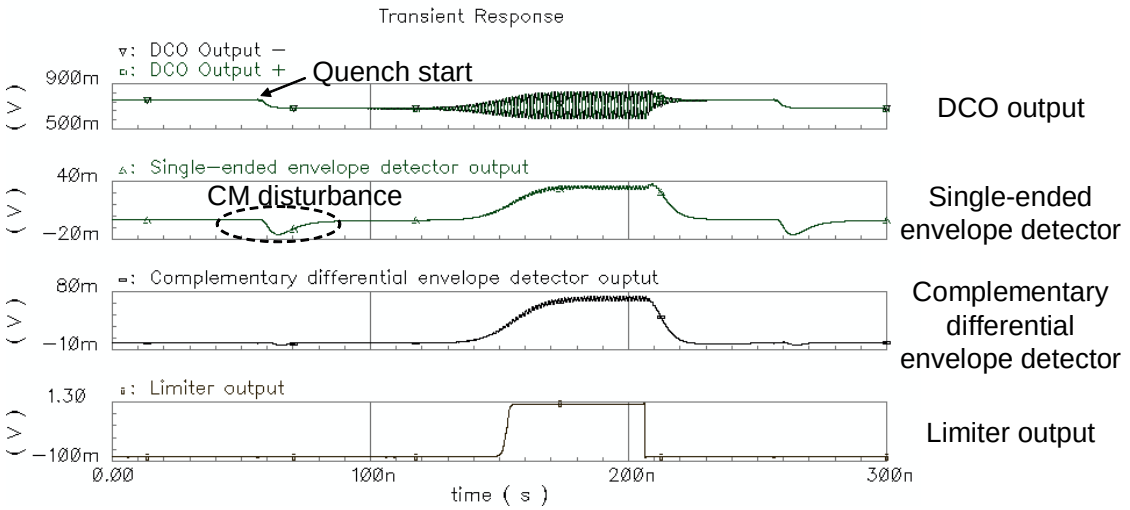
(a)



(b)



(c)



(d)

Fig. 4-7: (a) Conventional single-ended envelope detector, (b) modified complementary differential envelope detector, (c) complementary differential limiting amplifier, (d) simulated transient results

4.4.3 Charge Pump and Loop Capacitor

The Charge Pump compares the pulse width between reference pulse (V_{REF}) and limiter output (V_{LM}), and then outputs the residue current pulses. Then, these pulses are injected into loop capacitor (C_L), as shown in Fig. 4-8. The Charge Pump and loop capacitor adopt differential structure which can provide better Power-Supply-Rejection-Ratio and avoid coupling from digital circuits. A common-mode feedback is adopted in this architecture to define the bias voltage for the following Quantizer stage. The common-mode sensing resistors (R_F) are parallel connected to the loop capacitors (C_L), which would also provide a zero in the overall loop transfer function (i.e. $f_{CMFB}=1/(2\pi C_L*R_F)$). Therefore, the common-mode sensing resistor value (R_F) should be carefully selected to avoid the degradation of quantization suppress capability, while still allows acceptable common-mode settling time. The bias

current of Charge Pump is around 20 μA.

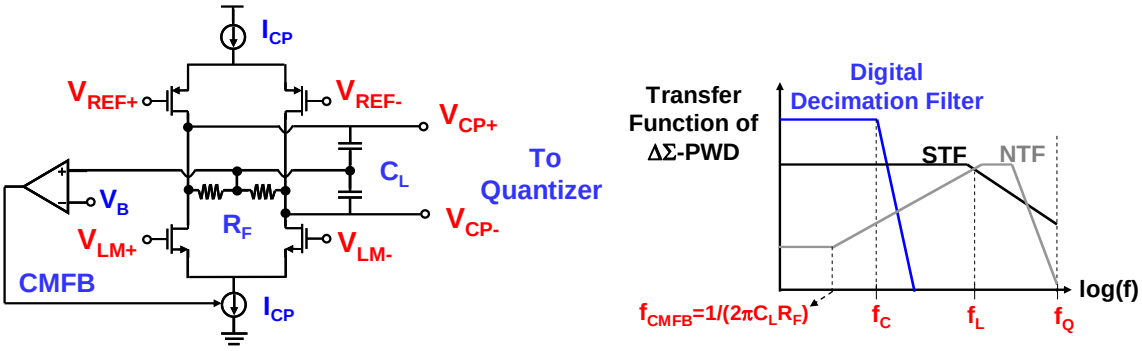


Fig. 4-8: Simplified schematic of the Charge Pump and loop capacitor, and frequency response change due to R_F

4.4.4 Single-bit Clocked Quantizer

Fig. 4-9 depicts the single-bit clocked quantizer schematic [28]. The sampling clock (i.e. CLK_{QT}) is generated by Quench Timing Controller (QTC) with the quench frequency of f_Q. The Quantizer delay is designed to be smaller enough (< 1 ns) to avoid degradation of NTF. The analog and digital supplies are separated to avoid coupling. This quantizer consumes 50 μA from 1.3-V supply.

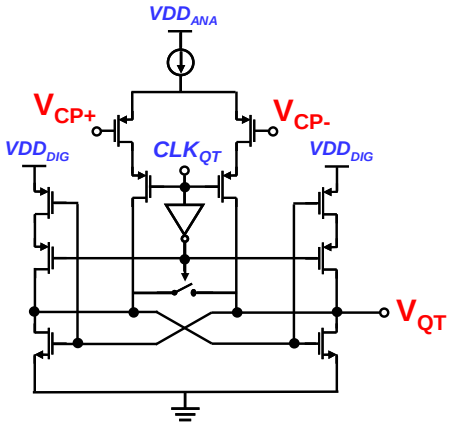
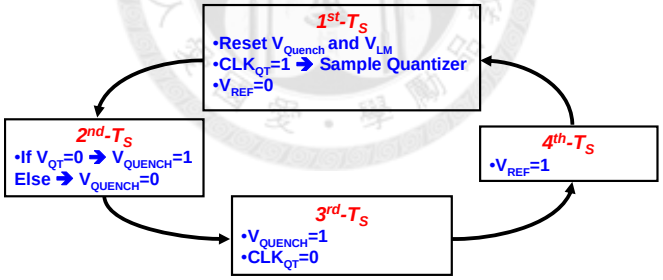


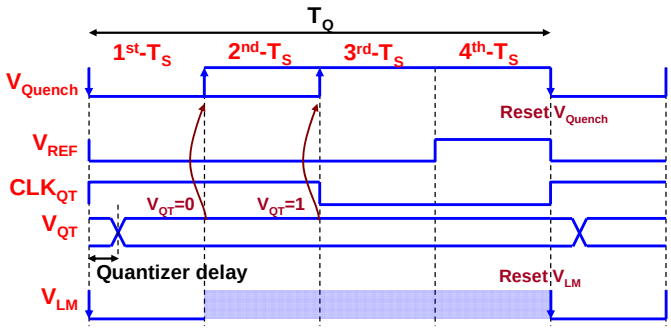
Fig. 4-9: Schematic of single-bit clocked quantizer

4.4.5 Quench Timing Controller (QTC)

The Quench Timing Controller uses 20-MHz sampling frequency (f_S) to generate all of the clocks and reference pulses of the ΔΣ-PWD. It is also the feedback element of the ΔΣ–PWD loop, which directly impacts the overall linearity and noise performances. As shown in Fig. 4-10(a), a finite-state-machine which represents Quench Timing Controller controls the signals of V_{Quench}, CLK_{QT} and V_{REF}. As the timing diagram shown in Fig. 4-10(b), the Quantizer is sampled at the start of 1^{st}-T_S duration and feedback to V_{Quench} at the 2^{nd}-T_S or 3^{rd}-T_S. Therefore, the delay of the Quantizer must be smaller than one-T_S to guarantee the proper function of this feedback system. The linearity of feedback element impacts the overall performance of ΔΣ feedback system. In this architecture, the linearity of QTC is guaranteed by the single-bit digital implementation. However, the jitter of sampling clock source (f_S) still directly inject into the loop through this feedback element.



(a)



(b)

Fig. 4-10: (a) Finite-state-machine of Quench Timing Controller, (b) Timing diagram of Quench Timing Controller

4.4.6 Digital Baseband

Many powerful baseband-signal processing function can be easily implemented in digital domain to process the signal digitized by ΔΣ-PWD. Fig. 4-11 shows the Digital Baseband simplified block diagram. L^{th}-order ΔΣ modulator typically requires $(L+1)^{th}$-order *sinc* decimation filter [24]. Hence, a $sinc^2$ digital filter is implemented in this work to suppress 1^{st}-order quantization noise. The threshold power level of input ASK RF signal can be detected by averaging several data period (T_{DATA}). Then, the filtered signal is down-sampled by four and decimated according the threshold detected by the Threshold Detector. The Threshold Detector can also be used to detect the signal saturation and adjust the RF gain (e.g. by changing the bias current of LNA and DCO). For example, if the threshold is detected too high (i.e. V_{QT} is almost all "0"), the DBB will reduce RF gain. In contrast, the DBB will increase RF gain if the detected threshold is too low (i.e. V_{QT} is almost all "0"). Therefore, the super-regenerative receiver with the proposed ΔΣ-PWD can accommodate wide range of input RF power. Nevertheless, the demodulation performance can be further improved by using a digital "Clock Synchronization" to recover the sampling clock timing and frequency offset [30].

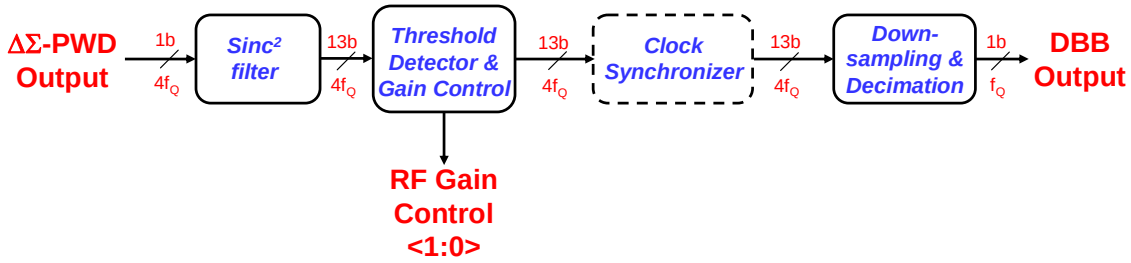


Fig. 4-11: Simplified architecture of Digital Baseband

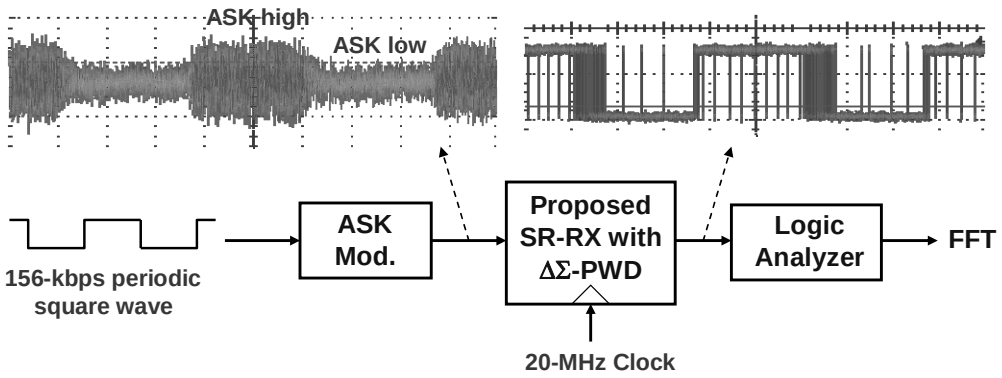
4.5 Experimental Results

This chip is fabricated in the 0.18-μm CMOS process. The whole super-regenerative receiver dissipates 700 μA from a 1.3-V supply. The quenched DCO with bulky on-chip spiral inductor (Q≈5) consumes the majority of total bias current (i.e. 600 μA). This receiver can support frequency range from 390 MHz to 485 MHz. The ΔΣ-PWD is sampled at 5-MHz which is generated by a 20-MHz clock.

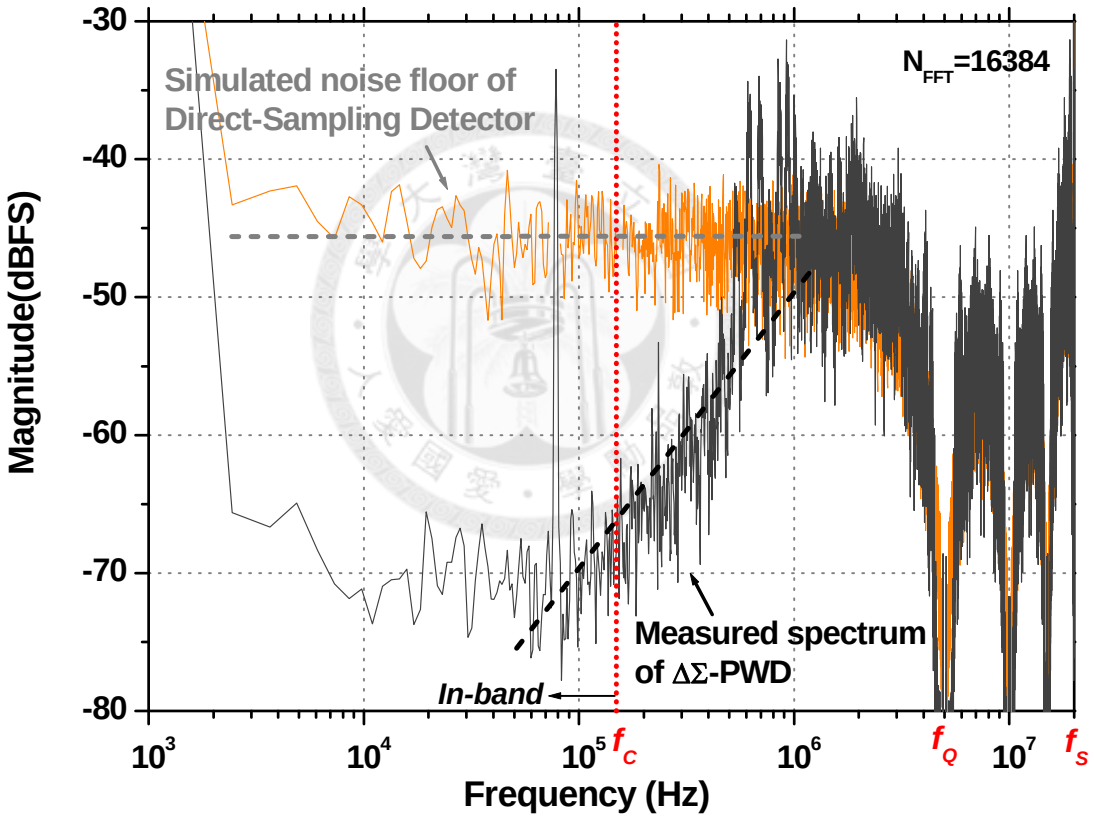
A 156-kbps periodic ASK signal with the RF power changing between two different level is provided as an input RF test signal in this measurement. In this case, the ΔΣ-PWD is sampled at 20 MHz while the Quantizer is sampled by quarter of the sampling rate (i.e. T_Q= 1/5MHz); hence, the over-sampling-ratio (OSR) is 32 (T_{DATA}=32T_Q=1/156kbps). The output digital code is captured by the logic analyzer for FFT spectrum analysis, as depicted in Fig. 4-12(a). Fig. 4-12(b) shows the measured FFT spectrum of ΔΣ-PWD output digital code with N_{FFT}=16384.When input power is higher, ΔΣ-PWD generates more "1"s; while it generates more "0"s when input power is lower. The full scale in Fig. 4-12(b) represents the pulse-width value of T_S. The integrated root-mean-square pulse-width error ($PW_{n,\Delta\Sigma PWD}$) within signal bandwidth (f_C) is calculated to be 0.27 ns. The close-in noise is mainly degraded by receiver noise. Fig. 4-12(b) also plots the simulated noise power density of direct-sampling type pulse-width detector, which can also be calculated by equation (4-12).

$$S_{PW\_DirectSample\_SSB}(f) = \frac{2 \cdot \frac{T_S^{\,2}}{12} \cdot \left(\frac{1}{f_Q}\right) \cdot \left(\frac{f_S}{16384}\right)}{T_S^{\,2}} = -44 \ dBFS \qquad (4\text{-}12)$$

The in-band root-mean-square pulse-width error of direct-sampling type detector with 20-MHz sampling frequency is calculated to be 3.6 ns. Hence, this ΔΣ-PWD can achieve around 23-dB Quantization-Jitter-Suppression-Ratio (QJSR).



(a)

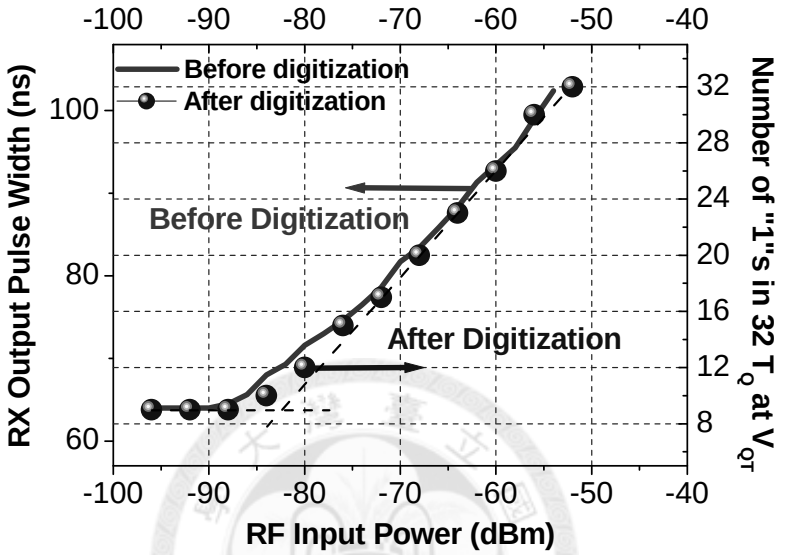


(b)

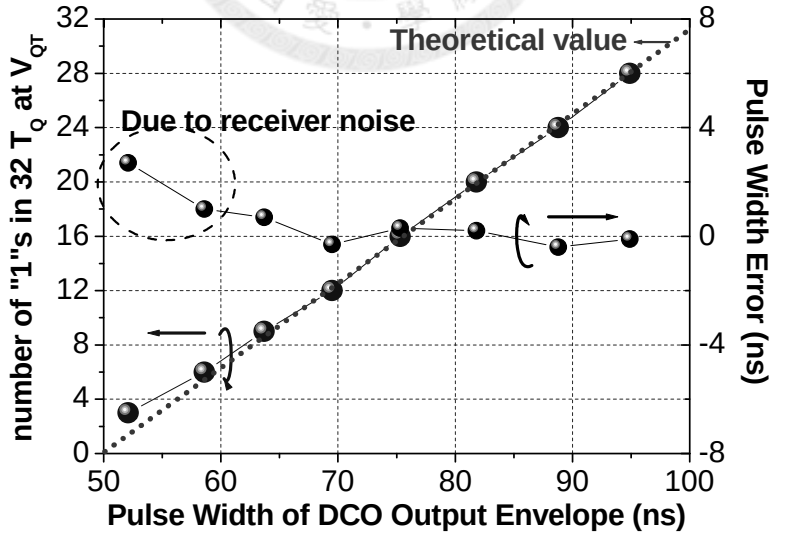
Fig. 4-12: (a) Measurement setup, (b) measured output spectrum of ΔΣ-PWD and simulated noise spectrum direct-sampling type pulse-width detector.

The output digital code can also be decimated by simply counting the number of one during 32 cycles. The measured number of "1" at V_{QT} versus input power is depicted in

Fig. 413(a); whereas Fig. 4-13(b) is plotted the error versus equivalent pulse width value. This figure shows that the error close to lower pulse-width value (i.e. smaller than 55 ns) is increased roughly three times, which is mainly contributed from large RX-noise jitter at lower input power level.



(a)



(b)

Fig. 4-13: Measured pulse-width digitized code by direct counting in 32 cycles (a) versus input power; (b) versus pulse width value.

Fig. 4-14 shows the measured pulse width at different RF gain setting. As summarized in Table 4-1, the noise level (P_{noise}) and T_{noise} are decreased when the bias current of LNA/DCO current is increased. The super-regenerative receiver can accommodate P_{RFIN} ranging from about -85 dBm to -35 dBm by adjusting the 2-bit RF gain control.

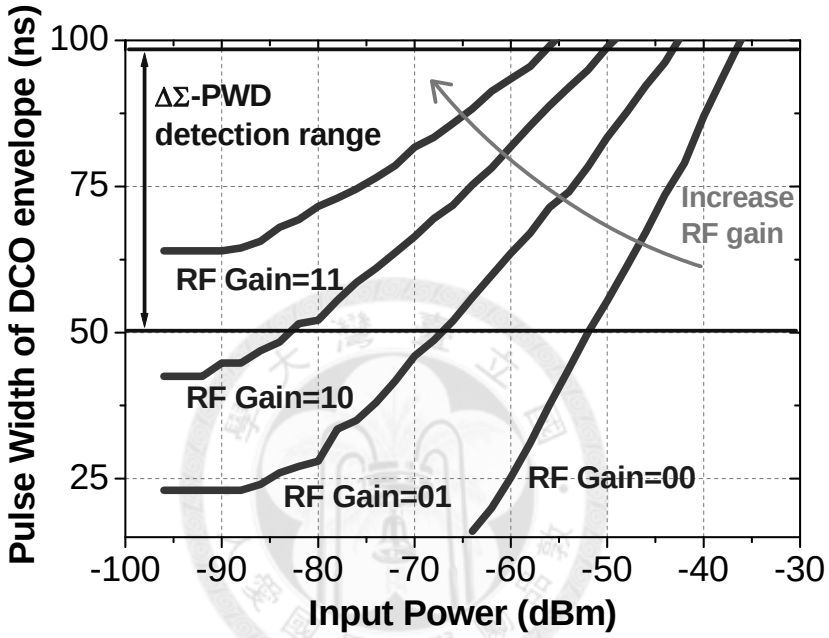
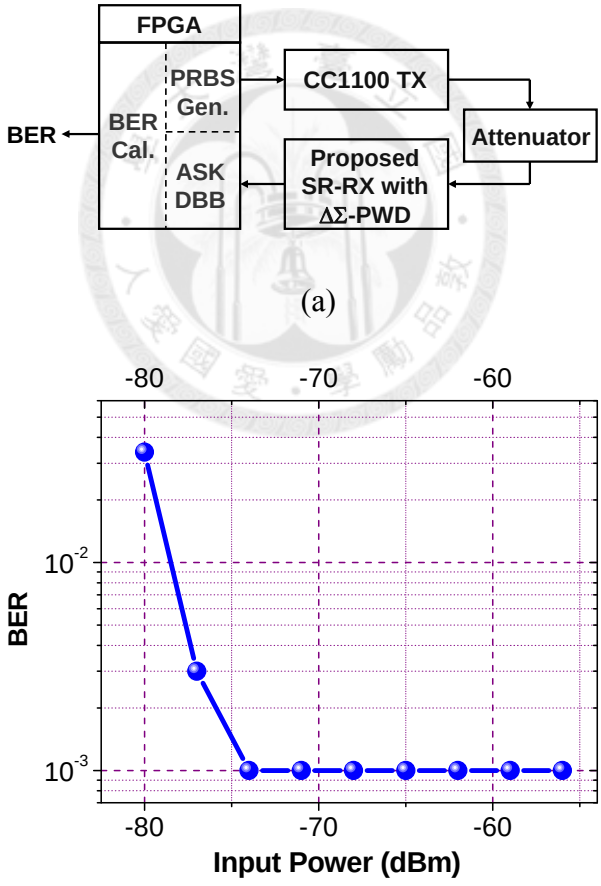


Fig. 4-14: Measured pulse width at different RF gain setting

Table 4-1: Measured Super-Regenerative Receiver Characteristic at Different Gain Setting

RF gain <1:0>	00	01	10	11
LNA bias current	200 μA	225 μA	250 μA	275 μA
Noise power (P_{noise})	-68 dBm	-80 dBm	-82 dBm	-85 dBm
Conversion gain (K)	3.1 ns/dBm	2.5 ns/dBm	1.6 ns/dBm	1.25 ns/dBm
Start-up time at noise level (T_{noise})	200-137=63 ns	200-126=74 ns	200-110=90 ns	200-86=114 ns
Power detection range	-50 ~ -35dBm	-70 ~ -40dBm	-80 ~ -50dBm	-85 ~ -55dBm

The proposed super-regenerative receiver is verified with the 156-kbps data rate ASK modulation. As shown in Fig. 4-15(a), the input RF signal is ASK modulated according to TX data, which is generated by consumer transceiver product CC1100. The output digital signal of ΔΣ-PWD (V_{QT}) is processed by the DBB circuit (which is implemented by a FPGA). Fig. 4-15(b) shows the super-regenerative receiver Bit-Error-Rate (BER) measurement. The receiver sensitivity is defined as the power level when BER is higher than 1%. This super-regenerative receiver with ΔΣ-PWD can achieve -78-dBm sensitivity. The BER performance is mainly limited by large RX-noise jitter and insufficient isolation between DCO and LNA input.



(a)

(b)

Fig. 4-15: (a) Time domain waveform of BER measurement, (b) BER versus input power

Fig. 4-16 shows the measured DCO oscillation frequency versus 6-bit frequency control words (i.e. CS<5:0>). The oscillation frequency is monitored by measuring the leakage of DCO oscillation signal at LNA input. The measurement shows the center frequency is monotonic decreasing. The DCO covers the frequency ranging from 390 MHz to 485 MHz, which can support FCC MICS band.

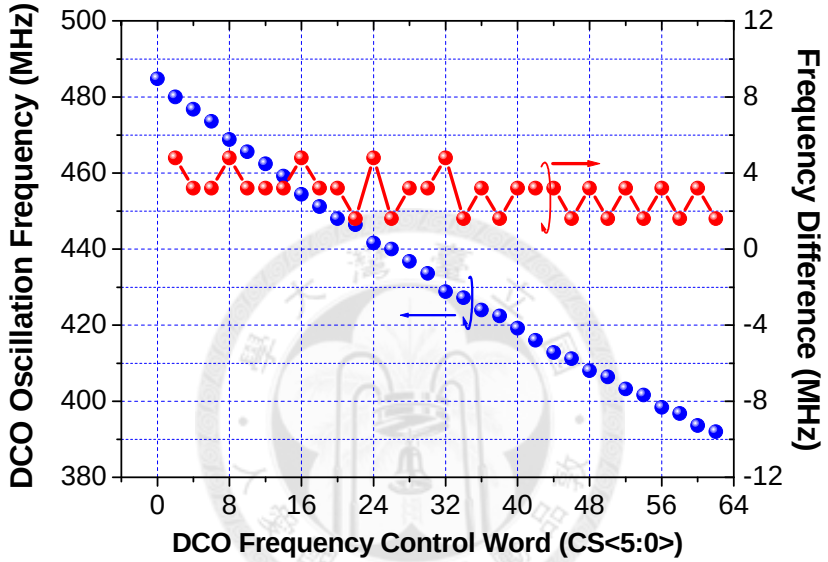


Fig. 4-16: DCO oscillation frequency versus 6-bit frequency control word

Fig. 4-17 shows the chip photo. This chip uses tsmc 0.18-μm CMOS technology with MIM capacitor and thick metal options. It occupies an area of 1.25 mm^2. Table 4-2 summarizes the measured super-regenerative receiver performance and compares with other similar works. This super-regenerative receiver achieves good energy efficiency (5.8 nJ/bit) even with the lossy on-chip spiral inductor. In addition, the proposed ΔΣ-PWD digitizes the pulse width with finest resolution.

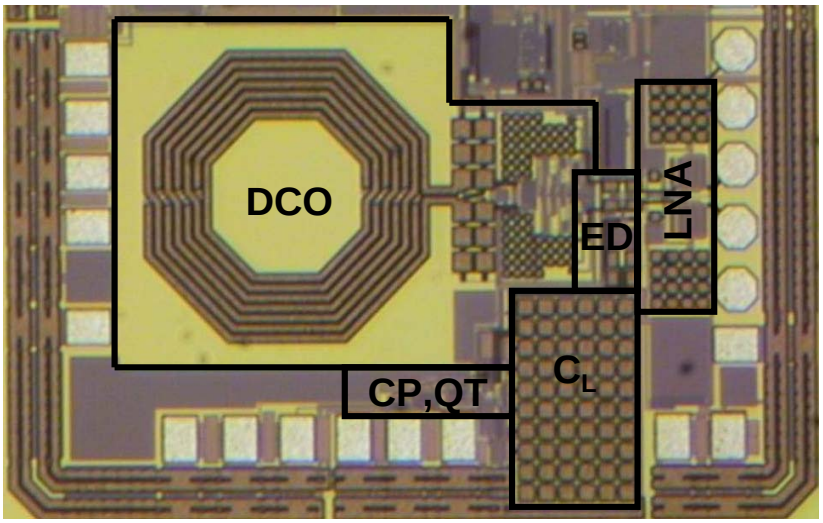


Fig. 4-17: Chip photo

Table 4-2: Performance Summary and Comparison of Super-Regenerative Receiver

	This work	[18]	[19]	[20]
Process	0.18 μm	0.13 μm	0.13 μm	0.18 μm
Supply Voltage	1.3 V	0.9 V	1.2 V	1 V
Operating Freq.	402 MHz	2 GHz	2.4 GHz	402 MHz
Data Rate	156 kbps	10 kbps	500 kbps	120 kbps
Sensitivity	-78 dBm	-100 dBm	-80 dBm	-93 dBm
Power	0.9 mW	0.4 mW	3.3 mW	0.35 mW
Energy/Bit	5.8 nJ/bit	40 nJ/bit	6.7 nJ/bit	2.9 nJ/bit
PW Detector	ΔΣ-PWD	LPF	Direct Sample	Direct Sample
RMS PW Error	**0.27 ns**	NA	60 ns*	3 ns*
DCO Resonator	On-chip	BAW	On-chip	PCB
*RMS pulse-width error of direct-sampling method is defined as $(T_S^2/12)^{0.5}$				

4.6 Conclusion

In this chapter, an ultra-low power super-regenerative receiver with high-resolution pulse-width digitization architecture is proposed for implantable bio-medical applications. The pulse-width digitization of super-regenerative receiver is

accomplished by applying Delta-Sigma modulator concept into pulse-width domain. In the proposed ΔΣ-PWD architecture, the drawbacks of the conventional pulse-width detection (low-pass-filtering and direct-sampling) architectures, such as quantization error due to insufficient sampling frequency, threshold voltage accuracy and data rate limitation, etc., are avoided.

One design trade-off of the proposed ΔΣ-PWD architecture is the selection of bit numbers and the over-sampling ratio. Both of them are dependent relation of each other. In the conventional Delta-Sigma Modulator design, both of them can be used to improve the quantization noise performance. However in the ΔΣ-PWD, the quantization noise can only be effectively improved by increasing the loop orders.

The proposed ΔΣ-PWD architecture is suitable to implement in low-voltage CMOS design. The high-resolution pulse-width digitization allows accommodating the CMOS digital signal processing capability to improve the overall receiver demodulation performance and flexibility. The time-domain signal processing of the proposed architecture enables the super-regenerative receiver to be less sensitive to analog non-idealities and PVT variations, and may lead to a more energy-efficient operation in advanced deep sub-micron CMOS processes. Moreover, the proposed ΔΣ-PWD can also be implemented in many other applications (e.g. sensor interface [31]) demanded for time-to-digital conversion.

Chapter 5
A MUX-based Dual-mode Uplink Transmitter: G/FSK Mode

5.1 Introduction

This dissertation proposed a MUX-based transmitter which can be adopted as a dual-mode FSK/PSK transmitter for uplink transmission. This chapter will firstly discuss the G/FSK transmitter implementation; whereas PSK transmitter will be individually presented in Chapter 6.

5.2 Proposed G/FSK Transmitter Architecture

Generally, FSK transmitters can be realized in PLL-based transmitter solutions for they are more hardware-efficient. In order to solve the issues of conventional PLL-based transmitter architectures mentioned in the Chapter 3, the block diagram of the proposed MUX-based pseudo-open-loop G/FSK transmitter architecture is depicted in Fig. 5-1. The proposed G/FSK transmitter consists of a PLL, a proposed Sigma-Delta modulated Phase Rotator (ΣΔ–PR), and frequency dividers. The PLL is designed to lock the VCO at a frequency slightly above twice the desired transmitter output frequency. The VCO output frequency is then divided by 2 to generate a set of multi-phase signals. G/FSK modulation signal is then synthesized by combining these multi-phase signals by the proposed ΣΔ–PR. In contrary to the conventional open-loop

topology, the VCO remains locked by the PLL continuously. Therefore, the proposed method prevents frequency instability and obviates periodic re-locking required in the conventional open-loop topology. In addition, since the frequency modulation is performed outside the loop, the data rate is no longer limited by the loop bandwidth, as in the closed-loop architecture.

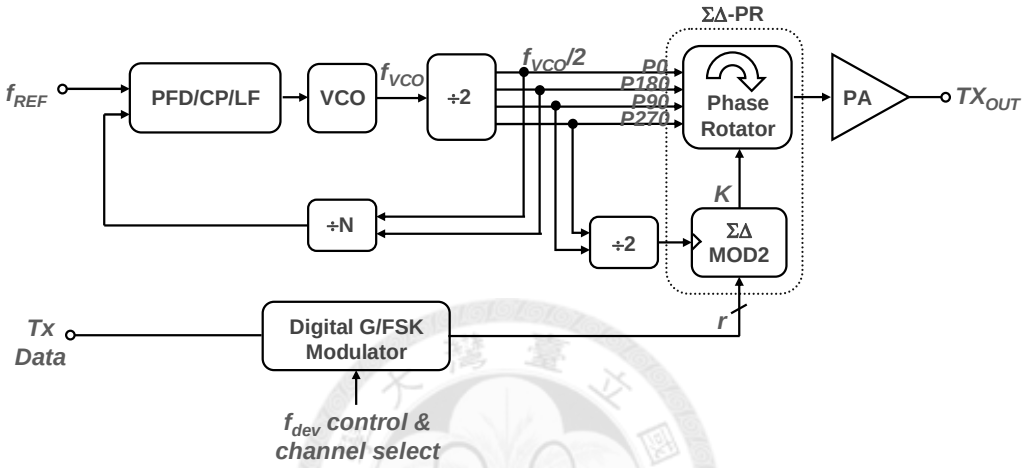


Fig. 5-1: Proposed MUX-based G/FSK transmitter architecture

The core of this architecture lies in the proposed ΣΔ–PR. A phase rotator (PR) takes multiple-phase input signals, and by properly combining these input phases, it can synthesize an output signal at a lower frequency [32, 33, 34 and 35]. Hence, it can serve as a fractional frequency divider. Its operation is usually based on the edge-combining principle. Fig. 5-2(a) illustrates the block diagram and the operation of a conventional edge-combined PR [32] which is composed of a Phase MUX, a Resampling stage, and a Phase Controller. In this circuit, if the input (f_{in}) to the PR is a set of 4 phase signals in quadrature, fractional frequency division with divide ratios of $1+K/4$ (K = 0, 1, 2, or 3) can be realized, with a divide-ratio step size of 1/4. Here, K is the phase control signal. It determines how the phases are selected for edge-combining. The frequency at the PR output can be expressed as

$$f_{out} = f_{in} \Big/ (1 + K \Big/ 4) \tag{4-1}$$

Evidently, the output frequency can be changed by selecting a different K value. However, for typical G/FSK applications, the frequency step from the conventional PR is too coarse to produce appropriate modulation signals. Furthermore, in the conventional PR architecture, a Resampling circuit triggered by the PR output is often employed to mask out the propagation delay of the Phase Controller. However, the propagation delay of the Phase MUX and the driving strength of the Resampling circuit, which are usually highly sensitive to process-voltage-temperature (PVT) variations, need to be well-controlled in order to ensure glitch-free phase transitions [32].

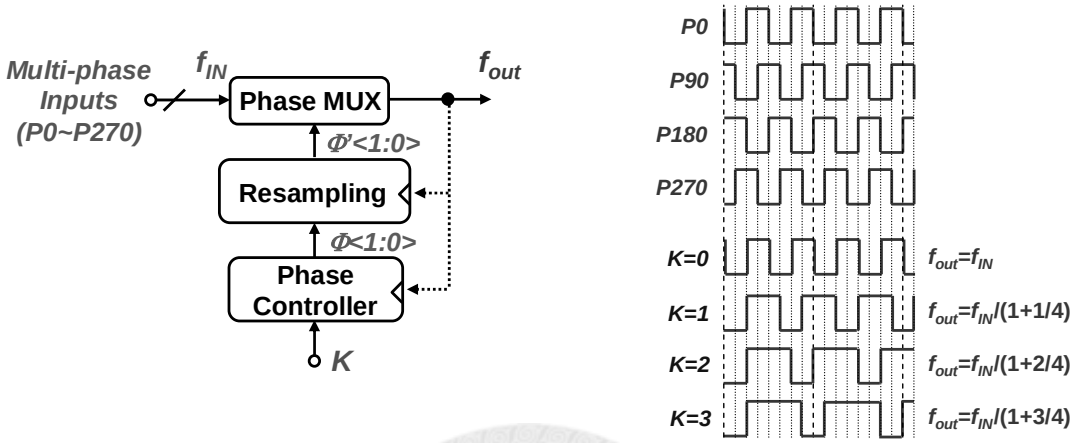
To obtain a finer frequency resolution, this dissertation proposes a ΣΔ–PR, where a dithered phase control signal K is applied to control the Phase MUX and produces an effective fractional frequency division step finer than 1/4. As illustrated in Fig. 5-2(b), the dithering operation is controlled by a Sigma-Delta modulator. In this work, the dithering operation is controlled by a 1-bit 2nd-order Sigma-Delta modulator (ΣΔ-MOD2). When a fractional number, r ($0 < r < 1$), is applied to the ΣΔ-MOD2, a modulated output bit stream K ($K = 0$ or 1) is produced to dither the Phase Rotator, and generates an average output frequency, f_{out}:

$$\begin{aligned} f_{out} &= r \times \frac{f_{in}}{1+1/4} + (1-r) \times \frac{f_{in}}{1+0/4} \\ &= f_{in} \times (1 - \frac{r}{5}) \end{aligned} \tag{5-1}$$

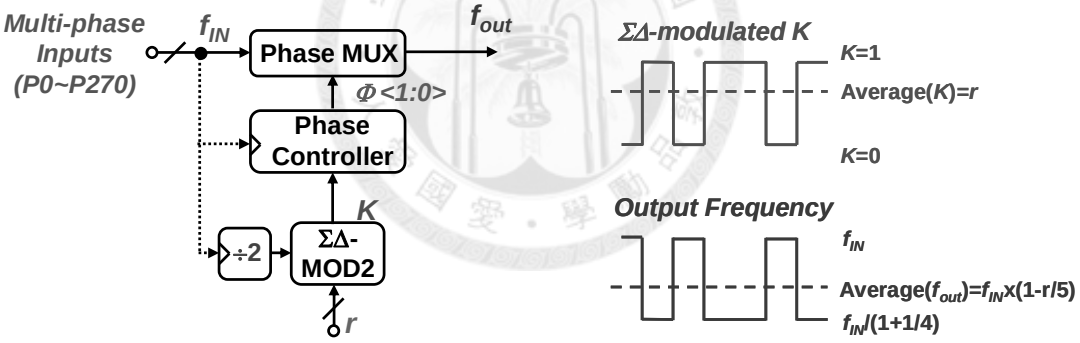
Therefore, a fine-resolution f_{out} is obtained by an appropriate selection of the word length to represent r. As a result, FSK modulation signals with a wide variety of frequency deviation and center frequency can be conveniently generated.

In the proposed ΣΔ–PR design (Fig. 5-2(b)), the Phase Controller is triggered by the input multi-phase signals to alleviate the propagation delay issue. The phase rotation (i.e.

edge combining) operation is therefore synchronized with the input signal. Hence, the timing margin and circuit driving strength requirements are relaxed such that the circuit is less sensitive to PVT variations compared to the conventional implementation.



(a)



(b)

Fig. 5-2: (a) A conventional PR and the corresponding waveforms with different phase control signal *K*, (b) the proposed ΣΔ-PR and its operation principle.

In short, the main idea of the proposed MUX-based G/FSK transmitter architecture is to generate modulation signals outside the PLL by using a fine-resolution fractional divider. In principle, one can also employ a ΣΔ-dithered divide-by-2/3 [32] frequency divider following the VCO to accomplish this task. In comparison with this approach, the proposed ΣΔ-PR following the divide-by-2 is essentially a ΣΔ-dithered divide-by-2/2.5 frequency divider. Therefore, the proposed implementation achieves a

smaller frequency step with better noise performance.

5.3 Noise Analysis of the Proposed ΣΔ-PR

Dithering the Phase Rotator introduces frequency quantization noise to the system. In this section, noise characteristic of the proposed G/FSK transmitter is investigated. The transmitter output noise power spectrum density (PSD) consists of the phase noise from the PLL (S_{θ_PLL}) and the modulation noise from the ΣΔ-MOD2 ($S_{\theta\_\Sigma\Delta}$). The noise PSD at transmitter output (S_θ) can be expressed as

$$S_\theta(f) = S_{\theta\_PLL} + S_{\theta\_\Sigma\Delta} \qquad (5\text{-}2)$$

Since the PLL noise has been well investigated in various literatures [27, 36], this section focuses on the noise due to ΣΔ-MOD2 (i.e. $S_{\theta\_\Sigma\Delta}$).

5.3.1 ΣΔ-PR Noise

The frequency at the ΣΔ-PR output is dithered by the ΣΔ-MOD2 with a frequency step (Δf) of $f_{in}/5$ (see (5-3)). Therefore, the output frequency variance is [37]

$$\sigma^2_{f\_\Sigma\Delta} = \frac{\Delta f^2}{12} = \frac{(f_{in} - f_{in}/1.25)^2}{12} = \frac{(f_{in}/5)^2}{12} \qquad (5\text{-}3)$$

The PSD of this dithered frequency is expressed as the variance divided by the sampling frequency of ΣΔ-MOD2, f_{CLK}, (here, f_{CLK} is half of the ΣΔ-PR input frequency, $f_{in}/2$) and then multiplied by the noise transfer function of the ΣΔ-MOD2 ($NTF_{\Sigma\Delta\text{-}MOD2}$), as expressed below.

$$
\begin{aligned}
S_{f\_\Sigma\Delta}(f) &= \frac{\sigma^2_{f\_\Sigma\Delta}}{f_{CLK}} \times NTF_{\Sigma\Delta-MOD2} \\
&= \frac{(f_{in}/5)^2}{12} \cdot \left(\frac{1}{f_{CLK}}\right) \cdot \left(2\sin\frac{\pi \cdot f}{f_{CLK}}\right)^4 \\
&= \frac{8}{75} \cdot f_{in} \cdot \left(\sin\frac{2 \cdot \pi \cdot f}{f_{in}}\right)^4
\end{aligned}
\tag{5-4}
$$

Since the phase noise is the integral of the frequency noise, the phase noise PSD is obtained by dividing the frequency noise PSD by the square of offset frequency, f, as expressed in (5-5).

$$
\begin{aligned}
S_{\theta\_\Sigma\Delta}(f) &= \frac{S_{f\_\Sigma\Delta}(f)}{f^2} \\
&= \frac{8}{75} \cdot \frac{f_{in}}{f^2} \left(\sin\frac{2 \cdot \pi \cdot f}{f_{in}}\right)^4
\end{aligned}
\tag{5-5}
$$

Equation (5-5) reveals that the noise $S_{\theta\_\Sigma\Delta}$ is high-pass shaped owing to the Sigma-Delta modulator operation, and is shifted away from the transmitter output frequency. Fig. 5-3 illustrates the simulated high-pass shaping characteristic of the $S_{\theta\_\Sigma\Delta}$. The noise due to ΣΔ-MOD2 is increased with a slope of 20 dB/dec. The noise from the ΣΔ-PR will dominate the output noise at higher offset frequencies. A high clock rate modulator and a transmitter output filter help to suppress the out-of-band noise and other spurious contents to some extent.

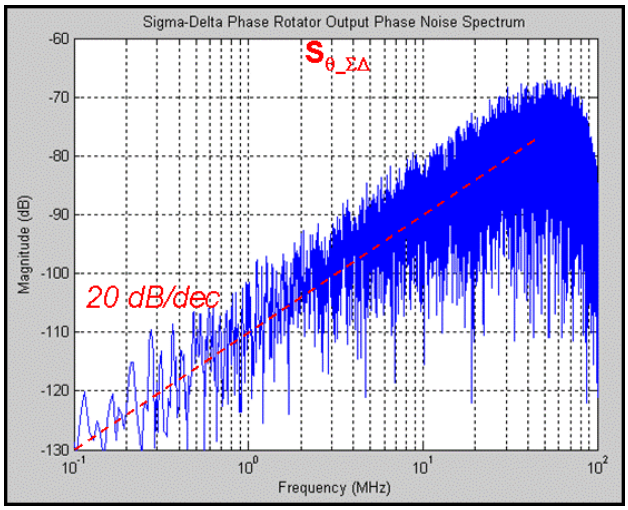
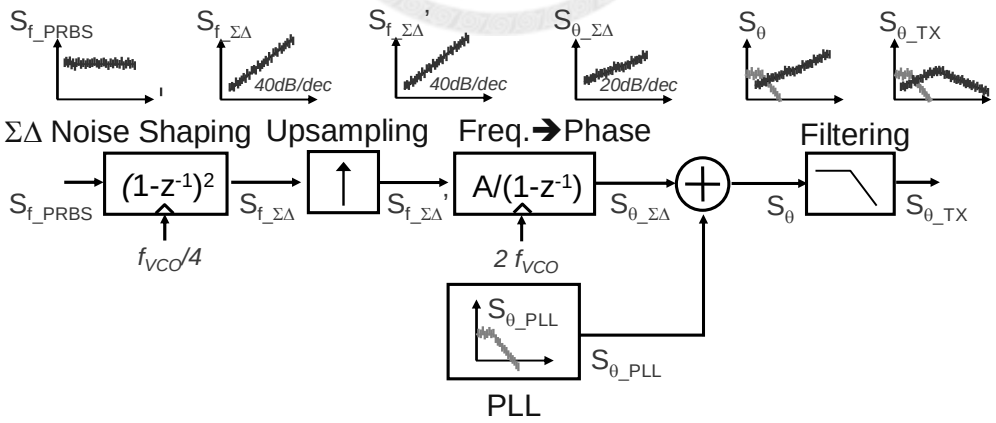


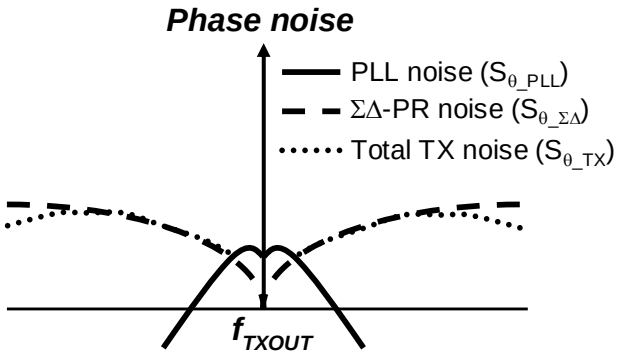
Fig. 5-3: Simulated phase noise PSD due to ΣΔ-dithering ($S_{\theta\_\Sigma\Delta}$)

5.3.2 Noise Analysis of the Proposed TX with ΣΔ-PR

In order to examine the noise contributions from the ΣΔ-PR and the PLL, and their effects on the total transmitter output noise, a phase-domain noise model is devised. As shown in Fig. 5-4(a), a white noise source and a 2nd-order differentiator sampled at a frequency of $f_{VCO}/4$ serve to model the ΣΔ-MOD2 frequency quantization noise ($S_{f\_\Sigma\Delta}$). A scaled accumulator transforms the $S_{f\_\Sigma\Delta}$ into the phase noise PSD ($S_{\theta\_\Sigma\Delta}$). The accumulator is clocked by a four-phase clock with a frequency of $f_{VCO}/2$, which is equivalently sampled at a rate of $2*f_{VCO}$. After summed with the PLL noise PSD (S_{θ_PLL}), the combined output noise PSD (S_θ) can be estimated. The combined noise is then filtered by the transmitter output filter. Fig. 5-4(b) conceptually illustrates the noise contributions from the PLL and the ΣΔ-PR, and the total transmitter noise (S_{θ_TX}). At high offset frequencies, $S_{\theta\_\Sigma\Delta}$ dominates the output noise performance; while at frequencies close to the carrier frequency, PLL dominates.



(a)



(b)

Fig. 5-4: (a) Noise modeling of the proposed TX; (b) plot illustrating various noise spectra and total TX output noise

5.4 Circuit Implementations

The proposed G/FSK transmitter, which consists of the ΣΔ-PR and a PLL operated at above twice the transmitter output frequency (see Fig. 5-1), is demonstrated in the 400-MHz frequency band. In this section, key building blocks are described in details.

5.4.1 High-speed Glitch-free Phase Controller (PC)

The proposed ΣΔ-PR operates on the 400-MHz multi-phase input signals and generates a phase-combined output. The "speed" of phase rotation is Sigma-Delta dithered to produce fractional frequency division with fine resolution. One key component of the ΣΔ-PR is the Phase Controller (PC). It determines how the input phases are combined in the Phase MUX. Fig. 5-5(a) shows the block diagram of the PC with the Phase MUX. The PC serves to detect and control how the phases are selected; whereas the Phase MUX combines the selected input phase signals (*P0 ~ P270*) according to the Phase State information (Φ<1:0>) from the PC. The detection and combining functions are implemented separately to relax the circuit timing constrains.

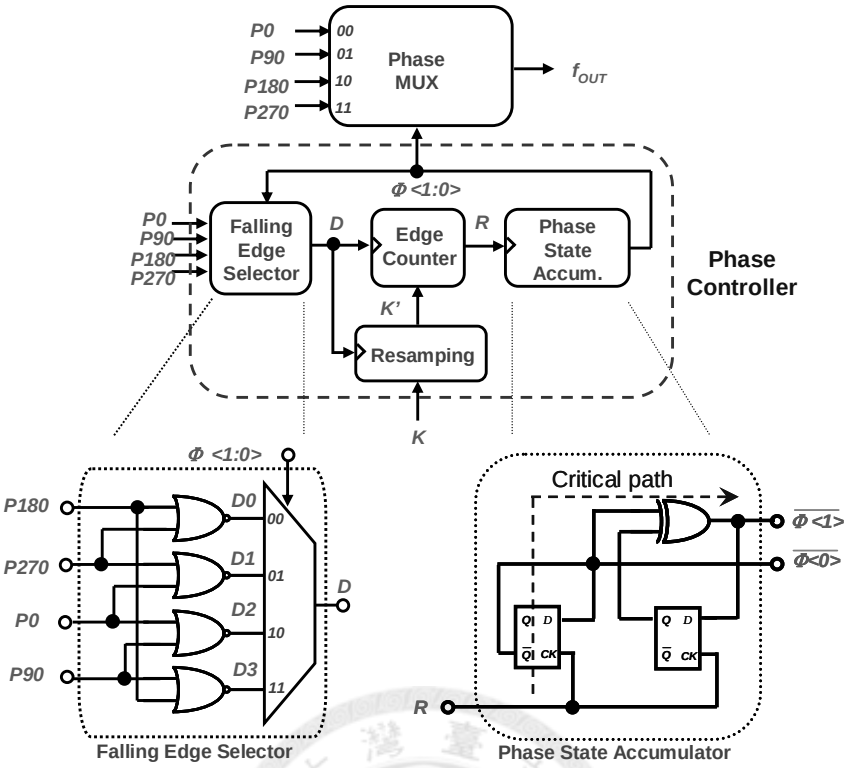
In Fig. 5-5(a), *K* is a 1-bit (0 or 1) stream from ΣΔ−MOD2. Depending on *K*, the frequency division ratio can alternate between 1 and 1.25 (see (5-1)). When *K*=0, the selected phase signal remains unchanged; the output frequency is the same as the input. When *K*=1, the Phase MUX selects the 4 phases sequentially, resulting in an equivalent divide-by-1.25 (/1.25) operation. To achieve a glitch-free and high-speed operation, the PC must be designed with care to ensure a smooth signal transition.

The PC (Fig. 5-5(a)) is mainly composed of a Falling Edge Selector (FES), an Edge Counter (EC), and a Phase State Accumulator (PSA). The operation timing diagram of the PC is depicted in Fig. 5-5(b), with the propagation delay ignored for simplicity. When *K*=1, to achieve seamless transitions between two adjacent phase signals (e.g. *P0* ➔ *P90*), Phase MUX should change its selection while both phase signals (e.g. *P0* and *P90*) are at the same logic levels (voltages). (If a transition from *P0* to *P90* occurs when *P0*=0 and *P90*=1, or *P0*=1 and *P90*=0, an extra pulse will appear at the output in the process of handover.) That is, the PC should update the Phase State Φ and trigger a phase signal transition under such condition. Furthermore, since the output period is longer than the input period (when *K*=1), the number of falling (or rising) edges of the input signal can be used as an indicator to signify when the phase transition should occur. Assuming the output is aligned with the input at the falling edges, if 2 falling edges from a given phase signal are detected, the PC will update the Phase State (Φ) and command the Phase MUX to move its selection to the next phase signal.

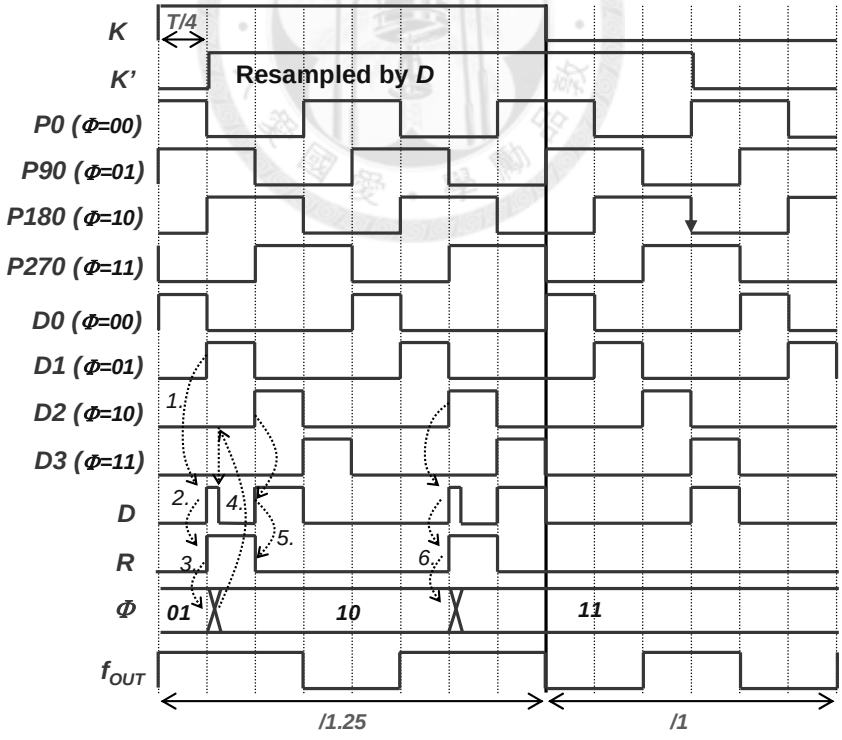
In the FES, before each arrival of the falling edges of the 4 input phases (*P0* ~ *P270*), a corresponding pulse signal (*D0* ~ *D3*) is generated (e.g. a positive pulse at *D0* is generated before the falling edge of *P0*). According to the 2-bit Phase State (Φ), one of these signals (*D0* ~ *D3*) is selected as the FES output, *D*. The signal *D* then triggers the EC which is a 1-bit counter. If *K'* is 1 (*K'* is the resampled *K*), the EC records the

number of *D* pulses (hence counting the number of falling edges). Overflow of EC output (*R*) indicates that a phase transition should take place. The EC output triggers the PSA (a 2-bit counter) to rotate the Phase State (Φ) sequentially. If *K'* is 0, the counting process is stopped; EC output and subsequently the Phase State remain unchanged. Therefore, the Phase MUX holds its previous phase selection. The Resampling circuit is added for timing alignment between *K'* and *D* to ensure a proper operation.

Fig. 5-5(b) explains the PC operation in details. Assuming at a certain instant, the Phase State, Φ*<1:0>*, is 01; as a result, *D=D1*, and the Phase MUX selects *P90* as its output. Before the arrival of the falling edge of signal *P90*, a positive pulse *D1* appears as *D* (step 1) and triggers EC. As a result, EC output (*R*) changes to 1 from 0 (step 2). The rising transition of *R* triggers PSA and increases the Phase State Φ*<1:0>* to 10 from 01 (step 3). The new Phase State (Φ*<1:0>*=10) commands the FES to select *D2* (which is at logic 0 at this instant) as its output *D* (step 4), and Phase MUX to select *P180* as its output. At this moment of phase handover, both signals *P90* and *P180* are at logic 1; hence the transition from *P90* to *P180* during this time interval is glitch free. Next, before the arrival of the falling edge of *P180*, a *D2* pulse is generated, causing *R* goes low (step 5). Finally, another D2 pulse arrives before the next falling edge of *P180*, and it triggers a change in *R* to update Φ*<1:0>* to 11 from 10 (step 6). The Phase MUX then moves on to the next phase signal, *P270*. The above operation constructs a glitch-free edge-combined output signal from the 4 input phases in a rotary sequence, and effectively divides the input frequency by 1.25. On the other hand, when *K*=0, the Phase State Φ<1:0> and hence the selected input phase signal remain unchanged. As a result, the divide ratio is 1.



(a)



(b)

Fig. 5-5: (a) Phase controller block diagram, (b) operation timing diagram

Fig. 5-5(a) also depicts the 2-bit PSA design. Conventional cascaded ripple counter is not suitable to implement this 2-bit accumulator for it has a long propagation delay. On the other hand, a typical 2-bit synchronous accumulator requires two DFF, three XOR, and two AND circuits [38], thus consuming a large current. The proposed PSA is optimized to achieve high-speed and low-power operation. The critical delay path of the PSA is also identified in Fig. 5-5(a), and the delay is carefully minimized to ensure an optimum operation of PC.

In Fig. 5-5(a), it can be observed that the FES, EC, and PSA form a digital feedback loop. Fig. 5-6 illustrates the simulated digital timing relationship of this loop when circuit propagation delays are present. T_C is the loop delay from the time signal *D* triggering the EC, to the next pulse signal (*D0* ~ *D3*) being selected as the FES output *D*. To ensure correct function of the high-speed PC, this loop delay (T_C) must be shorter than *T*/4, where *T* is the period of the input signal. This allows the following EC to record the number of *D* pulses properly.

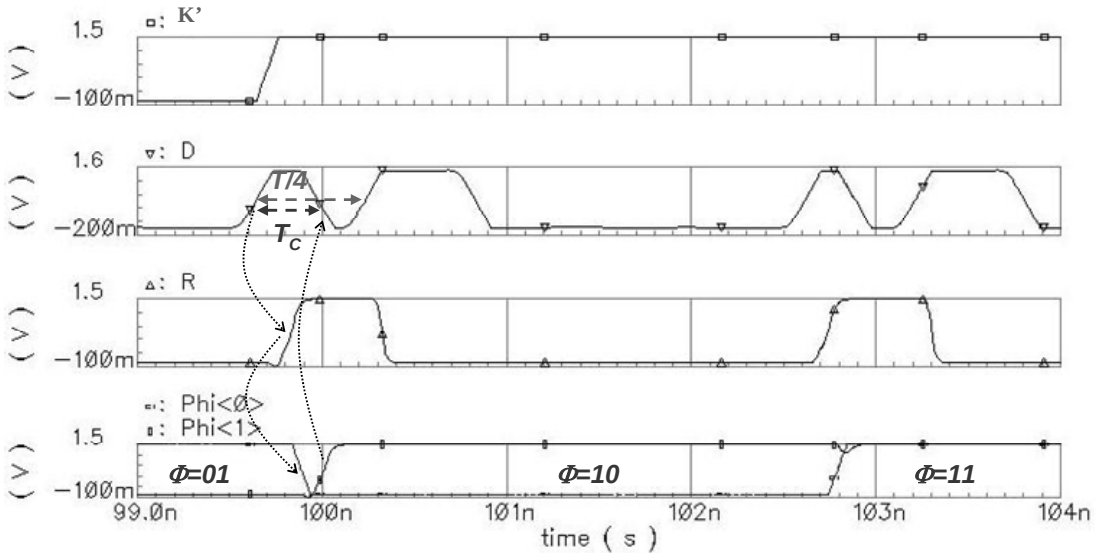


Fig. 5-6: Simulated digital timing waveforms of the digital loop

In the timing diagram shown in Fig. 5-5(b), the input multi-phase signals (*P0* ~ *P270*) are illustrated with 50% duty-cycle waveforms. If the signal duty cycle deviates from 50%, circuit timing margin is reduced. As the duty cycle moves away further, glitches during phase transitions will eventually occur. This will lead to increased spur levels and result in degradation of modulation accuracy. In this work, the input multi-phase signals are generated by the master-slave type divide-by-2 circuit [32] to ensure a reasonable 50% duty cycle.

5.4.2 High-speed Digital 2nd-order ΣΔ Modulator

The selection of the ΣΔ-MOD2 architecture is an optimization among speed, idle tones, quantization noise, and power consumption. The digital ΣΔ-modulator is implemented in a 2nd-order 1-bit single-loop architecture, as shown in Fig. 5-7 [24]. Multi-bit error-feedback MASH architecture is not adopted here, for it generates multi-bit output, which is not compatible with the single-bit phase control signal, *K*. The ΣΔ-MOD2 sampling frequency is chosen high (at half of the input frequency, around 200 MHz), in order to effectively shape the quantization noise. The feedback coefficients of the modulator are chosen to allow easy implementation (simply up-shifting the digital words) for reduced circuit complexity and facilitating high-speed operation. The input word length of the ΣΔ-MOD2 is 13 bits, making a frequency resolution of

$$f_{LSB} = f_{in} \times (1 - \frac{1}{1.25}) \Big/ 2^{13} \cong 10kHz \qquad (5\text{-}6)$$

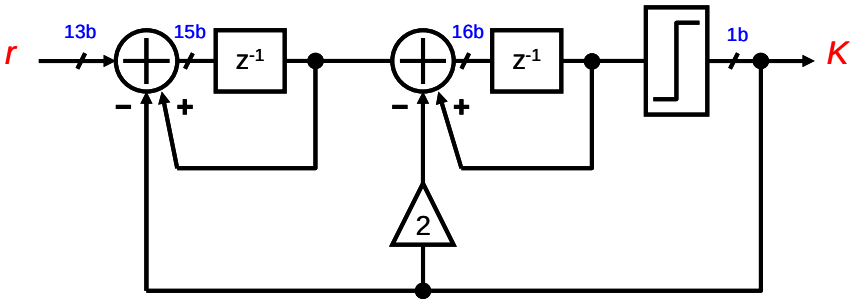


Fig. 5-7: Architecture of the 2nd-order 1-bit ΣΔ modulator

5.4.3 Digital G/FSK Modulator

Fig. 5-8 shows the digital G/FSK modulator, which implements core digital baseband functions. It includes a pseudo-random bit stream (PRBS) generator for characterization purpose, a FSK deviation frequency and data rate controller, and a 16-tape Gaussian FIR filter for GFSK modulation. Data MUX selects either the internal PRBS or external input data as the FSK data.

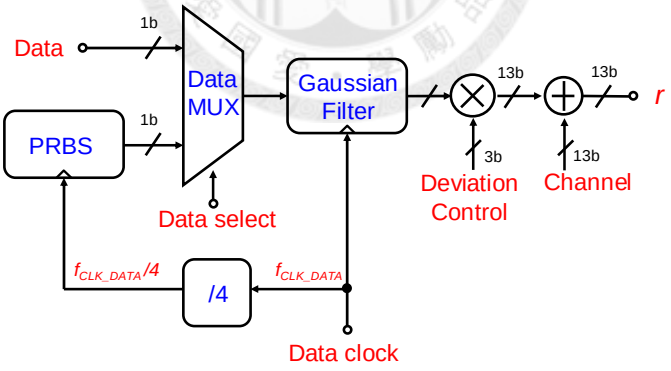
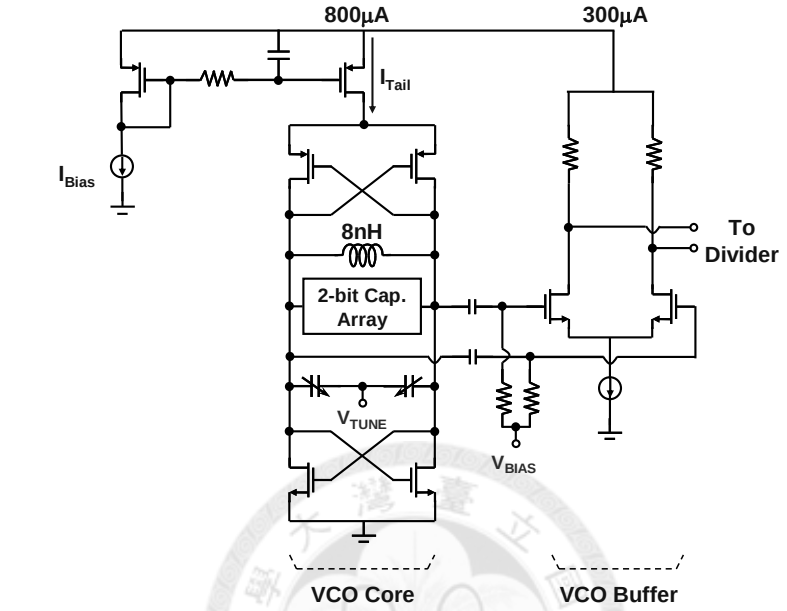


Fig. 5-8: Digital G/FSK Modulator

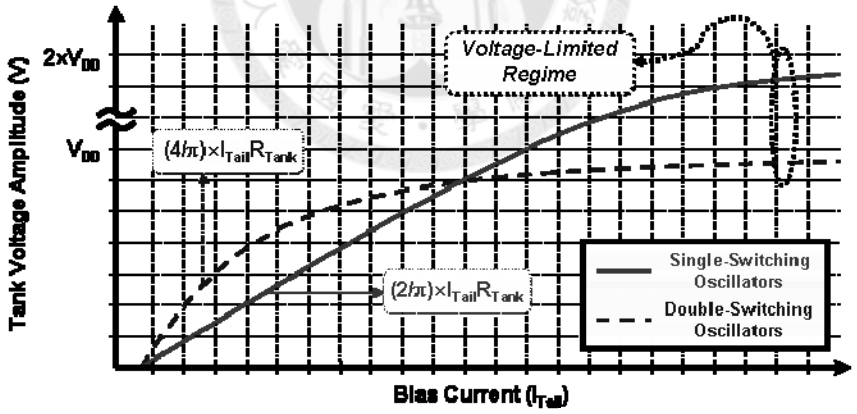
5.4.4 VCO

Fig. 5-9(a) shows the LC-VCO circuit which utilizes NMOS and PMOS double-switching pairs to reduce power consumption. Compared with the single-switching VCO, the double-switching VCO is easier to start-up and has higher

output voltage swing at low bias current, as shown in Fig. 5-9(b). To further reduce VCO current consumption, large inductance value (8 nH) is chosen to enhance the LC-tank resonant impedance (R_{Tank}).



(a)



(b)

Fig. 5-9: (a) Simplified schematic of the LC-VCO; (b) Comparison of the single-switching and double-switching VCOs

The VCO is operated at twice the carrier frequency. In addition to avoiding the pulling effect from PA, higher operating frequency also allows a smaller inductor with a

better quality factor. Moreover, the LC-tank impedance is increased at higher frequency, enabling a better oscillation condition.

The VCO covers frequencies ranging from 710 to 880 MHz, which supports transmitter output from 355 to 440 MHz. To cover the 20% tuning range while keeping a small VCO tuning gain (K_{VCO}), a 2-bit capacitor array is incorporated in the VCO tank circuit.

5.4.5 Frequency Synthesizer and Clock Plan

A frequency synthesizer must have a low phase noise to achieve a high-quality communication. In addition, a fast-locking frequency synthesizer is also preferable to minimize the energy wasted during the start-up period. This is especially important when the energy source is limited. In this work, the frequency synthesizer is based on a type-II phase-locked loop, as shown in Fig. 5.10. A CML divider divides the VCO frequency by two to generate quadrature-phase signals. To ensure balanced loadings among 4 phases and improve quadrature phase accuracy, signals with 0^o and 180^o phase are combined via a CML-to-logic buffer and send to the ΣΔ-MOD2; whereas signals with 90^o and 270^o are also combined in the same manner before reaching the prescaler of the PLL.

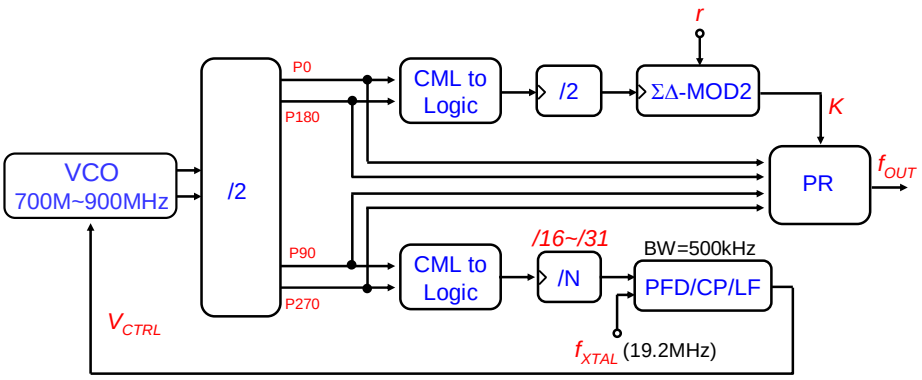
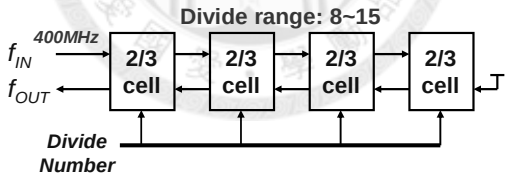


Fig. 5-10: Block diagram of the PLL implementation and clock generator

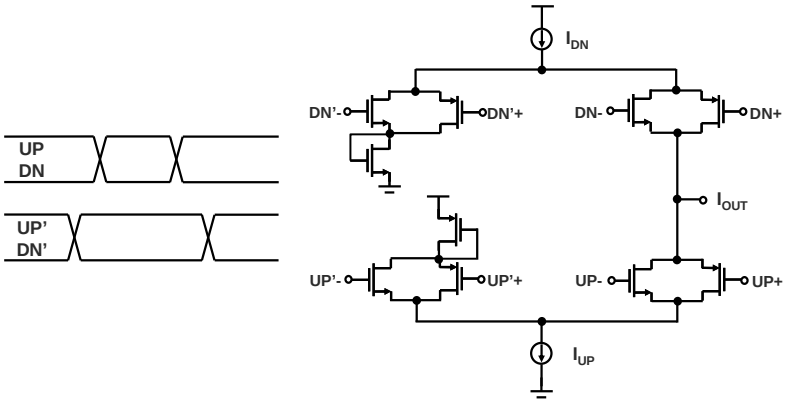
A loop bandwidth of 500 kHz is selected for it allows fast locking, optimum phase noise, and integration of an area-efficient 2nd-order passive loop filter. This 800-MHz frequency synthesizer consumes only 2.2 mA (including the VCO) from a 1.4-V supply.

The Prescaler adopts multi-modulus architecture with four stages of divided-by-2/3 cells, as shown in Fig. 5-11(a). Hence, the dividing ratio can be programmed from 8 to 15. The reference frequency is 19.2 MHz.

The $\Delta\theta \rightarrow I_{CP}$ linearity of PFD and Charge-Pump is an important parameter in terms of spurious performance of Frequency Synthesizer. Charge injection of switches in Charge-pump circuit is usually one of the dominant effects of $\Delta\theta \rightarrow I_{CP}$ linearity degradation. Therefore, the spurious suppression technique [43] is adopted in this work to improve the spectrum purity. Fig. 5-11(b) shows the Charge-Pump implementation and its control timing.



(a)



(b)

Fig. 5-11: (a) Multi-modulus divider; (b) charge-pump schematic and timing

5.5 Experimental Results

The proposed G/FSK transmitter is implemented in the TSMC 0.18-μm CMOS process. As shown in Fig. 5-12, the VCO covers frequencies ranging from 710 to 870 MHz, which supports G/FSK transmitter carrier frequency from 284 to 435 MHz. The PLL is measured with a 19.2-MHz reference crystal oscillator and a dividing ratio of 44 (N=22), which locks the VCO frequency (f_{VCO}) to 844.8 MHz. A 2nd-order passive loop filter is integrated on-chip. The PLL loop bandwidth is about 500 kHz.

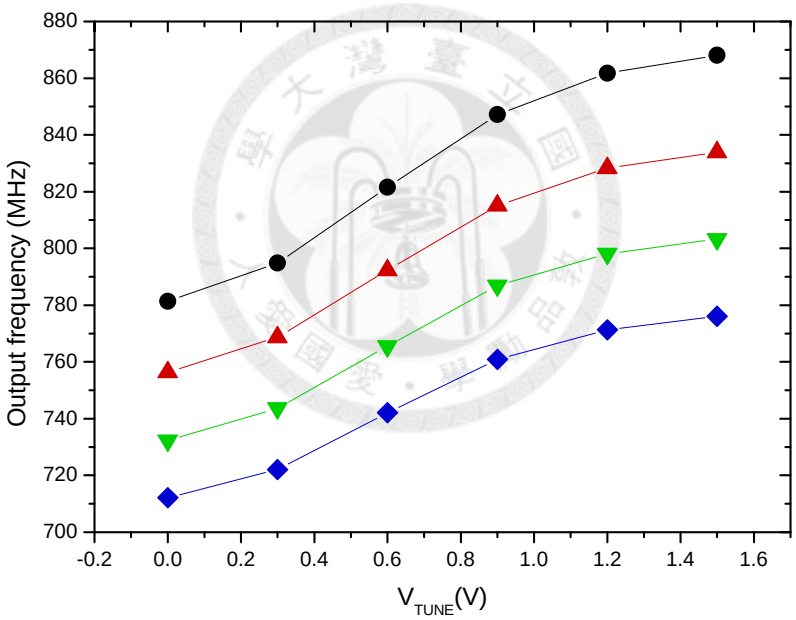
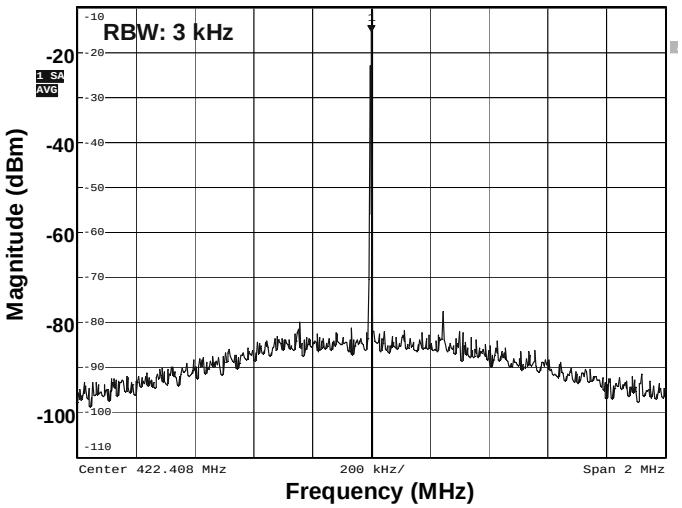
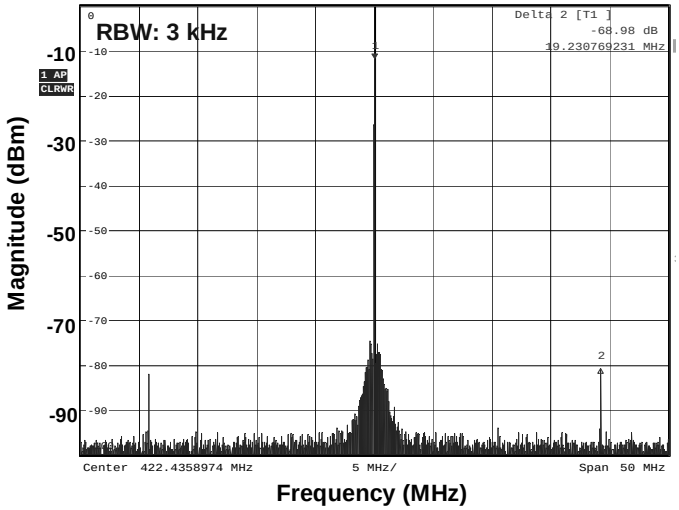


Fig. 5-12: Measured VCO frequency.

Close-in phase noise and spurs of LO signals are mainly contributed by the frequency synthesizer. They result in a rotation of the modulation constellation; thus degrading the EVM. Fig. 5-13(a) and 5-13(b) show the LO output spectra with a span of 2 MHz and 50 MHz, respectively. The reference spur level is suppressed to around -69 dBc. Fig. 5-14 shows the measured PLL start-up transient. With a loop bandwidth of 250 kHz, the PLL is settled within 16 μs.



(a)



(b)

Fig. 5-13: LO Spectra with (a) a 2-MHz span, and (b) a 50-MHz span.

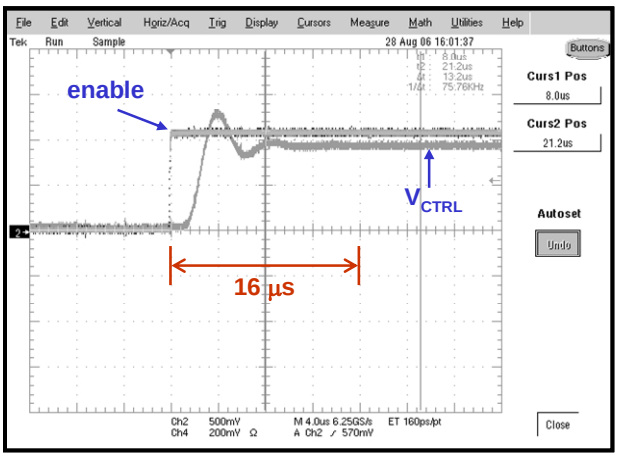
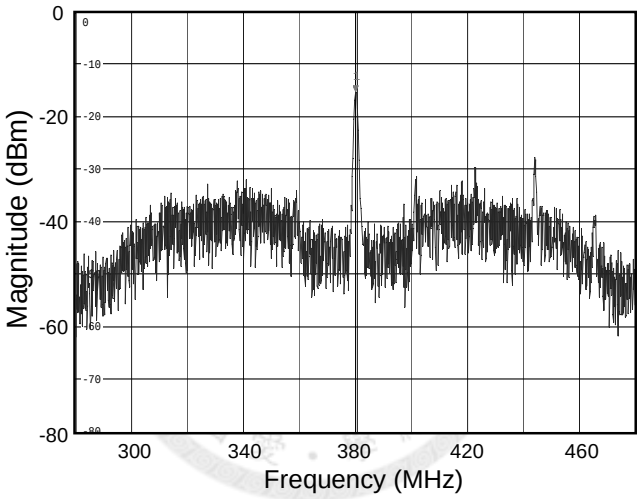
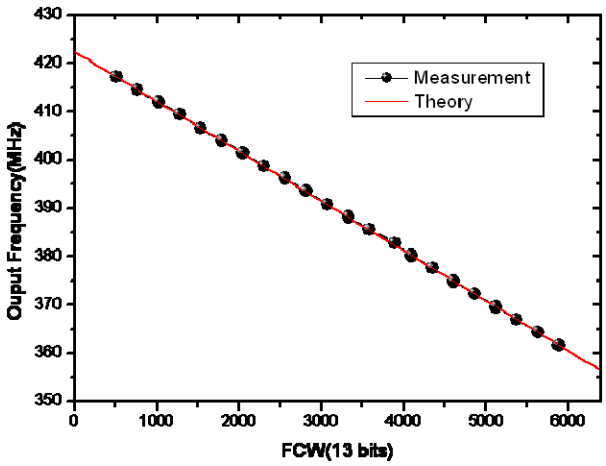


Fig. 5-14: Measured PLL start-up transient.

Fig. 5-15(a) shows the measured single-tone G/FSK transmitter output spectrum with r (see (5-2)) around 0.5. The close-in noise is about 30 dB below the carrier under a 1-MHz resolution bandwidth (RBW), which corresponds to a noise level roughly -90 dBc/Hz. The spurious tones at 22-MHz offset frequency and its harmonics at the transmitter output are originated from the idle tones of the ΣΔ-MOD2 and the non-linearity in the ΣΔ-PR operation. The characteristics of TX output frequency versus the 13-bit frequency control word (FCW) is plotted in Fig. 5-15(b). It shows a well-behaved characteristic as predicted in (5-1) (K in (5-1) is equal to FCW/2^{13})



(a)



(b)

Fig. 5-15: Measured (a) G/FSK transmitter single-tone output spectrum with a 200-MHz span; (b) frequency versus frequency control word (r).

The PLL phase noise (S_{θ_PLL}) measured at transmitter output (at a frequency of $f_{vco}/2$; when the ΣΔ-PR is disabled) is shown in Fig. 5-16. The PLL phase noise (measured at transmitter output) is -107.9 dBc/Hz and -110 dBc/Hz at 10-kHz and 100-kHz offset, respectively. The integrated phase error (from 1 kHz to 30 MHz) is only 0.31 degree. Fig. 5-16 also shows the measured and estimated total transmitter output noise (S_{θ}) when the ΣΔ-PR is activated. It is observed that the close-in phase noise is dominated by the PLL, while the phase noise at higher offset frequencies (i.e. larger than 10-MHz offset) is mainly contributed from the ΣΔ-modulation noise ($S_{\theta\_\Sigma\Delta}$). The measured total transmitter noise between 100-kHz to 10-MHz offset frequency is higher than that estimated from simulation. Further investigation into this discrepancy discovers that this is attributed to the resampling operation in the ΣΔ-PR. As described in Section IV-A, the resampling circuit is added for the purposes of timing alignment. However, this resampling operation deteriorates the noise-shaping characteristics of the ΣΔ-MOD2, resulting in higher noise. When the random modulation data are applied to the ΣΔ-MOD2 input, the magnitude of these spurious tones is lowered and has less impact on the modulation quality. Fig. 5-17 shows the measured modulation spectrum of 6-Mbps FSK signal.

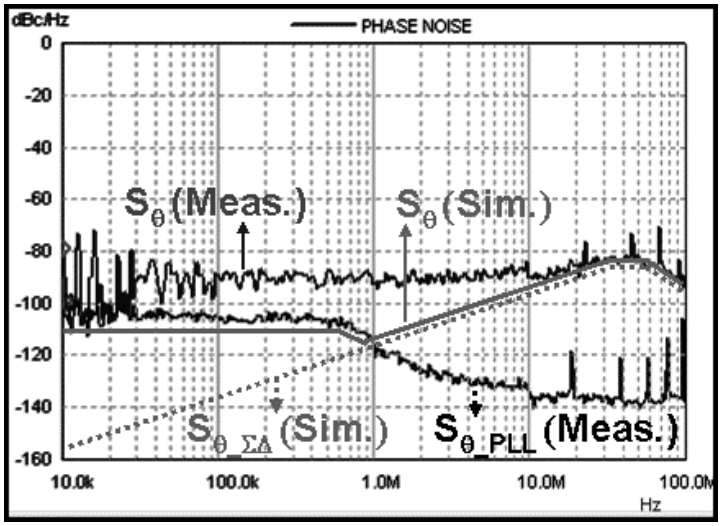


Fig. 5-16: Overlay of measured and simulated TX phase noise ($S_{\theta}=S_{\theta\_\Sigma\Delta}+S_{\theta\_PLL}$)

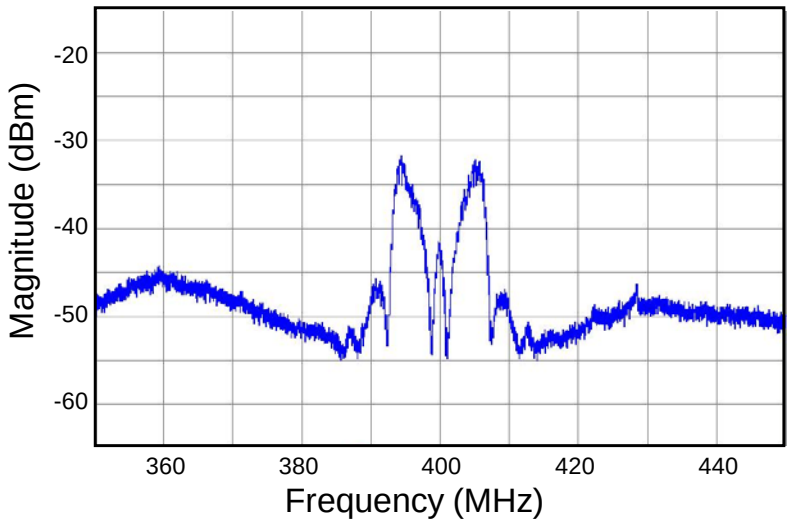


Fig. 5-17: Measured 6-Mbps FSK Modulation Spectrum

While the ΣΔ-dithering allows the Phase Rotator to achieve fine frequency resolution and wideband operation, the out-of-band emission performance is compromised as in other ΣΔ-dithered transmitter architecture [40]. This unwanted emission is regulated and is specified in various rules (e.g. [8]). Although the off-chip impedance matching network at transmitter output can help to lower the unwanted out-of-band noise power, the Q-factor of a low-cost matching circuit is typically limited (around 20). Its effect on noise reduction is also limited. If the transmitter is required to deliver a large output power, the out-of-band noise power also increases. A high-Q RF band-pass filter with a center frequency tuning circuit [40] is therefore needed to suppress the out-of-band noise power to below a level that satisfies the emission regulations. Since the required output power is low (< -10 dBm) in the targeted short-range wireless medical applications, the noise power and magnitude of spurious emission is also low. The filtering requirement is less demanding.

Fig. 5-18 depicts the transmitter modulation accuracy measurement setup. The proposed transmitter is verified with the 2-FSK and GFSK modulations. Fig. 5-19 shows the transmission quality measured at a center frequency of 403.2 MHz, by a

vector signal analyzer (VSA), Agilent MXA, The measured FSK errors at 6-Mbps data rate are 4.1% and 11.6% for 2-FSK and GFSK modulations, respectively. FSK error is defined as the ratio of the rms frequency jitter to the average FSK deviation frequency, and is a function of phase noise, deviation frequency, and transmission bandwidth [41]. In this architecture, the dominant source of FSK error is the modulation noise due to the ΣΔ-dithering (including the noise degradation caused by the resampling operation). Since this noise component theoretically increases with offset frequency, a higher transmission data rate (i.e. wider noise bandwidth) leads to a higher FSK error. For a given transmission data rate, FSK error can be improved by increasing the frequency deviation. However, this also increases the transmission bandwidth; thus limiting the improvement of the FSK error. Alternatively, employing a more sophisticated ΣΔ-modulator and resampling scheme may reduce the modulation noise; hence, lowering the FSK error. However, this is often at the cost of higher power consumption and design complexity. Fig. 5-20 plots the overall FSK and GFSK modulation quality under various transmission data rate (from 1 Mbps to 6.5 Mbps). Such signal quality is adequate for typical G/FSK demodulators to satisfy a BER of better than 10^{-3}.

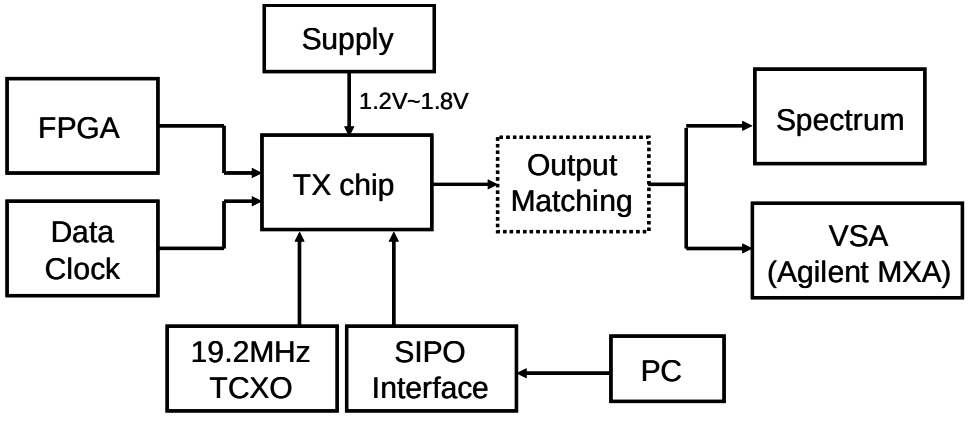
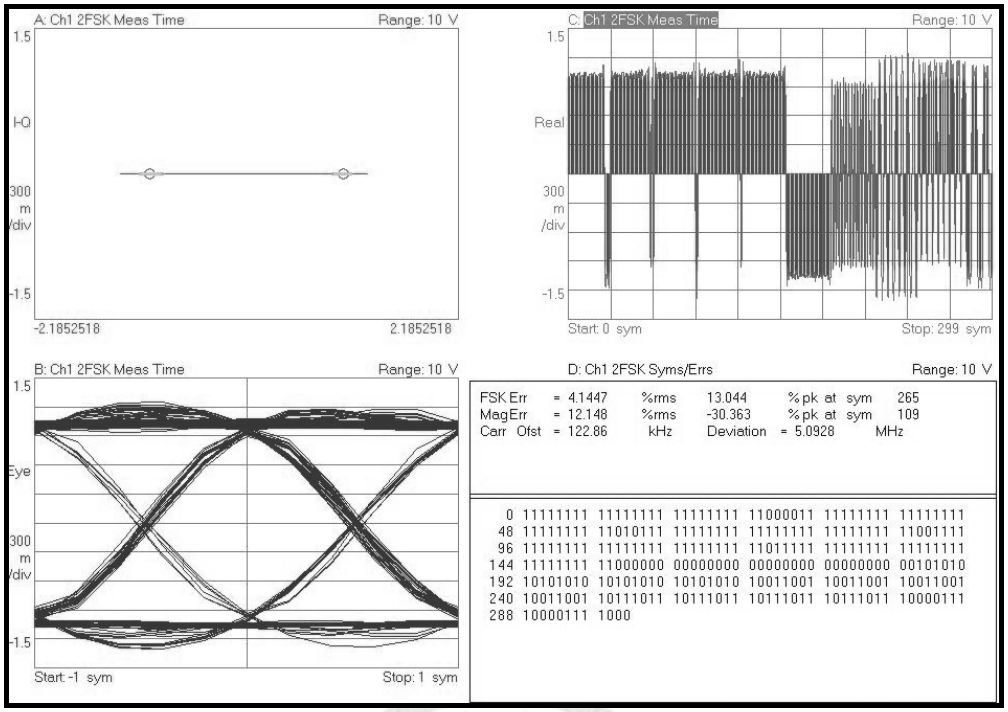
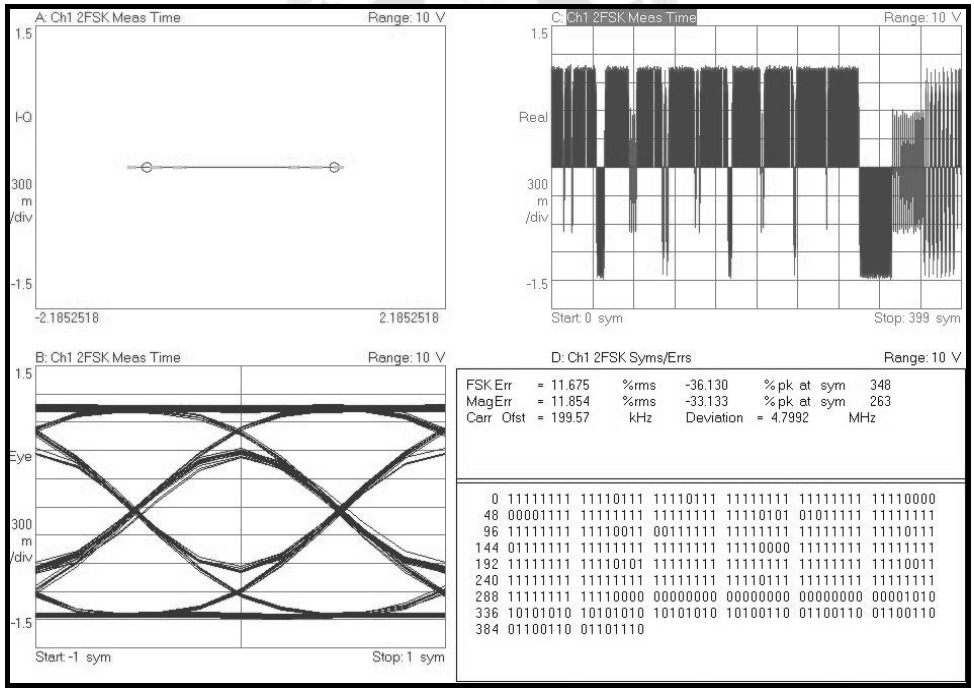


Fig. 5-18: Transmitter modulation accuracy measurement setup



(a)



(b)

Fig. 5-19: (a) Measured 6-Mbps FSK modulation characteristics at 403.2 MHz; (b) measured 6-Mbps GFSK modulation characteristics at 403.2 MHz

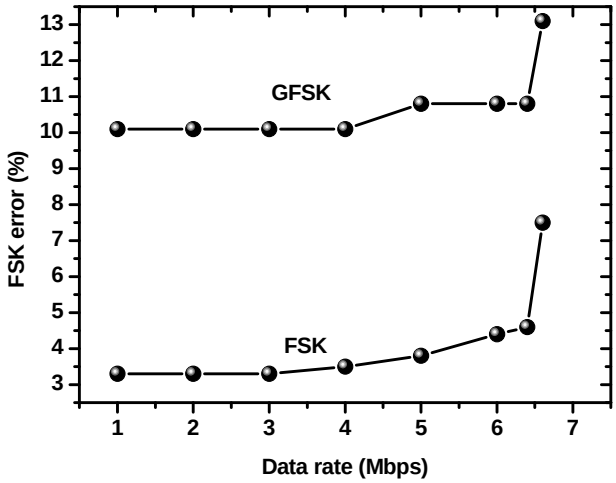


Fig. 5-20: Measured G/FSK errors versus data rate

Operated from a 1.4-V supply, the overall G/FSK transmitter draws 6.3 mA. This fully-integrated MUX-based G/FSK transmitter achieves an energy efficiency of 1.5 nJ/bit at 6 Mbps. Table 5-1 summaries the experimental results. The proposed G/FSK transmitter accomplishes a good energy-per-bit efficiency and delivers a reasonable output power level for short-range high-data-rate wireless applications.

Table 5-1: Performance Summary of G/FSK Transmitter

Modulation scheme	G/FSK
Process	0.18-μm CMOS
Supply voltage	1.4 V
Maximum data rate	6 Mbps
TX operating frequency	284 ~ 435 MHz
PLL bandwidth	500 kHz
PLL phase noise	-103 dBc/Hz @ 10 kHz
PA output power (P_{OUT})	-11 dBm
Total G/FSK TX current PLL (including VCO) ΣΔ-PR PA	6.3 mA 2.2 mA 3.5 mA 0.6 mA
Energy/bit (max. data rate)	1.5 nJ/bit

5.6 Conclusion

In this chapter, an energy-efficient MUX-based G/FSK transmitter architecture is proposed for high-data rate G/FSK applications. The modulation signals are generated by applying the FSK data to modulate the proposed ΣΔ-PR outside the PLL. In the proposed transmitter, the drawbacks of the conventional PLL-based (open-/closed-loop and two-point) architectures, such as VCO frequency drift, unsuppressed VCO phase noise, data rate limitation, accurate path matching requirement, etc., are avoided. In addition, the decoupling of the modulation and the frequency synthesizer loops allows independent optimization of the PLL for frequency planning, settling time, and phase noise considerations.

One issue with the proposed transmitter architecture is the noise contribution from the ΣΔ-PR operation. The high-pass noise shaping of the Sigma-Delta modulation results in elevated out-of-band noise power. High-Q filtering at transmitter output is required to suppress this noise component to below a power level specified by regulations. Fortunately, for the short-range bio-medical applications targeted in this dissertation, the transmitter is designed to deliver a low output power; hence, the out-of-band emission is also low. The filtering requirement is therefore relaxed and may be satisfied without resorting to complex filtering schemes.

The proposed transmitter architecture is inherently a digital design. The modulation characteristics, such as modulation schemes, carrier/deviation frequencies, and data rate, are easily programmable to adopt for different applications. The digital nature of the proposed architecture enables the transmitter to be less sensitive to analog non-idealities and PVT variations, and may lead to a more energy-efficient operation in advanced deep sub-micron CMOS processes.

Chapter 6
A MUX-based Dual-mode Uplink Transmitter: Offset-QPSK Mode

6.1 Introduction of Offset-QPSK Modulation

The O-QPSK modulation is a variant form of the QPSK modulation. The O-QPSK signal is generated by offsetting one of the data stream by half the symbol period. As a result, a transition between two diagonally opposite phases (e.g. Φ=11 and Φ=00) must pass through an intermediate phase (e.g. Φ=10), as illustrated in the constellation diagram in Fig. 6-1. This prevents the signal power from dropping considerably in the presence of finite circuit bandwidth during data transition. Therefore, the O-QPSK signal allows an efficient nonlinear power amplifier (PA) to be utilized for low-power consumption.

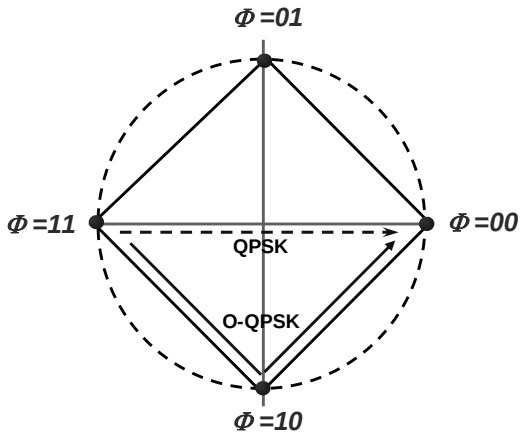


Fig. 6-1: Constellation of the O-QPSK modulation

6.2 Proposed O-QPSK Transmitter Architecture

To circumvent the problems of mixer-based transmitters mentioned in Chapter 3, a MUX-based (O-QPSK) transmitter is proposed in this chapter [42]. As shown in Fig. 6-2, in this architecture, the quadrature mixers in the conventional transmitter is transformed to the proposed Phase MUX. The Phase MUX selects one of the quadrature phases (P0 ~ P270) to the PA based on the basedband data (Φ<1:0>). Fundamentally, the proposed Phase MUX directly implements the quadrature phase-shift keying operation, and creates the desired O-QPSK/QPSK modulation signals in a hardware efficient way. In this architecture, the two power-hungry high-speed DACs and wide-bandwidth filters required in the conventional transmitters are eliminated.

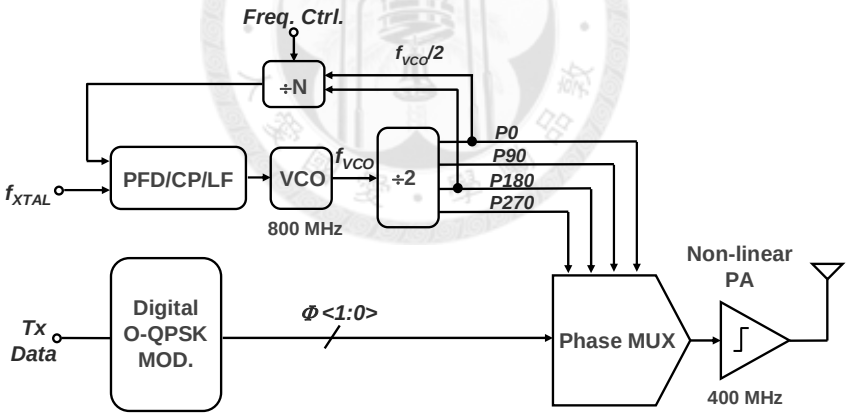


Fig. 6-2: block diagram of the proposed Phase-MUX-based O-QPSK transmitter

As will be explained in the next section, the Phase MUX consumes low power, and occupies small chip area, since large on-chip inductors for the mixers are no longer required. The digital O-QPSK modulator implements a compact digital baseband. The digital baseband data are utilized to control the Phase MUX operation. A charge pump frequency synthesizer operating at twice the transmitter output frequency is implemented in the proposed architecture. The VCO output is divided by 2 to generate

four phases in quadrature. Since the VCO is operated at twice the carrier frequency, direct pulling from PA is alleviated in this architecture. Furthermore, operating at higher frequency also enables a better inductor quality factor and increases the LC-tank impedance, which facilitates a better oscillation condition.

6.3 Circuit Implementation

As mentioned in chapter 5, the proposed ΣΔ Phase Rotator can also be adopted as a PSK-type transmitter. This can be achieved by direct selecting one of quadrature phases through the Phase MUX in the ΣΔ-PR while gating the FSK phase control signal by Data MUX, as shown in Fig. 6-3.

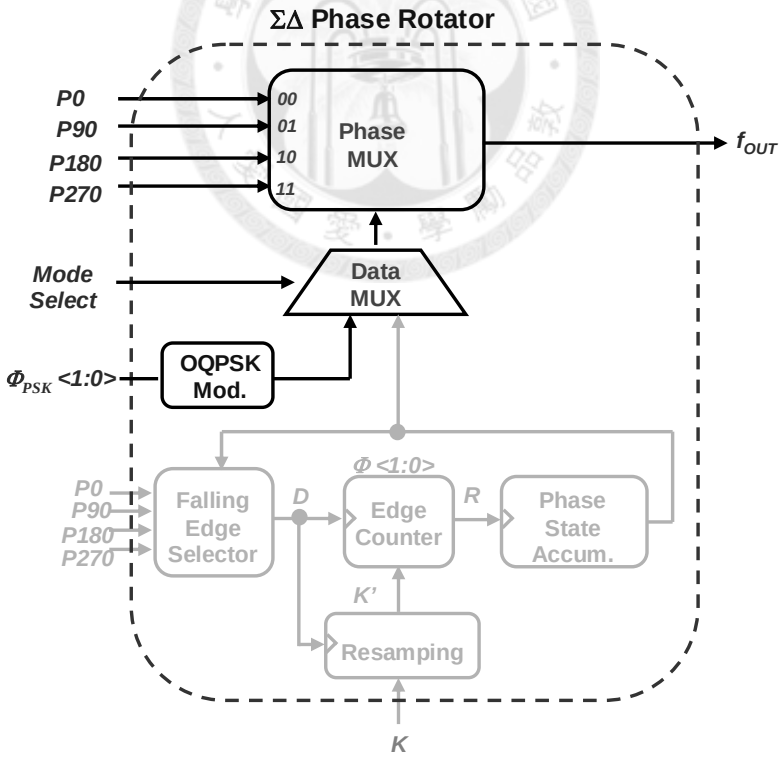


Fig. 6-3: Implementation of QPSK modulation using Phase MUX in ΣΔ Phase Rotator

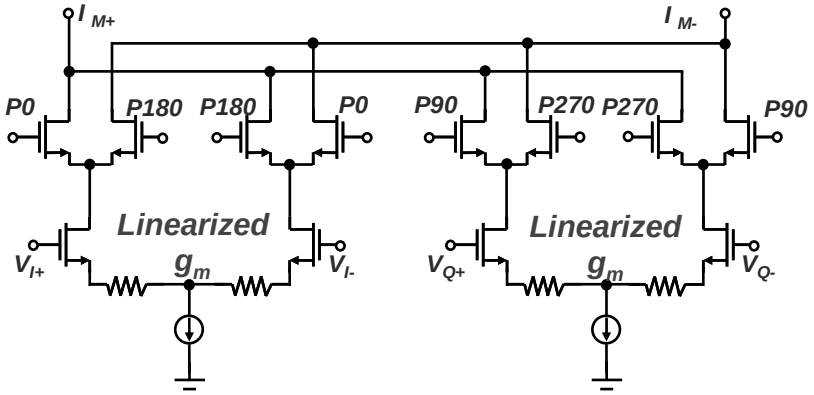
The proposed O-QPSK transmitter, which consists of a Phase MUX, a PA, and a PLL operated at twice the transmitter output frequency, is demonstrated in the 400-MHz frequency band. In this section, key building blocks, Phase MUX, PA and frequency synthesizer, are described in details.

6.3.1 Phase MUX

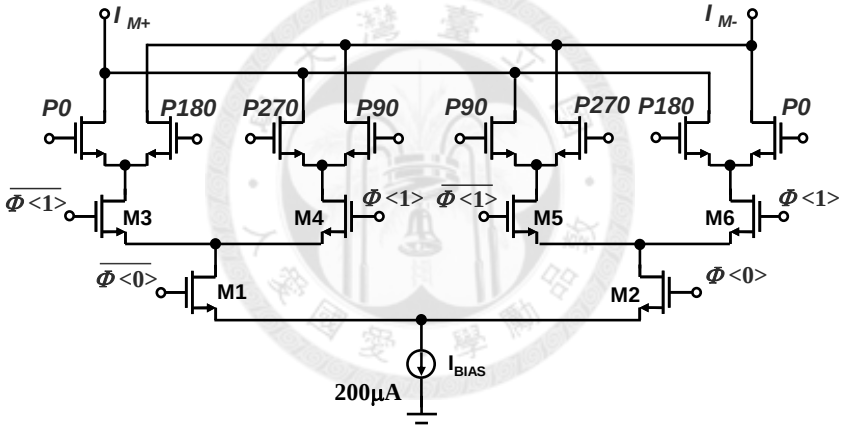
Before describing the Phase MUX circuit, we first examine a conventional implementation of a quadrature Gilbert-cell up-conversion mixer, as depicted in Fig. 6-4(a). The input trans-conductance (g_m) stage converts the input analog quadrature voltage signals (V_I, V_Q) into currents. The quadrature current signals are up-converted to the carrier frequency by the switching quads, and then are summed together in the current domain. In order to accommodate large baseband voltage amplitude while minimizing signal distortion, linearization techniques are usually adopted in realizing the g_m stage, which inevitably results in gain reduction. The power consumption of this conventional quadrature mixer is usually high in order to satisfy linearity and gain requirements simultaneously.

Fig. 6-4(b) shows the proposed Phase MUX circuit. The circuit selects a pair of complementary phases based on the data symbol Φ<1:0>. The Phase MUX can be considered as an over-driven quadrature Gilbert-cell mixer and is particularly suitable for generating PSK type of modulation signals. The proposed Phase MUX has several benefits. First of all, compared with the conventional mixers, this circuit is less sensitive to PVT variations, because there is no trans-conductance dependency in such a semi-digital implementation. Secondly, since there is no linearized g_m stage employed in this architecture, the Phase MUX avoids the gain and linearity trade-off that exists in

a conventional mixer design, thus allowing low-power consumption. Finally, large swings from the baseband data Φ<1:0> facilitate a fast circuit operation.



(a)



(b)

Fig. 6-4: (a) Schematic of a conventional quadrature Gilbert-cell mixer; (b) schematic of the proposed Phase MUX

6.3.2 Inverter-Type Power Amplifier

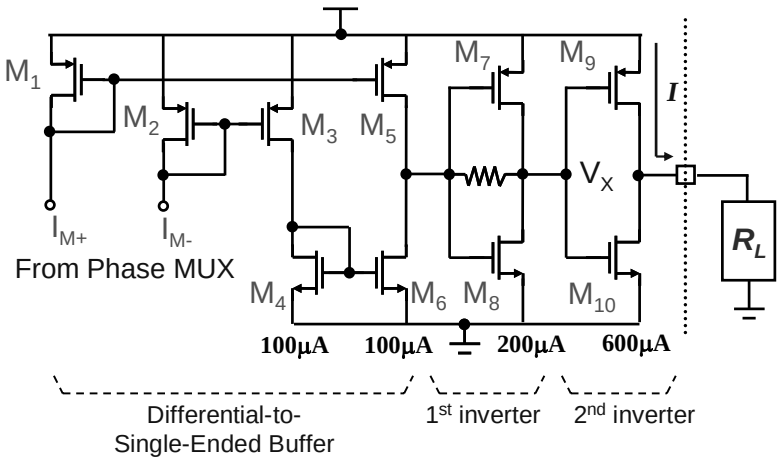
Fig. 6-5(a) shows the PA circuit implemented in this work. It is based on an inverter-type architecture. The differential currents from the Phase MUX output are first converted to single-ended form by the differential-to-single-ended buffer (M_1 ~ M_6),

and then drive two cascaded inverter stages. The 1st-stage inverter (M_7, M_8) is self-biased to maintain 50% duty-cycle waveforms, reducing the 2nd-order harmonic components. The 2nd-stage inverter (M_9, M_{10}) of the PA drives an external matching network.

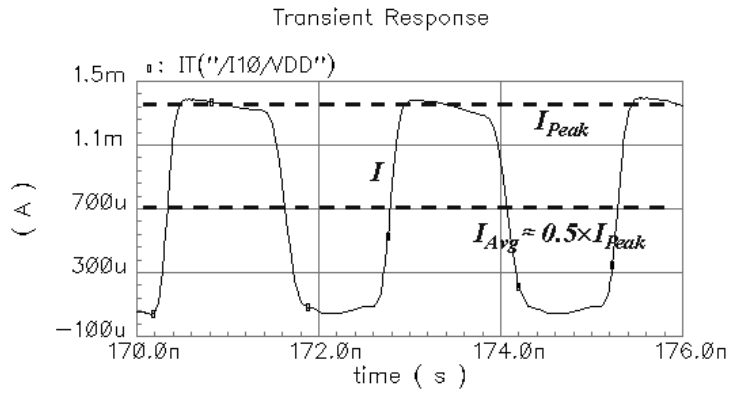
This inverter-type PA is compatible with the quasi constant-envelope nature of the O-QPSK modulation signal and has a better power efficiency. The efficiency is defined as the ratio of the output power to the average DC power consumption of the PA, as expressed in (6-1).

$$PA\ efficiency \equiv \frac{P_{OUT}}{DC\ Power} \approx \frac{2I_{Avg}{}^2 R_L}{V_{DD} \cdot I_{Avg}} \tag{6-1}$$

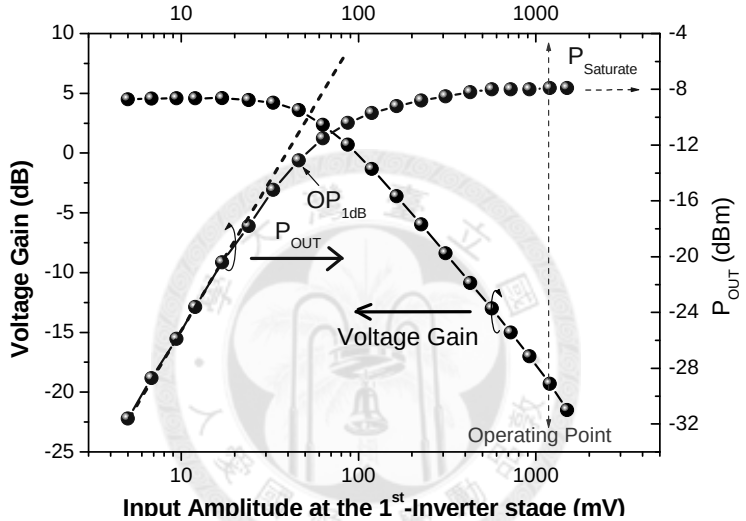
In (6-1), I_{Avg} is determined by the PA supply voltage, load impedance (R_L), device sizes, and the amplitude of the input driving signal. The simulated PA efficiency is around 15% at 1.5-V supply voltage. Fig. 6-5(b) shows the simulated output current waveform of the PA, which illustrates that the current waveform is close to 50%. Fig. 6-5(c) shows the simulated PA characteristics. The saturated output power is around -8 dBm, and the 1-dB compression output power is -12 dBm. This PA is designed to operate at the deep saturation region to achieve a better power efficiency.



(a)



(b)



(c)

Fig. 6-5: (a) The inverter-type power amplifier; (b) simulated output driving current of the PA; (c) simulated output power versus input driving voltage (at 1.5-V supply voltage).

6.3.3 Digital O-QPSK Modulator

Fig. 6-6 shows the digital O-QPSK modulator. The input 1-b TX data is sampled by two DFFs with inverted clock phases at half of the clock rate. This circuit produces a 2-b data stream, with one delayed by half symbol period with respect to the other. The data stream is then converted to the differential form for the Phase MUX. The input data

can be selected either from the pseudo-random bit stream (PRBS) generator or from an external data source by the Data MUX. The PRBS generator is implemented primarily for evaluation purpose.

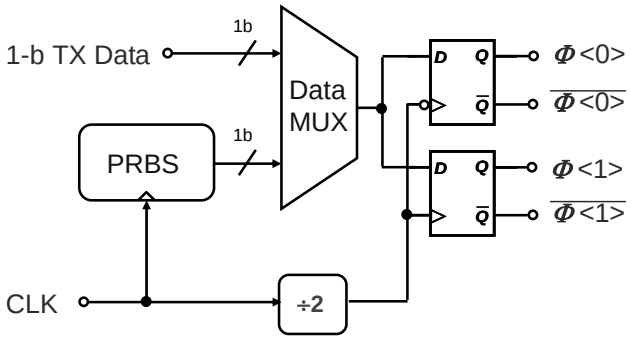


Fig. 6-6: Digital O-QPSK modulator

6.4 Design Considerations of the MUX-Based O-QPSK Transmitter

The performance of a wireless transmitter is affected by many factors, such as quadrature accuracy, analog offsets, nonlinearity, and phase noise [44]. Although the Phase-MUX-based transmitter is inherently more robust because of its semi-digital design, its performance may still be limited by some non-ideal effects. This section will discuss the limitation and design considerations of the proposed O-QPSK transmitter.

6.4.1 Quadrature Mismatch

The modulation quality of RF transmitters is significantly influenced by the quadrature gain and phase accuracy of the analog baseband and LO signals. The gain mismatch of a conventional quadrature mixer is dictated by the matching quality between the I-path and Q-path DACs, amplifiers, filters and mixer trans-conductor

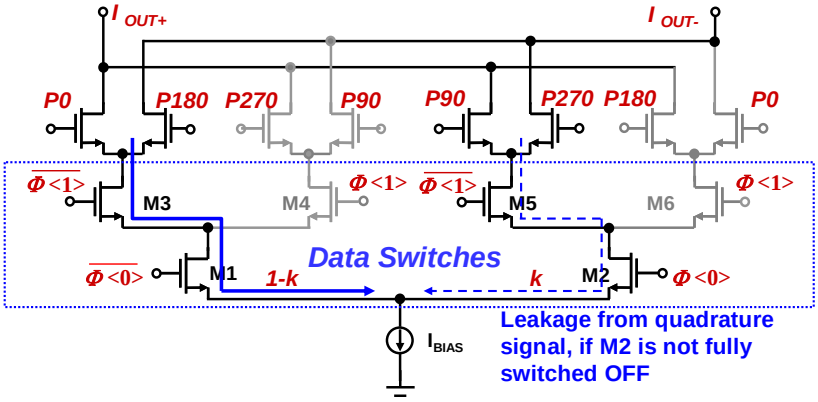
stages. In contrast, in the proposed architecture, better gain matching is inherently guaranteed because the same tail current source (I_{BIAS} in Fig. 6-4(b)) is shared between I and Q paths. In additional, the sources of mismatch are reduced since several analog circuits (e.g. DACs, filters, etc.) are removed from the signal paths in the proposed transmitter. The quadrature phase accuracy is ensured by well-balanced LC-VCO and divide-by-2 frequency divider designs.

6.4.2 Non-ideal Switching of the Data Switches

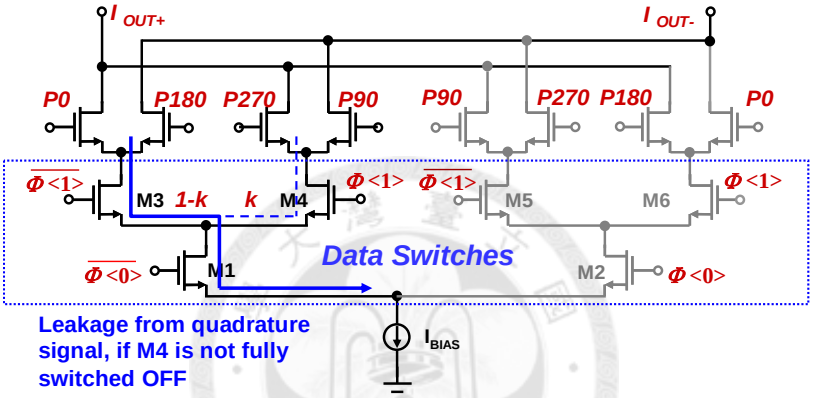
If the Data Switches of the Phase MUX (M1 ~ M6) are not fully switched, the signal leakage from quadrature phases would degrade the modulation accuracy. Fig. 6-7(a) illustrates the case when M1/M2 are not fully switched; while Fig. 6-7(b) illustrates the case when M3/M4 and M5/M6 are not fully switched. The quadrature phase current will leak to the output and sum with the desired phase current, rotating the I-Q constellation (see Fig. 6-7(c)). EVM degradation due to this phenomenon can be calculated by estimating the phase deviation, as expressed in (6-2), where *k* is the leakage percentage from the quadrature phase signal.

$$EVM_{DATA\_SW} \approx \tan^{-1}\left(\frac{k}{1-k}\right) \tag{6-2}$$

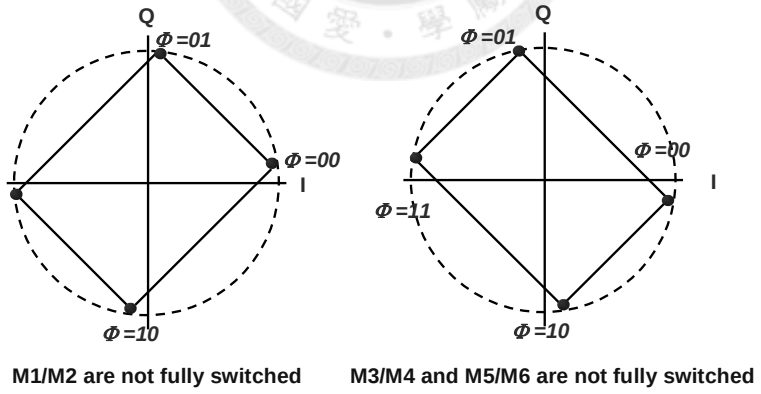
In the proposed transmitter, the input data (Φ<0> and Φ<1>) from the digital O-QPSK modulator are rail-to-rail signals. Incomplete switching of the Data Switches is therefore avoided in this design.



(a)



(b)



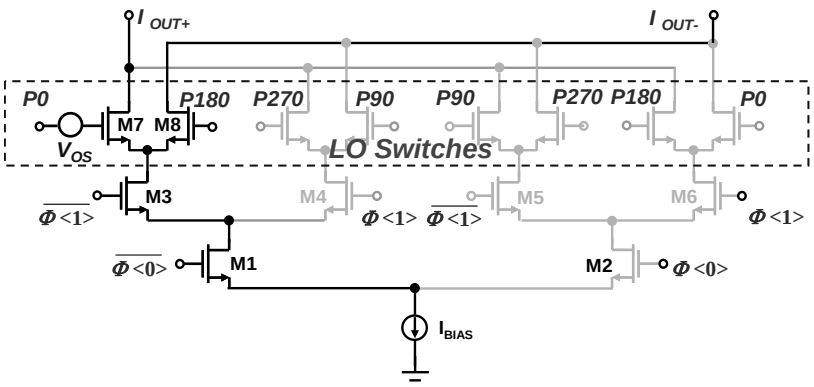
(c)

Fig. 6-7: (a) Non-ideal switching of Data Switches M1/M2, (b) Non-ideal switching of Data Switches M3/M4, (c) Non-ideal effects on I-Q constellation

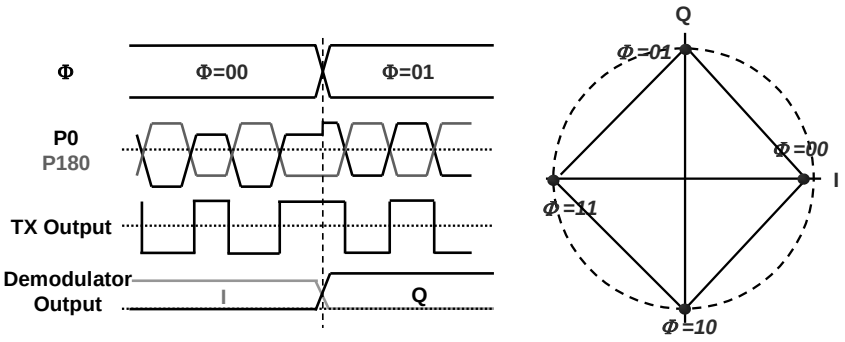
6.4.3 Offset of the LO Switches

LO leakage in RF transmitters also significantly affects modulation quality. It is mainly induced by DC offset voltage of the input trans-conductors and LO switches in the up-conversion mixers. Compared to a conventional quadrature mixer, the proposed Phase MUX is essentially free from the offset in the Data Switches (M1 ~ M6), since the effects of offset voltage are masked out by fully switching of these differential pairs.

However, the offset of the LO Switches will alter the duty cycle of output signal and degrade the modulation accuracy. As illustrated in Fig. 6-8(a) and 6-8(b), assuming an input-referred offset voltage (V_{OS}) exists at the LO Switches M7/M8, this offset voltage changes the duty cycle of the output signal. At the receiver, the altered duty cycle leads to a scaled DC value, thus changing the magnitude of the receiver demodulated output. Therefore, the modulation accuracy is affected. This non-ideality is generated in conjunction with the demodulation process in the external receiver; hence, the limiting action of inverter-type PA does not help in restoring the modulation accuracy. In order to reduce this duty-cycle variation, the slope of the LO signals (i.e. P0 ~ P270) should be made sharp enough to reduce the sensitivity of modulation accuracy to the LO Switches mismatches.



(a)



(b)

Fig. 6-8: (a) Offset of the LO Switches; (b) conceptual illustration of the offset effects on the modulation accuracy

6.4.4 Non-linearity

In a conventional transmitter, the nonlinearity is mainly attributed to the trans-conductor stages of the mixers and the PA. The linearity requirement is more demanding if a high-PAR modulation scheme is employed. In the proposed wireless interface and transmitter design, the linearity issue is relaxed by, first of all, choosing the low-PAR O-QPSK modulation scheme. Furthermore, the operation of the Phase MUX does not rely on linear trans-conductor stages; hence, eliminating this source of non-linearity.

6.5 Experimental Results

Fig. 6-9 shows the measured PA output power (P_{OUT}) and average current (I_{AVG}) versus supply voltage ($V_{DD,PA}$). By changing the supply voltage, output power can be adjusted to satisfy the up-link transmit distance requirements. The PA delivers around -15-dBm output power at 1.2-V supply voltage, which already can satisfy the 2-meter wireless link requirement for the target implantable neural recording applications. The

output power can be increased to -8 dBm when the PA supply voltage is raised to 1.8 V. The output power can also be increased by raising the bias current of the Phase MUX, which effectively increases the input amplitude of the PA.

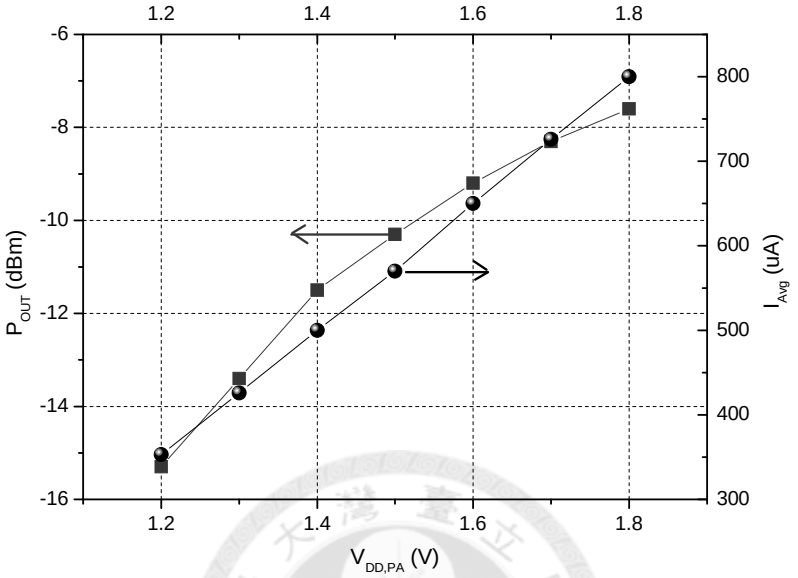
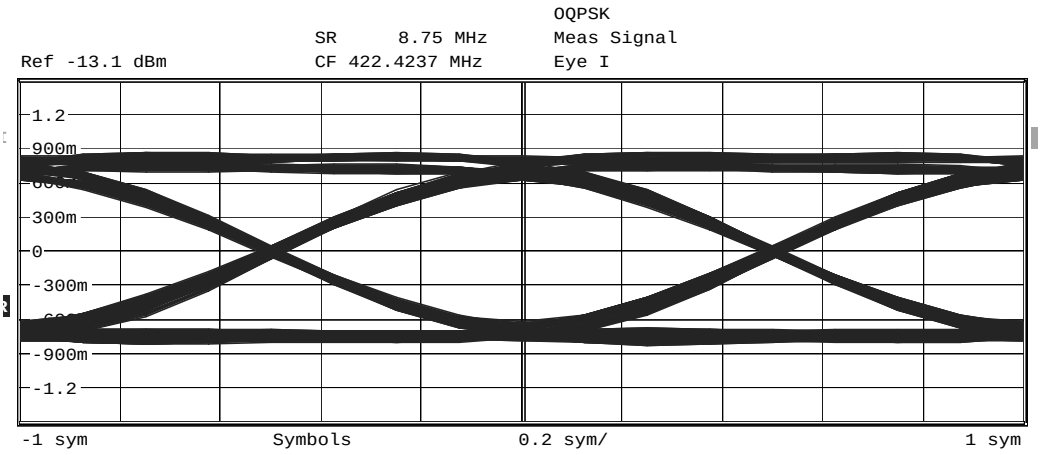
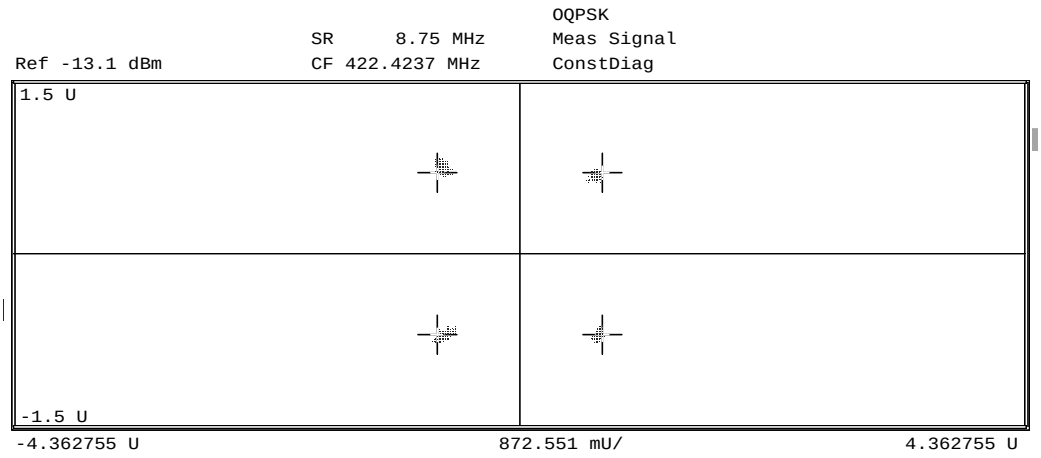


Fig. 6-9: Measured output power versus supply voltage

Fig. 6-10(a) and 6-10(b) shows the measured O-QPSK eye diagram, constellation, transmitter characteristics, and output spectrum (at 422.4 MHz) at a data rate of 17.5 Mbps. The transmission quality is measured by a vector signal analyzer (VSA) with built-in digital receiver filter. The modulated signal achieves an EVM of 7.2%, which is equivalent to 23-dB SNR. The EVM degradation is mainly attributed to quadrature phase mismatch, non-ideal switching of Data Switches, and phase noise of the LO signal. The modulation spectrum shows that 90% of the total output power is confined within 405 MHz to 440 MHz.



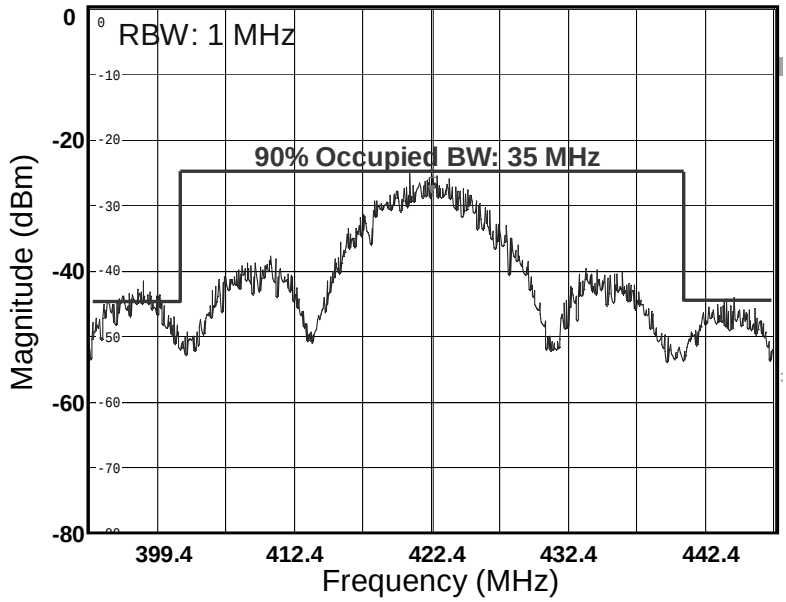


OQPSK
SR 8.75 MHz
Sym&Mod Acc
Ref -13.1 dBm
CF 422.4237 MHz

MODULATION ACCURACY				
	Result	Peak	atSym	Unit
EVM Offset	7.136	16.448	195	%
Magnitude Err	5.615	15.328	195	%
Phase Error	2.98	-7.28	81	deg
CarrierFreq Err	-15.90k			Hz
Ampt Droop	-0.02			dB
Origin Offset	-24.76			dB
Gain Imbalance	0.66			dB
Quadrature Err	0.57			deg
RHO	0.992694			
Mean Power	-16.86	-14.47	767	dBm
SNR (MER)	22.93			dB

SYMBOL TABLE (Hexadecimal)																	
00000	1	0	0	3	0	2	0	2	2	1	1	2	2	1	0	1	0	3
00018	0	2	0	1	3	2	2	3	3	2	2	3	0	0	3	1	3	2
00036	0	0	2	2	2	1	2	2	2	1	3	0	2	3	1	1	3	0
00054	1	1	1	0	1	1	1	0	2	0	1	2	3	3	1	3	3	3
00072	3	0	0	0	0	3	2	0	0	1	2	1	0	2	1	2	1	3
00090	0	3	0	2	2	0	3	3	2	3	0	1	0	1	0	2	0	2
00108	0	1	1	3	1	2	2	1	3	3	0	0	3	2	0	1	3	3
00126	3	1	0	1	1	0	2	1	3	0	2	2	0	0	2	1	2	3
00144	0	0	0	3	2	3	1	3	2	2	0	3	2	3	2	1	3	0
00162	3	1	1	2	3	1	1	1	3	1	1	2	2	3	1	3	1	0
00180	0	1	2	3	3	3	1	0	0	1	1	2	3	1	0	3	0	0
00198	1	2	1	2	3	0	3	3	3	2	1	0	3	1	3	0	0	1
00216	0	1	2	0	2	1	2	2	3	0	2	3	1	3	0	0	3	3

(a)



(b)

Fig. 6-10: (a) Eye diagram, constellation and modulation characteristics, (b) output spectrum

Fig. 6-11 plots the overall O-QPSK modulation quality (in measured EVM) versus various transmission data rate (from 1 kbps to 17.5 Mbps). As shown in Fig. 6-11, the signal quality up to 17.5 Mbps are more than adequate for typical O-QPSK demodulators to satisfy a BER of better than 10^{-4} (i.e. 23% EVM).

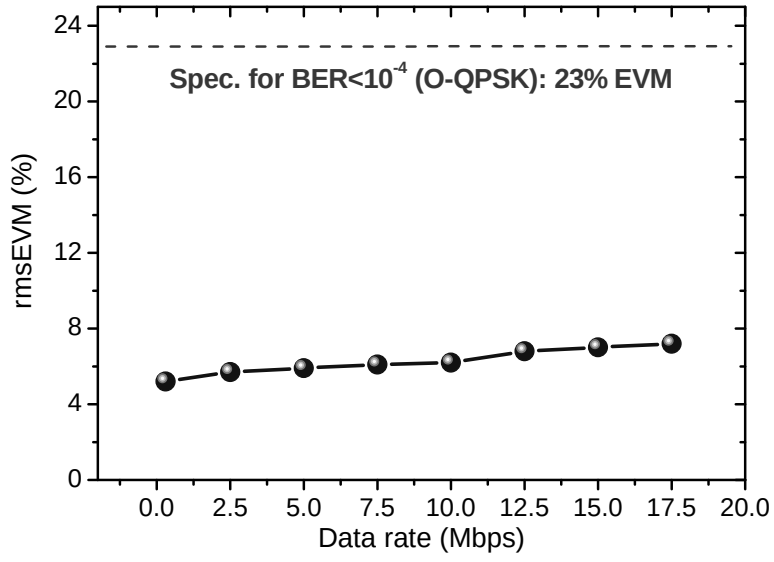


Fig. 6-11: Measured transmitter OQPSK EVM versus various data rate

Fig. 6-12 shows the dual-mode transmitter chip photo. The whole chip occupies an area of 1.2 mm^2; while the core circuits occupy 0.7 mm^2. The proposed ΣΔ-PR and PA only utilize a very small portion of the chip area since no inductor is required for these two circuits. The whole transmitter only incorporates one inductor, which is employed in the LC-VCO.

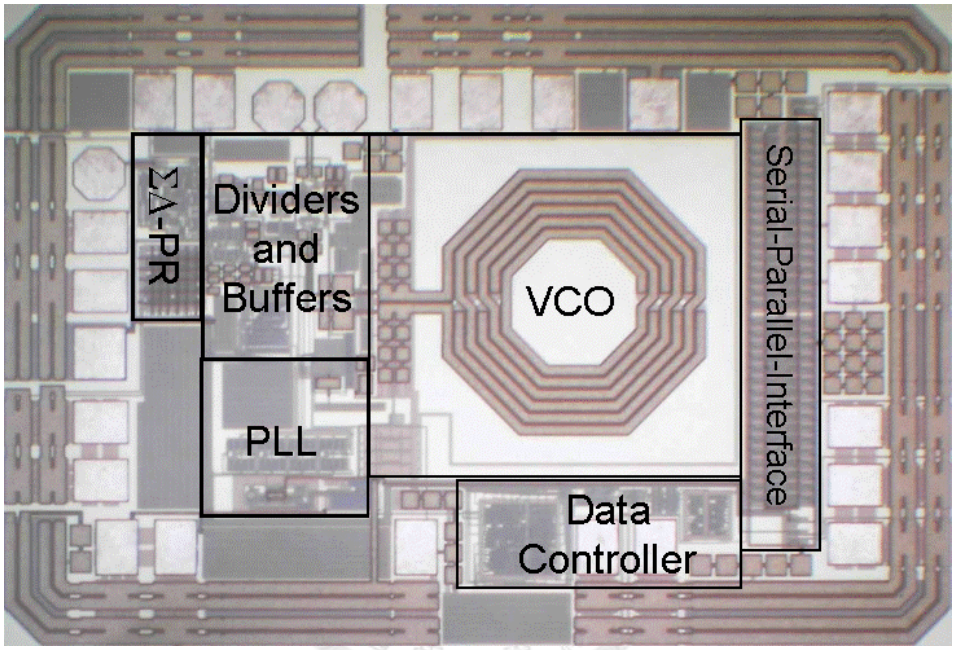


Fig. 6-12: Chip photo

Table 5-1 summaries the experimental results of the proposed O-QPSK transmitter. The complete O-QPSK transmitter consumes only 2.9 mA from a 1.2-V supply voltage. It achieves an energy efficiency of 200 pJ/bit at a data rate of 17.5 Mbps. Although the PA is usually the most power hungry component in a long-range wireless communication system, it is the VCO and PLL that dictates the power consumption in a short-range application as in this work.

Table 6-1: Performance Summary of O-QPSK Transmitter

Process	0.18-μm CMOS
Supply Voltage	1.2 ~ 1.8 V
Operation Frequency	355 ~ 440 MHz
Data Rate	1 kbps ~ 17.5 Mbps
P_{OUT}	-8 dBm @ $V_{DD,PA}$=1.8V -15 dBm @ $V_{DD,PA}$=1.2V
Bias Current (Total) PLL VCO + Buffer Phase MUX + Buffer PA	2.9 mA (at V_{DD}=1.2V) 1 mA 1.1 mA 0.4 mA 0.4 mA (0.8 mA at $V_{DD,PA}$=1.8V)
Chip area (Core area)	1.3 mm × 0.9 mm (0.85 mm × 0.55 mm)

Table 6-2: Performance Comparison with Other Low-Power Transmitter Works

	This Work		[11]	[39]
	PSK Mode	FSK Mode		
Process (CMOS)	0.18 μm		0.13 μm	0.18 μm
Supply Voltage	1.2 ~ 1.8 V	1.4 ~ 1.8 V	360 ~ 600 mV	0.9 V
Modulation Scheme	O-QPSK	G/FSK	FSK	FSK
Operation Frequency	355 ~ 440 MHz		2 ~ 2.4 GHz	900 MHz
Max. Data Rate	17.5 Mbps	6 Mbps	0.5 Mbps	1 Mbps
P_{OUT}	-15 ~ -8 dBm	-15 ~ -8 dBm	-9 ~ -2 dBm	-4 dBm
Power Consumption	3.5 mW	8.8 mW	1.3 mW	1.8 mW
Energy/bit	**0.2 nJ/bit**	1.5 nJ/bit	2.6 nJ/bit	1.7 nJ/bit

Table 5-2 compares the performance of the proposed O-QPSK transmitter with other related works. The proposed O-QPSK transmitter achieves a high data rate with very low power consumption, resulting in good energy/bit performance.

Fig. 6-13 compares this work (PSK mode) with other low-power transmitters. Although impulse Ultra-Wide-Band (UWB) transmitters [3] can achieve energy-per-bit performance better than 100 pJ/bit, narrow-band modulation transmitters are more favored for the targeted implantable application because of simpler demodulator design and better channel characteristics in an implanted environment.

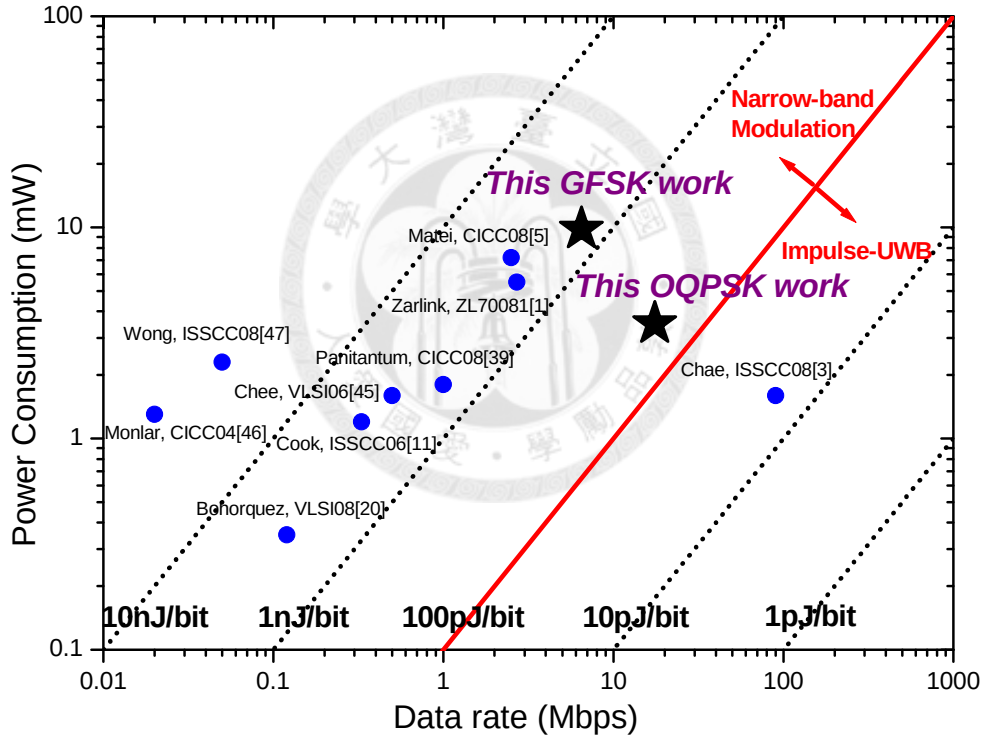


Fig. 6-13: Energy efficiency comparison of low-power transmitters

6.6 Conclusion

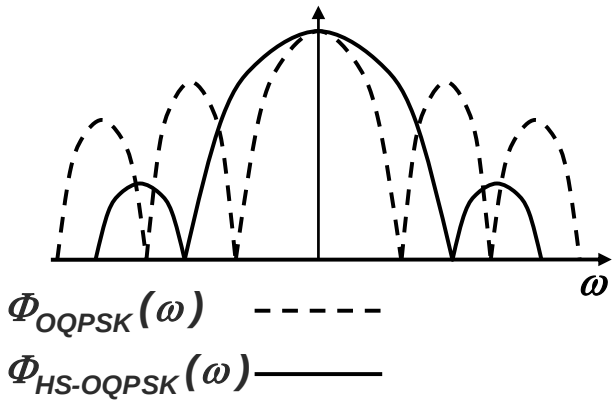
In this chapter, a 400-MHz low-power Phase-MUX-based transmitter has been demonstrated to support O-QPSK modulation with a wide data rate range. The proposed Phase MUX efficiently implements the direct phase-shift keying operation. This

architecture is insensitive to many analog non-idealities due to its semi-digital design approach. The high data rate transmitter with low-power consumption is suitable for wideband implantable medical applications.

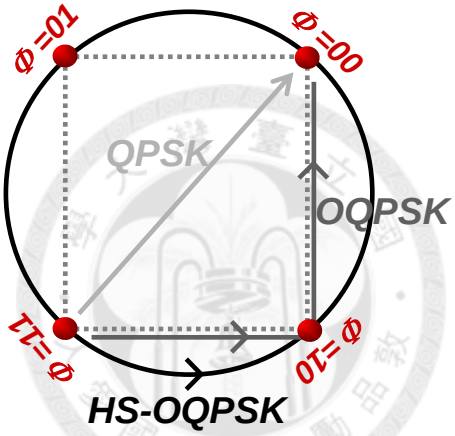
Chapter 7
An FIR-embedded MUX-based Transmitter for Half-sine Shaping O-QPSK Modulation

7.1 Introduction

In this chapter, a semi-digital filtering technique is adopted to improve the spectral efficiency of the MUX-based transmitter. As presented in chapter 6, the offset QPSK (OQPSK) modulation is a variant form of the QPSK modulation, which can prevents the signal power from dropping considerably in the presence of finite circuit bandwidth during data transition. However, as illustrated in Fig. 7-1(a), the signal sidelobe energy O-QPSK modulation is only 13 dB lower than signal mainlobe energy, resulting in poor spectral efficiency and large transmission bandwidth. Therefore, the transmission distance is decreased due to higher noise power, which requires higher output power to compensate the signal-to-noise ratio. A baseband filtering technique, usually half-sine shaping, can be applied in O-QPSK modulation (HS-OQPSK) to improve the phase continuity; thus reducing side-lobe energy to 27 dB lower than main-lobe energy. In addition, HS-OQPSK signal allows an efficient nonlinear power amplifier (PA) to be utilized for low-power consumption because of its constant-envelope characteristic, as shown in Fig. 7-1(b). .



(a)



(b)

Fig. 7-1: (a) Power spectrum density of baseband modulation, (b) constellation of the HS-OQPSK modulation

7.2 Proposed HS-OQPSK Transmitter

The proposed transmitter is designed to operate at around 300-MHz band. This transmitter adopts the half-sine shaping Offset-QPSK (HS-OQPSK) modulation scheme for it has a constant-envelope characteristic with high spectral efficiency. Fig. 7-2 shows the architecture of the proposed MUX-based transmitter, phase modulation

signals are created by dynamically selecting one of the quadrature signals according to the baseband data (i.e. *TX DATA*) via the proposed Phase MUX. The half-sine waveform shaping is performed by the FIR filtering which is embedded in the phase MUX. The Digital Modulator implements a compact digital baseband.

Conventional waveform-shaping PSK transmitters are often implemented with analog quadrature mixers and filters, which are sensitive to various analog imperfections. The proposed transmitter is free from the offset-induced LO leakage and is insensitive to PVT variations, since there is no analog offset and trans-conductance dependency in this digital-like circuit architecture. Good quadrature phase accuracy is ensured by well-balanced LC-VCO and divider designs.

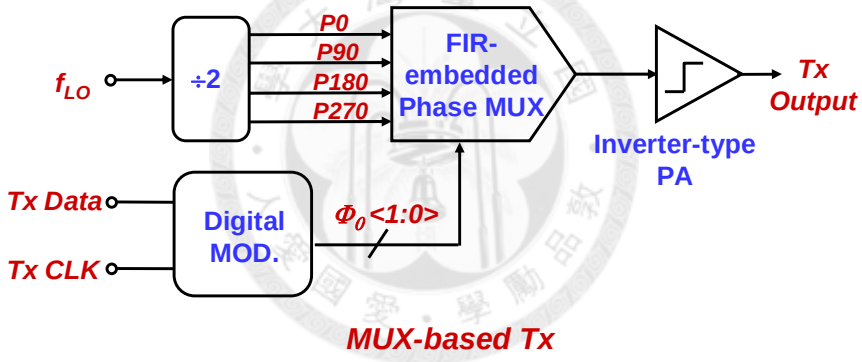


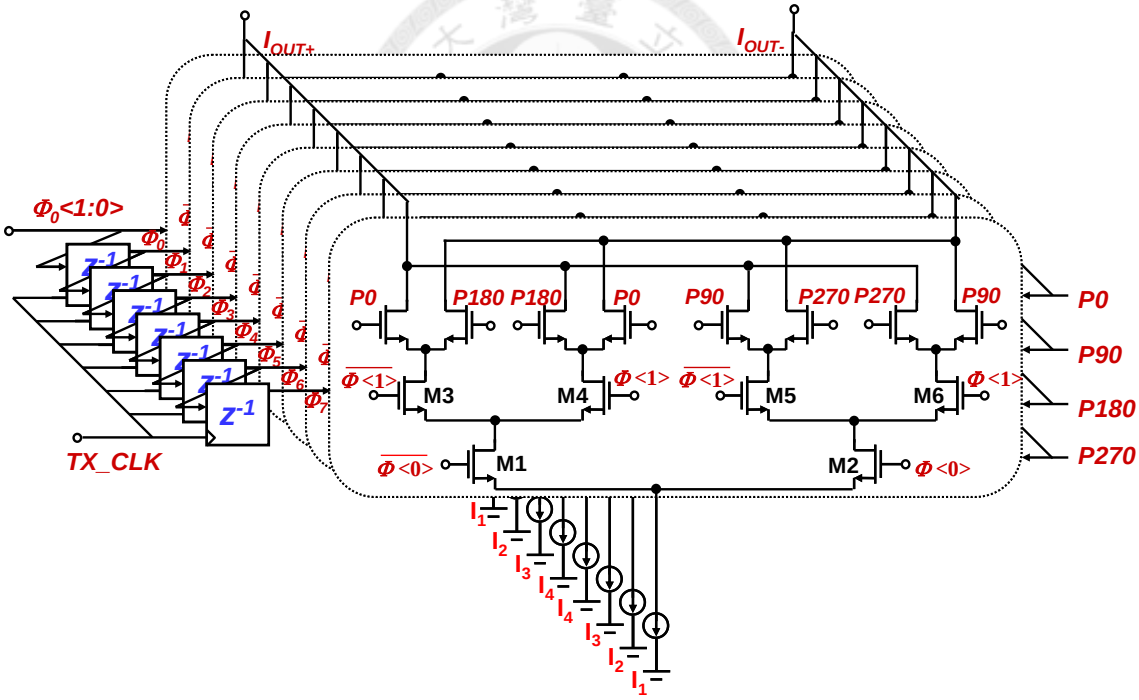
Fig. 7-2: Proposed HS-OQPSK transmitter test-chip block diagram

Fig. 7-3(a) depicts the proposed FIR-embedded phase MUX (FIR-PMUX). The phase-MUX-based transmitter architecture proofs to be energy efficient in transmitting PSK signals [42], since many analog components, e.g. DACs, filters, quadrature mixers, are eliminated. To generate HS-OQPSK modulation signals, the waveform shaping operation is accomplished by incorporating the FIR-filtering into the phase MUX.

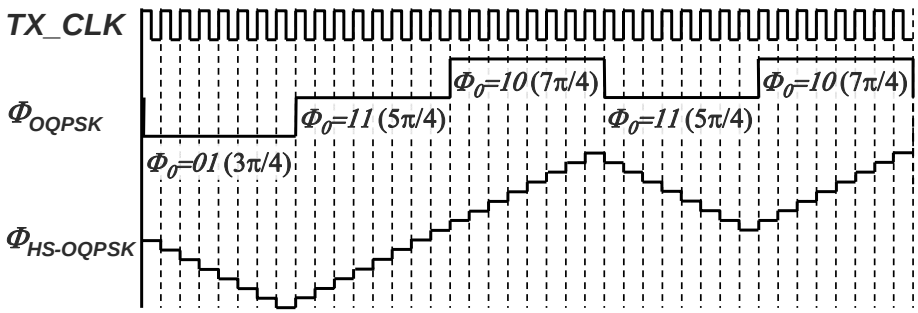
In Fig. 7-3(a), the overall phase MUX is comprised of 8 unit cells. The output of each cell is selected from one of the 4 input phases (*P0~P270*) according to the 2-bit control signal Φ<1:0>. The transmitter data Φ_0<1:0> propagates through the shift

registers with a delay (z^{-1}) equal to 1/8 of the transmitter data period; thus, generating Φ_1<1:0> to Φ_7<1:0> to be the control signal for each cell. By summing the output of all unit cells, the entire circuit operates as an 8-tap FIR filter. The FIR coefficients are set by the bias currents, I_1~I_4.

A rectangular-FIR filter is demonstrated in this design, where all cells are biased at 35 μA. Fig. 7-3(b) illustrates the operation of this FIR-PMUX. Φ_0 is the 2-bit data generated by the Digital Modulator, and Φ_{FIR} represents the equivalent baseband phase after FIR filtering operation. This rectangular-FIR filter approximates the *Sinc* filtering in the phase domain, which is equivalent to half-sine waveform shaping in the time domain.



(a)



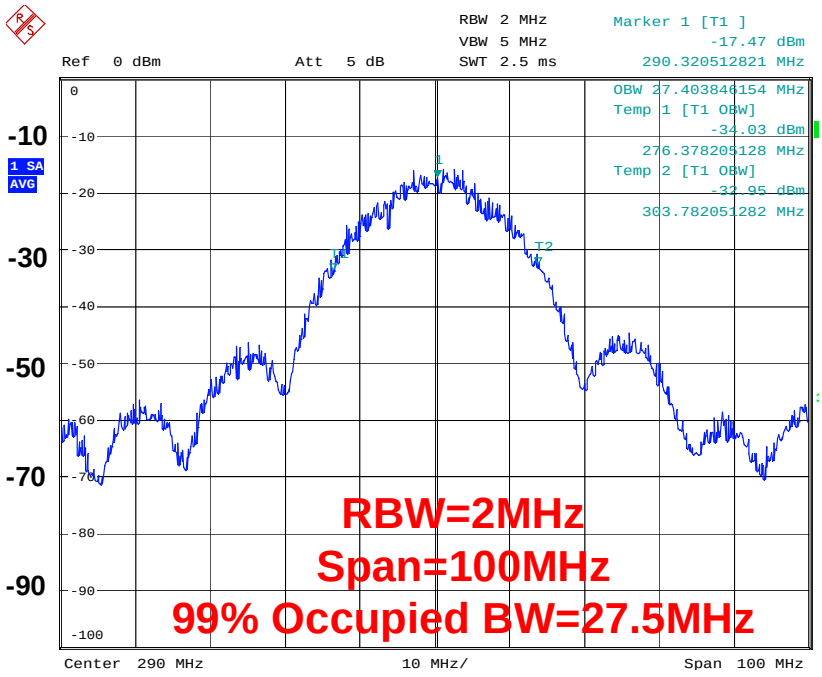
(b)

Fig. 7-3: (a) Simplified schematic of the proposed FIR-PMUX, (b) illustration of the operation principle of the proposed FIR-PMUX (TX_CLK is 8 times of the data rate)

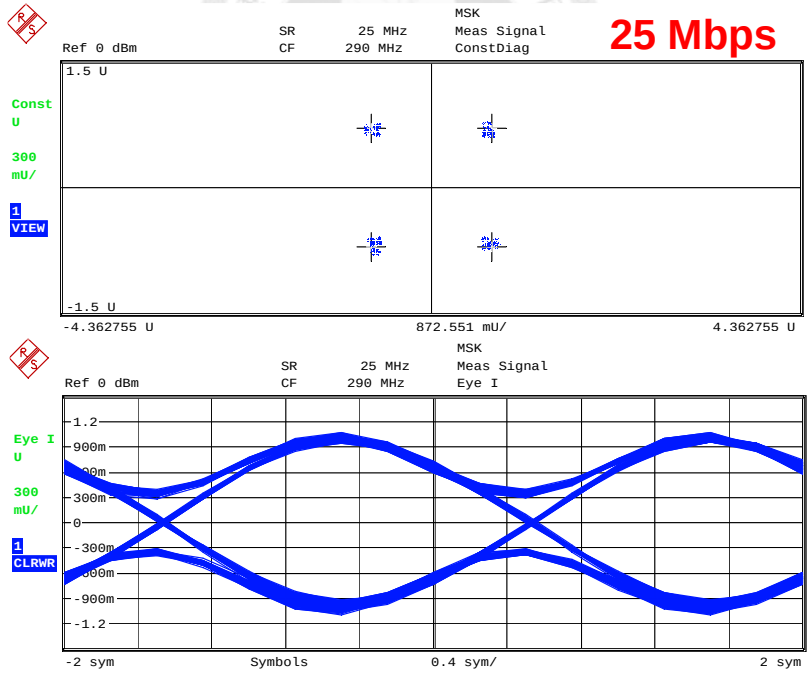
7.3 Experimental Results and Conclusion

This transmitter test chip was fabricated in the tsmc 0.18-μm CMOS process, and it occupies an area of 0.14 mm^2. The operation frequency of this transmitter is around 300 MHz.

Fig. 7-4(a) and 7-4(b) shows the measured transmitter output spectrum and the modulation accuracy at a data rate of 25 Mbps. The modulation signal achieves an EVM of 8%, which is equivalent to 22-dB SNR. Such transmitter signal quality is more than adequate for typical HS-OQPSK demodulators to satisfy BER < 10^{-4}. Moreover, this transmitter achieves 46-dB LO-leakage suppression and 0.06-dB quadrature gain accuracy, owing to the proposed FIR-PMUX architecture. The output spectrum shows that 99% of the total power of the 25-Mbps HS-OQPSK signal is confined in a 27.5-MHz bandwidth. Fig. 7-5 present the overall HS-OQPSK modulation quality (in EVM) versus the transmission data rate. The transmitter test chip dissipates 1.2 mA from a 1.2-V supply. The PA is capable of delivering an output power up to -7dBm.



(a)



I eye diagram: 0.4 sym/div

FILT
Ref 0 dBm
SR 25 MHz
CF 290 MHz
Sym&Mod Acc
1
CLRWR
Att
25 dB

MODULATION ACCURACY				
	Result	Peak	atSym	Unit
EVM	8.001	16.666	466	%
Magnitude Err	5.307	16.603	466	%
Phase Error	4.64	-12.50	303	deg
CarrierFreq Err	-42.90			Hz
Ampt Droop	-0.03			dB
Origin Offset	-44.50			dB
Gain Imbalance	0.01			dB
Quadrature Err	-0.59			deg
RHO	0.995291			
Mean Power	-8.59	-7.45	116	dBm
SNR (MER)	21.94			dB

SYMBOL TABLE (Hexadecimal)	
00000	1 1 0 0 1 0 0 0 1 0 1 0 0 0 1 0 0 0
00018	0 0 1 1 1 0 1 0 0 0 0 0 1 1 1 1 0 1
00036	1 0 1 0 0 1 1 0 1 0 0 1 0 1 0 1 1 1
00054	1 0 0 1 0 1 0 1 1 1 1 1 0 0 0 1 1 0
00072	1 1 1 0 0 1 0 0 1 1 0 0 0 0 0 1 0 0
00090	1 1 0 0 0 0 0 0 1 0 1 1 1 0 0 0 0 1
00108	0 0 1 0 0 0 1 0 1 0 1 1 0 1 1 1 0 1
00126	0 1 0 1 1 0 0 0 0 1 0 1 0 0 1 0 0 1
00144	0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 0 1 1
00162	1 0 1 0 1 1 0 0 1 0 0 1 0 0 1 1 1 0
00180	1 1 1 1 0 1 0 1 1 1 0 1 1 1 1 0 0 1
00198	1 1 0 1 1 0 1 1 0 1 1 1 1 0 0 0 0 0
00216	1 1 0 0 0 0 1 1 1 1 1 0 1 1 1 1 0 0

(b)

Fig. 7-4: Measured (a) TX output spectrum, (b) Eye diagram and constellation and modulation quality

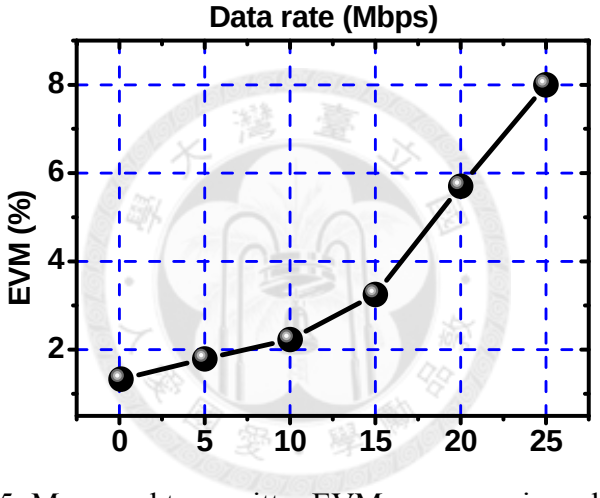


Fig. 7-5: Measured transmitter EVM versus various data rate

The chip photo is shown in Fig. 7-6. Table 7-1 summarizes the measured chip performance and compares with other similar short-range low-power RF transceiver designs.

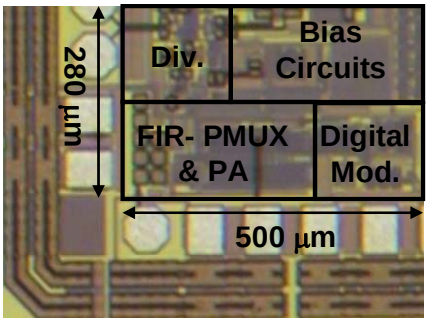


Fig. 7-6: Chip photo

Table 7-1: Performance Summary of HS-OQPSK Transmitter

CMOS Process	0.18 μm
Supply Voltage	1.2~1.8 V
Modulations	HS-OQPSK
Operation Freq.	300 MHz
Max. Data Rate	25 Mbps
Max. P_{OUT}	-7 dBm
Power Consumption	1.4 mW
Core Area	0.14 mm^2

7.4 Conclusion

A 300-MHz low-power transmitter with FIR-embedded Phase MUX has been demonstrated to support HS-OQPSK modulation with a good energy and spectral efficiency. The proposed FIR-embedded Phase MUX implements a semi-digital filter in phase domain, effectively half-sine shaping the digital baseband signal in time domain. This architecture is insensitive to many analog non-idealities due to its semi-digital design approach.

Chapter 8
Conclusion

This dissertation presents a wireless transceiver circuits designed for implantable medical applications requiring wideband transmission, such as multi-channel neural recording system or wireless capsule endoscope system. These applications need high-data-rate transmitters as well as fast start-up receivers. In addition, these transceivers must consume very low power due to limited energy source in the implanted environment.

In order to achieve optimized performance, the proposed transceiver is asymmetrical between uplink and downlink. Downlink reception uses low-data-rate ASK modulation; whereas uplink transmission adopts high-data-rate FSK or PSK modulation. The transceiver is designed to operate at the 400-MHz band and is able to compliant with Medical Implant Communications Serve (MICS) band.

A super-regenerative receiver is implemented as downlink ASK receiver. In order to achieve fine pulse-width digitization for super-regenerative receiver, this dissertation proposed a Delta-Sigma Pulse-Width Digitizer architecture. It is basically a pulse-width domain ΔΣ modulator, which can suppress the quantization noise by 22 dB, achieving 1% BER at -78-dBm ASK input level.

On the other hand, an uplink transmitter with ΣΔ-PR is proposed for wideband FSK/PSK dual-mode operation. In G/FSK mode, the ΣΔ-PR generates wideband FSK modulation signal without being constrained by PLL bandwidth, while achieving stable

carrier frequency since PLL is remained locked. ΔΣ-dithering between two frequencies can push the quantization phase noise to higher offset frequency; thus resulting in -100-dBm/Hz in-band phase noise. In O-QPSK mode, the transmitter is highly simplified by directly selecting one of the quandrature phases using Phase-MUX circuit. This Phase-MUX circuit with inverter-type PA in O-QPSK mode leads to excellent energy/bit efficiency.

Moreover, a FIR digital filter can be embedded into the proposed Phase MUX circuit to reduce the transmission bandwidth and also noise power, which can further reduce power consumption since lower transmission power is required to achieve same SNR.

In conclusion, the power consumption of RF transceiver circuits in implantable medical application is stringent, which requires non-conventional architecture to reduce power consumption. One of the most effective ways is to simplify the RF/ analog circuit, while enhancing the overall performances with the assistance of the digital circuits. In this work, delta-sigma noise shaping technique is used to facilatate a simple, coarse but low-power RF/analog circuit achieving better performance. Meanwhile, the digital-intensive implementation of the proposed architecture enables the RF circuits to be less sensitive to analog non-idealities and PVT variations, and may lead to a more energy-efficient operation in advanced deep sub-micron CMOS processes.

References

[1] Zarlink Semiconductor, "RF Integrated Circuits for Medical Applications: ZL70081," http://www.zarlink.com

[2] R. Harrison, P. Watkins, R. Jier, R. Lovejoy, D. Black, R. Normann, F. Solzbacher, "A Low-Power Integrated Circuit for A Wireless 100-electrode Neural Recording System," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers,* pp. 454-455, Feb. 2006.

[3] M. Chae, W. Liu, Z. Yang, T. Chen, J. Kim, M. Sivaprakasan, M. Yuce, "A 128-channel 6mW Wireless Neural Recording IC With On-the-fly Spike Sorting and UWB Transmitter," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers,* pp. 146-603, Feb. 2008.

[4] J. Aziz, R. Genov, M. Derchansky, B. Bardakjian, and P. Carlen, "256-Channel Neural Recording Microsystem with On-chip 3D Electrodes," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers,* pp. 160-161, Feb. 2007.

[5] E. Matei**,** E. Lee, J. Gord, P. Nercessian, P. Hess, H. Stover, T. Li, J. Wolfe, "A Biomedical Implantable FES Battery-powered Micro-stimulator," in *Proc. IEEE Custom Integrated Circuits Conference*, pp. 317-324, Sep. 2008.

[6] J. Ryckaert, P. D. Doncker, R. Meys, A. L. Hoye, S. Donnay, "Channel Model for Wireless Communication Around Human Body", *IEE Electronics Letters*, vol. 40, pp. 543-544, Apr. 2004.

[7] T. Akin, K. Najafi, R.M. Bradley, "A Wireless Implantable Multichannel Digital Neural Recording System for A Micromachined Sieve Electrode," *IEEE J.*

Solid-State Circuits, vol. 33, pp. 109-118, Jan. 1998.

[8] FCC Rules and Regulations, "MICS Band Plan," Part 95, Jan. 2003.

[9] L. E. Larson, RF and Microwave *Circuit Design for Wireless Communication*. Boston: Artech House, 1996.

[10] M. H. Perrott, T. L. Tewksbury III, and C. G. Sodini, "A 27-mW CMOS Fractional-*N* Synthesizer Using Digital Compensation for 2.5-Mb/s GFSK Modulation," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2048-2060, Dec. 1997.

[11] B. W. Cook, A. D. Berny, A. Molnar, S. Lanzisera, and K. S. J. Pister, "An Ultra-Low Power 2.4GHz RF Transceiver for Wireless Sensor Network in 0.13μm CMOS with 400mV Supply and Integrated Passive RX Front-End," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 370-371, Feb. 2006.

[12] C. Cojocaru, T. Pamir, F. Balteanu, A. Namdar, D. Payer, I. Gheorghe, T. Lipan, K. Sheikh, J. Pingot, H. Paananen, M. Littow, M. Cloutier, E. Macrobbie, "A 43mW Bluetooth Transceiver with -91dBm Sensitivity" in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 90-91, Feb. 2003.

[13] B. Sklar, *Digital Communications*. Upper Saddle River, N.J.: Prentice Hall, 2001.

[14] T. Kimura, H. Yano, Y. Aoki, N. Yoshida, J. Noda, T. Sukenari, Y. Konishi, T. Nakao, A. Mitsuhasi, D. Taguchi, "A Wireless Dual-Link System for Sensor Network Applications," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 534-535, Feb. 2008.

[15] D. C. Daly, P. P. Mercier, M. Bhardwaj, A. L. Stone, J. Voldman, R. B. Levine, J. G. Hildebrand, A. P. Chandrakasan, "A Pulsed UWB Receiver SoC for Insect Motion Control," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 200-201, Feb. 2009.

[16] E. H. Armstrong, "Some Recent Development of Regenerative Circuits," *Pro. IRE,*

vol. 10, pp. 244-260, Aug. 1922.

[17] A. Vouilloz, M. Declercq, and C. Dehollain, "A Low-power CMOS Super-regenerative Receiver at 1 GHz," *IEEE J. Solid-State Circuits*, vol. 36, pp. 440-451, March 2001.

[18] B. Otis, Y. H. Chee, J. Rabaey, "A 400μW-RX, 1.6mW-TX Super-Regenrative Transceiver for Wireless Sensor Networks," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 396-397, Feb. 2005.

[19] J.–Y. Chen, M. Flynn, J. P. Hayes, "A Fully Integrated Auto-Calibrated Super-Regenerative Receiver," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 376-377, Feb. 2006.

[20] J. L. Bohorquez, J. L. Dawson, A. P. Chandrakasan, "A 350μW CMOS MSK Transmitter and 400μW OOK Super-Regenerative Receiver for Medical Implant Communications," in *Proc. Symp. VLSI Circuits,* pp. 32-33, Jun., 2008.

[21] D. Shi, N. Behdad, J.-Y. Chen, M. P. Flynn, "A 5GHz Fully Integrated Super-Regenerative Receiver with On-Chip Slot Antenna in 0.13μm CMOS," in *Proc. Symp. VLSI Circuits,* pp. 34-35, Jun., 2008.

[22] Y.-H. Liu, H.-H. Liu, and T.-H. Lin, "A Super-Regenerative ASK Receiver with ΔΣ Pulse-width Digitizer and SAR-based Fast Frequency Calibration for MICS Applications," in *Proc. Symp. VLSI Circuits,* pp. 38-39, Jun., 2009.

[23] F. Colodro, A. Torralba, and M. Languna, "Continuous-Time Sigma-Delta Modulator with an Embedded Pulsewidth Modulation," *IEEE Tran. Circuits Syst. I,* vol. 55, pp. 775-785, Apr. 2008.

[24] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Chichester: Wiley, 2005.

[25] V. Dhanasekaran, M. Gambhir, M. M. Elsayed, E. Sanchez-Sinencio, J.

Silva-Martinez, C. Mishra, L. Chen, E. Pankratz, "A 20MHz BW 68dB DR CT ΔΣ ADC Based on a Multi-Bit Time-Domain Quantizer and Feedback Element," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 174-175, Feb. 2009.

[26] R. B. Staszewski, C.-M. Hung, K. Maggio, J. Wallberg, D. Leipold, P. T. Balsara, "All-Digital Phase-Domain TX Frequency Synthesizer for Bluetooth Radios in 0.13μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 275-276, Feb. 2004.

[27] M. H. Perrott, M. D. Trott, and C. G. Sodini, "A Modeling Approach for Σ–Δ Fractional-*N* Frequency Synthesizers Allowing Straightforward Noise Analysis," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1028-1038, Aug. 2002.

[28] E. Zwan, E. Dijkmans and J. Huijsing, "A 0.2 mW ΣΔ Modulator for Speech Coding with 80 dB Dynamic Range," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1873-1880, Dec. 1996.

[29] R. G. Meyer, "Low-power Monolithic RF Peak Detector Analysis," *IEEE J. Solid-State Circuits*, vol. 30, pp. 65-67, Jan. 1995.

[30] F. M. Gardner, "Interpolation in Digital Modem - Part I: Fundamental," *IEEE Tran. On Communications*, vol. 41, pp. 501-507, Mar. 1993.

[31] P. Chen, C.-C. Chen, C.-C. Tsai, W.-F. Lu, "A Time-to-Digital-Converter-Based CMOS Smart Temperature Sensor," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1642-1648, Aug. 2005.

[32] J. Craninckx and M. S. J. Steyaert, "A 1.75-GHz/3-V Dual-Modulus Divided-by-128/129 Prescaler in 0.7-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, pp. 890-897, July, 1996.

[33] C.-H. Heng and B.-S. Song, "A 1.8-GHz CMOS Fractional-N Frequency Synthesizer with Randomized Multiphase VCO," *IEEE J. Solid-State Circuits*, vol.

38, pp. 848-854, Jun., 2003.

[34] C.-H. Park, I. Kim, and B. Kim, "A 1.8-GHz Self-Calibrated Phase-Locked Loop with Precise I/Q Matching," *IEEE J. Solid-State Circuits*, vol. 31, pp. 777-783, May, 2001.

[35] A. M. Fahim and M. I. Elmasry, "A Wideband Sigma-Delta Phase-Locked Loop Modulator for Wireless Applications," *IEEE Tran. Circuits Syst. II,* vol. 55, pp. 775-785, Apr. 2008.

[36] W. P. Robins, *Phase Noise in Signal Sources*. London: Peter Peregrinus, 1982.

[37] R. B. Staszewski, C.-M. Hung, N. Barton, M.-C. Lee, and D. Leipold, "A Digitally Controlled Oscillator in a 90 nm Digital CMOS Process for Mobile Phones," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2203-2211, Nov. 2005.

[38] S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with VHDL Design*. Boston: McGraw-Hill, 2000.

[39] N. Panitantum, K. Mayaram, and T. S. Fiez, "A 900-MHz Low-Power Transmitter With Fast Frequency Calibration for Wireless Sensor Networks," in *Proc. IEEE Custom Integrated Circuits Conference,* pp. 595-598, Sep. 2008.

[40] A. Jerng and C. G. Sodini, "A Wideband ΔΣ Digital-RF Modulator for High Data Rate Transmitters," *IEEE J. Solid-State Circuits*, vol. 42, pp. 1710-1722, Aug. 2007.

[41] "HP 89440A/HP 89441A Operator's Guide", Hewlett-Packard Company, Palo Alto, CA, 1996.

[42] Y.-H. Liu and T.-H. Lin, "A 3.5-mW 15-Mbps O-QPSK transmitter for real-time wireless medical imaging applications," in *Proc. IEEE Custom Integrated Circuits Conference*, pp. 599-602, Sep. 2008.

[43] B. D. Muer, M. S. J. Steyaert, *CMOS Fractional-N Synthesizers*. Boston: Kluwer

Academic, 2003.

[44] Q. Gu, RF *System Design of Transceiver for Wireless Communications*. New York: Springer, 2005.

[45] Y. H. Chee, A. M. Niknejad, and J. Rabaey, "A 46% Efficient 0.8dBm Transmitter for Wireless Sensor Networks," in *Proc. Symp. VLSI Circuits,* pp. 43-44, Jun., 2006.

[46] A. Molnar, B. Lu, S. Lanzisera, B. W. Cook, and K. S. J. Pister, "An Ultra-low Power 900 MHz RF Transceiver for Wireless Sensor Networks," in *Proc. IEEE Custom Integrated Circuits Conference*, pp. 401-404, Sep. 2004.

[47] A. C.-W. Wong, D. McDonagh, G. Kathiresan, O. C. Omeni, O. El-Jamaly, T. C.-k. Chan, P. Paddan, A. J. Burdett, "A 1V, Micropower System-on-chip for Vital-sign Monitoring in Wireless Body Sensor Networks," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers,* pp. 138-139, Feb. 2008.

Publication List

International Journal

[1] **Y.-H. Liu**, Cheng-Lung Li, and T.-H. Lin, "A 200-pJ/b Wireless MUX-based RF Transmitter for Implantable Multi-Channel Neural Recording," *IEEE Trans. Microwave Theory Tech.*, OCT., 2009.

[2] **Y.-H. Liu** and T.-H. Lin, "A Wideband PLL-based G/FSK Transmitter in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, SEP.,2009.

[3] T.-H. Lin, C.-L. Ti and **Y.-H. Liu**, "Dynamic Current Matching Charge Pump and Gated-Offset Linearization Techniques for Delta-Sigma Fractional-N PLLs," *IEEE Tran. Circuits Syst. I*, vol. 56, pp. 877-885, MAY, 2009.

International Conference

[4] **Y.-H. Liu**, H.-H. Liu and T.-H. Lin, "A Super-regenerative ASK Receiver with ΔΣ Pulse-width Digitizer and SAR-based Fast Frequency Calibration for MICS Applications," in *Proc. Symp. VLSI Circuits*, pp. 38-39, Jun., 2009.

[5] **Y.-H. Liu** and T.-H. Lin, "A 3.5-mW 15-Mbps O-QPSK Transmitter for Real-time Wireless Medical Imaging Applications," in *Proc. IEEE Custom Integrated Circuits Conference*, pp. 599-602, Sep. 2008.

[6] C. -L. Ti, **Y.-H. Liu**, and T.-H. Lin, "A 2.4-GHz Fractional-N PLL with a PFD/CP Linearization and an Improved CP Circuit," *IEEE Int. Symp. Circuits Syst.*, pp. 1728-1731, May. 2008.

[7] **Y.-H. Liu** and T.-H. Lin, "An Energy-Efficient 1.5Mbps Wireless FSK Transmitter with A ΣΔ-Modulated Phase Rotator," *in Proc. ESSCIRC*, pp. 488-491, Sep. 2007.

[8] **Y.-H. Liu**, C.-J. Tung, and T.-H. Lin, "A Low-Power Asymmetrical MICS Wireless Interface and Transceiver Design for Medical Imaging," in *Proc. IEEE BioCAS*, pp. 162-165, Nov. 2006.

Local Conference

[9] C.-J. Tung, **Y.-H. Liu**, H.-H. Liu and T.-H. Lin, "A 400-MHz Super-Regenerative Receiver with Digital Calibration for Capsule Endoscope Systems in 0.18-μm CMOS," in *Proc. IEEE VLSI-DAT*, Apr. 2008.

Appendix A
Chip Description

A.1 MUX-Based Dual-Mode Transmitter

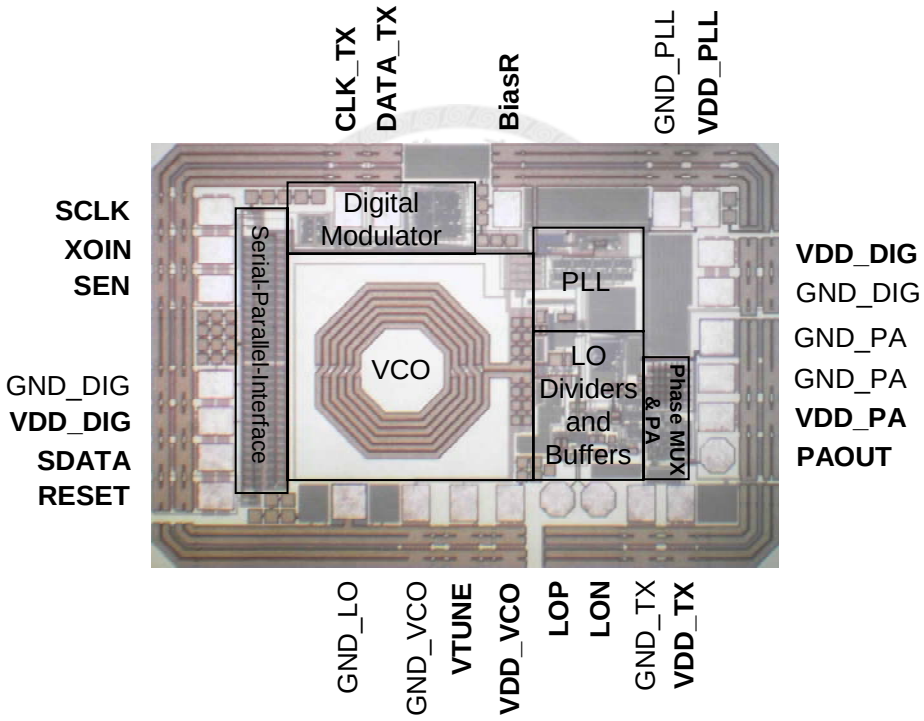


Fig. A-1: Pin description of MUX-based dual-mode transmitter

The MUX-based dual-mode transmitter supports G/FSK and O-QPSK modulations. This operation frequency range is from 355 to 435 MHz. This transceiver is operated at supply voltage from 1.4 V to 1.8V. The highest G/FSK transmitter data rate is 6 Mbps; whereas O-QPSK mode is 17.5 Mbps. This transmitter can be programmed by a 64-bit Serial-Parallel-Interface (SPI). The frequency synthesizer (including VCO and loop

filter) is fully integrated and only requires a external 19.2 MHz TCXO. The transmitter bias can be adjusted by changing the external resistor thought the Pin 24 (BiasR).

Table A-1: Pin description of MUX-based dual-mode transmitter

Pin	I/O	Name	Pin description
1	I	SCLK	SIPO clock
2	I	XOIN	TCXO input
3	I	SEN	SIPO enable
4		GND_DIG	Digital ground
5		VDD_DIG	Digital supply
6	I	SDATA	SIPO data
7	I	RESET	Digital reset
8		GND_LO	LO ground
9		GND_VCO	VCO ground
10	I/O	VTUNE	Control voltage of VCO
11	I	VDD_VCO	VCO supply
12	I	LOP	External LO input (positive)
13	I	LON	External LO input (negative)
14		GND_TX	TX ground
15	I	VDD_TX	TX supply
16	O	PAOUT	PA output
17	I	VDD_PA	PA supply
18		GND_PA	PA ground
19		GND_PA	PA ground
20		GND_DIG	Digital ground
21	I	VDD_DIG	Digital supply
22	I	VDD_PLL	PLL(analog part) supply
23		GND_PLL	PLL ground
24	I	BiasR	External bias resistor
25	I	DATA_TX	TX data input
26	I	CLK_TX	TX clock input

A.2 Asymmetrical Transceiver: ASK Super-Reg. RX and HS-OQPSK TX

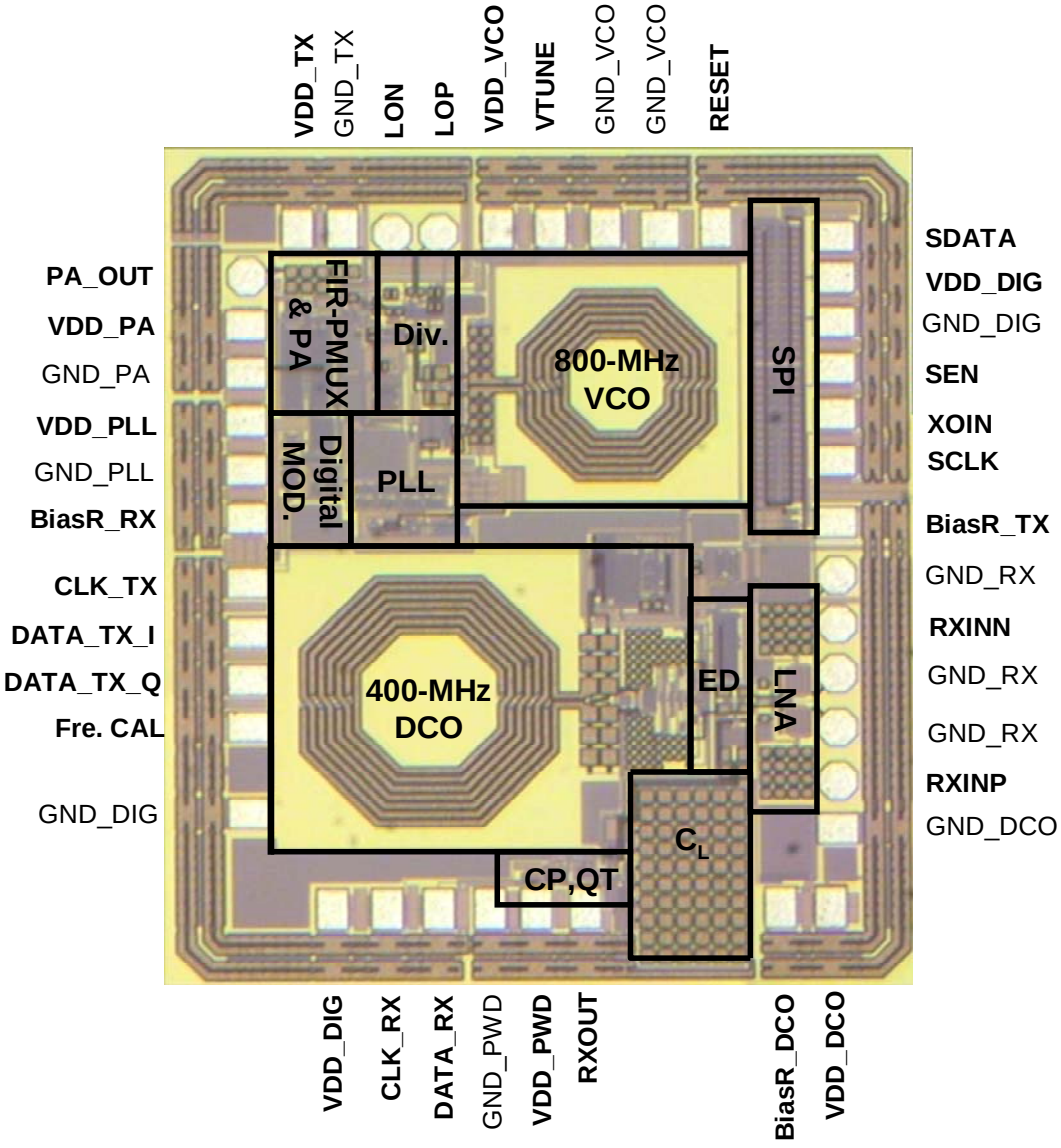


Fig. A-2: Pin description of asymmetrical transceiver

This asymmetrical transceiver designed for implantable medical applications supports low-data-rate ASK modulation for downlink, and high-data-rate HS-OQPSK modulation for uplink. This operation frequency range is from 400 MHz for receiver;

whereas 300 MHz for transmitter. This transceiver is operated at supply voltage from 1.2 V to 1.8V. The highest data rate of receiver is 156-kbps with -78-dBm sensitivity; while the highest data rate of HS-OQPSK transmitter is 25-Mbps. This transceiver can be programmed by a 64-bit Serial-Parallel-Interface (SPI). A automatic digital frequency calibration engine can be used to adjust the center frequency of super-regenerative receiver to MICS band by enabling pin 10 (Fre.CAL). The frequency synthesizer (including VCO and loop filter) is fully integrated and only requires a external 19.2 MHz TCXO. The transceiver bias can be adjusted by changing the external resistor thought the Pin 6, 18, 26.

Table A-2: Pin description of asymmetrical transceiver

Pin	I/O	Name	Pin description
1	O	PAOUT	PA output
2	I	VDD_PA	PA supply
3		GND_PA	PA ground
4	I	VDD_PLL	PLL(analog part) supply
5		GND_PLL	PLL ground
6	I	BiasR_RX	External bias resistor of receiver
7	I	CLK_TX	TX clock input
8	I	DATA_TX_I	TX I data input
9	I	DATA_TX_Q	TX Q data input
10	I	Fre.CAL	Frequency calibration enable
11		GND_DIG	Digital ground
12	I	VDD_DIG	Digital supply
13	I	CLK_RX	RX clock input
14	O	DATA_RX	RX data output
15		GND_PWD	ΔΣ-PWD ground
16	I	VDD_PWD	ΔΣ-PWD supply
17	O	RX_OUT	RX analog output
18	I	BiasR_DCO	External bias resistor of DCO
19	I	VDD_DCO	DCO supply

20		GND_DCO	DCO supply
21	I	RXINP	RX input (positive)
22		GND_RX	LNA ground
23		GND_RX	LNA ground
24	I	RXINN	RX input (negative)
25		GND_RX	LNA ground
26	I	BiasR_RX	External bias resistor of TX
27	I	SCLK	SIPO clock
28	I	XOIN	TCXO input
29	I	SEN	SIPO enable
30	I	VDD_DIG	Digital supply
31		GND_DIG	Digital ground
32	I	SDATA	SIPO data
33	I	RESET	Digital reset
34		GND_VCO	VCO ground
35		GND_VCO	VCO ground
36	I/O	VTUNE	Control voltage of VCO
37	I	VDD_VCO	VCO supply
38	I	LOP	External LO input (positive)
39	I	LON	External LO input (negative)
40		GND_TX	TX ground
41	I	VDD_TX	TX supply