國立臺灣大學電機資訊學院電子工程學研究所

碩士論文

Graduate Institute of Electronics Engineering
College of Electrical Engineering & Computer Science
National Taiwan University

Master Thesis

用於類比數位轉換器抖動誤差消除之時間數位轉換器

A Time-to-Digital Converter for ADC Jitter Error Cancellation

林晉宇

Chin-Yu Lin

指導教授：李泰成 博士

Advisor：Tai-Cheng Lee, Ph.D.

中華民國 98 年 7 月

July, 2008


國立臺灣大學
教育部獎勵學生愛國愛人

國立臺灣大學碩士學位論文
口試委員會審定書

用於類比數位轉換器抖動誤差消除之時間數位轉換器

A Time-to-Digital Converter for ADC Jitter Error Cancellation

本論文係林晉宇君（R96943007）在國立臺灣大學電子工程學研究所完成之碩士學位論文，於民國九十八年七月二十九日承下列考試委員審查通過及口試及格，特此證明

口試委員：

李泰成

(指導教授)

林宇里　陳信樹

陳巍仁

所長


國立臺灣大學
教育部獎勵學生愛國愛人

A Time-to-Digital Converter for ADC Jitter Error Cancellation

By

Chin-Yu Lin

THESIS

Submitted in partial fulfillment of the requirement
for the degree of Master of Science in Electronics Engineering
at National Taiwan University
Taipei, Taiwan, R.O.C.

July 2009

Approved by：

Advised by：

Approved by Director：


國立臺灣大學
教育部獎勵學生愛國愛人

誌謝

這篇論文就像一個逗點，代表著我將在台大繼續另一階段的人生。首先感謝李泰成老師兩年來的指導，從研究的方向到論文的完成，老師總以最嚴謹的專業態度進行指導，使我在專業知識的追尋與科學研究的心態上，都有著成熟而長足的進步。也誠摯的感謝林宗賢教授、陳信樹教授與陳巍仁教授，他們寶貴的建言使得此篇論文得以順利完成。

兩年的研究所生涯中，感謝家人們一直在背後給予我精神與實質上的支持，使我能順利完成碩士學業。雖然摯愛的爺爺在三月離開了我，不捨的同時卻也更堅定了我繼續深造的意念，未來我必定會兢兢業業地把握每一天，不會令您失望。再來要感謝實驗室的各位，已畢業的 Ph.D 學長大師兄與小耕，你們在專業上的素養以及處事的態度為學弟們樹立了優良的學習典範；尚未畢業的道長更是實驗室的寶，時常放下自己的事熱心為大家解決問題，而你在研究上的成果和對追求知識的熱忱亦令我欽佩不已；還有即將離開的星爺，時常為我在學術及人情世故方面熱心提供意見，看見你在學術研究上的幹勁讓我們這些後輩不禁汗顏。另外，士鈞、兆人、罩哥、汾秋、好厲害、胖胖、政校、科璁、DC 等學長姐的協助，讓我在求學路上不至於感到孤單，也豐富了我的實驗室生涯。感謝同屆的 GBK，蘇承道，硬融，不管是 meeting 前的憂鬱症或是 meeting 後超爽的，都是令我難忘的回憶，接下來的日子還要一起打拼。基羅獎、CCHo、金門、小安安，很高興有你們的加入，為這個實驗室加入新活力與想像力，期待之後能與你們激盪出更多想法，謝謝你們。

最後要感謝我的好友們，謝謝遠在新竹的 Ruka 與幸芸的時常關心；謝謝牧杰與冠文兩個認識近十年死黨，我們從高中一直到台大一路相互扶持的情誼實屬難得，如今你們的人生道路也將往新方向開展，祝福你們。再來感謝我的精神支柱周 Effi 不時的陪伴與開導，讓我在繁忙的研究生活中偶爾也能體會悠閒的感覺；還有謝 Pinky，雖然平時多半是我照顧妳，但還是謝謝妳常常與我聊天解悶。最後感謝惠我良多的淳惠，在我最低潮的時候鼓勵我擺脫陰霾，每每看到妳溫暖和煦如陽光般的笑容，所有煩惱便煙消雲散。

接下來的路或許艱辛，但因為有你們大家的支持，我會義無反顧地走下去。

林晉宇　98.08.18

To My Family

摘要

在現今高速、高精準度的類比數位轉換中，其對取樣時脈抖動之規格要求日益嚴苛，通常需要達到數個微微秒之內，故難以在晶片中產生符合規格之時脈。在這篇論文中，提出了一種適用於消除類比數位轉換器中之抖動誤差的方法。在此種方法中，信號每個取樣點之斜率為一重要的關鍵參數。隨著信號頻率增加，由此演算法所計算出之斜率會開始受到 sinc 函數的影響而導致失真。此時查表法可以用來補償這種效應，使得系統能操作在接近 Nyquist-rate 之頻率。

在所提出的架構中，需要一時間數位轉換器來進行數位化抖動誤差消除的演算法。此外，此時間數位轉換器必須擁有較大的動態範圍與高解析度，如此才能涵蓋峰對峰抖動範圍同時維持準確度。在此論文中，設計了一個 10 微微秒以及 5.12 奈秒動態範圍之基於倍化式延時鎖定迴路(multiplying DLL)局部被動內插(local passive interpolation)之時間數位轉換器。電路製作使用標準 90 奈米互補金氧半導體邏輯製程，所設計的時間數位轉換器在 1 伏特電壓源供應下，功率消耗為 6 毫瓦。此電路的晶片面積為 0.17 毫米平方。

Abstract

The requirement of sampling clock jitter becomes rigorous in the high-speed and high-precision analog-to-digital date conversion, usually around few pico-seconds, which is unreachable for the on-chip clock generation. A method is proposed to cancel the jitter-induced errors in ADC. One of the key parameters needed here is the derivative of each sampled points. The derivative calculated from the algorithm is distorted by a sinc function as the signal frequency gets higher. A look-up table method is applied to compensate the distortion factor which makes the system to operate well near Nyquist rate.

In this architecture, a time-to-digital converter (TDC) is desired to adopt the jitter cancellation algorithm in the digital domain. Besides, this TDC need to be wide dynamic range and high precision in order to cover the peak-to-peak jitter variation while maintain the accuracy. In this thesis, an MDLL-based TDC with local passive interpolation which has 10ps resolution and 5.12ns dynamic range is designed. Fabricated in a 90-nm CMOS technology, the TDC consumes 6.0mW from a 1-V power supply while the active area is only 0.017mm^2.

Table of Contents

Table of Contents **I**

List of Figures **V**

List of Tables **IX**

Chapter 1 Introduction **1**

1.1 Motivation and Research Goals 1

1.2 Thesis Overview 2

Chapter 2 Basic Concepts and Proposed Jitter Error Cancellation Algorithm **5**

2.1 Introduction 5

2.2 Basic Concepts 6

2.2.1 Conventional Jitter Requirement for Nyquist-Rate ADC 6

2.2.2 Generic Autocorrelation Function in the Linear Approximation 6

2.3 Proposed Jitter Error Cancellation Algorithm 8

2.3.1 Jitter Terminology and Measurement 9

2.3.2 Derivative Estimation by Two Points 11

2.3.3 Derivative Estimation by Three Points 12

2.3.4 High Frequency Response Improvement 14

2.4 Summary 16

Chapter 3 Fundamentals of Time-to-Digital Converter 17

3.1 Introduction 17

3.2 TDC Performance Metrics 18

3.2.1 Dynamic Range 18

3.2.2 Conversion Time and Dead Time 18

3.2.3 Single Shot Precision 18

3.2.4 Interpolation Factor 19

3.2.5 Nonlinearity 19

3.3 Architectures of Time-to-Digital Converter 21

3.3.1 Time-to-Voltage-to-Digital Converter 21

3.3.2 Vernier-Based TDC 22

3.3.3 Pulse-Shrinking Cyclic TDC 24

3.3.4 DLL Interpolation TDC 25

3.3.5 Local Passive Interpolation TDC 27

Chapter 4 System Architecture of a MDLL-Based TDC with Local Passive Interpolation 29

4.1 Introduction 29

4.1.1 Multiplying DLL 29

4.1.2 Local Passive Interpolation and Phase Averaging 33

4.2 Architecture of the MDLL-Based TDC with Local Passive Interpolation 36

4.2.1 System Architecture 36

4.2.2 Dynamic Range and Resolution 38

4.3 Summary 41

Chapter 5 Circuit Implementation 43

5.1 Introduction 43

5.2 Architecture 43

5.3 Delay Cell 44

5.4 Phase Frequency Detector 45

5.5 Charge Pump 47

5.6 Divider 48

5.7 Control Logic 49

5.8 Arbiter 50

5.9 Encoder 51

5.10 Output Buffers 52

5.10.1 Digital Output Buffer 52

5.10.2 Open-Drain Output Buffer 53

5.11 Transistor-Level Simulation 53

5.12 Layout and Performance Summary 57

Chapter 6 Test and Experimental Results 59

6.1 Introduction 59

6.2 Chip Die Photo 59

6.3 Test Strategy 60

6.3.1 Test Setup 60

6.3.2 Print Circuit Board Design 61

6.3 Experimental Results 64

Chapter 7 Conclusion 65

7.1 Conclusion 65

Bibliography 67

List of Figures

Chapter 1

Chapter 2

Fig. 2.1 Linear approximation of sampling process. 7

Fig. 2.2 System block diagram of proposed jitter cancellation. 9

Fig. 2.3 Illustrations of absolute jitter and period jitter. 9

Fig. 2.4 Measurement of period jitter. 10

Fig. 2.5 Sampling process in presence of clock jitter. 11

Fig. 2.6 SNR versus input signal frequency normalized to sampling frequency. 12

Fig. 2.7 Concept of average derivative. 13

Fig. 2.8 SNR versus input signal frequency normalized to sampling frequency. 14

Fig. 2.9 SNR versus input signal frequency normalized to sampling frequency. 15

Chapter 3

Fig. 3.1 Transfer function including error sources. (a) Offset error, (b) gain error. 20

Fig. 3.2 Transfer characteristic of TDC showing DNL. 21

Fig. 3.3 Transfer characteristic of TDC showing INL. 21

Fig. 3.4 Time-to-voltage-to-digital converter topology. 22

Fig. 3.5 Vernier-based TDC architecture. 23

Fig. 3.6 System architecture of a pulse-shrinking cyclic TDC. 24

Fig. 3.7 Delay line interpolation. 26

Fig. 3.8 The block diagram of a DLL interpolation TDC. 27

Fig. 3.9 Local passive interpolation TDC architecture. 28

Chapter 4

Fig. 4.1 The architecture and the timing diagram of a multiplying DLL . 30

Fig. 4.2 System model of the MDLL. 31

Fig. 4.3 Elmore delay model. 33

Fig. 4.4 Resistor averaging. 34

Fig. 4.5 A simplified model for analyzing a delay line with a R-string. 35

Fig. 4.6 Space response of R-string. 36

Fig. 4.7 Architecture of the MDLL-based TDC with local passive interpolation. 37

Fig. 4.8 Clock generation diagram. 38

Fig. 4.9 Inverter switching in ring oscillator, showing signal and noise current. 39

Chapter 5

Fig. 5.1 The complete architecture of the MDLL-based TDC. 44

Fig. 5.2 (a) Single ended delay cell (b) Delay cell with cross-couple inverters. 45

Fig. 5.3 Dynamic logic type PFD and its corresponding timing diagram. 46

Fig. 5.4 Transfer curve of a PFD. 46

Fig. 5.5 The Conceptual diagram of a charge pump. 47

Fig. 5.6 Differential charge pump. 48

Fig. 5.7 TSPC divide-by-two circuit. 48

Fig. 5.8 Modified control logic for MDLL. 49

Fig. 5.9 The operation mechanism of the control logic. 49

Fig. 5.10 High-resolution sense-amplifier-based flip-flops. 51

Fig. 5.11 The architecture of digital encoder. 52

Fig. 5.12 (a) The simulated effects about the pad, bonding wire and the probe. 53

(b) The output buffer. 53

Fig. 5.13 The open-drain buffer and the proceeding connection configuration. 53

Fig. 5.14 The transient waveform of reference and output clock before locking. 54

Fig. 5.15 The transient waveform of reference and output clock when locking. 54

Fig. 5.16 The settling behavior of control voltage. 55

Fig. 5.17 The timing diagram of local passive interpolation. 55

Fig. 5.18 The input/output characteristic of TDC. 56

Fig. 5.19 Causes of offset error (a) finite rising and falling time (b) gate delay. 56

Fig. 5.20 Layout of the MDLL-based TDC. 57

Fig. 5.21 The core layout of the MDLL-based TDC. 57

Chapter 6

Fig. 6.1 The die photo of the designed TDC. 60

Fig. 6.2 Test setup and equipments. 61

Fig. 6.3 The photograph of PCB. 62

Fig. 6.4 (a) The pin configurations of the TDC. 62

(b) The description of pin configurations. 63

Fig. 6.5 Output clock spectrum. 64

Chapter 7

List of Tables

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Table 5.1 The performance summary and the comparison table. 58

Chapter 6

Chapter 7

.

Chapter 1

Introduction

1.1 Motivation and Research Goals

Analog-to-digital converters (ADCs) provide the link between the analog world and the digital system. Due to their extensive use of analog and mixed analog-digital operations, ADCs often appear as the bottleneck in data processing applications, limiting the overall speed or precision [1].

In recent years, the demand for high performance ADCs has grown rapidly in modern mixed-signal system. Mobile wireless communication systems are major applications of recent ADCs. In these applications, the specifications of the ADC vary significantly across different receiver architectures. For example, IF-sampling superheteterdyne receivers require high-speed high-resolution ADCs because intermediate frequency (IF) signals are directly converted to digital codes [2]. On the other hand, homodyne receivers which convert RF signals to baseband directly, with more demanding front-end analog processing requirements, can significantly relax the specifications of the baseband ADC. Regardless of the receiver architectures, the high performance ADCs are key components.

Most ADCs use a sample-and-hold (S&H) circuit that essentially takes a snapshot of the ADC input at an instant in time. When the S&H switch is closed, the network at the

input of the ADC is connected to the sample capacitor. At the instant of the switch is opened, one-half clock cycle later, the voltage on the capacitor is recorded and held. Variation in time at which the switch is opened is known as aperture uncertainty, or jitter, and will result in an error voltage that is proportional to the magnitude of the jitter and the input-signal slew rate. In other words, the greater the input frequency and amplitude, the more susceptible ADCs are to jitter on the clock source.

1.2 Thesis Overview

This thesis contains seven chapters. A brief introduction of this thesis is described in Chapter 1. In Chapter 2, the impact of sampling clock jitter on ADC is first shown by building the mathematical relation among speed, aperture jitter, and SNR. Then the terminologies of jitter are reviewed. The proposed jitter error cancellation algorithm and the whole system architecture are also provided in the chapter.

Chapter 3 starts with the performance metrics used in TDC design, including dynamic range, conversion and dead time, noise performance, nonlinearity, and so on. And then the various time-to-digital converter architectures are presented.

Chapter 4 interprets the system design issues of a MDLL-based TDC with local passive interpolation. An introduction of a typical MDLL and passive component interpolation and averaging will first be given. After that, the proposed architecture of a MDLL-based TDC will be introduced. The function of each block will also be described. System design issues and constraints will also be presented in this chapter.

The details of circuit implementation are given in Chapter 5. In Chapter 5, a MDLL-based TDC realized in 90-nm CMOS technology is designed and implemented. The transistor level simulation and the layout will also be presented in the end of this chapter.

Chapter 5 presents the testing strategy and PCB design of the TDC prototype. The testing environment including the measurement instruments is also introduced. Then the experimental results of the prototype are shown.

Finally, conclusions are given in Chapter 7.


國立臺灣大學
學術品德・愛國愛人

Chapter 2

Basic Concepts and Proposed Jitter Error Cancellation Algorithm

---

2.1 Introduction

The demand for high performance analog-to-digital converters (ADCs) has grown rapidly in modern mixed- signal system. The design of the ADCs has drawn significant research in the past decade. However, the availability of low-jitter sampling clock source becomes the bottleneck for the high performance ADCs. The SNDR of state-of-the-art ADCs is limited by aperture uncertainty though the linearity of it meets the resolution specification [3],[2].

This chapter provides the basic concepts about how sampling clock jitter influence the performance of ADCs. Then an algorithm is proposed to cancel the jitter-induced errors in the digital domain for ADCs.

2.2 Basic Concepts

2.2.1 Conventional Jitter Requirement for Nyquist-Rate ADC

To arrive at a simple relation between maximum tolerable jitter and an ADC's speed and resolution, we can say that jitter has negligible effect on the overall SNR if the analog input varies by less than 1LSB during jitter-induced time deviation of the sampling point [1]. Thus, for a full-scale analog input $V_{in}=Asin2\pi ft$, whose maximum rate of change is equal to $2\pi fA$, the above condition can be expressed as

$$2\pi fA\Delta t < 1LSB = \frac{2A}{2^n} \tag{2.1}$$

where Δt represents the clock jitter and n is the converter's resolution. It follows that

$$\Delta t < \frac{1}{\pi f 2^n} \tag{2.2}$$

In Nyquist-rate conversion, f approaches half of the ADC conversion speed. Typically, the requirement of sampling clock jitter is rigorous in the high-precision data conversion, usually lies around several ppms of sampling clock period, which is hardly available for the on-chip clock generation.

2.2.2 Generic Autocorrelation Function in the Linear Approximation

A more precise equation which describes the relation among speed, aperture jitter, and SNR is derived, applicable to a jitter process with generic autocorrelation function and generic input signal in [4]. The sampling process is shown in Fig.2.1. Due to the impact of sampling clock jitter, the ideal sampling instant at kT is shifted to $kT+t_j(kT)$, thus generates an error Δy.

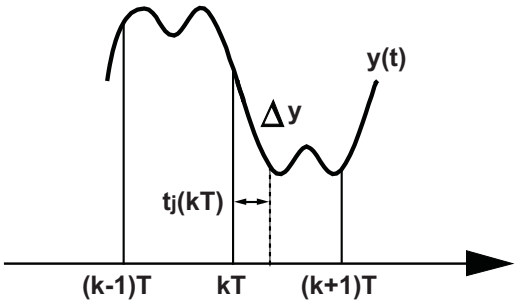


Figure 2.1 Linear approximation of sampling process.

With the linear approximation, the jitter-induced error Δy can be written as

$$\Delta y(kT) = y'(kT) \cdot t_j(kT) \tag{2.3}$$

where the prime denotes the derivative with respect to time and t_j is a time-discrete random process, so that every sampling instant has its own $t_j(kT)$. Therefore, the autocorrelation function of the jitter error is

$$r_{\Delta y}(mT) = -r_y''(mT) \cdot r_{tj}(mT). \tag{2.4}$$

Knowing that the power is the value of the autocorrelation at zero

$$SNR = 10\log\left(\frac{r_y(0)}{-r_y''(0) \cdot r_{tj}(0)}\right) dB. \tag{2.5}$$

With this expression, the jitter requirement can be evaluated for any signal as long as the power spectrum density is available. As application of the relationship (2.5), the SNR in case of sinusoidal input is calculated, and it is easy to find the well-known formula [5] for the aperture jitter SNR in sampling of sinusoidal signal.

$$SNR = 20\log\left(\frac{1}{2\pi f_{sig}\sigma_{tj}}\right) dB. \tag{2.6}$$

The upper bound of jitter requirement for a Nyquist-rate ADC can be found at the zero-crossing point where the quantization noise is equal to the jitter-induced noise, listed

in (2.7).

$$\left(2\pi f_{sig}\sigma_{tj}\right)^2 = \left(3\cdot 2^{2n-1}\right)^{-1}. \tag{2.7}$$

By solving (2.7), the jitter requirement for a Nyquist-rate ADC is

$$t_{rms} < \sqrt{\frac{2}{3}}\frac{1}{\pi\cdot 2^n}\frac{1}{f_s}. \tag{2.8}$$

As for the rectangular power spectrum that has the cutoff frequency *fc*, the result is

$$SNR = 20\log\left(\frac{\sqrt{3}}{2\pi f_c\sigma_{tj}}\right)dB. \tag{2.9}$$

Here comes an observation that a wideband signal has lower jitter requirement in comparison with a single-tone signal, assume the cutoff frequency is equal to that of sinusoidal input. Intuitively, that is because the other low-frequency components have "looser" jitter requirement, so that the "tighter" one is averaged. Therefore, the effective jitter requirement is relaxed.

2.3 Proposed Jitter Error Cancellation Algorithm

From the above, the linear approximation of the sampling process provides the jitter-induced error by multiplying jitter by its derivative. The error quantities can be eliminated if the jitter is measured and the derivative is estimated well. Owning to high density and low energy of digital circuits, analog blocks can be migrated to digital domain. In this work, a jitter error cancellation technique in digital domain is proposed, illustrated in Fig.2.2. The jitter cancellation are pushed to digital processing blocks except for the time-to-digital converter (TDC) which serves as an interface between analog and digital system. It is worth mentioning that this TDC need to be wide dynamic range as well as high precision in order to cover the peak-to-peak jitter variation while maintain the

accuracy.

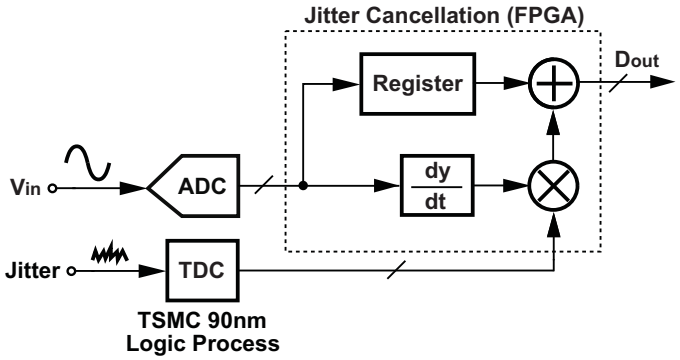


Figure 2.2 System block diagram of proposed jitter cancellation.

A 12-bit and 20MHz ADC will be a testing vehicle in this work; meanwhile, a 1% RMS jitter for a typical on-chip clock generation is assumed. Such clock generator degrades the ENOB of this ADC to 5 bits at Nyquist-rate conversion. Under these conditions, a 10-ps resolution TDC with larger than 5-ns dynamic range is required based on behavioral simulations.

2.3.1 Jitter Terminology and Measurement

The two most important and commonly used definitions, period jitter and absolute jitter, are shown in Fig.2.3 [6].

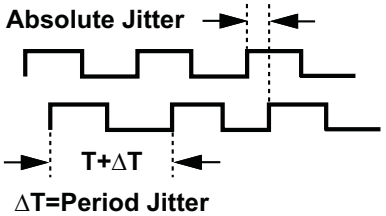


Figure 2.3 Illustrations of absolute jitter and period jitter.

The period jitter, edge-to-edge jitter, cycle jitter, and sometimes cycle-to-cycle jitter is the variation between one rising edge to the next with respect to the period of the oscillation, which is the main consideration in sampling application. Note that the term cycle-to-cycle jitter sometimes may be confusing because is also used to describe the jitter that represents the difference between two adjacent periods [7].

In the proposed architecture which deal with the sampling process jitter, the variation between two adjacent rising edges is concerned, namely, the period jitter should be monitored. Fig.2.4 shows the mechanism to measure the period jitter. The solid line is the perfect clock source and the dashed line represents the exact rising edge in the presence of jitter. By passing the clock through a low-noise delay cell, the difference between the rising of the clock and that of the delayed clock is the period jitter with a constant time offset and the constant offset can be expressed as

$$t_{offset} = T_{sample} - D. \tag{2.10}$$

If the delay, D, is equal to the sampling period, the constant offset is eliminated and the difference between two rising edge is exactly the measured period jitter. In practice, D needs not be equal to the sampling period and their difference just induce a constant correction offset.

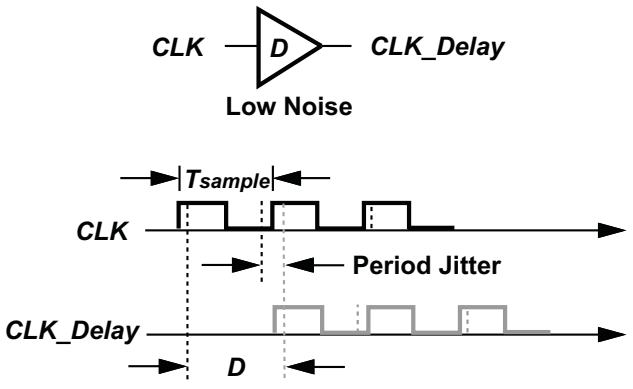


Figure 2.4 Measurement of period jitter.

2.3.2 Derivative Estimation by Two Points

In order to obtain the signal derivative, a linear approach estimates the signal derivative from two adjacent sampled points. In Fig.2.5, t_1 and t_2 are perfect sampling instants; the presence of jitter moves the respect sampling instants to $t_1^{'}$ and $t_2^{'}$, thus comes the error.

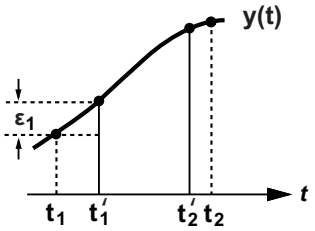


Figure 2.5 Sampling process in presence of clock jitter.

The derivative at t_1 can be approximated as the difference between $y\left(t_1^{'}\right)$ and $y\left(t_2^{'}\right)$ divided by $t_2^{'}-t_1^{'}$.

$$y^{'}\left(t_1\right)\sim\frac{y\left(t_2^{'}\right)-y\left(t_1^{'}\right)}{t_2^{'}-t_1^{'}}=\frac{y\left(t_2^{'}\right)-y\left(t_1^{'}\right)}{T_{sample}-t_{j1}+t_{j2}}. \tag{2.11}$$

Then the estimated error can be expressed as

$$\varepsilon_1\sim\hat{\varepsilon}_1\sim\frac{y\left(t_2^{'}\right)-y\left(t_1^{'}\right)}{T_{sample}-t_{j1}+t_{j2}}\cdot t_{j1}. \tag{2.12}$$

In a more general form,

$$\hat{\varepsilon}_n\sim\frac{y\left(t_{n+1}^{'}\right)-y\left(t_n^{'}\right)}{T_{sample}-t_{jn}+t_{j(n+1)}}\cdot t_{jn}. \tag{2.13}$$

Fig.2.6 shows the simulation results, the gray line stands for SNR versus input signal frequency under 1% RMS jitter and the dark line is that after jitter cancellation.

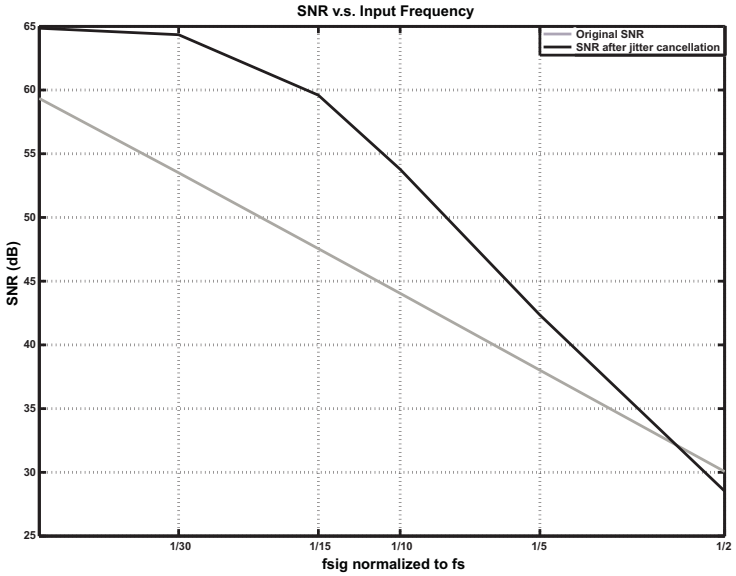


Figure 2.6 SNR versus input signal frequency normalized to sampling frequency.

The SNR with the proposed jitter cancellation technique still become worst as signal frequency gets higher, indicating that the linear estimated derivative is not accurate enough at high frequency. Therefore, the simple algorithm has to be modified to extend the signal bandwidth.

2.3.3 Derivative Estimation by Three Points

In Calculus, the mean value theorem states that given a section of a curve, there is at least one point on that section at which the derivative of the curve is equal to the "average" derivative of the section. The formal statement can be shown as

$$f:[a,b]\to R \text{ continuous on } [a,b] \text{ and differentiable on } (a,b)$$
$$\text{where } a<b$$
$$\text{Then there must exists } c \text{ in } (a,b) \text{ such that}$$
$$f'(c)=\frac{f(b)-f(a)}{b-a}$$

Be inspired by the above theorem, the concept of "average" derivative is imitated to make the estimation more accurate. Fig.2.7 shows three adjacent sampled points at a, c, and b individually and the symbols coincide with those used in mean value theorem for convenience. The derivative at c is approximated as the average derivative of a-c-b section of the curve.

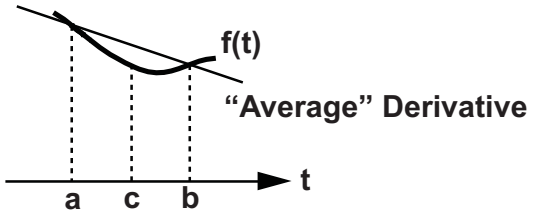


Figure 2.7 Concept of average derivative.

Intuitively, the estimated slope at c is considered as first order interpolation of derivative. On the other hand, this method can also be considered as the average of two adjacent derivatives in our first algorithm.

$$\frac{f(b)-f(a)}{b-a}=\frac{f(b)-f(a)}{2T_{sample}}=\frac{1}{2}\left[\frac{f(b)-f(c)}{T_{sample}}+\frac{f(c)-f(a)}{T_{sample}}\right]. \tag{2.14}$$

Fig.2.8 shows the simulation results of the modified algorithm, obviously the effective bandwidth is wider than before but the performance is still unsatisfied at high frequency.

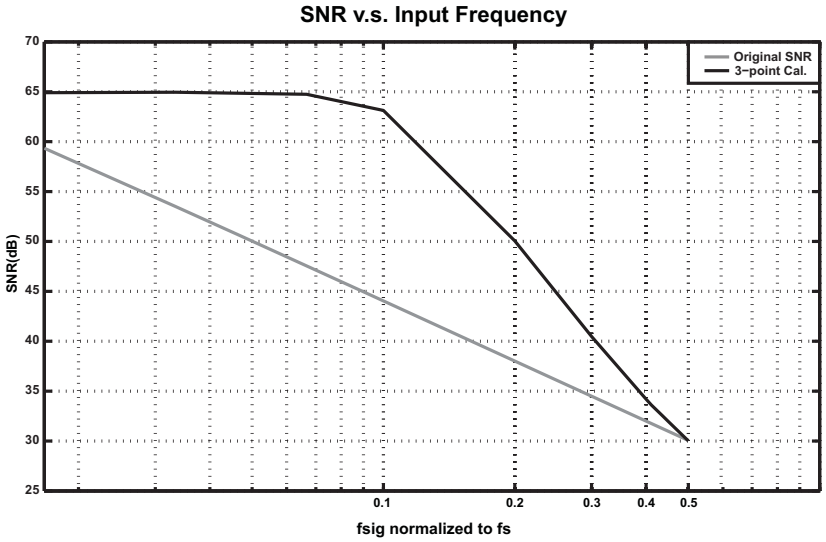


Figure 2.8 SNR versus input signal frequency normalized to sampling frequency.

2.3.4 High Frequency Response Improvement

Let's further look over what worsens the high frequency response. Consider the sinusoidal input $V_{in} = \sin \omega t$ and be sampled at *t*, *t*+*Ts*, and *t*+*2Ts*. Then the estimated slope at *t*+*Ts* is given by (2.15).

$$\begin{aligned} \hat{m}_{t+T_s} &= \frac{\sin \omega\left(t+2T_s\right) - \sin \omega t}{2T_s} \\ &= \omega \cdot \cos \omega\left(t+T_s\right) \cdot \frac{\sin \omega T_s}{\omega T_s} \end{aligned} \tag{2.15}$$

As shown, the estimated slope is modulated by a sinc function which is close to unity at low frequency and degrades at high frequency. This exactly explains the poor high frequency response of the former result. To further improve the performance, a look-up-table method is used to compensate this factor.

Follow the last case, the sinc function can be obtained by doing arithmetic on the three sampled points.

$$\begin{aligned}&\sin\omega\left(t+2T_s\right)+\sin\omega t-2\sin\omega\left(t+T_s\right)\\&=\left[\sin\omega\left(t+2T_s\right)-\sin\omega\left(t+T_s\right)\right]-\left[\sin\omega\left(t+T_s\right)-\sin\omega t\right].\\&=-4\sin^2\left(\frac{\omega T_s}{2}\right)\sin\omega\left(t+T_s\right)\end{aligned}\tag{2.16}$$

The result in (14) is related to the sinc function and the second sampled point.

Let $\Delta=\sin\omega\left(t+2T_s\right)+\sin\omega t-2\sin\omega\left(t+T_s\right)$. (2.17)

By substitution in (2.16),

$$\omega T_s=2\sin^{-1}\left(\sqrt{\frac{-\Delta}{4\sin\omega\left(t+T_s\right)}}\right).\tag{2.18}$$

Finally, the sinc function is expressed as

$$\frac{\sin\omega T_s}{\omega T_s}=\frac{\sin\left(2\sin^{-1}\left(\sqrt{\frac{-\Delta}{4\sin\omega\left(t+T_s\right)}}\right)\right)}{2\sin^{-1}\left(\sqrt{\frac{-\Delta}{4\sin\omega\left(t+T_s\right)}}\right)}.\tag{2.19}$$

With (2.19), a look-up-table can be applied to proposed algorithm to enhance high frequency performance further and Fig.2.9 is the simulation results.

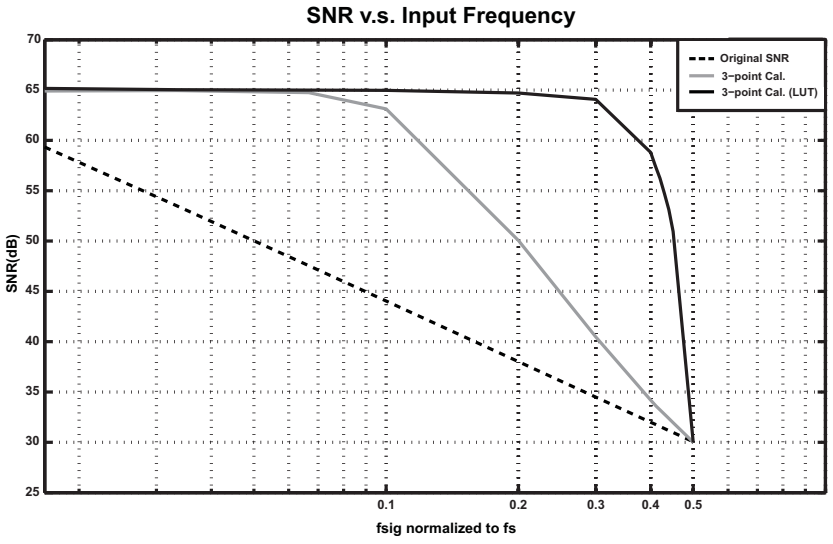


Figure 2.9 SNR versus input signal frequency normalized to sampling frequency.

2.4 Summary

It has long been known that the sampling clock jitter degrades performance of an ADC, so a method of jitter error cancellation in digital domain for ADC is proposed to alleviate the jitter requirement. The additional hardwares are four 12-bit registers, two multipliers, and a ROM table. The proposed method has at most 30dB improvement around Nyquist zone.

Chapter 3

Fundamentals of Time-to-Digital Converter

3.1 Introduction

This chapter reviews some of the fundamental issues in the design of a time-to-digital converter (TDC). As mentioned, a time-to-digital converter (TDC) is required to adapt the jitter cancellation algorithm in this system. Besides, it is supposed to have wide dynamic range and high precision in order to cover the peak-to-peak jitter variation while maintain the accuracy. As technology development is mainly driven by digital requirements, the scaling of time resolution is superior to voltage resolution. Thus, high-resolution TDCs become increasingly popular for time-of-flight measurements, full speed testing, e.g., jitter measurement, clock data recovery, measurement and instrumentation, and all-digital phase-locked loops (ADPLLs).

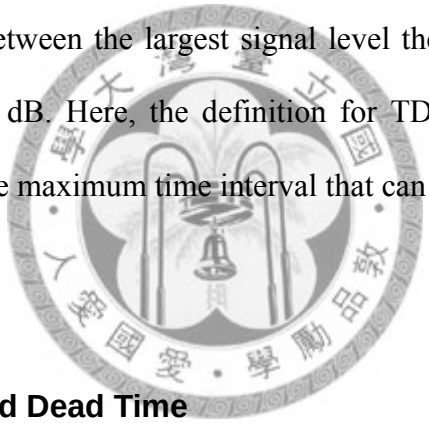
In order to characterize the TDCs thoroughly, a number of performance metrics are defined. Following a definition of performance metrics, we describe a number of TDC architectures commonly employed in high-resolution applications.

3.2 TDC Performance Metrics

Functionally, TDCs are very similar to ADCs except that not a continuous voltage but a continuous time interval is quantized. Hence, all performance figures describing the function of ADCs can also be applied to a TDC. In this section, the definitions of a number of important metrics are described.

3.2.1 Dynamic Range

Dynamic range is the ratio between the largest signal level the converter can handle and the noise level, expressed in dB. Here, the definition for TDC is a little different. The dynamic range of a TDC is the maximum time interval that can be measured and quantized without any saturation.



3.2.2 Conversion Time and Dead Time

The conversion time or the latency, respectively, describe how long it takes after a start or stop signal before the digital code is available at the output. However, the dead time is the minimum idle time between two adjacent conversions before the next measurement can be started.

3.2.3 Single Shot Precision

The noise performance of a TDC is usually described by the single shot precision: If a constant time interval is measured repeatedly, the digital output values vary with a standard

deviation that is called single shot precision.

The rms single shot precision σ_{rms} defines the rms value of the TDC noise performance

$$\sigma_{rms} = \sqrt{\sigma_q^2 + \sigma_{start}^2 + \sigma_{stop}^2 + \sigma_{tdc}^2} \quad . \tag{3.1}$$

where σ_q is the rms quantization noise, σ_{start} and σ_{stop} are the rms jitter of the start and stop signals, and σ_{tdc} is the total jitter contributed by TDC.

3.2.4 Interpolation Factor (IF)

For TDCs with sub-gate delay resolution, the interpolation factor IF is defined by $IF = T_{ref} / T_{LSB}$ which serves as a useful index to estimate which resolution is provided by the available technology and which additional resolution is accomplished by circuit techniques.

3.2.5 Nonlinearity

Another method to identify the performance of a data converter is to plot the input/output characteristic of it. The transfer characteristic for an ideal TDC progresses from low to high in a series of uniform steps. As the resolution increases, the input/output characteristic of TDC approximates a straight line. In practical TDC, the steps are not perfectly uniform due to nonidealities, such as offset error, gain error, and linearity error. Fig.3.1 shows the deviation of transfer characteristics resulted from offset error and gain error respectively.

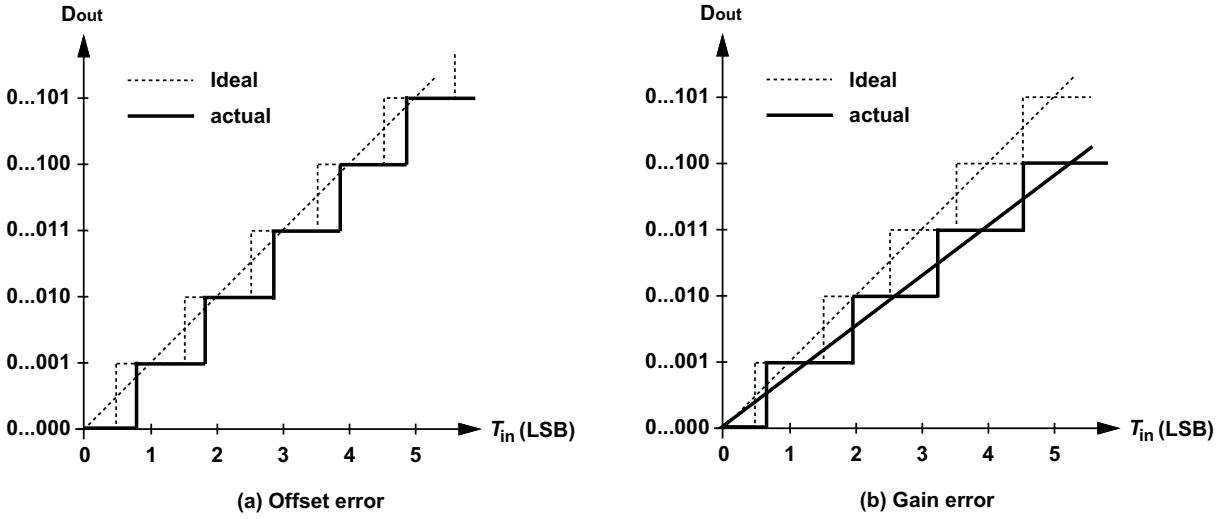


Figure 3.1 Transfer function including error sources. (a) Offset error, (b) gain error

Two types of nonlinearity measurement metrics are used to characterize this deviation. Differential nonlinearity (DNL) is the maximum deviation in the difference between two consecutive code transition points on the input axis from the ideal value of 1LSB. Integral nonlinearity (INL) is the maximum deviation of the input/output characteristic from a straight line passed through its end points. Fig.3.2 and Fig.3.3 illustrates the DNL and INL, which can be expressed as:

$$DNL(i) = \frac{UB(i+1) - UB(i)}{LSB} - 1$$
$$INL(i) = \frac{UB(i) - UB(i)_{ideal}}{LSB} \tag{3.2}$$

where $UB(i)$ is the transition level of i-th code.

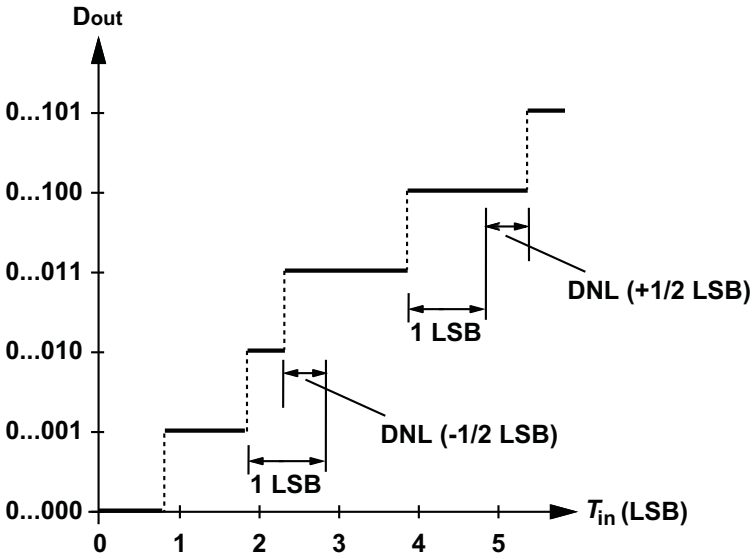


Figure 3.2 Transfer characteristic of TDC showing DNL.

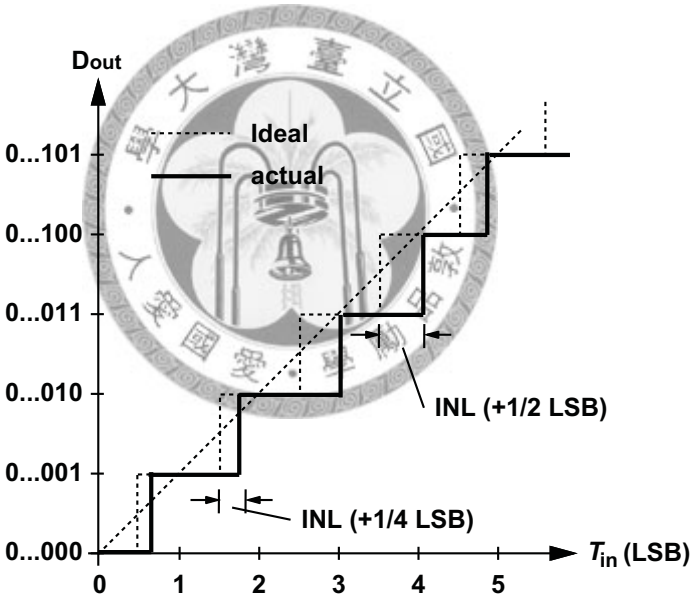


Figure 3.3 Transfer characteristic of TDC showing INL

3.3 Architectures of Time-to-Digital Converters

3.3.1 Time-to-Voltage-to-Digital Converters

The very first TDCs were actually time-to-voltage-to-digital converters [8], shown in

Fig.3.4. In this converter, the time interval to be measured is first converted into an analog voltage by a charge pump and record in a capacitor. Then a conventional analog-to-digital converter (ADC) translates the analog value equivalent of the time interval into the digital domain.

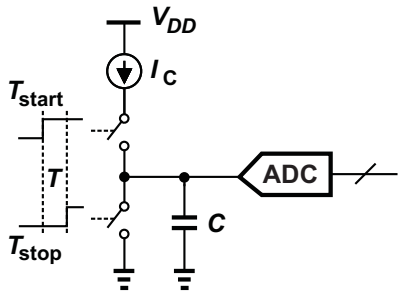


Figure 3.4 Time-to-voltage-to-digital converter topology

Although very high resolution has been reported [9], the attractiveness of these converters decreases for technologies below the quarter micron node. The resolution, the scalability, the robustness and the area and power consumption are limited by the internal ADC, so the time domain yields no profit compared to the voltage domain with strongly technology scaled.

3.3.2 Vernier-Based TDC

The Vernier TDC [10]-[12] utilizes parallel scaled delay elements to provide a high sub-gate delay resolution. Both the start and the stop signal are delayed in independent delay lines. The basic configuration is depicted in Fig.3.5.

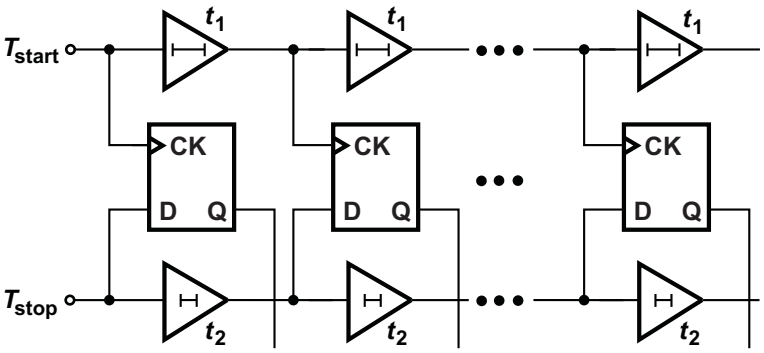


Figure 3.5 Vernier-based TDC architecture.

The delay for the stop signal t_1 is designed for slightly faster signal propagation than that of t_2 for the start signal. As the start and stop signals propagate in the respective delay chains, the time difference between them is decreased in each stage by $t_R = t_1 - t_2$ which is equivalent to the TDC's resolution T_{LSB}. The position X in the delay line, where the stop signal catches up with the start signal, gives the information about the measured time t_x with t_R resolution

$$X \cdot t_R < t_x < (X+1) \cdot t_R \quad . \tag{3.3}$$

Theoretically, the resolution t_R can be infinite small if t_1 and t_2 are close enough but the presence of noise and process variations will set the upper bound of the TDC. Assuming local process variations of the buffer delays, the time difference between the start and the stop edge in a certain stage is reduced with a 3σconfidence only if $T_{LSB} > 3\sqrt{2}\sigma_{buffer} = 6\sigma_{inv}$. This can be seen as a simple rule of thumb for an upper bound of the delay-line based TDC resolution [13].

As for the conversion time, according to $T_{conv} = 2T_{inv}\left(t_x / T_{LSB}\right)$, it increases linearly with measured time interval t_x and even hyperbolically with increasing resolution. The same holds for the area, thus, for large dynamic range and small T_{LSB}, Vernier TDCs

become both slow and area expensive.

3.3.3 Pulse-Shrinking Cyclic TDC

Pulse-shrinking TDC is based on unequally sized inverters, illustrated in Fig.3.6. First, the start and the stop signal are used to generate a pulse with a pulsewidth equal to the time difference. The dimensions of the gates I_1 and I_3 are the same. Only that of the gate I_2 is different. The inhomogeneous dimension of the gates makes the input pulse undergo different rising and falling time at the interface boundaries among the gates and be shrunk by T_{LSB}.

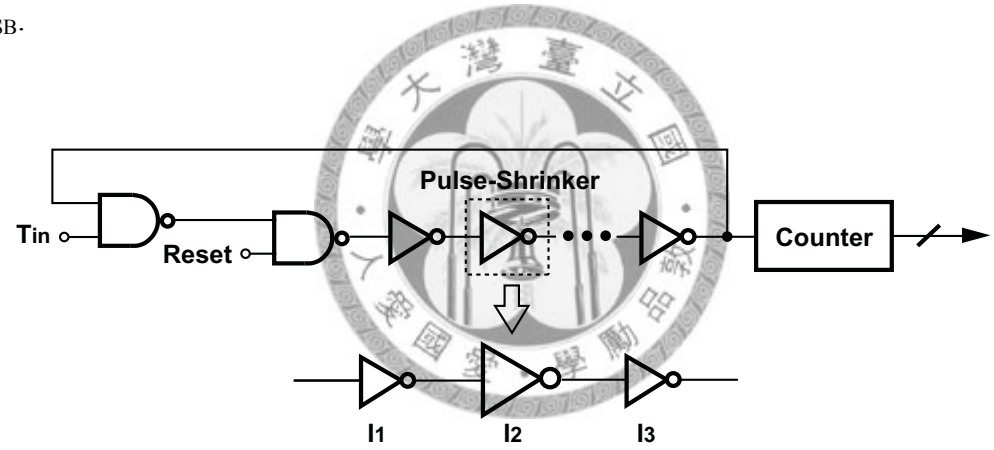


Figure 3.6 System architecture of a pulse-shrinking cyclic TDC.

The resolution of TDC T_{LSB} can be derived through the mismatch between the falling and the rising time [14]. The total pulse-shrinking time can be found as

$$T_{LSB} = \rho\left[C_2\left(\frac{1}{k_{p1}} - \frac{1}{k_{n1}}\right) - C_1\left(\frac{1}{k_{p2}} - \frac{1}{k_{n2}}\right)\right] \tag{3.4}$$

where

$$\rho = \frac{2V_{Tn}}{\left(V_{DD} - V_{Tn}\right)^2} + \frac{1}{\left(V_{DD} - V_{Tn}\right)} \cdot \ln\left(\frac{1.5V_{DD} - 2V_{Tn}}{0.5V_{DD}}\right) \tag{3.5}$$

is a constant factor which is more or less layout independent, $k_{n1,2}$, $k_{p1,2}$ are the transconductance of the gate I_1 and gate I_2 and $C_{1,2}$ are the effective input capacitance of them.

The input pulse is shrunk cyclically and vanishes when the time interval is completely measured. Since only one pulse-shrinking element exhibits, there is no matching problem in the cyclic TDC, hence, good linearity. But the conversion time and the dead time rapidly grow with increasing dynamic range and resolution.

3.3.4 DLL Interpolation TDC

One difficulty to all delay-line based TDCs is the dependence of the time resolution on the delay variation caused by global process variations. With the help of delay-locked loop (DLL), the cycle time of an external reference clock can be divided into several shorter time periods with a delay line. The incoming moment of the timing signal can then be interpolated inside the reference clock period by recording the state of this delay line, enabling the time interval to be defined with better resolution than by reference clock.

The time interval measurement method, with a counter and a delay line which divides one reference clock cycle T_{ref} into eight pieces, each of length t_1, is illustrated in Fig.3.7 [15]. The state of the delay line is recorded by asynchronous timing signals, while the counter counts full reference clock periods between these signals.

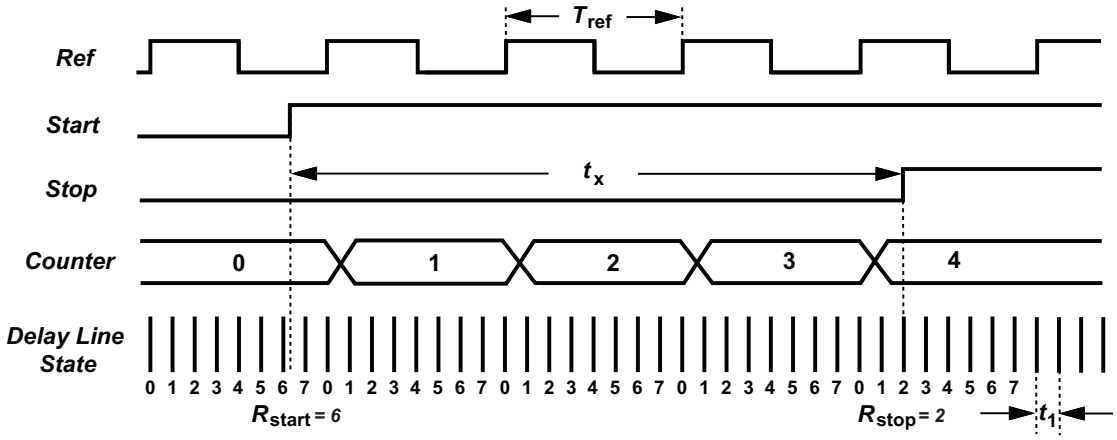


Figure 3.7 Delay line interpolation.

The measured time t_m for the real time interval t_x consists of the sum of the counter result C and the interpolated results, shown as

$$t_m = C \cdot T_{ref} + \left(R_{stop} - R_{start} \right) \cdot t_1 \quad . \tag{3.6}$$

The DLL interpolation method is based on the constant propagation delay of matched series-connected cells. A practical realization of that method including a counter and a delay line interpolation structure capable of generating and registering time periods equal to reference clock period, is shown in Fig.3.8. The counter is enabled with the start signal and disabled with the stop signal. The reference clock propagates through the delay line and the positions of both the start and stop signals are also recorded by the clock edges spacing t_1 and the arbiter array consists of D-type flip-flops for both start and stop.

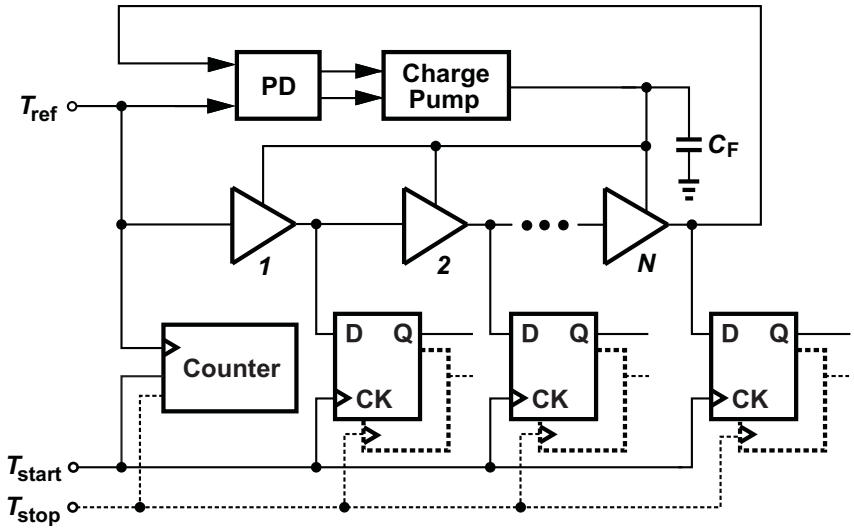


Figure 3.8 The block diagram of a DLL interpolation TDC

The signal propagation speed of the digital gates may be affected by temperature, voltage, and process parameter changes. To get over this problem, a DLL is typically applied to stabilize the delay in the delay line which is matched to the reference clock cycle with a control loop including a phase detector (PD), a charge pump, and a loop filter. The DLL adjust the delay of the elements with a control voltage until the PD sees that the feedback edge is aligned to the reference clock edge, which means the length of the line delay is then locked to the reference cycle period.

3.3.5 Local Passive Interpolation TDC

The local passive interpolation TDC [13] achieves a sub-gate delay resolution by subdividing the coarse time interval given by an inverter delay line. The basic principle is similar to the voltage interpolation in interpolating flash or folding ADCs [16] and is illustrated in Fig.3.9. Parallel sampling gives a high-resolution thermometer code but at the same low latency and dead time as for the buffer chain based TDC. In contrast to the

Vernier and pulse shrinking TDC, this means that the conversion time doesn't increase with increasing resolution.

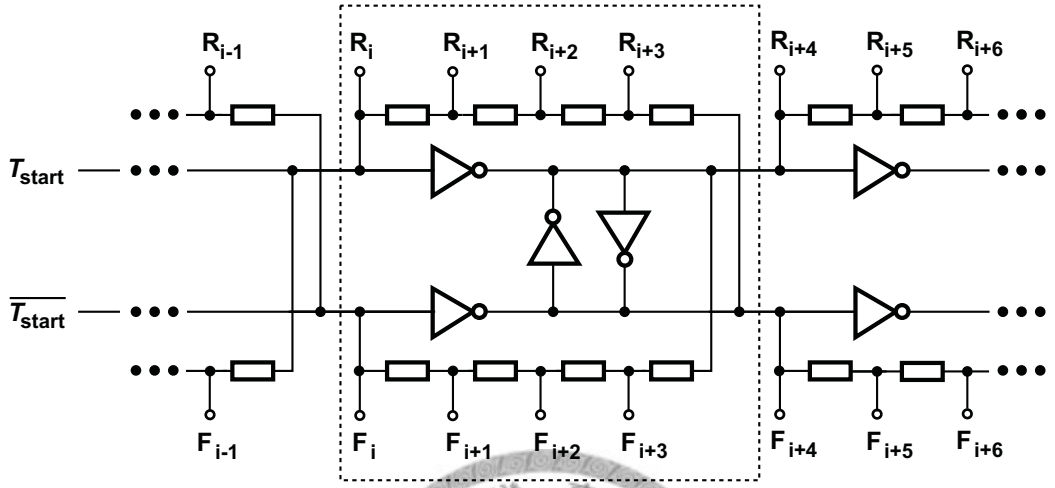


Figure 3.9 Local passive interpolation TDC architecture

Also, the LPI-TDC is monotonic by construction. The sequential inverter chain is monotonic even under strong variations due to the causality in the delay line. The passive interpolation also makes LPI-TDC to be robust against local variations. If the delay of an inverter stage varies, the passive interpolation translates this variation to a subdivided variation of the intermediate signals. The sequence of the interpolated signals remains unchanged even for strongly varying resistors.

Chapter 4

System Architecture of a MDLL-Based TDC with Local Passive Interpolation

4.1 Introduction

To meet the specification of our system, a MDLL-based TDC with local passive interpolation is proposed. As known, the multiplying delay-locked loop (MDLL) [17] eliminates phase error accumulation by zeroing the phase error on every input clock edge and recirculates the clock edge along the delay line. To take these advantages, low jitter as well as high dynamic range are achieved. With local passive interpolation, that is, connecting the outputs of adjacent delay cells by resistor string, sub-gate delay is generated. Furthermore, the phase differences between the delay cells caused by mismatch are averaged at the same time.

The basic building blocks utilized in this TDC including MDLL and interpolation as well as averaging resistor string, are first reviewed in the following text. Then the architecture of the MDLL-based TDC with local passive interpolation is presented.

4.1.1 Multiplying DLL (MDLL)

Fig.4.1 shows the basic concept of the multiplying DLL (MDLL) with its detail timing diagram. At beginning, the delay line is open and waits for the transition edge of the

reference clock. After receiving the clock edge, the control signal, V_{sel}, closed up the delay line via the multiplexer, a ring oscillator is formed that oscillates with a period twice that of the delay around the DLL loop composed of the inverters and multiplexer generating the multiplied output clock V_{out}. The divide-by-M counter divides down the multiplied output clock to generate a pulse, V_{div}, every M cycles of the V_{out}. The V_{div} signal triggers the control logic that switches the multiplexer input to pass a clean reference clock. This function resets the ring oscillator phase to the phase of the clean edge, removing the accumulated jitter over the past cycles. Therefore, the maximum number of cycles that the ring oscillator accumulates jitter is limited to *M*.

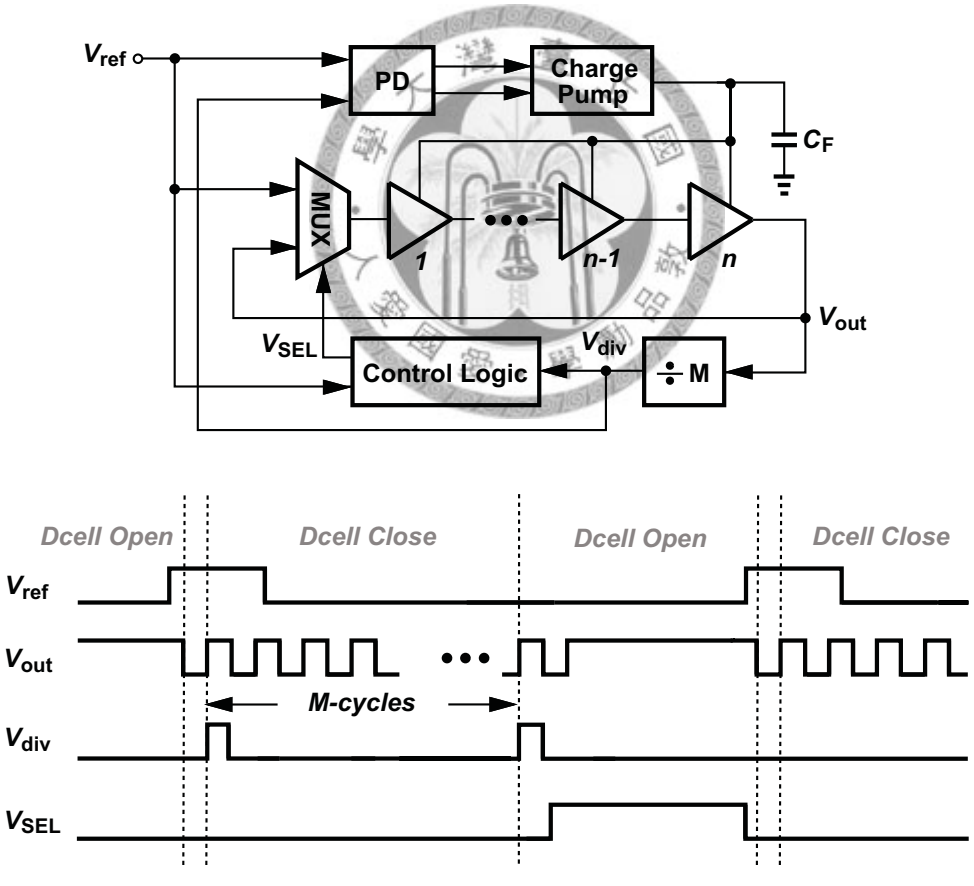


Figure 4.1 The architecture and the timing diagram of a multiplying DLL.

The PD and CP adjust the time delay of the delay line, and eventually the phase difference

between the reference clock and feedback clock drops to zero. We said that the system is locked and the MDLL generates the multiplied clock.

Any mismatch between the swing levels, transition times, and timing alignment of the reference clock edge to the corresponding multiplied output clock edge results error during signal multiplexing which leads to deterministic jitter in the output clock.

If the loop bandwidth of the MDLL is much smaller than the reference frequency, the loop bandwidth can be approximated by the *s*-domain approach. However, to obtain the maximum loop bandwidth, a more detail approach to analyze the loop stability and the settling time must be utilized. The discrete time model for the MDLL is shown in Fig.4.2 [18].

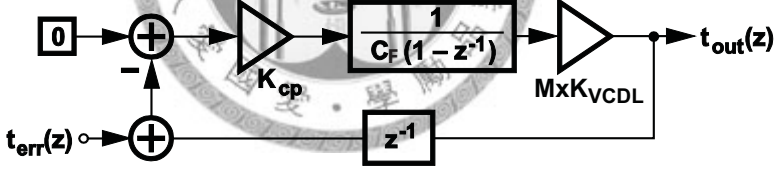


Figure 4.2 System model of the MDLL.

The feedback clock has a phase difference with the reference clock at beginning, and there will be an instant time error, t_{err}. The phase of the reference clock remains unchanged, and there is no input time error. The loop filter which consists of a capacitor acts as an integrator which can be modeled as $\frac{1}{1-z^{-1}}$ in a discrete time system. A charge pump can be modeled as a constant gain block which has a gain of $K_{cp}=I_{cp}$. The current signal is converted to the voltage signal by the loop filter and controls the VCDL which has a gain

of M times K_{VCDL} with divide-by-M counter modeled.

The input to output transfer function can be derived as

$$-(t_{out}(z)\cdot z^{-1}+t_{err}(z))\cdot\frac{K_{CP}\cdot M\cdot K_{VCDL}}{C_F\cdot(1-z^{-1})}=t_{out}(z)\ . \tag{4.1}$$

The definition of the open loop gain K can be expressed as

$$K=\frac{K_{CP}\cdot M\cdot K_{VCDL}}{C_F}\ . \tag{4.2}$$

Then the input/output transfer function can be obtain

$$\frac{t_{out}(z)}{t_{err}(z)}=\frac{-K}{1-(1-K)\cdot z^{-1}} \tag{4.3}$$

which is a first order system. The switching in feedback signal can be viewed as an instant time step input appears at the feedback path. This time step input can be expressed as

$$t_{err}(n)=\theta_o\cdot u(n)\ . \tag{4.4}$$

Applying z-transform, we can get

$$t_{err}(z)=\frac{\theta_o}{1-z^{-1}}\ . \tag{4.5}$$

The output time error will be

$$t_{out}(n)=-\theta_o\cdot(1-(1-K)^{n+1})\cdot u(n)\ . \tag{4.6}$$

For a stable MDLL, the open loop gain K must be larger than 0 and smaller than 2 for the consideration of the system stability. In practice, K is selected to be less than unity to avoid severe ringing in the control line. From above analyze, the maximum bandwidth of MDLL can be estimated, and the stability criterion is also obtained.

4.1.2 Local Passive Interpolation and Phase Averaging

As mentioned in the last chapter, local passive interpolation TDC interpolates the start signal along the delay line. However, in the MDLL-based TDC, clock phases are interpolated into sub-gate delay resolution to sample the asynchronous start and stop signal by local passive interpolation. Hence, the phase accuracy affects the linearity directly in this architecture. Fortunately, these passive interpolation components can also average the phase error for the multiphase generation.

For the interpolated signals to follow the input signals instantaneously, the RC value at each node should be lower to minimize the delay. Elmore delay model provides a good estimation on describing path delays in the RC network.

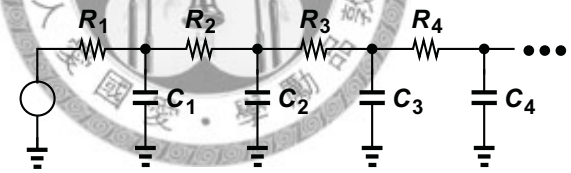


Figure 4.3 Elmore delay model.

Fig.4.3 illustrates the Elmore delay model and it states that at node *n* the signal delay can be roughly estimated as

$$\tau_{ED,n} = R_1C_1 + (R_1 + R_2)C_2 + \cdots + (R_1 + R_2 + \cdots + R_n)C_n. \quad (4.7)$$

From (4.7), the worst case delay in *n*X interpolation is

$$\tau_{ED,n} = \frac{n(n+1)}{2}RC. \quad (4.8)$$

The worst case delay must be much smaller than the rising time of the input signals which provides the insight on choosing the resister value.

One reported technique is to reduce the phase mismatch by resistor averaging [19]. The principle is to connect the neighboring delay cells together by resistor strings or resistor rings. The resistor strings or resistor rings have an averaging capability to suppress the phase mismatch introduced by the mismatch in delay cells. The architecture of a DLL with resistor averaging is shown in Fig.4.4

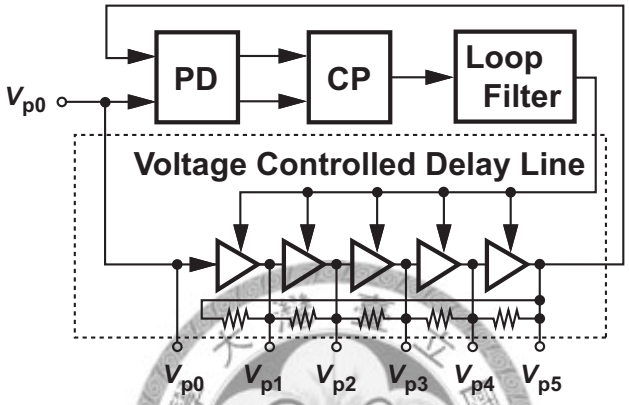


Figure 4.4 Resistor averaging

The resistor string and resistor ring bring spatial filtering effect on DLL's multiple outputs [20]. If the resistors are infinitely large, the operations of the delay cells are mutually independent. As the value of the resistors drop, the outputs of the delay cells are affected by the neighboring delay cells. The reason is that the output currents from each delay cell flow into the loads of their neighbors, rather than their own ones through the resistor string or ring. Hence, the resistor string and ring introduce a phase averaging effect. In order to quantitatively analyze the averaging network behavior, the simplified model shown in Fig.4.5 is used.

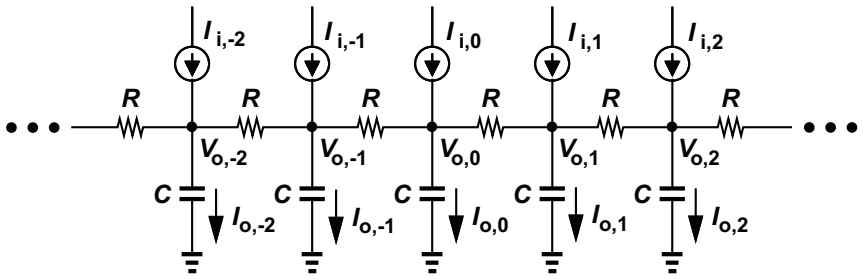


Figure 4.5 A simplified model for analyzing a delay line with a R-string

The capacitance at each output node is *C*. The delay cells are modeled as ideal current sources with sinusoidal output currents expressed as

$$I_{i,x} = I_A \sin\left(\omega_i t + \phi_{i,x}\right) \text{ , } x = 0, \pm 1, \pm 2, \ldots \tag{4.9}$$

where I_A is the current amplitude, ω_i is the clock frequency, and $\phi_{i,x}$ is the clock phase. The output current flowing into the output capacitor is $I_{o,x}$. Derived from the simplified model with $I_{i,x} = 0$ for $x \neq 0$, the transfer function of the single delay cell current $I_{o,0}$ to the output current $I_{o,x}$ can be expressed as [19]

$$\frac{I_{o,x}}{I_{o,0}} = \frac{R + \sqrt{R\left(R + 4Z_C\right)}}{R + \sqrt{R\left(R + 4Z_C\right)} + 4Z_C} \left[\frac{2Z_C}{2Z_C + R + \sqrt{R\left(R + 4Z_C\right)}} \right]^{|x|} . \tag{4.10}$$

Substituting $\omega_i RC$ with β, the above equation can be manipulated to

$$A_I\left(\beta, x\right) = \frac{I_{o,x}}{I_{o,0}} = \frac{\left(-\frac{4j}{\beta}\right)^{|x|}}{\sqrt{1 - \frac{4j}{\beta}} \left(1 + \sqrt{1 - \frac{4j}{\beta}}\right)^{|2x|}} \tag{4.11}$$

is the input frequency normalized by the *RC* product of the R-string

Fig.4.6 shows the space response of current gain versus different β. At x=0, the gain is increased for large β, i.e., at higher clock frequency, more current flows into the capacitor directly connected to the current source. For increasing β, $\left|A_I\left(\beta, 0\right)\right|$ approaches

1 and the resistor string loses its effect of phase averaging. For smaller β, the current is distributed more to the neighboring output node, resulting in a strong phase averaging. Hence the mismatch between delay cells is alleviated, and the linearity is improved.

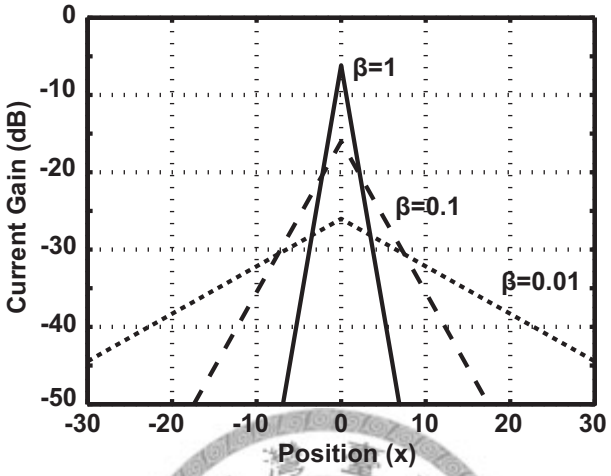


Figure 4.6 Space response of R-string

4.2 Architecture of the MDLL-Based TDC with Local Passive Interpolation

4.2.1 System Architecture

A MDLL-based TDC with local passive interpolation is proposed for jitter-induced error cancellation in ADC. Fig.4.7 shows the system block diagrams of it. This TDC is composed of an MDLL, an arbiter array, and an encoder. The MDLL provides sub-gate delay multiphase

clock system. The detail clock generation is illustrated in Fig.4.8. In this case, the divide ratio *M* is set to be *4* for simplification and there are *8* delay cells along the delay line with *4X* interpolation.

The arbiter array consists of D-type flip-flops to locate the positions of asynchronous start and stop signals along the interpolated delay line. Then the pseudo thermometer code output by the arbiter is fed into the encoder to generate binary digital code.

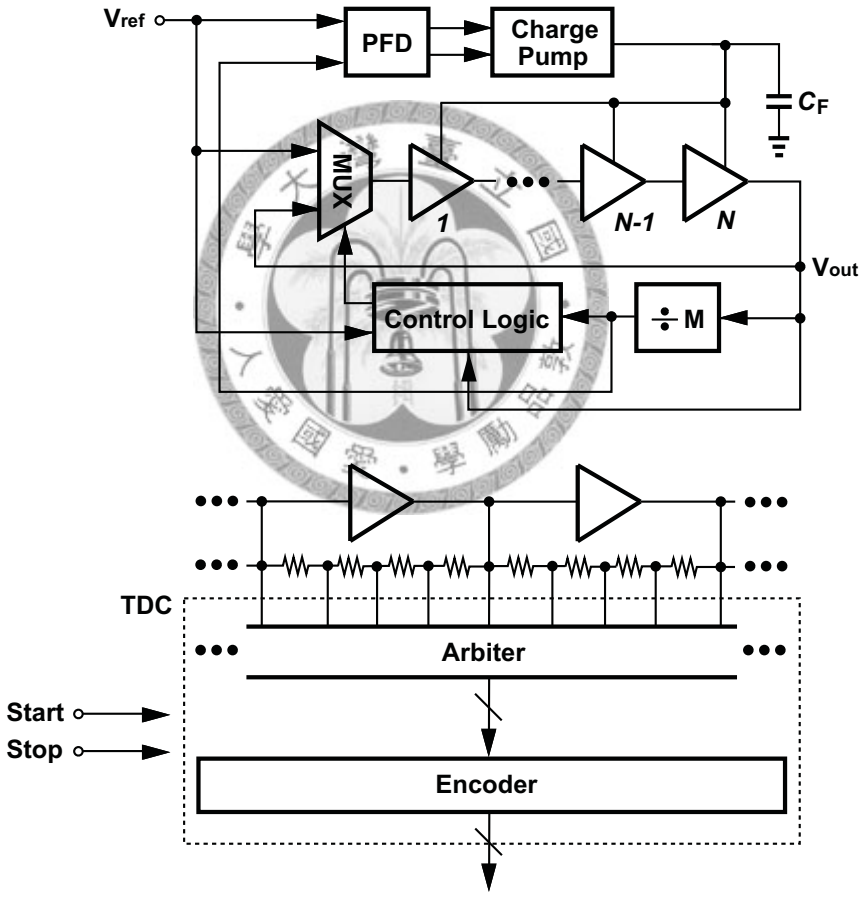


Figure 4.7 Architecture of the MDLL-based TDC with local passive interpolation.

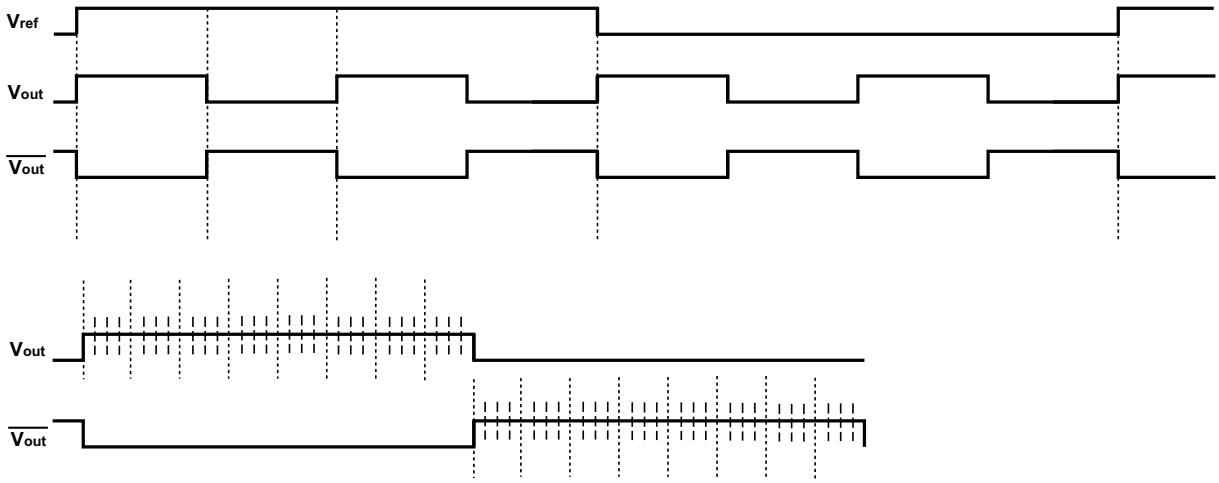


Figure 4.8 Clock generation diagram.

4.2.2 Dynamic Range and Resolution

The specification of the TDC in the whole system is defined to be 10ps resolution with more than 5ns dynamic range. The resolution T_{LSB} of the proposed TDC is mainly decided by the stabilized delay T_d of the MDLL and the local passive interpolation ratio r.

$$T_{LSB} = \frac{T_d}{r}. \tag{4.12}$$

Typically, in any passive interpolating design, *4X* interpolation is a reasonable choice to obtain an acceptable linearity. Hence the stabilized delay T_d is going to be designed as 40ps.In order to achieve the target dynamic range, *125X* interpolation is still required. The extra interpolation is contributed by the choice of number of the delay cells and the multiplying ratio of the MDLL. Assume that the number of the delay cells along the delay line is N, and the multiplying ratio is M, the extra interpolation is given by

$$Extra\ Interpolation = 2MN\ . \qquad . \tag{4.13}$$

Another advantage given by this architecture is that, for a fixed number of delay cells and a constant delay, the dynamic range is directly proportional to the multiplying ratio of the MDLL, only to add the extra bits to the counter. But the upper bound is limited by the accumulated jitter in the ring oscillator. The first-order analysis on inverter jitter due to white noise is enough for us to predict the accumulated jitter in the ring oscillator [21]. Consider a positive input step in Fig.4.9, the input shuts off the PMOS and biases the NMOS in the saturation.

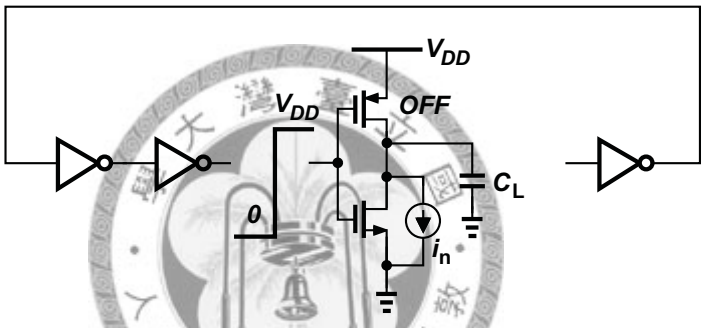


Figure 4.9 Inverter switching in ring oscillator, showing signal and noise currents

Then the uncertainty in propagation delay caused by current noise integrating on the capacitor C is

$$\sigma_{tdN}^2 = \frac{4kT\gamma_N t_{dN}}{I_N\left(V_{DD} - V_{tN}\right)} \tag{4.14}$$

where t_{dN} is the propagation delay, I_N is the noise current, and the coefficient γ is derived to be equal to 2/3 for long-channel transistors and may need to be replaced by a larger value for submicron MOSFETs [22]. Prior to the switching event the channel resistance of the PMOS pullup deposits an initial noise on the capacitor. The mean square noise and the associated jitter are

$$\left\langle v_n^2 \right\rangle = \frac{kT}{C} \tag{4.15}$$

$$\sigma_{tdN}^2 = \frac{\left\langle v_n^2 \right\rangle}{\left(I_N / C\right)^2} = \frac{kTC}{I_N^2}. \tag{4.16}$$

Thus, the total jitter due to these two uncorrelated white noise source is

$$\sigma_{tdN}^2 = \frac{4kT\gamma_N t_{dN}}{I_N\left(V_{DD} - V_{tN}\right)} + \frac{kTC}{I_N^2}. \tag{4.17}$$

The period of oscillation T_{osc} of a ring oscillator is defined by the time it takes for a transition to propagate twice around the ring. In a ring oscillator consists of N inverter delay stages, this involves N pulldowns by NMOSs and N pullups by PMOSs. Thus, the nominal frequency of oscillation f_{osc} is

$$f_{osc} = \frac{1}{N\left(t_{dN} + t_{dP}\right)} \sim \frac{2}{NCV_{DD}}\left(\frac{1}{I_N} + \frac{1}{I_P}\right)^{-1} \sim \frac{I/C}{NV_{DD}}. \tag{4.18}$$

Every propagation delay is jittered by noise in the pullup or pulldown process. These noise events are uncorrelated and add in the mean-square. Therefore, the variance of period jitter is

$$\sigma_T^2 = N\left(\sigma_{tdN}^2 + \sigma_{tdP}^2\right). \tag{4.19}$$

Using (4.15) and (4.16), and to simplify analysis assuming that $V_{tN} = V_{tP} = V_t$, this can be written as

$$\sigma_T^2 = \frac{2kT}{If_{osc}}\left(\frac{1}{V_{DD} - V_t}\left(\gamma_N + \gamma_P\right) + \frac{1}{V_{DD}}\right). \tag{4.20}$$

The accumulated jitter in the ring oscillator has to be smaller the $0.5T_{LSB}$. Thus,

$$\sigma_{accum} = \sqrt{M \times \sigma_T^2} < 0.5 \cdot \frac{T_{ref}}{2MN \times 4}. \tag{4.21}$$

The upper bound of the multiplying ratio is

$$M < \left(\frac{T_{ref}}{16N\sigma_T} \right)^{1/3} \tag{4.22}$$

where $T_{ref}=M/f_{osc}$.

4.3 Summary

From the above discussion, the specification and the noise performance set two design constraints as

$$Extra\ Interpolation = 2MN > 125 \tag{4.23}$$

and

$$M < \left(\frac{T_{ref}}{16N\sigma_T} \right)^{1/3}. \tag{4.24}$$

Both the multiplying ratio M and the number of the delay cells N are choose to be 8 to meet the constraints, meanwhile, the noise margin is also consider.

A 10ps, 5.12ns dynamic range, MDLL-based TDC with local passive interpolation is designed and provided with a 200MHz external reference clock.


國立臺灣大學
學術品德・愛國愛人

Chapter 5
Circuit Implementation

5.1 Introduction

This chapter provides a complete circuit design scheme of a MDLL-based TDC with local passive interpolation. From high-level architecture to building blocks implementation, both design considerations and simulation results are thoroughly introduced.

5.2 Architecture

Figure 5.1 illustrates the complete architecture of the MDLL-based TDC with local passive interpolation. The MDLL provides sub-gate delay multiphase clock system. And the arbiters decide which states the asynchronous start and stop signals are in. Then the pseudo thermometer code output by the arbiter is fed into the encoder to generate binary digital code for the start and stop respectively. The final result is combined by the digital processing unit out of chip in the real implementation. The detail circuit implementation and operating principles of each building block will be illustrated in the following sections.

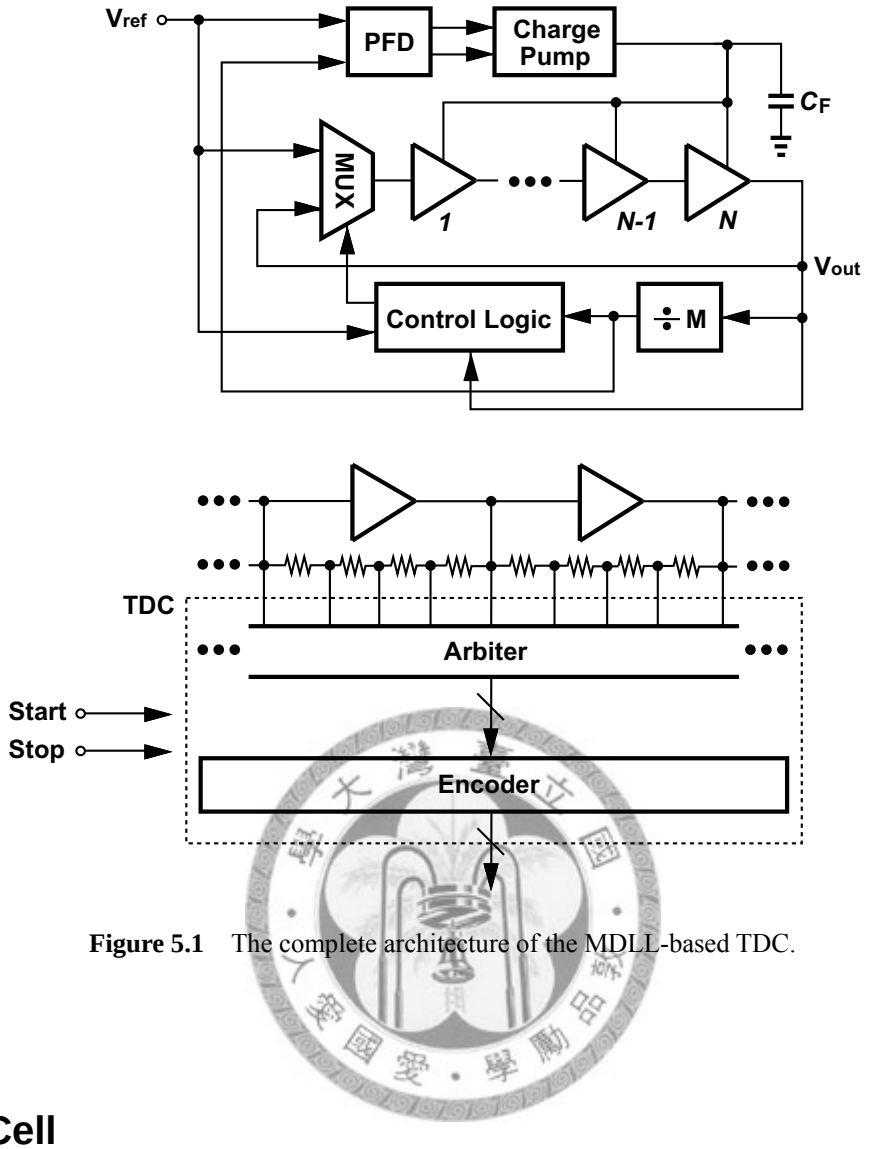
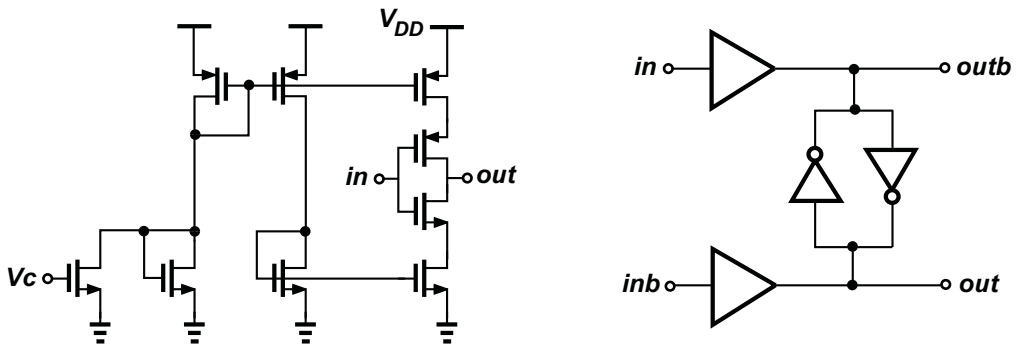


Figure 5.1 The complete architecture of the MDLL-based TDC.

5.3 Delay Cell

The delay cell adopted in this work is a current-starving inverter as shown in Fig.5.2. The amount of current flowing through the delay cell determines the propagation delay of the input signal. The circuit performs a rail-to-rail operation and doesn't consume static power. Differential operation is required here. Fig. shows that cross-coupled inverters are utilized to regulate differential outputs to perform the pseudo-differential operation. The aspect ratio of the cross-couple pair must be smaller than that of the inverter in the delay cell. If the aspect ratio of the inverter in the delay cell is 5 times larger than that of the cross-couple pair, the effect of it will degrade.



(a) (b)

Figure 5.2 (a) Single ended delay cell. (b) Delay cell with cross-couple inverters

5.4 Phase Frequency Detector (PFD)

Typically, the MDLL is started at its maximum startup control voltage to ensure the correct multiplexing function. In this work, the mechanism of the control logic is modified to make the MDLL work properly without the constraint of initial condition. Thus, a PD need to be replaced with a PFD in the system.

In this work, the operational frequency of PFD is about 200 MHz. So a dynamic logic type PFD is used [23], as shown in Fig.5.3. The critical path of this PFD is composed of three-gate feedback path. The shorten feedback path delay and dynamic operation allow high precision in the high frequency operation. If $V_{up} = V_{dn} = 0$ and V_{ref} goes high, V_{up} rises. If this event is followed by a rising transition on V_{dn}, V_{dn} goes high and the NOR gate sets both dynamic logics.

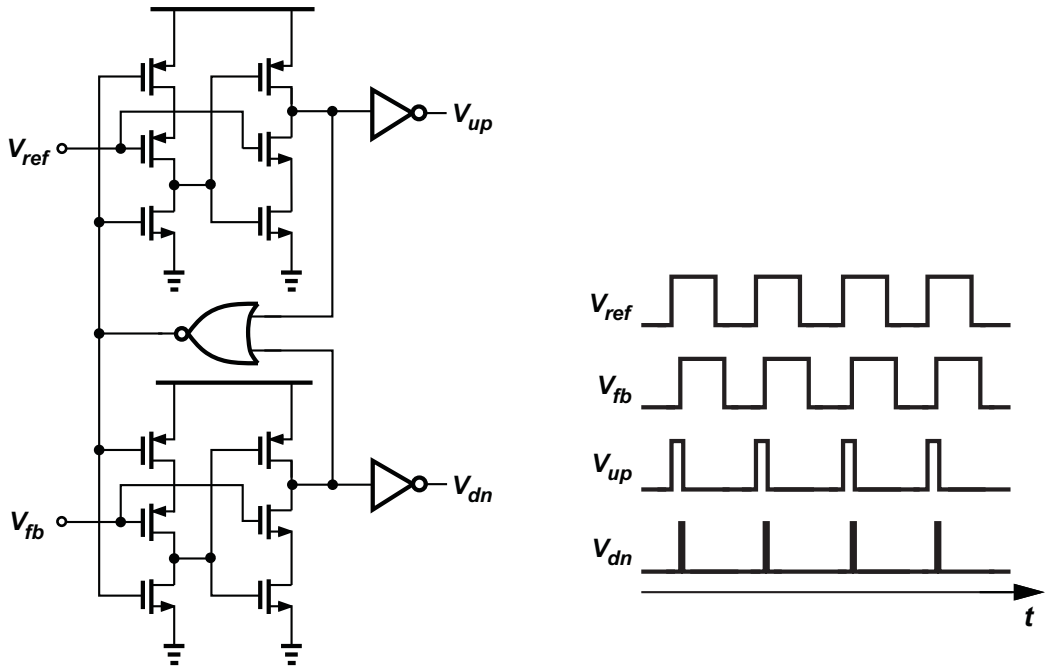


Figure 5.3 Dynamic logic type PFD and its corresponding timing diagram.

It is instructive to plot the input-output characteristic of the PFD, as shown in Fig.5.4. Defining the output as the difference between the average values of V_{up} and V_{dn} when $\omega_{ref} = \omega_{fb}$ and neglecting the effect of the narrow reset pulses, we note that the output varies symmetrically as $|\Delta\Phi|$ begins from zero. For $\Delta\Phi = \pm 360^{\circ}$, V_{out} reaches its maximum or minimum and subsequently change sign.

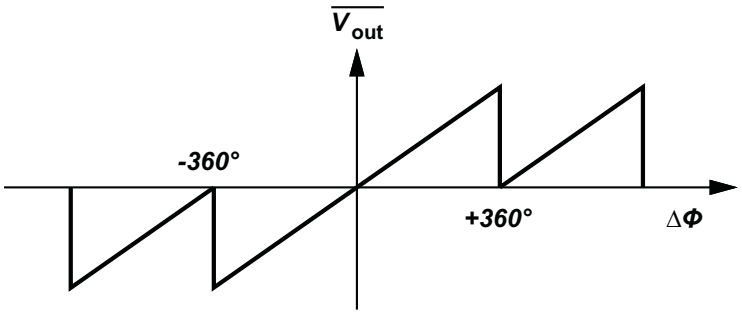


Figure 5.4 Transfer curve of a PFD

5.5 Charge Pump

The charge pump has been widely used in PLL and DLL applications. Fig.5.5 shows the conceptual diagram of a charge pump. The V_{up}/V_{dn} signals generated by the PFD are used to time-multiplex the currents from the current sources, I_{up} and I_{dn}, into the output node. Assuming that $I_{up}= I_{dn}= I_{cp}$, and the V_{up}/V_{dn} pulse shapes and switched are ideal, the pulse width difference between the V_{up} and V_{dn} signals indicate that the charges is deposited or withdrawn at the output node. The charge pump is a tri-state device that gives an output current of I_{up}, $-I_{dn}$, and zero, depending on the control signals from the PFD. However, the charge pump is usually connected to a loop filter, which coverts the charge pump output current to the VCDL control voltage, the problems of charge injection and clock feedthrough from the two switches may seriously degrade the noise performance of the DLL. Because of 200MHz reference frequency, a differential charge pump [18] is realized for the high-speed operation, as shown in Fig.5.6. The pseudo-differential V_{up}/V_{dn} control signals are produced by PFD. Effect of charge sharing and charge injection are removed by the unity-gain feedback amplifier in the charge pump, and the static phase error is reduced consequently.

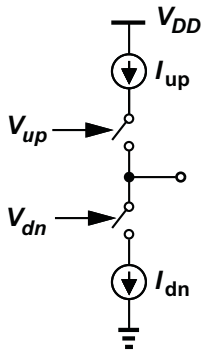


Figure 5.5 The conceptual diagram of a charge pump.

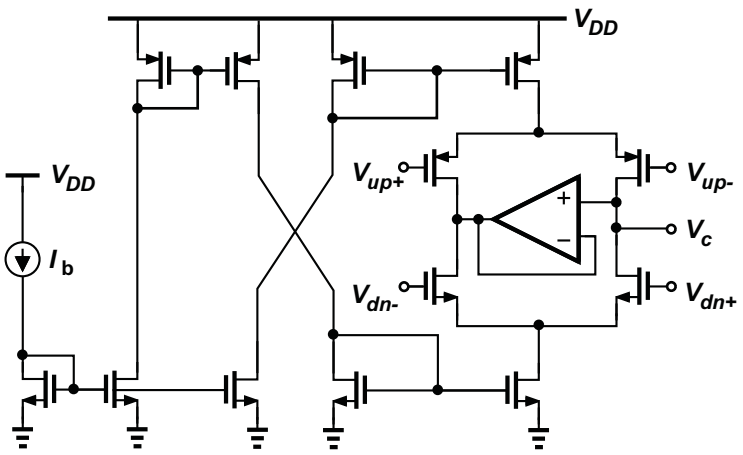


Figure 5.6 Differential charge pump.

5.6 Divider

Fig. is a divide-by-two circuit based on the true single-phase clocking (TSPC) scheme [24], achieving a high speed. The divide-by-eight circuit adopted in the MDLL is implemented by cascading three stages in an asynchronous configuration.

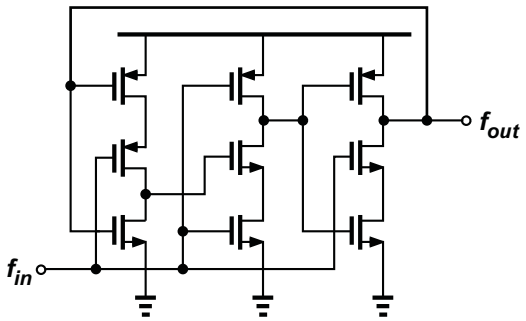


Figure 5.7 TSPC divide-by-two circuit.

5.7 Control Logic

In Fig.5.8, the circuit in the dash box is the conventional control logic for MDLL [17]. Based on this control logic, the MDLL must be started at its maximum startup control voltage to ensure the correct multiplexing function. The additional circuits are designed for the control logic to make sure that the MDLL can start up at any initial condition. Fig.5.9 shows the conceptual operation mechanism of the modified control logic.

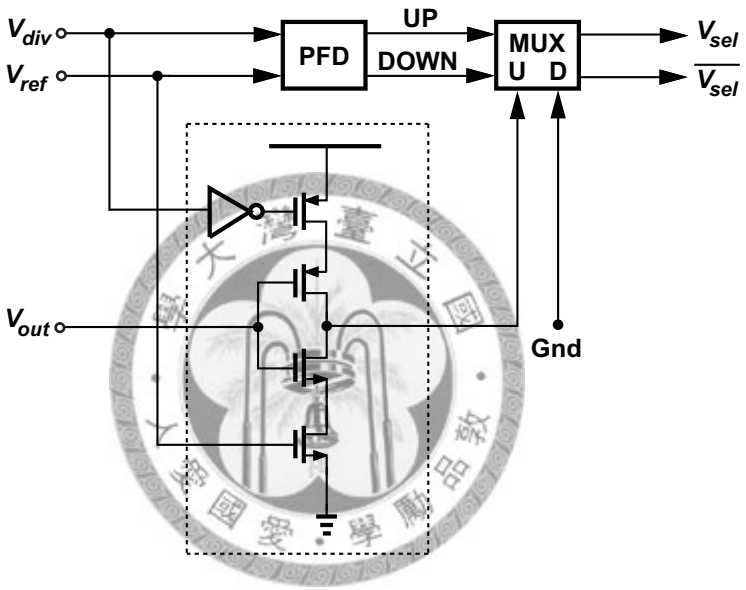


Figure 5.8 Modified control logic for MDLL.

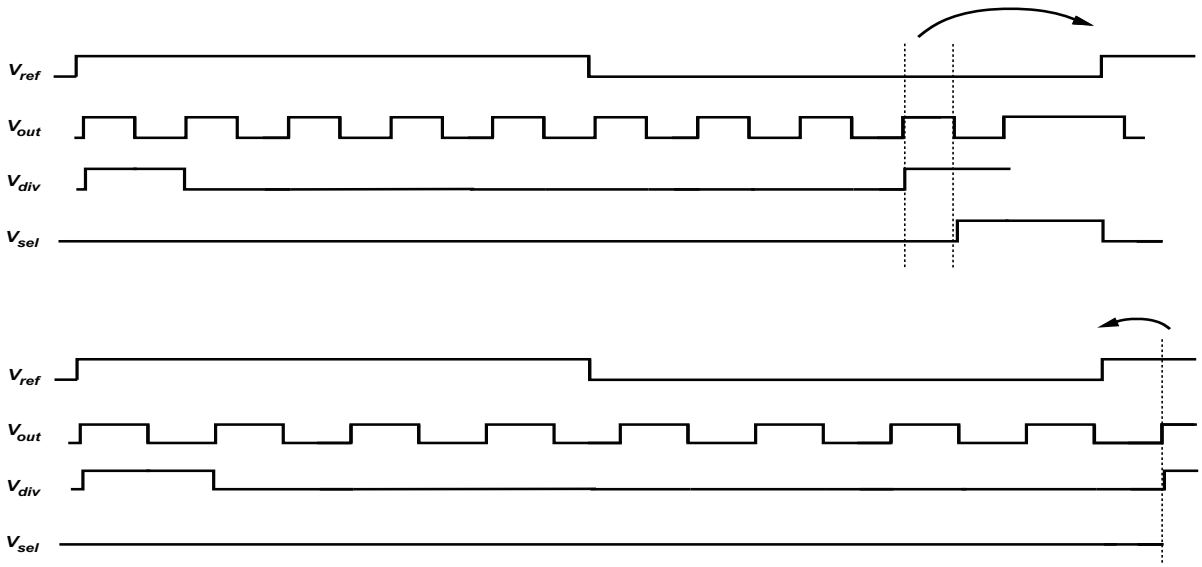


Figure 5.9 The operation mechanism of the control logic.

A PFD is used to detect whether the divide down signal is faster than the reference clock or not. If the V_{div} is faster than V_{ref}, that is, the control voltage is higher than its locked value, the PFD will output a up pulse. Then the multiplexer will pass the select signal which is generated from the conventional control logic. On the other hand, if the V_{ref} is faster than V_{div}, the PFD will output a down pulse which makes the multiplexer pass 0. When the select signal is 0, the multiplexer closes up the delay line and keeps it works as an oscillator. Under this condition, the entire system works like a PLL and the loop filter is charged by the charge pump periodically. As the control voltage exceeds its locked value, this means V_{div} is going to be faster than V_{ref}, the multiplexer will pass the signal from the conventional logic again and the system is back to the MDLL operation type.

5.8 Arbiter

Just as an ADC requires a latching comparator, so does a TDC. Either a flip-flop or an arbiter can be used as a comparator of which output determines the output codes of the TDC. Fig.5.10 shows a sense-amplifier-based flip-flops which is similar to a comparator used in a ADC. The flip-flops are symmetrical along the vertical axis and provide identical resolution of the rising and falling edge metastability of their input data. The loading of data input node is only a NMOS gate and their interconnect parasitic capacitance. The metastability window is reported [25] to be very small which is less than 1ps. This ensures no bubble error in the TDC. It should be noted that a typical flip-flops for high speed digital designs features nonsymmetrical metastability characteristic and the composite resolution window exceeds several inverter delays which sets the limitation of the TDC resolution. Although the mismatch in the data and clock propagation path is possible to results in a large time offset, the asynchronous DLL-interpolation architecture will cancel

the offset in the post processing unit.

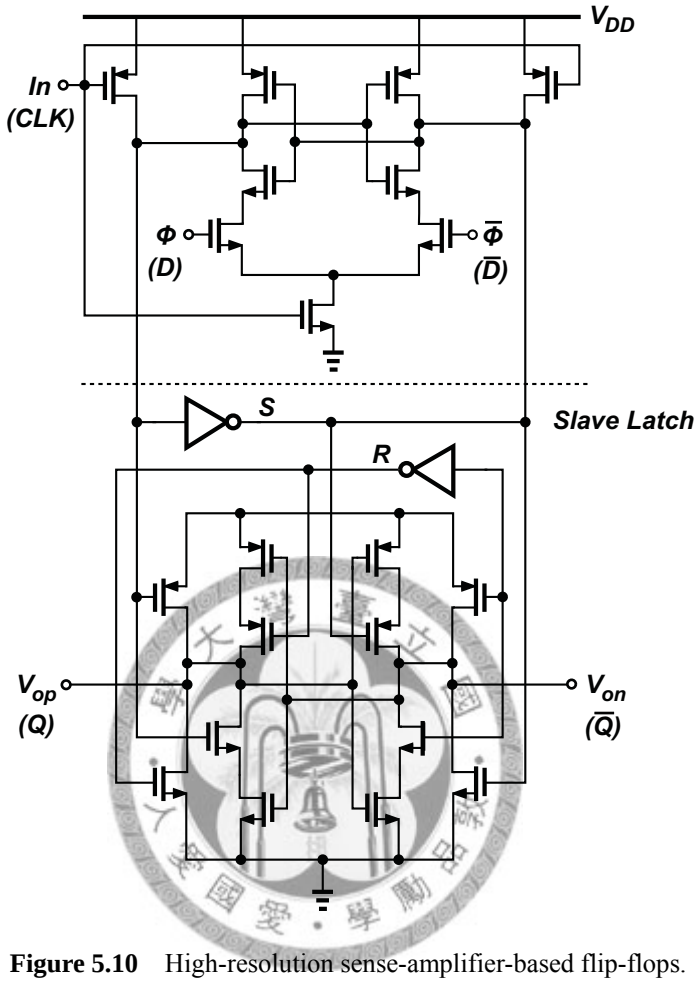


Figure 5.10 High-resolution sense-amplifier-based flip-flops.

5.9 Encoder

Fig.5.11 shows the schematic of the digital encoder where a one-of-n encoder is followed by a ROM. The pseudo-thermometer code generated from the arbiter array is first converted to one-of-n code by three-input AND gates which perform a first-order bubble error correction. At the output of the one-of-n encoder, only one of the word lines is at high voltage and pulls down the pre-charged bit lines where NMOS transistors are located.

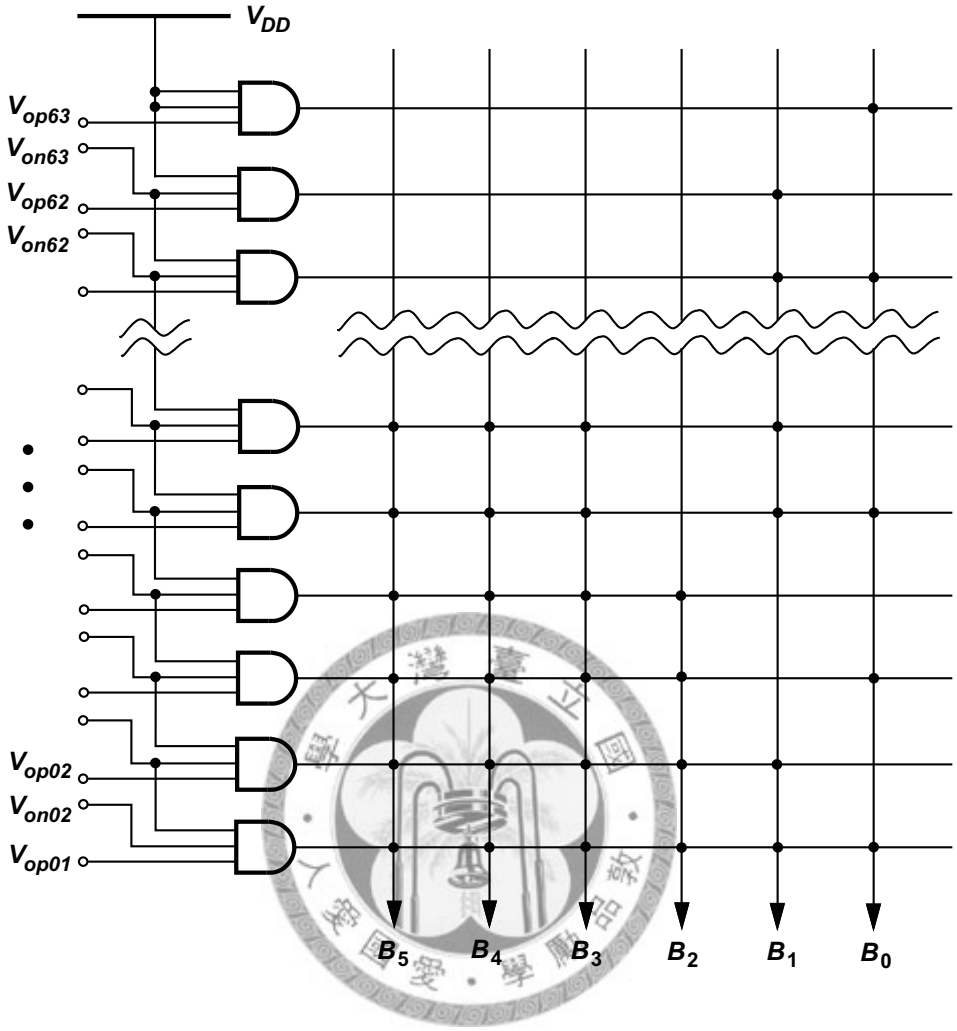


Figure 5.11 The architecture of digital encoder.

5.10 Output Buffers

5.10.1 Digital Output Buffer

In the whole chip simulation, the effects of pad, bond wire, and the probe are considered. Fig. 5.12 (a) shows the schematic of the effects. To enhance the driving capability, the output buffer is built as shown in Fig. 5.12 (b).

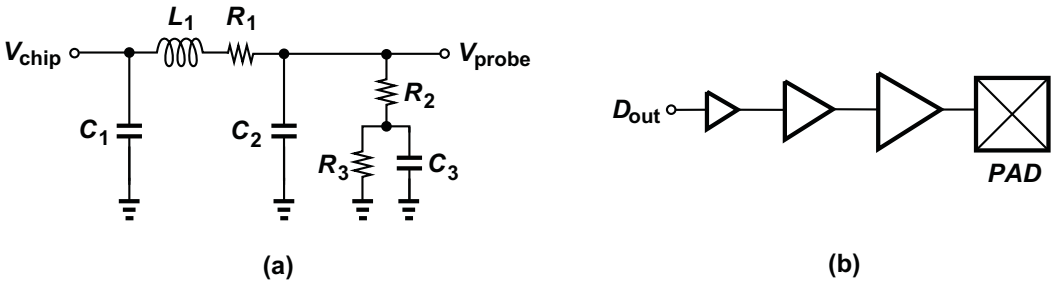


Figure 5.12 (a) The simulated effects about the pad, bonding wire and the probe. (b) The output buffer.

5.10.2 Open-Drain Output Buffer

To observe the multiplied output clock, a open-drain buffer is used and the detail schematic include buffer, pad, bond wire, and bias-tee is shown as Fig. 5.13. The size of open-drain buffer is choose based on the simulation of bond wire effect and driving capability.

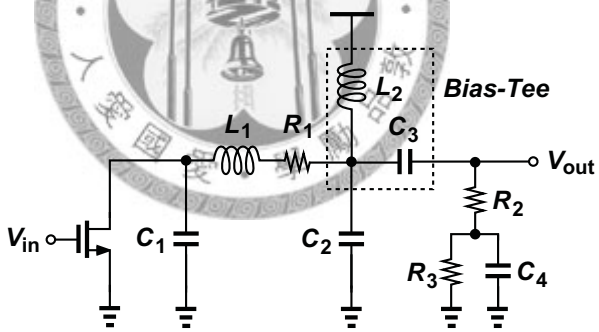


Figure 5.13 The open-drain buffer and the proceeding connection configuration.

5.11 Transistor-Level Simulation

After completing the design of building blocks respectively, the whole system of a MDLL-based TDC with local passive interpolation is constructed. We choose the logic-mode transistor model to perform the transistor level simulation. After the layout of the prototype is completed, it is believed that post-layout simulation is more close to the

performance of real circuit because of the parasitic capacitance is extracted. The transient waveform of reference clock and multiplied output clock before and after locking are shown in Fig.5.14 and Fig.5.15.

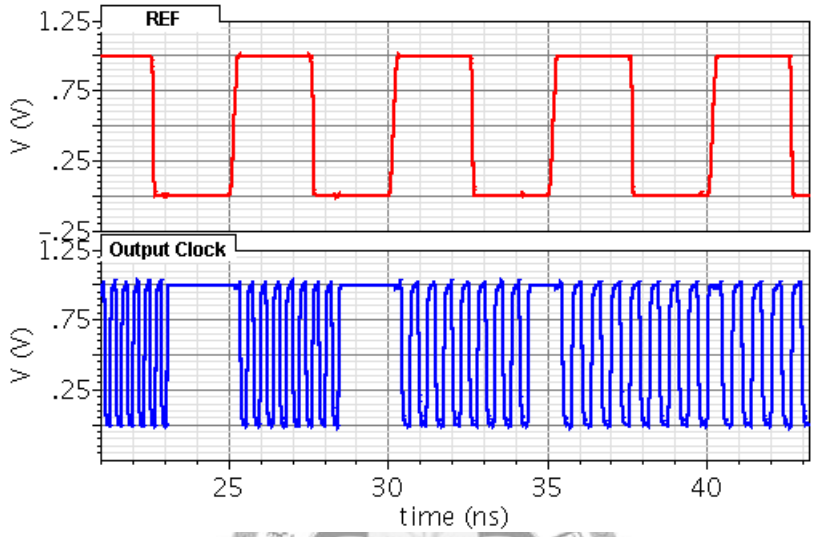


Figure 5.14 The transient waveform of reference and output clock before locking.

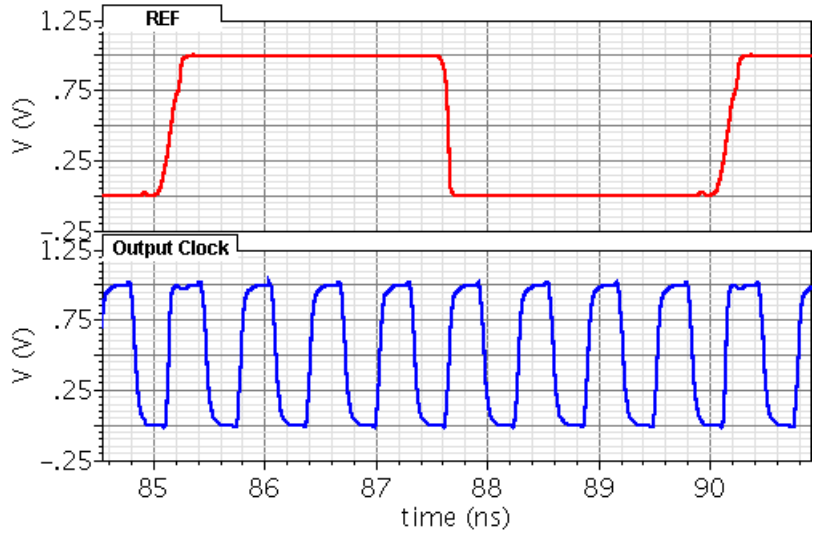


Figure 5.15 The transient waveform of reference and output clock when locking.

Fig.5.16 shows the setting behavior of the control voltage. As illustrated, the MDLL is locked at a low initial startup voltage.

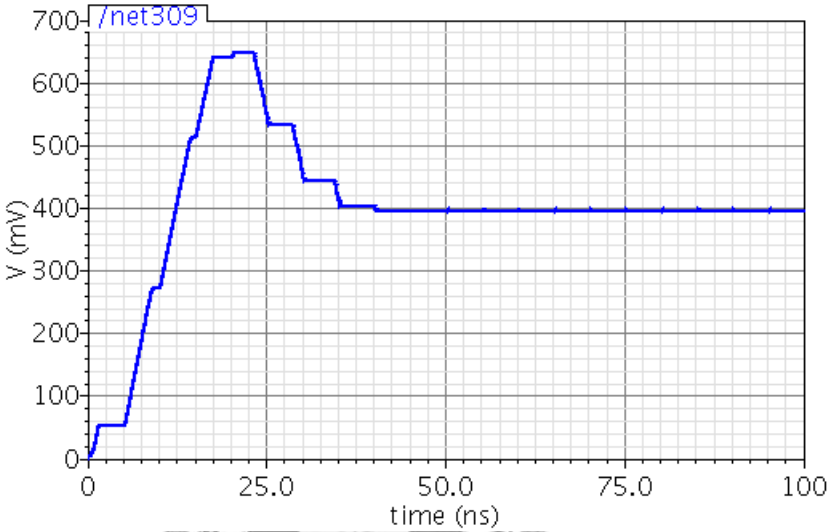


Figure 5.16 The settling behavior of control voltage.

Fig.5.17 shows the local passive interpolation result. The delay is locked at 35ps which is lower than the design goal 40ps. This is because there is excess delay along the path, i.e. the delay of the multiplexer.

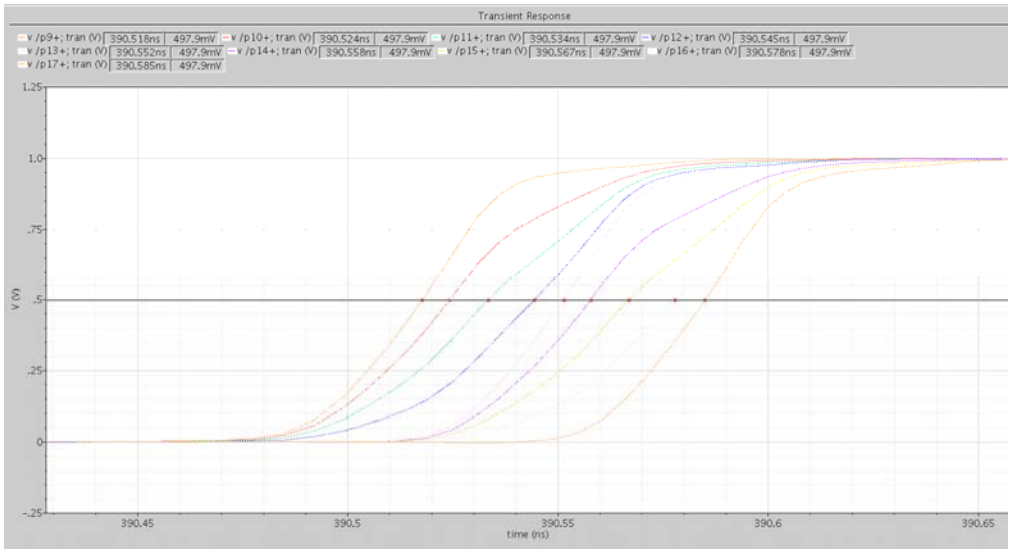


Figure 5.17 The timing diagram of local passive interpolation

Fig. 5.18 shows the input/output characteristic of the proposed TDC. 80-point ramp input each spacing 64ps is applied. The plot shows that the TDC is suffered from a constant offset because the finite rising and falling time of the input measured pulse and a constant gate delay.

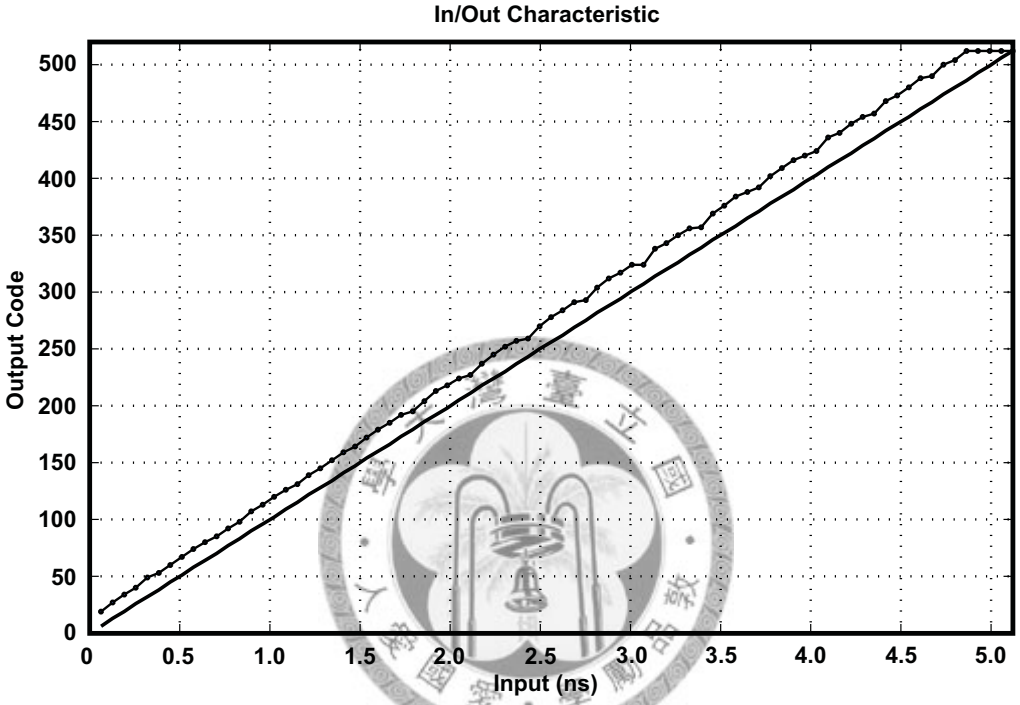


Figure 5.18 The input/output characteristic of TDC

As illustrated in Fig. 5.19 (a), the finite rising and falling time will contribute about 100ps constant offset to the measured pulse. Another cause of the offset error is shown in Fig. 5.19 (b). The stop pulse is generated from passing the start pulse through an inverter, and therefore a constant gate delay is translated to an offset between the start and the stop pulse.

Figure 5.19 Causes of offset error (a) finite rising and falling time and (b) gate delay.

5.11 Layout and Performance Summary

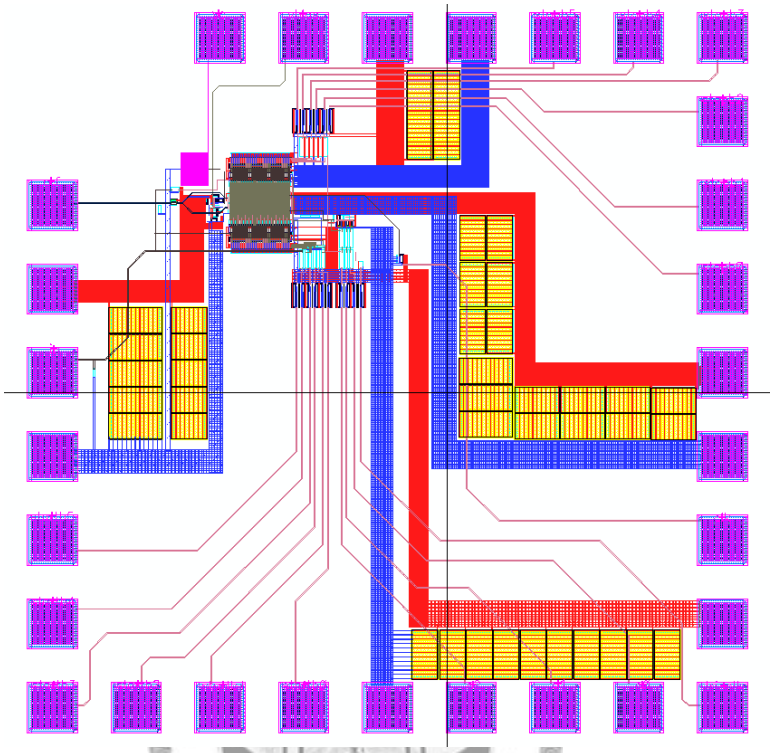


Figure 5.20 Layout of the MDLL-based TDC.

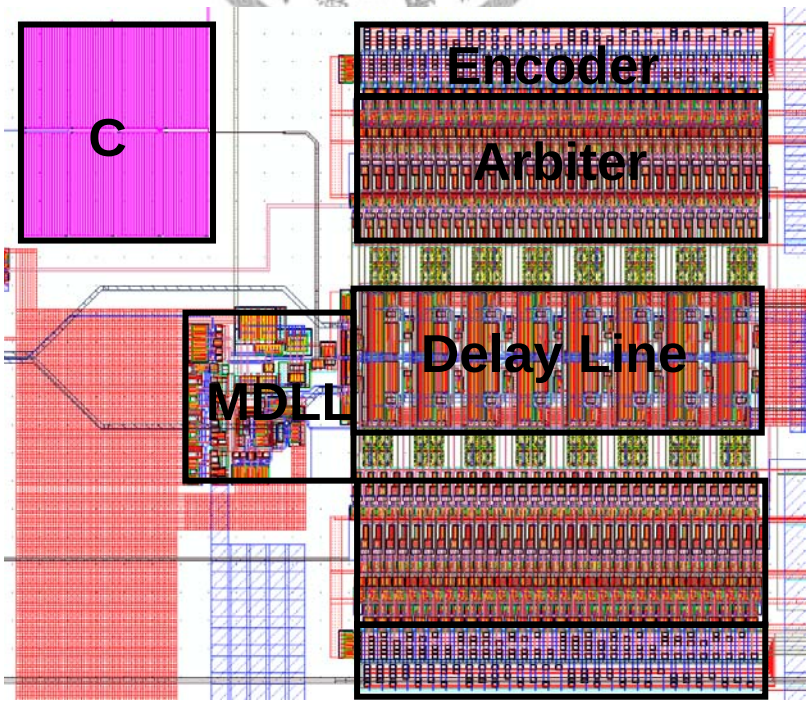


Figure 5.21 The core layout of the MDLL-based TDC

Fig.5.20 and Fig.5.21 illustrated the layout and the core of TDC fabricated in TSMC 90-nm technology and the area is 960μm×960μm with 29 PADs. The core is aside the control line PAD in order to guarantee the sensitive line as short as possible. Four power supplies are provided, for analog circuits, digital circuits, delay cells, and output buffers. Bypass capacitors are added between the DC voltage and ground to reduce noise. Fig. shows the core of the TDC. The analog part contains the PFD, charge pump, loop filter, control logic, divider, and delay line. The digital part contains the arbiter, counter, and output buffers. Though the core area of the TDC is fairly small, the need of I/O PAD leads the whole circuits occupying large area.

The performance summary and the comparison between this work and other recent TDCs are shown in Table 5.1.

Table 5.1 The performance summary and the comparison table.

COMPARISON OF RECENTLY REPORTED TDC PERFORMANCES

Architecture	Tech. [um]	LSB [ps]	Power [mW]	Area [mm^2]	DNL [LSB]	INL [LSB]
Delay line [15]	90	20	NA	0.01	0.6	0.7
Loc. passive interpol. [13]	90	4.7	NA	0.02	0.6	1.2
Counter & Delay line [26]	250	24.4	45	NA	0.49	3.0
Pulse Shrinking [14]	350	68	1.2	0.03	NA	NA
This work	90	10	6.0	0.017	0.6	0.9

Chapter 6

Test and Experimental Results

6.1 Introduction

In this chapter, Die photo is proposed at first. Then the MDLL-based TDC measurement equipment is introduced, and the print circuit board (PCB) is designed and set up for testing. Finally, the experimental results are analyzed and summarized.

6.2 Chip Die Photo

The MDLL-based TDC has been fabricated in 90-nm CMOS technology. The die photo of the designed TDC is illustrated in Fig. 6.1. The whole chip is filled with dummy metal cells except for the core because of design rule of metal density. The design is a pad-dominated layout and the whole chip occupies an area of $0.96 \times 0.96\ mm^2$.

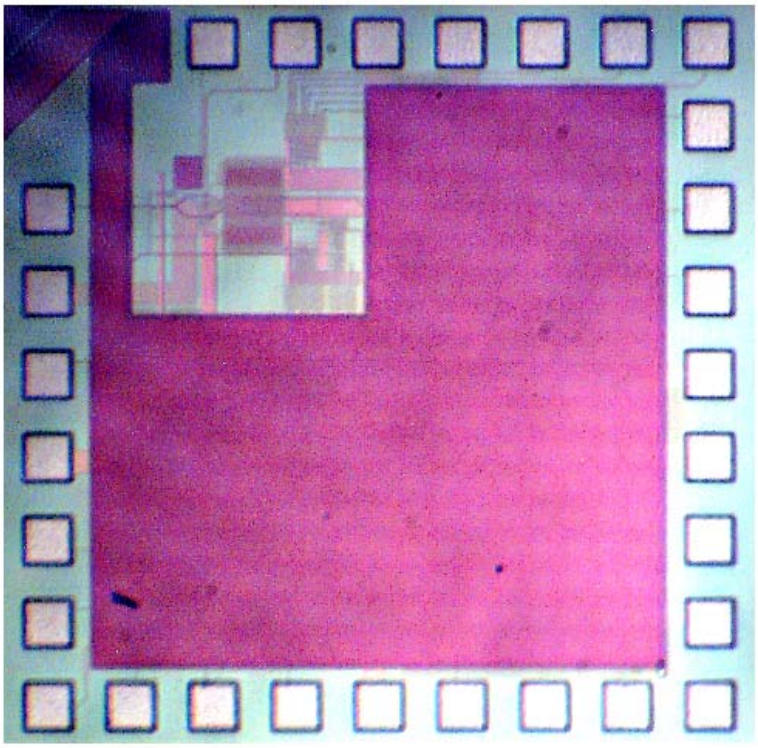


Figure 6.1 The die photo of the designed TDC.

6.3 Test Strategy

6.3.1 Test Setup

Fig. 6.2 shows the test setup and the photos of instruments for the TDC. The DC voltages are provided by Agilent E3646A and the reference clock is generated by R&S SMB 100A with bias-T. Agilent E4408B is used to analyze the MDLL output spectrum. As for the testing of TDC, the input pulse is generated by Tektronix AFG-3252 and TLA 5203 logic analyzer acquires the output codes.

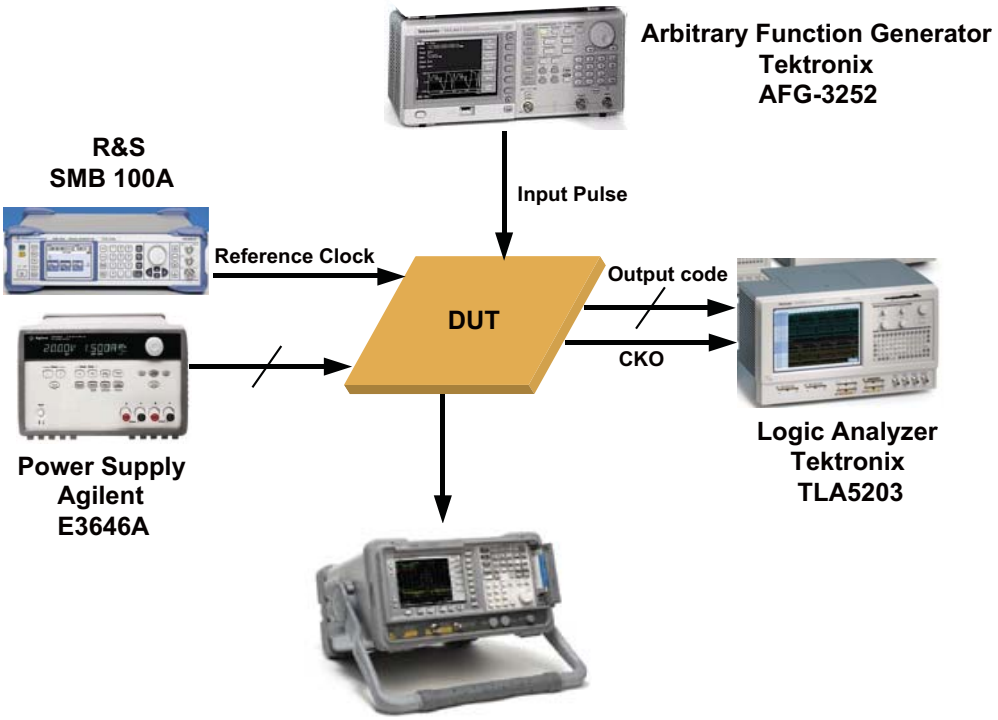


Figure 6.2 Test setup and equipments.

6.3.2 Print Circuit Board Design

The print circuit board is very important as the integrated circuit. Fig.6.3 shows the photograph of PC board. The whole system is powered by four independent supply voltages. In order to prevent the digital noise coupling to the analog circuits, tune the delay line individually, and estimate the power consumption of the output buffers, the PC board is taken as four parts. The power line of four parts are separated and isolated. Fig.6.4 shows the pin configurations of the prototype.

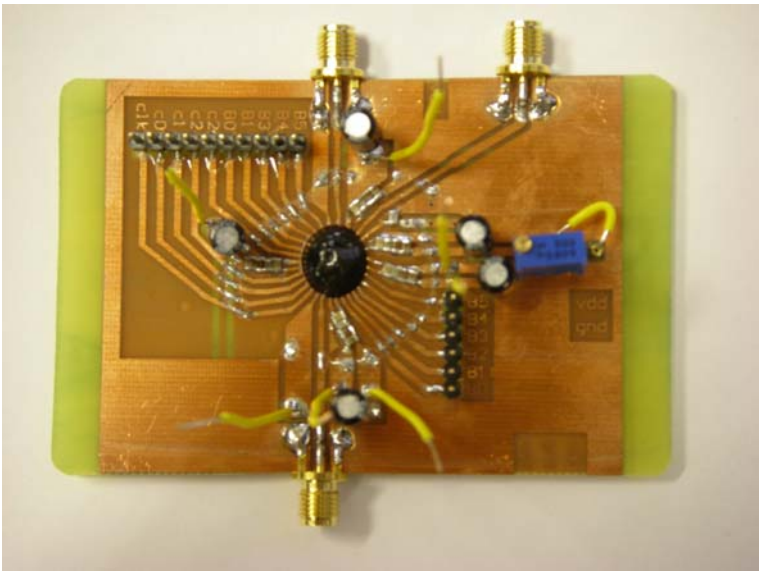


Figure 6.3 The photograph of PCB.

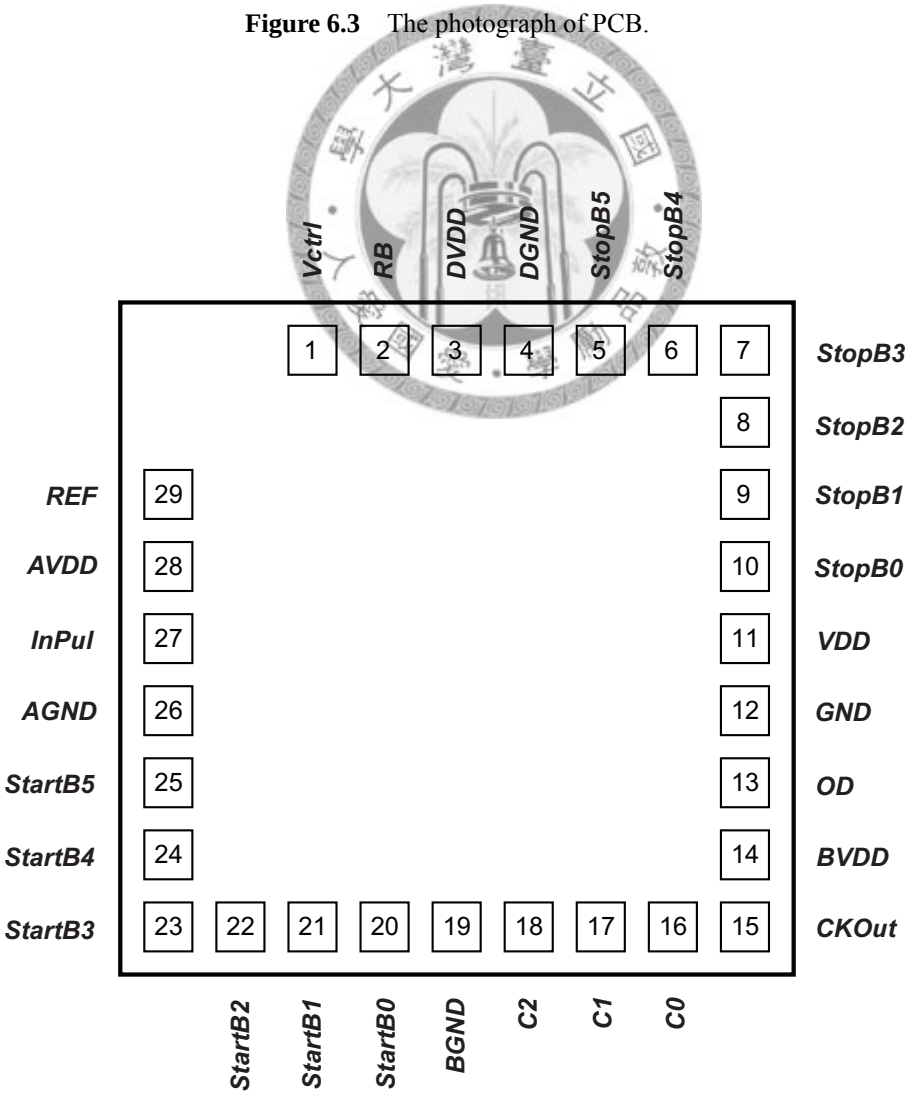


Figure 6.4 (a) The pin configurations of the TDC.

Pin	Name	I/O	Description
1	Vctrl	Out	Control line voltage
2	RB	In	Bias resistor
3	DVDD	In	Digital power
4	DGND	In	Digital ground
5	StopB5	Out	Digital output
6	StopB4	Out	Digital output
7	StopB3	Out	Digital output
8	StopB2	Out	Digital output
9	StopB1	Out	Digital output
10	StopB0	Out	Digital output
11	VDD	In	Delay line power
12	GND	In	Delay line ground
13	OD	Out	Open drain output
14	BVDD	In	Buffer power
15	CKOut	Out	Output clock
16	C0	Out	Digital output
17	C1	Out	Digital output
18	C2	Out	Digital output
19	BGND	In	Buffer ground
20	StartB0	Out	Digital output
21	StartB1	Out	Digital output
22	StartB2	Out	Digital output
23	StartB3	Out	Digital output
24	StartB4	Out	Digital output
25	StartB5	Out	Digital output
26	AGND	In	Analog ground
27	InPul	In	Input pulse
28	AVDD	In	Analog power
29	REF	In	Reference clock

Figure 6.4 (b) The description of pin configurations.

6.4 Experimental Results

The MDLL is provided with an external 200MHz reference clock and the output clock is going to be multiplied to 1.6GHz as designed. Fig.6.5 illustrated the output clock spectrum. The experimental result shows that the multiplied clock is locked at 1.6GHz with -5dBm power level.

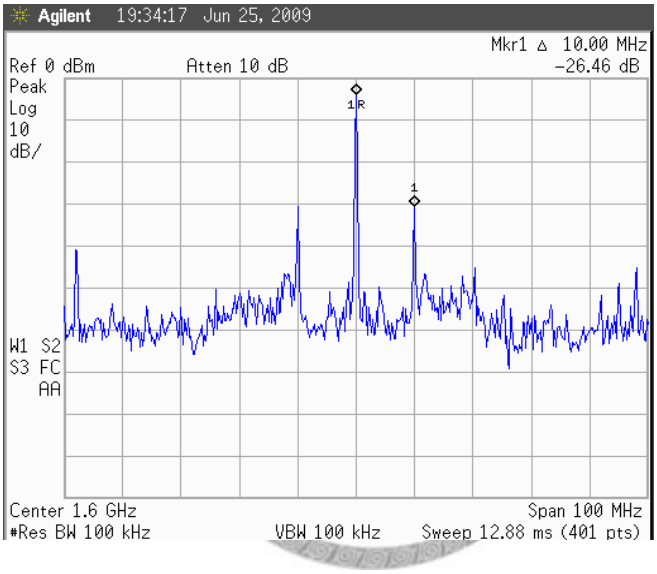


Figure 6.5 Output clock spectrum.

Chapter 7
Conclusions

7.1 Conclusions

The impact on performance of Nyquist-rate analog-to-digital converters (ADCs) with the presence of sampling clock jitter is first reviewed. Then the sampling clock jitter requirement is investigated based on the linearly approximated sampling model as well as the generic autocorrelation function approach. This leads to the motivation for cancelling the jitter-induced error in the digital domain. Two key points are desired in this method—acquisition of jitter quantities and signal derivative estimation. With the cancellation mechanism, the performance of a Nyquist ADC is improved to extend the performance at high-frequency input. In the other words, the stringent jitter requirement is alleviated.

A high-resolution and wide dynamic range time-to-digital converter (TDC) with short conversion time is an essential building block in the proposed architecture. The TDC in the system digitized the jitter quantities in order to perform the cancellation in the digital domain. A 10ps MDLL-based TDC is designed to meet the system specifications. A complete circuit design scheme of this work is presented in chapter4. From high-level architecture to building blocks implementations, both design considerations and simulation results are included in chapter 4. Fabricated in a 90-nm CMOS technology, the TDC

consumes 6.0mW from a 1-V power supply while the active area is only 0.017mm^2.

Bibliography

[1] Behzad Razavi, *Principles of Data Conversion System Design*. 1st Ed., Wiley-Interscience, 1995.

[2] B.-G. Lee, B.-M. Min, Gabriele Manganaro, and J. W. Valvano , "A 14-b 100-MS/s Pipelined ADC With a Merged SHA and First MDAC," *IEEE J. of Solid-State Circuits*, Vol. 43, pp. 2613-2619, Dec., 2008.

[3] Brad Brannon, "Aperture uncertainty and ADC system performance," AN-501 Application Note, Analog Device.

[4] N. D. Dalt, M. Harteneck, C. Sander, and Wiesbauer, "On the jitter requirements of the sampling clock for analog-to-digital converters," *IEEE Trans. Circuits and Syst. I:Fundmental Theory and Applications,* vol.49, no.9, pp. 1354-1360, Sep. 2002.

[5] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter analysis of high-speed sampling systems," *IEEE J. Solid-State Circuits,* vol. 25, pp. 220-224, Feb. 1990.

[6] U. K. Moon, Karti Mayaram, and John T. Stonick, "Spectral analysis of time-domain phase jitter measurements," *IEEE Trans. Circuits and Syst. II,* vol.49, no.5, pp. 321-327, May. 2002.

[7] F. Herzel and B. Razavi, "A study of oscillator jitter due to supply and substrate noise," *IEEE Trans. Circuits and Syst. II,* vol.46, no.31, pp. 56-62, Jan. 1999.

[8] Tian Xia and J.-C. Lo, "Time-to-Voltage Converter for On-Chip Jitter Measurement," *IEEE Trans. Instrumentation and Measurement,* vol.52, no.6, pp. 1738-1748, Dec. 2003.

[9] E. Raisanen-Ruotsalainen, T. Rahkonen, and J. Kostamovaara, "A High Resolution Time-to-Digital Converters Based on Time-to-Voltage Interpolation," in *Proc. 23rd European Solid-State Circuits Conf. (ESSCIRC)*,pp. 332-335, 1997.

[10] T. E. Rahkonen and J. T. Kostamovaara, "The Use of Stabilized CMOS Delay Lines for the Digitization of Short Time Intervals," *IEEE J. of Solid-State Circuits*, Vol. 28, pp. 887-894, Aug., 1993.

[11] V. Ramakrishnan and P. T. Balsara, "A Wide-Range, High Resolution, Compact, CMOS Time to Digital Converter," in *Proc. 19th Int. Conf. VLSI Design (VLSID'06)*, Jan., 2006.

[12] P. Dudek, S. Szczepanski, and J. Hatfield, "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line," *IEEE J. of Solid-State Circuits*, Vol. 35, pp. 240-247, Feb., 2000.

[13] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "A Local Passive Time Interpolation Concept for Variation-Tolerant High-Resolution Time-to-Digital Conversion, " *IEEE J. Solid-State Circuits,* vol. 43, pp. 1666-1676, July 2008.

[14] Poki Chen, S.-I. Liu, and Jingshown Wu, "A CMOS Pulse-Shrinking Delay Element for Time Interval Measurement," *IEEE Trans. Circuits and Syst. II,* vol.47, pp. 954-958, Sep. 2000.

[15] J.-P. Jansson, A. Mäntyniemi, and J. Kostamovaara, "A CMOS Time-to-Digital Converter with Better than 10ps Single-Shot Precision, " *IEEE J. Solid-State Circuits,* vol. 41, pp. 1286-1296, June 2006.

[16] J. van Valburg and R. J. van de Plassche, "An 8-b 650-MHz Folding ADC," *IEEE J. Solid-State Circuits,* vol. 27, pp. 1662-1666, Dec. 1992.

[17] R. Farjad-Rad , W. Dally , H.-T. Ng , R. Senthinathan , M.-J. E. Lee , R. Rathi and J. Poulton, "A Low-Power Multiplying DLL for Low-Jitter Multigigahertz Clock Generation in Highly Integrated Digital Chips, " *IEEE J. Solid-State Circuits*, vol. 37, pp. 1804-1812, Dec. 2002.

[18] Keng-Jan Hsiao, "A DLL-Based Frequency Multiplier for MBOA-UWB System," *Master thesis*, National Taiwan University, Taipei, Taiwan, R.O.C., July, 2005.

[19] J.-M. Chou, Y.-T. Hsieh, and J.-T. Wu, "Phase Averaging and Interpolation Using Resistor Strings or Resistor Rings for Multi-Phase Clock Generation," *IEEE Trans. Circuits and Syst. I,* vol.53, pp. 984-991, May. 2006.

[20] H. Pan and A. A. Abidi "Spatial Filtering in Flash A/D Converters," *IEEE Trans. Circuits and Syst. II,* vol.50, pp. 424-436, Aug. 2003.

[21] A. A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillators, " *IEEE J. Solid-State Circuits*, vol. 41, pp. 1803-1816, Aug. 2006.

[22] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*. 1st Ed., McGraw-Hill, 2001.

[23] S. Kim, K. Lee, Y. Moon, D.-K. Jeong, and H. K. Lim, "A 960-Mb/s/pin Interface for Skew-Tolerant Bus Using Low Jitter PLL, " *IEEE J. Solid-State Circuits*, vol. 32, pp. 691-700, May 1997.

[24] Behzad Razavi, *RF Microelectronics*, Prentice Hall, 1997.

[25] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. T. Balsara, "1.3V 20ps Time-to-Digital Converter for Frequency Synthesis in 90-nm CMOS," *IEEE Trans. Circuits and Syst. II,* vol.53, pp. 220-224, Mar. 2006.

[26] C.-S. Hwang, Poki Chen, and H.-W. Tsao, "A High-Precision Time-to-Digital Converter Using a Two-Level Conversion Scheme," *IEEE Trans. Nuclear Science,* vol.51, pp. 1349-1352, Aug. 2004.


國立臺灣大學
教育學程・愛國愛人