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碩士論文

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College of Electrical Engineering & Computer Science
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Master Thesis

高層數堆疊鍺矽通道奈米片及奈米線電晶體之製程整合

Process Integration of Highly Stacked GeSi Nanosheets and Nanowires FETs

闕世杰

Shee-Jier Chueh

指導教授：劉致為 博士

Advisor: Chee Wee Liu, Ph.D.

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奈米片及奈米線電晶體之製程整合

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本論文係 闕世杰(學號:R10943065) 在國立臺灣大學電子工程學研究所完成之碩士學位論文，於民國 112 年 7 月 16 日承下列考試委員審查通過及口試及格，特此證明。

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IEDMS Best Student Paper Award

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2022 IEDMS Best Paper Award

Shee-Jier Chueh, Yi-Chun Liu, Chun-Yi Cheng, Bo-Wei Huang, Chien-Te Tu, and C. W. Liu, "Highly Stacked $Ge_{0.75}Si_{0.25}$ Nanosheet nFETs" 2022 International Electron Devices and Materials Symposium (IEDMS), Nantou, Taiwan, Oct. 27-28, 2022.

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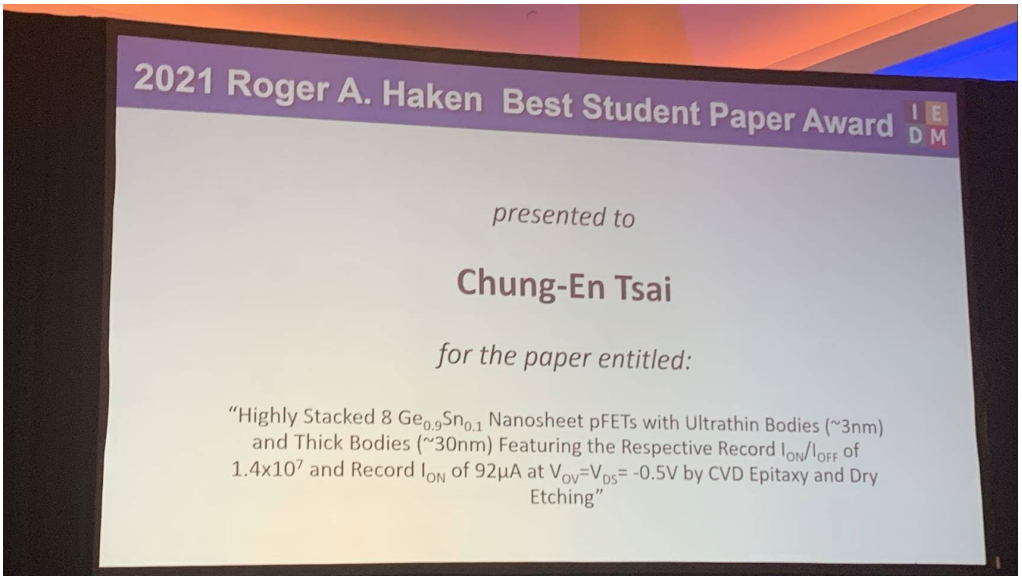
Roger A. Haken Best Student Paper Award

Roger A. Haken Best Student Paper Award

The Roger A. Haken Best Student Paper Award is awarded each year to the best student paper presented at IEDM, and is given at the IEDM conference in the following year. The award was created in memory of Roger A. Haken who served on the IEEE IEDM Executive Committee for several years including as technical program vice chair in 1990 when he passed away in June of that year.

Roger Haken was a Texas Instruments Senior Fellow & Research Manager of Submicron CMOS/BiCMOS at the TI Semiconductor Process and Design Center. He invented the use of both Phosphorus and Arsenic as doping in NMOSFET to improve junction breakdown and to reduce hot carrier generation. His work on self-aligned silicide led to the use of Titanium Nitride formed concurrently during self-aligned silicidation as local interconnect, published in IEDM 1985. He led the development of an 8ns 256KSRAM in 0.8μm technology utilizing a CMOS array and ECL IO, reported in IEDM 1987. Subsequently, in IEDM 1989, his team reported a 5ns 4Mb SRAM in 0.5μm CMOS/BiCMOS technology.

Before joining Texas Instruments, he was with the General Electric Company at the Hurst research Center, London. He received the Higher National Diploma in electrical and electronic engineering from Southampton College of Technology, Hampshire, England, in 1971 and the MS and PhD degrees in electronics from the University of Southampton in 1972 and in 1975, respectively. He held 43 patents and was author or co-author of over 30 technical publications.



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2021 IEDM Roger A Haken Best Student Paper Award, (the first winner from Taiwan) Chung En Tsai, Yi Chun Liu, Chien Te Tu, Bo Wei Huang, Sun Rong Jan, Yu Rui Chen, Jyun Yan Chen, **Shee Jier Chueh**, Chun Yi Cheng, Chia Jung Tsen Yichen Ma, and C W Liu,Liu, "Highly Stacked 8 $Ge_{0.9}Sn_{0.1}$ Nanosheet pFETs with Ultrathin Bodies 3 nm and Thick Bodies 30 nm Featuring the Respective Record I_{ON} /I_{OFF} of 1.4E7 and Record I_{ON} of 92 μA at V_{OV} =V_{DS} 0.5 V by CVD Epitaxy and Dry Etching," pp 569 572 International Electron Devices Meeting (2021)

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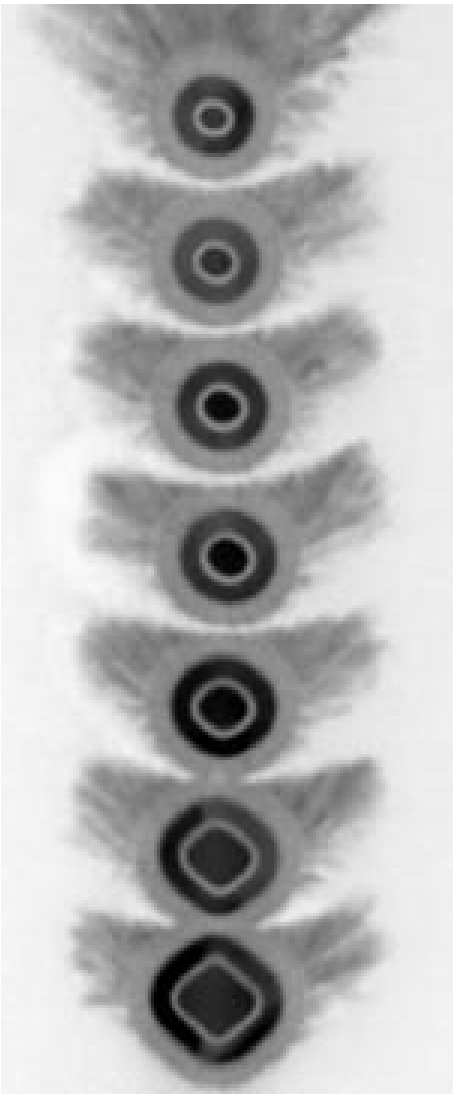
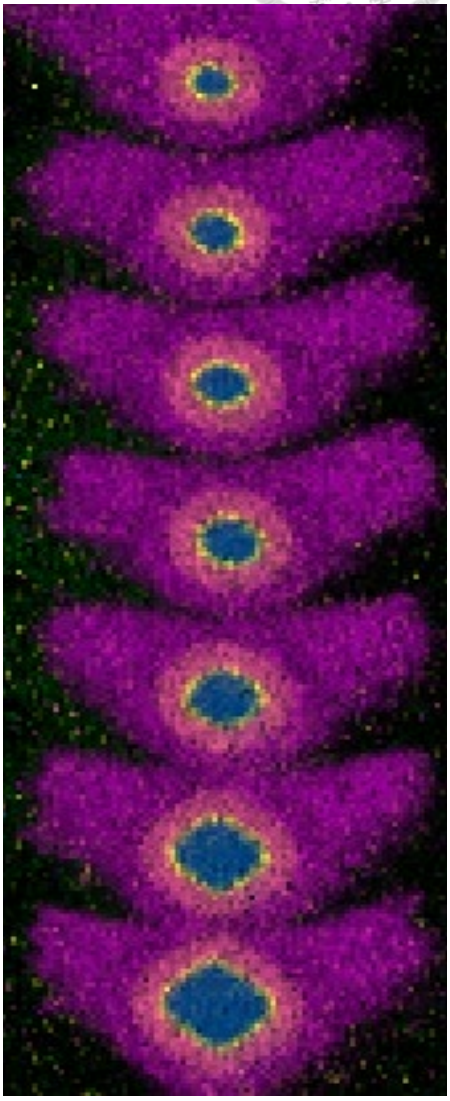
NTU Transistors Highlighted by VLSI and Nature Electronics in 2021





nature electronics

Reference:

i. **(Highlight paper)** Yi-Chun Liu, Chien-Te Tu, Chung-En Tsai, Yu-Rui Chen, Jyun-Yan Chen, Sun-Rong Jan, Bo-Wei Huang, **Shee-Jier Chueh**, Chia-Jung Tsen, and C. W. Liu, "First Highly Stacked $Ge_{0.95}Si_{0.05}$ nGAAFETs with Record I_{ON} = 110 μA (4100 μA/μm) at V_{OV}=V_{DS}=0.5V and High $G_{m,max}$ = 340 μS (13000 μS/μm) at V_{DS}=0.5V by Wet Etching," in ***Symp. VLSI Technol.***, June 2021, pp. T15-2.

ii. Thomas S., "Germanium nanowire transistors stack up," ***Nature Electronics***, Vol 4, No. 7, pp. 452, July 2021.

doi:10.6342/NTU202301581

VLSI-TSA Best Student Award

Contact

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TSA Best Student Paper Award

In 2005, the Symposium started the Best Student Paper Award annual contest. The selection will be based on the paper quality evaluated by technical committee members, as well as the presentation of the paper at the symposium. The paper should be presented by the key author who is a full-time student at the time of paper presentation. The Best Student Paper Award will be presented to the winning student at the next year's symposium.

2022 TSA Best Student Paper Award Winners ~ ***Congratulations!***

The 2022 TSA Best Student Paper Award will be presented at 2023 International VLSI Symposium on Technology, Systems and Applications opening ceremony and each winner will be rewarded by a certificate and US$500. Besides, the Symposium will also offer the winners the waiver of registration fee to attend the 2023 International VLSI Symposium on Technology, Systems and Applications.

• **6 Stacked $Ge_{0.95}Si_{0.05}$ nGAAFETs without Parasitic Channels by Wet Etching**
Chun-Yi Cheng, Wan-Hsuan Hsieh, Bo-Wei Huang, Yi-Chun Liu, Chien-Te Tu, Chung-En Tsai, Shee-Jier Chueh, Guan-Hua Chen, and C. W. Liu
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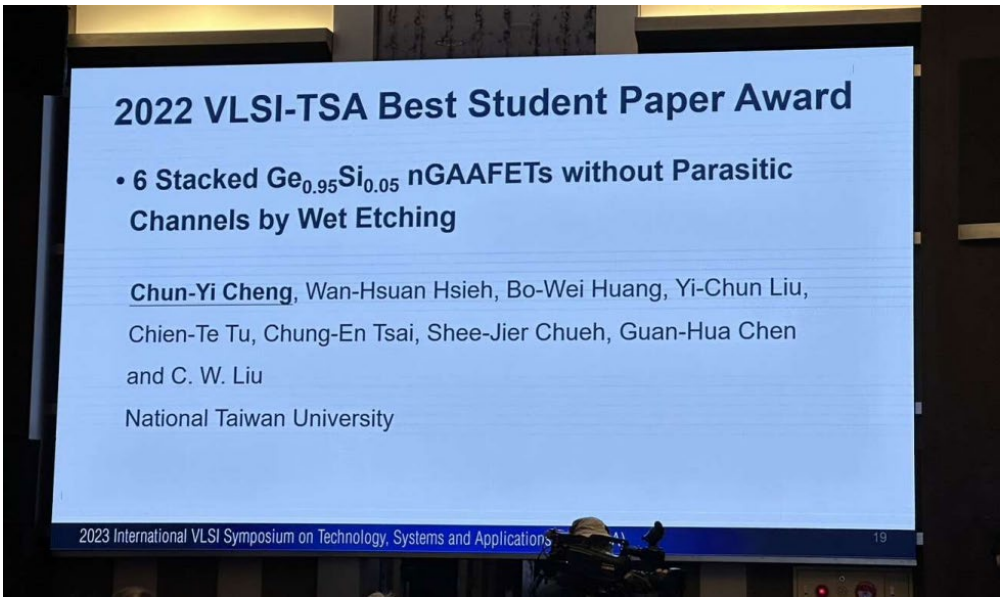

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2022 VLSI-TSA Best Student Award
Chun-Yi Cheng, Wan-Hsuan Hsieh, Bo-Wei Huang, Yi-Chun Liu, Chien-Te Tu, Chung-En Tsai, **Shee-Jier Chueh**, Guan-Hua Chen, and C. W. Liu, "6 Stacked $Ge_{0.95}Si_{0.05}$ nGAAFETs without Parasitic Channels by Wet Etching," 2022 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), Hsinchu, Taiwan, 2022, pp. 1-2

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Publication List (相關論文發表)

A: Journal Paper (學術期刊論文)

1. Chien-Te Tu, Wan-Hsuan Hsieh, Bo-Wei Huang, Yu-Rui Chen, Yi-Chun Liu, Chung-En Tsai, **Shee-Jier Chueh**, and C. W. Liu, "Experimental Demonstration of TreeFETs Combining Stacked Nanosheets and Low Doping Interbridges by Epitaxy and Wet Etching," IEEE Electron Device Letters, Vol. 43, No. 5, pp. 682-685, May 2022.
2. Bo-Wei Huang, Chung-En Tsai, Yi-Chun Liu, Chien-Te Tu, Wan-Hsuan Hsieh, Sun-Rong Jan, Yu-Rui Chen, **Shee-Jier Chueh**, Chun-Yi Cheng, and C. W. Liu, "Highly Stacked GeSn Nanosheets by CVD Epitaxy and Highly Selective Isotropic Dry Etching," IEEE Transactions on Electron Devices, Vol. 69, No. 4, pp. 2130-2136, Apr. 2022.
3. Yi-Chun Liu, Chien-Te Tu, Chung-En Tsai, Bo-Wei Huang, Chun-Yi Cheng, **Shee-Jier Chueh**, Jyun-Yan Chen, and C. W. Liu, "Highly Stacked GeSi Nanosheets and Nanowires by Low-Temperature Epitaxy and Wet Etching," IEEE Transactions on Electron Devices, Vol. 68, No. 12, pp. 6599-6604, Dec. 2021.

B: Conference Paper (學術會議論文)

1. **(Best Paper Award)** **Shee-Jier Chueh**, Yi-Chun Liu, Chun-Yi Cheng, Bo-Wei Huang, Chien-Te Tu, and C. W. Liu, "Highly Stacked $Ge_{0.75}Si_{0.25}$ Nanosheet nFETs" 2022 International Electron Devices and Materials Symposium (IEDMS), Nantou, Taiwan, Oct. 27-28, 2022.
2. Yi-Chun Liu, Yu-Rui Chen, Yun-Wen Chen, Hsin-Cheng Lin, Wan-Hsuan Hsieh, Chien-Te Tu, Bo-Wei Huang, Wei-Jen Chen, Chun-Yi Cheng, **Shee-Jier Chueh**, and C. W. Liu, "Extremely High-κ $Hf_{0.2}Zr_{0.8}O_2$ Gate Stacks Integrated into $Ge_{0.95}Si_{0.05}$ Nanowire and Nanosheet nFETs Featuring Respective Record I_{ON} per Footprint of 9200μA/μm and Record I_{ON} per Stack of 360μA at V_{OV}=V_{DS}=0.5V," Symposium on VLSI Technology and Circuits (VLSI), JUNE 11-16, 2023.
3. Yu-Rui Chen, Yi-Chun Liu, Zefu Zhao, Wan-Hsuan Hsieh, Jia-Yang Lee, Chien-Te Tu, Bo-Wei Huang, Jer-Fu Wang, **Shee-Jier Chueh**, Yifan Xing, Guan-Hua Chen, Hung-Chun Chou, Dong Soo Woo, M. H. Lee, and C. W. Liu, "First Stacked Nanosheet FeFET Featuring Memory Window of 1.8V at Record Low Write Voltage of 2V and Endurance >1E11 Cycles," Symposium on VLSI Technology and Circuits (VLSI), JUNE 11-16, 2023.

doi:10.6342/NTU202301581

4. Chien-Te Tu, Yi-Chun Liu, Bo-Wei Huang, Yu-Rui Chen, Wan-Hsuan Hsieh, Chung-En Tsai, **Shee-Jier Chueh**, Chun-Yi Cheng, Yichen Ma, and C. W. Liu, "First Demonstration of Monolithic 3D Self-aligned GeSi Channel and Common Gate Complementary FETs by CVD Epitaxy Using Multiple P/N Junction Isolation," International Electron Devices Meeting (IEDM), 2022.
5. Chung-En Tsai, Chun-Yi Cheng, Bo-Wei Huang, Hsin-Cheng Lin, Tao Chou, Chien-Te Tu, Yi-Chun Liu, Sun-Rong Jan, Yu-Rui Chen, Wan-Hsuan Hsieh, Kung-Ying Chiu, **Shee-Jier Chueh**, and C. W. Liu, "Nearly Ideal Subthreshold Swing and Delay Reduction of Stacked Nanosheets Using Ultrathin Bodies," Symposium on VLSI Technology and Circuits (VLSI), JUNE 13-17, 2022.
6. **(Best Student Paper Award)** Chun-Yi Cheng, Wan-Hsuan Hsieh, Bo-Wei Huang, Yi-Chun Liu, Chien-Te Tu, Chung-En Tsai, **Shee-Jier Chueh**, Guan-Hua Chen, and C. W. Liu, "6 Stacked $Ge_{0.95}Si_{0.05}$ nGAAFETs without Parasitic Channels by Wet Etching," accepted by 2022 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2022.
7. **(Best Student Paper Award, the first winner from Taiwan)** Chung-En Tsai, Yi-Chun Liu, Chien-Te Tu, Bo-Wei Huang, Sun-Rong Jan, Yu-Rui Chen, Jyun-Yan Chen, **Shee-Jier Chueh**, Chun-Yi Cheng, Chia-Jung Tsen, Yichen Ma, and C. W. Liu, "Highly Stacked 8 $Ge_{0.9}Sn_{0.1}$ Nanosheet pFETs with Ultrathin Bodies (~3nm) and Thick Bodies (~30nm) Featuring the Respective Record I_{ON}/I_{OFF} of 1.4x107 and Record I_{ON} of 92μA at VOV=VDS= -0.5V by CVD Epitaxy and Dry Etching," pp. 569-572, International Electron Devices Meeting (IEDM), 2021.
8. **(Research Highlight)** Nature Electronics, Vol. 4, July 2021, P452. **(Highlight paper)** Yi-Chun Liu, Chien-Te Tu, Chung-En Tsai, Yu-Rui Chen, Jyun-Yan Chen, Sun-Rong Jan, Bo-Wei Huang, **Shee-Jier Chueh**, Chia-Jung Tsen, and C. W. Liu, "First Highly Stacked $Ge_{0.95}Si_{0.05}$ nGAAFETs with Record ION = 110 μA (4100 μA/μm) at VOV=VDS=0.5V and High $G_{m,max}$ = 340 μS (13000 μS/μm) at VDS=0.5V by Wet Etching," Symposia on VLSI Technology and Circuits (VLSI), 2021.

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摘要

自 1940 年電晶體的發明以來，技術的進步已將其尺寸推向極限，摩爾定律恰好描述了每兩年電晶體數量翻倍的情況，至今仍然適用。MOSFET 由於其卓越的設計，已成為邏輯 IC 的首選。而 FinFET 取代了平面 MOSFET，而 GAAFET 將以其較佳的閘極控制力接續 FinFET，因其在縮小寬度和實現高寬比方面具有優勢。2022 年，GAAFET 在量產中正式取代了 FinFET。望後數十年的努力目標，包 含於鍺(Ge)的材料和使用 GAA 元件結構。

我們通過化學氣相沉積磊晶和高選擇性的蝕刻來製作高通道層數堆疊的鍺矽(GeSi)電晶體。GeSi 是一種高遷移率通道材料，被視為下一個世代的通道材料。磊晶層被精心設計以創建高度堆疊的元件結構。TEM、HRXRD、RSM 和 SIMS 等證實了磊晶層的成功生長和 GeSi 通道中的應變(strain)。製程流程包括化學氣相沉積磊晶、黃光製程、乾蝕刻(fin formation)及濕蝕刻(channel release)。濕蝕刻中，H_2O_2 用於去除鍺犧牲層(sacrificial layers)，而 NH_4OH 則去除了 Ge 緩衝層(buffer)下的不需要的 SOI (Silicon On Insulator)層，並且討論了兩者的濕蝕刻機制。我們成功展示了使用 $Ge_{0.95}Si_{0.05}$ 和 $Ge_{0.75}Si_{0.25}$ 通道層製作奈米片和奈米線電晶體的挑戰和製造流程，且無需進行源極-汲極再生長(S/D regrow)。

L_g =80nm 的 8 通道堆疊 $Ge_{0.75}Si_{0.25}$ 奈米片在 $V_{OV} = V_{DS} = 0.5V$ 時，I_{ON} =36μA（390μA/μm 對通道所占面積標準化），次臨界擺幅 SS=121mV/dec；L_g =70nm 的 7 通道堆疊 $Ge_{0.95}Si_{0.05}$ 奈米線在 $V_{OV} = V_{DS} = 0.5V$ 時， I_{ON} =128μA（為

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5800μA/μm 對通道所占面積標準化），次臨界擺幅 SS=112mV/dec。我們討論了寄生通道的存在對於元件 I-V 特性的影響。另外還探討了微橋效應(microbridge effect)，顯示了微橋結構帶來了增強的伸應變(tensile strain)和更好電子遷移率(electron mobility)。總體而言，製造的鍺矽奈米片和奈米線展示了好的 I-V 特性和應用於先進製程的潛力。

未來工作總結為三個方向：精進製程技術、縮小電晶體尺寸以提高元件性能，以及製作下一代電晶體結構:互補式場效電晶體(CFET)。

關鍵詞：n 型閘極環繞式電晶體、奈米片、奈米線，鍺矽，通道釋放，應變模擬

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Abstract

Since the invention of the transistor, technological advancements have pushed its size to the limits. The FinFET replaced planar MOSFETs, and GAAFETs are set to take over with superior gate controllability and electrostatic characteristics. GAAFETs offer advantages in scaling down width and achieving high aspect ratios. In 2022, GAAFETs replaced FinFETs in mass production. Future innovations include Ge-based materials and the adoption of GAA structure in device architecture.

We explore the fabrication of highly stacked GeSi channels using epitaxial structures and selective etching. GeSi, a high mobility channel material, is investigated as an alternative to enhance CMOS performance. The process flow involves epitaxy growth, lithography, fin formation, and channel release. Wet etching with H_2O_2 is used to selectively remove sacrificial layers, while NH_4OH eliminates unwanted layers beneath the Ge buffer. Discussion of the wet etching mechanism and the challenges and successful fabrication of nanosheet and nanowire devices using $Ge_{0.95}Si_{0.05}$ and Ge0.75Si0.25 channel layers are presented. The epitaxy layers are carefully designed to create a highly stacked device structure. Various techniques, such as TEM, HRXRD, RSM, and SIMS, confirm the successful growth of epitaxy layers and strain in the GeSi channels. The fabrication process includes steps such as thinning the SOI substrate, growing a Ge buffer layer, deposition of sacrificial and channel layers, gate stack

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formation, and S/D contact formation. The process is completed with the sputter deposition of S/D contacts using Pt. These devices hold promise for high-performance semiconductor devices and integrated circuits.

The electrical properties of the nanosheets and nanowires are comprehensively investigated, the 8 stacked $Ge_{0.75}Si_{0.25}$ nanosheets, each with an L_g of 80nm, exhibit an I_{ON} of 36μA per stack (390μA/μm per channel footprint) at V_{OV} and V_{DS} of 0.5V, with a SS of 121mV/dec and the 7 stacked $Ge_{0.95}Si_{0.05}$ nanowires, each with an L_g of 70nm, exhibit an I_{ON} of 128μA per stack (5800μA/μm per channel footprint) at $V_{OV} = V_{DS} =$ 0.5V, with a SS of 112mV/dec. The effect of parasitic channels is discussed, which affects the I-V characteristics in the I_{OFF} region of the devices. The microbridge effect is also explored, showing enhanced tensile strain and electron mobility. In short, the fabricated GeSi nanosheets and nanowires demonstrate desirable electrical characteristics and potential for advanced transistor applications.

In the end, future work is summarized in three directions: improve the processing technique, scale down certain dimensions to improve device performance, and build the next-generation device CFET, integrating the nanosheet or nanowire structure we discuss in this article.

Keywords: nGAAFET, Nanosheet, Nanowire, GeSi, Channel Release, Strain Simulation

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Chapter 1 Introduction

1.1 Research Background and Purpose

Since the invention of the first transistor in 1940, continuous technological advancements have pushed the size of transistors towards their physical limits. Integrated circuits (ICs) were successfully demonstrated a decade later, and since then, researchers, scientists, and engineers worldwide have been striving to improve the power, performance, and area (PPA) properties of small IC chips. Moore's Law [1] was proposed to describe the consistent increase in transistor count in ICs, stating that the number of transistors doubles approximately every two years. This trend has been followed and achieved for several decades, particularly when considering transistor density.

The PPA of a single transistor plays a crucial role in determining the overall quality of a chip. While the bipolar junction transistor (BJT) was the first to be demonstrated (**Fig. 1-1**), the metal-oxide-semiconductor field-effect transistor (MOSFET), with its superior design, is the transistor of choice for logic ICs. By combining p-channel and n-channel MOSFETs, complementary metal-oxide-semiconductor (CMOS) technology enables the design of logic circuits performing various computations such as NOT,

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NAND, NOR, and more. The CMOS property aligns perfectly with the needs of the digital world, making MOSFETs the dominant technology in the logic semiconductor industry.

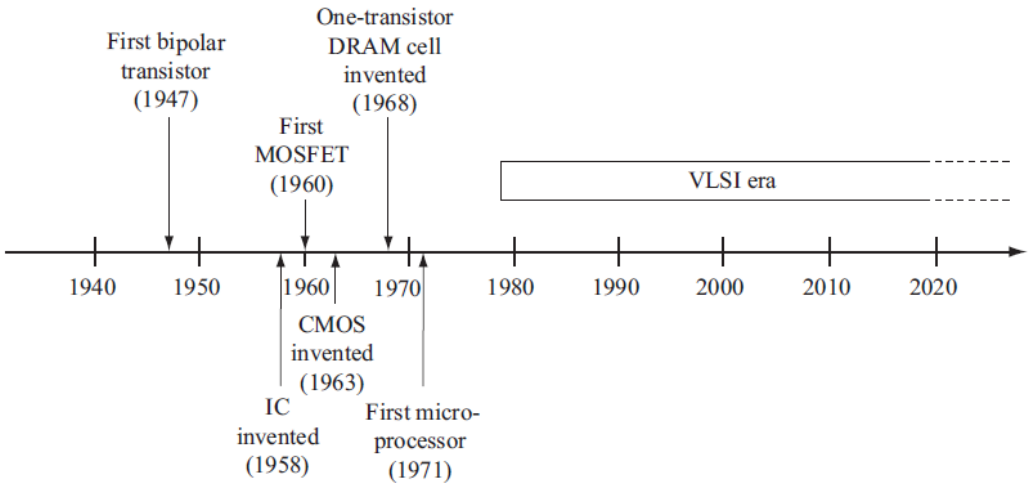

Figure 1-1 The history of transistor and timeline. [2]

Furthermore, MOSFET technology continues to evolve (**Fig. 1-2**). Initially, it adopted a planar architecture, but as technology progressed, innovators faced limitations. Many believed that Moore's Law would come to an end. However, the FinFET was introduced [3], replacing planar MOSFETs in subsequent technology nodes. Following the FinFET, the gate-all-around (GAA) structure is set to take its place in the next generation of nodes. The GAA architecture, whether in the form of nanosheets or nanowires, offers unmatched gate controllability and superior electrostatic characteristics compared to FinFETs [4-6]. It demonstrates improved performance in

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key electrostatic metrics such as shot channel effect (SCE), drain-induced barrier lowering (DIBL), and subthreshold slope (SS) [7-9].

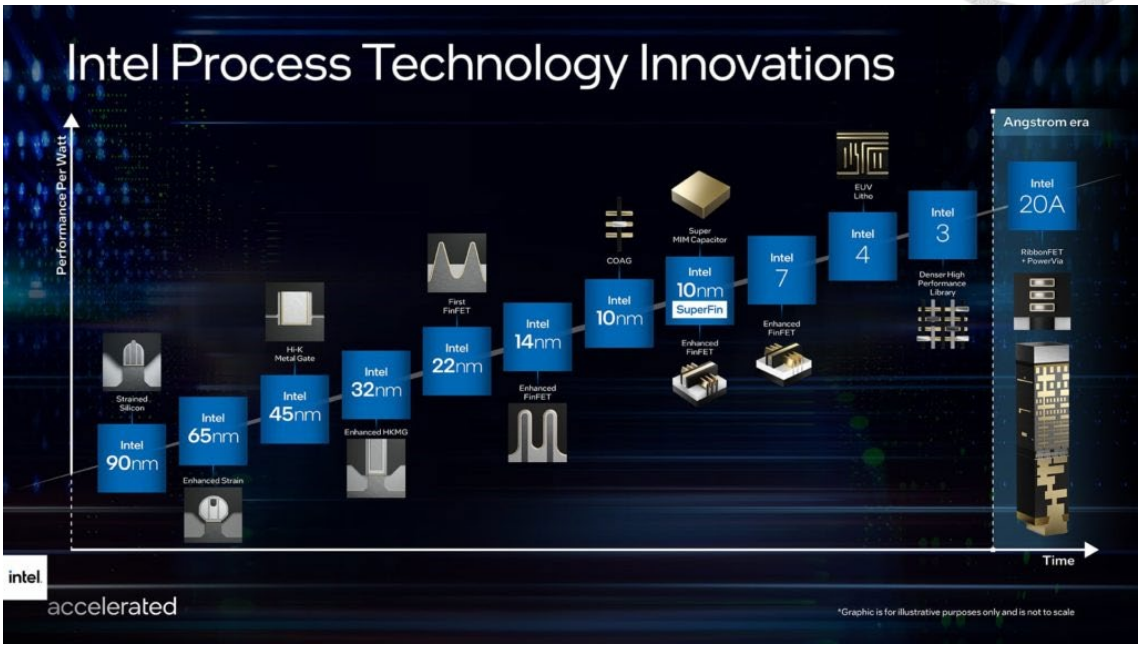

Figure 1-2 The history of technology node and big innovations timeline. [10]

In contrast, FinFETs face challenges in scaling down fin width (W_{fin}) and achieving high aspect ratios due to limitations in lithography and etching processes. GAAFETs, on the other hand, provide the advantage of flexible width design and a high channel width to channel height (W_{CH} / H_{CH}) ratio achieved through selective etching of different materials and epitaxy techniques. This flexibility in width design allows for greater optimization and improved control over the transistor's electrostatic properties. Also, GAA structure with channel stacking can give large current in a fixed area as compared to FinFET and therefore further enhance PPA of the IC chips [11]. As a result,

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in 2022, gate-all-around (GAA) FETs were successfully commercialized in mass production, replacing FinFETs in industry products [12].

Looking ahead to the next decade, there are numerous innovations set to become a reality. According to the International Roadmap for Devices and Systems (IRDS), Ge-based materials are favored for channel materials (**Fig. 1-3**). From both academic and industry perspectives, the GAA structure has been chosen to replace FinFETs in device architecture (**Fig. 1-4**).

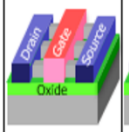
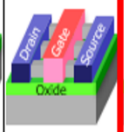
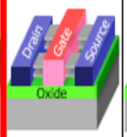
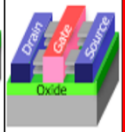
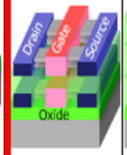
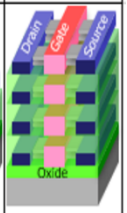
YEAR OF PRODUCTION	2021	2022	2025	2028	2031	2034
	G51M30	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4
Logic industry "Node Range" Labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
Platform device for logic	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
						
Channel material technology inflection	SiGe25%	SiGe50%	SiGe50%	Ge, 2D Mat	Ge, 2D Mat	Ge, 2D Mat

Figure 1-3 The roadmap of IEEE IRDS 2021. [13]

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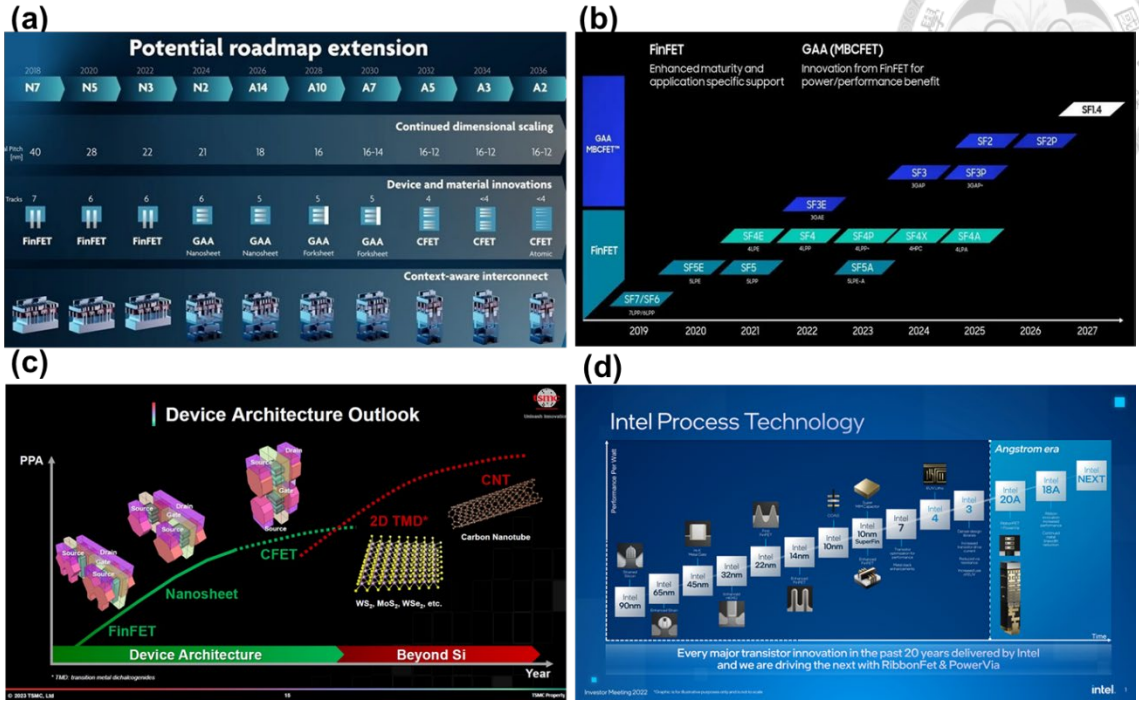

Figure 1-4 Transistor roadmap of (a) imec, (b) Samsung, (c)TSMC, and (d) intel. [14] [15] [16] [17]

Currently, in the material of advanced transistor, SiGe high mobility channel has start to been used in the industry since 5nm node (**Fig. 1-5(a)**). If we want to enhance the current of nanosheet devices, one way to do so is to stack more channels in a given footprint. This idea is already demonstrated by industry (**Fig. 1-5(b)**). In the research, a 7 stacked Si nanosheet device is also reported (**Fig. 1-5(c)**). But there is no work combining both techniques, high mobility channel and highly stacked nanosheet device, now. Therefore, this is the ideal we would like to realize and the results are shown in the **(Fig. 1-6).**

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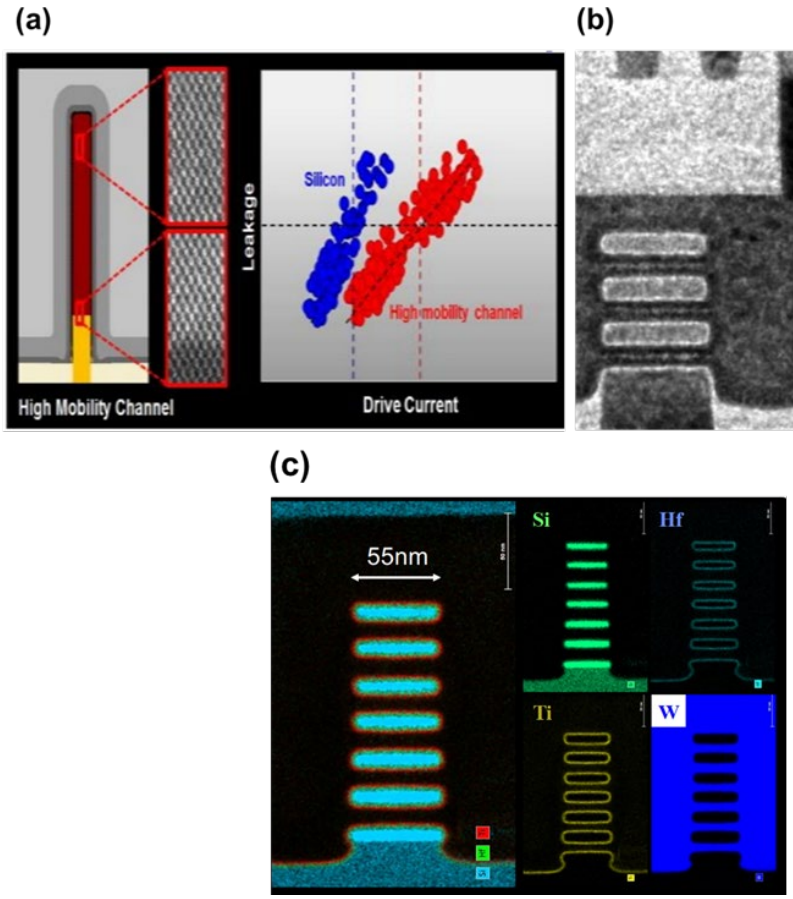

Figure 1-5 (a) SiGe high mobility channel is used 5nm node [18], (b) 3 stacked of nanosheet transistor is presented by industry [19], (c) the TEM of a 7 stacked Si nanosheet device [20]

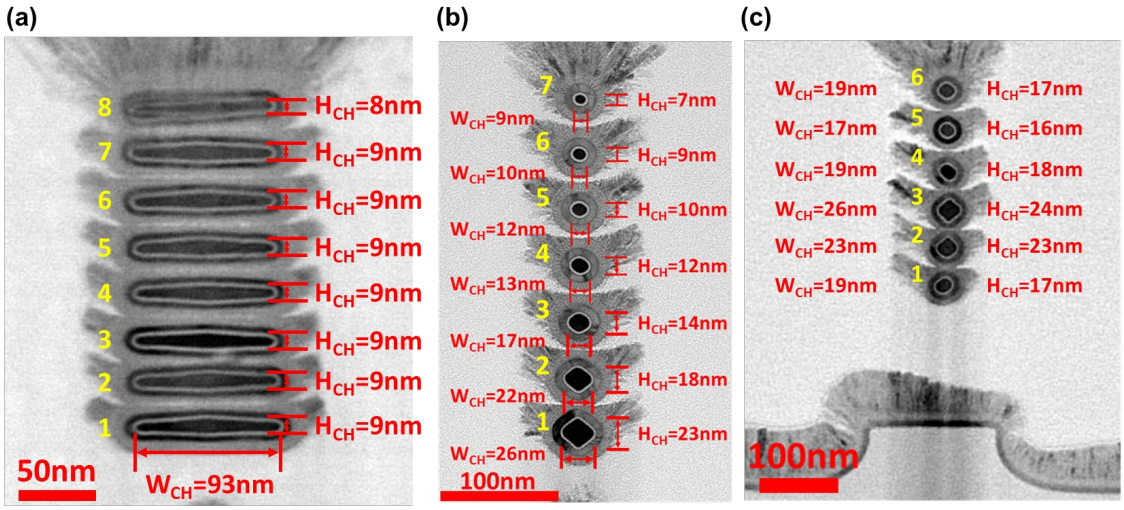

Figure 1-6 Our work of (a) $Ge_{0.75}Si_{0.25}$ highly stacked nanosheet device, (b) $Ge_{0.95}Si_{0.05}$ highly stacked nanowire device, (c) $Ge_{0.95}Si_{0.05}$ highly stacked nanowire without parasitic channel device. [21] [22] [23]

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1.2 Thesis Structure Organization

The thesis is structured into five chapters, each focusing on a specific aspect of the research topic.

Chapter 1 introduces the research background, highlighting the significance of improving the power, performance, and area (PPA) properties of integrated circuits (ICs). It also discusses the evolution of transistor technology from MOSFETs to FinFETs and the emergence of gate-all-around (GAA) FETs.

Chapter 2 delves into the fabrication of highly stacked GeSi nanosheets and nanowires for GAA structures. It discusses the introduction of channel stacked GAA structures as a replacement for FinFETs and explores the use of GeSi as a promising channel material. The chapter presents the process flow for fabricating stacked channels, including epitaxy growth, lithography, etching, and channel release techniques.

Chapter 3 focuses on the detailed fabrication process of highly stacked GeSi nanosheets and nanowires for GAA FETs. It explains the growth of epitaxial layers on a silicon-on-insulator (SOI) substrate, channel release to isolate the GeSi structures, gate stack formation for effective control of the channel region, and source/drain contact formation.

Chapter 4 is dedicated to characterizing and evaluating the performance of the fabricated GeSi nanosheets and nanowires. It discusses the electrical characteristics,

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mobility enhancement, and other relevant parameters of the devices. The chapter also examines the impact of parasitic channels and provides a comprehensive analysis of the experimental results.

Chapter 5 concludes the thesis with a summary of the research findings and presents future work directions. It offers a comprehensive summary of the thesis, highlighting the key contributions and outcomes of the research. Additionally, it identifies potential areas for further exploration and improvement, based on the current research findings.

Overall, the thesis structure is designed to provide a systematic and comprehensive investigation of the fabrication process and performance evaluation of highly stacked GeSi nanosheets and nanowires for application in advanced technology node.

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Chapter 2 Channel Release for Highly Stacked GeSi Nanosheets and Nanowires

2.1 Introduction

With the advancement of CMOS technology beyond the 3nm node, the introduction of channel stacked Gate-All-Around (GAA) structures has been accomplished as a replacement for FinFETs. The implementation of stacked GAA structures offers significant improvements in performance, power, and area, along with increased effective channel width (W_{eff}) and overall performance enhancement. Additionally, the use of stacked Si GAAFETs has been extensively researched, but they have encountered physical limitations during the scaling process. To address this, high mobility channel materials such as SiGe ([Si]>[Ge]), Ge, and GeSi ([Ge]>[Si]) have emerged as promising alternatives to enhance CMOS performance without compromising on the device footprint.

As a result, GeSi has gained attention as a channel material that can be grown on Ge sacrificial layers using Chemical Vapor Deposition (CVD) epitaxy, leading to the formation of effective strain for nFETs. This is due to the 4% misfit between Si and Ge,

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as illustrated in (**Fig. 2-1**).

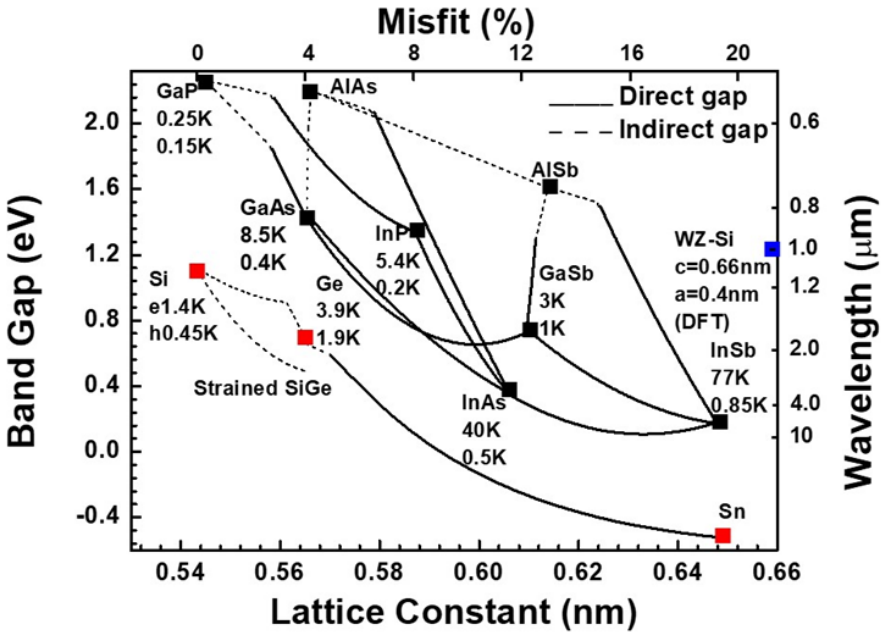

Fig. 2-1 Materials properties include Si and Ge. [24]

Besides, the reason why Ge has higher mobility than Si can be observed in their band structure (**Fig. 2-2**). Si has 6 valleys and Ge has 8 valleys. The former valley is like a hot dog because of the ratio of major and minor axis is 5. The valley of the later is like a bamboo due to the ratio is 20. In order to get the mobility in current direction [110], we need to project the effective mass to [110]. We can see that the effective mass of Ge is one order lower than that of Si. Smaller effective mass means higher mobility and higher mobility brings higher current density. Therefore, using Ge as channel material can ensure we have a higher intrinsic channel mobility.

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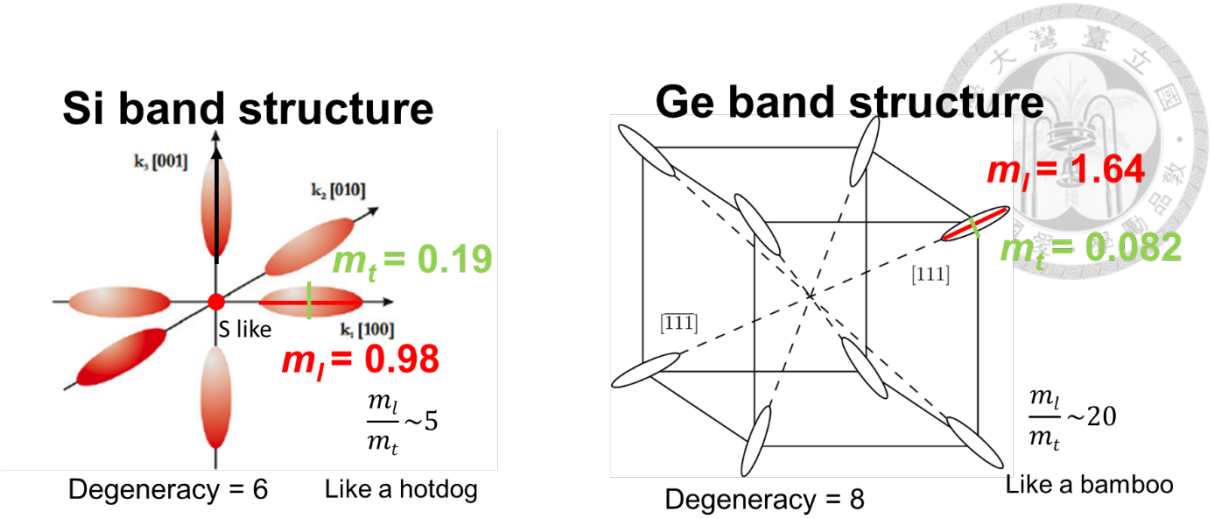

Fig. 2-2 The band structure of Si and Ge. [25]

In order to build the highly stacked channel, one feasible method is to deposit an epitaxial structure of two different materials alternately on the substrate. The sacrificial layers (SLs) can be removed to release the channels, taking advantage of the disparate etching rates between the two materials. Therefore, the selection of materials for the channel and sacrificial layers, defect control, the thickness of the epitaxial structure, and selective etching play crucial roles in the process.

The objective of this chapter is to fabricate highly stacked GeSi channels using epitaxial structures and selective etching. Wet etching with H_2O_2 demonstrates sufficient etching selectivity of Ge over GeSi, enabling the formation of wide stacked nanosheets. Moreover, we also experiment with different conditions of H_2O_2 to produce nanowires. Additionally, NH_4OH is utilized to remove the SOI layer beneath the Ge buffer and prevent the formation of parasitic channels. The results pertaining to these techniques

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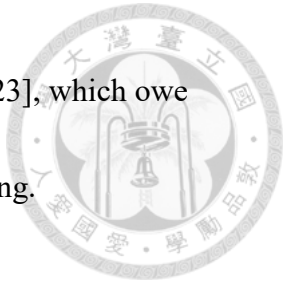

were published in VLSI 2021 [21], TED [22], and VLSI-TSA 2022 [23], which owe credit to the valuable contributions of senior researchers Liu and Cheng.

2.2 Process Flow of Stacked Channels

Fabricating a stacked channel device involves a series of steps aimed at achieving the desired structure. Firstly, a superlattice structure is grown, followed by the utilization of lithography and etching tools to define the fin area. Subsequently, channel release is conducted to obtain the stacked channel.

For the CVD epitaxy process, an 8" single-wafer rapid thermal CVD (RTCVD) system is employed to grow the epitaxy structure. All the epitaxy layers utilized in this study are grown using this machine, employing meticulously designed recipes to optimize the outcomes. Following the epitaxy growth, field oxide (FOX) deposition is carried out via plasma-enhanced chemical vapor deposition (PECVD), and then patterned to prevent oxidation and distortion of the samples.

As our objective is to construct a stacked channels device with gate length (Lg) ranging from 40 nm to 90 nm and width (W) ranging from 60 nm to 160 nm, electron-beam (e-beam) lithography is employed to define the fin area. Subsequently, an anisotropic dry etching tool is utilized for fin formation. This tool ensures the creation of straight and steep fins through the optimization of etching gas and time parameters.

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Following the fin formation, wet etching is employed to perform channel release, where sacrificial layers (SLs) are removed, leaving behind the channel layers. The width and height of the channels are primarily determined after the channel release process. Thus, channel release is the key to forming highly stacked channels and determining the dimensions of channels. One can find the process mentioned in (**Fig. 2-3**).

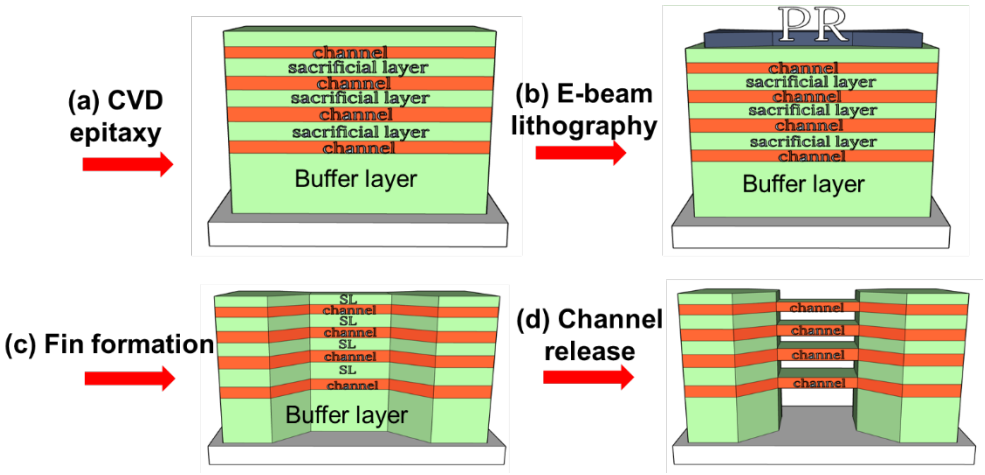

Fig. 2- 3 Process flow of stacked channels including (a) CVD epitaxy, (b) e-beam lithography, (c) fin formation, (d) channel release.

2.3 Channel Release for GeSi Channels

2.3.1 H_2O_2 and NH_4OH Wet Etching Mechanism

During the channel release process for our devices, the objective is to remove the Ge sacrificial layers while preserving the GeSi layers. To achieve this, we need to find an etchant that exhibits a higher etching selectivity for Ge over GeSi. Among the various candidates considered, a hydrogen peroxide (H_2O_2) solution is the most suitable

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and has been studied for etching Ge/Si [26-27]. Hydrogen peroxide can oxidize Ge, forming water-soluble GeOx. The reactions involved are as follows:

$$Ge + 2H_2O_2 \rightarrow GeO_2 + 2H_2O$$

$$GeO_2 + H_2O \rightarrow H_2GeO_3\ (aq)\ [28]$$

Oxidation also occurs in the GeSi layers; however, the presence of [Si] helps to alleviate the etching rate. Consequently, the GeSi layers can be preserved, allowing for the fabrication of stacked channels (**Fig. 2-3**).

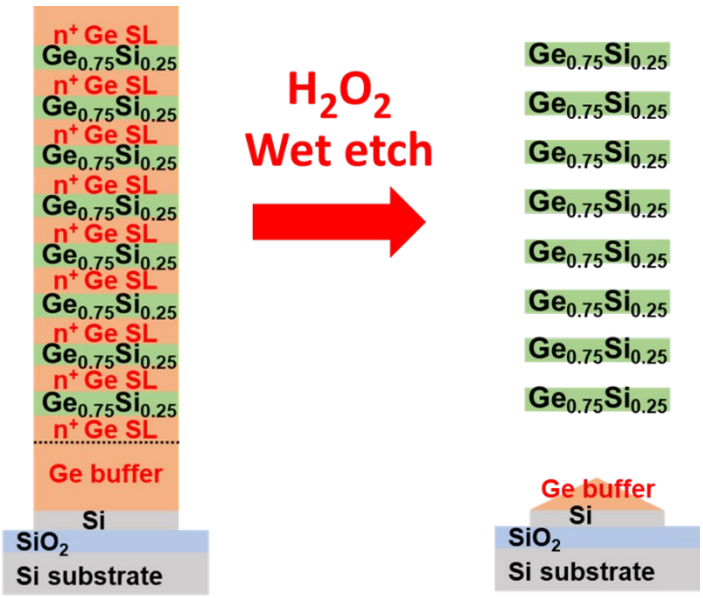

Fig. 2-4 Channel release using H_2O_2 for $Ge_{0.75}Si_{0.25}$ device. The Ge buffer and Si at the bottom is the parasitic channel.

In our epitaxy structure, we grow an 800-nm Ge buffer on SOI, which is thick enough to mitigate dislocation at the Ge/Si interface after an 800°C annealing. Subsequently, sacrificial layers and channel layers are grown using epitaxy design.

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However, when performing channel release, it proves challenging to completely remove the SOI beneath the Ge buffer using the hydrogen peroxide recipe mentioned earlier. If the SOI remains after channel release, it becomes a parasitic channel, leading to undesired current flow when the device is turned off. The impact of parasitic channels will be discussed in detail in Chapter 4.

Previous studies have shown that NH_4OH can exhibit high etching selectivity for Si and SiGe at an etching temperature of 75°C [29]. To eliminate the SOI layer beneath the Ge buffer during the channel release process, we introduce a recipe utilizing ammonium hydroxide (NH_4OH) prior to H_2O_2. The chemical reaction involving NH_4OH is as follows:

$$\mathbf{Si + 2OH^- + 4H_2O \rightarrow Si(OH)_6^{2-}{}_{(aq)} + 2H_2\ (g)\ [30\text{-}31]}$$

The product of this reaction are soluble material and hydrogen gas, which enables the removal of the SOI layer beneath the Ge buffer by utilizing NH_4OH in channel release process (**Fig. 2-4**). Note that, the gas release is observed during the NH_4OH the process and it requires extra carefulness.

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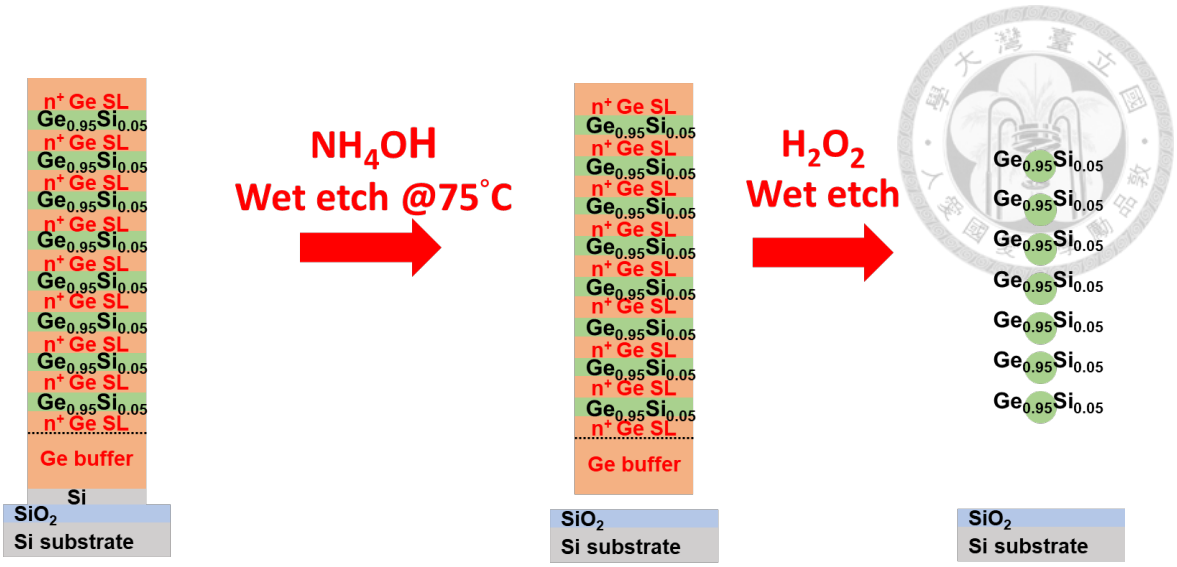

Fig. 2-5 Channel release combines NH_4OH and H_2O_2 for $Ge_{0.95}Si_{0.05}$ device. The Ge buffer and Si at the bottom is totally removed.

2.3.2 Discussion of $Ge_{0.95}Si_{0.05}$ and $Ge_{0.75}Si_{0.25}$

In pursuit of transistors with higher on-current (I_{ON}), numerous innovative technologies have been developed, such as high-k dielectric oxides and strain engineering. In our work, we aim to increase electron mobility by utilizing Ge-based channels. We grow channel layers with compositions of 75% Ge and 95% Ge. Increasing the [Ge] in GeSi is not as simple as adding more precursor or adjusting a single parameter. Several factors need to be considered, necessitating a process of trial and error. Initially, we grow testing wafers to evaluate the growth rate at each step and the effects of varying parameters. Since it is not feasible to test all conditions in a single round or due to cost constraints, multiple iterations are required until we obtain

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confident answers to proceed to the next step. Subsequently, we calculate the growth rate and convert it to the desired conditions for application on our SOI wafer. Fortunately, we obtain two successful epitaxy samples, enabling us to proceed with e-beam lithography and fin formation processes.

During the channel release process, H_2O_2 is used as a wet etchant for both the $Ge_{0.95}Si_{0.05}$ and $Ge_{0.75}Si_{0.25}$ samples. Etching entails numerous considerations, such as the quality of the etchant, etching time, and environmental temperature, among others. This stage also requires trial and error. In our case, we have two types of samples, and we know that higher [Si] leads to higher etching selectivity. Consequently, the etching rate of $Ge_{0.95}Si_{0.05}$ channels is significantly higher than that of $Ge_{0.75}Si_{0.25}$. It was a challenging task to determine the appropriate conditions for both samples. Eventually, we successfully fabricate nanosheet devices for the $Ge_{0.75}Si_{0.25}$ samples and nanowire devices for the $Ge_{0.95}Si_{0.05}$ samples.

2.4 Summary

In this chapter, we emphasize the importance of material selection, defect control, epitaxial structure thickness, and selective etching in the formation of stacked channels. Our goal is to fabricate highly stacked GeSi channels through epitaxial structures and selective etching method. Insights into the process flow for fabricating stacked channels, involving the growth of superlattice structures, lithography, etching, and

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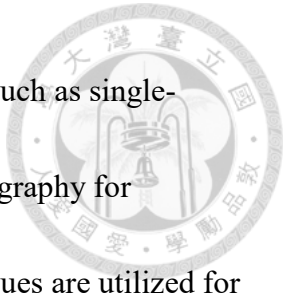

channel release are also presented. We employ advanced techniques such as single-wafer rapid thermal CVD for epitaxy growth and electron-beam lithography for defining the fin area. Anisotropic dry etching and wet etching techniques are utilized for fin formation and channel release, respectively.

We discuss the wet etching mechanism using H_2O_2 and NH_4OH for GeSi channels, explaining their selective etching properties and the elimination of unwanted layers. Furthermore, we present a detailed examination of the growth and etching processes for $Ge_{0.95}Si_{0.05}$ and $Ge_{0.75}Si_{0.25}$ channel layers, including the challenges faced and the successful fabrication of nanosheet and nanowire devices.

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Chapter 3 Fabrication of Highly Stacked GeSi Nanosheets and Nanowires

3.1 Introduction

This chapter presents the fabrication process of highly stacked germanium-silicon (GeSi) nanosheet and nanowire gate-all-around field-effect transistors (nGAAFETs) without source-drain regrowth. The process entails the growth of 17 epitaxial layers and a Ge buffer on a silicon-on-insulator (SOI) substrate. Subsequently, channel release, gate stack formation, and S/D contact formation are performed. The objective is to attain high electron mobility by utilizing undoped GeSi channel layers, thereby mitigating impurity scattering and reducing source/drain resistance through heavily phosphorus-doped germanium (Ge) sacrificial layers (SLs) in the S/D region.

The fabrication process commences with the growth of multiple epitaxial layers on the SOI substrate. This multilayer structure facilitates the formation of GeSi nanosheets and nanowires with superior structural integrity. Additionally, the inclusion of a Ge buffer layer serves to promote the lattice matching between the GeSi layers and the underlying SOI substrate, minimizing defects and enhancing device performance. Following the epitaxial growth, the channel release step is executed to isolate the GeSi structures from the substrate. This is achieved by selectively removing the SLs by using

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H_2O_2 and buried oxide layer using NH_4OH before H_2O_2. The resulting released nanowires exhibit enhanced electrical characteristics, as they are no longer influenced by the underlying substrate. Subsequently, the gate stack is formed to facilitate effective control of the channel region. EDX will be shown. The gate stack typically consists of a high-k dielectric layer and metal gate electrode. The high-k dielectric layer helps reduce gate leakage current, while the metal gate electrode enables efficient electrostatic control of the channel. Finally, the S/D contact formation is carried out to establish electrical connections with the GeSi channel. Heavily phosphorus-doped Ge sacrificial layers (SLs) are diffused during several annealing steps, which will reduce S/D resistance.

Epitaxy plays a crucial role in semiconductor manufacturing as it allows the creation of high-performance devices and integrated circuits. By growing epitaxial layers, we can introduce specific properties, such as different doping levels or channel Ge to Si ratios, to optimize the electrical and optical characteristics of the semiconductor material.

3.2 Epitaxy Layers Design

The ideal device architecture image is shown in (**Fig. 3-1**). So as to work it out, we need to carefully design our epitaxy structure. Following SOI thin down process, we can start grow epitaxy. It involves depositing a layer of Ge/Si onto another layer of Ge/Si

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which are both single-crystal substrate, creating a structure with precise atomic alignment and orientation. In order to fabricate a highly stacked channel device, as Chapter 2 mentioned, we have to deposit sacrificial layers and channel layers repeatedly and sandwich channel layer by sacrificial layers. In $Ge_{0.75}Si_{0.25}$ and $Ge_{0.95}Si_{0.05}$ devices, we both grow 8 channel layers and 9 sacrificial layers as in (**Fig. 3-2**).

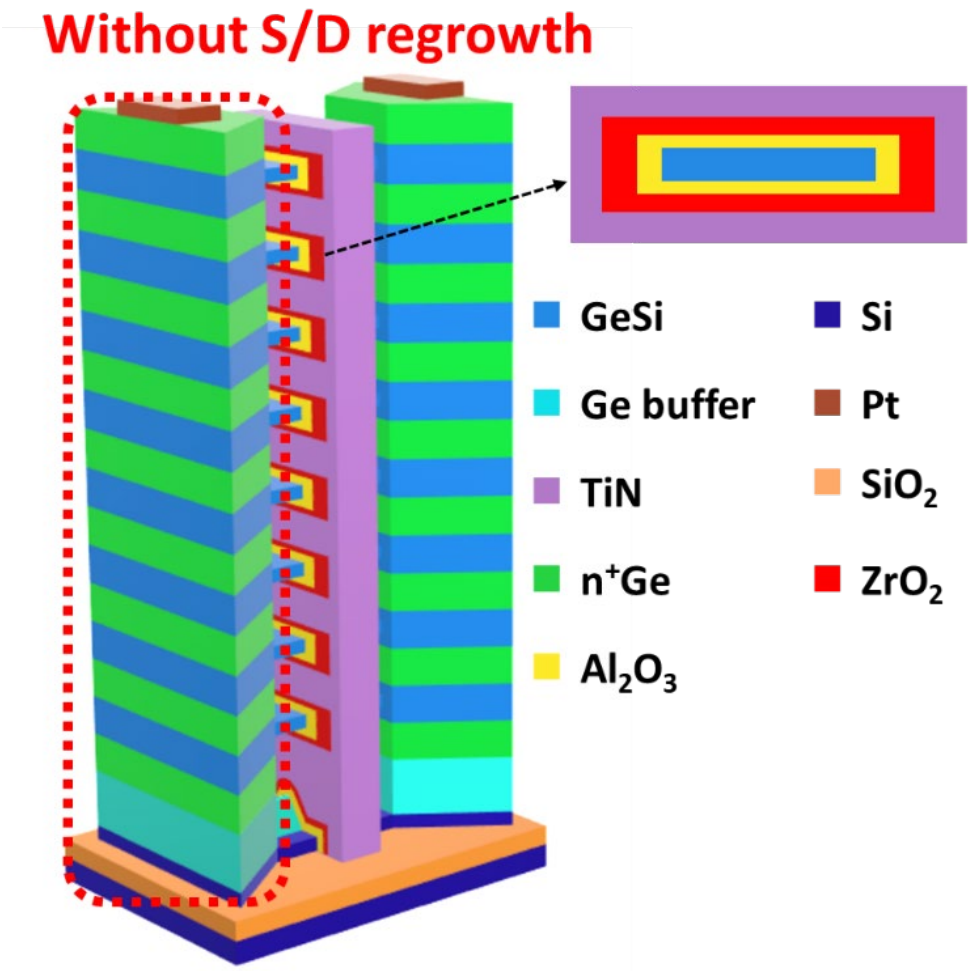

Fig. 3-1 The 3D schematic of our highly stacked device architecture.

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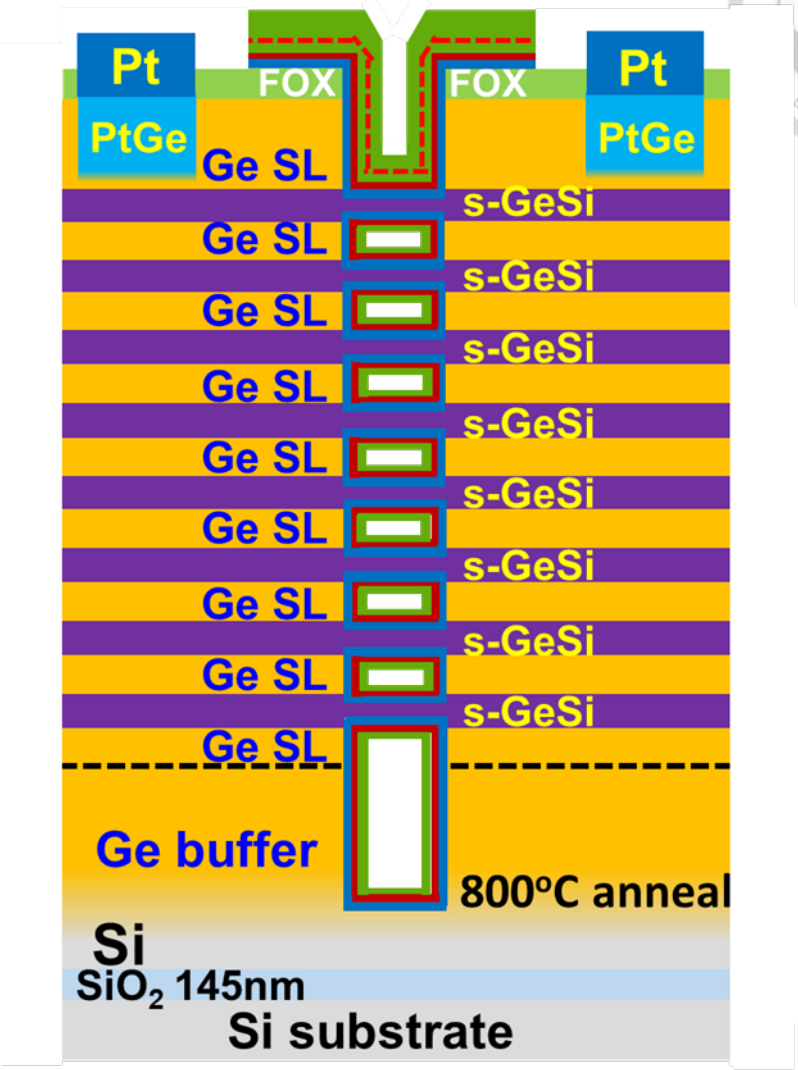

Fig. 3-2 Cross-section image of our device. There are 8 GeSi layers sandwiched by 9 Ge n^+ sacrificial layers.

Especially note that our design enables us to build this highly stacked device without source-drain (S/D) regrowth. S/D regrowth is a technique used in semiconductor processing to create the source and drain regions of a transistor. It involves selectively re-growing the semiconductor material in the source and drain

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regions after the formation of the gate structure. Nowadays, the industry does use S/D regrowth to improve device performance. However, there are also disadvantages associated with this technique:

Firstly, it increases complexity and cost: source-drain regrowth adds complexity to the fabrication process as it requires additional steps and equipment for epitaxial growth. This complexity can result in increased manufacturing costs, making the overall process more expensive. Besides, an additional process gives extra variability: source-drain regrowth introduces additional process variability. Variations in regrowth thickness, composition, and crystal quality can affect device performance and yield.

In this work, we focus on demonstrating a highly stacked device. Therefore, it would be suitable to build our devices in this novel way. By doing so, we can use epitaxy to define how many channels the final devices would have. Later, we can optimize our etching recipe, so we can make highly stacked devices.

3.3 Device Fabrication

(**Fig. 3-3**) presents the process flow. The fabrication process begins with the thinning of the top silicon layer of a 200-mm SOI substrate from 70 to 20 nm through oxidation and etching. An 800 °C annealing step is performed to confine misfit dislocations at the Ge/Si interface. Subsequently, an undoped 150-nm Ge buffer layer is

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grown on the SOI wafer at 375 °C. An in-situ annealing step at 800 °C further enhances the quality of the Ge buffer and reduces dislocations.

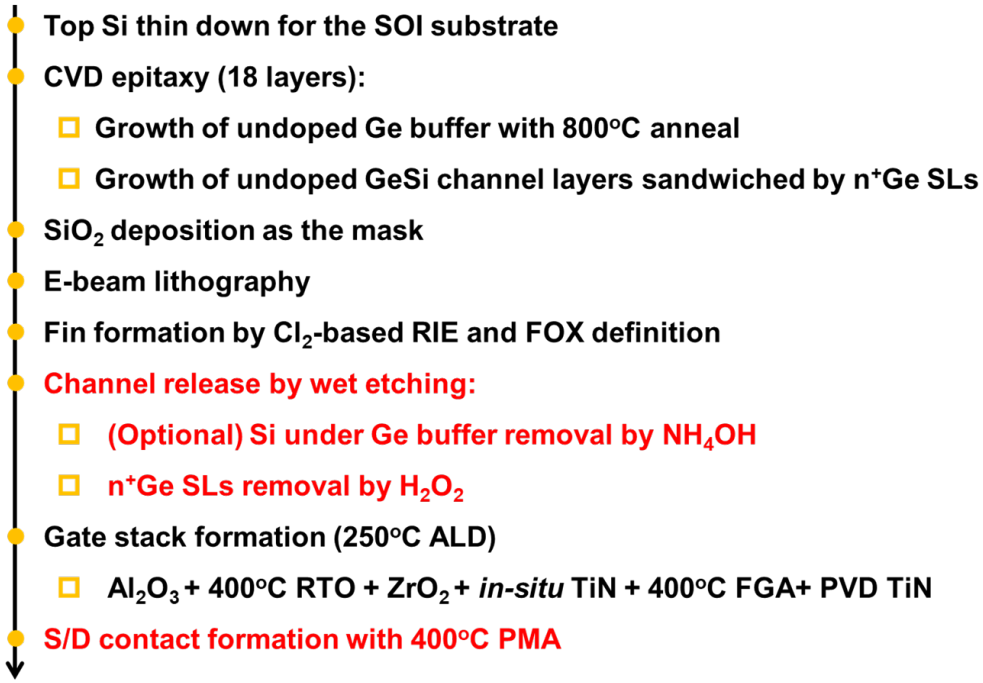

Fig. 3-3 Process flow of the 8 stacked $Ge_{0.75}Si_{0.25}$ nanosheet and 7 stacked $Ge_{0.95}Si_{0.05}$ nanowire device with extra NH_4OH wet etching to prevent parasitic channel

For $Ge_{0.75}Si_{0.25}$ channels, an alternating growth process involving the deposition of a 21-nm heavily phosphorus-doped Ge sacrificial layer and a 13-nm undoped $Ge_{0.75}Si_{0.25}$ channel layer is repeated eight times, followed by the deposition of a top 27-nm heavily phosphorus-doped Ge sacrificial layer. The same growth process is applied for $Ge_{0.95}Si_{0.05}$ channels, with the layer thicknesses adjusted accordingly. Transmission electron microscopy (TEM) images (**Fig. 3-4**) confirm the successful growth of the epitaxy layers.

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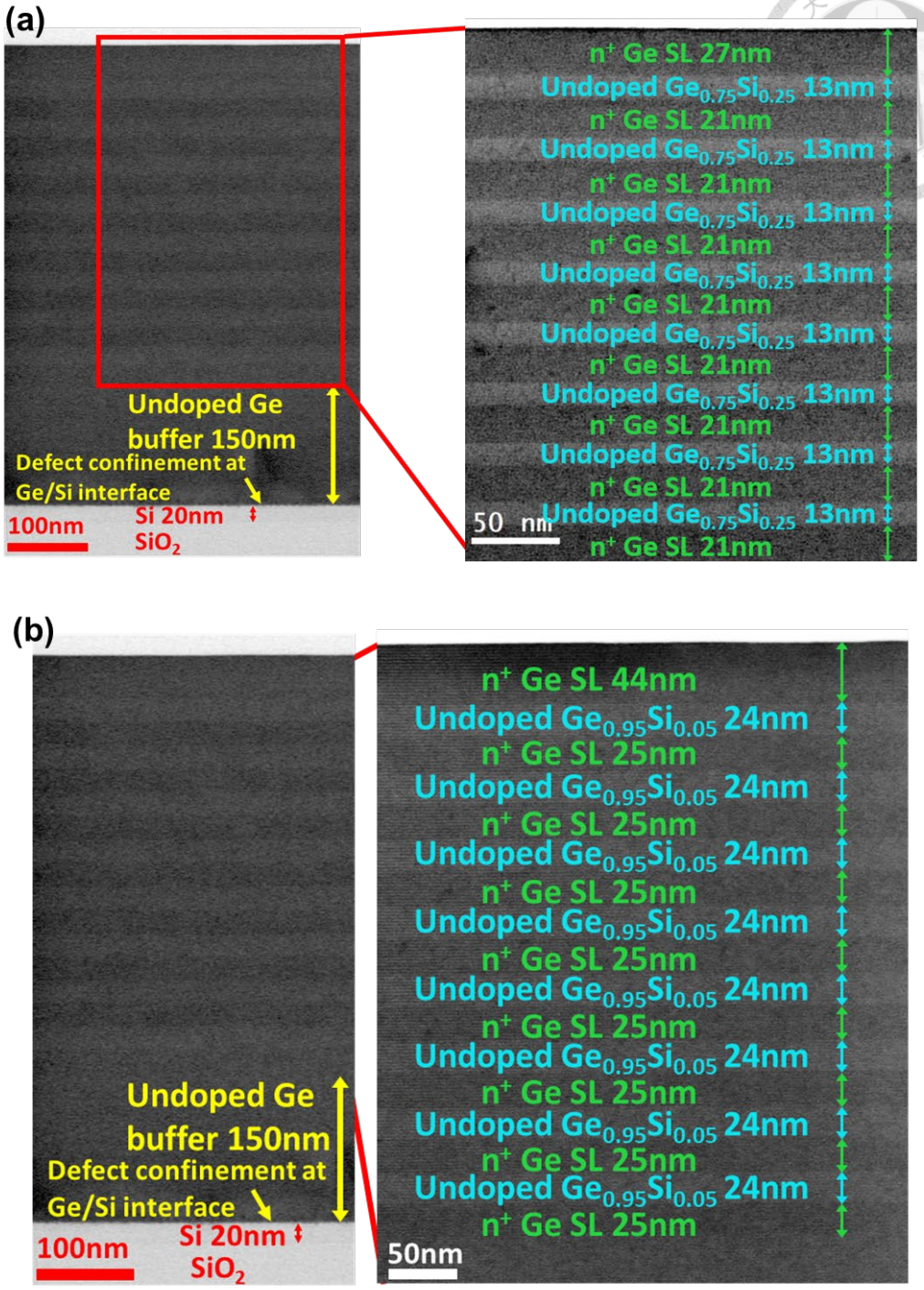

Fig. 3-4 TEM image of (a) epilayers with 8 $Ge_{0.75}Si_{0.25}$ channel, and (b) epilayers with 8 $Ge_{0.95}Si_{0.05}$ channel both sandwiched by 9 Ge SLs. [21-22]

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High-resolution X-ray diffraction (HRXRD) (**Fig. 3-5 (a) (c)**) analysis reveals tensile strain in the Ge buffer and GeSi channel. Reciprocal Space Mapping (RSM) confirms that there is 0.14% and 1.14% tensile strain in Ge and $Ge_{0.75}Si_{0.05}$. Also, in the case of Ge and $Ge_{0.95}Si_{0.05}$, there is 0.2% and 0.4% tensile strain respectively (**Fig. 3-5 (b) (d)**). The strain of GeSi on Ge is biaxial tensile strain due to lattice mismatch, and that of Ge buffer on Si substrate is caused by misfit of the thermal expansion coefficient after 800°C annealing. These strains can further enhance the electron mobility in channels.

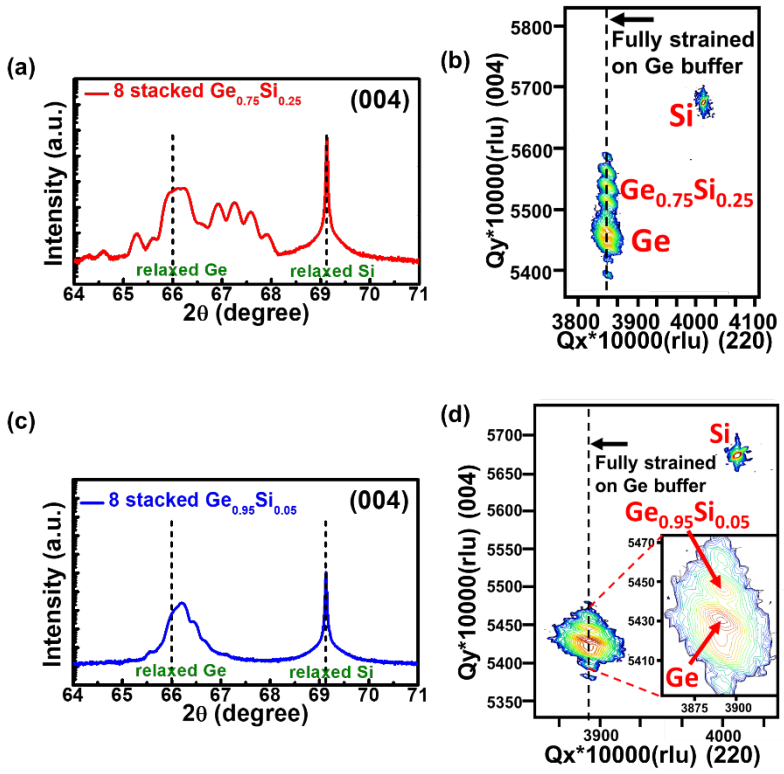

Fig. 3-5 HRXRD of the 2 as-grown epilayers with 8 stacked (a) $Ge_{0.75}Si_{0.25}$ and (c) $Ge_{0.95}Si_{0.05}$ channels. RSM of the 2 as-grown epilayers with 8 stacked (b) $Ge_{0.75}Si_{0.25}$ and (d) $Ge_{0.95}Si_{0.05}$ channels. [21-22]

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Secondary ion mass spectrometry (SIMS) profiles show the distribution of phosphorus dopants in the GeSi channels (**Fig. 3-6**), with the lowest [P] concentration at the top channel due to the shorter growth time that being heated in the chamber during epitaxy. We design no doping in channels in order to reduce impurity scattering, which further improve the device performance. In S/D region, the dopant in Ge can diffuse around, so the whole S/D resistance would be reduced.

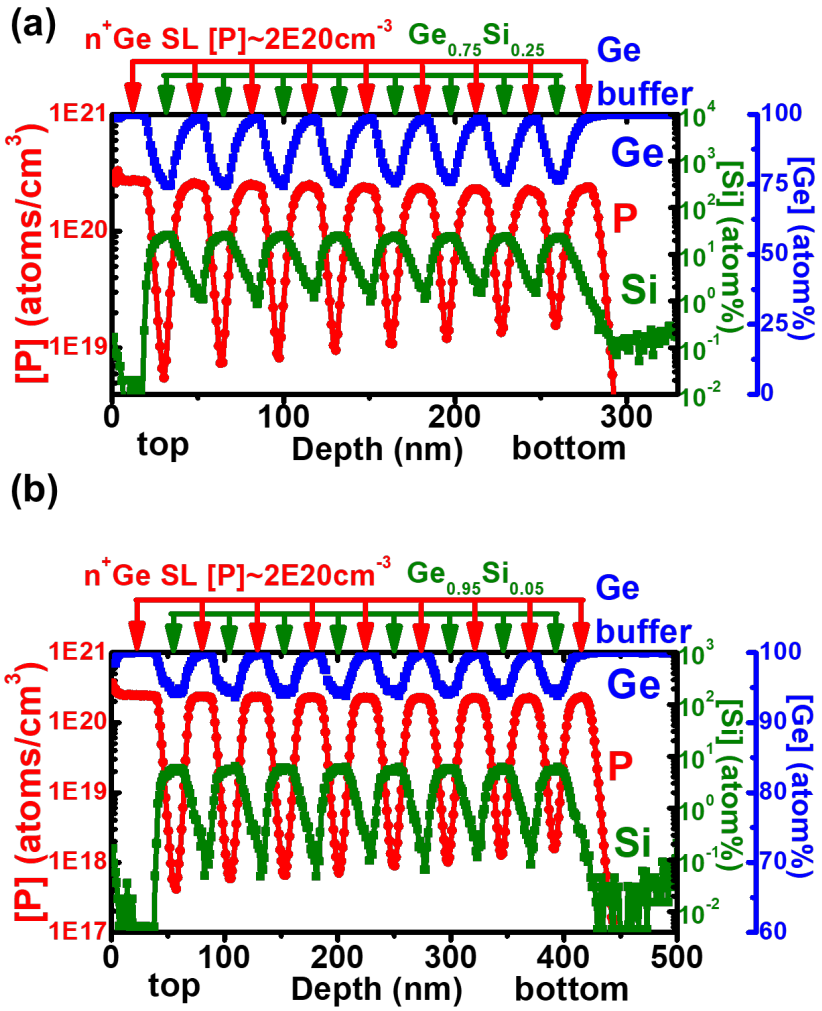

Fig. 3-6 SIMS of the 2 as-grown epilayers with 8 stacked (a) $Ge_{0.75}Si_{0.25}$ and (b) $Ge_{0.95}Si_{0.05}$ channels. [21-22]

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After epitaxial growth, a SiO_2 hard mask is deposited, and e-beam lithography is employed to pattern the channel and source/drain regions. Reactive ion etching is used to form the fin structures, and a field oxide (FOX) layer is deposited and patterned to protect the released channels. Scanning Electron Microscope (SEM) would be used to check the fin structure. (**Fig. 3-7**) shows the SEM images of the devices. Wet etching with H_2O_2 and $NH_4OH + H_2O_2$ is performed to remove the SOI and sacrificial layers, respectively, in the channel regions.

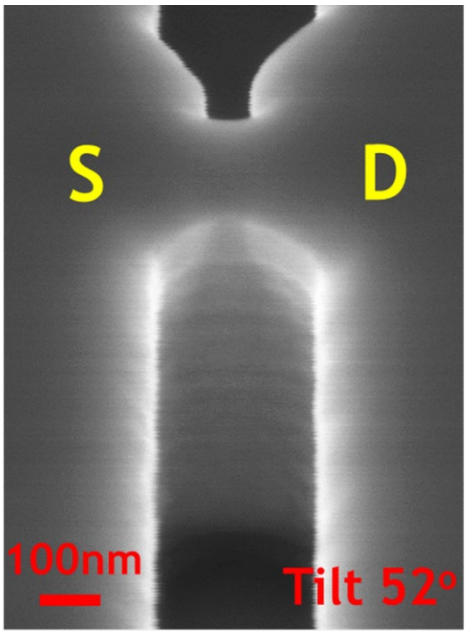

Fig. 3-7 Tilt 52° SEM images of fin structure. [21-22]

To prepare the GeSi channels for gate stack formation, a native oxide removal step is performed using a diluted HCl solution to ensure low surface roughness of the GeSi channels [32]. In-situ passivation with trimethylaluminum (TMA) reduces the interface trap density [33-34], followed by the conformal deposition of Al_2O_3 and ZrO_2 using

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plasma-enhanced atomic layer deposition (PEALD). Rapid thermal oxidation (RTO) is employed to form an interfacial layer at the Al_2O_3/GeSi interface because it can reduce interfacial layer at Al_2O_3/GeSi surface to reduce D_{it} [35]. TiN and ZrO_2 are deposited as the high-k gate stack, and forming gas annealing (FGA) at 400 °C crystallizes the ZrO2 layer for a large k value [36].

The fabrication is completed with the deposition of a thick sputter TiN layer as the gate metal pad and the formation of source/drain contacts using Pt deposition and post-metal annealing (PMA) at 400 °C. The final annealing process can drive phosphorus [37] from P-doped SLs into undoped GeSi channel layer in the S/D region and improve dopant activation for low S/D resistance.

The proposed fabrication process enables the creation of highly stacked GeSi nGAAFETs with improved electron mobility and reduced source/drain resistance.

3.4 Summary

The proposed fabrication process enables the creation of highly stacked GeSi nGAAFETs with enhanced electron mobility and reduced source/drain resistance. By leveraging epitaxy and advanced fabrication techniques, the devices achieve precise control over the number of channels without the need for source-drain regrowth. This approach eliminates complexity, cost, and process variability associated with regrowth

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techniques. The resulting GeSi nGAAFETs hold promise for high-performance semiconductor devices and integrated circuits, paving the way for advancements in IC technology.

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Chapter 4 Electrical Properties, Device Images, Strain Simulation of GeSi Nanosheets and Nanowires

4.1 Introduction

After the carefully performed fabrication process of GeSi nanosheets and nanowires, it becomes essential to assess their electrical properties comprehensively. The evaluation includes crucial parameters such as I_{ON}, I_{OFF}, I_{ON} to I_{OFF} ratio, threshold voltage (V_t), and subthreshold swing (SS), which can be obtained from the I_d-V_{gs} and I_d-V_d transfer curves. The measured electrical characteristics provide valuable insights into the performance capabilities and efficiency of the transistors.

Given the constraints of limited resources, it becomes impractical to analyze every fabricated device individually. Therefore, we rely on advanced characterization techniques, such as transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDX), to gain a deeper understanding of why certain devices are successful. These techniques allow us to examine the dimensions and distribution of material elements within the GeSi nanosheets and nanowires, providing valuable information on the structural properties of the devices.

In 4.2, we aim to investigate the electrical properties of GeSi nanosheets and

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nanowires comprehensively. By analyzing the transfer characteristics using the Keithley S4200 semiconductor system, we seek to characterize the performance of the devices, including their I_{ON}, I_{OFF}, I_{ON} to I_{OFF} ratio, Vt, and SS. Additionally, through TEM and EDX analysis, we will gain insights into the factors that contribute to the success of the fabricated devices, enabling us to optimize the fabrication process further. Following in 4.3, we investigate the effect of parasitic channel in I-V characteristics. Last but not least, microbridge effect, strain simulation result, and the discussion between the two is presented.

4.2 Device Images and Electrical Properties of Nanosheets and Nanowires

The transmission electron microscopy (TEM) images depicts the highly uniform structure of 8 stacked $Ge_{0.75}Si_{0.25}$ nanosheets, exhibiting consistent well-controlled channel height (H_{CH}) and width (W_{CH}), along with the complete removal of the heavily phosphorus-doped germanium ($n^{+}Ge$) sacrificial layers (SLs) after channel release via wet etching with H_2O_2 (**Fig. 4-1**). The $Ge_{0.75}Si_{0.25}$ nanosheets are enclosed by gate dielectrics and in-situ titanium nitride (TiN) layers, ensuring the confirmation of the gate-all-around (GAA) structure through energy-dispersive X-ray spectroscopy (EDS/EDX) mapping (**Fig. 4-2**). The 8 stacked $Ge_{0.75}Si_{0.25}$ nanosheets, each with a gate

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length (L_g) of 80nm, exhibit an ON-current (I_{ON}) of 36μA per stack (equivalent to 390μA/μm per channel footprint) at a gate overdrive voltage (VOV) and drain-to-source voltage (VDS) of 0.5V, with a subthreshold swing (SS) of 121mV/dec (**Fig. 4-3**). It is important to note that the I_{ON} per channel footprint in this study is normalized based on the channel width (W_{CH} = 93nm).

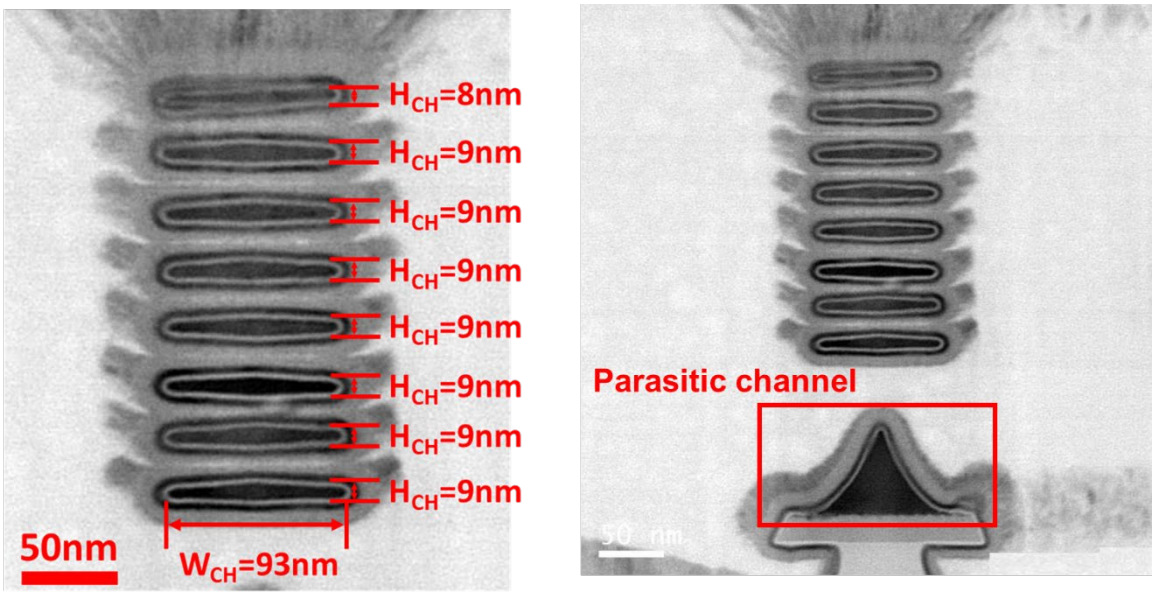

Fig. 4-1 TEM image of 8 stacked $Ge_{0.75}Si_{0.25}$ nanosheet device. [21-22]

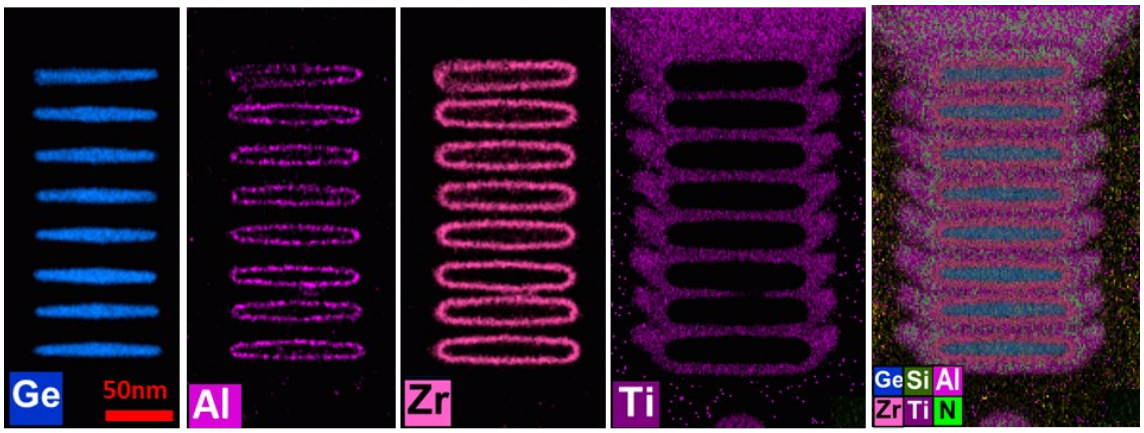

Fig. 4-2 EDX mapping of 8 stacked $Ge_{0.75}Si_{0.25}$ nanosheet device. [21-22]

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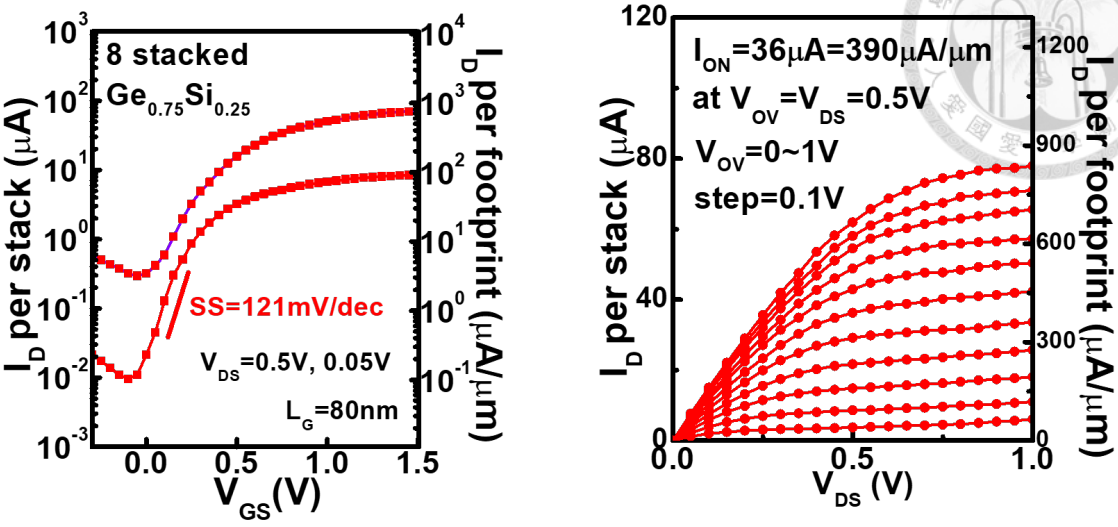

Fig. 4-3 I_D–V_{GS} and I_D–V_{DS} of 8 stacked $Ge_{0.75}Si_{0.25}$ nanosheet device. [21-22]

(**Fig. 4-4**) illustrates the $Ge_{0.95}Si_{0.25}$ nanowires, revealing a device configuration with 7 stacked channels after the removal of the parasitic bottom channel through wet etching using NH_4OH and H_2O_2. The $Ge_{0.95}Si_{0.05}$ nanowires are encompassed by gate dielectrics and in-situ TiN layers, ensuring the GAA structure confirmation through EDX mapping (**Fig. 4-5**). However, as you can see in the both images, the channel at the very bottom has a channel height of 27nm which is higher than its epitaxy channel layer thickness (24nm). It means that the SLs are not fully removed. The 7 stacked $Ge_{0.95}Si_{0.05}$ nanowires, each with a L_g of 70nm, exhibit an I_{ON} of 128μA per stack (equivalent to 5800μA/μm per channel footprint) at $V_{OV} = V_{DS} = 0.5V$, with a SS of 112mV/dec (**Fig. 4-6**). It should be noted that the I_{ON} per channel footprint for the nanowire device is normalized based on the maximum channel width (W_{CH} = 22nm).

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Due to the narrower width of the nanowire, the drain current (ID) per footprint is significantly higher compared to the nanosheet device.

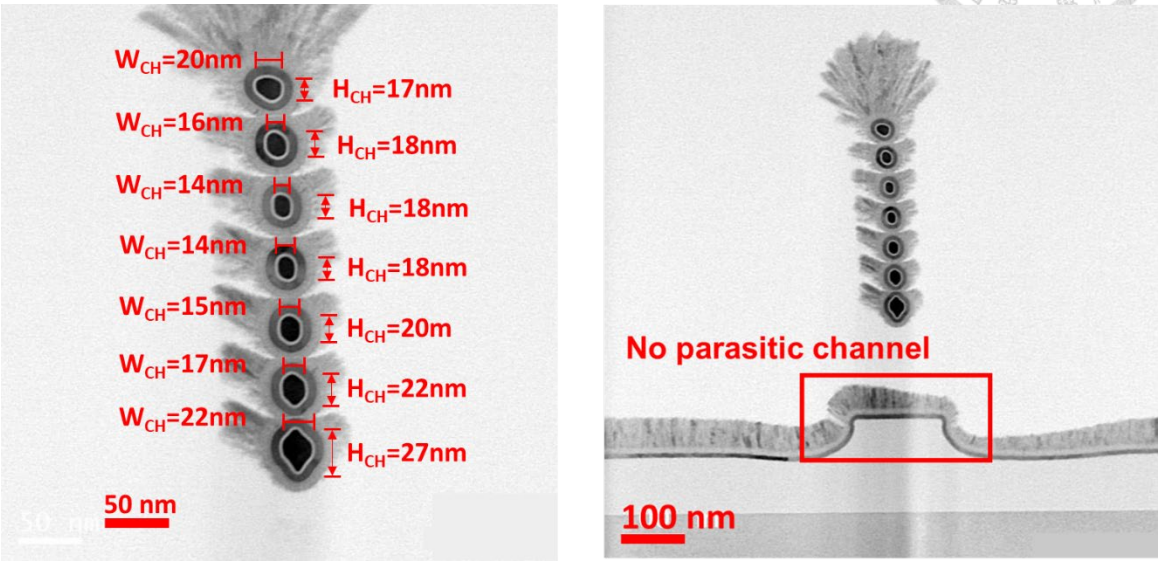

Fig. 4-4 TEM image of 7 stacked $Ge_{0.95}Si_{0.05}$ nanowire device without parasitic channel

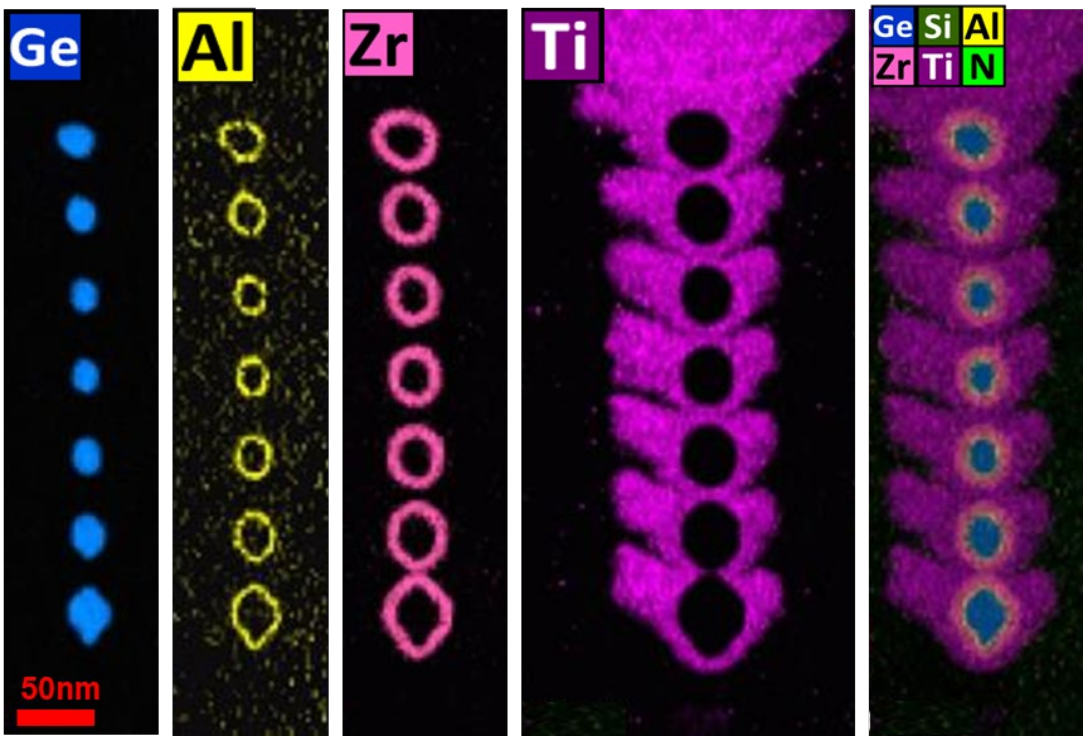

Fig. 4-5 EDX mapping of 7 stacked $Ge_{0.95}Si_{0.05}$ nanowire device without parasitic channel

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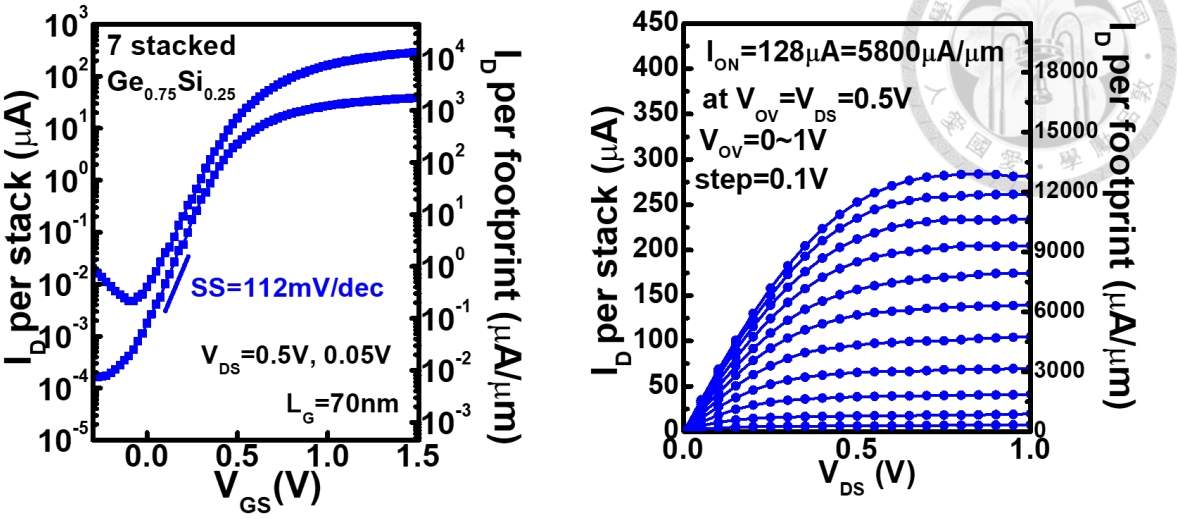

Fig. 4-6 I_D–V_{GS} and I_D–V_{DS} of 7 stacked $Ge_{0.95}Si_{0.05}$ nanowire device without parasitic channel

These findings demonstrate the successful fabrication of highly stacked GeSi nanosheets and nanowires with precise dimensions and controlled structural properties. The resulting devices exhibit desirable electrical characteristics, such as high I_{ON} and low SS, paving the way for advanced nanoscale transistor applications in semiconductor technology.

4.3 Parasitic Channel

In $Ge_{0.75}Si_{0.25}$ nanosheet device, as you can see in (**Fig. 4-1**), there is a parasitic channel composed of residual Ge buffer and SOI. It's because we use H_2O_2 only to do the channel release process. In $Ge_{0.95}Si_{0.05}$ nanowire device, Ge buffer and SOI are totally removed by NH_4OH in channel release step, confirmed by the (**Fig. 4-4).**

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When measuring a transistor, I-V characteristic, it's important to observe the I_{ON} / I_{OFF} (on to off current ratio). I_{ON} /I_{OFF} ratio provides insights into the efficiency, power consumption, and performance capabilities of a transistor. A higher I_{ON} / I_{OFF} ratio signifies improved control, reduced leakage current, enhanced power efficiency, and broader applicability in various electronic applications.

But in the 7 stacked $Ge_{0.95}Si_{0.05}$ nanowire device (**Fig. 4-6**), the SS and I_{ON} /I_{OFF} ratio are not good as the results of our previous work [22-23]. It is because the the bottom SLs are not fully removed, as you can see in (**Fig. 4-4**). The channel height of the bottom channel is 27nm which is higher than the original epitaxy layers thickness design (24nm).

Back to parasitic channel, its results and effects in I-V characteristics is illustrated in [22-23] by similar devices. In the I_{OFF} region, the current is dominated by the leakage current of parasitic channel and that means parasitic would do harm to I_{ON} / I_{OFF} ratio because our channels should perform lower current in I_{OFF} region due to its better gate control (**Fig. 4-7**). On the other hand, parasitic channel only contributed to I_{ON} at a lower level (5%).

If we can successfully remove the parasitic channel and maintain a good channel, as we can see in (**Fig. 4-8**). The SS of the is improved from 90 to 80 mV/dec. The I_{ON}/I_{OFF} is also improved in about one order.

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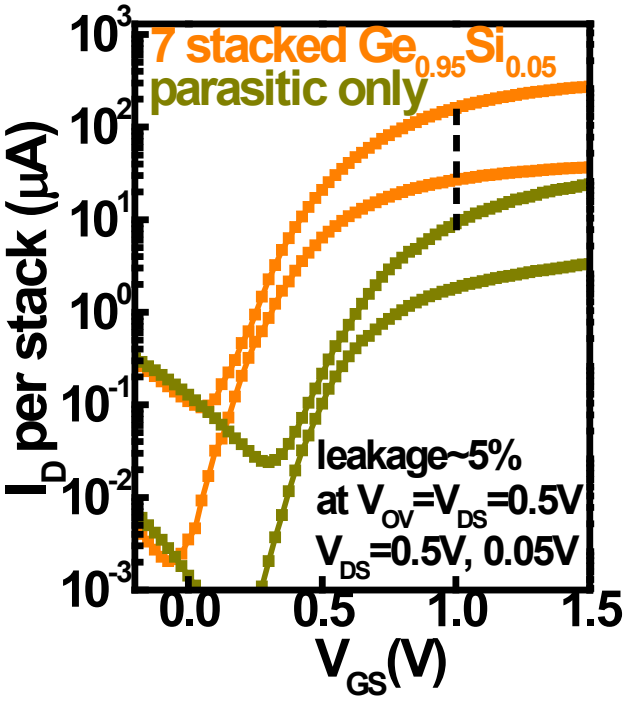

Fig. 4-7 The current of parasitic channel only contributes about 5% to I_{ON} at $V_{OV} = V_{DS} = 0.5$ V, but dominates the I_{OFF} current. [22-23]

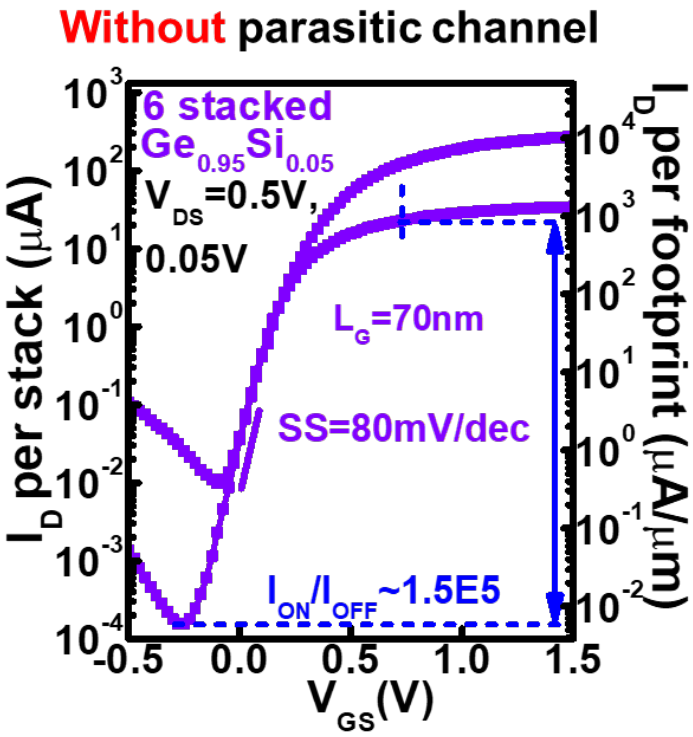

Fig. 4-8 SS and I_{ON}/I_{OFF} are both improved in the nanowire device without parasitic channel. [22-23]

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4.4 Strain Simulation

4.4.1 Microbridge Effect

Following the channel release step, the floating channels within the device can experience additional tensile strain through the microbridge structure, as simulated using ANSYS software [38]. The biaxial tensile strain present transforms into uniaxial strain due to the lattice mismatch between GeSi and Ge induced by the microbridge structure. In order to accurately extract the external tensile strain, strain simulations are performed using ANSYS Mechanical APDL. It is essential to ensure that the simulation results align with theoretical calculations to ensure the reliability and consistency of the ANSYS simulation tools for strain analysis in the nanoscale microbridge device.

The mechanisms and effects of the microbridge structure is based from refence [39-43]. The theory parameters include wire length (A), wire width (a), bridge length (B), bridge width (b), bridge length after strain enhancement (B'), initial biaxial (ε_0), and uniaxial strain along x (ε_{xx}). The formula derivation can be easily found in the reference. By the formula:

$$\text{Enhance Factor(EF)} = \frac{\varepsilon_{xx}{}^{A}}{\varepsilon_0} = \frac{1+\frac{A}{B-A}}{\frac{a}{b}+\frac{A}{B-A}}$$

We can have the ideal enhance factor (EF) according to the device e-beam pattern dimension of the $Ge_{0.75}Si_{0.25}$ nanosheet device to be 1.58.

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4.4.2 $Ge_{0.75}Si_{0.25}$ nanosheet Strain Simulation Results

In the strain simulation, we construe the device model (**Fig. 4-8**) and run the simulation in line with the real device dimension from epitaxy TEM for S/D epitaxy thickness (**Fig. 3-4 (a)**), e-beam pattern design for gate length and S/D region shape and dimension, and channel TEM for channel height and width (**Fig. 4-1**). It shows that after fin formation, the tensile strain along <110> channel direction is 1.3% (**Fig. 4-9**). After nanosheet formation, by virtue of the microbridge structure, the uniaxial tensile strain at the channel center is enlarged to 1.7%, to further enhance electron mobility.

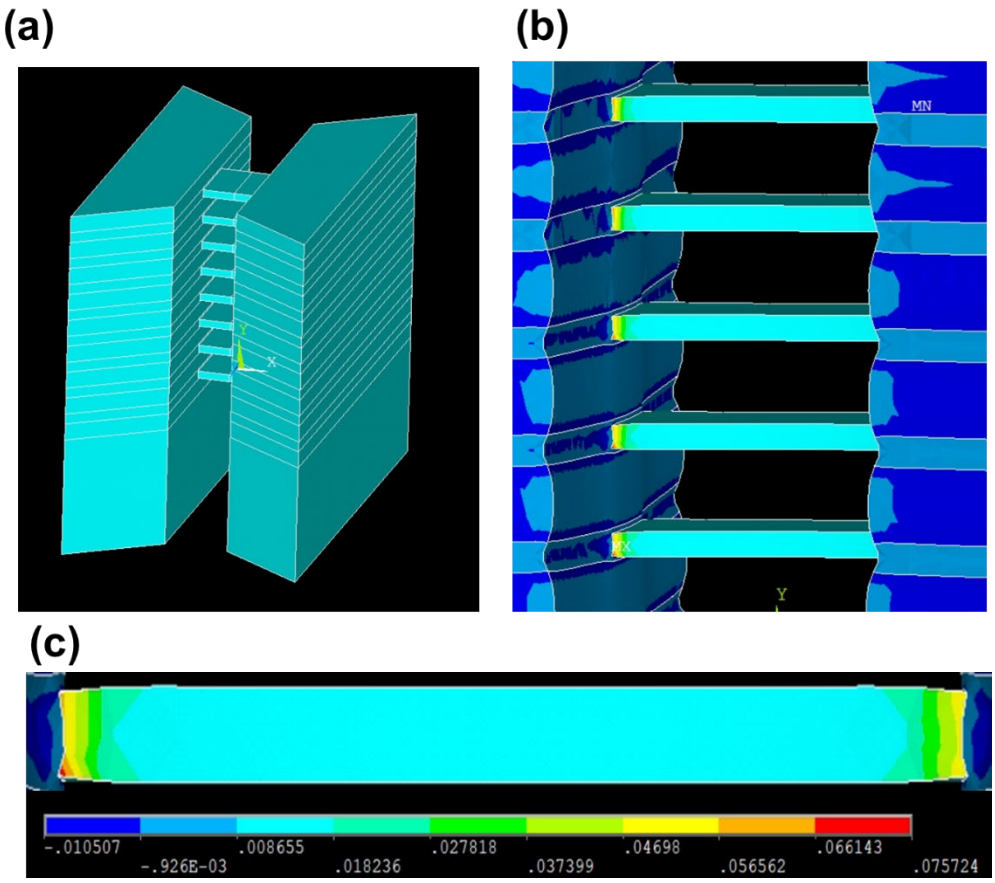

Fig. 4-9 (a) Device model schematic (b) zoom-in view of the channels (c) strain distribution in one channel

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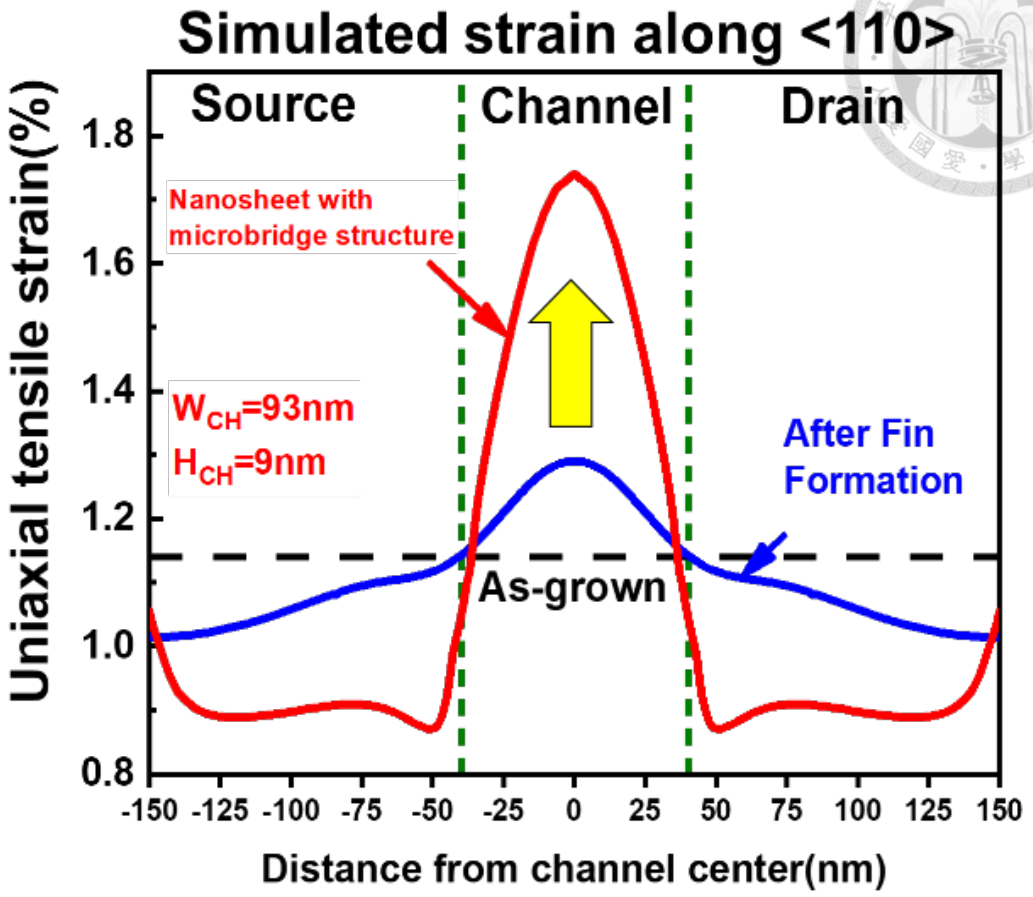

Fig. 4-10 Simulated strain of the channel along <110> by ANSYS. The tensile strain at the channel center are 1.3% and 1.7% after fin and nanosheet formation respectively.

To verify the ideal microbridge effect on our device, it's necessary to get the as grown tensile strain from RSM data, which is 1.14% in $Ge_{0.75}Si_{0.25}$ and 0.14% in Ge. The 1% difference is calculated by the [Si] (25%) times the lattice mismatch between Ge and Si (4%) because it is fully strain on Ge. Therefore, we can have the EF of the device to be 1.49X, similar to 1.58X in theory calculation. These findings clearly point out the benefit of microbridge effect that would improve tensile strain and then electron mobility, bringing better performance.

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4.5 Summary

The carefully fabricated GeSi nanosheets exhibited a highly uniform structure, and their electrical properties were characterized using the Keithley S4200 semiconductor system. The measurements revealed desirable characteristics such as high I_{ON} in both two kinds of devices. Additionally, TEM and EDX analysis provided valuable insights into the dimensions and distribution of material elements within the nanosheets and nanowires. The results of the nanosheet and nanowire device is shown in **Table 1-1**.

items	8 stacked $Ge_{0.75}Si_{0.25}$ Nanosheet FET	7 stacked $Ge_{0.95}Si_{0.05}$ Nanowire FET
I_{ON} per stack	36μA at $V_{OV}=V_{DS}=0.5V$	128μA at $V_{OV}=V_{DS}=0.5V$
I_{ON} per footprint	390μA/μm at $V_{OV}=V_{DS}=0.5V$	5800μA/μm at $V_{OV}=V_{DS}=0.5V$
Footprint	93nm	22nm
SS at $V_{DS}=0.05V$	121 mV/dec	112 mV/dec
Channel Release Recipe	H_2O_2	$NH_4OH+H_2O_2$
Parasitic channel	YES	NO

Table 1-1 Comparison of the device performance of 8 stacked $Ge_{0.75}Si_{0.25}$ Nanosheet FET and 7 stacked $Ge_{0.95}Si_{0.05}$ Nanowire FET

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We also investigated the presence of parasitic channels in the GeSi nanowire devices. The parasitic channel was found to be composed of residual Ge buffer and SOI, which affected the I-V characteristics of the transistors. The presence of the parasitic channel contributed to higher I_{OFF} currents, resulting in a reduced I_{ON} / I_{OFF} ratio and compromised gate control.

Furthermore, we explored the microbridge effect and its impact on strain simulation. Through ANSYS software simulations, we observed that the microbridge structure induced additional tensile strain in the floating channels of the devices, leading to enhanced electron mobility. The theoretical calculations and simulation results demonstrated the effectiveness of the microbridge structure in improving device performance. And compared to theory, our simulation results fit quite well with the calculation predictions.

In short, we focused on assessing the electrical properties of GeSi nanosheets and nanowires and understanding the impact of parasitic channels and strain simulation on device performance.

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Chapter 5 Summary and Future Work

5.1 Summary

This thesis begins with a brief recap of the research objectives and the methodology employed to achieve them. We summarize the key findings and contributions of the thesis, emphasizing the successful fabrication of highly stacked GeSi nanosheets and nanowires for GAA FETs. Highlights include the significance of material selection, epitaxial structure design, and selective etching in achieving the desired stacked channel structures. Due to the negative effect of parasitic channel in I_{OFF}, we underscore the importance of optimizing process parameters and addressing challenges related to parasitic channels.

Furthermore, we provide an overview of the electrical characteristics and mobility enhancement by microbridge effect achieved in the fabricated GeSi devices. It emphasizes the superior performance of the devices and their potential for application in advanced ICs.

5.2 Future Work

In terms of future work, the chapter identifies several areas that warrant further investigation and improvement. These include:

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1. Optimization of epitaxial growth parameters: The research can focus on refining the epitaxial growth process to enhance the crystalline quality and strain engineering in GeSi channel layers. Exploring different growth techniques and doping profiles may lead to further performance improvements.

2. Device scaling and integration: Investigating the scalability of the fabricated GeSi nanosheets and nanowires to smaller dimensions (ex: channel thickness and L_g) is crucial. There are many works undergoing [44-46], looking forward to scaling down channel thickness.

3. Device architecture evolution: It is already predicted that Complementary FET (CFET) is going to replace GAAFET someday and some research already has started to work on CFET [47-48]. Thus, next step we should build better CFET integrating nGAAFET and pGAAFET. Every process would need to be research deeper to make the advance of CFET sooner.

doi:10.6342/NTU202301581

Reference

[1] G. E. Moore, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff.," in IEEE Solid-State Circuits Society Newsletter, vol. 11, no. 3, pp. 33-35, Sept. 2006, doi: 10.1109/N-SSC.2006.4785860.

[2] Taur, Y., & Ning, T. (2021). *Fundamentals of Modern VLSI Devices* (3rd ed.). Cambridge: Cambridge University Press. doi:10.1017/9781108847087

[3] D. Hisamoto et al., "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," in IEEE Transactions on Electron Devices, vol. 47, no. 12, pp. 2320-2325, Dec. 2000, doi: 10.1109/16.887014.

[4] S. Bangsaruntip et al., “High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling,” in IEDM Tech. Dig., Dec. 2009, pp. 297–300, doi:10.1109/IEDM.2009.5424364.

[5] I. Lauer et al., “Si nanowire CMOS fabricated with minimal deviation from RMG FinFET technology showing record performance,” in Proc. Symp. VLSI Technol. (VLSI Technology), Jun. 2015, pp. T140–T141, doi:10.1109/VLSIT.2015.7223653.

doi:10.6342/NTU202301581

[6] N. Loubet et al., “Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET,” in Symp. VLSI Technol. Dig. Tech. Papers, Jun. 2017, pp. T230–T231, doi: 10.23919/VLSIT.2017.7998183.

[7] M. Y. Liu, “Breaking the Limitations of FinFET Scaling” in Symp. VLSI Short course on CMOS Technology Enablers for Pushing the Limits of Semiconductors: Materials to Packing, 2019.

[8] Jean-Pierre Colinge, “Multiple-gate SOI MOSFETs,” *Solid-State Electronics*, Volume 48, Issue 6, Pages 897-905, 2012.

[9] K. J. Kuhn, “Considerations for Ultimate CMOS Scaling,” in IEEE Transactions on Electron Devices, vol. 59, no. 7, pp. 1813-1828, July 2012, doi: 10.1109/TED.2012.2193129.

[10] intel, “Accelerated”, 2021, https://www.intc.com/news-events/press-releases/detail/1481/media-alert-intel-accelerated-webcast-on-july-26

[11] S. Barraud et al., “7-levels-stacked nanosheet GAA transistors for high performance computing,” in Proc. IEEE Symp. VLSI Technol., Jun. 2020, pp. 1–2, doi: 10.1109/VLSITechnology18217.2020.9265025.

[12] Amy Fan, Willis Ke " Samsung 3nm GAA commercialization signifies paradigm shift in transistor architecture." DIGITIMES Asia, 4 July 2022, https://www.digitimes.com/news/a20220704PD201/3nm-samsung.html.

doi:10.6342/NTU202301581

[13] “IEEE International Roadmap for Devices and Systems,” 2021.

[14] imec, “20-year semiconductor roadmap: tearing down the walls.”, August 2022

[15] Samsung, “Foundry Roadmap”, Foundry Forum, 2022

[16] TSMC, North America Technology Symposium, 2023

[17] intel, “A New Paradigm for Moore's Law”, 2022, https://www.intel.com.tw/content/www/tw/zh/silicon-innovations/6-pillars/process.html

[18] G. Yeap et al., "5nm CMOS Production Technology Platform featuring full-fledged EUV, and High Mobility Channel FinFETs with densest 0.021μm2 SRAM cells for Mobile SoC and High Performance Computing Applications," 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019, pp. 36.7.1-36.7.4, doi: 10.1109/IEDM19573.2019.8993577.

[19] M. Liu, "1.1 Unleashing the Future of Innovation," 2021 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021, pp. 9-16, doi: 10.1109/ISSCC42613.2021.9366060.

[20] S. Barraud, B. Previtali, C. Vizioz, J.-M. Hartmann, J. Sturm, J. Lassarre, C. Perrot, Ph. Rodriguez, V. Loup, A. Magalhaes-Lucas, R. Kies, G. Romano, M. Cassé, N. Bernier, A. Jannaud, A. Grenier, F. Andrieu, “7-Levels-Stacked Nanosheet GAA Transistors for High Performance Computing,” 2020 IEEE

doi:10.6342/NTU202301581

Symposium on VLSI Technology, 2020, pp. 1-2, doi: 10.1109/VLSITechnology18217.2020.9265025.

[21] Yi-Chun Liu et al., "First Highly Stacked $Ge_{0.95}Si_{0.05}$ nGAAFETs with Record ION = 110 μA (4100 μA/μm) at VOV=VDS=0.5V and High Gm,max = 340 μS (13000 μS/μm) at VDS=0.5V by Wet Etching," Symposia on VLSI Technology and Circuits (VLSI), T15-2 (2021)

[22] Y. -C. Liu et al., "Highly Stacked GeSi Nanosheets and Nanowires by Low-Temperature Epitaxy and Wet Etching," in IEEE Transactions on Electron Devices, vol. 68, no. 12, pp. 6599-6604, Dec. 2021, doi: 10.1109/TED.2021.3110838.

[23] C. -Y. Cheng et al., "6 Stacked $Ge_{0.95}Si_{0.05}$ nGAAFETs without Parasitic Channels by Wet Etching," 2022 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), Hsinchu, Taiwan, 2022, pp. 1-2, doi: 10.1109/VLSI-TSA54299.2022.9770969.

[24] C.W. Liu, M. Östling, and J.B. Hannon, "New Materials for Post-Si Computing", MRS Bulletin, Vol. 39, No. 8, pp. 658-662, August, 2014. https://doi.org/10.1557/mrs.2014.162

[25] Modern Semiconductor Devices for Integrated Circuits (C. Hu)

doi:10.6342/NTU202301581

[26] Manoranjan Ghosh, Shreyas Pitale, S.G. Singh, Husain Manasawala, Vijay Karki, Manish Singh, Kulwant Singh, G.D. Patra, Shashwati Sen, Fabrication of p+ contact by thermally induced solid state regrowth of Al on p-type Ge crystal, Materials Science in Semiconductor Processing, Volume 121, 2021, https://doi.org/10.1016/j.mssp.2020.105350.

[27] Xie, L.; Zhu, H.; Zhang, Y.; Ai, X.; Wang, G.; Li, J.; Du, A.; Kong, Z.; Yin, X.; Li, C.; et al. Strained Si0.2Ge0.8/Ge multilayer Stacks Epitaxially Grown on a Low-/High-Temperature Ge Buffer Layer and Selective Wet-Etching of Germanium. Nanomaterials 2020, 10, 1715, https://doi.org/10.3390/nano10091715

[28] H. Inge et. al., ECS Transactions, 2007, 6. 10.1149/1.2731205.

[29] F. Wang, Y. Shi, J. Liu, Y. Lu, S. Gu, and Y. Zheng, “Highly selective chemical etching of Si vs. Si1−X GeX using NH_4OH solution,” J. Electrochem. Soc., vol. 144, no. 3, pp. L37–L39, Mar. 1997, doi: 10.1149/1.1837485.

[30] Marc J. Madou. Fundamentals of Microfabrication (1st ed.). CRC-Press., 1997, ISBN 10: 0849394511

[31] W. Feng, et al., Journal of the Electrochemical Society 144.3, 1997, L37.

doi:10.6342/NTU202301581

[32] D. D. Cannon et al., “Tensile strained epitaxial Ge films on Si(100) substrates with potential application in L-band telecommunications,”Appl. Phys. Lett., vol. 84, no. 6, pp. 906–908, Feb. 2004, doi:10.1063/1.1645677.

[33] S. Sun, Y. Sun, Z. Liu, D.-I. Lee, S. Peterson, and P. Pianetta, “Surface termination and roughness of Ge(100) cleaned by HF and HCl solutions,”Appl. Phys. Lett., vol. 88, no. 2, Jan. 2006, Art. no. 021903, doi:10.1063/1.2162699.

[34] T.-E. Lee, K. Kato, M. Ke, M. Takenaka, and S. Takagi, “Improvement of SiGe MOS interface properties with a wide range of Ge contents by using TiN/Y2O3 gate stacks with TMA nassivation,”in Proc. Symp. VLSI Technol., Jun. 2019, pp. T100–T101, doi:10.23919/VLSIT.2019.8776523.

[35] T.-E. Lee, M. Ke, K. Toprasertpong, M. Takenaka, and S. Takagi, “Reduction of MOS interface defects in TiN/Y2O3/Si0.78Ge0.22 structures by trimethylaluminum treatment,”IEEE Trans. Electron Devices, vol. 67, no. 10, pp. 4067–4072, Oct. 2020, doi: 10.1109/TED.2020.3014563.

[36] Y.-S. Huang et al., “High-mobility CVD-grown Ge/strained Ge0.9Sn0.1/Ge quantum-well pMOSFETs on Si by optimizing Ge cap thickness,” IEEE Trans. Electron Devices, vol. 64, no. 6, pp. 2498–2504, Jun. 2017, doi: 10.1109/TED.2017.2695664

doi:10.6342/NTU202301581

[37] J.-H. Kim, V. Ignatova, P. Kücher, J. Heitmann, L. Oberbeck, and U. Schröder, "Physical and electrical characterization of high-K ZrO2 metal–insulator–metal capacitor," Thin Solid Films, vol. 516, no. 23, pp. 8333–8336, Oct. 2008, doi: 10.1016/j.tsf.2008.03.051.

[38] A. Chroneos, R. W. Grimes, and C. Tsamis, "Atomic scale simulations of arsenic–vacancy complexes in germanium and silicon," Mater. Sci. Semicond. Process., vol. 9, nos. 4–5, pp. 536–540, Aug. 2006, doi:10.1016/j.mssp.2006.08.059.

[39] M. J. Suess, R.Geiger, R.A.Minamisawa, G. Schiefler, J.Frigerio, D. Chrastina, G. Isella, R. Spolenak, J.Faist, and H. Sigg, "Analysis of enhanced light emission from highly strained germanium microbridges." Nature Photonics 7.6 (2013): 466-472.

[40] Minamisawa, R., Süess, M., Spolenak, R. et al. Top-down fabricated silicon nanowires under tensile elastic strain up to 4.5%. Nat Commun 3, 1096 (2012). https://doi.org/10.1038/ncomms2102

[41] Süess, Martin & Geiger, Richard & Minamiswa, Renato & Schiefler, Gustav & Frigerio, Jacopo & Chrastina, Daniel & Isella, Giovanni & Spolenak, Ralph & Faist, Jérôme & Sigg, Hans. (2013). Analysis of enhanced light emission from

doi:10.6342/NTU202301581

highly strained germanium microbridges. Nature Photonics. 7. 466-472. 10.1038/nphoton.2013.67.

[42] A. Agrawal et al., "Gate-All-Around Strained Si0.4Ge0.6 Nanosheet PMOS on Strain Relaxed Buffer for High Performance Low Power Logic Application," 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2020, pp. 2.2.1-2.2.4, doi: 10.1109/IEDM13553.2020.9371933.

[43] R. Tiwari, N. Parihar, K. Thakor, H. -Y. Wong and S. Mahapatra, "TCAD Framework to Estimate the NBTI Degradation in FinFET and GAA NSFET Under Mechanical Strain," 2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Udine, Italy, 2019, pp. 1-4, doi: 10.1109/SISPAD.2019.8870523.

[44] C. -E. Tsai et al., "Nearly Ideal Subthreshold Swing and Delay Reduction of Stacked Nanosheets Using Ultrathin Bodies," 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2022, pp. 401-402, doi: 10.1109/VLSITechnologyandCir46769.2022.9830357.

[45] B. -W. Huang et al., "Highly Stacked GeSn Nanosheets by CVD Epitaxy and Highly Selective Isotropic Dry Etching," in IEEE Transactions on Electron Devices, vol. 69, no. 4, pp. 2130-2136, April 2022, doi: 10.1109/TED.2022.3144105.

doi:10.6342/NTU202301581

[46] C. -E. Tsai et al., "Highly Stacked 8 Ge0.9Sn0.1 Nanosheet pFETs with Ultrathin Bodies (~3nm) and Thick Bodies (~30nm) Featuring the Respective Record ION/IOFF of 1.4x107 and Record ION of 92μA at Vov=VDS= -0.5V by CVD Epitaxy and Dry Etching," 2021 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2021, pp. 26.4.1-26.4.4, doi: 10.1109/IEDM19574.2021.9720660.

[47] C. -T. Tu, Y. -C. Liu, Y. -R. Chen, B. -W. Huang, C. -Y. Cheng and C. W. Liu, "Nanosheet Extensions and Beyond," 2023 International VLSI Symposium on Technology, Systems and Applications (VLSI-TSA/VLSI-DAT), HsinChu, Taiwan, 2023, pp. 1-1, doi: 10.1109/VLSI-TSA/VLSI-DAT57221.2023.10134258.

[48] C. -T. Tu et al., "First Demonstration of Monolithic 3D Self-aligned GeSi Channel and Common Gate Complementary FETs by CVD Epitaxy Using Multiple P/N Junction Isolation," 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2022, pp. 20.3.1-20.3.4, doi: 10.1109/IEDM45625.2022.10019532.

doi:10.6342/NTU202301581