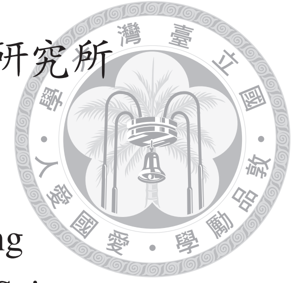

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National Taiwan University

Doctoral Dissertation

氧化層電荷對金氧半穿隧二極體在反轉區之電流及電容特性之影響

Impact of Oxide Charges on the Current and Capacitance Characteristics of Metal-Insulator-Semiconductor Tunneling Diode in Inversion Region

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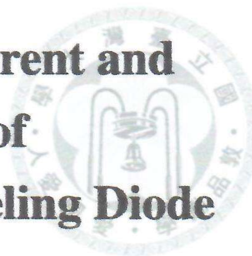

By

Kuan-Chu Chen

DISSERTATION

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摘要

本論文討論了氧化層電荷對於鋁/二氧化矽/p 型矽之金屬-氧化層-半導體穿隧二極體 (金氧半穿隧二極體) 在反偏壓下電氣特性的影響。我們提出了三個模型分別討論了金氧半穿隧二極體的高頻電容、電流及變頻電容特性。每一項特性皆經過實驗量測的驗證。我們的實驗使用了半徑 85 微米的圓形金氧半穿隧二極體，氧化層厚度大約在 25 埃，基板摻雜濃度爲 10^{16} cm^{-3}。首先，我們討論了金氧半穿隧二極體的高頻電容特性。臨界電壓的決定對於高頻電容特性至關重要。在施加電壓小於臨界電壓時，金氧半穿隧二極體的高頻電容特性和傳統金氧半電容類似。然而，當施加電壓大於臨界電壓時，金氧半穿隧二極體會進入深空乏區，其高頻電容特性變得類似於蕭特基二極體。我們推導了一個模型以解釋氧化層電荷和氧化層厚度對於臨界電壓的影響。對我們的元件而言，2.8×10^{11} cm^{-2} 的氧化層電荷濃度足以引起大於 10^4 微米的横向直流耦合距離，這一極長的耦合距離會導致臨界電壓提升 1 伏特以上。接著，我們討論了金氧半穿隧二極體的電流特性。氧化層電荷會導致横向耦合並提供額外的電子補充，這會提升蕭特基能障調變的程度。顯著的蕭特基能障調變會提升電洞電流的注入甚至主導金氧半穿隧二極體的電流。我們對於蕭特基能障調變及電洞電流做了詳細的計算與探討。在我們的元件之中，2.8×10^{11} cm^{-2} 的氧化層電荷濃度足以導致蕭特基能障下降 1 電子伏特，並使總電流上升超過四個數量級。最後，我們討論了金氧半穿隧二極體的變頻電容特性。氧化層電荷會造成一個隨量測頻率變動的横向控制區。這個横向控制區會對量測到的電容值造成影響，我們建立了一個模型以討論此影響。根據我們的計算結果，在量測頻率 10kHz 之下 2.8×10^{11} cm^{-2} 的氧化層電荷濃度足以引起 53 微米的横向交

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流訊號控制區。這個大小的控制區可以使量測到的電容值上升約 50%。以上的討論強調了氧化層電荷在金氧半穿隧二極體所扮演角色的重要性。相信本論文所提出的計算與分析對於金氧半穿隧二極體的設計與認識有相當程度的幫助。

關鍵字：金氧半穿隧二極體；金氧半電容；蕭特基能障調變；深空乏；氧化層電荷；橫向耦合；解析模型；穩態。

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Abstract

This work comprehensively discusses the influences of outer oxide charges (Q_{eff}) on the electrical characteristics of Al/SiO_2/Si(p) metal-insulator-semiconductor tunnel diode (MISTD) in the reverse-biased region. Three models are proposed for the high-frequency capacitance-voltage (HFCV), current-voltage (IV), and capacitance-frequency (CF) characteristics of MISTD. For each characteristic, experiments were carried out for discussion. The measured circle devices have an oxide thickness of around 25 Å, a radius of 85 μm, and a doping concentration of 10^{16} cm^{-3}. First, the HFCV of MISTD is discussed. For HFCV, determination of critical voltage V_{C} is of importance. At $V_{\mathrm{G}} < V_{\mathrm{C}}$, where V_{G} is the bias voltage applied on metal, MISTD acts like a traditional MOS capacitor. However, at $V_{\mathrm{G}} > V_{\mathrm{C}}$, MISTD enters the deep depletion region and acts like a Schottky diode. A procedure for calculating the dependency of V_{C} on oxide charges and oxide thickness is proposed. It was founded that an amount of 2.8×10^{11} cm^{-2} of Q_{eff}/q can lead to a DC lateral decay length larger than 10^4 μm and let V_{C} increase for over 1 V. Second, the IV of MISTD is discussed. Oxide charges will enhance the supplement of electrons from the lateral region and affect the level of Schottky barrier height modulation (SBHM). Significant SBHM leads to a high hole injection current, which can dominate the current of a MISTD. Detailed calculation of SBHM and the effect on hole current are explored. It was found that an amount of 2.8×10^{11} cm^{-2} of Q_{eff}/q can let the hole's Schottky barrier height decrease

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for over 1 eV and enhance the MISTD's current for over four orders. Finally, the CF relation is discussed. Oxide charges will cause a frequency-dependent lateral control region for MISTD. The lateral control region contributes extra capacitance to the total capacitance. A model considering the impact of oxide charges on capacitance value was proposed. The calculation from our model shows that an amount of $Q_{\text{eff}}/q = 2.8 \times 10^{11}$ cm^{-2} can induce a lateral AC control distance for about 53 μm at 10 kHz and increase the measured capacitance by around 50%. The above studies highlight the importance of outer oxide charges in MISTD. It is believed that the proposed detailed calculations and analysis in this work are helpful for designing and understanding MISTD.

Keywords: MIS tunnel diode; MIS capacitor; Schottky barrier height modulation; Deep depletion; Oxide charge; Lateral coupling; Analytical model; Steady state.

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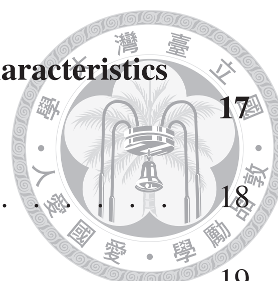

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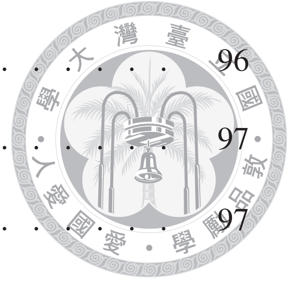

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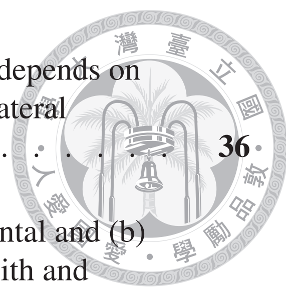

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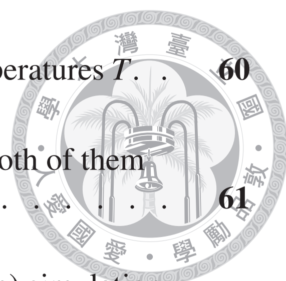

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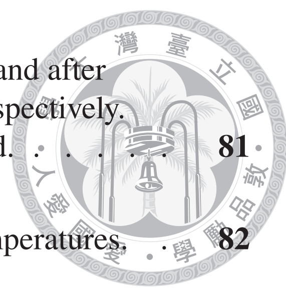

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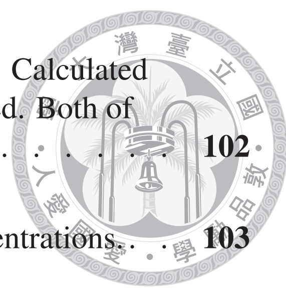

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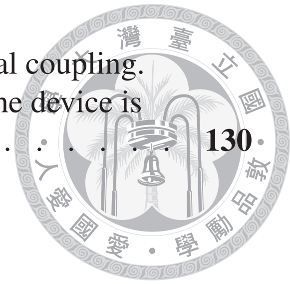

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1 Introduction

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1.1 Motivation

METAL-oxide-semiconductor field-effect transistor (MOSFET) is the most important device in very-large-scale-integration (VLSI) technology nowadays. MOSFET has experienced a significant evolution and has been systemically studied for several decades [1]. Metal-oxide-semiconductor (MOS) structure, the core part of MOSFET, is also widely studied because of the easier fabrication process. One primary purpose of the MOS capacitor is to estimate the properties of the semiconductor, insulating layer, and semiconductor-insulator interface. Measuring the capacitance and conductance of the

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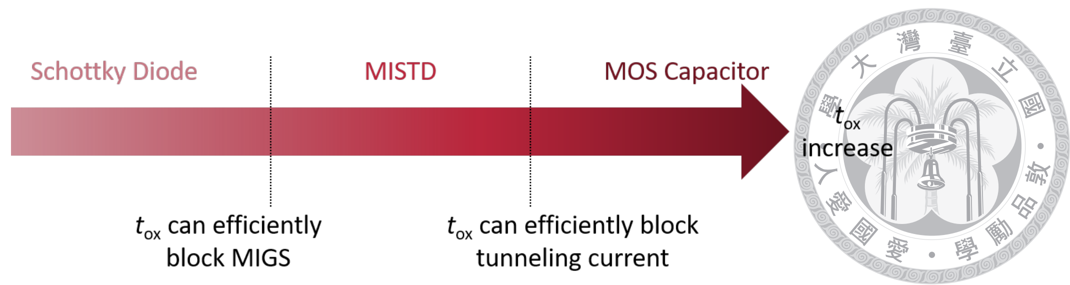

Figure 1–1. A schematic describing the difference between the Schottky diode, MISTD, and MOS capacitor. The MOS structure will act like a Schottky diode, MISTD, and MOS capacitor with increasing oxide thickness. However, there is no clear definition of the boundary of these devices.

MOS capacitor can decide the oxide thickness, doping concentration, amount of oxide charges, metal work function, interface state [2–4], and carrier lifetime [5, 6]. Detailed analysis of AC measurement on MOS capacitor had been finely described by Nicollian et al. [7, 8].

Metal-insulator-semiconductor tunnel diode (MISTD), a MOS capacitor with thinner oxide, is also widely studied to understand the ultra-thin oxide's properties [9–16]. As shown in **Figure 1–1** , MISTD has an insulating layer thickness between the MOS capacitor and Schottky diode. MOS structure with an extremely thin insulating layer acts like a Schottky diode. The wave function penetrating from metal to semiconductor leads to significant metal-induced gap states (MIGS) and Schottky barrier pinning [17, 18]. A thick enough insulating layer is needed to block MIGS and de-pin the Schottky barrier [19,20] to let the devices have the property of MISTD. When the insulator thickness of a MISTD further increases and is thick enough to eliminate the tunneling current efficiently, the device can be seen as a MOS capacitor. However, no clear boundaries are defined between the Schottky diode, MISTD, and MOS capacitor. This work mainly focuses on the Al/SiO_2/Si (p) MISTD with an oxide thickness of 1.5 - 3.5 nm, as shown in **Figure 1–2** .

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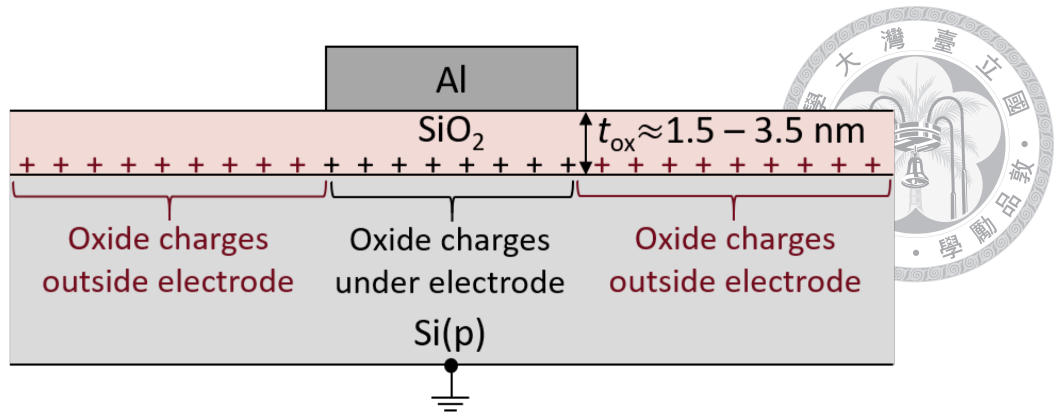

Figure 1–2. Schematic of a Al/SiO_2/Si(p) MISTD. The oxide charges under and outside the electrode are also labeled.

MISTD can be used to estimate basic properties such as semiconductor carrier lifetime [9] or electron effective mass in oxide [10]. Besides studying the material's characteristics, MISTD has many applications because the tunneling current of MISTD is very sensitive to environmental conditions. Applications of MISTD include temperature sensors [21], strain sensors [22], photodetectors [23, 24], solar cells [25], and transistors with subthreshold swings lower than 60 mV/dec [26].

MISTD, MOS capacitor, and MOSFET all suffer from the problem of oxide charges, which naturally exist because of oxygen vacancies [27]. Oxide charges will also be induced by ion pollution [28], hot electrons [29], electric field stress [30], and radiation [31]. Many works focus on studying the oxide charges under the electrode, which are labeled in **Figure 1–2** . Oxide charges under the electrode mainly impact the flat band voltage of the device, which is systematically studied and described in [7]. However, the impact of oxide charges on flat band voltage is minor for MISTD, which will be discussed in more detail in **Section 1.2**.

As shown in **Figure 1–2** , oxide charges also exist outside the electrode. These oxide charges will influence the characteristics of MISTD and MOS capacitor in ways different

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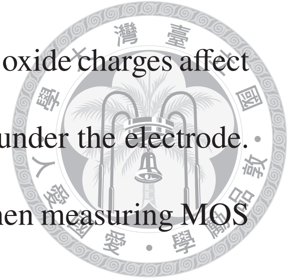

from the oxide charges under the electrode. We observed that the outer oxide charges affect the electrical property of MISTD much more than the oxide charges under the electrode. In the 1960s, few works observed the impact of outer oxide charges when measuring MOS capacitors [32–34]. Outer oxide charges are utilized to enhance the performance of MISTD solar cells after they are found in many different insulating layers [25].

Though the first observation and utilization of outer oxide charges on MISTD solar cells was explored, few articles quantitatively and systematically describe the impact of outer oxide charges on MISTD in the dark. In this work, we discuss the impact by doing experimental, TCAD simulations, and analytical calculations. The discussions focus on the fundamental understanding of the electrical characteristics of MISTD when outer oxide charges exist. The work helps one to know ultra-thin oxide in more detail and provide design consideration of MISTD devices for possible applications.

1.2 Impact of Oxide Charges on Flat-Band Voltage Shift

As mentioned in **Section 1.1**, many works study the flat-band voltage shift of MOS capacitor caused by oxide charges [7]. However, we will point out that flat-band voltage shift is minor for MISTD. In other words, estimating the number of oxide charges in MISTD by flat-band voltage shift is inappropriate. We also show that the existence of oxide charges does not strongly affect the electrical characteristics of MISTD in the accumulation and near flat band voltage regions.

Without otherwise notification, the MOS structure discussed in this work is Al/SiO_2/Si (p) with doping concentration N_a = 10^{16} cm^{-3}. **Figure 1–3** shows the detailed band diagram of the MOS structure without oxide charges and biased at the flat-band voltage

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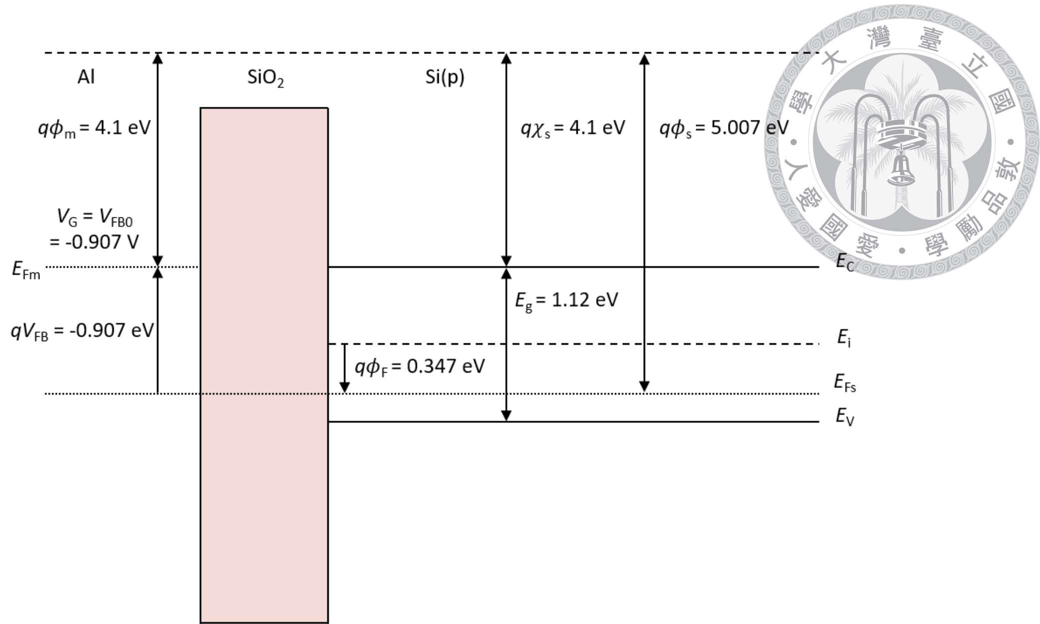

Figure 1–3. A detailed Al/SiO_2/Si(p) MOS structure band diagram with the gate bias of $V_G = V_{FB0} = -0.907$ V and doping concentration $N_a = 10^{16}$ cm^{-3}. In this band diagram, q is the elementary charge, ϕ_m is the metal work function, ϕ_F is the potential difference between intrinsic Fermi-level E_i and semiconductor bulk Fermi-level E_{Fs}, χ_s is the semiconductor electron affinity, E_g is the semiconductor band gap, and ϕ_s is the semiconductor work function.

$V_G = V_{FB0}$. Here V_{FB0} is

$$\begin{aligned} V_{FB0} &= \phi_m - \phi_s \\ &= \phi_m - (\chi_s + E_g/2q + \phi_F) = -0.907 \text{ V}, \end{aligned} \tag{1.1}$$

where ϕ_m is the metal work function, ϕ_s is the semiconductor work function, χ_s is the semiconductor electron affinity, E_g is the semiconductor band gap, q is the elementary charge, and ϕ_F is the potential difference between intrinsic Fermi-level E_i and semiconductor bulk Fermi-level E_{Fs}. When the oxide charges are considered, the band diagram needs to be redrawn and is shown in **Figure 1–4** (a). The charges inside silicon dioxide are mostly positive [27, 28]. These positive oxide charges will build up a negative oxide voltage V_{ox} when the device is biased in flat-band condition. The flat-band voltage V_{FB} considering

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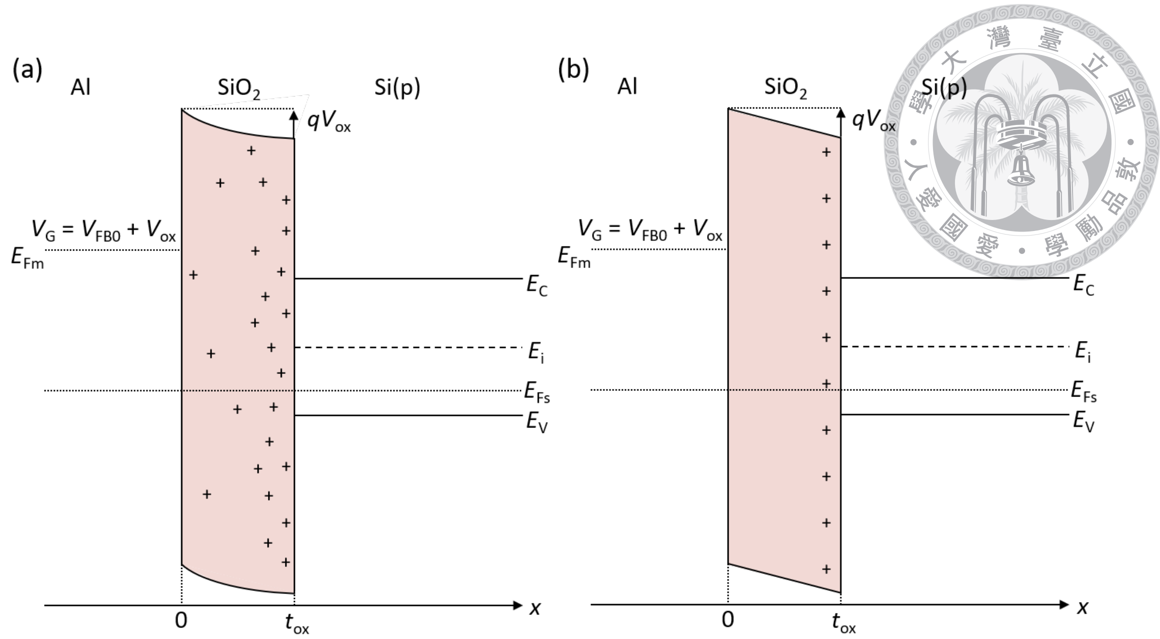

Figure 1–4. Band diagram of a MOS structure with (a) naturally distributed oxide charges and (b) an effective oxide charge sheet at Si – SiO_2 interface.

the oxide charges can be written as

$$\begin{aligned} V_{\mathrm{FB}} &= V_{\mathrm{FB0}} + V_{\mathrm{ox}} \\ &= V_{\mathrm{FB0}} - \int_0^{t_{\mathrm{ox}}} x \frac{Q_{\mathrm{ox}}(x)}{\epsilon_{\mathrm{ox}}} dx, \end{aligned} \tag{1.2}$$

where x is the coordinate labeled in **Figure 1–4** with origin at the Al – SiO_2 interface, $Q_{\mathrm{ox}}(x)$ is the density of oxide charges per unit volume at x, and ϵ_{ox} is the oxide permittivity. To avoid the integral term in (1.2), the oxide charges are usually lumped as an effective charge sheet at the Si – SiO_2 interface, as shown in **Figure 1–4** (b). With the adjustment, (1.2) can be rewritten as

$$V_{\mathrm{FB}} = V_{\mathrm{FB0}} - \frac{Q'_{\mathrm{ox}}}{C_{\mathrm{ox}}}, \tag{1.3}$$

where Q'_{ox} is effective charge density per unit area at Si – SiO_2 interface, and $C_{\mathrm{ox}} = \epsilon_{\mathrm{ox}}/t_{\mathrm{ox}}$ is the oxide capacitance. It is defined that $|\Delta V_{\mathrm{FB}}| = |V_{\mathrm{ox}}| = Q'_{\mathrm{ox}}/C_{\mathrm{ox}}$. The result of $|\Delta V_{\mathrm{FB}}|$

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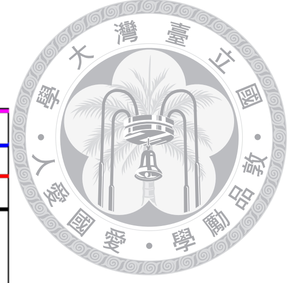

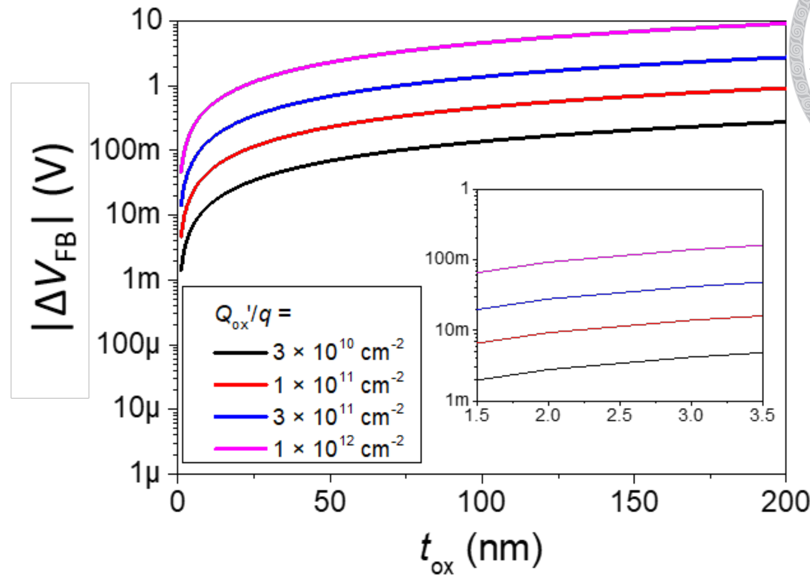

Figure 1–5. $|\Delta V_{FB}|$ v.s. t_{ox} with the amount of Q'_{ox}/q around 10^{10} – 10^{12} cm^{-2}.

at different Q'_{ox}/q and t_{ox} is plotted in **Figure 1–5**. The amount of Q'_{ox}/q are around 10^{10} – 10^{12} cm^{-2}, which are usually seen in silicon dioxide [27].

From **Figure 1–5**, one can observe that MOS capacitors with oxide thicknesses in tens or hundreds of nanometers have significant $|\Delta V_{FB}|$ for hundreds of millivolts to few volts. However, for MISTD with oxide thicknesses 1.5 - 3.5 nm, $|\Delta V_{FB}|$ is smaller than about 100 mV. $|\Delta V_{FB}|$ v.s. t_{ox} within 1.5 - 3.5 nm is enlarged and attached in **Figure 1–5**. $|\Delta V_{FB}|$ of MISTD will easily be distorted by other side effects. For example, the crystal orientation difference of aluminum can lead to tens of millivolts of ϕ_m variation [35]. Doping fluctuation in the silicon wafer, observed up to 50% [36], can lead to ϕ_s variation in about ten millivolts. From the above discussion, one can find that measuring $|\Delta V_{FB}|$ from capacitance-voltage relation is not an efficient method to calculate oxide charges in MISTD. To further confirm the situation, we do the TCAD simulation with an oxide thickness of 3 nm and Q'_{ox}/q of 0 and 2.8×10^{11} cm^{-2}. The simulation capacitance results at

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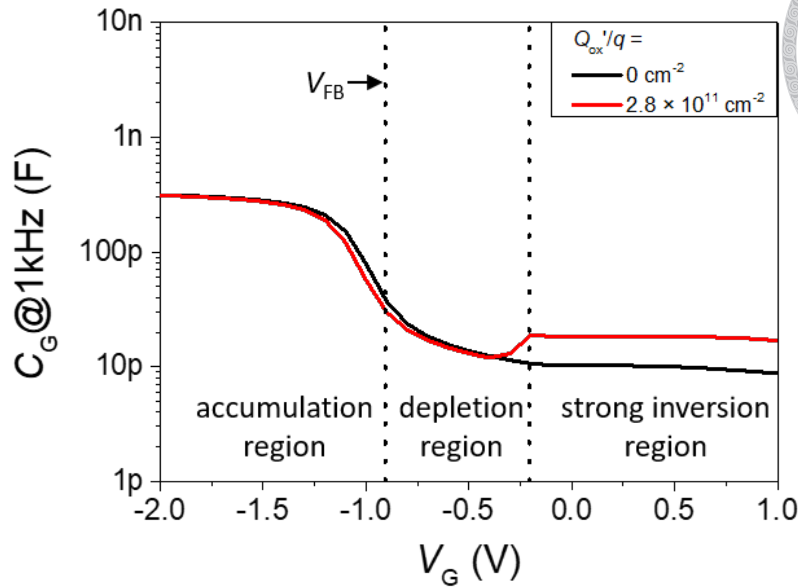

Figure 1–6. TCAD simulation results for MISTD with an oxide thickness of 3 nm and Q'_{ox}/q of 0 and 2.8×10^{11} cm^{-2}.

1 kHz are shown in **Figure 1–6**. In **Figure 1–6**, one can find that the capacitance characteristic of MISTD does not strongly affected by the oxide charges in the accumulation region and around V_{FB}. Only a $|\Delta V_{FB}|$ shift of around 50 mV is observed in these two samples. This level of $|\Delta V_{FB}|$ is challenging to be defined in experiments. However, the effect of oxide charges becomes significant in the strong inversion region.

As the result of this section, it is found that the oxide charges play a more critical role in strong inversion region than around V_{FB} for MISTD. For the Al/SiO_2/Si(p) MISTD, strong inversion roughly happens at positive bias. In this work, we mainly focus on the positive bias of Al/SiO_2/Si(p) MISTD.

1.3 Device Structure and Conditions Under Study

In this section, we briefly arrange the conditions for the structure of the studied devices and the bias region we are interested in.

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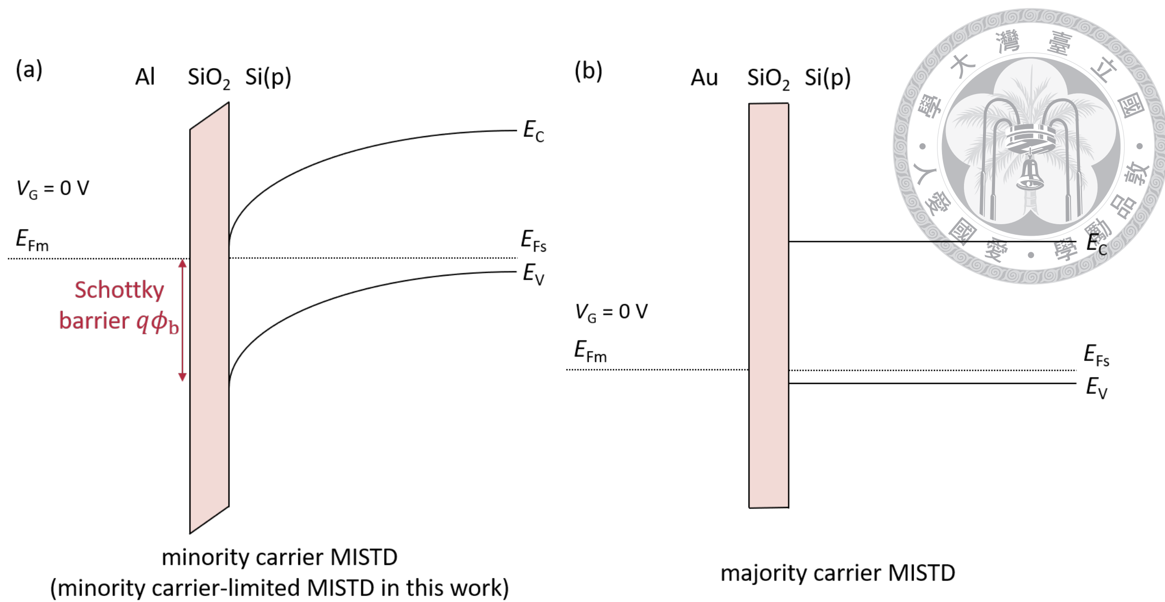

Figure 1–7. Band diagrams of p-type silicon substrate MISTDs with (a) aluminum and (b) gold as gate metal.

As mentioned in **Section 1.2**, *we select aluminum as the gate metal and p-type silicon as the substrate.* The band diagram of Al/SiO_2/Si(p) MISTD at $V_G = 0$ V is plotted in **Figure 1–7** (a). The work function difference of ~ 0.9 V between aluminum and p-type silicon shows a large Schottky barrier $q\phi_b$ for Al/SiO_2/Si(p) MISTD. This kind of MISTD is defined as "minority carrier MISTD" by Green et al. [11, 12] because the metal Fermi-level roughly aligns to near the conduction band of p-type silicon. In this work, we find that the role of majority carrier can't be neglected. We use the wording of "minority carrier-limited MISTD" here. This kind of MISTD has a diode-like current behavior due to its high $q\phi_b$ [11, 12]. On the other hand, if we select gold as the gate metal, the work function difference between metal and p-type silicon is very small. The band diagram for Au/SiO_2/Si(p) MISTD at $V_G = 0$ V is plotted in **Figure 1–7** (b). The device is called "majority carrier MISTD" [11,12] because the metal Fermi-level is close to near the valance band of p-type silicon. No significant Schottky barrier and no diode-like current

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behavior exist for this device [11, 12]. However, most MISTD applications utilized the diode-like current behavior of minority carrier-limited MISTD [21–24, 26]. By the way, many interesting phenomena are observed by modulating the Schottky barrier height of MISTD [37–40]. Thus, we chose the structure of Al/SiO_2/Si(p) to obtain a significant $q\phi_b$, which is important for our study.

Except for the material selection, it is also discussed in **Section 1.1** that *we experimentally focus on Al/SiO*$_2$*/Si(p) MISTD with oxide thicknesses within 1.5 - 3.5 nm.* For different materials or fabrication processes, the oxide thickness range for MISTD may be different. Because of the quantum confinement at the silicon surface [1] and the leakage of the oxide, it is difficult to extract the oxide thickness of MISTD directly from measuring C_{ox} at the accumulation region. Our work calculates the oxide thicknesses by fitting the tunneling current at $V_G = -0.9$ V with our database. The database measures the current of a set of MISTDs with different oxide thicknesses. The TEM images of these MISTDs are taken after the measurement to define the oxide thickness. Oxide thicknesses t_{ox} of the target device is decided by the following equation:

$$t_{ox} = t_{ox1} + (t_{ox2} - t_{ox1}) \times \frac{\log[I_{G1}(V_G = -0.9)] - \log[I_G(V_G = -0.9)]}{\log[I_{G1}(V_G = -0.9)] - \log[I_{G2}(V_G = -0.9)]}, \tag{1.4}$$

where t_{ox1} and t_{ox2} are the oxide thickness from the database with the condition $t_{ox2} > t_{ox} > t_{ox1}$, $I_{G1}(V_G = -0.9)$ and $I_{G2}(V_G = -0.9)$ are the measured current at $V_G = -0.9$ V from the database with oxide thickness t_{ox1} and t_{ox2}, and $I_G(V_G = -0.9)$ is the measured current at $V_G = -0.9$ V from the target device. The oxide thicknesses in the following chapters are the effective oxide thickness decided by (1.4).

Finally, as discussed in **Section 1.2**, we focus on the positive bias to study the impact

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of oxide charges on MISTD. In our work, *we mainly focus on* $V_G = 0-2.5$ V. For MISTD with relatively thicker oxide, which will act like a MOS capacitor, the oxide voltage approaches the boundary of inducing Fowler-Nordheim tunneling in SiO_2. The oxide layer will degrade easier in the Fowler-Nordheim tunneling region [41]. The degradation of the oxide layer is out of the scope of our work. The voltage region defined above is selected to avoid the severe degradation of the devices.

In this section, we highlight the conditions of MISTD we are interested in. These conditions are briefly listed below:

- Aluminum and p-type silicon are selected as the gate metal and the substrate of MISTD, respectively, to achieve a high Schottky barrier.
- Focus on the MISTDs with oxide thickness in 1.5 - 3.5 nm to let the devices have the properties of MISTD.
- Discuss the devices in the bias region of $V_G = 0-2.5$ V to avoid Fowler-Nordheim tunneling and oxide degradation.

1.4 Fabrication of MISTD

In this section, we describe the fabrication process of our devices. The fabricated devices will be measured and discussed in different ways throughout this work.

In our work, the oxide layer of MISTD is formed by the anodic oxidation (ANO) process [42]. The equipment of the ANO process is plotted in **Figure 1–8** . A silicon wafer was connected to positive bias as the anode, and a platinum plate was connected to negative bias as the cathode with a 15 V DC power source. The silicon wafer and platinum plate are immersed in a tank filled with room-temperature deionized water (DI water). When

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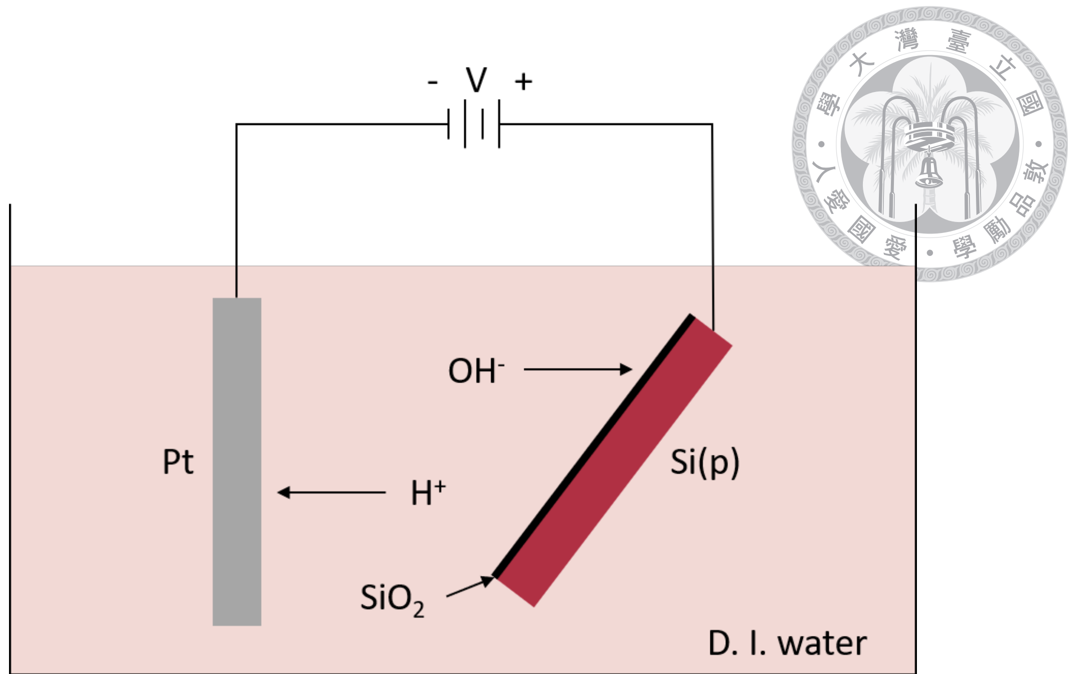

Figure 1–8. The equipment for the ANO process.

the power source is on, the reaction at the anode side is

$$Si + 4\,OH^{-} \rightarrow SiO_2 + 4\,e^{-} + 2\,H_2O. \tag{1.5}$$

This process will form a thin layer of SiO_2 on the silicon wafer. As shown in **Figure 1–8**, the silicon wafer is tilted to let the distance between the two electrodes varies between 1 - 3 cm. Because of different distances and electric fields, the oxide layer will have different thicknesses throughout the wafer. In our ANO process, we usually turn on the power source for between 6 - 10 min to finely tune the oxide thicknesses.

Figure 1–9 is the schematic of the fabrication process. P-type silicon wafers with a doping concentration of N_a = 10^{16} cm^{-3} and surface orientation of (100) are used. Radio Corporation of America (RCA) clean process is adopted to remove organic particles, ion impurities, and native oxide [43]. The ANO process forms the oxide layer within 1.5 - 3.5

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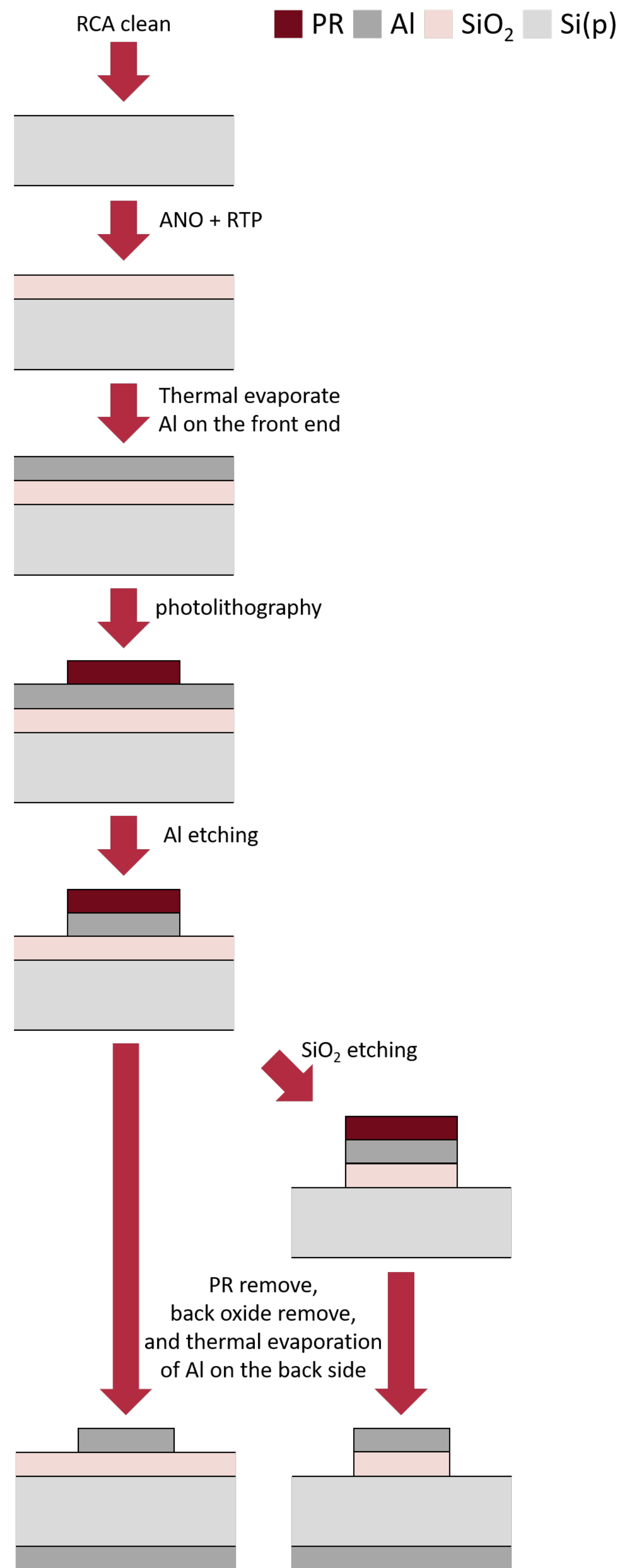

Figure 1–9. Schematic of the fabrication process.

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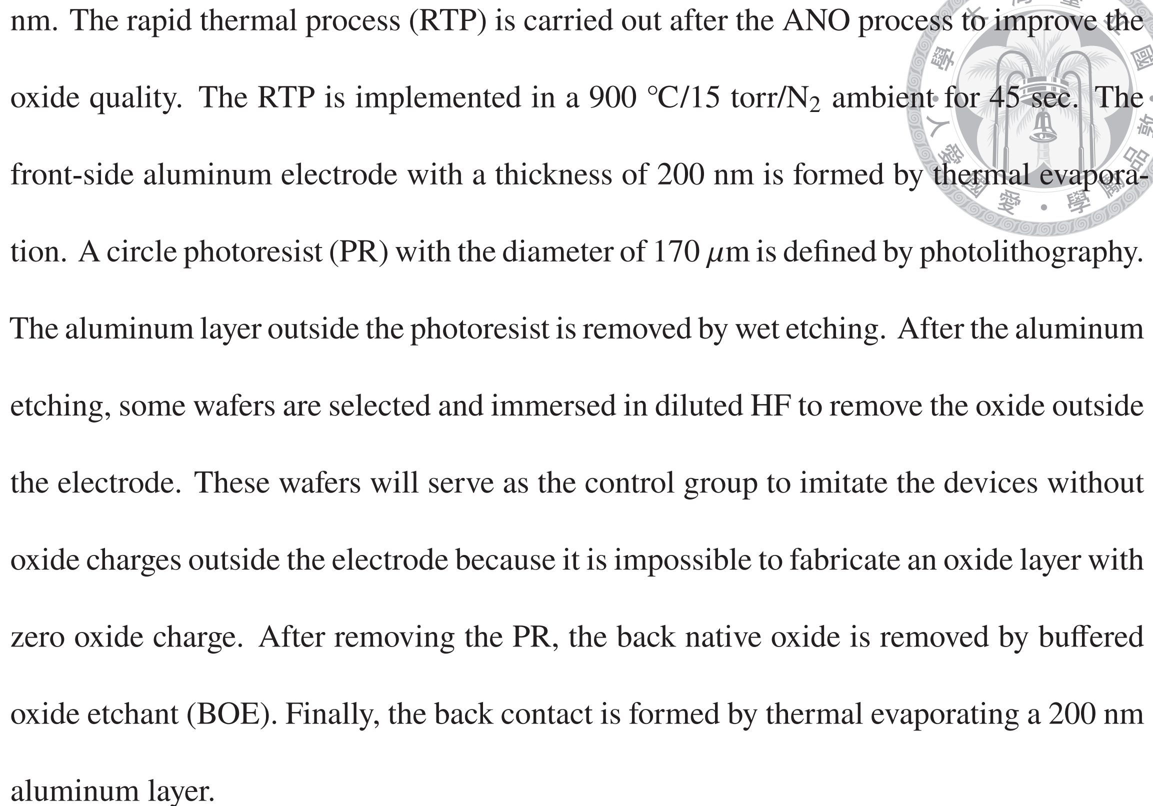

nm. The rapid thermal process (RTP) is carried out after the ANO process to improve the oxide quality. The RTP is implemented in a 900 °C/15 torr/N_2 ambient for 45 sec. The front-side aluminum electrode with a thickness of 200 nm is formed by thermal evaporation. A circle photoresist (PR) with the diameter of 170 μm is defined by photolithography. The aluminum layer outside the photoresist is removed by wet etching. After the aluminum etching, some wafers are selected and immersed in diluted HF to remove the oxide outside the electrode. These wafers will serve as the control group to imitate the devices without oxide charges outside the electrode because it is impossible to fabricate an oxide layer with zero oxide charge. After removing the PR, the back native oxide is removed by buffered oxide etchant (BOE). Finally, the back contact is formed by thermal evaporating a 200 nm aluminum layer.

Two sets of MISTD, one with outer oxide and the other without outer oxide, are fabricated in our work. Both sets have circle electrode with the diameter of 170 μm and oxide thicknesses around 1.5 - 3.5 nm. These devices are measured by Agilent B1500A semiconductor device parameter analyzer. The detailed measurement methods will be discussed in the following chapter.

1.5 TCAD simulation

In this work, some TCAD simulations are carried out for comparison. We use Silvaco ATLAS to implement the simulation. Without otherwise mentioned, our simulation structure is an Al/SiO_2/Si(p) stacking with a circle electrode in a cylindrical coordinate. The diameter of the electrode is 170 μm, the same as the experimental device. The oxide charges' distribution is defined to be uniformly located at the SiO_2/Si(p) interface.

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1.6 Chapter Organization

In **Chapter 2**, we first review three phenomena of MISTD and MOS capacitor. These phenomena are listed below:

- Deep depletion (DD) on high-frequency (HF) capacitance characteristic of MISTD.
- Schottky barrier height modulation (SBHM) effect on current characteristic of MISTD.
- Capacitance values increases in of the MOS capacitor under inversion region.

These characteristics are observed and discussed in [11, 12, 16], [24, 40], and [7], respectively. In the second half of **Chapter 2**, we qualitatively discussed the observations on the impacts of outer oxide charges on these three phenomena. The detailed quantitative models of these impacts are proposed in **Chapter 3**, **Chapter 4**, and **Chapter 5**, respectively. Finally, we give conclusions and suggest possible future works in **Chapter 6**.

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2

Impact of Oxide Charges on the Current and Capacitance Characteristics of MISTD

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2.1 Background

MISTD has electrical characteristics similar to Schottky Diode and MOS capacitor. However, MISTD does not totally the same as Schottky Diode and MOS capacitor in the whole bias region. When considering the high-frequency capacitance-voltage (HFCV) relation, MISTD acts like a MOS capacitor at low bias voltage and like Schottky Diode at high bias voltage [11, 12, 16, 44]. In the aspect of current-voltage (IV) relation, MISTD has a diode-like IV similar to the Schottky diode, but some unusual current behaviors are observed. For example, the reverse biased saturation current of MISTD increase with oxide thickness because of Schottky barrier height modulation (SBHM) [24, 40]. These IV and HFCV characteristics of MISTD will be reviewed in **Section 2.3.2**. The discussion in [11, 12, 16, 24, 40, 44] all adopt a 1D model, which considers only the region under the electrode, to simplify the analysis. The deviation between the 1D model and experimental results has been pointed out recently [16]. In our work, we propose that by considering the impact of outer oxide charges at the lateral region, one can know the origin of the above deviation. The consideration of outer oxide charges is discussed in **Section 2.3.3**.

Except for IV and HFCV, measurement of the capacitance-frequency (CF) relation is an important method to characterize the MOS structure [7]. CF measurement is usually used to estimate carrier lifetime [6, 7]. However, the existence of outer oxide charges will distort the CF relation of the MOS capacitor [32–34]. We observed that the deviation also appears in MISTD [45]. The observation and the discussion will be described in **Section 2.3.4** and **Section 2.3.5**, respectively.

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2.2 Experimental Details

In this chapter, three MISTDs with outer oxide and three MISTDs without outer oxide are selected for comparison. The thicknesses of the three MISTDs with outer oxide are 17.6, 20.9, and 24.8 Å. For MISTDs without outer oxide are 17.9, 21.2, and 24.6 Å. IV and CV characteristics of these devices are measured for discussion. In **Section 2.3.1**, IV characteristics under illumination are carried out to evaluate the effect of the removal of the outer oxide charges. The light source is a commercial LED with a color temperature of 6000-6500 K.

2.3 Result and Discussion

2.3.1 Evidence of Outer Oxide Charges by Oxide Removal

Before further discussion, we measure the photosensitivity of the devices to confirm that our fabrication process had efficiently removed the outer oxide and outer oxide charges. In this section, one MISTD with outer oxide (t_{ox} = 20.9 Å) and another MISTD without outer oxide (t_{ox} = 21.2 Å) are selected for comparison.

As mentioned in **Section 1.1**, oxide charges in the outer oxide are used to enhance the efficiency of the MISTD solar cell [25]. The schematic of the mechanism is plotted in **Figure 2–1** . The oxide charges in the outer oxide will deplete holes in the substrate and induce some electrons at the silicon surface. The field inside the depletion region will separate the photon-generated electron-hole pairs to avoid recombination. The generated electrons will laterally diffuse to the electrode by the conduction channel induced by the oxide charges. The sensitivity of the device is therefore enhanced by the two mechanisms:

- Less recombination of the photon generated electrons by the oxide charges induced

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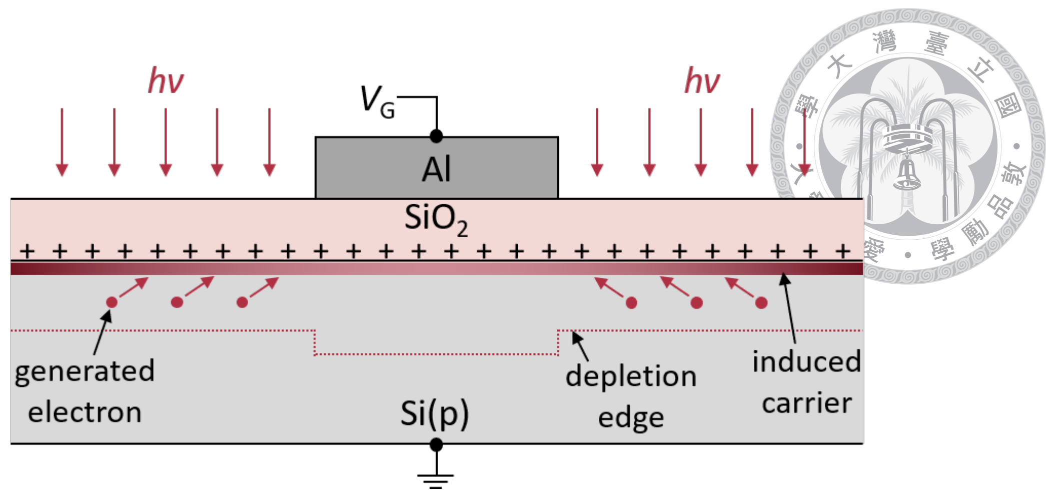

Figure 2–1. Schematic of how the oxide charges enhance the photosensitivity.

field.

- Larger effective absorption region by oxide charges induced lateral conduction channel in depletion region.

Based on the mechanism, if the outer oxide is removed by the diluted HF as described in **Section 1.4**, the photosensitivity of the device will decrease.

The measured IV curves of these two devices are shown in **Figure 2–2**. **Figure 2–2** (a) and (b) show the measured results of MISTD with and without outer oxide. Double sweep is adopted to avoid the confusion of displacement current. In **Figure 2–2**, the red curves are measured under illumination with a photon flux of 10^{13} $cm^{-2}sec^{-1}$. A larger photon current is observed for the device with outer oxide. With the enlarged IV curves from -0.3 to 0.2 V, a larger open circuit voltage V_{OC} is measured when the outer oxide exists.

The measured results shown in **Figure 2–2** prove that the outer oxide and oxide charges can be efficiently removed by oxide removal. Although native oxide with a few Å thicknesses may form when the silicon is exposured to air [46], the characteristics of MISTD without outer oxide are not strongly affected by native oxide in our work.

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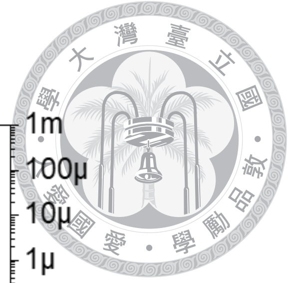

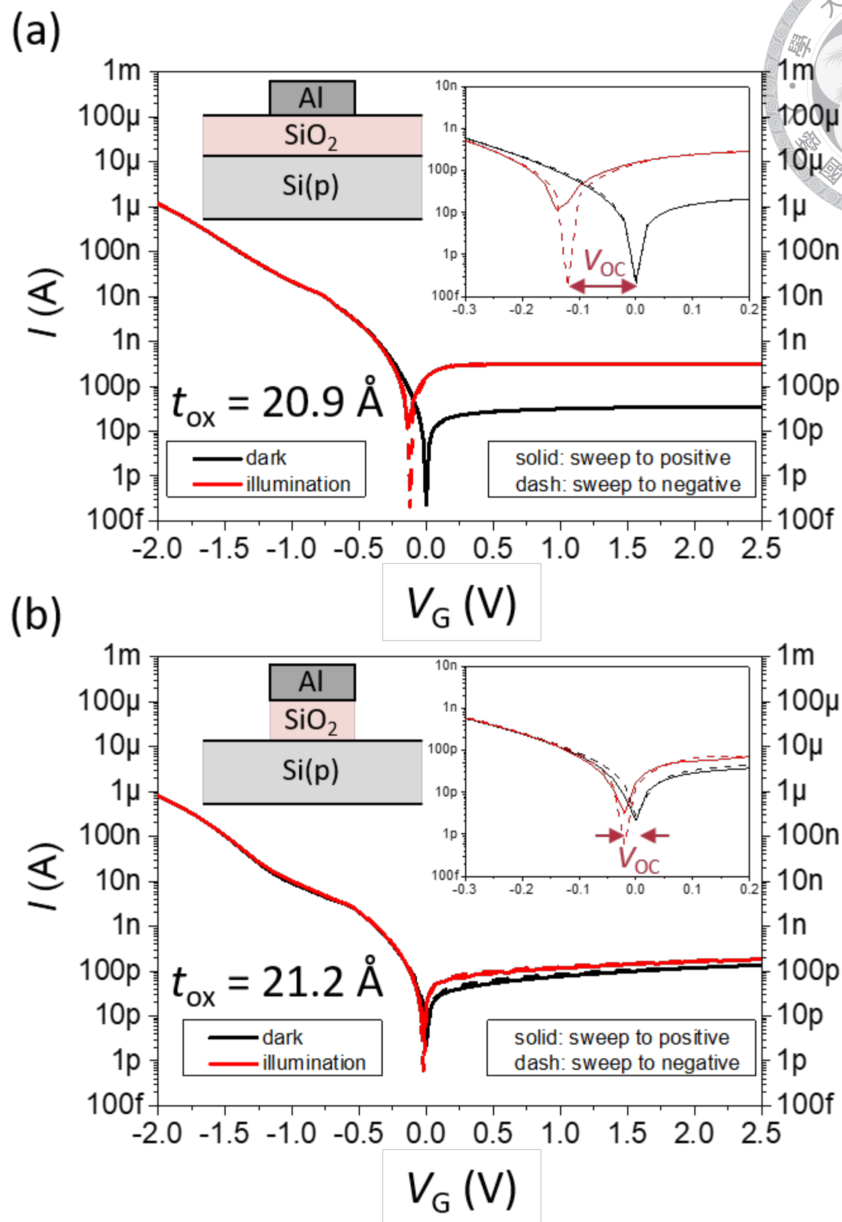

Figure 2–2. Measured IV characteristics in the dark and under the illumination of MISTD (a) with and (b) without outer oxide. The device with outer oxide has better photosensitivity.

2.3.2 High Frequency Capacitance-Voltage and Current-Voltage of MISTD

Figure 2–3 shows the HFCV of six devices mentioned in **Section 2.2**. HFCV for the devices with and without outer oxide are plotted in **Figure 2–3** (a) and (b), respectively.

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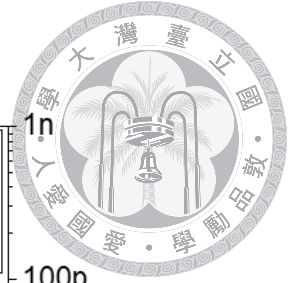

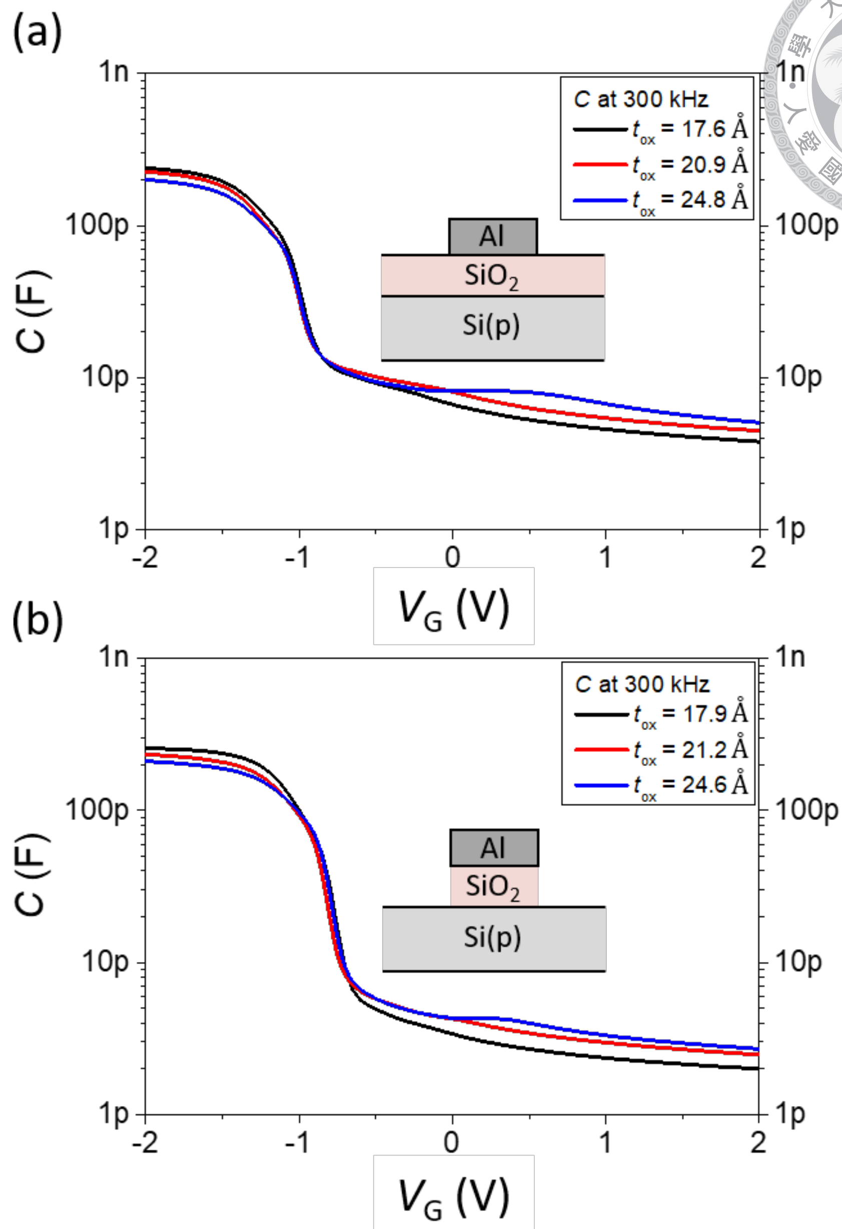

Figure 2–3. Measured HFCV characteristics of different oxide thicknesses MISTDs (a) with and (b) without outer oxide.

The HFCV curves are measured under 300 kHz. At negative bias, the HFCV of MISTD is similar to the MOS capacitor. The difference between them is observed in positive bias. For the MOS capacitor, the high-frequency capacitance value is almost constant because the surface band bending is pinned around $2\phi_F$, where ϕ_F is defined in **Figure 1–3**, in

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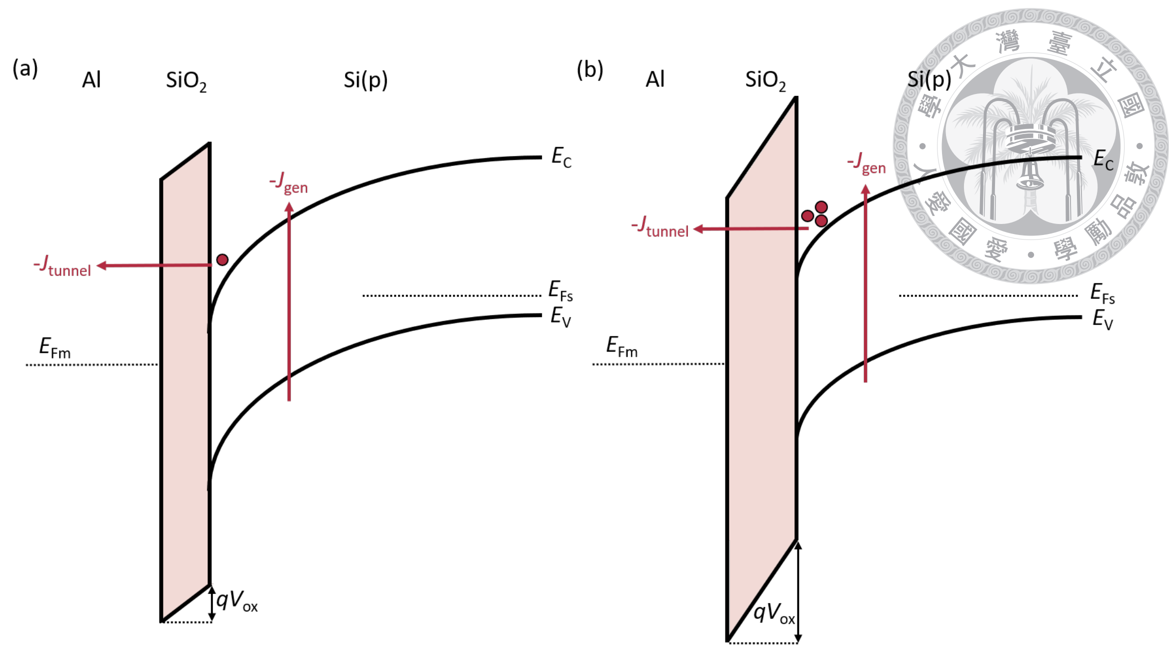

Figure 2–4. Band diagrams of MISTD with (a) thinner and (b) thicker oxide layers. The MISTD with relatively thicker oxide is able to hold more inversion charges.

the strong inversion region. However, the capacitance value of MISTD decreases in the positive bias region. The decrease in capacitance is caused by the deep depletion (DD) effect. The mechanism of DD is shown in **Figure 2–4** (a). Because of the leakage oxide layer of MISTD, the generated electron current $-J_{\mathrm{gen}}$ in bulk silicon is difficult to balance with the tunnel current $-J_{\mathrm{tunnel}}$ with an existing inversion charge layer. Thus, the oxide voltage V_{ox} is difficult to increase. Most of the applied bias is dropped on silicon cause DD and the depletion width is increased. The increasing depletion region reduces the capacitance value.

However, an interesting behavior can be observed for the devices with t_{ox} = 24.8 Å and t_{ox} = 24.6 Å in **Figure 2–3** (a) and (b), respectively. These two devices hold at a constant capacitance value in the low positive bias region and go into the DD region in the higher bias region. The mechanism is described in **Figure 2–4** (b). At the low bias

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region, the oxide's leakage is insignificant because of its relatively thicker thickness. In this situation, the $-J_{gen}$ is able to compensate $-J_{tunnel}$ and an inversion layer is built-up like a MOS capacitor. However, the $-J_{tunnel}$ will increase with V_{ox} until the $-J_{gen}$ is no longer to overcome the $-J_{tunnel}$. The MISTD will finally be driven into the DD region at a higher bias voltage. The phenomenon was first observed by Green et al. [11] but still needs more detailed analysis. The analytical calculation of DD in MISTD will be proposed in **Chapter 3**.

Figure 2−5 shows the IV curves of MISTDs with and without outer oxide. In this section, we focus on discussing the devices with outer oxide as shown in **Figure 2−5** (a). At negative bias, the diode currents decrease with increasing oxide thickness, which is intuitive because of lower oxide tunneling probability. However, a reverse situation is observed in positive bias. The reverse bias saturation currents of our MISTDs increase with oxide thickness. This phenomenon was observed in some works [9, 47]. The mechanism of this phenomenon was proposed by our group in 2014 [24]. The band diagram in **Figure 2−6** can describe the mechanism. As discussed in **Section 1.2**, V_{ox} is very small at $V_G = V_{FB}$ for MISTD; thus, as plotted in **Figure 2−6** (a) and (c), MISTD with both thinner and thicker oxide layers have an initial hole Schottky barrier $q\phi_{b0}$. However, at $V_G = 2$ V, the MISTD with thicker oxide is able to reach higher oxide voltage V_{ox}, which leads to a more significant shifting of relative position between E_{Fm} and E_V in silicon, and modulates the Schottky barrier to a lower value. The modulated Schottky barrier is plotted in **Figure 2−6** (b) and (d). From **Figure 2−6** , one can observe that the hole Schottky barrier

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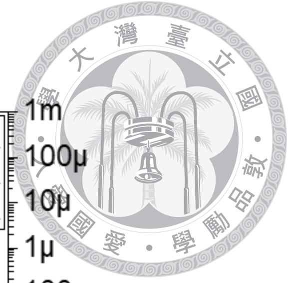

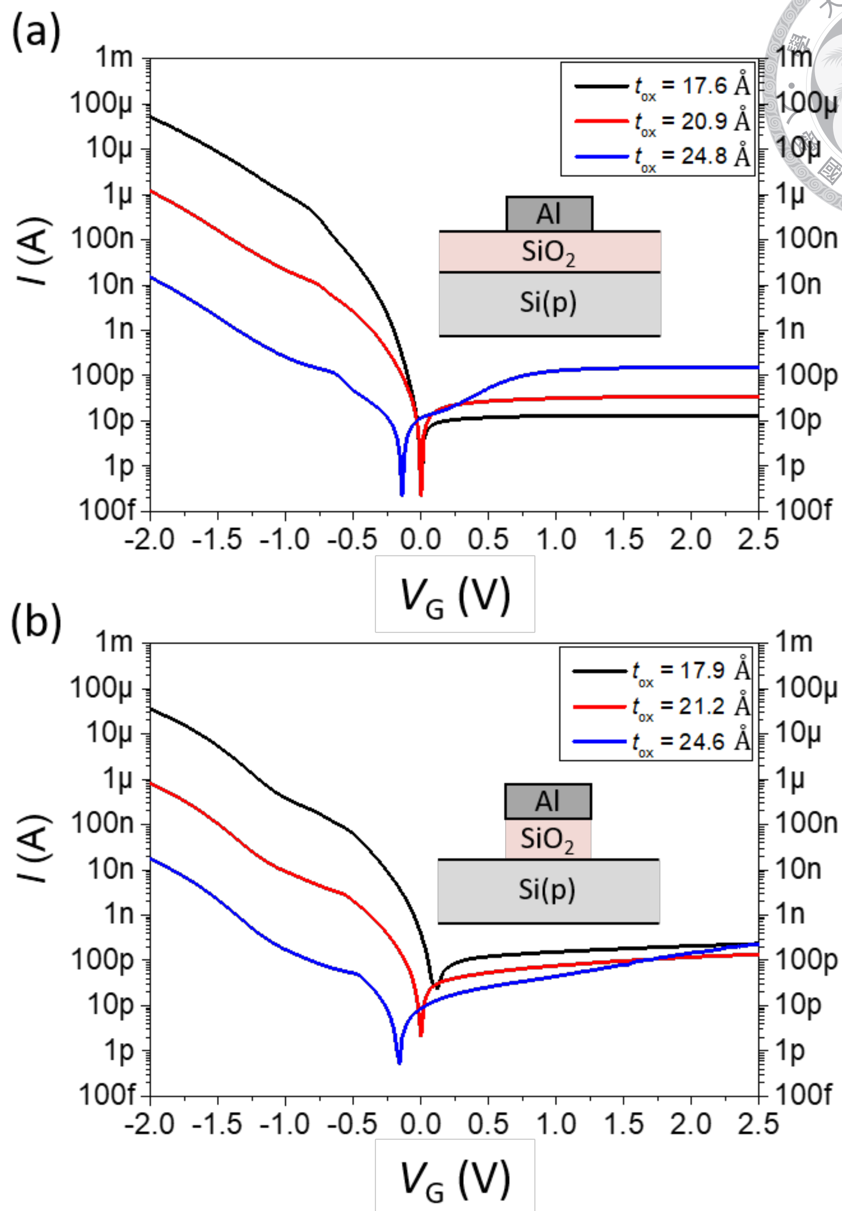

Figure 2–5. Measured IV characteristics of different oxide thicknesses MISTDs (a) with and (b) without outer oxide.

height $q\phi_{\mathrm{b}}$ is related to oxide voltage V_{ox} and can be written down as [24]

$$q\phi_{\mathrm{b}} = q\phi_{\mathrm{b0}} - qV_{\mathrm{ox}}, \tag{2.1}$$

where $q\phi_{\mathrm{b0}}$ is the Schottky barrier height at $V_{\mathrm{ox}} = 0$ V. The tunneling hole current J_{h} of

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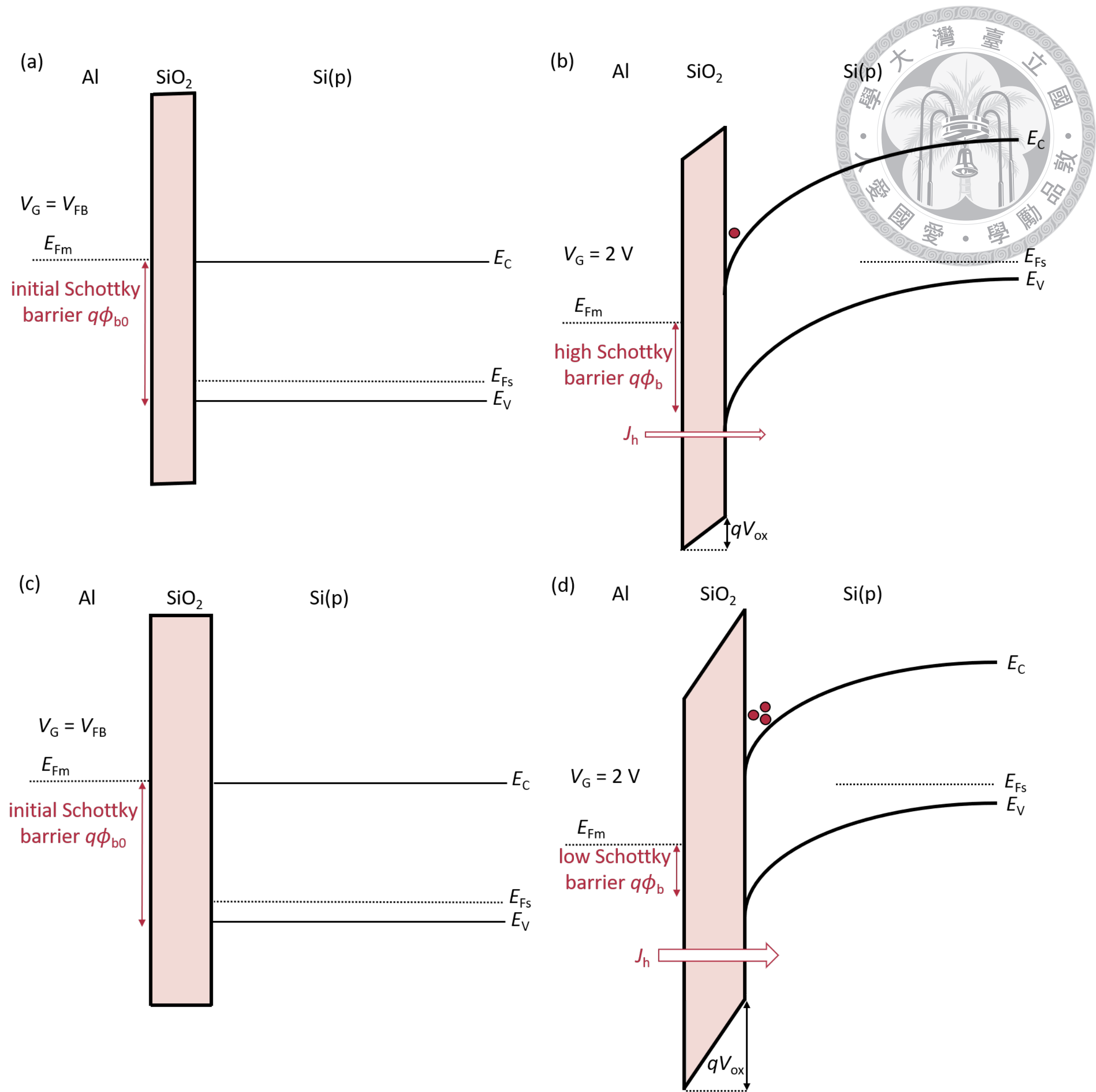

Figure 2–6. Band diagrams of MISTD with thinner oxide layer at (a) $V_G = V_{FB}$ and (b) $V_G = 2$ V. Band diagrams of MISTD with thicker oxide layer at (c) $V_G = V_{FB}$ and (d) $V_G = 2$ V. The MISTD with relatively thicker oxide is able to reach higher oxide voltage V_{ox} and modulate the Schottky barrier to a lower value at $V_G = 2$ V.

MISTD can be approximated as a combination of tunneling probability and thermionic emission equation [24, 48]

$$J_h \approx A^* T^2 P_{th} \exp(-q\phi_b/kT), \tag{2.2}$$

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where A^* is the Richardson constant for hole [49], T is the temperature, P_{th} is the hole tunneling probability, and k is the Boltzmann constant. As shown in **Figure 2–6**, MISTD with thicker oxide can hold more inversion charges and reach higher oxide voltage. Higher oxide voltage leads to a lower Schottky barrier and larger hole current. The mechanism is named "Schottky barrier height modulation" (SBHM) [24]. However, detailed analytical calculation about SBHM is still lack of discussion. Two questions about the approximation of SBHM in (2.2) are proposed in this work:

- SBHM assumes the increasing of $\exp(-q\phi_b/kT)$ with oxide thickness dominates J_h. However, the term P_{th} decreases with increasing oxide thickness and competing against $\exp(-q\phi_b/kT)$. To determine the validity of SBHM, one needs to know which one is the domination term and what oxide thickness range is critical for the mechanism.

- As shown in (2.1), a negative ϕ_b appears when V_{ox} reaches a value higher than ϕ_{b0}. However, the term of thermionic emission $\exp(-q\phi_b/kT)$ is value based on the assumption of a positive $\phi_b > 3kT/q$.

For solving the problems, a more detailed analytical model considering tunneling probability at the different energy levels and Fermi-Dirac distribution of the hole is needed. The model will be discussed in **Chapter 4**.

With the above discussion, one can find that HFCV and IV characteristics are highly co-related and are both sensitive to the oxide thickness. The oxide thickness decides the highest reachable V_{ox} of a MISTD and affects the bias region of constant high-frequency capacitance value. The highest V_{ox} also decides the level of SBHM and J_h. The normalized HFCV and IV of the MISTD with an outer oxide of 24.8 Å are plotted in **Figure 2–7**. At

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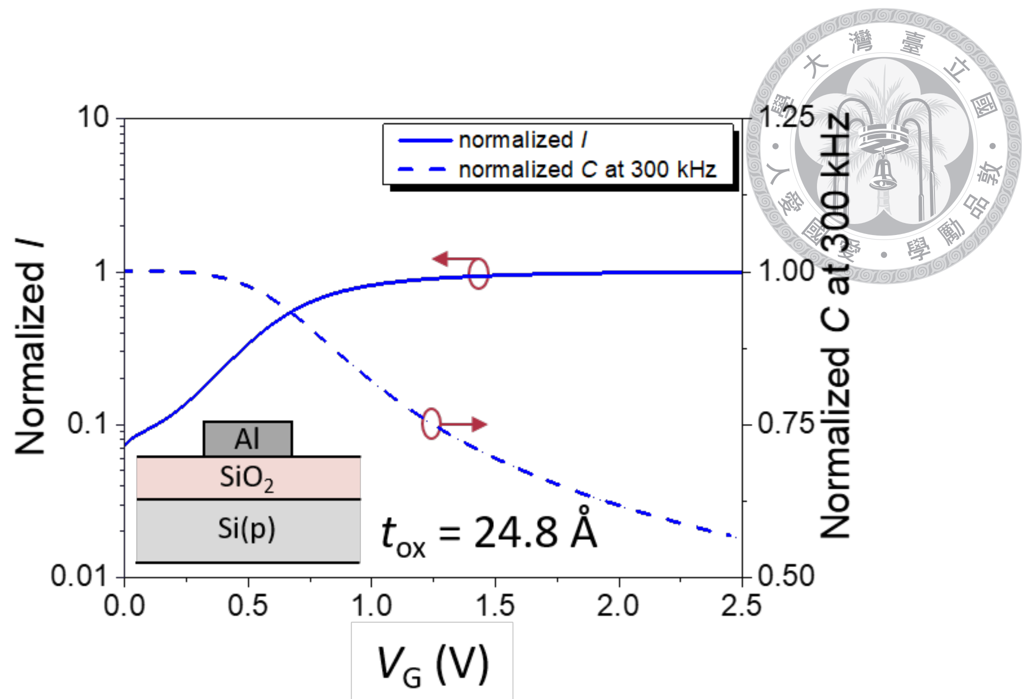

Figure 2–7. Normalized HFCV and IV of the MISTD with an outer oxide of 24.8 Å. The HFCV curve is normalized to the capacitance value at $V_G = 0$ V, and the IV curve is normalized to the current at $V_G = 2.5$ V.

low bias, the constant capacitance value of MISTD indicates that the band bending of silicon is pinned, and the oxide voltage keeps increasing, similar to a MOS capacitor. In this bias region, the hole tunneling current J_h keeps increasing because of SBHM. The device operates in the DD region at the high bias voltage, and the oxide voltage is pinned. The tunneling current is also pinned at a constant value because the Schottky barrier is no longer modulated.

In this section, we briefly discuss the DD effect in HFCV and the SBHM effect in IV. These two effects are strongly co-related. Mechanisms of DD and SBHM are proposed previously and observed in our experiments. However, quantitative analysis of these two mechanisms still needs to be explored. We try to suggest analytical models about them in **Chapter 3** and **Chapter 4**, respectively.

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2.3.3 Impact of Outer Oxide Charges on the High Frequency Capacitance-Voltage and Current-Voltage Characteristics of MISTD

In the previous section, we discuss HFCV and IV characteristics of MISTD by only considering the region under the electrode. In other words, only the 1D model of Al/SiO_2/Si stacking is considered. The 1D model is usually used when discussing MOS structure. However, we find deviations between the MISTDs with and without outer oxide. The deviations can be observed in **Figure 2−3** and **Figure 2−5**. These deviations indicate that the outer oxide plays an important role in the electrical properties of MISTD.

In **Figure 2−3**, one can observe that the two thickest devices (t_{ox} = 24.8 Åfor the device with outer oxide and t_{ox} = 24.6 Åfor the device without outer oxide) go into the DD region in different bias voltages. The device with outer oxide can hold a constant capacitance value to a higher positive bias. In **Figure 2−5** (b), one can find almost no SBHM effect for the MISTDs without outer oxide. These phenomena can be attributed to the outer oxide charges. Schematics of the mechanism are plotted in **Figure 2−8**. In **Figure 2−4**, we assume the supplement of the minority electrons $-J_{gen}$ is mainly generated from the region under the electrode. $-J_{gen}$ is renamed as $-J_{gen,bulk}$ and plotted in **Figure 2−8** (a) here. As shown in **Figure 2−8** (a), the outer oxide charges will induce additional lateral conduction channel. When a positive bias applies on the electrode, the potential will laterally extend and increase the effective control area of the MISTD. The generated electrons in this lateral area $-J_{gen,lateral}$ will laterally diffuse to the electrode through the conduction channel. As shown in **Figure 2−8** (b), one can observe that the tunnel current $-J_{tunnel}$ needs to balance with $-(J_{gen,bulk} + J_{gen,lateral})$.

With the extra electron supplement, the electrical characteristics of MISTD will be

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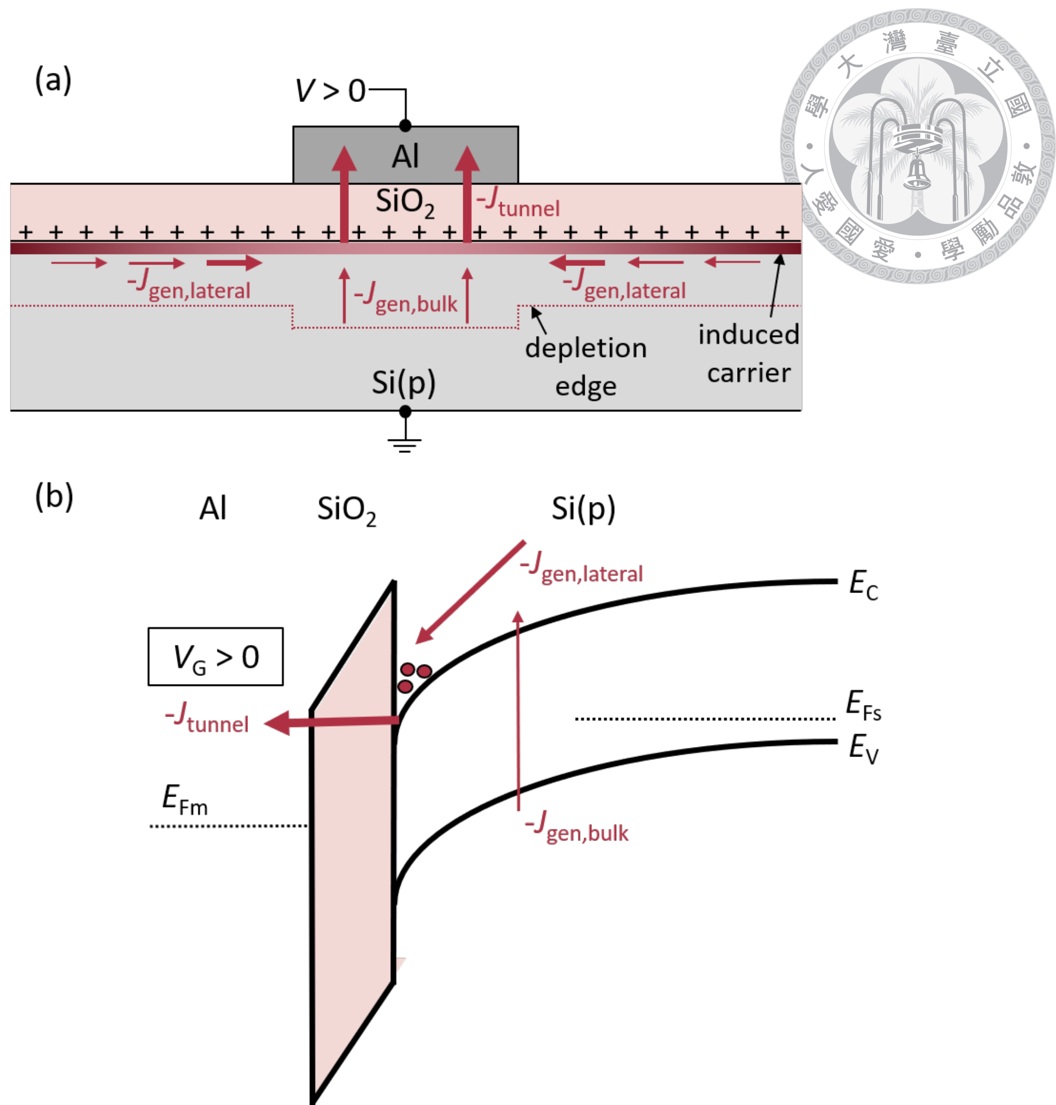

Figure 2–8. (a) The schematic for the mechanism of lateral electron supplement. The applied potential on the electrode laterally extends through the surface conducting channel, induced by oxide charges, and collects the generated electrons in the lateral region. (b) The band diagram under the electrode considering the lateral electron supplement.

affected. In **Figure 2–9** (a), we show the normalized HFCV of MISTD with similar oxide thickness but one with and the other without outer oxide. The HFCV curve is normalized to the capacitance value at $V_G = 0$ V. In **Figure 2–9** (a), one can observe that the MISTD with outer oxide goes into the DD region at a higher positive bias. The extra electron supplement $-J_{gen,lateral}$ lets the device can increase the inversion layer more efficiently and act like a MOS capacitor to a higher bias voltage. To further confirm the impact of

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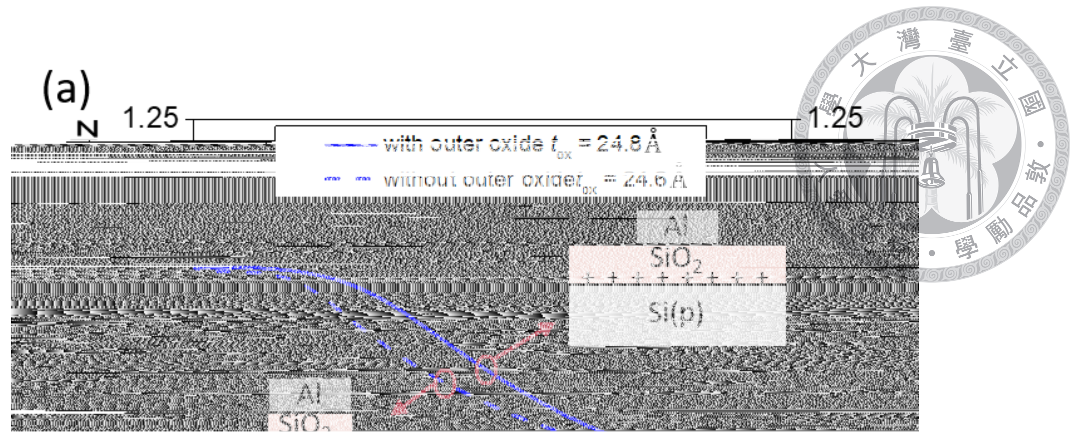

Figure 2–9. The normalized HFCV curves at 300kHz from (a) experimental and (b) TCAD simulation. The curves from devices with and without outer oxide charges are plotted in solid and dash lines, respectively.

oxide charges, the TCAD simulation is carried out. Simulated HFCV curves at 300kHz of MISTDs with an oxide thickness of 25 Å are shown in **Figure 2–9** (b). MISTD with effective oxide charges Q_{eff}/q of 2.6×10^{11} and 0 cm^{-2} are plotted in solid and dash lines, respectively. We define the term "Q_{eff}" as the total oxide charges in the oxide, including

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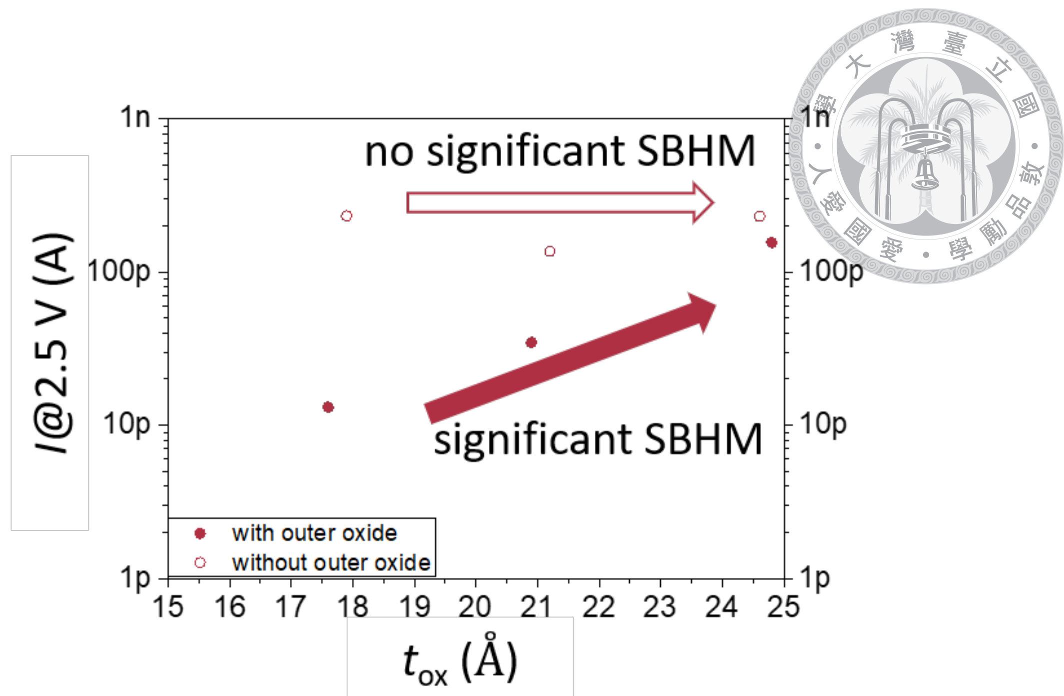

Figure 2–10. The reverse biased current at V_G = 2.5 V for devices with and without outer oxide. A more significant SBHM effect is observed for the devices with outer oxide.

oxide fixed charges, oxide trap charges, ions, and interface charges. "Q_{eff}" will be used throughout this work. In **Figure 2–9** (b), one can observe that the MISTD with Q_{eff}/q = 2.6×10^{11} cm^{-2} holds a constant capacitance value to a higher bias voltage, similar to the MISTD with outer oxide in the experiment. However, for the MISTD with Q_{eff}/q = 0 cm^{-2}, the device is in the DD region in the whole positive bias region because lacking $-J_{gen,lateral}$. The detailed quantitative discussion on the impact of outer oxide charges on HFCV will be described in **Chapter 3**.

Outer oxide charges will affect the amount of $-J_{gen,lateral}$ and the formation of the inversion layer. Different levels of the amount of inversion charges will affect V_{ox} and the level of SBHM. The extracted reverse bias currents at V_G = 2.5 V from **Figure 2–5** are shown in **Figure 2–10**. With the existing outer oxide and $-J_{gen,lateral}$, V_{ox} is easier to increase, and the SBHM effect is easier to appear for MISTD with outer oxide. Theoretically, MISTDs

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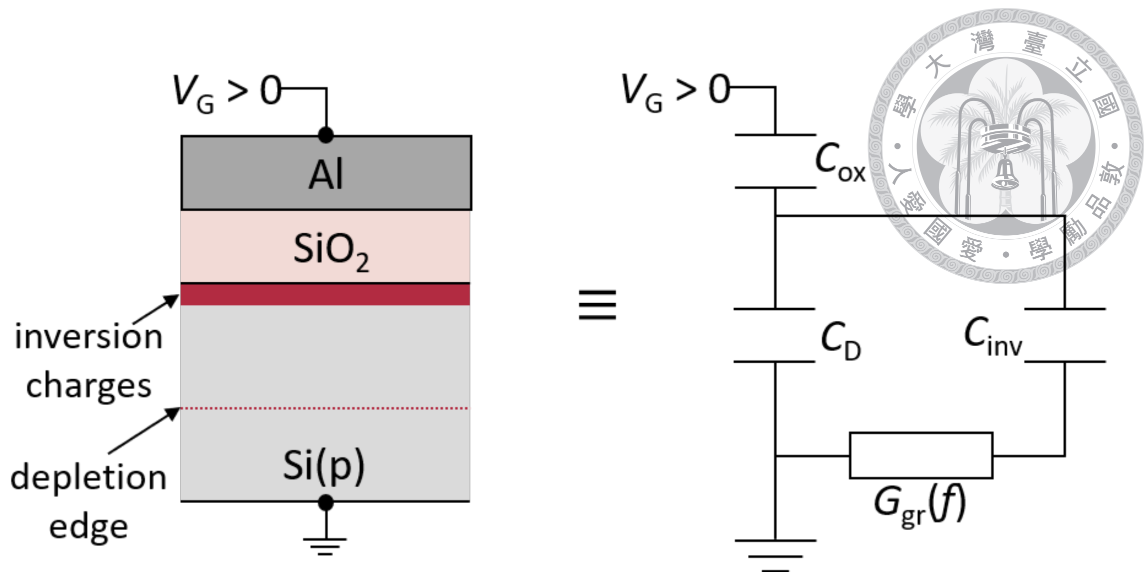

Figure 2–11. The equivalent circuit for the MOS structure, which is biased in the strong inversion region without considering the outer region.

with outer oxide have an extra minority carriers supply and a more significant SBHM. They should have a higher current level compared with MISTD without outer oxide. However, because of the edge defects formed in the SiO_2 etching process, the currents of MISTDs without outer oxide are much more difficult to be predicted exactly [39]. Discussion of current behavior without outer oxide is out of the scope of this work. An analytical model of the impact of outer oxide charges on the SBHM effect will be discussed in **Chapter 4**.

2.3.4 Frequency Dependency of Capacitance in MISTD

CF property of MOS structure is widely discussed and usually used to extract the carrier lifetime of the semiconductor [6, 7]. The equivalent circuit of a MOS structure measured under the strong inversion is shown in **Figure 2–11** [7]. In **Figure 2–11** , C_{ox} is the capacitance of oxide layer, C_D is the capacitance of depletion region, C_{inv} is the capacitance of inversion layer, and $G_{gr}(f)$ is the effective conductance from the generation-recombination process depending on measuring frequency f. $G_{gr}(f)$ will increase with decreasing f

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and lead to the rising of the measured capacitance [7]. Usually, the measured capacitance value does not significantly rise at $f > 100$ Hz for silicon substrate [33] because of its slow thermal generation process [50]. For $f > 100$ Hz, $G_{gr}(f)$ is negligibly small. In this situation, the measured capacitance can be seen as a series connection of C_{ox} and C_D, and is independent of frequency.

Figure 2–12 shows the measured CV relations at 300, 100, 30, 10, 3, and 1kHz. Devices with and without outer oxide are shown in **Figure 2–12** (a) and (b), respectively. No significant frequency dispersion is observed in **Figure 2–12** (b) for the device without outer oxide because the lowest measuring frequency is 1kHz, which is still in the high-frequency region for a silicon substrate. Though the experimental result in **Figure 2–12** (b) matches the mechanism discussed in **Figure 2–11** , the measured result in **Figure 2–12** (a) significantly increases at 1kHz. The increasing capacitance value for the device with outer oxide is also attributed to the impact of outer oxide charges.

2.3.5 Impact of Outer Oxide Charges on the Capacitance-Frequency Relation of MISTD

The mechanism of how the outer oxide charges affecting the capacitance value is shown in **Figure 2–13** . Similar to the discussion in **Figure 2–8** , the applied potential on the electrode will laterally extend through the conduction channel induced by outer oxide charges. The lateral extending distance $\ell_{AC}(f)$ will increase the device's effective control area and the measured capacitance value. Because of the RC delay in the lateral conducting channel, $\ell_{AC}(f)$ depends on the measuring frequency f and leads to the frequency dispersion observed in **Figure 2–12** (a). The rising capacitance value at $f > 100$ Hz does not stem from the generation-recombination process described in **Section 2.3.4** but from the vary-

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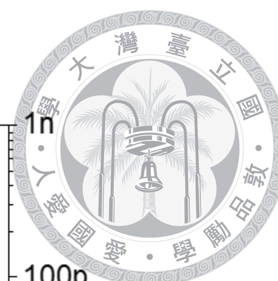

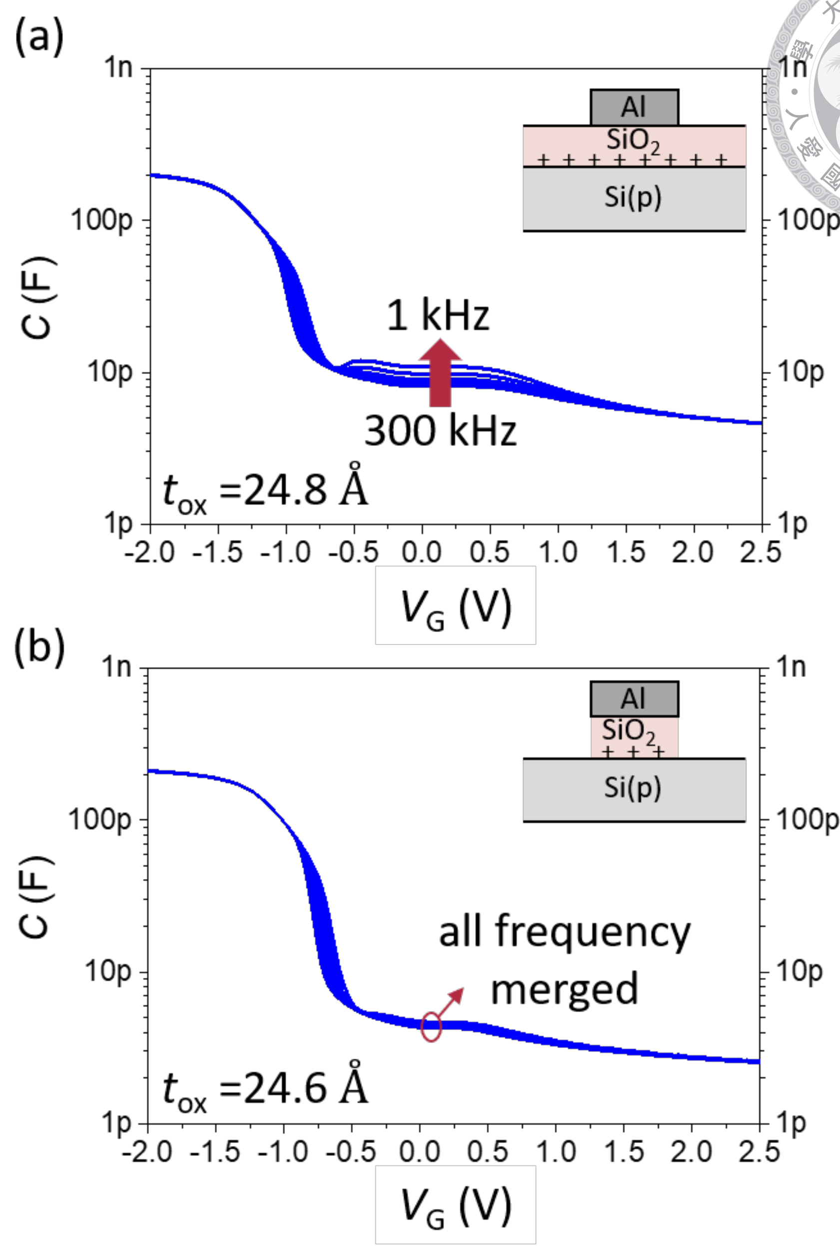

Figure 2–12. The measured CV characteristics of devices (a) with and (b) without outer oxide. The measuring frequency varies from 300, 100, 30, 10, 3, to 1kHz. A significant frequency dispersion is observed for the device with outer oxide.

ing lateral control area.

To further confirm the concept, we extract the normalized CF relations at $V_G = 0$ V in **Figure 2–12** and compare them with TCAD simulation. The CF relations are normalized

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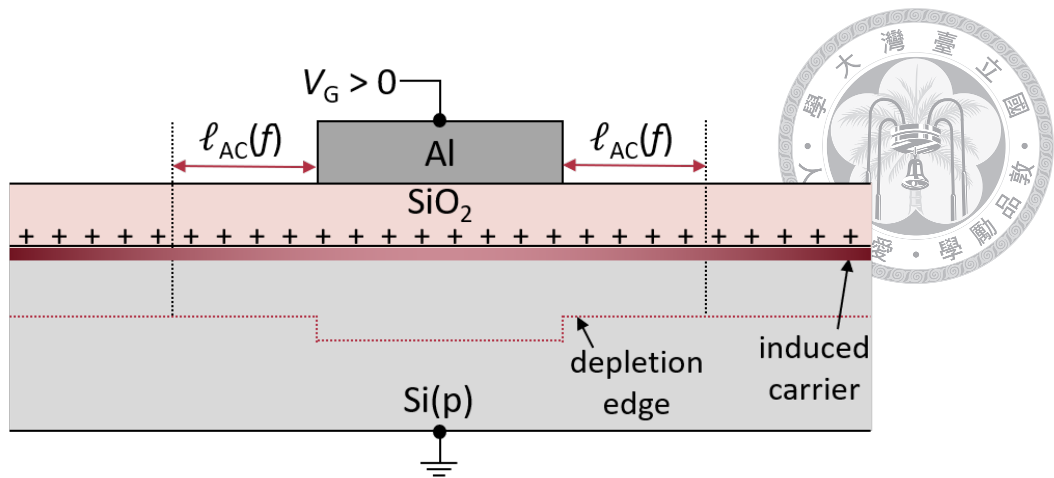

Figure 2–13. Schematic of lateral control distance $\ell_{AC}(f)$. $\ell_{AC}(f)$ depends on measuring frequency because of the RC delay in the lateral conducting channel.

to the capacitance value at the highest frequency. The extracted CF relations from the experiments and TCAD simulation are shown in **Figure 2–14** (a) and (b), respectively. From **Figure 2–14** (a), one can observe that the capacitance value of the device with outer oxide increases by more than 30% when the measuring frequency decreases from 300kHz to 1kHz. However, for the device without outer oxide, the capacitance value only increases by less than 10% in the same frequency range. The observation implies that the outer oxide plays an important role in the CF relation of MISTD. In TCAD simulation, devices with Q_{eff}/q of 2.8×10^{11} and 0 cm^{-2} are shown. The capacitance value of the device with oxide charges increases by over 40% from 1 MHz to 1 kHz. On the other hand, no increase in capacitance value is observed for the device without oxide charges. One can find that there is about a 10% difference between the experimental and the simulation devices without oxide charges. This phenomenon may be attributed to the existence of surface charges and the native oxide for the experimental device. The quantitative calculation for the impact of outer oxide charges on the CF relation will be described in **Chapter 5**.

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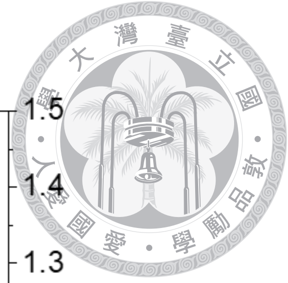

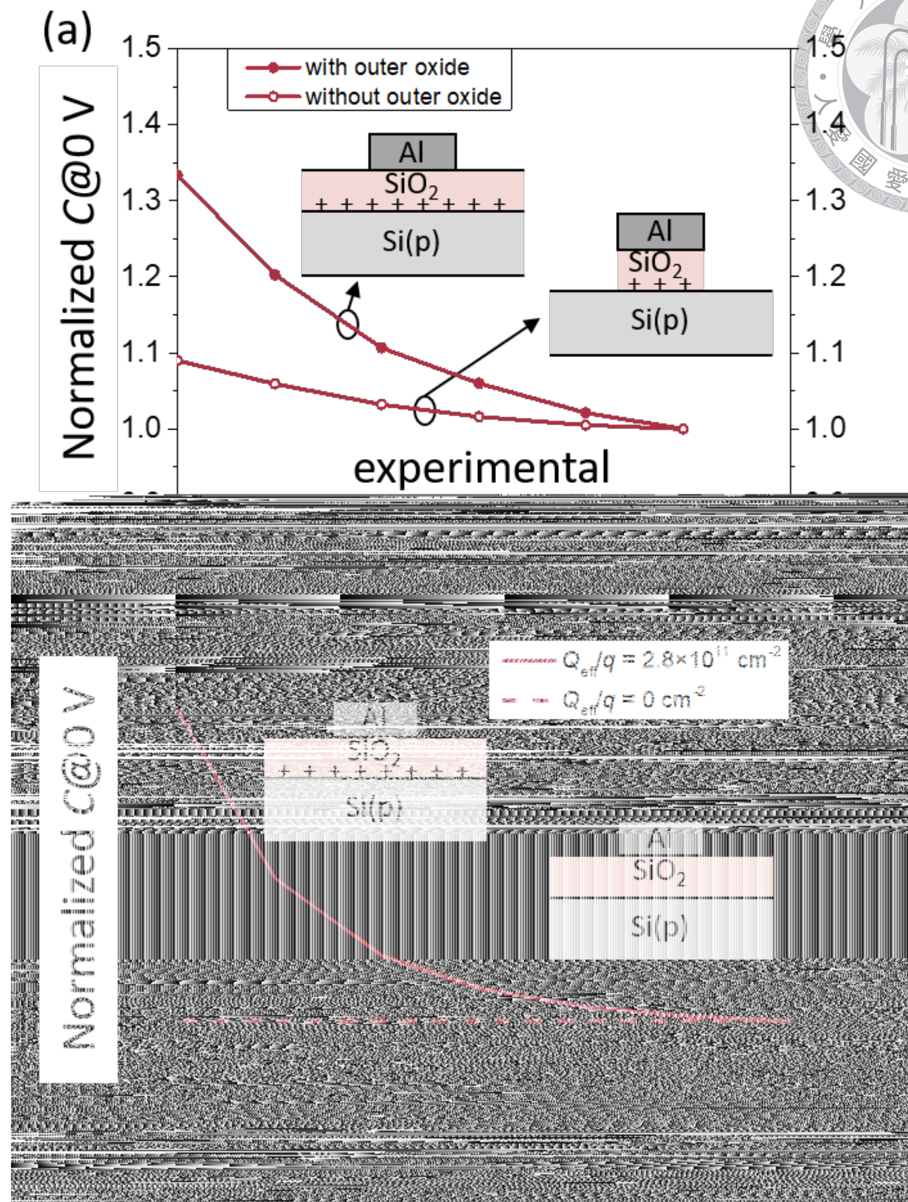

Figure 2–14. Normalized CF relation of MISTD from (a) experimental and (b) TCAD simulation. The measured results of devices with and without oxide are shown. Simulated result of devices with Q_{eff}/q of 2.8×10^{11} and 0 cm^{-2} are selected for comparison.

2.4 Summary

In this chapter, we review the mechanism of DD in HFCV, SBHM in IV, and frequency dispersion in CF in beginning. The above mechanisms had been mentioned in [11,44], [24],

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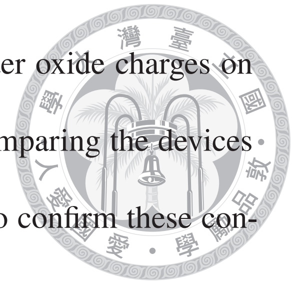

and [7], respectively. Here, it is the first time that the impact of outer oxide charges on these mechanisms is highlighted. The impact was pointed out by comparing the devices with and without outer oxide. TCAD simulations are also adopted to confirm these concepts. A quantitative analysis of the impact of oxide charges will be carried out in the following chapters.

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3

Modeling I: Impact of Oxide Charge on the High-Frequency Capacitance (Electrostatic) Characteristic of MISTD

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3.1 Background

The distribution of the voltage on the oxide layer and semiconductor under a certain applied voltage V_G had been decided by the theory of MOS capacitor [7]. Potentials on the oxide layer and semiconductor are traditionally named as V_{ox} and ψ_s, respectively. By distinguishing the applied voltage in accumulation, depletion, and inversion regions, the distribution of V_{ox} and ψ_s can be calculated analytically. The theory of MOS capacitors has been widely used in evaluating the properties of MOS capacitors and metal-oxide-semiconductor field-effect transistors (MOSFET) in the past few decades.

However, with the scaling down of the technology nodes, the thinner gate oxide is required to avoid severe short-channel effects (SCE). Significant leakage current appears with a thin gate oxide, making the traditional MOS capacitor's theory invalid. In 1990s, several works focused on studying ultra-thin oxide's leakage current [10,51,52]. Although the leakage current is well discussed in these works, the situation is different from the MISTD. These works discussed the MOS structures with the heavily doped substrate [51], biased in accumulation region [10], and on MOSFET [52]. The methods used in the above works created an environment to let the additional applied voltage mainly drops on the oxide layers. **Figure 3–1** (a) shows the band diagrams of MOS structure on MOSFET for comparison. When the bias voltage V_G increases, the inversion layer is efficiently built-up because of sufficient electron supply from the S/D region. The additional bias voltage drops on the oxide layer, and the silicon's surface band bending ψ_s keeps at around $2\phi_F$. With the applied voltage mainly drops on V_{ox}, one can reduce the complexity when discussing the current-voltage relation of ultra-thin oxide.

Nevertheless, the current-voltage relation discussed in [10, 51, 52] differs from the sit-

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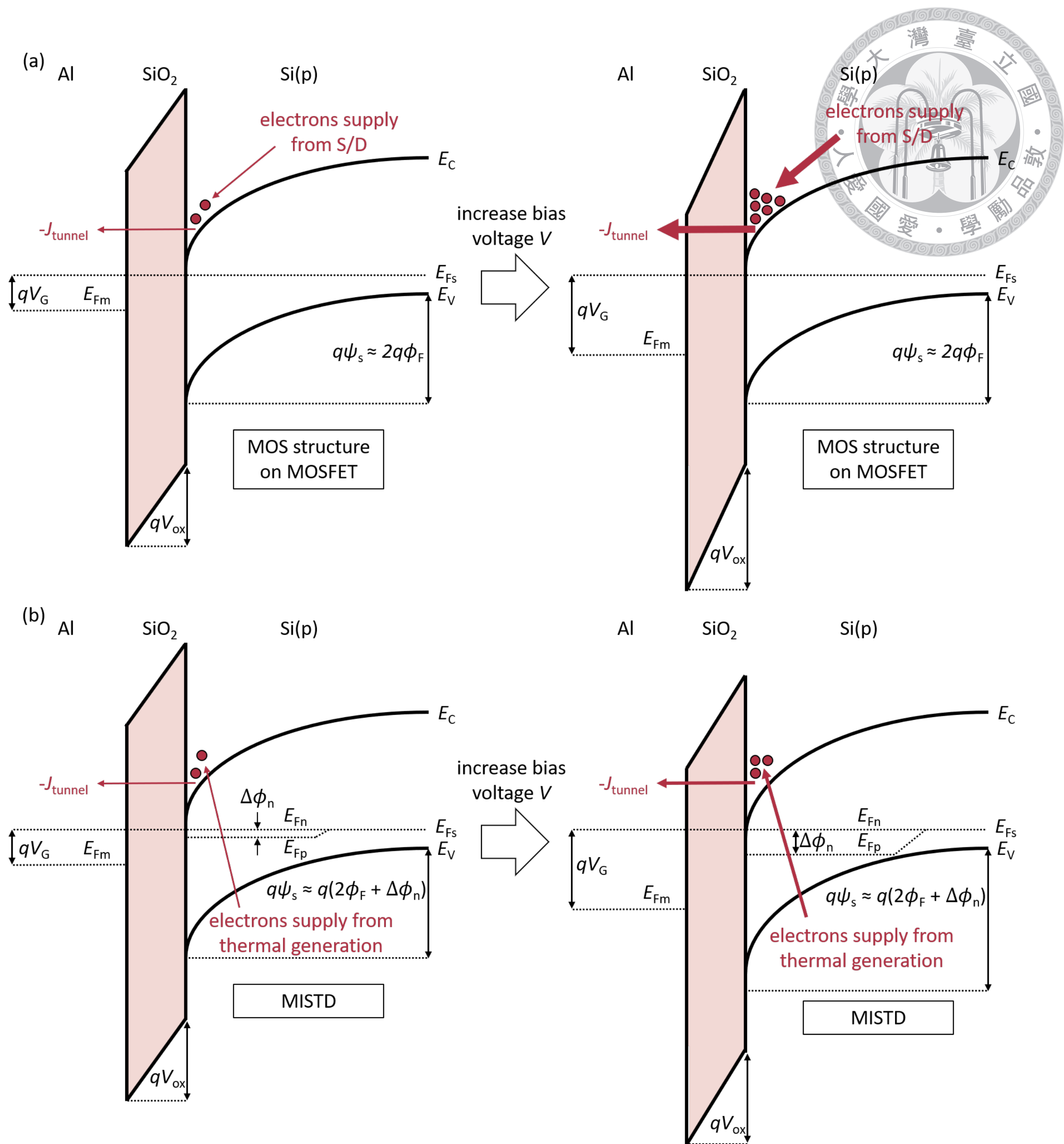

Figure 3–1. Band diagrams of (a) MOS structure on MOSFET and (b) MISTD. For MOS structure on MOSFET, most increased voltage drops on the oxide layer. However, the additional applied voltage drops partially on the oxide layer and partially on the silicon substrate for MISTD.

uation in MISTD. The band diagram of MISTD is plotted in **Figure 3–1** (b). When the bias voltage increases, the inversion layer cannot form as efficiently as the MOS structure on MOSFET because of the supplement of electrons mainly comes from thermal generation. Thermal generation is a relatively slow process for silicon [50]. As shown

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in **Figure 3–1** (b), the additional applied voltage on MISTD drops partially on the oxide layer and partially on the silicon substrate. The works discussing oxide leakage current usually avoid using MISTD with moderate doping concentration and with bias in inversion region [10, 51, 52] because of its complex voltage distribution.

However, many applications of MISTD discussed in **Section 1.1** utilize the leakage current in the inversion region. Fortunately, it is found that most of the applied voltage on MISTD drops on the oxide layer before a critical voltage V_C. After V_C, the device will go into the DD region, and most additional voltage increases on the silicon substrate. [44] Recently, our group proposed an analytical model to determine the relation between V_C and oxide thickness t_{ox} [16]. However, there is a systematical deviation between the model and the experimental result. The origin of this devistion is of interst. This chapter proposes an improved model based on [16] to explain the observed deviation. This model can correctly describe the voltage distribution within MISTD, which is important for calculating the SBHM effect and hole currents discussed in the next chapter.

3.2 Model Derivation

As discussed in **Section A.1**, a cylindrical coordinate is adopted for modeling. The coordinate is also attached in **Figure 3–2** (a). The origin of radial direction r is at the center of the device, and the origin of depth y is at the interface of the oxide layer and substrate. From **Figure 3–2** (a), one can find that the electron current components need to satisfy the condition of

$$I_{\text{tunnel}} = I_{\text{gen,bulk}} + I_{\text{gen,lateral}} \tag{3.1}$$

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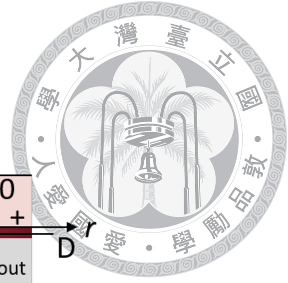

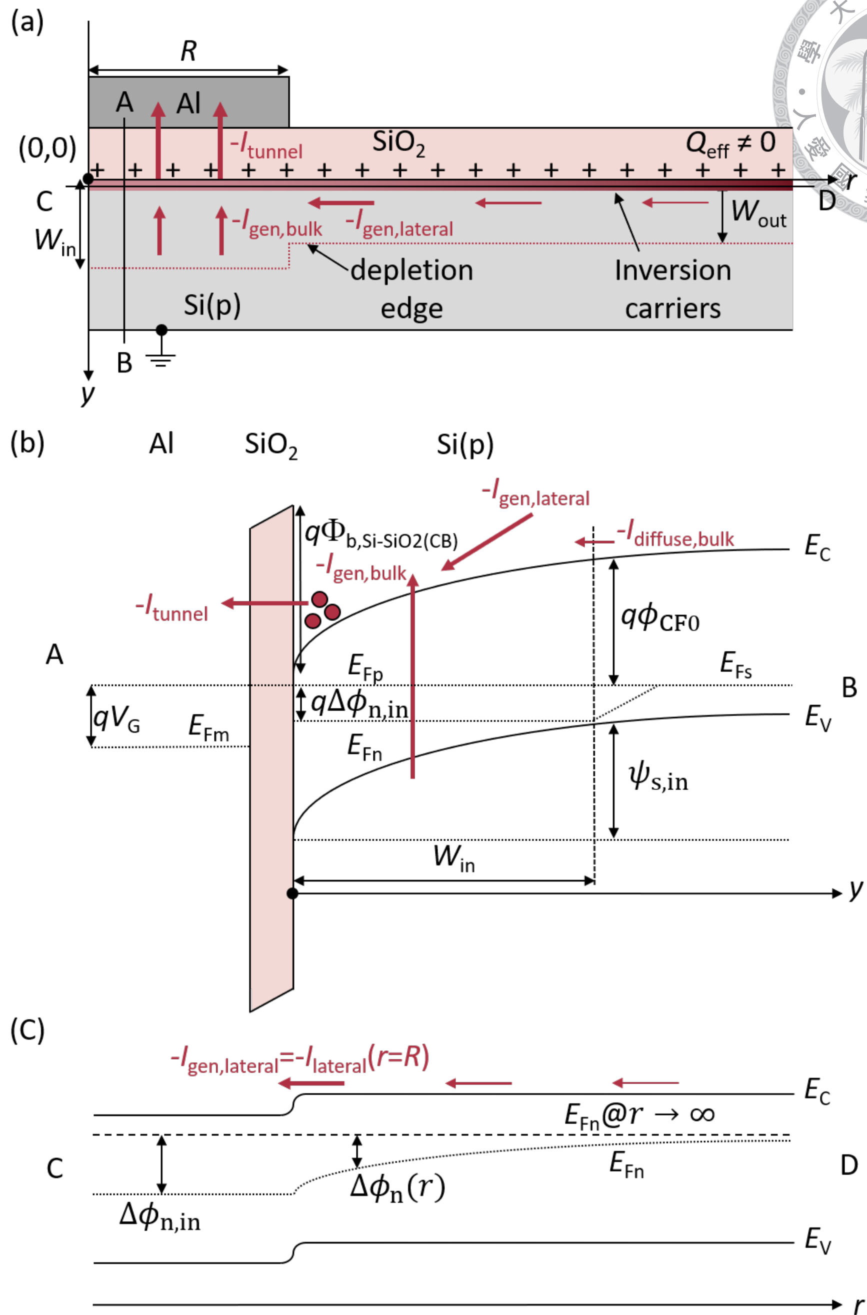

Figure 3–2. (a) Device structure and coordinate for modeling. (b) and (c) are band diagrams at cut lines $\overline{AB}$ and $\overline{CD}$ in (a), respectively.

under steady state, where I_{tunnel} is the tunneling current, $I_{gen,bulk}$ is the generation current under the electrode, and $I_{gen,lateral}$ is the generation current outside the electrode. In **Section 3.2.1**, some approximations will be adopted to reduce the complexity of modeling.

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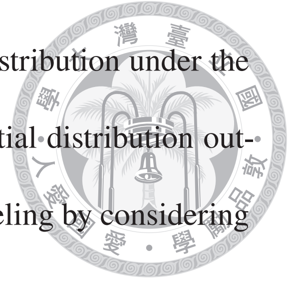

Section 3.2.2 calculates I_{tunnel}, $I_{\mathrm{gen,bulk}}$ and discusses the potential distribution under the electrode. **Section 3.2.3** calculates $I_{\mathrm{gen,lateral}}$ and discusses the potential distribution outside the electrode. Finally, **Section 3.2.4** gives a process flow of modeling by considering (3.1).

3.2.1 Approximations

Some major approximations were adopted in the model. They are:

1. The effect of image force lowering [1] is neglected.
2. Quantum confinement at the silicon surface [1] is neglected.
3. The fringing field effect is neglected.
4. Assume the hole quasi-Fermi level E_{Fp} and electron quasi-Fermi level E_{Fn} are independent of y [53].
5. Although holes will inject from the electrode when the SBHM effect is significant [24, 40], we assume the holes will quickly be swept away by the surface field and not affect the electrostatic of MISTD. In other words, it is assumed that the electrostatic of MISTD is governed by electrons and space charges.
6. Assume all the oxide charges are fixed oxide charges, and the amount is independent of bias, frequency, and time.
7. WKB approximation is adopted to calculate the tunneling probability of the oxide layer.
8. Assume the generation of minority carriers is governed by the Shockley-Read-Hall process [54, 55].

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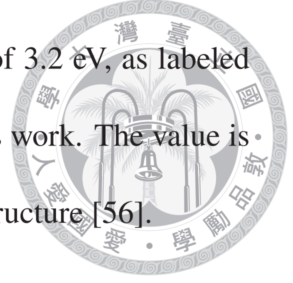

9. The conduction band energy difference between Si and SiO_2 of 3.2 eV, as labeled by $q\Phi_{\text{b,Si-SiO2(CB)}}$ in **Figure 3–2** (b), is adopted throughout this work. The value is extracted according to the photoinjected current of the MOS structure [56].

10. Electron effective mass in the oxide of $m_{\text{ox,e}} = 0.42m_0$ is used in this work. The value is extracted according to the Fowler-Nordheim tunneling current of the MOS structure. [57].

3.2.2 Potential Distribution Under Electrode

In this section, we discuss the potential distribution under the electrode assuming a known surface band bending $\psi_{\text{s,in}}$, when biasing a specific voltage V_{G} on the MISTD with known oxide thickness t_{ox}. The band diagram under the electrode is plotted in **Figure 3–2** (b). With known V_{G}, V_{FB}, $\psi_{\text{s,in}}$, one can calculate the oxide voltage by

$$V_{\text{ox}} = V_{\text{G}} - V_{\text{FB}} - \psi_{\text{s,in}}. \tag{3.2}$$

Silicon charges concentration under the electrode $Q_{\text{s,in}}$ can be written down as

$$Q_{\text{s,in}} = -C_{\text{ox}}V_{\text{ox}}. \tag{3.3}$$

Considering that the electron and hole quasi-Fermi levels are independent of depth y, $Q_{\text{s,in}}$ can be approximated as

$$Q_{\text{s,in}} = -C_{\text{ox}}V_{\text{ox}} \approx -\sqrt{2\epsilon_{\text{si}}kTN_{\text{a}}}\left[\frac{q\psi_{\text{s,in}}}{kT} + \frac{n_{\text{i}}^2}{N_{\text{a}}^2}e^{q(\psi_{\text{s,in}}-\Delta\phi_{\text{n,in}})/kT}\right]^{1/2}, \tag{3.4}$$

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where ϵ_{si} is the permittivity of silicon, N_a is the doping concentration, n_i is the intrinsic carrier concentration of silicon, and $\Delta\phi_{n,in}$ is the difference of electron and hole quasi Fermi level under the electrode. $\Delta\phi_{n,in}$ can be solved by rearranging (3.4) as

$$\begin{aligned}\Delta\phi_{n,in} &= \psi_{s,in} - \frac{kT}{q}\ln\left[\frac{N_a^2}{n_i^2}\left(\frac{C_{ox}^2 V_{ox}^2}{2\epsilon_{si} kTN_a} - \frac{q\psi_{s,in}}{kT}\right)\right] \\ &= \psi_{s,in} - 2\phi_F - \frac{kT}{q}\ln\left(\frac{Q_{s,in}^2}{2\epsilon_{si} kTN_a} - \frac{q\psi_{s,in}}{kT}\right).\end{aligned} \tag{3.5}$$

With known V_G, V_{ox}, $\psi_{s,in}$, and $\Delta\phi_{n,in}$, the shape of the band diagram in **Figure 3–2** (b) can be precisely defined, and each current component can be calculated.

The total generation current under electrode $-I_{gen,bulk}$ can be simplified by neglecting the minority carrier concentration in the depletion region:

$$-I_{gen,bulk} = -qA\int_0^{W_{in}(\psi_{s,in})} \frac{n_i}{2\tau_0}\frac{1 - e^{-q\Delta\phi_{n,in}/kT}}{1 + \frac{N_a}{2n_i}e^{-q\psi_{in}(y)/kT}}dy, \tag{3.6}$$

where A is the device area, $W_{in}(\psi_{s,in})$ is the depletion width under the electrode depending on $\psi_{s,in}$, τ_0 is the average of electron and hole carrier life time, $\psi_{in}(y)$ is the band bending under the electrode depending on y. In this work, the dependency of τ_0 on doping concentration is considered [1] (e.g. $\tau_0 = 2.9 \times 10^{-5}$ sec for $N_a = 10^{16}$ cm^{-3}). Depletion approximation is adopted to calculate $W_{in}(\psi_{s,in})$ and $\psi_{in}(y)$ as

$$W_{in}(\psi_{s,in}) = \sqrt{\frac{2\epsilon_{Si}\psi_{s,in}}{qN_a}}, \tag{3.7}$$

and

$$\psi_{in}(y) = \psi_{s,in}\left(1 - \frac{y}{W_{in}}\right)^2. \tag{3.8}$$

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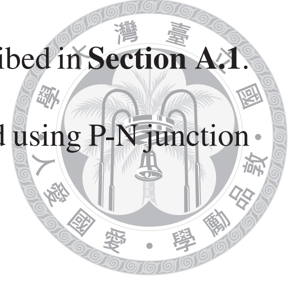

The derivation process of (3.6) is the same as (A.14) and is finely described in **Section A.1**. The diffusion current under the electrode $-I_{\text{diffuse,bulk}}$ can be calculated using P-N junction current theory [1]:

$$-I_{\text{diffuse,bulk}} = -\frac{qAD_\text{n}n_\text{i}^2}{L_\text{n}N_\text{a}}(1 - e^{-q\Delta\phi_{\text{n,in}}/kT}), \tag{3.9}$$

where D_n is the diffusion coefficient of electron, L_n is the diffusion length of electron. However, as discussed in **Section A.1**, the diffusion current is about two orders lower than the generation current for silicon. $-I_{\text{diffuse,bulk}}$ is neglected in our model.

We then calculate the leakage current by using the surface potential-based compact model (SP model) [58]. The model simplifies the calculation of tunneling current by assigning the tunneling probability at the lowest allowable energy to all energy levels. The tunneling current $-I_{\text{tunnel}}$ as plotted in **Figure 3–2** (a) can be expressed as

$$I_{\text{tunnel}} = A \cdot J_{\text{tunnel,0}} \cdot P_\text{t} \cdot S, \tag{3.10}$$

where $J_{\text{tunnel,0}}$ is a value depends on material and temperature, P_t is the tunneling probability at the lowest allowable energy, and S is the supply function. The value $J_{\text{tunnel,0}}$ is

$$J_{\text{tunnel,0}} = \frac{qm^* k^2 T^2}{2\pi^2\hbar^3}, \tag{3.11}$$

where $m^* = 0.92m_0$ is the longitudinal electron effective mass for silicon [1], $\hbar$ is the reduced Planck constant. P_t can be calculated by WKB approximation. For $V_{\text{ox}} > \Phi_{\text{b,Si-SiO2(CB)}}$,

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the oxide barrier is a triangular shape with the tunneling probability of

$$P_{\mathrm{t}} = \exp\left(- \frac{4\sqrt{2m_{\mathrm{ox,e}}}\left(q\Phi_{\mathrm{b,Si\text{-}SiO2(CB)}}\right)^{3/2}}{3\hbar q\varepsilon_{\mathrm{ox}}} \right), \tag{3.12}$$

where $\varepsilon_{\mathrm{ox}} = V_{\mathrm{ox}}/t_{\mathrm{ox}}$ is the oxide field. For $V_{\mathrm{ox}} < \Phi_{\mathrm{b,Si\text{-}SiO2(CB)}}$, the oxide barrier is a trapezoidal shape with the tunneling probability of

$$P_{\mathrm{t}} = \exp\left(- \frac{4\sqrt{2m_{\mathrm{ox,e}}}\left(q\Phi_{\mathrm{b,Si\text{-}SiO2(CB)}}\right)^{3/2}\left[1 - \left(1 - V_{\mathrm{ox}}/\Phi_{\mathrm{b,Si\text{-}SiO2(CB)}}\right)^{3/2}\right]}{3\hbar q\varepsilon_{\mathrm{ox}}} \right). \tag{3.13}$$

The supply function S is determined by the energy difference between the conduction band and Fermi levels in metal and silicon as

$$\begin{aligned} S &= \ln\left[\frac{1 + \exp\left(- \frac{E_{\mathrm{C}}(y=0) - E_{\mathrm{Fn}}}{kT} \right)}{1 + \exp\left(- \frac{E_{\mathrm{C}}(y=0) - E_{\mathrm{Fm}}}{kT} \right)} \right] \\ &= \ln\left[\frac{1 + \exp\left(- \frac{q(\phi_{\mathrm{CF0}} - \psi_{\mathrm{s,in}} + \Delta\phi_{\mathrm{n,in}})}{kT} \right)}{1 + \exp\left(- \frac{q(\phi_{\mathrm{CF0}} - \psi_{\mathrm{s,in}} + V)}{kT} \right)} \right], \end{aligned} \tag{3.14}$$

where ϕ_{CF0} is the potential difference between bulk hole quasi Fermi level and bulk conduction band in silicon. ϕ_{CF0} is also labelled in **Figure 3−2** (b).

From the above discussion, one can calculate $I_{\mathrm{gen,bulk}}$ and I_{tunnel} with known V_{G}, $\psi_{\mathrm{s,in}}$, and t_{ox}. We will calculate $I_{\mathrm{gen,lateral}}$ in the next section to find out all terms in (3.1).

3.2.3 Potential Distribution Outside Electrode

Figure 3−2 (c) shows the profile of $\Delta\phi_{\mathrm{n}}(r)$ outside the electrode. One can observe that the two boundary conditions of $\Delta\phi_{\mathrm{n}}(r)$ are

$$\Delta\phi_{\mathrm{n}}(r = R) = \Delta\phi_{\mathrm{n,in}}, \tag{3.15}$$

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and

$$\Delta\phi_{\rm n}(r \to \infty) = 0, \tag{3.16}$$

where R is the radius of the electrode. Thus, $I_{\rm gen,lateral}$ can be decided by $\Delta\phi_{\rm n,in}$. Fortunately, $\Delta\phi_{\rm n,in}$ can be calculated from known $V_{\rm G}$, $\psi_{\rm s,in}$, and $t_{\rm ox}$ by (3.2) to (3.5). In other words, $I_{\rm gen,lateral}$ is able to be calculated from $V_{\rm G}$, $\psi_{\rm s,in}$, and $t_{\rm ox}$. With the detailed calculation in **Appendix A**, we find that $\Delta\phi_{\rm n}(r)$ satisfies (A.32)

$$1 - e^{-q\Delta\phi_{\rm n}(r)/kT} = \frac{1 - e^{-q\Delta\phi_{\rm n,in}/kT}}{K_0(\alpha R)} K_0(\alpha r), \tag{3.17}$$

where K_0 is modified Bessel functions of the second kind with orders 0, and α is the inversion of lateral coupling length Λ

$$\Lambda = \alpha^{-1} = \left[\frac{qN_{\rm a}}{2\tau_0 kT\mu_{\rm n} n_{\rm i}} \frac{\int_0^{W_{\rm out}} \frac{dy}{1+\frac{N_{\rm a}}{2n_{\rm i}} e^{-q\psi_{\rm out}(y)/kT}}}{\int_0^{W_{\rm out}} e^{q\psi_{\rm out}(y)/kT} dy} \right]^{-1/2}, \tag{3.18}$$

where $\mu_{\rm n}$ is the electron mobility, $n_{\rm i}$ is the intrinsic carrier concentration for silicon, $W_{\rm out}$ is the depletion width outside the electrode, and $\psi_{\rm out}(y)$ is the band bending outside the electrode. In this work, the dependency of $\mu_{\rm n}$ on doping concentration is considered [1,59] (e.g. $\mu_{\rm n} = 1255\,{\rm cm^2V^{-1}sec^{-1}}$ for $N_{\rm a} = 10^{16}\,{\rm cm^{-3}}$). $W_{\rm out}$ and $\psi_{\rm out}(y)$ are induced by total effective oxide charges $Q_{\rm eff}$. We calculate $W_{\rm out}$ and $\psi_{\rm out}(y)$ by using space charge approximation as

$$W_{\rm out} = \frac{Q_{\rm eff}}{qN_{\rm a}}, \tag{3.19}$$

and

$$\psi_{\rm out}(y) = \psi_{\rm s,out}(1 - \frac{y}{W})^2 = \frac{Q_{\rm eff}^2}{2\epsilon_{\rm si} qN_{\rm a}}(1 - \frac{y}{Q_{\rm eff}/qN_{\rm a}})^2, \tag{3.20}$$

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where $\psi_{s,out}$ is the surface band bending outside the electrode. The derivation of (3.19), (3.20), and the validity of space charge approximation are discussed in **Appendix A**. The lateral electron current $I_{lateral}(r)$, mainly contributed by diffusion current, can be calculated by the gradient of electron concentration. The electron concentration is dependent on $\Delta\phi_n(r)$ and $\psi_{out}(y)$. From the detailed calculation in **Appendix A**, $I_{lateral}(r)$ can be expressed as

$$I_{lateral}(r) = -\frac{2\pi q\mu_n n_i^2}{N_a}\left[\int_0^{W_{out}} e^{q\psi_{out}(y)/kT}dy\right] r\frac{d\Delta\phi_n(r)}{dr}e^{-q\Delta\phi_n(r)/kT}. \tag{3.21}$$

The total lateral generation current $I_{gen,lateral}$ is $I_{lateral}(r)$ at $r = R$. Utilizing (3.17), one can calculate $I_{gen,lateral}$ as

$$\begin{aligned} I_{gen,lateral} &= I_{lateral}(r = R) \\ &= \frac{2\pi RkT\mu_n n_i^2\alpha}{N_a}\left[\int_0^{W_{out}} e^{q\psi_{out}(y)/kT}dy\right](1 - e^{-q\Delta\phi_{n,in}/kT})\frac{K_1(\alpha R)}{K_0(\alpha R)}, \end{aligned} \tag{3.22}$$

where K_1 is modified Bessel functions of the second kind with orders 1. With (3.18) to (3.23), $I_{gen,lateral}$ can be calculated with known $\Delta\phi_{n,in}$ under a specific Q_{eff}.

3.2.4 Procedure of Modeling

In **Section 3.2.2** and **Section 3.2.3**, we assume a known $\psi_{s,in}$ under a specific bias voltage V_G. However, $\psi_{s,in}$ is an unknown value initially. Actually, we "guess" a $\psi_{s,in}$ to calculate I_{tunnel}, $I_{gen,bulk}$, and $I_{gen,lateral}$, then check the condition of (3.1) to modify the guessing of $\psi_{s,in}$. In this section, we give a process flow to describe the procedure of modeling in **Figure 3−3** . The calculation of each term in **Figure 3−3** is dependent on the equations discussed above. **TABLE 3−I** show the equations and brief descriptions of each term in

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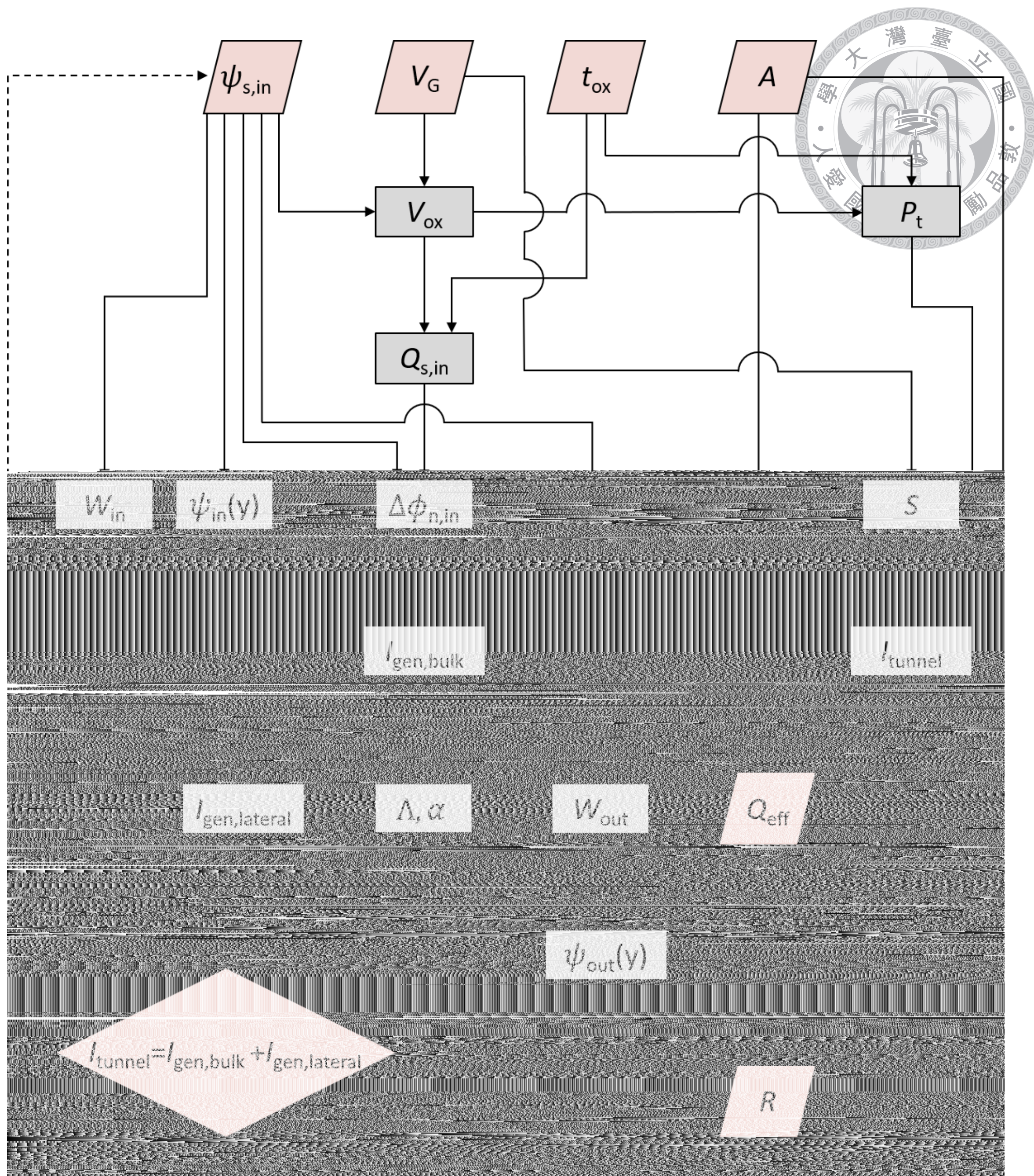

Figure 3–3. The procedure of modeling. The calculation of each term is dependent on the equations discussed in **Section 3.2.2** and **Section 3.2.3**.

Figure 3–3 .

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TABLE 3–I

The corresponding equations to calculate terms in **Figure 3–3**

Term	Description	Unit	Equation
V_{ox}	oxide voltage	V	(3.2)
$Q_{\text{s,in}}$	charge density under electrode	C / cm^2	(3.3)
$\Delta\phi_{\text{n,in}}$	difference of electron and hole quasi-Fermi level under electrode	V	(3.5)
W_{in}	depletion region width under electrode	cm	(3.7)
ψ_{in}	band bending under electrode	V	(3.8)
$I_{\text{gen,bulk}}$	generated electron current under electrode	A	(3.6)
P_{t}	tunneling probability		(3.12), (3.13)
S	supply function		(3.14)
I_{tunnel}	tunneling electron current	A	(3.10)
W_{out}	depletion region width outside electrode	cm	(3.19)
ψ_{out}	band bending outside electrode	V	(3.20)
Λ	lateral decay length	cm	(3.18)
$I_{\text{gen,lateral}}$	generated electron current outside electrode	A	(3.23)

3.3 Experimental Detail

In this chapter, HFCV curves of 11 MISTDs with different oxide thicknesses are measured at 300 kHz. The oxide thicknesses of the devices are 18.7, 19.7, 20.8, 22.1, 23.5, 25.2, 26.5, 27.0, 28.5, 30.0, and 31.3 Å. After the first measurement, the wafers are immersed into the D.I. water for 30 seconds and dried by a Nitrogen gun in the clean room because water can affect the number of oxide charges [60]. HFCV curves of these devices are measured immediately after drying. Using the above mentioned process, one can get two sets of HFCV curves with different amounts of oxide charges. Finally, a device fabricated on another wafer (t_{ox} = 22.8 Å) without immersing in the D.I. water is selected and measured under low temperature to observe the activation energy of lateral decay length Λ.

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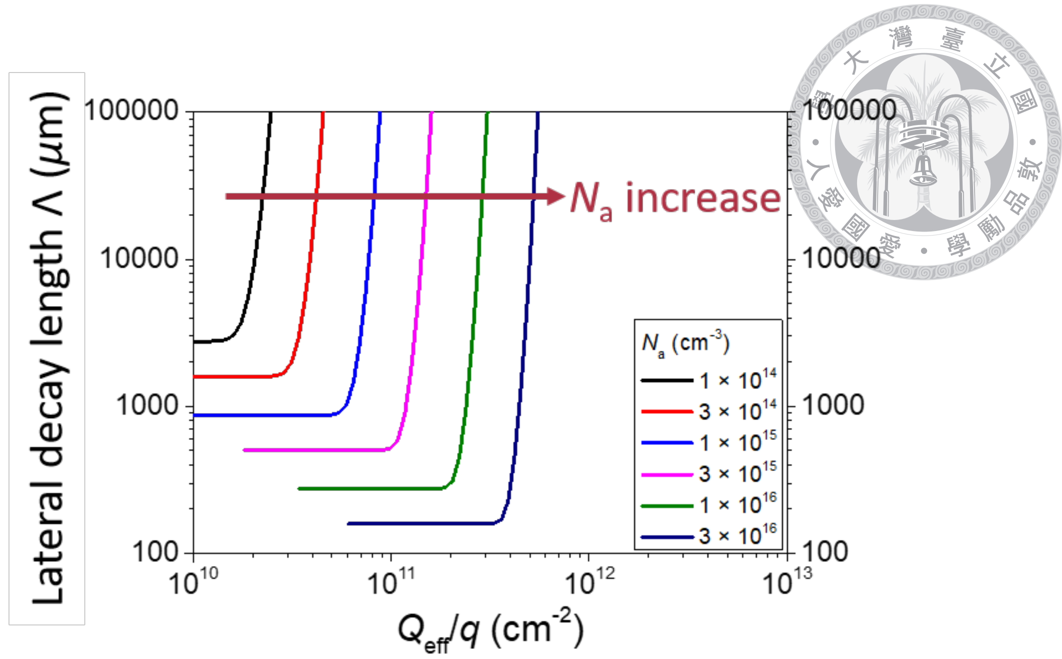

Figure 3–4. Calculated lateral decay length Λ for different N_a and Q_{eff}/q.

3.4 Result and Discussion

3.4.1 Lateral Decay Length and Lateral Electron Supplement

In this section, we discuss the level of impact from the lateral region based on our model. The calculated results of Λ for different N_a and Q_{eff}/q are shown in **Figure 3–4**. **Figure 3–4** shows that the lateral decay length will increase dramatically when the amount of Q_{eff}/q is high enough to induce inversion ($\psi_s > \phi_F$) in the silicon substrate. The amount of needed Q_{eff}/q for inducing inversion increases with doping concentration. When Q_{eff}/q is not large enough to induce inversion, Λ approaches to the diffusion length $\sqrt{D_n \tau_n}$ of the silicon substrate. We further calculate the ratio of $I_{gen,lateral}/I_{gen,bulk}$ v.s. Q_{eff}/q at $V_G = 2.5$ V for $t_{ox} = 25$ Å and $N_a = 10^{16}$ cm^{-3}. The result is plotted in **Figure 3–5**. **Figure 3–5** implies that at $Q_{eff}/q \approx 2.2 \times 10^{11}$ cm^{-2} for $N_a = 10^{16}$ cm^{-3}, $I_{gen,lateral}$ becomes comparable with $I_{gen,bulk}$. If Q_{eff}/q further increases, $I_{gen,lateral}$ will dominate the electron current.

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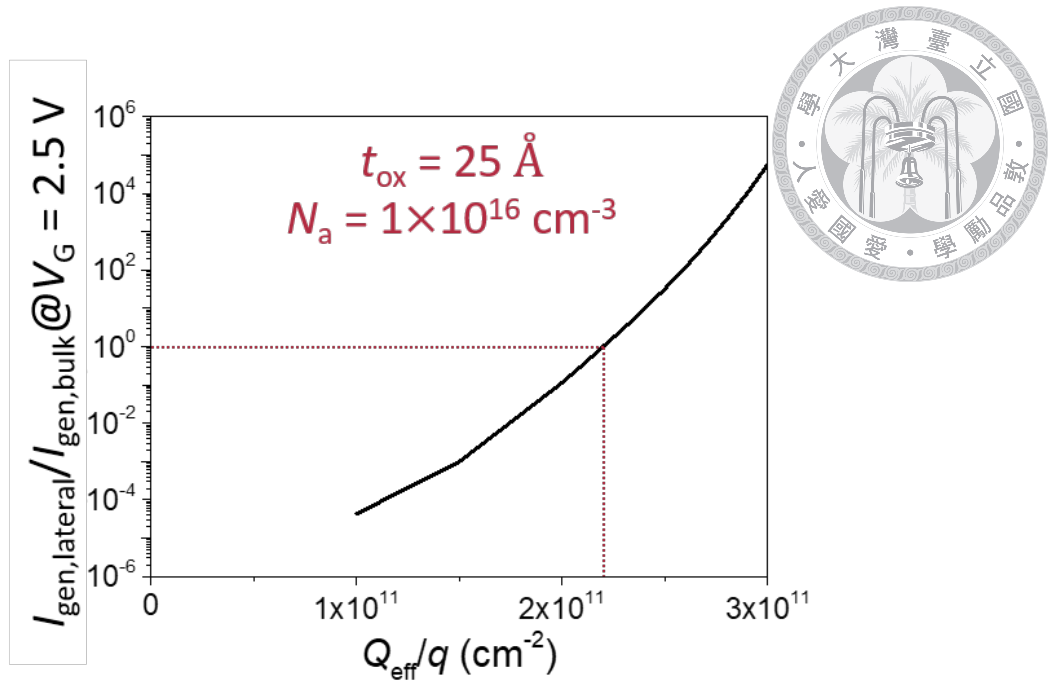

Figure 3–5. Calculated ratio of $I_{\text{gen,lateral}}/I_{\text{gen,bulk}}$ at $V_G = 2.5$ V.

3.4.2 Extraction of Critical Voltage by HFCV

The measured HFCV curves before and after immersing in D.I. water are shown in **Figure 3–6** (a) and (b), respectively. The enlarged parts at 0 to 2.5 V of **Figure 3–6** (a) and (b) are attached in **Figure 3–6** (c) and (d), respectively. From **Figure 3–6** (a) and (b), one can observe that immersing in D.I. water (or increasing outer oxide charges) does not strongly affect the HFCV at the accumulation region. However, **Figure 3–6** (c) and (d) show that the devices can hold constant capacitance values to higher bias voltages after immersing in D.I. water. We attribute the phenomenon to the increase of outer oxide charges and lateral decay length Λ after immersing. To extract the critical voltage V_C we calculate these devices' surface band bending using a high-frequency capacitance model [7]. We further defined that the electron quasi-Fermi level difference $\Delta\phi_{n,in}(V_G)$ is roughly equal to the

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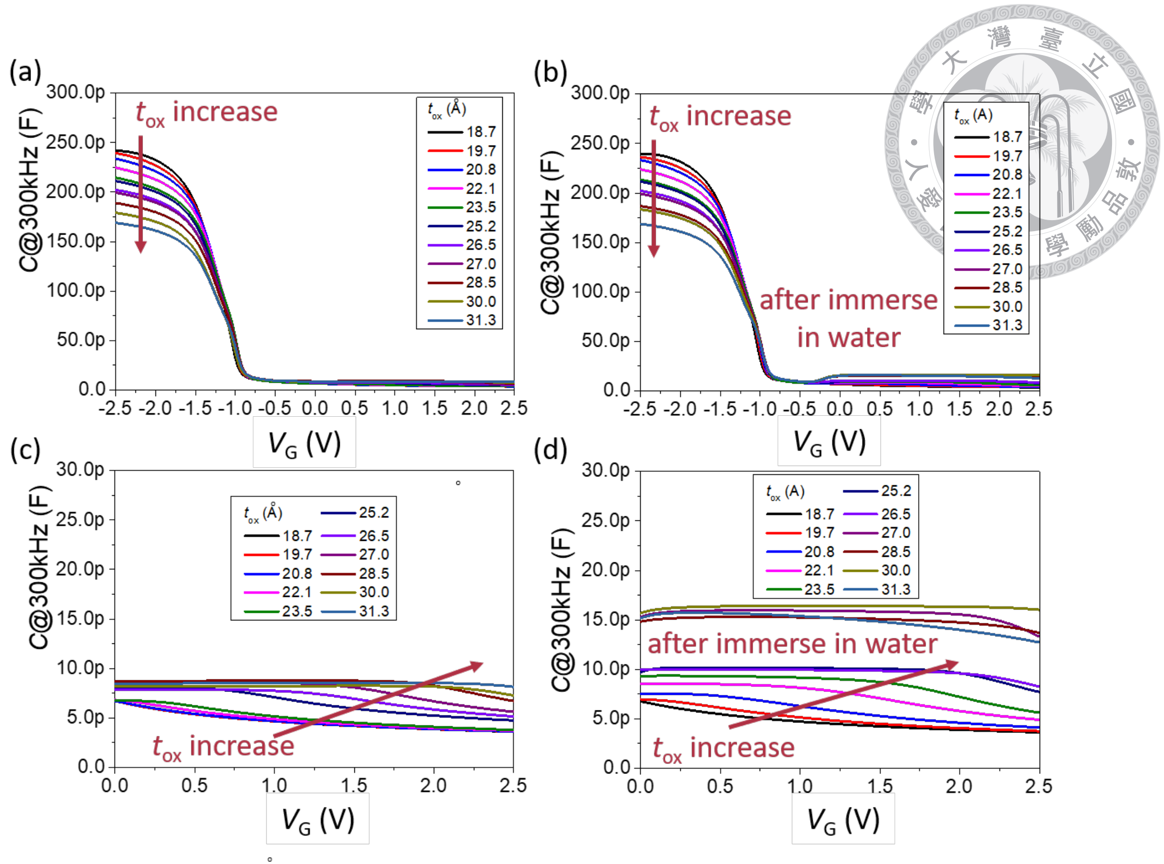

Figure 3–6. Measured HFCV curves (a) before and (b) after immersing in D.I. water. The enlarged parts of (a) and (b) at 0 to 2.5 V are shown in (c) and (d), respectively.

increase of surface band bending $\Delta\psi_{s,in}(V_G)$:

$$\Delta\phi_{n,in}(V_G) \approx \Delta\psi_{s,in}(V_G) = \psi_{s,in}(V_G) - \psi_{s,in}(0), \tag{3.23}$$

where $\psi_{s,in}(V_G)$ and $\psi_{s,in}(0)$ are extracted surface band bending at bias voltage V_G and 0. The extracted $\Delta\psi_{s,in}(V_G)$ curves are shown in **Figure 3–7**. In **Figure 3–7**, one can find that $\Delta\psi_{s,in}(V_G)$ keeps around 0 before a critical voltage and increases almost linearly with the bias voltage after the critical voltage. The saturation of the generation current causes the near linear increase. When $\Delta\phi_{n,in}$ is larger than few kT/q, the term of $1 - \exp(-q\Delta\phi_{n,in}/kT)$ in (3.6) approaches to 1, and the total generation current almost

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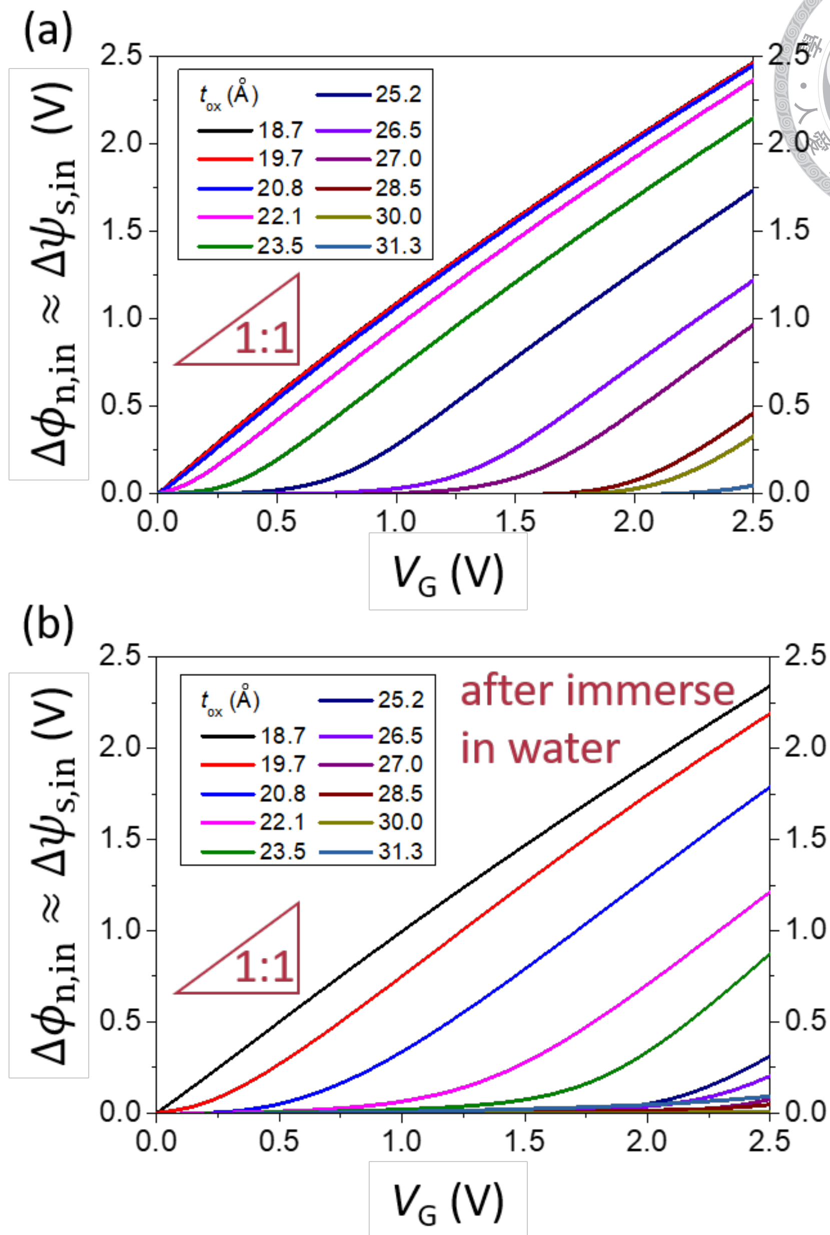

Figure 3–7. Extracted $\Delta\phi_{n,in}(V_G) \approx \Delta\psi_{s,in}(V_G)$ from **Figure 3–6** (a) before and (b) after immersing in D.I. water.

saturate as shown in **Figure A–3**. The saturation of the thermal generation current cannot supply the increase of inversion charges. The number of inversion charges and oxide voltage V_{ox} therefore saturate. Thus, most of the applied voltage drops on the silicon substrate. The modeling result as plotted in **Figure 3–8** can describe the concept in more

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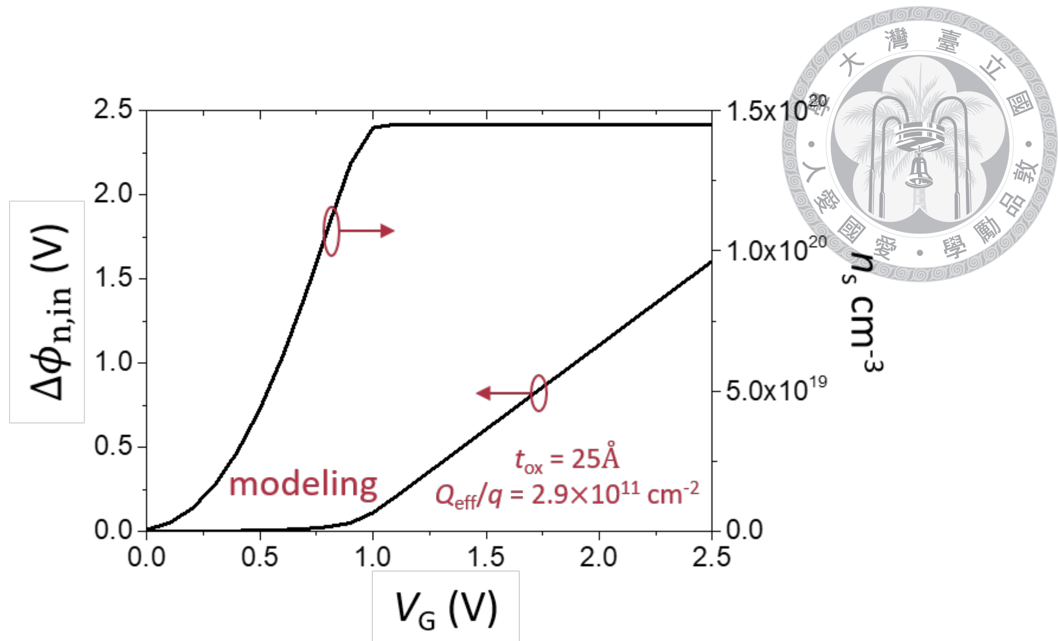

Figure 3–8. The calculated $\Delta\phi_{\mathrm{n,in}}$ and surface electron concentration n_{s} of a device with $t_{\mathrm{ox}} = 25$ Å and oxide charges $Q_{\mathrm{eff}}/q = 2.9 \times 10^{11}$ cm^{-2}.

detail as discussed above. **Figure 3–8** shows the calculated $\Delta\phi_{\mathrm{n,in}}$ and surface electron concentration n_{s} of a device with $t_{\mathrm{ox}} = 25$ Å and oxide charges $Q_{\mathrm{eff}}/q = 2.9 \times 10^{11}$ cm^{-2}. Saturation of n_{s} is observed when $\Delta\phi_{\mathrm{n,in}}$ starts to increase significantly.

We then extract V_{C} of experimental devices at $\Delta\psi_{\mathrm{s,in}}(V_{\mathrm{G}}) = 3kT/q$ from **Figure 3–7**, and compare the experimental V_{C} with modeling. To be mentioned that the thickest device has V_{C} out of our measuring scope before immersing. After immersing, only the six thinnest devices have V_{C} in our measuring scope. The V_{C} before and after the immersion are plotted as square and circle symbols in **Figure 3–9**. The modeling curves of $V_{\mathrm{C}} - t_{\mathrm{ox}}$ at different Q_{eff}/q are plotted as solid lines in **Figure 3–9**. In **Figure 3–9**, one can observe that the V_{C} increases with both t_{ox} and Q_{eff}/q. The tendency of $V_{\mathrm{C}} - t_{\mathrm{ox}}$ can describe by our modeling with Q_{eff}/q around $2.8 - 2.9 \times 10^{11}$ cm^{-2} before immersing. After immersing in D.I. water, the oxide charges and V_{C} increase, and the V_{C} v.s. t_{ox} well fit with modeling at $Q_{\mathrm{eff}}/q = 3.1 \times 10^{11}$ cm^{-2}.

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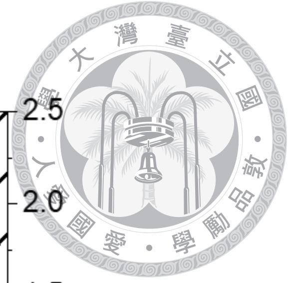

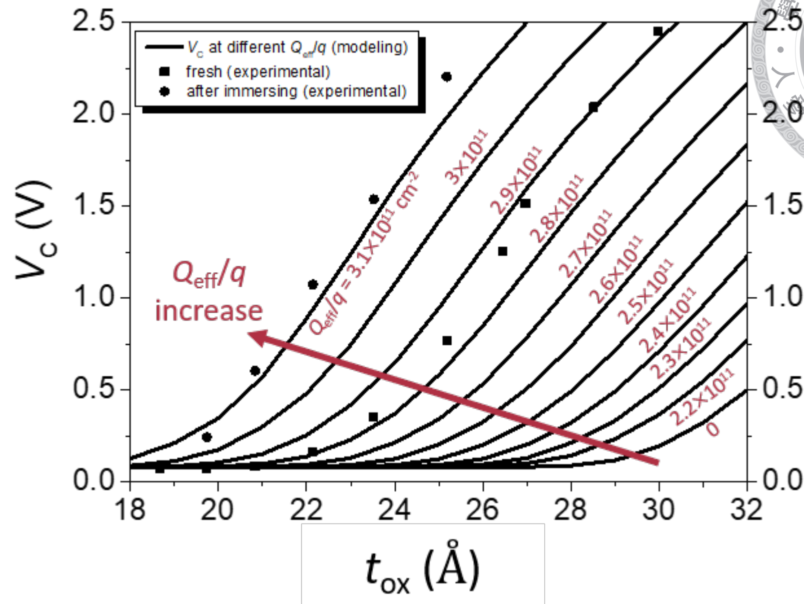

Figure 3–9. The $V_C - t_{ox}$ relation extracted from experimental and modeling at different Q_{eff}/q. The extracted V_C before and after immersing are plotted in square and circle symbols. The modeling results are plotted in solid lines.

3.4.3 Extraction of Lateral Decay Length's Activation Energy

In this section, the photon current behavior of a device on another wafer is measured under different temperatures, which can reflect the activation energy of lateral decay length Λ. To avoid the confusion of injection hole current caused by the SBHM effect, a MISTD with a relatively thin oxide layer of 22.8 Å is selected. For the thin device, the SBHM effect is negligible, and the current is dominated by electron current [40]. The mechanism to extract the activation energy of Λ is shown in **Figure 3–10** . **Figure 3–10** (b) plots the band diagram of cut line $\overline{AB}$ in **Figure 3–10** (a). The photon-induced electron will laterally diffuse under the electrode because of the gradient of the electron quasi-Fermi level. If the light intensity is very weak and does not strongly affect the profile we discussed under dark in **Section 3.2.3**, the photon current can reflect the area of Λ^2. However, the

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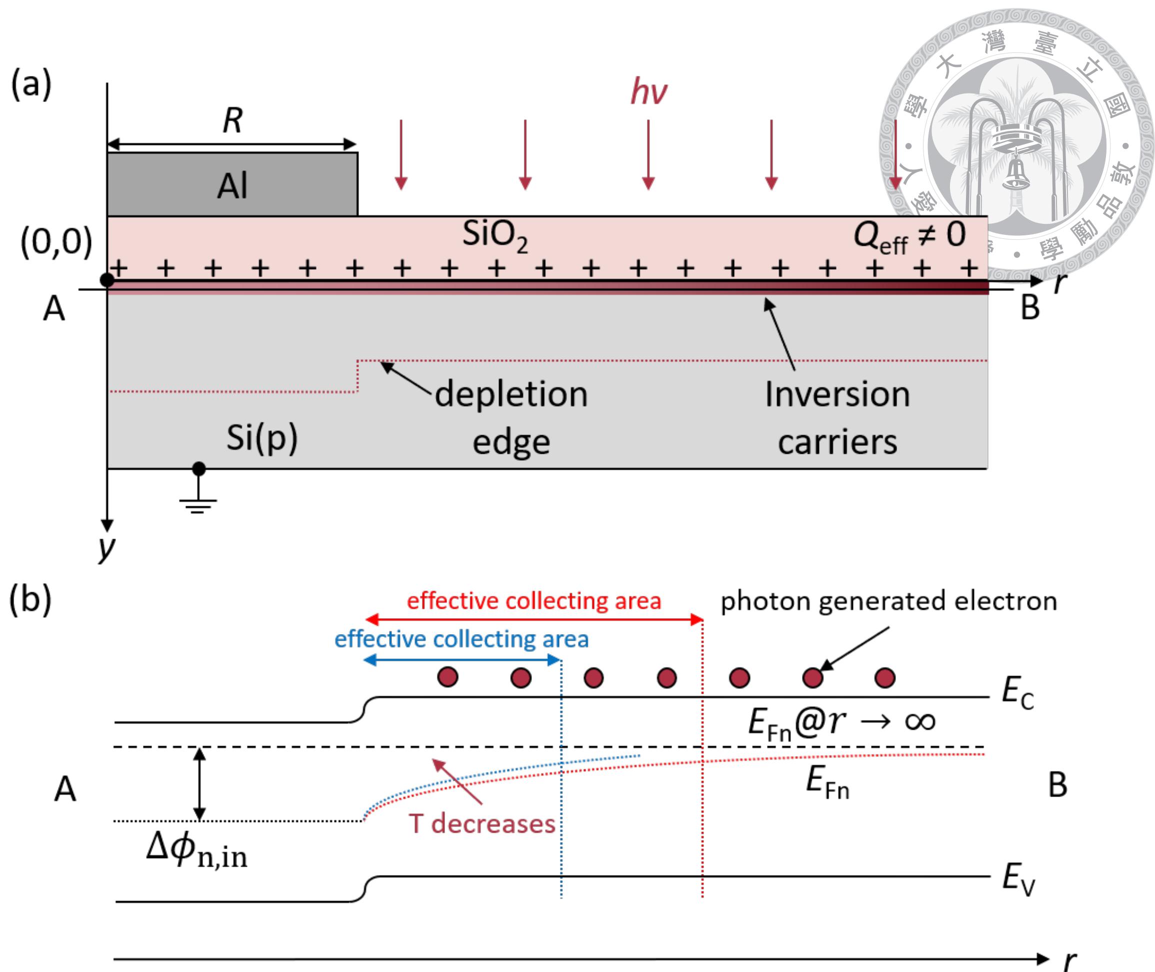

Figure 3–10. (a) Schematic of MISTD under illumination. (b) Band diagram of cut line $\overline{AB}$ in (a). Profiles of quasi-Fermi level differences at different temperatures are shown.

electron current is dominated by the generated electrons at room temperature under weak light. Thus, we measure the MISTD's current under low temperatures to eliminate the thermal generation current. The measured currents at $V_G = 2.5$ V under different temperatures T are shown in **Figure 3–11** by square symbols. The measuring temperatures are 230, 240, 250, 260, 270, 280, 290, 300, 315, 330, and 345 K. The measurement is taken in a chamber with a weak leakage light from the environment. Electron currents calculated under different T are also attached. Modeling current with $Q_{eff}/q = 2.4 \times 10^{11}$ and 2.5×10^{11} cm^{-2} are plotted as the red and blue lines, respectively. When modeling under

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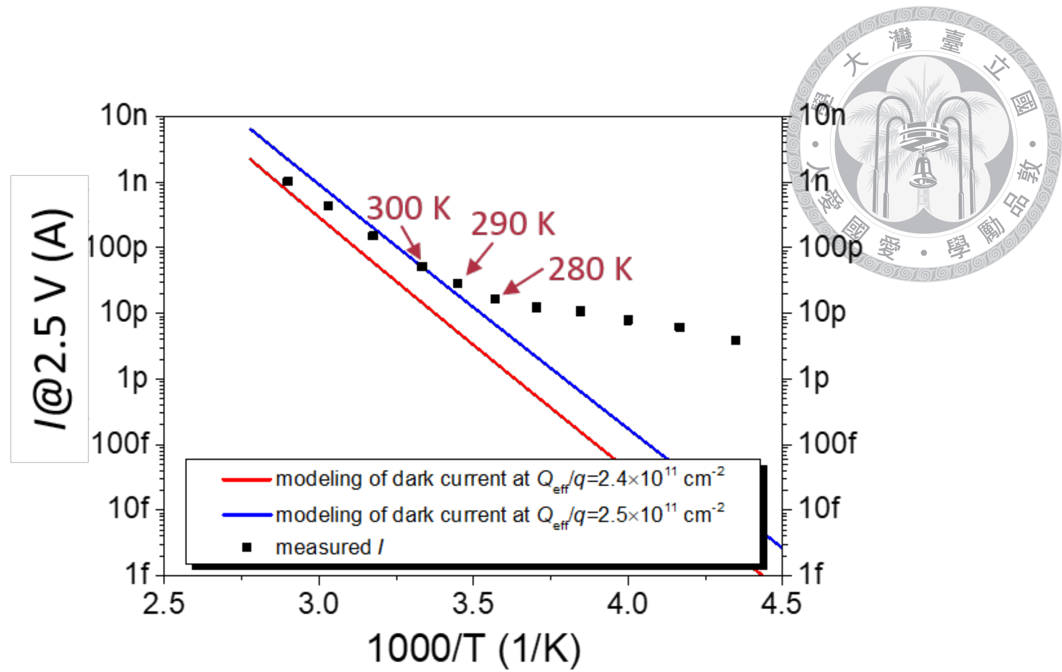

Figure 3–11. Measured currents at V_G = 2.5 V under different temperatures T.

different temperatures, the temperature dependency of mobility [61], carrier lifetime [61], and band gap [62] are considered. The calculated dark currents have a tendency similar to the measurement above 290 K. However, the photon current dominates under temperatures lower than around 280 K. The measured current at V_G = 2.5 V and calculated Λ^2 are shown in **Figure 3–12**. Both of them are normalized to 280 K. The Arrhenius plot in **Figure 3–12** shows an activation energy E_a around 0.15 eV for both the device's current and Λ^2. The result gives a strong evidence on the existence of lateral decay length Λ.

3.4.4 Comparison with TCAD Simulation

We extract some parameters, which are difficult to extract by experimental, from the TCAD simulation and compare them with the modeling in this section. The simulation uses the device structure and coordinates the same as the schematic shown in **Figure 3–2** (a). **Figure 3–13** (a) and (b) show the quasi-Fermi level difference $\Delta\phi_n(r)$ from modeling and

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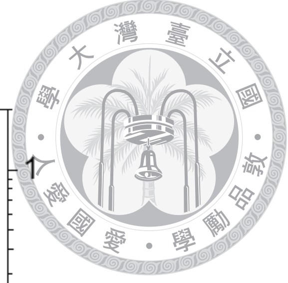

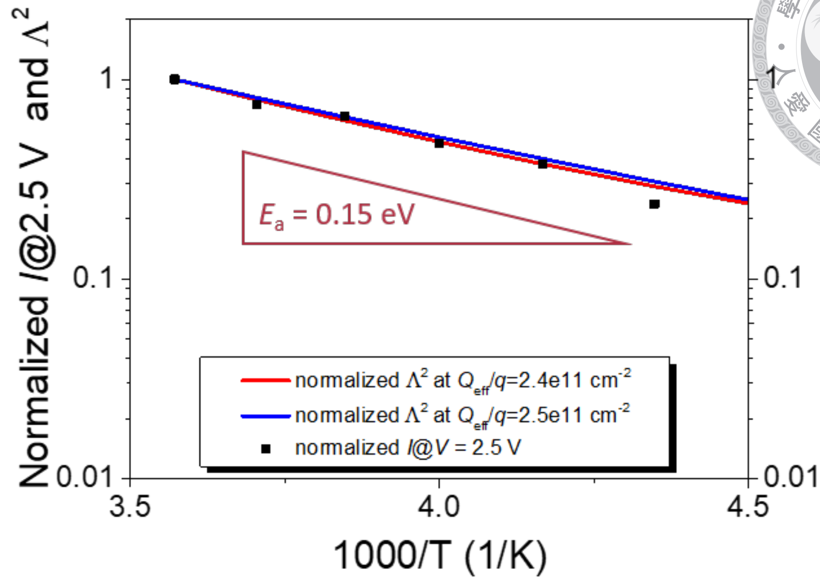

Figure 3–12. Measured current at V_G = 2.5 V and calculated Λ^2. Both of them are normalized to 280 K.

simulation, respectively. The $\Delta\phi_n(r)$ from the simulation is extracted by the difference of electron quasi-Fermi level at the silicon surface and bulk region. **Figure 3–14** plots the corresponding surface electron concentration n_s of **Figure 3–13**. The device considered in **Figure 3–13** and **Figure 3–14** has t_{ox} = 25 Å and Q_{eff}/q = 2.8 × 10^{11} cm^{-2}. From **Figure 3–13** and **Figure 3–14**, one can observe flat $\Delta\phi_n(r)$ and n_s at $V_G < V_c$. In this situation, the lateral electron supply will increase with increasing $\Delta\phi_{n,in}$ because the lateral supplement is still unsaturated. However, step profiles of $\Delta\phi_n(r)$ and n_s near the device's edge at $V_G > V_c$ are observed. The situation is similar to the "pinch-off" effect in MOSFET, but the electron flow is driven by the concentration gradient. When the "pinch-off" effect occurs, the electron supplement saturates, leading to the deep depletion effect observed at $V_G > V_c$. The modeling has a similar tendency to the simulation. However, a deviation of around 0.3 V is observed in **Figure 3–13** and **Figure 3–14**.

We further extract the V_C for different t_{ox} and Q_{eff}/q from modeling and simulation.

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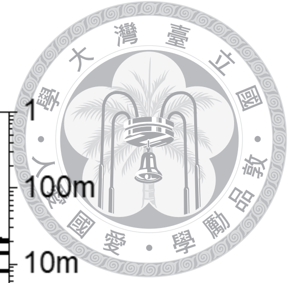

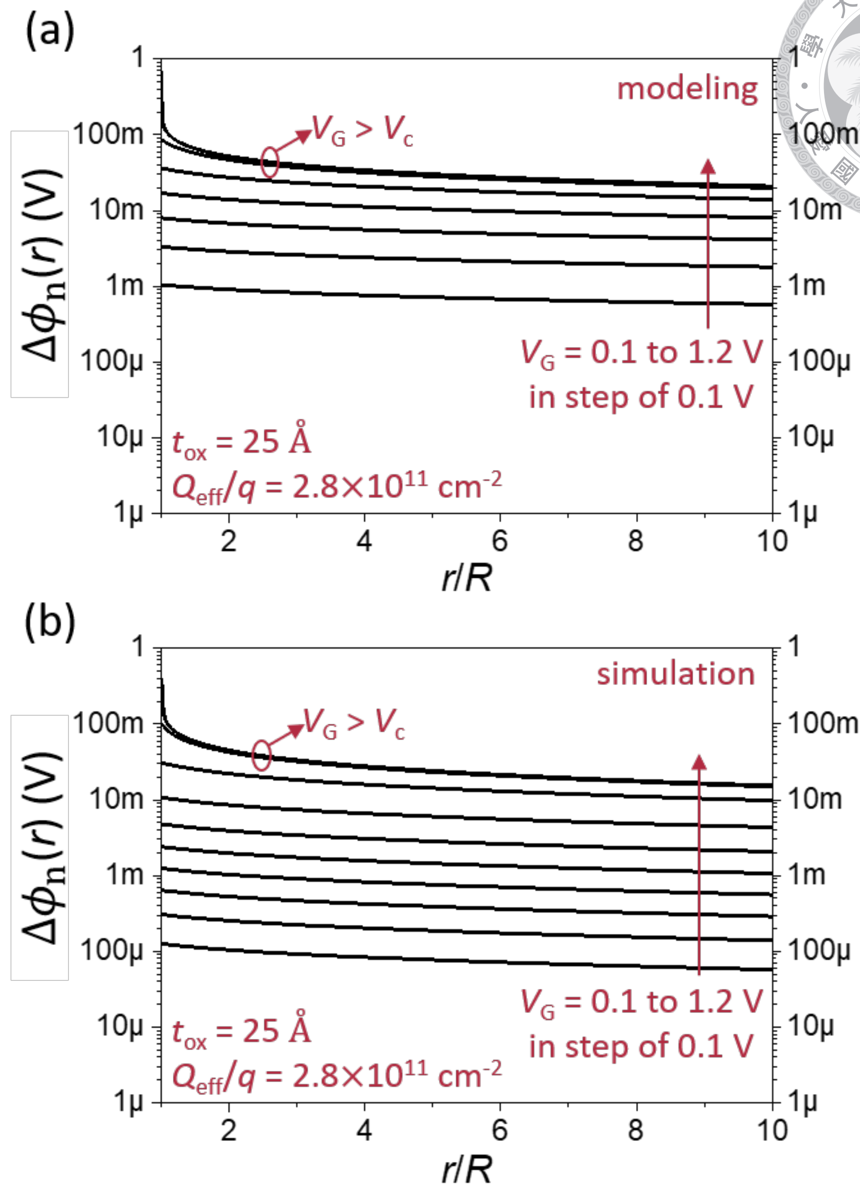

Figure 3–13. Quasi-Fermi level difference from (a) modeling and (b) simulation. A MISTD with t_{ox} = 25 Å and $Q_{eff}/q = 2.8 \times 10^{11}$ cm^{-2} is considered.

The modeling and simulation results are shown in **Figure 3–15** (a) and (b), respectively. t_{ox} ranging from 22 to 32 Å and Q_{eff}/q ranging from 2.2 to 2.8×10^{11} cm^{-2} are considered. A deviation of around 0.2-0.3 V between the modeling and simulation is observed in the V_C mapping. We suggest that the deviation mainly stems from:

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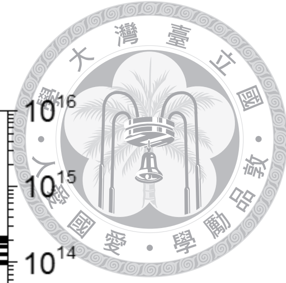

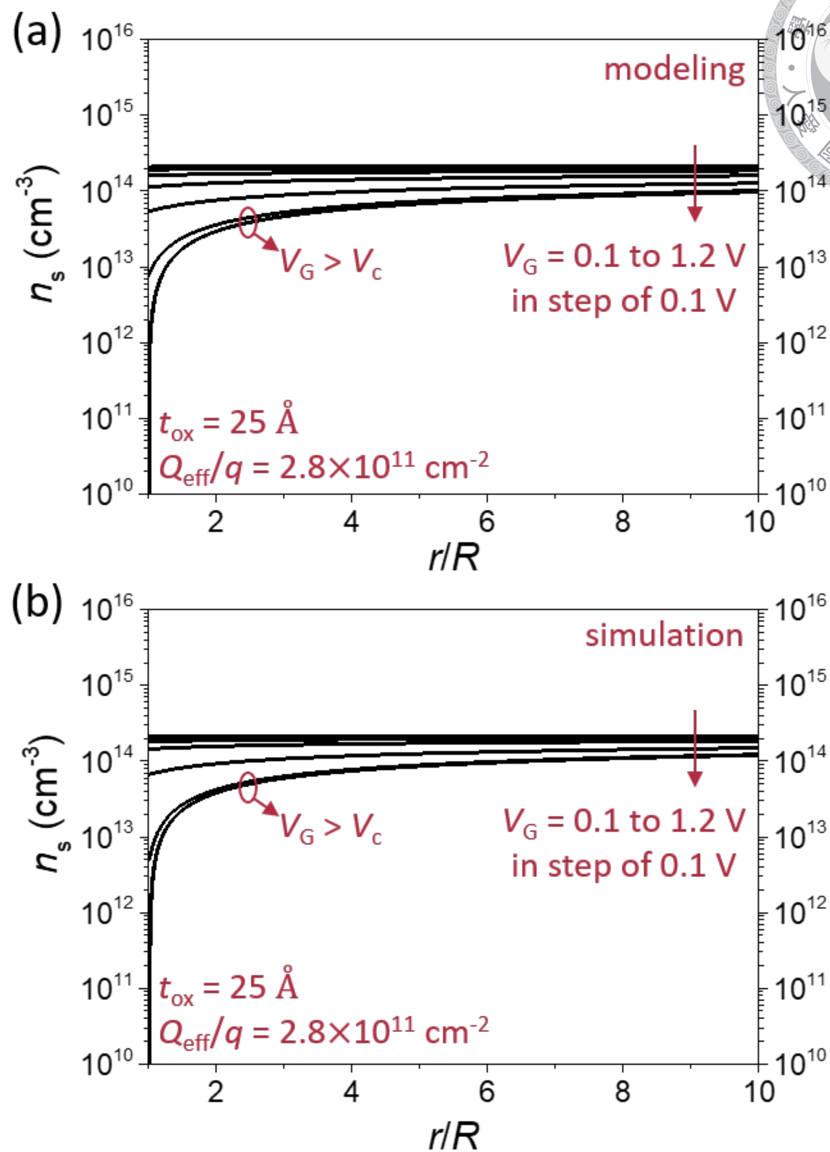

Figure 3–14. Surface electron concentration n_s from (a) modeling and (b) simulation. The device's conditions are the same as **Figure 3–13**.

- A more complex field-dependent electron mobility is considered in TCAD simulation, which will affect Λ as calculated in (3.18).
- Quantum confinement is considered in TCAD simulation, which will lead to a lower surface electron concentration and a thicker effective tunneling thickness.

Though the deviation exists, the modeling and simulation both indicate that not only the

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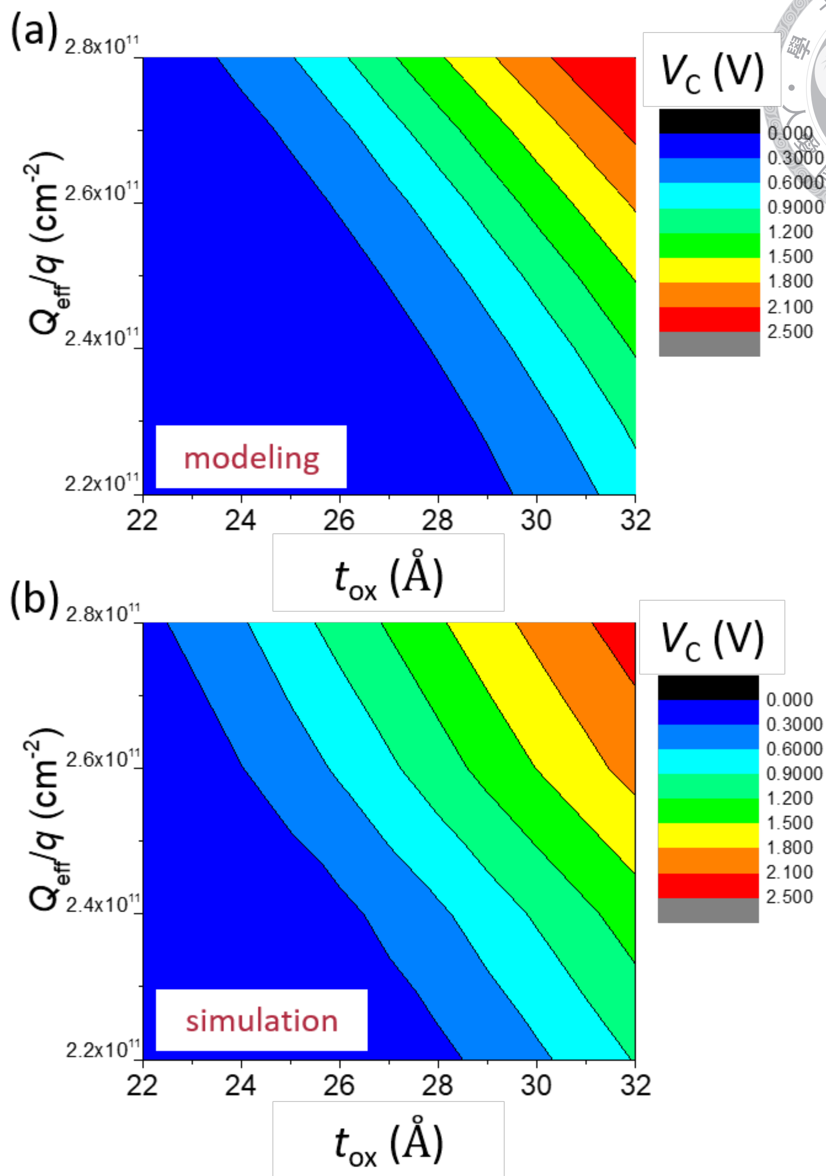

Figure 3–15. V_C mapping from (a) modeling and (b) TCAD simulation. t_{ox} ranging from 22 to 32 Å and Q_{eff}/q ranging from 2.2 to 2.8×10^{11} cm^{-2} are considered.

oxide thickness but also the oxide charges will strongly affect the electrostatic characteristic of MISTD.

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3.5 Summary

In this chapter, a detailed model is proposed to calculate the impact of outer oxide charges on the electrostatic characteristic of MISTD. By finely tuning the number of oxide charges, the model can predict the critical voltage of MISTDs. In the modeling, a concept of lateral decay length Λ is proposed. Λ can extend for hundreds or thousands of micro-meter and strongly affect the behavior of MISTD if the amount of oxide charges is high enough to induce inversion at the silicon surface. The activation energy of Λ is also extracted by measuring photocurrent under low temperatures. The extracted result fits well with our modeling. Finally, we compare the model with the TCAD simulation. The model can describe the tendency of quasi-Fermi level and electron concentration profiles similar to the TCAD simulation.

Except for the HFCV (electrostatic) characteristic, the IV behavior of MISTD is also of interest. As discussed in **Section 2.3.2** and **Section 2.3.3**, the HFCV and IV of MISTD are strongly related. In the next chapter, we will derive the IV characteristic of MISTD based on the model discussed in this chapter.

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4

Modeling II: Impact of Oxide Charge on the Current-Voltage Characteristic of MISTD

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4.1 Objective

As discussed in **Section 2.3.2** and **Section 2.3.3**, IV is strongly related to HFCV for MISTD, and the hole injection current depends on V_{ox} [24, 40]. From the model discussed in **Chapter 3**, one can derive V_{ox} in the whole reverse bias region with known t_{ox}, Q_{eff}/q, and R. With the relation of $V_{\text{ox}} - V$, one can clearly define the level of SBHM effect at each bias voltage to calculate hole current. However, we have pointed out some problems with the simplified hole injection current equation proposed by [24] and shown in (2.2), in **Section 2.3.2**. Thus, we derive a more detailed hole injection current equation in this chapter. We then combine the improved hole injection current equation with $V_{\text{ox}} - V$ relation, derived by the model in **Chapter 3**, to calculate the IV characteristic of MISTD.

4.2 Model Derivation

4.2.1 SBHM and Hole Injection Current Equation

An ideal band diagram of MISTD is shown in **Figure 4−1** to assist the derivation of hole injection current. We define the hole Schottky barrier height $q\phi_{\text{b}}$ as the energy difference between E_{Fm} and E_{V} at silicon's surface. With considering (2.1) and **Figure 4−1**, one can calculate the hole Schottky barrier height as

$$\begin{aligned} q\phi_{\text{b}} &= q(\phi_{\text{b0}} - V_{\text{ox}}) \\ &= 1.1 - qV_{\text{ox}} \text{ eV}, \end{aligned} \tag{4.1}$$

where the initial hole barrier high $q\phi_{\text{b0}}$ is roughly equal to silicon's band-gap because the aluminum's Fermi level nearly aligns to the conduction band of silicon at zero oxide voltage. When the barrier high $q\phi_{\text{b}}$ is known, one can calculate the hole current I_{h} by an

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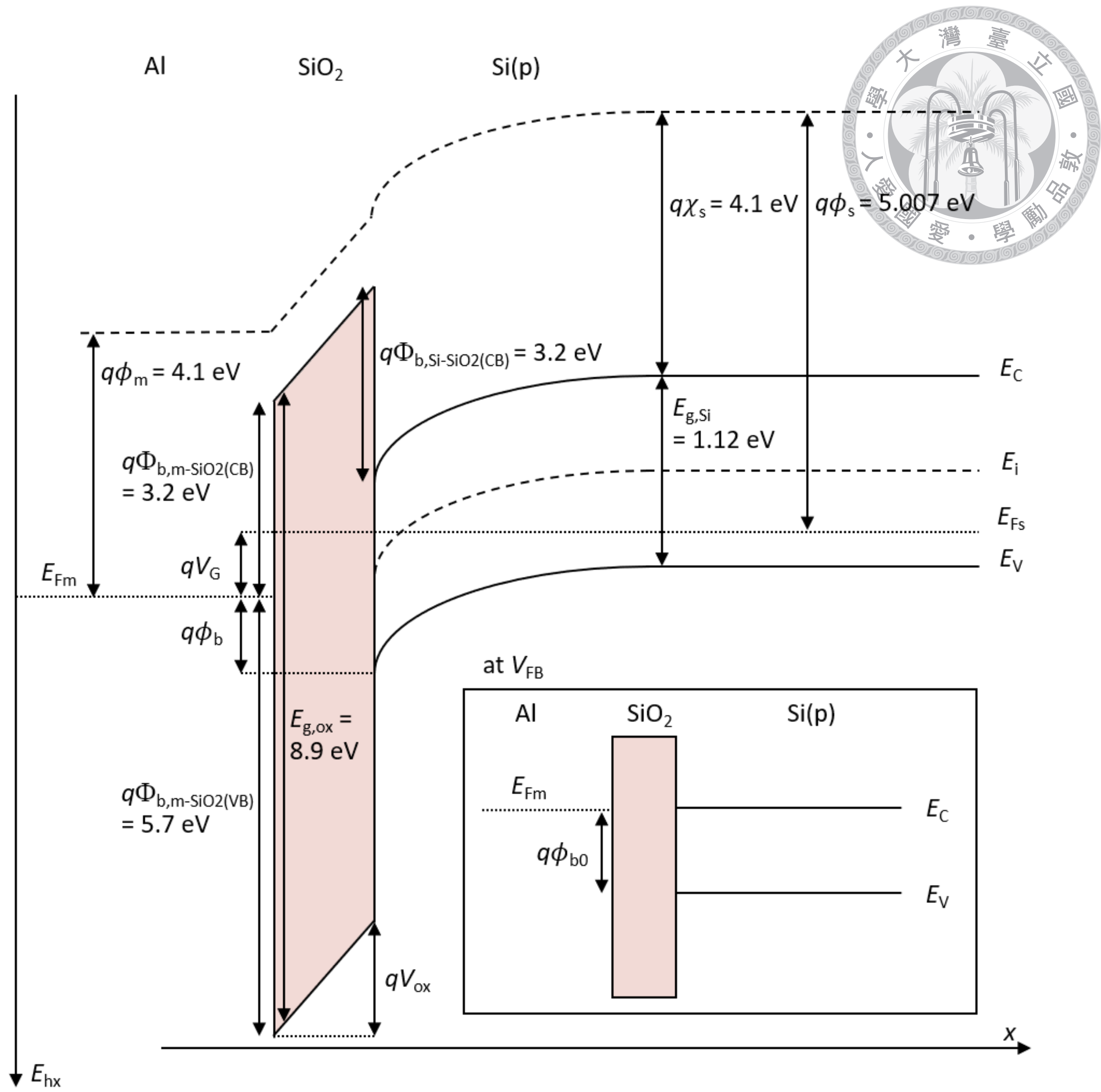

Figure 4–1. An ideal band diagram of MISTD under positive bias, where the barriers between metal and conduction/valance band of silicon dioxide are labeled as $q\Phi_{\text{b,m-SiO2(CB)}}/q\Phi_{\text{b,m-SiO2(VB)}}$. The band diagram at V_{FB} and magnitude of $q\phi_{\text{b0}}$ are also attached.

improved hole current equation, which is finely derived in **Appendix B**. The hole current equation is expressed as

$$I_{\text{h}} = \frac{4\pi qkTAm}{h^3} \int_{q\phi_{\text{b}}}^{+\infty} P_{\text{th}}(E')\ln(1 + e^{-E'/kT})dE', \tag{4.2}$$

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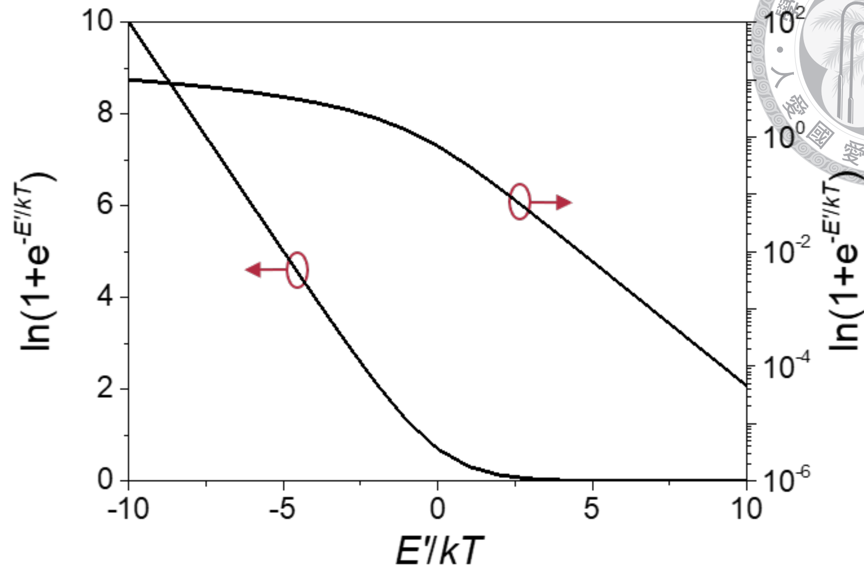

Figure 4–2. $\ln(1 + e^{-E'/kT})$ v.s. E'/kT

where m is the hole effective mass in aluminum (we abruptly assume m equals to free electron mass in our model), h is the Planck constant, $P_{\mathrm{th}}(E')$ is the hole tunneling probability at energy level E', $E' = E_{\mathrm{hx}} - E_{\mathrm{Fm}}$ is the hole energy in x direction (E_{hx}) reference to metal's Fermi energy (E_{Fm}). To be mentioned that the hole's energy E' increases with toward the axis in the band diagram as labeled in **Figure 4–1** . The term $\ln(1 + e^{-E'/kT})$ in (4.2) reflects the multiplication of available holes and their injection velocity at energy level E'. **Figure 4–2** shows $\ln(1 + e^{-E'/kT})$ v.s. E'/kT. As shown in **Figure 4–2** , when $q\phi_{\mathrm{b}}$ in (4.2) is larger than about $3kT/q$, the term $\ln(1+e^{-E'/kT})$ closes to $e^{-E'/kT}$, and the calculated result approaches to the traditional Schottky diode current equation. However, a negative Schottky barrier appears when V_{ox} in (4.1) is higher than 1.1 V. The schematic of the negative Schottky barrier is plotted in **Figure B–1** (b). In this situation, the term $\ln(1 + e^{-E'/kT})$ becomes $\approx -E'/kT$, and linearly increases with decreasing of E'. The increase in injected holes will lead to a significant increase in hole current.

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From **Figure 4−1** , the hole's tunneling barrier $q\Phi_b(E')$ at energy level E' is

$$\begin{aligned} q\Phi_b(E') &= q\Phi_{b,\text{m-SiO2(VB)}} - E' \\ &= 5.7 - E' \text{ eV}, \end{aligned} \tag{4.3}$$

where $q\Phi_{b,\text{m-SiO2(VB)}}$, labelled in **Figure 4−1** , is the oxide layer's tunneling barrier seen by hole at metal's Fermi level. The hole tunneling probability $P_{th}(E')$ in (4.2) is calculated by WKB approximation with trapezoidal shape barrier

$$P_{th}(E') = \exp\left(- \frac{4\sqrt{2m_{ox,h}}(q\Phi_b)^{3/2}[1 - (1 - V_{ox}/\Phi_b)^{3/2}]}{3\hbar q \varepsilon_{ox}} \right), \tag{4.4}$$

where $m_{ox,h}$ is the hole effective mass in silicon dioxide. Unlike the electron effective mass in oxide, many works get different oxide's hole effective mass ranging from 0.23 to $0.58m_0$ [51, 63–66]. In this work, a relative light $m_{ox,h}$ of $0.23m_0$ is selected [63]. This effective mass is extracted by measuring the Fowler-Nordheim tunneling current of oxide layers on 6H-SiC. The electron and hole components of the Fowler-Nordheim tunneling current is studied by different doping layers in the substrate. [63]

4.2.2 Procedure of Modeling

From the model discussed in **Section 4.2.1**, one can calculate the hole injection current with known V_{ox}. With the V_{ox} calculated in **Chapter 3**, the total current I_{total} of a MISTD can be derived with suitable process flow. The detailed process flow is plotted in **Figure 4−3** . **Figure 4−3** shows that the IV characteristic of a MISTD can be determined when the physical conditions R, A, t_{ox}, Q_{eff}, and V_G are known. The equations used to calculate the terms in **Figure 4−3** are also listed in **TABLE 5−I** .

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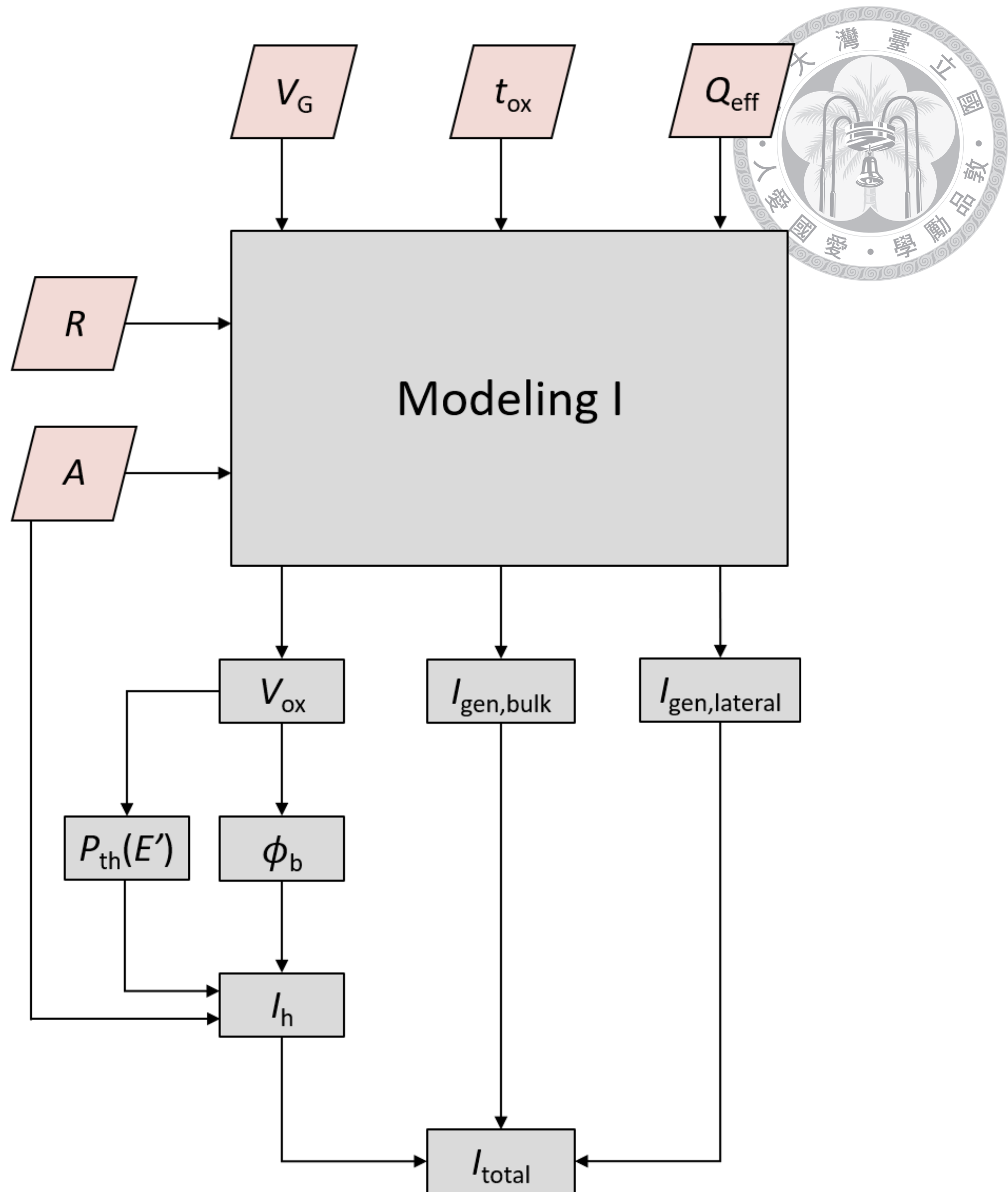

Figure 4–3. The detailed process flow to calculate the total current I_{total} of a MISTD.

TABLE 4–I

The corresponding equations to calculate terms in **Figure 4–3**.

Term	Description	Unit	Equation
ϕ_b	hole Schottky barrier height	V	(4.1)
P_{th}	hole's tunneling probability		(4.4)
I_h	hole injection current	A	(4.2)

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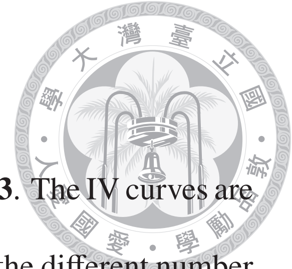

4.3 Experimental Detail

In this chapter, we measure IV of the 11 devices measured in **Chapter 3**. The IV curves are measured before and after immersing in D.I. water to get the result of the different number of oxide charges. The current characteristic of another device on another wafer with an oxide thickness of 26.5 Å is measured under different temperatures to find the evidence of hole injection current. This thickness is thick enough to partially hold the inversion layer and exhibit the phenomenon of SBHM.

4.4 Result and Discussion

The increasing reverse bias current with oxide thickness is discussed in **Section 2.3.2** and **Section 2.3.3**. Here, we will quantitatively discuss how the SBHM effect and hole injection current cause the phenomenon based on the model suggested in **Section 4.2**. The comparison with experimental results further confirms the importance of the hole injection current.

4.4.1 Role of Hole Injection Current on MISTD

Figure 4−4 (a) shows the calculated V_{ox} at $V_G = 2.5$ V from **Chapter 3**. As plotted in **Figure 3−15** , MISTDs with thicker oxide thickness and higher Q_{eff}/q have higher V_C. Higher V_C indicates that the device can hold higher V_{ox}. **Figure 4−4** (b) is the hole Schottky barrier height $q\phi_b$ at $V_G = 2.5$ V calculated from (4.1). Higher V_{ox} can modulate $q\phi_b$ to a lower value. Negative $q\phi_b$s are observed for devices with enough oxide thickness and oxide charges. With known V_{ox} and $q\phi_b$, one can calculate the hole injection current I_h from (4.2). The calculated I_h at $V_G = 2.5$ V for $Q_{eff}/q = 2.9 \times 10^{11}$ cm^{-2} is plotted in

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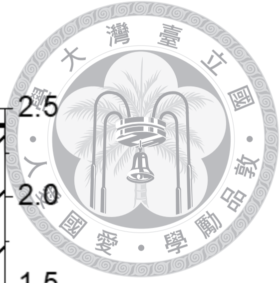

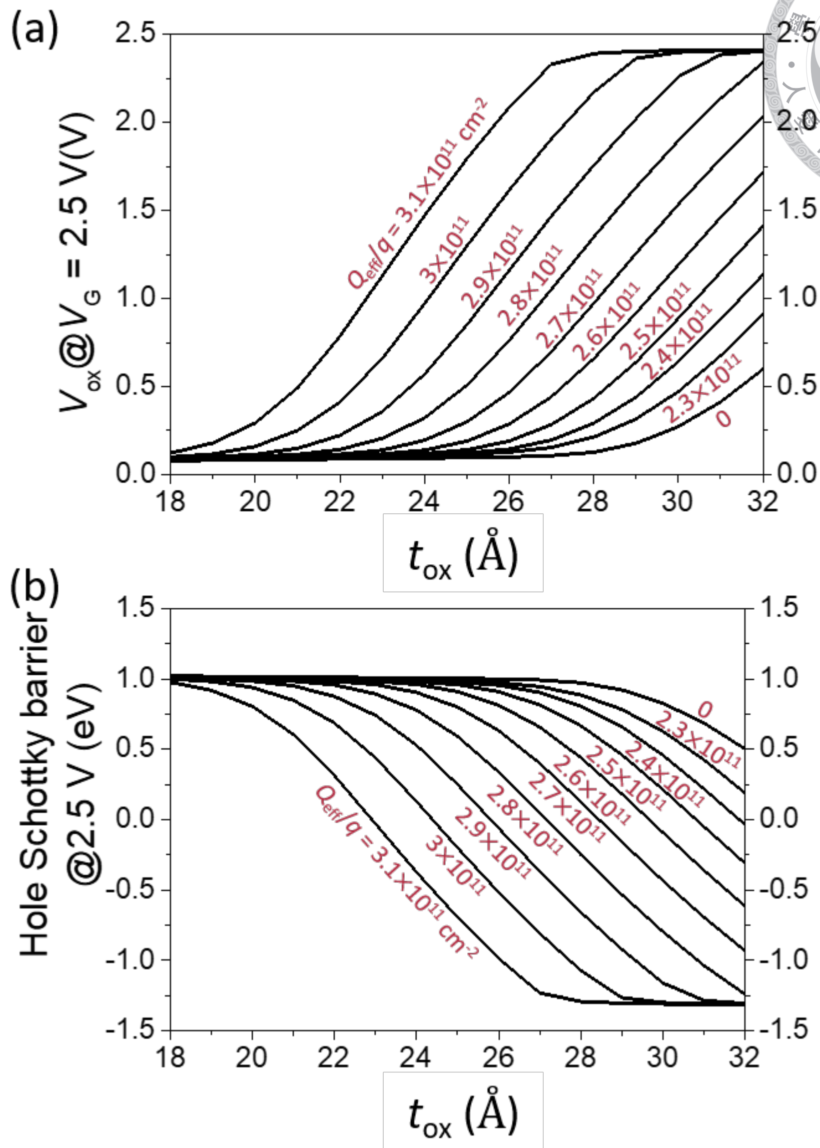

Figure 4‒4. (a) The calculated V_{ox} at V_G = 2.5 V from **Chapter 3**. (b) The calculated $q\phi_b$ from (a).

Figure 4‒5 as the blue line. Except for I_h, we also define the electron current I_e as

$$I_e = I_{gen,bulk} + I_{gen,lateral}, \tag{4.5}$$

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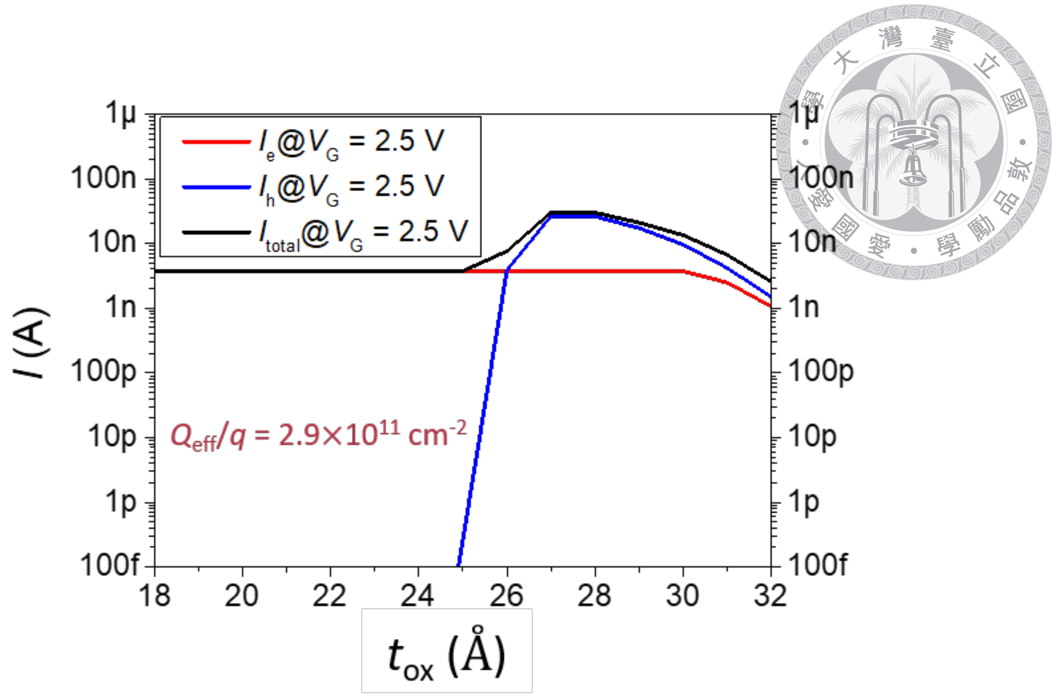

Figure 4–5. Calculated I_e, I_h, and I_{total} versus oxide thickness. The MISTD with $Q_{eff}/q = 2.9 \times 10^{11}$ cm^{-2} and biased at $V_G = 2.5$ V is considered.

where $I_{gen,bulk}$ and $I_{gen,lateral}$ are the thermal generated electron current under and outside the electrode, defined in **Chapter 3**. The total current I_{total} is also defined as

$$I_{total} = I_e + I_h. \tag{4.6}$$

I_e and I_{total} at $V_G = 2.5$ V are also plotted in **Figure 4–5** as the red and black lines, respectively. There are significantly two different regions in **Figure 4–5**. When t_{ox} is thinner than around 25 Å, the device's current is dominated by an almost constant electron current. Compared with **Figure 4–4** (b), a positive $q\phi_b$ is observed for $Q_{eff}/q = 2.9 \times 10^{11}$ cm^{-2} at $t_{ox} < 25$ Å. In this situation, the hole barrier blocks the hole current, and the devices are dominated by electron current. The region of almost constant electron current is related to the slight depletion width variation for devices with different oxide

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thicknesses. As shown in **Figure 4−4** (b), for devices with $Q_{\text{eff}}/q = 2.9 \times 10^{11}$ cm^{-2}, $q\phi_{\text{b}}$ becomes negative when $t_{\text{ox}} > 25$ Å. The appearance of negative $q\phi_{\text{b}}$ leads to a quick increase of I_{h}, as shown in **Figure 4−5** . I_{h} plays an important role at $t_{\text{ox}} > 25$ Å. One can observe that I_{total} increases with t_{ox} in a specific oxide thickness range in **Figure 4−5** . The calculated results imply that the SBHM effect and hole injection current is non-negligible and may cause the unusual $I_{\text{total}} - t_{\text{ox}}$ relation under specific conditions.

4.4.2 Comparison with Experimental

Figure 4−6 (a) and (b) show the measured IV curves before and after immersing in D.I. water. In **Figure 4−6** , zero current is observed at positive bias voltage but not $V_{\text{G}} = 0$ V. The phenomenon is caused by the existence of displacement current†. **Figure 4−6** shows a significantly higher reverse bias current after immersion because of the increase of oxide charges. However, the current in the accumulation region is almost unchanged. To look

†Displacement current is observed when sweeping on electron devices. The displacement current is related to the capacitance value of the device and the sweeping rate. The displacement current I_{dis} can be expressed as

$$I_{\text{dis}}(V_{\text{G}}) = \alpha C_{\text{G}}(V_{\text{G}}), \tag{4.7}$$

where $\alpha = dV_{\text{G}}/dt$ is the sweeping rate, and $C_{\text{G}}(V_{\text{G}})$ is the capacitance value at V_{G}. With considering the displacement current, the measured current under sweeping $I_{\text{G,sweep}}$ can be written down as

$$I_{\text{G,sweep}}(V_{\text{G}}) = I_{\text{G,steady}}(V_{\text{G}}) + I_{\text{dis}} = I_{\text{G,steady}}(V_{\text{G}}) + \alpha C_{\text{G}}(V_{\text{G}}), \tag{4.8}$$

where $I_{\text{G,steady}}(V_{\text{G}})$ is the steady current at V_{G}. For **Figure 4−6** , sweeping V_{G} from 2.5 to -2 V, the sweeping condition leads to negative α and I_{dis}; thus, zero currents are observed at positive V_{G} when $I_{\text{G,steady}}(V_{\text{G}}) + \alpha C_{\text{G}}(V_{\text{G}}) = 0$.

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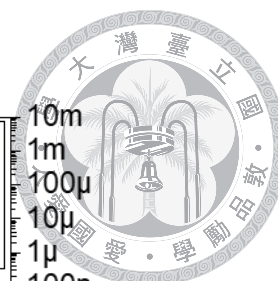

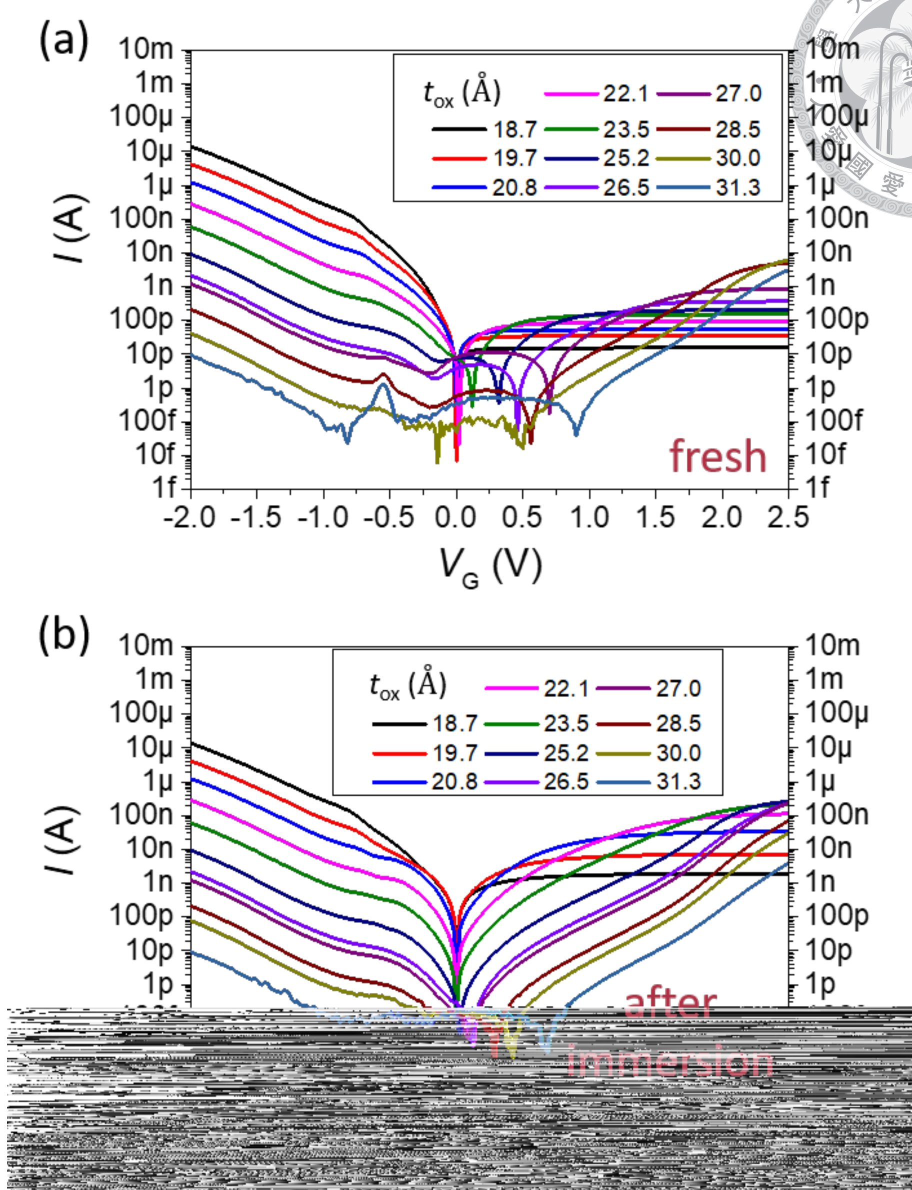

Figure 4–6. IV curves of the 11 devices (a) before and (b) after immersing in D.I. water. The IV curves are swept from 2.5 to -2 V.

insight how the oxide charges affect the current behavior, IV curves with t_{ox} = 27 Å are extracted to compare with modeling as shown in **Figure 4–7**. Measured IV curves are plotted in **Figure 4–7** (a). The averages of the measured currents in opposite sweeping directions are adopted to avoid confusion from the displacement currents. The fresh and after-immersed IV curves are shown as black and red lines, respectively. The black

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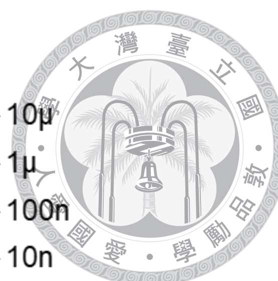

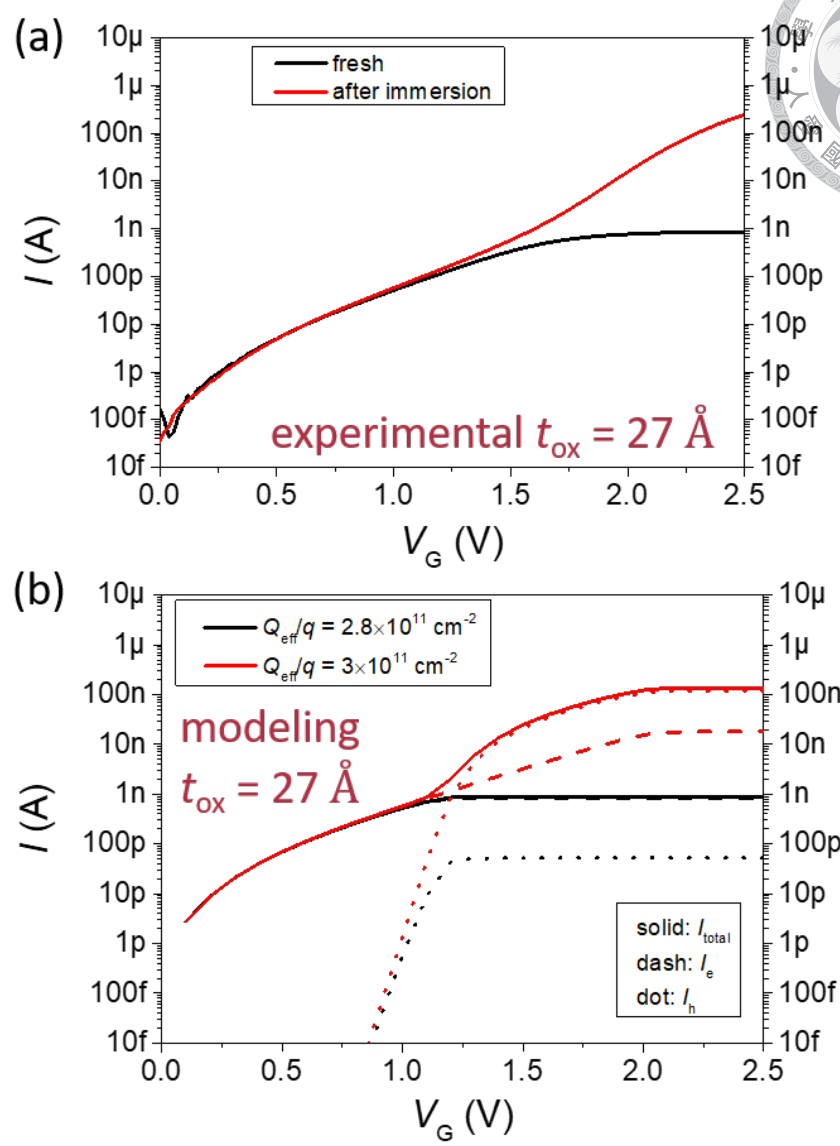

Figure 4–7. (a) Measured IV curves before and after immersing in D.I. water. (b) Calculated IV curves with $Q_{\mathrm{eff}}/q = 2.8$ and 3×10^{11} cm^{-2}. The total current, electron current, and hole current are plotted in solid, dash, and dot lines, respectively.

and red lines almost overlap with each other under low bias voltages. At low bias voltage, the MISTD works like a MOS capacitor. The V_{ox}, inversion layer, tunneling probability, and SBHM are similar for sample measured before and after immersions. However, a sudden increase in current is observed at a certain bias voltage for the red line in **Figure 4–7** (a). The modeling results with $Q_{\mathrm{eff}}/q = 2.8$ and 3×10^{11} cm^{-2} are shown

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in **Figure 4−7** (b) by black and red lines to simulate the dramatic increase at high bias voltage. In **Figure 4−7** (b), the total current, electron current, and hole current are plotted in solid, dash, and dot lines, respectively. The overlapping of I_{total} is also observed at low bias voltage. However, the current of the device with $Q_{\mathrm{eff}}/q = 3 \times 10^{11}$ cm^{-2} becomes significantly higher at $V_{\mathrm{G}} > 1$ V. From **Figure 4−7** (b), one can find that I_{e} and I_{h} both become higher for the device with more oxide charges. More oxide charges lead to a longer Λ and more lateral electron supplement. Thus, the device can hold a higher V_{ox}. The rising of V_{ox} can increase I_{e} for the following two reasons:

- Linearly increase of inversion layer.
- Exponentially increase of tunneling probability.

However, increasing V_{ox} can also enhance I_{h} for the following two reasons:

- Exponentially increase of holes with energy higher than the hole's Schottky barrier height because of SBHM effect.
- Exponentially increase of tunneling probability.

When compared to I_{e}, I_{h} has a much faster increase rate with V_{ox}. It is the significant increase of I_{h} leading to a much higher current for devices with more oxide charges. This significant increase is observed in both the experimental and modeling.

The measured currents at 2.5 V from **Figure 4−6** (a) and (b) are shown in **Figure 4−8** as square and circle symbols, respectively. The calculated results of different Q_{eff}/q are also attached. From **Figure 4−8** , two following phenomena are observed:

- For thick devices (e.g. $t_{\mathrm{ox}} \gtrsim 26$ Å), the increase of reverse bias current with oxide thickness is governed by the SBHM effect and dominated by hole current. For thin

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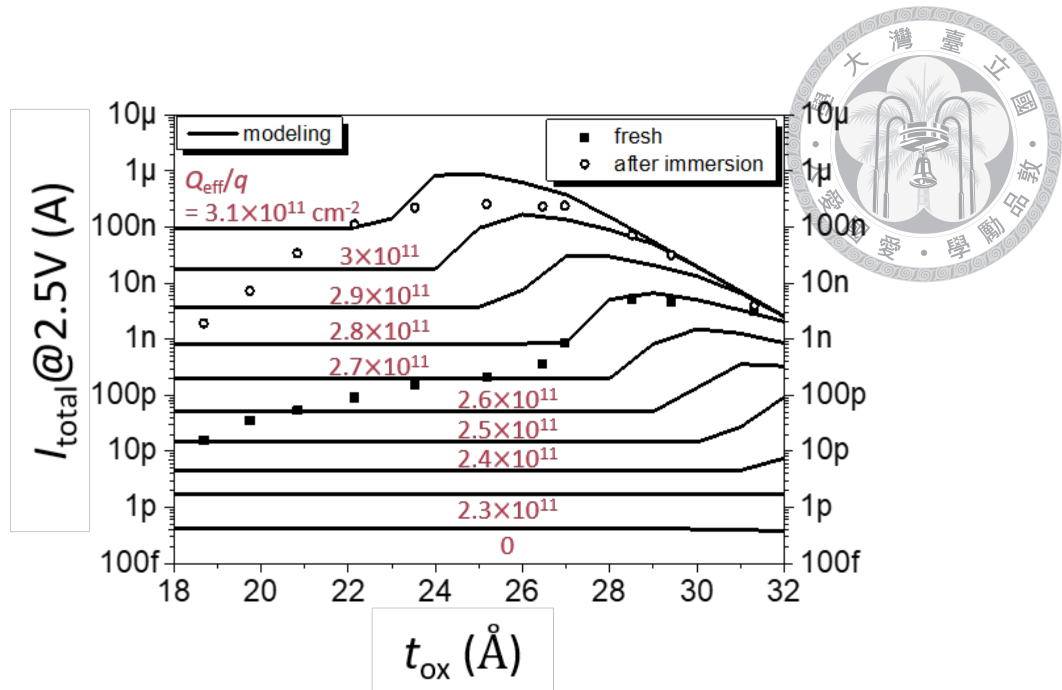

Figure 4–8. Measured current at 2.5 V from **Figure 4–6** (a) and (b) are plotted as square and circle symbols, respectively. Modeling currents for different Q_{eff}/q at 2.5 V are also attached.

devices (e.g. $t_{\mathrm{ox}} \lesssim 26$ Å), it was observed that the reverse bias current increase with oxide thicknesses due to increased oxide charges.

- For thick devices ($t_{\mathrm{ox}} \gtrsim 26$ Å), the Q_{eff}/q roughly increases from 2.8×10^{11} cm^{-2} to 3.05×10^{11} cm^{-2} after immersion. However, more oxide charges increase is observed for thinner devices. For example, an increase of around 4×10^{10} cm^{-2} is observed for the device with $t_{\mathrm{ox}} = 23.5$ Å.

The hole Schottky barrier heights of the experimental devices are also estimated by utilizing the V_{C}s shown in **Figure 3–9** , which are extracted from HFCV. It is defined that

$$\begin{cases} V_{\mathrm{ox}} = V_{\mathrm{G}} - V_{\mathrm{FB}} - \psi_{\mathrm{s,sat}}, V_{\mathrm{G}} < V_{\mathrm{C}}; \\ V_{\mathrm{ox}} = V_{\mathrm{C}} - V_{\mathrm{FB}} - \psi_{\mathrm{s,sat}}, V_{\mathrm{G}} \geq V_{\mathrm{C}}, \end{cases} \tag{4.9}$$

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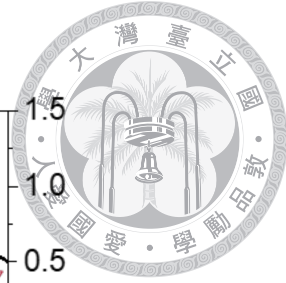

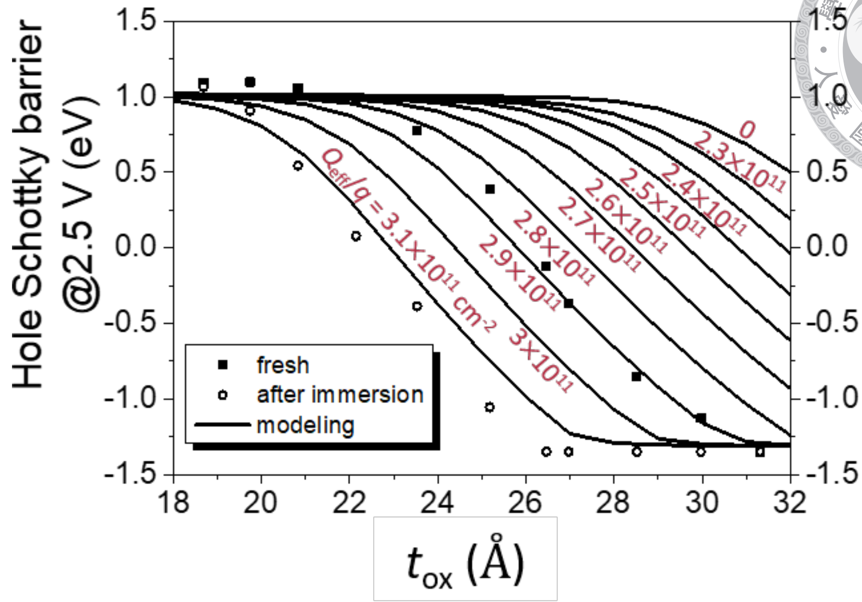

Figure 4–9. Extracted hole Schottky barrier height at 2.5 V before and after immersing are plotted as square and circle symbols, respectively. Modeling results from **Figure 4–4** (b) are also attached.

where $\psi_{s,sat}$ is the saturated surface band bending before deep depletion. An empirical value of $\psi_{s,sat} \approx 0.95$ V is adopted. The calculated V_{ox} is inserted to (4.1) to calculate the hole Schottky barrier height. The calculated results before and after immersion are shown in **Figure 4–9** as square and circle symbols, respectively. The modeling results from **Figure 4–4** (b) are also attached for comparison. A significant decrease in the hole Schottky barrier is observed for the device after immersion. Increasing of Q_{eff}/q within the range of 2.9 to 3.1×10^{11} cm^{-2} is also observed. The variance of Q_{eff}/q is close to the observation in **Figure 4–8** . The above comparisons show that the outer oxide charges strongly affect the electrostatic and current behavior of the MISTDs.

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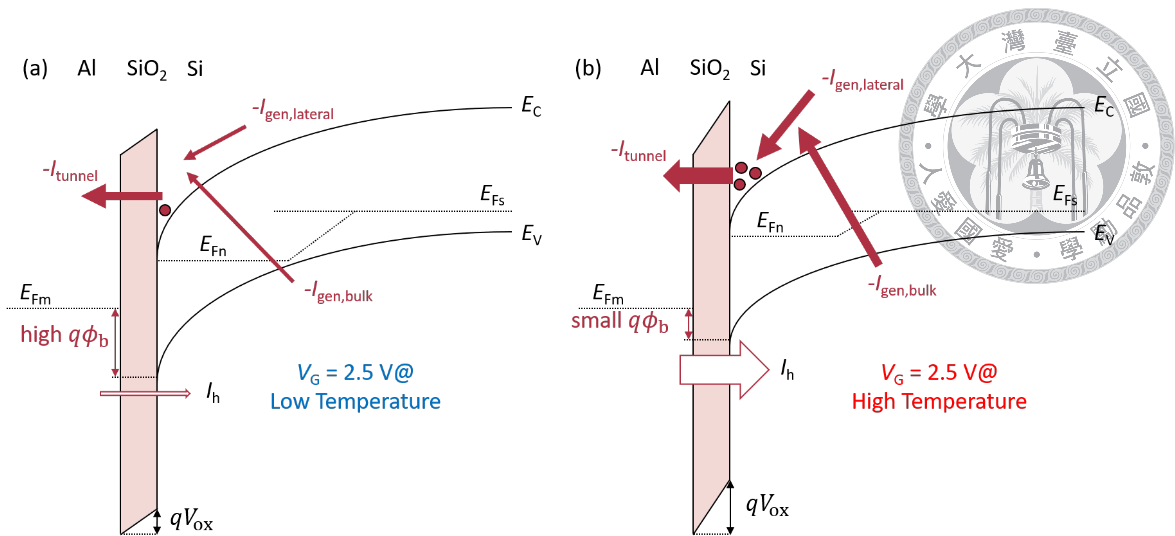

Figure 4–10. Band diagram at 2.5 V under (a) low and (b) high temperatures.

4.4.3 Evidence of Hole Injection Current–Measurement Under Various Temperature

The measurements under different temperatures are carried out to find out the importance of hole injection current. **Figure 4–10** (a) and (b) show the band diagram at 2.5 V under low and high temperatures. V_{ox} holds a lower value at a low temperature because of the less thermal generation electron. In this situation, the hole current is blocked by a high Schottky barrier height. Thus, the current of the MISTD is dominated by the electron current. The dominance of electron current at low temperatures is shown by the modeling result in **Figure 4–11** (a). The modeling result is calculated with t_{ox} = 26.5 Å and Q_{eff}/q = 2.8×10^{11} cm^{-2}. In **Figure 4–11** (a), one can find that the I_e dominates I_{total} for about T < 300 K. The variance of I_e is governed by thermal generation rate and effective generation area, which are proportional to n_i and Λ^2, respectively. I_e can be approximated to

$$I_e \propto n_i\Lambda^2. \tag{4.10}$$

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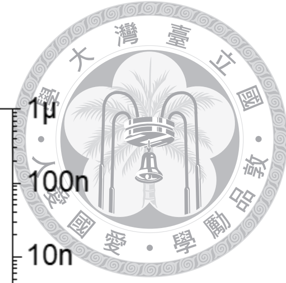

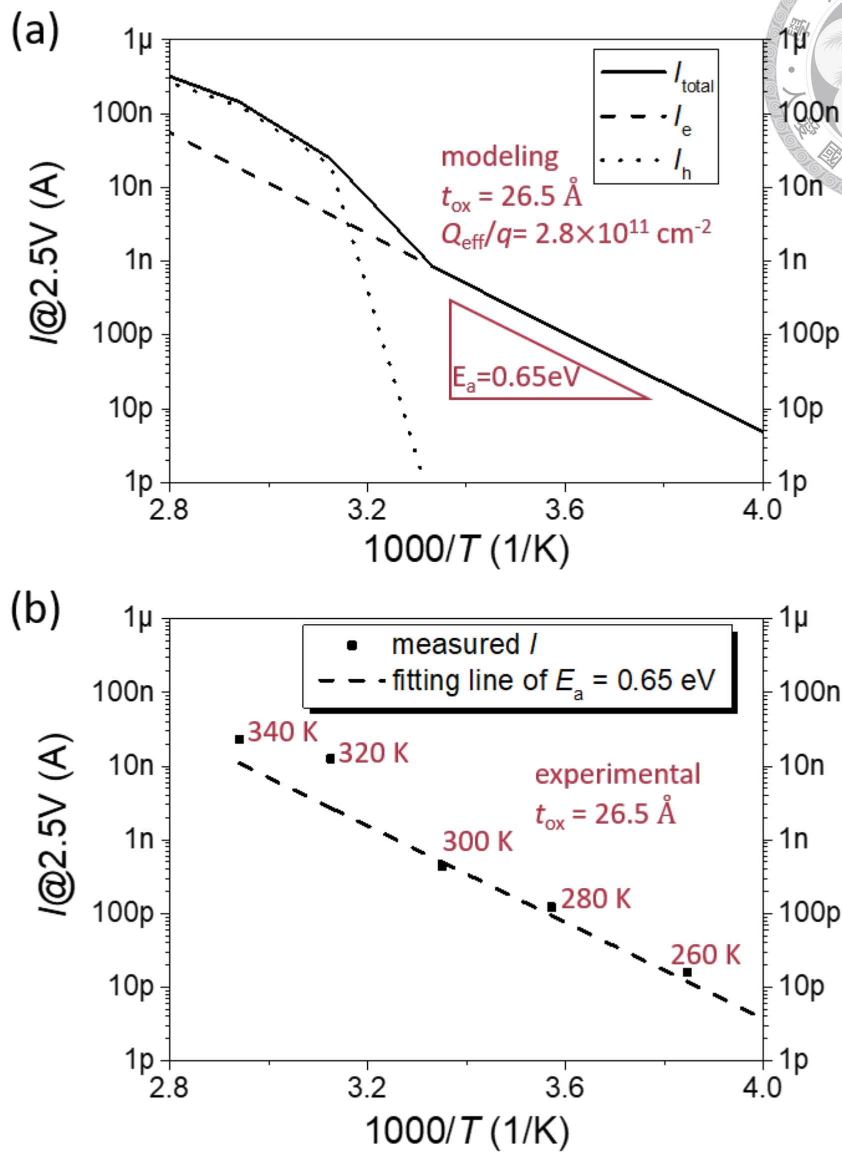

Figure 4–11. (a) Modeling and (b) measured current at 2.5 V for various temperature.

n_i has an activation energy of $\approx$ 0.55 eV, and Λ with Q_{eff}/q of 2.8×10^{11} cm^{-2} has an activation energy of $\approx$ 0.05 eV. Thus, I_e has an activation energy of $\approx$ 0.65 eV, which is labeled in **Figure 4–11** (a). On the other hand, in the higher temperature case in **Figure 4–10** (b), a larger thermal generation current supplies the inversion layers and therefore carrying a higher V_{ox}. In this situation, the hole Schottky barrier height becomes smaller (or even

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negative) and let the hole injection current dominates. The dominance of hole current is shown in **Figure 4−11** (a) for around $T > 300$ K. The calculated current behavior in **Figure 4−11** (a) shows that I_{total} follows $E_{\mathrm{a}} = 0.65$ eV at low temperatures but deviates from $E_{\mathrm{a}} = 0.65$ eV at high temperatures when the hole injection current becomes significant.

To confirm the observation in modeling, a fresh device on the same wafer with $t_{\mathrm{ox}} =$ 26.5 Å is measured. The measured results are shown in **Figure 4−11** (b). For $T =$ 260, 280, and 300 K, the measured current follows $E_{\mathrm{a}} = 0.65$ eV. However, at $T =$ 320 and 340 K, a current level higher than $E_{\mathrm{a}} = 0.65$ eV fitting line is observed. The tendency of the measured current-temperature relation is similar to the modeling as shown in **Figure 4−11** (a).

4.5 Summary

This chapter proposes a model based on the model in **Chapter 3**. This model utilizes the electrostatic of MISTD calculated in **Chapter 3** to derive the hole injection current. The magnitude of the hole injection current is strongly dependent on the level of SBHM. A quantitative calculation of SBHM and hole injection current is described in **Section 4.2**. In **Section 4.4.1**, the importance of hole current is demonstrated by calculation, and the increase of MISTD's reverse biased current with oxide thickness is also shown. The comparisons between the modeling and the experimental are shown in **Section 4.4.2**. The comparisons indicate that the oxide charges play an important role in the current behavior of MISTD. Our modeling can describe the tendency of MISTD's current with different t_{ox} and the number of Q_{eff}/q. In **Section 4.4.3**, the relation between current and temperature is examined by modeling and experimental. The modeling can predict the tendency

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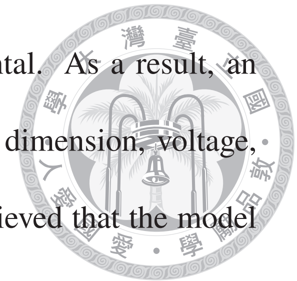

of current-temperature relation when compared with the experimental. As a result, an universal model considering oxide charges, oxide thickness, device dimension, voltage, and temperature is suggested in **Chapter 3** and **Chapter 4**. It is believed that the model discussed in these two chapters can describe the electrostatic and current behavior of a MISTD completely.

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5

Modeling III: Impact of Oxide Charge on the Capacitance-Frequency Characteristic of MISTD

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5.1 Background

In previous chapters, the impacts of oxide charges on HFCV and IV characteristics are discussed. As described in **Section 2.3.5**, it is known that the outer oxide charges will affect the Capacitance-Frequency (CF) relation. Actually, the phenomenon was first observed by Hofstein et al. in 1964 [32]. Hofstein et al. found that the CF relation for MOS capacitors with n-type and p-type substrates are very different and suspected that the existence of positive oxide charges in the SiO_2 layer causes the observation. In 1965, the mechanism of how the oxide charges affect CF relation was discussed by both Hofstein et al. [33] and Nicollion et al. [34]. They proposed a schematic mechanism as shown in **Figure 5–1**. The positive oxide charges will deplete the majority holes in the p-type substrate to form a depletion capacitance and attract some minority electrons to form a lateral conduction channel. The conduction channel will laterally transport the AC signal, increasing the effective control region and the measured capacitance. Though the mechanism has been proposed, a detailed comparison between calculation and experimental is still lack of discussion.

Since the 1970s, few works have discussed the impact of outer oxide charges on the CF relation because of the development of annealing processes. The annealing processes can reduce the oxide charges to the order of $Q_{\mathrm{eff}}/q = 10^{11}$ cm^{-2} or even less [67–70]. With Q_{eff}/q in the order of 10^{11} cm^{-2}, the effect of outer oxide charges becomes less significant.

Though the influence of outer oxide charge decreased because of the improved annealing process, the phenomenon still attracts some work in recent decades. Significant differences in frequency responses between MOS(n) and MOS(p) capacitors are observed [6, 71, 72]. It is pointed out that the difference can affect the result when extracting the

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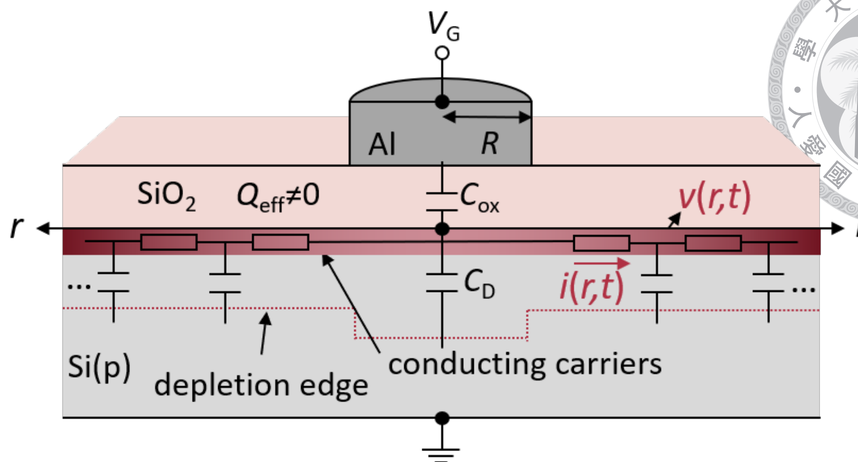

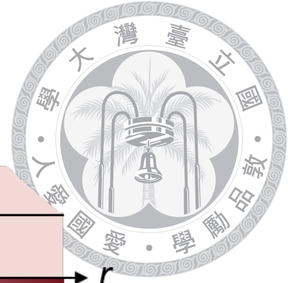

Figure 5–1. Mechanism of how the outer oxide charges contribute to the capacitance of MOS structure. The mechanism was proposed by Hofstein et al. [33] and Nicollion et al. [34] in 1965. AC current signal $i(r,t)$, voltage signal $v(r,t)$, and coordinate for model derivation are also attached.

minority carrier's lifetime by measuring transition frequency [6]. By the way, a measured conductance G of the MOS capacitor following the relation of $G \propto \omega^s$ is observed [73], where ω is the measuring angular frequency, and s is a fitting parameter. The works mentioned above [6, 71–73] attribute their abnormal observations to the existence of the oxide charges and the lateral coupling. However, the above works focus on something other than discussing the outer oxide charges. Thus, a detailed calculation of how the outer oxide charges affect the capacitance (C) and conductance (G) of MOS structures is still unclear.

In this chapter, we derive an analytical model for describing C and G of MOS structures depending on device dimension, doping concentration, measuring frequency, and the number of oxide charges. A MISTD is also measured for comparison. Finally, the model is compared with TCAD simulations under various situations.

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5.2 Model Derivation

In this section, the impact of outer oxide charges on a circle MOS device with a radius R is explored. The structure is the same as our experimental device. Devices biased at $0 < V_G < V_C$ are considered to simplify the derivation. In this situation, electron concentration distribution outside the electrode is nearly uniform.

5.2.1 Admittance Contribution from Lateral Region

The positive effective oxide charges Q_{eff} outside the electrode will attract minority electrons to form a lateral conducting channel with sheet resistance R_s and deplete majority holes to form a depletion capacitance $C_{d,out}$ per unit area. To analytically calculate the capacitance value laterally contributed by the lateral region, we define the origin of the radial direction at the center of the circle device. The definition of coordinate is indicated in **Figure 5−1** . The lateral region can be lumped up as an equivalent circuit as shown in **Figure 5−2** (a). From the equivalent circuit in **Figure 5−2** (a), one can observe a set of serially connected resistors with incremental conductance $dG_L(r)$ and parallel connected capacitors with incremental capacitance $dC_L(r)$ at $r > R$, where r is the radius of circle coordinate. With considering the circle coordinate, the conductance $dG_L(r)$ and capacitance $dC_L(r)$ values at position r can be written down as

$$dG_L(r) = \frac{2\pi r}{R_s dr}, \tag{5.1}$$

and

$$dC_L(r) = 2\pi r C_{d,out} dr. \tag{5.2}$$

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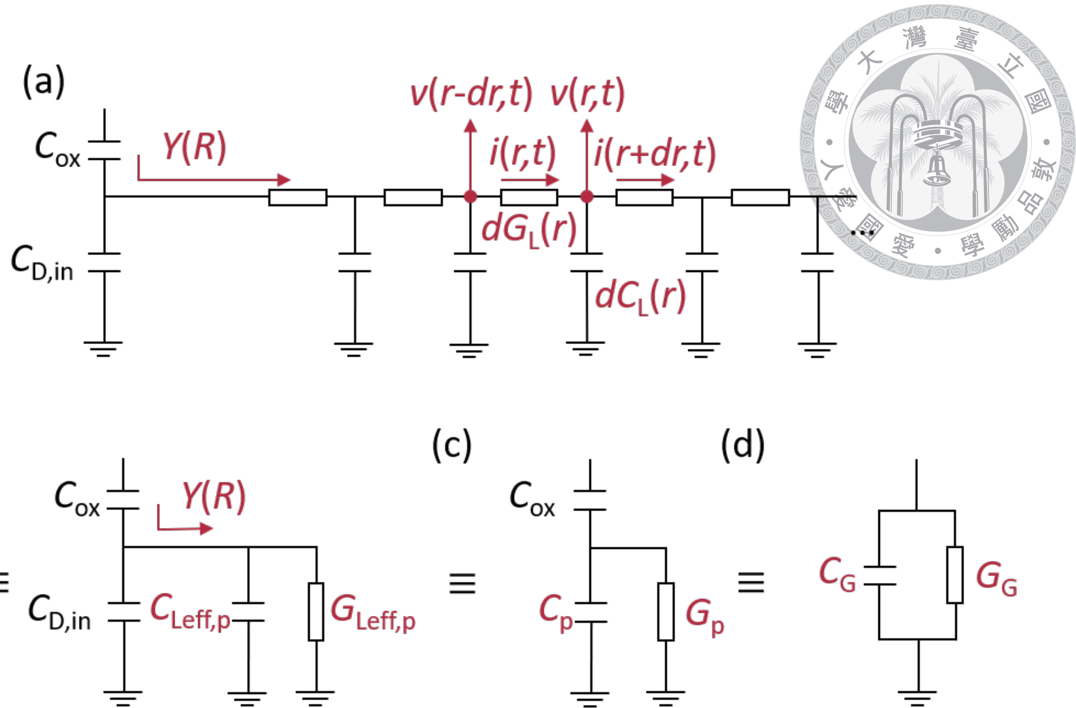

Figure 5–2. (a) Equivalent circuit considering the contribution of the lateral region. (b) The equivalent circuit of (a) with $Y(R)$ being seen as a parallel connection of $C_{\mathrm{Leff,p}}$ and $G_{\mathrm{Leff,p}}$. (c) The equivalent circuit of (b) with the part of silicon being seen as a parallel connection of C_{p} and G_{p}. (d) The overall equivalent circuit from measurement.

We further define the current and voltage of the AC signal as $i(r,t)$ and $v(r,t)$, depending on radius r and time t. $dG_{\mathrm{L}}(r)$, $dC_{\mathrm{L}}(r)$, $i(r,t)$, and $v(r,t)$ are all labeled in **Figure 5–2** (a). In **Figure 5–2** (a), the oxide capacitance C_{ox} and depletion capacitance under the electrode $C_{\mathrm{D,in}}$ are also considered. The serial connection of C_{ox} and $C_{\mathrm{D,in}}$ is the classic model for high-frequency capacitance [7]. It is defined that the admittance seen at the device's edge by $Y(R)$, which is contributed by the lateral region. With the above definitions and detailed calculations in **Appendix C**, one can derive that

$$Y(R) = 2\pi R\sqrt{\frac{\omega C_{\mathrm{d,out}}}{R_{\mathrm{s}}}}\frac{K_1(j^{\frac{1}{2}}R\sqrt{\omega C_{\mathrm{d,out}}R_{\mathrm{s}}})}{K_0(j^{\frac{1}{2}}R\sqrt{\omega C_{\mathrm{d,out}}R_{\mathrm{s}}})}j^{\frac{1}{2}}, \tag{5.3}$$

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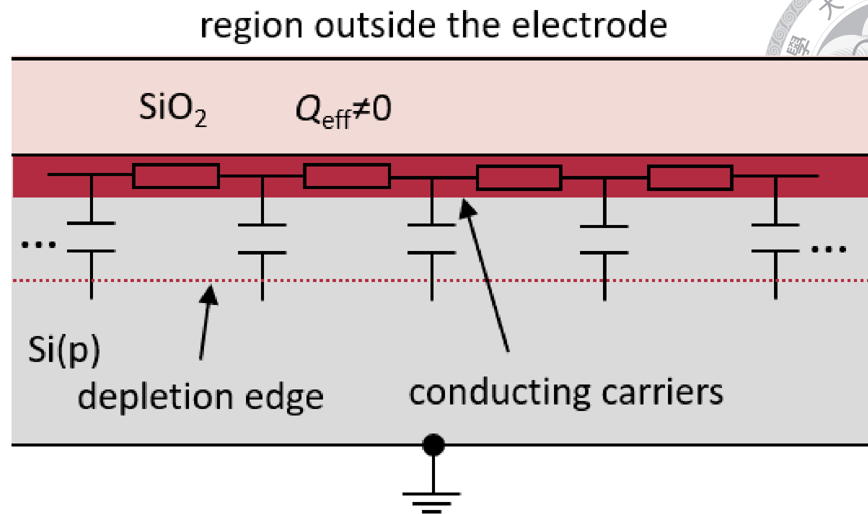

Figure 5–3. The oxide-semiconductor system outside the electrode.

where ω is the measuring angular frequency, and K_1/K_0 is the modified Bessel function of the second kind with orders 1/0.

In the above calculations, R_s and $C_{d,out}$ are treated as known values. However, R_s and $C_{d,out}$ are dependent on N_a and Q_{eff}. Fortunately, R_s and $C_{d,out}$ can be derived from the semiconductor's basic theories [1]. As shown in **Figure 5–3**, the region outside the electrode is an oxide-semiconductor system. Charges per unit area in silicon Q_{si} need to balance with Q_{eff}. Thus, $\psi_{s,out}$ needs to satisfy the equation

$$Q_{eff} = -Q_{si} = \sqrt{2qN_a\epsilon_{si}\psi_{s,out}(1 + \frac{kT}{q\psi_{s,out}}\frac{n_i^2}{N_a^2}e^{\frac{q\psi_{s,out}}{kT}})}, \tag{5.4}$$

From (5.4), one can find that $\psi_{s,out}$ is decided when N_a and Q_{eff} are known. With the decided $\psi_{s,out}$, $C_{d,out}$ can be calculated by using depletion approximation as

$$C_{d,out} = \sqrt{\frac{qN_a\epsilon_{si}}{2\psi_{s,out}}}, \tag{5.5}$$

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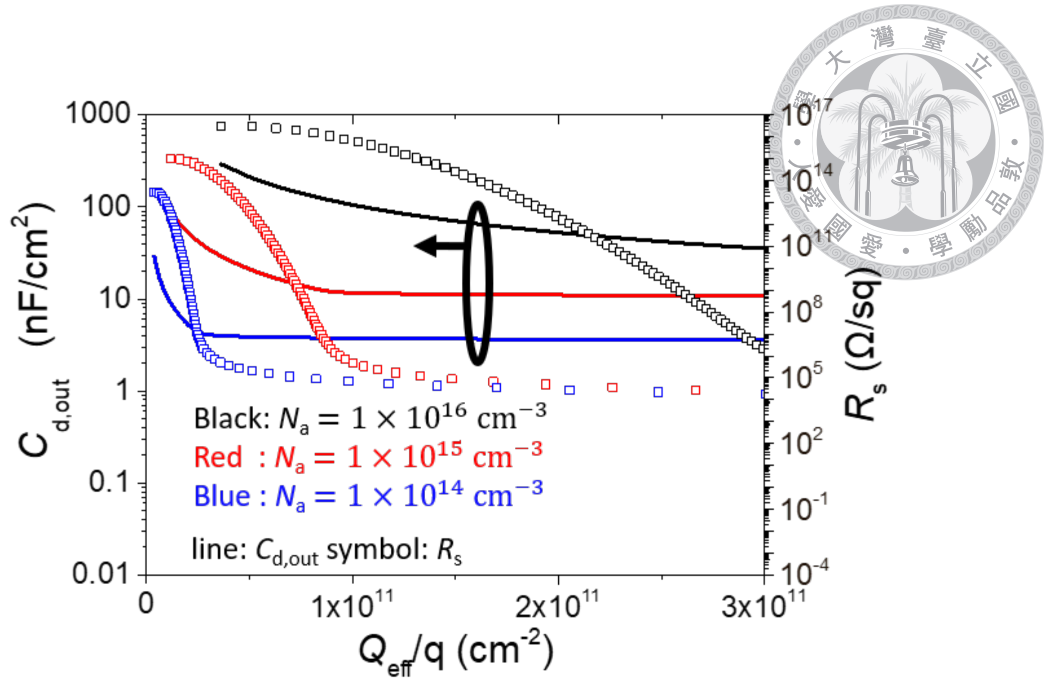

Figure 5–4. The calculated $C_{\mathrm{d,out}}$ and R_{s} under different N_{a} and Q_{eff}.

and R_{s} can be expressed as

$$R_{\mathrm{s}} = \frac{1}{\mu_{\mathrm{n}}|Q_{\mathrm{Si,e}}|} = \frac{1}{\mu_{\mathrm{n}}\sqrt{2qN_{\mathrm{a}}\epsilon_{\mathrm{si}}\psi_{\mathrm{s,out}}}}[\sqrt{1+\frac{kT}{q\psi_{\mathrm{s,out}}}\frac{n_i^2}{N_{\mathrm{a}}^2}e^{\frac{q\psi_{\mathrm{s,out}}}{kT}}}-1]^{-1}, \tag{5.6}$$

where $Q_{\mathrm{Si,e}}$ is electron's charges per unit area in silicon. The calculated $C_{\mathrm{d,out}}$ and R_{s} under different N_{a} and Q_{eff} are plotted in **Figure 5–4**. With the above discussion, the laterally contributed capacitance and conductance as induced by outer oxide charges can be calculated with known R, N_{a}, Q_{eff}, and ω.

5.2.2 Admittance Contribution from Lateral Region-An Approximation

Though the discussion in **Section 5.2.1** can calculate $Y(R)$, the calculation is complex because of the Bessel function in (5.3) and the balancing condition in (5.4). In this section, we propose some simplified equations to calculate $Y(R)$ in a "pen and paper" way.

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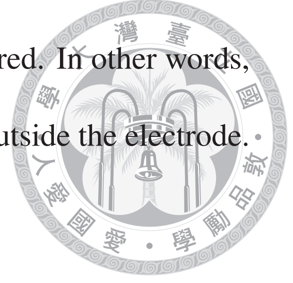

To simplify the balancing condition (5.4), $\psi_{\text{s,out}} < 2\phi_{\text{F}}$ is considered. In other words, we consider the situation where Q_{eff} cannot induce strong inversion outside the electrode. In this situation, (5.4) can be simplified as

$$Q_{\text{eff}} = -Q_{\text{si}} = \sqrt{2qN_{\text{a}}\epsilon_{\text{si}}\psi_{\text{s,out}}},\ \psi_{\text{s,out}} < 2\phi_{\text{F}}. \tag{5.7}$$

The outer region without strong inversion also implies a higher R_{s}.

$Y(R)$ with high R_{s} is subsequently considered to simplify the Bessel function. As shown in **Figure 5–2** (b), $Y(R)$ can be seen as a set of parallel connection of lateral effect capacitor ($C_{\text{Leff,p}}$) and resistor ($G_{\text{Leff,p}}$). $Y(R)$ can be written down as

$$Y(R) = G_{\text{Leff,p}} + j\omega C_{\text{Leff,p}}. \tag{5.8}$$

We also define the part of the Bessel function in (5.3) as

$$\widetilde{Y}(R\sqrt{\omega R_{\text{s}}C_{\text{d,out}}}) = \frac{K_1(j^{\frac{1}{2}}R\sqrt{\omega R_{\text{s}}C_{\text{d,out}}})}{K_0(j^{\frac{1}{2}}R\sqrt{\omega R_{\text{s}}C_{\text{d,out}}})}j^{\frac{1}{2}}, \tag{5.9}$$

which is a dimension less complex number. The calculated phase and amplitude of $\widetilde{Y}(R\sqrt{\omega R_{\text{s}}C_{\text{d,out}}})$ under different $R\sqrt{\omega R_{\text{s}}C_{\text{d,out}}}$ are plotted in **Figure 5–5** (a) and (b), respectively. From **Figure 5–5** , one can find that

$$\widetilde{Y}(R\sqrt{\omega R_{\text{s}}C_{\text{d,out}}}) \approx e^{j\frac{\pi}{4}} = \frac{1}{\sqrt{2}} + \frac{1}{\sqrt{2}}j \tag{5.10}$$

when $R\sqrt{\omega R_{\text{s}}C_{\text{d,out}}}$ is high enough. By inserting (5.10) to (5.3), the admittance contributed

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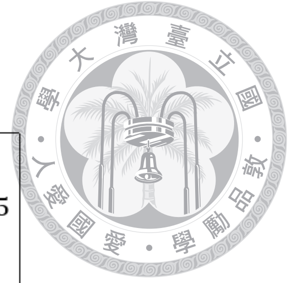

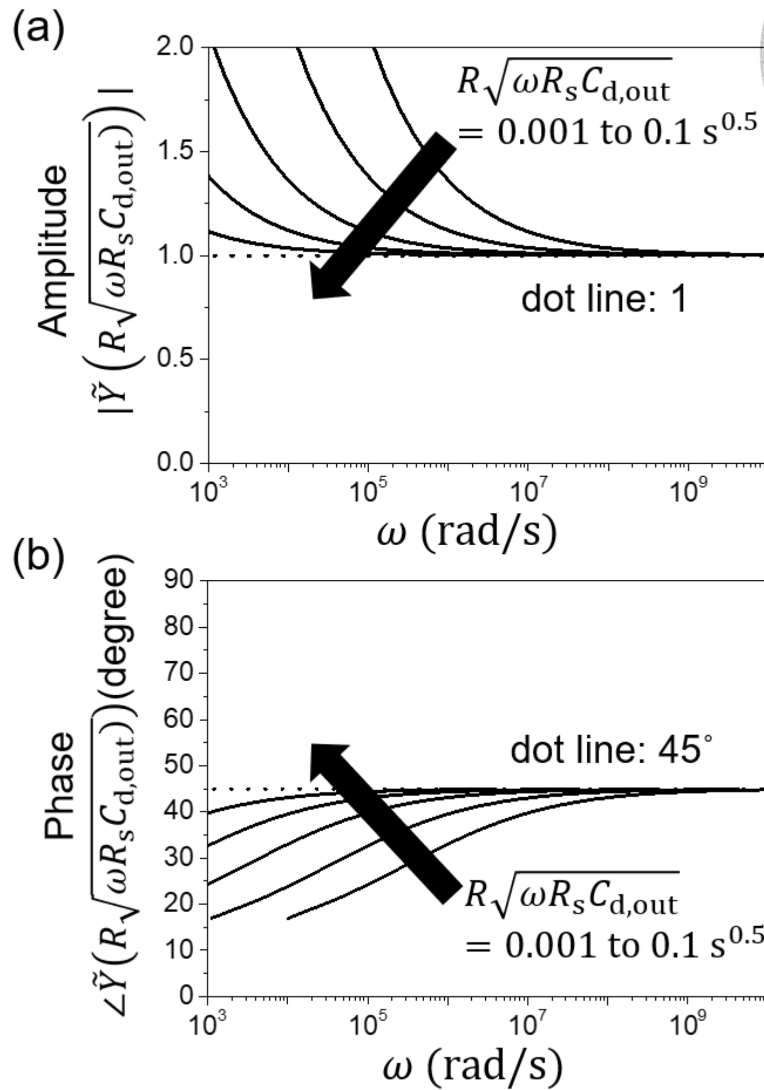

Figure 5−5. (a) Amplitude and (b) phase of $\widetilde{Y}(R\sqrt{\omega R_s C_{d,out}})$.

by the lateral region can be approximated to

$$Y(R) \approx 2\pi R\sqrt{\frac{\omega C_{d,out}}{R_s}}(\frac{1}{\sqrt{2}}+\frac{1}{\sqrt{2}}j) = G_{Leff,p} + j\omega C_{Leff,p} \tag{5.11}$$

$G_{Leff,p}$ and $C_{Leff,p}$ can be extracted from (5.11) as

$$G_{Leff,p} = 2\pi R\sqrt{\frac{\omega C_{d,out}}{2R_s}}, \tag{5.12}$$

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and

$$C_{\text{Leff,p}} = 2\pi R\sqrt{\frac{C_{\text{d,out}}}{2\omega R_{\text{s}}}}. \tag{5.13}$$

The decreasing of $C_{\text{Leff,p}}$ with ω implies that the effective lateral control region decreases with ω. The effect of the lateral region can be easily calculated by the discussion in this section when $R\sqrt{\omega R_{\text{s}} C_{\text{d,out}}}$ is high enough.

5.2.3 Modeling Procedure

Figure 5−6 shows the procedure to calculate the laterally contributed admittance $Y(R)$. Corresponding equations to calculate each term are listed in **TABLE 5−I**.

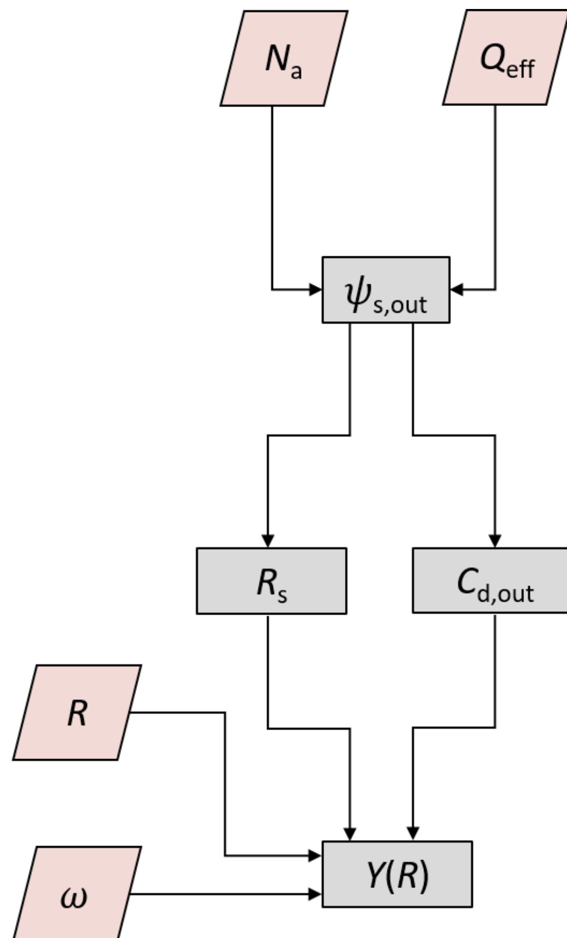

Figure 5−6. Modeling procedure to calculate the laterally contributed admittance $Y(R)$.

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TABLE 5–I
The corresponding equations to calculate the term in **Figure 5–6** .

Term	Description	Unit	Equation	Equation for Approximation
$\psi_{\mathrm{s,out}}$	surface band bending outside the electrode	V	(5.4)	(5.7)
$C_{\mathrm{d,out}}$	depletion capacitance outside the electrode	F/cm^2	(5.5)	(5.5)
R_{s}	surface sheet resistance outside the electrode	Ω/sq	(5.6)	(5.6)
$Y(R)$	admittance contributed by the lateral region	1/Ω	(5.3)	(5.8), (5.12), (5.13)

5.3 Experimental Detail

A MISTD with an oxide thickness of 25.2Å is selected to measure the CF characteristic. Measuring frequencies are 1, 3, 10, 30, 100, and 300 kHz. Measurements before and after immersion in D.I. water are carried out. TCAD simulations for different N_{a}, Q_{eff}, R, and ω are implemented to check the validity of the modeling.

5.4 Result and Discussion

5.4.1 AC Lateral Decay Length

The oxide-charge-induced channel can enlarge the effective lateral control region of the MOS device. As discussed in **Section 5.2**, the lateral control region will be affected by ω, Q_{eff}, and N_{a}. In this section, an AC signal's effective lateral control length l_{AC} is defined to estimate the control regions depending on different conditions. (C.8), calculated in **Appendix C**, shows that the voltage's AC signal on the silicon's surface is

$$v(r) = C_1 K_0(j^{\frac{1}{2}} r \sqrt{\omega C_{\mathrm{d,out}} R_{\mathrm{s}}}) e^{j\omega t}, \tag{5.14}$$

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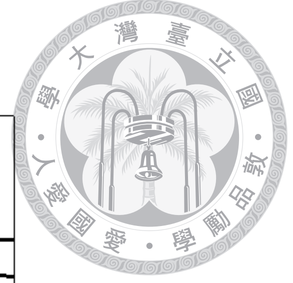

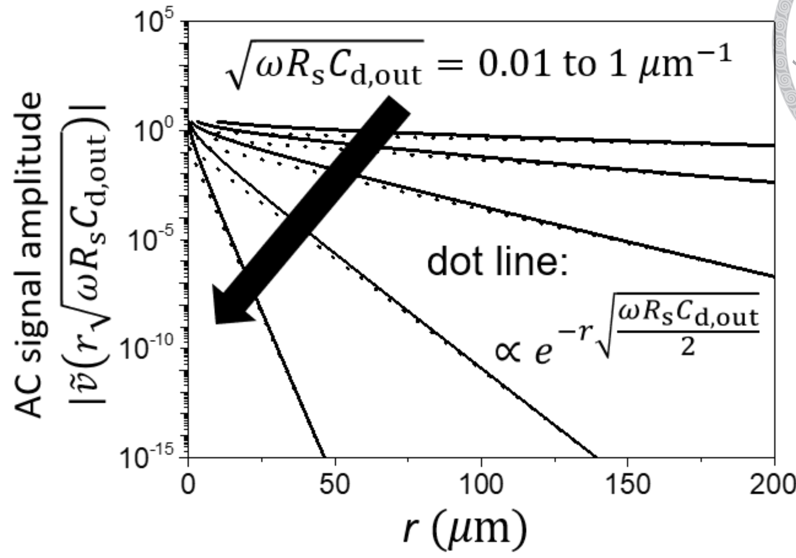

Figure 5−7. Amplitude of dimension less AC signal $\widetilde{v}(r\sqrt{\omega C_{\mathrm{d,out}} R_{\mathrm{s}}})$.

where C_1 is a constant depending on the boundary condition. We define the complex part of $v(r)$ as

$$\widetilde{v}(r\sqrt{\omega C_{\mathrm{d,out}} R_{\mathrm{s}}}) = K_0(j^{\frac{1}{2}} r\sqrt{\omega C_{\mathrm{d,out}} R_{\mathrm{s}}})e^{j\omega t}, \tag{5.15}$$

which is a dimension less term. $\widetilde{v}(r\sqrt{\omega C_{\mathrm{d,out}} R_{\mathrm{s}}})$ under different $\sqrt{\omega C_{\mathrm{d,out}} R_{\mathrm{s}}}$ is plotted in **Figure 5−7** . As shown in **Figure 5−7** , $\widetilde{v}(r\sqrt{\omega C_{\mathrm{d,out}} R_{\mathrm{s}}})$ is proportional to $\exp(-r\sqrt{\omega C_{\mathrm{d,out}} R_{\mathrm{s}}/2})$ when r is large enough. The l_{AC} is defined as

$$l_{\mathrm{AC}} = \sqrt{\frac{2}{\omega C_{\mathrm{d,out}} R_{\mathrm{s}}}}. \tag{5.16}$$

Visualized schematics of l_{AC} under different conditions are plotted in **Figure 5−8** . Schematic in **Figure 5−8** (a) shows l_{AC} decreases with f because the equivalent circuit of the outer region, as shown in **Figure 5−2** (a), is a serial connection of low-pass filters. **Figure 5−8** (b) indicates l_{AC} increases with Q_{eff} because higher Q_{eff} attracts more electrons and forms

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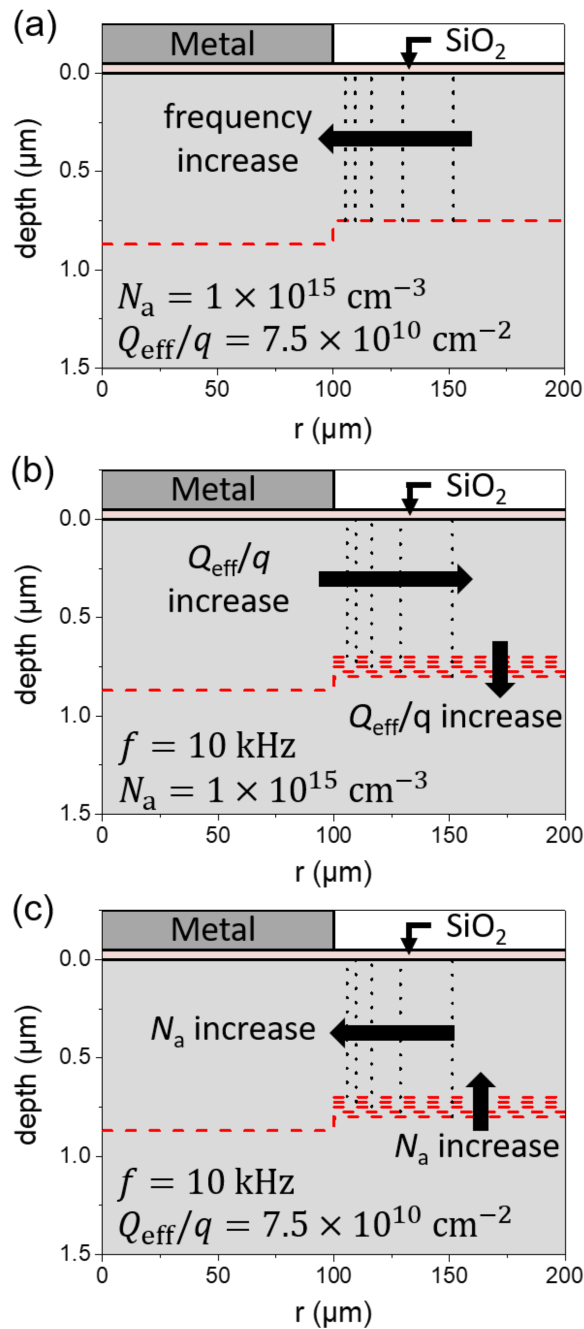

Figure 5–8. Visualized schematics of l_{AC}. The red dashed line is the depletion boundary, and the black dot line is the position of l_{AC}. (a) Frequency increases from 1 to 100 kHz with fixed $N_a = 10^{15}$ cm^{-3} and $Q_{eff}/q = 7.5 \times 10^{10}$ cm^{-2}. (b) Q_{eff}/q increases from 7 to 8×10^{10} cm^{-2} with fixed $N_a = 10^{15}$ cm^{-3} and $f = 10$ kHz. (b) N_a increases from 9×10^{14} to 1.1×10^{15} cm^{-3} with fixed $Q_{eff}/q = 7.5 \times 10^{10}$ cm^{-2} and $f = 10$ kHz.

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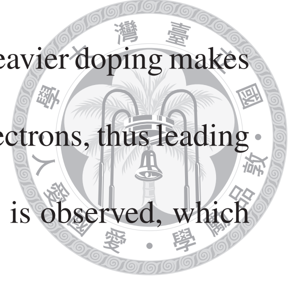

lower R_s. Finally, **Figure 5−8** (c) shows that l_{AC} decreases with N_a. Heavier doping makes Q_{eff} more difficult to invert the surface band bending and attract less electrons, thus leading to higher R_s. From **Figure 5−8**, l_{AC} with dimension of micrometers is observed, which is non-negligible when compared with the device's size.

5.4.2 Comparison with Experimental

Measured capacitance C_G from -2 to 2 V under frequencies 1, 3, 10, 30, 100, and 300 kHz are shown in **Figure 5−9**. **Figure 5−9** (a) and (b) are measured before and after immersion in D.I. water. The equivalent circuit of C_G is shown in **Figure 5−2** (d), where G_G is the measured conductance. With the equivalent circuits from **Figure 5−2** (c) and (d), C_p and G_p can be calculated from C_G and G_G as

$$C_p = \frac{\omega^2 C_G(C_{ox} - C_G) - G_G^2}{G_G^2 + \omega^2(C_{ox} - C_G)^2} C_{ox}, \tag{5.17}$$

and

$$G_p = \frac{\omega^2 C_{ox}^2 G_G}{G_G^2 + \omega^2(C_{ox} - C_G)^2}. \tag{5.18}$$

Comparing the equivalent circuit in **Figure 5−2** (b) and (c), one can find that

$$C_{Leff,p} = C_p - C_{D,in}, \tag{5.19}$$

and

$$G_{Leff,p} = G_p. \tag{5.20}$$

In (5.19), $C_{D,in}$ can be calculated with the relation between $C_{Leff,p}$ and $G_{Leff,p}$. Comparing (5.12) and (5.13), the relation of $C_{Leff,p} = G_{Leff,p}/\omega$ is observed. Thus, $C_{D,in}$ can be

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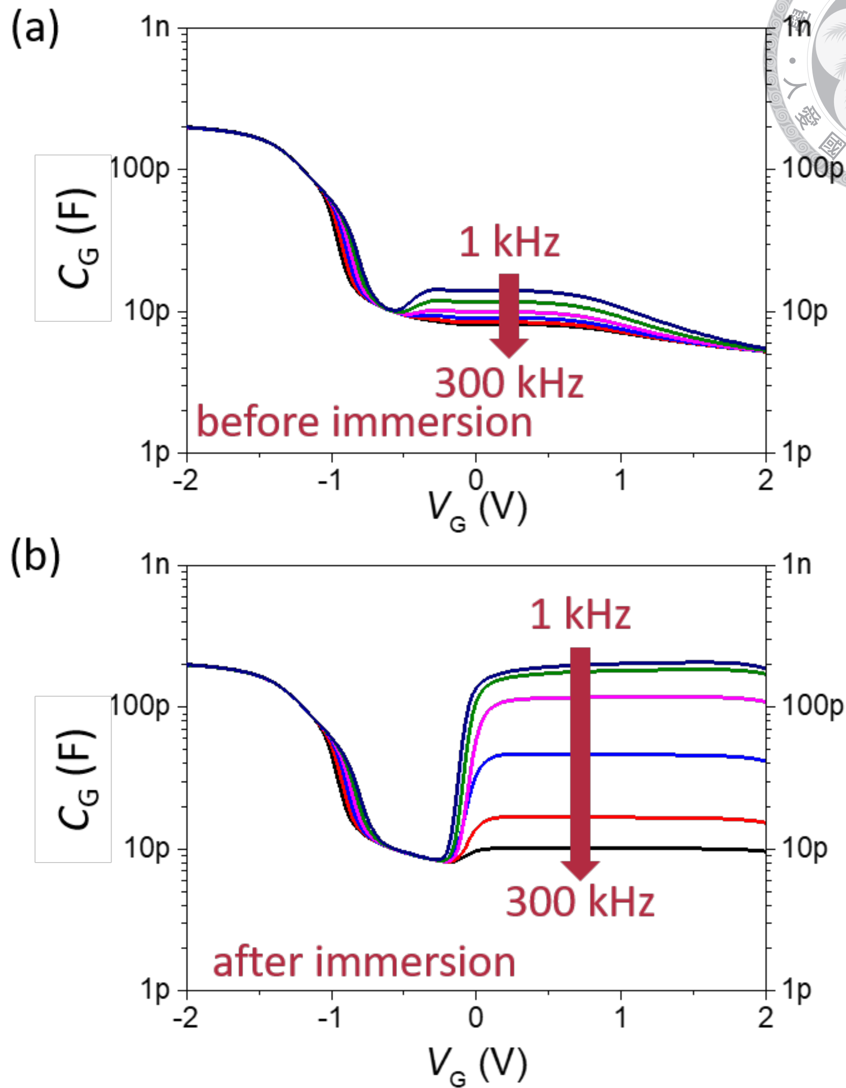

Figure 5–9. Measured capacitance under 1, 3, 10, 30, 100, and 300 kHz (a) before and (b) after immersion in D.I. water.

extracted from the relation

$$C_p - C_{D,in} = \frac{G_p}{\omega}. \tag{5.21}$$

The laterally effective contributed capacitance $C_{Leff,p}$ can be extracted from the measurement using (5.17) to (5.21). Extracted $C_{Leff,p}$ from **Figure 5–9** at $V_G = 0.5$ V is plotted in **Figure 5–10**. In **Figure 5–10**, calculated $C_{Leff,p}$ at various Q_{eff}/q from modeling is also attached. $C_{Leff,p}$ from the full model is plotted in solid lines, and $C_{Leff,p}$ from the ap-

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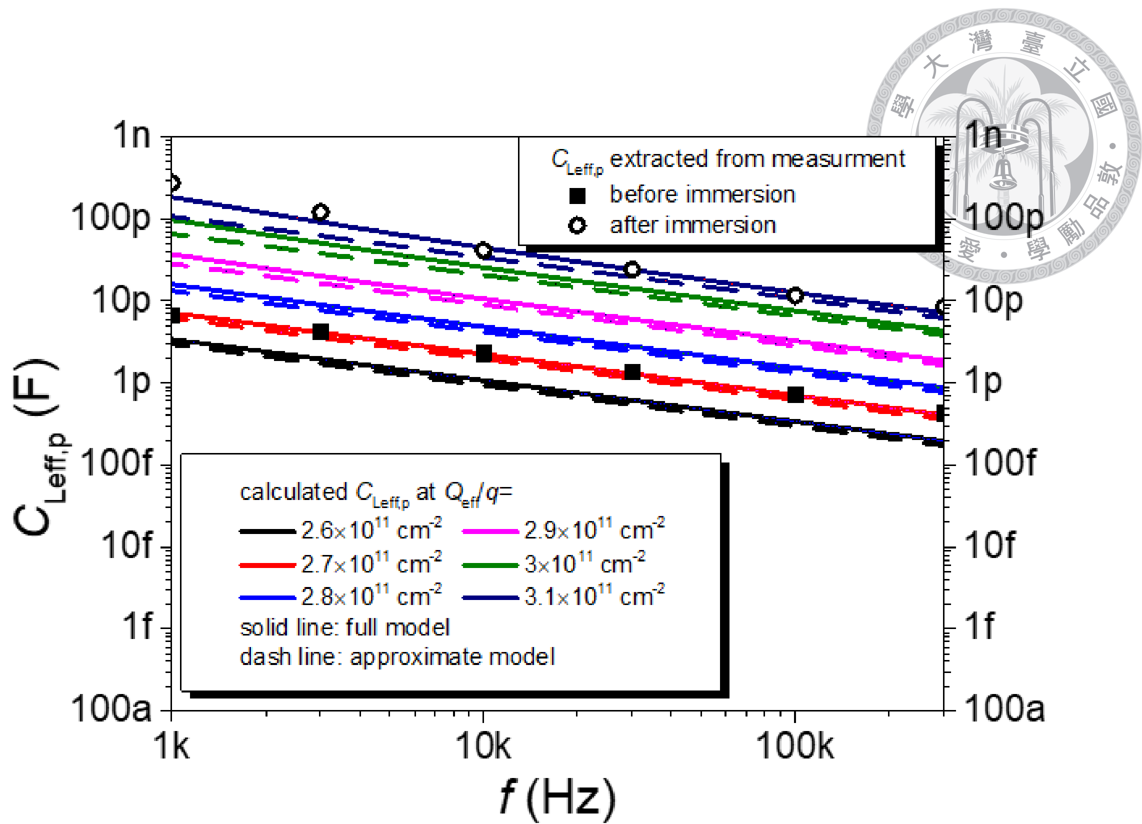

Figure 5–10. The extracted $C_{\text{Leff,p}}$ from **Figure 5–9** at $V_{\text{G}} = 0.5$ V. Calculated $C_{\text{Leff,p}}$ at various Q_{eff}/q from modeling is also attached. Both of full and approximate models are shown.

proximation model is plotted in dash lines. The approximation model agrees well with the full model before strong inversion ($Q_{\text{eff}}/q < 3 \times 10^{10}$ cm^{-2} for $N_{\text{a}} = 10^{16}$ cm^{-3}). From **Figure 5–10**, one can find that our experimental data fit well with $Q_{\text{eff}}/q = 2.7 \times 10^{10}$ and 3.1×10^{10} cm^{-2} before and after immersion, respectively. In **Figure 4–8**, Q_{eff}/q of the same device is expected to increase from 2.7×10^{10} to 3.05×10^{10} cm^{-2} when calculating the current characteristic. The range of Q_{eff} extract in this chapter agrees well with **Chapter 4**.

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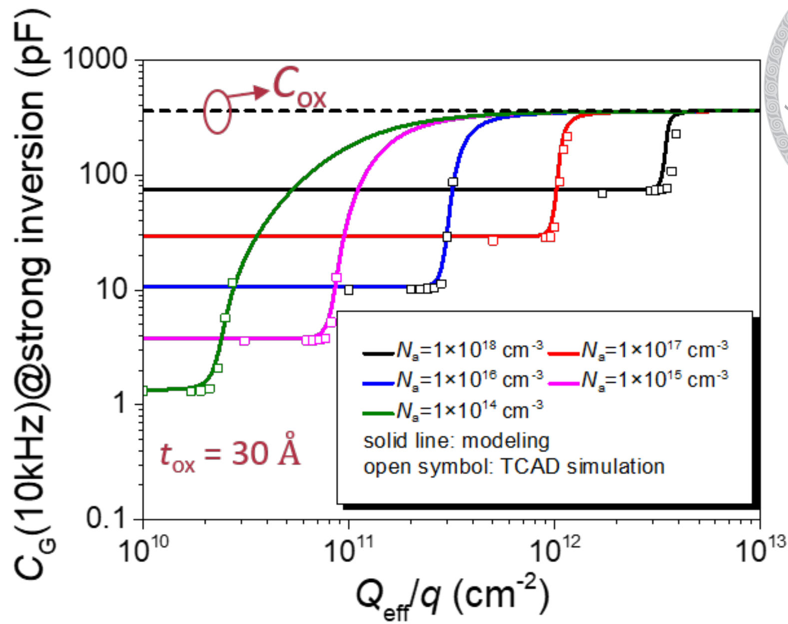

Figure 5–11. C_{G} v.s. Q_{eff}/q at 10 kHz under different doping concentrations.

5.4.3 Comparison with TCAD Simulation

In this section, TCAD simulations under different conditions are carried out to compare with our modeling. The capacitance values are extracted at V_{G} biased in strong inversion but lower than V_{C}.

Figure 5–11 shows the calculated and simulated relations of C_{G} v.s. Q_{eff}/q at 10 kHz under different doping concentrations. The calculated results are plotted in lines, and the simulated results are plotted in open symbols. With the equivalent circuits shown in **Figure 5–2** (c) and (d), the total capacitance C_{G} can be expressed as

$$C_{\mathrm{G}} = \frac{G_{\mathrm{p}}^2 + \omega^2 C_{\mathrm{p}}(C_{\mathrm{p}} + C_{\mathrm{ox}})}{G_{\mathrm{p}}^2 + \omega^2 (C_{\mathrm{p}} + C_{\mathrm{ox}})^2} C_{\mathrm{ox}}. \tag{5.22}$$

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Under high-frequency condition, C_G can be approximated as

$$C_G \approx \frac{C_p C_{ox}}{C_p + C_{ox}}. \tag{5.23}$$

When Q_{eff} is insufficient to invert the surface band bending, R_s is very high, and $C_p \approx C_{D,in}$. In this situation, C_G approaches to $C_{D,in}C_{ox}/(C_{D,in} + C_{ox})$, which is the classical model of HFCV [7]. However, when Q_{eff} can induce strong inversion at the silicon's surface, low R_s will lead to $C_p >> C_{ox}$. C_G approaches to C_{ox} in this high Q_{eff} situation. The calculated solid lines in **Figure 5−11** show the transition from $C_{D,in}C_{ox}/(C_{D,in} + C_{ox})$ to C_{ox} when Q_{eff} increases. In **Figure 5−11** , one can find that the TCAD simulations match well with our modeling under light and moderate doping concentrations, but a deviation is observed for $N_a = 10^{18}$ cm^{-3}. The deviation is possibly attributed to the strong surface field, which will lead to significant quantum confinement.

In our modeling, the device's dimension R is considered. **Figure 5−12** shows C_G v.s. f from modeling and simulation with different R. In **Figure 5−12** , fixed $N_a = 10^{15}$ cm^{-3} and $Q_{eff}/q = 10^{11}$ cm^{-2} are adopted. For large devices, $C_G \approx C_{ox}$ at lower frequencies because of large C_p, and $C_G \approx C_{D,in}C_{ox}/(C_{D,in} + C_{ox})$ at higher frequencies because $C_p \approx C_{D,in}$. However, for small devices, $C_p >> C_{D,in}$ in a wide frequency range because l_{AC} is larger than the device's dimension even under higher frequency. Thus, C_G keeps around C_{ox} for small devices.

In our modeling, the contribution from the lateral region is independent of t_{ox} when R, N_a, and Q_{eff} are fixed. However, the final C_G needs to consider the serially connected C_{ox}. The calculated and simulated C_G/C_{ox} v.s. t_{ox} at $N_a = 10^{15}$ cm^{-3} are plotted in **Figure 5−13** . The V_G's for strong inversion of various t_{ox}'s are also indicated for ref-

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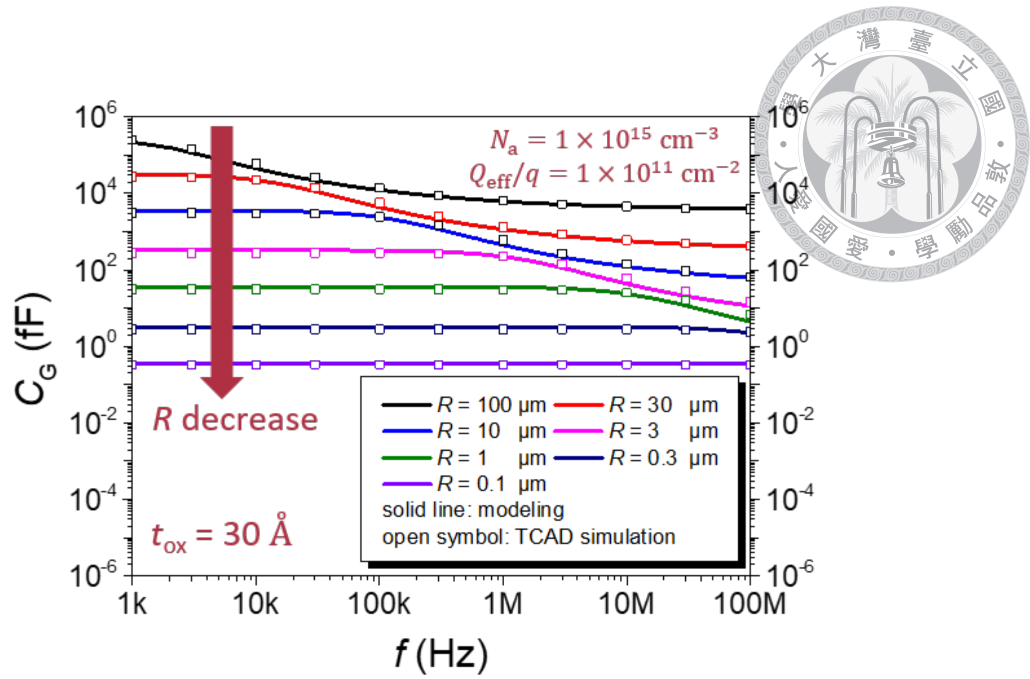

Figure 5–12. Modeled and simulated C_G v.s. f with different R. Fixed $N_a = 10^{15}$ cm^{-3} and $Q_{eff}/q = 10^{11}$ cm^{-2} are adopted.

erence. $Q_{eff}/q = 5 \times 10^{10}$ and 1×10^{11} cm^{-2} are shown in **Figure 5–13** (a) and (b), respectively. For **Figure 5–13** (a), $C_G \approx C_{D,in}C_{ox}/(C_{D,in} + C_{ox})$ for various frequencies because Q_{eff} is not large enough to invert the silicon's surface so the $C_{Leff,p}$ is very small. However, severe frequency dispersion is observed in **Figure 5–13** (b) because $C_{Leff,p}$ plays an important role. Our modeling fit well with the TCAD simulations under different t_{ox}, indicating the validity of our modeling.

5.5 Summary

In this chapter, a model considering the oxide-charge-induced lateral coupling is proposed to describe the capacitance of the MOS device. The model is based on the device's physical conditions (R, N_a, Q_{eff}) and measuring frequency. An approximation model suitable for Q_{eff} not large enough to induce strong inversion at the silicon's surface is proposed. The calculated l_{AC} in **Section 5.4.1** shows that the lateral control region can extend for around

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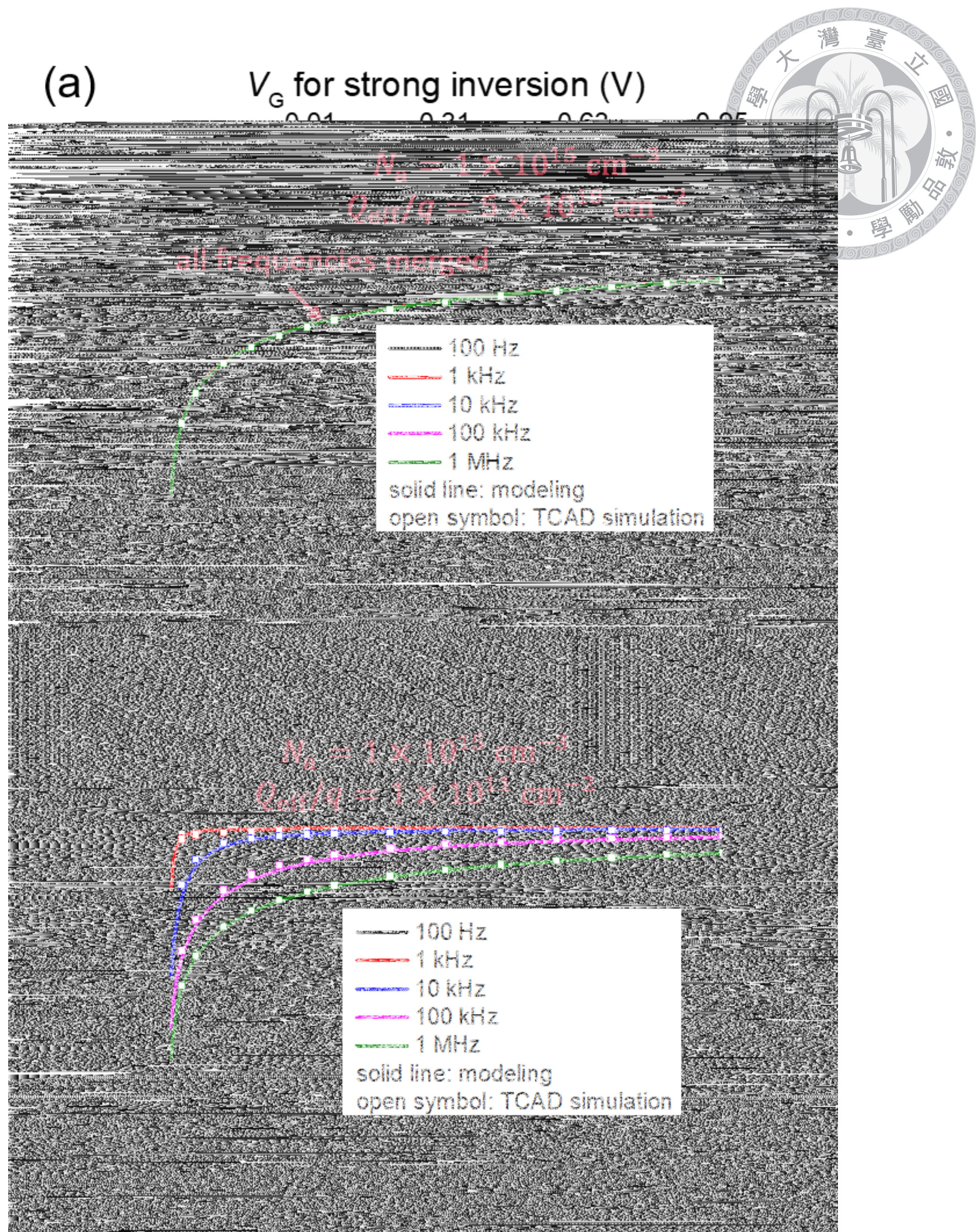

Figure 5–13. Calculated and simulated C_G/C_{ox} v.s. t_{ox} at $N_a = 10^{15}$ cm^{-3} with Q_{eff}/q = (a) 5×10^{10} and (b) 1×10^{11} cm^{-2}.

52 μm at 1 kHz for $N_a = 10^{15}$ cm^{-3} and $Q_{eff}/q = 10^{11}$ cm^{-2}. The l_{AC} is non-negligible in comparison with the device's dimension. The model is also compared with experimental and TCAD simulations in **Section 5.4.2** and **Section 5.4.3**. The comparison shows that the model works well under various conditions.

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6

Conclusions and Future Works

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6.2 Future Works. 108

6.1 Conclusions

In this dissertation, the impacts of outer oxide charges on the MISTD's electrical characteristics are widely discussed. It is found that the existence of outer oxide charges can strongly affect the capacitance and current characteristics of MISTD. Oxide-charge-induced lateral coupling mechanisms, which are believed to be responsible for the observations on experimental, are proposed. It is demonstrated that lateral coupling can extend for extremely long distances. These lateral coupling regions contribute to generation current, level of SBHM, and capacitance values.

Quantitative calculations of oxide-charge-induced lateral coupling are carried out from **Chapter 3** to **Chapter 5**. The HFCV (electrostatic) characteristic is first discussed in **Chapter 3** to find out the V_C and potential distribution of the devices. V_C increases with Q_{eff} because of the extra supplement of electron current from the lateral region. Based on the model of HFCV(electrostatic), SBHM and hole injection current are calculated in

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Chapter 4. Q_{eff} can affect the $I_{\text{total}} - t_{\text{ox}}$ relation and enlarge I_{total} for a few orders. The capacitance value considering lateral coupling is calculated in **Chapter 5**. Extra capacitance contributed from the lateral coupling region increases with Q_{eff} because of lower surface sheet resistance R_{s}. In **Chapter 3** to **Chapter 5**, the models are compared with experimental results or TCAD simulations for various conditions. The models proposed in this work are fundamental and are helpful for understanding MISTD.

6.2 Future Works

Some shortcomings of the models in this work are suggested to be improved in future works.

In **Figure 3–15** , the deviation between modeling and TCAD simulation for about 0.2-0.3 V is observed. It is possibly attributed to quantum confinement and field-dependent mobility in **Section 3.4.4**. The definition of an effective oxide thickness $t_{\text{ox,eff}}$ and effective mobility μ_{eff} is needed to calibrate the model. By the way, the lateral decay length Λ calculated in (3.18) adopts the depletion approximation. Thus, the model does not work well when amount of Q_{eff} is large enough to induce strong inversion at the silicon's surface. Charge sheet approximation [1] is a possible method to improve the model. The above improvement may be helpful for deciding V_{C} and calculating I_{total}.

As shown in **Figure 5–11** , our modeling deviates from TCAD simulation at $N_{\text{a}} = 10^{18}\ \text{cm}^{-3}$. It is attributed to the strong surface field for the heavily doped substrate. The strong surface field will cause quantum confinement (QC) at the silicon's surface. As a result, the lateral part in **Figure 5–2** (a) needs to be improved, as shown in **Figure 6–1** . In **Figure 6–1** , a quantum capacitance $dC_{\text{Q}}(r)$ is added when QC is significant [74]. TCAD simulations with and without the QC model are carried out to confirm our infer-

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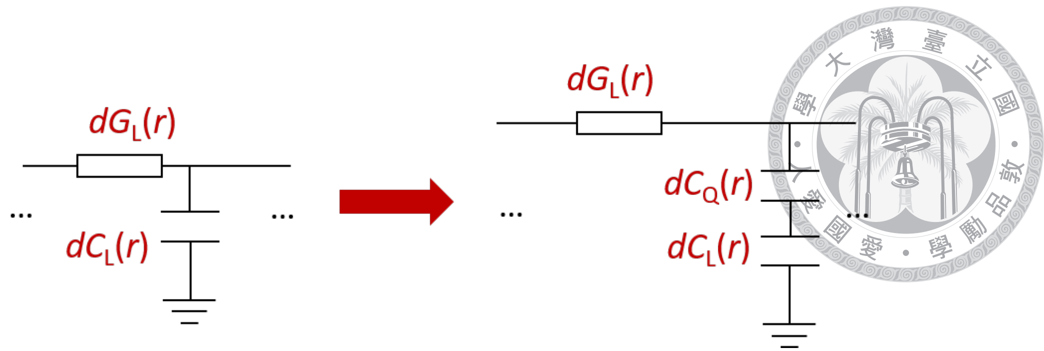

Figure 6–1. The improved lateral part of **Figure 5–2** (a) with QC effect considered.

ence. Simulated and calculated C_G v.s. f with $N_a = 10^{15}$ and 10^{18} cm^{-3} are plotted in **Figure 6–2** (a) and (b), respectively. In **Figure 6–2** (a), the simulation with and without the QC model overlaps, and the calculated result can describe the tendency of simulation because of the low doping concentration and surface field. However, a significant deviation between calculation and simulation with the QC model is observed in **Figure 6–2** (b). Once the QC model is removed, the simulated result overlap with our calculation. The result in **Figure 6–2** (b) indicates that the QC effect is the main reason causing the deviation between the calculation and simulation.

In **Chapter 5**, V_G biases in strong inversion but smaller than V_C is considered. The distribution of the electron's concentration outside the electrode is uniform under this bias region. Thus, a constant R_s can be used to derive the model. On the other hand, the electron's concentration outside the electrode, related to the profile of quasi-Fermi level difference in (3.17), is complex when biased in the DD region. However, MISTD's behavior in DD region is of interest because many applications of MISTD operate under this region. Solving the laterally contributed capacitance in the DD region is suggested for future work.

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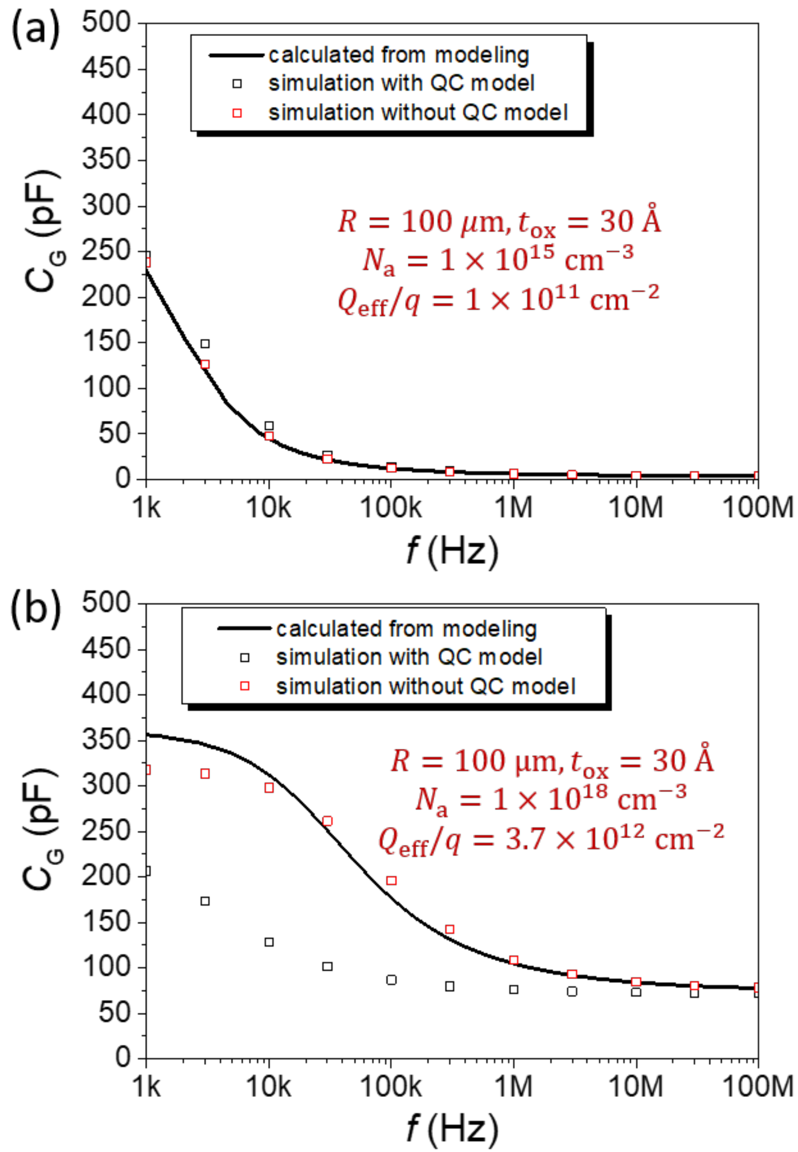

Figure 6–2. Simulated and calculated C_G v.s. f with N_a = (a) 10^{15} and (b) 10^{18} cm^{-3}. Simulations with and without the QC model are carried out for comparison.

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Appendix A

Oxide-Charge-Induced Lateral Coupling Length

A.1 Coordinate Definition and Approximations 111

A.2 Derivation of Oxide-Charge-Induced Lateral Coupling Length . 118

A.1 Coordinate Definition and Approximations

THE coordinate system needs to be defined to derive the analytical result of oxide-charge-induced lateral coupling length. The radial axis is presented as r and depth axis as y. We define the origin of radial direction at the center of a circle metal-insulator-semiconductor tunnel diode (MISTD) and the origin of depth y at the interface of oxide and silicon. The cross-section of the device and the coordinate axes (r, y) are plotted in **Figure A−1** (a). When a positive bias is applied to the electrode, the electrons under the electrode start to leak. The lacking of electrons leads to the non-equilibrium and quasi-Fermi-level (QFL) difference under the electrode as

$$\Delta\phi_{\mathrm{n,in}} = \frac{1}{-q}(E_{\mathrm{Fn}} - E_{\mathrm{Fp}}), \tag{A.1}$$

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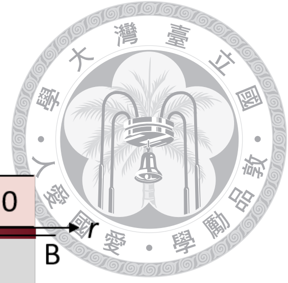

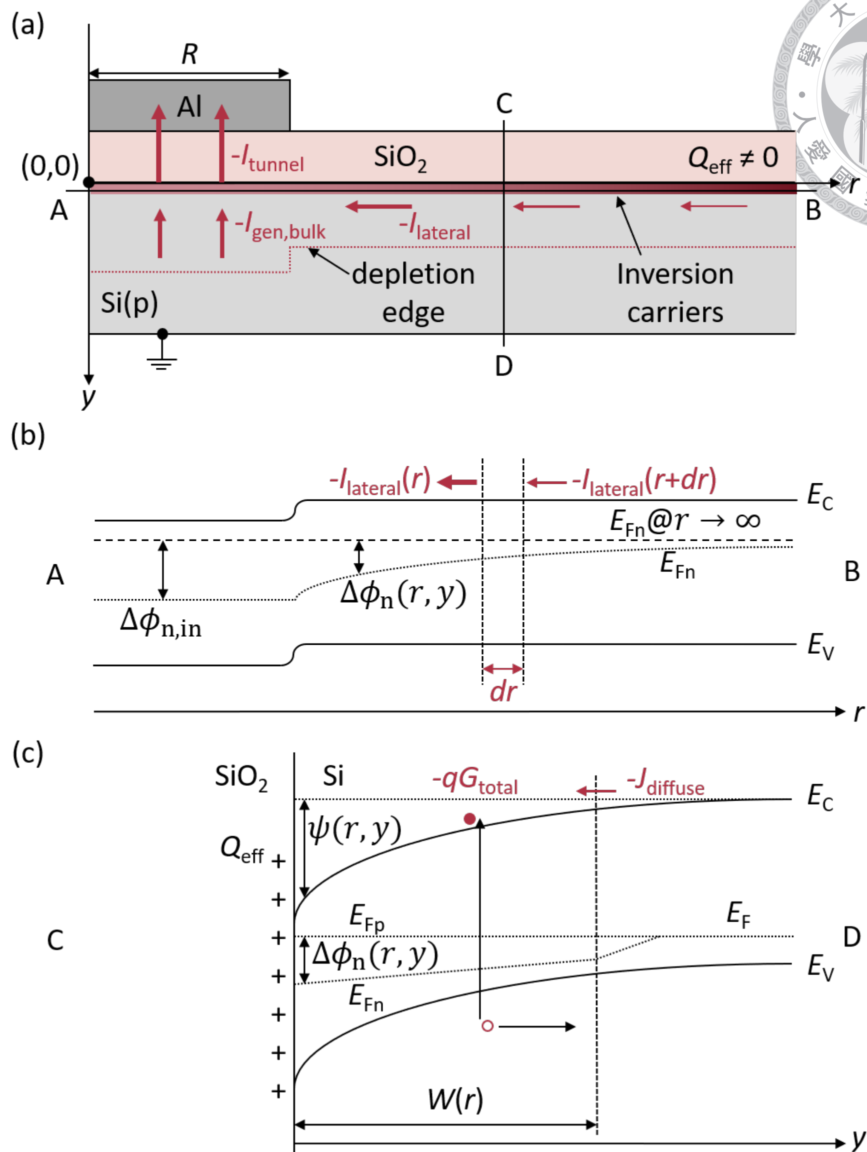

Figure A–1. (a) The cross-section of MISTD with coordinate (r, y). (b) and (c) are the band diagrams of the cut lines $\overline{AB}$ and $\overline{CD}$ in (a), respectively.

where E_{Fn} and E_{Fp} are electron and hole QFLs. Because of the lacking of electrons under the electrode, the oxide-charge-induced lateral coupling channel will supply the electrons from the region outside the electrode and also leads to QFL difference $\Delta\phi_n(r, y)$ outside the electrode. The band diagram containing $\Delta\phi_n(r, y)$ is plotted in **Figure A–1** (b). This band diagram is from the cut line $\overline{AB}$ in **Figure A–1** (a). From **Figure A–1** (b), two boundary

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conditions

$$\Delta\phi_{\mathrm{n}}(r = R, y) = \Delta\phi_{\mathrm{n,in}}, \tag{A.2}$$

and

$$\Delta\phi_{\mathrm{n}}(r \to \infty, y) = 0 \tag{A.3}$$

are assumed, where R is the radius of the electrode. The band diagram from cut line $\overline{\mathrm{CD}}$ in **Figure A−1** (a) is shown in **Figure A−1** (c). From **Figure A−1** (c), one can find a boundary condition of balancing between effective oxide charges Q_{eff} and charges in semiconductor Q_{s}. If Q_{eff} is mainly balanced by Q_{s} just below it, the equation of charge balancing under inversion can be written down as

$$Q_{\mathrm{eff}} = -Q_{\mathrm{s}} = -\int_0^{W(r)} -q\left[N_{\mathrm{a}} + \frac{n_{\mathrm{i}}^2}{N_{\mathrm{a}}} e^{q(\psi(r,y)-\Delta\phi_{\mathrm{n}}(r,y))/kT}\right] dy, \tag{A.4}$$

where $W(r)$ is the depletion width at radius r, N_{a} is the doping concentration, and n_{i} is the intrinsic carrier concentration of silicon. The boundary condition at $y \to \infty$ is assumed as,

$$\Delta\phi_{\mathrm{n}}(r, y \to \infty) = \psi(r, y \to \infty) = 0, \tag{A.5}$$

which can also be observed in **Figure A−1** (c). From the boundary conditions in eqs. (A.2) to (A.5), the profile of $\Delta\phi_{\mathrm{n}}(r, y)$ is able to be solved by considering the continuous equation

$$\frac{\partial n(r, y)}{\partial t} = 0 = \frac{1}{q}\nabla \cdot \mathbf{J}_{\mathrm{n}} + G(r, y), \tag{A.6}$$

where $n(r, y)$ is the electron concentration, $\mathbf{J}_{\mathrm{n}}$ is the electron current concentration, and $G(r, y)$ is the generation rate. However, it is challenging to get an analytical result without

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any further assumptions.

To reduce the modeling complexity, a few approximations discussed below are adopted. *Previous work proves that $\Delta\phi_n$ is almost a constant in the y direction inside the depletion region [53].* With the approximation, eq. (A.4) can be decoupled from y and reduce to

$$Q_{\text{eff}} = -Q_s \approx \sqrt{2\epsilon_{\text{si}} kTN_a}\left[\frac{q\psi_s(r)}{kT} + \frac{n_i^2}{N_a^2} e^{q(\psi_s(r)-\Delta\phi_n(r))/kT}\right]^{1/2}, \tag{A.7}$$

where $\psi_s(r)$ is surface band bending at r.

When the amount of Q_{eff} is not large enough to induce strong inversion outside the electrode, e.g., $N_a = 10^{16}\ \text{cm}^{-3}$, and $Q_{\text{eff}}/q \leq 3 \times 10^{11}\ \text{cm}^{-2}$, the second term in the brackets of eq. (A.7) can be neglected when calculating the value of $\psi_s(r, y)$. It is similar to the situation of subthreshold region in MOSFET. The simplified balancing equation of $Q_{\text{eff}} = -Q_s$ becomes

$$Q_{\text{eff}} = -Q_s \approx \sqrt{2\epsilon_{\text{si}} qN_a\psi_s}, \tag{A.8}$$

which is the well known space charge approximation. With space charge approximation, band bending ψ and depletion width W can be decoupled from r. The calculated ψ_s v.s. $\Delta\phi_n$ from eq. (A.7) is plotted in **Figure A–2** as solid lines, and the ψ_s calculated from eq. (A.8) is also attached as dash lines. As shown in **Figure A–2**, in the amount of Q_{eff}/q we are interested in ($\leq 3 \times 10^{11}\ \text{cm}^{-2}$), the deviation between eq. (A.7) and eq. (A.8) are less than 2 %. *Thus, we adopt space charge approximation in our modeling in this work.* By using space charge approximation, the band bending ψ can be represented as

$$\psi(y) = \psi_s\left(1 - \frac{y}{W}\right)^2 = \frac{Q_{\text{eff}}^2}{2\epsilon_{\text{si}} qN_a}\left(1 - \frac{y}{Q_{\text{eff}}/qN_a}\right)^2, \tag{A.9}$$

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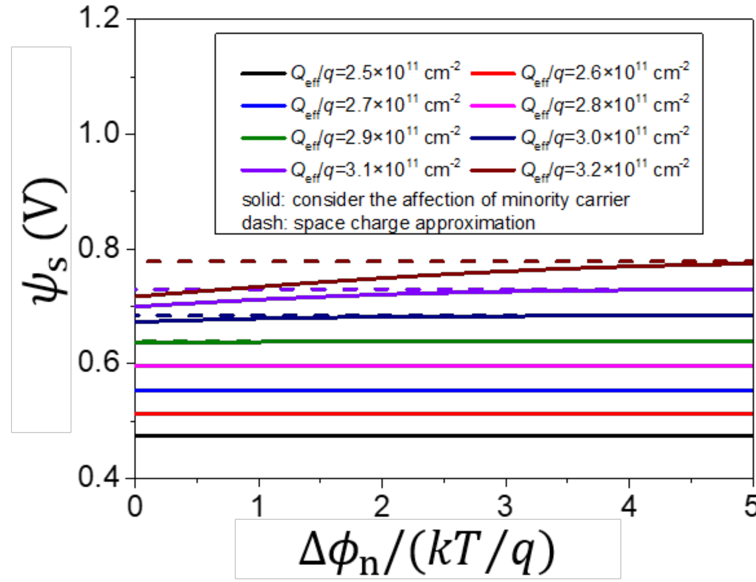

Figure A–2. ψ_s with and without considering the effect of minority carriers calculated from eqs. (A.7) and (A.8). Different amount of Q_{eff} is considered with substrate doping concentration of $N_a = 10^{16}$ cm^{-3}.

where $W = Q_{eff}/qN_a$ is depletion width from space charge approximation. With the simplified $\psi(y)$, we can analytically calculate the generated charges $-qG_{total}$ and diffusion current $-J_{diffuse}$ as mentioned in **Figure A–1** (c). It must be mentioned that both the electrons from generation and diffusion will laterally supply to the MISTD. For the Shockley-Read-Hall process, the generation rate can be expressed as [54, 55]

$$G = \frac{n_i^2(1 - e^{-q\Delta\phi_n/kT})}{\tau_{p0}(n + n_i) + \tau_{n0}(p + n_i)}, \tag{A.10}$$

where n and p are electron and hole concentrations, respectively, τ_{p0} and τ_{n0} are hole and

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electron lifetimes. n and p can be written as

$$n = \frac{n_i^2}{N_\mathrm{a}} e^{q(\psi - \Delta\phi_\mathrm{n})/kT}, \tag{A.11}$$

and

$$p = N_\mathrm{a} e^{-q\psi/kT}, \tag{A.12}$$

With Q_eff smaller than the threshold of inducing strong inversion, the electron concentration n can be neglected. It is also assumed that $\tau_\mathrm{n0} \approx \tau_\mathrm{p0} \approx \tau_0$. The generation rate can be simplified as

$$G \approx \frac{n_\mathrm{i}^2 (1 - e^{-q\Delta\phi_\mathrm{n}/kT})}{2\tau_0 n_\mathrm{i} + \tau_0 N_\mathrm{a} e^{-q\psi/kT}} = \frac{n_\mathrm{i}}{2\tau_0} \frac{1 - e^{-q\Delta\phi_\mathrm{n}/kT}}{1 + \frac{N_\mathrm{a}}{2n_\mathrm{i}} e^{-q\psi/kT}}. \tag{A.13}$$

The total generated charges per unit area $-qG_\mathrm{total}(r)$ at position r can be calculated from the below integration equation

$$-qG_\mathrm{total}(r) = -q \int_0^W \frac{n_\mathrm{i}}{2\tau_0} \frac{1 - e^{-q\Delta\phi_\mathrm{n}(r)/kT}}{1 + \frac{N_\mathrm{a}}{2n_\mathrm{i}} e^{-q\psi(y)/kT}} dy. \tag{A.14}$$

Insert eq. (A.9) into eq. (A.14), one can numerically calculate the qG_total v.s. $\Delta\phi_\mathrm{n}$. The results are shown in **Figure A–3** as solid lines for different Q_eff. By the way, the diffusion current $-J_\mathrm{diffuse}(r)$ can be calculated from the traditional equation of the diode's diffusion current [1]

$$-J_\mathrm{diffuse}(r) = -\frac{qD_\mathrm{n} n_\mathrm{i}^2}{L_\mathrm{n} N_\mathrm{a}} (1 - e^{-q\Delta\phi_\mathrm{n}(r)/kT}), \tag{A.15}$$

where D_n is diffusion coefficient for electron, and L_n is diffusion length for electron. J_diffuse v.s. $\Delta\phi_\mathrm{n}$ is attached in **Figure A–3** as dash lines. We can find that qG_total is larger than J_diffuse for about two orders in a wide range of $\Delta\phi_\mathrm{n}$. *Thus, we neglect the diffusion current*

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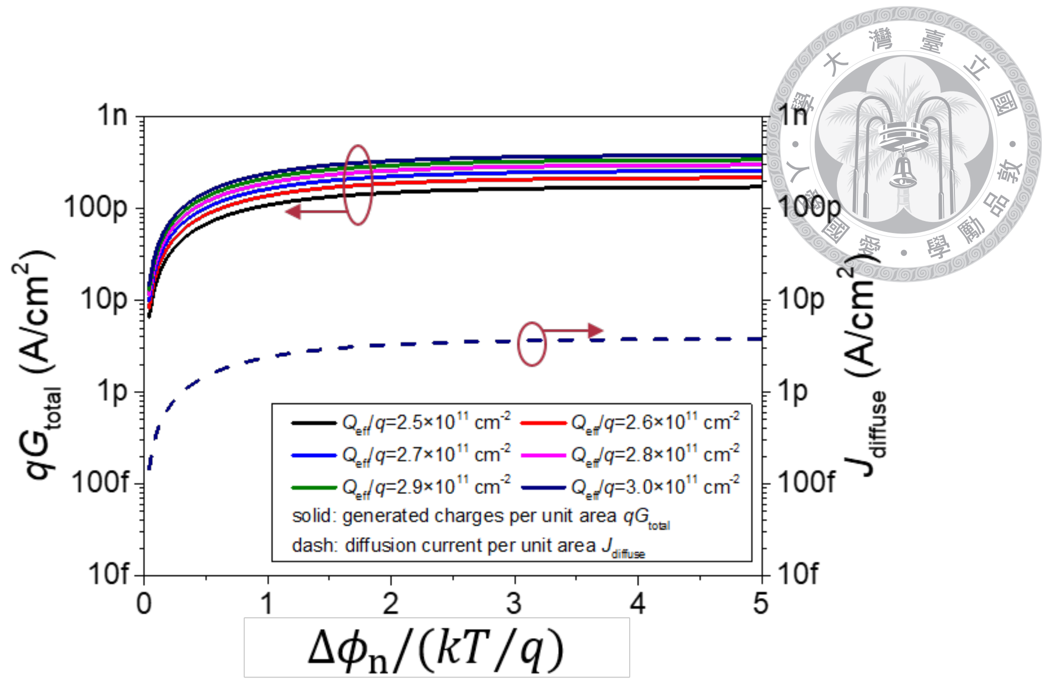

Figure A–3. Generated charges per unit area qG_{total} and diffusion current concentration J_{diffuse} calculated from eqs. (A.14) and (A.15) under different Q_{eff} and $\Delta\phi_{\text{n}}$.

from the substrate in our modeling. With this approximation, we only need to solve the problem inside the depletion region.

In this section, we have made four major approximations to simplify the model. The four approximations are summarized as follows:

- Assume $\Delta\phi_{\text{n}}$ is independent of y [53] but dependent on r.
- Focus on the situation with Q_{eff} not large enough to induce strong inversion outside the electrode.
- Use space charge approximation and decouple ψ and W from r.
- Neglect the diffusion current from the substrate.

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A.2 Derivation of Oxide-Charge-Induced Lateral Coupling Length

From the approximations mentioned in the previous section, the interesting region limited to the rectangle EFGH in **Figure A−4**. The boundary conditions of this region are:

$$\psi(y=0) = \psi_s \approx \frac{Q_{\text{eff}}^2}{2\epsilon_{\text{si}} q N_{\text{a}}}, \tag{A.16}$$

$$\psi(y=W) = 0, \tag{A.17}$$

$$\Delta\phi_{\text{n}}(r=R) = \Delta\phi_{\text{n0}}, \tag{A.18}$$

and

$$\Delta\phi_{\text{n}}(r \to \infty) = 0. \tag{A.19}$$

The problem is that there are two one-dimensional equations, $\Delta\phi_{\text{n}}(r)$ and $\psi(y)$, overlapped in a two-dimensional coordinate. According to the space charge approximation, $\psi(y)$ is known as expressed in eq. (A.9). Solving $\Delta\phi_{\text{n}}(r)$ is the only remaining parameter to solve in our modeling.

The electron flow $-I_{\text{lateral}}(r)$ in **Figure A−1** (b) can be written down as

$$\begin{aligned} -I_{\text{lateral}}(r) &= 2\pi r \int_0^W q\mu_{\text{n}} n(r,y) \frac{d\Delta\phi_{\text{n}}(r)}{dr} dy \\ &= 2\pi r \int_0^W q\mu_{\text{n}} \frac{n_{\text{i}}^2}{N_{\text{a}}} e^{q(\psi(y)-\Delta\phi_{\text{n}}(r))/kT} \frac{d\Delta\phi_{\text{n}}(r)}{dr} dy \\ &= \frac{2\pi q\mu_{\text{n}} n_{\text{i}}^2}{N_{\text{a}}} \left[\int_0^W e^{q\psi(y)/kT} dy \right] r \frac{d\Delta\phi_{\text{n}}(r)}{dr} e^{-q\Delta\phi_{\text{n}}(r)/kT}. \end{aligned} \tag{A.20}$$

The difference in electron flow $-I_{\text{lateral}}(r)$ and $-I_{\text{lateral}}(r+dr)$ in **Figure A−1** (b) is mainly

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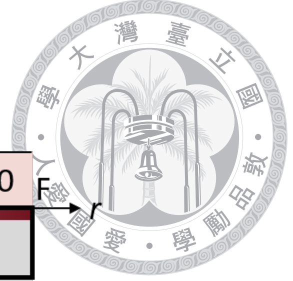

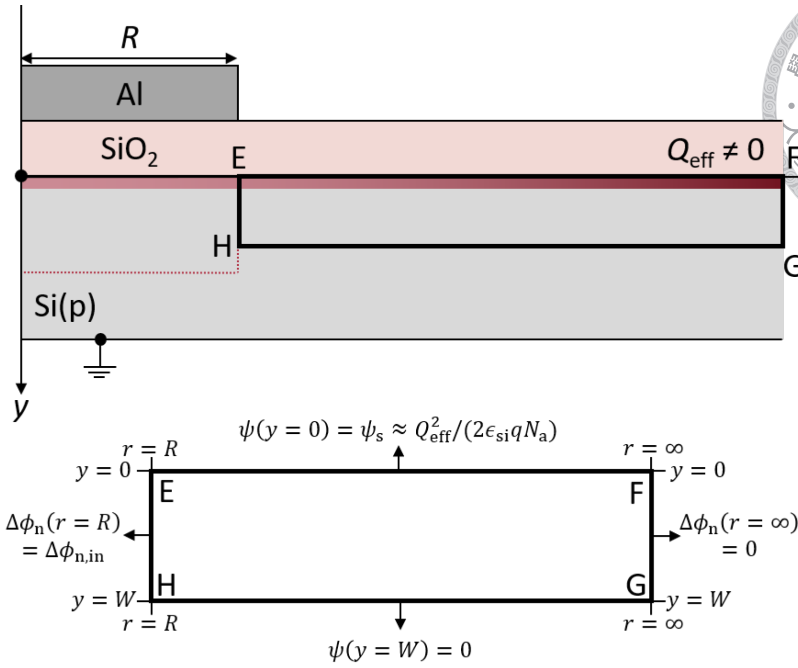

Figure A–4. The region and boundary conditions after making the approximations. It is used for the derivation of oxide-charge-induced lateral coupling length.

caused by the generated charges inside the dr region. By applying $-qG_{\mathrm{total}}$ in eq. (A.14), one can write down

$$
\begin{aligned}
[-I_{\mathrm{lateral}}(r)] - [-I_{\mathrm{lateral}}(r+dr)] &= -2\pi r\, dr\, q G_{\mathrm{total}} \\
&= -2\pi r\, dr\, q \int_0^W \frac{n_{\mathrm{i}}}{2\tau_0} \frac{1 - e^{-q\Delta\phi_{\mathrm{n}}(r)/kT}}{1 + \frac{N_{\mathrm{a}}}{2n_{\mathrm{i}}} e^{-q\psi(y)/kT}} dy \\
&= -\frac{2\pi q n_{\mathrm{i}}}{2\tau_0} \left[\int_0^W \frac{dy}{1 + \frac{N_{\mathrm{a}}}{2n_{\mathrm{i}}} e^{-q\psi(y)/kT}} \right] r \left(1 - e^{-q\Delta\phi_{\mathrm{n}}(r)/kT}\right) dr.
\end{aligned}
\tag{A.21}
$$

Eq. (A.21) can be rearranged as

$$
\frac{dI_{\mathrm{lateral}}(r)}{dr} = -\frac{2\pi q n_{\mathrm{i}}}{2\tau_0} \left[\int_0^W \frac{dy}{1 + \frac{N_{\mathrm{a}}}{2n_{\mathrm{i}}} e^{-q\psi(y)/kT}} \right] r \left(1 - e^{-q\Delta\phi_{\mathrm{n}}(r)/kT}\right). \tag{A.22}
$$

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Before solving eq. (A.22), we define

$$u = 1 - e^{-q\Delta\phi_{\mathrm{n}}(r)/kT}, \tag{A.23}$$

and

$$du/dr = \frac{q}{kT}\frac{d\Delta\phi_{\mathrm{n}}(r)}{dr}e^{-q\Delta\phi_{\mathrm{n}}(r)/kT} \tag{A.24}$$

to reduce eq. (A.22) to a linear differential equation. By substituting the term u, eq. (A.20) can be rewritten as

$$-I_{\mathrm{lateral}}(r) = \frac{2\pi kT\mu_{\mathrm{n}}n_{\mathrm{i}}^2}{N_{\mathrm{a}}}\left[\int_0^W e^{q\psi(y)/kT}dy\right]r\frac{du}{dr}. \tag{A.25}$$

Insert eqs. (A.23) and (A.25) into eq. (A.22) one can get

$$-\frac{2\pi kT\mu_{\mathrm{n}}n_{\mathrm{i}}^2}{N_{\mathrm{a}}}\left[\int_0^W e^{q\psi(y)/kT}dy\right]\left[r\frac{d^2u}{dr^2}+\frac{du}{dr}\right] = -\frac{2\pi qn_{\mathrm{i}}}{2\tau_0}\left[\int_0^W \frac{dy}{1+\frac{N_{\mathrm{a}}}{2n_{\mathrm{i}}}e^{-q\psi(y)/kT}}\right]ru. \tag{A.26}$$

Eq. (A.26) can further be rearranged as

$$r^2\frac{d^2u}{dr^2}+r\frac{du}{dr}-\left[\frac{qN_{\mathrm{a}}}{2\tau_0 kT\mu_{\mathrm{n}}n_{\mathrm{i}}}\frac{\int_0^W \frac{dy}{1+\frac{N_{\mathrm{a}}}{2n_{\mathrm{i}}}e^{-q\psi(y)/kT}}}{\int_0^W e^{q\psi(y)/kT}dy}\right]r^2u = 0. \tag{A.27}$$

Let

$$\alpha = \left[\frac{qN_{\mathrm{a}}}{2\tau_0 kT\mu_{\mathrm{n}}n_{\mathrm{i}}}\frac{\int_0^W \frac{dy}{1+\frac{N_{\mathrm{a}}}{2n_{\mathrm{i}}}e^{-q\psi(y)/kT}}}{\int_0^W e^{q\psi(y)/kT}dy}\right]^{1/2}, \tag{A.28}$$

and rewrite eq. (A.27) as

$$r^2\frac{d^2u}{dr^2}+r\frac{du}{dr}-\alpha^2r^2u = 0. \tag{A.29}$$

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This is a typical form of modified Bessel's differential equation. The term u can be solved as

$$u(r) = 1 - e^{-q\Delta\phi_{\mathrm{n}}(r)/kT} = CK_0(\alpha r), \tag{A.30}$$

where C is a constant. For boundary condition maching

$$u(R) = 1 - e^{-q\Delta\phi_{\mathrm{n,in}}/kT} = CK_0(\alpha R), \tag{A.31}$$

and K_0 is modified Bessel functions of the second kind with orders 0. Finally, we get

$$u(r) = 1 - e^{-q\Delta\phi_{\mathrm{n}}(r)/kT} = \frac{1 - e^{-q\Delta\phi_{\mathrm{n,in}}/kT}}{K_0(\alpha R)} K_0(\alpha r). \tag{A.32}$$

The term $1 - e^{-q\Delta\phi_{\mathrm{n}}(r)/kT}$ is highly related to the generation rate in the lateral region. Thus, we define oxide-charge-induced lateral coupling Length Λ as

$$\Lambda = \alpha^{-1} = \left[\frac{qN_{\mathrm{a}}}{2\tau_0 kT \mu_{\mathrm{n}} n_{\mathrm{i}}} \frac{\int_0^W \frac{dy}{1+\frac{N_{\mathrm{a}}}{2n_{\mathrm{i}}} e^{-q\psi(y)/kT}}}{\int_0^W e^{q\psi(y)/kT} dy} \right]^{-1/2}. \tag{A.33}$$

The variables in eq. (A.33) are all known for a specific device. It is noticed that the effect of effective oxide charges is included in $\psi(y)$ according to eq. (A.9).

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Appendix B

Modified Schottky Diode Current Equation with the Consideration of Oxide Barrier

In the derivation current, we focus on the role of hole, but not electron. However, the result can also be applied to the derivation of electron current of MISTD. **Figure B−1** (a) and (b) show detailed band diagrams with positive and negative hole barrier $q\phi_b$, respectively. We define x as the direction normal to the interface of the materials. Hole energy in x direction E_{hx} is also defined. Because we are considering the hole injection from metal, hole carriers' energy increases toward the lower part of the band diagram. From **Figure B−1** , one can write down the equation of hole injection current I_h as

$$I_h = qA \int_{E_{hx} > E_{Fm} + q\phi_b} v_{hx} P_{th}(E_{hx}) N(E_h) f_h(E_h) dE_h, \qquad \text{(B.1)}$$

where A is the device area, E_{Fm} is the Fermi-level in metal, $q\phi_b$ is the barrier height seen by the holes in metal, v_{hx} is the hole velocity in x direction, $P_{th}(E_{hx})$ is hole tunneling probability depending on E_{hx}, E_h is the hole energy, $N(E_h)$ is hole density of state depending on E_h, and $f_h(E_h)$ is hole filling rate depending on E_h. The equation is similar to

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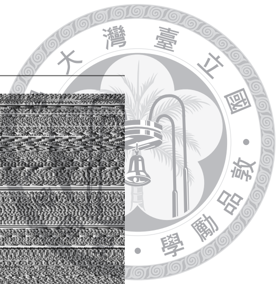

Figure B–1. Detailed band diagram at (a) $V_{\mathrm{ox}} < 1$ V and (b) $V_{\mathrm{ox}} > 1$ V. The hole barrier height, hole energy, and the direction x for thermal emission from metal to silicon are also labeled.

the traditional Schottky diode current equation [75] but different in two parts:

- Tunneling probability $P_{\mathrm{th}}(E_{\mathrm{hx}})$ is considered because of the existence of an oxide

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barrier.

- Full Fermi-Dirac distribution $f_{\mathrm{h}}(E_{\mathrm{h}})$ is adopted to replace Boltzmann approximation because the hole barrier will be modulated from a positive to a negative value with the increasing oxide voltage V_{ox}.

In eq. (B.1), some terms of v_{hx} and E_{hx} are related to x, which is perpendicular to the materials' interface. Thus, we consider holes are freely moving in the metal as shown in **Figure B−2** (a) and define an orthogonal xyz coordinate system to describe the velocity direction of the carriers. In this coordinate system, the x direction is normal to the interface of materials, the same as the definition in **Figure B−1** . The allowable states can be transferred into velocity space, as shown in **Figure B−2** (b) [76]. The distance between allowable states is h/m [76],where h is the Planck constant, and m is the carrier's effective mass. In **Figure B−2** (b), hole velocities in x, y, and z are defined as v_{hx}, v_{hy}, and v_{hz}. The total velocity and energy of the hole can be written down as

$$v_{\mathrm{h}} = (v_{\mathrm{hx}}^2 + v_{\mathrm{hy}}^2 + v_{\mathrm{hz}}^2)^{1/2}, \tag{B.2}$$

and

$$E_{\mathrm{h}} = \frac{1}{2} m v_{\mathrm{h}}^2 = \frac{1}{2} m (v_{\mathrm{hx}}^2 + v_{\mathrm{hy}}^2 + v_{\mathrm{hz}}^2). \tag{B.3}$$

As shown in **Figure B−2** , for v_{h} smaller than Fermi velocity v_{F}, the states are filled mainly by the hole. However, for v_{h} larger than v_{F}, electrons occupy most states. Holes inject from metal should have

$$E_{\mathrm{hx}} = \frac{1}{2} m v_{\mathrm{hx}}^2 > E_{\mathrm{Fm}} + q\phi_{\mathrm{b}}. \tag{B.4}$$

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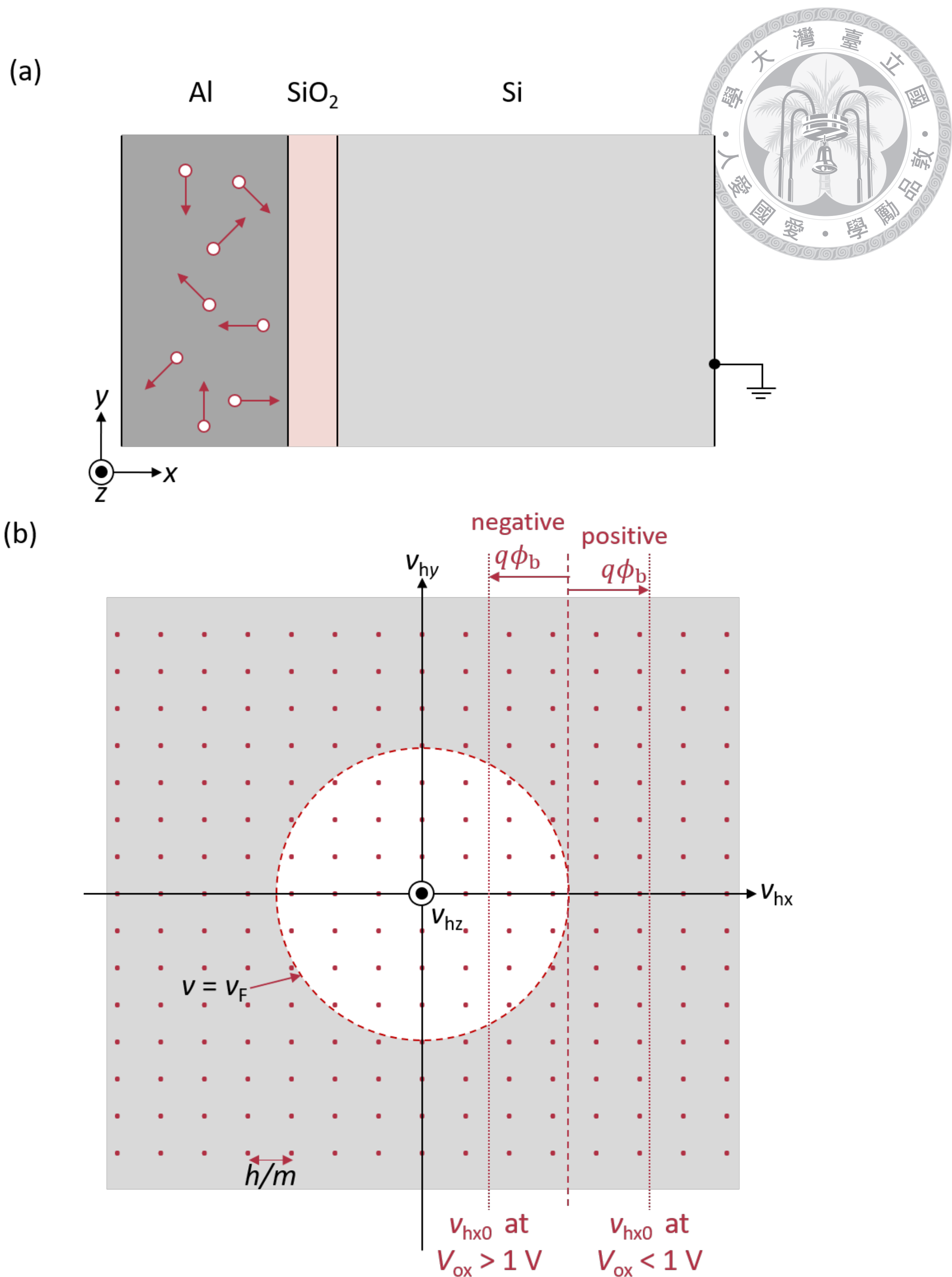

Figure B–2. (a) Definition of the orthogonal xyz coordinate system. It is assumed that holes inside the metal are freely moving in three-dimensional space. (b) The allowable states in velocity space. v_{hx0} for the case of $V_{\mathrm{ox}} < 1$ V and $V_{\mathrm{ox}} > 1$ V are also labeled.

We define

$$\frac{1}{2}mv_{\mathrm{hx0}}^2 = E_{\mathrm{Fm}} + q\phi_{\mathrm{b}}, \tag{B.5}$$

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where v_{hx0} is the velocity just large enough to thermally emit into silicon. Thus, we need to integrate the range of $v_{\mathrm{hx}} > v_{\mathrm{hx0}}$ in the velocity space. v_{hx0} at V_{ox} smaller and large than 1 V, which correspond to **Figure B−1** (a) and **Figure B−1** (b), are labeled in **Figure B−2** (b). For $V_{\mathrm{ox}} > 1$ V or $q\phi_{\mathrm{b}} < 0$, v_{F} becomes larger than v_{hx0}, and a great number of holes are included in the integration region. Considering the velocity space in **Figure B−2** (b) and the definition in eq. (B.5), one can rewrite eq. (B.1) as

$$I_{\mathrm{h}} = qA \int_{v_{\mathrm{hx0}}}^{+\infty} \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} v_{\mathrm{hx}} P_{\mathrm{th}}(E_{\mathrm{hx}}) 2(\frac{m}{h})^3 f_{\mathrm{h}}(E_{\mathrm{h}}) dv_{\mathrm{hy}} dv_{\mathrm{hz}} dv_{\mathrm{hx}}, \tag{B.6}$$

where $(m/h)^3$ is the density of states in velocity space, 2 indicates that two electrons in different spin are allowable in one state, and $f_{\mathrm{h}}(E_{\mathrm{h}})$ can be written as

$$f_{\mathrm{h}}(E_{\mathrm{h}}) = \frac{1}{1 + e^{(E_{\mathrm{h}} - E_{\mathrm{Fm}})/kT}} = \frac{1}{1 + e^{[\frac{1}{2}m(v_{\mathrm{hx}}^2 + v_{\mathrm{hy}}^2 + v_{\mathrm{hz}}^2) - E_{\mathrm{Fm}}]/kT}}. \tag{B.7}$$

Insert eq. (B.7) into eq. (B.6) one can get:

$$\begin{aligned} I_{\mathrm{h}} &= \frac{2qAm^3}{h^3} \int_{v_{\mathrm{hx0}}}^{+\infty} \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} \frac{v_{\mathrm{hx}} P_{\mathrm{th}}(E_{\mathrm{hx}})}{1 + e^{[\frac{1}{2}m(v_{\mathrm{hx}}^2 + v_{\mathrm{hy}}^2 + v_{\mathrm{hz}}^2) - E_{\mathrm{Fm}}]/kT}} dv_{\mathrm{hy}} dv_{\mathrm{hz}} dv_{\mathrm{hx}} \\ &= \frac{2qAm^3}{h^3} \int_{v_{\mathrm{hx0}}}^{+\infty} v_{\mathrm{hx}} P_{\mathrm{th}}(E_{\mathrm{hx}}) \left[\int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} \frac{dv_{\mathrm{hy}} dv_{\mathrm{hz}}}{1 + e^{[\frac{1}{2}m(v_{\mathrm{hx}}^2 + v_{\mathrm{hy}}^2 + v_{\mathrm{hz}}^2) - E_{\mathrm{Fm}}]/kT}} \right] dv_{\mathrm{hx}}. \end{aligned} \tag{B.8}$$

We define the term inside the big brackets as

$$U = \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} \frac{dv_{\mathrm{hy}} dv_{\mathrm{hz}}}{1 + e^{[\frac{1}{2}m(v_{\mathrm{hx}}^2 + v_{\mathrm{hy}}^2 + v_{\mathrm{hz}}^2) - E_{\mathrm{Fm}}]/kT}}. \tag{B.9}$$

To integrate U, one can transfer the $(v_{\mathrm{hy}}, v_{\mathrm{hz}})$ coordinate into (r, θ) system and rewrite eq.

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(B.9) as

$$U = \int_0^{2\pi} \int_0^{+\infty} \frac{r dr d\theta}{1 + e^{[\frac{1}{2}m(v_{\mathrm{hx}}^2 + r^2) - E_{\mathrm{Fm}}]/kT}}. \tag{B.10}$$

After integrating by suitable substituting (e.g., let substitution term as $1+e^{[\frac{1}{2}m(v_{\mathrm{hx}}^2+r^2)-E_{\mathrm{Fm}}]/kT}$.), U can be calculated as

$$U = \frac{2\pi kT}{m} \ln(1 + e^{-(\frac{1}{2}mv_{\mathrm{hx}}^2 - E_{\mathrm{Fm}})/kT}). \tag{B.11}$$

One can substitute eq. (B.11) into eq. (B.8) to get

$$I_{\mathrm{h}} = \frac{4\pi qkTAm^2}{h^3} \int_{v_{\mathrm{hx0}}}^{+\infty} v_{\mathrm{hx}} P_{\mathrm{th}}(E_{\mathrm{hx}}) \ln(1 + e^{-(\frac{1}{2}mv_{\mathrm{hx}}^2 - E_{\mathrm{Fm}})/kT}) dv_{\mathrm{hx}}. \tag{B.12}$$

Finally, we define

$$E' = \frac{1}{2}mv_{\mathrm{hx}}^2 - E_{\mathrm{Fm}}, \tag{B.13}$$

and insert it to eq. (B.12) to get

$$I_{\mathrm{h}} = \frac{4\pi qkTAm}{h^3} \int_{q\phi_{\mathrm{b}}}^{+\infty} P_{\mathrm{th}}(E') \ln(1 + e^{-E'/kT}) dE'. \tag{B.14}$$

We named eq. (B.14) as “modified Schottky diode current equation”, which considers the effect of Schottky barrier height modulation and the existence of an oxide barrier.

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Appendix C

Lateral Coupling Capacitance Induced by Existing Oxide Charges

A Detailed schematic diagram and the equivalent circuit of a circle device are plotted in **Figure C−1**. From the equivalent circuit in **Figure C−1**, one can write down two coupled differential equations

$$i(r,t) = [v(r-dr,t) - v(r,t)]dG_{\mathrm{L}}(r) = -\frac{2\pi r}{R_{\mathrm{s}}}\frac{\partial v(r,t)}{\partial r}, \tag{C.1}$$

and

$$\frac{\partial v(r,t)}{\partial t} = \frac{[i(r,t) - i(r+dr,t)]}{dC_{\mathrm{L}}(r)} = -\frac{1}{2\pi r C_{\mathrm{d,out}}}\frac{\partial i(r,t)}{\partial r}. \tag{C.2}$$

It is assumed that the solution to $i(r,t)$ and $v(r,t)$ can be performed by phasor form as

$$i(r,t) = i_{\mathrm{r}}(r)e^{j\omega t}, \tag{C.3}$$

and

$$v(r,t) = v_{\mathrm{r}}(r)e^{j\omega t}, \tag{C.4}$$

where ω is the angular frequency, $i_{\mathrm{r}}(r)$ and $v_{\mathrm{r}}(r)$ are current and voltage amplitudes of

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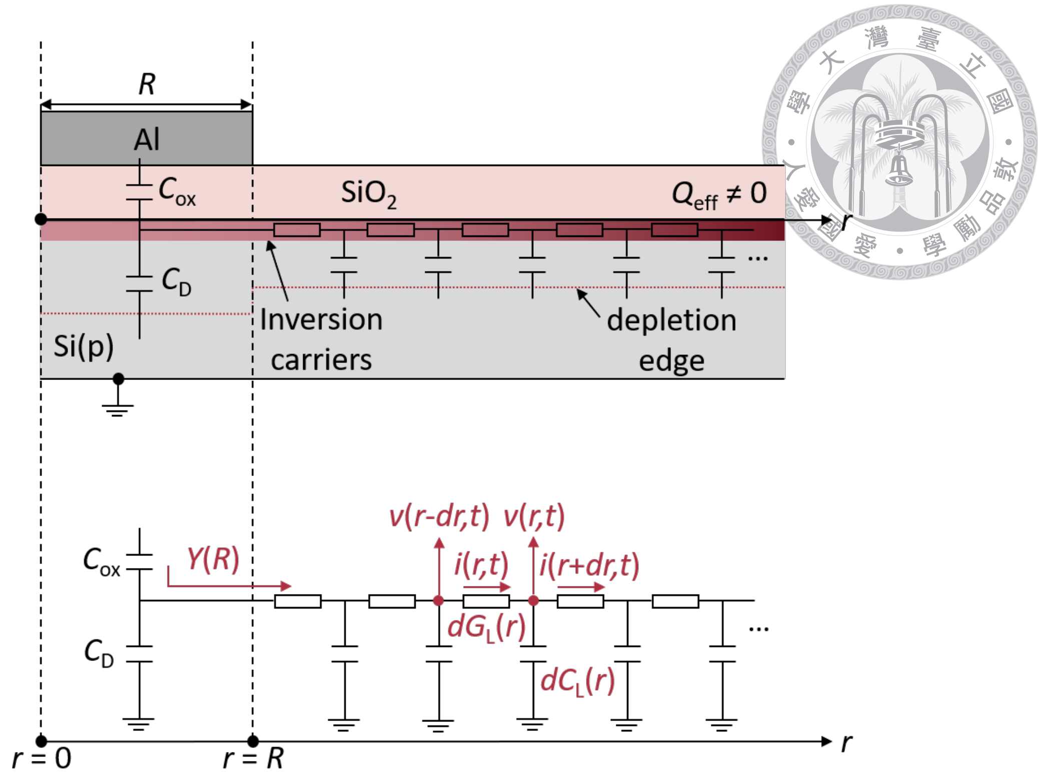

Figure C–1. The detailed schematic and equivalent circuit for lateral coupling. The radial coordinate with the origin at the center of the device is also attached.

AC signal depending on r. By inserting eq. (C.3) and (C.4) into eq. (C.1) and (C.2), one can get a differential equation:

$$r^2 v_\mathrm{r}''(r) + r v_\mathrm{r}'(r) - j\omega C_\mathrm{d,out} R_\mathrm{s} r^2 v_\mathrm{r}(r) = 0, \tag{C.5}$$

which is a typical form of the modified Bessel equation. The solution of $v_\mathrm{r}(r)$ can be solved as

$$v_\mathrm{r}(r) = C_1 K_0 (j^{\frac{1}{2}} r \sqrt{\omega C_\mathrm{d,out} R_\mathrm{s}}), \tag{C.6}$$

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where C_1 is a constant, and K_0 is the modified Bessel function of the second kind with orders 0. By inserting eq. (C.6) into eq. (C.1), one can get $i_\mathrm{r}(r)$ as

$$i_\mathrm{r}(r) = C_1 2\pi r \sqrt{\frac{\omega C_\mathrm{d,out}}{R_\mathrm{s}}} K_1(j^{\frac{1}{2}} r \sqrt{\omega C_\mathrm{d,out} R_\mathrm{s}}) j^{\frac{1}{2}}, \tag{C.7}$$

where K_1 is the modified Bessel function of the second kind with orders 1. With multiplying the phasor part $e^{j\omega t}$, $v(r,t)$ and $i(r,t)$ can be expressed as

$$v(r) = C_1 K_0(j^{\frac{1}{2}} r \sqrt{\omega C_\mathrm{d,out} R_\mathrm{s}}) e^{j\omega t},\ r \geq R, \tag{C.8}$$

and

$$i(r) = C_1 2\pi r \sqrt{\frac{\omega C_\mathrm{d,out}}{R_\mathrm{s}}} K_1(j^{\frac{1}{2}} r \sqrt{\omega C_\mathrm{d,out} R_\mathrm{s}}) j^{\frac{1}{2}} e^{j\omega t},\ r \geq R, \tag{C.9}$$

where R is the radius of the device. Eqs. (C.8) and (C.9) are only valid outside the electrode $r > R$ because it is assumed that the silicon surface AC signal inside the electrode is fully controlled by the voltage applied to the metal. As plotted in **Figure C–1**, one needs to calculate admittance seen at the device edge $Y(r = R)$. $Y(r = R)$ can be written down as

$$Y(r = R) = \frac{i(r = R)}{v(r = R)} = 2\pi R \sqrt{\frac{\omega C_\mathrm{d,out}}{R_\mathrm{s}}} \frac{K_1(j^{\frac{1}{2}} R \sqrt{\omega C_\mathrm{d,out} R_\mathrm{s}})}{K_0(j^{\frac{1}{2}} R \sqrt{\omega C_\mathrm{d,out} R_\mathrm{s}})} j^{\frac{1}{2}}. \tag{C.10}$$

Eq. (C.10) includes the capacitance and conductance value contributed from the lateral region.

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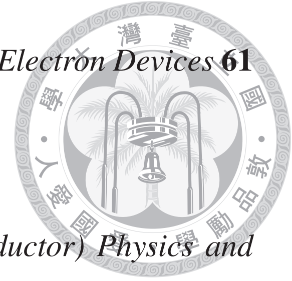

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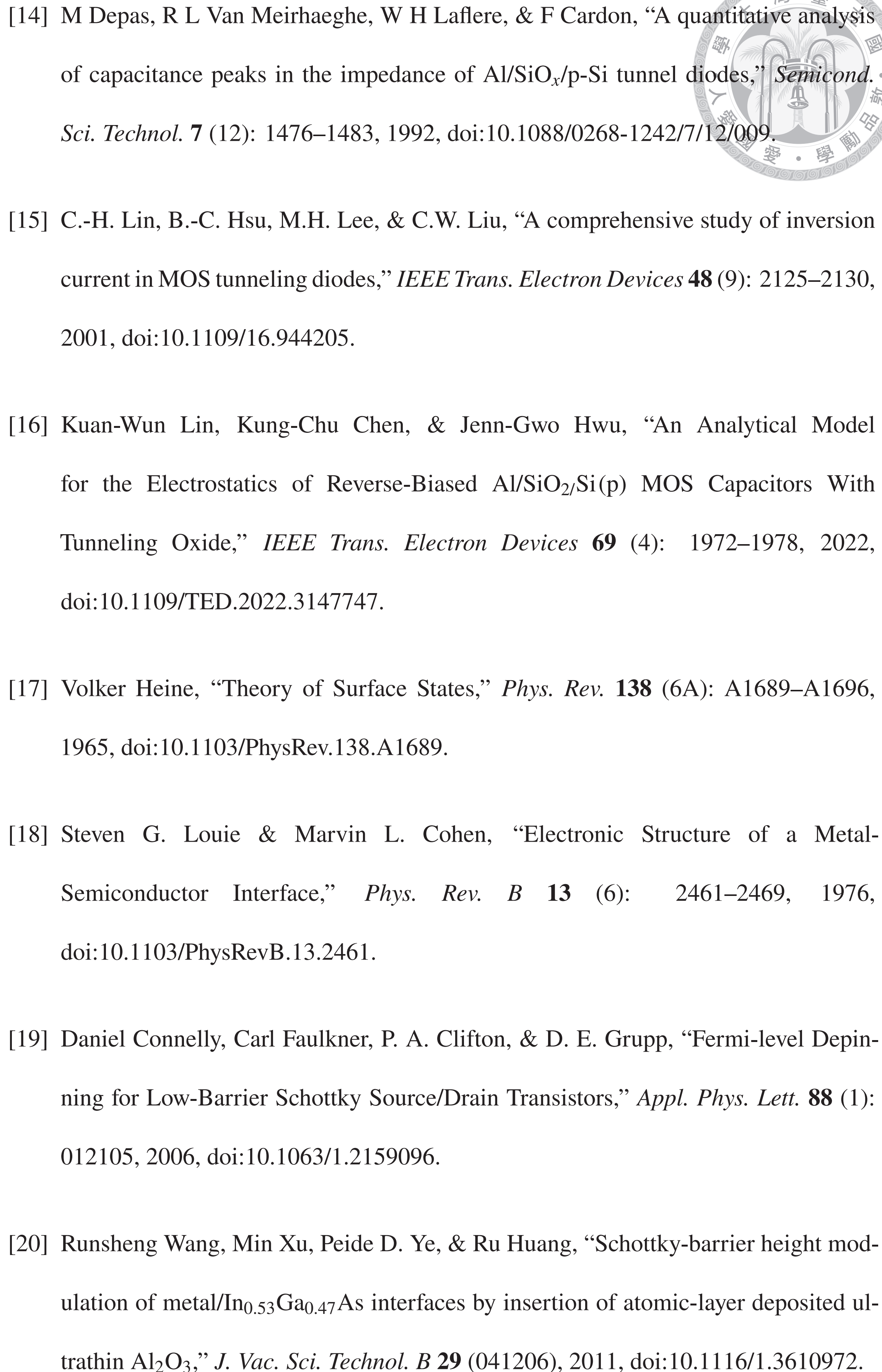

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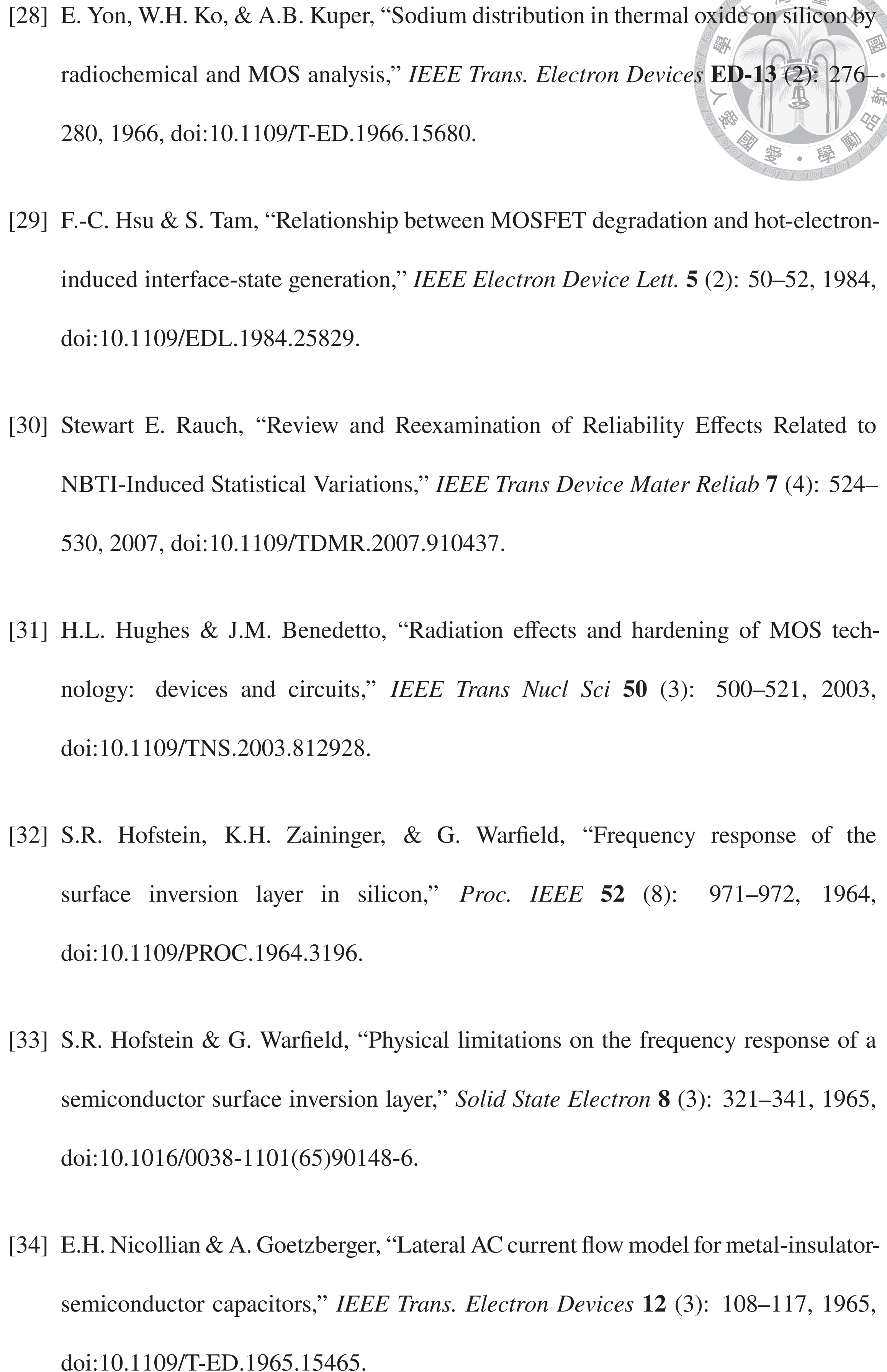

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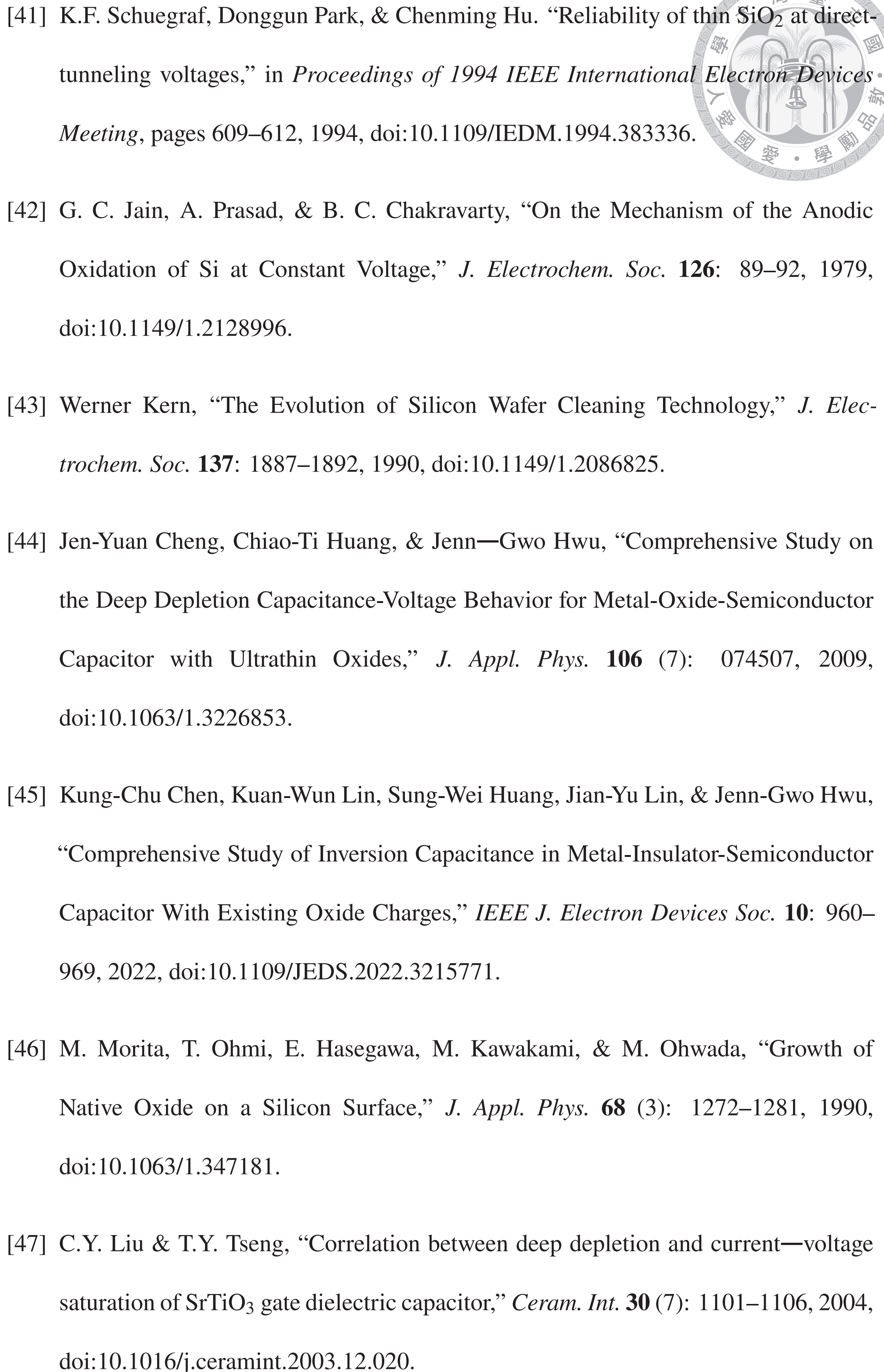

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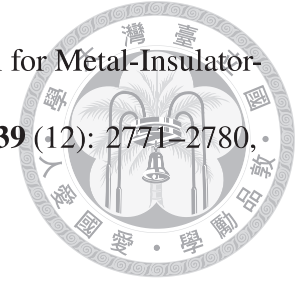

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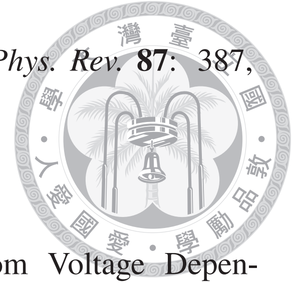

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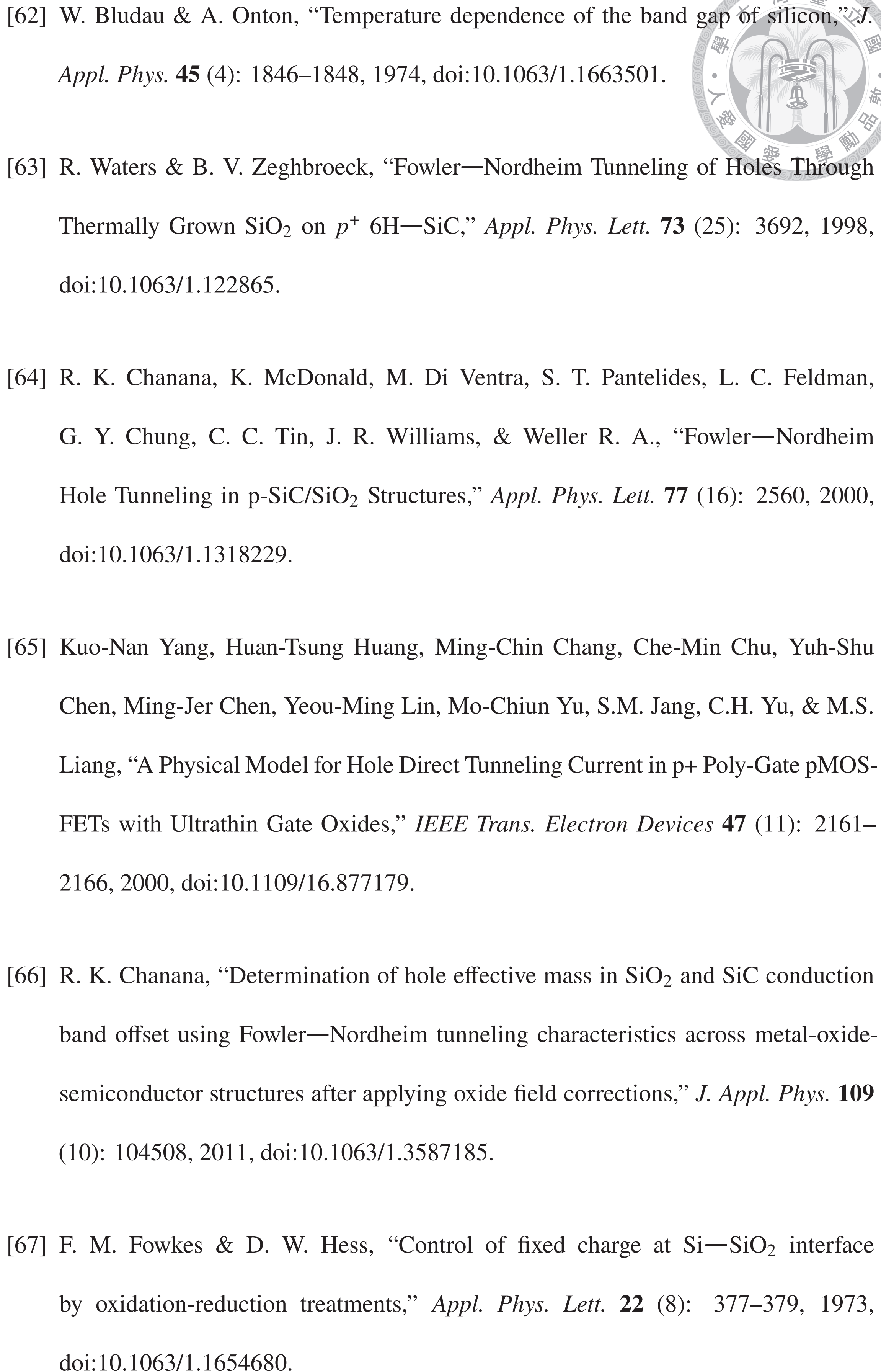

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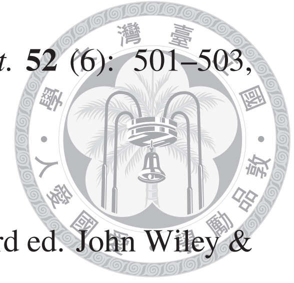

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