國立臺灣大學電機資訊學院電子工程學研究所

博士論文

Graduate Institute of Electronics Engineering
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Doctoral Dissertation

在低功耗無線感測應用中弛張振盪器的運用法

Utilization of Relaxation Oscillators in Low-Power Wireless Sensing Applications

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在低功耗無線感測應用中弛張振盪器的運用法
Utilization of Relaxation Oscillators in Low-Power Wireless Sensing Applications

本論文係蔡渝楷君（F98943004）在國立臺灣大學電子工程學研究所完成之博士學位論文，於民國 107 年 1 月 16 日承下列考試委員審查通過及口試及格，特此證明

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Utilization of Relaxation Oscillators in Low-Power Wireless Sensing Applications

By

Yu-Kai Tsai

Dissertation

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摘要

近年來自動化生產以及物聯網相關的應用在業界與學界掀起了一陣旋風，為了實現這些功能，大量的感測器端點扮演了不可或缺的角色。為了減少端點之間的連結的困難，勢必得利用無線傳輸進行端點間的溝通或資料的傳輸。這些端點通常會使用電池或是從外界環境進行能量擷取，而如何降低端點功耗來延長電池壽命或增加能量擷取的效率便成了一個重要的課題。一般來說，無線收發端需要消耗較多的能量，然而可以靠縮短其工作周期減低其平均消耗功率。此時，在感測器端點內持續操作不間斷的電路消耗了大部分的能量，在本論文中，挑選了其中兩種電路：時脈產生器與感測器介面電路在 90 奈米互補式金氧半製程使用具備效率優勢的弛張振盪器進行實做。

首先，對於一個做為時脈產生器的弛張振盪器，其比較器隨著溫度變化的延遲時間是實現一個高頻率對溫度穩定度的最大難題。本論文提出了一個累積誤差迴授技巧搭配上組合溫度係數相反的電阻，成功實現出一振盪頻率為 51.3 MHz，等效溫度係數為 21.8 ppm/°C 且溫度操作範圍為-20°C 至 100°C 的弛張振盪器。此振盪器當供應電壓由 0.8 V 變化至 1.2 V 時相對應的頻率變化為±0.53 %。

本論文接下來將基於振盪器架構實現的時間模式積分微分調變電容數位轉換器依據其數位輸出與振盪器的周期或是頻率成正比來簡單區分為周期型與頻率型。首先闡述了周期型架構的操作原理與雜訊來源的數學分析，並藉由一個循序搜尋頻率校準電路來解決振盪器頻率隨製程變異飄移的問題，成功實現一個等效解析度為 8.8 位元，品質因數為 1.16 pJ/c.-s.的電容數位轉換器。同時也實做了頻率型電容數位轉換器用以比較，藉由分析非線性誤差產生的來源，本論文提出了一個非線性誤差補償技巧。此頻率型電容數位轉換器等效解析度為 7.9 位元，品質因數為 10.6 pJ/c.-s.。最後則提出了對於上述電路實做之心得以及比較作為結論。

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Abstract

As the dramatically increase of the number of sensor nodes in the future wireless sensor network for Internet of things or factory automation, lowering the power consumption of each sensor node becomes an important issue. In this thesis, two essential blocks of a typical wireless sensor node are chosen and realized with energy-efficient relaxation oscillators in a 90-nm general-purpose CMOS process. To begin with, a 51.3-MHz CMOS relaxation oscillator is implemented. By pointing out the main challenge of achieving high frequency stability versus temperature is the delay time variation of the comparator, an integrated error feedback (IEF) is proposed to conquer the challenge. Due to the use of the proposed IEF technique and composite resistors, the fabricated circuit demonstrates an average frequency drift of 21.8 ppm/°C for a temperature range from -20 to 100°C. As the supply voltage changes from 0.8 to 1.2 V, the frequency variation is ±0.53%. It is well suited for emerging applications where low-power operations are required. Then, a period-mode oscillator-based capacitance-to-digital converter (CDCs) is implemented. With the help of the comprehensive analysis of the noise contribution and the sequential search frequency calibration (SSFC), the CDC achieves an equivalent bits of resolution of 8.8 bit with an FoM of 1.16 pJ/c.-s. for off-chip capacitance ranging from 0 to 15 pF. Furthermore, a frequency-mode oscillator-based capacitance-to-digital converter (CDCs) is implemented for comparison. A linearity compensation method is adopted by considering all causes of nonlinearity in detail. As the result, a highly linear performance can be expected when facing on-chip capacitive sensors or connecting the sensor and the CDC directly by bond wires. The frequency-mode CDC demonstrates an equivalent bits of resolution of 7.9 bit with an FoM of 10.6 pJ/c.-s. for an off-chip capacitance ranging from 0 to 12 pF. Finally, a conclusion of oscillator-based circuits is given.

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Chapter 1
Introduction

1.1 Motivation

The rising tide of artificial intelligence and Internet of things draw a lot of attention not only in academic but also in industry. Thanks to the massive computing power of integrated circuits nowadays and high data throughput of current wireless transmission, a huge wireless network consists of thousands sensor nodes becomes possible. As the required number of sensor nodes rises dramatically, how to lower the power consumption of each node becomes an important issue.

A typical sensor node consists of sensor, interface circuit, power module, clock source, wireless transceiver (TRx), micro controller unit (MCU), and memory as shown in Fig. 1.1. The wireless transceiver is the most power-consuming unit. By compressing the sensed data and then storing it in the memory, the wireless transceiver can only work for a small period to transmit the data. The average power consumption of the transceiver can be reduced. The most power-consuming unit now falls on the unit which needs to be turned on all the time. The clock source needs to operate all the

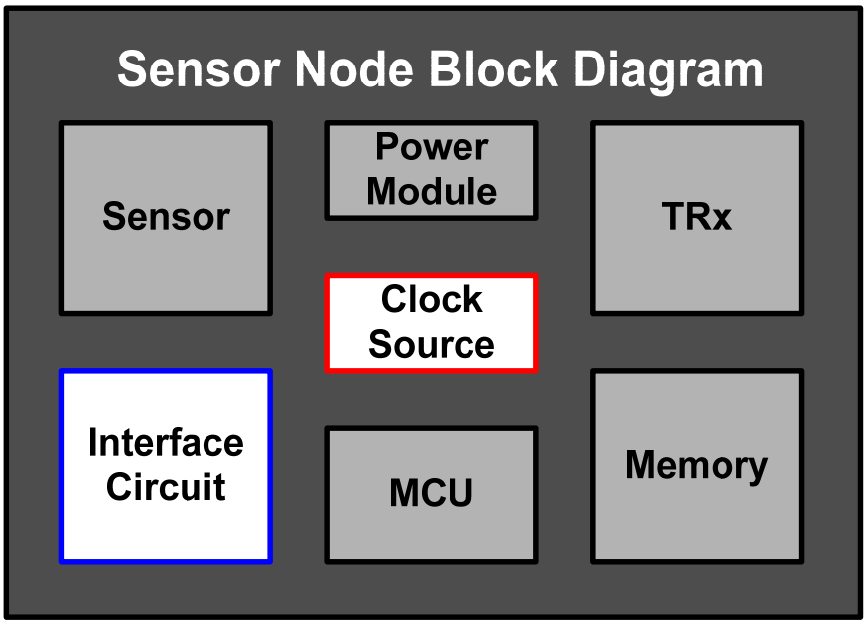

Fig. 1.1 The block diagram of a typical sensor node.

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time to provide the correct timing for other blocks, and the sensor interface circuit needs to watch over the change of sensor for recording or alarming. If the power consumption of these units can be effectively suppressed, the power efficiency of the sensor node can be much improved.

Power consumption is not the only important issue of a wireless sensor node, the capability of integration and the cost of fabrication are important. The relaxation oscillator is considered a promising candidate to realize low-cost and low-power on-chip clock signal. For the power efficiency of MCU and memory, advanced CMOS process is preferred, which usually have a limited voltage headroom. Time mode signal processing can move the signal from voltage domain to time domain and break the limit of voltage headroom. The relaxation oscillator is also a popular solution for oscillator-based time-mode signal processing.

In this thesis, the utilization of relaxation oscillators in low-power wireless sensing applications as the clock source and interface circuits for capacitive sensors are proposed. By analyzing the circuit operation in detail, the challenges and solutions for relaxation oscillators in these applications are discussed and proposed with silicon verifications, respectively.

1.2 Thesis Organization

The subsequent chapters of this thesis are organized as follows: Chapter 2 introduces a temperature compensated CMOS relaxation oscillator. In addition, in order to point out the challenges and breakthroughs, a literature survey of the solutions for clock source is presented. In Chapter 3, the background of capacitive sensor interface circuits along with a proposed classification for oscillator-based capacitor-to-digital converter (CDC). A period-mode CDC and a frequency-mode CDC are fabricated and analyzed in Chapter 4 and Chapter 5, respectively. The comparison of calculated result and measured result is provided. Finally, a conclusion is given in the end of the thesis.

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Chapter 2
A Temperature Compensated CMOS Relaxation Oscillator

2.1 Motivation and Specification of Clock Signals

Most electronic systems require a clock signal to provide the timing information and to synchronize the operation of each building blocks. For digital logic, the clock signal regulates the sequencing of digital state machines, which ensures that the key timing parameters like setup and hold times and propagation delay are within allowable limits. In communication systems, the clock signal regulates the speed of synchronized data transmission over the link. The clock signal is also required as reference in wireless transceivers or adopted as a wake-up timer in sensor nodes.

In a typical wireless sensor node for IoT application, there are two major specification for a clock signal: frequency stability and jitter/phase noise requirement. In addition, the specifications varies with different purposes, such as sleep-time clock, sampling clock of data converter, reference of radio frequency (RF) carrier, and data synchronization. The following will introduce the specifications and effects in these purposes.

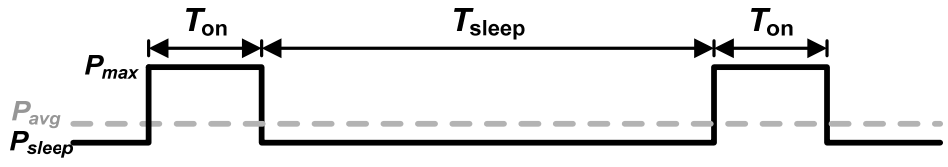

Fig. 2.1 The illustration of cyclic sleep scenario.

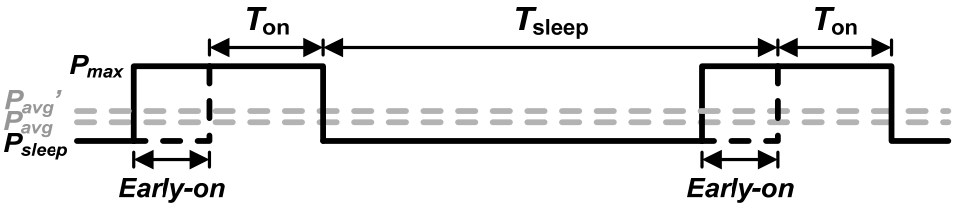

Fig. 2.2 The illustration of cyclic sleep scenario with early-on.

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2.1.1 Frequency stability of Sleep-Time Clocks

The cyclic sleep scenario [1] is typically adopted in low-power applications where the device core is shut down for a pre-set time called “sleep time” typically in the range of 2 to 10 seconds and “woken” when it needs to transmit data during a short burst time which lasting a few milliseconds. This scenario results a low duty cycle, which leads to lower average power consumption as illustrated in Fig. 2.1. To awake the circuit at the right time, a clock signal is required, which is usually named as sleep-time clock (STC). The frequency tolerance of a typical crystal oscillator for STC in Bluetooth 5.0 is ±500 ppm [2] and the frequency of STC is usually selected to be 32.768 kHz. In addition, the jitter/phase noise requirement of STC has no special specification. The frequency inaccuracies of the STC s result in a certain level of uncertainty in the time when sensor node wakes up from sleep to listen to packets from the control unit. Due to this uncertainty, the sensor node must wakes up and starts listening earlier as shown in Fig. 2.2. The duty cycle of the sensor node is increased due to early-on, hence the average power consumption is increased. The battery life extension ratio with a SiT1552 5-ppm 32 kHz TCXO over a 100 ppm and 200 ppm XO is shown in Fig. 2.3 [1], which indicates that the frequency accuracy of STC directly affects the battery life of a sensor node.

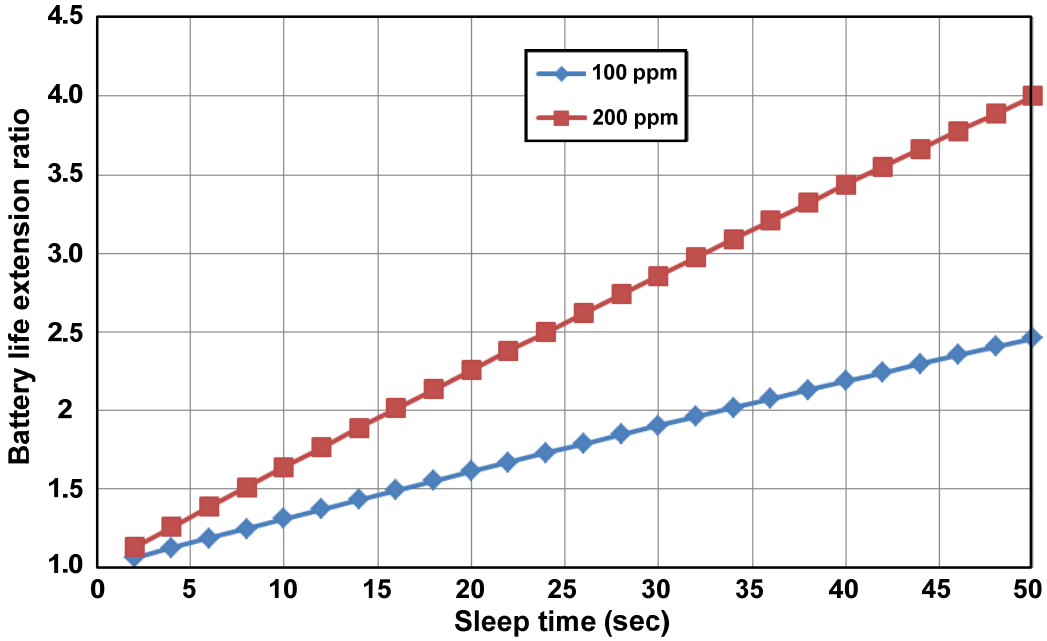

Fig. 2.3 Battery life extension ratio with a SiT1552 5-ppm 32 kHz TCXO over a 100 ppm and 200 ppm XO [1]

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2.1.2 Sampling clock jitter of data converter

To begin with, Fig. 2.4 shows the effect of sampling clock jitter in an analog-to-digital converter. The uncertain timing of the rising edge Δt results the sampled voltage error ΔV which can be obtained by multiplying Δt by the slope of the tangent line to the input signal s_1. Assume an input signal given by

$$V_{\text{in}}(t) = A\sin(2\pi ft)\,. \tag{2.1}$$

Then the slope of the tangent line to the input signal is given by

$$s_1 = \frac{dV_{\text{in}}(t)}{dt} = 2\pi fA\cos(2\pi ft)\,, \tag{2.2}$$

which has a root-mean-square (rms) value of

$$s_1\big|_{rms} = \frac{2\pi fA}{\sqrt{2}}\,. \tag{2.3}$$

Now the rms value of ΔV can be obtained by multiplying the rms jitter of the sampling clock by (2.3), which is given by

$$\Delta V_{rms} = \frac{2\pi fA\tau_{\text{CLK}}}{\sqrt{2}}\,, \tag{2.4}$$

where τ_{CLK} is the rms jitter of the sampling clock. The theoretical signal-to-noise-ratio (SNR) when considering sampling clock jitter can be calculated as

$$SNR = \frac{Signal\ Power\big|_{rms}}{Noise\ Power\big|_{rms}} = 20\cdot\log\left(\frac{A/\sqrt{2}}{2\pi fA\tau_{\text{CLK}}/\sqrt{2}}\right) = 20\cdot\log\left(\frac{1}{2\pi f\tau_{\text{CLK}}}\right). \tag{2.5}$$

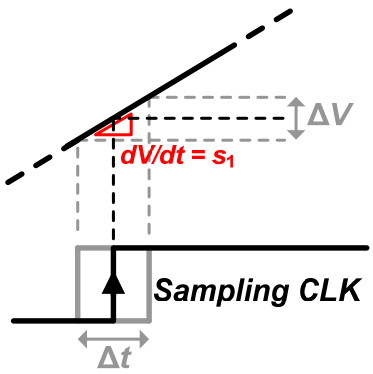

Fig. 2.4 The effect of sampling clock jitter

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From (2.5), the required τ_{CLK} for a 10-bit Nyquist-rate data converter is 0.3962% of T_{CLK}, which can be further relieved if an oversampling data converter is adopted.

2.1.3 Frequency tolerance in wireless transceivers

Table 2.1 lists the requirement of clock signal in several popular wireless transmission standards [2]−[5]. All of them require the accuracy of clock frequency at a level of several tens of ppm. However, such high frequency stability requirement is hard to be realized by only CMOS circuits, which limits the use of pure CMOS relaxation oscillators as the reference clock of the wireless transceivers.

Table 2.1 Clock requirement of popular wireless transfer standards for sensor applications

802.15.4 LOW-RATE WIRELESS PERSONAL AREA NETWORKS						
Transmitted center frequency tolerance						
O-QPSK[a]	BPSK[b]	ASK[c]	CSS[d]	UWB[e]	GFSK[f]	MSK[g]
±40 ppm	±40 ppm	±40 ppm	±40 ppm	±20 ppm	±40 ppm	±40 ppm

802.15.6 WIRELESS BODY AREA NETWORKS		
Narrow band	UWB[e]	Human body communications
Transmit center frequency tolerance	Symbol clock frequency tolerance	
±20 ppm	±20 ppm	

BLUETOOTH 5.0
Active clock accuracy: ±50 ppm
Transmitted initial center frequency shall be within ±75 kHz from f_c.
f_c: 2402~2480 MHz

ANT[h]	
Frequency tolerance	Symbol clock frequency tolerance
±61.5 ppm	±50 ppm

[a] Offset quadrature phase-shift keying
[b] Binary phase-shift keying
[c] Amplitude shift keying
[d] Chirp spread spectrum
[e] Ultra-wide band
[f] Gaussian frequency-shift keying
[g] Minimum shift keying
[h] ANT is an open access proprietary multicast wireless sensor network technology designed and marketed by ANT Wireless. (A division of Dynastream Innovations, in turn a wholly owned subsidiary of Garmin.)

Table 2.2 Comparison of different implementations of clock sources

	Pros.	***Cons.***
Crystal	◆ Nearly null TCF ◆ High accuracy	◆ Fragile ◆ High package cost and volume
MEMS	◆ Robust ◆ Low manufacturing cost	◆ Higher TCF (~30 ppm/°C) ◆ ±2% frequency offset
CMOS	◆ Low manufacturing cost ◆ μW power consumption	◆ Need additional circuits for calibration ◆ Poor noise performance

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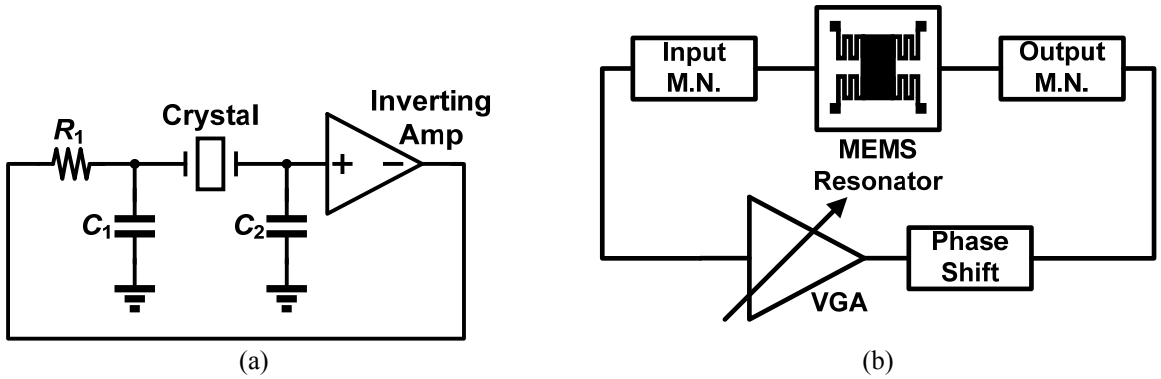
2.2 Techniques for Generating a Stable Clock Signal

Table 2.2 lists three popular solutions of clock-signal generation. Crystal oscillators have been adopted for several decades due to their highly stable electrostriction. The crystal can be regarded as a high quality factor resonator. Cooperated with an amplifier for loss compensation and additional phase shift component, the crystal can be used to generate a low-noise and nearly null temperature coefficient (TCF) clock signal. Fig. 2.5 (a) shows the schematic of the famous Pierce crystal oscillator. However, the crystal is fragile due to its physical characteristic, which results in the high package cost and volume.

The high quality factor resonator can also be realized by microelectromechanical systems (MEMS). MEMS catches the eyes of industry and academics due to their mass-producing potential as the integrated circuits. Fig. 2.5 (b) shows a typical MEMS oscillator. As the same as the crystal oscillator, an amplifier and a phase shifting component are required. In addition, due to the nonlinearity of MEMS resonator when facing a large input signal, a gain control mechanism is inevitable. The characteristics of MEMS resonator usually change with temperature. Several techniques have been proposed to improve the frequency stability versus temperature variation, such as integrated micro-ovens [6]−[8] and on-chip temperature sensor with calibration circuits [9]. However, these techniques increase the power consumption and circuit complexity.

For emerging applications such as wearable devices, Internet of things, and wireless sensor networks, the relaxation oscillator is considered a promising candidate to realize low-cost and low-



(a) (b)

Fig. 2.5 (a) The Pierce crystal oscillator and (b) a typical MEMS oscillator.

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power on-chip clock signal. Even though the frequency accuracy requirement mentioned in 2.1.3 rules out the possibility of relaxation oscillator as the LO or reference clock for wireless transceiver, the operating scheme of the wireless sensor node. The MEMS oscillators [6]−[8] occupy mW-level power consumption. In a typical wireless sensor node, the transceiver only operates with a small duty cycle for power efficiency consideration. When the transceiver is shut-down, keeping the MEMS oscillators or crystal oscillators running is unwise. The relaxation oscillator with microwatt power consumption can be adopted as the system clock for ADC and digital blocks such as MCU and memory. By replacing milliwatt oscillators with relaxation oscillators when the transceiver is off duty, the power efficiency of the sensor node can be further improved.

Although the requirement of frequency stability is alleviated in ADC and digital blocks, relaxation oscillators still need to conquer several challenges to meet the target. Due to the inherent delay variations of the comparators and logic gates, a relaxation oscillator generally suffers from inferior frequency stability at the output. In low-frequency designs, this effect is negligible if the delay is much smaller than the period of the oscillation signal. However, as the output frequency exceeds tens of megahertz, excessive power consumption is inevitable in the oscillator design to keep the delay within a reasonable range for desirable frequency stability.

In order to overcome such limitations, frequency-locked loop has been adopted. In circuit implementations, frequency-to-voltage converters are utilized to convert the oscillation frequency into a voltage, which is compared and locked to a reference [10]−[11]. For the purpose of reducing circuit complexity, various techniques such as voltage average feedback [12] and feedforward delay cancellation scheme [13] have been developed. However, additional compensated voltage references or replicas of comparators are still required in the proposed techniques. Alternatively, a relaxation oscillator with an integrated error feedback (IEF) has been presented in [14], in which additional comparators are adopted for the timing control.

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2.3 The Proposed 51.3-MHz 21.8-ppm/°C CMOS Relaxation Oscillator

2.3.1 Overview of Operation

Fig. 2.6 shows the block diagram of the proposed relaxation oscillator, which is composed of two identical parts each dominating half of the oscillation cycle. The current source, including R_{ref1}, *op-amp*$_1$ and M_1, provides a charging current for C_{ref1}. The comparator compares the capacitor voltage V_{c1} with the threshold voltage V_{th1}, while the result resets the SR latch to complete half of the cycle. It is noted that the value of V_{th1} is generated by the IEF consisting of C_{s1}, C_{int1} and *op-amp*$_2$. S_1 is included only for measurement purposes and can be neglected for circuit operation. All op-amps and comparators are realized by folded cascode differential pairs with a constant-g_m biasing technique to provide proper gain and dc bias over a wide temperature range. The schematic of the building blocks is illustrated in Fig. 2.7 where the start-up circuits are not shown. Based on the operating principle of a relaxation oscillator, the period T_{OSC} is given by

$$T_{OSC} = 2 \cdot \left[\frac{C_{ref} \cdot V_{th}}{(V_{DD} - V_{ref}) / R_{ref}} + t_d \right], \tag{2.6}$$

where t_d is the delay time dominated by the comparators.

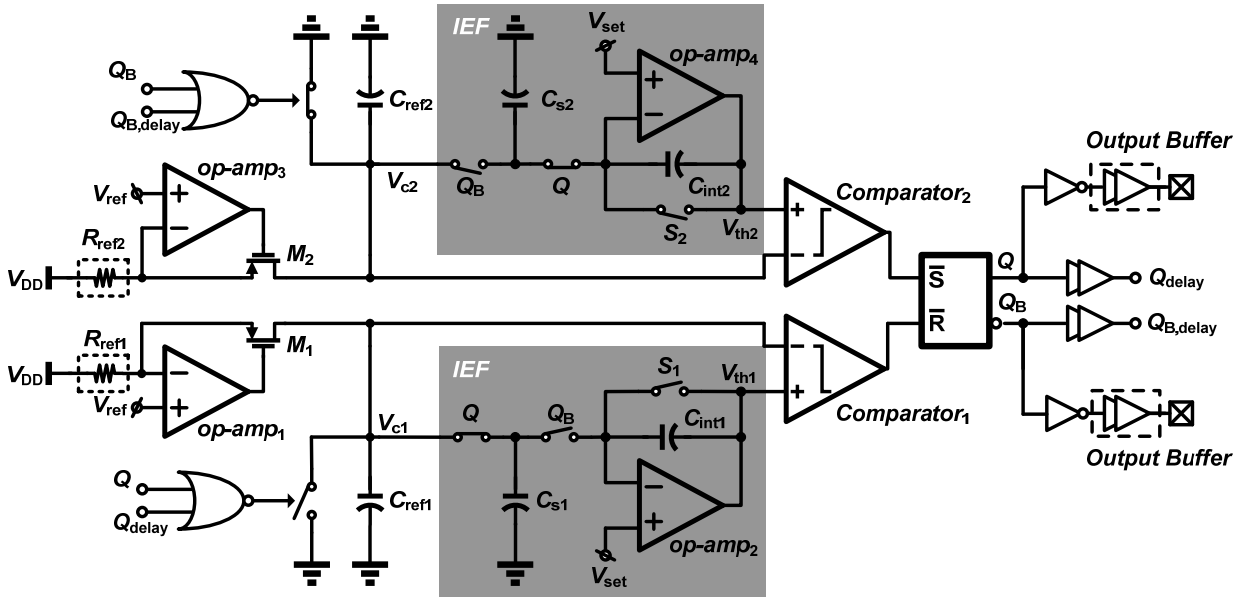

Fig. 2.6 The block diagram of the proposed relaxation oscillator.

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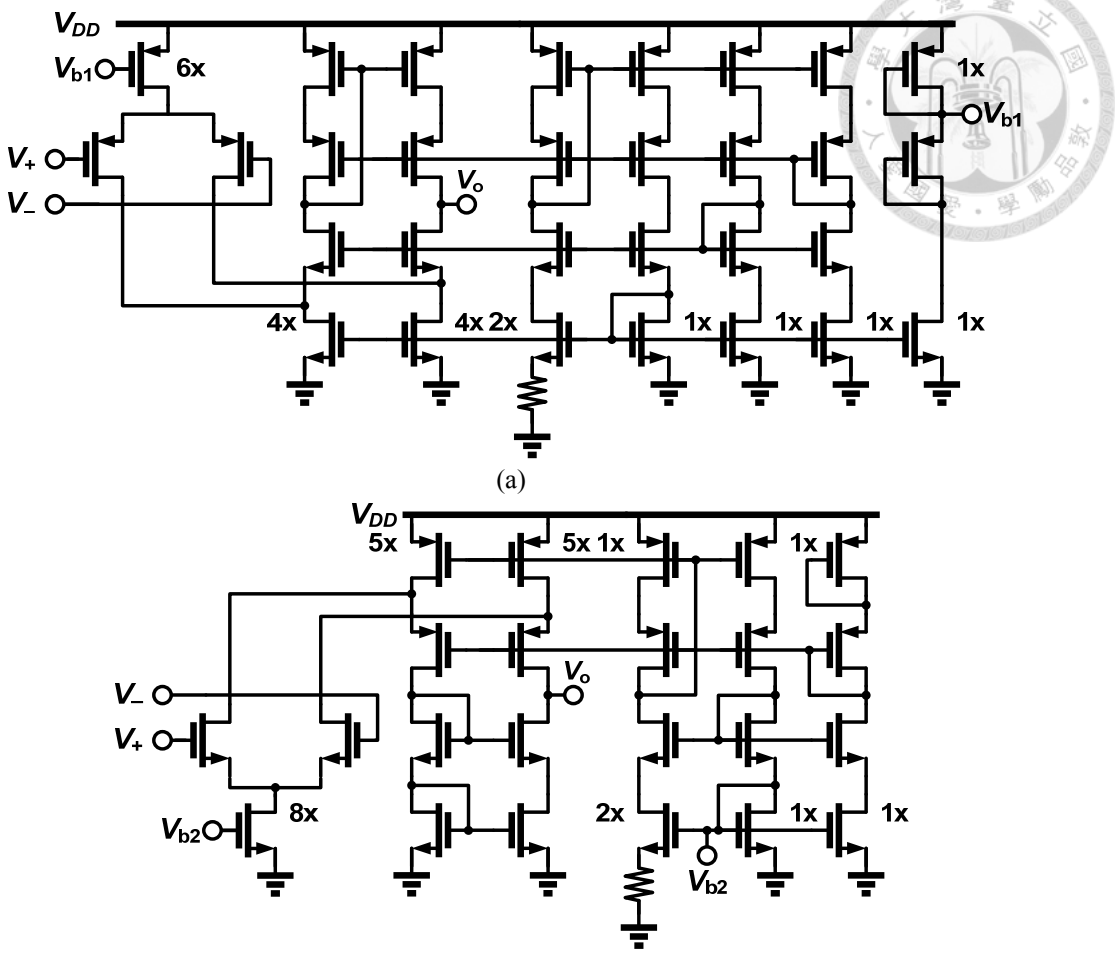

Fig. 2.7 The schematic of (a) the comparator with bias circuit and (b) the op-amp with bias circuit.

2.3.2 Integrated Error Feedback (IEF)

According to circuit simulations, the delay of the comparator has a variation up to ±13% for a temperature range from -20 to 100°C. In order to maintain an average oscillation frequency drift less than 30 ppm/°C in this particular design without the assistance of calibration schemes, the ratio of t_d to T_{OSC} should be kept less than 1.4%. By observing the waveform at positive input node of the comparator, the charging slope is generally inversely proportional to T_{OSC}. The driving current of the comparator can be approximated by the voltage difference between the input nodes multiplied by its transconductance. As a result, the condition for the SR latch to reach the switching threshold is given by

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$$\int_{t=0}^{t_d} G_m \cdot m \cdot t \; dt = C_{in} \cdot \Delta V \;, \tag{2.7}$$

where G_m is the transconductance of the comparator, m is the voltage rising slope of V_{c1}, C_{in} is the input capacitance of the SR latch, and ΔV is the switching threshold of the SR latch to change state. Based on (2.7), the dependence of t_d on the circuit parameters is simply

$$t_d \propto \sqrt{C_{in} \cdot T_{OSC} / G_m} \;. \tag{2.8}$$

In order to maintain a nearly constant ratio of t_d to T_{OSC}, the required G_m is proportional to $1/T_{OSC}$, indicating a required bias current proportional to $1/T_{OSC}^2$. Note that the cost of minimizing t_d in high-frequency applications is a significant increase in the bias current of the comparator. Therefore, rather than reducing the delay of the comparator, it is desirable to achieve the frequency stability versus temperature by proper calibration schemes.

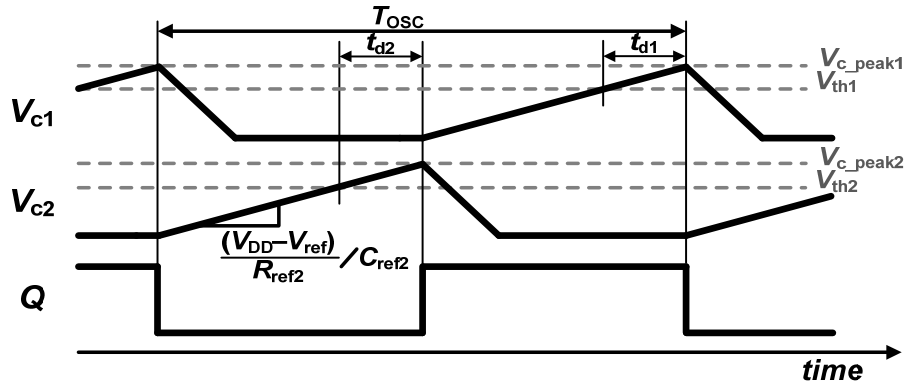

Fig. 2.8 The timing diagrams of relaxation oscillator with a delay t_d.

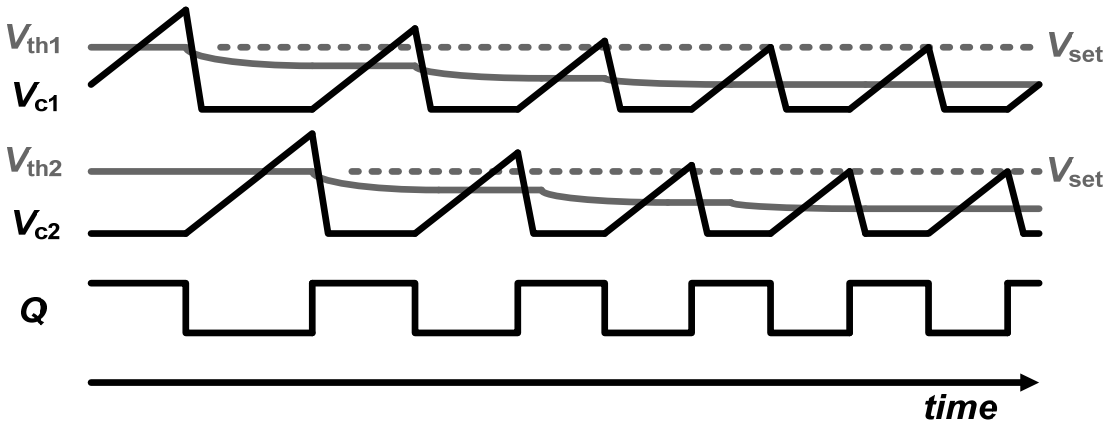

Fig. 2.9 Operating waveforms of the relaxation oscillator.

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In the proposed relaxation oscillator, an IEF is adopted to relieve the power requirement of the comparators. As illustrated in Fig. 2.8, due to the existence of t_d, the voltage V_c tends to be charged beyond the comparator threshold, and T_{OSC} can be expressed by the peak capacitor voltage V_{c_peak} as

$$T_{OSC} = 2R_{ref}C_{ref} \cdot \frac{V_{c\_peak}}{(V_{DD} - V_{ref})}, \tag{2.9}$$

indicating that the frequency stability is mainly determined by the sensitivities of V_{c_peak} and R_{ref} to temperature.

Fig. 2.9 shows a conceptual illustration of the waveforms as the IEF shown in Fig. 2.10 is adopted to suppress the overshoot of V_{c1} and V_{c2} due to the delay t_d. In each half-cycle, C_{ref} is charged by the current source. As the value of V_c reaches the threshold voltage V_{th}, the comparator changes its output state after certain delay, ends the half-cycle and activates the alternative subcircuit. By the end of the half-cycle, the peak value of V_c is sampled by the sensing capacitor C_s and then connects to the negative input terminal of the op-amp in the IEF. Due to the virtual short characteristic of the op-amp with negative feedback, the voltage of C_s drops to V_{set} and the excessive

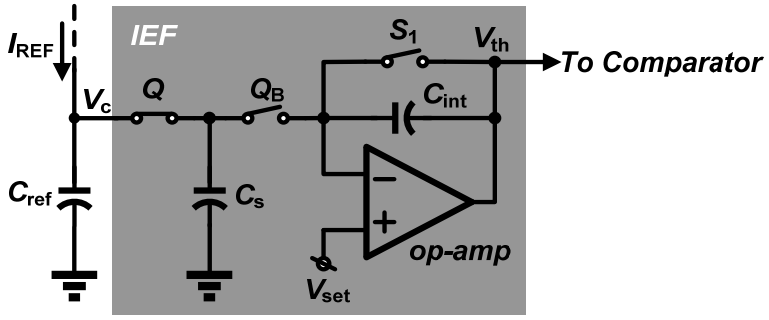

Fig. 2.10 The schematic of the integrated error feedback.

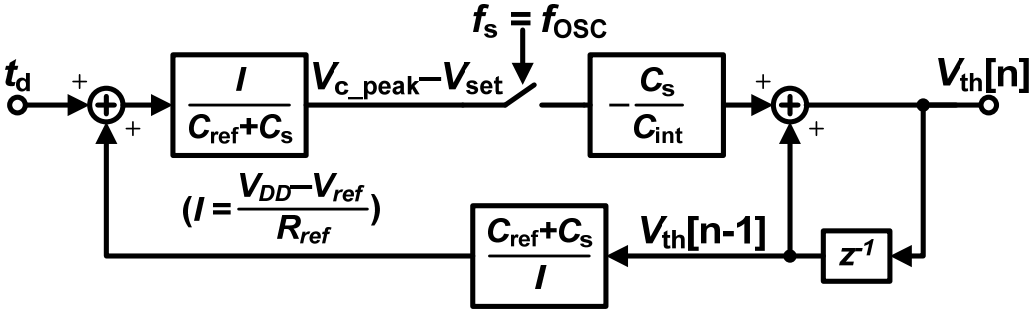

Fig. 2.11 The simplified circuit model of the integrated error feedback (IEF).

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charge is transferred to C_{int}, resulting in a decrease in V_{th} for the following oscillation cycle. The error voltage (V_{c_peak} - V_{set}) is integrated in C_{int} to dynamically adjust V_{th} until V_{c_peak} settles at V_{set}.

The behavior of the IEF can be evaluated by the simplified model as shown in Fig. 2.11, where t_d is considered constant at a fixed temperature and the charging current for C_{ref} is denoted as I. Consequently, the transfer function of IEF is given by

$$H(z)=\frac{V_{th}(z)}{t_d(z)}=\frac{-\frac{I}{C_{ref}+C_s}\cdot\frac{C_s}{C_{int}}}{1-z^{-1}\left(1-\frac{C_s}{C_{int}}\right)}, \tag{2.10}$$

where $I = (V_{DD} - V_{ref})/R_{ref}$. The feedback is considered stable as

$$\left|1-\frac{C_s}{C_{int}}\right|<1 \Rightarrow 0<C_s<2\cdot C_{int}, \tag{2.11}$$

and the required number of operating cycles N for (V_{c_peak} - V_{set}) to settle within 0.1% of the preset value can be estimated as

$$N>\frac{\log_{10}(0.1\%)}{\log_{10}\left(\left|1-\frac{C_s}{C_{int}}\right|\right)}. \tag{2.12}$$

By taking the leakage current of the integrator into account, a design value of 4.6% is used for C_s/C_{int}. Based on (2.12), the required cycles N in this particular design is estimated 147 cycles.

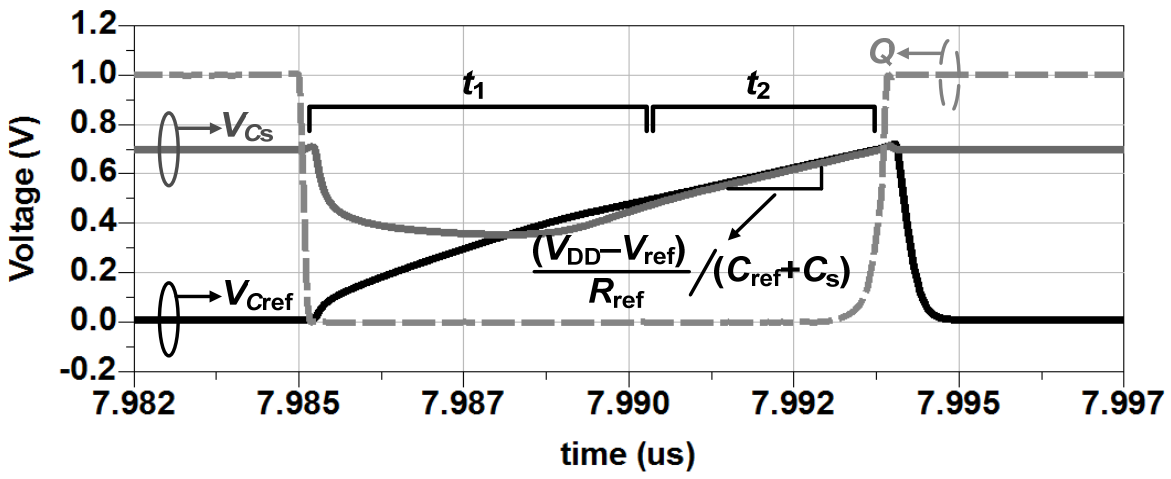

Fig. 2.12 Simulated voltage waveforms at C_s and C_{ref}.

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2.3.3 Sampling Capacitor C_S

It is noted that the voltage across C_s is not reset to zero before sampling. At the end of each operation cycle of the IEF, the voltage of C_s is set to V_{set}, and then connects to C_{ref} in shunt by a switch during the charging phase. Fig. 2.12 depicts the simulated voltage waveforms. During t_1, charge redistribution takes place between C_s and C_{ref}, leading to a sharp decrease of the voltage across C_s, namely V_{Cs}, at the beginning of t_1 as C_{ref} is four times as large as C_s. The current source provides a constant current to C_s and C_{ref} during t_1 and t_2. After the charge redistribution between C_s and C_{ref} completes, the voltage cross C_s and the voltage across C_{ref} are both rising with the slope of

$$\frac{(V_{DD}-V_{ref})}{R_{ref}} \Big/ (C_{ref}+C_s), \tag{2.13}$$

as illustrated in the timing waveforms during t_2. The required charging period is given as

$$\begin{aligned} t_1 + t_2 &= \frac{Q}{I} \\ &= \frac{V_{set}\cdot(C_{ref}+C_s)-V_{set}\cdot C_s}{(V_{DD}-V_{ref})/R_{ref}} = \frac{V_{set}\cdot C_{ref}}{(V_{DD}-V_{ref})/R_{ref}}. \end{aligned} \tag{2.14}$$

It is noted that the value of C_s only affects the charging slope but has no influence on the oscillation period of the proposed circuit. Due to the on-resistance of switches, there is a 4-mV tracking error voltage between C_s and C_{ref}. This error results in a frequency offset and a residual temperature coefficient of the oscillator.

2.3.4 Generation of the Reference

By employing the IEF, the peak voltage V_{c_peak} is locked to the value of V_{set}, while V_{ref} and V_{set} are implemented by resistor voltage dividers between V_{DD} and ground. As a result, T_{OSC} in (2.9) can be rewritten as

$$T_{OSC} = 2R_{ref}C_{ref}\cdot\frac{\beta}{(1-\alpha)}, \tag{2.15}$$

where $\alpha = V_{ref}/V_{DD}$ and $\beta = V_{set}/V_{DD}$. The temperature coefficient of T_{OSC} is dominated by R_{ref} as α and β are resistance ratios, while the temperature coefficient of capacitor are rather small.

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To realize the on-chip resistance R_{ref} in the proposed circuit, the technique of composite resistor is utilized. As shown in Fig. 2.13, the resistance is implemented by a parallel-combined resistor R_A and a series-combined resistor R_B, while both R_A and R_B are composed of two types of resistors with opposite 1st-order temperature coefficients (TCs). Fig. 2.14 shows the resistance variation corresponding to different temperature of parallel-combined, series-combined, and mixed resistor, respectively. It is noted that parallel-combined resistor has an opposite 2nd-order temperature coefficients compared to series-combined resistor, while mixing them together can further cancel the resistance variation due to temperature. Compared with the composite resistors in [12]−[13], [15]−[17], this device arrangement not only allows the designers to choose the desirable TC but also enhances the frequency stability at the presence of process variations. Fig. 2.15 shows the Monte-Carlo simulation of composite resistors, which indicates that the composite resistor adopting both parallel-combined and series-combined resistors has better stability.

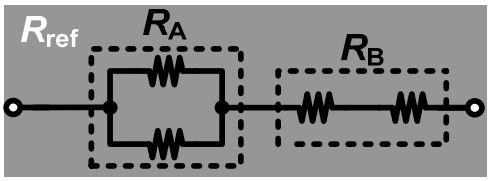

Fig. 2.13 The R_{ref} implemented by the technique of composite resistor

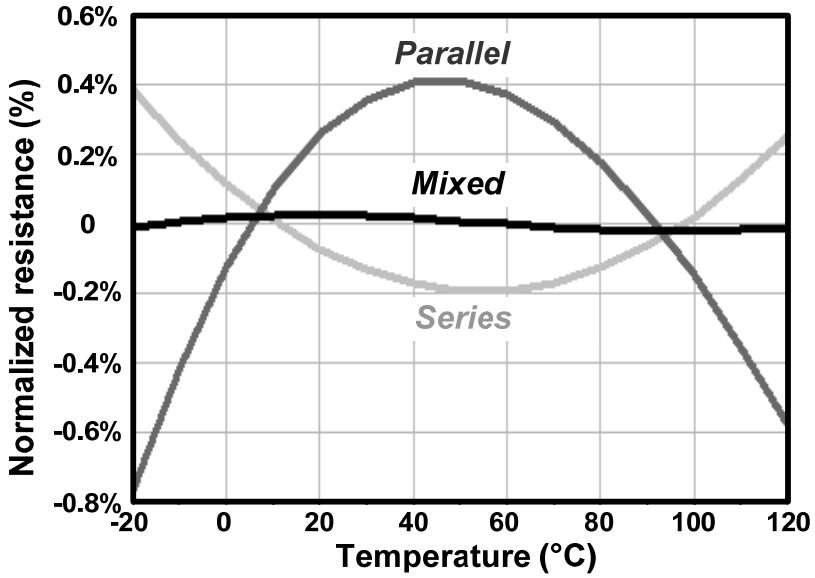

Fig. 2.14 Simulated normalized resistance of composite resistors in different ways of connection

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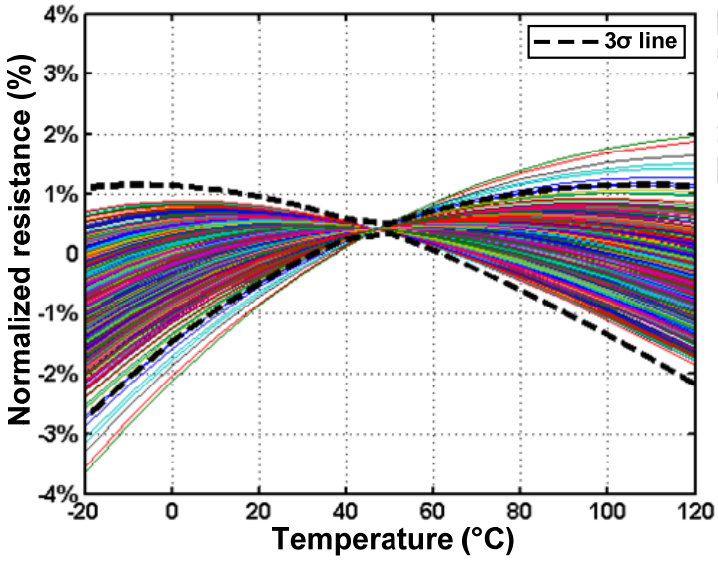
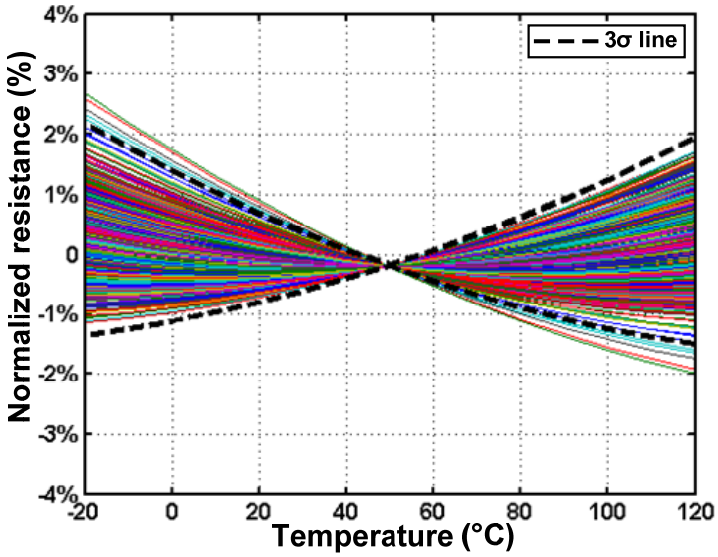
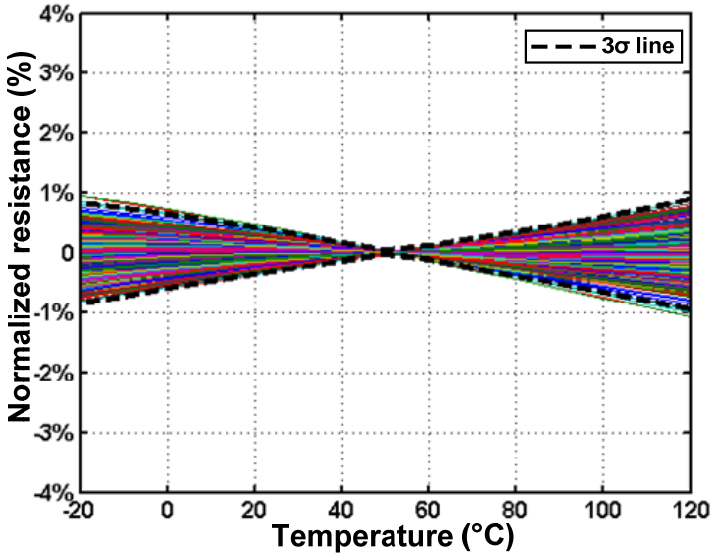


(a)



(b)



(c)

Fig. 2.15 Monte-Carlo simulation of normalized resistance deviation of composite resistors: (a) series-combined, (b) parallel-combined and (c) mixed combined.

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In most circuit implementations, the composite resistors are generally employed to realize a resistance with zero TC. However, in this proposed circuit, the design target of the composite resistor is to compensate for the remaining TC of the oscillator due to the variations of on-resistance of the switches and open-loop gains of the op-amps versus temperature. To have a better understanding of the design concept, normalized frequency variations based on circuit simulations are illustrated in Fig. 2.16. With a composite resistor with zero TC, the proposed relaxation oscillator demonstrates a normalized frequency variation of ±0.28% with the temperature range from -20 to 100°C. On the other hand, by properly choosing the TC of the composite resistors to follow the temperature dependence of the oscillator, the compensated relaxation oscillator can achieve better frequency stability versus temperature, leading to a normalized frequency variation of ±0.06% with the same temperature range in this particular case.

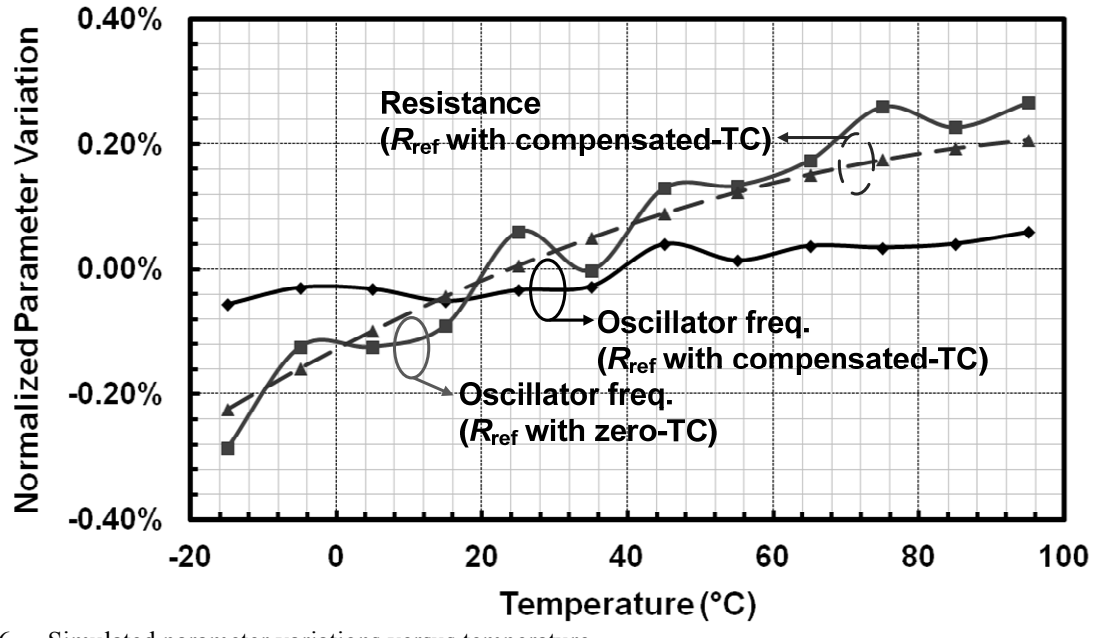

Fig. 2.16 Simulated parameter variations versus temperature.

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2.4 Experimental Results

The proposed clock oscillator is fabricated in a 90-nm general-purpose CMOS process. Fig. 2.17(a) shows the die photo with a core area of 0.027 mm^2. Operated at a supply voltage of 0.8 V, the power consumption at room temperature is 18 μW. Fig. 2.17 (b) illustrates the power breakdown diagram, where the comparators account for 45% of the total power. The oscillation frequency is measured by an Agilent 53220A 350-MHz universal frequency counter/timer. Fig. 2.18 shows the measured oscillation frequency and power consumption, indicating a frequency variation of ±0.53% as the supply voltage changes from 0.8 to 1.2 V.

In order to evaluate the effectiveness of the proposed technique, switches S_1 and S_2 are included in the circuit implementation to disable the function of the IEF. Fig. 2.19 shows the output frequency of the relaxation oscillator with and without the IEF. For a temperature range from -20 to 100°C, the measured frequency variation of the proposed oscillator without IEF is ±9.2%. As the IEF is activated, the measured frequency variation is less than ±0.13%, leading to an average frequency drift of 21.8 ppm/°C. Fig. 2.20 shows the close-in phase noise of the fabricated circuit at room temperature. At offset frequencies of 100 kHz and 1 MHz, the measured phase noises are -67.35 and -83.29 dBc/Hz, respectively. The measured rms jitter is 89.27 ps.

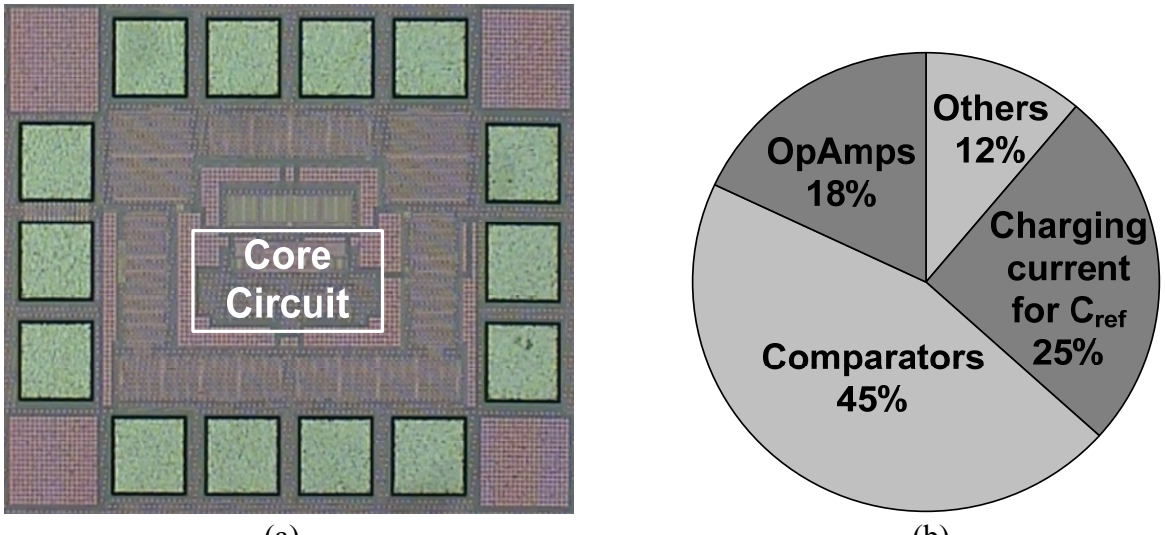

Fig. 2.17 (a) The microphotograph of the fabricated circuit, and (b) power breakdown of the proposed relaxation oscillator.

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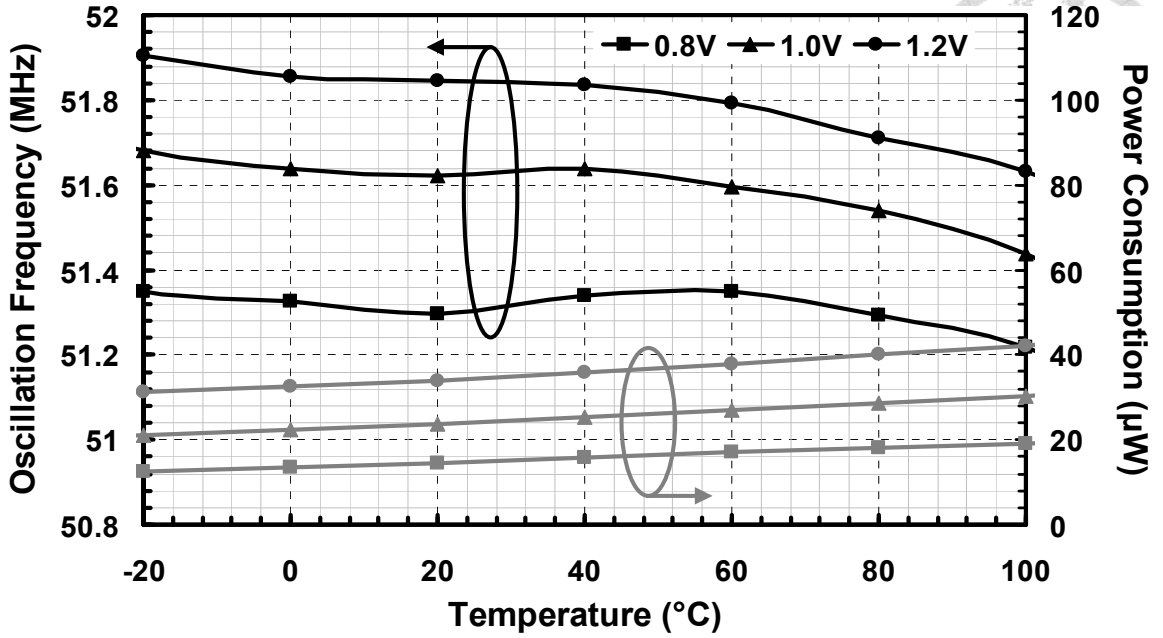

Fig. 2.18 Measured frequency and power of the oscillator from -20 to 100°C.

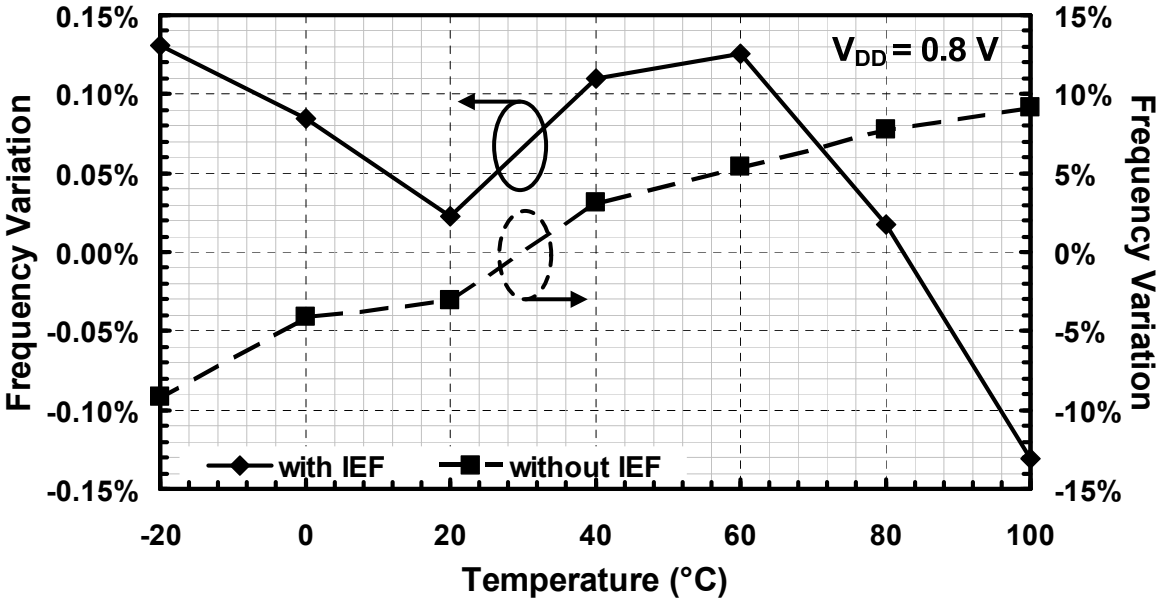

Fig. 2.19 Measured frequency variation of the oscillator with and without IEF.

By applying a step control signal to switch S_1, the settling time of IEF is examined. Fig. 2.21 depicts the measured settling behavior of the output frequency by using an Anritsu MS2690A signal analyzer. The settling time of the IEF is 3.3 μs, which is approximately 150 cycles as predicted by (2.12).

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The performance of the fabricated circuit is summarized in Table 2.3, where a figure of merit (FoM) is introduced to compare the frequency sensitivity to temperature under different power and frequency as

$$\mathrm{FoM} = 10\log\left(\frac{f_{\mathrm{osc}}}{P_{\mathrm{DC}}}\cdot\frac{T_{\mathrm{range}}}{|TC|}\right). \tag{2.16}$$

It is noted that the relaxation oscillator presented in this paper achieves the best FoM of 192 among the state-of-the-art designs.

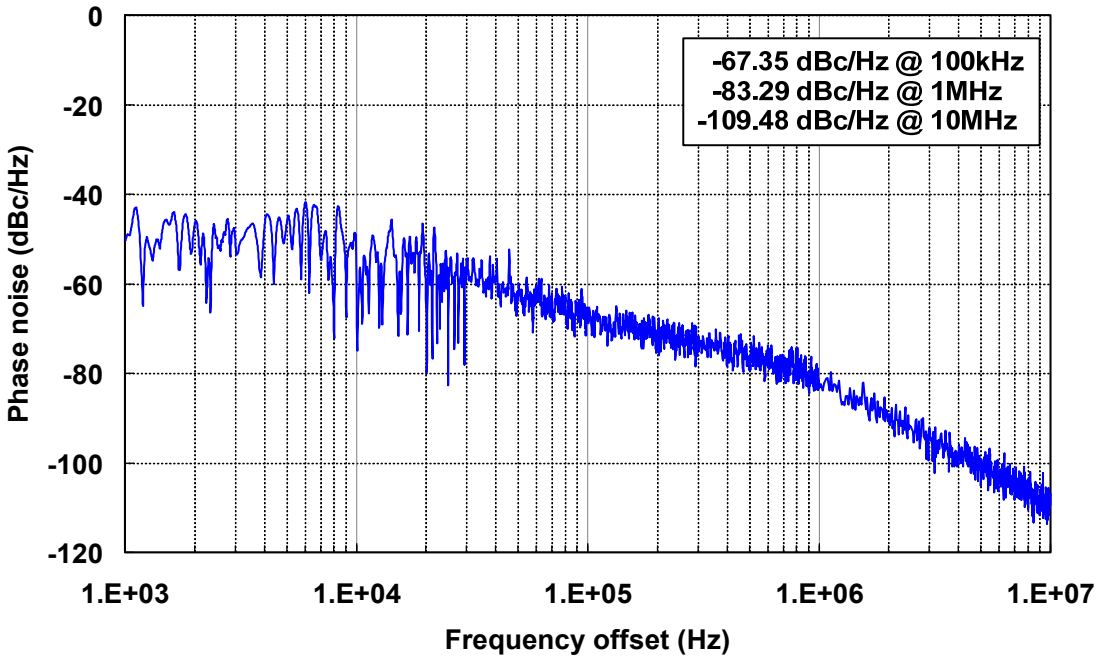

Fig. 2.20 Measured close-in phase noise of the oscillator at room temperature.

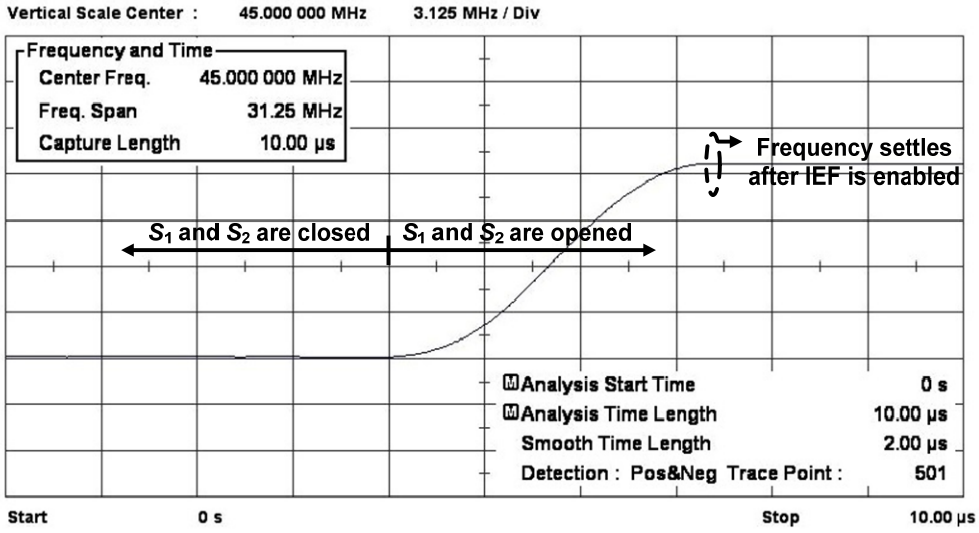

Fig. 2.21 Measured settling diagram of the output frequency.

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Table 2.3 Performance summary and comparison

	[10]	[11]	[12]	[13]	[14]	[15]	[16]	**This Work**
Process [CMOS]	0.18 μm	0.18 μm	0.18 μm	90 nm	65 nm	0.35 μm	0.18 μm	**90 nm**
Freq. [MHz]	10	32.8	14	0.1	12.6	30	1.1	**51.3**
V_{DD} [V]	1.2	1.5	1.8	0.8	1.2	3	1.8	**0.8**
Power [μW]	80	16.6	45	0.28	98.4	180	0.86	**18**
Temp. Coeff. [ppm/°C]	67@ -20 to 100°C	134@ -40 to 85°C	23[a]@ -40 to 125°C	105@ -40 to 90°C	205@ 0 to 80°C	90@ -20 to 100°C	64.3@ -20 to 80°C	**21.8@ -20 to 100°C**
Freq. variation with Supply [%]	±0.05 @ 3 to 1.2 V	±0.27 @ 3.6 to 1.5 V	±0.16 @ 1.9 to 1.7 V	±0.82 @ 0.9 to 0.725 V	±0.07 @ 1.5 to 1.1 V	±2.4 @ 3 to 1.8 V	±1.8 @ @2.4 to 1.2 V	**±0.53 @ 1.2 to 0.8 V**
Area [mm^2]	0.22	0.013	0.04	0.12	0.01	0.08	0.075	**0.027**
Phase noise [dBc/Hz]	-	-	-115[b] @ 1MHz offset	-	-120 @ 1MHz offset	-96 @ 1MHz offset	-74.2 @ 1MHz offset	**-83.3 @ 1MHz offset**
$Jitter_{rms}$/Period [%]	-	-	0.042	-	0.08	-	-	**0.45**
FoM [dB]	173.5	182.7	183.5	176.5	167	173.5	183	**192**
FoM_{noise} [dB][c]	-	-	181.4	-	182.1	163	135.7	**165**

[a]Additional compensated V_{ref} is required.
[b]Estimated from figure.
[c]$FoM_{noise} = 10\cdot\log(f_{osc}^2/[f_m^2\cdot L(f_m)]/P_{DC})$, where f_m is the carrier offset frequency and $L(f_m)$ is the measured phase noise.

2.5 Summary

A 51.3-MHz, 18-μW, 21.8-ppm/°C relaxation oscillator is presented in 90-nm CMOS. The proposed oscillator employs an integrated error feedback (IEF) and composite resistors to minimize its sensitivity to temperature variations. For a temperature range from -20 to 100°C, the fabricated circuit demonstrates a frequency variation less than ±0.13%, leading to an average frequency drift of 21.8 ppm/°C. As the supply voltage changes from 0.8 to 1.2 V, the frequency variation is ±0.53%. The measured rms jitter and phase noise at 1-MHz offset are 89.27 ps and -83.29 dBc/Hz, respectively.

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Chapter 3
Background of Capacitive Sensor Interface Circuits

3.1 Capacitive Sensors

Capacitive sensors are popular due to their characteristics of simple structure and consuming no static current. Fig. 3.1 shows a simple parallel plate capacitor, the value of capacitance is given by

$$C = \frac{\varepsilon A}{d}, \tag{3.1}$$

where ε is the dielectric constant of the dielectric, A is the overlapping area of parallel plates, and d is the distance between the parallel plates. Each parameter in (3.1) can be used for sensing. In [18], the capacitive sensor consists of two semicylindrical conductive plates and the flowing fluid possess a varying ε according to the flow rate. By acquire the value of capacitance, the flow rate can be estimated. By mounting several conductive plates on the sides of a flexible dielectric material [19], the overlapping area A can change with the force applied to the dielectric material. The value of the capacitance can represent the direction and magnitude of the force. By directly applying a pressure

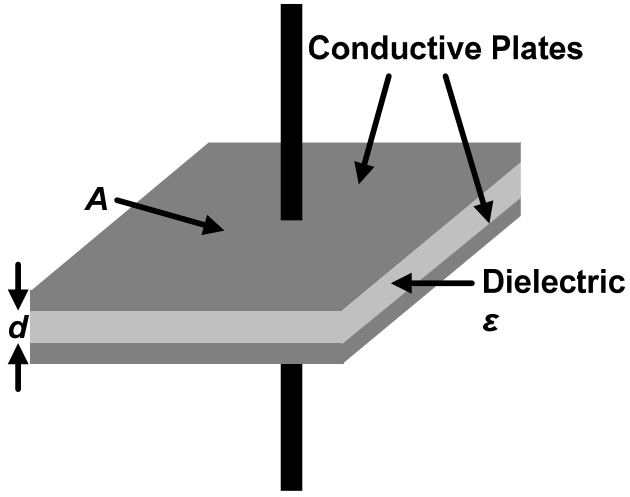

Fig. 3.1 A parallel plate capacitor.

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perpendicularly to conductive plate of the capacitor [20], the distance between the parallel plates will change with the pressure hence the capacitance. As mentioned above, the capacitive sensors can be adopted in a wide range of applications, such as pressure monitoring [20]–[21], displacement sensing [22], humidity sensing [23] and flow sensing [18], [24].

It is worth noting that not all categories of capacitive sensors have their both terminals to be floating. In some applications, one terminal of the capacitive sensor must be connected to the ground because of cost and safety reasons. Such a configuration has many applications including liquid-level sensing [25]–[26], human proximity sensing [27], non-contact ice layer detection [28], RF connector tightness sensing [29] and capacitive microwave power sensing [30]. Such type of capacitive sensors are noted as grounded capacitive sensors and the capacitive sensors with two floating terminals are noted as floating capacitive sensors [31]−[33].

3.2 State-of-the-Art Techniques for Interface Circuits

With the fast-growing market in Internet of Things (IoT), the demand for energy-efficient capacitive-sensor interface circuits with moderate resolution has been increasing dramatically in the past few years. The conventional approach for capacitive-sensor interface is to convert the capacitance of the sensor into voltage domain (C2V) [34]–[36], followed by an analog-to-digital converter (ADC) to provide the required digital outputs [37]–[38]. In order to further reduce the power dissipation and chip area, direct digitization of the sensor capacitance is preferred. As a result, the successive approximation register (SAR) technique has been adopted for capacitor-to-digital converters (CDC) [39]–[40] with excellent power efficiency. However, they are not applicable for grounded capacitive sensors mentioned in 3.1. The switched-capacitor delta-sigma technique [32], [41] as well as hybrid method [42] were also proposed to realize the capacitance-to-digital conversion. Due to the trend of device scaling for CMOS fabrication technologies, the reduced voltage headroom imposes additional challenges in the design of analog integrated circuits. Shifting the signal processing from voltage to time domain has become a promising approach to realize CDC circuits in

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advanced CMOS technologies. Recently, a dual-slope technique [43] and an iterative delay-chain discharging technique [44] have been proposed for capacitance-to-digital conversion. Alternatively, oscillator-based CDCs [45]–[47], which mainly consist of oscillators and counters as the key building blocks, have also attracted great attention for capacitive sensing. Similar to their counterparts such as ADCs [48]–[49] and time-to-digital converters [50]–[51], oscillator-based CDCs possess the advantages of inherited anti-aliasing filtering, simple system structure in circuit implementations, and capability of operating at a limited supply voltage.

3.3 Important Parameters of Interface Circuits

Important parameters of CDCs is similar to those in ADCs. The difference is whether the input is a voltage signal or a capacitor. In addition, the CDCs need to deal with a constant value of capacitance as input, while in most ADCs the dc input voltage is set to 0 due to differential operation. The parameters are listed as follows:

3.3.1 Input Capacitance Range

The capacitance range depends on the sensors, thus there is no specific standard of the input Capacitance range for CDCs. In most capacitive sensors [18], [22]–[24], [29], [46], [52], the capacitance range falls within the range from 0 pF to 20 pF. Due to the requirement of measuring non-varying capacitance of input, the input capacitance range usually regarded as peak-to-peak capacitance swing of the CDC. As the result, the signal power of the CDC can be estimated by the root mean square value of the capacitance swing.

3.3.2 Sampling frequency / Conversion Time

Due to various type of CDCs, not all CDCs are operated with Nyquist rate. Directly comparing the sampling frequency of different types of CDC is meaningless. To correctly characterize different types of CDCs, the parameter noted as conversion time is adopted. The conversion time means the required time of the CDC to acquire an output. The conversion time of a Nyquist rate CDC

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equals $1/f_s$, where f_s is the sampling frequency. When it comes to oversampling CDCs, the conversion time equals OSR/f_s, where OSR is the oversampling ratio.

3.3.3 Capacitance Resolution

The resolution can be defined by the capacitance range incorporating the root mean square value of the output code when measuring a constant capacitance, or by integrating the noise power of the fast Fourier transform (FFT) result of the CDC in a defined frequency bandwidth when an oversampling CDC is adopted.

3.3.4 Linearity

Due to a capacitive ramp is hard to realized for testing of CDCs, the linearity of the CDC usually depicted by the error between the output code and the ideal regression line or by square of the correlation coefficient of the output code and input capacitance.

3.3.5 Power Consumption

The power consumption of the CDC is very important when the CDC is adopted in a wireless sensor node. The power consumption of the CDC directly affect the life time of the battery and occupies a large portion of the sensor-node power consumption when TRx is shut down.

3.4 Principles of Oscillator-Based CDC: Period Mode & Frequency Mode

The main idea of oscillator-based CDCs is generating a signal whose period/frequency is related to the value of capacitance. The period/frequency can be measured by following circuits, then the corresponding input capacitance can be obtained. To estimate the period/frequency of an unknown signal correctly, the most intuitive way is comparing it with a reference clock. According to the relation between the output code of the oscillator-based CDC and the period/frequency of the oscillator, the oscillator-based CDCs can be divided into two categories.

Oscillator-based CDCs generating varying period proportional to the output code is defined as

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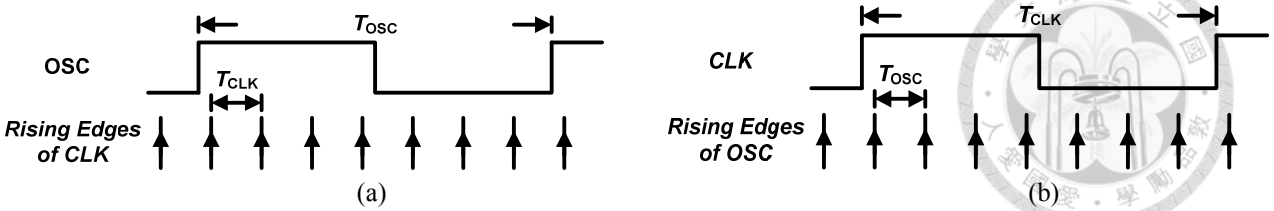

Fig. 3.2 The timing diagram of (a) a period-mode oscillator-based CDC and (b) a frequency-mode oscillator-based CDC.

period-mode CDCs in this thesis. Fig. 3.2 (a) shows the timing diagram of a period-mod CDC, the period of oscillator can be estimated by using a counter to record the times of occurrence of rising edges of *CLK* in a single period of the OSC. On the contrary, oscillator-based CDCs generating varying frequency proportional to the output code is defined as frequency-mode, and the timing diagram of a frequency-mode CDC is shown in Fig. 3.2 (b). The frequency of the oscillator can be estimated by recording the times of occurrence of rising edges of OSC in a single period of *CLK*.

The first difference between period-mode and frequency-mode is the output codes proportional to the period or the frequency of the oscillator, respectively. In order to generate a linear CDC, the oscillator in period-mode requires a period proportional to the capacitance of device-under-test (C_{DUT}), and a frequency proportional to C_{DUT} in required in frequency-mode oscillator-based CDCs on the contrary.

The second difference is the noise contribution of the oscillator adopted in the CDC. Usually, the reference clock has a much better jitter performance than the oscillator. In period-mode CDCs, the noise contribution of the oscillator is only one time for per output, and the noise contribution of *CLK* is proportional to the output codes. On the other hand, the noise contribution of the oscillator is proportional to the output codes in the frequency-mode CDCs.

The third difference is about the equivalent unit of the least significant bit (LSB). The LSB in period-mode CDCs is defined by the reference clock, and the LSB can be regarded as the period of *CLK*, or 2π rad of the phase of *CLK*. As for the LSB in frequency-mode CDCs, the period of OSC varies with C_{DUT}, so the LSB means different time length for each C_{DUT}. The LSB can only be regarded as 2π rad of the phase of the oscillator.

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The final worth mentioning difference between period-mode and frequency-mode CDCs is the interval between each samples. In the period-mode CDCs, the interval between each sample is defined by the period of the OSC, which is varying with the C_{DUT}. The interval between each sample in the frequency-mode CDCs is constant and equals T_{CLK}. Due to these reasons, the mode of oscillator-based CDCs should be choose according the type of capacitive sensors. In addition, the jitter/phase noise requirement of oscillators in different modes of oscillator-based CDCs need to be carefully characterized.

It is noted that the time-mode signal circuit simulation is not well established in major simulating software, only transient simulation can be used for time-mode signal simulation. The time step of transient simulation directly affects the resolution of time-mode signal processing. To correctly simulate the equivalent resolution of an oversampling oscillator-based CDC, the time step needs to be smaller than 0.5 LSB. In the CDCs proposed in this thesis, the required time step is about 2 nanoseconds. In addition, to observe the effect of flicker noise, the required length of simulation time should be several tens of millisecond. Such a long simulation time with a fine time step, the required computing power is large and it is time consuming. To obtain a correct estimation of the performance without long simulating time and large computing load, mathematical models of the operation of the oscillator-based CDC are required. The following chapters present a period-mode CDC and a frequency-mode CDC along with their mathematical analysis and silicon verifications.

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Chapter 4
A Period-Mode Oscillator-Based Capacitor-to-Digital Converter

4.1 Overview of Operation

Fig. 4.1 demonstrates the schematic of the proposed oscillator-based CDC, which consists of a capacitor-controlled oscillator (CCO), a residue generator, an RC oscillator (RCO) with calibrating circuitry and two counters. The CCO continuously generates a timing signal with a period proportional to the capacitance of the device under test (C_{DUT}), while a counter with an external clock is utilized to quantize this period. The timing diagram of the CDC is shown in Fig. 4.2. The output of *Counter*1 represents the number of rising edges of the external clock (*CLK*) in each period of the CCO output and is given by

$$y_1[n] = \frac{1}{T_{CLK}}\left(T_{CCO}[n] + T_{q1}[n] - T_{q1}[n+1]\right), \tag{4.1}$$

where T_{CLK} is the period of the external clock, T_{CCO} is the period of CCO, and T_{q1} is the associated quantization error. Applying Z-transform to (4.1), the simplified result is given by

$$Y_{CCO}[z] = T_{CLK} \cdot Y_1[z] + z \cdot \left(1 - z^{-1}\right) \cdot Y_{q1}[z], \tag{4.2}$$

implying that T_{CCO} can be retrieved from y_1 with first-order shaped T_{q1}, which can be filtered by a decimation filter.

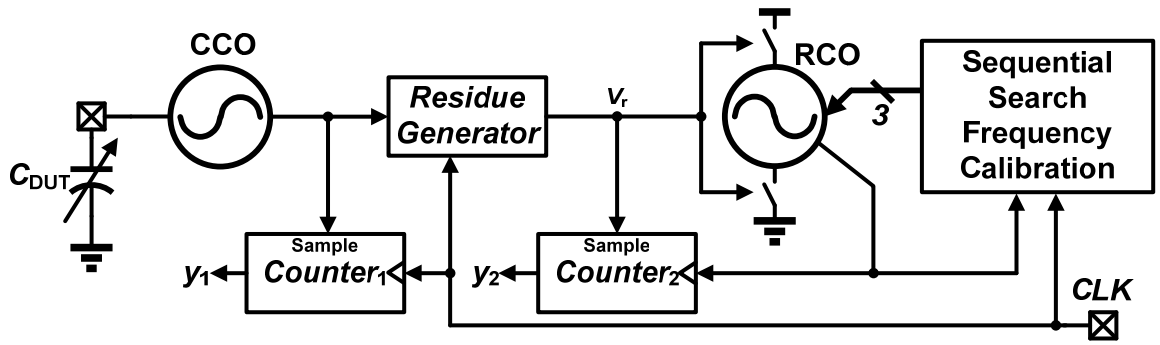

Fig. 4.1 The schematic of the proposed oscillator-based CDC.

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In addition, to further reduce the quantization error, a residue generator is utilized to generate a residue timing signal (V_r) with a pulse-width of

$$T_r[n] = 2 \cdot T_{CLK} - T_{q1}[n], \tag{4.3}$$

gating the oscillation of the RCO. The grey line in Fig. 4.2 illustrates the waveform of the RCO. When V_r goes high, the RCO starts to oscillate with a period proportional to the product of its resistance and capacitance. When V_r goes low, the charging and discharging paths of the capacitor in RCO are cut off. The voltage of the capacitor is held, while the phase of the RCO remains until V_r goes high. More details of the RCO operation will be presented in 4.3.2. It is noted that a constraint on the minimal T_{CCO} is added to the residue generator in order to avoid the generation of a nearly zero pulse width. As a result, the period of T_{CCO} is defined to be at least three times greater than T_{CLK}.

Triggered by the output of RCO, *Counter*2 is utilized to count the number of rising edges during the period of the residue waveform (V_r) and the output can be expressed as

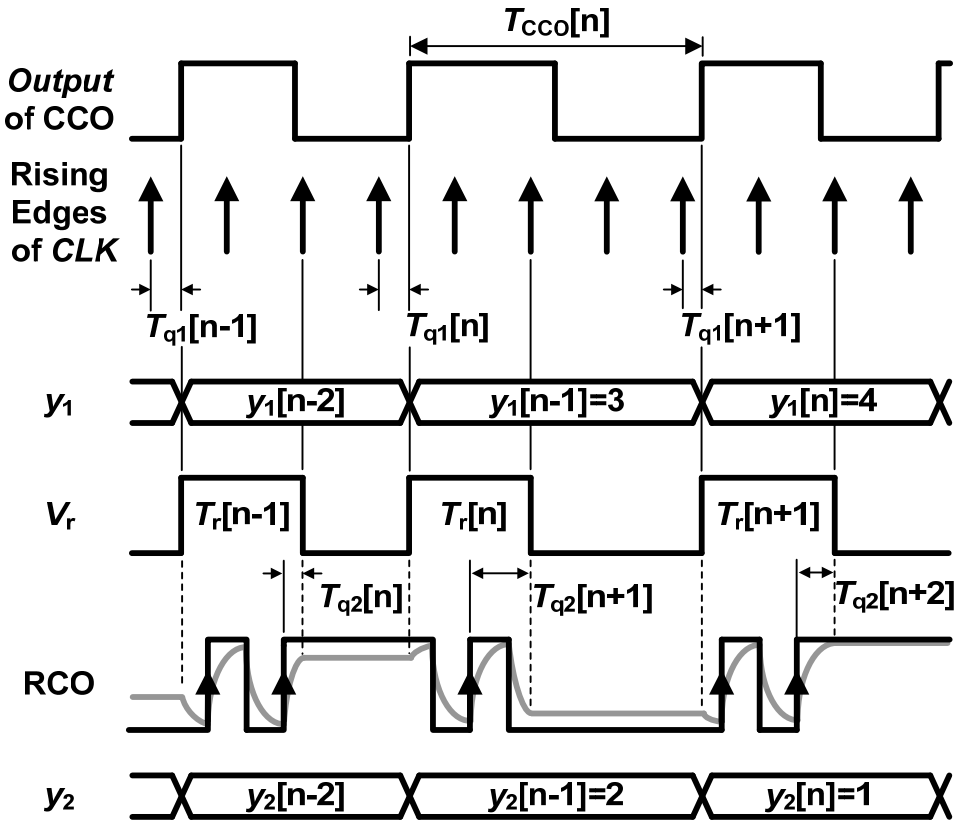

Fig. 4.2 The timing diagram of the proposed CDC.

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$$y_2[\mathrm{n}] = \frac{1}{T_{\mathrm{RCO}}}\left(T_{\mathrm{r}}[\mathrm{n}] + T_{\mathrm{q2}}[\mathrm{n}] - T_{\mathrm{q2}}[\mathrm{n}+1]\right), \tag{4.4}$$

where T_{RCO} is the period of the RCO output waveform and T_{q2} is defined as the quantization error of T_{r}. Applying (4.3) to (4.4), the Z-transform of the result is given by

$$Y_2[\mathrm{z}] = \frac{1}{T_{\mathrm{RCO}}} \cdot \left[2 \cdot T_{\mathrm{CLK}} - Y_{\mathrm{q1}}[\mathrm{z}] - \mathrm{z} \cdot \left(1 - \mathrm{z}^{-1}\right) \cdot Y_{\mathrm{q2}}[\mathrm{z}]\right]. \tag{4.5}$$

By assuming $T_{\mathrm{RCO}} = k \cdot T_{\mathrm{CLK}}$ and combining $y_1[\mathrm{n}]$ and $y_2[\mathrm{n}]$ in the form of $y_1[\mathrm{n}] + \mathrm{k} \cdot (y_2[\mathrm{n}] - y_2[\mathrm{n+1}])$, the Z-transform of the result from (4.1)–(4.5) is given by

$$Y_{\mathrm{CCO}}[\mathrm{z}] = T_{\mathrm{CLK}} \cdot \left[Y_1[\mathrm{z}] + k \cdot (1 - \mathrm{z}) \cdot Y_2[\mathrm{z}]\right] + \mathrm{z}^2 \cdot \left(1 - \mathrm{z}^{-1}\right)^2 \cdot Y_{\mathrm{q2}}[\mathrm{z}], \tag{4.6}$$

which implies that T_{CCO} can be retrieved from y_1, y_2 and a second-order shaped T_{q2}. As the second-order shaped quantization noise is filtered by a decimation filter, the capacitance of C_{DUT} can be obtained with improved precision.

The theoretical signal-to-noise ratio (SNR) can be obtained by using a similar method to that of a second-order delta-sigma ADC in [53]. The quantization noise power of the second-order shaped T_{q2} is given by

$$P_{\mathrm{q2}} \cong \frac{k^2 \cdot {T_{\mathrm{CLK}}}^2 \cdot \pi^4}{60} \left(\frac{f_{\mathrm{BW}}}{f_{\mathrm{CCO}}/2}\right)^5, \tag{4.7}$$

where f_{BW} is the bandwidth of an ideal sinc filter for decimation, and f_{CCO} is the oscillating frequency of the CCO. The signal power is defined as

$$P_{\mathrm{s}} = \frac{1}{2}\left(\frac{\Delta T_{\mathrm{CCO}}}{2}\right)^2, \tag{4.8}$$

where ΔT_{CCO} is the difference between the period of CCO for maximum and minimal C_{DUT}. Consequently, the SNR can be estimated as

$$\mathrm{SNR} = 10 \cdot \log_{10}\left(P_{\mathrm{s}}/P_{\mathrm{q2}}\right) = 20 \cdot \log_{10}\left(\Delta T_{\mathrm{CCO}}/T_{\mathrm{CLK}}\right) - 11.14 - 20 \cdot \log_{10} k + 50 \cdot \log_{10}\left(\frac{f_{\mathrm{CCO}}/2}{f_{\mathrm{BW}}}\right). \tag{4.9}$$

The last term in (4.9) indicates that halving f_{BW} improves the SNR for a second-order modulator by

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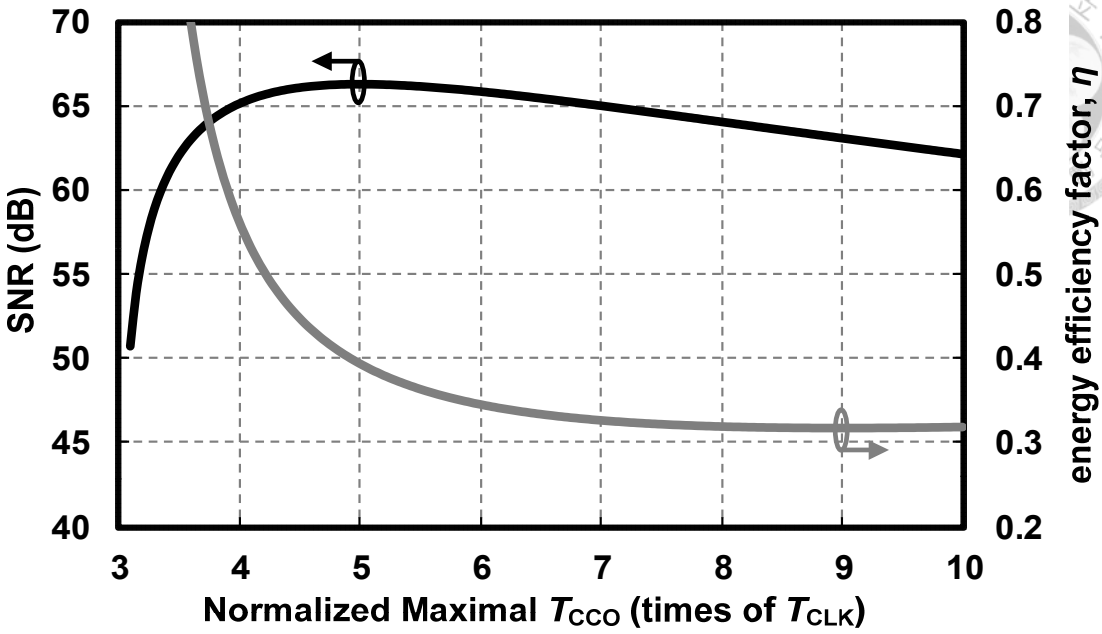

Fig. 4.3 The estimated SNR and energy efficiency factor with different maximum T_{CCO}.

15 dB, which is the same as a second-order delta-sigma ADC. In addition, the SNR also benefits by increasing f_{CCO}. Fig. 4.3 shows the estimated SNR from (4.9) with different maximum T_{CCO} which is normalized to T_{CLK} under the conditions that $k = 3$, $T_{CLK} = 300$ ns, and $f_{BW} = 8$ kHz. In addition, the power consumption of the CDC is proportional to f_{CCO}. The energy efficiency of CDC can be estimate by introducing an energy efficiency factor given by

$$\eta = \frac{1}{T_{CCO\_max}/T_{CLK}} \Big/ 2^{(SNR-1.76)/6.02}, \tag{4.10}$$

which is proportional to the required energy for per conversion step. The estimated SNR peaks when maximum T_{CCO} equals $5 \cdot T_{CLK}$, and η hits the minimum when maximum T_{CCO} equals $9 \cdot T_{CLK}$.

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4.2 Non-Ideal Effects

There are several non-ideal effects degrading the performance of proposed CDC, such as jitter due to circuit noise and process variations. To have better understanding on the design constraints, these effects associated with the individual building blocks are discussed in this section.

4.2.1 Jitter of CCO

The CCO provides a timing signal with a period proportional to the capacitance of C_{DUT}. Therefore, the jitter of the CCO is indistinguishable from the actual input signal. To simplify the analysis, jitter with a Gaussian probability density function is taken into account and the noise power contributed by the jitter of the CCO is given by

$$P_{n\_CCO} = \tau_{CCO}^{\ 2} \cdot \frac{f_{BW}}{f_{CCO}/2}, \tag{4.11}$$

where τ_{CCO} is the root-mean-square (rms) jitter of the CCO. It is noted that only the noise power with a frequency lower than f_{BW} affects the output accuracy as a decimation filter is applied to y_1.

4.2.2 Jitter of *CLK*

Based on (4.1), y_1 is inversely proportional to period of the external clock (*CLK*), and the fluctuation of T_{CLK} has direct impact on the CDC output. The noise contribution of clock jitter is expressed as

$$P_{n\_CLK} = \tau_{CLK}^{\ 2} \cdot \frac{f_{CLK}}{f_{CCO}} \cdot \frac{f_{BW}}{f_{CCO}/2}, \tag{4.12}$$

where f_{CLK} and τ_{CLK} are the frequency and rms jitter of *CLK*, respectively. In contrast with P_{n_CCO}, P_{n_CLK} increases with the ratio of f_{CLK} and f_{CCO}. As the ratio becomes larger, more transition edges of *CLK* are accountable for the noise contribution at the CDC output.

4.2.3 Jitter of RCO

According to the operation principles of the proposed CDC, y_1 is influenced by the jitter of CCO while y_2 is vulnerable to the jitter of RCO. As y_2 multiplied by (1-z) is presented at the output of the

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CDC, the noise contributed by the jitter of the RCO is also first-order shaped. The noise power is given by

$$P_{\text{n\_RCO}} = \tau_{\text{RCO}}^{\,2} \cdot \frac{\alpha \cdot f_{\text{RCO}}}{f_{\text{CLK}}} \cdot \frac{\pi^2}{3} \left(\frac{f_{\text{BW}}}{f_{\text{CCO}}/2} \right)^3, \tag{4.13}$$

where τ_{RCO} is the rms jitter of the RCO and α is the ratio of average T_{r} to T_{CLK}, which is 1.5 in this particular CDC design as the average T_{q1} equals $0.5 \cdot T_{\text{CLK}}$.

4.2.4 Period Deviation between $k \cdot T_{\text{CLK}}$ and T_{RCO}

The Z-transform in (4.6) is obtained based on the assumption $T_{\text{RCO}} = k \cdot T_{\text{CLK}}$. However, due to process variations and device parasitics, it is inevitable that T_{RCO} may deviate from the design value as the circuits are fabricated. With k' denoting the actual ratio of T_{RCO} to T_{CLK} for the fabricated circuit, (4.6) can be rewritten as

$$Y_{\text{CCO}}[\text{z}] = T_{\text{CLK}} \cdot \left[Y_1[\text{z}] + k \cdot (1-\text{z}) \cdot Y_2[\text{z}] \right] + \text{z} \cdot \left(1-\text{z}^{-1}\right) \cdot Y_{\text{q1}}[\text{z}] \cdot (1-k/k') + \text{z}^2 \cdot \left(1-\text{z}^{-1}\right)^2 \cdot Y_{\text{q2}}[\text{z}] \cdot (k/k'), \tag{4.14}$$

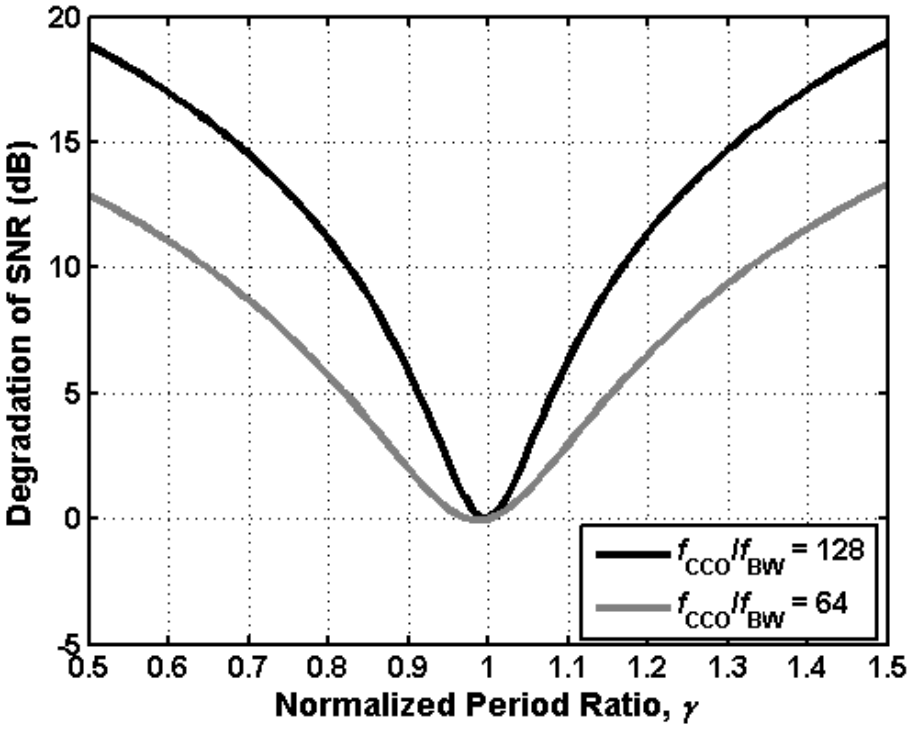

Fig. 4.4 The degradation of SNR with different γ.

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indicating that the period deviation of the RCO results in the remaining first-order shaped quantization noise power. The associated noise power can be calculated in the same way as in (4.7), leading to the expression as

$$P_{q1} \cong \frac{{T_{CLK}}^2 \cdot \pi^2}{36} \left(\frac{f_{BW}}{f_{CCO}/2} \right)^3 . \tag{4.15}$$

Fig. 4.4 shows the degradation of SNR due to period deviation from (4.7)–(4.8) and (4.14)–(4.15), where γ is defined as the ratio of k/k'. Fig. 4.4 indicates that γ needs to be confined within the range from 0.95 to 1.05 in order to keep the loss of resolution smaller than 0.5 bit, which can be achieved by adopting a sequential search frequency calibration (SSFC) in the proposed CDC circuit.

4.2.5 Leakage and Dead-Zone of the Gated RCO

Due to current leakage of the gating switches and charge sharing between parasitic capacitors, the phase of the RCO varies during gating. This variation can be reduced by increasing the capacitance of the RCO and by utilizing devices with a high threshold voltage as the gating switches. In addition, dead-zones are typically observed in the transfer characteristics of a gated oscillator at integer multiples of the oscillating period as described in [54]. In the proposed CDC, the input of gated

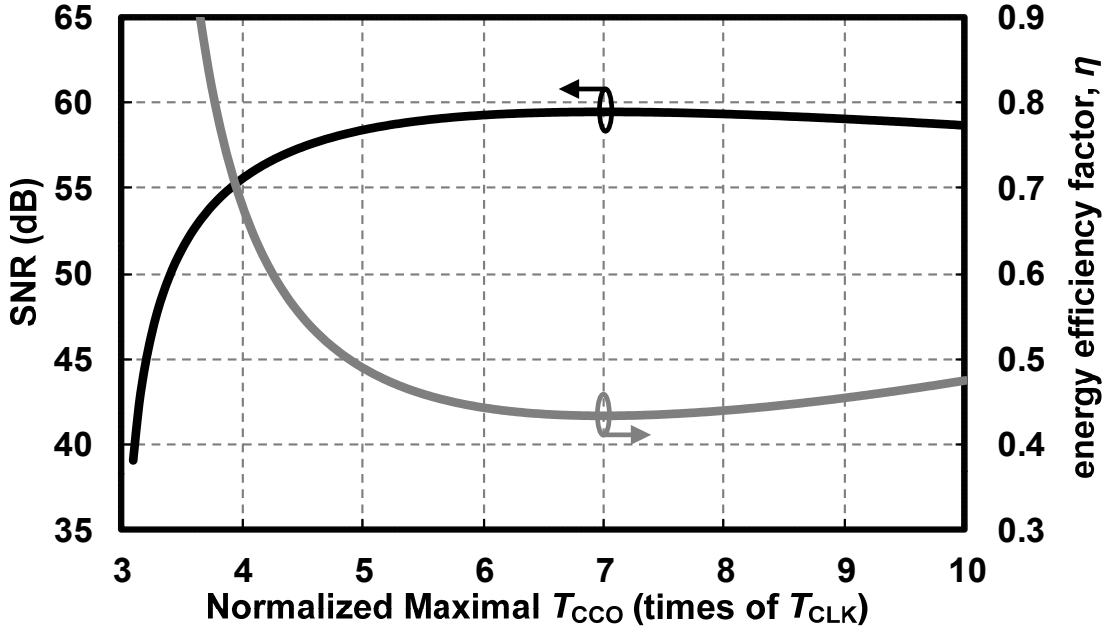

Fig. 4.5 The estimated SNR and energy efficiency factor with different normalized maximum T_{CCO} considering the non-ideal effects.

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Table 4.1 Parameters for a Typical Case

Parameter	Value
T_{CLK}	300 nsec
f_{BW}	8 kHz
k	3
γ	0.95
minimal T_{CCO}	900 nsec
τ_{CCO}	$T_{CCO}/1000$
τ_{CLK}	$T_{CLK}/10000$
τ_{RCO}	$k \cdot T_{CLK}/1000$

RCO is equivalently the quantization error of the CCO, which has a value between T_{CLK} and $2 \cdot T_{CLK}$. By choosing the design value $k = 3$, the input of the gated RCO is within the range between $1/3 \cdot T_{RCO}$ and $2/3 \cdot T_{RCO}$ such that the dead-zone can be generally avoided.

4.2.6 Estimated SNR with Non-Ideal Effects

After elaborating several important non-ideal effects, the estimated SNR is reexamined versus the maximum T_{CCO}. The total noise power by taking the non-ideal effects into account is given by

$$P_{n\_total} = P_{n\_CCO} + P_{n\_CLK} + P_{n\_RCO} + (1-\gamma)^2 \cdot P_{q1} + \gamma^2 \cdot P_{q2}. \quad (4.16)$$

With the typical parameters listed in Table 4.1 as an example, the estimated SNR with different normalized maximum T_{CCO} is shown in Fig. 4.5. It is noted that, based on the above assumptions and derivations of the non-ideal effects, the SNR and η reach their maximum and minimum values, respectively, as the maximum T_{CCO} equals $7 \cdot T_{CLK}$.

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4.3 Circuit Implementation of the Proposed CDC

4.3.1 Capacitor-Controlled Oscillator

Fig. 4.6 shows the schematic of the CCO, which consists of a bias circuit, a current-mode comparator (CMC) [55], a voltage-mode comparator (VMC), R_0 and C_0, while C_{DUT} represents the capacitance of the device under test. It is noted that the start-up in the bias circuit is omitted in the circuit schematic. The CMC, R_0 and C_0 form a relaxation oscillator as proposed in [56], possessing the advantage of non-susceptibility to the variations of the bias current. However, it is vulnerable to the mismatch between M_{p1} and M_{p2}. Special care has to be taken in choosing the device size and generating the device layout. In addition, the noise rejection of the relaxation oscillator also benefits from the use of the CMC.

The gate bias of M_{p1} in Fig. 4.6 is provided by a constant-g_m circuit. As the current I_1 generated by M_{p1} flows through the resistance R_0, the voltage drop V_R is used for voltage comparison. In the circuit implementation, M_{p2} generates the current $I_2 = 4 \cdot I_1$ to charge the capacitance of C_0 and C_{DUT}.

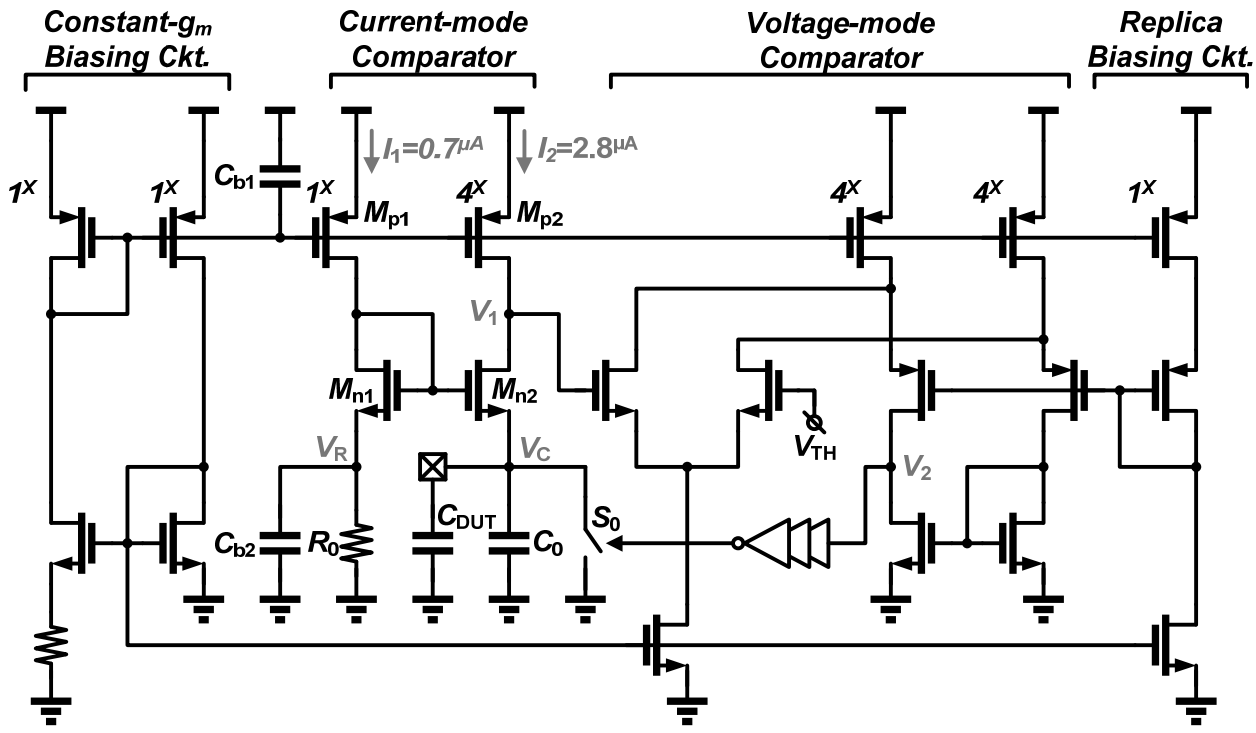

Fig. 4.6 The schematic of the capacitor-controlled oscillator.

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When the value of V_C exceeds that of V_R, M_{n2} is turned off and the current I_2 starts to charge the parasitic capacitor at the drain of M_{n2} and the input capacitance of the VMC. As the voltage at V_1 exceeds V_{TH}, V_2 goes low and the capacitors C_0 and C_{DUT} are discharged by turning on S_0. The resulting period of the CCO is given by

$$T_{CCO} = R_0 \cdot (C_0 + C_{DUT})/4 + \tau, \tag{4.17}$$

where τ is the delay of comparators, which is less than 1% of the T_{CCO}. In addition, the variation of τ for different values of C_{DUT} is about 0.16% of the time difference between the maximum T_{CCO} and minimum T_{CCO}.

In a conventional relaxation oscillator, the VMC is directly connected to the top plates of C_0 and C_{DUT}. The jitter of oscillator can be estimated by dividing the total voltage noise at the top plates of C_0 and C_{DUT} by the ascending slope of V_C, while the total noise is considered the combination of input-referred voltage noise of the VMC and the voltage noise generated by the charging current and the equivalent impedance of C_0 and C_{DUT}. The simulated waveforms of V_1 and V_C near the transition of V_2 are shown in Fig. 4.7, where s_1 and s_2 are the values of the ascending slopes of V_1 and V_C, respectively. Based on the simulation results, s_1 is approximately 5.5 times larger than s_2. Together with the simulated noise voltages as depicted in Fig. 4.8, it is observed that by changing the input of the VMC from V_C to V_1, the jitter generated by input-referred voltage noise of the VMC is suppressed by the ratio of s_1 to s_2. As a result, the jitter of the CCO is dominated by the noise of the CMC, which can be effectively reduced by adding additional capacitors C_{b1} and C_{b2} in Fig. 4.6.

Based on the design guidelines of the CDC, T_{CCO} should be designed within the range from $3 \cdot T_{CLK}$ to $6 \cdot T_{CLK}$ by taking the corresponding input range of C_{DUT} into account. However, considering the overall power consumption, a maximum T_{CCO} of $10 \cdot T_{CLK}$ is chosen in this particular design without significant degradation of the SNR. The simulated transfer curve of T_{CCO} to C_{DUT} and the period deviation compared with a linear regression line are depicted in Fig. 4.9.

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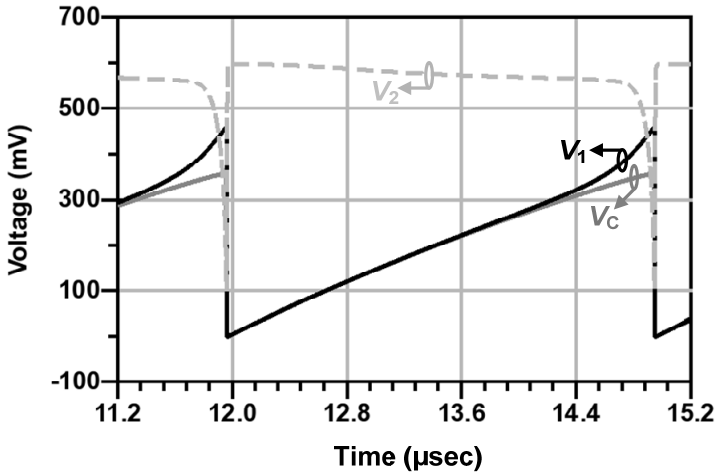
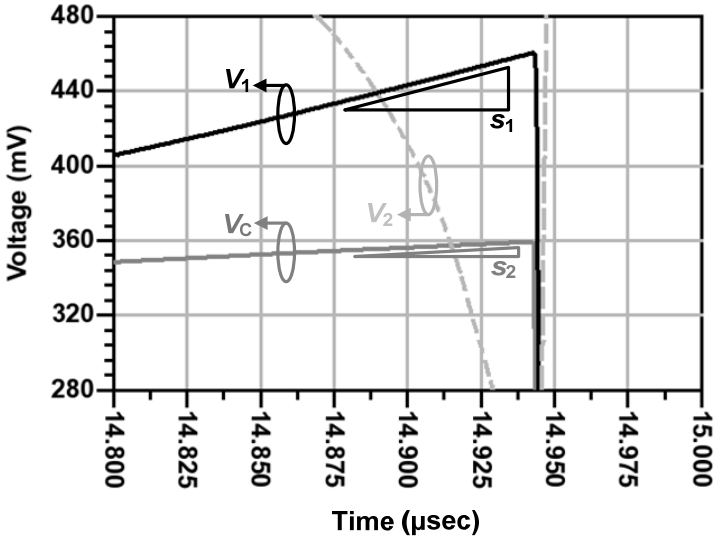


(a)



(b)

Fig. 4.7 (a) Simulated waveforms of V_C, V_1 and V_2 and (b) waveforms near the transition of V_2.

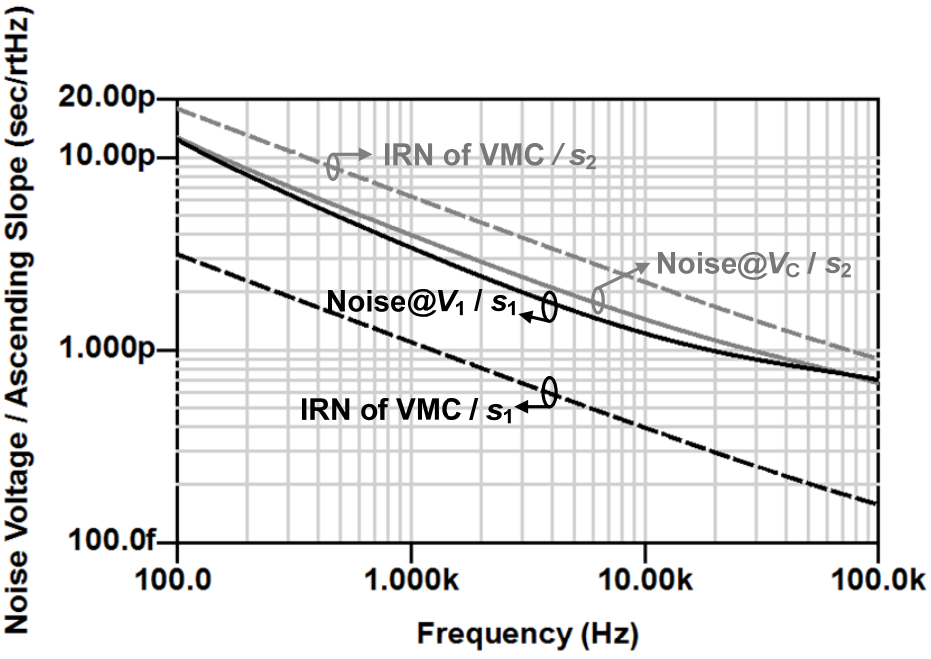


Fig. 4.8 The simulated noise voltages at V_1/V_C and the input-referred noise of VMC divided by ascending slopes.

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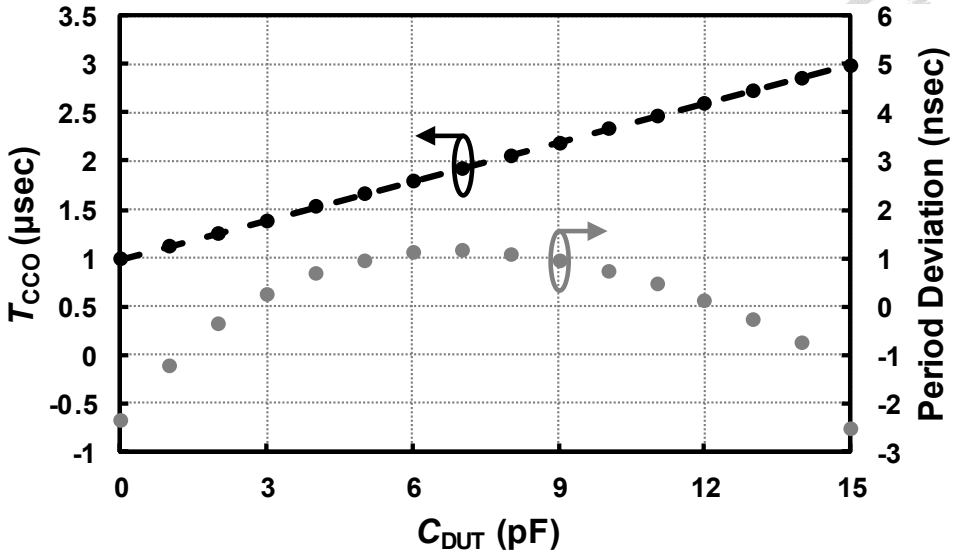

Fig. 4.9 The simulated transfer curve of T_{CCO} to C_{DUT} and the period deviation compared with a linear regression line.

4.3.2 Gated RCO

Fig. 4.10 shows the schematic of the gated RCO, which is composed of a single-pole-double-throw (SPDT) switch, R_1, C_1 and a hysteresis inverter [57]. The inverter compares V_{C1} with two threshold voltages V_H and V_L, while the result toggles the SPDT switch between V_{DD} and ground, leading to exponential charging/discharging of V_{C1} to V_{DD} and ground, respectively. The illustrated waveform of V_{C1} is shown in Fig. 4.11. The associated period T_{RCO} can be expressed as

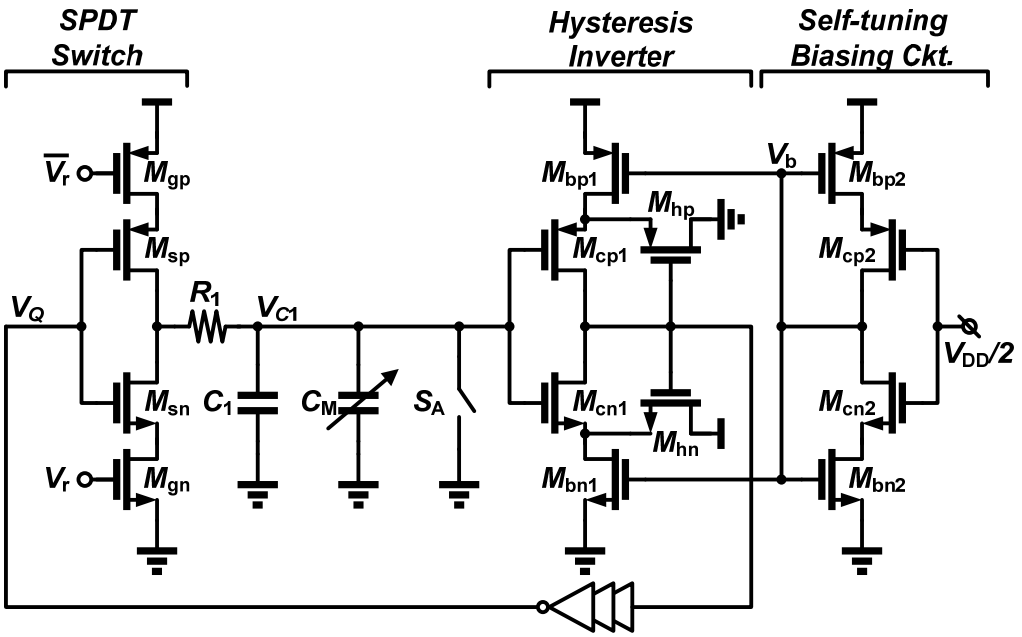

Fig. 4.10 The schematic of the gated RCO

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$$T_{\mathrm{RCO}} = 2 \cdot R_1 \cdot C_1 \cdot \ln\left(1 + \frac{V_{\mathrm{H}} - V_{\mathrm{L}}}{\Delta V}\right), \tag{4.18}$$

by assuming $V_{\Delta H} = V_{\Delta L} = \Delta V$.

The phase error during gating is mainly resulted from the leakage current flowing through the SPDT switch. Fig. 4.12 shows the equivalent circuit models of the SPDT switch when gated, where R_{up} is the equivalent series resistance of M_{gp} and M_{sp}, and R_{dn} is the equivalent series resistance of M_{gn} and M_{sn}. The value of R_{up} and R_{dn} dominate the time constant of the leakage as shown in Fig. 4.12. In order to reduce the gating error, the values of R_{up} and R_{dn} are designed to be at least 300 times larger than that of R_1.

As mentioned in 4.2.4, the period deviation between $3 \cdot T_{CLK}$ and T_{RCO} leads to degradation in the SNR. A self-tuning biasing circuit [58]−[59] and a 3-bit controlled capacitor array C_M, are added to compensate for the period deviation due to process variation. C_M is designed to provide a ±17.5% period tuning capability in the vicinity of the center frequency of RCO. The Monte Carlo simulated results of T_{RCO} are shown in Fig. 4.13 with 3-σ upper and lower limits. The 3-σ limits both fall into

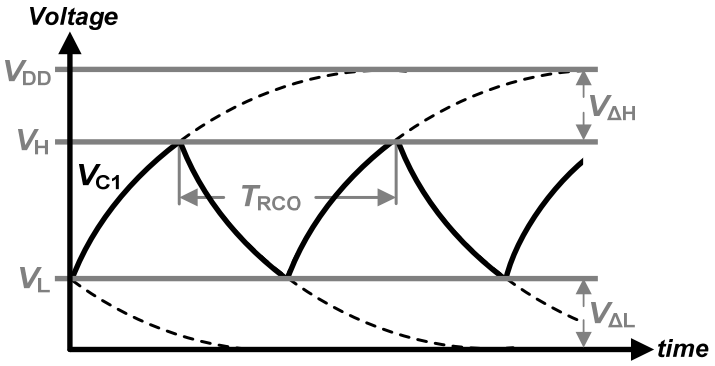

Fig. 4.11 The illustrated waveform of V_{C1}.

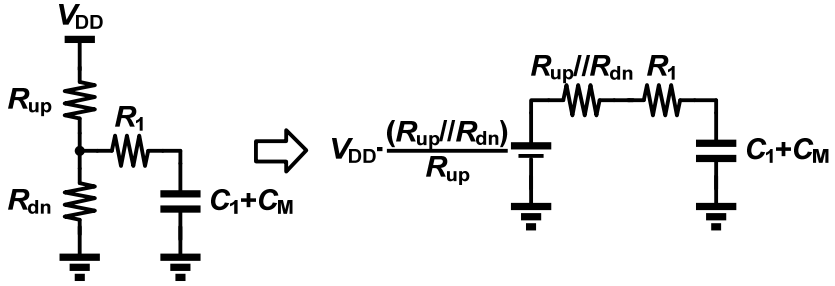

Fig. 4.12 Equivalent circuit models of the SPDT switch with R_1 and C_1 when gated.

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the grey region representing ±10% period deviation, which means that in most cases the worst period deviation can be confined within 10% by connecting/disconnecting all capacitors in C_M.

4.3.3 Sequential Search Frequency Calibration

To further decrease the period deviation, a SSFC is adopted in the CDC design. The basic idea of the frequency calibration is comparing the value of $3 \cdot T_{CLK}$ and T_{RCO} by counters, which can be realized by binary ripple counters. By adopting the switch S_A as shown in Fig. 4.10, the timing of *CLK* and output of RCO can be properly aligned for comparison. The flow chart and the circuit diagram of the SSFC are shown in Fig. 4.14 and Fig. 4.15, respectively. In this particular design, an off-line calibration scheme is employed, and a control signal *Cal* is used to enable the frequency calibration.

At the initial state, the control bits of the capacitor array C_M is selected by a multiplexer controlled by *Cal* to be N<2:0>, which value is set to 000. Then S_A is switched off, and the RCO starts to oscillate. The comparison of period is drawn between $12 \cdot T_{CLK}$ and $4 \cdot T_{RCO}$ for enhanced precision. At the end of the 12th period of *CLK*, the MSB of the *OSC Counter* is observed. For the case of MSB = 1, the time interval of $4 \cdot T_{RCO}$ is shorter than that of $12 \cdot T_{CLK}$. N<2:0> is carried and an additional unit capacitor in C_M is connected to the RCO. As a result, T_{RCO} increases accordingly and the

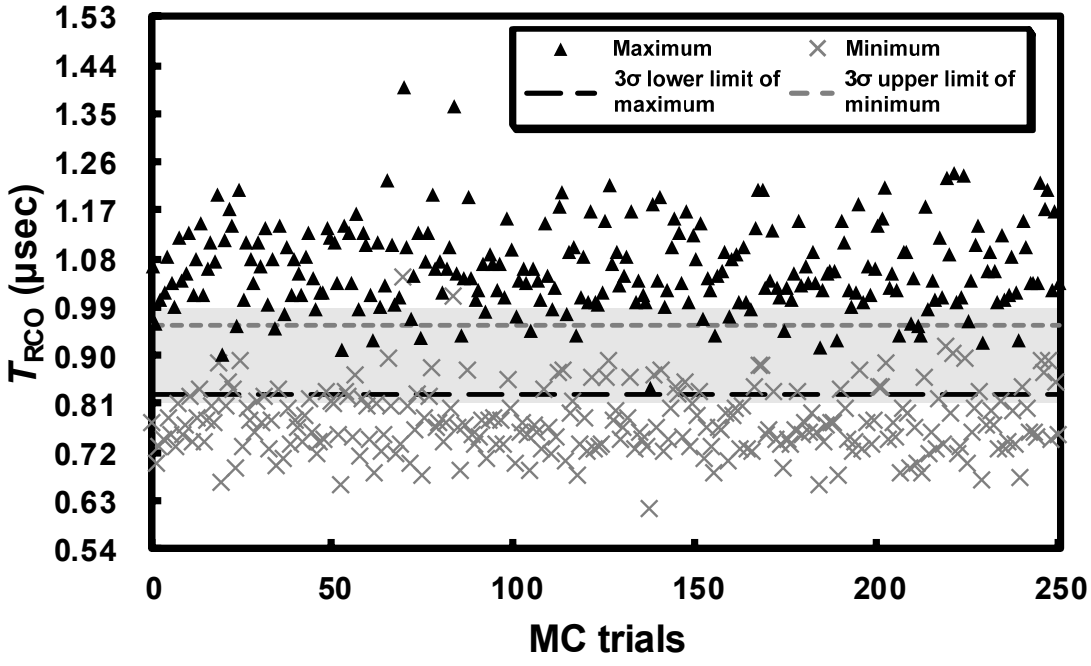

Fig. 4.13 The Monte Carlo simulated results of T_{RCO}.

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comparison is repeated after resetting the *OSC Counter* and the *CLK Counter*. Once the MSB becomes 0 or *N*<2:0> reaches its maximum count at the end of the 12th period of *CLK*, *Fin* rises to high level and generates a flag bit *Flag* to indicate the end of calibration. Finally, the *Register* memorizes the current state of *N*<2:0> and the code is stored in *M*<2:0>. To have a better understanding

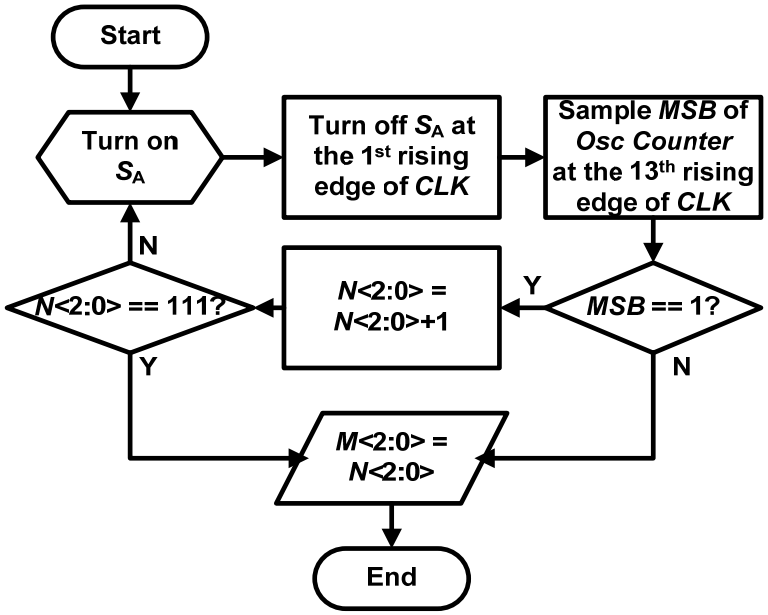

Fig. 4.14 The flowchart of the sequential search frequency calibration.

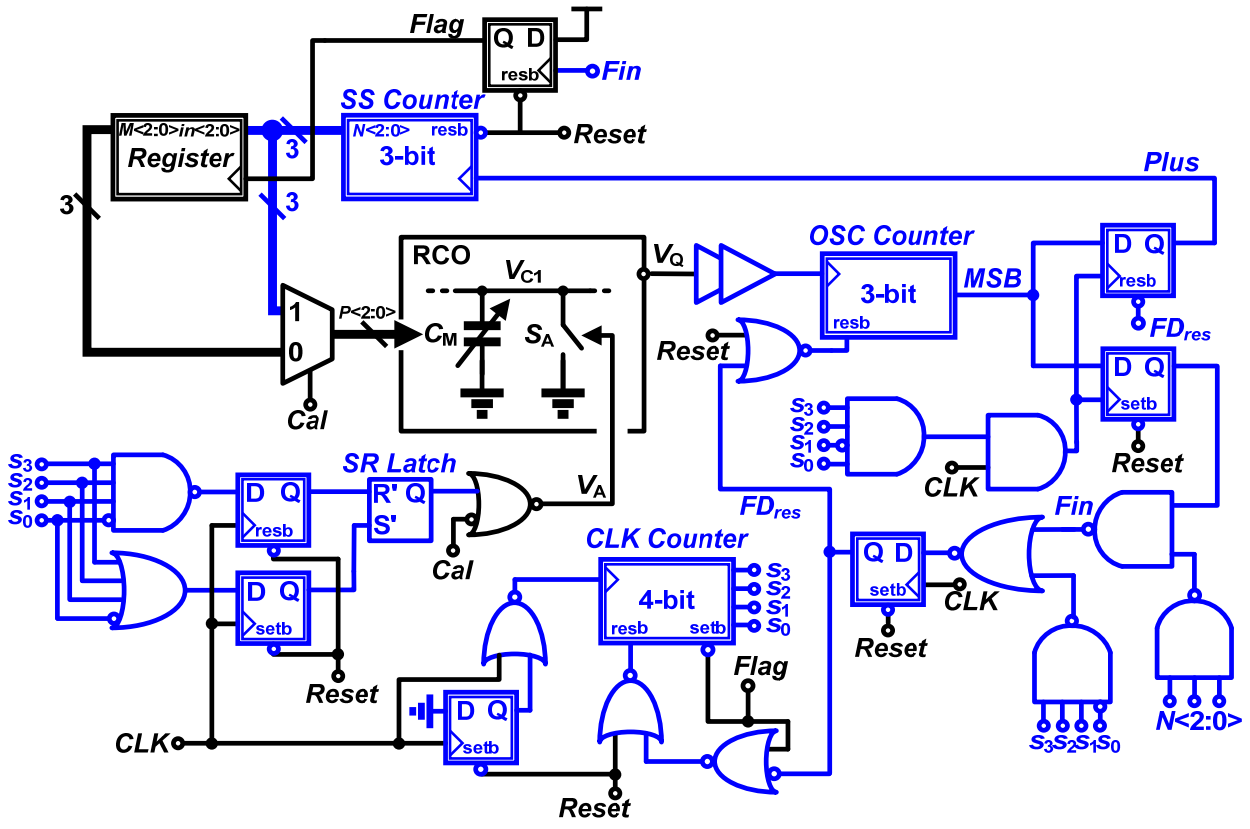

Fig. 4.15 The circuit diagram of sequential search frequency calibration.

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of how the SSFC works, the timing diagrams with a final state N<2:0> of 001, as an example, are depicted in Fig. 4.16.

Note that most of the building blocks as indicated in Fig. 4.15 are for off-line calibration and can be shut down after the calibration procedure is completed for power saving and noise reduction purposes. The control bits of C_M are switched to M<2:0> by setting Cal = 0. It is also worth mentioning that the maximum number of required reference clock cycles to complete calibration is 103. By designing the unit incremental step of C_M to be 5% of T_{CLK}, the maximum period deviation can be limited within 5% by SSFC, which keeps the degradation of CDC resolution smaller than 0.5 bit as presented in Fig. 4.4.

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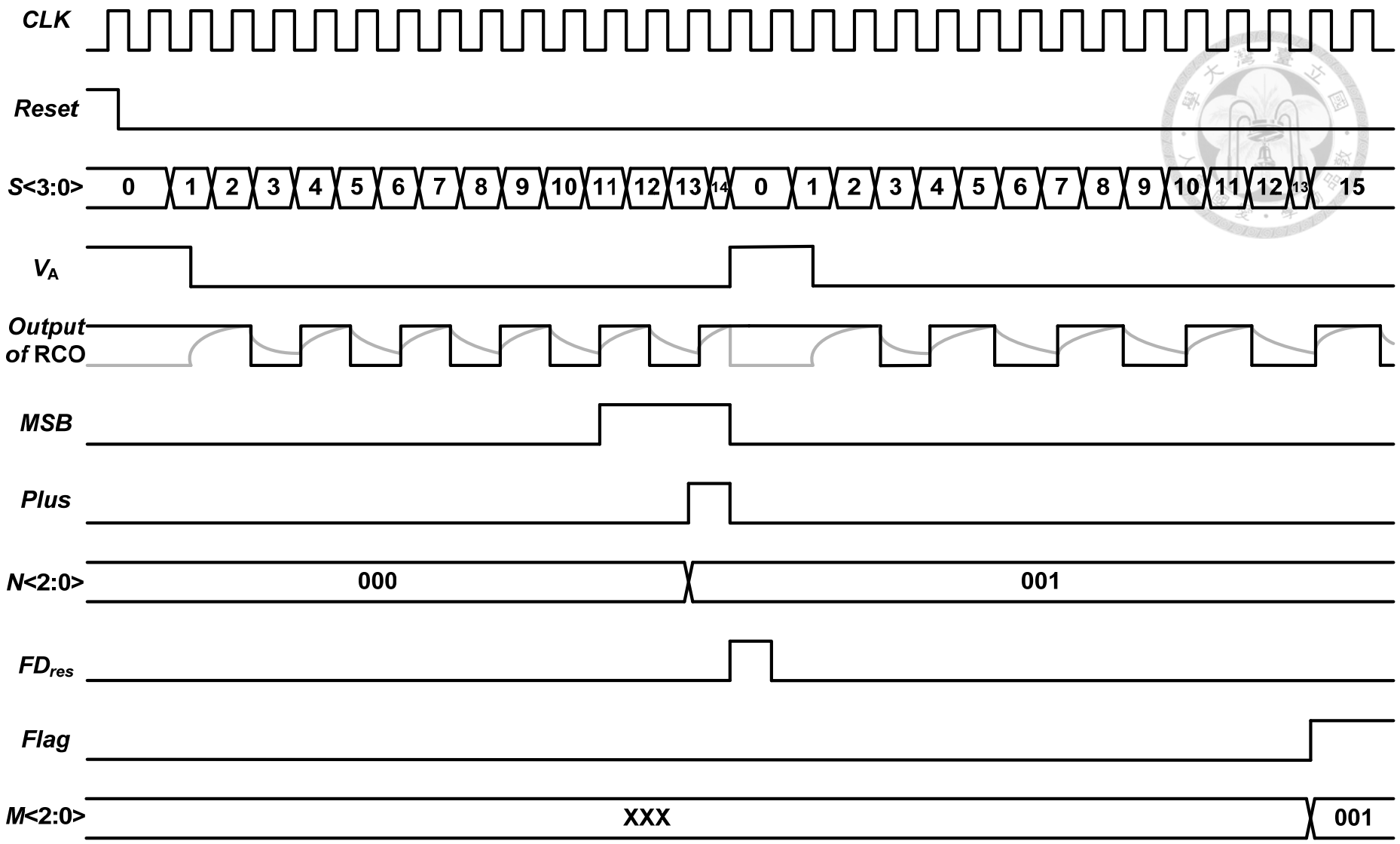

Fig. 4.16 The timing diagram of SSFC with a final state *N*<2:0> of 001.

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4.3.4 Residue Generator and Counters

Fig. 4.17(a) shows the circuit schematic of the residue generator, where *CLK*' is the inverted *CLK*. Both *Counter*$_1$ and *Counter*$_2$ are realized by Johnson counter as shown in Fig. 4.17(b) and (c), respectively. To reduce the number of I/O pads, an on-chip decoder is also included to the output bits of *Counter*$_1$ for generation of a 4-bit binary code.

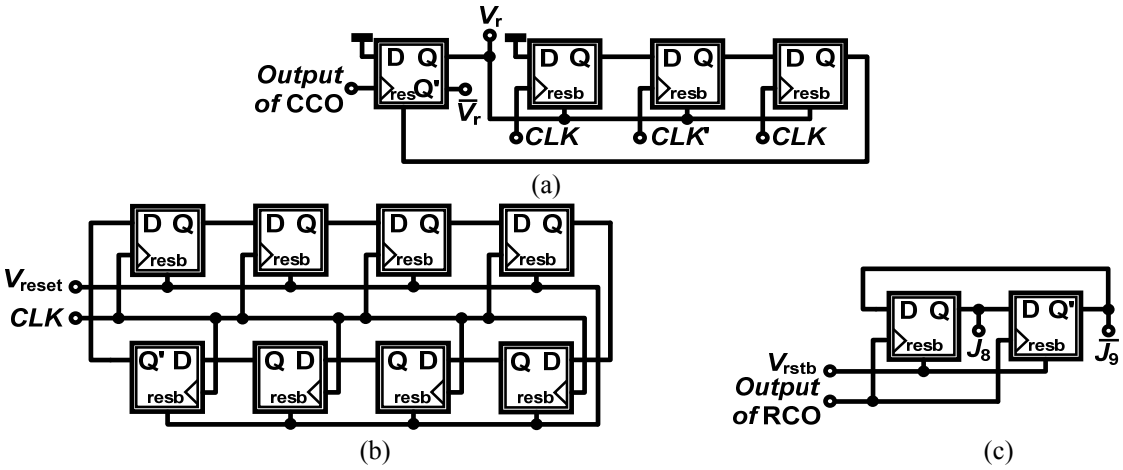

Fig. 4.17 The circuit schematics of (a) residue generator, (b) *Counter*$_1$ and (c) *Counter*$_2$.

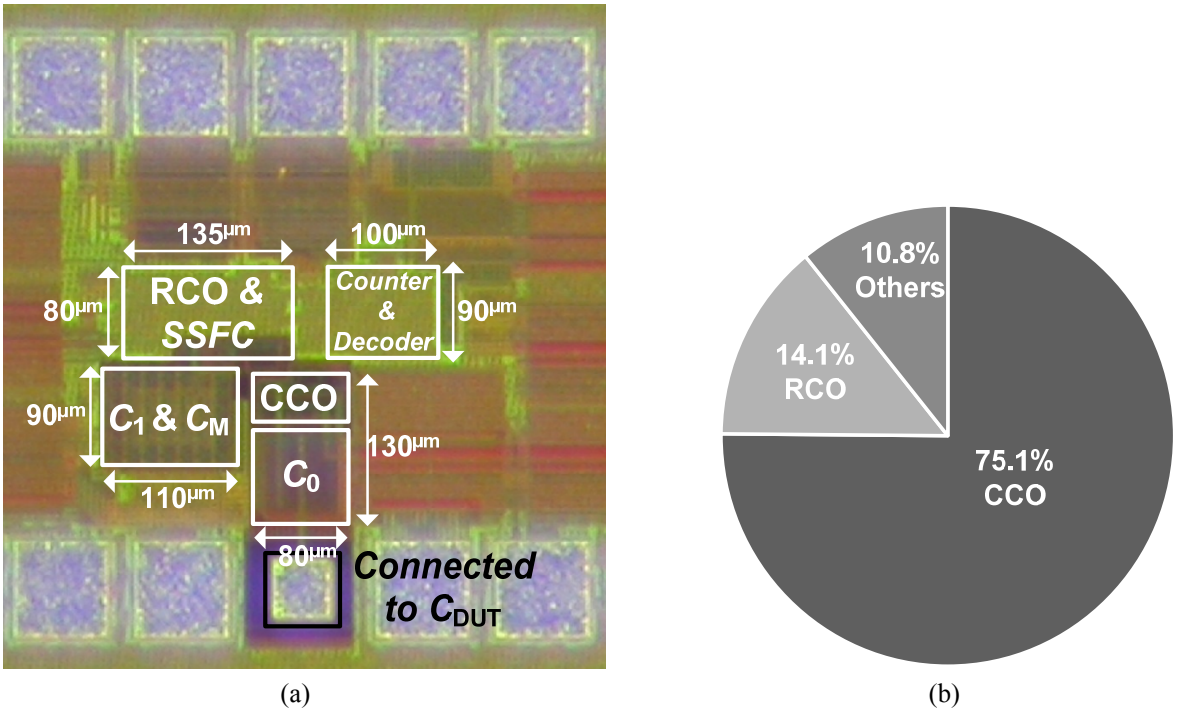

Fig. 4.18 (a) The microphotograph of the fabricated circuit and (b) the power breakdown diagram.

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4.4 Measurement Results

The proposed CDC is fabricated by using a standard 1P9M 90-nm CMOS process. Fig. 4.18 (a) shows the microphotograph of the fabricated circuit with a chip area of 0.051 mm^2 for core circuitry. Tested at a T_{CLK} of 300 ns, the CDC consumes a total power of 8.04 μW from a supply voltage of 0.6 V as the SSFC is shut down and measurement buffers are excluded. Fig. 4.18 (b) shows the power breakdown diagram. The measurement setup is shown in Fig. 4.19, where the CDC chip is bonded with a printed circuit board (PCB) for testing. A Keysight B2926A Power Source is used to provide the supply voltage and biasing voltages for the CDC, and a Keysight 33622A Waveform Generator is used to provide the 0.6-V 300-ns *CLK*.

An Agilent 53220A Universal Frequency Counter/Timer is used to characterize the period and rms jitter of the oscillators. Fig. 4.20 shows the measured T_{RCO} and rms jitter versus the control bits of C_M. Though the measured T_{RCO}, in this particular case, is generally lower than the designed value due to process variations, the RCO still provides a period deviation less than 5%, which is within the range of the SSFC coverage. In order to verify the proposed calibration function, the waveforms

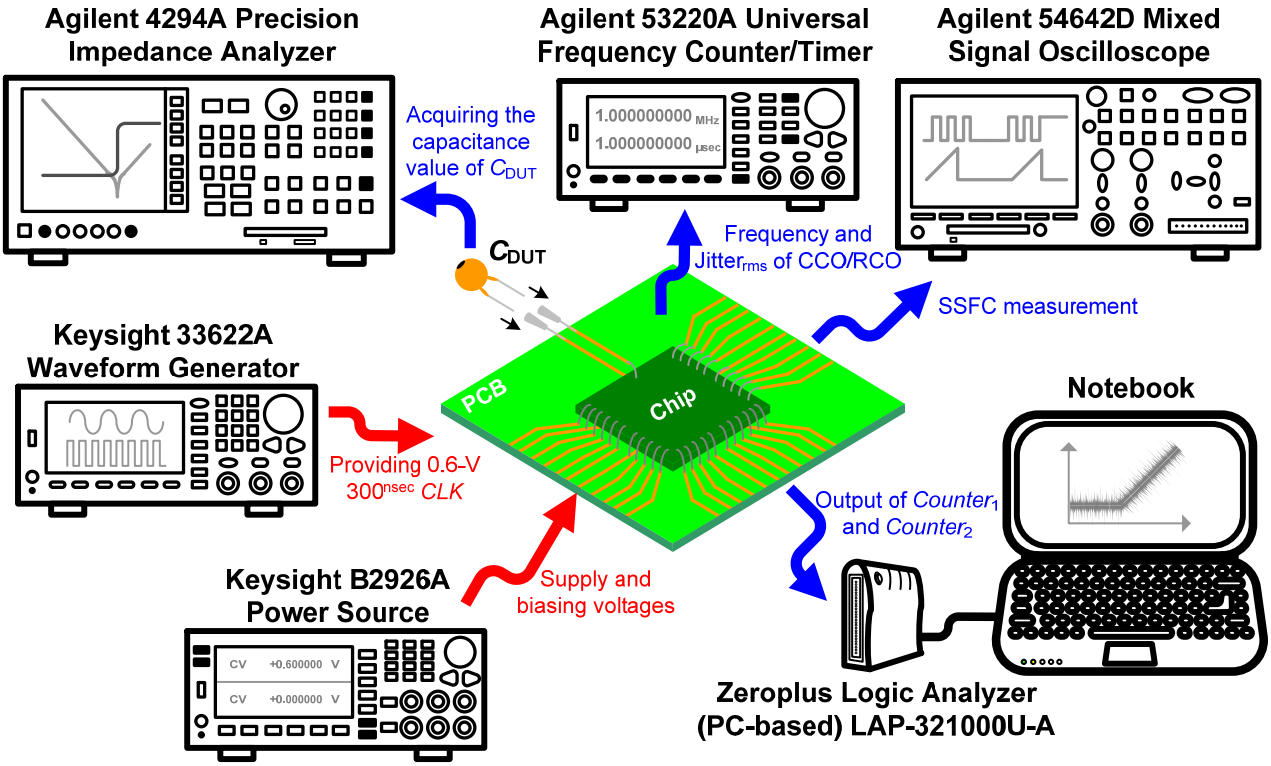

Fig. 4.19 The measurement setup.

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of the RCO and SSFC are characterized by an Agilent 54642D Mixed-Signal Oscilloscope, where *CLK* and *Reset* are measured by the analog channels while the other signals are measured by the logic channels. Fig. 4.21 shows the measurement results with T_{CLK} = 300 ns. As indicated in Fig. 4.21, SSFC starts as *Reset* goes low, while *P*<2:0>, the control bits of C_M, are switched to *N*<2:0> by the multiplexer and increase successively. It is observed that the period T_{RCO} increases with

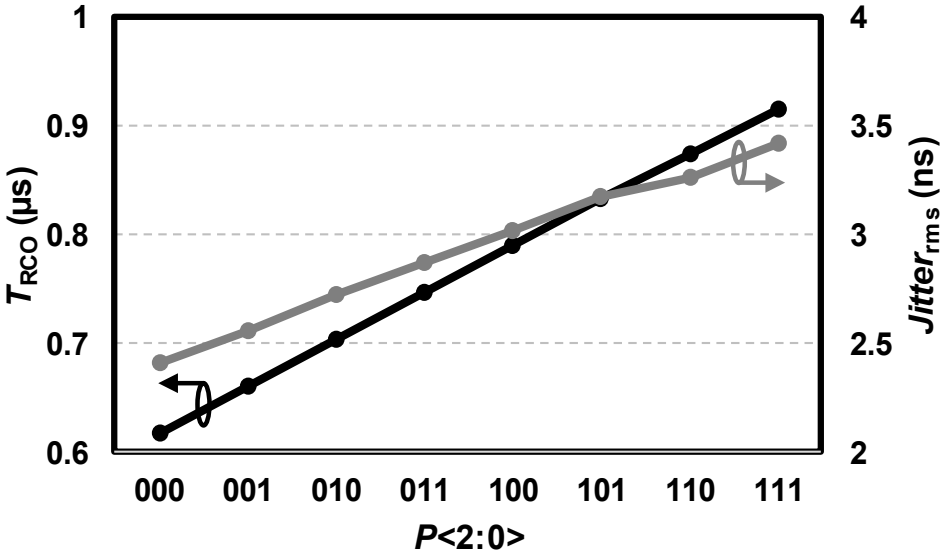

Fig. 4.20 The measured T_{RCO} and rms jitter of RCO versus different control bits of C_M.

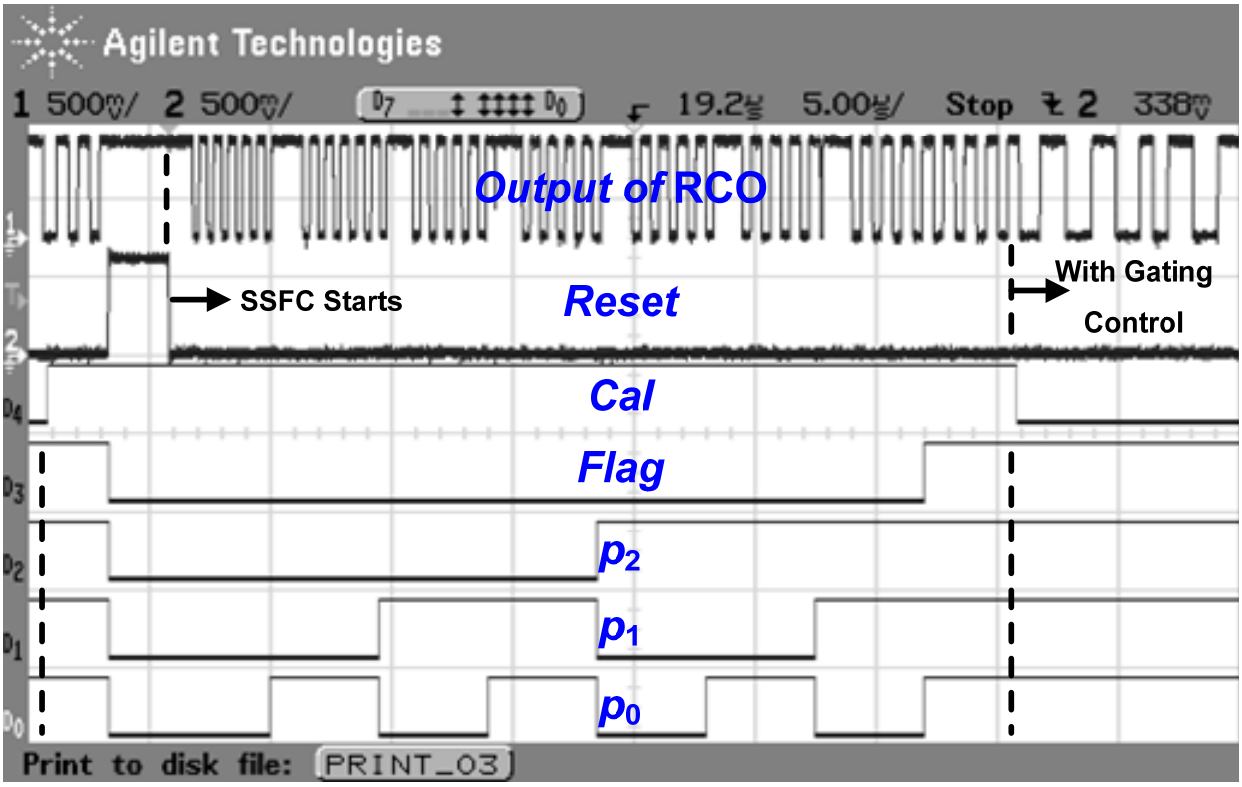

Fig. 4.21 The measured waveforms of RCO and SSFC with T_{CLK} of 300 ns.

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Table 4.2 Capacitors for Testing

C_{DUT}	C_{T1}	C_{T2}	C_{T3}	C_{T4}
pF	0.923488	2.02838	2.96895	3.94568
C_{DUT}	C_{T5}	C_{T6}	C_{T7}	C_{T8}
pF	4.91625	6.10603	7.00277	7.85888
C_{DUT}	C_{T9}	C_{T10}	C_{T11}	
pF	9.92961	12.0595	15.0409	

P<2:0> as the calibration procedure is in progress. In this measurement condition with T_{CLK} = 300 ns, SSFC is completed when P<2:0> = 111, corresponding to a T_{RCO} of 916 ns according to the experimental results in Fig. 4.20. Finally, *Cal* goes low and control bits P<2:0> are switched to M<2:0>. As a result, the frequency deviations of the RCO are properly calibrated to minimize the performance degradation of the CDC due to process variations.

Off-chip ceramic capacitors are adopted as the C_{DUT}, and their accurate capacitance values are characterized by an Agilent 4294A Precision Impedance Analyzer as tabulated in Table 4.2. The ceramic capacitors are then plugged into the socket mounded on the PCB. Via the PCB, one terminal of the capacitor is directly connected to the CDC and the other terminal is connected to the ground. Fig. 4.22 shows the measured period and rms jitter of T_{CCO} with various capacitances as the C_{DUT}. For C_{DUT} ranges from 0 to 15 pF, the period of the CCO (T_{CCO}) varies from 1.07 to 2.82 μs

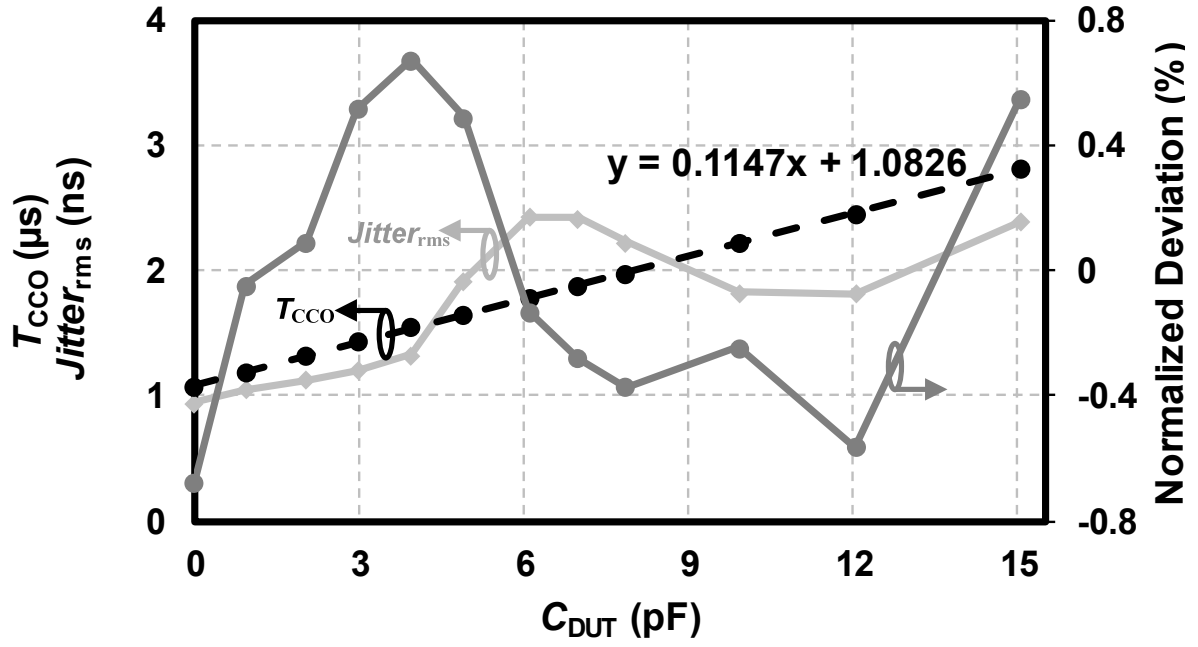

Fig. 4.22 The measured T_{CCO}, rms jitter of T_{CCO} and the deviation between T_{CCO} and its linear regression line.

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with an rms jitter around 2 ns. The linearity of the transfer function of C_{DUT} to T_{CCO} is also characterized by calculating the deviation between T_{CCO} and its linear regression line as shown in Fig. 4.22, indicating a maximum deviation of ±0.67%.

Finally, with values of C_{DUT} as listed in Table 4.2, the performance of the CDC is investigated. In order to obtain the conversion results, the output codes of CDC are recorded by a logic analyzer while a computer is utilized to perform the FFT. The FFT results are given by

$$D_{out}[n] = y_1[n] + 3 \cdot \left(y_2[n] - y_2[n+1] \right), \tag{4.19}$$

and the experimental results with C_{DUT} = 0 and 15 pF are demonstrated in Fig. 4.23, respectively. The estimation of non-ideal effects based on (4.11)−(4.15) is also provided in Fig. 4.23 to verify the circuit analysis with experimental results. The remaining 1st-order shaped quantization noise owing to period deviation is effectively suppressed by adopting SSFC. It is observed that the noise spectrum is dominated by the 2nd-order shaped quantization noise at high frequencies. On the other hand, the in-band noise floor is determined by the jitter of the CCO which can be estimated by the simulated rms jitter of the CCO and the simulated noise voltage at V_1.

Fig. 4.24 shows the output of CDC with various capacitors as C_{DUT} with R^2 = 0.9996. From [40] and [60], the SNR at the CDC output can be expressed as

$$\text{SNR} = 20\log\left(\frac{\text{Capacitance Range}/2/\sqrt{2}}{\text{RMS Capacitance Resolution}} \right), \tag{4.20}$$

Fig. 4.25 shows the measured SNR degradation of the CDC versus the control bits of C_M. Due to the in-band noise floor, the degradation is smaller when compared to Fig. 4.4. In order to evaluate the overall performance of the CDC, a figure-of-merit (FoM) [61]−[62] is given by

$$\text{FoM} = \frac{\text{Power}}{2^{\text{Resolution}} \cdot 2 \cdot f_{BW}}, \tag{4.21}$$

where resolution is defined as (SNR-1.76)/6.02, while f_{BW} is 8 kHz in this particular case.

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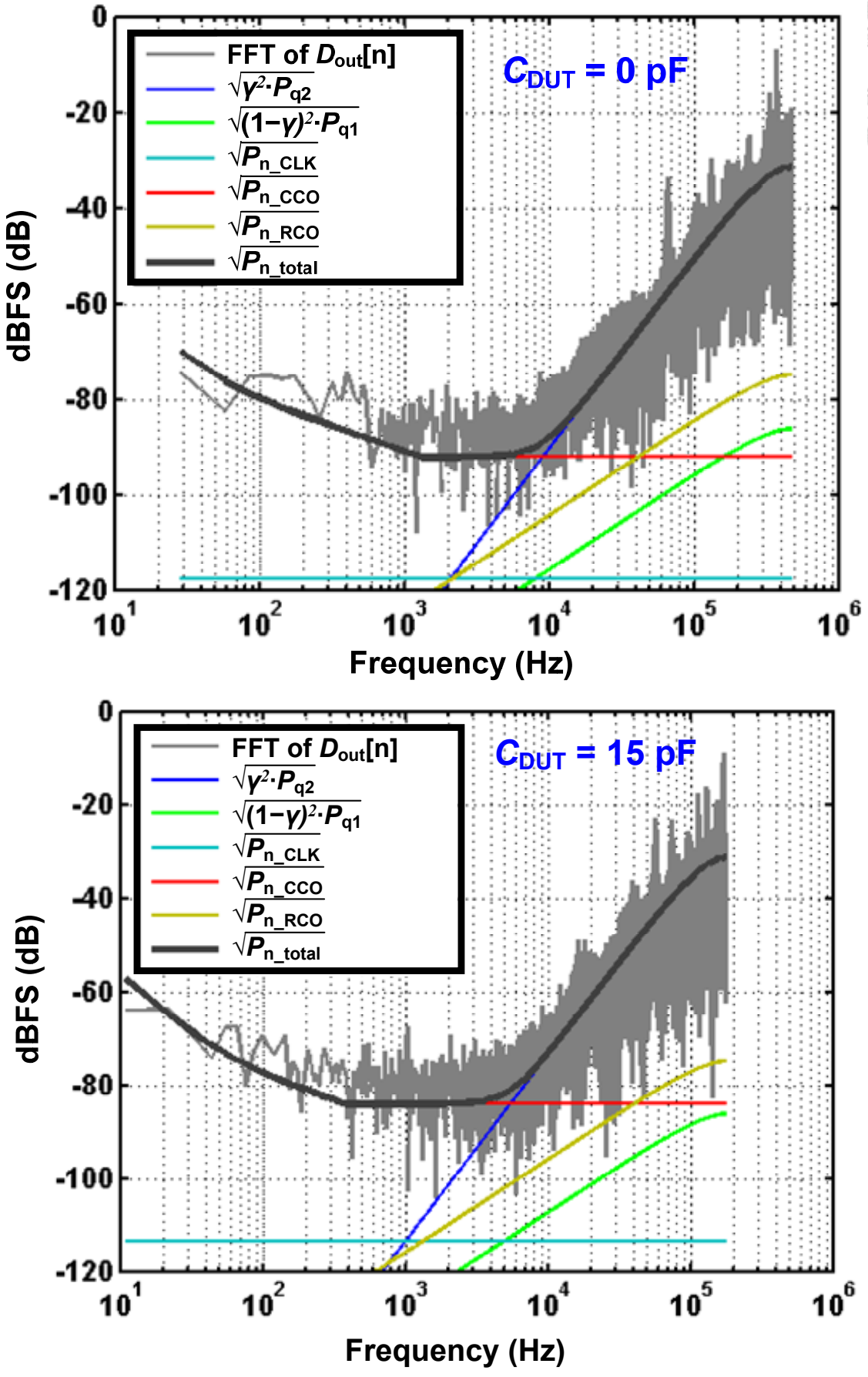

Fig. 4.23 The FFT results of D_{out} when C_{DUT} equals 0 pF and 15 pF, respectively.

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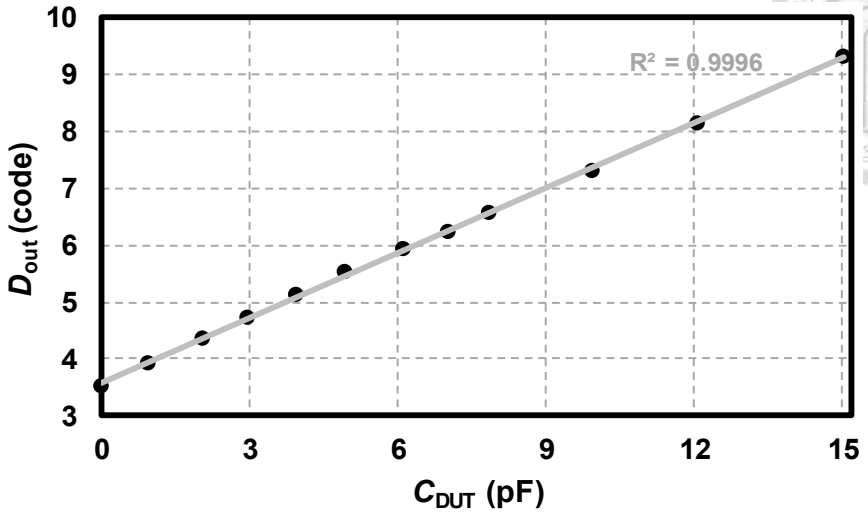

Fig. 4.24 The output of CDC with various C_{DUT} values.

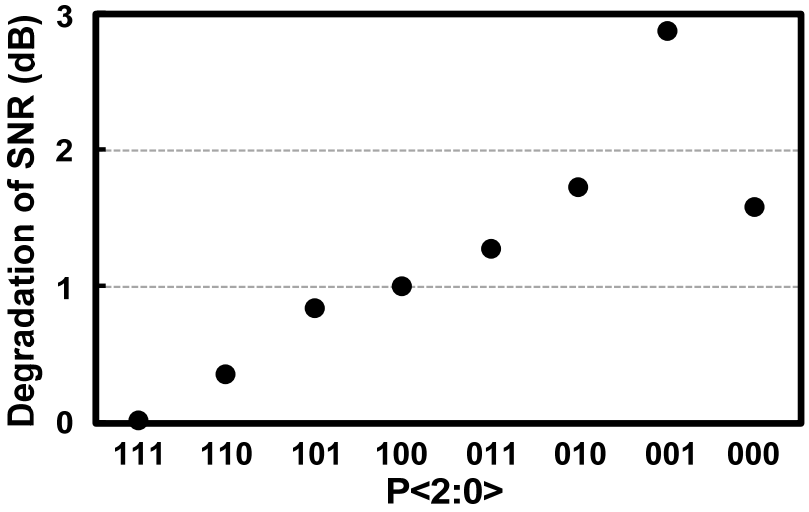

Fig. 4.25 The measured degradation of SNR versus different control bits of C_M.

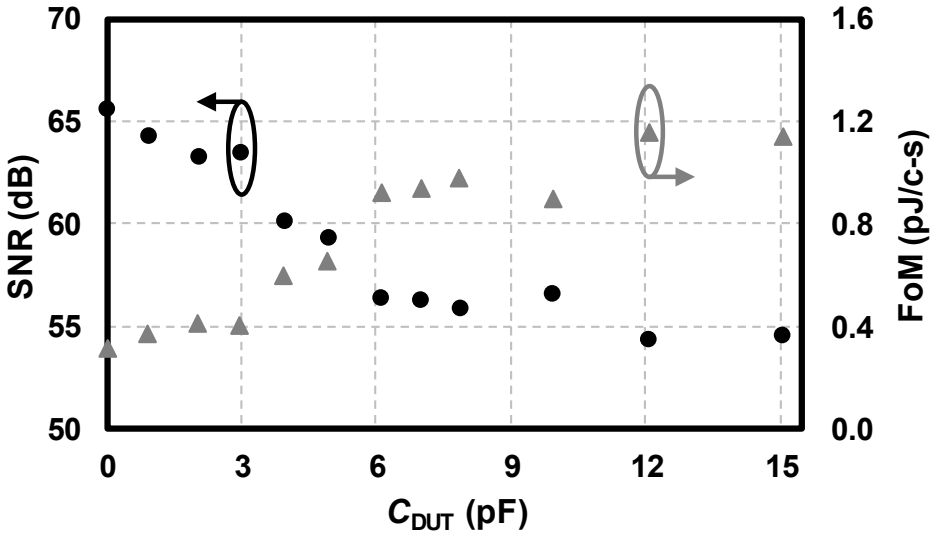

Fig. 4.26 The SNR and FoM of the proposed CDC with various C_{DUT} values.

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At various C_{DUT} values, the SNR and FoM are shown in Fig. 4.26. As the value of C_{DUT} increases, the charging slope of the voltage of C_{DUT} decreased. Therefore, the rms jitter of CCO due to noise of CMC becomes larger and degrades the SNR. In addition, the power consumption of the CDC is dominated by the charging current of CCO, which is independent of the value of C_{DUT}. As a result, the FoM is dominated by the SNR and degraded when C_{DUT} is large. The performance summary and comparison are provided in Table 4.3.

4.5 Summary

This chapter presents a period-mode oscillator-based time-mode delta-sigma CDC. In order to alleviate the performance degradation due to period deviations, a SSFC technique is adopted in the circuit implementation. In addition to derivations and analysis of the design constraints, the proposed circuit is successfully fabricated in a 90-nm CMOS technology for verification. The fabricated chip is tested with off-chip capacitance ranging from 0 to 15 pF, demonstrating an equivalent bits of resolution of 8.8 bit with an FoM of 1.16 pJ/c.-s. with a bandwidth of 8 kHz.

Table 4.3 Performance Summary and Comparison

Parameter	Unit	[40] TCAS-I'17	[39] ISSCC'14	[42] VLSI'14	[23] JSSC'13
Architecture	-	SAR	SAR	SAR +ΔΣ	ΔΣ
Technology	nm	180	180	180	160
Area	mm^2	0.055	0.49	0.46	0.28
V_{DD}	V	0.8 & 1.2	0.9 & 1.2	1.4	1.2
Power	μW	6.44	0.16	33.7	10.3
Conv. Time or $1/(2f_{BW})$	μsec	16	4000	230	800
Cap. Range	pF	12.66	10	24	0.52
Resolution	bit	11.6	8.9	15.4	11.1
FoM	pJ/c.-s.	0.033	1.33	0.179	3.76

Parameter	Unit	[41] TCAS-I'14	[43] JSSC'15	[44] ISSCC'15	[45] ESSCIRC'11	**This Work**
Architecture	-	ΔΣ	Dual-slope	IDCD[a]	OSC-based	**OSC-based**
Technology	nm	180	180	40	130	**90**
Area	mm^2	0.2	0.1	0.0017	0.0725	**0.051**
V_{DD}	V	1.6	0.6 & 1.2	0.45 & 1	0.3	**0.6**
Power	μW	80	0.11	1.84	0.27	**8.04**
Conv. Time or $1/(2f_{BW})$	μsec	1000	6400	19	1000	**62.5**
Cap. Range	pF	3	4	0.7−11.3	0.3	**15**
Resolution	bit	14.2	7	8	6.1	**8.8**
FoM	pJ/c.-s.	4.25	5.3	0.141	2.1	**1.16**

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Chapter 5
A Frequency-Mode Oscillator-Based Capacitor-to-Digital Converter

5.1 Overview of Operation

Fig. 5.1 demonstrates the schematic of the proposed frequency-mode oscillator-based CDC, which consists of a capacitance-to-voltage converter (C2V), a voltage-controlled oscillator (VCO), a gated VCO, a residue generator with two counters. The C2V generates the threshold voltage (V_{th}) for the VCOs according to the capacitance of the device under test (C_{DUT}). The VCOs continuously generate timing signals with frequencies inversely proportional to $V_{th,}$ while the counters are utilized to quantize the frequencies with an external clock. As the same as in Chapter 4, a residue generator and gated switches are added to create the second-ordered noise shaping effect. The timing diagram of the frequency-mode CDC is shown in Fig. 5.2. The output of *Counter*1 represents the number of rising edges of the VCO_1 in each period of the external clock (*CLK*) and is given by

$$y_1[\mathrm{n}] = \frac{1}{T_{\mathrm{VCO1}}}\left(T_{\mathrm{CLK}} + T_{\mathrm{q1}}[\mathrm{n}] - T_{\mathrm{q1}}[\mathrm{n}+1]\right) = \frac{T_{\mathrm{CLK}}}{T_{\mathrm{VCO1}}} + \frac{\phi_{\mathrm{q1}}[\mathrm{n}] - \phi_{\mathrm{q1}}[\mathrm{n}+1]}{2\pi}, \tag{5.1}$$

where T_{CLK} is the period of the external clock, T_{VCO1} is the period of VCO_1, T_{q1} is the associated

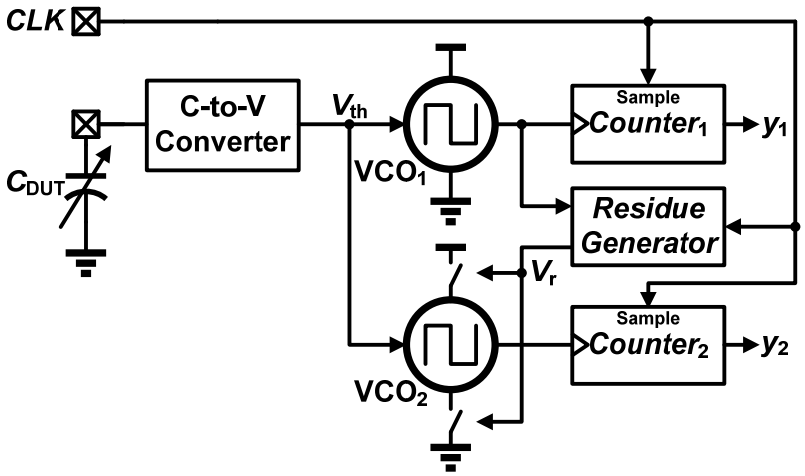

Fig. 5.1 The schematic of the proposed frequency-mode oscillator-based CDC.

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quantization error in the time domain, and ϕ_{q1} is the associated quantization error in the phase domain. By taking the advantage of oversampling ratio between the sampling frequency and the varying rate of C_{DUT}, T_{VCO1} is regarded as constant in each sample. Applying Z-transform to (5.1), the simplified result is given by

$$Y_1[z] = \frac{T_{CLK}}{T_{VCO1}} - z \cdot (1 - z^{-1}) \cdot \frac{Y_{\phi_{q1}}[z]}{2\pi}, \tag{5.2}$$

impling that y_1 can represent the ratio of f_{VCO1} to f_{CLK} if the first-order shaped ϕ_{q1} is filtered out by the decimation filter. After applying the inverse transfer function of the C2V with the gain (K_V) of VCO_1 to the filtered result, the capacitance of the C_{DUT} can be retrieved.

In addition, to further reduce the quantization error, a residue generator is utilized to generate a residue timing signal (V_r) with a pulse-width of

$$T_r[n] = 2 \cdot T_{VCO1} - T_{q1}[n] = T_{VCO1} \cdot \left(2 - \frac{\phi_{q1}[n]}{2\pi}\right), \tag{5.3}$$

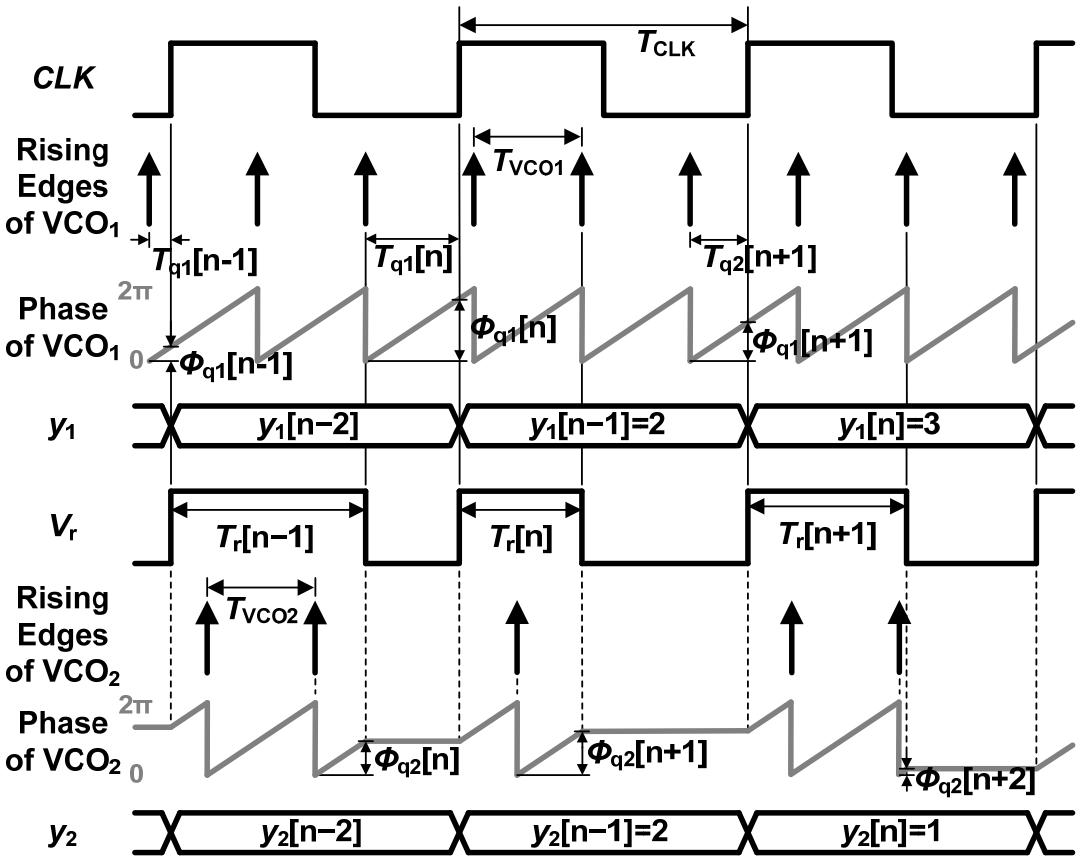

Fig. 5.2 The timing diagram of the proposed frequency-mode CDC

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gating the charging current of VCO_2. When V_r goes low, the charging path of the capacitor in VCO_2 is cut off. The voltage of the capacitor is held, while the phase of VCO_2 remains until V_r goes high. More details of the VCO_2 operation will be presented in 5.2.2. It is noted that a constraint on the maximum T_{VCO1} is added to the residue generator in order to avoid the generation of a nearly zero pulse width. As a result, the period of VCO_1 is defined to be no more than one third of T_{CLK}.

Counter$_2$ is utilized to count the number of rising edges of VCO_2 during the period of V_r and the output can be expressed as

$$y_2[\mathrm{n}] = \frac{1}{T_{VCO2}}\left(T_r[\mathrm{n}] + T_{q2}[\mathrm{n}] - T_{q2}[\mathrm{n}+1]\right) = \frac{T_r[\mathrm{n}]}{T_{VCO2}} + \frac{\phi_{q2}[\mathrm{n}] - \phi_{q2}[\mathrm{n}+1]}{2\pi}, \tag{5.4}$$

where T_{VCO2} is the period of the VCO_2 output waveform, T_{q2} is defined as the quantization error of T_r, and ϕ_{q2} is the associated quantization error in the phase domain. By assuming $T_{VCO1} = T_{VCO2}$ and applying (5.3) to (5.4), the Z-transform of the result is given by

$$Y_2[\mathrm{z}] = \left(2 - \frac{Y_{\phi q1}[\mathrm{z}]}{2\pi}\right) - \mathrm{z}\cdot\left(1-\mathrm{z}^{-1}\right)\cdot\frac{Y_{\phi q2}[\mathrm{z}]}{2\pi}, \tag{5.5}$$

By combining $y_1[\mathrm{n}]$ and $y_2[\mathrm{n}]$ in the form of

$$D_{out}[\mathrm{n}] = y_1[\mathrm{n}] + y_2[\mathrm{n}] - y_2[\mathrm{n}+1], \tag{5.6}$$

the Z-transform of $D_{out}[\mathrm{n}]$ from (5.1)–(5.5) is given by

$$Y_1[\mathrm{z}] + (1-\mathrm{z})\cdot Y_2[\mathrm{z}] = \frac{T_{CLK}}{T_{VCO1}} - \mathrm{z}^2\cdot\left(1-\mathrm{z}^{-1}\right)^2\cdot\frac{Y_{\phi q2}[\mathrm{z}]}{2\pi}, \tag{5.7}$$

which implies that the ratio of T_{VCO1} to T_{CLK} can be retrieved from y_1 and y_2 with a second-order shaped ϕ_{q2}, which can be filtered by the decimation filter. As the result, the capacitance of C_{DUT} can be obtained with improved precision.

The theoretical signal-to-noise ratio (SNR) can be obtained by the same steps as in Section 4.1. The quantization noise power of the second-order shaped ϕ_{q2} is given by

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$$P_{q2} \cong \frac{(2\pi)^2 \cdot \pi^4}{60} OSR^{-5}, \tag{5.8}$$

where OSR is the oversampling ratio given by

$$\mathrm{OSR} = \frac{f_{\mathrm{CLK}}}{2 \cdot f_{\mathrm{BW}}}, \tag{5.9}$$

where f_{BW} is the bandwidth of an ideal sinc filter for decimation and f_{CLK} is the frequency of the external clock. The signal power is defined as

$$P_{\mathrm{s}} = \frac{1}{2}\left(\frac{\Delta f_{\mathrm{VCO1}} / f_{\mathrm{CLK}}}{2}\right)^2, \tag{5.10}$$

where Δf_{VCO1} is the difference between the frequencies of $\mathrm{VCO_1}$ for maximal and minimal C_{DUT}. Consequently, the SNR can be estimated as

$$\mathrm{SNR} = 10 \cdot \log_{10}\left\{P_{\mathrm{s}} \Big/ \left[P_{\mathrm{q2}} / (2\pi)^2\right]\right\} = 20 \cdot \log_{10}\left(\Delta f_{\mathrm{VCO1}} / f_{\mathrm{CLK}}\right) - 11.14 + 50 \cdot \log_{10}(\mathrm{OSR}). \tag{5.11}$$

The last term in (5.11) indicates that doubling OSR improves the SNR by 15 dB, which is the same as a second-order delta-sigma ADC.

Fig. 5.3 shows the estimated SNR from (5.11) with different maximum f_{VCO} which is normalized to f_{CLK} under the conditions that OSR = 64. The estimated SNR increases with the f_{VCO1}, however,

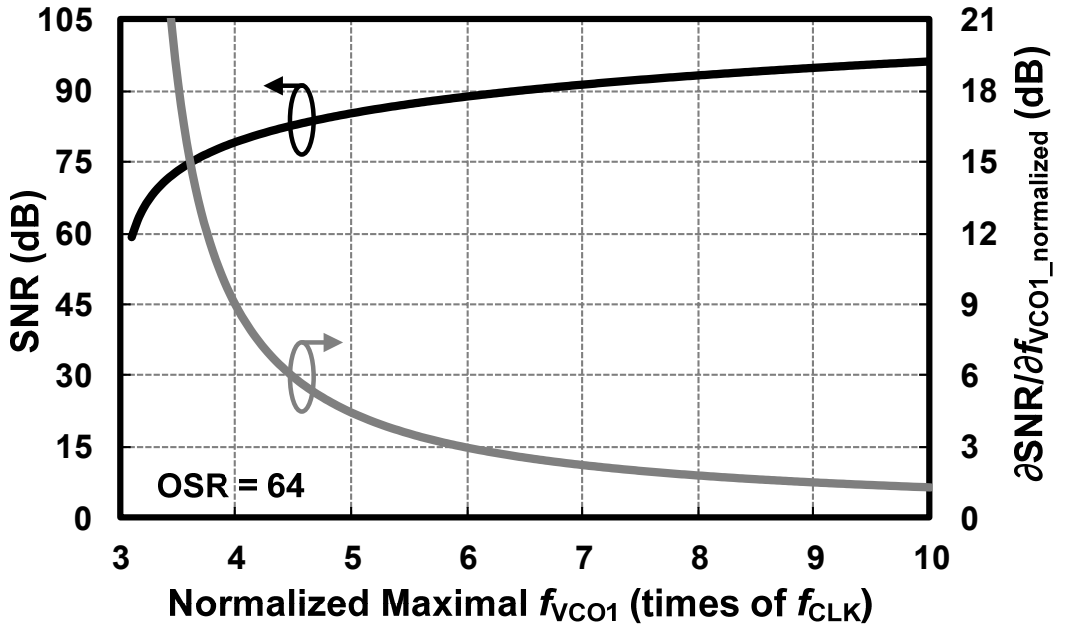

Fig. 5.3 The estimated SNR with different maximal f_{VCO1} with an OSR of 64.

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the increases become insignificant when f_{VCO1} is larger than 6 times of f_{CLK}.

5.2 Circuit Implementation of the Proposed CDC

5.2.1 C-to-V Converter and VCO_1

Before introducing the C-to-V converter adopted in the proposed CDC, a quick review of prior arts of C2V is given. Fig. 5.4 (a) shows a C2V consists of a sinusoidal excitation and an envelope detector with an amplifying stage [19], [63]−[64]. The gain of amplifying stage is given by

$$A_v = \frac{V_A}{V_E} = -\frac{sR_F C_{DUT}}{1+sR_F C_F}, \tag{5.12}$$

which is proportion to C_{DUT}. The following envelope detector extracts the envelope of the amplified signal, resulting an output voltage V_O, which is proportional to C_{DUT}. Other C2Vs based on charge-transfer method [34] and current-mode excitation [35] have also been proposed. In addition, a popular method in recent years is the switched-capacitor charge amplifier as shown in Fig. 5.4 (b). The switched-capacitor structure [65]−[67] can be easily extended into differential operation [66] and combined with well developed noise cancelling techniques [67] to get a finer resolution of C_{DUT}.

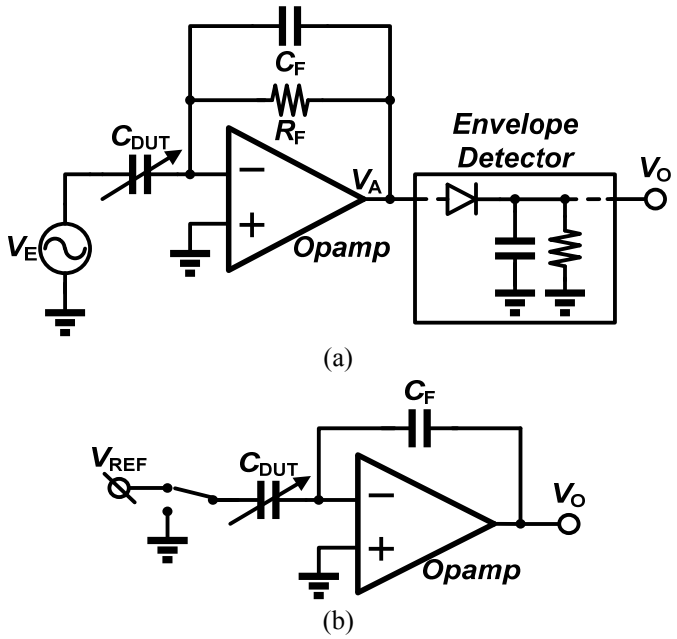

Fig. 5.4 (a) a capacitance-to-voltage converters based on a sinusoidal excitation with an envelope detector and (b) the switched-capacitor charge amplifier.

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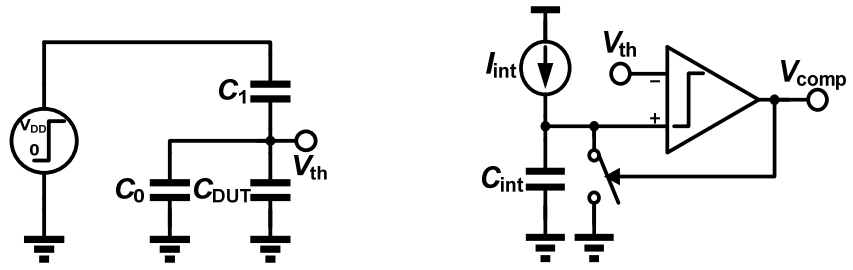
However most of above mentioned methods require high open-loop gain opamps, which are difficult to be realized under a limited supply voltage such as 0.6 V.

Fig. 5.5 (a) shows the proposed C2V without high-gain OTAs. By exciting the series-connected capacitors with a voltage step function. The voltage at the output of the C2V is given by

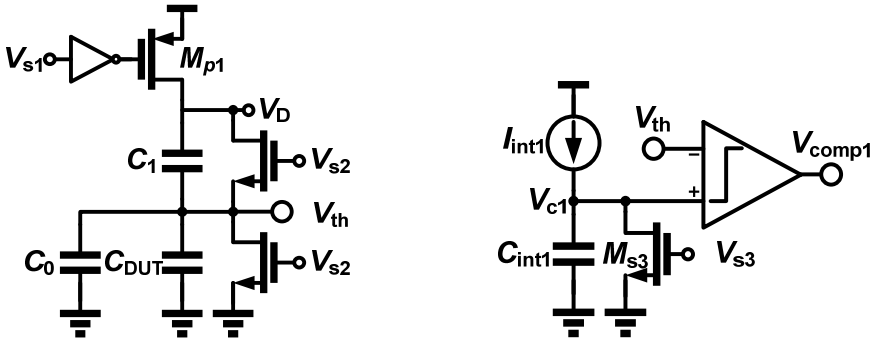
$$V_{\text{th}} = V_{\text{DD}} \cdot \frac{C_1}{C_0 + C_1 + C_{\text{DUT}}}. \tag{5.13}$$

In order to generate the V_{th} in the suitable input range of the comparator, which is about $0.4 \cdot V_{\text{DD}}$ to $0.75 \cdot V_{\text{DD}}$. The values of C_0 and C_1 are selected according to the range of C_{DUT}. The targeting range of C_{DUT} is 0 to 12 pF, as a result, the values of C_0 and C_1 are 3.75 pF and 11.75 pF, respectively. By



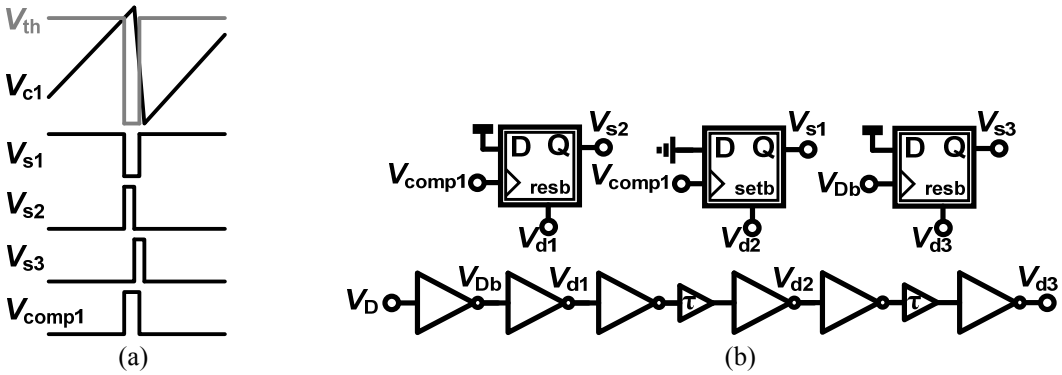
(a) (b)

Fig. 5.5 The proposed (a) capacitance-to voltage converter and (b) the following relaxation oscillator.



(a) (b)

Fig. 5.6 The schematics of the proposed (a) C2V and (b) VCO_1



(a) (b)

Fig. 5.7 (a) The timing diagram of the control signals and (b) peripheral circuit blocks.

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adopting this voltage as the threshold voltage for VCO_1 depicted in Fig. 5.5 (b), the frequency of VCO_1 is given by

$$f_{VCO1} = \frac{I_{int}}{C_{int}} \cdot \frac{C_0 + C_1 + C_{DUT}}{V_{DD} \cdot C_1}, \quad (5.14)$$

which is linearly increased with C_{DUT}. Fig. 5.6 shows the schematics of the C2V and VCO_1 with re-setting switches, and Fig. 5.7 shows the timing diagram of control signals and associated control circuits. Once the cross voltage of C_{int1} (V_{c1}) reaches V_{th}, the output of the comparator (V_{comp1}) rises to V_{DD} and triggers the D flip-flop (DFF) to pull V_{s1} to the ground voltage and push V_{s2} to V_{DD}. As the rising of V_{s2}, the the C2V is reset by connecting the top plate and bottom plate of the capacitors together, while M_{p1} is cut-off to prevent from drawing large current from V_{DD} during resetting. A inverter-based delay chain is adopted to generate delayed signals of V_D and applied to the DFFs. While V_D is pulled to ground, C_{int1} starts discharging after a small delay. Then, the resetting switches of C2V are turned off, and the capacitors are excited with a voltage step controlled by V_{s1}. Finally, the resetting switch of VCO_1 is turned off, and VCO_1 enters next oscillating cycle. It is noted that M_{p1} must be turned on after the falling of V_{s2} to generate correct V_{th}, and VCO_1 cannot be reset too early to provide a wide enough pulse width of V_{comp1} for subsequent operation.

5.2.2 Gated VCO_2

Fig. 5.8 (a) shows the schematic of VCO_2. To make the frequencies of VCO_1 and VCO_2 as close as possible, VCO_2 uses the same structure as the VCO_1, the charging current I_{int2} equals I_{int1}, and C_{int2} equals C_{int1}. An additional switch M_G is added in VCO_2 to gate the oscillation, and a buffer is

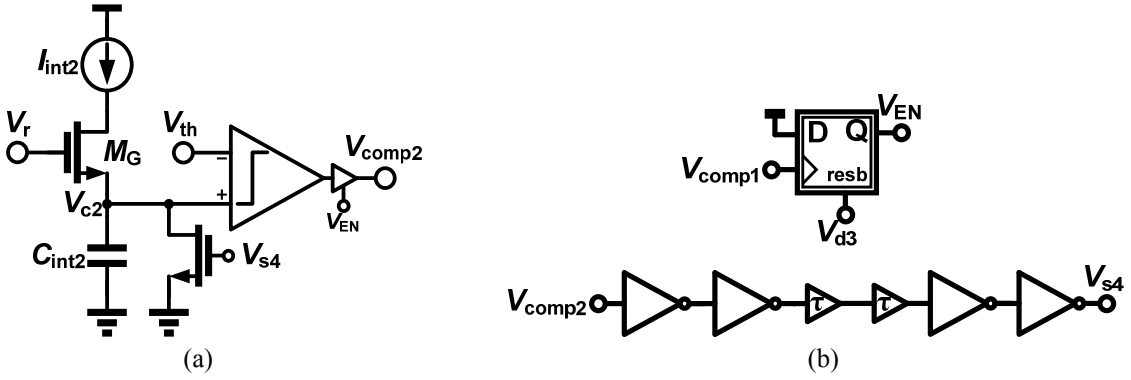

Fig. 5.8 The schematic of (a) gated VCO_2 and (b) peripheral circuit blocks.

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added after the comparator to prevent false trigger of following circuit during the resetting phase of the C2V. Fig. 5.8 (b) shows the circuit blocks for generating resetting signal and enabling signal for VCO_2.

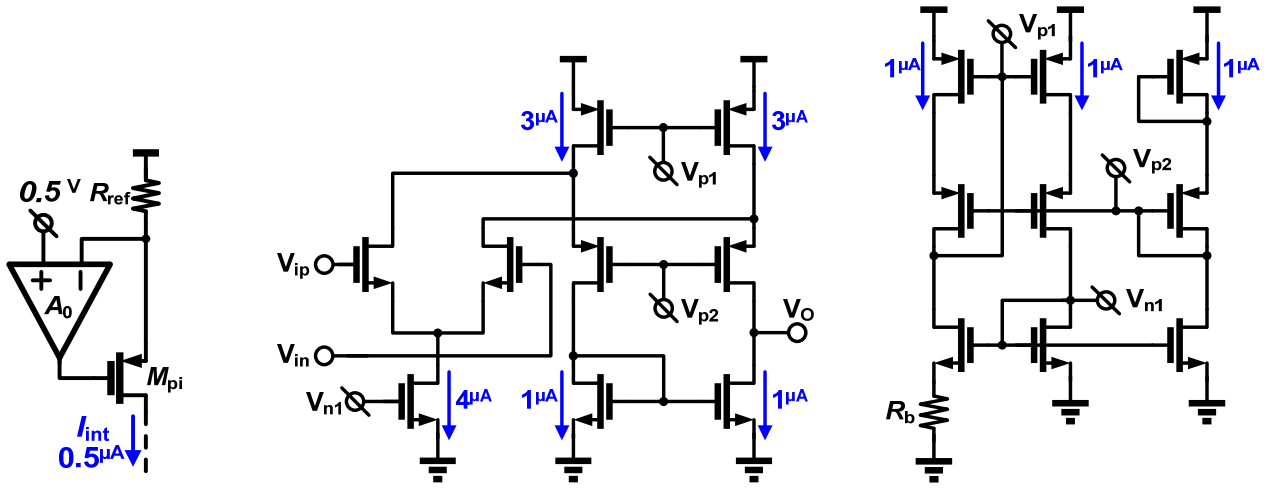
5.2.3 Implementation of I_{int} and opamps

In order to provide a constant current during the charging phase of the VCOs, an output-impedance boosting current source is adopted as shown in Fig. 5.9 (a). The output impedance is given by

$$R_{out} = (1 + A_0) g_m r_o R_{ref} + r_o + R_{ref} . \tag{5.15}$$

where A_0 is the gain of the opamp, g_m is the transconductance of M_{pi}, and r_o is the equivalent resistor due to the early effect of M_{pi}. The resulting value of I_{int} is given by

$$I_{int} = (V_{DD} - 0.5^{V}) / R_{ref} . \tag{5.16}$$



(a) (b) (c)

Fig. 5.9 The circuit schematics of (a) the I_{int} generator, (b) the adopted opamp with (c) the biasing circuit.

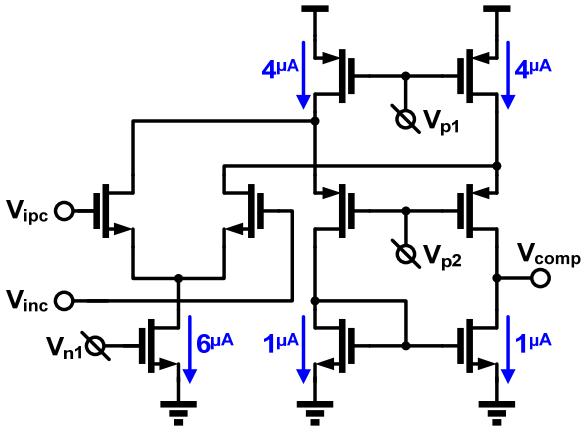


Fig. 5.10 The circuit schematic of comparators.

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where V_{DD} equals 0.6 V, and R_{ref} equals 200 kohm in this particular design.

Fig. 5.9 (b) and (c) shows the schematic of the opamp and the biasing circuit, respectively. The start-up circuit for the biasing circuit is omitted for simplicity. Due to the limited supply voltage in this work, low-threshold-voltage (lvt) NMOS is adopted in the opamp and the biasing circuit. The current consumption of each branches is also depicted in Fig. 5.9. The comparators adopted in the work use the same architecture of opamp with different ratios of current mirror due to consideration of delay time as shown in Fig. 5.10. The comparators share the bias circuit with opamps for energy efficiency.

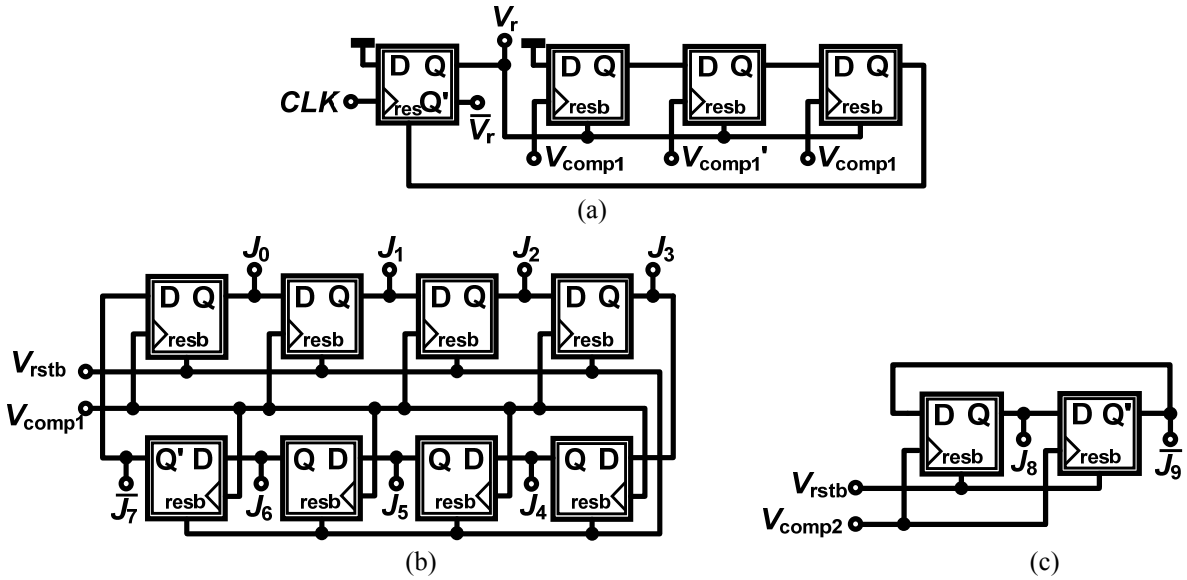

Fig. 5.11 The circuit schematics of (a) residue generator, (b) *Counter*$_1$ and (c) *Counter*$_2$.

5.2.4 Residue Generator and Counters

The residue generator and counters adopted in this work is the same as in 4.3.4 with different input configurations as shown in Fig. 5.11.

5.3 Non-Ideal Effects for Noise Consideration

According to the circuit schematics adopted in this work, several non-ideal effects degrades the performance of proposed CDC, such as jitter due to circuit noise and process variations and leakage current of switches. This section discusses the non-ideal effects in each building blocks, which degrade the noise rejection of the CDC.

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5.3.1 Jitter of *CLK*

The jitter of *CLK* has the same effect as the jitter of sampling clock in analog-to-digital converter in voltage domain as mentioned in 2.1.2. However, the equivalent time width of one least significant bit (LSB) varies with T_{VCO1}. The jitter of *CLK* should be normalized to T_{VCO1} to be compared with the signal power of measured digital codes. The noise contribution of clock jitter is given as

$$P_{n\_CLK} = \left(\frac{\tau_{CLK}}{T_{VCO1}} \right)^2 \cdot \mathrm{OSR}^{-1}, \tag{5.17}$$

where τ_{CLK} is the rms jitter of *CLK*. It is noted that only the noise power within the f_{BW} affects the output accuracy since a decimation filter is applied to y_1.

5.3.2 Jitter of VCO_1

The jitter of VCO_1 directly affect the equivalent time width of unit LSB as the *CLK* in 4.2.2. However, the digital code is proportional to the frequency of the VCO_1 not the period in a frequency-mode CDC. By using the relation of $(1+x)^{-1} \approx 1-x$, the noise contribution by the jitter of the VCO_1 can be approximated by

$$P_{n\_VCO1} \approx \left(\frac{\tau_{VCO1}}{T_{VCO1}} \right)^2 \cdot \frac{f_{VCO1}}{f_{CLK}} \cdot \mathrm{OSR}^{-1}, \tag{5.18}$$

where τ_{VCO1} is the rms jitter of VCO_1. P_{n_VCO1} increases with the ratio of f_{VCO1} to f_{CLK}. As the ratio becomes larger, more transition edges of VCO_1 are accountable for the noise contribution at the CDC output.

5.3.3 Jitter of VCO_2

Observed from Fig. 5.2 and (5.7), y_1 is influenced by the jitter of VCO_1 while y_2 is vulnerable to the jitter of VCO_2. As y_2 multiplied by (1-z) is presented at the output of the CDC, the noise contributed by the jitter of the VCO_2 is also first-order shaped. By adopting the same approximation in 5.3.2, the noise power is given by

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$$P_{\text{n\_VCO2}} \approx \left(\frac{\tau_{\text{VCO2}}}{T_{\text{VCO2}}}\right)^2 \cdot \frac{\alpha \cdot T_{\text{VCO1}}}{T_{\text{VCO2}}} \cdot \frac{\pi^2}{3} \cdot \text{OSR}^{-3}, \tag{5.19}$$

where τ_{VCO2} is the rms jitter of the VCO_2 and α is the ratio of average T_r to T_{VCO1}, which is 1.5 in this particular CDC design as the average Φ_{q1} equals π.

5.3.4 Frequency mismatch between VCO_1 and VCO_2

The Z-transform in (5.7) is obtained based on the assumption $f_{\text{VCO2}} = f_{\text{VCO1}}$. However, due to process variations and device parasitics, it is inevitable that f_{VCO2} may deviate from the design value as the circuits are fabricated. With γ denoting the actual ratio of f_{VCO2} to f_{VCO1} for the fabricated circuit, (5.7) can be rewritten as

$$Y_{\text{out}}[z] = \frac{f_{\text{VCO1}}}{f_{\text{CLK}}} - z \cdot (1 - z^{-1}) \cdot \frac{Y_{\phi q1}[z]}{2\pi} \cdot (1 - \gamma) + z^2 \cdot (1 - z^{-1})^2 \cdot \frac{Y_{\phi q2}[z]}{2\pi}, \tag{5.20}$$

indicating that the frequency deviation of the VCO_2 results in the remaining first-order shaped quantization noise power. The associated noise power can be calculated in the same way as in (5.8), leading to the expression as

$$P_{q1} \cong \frac{(2\pi)^2 \cdot \pi^2}{36} \cdot \text{OSR}^{-3}. \tag{5.21}$$

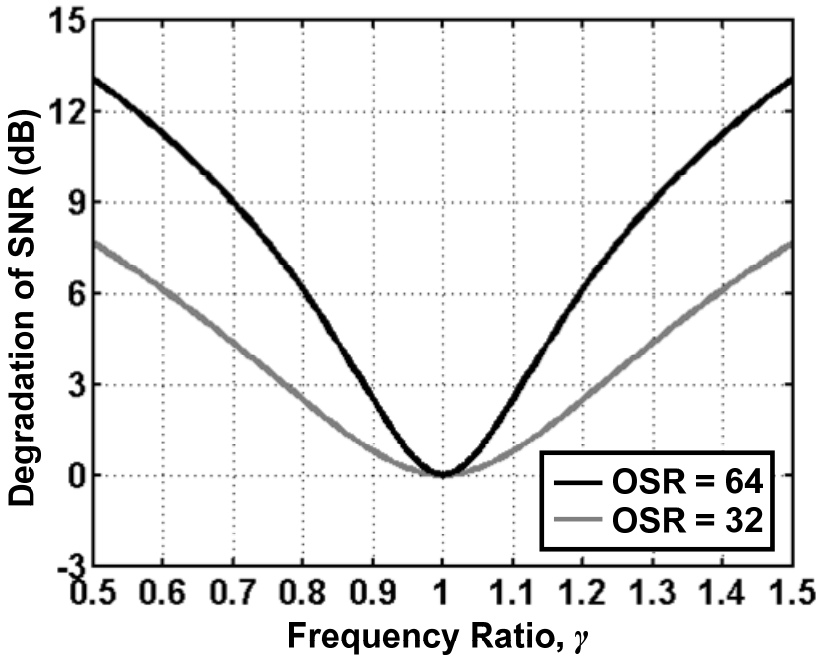

Fig. 5.12 The degradation of SNR with different γ.

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Fig. 5.12 shows the degradation of SNR due to frequency deviation from (5.8)–(5.9) and (5.20)–(5.21), and indicates that the resulting degradation of resolution is confined to 1 bit with a ±20% frequency variation.

5.3.5 Estimated SNR with Jitter and Frequency Deviation

Now the estimated SNR can be reexamined versus the maxial f_{VCO1} after elaborating several important non-ideal effects. The total noise power by taking the jitter and frequency deviation into account is given by

$$P_{n\_total} = P_{n\_CLK} + P_{n\_VCO1} + P_{n\_VCO2} + (1-\gamma)^2 \cdot \frac{P_{q1}}{(2\pi)^2} + \frac{P_{q2}}{(2\pi)^2}. \tag{5.22}$$

With the typical parameters listed in Table 5.1 as an example, the estimated SNR with different

Table 5.1 Parameters for a Typical Case

Parameter	Value
T_{CLK}	900 nsec
OSR	64
γ	0.9
τ_{CLK}	0.1‰·T_{CLK}
τ_{VCO1}	4‰·T_{VCO1}
τ_{VCO2}	4‰·T_{VCO2}

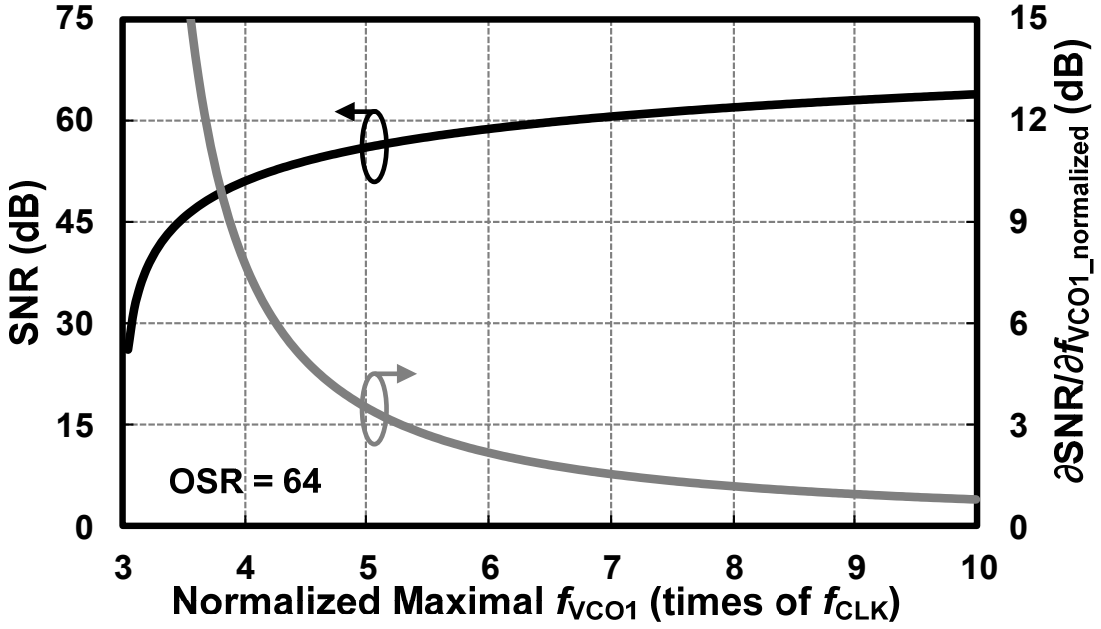

Fig. 5.13 The estimated SNR versus different maximal f_{VCO1} with jitter and frequency deviation.

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maximal f_{VCO1} is shown in Fig. 5.13. Based on the above assumptions and derivations of the effects of jitter and frequency deviation, the maximal f_{VCO1} is chosen to be around 5.5 times of f_{CLK}.

5.4 Non-Ideal Effects for Linearity Consideration

The linearity of the CDC is dominated by the C2V and VCO_1. This section focuses on the non-ideal effects in C2V and VCO_1, and a compensating method for improving the linearity.

5.4.1 Delay Time of the Comparator and Digital Blocks

By taking the delay time of the comparator and digital blocks into consideration, (5.14) is rewritten as

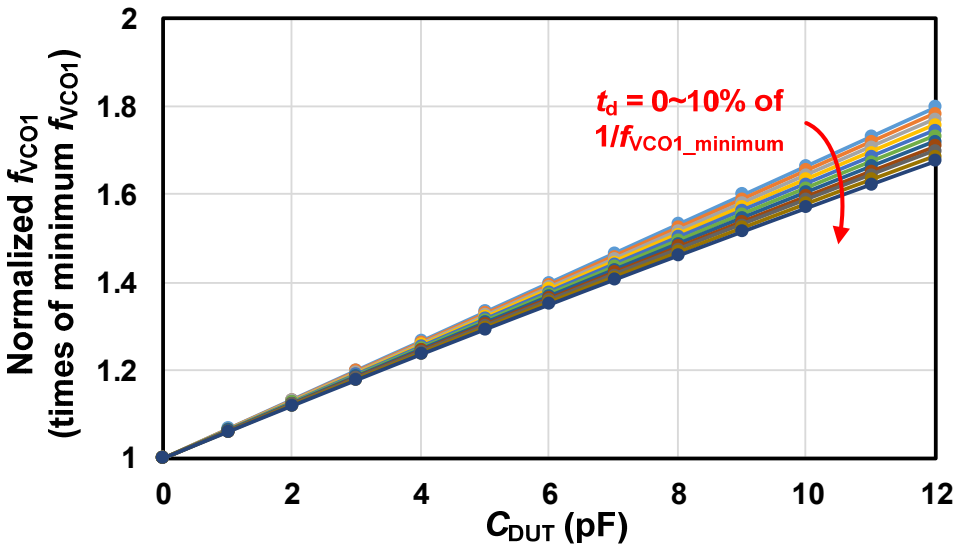

Fig. 5.14 Simulated f_{VCO1} versus C_{DUT} with different t_d.

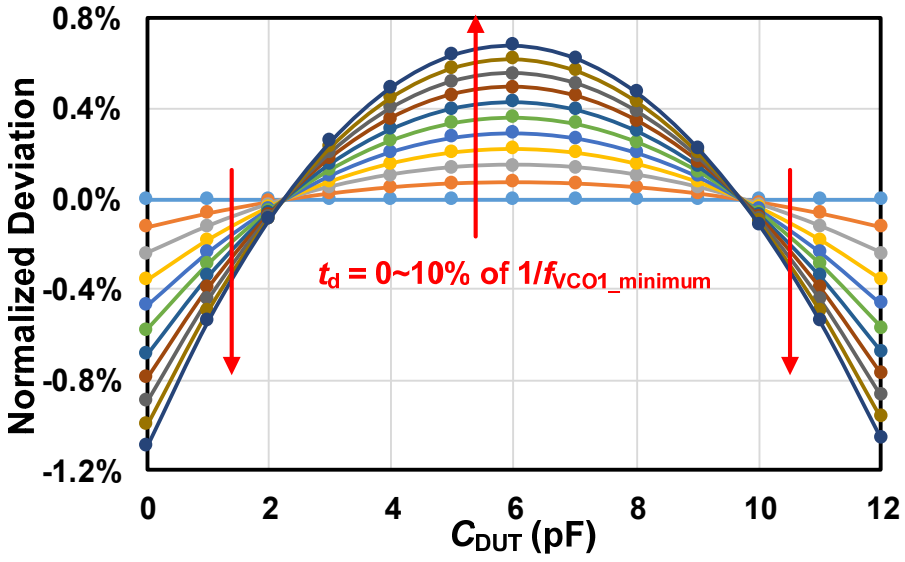

Fig. 5.15 The deviation between f_{VCO1} and its linear regression line versus C_{DUT} with different t_d.

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$$f_{\mathrm{VCO1}} = \left(\frac{C_{\mathrm{int}}}{I_{\mathrm{int}}} \cdot \frac{V_{\mathrm{DD}} \cdot C_1}{C_0 + C_1 + C_{\mathrm{DUT}}} + t_{\mathrm{d}} \right)^{-1}, \tag{5.23}$$

where t_{d} is the total delay time of the comparator and digital blocks. The f_{VCO1} is no longer proportional to C_{DUT} because t_{d} is added to the denominator. Fig. 5.14 shows the f_{VCO1} versus C_{DUT} with different t_{d}. To acquire the effect of t_{d} for general cases, f_{VCO1} is normalized to its minimum value, and t_{d} is normalized to the minimum T_{VCO1} in Fig. 5.14. The increment of f_{VCO1} according to per picofarad increase of C_{DUT} is descending with the value of C_{DUT} due to t_{d}, and results the down bending curves in Fig. 5.14. Fig. 5.15 shows the deviation between f_{VCO1} and its linear regression line versus C_{DUT} with different t_{d}, which is normalized to the total range of f_{VCO1}. The resulting square of

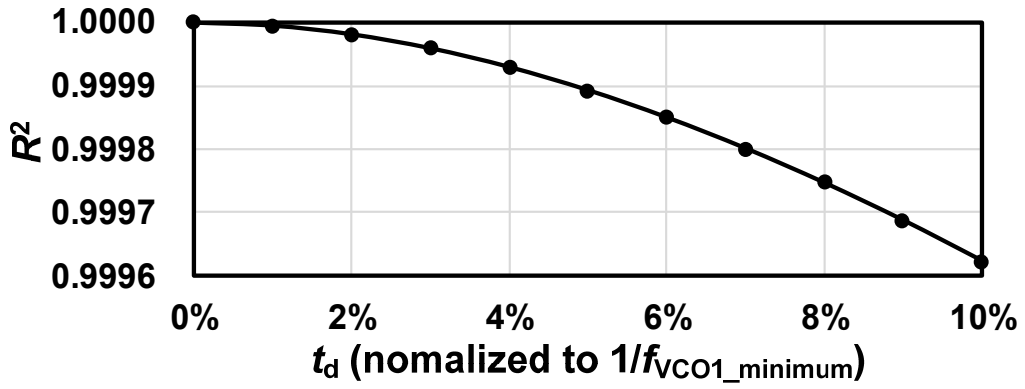

Fig. 5.16 The correlation coefficient of f_{VCO1} and C_{DUT} with different t_{d}.

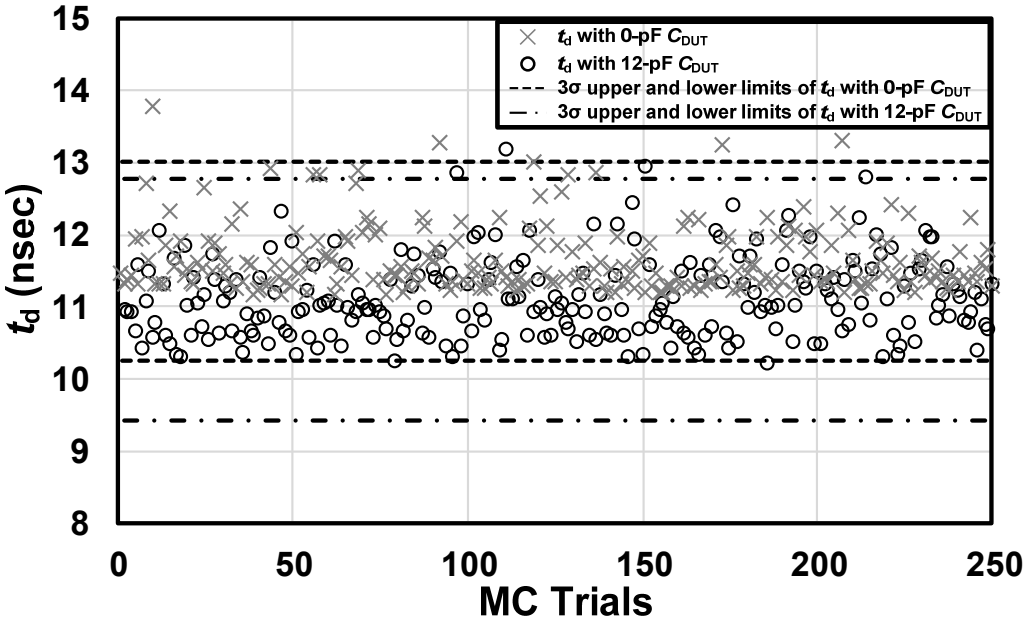

Fig. 5.17 The Monte-Carlo simulation results of t_{d} with 0-pF C_{DUT} and 12-pF C_{DUT}, respectively.

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correlation coefficient with different t_d is shown in Fig. 5.16. Fig. 5.17 shows the Monte-Carlo simulation results of t_d with 0-pF C_{DUT} and 12-pF C_{DUT}, respectively. Change of C_{DUT} does not affect t_d as much as it does to the T_{VCO1}. The average of t_d is about 11 nsec, which is 3.8% of maximum T_{VCO1}.

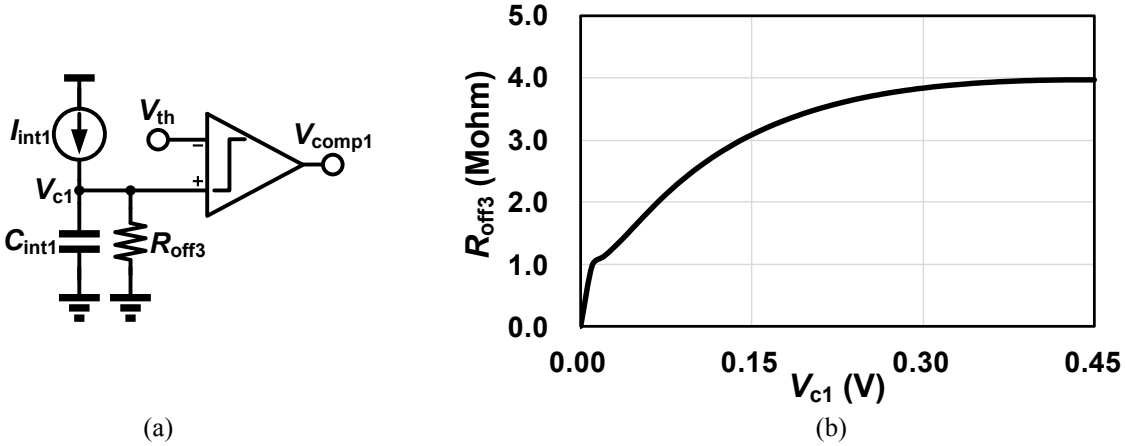
5.4.2 Leakage Current of the Reset Switch in VCO_1

The switch M_{s3} in Fig. 5.6 (b) is cut-off when C_{int} is charged by I_{int}. However, there is a small portion of I_{int} flowing through M_{s3} because of the finite resistance of the switch. By using R_{off3} to model the resistance of the cut-off switch as shown in Fig. 5.18 (a), the period of VCO_1 is given by

$$T_{VCO1} = R_{off3} \cdot C_{int} \cdot \ell n\left[1 \Big/ \left(1 - \frac{V_{th}}{I_{int} \cdot R_{off3}}\right)\right], \tag{5.24}$$

where R_{off3} is the equivalent resistance of the cut-off M_{s3}. Fig. 5.19 shows the frequency of VCO1 and normalized deviation between f_{VCO1} and its linear regression line versus C_{DUT} with different R_{off3}. As a result, a large cut-off resistance of M_{s3} is preferred for improving the linearity, which can be realized by choosing a small size of M_{s3} or increasing the length of the device. However, the on resistance of M_{s3} should be small enough to reset the cross voltage of the C_{int} during the reset time created by the delay cells in Fig. 5.7 (b). A device size of 2x10μm/0.1μm is chosen for the M_{s3} under the consideration of both on and off resistance.

In addition, R_{off3} varies with its cross voltage as shown in Fig. 5.18 (b). R_{off3} becoming smaller



(a) (b)

Fig. 5.18 (a) The schematic of VCO_1 with the equivalent resistance of the cut-off switch M_{s3}, and (b) the simulated value of R_{off3} with different cross voltage.

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when the cross voltage is low further degrades the linearity of the transfer curve of f_{VCO1} to C_{DUT}.

Fig. 5.20 shows f_{VCO1} and its normalized deviation with the varying R_{off3}.

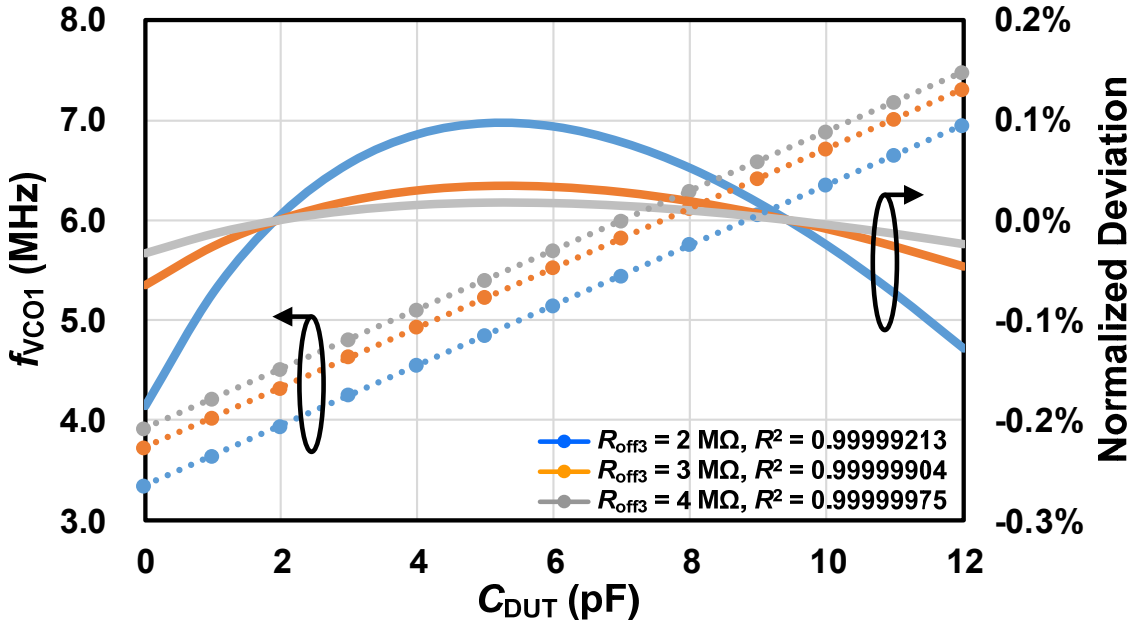

Fig. 5.19 Simulated f_{VCO1} and the normalized deviation between f_{VCO1} and its linear regression line versus C_{DUT}.

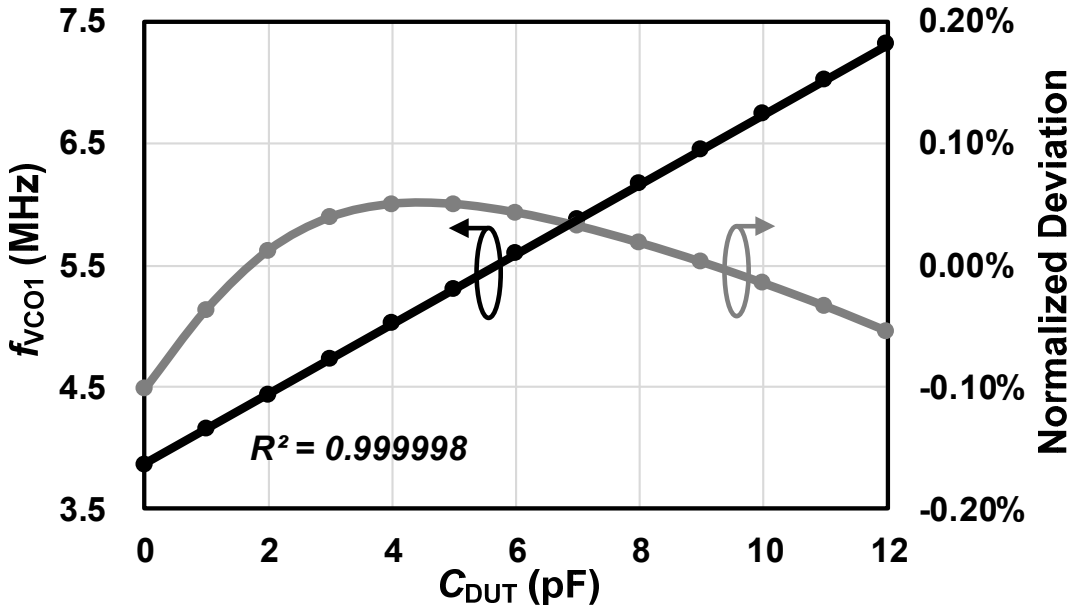

Fig. 5.20 Simulated f_{VCO1} and the normalized deviation between f_{VCO1} and its linear regression line versus C_{DUT} with the varying R_{off3}.

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5.4.3 Finite Output Impedance of I_{int}

The output impedance of I_{int} directly affects current flows to C_{int}. A small output impedance results in I_{int} changing with the cross voltage of C_{int}. Fig. 5.21 show the simulated I_{int} with different V_c by a single PMOS without cascoding, two cascoded PMOSes, and the output-impedance boosting technique adopted in this work, respectively. The threshold voltage provided by C2V according to different C_{DUT} is also marked in Fig. 5.21. Fig. 5.22 shows the normalized deviation between f_{VCO1}

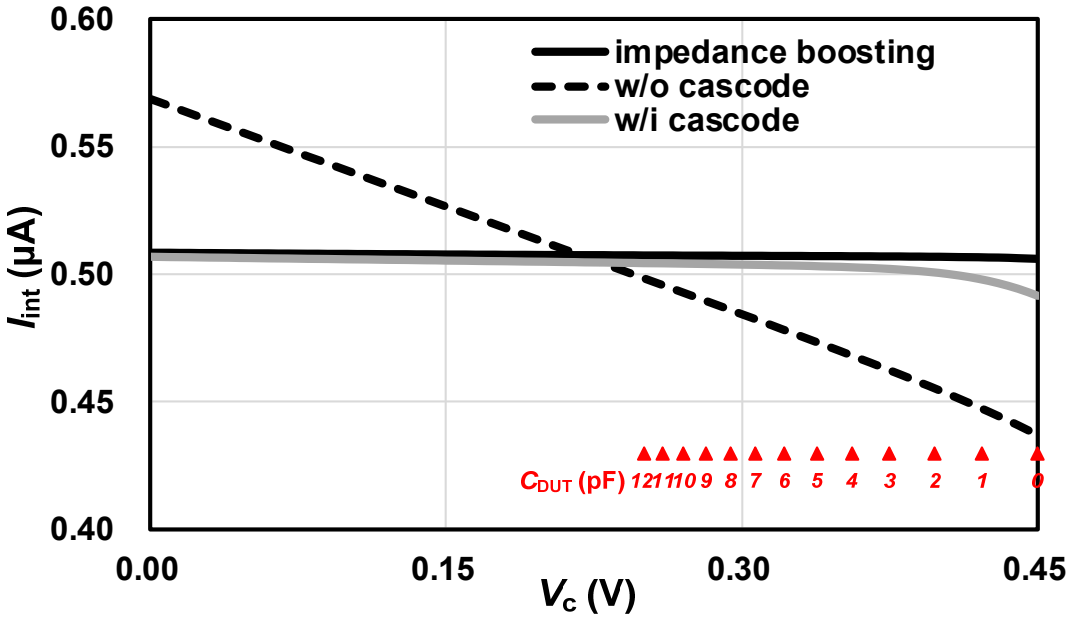

Fig. 5.21 Simulated I_{int} versus V_c with different generating methods.

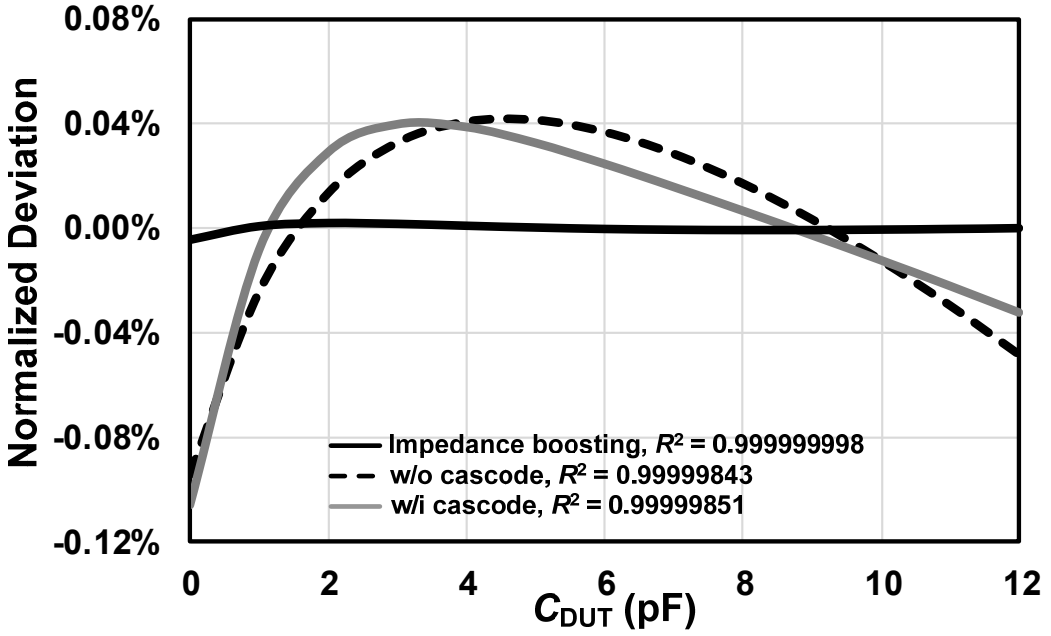

Fig. 5.22 Simulated normalized deviation between f_{VCO1} and its linear regression line versus C_{DUT} with the different I_{int} generating methods.

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and its linear regression line versus C_{DUT} with the different I_{int} generating methods. The deviation of cascoded PMOSes is close to that of a single PMOS owing to the curvature of I_{int} when C_{DUT} is small. The output-impedance boosting technique shows great linearity compared to other methods.

5.4.4 Leakage Current of the Switches in C2V

The C2V converter generates V_{th} by applying a step input to the series capacitors, the charge at the node of V_{th} is automatically redistributed to C_1, C_0, and C_{DUT} according to their values. Switches M_{s2up} and M_{s2dn} are added to reset the C2V, which also introduced additional leakage current when the switches are turned off. Fig. 5.23 (a) and (b) show the schematic of the C2V when V_{th} is held and equivalent resistors of the switches, R_{off2up} and R_{off2dn}, respectively. It is noted that the body of

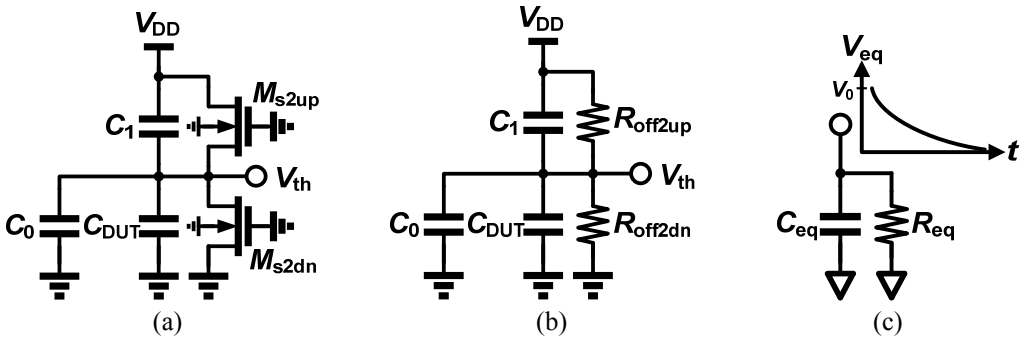

Fig. 5.23 The schematics of the C2V (a) when V_{th} is held, (b) by replacing the mosfets by their equivalent resistors, and (c) the equivalent RC discharging model.

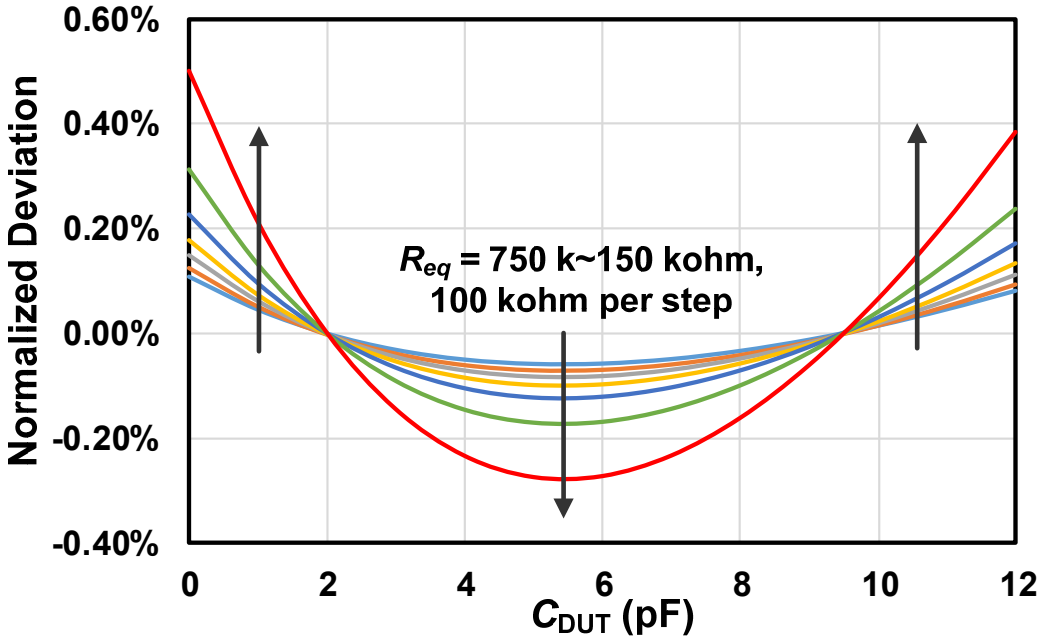

Fig. 5.24 Simulated normalized deviation between f_{VCO1} and its linear regression line versus C_{DUT} with different R_{eq}.

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the switches are connected to ground, which introduces the body effect and increase the threshold voltage of M_{s2up}. Combining with the negative V_{GS} of M_{s2up}, R_{off2up} is much larger than R_{off2dn} even though M_{s2up} has the same device size as M_{s2dn}. According to simulation, R_{off2up} is about 40 times of R_{off2dn}. The effect of leakage current to the output of C2V can be modeled by an RC discharging model as depicted in Fig. 5.23 (c). The values of R_{eq}, C_{eq}, and V_0 is given as

$$R_{eq} = R_{off2up} // R_{off2dn}, \tag{5.25}$$

$$C_{eq} = C_1 + C_0 + C_{DUT}, \tag{5.26}$$

$$\text{and} \quad V_0 = V_{th0} - V_{DD} \cdot R_{off2dn} / \left(R_{off2up} + R_{off2dn}\right) \approx V_{th0}, \tag{5.27}$$

where V_{th0} is the value of V_{th} right after the end of the step input and equals $V_{DD} \cdot C_1 / C_{eq}$. Then, the period of VCO_1 can be estimated by equating $V_{th}(t)$ and $V_c(t)$:

$$\begin{cases} V_{th}(t) = V_{th0} \cdot e^{\frac{-t}{R_{eq} C_{eq}}} & (5.28) \\ V_c(t) = \dfrac{I_{int} \cdot t}{C_{int}} & (5.29) \end{cases},$$

where $V_c(t)$ ignores the effect of leakage current in VCO_1 for simplicity. Fig. 5.24 shows the simulated normalized deviation between f_{VCO1} and its linear regression line based on (5.25)−(5.29). It is noted that the deviation due to leakage current in C2V has reversal trend compared to the other nonlinearity mentioned in 5.4.1 and 5.4.2. By adding an additional resistor between V_{th} and ground, the R_{eq} is made to be about 225 kohm, and the nonlinearity mentioned in 5.4.1 and 5.4.2 can be partially compensated.

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5.5 Measurement Results

The proposed CDC is fabricated by using a standard 1P9M 90-nm CMOS process. Fig. 5.25 shows the microphotograph of the fabricated circuit. The measurement setup is shown in Fig. 5.26, where the CDC chip is bonded with a printed circuit board (PCB) for testing. A Keysight B2926A Power Source is used to provide the supply voltage and biasing voltages for the CDC, and a Keysight 33622A Waveform Generator is used to provide the 0.6-V 900-ns *CLK*.

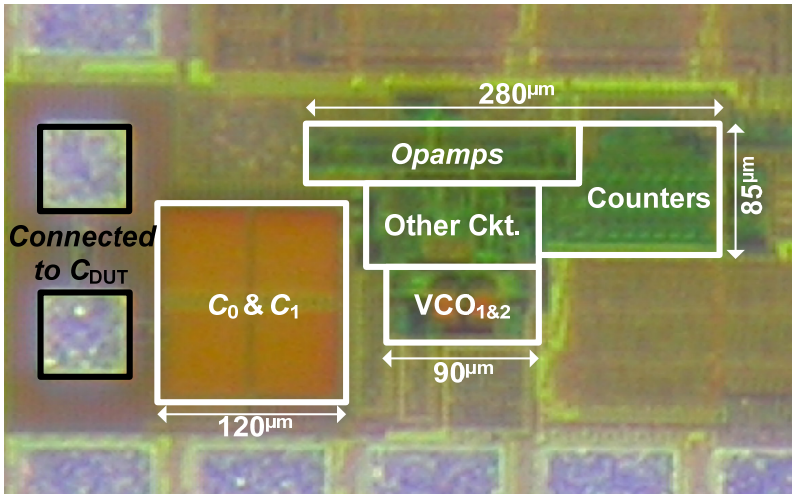

Fig. 5.25 The microphotograph of the fabricated circuit.

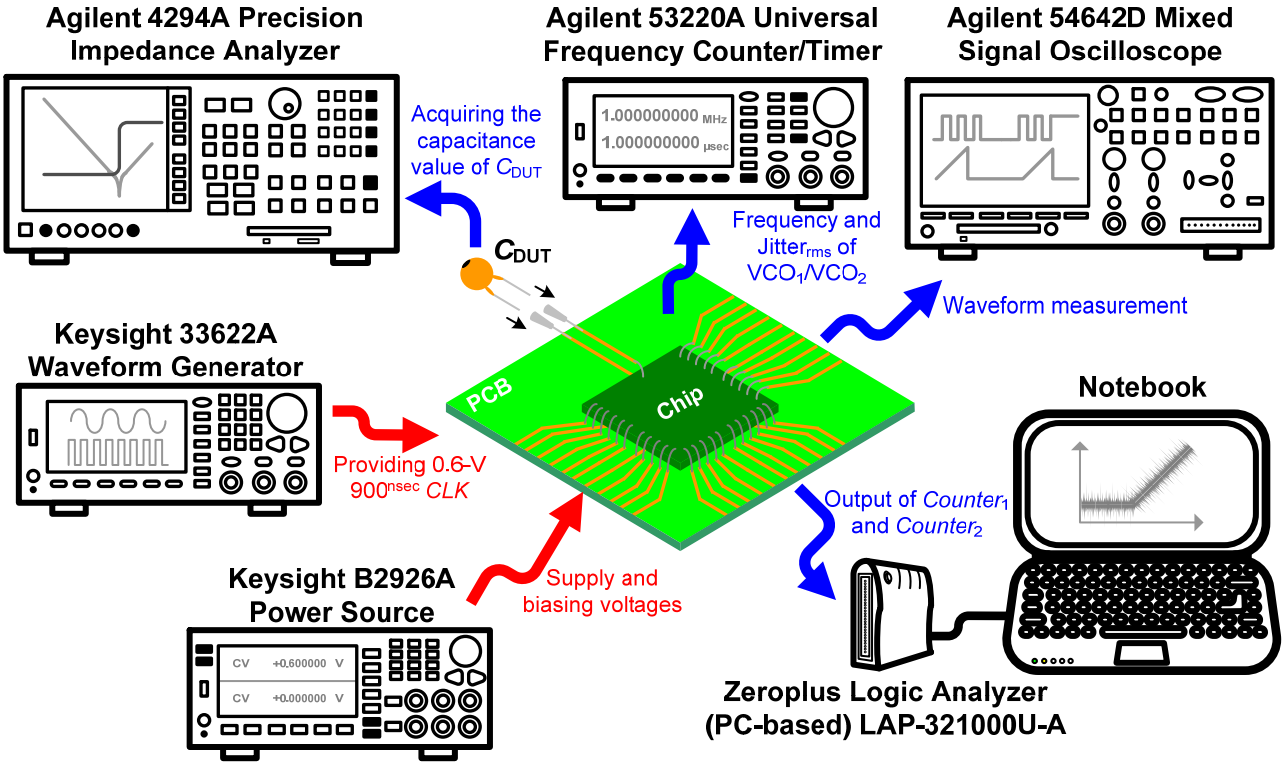

Fig. 5.26 The measurement setup.

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Table 5.2 Capacitors for Testing

C_{DUT}	C_{T1}	C_{T2}	C_{T3}	C_{T4}
pF	0.923488	2.02838	2.96895	3.94568
C_{DUT}	C_{T5}	C_{T6}	C_{T7}	C_{T8}
pF	4.91625	6.10603	7.00277	7.85888
C_{DUT}	C_{T9}	C_{T10}		
pF	9.92961	12.0595		

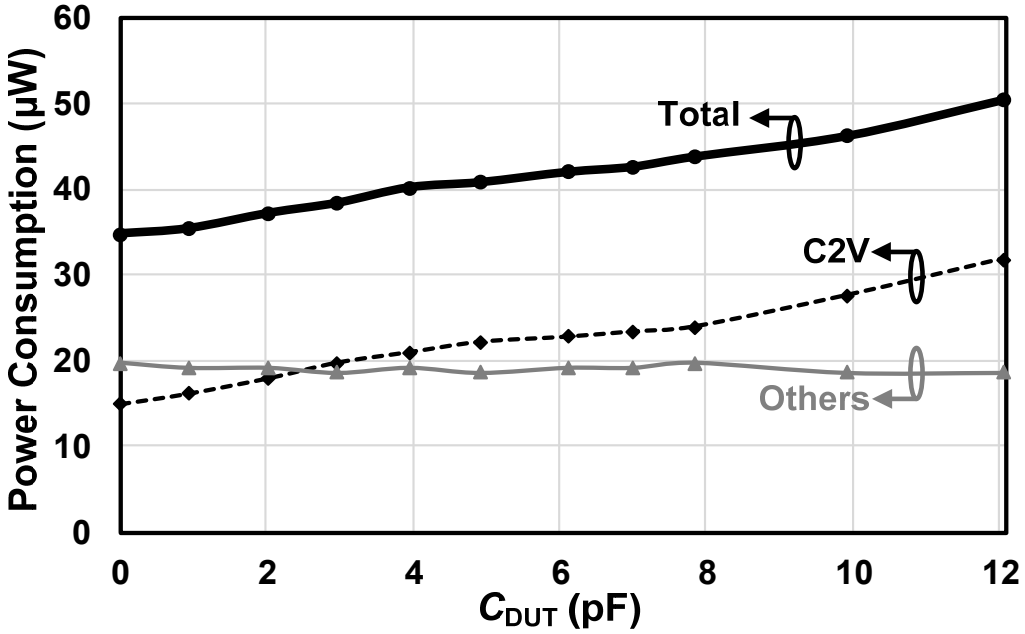

Fig. 5.27 The power consumption of CDC versus C_{DUT}.

An Agilent 53220A Universal Frequency Counter/Timer is used to characterize the period and rms jitter of the oscillators. Off-chip ceramic capacitors are adopted as the C_{DUT}, and their accurate capacitance values are characterized by an Agilent 4294A Precision Impedance Analyzer as tabulated in Table 5.2. The ceramic capacitors are then plugged into the socket mounded on the PCB. Via the PCB, one terminal of the capacitor is directly connected to the CDC and the other terminal is connected to the ground. Tested at a T_{CLK} of 900 ns, the CDC consumes a total power of 50.4−34.8 μW from a supply voltage of 0.6 V as the measurement buffers are excluded. Fig. 5.27 shows the power consumption of the CDC. The power of C2V increases with the C_{DUT}, and the power of VCOs and other digital blocks are nearly constant. Fig. 5.28 shows the measured frequency of VCO_1 with various capacitances as the C_{DUT}. The linearity of the transfer function of

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C_{DUT} to f_{VCO1} is also characterized by calculating the normalized deviation between f_{VCO1} and its linear regression line as shown in Fig. 5.29, which is much larger than expected. It is noted that the normalized deviation doesn't vary with V_{ref}, which means the deviation is not due to the ratio of t_d to T_{VCO1}.

Fig. 5.30 shows the comparison between the simulated result and measurement with different connections under the condition of V_{ref} equaling 0.5 V. If C_{DUT} is directly connected to the CDC or connected via a bondwire with an equivalent inductance about 2 nH, the deviation is successfully suppressed as mentioned in 5.4. However, the deviation becomes larger when an additional 2-cm wireline on PCB is adopted for connection. Fig. 5.31 The simulated waveform of V_{th} with different connecting methods. Fig. 5.31 shows the simulated output waveform of C2V versus different connecting methods with a 12-pF C_{DUT}. The step excitation occurs at 50 nsec. When the wireline on PCB involves in the connection, a large ringing waveform is observed in the simulation, which changes the output of C2V. Fig. 5.32 shows the measured waveform of Vth by using the load of probe as the device under test (1MΩ//12pF). Unfortunately, the wireline on PCB is not taken into consideration in the design phase, which is the author's mistake.

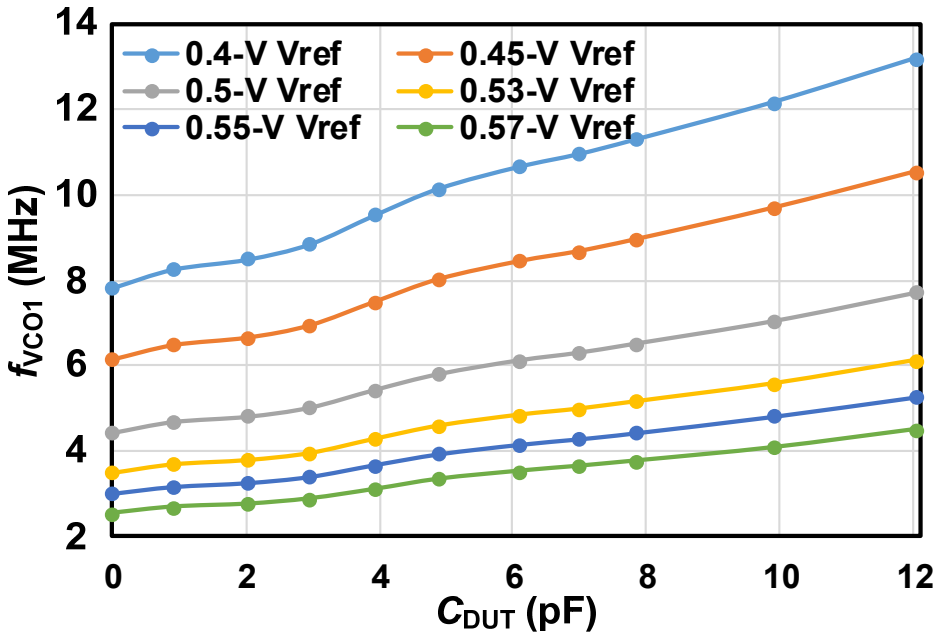

Fig. 5.28 The measured f_{VCO1} versus various C_{DUT} with different V_{ref}.

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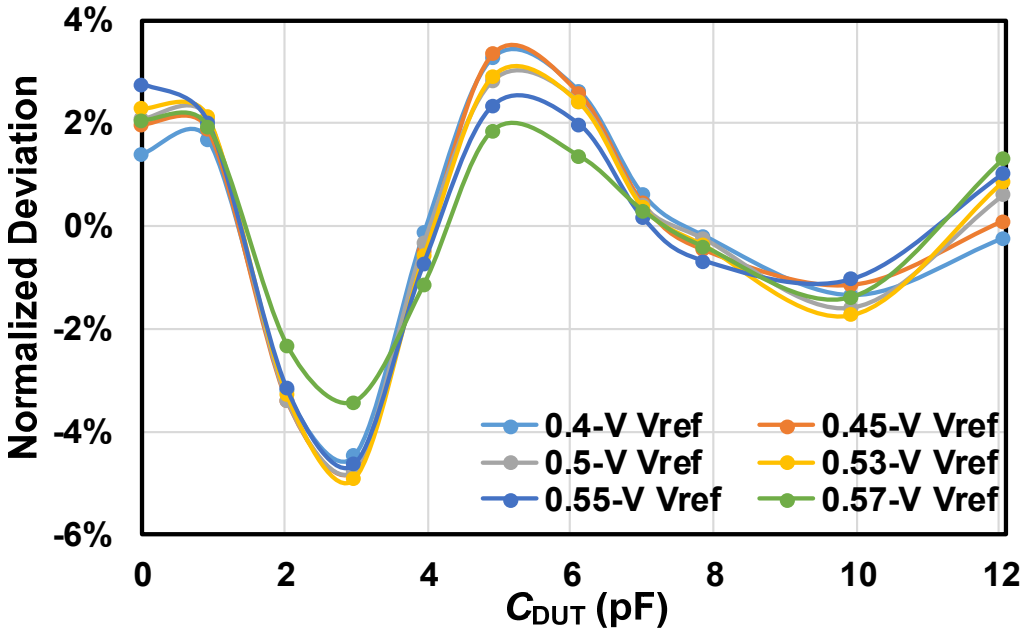

Fig. 5.29 The normalized deviation between f_{VCO1} and its linear regression line with different V_{ref}.

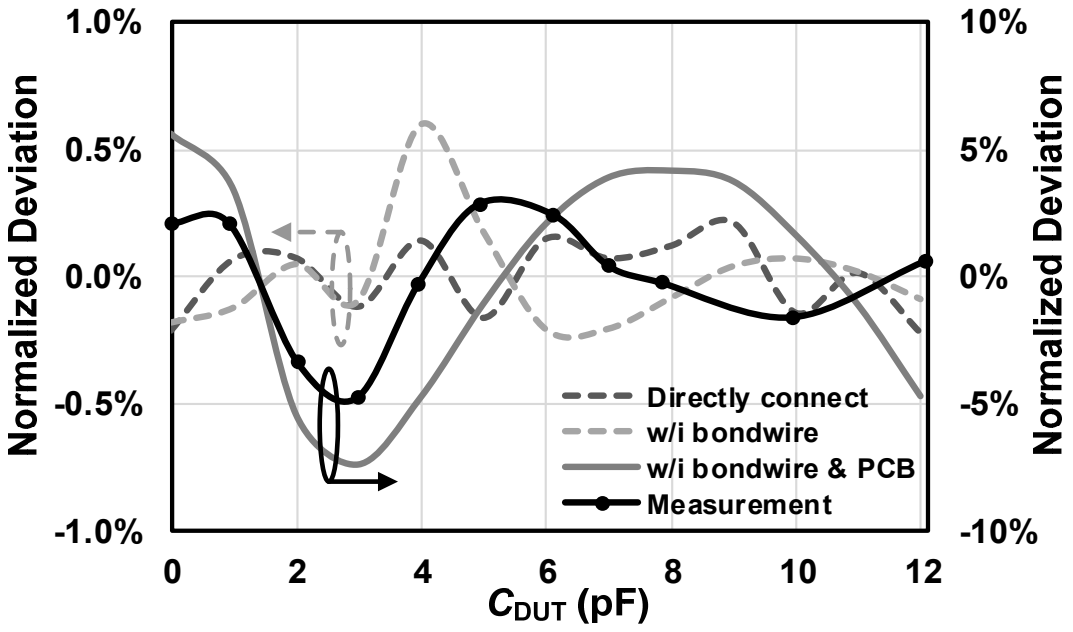

Fig. 5.30 The comparison of normalized deviation of f_{VCO1} in 4 cases: simulated result with C_{DUT} directly connected to the chip, simulated result of C_{DUT} connecting to the chip via a 2-nH bondwire, simulated result with C_{DUT} connecting to the chip via a 2-nH bondwire with the following PCB wire,and the measurement result.

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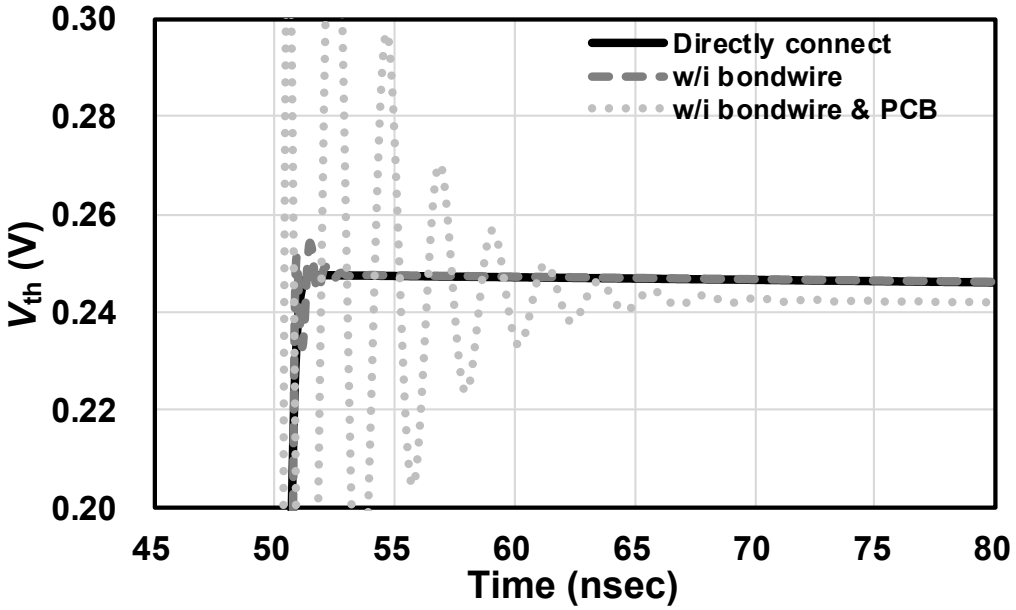

Fig. 5.31 The simulated waveform of V_{th} with different connecting methods.

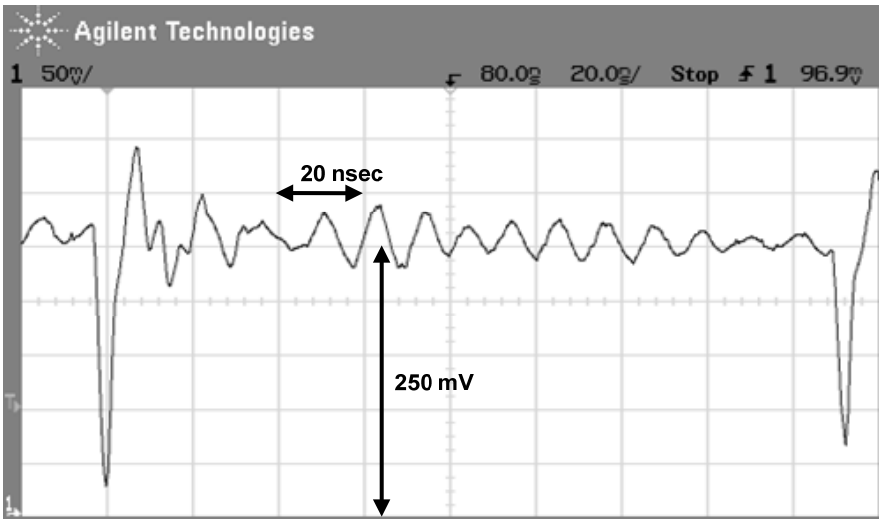

Fig. 5.32 The measured waveform of V_{th} by using the load capacitance of probe as C_{DUT}.

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The frequency of VCO_2 is also measured as shown in Fig. 5.33. The mismatch between VCO_1 and VCO_2 is about 10%. The rms jitter of VCO_1 and VCO_2 are measured and normalized to their period as shown in Fig. 5.34. The rms jitter of VCO_2 is larger than that of VCO_1 because of the C2V may be reset during the charging phase of VCO_2. Additional control circuits are added to prevent the comparator of VCO_2 change its state during the resetting duration.

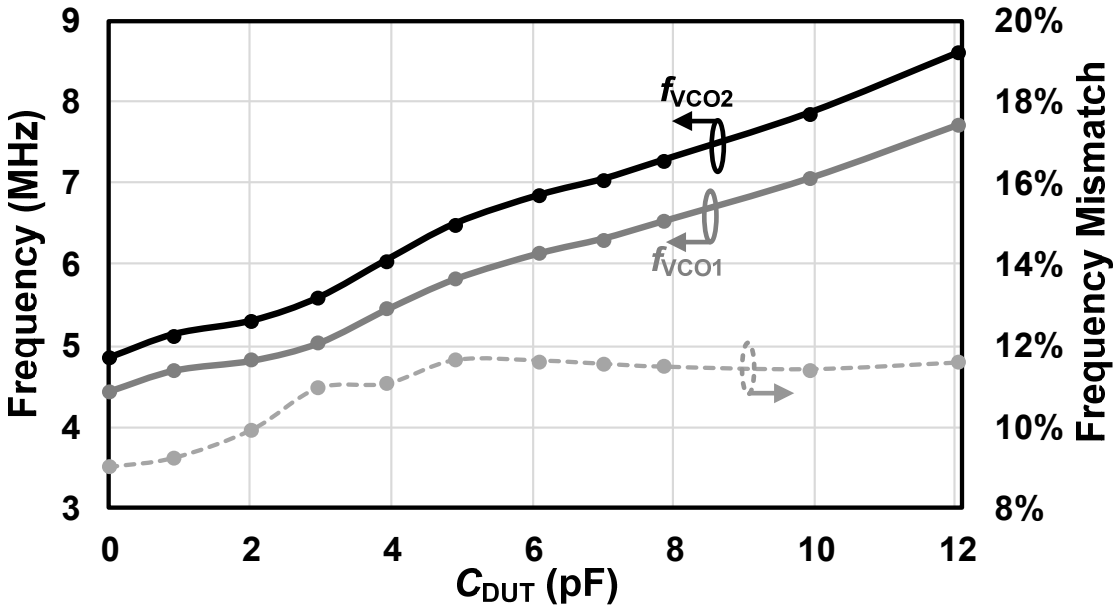

Fig. 5.33 The measured frequency and frequency mismatch of VCO_1 and VCO_2.

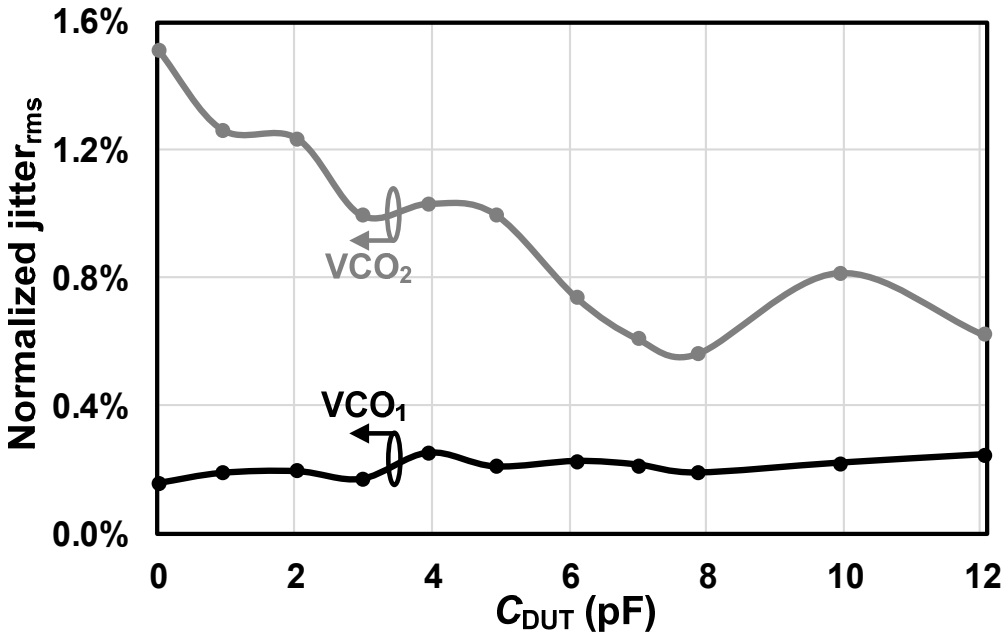

Fig. 5.34 The measured normalized RMS jitter of VCO_1 and VCO_2.

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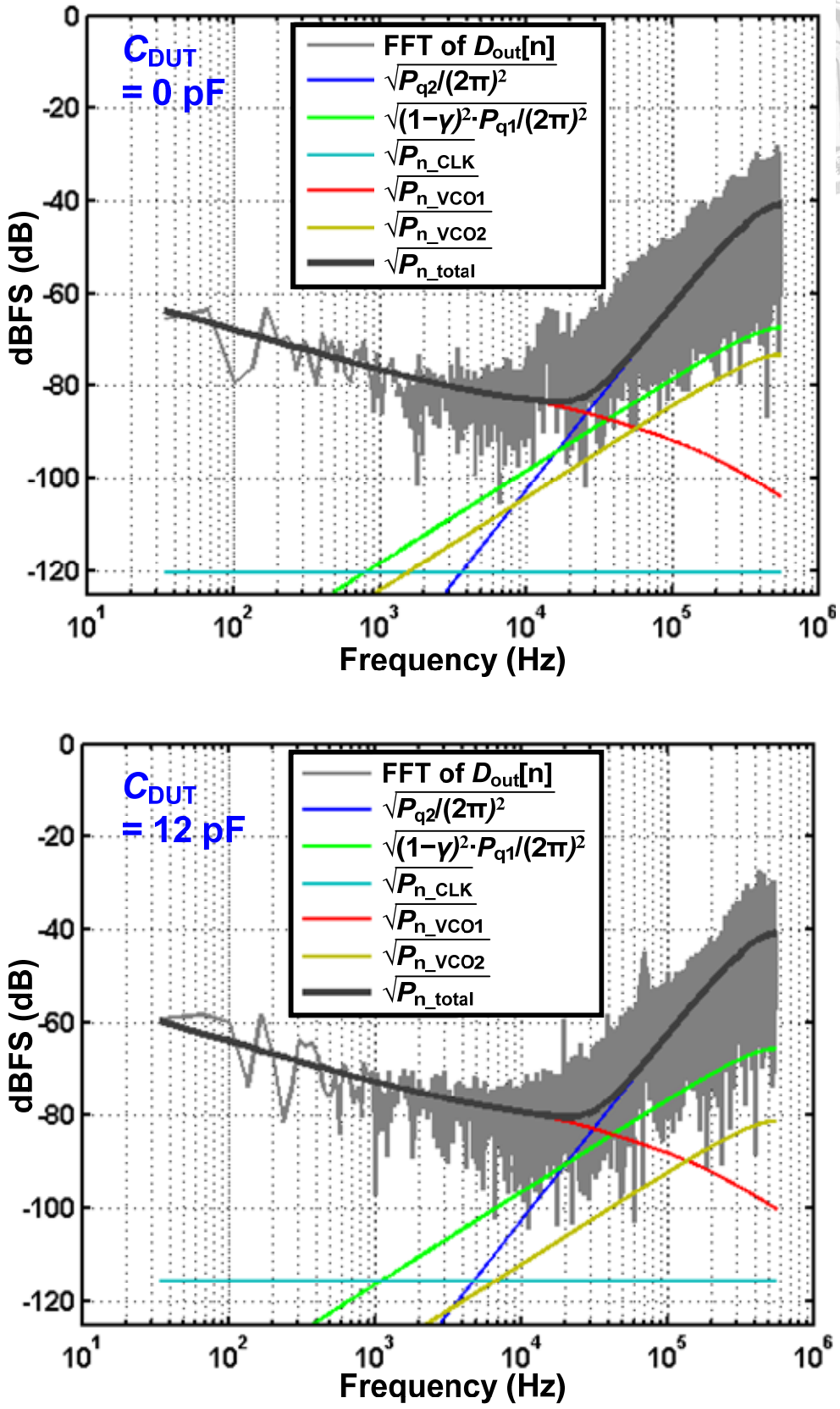

Fig. 5.35 The FFT results of D_{out} when C_{DUT} equals 0 pF and 12 pF, respectively.

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Finally, with values of C_{DUT} as listed in Table 5.2, the noise performance of the CDC is investigated. In order to obtain the conversion results, the output codes of CDC are recorded by a logic analyzer while a computer is utilized to perform the FFT. The FFT results are given by

$$D_{out}[n] = y_1[n] + 3 \cdot \left(y_2[n] - y_2[n+1] \right), \tag{5.30}$$

and the experimental results with C_{DUT} = 0 and 12 pF are demonstrated in Fig. 5.35, respectively. The estimation of non-ideal effects based on (5.17)−(5.22) is also provided in Fig. 5.35 to verify the circuit analysis with experimental results. The sampling frequency f_{CLK} is 1.111 MHz and the OSR is 64, which results the f_{BW} equals 8.68 kHz. The remaining 1st-order shaped quantization noise owing to period deviation is suppressed to a insignificant level in the in-band frequency. It is observed

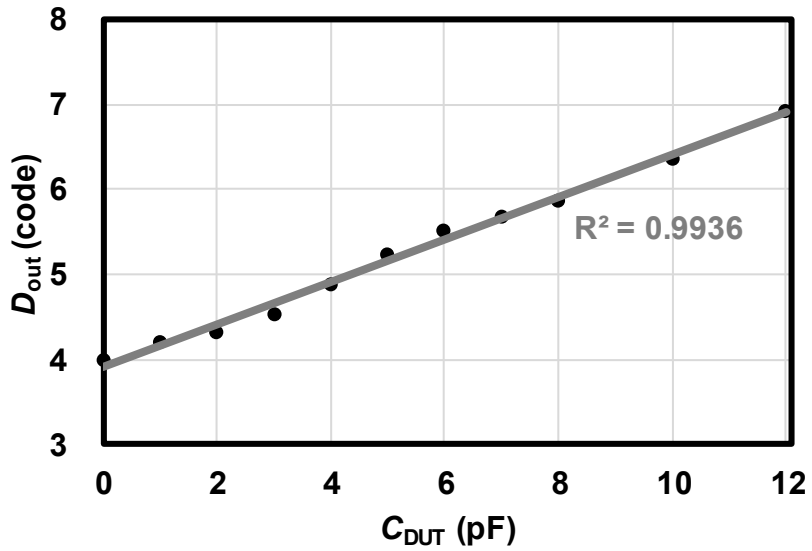

Fig. 5.36 The output of CDC with various C_{DUT} values.

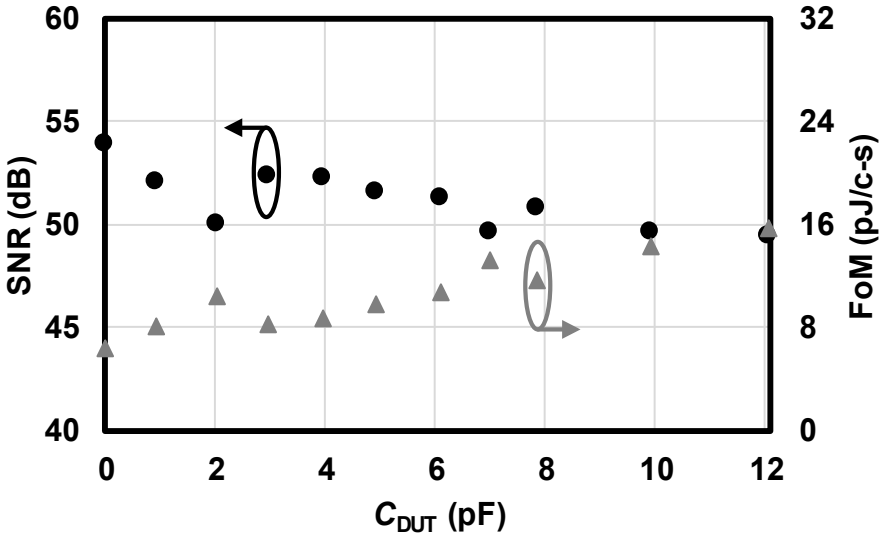

Fig. 5.37 The SNR and FoM of the proposed CDC with various C_{DUT} values.

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that the noise spectrum is dominated by the 2nd-order shaped quantization noise at high frequencies. On the other hand, the in-band noise floor is determined by the jitter of VCO_1, which can be estimated by the simulated noise voltage at V_{th}, V_{c1}, the input-referred noise voltage of the comparator, and the simulated voltage rising slope at V_{c1} in Fig. 5.6.

Fig. 4.24 shows the output of CDC with various capacitors as C_{DUT} with $R^2 = 0.9936$. The simulated R^2 of directly connected method and method of connecting the C_{DUT} via a bondwire are 0.999978 and 0.999901, respectively.

The SNR of the CDC output can be expressed by (4.20), and a figure-of-merit (FoM) for evaluating the overall performance of the CDC is given by (4.21) as the same as in Section 4.4, while f_{BW} is 8.68 kHz in this particular case. At various C_{DUT} values, the SNR and FoM are shown in Fig. 5.37. The SNR doesn't change significantly with the value of C_{DUT}. However, due to the power consumption of C2V increases with the C_{DUT} as shown in Fig. 5.27, the FoM rises with the value of C_{DUT}. The performance summary and comparison are provided in Table 5.3.

Table 5.3 Performance Summary and Comparison

Parameter	Unit	[40] TCAS-I'17	[39] ISSCC'14	[42] VLSI'14	[23] JSSC'13	[41] TCAS-I'14
Architecture	-	SAR	SAR	SAR +ΔΣ	ΔΣ	ΔΣ
Technology	nm	180	180	180	160	180
Area	mm^2	0.055	0.49	0.46	0.28	0.2
V_{DD}	V	0.8 & 1.2	0.9 & 1.2	1.4	1.2	1.6
Power	μW	6.44	0.16	33.7	10.3	80
Conv. Time or $1/(2{\cdot}f_{BW})$	μsec	16	4000	230	800	1000
Cap. Range	pF	12.66	10	24	0.52	3
Resolution	bit	11.6	8.9	15.4	11.1	14.2
FoM	pJ/c.-s.	0.033	1.33	0.179	3.76	4.25

Parameter	Unit	[43] JSSC'15	[44] ISSCC'15	[45] ESSCIRC'11	**Proposed Period-Mode CDC**	**This Work**
Architecture	-	Dual-slope	IDCD[a]	OSC-based	**OSC-based**	**OSC-based**
Technology	nm	180	40	130	**90**	**90**
Area	mm^2	0.1	0.0017	0.0725	**0.051**	**0.037**
V_{DD}	V	0.6 & 1.2	0.45 & 1	0.3	**0.6**	**0.6**
Power	μW	0.11	1.84	0.27	**8.04**	**50.4−34.8**
Conv. Time or $1/(2{\cdot}f_{BW})$	μsec	6400	19	1000	**62.5**	**57.6**
Cap. Range	pF	4	0.7−11.3	0.3	**15**	**12**
Resolution	bit	7	8	6.1	**8.8**	**7.9**
FoM	pJ/c.-s.	5.3	0.141	2.1	**1.16**	**10.6(average)**

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5.6 Summary

This chapter presents a frequency-mode oscillator-based time-mode delta-sigma CDC. A linearity compensation method is proposed by discussing all causes of nonlinearity in detail. Although the measured result is deteriorate by the parasitic effect of PCB connection, a highly linear performance can be expected when facing on-chip capacitive sensors or connecting the sensor and interface circuit directly by bond wires. In addition to derivations and analysis of the design constraints, the proposed circuit is fabricated in a 90-nm CMOS technology for verification. The fabricated chip is tested with off-chip capacitance ranging from 0 to 12 pF, demonstrating an equivalent bits of resolution of 7.9 bit with an FoM of 10.6 pJ/c.-s. with a bandwidth of 8.68 kHz.

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Conclusion

By pointing out the main challenge of achieving high frequency stability versus temperature is the delay time variation of the comparator, a 51.3-MHz CMOS relaxation oscillator is implemented in a 90-nm CMOS technology with the proposed integrated error feedback (IEF). Collaborating with composite resistors, the fabricated circuit demonstrates excellent frequency stability versus temperature and supply voltage variations. It is well suited for emerging applications where low-power operations are required. However, the poor jitter performance still remains to be solved when being adopted as the reference signal for wireless transmission.

Time-mode oscillator-based CDCs are introduced in this thesis as solutions for sensor interface circuits with the limited voltage head room in advance CMOS process. The oscillator-based CDCs is divided into period-mode and frequency-mode according to their frequencies are smaller or larger than the reference frequency, respectively. With the help of the comprehensive analysis of the noise contribution and the sequential search frequency calibration (SSFC), a period-mode oscillator-based CDC is implemented in a 90-nm CMOS technology with an equivalent bits of resolution of 8.8 bit and an FoM of 1.16 pJ/c.-s. In order to compare the characteristics of different modes of oscillator-based CDCs, a frequency-mode CDC is also implemented with a linearity error compensating method. In both CDCs, the comparison of measurement result and the mathematical analysis shows high agreement. A standard design flow can be established from the experience of implementing the oscillator-based CDCs in this thesis. First, by establishing the mathematical model of the CDC, the frequency relation of the oscillator and reference clock can be chosen according to the target resolution as shown in Fig. 4.3 and Fig. 5.3. Second, by using the simulation results such as: AC noise simulation, Monte-Carlo simulation, transient noise simulation, the non-ideal effects of flicker noise and frequency mismatch can be added into the mathematical model. Then, reexamining the frequency relation and making modifications. Finally, the parasitics due to measurement setups should be considered carefully to reproduce the performance of simulation in the silicon implementation.

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Table 6.1 Performance Comparison of Proposed Period-Mode/ Frequency-Mode CDCs

Parameter	Unit	Proposed period-mode CDC	Proposed frequency-mode CDC
Architecture	-	OSC-based	OSC-based
Technology	nm	90	90
Area	mm^2	0.051	**0.037**
V_{DD}	V	0.6	0.6
Power	μW	**8.04**	34.8−50.4
Power by parts	μW	CCO 6.04 RCO 1.13[a] Others 0.87[a]	C2V 15−31.8 VCO_1 9.1[a] VCO_2 8.1[a] Others 2.6[a]
Freq. of OSCs	MHz	0.35−0.93 & 1.1	4.4−7.7 & 4.8−8.6
Freq. of CLK	MHz	3.333	1.111
Normalized rms Jitter	‰	0.97[c]/3.8[d]	2[e]/9.5[f]
f_{BW}	kHz	8	8.68
Cap. Range	pF	15	12
Resolution	bit	**8.8**	7.9
Linearity Error	%	-0.57/+0.54	-4.76/+3.34 **-0.22/+0.22** (expected)
FoM	pJ/c.-s.	**1.16**	10.6 (average)

[a] Estimated with simulation results.
[b] Jitter of CCO.
[c] Jitter of RCO.
[d] Jitter of VCO_1.
[e] Jitter of VCO_2.

The detail performance comparison of proposed period-mode and frequency-mode CDCs is given in Table 6.1. The resolution of period-mode and frequency-mode CDC is dominated by the normalized rms jitter of the CCO and VCO_1, respectively. The reason is that the in-band noise floor is dominated by CCO and VCO_1 as observed in Fig. 4.23 and Fig. 5.35. The period-mode CDC benefits from the topologies of CCO and RCO, only one voltage comparator with static power consumption is adopted. As the result, the power consumption of oscillators is smaller than that in the frequency-mode CDC. However, the frequency of RCO in the period-mode CDC is suffered from process variation, an additional SSFC is required. The chip area and system complexity of the period-mode CDC are increased. The total power consumption of frequency-mode CDC is much larger than that of period-mode CDC, which is due to the power consumption of C2V. The C2V may be removed if a new topology of CCO is found, which has a frequency proportional to the capacitance.

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