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毫米波除頻器及相移器之研究

Research on Millimeter-Wave Frequency Dividers and Phase Shifters

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本論文係林毓軒君（F99942093）在國立臺灣大學電信工程學研究所完成之碩（博）士學位論文，於民國 106 年 12 月 29 日承下列考試委員審查通過及口試及格，特此證明

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中文摘要

本論文主要分為兩部分，分別是毫米波寬頻除頻器和毫米波低相位移和振幅誤差之相移器。

第一部分是有關毫米波寬頻除頻器的研究。除頻器是鎖相迴路中的關鍵電路之一，在毫米波頻段的米勒除頻器(Miller frequency divider)和注入鎖定式除頻器(Injection-locked frequency divider)廣泛的被使用，然而和低頻率的除頻器相比頻寬受到相當大的限制，因此本論文提出兩個方法，用來改善兩種毫米波除頻器的頻寬。第一個除頻器是操作在 60GHz 且使用 65 奈米 CMOS 製程製作的米勒除頻器。此除頻器使用了弱反轉區(weak inversion region)偏壓的混頻器使其能達到 57%的鎖定比例頻寬(35.7 至 64.2 GHz)，而且功耗僅 1.6 毫瓦。第二個除頻器是使用分裂式變壓器耦合振盪器(split transformer-coupled oscillator)的注入鎖定式除頻器。使用了此架構的注入鎖定式除頻器可以增加操作頻率和鎖定頻寬且不會增加額外晶片面積及功率消耗。此注入鎖定式除頻器在不需要額外調控機制下達到 25.4%的鎖定比例頻寬(75.1 至 97 GHz)，且在 0.7V 供給電壓下有 2.45 毫瓦的功率消耗。

第二部分是有關應用在 60GHz 相位陣列的毫米波低相位移和振幅誤差之相移器設計。相移器為相位陣列(phased array)系統中的關鍵元件，本論文中，設計了一種低相位移和振幅誤差的四相位旋轉器由四相位產生器和相位選擇器所組成，用以搭配射頻(RF)端和本地振盪源(LO)端相移器，使這兩個相移器皆能達到 360 度的相移而且具有低相位移和振幅誤差的特性。射頻端相移器是基於開關式相移器所設計，是全被動的架構且達到四位元的數位式控制。此相移器最大均方根振幅誤

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差為 0.5dB，最大的均方根相位誤差為 5 度。另一個本地震盪源端相移器使採用注入鎖定式架構，此相移器達最大震幅誤差為±0.3 dB，最大相為誤差為 5 度。具有 -10 B dBm 的輸出功率和 18 毫瓦的功率消耗。

關鍵字 ： 互補式金氧半場效電金體、除頻器、變壓器、振盪器、注入鎖定、相移器

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ABSTRACT

This dissertation consists of two main parts, the first part is design of wide band-width millimeter-wave (MMW) frequency divider, and the second part is about 60 GHz phase shifter with low phase and amplitude error.

In the first part, two MMW frequency dividers for MMW PLL are presented. The first frequency divider is 60 GHz Miller divider demonstrated in 65 nm CMOS. The Miller divider achieves 57% input locking range from 35.7 to 64.2 GHz with power consumption of 1.6 mW owing to using weak inversion bias mixer. The second frequency divider is a W-band injection-locked frequency divider (ILFD) fabricated in 90 nm CMOS, The STCO (split transformer-coupled oscillator) technique is proposed and utilized in ILFD and the operation frequency and locking range of the proposed ILFD can be increased without extra chip area and power consumption. The input locking range is 25.4% from 75.1 to 97 GHz at 0-dBm input power without any frequency tuning mechanism. The dc power consumption is 2.45 mW with a 0.7-V supply voltage.

The second part is about phase shifter design for 60 GHz phased array system. A RF phase shifter and a LO phase shifter are presented and fabricated in 90 nm CMOS. The quadrature phase rotator (QPR) included vector generator and vector selector is proposed and applied in both phase shifter to achieve 360° phase shift with low phase and amplitude error. The proposed RF phase shifter based on STPS (switch type phase shifter) is all passive and fully digital control with 4 bit resolution. It demonstrates the maximum RMS amplitude error of 0.5 dB and phase error of 5°. Another proposed LO phase shifter based on ILPS (injection-locked phase shifter) exhibits the maximum am-

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plitude error of ±0.3 dB and phase error of 5°. The output power of the proposed LO phase shifter is -10 dBm with 18 mW dc consumption.

Index Terms – CMOS, frequency divider, oscillator, phased array, phase shifter.

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Chapter 1 Introduction

1.1 Background and Motivation

As modern CMOS technology continuous to scale down, millimeter wave (MMW) wireless systems have drawn lots of attention. Recently, MMW frequency band have been allocated for different wireless application, as shown in Fig. 1.1. The 57 to 64 GHz unlicensed band have been released for short range communication [1]. According to IEEE 802.15.3c standard [2], the band around 60 GHz can be divided into four 2.16 GHz channels. It is capable of achieving data rate of 3.5Gbps/Ch in QPSK modulation and 7 Gbps/ch in 16 QAM modulation. Besides, 71-76/81-86 GHz licensed band are reserved for point-to-point communication [3]. Total of 10 GHz bandwidth can be utilized in E-band for high capacity link. In addition to wireless communication application, 77 GHz and 94 GHz are planned for automotive anti-collision radar and image sensor, respectively [4]-[5].

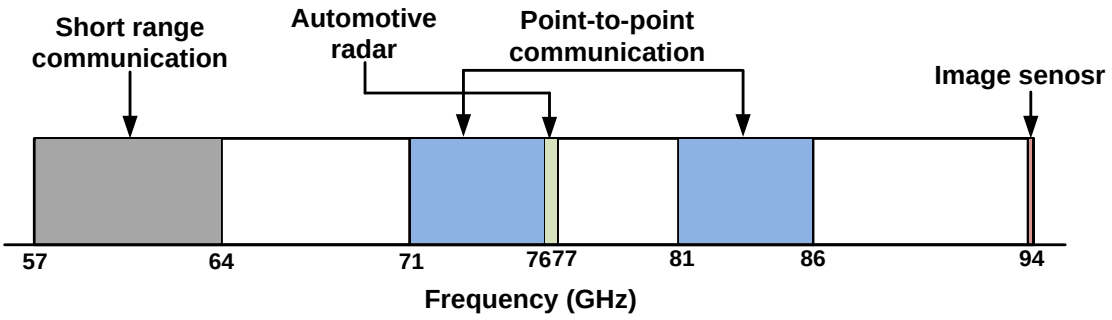

Fig. 1.1. The frequency allocation for MMW application.

In MMW wireless system, the Phase lock loop (PLL) is a key building block to provide local oscillator source. Fig. 1.2 shows the block diagram conventional PLL

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which included a phase frequency detector (PFD), a charge pump (CP), a loop filter, a voltage-controlled oscillator (VCO) and frequency dividers. The most challenge components of MMW PLL are VCO and frequency divider. The VCO in CMOS process can operate in very high frequency, but frequency tuning range, phase noise, power consumption, and output power are still the design issue. On the other hand, the CMOS frequency divider such as Miller divider and injection-locked frequency divider (ILFD) can operate in MMW frequency easily. However, the bandwidth is narrow compared with frequency divider at low frequency. Besides, the bandwidth of frequency divider should be designed much wider than tuning range of VCO due to process-voltage-temperature (PVT) variation. In this dissertation, two wide bandwidth MMW frequency dividers with low power consumption are proposed for low power MMW PLL design.

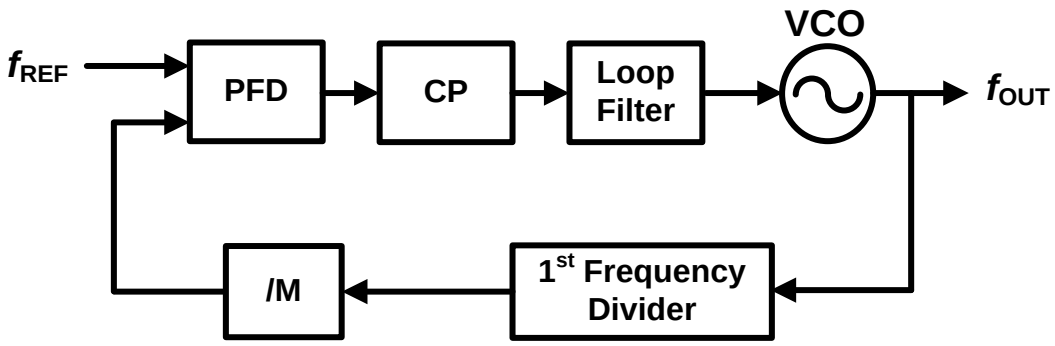

Fig. 1.2. Block diagram of conventional PLL.

Since the free space loss in MMW frequency is tremendously higher than that in microwave frequency and the output power provided by power amplifier is lower, the radiation region is limited. Phased array system which is a multi-channel transceiver is developed to solve this problem. It can increase the output power and system sensitivity

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by combining the coherent signal in space. Also, the radiation beam can be steered by changing the phase in each channel. Phased array systems require phase shifter to control the phase in each channel path. However, there are several design challenges such as loss, phase error, amplitude error, and phase resolution. This dissertation proposes two architectures of phase shifter for two type of phased array system to solve these issues.

1.2 Literature Survey

1.2.1 MMW frequency dividers

In MMW PLL, the design of first-stage frequency divider is as critical as VCO since PLL require reliable tracking and lower power consumption. For MMW frequency, static frequency divider, Miller frequency divider, and ILFD are widely applied in MMW PLLs.

Static frequency divider has wide bandwidth performance. It can work at MMW frequency by using current mode logic (CML) topology. A wide bandwidth frequency divider demonstrates operation frequency from 5 to 66 GHz [6]. To reach higher frequency, another static frequency divider in W-band frequency has been presented [7]. However, the power consumption increases tremendously with increasing operation frequency. Also the bandwidth is constrained in high operation frequency. Miller divider is mixer-based frequency divider can operate at MMW frequency easily with moderate bandwidth and power consumption. Two Miller dividers operated in V-band have been reported [8], [9]. The two Miller dividers are applied the techniques of current bleeding

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and transformer injection, respectively. The power consumption is much lower than static frequency divider. Nevertheless, the maximum operation frequency is still limit. Among all frequency divider, ILFD has the highest operation frequency and the lowest power consumption. Three ILFD have been demonstrated in V-band and W-band frequencies with quite low power consumption, but their bandwidth is narrower [10]-[12]. In order to enhance the operation bandwidth, the ILFD with dual-mixing technique has been proposed [13]. The locking range is improved significantly with additional power consumption. The other methods to improve the locking range without extra power consumption are distributed LC structure and inductor peaking technique [14], [15]. Both the methods require multiple inductors and result in large chip area.

Table 1.1 summarizes the comparison of reported MMW frequency divider. Although Miller dividers consume much lower power consumption than that of CML divider, the operation bandwidth is still limited. On the contrary, thanks to certain techniques proposed and applied in ILFD, the bandwidth is extend significantly. The ILFD shows the great potential for MMW PLL integration.

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Table 1.1. Summary of reported MMW frequency divider

Ref.	Process	Topology	Input Frequency (GHz)	Bandwidth (GHz)	Input Power (dBm)	V_{DD} (V)	P_{DC} (mW)	FOM
[6]	90 nm CMOS	CML	5-66	51 (171%)	0	1.4	44.6	1.14
[7]	65 nm CMOS	CML	76-94.4	18.4 (21.6%)	0	2.4	64.9	0.28
[8]	0.13 μm CMOS	Miller	56.5-72.2	15.7 (24.4%)	0	1	4.65	3.37
[9]	0.13 μm CMOS	Miller	57-72	15 (23.2%)	0	0.8	5	3
[10]	65 nm CMOS	ILFD	82-94.1	12.1 (13.7%)	0	0.56	3.92	3.09
[11]	0.13 μm CMOS	ILFD	67.2-75.4	8.2 (11.5%)	0	1	4.4	1.86
[12]	90 nm CMOS	ILFD	85.5-96.2	10.7 (11.7%)	0	1.2	3.5	3.06
[13]	90 nm CMOS	ILFD	51-74	23 (36.8%)	0	0.5	3	7.67
[14]	65 nm CMOS	ILFD	107.9-128.8	20.9 (17.7%)	-2	1.1	6.27	3.33
[15]	65 nm CMOS	ILFD	53.4-79.4	26 (39.2)	0	`0.8	2.9	8.97

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1.2.2 MMW phase shifters

Several topologies of phase shifter have been utilized in phased array system. The transmission line phase shifter (TLPS) is simple way to achieve continuous phase shift but the phase shift range is narrow [16]. Wider phase shift can be obtained by adding more stages of TLPS, but insertion loss will be degraded. Therefore, TLPS is seldom used in MMW frequency. Another way to perform wider continuous phase shift is reflection type phase shifter (RTPS), but phase shift range is limited by reflection load [17]. The phase shift range can be enhanced by modifying reflection load. However, wider phase tuning cause higher reflective loss variation. Several MMW RTPSs have been published in silicon process [18]-[20]. Single RTPS can cover 180° phase shift but suffer from high loss variation [18]. Casacading multiple RTPSs can achieve similar phase shift and reduce the loss variation [19], [20]. To reach full 360° phase shift, vector sum phase shifter (VSPS) is proposed. This phase shifter provides continuous phase shift by synthesizing quadrature signals [21]. By adjusting each path signal gain level, the arbitrary phase shift can be obtained. Among all VSPS, quadrature phase generator is a key component to generate accurate quadrature signal. Quadrature all-pass filter (QAF) consisted of lumped inductors and capacitors is used as quadrature phase generator in VSPS [21],[22]. However, in MMW frequency, the bandwidth of QAF is limited. Owing to the operation frequency extended to MMW region, a few microwave passive component technique can implemented in CMOS process, such as 90° coupler and left hand transmission line. Those are applied in VSPS for quadrature signal generation and achieve good phase and amplitude accuracy [23], [24]. Nevertheless, VSPS require more building block which cause higher power consumption and larger chip area.

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In addition to continuous tuning phase shifter, the discrete phase shift control can be achieved by switch type phase shifter (STPS) [25]. Phase shift in STPS can be controlled by digital signal without digital-to-analog converter (DAC). It is more convenient than other topology and save DC power of DAC. Traditional STPS is utilized switching low pass and high pass network to obtain certain phase shift. However, the chip size is larger due to low pass and high pass network. Also, the parasitic resistance of switch cause high loss. Two type of low pass filter (LPF) based STPS have been proposed to reduce the chip size and loss by reduce the passive component and number of switch [25], [26]. Nonetheless, both the above STPS cannot cover more than 90° phase shift. The great advantage of STPS is that *N*-bit digital control 360° phase shifter can be easily implemented by series connecting *N*-stage STPS [25]-[29].

Recently, injection-locked phenomenon has been used for achieving phase shift and it is suitable to use in LO path phased array [30] due to the low power consumption. However, the drawback is the narrow phase tuning range limited by injection-locked mechanism. Several injection-locked phase shifters (ILPSs) cascading with multiplier have been proposed to multiply phase shift tuning range [31]-[33].

Table 1.2 summarizes the performance of reported MMW phase shifter. All kind of phase shifters can be applied in phased array system depends on different system requirement. Among all phase shifter, Only STPS can work without dc power and extra DAC. Therefore, STPS is the better choice for large scale phased array transceiver.

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Table 1.2. Summary of reported MMW phase shifter

Ref.	Process	Topology	Freq. (GHz)	Phase Range	Resolution	Insertion Loss	P_{DC} (mW)
[18]	0.13 μm SiGe	RTPS	57-64	180	Continuous	4.2-7.8	0
[19]	65 nm CMOS	RTPS	55-65	180	Continuous	5-8.3	0
[20]	0.12 μm SiGe	RTPS	57-66	200	Continuous	6.3-8.2	0
[22]	90 nm CMOS	VSPS	40-67	360	22.5 (Extra DAC)	5-9	23
[23]	90 nm CMOS	VSPS	57-64	360	22.5 (Extra DAC)	3.4-7.2	34
[24]	90 nm CMOS	VSPS	57-66	360	22.5 (Extra DAC)	2.2-5	15.6
[27]	90 nm CMOS	STPS	57-64	360	11.25	11.6-18	0
[28]	0.13 μm SiGe	STPS	67-82	360	22.5	15.5-23	0
[29]	65 nm CMOS	STPS	75-85	360	22.5	22.9-27	0
[31]	65 nm CMOS	ILPS	43-50	±90	22.5 (Extra DAC)	-	85*
[32]	90 nm SiGe	ILPS	57-61	±80	Continuous	-	117**
[33]	90 nm SiGe	ILPS	62-73	±300	Continuous	-	236*

* 4 element arrays

** 2 element arrays

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1.3 Contributions

In this dissertation, two MMW frequency dividers were demonstrated with wide locking range for MMW low power PLL applications. Besides, two MMW phase shifters with low phase and amplitude error are presented for 60 GHz phased array. The major contributions in this dissertation are described briefly as follows.

First, a 35.7 to 64.2 GHz Miller divider with weak inversion mixer is presented. Conventional Miller divider using Gilbert cell mixer have narrow bandwidth. Even though a few techniques are proposed, the fractional bandwidth is smaller than 25%. To enhance the locking range of divider and save power consumption, a Miller divider based on weak inversion mixer is proposed. Unlike conventional Miller divider, the weak inversion mixer is applied in proposed Miller divider due to its low dc power and low LO driving power. Much wider bandwidth and smaller dc power can be obtained in proposed Miller divider. The proposed Miller divider is implemented in 65 nm CMOS and exhibits 57% locking range from 35.7 to 64.2 GHz at an input power of 0 dBm while consuming 1.6-mW dc power at 0.4 V supply voltage. Compared to the previously reported CMOS MMW frequency dividers, the proposed divider achieves the widest fractional bandwidth without any frequency tuning mechanism.

For higher frequency operation, a W-band injection-locked frequency divider (ILFD) with low power and wide locking range is demonstrated. Split transformer-coupled oscillator (STCO) technique is proposed to enhance the operation frequency and relieve the oscillation condition. Besides, the STCO applied in ILFD can enhance the locking range without increasing chip area and dc power consumption. On the other

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hand, the optimum bias and the size of injection transistor are chosen to achieve wider locking range. The detail analysis and design procedure of proposed ILFD are described in this dissertation. The proposed ILFD is implemented in 90-nm CMOS and exhibits 25.4% locking range from 75.1 to 99 GHz at an input power of 0 dBm without any tuning mechanism. The core dc power consumption is 2.45 mW with a supply voltage of 0.7 V and the core chip size is 0.13×0.2 mm^2.

In second part, two 60 GHz phase shifters with low phase and amplitude error for the beam-forming systems are presented. Among different phased array architectures, RF and LO phased array are widely used in wireless application. Therefore, the proposed phase shifters are designed for RF and LO phased arrays, respectively. The quadrature phase rotator (QPR) which consists of a vector generator and a vector selector is used in two phase shifters to achieve 360° phase shift. The QPR also contribute low phase and amplitude error with small chip size. Two phase shifters are designed and fabricated in 90-nm CMOS process. The first phase shifter is RF phase shifter used LPF based STPS to obtain zero power consumption and full digital control. The modified design equations are derived to acquire more accurate phase response. Based on the derived equations, this RF phase shifter realizes 22.5° resolution and 360° phase range with the quadrature phase rotator (QPR). The measured insertion loss is 17.5 dB with loss flatness of ±0.4dB, and the measured RMS phase and amplitude error are < 5° and 0.5 dB, respectively, from 57-66 GHz. The second phase shifter is LO phase shifter based on ILPS for low power and high linear phase tuning range. Different from previous reported works [31]-[33], the proposed LO phase shifter composed of an ILPS cascade with QPR. With the QPR, the ILPS overcomes the weakness of low phase tuning

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range. The measured amplitude variation is within 0.3 dB, and maximum phase error is 5° at 60 GHz.

1.4 Dissertation Organization

This dissertation is organized as follow:

In chapter 2, the brief introduction of different kinds of frequency divider operated in MMW frequency is given first. Then, section 2.2 present a 60 GHz Miller divider with weak inversion mixer in 65 nm CMOS. In section 2.3, a wide locking range ILFD using split transformer coupled oscillator (STCO) is proposed. The detail analysis of proposed STCO and ILFD are included in this section. The summary of two MMW frequency dividers is shown in the end of this chapter.

In chapter 3, at first, the brief introduction of phased array system and different phased array architecture are described. Also different types of phase shifters are also mentioned. Then, two phase shifters with low phase and amplitude error are presented in section 3.4 and 3.5, respectively. This two phase shifters are designed with QPR and can be applied in RF and LO phased array system, respectively. The design methods and measurement results are presented in both phase shifters and summary are shown in the end of this chapter.

Finally, a brief conclusion of this dissertation will be given in chapter 4.

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Chapter 2 Millimeter-wave Frequency Divider Design

2.1 Overview of Frequency Divider

2.1.1 Static Frequency Divider [6], [7]

As shown in Fig. 2.2(a), a static frequency divider includes a flip-flop constructed by two latches in a negative feedback loop. This circuit works by continuously toggling the output state after every rising edge of clock. The mechanism effectively causes the output to toggle between one and zero at a half period of the input clock. Therefore, the frequency division is obtained. By driving differential input clock, the output quadrature output signals at half of the input frequency are provided by the two latches, as shown in Fig. 2.1(b). Since the latches can save the data permanently, the static frequency dividers can operate at very low frequency, and also have wide bandwidth performance. However, there is time delay between input and output, the maximum operation frequency is limit.

At low frequency, true single phase clocking (TSPC) latches are adopted in static frequency divider, due to its compact size, and no static power consumption. The rail-to-rail clock swings are required for correct operation. Also, it does not provide quadrature output. For high speed operation, the latch is implemented by current mode logic (CML), as shown in Fig. 2.2. This circuit is controlled by the clocked pair, $M_{5\text{-}6}$. It samples the input through input pair, $M_{1\text{-}2}$, and holds the data by cross-coupled pair $M_{3\text{-}4}$ as long as the loop gain of cross-coupled pair exceeds unity. Since the propagation delay of CML is smaller than TSPC, the CML can achieve higher speed. Although CML fre-

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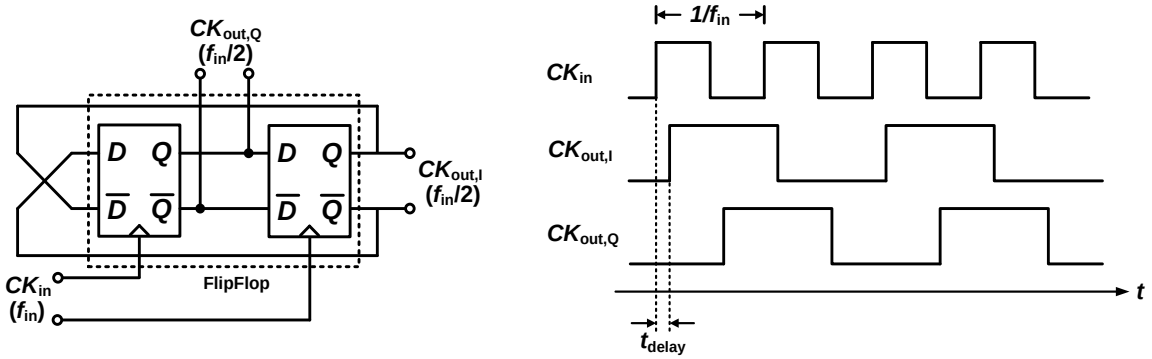
quency divider can operate at MMW region [6], [7], the tradeoff is requiring more power consumption to compensate the degradation of loop gain at high operation frequency. Another way to increase the operation frequency without extra power consumption is using inductor peaking technique. However, it has drawbacks of narrower bandwidth and larger area.



(a) (b)

Fig. 2.1. (a) Static frequency divider, and (b) its time domain waveform.

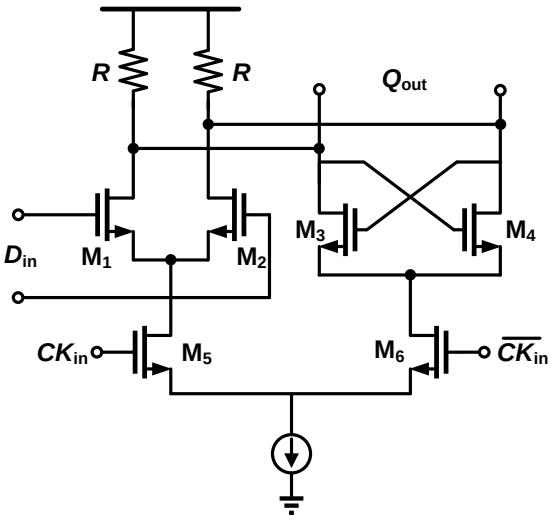


Fig. 2.2. D-latch of current mode logic (CML)

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2.1.2 Miller Frequency Divider [34], [35]

The Miller divider, or so-called regenerative divider, is originally proposed by Miller in 1939 [34] as shown in Fig. 2.3. The conventional Miller divider consists of a mixer and a low-pass filter (LPF) in a feedback loop. The mechanism is based on mixing the output and input signal and the result is applied to low-pass filter (LPF). The up-conversion signal is suppressed by LPF, and the divide-by-two signal is regenerated at output. Since the device parasitic capacitance can be absorb as part of LPF, Miller divider can achieve higher speed than static frequency divider. Besides, the phase and gain condition need to be satisfied. To realize the Miller divider with enough phase shift, the emitter follower is used in the Miller divider with BJT process as shown in Fig. 2.4 [35]. This topology is difficult to implement in CMOS process due to its low transconductance in a source follower configuration and low voltage headroom. To solve this problem, the Miller divider with inductive load has been proposed [35]. A band-pass filter (BPF) formed by LC-tank replaces the original LPF to suppress the high-order harmonic and ensure the loop gain at $f_{in}/2$ continually exceeds unity. Also, the BPF provide enough phase shift to achieve phase condition. Hence, the Miller divider in CMOS process can operate at MMW frequency.

Base on the difference of feedback path, the Miller divider with inductive load has two configurations. The output port could either feedback to the RF-port or LO-port of the mixer, as shown in Fig. 2.5. The RF-port feedback Miller divider needs extra capacitors to isolate the DC bias. The more parasitic capacitance may degrade the operation frequency and the loop gain. Therefore, the LO-port feedback Miller divider is more preferable in MMW frequency.

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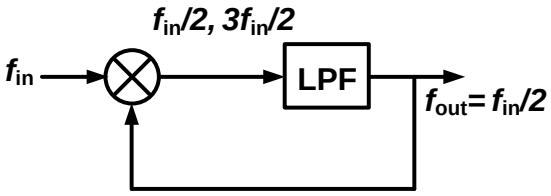

Fig. 2.3. The model of Miller frequency divider

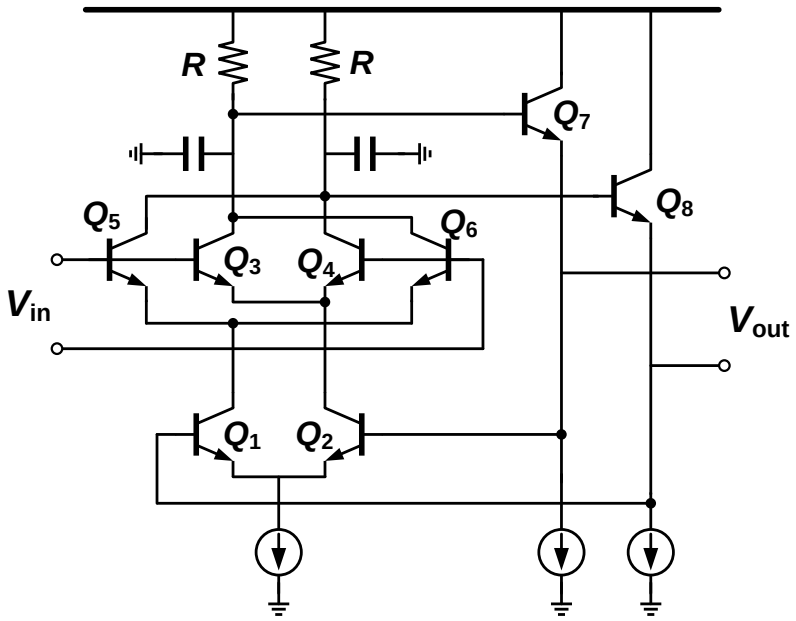

Fig. 2.4. Bipolar Miller divider

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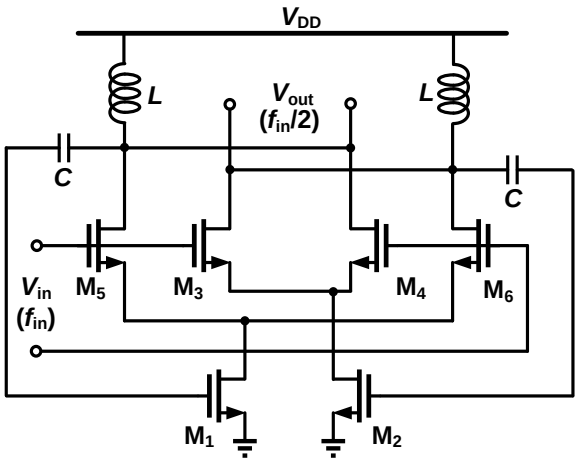
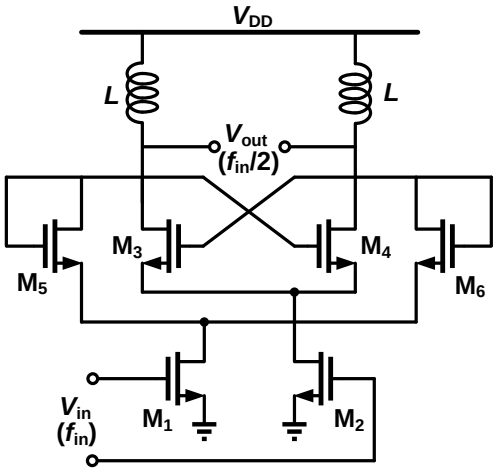


(a)



(b)

Fig. 2.5. (a) RF-port feedback Miller divider. (b) LO-port feedback Miller divider

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2.1.3 Injection-Locked Frequency Divider [36], [37]

Injection locking is a phenomenon which can be observed in all kinds of oscillators. When an oscillator is injected by an external signal which is close to the free-running frequency of the oscillator, the oscillation frequency of oscillator is changed to identical frequency of injection signal, i.e. the oscillator is locked by external signal, and the phenomenon is known as injection locking. Consider the oscillator provides differential output, as the external signal which is approximately twice the oscillator's free-running frequency inject into the common-mode point and make the oscillator locked, the frequency division is achieved. Among all kinds of frequency dividers, ILFD reaches the highest operation frequency among all frequency divider topology.

The phenomenon of injection locking can be explained by adding an external sinusoidal current I_{inj} to a conventional cross-coupled oscillator as shown in Fig. 2.6(a). Additional phase shift ϕ_0 caused by I_{inj} is inserted in the loop. The oscillator can no longer oscillate at ω_0 because the total phase shift at this frequency departs from 360° by ϕ_0. The oscillation frequency must change to injection frequency ω_{inj}. At frequency of ω_{inj}, the phase shift contributed by I_{inj}, I_{osc} (the oscillation current) and I_{tank} (current through LC tank) need to sustain a certain phase difference, meaning that the total phase shift maintain 360° From above description, the injection locking only occur at the frequency near ω_0 and the locking range is limited. As the matter of fact, the locking range was analytically derived as [37], [38]

$$\Delta\omega = \frac{\omega_0}{Q}\frac{I_{inj}}{I_{osc}}\frac{1}{\sqrt{1-\frac{I_{inj}^2}{I_{osc}^2}}} \tag{2.1}$$

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where Q is the quality factor of the LC tank. As a special case, if $I_{inj} \ll I_{osc}$, can be degenerated to

$$\Delta\omega = \frac{\omega_0}{Q}\frac{I_{inj}}{I_{osc}} \tag{2.2}$$

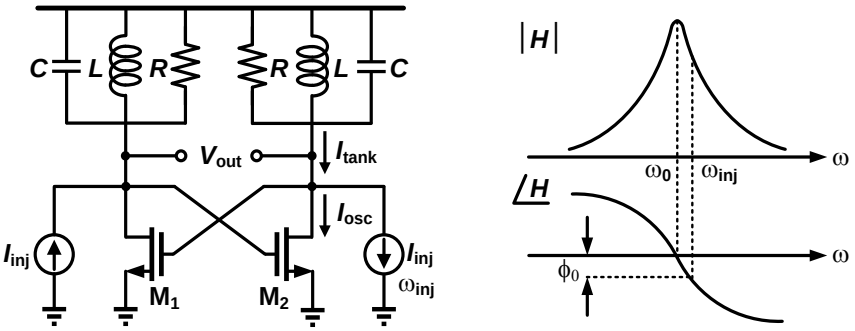
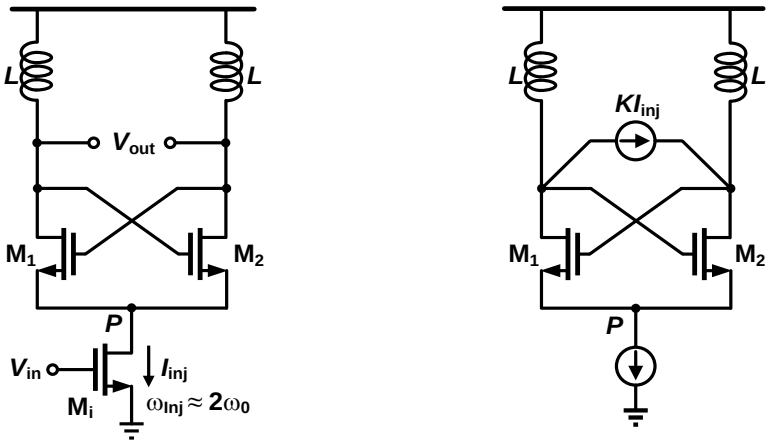


Fig. 2.6. Oscillator under injection locking.



(a) (b)

Fig. 2.7. (a) Conventional ILFD. (b) Equivalent circuit.

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The injection locking technique can be easily applied in frequency dividers. Fig. 2.7(a) shows conventional injection-locked frequency divider. The input signal injected through tail current transistor is twice the LC tank resonance frequency. The cross-coupled pair M_1 and M_2 form a mixer that down-converts ω_{inj} into ω_{inj} - ω_0 (up-converted component is suppressed by LC tank). A current of I_{inj} at ω_{inj} into node *P* is equivalent to a current of KI_{inj} at ω_{inj} - ω_0 into LC tank, as depicted in Fig. 2.7(b). If M_1 and M_2 can be switched on and off fully with enough voltage swing at V_{out}, then *K* is equal to $2/\pi$, and the locking range of ILFD can be written as

$$\Delta\omega = \frac{\omega_0}{Q}\frac{2}{\pi}\frac{I_{inj}}{I_{osc}}. \tag{2.3}$$

Referred to the input, the locking range is twice this value:

$$\Delta\omega = \frac{\omega_0}{Q}\frac{4}{\pi}\frac{I_{inj}}{I_{osc}} \tag{2.4}$$

A few techniques can be applied in ILFD to enhance the locking range of conventional ILFD in Fig. 2.7(a). To increase the injection current I_{inj}, the size of M_i is chosen large, causing large parasitic capacitance at node *P*. At high frequency, part of injection current pass though the capacitor to ground, and decrease the locking range. A modified ILFD with shunt peaking inductor *L*s to resonate the parasitic capacitor C_p is shown in Fig. 2.8(a) [39]. Although the locking range is improved, the extra inductor requires more area. The other modified ILFD in Fig. 2.8(b) is proposed to enhance the injection efficiency [40]. Because the injection current is directly injected to LC-tank, the injection efficiency is not degraded without extra inductor. Therefore, the ILFD with direct injection is widely utilized in high frequency CMOS PLL design.

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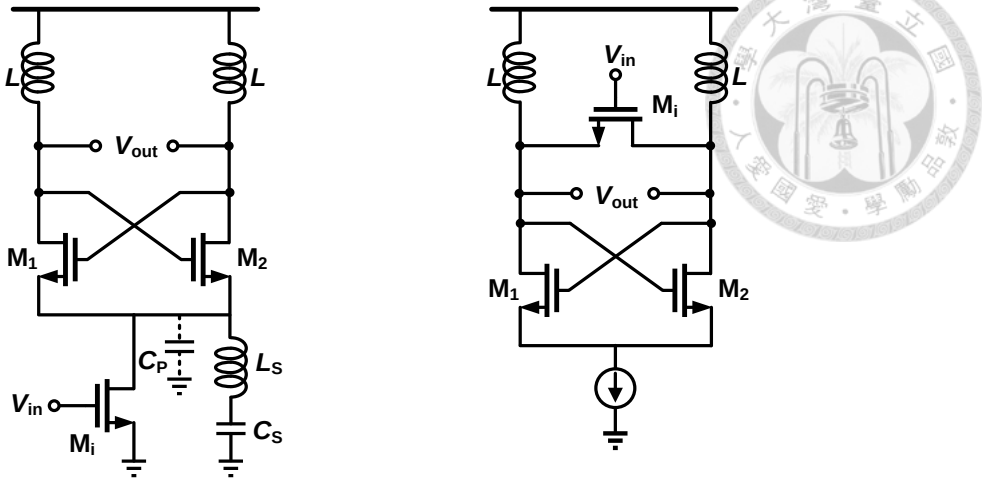

Fig. 2.8. Modified ILFD with (a) shunt peaking inductor (b) direct injection.

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2.2 35.7–64.2 GHz low power Miller Divider with Weak Inversion Mixer in 65 nm CMOS

2.2.1 Introduction of MMW Miller Divider

The millimeter wave (MMW) communication system has been developed rapidly due to the unlicensed band around 60 GHz. These systems require a phase lock loop (PLL) to provide local oscillator (LO) source for frequency conversion. The PLL needs a frequency divider to connect with voltage control oscillator (VCO) operated at high frequency, and the power consumption and locking range must be considered carefully. Due to the process variation, the bandwidth of divider is better to be several times wider than the tuning range of VCO. Therefore, a wide bandwidth with low power frequency divider is desired.

Static current mode logic (CML) frequency divider, injection lock frequency divider (ILFD) and Miller frequency divider are widely used in high speed PLL and synthesizer. The Miller divider has wider frequency response than ILFD with moderate power consumption. Therefore, the Miller divider is suitable for high frequency divider.

To implement Miller divider in CMOS process, the BPF is required. The block diagram of Miller divider with BPF is shown in Fig. 2.9(a). The mechanism is based on mixing the output and input signal and the result is filtered by BPF to get the divide-by-two signal. In the most cases, the Gilbert cell mixer shown in Fig. 2.9(b) is chosen in Miller divider design due to the simple implementation. However, the locking range is limited by the conversion gain (CG) of mixer, BPF response and parasitic effect of mixer. To solve these problems, transformer injection [8] and current bleeding [9] are

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proposed. These two techniques improve the CG of mixer and achieve wider locking range. Nevertheless, the improvements are limited, and it takes extra chip area and power consumption. Another effective way to enhance the bandwidth of Miller divider is using the band-switched Miller divider [41]. To select suitable band automatically, the additional calibration circuit is required. It can increase the operation frequency significantly. However, it also suffers from the large chip size and high dc power. In this section, a Miller divider with weak inversion biasing mixer is presented. By using the weak inversion mixer as mixer core of Miller divider, this divider achieves the locking range of 57 % from 35.7 to 64.2 GHz at 0-dBm injection power with low power consumption of 1.6 mW.

2.2.2 Circuit Design

Most of the Miller dividers include a mixer with good performance. Usually, these mixers have high CG, wide frequency response and low dc power. In previous reported work [8], [9], [35], Gilbert cell mixer is chosen as mixer core in Miller divider design. However, a conventional Gilbert cell mixer (Fig. 1(b)) consumes high dc power, and requires high voltage power supply for stack transistor topology. Passive mixer shown in Fig. 2.9(c), which can be operated without dc power; nevertheless, it still needs buffer amplifier for CG. To obtain sufficient CG with low dc power and low voltage supply, the weak inversion mixer is proposed and shown in Fig. 2.9(d) [42].This mixer has advantage over other mixer, and is suitable as mixer core of Miller divider.

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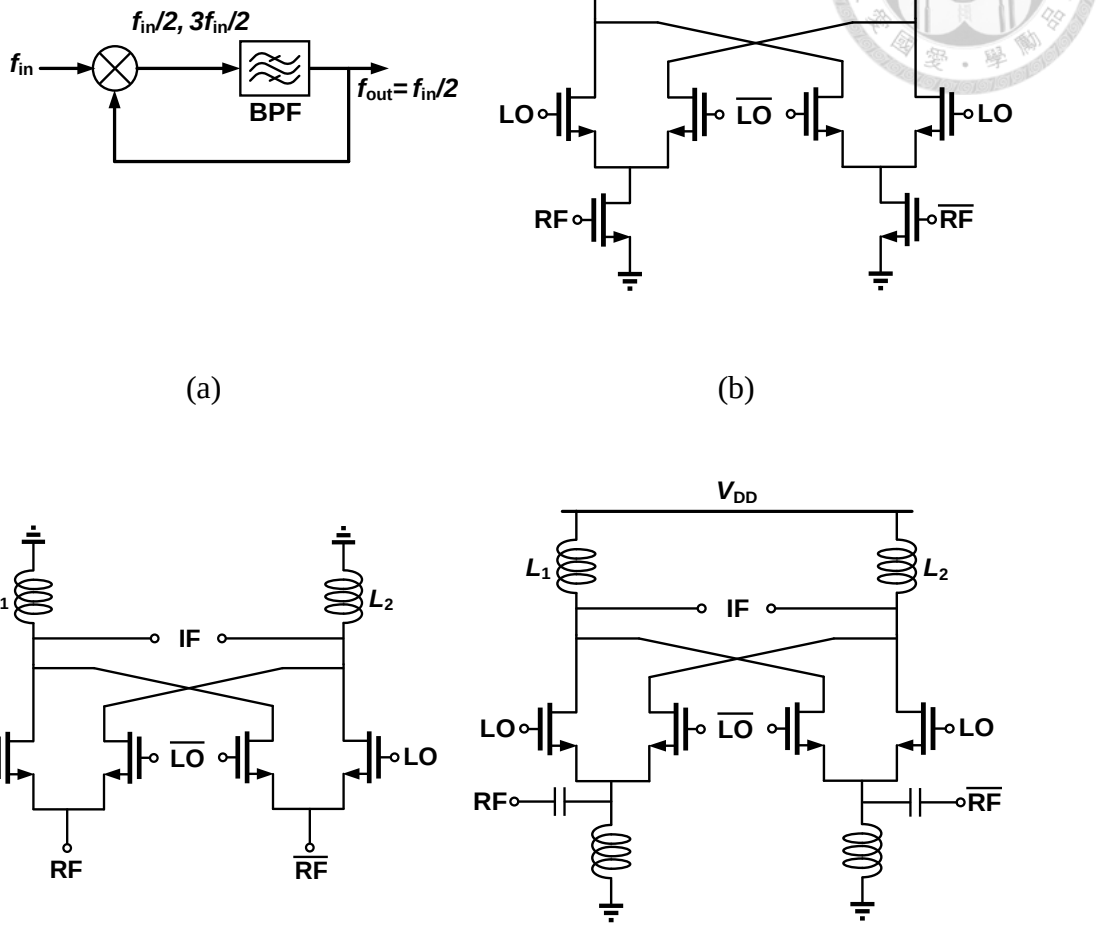

Fig. 2.9. (a) Block diagram of Miller divider, (b) conventional Gilbert cell mixer, (c) passive mixer, and (d) weak inversion biasing mixer

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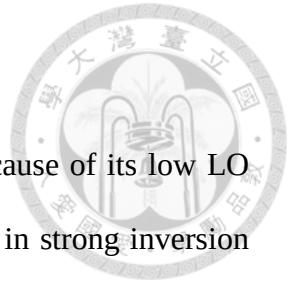

2.2.2.1 Weak Inversion Biasing mixer

The mixer with weak inversion bias technique is attractive because of its low LO power and low dc power. Traditional Gilbert cell mixer is operated in strong inversion region ($V_{GS} > V_{TH}$). In the weak inversion region, the gate-source V_{GS} is lower than threshold voltage V_{TH}, and the i_{DS} vs V_{GS} of MOS transistor is exponential dependence rather than square-law characteristics [42]. At this bias condition, the LO voltage swing requirement is relatively low.

Fig. 2.10(a) shows the simulated mixer conversion gain with different type mixers (Fig. 2.9(b), (c), (d)) at MMW frequency in 65 nm CMOS. Each mixer has the same device size (18 μm gate width) and inductor value with equal quality factor for a fair comparison. The only difference is bias condition. As can be observed, no matter with or without V_{GS} biasing, the conventional passive mixer has the lowest gain even in high LO voltage swing. A traditional Gilbert cell mixer in typical bias point has the highest gain in high LO voltage. Owing to operating in MMW, the gain provided by transconductance stage of Gilbert cell mixer is limited. By adopting the weak inversion bias in weak inversion mixer, this mixer improves conversion gain in low LO voltage region. The simulated mixer conversion gain versus input RF frequency is shown in Fig. 2.10(b). The weak inversion mixer exhibits better frequency response than others at low LO voltage. Moreover, this mixer consumes lower dc power than traditional Gilbert cell mixer.

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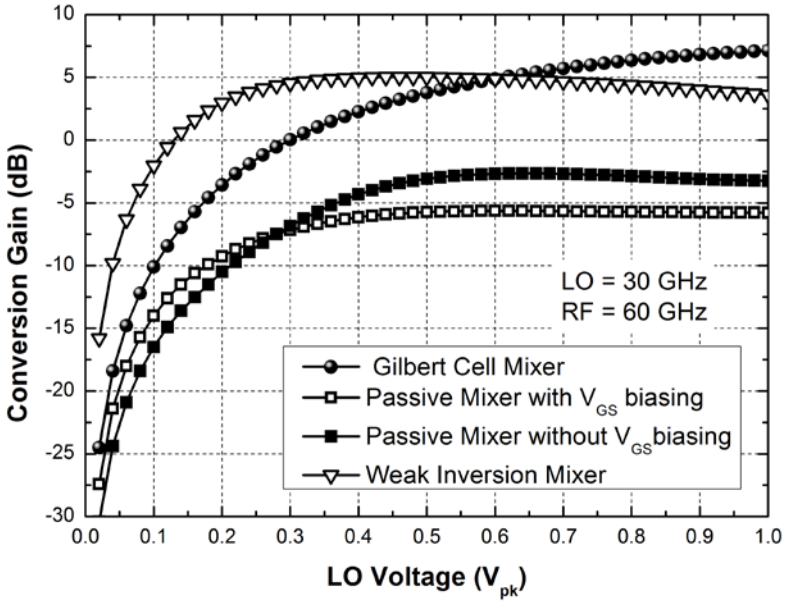
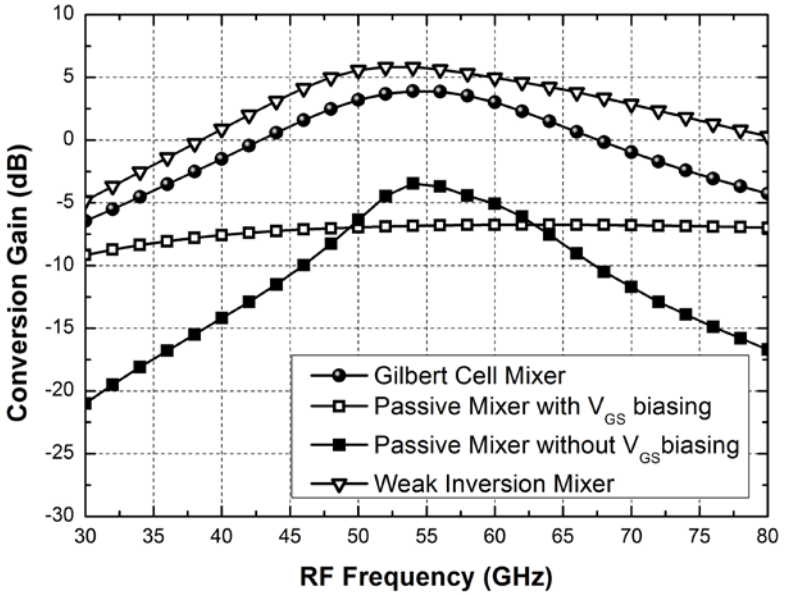


(a)



(b)

Fig. 2.10. Simulated (a) conversion gain versus LO voltage, and (b) conversion gain versus input frequency of each mixers

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2.2.2.2 Bandwidth of Miller Divider with BPF

The block diagram of Miller divider with BPF is shown in Fig. 2.11. Considering the mixer is ideal, and BPF is simple parallel RLC network. The impedance of RLC tank can be expressed as

$$Z_{\text{tank}} = \frac{\frac{j\omega_n\omega}{Q}R}{\omega_n^2 + \frac{j\omega_n\omega}{Q} - \omega^2} \tag{2.5}$$

where $\omega_n = 1/\sqrt{LC}$ and $Q = \omega RC$. As the switch pairs of mixer are fully switching, the conversion gain of mixer is equal to $(2/\pi)g_m$ multiplying by impedance of RLC tank, where g_m is the transconductance of transconductor stage of mixer. Also, the loop gain is equal to conversion gain of mixer, and to divide successfully, the loop gain at $\omega_{in}/2$ has to excess unity at $\omega_{in}/2$, the condition can be written as

$$\frac{2}{\pi}g_m\left|\frac{\frac{j\omega_n\omega_{in}}{2Q}R}{\omega_n^2 + \frac{j\omega_n\omega_{in}}{2Q} - \frac{\omega_{in}^2}{4}}\right| \geq 1 \tag{2.6}$$

$$\frac{2}{\pi}g_m R\frac{\frac{\omega_n\omega_{in}}{2Q}}{\sqrt{\left(\omega_n^2 - \frac{\omega_{in}^2}{4}\right)^2 + \frac{\omega_n^2\omega_{in}^2}{4Q^2}}} \geq 1 \tag{2.7}$$

Obviously, the peak loop gain is $(2/\pi)g_mR$ at $\omega_{in} = \omega_n/2$, and (2.7) can rewritten as

$$\frac{2}{\pi}g_m R \geq \sqrt{1 + \frac{\left(1 - \frac{\omega_{in}^2}{4\omega_n^2}\right)^2}{\frac{1}{4Q^2}\frac{\omega_{in}^2}{\omega_n^2}}} \tag{2.8}$$

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For $\Delta\omega = \left|\omega_{in} - 2\omega_n\right| \ll 2\omega_n$, we have

$$\begin{aligned} 1 - \frac{\omega_{in}^2}{4\omega_n^2} &= \frac{\left(2\omega_n + \omega_{in}\right)\left(2\omega_n - \omega_{in}\right)}{4\omega_n^2} \\ &\approx \frac{4\omega_n\left(2\omega_n - \omega_{in}\right)}{4\omega_n^2} \\ &\approx \frac{\Delta\omega}{\omega_n} \end{aligned} \tag{2.9}$$

Therefore, the denominator under the square root in (2.8) can be reduced to $(Q\Delta\omega/\omega_n)^2$, resulting in

$$\frac{2}{\pi} g_m R \geq \sqrt{1 + \left(\frac{Q\Delta\omega}{\omega_n}\right)^2} \tag{2.10}$$

Then,

$$\Delta\omega = \frac{\omega_n}{Q}\left[\left(\frac{2}{\pi} g_m R\right)^2 - 1\right] \approx \frac{\omega_n}{Q}\left(\frac{2}{\pi} g_m R\right)^2 \tag{2.11}$$

Let CG = $2g_mR/\pi$, (2.11) can be written as

$$\Delta\omega \approx \frac{\omega_n}{Q}\left(CG\right)^2 \tag{2.12}$$

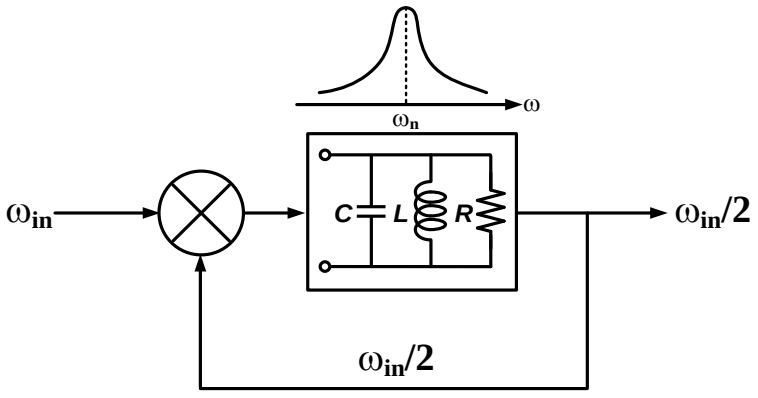

Fig. 2.11. Miller divider with BPF as RLC tank.

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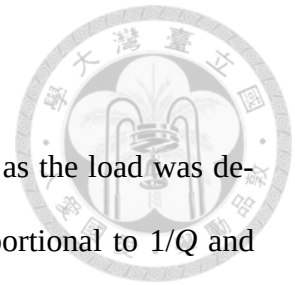

2.2.2.3 Proposed Miller Divider

The operation frequency range of Miller divider with LC tank as the load was derived as (2.12). From (2.12), the operation frequency range is proportional to $1/Q$ and CG. It can be observed that increasing the CG of mixer is effective to improve the locking range of Miller divider. Generally, CG is equal to $2g_mR/\pi$ and independent of LO voltage [35], and it is true when LO voltage is high enough. However, as long as LO voltage is not sufficient, CG is lower with lower LO voltage. As shown in Fig. 2.10(a), CG is dependent on LO voltage. From the principle of Miller divider, the mixer output port is fed back to LO port to mix with the divide-by-two signal. For low dc operation, the swing of output signals is small. As above mentioned, the weak inversion mixer has higher gain at low LO input. Also, based on Fig. 2.10(b), the weak inversion mixer has better frequency response. Therefore, the Miller divider with this mixer has a wider locking range than others. The proposed Miller divider is shown in Fig. 2.12. M_1-M_4 form the mixer core with weak inversion bias, and IF port is connected to LO port directly to form feedback loop. The gate and drain node share the same voltage source, since the performance does not improve by separating the bias. The size of transistor is selected appropriately to construct desired BPF center frequency with inductors L_1 and L_2. Instead of the RF choke, the Marchand balun is utilized to construct current coupling and differential signal between input and divider core; also, the required supply voltage will be decreased. Besides, the input matching network is not needed because the impedance looking into the source of MOS transistor is close to the output impedance of the Marchand balun. For measurement requirement, the common source amplifier used

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as test buffer to isolate the load of instruments, otherwise the BPF response will be influenced. To save the chip area, the load is realized by a resistor rather than an inductor.

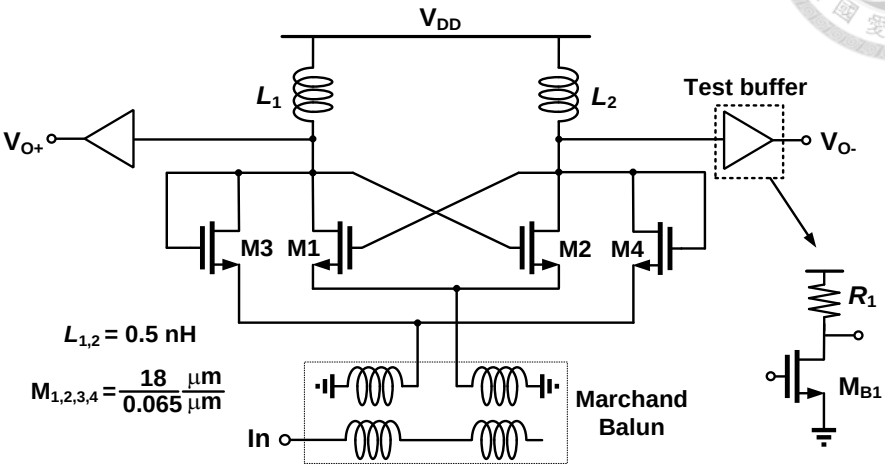

Fig. 2.12. Proposed Miller divider based on weak inversion mixer.

2.2.3 Measurement Results

The proposed Miller divider is implemented in 65-nm CMOS general process. The chip microphotograph is shown in Fig. 2.13 with a die size of 0.35 × 0.45 mm^2, including DC and RF pads. This divider is measured via on-wafer probing. The input is generated by a signal generator Agilent E8257D, and the output signal is captured by spectrum analyzer Agilent E4448A. This frequency divider operates at 0.4-V supply voltage and consumes 1.6 mW. The measured and simulated input sensitivity curve is shown in Fig. 2.14. It indicates that no self-oscillation is observed. The measured input locking range is from 35.7 to 64.2 GHz (57%) without frequency tuning. The measured sensitivity curve with supply voltage of 0.5 V is also shown in Fig. 2.14. The locking range is limited because the bias region is not in weak inversion region. The simulated and measured output powers are shown in Fig. 2.15. The tendency of the measured output

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power is similar to the simulation and it varies from -23 to -17 dBm. For phase noise measurement, as the input frequency is 50 GHz with input power of 0 dBm, the measured output phase noise is -106 dBc/Hz, which is better than input phase noise of -100 dBc/Hz at 100-kHz offset, and consistent with the theoretical value. Table 2.1 summarizes the performance of previously reported MMW Miller divider in CMOS process. Due to the weak inversion mixer, the proposed Miller divider has the widest locking range at 0-dBm input power among the previous reported Miller frequency dividers. The proposed Miller divider is also compared with other MMW ILFD, as summarized in Table 2.2. Compared with other published MMW ILFD, the proposed Miller divider has the lowest power consumption. This circuit also demonstrates the highest locking range and highest FOM [13] compared with others in MMW range.

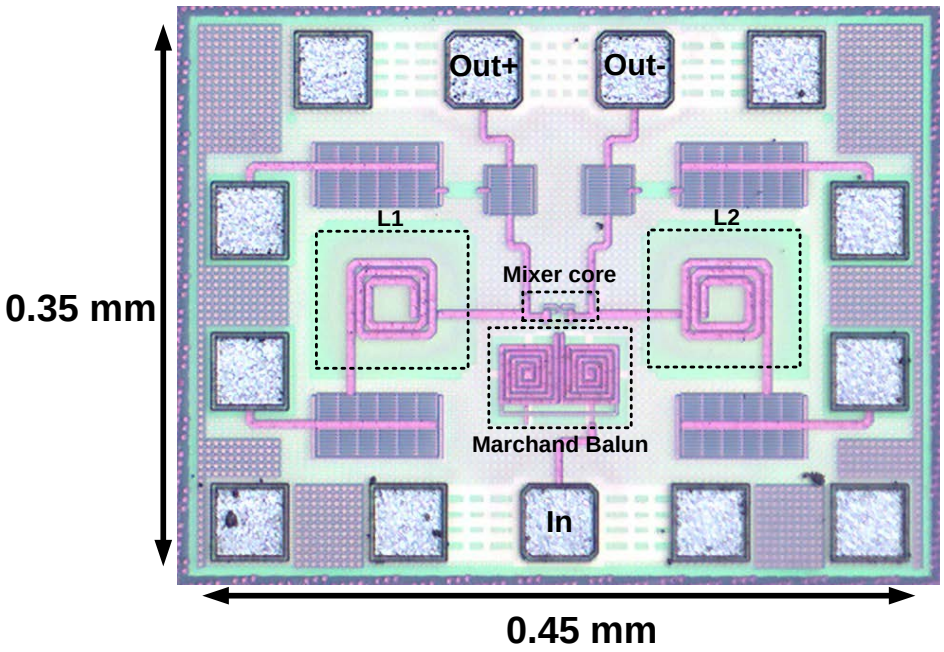

Fig. 2.13. Chip photo of proposed Miller divider.

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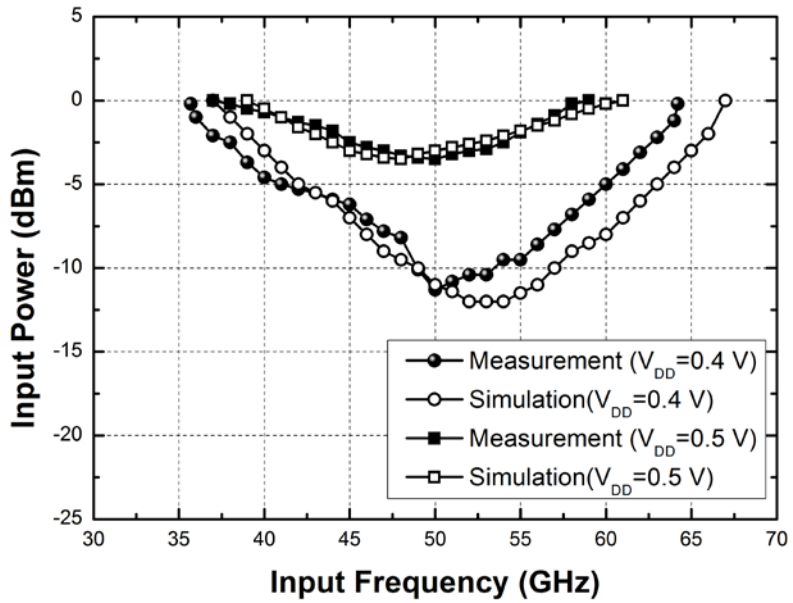

Fig. 2.14. Simulated and measured sensitivity curve of proposed Miller divider.

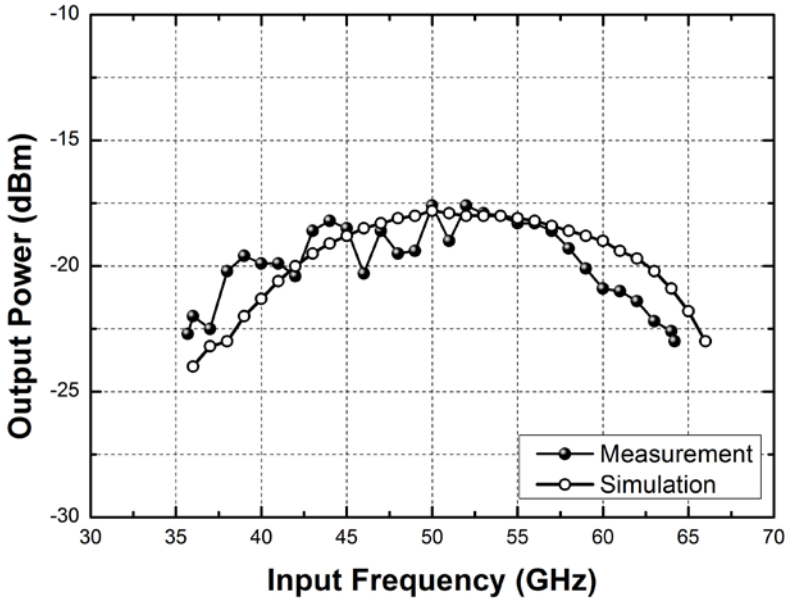

Fig. 2.15. Simulated and measured output power of proposed Miller divider at injection power of 0 dBm.

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Table 2.1. Comparison of Published MMW Miller dividers

		[35]	[8]	[9]	**This Work**
Technology		0.18μm CMOS	0.13 μm CMOS	0.13μm CMOS	65 nm CMOS
Topology		Miller	Miller	Miller	Miller
Input Frequency (GHz)		38-41	56.5-72.2	57-72	35.7-64.2
Locking Range	(GHz)	3	15.7	15	28.5
	(%)	7.6%	24.4%	23.2%	57%
Input Power (dBm)		3	0	0	0
V_{DD}(V)		2.5	1	0.8	0.4
P_{DC} (mW)		16.8	4.65	5	1.6
FOM (GHz/mW)		0.18	3.37	3	17.81
Chip Size (mm^2)		0.35	0.42	*0.007	0.156

* core area only

Table 2.2. Comparison of Published MMW ILFDs and proposed Miller divider

		[43]	[44]	[13]	[15]	**This Work**
Technology		0.18 μm CMOS	65nm CMOS	90nm CMOS	65nm CMOS	65 nm CMOS
Topology		ILFD	ILFD	ILFD	ILFD	Miller
Input Frequency (GHz)		37.5-49	53.7-72	51-74	53.4-79.4	35.7-64.2
Locking Range	(GHz)	11.5	23	18.3	26	28.5
	(%)	26.6%	36.8%	29%	39.2%	57%
Input Power (dBm)		0	0	0	0	0
V_{DD}(V)		1	0.8	0.5	0.8	0.4
P_{DC} (mW)		6	1.9	3	2.9	1.6
FOM (GHz/mW)		1.92	9.63	7.67	8.97	17.81
Chip Size (mm^2)		0.428	*0.023	0.136	*0.126	0.156

* core area only

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2.2.4 Discussions

There are several issues to be further discussed. The measured locking range is sensitive to supply voltage V_{DD} due to the bias condition. Although this circuit still can operate below 0.4-V supply voltage, the performance is degraded. As MOS is biased in weak inversion region, the relation for the transcondance of MOS (g_m) vs V_{GS} is exponential dependence like i_D vs V_{GS}. Hence, Miller divider with larger V_{DD} has wider locking range as biasing in weak inversion region. However, as V_{DD} larger than 0.45 V, the MOS is not biased in weak inversion region, which causes smaller CG. Therefore, bandwidth is limited and it has been demonstrated in measurement (Fig. 2.14).

Furthermore, due to no self-oscillation, this Miller divider cannot operate at low input power. In order to drive Miller divider with low input power, Miller divider need to be designed with self-oscillation which can be obtained by increasing the device size M_1 and M_2 since M_1, M_2 and the inductor (L_1 and L_2) form a cross-coupled oscillator. However, it will consume more dc power.

For output power measurement, since the power was measured from output buffer, the resistive-load buffer cannot provide enough power. However, in real application, the resistive-load buffer is not required. The voltage swing at Miller divider output is enough to drive next stage divider. Unfortunately, the voltage swing is not easy to measure in MMW region. Hence, the simulated output peak-to-peak voltage > 0.6 V is provided as shown in Fig. 2.16, and this is large enough to drive the next frequency divider chain.

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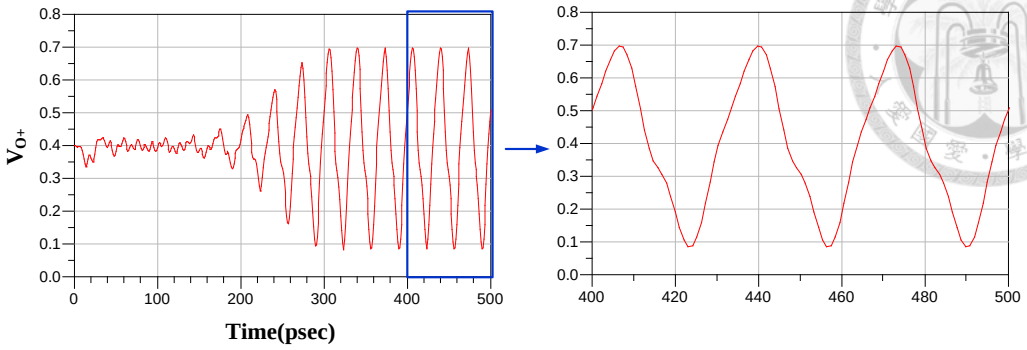

Fig. 2.16. Simulated transient response of V_{o+} with 0 dBm input power.

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2.3 W-band Injection-Locked Frequency Divider Using Split Transformer-Coupled Oscillator Technique

2.3.1 Introduction of MMW ILFD

With rapid progress in modern CMOS technology, the MMW applications have obtained lots of attention, such as 77 GHz automotive radars, 94 GHz image sensors, and point to point communications. These systems require a PLL to provide signal source or local oscillator (LO) source for frequency conversion. For the MMW PLLs, the main blocks are the VCO and frequency divider. The design challenges of MMW VCOs are the frequency tuning range, phase noise, and power consumption. For the frequency dividers, the first stage divider is a critical block since its operation frequency has to cover the frequency tuning range of VCOs. In addition, low power consumption is also an important issue for high frequency PLLs.

Static CML frequency dividers [6], [7], Miller frequency dividers [8], [9], [35] and ILFD [10]-[15], [39], [40],[43]-[47]are widely used in high speed PLLs. CML divider has the widest locking range and small size, but it suffers from high dc power consumption and lower operation frequency. Miller divider can operate at higher frequency with lower power consumption than CML divider, however, the locking range is still narrow. Among all the high frequency dividers, ILFD has the highest operation frequency and the lowest dc power consumption, but with the narrowest locking range. Nevertheless, ILFD still has potential for MMW low power PLLs.

The principle of ILFD has been described in section 2.1.3, the ILFD with direct injection have the wider locking range and much wider used in MMW PLL. Several

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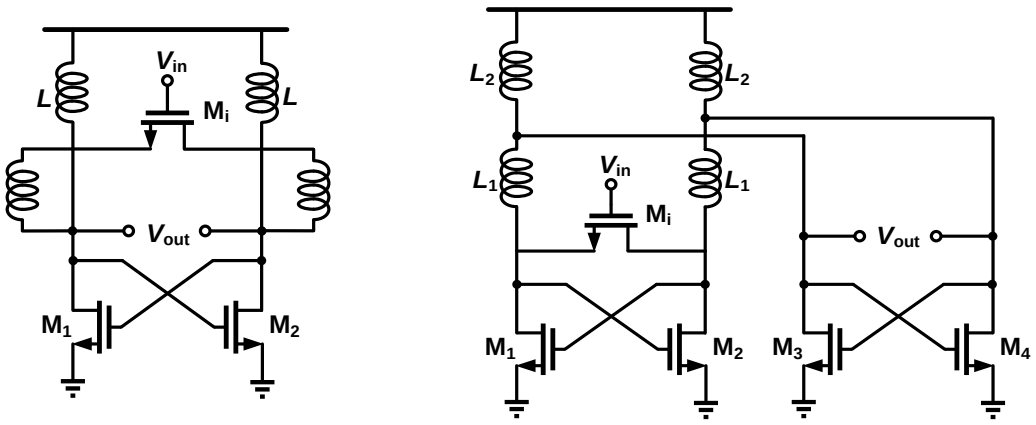
techniques have been proposed to improve the locking range of ILFD with direct injection. The inductor peaking is one of the useful techniques as shown in Fig. 2.17(a) [15], [43]. By inserting the inductors in injection transistor, the locking range can be enhanced by boosting its transconductance. Another method to improve locking range is using distributed LC structures illustrated in Fig. 2.17(b) [14], [45]. The parasitic capacitance is separated by distributed LC network to obtain higher operation frequency and wider locking range. However, these techniques require multiple inductors, and occupy larger chip areas as well as the design complexity of integration with the VCO.

In this section, a W-band divide-by-two ILFD with split transformer-coupled oscillator (STCO) is proposed to enhance the locking range of ILFD without additional inductors. Also, with splitting cross-coupled transistor and splitting transformer, the operation frequency is increased and oscillation condition can be easily satisfied without sacrificing dc power consumption.



(a) (b)

Fig. 2.17. ILFD with (a) inductor peaking technique and (b) distributed LC structure

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2.3.2 Split Transformer-Coupled Oscillator

Transformer-coupled oscillators have been proposed to achieve wide tuning range with low phase noise [48], [49]. The idea is utilizing multiple coupled oscillators which are controlled by switch to realize multi-band operation. In this design, the transformer couples two split cross-coupled pair transistors to increase the oscillation frequency and eases the oscillation condition.

2.3.2.1 Oscillation Frequency

A conventional LC oscillator and its equivalent model are shown in Fig. 2.18. The oscillation frequency is expressed as $\omega_0 = 1/\sqrt{LC}$, where L is the total inductance and C is the total parasitic capacitance contributed by MOS transistors and L.

The proposed STCO is shown in Fig. 2.19. The original inductor L is decomposed to two inductors L_1 and L_2, and a transformer with coupling coefficient k is constructed by the two inductors. The original cross-coupled pair transistor is split into two pairs of cross-coupled pair transistor. The equivalent model of STCO is also shown in Fig. 2. C_1 and C_2 are parasitic capacitance on two sides of transistor and inductor. The parasitic resistors of the transformer are R_1 and R_2. The input impedance of transformer can be derived as.

$$Z_{\text{in}}(s) = \frac{s^3(1-k^2)L_1L_2C_2 + s^2(L_1R_2 + L_2R_1)C_2 + s(L_1 + R_1R_2C_2) + R_1}{s^4(1-k^2)L_1L_2C_1C_2 + s^3(L_1R_2 + L_2R_1)C_1C_2 + s^2(L_1C_1 + L_2C_2 + R_1R_2C_1C_2) + s(R_1C_1 + R_2C_2) + 1} \quad (2.13)$$

By setting imaginary part of the denominator to zero, the oscillation frequency is calculated as

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$$\omega_{L,H} = \sqrt{\frac{L_1C_1 + L_2C_2 \pm \sqrt{(L_1C_1 + L_2C_2)^2 - 4(1-k^2)L_1L_2C_1C_2}}{2(1-k^2)L_1L_2C_1C_2}} \tag{2.14}$$

By splitting transformer-coupled oscillator, the total inductance and capacitance of split transformer-coupled oscillator are equal to the conventional cross-coupled oscillator ($L = L_1 + L_2$, $C = C_1 + C_2$). Because of the symmetric architecture, we assume $L_1 = L_2 = L/2$, and $C_1 = C_2 = C/2$, then the oscillation frequency can be rewritten as

$$\omega_L = \frac{2}{\sqrt{(1+k)LC}} = \frac{2}{\sqrt{(1+k)}}\omega_0 \tag{2.15a}$$

$$\omega_H = \frac{2}{\sqrt{(1-k)LC}} = \frac{2}{\sqrt{(1-k)}}\omega_0 \tag{2.15b}$$

Note that STCO has two oscillation frequencies. Usually, it only operates at low frequency because the currents in two inductors, L_1 and L_2, are in phase. For higher frequency, the currents are out of phase, causing larger inductor loss. The frequency increasing ratio is defined as ω_L/ω_0. For a special case of $k = 1$, the oscillation frequency, $\omega_L = \sqrt{2}\omega_0 \approx 1.414\omega_0$, i.e., the frequency at least increase 41.4%, and the increasing ratio is higher than distributed LC-oscillator [14]. From (2.8a), it also shows that the oscillation frequency can be increased by reducing k. However, once ω_L is increased by reducing k, ω_H is decreased. The lower k makes the two oscillation frequency close to each other. The higher oscillation frequency mode cannot be eliminated easily and thus, the two tone oscillations may occur in STCO simultaneously. Hence, the ILFD may not divide to correct frequency by this phenomenon. Also, the oscillation condition can be influenced by k, which will be discussed in the next paragraph.

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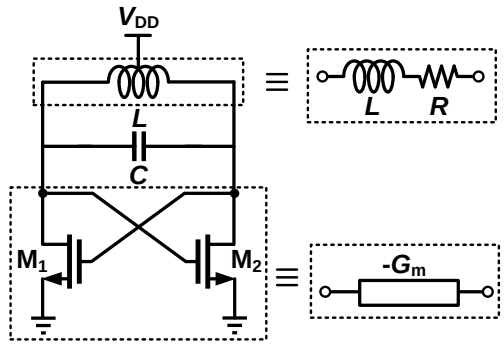

Fig. 2.18. Conventional cross-coupled oscillator.

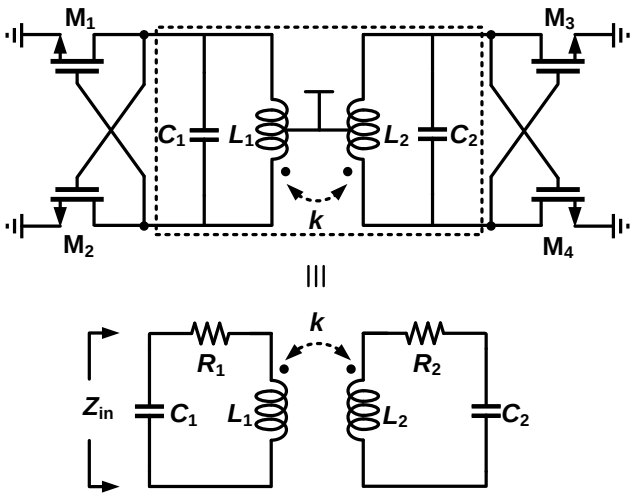

Fig. 2.19. Proposed split transformer coupled oscillator (STCO).

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2.3.2.2 Oscillation Condition

To satisfy the oscillation condition of oscillator, the cross-coupled pair transistors must provide enough negative conductance, $-G_m$, to compensate the loss of LC-tank. Assuming the series resistance of inductor dominates the total loss of LC-tank, the equivalent parallel resistance of LC-tank is equal to $R_p \approx Q\sqrt{L/C}$, where $Q = \omega L/R$ is the quality factor of inductor. As a result, the oscillation condition of conventional LC oscillator can be expressed as

$$G_m Q\sqrt{\frac{L}{C}} > 1 \tag{2.16}$$

Considering a conventional LC oscillator operated at 40 GHz as an example, L is 0.3 nH with Q = 15, and the total parasitic capacitor C is 50 fF. By (2.16), the minimum required G_m is equal to 0.86 mS. The oscillation condition of STCO can be derived by using the equivalent circuit model in Fig. 2.20. The equivalent parallel resistance of transformer $R_{p,T}$ in two frequency modes can be calculated from (2.13) as

$$R_{p,T}(\omega_L) = \mathrm{Re}[Z_{in}(\omega_L)] \approx \frac{Q(1+k)}{2}\sqrt{\frac{(1+k)L}{C}} \tag{2.17a}$$

$$R_{p,T}(\omega_H) = \mathrm{Re}[Z_{in}(\omega_H)] \approx \frac{Q(1-k)}{2}\sqrt{\frac{(1-k)L}{C}} \tag{2.17b}$$

The negative transconductance $-G_{m2}$ which is transformed by transformer can be represented as $\mathrm{Re}[Y_{in}]$, and is derived as

$$\mathrm{Re}[Y_{in}(\omega)] = \frac{-k^2 G_{m2}}{\frac{\omega^4 L^2 C^2 (k^2-1)^2}{16} + \frac{\omega^2 LC(k^2-1)}{2} + \frac{\omega^2 L^2 G_{m2}^2 (k^2-1)^2}{4}} \tag{2.18}$$

Then, the total equivalent transconductance, $G_{m,eq}$, is given as

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$$G_{\mathrm{m,eq}}(\omega) = G_{\mathrm{m1}} + \left|\mathrm{Re}[Y_{\mathrm{in}}(\omega)]\right| \tag{2.19}$$

Setting $G_{\mathrm{m1}} = G_{\mathrm{m2}} = G_{\mathrm{m}}/2$ due to the symmetry of splitting cross-coupled pair transistor, the $G_{\mathrm{m,eq}}$ in low and high oscillation frequency can be expressed as

$$G_{\mathrm{m,eq}}(\omega_{\mathrm{L}}) = \frac{G_{\mathrm{m}}}{2} + \frac{1}{2}\frac{k^2 G_{\mathrm{m}}}{k^2 + (k+1)(k-1)^2 \dfrac{L}{C} G_{\mathrm{m}}^2} \tag{2.20a}$$

and

$$G_{\mathrm{m,eq}}(\omega_{\mathrm{H}}) = \frac{G_{\mathrm{m}}}{2} + \frac{1}{2}\frac{k^2 G_{\mathrm{m}}}{k^2 + (k+1)^2(k-1) \dfrac{L}{C} G_{\mathrm{m}}^2}. \tag{2.20b}$$

Accordingly, to ensure the oscillation occurs at the lower frequency, the following condition need to be satisfied.

$$G_{\mathrm{m,eq}}(\omega_{\mathrm{L}}) R_{\mathrm{p,T}}(\omega_{\mathrm{L}}) > 1 \tag{2.21a}$$

$$G_{\mathrm{m,eq}}(\omega_{\mathrm{H}}) R_{\mathrm{p,T}}(\omega_{\mathrm{H}}) < 1. \tag{2.21b}$$

Otherwise, concurrent dual mode oscillation may occur. As mentioned before, choosing higher k can avoid this phenomenon easily because the higher k leads to higher loss of transformer in high frequency from (2.17b). In addition, this condition also can be achieved by choosing appropriate G_{m} value. Considering STCO only operated in the lower frequency mode, the minimum required G_{m} of STCO can be found in (2.21a). Fig. 2.21(a) shows the minimum required G_{m} and frequency increasing ratio versus different k. STCO has higher oscillation frequency for all k value, and requires less G_{m} as k is higher than 0.6. To make a fair comparison, the frequency increasing ratio is normalized to unity by changing the inductor value of STCO with the same total transistor size as conventional LC oscillator (constant total G_{m} and capacitance). The minimum required

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G_m versus different k under the same oscillation frequency is shown in Fig. 2.21(b). It can be observed that the minimum required G_m for proposed STCO is lower than conventional LC-oscillator when k is larger than 0.2, and the higher k will further relieve the oscillation condition.

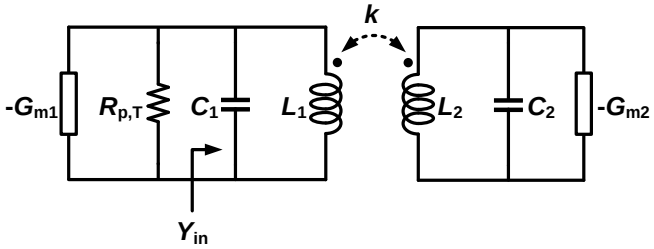

Fig. 2.20. Equivalent circuit of STCO

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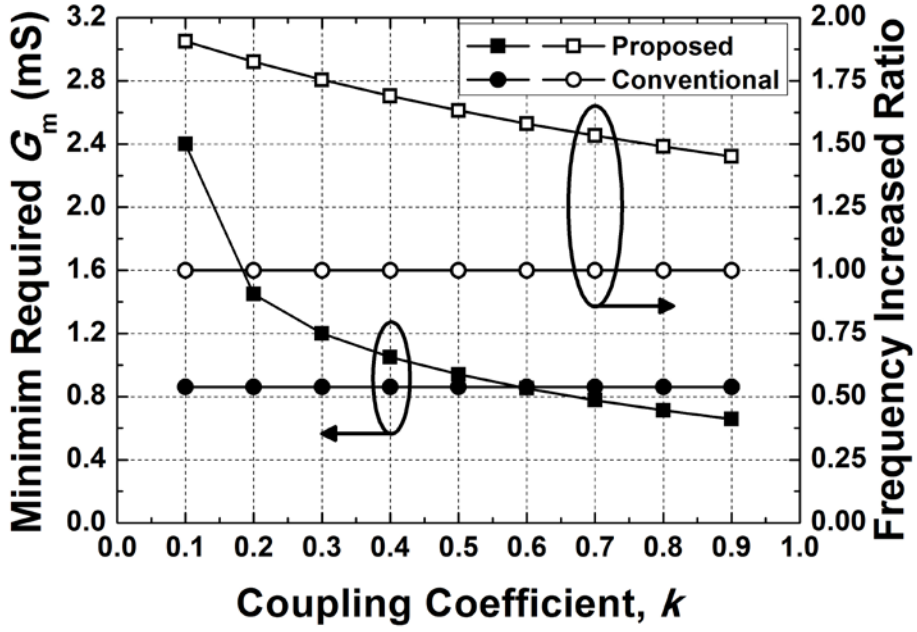
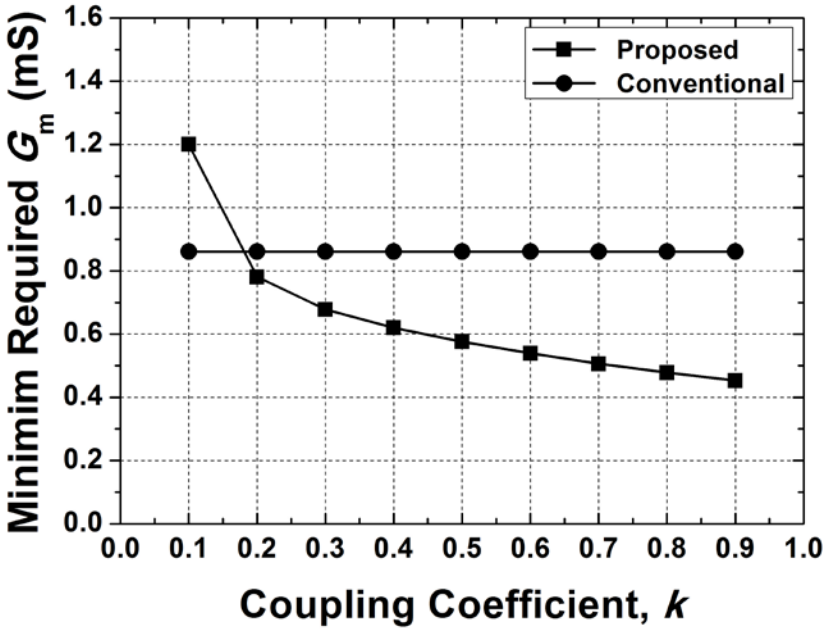


(a)



(b)

Fig. 2.21. Calculated (a) Minimum required G_m and frequency increasing ratio versus transformer coupling coefficient, *k*, and (b) minimum required Gm versus transformer coupling coefficient under the same oscillation frequency.

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2.3.3 Analysis of ILFD

2.3.3.1 Locking Range Analysis

The schematic and equivalent circuit model of divide-by-two ILFD with direct injection are shown in Fig. 2.22(a) and (b). This ILFD is realized by conventional-LC oscillator, and the injection transistor, M_i is connected to LC-tank directly. Before injecting signal, the output frequency of the ILFD is free-running oscillation frequency ω_0. When input frequency $\omega \approx 2\omega_0$ is injected into the injection transistor, the output frequency is locked to half of input frequency ω. The injection transistor can be modeled as an injection current source, $i_{inj}(t)$, controlled by input and output voltage, and a parasitic resistor, R_{inj}. The input voltage $v_{in}(t)$ is $V_i\cos(2\omega t+\phi)$, and the differential output voltage $v_{o+}(t)$ and $v_{o-}(t)$ are $\pm(V_o/2)\cos\omega t$, where V_i and V_o are the magnitudes of input and output voltage, respectively, and ϕ is the phase shift between input and output voltage. $i_{inj}(t)$ is derived by multiplying input and output voltage as

$$i_{inj}(t) = \alpha_{inj} V_i \cdot V_o \cos(2\omega t + \phi)\cos\omega t \tag{2.22}$$

where α_{inj} is the mixing factor which depends on device size and bias voltage. Assuming that the frequency components far from resonant frequency ω_0 are filtered by LC-tank, (2.22) can be simplified as

$$i_{inj}(t) = \alpha_{inj} V_i \cdot V_o (\cos\phi\cos\omega t - \sin\phi\sin\omega t) \tag{2.23}$$

Using complex exponential to replace sines and cosines, so the injection current can be expressed by phasor form as

$$I_{inj} = I_{inj,i} + I_{inj,q} = \alpha_{inj} V_i \cdot V_o (\cos\phi - j\cdot\sin\phi) \tag{2.24}$$

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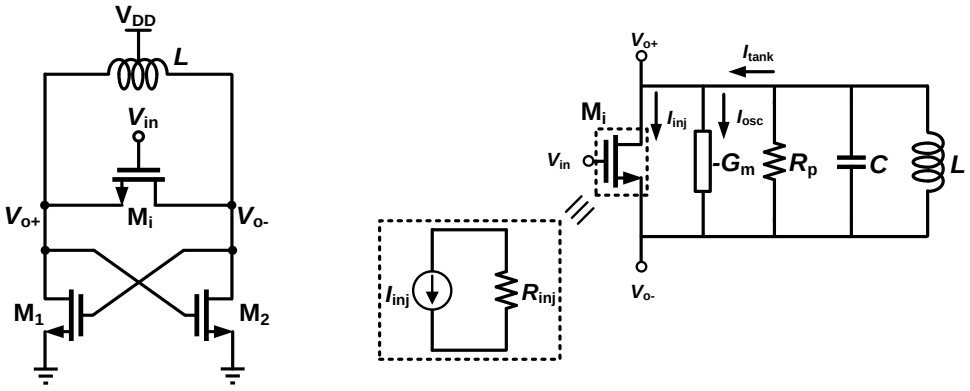
where $I_{inj,i}$ and $I_{inj,q}$ are in-phase and quadrature-phase current, respectively. The locking range of ILFD is determined by phase [37] and gain condition [15], [14]. The phase condition means that the phase of total input current should be equal to the phase of current through LC-tank when ILFD is locked and stable oscillation is maintained.



(a) (b)

Fig. 2.22. (a) ILFD with direct injection and (b) its equivalent circuit model.

As the input frequency is $2\omega_0$, the total quadrature phase current in LC-tank is zero. Then $I_{inj,q}$ is equal to zero and ϕ is equal to 0 or π. In other words, the total quadrature phase currents are equal to zero when ILFD is locked by the input signal. When the input frequency is not equal to $2\omega_0$, an extra $I_{inj,q}$ is induced to make the summation of the quadrature phase current to zero. The maximum magnitude of $I_{inj,q}$ is obtained as ϕ is equal to $\pi/2$ or $3\pi/2$, and the lowest and the highest input frequency can be achieved. ϕ is equal to $3\pi/2$ at the highest input frequency, if the highest frequency is equal to $\omega_0+\Delta\omega$. The total current I_{tank} through LC-tank is equal to the summation of injection current I_{inj} and oscillation current I_{osc} ($I_{osc} + I_{inj} = I_{tank}$), and satisfies the following equation,

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$$G_{\mathrm{m}}V_{\mathrm{o}} + j\alpha_{\mathrm{inj}}V_{\mathrm{i}} \cdot V_{\mathrm{o}} = V_{\mathrm{o}}\left(\frac{1}{R_{\mathrm{eff}}} + \frac{1}{j(\omega_0 + \Delta\omega)L} + j(\omega_0 + \Delta\omega)C\right) \tag{2.25}$$

where R_{eff} is the effective parallel resistance and given as

$$R_{\mathrm{eff}} = R_{\mathrm{p}} // R_{\mathrm{inj}}. \tag{2.26}$$

By the equality of phase of total current, the phase term in (2.26) can be calculated as

$$\frac{\alpha_{\mathrm{inj}}V_{\mathrm{i}}}{G_{\mathrm{m}}} = \frac{R_{\mathrm{eff}}}{\omega_0 L}\left[\left(1+\frac{\Delta\omega}{\omega_0}\right) - \left(1+\frac{\Delta\omega}{\omega_0}\right)^{-1}\right] \tag{2.27}$$

Provided that $\Delta\omega << \omega_0$, substituting the following approximation into (2.27)

$$\left(1+\frac{\Delta\omega}{\omega_0}\right)^{n} \approx 1 + n\frac{\Delta\omega}{\omega_0} \tag{2.28}$$

then

$$\Delta\omega \approx \frac{\alpha_{\mathrm{inj}}V_{\mathrm{i}}\omega_0^2 L}{2G_{\mathrm{m}}R_{\mathrm{eff}}} = \frac{\alpha_{\mathrm{inj}}V_{\mathrm{i}}}{2G_{\mathrm{m}}R_{\mathrm{eff}}C}. \tag{2.29}$$

At the lowest frequency ω_0-$\Delta\omega$, ϕ is equal to $\pi/2$. Similar to the above derivation, the same $\Delta\omega$ can be obtained. Therefore, the locking range by phase condition is derived as

$$LR_{\mathrm{phase}} = 4\Delta\omega \approx \frac{2\alpha_{\mathrm{inj}}V_i}{G_{\mathrm{m}}R_{\mathrm{eff}}C} \tag{2.30}$$

The locking range (2.30) is valid if ILFD satisfies oscillation condition without injection signal ($G_{\mathrm{m}}R_{\mathrm{eff}} > 1$) and the maximum locking range can be achieved when $G_{\mathrm{m}}R_{\mathrm{eff}} = 1$. If $G_{\mathrm{m}}R_{\mathrm{eff}}$ is smaller than 1, the locking range can be obtained by gain condition. Since the effective parallel resistance is degraded by R_{inj}, ILFD may not oscillate without injection signal. In fact, even the condition, $G_{\mathrm{m}}R_{\mathrm{eff}} > 1$ is not satisfied, ILFD still can operate normally by external injection signal. From (2.24), after ILFD receives the injection current, the equivalent transconductance is increased by in-phase injection current. The

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additional equivalent transconductance is $\alpha_{\text{inj}}V_{\text{i}}\cos\phi$ and the oscillation condition now becomes

$$(G_{\text{m}} + \alpha_{\text{inj}}V_{\text{i}}\cos\phi)R_{\text{eff}} > 1. \tag{2.31}$$

If ILFD requires an injection signal to satisfy oscillation condition (2.31) with the phase shift ϕ_0 from π to $3\pi/2$, the highest frequency $\omega_0+\Delta\omega$ is reduced, and then the total current equation can be expressed as

$$G_{\text{m}}V_{\text{o}} + \alpha_{\text{inj}}V_{\text{i}}\cdot V_{\text{o}}\cos\phi_0 + j\alpha_{\text{inj}}V_{\text{i}}\cdot V_{\text{o}}\sin\phi_0 = V_{\text{o}}\left(\frac{1}{R_{\text{eff}}} + \frac{1}{j(\omega_0+\Delta\omega)L} + j(\omega_0+\Delta\omega)C\right) \tag{2.32}$$

where

$$\phi_0 = \cos^{-1}\left(\frac{R_{\text{eff}}^{-1} - G_{\text{m}}}{\alpha_{\text{inj}}V_{\text{i}}}\right). \tag{2.33}$$

By equating the phase of total current, the phase term in (2.25) can be calculated as

$$\frac{\alpha_{\text{inj}}V_{\text{i}}\sin\phi_0}{G_{\text{m}} + \alpha_{\text{inj}}V_{\text{i}}\cos\phi_0} = \frac{R_{\text{eff}}}{\omega_0 L}\left[\left(1+\frac{\Delta\omega}{\omega_0}\right) - \left(1+\frac{\Delta\omega}{\omega_0}\right)^{-1}\right] \tag{2.34}$$

Meanwhile, the lowest frequency ω_0-$\Delta\omega$ is reduced for satisfying oscillation condition with ϕ_0 from 0 to $\pi/2$. With a similar derivation and approximation (2.28) as above, the locking range derived by gain condition can be expressed as

$$LR_{\text{gain}} = 4\Delta\omega \approx \frac{2\alpha_{\text{inj}}V_{\text{i}}\sin\phi_0}{C} = \frac{2\alpha_{\text{inj}}V_i}{C}\sqrt{1-\left(\frac{1-G_{\text{m}}R_{\text{eff}}}{\alpha_{\text{inj}}V_{\text{i}}R_{\text{eff}}}\right)^2} \tag{2.35}$$

If ILFD is at the boundary of oscillation condition ($G_{\text{m}}R_{\text{eff}}$ = 1), the locking ranges derived by gain condition and phase condition are the same. Equation (2.30) and (2.35) also indicate as $G_{\text{m}}R_{\text{eff}}$ is equal to unity, the maximum locking range can be defined as

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$$LR_{\max} \approx \frac{2\alpha_{\text{inj}} V_{\text{i}}}{C}. \tag{2.36}$$

To further increase the locking range, the total capacitance C has to be small. Besides, α_{inj} should be designed as large as possible by increasing the size of injection transistor. However, the larger device causes the smaller R_{eff}, and the locking range is decreased since the locking range is determined by gain condition (2.35). Therefore, maximum locking range (2.36) can be acquired by selecting an appropriate size of M_i.

The proposed ILFD realized by STCO and its equivalent model are shown in Fig. 2.23(a) and (b). The injection transistor M_i is connected to the first coil of transformer directly. The transconductance G_{m2} is transformed into Re[Y_{in}]. The summation of Re[Y_{in}] and G_{m1} is equal to the total equivalent transconductance $G_{m,eq}$ which was derived in previous section. Benefited from the splitting transformer, the parasitic capacitance is reduced. The split transformer and its equivalent circuit model are shown in Fig. 2.24. Because of the symmetric architecture, ($L_1 = L_2 = L/2$, and $C_1 = C_2 = C/2$) the input admittance Y_{in} can be derived as

$$Y_{\text{in}} = \frac{\left(-1+\frac{LC\omega^2}{4}\right)}{\frac{\omega L}{2}\left(1-\frac{(1-k^2)LC\omega^2}{4}\right)} = \frac{\frac{k^2 C\omega}{2}}{\left(1-\frac{(1-k^2)LC\omega^2}{4}\right)} - \frac{2}{\omega L}. \tag{2.37}$$

From the input admittance of transformer (2.37), the transformer can be modeled as parallel inductor and capacitor. L' can be obtained as $L/2$, and when ω is close to ω_L, C_2' can be approximated as

$$C_2' \approx \frac{\frac{k^2 C}{2}}{1-\frac{\omega^2 LC\left(1-k^2\right)}{4}} = \frac{kC}{2}. \tag{2.38}$$

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The effective parallel resistor of proposed ILFD is given as

$$R_{\text{eff,T}} = R_{\text{p,T}} // R_{\text{inj}} . \tag{2.39}$$

Hence, the locking range of proposal ILFD derived by gain condition can be expressed as

$$LR_{\text{gain}} = \frac{2\alpha_{\text{inj}} V_i}{C_1 + C_2'} \sqrt{1 - \left(\frac{1 - G_{\text{m,eq}} R_{\text{eff,T}}}{\alpha_{\text{inj}} V_{\text{i}} R_{\text{eff,T}}} \right)^2} = \frac{4\alpha_{\text{inj}} V_i}{(1+k)C} \sqrt{1 - \left(\frac{1 - G_{\text{m,eq}} R_{\text{eff,T}}}{\alpha_{\text{inj}} V_{\text{i}} R_{\text{eff,T}}} \right)^2} \tag{2.40}$$

and the maximum locking range is given as

$$LR_{\text{max}} \approx \frac{4\alpha_{\text{inj}} V_{\text{i}}}{(1+k)C} . \tag{2.41}$$

Compared with the locking range of conventional ILFD (2.36), the locking range is improved since the total equivalent capacitance is smaller. Also, the locking range can be extended further by reducing the coupling coefficient, *k*. Nevertheless, the lower *k* results in no oscillation from discussion in section 2.3.2, and the locking range is degraded by gain condition. In consequence, the suitable *k* should be selected for optimum locking range. Fig. 2.25 shows the simulated locking range versus different *k*, and the widest locking range is achieved at $k = 0.6$. In higher *k* region, the locking range is also decreased since the total equivalent capacitance is larger.

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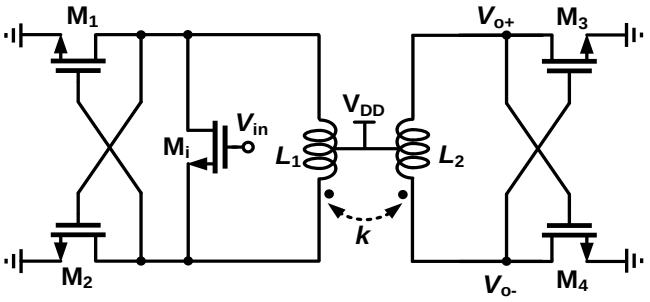
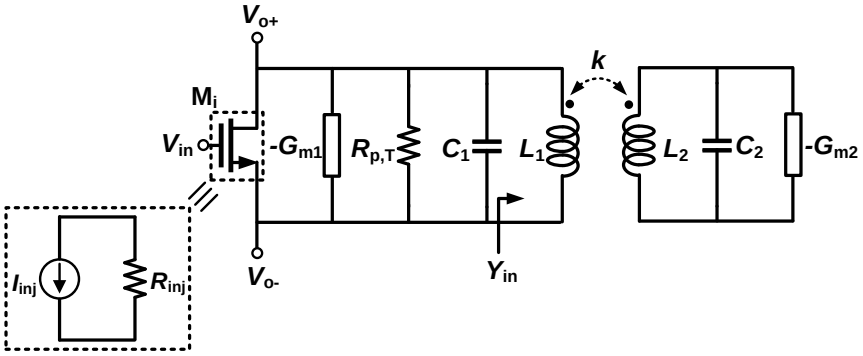


(a)



(b)

Fig. 2.23. The proposed ILFD realized by STCO and (b) its equivalent circuit model.

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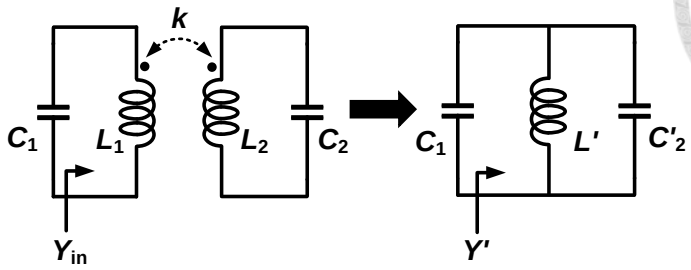

Fig. 2.24. Split transformer and its equivalent circuit model.

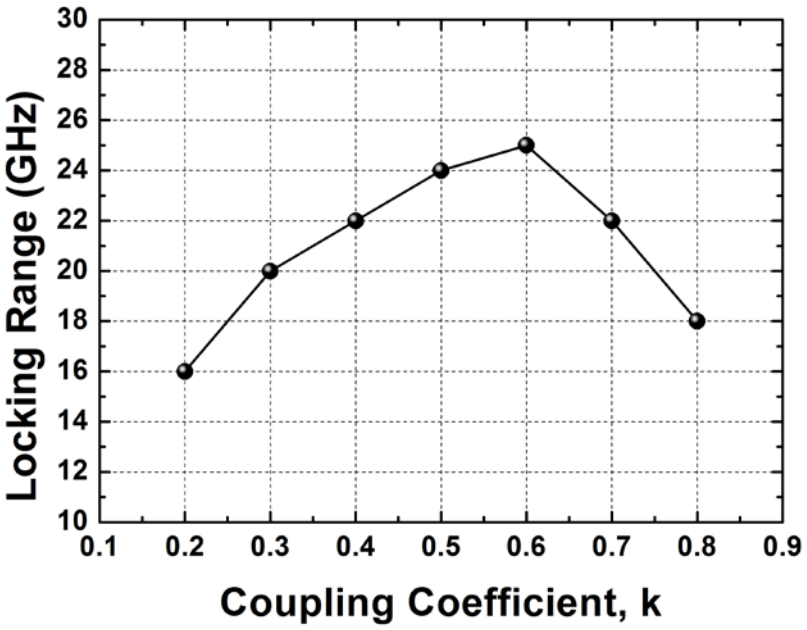

Fig. 2.25. Simulated locking range versus different coupling coefficient, *k*.

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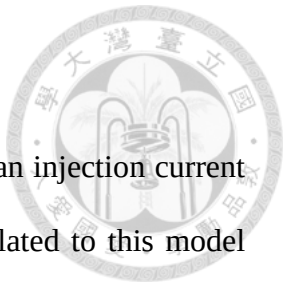

2.3.3.2 Injection Transistor

Fig. 2.22 shows that the injection transistor can be modeled as an injection current source and a parasitic resistor, and the locking range of ILFD is related to this model from the above derivation. According to previous discussion, the wider locking range can be achieved by higher α_{inj}. Since the nonlinear behavior of injection transistor is too complicated to express by equations, the parameters of injection transistor model are obtained through simulation. The simulated mixing factor, α_{inj} and parasitic resistor, R_{inj} of the transistor versus V_{GS} in 90-nm CMOS among different device size is shown in Fig. 2.26(a) and (b), respectively. From above analysis, the V_{GS} should be chosen for maximum value, and α_{inj} also can be improved with the large device size. In addition, the R_{inj} is inversely proportional to V_{GS} and device size from Fig. 2.26(b), and the locking range is degraded by smaller R_{inj} because of gain condition. Therefore, there is a design tradeoff between the size of injection transistor and the locking range. Furthermore, the injection transistor has additional capacitance which is proportional to the size of injection transistor. This has not been mentioned in previous analysis for simplicity. As the matter of fact, the capacitor value is quite smaller than other parasitic capacitance, so the locking range is not influenced significantly.

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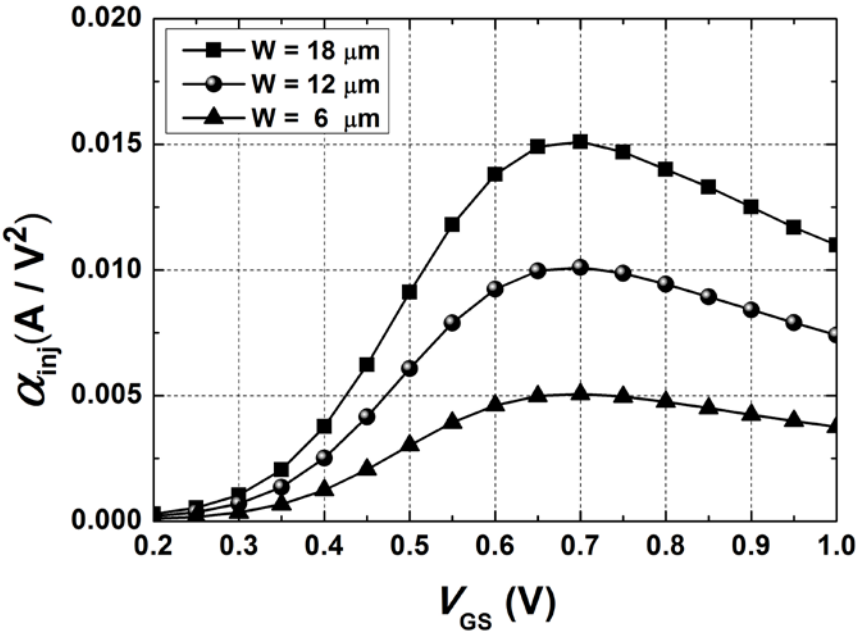
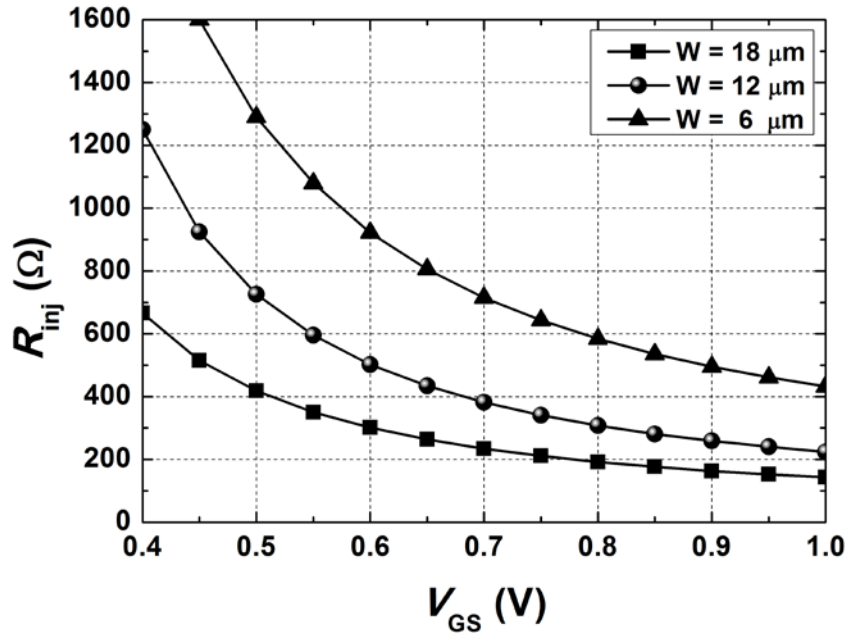


(a)



(b)

Fig. 2.26. Simulated (a) α_{inj} and (b) R_{inj} of injection transistor versus V_{GS}.

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2.3.4 Circuit Design

The proposed ILFD was designed using CMOS 90 nm technology, and the f_T and f_{max} are 100 and 160 GHz, respectively. This process provides one poly layer and nine metal layers for interconnection and the top layer metal is thickened to 3.4 μm to minimize the metal loss. Metal–insulator–metal (MIM) capacitors, spiral inductors and poly resistors are also available in this process. The complete circuit schematic of the proposed ILFD is shown in Fig. 2.27, and the design parameters are tabulated in Table I. This ILFD is realized based on STCO with direct injection, and can achieve wide locking range without varactor tuning.

The device sizes of cross-coupled pair transistor are chosen carefully for reaching the edge of oscillation condition. Due to the extra parallel resistance contributed by injection transistor, the size of cross-coupled pair should be overestimated. Two cross-coupled pair transistors are coupled by the transformer. The top view of the transformer is shown in Fig. 2.28. As discussed in previous section, the operation frequency and locking range of ILFD can be optimized by varying the coupling coefficient. The two inductors are connected to individual cross-coupled pair transistors. To reduce the metal loss, the two coils of transformer are implemented by top layer metal with edge coupling. The metal width of two inductors is 4 μm, and the simulated inductor values are 0.27 and 0.33 nH at 40 GHz with quality factor of 18, respectively. The metal spacing of transformer is minimum value of 2 μm for satisfying the design rule with optimum coupling coefficient of 0.6. The appropriate selection of device size and coupling coefficient ensure that the STCO only oscillates at low frequency mode since the nega-

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tive transconductance is eliminated at high frequency mode. The size of transformer is only 74 × 70 μm^2, which is more compact than the design in [45] and [14].

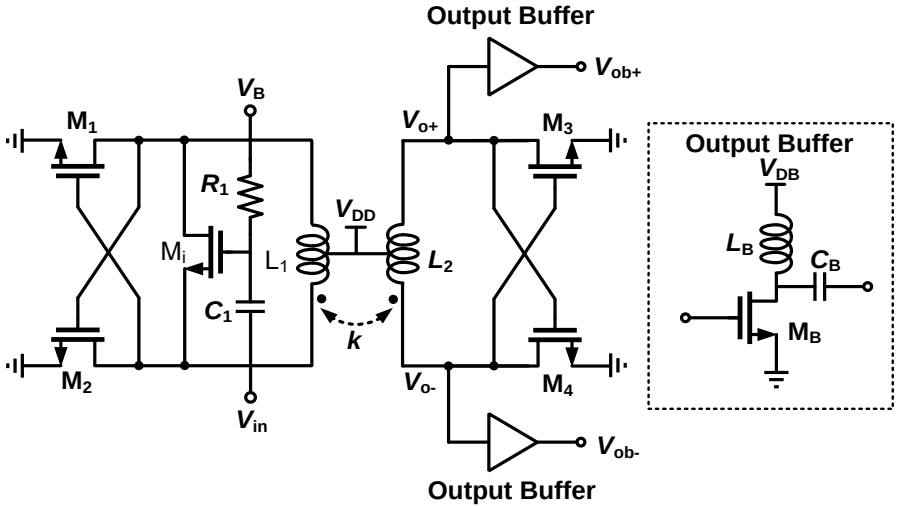

Fig. 2.27. The complete circuit schematic of proposed ILFD.

Table 2.3. Design parameters of proposed ILFD.

Design parameter	Value
M_1-M_4(W/L)(μm/μm)	10/0.09
M_i(W/L) (μm/μm)	12/0.09
L_1(nH)	0.27
L_2(nH)	0.33
k	0.6
C_1(pF)	0.4
R_1(Ω)	2k
M_B(W/L) (μm/μm)	10/0.09
L_B(nH)	0.3
C_B(pF)	0.4

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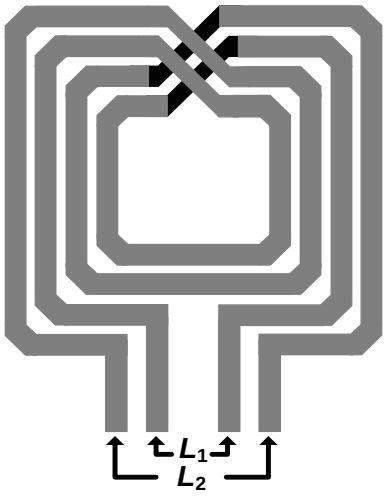

Fig. 2.28. Layout of transformer.

The design of injection transistor is followed by the previous section. The optimum locking range can be achieved by choosing appropriate input bias voltage and device size of injection transistor. To validate the previous analysis, Fig. 2.29 and Fig. 2.30 plot the locking range versus injection transistor size and gate to source voltage, V_{GS}, respectively. The widest locking range is achieved with injection transistor size of 12 μm and V_{GS} is 0.6 V. The α_{inj} is not the best value in this bias point, because the higher V_{GS} will reduce the R_{inj} more, limiting locking range by the gain condition. Additionally, the extra parasitic capacitance of injection transistor should be put into consideration. It will decrease the operation frequency and the locking range of ILFD. The output buffer implemented by common source amplifier is utilized to isolate the STCO from output loading effect. It is connected to the second coil of transformer L_2 to balance the total capacitance in two sides of transformer. The transformer and other passive components are simulated by full-wave EM simulation tool [50].

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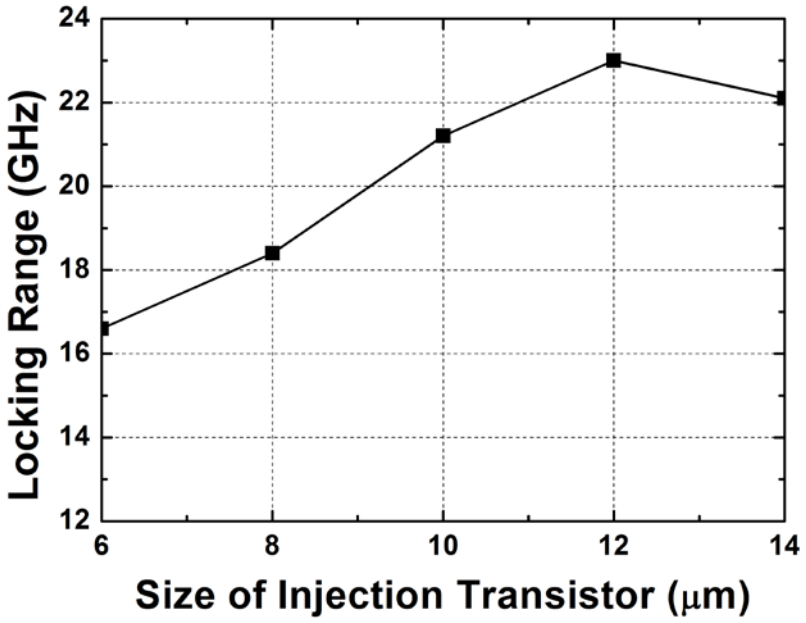

Fig. 2.29. Simulated locking range of proposed ILFD versus size of injection transistor, with V_{GS} = 0.6 V.

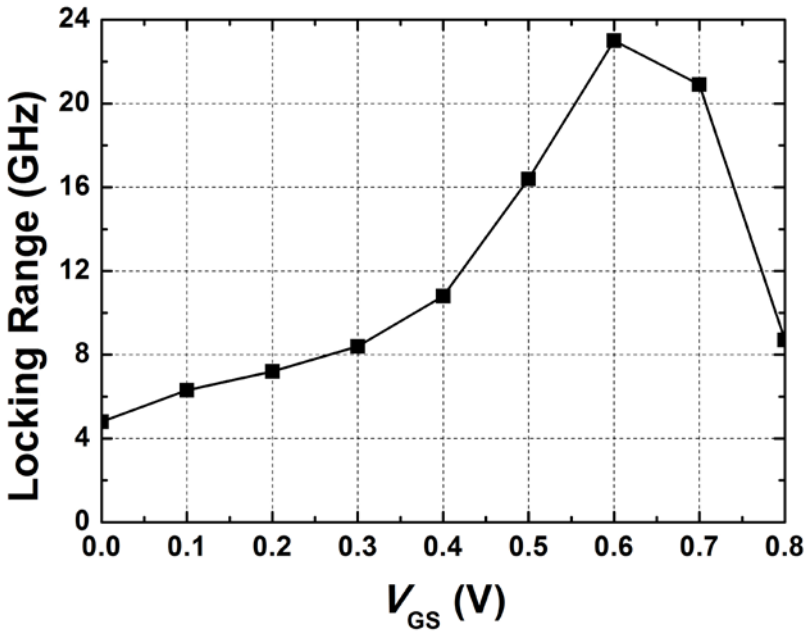

Fig. 2.30. Simulated locking range of proposed ILFD versus V_{GS} of injection transistor, with injection transistor size of 12 μm.

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To compare with conventional ILFD fairly, a conventional ILFD (Fig. 2.22) is simulated with the same injection transistor size, and the inductor value is adjusted to similar operation frequency with the same quality factor. The simulated locking ranges of the conventional and the proposal ILFD versus input voltage are shown in Fig. 2.31. Two ILFDs have the same supply voltage and power consumption, so the output voltage swings are the same. The locking range of the proposed ILFD and conventional ILFD are 22.5 and 18 GHz, respectively. The locking range improves about 25% without extra power consumption.

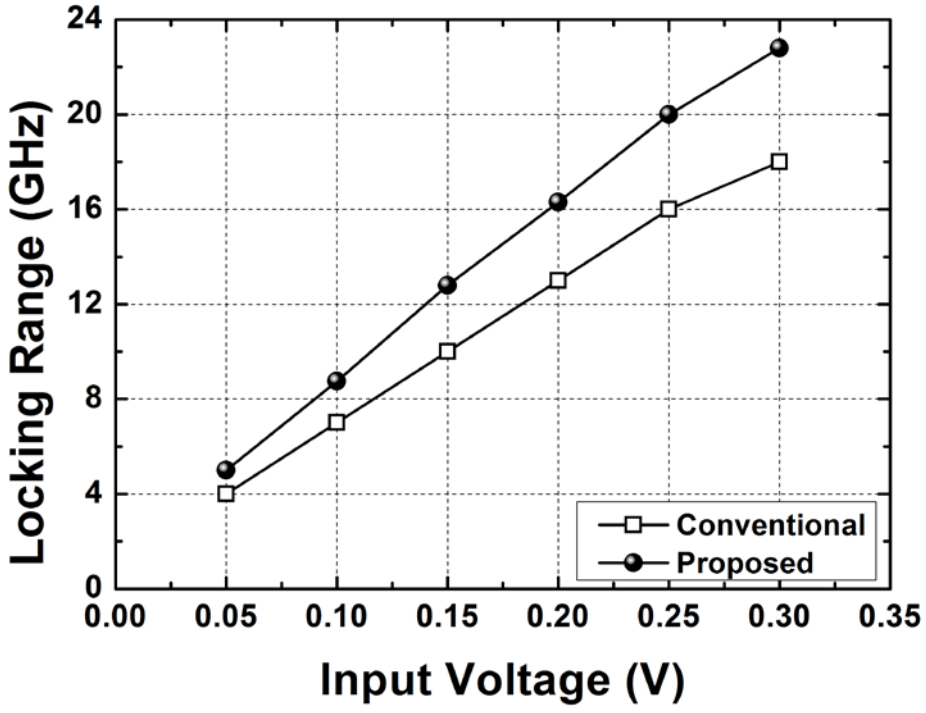

Fig. 2.31. Simulated locking range of the conventional and proposed ILFD.

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2.3.5 Measurement Results

Fig. 2.32 shows the chip microphotograph of the proposed ILFD fabricated in 90 nm CMOS technology. The die size is 0.58 × 0.35 mm^2 with all the dc and RF pads, and the ILFD core size is 0.2 × 0.13 mm^2. This circuit is measured via on-wafer probing. The block diagram of measurement setup is shown in Fig. 2.33. The input W-band signal is generated by signal generator Agilent E8257D and Agilent 83558A source module. The input power level is monitored by power meter Agilent E4418C. The output signal is measured by spectrum analyzer, Agilent E4448A. This circuit consumes 2.45 mW with 0.7 V supply voltage, excluding buffers.

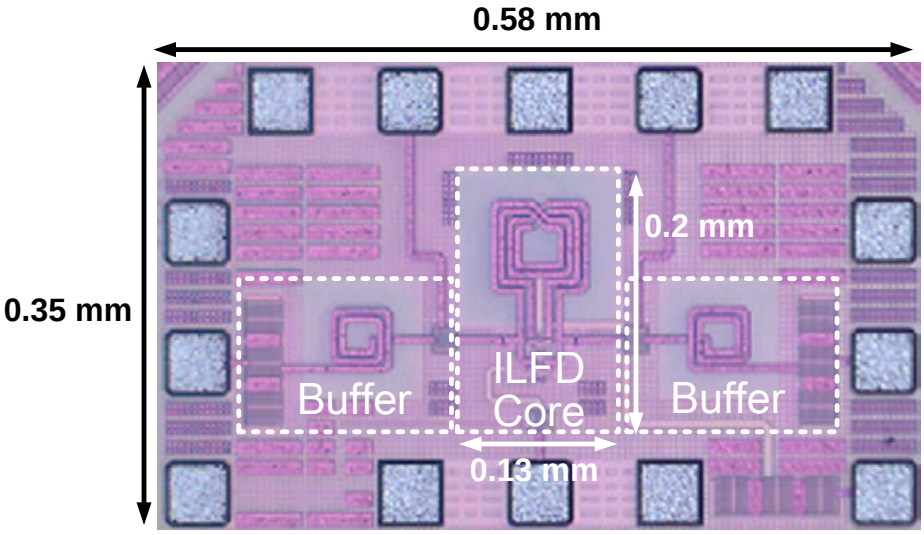

Fig. 2.32. Chip photo of proposed ILFD.

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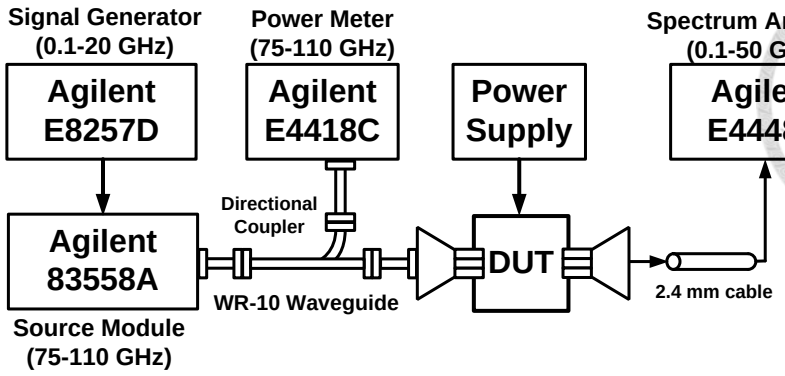

Fig. 2.33. The measurement setup for proposed ILFD.

Both the simulated and measured input sensitivity curves with a good agreement are shown in Fig. 2.34. At 0 dBm input power, the measured locking range is from 75.1 to 97 GHz at supply voltage of 0.7 V. The operating frequency shifts a little bit mainly due to inaccurate transistor model and passive element in MMW frequencies. Fig. 2.34 also shows the measured locking range at supply voltage of 0.8 and 0.9 V. Even if the self-oscillation frequency drifts slightly due to supply pushing, the locking range is not changed significantly. The locking range versus input bias voltage V_B is measured and plotted in Fig. 2.35 with the simulation results. Also, the highest and lowest locked frequencies (f_L and f_H) are shown. The locking range is raised significantly while V_B is varied from 0.6 to 1.3 V. As V_B surpasses 1.3 V, the locking range will be degraded. This measurement verifies the simulation in section IV. The simulated and measured output powers are shown in Fig. 2.36. The tendency of the measured output power is similar to the simulation and it varies from -30 to -20 dBm. Since the output power was measured from buffer's output, V_{ob}, the output power is limited. Nevertheless, the output voltage swing of divider's output, V_o, is high enough to drive the frequency divider at the next stage in practical application.

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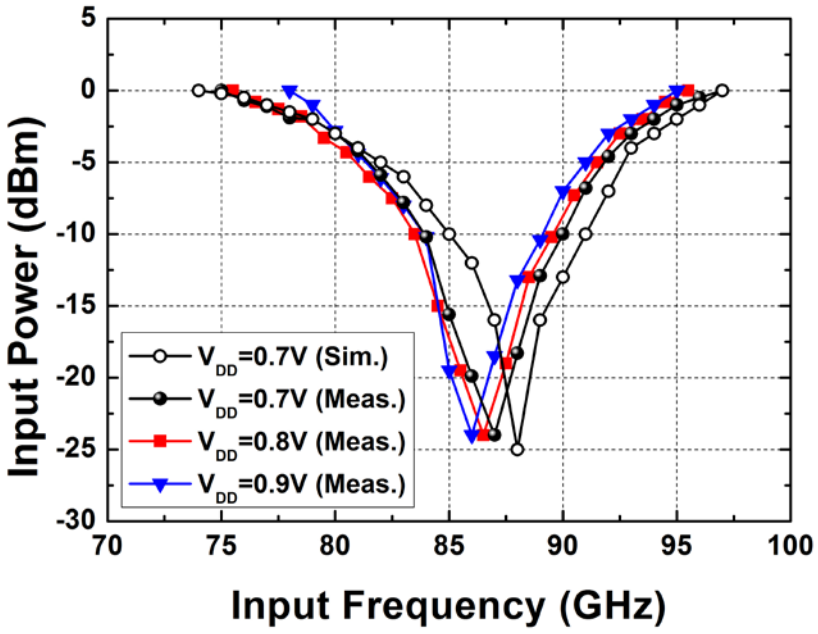

Fig. 2.34. Measured and simulated input sensitivity curves of proposed ILFD with different supply voltage.

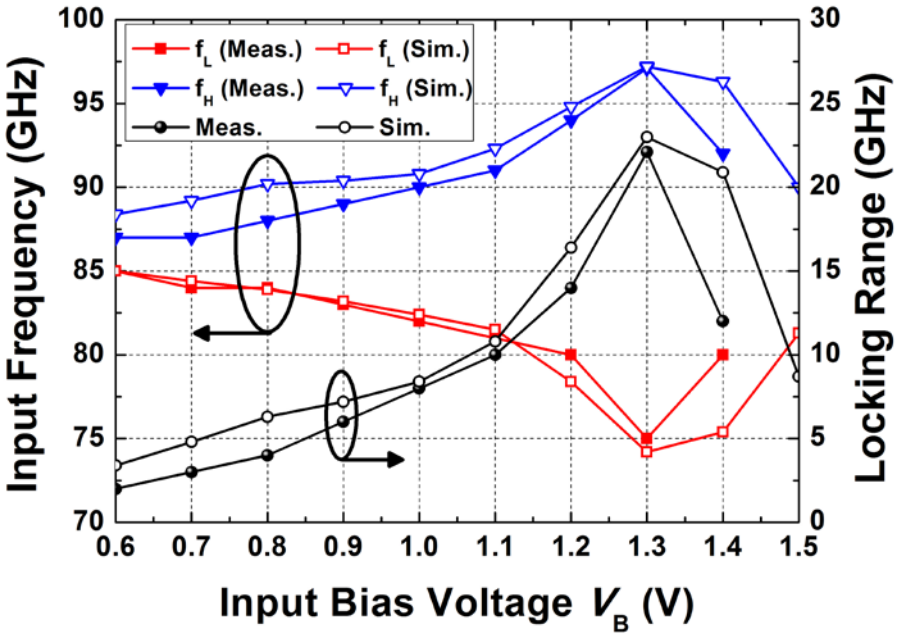

Fig. 2.35. Measured and simulated locking range versus input bias voltage V_B.

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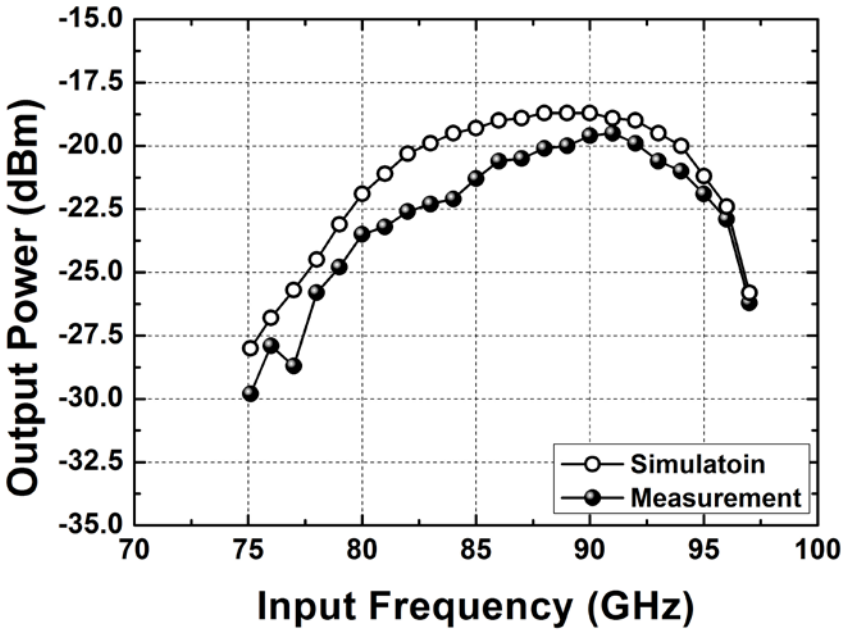

Fig. 2.36. Measured and simulated output power of proposed ILFD.

The measured input and output phase noises under lock condition are shown in Fig. 2.37. When the input frequency is 86 GHz, the measured phase noises of the input signal source and the ILFD output are -97.2 and -103.1 dBc/Hz at 100 kHz offset, respectively. This decreased phase noise is consistent with the theoretical value. Over 200 kHz offset frequency, the phase noise is corrupted by flat noise floor, and not dominated by input signal. Since the phase noise of PLL is mainly contributed by VCO, the proposed ILFD will not degrade phase noise of PLL.

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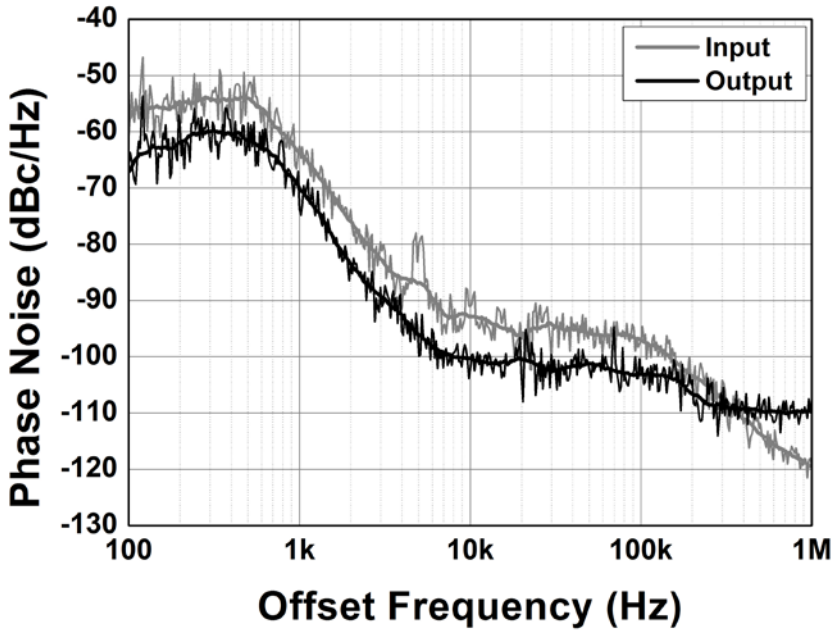

Fig. 2.37. Measured phase noise of input signal and output signal.

Table 2.4 summarizes the performance of previously reported divide-by-two frequency divider. Compared with CML divider [7], this divider has wider locking range and much lower power consumption. The proposed divide-by-two ILFD also has the competitive performance among W-band ILFDs. In general, the performance of ILFD can be evaluated with figure of merit (FOM) expressed as [13]

$$\text{FOM} = \text{Locking Range} / P_{DC} \tag{2.42}$$

Power consumption of buffer is not included in FOM calculation since buffer is not required in practical application. This ILFD has the highest FOM except for [14], due to its higher level technology and lower operation frequency. Consider the operation frequency of ILFD, the FOM_H is defined as [51]

$$\text{FOM}_H = \text{Locking Range} \times f_H / P_{DC} \tag{2.43}$$

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where f_H is the highest operation frequency of ILFD. This ILFD demonstrates the highest FOM_H among all the frequency dividers operated around W-band.

The output power is not consider into FOM and FOM_H since the output voltage swing of ILFD is usually large enough. To verify that the proposed ILFD can drive next stage divider, a 50 GHz Miller divider (Fig. 2.38) are designed as next stage divider in 90 nm CMOS and co-simulated with prosed ILFD. The simulated input and each divider output waveform are shown in Fig. 2.39. Each output frequencies are half of the previous input frequencies. It also provided enough output swing. This simulation indicates that the proposed ILFD can be applied in frequency divider chain.

Table 2.4. Comparison of published millimeter wave frequency dividers

	[7] 2008 ISSCC	[10] 2007 ISSCC	[11] 2007 TMTT	[12] 2008 ISSCC	[13] 2009 TMTT	[14] 2011 JSSC	[15] 2013 JSSC	**This Work**
Technology	65nm CMOS	65 nm CMOS	0.13 μm CMOS	90 nm CMOS	90nm CMOS	65nm CMOS	65 nm CMOS	90 nm CMOS
Topology	CML	ILFD	ILFD	ILFD	ILFD	ILFD	ILFD	ILFD
Input Frequency (GHz)	76-94.4	82-94.1	67.2-75.4	85.5-96.2	51-74	107.9 -128.8	53.4-79.4	75.1-97
Locking Range (GHz)	18.4 (21.6%)	12.1 (13.7%)	8.2 (11.5%)	10.7 (11.7%)	23 (36.8%)	20.9 (17.7%)	26 (39.2%)	21.9 (25.4%)
Input Power (dBm)	0	0	0	0	0	-2	0	0
V_{DD} (V)	2.4	0.56	1	1.2	0.5	1.1	0.8	0.7
P_{DC} (mW)[#]	64.9	3.92	4.4	3.5	3	6.27	2.9	2.45
FOM	0.28	3.09	1.86	3.06	7.67	3.33	8.97	8.94
FOM_H	26.4	290.8	140.2	294.4	567.58	428.9	712.2	867.2
Chip Size (mm^2)	0.1×0.04*	1.15×0.85	0.15×0.1*	0.66×0.51	0.13×0.29	0.32×0.17*	0.3×0.42*	0.58×0.35 (0.13×0.2*)

*core size
[#]excluding buffer

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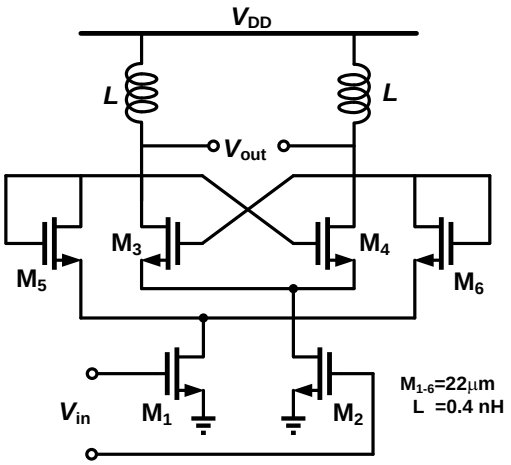

Fig. 2.38. Designed 50 GHz Miller divider as next stage divider in 90 nm CMOS

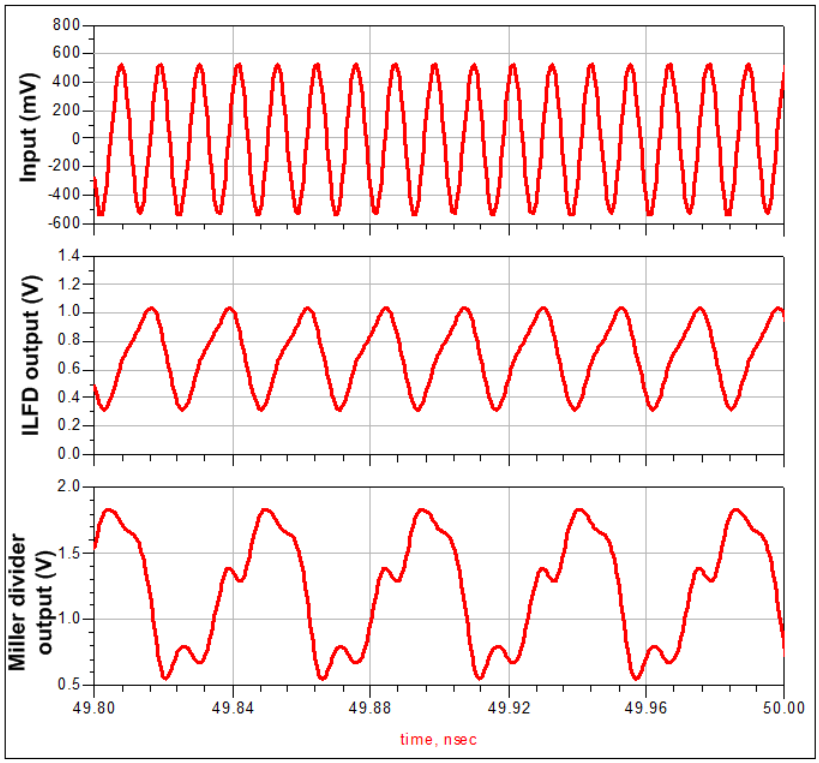

Fig. 2.39. Simulated input and each divider output waveform.

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2.4 Summary

This chapter presents two MMW frequency dividers, and proposed two methods for Miller divider and ILFD, respectively, to improve operation bandwidth.

A 60 GHz Miller divider with weak inversion mixer is proposed first. Weak inversion mixer has the advantage of high CG and low power consumption with low LO power. By using weak inversion mixer, this Miller divider exhibits very wide locking range and quite low power consumption. This Miller divider implemented in 65 nm CMOS achieves the 57% locking range from 35.7 to 64.2 GHz with 1.6-mW dc power. The proposed Miller divider has the widest locking range and the highest FOM among previous published frequency divider in MMW frequency.

The second part presents the design and analysis of a divide-by-two ILFD realized by STCO technique. The operation frequency and locking range can be improved by the proposed technique without extra power consumption and chip area. Also, from the analysis, the optimum locking range can be obtained with suitable bias and size of injection transistor. The proposed ILFD has been fabricated in 90 nm CMOS technology. The measured locking range is 21.9% from 75.1 to 97 GHz at 0-dBm input power without any frequency tuning mechanism. The dc power consumption is 2.45 mW with a 0.7-V supply voltage.

Two frequency dividers have low power, wide bandwidth and small size, and it is suitable for integration in low power PLLs in MMW frequency.

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Chapter 3 Millimeter-wave Phase Shifter Design

3.1 Introduction of Phased Array [52], [53]

Phased array which is special case of multiple-input-multiple-output (MIMO) systems applied in radar and astronomy application. The antenna beam can be formed and steered in desired direction by controlling the phase delay in each path independently, shown in Fig. 3.1. In addition to provide beam steering and beam forming capabilities, the effective isotropic radiated power (EIRP) in main beam direction is improved 20log(*N*) dB (*N* is number of phased array element), Due to the coherent addition of signals in *N*-element phased array transmitter. Meanwhile, the uncoherent addition of signals at undesired direction assures less interference is generated at receivers which are not targeted. Similarly, in phased array receiver, the received signals also combined coherently in desired direction and attenuate interfering signals from other direction. Because the noise generated from each element is uncorrelated, the output signal to noise ratio (SNR) can be improved 10log(*N*) dB, thereby improves receiver's sensitivity. Due to the above benefits, phased array based transceiver leads to higher data rates and network capacity.

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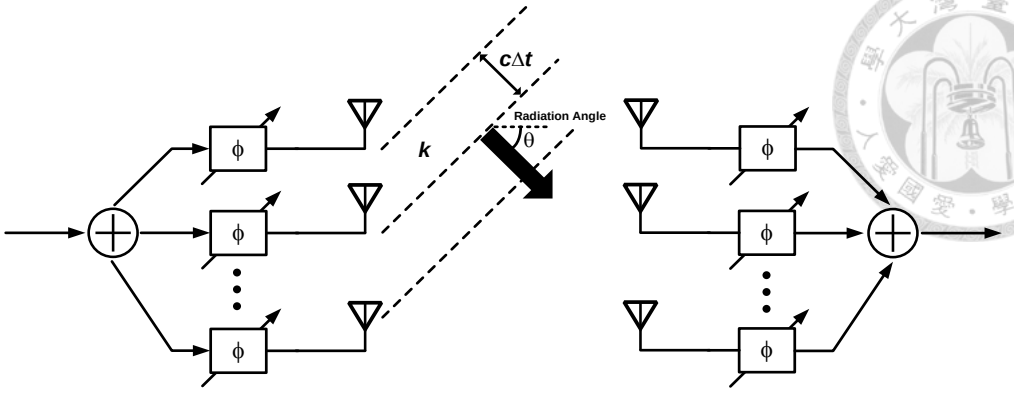

Fig. 3.1. *N*-element phased array transmitter and receiver.

3.2 Phased Array Architectures

There are several phased array architectures. Based on the method of phase shifting, the phased arrays can be categorized into digital phase shifting [54], IF phase shifting [55], LO phase shifting [31]-[33], [57], [58], and RF phase shifting [59]-[63].

The architecture of RF phase shifting is shown in Fig. 3.2(a). This architecture with tunable phase shifter in each RF path combine signal at RF path. RF phase shifting has the advantage of low power consumption and small chip size since the required number of components is minimum. However, the transceiver performance is influenced by phase shifter easily since the phase shifters are located in RF signal paths directly. On the other hand, LO phase shifting performs phase shift in LO signal paths as shown in Fig. 3.2(b), so the transceiver performance is insensitive to the phase shifter. The disadvantage of LO phase shifting is complex LO distribution network. Also the large number of components leads to high power consumption and large chip area. The IF phase shifting shown in Fig. 3.2(c) executes phase shift at low frequency, so the design challenge of phase shift are relaxed. Nevertheless, the phase shifters at IF frequency need higher fractional bandwidth and larger chip size than that at RF and LO frequency. Be-

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sides, it also suffers from the same issue as LO phase shifting. The architecture of digital phase shifting is shown in Fig. 3.2(d). The down-converted signals are digitalized by analog-to-digital converter (ADC), and the antenna beam is steered by digital function instead of using phase shifters at each element in the phased array. The operation bandwidth is limited by ADC, and the high resolution and dynamic range ADCs require high power consumption. To achieve wideband and low power application, RF and LO phase shifting are more desirable architectures.

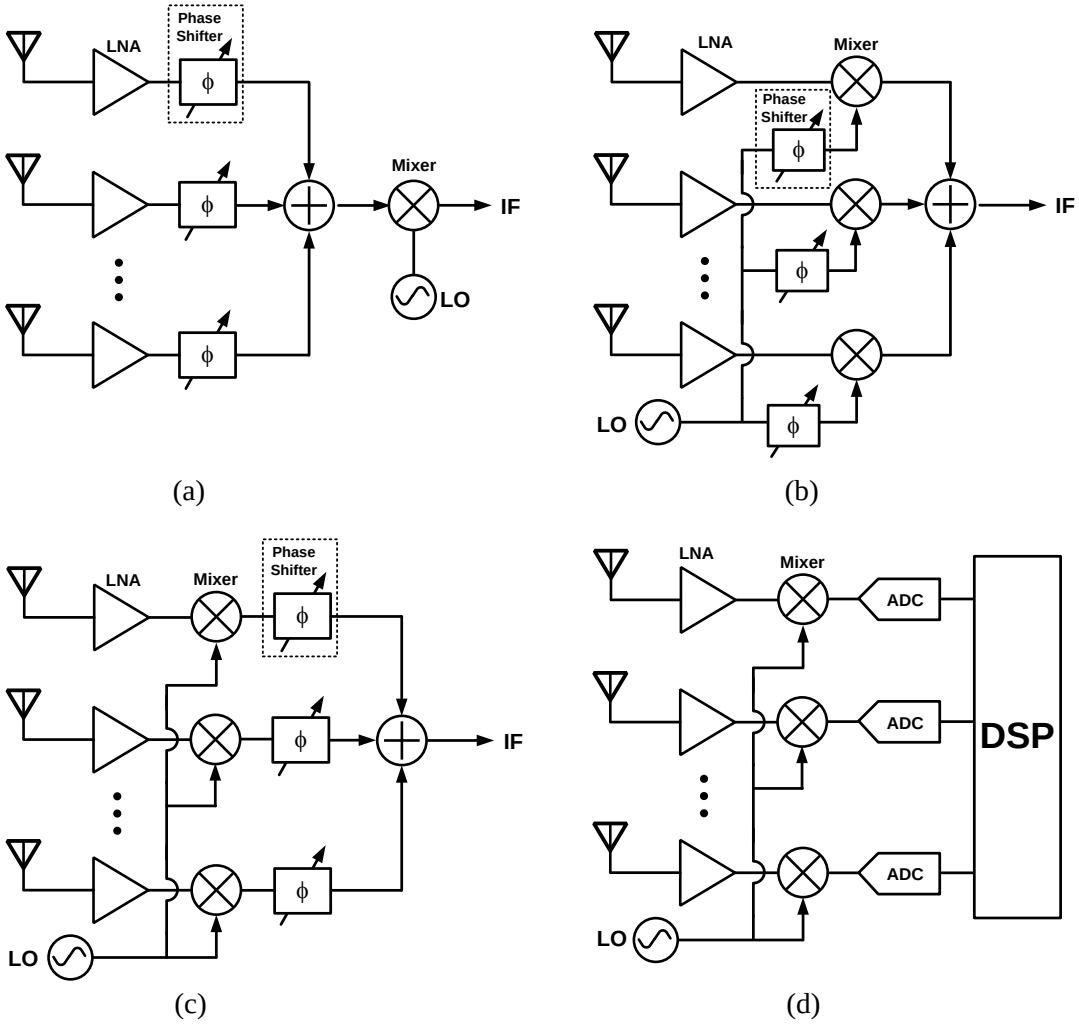

Fig. 3.2. Different phased array architecture: (a) RF phase shifting. (b) LO phase shifting. (c) IF phase shifting. (d) Digital phase shifting.

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Table 3.1 summarizes the comparison of 4 type phased array architecture. Typically, the phased array transceivers with large number of channels (i.e., >16) is usually implemented using RF phase shifting architecture. For the transceivers with small number of channels (i.e., <4), the LO phase shifting architecture is more suitable.

Table 3.1. Comparison of 4 type phased array architecture

Architecture	DC Power	Bandwidth	Chip Size	Design Challenge
RF Phase Shifting	Low	Wide	Small	Low loss, low amplitude variation
LO Phase Shifting	High	Wide	Large	LO distribution
IF Phase Shifting	High	Narrow	Large	LO distribution, low amplitude variation
Digital Phase Shifting	High	Narrow	Large	LO distribution, fast ADC

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3.3 Overview of Phase Shifter

3.3.1 Transmission Line Phase Shifter [16]

The transmission line phase shifter (TLPS) is composed of distributed low-pass sections as artificial transmission line. As shown in Fig. 3.3, the low-pass distributed section is a π configuration with tunable capacitors. The insertion phase can be varied by the tunable capacitors, and the insertion phase of each π section can be derived as [16]

$$\phi(C) = \tan^{-1}\left[\frac{\omega C^2 Z_0^3 / L - 2\omega C Z_0 - \omega L / Z_0}{2\left(1-\omega^2 LC\right)}\right]. \tag{3.1}$$

The maximum relative phase shift is given as

$$\Delta\phi_{\max} = \left|\phi(C_{\max}) - \phi(C_{\min})\right| \tag{3.2}$$

It can be observed that the phase shift range is limited by the tunable capacitors. Larger phase shift can be obtained by adding more stages of π section, but insertion loss is degraded by more stages. Therefore, there is the tradeoff between phase shift range and total insertion loss. To solve this issue, the active inductors can be utilized in TLPS design [64].

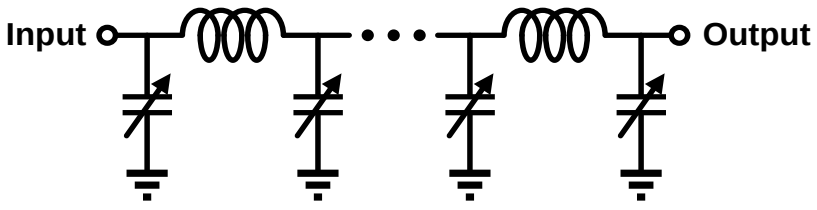

Fig. 3.3. Transmission line phase shifter [16].

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3.3.2 Reflection Type Phase Shifter [17]

As shown in Fig. 3.4, reflection type phase shifter (RTPS) is consisted of a 3-dB quadrature coupler and two identical reflection loads. The phase shift is generated by phase difference of input and reflected signals. By signal flow in Fig. 3.4, the output phase can be written as

$$\phi(Z_L) = \frac{\pi}{2} + \theta \tag{3.3}$$

where θ is the phase of reflection coefficient of reflection load which can be expressed as

$$\theta = \angle\Gamma_L = \tan^{-1}\left[\frac{\mathrm{Im}(Z_L)}{\mathrm{Re}(Z_L) - Z_0}\right] - \tan^{-1}\left[\frac{\mathrm{Im}(Z_L)}{\mathrm{Re}(Z_L) + Z_0}\right] \tag{3.4}$$

Z_L is the impedance of reflection load with maximum and minimum values of Z_{max} and Z_{min}, respectively, and Z_0 is the characteristic impedance of coupler. Thus, the maximum relative phase shift is given as

$$\Delta\phi_{max} = \left|\phi(Z_{max}) - \phi(Z_{min})\right| \tag{3.5}$$

It can be observed that the phase shift range is limited by the phase tuning of reflection coefficient. However, wider phase tuning cause higher reflective loss variation, so there is the tradeoff between phase shift range and loss variation [17].

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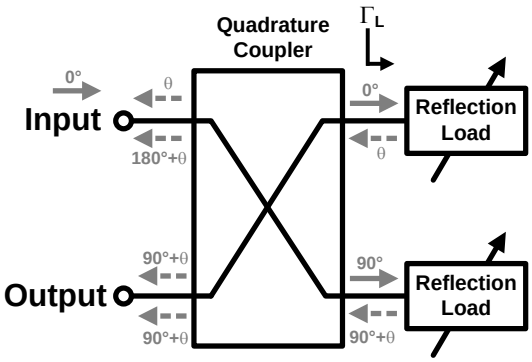

Fig. 3.4. Reflection type phase shifter [17].

3.3.3 Vector Sum Phase Shifter [21]

Fig. 3.5 shows the vector sum phase shifter which contains quadrature generator, variable gain amplifier (VGA) and adder. The input signal is spilt into in-phase and quadrature-phase signal by quadrature generator. Then, two quadrature signals are amplified independently by VGA, and summed together at output. The desired arbitrary phase shift can be obtained by adjust each gain of VGA. However, large chip area and high power consumption make it hardly to be integrated in phase array system.

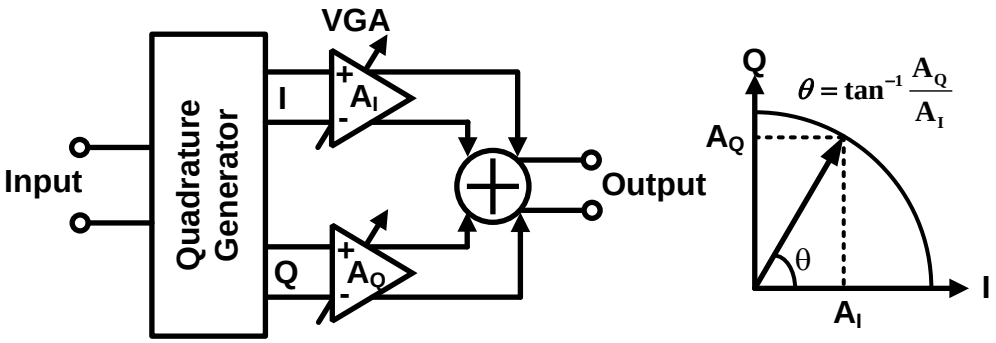

Fig. 3.5. Vector sum phase shifter [21].

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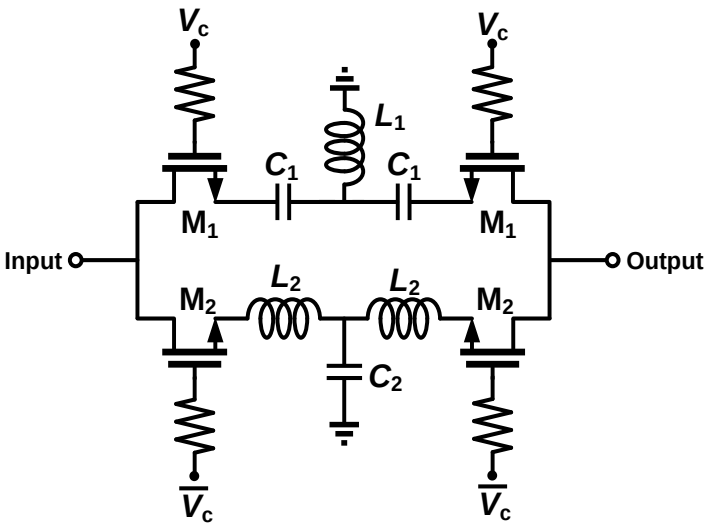
3.3.4 Switch Type Phase Shifter [25]

The general switch type phase shifter (STPS) which include switch and delay cell perform phase shift by switching different signal paths of delay cells. Fig. 3.6(a) shows the conventional STPS of which delay cell is implemented by low-pass filter (LPF) and high-pass filter (HPF) [25]. The LPF and HPF in STPS can provide positive and negative phase shift, respectively, so the desired arbitrary phase shift can be obtained by choosing appropriate inductor and capacitor values. Since this type of phase shifter is discretely controlled, the n bit 360° phase shifter can be easily achieved by series connecting multi-stage STPS, as illustrated in Fig. 3.6(b). Fully digital control is the main advantage of this type of phase shifter. However, in CMOS process, it suffers from high loss and large area of passive components. Another STPS topology to solve the issue will be presented in section 3.4.



(a)

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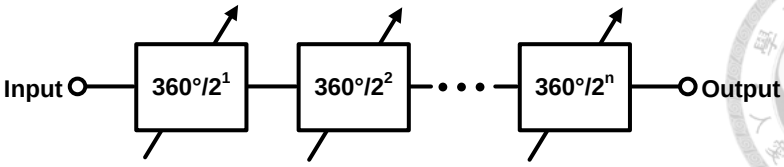

(b)

Fig. 3.6. (a) The switch type phase shifter [25], and (b) multi-stage switch type phase shifter.

3.3.5 Injection-Locked Phase Shifter [30]

In addition to frequency division, the injection locking also can be used in phase shifting. The locking phenomenon has been presented in section 2.1.3. The injection-locked phase shifter is based on injection-locked oscillator (ILO). When an ILO is locked by injection signal, the output frequency is equal to input frequency, and tuning the self-oscillation frequency results in phase shifting between input and output frequency. Since the output voltage swing is dominated by the oscillation current of ILO and voltage swing, the output amplitude variation over tuning phase range is small. However, the phase tuning range of ILPS is small. More detail of ILPS will be described in section 3.5, and a method to overcome the drawback of ILPS also will be presented.

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3.4 Four Bit RF Phase Shifter for 60-GHz RF Phased Array

3.4.1 Introduction

In recent years, several RF phased arrays are employed in beamforming system due to the small area and low power consumption. As mention before, RF phased array system is easily affected by phase shifter. Hence, the high performance phase shifter is desired. Besides, in MMW, there are many design challenges such as phase resolution, phase and gain error, etc.

Several type topologies of phase shifter have been proposed and presented in previous section. The RTPS and VSPS are attractive due to large phase shift range and continuous phase tuning. However, they need a high resolution DAC for digital controlling. The STPS has advantage of digital control. Nevertheless, to achieve wide phase range, more cascade stages contribute the higher loss and occupy larger area. Furthermore, most of phase shifters suffer from high gain and phase error which result in inaccuracy of beam. Therefore, VGA are usually integrated with phase shifter in phase array system to minimize the gain error [27]. However, when the gain error is compensated by VGA, the VGA will contribute some phase error. The phase error produced by VGA cannot be eliminated easily.

Section 3.4 presents a 60 GHz 4 bit passive phase shifter with low phase and gain error. This phase shifter can achieve 360° phase tuning range and resolution of 22.5°. Phased array with 4 bit resolution can achieve 7° beam steering resolution and satisfy many reported beam forming applications [22]-[24], [62], [65]. STPS is used for small phase shift, while the large phase shift is realized by quadrature phase rotator (QPR).

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This phase shifter not only exhibits low phase and amplitude error, but also has low gain flatness. Besides, this phase shifter can be operated without dc power consumption and DAC requirement.

3.4.2 Architecture

The traditional 4-bit phase shifter is consisted of 4-stage STPS to generate 16 phase states. The advantages of this topology are zero dc power and no need of extra DACs. However, due to the process variation, each STPS will contribute some phase and amplitude error, especially at 90° and 180° stage. To minimize the phase and amplitude error, the quadrature phase rotator are utilized to replace the 90° and 180° STPS in this design.

The block diagram of proposed phase shifter is shown in Fig. 3.7. This phase shifter includes a 2-stage STPS and a QPR. The STPS is used to perform 22.5° and 45° phase shifts due to its good performance in small phase shift. The output of STPS is connected to a vector generator to generate quadrate signals. The quadrate signals will pass through vector selector to synthesize the phase of 90° and 180°. The phase and amplitude error induced by vector selector are small. Besides, it consumes zero dc power and has similar loss as the traditional STPSs.

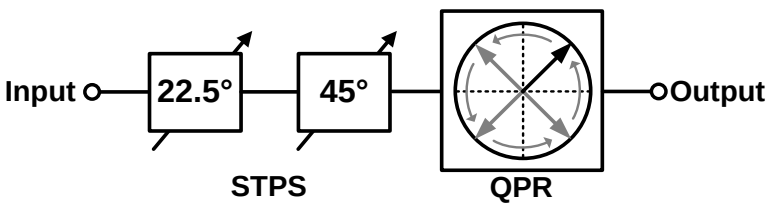

Fig. 3.7. Block diagram of proposed 4 bit RF phase shifter.

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3.4.3 Switch Type Phase Shifter

The conventional STPS based on switching LPF and HPF has been introduced in section 3.3.4. Although large phase shift can be obtained easily by this topology, it is still not suitable to realize in CMOS process at MMW due to high loss and large area of passive component. In fact, there are other better methods to implement STPS. Fig. 3.8(a) shows the schematic of π-type LPF-based STPS which is consisted of two capacitors, two inductors, and two MOS switches [26]. When M_1 is turned off and M_2 is turned on, the circuit is equivalent to a π-type LPF as shown in Fig. 3.8(b), which generates a phase delay. When M_1 is turned on and M_2 is turned off, L_R resonates with parasitic capacitor C_{off} contributed by off-state M_2, creates an open circuit at resonated frequency. Then the equivalent circuit can be simplified as Fig. 3.8(c). The desired phase shift is determined by parameter of L_S, C_P and L_R derived as [26]

$$L_S = \frac{Z_0 \sin \Delta\phi}{\omega_0} \tag{3.6}$$

$$C_P = \frac{1}{\omega_0 Z_0} \tan \frac{\Delta\phi}{2} \tag{3.7}$$

$$L_R = \frac{1}{\omega_0^2 C_{off}} \tag{3.8}$$

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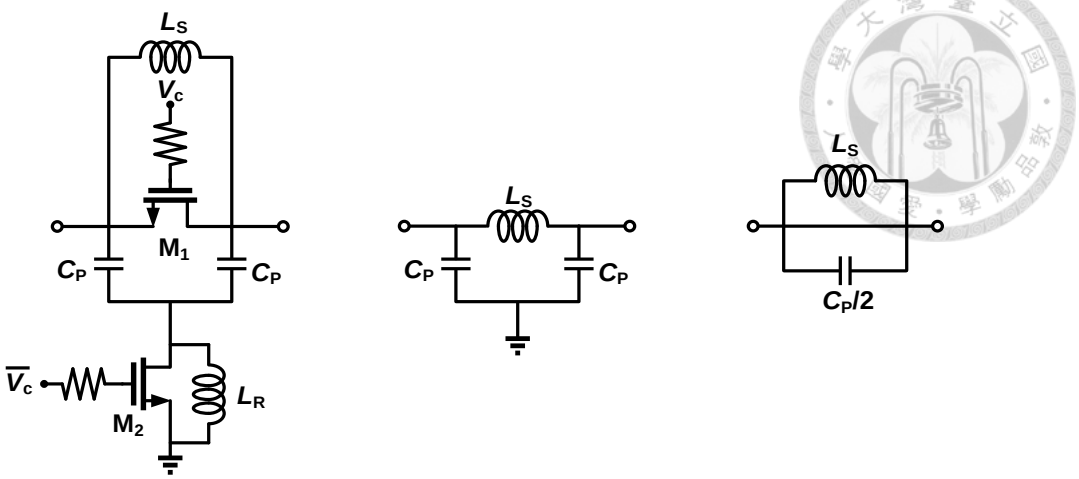

(a) (b) (c)

Fig. 3.8. (a) π-type LPF-based STPS. (b) Equivalent circuit when V_c = 0 V. (c) Equivalent circuit when V_c = 1.2 V.

Fig. 3.9(a) shows the T-type LPF-based STPS which comprise three inductors and three MOS switches [25]. When M_1 and M_2 are turned off and M_3 is on, the circuit is equivalent to a low pass filter as shown in Fig. 3.9(b), which produces a phase delay. When M_1 and M_2 are turned on and M_3 is turned off, the circuit can be simplified to a parallel resonator, as shown in Fig. 3.9(c). By switching these two states, the desired phase shift can be obtained by design parameter L_1, L_2, C_2 and C_3 was also derived as [25]

$$L_1 = \frac{Z_0}{\omega_0}\tan\left(\frac{\Delta\phi}{2}\right) \tag{3.9}$$

$$L_2 = \frac{1}{\omega_0^2 C_3} \tag{3.10}$$

$$C_2 = \frac{\sin\Delta\phi}{\omega_0 Z_0} \tag{3.11}$$

$$C_3 = \frac{2L_1}{Z_0^2} \tag{3.12}$$

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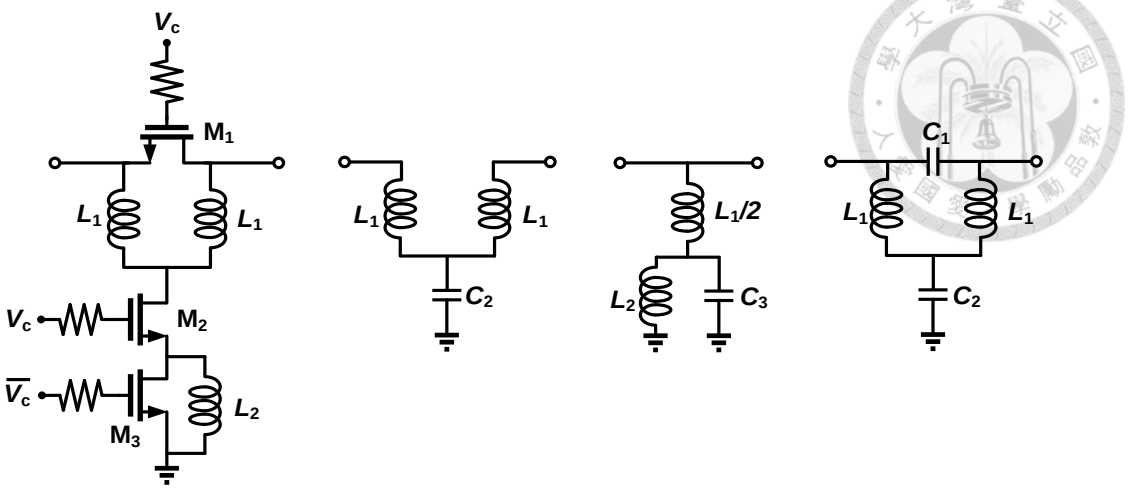

Fig. 3.9. (a) T-type LPF-based STPS. (b) Equivalent circuit when V_c = 0 V. (c) Equivalent circuit when V_c = 1.2 V. (d) Modified equivalent circuit when V_c = 0 V.

π-type LPF-based STPS need extra capacitor to construct LPF. Since the capacitor implemented by metal insulator metal has less accuracy in MMW due to process variation, T-type LPF-based STPS is adopted in proposed phase shifter design.

In previous analysis, the off-capacitance C_1 contributed by M_1 is neglected, since the capacitor value is small in lower frequency. However, in millimeter wave frequency, the parallel capacitor C_1 together with the low pass filter transform into band-pass filter as shown in Fig. 3.9(d), and the performance of phase shifter are influenced significantly. Considering the off-capacitance C_1, the detail analysis is shown as follow. When the phase shifter is set as band-pass filter, S_{11} and S_{21} are derived as

$$S_{11} = \frac{j\omega\left(2\omega^2 L_1 C_1 C_2 Z_0^2 - \omega^2 L_1^2 C_2 - C_2 Z_0^2 + 2L_1\right)}{\left(2 - \omega^2 L_1 C_2 + j\omega C_2 Z_0\right)\left(Z_0 - 2\omega^2 L_1 C_1 Z_0 + j\omega L_1\right)} \tag{3.13}$$

$$S_{21} = \frac{2Z_0\left(1 - 2\omega^2 L_1 C_1 + \omega^4 L_1^2 C_1 C_2\right)}{\left(2 - \omega^2 L_1 C_2 + j\omega C_2 Z_0\right)\left(Z_0 - 2\omega^2 L_1 C_1 Z_0 + j\omega L_1\right)}. \tag{3.14}$$

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From (2), the insertion phase ϕ_1 can be expressed as

$$\phi_1 = -\tan^{-1}\left(\frac{\omega C_2 Z_0}{2-\omega^2 L_1 C_2}\right) - \tan^{-1}\left(\frac{\omega L_1}{Z_0 - 2\omega^2 L_1 C_1}\right) \tag{3.15}$$

For perfect matching at frequency ω_0, S_{11} is set to be zero, and the capacitance C_2 can be express as

$$C_2 = \frac{2L_1}{Z_0^2 + \omega_0^2 L_1^2 - 2\omega_0^2 Z_0^2 L_1 C_1} \tag{3.16}$$

According to [25], when phase shifter is switched as a parallel resonator, the insertion phase ϕ_2 is zero at frequency ω_0 and the phase shift $\Delta\phi$ can be obtained by subtracting ϕ_1 from ϕ_2 ($\phi = \phi_2 - \phi_1$). Thus, the design equation for L_1 is obtained as

$$L_1 = \frac{Z_0 \tan\left(\frac{\Delta\phi}{2}\right)}{\omega_0\left(1 + 2\omega_0 C_1 Z_0 \tan\left(\frac{\Delta\phi}{2}\right)\right)} \tag{3.17}$$

Also, perfect matching should satisfied in parallel resonator mode, the relationship of inductance and capacitance can be found as [25]

$$L_2 = \frac{1}{\omega_0^2 C_3} \tag{3.18}$$

To achieve broadband phase shift, the phase response should have same variation in frequency ω_0. The condition can be written as

$$\left.\frac{d\phi_1}{d\omega}\right|_{\omega=\omega_0} = \left.\frac{d\phi_2}{d\omega}\right|_{\omega=\omega_0}. \tag{3.19}$$

As band pass filter mode, the derivative of the insertion phase ϕ_1 at frequency ω_0 can be calculated as

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$$\left.\frac{d\phi_1}{d\omega}\right|_{\omega=\omega_0} = -\frac{2C_2(2+\omega_0^2 C_2 L_1)Z_0}{4-4\omega_0^2 C_2 L_1+\omega_0^4 C_2^2 L_1^2+\omega_0^2 C_2^2 Z_0^2}. \quad (3.20)$$

As parallel resonator mode, the derivative of insertion phase ϕ_1 at frequency ω_0 has been calculated in [25] and shown as

$$\left.\frac{d\phi_2}{d\omega}\right|_{\omega=\omega_0} = -C_3 Z_0 \quad (3.21)$$

By the equality of (8) and (9), the following condition can be obtained for broad band phase response.

$$C_3 = \frac{2C_2(2+\omega_0^2 C_2 L_1)}{4-4\omega_0^2 C_2 L_1+\omega_0^4 C_2^2 L_1^2+\omega_0^2 C_2^2 Z_0^2} \quad (3.22)$$

Thus, the new design equations (3.4)-(3.6) and (3.10) can be used to calculate the design parameters of the T-type LPF-based STPS. In fact, there will be parasitic resistance as the switch turns on. Since the on-resistance of M_1 is inversely proportional to C_1, considering that on-resistance is smaller than 10 Ω, C_1 should at least 20 fF. At the condition of Z_0 = 50 Ω and $\omega_0 = 2\pi \times$ 60 GHz, the design parameters of 22.5° and 45° STPS are shown in Table 3.2. Fig. 3.10 shows the phase response of STPS with and without C_1. It shows that the phase shift has at least 10% variation without C_1. Consequently, the STPS designed with modified equation can achieve more accurate phase shift. The schematic of the STPS which cascade two stages together is shown in Fig. 3.11. To achieve compacted chip size and reduce the influence caused by process variation, the inductors are implemented using microstrip lines.

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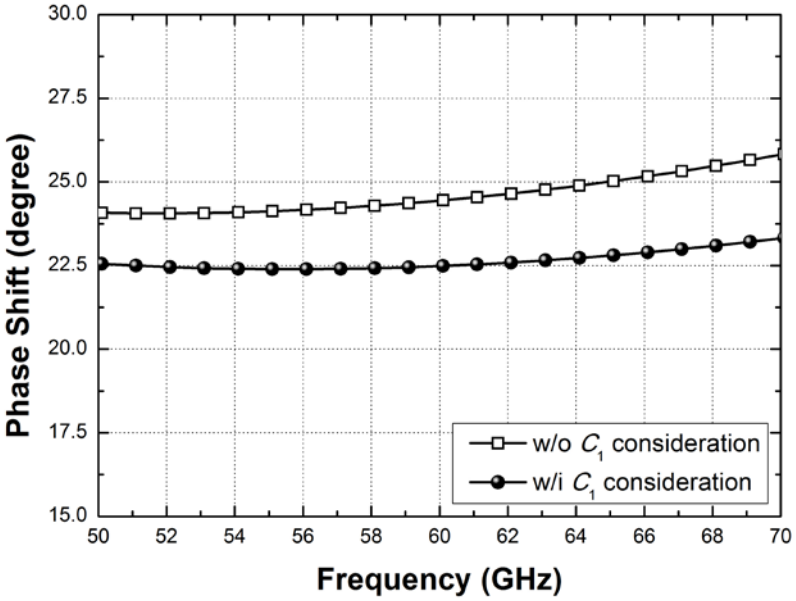
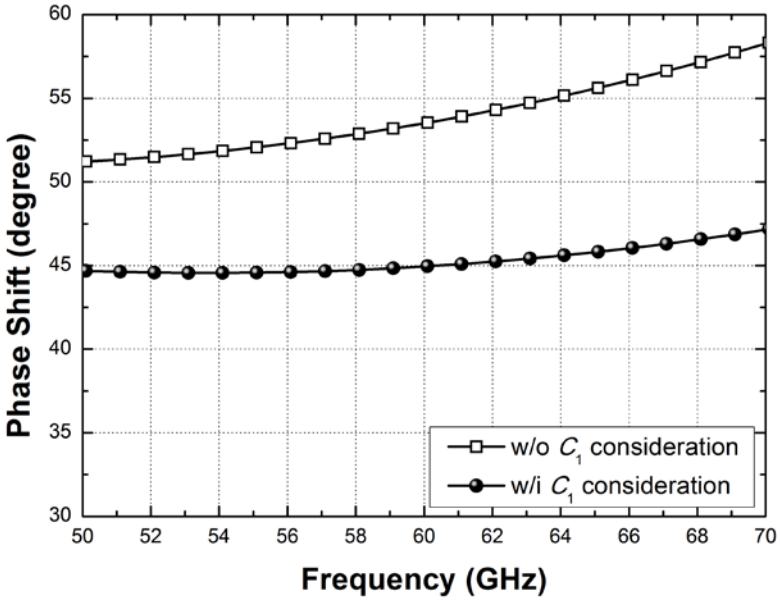


(a)



(b)

Fig. 3.10. Simulated phase shift of (a) 22.5° and (b) 45° STPS with and without C_1 consideration

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Table 3.2. Calculated design parameters for STPS

	L_1(pH)	L_2(pH)	C_2(fF)	C_3(fF)
22.5°	22.9	324	20.4	21.7
45°	41.9	149	38.8	47.3

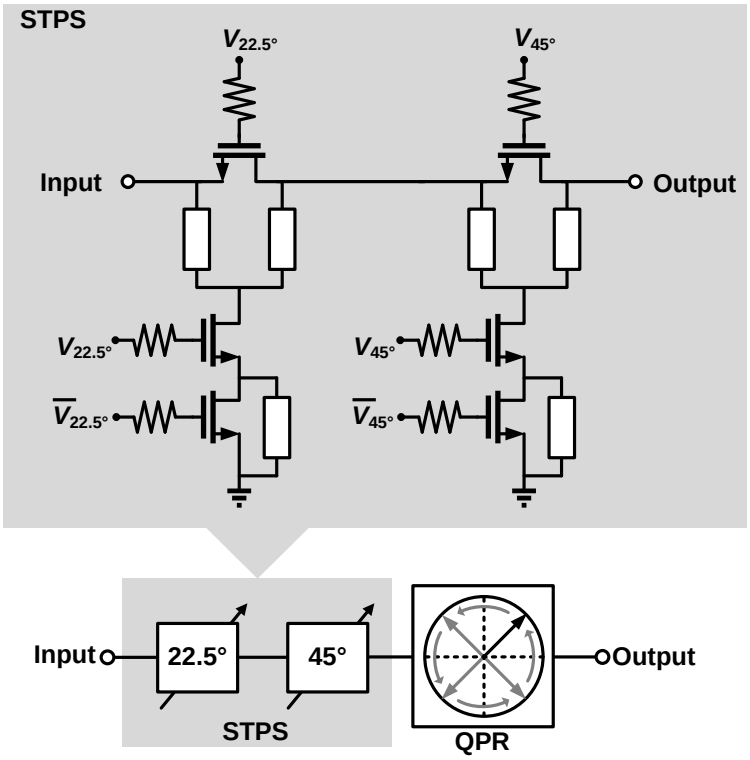

Fig. 3.11. Schematic of 2 stages STPS.

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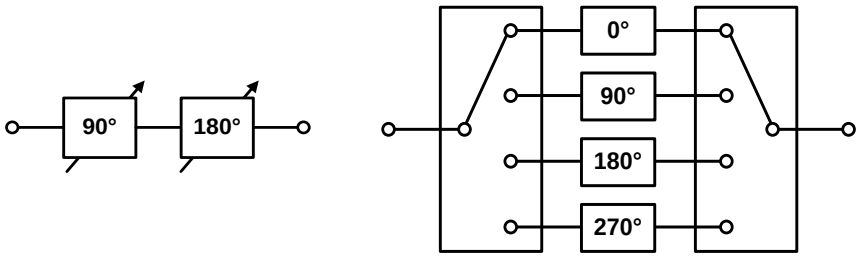
3.4.4 Quadrature Phase Rotator (QPR)

QPR is a type of phase shifter which can achieve arbitrary quadrature phase shift. The conventional way to implement QPR is using series STPS as shown in Fig. 3.12(a). By series connecting two variable phase shifters, the arbitrary quadrature phases can be obtained. However, the insertion loss and phase shift are changed significantly between different phase states, since the input and output loads of individual phase shifter will vary during switching the phase states. The other way to realize quadrature phase rotator is parallel switch type phase shifter, which comprise absorptive single pole four though (SP4T) switch and four fixed phase shifters as shown in Fig. 3.12(b). By adopting the absorptive SP4T switch, the input and output impedances of the fixed phase shifters are similar in different phase states, and thus, the phase and amplitude error are relatively small. Nevertheless, it requires more building blocks and occupies larger area. Also, the absorptive SP4T switch contributes higher loss in CMOS process. As shown in Fig. 3.13, a quadrature phase rotator consisting of a vector generator and a vector selector is proposed. This QPR exhibits low phase and amplitude errors, as well as compact size.



(a) (b)

Fig. 3.12. Block diagram of (a) series STPS and (b) parallel STPS.

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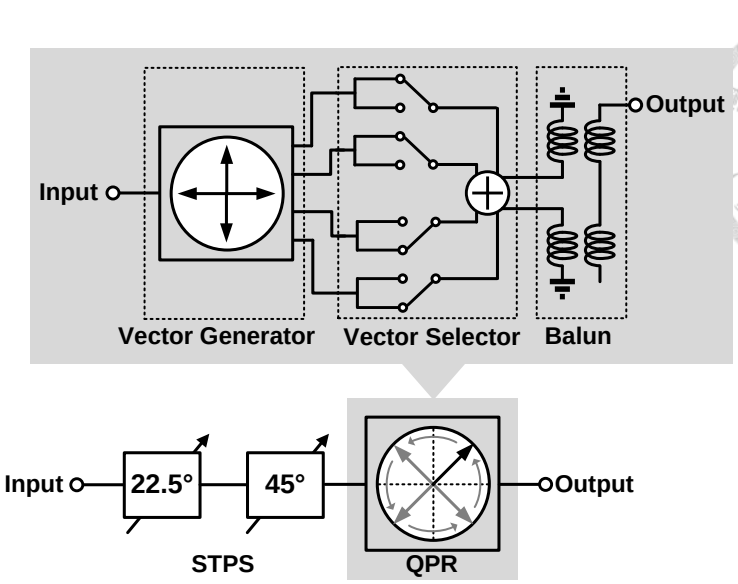

Fig. 3.13. Proposed quadrature phase rotator (QPR).

3.4.4.1 Vector Generator

The vector generator is a single input and four quadrature outputs power divider with low magnitude and phase imbalance. This vector generator consists of a 90° coupler and two balun, as shown in Fig. 3. The Marchand balun is used due to its broadband response [66]. The broadside coupling is utilized to obtain higher coupling coefficient. For the 90° coupler, a broadside coupler also implemented using thin-film microstrip line structure [66]. To acquire appropriate coupling coefficient, additional horizontal offset is introduced. The input and output impedance are designed to match the reference impedance 50 Ω over wide bandwidth. Besides, the 90° coupler can be meandered and the Marchand balun can be wounded into coils to achieve compact layout, and the total size of vector generator is 290 × 140 μm^2. The 3D-view of vector generator is shown in Fig. 3.15. Fig. 3.16 shows simulated magnitudes and phases of output quadrature signals by full electromagnetic modeling. The simulated insertion losses are

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8.5 dB from 55 to 67 GHz. The magnitude and phase imbalance between quadrature outputs are within 0.6 dB and 3°, respectively.

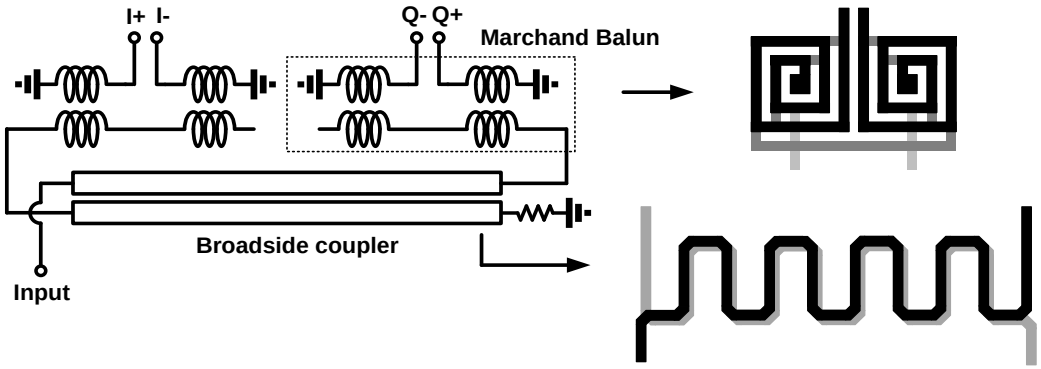

Fig. 3.14. Schematic of vector generator.

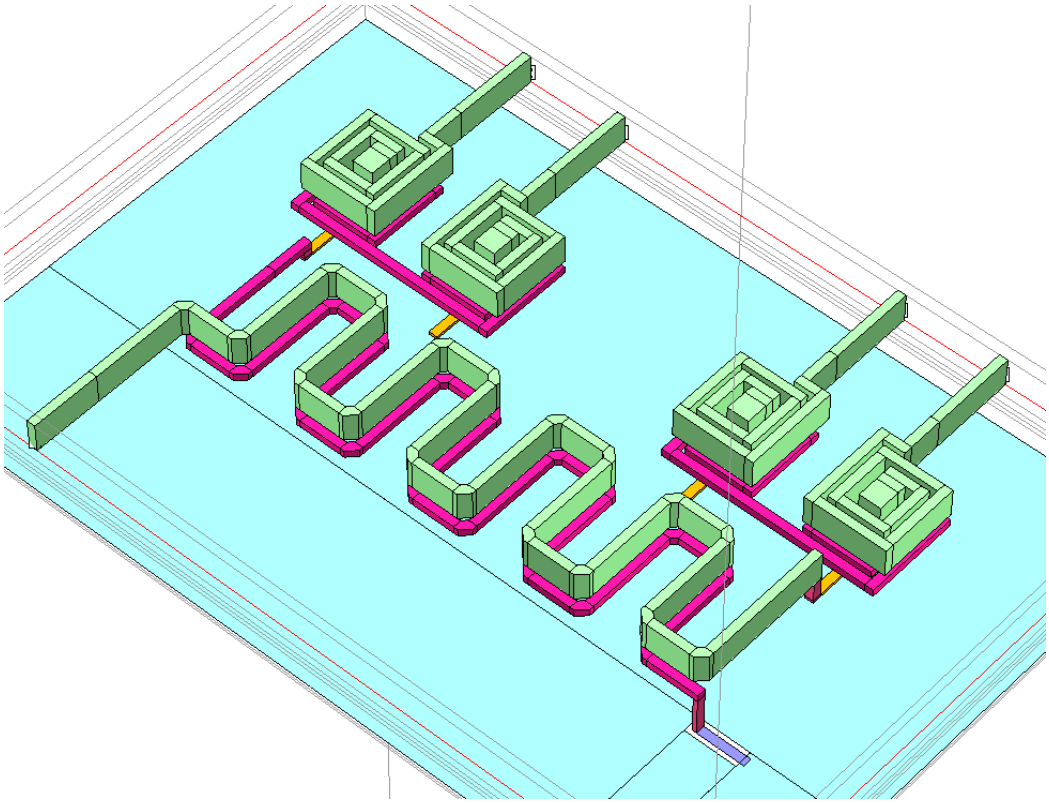

Fig. 3.15. 3D view of vector generator in full EM simulator.

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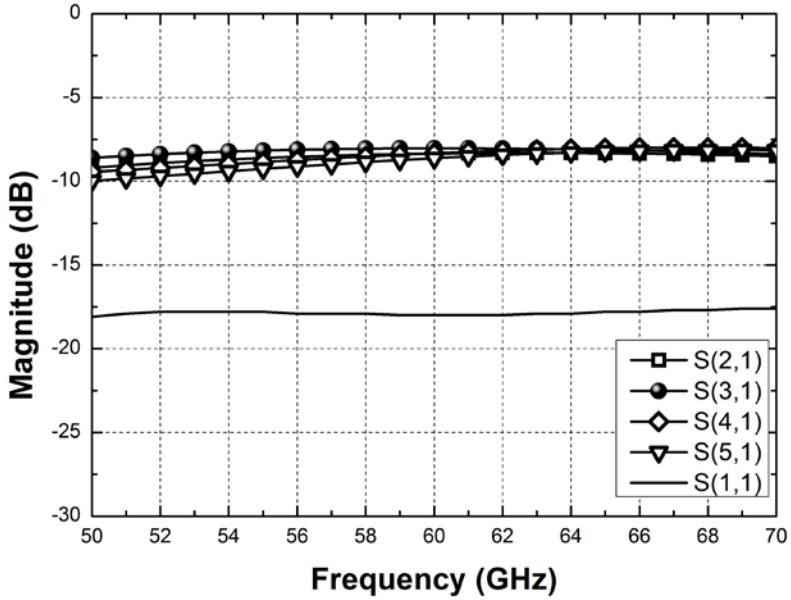
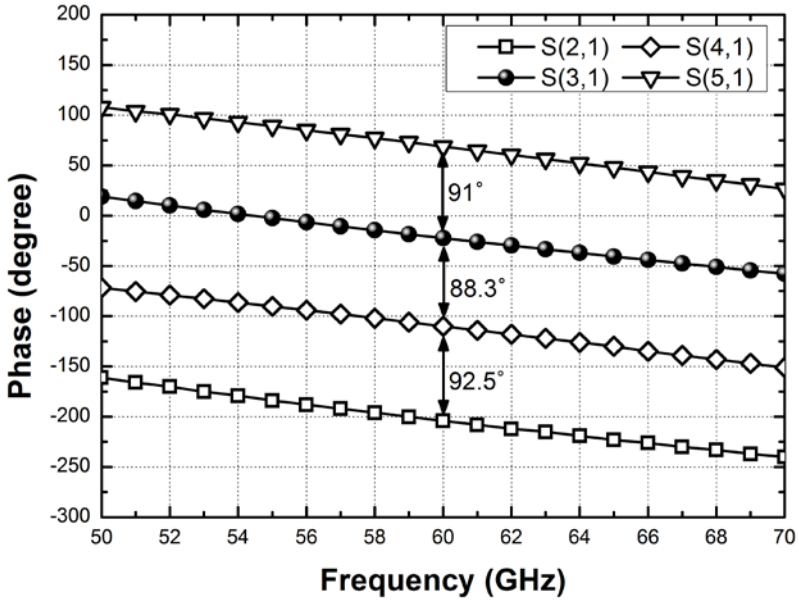


(a)



(b)

Fig. 3.16. Simulated (a) magnitude and (b) phase response of the vector generator.

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3.4.4.2 Vector Selector

The schematic of the proposed vector selector is shown in Fig. 3.17. A pair of double balanced switched pairs are adopted, which can ensure the input and output impedances of each state are the same. Therefore, the amplitude difference of each state will be minimized.

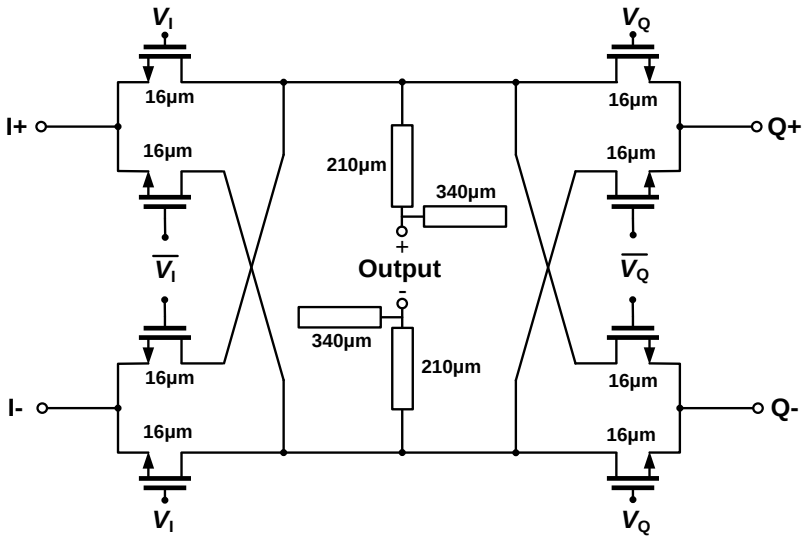

Fig. 3.17. Schematic of proposed vector selector

To achieve broadband response, the quadrature phase signals generated by vector generator enter the switching stage directly since the vector generator requires 50 Ω output loading. The size of transistor is selected to provide about 40-j*21 Ω load at each I/Q input. The switch controlled by V_I and V_Q can determine the phases of the signals. By using vector selector, the proposed phase shifter can achieve 90°, 180° and 270° phase shifts. The equivalent circuits of vector selector at 4 phase selection are shown in Fig. 3.18.

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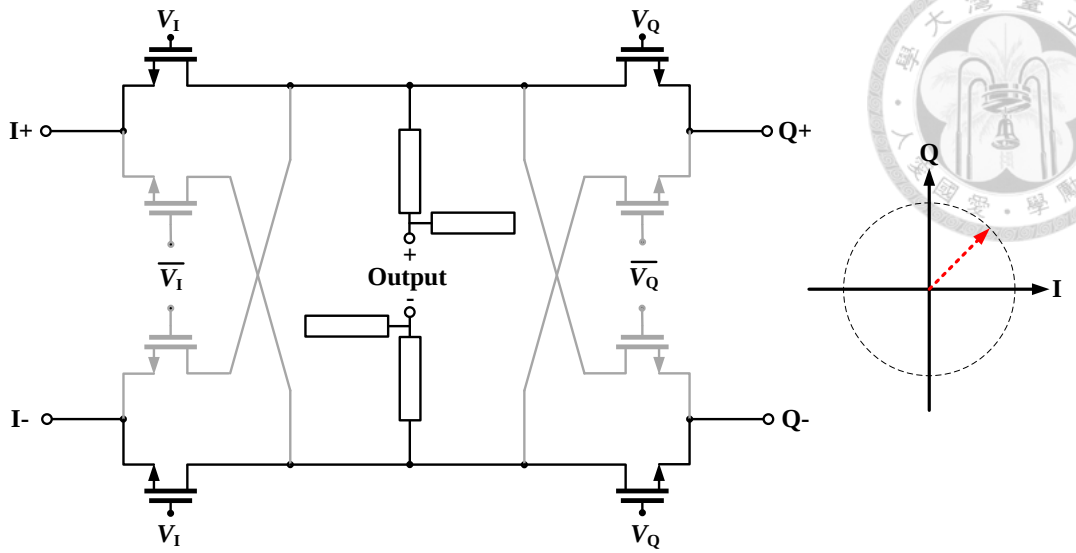

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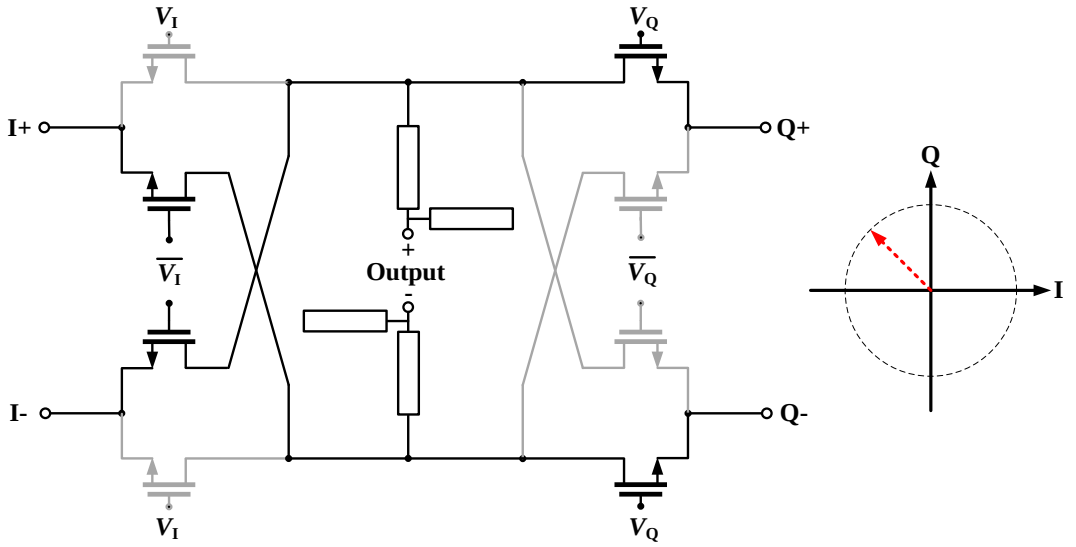

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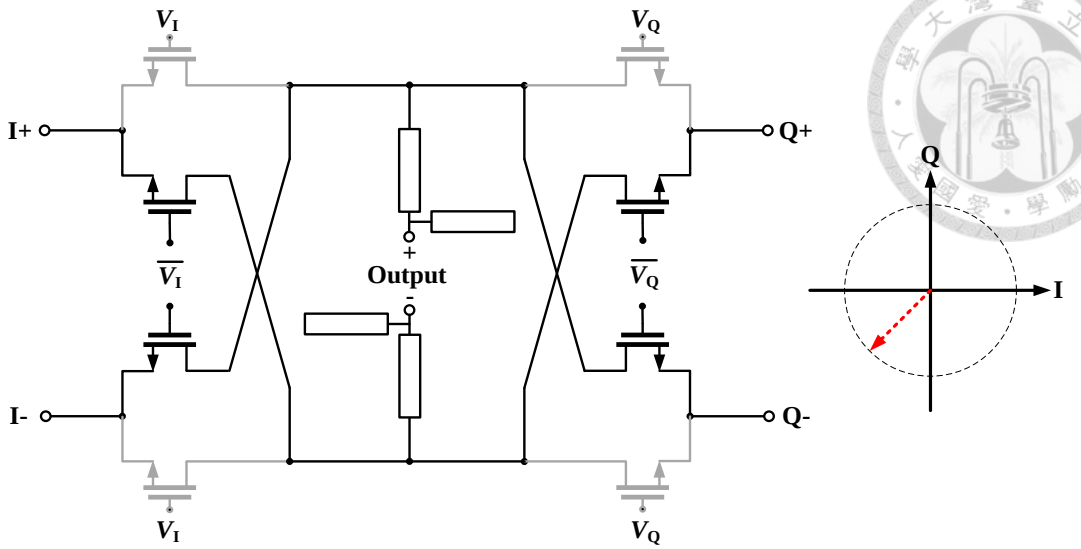

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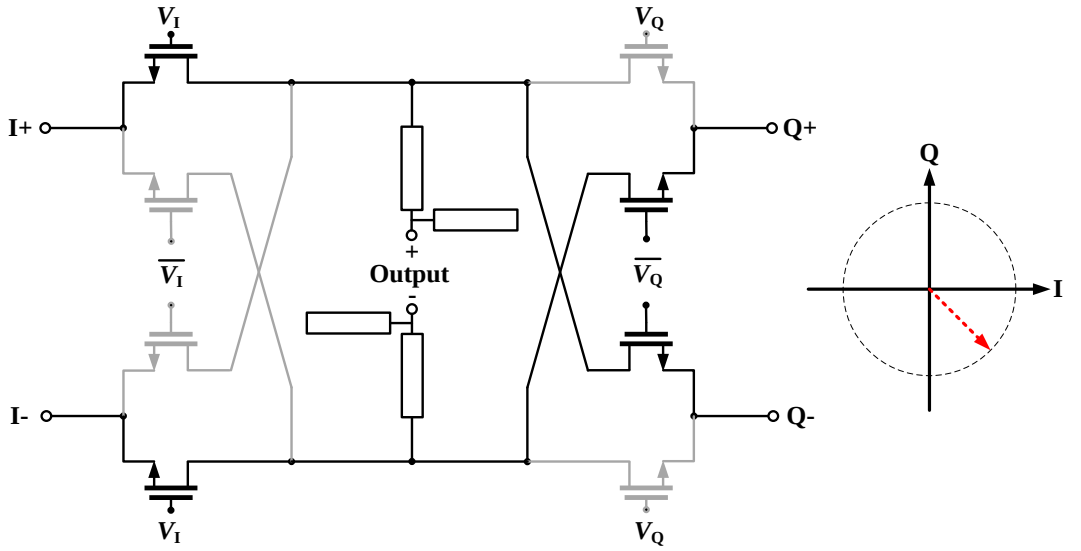

(d)

Fig. 3.18. Equivalent circuit of vector selector at 4 phase selection (a) first phase, (b) second phase, (c) third phase, and (d) fourth phase.

The transmission lines are used for impedance matching. After the switching stage, a Marchand balun is used to combine the output signal for measurement requirement (singe I/O). Due to the symmetric structure, the phase and amplitude error contributed

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by vector selector are smaller than those of STPS. Moreover, this vector selector consumes zero dc power and occupies small area. The simulated phase response and insertion loss of QPR at four phase states are shown in Fig. 3.19. It shows that the individual phase error is smaller than 3°. The insertion loss is 10.5±0.5 dB from 57 to 66 GHz. The theoretical insertion loss of QPR is 6 dB due to power division of vector generator. Both the extra insertion loss of vector generator and vector selector are about 2 dB. The QPR has lower loss than series STPS [56]. Besides, the proposed QPR is all passive so that it has high input dynamic range. The simulated input P_{1dB} is about 12 dBm.

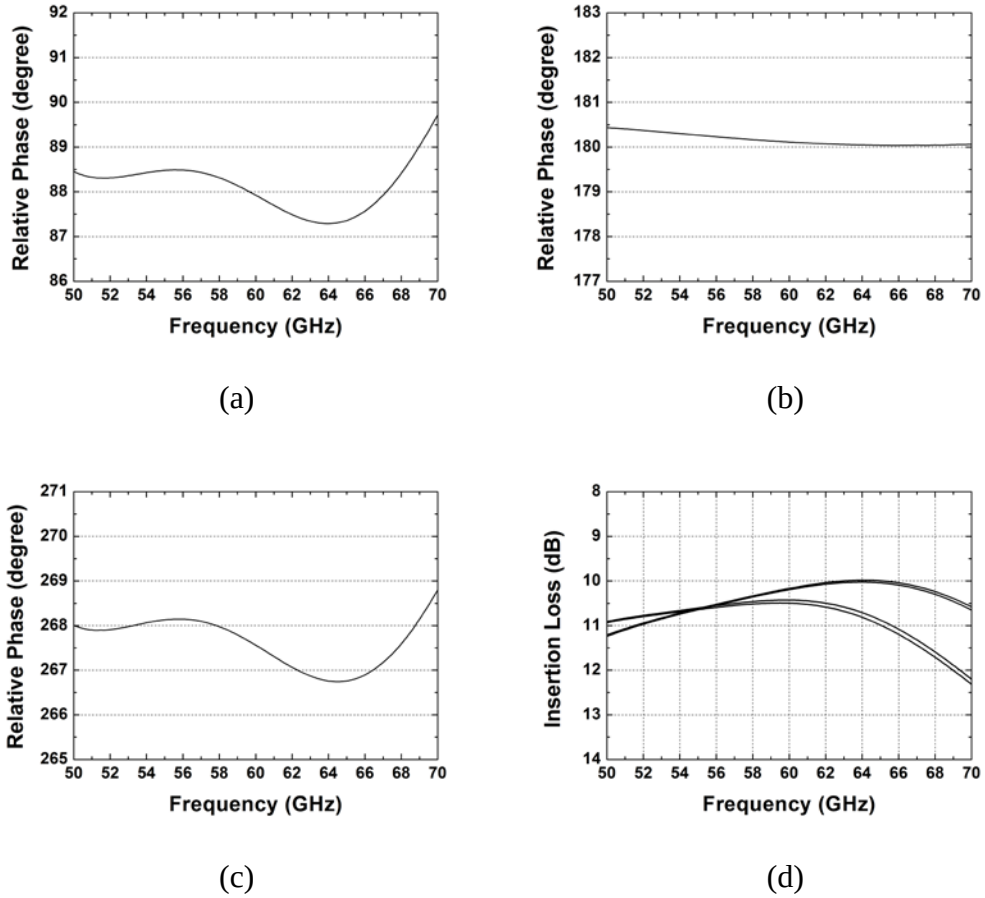

Fig. 3.19. Simulated relative phase of QPR: (a) 90° (b) 180° (c) 270°. (d) Simulated insertion loss of QPR.

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3.4.5 Measurement Results

The proposed phase shifter is fabricated in TSMC 90-nm CMOS technology. The chip photo is shown in Fig. 3.20, with a chip size of 0.45 × 0.68 mm^2 including all the pads, and the core size is 0.3 × 0.56 mm^2. This circuit is measured via on-wafer probing on input and output ports with the GSG probe. The S-parameter was measured by Agilent E8361A. The measured insertion loss of 16 phase states and RMS amplitude error are shown in Fig. 3.21. The average insertion loss is 17.5 dB at 60 GHz and the loss flatness is ±0.4 dB from 57 to 66 GHz. Thanks to using all passive structure and QPR, the phase shifter demonstrate very good loss flatness. Large degree STPS need large parasitic capacitance limited the high frequency response [27]. The RMS amplitude error is below 0.5 dB over 57-66 GHz. Fig. 3.22 shows the measured phase responses of 16 phase states with a resolution of 22.5°. It also shows that the measured RMS phase error is below 5° from 57 to 66 GHz. Table 3.3 summarizes the performance of previously reported MMW 360° phase shifter for the RF phased array. By using vector generator and vector selector, the proposed phase shifter has good performance in RMS phase and amplitude error. It also demonstrates the lowest loss flatness than other works. Therefore, The VGA is not required for loss compensation in the proposed phase shifter. Although the loss of this phase shifter is higher than other VSPS, this phase shifter consumes zero dc power and do not require extra DACs. These features are preferable in RF phased array with large number of channel.

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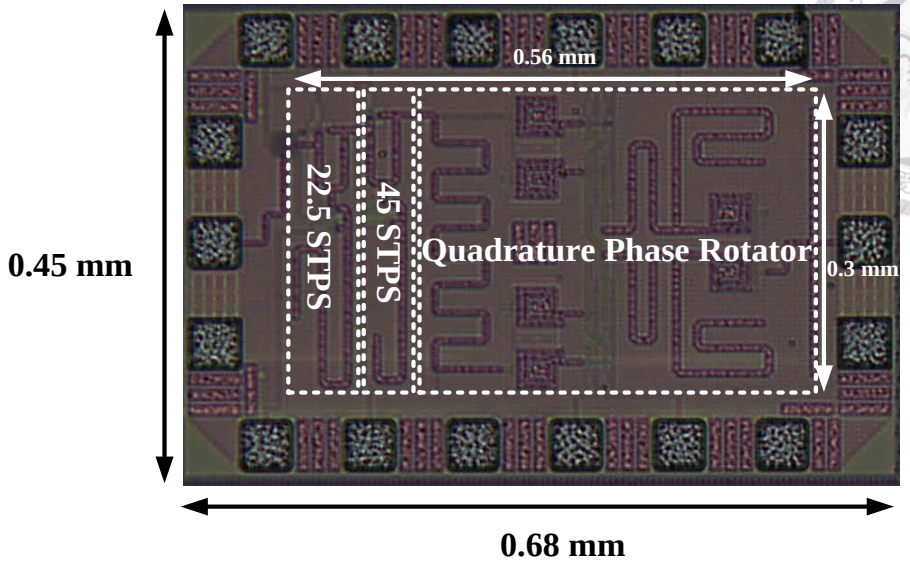

Fig. 3.20. Chip photo of 4 bit passive RF phase shifter

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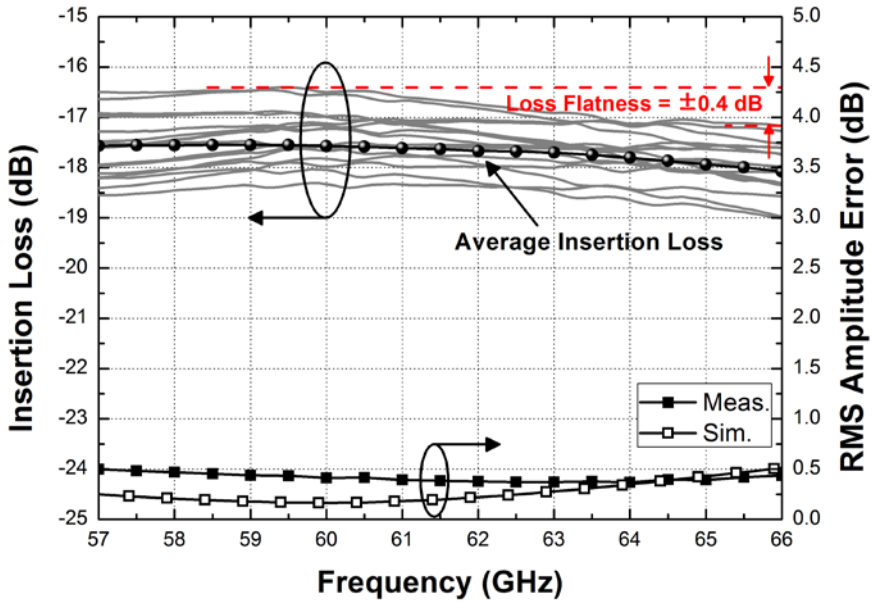

Fig. 3.21. Measured insertion loss (S_{21}) of 16 phase states and RMS amplitude error.

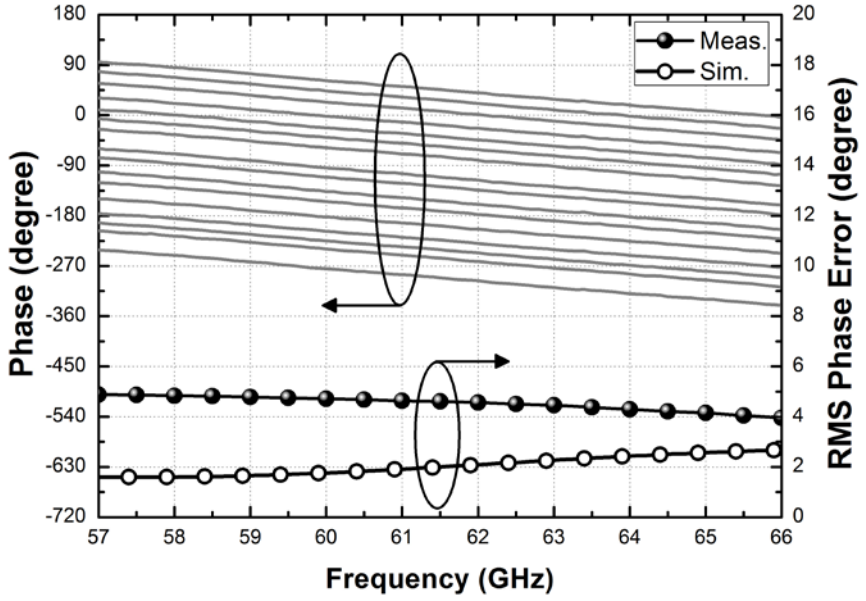

Fig. 3.22. Measured phase of 16 phase states and RMS phase error.

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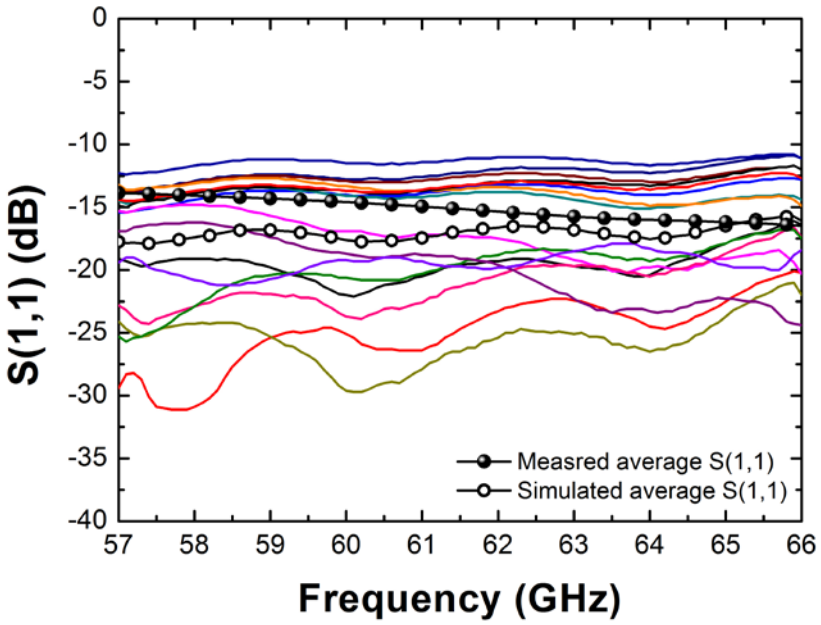

Fig. 3.23. Measured input return loss of 16 phase states

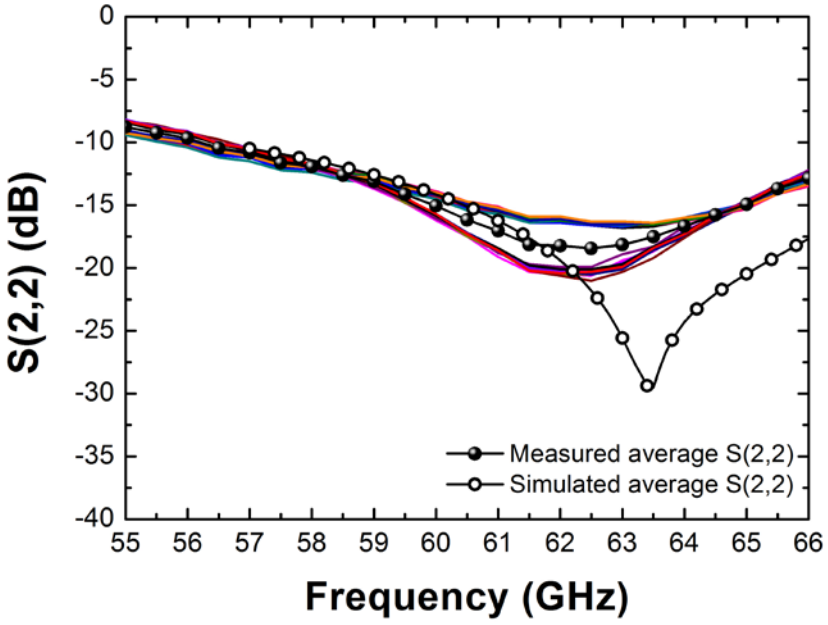

Fig. 3.24. Measured output return loss of 16 phase states

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Table 3.3. Comparison of published MMW RF phase shifters

Ref	[18]	[23]	[24]	[24]	[27]	[27]	[28]	[29]	**This Work**
Technology	0.13μm SiGe	90nm CMOS	90nm CMOS	45nm CMOS	90nm CMOS	90nm CMOS	0.13μm SiGe	65nm CMOS	90nm CMOS
Topology	VSPS	VSPS+ VGA	VSPS+ Amp.	VSPS	STPS	STPS +VGA	STPS	STPS	STPS +QPR
Frequency (GHz)	57-64	57-64	57-66	40-67	57-64	58-65	67-82	75-85	57-66
Phase Range (°)	360	360	360	360	360	360	360	360	360
Resolution (°)	11.25	22.5	22.5	22.5	11.25	11.25	22.5	22.5	22.5
Average Insertion Loss (dB)	2	5.4	4	7	17	5.4	19.2	25	17.5
Loss Flatness (dB)	N/A	±2.3*	±1*	±3.5*	±0.8	±0.8	±3.7*	±1.5*	±0.4
RMS amplitude Error (dB)	N/A	<0.8	<0.52	<1.2	<2.2	<2	<2.4	<1.8	<0.5
RMS Phase Error (°)	<5	<5.2	<5.1	<12	<10	<9.9	<10.8	<11.2	<5
Extra DAC Requirement	Yes	Yes	Yes	Yes	No	Yes	No	No	No
P_{DC}(mW)	32.4	34	15.6	23	0	31.2	0	0	0
Chip Size (mm^2)	0.56	0.66	0.315	0.51	0.34	0.58	0.135	0.135	0.168

*Estimated from measured data

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3.5 Injection-Locked Phase Shifter for 60-GHz LO Phased Array

3.5.1 Introduction

In recent years, a few LO phased arrays are proposed for beamforming system. To perform phase difference in each LO chain, the ring VCO which generates discrete multi-phase selected and distributed to each LO chain [57]. However, it cost significant area and power consumption. Furthermore, the phase resolution is limited by the number of phase of ring VCO. The VSPS was applied as LO phase shifter in LO chain to provide continuous phase shift, also inducing additional dc power [58]. Injection-locked phase shifter (ILPS) is adopted in LO phased array due to low power and higher linear phase tuning range [31]-[33]. The drawback of ILPS is small phase tuning range. To solve this issue, several ILPS cascade with multiplier have been presented to multiply the phase tuning range [31]-[33]. However, the multiplier may induce extra harmonic tones. Also, the phase noise is degraded by multiplied mechanism.

In this section, the ILPS is cascaded with QPR rather than multiplier. With QPR, this phase shifter achieves wider linear phase tuning range with smaller phase and amplitude error.

3.5.2 Phase shift of ILPS

When an oscillator is locked by injection signal, the output frequency is equal to input frequency, and tuning the self-oscillation frequency results in phase shift between

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input and output frequency. The phase difference of an ILO with an injection signal close to its elf-oscillation frequency are described by Adler's equation as [38]

$$\frac{d\phi}{dt} = \omega_0 - \omega_{\text{inj}} + \omega_{\text{L}} \sin\left(\phi_{\text{in}} - \phi\right) \tag{3.23}$$

where ω_{in}, ω_0 ,and ω_{L} are the input frequency, self-oscillation frequency and single sideband locking range of ILO, respectively. ϕ and ϕ_{in} are instantaneous phases of the oscillator and the injection signal. Under steady state ($d\phi/dt$ = 0), the phase difference between the oscillator and injection signal can be express as

$$\Delta\phi = \sin^{-1}\left(\frac{\omega_{\text{inj}} - \omega_0}{\omega_{\text{L}}}\right) \text{ (rad).} \tag{3.24}$$

Equation (3.24) indicates that the maximum phase shift is ±90° at the boundary of injection locking range ($\omega_{\text{inj}} = \omega_0 \pm \omega_{\text{L}}$). In the large phase shift region, the phase shift does not change linearly with ω_{in}. To find the maximum allowable linear phase tuning range, the phase deviation is defined as

$$\Delta\theta = \sin^{-1}\left(\frac{\omega_{\text{in}} - \omega_0}{\omega_{\text{L}}}\right) - \frac{\omega_{\text{in}} - \omega_0}{\omega_{\text{L}}} \text{ (rad).} \tag{3.25}$$

Fig. 3.25 plots the phase shift and phase deviation versus ω_{in}. The phase tuning of ILPS is continuous, the phase resolution is dependent on DAC resolution. To achieve 5 bit accuracy (11.25° phase resolution), $\Delta\theta$ should be smaller than 5.625°. Based on Fig. 9, the maximum allowable linear phase tuning range is within ±48° and the frequency tuning range also needs to exceed 1.5 × ω_{L}. With the QPR, the linear phase shift range can cover full 360°.

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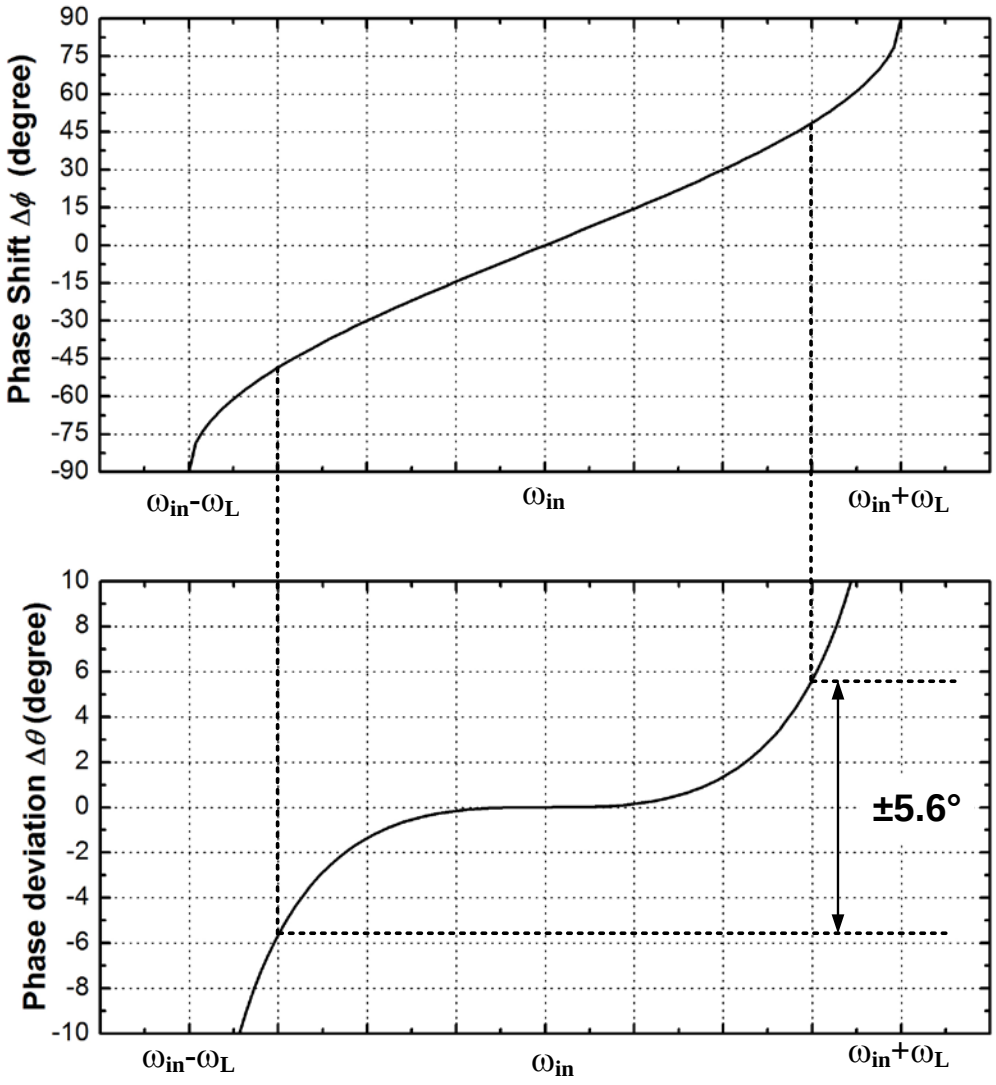

Fig. 3.25. Plot of the phase shift and phase deviation versus ω_{in}

3.5.3 Circuit Design

To demonstrate the phase shifting using ILO, a 60 GHz ILPS with the proposed QPR is designed and the circuit block diagram is shown in Fig. 3.26. The buffer amplifier is followed by ILPS to provide sufficient output power. The output of buffer is applied to proposed QPR described in section 3.4.4 to provide 360° phase shift.

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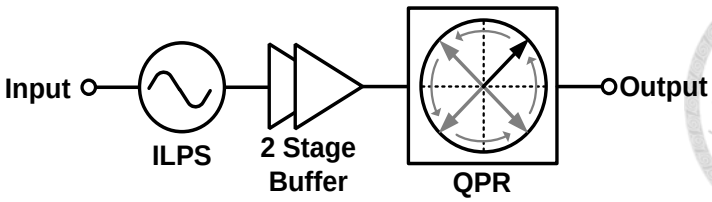

Fig. 3.26. Block diagram of proposed LO phase shifter.

The schematic of the ILPS is shown in Fig. 3.27. The cross-coupled pair transistors M_1 and M_2 provide negative transconductance to achieve self-oscillation. The oscillation frequency is tuned by varactors. The tuning range is designed from 57 to 65 GHz to cover the four channels of 58.32 GHz, 60.48 GHz, 62.64 GHz, and 64.8 GHz according to IEEE 802.15.3c standard [2]. The simulated tuning range of free-running ILO is shown in Fig. 3.28(a). The injection signal is applied via injection transistor M_3. To save the power consumption, the sizes of injection transistors are half of the cross-coupled pair transistors. The locking range of ILO can be express as [22]

$$\omega_{\mathrm{L}} = \frac{\omega_0}{2Q}\frac{I_{\mathrm{inj}}}{I_{\mathrm{osc}}} \tag{3.26}$$

where I_{inj} and I_{osc} are injection current and oscillation current, respectively. Q is the quality factor of LC tank. Thus, the desired locking range can be obtained by adjust the parameters $I_{\mathrm{inj}}/I_{\mathrm{osc}}$ and Q. The designed locking range is 3 GHz (single sideband locking range is 1.5 GHz), and the simulated locking range of ILO is shown in Fig. 3.28(b). Unlike ILFD, the locking range of ILO is not designed as wide as possible. As the matter of fact, for ILPS application, only if the designed locking range of ILO is covered by the frequency tuning range, the desired phase shift can be obtained. The proposed ILPS can achieve at least 90° phase shift in four channel's frequency. Phase shift characteristic can be obtained by observing time-domain waveform variation as the control voltage

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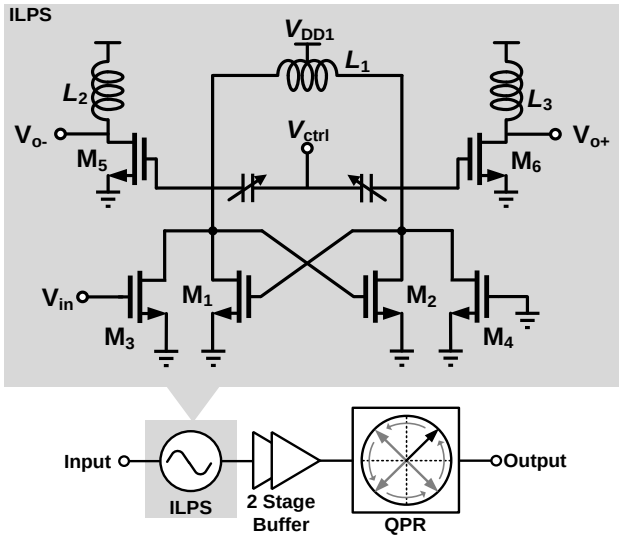
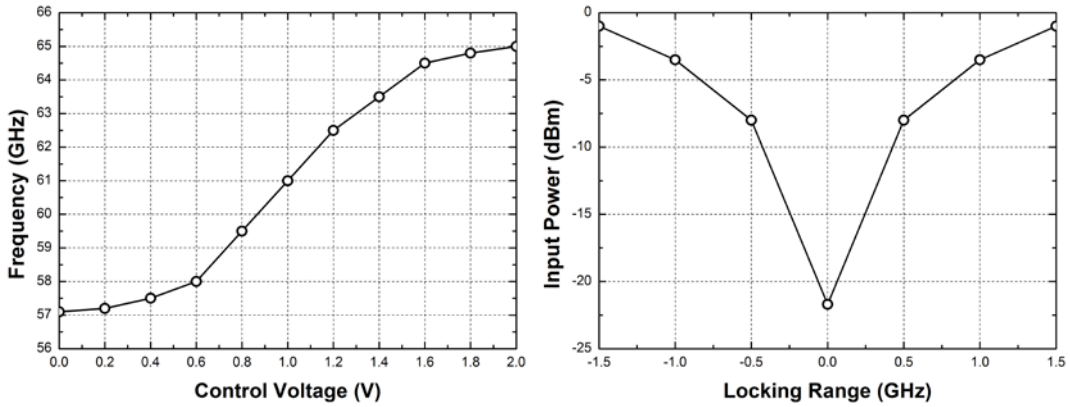
varied with fixed input frequency and power. The simulated results of time domain waveforms are shown in Fig. 3.29. The ILPS is locked to the injection signal with input power of -6 dBm at 62.64-GHz frequency, and the maximum phase shift is 90° with 2% amplitude variation.



	Value
M_1,M_2	16 μm
M_3,M_4	8 μm
M_5,M_6	16 μm
L_1	0.14 nH
L_2,L_3	0.12 nH

Fig. 3.27. Schematic of ILPS.



(a) (b)

Fig. 3.28. (a) Simulated free-running tuning range of ILO. (b) Simultedd locking range as ILO locked by input signal.

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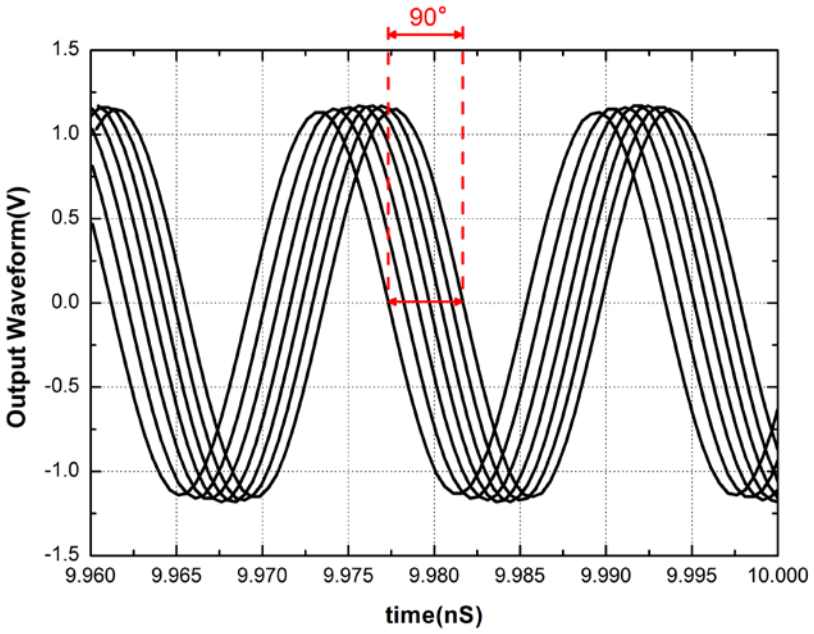

Fig. 3.29. Simulated output waveform of ILPS.

The buffer amplifier is designed using two stages of common-source amplifier as shown in Fig. 3.30. Both devices in the first stage and the second stage are selected 36 μm and biased with 6 mA from 1.2 V supply. The simulated S-parameter is shown in Fig. 3.31. Within the bandwidth, this amplifier can provide gain of 10 dB and output power of 0 dBm.

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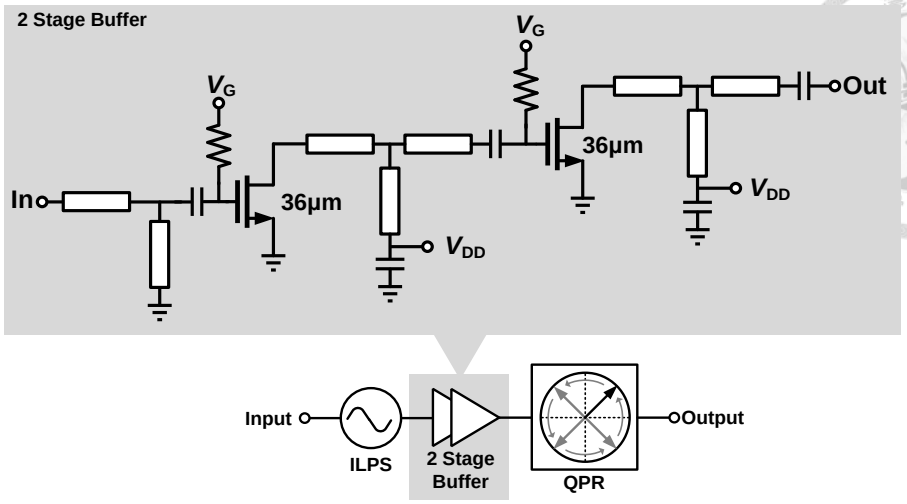

Fig. 3.30. Schematic of buffer amplifier.

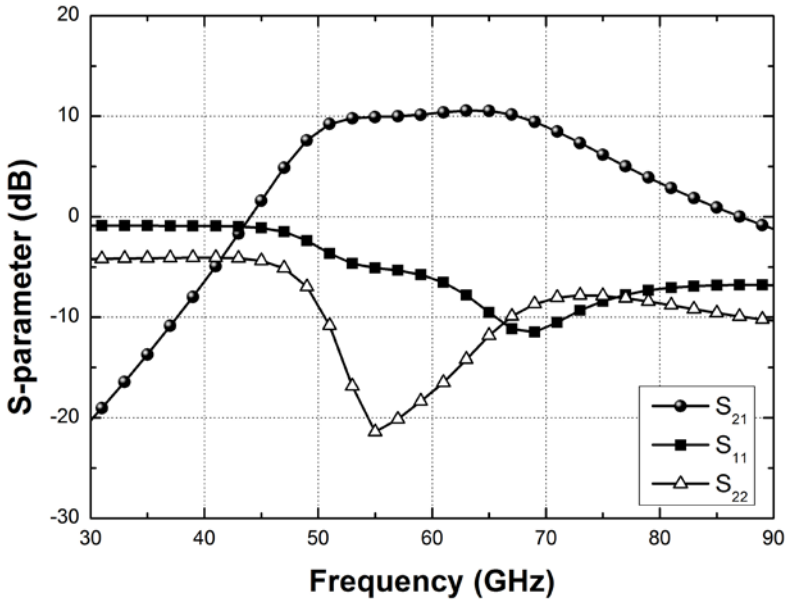

Fig. 3.31. Simulated S-parameter of buffer amplifier.

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3.5.4 Measurement Results

The chip photo is shown in Fig. 3.32, with a chip size of 0.5 × 0.92 mm^2 including all dc and RF pads, and the core size is 0.37 × 0.77 mm^2. This phase shifter is measured via on-wafer probing on input and output ports with the GSG probe. The injection signal is generated by signal generator Agilent E8257D. The spectrum analyzer Agilent E4448A with V-band preselected mixer Agilent 11974 V is used to measure the output oscillation frequency. Without injection signal, the measured tuning range of oscillator is shown in Fig. 3.33(a), and the oscillator has the tuning range from 59.1 GHz to 63.5 GHz. The measured output power is about -11±1 dBm in all oscillation frequency as shown in Fig. 3.33(b). With injection signal, the measured locking range of ILO is plotted in Fig. 3.33(c), and the ILO exhibited a locking range of 3 GHz with an injection power of 0 dBm.

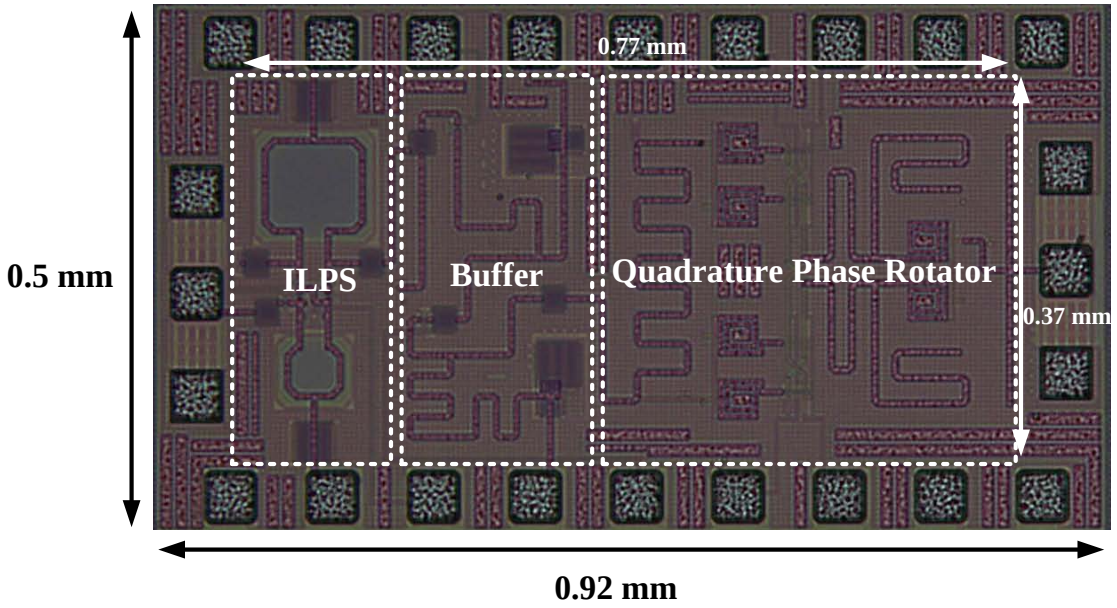

Fig. 3.32. Chip photo of proposed LO phase shifter.

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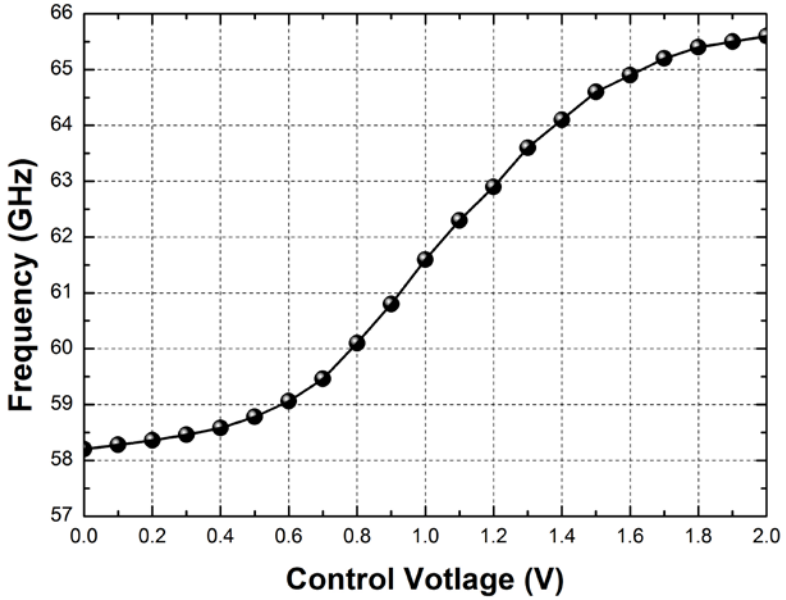
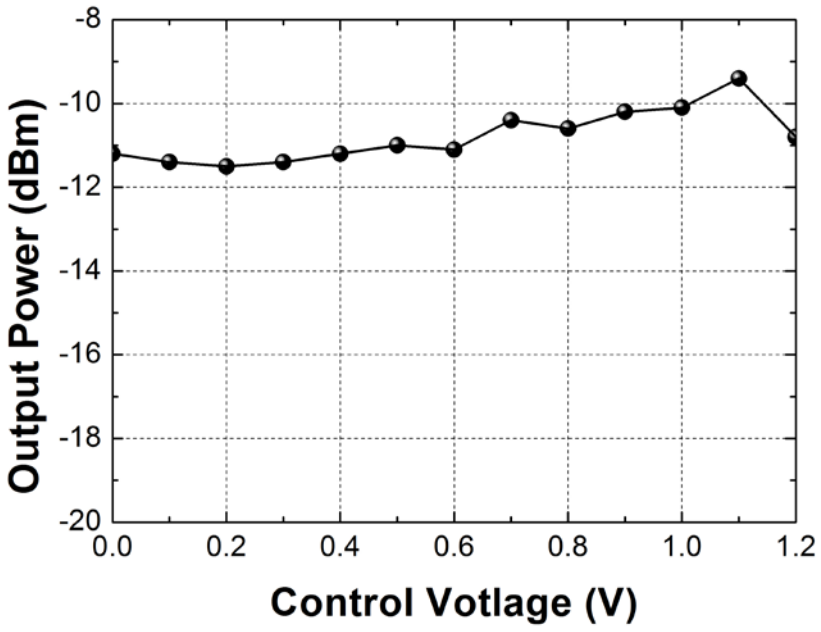


(a)



(b)

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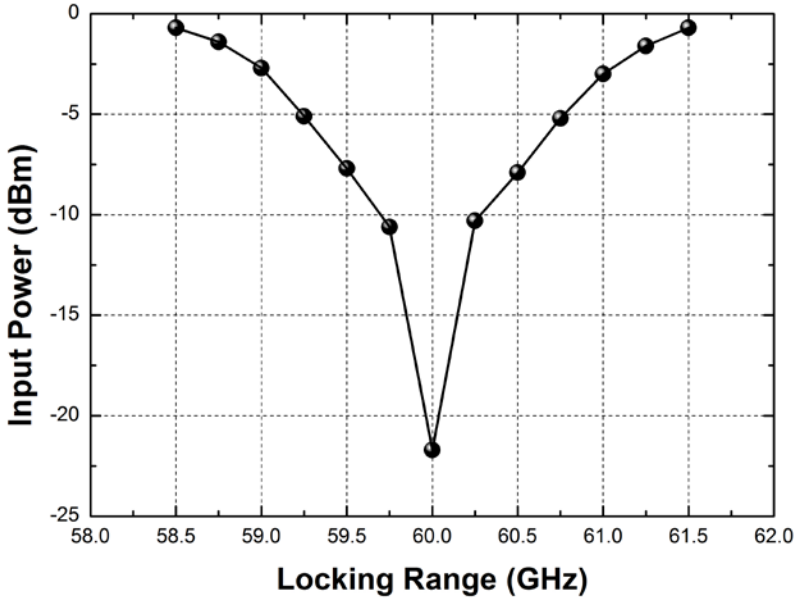

(c)

Fig. 3.33. (a) Measured free-running tuning range of ILO. (b) Measured output power of ILO(c) Measured locking range as ILO locked by input signal.

The phase shift measurement setup is shown in Fig. 3.34. The output locked signal and injection signal are both down-converted to lower frequency with two V-band mixers and captured by oscilloscope Agilent DSO 81304B. The phase shift characteristic can be obtained by observing the difference between two waveforms, and the extra calibration is not required. This characteristic exists as long as the frequency of injection signal is within the locking range. The measured output waveform is shown in Fig. 3.35 for -45° and 45° phase shifts controlled by tuning voltage V_{ctrl}. To observe the phase difference more easily, the amplitude of two signals are normalized. Measured phase shift at 60 GHz of two chips under 0-dBm injection power are shown in Fig. 3.36. 360° phase shift also can be attained at different frequency in two chips. Even though the locking ranges are different in different chips, the desired phase shift can be obtained by

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tuning oscillation frequency. Fig. 3.37 and Fig. 3.38 show the measured phase and amplitude error versus different phase shift, respectively. The maximum phase and amplitude error is smaller than 5° and 0.3 dB, respectively. The measured output power levels are -11 dBm in each phase state. Table 3.4 summarize the measured performance and compare with published LO-phase shifter. This phase shifter is the first multiplier-less ILPS over 60 GHz and can cover full 360° phase shift with low phase and amplitude error, owning to proposed QPR.

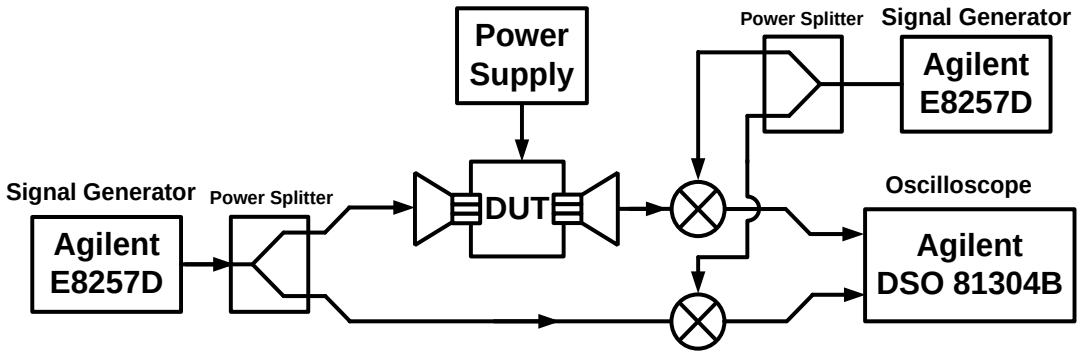

Fig. 3.34. Test setup for phase shift measurement.

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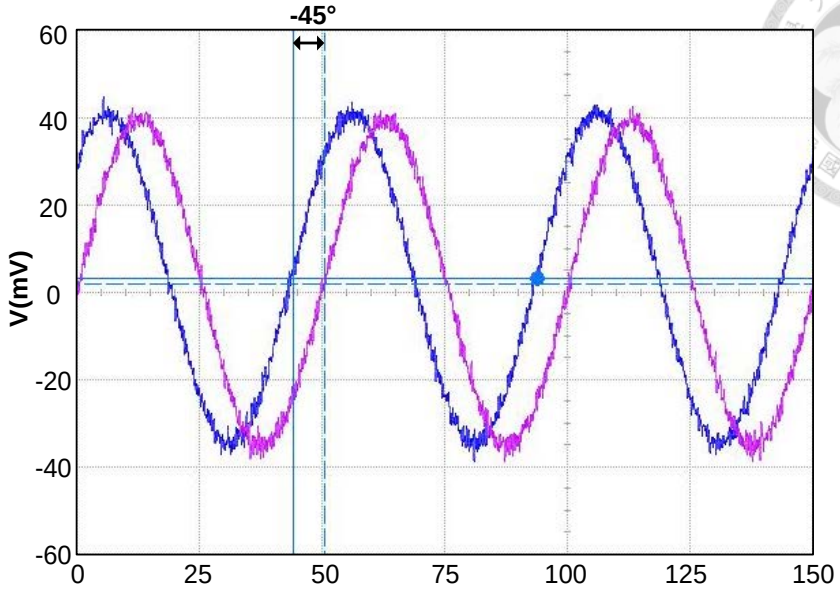
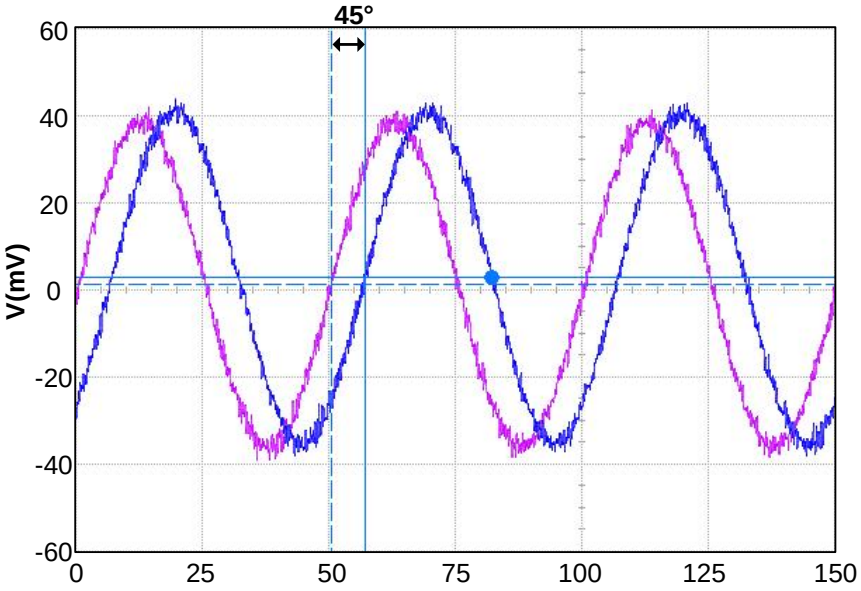


(a)



(b)

Fig. 3.35. Measured output waveform of proposed ILPS. (a) -45°. (b) 45°.

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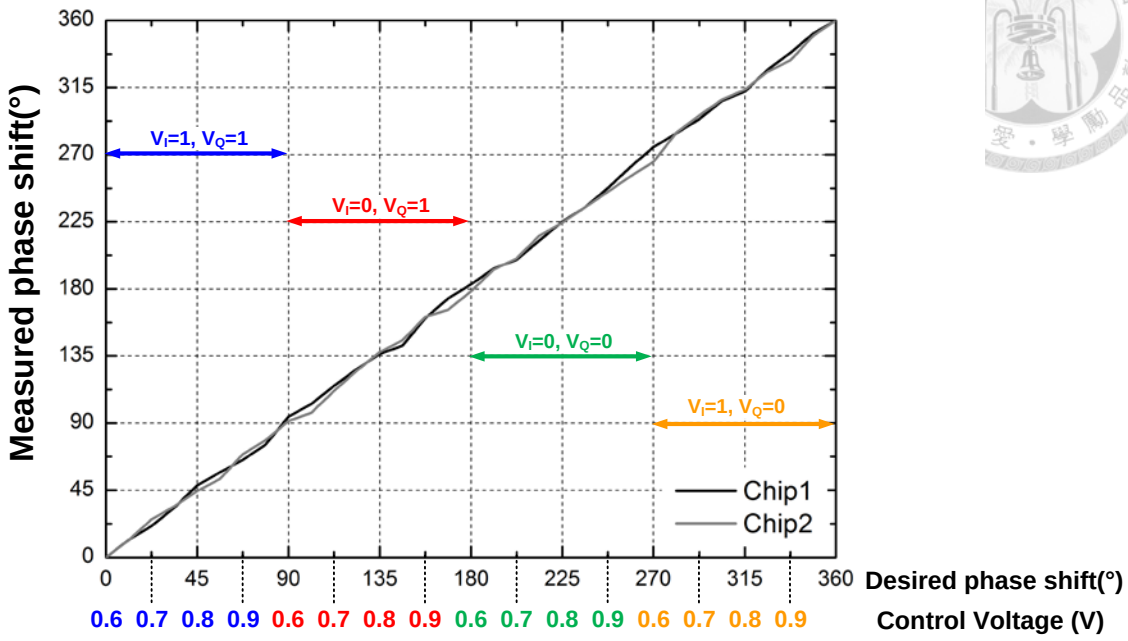

Fig. 3.36. Measured phase shift of proposed ILPS.

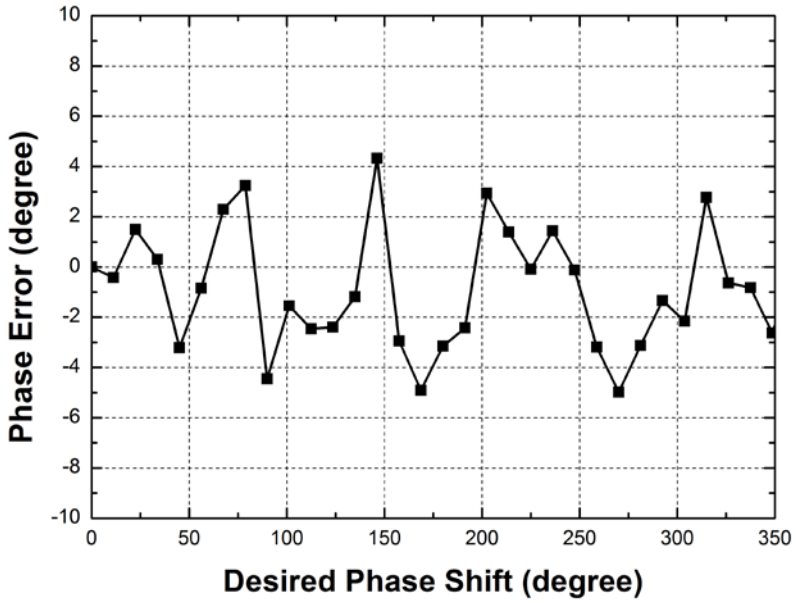

Fig. 3.37. Measured phase error of proposed ILPS.

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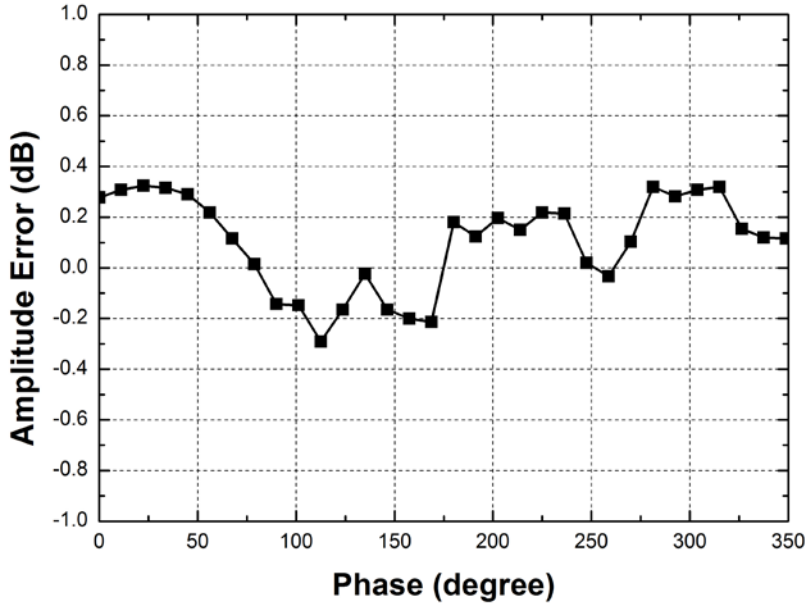

Fig. 3.38. Measured amplitude error of proposed ILPS.

Table 3.4. Comparison of published MMW LO phase shifters

Ref	[67]	[31]	[32]	[33]	**This Work**
Technology	130nm SiGe	65nm CMOS	90nm SiGe	90nm SiGe	90nm CMOS
Topology	Harmonic ILO	ILO + Tripler	ILO + Quadrupler	ILO + Quadrupler	ILO + QPR
Frequency (GHz)	24	42.7-49.5	57.2-61.4	62-72.8	58-65
Phase Range (°)	180	±90	±80	±300	360
Phase Error (°)	<4	<1.5	N/A	<5	<5
Amplitude Error (dB)	1.5	±0.35	N/A	0.4-0.9	±0.3
P_{DC}(mW)	24*	85**	117*	236**	18

*2 elements array
**4 elements array

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3.6 Summary

In this chapter, two phase shifters with low phase and amplitude error in 90 nm CMOS have been designed, fabricated and measured. The two phase shifters are based on STPS and ILPS, respectively. QPR included vector generator and passive vector selector is adopted in the two phase shifter to achieve 360° phase shift. The vector generator has broadband response and identical output impedance, and the passive vector selector is symmetric structure which results in low phase and amplitude error. The first phase shifter based on STPS demonstrates the maximum RMS amplitude error of 0.5 dB and phase error of 5°. This phase shifter also has the lowest loss flatness among the reported phase shifter in 60 GHz. Thus, the compensation by VGA is not needed. The second phase shifter based on ILO exhibits the maximum amplitude error of ±0.3 dB and phase error of 5°. Also, it is the first multiplier-less ILO phase shifter over 60 GHz and can cover full 360° phase shift. The two phase shifters occupy the size of 0.168 and 0.285 mm^2, respectively. Meanwhile, they show great potential for the integration with RF and LO phased array systems, respectively.

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Chapter 4 Conclusion

This dissertation consists of two main parts: The first part is design of wide bandwidth MMW frequency divider, and the second part is design of 60 GHz phase shifter with low phase and amplitude error.

In the first part, a 60 GHz Miller divider demonstrated in 65 nm CMOS, and a W-band ILFD is fabricated in 90 nm CMOS. The Miller divider achieves 57% input locking range from 35.7 to 64.2 GHz with power consumption of 1.6 mW owing to using weak inversion bias mixer. On the other hand, The STCO technique is proposed and utilized in ILFD and the operation frequency and locking range of the proposed ILFD can be increased without extra chip area and power consumption. The input locking range is 21.9% from 75.1 to 97 GHz at 0-dBm input power without any frequency tuning mechanism. The dc power consumption is 2.45 mW with a 0.7-V supply voltage. Both the proposed frequency dividers are suitable to integrate with low power MMW PLLs.

The second part is about phase shifter design for 60 GHz phased array system. Since there are different benefit in RF and LO phased array, individually, a RF phase shifter and a LO phase shifter are presented and fabricated in 90 nm CMOS. The QPR included vector generator and vector selector is proposed and applied in both phase shifter to achieve 360° phase shift with low phase and amplitude error. The proposed RF phase shifter based on STPS is all passive and fully digital control with 4 bit resolution. It demonstrates the maximum RMS amplitude error of 0.5 dB and phase error of 5°. Another proposed LO phase shifter based on ILPS exhibits the maximum amplitude error of ±0.3 dB and phase error of 5°. The output power of the proposed LO phase shifter

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is -10 dBm with 18 mW dc consumption. Both proposed phase shifters show great potential for integration with RF and LO phase array system, respectively.

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