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深空乏現象對超薄閘極氧化層金氧半電容元件光反應之影響

Deep Depletion Behavior in the Photoresponse of MOS Capacitors with Ultrathin Oxides

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THESIS

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摘要

本篇論文主要關注於超薄閘極氧化層金氧半電容元件之深空乏現象，為了深入瞭解此現象，引入各元件的光反應作為對照。首先，製造並加以量測具有簡單正方形圖案之金氧半電容元件。當少數載子的生成電流無法供給漏電流時，深空乏現象將會發生，且伴隨著閘極電流的飽和。側面不均勻性之加劇，如照光或氧化層厚度減少，均會強化邊緣電場，使得飽和電流更容易流經電容元件之邊緣。

接著，為了進一步探討邊緣區域的尺度，設計出變化邊緣相關參數之圖案。電極寬度大於10 μm，且電極間距為30 μm之元件的電容-電壓及電流-電壓曲線，與簡單正方形圖案的相近。然而，電極間距小於 20 μm，且電極寬度為 30 μm之元件的電流-電壓曲線，在電流飽和之過程中出現特別的過渡區；本文提出可能的解釋與圖例，認為此現象起因於兩臨近電極之邊緣空乏區耦合及少數載子共享。照光後，由於少數載子數量充足，此一過渡區將會消失。

Abstract

In this thesis, deep depletion behavior of MOS capacitors with ultrathin oxides is of major concern, while the photoresponse of each sample is also included for better understanding of this behavior. First, MOS capacitors with simple square patterns are fabricated and measured. Accompanied by saturation of gate current, deep depletion behavior occurs when the generation current of minority carriers fails to supply the leakage current. Enhancement of lateral nonuniformity such as illumination or decrease in oxide thickness intensifies the fringing field at edge and makes the saturation current pass through the edge of MOS capacitors more likely.

Subsequently, patterns with various changes in the edge-related parameters are designed so as to further recognize the approximate scales of edge regions. The capacitance-voltage and current-voltage curves of samples with electrode width lager than 10 μm and electrode separation of 30 μm are similar to those with simple square patterns. However, current-voltage curves of samples with electrode separation smaller than 20 μm and electrode width of 30 μm exhibit particular transition regions during the saturation of gate currents. Explanation and illustration are consequently proposed, supposing that the behavior originates from the coupling of edge depletion region and the sharing of minority charges between two adjacent electrodes. Under illumination, the transition regions disappear due to the abundant minority carriers.

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Chapter 1

Introduction

1-1 Motivation of This Work

The last half century is said to be the Age of Silicon because silicon ICs have changed human life enormously since Kilby and Noyce gave birth of the first integrated circuit in 1959 [1] - [2]. Innovative high-tech products such as portable media players, smartphones, or tablet PCs are introduced to the world more and more rapidly, and all of these are largely attributed to the improvement of semiconductor industry. Moore's law, the guideline of IC technology advancement, states that the number of transistors on a chip doubles every 18 to 24 months, as shown in Figure 1-1. Here is an analogy demonstrating how Moore's law works. In 1970, the number

of transistors in a microprocessor equals 2300, approximately the quantity of the audience of a music hall, while today this number has exploded to 1.3 billion, which is the population of China. The most astonishing part of Moore's law is that all the 1.3 billion transistors still occupy a chip size as the original one, just like those 1.3 billion people fit into the original music hall. Moore's law has been confirmed to be valid for 40 years, and it continues to exert its influence on every domain of semiconductor industry. According to the 2011 International Technology Roadmap for Semiconductors (ITRS), the scaling of effective oxide thickness (EOT) in silicon CMOS will reach below 0.8 nm in 2013. Aside from the manufacturing difficulty, MOS structures with this thin oxide possess different characteristics. Some behaviors, for example direct tunneling and deep depletion, which are insignificant while oxide is thick enough, become important and must be taken into consideration. In order to come to a better understanding of MOS structures with ultrathin oxide, simple MOS capacitors are fabricated and examined. In chapter 2 of this work, the photoresponse of the MOS capacitors are characterized from the aspect of C-V curve and I-V curve. Afterwards, MOS structure devices with particular patterns are designed for the purpose of identifying deep depletion behavior in chapter 3.

1-2 Ultrathin Oxide Prepared by Anodization

Anodization, or anodic oxidation, was first proposed by P. F. Schmidt and W.

Michel in 1957 [4], and this technique has been investigated through many researches since then [5] - [6]. Figure 1-2 illustrates the anodization system setup in this work. A silicon wafer, which serves as the anode, is placed in deionized (D.I.) water and connected to the positive terminal of a power supply. The cathode is a platinum plate, connected to the negative terminal of the supply. Then silicon oxide builds up gradually on the surface of the wafer until the power supply being turned off. Two factors, including the power supply intensity as well as spacing between the wafer and the platinum plate, determine the reaction rate of oxide growth, and thus are carefully selected. According to Ghandhi, the mechanism of anodization can be described below [7]:

1. In the beginning, D.I. water, the electrolyte, is dissociated into H^+ and $(OH)^-$ ions:

$$2H_2O \leftrightarrow 2H^+ + 2(OH)^- \tag{1-1}$$

2. The difference in electrochemical potentials between the silicon substrate and the D.I. water results in charge transfer from the silicon until equilibrium is accomplished. Therefore, the surface layer is partially depleted of electrons and holes are supplied from the bulk of silicon to the silicon-electrolyte interfaces during anodization. The silicon atoms on the substrate surface are thus promoted to a higher oxidation state:

$$Si + 2h^+ \rightarrow Si^{2+} \tag{1-2}$$

3. The Si^{2+} combines with $(OH)^-$ to form the hydroxide.

$$Si^{2+} + 2(OH)^- \rightarrow Si(OH)_2 \quad (1\text{-}3)$$

4. $Si(OH)_2$ subsequently forms SiO_2, together with hydrogen molecule.

$$Si(OH)_2 \rightarrow SiO_2 + H_2 \quad (1\text{-}4)$$

The overall reaction is as follows:

$$Si + 2h^+ + 2H_2O \rightarrow SiO_2 + 2H^+ + H_2 \quad (1\text{-}5)$$

In addition, in 1992, H. J. Lewerenz hypothesized that the formation of anodic oxides is composed of the following reactions [8]:

$$Si + H_2O + h^+ \rightarrow SiOH + H^+ \quad (1\text{-}6)$$

$$2SiOH \rightarrow Si_2O + H_2O \quad (1\text{-}7)$$

$$2Si_2O \rightarrow SiO_2 + 3Si \quad (1\text{-}8)$$

The overall oxidation reaction is shown below:

$$Si + H_2O + 4h^+ \rightarrow SiO_2 + 4H^+ \quad (1\text{-}9)$$

Anodization is adopted as the ultrathin oxide growth technique because it has several distinct advantages. As mentioned above, oxide thickness can be controlled precisely by varying the duration and voltage of the power supply. Besides, the process is very simple and time-efficient, whereas its low temperature characteristic enables the impurity profile of the wafer to stay constant. Last but not least, the oxide

prepared by anodization possesses good dielectric quality and low leakage current, therefore is suitable to be the gate oxide [9].

1-3 Experimental Setup and Measurement Systems

In this work, all of the MOS structure devices are fabricated in a similar way. Figure 1-3 demonstrates the flowchart of the fabrication processes. First, 3-inch boron-doped p-type (100) silicon wafers with the resistivity of 1-10 Ω-cm were used as the substrates. After performing the standard RCA cleaning to eliminate organic particles as well as ionic contaminants, the native thin oxide layers were removed by a short immersion in a diluted HF solution [10]. Next, ultrathin gate oxides were grown on the silicon substrates by anodization in D.I. water. Direct-current voltage of 15 V was applied between the wafer and the platinum plate for 8 minutes. In order to obtain different oxide thicknesses on one wafer, the platinum cathode was tilted, making the spacing between the cathode and the anode to be 2 units in minimum and 6 units in maximum. Each unit equals to 5 mm approximately. Subsequently, post-oxidation annealing (POA) was implemented in 20 torr, N_2 ambient at 950℃ for 15 seconds, with the aid of an ARTS 100 rapid thermal process. The temperature setting profile is shown in Figure 1-4. High purity aluminum was later evaporated on the oxide by a DAH YOUNG DMC-400 high vacuum coater and the 3000-Å aluminum film serves as the metal gate of MOS capacitors. Afterwards, conventional photolithography was

carried out, by the use of an SUSS MJB4 mask aligner, to define the required electrode patterns. Finally, removal of the back oxide was performed with buffered oxide etchant (BOE), followed by aluminum evaporation to make up the back contacts.

After the devices fabrication, all of the high-frequency capacitance-voltage (C-V) characteristics were measured by an Agilent 4284A precision LCR meter, while the current-voltage (I-V) characteristics were measured by an HP 4140B picoampere meter [11]. Both capacitance-voltage and current-voltage characteristics under illumination were examined with the aid of an incandescent lamp, whose irrandiance was measured by a Newport 841-PE power meter.

1-4 Determination of Ultrathin Oxide Thickness

Conventionally, optical ellipsometers are commonly used to distinguish film thickness, providing an accuracy of a few angstroms. However, when the thickness of gate oxide scales down to an ultrathin level, a suitable measurement technique must possess the capability to identify the subtle differences between one angstrom or even smaller. A much simpler and effective alternative is achieved by analyzing the capacitance-voltage characteristics of MOS devices.

When a MOS capacitor stays in accumulation mode, its total capacitance approximates to its gate oxide capacitance. Hence, the oxide thickness can be

obtained by eq. (1-10), where A is the area of the MOS capacitor, ϵ_{OX} is the permittivity of SiO_2, and t_{OX} is the thickness of the oxide layer.

$$C_{total}(acc) \cong C_{OX} = A\frac{\epsilon_{OX}}{t_{OX}} \tag{1-10}$$

As oxide thickness is reduced, new problems arise from the exponentially increasing gate leakage current due to direct tunneling. In order to eliminate the leakage problem, capacitance-voltage curves are measured at high frequencies so that capacitive currents are dominant. A two-frequency correction technique based on a three-element equivalent circuit of MOS capacitors has been proposed by K. J. Yang and C. Hu to extract the ultrathin oxide thickness accurately [12]. The circuit models are shown in Figure 1-5, where C is the actual capacitance, R_P is the effective resistance due to oxide leakage current, and R_S is the series resistance of the substrate and the gate. The total impedance of the circuit model can be derived as eq. (1-11).

$$Z = R_S + \frac{R_P\left(1 - j\omega CR_P\right)}{1 + \omega^2 C^2 R_P^2} \tag{1-11}$$

On the other hand, the measured impedance of the circuit model, in which values of respective elements are measurable under parallel mode, is given by eq. (1-12).

$$Z = \frac{D' - j}{\omega C'\left(1 + D'^2\right)} \tag{1-12}$$

where $D' = \frac{1}{\omega R' C'}$ is the dissipation, and R' and C' are measured values. Equating the imaginary part of the above two impedance, one obtains

$$\frac{1+\omega^2 C^2 R_P^2}{C R_P^2} = \omega^2 C'\left(1+D'^2\right) \tag{1-13}$$

Substituting the capacitance and dissipation measured at two different frequencies into eq. (1-13), one can derive the actual capacitance as

$$C = \frac{f_1^2 C'_1\left(1+D'^2_1\right) - f_2^2 C'_2\left(1+D'^2_2\right)}{f_1^2 - f_2^2} \tag{1-14}$$

where C'_1 and D'_1 refer to the values measured at the frequency of f_1 while C'_2 and D'_2 refer to the values measured at the frequency of f_2.

After obtaining the actual capacitance value of MOS capacitors, one should also take account of the quantum mechanical effect when determining the ultrathin oxide thickness. In this work, we use a quantum mechanical capacitance-voltage simulator as developed by K. Yang, Y. C. King, and C. Hu [13] - [14]. In this way, the displacement of the wave function peak of inversion charges is appropriately considered, and the extracted thickness won't be overestimated.

1-5 Deep Depletion Behavior in Capacitance-Voltage Curve

In ideal conditions, the total capacitance C_{total} of a MOS capacitor can be regarded as the oxide capacitance C_{OX} in series with the semiconductor capacitance

C_S as eq. (1-15)

$$\frac{1}{C_{total}} = \frac{1}{C_{OX}} + \frac{1}{C_S} \tag{1-15}$$

When the MOS capacitor is operated under depletion mode, for example, a positive voltage drops on the semiconductor part of a MOS(p) capacitor, acceptor atoms near the oxide-semiconductor surface are ionized in order to maintain charge neutrality and thus a depletion region is induced. The total high frequency capacitance C_{HF} can be further derived as eq. (1-16) because C_S is relatively smaller than C_{OX}.

$$C_{HF}(dep) \cong C_S = A\frac{\epsilon_S}{W} \tag{1-16}$$

where A is the area of the MOS capacitor, ϵ_S is the permittivity of the semiconductor, and W is the width of the depletion region. The depletion width expands with the increasing voltage drop until the MOS capacitor enters inversion mode, in which the minority carriers form an inversion layer. At high frequency, the minority carriers have no influence on C_{HF} due to the slow response time. As a result, the depletion width reaches a maximum, while both C_S and C_{HF} stay constant at their minimum.

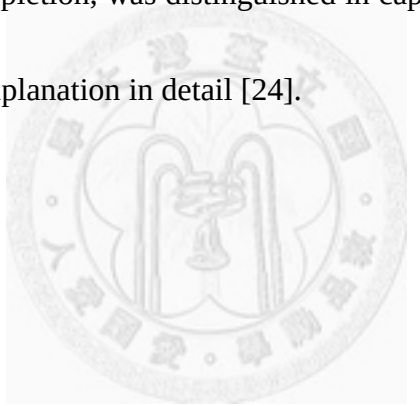
Conventional deep depletion can be observed when a ramp voltage on an MOS capacitor sweeps too fast in the direction from accumulation towards inversion [15] - [16]. At a high sweep speed, generation of minority carriers cannot follow up the change rate of gate bias. In order to maintain charge neutrality, the depletion region

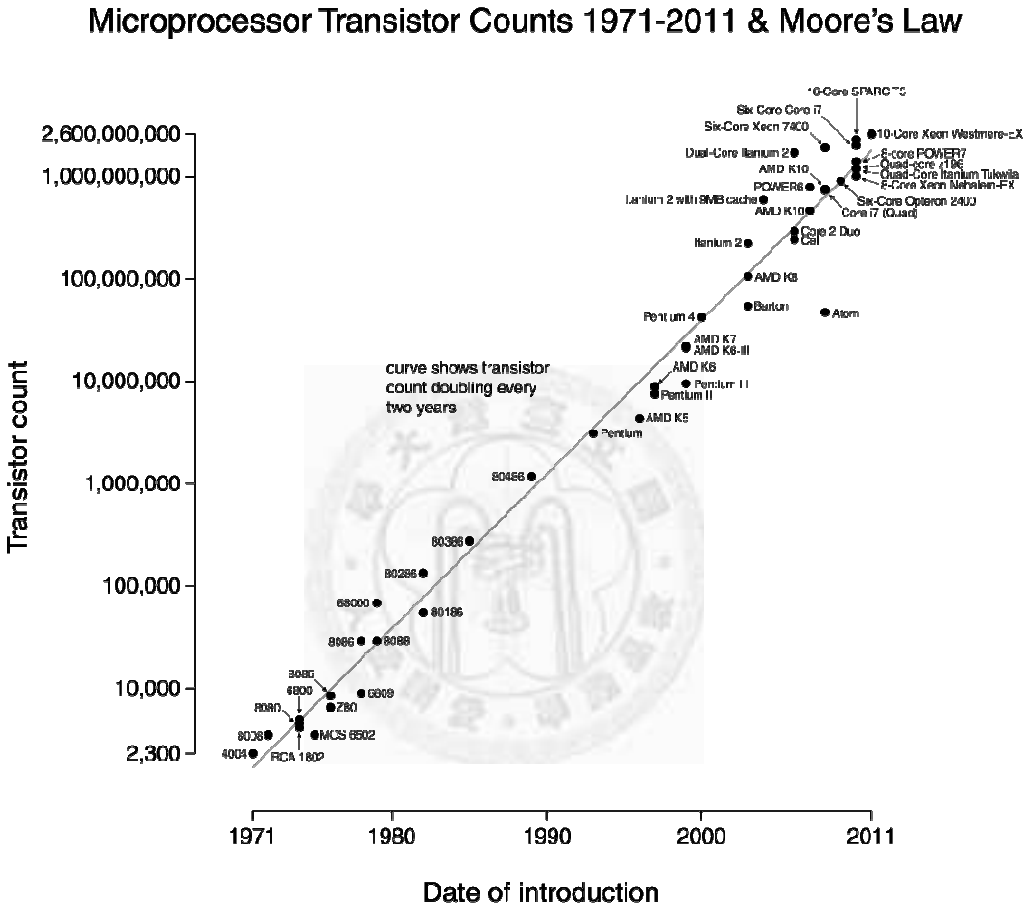
expands broader than in thermal equilibrium, and thus C_S as well as C_{HF} decreases below its minimum value. More importantly, the conventional deep depletion is a nonequilibrium behavior. If the ramp voltage stops sweeping, minority carriers will generate gradually, and the depletion region will shrink to the original width as in equilibrium.

On the contrary, another kind of deep depletion behavior is discussed in this thesis. For MOS capacitors with ultrathin oxides, high gate leakage currents in depletion mode result in a lack of minority carriers. In order to maintain current continuity, the depletion region widens and thus the capacitance-voltage curve shows the deep-depletion characteristics [17] - [19]. This kind of deep depletion is a steady-state phenomenon, and is independent of the sweep speed. Besides, it is the high tunneling current that leads the lack of minority carriers, not the slow generation rate as in conventional deep depletion.

Recent works presented some characteristics of the tunneling-induced deep depletion behavior in MOS capacitors. In capacitance-voltage plots, initiation of deep depletion can be clearly identified by a turning point between a constant value and a subsequently decreasing curve; however, if the oxide thickness is around 25 Å or below, the tunneling current will become so large that the constant value of capacitance will not exist [20]. Later, calculation between increments of gate voltage,

depletion width and inversion tunneling current was demonstrated in order to prove the relation of deep depletion and inversion tunneling current [21]. With the aid of scanning capacitance microscopy (SCM), deeper depletion width in certain local area was observed, revealing the concept of local depletion capacitance (LDC) [22]. Based on LDC, lateral nonuniformity due to local charged defects was further included to explain why the initiation voltage of deep depletion increases with oxide thickness [23]. Finally, different stages of deep depletion, depletion-inversion, edge deep depletion and bulk deep depletion, was distinguished in capacitance-voltage curves of MOS capacitors with an explanation in detail [24].




Microprocessor Transistor Counts 1971-2011 & Moore's Law
Transistor count
2,600,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300
curve shows transistor count doubling every two years
Six Core Core i7
Six-Core Xeon 7400
Dual-Core Itanium 2
AMD K10
POWER6
Itanium 2 with 9MB cache
AMD K10
Core i7 (Quad)
Six-Core Opteron 2400
Core 2 Duo
Cell
Itanium 2
AMD K8
Pentium 4
Barton
Atom
AMD K7
AMD K6-III
AMD K6
Pentium II
AMD K5
Pentium
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RCA 1802
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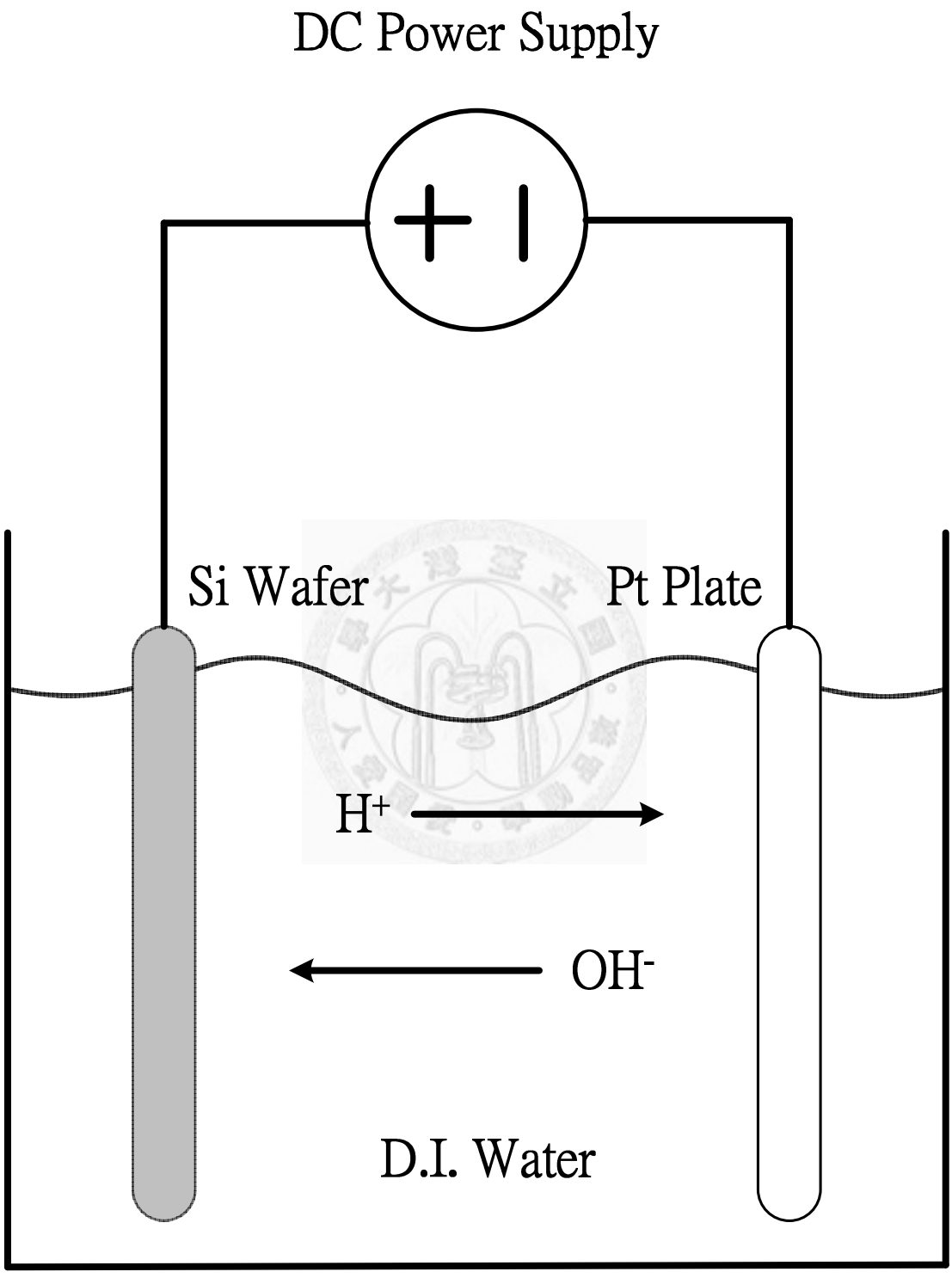


Figure 1-2 The schematic diagram for the anodization (ANO) system.

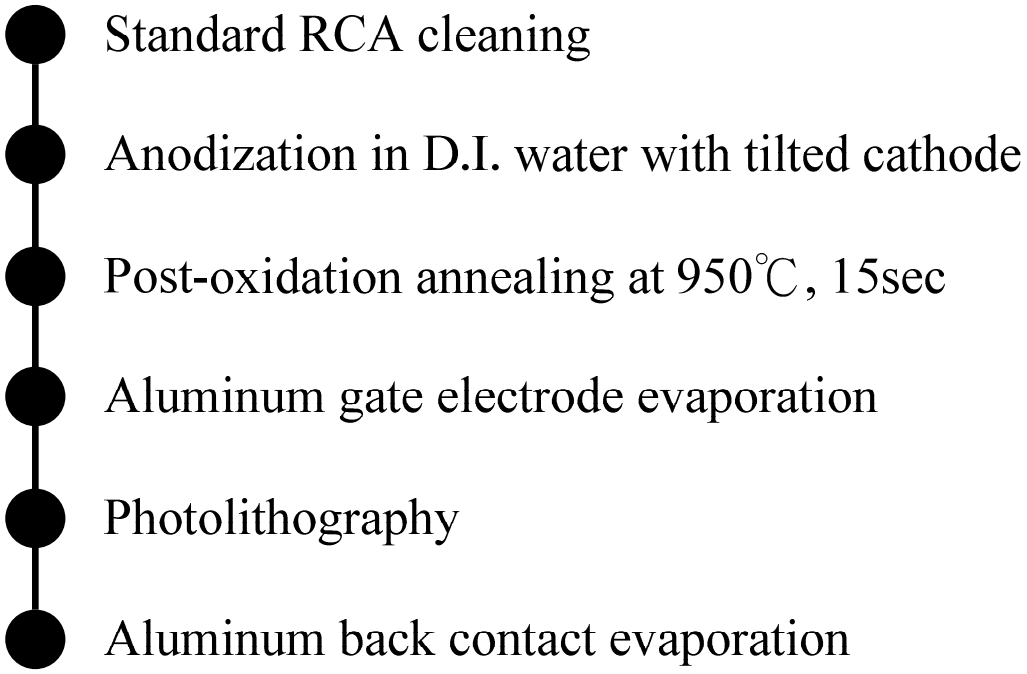


Figure 1-3 Fabrication flows of MOS capacitors.

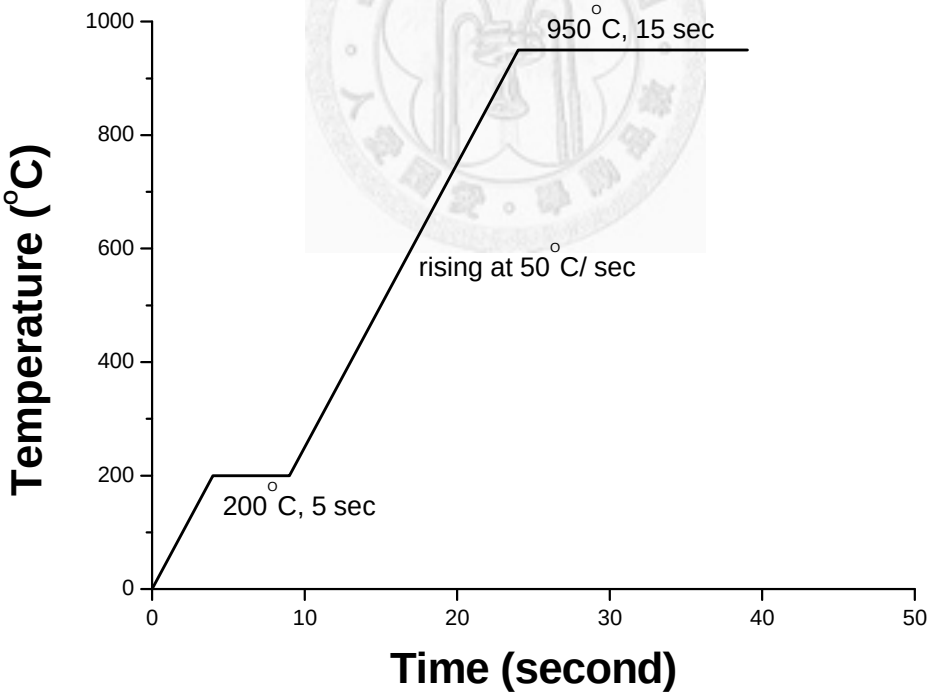


Figure 1-4 The temperature setting profile of RTP.

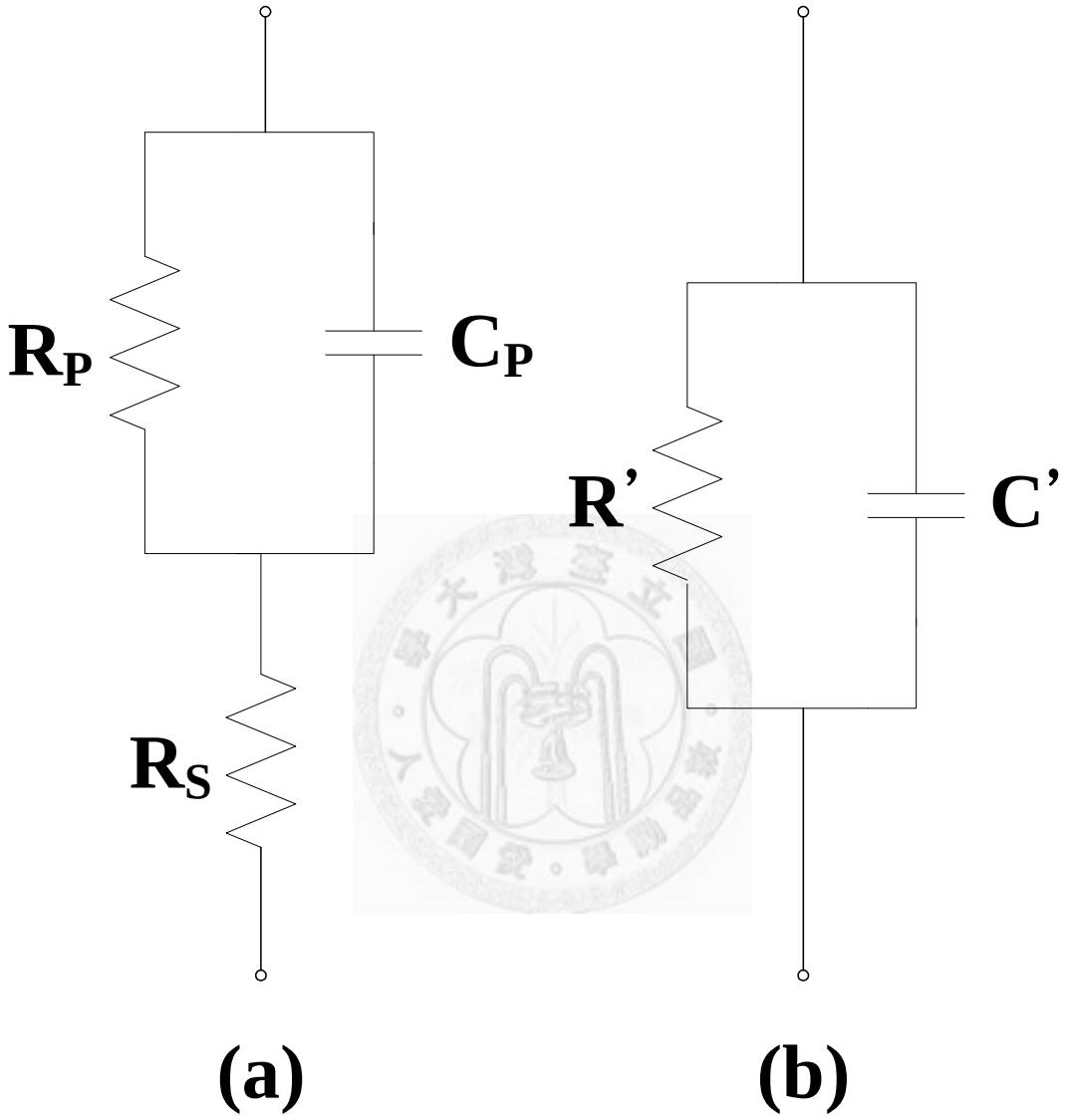


Figure 1-5 Small signal equivalent circuit models of MOS capacitors: (a) accurate model, (b) parallel circuit model for low series resistance devices.

Chapter 2

Fundamental Characteristics of MOS Structures

2-1 Introduction

In this chapter, we will discuss several fundamental characteristics of MOS capacitors with ultrathin oxides, especially those related to deep depletion behavior. First, saturation of gate current is a phenomenon in current-voltage characteristics corresponding to deep depletion behavior, proved to be relevant to the long generation time of minority carrier [21]. The lateral nonuniformity issue will also be included for

discovering more about the saturation current.

Furthermore, according to previous literature, initiation of deep depletion is related to the oxide thickness, and may serve as a basis when determining the qualities of dielectrics [23]. A typical deep depletion phenomenon of high-frequency capacitance-voltage characteristic of MOS capacitor with oxide thicker than 25 Å is shown in Figure 2-1. However, as the oxide thickness keeps decreasing, the deep depletion phenomenon does not exhibit an obvious initiation. Both the capacitance-voltage and current-voltage characteristics of MOS capacitors with ultrathin oxides will be examined with the aid of photo excitation.

For simplicity, the MOS capacitors studied in this chapter are defined as square patterns with three different sizes, 150 μm × 150 μm, 300 μm × 300 μm, and 600 μm × 600 μm. The cross sections are illustrated in Figure 2-2.

2-2 Correlation Between Deep Depletion Behavior and Saturation Current

In MOS capacitors with ultrathin oxides, the saturation of gate currents can be perceived after the substrate is strongly depleted, for example, a MOS(p) capacitor under positive bias. Unlike a gate injection current, whose carriers are abundant from the metal, this saturation current is a substrate injection current and thus is limited to the amount of minority carriers. Consequently, one can infer that the saturation of gate

currents is largely related to the generation mechanisms of minority carriers. According to former researches, the generation current of minority carriers can be derived as [18], [25]:

$$J = \int_{w_m}^{w} \frac{qn_i}{\tau_g(x)} dx + qn_i s + \frac{qn_i^2 D_n}{N_A L_n} \tag{2-1}$$

where J is the generation current density, q is the electronic charge, w is the depletion width when the potential drop across the semiconductor equals Ψ_s, w_m is the depletion width at strong inversion, n_i is the intrinsic concentration, τ_g is the generation lifetime, s is the surface recombination velocity which depends on the interface state density, N_A is the substrate dopant concentration, and D_n and L_n are the diffusion coefficient and diffusion length of minority carriers, respectively. The first term in eq. (2-1) originates from the generation of minority carriers through bulk traps, while the second term comes from interface states. The last term represents the minority carriers diffusing from the back contact, which dominates at high temperature yet is usually neglected at room temperature. Since the amount of interface states is meant to be the same, the second term in eq. (2-1) stays as a constant value. Chen et al. utilized the increments of gate voltage (ΔV_g), depletion region width (ΔW_D) and inversion tunneling current (ΔJ_{inv}) to eliminate the effect of the constant current component attributed to interface states [21]. Accordingly, eq. (2-1) can be further derived as:

$$\Delta J = \Delta J_{inv} = \frac{q n_i \Delta W_D}{\tau_g} \tag{2-2}$$

It is believed that saturation of the gate current happens when the generation current fails to supply the large leakage current tunneling through an ultrathin gate oxide. In order to maintain current continuity, as implied in eq. (2-2), additional increment of generation current results in the broadening of depletion region width, namely, the deep depletion behavior. Due to the relatively larger bulk trap generation lifetime, the extra depletion region width can merely contribute to a slight increase in the generation current. Observations also indicate that the saturation of gate currents on current-voltage curves is accompanied by the initiation of deep depletion behavior on the corresponding capacitance-voltage curves.

Nevertheless, to know more about the saturation current of MOS capacitors, effects of geometrical features must be taken into account. For the sake of edge fringing field and electrical local thinning, saturation current tends to take place in geometrical perimeter of MOS capacitors [26], [27]. In other words, most of the saturation current passes through the perimeter of MOS capacitors instead of uniformly distributed over the whole area under the gate electrode. The device edge is suggested to serve as the tunneling center of minority carriers.

Figure 2-3 shows the current-voltage characteristics of MOS capacitors with an

oxide thickness of 21 Å. In the right part of the curves, a quick occurrence of saturation can be observed after the gate voltage turns into positive. Beyond the saturation voltage, gate currents increase very slowly, comparing to the large current variation in the left part of the curves. In order to examine the edge dependence of saturation current, gate currents are respectively divided by the device perimeter as shown in Figure 2-4. The saturation current in Figure 2-4 appears to merge closer than that in the original current-voltage curves, which manifests the previous discussion.

Following the scaling down of oxide thickness, lateral nonuniformity issue exerts more influence on the characteristics of MOS structures. As shown in Figure 2-5, it is expected that the fringing field concentrates more on the edge in devices with thinner oxides, leading to higher tunneling rate from the geometrical perimeter than from the bulk area of devices. Researches have reported that lateral nonuniformity becomes more distinct in MOS capacitors with thinner oxides, which increases the electrical local oxide thinning and induces the current crowding phenomenon on the edge [27], [28]. Figure 2-6 shows the gate current density per perimeter versus gate voltage for MOS capacitors with an oxide thickness of 19 Å. Comparing to the 21 Å one in Figure 2-4, the saturation currents merge even closer. This represents that the saturation current as well as the deep depletion phenomenon takes place more easily on the edge of MOS capacitors with thinner oxides.

It has been known that lateral nonuniformity of MOS capacitors will be enhanced under illumination, because the light will focus on the edge of devices and has little influence on the area under the opaque metal gate. Evidence confirms the above discussion from Figure 2-7, where the saturation current in the curves almost overlap under illumination. To be concluded, as long as the lateral nonuniformity is enhanced, no matter due to illumination or decrease in oxide thickness, saturation current is more likely to pass from the edge of the devices, accompanied by the occurrence of substrate deep depletion on the edge.

2-3 Capacitance-Voltage Characteristics of MOS Capacitors under Illumination

Deep depletion behavior in the capacitance-voltage characteristics of MOS capacitors has been discussed recently, with a model of dividing the capacitance-voltage curves into three regions, i.e., depletion-inversion region, edge deep depletion region, and bulk deep depletion region [24]. The depletion-inversion region can be recognized by a constant value appearing in the capacitance-voltage curves. In this first stage of deep depletion, the capacitance-voltage curves look identical to conventional high-frequency capacitance-voltage curves, where the constant value equals its minimum capacitance. The generation current of minority carriers can still supply the leakage current, and thus there is no need for the depletion

width to expand. Next, the second region, edge deep depletion region, can be identified by a subsequently decreasing trend in the capacitance-voltage curves. In this stage, edge deep depletion is believed to initiate due to stronger electrical fringing field on the edge, while the depletion width under bulk area remains unchanged. Finally, as the bias voltage keeps rising, the substrate under bulk area is also deep depleted owing to lack of minority carriers, so this third stage is called bulk deep depletion.

However, if the oxide thickness of MOS capacitors is too thin, the tunneling current will become so large that the depletion-inversion region does not appear in the capacitance-voltage characteristics. As shown in Figure 2-8(a), every capacitance-voltage curve of the MOS capacitors with different oxide thickness (below 25 Å) shows the deep depletion behavior directly, without a depletion-inversion region. The circumstance that the samples with different oxide thickness exhibit similar curves can be explained as they have nearly the same depletion width, because the high-frequency capacitance is determined by depletion width as mentioned in eq. (1-16). From the aspect of current-voltage characteristics, Figure 2-8(b) also indicates that the samples present similar saturation status, that is, a quick saturation after positive bias. Thus, the samples surely have identical deep depletion behavior.

In the following, the photoresponse of the MOS capacitors is examined. It has been reported that the depletion width will shrinks under illumination, especially on the edge of the devices [26], [29]. The generation of excess minority carriers largely increases because of photon excitation. Consequently, generation current due to illumination can totally supply the leakage current, and it does not need to rely on the extension of depletion region, which causes the deep depletion phenomenon. The depletion width of illuminated devices will become shorter than that of unlighted devices, namely, the deep depletion shrinkage. Figure 2-9 demonstrates the illuminated capacitance-voltage and current-voltage characteristics of the same samples as shown in Figure 2-8. Obviously, the depletion-inversion region, which can be seen only in capacitance-voltage curves of samples with thicker oxides, appears again. The photo-exited minority carriers prevent the depletion width from extending and thus the high-frequency capacitances of the samples can stay constant. Although illumination leads to deep depletion shrinkage at first, when the generation current excited by photon is unable to supply the leakage current, deep depletion occurs again. In other words, illumination brings about a delay of the initiation of deep depletion. This special property may be applied to the examination of ultrathin dielectric quality [23], [30]. Because the initiation of deep depletion behavior is related to the magnitude of leakage current, for devices with the same parameters, the later deep

depletion occurs, the better quality one possesses. When the oxides of MOS capacitors are too thin, the initiation of deep depletion cannot be observed and the capacitance-voltage curves merge together; nevertheless, curves can be discriminated under illumination. As shown in Figure 2-9(a), for MOS capacitors with larger oxide thickness, due to lower leakage currents, lack of minority carriers happens later, and thus deep depletion initiates later. The difference of gate capacitance for devices before and under illumination is calculated and is shown in Figure 2-10. The voltage which corresponds to the maximum of the difference capacitance can be regarded as the initiation voltage of deep depletion under illumination [29]. Indeed, samples with thicker oxides exhibits a larger initiation voltage of deep depletion under illumination. On the other hand, the photoresponse of the samples in Figure 2-9(b) also indicates a lag of current saturation, comparing to the dark current-voltage characteristics. Moreover, the voltage corresponding to the saturation of light current is consistent with the initiation voltage of deep depletion under illumination.

2-4 Summary

For MOS capacitors with ultrathin oxides, when the generation current of minority carriers in the substrate fails to supply the leakage current tunneling through the oxide, saturation of the gate current occurs. Furthermore, the geometrical perimeter of MOS capacitors is where the saturation current mainly takes place. The

gate-current-per-perimeter-versus-gate-voltage curves of samples with different areas merge closely, while illumination or decrease in oxide thickness both make the curves overlap better. Stages of deep depletion are also introduced; however, the depletion-inversion region in capacitance-voltage curves may not appear when the oxides are too thin. Under illumination, generation of minority carriers increases, leading to the shrinkage of depletion width. Therefore, illumination is able to postpone the initiation of deep depletion behavior as well as saturation of gate current. The voltage corresponding to the maximum difference capacitance can be regarded as the initiation voltage of deep depletion under illumination, showing a great consistency with the saturation voltage of the light current.

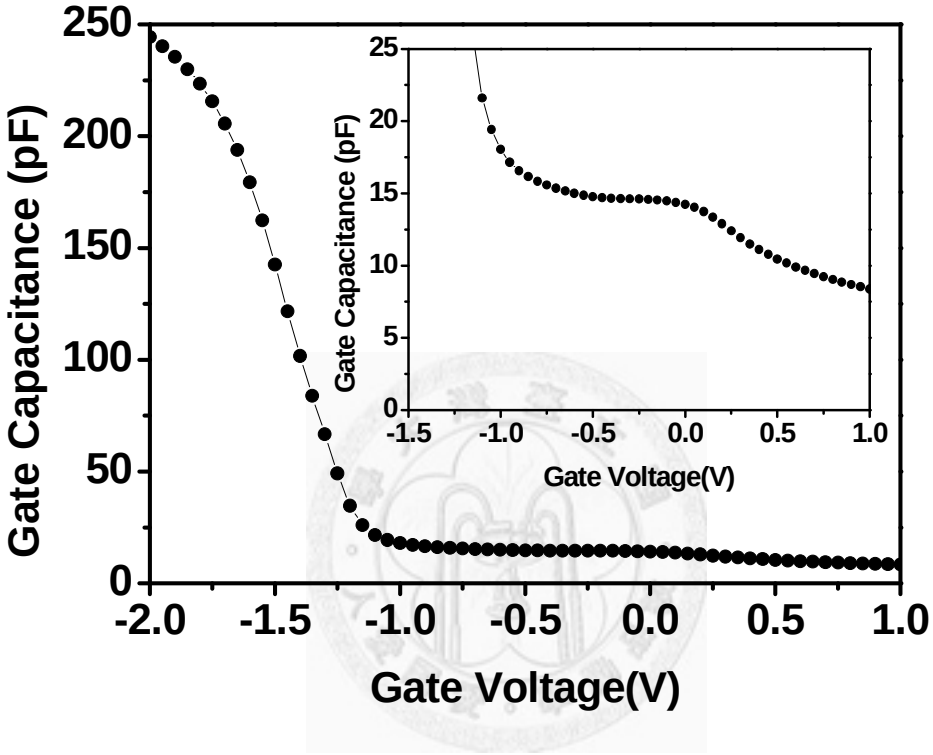


Figure 2-1 A typical high-frequency C-V curve of MOS(p) capacitor with oxide thicker than 25 Å. Deep depletion region of the curve is enlarged in the inset.

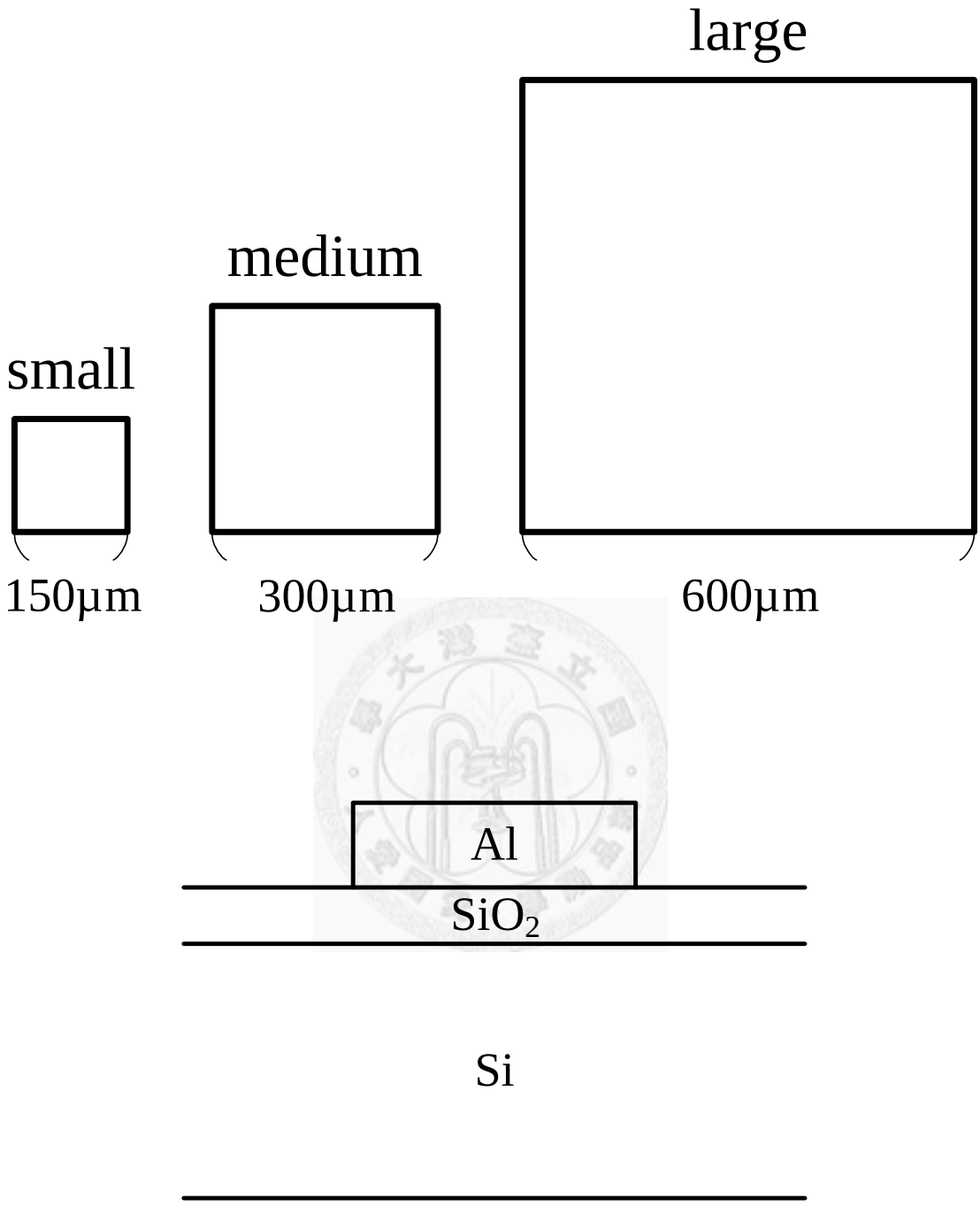


Figure 2-2 Illustration of (a) the top view and (b) the side view of the patterns used in this work.

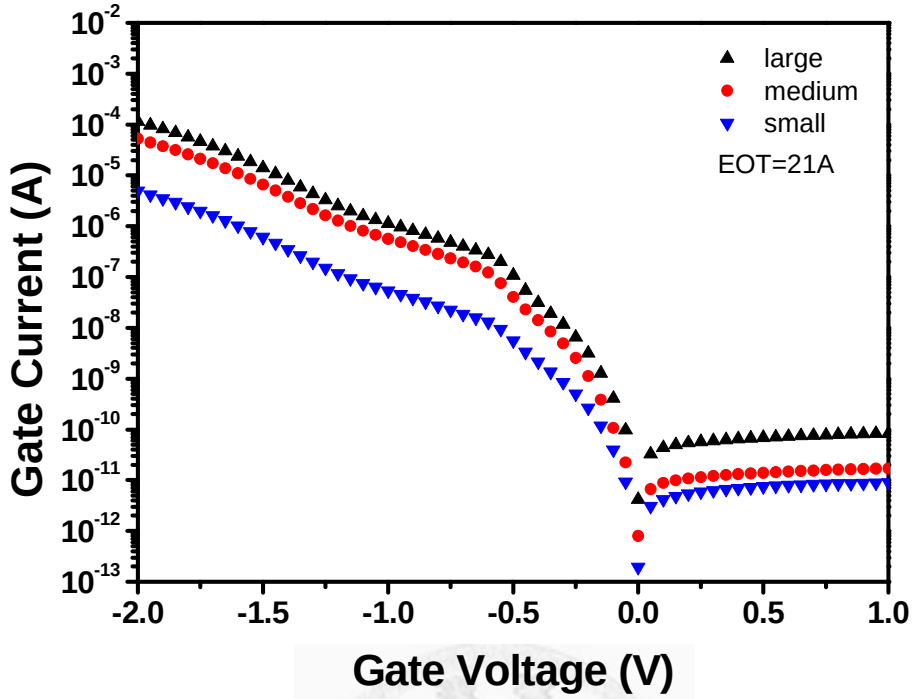


Figure 2-3 Original current-voltage characteristics of MOS capacitors with device areas of large, medium, and small sizes.

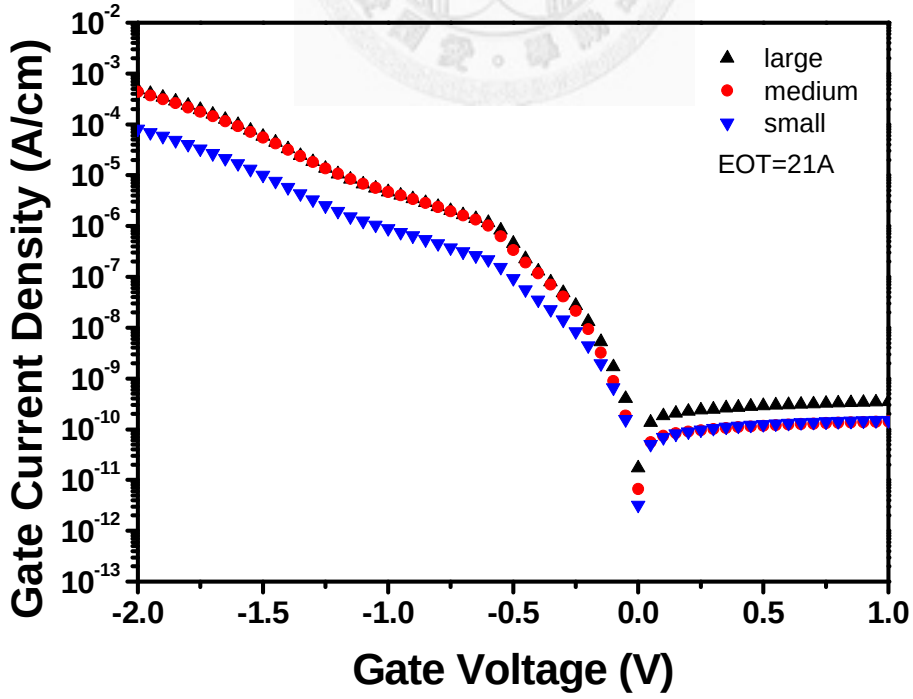
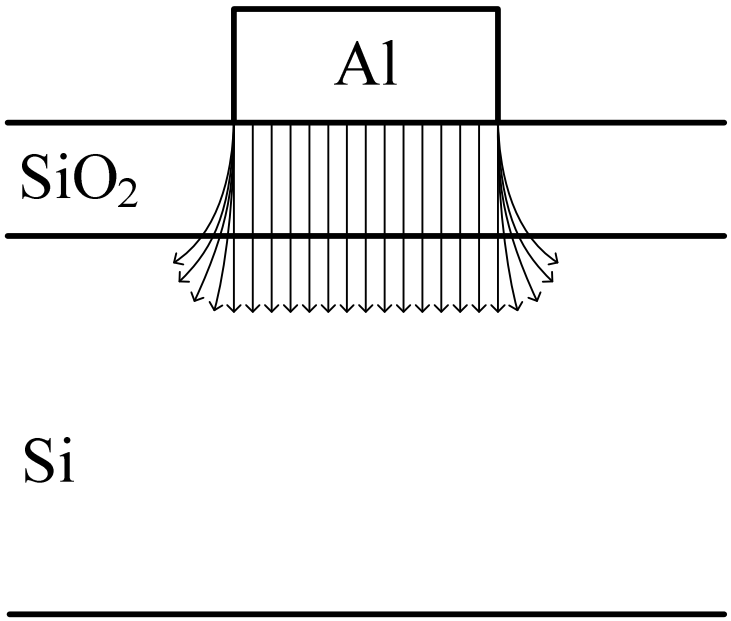
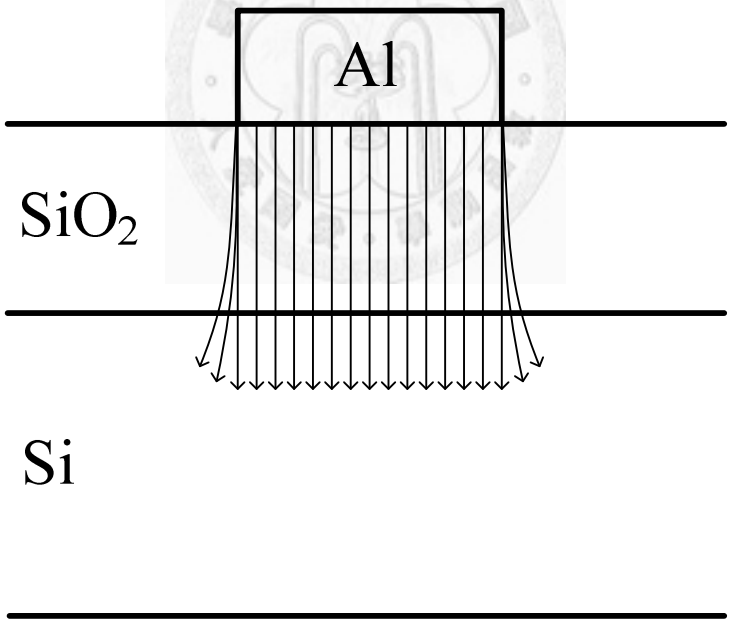


Figure 2-4 The gate current density per perimeter versus gate voltage curves for MOS capacitors with an oxide thickness of 21 Å.



(a)



(b)

Figure 2-5 Schematic diagrams of fringing field distribution for MOS capacitors with (a) thinner and (b) thicker oxide.

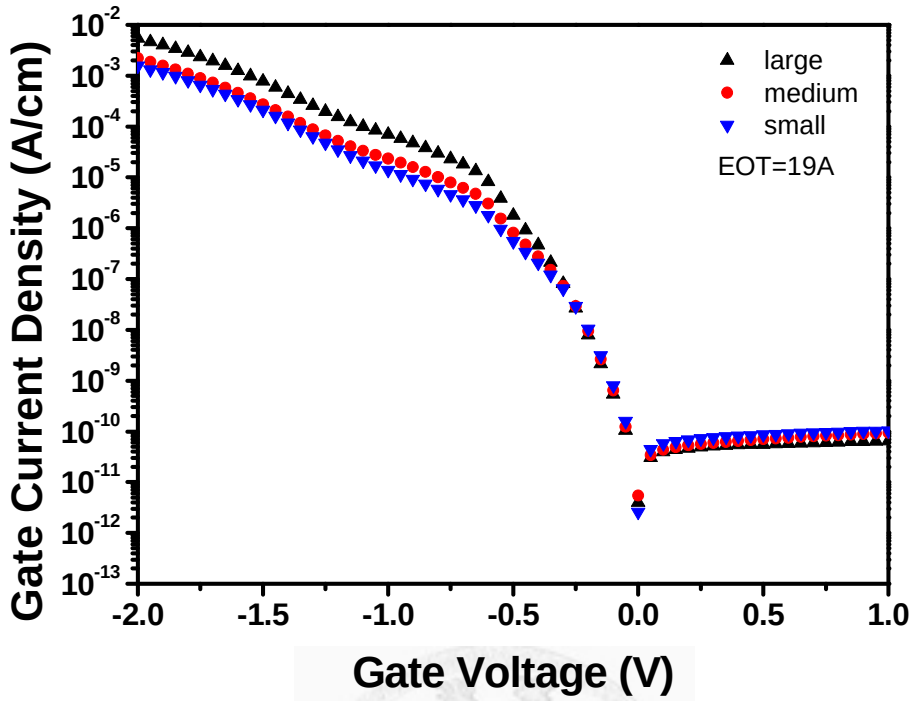


Figure 2-6 The gate current density per perimeter versus gate voltage curves for MOS capacitors with an oxide thickness of 19 Å.

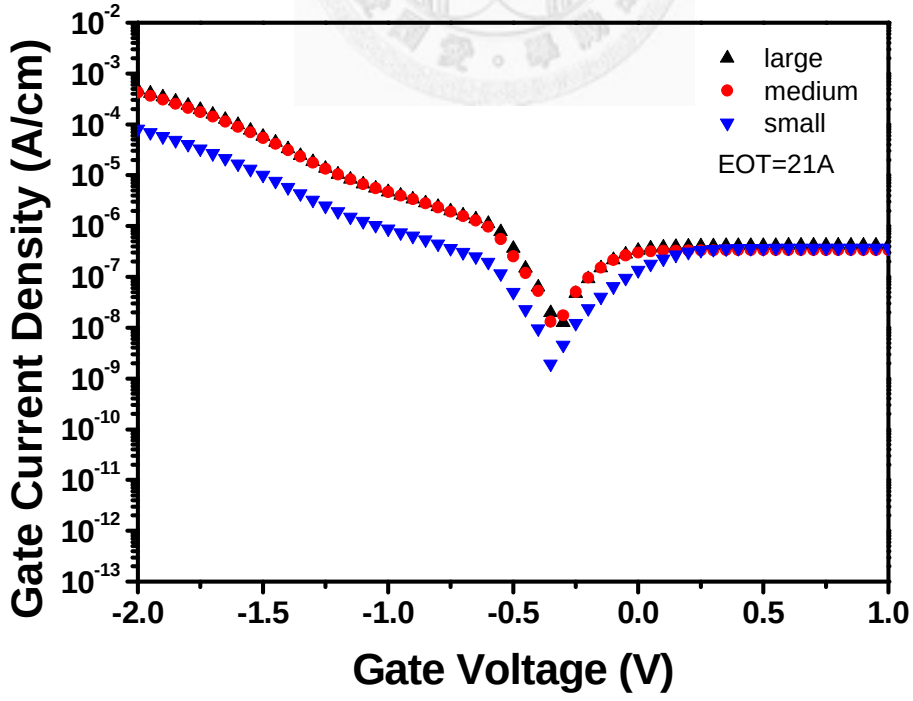
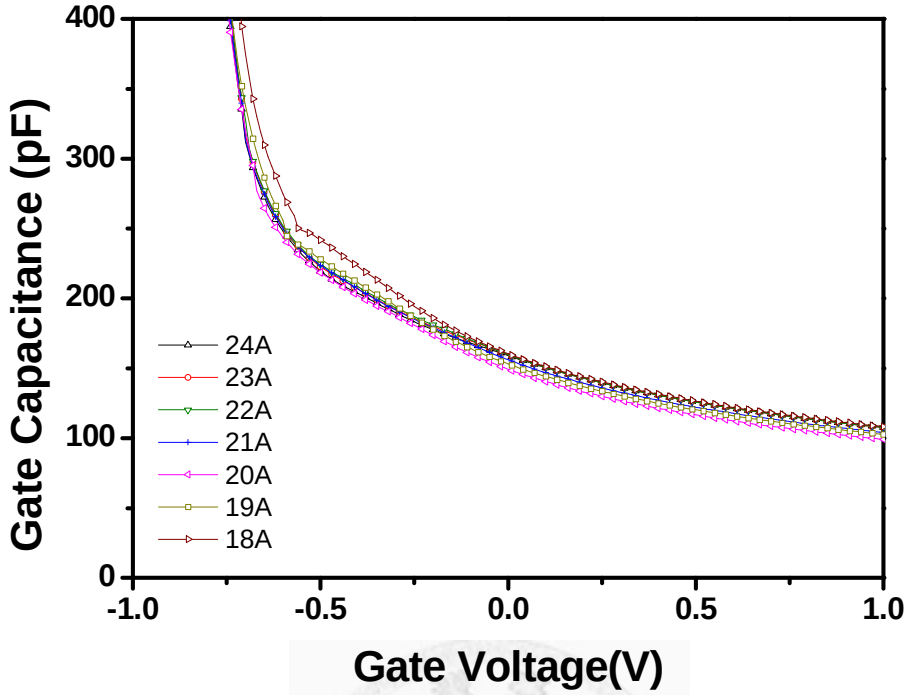
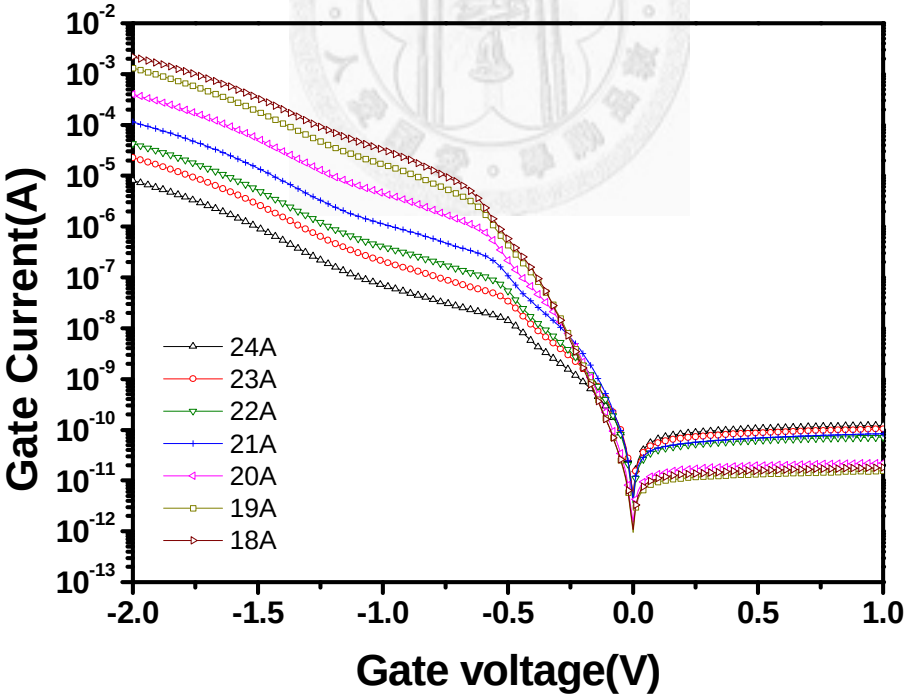


Figure 2-7 The gate current density per perimeter versus gate voltage curves for MOS capacitors with an oxide thickness of 21 Å under illumination.

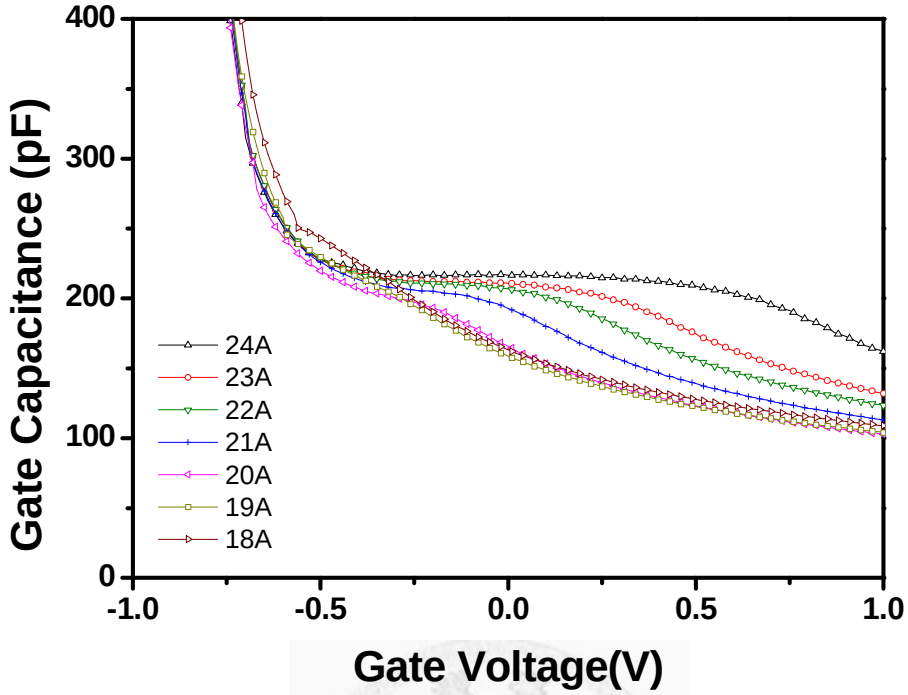


(a)

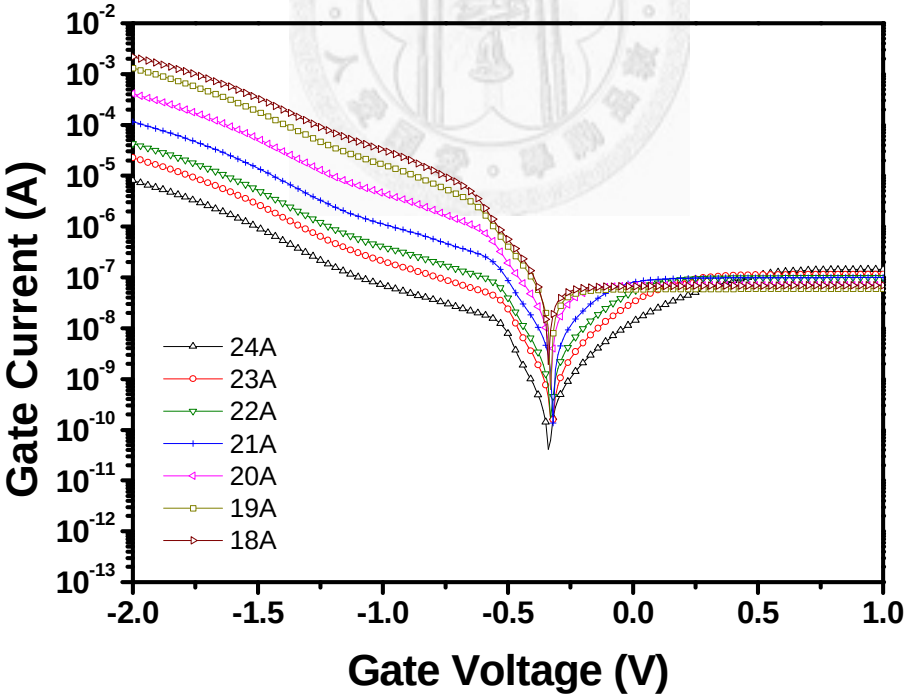


(b)

Figure 2-8 The (a) C-V curves and (b) I-V curves for MOS capacitors with different oxide thickness before illumination. The area of every sample is 600 μm × 600 μm.



(a)



(b)

Figure 2-9 The (a) C-V curves and (b) I-V curves for MOS capacitors with different oxide thickness under illumination. The area of every sample is 600 μm × 600 μm.

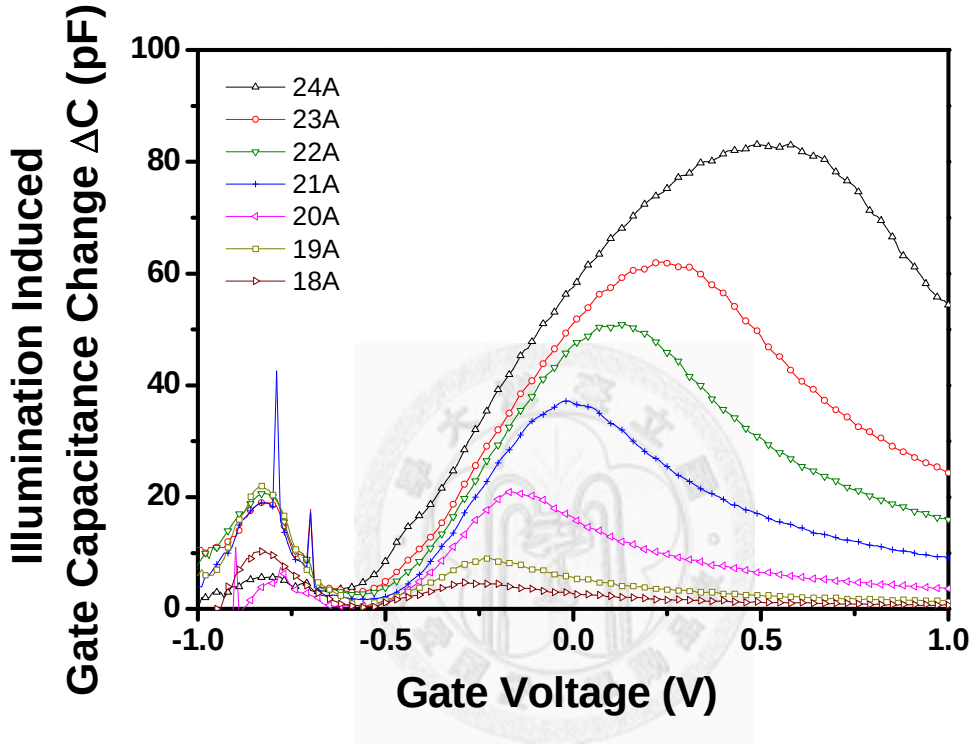


Figure 2-10 Difference of the gate capacitance due to illumination based on Figure 2-8(a) and Figure 2-9(a).

Chapter 3

Characterization of Deep Depletion Behavior by Pattern Design

3-1 Introduction

From the previous discussion, it is known that the fringing field at the edge of MOS capacitors induces the major portion of the conduction of the saturation current. Furthermore, the edge region and bulk region of the substrate are supposed to exhibit different deep depletion behaviors, according to the capacitance-voltage curves of MOS capacitors with ultrathin oxides. However, the exact scales of edge region and

bulk region cannot be clearly recognized through the data of the aforementioned MOS capacitors with simple three-size patterns. As a result, patterns with various changes in the edge-related parameters are designed, in order to characterize the effect of edge fringing field on the deep depletion behavior as well as the saturation of gate current in a qualitative way. Samples with oxide thickness of 18 Å are fabricated so as to enlarge the edge fringing effect.

3-2 Parameters of Designed Patterns

In our assumption, variation of either the electrode width or the electrode separation may alter the coupling of the depletion region under MOS capacitors. Thus, patterns with parameters of electrode width (W) and electrode separation (S) are designed to confirm our assumption. Figure 3-1 illustrates the schematic diagrams of the top view and the cross section of the MOS capacitors with designed patterns. As can be seen on the diagrams, the patterns are designed to define the electrode of each MOS capacitor with a comb-shaped part and a small rectangular part. The small rectangular part of the electrode serves as the contact, while the comb-shaped part of the electrode mainly determines the electrical characteristics of our concern.

The designed patterns are classified into two groups, patterns with different electrode width and patterns with different separation, whose parameters are listed in Table 3-1 and Table 3-2, respectively. As shown in Table 3-1, samples with constant

electrode separation but different electrode width n are denoted as W_n, while they have the same device perimeter but different device areas. On the contrary, samples with constant electrode width but different electrode separation n are denoted as S_n, possessing equal device perimeters and areas, as shown in Table 3-2.

3-3 Results and Discussion

3-3-1 Samples with Different Electrode Width

The capacitance-voltage characteristics of samples with different electrode width are shown in Figure 3-2. The oxide thickness of the samples is 18 Å, and therefore the leakage currents are so high that the substrates seem to enter the edge deep depletion stage directly, without the appearance of constant capacitance in depletion-inversion stage. The device areas of the samples differ a little, and the high-frequency capacitances of the samples are observed to show a proportional relation to the device areas approximately, as shown in Figure 3-2(b). This implies that the substrates of the MOS capacitors possess similar deep depletion behaviors.

Figure 3-3 shows the current-voltage characteristics of the above samples, and it is clearly seen that every curve exhibits a quick saturation, corresponding to the early deep depletion behavior in the capacitance-voltage curve. The values of the saturation currents vary slightly, manifesting once again that the saturation currents come from the edges of the samples. To sum up, the saturation currents of MOS capacitors with

electrode width lager than 10 μm and electrode separation of 30 μm are still proportional to the geometrical perimeters, without the effect of coupling depletion region due to nearby electrodes.

3-3-2 Samples with Different Electrode Separation

The capacitance-voltage characteristics of samples with different electrode separation are shown in Figure 3-4. Owing to the ultrathin oxides, the curves also lack the appearance of constant capacitance in depletion-inversion region and exhibit early deep depletion behavior. Moreover, the capacitance-voltage curves of different samples appear to merge together under positive bias. According to eq. (1-16), the high-frequency capacitance of a MOS capacitor is proportional to its area and is inversely proportional to its depletion width. Since the edge region has a relatively smaller area and a larger depletion width, the edge capacitance component is supposed to be ignorable. Therefore, the high-frequency capacitances are dominated by the bulk capacitance components under large positive bias. The edge deep depletion behaviors of different samples are possibly diversified, however, it is suggested that the deep depletion behaviors of the bulk regions of different samples are nearly the same.

Figure 3-5 shows the current-voltage characteristics of the samples with different electrode separation. For samples with electrode separation of 25 μm and 30 μm (S_{25}

and S_{30}), the current-voltage curves shape like those of simple square MOS capacitors with ultrathin oxides, presenting quick saturation of the gate currents. However, the current-voltage curves of samples with electrode separation below 20 μm (S_{20} , S_{15}, S_{10}, S_5 and S_3) display obvious differences from the previous current-voltage characteristics, and seem to undergo a transition region when the curves are about to saturate. Unlike the aforementioned current saturation behavior, the currents of these samples rise up again to a certain extent after the first occurrence of saturation, then apparently reach to their second saturation. Moreover, it is perceived that the samples with smaller electrode separation exhibit slower rising of currents at the second time and smaller final saturation currents.

Explanation about the carrier conduction mechanism of the samples with different electrode separation is proposed as follows. For the samples with larger electrode separation (S_{25} and S_{30}), the minority carrier conduction goes through three stages, which also correspond to the capacitance-voltage models of deep depletion behavior introduced previously, i.e., depletion-inversion stage, edge deep depletion stage, and bulk deep depletion stage, as shown in Figure 3-6 (a), (b), and (c), respectively. First, in the depletion-inversion stage, the current-voltage curve presents a steep climb, while the leakage current that tunnels through the oxide is still small and is sufficiently supplied by the generation of minority carriers. As seen in Figure

3-6 (a), the tunneling carriers mainly come from the edge region, where the fringing field induces deeper depletion width than the bulk region. Although this stage is called depletion-inversion stage, the inversion layer forms hardly or just locally due to the leakage current. Next, as the leakage current keeps on increasing, the generation of minority carriers fails to supply the leakage current. The current-voltage curve displays a slight rise, said to enter the edge deep depletion stage. Since the fringing field concentrates on the geometrical perimeters, the edge region encounters deep depletion ahead of the bulk region. It is known that extension of the depletion region only introduces a small increase in the generation of minority carriers, as illustrated in Figure 3-6 (b). From this stage on, the gate current is considered to become saturated, and mainly comes from the edge region. Finally, the current-voltage curve enters the bulk deep depletion stage, which is recognized by the barely increasing slope of the curve. In this stage, deep depletion also initiates in the bulk region as shown in Figure 3-6 (c).

On the other hand, for the samples with smaller electrode separation (S_{20} , S_{15}, S_{10}, S_5 and S_3), the minority carrier conduction seems to undergo four stages, which are proposed as depletion-inversion stage, edge deep depletion stage, front stage of bulk deep depletion, and bulk deep depletion stage, as shown in Figure 3-7 (a), (b), (c), and (d), respectively. It is supposed that the depletion regions under the comb-shaped

electrodes are partly overlapped due to the small electrode separation. In the first stage, depletion-inversion stage, the generation of minority carriers is still able to supply the leakage current, while the depletion regions have not started to expand obviously, as depicted in Figure 3-7 (a). While the leakage current continues to increase, the minority charges generated in the depletion region become insufficient for the supply of the tunneling current into two adjacent electrodes. The values of the gate currents appear to be screened, comparing to the current-voltage curves of the samples with larger electrode separation. It is suggested that this characteristic results from the coupling of the depletion regions under the edge areas, as shown in Figure 3-7 (b). The knowledge that the saturation currents mostly come from the edge region supports this speculation, because different current-voltage characteristics between the two groups of samples are also caused by the edge-related parameter and electrode separation. Therefore, in the second stage, edge deep depletion occurs and the saturation current from the edge region seems to be screened due to the sharing of minority charges between two adjacent electrodes. Subsequently, when the current-voltage curves start to go up at the second time, the third stage begins. Since the gate current from the edge is limited, the increase in the gate current is reasonably explained by the addition of leakage current from the bulk region. The minority carriers, probably including bulk-generated charges or local inversion charges, give

rise to the noticeable increase in gate current, as shown in Figure 3-7 (c). Finally, the last stage, bulk deep depletion stage, happens when the supply of minority carriers is overtaken again by the leakage current. It is believed that the bulk electric field exceeds the critical field of deep depletion in this stage, and the saturation of current occurs at the second time. An extension of the bulk depletion width leads to a slight increase in the gate current. The schematic diagram of the minority carrier conduction in this stage is illustrated by Figure 3-7 (d).

Aside from the previous discussion, it is supposed that the coupling of depletion region also exerts some influence on the edge electric field for the samples with smaller electrode separation. For the samples with larger electrode separation, when the gate current collected from the edge region reaches to a certain extent, the bulk deep depletion occurs and contributes to a small increase in the gate current. However, for the samples with smaller electrode separation, the gate current collected from the edge region fails to reach to the enough amount as in S_{25} and S_{30} due to the sharing of minority carriers, and thus the electric field keeps on adding on the edge region until the initiation of front stage of bulk deep depletion. Therefore, the samples with smaller electrode separation possess longer stay in the edge deep depletion stage, and later occurrence of front stage of bulk deep depletion as well as bulk deep depletion stage. On the aspect of final saturation currents, the characteristic which samples with

smaller electrode separation exhibit smaller values is suggested to originate from the less total volume of depletion region, for the generation current of minority carriers is proportional to the volume of depletion region. Although the volume of bulk depletion region seems to be similar for the two groups of samples, the volume of total depletion region on the edge is still less due to the coupling of depletion region for the samples with smaller electrode separation.

Illumination has been discussed formerly to excite the generation of minority carriers and cause the shrinkage of depletion width on the edge region. Figure 3-8 shows the current-voltage characteristics of samples with different electrode separation under illumination. It is observed that every curve shows a quick saturation, without the transition region, and the photocurrents under positive bias increase with the electrode separation. The schematic diagrams for the conduction and generation mechanism of minority carriers under illumination for large and small separations are illustrated in Figure 3-9 (a) and (b), respectively. It is believed that the sum of minority charges collected from the edge depletion region is smaller for the samples with smaller electrode separation, due to the coupling of the depletion region as well as the sharing of minority charges. The disappearance of the transition region may results from the abundant photo-excited minority carriers. The lateral nonuniformity between edge region and bulk region is intensified by illumination which makes the

effect of bulk region ignorable. Photocurrents of the samples at the bias of 4 V are recorded under changing irradiance, as shown in Figure 3-10. It is clearly seen that the photocurrents of samples with different electrode separation approximately maintain the same tendency to the irradiance. Under stronger irradiance, the photo-excited charges generate more and thus the photocurrents increase for all the samples.

3-4 Summary

In this chapter, patterns with different electrode width and separation are designed and MOS capacitors with the patterns are fabricated. Both the capacitance-voltage and current-voltage characteristics of the samples with different electrode width exhibit great similarity with the MOS capacitors having simple square electrodes. Nevertheless, the current-voltage curves of samples with smaller electrode separation seem to be screened and undergo a transition region comparing to the normal curves. Explanation and illustration are consequently proposed, supposing that the behavior originates from the coupling of edge depletion region and the sharing of minority charges between two adjacent electrodes. In addition, photoresponse of the samples with different electrode separation is also examined. The transition regions on the current-voltage curves of samples with smaller electrode separation disappear due to the abundant minority carriers exited under illumination.

Table 3-1 Parameters of the designed patterns with different electrode width.

sample notation	electrode width (μm)	electrode separation (μm)	electrode area (μm^2)	edge perimeter (μm)
W_{10}	10	30	45000	10500
W_{15}	15	30	67500	10500
W_{20}	20	30	90000	10500
W_{25}	25	30	112500	10500
W_{30}	30	30	135000	10500

Table 3-2 Parameters of the designed patterns with different electrode separation.

sample notation	electrode width (μm)	electrode separation (μm)	electrode area (μm^2)	edge perimeter (μm)
S_3	30	3	135000	10500
S_5	30	5	135000	10500
S_{10}	30	10	135000	10500
S_{15}	30	15	135000	10500
S_{20}	30	20	135000	10500
S_{25}	30	25	135000	10500
S_{30}	30	30	135000	10500

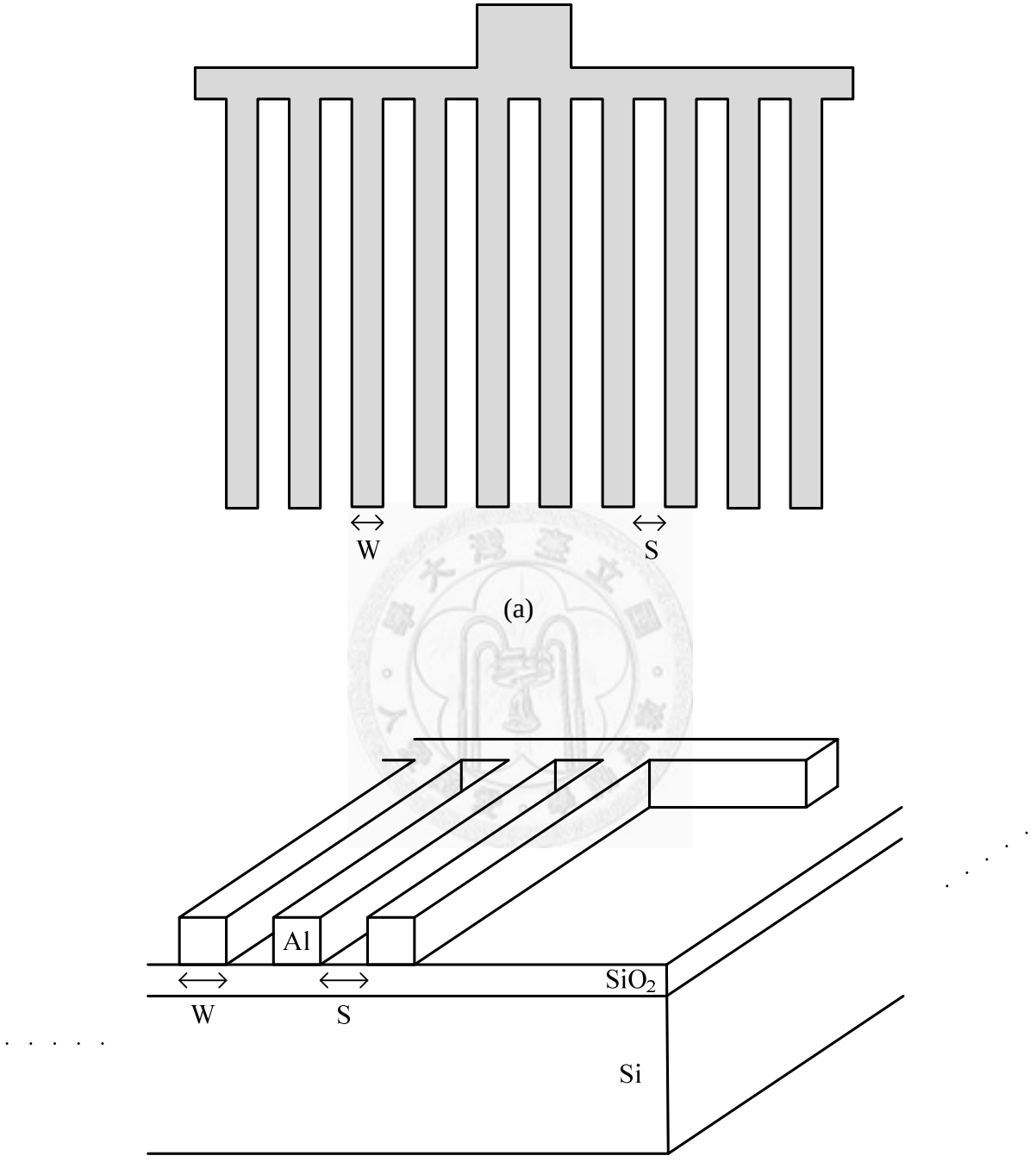
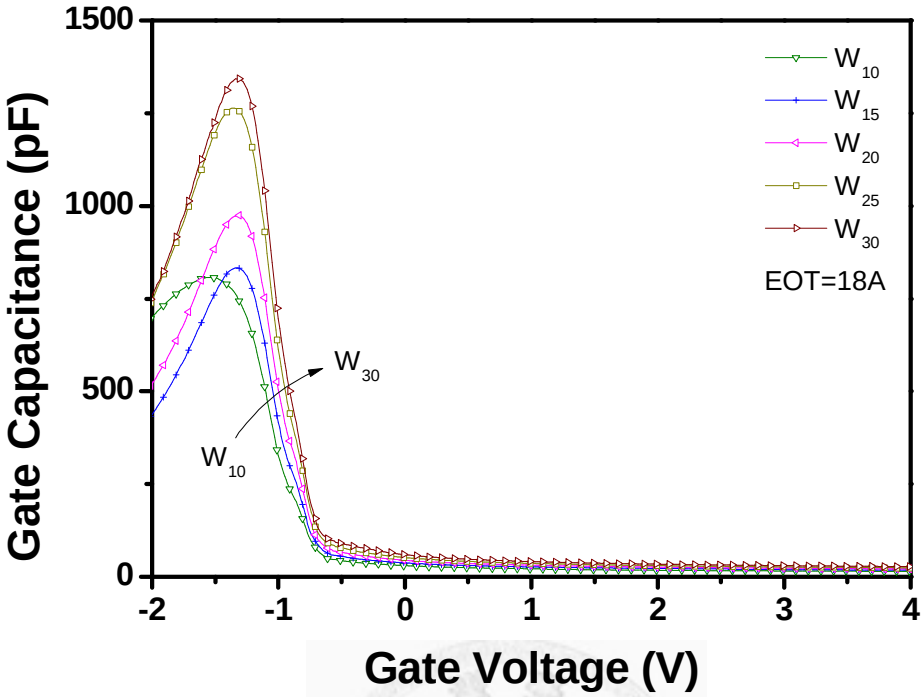
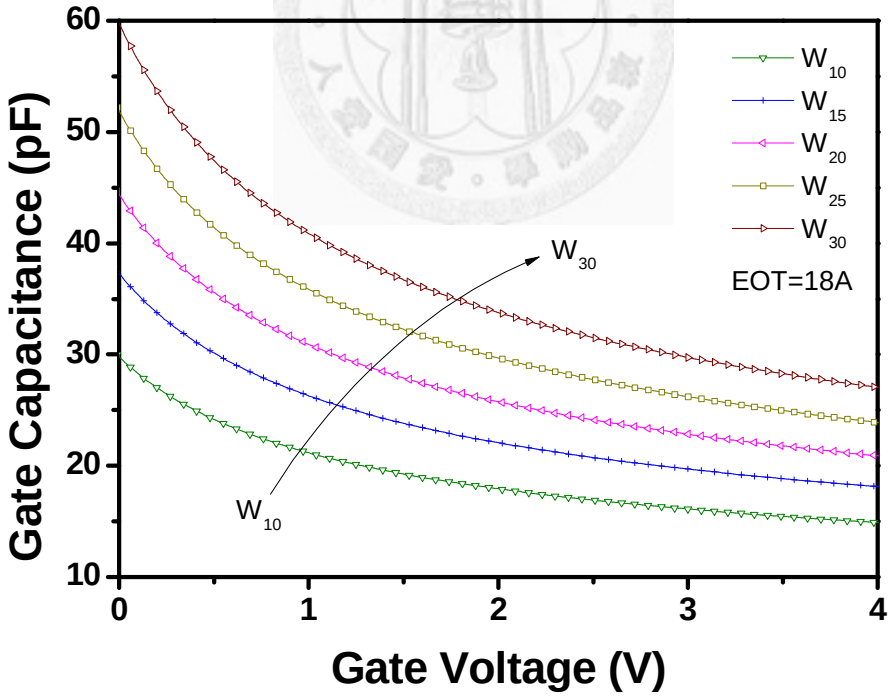


Figure 3-1 Illustration of (a) the top view and (b) the cross section of the MOS capacitors with designed patterns of various electrode width (W) and separation (S).

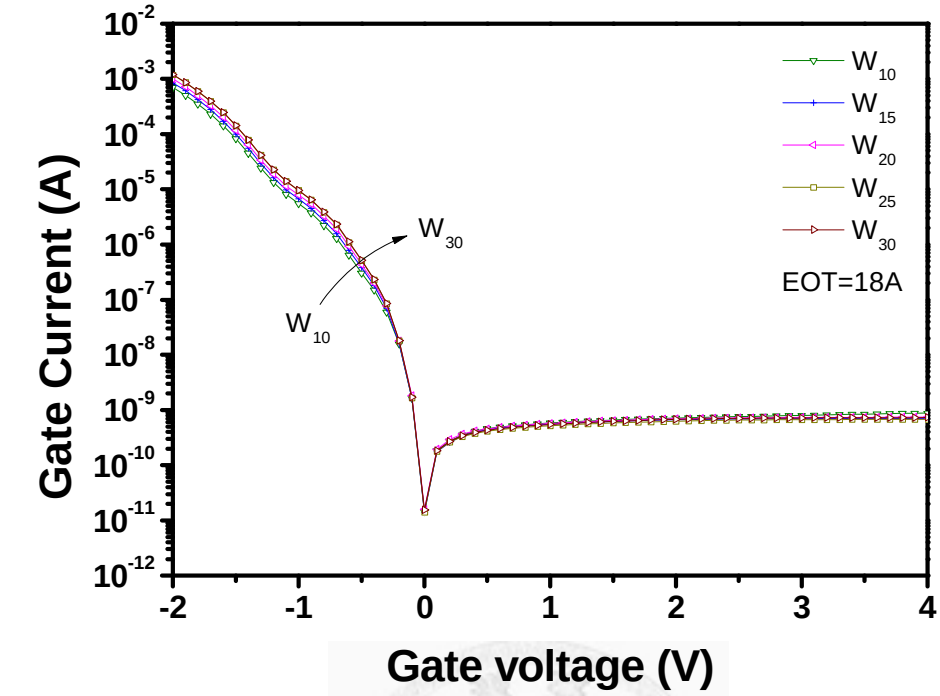


(a)

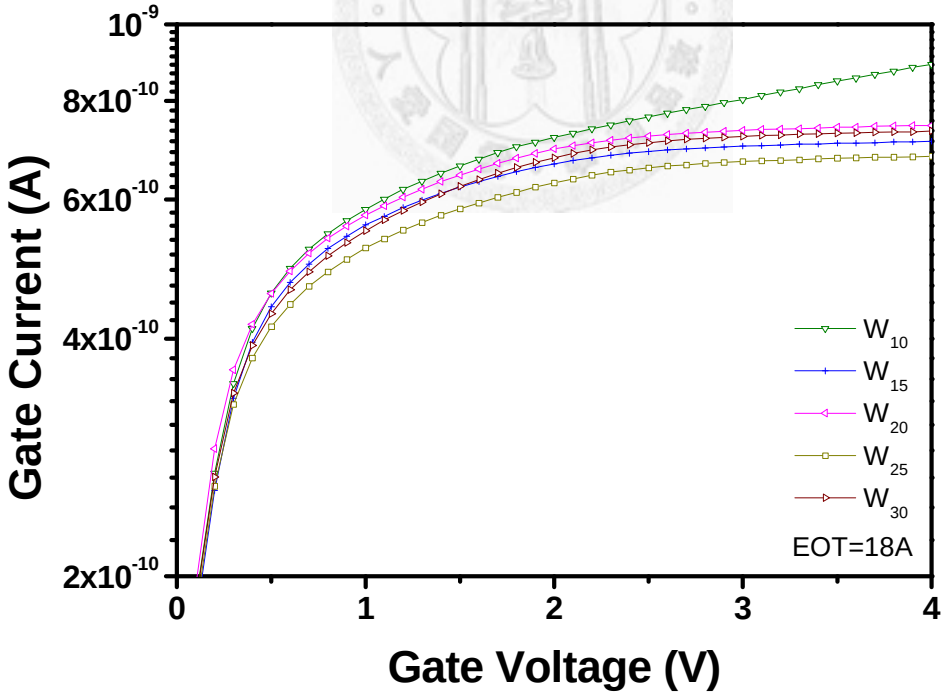


(b)

Figure 3-2 (a) Original and (b) local-magnified capacitance-voltage characteristics of samples with different electrode width.

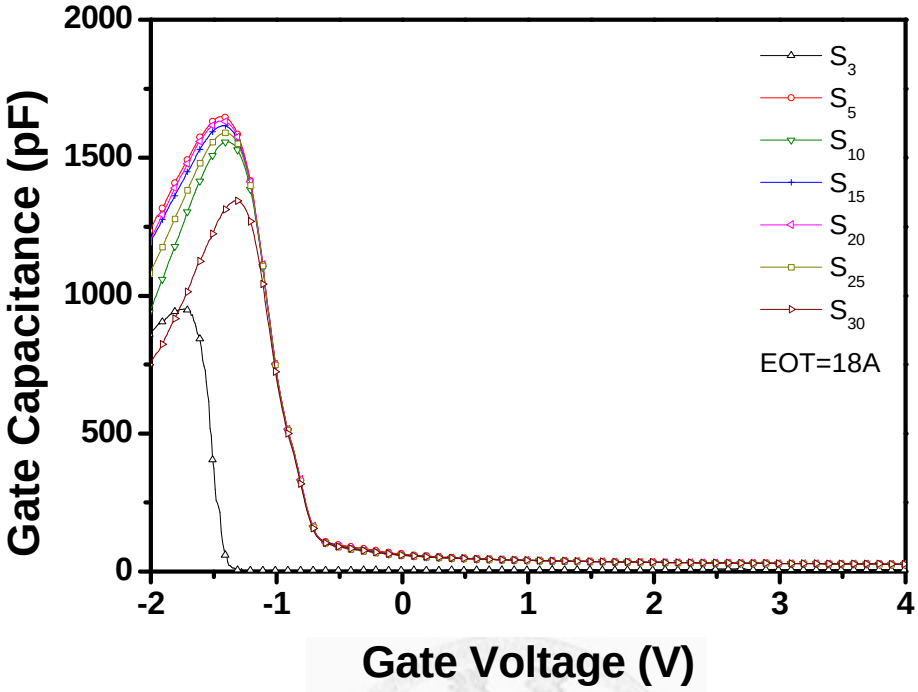


(a)

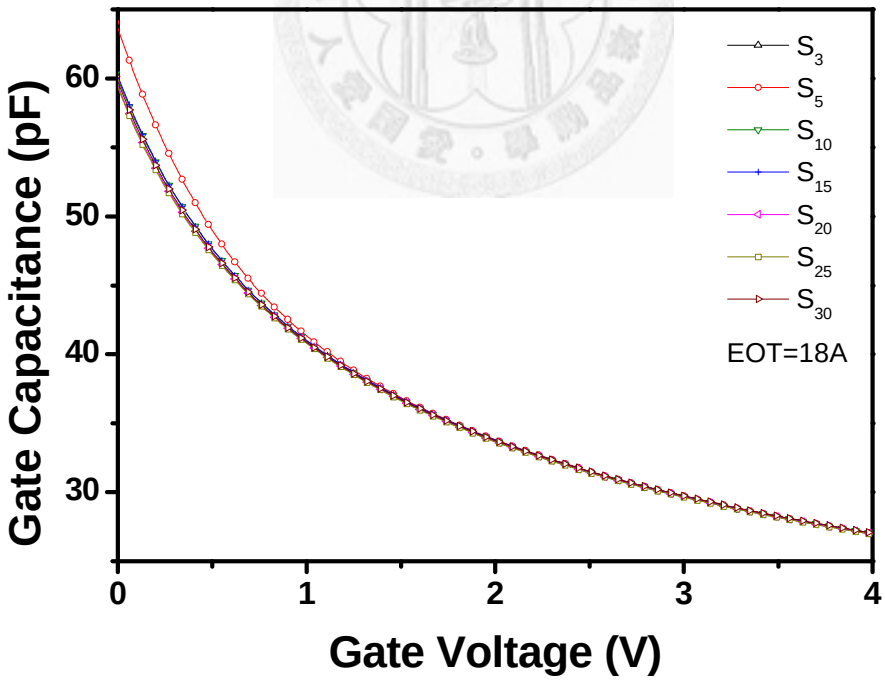


(b)

Figure 3-3 (a) Original and (b) local-magnified current-voltage characteristics of samples with different electrode width.

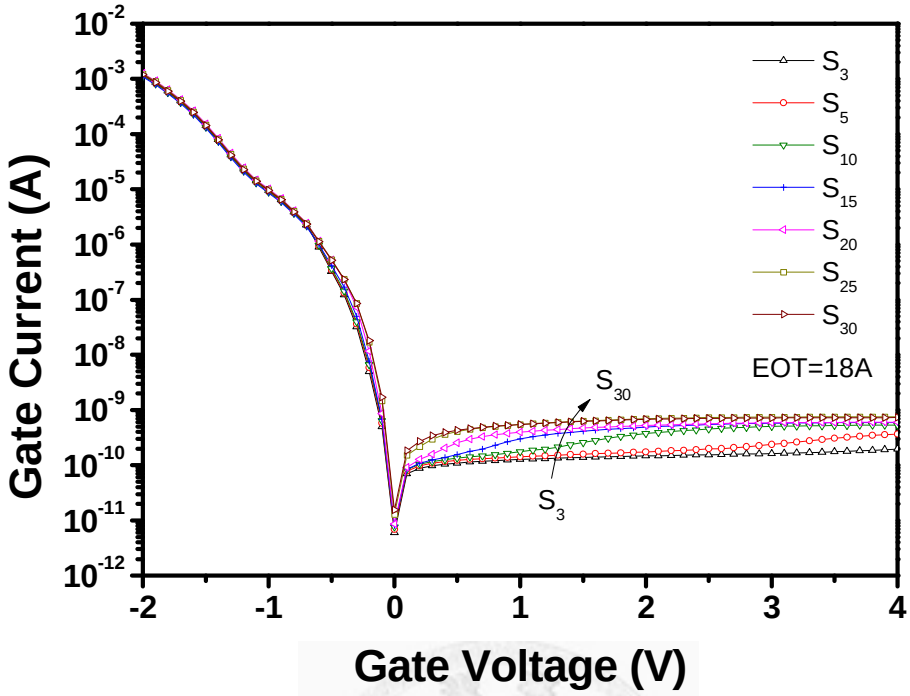


(a)

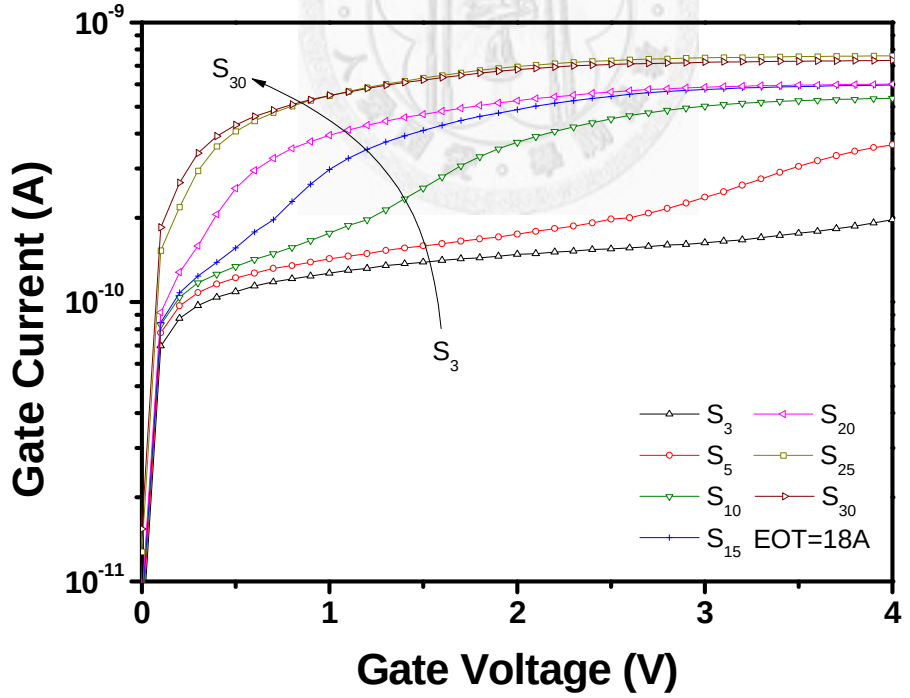


(b)

Figure 3-4 (a) Original and (b) local-magnified capacitance-voltage characteristics of samples with different electrode separation.

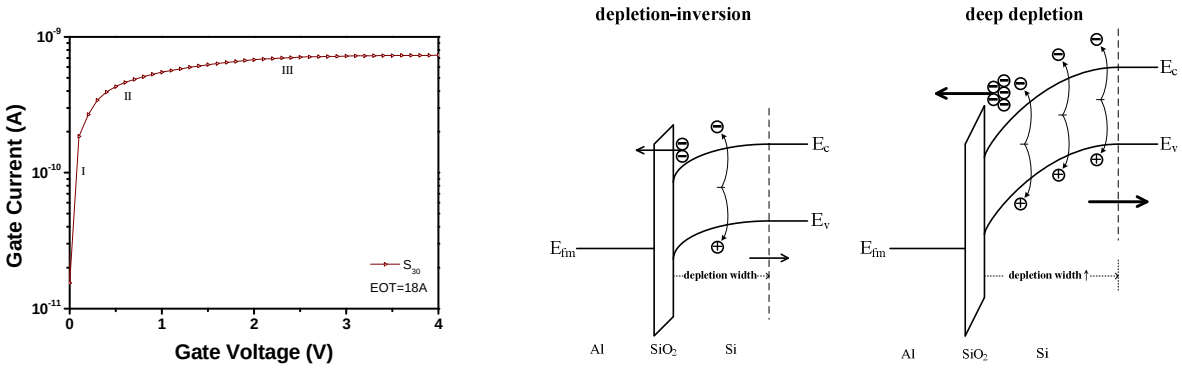


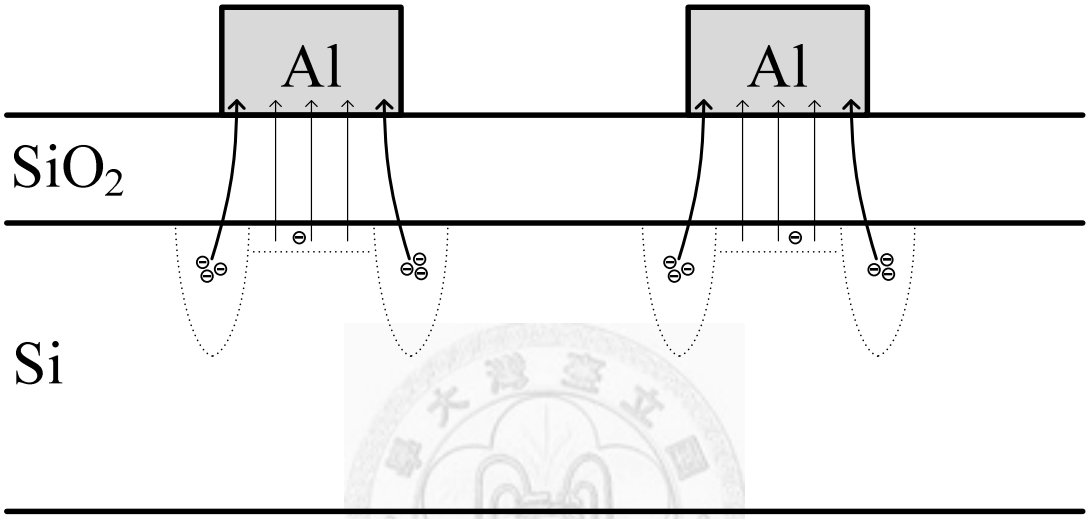
(a)



(b)

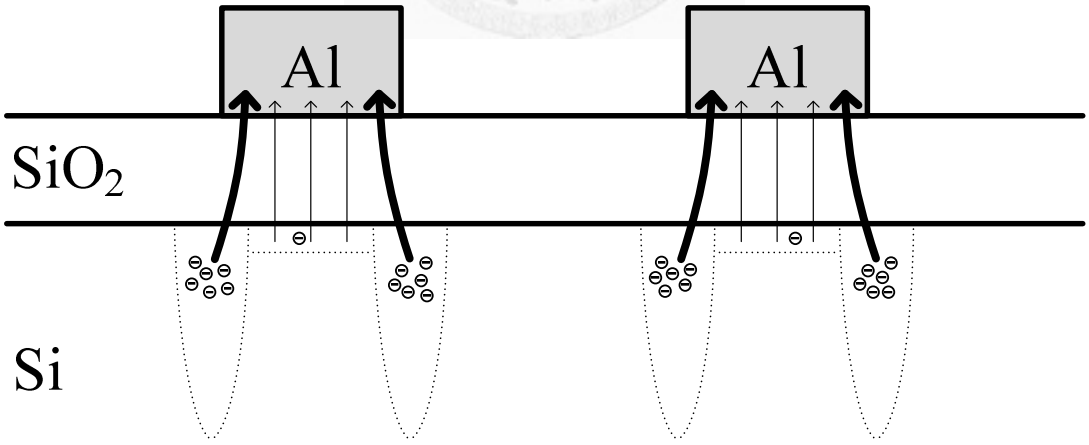
Figure 3-5 (a) Original and (b) local-magnified current-voltage characteristics of samples with different electrode separation.





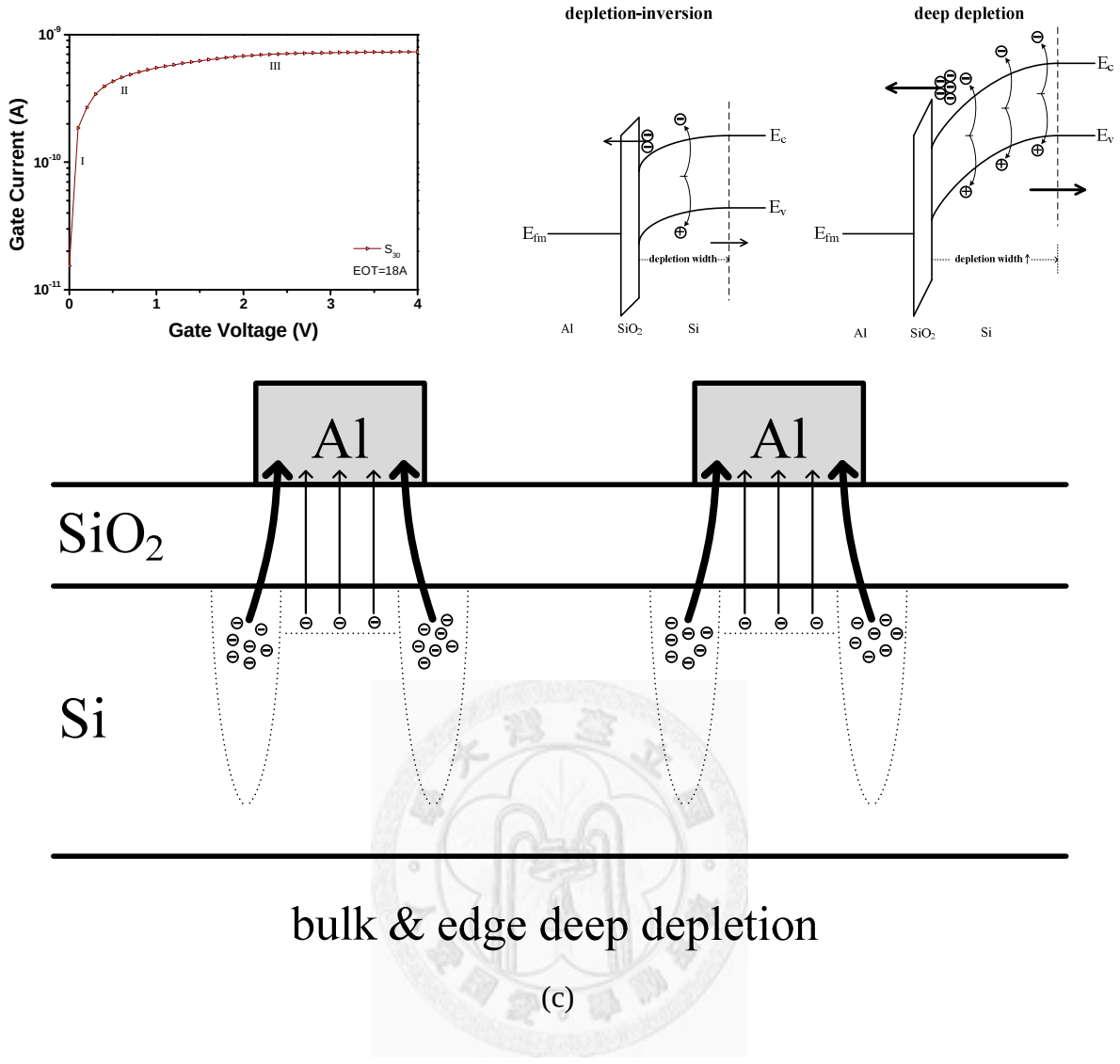
bulk & edge depletion-inversion

(a)



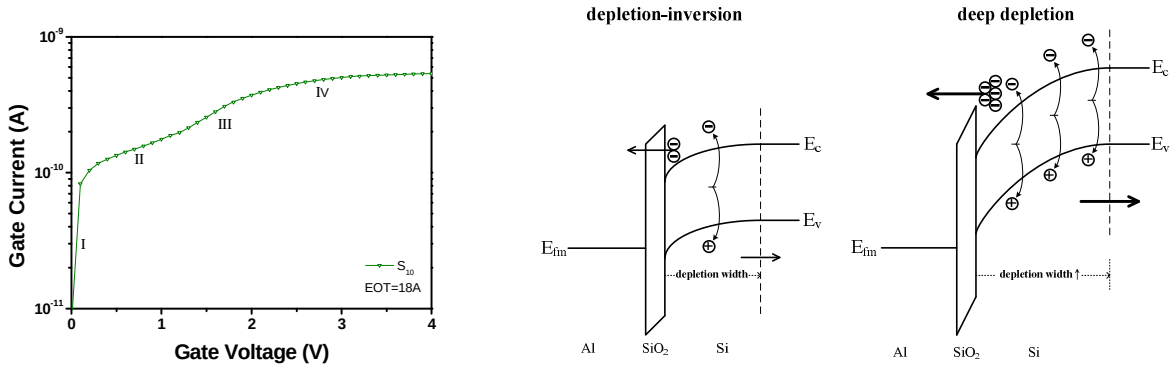
bulk depletion-inversion / edge deep depletion

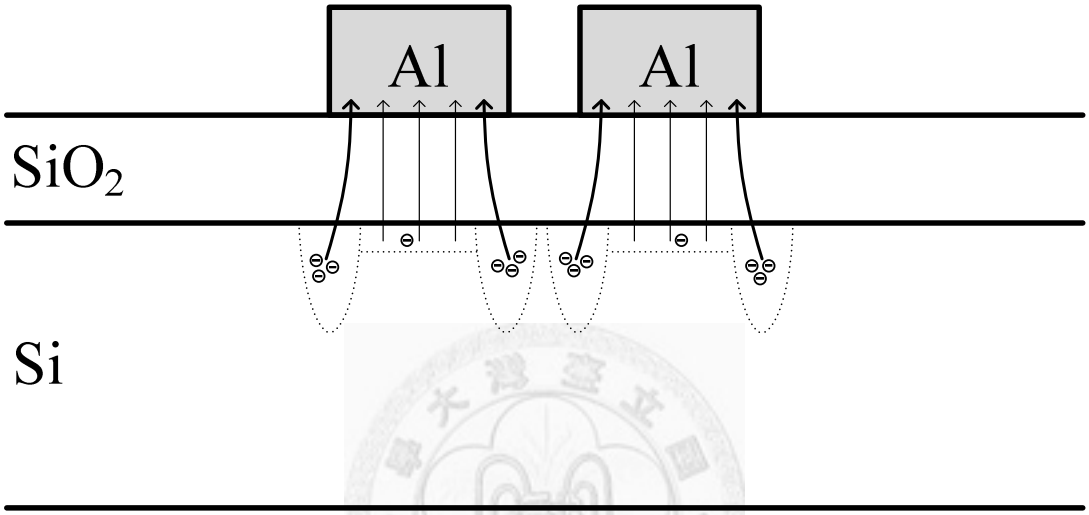
(b)



(c)

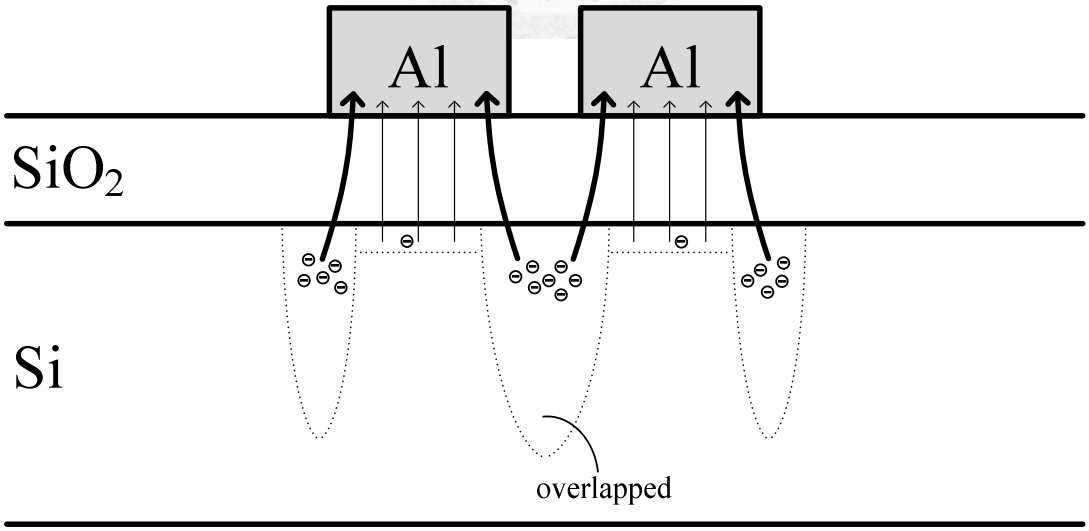
Figure 3-6 Schematic diagrams for minority carrier conduction of samples with larger electrode separation at (a) Region I, depletion-inversion stage, (b) Region II, edge deep depletion stage, and (c) Region III, bulk deep depletion stage.





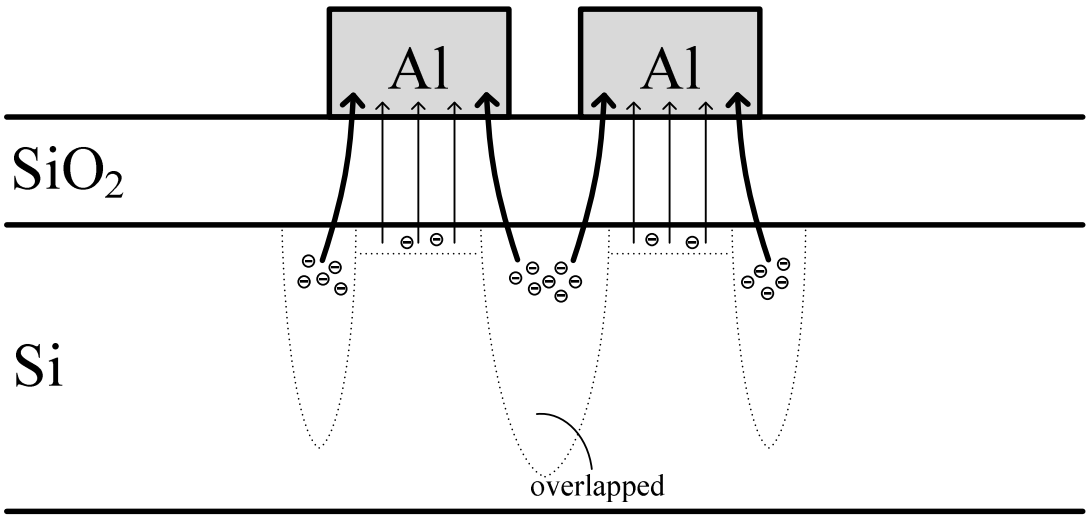
bulk & edge depletion-inversion

(a)



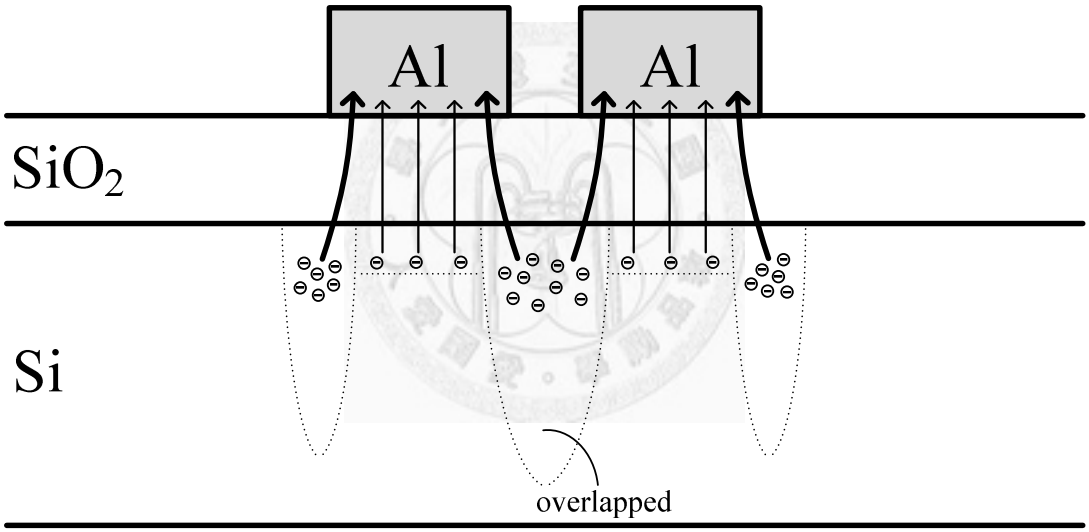
bulk depletion-inversion / edge deep depletion

(b)



front stage of bulk deep depletion / edge deep depletion

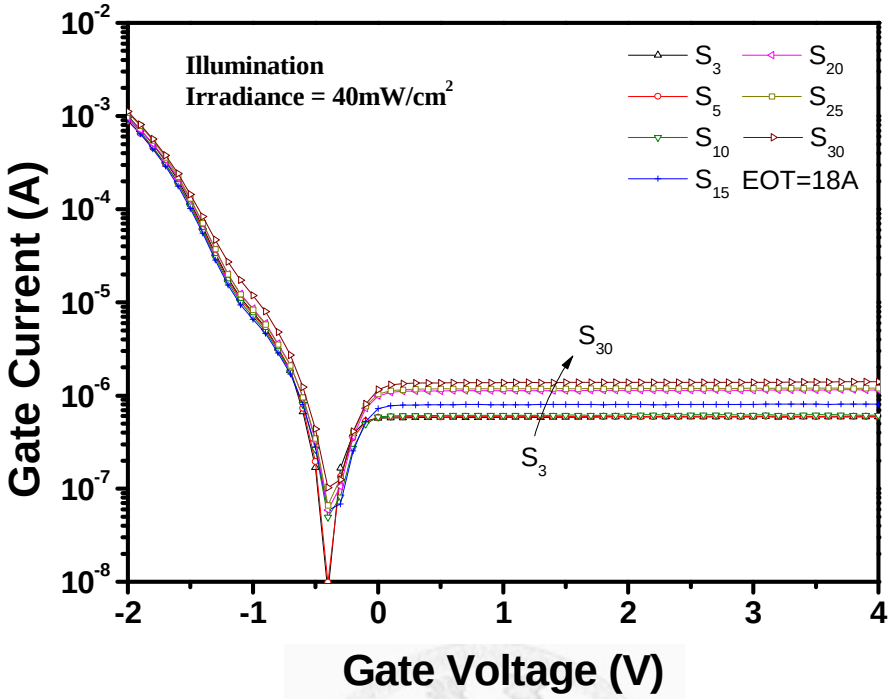
(c)



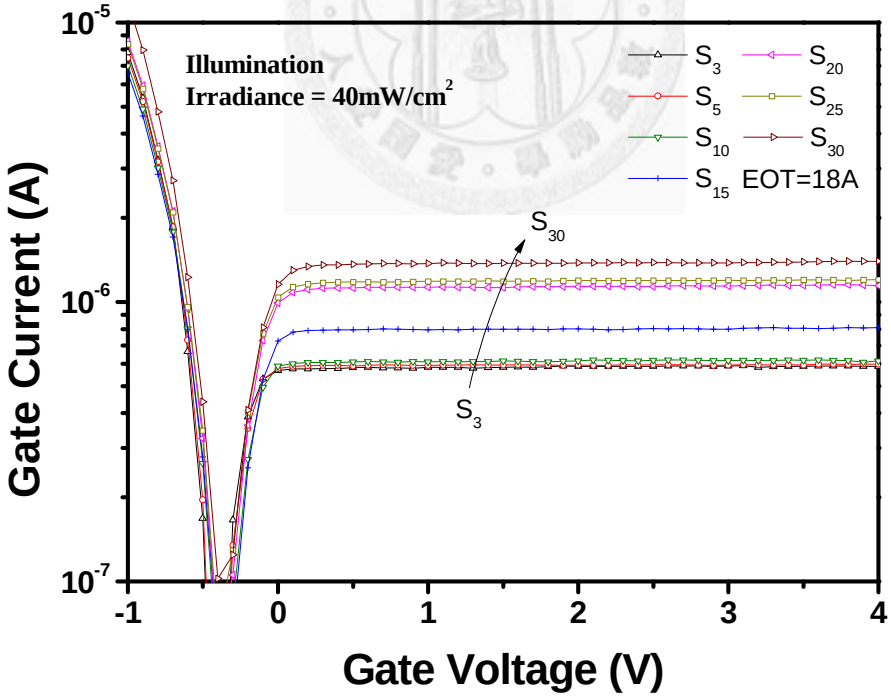
bulk & edge deep depletion

(d)

Figure 3-7 Schematic diagrams for minority carrier conduction of samples with smaller electrode separation at (a) Region I, depletion-inversion stage, (b) Region II, edge deep depletion stage, (c) Region III, front stage of bulk deep depletion, and (d) Region IV, bulk deep depletion stage. The depletion regions at edge between two electrodes are overlapped.



(a)



(b)

Figure 3-8 (a) Original and (b) local-magnified current-voltage characteristics of samples with different electrode separation under illumination.

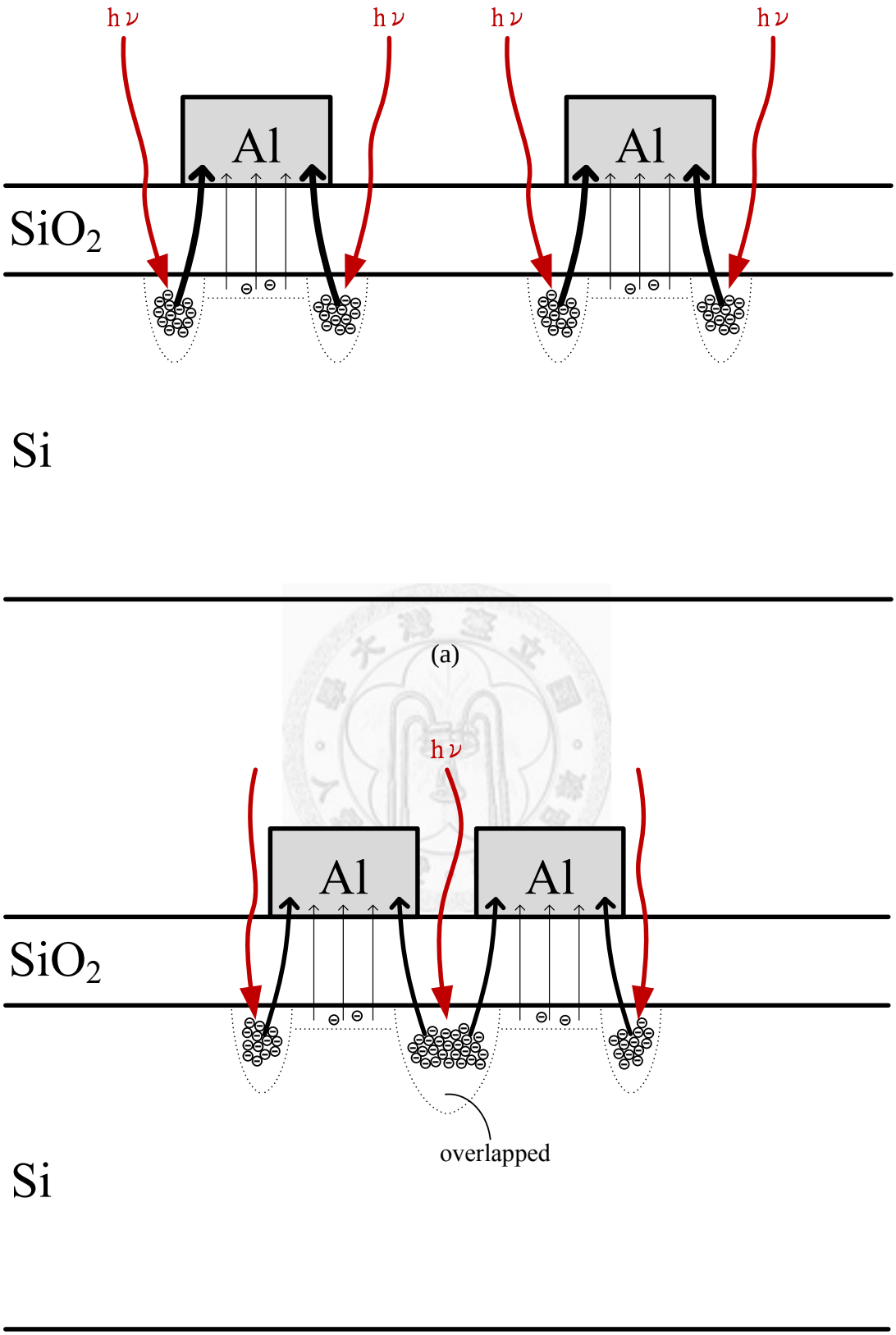


Figure 3-9 Schematic diagrams for minority carrier conduction of samples with (a) larger and (b) smaller electrode separation under illumination.

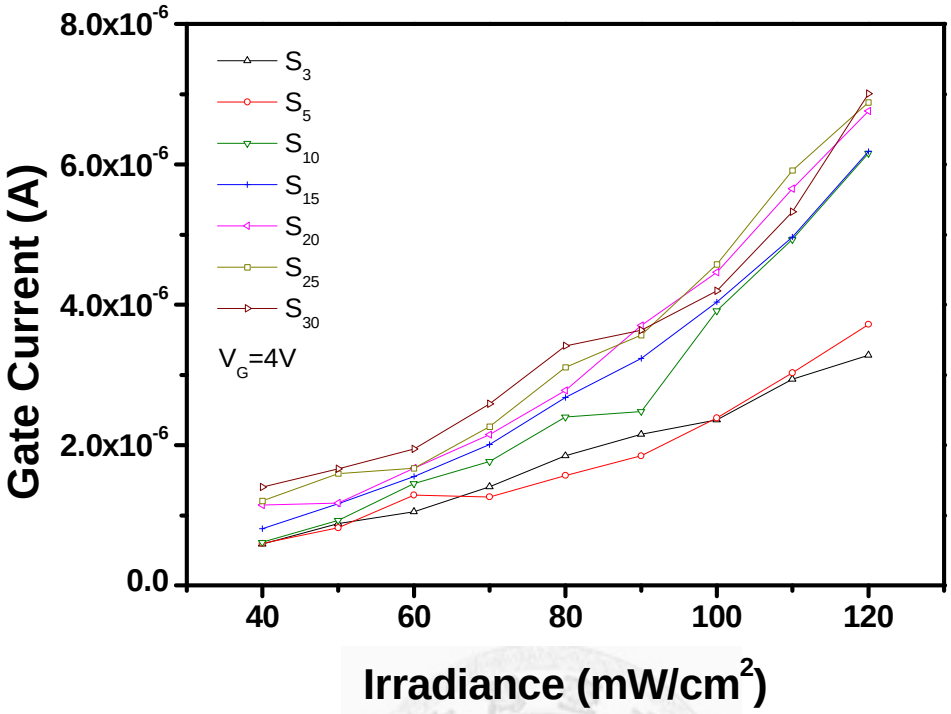


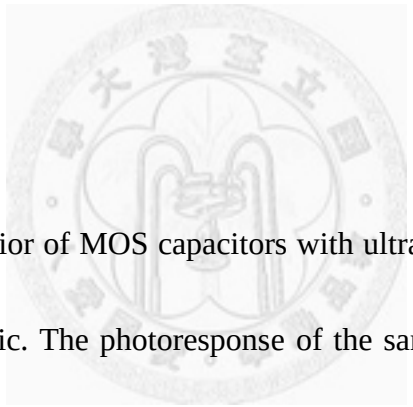
Figure 3-10 Gate current versus irradiance measured under bias of 4V for samples with different electrode separation.

Chapter 4

Conclusions and Suggestions for Future Work

4-1 Conclusions

4-2 Suggestions for Future Work



4-1 Conclusions

Deep depletion behavior of MOS capacitors with ultrathin oxides is discussed in this thesis as the main topic. The photoresponse of the samples is also examined, in order to achieve better understanding of the mechanism of the deep depletion phenomenon. In chapter 1, background knowledge about this work is introduced, including experimental setup, measurement system, and some basic physics of MOS capacitors. In chapter 2, the generation current of minority carriers is analyzed to explain why saturation of gate current and deep depletion behavior seem to occur at the same time. The geometrical perimeter of MOS capacitors is supposed to serve as the generation center of minority carriers. Enhancement of lateral nonuniformity such as illumination or decrease in oxide thickness makes the saturation current pass

through the edge of MOS capacitors more likely. In addition, due to photo-excited excess minority carriers, illumination is found to be able to postpone the occurrence of deep depletion behavior as well as saturation of gate current. In chapter 3, special patterns are designed for further characterization of deep depletion behavior. Samples with different electrode width show similar characteristics with those of MOS capacitors with simple square patterns. However, current-voltage curves of samples with different electrode separation exhibit particular transition regions during the saturation of gate currents, which is believed to result from the sharing of minority charges due to the coupling of depletion regions between adjacent electrodes. Under illumination, the transition regions disappear as the photo-exited minority carriers become sufficient.

4-2 Suggestions for Future Work

As previously mentioned, the delay of both deep depletion behavior and saturation of gate current due to illumination can serve as a basis when determining the qualities of dielectrics. However, the dark and illuminated characteristics are barely distinguished for MOS capacitors with oxide thickness around 18 Å or below. In chapter 2, only one magnitude of the light intensity is applied on the MOS capacitors when we examine the capacitance-voltage and current-voltage characteristics of the samples. It is suggested that light sources of higher intensities

may illuminate on the MOS capacitors, in order to inspect the dependence of the delay condition of deep depletion behavior on light intensity. If light source of higher intensity is confirmed to further postpone the occurrence of deep depletion behavior, qualities of thinner dielectrics can thus be determined by the aforementioned method.

In chapter 3, it is observed that samples with different electrode width lager than 10 μm do not possess particular characteristics from those of MOS capacitors with simple square patterns. In addition, the perimeters of the designed patterns are all the same, so the correlation between saturation current and perimeter has not been further assured. As a result, patterns with smaller electrode width and different perimeter may be designed in the future to continuingly investigate the scales of edge region and bulk region.

On the other hand, the oxide thickness of the samples mentioned in chapter 3 remains fixed at 18 Å. Samples with various oxide thicknesses, especially those with different electrode separation, may be fabricated so as to observe the effect of oxide thickness on the characteristics of the samples. It is conjectured that different fringing field due to various oxide thicknesses leads to dissimilar transition regions in the current-voltage curves of samples with different electrode separation.

Finally, capacitance-voltage characteristics of samples with different electrode separation under illumination have not been put into measurement yet. Although the

distribution of minority carriers as well as depletion regions becomes different, capacitance-voltage characteristics under illumination may still be helpful in creating a complete image of the behavior of depletion regions under the ultrathin oxide layers of MOS capacitors.

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