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一個使用不完全趨穩技巧伴隨著背景調整取樣時間

校正的高速導管式類比數位轉換器

A High-speed Pipelined ADC Using Incomplete-
settling Technique with Background Sampling-point
Calibration

賴傑帆

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摘要

本論文採用了不完全趨穩的技巧，提出了背景調整取樣時間校正來實現一個六位元、每秒十億次取樣的導管式類比數位轉換器。不完全趨穩的技巧伴隨著背景調整取樣時間校正能夠降低類比數位轉換器中運算放大器對於增益和頻寬的需求從而降低運算放大器的功率消耗。

本晶片使用台積電 65nm CMOS 一般製程製作。根據量測結果，在 1 GS/s 的轉換率下的 DNL 和 INL 分別為+0.72/-0.68 LSB 和+0.76/-0.68 LSB。在輸入頻率為 499.0 MHz 且在 1 GS/s 的轉換率下時，SNDR 和 SFDR 分別為 33.39 dB 和 41.03 dB。然而在輸入頻率為 9.7 MHz 且在 900 MS/s 的轉換率下時，SNDR 和 SFDR 分別為 35.17 dB 和 49.50 dB。在 1 V 的電壓和 1 GS/s 的轉換率下的功率消耗為 62 mW。全部的晶片面積大小為 0.89 mm²，然而主動電路所占的面積只有 0.30 mm²。

Abstract

This thesis adopts incomplete-settling technique and proposes background sampling-point calibration to realize 6-bit, 1GS/s pipelined ADC. Incomplete-settling technique with proposed background sampling-point calibration allows low-gain and low-bandwidth opamp to be used and lowers the power consumption of opamp.

This prototype ADC is fabricated in TSMC 65nm CMOS general-process. According to measurement results, this prototype ADC exhibits DNL of $+0.72/-0.68$ LSB and INL of $+0.76/-0.68$ LSB at sampling rate of 1 GS/s. SNDR and SFDR are 33.39 dB and 41.03 dB at 1 GS/s with 499.0 MHz input frequency. But at 900 MS/s with 9.7 MHz input frequency, SNDR and SFDR are 35.17 dB and 49.50 dB. The power consumption is 62 mW at 1 V supply voltage and 1 GS/s sampling rate. Active area is 0.30 mm^2 , and whole chip with pads occupies 0.89 mm^2 .

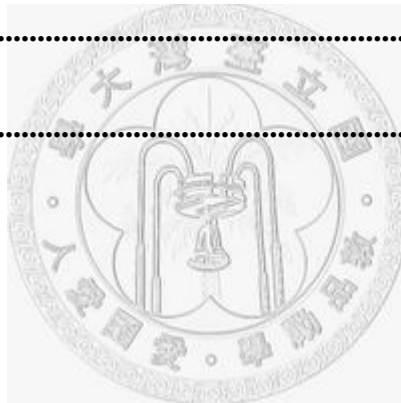
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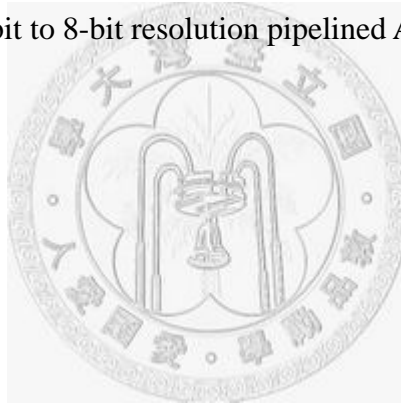
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Chapter 1 Introduction

1.1 Motivation

High-speed applications such as magnetic and optical read channels, serial-link receivers, and ultra-wideband (UWB) radios need fast ADC with low resolution. Pipelined ADC architecture has the advantages of high sampling rate and low input capacitance and is adopted in this thesis. Opamp in pipelined ADC is a key building block. However, it is also a power-hungry block. Two main approaches about opamp are researched to lower the power consumption of pipelined ADC. The first approach tries to reduce the power consumption of opamp by using circuit techniques such as incomplete-settling technique [1][2], correlated-level-shifting (CLS) technique [3], opamp-sharing technique [4], capacitor-sharing technique [5], and time-sharing technique [6]. The second approach attempts to replace opamp by introducing modified architectures such as comparator-based architecture [7], charge-pump-based architecture [8], and ring-oscillator-based architecture [9]. This thesis follows the first approach. It adopts incomplete-settling technique and proposes background sampling-point calibration to decrease the power consumption of opamp.

1.2 Thesis Organization

This thesis contains six chapters. In chapter one, it describes motivation and thesis organization. In chapter two, it gives the overview of the basic knowledge of ADC. Chapter three discusses different calibrations for incomplete-settling technique and proposed ADC architecture with some non-idealities. Chapter four introduces proposed building blocks with analysis, circuit implementation, and simulation results. Measurement results are shown in chapter five. Finally, conclusions about this thesis are made in chapter six.



Chapter 2 Fundamentals of ADC

2.1 Introduction

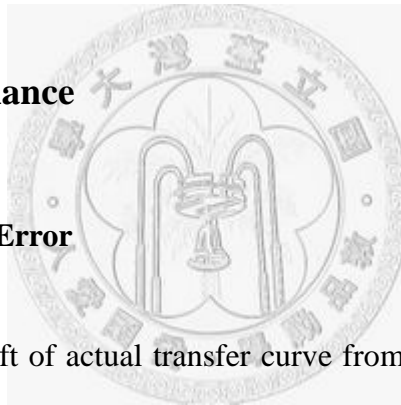
Some important performance metrics about the static and dynamic performance of ADC will be defined. And a number of ADC architectures will be described.

2.2 Performance Metrics

2.2.1 Static Performance

2.2.1.1 Offset and Gain Error

Offset error is the shift of actual transfer curve from ideal transfer curve shown in Fig. 2-1(a). And gain error is the difference of the slopes of actual transfer curve and ideal transfer curve when offset error is zero shown in Fig. 2-1(b).



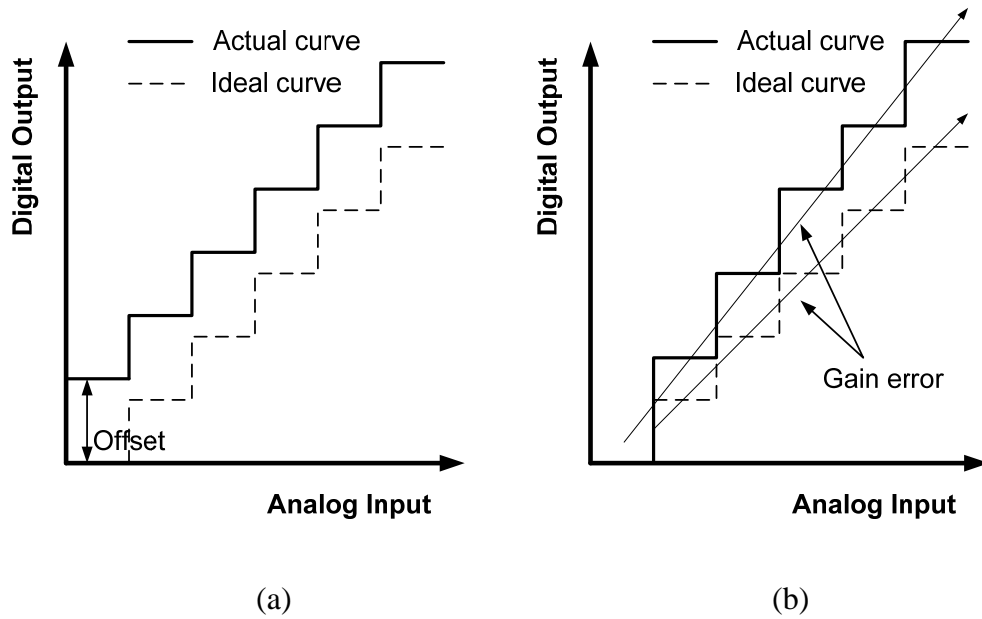


Fig. 2-1 transfer curve with (a) offset error (b) gain error

2.2.1.2 Differential and Integral Nonlinearities (DNL, INL)

Differential nonlinearity (DNL) is defined as the difference of each actual transition level width and ideal transition level width without offset and gain error.

DNL at code n is given as:

$$DNL = \frac{V_{n+1} - V_n}{V_{LSB}} - 1, \quad 0 \leq n \leq (2^N - 1) \quad (2.1)$$

where V_n is actual transition point of digital output code n , and N is the resolution of ADC. V_{LSB} is amplitude voltage of 1 LSB, so DNL is expressed by LSB.

Integral nonlinearity (INL) is defined as the deviation of actual transfer curve from an ideal straight line and is also expressed by LSB. INL at code n is said to be

the width difference of actual transition point n and ideal transition point n . Summing

up DNL from code 0 to code n is another way to evaluate INL:

$$INL(n) = \sum_{i=1}^n DNL(i) \quad (2.2)$$

DNL and INL are shown in Fig. 2-2.

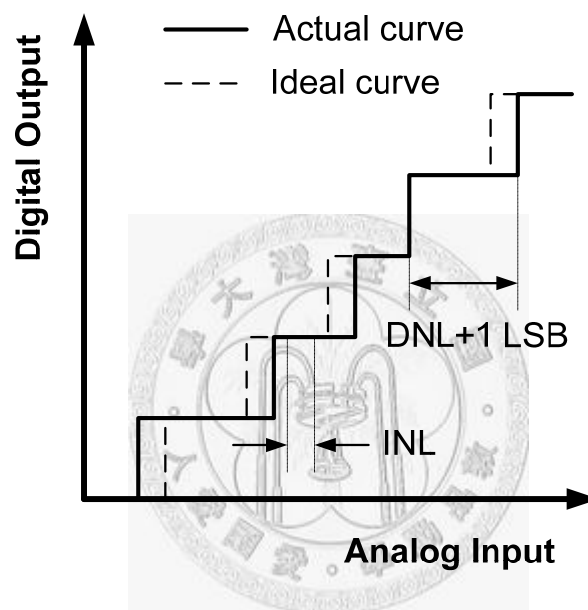


Fig. 2-2 transfer curve with DNL and INL

DNL and INL are sometimes said to be the maximum value.

2.2.2 Dynamic Performance

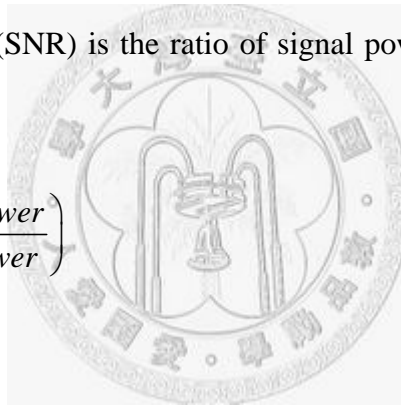
Dynamic performance is based on FFT analysis. A sine wave as the analog input of ADC is applied, and the digital output of ADC is processed by FFT analysis. The

total power of digital output can be sorted into three parts. The first part is signal power. The second part is harmonic power. The number of harmonics which are included in harmonic power depends on individual definition. The third is noise power. Noise power is calculated by subtracting signal power and harmonic power from total power.

2.2.2.1 Signal to Noise Ratio (SNR)

Signal to noise ratio (SNR) is the ratio of signal power to noise power. SNR is written as:

$$SNR|_{dB} = 10 \log \left(\frac{\text{signal power}}{\text{noise power}} \right) \quad (2.3)$$



2.2.2.2 Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of harmonic power to signal power. The first five harmonics are included in harmonic power in this thesis. THD is expressed as:

$$THD|_{dB} = 10 \log \left(\frac{\text{harmonics power}}{\text{signal power}} \right) \quad (2.4)$$

2.2.2.3 Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range (SFDR) is the ratio of signal power to the largest harmonic power. SFDR is mentioned as:

$$SFDR|_{dB} = 10 \log \left(\frac{\text{signal power}}{\text{largest harmonic power}} \right) \quad (2.5)$$

2.2.2.4 Signal to Noise and Distortion Ratio (SNDR) and Effective Number of

Bits (ENOB)

Signal to noise and distortion ratio (SNDR) is the ratio of signal power to noise power and harmonic power. SNDR is described as:

$$SNDR|_{dB} = 10 \log \left(\frac{\text{signal power}}{\text{noise power} + \text{harmonics power}} \right) \quad (2.6)$$

Effective number of bits (ENOB) is a measure based on SNDR and is calculated as:

$$ENOB|_{bit} = \frac{SNDR|_{dB} - 1.76}{6.02} \quad (2.7)$$

2.2.2.5 Figure of Merit (FoM)

Figure of Merit (FoM) is the important performance metric of ADC in terms of power, speed and accuracy. FoM is defined as:

$$FoM = \frac{Power}{2^{ENOB} \times 2f_{in}} \quad (2.8)$$

2.3 ADC Architectures

2.3.1 Flash ADC Architecture

Flash ADC architecture is shown in Fig. 2-3. It contains several $2^N - 1$ comparators where N is the resolution of ADC and a decoder. The analog input of flash ADC is compared with reference voltages generated by resistor-ladder simultaneously with the comparators. The differences of the analog input and the reference voltages are amplified to digital levels, and thermometer code is generated. Then the thermometer code is converted to binary code by the decoder. Moreover, preamplifiers are often added in front of the comparators to decrease input-referred offset. Flash ADC achieves the fastest sampling rate because of parallel processing. However, when the resolution of flash ADC increases, power and area consumption increase exponentially. Therefore, flash ADC is usually implemented in low resolution and high-speed design.

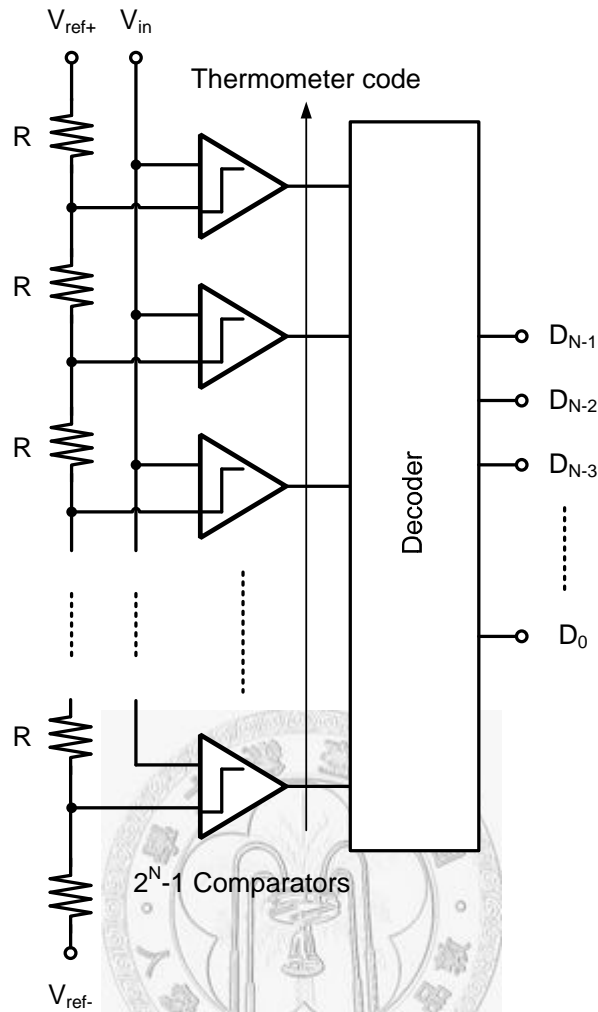


Fig. 2-3 flash ADC architecture

2.3.2 Successive-approximation ADC Architecture

Successive-approximation ADC architecture is shown in Fig. 2-4. It is composed of a front-end sample-and-hold amplifier (SHA), a comparator, a successive-approximation (SA) control logic, and a DAC. It applies binary search algorithm to resolve the digital output of successive-approximation ADC. With binary search algorithm, successive-approximation ADC halves the maximum difference of

the analog output of the SHA which is V_{SHA} and the analog output of the DAC which is V_{DAC} in each step. In the first step, the registers of the SA control logic are set 100000 for 6-bit resolution for example, and then V_{DAC} is set $\frac{V_{ref}}{2}$. The comparator compares V_{SHA} with V_{DAC} to make a decision and control the SA control logic. If V_{SHA} is larger than V_{DAC} , the register of MSB is still 1. In the second step, the registers of the SA control logic is set 110000 and the above steps are repeated. Successive-approximation ADC is N times where N is the resolution of ADC slower than flash ADC. However, offset of the comparator is independent of the linearity of successive-approximation ADC because only one comparator is used. Successive-approximation ADC is usually implemented in low-to-medium resolution and low-power design.

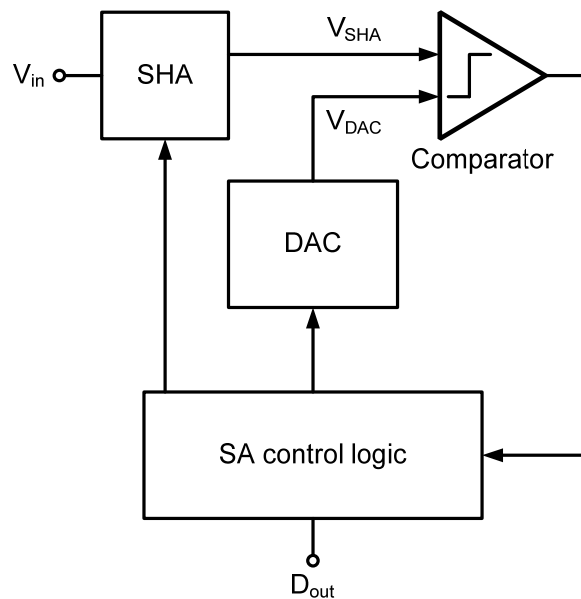


Fig. 2-4 successive-approximation ADC architecture

2.3.3 Pipelined ADC Architecture

Pipelined ADC architecture is shown in Fig. 2-5. It consists of a series of stages. Each stage is made up of a SHA, a sub-ADC, a sub-DAC, and an amplifier. It mainly operates in two phases which are amplification phase and sampling phase. When the i^{th} stage is in amplification phase, the $(i-1)^{\text{th}}$ and $(i+1)^{\text{th}}$ stages are in sampling phase, and vice versa. When the i^{th} stage is in amplification phase, assuming that the resolution of the i^{th} stage is M-bit, it generates an M-bit digital output and a residual voltage, and then the amplifier amplifies the residual voltage by 2^{M-1} times to a residue output sampled as the input of the $(i+1)^{\text{th}}$ stage. When the i^{th} stage is in sampling phase, it samples the residue output of the $(i-1)^{\text{th}}$ stage. This arrangement lets all stages of pipelined ADC work concurrently, so sampling rate is independent of the number of stages of pipelined ADC. Due to amplification between stages, critical accuracy is in the first stage, and accuracy of later stages is relaxed. Pipelined ADC is usually implemented in medium-to-high resolution and high-speed design.

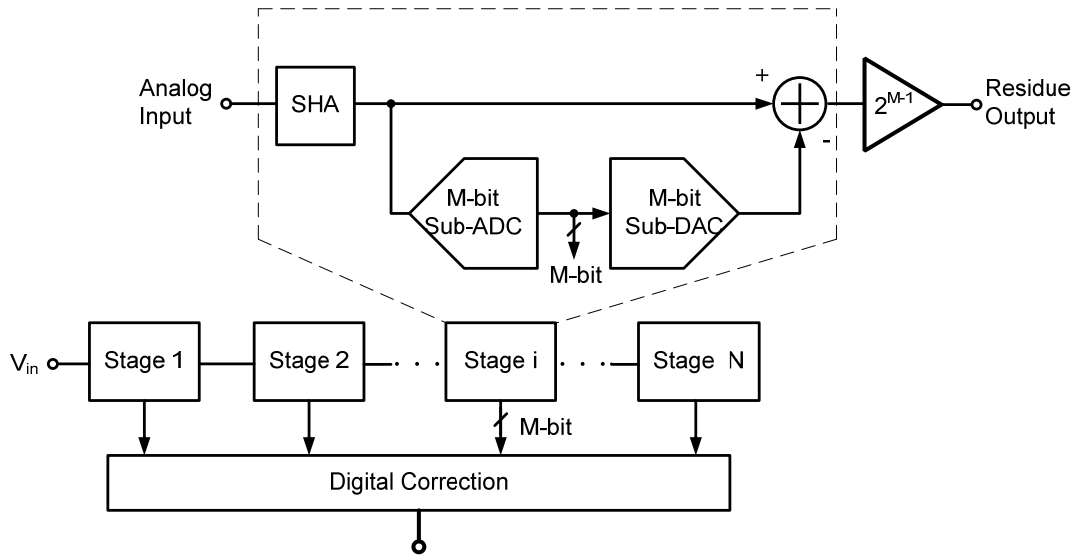


Fig. 2-5 pipelined ADC architecture

2.3.4 Continuous-time Delta-sigma ADC Architecture

Continuous-time delta-sigma ADC architecture is shown in Fig. 2-6. It is comprised of a continuous-time delta-sigma modulator and a digital decimation filter.

The continuous-time delta-sigma modulator is a feedback loop which includes a low-resolution ADC, a low-resolution DAC, and a continuous-time integrator. It adopts over-sampling and noise-shaping technique [10] to improve SNR. With over-sampling technique, the analog input of ADC is sampled with sampling rate much higher than Nyquist-rate. This spreads quantization noise power to bandwidth of sampling rate and leaves less quantization noise power in signal-band. With noise-shaping technique, the feedback loop pushes quantization noise power to high-frequency and also leaves less quantization noise power in signal-band. The

digital decimation filter removes quantization noise power out of signal-band to obtain the digital output of ADC. Continuous-time delta-sigma ADC is usually implemented in high resolution and low-power design.

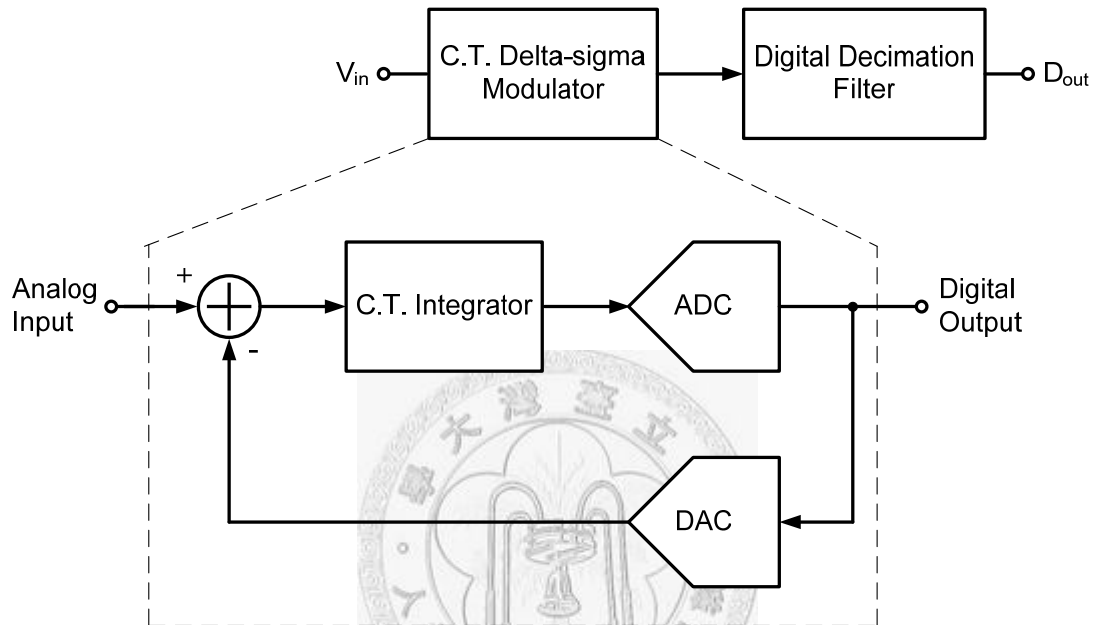


Fig. 2-6 continuous-time delta-sigma ADC architecture

2.4 Summary

First, static and dynamic performance are introduced. Static performance includes offset, gain error and DNL, and INL. Dynamic performance includes SNR, THD, SFDR, SNDR, ENOB, and FoM. Second, three ADC architectures which contains flash ADC, successive-approximation ADC, pipelined ADC, and

continuous-time delta-sigma ADC are mentioned and applied according to different applications.



Chapter 3 Proposed Background Sampling-point

Calibration for Pipelined ADC Using

Incomplete-settling Technique

3.1 Introduction

As described in 2.3.3, Fig. 3-1 shows the conventional 1.5-bit pipelined ADC i^{th} stage which contains sub-ADC and MDAC. Sub-ADC is composed of two comparators and a decoder. MDAC which realizes the function of SHA, sub-DAC, and an amplifier is composed of opamp, sampling capacitor C_s , feedback capacitor C_f , and a multiplexer. V_{in} and V_{ref} are the analog input and the reference voltage of ADC, respectively. In sampling phase, switch S_1 is on. Switches S_2 and S_3 connect the residue output $V_{out_{i-1}}$ of the $(i-1)^{th}$ stage to C_s and C_f . Then $V_{out_{i-1}}$ is sampled as the input V_{in_i} of the i^{th} stage. Sub-ADC compares $V_{out_{i-1}}$ with $\pm \frac{V_{ref}}{4}$ in the end of sampling phase to decide which voltage ($+V_{ref}$ or 0 or $-V_{ref}$) is connected to the output of the multiplexer. In amplification phase, S_1 is off. S_2 and S_3 respectively connect C_f and C_s to the outputs of opamp and the output of the multiplexer. Assuming that the system has only one pole ω_p contributed by opamp, the residue output $V_{out_i}(t)$ of the i^{th} stage is described as:

$$V_{out_i}(t) = \left(1 + \frac{C_s}{C_f}\right) \left(\frac{1}{1 + \frac{1}{A_0\beta}}\right) (1 - e^{-\frac{t}{\tau}}) \left[V_{in_i} - \left(\frac{C_s}{C_s + C_f}\right) D_i \cdot V_{ref}\right]$$

$$D_i = \begin{cases} +1, & \text{if } V_{out_i-1} > +\frac{V_{ref}}{4} \\ 0, & \text{if } +\frac{V_{ref}}{4} > V_{out_i-1} > -\frac{V_{ref}}{4} \\ -1, & \text{if } -\frac{V_{ref}}{4} > V_{out_i-1} \end{cases} \quad (3.1)$$

A_0 is dc gain of opamp, and $\beta (= \frac{C_f}{C_s + C_f + C_p})$, where C_p is the parasitic capacitance of the inputs of opamp, is feedback factor. τ is time constant and $\frac{1}{\tau}$ is closed-loop $\omega_{-3dB} (= (1 + A_0\beta)\omega_p)$. $\frac{1}{\tau}$ is equal to loop-gain unit gain bandwidth $\omega_{u_loop} (= A_0\beta\omega_p)$ if loop-gain dc gain $A_0\beta$ is much larger than 1. Fig. 3-2 shows the relation of ω_p , ω_{-3dB} , and ω_{u_loop} in Bode plot. D_i is a digital code. Usually $A_0\beta$ is much larger than 1, and (3.1) can be approximately rewritten as:

$$V_{out_i}(t) \approx \left(1 + \frac{C_s}{C_f}\right) \left(1 - \frac{1}{A_0\beta}\right) (1 - e^{-\frac{t}{\tau}}) \left[V_{in_i} - \left(\frac{C_s}{C_s + C_f}\right) D_i \cdot V_{ref}\right] \quad (3.2)$$

Assuming that C_s and C_f are matched and not taken into consideration, there are two error terms which are static error $(1 - \frac{1}{A_0\beta})$ caused by finite dc gain of opamp and dynamic error $(1 - e^{-\frac{t}{\tau}})$ caused by insufficient time. If V_{out_i} has to conform to $\frac{1}{2} LSB$ of N-bit accuracy, two limits about static error and dynamic error have to be obeyed:

static error limit:

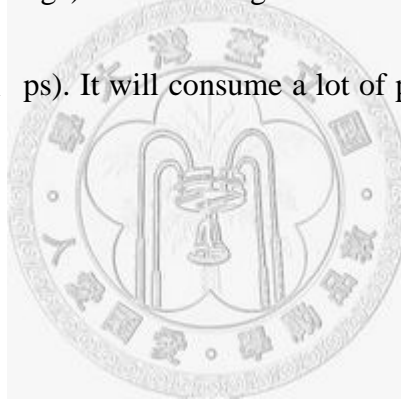
$$\varepsilon_s = \frac{1}{A_0\beta} < \frac{1}{2^{N+1}} \quad (3.3)$$

dynamic error limit:

$$\varepsilon_d = e^{-\frac{t_s}{\tau}} < \frac{1}{2^{N+1}} \quad (3.4)$$

where t_s is settling time which corresponds to $\frac{1}{2}LSB$ of N-bit accuracy.

For example, for 6-bit resolution, 1GS/s sampling rate design with conventional 1.5-bit stages, assuming that t_s is 200 ps, the requirements of the first stage (N=5 because 1 bit is already resolved by the first stage) for A_0 of opamp is about 42.1 dB ($\beta \approx \frac{1}{2}$ because of 1.5-bit stage) and for unit gain bandwidth $\omega_u (= A_0\omega_p)$ of opamp is about 6.6 GHz ($\tau = 48.1$ ps). It will consume a lot of power for opamp to achieve the above requirements.



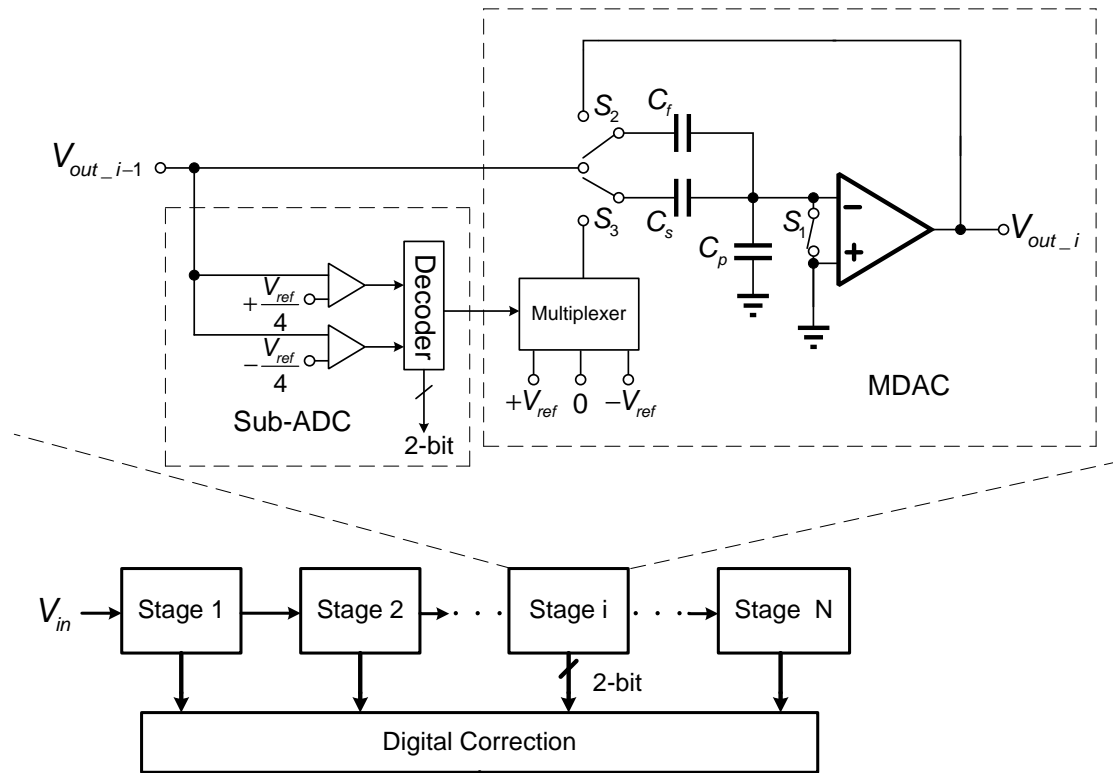


Fig. 3-1 conventional 1.5-bit pipelined ADC i^{th} stage

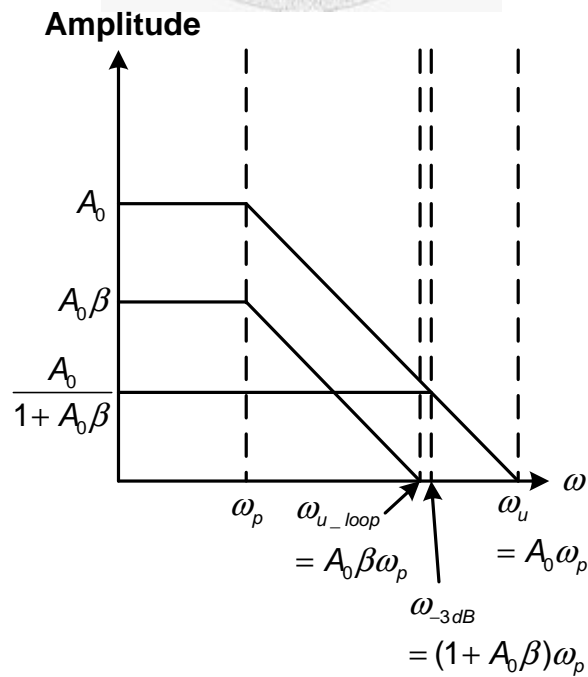


Fig. 3-2 relation of ω_p , ω_{-3dB} , and ω_{u_loop} in Bode plot

3.2 Incomplete-settling Technique

3.2.1 Concept of Incomplete-settling Technique

Two parameters G_{fix} and $G_{eff}(t)$ are introduced here. G_{fix} represents interstage gain defined by hardware implementation ($G_{fix} = 1 + \frac{C_s}{C_f}$ when conventional closed-loop 1.5-bit stage is used for example). $G_{eff}(t)$ represents actual interstage gain at time t . Moreover, G_{fix} and $G_{eff}(t)$ are related in closed-loop topology:

$$G_{eff}(t) \equiv G_{fix} \left(\frac{1}{1 + \frac{1}{A_0 \beta}} \right) (1 - e^{-\frac{t}{\tau}}) \quad (3.5)$$

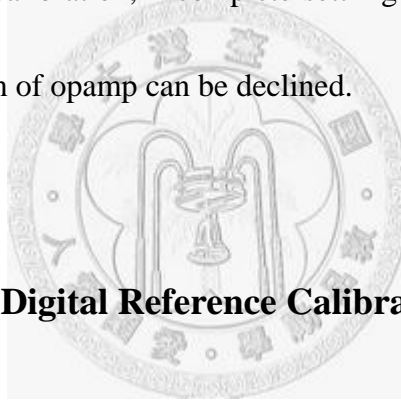
Conventionally, $G_{eff}(t_s)$ is equal to G_{fix} with small static and dynamic error limited by (3.3) and (3.4). Opamp dc gain A_0 and unit gain bandwidth $\omega_u (= A_0 \omega_p)$ requirements are based on (3.3) and (3.4):

$$A_0 > \frac{2^{N+1}}{\beta} \quad (3.6)$$

$$\omega_u = A_0 \omega_p \approx \frac{1}{\beta \tau} > \frac{(N+1) \ln 2}{\beta t_s} \quad (3.7)$$

If the requirements for opamp A_0 and ω_u can be reduced, the power consumption of opamp can hence be reduced. This is the concept of incomplete-settling technique [1][2]. Incomplete-settling technique ignores these requirements and uses opamp

which has smaller A_0 and ω_u than (3.6) and (3.7) to lower the power consumption of opamp. However, from (3.3), if A_0 decreases, ε_s will increase. Similarly, from (3.4), if ω_u decreases, ε_d will increase (because $\varepsilon_d = e^{-\frac{t_s}{\tau}} \approx e^{-\omega_{u_loop} t_s} = e^{-\beta \omega_u t_s}$), too. That is, ε_s and ε_d will become larger and larger with the decrease of A_0 and ω_u . Also, from (3.5), $G_{eff}(t_s)$ will become smaller and smaller than G_{fix} . If the big difference between G_{fix} and $G_{eff}(t_s)$ can be compensated during ADC conversion by digital reference calibration [1], digital signal processing calibration [2], and proposed sampling-point calibration, incomplete-settling technique can be adopted, and the power consumption of opamp can be declined.



3.2.2 Prior Work 1: Digital Reference Calibration

In prior work 1 [1], 1.5-bit stage at each stage uses closed-loop topology where G_{fix} is 2 and $G_{eff}(t_s)$ is 1.6 (no need to be precise because settling behavior changes with PVT and digital reference calibration can accommodate this variation) at fixed t_s . Tuning the reference voltage of each stage is one method to compensate the difference between G_{fix} and $G_{eff}(t_s)$. There is interstage gain error defined as

$\frac{G_{eff}(t_s)}{G_{fix}} (= \frac{1.6}{2} = 0.8)$ at each stage shown in Fig. 3-3 (a), and the reference voltage of

each stage also multiplies 0.8, no error will be induced during ADC conversion shown

in Fig. 3-3 (b).

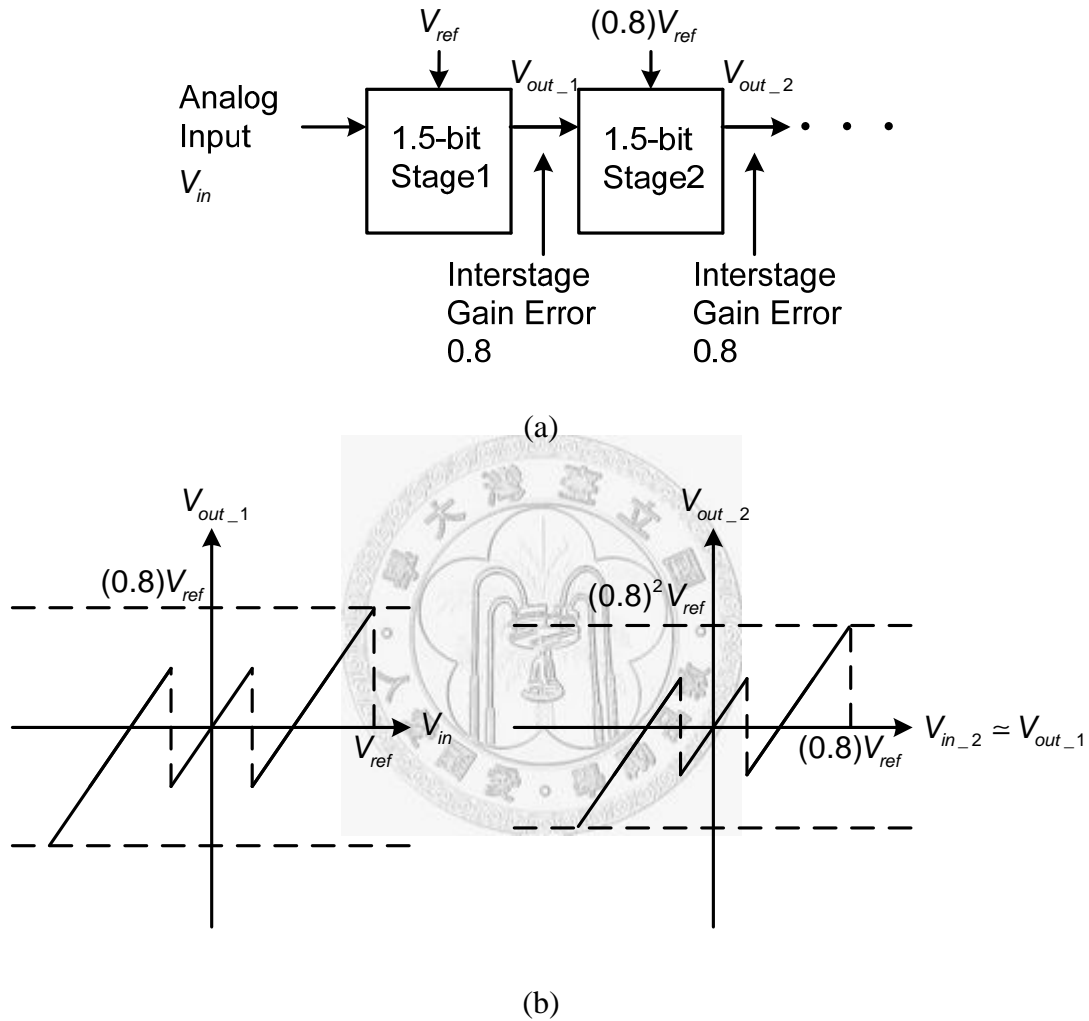
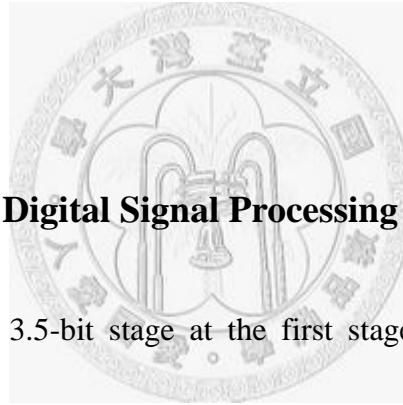


Fig. 3-3 (a) interstage gain error 0.8 at each stage (b) reference voltage of each stage

multiplies 0.8

In practice, the reference voltage of each stage can be adjusted independently to avoid mismatches between stages and achieve better performance. Digital reference

calibration based on maximizing SNDR is adopted to find the right reference voltage which corresponds to each stage. However, there are some disadvantages. First, because of interstage gain error, the reference voltage of each stage shrinks stage by stage. Assuming that noise except quantization noise remains unchanged, the effect of the noise is bigger than convention, so ADC performance cannot be as good as convention. Second, the calibration is so complex as to be not embedded on-chip. Third, the calibration is foreground and cannot adapt to environment variation continuously.



3.2.3 Prior Work 2: Digital Signal Processing Calibration

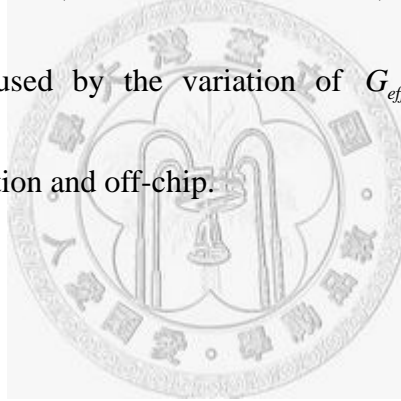
In prior work 2 [2], 3.5-bit stage at the first stage uses open-loop topology. Because of open-loop topology, assuming that the system has only one pole $\omega_p (= \frac{1}{R_0 C_L})$ where R_0 is output resistance and C_L is load capacitor, and the pole is contributed by opamp, the residue output V_{out_i} of the i^{th} stage in amplification phase is described as:

$$V_{out_i}(t) = A_0(1 - e^{\frac{-t}{\tau_{open}}})[V_{in_i} - D_i \cdot \frac{V_{ref}}{2}] \quad (3.8)$$

where $\frac{1}{\tau_{open}}$ is ω_p . G_{fix} ($G_{fix} = A_0$ in open-loop topology) and $G_{eff}(t)$ are related in open-loop topology:

$$G_{eff}(t) \equiv G_{fix} (1 - e^{-\frac{t}{\tau_{open}}}) \quad (3.9)$$

G_{fix} is bigger than 8 and ideally $G_{eff}(t_s)$ is 8 (no need to be precise because settling behavior changes with PVT and digital signal processing calibration can accommodate this variation) at fixed t_s . The reason why G_{fix} is bigger than 8 is to create a cross point where $G_{eff}(t_s)$ is exactly 8 shown in Fig. 3-4. Because settling behavior varies with PVT, $G_{eff}(t_s)$ may not be 8 at fixed t_s . Digital signal processing calibration which directly processes the digital output of ADC is adopted to compensate linear error (linear because from (3.8) and (3.9), $G_{eff}(t_s)$ is independent of V_{in_i}) caused by the variation of $G_{eff}(t_s)$. The calibration has disadvantages of complication and off-chip.



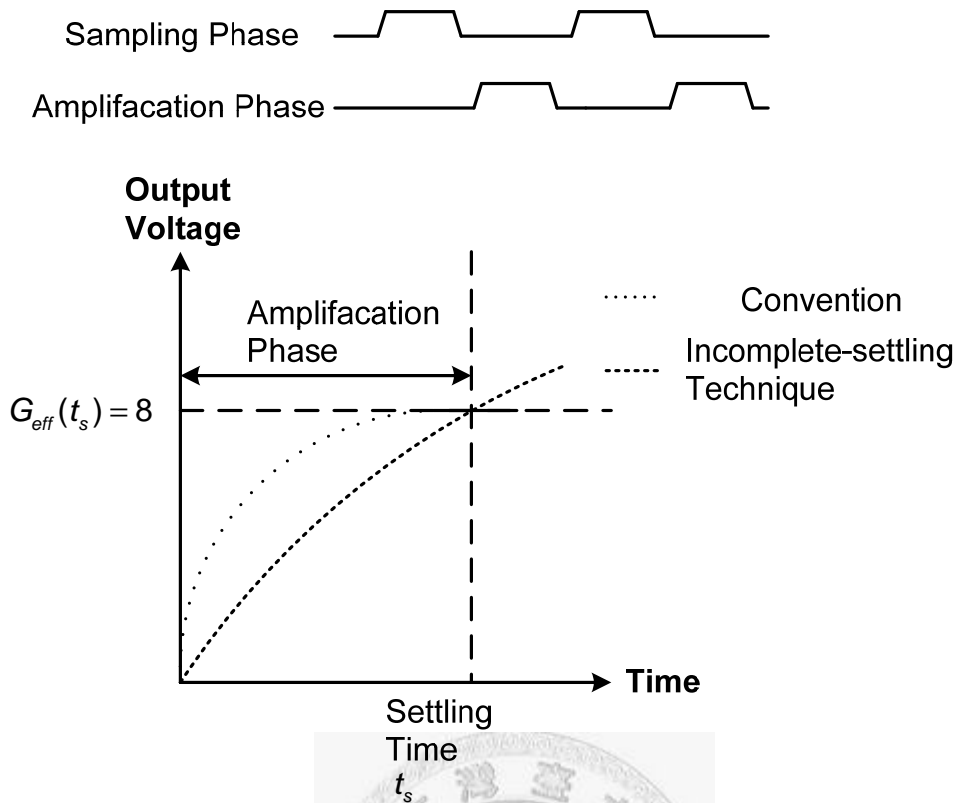


Fig. 3-4 G_{fix} is bigger than 8 is to create a cross point where $G_{eff}(t_s)$ is exactly 8

3.3 Proposed Pipelined ADC Architecture and Background Sampling-point Calibration

3.3.1 Pipelined ADC Architecture

Fig. 3-5 shows 6-bit, 1GS/s pipelined ADC architecture. It is composed of four identical 2-bit stages and a 2-bit flash at the end for ADC conversion. The digital codes resolved by each stage are aligned and added to obtain the digital output of ADC. Calibration circuits which contain two replica stages, a calibration comparator

with offset calibration, and a digital loop filter are added for background sampling-point calibration. Why two rather than one replica stage is used is according to analysis later. The replica stages are the same as those stages for ADC conversion. Moreover, a global clock generator which produces clock phases is shared among all the stages.

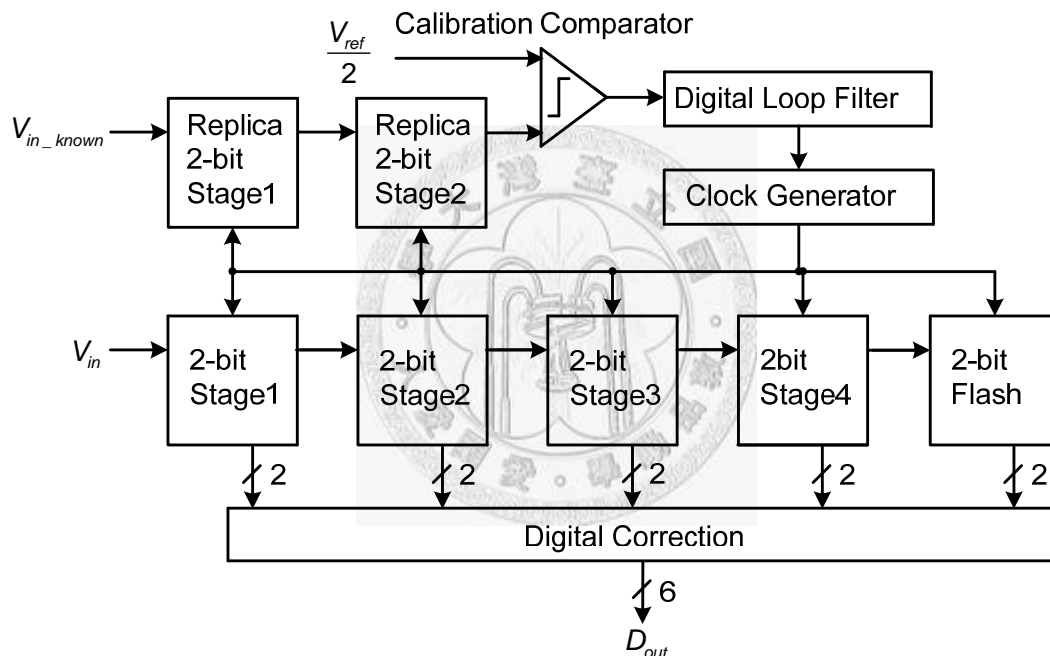


Fig. 3-5 ADC architecture with background sampling-point calibration

3.3.2 Background Sampling-point Calibration

All the stages use incomplete-settling technique with closed-loop topology. From (3.5), there are some parameters such as G_{fix} , β , A_0 , τ , and t_s chosen to tune

$G_{eff}(t_s)$. First, since G_{fix} is roughly equal to $\frac{1}{\beta}$ (because $G_{fix} = 1 + \frac{C_s}{C_f}$ and

$\frac{1}{\beta} = \frac{C_s + C_f + C_p}{C_f}$ when conventional closed-loop 1.5-bit stage is always used for

example in this section), tuning G_{fix} and β is considered together. G_{fix} and β

are related to capacitor ratio [11]. The variable capacitor ratio increases circuit

complexity and parasitic capacitance in the signal path of MDAC due to additional

switches for tuning, and this decreases sampling rate. Second, tuning A_0 is

considered. A_0 is tuned by changing the bias point of opamp [12]. Also, the variable

bias point rises circuit complexity and parasitic capacitance in the signal path of

MDAC. Third, tuning τ is considered. Because τ is $\frac{1}{\omega_{-3dB}} (= \frac{1}{(1 + A_0\beta)\omega_p})$, τ

can be tuned by tuning A_0 and β considered above. Fourth, tuning t_s is

considered. t_s is tuned by adding delay elements with variable delay into clock

generator. That is, sampling-point can be adjusted. No extra circuit is required in the

signal path of MDAC, and this achieves fast sampling rate. Besides, the tuning range

of $G_{eff}(t_s)$ is wider by altering sampling-point than the capacitor ratio or the bias

point of opamp with less circuit. Finally, G_{fix} is 16 and $G_{eff}(t_s)$ is 2 according to

analysis later. Although settling behavior varies with PVT, sampling-point can be

adjusted to let $G_{eff}(t_s)$ be 2 shown in Fig. 3-6.

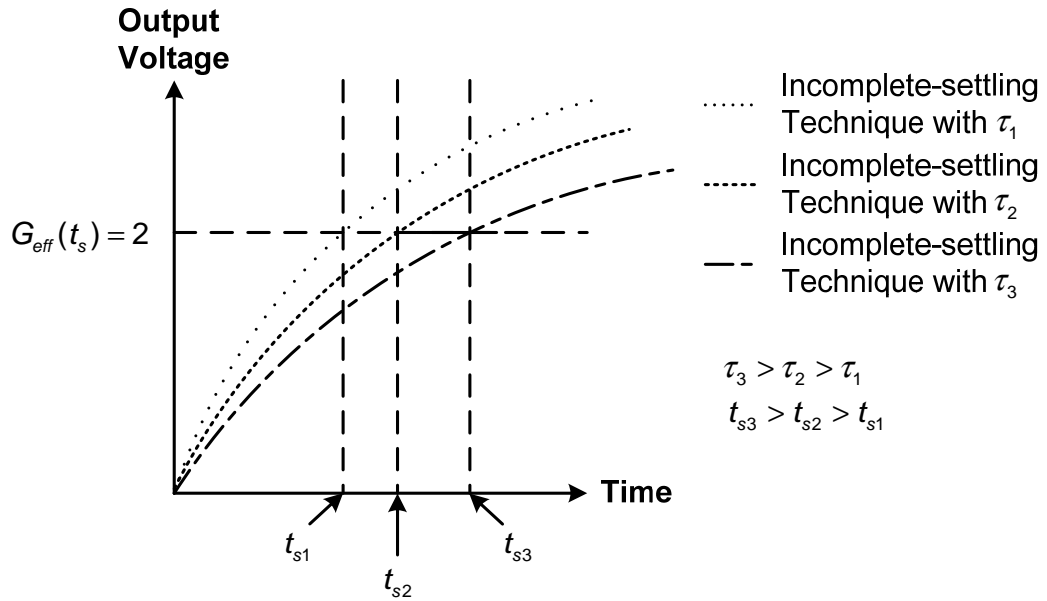
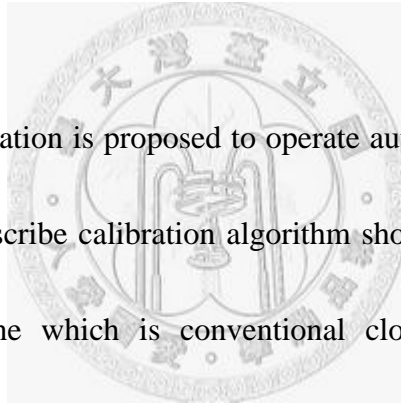


Fig. 3-6 sampling-point is adjusted to let $G_{eff}(t_s)$ be 2



Sampling-point calibration is proposed to operate automatically with the help of calibration circuits (To describe calibration algorithm shown in Fig. 3-7, two replica stages are reduced to one which is conventional closed-loop 1.5-bit stage for simplicity for example in this section). Before the beginning of sampling-point calibration, a calibration comparator is calibrated to eliminate offset, and then sampling-point calibration starts. First, a known analog input V_{in_known} set $\frac{V_{ref}}{4}$ is sampled by the replica stage. After being amplified by the replica stage, the residue output $V_{out_replica}(t_s)$ of the replica stage at t_s is compared with an analog value set $\frac{V_{ref}}{2}$ with the calibration comparator. $\frac{V_{ref}}{2}$ corresponds to $\frac{V_{ref}}{4}$, assuming that $G_{eff}(t_s)$ is 2. If $V_{out_replica}(t_s)$ is larger than $\frac{V_{ref}}{2}$, or in other words, $G_{eff}(t_s)$ is larger than 2, sampling-point is adjusted to let t_s and $G_{eff}(t_s)$ decrease, and vice

versa. Finally, $G_{eff}(t_s)$ of all the stages is 2 at decided sampling-point. Because the replica stage is independent of those stages for ADC conversion, sampling-point calibration is background and never stops.

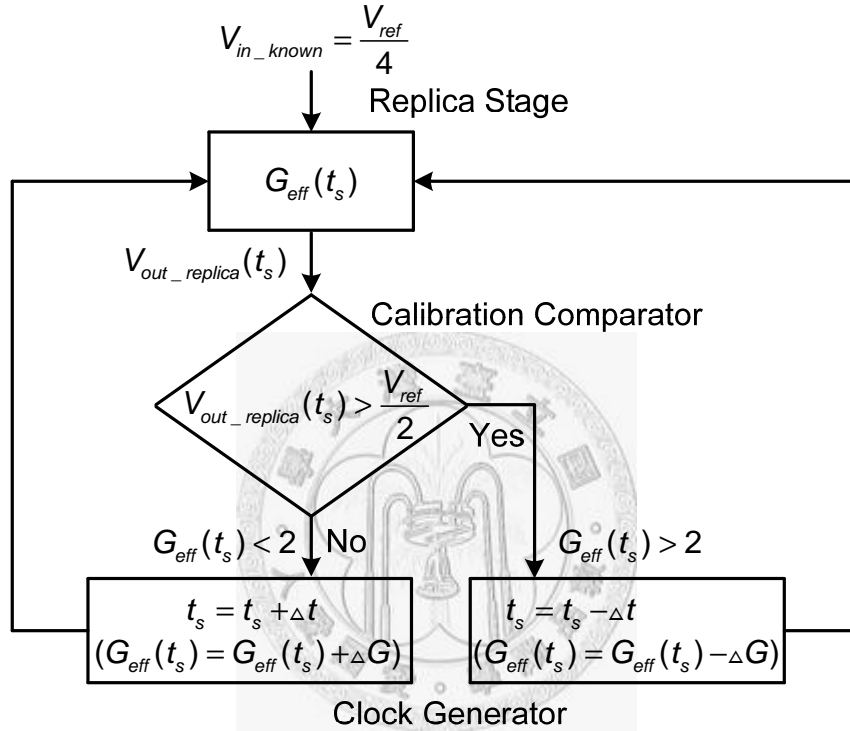


Fig. 3-7 sampling-point calibration algorithm

3.4 Non-Idealities of Background Sampling-point

Calibration

Non-idealities of sampling-point calibration are discussed in terms of either voltage or gain. In terms of voltage, if the residue output $V_{out_i}(t)$ of the i^{th} stage

want to satisfy $\frac{1}{2}LSB$ of N-bit accuracy, the voltage error of $V_{out_i}(t)$ caused by separate non-idealities is required to be less than $\frac{V_{ref}}{2^{N+1}}$. In terms of gain, Fig. 3-8 shows SNDR v.s. interstage gain $G_{eff}(t_s)$ in behavior simulation. $G_{eff}(t_s)$ from 1.90 to 2.07 ensures maximum reduction by 3 dB from ideal SNDR of 37.88(= 6.02 · 6 + 1.76) dB of 6-bit ADC. That is, the stage gain error of each stage caused by separate non-idealities should be less than 0.07 to obtain SNDR of 34.88(= 6.02 · 6 + 1.76 – 3 = 37.88 – 3) dB above in behavior simulation.

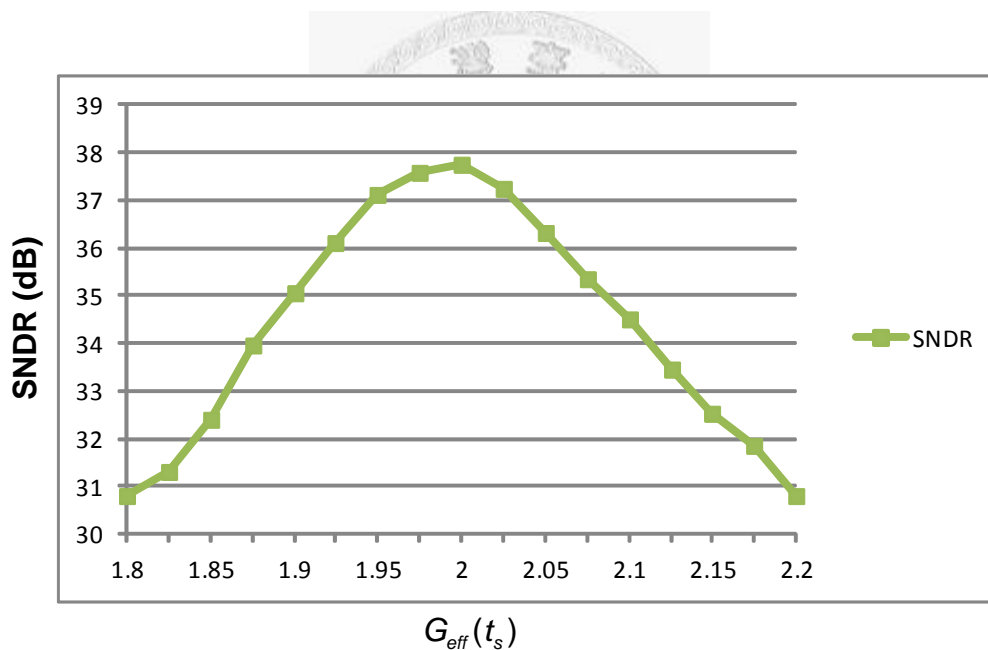


Fig. 3-8 SNDR v.s. interstage gain $G_{eff}(t_s)$ in behavior simulation

3.4.1 Opamp Slewing and DC Gain, Unit Gain Bandwidth

Variation with Output Swing

Incomplete-settling technique is based on linear amplification. However, there are two sources which cause non-linear amplification. First, opamp slewing is one source. Opamp slewing happens when the voltage difference of the inputs of opamp exceed $1.4 V_{ov}$ [13] where V_{ov} is the overdrive voltage of the input differential pair of opamp. Opamp slewing is most likely to occur in the beginning of amplification phase (ϕ_2). Fig. 3-9 (a) and (b) show that conventional 1.5-bit MDAC is in sampling phase (ϕ_1) and in the beginning of ϕ_2 , respectively. The resultant initial voltage difference ΔV_x of the inputs of opamp in the beginning of ϕ_2 is calculated by charge conservation [1] (In the end of ϕ_1 , charge is $2C_u V_{in_i}$. In the beginning of ϕ_2 , charge is $C_u (D_i \cdot V_{ref} - \Delta V_x) + (C_{eq} + C_p)(-\Delta V_x)$):

$$2C_u V_{in_i} = C_u (D_i \cdot V_{ref} - \Delta V_x) + (C_{eq} + C_p)(-\Delta V_x) \quad (3.10)$$

where V_{in_i} is the input of the i^{th} stage, C_u is the capacitor value of C_s and C_f ,

C_L is load capacitor, C_{eq} is $\frac{C_u C_L}{C_u + C_L}$ which is series connection of C_u and C_L ,

and C_p is the parasitic capacitance of the inputs of opamp.

(3.10) is rearranged as:

$$\Delta V_x = \frac{-2C_u V_{in_i} + C_u D_i \cdot V_{ref}}{C_u + C_{eq} + C_p} \quad (3.11)$$

And ΔV_x is required to be less than $1.4 V_{ov}$, no matter what V_{in_i} is to ensure that non-linear amplification will not take place. For example, assuming that V_{ov} is 100 mV, ΔV_x should be less than 140 mV for all input range.

Second, opamp dc gain A_0 and unit gain bandwidth $\omega_u (= A_0 \omega_p)$ variation with output swing are another source. From (3.1), $(1 + \frac{C_s}{C_f})$ is replaced with G_{fix} , and $(\frac{C_s}{C_s + C_f})$ is replaced with $\frac{1}{2}$ for generalization. (3.1) is rewritten as:

$$V_{out_i}(t) = G_{fix} \left(\frac{1}{1 + \frac{1}{A_0 \beta}} \right) (1 - e^{-\frac{t}{\tau}}) (V_{in_i} - D_i \cdot \frac{V_{ref}}{2}) \quad (3.12)$$

A_0 and $\tau (= \frac{1}{(1 + A_0 \beta) \omega_p})$ ideally are constants with output swing to guarantee linear amplification. However, in practice, A_0 and τ will change with output swing and are represented as A_0' and τ' for discrimination:

$$A_0' = A_0 - \Delta A_0 [V_{out_i}(t)] \quad (3.13)$$

$$\tau' = \tau + \Delta \tau [V_{out_i}(t)] \quad (3.14)$$

where A_0 and τ denote that A_0' and τ' have 0 output swing. $V_{out_swing_i}(t)$ stands for the output of the i^{th} stage with A_0' and τ' and is expressed as:

$$V_{out_swing_i}(t) = G_{fix} \left(\frac{1}{1 + \frac{1}{A_0' \beta}} \right) (1 - e^{-\frac{t}{\tau'}}) (V_{in_i} - D_i \cdot \frac{V_{ref}}{2}) \quad (3.15)$$

Output voltage error ΔV_y due to A_0 and τ variation with output swing, for given t_s , is written as:

$$\Delta V_y = V_{out_swing_i}(t) - V_{out_i}(t) \Big|_{t=t_s} \quad (3.16)$$

If V_{out_i} want to fulfill $\frac{1}{2}LSB$ of N-bit accuracy, ΔV_y is required to be less than $\frac{V_{ref}}{2^{N+1}}$ no matter what V_{in_i} is. For example, for 6-bit resolution design with conventional 1.5-bit stages, ΔV_y of the first stage (N=5 because 1 bit is already resolved by the first stage) should be less than $\frac{V_{ref}}{2^{5+1}}$ for all input range.

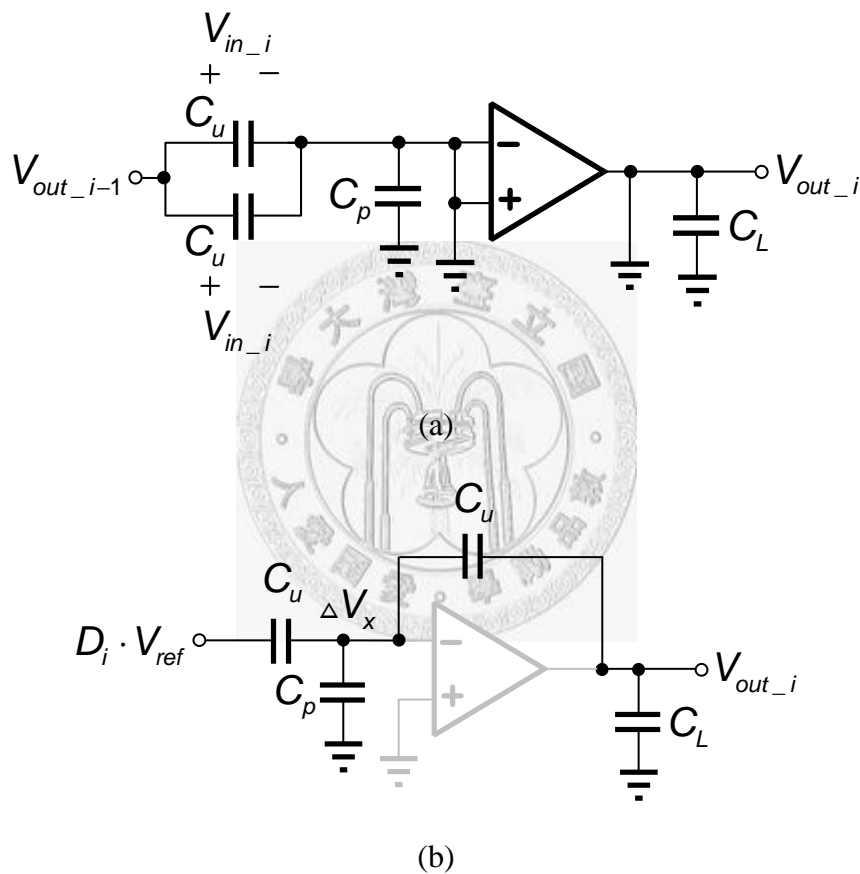


Fig. 3-9 MDAC in (a) sampling phase (b) the beginning of amplification phase

3.4.2 Discrete Sampling-point and Clock Jitter

Because of discrete sampling-point which is controlled by digital control bits, the resolution of sampling-point need to be fine enough to achieve the required resolution of ADC with the existence of clock jitter. (3.5) is differentiated with time and expressed as:

$$\begin{aligned} \frac{dG_{eff}(t)}{dt} &= G_{fix} \left(\frac{1}{1 + \frac{1}{A_0\beta}} \right) \left(\frac{1}{\tau} e^{-\frac{t}{\tau}} \right) \\ &= \frac{G_{fix} \left(\frac{1}{1 + \frac{1}{A_0\beta}} \right) - G_{eff}(t)}{\tau} \end{aligned} \quad (3.17)$$

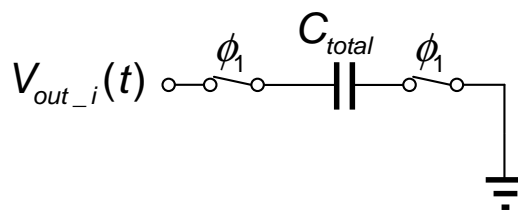
If there is sampling-point variation Δt introduced by discrete control and clock jitter, for given ideal sampling-point t_c where $G_{eff}(t_{ideal})$ is exactly 2, stage gain error ΔG_x is expressed as:

$$\begin{aligned} \Delta G_x &= \left. \frac{dG_{eff}(t)}{dt} \right|_{t=t_{ideal}} \Delta t = \frac{G_{fix} \left(\frac{1}{1 + \frac{1}{A_0\beta}} \right) - G_{eff}(t_{ideal})}{\tau} \Delta t \\ &= \frac{G_{fix} \left(\frac{1}{1 + \frac{1}{A_0\beta}} \right) - 2}{\tau} \Delta t \end{aligned} \quad (3.18)$$

From (3.18), the finer the resolution of sampling-point is and the bigger t_{ideal} is, the smaller ΔG_x is. For example, refer to Fig. 3-8, ΔG_x of each stage should be less than 0.07 to get SNDR of $34.88(=6.02 \cdot 6 + 1.76 - 3 = 37.88 - 3)$ dB above of 6-bit ADC.

3.4.3 Sampling Attenuation

Conventionally, the output of the i^{th} stage settles to required accuracy when the $(i+1)^{th}$ stage samples. That is, when the $(i+1)^{th}$ stage samples, the output of the i^{th} stage is almost a dc value. Therefore, RC delay in the sampling network of the $(i+1)^{th}$ stage does not cause error and the input of the $(i+1)^{th}$ stage which samples the output of the i^{th} stage is equal to that of the i^{th} stage. However, because of incomplete-settling technique, the output of the i^{th} stage is still amplifying when the $(i+1)^{th}$ stage samples, and RC delay in the sampling network of the $(i+1)^{th}$ stage will cause sampling attenuation G_y between the output of the i^{th} stage and the input of the $(i+1)^{th}$ stage. The sampling network of each stage and equivalent model in ϕ_1 is shown in Fig. 3-10 (a) and (b).



(a)

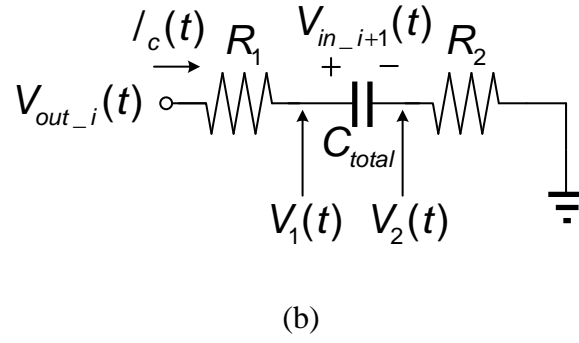


Fig. 3-10 (a) sampling network (b) equivalent model

where C_{total} is total capacitors for sampling ($C_{total} = C_s + C_f$ which is shunt connection of C_s and C_f with conventional 1.5-bit MDAC for example), R_1 and R_2 are the turn-on resistance of sampling switches, and $V_{in_i}(t)$, $V_1(t)$, $V_2(t)$, and $I_c(t)$ are voltage difference across C_{total} , voltage at the bottom-plate of C_{total} , voltage at the top-plate of C_{total} , and the current which flows through C_{total} of the $(i+1)^{th}$ stage during sampling phase of the $(i+1)^{th}$ stage, respectively.

Taylor series of $e^{-\frac{t}{\tau}}$ is mentioned as:

$$e^{-\frac{t}{\tau}} = 1 + \left(-\frac{t}{\tau}\right) + \frac{1}{2}\left(\frac{t^2}{\tau^2}\right) + \frac{1}{6}\left(-\frac{t^3}{\tau^3}\right) + \dots \quad (3.19)$$

If $\frac{t}{\tau}$ is much less than 1, (3.19) is approximately rewritten as:

$$e^{-\frac{t}{\tau}} \approx 1 + \left(-\frac{t}{\tau}\right) \quad (3.20)$$

From (3.20), (3.12) is replaced as:

$$V_{out_i}(t) = \gamma t \quad (3.21)$$

where γ is $G_{fix} \left(\frac{1}{1 + \frac{1}{A_0 \beta}} \right) \left(\frac{1}{\tau} \right) (V_{in_i} - D_i \cdot \frac{V_{ref}}{2})$.

$V_1(t)$, $V_2(t)$, and $I_c(t)$ are related:

$$I_c(t) = C_{total} \frac{d(V_1(t) - V_2(t))}{dt} = \frac{V_{out_i}(t) - V_1(t)}{R_1} = \frac{V_2(t)}{R_2} \quad (3.22)$$

with initial condition:

$$V_1(t=0) = V_2(t=0) = 0 \quad (3.23)$$

$V_1(t)$, $V_2(t)$, and thus $V_{in_i+1}(t)$ are calculated from (3.21) to (3.23) and given as:

$$V_1(t) = \gamma t + (-\gamma R_1 C_{total}) (1 - e^{-\frac{t}{\tau_s}}) \quad (3.24)$$

$$V_2(t) = \frac{R_2}{R_1} \left[\gamma R_1 C_{total} (1 - e^{-\frac{t}{\tau_s}}) \right] \quad (3.25)$$

$$V_{in_i+1}(t) = V_1(t) - V_2(t) = \gamma t \left[1 - \frac{\tau_s}{t} (1 - e^{-\frac{t}{\tau_s}}) \right] \quad (3.26)$$

where τ_s is $(R_1 + R_2)C_{total}$.

G_y is defined as the ratio of the input of the $(i+1)^{th}$ stage to the output of the i^{th}

stage, for given t_s :

$$G_y = \frac{V_{in_i+1}(t)}{V_{out_i}(t)} \Big|_{t=t_s} = 1 - \frac{\tau_s}{t_s} (1 - e^{-\frac{t_s}{\tau_s}}) \quad (3.27)$$

From (3.27), assuming that t_s is much larger than τ_s , (3.27) is about expressed as:

$$G_y \approx 1 - \frac{\tau_s}{t_s} \quad (3.28)$$

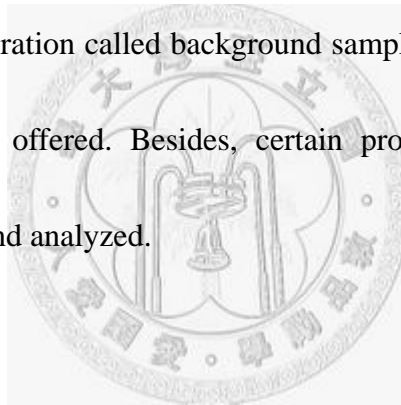
From (3.28), the smaller τ_s are, the smaller G_y deviates from ideal 1. For example,

if G_y is required be larger than 0.95, assuming that t_s is 200 ps, τ_s is 10 ps. This

satisfies the assumption which is that t_s is much larger than τ_s . Assuming that C_{total} is 160 fF, $R_1 + R_2$ which is series connection of R_1 and R_2 should be less than 63 Ω .

3.5 Summary

Incomplete-settling technique is introduced to overcome some limits with conventional approach. Several calibrations with incomplete-settling technique are compared, and a new calibration called background sampling-point calibration with a number of advantages is offered. Besides, certain problems about the proposed calibration are discussed and analyzed.

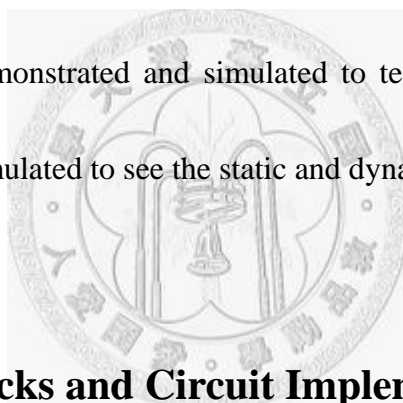


Chapter 4 Proposed Building Blocks and Circuit

Implementation

4.1 Introduction

Refer to Fig. 3-1 and 3-5, the building blocks which contain MDAC, sub-ADC, a clock generator, and calibration circuits of ADC are discussed. The architectures of the building blocks are analyzed and chosen. The practical circuit implementation of the building blocks is demonstrated and simulated to test and verify analysis, too. Finally, overall ADC is simulated to see the static and dynamic performance of ADC.



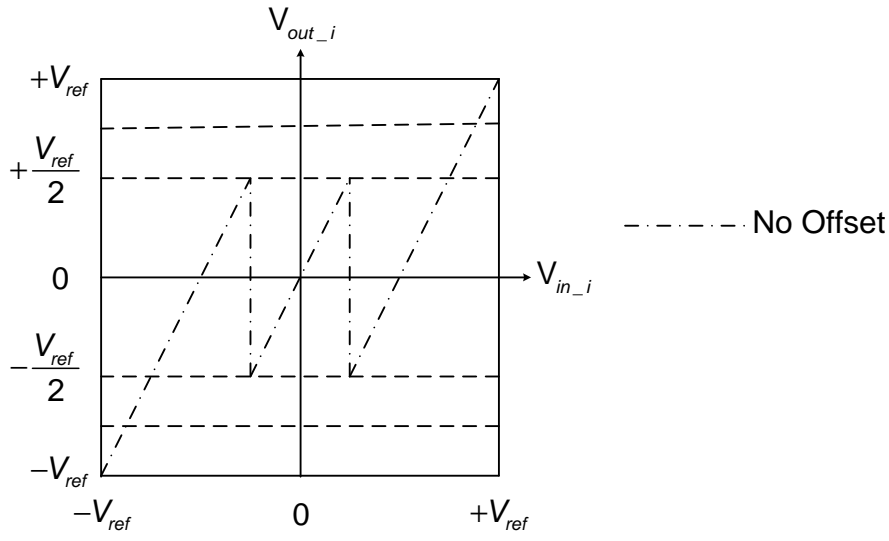
4.2 Building Blocks and Circuit Implementation

4.2.1 MDAC

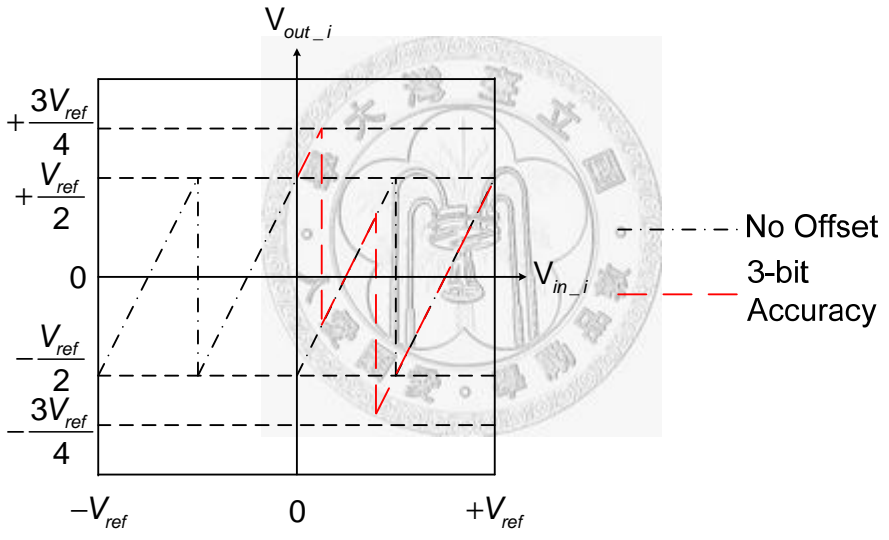
4.2.1.1 Folded-Residue

As described in 3.4.1, non-linear amplification is caused by opamp slewing and dc gain A_o , unit gain bandwidth $\omega_u (= A_o \omega_p)$ variation with output swing. From (3.11), ΔV_x is proportional to V_{in_i} which samples V_{out_i-1} . If the maximum output swing of each stage can be reduced, ΔV_x can be reduced, too. That is, opamp

slewing is more impossible to occur. Moreover, A_0 and $\tau(= \frac{1}{(1 + A_0\beta)\omega_p})$ variation are less severe because of the reduced maximum output swing. Therefore, folded-residue technique [14] is adopted to reduce the maximum output swing. Fig. 4-1 (a) shows residue plot of conventional 1.5-bit stage. The maximum output swing is $\pm V_{ref}$. By adding an additional comparator to each conventional 1.5-bit stage, folded-residue technique can be realized to reduce the maximum output swing to $\pm \frac{V_{ref}}{2}$, assuming that every comparator in each stage has no offset. Even if the comparators in each stage are designed to achieve maximum $\pm \frac{V_{ref}}{8}$ offset, or 3-bit accuracy, the maximum output swing is limited within $\pm \frac{3V_{ref}}{4}$. Residue plot of 2-bit stage with folded-residue technique which uses comparators without offset and with maximum $\pm \frac{V_{ref}}{8}$ offset is shown in Fig. 4-1 (b). Folded residue technique reduces the maximum output swing to ensure more linear amplification at the cost of an additional comparator to each stage.



(a)



(b)

Fig. 4-1 residue plot of (a) conventional 1.5-bit stage (b) 2-bit stage with folded-residue technique which uses comparators without offset and with maximum

$$\pm \frac{V_{ref}}{8} \text{ offset}$$

4.2.1.2 Amplification Multiple

MDAC with incomplete-settling technique adopts 2-bit and flip-around architecture to achieve larger feedback factor β and faster speed. Assuming that sampling capacitors C_s and feedback capacitor C_f are matched, the residue output $V_{out_i}(t)$ of the i^{th} stage is described as:

$$V_{out_i}(t) = G_{fix} \left(\frac{1}{1 + \frac{1}{A_0\beta}} \right) (1 - e^{-\frac{t}{\tau}}) \left(V_{in_i} - D_{1_i} \cdot \frac{V_{ref}}{2} - D_{2_i} \cdot \frac{V_{ref}}{4} \right)$$

$$D_{1_i}, D_{2_i} = \begin{cases} +1, +1 & \text{if } V_{out_i-1} > +\frac{V_{ref}}{2} \\ 0, +1 & \text{if } +\frac{V_{ref}}{2} > V_{out_i-1} > 0 \\ 0, -1 & \text{if } 0 > V_{out_i-1} > -\frac{V_{ref}}{2} \\ -1, -1 & \text{if } -\frac{V_{ref}}{2} > V_{out_i-1} \end{cases} \quad (4.1)$$

where D_{1_i} and D_{2_i} are digital codes. To realize (4.1), Fig. 4-2 shows the block diagram of MDAC of each stage (single-ended version for simplicity but fully-differential actual). It contains opamp, C_s , and C_f . C_s and C_f have the same capacitor value C_u . In sampling phase (ϕ_1), the residue output $V_{out_i-1}(t)$ of the $(i-1)^{th}$ stage is sampled as the input V_{in_i} of the i^{th} stage, and in amplification phase (ϕ_2), charge transfers to realize plus or minus to reference voltages and amplification.

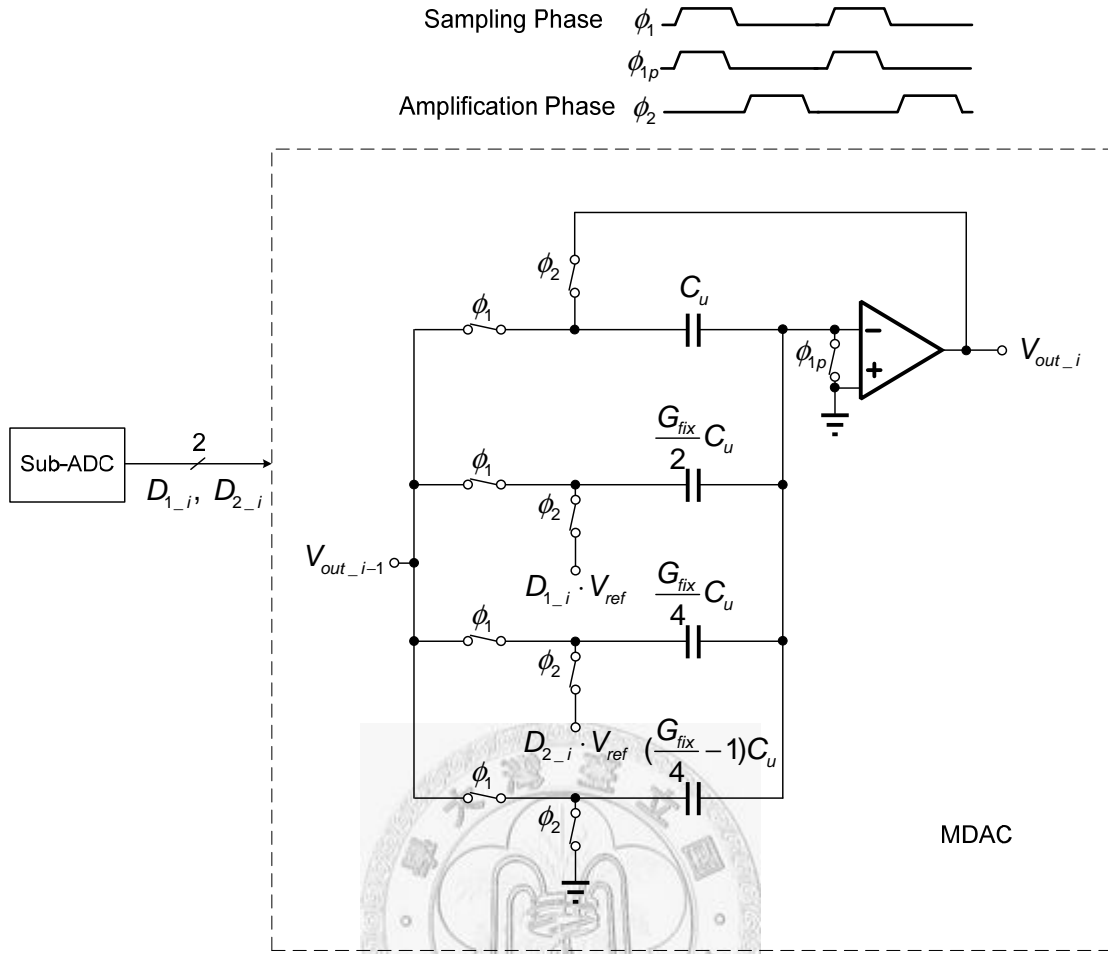


Fig. 4-2 block diagram of MDAC

Assuming that opamp with single stage has dc gain A_0 and a pole $\omega_p (= \frac{1}{R_0 C_L})$ where R_0 is output resistance and C_L is load capacitor which contains the capacitor seen by the outputs of opamp of this stage ($1 \cdot C_u$) and the capacitors for sampling of next stage in amplification phase of this stage ($G_{fix} \cdot C_u$), R_0 and C_L are described as:

$$R_0 = \frac{A_0}{g_m} \quad (4.2)$$

$$C_L \approx (1 + G_{fix}) C_u \quad (4.3)$$

where g_m is transconductance of the input differential pair of opamp. From (4.2) and

(4.3), closed-loop $\omega_{-3dB} (= \frac{1}{\tau})$ is mentioned as:

$$\begin{aligned} \frac{1}{\tau} &= (1 + A_0\beta)\omega_p \\ &= (1 + A_0\beta)\left(\frac{1}{R_0C_L}\right) \\ &= (1 + A_0\beta)\left[\frac{g_m}{A_0(1 + G_{fix})C_u}\right] \end{aligned} \quad (4.4)$$

$\frac{1}{\beta}$ is roughly equal to G_{fix} , and from (4.4), (3.5) is rewritten as:

$$G_{eff}(t_s) = G_{fix} \left(\frac{1}{1 + \frac{G_{fix}}{A_0}} \right) \left\{ 1 - e^{-t_s \left(1 + \frac{A_0}{G_{fix}}\right) \left[\frac{g_m}{A_0(1 + G_{fix})C_u}\right]} \right\} \quad (4.5)$$

With reasonable assumption where t_s is 200 ps for 1GS/s sampling rate, C_u is chosen 10 fF for 6-bit matching, and g_m is 10 mS, $G_{eff}(t_s)$ can be expressed as a function of A_0 with different G_{fix} . G_{fix} is a multiple of 4 from (4.1). Normalized G_{norm} where maximum $G_{eff}(t_s)$ is set 1 is shown in Fig. 4-3. Under the same assumption, the larger G_{norm} is, the faster the speed of amplification is. Refer to Fig. 4-3, G_{norm} is a maximum when G_{fix} is 12 or 16, and G_{fix} is chosen 16.

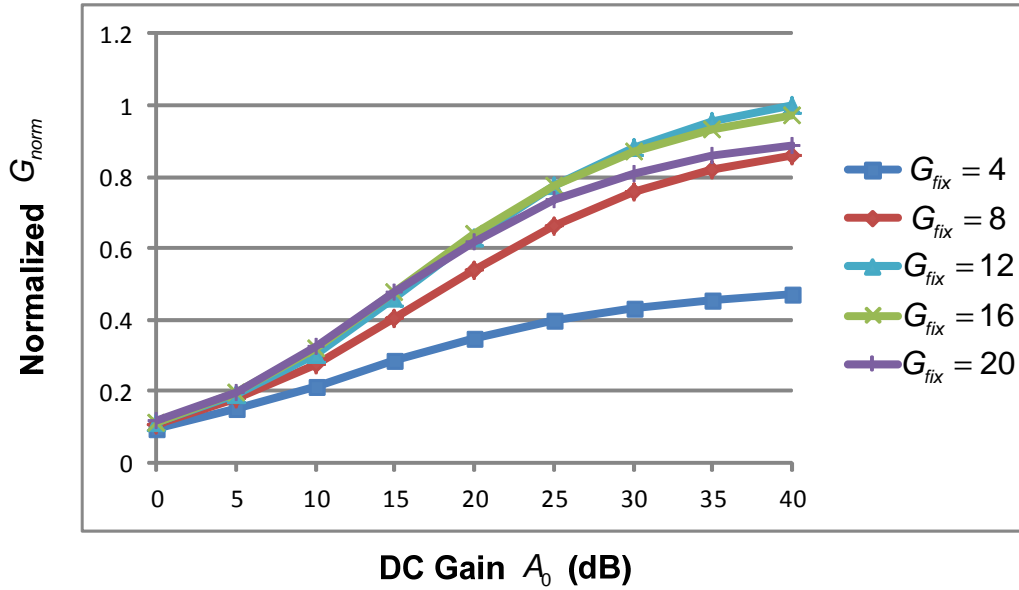
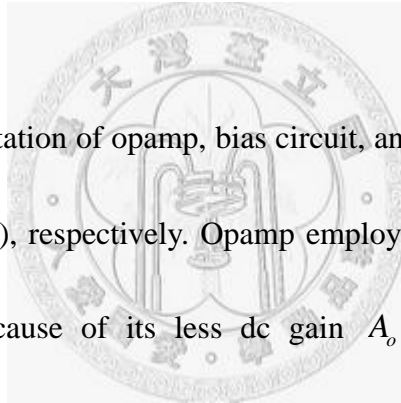


Fig. 4-3 normalized G_{norm} is expressed as a function of A_0 with different G_{fix}



The circuit implementation of opamp, bias circuit, and CMFB circuits are shown in Fig. 4-4 (a), (b), and (c), respectively. Opamp employs two-stage topology rather than single-stage one because of its less dc gain A_0 and unit gain bandwidth $\omega_u (= A_0 \omega_p)$ variation with output swing. Bias circuit undergoes the same condition as opamp. V_{cmi} is the common-mode voltage of the inputs of opamp. CMFB circuit use switched-capacitor topology owing to the existence of non-overlapping phases used in pipelined ADC architecture. There are two CMFB circuits for the outputs of the first and the second stage of opamp, respectively. V_{cm} is the common-mode voltage of the outputs of the second stage of opamp.

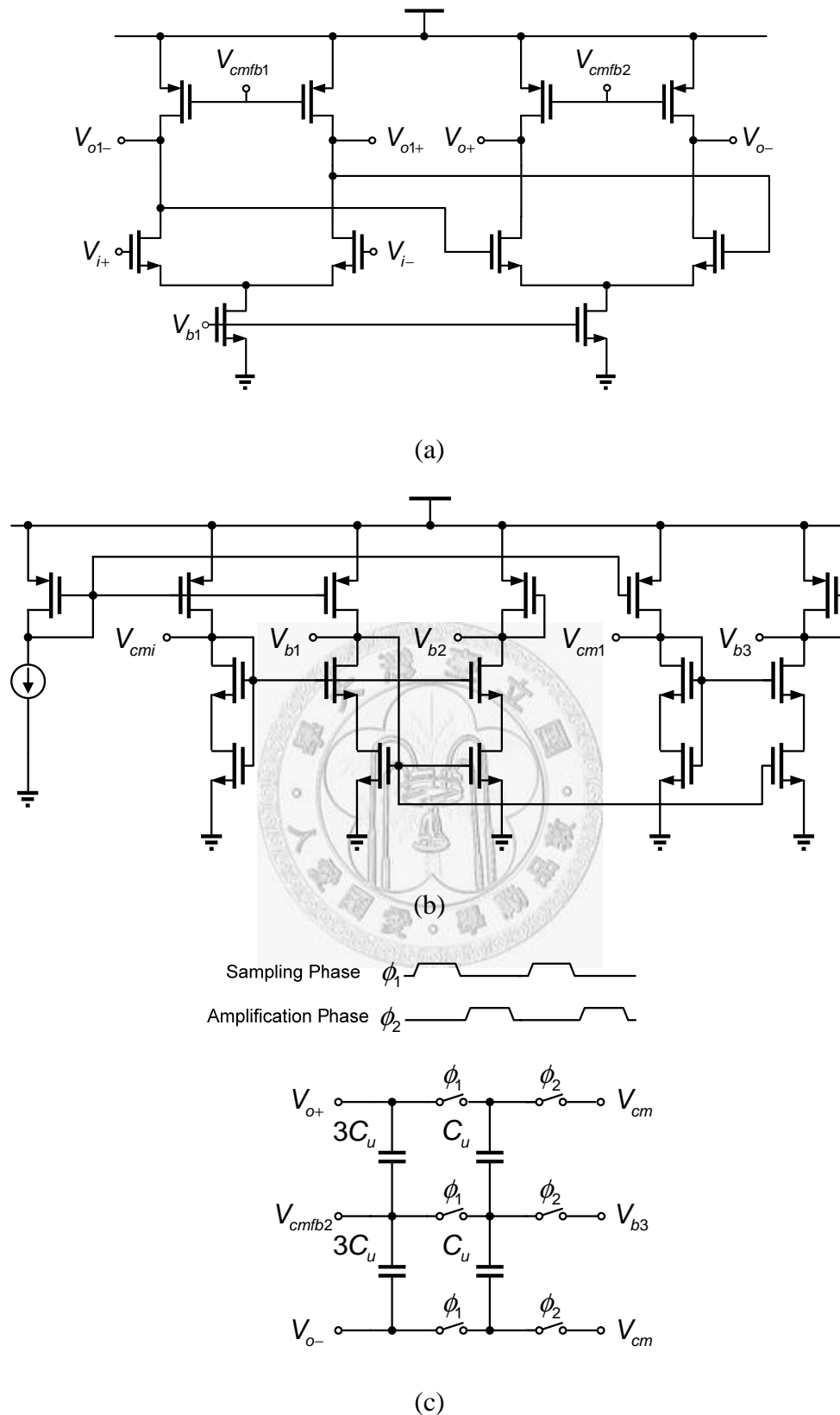


Fig. 4-4 circuit implementation of (a) opamp (b) bias circuit (c) CMFB circuit

Fig. 4-5 shows the ac analysis of MDAC and opamp when output swing is 0 in post-simulation. Opamp dc gain is 29.1 dB, and loop-gain dc gain is 2.3 dB. Loop-gain phase margin is 125.9 degree. Each opamp consumes 4.5 mW, and input-referred offset of opamp is $\pm 15\text{ mV}$ (3σ) in post-simulation.

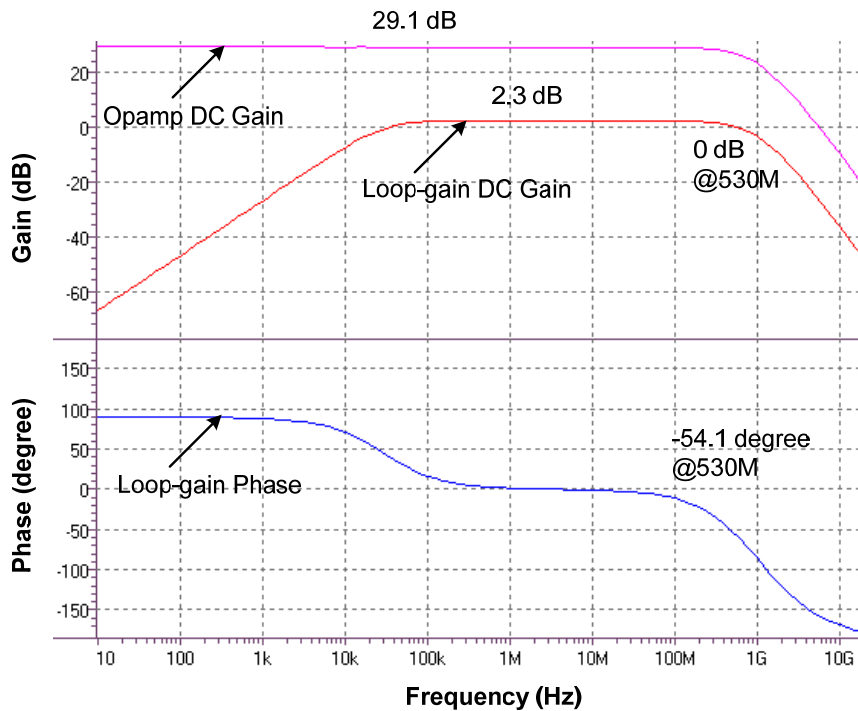


Fig. 4-5 ac analysis of MDAC and opamp when output swing is 0

As described in 3.4.1, opamp slewing will cause non-linear amplification and should be avoided. Fig. 4-6 shows ΔV_x for all input range when V_{ref} is 250 mV in post-simulation. The overdrive voltage V_{ov} of the input differential pair of opamp is set 100 mV in post-simulation. Refer to Fig. 4-6, ΔV_x is much smaller than $1.4 V_{ov}$ ($=140\text{ mV}$). Therefore, opamp slewing will not take place.

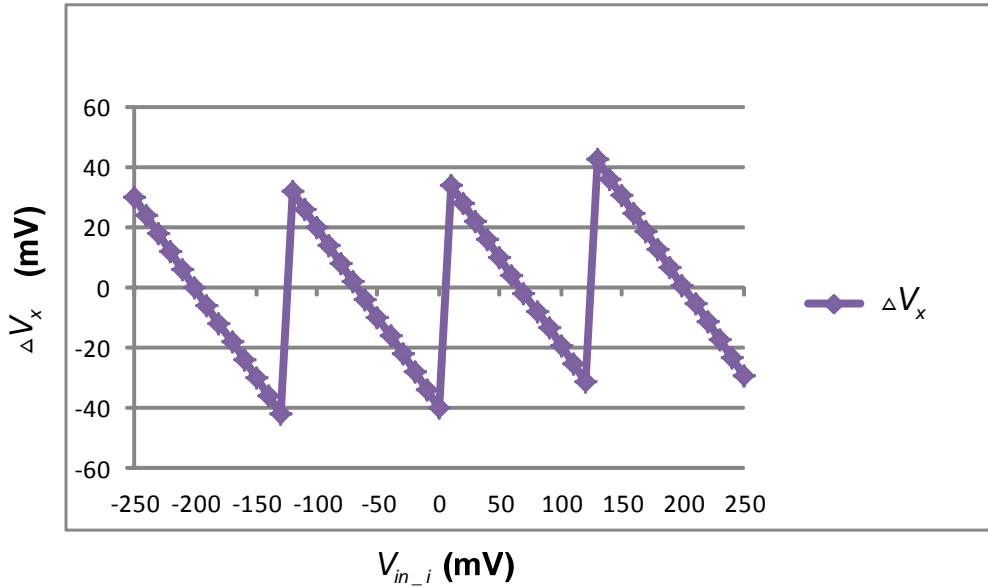
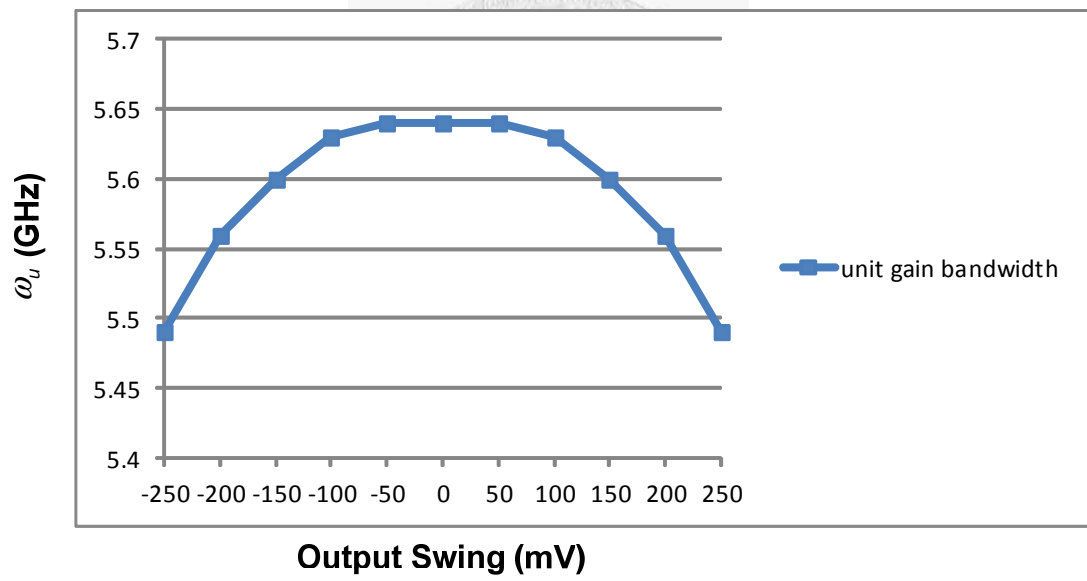
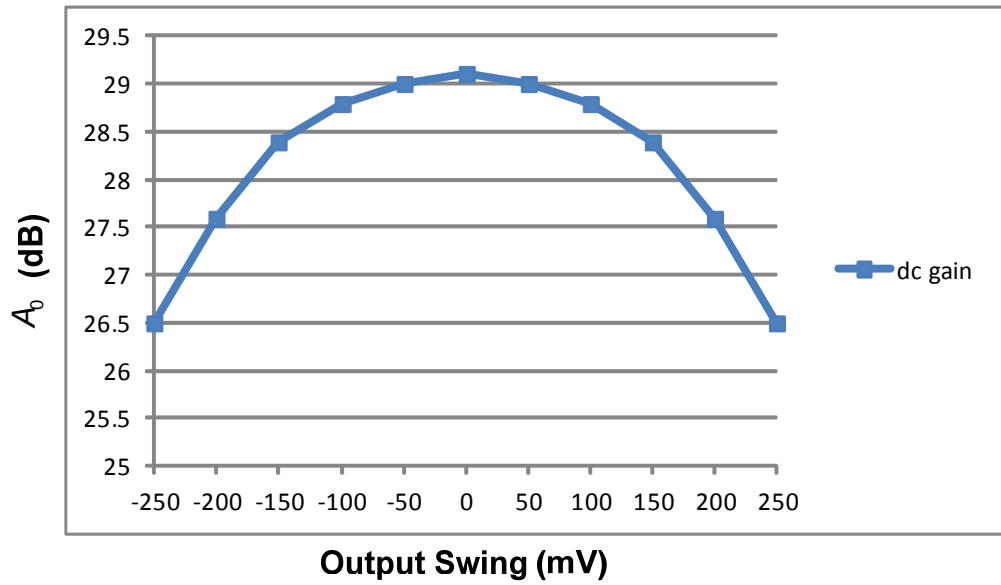
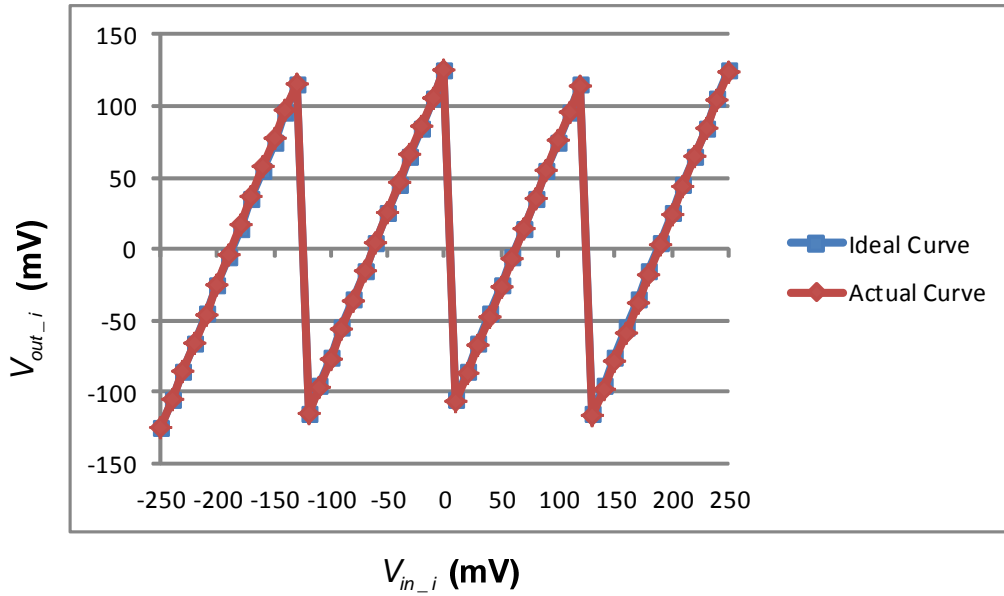


Fig. 4-6 ΔV_x for all input range

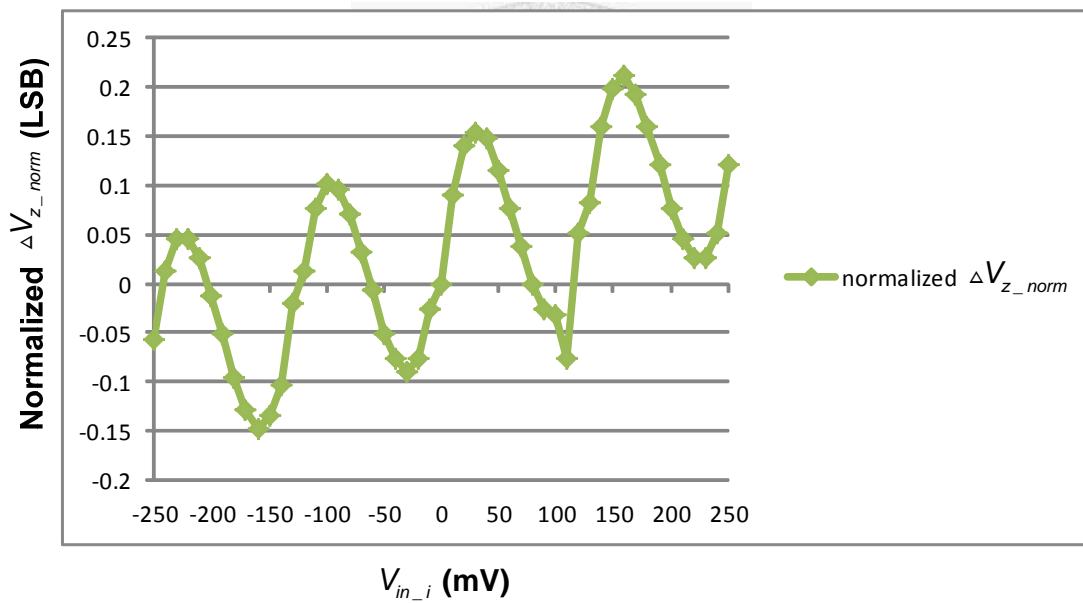
As described in 3.4.1, opamp dc gain A_o and unit gain bandwidth $\omega_u (= A_o \omega_p)$ vary with output swing. Fig. 4-7 (a) show how A_o and ω_u change with output swing in post-simulation. A_o and ω_u respectively change from 29.1 dB to 26.5 dB and from 5.64 GHz to 5.49 GHz when the absolute value of output swing changes from 0 mV to 250 mV. Fig. 4-7 (b) shows residue plots of ideal and actual transfer curve in post-simulation. Output voltage error ΔV_z defined as the voltage difference between ideal and actual transfer curve. Fig. 4-7 (c) shows normalized ΔV_{z_norm} where ΔV_z is normalized to 5-bit accuracy (because 1 bit is already resolved by the first stage) in post-simulation. Refer to Fig. 4-7 (c), ΔV_{z_norm} is within 0.21 LSB of 5-bit accuracy.



(a)



(b)



(c)

Fig. 4-7 (a) A_o and ω_u changes with output swing (b) residue plots of ideal and

actual transfer curve (c) normalized ΔV_{z_norm} defined as the voltage difference

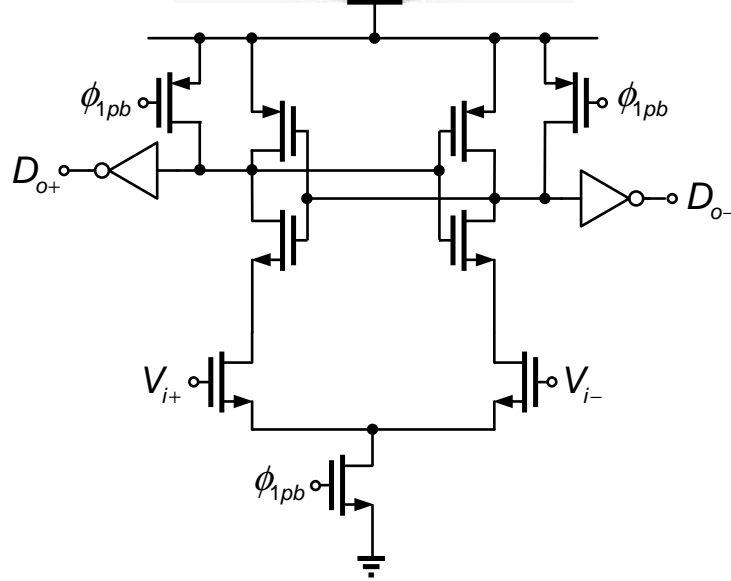
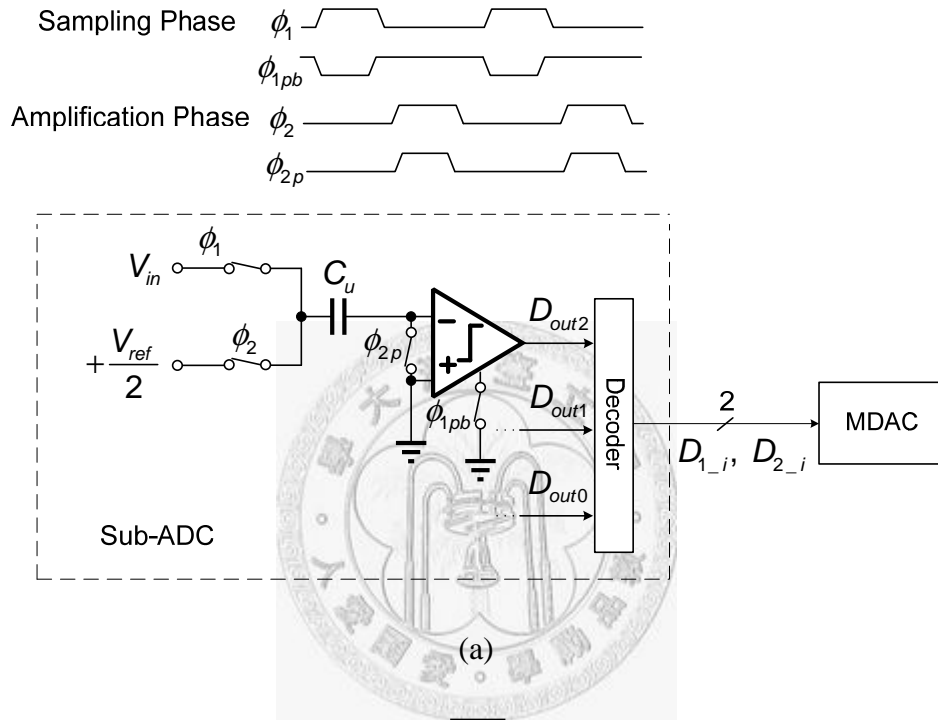
between ideal and actual transfer curve

As described in 3.4.3, t_s is 190 ps and C_{total} is 160 fF in post-simulation. From (3.28), G_y is required be larger than 0.95 in post-simulation, so τ_s should be smaller than 9.5 ps, and $R_1 + R_2$ should be smaller than 59 Ω . R_1 is above 21 Ω for all input range, and R_2 is 30 Ω in post-simulation

4.2.2 Sub-ADC

Fig. 4-8 (a) shows the block diagram of sub-ADC of each stage. It is composed of three comparators and a decoder. Each comparator has front-end three switches and one capacitor (single-ended for simplicity but fully-differential actual) [5]. In amplification phase (ϕ_2), the capacitors are charged by respective reference voltages $\pm \frac{V_{ref}}{2}$ and 0. Then in sampling phase (ϕ_1), voltage difference between input V_{in} and the reference voltages appears at the inputs of the comparators. And the comparators make decisions in the end of sampling phase. The outputs D_{out2} , D_{out1} , and D_{out0} of the comparators are sent to the decoder to control the switches of MDAC. There is an advantage to use the front-end switches and capacitors. As described in 4.2.1.1, offset of the comparators will increase the maximum output swing of opamp. This let non-linear amplification be more serious. And the usage of the switches and capacitors removes offset of the comparators from the difference of the common-mode voltages of input and the reference voltages [15].

The circuit implementation of the comparators [16] is shown in Fig. 4-8 (b). The comparators employ dynamic topology to reduce power consumption and compare input V_{i+} and V_{i-} in the end of sampling phase to generate output D_{o+} and D_{o-} .



(b)

Fig. 4-8 (a) block diagram of sub-ADC (b) circuit implementation of comparator

Input-referred offset of the comparators is $\pm 17 \text{ mV} (3\sigma)$ in post-simulation.

4.2.3 Clock Generator

Fig. 4-9 (a) shows the block diagram of a clock generator. All phases are generated by a sinusoidal input V_{clk} . Main phases contains ϕ_{1p} , ϕ_{2p} , ϕ_1 , and ϕ_2 .

ϕ_{1p} and ϕ_{2p} (or ϕ_1 and ϕ_2) are two non-overlapping phases with the same pulse width $T_{\phi p}$ (or T_{ϕ}) and the phase difference of 180 degree. The falling edge of ϕ_1 (or ϕ_2) comes after that of ϕ_{1p} (or ϕ_{2p}) by the delay of inv1 and inv3 T_{d_inv} (or inv2 and inv4) to realize bottom-plate sampling [17] whereas the rising edge of ϕ_1 (or ϕ_2) is the same as that of ϕ_{1p} (or ϕ_{2p}). There are two digital-to-time converters

(DTC) controlled by binary digital control bits $x_5, x_4, x_3, x_2, x_1, x_0$ decoded to $a_2, a_1, a_0, \dots, f_2, f_1, f_0$ to adjust the delay of DTC T_{d_dtc} . $T_{\phi p}$ is time difference

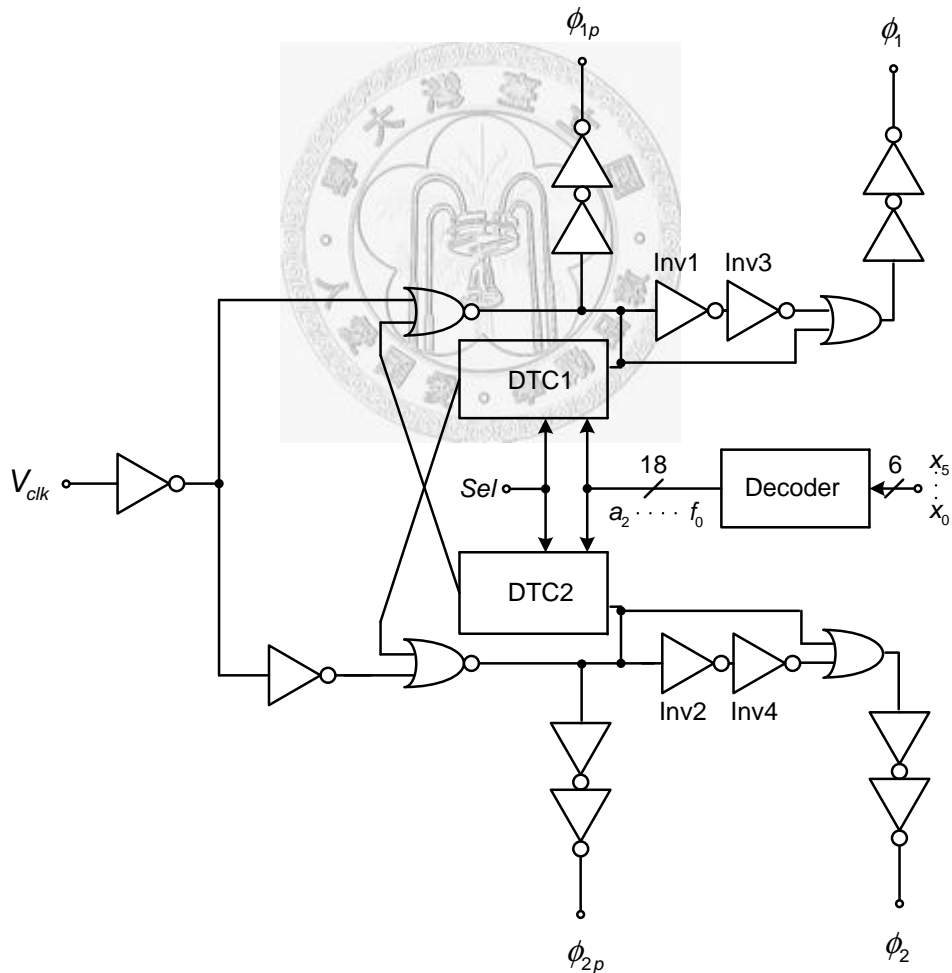
between a half of the reciprocal of sampling rate $\frac{T_s}{2}$ and T_{d_dtc} and is changed by

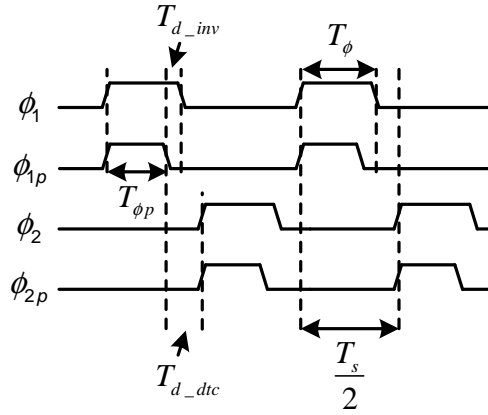
changing T_{d_dtc} . $T_{\phi p}$, T_{ϕ} , T_{d_inv} , T_{d_dtc} , and $\frac{T_s}{2}$ are related:

$$T_{\phi} = T_{\phi p} + T_{d_inv} \quad (4.6)$$

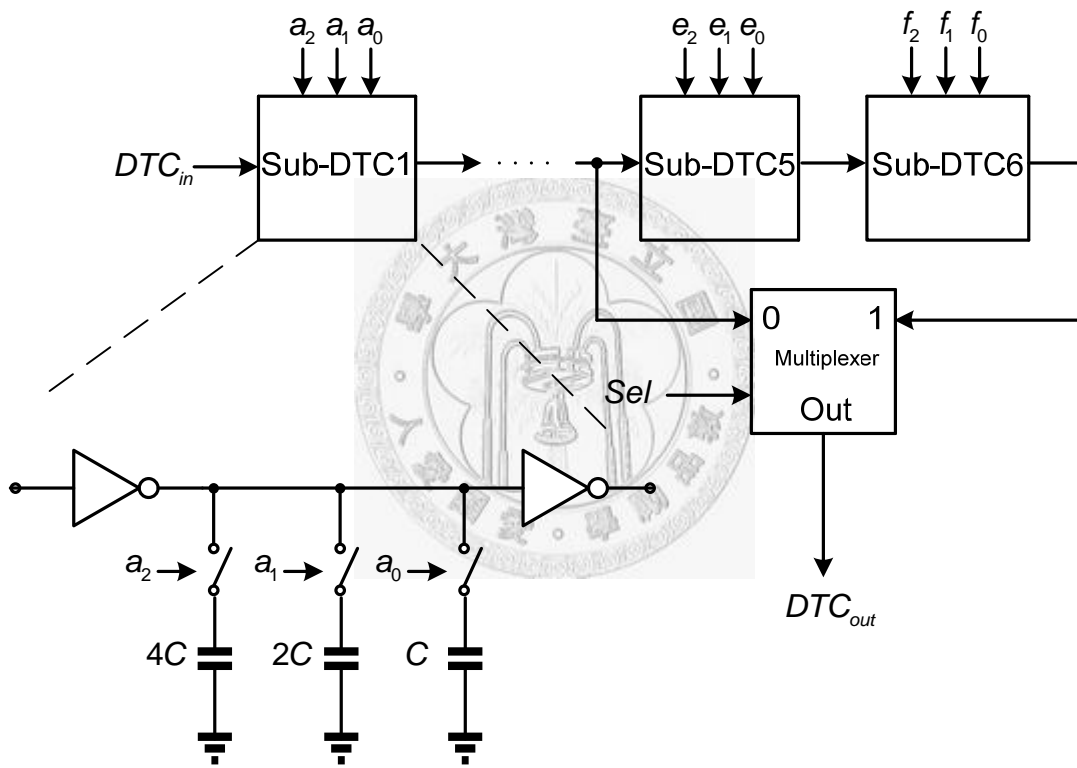
$$T_{\phi p} = \frac{T_s}{2} - T_{d_dtc} \quad (4.7)$$

Figure 4-9 (b) shows the block diagram of DTC. It contains six sub-DTC and a multiplexer. Sub-DTC is composed of two inverters and three binary-weighted capacitors controlled by digital control bits. The series of numerous sub-DTC with the multiplexer controlled by Sel at the end ensure wide delay range to adapt to environment variation. T_{d_dtc} is varied and guaranteed to be monotonic with the increase of $x_5 \dots x_0$.





(a)



(b)

Fig. 4-9 (a) block diagram of clock generator (b) block diagram of DTC

As described in 3.4.2, $\left. \frac{dG_{eff}(t)}{dt} \right|_{t=t_{ideal}}$ is 0.007 1/ps in post-simulation. Refer to

Fig. 3-8, SNDR is above 34.88(= 6.02·6+1.76-3=37.88-3) dB when ΔG_x is

within 0.07. That is, Δt is required within 10ps. Therefore, the resolution of DTC is set 5 ps, and the other 5 ps of Δt is reserved for clock jitter.

Fig. 4-10 shows T_{d_dtc} with Sel and binary digital control bits $x_5, x_4, x_3, x_2, x_1, x_0$ in decimal expression in post-simulation. $x_5 \dots x_0$ are from 0 to 28 when Sel is 0 and from 0 to 42 when Sel is 1. T_{d_dtc} is from 161~295 ps with 4~5 ps step when Sel is 0 and from 229~430 ps with the same step when Sel is 1. The delay range of DTC is 269 ps.

$T_{\phi p}$ is also the time of amplification phase and is unchanged no matter how $\frac{T_s}{2}$ changes. From (4.7), because T_{d_dtc} has range, the range of $\frac{T_s}{2}$ is limited. $T_{\phi p}$ is 190 ps, and T_{d_dtc} has maximum 430 ps in post-simulation. Therefore, $\frac{T_s}{2}$ has maximum 620 ps in post-simulation. That is, sampling rate has minimum 810 MS/s in post-simulation.

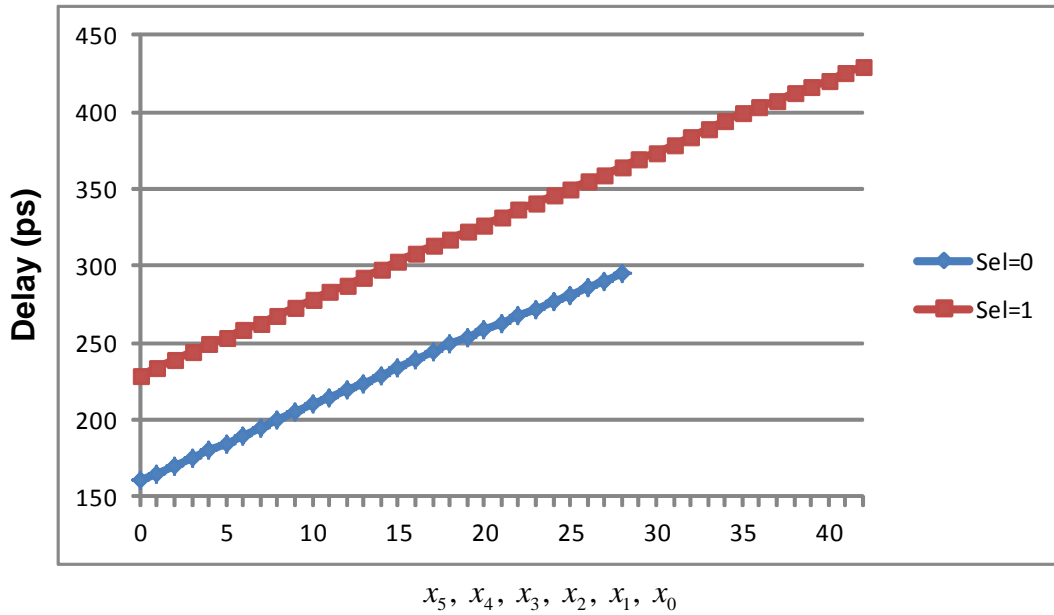
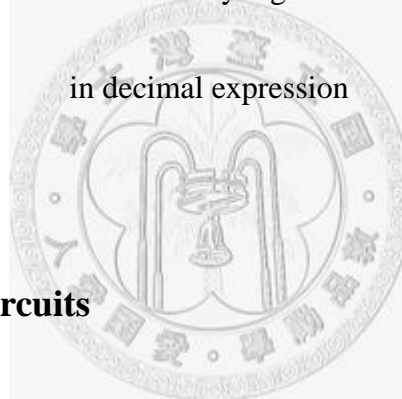


Fig. 4-10 delay of DTC with *Sel* v.s. binary digital control bits $x_5, x_4, x_3, x_2, x_1, x_0$



4.2.4 Calibration Circuits

Fig. 4-11 (a) shows the block diagram of calibration circuits. It contains two replica stages, a calibration comparator with offset calibration, and a digital loop filter. As described in 3.4.3, because of incomplete-settling technique, there is sampling attenuation between stages. Sampling attenuation can be compensated:

$$G_{eff}(t_s) \cdot G_y = 2 \quad (4.8)$$

From (4.8), $G_{eff}(t_s)$ is $\frac{2}{G_y}$. Because sampling attenuation happens between stages,

if only the first replica stage with residue plot shown in Fig. 4-11 (b) is applied, a

known analog input V_{in_known} set 0 with $D_{1_replica1}$ set 0 and $D_{1_replica2}$ set -1 is given,

and an analog value set $\frac{V_{ref}}{2}$ which corresponds to V_{in_known} is compared with the residue output $V_{out_replica1}(t_s)$ of the first replica stage at t_s , assuming that the comparator is calibrated and has no offset, from (4.1):

$$\begin{aligned} V_{out_replica1}(t_s) &= G_{eff}(t_s)(V_{in_known} - D_{1_replica1} \cdot \frac{V_{ref}}{2} - D_{2_replica1} \cdot \frac{V_{ref}}{4}) \\ &= G_{eff}(t_s)(\frac{V_{ref}}{4}) \end{aligned} \quad (4.9)$$

From (4.9), if $V_{out_replica1}(t_s)$ is compared with $\frac{V_{ref}}{2}$, $G_{eff}(t_s)$ is calculated as 2 rather than $\frac{2}{G_y}$. In other words, sampling attenuation cannot be compensated. If the

second replica stage with residue plot shown in Fig. 4-11 (c) is added with $D_{1_replica2}$ set 0 and $D_{2_replica2}$ set 1, and $\frac{V_{ref}}{2}$ which corresponds to V_{in_known} and $V_{out_replica1}(t_s)$ is compared with the residue output $V_{out_replica2}(t_s)$ of the second replica stage at t_s , assuming that the comparator is calibrated and has no offset, from (4.1) and (4.9):

$$\begin{aligned} V_{out_replica2}(t_s) &= G_{eff}(t_s)(V_{in_replica2} - D_{1_replica2} \cdot \frac{V_{ref}}{2} - D_{2_replica2} \cdot \frac{V_{ref}}{4}) \\ &= G_{eff}(t_s)(G_y V_{out_replica1}(t_s) - D_{1_replica2} \cdot \frac{V_{ref}}{2} - D_{2_replica2} \cdot \frac{V_{ref}}{4}) \\ &= G_{eff}(t_s)\{G_y[G_{eff}(t_s)(\frac{V_{ref}}{4})] - \frac{V_{ref}}{4}\} \end{aligned} \quad (4.10)$$

From (4.10), if $V_{out_replica2}(t_s)$ is compared with $\frac{V_{ref}}{2}$, $G_{eff}(t_s)$ is calculated as:

$$G_{eff}(t_s) = \frac{1 + \sqrt{1 + 8G_y}}{2G_y} \quad (4.11)$$

From (4.11), $G_{eff}(t_s)$ is larger than 2 but smaller than $\frac{2}{G_y}$. Using two replica stages indeed partially compensates sampling attenuation. As described in 4.2.2,

$\left. \frac{dG_{eff}(t)}{dt} \right|_{t=t_{ideal}}$ is 0.007 1/ps, and the resolution of DTC is 5 ps.

$\Delta G_x (= \left. \frac{dG_{eff}(t)}{dt} \right|_{t=t_{ideal}} \Delta t)$ of neighboring binary digital control bits

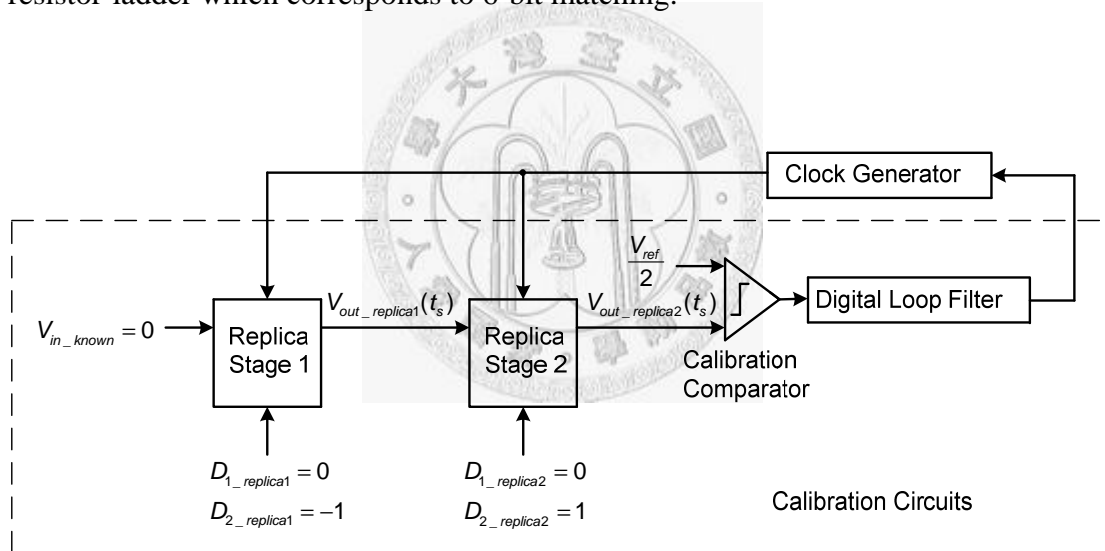
$x_5, x_4, x_3, x_2, x_1, x_0$ is 0.035, assuming that there is no clock jitter.

If $x_5 \dots x_0$ of $G_{eff}(t_s) (= \frac{1 + \sqrt{1 + 8G_y}}{2G_y})$ differ from that of $\frac{2}{G_y}$ by at most a digital

control bit (or $\frac{2}{G_y} - \frac{1 + \sqrt{1 + 8G_y}}{2G_y} < 0.035$), G_y is required be larger than 0.95.

To deserve to be mentioned, $\frac{V_{ref}}{2}$ used for calibration is generated in chip by a

resistor-ladder which corresponds to 6-bit matching.



(a)

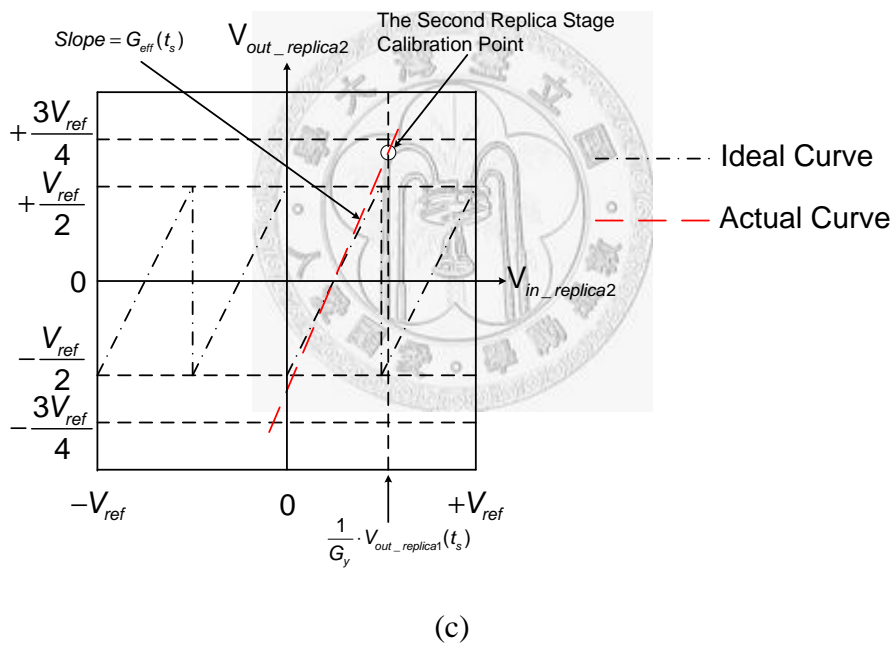
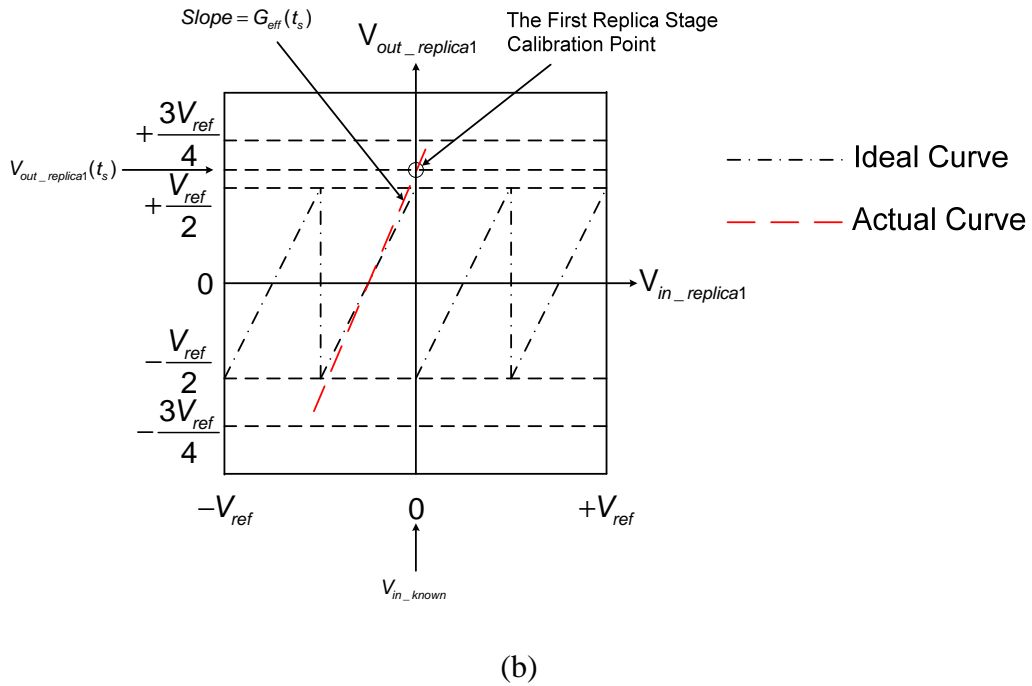


Fig. 4-11 (a) block diagram of calibration circuits (b) residue plot of the first replica stage (c) residue plot of the second replica stage

Besides, offset of opamp of the replica stages will cause error when $G_{eff}(t_s)$ is determined. Assuming that offset of opamp of the first and second replica stages is

V_{os1} and V_{os2} , respectively, the residue output $V_{out_replica1}(t_s)$ of the first replica stage at t_s without considering sampling attenuation and offset of the calibration comparator:

$$\begin{aligned} V_{out_replica1}(t_s) &= G_{eff}(t_s)(V_{in_replica1} - D_{1_replica1} \cdot \frac{V_{ref}}{2} - D_{2_replica1} \cdot \frac{V_{ref}}{4} + V_{os1}) \\ &= G_{eff}(t_s)(\frac{V_{ref}}{4} + V_{os1}) \end{aligned} \quad (4.12)$$

and the residue output $V_{out_replica2}(t_s)$ of the second replica stage at t_s :

$$\begin{aligned} V_{out_replica2}(t_s) &= G_{eff}(t_s)(V_{in_replica2} - D_{1_replica2} \cdot \frac{V_{ref}}{2} - D_{2_replica2} \cdot \frac{V_{ref}}{4} + V_{os2}) \\ &= G_{eff}(t_s)(V_{out_replica1} - D_{1_replica2} \cdot \frac{V_{ref}}{2} - D_{2_replica2} \cdot \frac{V_{ref}}{4} + V_{os2}) \\ &= G_{eff}(t_s)[G_{eff}(t_s)(\frac{V_{ref}}{4} + V_{os1}) - \frac{V_{ref}}{4} + V_{os2}] \end{aligned} \quad (4.13)$$

From (4.13), if $V_{out_replica2}(t_s)$ is compared with $\frac{V_{ref}}{2}$, $G_{eff}(t_s)$ is not 2 and results in error. Input-offset-storage (IOS) technique [18] is used to suppress the effect of offset of opamp of the replica stages. Fig. 4-12 (a) and (b) shows that input-offset-storage (IOS) technique is used in sampling phase and amplification phase, respectively. The output offset voltage of the outputs of opamp due to offset V_{os} is reduced to $\frac{V_{os}}{A_0}$ where A_0 is opamp dc gain with IOS technique rather than V_{os} without IOS technique.

$$\frac{V_{os1}}{A_0} \text{ and } \frac{V_{os2}}{A_0} \text{ are } \pm 0.5 \text{ mV} (3\sigma) \text{ (} V_{os1} \text{ and } V_{os2} \text{ are } \pm 15 \text{ mV} (3\sigma) \text{ and } A_0$$

is 29.1 dB) in post-simulation. From (4.13), $V_{out_replica2}(t_s)$ is compared with

$\frac{V_{ref}}{2}$ ($=125\text{ mV}$), and $G_{eff}(t_s)$ deviate from 2 by ± 0.016 which is small enough

refer to Fig. 3-8.

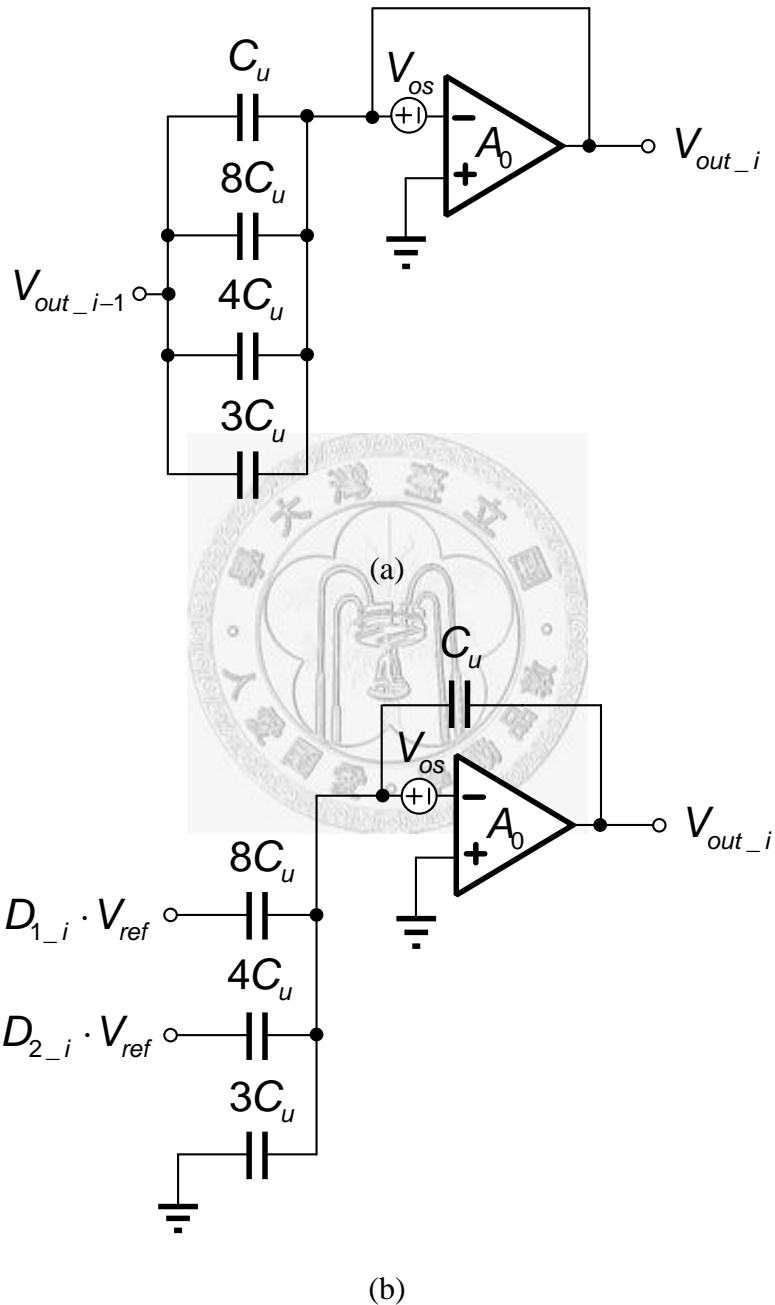


Fig. 4-12 IOS technique is used (a) in sampling phase (b) in amplification phase

If offset of the calibration comparator after offset calibration is V_{os_cal} , from (4.13), equivalently, $V_{out_replica2}(t_s)$ is compared with $\frac{V_{ref}}{2}(=125\text{ mV})+V_{os_cal}$. Assuming that sampling attenuation, V_{os1} , and V_{os2} are not taken into consideration, V_{os_cal} with maximum $\pm\frac{V_{LSB}}{5}(=\pm 1.5\text{ mV})$ let $G_{eff}(t_s)$ deviate from 2 by ± 0.008 which is small enough refer to Fig. 3-8.

The circuit implementation of the calibration comparator with offset calibration is shown in Fig. 4-13. There are four binary-weighted current controlled by digital control bits y_3, y_2, y_1, y_0 and z_3, z_2, z_1, z_0 at each side of the calibration comparator to compensate offset of the calibration comparator before offset calibration.

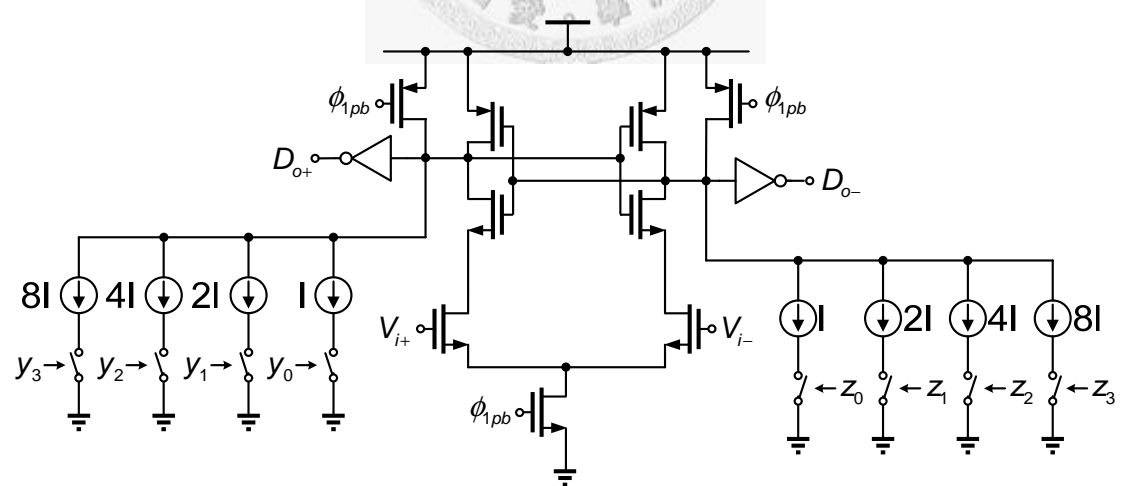


Fig. 4-13 circuit implementation of calibration comparator with offset calibration

Input-referred offset of the calibration comparator before offset calibration is $\pm 17 \text{ mV}$ (3σ) in post-simulation. Fig. 4-14 shows embedded calibration offset v.s. $y_3 \dots y_0$ (or $z_3 \dots z_0$) in decimal expression in post-simulation. Maximum embedded calibration offset is $\pm 17.9 \text{ mV}$ with maximum 1.5 mV step.

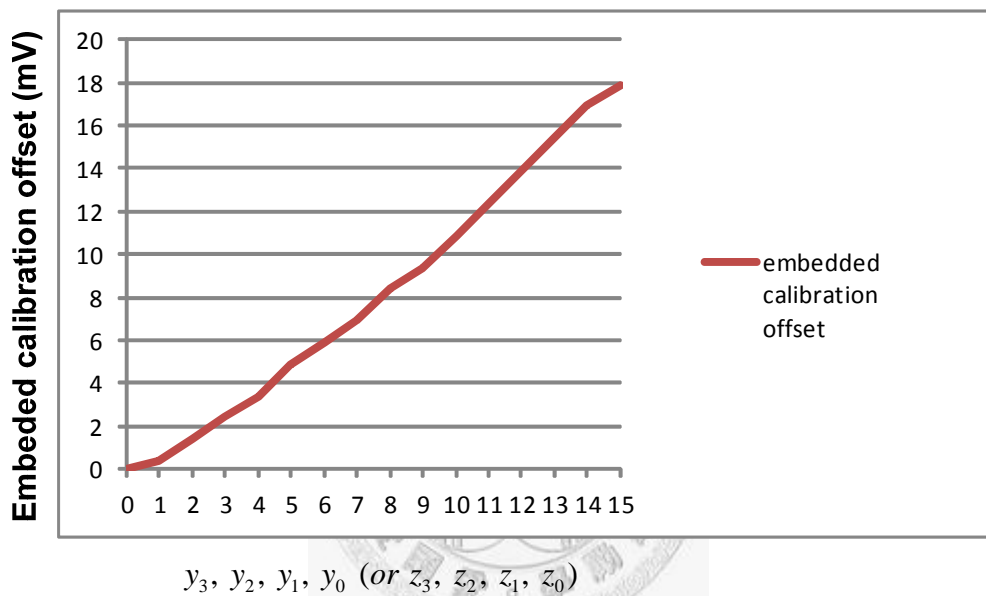


Fig. 4-14 embedded calibration offset v.s. $y_3 \dots y_0$ (or $z_3 \dots z_0$)

Fig. 4-15 (a) shows the block diagram of the digital loop filter. It contains two cascaded sub-filter and back-end digital circuits. The function of the digital loop filter is to eliminate the disturbance of noise.

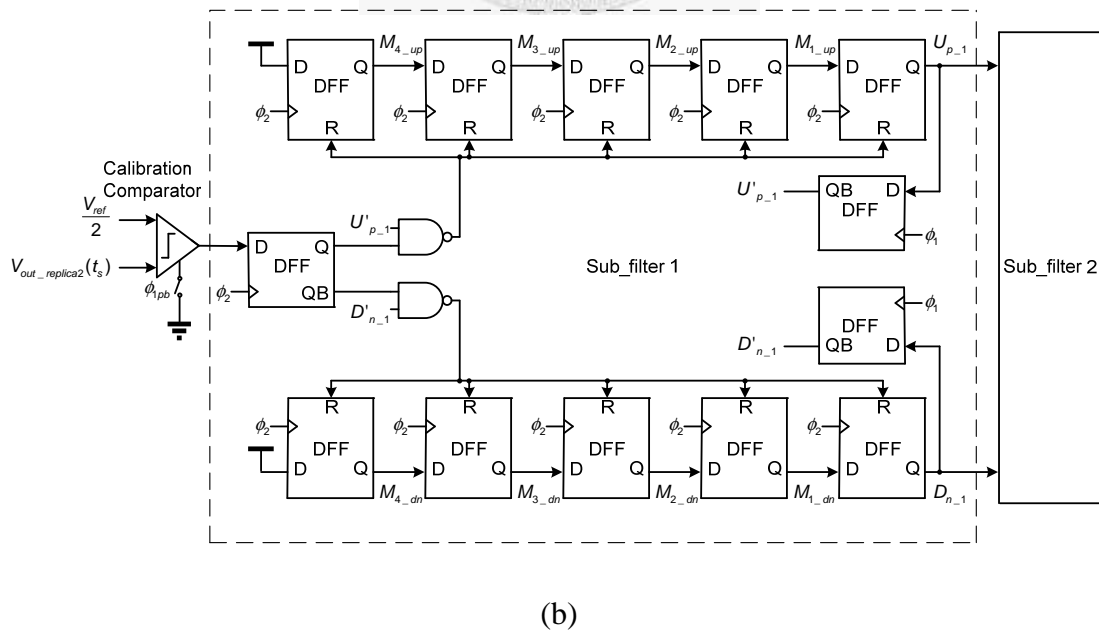
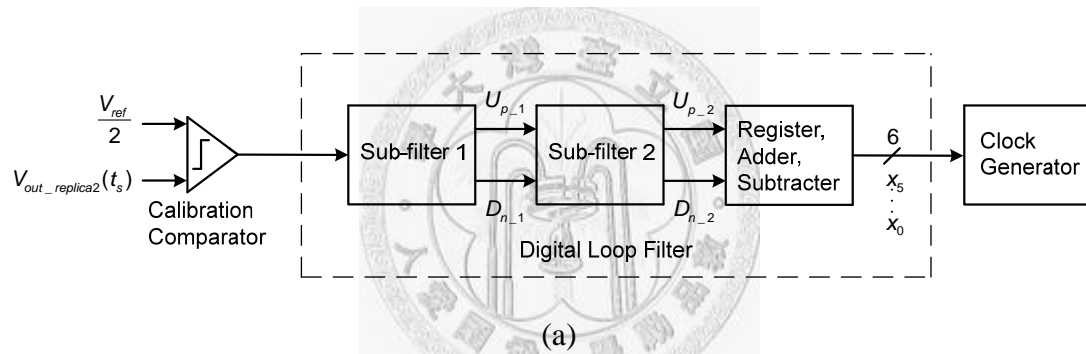
The first sub-filter shown in Fig. 4-15 (b) is composed of a front-end D flip-flop (DFF), two DFF chains, and two reset DFF. Each DFF chain has 5 DFF. The front-end DFF captures the comparison result of the calibration comparator. If the comparison

result is 1, the up DFF chain shifts 1 right and reset the down DFF chain, and vice versa. Once 1 is shifted to the most right of either the up or down DFF chain, both them are reset. For example, the outputs $M_{4_up}, M_{3_up}, M_{2_up}, M_{1_up}, U_{p-1}$ of the up DFF chain are 11000 and the outputs $M_{4_dn}, M_{3_dn}, M_{2_dn}, M_{1_dn}, D_{n-1}$ of the down DFF chain are 00000 at this moment. If next comparison result is 1, $M_{4_up} \dots U_{p-1}$ is 11100, and $M_{4_dn} \dots D_{n-1}$ is 00000. And if next comparison result is 0, $M_{4_up} \dots U_{p-1}$ is 00000, and $M_{4_dn} \dots D_{n-1}$ is 10000. Only that five consecutive 1 of the comparison result appears, U_{p-1} becomes 1, and vice versa.

The second sub-filter shown in Fig. 4-15 (c) is composed of a reset DFF and two DFF chains. Each DFF chain has 5 DFF. Before the beginning of sampling-point calibration, DFF of the DFF chains is reset by *init*. Then sampling-point calibration starts. The clock of the DFF chains is triggered by *trig* which becomes 1 when either U_{p-1} or D_{n-1} becomes 1. When U_{p-1} becomes 1, the up DFF chain shifts 1 right, and the down DFF chain shifts 0 left, and vice versa. Once 1 is shifted to the most right of either the up or down DFF chain, both them are reset. For example, the outputs $N_{4_up}, N_{3_up}, N_{2_up}, N_{1_up}, U_{p-2}$ of the up DFF chain are 11100 and the outputs $N_{4_dn}, N_{3_dn}, N_{2_dn}, N_{1_dn}, D_{n-2}$ of the down DFF chain are 10000 at this moment. If U_{p-1} becomes 1, $N_{4_up} \dots U_{p-2}$ is 11110, and $N_{4_dn} \dots D_{n-2}$ is 00000. And if D_{n-1} becomes 1, $N_{4_up} \dots U_{p-2}$ is 11000, and $N_{4_dn} \dots D_{n-2}$ is 11000.

Only that the accumulation of the number of times of 1 of U_{p-1} larger than that of D_{n-1} is five, U_{p-2} becomes 1, and vice versa.

The back-end digital circuits comprise the registers, an adder, and a subtractor. As described in 4.2.3, the registers are used to store current binary digital control bits $x_5, x_4, x_3, x_2, x_1, x_0$. Once U_{p-2} becomes 1, current $x_5 \dots x_0$ plus 1 to increase the delay of DTC and are stored in the registers. In the contrary, once D_{n-2} becomes 1, current $x_5 \dots x_0$ minus 1 to decrease the delay of DTC and are stored in the registers.



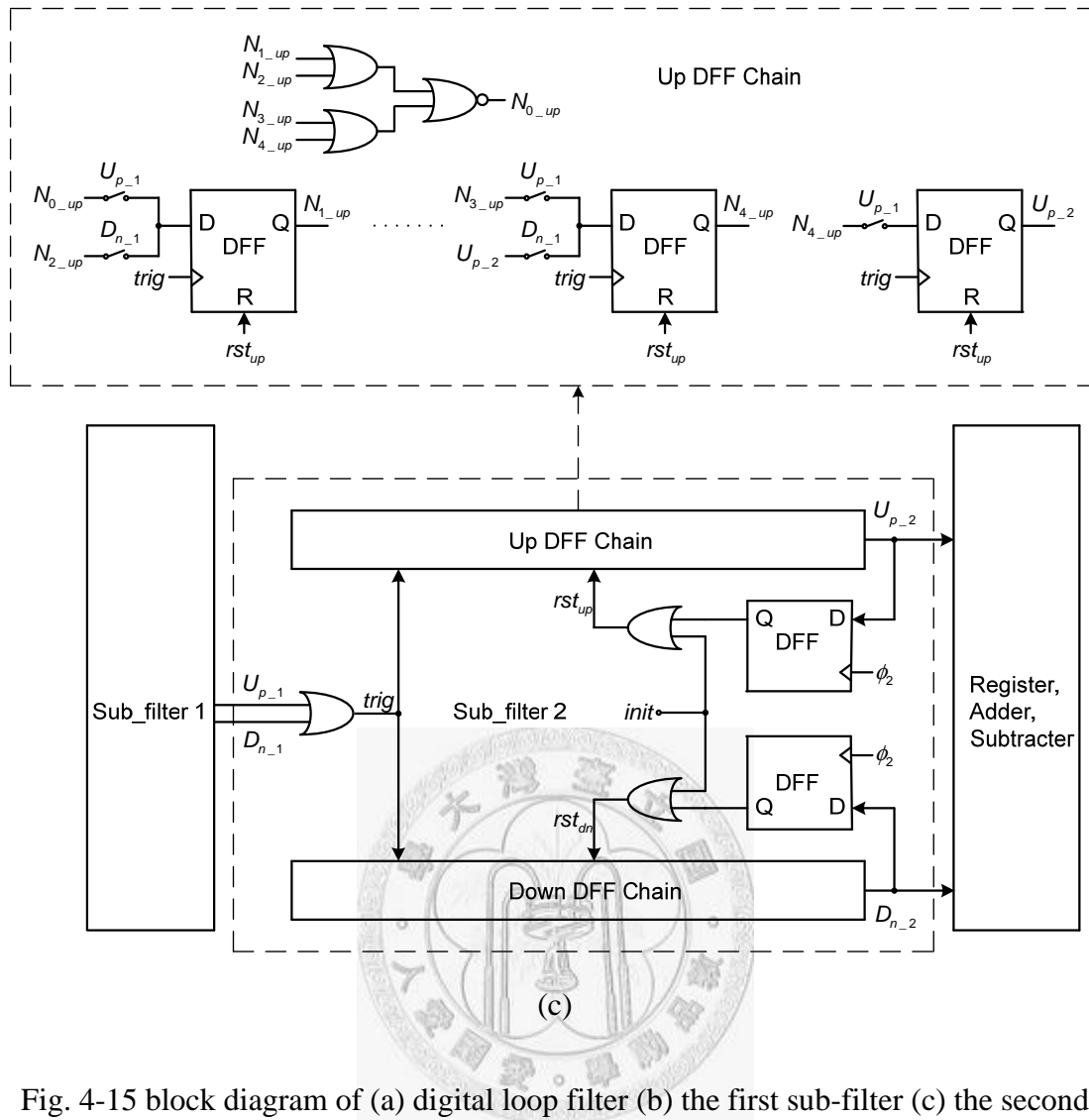


Fig. 4-15 block diagram of (a) digital loop filter (b) the first sub-filter (c) the second sub-filter

4.2.5 Timing Arrangement

Fig. 4-16 shows the timing arrangement of MDAC. Six operations are performed in one period. This stage samples the residue output of prior stage in duration 1. Duration 2 is used to realize bottom-plate sampling for this stage, and sub-ADC starts to compare at the same time. In duration 3, sub-ADC obtains comparison results and

them are decoded by a decoder to control the switches of MDAC. Then corresponding reference voltages at the bottom-plates of the capacitors of MDAC settle. This stage amplifies in duration 4. Also duration 5 is reserved to carry out bottom-plate sampling for next stage. In duration 6, the capacitors of MDAC, the inputs, and outputs of opamp are reset. Duration 1, 2, and 3 (or 4, 5, and 6) occupy half of the reciprocal of sampling rate $\frac{T_s}{2}$.



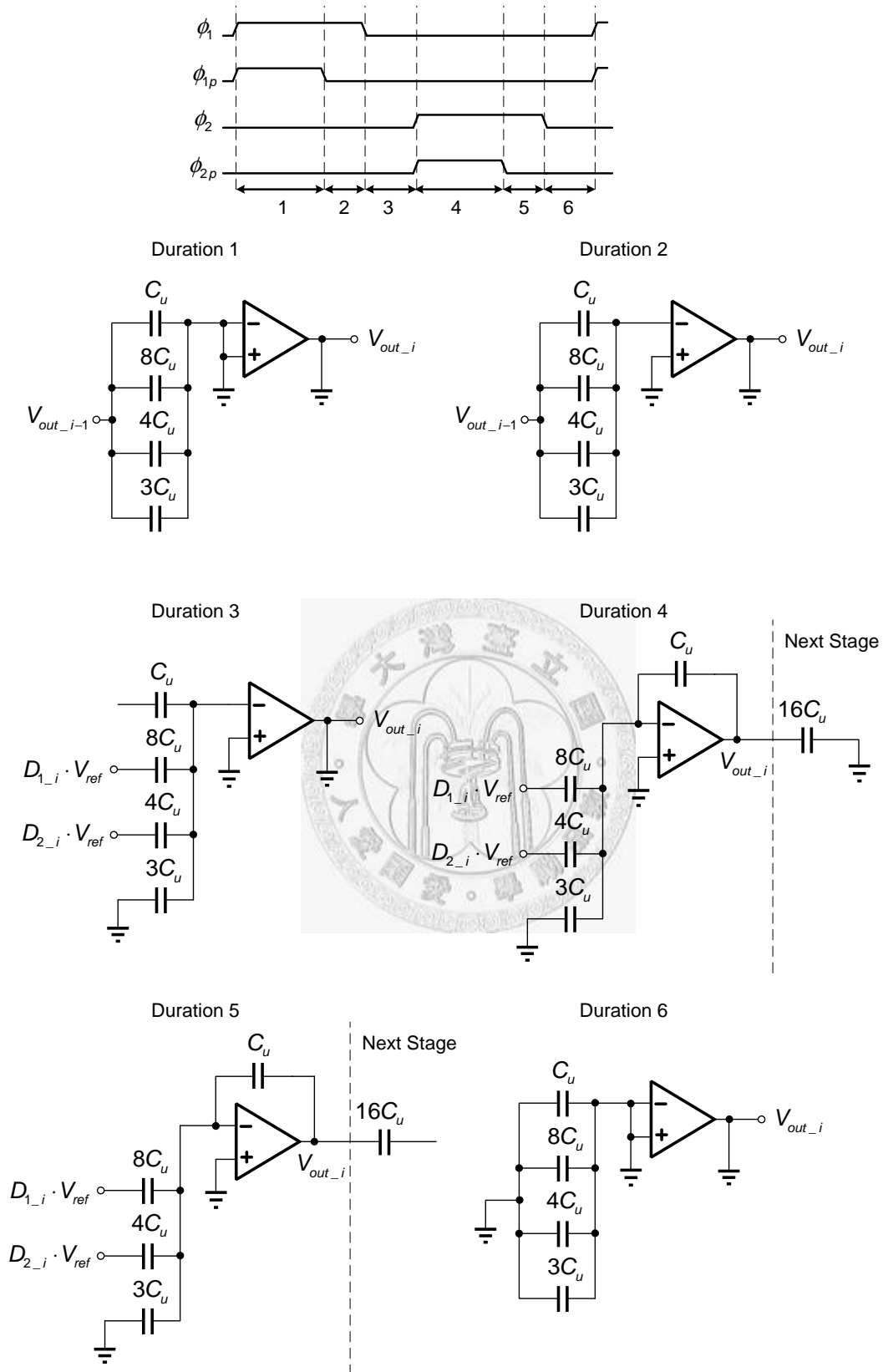


Fig. 4-16 timing arrangement of MDAC

To deserve to be mentioned, opamp-sharing technique between stages can be adopted in this ADC. Memory effect due to opamp-sharing technique is eliminated by modifying action in duration 5 when the inputs of opamp are reset shown in Fig. 4-17.

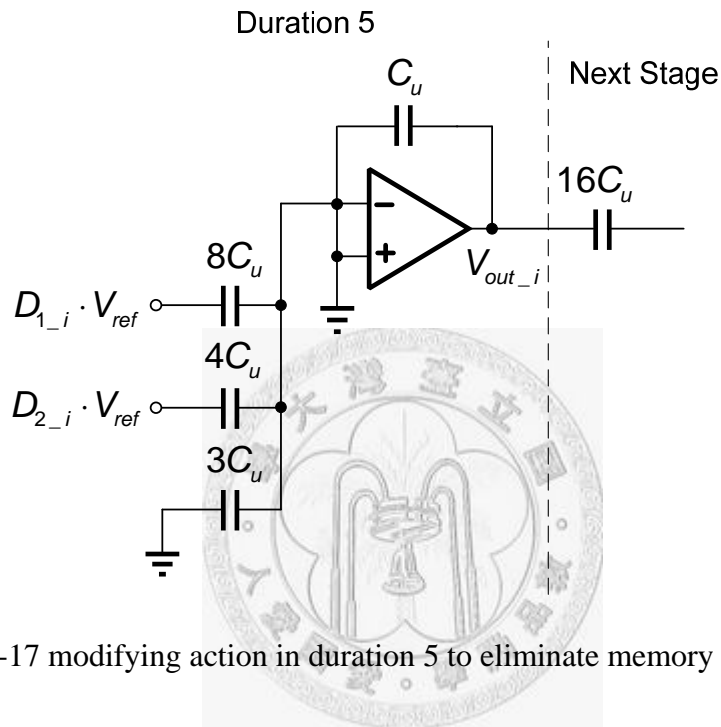


Fig. 4-17 modifying action in duration 5 to eliminate memory effect due to opamp-sharing technique

Table 4-1 indicates the timing arrangement in post-simulation when sampling rate (F_s) is 1 GS/s and corresponding $\frac{T_s}{2}$ is 500ps. The time when sub-ADC compares is estimated when the voltage difference of the inputs of one of the comparators is $\frac{V_{LSB}}{2}$. The bottleneck of sampling rate is the time when duration 1, 2, and 3 go through because duration 1, 2, and 3 occupy $\frac{T_s}{2}$.

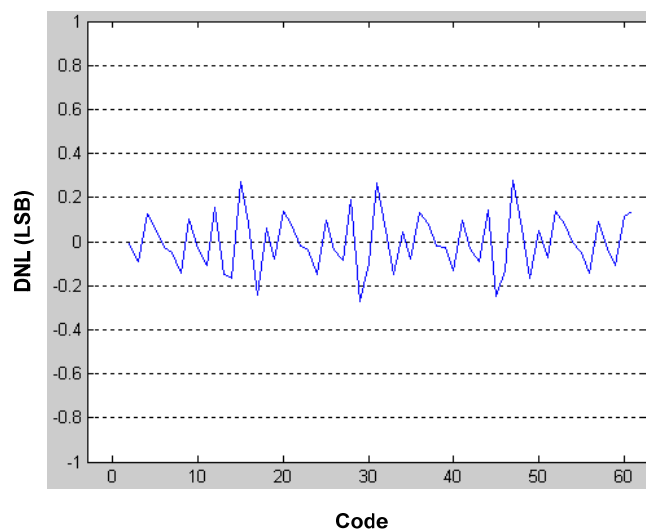
	Duration	Time	Action
$\frac{T_s}{2} = 500 \text{ ps}$	1	190 ps	MDAC Sample : 190 ps
	2	47 ps	Sub-ADC
	3	263 ps	Compare : 124 ps
$\frac{T_s}{2} = 500 \text{ ps}$	4	190 ps	MDAC Amplify : 190 ps
	5	47 ps	Bottom-plate Sample : 47 ps
	6	263 ps	Capacitor Reset : 109ps

Table 4-1 timing arrangement

4.3 Overall ADC Simulation Results

4.3.1 Static Performance

Fig. 4-18 shows DNL and INL of ADC in post-simulation when sampling rate (F_s) is 1 GS/s, and input frequency (F_{in}) is 492.1 MHz. DNL and INL are +0.28/-0.27 LSB and +0.17/-0.28 LSB, respectively.



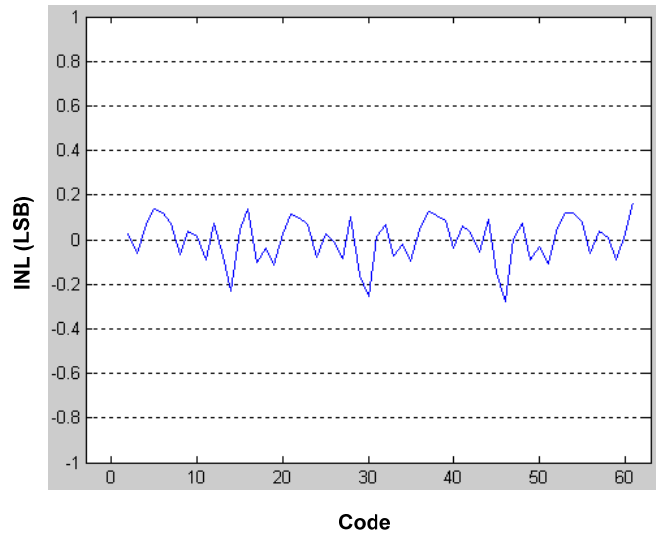


Fig. 4-18 DNL and INL of ADC @ $F_s = 1$ GS/s, $F_{in} = 492.1$ MHz

4.3.2 Dynamic Performance

Fig. 4-19 shows the FFT test of ADC in post-simulation. Sampling rate (F_s) is 1 GS/s, and input frequency (F_{in}) is 492.1 MHz. ENOB is 5.98 bits.

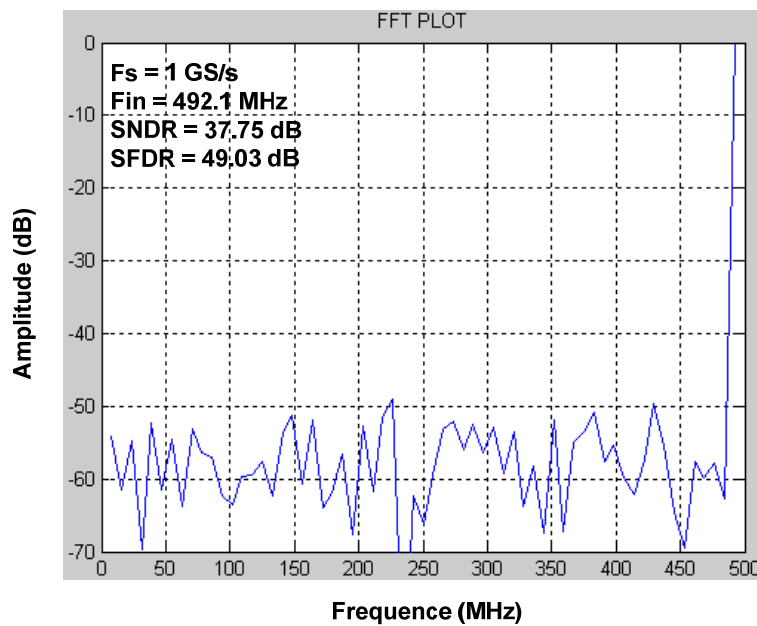


Fig. 4-19 FFT test of ADC @ $F_s = 1$ GS/s, $F_{in} = 492.1$ MHz

4.4 Summary

6-bit, 1GS/s pipelined ADC using incomplete-settling technique with background sampling-point calibration is implemented in this thesis. The performance of ADC in post simulation is summarized in Table 4-2.

Technology	TSMC 65nm CMOS GP
Resolution	6-bit
Active Area	0.3 mm ²
Supply Voltage	1 V
Sampling Rate	1 GS/s
Input Frequency	492.1 MHz
Power	60 mW*
DNL	+0.28/-0.27 LSB
INL	+0.17/-0.28 LSB
SNR	38.10 dB
THD	-48.84 dB
SFDR	49.03 dB
SNDR	37.75 dB
ENOB	5.98 bits
FoM	0.95 pJ/step

Table 4-2 performance of ADC

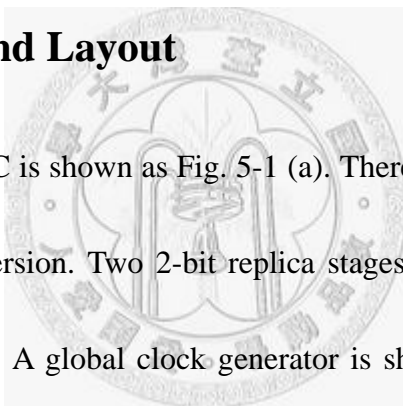
*include calibration circuits

Chapter 5 Measurement Results

5.1 Introduction

First, floor plan and layout are exhibited. Second, PCB design is demonstrated. Third, test setup with some considerations is discussed. Finally, measurement results composed of static and dynamic performance are illustrated.

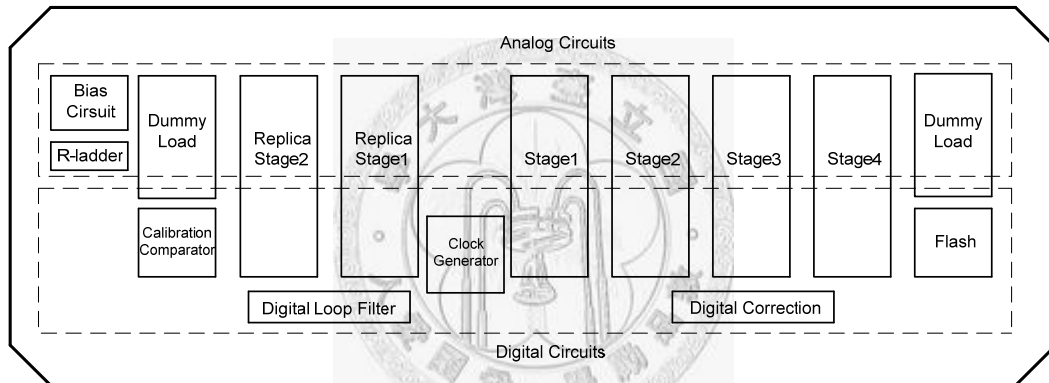
5.2 Floor Plan and Layout



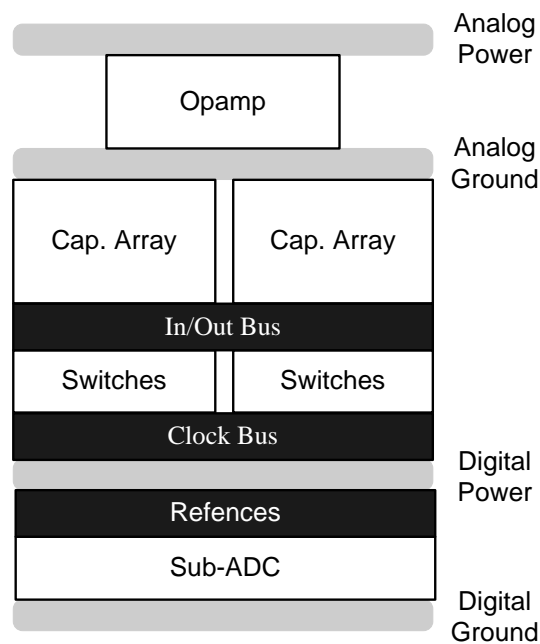
The floor plan of ADC is shown as Fig. 5-1 (a). There are four 2-bit stages and a 2-bit flash for ADC conversion. Two 2-bit replica stages are added for background sampling-point calibration. A global clock generator is shared among all the stages. Sampling-point calibration applies under the premise that all the stages are matched enough because the same phases produced by the clock generator are shared by them, so two dummy loads are added for the fourth stage and the second replica stage, respectively. The matching requirement of the first stage for ADC conversion and the first replica stage is the strictest since critical accuracy is in the first stage due to amplification between stages. Therefore, the first stage and the first replica stage are put as near as possible, and the clock generator is placed between them. Analog

circuits such as opamp, capacitor array, and bias circuit are separated from digital circuits such as sub-ADC and the clock generator to let rail-to-rail digital signals have less impact on sensitive analog signals for better performance.

The floor plan of one of all the stages is shown as Fig. 5-1 (b). Analog circuits which contains opamp and capacitor array and digital circuits which contains switches and sub-ADC are detached.



(a)



(b)

Fig. 5-1 floor plan of (a) ADC (b) one of all the stages

The layout of ADC is shown in Fig. 5-2. It is fabricated in TSMC 65nm CMOS general-process (GP). Table 5-2 displays the functions of the 45 pins of ADC.

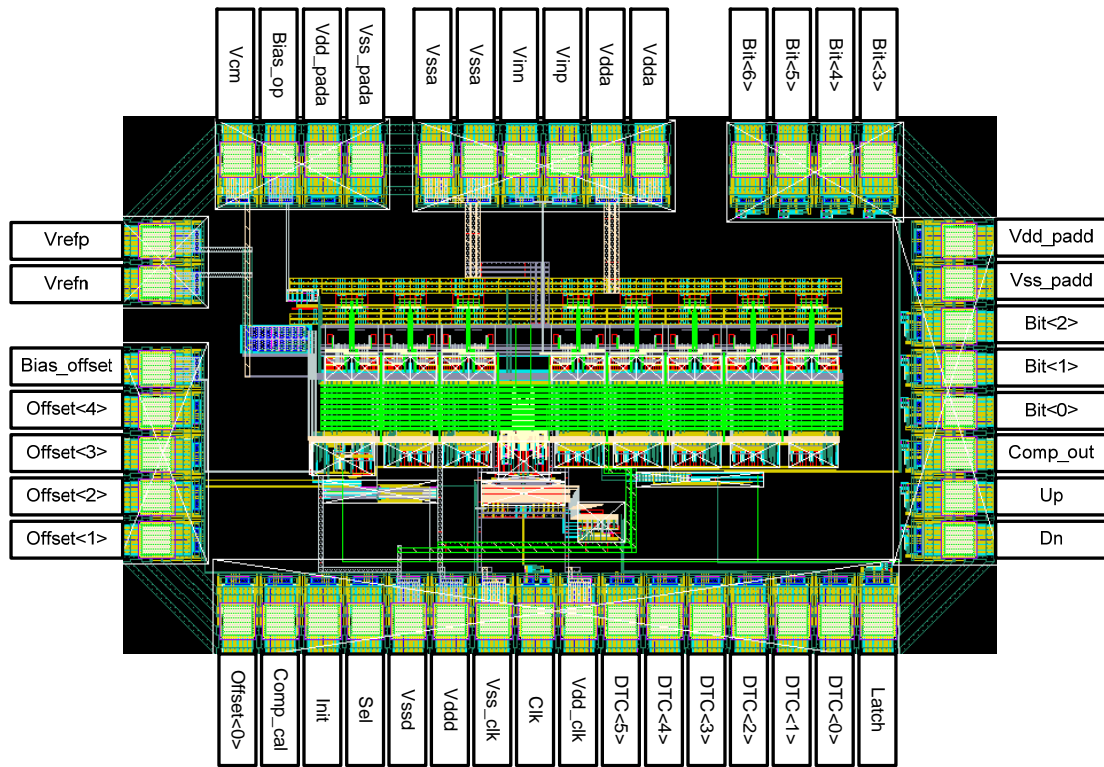


Fig. 5-2 layout of ADC

Pin	Description
Vdda	Analog supply
Vinp	Positive input signal
Vinn	Negative input signal
Vssa	Analog ground
Vss_pada	Ground for analog pad

Vdd_pada	Supply for analog pad
Bias_op	Current source of bias circuit
Vcm	Common mode voltage
Vrefp	Positive reference voltage
Vrefn	Negative reference voltage
Bias_offset	Current source of calibration comparator
Offset<4>	Calibration comparator digital control signal 4
Offset<3>	Calibration comparator digital control signal 3
Offset<2>	Calibration comparator digital control signal 2
Offset<1>	Calibration comparator digital control signal 1
Offset<0>	Calibration comparator digital control signal 0
Comp_cal	Calibration comparator calibration startup
Init	Digital loop filter reset signal <i>init</i>
Sel	DTC digital control signal <i>Sel</i>
Vssd	Digital ground
Vddd	Digital supply
Vss_clk	Clock ground
Clk	Clock signal
Vdd_clk	Clock supply
DTC<5>	DTC digital control signal x_5
DTC<4>	DTC digital control signal x_4
DTC<3>	DTC digital control signal x_3
DTC<2>	DTC digital control signal x_2
DTC<1>	DTC digital control signal x_1
DTC<0>	DTC digital control signal x_0
Latch	Divided clock signal
Dn	Second sub_filter of digital loop filter output D_{n-2}
Up	Second sub_filter of digital loop filter output U_{p-2}
Comp_out	Divided calibration comparator output
Bit<0>	Divided digital output bit 0
Bit<1>	Divided digital output bit 1
Bit<2>	Divided digital output bit 2
Vss_padd	Ground for digital pad
Vdd_padd	Supply for digital pad
Bit<3>	Divided digital output bit 3
Bit<4>	Divided digital output bit 4
Bit<5>	Divided digital output bit 5

Bit<6>	Divided digital output bit 6
--------	------------------------------

Table 5-1 functions of the 45 pins of ADC

5.3 PCB design

The goal of PCB design is to provide a platform which offers good test environment for ADC. Power and ground noise are generated by current which flows through power and ground lines which have resistance and inductance. Four-layer PCB is employed to provide a power and a ground plate. Both plates have large area, so the low resistance and inductance are achieved to lower power and ground noise. Every set of power and ground is decoupled by some 10 uF, 0.1 uF, and 0.01 uF capacitors. Three different capacitor values are used to reject noise which has different frequency.

Fig. 5-3 shows the schematic of an analog input on PCB. A single-ended analog input signal is converted to differential one by a RF transformer (JTX-4-10T).

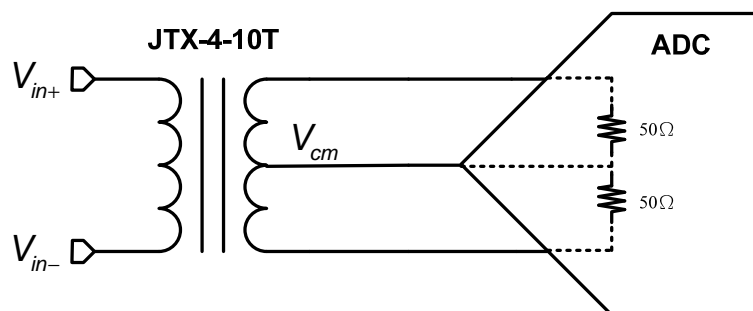


Fig. 5-3 schematic of analog input on PCB

Fig. 5-4 shows the schematic of reference voltages on PCB. A master reference voltage is produced by a Zener diode (LM385) to provide stable 2.5 V. The master reference voltage is connected to three variable resistors and generates three other reference voltages which contains V_{refp} , V_{refn} , and V_{cm} . V_{cm} is the common mode voltage of V_{refp} and V_{refn} . The reference voltages are buffered by opamp (AD8031) which is configured as a unit gain buffer. Three capacitor values 10 uF, 0.1 uF, and 0.01 uF are also used to decouple the reference voltages.

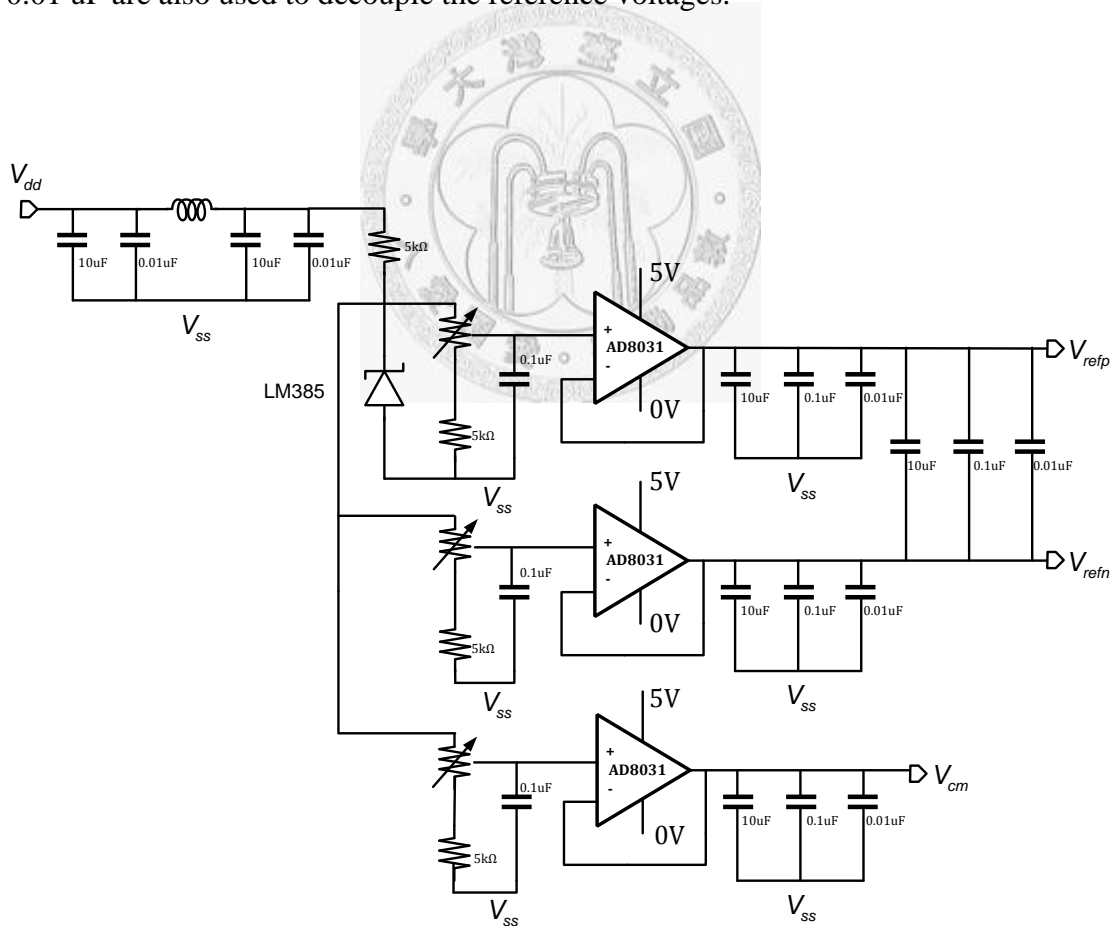


Fig. 5-4 schematic of reference voltages on PCB

Fig. 5-5 shows the schematic of power supplies on PCB. The power supplies V_{dda} , V_{ddd} , and V_{dd_clock} are generated by voltage regulators (LT3020). Three capacitor values 10 uF, 0.1 uF, and 0.01 uF are used to decouple the power supplies as well.

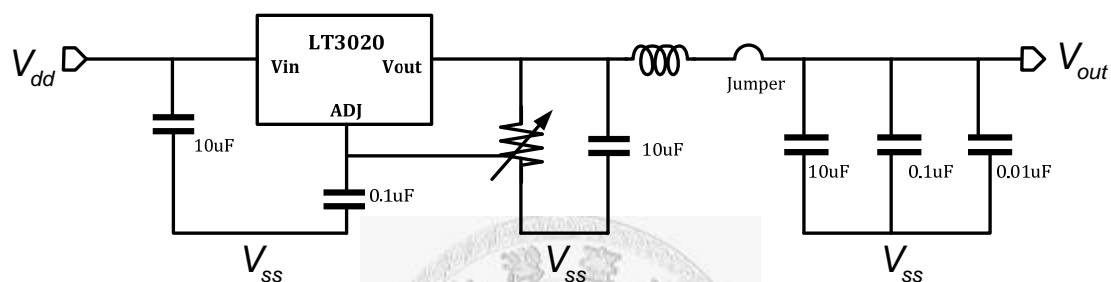
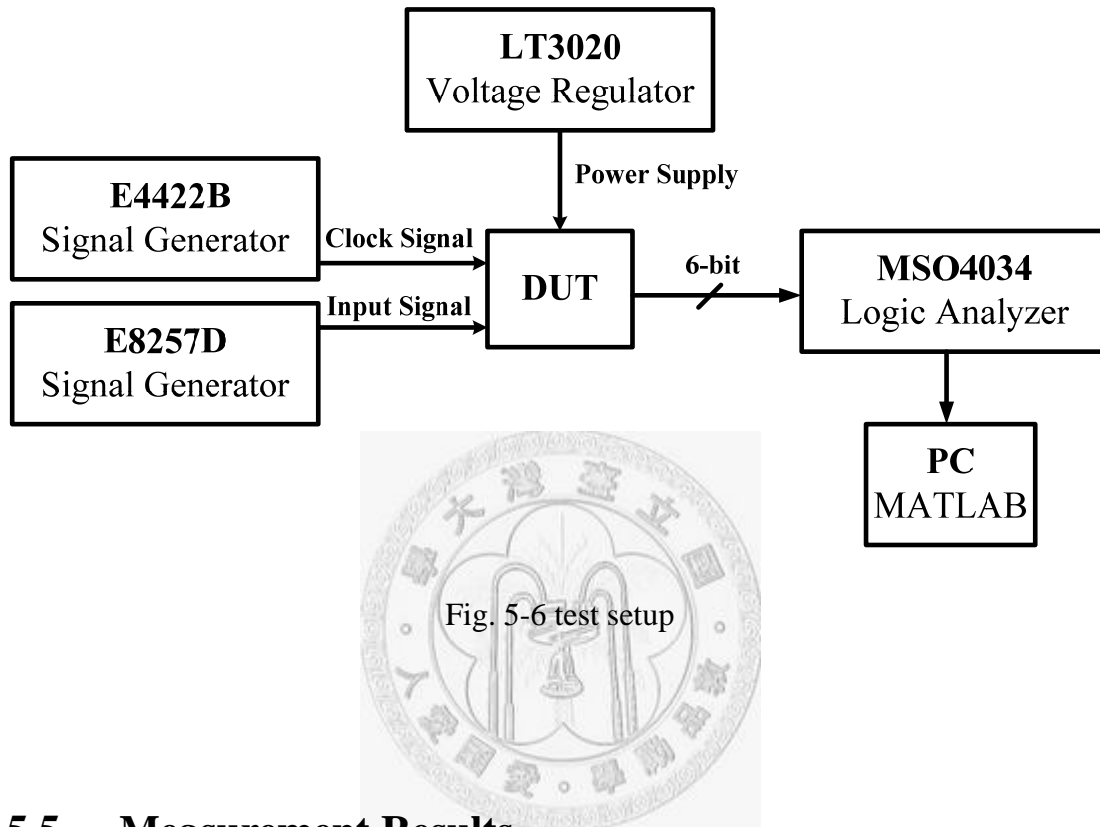


Fig. 5-5 schematic of power supplies on PCB

5.4 Test Setup

Test setup is shown in Fig. 5-6. Two signal generators (E8257D and E4422B) are applied to generate an analog input signal and a clock signal. Both signals are filtered by passive band-pass-filter (BPF) and separately connected by SMA cables. To convert the single-ended analog input signal to differential one, a RF transformer (JTX-4-10T) is chosen. The power supplies of design-under-test (DUT) are generated by voltage regulators (LT3020). A 6-bit digital output signal is captured by a logic

analyzer (MSO4034). The digital output signal is downloaded to a personal computer (PC) and processed by MATLAB to obtain static and dynamic performance.



5.5 Measurement Results

Fig. 5-7 shows the die photo of ADC. Active area is 0.30 mm^2 , and whole chip with pads occupies 0.89 mm^2 .

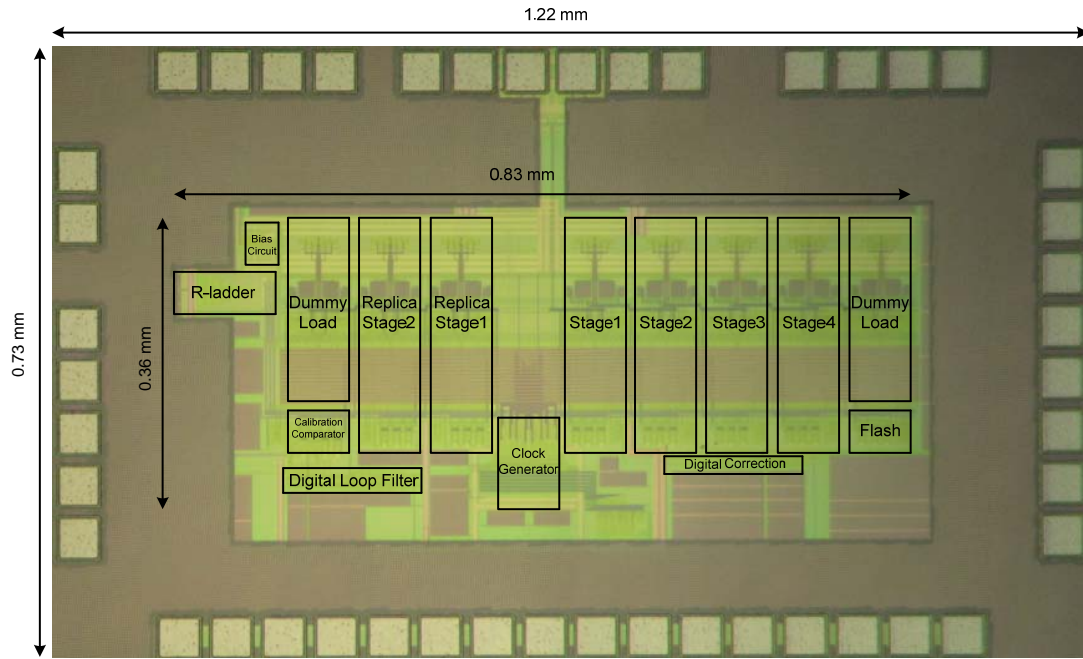
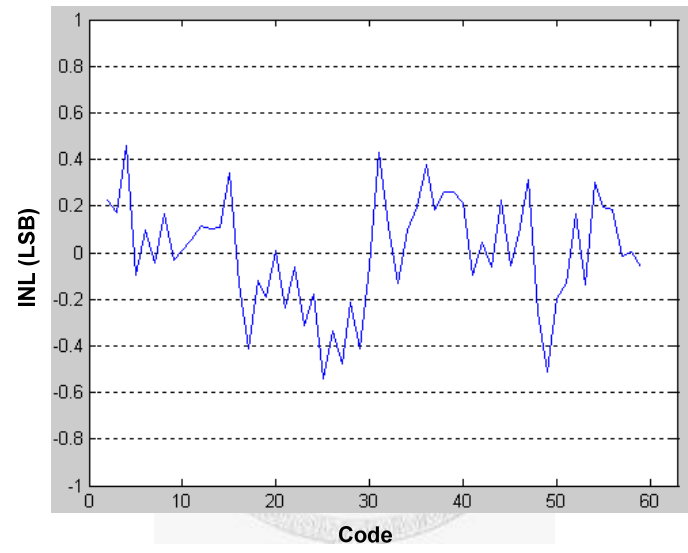
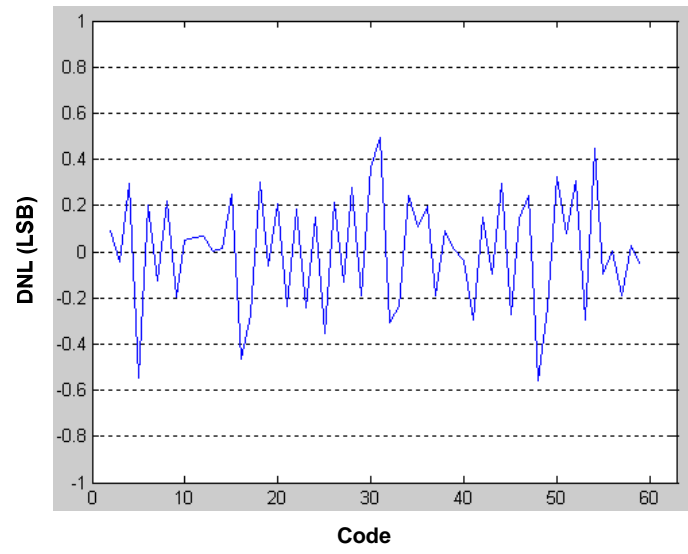


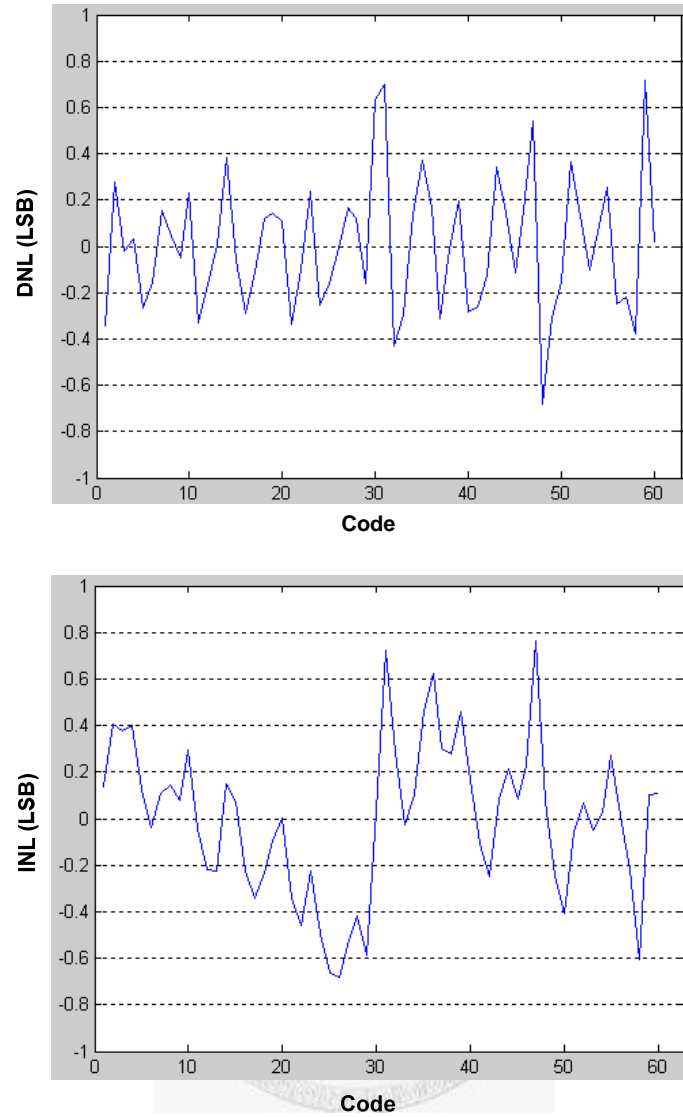
Fig. 5-7 die photo of ADC

5.5.1 Static Performance

Fig. 5-8 (a) shows DNL and INL of ADC in measurement when sampling rate (F_s) is 900 MS/s, and input frequency (F_{in}) is 9.7 MHz. DNL and INL of ADC are +0.50/-0.56 LSB and +0.46/-0.54 LSB, respectively. Fig. 5-8 (b) shows DNL and INL when F_s is 1 GS/s, F_{in} is 499.0 MHz. DNL and INL of ADC are +0.72/-0.68 LSB and +0.76/-0.68 LSB, respectively.



(a)



(b)

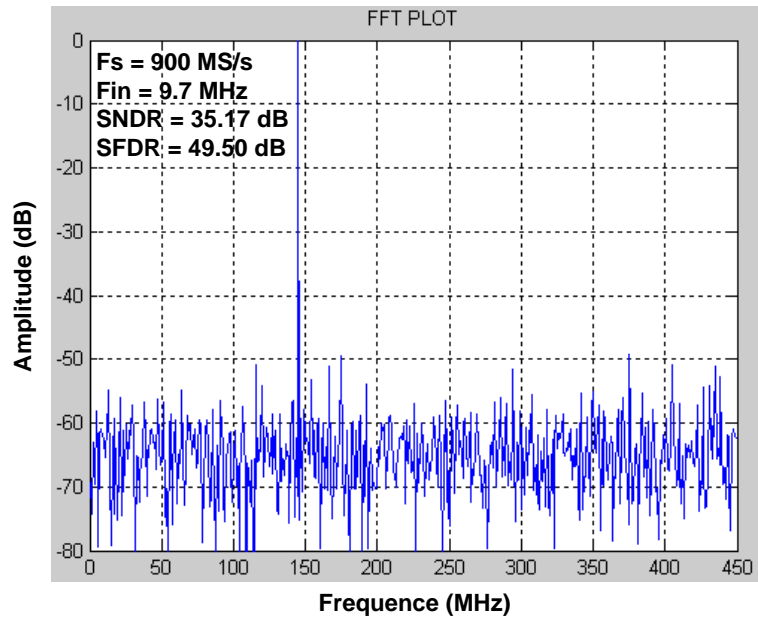
Fig. 5-8 DNL and INL of ADC (a) @ $F_s = 900$ MS/s, $F_{in} = 9.7$ MHz (b) @ $F_s = 1$

GS/s, $F_{in} = 499.0$ MHz

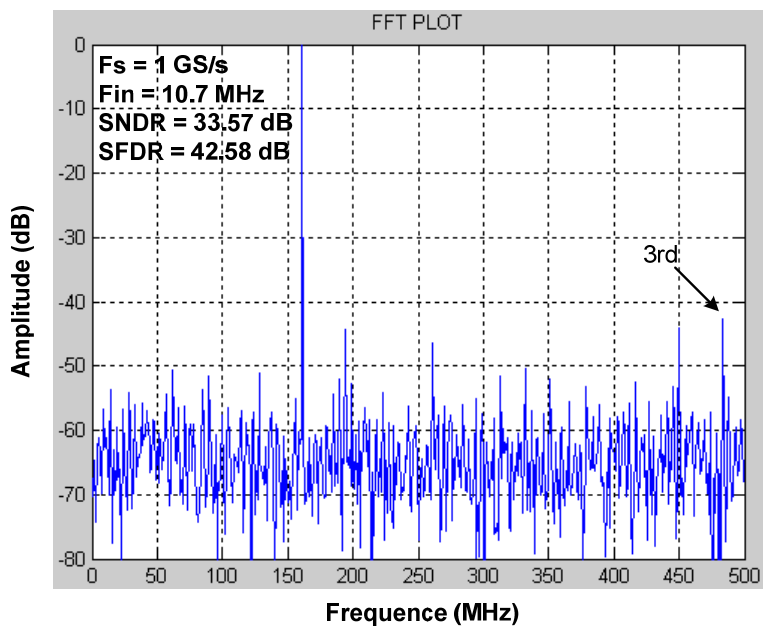
5.5.2 Dynamic Performance

Fig. 5-9 (a) shows FFT test of ADC in measurement when sampling rate (F_s) is 900 MS/s, and input frequency (F_{in}) is 9.7 MHz, and SNDR and SFDR are 35.17 dB

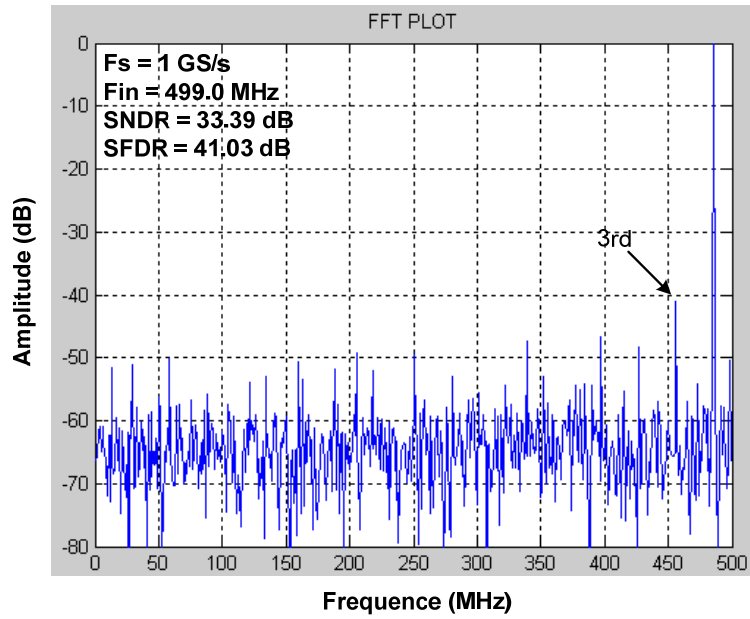
and 49.50 dB, respectively. Fig. 5-9 (b) shows FFT test when F_s is 1 GS/s, and F_{in} is 10.7 MHz, and SNDR and SFDR are 33.57 dB and 42.58 dB, respectively. Fig. 5-9 (c) shows FFT test when F_s is 1 GS/s, and F_{in} is 499.0 MHz, and SNDR and SFDR are 33.39 dB and 41.03 dB, respectively. By the way, the digital output of ADC is decimated by 15. Fig. 5-10 shows dynamic performance v.s. F_s when F_{in} is 10.7 MHz. Dynamic performance starts to degrade when F_s is larger than 950 MS/s because reference voltages at the bottom-plates of the capacitors of MDAC do not have enough time to fully settle before amplification phase. Fig. 5-11 shows dynamic performance v.s. F_{in} when F_s is 1 GS/s. Dynamic performance is fairly constant for all F_{in} because input capacitance is low. Fig. 5-12 shows ENOB v.s. binary digital control bits $x_5, x_4, x_3, x_2, x_1, x_0$ in decimal expression with Sel of DTC set 0 when F_s is 1 GS/s, and F_{in} is 10.7 MHz. ENOB is maximum when $x_5 \dots x_0$ in decimal expression is 15, or corresponding $G_{eff}(t_s)$ is 2. ENOB drops when $x_5 \dots x_0$ in decimal expression is bigger or smaller than 15, or $G_{eff}(t_s)$ is bigger or smaller than 2.



(a)



(b)



(c)

Fig. 5-9 FFT test of ADC (a) $F_s = 900 \text{ MS/s}$, $F_{in} = 9.7 \text{ MHz}$ (b) @ $F_s = 1 \text{ GS/s}$,

$F_{in} = 10.7 \text{ MHz}$ (c) @ $F_s = 1 \text{ GS/s}$, $F_{in} = 499.0 \text{ MHz}$

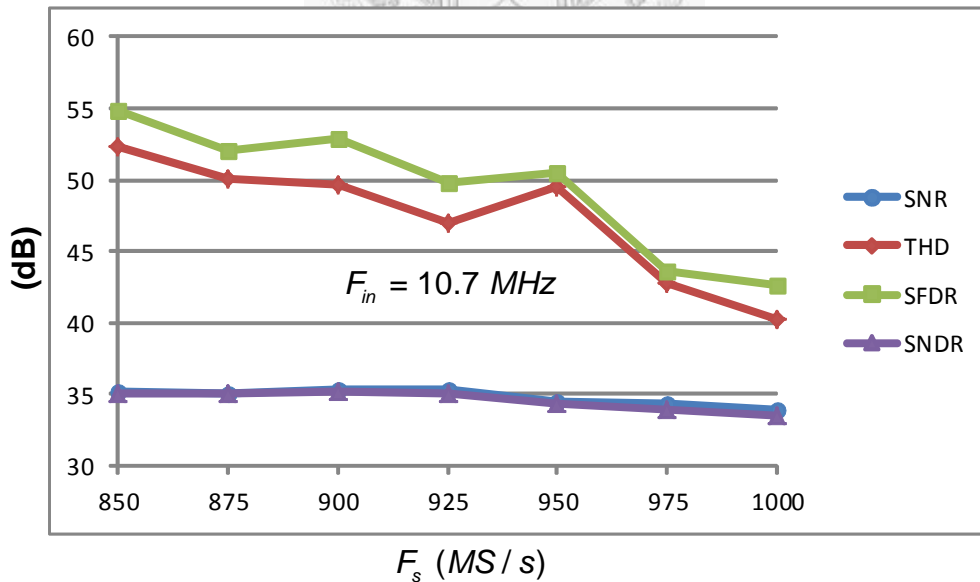


Fig. 5-10 F_s v.s. dynamic performance @ $F_{in} = 10.7 \text{ MHz}$

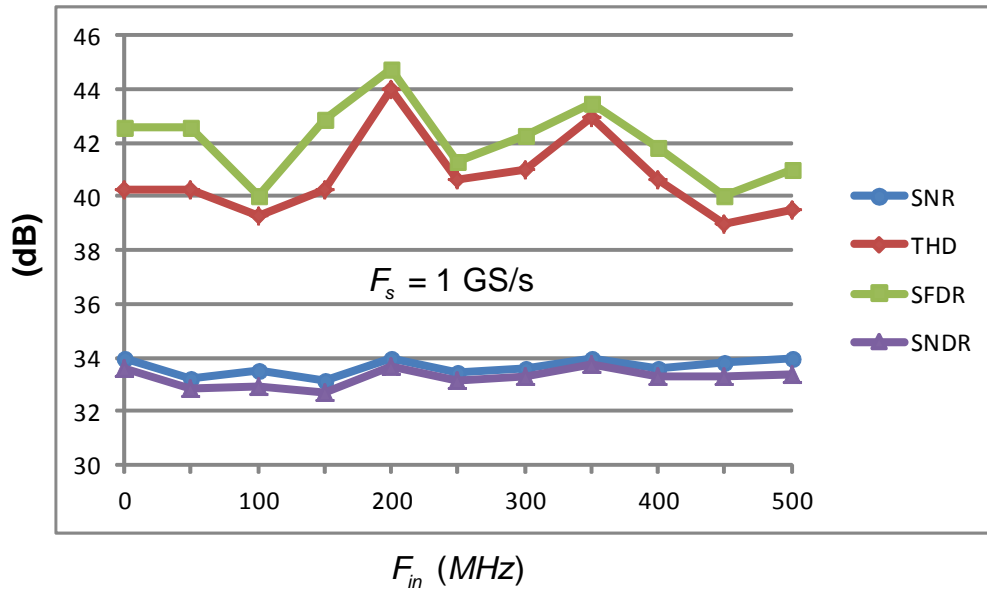


Fig. 5-11 F_{in} v.s. dynamic performance @ $F_s = 1$ GS/s

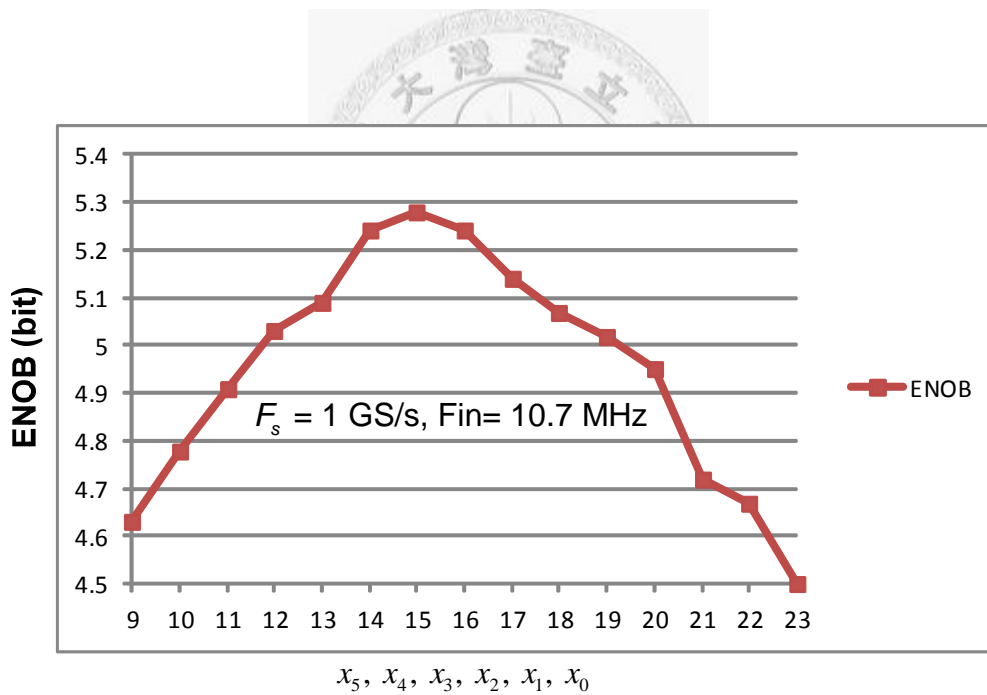


Fig. 5-12 ENOB v.s. binary digital control bits $x_5, x_4, x_3, x_2, x_1, x_0$ in decimal

expression with Sel of DTC set 0 @ $F_s = 1$ GS/s, $F_{in} = 10.7$ MHz

5.6 Summary

6-bit, 1GS/s pipelined ADC using incomplete-settling technique with background sampling-point calibration is implemented in this thesis. The performance of ADC in measurement is summarized in Table 5-2.

Technology	TSMC 65nm CMOS GP		
Resolution	6-bit		
Active Area	0.3 mm ²		
Supply Voltage	1 V		
Sampling Rate	900 MS/s	1 GS/s	
Power	59.4 mW (analog 29.0 mW, digital 6.3 mW, and clock 24.1 mW)*	62.0 mW (analog 29.1 mW, digital 6.8 mW, and clock 26.1 mW)*	
DNL	+0.50/-0.56 LSB	+0.72/-0.68 LSB	
INL	+0.46/-0.54 LSB	+0.76/-0.68 LSB	
Input Frequency	9.7 MHz	10.7 MHz	499.0 MHz
SNR	35.45 dB	33.94 dB	33.99 dB
THD	-46.7 dB	-40.27 dB	-39.54 dB
SFDR	49.50 dB	42.58 dB	41.03 dB
SNDR	35.17 dB	33.57 dB	33.39 dB
ENOB	5.55 bits	5.28 bits	5.25 bits
FoM	1.41 pJ/step	1.60 pJ/step	1.63 pJ/step

Table 5-2 performance of ADC

*include calibration circuits

Table 5-3 compares this work with other pipelined ADC with 5-bit to 8-bit resolution.

	This Work	2006 JSSC [1]	2007 JSSC [11]	2009 JSSC [19]	2011 JSSC [20]
Technology	65nm	0.18um	0.18um	0.13um	65nm
Active Area (mm ²)	0.30	-	0.50	-	0.04
Resolution (bits)	6	5	6	5	8
Fs (GS/s)	1	0.6	0.8	4.8	2.4
Number of Channels	1	1	2	4	1*
Power (mW)	62	70	105	300	309
THD @Nyquist (dB)	-39.5	-	-	-	-36.3
SFDR @Nyquist (dB)	41.0	-	37.5	-	40.7
SNDR @Nyquist (dB)	33.4	25.6	31.5	30.4	31.3
ENOB @Nyquist (bits)	5.25	3.96	4.94	4.76	4.91
FoM (pJ/step)	1.63	7.50	4.28	2.31	4.28

Table 5-3 comparison of 5-bit to 8-bit resolution pipelined ADC

*double-sampling

Chapter 6 Conclusions

In this thesis, 6-bit, 1GS/s pipelined ADC is realized. It adopts incomplete-settling technique with proposed background sampling-point calibration to lower the requirements for opamp dc gain and unit gain bandwidth. Then the power consumption of opamp can be reduced. However, the existence of sampling attenuation is beyond expectations. Proposed background sampling-point calibration works with sampling attenuation under the premise of following two. First, the turn-on resistance of the sampling switches of each stage should be small. In other words, the size of the sampling switches should be very large. This implies that the size of the buffers of the clock generator should be very large, too. Hence, the power consumption of the clock generator is unexpectedly large. Second, an additional replica stage is needed. This not only increases the power consumption of the clock generator due to additional loading, but also adds additional opamp from the additional replica stage. Because of sampling attenuation, the total power consumption of ADC is larger than anticipation.

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- [1] A. Varzaghani and C. K. Yang, "A 600-MS/s 5-Bit Pipeline A/D Converter Using Digital Reference Calibration" *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 310–319, February 2006.
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