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應用於具備低待機功耗之隔離型切換式電源供應器的回授電路研究

Study of Feedback Circuit for Low-Standby-Power Isolated Switch-Mode Power Supplies

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本論文係張家榮君（F97943001）在國立臺灣大學電子工程學研究所完成之博士學位論文，於民國 102 年 6 月 27 日承下列考試委員審查通過及口試及格，特此證明

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Study of Feedback Circuit for Low-Standby-Power Isolated Switch-Mode Power Supplies

By

Chang, Chia-Jung

Dissertation

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誌謝

能完成這一本研究論文，實得力於許多人的幫助。首先感謝陳秋麟教授的指導，我從教授身上學到的，不單只是做研究的部份，更多的是在待人處世的態度與思考邏輯的訓練上。在日常研究生活中，老師也很關心學生們，也樂於與學生分享他的生活經驗。這麼長的歲月能與教授以一種益師益友的關係相處，是我一輩子難忘而且珍惜的回憶。俗話說：「一日為師，終生為父。」除了謝謝老師在研究上的指導與工作上的信賴，未來山高水長，希望還會有機會跟老師一起共事。

接著，要謝謝許多人的指導。謝謝李教授，你對研究的執著與一絲不苟的態度是我很好的學習對象，也謝謝你曾經對我的信任與特別的一對一指導，即便最後我們處的不甚愉快，但我還是非常謝謝你以前給的訓練。懷德、豆哥，你們是我進入電路設計領域的啟蒙學長，多虧你們長達一年半的全套各種教學與訓練，甚至是跟老師的應對，都幫助我為之後的獨立研究階段建立了非常穩固的基礎。蘇老大、洪爺，謝謝你們以業界的職業身分來協助我的研究題目並給予我電路設計方面的指導，讓我除了能以非常快的速度掌握自己的研究以外，也讓我在設計電路時的思考更為全面。

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研究的路途顛簸難行，但終究是順利完成。一個人的力量太渺小，絕不足以完成一個大研究。時時得之於人者太多，單純出之於己者太少。要謝謝的人太多，最後還是謝謝上帝的帶領吧。

摘要

本論文旨在探討具備低待機功耗之隔離型切換式電源供應器的回授電路。傳統的回授電路使用一光耦合器來回授輸出資訊，然而，其雙邊的電流將隨著系統輸出能量的減少而增加，造成系統的損耗增加，而最糟的狀況將發生在輸出無負載之時。這一現象對於追求低待機功耗的系統設計者來說，無疑是一大障礙。

有鑑於此，我們提出一可應用於隔離型切換式電源供應器的回授電路，此電路能在轉換器操作於無載時將光耦合器雙邊之電流降至幾乎為零。在這個所提出的回授架構裡，我們使用了一個新提出的反相式並聯穩壓器來產生用於光耦合機制的誤差訊號，而為了接收此誤差訊號並產生正確的驅動訊號，必須採用一個修改過的脈波寬度調變控制器來搭配。此回授架構的能量損耗分析與頻率補償分析均詳述於本論文中。其與傳統回授架構相較，本論文提出的架構具備有極低待機功耗的特色。此外，轉換器操作於輕載時的效率也可有效提升。

為了建構所提出的回授方案，我們使用世界先進公司 0.5-μm、5-V/40-V 的高壓互補式金屬氧化物半導體製程設計並製作了先前提到的脈波寬度調變器與反相式並聯穩壓器等兩顆積體電路。利用這兩顆積體電路，我們實作了兩個輸出電壓 12 伏特、最大輸出功率 18 瓦並分別採用傳統與本文提出之回授架構的返馳式轉換器。實驗結果顯示與採用傳統回授架構的轉換器比較，採用本論文提出之回授方案的返馳式轉換器可以在操作於無載狀況下時減少至少 27 mW 的功率損耗。不僅如此，在輸入電壓為 $110\sqrt{2}$ 伏特狀況下，當操作於最大輸出功率 10%的輸出能量(1.8 瓦輸出能量)下，系統可以提升 2.2%的轉換效率；而操作於最大輸出功率 5%的輸出能量(0.9 瓦輸出能量)下，系統可以提升 3.6%的轉換效率。

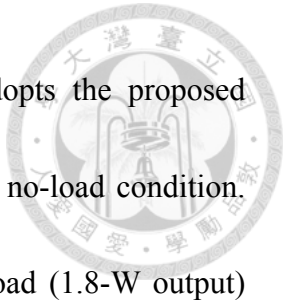
關鍵字：回授架構、切換式電源供應器、待機功耗、脈波寬度調變器、反相式並聯穩壓器。

Abstract

This dissertation focuses on the feedback circuit for isolated switch-mode power supplies with low-standby power. The conventional feedback network uses an optocoupler to feedback the output information; however, the currents of that optocoupler on its two sides get larger with the decrease of the output power, and the worst case happens when there is no output load applied. This fact leaves an obstacle for system designers to pursue a low standby power.

In view of this, a feedback network for isolated switch-mode power supplies that automatically reduces the currents flowing through the optocoupler to nearly zero under the no-load condition is proposed. This feedback network uses a proposed reverse-type shunt regulator to generate an error signal for optical coupling, and a modified pulse-width-modulation (PWM) controller is adopted to receive the feedback signal. The power loss analysis and the frequency compensation method are both presented in this dissertation. In comparison to the conventional topology, this proposed one exhibits much lower standby power loss. Besides, light-load efficiency can be improved as well.

For implementing the proposed scheme, the PWM controller and the reverse-type shunt regulator are designed and fabricated in VIS 0.5-μm 5-V/40-V high-voltage CMOS technology. Two 12-V/18-W flyback converters adopting respectively the proposed and the conventional feedback topology are then implemented to compare



with each other. Experiments reveal that the converter which adopts the proposed feedback technique will save a power of at least 27 mW under the no-load condition. The system efficiency is also improved by 2.2% under the 10%-load (1.8-W output) condition and by 3.6% under the 5%-load (0.9-W output) condition when the input voltage is $110\sqrt{2}$ V.

Index terms: Feedback topology, switch-mode power supply, standby power, pulse-width-modulation (PWM) controller, reverse-type shunt regulator.

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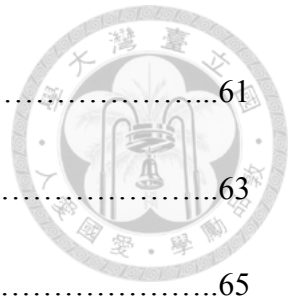

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Chapter 1

Introduction

1.1 Background

Over the decades, the number of electronics products has continued to increase rapidly. As a result, the accumulated energy loss caused by their power supply devices has gradually been a significant part of total electricity expenditure. Among this energy loss, there is a great portion that can be mainly attributed to the standby power loss, which is normally defined as the electricity used by appliances while they are not performing their primary functions. Since the early 1990's, institutes and government agencies have started to raise the profile of standby power. Up to the present, numerous studies to estimate the amount of standby leakage power in different regions have been conducted [1]-[9]. Fig. 1.1 summarizes these investigation results. The y-axis represents the estimated total standby loss as a fraction of the total residential electricity, and the x-axis indicates the year of survey. From this figure, it can be concluded that standby power generally accounts for 3% to 13% of whole residential electricity use. This considerable energy burden does not only accelerate the use of energy resources, but deteriorate the global carbon balance. For example, the annual residential standby power consumption in Australia was evaluated to account for $1.1 billion in energy cost

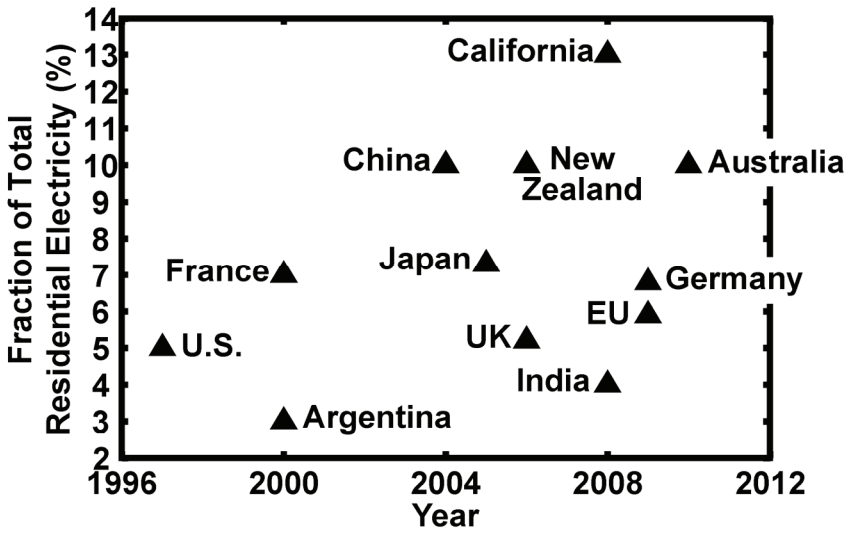


Fig. 1.1. Summary of global standby power surveys.

and nearly 5.7 million tons of carbon dioxide emissions [1]. In order to cut down the enormous energy waste, more stringent standards and product labels targeting even lower standby power consumption have been successively established. For instance, according to the existing regulations and ratings of product labels [10]-[14] which are summarized in Fig. 1.2, today's top-ranked low-power battery charger on the market must consume less than 30 mW (an extremely low value compared to the requirement of the "1-Watt Plan" proposed in 1998 [15]) in the standby mode. This situation can be found in other types of products as well, leading to a motivation for both industry and academia to work on promoting the performances of power supply devices.

1.2 Motivation

A power supply unit basically deals with mains voltages to provide a proper voltage for supplying an end-point electronic device with the demanded current.

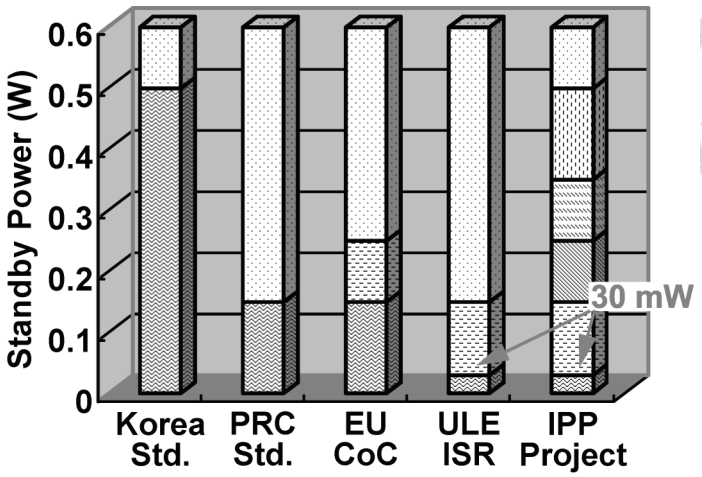


Fig. 1.2. Regulations and ratings of product labels for low-power battery chargers.

However, when a electronic device enters its standby mode, its current demanding will be very little and the power dissipation of the power supply unit itself may instead become the largest portion of the total energy use of the whole system. This fact drives us to focus on the power loss of a supply device under very light/no-load conditions.

To find out what are the causes of energy losses, we first inspect every part of an ordinary power supply unit. A typical architecture of an isolated offline switch-mode power supply is shown in Fig. 1.3. It mainly comprises an EMI filter, a bridge rectifier, and an isolated DC-DC converter. A power-factor-correction stage, if required, should be added after the rectifier. The DC-DC stage can be further divided into three parts: a power stage, an isolated feedback network, and a controller. In order to reduce the standby loss of a system, the power consumption under very light/no-load conditions should be kept as low as possible [16]-[20]. Over the past few years, a lot of researches and techniques have been reported and many of them have already been adopted in

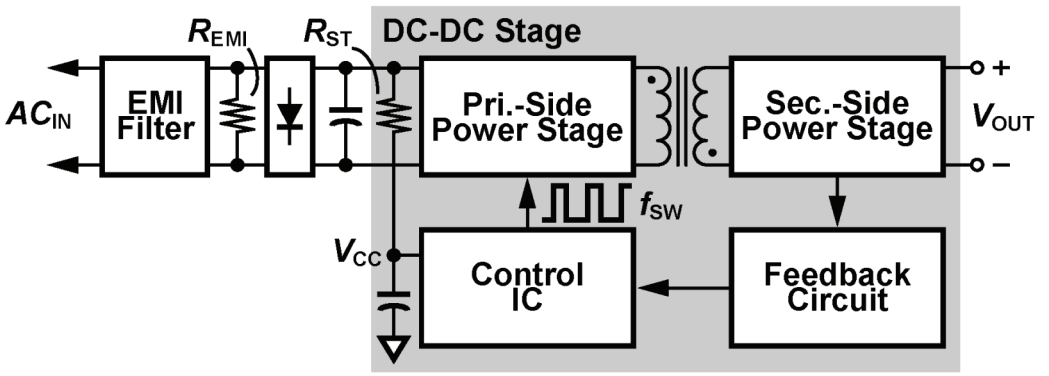


Fig. 1.3. Architecture of isolated offline switch-mode power supply.

commercial products. For example, to minimize switching losses, several modulation techniques including pulse-frequency modulation [21]-[30], pulse-skipping modulation [31]-[38], and burst mode control [39]-[42] are often mixedly used with pulse-width modulation (PWM) in switch-mode power supply circuits to decrease the equivalent switching frequency (f_{SW}) under light/no-load conditions. Other major sources of power dissipation include the start-up resistor (R_{ST}) and the bleeding resistor (R_{EMI}). The former provides a current path to activate the control IC during start-up; the latter is used for discharging the stored energy in the EMI filter whenever the AC input is cut off from the system. Under normal operation, however, these two resistors will continuously dissipate energy, resulting in unnecessary power loss. Thanks to the development of high-voltage process technology that allows control ICs to be tied directly to mains voltages, approaches to switching off the start-up path [43] and the bleeding path of EMI filter [44], [45] were also proposed to solve the problems. With all the above techniques and a low-power commercial control IC applied, the standby

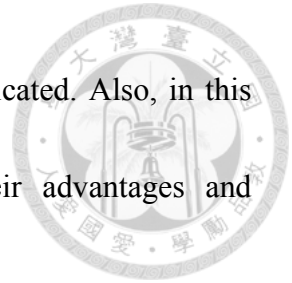
power loss of a supply unit like that in Fig. 1.3 can be reduced down to below 100 mW, and the remaining power consumption principally comes from the feedback circuit.

Feedback network also causes severe standby power loss. On account of isolation requirements for safety concerns, feedback via optical coupling is very prevalent in the industry. However, the use of an optocoupler requires two large branch currents to flow through it. In the conventional feedback topology, these two currents will reach their maximum values under the no-load condition, leading to a high standby power loss. Over a long period of time, feedback network has had a fixed circuit structure in consideration of the cost. In the past times when standby power was not of great concern, the conventional feedback circuit performs well in most of applications in which the isolated feedback is needed. Nevertheless, when we have to start caring about every milliwatt of power leakage, the feedback scheme which we are familiar with then seems to have room for improvement. It thus inspires us to develop a new feedback method that meets our present expectation for low-standby-power consumption.

1.3 Dissertation Overview

In this dissertation, five chapters in total are included, and each of them is briefly described as follows.

In Chapter 2, the conventional feedback circuit for isolated switch-mode power converters will first be reviewed. After the operating principles are explained, the



essential difficulty suffered by the conventional circuit will be indicated. Also, in this chapter, previous related researches will be analyzed, and their advantages and disadvantages will be pointed out.

Chapter 3 presents the proposed feedback network to address the power loss issue. The proposed solution aims at minimizing its standby power consumption while ensuring feasible compensation of control loop. The central concept is provided first and then is followed by system and circuit design considerations. At last, the power loss and the control loop compensation method of the proposed feedback network will be analyzed, respectively.

All of the materials related to experiments will be given in Chapter 4. Contents include the design and fabrication of integrated circuits, the implement of the proposed and the conventional systems for testing and comparison, measurement approaches, experimental results, and discussions on the outcomes.

Finally, Chapter 5 summarizes this dissertation and gives ideas for future work.

Chapter 2
Conventional Isolated Feedback Network and Previous Researches

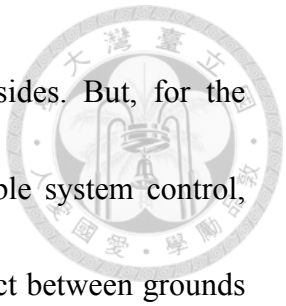
2.1 Introduction

This chapter comprises two major parts. The first part introduces the basic knowledge of the conventional isolated feedback network, including the operating principles and the compensation method. Since what we care the most about is the power loss when a power converter operates under very light/no-load conditions, the power analysis of the feedback network will be carried out as well. The second part includes three recent techniques that can help reduce the power dissipation of the feedback network under very light/no-load conditions. Both their advantages and disadvantages will be discussed.

2.2 Conventional Feedback Network

2.2.1 Architecture

Generally, in order to meet the safety regulations (e.g., IEC 60950) for safety concerns, the outputs of power supplies must be kept insulated from inputs to ensure galvanic isolation. For power stages, it will not be a problem since we can easily choose those transformer-isolated topologies, such as flyback and forward topologies where



their secondary sides are inherently isolated from their primary sides. But, for the control loop to feedback the output information and acquire a stable system control, additional efforts and cost should be paid to prevent electrical contact between grounds on the input and output sides. Among contactless signal transmission techniques, the magnetic flux coupling through a transformer and the AC (alternating current) signal coupling through a capacitor are not favorable because in this case it is supposed to feedback a very-low-frequency analog signal. Instead, optical coupling through an optocoupler proves to be a cost-effective approach to transmit such a feedback signal. A typical optocoupler is most likely composed of an infrared light-emitting-diode (LED) and a phototransistor, which are encapsulated into one same package. The strength of the emitted light from the LED will be determined by the current flowing through it, and the phototransistor will convert the light that reaches its base terminal into its collector current.

Fig 2.1 shows a transformer-isolated power converter with a conventional feedback network where an optocoupler is used as an interface of signal transmission. A shunt regulator rather than an operational amplifier is placed in series with the optocoupler to pull down an error signal of current for flowing through the LED inside that optocoupler. In comparison to a standard operational amplifier, a shunt regulator is a low-cost single IC with simply three pin connections such that it is overwhelming for applications in

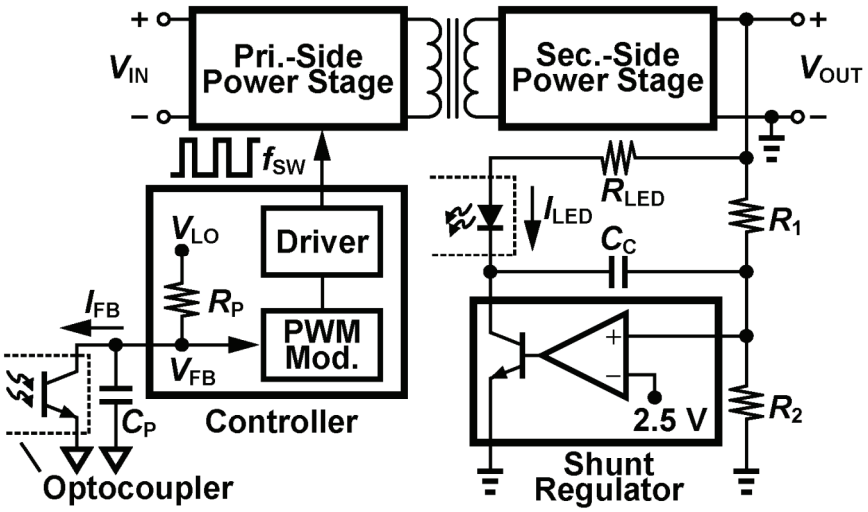


Fig. 2.1. Conventional feedback network in a transformer-isolated topology.

power conversion. Its internal circuit structure can be viewed as an operational amplifier with its output driving an npn bipolar transistor, which makes its output capable of sinking current only. The inverting terminal of the internal operational amplifier is connected to a built-in reference voltage. When the voltage on the non-inverting terminal is below the reference voltage, the npn transistor remains open-circuit and the shunt regulator is transparent to the circuit. As long as the voltage exceeds the reference, the transistor will begin to conduct.

In Fig. 2.1, the input voltage V_{IN} can be from the previous power-factor-correction stage or directly from the rectified AC line. A PWM controller is used to receive the feedback signal from the phototransistor inside the optocoupler and, in response to the feedback information, output switching pulses to control the ON/OFF of the power switches in the primary-side power stage. The entire feedback network, which consists of R_1, R_2, C_C, R_{LED}, C_P, a shunt regulator (commercially well-know as TL431), and an

optocoupler, delivers the output voltage V_{OUT} information to the PWM controller while maintaining galvanic isolation between the primary and the secondary sides.

2.2.2 Operating Principle

Fundamental operating principles of the feedback circuit are delineated as follows. In Fig. 2.1, V_{OUT} is divided by the voltage divider which is composed of R_1 and R_2. The shunt regulator compares the divided output voltage with its built-in reference voltage, and an error signal I_{LED} is drawn according to their difference. The current I_{LED}, sunk by the shunt regulator, will flow through R_{LED} and the LED inside the optocoupler. With the help of the optocoupler, I_{LED} is transferred to the primary side by a current transfer ratio *CTR*. A resistor R_P which will generally be integrated in the PWM controller connects the phototransistor collector to an internal supply voltage V_{LO}, and the induced primary-side current I_{FB} will be converted to a voltage form V_{FB}. V_{FB} will next be modulated by the PWM modulator to produce gate-driving signals, and finally the gate driver outputs the modulated pulses to switch the power devices in the primary-side power stage.

Overall speaking, when V_{OUT} drops and the divided output voltage is lower than the built-in reference voltage in the shunt regulator, which means, in the system's point of view, the converted energy is insufficient for supporting the present output current request, I_{LED} and I_{FB} will be decreased to raise V_{FB}. A higher V_{FB} results in a higher

inductor current limit and therefore makes the modulator increase the duty cycle of the driving pulse, and eventually more energy is delivered to the output. In contrast, when the converted energy exceeds the output request and V_{OUT} grows up, I_{LED} and I_{FB} will be increased to reduce V_{FB}. Due to the lower current limit caused by the lower V_{FB}, the modulator decreases the pulse duty cycle, making less energy converted by the converter in a switching period.

The modulator in today's green-mode PWM controller may be somewhat more complicated than just described. Fig. 2.2 portrays a probable control scheme arrangement in commercial products. In order to reduce switching losses, it is very common that when V_{FB} drops to a green-mode threshold voltage V_{GR}, the modulator starts using pulse-frequency modulation (PFM) to decrease the switching frequency in stead of keeping trying to reduce the pulse width for regulation. Besides, burst mode [39], [40] is widely adopted to control a converter under very light/no-load conditions (i.e., V_{FB} is lower than V_{BU}). In the later discussion where the standby power is analyzed, we will describe the burst mode operation in more details.

The above principles are not limited to any converter topology, that is, this conventional feedback circuit is applicable to many kinds of transformer-isolated topology. Fig. 2.3 gives two examples, one of which is a flyback converter and the other one is a forward converter. Although they differ in the configurations of power stage,

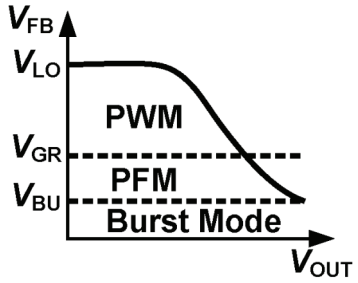
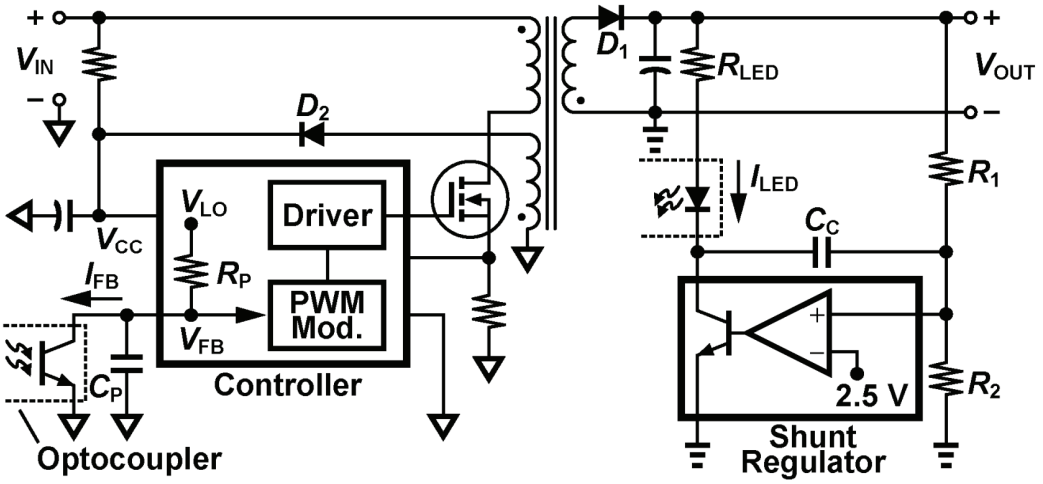
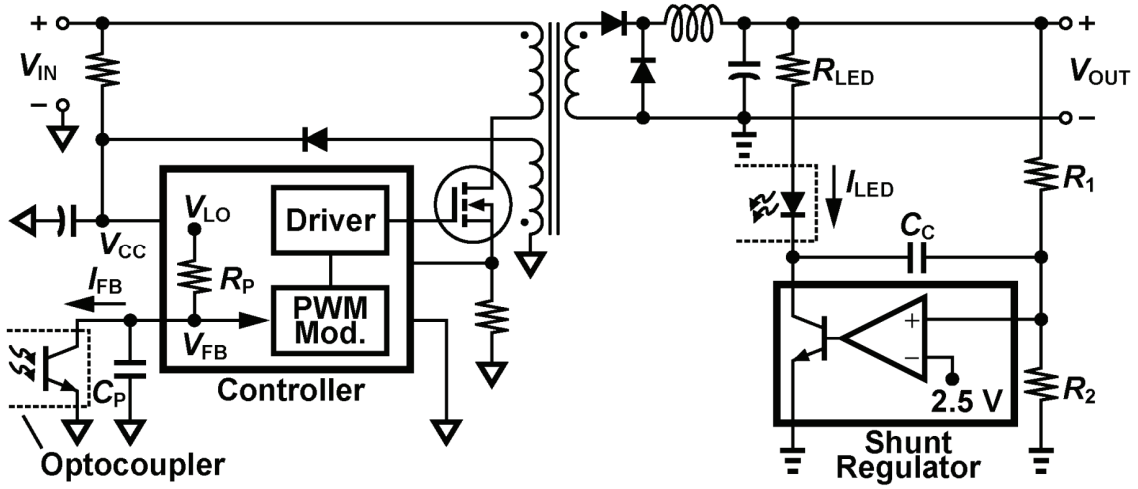


Fig. 2.2. The relationship of V_{FB} versus V_{OUT} and the control scheme division.



(a)



(b)

Fig. 2.3. Conventional feedback network in (a) flyback and (b) forward topologies.

the functions of their feedback circuits are exactly identical.

2.2.3 Control Loop Compensation

The conventional feedback circuit also provides frequency compensation for stabilizing the control loop. To have deeper insights into how the compensator works, we can simply perform the small-signal analysis on the feedback circuit. Fig. 2.4 illustrates the small-signal equivalent circuit of the feedback network from V_{OUT} shown in Fig. 2.1 to V_{FB}. The shunt regulator can be modeled as a voltage-controlled current source with a transconductance G_m, and the optocoupler is treated as a current-controlled current source with a current gain of *CTR*. The internal pole of the optocoupler is considered by including C_{OPT}. Note that the dynamic resistance of the light emitting diode is much smaller than R_{LED} and therefore is omitted from the following analysis.

By observing Fig. 2.4, we can first recognize that I_C is the difference of currents through R_1 and R_2. That is,

$$I_C = \frac{V_1}{R_2} - \frac{V_{OUT} - V_1}{R_1}. \tag{2.1}$$

Also, we can find two expressions for V_2:

$$\begin{aligned} V_2 &= V_{OUT} - I_{LED} R_{LED} \\ &= V_{OUT} - (G_m V_1 + I_C) R_{LED} \end{aligned} \tag{2.2}$$

and

$$V_2 = V_1 + \frac{I_C}{sC_C}. \tag{2.3}$$

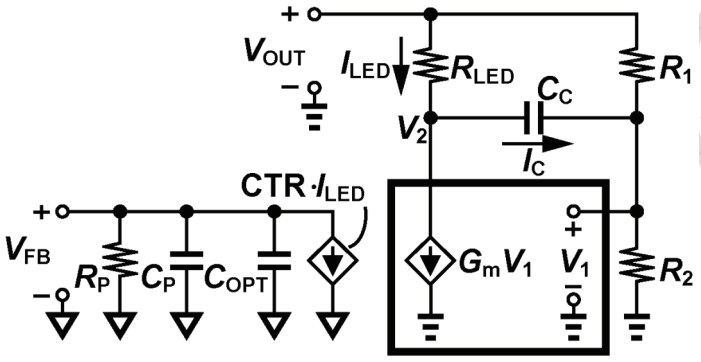


Fig. 2.4. Small-signal equivalent circuit of the conventional feedback circuit.

Equating (2.2) with (2.3), substituting (2.1) into it, and rearranging that, we can obtain V_1 as a function of V_{OUT}:

$$V_1 = \frac{1 + \frac{R_{LED}}{R_1} + \frac{1}{sR_1C_C}}{G_m R_{LED} + \left(\frac{1}{R_1} + \frac{1}{R_2}\right)R_{LED} + 1 + \left(\frac{1}{R_1} + \frac{1}{R_2}\right)\frac{1}{sC_C}} V_{OUT} \cdot \tag{2.4}$$

Since

$$I_{LED} = G_m V_1 + I_C \tag{2.5}$$

and

$$V_{FB} = -CTR \cdot I_{LED} \cdot \frac{R_P}{1 + sR_P\left(C_P + C_{OPT}\right)}, \tag{2.6}$$

we can finally arrive at the overall transfer function by substituting (2.1), (2.4), and (2.5) into (2.6):

$$\frac{V_{FB}}{V_{OUT}} = G_0 \frac{1 + s\omega_z^{-1}}{\left(1 + s\omega_{p1}^{-1}\right)\left(1 + s\omega_{p2}^{-1}\right)} \tag{2.7}$$

where

$$G_0 = -\frac{R_P R_2 G_m}{R_1 + R_2} \cdot CTR\,, \tag{2.8}$$

$$\omega_z = \frac{1}{\left(\frac{R_1}{R_2 G_m} + R_1\right) C_C} \approx \frac{1}{R_1 C_C}, \tag{2.9}$$

$$\omega_{p1} = \frac{1}{\left[(R_1 \parallel R_2)(R_{LED} G_m + 1) + R_{\mathrm{LED}}\right] C_C} \approx \frac{1}{(R_1 \parallel R_2) R_{LED} G_m C_C}, \tag{2.10}$$

and

$$\omega_{p2} = \frac{1}{R_P (C_P + C_{OPT})}. \tag{2.11}$$

From equation (2.7), we can find that this network exhibits a two-pole one-zero characteristic. Since a current-mode control power stage has only one dominant pole at low frequencies of interest, this conventional feedback network thus can be easily utilized for the type-1 or type-2 compensations [46]. The dominant pole ω_{p1} is created by the Miller effect capacitor C_C, and the second pole ω_{p2} is formed basically by the internal capacitor of the optocoupler and can be adjusted by varying capacitor C_P.

To design a type-2 compensator, the very first step starts from drawing the Bode plot of the well-designed power stage that is going to be compensated, as shown in Fig. 2.5. Then, we have to choose a crossover frequency f_C for the final loop gain. Regarding how to select f_C, previous literature [47] has given a method to analytically derive the crossover point depending on the specification of the maximum undershoot. Now, since the final loop gain has to cross the 0-dB line at f_C, we can design the midband gain G_{MID} of the compensator to cancel out the extra gain of the power stage at f_C. The midband

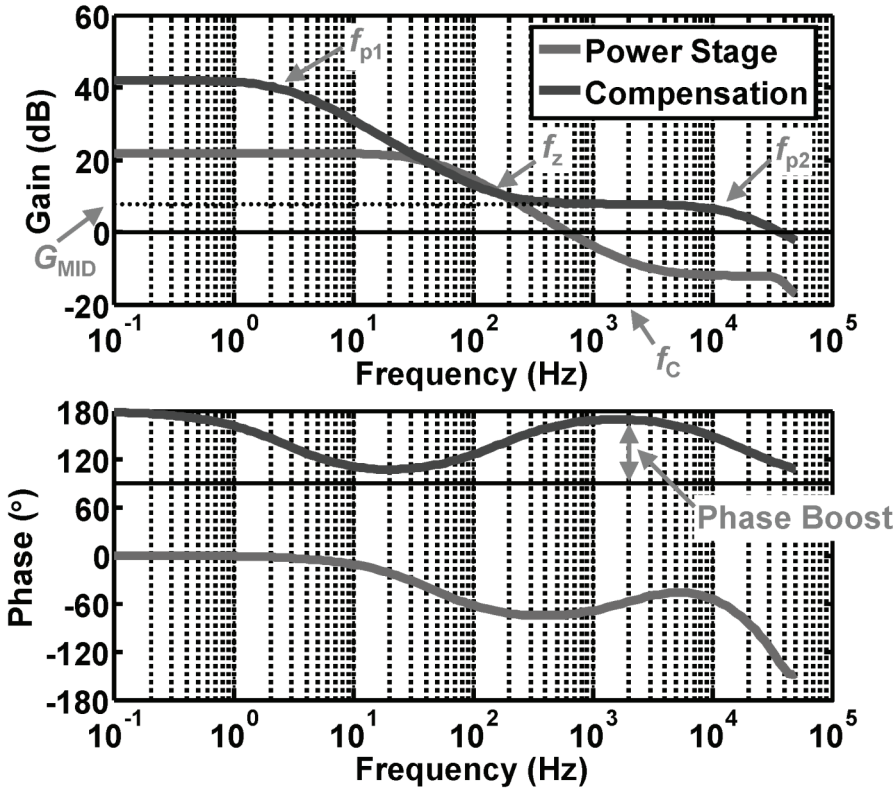


Fig. 2.5. An example of compensator design.

gain can be derived as

$$G_{MID} = \frac{R_P \cdot CTR}{R_{LED}}. \tag{2.12}$$

Note that it has nothing to do with C_C and, for system designers, the only way to adjust G_{MID} is to vary R_{LED}. After G_{MID} is defined, the actual locations of f_z and f_{p2} can be selected based on how much phase boost is required at f_C and thus C_C and C_P can be calculated out [48]. In this example, the Bode plot of the final loop gain is sketched in Fig. 2.6. As for the type-1 compensation, it can be done by making f_z and f_{p2} coincident to leave f_{p1} alone.

Although the compensator in the conventional feedback network suffices for the needs in most of applications, there exists a limitation of choosing the midband gain. To

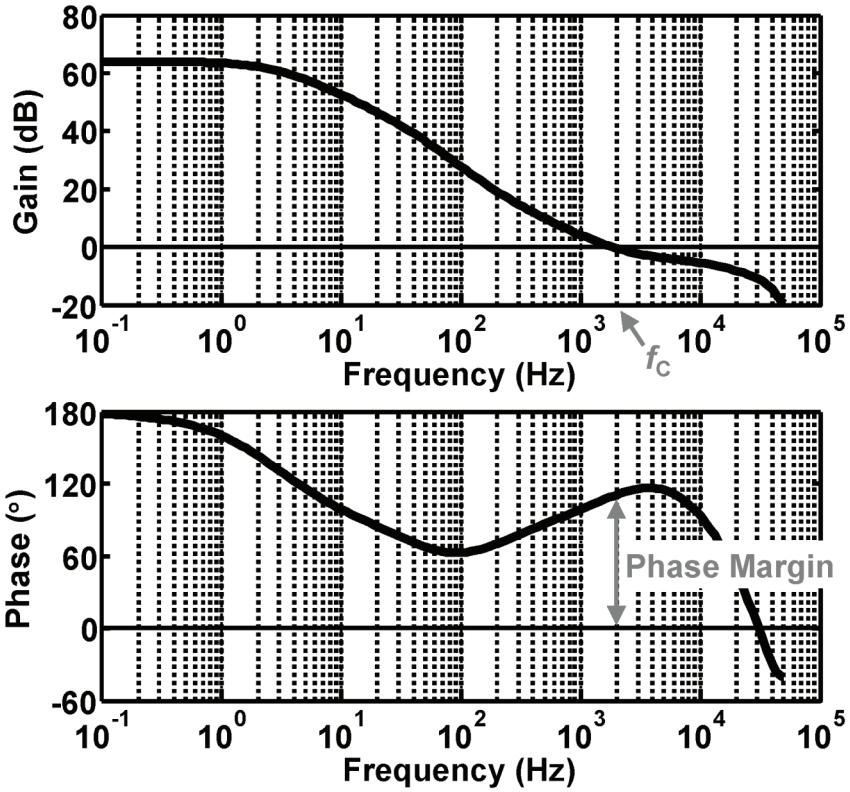
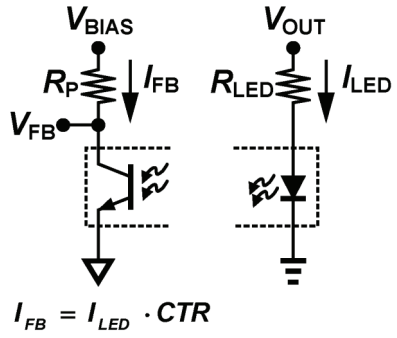
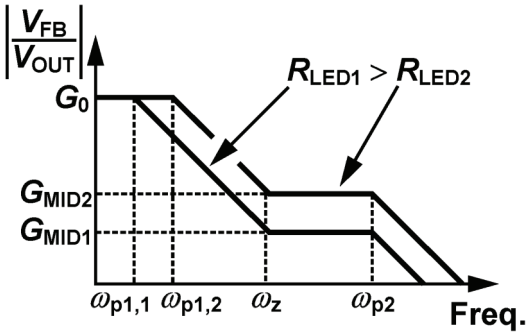


Fig. 2.6. Bode plot of compensated loop gain.

realize this restriction, we observe the circuit structure drawn in Fig. 2.7(a). We can find that since there requires a certain amount of I_{FB} flowing through the phototransistor collector for dropping down V_{FB}, R_{LED} will inherently have an upper limit to allow of a large-enough I_{LED}. The resulting difficulty indicated by equation (2.12) is that the type-2 compensator will suffer from a minimum midband gain limitation, which implies the design freedom to boost or attenuate the power-stage gain curve at the selected crossover frequency is also limited [48]. The reason why it causes this phenomenon is that the only means for system designers to adjust the ratio of the first pole to the zero is to vary R_{LED}. As shown in Fig. 2.7(b), a larger R_{LED} will result in a lower midband gain without moving the zero. Therefore, to be more precise, the restriction in choosing R_{LED}



(a)



(b)

Fig. 2.7. (a) Circuit that limits R_{LED} and (b) the effect of R_{LED} on midband gain.

actually limits how far the first pole and the zero can be separated, leading to a trouble achieving the desired midband gain.

2.2.4 Power Loss Analysis

In Section 2.2.2, since the whole ideas about the operation of the feedback network have been introduced, we now focus on the power loss that caused by this network. Refer to Fig. 2.1, we observe that there exist three current branches. The first one is the current consumed by the resistor divider (R_1 and R_2), while the second and the third one are I_{LED} and I_{FB}, respectively. If we temporarily do not consider the loss inside the power stage, then, based on the observation, we can formulate the power loss of the

feedback network as

$$P_{L,con.} = \frac{V_{OUT}^2}{R_1 + R_2} + V_{OUT} I_{LED} + V_{CC} I_{FB} . \quad (2.13)$$

Note that V_{CC} is the supply voltage of the control IC. Since I_{LED} can be expressed as I_{FB} divided by *CTR*, we can rewrite (2.13) as

$$P_{L,con.} = \frac{V_{OUT}^2}{R_1 + R_2} + I_{FB}\left(\frac{V_{OUT}}{CTR} + V_{CC}\right). \quad (2.14)$$

Finally, replace I_{FB} by

$$I_{FB} = \frac{V_{LO} - V_{FB}}{R_P}, \quad (2.15)$$

and (2.14) will become

$$P_{L,con.} = \frac{V_{OUT}^2}{R_1 + R_2} + \left(\frac{V_{LO} - V_{FB}}{R_P}\right)\left(\frac{V_{OUT}}{CTR} + V_{CC}\right). \quad (2.16)$$

This equation is an ideal approximation, where many non-idealities are not taken into account. For instance, if we consider voltage drops of diodes in a flyback converter as shown in Fig. 2.3(a), (2.16) can be modified as

$$P_{L,con.} = \frac{V_{OUT} \cdot V'_{OUT}}{R_1 + R_2} + \left(\frac{V_{LO} - V_{FB}}{R_P}\right)\left(\frac{V'_{OUT}}{CTR} + V'_{CC}\right) \quad (2.17)$$

where

$$V'_{OUT} = V_{OUT} + V_{D1} \quad (2.18)$$

and

$$V'_{CC} = V_{CC} + V_{D2} . \quad (2.19)$$

Remember that we still do not consider the transformer loss and switching loss in (2.17)

for simplicity. The second term of (2.16) or (2.17) is essentially caused by currents flowing through the optocoupler, and it gives us a hint that the steady-state voltage of V_{FB} will determine the actual power loss. In view of this, we proceed to discuss how much does it really contribute to the standby power when the system operates under very light/no-load conditions.

We have known from Section 2.2.2 that a typical controller will adopt the burst mode to control a converter when its output demands very little current. Under this circumstance, what does V_{FB} behave like? Fig. 2.8 gives simulated waveforms of a typical flyback converter operating in the burst mode. V_G is the gate driving signal for a switching power device. If the current request at the output is drastically reduced, V_{FB} is going to drop continuously due to excessive power delivery. When it falls below the burst-mode threshold voltage V_{BU} set in the controller, the output switching pulses will be blocked. After the converter's output voltage drops down and V_{FB} recovers to exceed V_{BU}, the driving signals will be released again. As suggested by the name, burst mode, this blocking-and-releasing mechanism makes V_G look like a periodic burst of consecutive pulses and causes V_{FB} to move around the burst-mode threshold voltage V_{BU}. Therefore, when a system operates in the burst mode, we can estimate (2.16) or (2.17) as

$$P_{L,con.} \approx \frac{V_{OUT}^2}{R_1 + R_2} + \left(\frac{V_{LO} - V_{BU}}{R_P} \right) \left(\frac{V_{OUT}}{CTR} + V_{CC} \right) \tag{2.20}$$

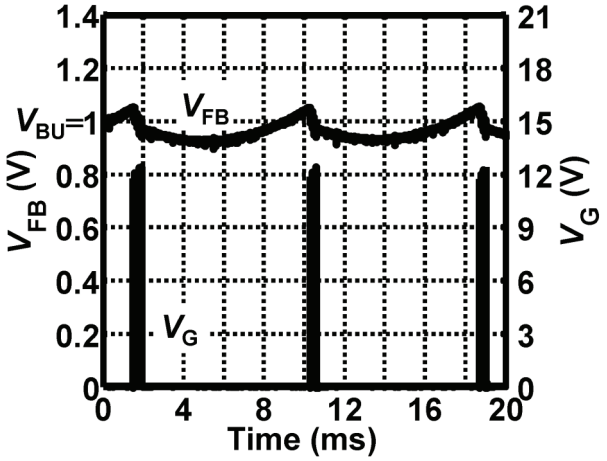


Fig. 2.8. Simulated waveforms of a conventional flyback converter in burst mode.

or

$$P_{L,con.} \approx \frac{V_{OUT} \cdot V'_{OUT}}{R_1 + R_2} + \left(\frac{V_{LO} - V_{BU}}{R_P} \right) \left(\frac{V'_{OUT}}{CTR} + V'_{CC} \right). \tag{2.21}$$

Take a typical 12-V flyback converter with V_{CC} = 10 V, V_{LO} = 5 V, R_P = 4 kΩ, and V_{BU} = 1 V as an example. Assume that *CTR* is 100% and forward voltages of diodes are both 0.5 V. In the burst mode, the second term in (2.21) will result in a 23-mW power loss, leading to an obstacle to the low-standby-power target.

Through the previous discussion, we have known that a higher V_{FB} will correspond to a lower V_{OUT} and the modulator should increase its output pulse width for keeping a constant output voltage. Fig. 2.9 shows the relationship between V_{FB} and the output power in a conventional flyback converter. As a higher inductor peak current is demanded by a heavier load, V_{FB} should stay at a higher level to have a larger inductor current limit. Therefore, I_{FB} and hence I_{LED} are smaller under this condition. In contrast, when the load gets lighter, V_{FB} drops to a lower value and both I_{LED} and I_{FB} become

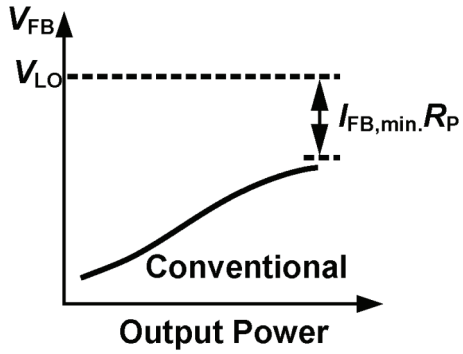


Fig. 2.9. The relationship between steady-state V_{FB} and the output power.

larger. This means the power loss expressed by (2.16) or (2.17) will increase while the output power becomes smaller, and the worst case happens when there is no output load applied. Although this amount of loss looks small in value, it evidently degrades the light-load efficiency and, more importantly, occupies a significant portion of the total standby power. Since most of the time, power supplies operate only in the light to medium load range [49] or just remain plugged in but idle, this conventional feedback topology seems to be unfavorable from an energy-saving point of view. Of course, one can reduce steady-state I_{LED} and I_{FB} by raising the value of R_P. However, a minimum current $I_{LED,min.}$ is still required to supply the shunt regulator for proper functioning, and this current will cause a minimum voltage drop equaling $I_{FB,min.}R_P$ across R_P, as indicated in Fig 2.9. Thus, using a too large R_P here will leave V_{FB} a very small voltage dynamic range and result in poor noise immunity for the feedback path. Besides, Fig. 2.10 shows the normalized frequency response of a commercial optocoupler [50] with different R_P values. A larger R_P gives rise to a lower-frequency pole, which means the

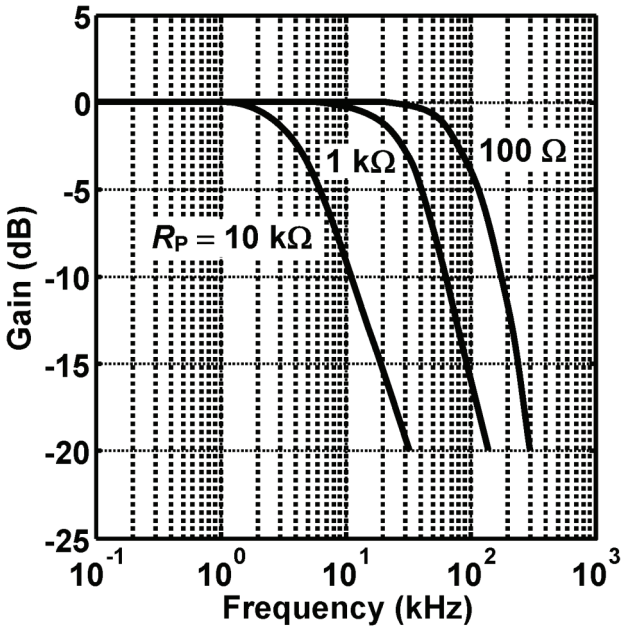


Fig. 2.10. Frequency response of a commercial optocoupler with different R_P values.

design freedom of the second pole ω_{p2} given in (2.11) is limited. Therefore, the maximum value of R_P is also limited by the desired crossover frequency of a converter.

2.3 Previous Solutions

We have introduced the whole background knowledge about the feedback network in previous sections, and also the power loss disadvantage has been pointed out and explained. In recent years, there have been some companies issuing patents to address this problem. With an attempt to obtain and learn some experiences, prior published techniques toward the standby power loss issue are summarized and compared with each other in this section.

2.3.1 Primary Sensing Technique

The primary sensing [51]-[54] means the output information is not feedback

through the explicit signal path. Instead, it tries to extract the output voltage from the information already existing on the primary side. Hence, the entire feedback network can be removed. Not only the cost can be largely saved from this technique, but also the losses due to current branches in the conventional feedback network disappear. Fig. 2.11 shows a simplified primary-side-control flyback converter, where there is no any direct signal path for feedback except for the flux coupling through the flyback transformer.

To show how the voltage extraction technique takes effect, the operating waveforms of the converter in Fig. 2.11 are illustrated in Fig. 2.12. To obtain the V_{OUT} information, we first recognize that the ratio of the transformer winding voltages is proportional to that of their turn numbers. That is,

$$V_{PW} : V_{SW} : V_{AUX} = N_P : N_S : N_A . \tag{2.22}$$

In t_1 shown in Fig. 2.12, the power MOS is turned ON and V_{DRAIN} is nearly shorted to the ground. The flyback transformer is charged with V_{PW} equal to V_{IN}, making the primary-side inductor current I_{LP} continuously climb up. Due to the flux coupling, the auxiliary winding (tertiary winding) then reflects a voltage of $-(N_{\mathrm{A}}/N_{\mathrm{P}})V_{\mathrm{IN}}$. Next, in t_2 when the power MOS is turned OFF, the transformer starts discharging through the secondary winding. The secondary winding sees a voltage V_{SW} equal to V_{OUT} plus the diode voltage V_{D1}, so the secondary-side inductor current I_{LS} declines gradually with a slope of $-V_{\mathrm{SW}}/L_{\mathrm{S}}$. In the meantime, V_{AUX} reflects a voltage of

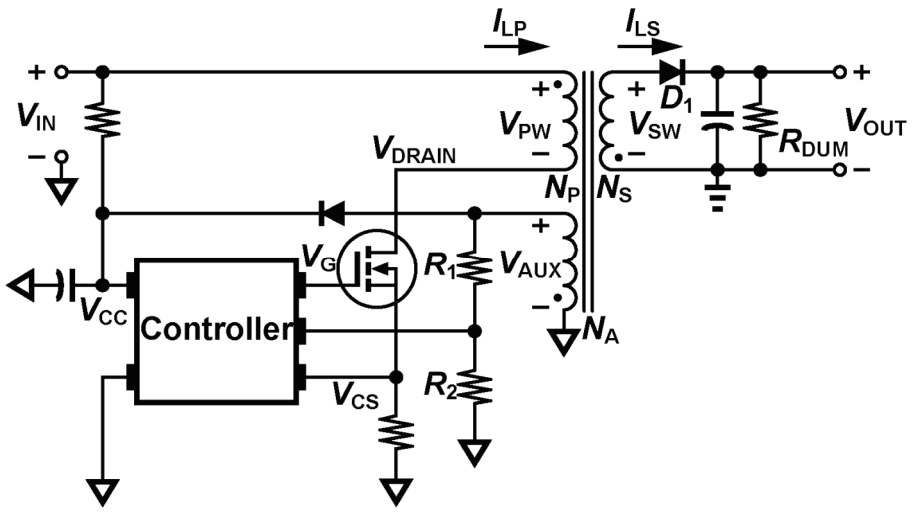


Fig. 2.11. Primary-side control flyback converter.

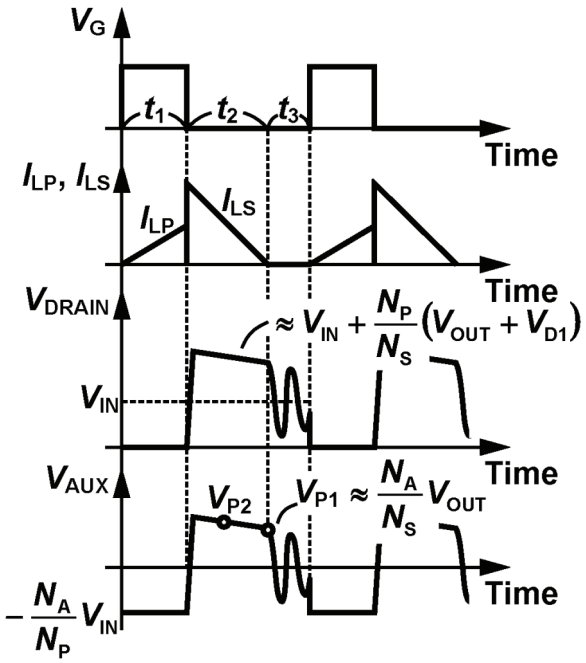


Fig. 2.12. Operating waveforms of primary-side-control flyback converter.

$$V_{AUX} = \frac{N_A}{N_S}\left(V_{OUT} + V_{D1}\right). \tag{2.23}$$

V_{PW} also reflects a voltage, and V_{DRAIN} can be expressed as

$$V_{DRAIN} = V_{IN} + \frac{N_P}{N_S}\left(V_{OUT} + V_{D1}\right). \tag{2.24}$$

The above two equations thus inspire us that they contain the output information in this

period of time. Although theoretically it is possible to obtain V_{OUT} from V_{DRAIN} [51], the quite high voltage there which would probably cause troubles and inconvenience makes it a worse choice. Therefore, V_{AUX} is mostly chosen for extracting V_{OUT} for feedback and the controller IC generally samples the divided V_{AUX}. In t_3, the energy in the transformer is empty. The parasitic capacitance at the drain of the power MOS and the primary-side magnetizing inductance L_P begin to resonate with each other, leading to decayed sinusoidal voltage waveforms of the transformer windings. Now we focus on the t_2 period. Since I_{LS} is getting smaller and so is V_{D1}, V_{AUX} in this time is actually not constant. It then becomes a problem that where is exactly the best point to sample V_{AUX} for extracting V_{OUT}. Some products samples V_{AUX} at the point V_{P1} where I_{LS} is just discharged to zero. At that point, since almost zero current flows through the diode, V_{D1} is nearly zero and V_{AUX} can be approximated as $(N_A/N_S)V_{OUT}$ which is proportional to the output voltage. However, the slope of V_{AUX} around there changes so drastically, making it very difficult to acquire the voltage accurately. Some researches [52] try to sample V_{AUX} at a point prior to V_{P1} (e.g., V_{P2} in Fig. 2.12). If V_{AUX} is captured at a fixed I_{LS} in each cycle, V_{D1} is fixed and we can still take out V_{OUT} from V_{AUX} with high accuracy as well. Compared to V_{P1}, there is no abruptly voltage change around V_{P2}. However, how to ensure a fixed I_{LS} in each sampling time imposes another difficulty to the circuit designers. No matter which sampling point is chosen, both of them tell us

that sampling V_{OUT} from V_{AUX} would basically cause a relatively poor regulation in comparison with directly using the optical-coupling feedback network.

Although this existing primary-side-control power conversion solution which indirectly senses the output information through the auxiliary (tertiary) winding and hence obviates the need for isolated feedback network can achieve low cost and low standby power consumption in nature, it still has many limitations. First, this technique is only applicable to flyback topology. Other topologies in essence do not have the property that the output voltage will be reflected in any of the winding voltages on the primary side. Second, as described just now, the auxiliary winding voltage contains not only the output voltage but also the voltage of the secondary-side rectifier diode, making it very hard to precisely extract the output information. Third, primary-side-control flyback converter is mostly limited to the discontinuous-conduction-mode operation. Because in the continuous-conduction mode, I_{LS} is not going to drop down to zero and thus it is even hard to predict I_{LS} at the sampling point, a primary-side-control converter operating in this mode would encounter an even worse output variation problem. Fourth, there is generally a dummy load R_{DUM} required at the output, as shown in Fig. 2.11, leading to an additional power dissipation. When there is no output load applied, switching may be required only after a long period of time to maintain the output voltage. However, this fact also makes the controller blind of the output voltage

in that period of time. To ensure a prompt response to a suddenly applied heavy load, primary-side controllers must possess a maximum OFF-time limit to keep updating the output condition and a dummy load is thus necessary to prevent the over voltage at the output node.

From the above, it is therefore that such converters generally suffer from poor output regulation and also have a very limited application scope. As a result, using an optocoupler to feedback information is still necessary in most applications and, consequently, lowering down the power dissipation of isolated feedback network under the no-load condition is potentially of great interest. In the following sections, two circuit techniques are introduced to reduce the no-load power loss of the conventional feedback network.

2.3.2 Output Voltage Control Method

In [55], a technique called output voltage control of power converters was disclosed. Originally designed based on flyback topology, this technique requires only circuit designs inside the controller without any change in the system structure shown in Fig. 2.3(a). In Fig. 2.9, since V_{FB} decreases (due to the increase of V_{OUT}) with the output power, the central concept in [55] is to drop the output voltage to lower down I_{LED} under very light/no-load conditions. The entire on-chip feedback circuit reported in [55] is redrawn in Fig. 2.13. V_{FB} should still be connected to the phototransistor collector of an

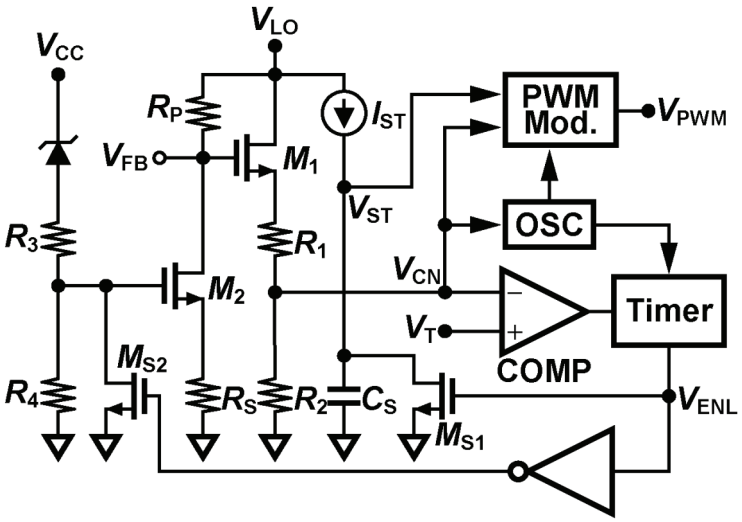


Fig. 2.13. Primary-side feedback circuit of output voltage control method with V_{FB} and V_{CC} as feedback signals.

optocoupler, and V_{CC} is the supply voltage. V_{ST} which is generated by using a current source I_{ST} to charge a capacitor C_S serves as a current limit in start-up process. A modulator takes two inputs V_{ST} and V_{CN}, and actually the lower one of the two voltages acts as the current limit or the ramp limit for modulating pulse signals. An oscillator provides clock signals for the PWM modulator and a timer, and its frequency may slow down if V_{CN} (which will be described later) drops too low. A comparator is used to determine whether or not the controller enters the light-load operation mode by comparing V_{CN} with V_T.

Under heavy load conditions, V_{CN} will be larger than V_T and the indicator V_{ENL} is low. Therefore, switch M_{S1} is open and M_{S2} is closed, and we can simplify the circuit in this situation as shown in Fig. 2.14. It is very similar to the conventional feedback circuit introduced before. M_1 only provides level shift, and $R_{1\text{-}2}$ are used to desensitize

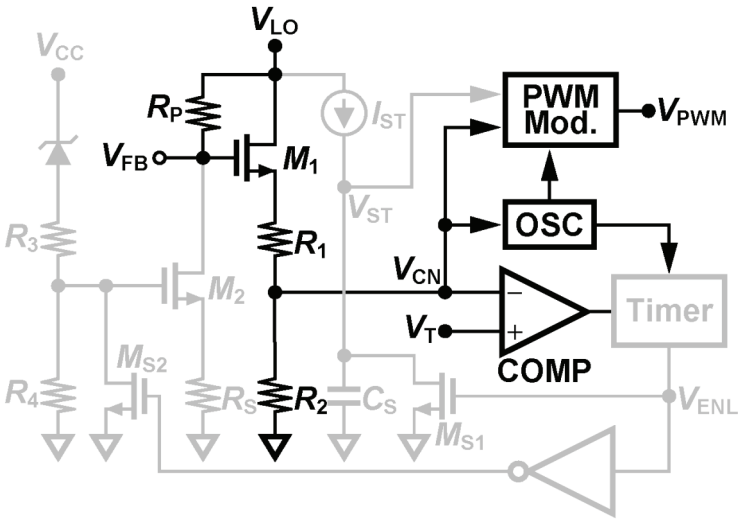


Fig. 2.14. Simplified feedback circuit under heavy load conditions.

the feedback signal to the noise interference at V_{FB}. The modulator at this time generates a pulse signal according to V_{CN} (after the start-up), and the comparator keeps monitoring V_{CN} in case the output load becomes very light.

When the output load is changed to a quite light load, V_{OUT} will run high such that V_{CN} drops lower than V_T. The comparator thus triggers the timer and V_{ENL} is turned to logic HIGH. Now, two things take place. One, M_{S1} shorts V_{ST} to the ground, making the modulator only output pulses with a minimum ON-time at this moment. Two, M_{S2} is opened. V_{CC} after being blocked a reference voltage by the zener diode and then divided by $R_{3\text{-}4}$ now begins to conduct M_2. V_{FB} is thus further dropped to an even lower value. At this time, although the modulator only generates minimum ON-time pulses, V_{CN} will adjust the switching frequency to control the power delivery. It is not the output voltage of the converter but V_{CC} that is the controlled target and is going to be regulated to a

certain lower level. Through the transformer coupling, V_{OUT} will be also maintained to a lower value than before. Hence, I_{LED} and I_{FB} [refer to Fig. 2.3(a)] are largely reduced to save power dissipation. Once a heavy load is applied to the output, the converter's output voltage continuously drops and the flyback transformer will deliver most of the inductor's energy to the output rather than V_{CC}. Without enough energy replenishment, V_{CC} continuously drops and V_{CN} rises up. If V_{CN} exceeds V_T again for a set time, V_{ENL} is turned to zero and the light-load operation ends up. Nevertheless, to prevent the system from the instability caused by suddenly expanded pulse duty, the converter should undergo a soft-start process again for ensuring a smooth mode switching.

In summary, Fig. 2.15 shows the behaviors of the output voltage V_{OUT} and V_{FB} versus the output power of the converter. When the output load goes from a heavy load to a lighter load, V_{OUT} slightly rises to drop down V_{FB} for less power transfer. In this region, the converter is feedback controlled by the output-directly-related signal V_{FB}. At an output power of P_{T1}, V_{FB} reaches a threshold voltage at which V_{CN} is equal to V_T. The light-load operation mode is enabled, and the V_{CC} feedback control starts dropping V_{OUT} and makes V_{FB} even lower. If the load keeps decreasing, the excessive energy in the transformer will discharge to V_{OUT} and V_{CC}. The increase in V_{CC} will then lower down V_{FB} to further decrease the power transfer. In contrast, when the load demands more current, the decrease in V_{OUT} makes V_{CC} get less energy from the flyback transformer.

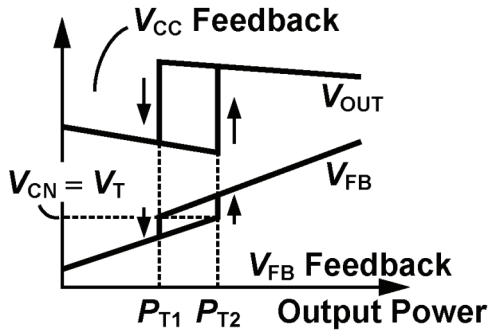


Fig. 2.15. Curves of steady-state output voltage and V_{FB} versus output power.

V_{CC} drops and thus V_{FB} rises. At an output power of P_{T2}, V_{FB} recovers to the voltage where V_{CN} equals V_T again. The V_{CC} feedback control ends up and V_{FB} takes over the system control.

This technique of output voltage control is indeed useful for decreasing the power loss under very light/no-load conditions, but there are three major disadvantages. First of all, in the light-load operation mode, although V_{OUT} is dropped to reduce I_{LED} and I_{FB}, M_2 in Fig 2.13 still has to conduct a large current for pulling down V_{FB}. That is, this technique actually only reduces I_{LED}, but the current flowing through R_P remains unchanged. Moreover, a part of I_{LED} is used for supplying the shunt regulator, leading to a minimum I_{LED} that should always exist even in the light-load operation mode. The second drawback is regarding the mode switching from the light-load to the heavy-load mode. The controller should wait until V_{CC} and thus V_{CN} drops below some certain levels, and after that the converter must again undergo a soft-start process. Therefore, the pretty long response time to a suddenly applied heavy load will cause a large voltage

dip at the output. However, if the soft-start process is not applied when the output load suddenly changes from a light to a heavy load, the abruptly spread duty cycle of gate-driving pulses probably results in the instability. Third, when operating in the light-load mode, a converter adopting this technique hugely relies on the cross regulation to regulated its output voltage. This feature definitely causes poor output regulation as the cross regulation has much to do with the leakage inductance of the transformer, and thus the yield rate in mass production is hard to guaranteed.

2.3.3 Feedback Impedance Modulation

Very recently, in [56], another technique called feedback impedance modulation was revealed to address the power loss issue of the conventional feedback network. Similar to the output voltage control described in Section 2.3.2, this technique provides a controller solution without the need to modify the system circuit. It proposes increasing the value of the resistor which is connected to the collector of the phototransistor inside the optocoupler only under very light/no-load conditions, and the operating current will be reduced to an extent. Fig. 2.16 shows the proposed feedback circuit in [56]. V_{FB} should still be connected to the phototransistor collector of an optocoupler. A resistor string composed of R_1-R_N with each resistor in parallel with a separate switch S_1-S_N is in series with a fundamental feedback resistor R_P, and each of the switches is controlled by an individual digital signal from a counter. A comparator

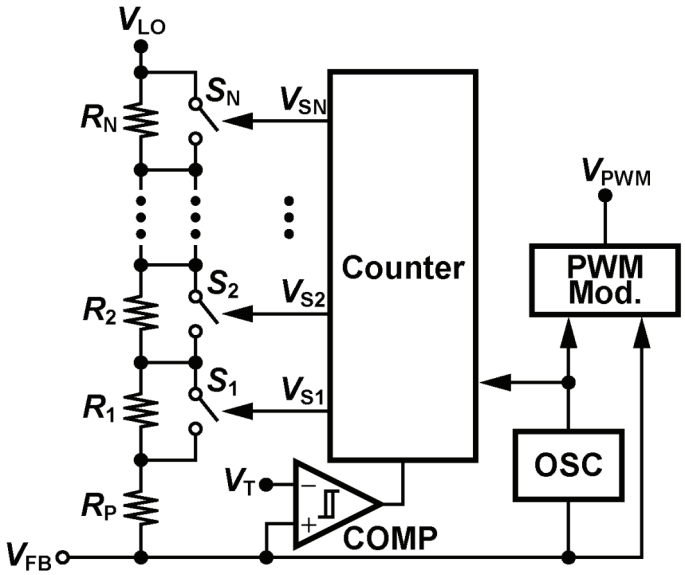


Fig. 2.16. Primary-side feedback circuit with impedance modulation.

with a hysteresis window compares V_{FB} with a threshold voltage V_T to monitor the output load condition, and its output is sent to the counter. V_T is also the burst mode threshold voltage of the controller. An oscillator provides a clock signal for the counter and the modulator with its frequency f_{SW} controlled by V_{FB}, and the PWM modulator generates pulses for gate driving.

When a converter adopting the feedback impedance modulation technique operates under a heavy-load condition, V_{FB} is higher than V_T and all the switches S_1-S_N are closed to bypass the resistor string. The feedback impedance remains only R_P, which is set the same as that in the conventional feedback network. However, when the load varies to a very light/no-load condition, the counter resets all its output signals (V_{S1}-V_{SN}) to zero as soon as V_{FB} drops below V_T. Now, the total feedback impedance Z_{FB} becomes

$$Z_{FB} = R_P + R_1 + R_2 + ... + R_N . \tag{2.25}$$

This abruptly increased feedback impedance will likely let V_{FB} fall down to well below the burst-mode threshold voltage (V_T) because I_{LED} has not been changed at that instant. Then, the output voltage starts dropping a little bit due to the insufficient power delivery. Eventually, it will settle down to a level where the corresponding V_{FB} is approximately equal to the burst-mode threshold voltage since the converter basically operates in the burst mode. In overall, the enlargement of Z_{FB} makes it much easier to drop down V_{FB} with only little I_{FB}, and the resulting effect is that the output voltage drops a little (but it is still regulated) to lower down I_{LED} and thus I_{FB}. Z_{FB} given in (2.25) can be chosen such that the minimum supplying current $I_{LED,min.}$ for the shunt regulator is sufficient for pulling down V_{FB}. Therefore, the power loss of a flyback converter described in equation (2.21) under very light/no-load conditions can be estimated as

$$P_{L,con.} \approx \frac{V_{OUT}'^2}{R_1 + R_2} + I_{LED,\min.} \cdot CTR \cdot \left(\frac{V_{OUT}'}{CTR} + V_{CC}' \right), \tag{2.26}$$

which indicates that the second term is minimized under such traditional system circuit structure. Now, if the output load increases, V_{OUT} drops and V_{FB} rises to exceed V_T. The counter starts gradually bypassing the resistor string as soon as the comparator changes its output state. Why can not all the resistors $R_{1\text{-}N}$ get shorted at a time? Because if we do that, V_{FB} will rush quite highly and the PWM modulator will widen the pulse duty cycle rapidly. Then, the resulting a large amount of energy is poured to the output, which will probably make the controller enter the light-load operation mode again, and

the reciprocating between the light-load and the heavy-load operation modes leads to an instability phenomenon in the end. In view of this, switches $S_{1\text{-}N}$ in Fig. 2.16 will be closed in sequence.

Fig. 2.17 summarizes the complete operating procedure with practical values. When V_{FB} is high, the switching frequency f_{SW} is at its maximum value (say, 60 kHz) and the feedback impedance Z_{FB} is at its minimum value of 5 kΩ. If V_{FB} reduces (but still larger than V_T), f_{SW} may be also decreased with a minimum value of 20 kHz while Z_{FB} still remains at 5 kΩ. Once V_{FB} drops below the burst-mode threshold voltage V_T (a small hysteresis window exists), the switching stops and Z_{FB} is directly switched to a maximum value of 50 kΩ. No switching action in the following time makes V_{FB} recovers. If V_{FB} exceeds V_T, the resistor string begins to be gradually bypassed. Unless V_{FB} falls below V_T once again, Z_{FB} will be decreased from 50 kΩ toward 5 kΩ with a step of 1 kΩ in every switching cycle. Fig. 2.18 shows the transient waveforms of V_{FB} and the gate-driving pulses in the burst mode. In the switching-ceased period, Z_{FB} is 50 kΩ, while within the burst period every switching pulse is accompanied with a 1-kΩ decrease of Z_{FB}.

Compared with the output voltage control technique [55] which regulates V_{CC} in the light-load operation mode, a converter adopting this feedback impedance modulation technique still controls the output voltage rather than other system variables.

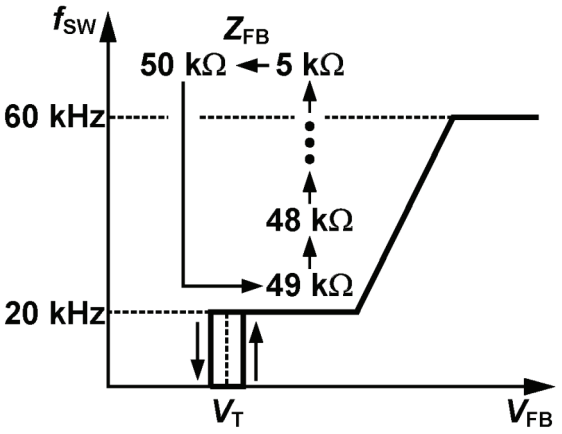


Fig. 2.17. The change of Z_{FB} and the relationship between switching frequency f_{SW} and V_{FB}.

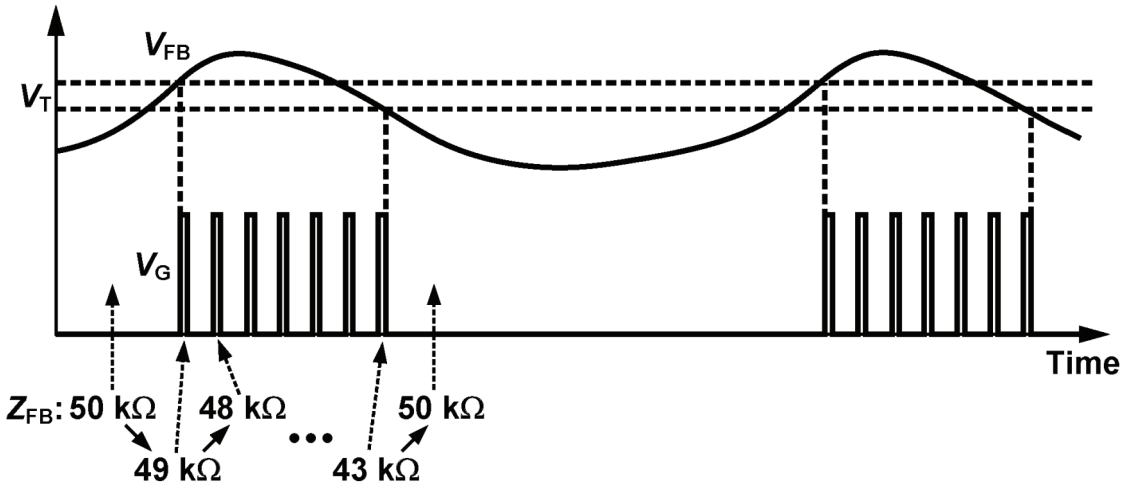


Fig. 2.18. Waveforms of V_{FB} and gate-driving signal in burst mode operation.

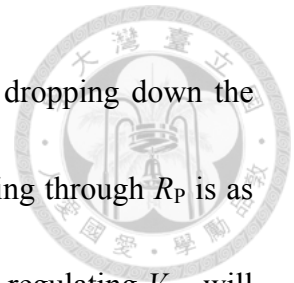
Therefore, the output regulation is largely improved. Besides, although both of the two techniques [55], [56] aim at minimizing currents of the optocoupler, the current flows through R_P is in fact not reduced in [55], making the the reduction in power loss not thorough enough. However, both of the two techniques would cause a risk of instability when their systems go from light-load to heavy-load conditions. It is therefore that a slow recovery procedure (i.e., the soft-start process in [55] or the gradual resistors

bypass in [56]) is necessary in both of the techniques, and this shortcoming brings about the need to trade off the response time required for the transient from a very light to a much heavier load.

2.4 Conclusion

The conventional feedback network is widely adopted in isolated offline switch-mode power supplies in industry owing to the benefits of the simple circuit structure and low cost. However, the power loss under very light/no-load conditions makes it become an obstacle for designers to pursue low standby power. Besides, although the compensator of the conventional feedback network suffices the needs in most applications, there exists a minimum midband gain limitation on building the type-2 compensation, which degrades the flexibility in system design.

Previous literature provides some techniques to address the power loss issue. Primary-side control removes the entire traditional feedback network and features low standby power and low cost. Nonetheless, a primary-side-control converter has a poor output regulation and is mainly limited to the discontinuous-conduction mode due to the difficulty in extracting the output voltage. Furthermore, the necessity of a dummy load at the output increases the power loss. The output voltage control technique and the feedback impedance modulation offer controller solutions without any change in the system circuit. Under very light/no-load conditions, the output voltage control technique



regulates the supply voltage of the controller to a lower value for dropping down the output voltage. Although I_{LED} and I_{FB} are reduced, the current flowing through R_P is as large as before. Besides, controlling the output voltage indirectly by regulating V_{CC} will give rise to a poor output regulation. The feedback impedance modulation switches the feedback impedance to a high value under very light/no-load conditions. The current flowing through R_P is truly reduced, and the output voltage is kept regulated. However, both the feedback impedance modulation and the output voltage control technique require a long recovery process to avoid the instability when the load changes from a light to a heavy one, leading to a long transient response time.

Chapter 3

Low-Standby-Power Output Feedback Scheme

3.1 Introduction

The proposed output feedback scheme with low standby power consumption is introduced in this chapter. Beginning from the central concept that originated from the previously described knowledge, the following sections explain the whole thoughts on the design of the proposed feedback network circuit step by step. After that, the analyses of the power loss and the compensation method are carried out and compared with those of the traditional feedback network. Finally, comparisons with prior techniques are provided to reveal the superiority of this solution.

3.2 Phase Reversal Concept

In Section 2.2.4, we have disclosed that the power loss of the conventional feedback network increases with the decrease of the output power and it comes to a maximum value while there is no output load applied. Although the power consumption can be reduced by existing approaches [55], [56] under very light/no-load conditions, it is still not minimized and those techniques need to sacrifice the light-to-heavy-load transient response time for ensuring the system stability. These facts thus motivate us to think over the possibility of a better solution.

To overcome the difficulty suffered by the conventional feedback topology, we first review the relationship between V_{FB} and the output power, as the gray line shown in Fig. 3.1. Two major problems can be pointed out. One, the positive correlation between V_{FB} and the output power is unfavorable for pursuing a low standby power. Two, the current for supplying the shunt regulator causes a minimum voltage drop across R_P and leads to irremovable losses on both the primary and the secondary sides. In consideration of these, we come up with a helpful solution to reverse the situation. The fundamental concept is that, as shown in Fig. 3.1, we flip the conventional V_{FB} curve vertically. The resulting new V_{FB} curve (black line) suggests that a higher V_{FB} should correspond to a lighter load, making the power loss due to I_{LED} and I_{FB} decrease with the output power. That is, the phase relationship between I_{LED} (or I_{FB}) and the output power is reversed. In this way, the power consumption naturally shrinks to a minimum value when no load is presented at the output. Besides, to eliminate the voltage drop $I_{FB,min.}R_P$ caused by the supply current of the shunt regulator and in the meanwhile to prevent that current from causing power loss on the primary side, we should keep the supply current from flowing through the optocoupler.

3.3 System Architecture

For realizing the proposed concept, the whole feedback circuit should be thought over. Starting from the circuit on the secondary side to the primary side, the circuit

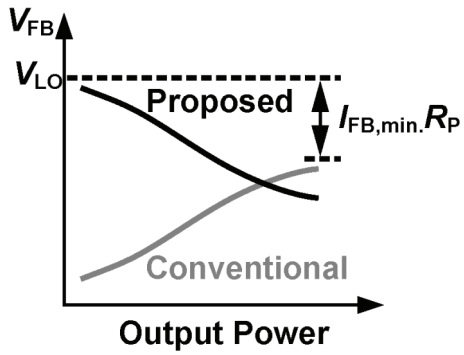


Fig. 3.1. V_{FB} versus the output power in conventional and proposed networks.

design considerations are fully uncovered in the following subsections.

3.3.1 Secondary Side

To make V_{FB} increase with the decrease of the output power, we should try to reduce I_{FB} when the output demands less energy such that the output voltage starts growing. This means the desired correlation between I_{FB} and the output voltage should be reversed compared to that in the conventional circuit. With this observation, the first thought coming to our minds is that it can be easily achieved by simply interchanging the positive and the negative terminals of the operational amplifier in the shunt regulator, as shown in Fig. 3.2(b). For reference, the conventional circuit is also illustrated in Fig. 3.2(a). However, the configuration in Fig. 3.2(b) makes it not a negative feedback path from V_2 back to V_1. The Miller capacitor C_C thus can not be placed between the two nodes to build a dominant pole. A compromise is to connect the capacitor between V_3 and V_1; however, not only an additional pin is required but also the output current capability of the operational amplifier should be quite enhanced for ensuring a sufficient

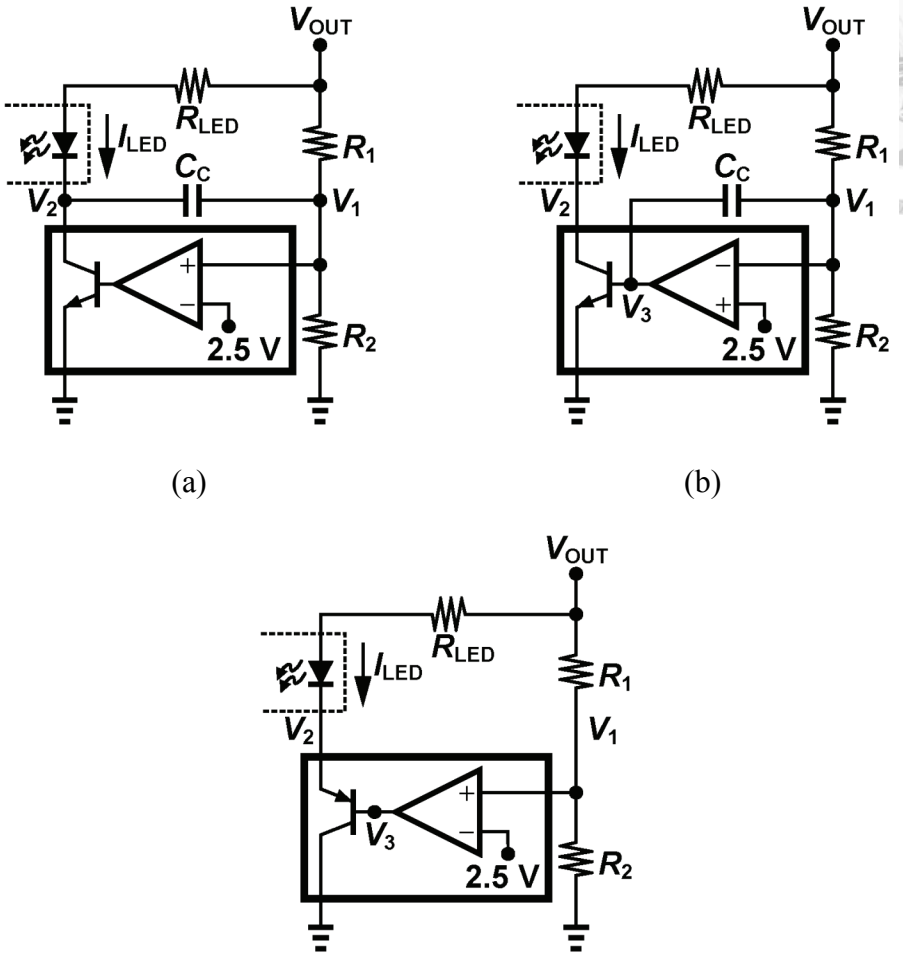
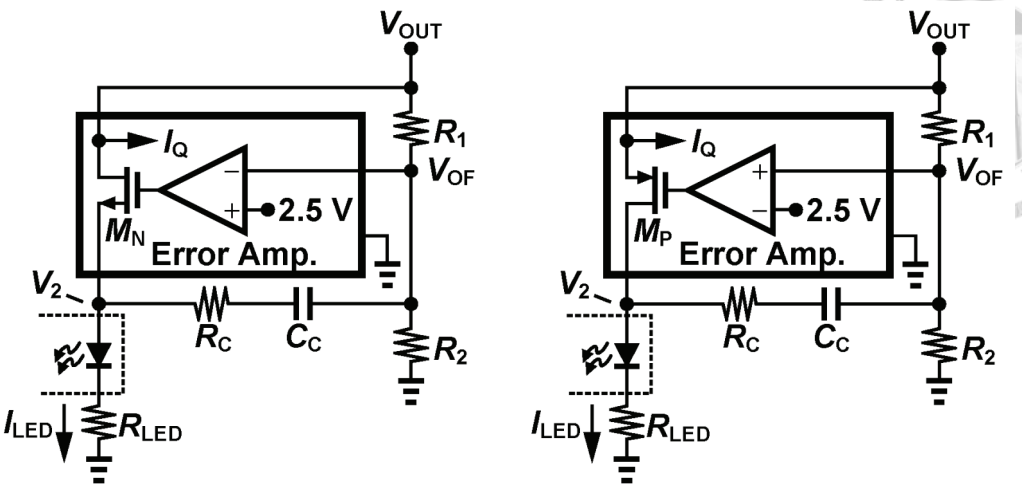


Fig. 3.2. (a) Conventional secondary-side feedback circuit and (b)(c) two modifications.

slew rate. These outcomes make this solution not really fascinating at all. Instead of interchanging the two input terminals of the operational amplifier, another choice is to replace the npn transistor with a pnp type. In Fig. 3.2(c), the pnp transistor fundamentally acts as an emitter follower, and now V_2, V_3, and V_1 all have the same phase polarity. The Miller compensation therefore can not be built between any two of the three nodes, which discourages the feasibility of this idea.

Through the two previous trials of circuit modification, we get to understand that

the expected relationship between I_{LED} and the output voltage will destroy the negative feedback path from V_2 to V_1. The reason is that I_{LED} flows through R_{LED} before through the current-controlling transistor. With this recognition, we then attempt to change that sequence and offer two possible structures drawing in Fig. 3.3. In both Fig. 3.3(a) and (b), V_{OUT} is divided by R_1 and R_2 to V_{OF}, and an operational amplifier (functionally an error amplifier) amplifies the difference of V_{OF} and a reference voltage to drive a current-controlling device. Note that here we use a MOS transistor rather than a bipolar transistor as the current-controlling device just because we will apply a CMOS process technology to implement chips. In Fig. 3.3(a), the nMOS M_N works as a source follower, while the pMOS M_P in Fig. 3.3(b) is configured as a common-source amplifier. An optocoupler and a resistor R_{LED} are placed in series between the current-controlling device (M_N or M_P) and the ground. Functionally speaking, both of the two possible structures meet our need for a negative correlation between V_{OUT} and I_{LED}. The major difference between the two circuits in Fig. 3.3 and the three in Fig. 3.2 is that the current-controlling devices in Fig. 3.3 directly connect to V_{OUT} to serve as current sources rather than current sinks. As a result, when V_{OUT} and thus V_{OF} increase, M_N in Fig. 3.3(a) or M_P in Fig. 3.3(b) lowers down I_{LED} and V_2 also drops. This represents that the path from V_2 back to V_{OF} is a negative feedback where the Miller compensation can be constructed. Since both of the two circuits in Fig. 3.3 are feasible, what are exactly



(a) (b)

Fig. 3.3. Two practical secondary-side circuits with, respectively, (a) nMOS and (b) pMOS as current-controlling devices.

their merits and drawbacks in comparison with each other? In Fig. 3.3(a), the source follower provides better noise immunity as V_{OUT} would see a relatively large impedance toward M_N. However, the serious body effect of M_N enlarges its threshold voltage badly. Even though there is a device called isolated nMOS which enables its body and source to be tied together, it consumes a relatively large area in comparison with a standard nMOS. In view of this, we eventually make a choice of the pMOS as the current-controlling device. Note that I_Q in Fig. 3.3 is the current for supplying the internal error amplifier and the voltage reference, and that current will not pass through the current-controlling device. By separating it from I_{LED}, the minimum values of I_{FB} and I_{LED} are basically not limited.

3.3.2 Primary Side

Fig. 3.4(a) is the original primary-side feedback circuit. If we do nothing to it but

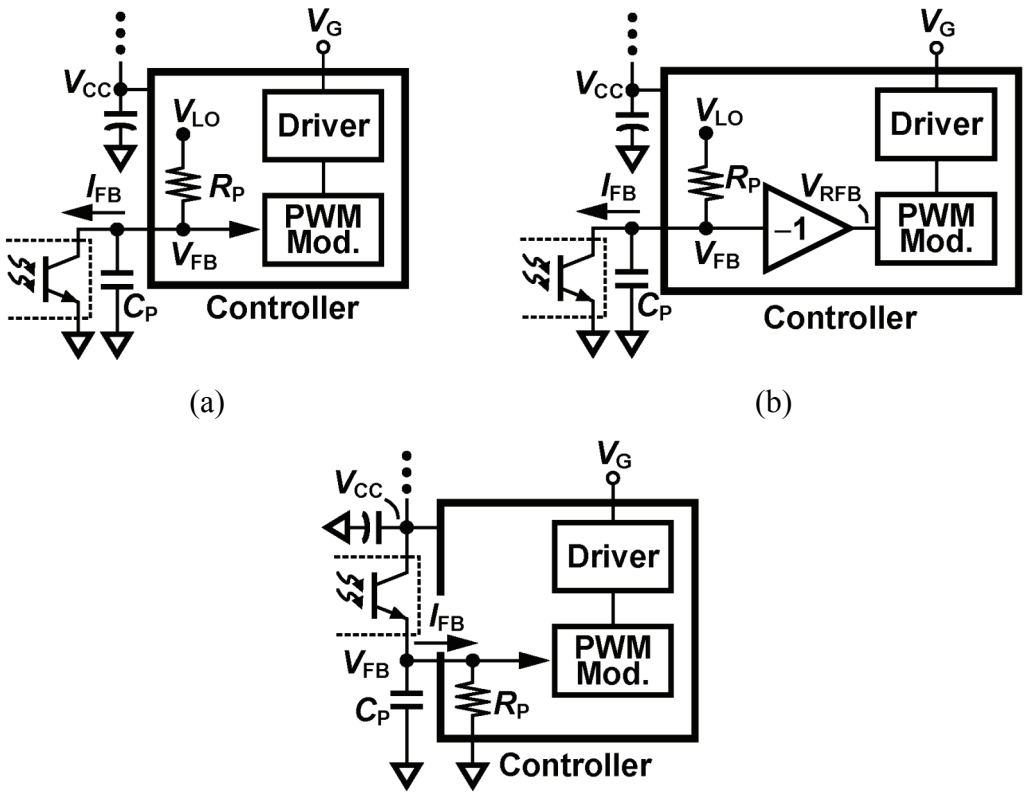


Fig. 3.4. (a) Conventional primary-side feedback circuit and (b)(c) two modifications for the phase-reversal technique.

close the loop with the circuit shown in Fig. 3.3(a) or (b) adopted as the secondary-side feedback circuit, what results will occur? When the output voltage drops and I_{LED} and I_{FB} are increased, V_{FB} is pulled down. Then, the modulator narrower the duty cycle of output pulses, making even less power delivered and the output voltage continuously drop. Similarly, when the output voltage increases, the modulator outputs even wider pulses to raise the output voltage even more quickly. In other words, the system forms a positive feedback loop and in the end leads to a malfunction.

The problem lies in the feedback signal polarity. Because we have reversed the relationship between I_{LED} and V_{OUT}, the signal polarity of V_{FB} now is the same as that of

V_{OUT}. That is, V_{FB} will grow up with V_{OUT}, and vice versa. Therefore, using a typical PWM modulator to directly modulate this V_{FB} into switching pulses simply causes a positive feedback loop. A simple solution is to just put an inverting amplifier with a unit gain before the modulator, as shown in Fig. 3.4(b). It helps reverse again the phase of V_{FB} before it is used for the following modulation. The output voltage V_{RFB} of the inverting amplifier will thus vary in the opposite direction of the way that V_{FB} goes. By doing so, the negative feedback loop is maintained. Fig. 3.4(c) provides an alternative way where the optocoupler is connected between the supply voltage V_{CC} of the controller and V_{FB}. Instead of sinking current, the optocoupler in Fig. 3.4(c) sources the induced current equal to I_{LED} multiplied by *CTR* to R_P. As a result, the phase of V_{FB} is also reversed compared to that in Fig. 3.4(a), and this V_{FB} can be directly modulated. Then, which solution of Fig. 3.4(b) and (c) is better? The circuit in Fig. 3.4(c) is merely a rearrangement of the circuit in Fig. 3.4(a), and it seems there is no more additional effort should be paid for it. However, we can think that when the output voltage of a converter is still lower than the desired value, I_{LED} will be at its maximum value which is mainly determined by the present output voltage and R_{LED}. If I_{LED} is not properly limited, V_{FB} in Fig. 3.4(c) has a possibility of exceeding the internal supply voltage V_{LO} which is generated from V_{CC} for supplying low-voltage-rating devices. In view of this concern, circuits inside the controller that would be connected to V_{FB} should be

designed using high-voltage-rating devices, but the consequence is the largely increased area consumption. The circuit in Fig. 3.4(b) is free from this issue, although it requires an extra inverting amplifier and thus causes more power loss. Fortunately, unlike the operating currents of the optocoupler, this inverting amplifier which is just used to process an on-chip low-speed signal needs only few tens of microamperes. Hence, we choose it as the preferred solution.

3.3.3 Overall System

The proposed complete feedback scheme applied to an isolated switch-mode power supply is shown in Fig. 3.5, and two examples of a flyback and a forward converters are presented in Fig. 3.6. In these implementations, a secondary-side integrated circuit is substituted for the traditional shunt regulator. It pulls down I_{LED} according to the difference between V_{OF} and the built-in reference voltage. The higher V_{OUT} is, the smaller I_{LED} will be conducted. As its operation is reversed compared to the traditional shunt regulator which will draw a larger I_{LED} with a larger V_{OUT}, we call it the reverse-type shunt regulator (RTSR). Note that the supply current I_Q will not flow through M_P and is not contained in I_{LED}. On the primary side, the only difference in the controller is that an inverting amplifier is presented before the PWM modulator. Other off-chip components, including R_{LED}, C_P, R_C, and C_C, are added for implementing a frequency compensator, which will be described later.

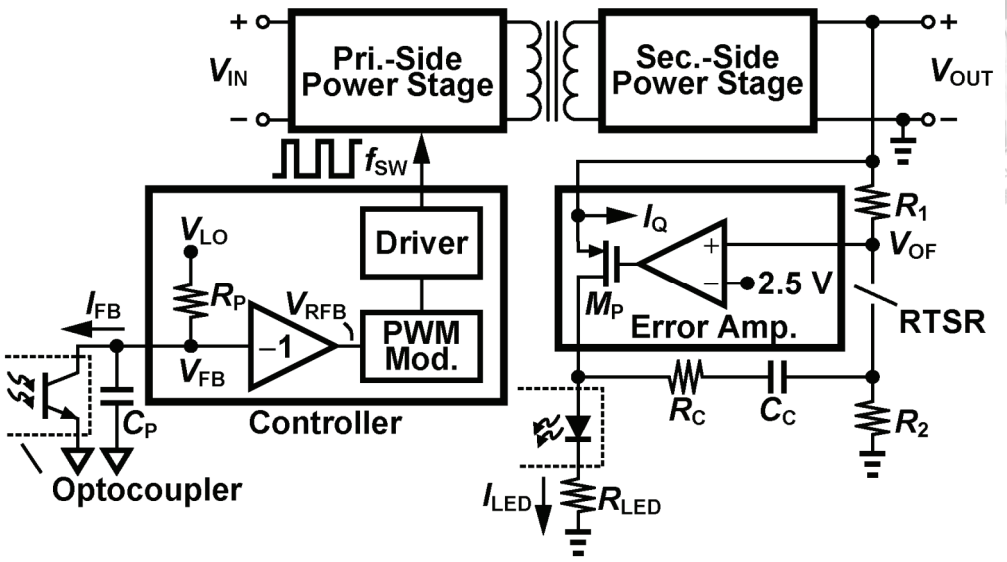
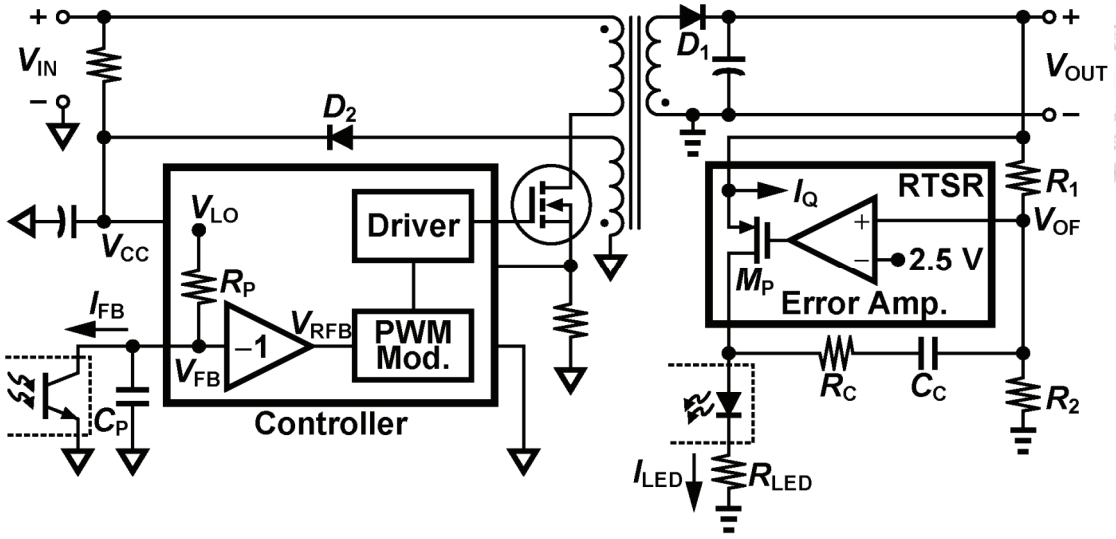
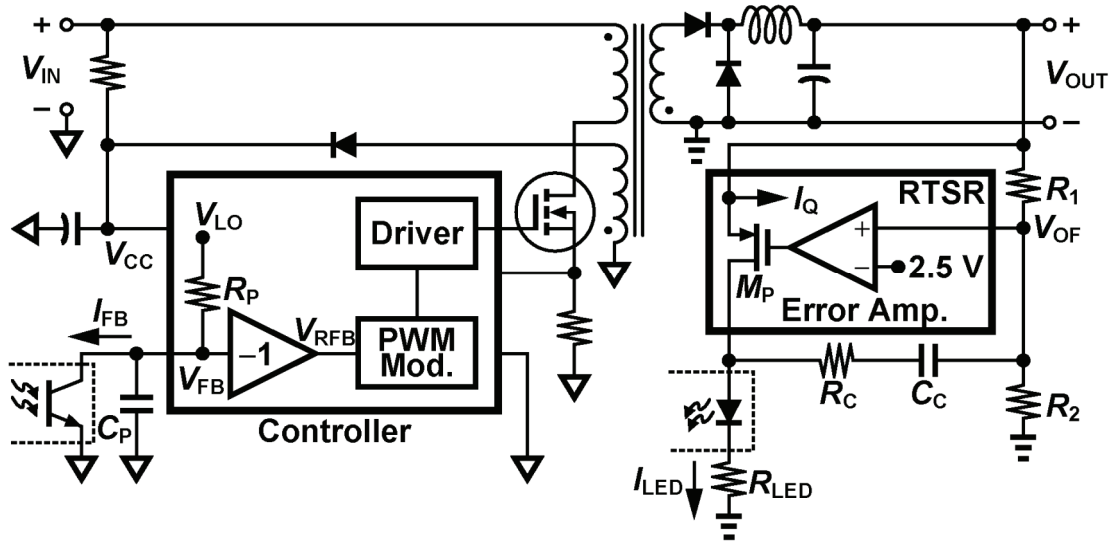


Fig. 3.5. The proposed complete low-standby-power feedback network.

The proposed feedback network basically performs the same function as the conventional one does, but the key point is that the phase of the intermediate error signal for optical coupling is reversed. With this proposed feedback scheme adopted, a higher V_{FB}, which gives a lower V_{RFB}, will correspond to a higher V_{OUT}, and therefore losses due to I_{LED} and I_{FB} will automatically reach minimum values under the no-load condition. Concerns may be aroused that whether or not the additional power losses caused by the inverting amplifier and I_Q surpass the saved power under the no-load condition. As previously mentioned, the current consumption of the inverting amplifier can be designed to be only a few tens of microamperes. Also, the supply current of the shunt regulator is not contained in I_{LED}, and thus the minimum values of I_{LED} and I_{FB} for operating are essentially not limited and can be designed to be very small. With these two features, the power loss of the feedback network under the no-load condition can be



(a)



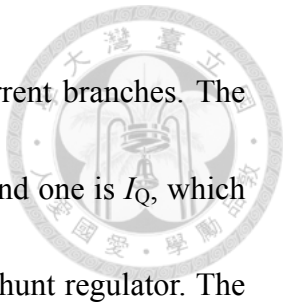
(b)

Fig. 3.6. Proposed feedback network adopted in (a) flyback and (b) forward topologies.

minimized. In the following sections, we will present the power loss analysis as well as the control loop compensation analysis.

3.4 Power Loss Analysis

As what we have done for the conventional feedback network in Section 2.2.4, we also want to formulate the power loss that is associated with the proposed feedback



circuit. First, we can recognize from Fig. 3.5 that there are five current branches. The first one is the current flowing through the voltage divider. The second one is I_{Q}, which is consumed by the error amplifier and the voltage reference in the shunt regulator. The third one is I_{LED}, which is conducted by M_{P} and the optocoupler. The fourth and fifth ones are respectively I_{FB} and the current dissipation of the inverting amplifier. Since there is only a slight power consumed by the inverting amplifier, we directly denote it as P_{IV} for convenience. Thus, if we first make an assumption of ideal energy conversion, the power loss ($P_{\mathrm{L,pro.}}$) of the entire feedback network can be estimated by

$$P_{L,pro.} = \frac{V_{OUT}^2}{R_1 + R_2} + I_Q V_{OUT} + I_{LED} V_{OUT} + I_{FB} V_{CC} + P_{IV} . \tag{3.1}$$

Now since I_{LED} can be expressed as I_{FB} divided by CTR, it follows that

$$P_{L,pro.} = \frac{V_{OUT}^2}{R_1 + R_2} + I_{FB}\left(V_{CC} + \frac{V_{OUT}}{CTR}\right) + I_Q V_{OUT} + P_{IV} . \tag{3.2}$$

Derive I_{FB} from V_{FB}, (3.2) becomes

$$P_{L,pro.} = \frac{V_{OUT}^2}{R_1 + R_2} + \left(\frac{V_{LO} - V_{FB}}{R_P}\right)\left(V_{CC} + \frac{V_{OUT}}{CTR}\right) + I_Q V_{OUT} + P_{IV} . \tag{3.3}$$

From observing (3.3), we see that the second term is the power loss caused by currents flowing through the optocoupler on the primary and the secondary sides. For a well-designed power converter, this part of loss will vary with V_{FB}, which is determined by the present load condition. Equation (3.3) is a simplified general estimation for any transformer-isolated converter adopting the proposed feedback network. If we solely

consider a flyback converter, as shown in Fig. 3.6(a), equation (3.3) can be further written as

$$P_{L,pro.} = \frac{V_{OUT} \cdot V'_{OUT}}{R_1 + R_2} + \left(\frac{V_{LO} - V_{FB}}{R_P} \right) \left(V'_{CC} + \frac{V'_{OUT}}{CTR} \right) + I_Q V'_{OUT} + P_{IV} \tag{3.4}$$

where

$$V'_{OUT} = V_{OUT} + V_{D1} \tag{3.5}$$

and

$$V'_{CC} = V_{CC} + V_{D2}\,. \tag{3.6}$$

V_{D1} and V_{D2} represent the forward voltages of diodes D_1 and D_2.

When operating under the no-load condition, converters generally adopt the burst mode control to regulate their outputs [39], [40]. As previously mentioned in Section 2.2.4, for a conventional PWM controller, it will start using the burst mode to control the system when V_{FB} is lower than a threshold voltage [57]. This mechanism is inappropriate for the proposed feedback topology in which, as shown in Fig. 3.1, V_{FB} increases with the decrease of the output power. Under this circumstance, the burst mode threshold voltage V_{BU} should be set close to V_{LO}, and the burst mode control should be activated when V_{FB} is larger than V_{BU}. Fig. 3.7 illustrates simulated waveforms of V_{FB} and the gate-driving signal V_G in the burst mode under the no-load condition. In this case, V_{BU} is set 4.5 V while V_{LO} is 5 V. The driving signal V_G is disabled if V_{FB} is higher than V_{BU}. Since V_{BU} can be set very close to V_{LO} (recall that the

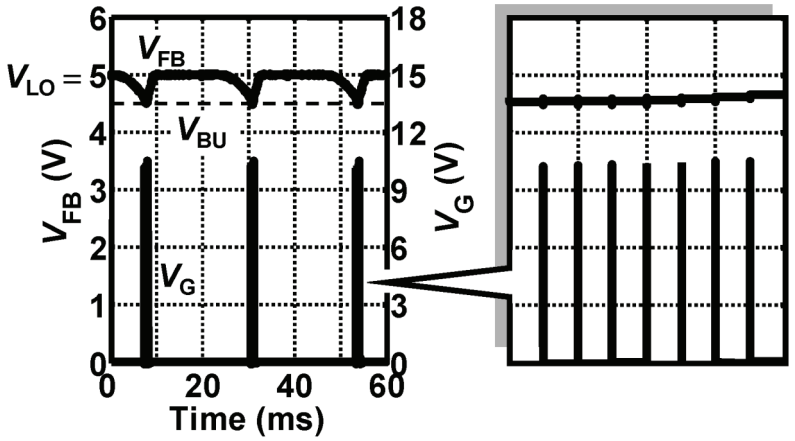


Fig. 3.7. Simulated burst-mode waveforms with proposed feedback topology adopted.

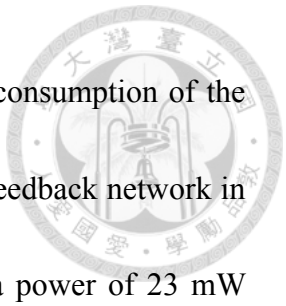
minimum values of I_{LED} and I_{FB} are not limited in the proposed feedback scheme) and therefore the loop response is very slow under the no-load condition, V_{FB} can be designed deliberately to touch and stay at V_{LO} in the period between the bursts. In this way, the optocoupler actually conducts zero currents on both sides in that duration. Because the only current dissipation at the output node comes from the resistor divider, the switching-ceased period is relatively long. Thus, under the no-load condition, (3.3) and (3.4) can be respectively approximated as

$$P_{L,pro.} \approx \frac{V_{OUT}^2}{R_1 + R_2} + I_Q V_{OUT} + P_{IV} \tag{3.7}$$

and

$$P_{L,pro.} \approx \frac{V_{OUT} \cdot V'_{OUT}}{R_1 + R_2} + I_Q V'_{OUT} + P_{IV}\,. \tag{3.8}$$

In our design which is going to be described in Chapter 4, I_Q is about 250 μA and the current of the inverting amplifier is 25 μA. The second and the third terms in (3.8) together add up to merely 3.4 mW under the condition that V_{OUT} = 12 V, V_{CC} = 10 V,



and $V_{D1\text{-}D2}$ = 0.5 V, making $P_{L,pro.}$ mainly dominated by the power consumption of the resistor divider only. Recall that, in Section 2.2.4, the conventional feedback network in a typical flyback converter having the same conditions consumes a power of 23 mW excluding the part of the resistor divider. Comparing the power losses of the conventional and the proposed feedback circuits, we can find that a power of 19.6 mW can be saved by simply applying the proposed feedback scheme. It should be noted that here we do not consider switching losses for simplicity. The estimated saved power is thus underestimated, which will be discussed more in Chapter 4.

3.5 Control Loop Analysis

The compensation design in the control loop must be considered for achieving a stable converter system. The proposed feedback network is provided with a compensator which is very similar to that in the conventional one. Fig. 3.8 shows the small-signal equivalent circuit of the proposed feedback network from V_{OUT} to V_{RFB} (the output voltage of the inverting amplifier). The reverse-type shunt regulator is regarded as a voltage-controlled current source with a transconductance G_{mrv}, while the optocoupler is treated as a current-controlled current source with a current gain of *CTR*. Again, the internal pole of the optocoupler is considered by including C_{OPT}, and the dynamic resistance of the light emitting diode is omitted from the following analysis as it is much smaller than R_{LED}.

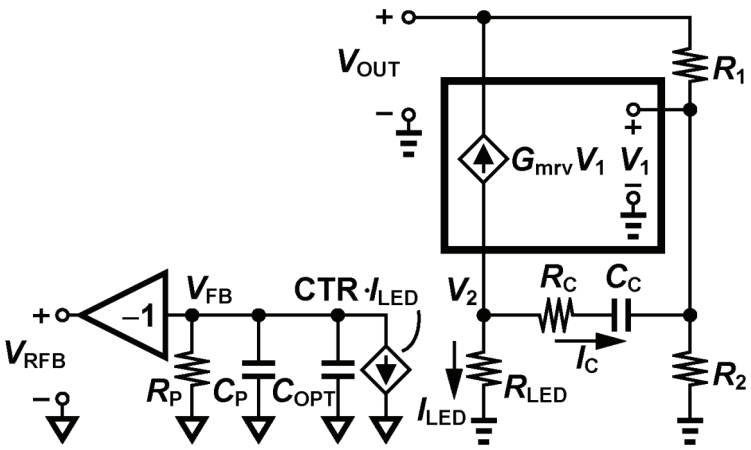


Fig. 3.8. Equivalent circuit for small-signal analysis.

Observing Fig. 3.8, we recognize that

$$V_2 = I_{LED} \times R_{LED} \tag{3.9}$$

where

$$I_{LED} = -\left(G_{mrv} V_1 + I_C\right). \tag{3.10}$$

Thus, I_C can be written as:

$$I_C = \frac{V_2 - V_1}{R_C + \frac{1}{sC_C}} = \frac{-R_{LED}\left(G_{mrv} V_1 + I_C\right) - V_1}{R_C + \frac{1}{sC_C}}. \tag{3.11}$$

On the other hand, I_C is equal to the difference of currents though R_1 and R_2. That is,

$$I_C = \frac{V_1}{R_2} - \frac{V_{OUT} - V_1}{R_1}. \tag{3.12}$$

Equating (3.11) with (3.12), we can obtain V_1 as a function of V_{OUT}:

$$V_1 = \frac{\frac{R_{LED}}{R_1} + \frac{1}{R_1}\left(R_C + \frac{1}{sC_C}\right)}{G_{mrv} R_{LED} + \left(\frac{1}{R_1} + \frac{1}{R_2}\right) R_{LED} + 1 + \left(\frac{1}{R_1} + \frac{1}{R_2}\right)\left(R_C + \frac{1}{sC_C}\right)} V_{OUT}. \tag{3.13}$$

Since we have (3.10), (3.12), (3.13), and

$$V_{RFB} = CTR \cdot I_{LED} \cdot \frac{R_P}{1 + sR_P\left(C_P + C_{OPT}\right)}, \tag{3.14}$$

we arrive at the final transfer function

$$\frac{V_{RFB}}{V_{OUT}} = G_0 \frac{1 + s\omega_z^{-1}}{\left(1 + s\omega_{p1}^{-1}\right)\left(1 + s\omega_{p2}^{-1}\right)} \tag{3.15}$$

where

$$G_0 = -\frac{R_P R_2 G_{mrv}}{R_1 + R_2} \cdot CTR\,, \tag{3.16}$$

$$\begin{aligned} \omega_z &= \frac{1}{\left(R_C - G_{mrv}^{-1}\right)C_C} \\ &\approx \frac{1}{R_C C_C}, \end{aligned} \tag{3.17}$$

$$\begin{aligned} \omega_{p1} &= \frac{1}{\left[\left(R_1 \parallel R_2\right)\left(R_{LED} G_{mrv} + 1\right) + R_{LED} + R_C\right]C_C} \\ &\approx \frac{1}{\left(R_1 \parallel R_2\right) R_{LED} G_{mrv} C_C}, \end{aligned} \tag{3.18}$$

and

$$\omega_{p2} = \frac{1}{R_P\left(C_P + C_{OPT}\right)}. \tag{3.19}$$

These results show that the proposed network still exhibits a two-pole one-zero characteristic, which can be easily utilized for the type-2 compensation. Moreover, the magnitude of G_0 and positions of the two poles are basically the same (i.e., determined by the same parameters) as their counterparts in the conventional feedback network. The only difference is that the zero in the conventional topology is at about $1/R_1C_C$, whereas in the proposed topology, we need to additionally place R_C in series with C_C to intentionally create a negative zero given by (3.17).

In the previous chapter, we have talked about the maximum value limitation on

R_{LED} and the minimum midband gain issue of the conventional feedback network. Its effect is, when we design the overall loop gain and try to stabilize a converter, the freedom to boost or attenuate the power-stage gain curve at the selected crossover frequency is limited. However, in the proposed feedback network, the midband gain can be derived as

$$G_{MID} = \frac{R_P R_C \cdot CTR}{R_1 R_{LED}}. \tag{3.20}$$

Unlike the midband gain in the conventional network, (3.20) tells that R_C provides us with another free variable to reach the appropriate midband gain. The ratio of the first pole to the zero will thus never be limited by R_{LED}. Although the maximum value limitation imposed on R_{LED} still exists in the proposed topology, the design flexibility of frequency compensation has already been promoted.

3.6 Comparison

In Section 2.3, we have introduced three different solutions trying to reduce the power loss of the conventional feedback network. The primary-side control solution leaves out the entire feedback network while suffering from poor output voltage regulation. The system output power (continuous-conduction mode is avoided) and the minimum output load (dummy load is needed) are both limited. These disadvantages are in fact originated from the removal of the explicit feedback path and are not going to bother designers in [55], [56], and this proposed work.

In comparison to the output voltage control method [55] and the feedback impedance modulation technique [56], this proposed method does not explicitly change the system feedback behaviors such as the feedback impedance or the controlled target. No matter how the load changes, from a light to a heavy load or vice versa, the feedback loop will constantly exist and automatically react to the present load condition without any purposely interrupting by the controller. As long as the loop gain is properly designed, there is basically no risk of instability under which the converter system leaps back and forth between the heavy-load and the light-load modes. As for the performance on saving the power under very light/no-load conditions, the proposed scheme clears out both the primary and the secondary-side currents of the optocoupler by separating the supply current of the reverse-type shunt regulator from flowing through the optocoupler. The loss caused by the supply current is thus not replicated. Accordingly, this proposed feedback network consumes even less power than those two previous techniques do. However, a main shortcoming is that the proposed reverse-type shunt regulator requires a 4-pin encapsulation rather than only 3 pins as the conventional shunt regulator does, leading to a slightly increase in cost.

3.7 Conclusion

The phase reversal concept is proposed to address the power loss issue of the feedback network. With this idea, the currents (I_{LED} and I_{FB}) flowing though the

optocoupler and thus the generated power loss are decreased with the output power. Following that, a complete feedback network is designed in accordance with the proposed concept. On the secondary side, on account of the feasibility of building the Miller compensation, we use a reverse-type shunt regulator to source current to the optocoupler. The current controlling device inside the regulator is realized with a pMOS rather than an nMOS to avoid the body effect. Also, the supply current of the reverse-type shunt regulator is not going to flow through the optocoupler, which makes this part of power dissipation not reproduced on the primary side. On the primary side, an additional inverting amplifier is adopted right before the PWM modulator to reverse the feedback signal again for achieving a negative feedback loop. The power loss analysis of the proposed feedback network shows an evident improvement over the traditional circuit when the converter operates in the burst mode. Also, the control loop of the proposed network is analyzed to check its validity, which shows that the midband gain will never be limited by R_{LED}. In comparison with prior techniques, the proposed feedback network not only really minimizes its power loss under very light/no load conditions but also possesses no potential instability issue when the output load suddenly changes from a light to a heavy load.

Chapter 4

Experiments

4.1 Introduction

In this chapter, material regarding experiments is presented. To verify the effectiveness of the proposed feedback network, we intend to apply the feedback network to a flyback converter and carry out a set of experiments. Therefore, the first part in this chapter presents the designs of a PWM controller and a reverse-type shunt regulator which is used for implementing the proposed system. Following that, a conventional and a proposed testing systems are implemented for comparison. Experimental results together with discussions are described at last.

4.2 Integrated Circuit Design

The chip design is of much great importance for a reliable system and hence should be done with great caution. We present the design considerations for key building blocks in the two integrated circuits.

4.2.1 Reverse-Type Shunt Regulator

The whole circuit diagram of the reverse-type shunt regulator is illustrated in Fig. 4.1. It features 4-pin connections, including a supply pin VDD, a pin VOF for the positive input terminal of the error amplifier, a pin VDT for the drain terminal of M_P,

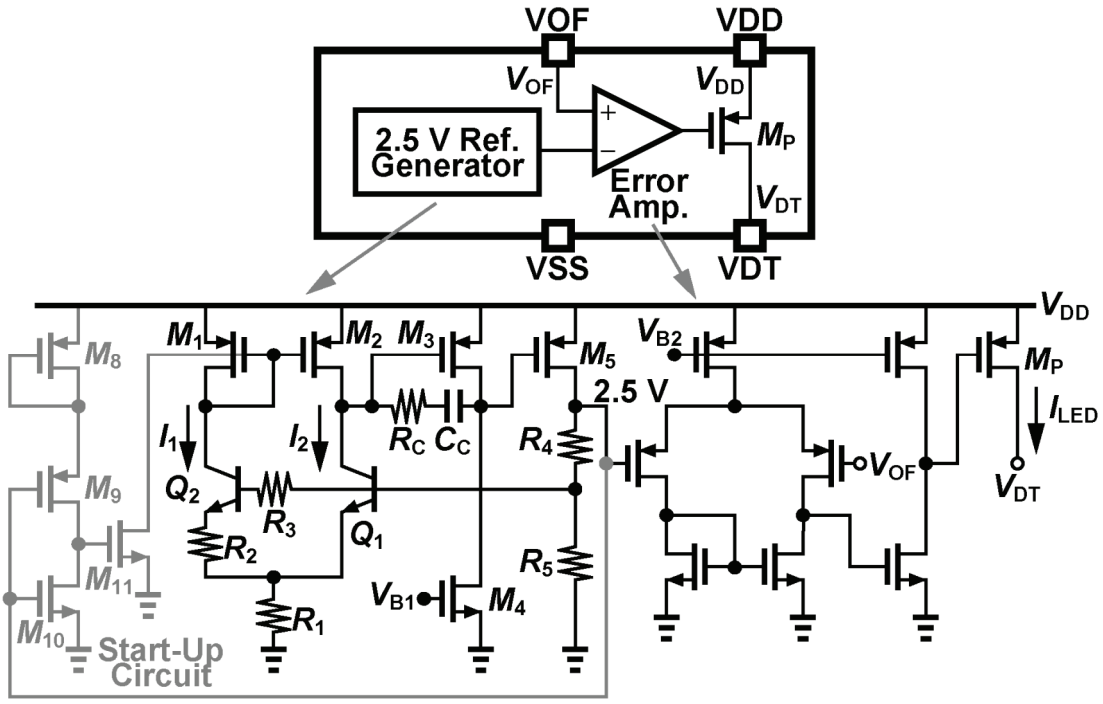


Fig. 4.1. The reverse-type shunt regulator.

and a ground pin VSS. In the system configuration, V_{DD} is supplied by the converter output, whereas V_{OF} is tied to the properly divided one. The reference generator shown in the left part of the figure employs the three-terminal bandgap reference technique [58], and it directly produces a temperature-compensated output voltage of 2.5 V with a simple circuit structure. The bandgap core circuit is composed of a pMOS current mirror which takes the difference between I_1 and I_2 to drive the next stage, a pair of npn transistors with Q_2 larger than Q_1 by a ratio of 8 to 1, and resistors R_1 and R_2. For narrowing the variation of the generated reference voltage, an additional common-source amplifier stage made of M_3 and M_4 is inserted between the bandgap core circuit and the output stage to increase the loop gain. Its bias current is mirrored directly from the current mirror $M_{1\text{-}2}$. R_4 and R_5 are tuned such that a voltage of 2.5 V is obtained,

while R_3 is set according to [58] for minimizing the base current effect. For stabilizing the loop, we utilize the added common-source amplifier to build the Miller compensation. The simulation (Fig. 4.2) shows that this reference generator presents a voltage variation of 0.34% with V_{DD} varying from 4.5 V to 12.5 V and temperature from –40 °C to 100 °C. The loop possesses a DC gain of 73 dB while maintaining an overall phase margin greater than 70°. It should be noted that the start-up circuit (the gray portion in Fig. 4.1) is appended to prevent the bandgap core from getting stuck in the zero-current state. As the reference voltage is high enough, the pull-down device (M_{11}) will be turned OFF and in the long run leave no effect on the performance of the reference generator.

For the consideration of large output swing, the error amplifier adopts the two-stage operational amplifier structure with its bias current mirrored from the reference generator. The output of the amplifier drives an open-drain configured pMOS M_P for controlling I_{LED}. The error amplifier must provide a sufficient speed while consuming a power as little as possible. For large-signal operations, we ensure that the slew rate is large enough to pull the gate voltage of M_P up to V_{DD} or down to ground within a switching cycle period. Since the maximum switching frequency in our system would be 60 kHz, the target slew rate is set 0.8 V/μs. For the small-signal behavior, the 3-dB corner frequency is kept beyond 10 kHz in order to have little impact on the

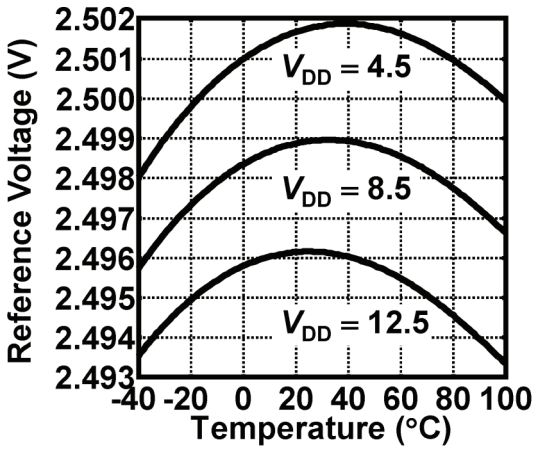


Fig. 4.2. Simulation result of the reference generator.

compensator design of converter system. The simulation shows that the corner frequency is at 15 kHz. The simulated equivalent transconductance G_{mrv} at low frequency is 4.86 Ω^{-1} under the condition that M_P conducts a I_{LED} of 1 mA.

4.2.2 PWM Controller

Owing to the fact that, as described previously, the phase of the feedback signal is reversed, existing PWM controllers on the market are not applicable to power converters using the proposed feedback network. Besides, to measure how much benefit will result from the proposed feedback scheme, we plan to design and compare two converters with different feedback topologies; however, their performances are highly dependent on the qualities of their controllers, making it very hard to purely evaluate the relative merits of feedback methods if an arbitrary commercial controller is used to build the conventional converter. For these two reasons, we design a PWM controller in which a proposed and a conventional feedback paths are both integrated. Adopting this

specially designed controller in converters with respectively the proposed and the conventional feedback schemes can promise a fair comparison between them because they are different only in the feedback circuits while all the other building blocks are the same.

Fig. 4.3 shows the block diagram. VCC is the power supply pin, from whose voltage V_{CC} an on-chip LDO regulates an output voltage V_{LO} of 5 V. Except the gate driver, the under-voltage-lockout (UVLO) circuit, and the LDO, all the other circuits are supplied by V_{LO}. The dual-mode feedback circuit includes a conventional and a proposed feedback paths and can be manually selected by applying an external voltage to V_{MS}. Once V_{MS} is given, the feedback circuit will receive the output voltage information from FBP or FBC pin and send an analogue signal V_{CT} to the PWM modulator and the oscillator. The switching frequency f_{SW} provided by the oscillator is normally set 60 kHz. Nonetheless, under light-load conditions, the oscillator which is controlled by V_{CT} will enter the power-saving mode and the frequency will be gradually decreased with a minimum value of 20 kHz. If even less current is demanded by the output load such that V_{CT} continuously drops below the burst-mode threshold voltage, the oscillator will stop switching. Fig. 4.4 shows the simulated switching frequency versus V_{CT}. The burst-mode threshold voltages for the proposed (V_{RBUP}, from the viewpoint of V_{CT}) and the conventional (V_{BUC}) networks are different and are also

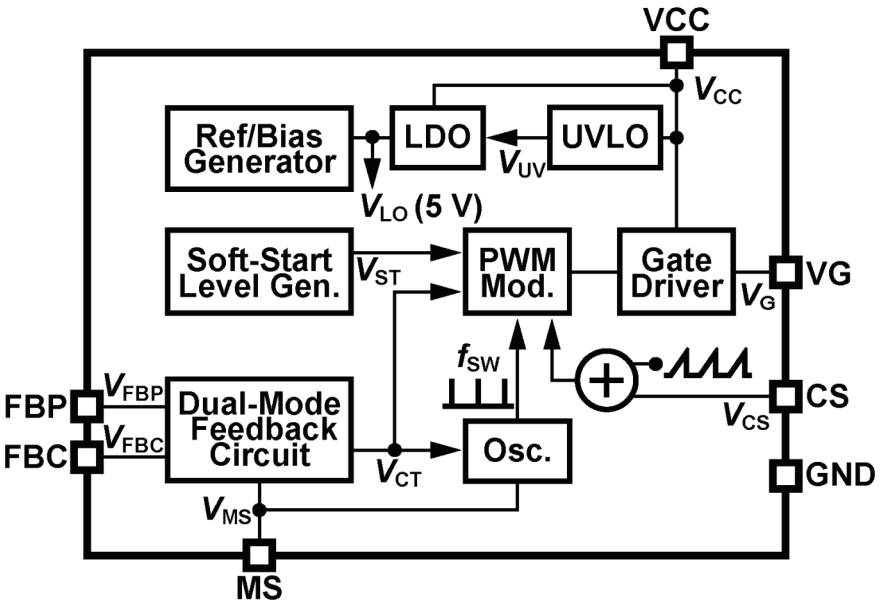


Fig. 4.3. Block diagram of the PWM controller.

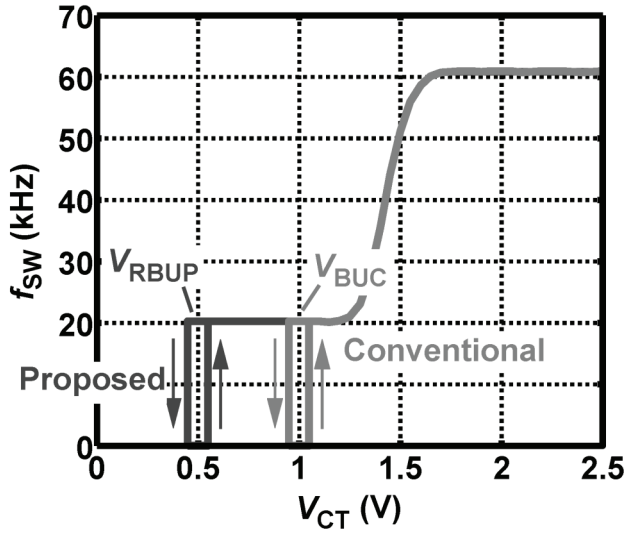


Fig. 4.4. Simulated switching frequency versus V_{CT}.

selected according to V_{MS}. The reason for the difference will be explained later. In order to ensure a successful start-up, a soft-start level generator that offers preset voltage levels for the PWM modulator is also included. The modulator simultaneously takes V_{ST} and V_{CT} as the current limit, but only the lower one of them involves in the pulse

generation process. Note that the sensed inductor current V_{CS} is slope-compensated for achieving a stable current-mode control when the converter operates in the continuous-conduction mode.

The detailed primary-side feedback circuit is illustrated in Fig. 4.5. There are two major blocks. The upper one is just the conventional feedback path, while the lower one is for the proposed feedback scheme. The actual path in use depends on the one-bit selection voltage V_{MS} which is externally applied. Thus, the PWM controller is capable of the dual-mode operation. Note that, although not clearly illustrated in the figure for simplicity, V_{MS} not only determines which path is to be used, but also is responsible for activating a mechanism to turn OFF all the circuits in the unselected path. That is, when one of the two paths is chosen for operation, the other one will be completely disabled and consume zero current. Consequently, adopting this controller in converters with different feedback schemes ensures a fair comparison. Now, let us look into the block of the proposed feedback path. The inverting amplifier is implemented by incorporating the Opamp together with R_{I1} and R_{I2}. The values of R_{I1} and R_{I2} are selected to be much larger than R_{P1} so as to reduce the loading effect imposed on V_{FBP}. In addition, the corner frequency of this inverting amplifier should be kept sufficiently large; otherwise it will affect the frequency compensation of system. In our design, we choose $R_{P1} = R_{P2}$ = 4 kΩ and $R_{I1} = R_{I2}$ = 300 kΩ, resulting in an amplifier gain of −1 V/V and a 3-dB

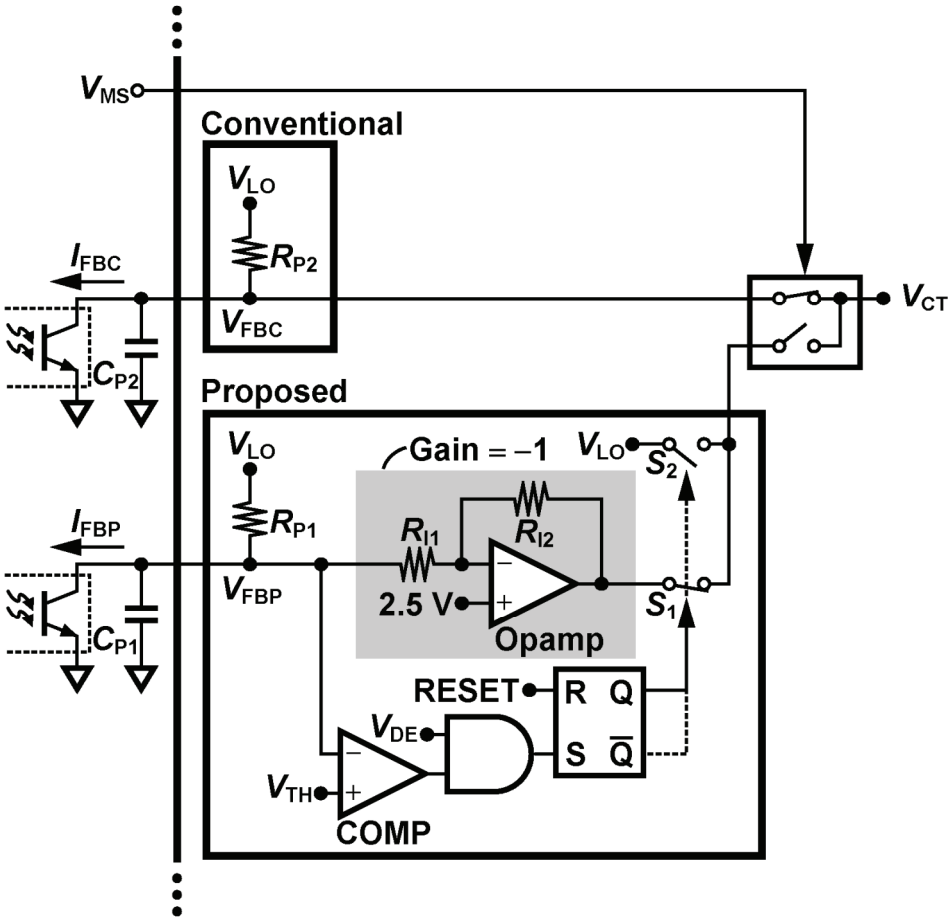
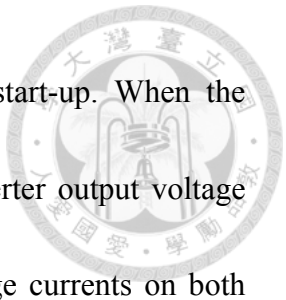


Fig. 4.5. Dual-mode feedback circuit.

bandwidth of 70 kHz. Note that the bias voltage of the Opamp's positive input terminal is 2.5 V; hence, the Opamp's output voltage and V_{FBP} are in fact symmetric about $V_{LO}/2$. In Section 3.4, we say that in the proposed scheme the burst-mode threshold voltage V_{BUP} from the viewpoint of V_{FBP} should be set close to V_{LO}. This can be done as well by setting the threshold voltage V_{RBUP} from the viewpoint of V_{CT} to be close to the ground because when the proposed feedback path is selected, V_{FBP} and V_{CT} have opposite phases. In the burst mode, the lower V_{RBUP} is, the higher V_{FBP} and thus the lower I_{FBP} would be. This is why we set V_{RBUP} lower than V_{BUC} as Fig. 4.4 shows.



Another issue that we have to cope with is related to the start-up. When the proposed feedback network is adopted, we expect that if the converter output voltage V_{OUT} is below the nominal value, the optocoupler would draw large currents on both sides and V_{FBP} in Fig. 4.5 would be pulled down. This prediction is true, however, only when V_{OUT} is at least larger than a certain value that enables the reverse-type shunt regulator to function normally and to draw sufficiently large current (I_{LED}). To inspect what really happens during start-up, we illustrate some key waveforms in Fig. 4.6. The start-up process will begin after the UVLO is triggered (V_{UV} is high). At the very beginning of this period, V_{FBP} will be directly pulled up to V_{LO} because of zero I_{LED} and I_{FBP}. This phenomenon will lead to a minimum ON-time of the power switch, which will cause a strong possibility of start-up failure. In order to fix this problem, the soft-start level generator along with some control logics can help get over it. Also shown in Fig. 4.5, two switches S_1 and S_2 controlled by a pair of complementary signals from an SR latch are applied to pass through the feedback signal or directly to short V_{CT} to V_{LO}. Before all the reference/bias voltages are settled down, the SR latch is reset. Therefore, V_{CT} is shorted to V_{LO} and the duty cycle of driving pulses is preliminary determined by the soft-start levels (V_{ST}) because in this time V_{CT} is larger than V_{ST}. Later, V_{FBP} will gradually slide down to zero with V_{OUT} climbing up. Once V_{FBP} drops below V_{TH} (1 V in our design), the comparator will change its output state. If V_{DE} is also

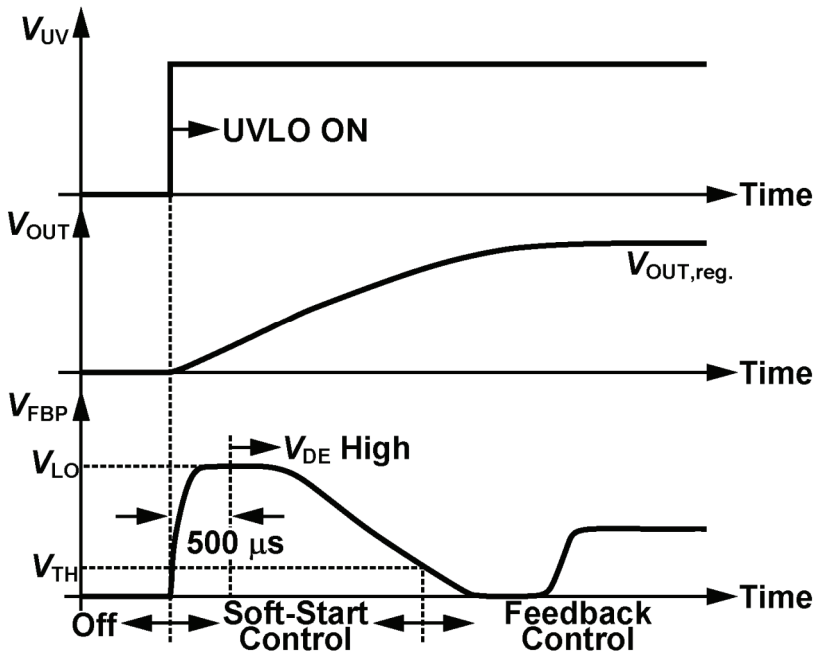
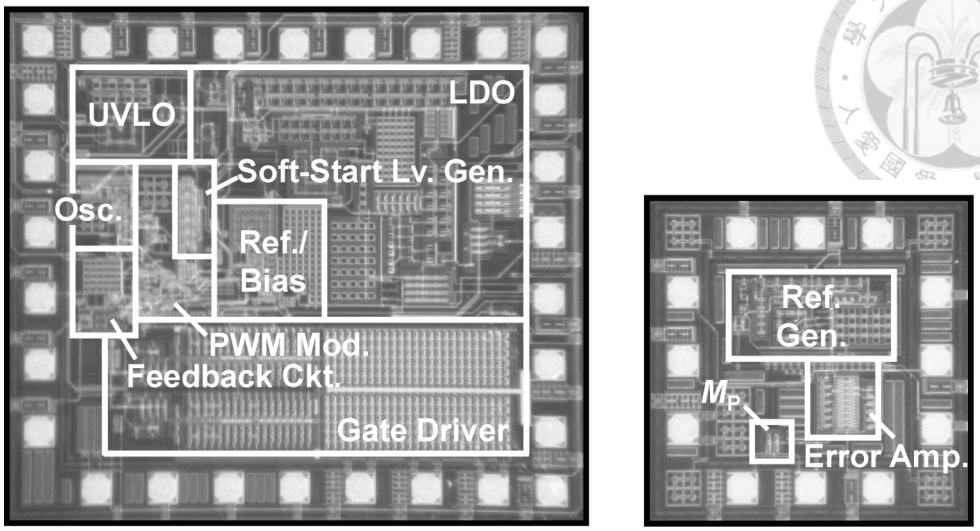


Fig. 4.6. Simulated waveforms during start-up.

logic HIGH in the meantime, the AND gate will set the SR latch such that S_1 and S_2 interchange their states. Afterwards, the feedback loop is established to take over the system control. The purpose of V_{DE} is to blank the time period at which V_{FBP} is charged to V_{LO}. Since this period is relatively short (e.g., it takes about 120 μs for V_{FBP} to achieve 90% of V_{LO} with C_{P1} = 10 nF) compared to the overall start-up duration, we allocate a blanking time interval of 500 μs, therefore. Simulations give that when this controller drives a 1-nF capacitor, the average current consumption is 1.8 mA with V_{FBP} = 2.5 V and becomes 0.3 mA with V_{FBP} = 5 V. The reduction in power is principally resulted from both the zero I_{FBP} and the ceasing of gate driving.

4.2.3 Chip Fabrication

The proposed reverse-type shunt regulator and the PWM controller have been



(a) (b)

Fig. 4.7. Die micrographs of (a) the PWM controller and
(b) the reverse-type shunt regulator.

designed and fabricated in VIS 0.5-μm 5-V/40-V high-voltage CMOS technology. Fig. 4.7 shows the die micrographs, where the PWM controller occupies 4.67 mm^2 and the reverse-type shunt regulator 1.22 mm^2 including pads. Single-chip measurements confirm that $R_{P1} = R_{P2} = 4$ kΩ and V_{LO} is 5 V. The burst-mode threshold voltages V_{BUP} and V_{BUC} are measured to be 4.5 V and 1 V, respectively. The measured supply current I_Q of the reverse-type shunt regulator is around 250 μA.

4.3 System Design

After the PWM controller and the reverse-type shunt regulator are ready, converters for experiments can be designed. The system specification we choose is a 12-V/18-W single-output flyback converter with universal inputs, and the crossover frequency is at 2 kHz with a phase margin of 90°. Fig. 4.8 shows the well-designed

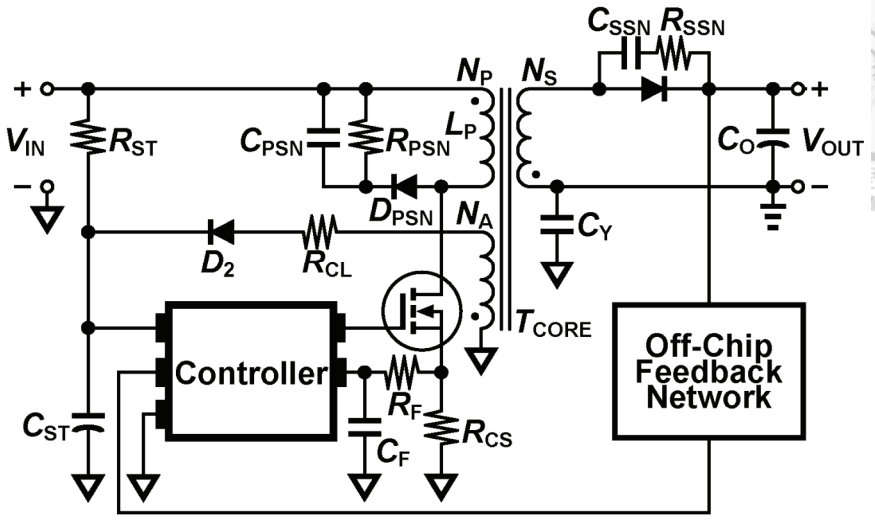


Fig. 4.8. Power stage of the flyback converter for experiments.

TABLE 4.1
Component Values and Part Numbers in the Power Stage

Parameter	Value	Parameter	Value
V_{IN}	120-380 VDC	R_{CL}	7.7 Ω
V_{OUT}	12 V/18 W	C_F	100 pF
V_{CC}	10 V (Under no load)	R_F	100 Ω
		R_{CS}	1.2 Ω
R_{ST}	1.5 MΩ	D_1	MBRF10200CT
C_{ST}	10 μF	C_{SSN}	1 nF
C_{PSN}	2.2 nF	R_{SSN}	11 Ω
R_{PSN}	100 kΩ	C_O	1000 μF
D_{PSN}, D_2	1N4007	L_P	1.4 mH
Power MOS	HFS4N60	T_{CORE}	PC40/RM5
C_Y	3.3 nF	N_P:N_S:N_A	44:5:6

power stage with all component values and part numbers listed in Table 4.1. To design the feedback network, we should first use a simulator to obtain the transfer function of the power stage from V_{CT} to the output. The result is portrayed using the lighter line in

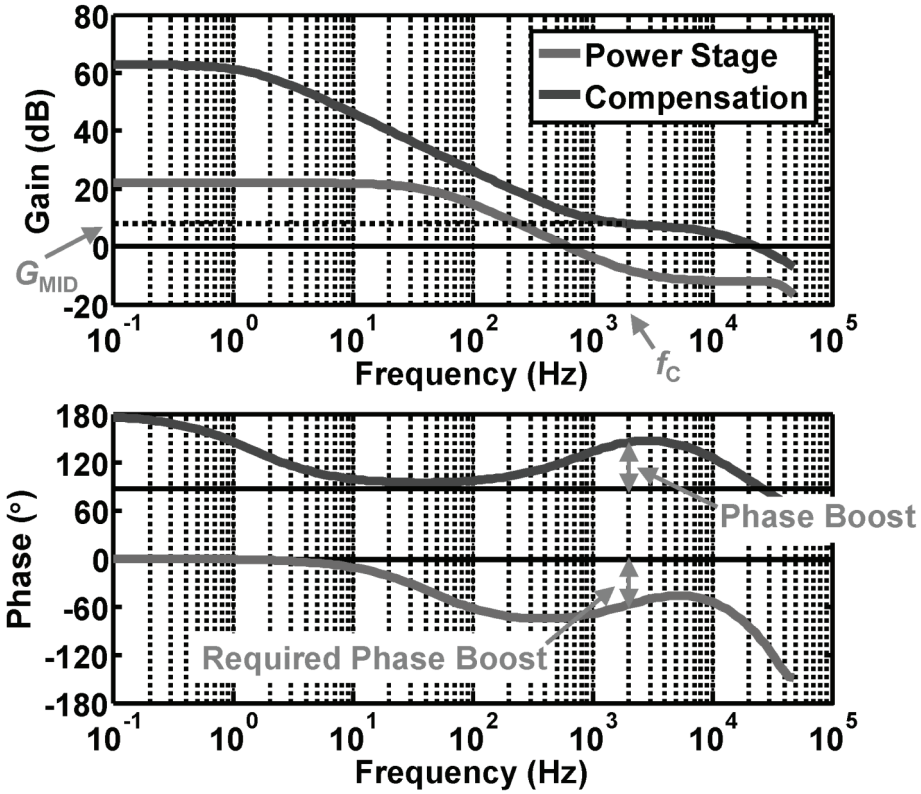


Fig. 4.9. Bode plot of the designed power stage and the proposed feedback network.

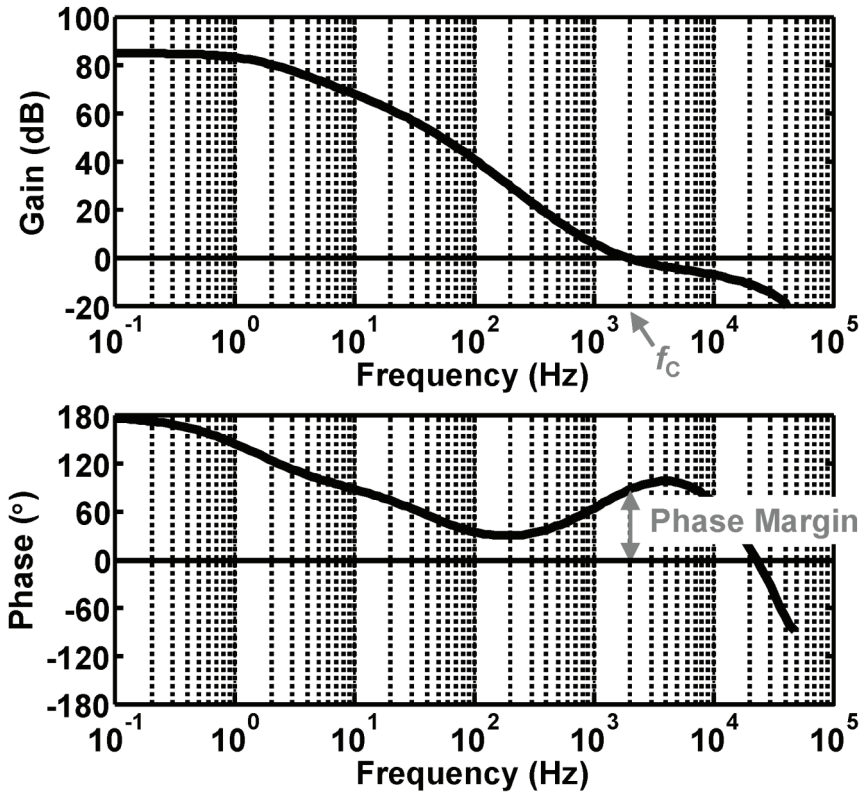


Fig. 4.10. The designed loop gain of the converter adopting the proposed feedback scheme.

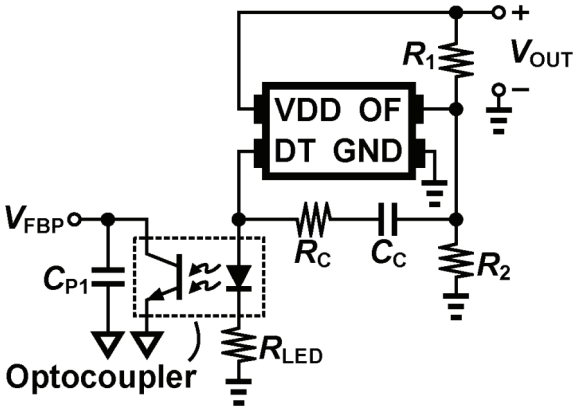


Fig. 4.11. The off-chip feedback circuit of the converter adopting the proposed feedback scheme.

TABLE 4.2
Component Values and Part Numbers in the Proposed Feedback Circuit

Parameter	Value	Parameter	Value
R_1	10 kΩ	C_C	2 nF
R_2	2.61 kΩ	R_{LED}	6.8 kΩ
R_C	75 kΩ	C_{P1}	2 nF
Optocoupler	PC817C		

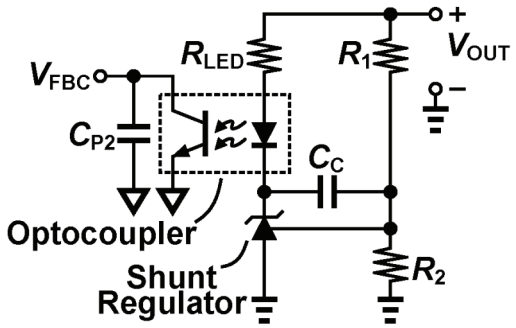


Fig. 4.12. The off-chip feedback circuit of the conventional converter.

Fig. 4.9 which shows that the feedback loop should provide an additional gain of about 7.8 dB and a phase boost of 57° at f_C. The designed frequency response of the proposed feedback loop is depicted using the darker line in Fig. 4.9. Fig. 4.10 gives the Bode plot

TABLE 4.3
Component Values and Part Numbers in the Conventional Feedback Circuit

Parameter	Value	Parameter	Value
R_1	10 kΩ	Optocoupler	PC817C
R_2	2.61 kΩ	Shunt Regulator	TL431
C_C	100 nF		
R_{LED}	680 Ω	C_{P2}	2.2 nF

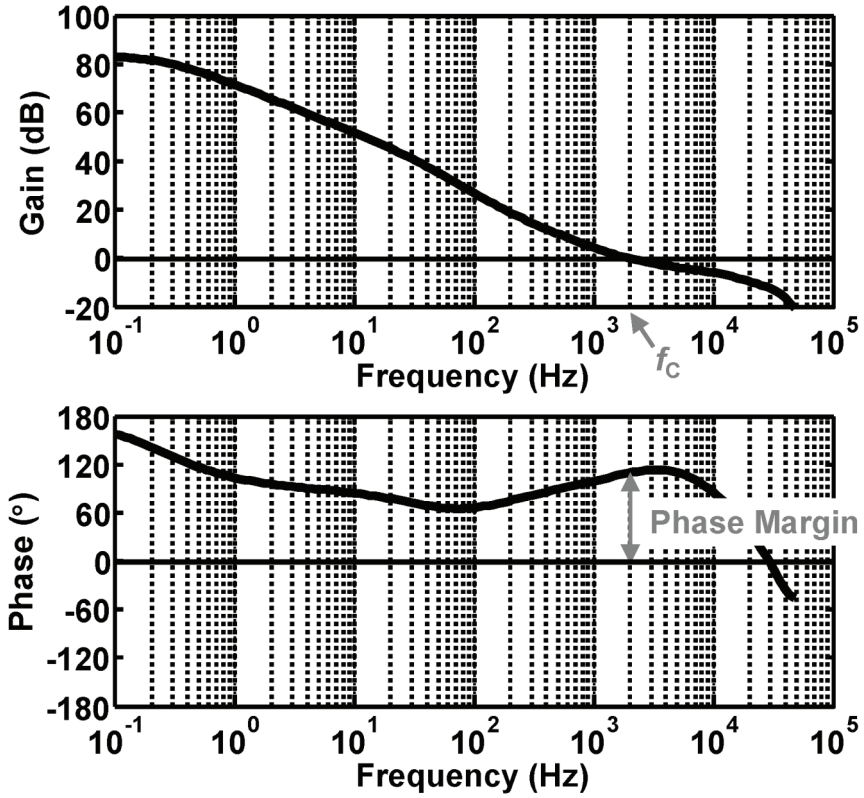
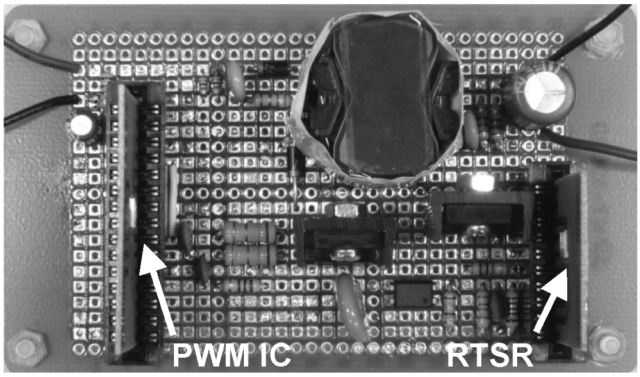
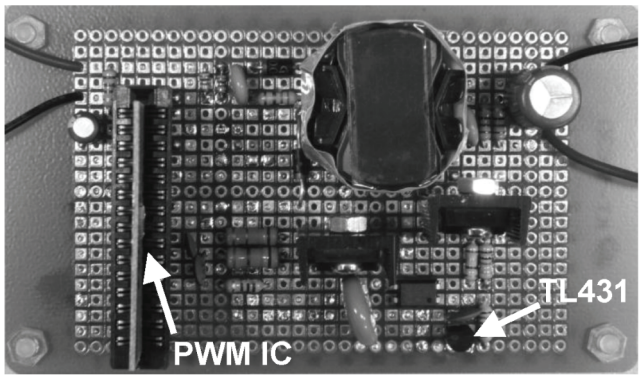


Fig. 4.13. The designed loop gain of the conventional converter.

of the overall loop gain, and it shows that the phase margin is nearly 90° at 2 kHz. Fig. 4.11 shows the overall proposed off-chip feedback circuit with all component values and part numbers listed in Table 4.2. Similarly, the conventional feedback network designed for the same power stage is illustrated in Fig. 4.12 with all component values and part numbers listed in Table 4.3. Fig. 4.13 shows the Bode plot of the resulted



(a)



(b)

Fig. 4.14. Testing boards of (a) converter adopting the proposed feedback topology and (b) converter with the conventional feedback topology.

overall loop gain. Note that the power stages of the two converters are exactly the same. In addition, output voltage dividers of the two converters are set identical, making them dissipate the same amount of power to ensure fairness. Fig. 4.14 shows the testing boards of the two converters. The bare dies of both the PWM controller and the reverse-type shunt regulator are first placed and wire-bonded to printed circuit boards, and then those boards can be plugged into sockets on the system boards.

4.4 Experimental Results and Discussions

The two demo boards shown in Fig. 4.14 are next taken for testing. We describe

the experimental results and make some discussions as follows.

4.4.1 No-Load Power Loss

First, we measure the performances of the two converters with no load applied. The testing setup for this experiment is shown in Fig. 4.15. A power analyzer is connected in series between a DC power supply and the device under test, and an oscilloscope is used to observe the waveforms. Fig. 4.16(a) shows the captured operating waveforms of the converter with the proposed feedback network under the no-load condition. Since the burst mode threshold voltage V_{BUP} is set 4.5 V and V_{FBP} remains at V_{LO} for about three quarters of one burst period, the power loss resulted from the second term in (3.3) or (3.4) can be estimated to be well below 1 mW, which proves the validity of the approximation equations (3.7) and (3.8). As for the conventional converter, its waveforms under the no-load condition are shown in Fig. 4.16(b). In this case, V_{FBC} almost sticks to the burst-mode threshold voltage V_{BUC} of 1 V, and the measured I_{FBC} is 1 mA. These truths rationalize the calculation of $P_{L,con.}$ in Section 2.2.4.

The power analyzer PM1000+, which is capable of low-standby-power measurements, is used to capture and average the output power of the DC supply in every 10 seconds. We record the no-load power losses of the two converter systems at different V_{IN}, and the results are shown together in Fig. 4.17. It can be seen that with V_{IN}

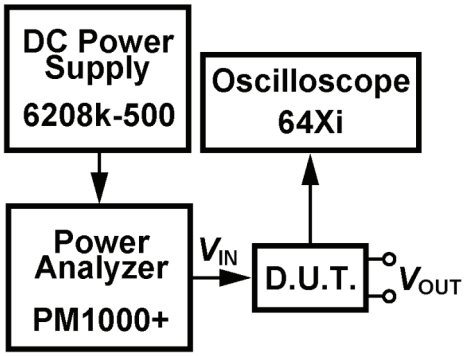
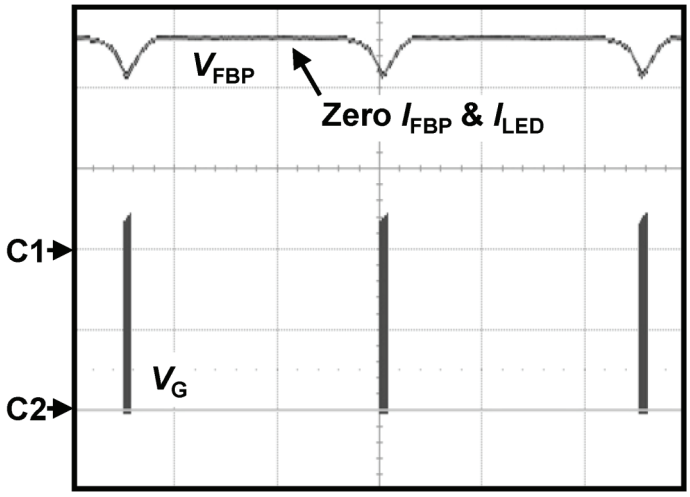
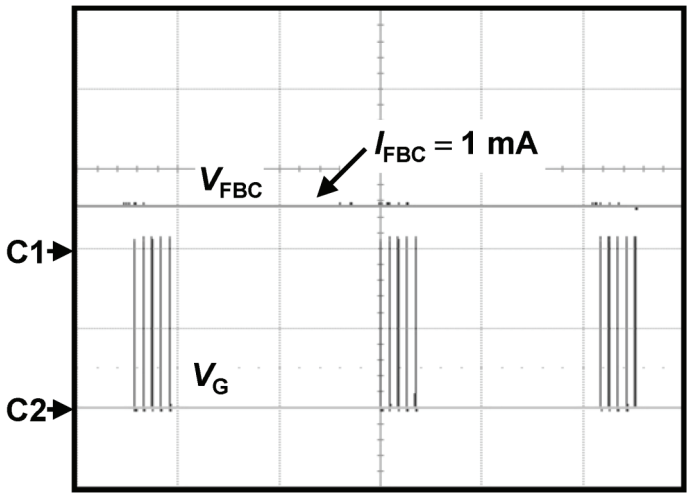


Fig. 4.15. Testing setup for measuring performance under no-load condition.



(a)



(b)

Fig. 4.16. Measured waveforms of converters adopting respectively (a) the proposed feedback topology and (b) the conventional feedback topology. (C1: V_{FB}, 2 V/div; C2: V_G, 5 V/div; horizontal scale: (a) 10 ms/div, (b) 0.5 ms/div.)

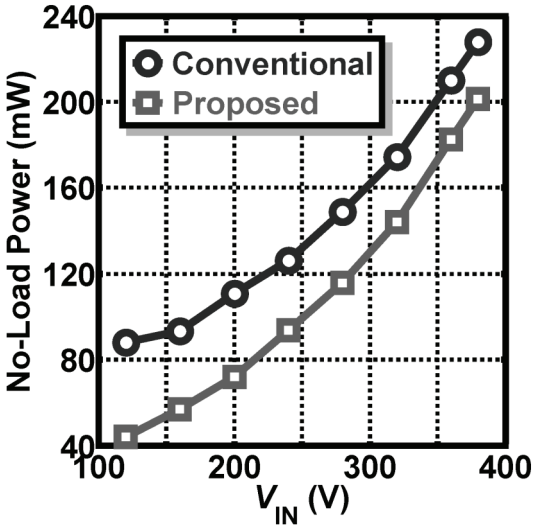


Fig. 4.17. Measured no-load power losses.

ranging from 120 V to 380 V, the system with the proposed feedback scheme saves at least 27 mW. It also shows that the measured power difference between the two converters is not constant and is larger than what we have expected in Section 3.4. Some factors contribute to these results:

1) The number of switching times of the converter with the proposed feedback topology is much less because of the very little current consumption at the output node. Therefore, its switching loss, which is also a very significant part under the no-load condition, is also reduced.

2) The number of switching times required to maintain the output voltage is deeply affected by V_{IN}, making the difference of the two curves in Fig. 4.17 is not constant. A higher V_{IN} enables more power delivery to the output in one pulse switching. Since originally there are relatively more switching times

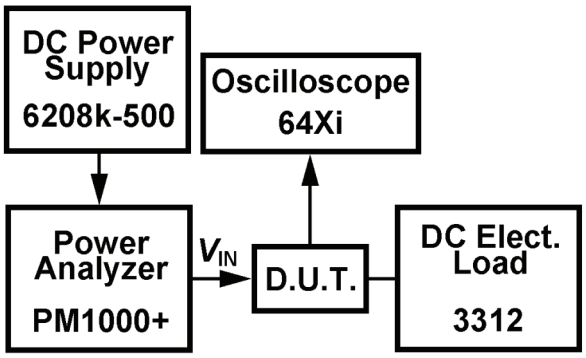


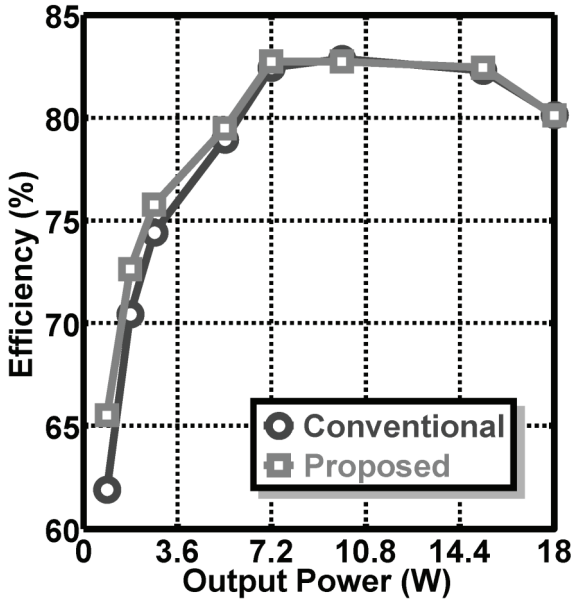
Fig. 4.18. Testing setup for measuring conversion efficiencies.

required in the conventional converter under this no-load condition, its reduced number of switching pulses which is brought about by raising V_{IN} will be also more than that of the proposed converter. This fact makes the difference of two curves decrease with the increase of V_{IN}.

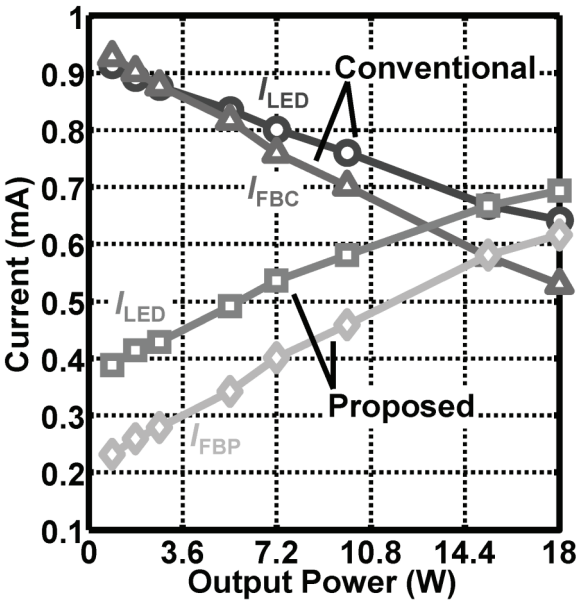
3) The variation in V_{CC} also affects the amount of saved power. In both of the two converters, V_{CC} decreases with the increase of V_{IN} owing to less switching times required to maintain V_{OUT}. However, the reduction of V_{CC} helps reduce more power in the conventional topology since its I_{FBC} is much larger than I_{FBP} in the proposed topology. This is another major reason that two curves in Fig. 4.17 get close to each other when V_{IN} goes higher.

4.4.2 Conversion Efficiency

To measure conversion efficiencies under different load conditions, we connect the output of device under test to a DC electronic load. The testing setup is shown in Fig. 4.18. We calculate the conversion efficiency by dividing the power displayed on the DC



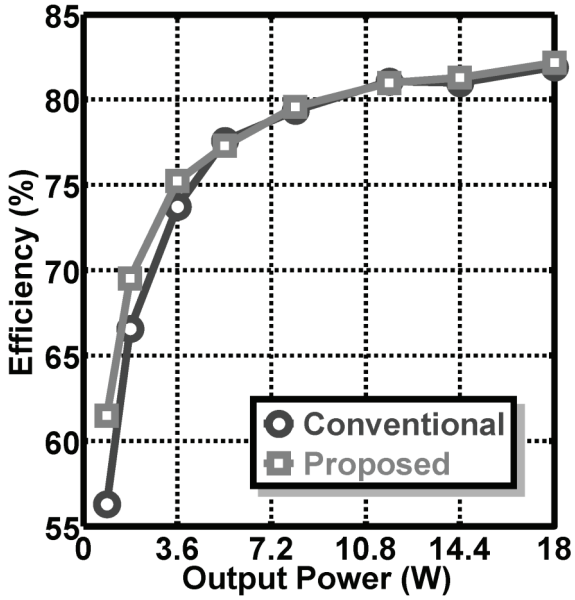
(a)



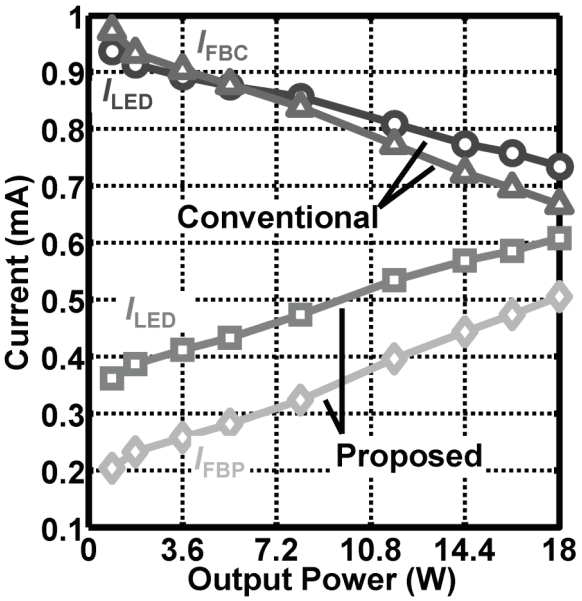
(b)

Fig. 4.19. Measured (a) conversion efficiencies and (b) currents flowing through the optocouplers when $V_{IN} = 110\sqrt{2}$ V.

electronic load by the power read from the power analyzer. Two groups of experiment with respectively $V_{IN} = 110\sqrt{2}$ V and $V_{IN} = 220\sqrt{2}$ V are conducted, and the results are portrayed in Fig. 4.19 and Fig. 4.20, respectively. In Fig. 4.19(a), we can observe that the conventional flyback converter performs nearly the same efficiency as the



(a)



(b)

Fig. 4.20. Measured (a) conversion efficiencies and (b) currents flowing through the optocouplers when $V_{IN} = 220\sqrt{2}$ V.

proposed counterpart does when the output power is larger than 7.2 W. But when the load gets lighter, the converter with the proposed feedback circuit presents evidently better efficiencies. For example, there is a 2.2% efficiency improvement under the 1.8-W output power (10% load) and a 3.6% improvement under the 0.9-W output (5%

load). Fig. 4.19(b) gives the measured currents of optocouplers in both of the converters. Under light-loads conditions, I_{LED} and I_{FBC} in the conventional converter are larger than I_{LED} and I_{FBP} in the proposed one, and their differences become even larger with the decrease of the output power. This fact forms the basic reason for the light-load efficiency improvement. Fig. 4.19(b) also indicates that the current transfer ratio *CTR* of the optocoupler continuously degrades with the decrease of the conducting currents. Therefore, the decrease of I_{LED} is not as much as that of I_{FBP} or I_{FBC}.

Fig. 4.20 shows a very similar situation when a higher input voltage (V_{IN} = $220\sqrt{2}$ V) is applied. The conversion efficiencies of the proposed flyback converter shown in Fig. 4.20(a) are much better than that of the conventional one when the load is lighter than 5.4 W. For instance, there is a 2.9% efficiency improvement under the 1.8-W output power and a 5.1% improvement under the 0.9-W output. Fig. 4.20(b) also depicts the measured currents of optocouplers in both of the converters. Comparing Fig. 4.20(b) with Fig. 4.19(b), we can see that in Fig. 4.20(b), the two conventional curves and the two proposed curves are separated even further. It is due to the higher input voltage such that the inductor current level limit becomes lower under the same output power condition. Therefore, V_{FBC} becomes lower and V_{FBP} becomes higher, leading to this phenomenon. This outcome also explains why the proposed converter improves more efficiency under the same light-load condition when a higher input voltage is

applied.

4.5 Conclusion

The PWM controller and the reverse-type shunt regulator are designed and fabricated for implementing a flyback converter adopting the proposed feedback scheme. By integrating both a proposed and a conventional feedback paths, the controller can be adopted for the conventional feedback topology as well. Two flyback converters with different feedback schemes are implemented using the fabricated chips for experiments. The comparisons between the two converters are made as fair as possible by setting their power stages and their resistor dividers identical, and even in their controllers, all other building blocks except for the feedback circuits are the same. In the measurements of the no-load power consumption, the converter adopting the proposed feedback network is obviously superior to the conventional converter, and the currents of the optocoupler in the proposed topology are proved to be almost zero under this condition. Better light-load conversion efficiencies are observed in the converter with the proposed feedback network, while at heavy loads, there is no significant distinction between the efficiencies of the two converters.

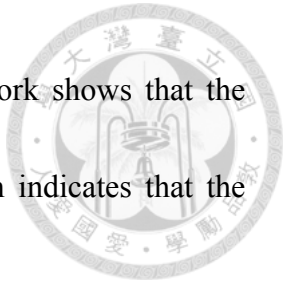
Chapter 5

Dissertation Conclusion and Future Work

5.1 Dissertation Conclusion

Standby power has resulted in a huge amount of energy waste in recent years, which makes both industry and academia gradually put concentration on this issue. The conventional feedback network is widely adopted in isolated offline switch-mode power supplies owing to the benefits of the simple circuit structure and low cost. However, the power loss under very light/no-load conditions causes severe standby power problem because the currents following through the optocoupler are increased with the decrease of the output power. Previous literature offers some techniques to address the power loss issue, while all of them bring about more or less disadvantages and are still not very ideal solutions at all.

This dissertation proposes the phase reversal concept to address the power loss issue of the feedback network. With this idea, the currents flowing through the optocoupler and thus the generated power loss are both decreased with the output power. Also, the supply current of the reverse-type shunt regulator is designed not to flow through the optocoupler, making this part of power dissipation not reproduced on the primary side. Following these thoughts, a complete isolated feedback network is

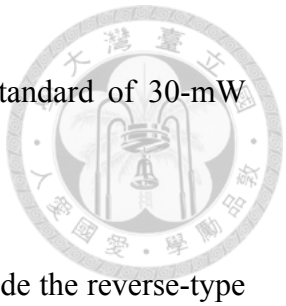


proposed. The power loss analysis of the proposed feedback network shows that the optocoupler conducts averagely zero currents on both sides, which indicates that the standby power of the feedback network is minimized.

The PWM controller and the reverse-type shunt regulator are designed and fabricated for implementing a flyback converter adopting the proposed feedback scheme. Two flyback converters with different feedback schemes are implemented using the fabricated chips. Experiments demonstrate a significant improvement in the no-load power loss over the conventional flyback converter. Better light-load efficiency is also achieved. Although the experiments are carried out on the basis of flyback converter, we do believe that it is also applicable to other transformer-isolated topologies. With the above advantages, the proposed isolated feedback scheme proves to be a promising solution for future low-standby-power converters.

5.2 Future Work

In this dissertation, we only examine the performance difference between two converters adopting respectively the proposed and the conventional feedback topology. It is encouraged to incorporate this proposed feedback method with other techniques, such as the high voltage start-up, the low-standby-power EMI capacitor discharging method, and a low-power controller, into a power supply unit to see how actually low-standby-power it can achieve. For example, a low-power battery charger adopting



all aforementioned techniques would probably meet the strictest standard of 30-mW standby power.

Another point that deserves improving is the error amplifier inside the reverse-type shunt regulator. Originally designed with the two-stage operational amplifier structure for simplicity and large output swing, it can be modified and implemented with an even lower-quiescent-current circuit, such as a class AB amplifier. The lower quiescent current is consumed, the lower standby power can be achieved.

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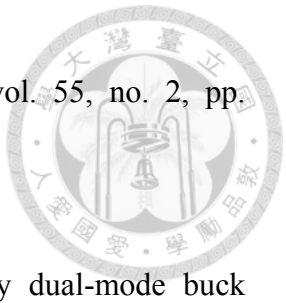

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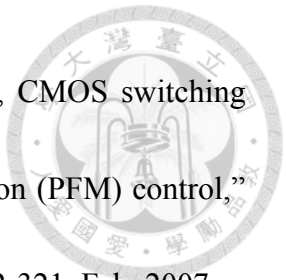

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