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以奈米壓印術製作應用於有機電子元件之奈米金屬網格
Fabrication of Nano Metal Meshes by Nanoimprint Lithography
for Organic Electronics Device Applications

方 向

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Applications

本論文係方向君（學號 R01941091）在國立臺灣大學光
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Thank you everyone.

皆さん、ありがとうございます。

方向

中文摘要



近年來，各種軟性電子元件的發展逐漸成熟，其中具有低成本、大面積量產能力等優點的液態製程有機電晶體其潛力更是突出。本論文研究主題是參與交通大學冉曉雯教授、孟心飛教授所組成的共同合作團隊之研究項目，針對空間電荷限制的有機垂直電晶體進行改進。過去這個團隊雖然可以製作出同時具有高輸出電流、高開關電流比與低操作偏壓等良好特性的有機垂直電晶體，但元件電性常常受限於製程方式，例如利用非緊密排列的奈米球作為金屬基極蒸鍍遮罩時，容易因為奈米球的隨機排列，造成球聚集而產生孔洞過大的問題。研究結果顯示，過大的電子傳輸通道將會產生較大的漏電流。

為解決這一個棘手問題，本實驗室以干涉曝光微影術結合奈米壓印術，成功製作出規則金屬網基極。

但是干涉曝光之解析度受限於光源波長，無法製作出小於一百奈米之網格圖案；而濕式蝕刻在製作規則金屬網的同時，則會對元件上造成有機材料的離子汙染，而產生漏電流。本研究首先引進原子層沉積製程，在縮小孔洞直徑的同時加強光阻結構之機械強度。而後為了將濕式蝕刻從製程中去除，改以奈米壓印搭配剝離法來製作奈米金屬網，因此有了突破性的成果，成功製作出大面積(大於四平方公分)、直徑小於一百奈米的金屬網格，並成功將電晶體基極漏電流縮小近一個數量級，同時具備高製程容忍度與高再現性，製作出元件具有開電流 4.64 mA/cm^2 及開關電流比到 10^5 以上的元件特性。

關鍵字：干涉微影、奈米壓印、原子層沉積、有機電晶體、空間電荷限制電晶體

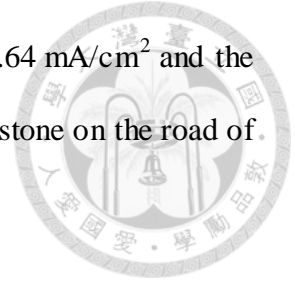
ABSTRACT



Owing to the rapid development of flexible electronic devices in recent years, the solution-processed organic transistors have shown their great potential in many applications by employing low-cost, roll-to-roll, and large-area mass production. This thesis mainly focuses on the performance improvement on space-charge-limited organic transistor (SCLT), jointly developed by Prof. Zan's, Prof. Meng's and our groups. Though SCLT usually has high output current, high ON/OFF current ratio and relatively low operational voltage, its performance is still unstable due to the defects in fabrication process. The nano sphere is used as an evaporation mask for base-electrode in the colloidal lithographic process. But accommodation effect may occur because of the random arrangement of spheres. It may produce larger hole on the electrode, causing larger leakage current of SCLT. To solve this problem, we fabricate the well-regular-ordered metal mesh base-electrode by combing interference lithography (IL) and nanoimprint.

Since the resolution of IL is limited by the wavelength of light source, sub-100 nm metal mesh cannot be realized. In addition, the ion contamination caused by wet-etching may induce large base leakage current. We therefore introduce the atomic layer deposition process to reduce the hole diameter of photoresist pattern down to smaller than 100 nm. And the mechanical strength of photoresist structure also has been reinforced to be hard enough as an imprint mold at the same time. Then we adopt the strip-off method to replace wet-etching method in mesh fabrication. We successfully combine nanoimprint with strip-off method to fabricate large area ($> 4 \text{ cm}^2$) and sub-100 nm resolution metal mesh. The base leakage current has been reduced by nearly an order of magnitude. And the process tolerance and reproducibility of SCLT remain

high at the same time. The output current of SCLT device reaches 4.64 mA/cm^2 and the ON/OFF current ratio increases to more than 10^5 , setting a new milestone on the road of SCLT development.



Keywords: interference lithography, nanoimprint, ALD, organic transistor, space-charge-limited transistor

Statement of Contributions



1. Combining two-beam interference lithography and ALD to fabricate sub-100 nm photoresist hole-array pattern as an imprint mold. The ON/OFF current ratio of SCLT reaches 10^4 . This work is cooperated with Prof. Zan's and Prof. Meng's group in NCTU.

The result had been oral presented in *MNC 2013*, and published on the journal *Organic Electronics* in 2014.

2. Cooperate with the group of Prof. Lee in NTU to fabricate nano metal grating as circular polarizer.

This result had been submitted to the journal *Optics Express* (published in 2014) and *Applied Optics*.

3. Developed strip-off method to replace the wet-etching method in SCLT fabrication.

The leakage current of SCLT has successfully reduced one order. The ON/OFF current ratio of SCLT reaches 10^5 . This work is cooperated with Prof. Zan's and Prof. Meng's group in NCTU.

This result had been poster presented in *SSDM 2014*, and will be submitted to the journal *Organic Electronics* in 2015.

CONTENTS



誌謝	i
中文摘要	iii
ABSTRACT	iv
Statement of Contributions.....	vi
CONTENTS	viii
LIST OF FIGURES	ix
LIST OF TABLES	xiii
Chapter 1 Motivation and Introduction.....	1
1-1 Motivation.....	1
1-2 Space-charge-limited transistors.....	3
1-3 Organization of the Thesis	8
Chapter 2 Fabrication of Imprinted SCLT.....	9
2-1 Nanoimprint Lithography	9
2-2 Two-beam interference lithography.....	12
2-2-1 IL concept.....	12
2-2-2 ARC thickness design.	16
2-2-3 Exposure dose of photoresist pattern	19
2-3 Fabrication processes of imprinted SCLT	23
Chapter 3 Sub-100 nm ALD-assisted Nanoimprint Lithography.....	28
3-1 ALD-assisted dimension shrinkage	28
3-2 Hot-embossing imprint process	36
3-2-1 Fabrication of h-PDMS imprint stamp.....	36

3-2-2	Mold release agent.....	39
3-3	Fabrication of Al nano meshes by wet-etching.....	41
3.4	Measurement results	44
Chapter 4	Fabrication of Nano Metal Meshes by Strip-off Method	48
4-1	Advantages of lift-off method.....	48
4-2	Dissolvable imprint resist	50
4-3	Patterning the microfiber by imprinting	53
4-4	Fabrication process of lift-off method	56
4-4-1	Problems of lift-off method.....	56
4-4-2	Tilted evaporation of SiO caps.....	61
4-4-3	Strip-off method.....	64
4-5	Measurement results	68
4-5-1	Leakage current at PVP-Al interface.....	68
4-5-2	Strip-off method without residue removal.....	72
Chapter 5	Applications of Nano Metal Structures Using Strip-off method..	78
5-1	Nano metal gratings for optical applications	78
5-2	Nano metal structures for electronic devices.....	83
5-3	Nano metal structures for sensing devices.....	86
Chapter 6	Conclusions and Future Works.....	87
6-1	Conclusions.....	87
6-2	Future works	89
References.....		92

LIST OF FIGURES



Fig. 1-1 Schematic diagram of a vacuum tube.....	5
Fig. 1-2 Schematic diagram of an SCLT.....	5
Fig. 1-3 Potential distribution from emitter to collector at the center of channel.....	6
Fig. 1-4 Nano mesh made by (a) colloidal lithography (random order) and (b) nanoimprint lithography (periodic order).....	7
Fig. 2-1 Schematic diagram of the NIL process [8].....	11
Fig. 2-2 SEM photos of (a)holes and (b)dots array pattern made by NIL, both of them are 25 nm in diameter [8].....	11
Fig. 2-3 Schematic of 2-beam IL [10].....	14
Fig. 2-4 Schematic of the 2-beam IL system in our lab [11].....	15
Fig. 2-5 Intensity distribution diagram along the perpendicular direction of substrate and PR surface.....	17
Fig. 2-6 Defects on the PR sidewall caused by standing wave effect.....	17
Fig. 2-7 Interference in a quarter-wave anti-reflection coating.....	18
Fig. 2-8 Illustration of two exposed photoresists with different tone after development process.....	20
Fig. 2-9 The binary photoresist model for exposure and development. The regions of exposure dose higher than threshold dose are exposed. There are more exposed regions whose doses are higher than threshold dose when D_{avg} increases. The increasing exposed areas represent smaller linewidth, for positive photoresist and bigger linewidth for negative photoresist.....	21
Fig. 2-10 Hole-array PR pattern generated by double-exposure.....	22

Fig. 2-11 PR patterns with different exposure dose. All patterns have the same period setting (245 nm).....	22
Fig. 2-12 Patterned ITO glass substrate of an SCLT.....	23
Fig. 2-13 Fabrication process of an imprinted SCLT.....	27
Fig. 3-1 Transfer characteristics of SCLT devices with different hole diameters.....	31
Fig. 3-2 Relation between grating period and hole diameter.....	31
Fig. 3-3 SEM images of the (a) ARC pattern and Al nanopore structure after Al wet etching. (b) and (c) Vertically oriented PVP cylindrical nanopores covered by the Al hard mask [15].....	32
Fig. 3-4 Fabrication process of the ALD-assisted dimension shrinkage method.....	32
Fig. 3-5 SEM images of (a) PR pattern before growing ALD Al_2O_3 . (hole diameter = 180 nm) And (b) PR pattern after growing ALD Al_2O_3 . (hole diameter = 85 nm).....	33
Fig. 3-6 (a) Cross-sectional SEM image of an ALD-covered mold. AFM images of (b) a new mold and (c) the same mold after more than 30 times for imprint use.....	34
Fig. 3-7 The ALD machine we used in this work, which is located at NCTU.....	35
Fig. 3-8 An <i>h</i> -PDMS / PDMS hybrid stamp is demolding from the imprint mold.....	38
Fig. 3-9 Chemical structure formula of FPTs.....	39
Fig. 3-10 AFM photos of <i>h</i> -PDMS stamp (a)without and (b)with FPTs applied.....	40
Fig. 3-11 AFM photo of Al meshes made by wet-etching.....	41
Fig. 3-12 (a)AFM photo of the incomplete-etched AL meshes. (b) Unwanted PVP column (red circle) during PVP etching.....	42
Fig. 3-13 (a) Emitter current, (b) output curve, (c) base current and (d) ON/OFF current ratio of an outstanding second generation SCLT.....	45
Fig. 3-14 (a) Emitter current, (b) output curve, (c) base current and (d) ON/OFF current ratio of a normal second generation SCLT.....	46

Fig. 4-1 Silver gratings fabricated by IL and lift-off method. (Period: 250 nm).....	48
Fig. 4-2 Imprint process parameters of (a) ARC and (b) mr-I 7020R. The redline represents the temperature and the blue line represents the pressure.....	51
Fig. 4-3 Fabrication process of an imprinted SCLT using lift-off method.....	53
Fig. 4-4 Aluminum meshes made by (a) wet-etching and (b) lift-off.....	54
Fig. 4-5 Cases of failed lift-off processes.....	57
Fig. 4-6 Lift-off results of different thickness metal meshes. (a) 20 nm Ag. (b) and (c) 25 nm Ag. (d) 40 nm Au.....	58
Fig. 4-7 The aluminum mesh with 20 nm thickness has been damaged by O ₂ plasma after PVP etching process (red arrow).....	59
Fig. 4-8 The undercut-shape sacrificial structure for lift-off method.....	61
Fig. 4-9 Fabrication process of tiled evaporation.....	62
Fig. 4-10 SEM photos of (a) top and (b) side view of the SiO caps (red circle) on top of sacrificial structures (mr-I 7020R).....	62
Fig. 4-11 Fabrication process of strip-off method.....	65
Fig. 4-12 (a) Bad collimation of evaporator and (b) bad collimation of sidewall of sacrificial structures.....	65
Fig. 4-13 (a) 2 x 2 cm ² Al mesh fabricated by strip-off. (b) Top view (d = 80 nm) and (c) side view of the Al mesh after PVP etching process.....	66
Fig. 4-14 (a) Output curve, (b) base current, and (c) cross-section photo of the third generation SCLT.....	68
Fig. 4-15 Base current of (a) pure PVP and (b) PVP coated with mr-I 7020R.....	70
Fig. 4-16 Fabrication process of the modified strip-off method using ARC as the imprint resist.....	72
Fig. 4-17 SEM photos of imprinted ARC rod-array pattern.....	73

Fig. 4-18 SEM photos of Al mesh (a) before and (b) after PVP etching.....	74
Fig. 4-19 Electrical measurement results of the third generation SCLT: (a) output curve (b) base current (c) emitter current and (d) ON/OFF current ratio.....	75
Fig. 4-20 Cross-section SEM photo of an SCLT with OTS-18 treatment.....	76
Fig. 4-21 Electrical measurement results of the third generation SCLT with OTS-18 treatment: (a) output curve (b) base current (c) emitter current (d) ON/OFF current ratio.....	76
Fig. 5-1 The simulated 0th order transmission spectra for TE and TM waves with various slit width (grating period = 300 nm).....	79
Fig. 5-2 The grating pattern has been fine-tuned by ALD.....	79
Fig. 5-3 SEM photo of designated aluminum grating on glass substrate.....	80
Fig. 5-4 Fabrication process of silicon fiber grating using MacEtch.....	81
Fig. 5-5 Base current of SCLT which made by (a) wet-etching and (b) strip-off method. (c) ON/OFF current ratio of 1st (black) and 3rd (red) generation SCLT.....	83
Fig. 5-6 SEM images of the silver nanopillar array (tilted view: 45°).....	85
Fig. 6-1 Schematic diagram of a mass production system with R2P imprinter and roller strip-off instrument.....	89
Fig. 6-2 Flexible SCLT device using PEN substrate to replace ITO glass.....	89
Fig. 6-3 Base current of flexible SCLT on PEN substrate.....	90
Fig. 6-4 Two prototypes of future organic transistors.....	90

LIST OF TABLES



Table 2-1 Descriptions of symbols.....	14
Table 2-2 Parameters of lithography process.....	26
Table 4-1 Comparison sheet of ARC and mr-I 7020R..	51
Table 5-1 Comparison table of wet-etch and strip-off method.....	85

Chapter 1 Motivation and Introduction



1-1 Motivation

In recent years, portable electronic devices have shown their great profit margins in consumer market. Frequent change in product generation indicates the likely winning keys for these types of products are low-cost, large-area mass production, and flexible substrates.

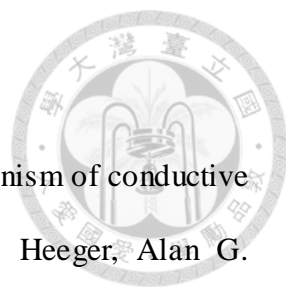
Two major conventional fabrication processes for organic electronic devices are the evaporation-based and the solution-based processes. The evaporation-based process needs more expensive vacuum equipment and longer process time. Furthermore, when applied in larger-area fabrication, bigger vacuum equipment is also needed, which is definitely much more expensive. This is also the reason why the large-area active-matrix organic light-emitting diodes (AMOLEDs) display products are usually expensive. On the other hand, the organic transistors made by solution-based process are low-cost and time-saving, because of the use of spin-coating or spray-coating equipment in the fabrication process. But using conventional photolithography to pattern a solution-processed, flexible large-area substrate is difficult.

According to our study, the key contributions parameters to improving the performance of space-charge-limited transistor (SCLT) device are (1) to reduce the hole diameter of metal mesh, and the (2) to decrease leakage current of base-electrode when the pattern uniformity of metal mesh is obtained. However, the hole diameter was limited by the wavelength resolution of optical lithography' light source. And wet-etching method which used to fabricate metal mesh might produce residue in the

channel, causing large leakage current.

In this thesis we demonstrate the usage of atomic layer deposition-assisted (ALD-assisted) nanoimprint lithography (NIL) to transfer patterns generated by interference lithography (IL) from mold to substrate. The well-ordered, sub-100 nm nano metal meshes used as the base-electrode for the space-charge-limited transistor (SCLT) could be obtained. And the output current of SCLT increased 1000%. Furthermore, we developed a solvent-free lift-off method: the strip-off method to replace wet-etching method. The base leakage current reduced nearly ten times after strip-off method was applied. And the pattern uniformity of mesh was significantly improved. We believe this novel method is very promising for large area fabrication process for variety types of substrates.

1-2 Space-charge-limited transistors



Before 1970s, the charge transfer mechanism and doping mechanism of conductive polymers had not been explained clearly yet. In 1977, Alan J. Heeger, Alan G. MacDiarmid from University of Pennsylvania and Hideki Shirakawa from University of Tsukuba both reported high conductivity in oxidized iodine-doped polyacetylene and successfully clarified its conductivity with classic electron transportation theory [1]. Their works drew attention of scientists and encouraged the rapid growth of the field. And they were rewarded the 2000 Nobel Prize in Chemistry "*for the discovery and development of conductive polymers*". In 1987, Ching W. Tang and Steven V. Slyke from Eastman Kodak developed the first organic diode. This device used a novel two-layer structure with separate hole transporting and electron transporting layers such that recombination and light emission occurred in the middle of the organic layer [2]. This resulted in a reduction in operating voltage and improvements in efficiency that led to the current era of organic light-emitting diode (OLED) research and device production. In 2005, Philips revealed their flexible 4.7-inch display technology. They used organic thin film transistors as the driver for AMOLED.

The long channel length of traditional horizontal-channel OTFT might cause disadvantages such as low output current and high operational voltage. Since the channel length was determined by lithography process, to shorten the channel length, we need higher resolution lithography equipment, and therefore higher production cost.

In 2006, Hsin-Fei Meng and Sheng-Fu Horng from National Chiao Tung University and National Tsing Hua University developed the vertical-channel organic transistor: space-charge-limited transistor (SCLT). The length of its vertical-channel was determined by the thickness of the active layer, which could be easily controlled by

changing coating parameters.

The working concept of SCLT is similar to a vacuum tube, which is schematically shown in Fig. 1-1. The heated filament (cathode) releases electrons into the vacuum, a process called thermionic emission. A second electrode, the anode or plate, will attract those electrons if it is at a more positive voltage. The result is a net flow of electrons from the filament to plate. Electrons cannot flow in the reverse direction because the plate is not heated and does not emit electrons. The magnitude of this current can be controlled by a voltage applied between the cathode and the grid. The grid acts like a gate for the electrons. A more negative voltage on the grid will repel some of the electrons, so fewer get through to the plate, reducing the plate current.

Similarly, the carrier (hole) in SCLT's channel was injected from emitter. The nano meshes base-electrode labeled in Fig. 1-2 acts as a switch to control the carrier flow [3, 4]. The organic material is used as a channel for carriers. As Fig. 1-3 shows, when the bias applied on the base electrode is positive, there will be a high potential barrier in the channel. The injected carrier cannot pass through the channel (OFF state). On the other hand, when the applied bias is negative, the potential barrier will not exist. The carrier can pass to the collector via channel (ON state). So the fabrication of nano mesh base-electrode is the major factor that determines the performance of SCLT.

However, the colloidal lithography [5] used in the previous work might not be compatible with existing commercialized process tools, and even worse the inevitable random accumulation of nanospheres during the process could incur large holes on the base electrode as shown in Fig. 1-3(a), causing leakage current and made it difficult to have uniform leakage control [6].

A solution to completely removing such accumulation is to use NIL and IL. IL is a mask-free photolithography method. Its major advantage is its capability of fabricating

a large-area periodic nano pattern in one exposure step. By the help of IL, we can easily fabricate large-area periodic hole-array pattern which has shown in Fig. 1-3(b) and transfer the pattern to the surface of SCLT substrate by NIL. The large-area, well-ordered nano metal mesh used as the base-electrode could be fabricated in a fast and cheap way. Compared to the short channel length OFET with much higher carrier mobility ($>10 \text{ cm}^2/\text{V}\cdot\text{s}$) active material [7], the *imprinted* SCLT has lower production cost and it can operate at a relative low voltage ($\sim 2\text{V}$). The performance of SCLT thus can be significantly improved when a high mobility material is applied.

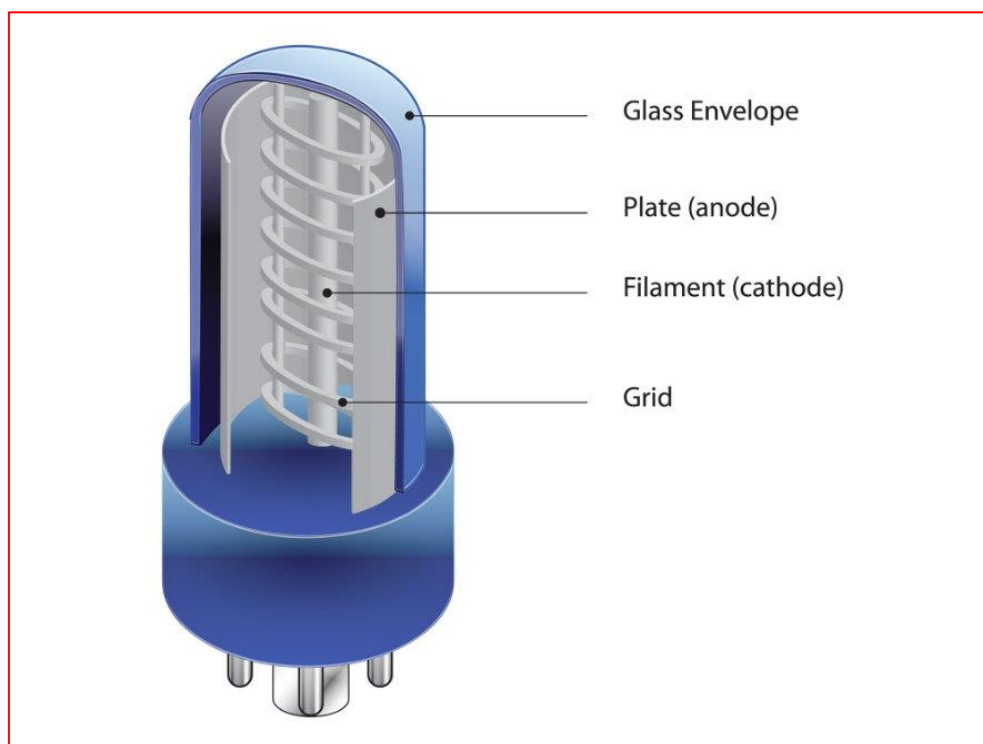


Fig. 1-1 Schematic diagram of a vacuum tube.

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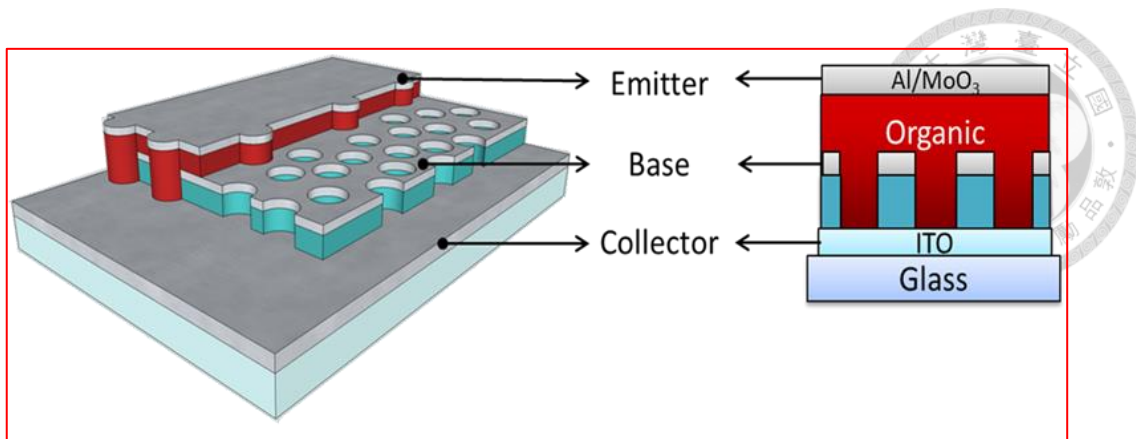


Fig. 1-2 Schematic diagram of an SCLT.

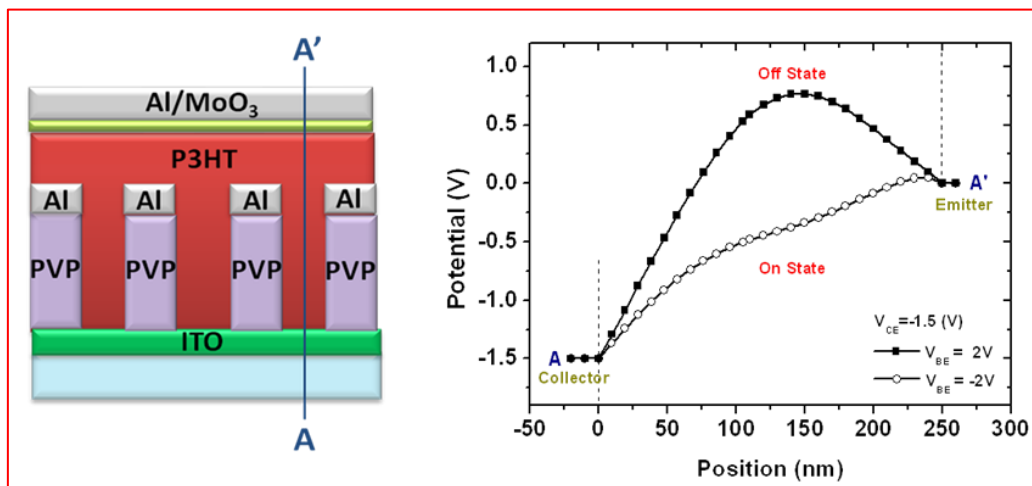


Fig. 1-3 Potential distribution from emitter to collector at the center of channel.

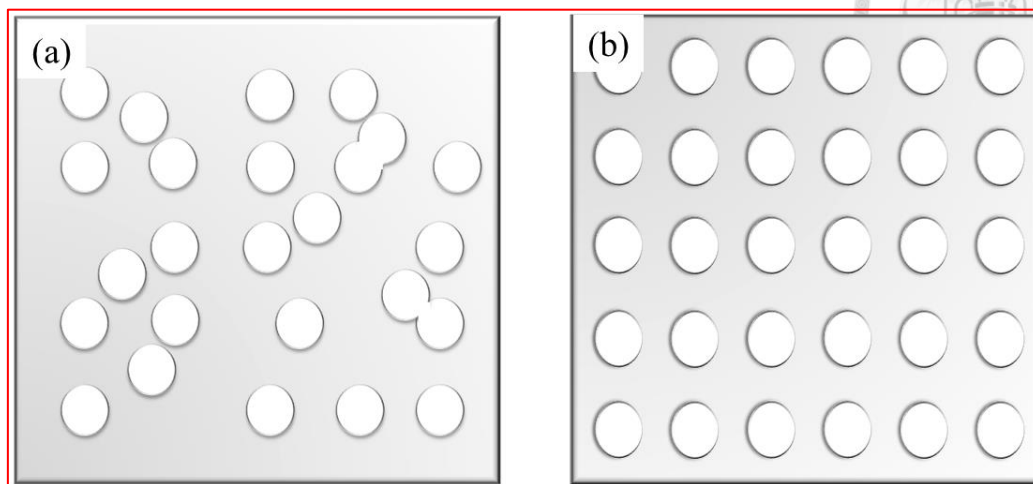
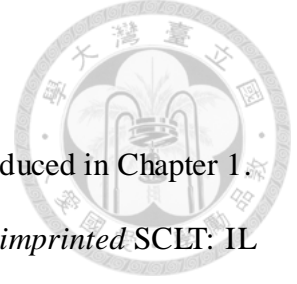


Fig. 1-4 Nano mesh made by (a) colloidal lithography (random order) and (b) nanoimprint lithography (periodic order).

1-3 Organization of the thesis



The background and working principle of SCLT are briefly introduced in Chapter 1. In Chapter 2, we will introduce the basic fabrication methods of the *imprinted* SCLT: IL and NIL. The two beam IL system in our lab and its working principle will be discussed. The history and working principle of NIL will be also introduced, and followed up by the fabrication process of the 1st generation SCLT.

In Chapter 3, the ALD process will be introduced to reduce hole diameter of metal mesh. To successfully transfer the pattern by NIL, we will introduce *h*-PDMS as our new imprint stamp material, and then briefly describe the fabrication process of the 2nd generation SCLT. The discussion of the electrical measurement results of SCLT will be in at the last part of this chapter.

To reduce the base leakage current, we will introduce the non-wet-etching method, the lift-off method to replace the wet-etching method in the fabrication process in Chapter 4. The basic concept of lift-off and its merits and drawbacks will be discussed. To overcome all the problems, a novel strip-off method will be introduced. The inspiration of developing the strip-off method and its working principle will be described. Finally the electrical measurement results of the 3rd generation SCLT will be listed and compared to the 1st and 2nd generation SCLTs.

In Chapter 5, the possible applications of nano metal structures which made by strip-off method will be listed, including optic devices, electronic devices, and sensing devices.

In Chapter 6, we will make a brief conclusion of the development of *imprinted* SCLTs. The needed improvements for future development and potential will be also described.

Chapter 2 Fabrication of Imprinted SCLT



2-1 Nanoimprint Lithography

Nanoimprint lithography (NIL) is a simple nanolithography process with low cost, high throughput and high resolution. In 1996, Stephen Y. Chou from University of Minnesota first demonstrated this hot-embossing technique in *Science* [8]. After worldwide efforts, nanoimprint lithography has been added to the International Technology Roadmap for Semiconductors (ITRS) for one of the candidate for 32 nm nodes in 2003. Since then nanoimprint has been listed as a potential tool for ever smaller nodes by ITRS, for example, 12 nm node in 2013.

There are many different types of nanoimprint lithography, two of them are most important: *thermoplastic nanoimprint lithography* and *photo nanoimprint lithography*. Both of them require originally patterned imprint stamp in order to transfer the pattern to a target substrate.

A simple thermal NIL process is shown in Fig. 2-1. First, the thermoplastic resist is coated on a substrate. Then the patterned stamp with nanometer-scale features is pressed to the resist cast on the substrate. The resist must be heated during the pressing step. If the temperature is above the polymer's glass transition temperature (T_g), the polymer behaves as a viscous liquid and is able to flow, thereby conforming to the stamp. After the stamp is removed, an isotropic etching process (e.g. reactive ion etching) is used to transfer the pattern into the entire resist thickness by removing the residual layer in the compressed areas.

Because the NIL method is a physical contact patterning method, so it will not face

the resolution restriction caused by diffraction limit. Once the imprint stamp fabricated by e-beam lithography or DUV lithography, it can be used to duplicate the pattern for many times. The sub-100 nm large-area pattern like hole-array and rod array which have shown in Fig. 2-2 can be fabricated faster and cheaper than by using conventional photolithography [8].

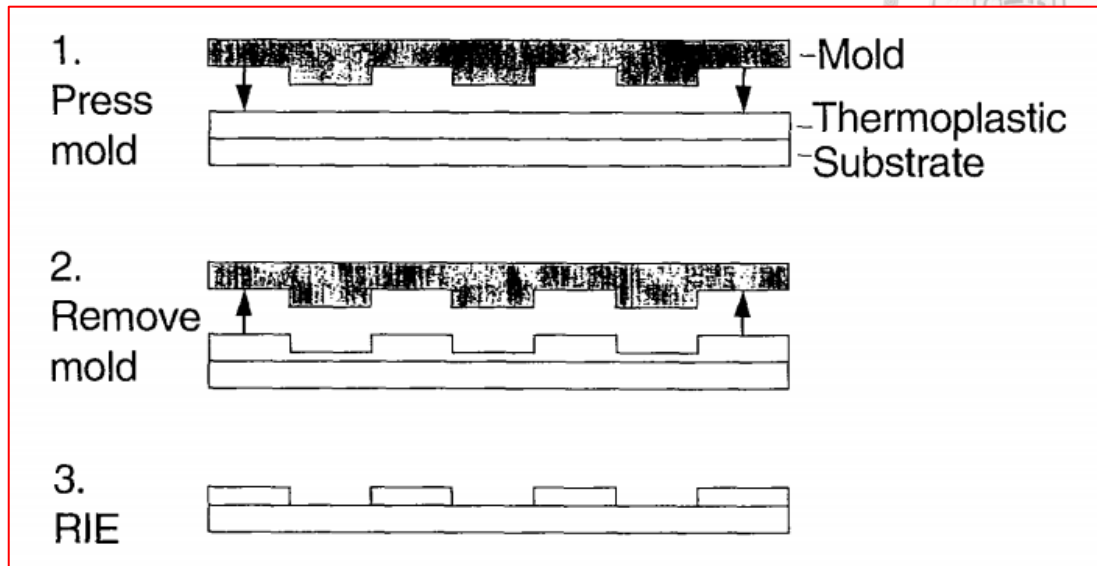


Fig. 2-1 Schematic diagram of the NIL process [8].

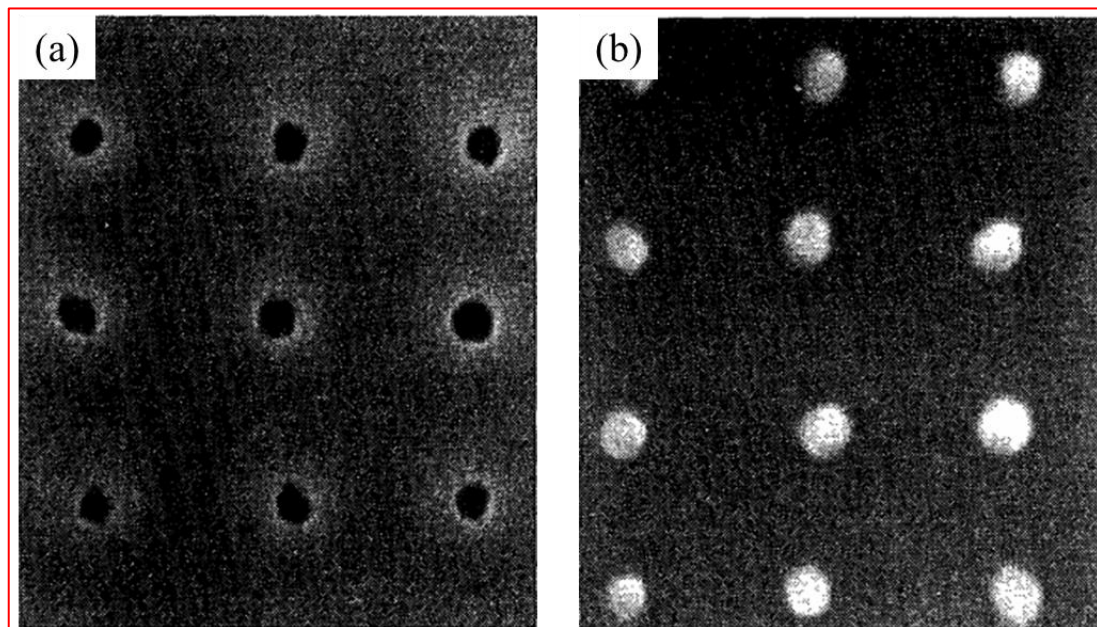


Fig. 2-2 SEM photos of (a)holes and (b)dots array pattern made by NIL, both of them are 25 nm in diameter [8].

2-2 Two-beam interference lithography



2-2-1 IL concept

Photolithography is widely used in semiconductor fabs to create integrated circuits (IC). As compared to the well-established traditional mask-based optical lithography, mask-free interference lithography (IL) is one of the most powerful yet relatively inexpensive methodologies for creating large-area patterns with micron- to nanometer-scale periodicities [9].

Assume an incident light can be written as:

$$\mathbf{E}_j = E_j \exp[i(\vec{k}_j \cdot \vec{r} - \omega t + \varphi_j)] \quad (2.1)$$

All the parameters are described in Table 2-1. Following the superposition principle, the total electric field \mathbf{E} consists of multiple coherent light \mathbf{E}_j can be written as:

$$\mathbf{E}(r, t) = \mathbf{E}_1(r, t) + \mathbf{E}_2(r, t) + \cdots + \mathbf{E}_n(r, t) \quad (2.2)$$

Then the intensity distribution of the light will be:

$$I(r) \propto |\mathbf{E}(r, t)|^2 = \sum_{i=1}^n |E_i|^2 + \left\{ \sum_{a=1}^n \sum_{b=1}^n \mathbf{E}_a \mathbf{E}_b \exp i[(\vec{k}_a - \vec{k}_b) \cdot \vec{r} + (\varphi_a - \varphi_b)] \right\}_{a \neq b} \quad (2.3)$$

It is clear to see that the intensity has a periodical variation. In the case of

two-beam interference lithography which is shown in Fig. 2-3, the period (Λ) of interference fringes on the exposure plane is:



$$\Lambda = \frac{\lambda}{\sin \theta_L + \sin \theta_R} \quad (2.4)$$

where λ is the wavelength of incident light, θ_L and θ_R are the incident angles of left and right beams.

Fig. 2-4 shows our IL system used in this study. The light source is an argon-ion laser (BeamLok 2060, ©Spectra-Physics), emitting in ultra-violet (UV) at a wavelength 364 nm with a continuous-wave (CW) output power of about 135 mW. Since the positions of two reflective mirrors (M_{IL-1} , M_{IL-2}) are symmetric, then the incident angles $\theta_R = \theta_L = \theta$. So the incident angles of both beams are the same. Eq. (2.4) can therefore be written as:

$$\Lambda = \frac{364}{2 \sin \theta} nm \quad (2.5)$$

E	E	\vec{k}	\vec{r}	ω	t	φ
electric field	amplitude of electric field	wave vector	position vector	angular frequency	time	phase

Table 2-1 Descriptions of symbols.

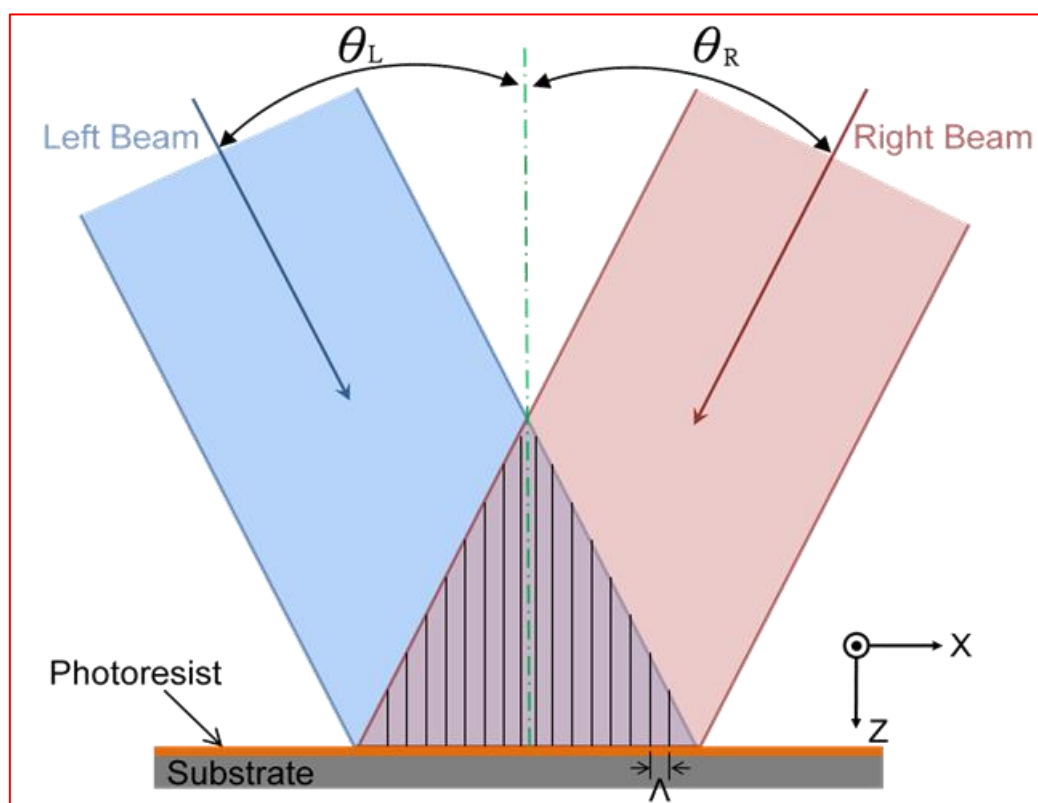


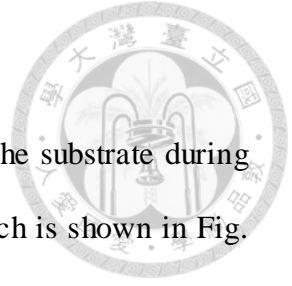
Fig. 2-3 Schematic of 2-beam IL [10].

2-2-2 ARC thickness design

The incident light may interfere with the light reflected from the substrate during exposure process, causing periodic exposure intensity variation which is shown in Fig. 2-5. This phenomenon is so called “standing wave effect”.

Standing wave effect will cause wave-like profile on the sidewall of photoresist (PR) structure as shown in Fig. 2-6. Since the PR structure will be used as the original imprint mold, these defects will become problematic when the stamp is removed from the mold.

A solution to preventing this effect is to use anti-reflection coating (ARC). ARC is composed of transparent thin film structures, with alternating layers of contrasting refractive indices [12]. The layer thickness labeled in Fig. 2-7 was controlled precisely such that it is exactly one quarter of the wavelength of light in the layer ($\lambda/4$). If the intensities of the two beams R_1 and R_2 are exactly equal, they will destructively interfere and cancel each other since they are exactly out of phase. Therefore, there is no reflection from the surface of substrate. The ARC we used in this work (XHRiC-11, © Nissan Chemical Industries) is designed for i-line ($\lambda=365$ nm) lithography, so it is suitable for our argon laser IL.



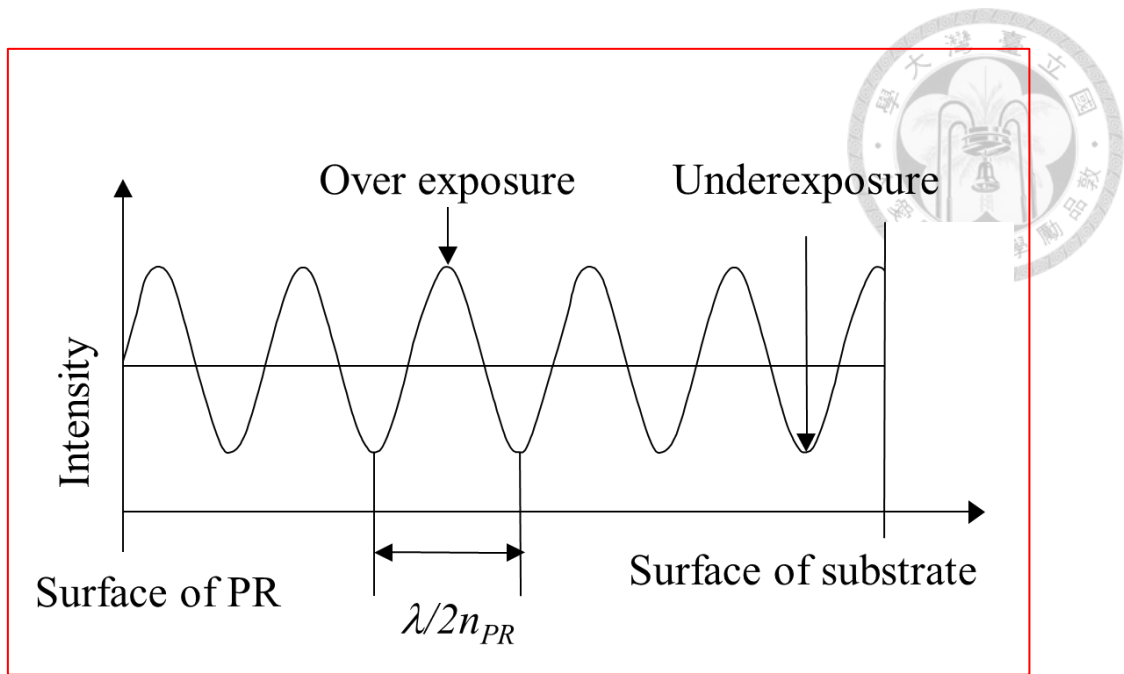


Fig. 2-5 Intensity distribution diagram along the perpendicular direction of substrate and PR surface.

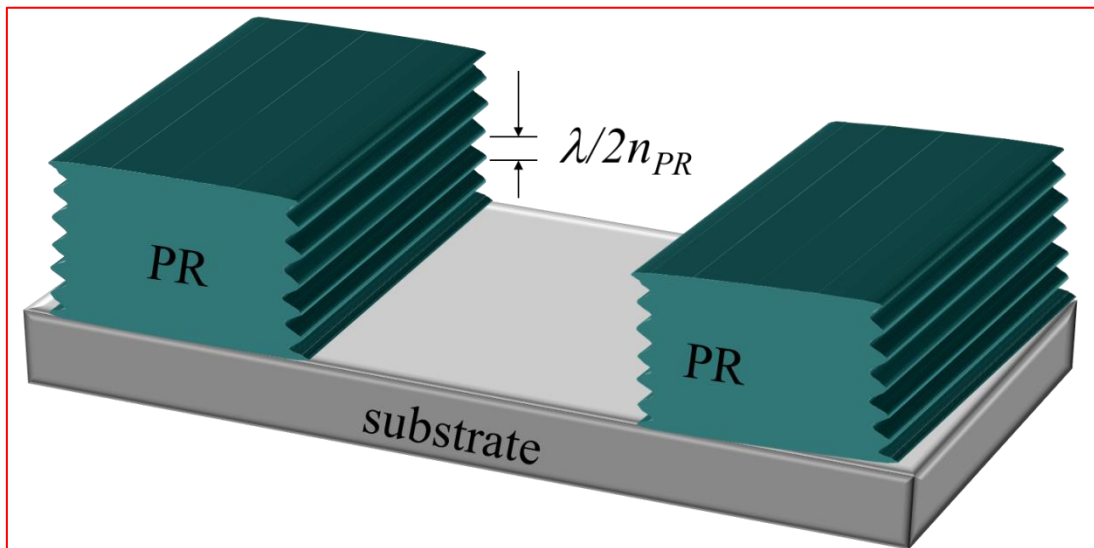


Fig. 2-6 Defects on the PR sidewall caused by Standing Wave Effect.

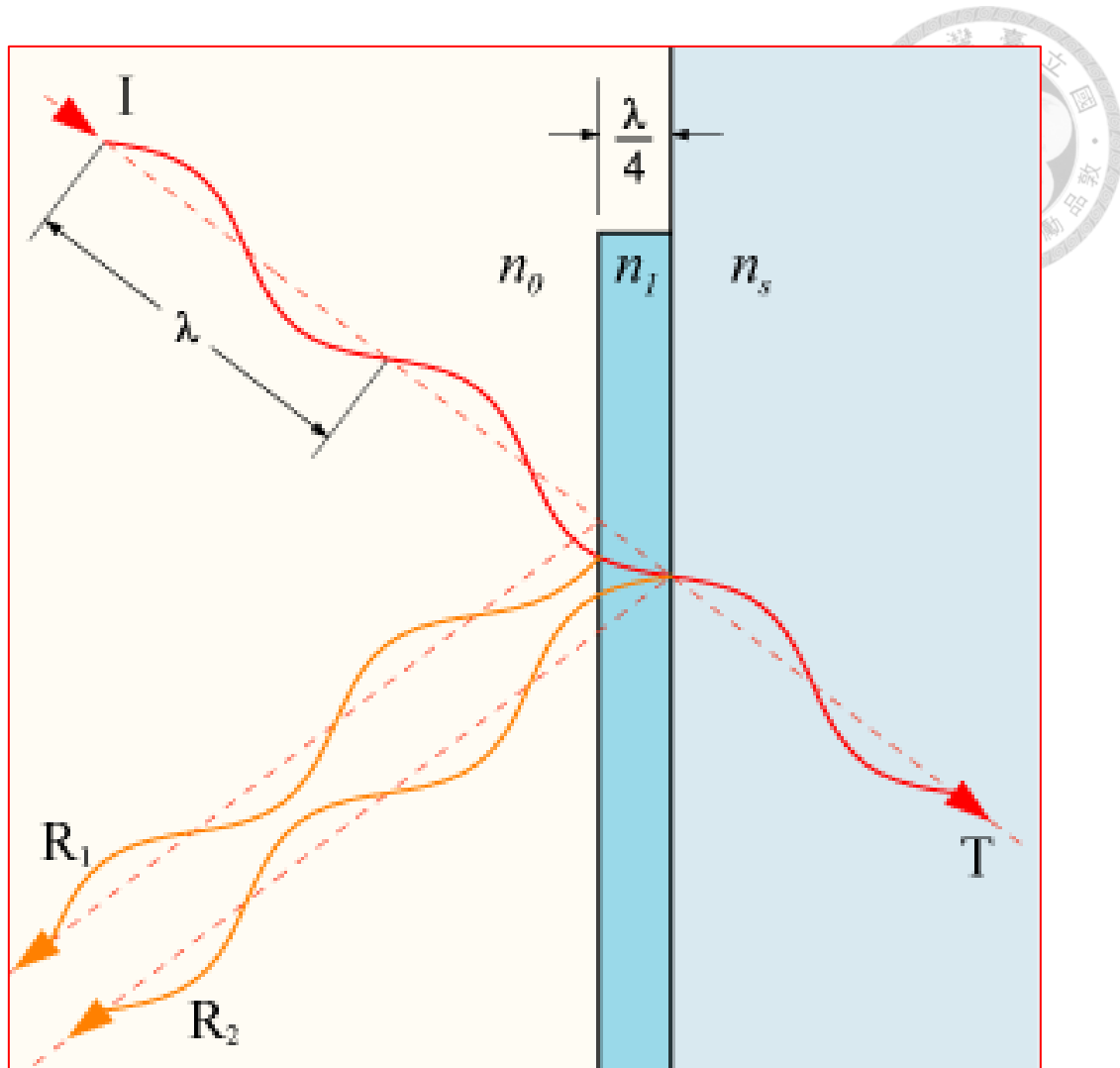
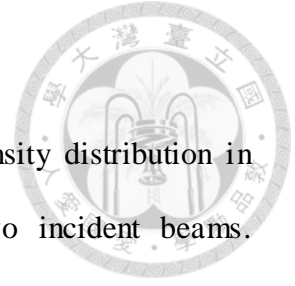


Fig. 2-7 Interference in a quarter-wave anti-reflection coating.

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2-2-3 Exposure dose of photoresist pattern



Two-beam interference lithography results in sinusoidal intensity distribution in horizontal direction over the overlapping exposure area of two incident beams. Depending on the amount of energy received locally, the photoresist will either be exposed or unexposed. After development process, the exposed/unexposed region dissolves, depending on the tone of photoresist. Fig. 2-8 shows the latent image of exposed photoresist and a wider exposed region on top due to the light absorption by photoresist.

A simple binary model is used here to estimate the linewidth of PR pattern. The PR is assumed to have infinite material contrast. In a binary PR model shown in Fig. 2-9, the PR regions receiving a dose above the threshold dose are fully exposed and the other regions are unexposed. As discussed in Fig. 2-8, the exposed regions of positive resist are removed by the developer. However, for the negative resist the unexposed regions are removed. The linewidths of residual resists labeled in Fig. 2-9 for both negative and positive are d_n and d_p , respectively. D_{avg} represents the average dose and $D_{threshold}$ represents the threshold dose of PR.

The ratio of linewidth and grating period is called duty cycle, which is affected by two parameters, exposure dose and contrast, in the binary model. Since the intensities of the two beams in our work are set to the same, the exposure dose is the most general way for the linewidth control. As depicted in Fig. 2-9, the dose D_2 is two times of D_1 and D_3 is three times of D_1 . By increasing the dose, there will be more exposed regions whose doses are higher than $D_{threshold}$. The increasing exposed areas represent smaller linewidth for positive photoresist (d_p) and bigger linewidth for negative photoresist (d_n). Oppositely the duty cycle is increased for negative photoresist.

The pattern generated by 2-beam IL is grating, which is a composed set of straight lines. To fabricate the hole-array pattern suitable for base-electrode, the double-exposure method is introduced.

After the first exposure with half of the designed exposure dose, the substrate is rotate by 90 degree. Then the second exposure with the same dose is applied. Since the margin of PR pattern will form a continuous curve after post-exposure bake (PEB), the hole-array pattern which has shown in Fig. 2-10 can be fabricated.

As mentioned, we can adjust the sidewall thickness of PR pattern by changing the exposure dose. Fig. 2-11 shows the shape variation of different doses.

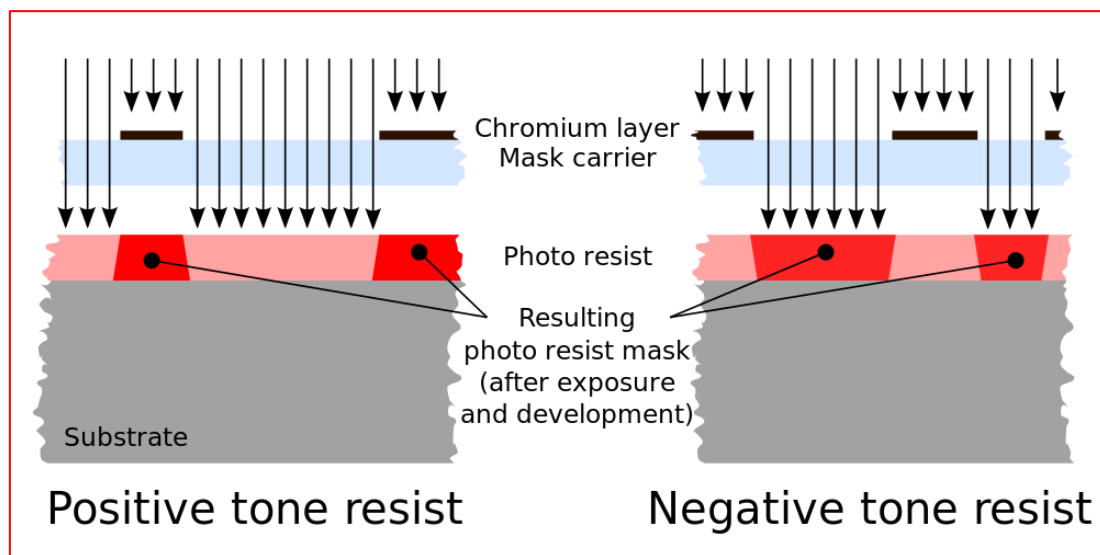


Fig. 2-8 Illustration of two exposed photoresists with different tone after development.
Copyright © Wikipedia Commons

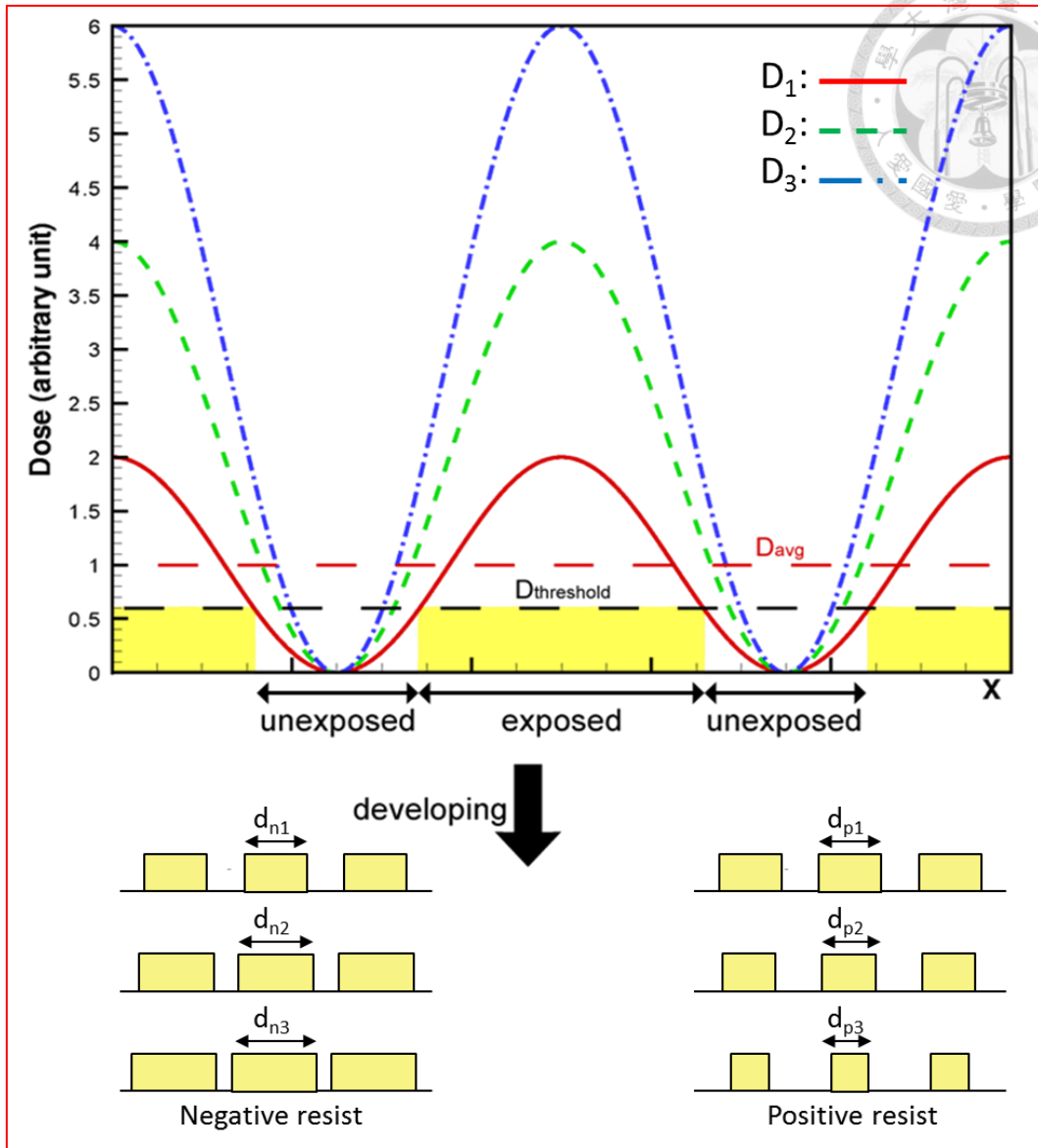


Fig. 2-9 The binary photoresist model for exposure and development. The regions of exposure dose higher than threshold dose are exposed. There are more exposed regions whose doses are higher than threshold dose when D_{avg} increases. The increasing exposed areas represent smaller linewidth, for positive photoresist and bigger linewidth for negative photoresist.

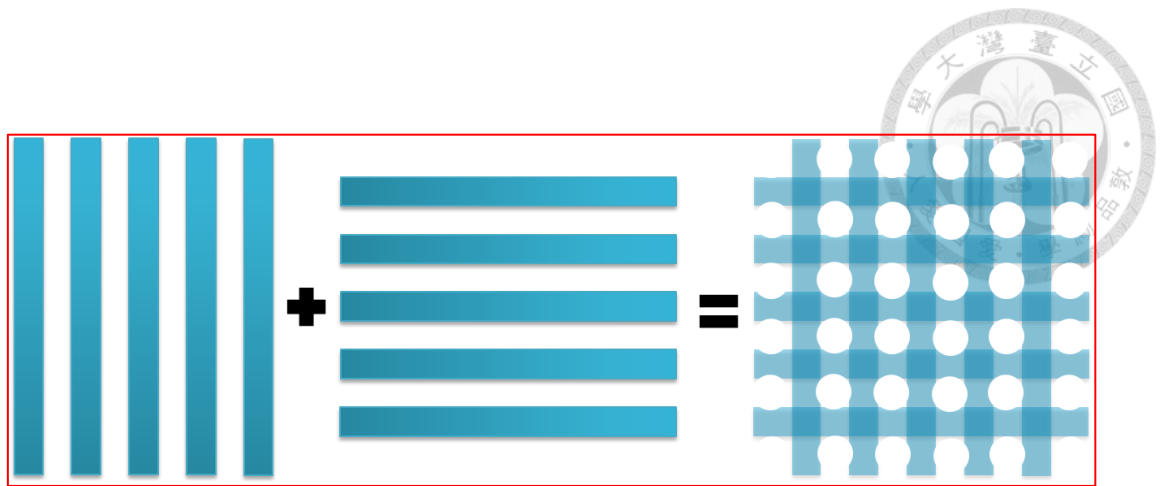


Fig. 2-10 Hole-array PR pattern generated by double-exposure.

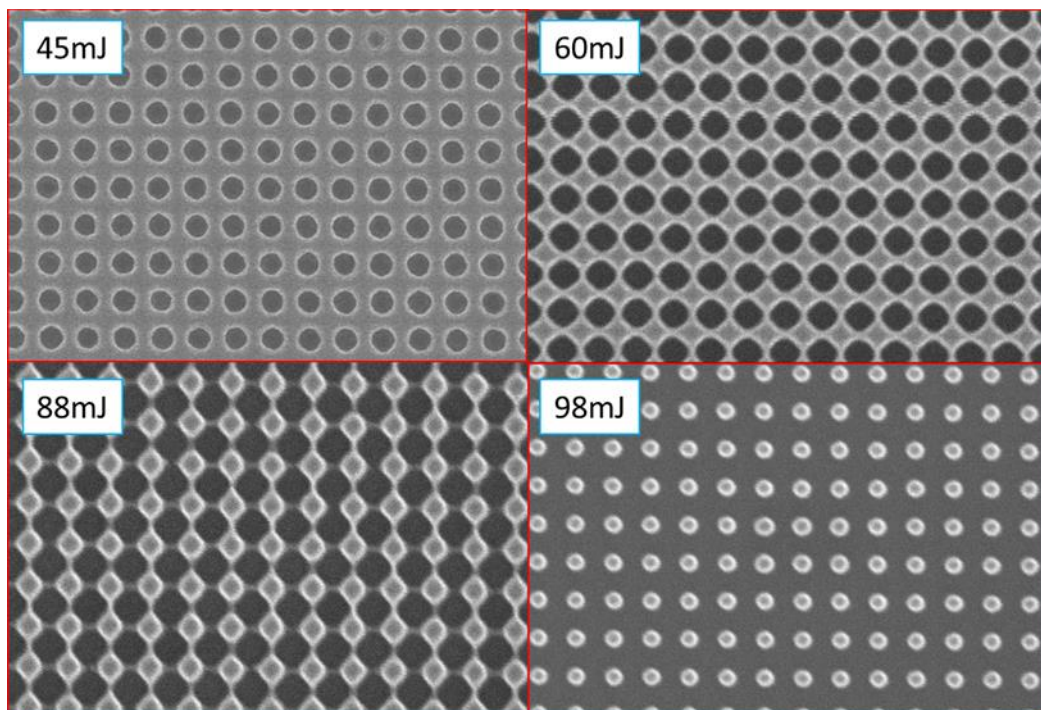


Fig. 2-11 PR patterns with different exposure dose. All patterns have the same period setting (245 nm).

2-3 Fabrication processes of imprinted SCLT



Substrate fabrication

The substrate of the SCLT device is a 3*3 cm² Indium Tin oxide (ITO) glass. Total thickness is 7mm. Thickness of ITO layer is 200 nm. The PR pattern which has shown in Fig. 2-12 will be transferred to ITO layer by wet etching (etchant: HCl).



Fig. 2-12 Patterned ITO glass substrate of an SCLT.



Fabrication of SCLT

The fabrication process of an *imprinted* SCLT has been shown in Fig. 2-13. The lithography parameters are listed in table 2-1.

(a) The positive photoresist (ULTRA-*i*TM123, © Rohm and Haas Electronic Materials) has been spun onto a 4-inch silicon wafer which was coated with the ARC layer.

(b) The double-exposure IL has been applied in order to fabricate PR hole-array pattern. The wavelength of light source is 364 nm. Then we use *tetramethylammonium hydroxide* (TMAH) 2.38% solution (NMD-W, © Eternal Chemical Co., Ltd) as the developer.

(c) The *polydimethylsiloxane* (PDMS) (Sylgard 184, © Dow Corning) was poured onto the PR pattern and be baked at 65°C for 8 hours in order to form a patterned imprint stamp.


(d) The ITO glass substrate has been soaked in acetone for 10 minutes supersonic vibration cleaning. Then the acetone will be replaced by *iso-Propyl alcohol* (IPA) for another 10 minutes cleaning.

(e) The 100 W power O₂ plasma generated by reactive ion etcher (RIE) was used to planarize ITO surface.

(f) The cross-linkable *poly(4-vinyl phenol)* (PVP) (8 wt.%) and cross-linking agent *poly(melamine-co-formaldehyde)* (PMF) were dissolved in *propylene glycol monomethyl ether acetate* (PGMEA) with a PVP:PMF mass ratio of 11 : 4. The solution was spin coated on an ITO glass substrate and annealed at 200°C for 1 hour to form a 300 nm film.

(g) Then the ARC layer which is used as the imprint resist was spun coated onto

aluminum layer.

- 
- (h) The pattern of PDMS stamp was transferred to the ARC layer by thermal NIL.
 - (i) The residual layer of ARC after NIL process was removed by CF_4/O_2 mixture plasma.
 - (j) An aluminum wet etchant ($\text{H}_3\text{PO}_4 : \text{HNO}_3 : \text{CH}_3\text{COOH} : \text{H}_2\text{O} = 50 : 2 : 10 : 9$) was used to etch the uncovered aluminum to fabricate nano aluminum meshes.
 - (k) Then we use Al meshes as the etch mask. Uncovered PVP was etched by O_2 plasma in order to form the vertical channel of SCLT.
 - (l) The 4.5 wt% *poly(3-hexylthiophene)* (P3HT) solution which *chlorobenzene* (CB) was the solvent then will be coated to form the active layer of SCLT. Layer thickness is around 400 nm.
 - (m) Finally the 10 nm-thick MoO_3 and 40 nm-thick Al have been evaporated onto P3HT sequentially in order to be the upper emitter-electrode.



	ARC	Photoresist
Spin rate (rpm)	500, 18sec	500, 10sec
	1700, 90sec	3500, 90sec
Soft bake (°C)		90, 90sec
Post-exposure bake (°C)		120, 120sec
Develop (sec)		60
Hard bake (°C)	175, 90sec	120, 90sec

Table 2-2 Parameters of lithography process.

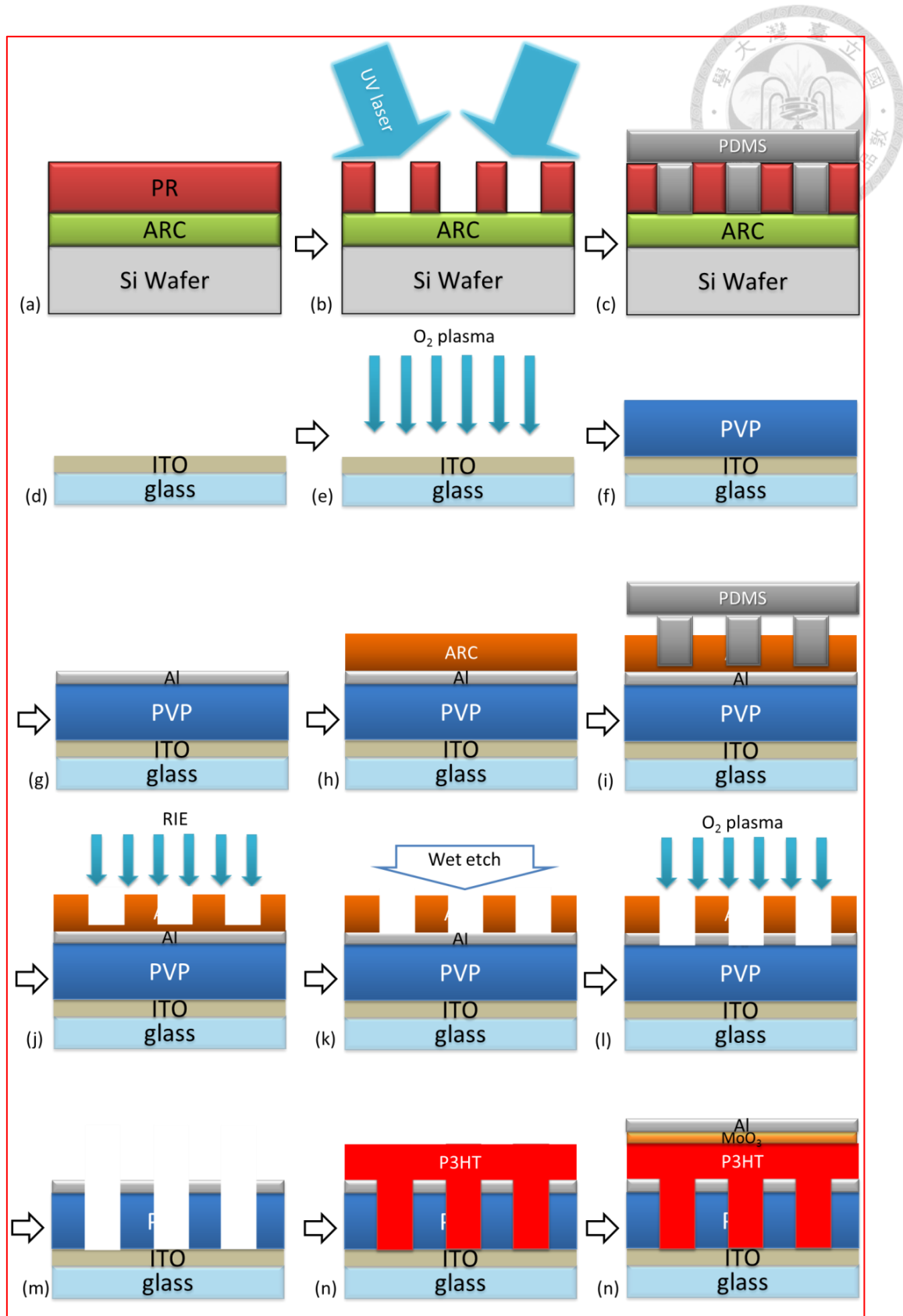


Fig. 2-13 Fabrication process of an imprinted SCLT.

Chapter 3 Sub-100 nm ALD-assisted Nanoimprint Lithography



3-1 ALD-assisted dimension shrinkage

In the previous study, we found that the capability of potential control from the SCLT's metal mesh electrodes was not uniform. Due to the potential distribution inside the vertical channel, the controlling ability of base electrode is the strongest at the middle of the channel length. To improve the ON/OFF current ratio of SCLT, we need to increase the channel density and reduce the channel dimension at the same time [13, 14]. According to the simulation results shown in Fig. 3-1, the ON/OFF current ratio of a SCLT device which has 100 nm hole diameter of its base-electrode is two orders of magnitude higher than the one which has 300 nm hole diameter.

With the help of nanoimprint lithography, we successfully avoided the random accumulation of nanospheres which might cause large holes on the base-electrode. However, since the thickness of aluminum layer in an SCLT was around 40 nm, the sidewall thickness of hole-array pattern should be greater than 50 nm to accommodate the tolerance needed for isotropic wet etching the aluminum layer. As shown in Fig. 3-2, if the diameter of hole is initially set to be 120 nm, the period of IL pattern will be 170 nm, which is beyond the current capability of our IL system. The first generation *imprinted* SCLT in our lab whose hole diameter was 270 nm exhibited an ON current of 0.35 mA/cm² and an ON/OFF current ratio of around 3000 at 1.8 V [15].

Limited by our current lithography equipment set up, the period of our IL-generated pattern is at least 250 nm, therefore, a physical dimension shrinkage

method is desired to obtain sub-100 nm hole diameter without reducing the sidewall thickness. One possibility without resorting to immersion lithography or e-beam lithography is the use of ALD. It is known that ALD has an inherent advantage of being able to deposit an ultrathin (\sim few Å), conformal, and smooth films on a structured surface. It could also be used to accurately adjust the hole diameter of a hole-array pattern [16-18].

The fabrication process of the ALD-assisted dimension shrinkage is shown in Fig. 3-4. After the ALD process, the original hole-array pattern PR mold was completely covered by aluminum-oxide (Al_2O_3) thin film. Since the sidewall of hole-array structure became thicker, the hole diameter could be successfully reduced.

However, the photoresist we used in this work would melt down around 150°C . So the *low-temperature* ALD process instead of the conventional method [19] was used, in which large gas purge and high pressure water vapor [20, 21] were applied to the polymer surface. The ALD equipment we used in this work has shown in Fig. 3-5. After 10 ~ 15 cycles of ALD process, an aluminum-oxide (Al_2O_3) film with 40~50 nm thickness with good uniformity was formed on the PR pattern. The diameter of the hole in the pattern was reduced by 50% as shown in Fig. 3-6. Note that the sidewall of hole-array pattern also became thicker, which increased the subsequent process tolerance.

In many cases, the imprint mold is generally made from Si, SiO_2 , or other rigid materials. A photoresist layer was usually used as a sacrificial etch mask and then completely removed after the pattern was transferred from the PR layer to the rigid substrate by using etching method. However, it is known that fine-tuning the profile of etched pattern is hard during mold fabrication, especially for the high aspect ratio pattern. In contrast, fine-tuning the profile of PR pattern is much easier. The Al_2O_3 thin

film on the PR surface is hard and tough enough to protect the inner polymer structure [22]. Since oxygen, moisture and other components in the air were isolated from the inner PR structure, the lifetime of pattern would be prolonged. The ALD-assisted Al_2O_3 -covered PR pattern could therefore be directly used as an imprint mold with good profile control. Fig. 3-7 shows good mechanical durability when a new stamp was used more than 30 times for imprinting. The defects in Fig. 3-7(c) were resulted from the unprotected storage environment of the mold.

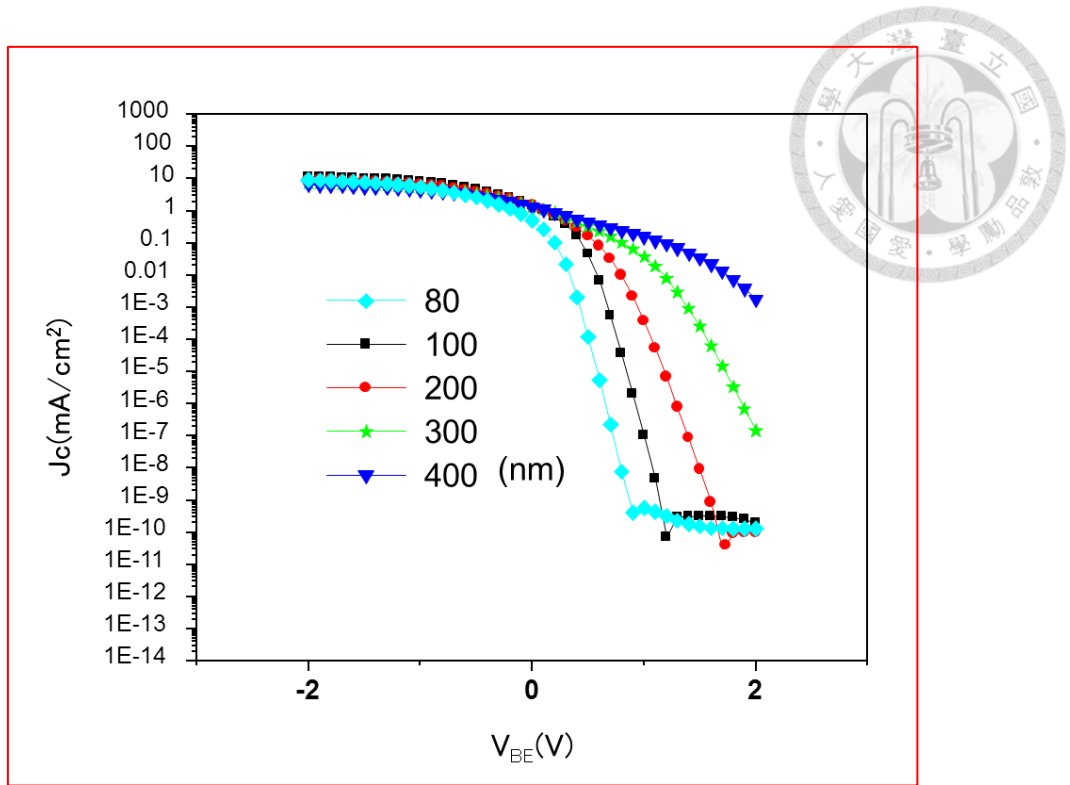


Fig. 3-1 Transfer characteristics of SCLT devices with different hole diameters.

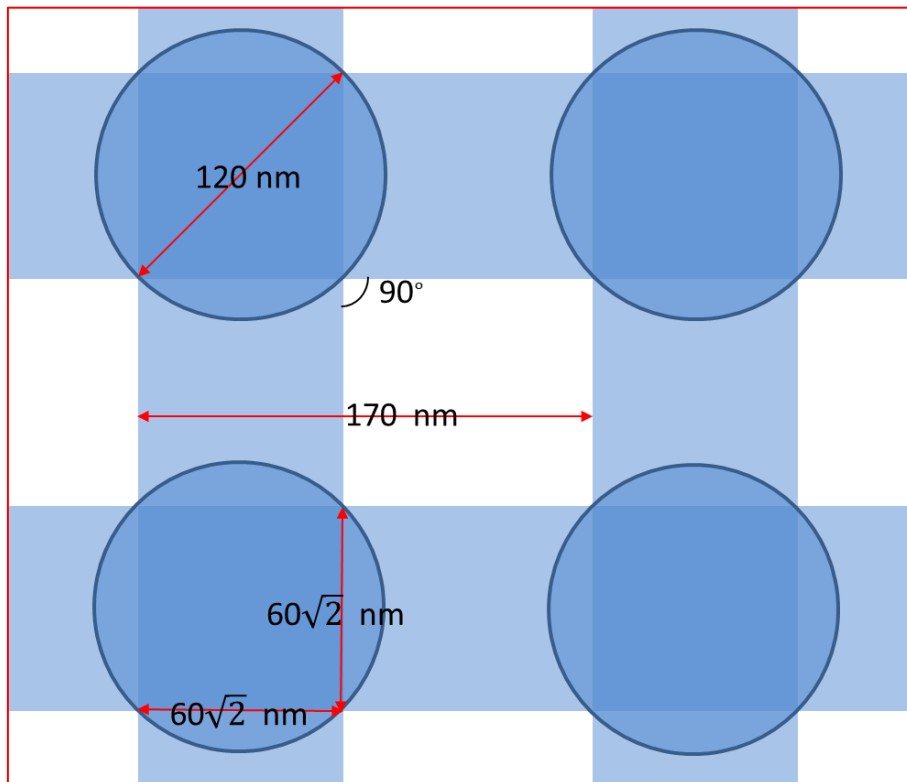


Fig. 3-2 Relation between grating period and hole diameter.

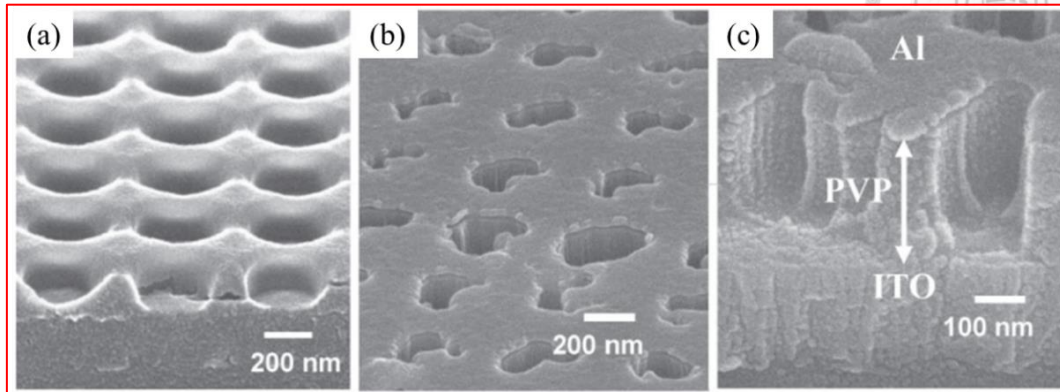


Fig. 3-3 SEM images of the (a) ARC pattern and Al nanopore structure after Al wet etching. (b) and (c) Vertically oriented PVP cylindrical nanopores covered by the Al hard mask [15].

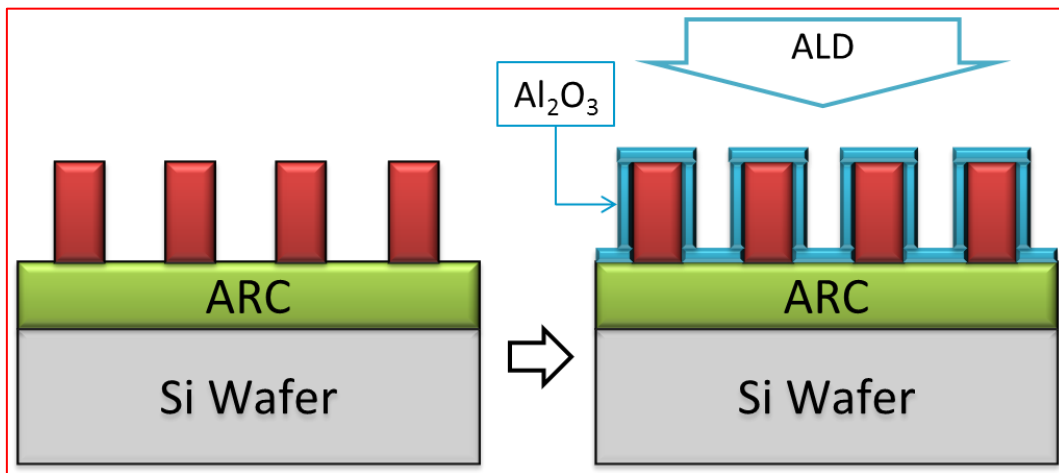


Fig. 3-4 Fabrication process of the ALD-assisted dimension shrinkage method.

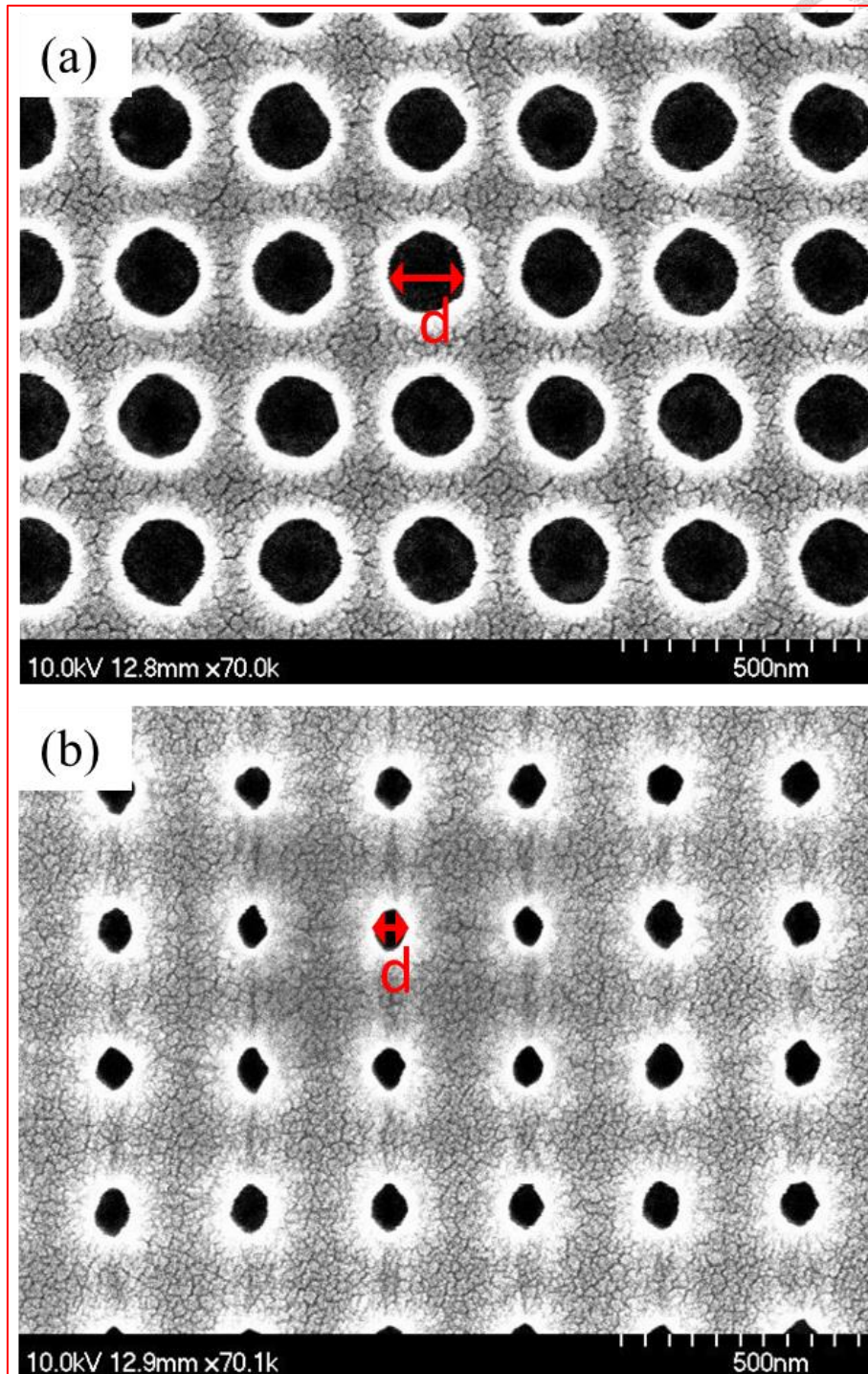


Fig. 3-5 SEM images of (a) PR pattern before growing ALD Al_2O_3 .

(hole diameter = 180 nm)

And (b) PR pattern after growing ALD Al_2O_3 . (hole diameter = 85 nm)

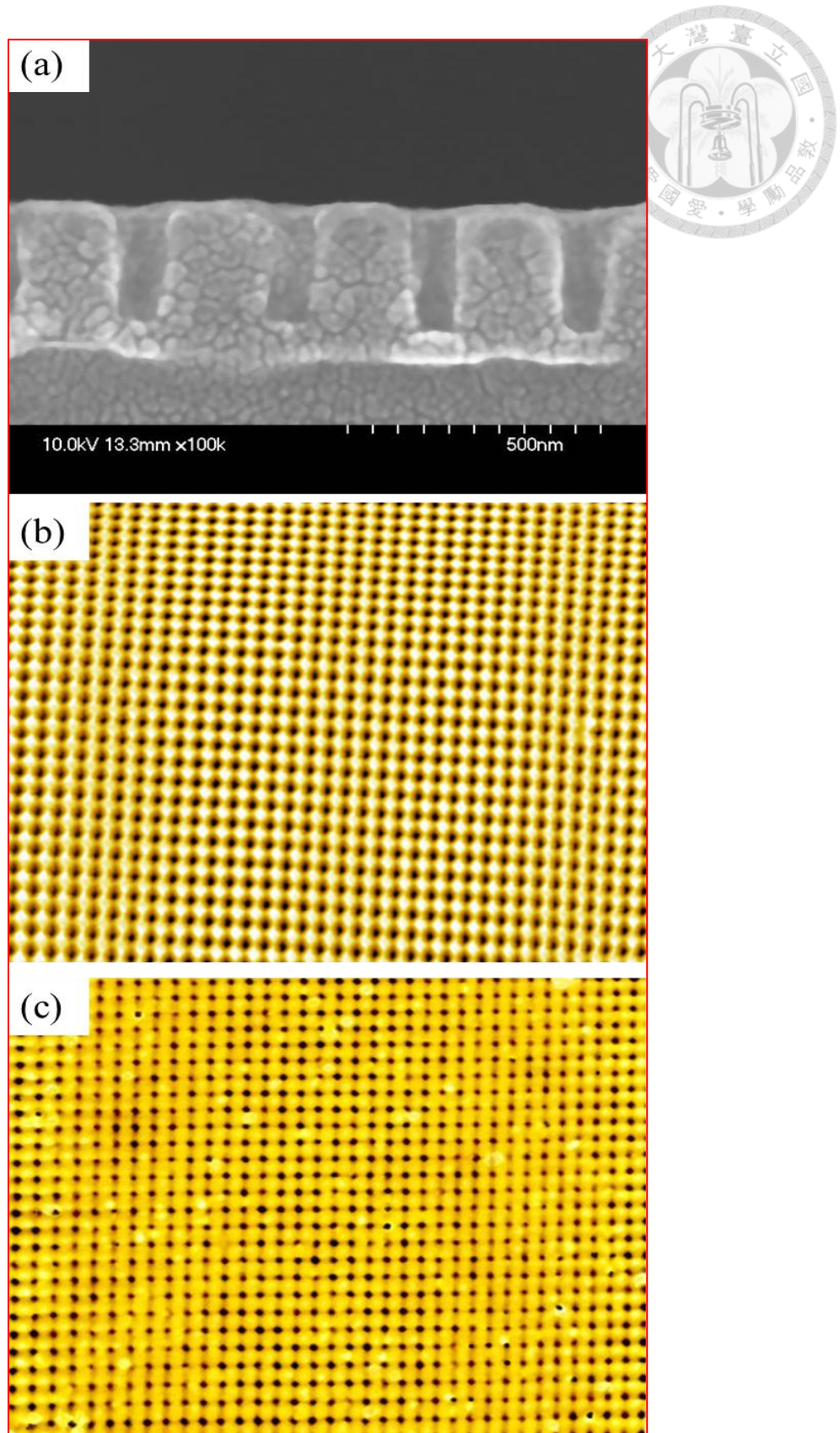


Fig. 3-6 (a) Cross-sectional SEM image of an ALD-covered mold. AFM images of (b) a new mold and (c) the same mold after more than 30 times for imprint use.



Fig. 3-7 The ALD machine we used in this work, which is located at NCTU.

3-2 Hot-embossing imprint process



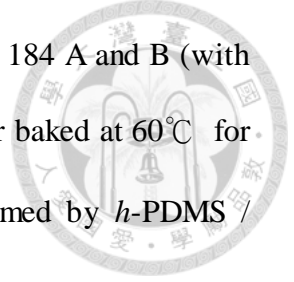
3-2-1 Fabrication of *h*-PDMS imprint stamp

PDMS was used as a stamp to transfer the pattern from the mold to the substrate in our hot-embossing NIL. However, the resolution of conventional PDMS (Sylgard® 184, © Dow Corning) stamp was not good enough for sub-100 nm NIL process [23]. The *h*-PDMS, a harder elastomer suitable for NIL was introduced. The stamp material was composed of vinylmethyl copolymers and hydrosilane components (agent A) and some additional glass fillers (agent B), and was found to be the best candidates for high-resolution NIL [24]. The *h*-PDMS was more fragile than the conventional PDMS, and easily broken during the hot embossing NIL process. To overcome this problem, we used a thick, flexible PDMS slab as a buffer layer to support the thin, stiff *h*-PDMS under layer. Such a hybrid PDMS imprint stamp which shown in Fig. 3-8 was easy to handle and released from the mold during preparation [25].

The fabrication process of an *h*-PDMS / PDMS hybrid imprint stamp is as follows:

- (1) The mixture of 2.5 g *vinylmethylsiloxane-dimethylsiloxane* copolymers (VDT-731, © Gelest), 0.0625 g *1,3,5,7-tetramethyl-teravinyl-cyclotetrasiloxane* (SIT-7900, © Gelest), and 0.0125 g *platinum divinyldimethylhydrosiloxane* (479535 catalyst, © Sigma-Aldrich) has been stirred well and degased for 10 minutes.
- (2) Then 0.25 g *hydrosilane prepolymer* (HMS-301, © Gelest) has been added to the mixture.
- (3) The whole mixture has been stirred well again and been degased for 5 minutes.
- (4) The mixture of *h*-PDMS has been spun onto the patterned mold to form a 2 μm -thick *h*-PDMS layer. And then heated at 60°C for 30 minutes.

- (5) Then, conventional PDMS produced by the mixture of Sylgard 184 A and B (with a ratio as 10 to 1) was poured slowly onto *h*-PDMS layer. After baked at 60°C for 8 hours, we slowly demolded the stamp. The stamp was formed by *h*-PDMS / PDMS hybrid structure with periodic hole-array pattern.



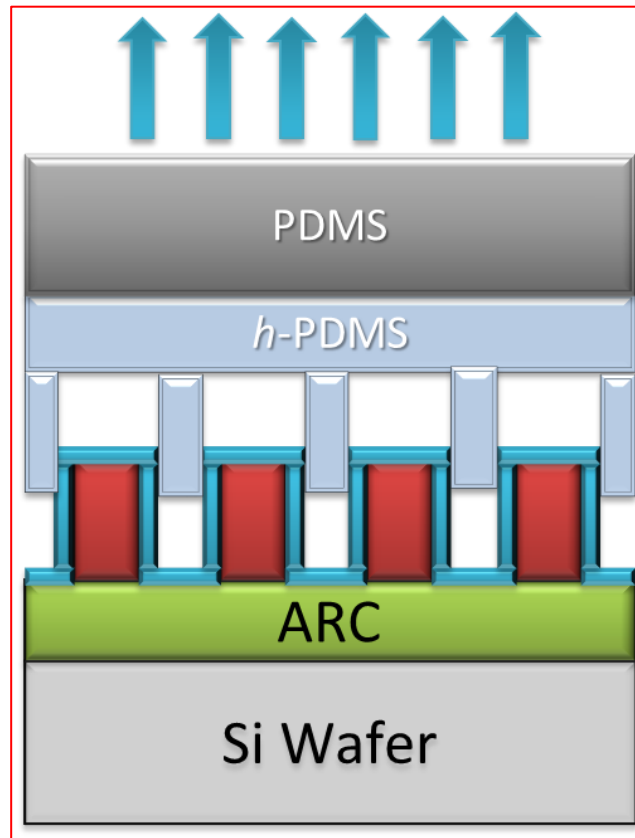


Fig. 3-8 An *h*-PDMS / PDMS hybrid stamp is demolding from the imprint mold.

3-2-2 Mold release agent

However, the large friction between *h*-PDMS and Al_2O_3 often caused structural damage of the stamp when peeled off from the mold. Such damages could be prevented by immersing the imprint mold in the toluene solution with *trichloro(3,3,3-trifluoropropyl)silane* (FPTS) as solute. The FPTS ($\text{CF}_3\text{CH}_2\text{CH}_2\text{SiCl}_3$) whose chemical structure formula has shown in Fig. 3-9 is one of the self-assembled monolayer (SAM) materials. SAM material is composed by a long alkyl group as the tail group and polar molecules stich on one side of the structure as the head group. Since the large Van der Waals force between the head group and the substrate, SAM can attach to the substrate very tightly.

To form the FPTS monolayer, the imprint mold should have to be soaked into 0.01M toluene solution with FPTS as solute for 12 hours, and then be rinsed by toluene. After baked the mold at 100°C for 1 hour, the mold can be successfully covered by FPTS monolayer.

Due to its fluorinated tail group, the FPTS monolayer reduces surface energy. So it could serve as an anti-adhesion monolayer [26]. Fig. 3-10 shows the effectiveness of FPTS on reducing pattern defects when demolding.

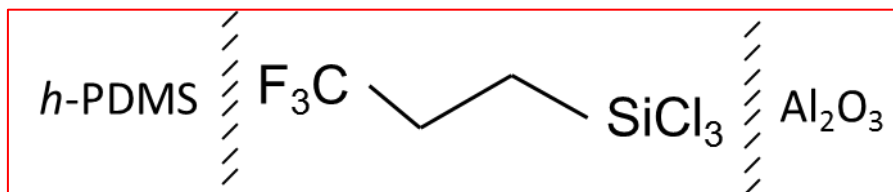


Fig. 3-9 Chemical structure formula of FPTS.

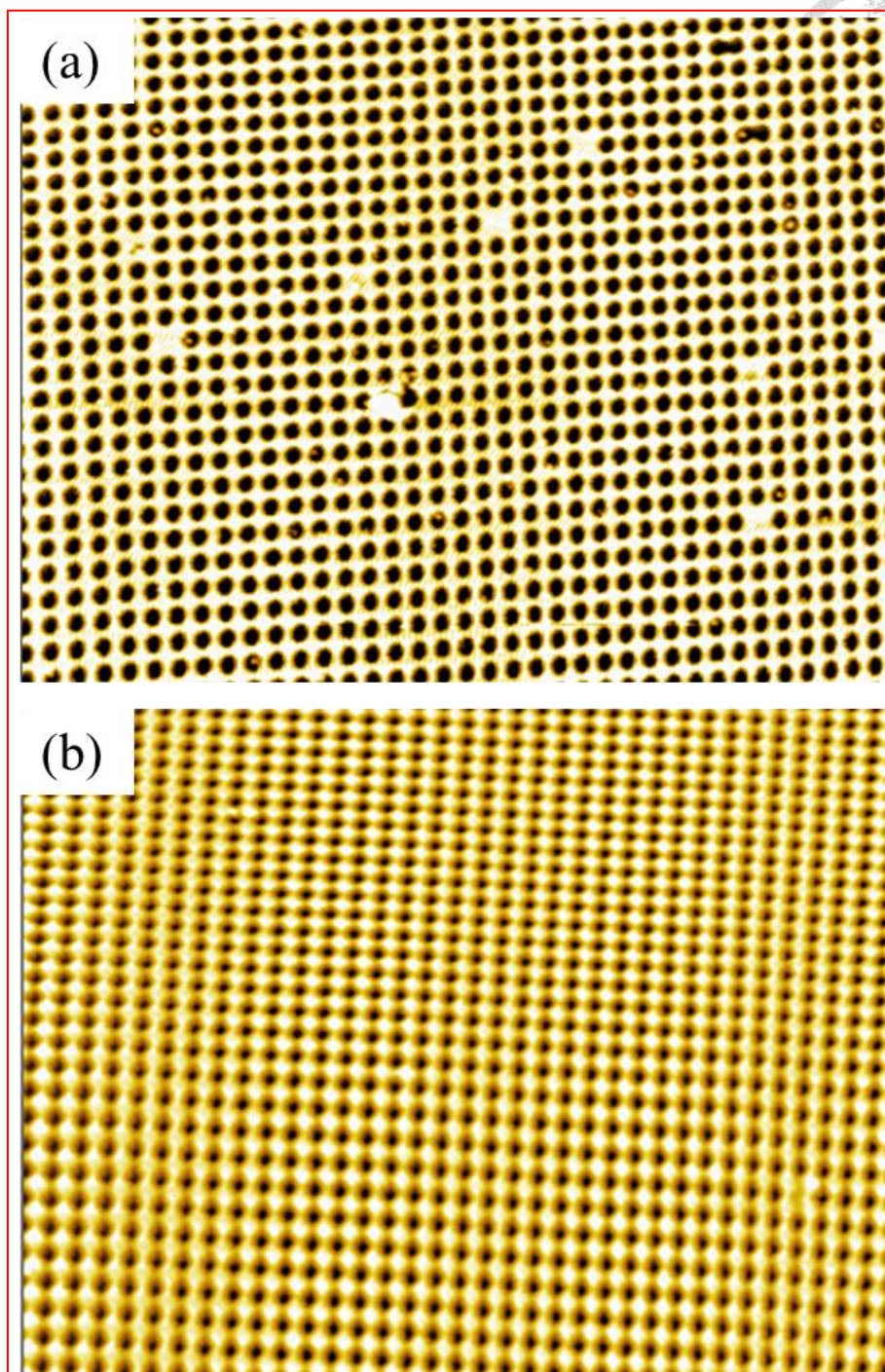


Fig. 3-10 AFM photos of h-PDMS stamp (a)without and (b)with FPTS applied.

3-3 Fabrication of Al nano meshes by wet-etching

After the hole-array pattern was transferred to ARC layer which coated on aluminum substrate, we use RIE to remove the residual ARC layer. Then we use the standard aluminum etchant ($\text{H}_3\text{PO}_4 : \text{HNO}_3 : \text{CH}_3\text{COOH} : \text{H}_2\text{O} = 50 : 2 : 10 : 9$) to etch the uncovered aluminum in order to fabricate Al nano meshes which shown in Fig. 3-11.

However, the aluminum might be oxidized by O_2 plasma during residual layer removing process. Since the aluminum etchant cannot etch aluminum-oxide, causing incomplete-etching. The incomplete-etching of Al may produce unwanted PVP column labeled in Fig. 3-12. This phenomenon will reduce the inject current of emitter-electrode, which is a negative factor for SCLT performance.

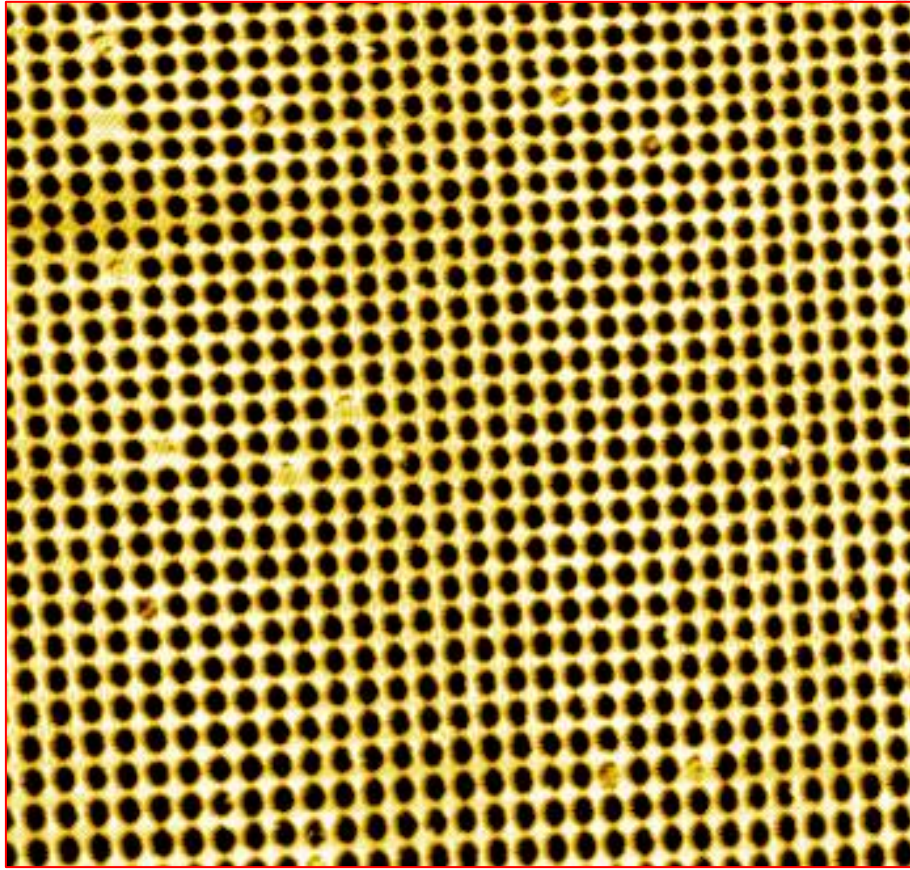


Fig. 3-11 AFM photo of Al meshes made by wet-etching.

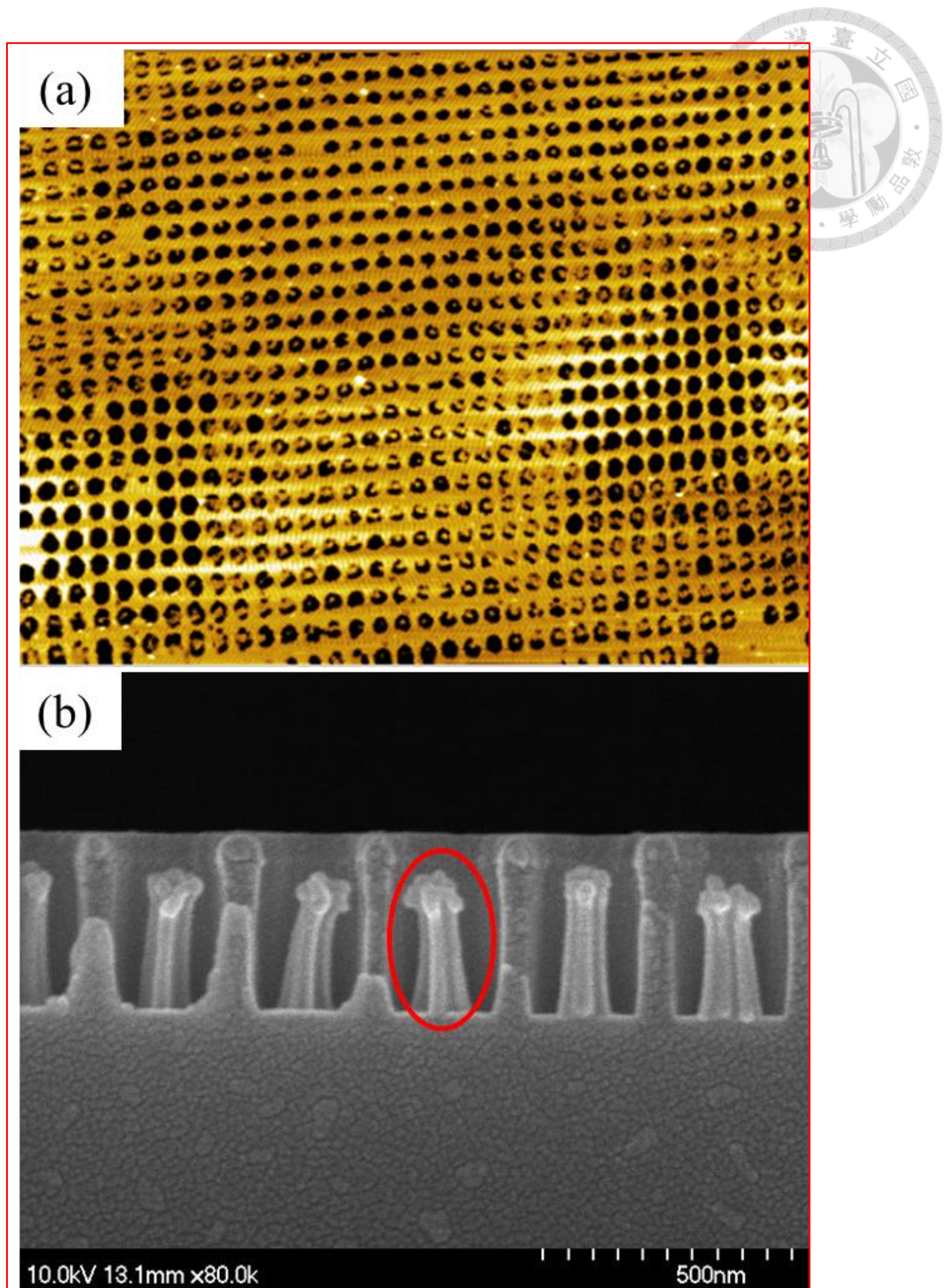



Fig. 3-12 (a)AFM photo of the incomplete-etched AL meshes.

(b) Unwanted PVP column (red circle) during PVP etching.

3-4 Measurement results



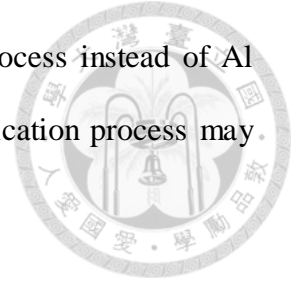
The impact of the application of ALD is positive to the better performance of SCLT. The electrical measurements of the second generation *imprinted* SCLTs have been shown in Fig. 3-13 and Fig. 3-14. Due to the aluminum wet etching process, the diameter of the vertical channel was increased to be around 150 nm. The collector current density (J_C) as a function of collector to emitter voltage (V_{CE}) is plotted in Fig. 3-13(b). When base to emitter voltage (V_{BE}) was -1.5 V and V_{CE} was -1.5 V, output current density as high as 4.35 mA/cm² could be obtained. Such a current density was 10 times larger than the first generation imprinted SCLT [15]. The ON/OFF current ratio is also plotted as a function of V_{CE} in Fig. 3-13(d). When V_{CE} was -0.5 V to -1 V, ON/OFF current ratio higher than 10000 was obtained and the off state current density was around $2\sim5\times10^{-4}$ mA/cm², which corresponded to 20-50 pA when the active region was 100 $\mu\text{m}\times100\text{ }\mu\text{m}$ [27]. In our previous reported first generation *imprinted* SCLT, ON/OFF ratio was 3000 and the output current was only 0.35 mA/cm². Here in this work, the 150 nm channel diameter successfully improved the transistor performance.

However, the repeatability of such a performance is not good enough. Fig. 3-14(b) shows high off state current due to high base leakage current labeled in Fig. 3-14(c). The ON/OFF current ratio was therefore down to lower than 1000.

There are several possible reasons of high leakage current:

- (1) The side products produced in wet-etching process may attach on Al surface, changing its work function and induce leakage between aluminum and P3HT.
- (2) Insulativity of PVP may change during wet-etching process, inducing leakage current at the interface of aluminum and PVP.
- (3) The unexpected large holes of Al mesh due to over-etch.

To eliminate these obstacles, we will introduce the lift-off process instead of Al wet-etching process in the next chapter. The wet-etching-free fabrication process may solve the problem of large leakage current.



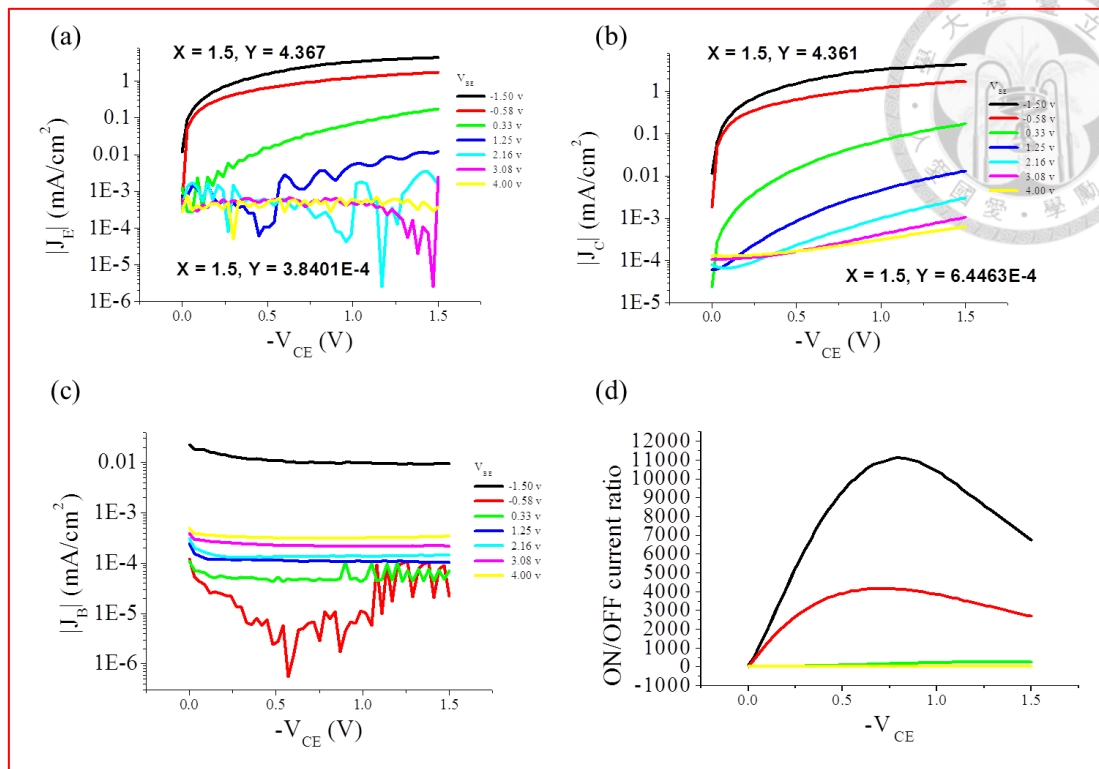


Fig. 3-13 (a) Emitter current, (b) output curve, (c) base current and (d) ON/OFF current ratio of an outstanding second generation SCLT.

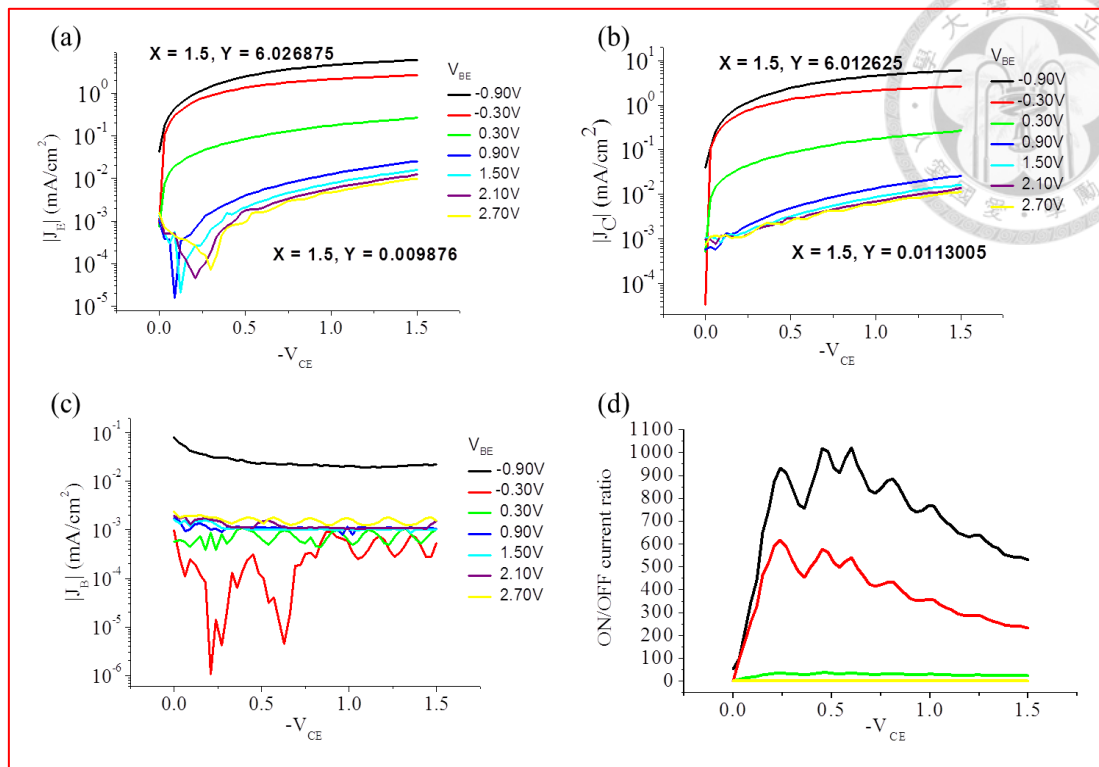


Fig. 3-14 (a) Emitter current, (b) output curve, (c) base current and (d) ON/OFF current ratio of a normal second generation SCLT.

Chapter 4 Fabrication of Nano Metal

Meshes by Strip-off Method



4-1 Advantages of lift-off method

Lift-off process in microstructuring technology is a method of creating structures (patterning) of a target material on the surface of a substrate using a sacrificial material (ex. photoresist). It is an additive technique as opposed to more traditional subtractive technique like etching. Lift-off method is applied to the cases where a direct etching of structural material would have undesirable effects on the layer below, just like our imprinted SCLTs. There are three basic factors to accomplish lift-off: (1) dissolvable sacrificial layer (2) good collimation of evaporator (3) good collimation of the sidewall of sacrificial structure. For example, our IL-generated PR grating structure has perpendicular sidewall (good collimation). And it is dissolvable in acetone. If we use a thermal evaporator with good collimation, we can easily get metal nano gratings which is shown in Fig. 4-1.

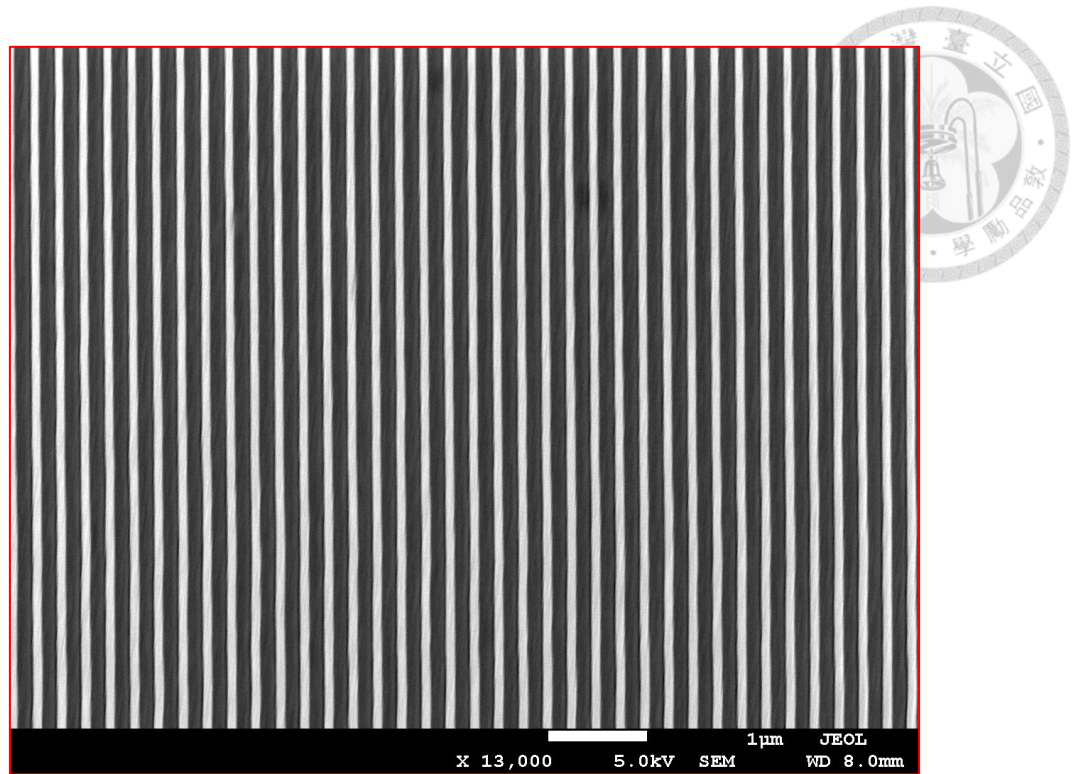


Fig. 4-1 Silver gratings fabricated by IL and lift-off method. (Period: 250 nm)

4-2 Dissolvable imprint resist

As we mentioned in last section, lift-off method needs a dissolvable sacrificial layer. However, the imprint resist we used in previous work, ARC, is only dissolvable in organic solvents like *propylene glycol monomethyl ether acetate* (PMGEA) which can also dissolve PVP. Since PVP is insoluble in the common solvent acetone, finding a new imprint resist which can be dissolved in acetone is crucial in lift-off process.

Here we introduce the thermoplastic imprint resist (mr-I 7020R, © micro resist technology GmbH) to replace ARC. The comparison sheet of ARC and mr-I 7020R is shown in Table 4-1.

The major difference between ARC and mr-I 7020R is the type. Since ARC is thermosetting, the stamp was put directly onto ARC layer without any bake. The ARC layer was then heated to 175°C after the pressure was applied. On the other hand, mr-I 7020R has the glass transition temperature (T_g) since it is thermoplastic. So it should be soft-baked after it has been spun onto the substrate. Then the pressure is applied after the imprint temperature was achieved. We can see this major difference in Fig. 4-2. Note that the 2-step imprint process labeled in Fig. 4-2(b) which has lower pressure during cooling step. Since the imprint resist becomes harder when temperature gets lower, structural damage of the imprint resist structure can be prevented by this procedure [28].



	ARC	mr-I 7020R
Type	Thermosetting	Thermoplastic
Imprint temperature	175°C	135°C
Imprint pressure	10 bar	25 bar
Resolution	Sub-100 nm	Sub-30 nm
Residue thickness	40~50 nm	<30 nm
Etch resistance	Low	High
Lift-off applicability	Negative	Positive

Table 4-1 Comparison sheet of ARC and mr-I 7020R.

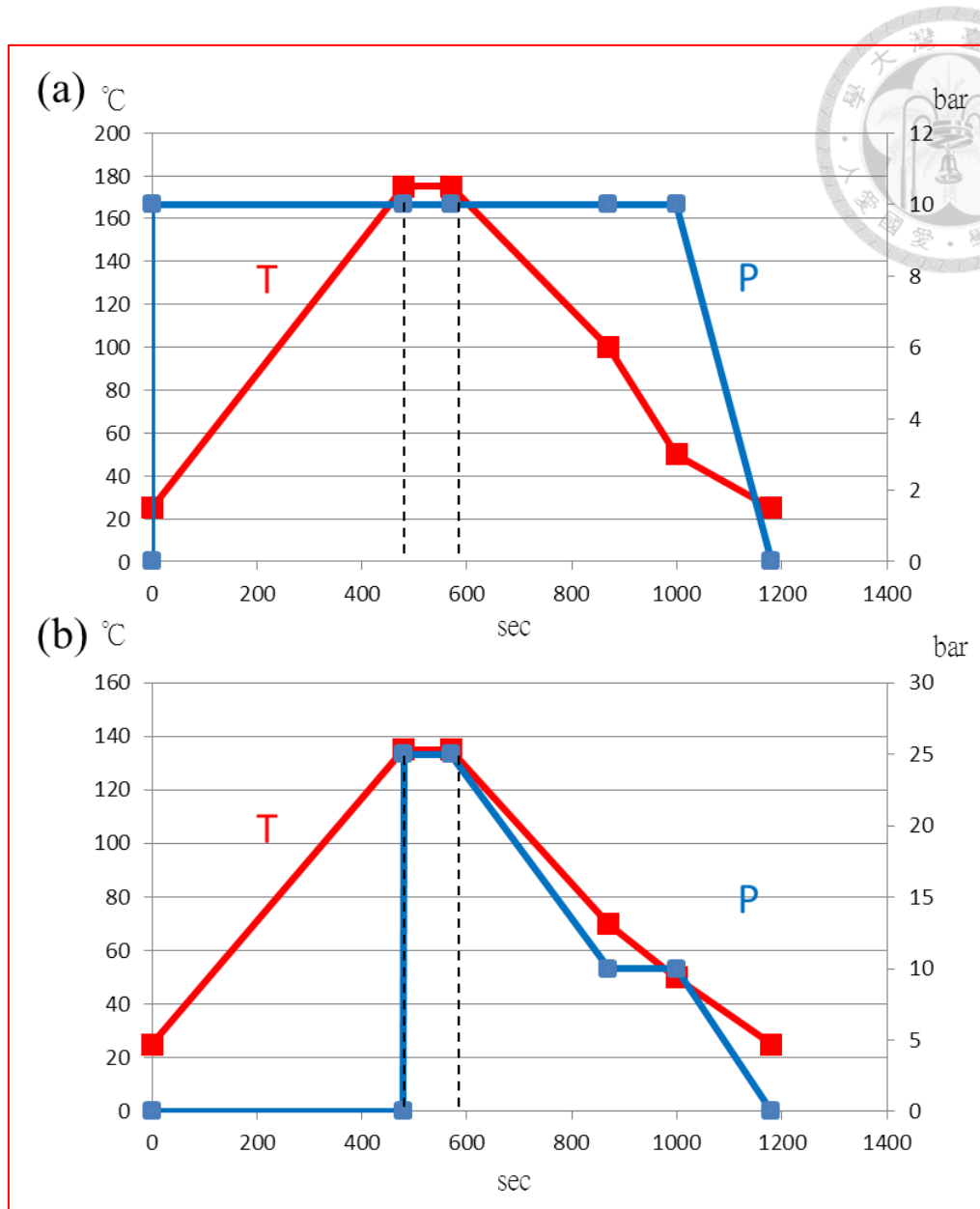
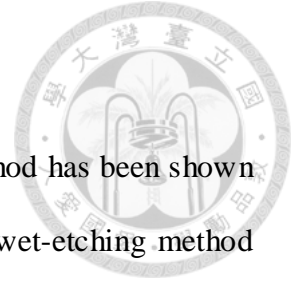


Fig. 4-2 Imprint process parameters of (a) ARC and (b) mr-I 7020R.

The redline represents the temperature and the blue line represents the pressure.

4-3 Fabrication process of lift-off method



The fabrication process of imprinted SCLT using lift-off method has been shown in Fig. 4-3. The major difference between lift-off method and the wet-etching method mentioned in Chapter 2 is the fabrication of aluminum mesh. After the residual layer of mr-I 7020R has been removed by RIE, the aluminum layer was directly deposited onto the PVP layer and the top of sacrificial resist structure. Then the resist will be dissolved by acetone, and the adhesive aluminum layer will be removed at the same time as Fig. 4-3(k) shows.

The result of lift-off method is shown in Fig. 4-4(b). Compared to aluminum meshes made by wet-etching method, the edge of each hole is smoother, and the size of hole is more uniform. However, there are some new problems of lift-off method. We will discuss them in the next section.

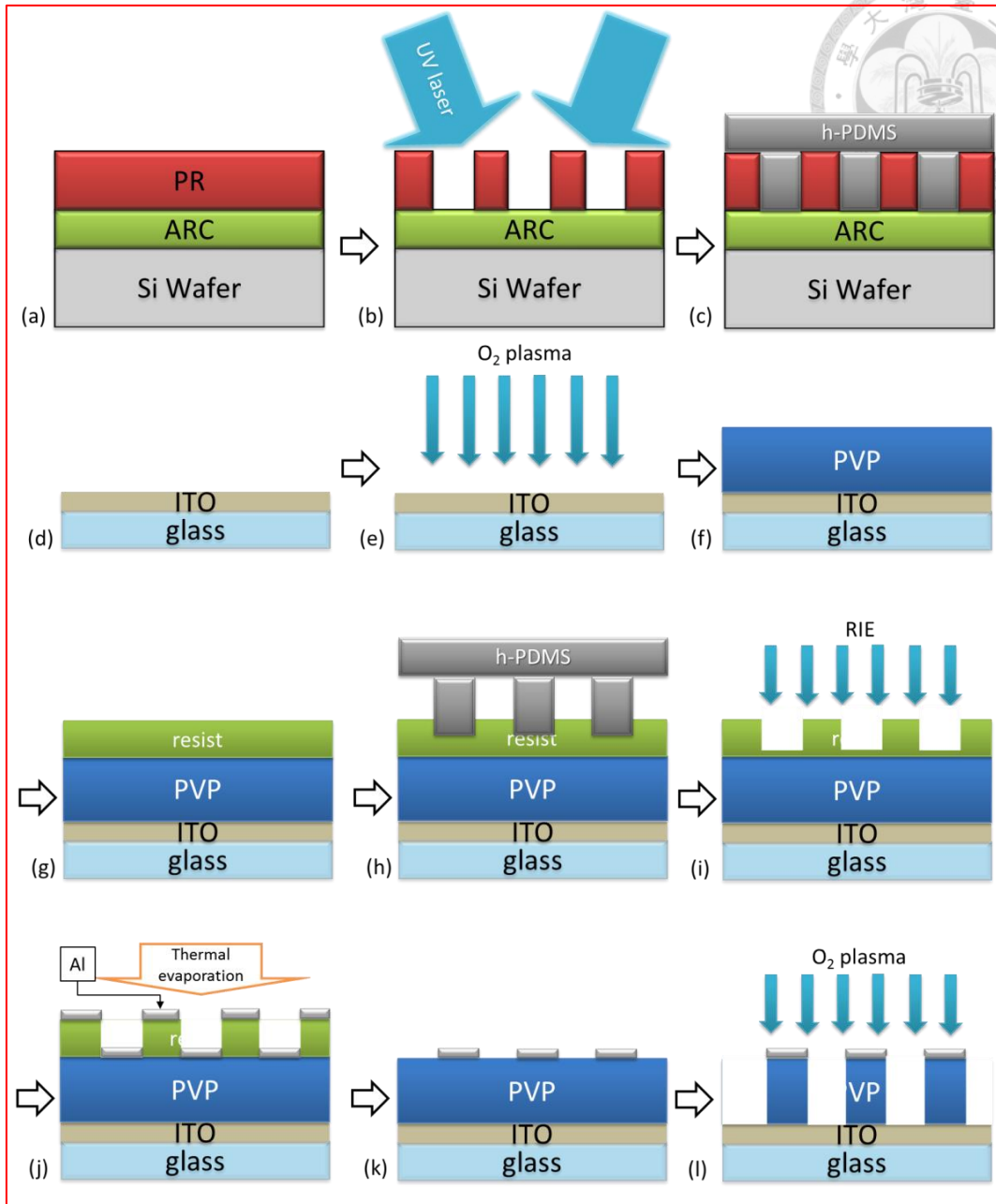


Fig. 4-3 Fabrication process of an imprinted SCLT using lift-off method.

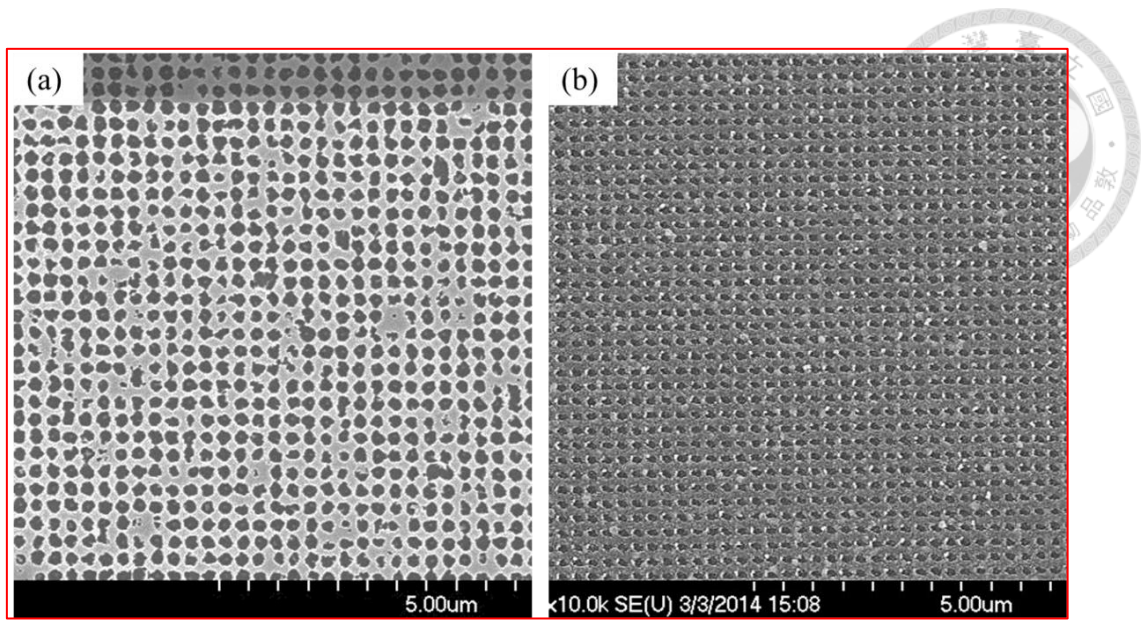


Fig. 4-4 Aluminum meshes made by (a) wet-etching and (b) lift-off.

4-4 Fabrication process of strip-off method



4-4-1 Problems of lift-off method

There are three major problems with lift-off method: (1) *retention*, (2) *ears*, and (3) *redeposition* [29].

Retention

This is the worst problem in the liftoff processes. If this problem occurs, unwanted parts of the metal layer will remain on the wafer. This can be caused by different situations. The resist below the parts that should have been lifted off could not have dissolved properly. Also, it is possible that the metal has adhered so tightly to the other metal parts which should have remained on the substrate.

Ears

When the metal is deposited, and it covers the sidewalls of the resist, "ears" can be formed. These are made of the metal along the sidewall which will be standing upwards from the surface. Also, it is possible that these ears will fall over on the surface, causing an unwanted shape on the substrate.

If the ears remain on the surface, the risk remains that these ears will go through different layers put on top of the wafer and they might cause unwanted connections of the device.

Redeposition

During the liftoff process it is possible that particles of metal will become reattached to the surface, at a random location. It is very difficult to remove

these particles after the wafer has dried.

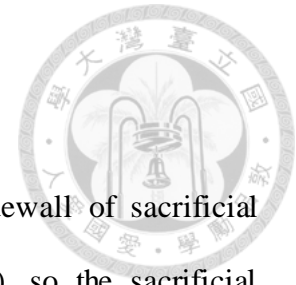


Fig. 4-5 shows some cases of failed lift-off examples. Sidewall of sacrificial structure has been covered by unwanted metal film (red circle), so the sacrificial structure could not have dissolved properly. Retention has occurred (4). On the other hand, the metal on top of the sacrificial structures could not be removed correctly in green circle area, so redeposition has occurred (2&3). Although the metal film adhered on the sidewall of sacrificial structure in blue circle might not obstruct the removal of inside sacrificial structure, the metal film remains and forms ear (1).

The thickness of metal layer has been determined by time length of deposition. The longer the time, the thicker the metal layer is. However, longer deposition time also causes thicker metal film adhered on the sidewall of sacrificial structures. Fig. 4-6 shows the lift-off results of our metal meshes with different metal thickness. The metal can be successfully lifted-off with 20 nm thickness. But with just 25 nm metal thickness, redeposition and ear have occurred. The worst case: retention has occurred with the situation which the metal thickness is 40 nm.

However, according to our previous work, the metal thickness has to be around 40 nm to endure the following PVP etching and perform good electrical characteristics. So we must find some way to help improve the yield of the thicker metal mesh.

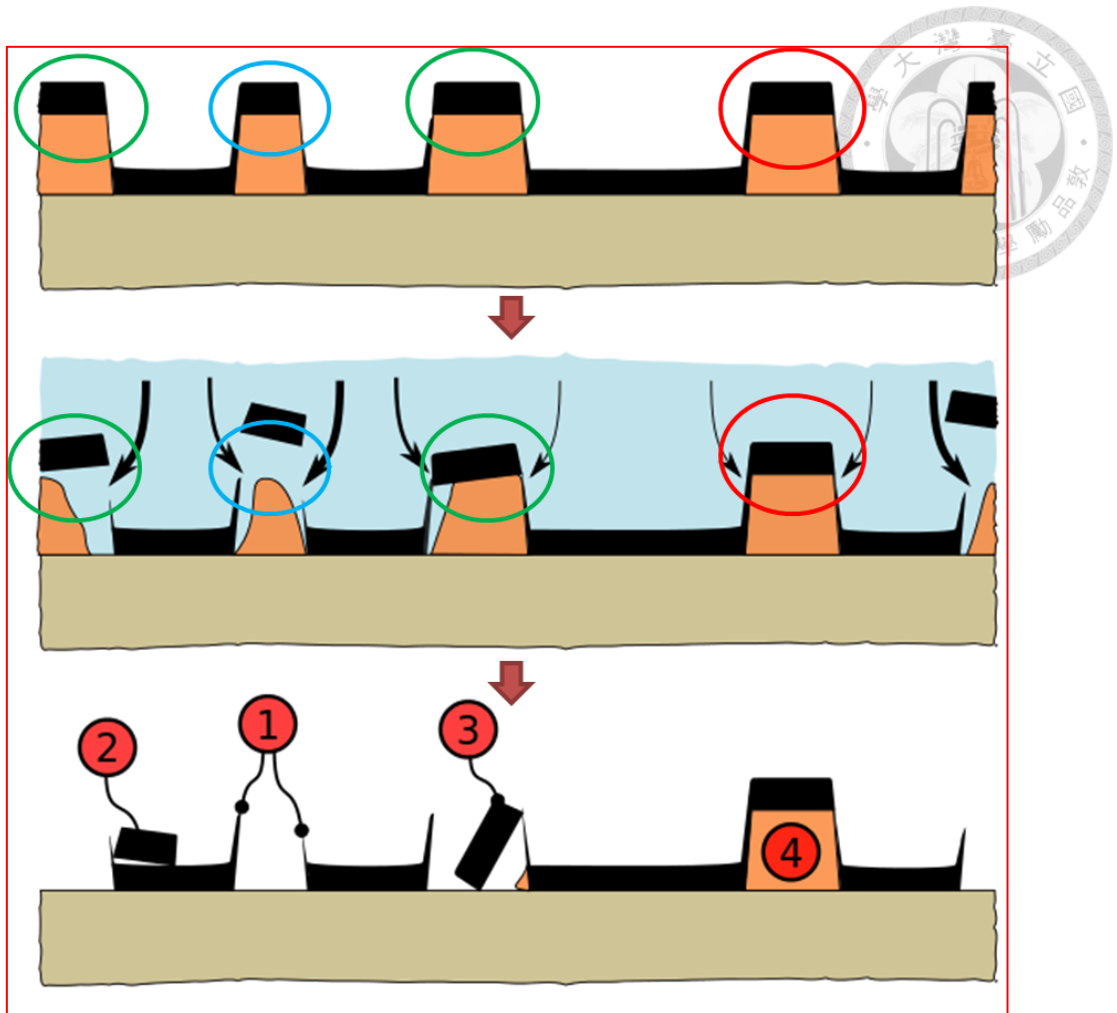


Fig. 4-5 Cases of failed lift-off processes.

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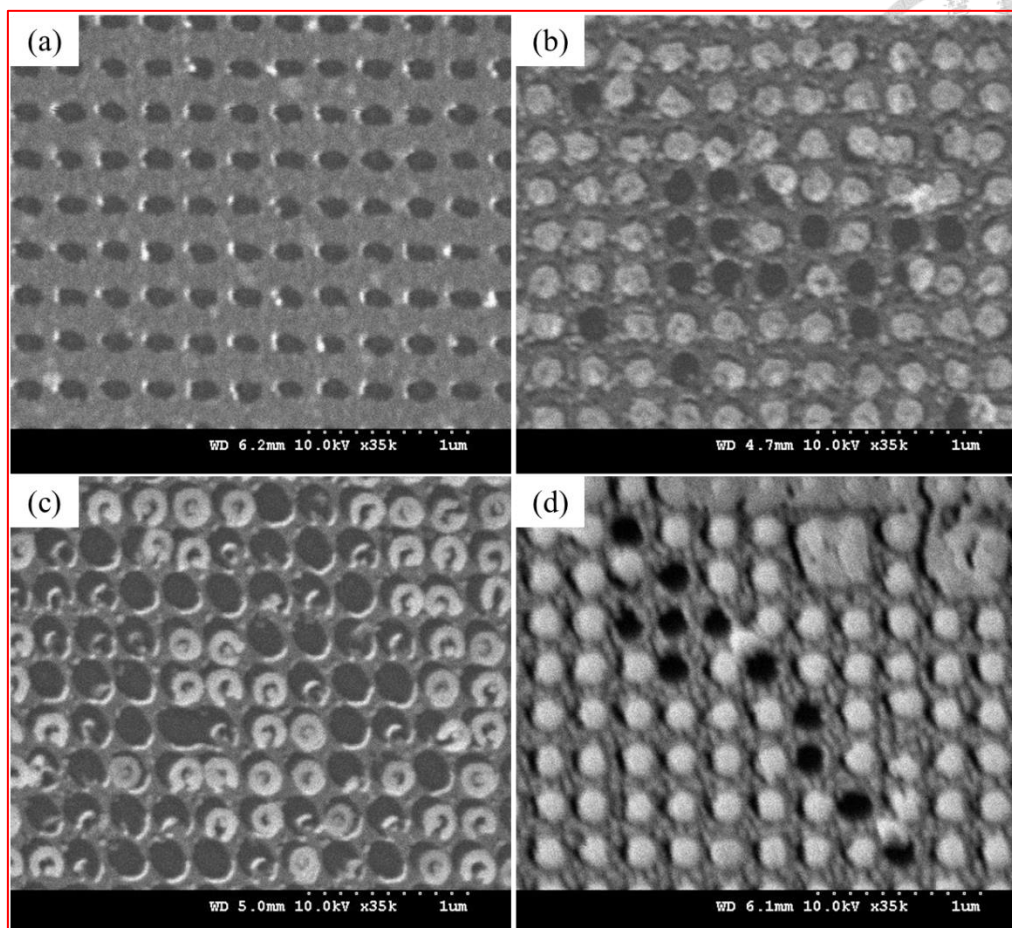


Fig. 4-6 Lift-off results of different thickness metal meshes. (a) 20 nm Ag.

(b) and (c) 25 nm Ag. (d) 40 nm Au.

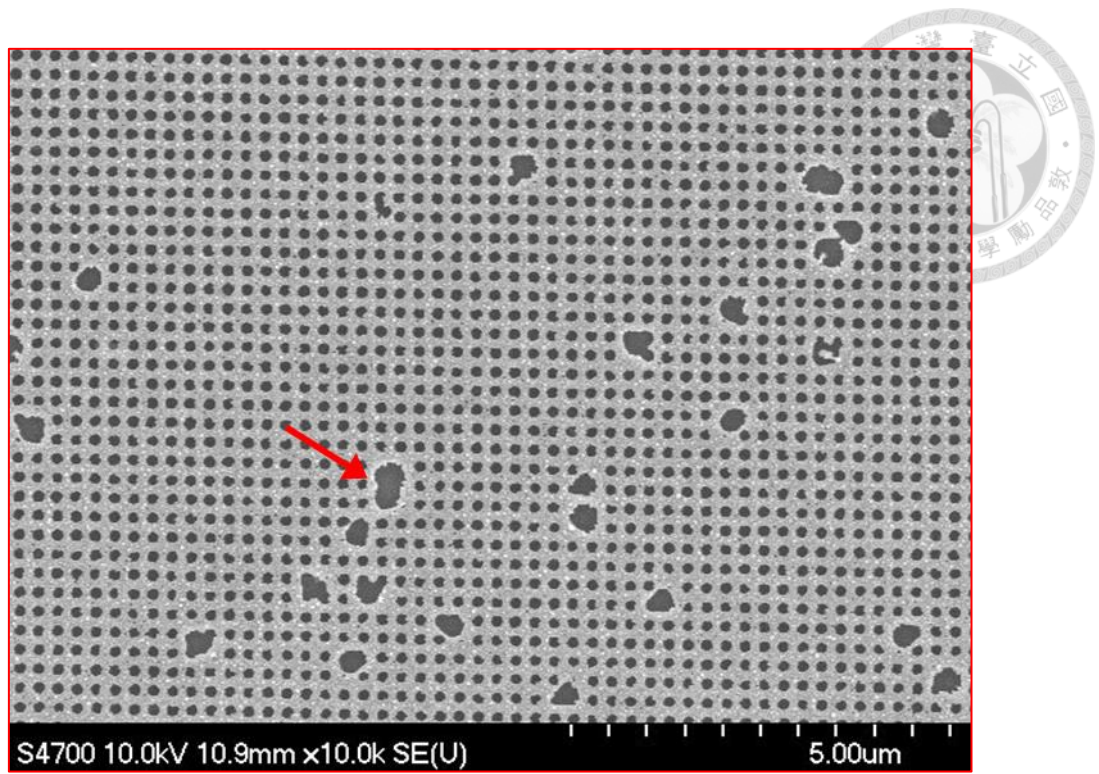


Fig. 4-7 The aluminum mesh with 20 nm thickness has been damaged by O_2 plasma after PVP etching process (red arrow).

4-4-2 Tilted evaporation of SiO caps

Using supersonic vibration during lift-off process can help the unwanted metal parts to be removed. However, it might also induce damages to the nano-scale metal mesh. A better solution is using undercut-shape sacrificial structure labeled in Fig. 4-8. The bigger upper part of sacrificial structure performs as a cap, preventing unwanted metal film from being deposited on the sidewall of sacrificial structure. However, the undercut-shape structure might be damaged during mold-releasing process after imprint because of its sidewall profile.

To solve this problem, we introduced the *tilted evaporation method* to produce the additional caps on top of the sacrificial structures after imprint process. The fabrication process is shown in Fig. 4-9. Unlike normal evaporation process, the sample has been tilted for an angle θ . Since the path of evaporated target material was blocked by the sacrificial structure, the target material could not deposit on the bottom of sacrificial structure, forming a “cap” on top of the structure.

Moreover, the cap labeled in Fig. 4-10 is made of SiO, which will not to be etched by O₂ plasma. So the sacrificial structure could maintain its height during residual layer removal process, making it easier to be lifted-off [30].

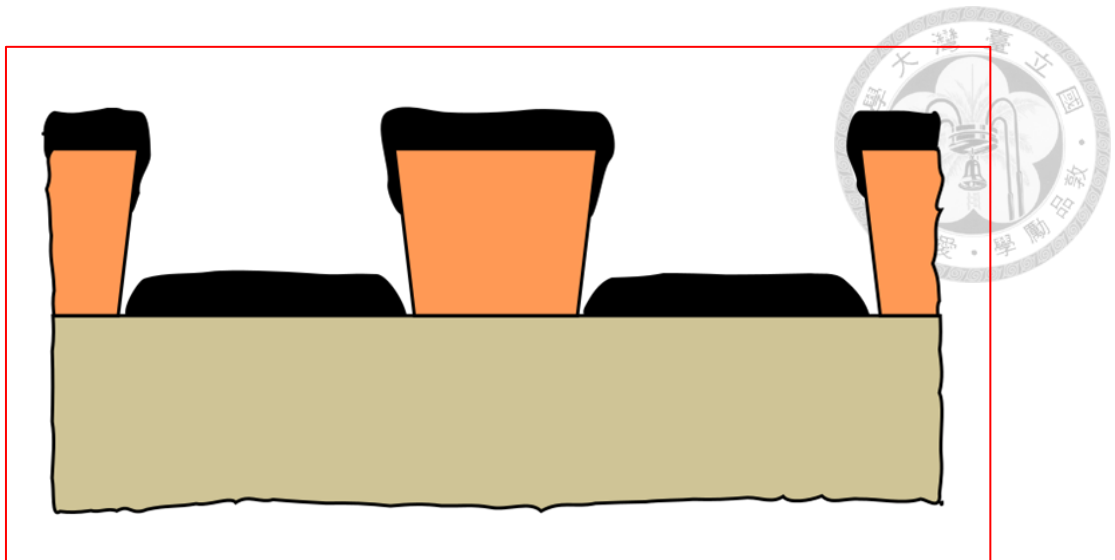


Fig. 4-8 The undercut-shape sacrificial structure for lift-off method.

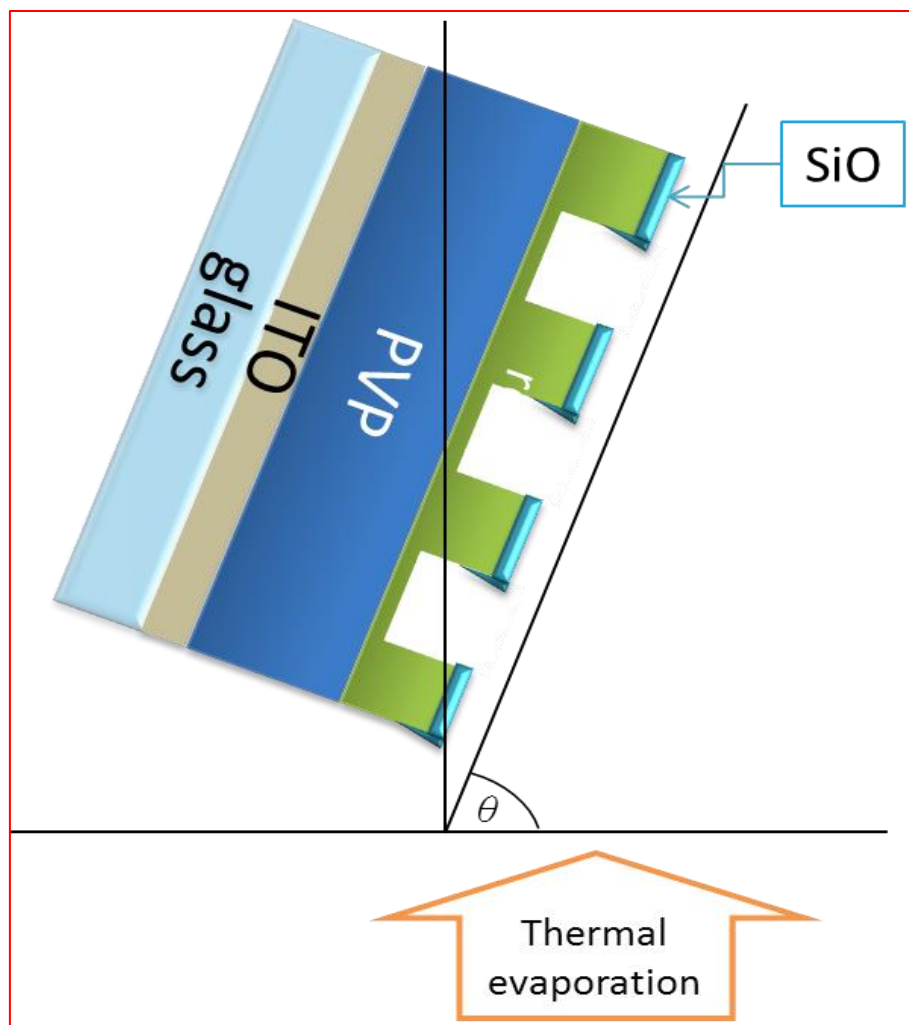


Fig. 4-9 Fabrication process of tiled evaporation.

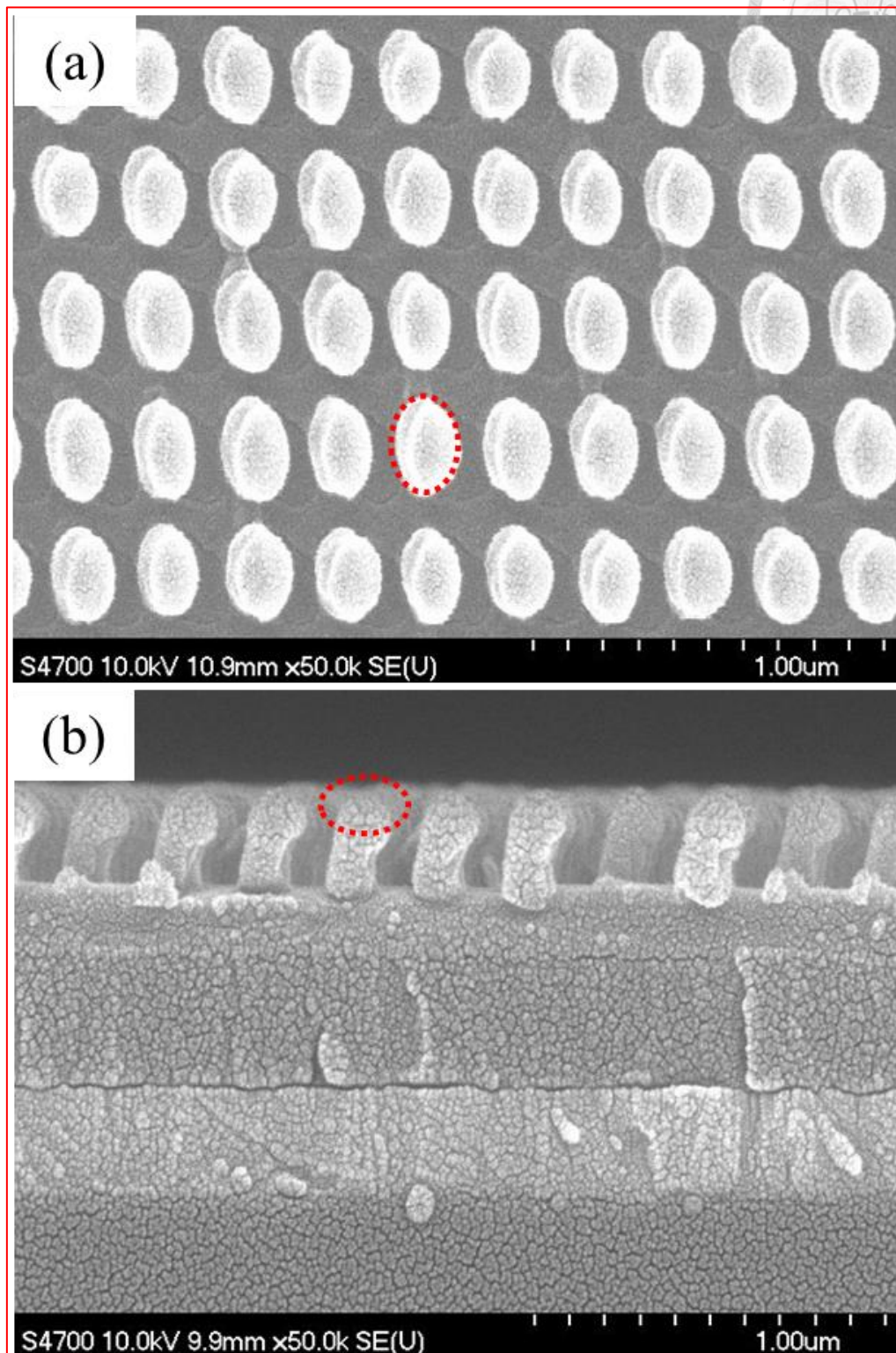


Fig. 4-10 SEM photos of (a) top and (b) side view of the SiO caps (red circle) on top of sacrificial structures (mr-I 7020R).

4-4-3 Strip-off method

Another way to improve the yield of the thicker metal mesh fabrication is introducing mechanical-assisted lift-off method. The *Carbon-Dioxide-Snow-Technique* uses conventional dry CO₂ wafer clean system to freeze the metal and sacrificial layer. Because the thermal expansion coefficients are different between these two materials, fractures can be produced on the metal film, and the mechanical strength of metal film decreases. After that, a CO₂ jet stream with specified incident angle removes the fractured sacrificial structure and adhered metal film. This solvent-free lift-off method can prevent redeposition and retention [31].

However, the Carbon-Dioxide-Snow-Technique also requires a dry CO₂ wafer clean system, which is an additional cost of the whole fabrication process. Here we introduce the *strip-off* method, another solvent-free lift-off method using a conventional adhesive tape.

The original idea of strip-off method comes from the mechanical exfoliation method of monolayer graphene [32]. In 2004, Andre Geim and his Ph.D. student Kostya Novoselov at University of Manchester extracted single-atom-thick crystallites from bulk graphite. They pulled graphene layers from graphite and transferred them onto thin SiO₂ on a silicon wafer in a process called either micromechanical cleavage or the scotch tape technique. The SiO₂ electrically isolated the graphene and weakly interacted with it, providing nearly charge-neutral graphene layers. The silicon beneath the SiO₂ could be used as a "back gate" electrode to vary the charge density in the graphene over a wide range. For their pioneering research on graphene, Geim and Novoselev received the 2010 Nobel Prize in Physics. In 2010, researchers in Korea announced that they improved this method for wafer-scale (3-inch), large-area monolayer graphene

fabrication [33]. So the mechanical exfoliation's ability of large-area fabrication has been approved.

The fabrication process of strip-off method is shown in Fig. 4-11. Note that metal film adheres on the sidewall of sacrificial structure labeled in Fig. 4-11(d). It will impede acetone to dissolve the sacrificial structures in normal lift-off process. The conventional adhesive tape (Scotch® , 3M) pasted on the upper metal film which labeled in Fig. 4-11(e) can solve this problem. Since the adhesive force between tape and upper metal film is stronger than the structural strength of sacrificial structure and adhered metal film, the structure has been broken when the tape has been peeled off.

There are two main factors that determine the success rate of lift-off process in our work: (1) collimation of the evaporator, (2) collimation of the sidewall of sacrificial structure. If the collimation of the evaporator or the sidewall is not good, there will be some metal thin film adhered on the structure's sidewall as labeled in Fig. 4-12. If the film thickness is not too thick, the supersonic vibration could make it broken and the sacrificial structure and unwanted metal could be successfully removed by acetone. However, if the metal layer became thicker, the adhered film also did. Then supersonic vibration could not make fractures on metal thin film anymore. So the target thickness of metal layer has been limited to 20 nm in our previous work.

On the other hand, with the help of the adhesive tape, strip-off method can be used to easily fabricate large-area Al mesh whose thickness is 40 nm. Now the Al mesh is thick enough to endure O₂ plasma during PVP etching process. The metal mesh suitable for the base-electrode of SCLT device can be fabricated by the solvent-free, strip-off method.

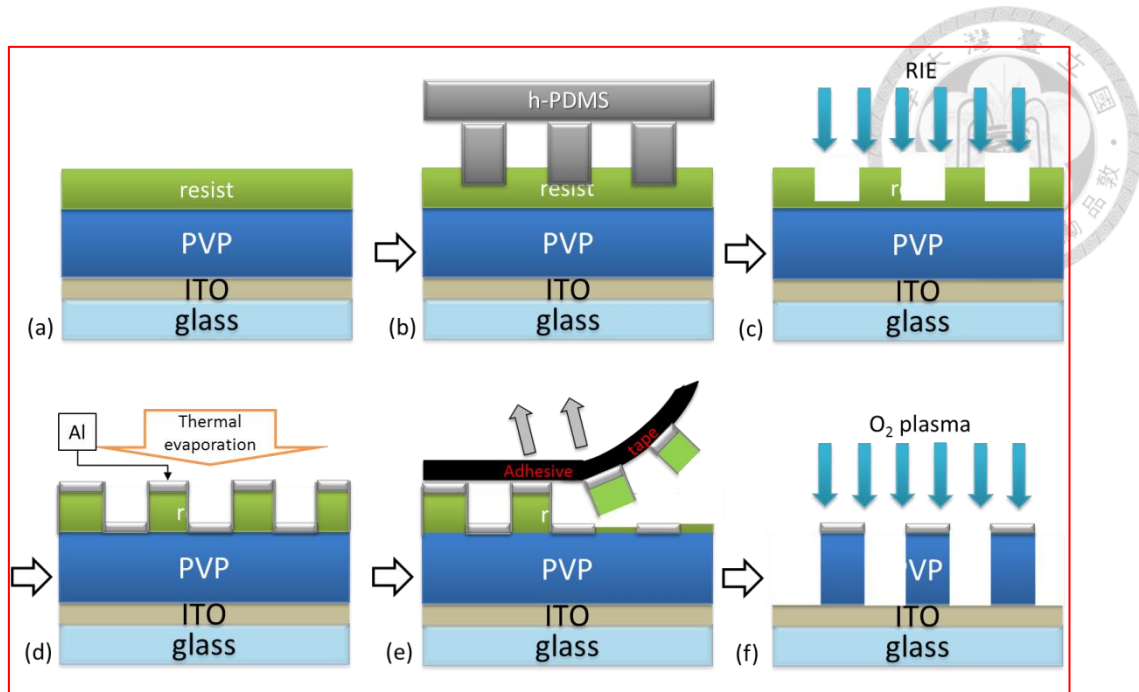


Fig. 4-11 Fabrication process of strip-off method.

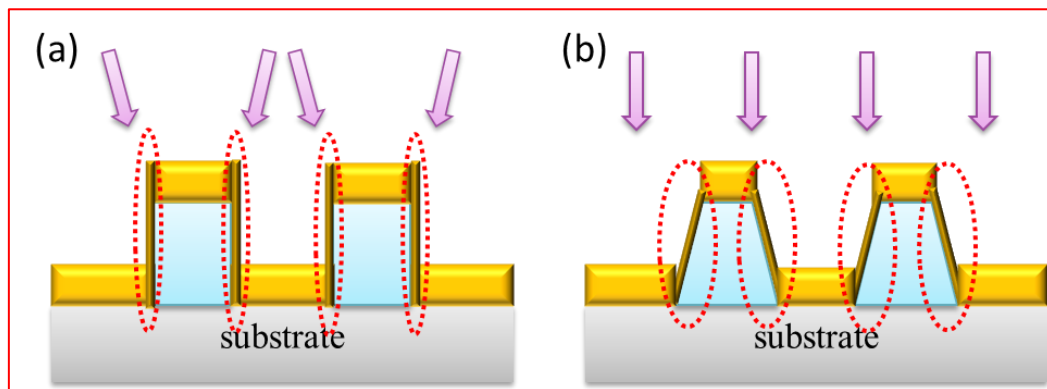


Fig. 4-12 (a) Bad collimation of evaporator and (b) bad collimation of sidewall of sacrificial structures.

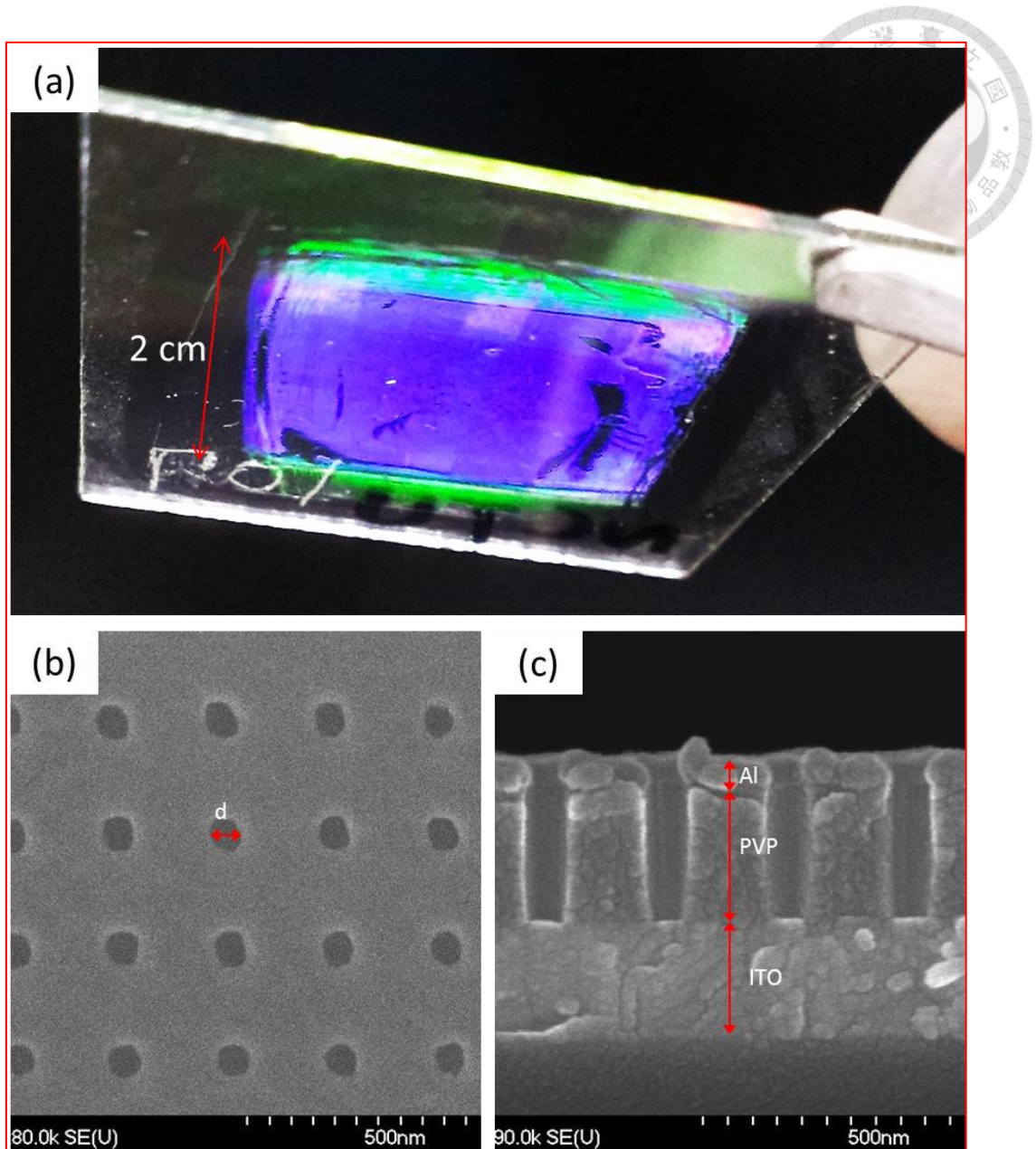


Fig. 4-13 (a) $2 \times 2 \text{ cm}^2$ Al mesh fabricated by strip-off. (b) Top view ($d = 80 \text{ nm}$) and (c) side view of the Al mesh after PVP etching process.

4-5 Measurement results



4-5-1 Leakage current at PVP-Al interface

With the help of strip-off method, we successfully fabricate sub-100 nm Al mesh with desired thickness as the base-electrode of SCLT. However, the electrical measurement results of the third generation SCLTs were below our expectations. Fig. 4-14 shows the cross-section of a third generation SCLT device and its electrical measurement results. The leakage current was not reduced as expected. Even worse, the leakage current was nearly two-order higher than the one of second generation SCLT. Since Fig. 4-14(c) shows that there is no obvious structural defect of the SCLT, we listed two possible reasons: (1) new imprint resist, (2) O₂ plasma etching process.

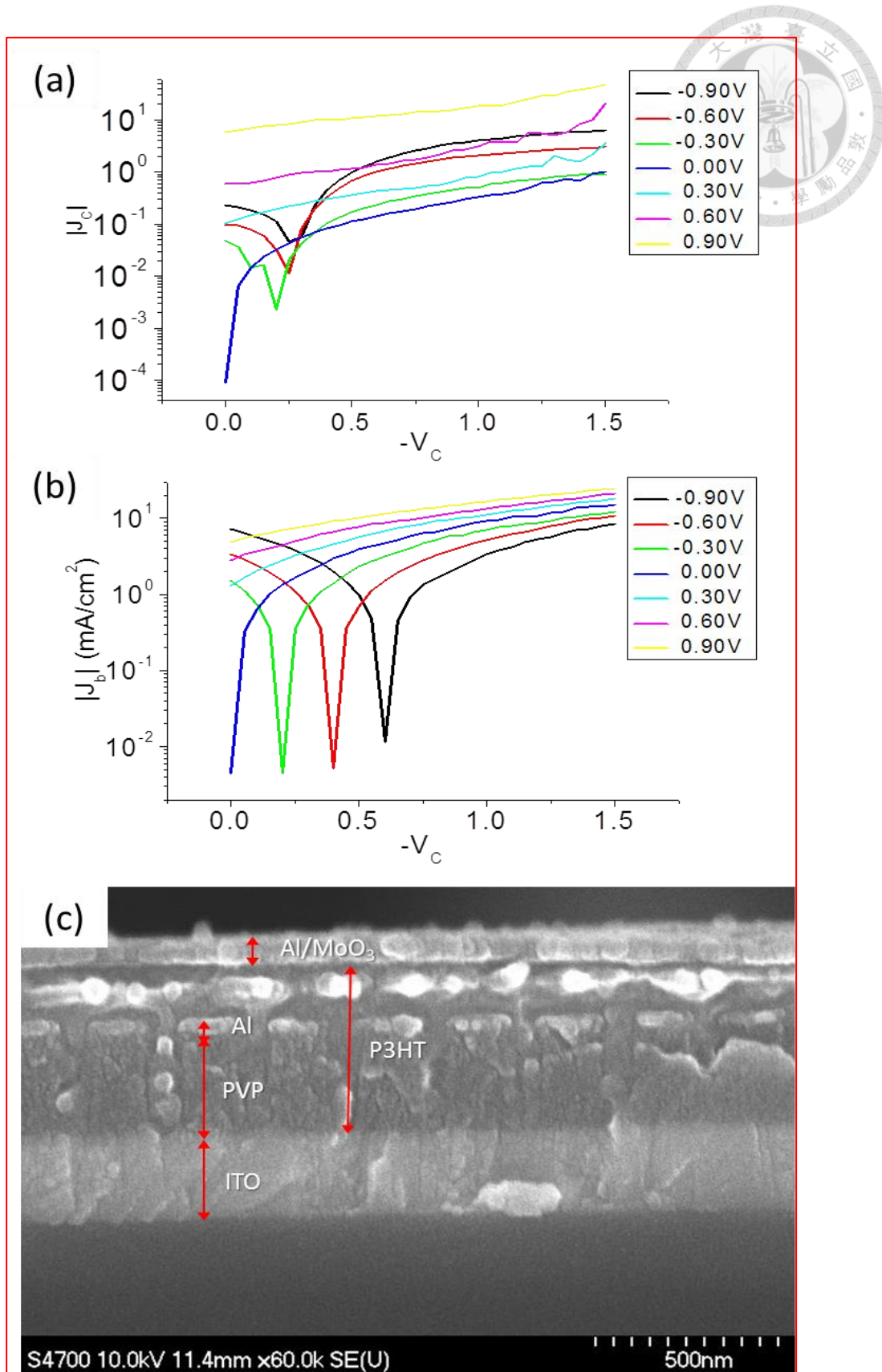


Fig. 4-14 (a) Output curve, (b) base current, and (c) cross-section photo of the third generation SCLT.

In the fabrication process of the second generation SCLT, the ARC was coated on the surface of aluminum layer, but the mr-I 7020R is now coated directly on the surface of PVP. The solvent of imprint resist might affect the insulativity of PVP. We test the leakage current of the original PVP, and PVP coated with mr-I 7020R (removed before aluminum evaporation). The results have shown in Fig. 4-15. We can see there is no obvious difference between two samples.

The other possible reason is the surface roughness of PVP surface after residual layer removal. In the fabrication process of the second generation SCLT, the plasma could not reach the PVP layer because the aluminum layer on its surface. However, the mr-I 7020R is directly coated onto the PVP surface. The O₂ plasma might etch the PVP surface during residual layer removal, increasing the surface roughness. Previous research results showed that rough PVP surface might induce larger leakage current [34]. To verify this assumption, we measured the leakage current of a bare PVP sample and a PVP sample with 100 W O₂ plasma treatment for 100 seconds. The results have shown in Fig. 4-16. It is clear to see that after the plasma etch, the leakage current increases nearly 100 times. So the ON/OFF current ratio could not be higher than our previous work.

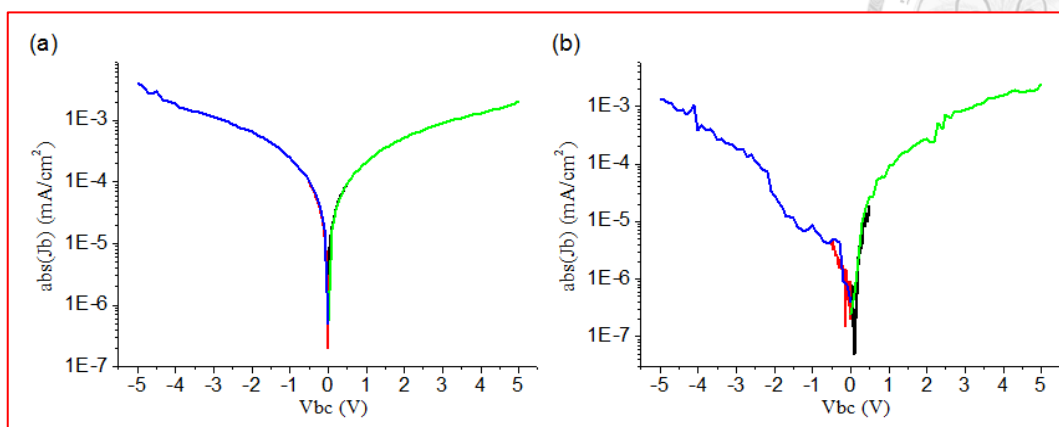


Fig. 4-15 Base current of (a) pure PVP and (b) PVP coated with mr-I 7020R.

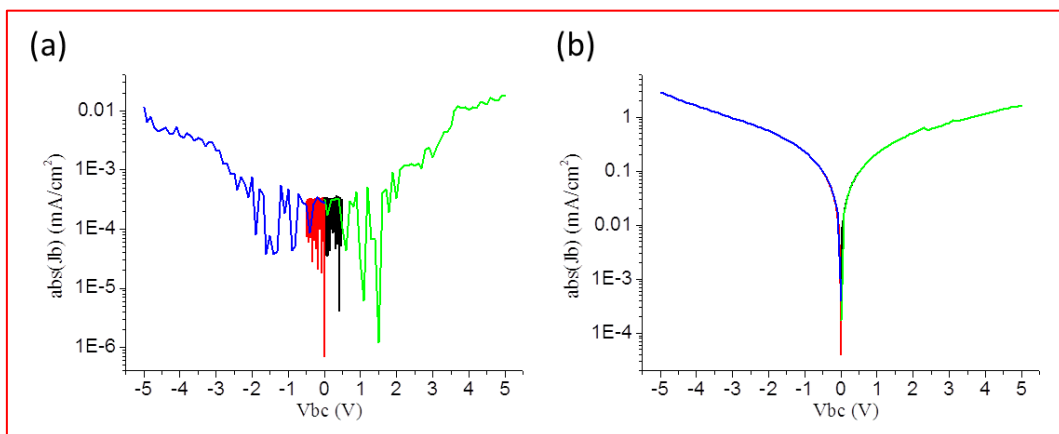
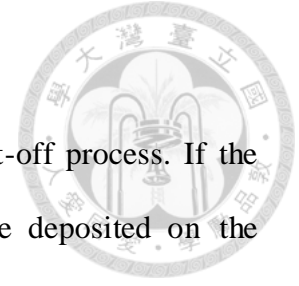


Fig. 4-15 Base current of (a) bare PVP and (b) PVP after O₂ plasma treatment.

4-5-2 Strip-off method without residue removal



The residual layer removal process is essential in normal lift-off process. If the residue has not been removed completely, the metal will not be deposited on the substrate properly. However, it is hard to determine the end point of residual layer removal because the PVP layer will also be etched by O₂ plasma. Luckily, the strip-off method gives us a choice for the solvent-free process. The modified fabrication process has shown in Fig. 4-16. Since we do not need solvable imprint resist anymore, we use the ARC as the imprint resist here again. The residual layer labeled in Fig. 4-16(b) has not been totally etched by plasma. Then the sample has been annealed at 200°C for 10 minutes. Since ARC is a thermosetting material, it could be adhered on PVP more tightly after annealing. On the other hand, mr-I 7020R is less adhesive to PVP than ARC. Fig. 4-17 shows the imprinted ARC rod-array patterns.

Fig. 4-18 shows SEM photos of aluminum meshes fabricated by modified strip-off method. Before the PVP etching process, the aluminum mesh is hardly to be recognized because there is nearly no height difference between aluminum mesh and residual ARC layer. But the aluminum mesh which labeled in Fig. 4-18(b) has been clearly revealed after the residual ARC and PVP were both etched by O₂ plasma.

The contribution of not-etching the residual layer is obvious. The leakage current which labeled in Fig. 4-19(b) is around 5×10^{-5} mA, much lower than the one labeled in Fig. 4-14(b). Therefore the ON/OFF current can reach over 70000.

To seek higher switching performance of our third generation SCLT, we introduce the self-assembled monolayer *octadecyltrichlorosilane* (OTS-18). OTS-18 molecules will attach on the sidewall of PVP tunnels [35]. The fill factor of P3HT in the tunnel can be increased with the help of OTS-18 [36]. The cross-section photo of an SAM-treated

SCLT is shown in Fig. 4-20. And its electrical measurement results is shown in Fig. 4-21. The output current has reached 4.65 mA/cm^2 , as good as our former record [37]. Since the leakage current has been lowered to $3 \times 10^{-5} \text{ mA/cm}^2$ with the help of our modified strip-off method, the ON/OFF current ratio is now over 10^5 , setting a new milestone of imprinted SCLT device.

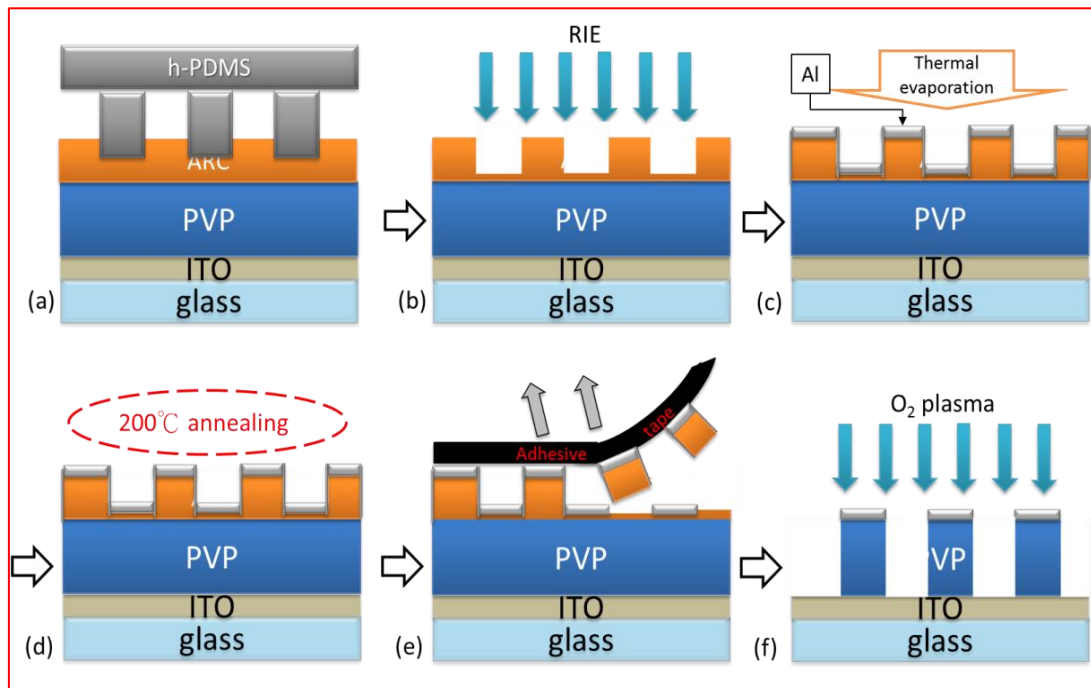


Fig. 4-16 Fabrication process of the modified strip-off method using ARC as the imprint resist.

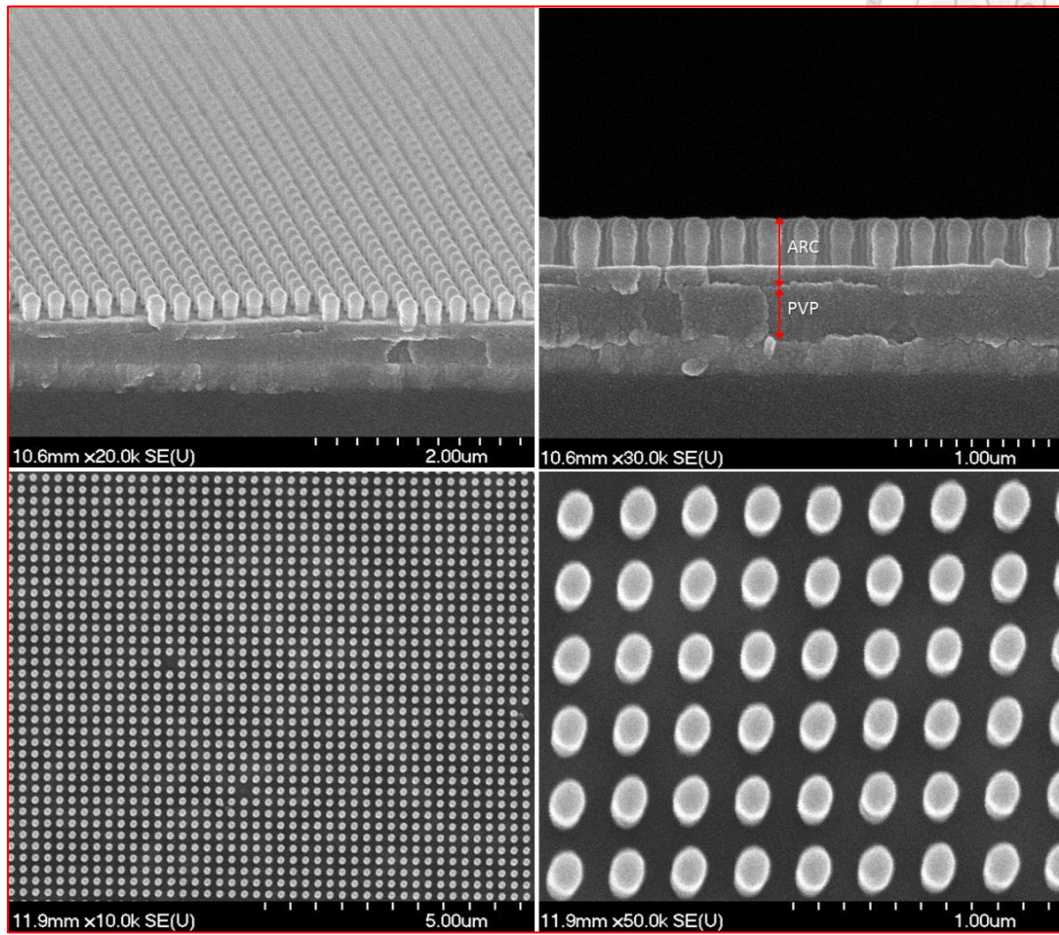


Fig. 4-17 SEM photos of imprinted ARC rod-array pattern.

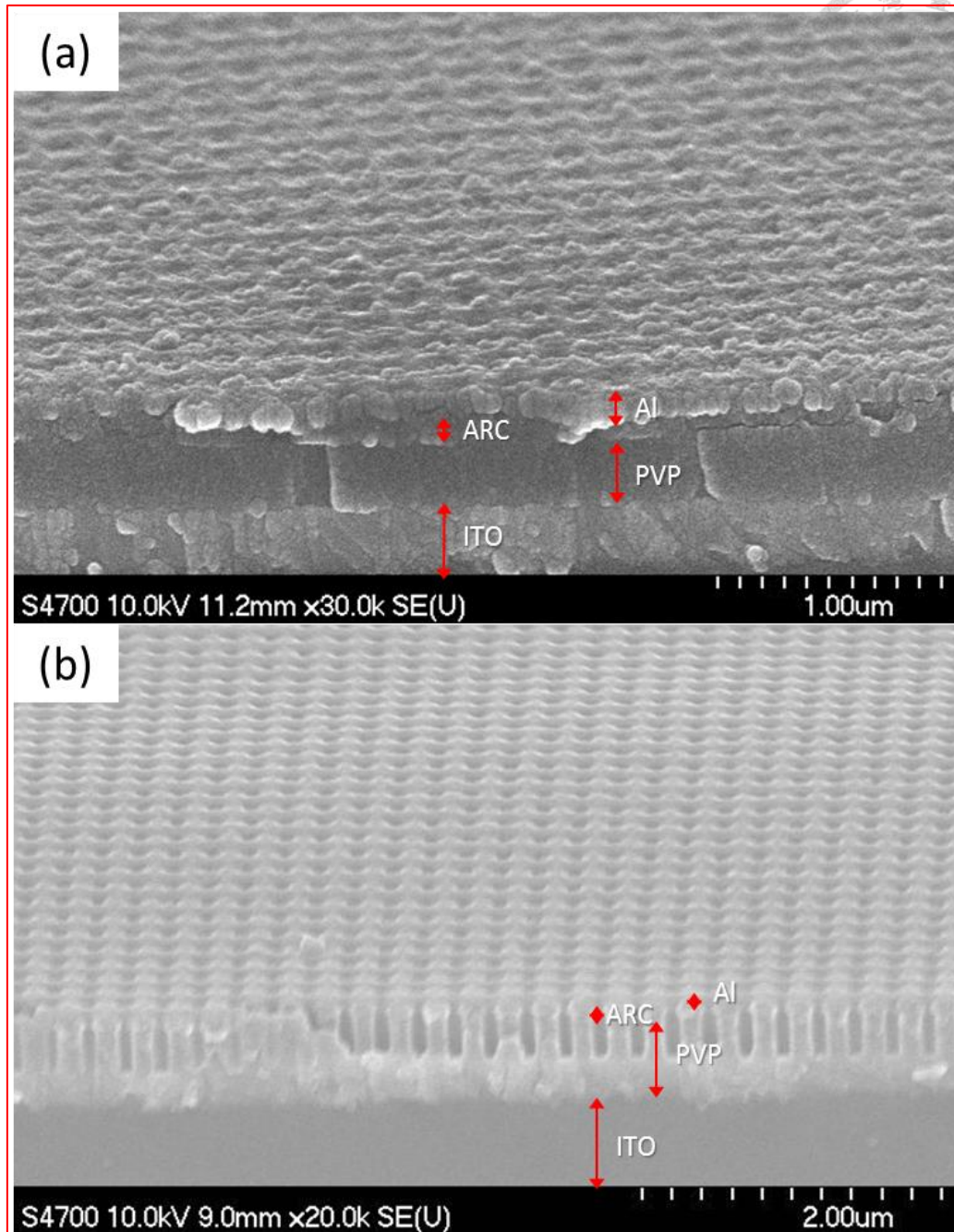


Fig. 4-18 SEM photos of Al mesh (a) before and (b) after PVP etching.

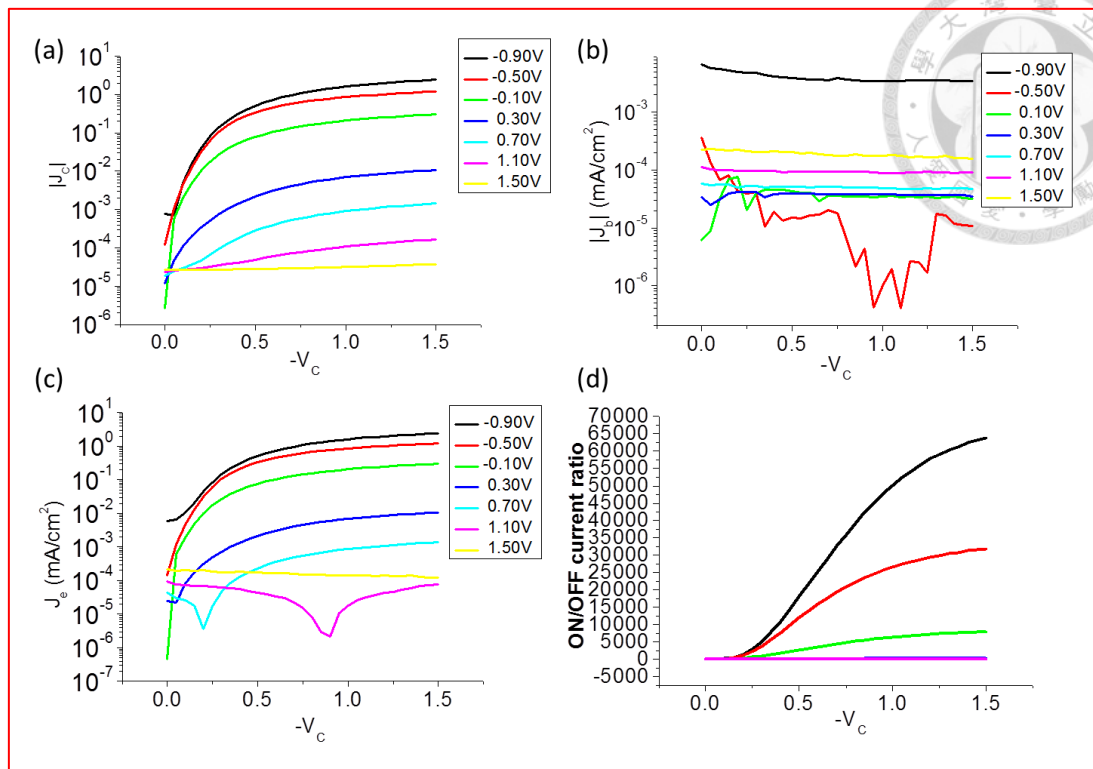


Fig. 4-19 Electrical measurement results of the third generation SCLT: (a) output curve (b) base current (c) emitter current and (d) ON/OFF current ratio.

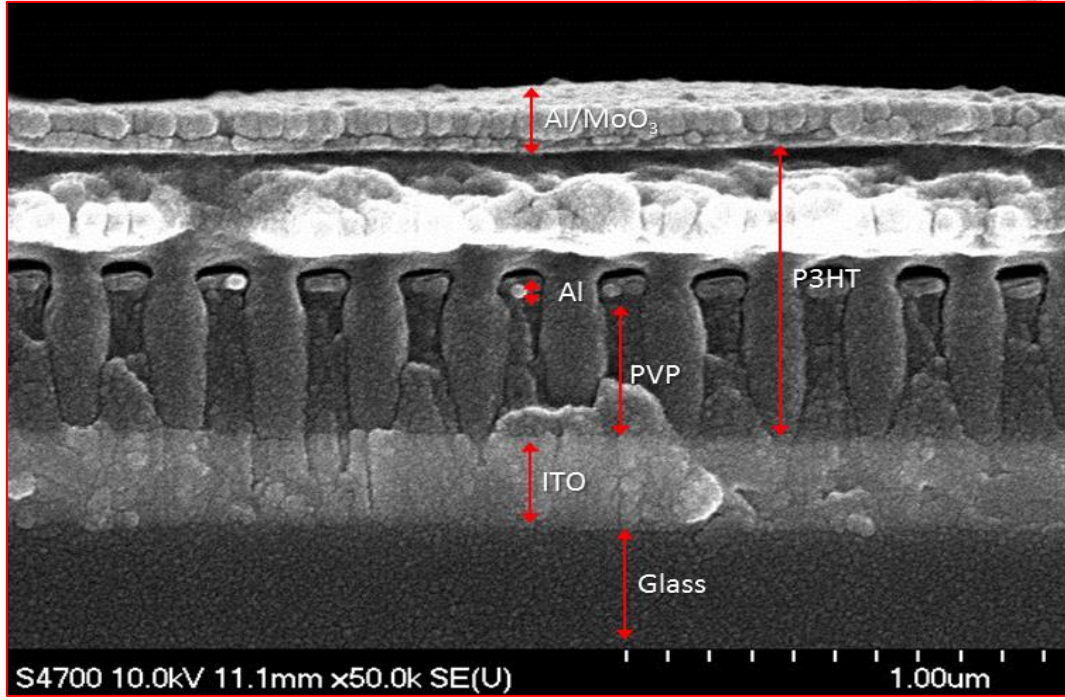


Fig. 4-20 Cross-section SEM photo of an SCLT with OTS-18 treatment.

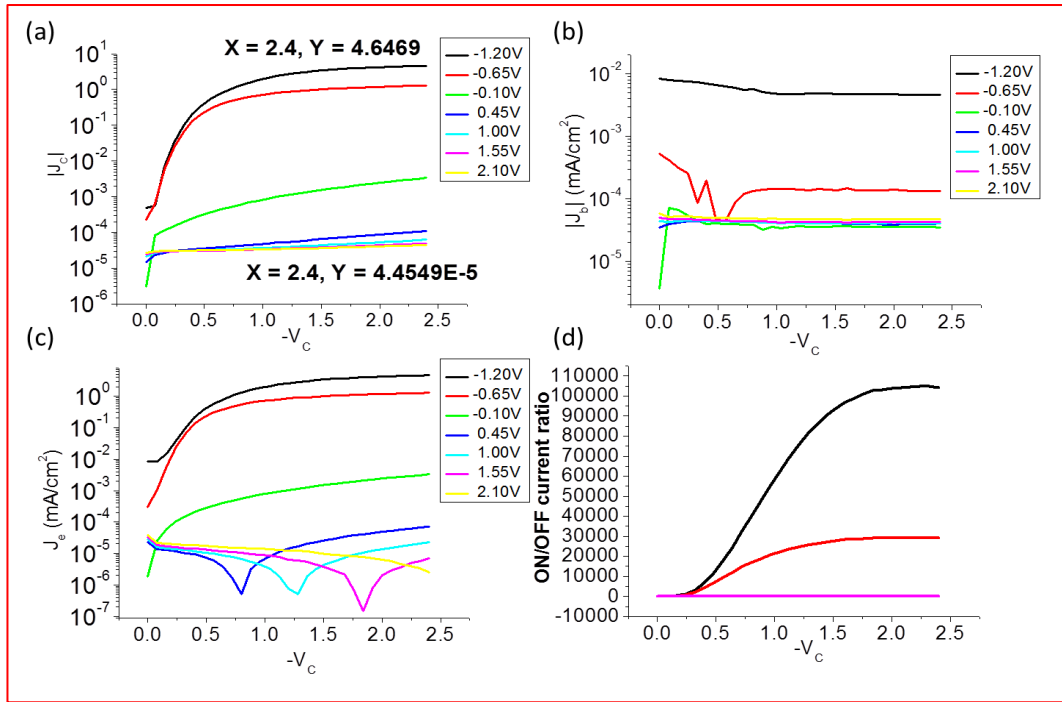
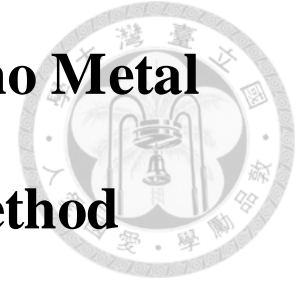


Fig. 4-21 Electrical measurement results of the third generation SCLT with OTS-18 treatment: (a) output curve (b) base current (c) emitter current (d) ON/OFF current ratio.

Chapter 5 Applications of Nano Metal

Structures Using Strip-off method



5-1 Nano metal gratings for optical applications

The polarized light has been applied in scientific studies of photo-chemical or photo-biological reactions recently [38]. The grating structure functions as a polarizer to select the transverse magnetic (TM) wave and reflect transverse electric (TE) wave in the wavelength range of 400-700 nm [38]. Previously, many efforts have focused on designing quarter-wave plates based on dielectric subwavelength gratings [39-46]. However, the design based on metallic subwavelength gratings is rare [47]. We cooperated with Prof. Si-Chen Lee's group from National Taiwan University to fabricate such gratings. By combining the IL, ALD, NIL, and strip-off method, large-area metal grating with designed period can be fabricated on a transparent substrate [48].

Fig. 5-1 shows the simulation result of 0th order transmission spectra for TE and TM waves with various slit widths. To obtain equal and highest transmissions for TE and TM waves, the slit width should be chosen to be 200 nm. However, the duty cycle of IL pattern is normally 1:1, which means the slit width and grating pitch are both 150 nm. With the help of ALD, the fine-tuning of grating pattern can be easily realized.

As Fig. 5-2 shows, the grating period of original IL pattern was 300 nm, and grating pitch was 150 nm. After ALD process, the pitch reduced to 100 nm, and period remained the same.

The metal assisted chemical etching (MacEtch) is a recently developed anisotropic

wet etching method that is capable of producing high aspect ratio semiconductor nanostructures from patterned metal film [49, 50]. The patterned gold thin film was used as the catalyst of MacEtch. The metal thin film was usually patterned by e-beam lithography (EBL) or anodic aluminum oxide (AAO) [51]. For larger-area fabrication and patterning on a curved surface, like a silicon fiber [52], NIL and strip-off method seems to be a better solution with low cost than other patterning methods. Fig. 5-4 shows the fabrication process of silicon fiber grating which made by using the strip-off method and MacEtch.

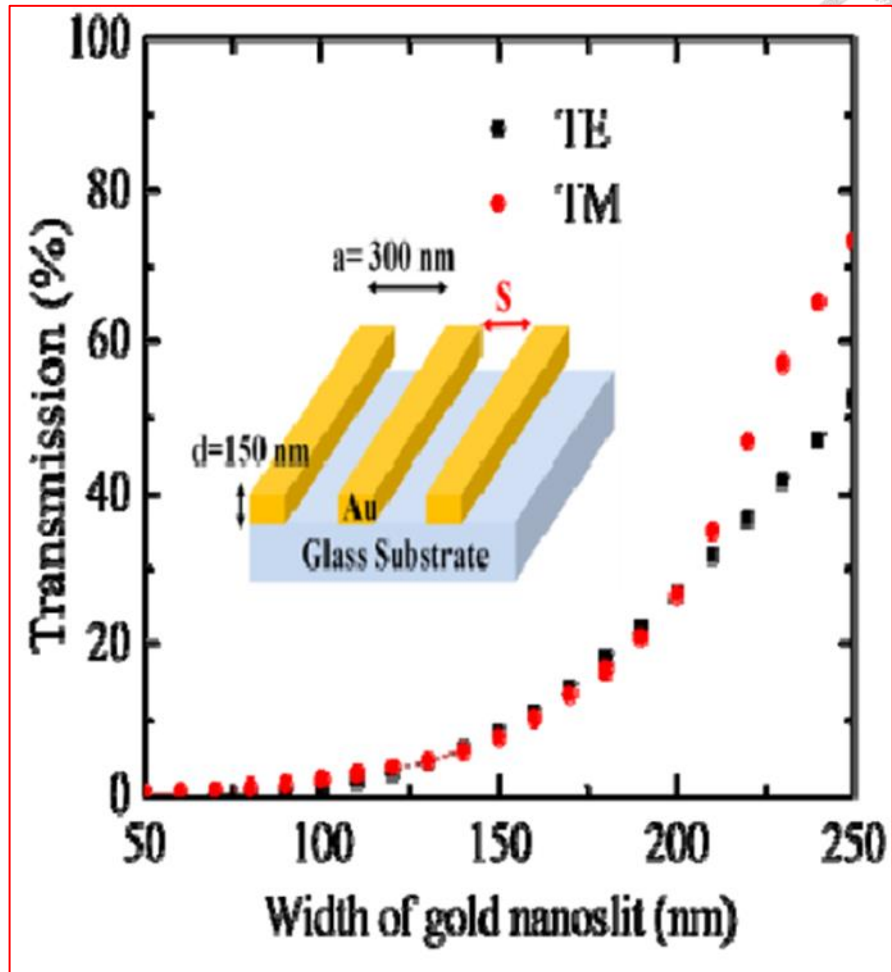


Fig. 5-1 The simulated 0th order transmission spectra for TE and TM waves with various slit width (grating period = 300 nm) [44].

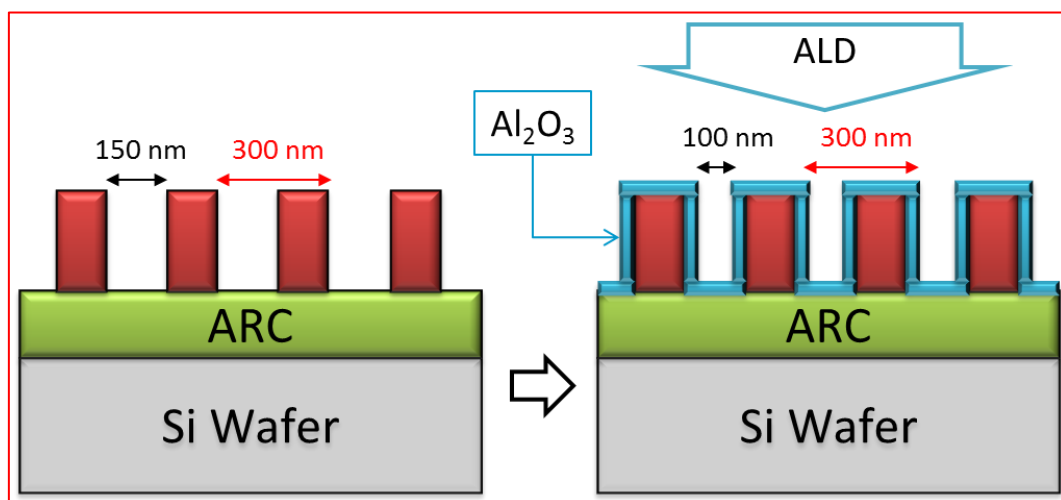


Fig. 5-2 The grating pattern has been fine-tuned by ALD.

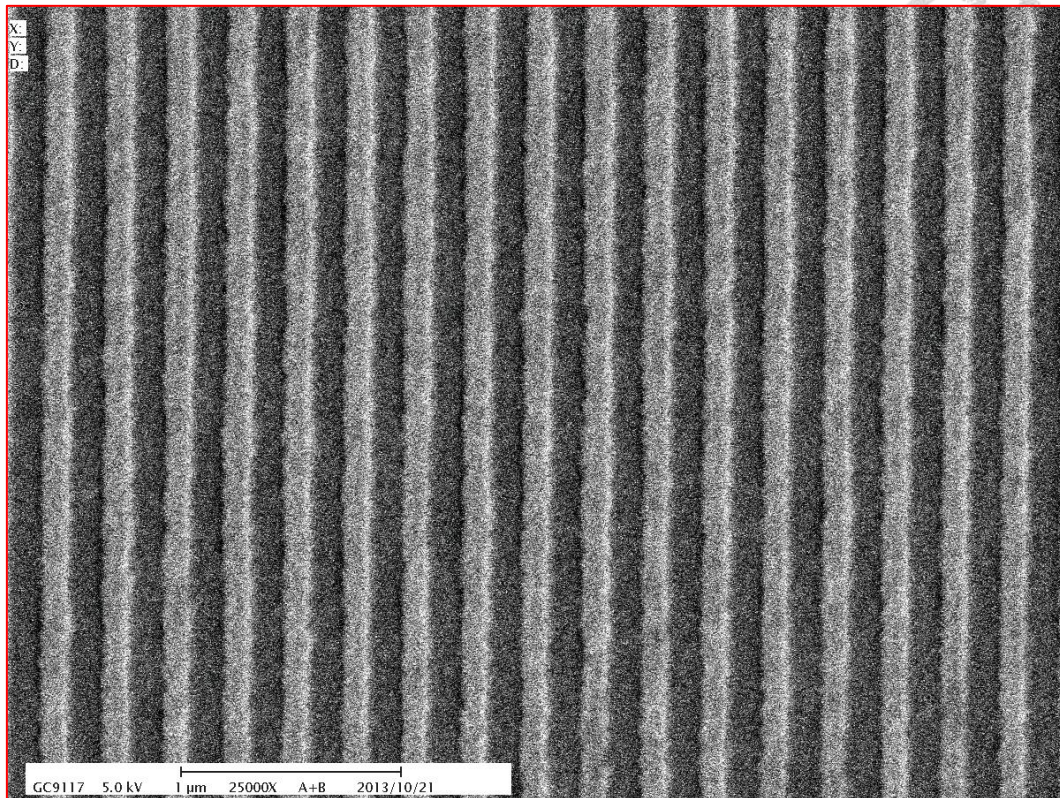


Fig. 5-3 SEM photo of designated aluminum grating on glass substrate.

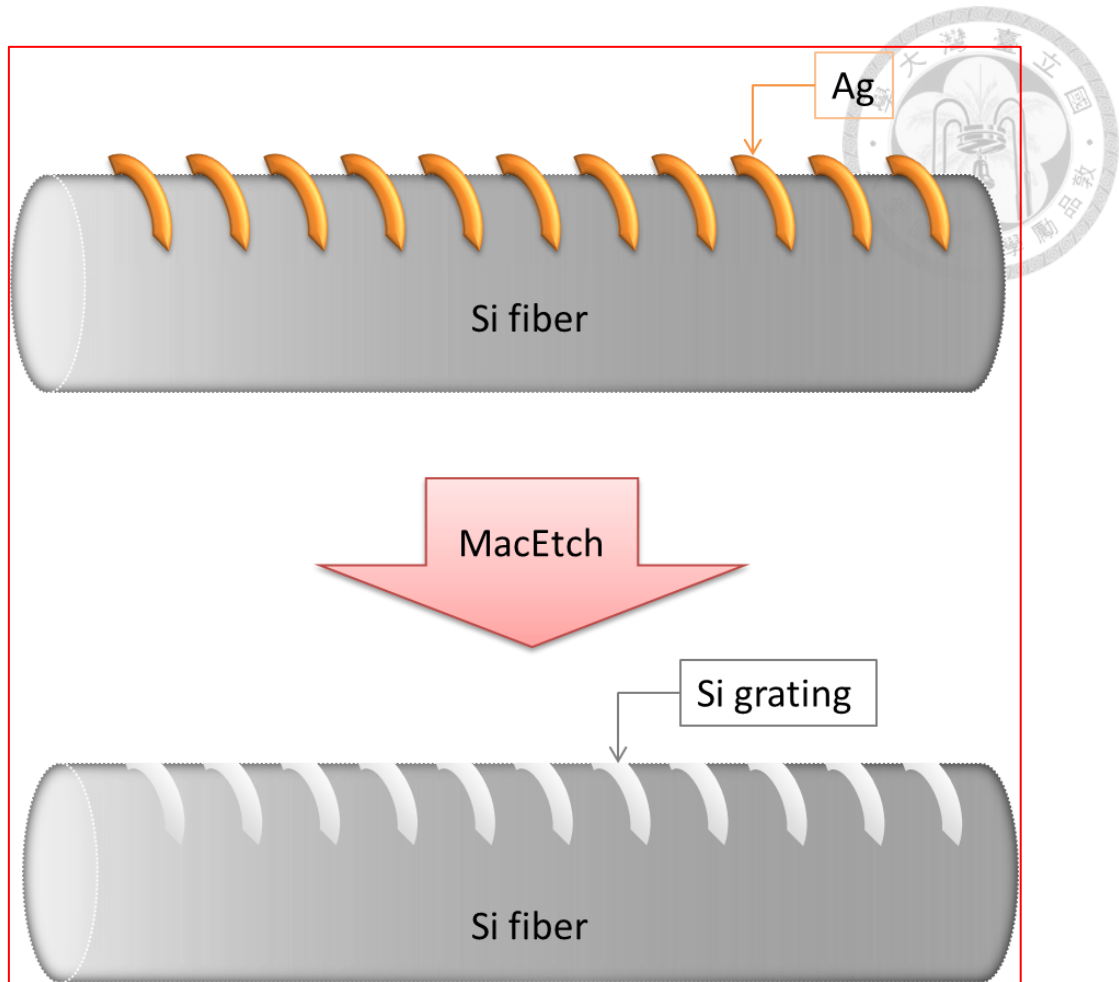
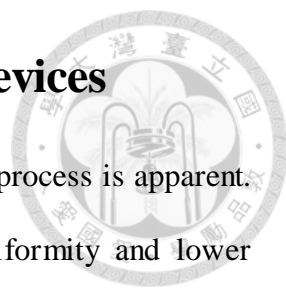


Fig. 5-4 Fabrication process of silicon fiber grating using MacEtch.

5-2 Nano metal structures for electronic devices



The effect of the applying strip-off method to SCLT fabrication process is apparent. The metal mesh made by strip-off method has better pattern uniformity and lower leakage current as the base-electrode of SCLT. As mentioned in the last chapter, due to the unideal collimation of metal deposition in large-area fabrication, the yield of traditional lift-off process is not good as well. The yield on the edge of pattern is lower than the one at the center of pattern. The tape-assisted strip-off method could solve this problem. The unwanted metal thin film attached on the sidewall of sacrificial structure can be easily removed when the tape was peeled off. So the pattern uniformity and yield of large-area fabrication were thus significantly improved.

Fig. 5-5 shows the electrical measurement results comparison of the first generation and the third generation SCLT. After applying the non-wet-etch and solvent-free strip-off process, the base leakage of SCLT has been significantly reduced over one order. The ON/OFF current ratio thus increased to 10^5 , nearly 30 times better than before. The differences between wet-etch and strip-off method have been listed in Table 5-1.

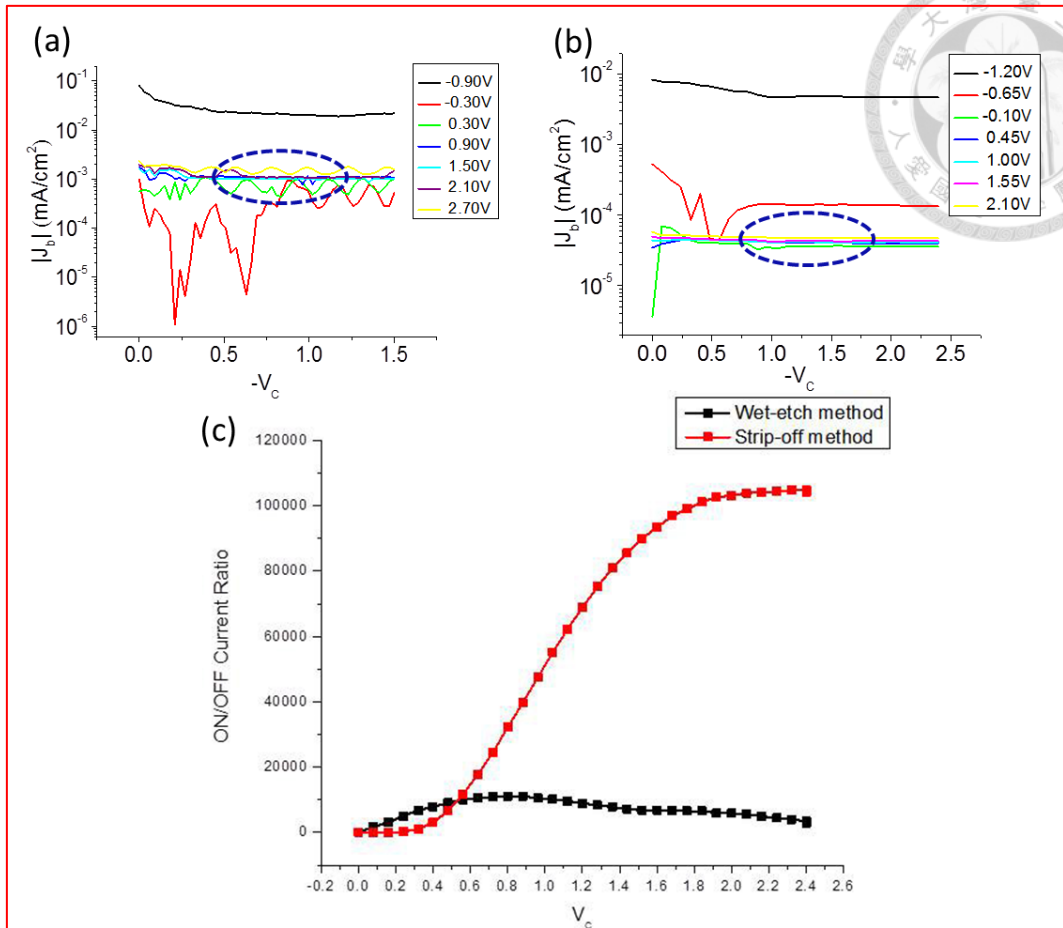
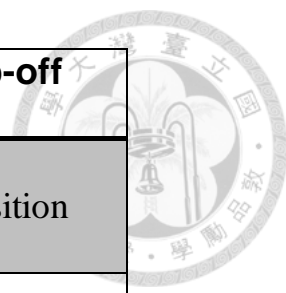


Fig. 5-5 Base current of SCLT which made by (a) wet-etching and (b) strip-off method.

(c) ON/OFF current ratio of 1st (black) and 3rd (red) generation SCLT.



	wet-etch	strip-off
Mesh formation	etching	deposition
Etchant	Al etchant	
Pattern uniformity	normal	good
Hole diameter	100 nm	80 nm
Output current	4.3 mA	4.6 mA
Base leakage	10^{-3} mA	5×10^{-5} mA
ON/OFF ratio	10^4	10^5

Table 5-1 Comparison table of wet-etch and strip-off method.

5-3 Nano metal structures for sensing devices

Surface plasmons have attracted the attention of physicists, chemists, biologists and material scientists for widespread use in areas such as electronics, optical sensing, biomedicine, data storage and light generation. Recent developments in nanotechnology have generated new insights about control of various properties of nanomaterials that can support surface plasmons for specific applications. Localized surface plasmon resonance (LSPR) is an optical phenomena generated by a light wave trapped within conductive nanostructures smaller than the wavelength of light [49]. Nanostructures that support plasmons play a significant role in enabling surface enhanced techniques, such as surface enhanced Raman spectroscopy (SERS). Previous research shows that increased symmetry results in increases of LSPR intensity [50]. Our IL process is good at generating large-area periodic nano patterns. So large-area fabrication of periodic nano metal structures like rods, holes could be easily realized by our IL/strip-off method.

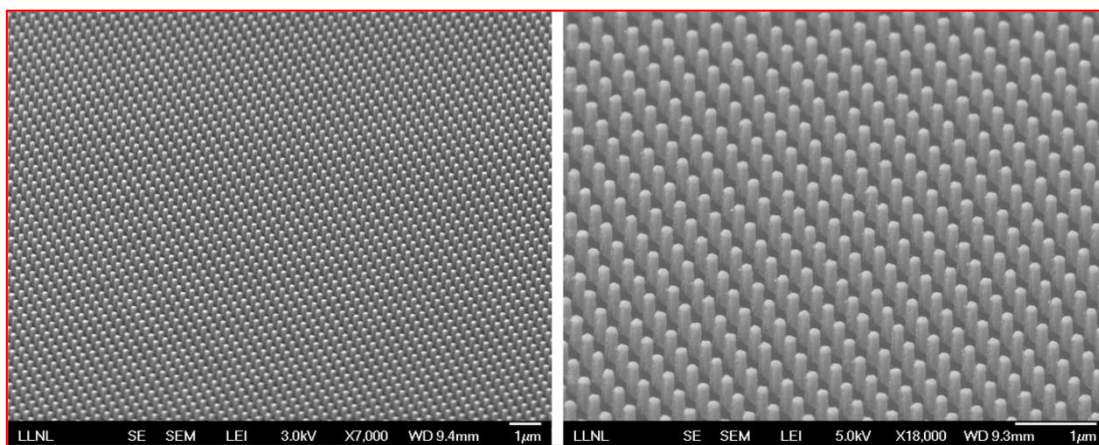


Fig. 5-6 SEM images of the silver nanopillar array (tilted view: 45°) [51].

Chapter 6 Conclusions and Future Works



6-1 Conclusions

The development of three generations of *imprinted* SCLTs has been described in this thesis. The previous research showed that smaller hole diameter of metal mesh and lower base leakage current were the key point of improving the performance of SCLT. We developed a novel method which combines IL and ALD in order to overcome the resolution limit of IL. Large-area, sub-100 nm imprint mold could be fabricated by depositing an aluminum-oxide thin film on the surface of photoresist structure conformably. The hole diameter of base-electrode thus reduced from 180 nm to 90 nm, smaller than resolution limit of our IL system. The output current of the 2nd generation SCLT increased to 4.35 mA, more than ten times better than the 1st generation SCLT (0.35 mA). The ON/OFF current ratio also increased 300% to 10^4 .

Though the output current of *imprinted* SCLT has been improved, the next step is to reduce the base leakage. Wet-etching method used in mesh fabrication process might produce side products which were attached to the sidewall of channel, affecting the insulativity of PVP. We introduced a novel tape-assisted lift-off, the strip-off method, to replace the wet-etching method in the fabrication process. This solvent-free technique significantly improved the process tolerance in large-area fabrication. Since there was no liquid etchant or solvent in the process, the base leakage current of the 3rd generation SCLT decreased nearly one order of magnitude to 5×10^{-5} mA while the output current remained the same level. The ON/OFF current ratio also increased to over 10^5 , thirty times better than the 1st generation SCLT. And the yield of reproduction has been also

improved.

The obtained low leakage current and high ON/OFF ratio of 3rd generation *imprinted* SCLT has made itself a competitive option in driving OLED for future applications.



6-2 Future works

Short term target:

The leakage current of the 3rd generation SCLT is now at the same level of other organic transistors after the strip-off method is applied. To further improve SCLT's performance, we need to increase the output current. But P3HT used as the active material of SCLT was not originally designed for vertical-channel transistors. It cannot stack in the channel tier upon tier perfectly due to its molecular shape. Finding a new material with higher carrier mobility might be helpful for improving the output current.

Long term target:

There are two possible developing directions: (1) improving mass production ability, and (2) developing new types of organic transistors.

For the purpose of improving mass production ability, we can introduce the roll-to-roll (R2R) or roll-to-plate (R2P) imprint system which are shown in Fig. 6-1. A large roller with adhesive surface serves as an infinite-long adhesive tape. The introduction of strip-off method also provides the possibility of polymer-based flexible substrate application since it's a non-etching and solvent-free process. Fig. 6-2 shows a prototype of flexible SCLT using *poly(ethylene 2,6-naphthalate)* (PEN) as substrate. The base current labeled in Fig. 6-3 shows the applicability of strip-off method, the leakage of base electrode on a PEN substrate remains the same as the one on an ITO substrate.

On the other hand, improving the insulativity among different electrodes is the key point of improving the energy efficiency of transistors. The new types of organic transistors which labeled in Fig. 6-4 use Al_2O_3 as the insulating layer in order to achieve zero gate current at cut-off state.



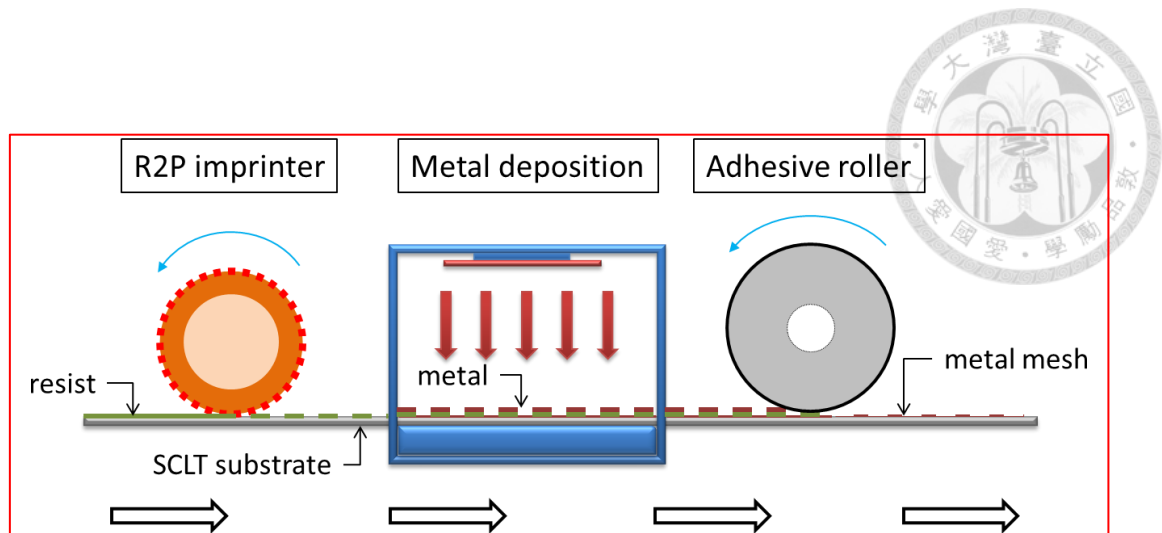


Fig. 6-1 Schematic diagram of a mass production system with R2P imprinter and roller strip-off instrument.

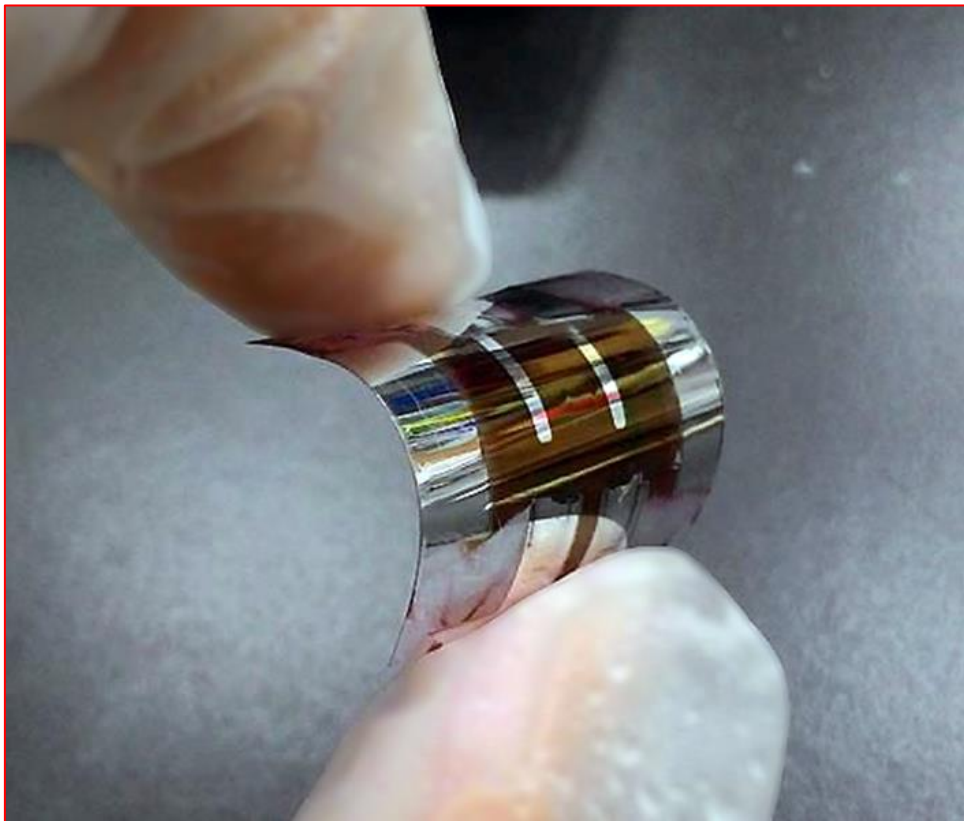


Fig. 6-2 Flexible SCLT device using PEN substrate to replace ITO glass.

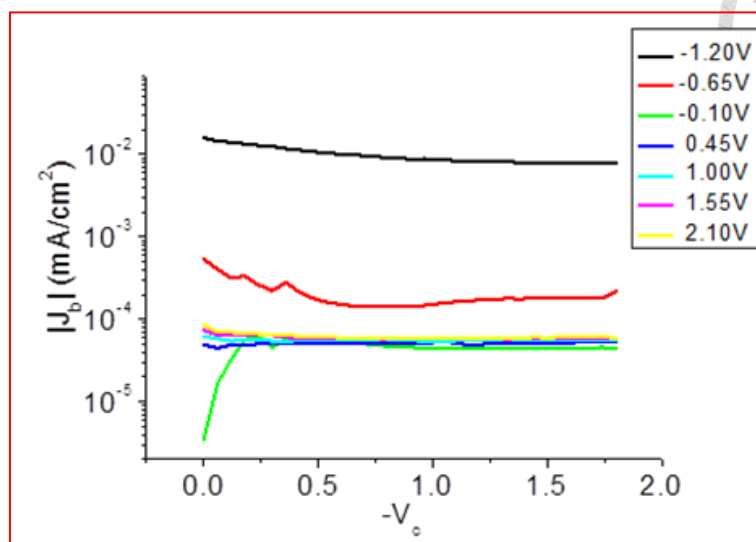


Fig. 6-3 Base current of flexible SCLT on PEN substrate.

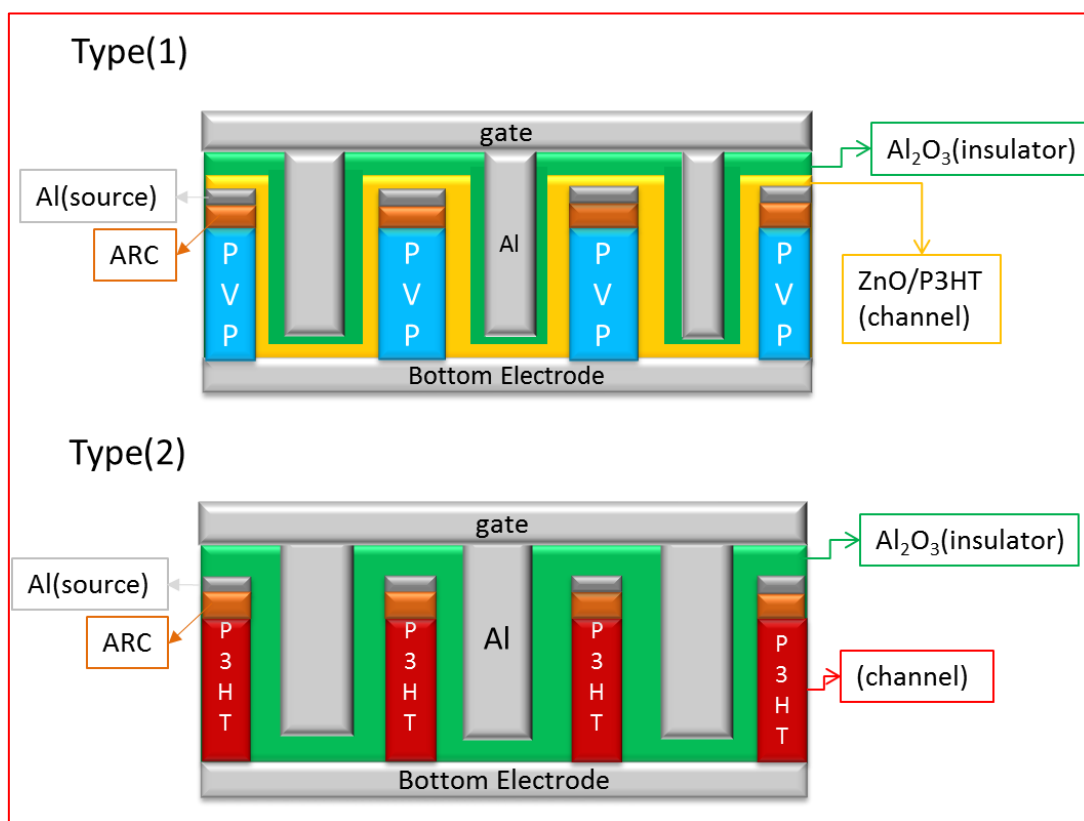
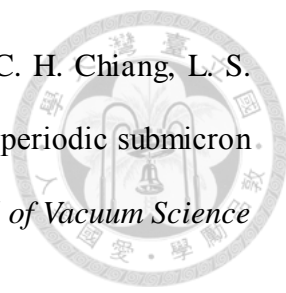


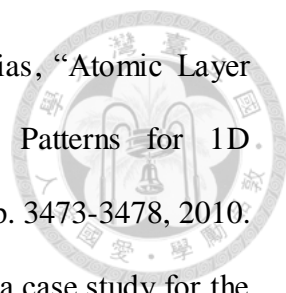
Fig. 6-4 Two prototypes of future organic transistors.

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