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Master Thesis

一個高速採用時間交錯式的連續漸進式類比至數位轉換器

A High-Speed Time-Interleaved SAR ADC

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本論文係 黃維家 君（R02943026）在國立臺灣大學電子工程學研究所完成之碩士學位論文，於民國 105 年 7 月 13 日承下列考試委員審查通過及口試及格，特此證明

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A High-Speed Time-Interleaved SAR ADC

By

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THESIS

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摘要

在次世代無線通訊系統中，類比至數位轉換器必須操作在極高速的取樣頻率及低中解析度下。

本論文提出一個以 40 奈米 CMOS 一般製程，實現出六位元每秒四十五億次取樣的時間交錯連續漸進式類比至數位轉換器，藉由結合前端輸入緩衝器的架構及分組式技巧，有效地降低時間交錯式架構的輸入電容負載，並增加輸入訊號的可用安定時間，提出的 16 通道的時間交錯連續漸進式類比至數位轉換器得以達到高取樣速度及高輸入頻寬的表現。透過使用零交越 (zero-crossing) 偵測技巧，可以補償多通道間時間偏移的誤差，並透過數位校正處理多通道間的增益電壓及偏移電壓不匹配。在單通道方面，採用連續漸進式架構，並使用非同步處理及單向電容切換技巧使單通道具有高速度及高能量效率的特性。除此之外，任意選擇權重之電容陣列解決了單通道中比較器的動態偏移電壓的問題。

量測結果顯示，在每秒四十億的轉換，DNL 和 INL 分別為+0.17/-0.29 LSB 和+0.20/-0.18 LSB。在每秒四十五億的轉換及輸入頻率為一億赫茲下，SNDR 和 SFDR 分別為 32.15 dB 和 41.04 dB，在 1.2 V 的供應電壓下，功率消耗為 24.9 毫瓦，品質因數(FoM)為 159 fJ/c.-s。全部的晶片面積大小為 1.275 mm^2，核心電路的面積是 0.195 平方毫米。

關鍵詞:類比至數位轉換器、時間交錯式、連續漸進式、分組技巧、高輸入頻寬

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Abstract

Analog-to-digital converter (ADC) has to operate at ultra-high speed with low to medium resolution in the next-generation wireless communication systems.

A 6-bit 4.5 GS/s time-interleaved SAR ADC in 40 nm CMOS general–process (GP) technology is proposed. By combining the front-end input buffers and the grouping technique into the time-interleaved architecture, the input capacitance effectively decreases and the available settling of input buffers increases. The proposed 16-channel time-interleaved SAR ADC achieves the performance of high-speed sampling rate and high input bandwidth. A zero-crossing detection technique is employed to correct timing skew among sub-ADCs. Gain and offset mismatches between sub-ADCs are calibrated in the digital domain. Asynchronous processing and monotonic capacitor switching technique used in the single-channel SAR ADC make the sub-ADC high speed and power-efficiency. Furthermore, AWCA technique solves the dynamic offset problem of the comparator in the sub-ADC.

The measurement results show that ADC exhibits DNL of +0.17/-0.29 LSB and INL of +0.20/-0.18 LSB at 4 GS/s with F_{in} of 50 MHz. SNDR and SFDR are 32.15 dB and 41.04 dB at 4.5 GS/s with F_{in} of 1 GHz. The power consumption is 24.9 mW at 1.2 V supply voltage. As a result, the FoM ($Power/2^{ENOB}/F_S$) is 159 fJ/conversion-step. The whole chip including pads occupies 1.275 mm^2 while area of core circuit is 0.195 mm^2.

Keywords**:** analog to digital converter, time-interleaved, SAR, grouping technique, high input bandwidth

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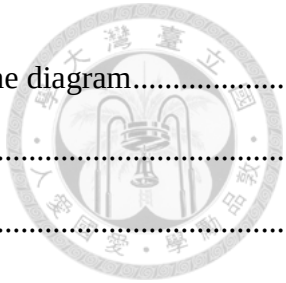

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Chapter 1

Introduction

1.1 Motivation

Analog-to-digital converters (ADCs) are the essential interface between the analog world and the digital system. ADCs acquire and quantize the analog signal for digital signal processing (DSP). The process of signals in the digital domain has an advantage of high accuracy. It also acquires higher data rate and great power efficiency with the advanced CMOS technology.

High-speed ADCs with multi-GS/s and 4-8 bit resolutions have become an important trend for next-generation communication system such as 60-GHz wireless transceivers, high-speed serial link transceivers, ultra-wideband systems, and millimeter-wave standards system [1], [2]. In the past, ADCs of the flash architecture has been dominantly used for the communication network. However, the flash architecture requires many parallel preamplifiers and comparators to quantize the analog signal at the same time, resulting larger power consumption. Although another ADCs of the pipeline architecture also achieve these requirements, the design of high-performance operational amplifier (OPA) is more challenging with the advanced CMOS process. Moreover, OPAs consume large power in pipelined ADCs.

In recent years, ADCs of the successive approximation register (SAR) architecture have become a mainstream architecture. The SAR ADC is a digital-friendly architecture and the comparator-only operation makes the SAR ADC gain higher conversion rate and area- and power-efficiency with the

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advanced CMOS process [3]-[6]. However, the SAR ADC requires several comparison cycles to complete one conversion and limits the ADC in much higher speed applications. On the other hand, when the speed of these single-channel ADCs increases to some limitation, the power consumption grows exponentially.

The time-interleaved (TI) architecture is adopted to fulfill much higher sampling rate by using multiple sub-ADCs in parallel. Sub-ADCs can be any type of ADC architectures, such as flash, pipelined, and SAR architectures. SAR architecture is suitable for TI architecture because it only needs to operate in moderate sampling rate and thus the entire TI ADC maintain good power efficiency [7]-[10]. However, TI ADC suffers from mismatches between sub-ADCs, such as offset, gain, and timing skew [11]. These mismatches degrade the overall performance of ADC. Furthermore, the input capacitance increases proportionally with the number of sub-ADCs, and hence it limits the input bandwidth of the overall ADC.

In this thesis, the proposed frond-end architecture is proposed to overcome the input bandwidth of TI ADC, thus achieving a 16-channel TI SAR ADC of high-speed sampling rate.

1.2 Thesis Organization

This thesis contains seven chapters. In chapter one, it briefly introduces the motivation and the thesis organization. Chapter two presents the basic ADC knowledge and error sources and several methods of calibration in TI ADCs. Chapter three discusses prior works of TI ADCs and the proposed

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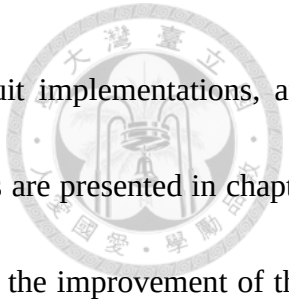

TI SAR ADC. Details of proposed building blocks with analyses, circuit implementations, and simulation results are described in chapter four. Next, measurement results are presented in chapter five. Finally, chapter six concludes this thesis and chapter seven point out the improvement of this work.

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Chapter 2

Fundamentals of Analog to Digital Converter

2.1 Introduction

Several important performance metrics about static and dynamic performance of ADC are defined [16]. Three types of commonly used ADC architectures are described [16]. Finally, the error sources and related methods of calibration in time-interleaved architecture are discussed.

2.2 Performance Metrics

The performance of ADC requires a number of parameters. These parameters can be divided into static and dynamic performance.

2.2.1 Static Performance

2.2.1.1 Offset and Gain Error

Offset error is the shift of actual transfer curve from ideal transfer curve shown in Fig. 2.1(a). Gain error is the difference of the slopes of actual transfer curve and ideal transfer curve when offset error is zero shown in Fig. 2.1(b).

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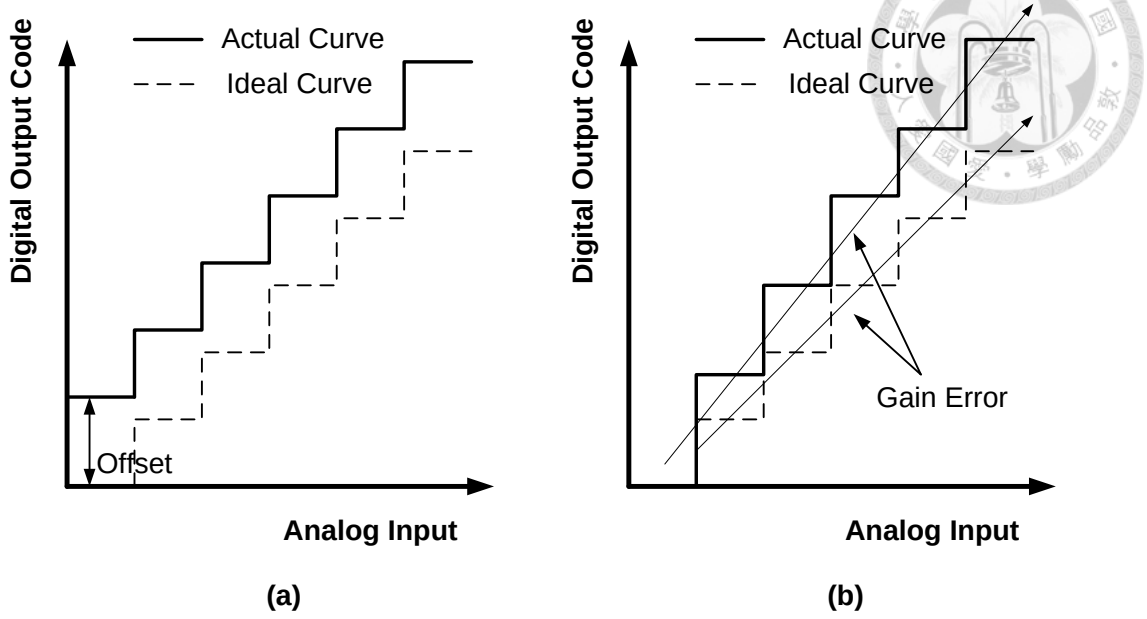

Fig. 2.1 Transfer curve with (a) offset and (b) gain error

2.2.1.2 Differential and Integral Nonlinearities (DNL, and INL)

Differential nonlinearity (DNL) is defined as the difference of each actual transition level width and ideal transition level width without offset and gain error. DNL at code n is given as:

$$DNL = \frac{V_{n+1} - V_n}{V_{LSB}} - 1 \ , \ 0 \le n \le (2^N - 1) \tag{2.1}$$

where V_n is an actual transition point of digital output code n, and N is the resolution of ADC. V_{LSB} is an amplitude voltage of a Least significant bit (LSB), so DNL is expressed by LSB.

Integral nonlinearity (INL) is defined as the deviation of actual transfer curve from an ideal straight line and is also expressed by LSB. INL at code n is said to be the width difference of actual transition point n and ideal transition point n. Summing up DNL from code 0 to code n is an another way to evaluate INL:

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$$INL(n) = \sum_{i=1}^{n} DNL(i) \tag{2.2}$$

DNL and INL are shown in Fig. 2.2. DNL or INL is often expressed like +0.5/-0.5LSB, which are maximum and minimum value from corresponding DNL or INL sequence.

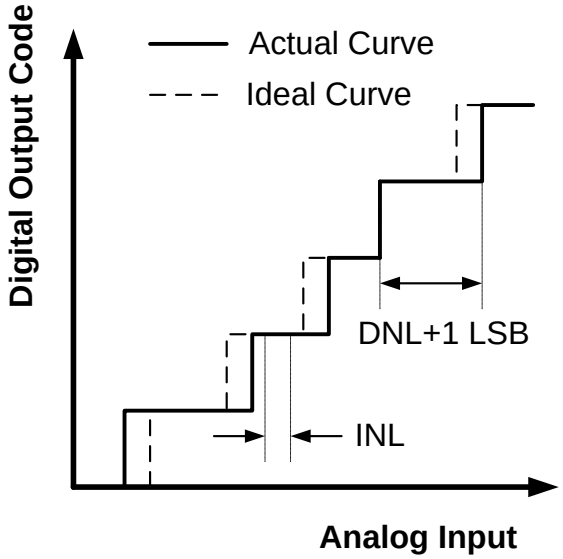

Fig. 2.2 Transfer curve with DNL and INL

2.2.2 Dynamic Performance

Dynamic performance is measured by Fast Fourier Transformer (FFT) analyzer, which is a hardware device or mathematic software such as MATLAB. Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD), Spurious Free Dynamic Range (SFDR), Signal-to-Noise and Distortion Ratio (SNDR) are the important dynamic performances to evaluate an ADC.

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2.2.2.1 Signal-to-Noise Ratio (SNR)

Signal to noise ratio (SNR) is the ratio of signal power to noise power. SNR is written as:

$$\mathrm{SNR}\big|_{\mathrm{dB}} = 10\log\left(\frac{\text{Signal Power}}{\text{Noise Power}}\right) \tag{2.3}$$

2.2.2.2 Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of harmonics power to signal power. Harmonics power is defined as the root mean square (RMS) of all harmonics in the FFT spectrum. However, in the most cases, the sum of first five harmonics power to represent harmonics power is enough because the rest is insignificant and is submerged in noise flow. THD is expressed as:

$$\mathrm{THD}\big|_{\mathrm{dB}} = 10\log\left(\frac{\text{Harmonics Power}}{\text{Signal Power}}\right) \tag{2.4}$$

2.2.2.3 Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range (SFDR) is the ratio of signal power to the largest power of distortion. For single-channel ADC, the largest distortive power is mainly caused by harmonic distortion. However, for time-interleaved ADC, the largest distortive power may be from mismatch among sub-ADCs. SFDR is mentioned as:

$$\mathrm{SFDR}\big|_{\mathrm{dB}} = 10\log\left(\frac{\text{Signal Power}}{\text{Largest Distortion Power}}\right) \tag{2.5}$$

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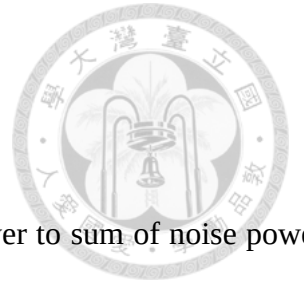

2.2.2.4 Signal-to-Noise and Distortion Ratio (SNDR)

Signal to noise and distortion ratio (SNDR) is the ratio of signal power to sum of noise power and harmonics power. SNDR is described as:

$$\text{SNDR}\big|_{\text{dB}} = 10\log\left(\frac{\text{Signal Power}}{\text{Noise Power} + \text{Harmonics Power}}\right) \tag{2.6}$$

2.2.2.5 Effective Number of Bits (ENOB)

Effective number of bits (ENOB) is a measure of the quality of a digitized signal. ENOB is derived from SNDR:

$$\text{ENOB}\big|_{\text{bit}} = \frac{\text{SNDR}\big|_{\text{dB}} - 1.76}{6.02} \tag{2.7}$$

2.2.2.6 Figure of Merit (FoM)

Figure of Merit (FoM) is an important performance metric of ADC in terms of power, speed, and accuracy. It is a measure that various types of ADCs can be put together and compared together. FoM is defined as:

$$\text{FoM} = \frac{\text{Power}}{2^{\text{ENOB}} \times F_S} \quad \text{or} \quad \frac{\text{Power}}{2^{\text{ENOB}} \times ERBW} \tag{2.8}$$

where F_S is the conversion rate of ADC and ERBW is the signal frequency at which SNDR drops by 3dB compared to low frequency value.

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2.3 Architectures

2.3.1 Flash Architecture

Flash architecture is shown in Fig. 2.3. It contains several $2^N - 1$ comparators where N is the resolution of ADC and a decoder. Operation of flash ADC is as follows. Analog input of flash ADC is compared with reference voltages generated by resistor-ladder. Output of a comparator is digital "1" if analog input is larger than corresponding reference voltage. On the other hand, output of a comparator is digital "0" if analog input is smaller than corresponding reference voltage. By collecting digital output of the comparators in order, thermometer code is generated. A decoder converts the thermometer code to the binary code. Besides comparators, preamplifiers are often added in front of comparators to decrease input-referred offset. Flash ADC achieves the fastest conversion rate because of the parallel processing. However, when the resolution of flash ADC increases, power and area consumption increase exponentially. As a result, flash ADC is usually implemented in low resolution and high-speed design.

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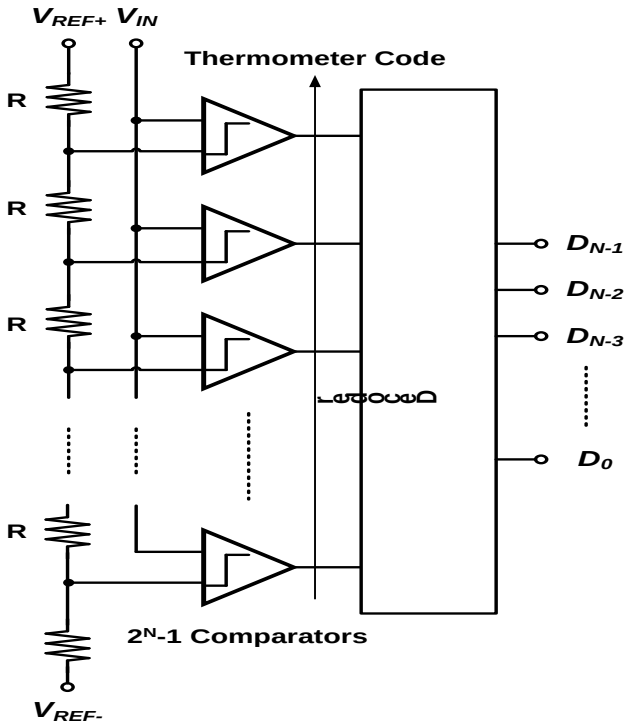

Fig. 2.3 Flash architecture

2.3.2 Successive-Approximation-Register Architecture

Successive-approximation-register (SAR) ADC architecture is shown in Fig. 2.4. It is composed of a front-end track-and-hold circuit (T/H), a comparator, a successive-approximation (SA) control logic, and a digital-to-analog converter (DAC). Binary search algorithm is applied to approach analog input and to simultaneously determine the digital output. Take a 6-bit resolution SAR ADC as an example. First, T/H acquires analog input voltage while the registers of the SA control logic are set "100000". Through DAC, V_{DAC} is set $\frac{V_{REF}}{2}$. Next, the comparator compares $V_{T/H}$ with V_{DAC}, and the result of comparison is send to the SA control logic. If $V_{T/H}$ is larger than V_{DAC}, most significant bit (MSB) is still "1", and SA control logic is set "110000". Then, V_{DAC} becomes $\frac{3V_{REF}}{4}$ for next

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comparison. Otherwise, most significant bit (MSB) is changed to 0, and SA control logic is set "010000" which makes V_{DAC} equal to $\frac{V_{REF}}{4}$ for next comparison. The procedure repeats until six digital code is determined.

Because only one comparator is used in SAR ADC, power consumption is therefore much lower than other ADC. The comparator offset is independent of the linearity since it just shift the entire transfer characteristic. Furthermore, SAR ADC benefits from the advanced CMOS technology and the lower supply voltage due to its digital-friendly architecture. Therefore, SAR ADC recently becomes a popular ADC architecture in medium-to-high resolution and low-power design.

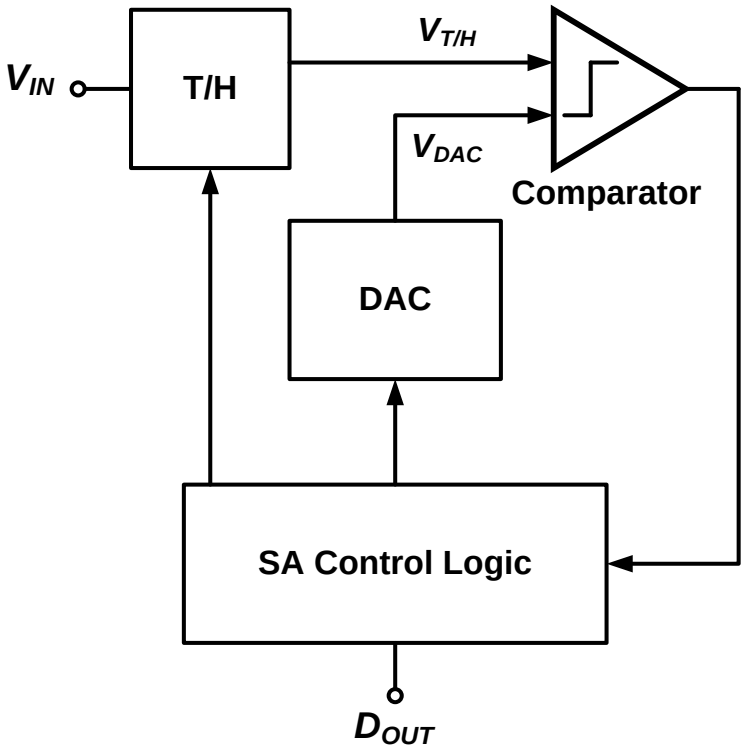

Fig. 2.4 Successive-approximation-register architecture

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2.3.1 Time-Interleaved Architecture

The time-interleaved ADC is an effective way to achieve a high-speed conversion rate. The architecture of time-interleaved ADC is shown in Fig. 2.5. It is established by paralleling M ADCs where M is the number of ADC channels (sub-ADCs). The time-interleaved ADC can be implemented by various type of ADC architecture such as flash, SAR or pipelined architecture. It works as follow: In a time-interleaved ADC with M channels, the sampling clock enters clock generator and divided into multiple clock phases (clk1~clkM), and each clock phase triggers the corresponding sub-ADC to sample V_{in} analog signal and then the sub-ADC starts to digitize V_{in} analog signal. When conversion is done, digital output of channels are realigned through multiplexer (MUX) circuit. The timing diagram of TI ADC is shown in Fig. 2.6. The time interval between subsequent channels is one sampling period $\frac{1}{F_s}$. By interleaving M channels, the time-interleaved ADC operate M-times faster than the single-channel ADC. This architecture relieves the harsh requirement that avoids designing a single-channel ADC to work at high conversion rate, and hence lowers the power consumption. However, the time-interleaved ADC suffers from mismatch between channels, such as offset, gain, and timing skew mismatches. These mismatch degrade the performance heavily and the ADC needs to be calibrated [12]-[15]. Furthermore, the Nyquist frequency of the time-interleaved ADC is M times faster than a single-channel ADC. It makes the front-end circuit of ADC such as input buffers and T/H circuits need sample M times faster frequency of input signal. Therefore, the front-end circuit becomes a challenging issue in the time-interleaved architecture.

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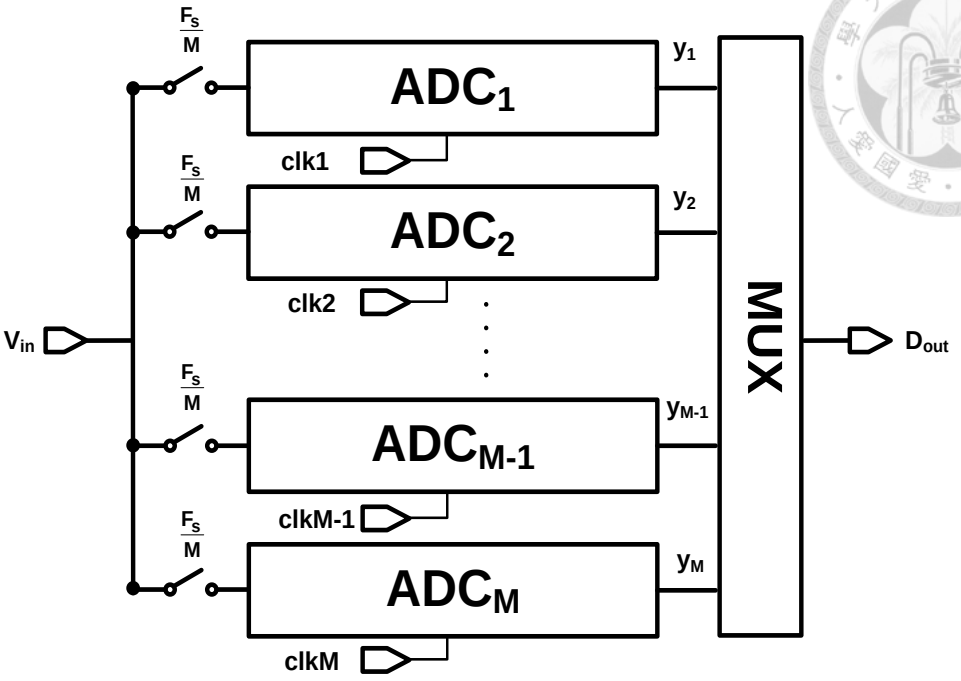

Fig. 2.5 Time-interleaved architecture

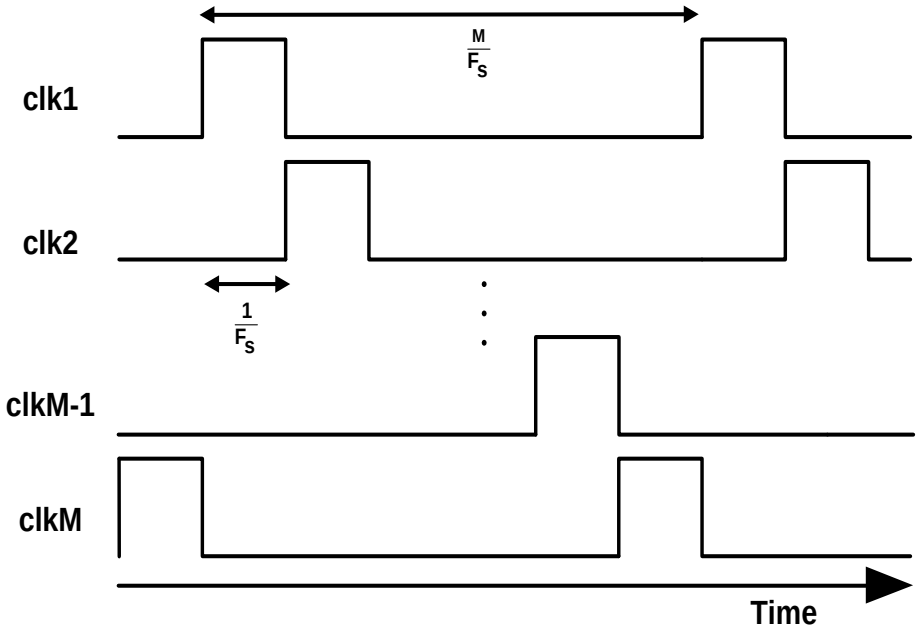

Fig. 2.6 Time-interleaved timing diagram

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2.4 Error Sources and Calibrations in Time-Interleaved Architecture

Although the time-interleaved ADC has high sampling rate and high energy-efficiency, mismatches among sub-ADCs cause undesired spur over the signal spectrum. These phenomena are described and related techniques of calibration are also introduced in this section. Generally, calibration is processed in two steps: mismatch detection and error correction. Two steps perform in either digital or analog domain. In addition, the calibration is implemented in either foreground or background. Foreground calibration means that the ADC is calibrated during start-up and ADC starts normal operation after calibration. On the contrary, background calibration enables continuous calibration while ADC maintains the normal operation.

2.4.1 Offset Mismatch and Calibration

A two-channel time-interleaved ADC having offset mismatch is shown in Fig. 2.7, and assuming that other characteristics are ideal. If the input is a sinusoidal signal $V_{in} = \cos(2\pi f_{in} t+\theta)$, the output of two-channel ADC is written as

$$\begin{aligned} y_1[n] &= cos(2\pi f_{in} nT_s + \theta) + V_{os1} \quad n = even \\ y_2[n] &= cos(2\pi f_{in} nT_s + \theta) + V_{os2} \quad n = odd \end{aligned} \tag{2.9}$$

where f_{in} is input frequency; n is sampling point; T_s is sampling period ; and V_{osi} is channel's offset (i=1, 2).

Considering (2.9), the output of the ADC is expressed as

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$$y[n] = cos(2\pi f_{in} nT_s + \theta) + V_{os} + \frac{\Delta V_{os}}{2} cos(2\pi \frac{f_s}{2} nT_s) \quad (2.10)$$

where $V_{os} = 0.5(V_{os1+} V_{os2})$, $\Delta V_{os} = V_{os1}-V_{os2;}$ and f_s is sampling frequency.

In (2.10), the third term shows that offset mismatch causes a tone at $\frac{f_s}{2}$ and it is independent of the amplitude or frequency of the input. As shown in Fig.2.8, the error due to offset mismatch does not depend on the input signal and the noise tone is observed at $\frac{f_s}{2}$ in the output spectrum.

In more channels than two-channel tome-interleaved ADC, the distortions caused by offset mismatch appear at the frequencies:

$$\frac{k}{M} f_s \qquad k = 1, ..., M-1 \quad (2.11)$$

where M is the number of channels in a time-interleaved ADC.

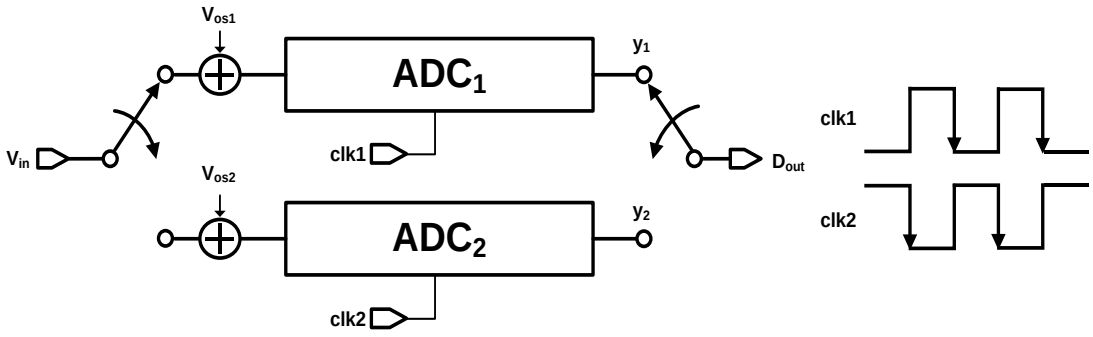

Fig. 2.7 A two-channel time-interleaved ADC with offset mismatch

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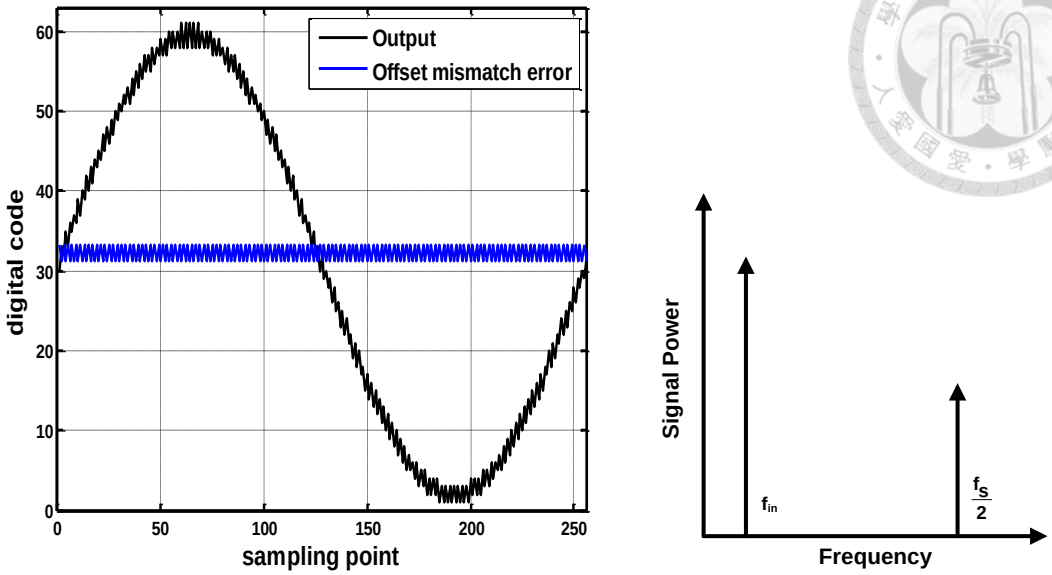

(a) (b)

Fig. 2.8 Offset mismatch (a) ADC output and error signal in time domain (b) ADC output power spectrum

To solve offset mismatch is relatively simple as hardware and algorithm complexity. Fig. 2.9 shows a common calibration technique [12], [17] in analog domain. First, the analog input nodes are shorted and then the output would correspond to the sigh of the input-refereed offset during detection. Next, the calibration logic such as DAC starts to adjust the comparator's current sources or variable capacitors and compensate the offset voltage. Finally, the digital output begins to oscillate and the offset converges to the smallest correction step at the end of calibration. Moreover, if ADC has front-end buffers, these buffers may cause offset mismatch. The problem is solved by the same technique. Other calibration technique in digital domain is extensively used [15], [18]-[19]. Each sub-ADC's offset is detected by calculating long term mean of its output with a quasi-stationary input signal such

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as sinusoidal wave. Then offset is calibrated by subtracting the offset value from its respective output.

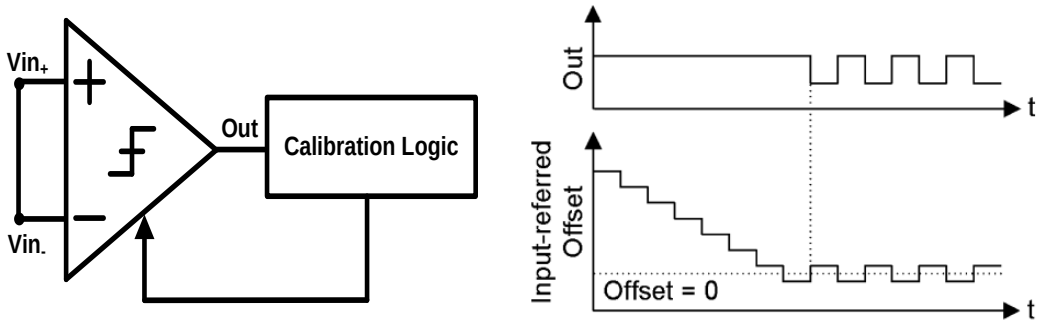

Fig. 2.9 Offset mismatch calibration in analog domain

2.4.2 Gain Mismatch and Calibration

Fig. 2.10 shows a two-channel time-interleaved ADC with gain mismatch. Similarly, suppose that other characteristics are ideal and the input is a sinusoidal signal $V_{in} = \cos(2\pi f_{in} t+\theta)$, the output of two-channel ADC is written as

$$\begin{aligned} y_1[n] &= G_1 cos(2\pi f_{in} nT_s + \theta) \quad n = even \\ y_2[n] &= G_2 cos(2\pi f_{in} nT_s + \theta) \quad n = odd \end{aligned} \tag{2.12}$$

where f_{in} is input frequency; n is sampling point; G_i (i=1,2) is gain of the ADC; and T_s is sampling period.

Considering (2.12), the output of the ADC is expressed as

$$y[n] = Gcos(2\pi f_{in} nT_s + \theta) + \frac{\Delta G}{2} cos\left[2\pi(f_{in} - \frac{f_s}{2}) nT_s + \theta \right] \tag{2.13}$$

where $G = 0.5(G_{1+}G_2)$; $\Delta G = G_1 - G_2$; f_s is sampling frequency.

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In (2.13), the second term shows that gain mismatch causes a noise tone at $f_{in}-\frac{f_s}{2}$. Consequently, it is dependent on the input frequency but independent of the input amplitude. As shown in Fig.2.11, the noise tone is at $f_{in}-\frac{f_s}{2}$ in the output spectrum. In time domain, the largest error occurs at the peak of the sinusoid wave. In more channels than two-channel tome-interleaved ADC, the distortions caused by gain mismatch appear at the frequencies:

$$\pm f_{in}+\frac{k}{M}f_s \qquad k=1,...,M-1 \tag{2.14}$$

where M is the number of channels in a time-interleaved ADC.

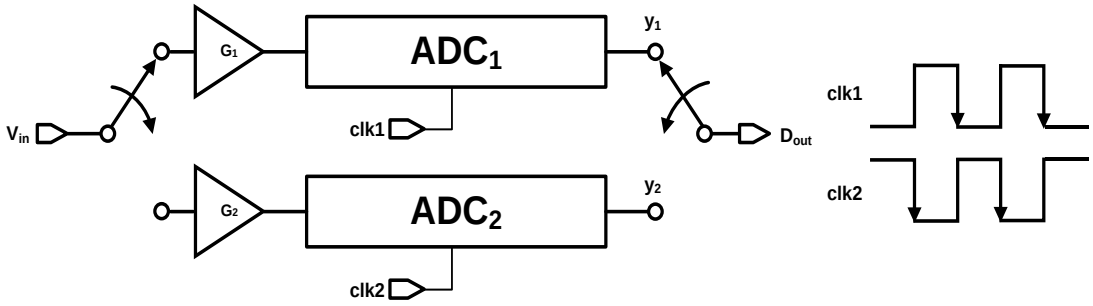

Fig. 2.10 A two-channel time-interleaved ADC with gain mismatch

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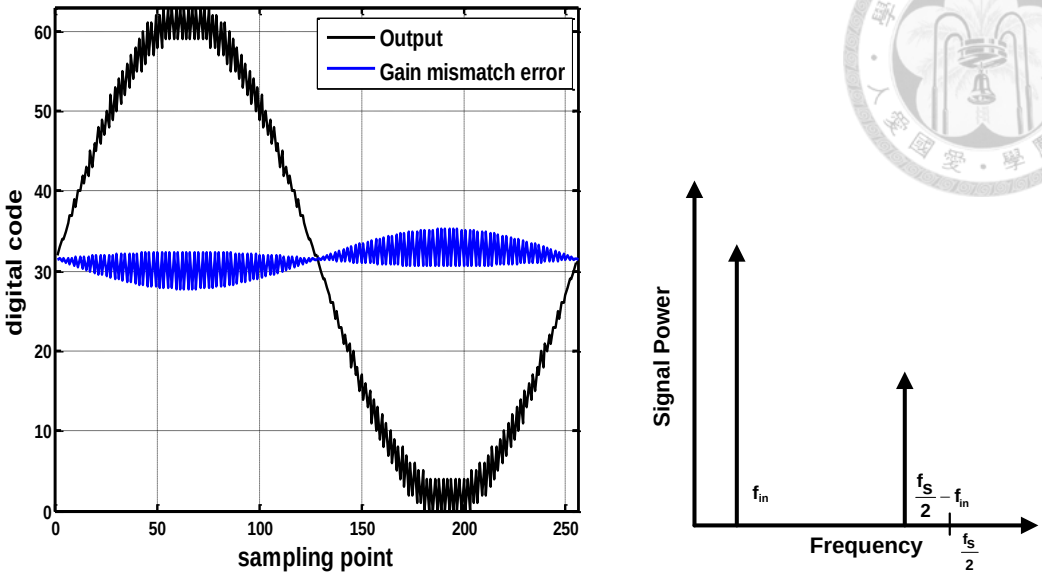

Fig. 2.11 Gain mismatch (a) ADC output and error signal in time domain (b) ADC output power spectrum

Gain mismatch calibration is similar to that in offset mismatch and they are generally calibrated together [15], [18]-[19]. Each sub-ADC's gain is detected by long term average of each absolute output with sinusoidal wave and then gain mismatch can be corrected by dividing each sub-ADC output's estimated gain in digital domain. Using calibration DAC to correct sub-ADCs' or front-end buffers' gain is also a correction method in analog domain [9], [20], [21].

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2.4.1 Timing Skew Mismatch and Calibration

As shown in Fig. 2.12, the two-channel time-interleaved ADC is considered again with timing mismatch. It is supposed that clk_1 is sampling ideally but clk_2 has timing skew dt. In this situation, the output of two-channel ADC can be written as

$$\begin{aligned} y_1[n] &= cos(2\pi f_{in} n T_s + \theta) \qquad n = even \\ y_2[n] &= cos[2\pi f_{in} n(T_s + dt) + \theta] \quad n = odd \end{aligned} \tag{2.15}$$

where f_{in} is input frequency; n is sampling point; T_s is sampling period; dt is ADC_2's timing skew.

By combing two sub-ADCs' output through some computation simplification, the output of the ADC is expressed as

$$y[n] = cos(2\pi f_{in} nT + \pi f_{in} dt + \theta) - \frac{\omega dt}{2} sin[2\pi(\frac{f_s}{2} - f_{in})nT - 2\pi f_{in}\frac{dt}{2} - \theta] \tag{2.16}$$

In (2.13), the first term is the actual input sample which has a little amplitude modulation because of the timing skew. The second term causes the noise tone of the timing skew at $\frac{f_s}{2}$-f_{in}. It is shifted by 90 degree compared to the gain mismatch while the location of noise tones is the same as that of gain mismatch in the output spectrum. As shown in Fig. 2.13, the largest error occurs when the input signal has the largest slope in the time domain. Furthermore, in more channels than two-channel tome-interleaved ADC, the distortions caused by timing skew mismatch appear at the frequencies:

$$\pm f_{in} + \frac{k}{M} f_s \qquad k = 1, ..., M-1 \tag{2.17}$$

where M is the number of channels in a time-interleaved ADC.

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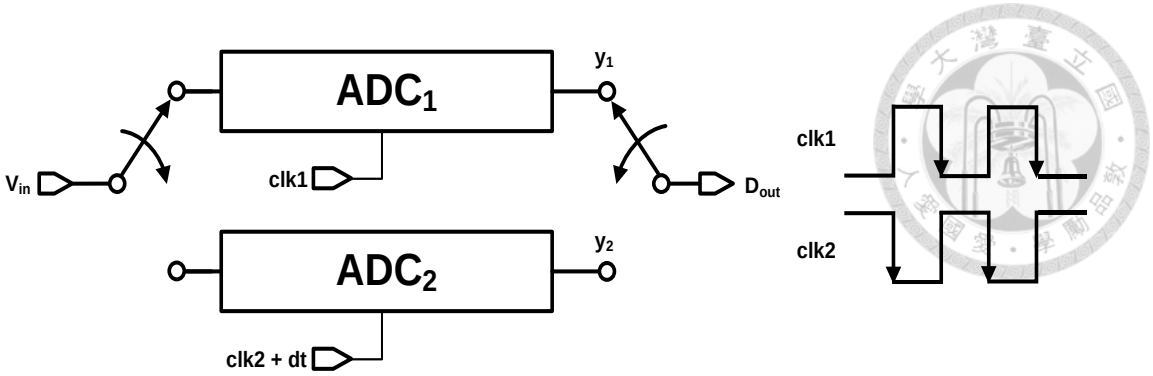

Fig. 2.12 A two-channel time-interleaved ADC with timing skew mismatch

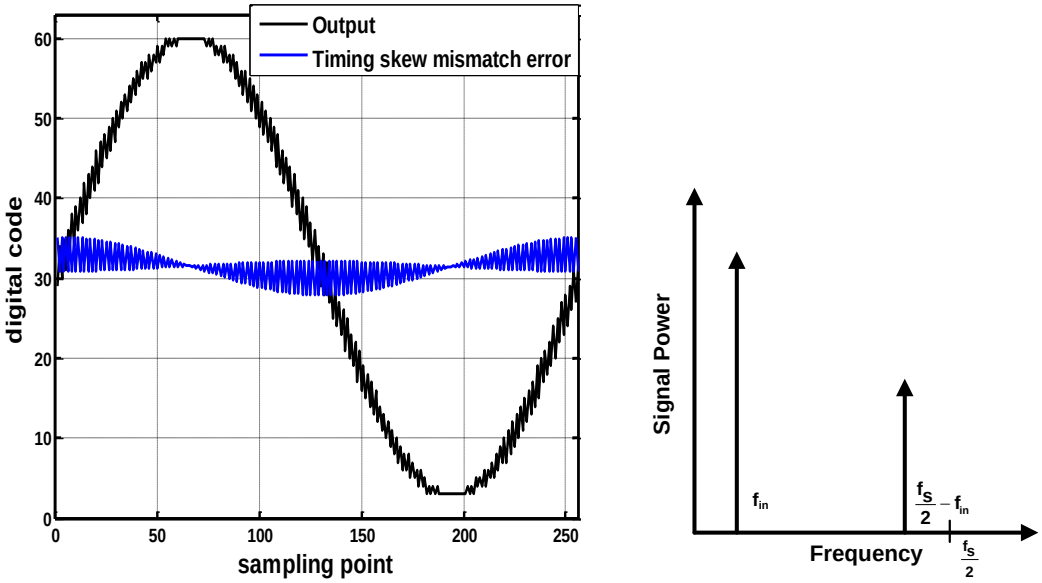

Fig. 2.13 Timing skew mismatch (a) ADC output and error signal in time domain (b) ADC output power spectrum

Unlike offset mismatch or gain mismatch, it is much harder to detect and correct timing skew mismatch. Although there are several techniques proposed to calibrate timing-skew mismatch, each technique has its own disadvantage and this issue is still being researched. In the beginning, digital calibration methods related digital signal processing (DSP) approaches is presented. It needs FIR

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filters or FFT processors and causes large chip-area and high power consumption. Hence, this method is seldom implemented in real chips. In [12], a correlation-based algorithm is used between sub-ADCs to estimated timing skew in background. In [10], the derivative of the input signal was estimated and thus timing skew is measured by combing the input derivative and error in sub-ADC output. However, both works [10] and [12] require additional reference ADCs for calibration. Another method in [13] detects timing skew by computing the probability of a zero crossing among additional samples. Nevertheless, these additional samples result in extra timing error. Fig. 2.14 shows a common detection method used recently [22]. The average value of $|x_2-x_1|-|x_3-x_2|$ is proportional to timing skew value if analog input signal is wide-sense stationary (WSS) such as sinusoidal wave. In this situation, the autocorrelation of input signal depends only on time difference rather than time absolute value. Then, timing skew can be detected due to this property. After timing skew is detected, the correction is done in digital or analog domain. However, the convergence time of these techniques of calibration is another problem in real application. In digital domain, numerous digital filters are needed, which costs high power and large area. On the other hand, variable delay line are added at the sampling clock to adjust timing skew in analog domain, while it increases the noise and jitter of the sampling clock.

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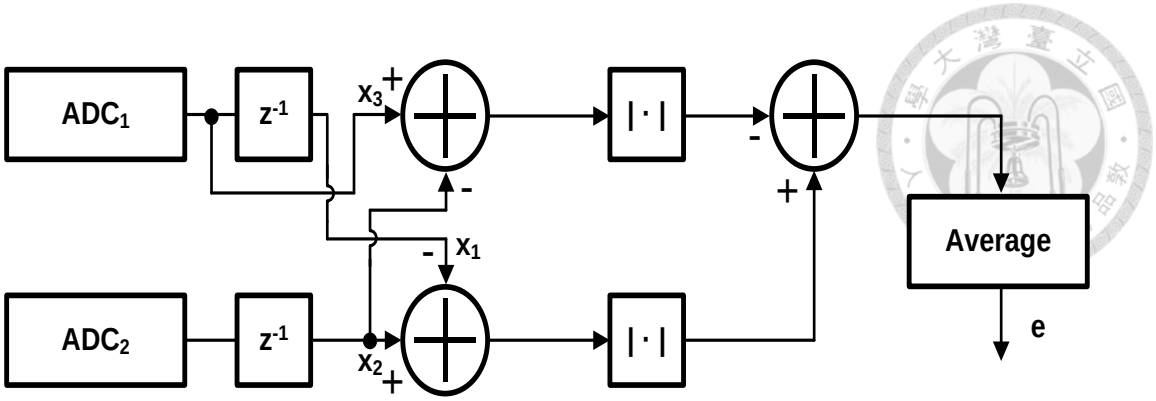

Fig. 2.14 Timing-skew detection method

2.5 Summary

In Chapter 2, how to quantify the performance of ADC is introduced and various types of ADC such as flash, SAR, and time-interleaved architecture mentioned in this thesis are also described. Detailed discussion about mismatch and calibration in time-interleaved architecture help to understand the proposed time-interleaved SAR ADC in Chapter 3.

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Chapter 3

Proposed Time-Interleaved SAR ADC

3.1 Introduction

As mentioned in Section 2.3, the time-interleaved architecture is popular for multi-GS/s conversion rate because it maintains excellent power efficiency. However, the input bandwidth of the time-interleaved architecture is a challenge because the Nyquist frequency is N times higher than that of a single-channel ADC.

On the other hand, as a single-channel architecture, SAR architecture shows great power-efficient in advanced CMOS technology. Therefore, the SAR ADC with time-interleaved technique is proposed in this thesis. In this chapter, the time-interleaved ADC architecture and an issue of bandwidth are introduced in Section 3.2. Section 3.3 presents the proposed time-interleaved SAR ADC and discusses the design consideration. Finally, Section 3.4 summarizes this work.

3.2 Time-Interleaved ADC Architecture

In this section, two conventional time-interleaved architectures are described. However, these architectures have limitation of the input bandwidth when the number of channel becomes large. Recently, grouping technique is a solution to overcome this issue. Three related prior works [9], [21], [23] are introduced to draw forth the proposed time-interleaved SAR ADC.

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3.2.1 One Rank Time-Interleaved Architecture

Fig. 3.1 shows the first conventional time-interleaved architecture and it is also called one rank time-interleaved architecture [32]. The sampling rate of a time-interleaved ADC is M times faster than that of sub-ADC where M is the number of sub-ADCs. Each sub-ADC has its track-and-hold (T/H) circuit which is triggered by corresponding clock phases (clki, i=1, 2…, M-1, M). This architecture achieves high sampling rate, but the problem of timing skew which is described in Section 2.4.1 degrades performance of ADC and needed to be solved.

The input bandwidth is an important consideration of time-interleaved ADC because it determines the operation speed and the allowable number of sub-ADCs. Two main factors which affect the input bandwidth are the input capacitance and the available settling time. According to [31], an approximation for the total input capacitance is

$$C_{IN} = N \cdot C_{sample} + M \cdot C_{switch} + M^2 \cdot C_{wire} \tag{3.1}$$

where C_{sample} is sampling capacitance of a single-channel ADC, C_{switch} is the capacitance of T/H circuit and C_{switch} consists of gata capacitances, C_{wire} is the capacitance of wire of a definite length, N is the number of T/H circuits which turn on at the same time, and M is the number of T/H circuits which connect the input. C_{sample} usually dominates the input capacitance. The input capacitance is proportional to N and the input bandwidth decreases as the input capacitances increases. Besides the input capacitance, the available settling time affects the requirement of input bandwidth. The available settling time is determined by the track-time of T/H circuits and duty cycle of clock phases.

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As shown in Fig. 3.2, the different time diagrams of clock phases cause different influences on the input bandwidth, where M is the number of sub-ADCs, and Fs is the sampling rate. Take an 8 GS/s 16-channel (M=16) TI ADC as an example, and two different time diagrams of clock phases are described. In Fig. 3.2(a), a number of 8 T/H circuits are in the sampling mode at the moment due to 50 % duty cycle of clock phases. An approximation for the total input capacitance is

$$C_{IN} = 8 \cdot C_{sample} + 16 \cdot C_{switch} + 16^2 \cdot C_{wire} \tag{3.2}$$

The third team is ignored for simplicity, and hence the input capacitance is 8 times larger than that of a single channel ADC. Due to 50 % duty cycle of clock phases, the available settling time is 1ns. The number of channels is limited due to the insufficient bandwidth. Moreover, this time diagram causes charge sharing between T/H switches and degrades the accuracy of the sampling signals. Therefore, this architecture is seldom used in recent years.

Another timing diagram is shown in in Fig. 3.2 (b). The duty cycle of clock phases is less than 6.25%. An available settling time of one period is less than 125 ps. This timing diagram ensures that only one input capacitance of sub-ADC is connect to the input at a time, lowering the input capacitance and enabling the higher number of channels. An approximation for the total input capacitance is

$$C_{IN} = 1 \cdot C_{sample} + 16 \cdot C_{switch} + 16^2 \cdot C_{wire} \tag{3.3}$$

However, as the number of channels increases, the duty cycle of clock phases decreases. The available time for sampling capacitance to settle is reduced. C_{switch} and C_{wire} still increase when the number of

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channels increases. The improvement of the bandwidth is still limited.

In conclusion, both timing diagrams of the conventional time-interleaved architecture have the problem of limited bandwidth if the number of channels becomes large.

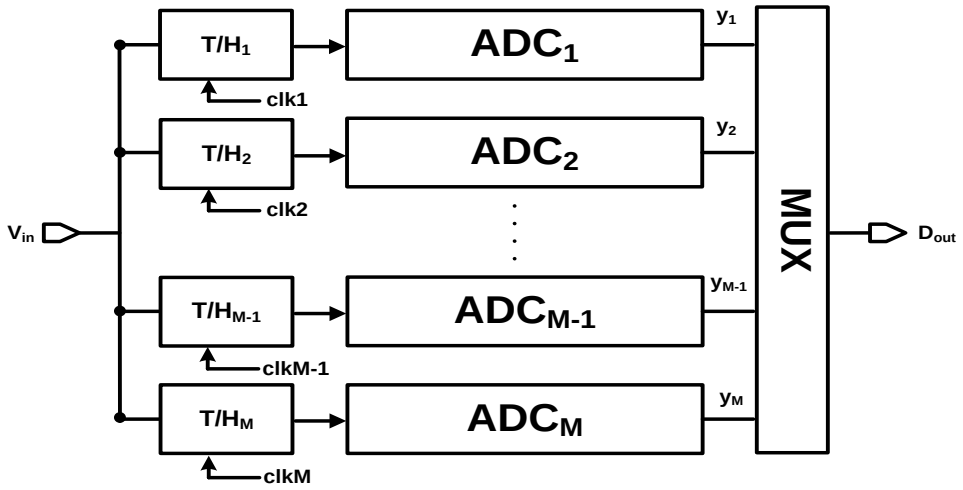
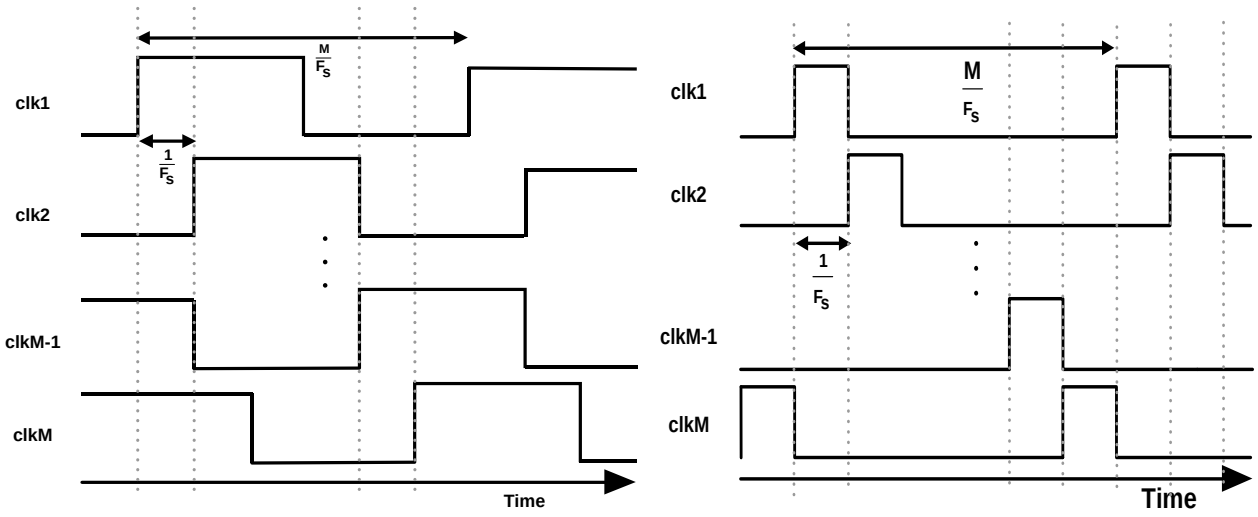


Fig. 3.1 One rank time-interleaved architecture



(a) (b)

Fig. 3.2 Timing diagram of (a) track-time of 50% duty cycle (b) track-time of $\frac{1}{M}$ % duty cycle

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3.2.2 Two Rank Time-Interleaved Architecture

For one rank time-interleaved architecture, timing skew mismatch between T/H switches results in error of sampling instants and degrades the SNDR of the ADC. To solve the timing skew issue, a two rank architecture also called the frontend sampler time-interleaved architecture [17]-[19], [33] is shown in Fig. 3.3. Fig. 3.4 shows the timing diagram. The frontend sampler operates at maximum sampling rate F_s with the same clock phase, sampling all the input signal. Then T/H circuits of sub-ADCs sample the constant DC signal from the frontend sampler. Thus, timing skew issue does not affect performance even if timing skew mismatch between sub-ADCs occurs. Because there are two rank of T/H, the concept of hierarchy is introduced and spread by other wok recently. It is discussed in Section 3.2.3.3.

The disadvantage is that the frontend sampler need to operate at the full sampling rate and the track time is $\frac{1}{2M}$ % duty cycle. The track time is half shorter than the one rank architecture shown in Fig. 3.2 (b). An approximation for the total input capacitance is

$$C_{IN} = 1 \cdot C_{sample} + M \cdot C_{switch} + M^2 \cdot C_{wire} \tag{3.4}$$

C_{switch} and C_{wire} also limit the bandwidth of fronted sampler when the channel increases.

Therefore, in this architecture, the frontend sampler limits the sampling rate of the ADC and the speed of the ADC cannot operate as fast as the one rank time-interleaved architecture.

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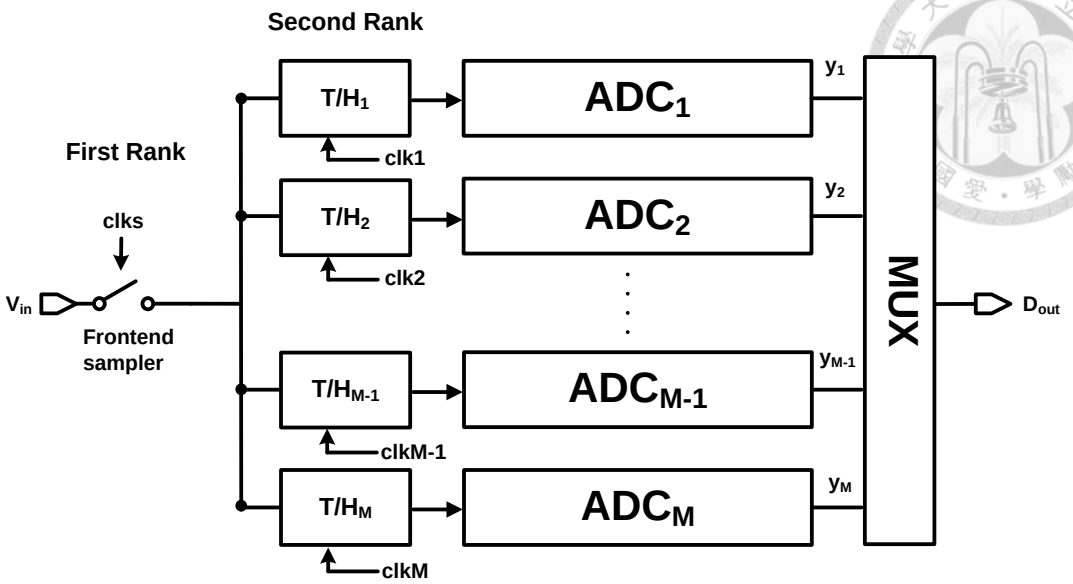

Fig. 3.3 Two rank time-interleaved architecture

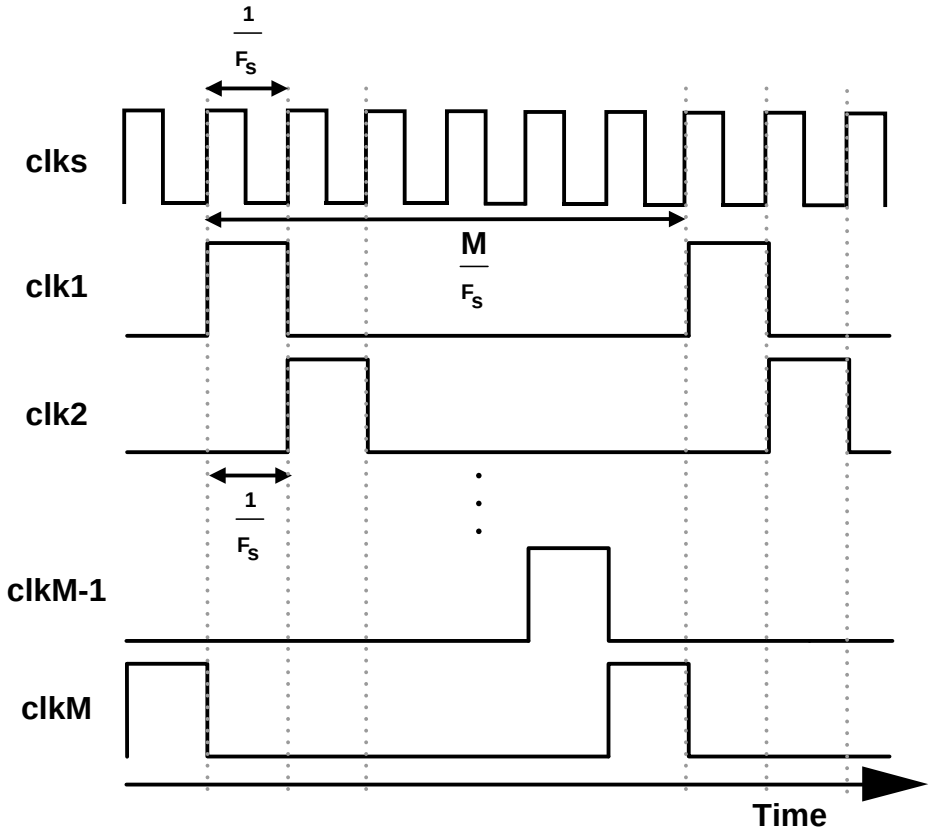

Fig. 3.4 Timing diagram of the two rank time-interleaved architecture

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3.2.3 Grouping Technique

Grouping technique is used to solve the input bandwidth of time-interleaved architecture when the number of channels becomes extensive. Fig. 3.5 is the basic time-interleaved architecture using grouping technique. There are totally $M \times N$ sub-ADCs which is divided into M groups. Each group usually has a frond-end sampler forwarding the input signal to the sampling capacitor of the sub-ADC. The parasitic capacitance at the output of Frond-end sampler is thus reduced drastically because a small number of parallel T/H circuits in a group. Like the timing diagram in Fig. 3.5, if only one T/H turns on at a time, the input capacitance is roughly the same as a single channel ADC. An approximation for the total input capacitance is

$$C_{IN} = 1 \cdot C_{sample} + M \cdot C_{switch} + M^2 \cdot C_{wire} \tag{3.5}$$

C_{switch} and C_{wire} are N times smaller than architecture without grouping technique.

Moreover, combining grouping technique with hierarchical concept makes time-interleaved architecture have a variety of architectures. Three related prior works [9], [21], [23] are introduced to draw forth the proposed time-interleaved SAR ADC.

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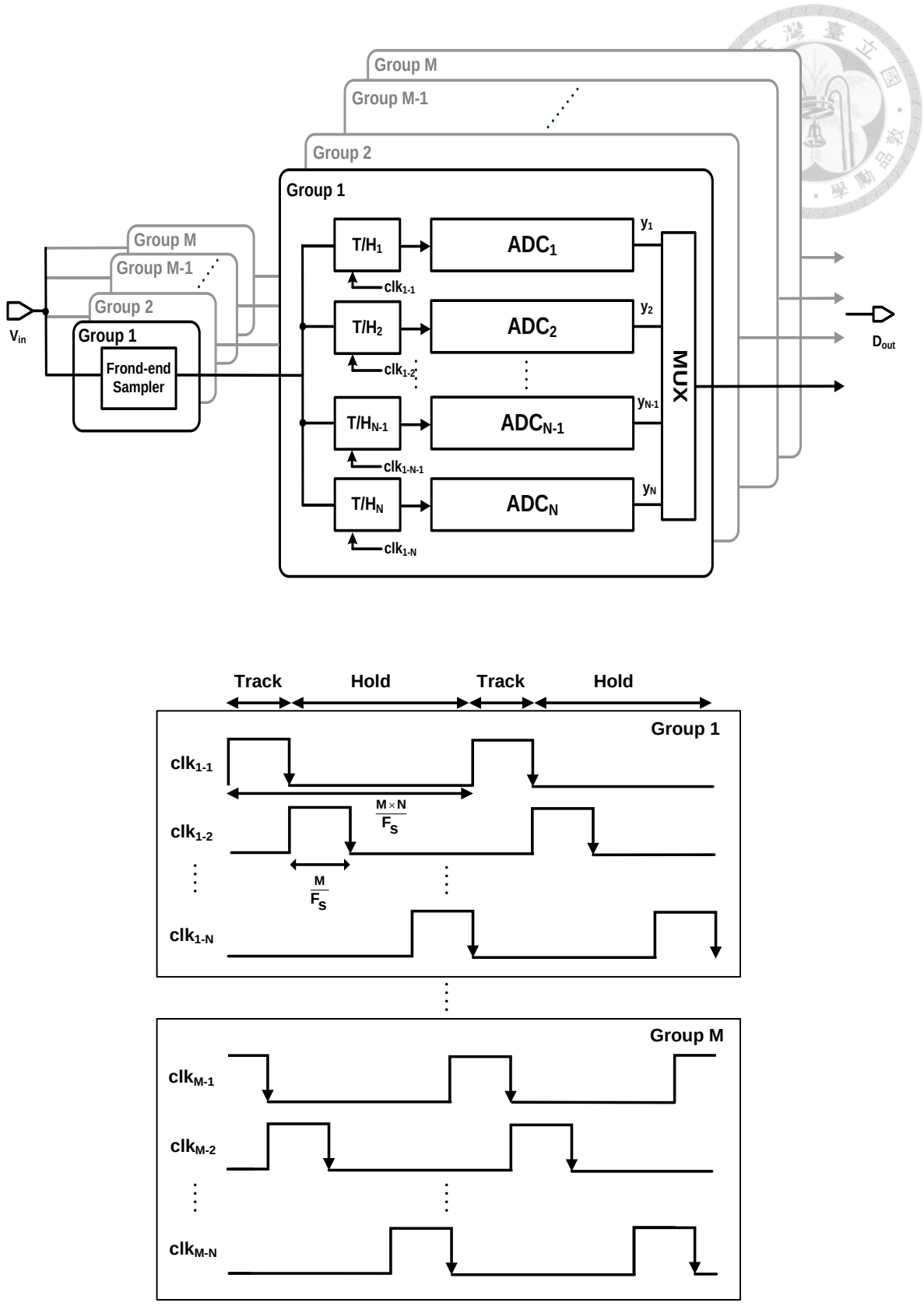

Fig. 3.5 Time-interleaved architecture using grouping technique and the time diagram

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3.2.3.1 Prior Work 1: The 64-Channel Time-Interleaved 10-Bit SAR ADC [9]

Prior work 1 aims at a high resolution ADC for GS/s rates. As resolution increases, the sampling capacitor also inevitably increases to solve thermal noise due to $\frac{C}{kT}$. This phenomenon causes the limitation of the number of channels when one rank or two rank time-interleaved architecture are used. Therefore, this prior work use a grouping concept to successfully interleave 64 SAR ADCs.

This prior work implemented a 64-channel 10-bit 2.6 GS/s time-interleaved SAR ADC in 65 nm CMOS. Fig. 3.6 shows ADC architecture and the timing diagram. 64 ADC units are arranged in four groups. Each group is partitioned into two domain: T/H and Quarter SAR ADC arrays. Each T/H drives a Quarter ADC array (QADC) which consists of 16 SAR ADCs. An on-chip calibration corrects gain and offset mismatches.

The operation using the time diagram is described as follows. A clock generator receives 2.6 GHz CLK and each Local clk generates 650 MHz clocks with 50% duty cycle for the operation of T/H. In addition, four QADCs receive 650 MHz clocks with 0°, 90°, 180°, 270°, which are used to generate local clocks for the operation of each SAR ADC. Each SAR ADC produces 10-bit data after 12 cycles, one for resampling input signal and 11 for quantization.

Partitioning ADC into 4 groups makes T/H and SAR ADC arrays separate interconnect from each group. It reduces parasitic capacitance of T/H from routing of connecting ADC arrays and clock circuit, enabling wide input bandwidth and allows the use of 64-channel ADCs. However, using one buffer to drive a QADC which has 16 ADC units is still difficult due to large output load. Accordingly,

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one SAR ADC is driven by one buffer to reduce load and 1-16 demultiplexer (demux) resamples the signal on the main sampling capacitor Cs to one buffer. The disadvantage is that large power is consumed due to a total of 64 buffers.

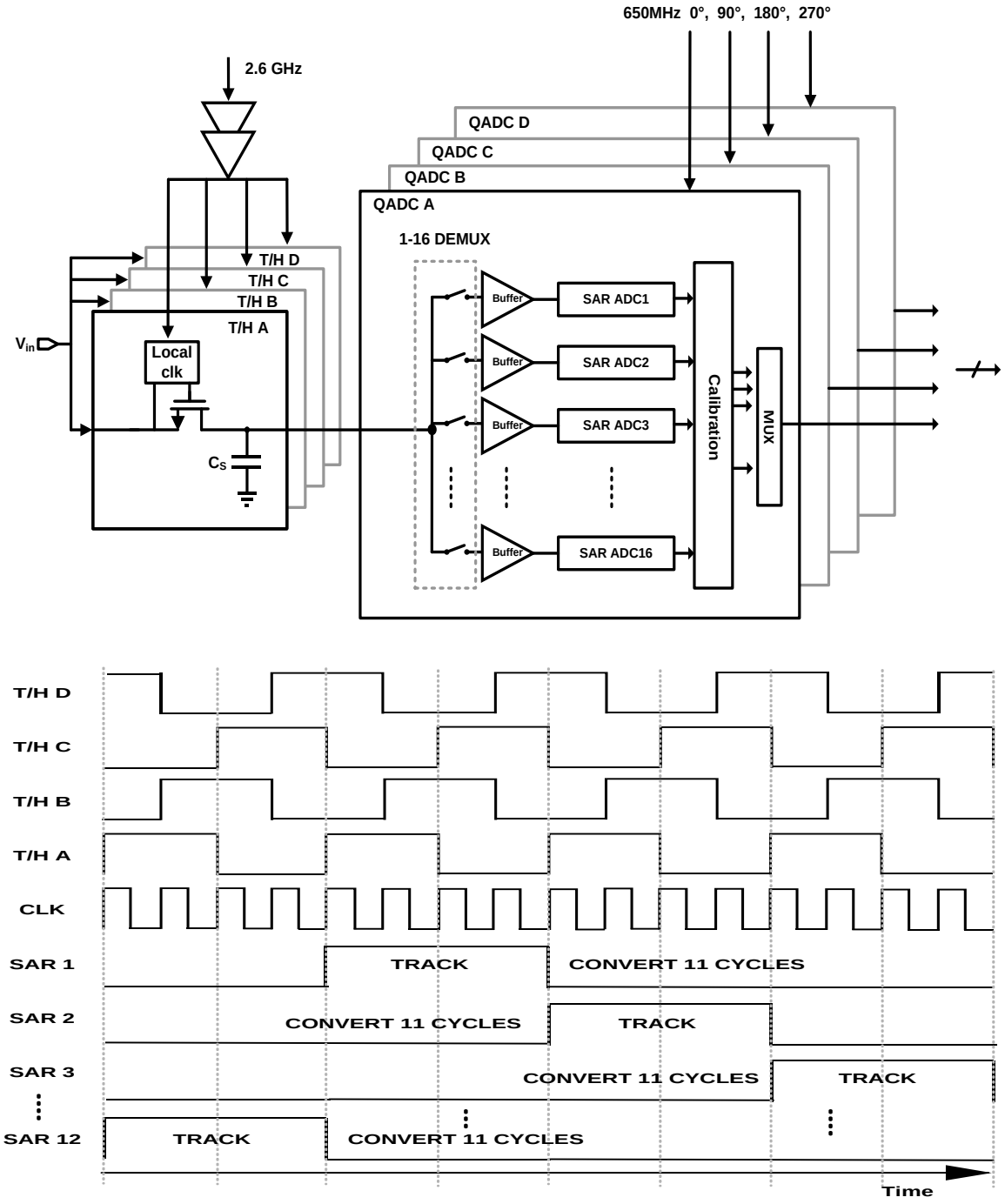

Fig. 3.6 ADC architecture and the timing diagram of prior work 1

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3.2.3.2 Prior Work 2: The 4-Channel Time-Interleaved 6-Bit Flash ADC [21]

Prior work 2 proposed the interleaved architecture to improve the input bandwidth limitation of the TI ADC. As shown in Fig. 3.7, T/H switches of 4-channel sub-ADCs are driven by one buffer G_1. In architecture 1, two clock phases such as clk1and clk2 overlap each other at the same time, corrupting the sampling input signal because charge sharing between two T/H switches causes an error in the sampling signal. For architecture 2 in Fig.3.7, this problem is solved by dividing T/H switches in two groups. And clock phases are exchanged. For example, clk1 and clk3 are in one group now and they do not overlap each other. As a result, each group is driven by one buffer G_1 and charge sharing does not occur. Another advantage is that the track-time of T/H switches becomes 50% duty cycle by grouping sub-ADCs. The available settling time is prolonged. The concept of architecture 2 is used in this work.

Fig. 3.8 shows the architecture of TI ADC in prior work 2. This prior work implemented a 4-channel 6-bit 10.3 GS/s time-interleaved flash ADC in 40 nm CMOS. The ADC comprises of two frontend variable gain amplifiers VGAs (G1) and 4-channel sub-ADCs with their own VGAs (G2). A G1 provides coarse gain control at high bandwidth, while a slower G2 provides fine gain control. Each G1 drives a pair of T/H switches that are triggered by complementary 2.575-GHz clock phases. Since only small capacitance is used in T/H switch's output, G1 achieves high tracking bandwidth allowably. Then, each G2 connects a T/H circuit and drives the sub-ADC's input load. However, both buffer G1 and G2 have programmable resistor array that vary gain to calibrate gain mismatch. G2

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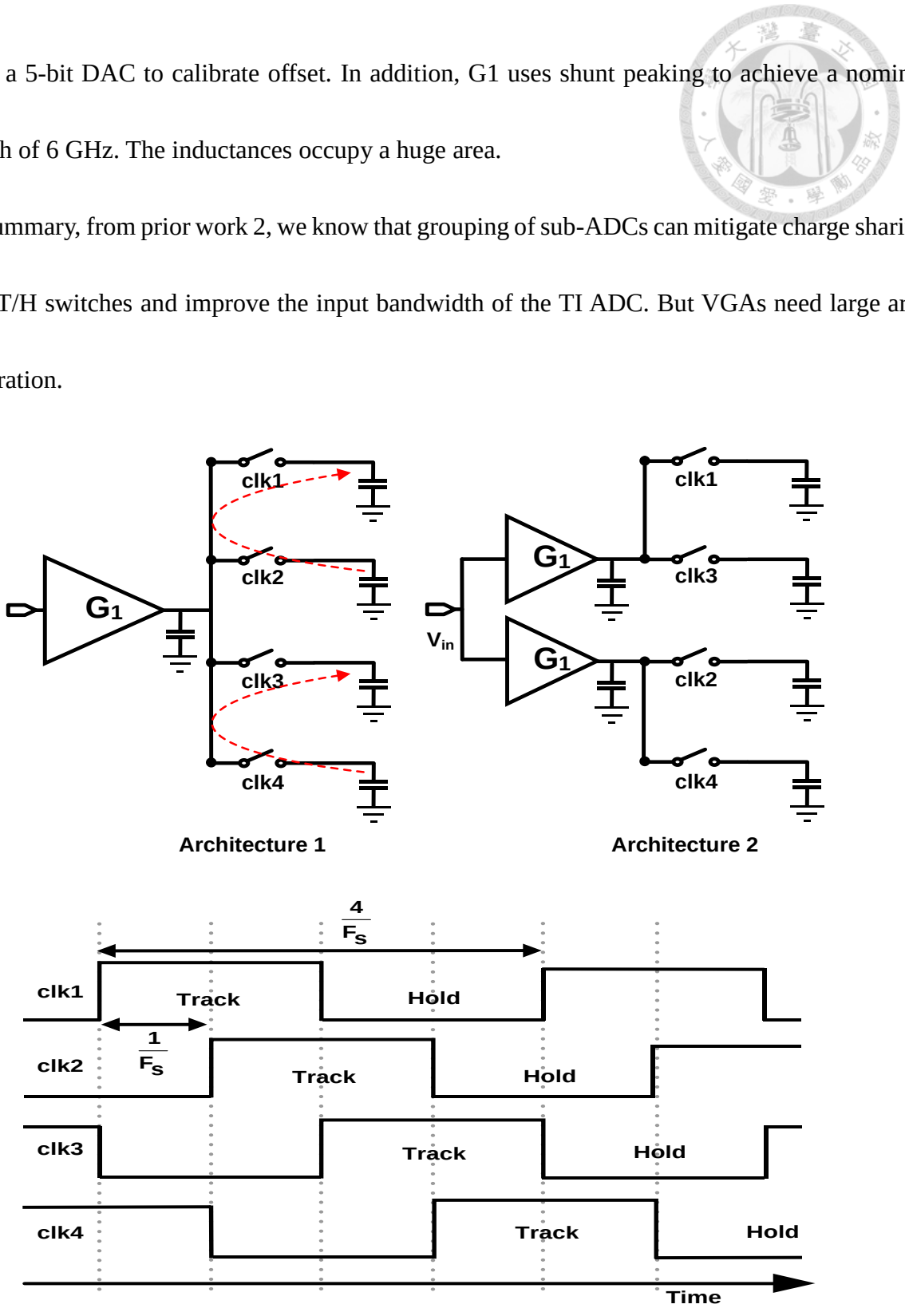

Fig. 3.7 Charge sharing problem between T/H switches

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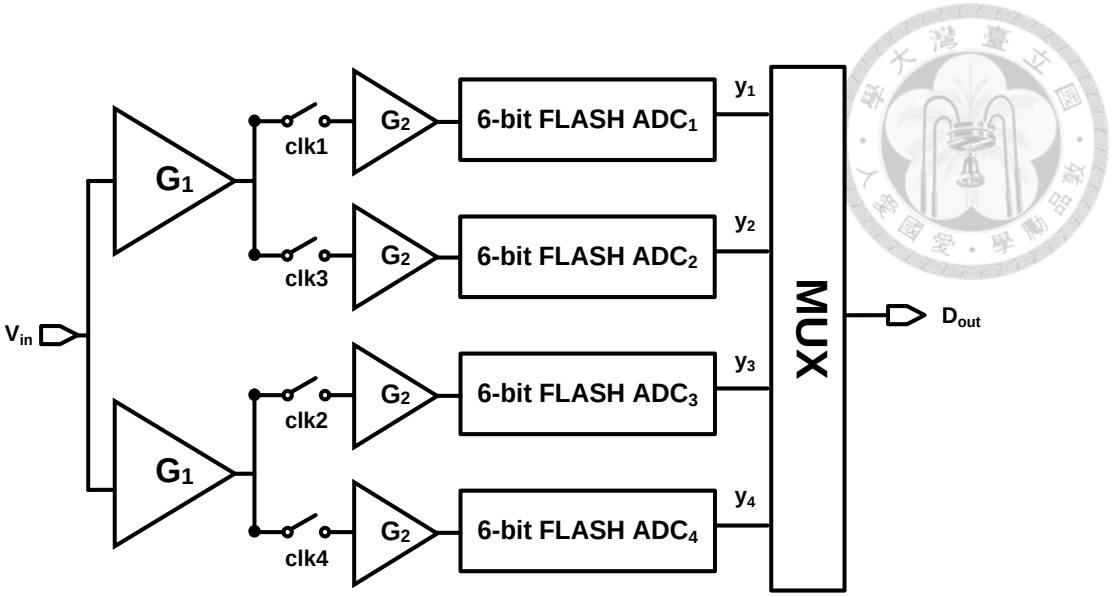

Fig. 3.8 Block diagram of prior work 2

3.2.3.3 Prior Work 3: The 32-Channel Hierarchical Sampling Time-Interleaved 7-Bit SAR ADC [23]

As discussed in Section 3.2.2, as the number of sub-ADCs becomes large, it is challenging to drive the overall sub-ADCs at high frequency because the enormous sampling and parasitic capacitances limit the bandwidth. A broadband input buffer may be added to increase bandwidth. Nevertheless, this buffer has to consume excessive power to meet high demand [24].

Prior work 3 proposed a hierarchical sampling architecture combined with the grouping technique to overcome these issues if 32 sub-ADCs are used. This prior work implemented a 32-channel 7-bit 12.8 GS/s time-interleaved SAR ADC in 65 nm CMOS. The architecture and timing diagram are shown in Fig. 3.9. The hierarchical sampling architecture consists of three rank of samplers (Rank 1-3). Each rank of samplers includes the buffer, T/H switches, and sampling

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capacitance. First, Rank-1 sampler is adopted to sample the input signal when phase Φ_1 triggers the T/H circuit. As described in Section 3.2.2, the output voltage of Rank-1 sampler is constant during the hold time. As a result, the timing mismatch caused in the Rank-2 and Rank-3 samplers does not degrade the performance. However, Rank-1 sampler still needs a lot of effort such as power and area to achieve high bandwidth.

The input bandwidth requirements in the Rank-2 and Rank-3 samplers are also alleviated due to the constant voltage of signal. Next, the Rank-2 sampler is triggered by clock phase $\Phi_{2A<1:4>}$. In this stage, through proper arrangement of clock phases, the buffer only need to drive one sampling capacitance at a time. Finally, in a Rank-3 stage, 32-channel sub-ADCs are divided into 4 groups. Each group has 8-channel sub-ADCs which are driven by one buffer. The previous held sampled signal is then buffered and re-tracked by the T/H circuit of the sub-ADC. Like the Rank-2 sampler, Rank-3 sampler also drives one sampling capacitance at a time. Therefore, in Rank-2 and Rank-3 stage, parasitic and sampling capacitances are greatly reduced. The input bandwidth of the ADC is not limited.

In summary, this work use three rank architecture combining with grouping technique to lower the requirement of input bandwidth if the large number of sub-ADCs is required. In addition, unlike the prior work 1, the number of buffers is reduced to six with the aid of three rank. However, the input bandwidth of Rank-1 sampler consist of a buffer and T/H is still a problem and G_1 consumes huge power.

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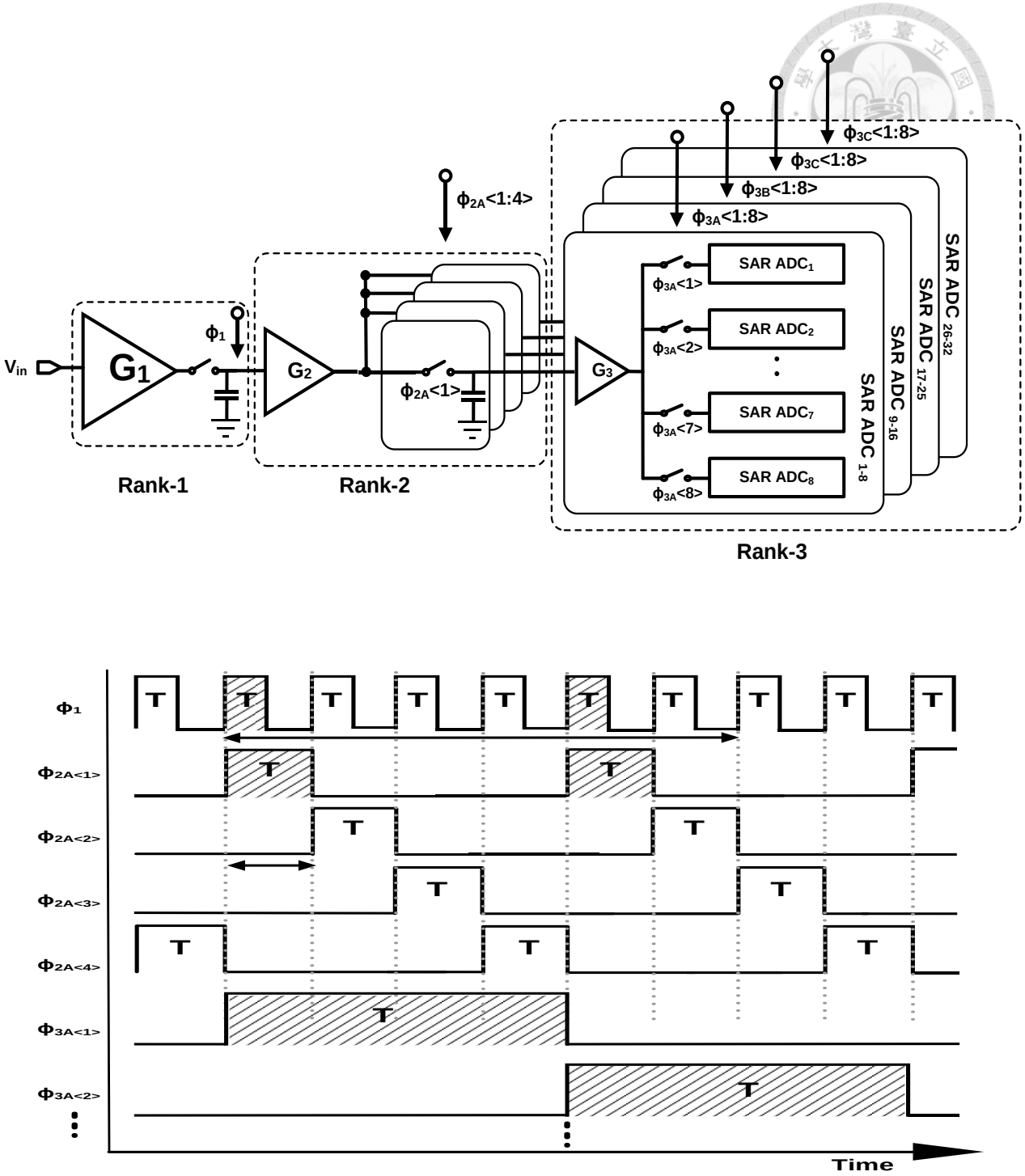

Fig. 3.9 Architecture and timing diagram of prior work 3

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3.3 Proposed Time-Interleaved SAR ADC

According to the discussion of time-interleaved architecture in Section 3.2, we summarize some techniques briefly. One rank architecture is the simplest way to implement a time-interleaved technique. However, it has both problems of the input bandwidth and timing skew. Next, two rank architecture which pluses a front-end sampler to solve the timing skew issue. The disadvantage is that the front-end sampler should operate at the full sampling rate, and its track-time is worse than one rank architecture. Both architectures have limitation of the number of interleaved channels when ADC extends to multi-GS/s operation. On the other hand, recently, grouping technique is proposed to overcome this issue.

Prior work 1 and work 2 both have the technique that groups sub-ADCs into several section. The input load is thus reduced and become unrelated to the number of whole channels. Accordingly, accomplishing the demand of high input bandwidth is much more effortless than the conventional architecture. Nevertheless, how to grouping sub-ADCs depends on the number of channels and the specifications of ADC. For example, Prior work 1 still needs 64 buffers to drive sub-ADCs because there are still 16 sub-ADCs in a group. The number of sub-ADCs in a group is still large. Prior work 2 only has 4-channel ADCs, so grouping ADC is simple. But the design of VGA is complicated and VGA consumes huge area due to calibration and the inductances. The architecture in prior work 3 combines the hierarchy with grouping technique. There rank of samplers and four group of sub-ADCs are determined to confront a large load from 32 sub-ADCs. Nevertheless, the operation of Rank-1

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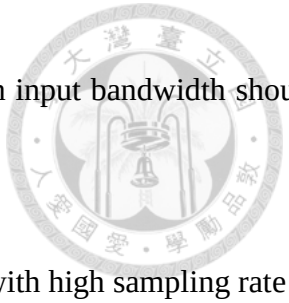

stage is still like the conventional two rank architecture. Acquiring enough input bandwidth should pay for excessive power consumption.

Look back to our goal, we aim to implement a low power 6-bit ADC with high sampling rate of greater than multi-GS/s. The SAR architecture is chosen as a sub-ADC for its high power efficiency in the advanced CMOS process. Furthermore, time-interleaved architecture extends this advantage properly. On the basis of the specification, we interleave 16-channel SAR ADCs and achieve the goal by combining the front-end input buffers and the grouping technique for time-interleaved architecture.

With a 16-channel time-interleaved ADC, different hierarchical architecture and grouping technique affect performance. The relationship is discussed as follows. It may provide the best optimum architecture for the 16-channel time-interleaved ADC. Table. 3-1 summarizes this relationship. We define M is the number of sub-ADCs, H is the number of hierarchy and G is the number of groups. t_{settle} is the worst time for the input buffer to settle; Duty Cycle is the ratio of the sampling time and the conversion time for a sub-ADC; and Buffer is the number of the needed buffers. For example, if H=2, the architecture is like the two rank architecture and t_{settle} is too short to meet the settling requirement. Thus, H=2 is not considered as a chosen architecture. Because the ADC only has 16-channel, H=3 or 3-rank architecture like prior work 3 is unnecessary in this architecture. When H=1 and G=8, t_{settle} is longest but it needs 8 buffers and suffers from higher power consumption. On the other hand, if G is 2, the duty cycle for the sub-ADC is unbalanced because the track-time is still short and the conversion time is too long for the 6-bit SAR ADC. It may has idle time for conversion.

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Therefore, the most favorable architecture is H=1 and G=4. In this choice, t_{settle} is available for input buffers to settle and 25% duty cycle is balanced for the operation of sub-ADC.

Table 3-1 Comparison of different ADC architecture when M = 16

M	H	G	t_{settle}	Duty Cycle	Buffer
16	1	2	$2T_s$	12.5%	2
16	**1**	**4**	**$4T_s$**	**25%**	**4**
16	1	8	8T	50%	8
16	2	2	$0.5T_s$	12.5%	3
16	2	4	$0.5T_s$	25%	5

The proposed time-interleaved SAR ADC and timing diagram are shown in Fig. 3.10. The architecture is composed of 16-channel SAR ADCs, 4 groups of front-end buffers, a clock generator and a multiplexer (MUX) circuit. In this design, the input signal is sampled by 4 groups of source followers (SF). Each SF drives one group of ADCs which consist of 4 SAR ADCs. Each T/H circuit of the sub-ADC samples the signal forwarded by the SF with the 25% duty cycle clock. Then, SAR ADCs of each group convert the input signal to 7-bit output data with 1-bit redundancy. Output data from each ADC are combined by the multiplexer (MUX) and decoded to six binary bits. Calibrations of the offset and gain mismatch between channels are performed off-chip. The timing-skew mismatch is also detected off-chip and then the delay cells of the clock generator is adjusted to suppress the timing skew.

A timing diagram is shown in Fig. 3.10. In GROUP 1, the SAR ARC_1 samples the input signal

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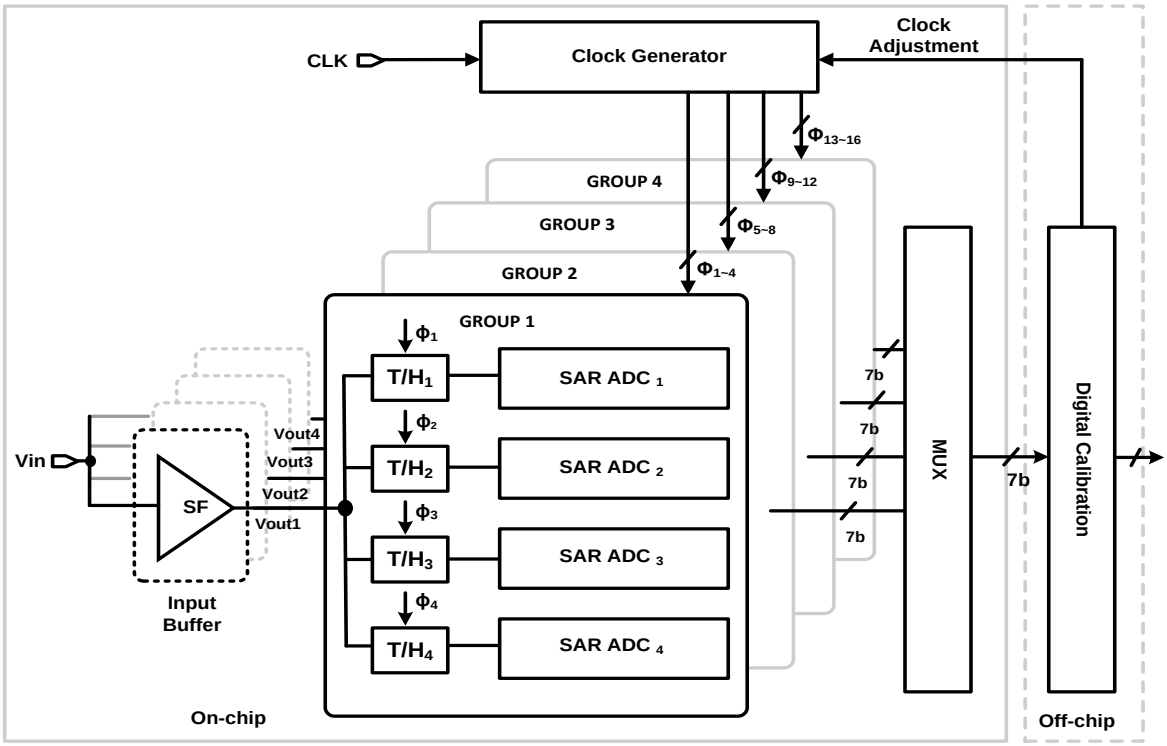
when Φ_1 is high, starting conversion when Φ_1 is low. Similarly, other SAR ADCs operates sequentially. Although sampling phases overlap between groups, front-end SFs separate the path of the charge sharing between T/H circuits. In other words, by grouping sub-ADCs, only one T/H circuit of the SAR ADC samples the input signal at the same time in a group. Thus, it avoids the problem of the charge sharing between sub-ADCs with the proper duty cycle of clock phase. It solves the distortion of the sampling signal. An approximation for the total input capacitance is

$$C_{IN} = 1 \cdot C_{sample} + 4 \cdot C_{switch} + 4^2 \cdot C_{wire} \tag{3.6}$$

The input capacitance is nearly the same as a single-channel ADC. Consequently, buffers' load greatly decreased even 16-channel is adopted. Another benefit is that the 25% duty cycle clock used also fits the operation of the SAR ADC.



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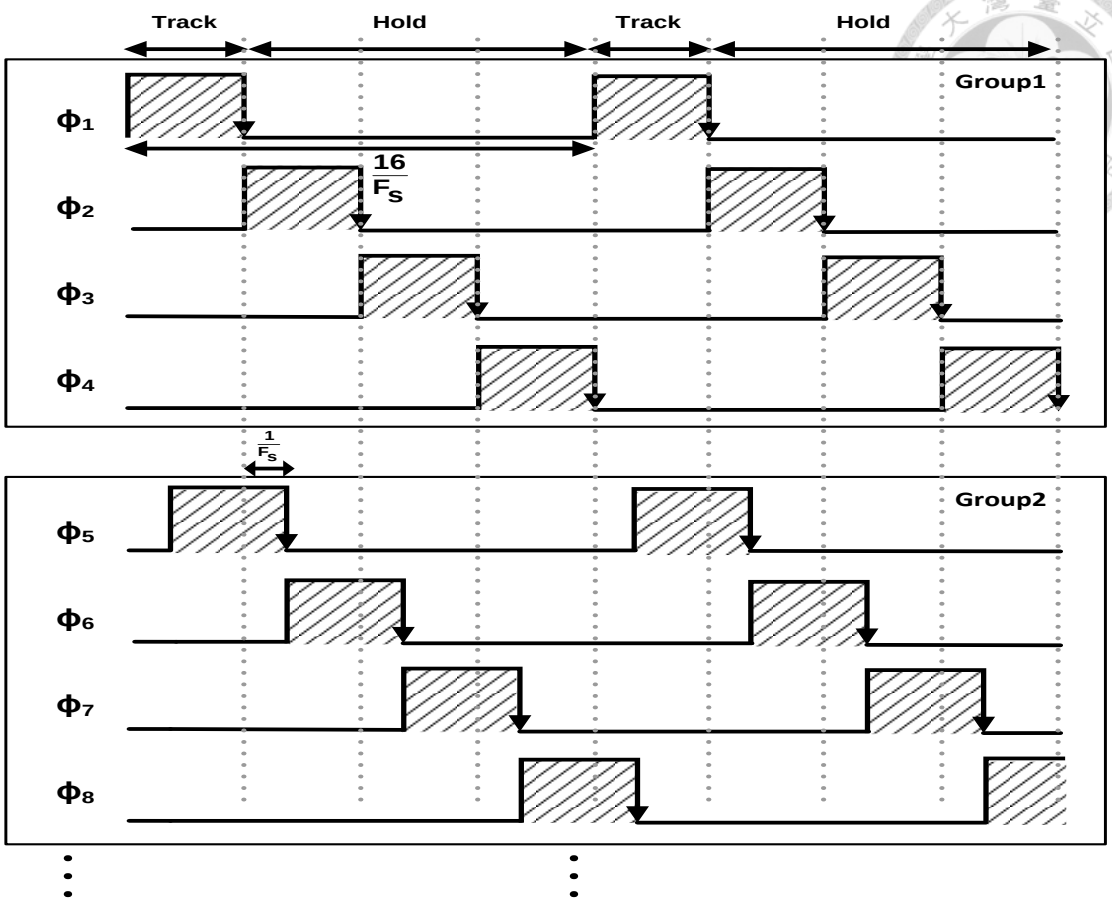

Fig. 3.10 Architecture and timing diagram of the proposed time-interleaved SAR ADC

In sub-ADC, the 6-bit SAR ADC is shown in Fig. 3.11. It is composed of transmission gate switches, arbitrary weight capacitor array (AWCA), a comparator, and SAR logic. Top-plate sampling and the monotonic switching are used for its simple digital logic and low power consumption. Although the monotonic switching may cause a signal-dependent dynamic offset, the AWCA [25] technique adopted solves this problem. Since the AWCA is based on the non-binary concept, one additional comparison is performed in 6-bit SAR ADC.

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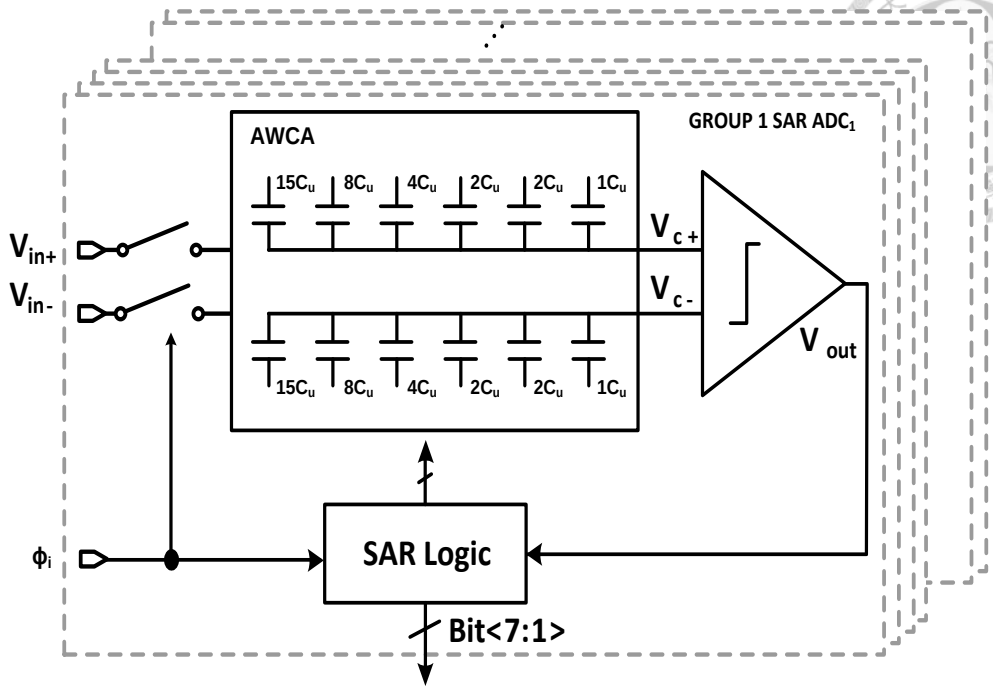

Fig. 3.11 Architecture of sub-ADC

3.3.1 Design Considerations

In this section, we discuss the design consideration of the proposed time-interleaved SAR ADC. First, we analyze the input bandwidth of the ADC in Section 3.3.1.1. Second, mismatches in this design is considered in Section 3.3.1.2 and 3.3.1.3. Finally, several techniques in single-channel SAR ADC are described in Section 3.3.1.4.

3.3.1.1 Input Bandwidth and Settling Time Requirement

As described in Section 3.3, front-end buffers are used to drive sub-ADCs and become a key point whether the ADC have enough bandwidth.

This work chooses the source follower, rather than the operational amplifier (OPAMP) for

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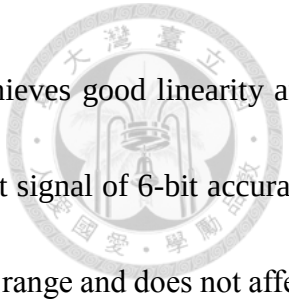

several reasons although the OPAMP based closed-loop configuration achieves good linearity and gain desensitization. First, the open-loop buffer that accomplishes the input signal of 6-bit accuracy is enough in this design. Second, the buffer's gain only changes the signal's range and does not affect linearity severely so the unity-gain buffer based closed-loop configuration is unnecessary. Finally, it is very hard to design an OPAMP based closed-loop residue amplifier that conforms to the require bandwidth in the gigahertz range because voltage headroom and output resistance are small in 40 nm CMOS technology. Instead, the open-loop source follower offers a higher bandwidth and faster settling time easily when compared to the OPAMP based closed-loop residue amplifier.

The PMOS source follower depicted in Fig. 3.12(a), where C_L is the equivalent capacitance load contributed mainly by the AWCA of the SAR ADC. The bulk of the PMOST is tied to the source, which eliminates the nonlinearity due to body effect. Using the ideal current source replaces the bias circuit of the source follower to simplify analysis. As the small-signal model is shown in Fig. 3.12(b), the output resistance of M_1 is r_{O1}. The output resistance of current source is r_{O2}. It is implemented by cascode PMOS current source in practice. .

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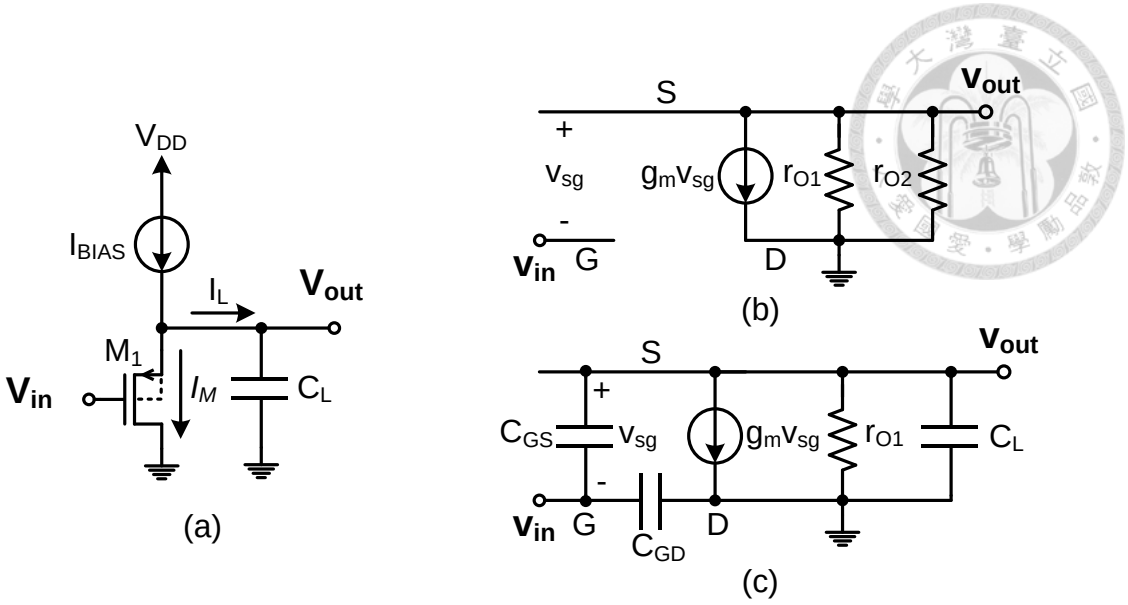

Fig. 3.12 (a) Source follower with ideal bias current, its (b) small-signal model, and its (c) high-frequency equivalent model

The V_{out} of source follower is expressed as:

$$v_{out} = -g_m(v_{out} - v_{in})(r_{O1} // r_{O2}) \tag{3.7}$$

Since r_{O2} is larger than r_{O1}, it follows that

$$\frac{v_{out}}{v_{in}} = \frac{g_m(r_{O1} // r_{O2})}{1 + g_m(r_{O1} // r_{O2})} \approx \frac{g_m r_{O1}}{1 + g_m r_{O1}} = 1 - \frac{1}{1 + g_m r_{O1}} \tag{3.8}$$

where $g_m r_{O1}$ is the intrinsic gain of transistor M_1. Hence, the gain of the source follower is roughly smaller than 1, but this situation does not cause influence on the conversion of the ADC.

The input bandwidth of the source follower dominantly determines the performance of the ADC at high input frequency. It is obtained through high-frequency equivalent model shown in Fig. 3.12 (c). By applying Kirchhoff's current law at output node (V_{out}), we add up all of the current:

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$$v_{sg}C_{GS}s + g_m v_{sg} + v_{out}(sC_L + \frac{1}{r_{O1}}) = 0 \tag{3.9}$$

It follows that

$$v_{sg} = -\frac{sC_L + \frac{1}{r_O}}{g_m + C_{GS}s} v_{out} \tag{3.10}$$

And

$$v_{in} = v_{out} - v_{sg} \tag{3.11}$$

Substituting equation (3.10) into equation (3.11), we have

$$\frac{v_{out}}{v_{in}} = \frac{g_m + C_{GS}s}{s(C_L + C_{GS}) + g_m + \frac{1}{r_{O1}}} \tag{3.12}$$

Consequently, the unity-gain bandwidth is

$$\omega_u = \omega_{3dB} \approx \omega_p = \frac{g_m + \frac{1}{r_{O1}}}{C_L + C_{GS}} \approx \frac{g_m}{C_L + C_{GS}} \tag{3.13}$$

Next, we calculate the requirement of the frond-end circuit on the basic of the input bandwidth and the settling time. Fig. 3.13 shows a first-order RC model of the frond-end circuit and the bandwidth at V_{out} is

$$\omega_{vout} = \frac{1}{(R_O + R_{on})C_{IN}} \tag{3.14}$$

where R_O is the output impedance of the source follower and R_O is $\frac{1}{g_m}$, R_{on} is an equivalent on-resistance of the T/H switch, and C_{IN} is the total input capacitance.

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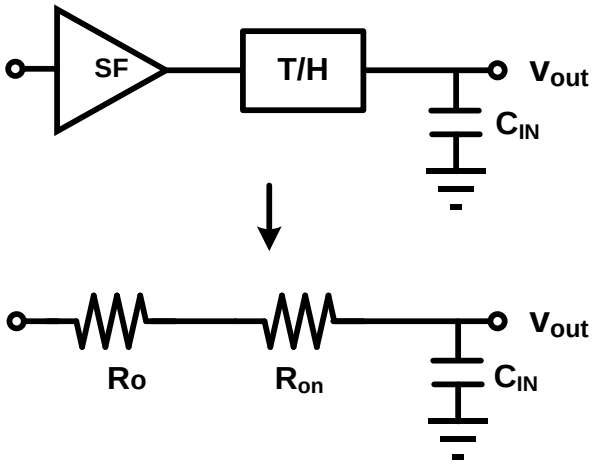

Fig. 3.13 The RC model of the frond-end circuit

The setting error should less than $\frac{1}{2}V_{LSB}$ to attain the required accuracy. Hence, the settling time of the frond-end circuit is defined as the required time that V_{out} reaches to within $\frac{1}{2}V_{LSB}$ of its final value and it is written as:

$$V_{out}(t=t_{settle})=V_{final}(1-e^{t_{settle}/\tau})\geq V_{final}(1-\frac{1}{2^{n+1}}) \tag{3.15}$$

where t_{settle} is the required settling time, V_{final} is the final voltage of V_{out}, τ is the RC time constant, and n is the resolution of the ADC.

Rearrange (3.15), we have

$$t_{settle}\geq(n+1)\cdot\tau\cdot\ln(2) \tag{3.16}$$

In fact, t_{settle} is determined by the track-time of clock phases and it is fixed. According to the value of t_{settle}, we know the required input bandwidth of the frond-end circuit and ensure the goal of design. By rearranging (3.16) and substituting $\tau=\frac{1}{\omega_{vout}}$, the required input bandwidth is

$$\omega_{vout}=2\pi f_{vout}\geq\frac{1}{t_{settle}}\cdot(n+1)\cdot\ln(2) \tag{3.17}$$

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For example, in this work, the maximum settling time is $T_s \times 16 \times \frac{1}{4}$ due to 16-channels and duty cycle clock is 25% where T_s is the sampling period. Assuming that the ADC operate at 8 GS/s sampling rate, T_s is 125 ps and the maximum settling time is 500ps. By substituting $n=6$ and t_{settle} =500 p into (3.14), the required bandwidth of the front-end circuit is approximately 1.55 GHz.

Table 3-2 compares the input bandwidth requirement of time-interleaved architecture mentioned in Section 3.2 and 3.3. In these architectures, we assume a 6-bit 16-channel TI ADC under the sampling rate of 8 GS/s and clock phases do not overlap each other. Consequently, one rank time-interleaved architecture in Fig. 3.2(b) only has 6.25% duty cycle and the available settling time is 125 ps. According to (3.14), the required input bandwidth is 6.2 GHz. Two rank time-interleaved architecture has the shorter available settling time due to its frontend sampler and the required input bandwidth is 12.4 GHz. On the other hand, the proposed architecture has the lowest requirement of input bandwidth. The available settling time is 500 ps and the requirement of input bandwidth is only 1.55 GHz. This requirement of the input bandwidth in this work is 4 time lower than that of one rank time-interleaved architecture and 8 time lower than that of two rank time-interleaved architecture. It effectively makes the design of the front-end circuit easier than other architectures.

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Table 3-2 Comparison of the required input bandwidth for time-interleaved architecture

Architecture	Available settling time (ps)	Required input bandwidth (GHz)
Proposed	500	1.55
One rank (Fig. 3.2b)	125	6.2
Two rank	62.5	12.4

3.3.1.2 Offset and Gain Mismatch Calibration

As mentioned in Section 2.4, in time-interleaved architecture, the problem of mismatch among sub-ADCs should be considered and eliminated. In our work, offset mismatch is attributed to 4 groups of source followers and the comparator of the SAR ADC among 16-channels. The sources of gain mismatch are mainly the same as that offset mismatch. Moreover, other major sources of gain mismatch are from reference voltage mismatch and capacitive DACs. Therefore, these mismatches need to be calibrated.

The effort of the calibration is simple. We use the method described in Section 2.4.1. It follows that each sub-ADC's offset is detected by calculating long term mean of its output with a quasi-stationary input signal such as sinusoidal wave. Then the offset value is subtracted from its respective output [15], [18]-[19]. Likewise, the gain calibration method we use is described in Section 2.4.2. Each sub-ADC's gain is detected by long term average of each absolute output with sinusoidal wave and then gain mismatch is corrected by dividing each sub-ADC output's estimated gain in digital domain [15], [18]-[19].

Fig. 3.14 shows 2-channel TI ADC as an example. According to the above algorithm, $offset_2$ is

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the estimated offset mismatch of SAR ADC_2 relative to SAR ADC_1. Then, y_{2_cal1} represents the offset-calibrated digital output of SAR ADC_2. Next, by normalizing y_{2_cal1} with respect to y_1, the final calibrated digital output y_{2_cal2} is acquired. This calibration is realized via MATLAB for its simplicity.

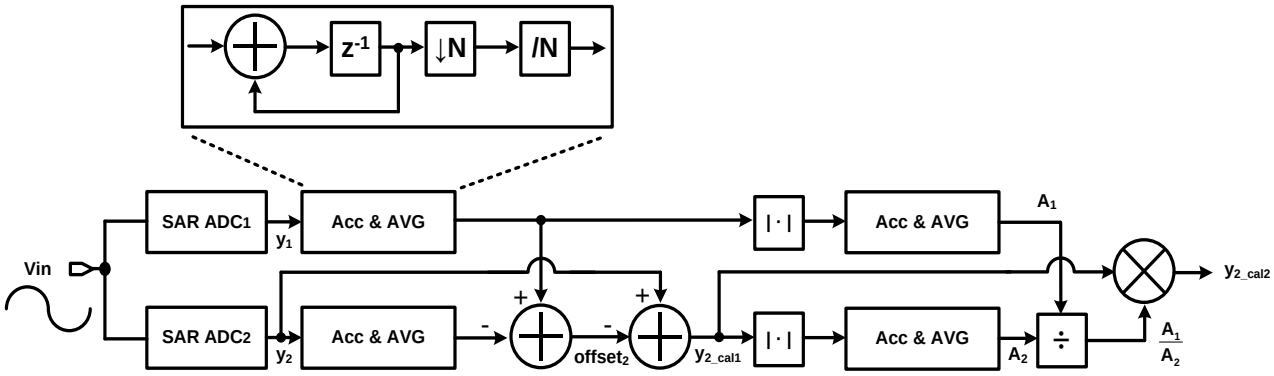

Fig. 3.14 The block diagram of offset and gain mismatch calibration

3.3.1.3 Timing Skew Mismatch Calibration

After offset and gain mismatches are calibrated, the timing skew should be detected and corrected. We use the approach based on the correlation between the probability density of zero-crossing and the difference of the ADC output [26].

Fig. 3.15 is an example how to calculate the difference of the correlation ε. The difference of the correlation ε is a function of the timing mismatch between SAR ADC_1 and SAR ADC_2. Assuming that the input is a stationary signal with zero mean such as sinusoidal wave and SAR ADC_2 samples the input signal x_2 at t_2, which is skewed by ΔT. Now, we calculate the cross-correlation between the difference y_2-y_1 and the sign signal S_2, obtaining C_1 which is proportional to timing skew ΔT.

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Similarly, C_2 is acquired by the same computation. The difference of the correlations C_1 and C_2 is ε. The long term accumulation of ε would represents the relative skew. Then, we can adjust the delay cells of the clock phase Φ_1 to correct the timing skew ΔT.

The detailed explanation is as follows. The difference of digital output of ADCs between adjacent channels is

$$a_i = y_i - y_{i+1} \tag{3.15}$$

where i refers the channel number.

Then, the sign signal S_i belongs to {-1, 0, +1}, which is obtained by zero-crossing detection (ZCD). When zero-crossing (ZC) occurs, S_i produces either -1 or +1. When ZC does not occur, S_i is 0. It is written as

$$\begin{aligned} S_{i+1} &= sign(y_i - y_{i+1}) \\ &= \frac{y_i - y_{i+1}}{|y_i - y_{i+1}|} \end{aligned} \tag{3.16}$$

Next, the cross-correlation between S_{i+1} and a_i according to the definition is

$$\begin{aligned} C_i &= E[S_{i+1} \times a_i] \\ &= E[S_{i+1} \times (y_i - y_{i+1})] \end{aligned} \tag{3.17}$$

Substitute (3.16) into (3.17), then

$$\begin{aligned} C_i &= E[(\frac{y_i - y_{i+1}}{|y_i - y_{i+1}|}) \times (y_i - y_{i+1})] \\ &= E[|y_i - y_{i+1}|] \end{aligned} \tag{3.18}$$

In accordance with the property of the ZC [13], the ZC probability between y_1 and y_2 is proportional to the sampling interval T_s. If timing skew ΔT occurs and then sampling interval changes

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into $T_s+\Delta T$, the C_i becomes

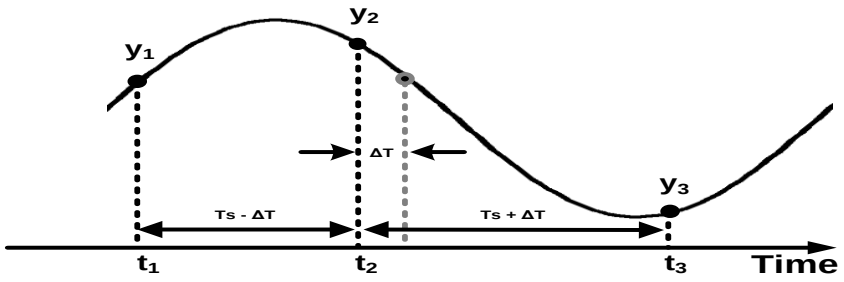
$$C_i = E[|y_i - y_{i+1}|] \propto \sum |y_i - y_{i+1}| \propto [2 f_i \times (T_s + \Delta T)] \tag{3.19}$$

where $2 f_i \times (T_s + \Delta T)$ is the probability if zero-crossing.

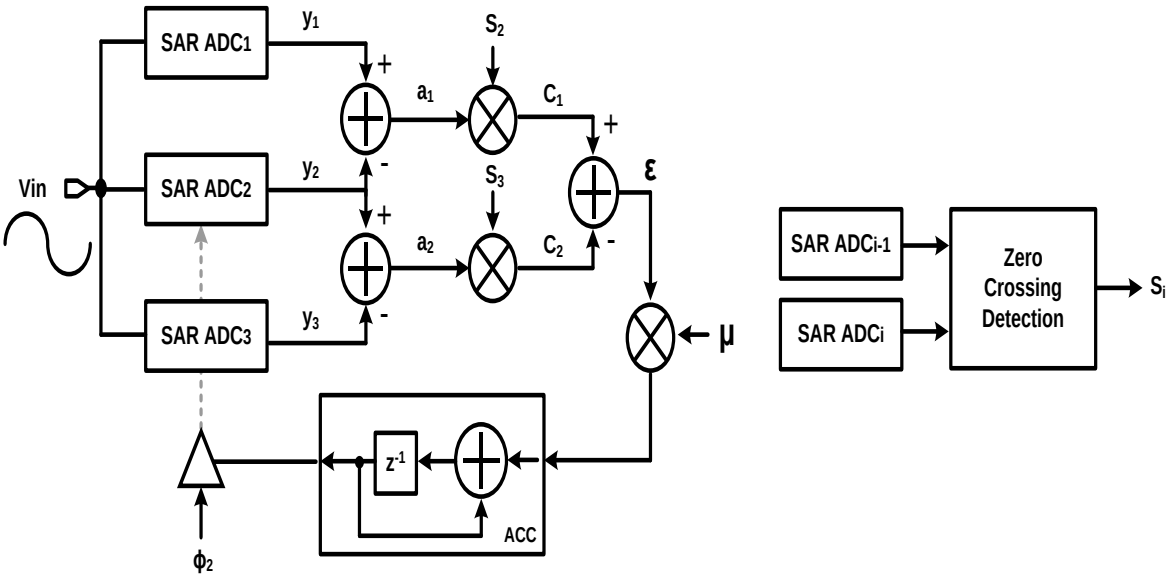
Eventually,

$$\begin{aligned} \varepsilon &= C_{i-1} - C_i \\ &= E[|y_{i-1} - y_i|] - E[|y_i - y_{i+1}|] \end{aligned} \tag{3.20}$$

ε becomes the relative timing skew between adjacent channels.



(a)



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(b)

Fig. 3.15 (a) Sampling waveform of TI ADC (b) block diagram of the timing skew mismatch detection

3.3.1.4 Single-Channel SAR ADC

In this section, design consideration of the single-channel SAR ADC for time-interleaved ADC is discussed.

3.3.1.4.1 Asynchronous Processing

Fig. 3.16 demonstrates the concept of synchronous and asynchronous processing of SAR ADC. The SAR ADC has two main phases: sampling phase and conversion phases. In synchronous processing, the clock phase are divided into N+1 equal cycle in N-bit resolution. One cycle is for sampling, while other N cycles are for the bits conversion. Each bit is processed in each cycle. In this technique, one disadvantages is that a clock signal which is N+1 times higher than the conversion rate. Such clock generator consumes huge power to operate at high frequency. Moreover, synchronous processing wastes a lot of time because the time of each cycle is determined by maximum DAC settling time. To eliminate these disadvantages, asynchronous clock control is adopted [3]. In asynchronous process, when the comparator finishes comparison, the comparator starts the next comparison through the control of SAR logic. Therefore, time of every cycle is optimized. In this design, asynchronous processing exert its advantage with 25% of the clock phase.

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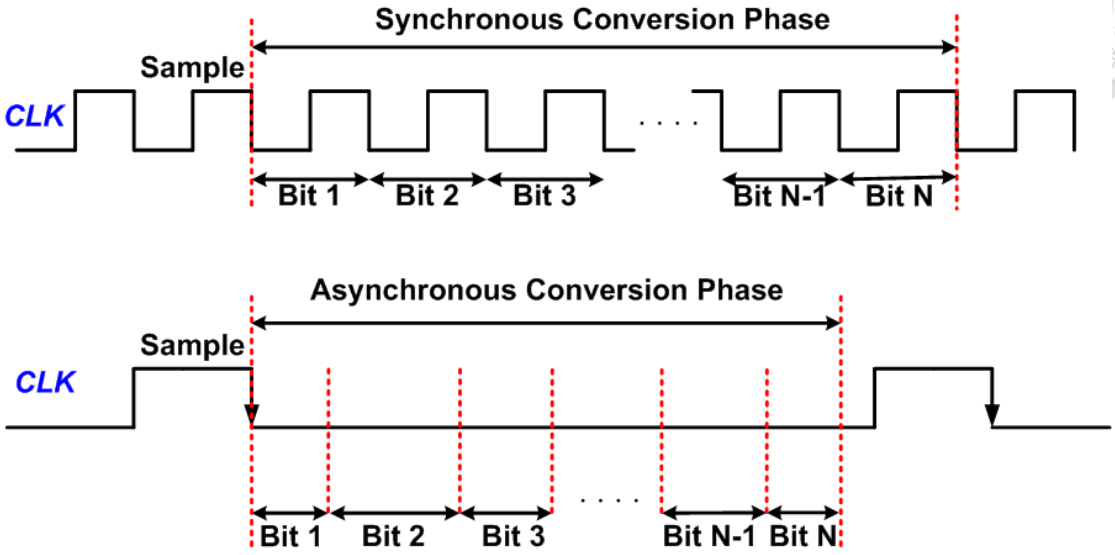

Fig. 3.16 Synchronous and asynchronous processing

3.3.1.4.2 Monotonic Capacitor Switching

For SAR ADC, switching methods of capacitive DAC is a developing filed. Several power-efficient switching methods have been proposed to reduce the power consumption such as split-capacitor switching [27], V_{COM}-based switching [28], and monotonic capacitor switching [29]. However, the power consumption in high-speed and low-to-medium resolution ADC is only roughly 15% or less in the overall power consumption of SAR ADC. Therefore, we choose the switching method based on other considerations.

Monotonic switching method is used because it has an advantage in speed when compared with other switching methods. Fig. 3.17 shows the monotonic switching method in a 3-bit ADC. The operation is as follows. All bottom plates of the capacitors are connected to V_{REF} during the sampling

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phase, and next they are switched to ground step by step during the each conversion phase. V_{inp} or V_{inn} in each phase decreases and V_{cm} gradually decreases from $\frac{1}{2}V_{ref}$ to 0. When a PMOS type dynamic comparator is adopted, its comparison time becomes faster due to the falling V_{cm}. However, this property also causes the problem of the dynamic offset. It needs to be solved and is discussed in Section 3.3.1.4.3 and Section 3.3.1.4.4.

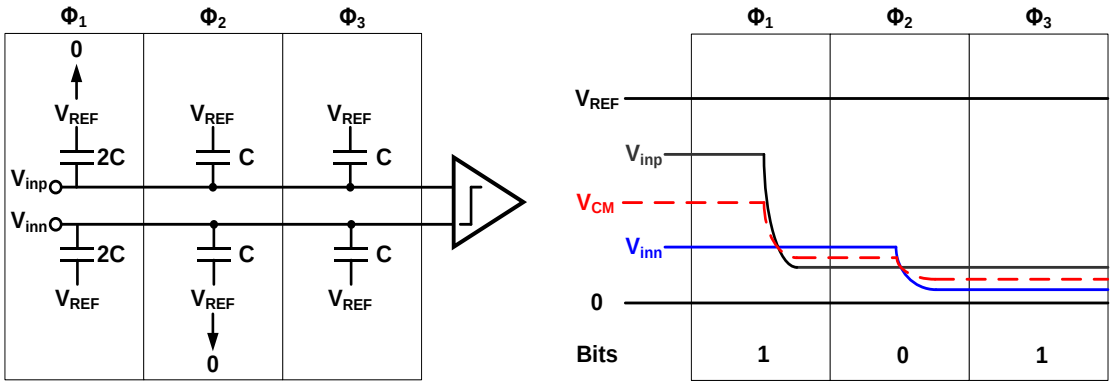

Fig. 3.17 Monotonic switching method

3.3.1.4.3 Dynamic Offset

The offset voltage of one comparator is expressed by

$$V_{OS} = \Delta V_{TH} + \frac{(V_{GS} - V_{TH})}{2}\left(\frac{\Delta S}{S} + \frac{\Delta R}{R}\right) \tag{3.21}$$

where ΔV_{TH} and V_{GS} are the threshold voltage and the gate-to-source voltage of the input differential pair; Δ_S and Δ_R are the differential pair and their load resistance mismatch.

ΔV_{TH} is a static offset which does not affect the linearity because all digital codes are shifted by

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the same offset. However, the second term is the dynamic offset for its variable value (V_{GS}-V_{TH}) when the monotonic switching method is used.

As shown in Fig. 3.17, (V_{GS}-V_{TH}) stands for the common-mode voltage and descends along with the switching procedure. The dynamic offset affect the linearity heavily. Fig. 3.17 shows a 6-bit ADC with dynamic offset. It is assumed that $V_{os}(p+1)=\frac{V_{os}(p)}{2}$, where p is the comparison cycle, starting from 1 to 5 and $V_{os}(1)$ is 5 LSB. Input range is 0.4 V. There are many missing code resulting in poor linearity as shown in Fig. 3.18.

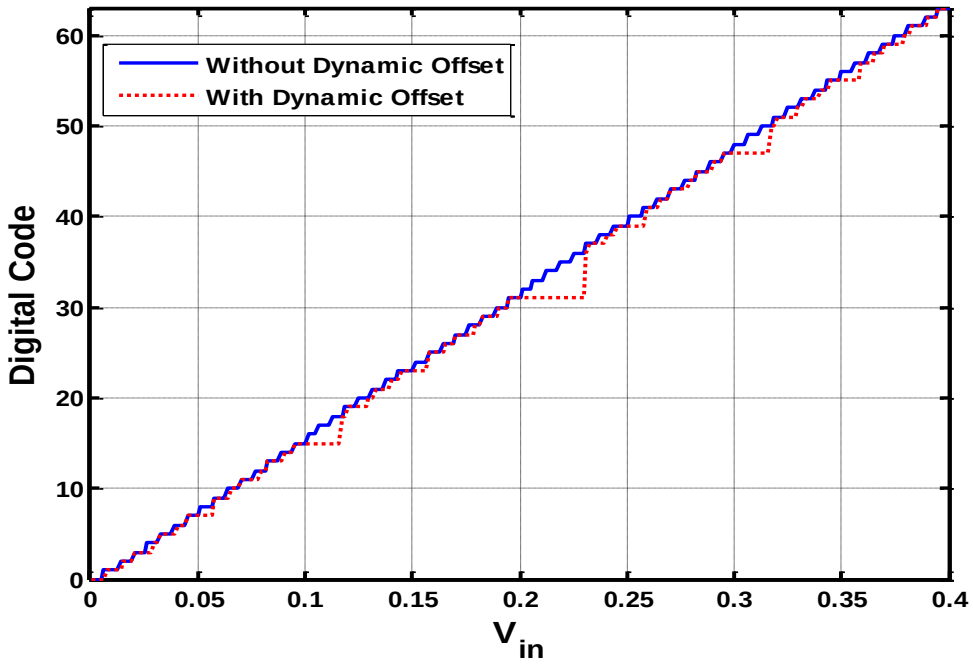

Fig. 3.18 Dynamic Offset

3.3.1.4.4 Arbitrary Weight Capacitor Array (AWCA) Technique

As described in Section 3.3.1.4.3, AWCA technique [25] is adopted to solve dynamic offset.

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AWCA is the concept of non-binary technique. We choose arbitrary radix which is less or equal to 2 between adjacent capacitors. The capacitor weight from MSB to LSB are [15 8 4 2 2 1] in this design.

The following equations which represent successive-approximation algorithm in conventional binary-weight DAC and AWCA in 6-bit resolution.

$$V_{IN} - (b_1 \frac{32}{64} V_{REF} + b_2 \frac{16}{64} V_{REF} + b_3 \frac{8}{64} V_{REF} + b_4 \frac{4}{64} V_{REF} + b_5 \frac{2}{64} V_{REF} + b_6 \frac{1}{64} V_{REF}) = V_Q \quad (3.22)$$

$$V_{IN} - (b_1 \frac{30}{64} V_{REF} + b_2 \frac{16}{64} V_{REF} + b_3 \frac{8}{64} V_{REF} + b_4 \frac{4}{64} V_{REF} + b_5 \frac{4}{64} V_{REF} + b_6 \frac{2}{64} V_{REF} + b_7 \frac{1}{64} V_{REF}) = V_Q \quad (3.23)$$

where V_Q is quantization error.

As a result, V_Q should match the following condition.

$$0 \le V_Q < V_{LSB} \quad (3.24)$$

where $V_{LSB} = \frac{1}{64} V_{REF}$.

In (3.22), if b_1 is falsely determined by the comparator due to the dynamic offset, V_Q cannot meet the condition in (3.24). Digital output code is thus incorrect. On the contrary, if b_1 is also wrongly determined in (3.23), following bits still make V_Q follow (3.24). It means that different digital codes represent the same input voltage. Since b_2~b_7 represent $\frac{35}{64} V_{REF}$ in total, the error tolerance interval of V_{IN} at MSB cycle is

$$\frac{30}{64} V_{REF} \le V_{IN} < \frac{35}{64} V_{REF} + V_Q = \frac{36}{64} V_{REF} \quad (3.25)$$

In (3.25), it is the range of V_{IN} at MSB cycle that is covered up even though b_1, or MSB, is wrongly determined. Calculating error tolerance interval at other conversion cycles is similar if a wrong decision occurs in that cycle. Table 3-2 summarizes error tolerance of corresponding bit in this

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design. If dynamic offset of the comparator is designed within ±3 LSB, the conversion result is still right. Although the last two cycle do not have redundancy, the variation of V_{cm} as well as offset is small. The problem of dynamic offset is insignificant at last conversion cycles.

Table 3-3 Error tolerance of corresponding bit

Capacitor size	15C	8C	4C	2C	2C	1C	
Weight	30	16	8	4	4	2	1
Error tolerance	±3	±2	±2	±2	0	0	

3.3.1.4.5 Thermal Noise of AWCA

In this design, total capacitance of 3fF or unit capacitance of 0.05fF is adequate for a 6-bit design if RMS noise voltage is less or equal to one-tenth of V_{LSB} ($\sqrt{\frac{kT}{C}} < \frac{1}{10}V_{LSB}$). However, such a small unit capacitance is hard to use in practice and cannot meet accuracy requirement of DAC due to process limitation. Therefore, unit capacitance of 1.25 fF is chosen to achieve AWCA. RMS noise voltage is really small to be neglected.

3.4 Summary

This thesis presents a 16-channel time-interleaved SAR ADC. First, by combining the front-end input buffers and the grouping technique, the proposed ADC achieves the performance of high input bandwidth. Second, design consideration of the input bandwidth and the settling time are discussed. Next, mismatch including gain mismatch, offset mismatch, and timing skew among sun-ADCs are

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considered. Finally, the SAR ADC is used as a sub-ADC for its great power efficiencies. Asynchronous processing, monotonic capacitor switching, and AWCA technique aim at making sub-ADC become faster and robust.

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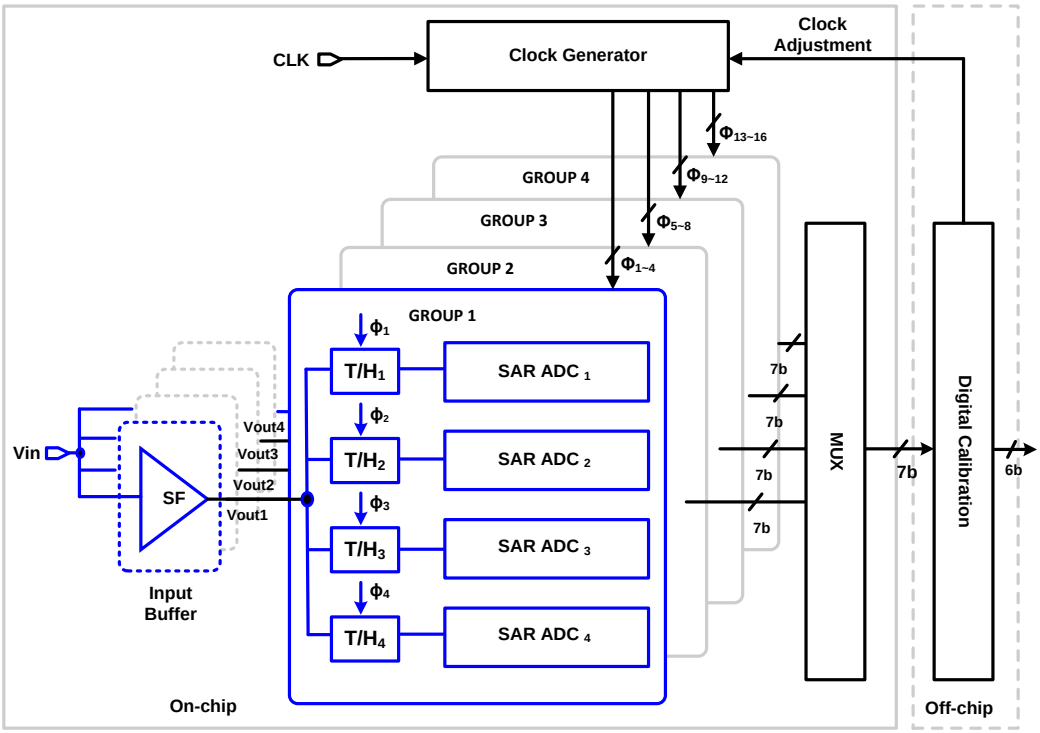
Chapter 4

Circuit Implementation and Simulation Results

4.1 Introduction

In this chapter, circuit implementation and simulation results will be described in detail. Fig. 4.1 presents the building blocks of the proposed time-interleaved SAR ADC. The architecture is composed of 16-channel SAR ADCs, 4 groups of front-end buffers, a clock generator and a multiplexer (MUX) circuit.

First, the circuit blocks and their simulation are described, including front-end circuit, bias circuit, single-channel SAR ADC, clock generator, divider and multiplexer. Second, the overall ADC simulation result is shown. Finally, performance metrics of the proposed ADC are listed in table 4-1.



4.1 Building blocks of the proposed time-interleaved SAR ADC

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4.2 Building Blocks and Circuit Implementation

4.2.1 Front-End Circuit

As descried in Section 3.3.1, the front-end circuit is regard as source followers (SF), T/H switches, and AWCA of the SAR ADC. Fig. 4.2 shows this front-end circuit. The source follower is biased by cascode PMOS current source in order to suppress the effect of channel-modulation. Consequently, the linearity of the SF is less affected by the variation of the output voltage. The transmission gate is used as a T/H switch for its high speed operation. Although its linearity is worse than the bootstrapped switch, the linearity is sufficient in this design.

In Fig.4.2 (b), the high-swing current mirror with two input branch, V_{b1} and V_{b2}, is adopted as the biasing circuit of the source follower and I_{REF} is determined outside the chip and can be tuned by manual. The ratio of I_{BIAS} and I_{REF} is 5.

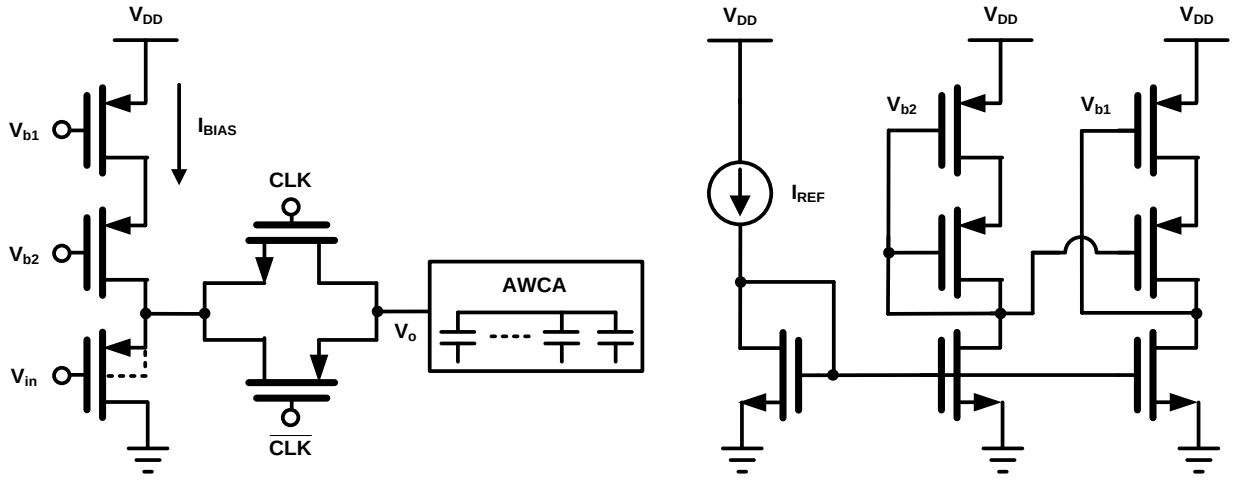

Fig. 4.2 (a) Front-end circuit (b) biasing circuit of the source follower

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As discussed in Section 3.4.1, the settling time and the required input bandwidth are calculated to meet the specification of ADC. Fig. 4.3 shows the 3-dB frequency of the front-end circuit versus $I_{BIAS.}$ It simulates the order of I_{BIAS} which is properly chosen.The Nyquist frequency is 4 GHz in this design. The suitable range of 3-dB frequency is from 8 GHz to 10 GHz to ensure the input bandwidth two times higher than the Nyquist frequency. The enough input bandwidth avoids the problem of bandwidth mismatch [11].

However, the large-signal behavior of the front-end circuit fits the operation of the ADC in reality. More precisely, the dynamic linearity of the front-end circuit should be ensured to achieve the precision of this SAR ADC. Therefore, through FFT simulation, Fig. 4.4 presents the simulated SFDR versus I_{BIAS} when input $V_{pp,diff}$ is 800 mv and I_{BIAS} is chosen to be around 0.2 mA. The input frequency is 4 GHz. Moreover, as shown in Fig. 4.5 and Fig 4.6, the input amplitude and common mode have to be analyzed to find the most proper performance. A common mode voltage around 200 mV and input around 800 m $V_{pp,diff}$ are used to satisfy the requirement of this work.

As mentioned in Section 2.4.1, offset mismatch is an important issue in time-interleaved architecture and SF contributes to offset mismatch. A number of 5000 Monte Carlo simulations is used to calculate offset voltage. The result shows that the standard deviation of offset is around 2 mv (0.08 LSB).

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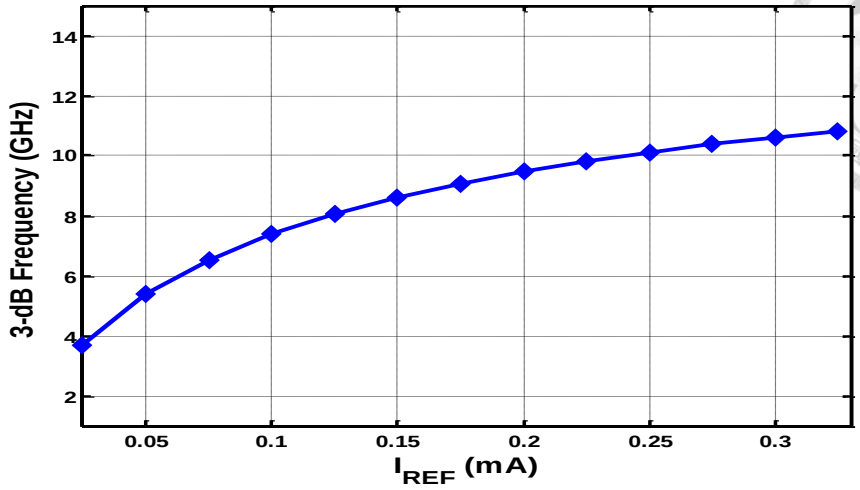

Fig. 4.3 Simulated 3-dB frequency versus I_{REF}

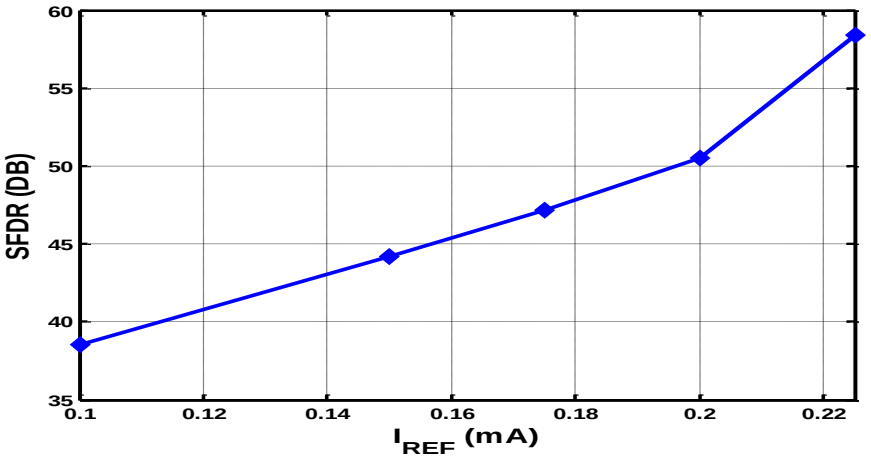

Fig. 4.4 Simulated SFDR versus I_{BIAS} with 3.78 GHz input frequency

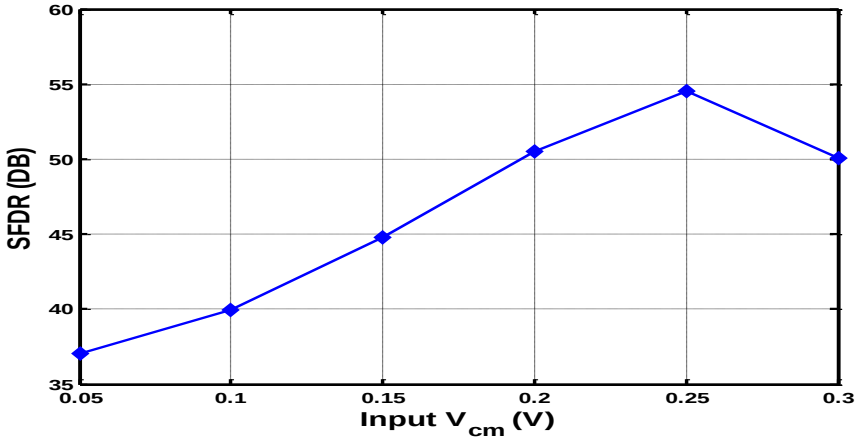

Fig. 4.5 Simulated SFDR versus input common mode voltage with 3.78 GHz input frequency

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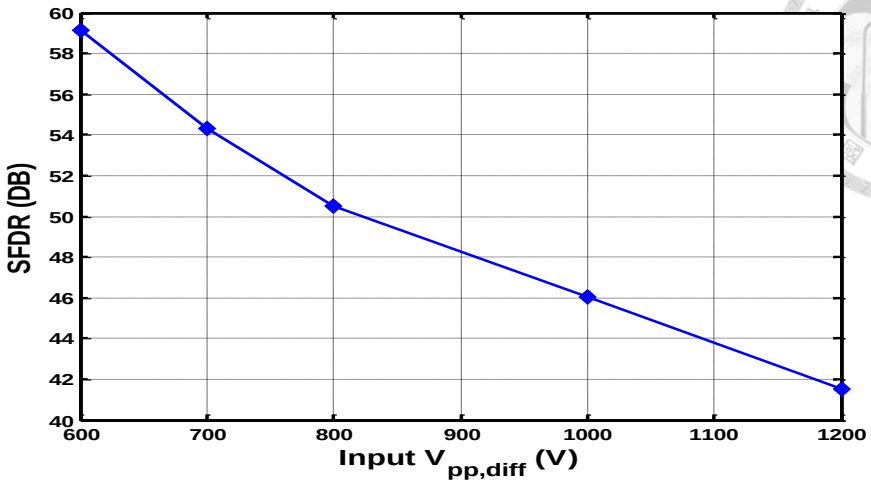

Fig. 4.6 Simulated SFDR versus input amplitude with 3.78 GHz input frequency

4.2.2 Bias Circuit

In this design, because 8 groups of source followers (SF) circuit including differential circuits are implemented, the current mismatch among SFs should be reduced in case they exceed the offset and gain mismatch calibrated range. In layout, the distance among each group of source follower is inevitably long in order to maintain the input signal systematic matching. This layout style would cause considerable current mismatch if current mirror are built through the voltage routing of bias signals.

To overcome this problem, we use a combination of voltage and current routing technique. For example, Fig.4.7 shows the two group of SFs with their current sources. M_1-M_3, M_{11}-M_{12} and other current mirrors are close together to reduce the effect of interconnect resistance and mismatch of threshold voltage. The current I_{REF1}-I_{REF4} are routed to the vicinity of the building blocks for their long length. On the other hand, the cascade current source with two input branches such as M_4-M_{10}

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and M_{13}-M_{19} uses voltage routing locally. Accordingly, current sources of source followers do not have large parasitic capacitance and maintain agreeable high-frequency process.

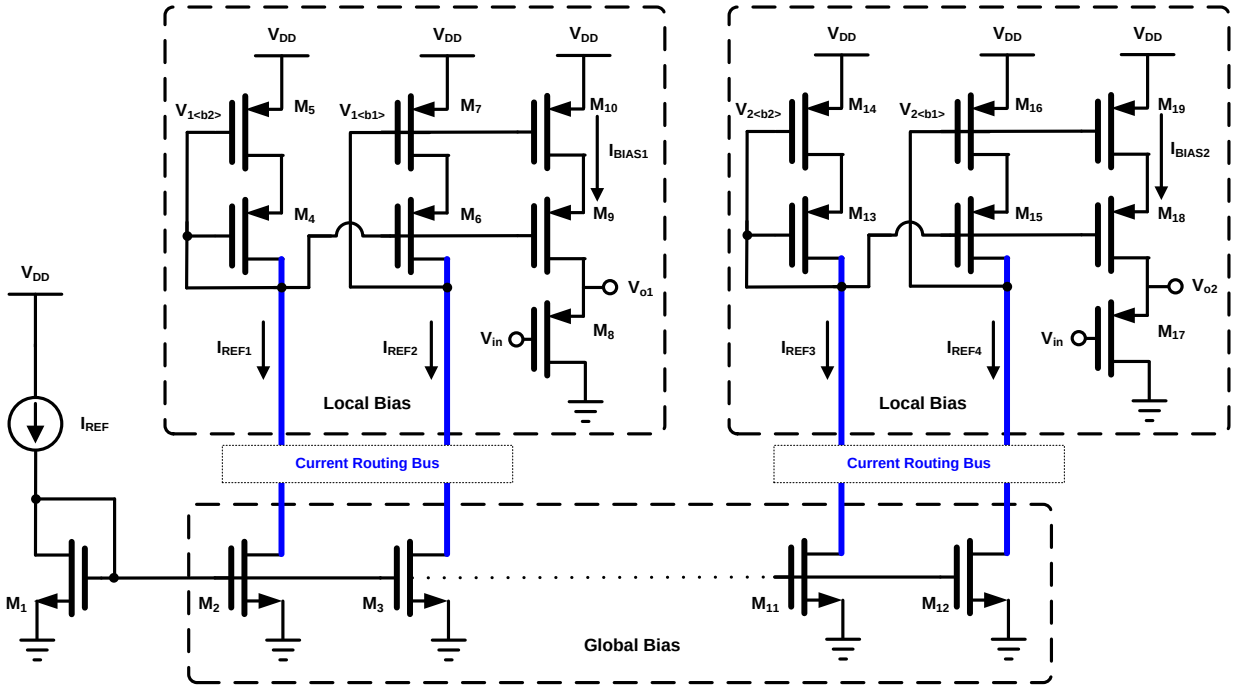

Fig. 4.7 Bias circuit with current routing and voltage routing

4.2.3 Single-Channel SAR ADC

In Section 4.2.3, the circuit block and simulation of the single-channel SAR ADC are described, including sampling switch, Arbitrary weight capacitor array (AWCA), comparator, SAR logic.

4.2.3.1 Sampling Switch

Transmission gates are chosen as sampling switches for their advantage of high-speed. The detailed simulation is described in Section 4.2.1. Dummy switches and cross-coupled path are used

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to cancel the effect of the signal feedthrough as shown in Fig.4.8 [29]. The effect of channel charge injection and clock feedthrough do not excessively degrade linearity for the target 6-bit design. Fig. 4.9 shows the turn-on resistance (R_{on}) of the sampling switch versus V_{IN} (V_{op}, V_{on}). The range of V_{IN} used keeps from 0.4 V to 0.6 V due to linearity of SF. R_{on} maintains around 100 Ω to have enough input bandwidth. Therefore, the sampling switch maintain acceptable linearity at high input frequency.

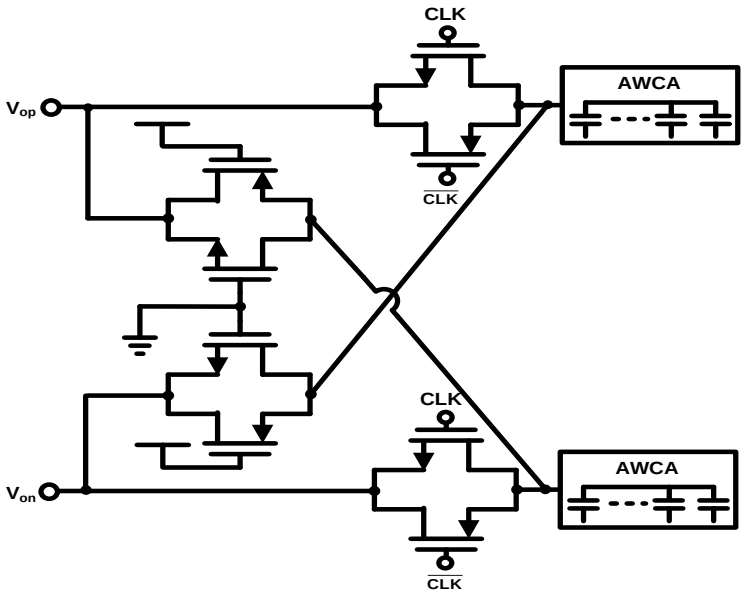

Fig. 4.8 Sampling switch

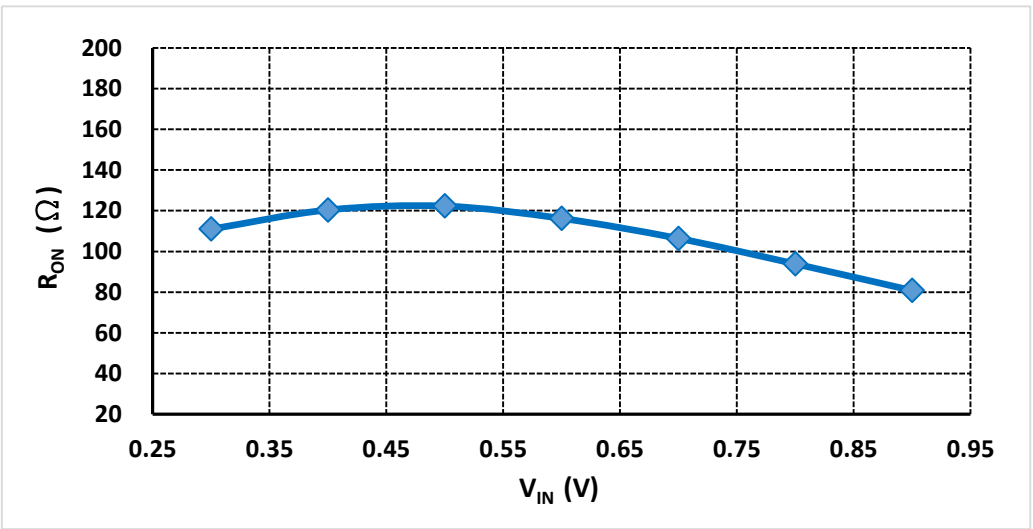

Fig. 4.9 Turn-on resistance (R_{on}) of the sampling switch versus V_{IN} (V_{op}, V_{on})

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4.2.3.2 Arbitrary Weight Capacitor Array (AWCA)

As mentioned from Section 3.3.1.4.4 to Section 3.3.1.4.5, AWCA technique is adopted to deal with the problem of dynamic offset. Fig. 4.10 shows AWCA in this design. The conventional capacitor array with monotonic switching method is [16 8 4 2 1 1]. For AWCA technique, $1C_u$ from MSB capacitor is taken and added into LSB capacitor, where C_u is unit capacitor. Moreover, additional 1 C_u is added as a new LSB capacitor while original LSB capacitor become $2C_u$. The capacitive DAC becomes [15 8 4 2 2 1], and the last C_u in the conventional capacitor array is unnecessary because its function is just likes parasitic capacitance. The max error tolerance of AWCA is about 3 V_{LSB} (~37.5 mV)

The switching operation of AWCA is described in Section 3.3.1.4.2. In particular, the NAND gates and signal RESET are used to reset all the bottom plates of the capacitors. If RESET coincides with next sampling conversion, the sampling signal is disturbed by the bottom-plate switching disturbance. Alternatively, signal RESET is triggered immediately when the last bit conversion is complete in this design. This manner improves that disturbance and increases the sampling speed.

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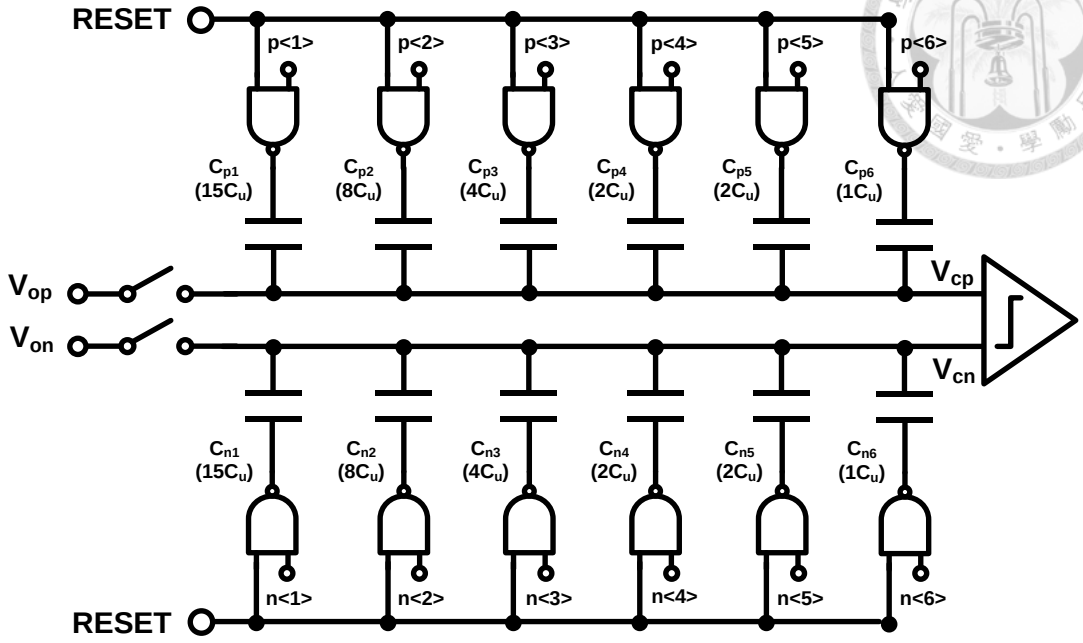

Fig. 4.10 Arbitrary weight capacitor array

Fig. 4.11 depicts behavior simulation of ENOB versus dynamic offset when ADC uses binary-weighted capacitor array and AWCA. To maintain ENOB higher than 5.5-bit, dynamic offset V_{OS} must be confined to within 25 mV (2 V_{LSB}) in the architecture of binary capacitor arrays. In contrast, AWCA technique broadens the tolerable V_{OS} range which becomes around 65 mV (5 V_{LSB}).

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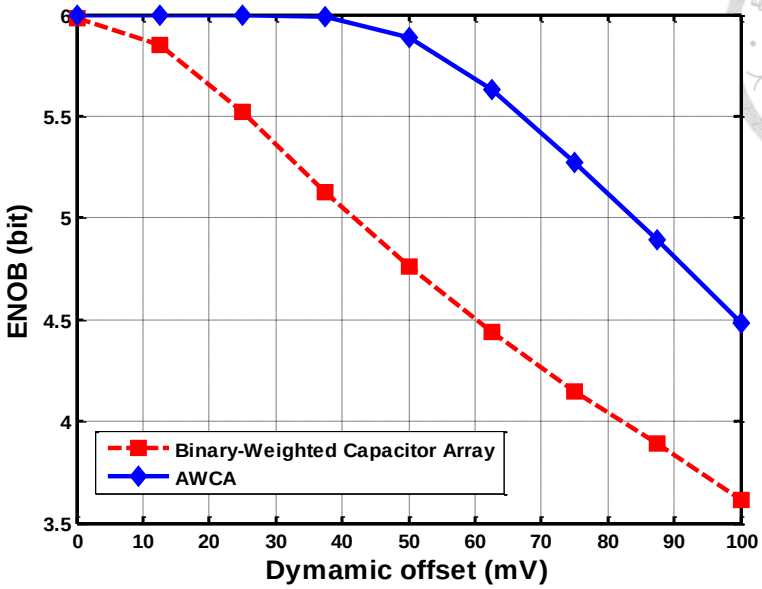

Fig. 4.11 ENOB versus offset using binary-weighted capacitor array and AWCA

4.2.3.3 Comparator

For ADC, the comparator is classified into two types: It has a static preamplifier or not. In general, the comparator with static preamplifier is often applied in high resolution due to effect of noise. On the other hand, the dynamic comparator is usually used in high-speed low resolution ADC for its high speed and low power. The design consideration of the comparator are speed, offset, and noise in high-speed SAR ADC.

Fig. 4.12 shows the schematic of the comparator in this work. It uses PMOS as input differential. Only NMOS type latch is adopted to decrease the number of transistors in low supply voltage. The operation is described as follows. When LA signal is high, the comparator is in the reset mode, and SN and SP are also reset to ground. When the comparator enters into comparison, LA signal goes to

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low and SN and SP are in positive feedback loop to pull themselves to high and ground.

The key parameter in latch-type comparator designs is the regeneration time-constant [30]

$$\tau = \frac{C_L}{g_m} \tag{4.1}$$

where C_L is the total capacitance at the latch output and g_m is the transconductance of the latch transistors. By enlarging $\frac{W}{L}$ ration of input transistors, τ becomes smaller and the comparator can increase speed to meet the requirement. As single-channel ADC operate at 500 MS/s and duty cycle of clock is 25%, the total time that the operation of comparator do seven times of comparison and reset is 1500 ps. Average comparison time is around 100 ps.

As mentioned in Section 2.4.1, offset mismatch is an important issue in time-interleaved architecture and comparators contribute to offset mismatch. A number of 5000 Monte Carlo simulations is used to calculate offset voltage. The result shows that the standard deviation of offset is around 0.7 V_{LSB} (about 9 mv).

Finally, the kickback noise is ignored because the input signal ruined by regeneration mode is returned to original one due to the following reset mode. On the other hand, through a number of 5000 Monte Carlo noise analysis, the standard deviation of transient noise is less than $\frac{1}{100}V_{LSB}$ (about 0.1 mv).

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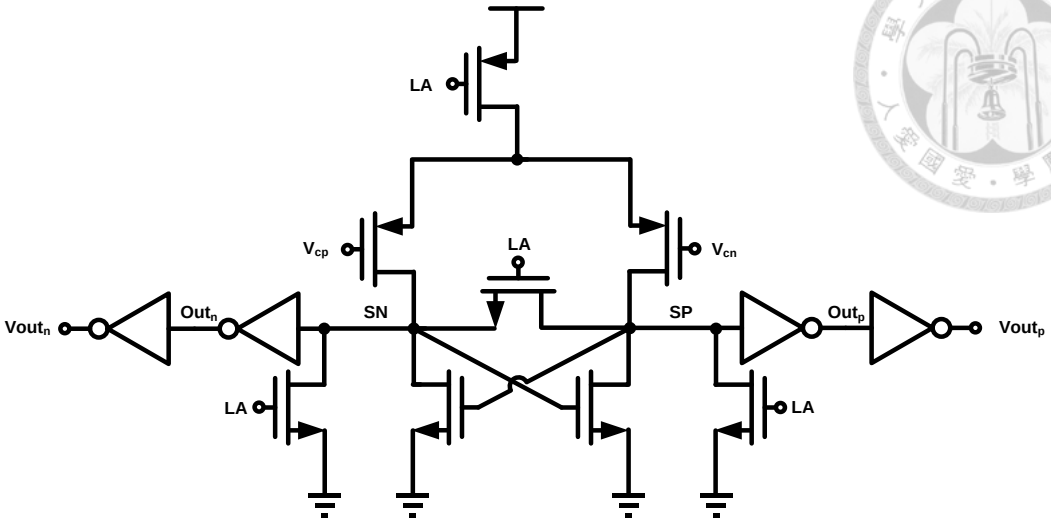

Fig. 4.12 Schematic of the dynamic comparator

4.2.3.4 SAR Logic

The asynchronous processing is adopted to increase conversion rate as mentioned in Section 3.3.1.4.1. Fig. 4.13 (a) shows the schematic of the asynchronous control loop and shift registers. The operation is explained as shown in Fig. 4.13 (b). When sampling phases is converted to conversion, signal Start rises to high and triggers this control loop. First, signal LA becomes low to initiate the comparator. Then, one of the comparator output $Outp_i$ or $Outn_i$ would fall to low due to the comparison of the comparator, and signal Done rises to high from low. Next, LA goes high to reset the comparator. As the comparator has been reset, Done begins to go from high to low. Finally, LA becomes low again, initiating the following comparison. This process repeats until signal Stop is triggered from low to high. The period of signal LA can be calculated as

$$T_{cycle} = T_{cmp} + T_{reset} + 2 \times T_{gate} \tag{4.2}$$

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where T_{cmp} is the comparison time of the comparator, T_{reset} is the reset time of the comparator, and T_{gate} is the gate delay of logic circuit in this loop. The gate delay includes two inverters, one XNOR gate, one NOR gate, and one NAND gate.

At the same time, the shift register generates SR<1> to SR<7> to control AWCA switching and counts the number of comparisons. When ADC enters the next sampling, Start reset all shift registers to initial state.

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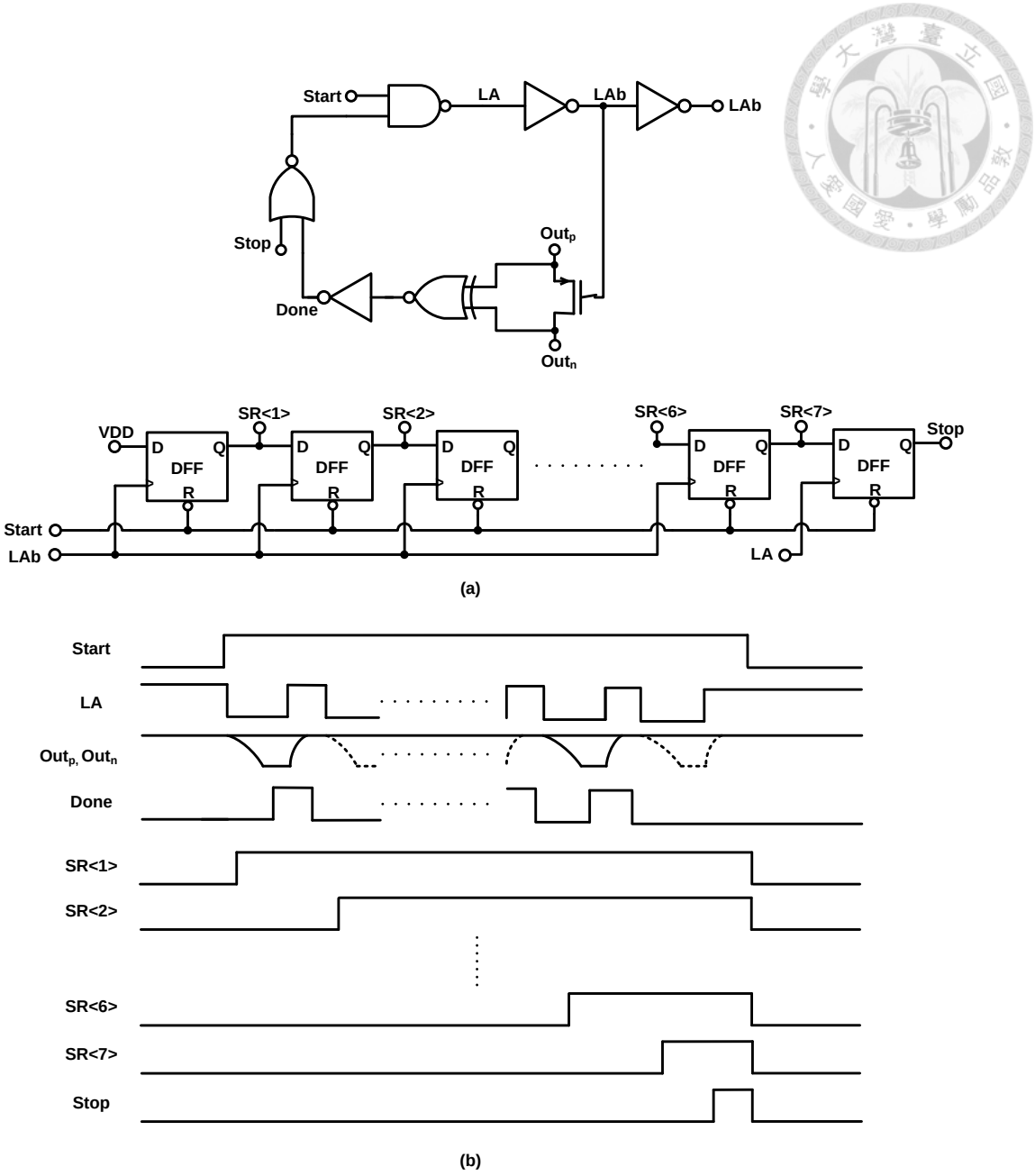

Fig. 4.13 (a) Block diagrams and (b) waveforms of asynchronous SAR logic

The conventional DFF control logic is used to connect comparator and the capacitive DAC, as depicted in Fig. 4.14 (a). However, it needs much transistors due to differential structure.

On the contrary, in Fig. 4.14 (b), the differential control logic (DCL) replaces DFFs when the

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input signal is digital code. Initially, LA is low, resetting Q and Qb to ground while D and Db are low. Then, SR<1:7> are fed into LA of the corresponding DCL to trigger it. When D or Db becomes high, the regeneration latch reacts quickly to pull Q or Qb to high. Once Q and Qb are determined, there are two positive feedback loops to lock the DCL. Hence, the DCL output remains same no matter how D and Db vary due to the comparison of the comparator.

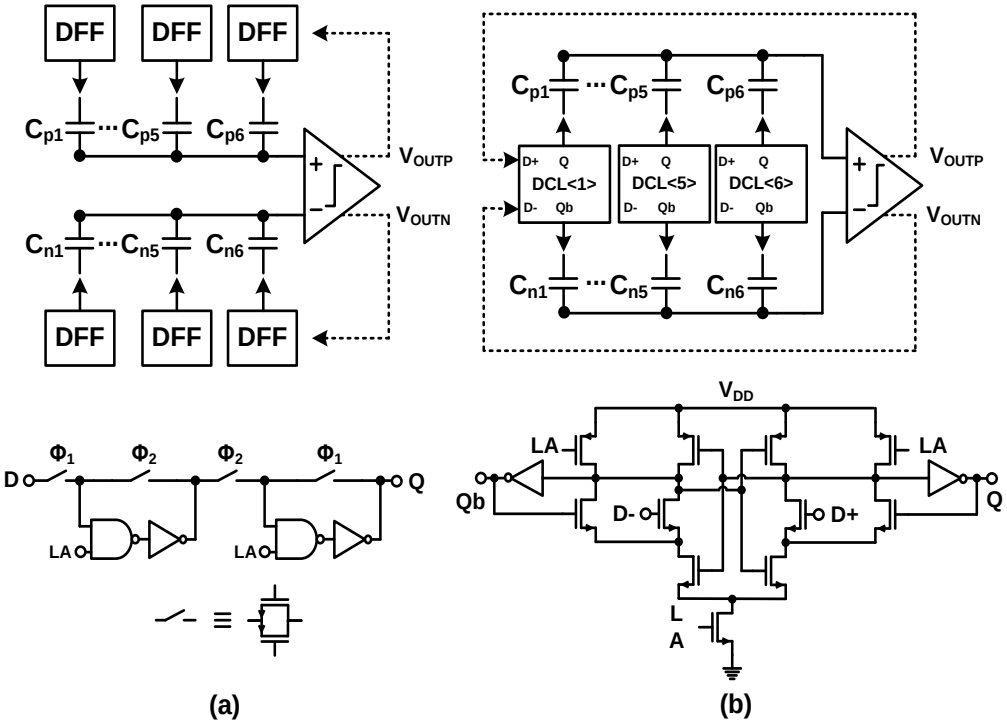

Fig. 4.14 (a) Conventional DFF control logic (b) DCL

4.2.3 Clock Generator

The clock generator creates clocks which determine the sampling and conversion phases of a SAR ADC. A duty-cycle 25% clock is used and longer conversion time provides high conversion rate

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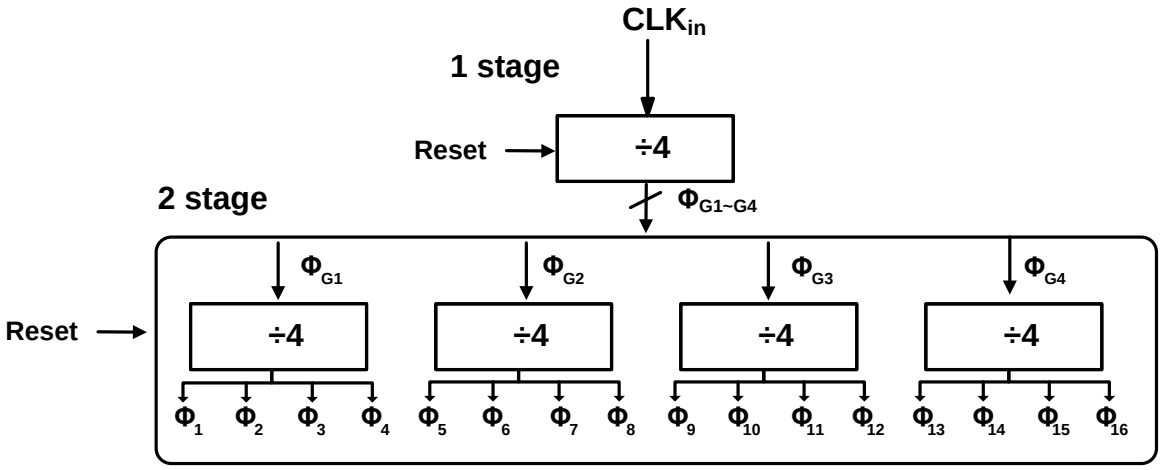
for asynchronous SAR SDC.

Fig. 4.15 shows the clock generator and corresponding waveform. The external signal CLK_{in} is fed into the ÷4 divider of the first stage to generate clock phases Φ_{G1}~Φ_{G4} and each phase generates 4 clock phases through the ÷4 divider of the second stage. Finally, totally 16 different clock phases Φ_1~Φ_{16} would be generated and are distributed to each sub-ADC. For example, during the reset mode, Φ_{G1} is preloaded with high, while the other phases Φ_{G2}~Φ_{G4} are low. In this way, during the normal operation mode, 25% duty clock phases Φ_{G1}~Φ_{G4} are generated. Likewise, non-overlapping clock phases Φ_1~Φ_{16} are generated to achieve proposed front-end sampling architecture and only one external clock signal CLK_{in} is needed.



(a)

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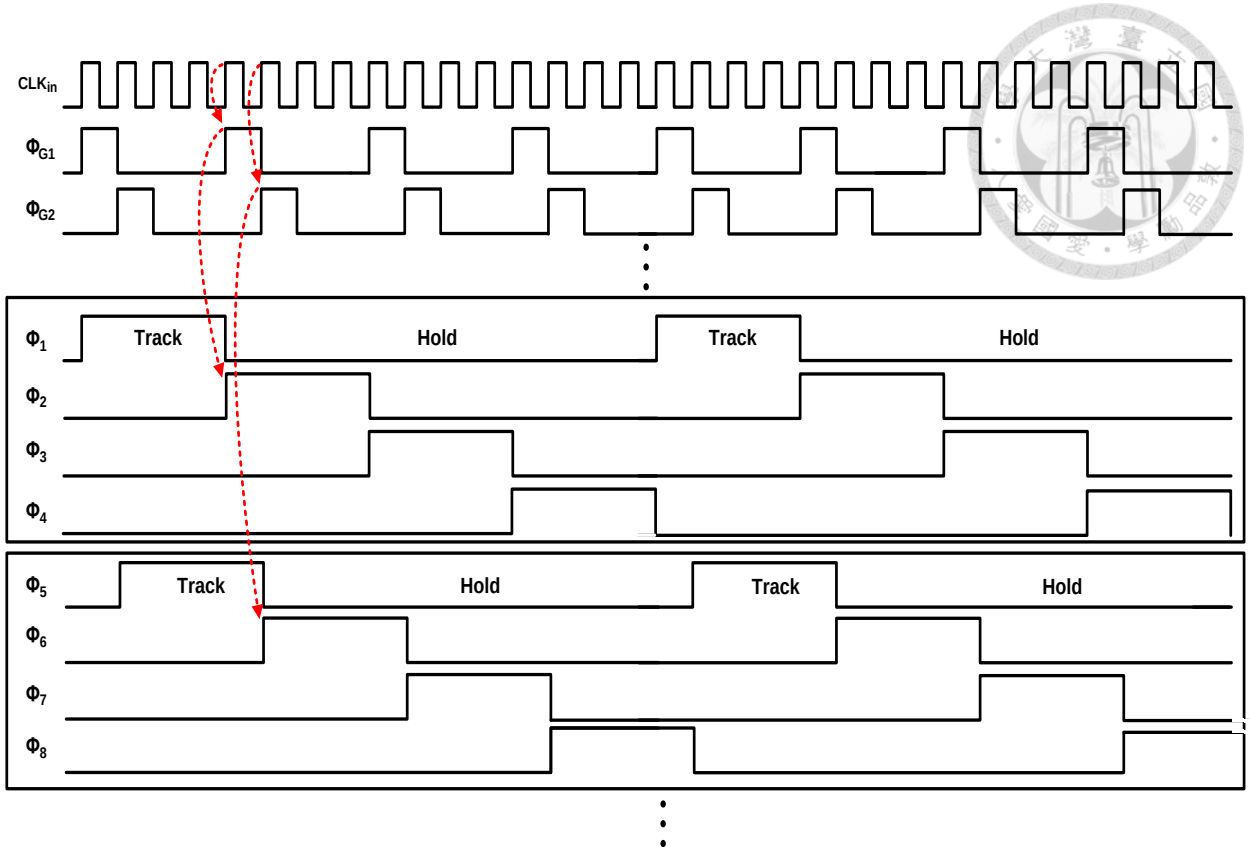

(b)

Fig. 4.15 (a) Block diagrams and (b) waveforms of clock generator

As shown in Fig. 4.16, a ÷4 divider consists of a ring of 4 flip-flops, one of which is preset to high, while the others are preset to low. The flip-flop adopts true single-phase clocking (TSPC) architecture for its high speed and low power dissipation. Fig. 4.17 shows a schematic of TSPC flip-flop. One type of schematic is preset to high, while the other is preset to low. Dummy transistors M_4~M_5, M_9~M_{10}, M_{15}~M_{16} are added to make two types of TSPC symmetrical. Consequently, parasitic capacitance of two type of TSPCs are nearly equal and timing skew is reduced. Moreover, TSPC have a floating net on the drain of transistor M_2 and this net has leakage current if M_2 and M_3

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cannot entirely cut off. Hence, M_2 and M_2 are types of high voltage threshold (hvt) PMOS transistors to decrease the leakage current.

The circuit operates as follows. When CLK is low, the first stage operates as an inverter, an opposite signal of D is at A and the signal at B is high. When CLK goes high, the first stage turn off and the second and third stage become active. The signal is opposite of A at B. The signal Qb is opposite of B. Accordingly, Qb is equal to A and Q is equivalent to D.

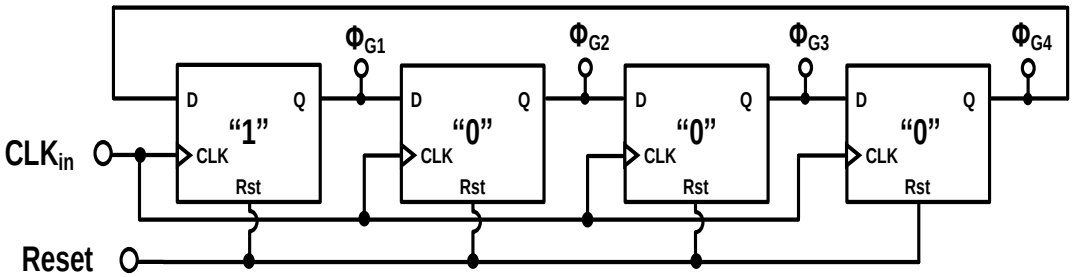
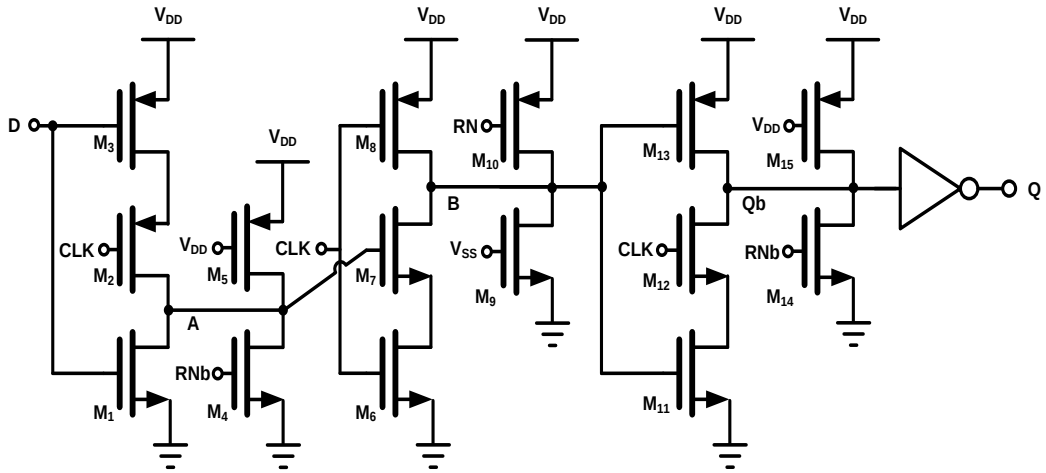


Fig. 4.16 Diagram of ÷4 divider



(a)

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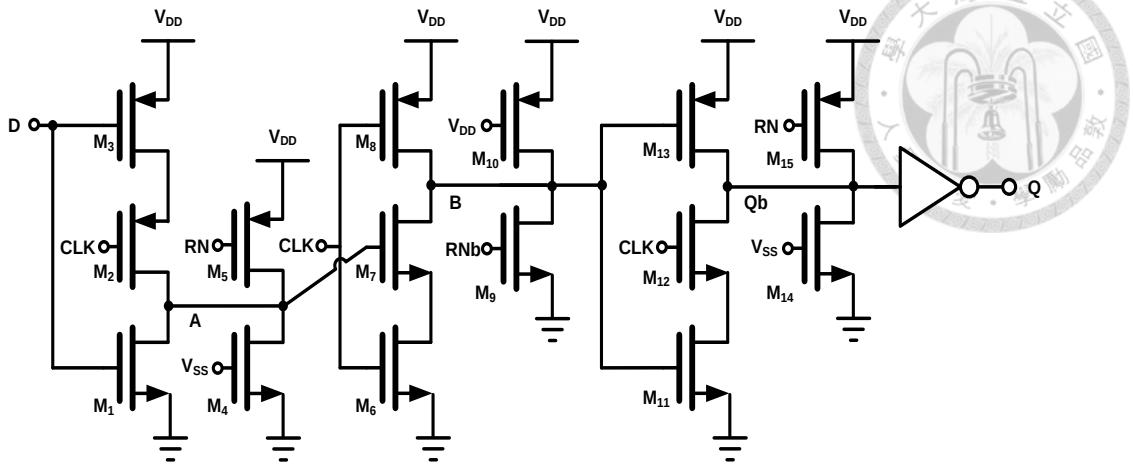

(b)

Fig. 4.17 Schematic of TSPC flip-flop preloaded (a) with high (b) with low

4.2.4 Delay Line

Since different clock phases would cause timing skew, delay line is used to adjust clock phases and correct timing skew. A tolerate timing skew can be estimated as in (4.3) and we know how to design delay line [12]

$$\sigma_t^2 \le \left(\frac{N}{N-1}\right)\cdot\left(\frac{2}{3\cdot 2^{2m}}\right)\cdot\left(\frac{1}{(2\pi f_{in})^2}\right) \tag{4.3}$$

where σ_t is the standard deviation of the timing skew among sub-ADCs; N is the number of sub-ADCs; m is the resolution of ADC; and f_{in} is the sinusoidal input frequency. In this design, N = 16, m = 6, f_{in} = 4 GHz are substituted into (4.3) and σ_t should be less than 0.6 ps.

Delay line is shown in Fig. 4.18. It consists inverters and delay cells. Delay cells have coarse and fine delay control to provide different step size. Delay cells are MOS-capacitors and we change their capacitive load by control CTRL<1:7>. Then, different capacitive load makes clock phases have

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different delay. The total correction range is based on the C-CC post-layout simulation which shows that the standard deviation of the timing skew is around 1.6ps. Thus, the total range of delay line is 1.8 ps. The coarse delay and fine delay are designed to have 0.6 ps and 0.12 ps with a step size. The residual timing skew after correction is less than 0.6 ps.

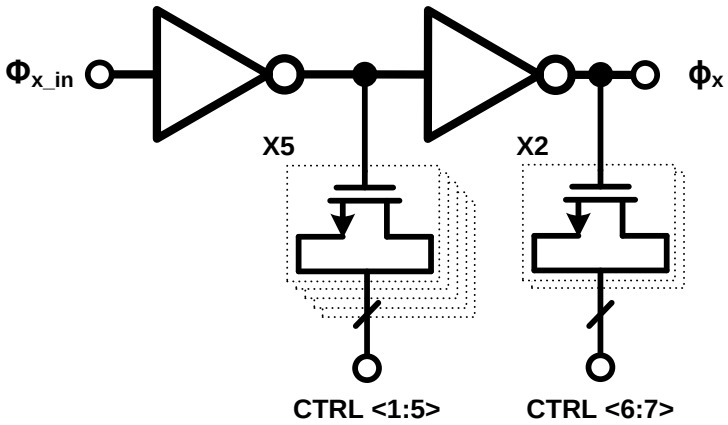

Fig. 4.18 Schematic of delay line

4.2.5 Clock Divider and Multiplexer

The sampling frequency is extremely high in this design. A mix signal oscilloscope MSO 4034 in test setup cannot operate as high as 5 GHz sampling rate. The frequency of outputs' clock needs to be decimated.

In this design, the output data is decimated by 125, which is relatively prime to the number of channels, 16. Fig. 4.19 shows the circuit of the clock divider, three ÷5 dividers are in series connection to generate divisor of 125. Then, this clock signal is fed to D flip-flop to trigger digital output in each

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single-channel ADC. Next, digital output are combined by Multiplexer (MUX) to compose one group of output data of time-interleaved ADC. The diagram of MUX is presented in Fig. 4.20. It is a 16-to-1 MUX which consists of simple transmission gates and inverters. The selection signals of MUX, Div_1~Div_2 are produced a ring of 16 flip-flops. The sequence of the selection signal in MUX is related to the number of decimation, 125. In this work, the sequence is {$channel_1$, $channel_{14}$, $channel_{11}$, $channel_8$, $channel_5$, $channel_2$, $channel_{15}$, $channel_{12}$, $channel_9$, $channel_6$, $channel_3$, $channel_{16}$, $channel_{13}$, $channel_{10}$, $channel_7$, $channel_4$}. Fig. 4.21 shows the timing diagram of the clock divider. For example, if the 5 GHz output data OUTPUT through this clock divider, the output signal is Final Data with 40 MHz. As a result, MSO 4034 successfully retrieves 40 MHz digital output.

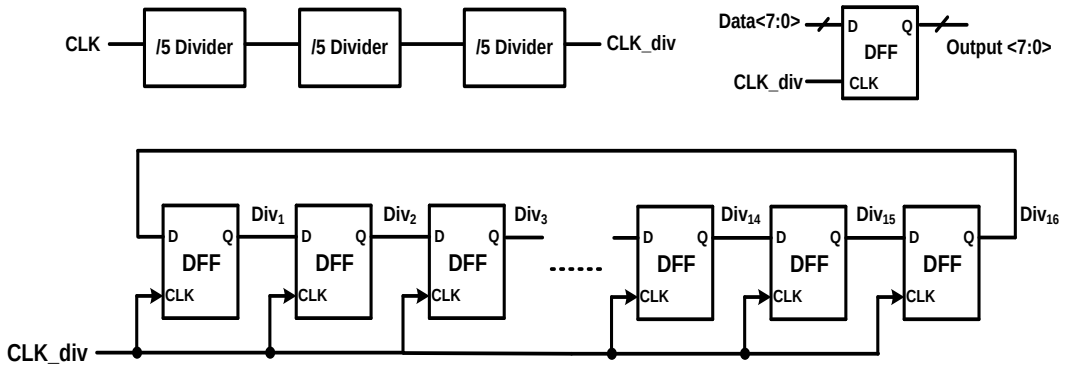

Fig. 4.19 Circuit of the clock divider

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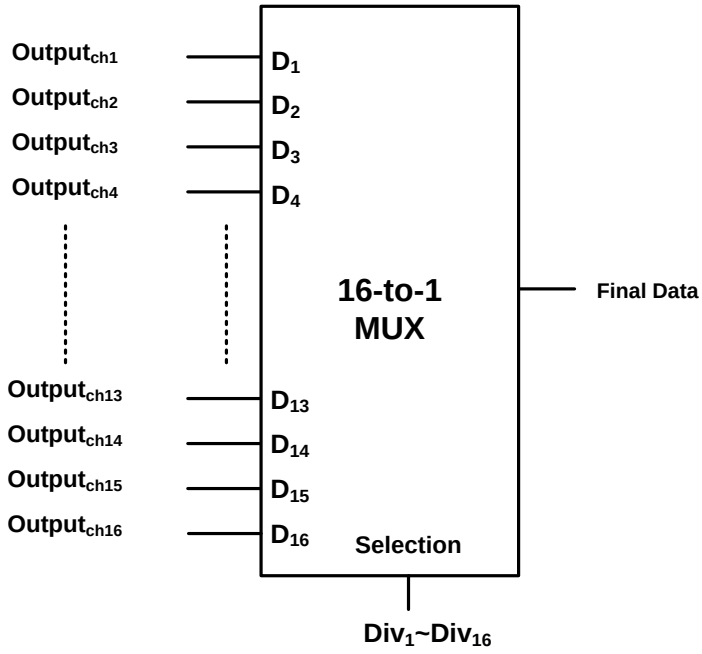

Fig. 4.20 Diagram of Multiplexer

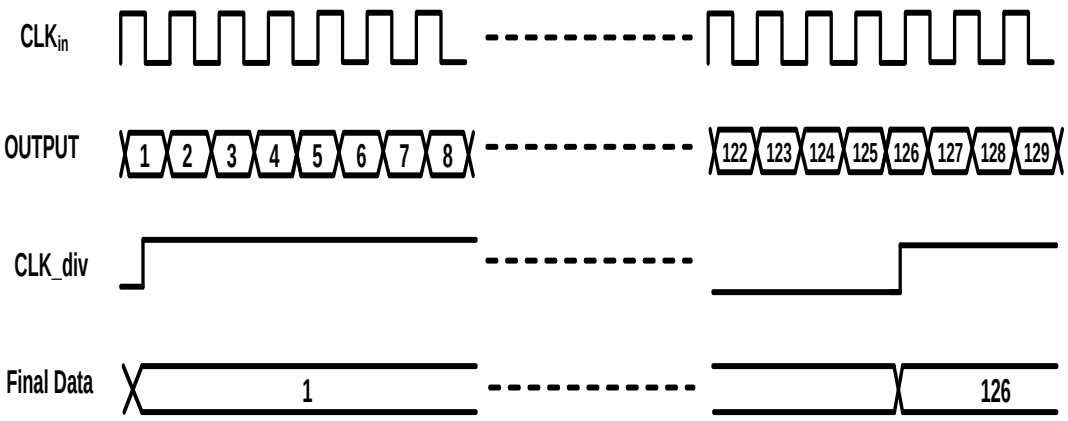

Fig. 4.21 Timing diagram of clock divider

4.3 Overall ADC Simulation Results

The transistor level with C-CC post-layout simulation is done by HSPICE. The dynamic performance of this ADC is characterized by FFT analysis. Fig. 4.22 shows 256-point digital output

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spectrum with sampling rate of 8GS/s and input frequency of 93.75 MHz. The SFDR and SNDR are 48.39 dB and 37.48 dB respectively. For Nyquist input frequency of 3.78 GHz, 256-point digital output spectrums are shown in Fig. 4.23 and Fig. 4.24. Fig. 4.23 shows digital output spectrums without timing skew calibration, and the SFDR and SNDR are 48.39 dB and 37.48 dB. The performance degrades because the power of noise spurs caused by timing skew increases. The worst spur is around 35 dB. After timing skew calibration, the SFDR and SNDR are 47.15 dB and 36.13 dB, as shown in Fig. 4.24. The noise spurs of timing skew are below 45 dB.

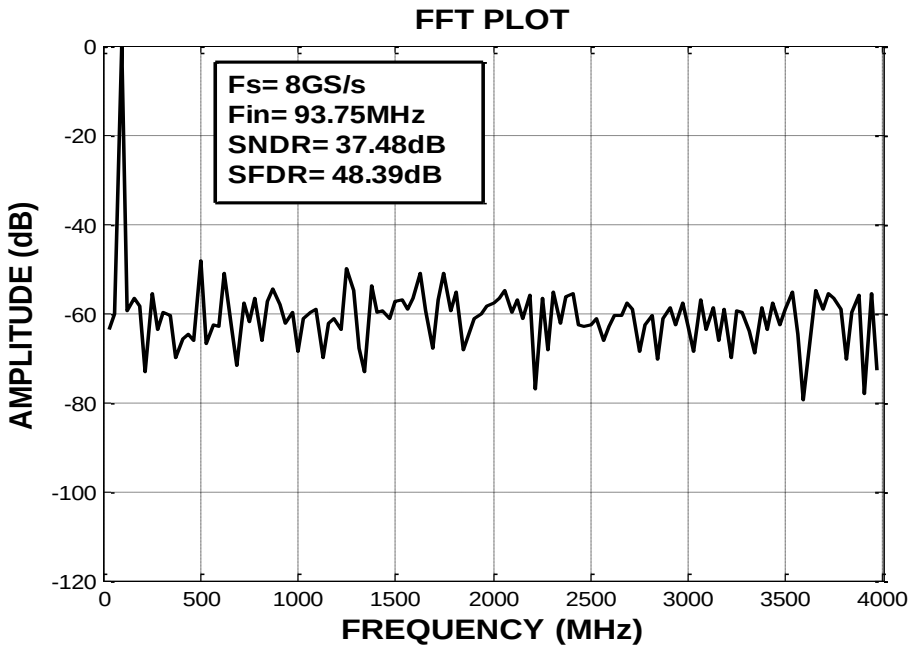

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Fig. 4.22 FFT spectrum with low input frequency

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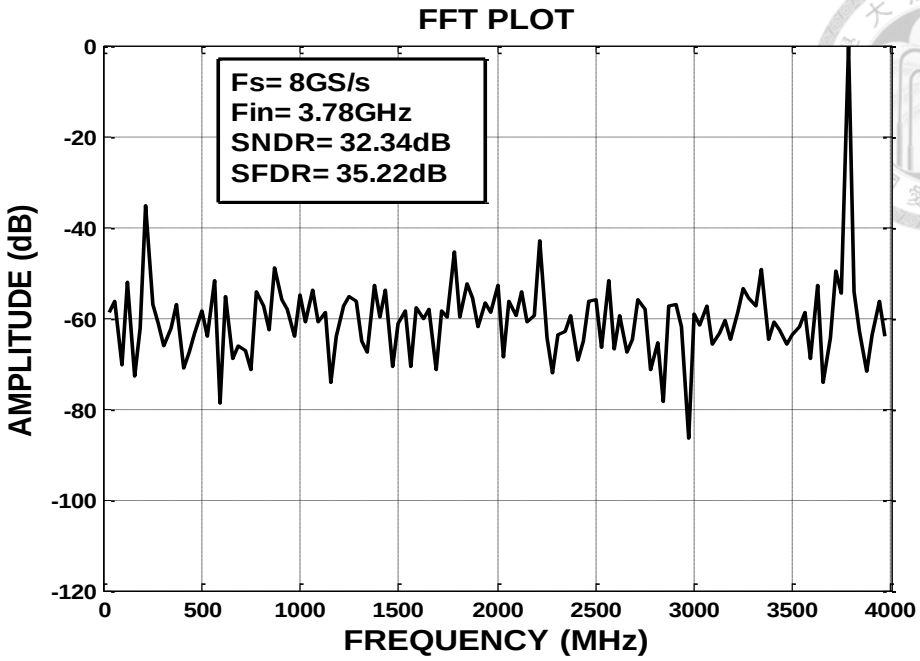

Fig. 4.23 FFT spectrum with Nyquist rate input frequency before timing skew calibration

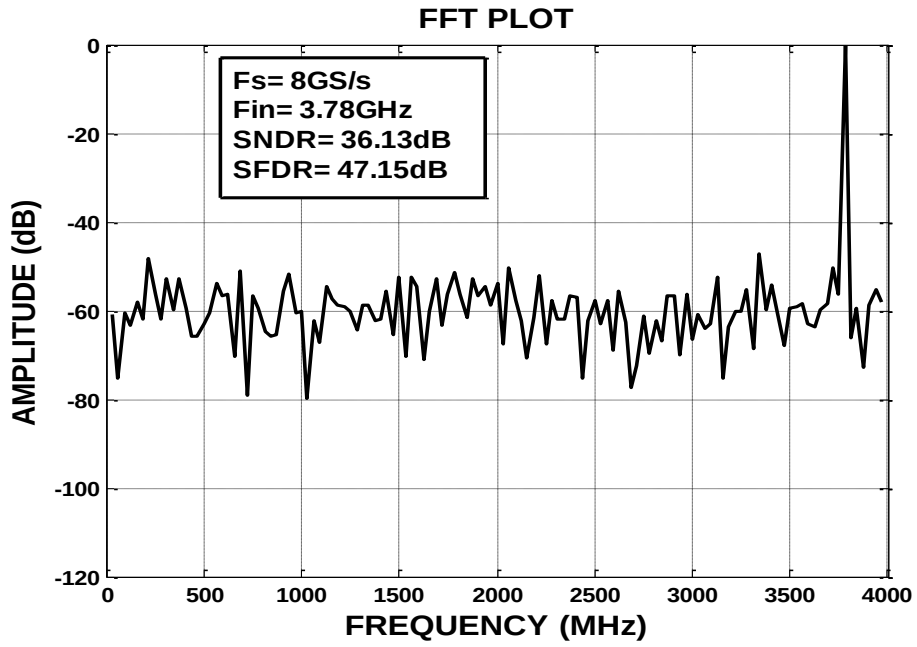

Fig. 4.24 FFT spectrum with Nyquist rate input frequency after timing skew calibration

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4.4 Summary

This chapter provides the detailed content of circuit implementation and simulation. And the performance metrics of this work in C-CC post-layout simulation are listed in Table 4-1.

Table 4-1 Performance summary of post-layout simulation for the proposed ADC

	This Work
	Post-simulation
Technology	TSMC 40nm CMOS GP
Voltage	1.2V
Resolution	6-bit
Area	780×250 μm^2
Input Swing	0.8 V_{pp}
Sampling Rate	8 GS/s
Input Frequency	3.78 GHz (Nyquist rate)
Power	39.92 mW (Exclude the clock buffer)
SFDR	47.15 dB
SNDR	36.13 dB
ENOB	5.71 -bit
Figure of Merit	95.33 fJ/conversion-step

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Chapter 5

Measurement Results

5.1 Introduction

In this section, several topics related to the measurement of this work are discussed. First, floor plan and layout are described. Second, the design of print circuit board (PCB) is demonstrated. Third, test setup is introduced. Fourth, we show and discuss measurement results. Finally, summary table is presented.

5.2 Floor Plan and Layout Design

The floor plan of time-interleaved SAR ADC is shown in Fig.5.1, and the floor plan of signal-channel is in Fig.5.2. The path of analog input signal is from top of the chip and it is tree structure for equal delay. On the other hand, the clock signal goes from the bottom of the chip to separate the disturbance from the input signal, and it is also the same layout style as the input signal. The separation of digital and analog power supply is to avoid transient noise generated by digital signals. Besides, the power supply of clock generator and out buffers are segregated to prevent the large transient current. Each supply voltage has their own decoupling capacitors to stabilize supply voltage.

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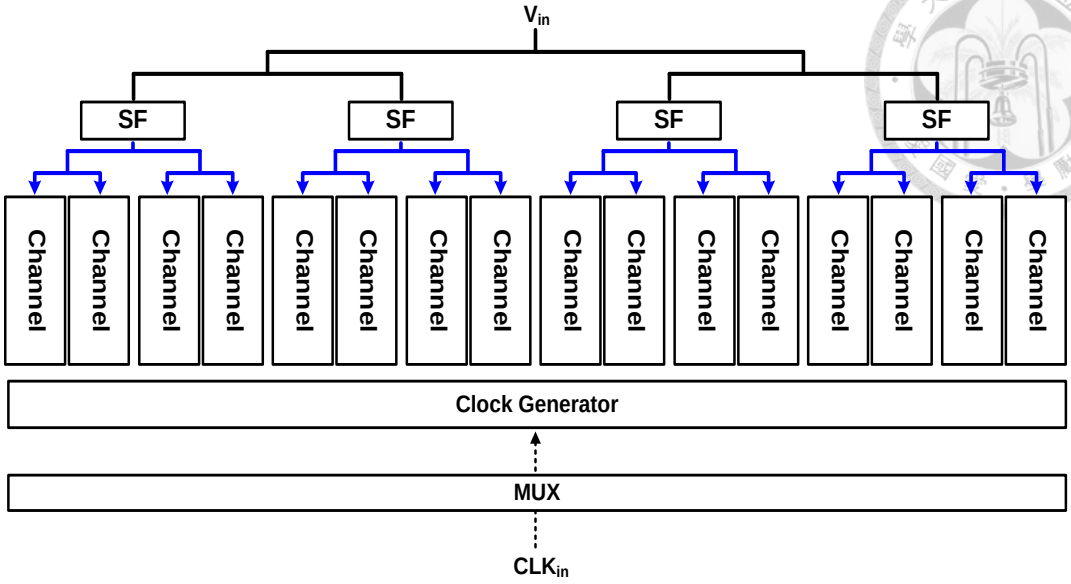

Fig. 5.1 Floor plan of proposed time-interleaved SAR ADC

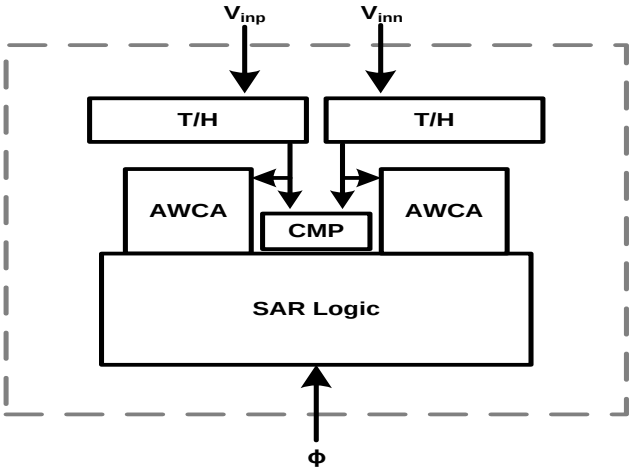

Fig. 5.2 Floor plan of single-channel SAR ADC

The layout of ADC is shown in Fig. 5.3. It is implemented in TSMC 40nm CMOS general-process (GP). Table 5-1 describes functions of the 55 pins.

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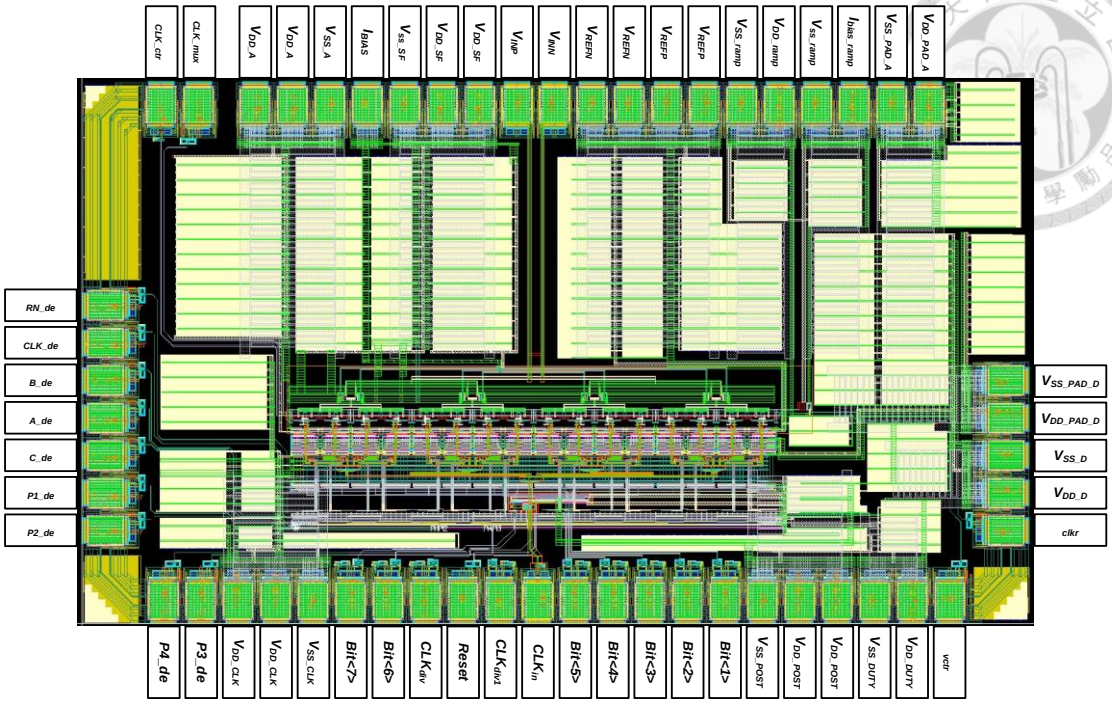

Fig. 5.3 Layout of proposed time-interleaved SAR ADC

Table 5-1 Functions of 55 pins in proposed ADC

Name	Description
V_{INP}	Positive input signal
V_{INN}	Negative input signal
V_{REFP}	Positive reference voltage
V_{REFN}	Negative reference voltage
V_{DD_A}	Analog supply
V_{SS_A}	Analog ground
I_{BIAS}	Input current for SF's biasing circuit
V_{DD_SF}	SF supply
V_{SS_SF}	SF ground
V_{DD_D}	Digital supply
V_{SS_D}	Digital ground
V_{DD_DUTY}	Other digital CKT supply
V_{SS_DUTY}	Other digital CKT ground
V_{DD_POST}	POST CKT supply

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V_{SS_POST}	POST CKT ground
V_{DD_CLK}	CLK GEN supply
V_{SS_CLK}	CLK GEN ground
$V_{DD\_PAD\_A}$	Analog pad supply
$V_{SS\_PAD\_A}$	Analog pad ground
$V_{DD\_PAD\_D}$	Digital pad supply
$V_{ss\_pad\_d}$	Digital pad ground
CLK_{in}	Clock signal
CLK_{div}	Clock for output sampling
CLK_{div1}	Clock of CH_1 for output sampling
Bit<7:1>	Digital output bit
P<1:3>_de	Decoder signal
<A:C>_de	Decoder signal
RN_de	Decoder signal
CLK_de	Decoder signal
CLK_mux	Timing skew control signal
CLK_ctr	Timing skew control signal
vctr	Timing skew control signal
V_{DD_RAMP}	Timing skew control supply
V_{SS_RAMP}	Timing skew control ground
I_{BIAS_RAMP}	Timing skew control supply

5.3 PCB Design

The goal of PCB design is to provide a platform which offers good test environment for ADC. Power and ground noises are generated by current which flows through power and ground lines which have equivalent series resistance (ESR) and equivalent series inductance (ESL). This noise will degrade performance. Hence, careful design of the AC current feedback path is very important. Four-layer PCB is employed to provide a power and a ground plate. Both plates have large area, so the low

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resistance and inductance are achieved to lower power and ground noise. Every set of power and ground is decoupled by some 10 uF, 0.1 uF, and 0.01 uF capacitors. Three different capacitor values are used to filter out noise in different frequency band.

Fig. 5.4 shows the schematic of an analog input on PCB. Two types of configuration of RF transformer are used for different requirement of input bandwidth. A single-ended analog input signal is converted to differential one by a RF transformer. Table 5-2 shows the specification of RF transformers which are used in our measurement [38]–[40]. However, different types of RF transformers impact differently on ADC. This issue is discussed in Section 5.6.

Table 5-2 Specification of RF transformers

RF transformer	Frequency Range (MHz)
ADT4-1WT	2 - 775
JTX-4-10T	50 - 1000
TCM4-14+	200 - 1400
TCM4-452X+	20 - 4500

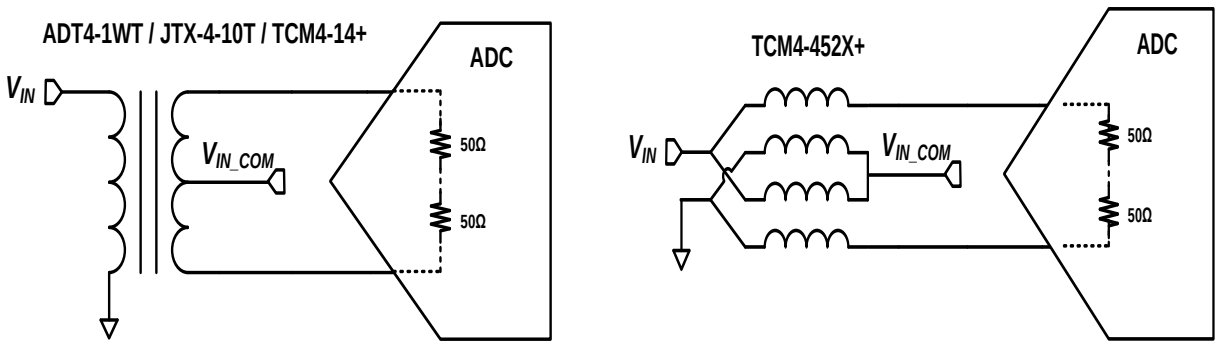

Fig. 5.4 Schematic of analog input on PCB

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Fig. 5.5 shows the schematic of reference voltages on PCB. A master reference voltage is produced by a Zener diode (LM385) to provide stable 2.5 V. The master reference voltage is connected to four variable resistors and generates four reference voltages including V_{REFP}, V_{REFN}, V_{IN_COM}, V_{DD_SF}, and V_{DD_A}. The five reference voltages are buffered by OPAMP (AD8031) which is utilized as a unit gain buffer. Three capacitors, which values are 10 uF, 0.1 uF and 10 nF, are also used to decouple the reference voltages. The master reference voltage also generates current reference I_{BIAS} by connecting additional variable resistor between output terminal of AD8031 and input terminal of the chip.

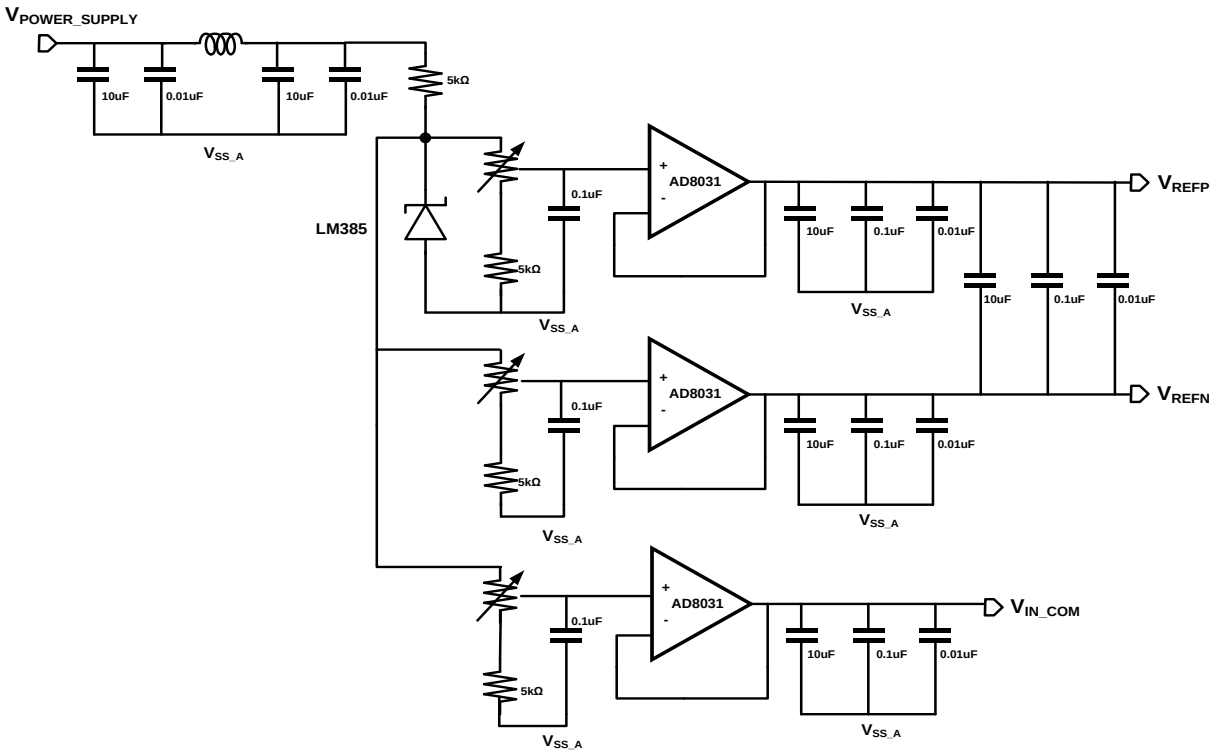

Fig. 5.5 Schemtaic of reference voltage on PCB

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Fig. 5.6 shows the schematic of power supplies on PCB. The power supplies V_{DD_D}, V_{DD_POST}, V_{DD_DUTY}, V_{DD_CLK}, $V_{DD\_PAD\_A}$ and $V_{DD\_PAD\_D}$ are generated by voltage regulators (LT3020). Three capacitors, which values are 10 uF, 0.1 uF and 10 nF, are also used to decouple the power supply as well.

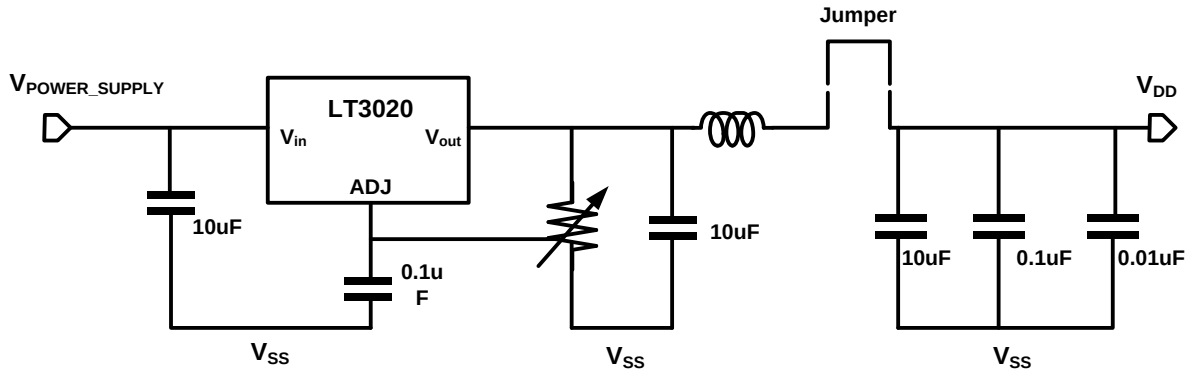

Fig. 5.6 Schematic of power supplies on PCB

The ground and signal of PCB is configured as Fig. 5.7. The mother board is used to provide the master reference voltage and power supply generation. V_{SS_A}, V_{SS_D}, $V_{SS\_PAD\_A}$, $V_{SS\_PAD\_D}$, V_{SS_POST}, V_{SS_DUTY}, and V_{SS_CLK} are not connected to each other in the chip, but on PCB by the ferrite beads and copper lines to achieve better performance. On the other hand, the daughter board is mainly used to connect analog input signal and clock signal. In this way, the daughter board can separate noise of power supply from mother board. It also decrease bond-wire effect from solder and thus the high-speed signal can be imported to the chip. Fig. 5.8 shows the photo of whole PCB with time-interleaved

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ADC chip and all the components used on the PCB platform are listed in Table 5-3.

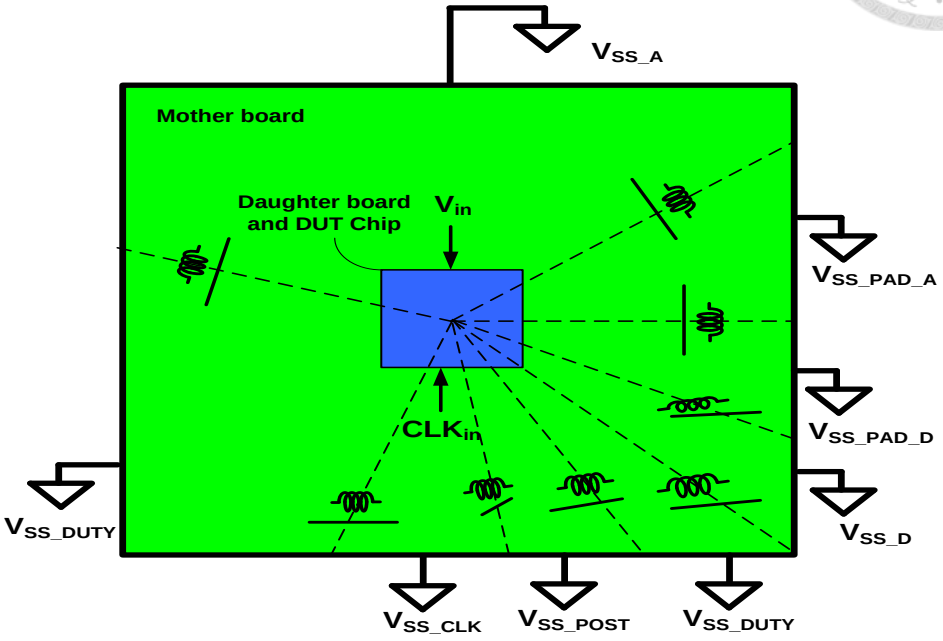

Fig. 5.7 Ground and signal of configuration on PCB

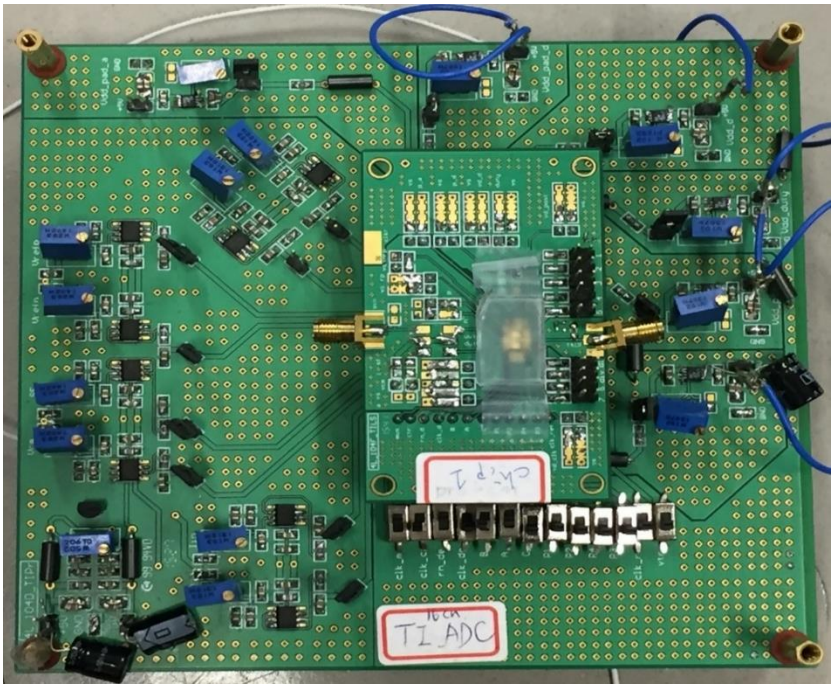

Fig. 5.8 Photo of whole PCB with time-interleaved ADC chip

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Table 5-3 List of materials

Item	Description	Manufacturer
LT3020	Low Dropout Linear Regulator	Linear Technology
AD8031	Operational Amplifier	Analog Device
LM385	Adjustable Micro-power Voltage Reference	National Semiconductor
ADT4-1WT / JTX-4-10T/ TCM4-14+ / TCM4-452X+	Transformer	Mini-Circuits
10μF / 0.1μF / 10nF	Tantalum Capacitor	
1kΩ / 5kΩ / 10kΩ	Variable Resistor	
Ferrite Bead		
Jumper		
SMA		
switch		

5.4 Test Setup

Test setup is shown in Fig. 5.9. Two signal generators (Agilent E8257D and SMA100) are applied to generate a clock signal and an analog input signal. Both signals are filtered by passive band-pass-filter (BPF) and separately connected by SMA cables. To convert the single-ended analog input signal to differential one, a RF transformer is chosen. The power supplies of design-under-test (DUT) are generated by voltage regulators (LT3020). A 7-bit digital output is captured by a mix signal oscilloscope (MSO4034). The digital output is downloaded to a personal computer (PC) and processed by MATLAB to obtain static and dynamic performance. The equipment photos of Agilent E8257D, SMA100, and PPT-3615 are shown in Fig. 5.10.

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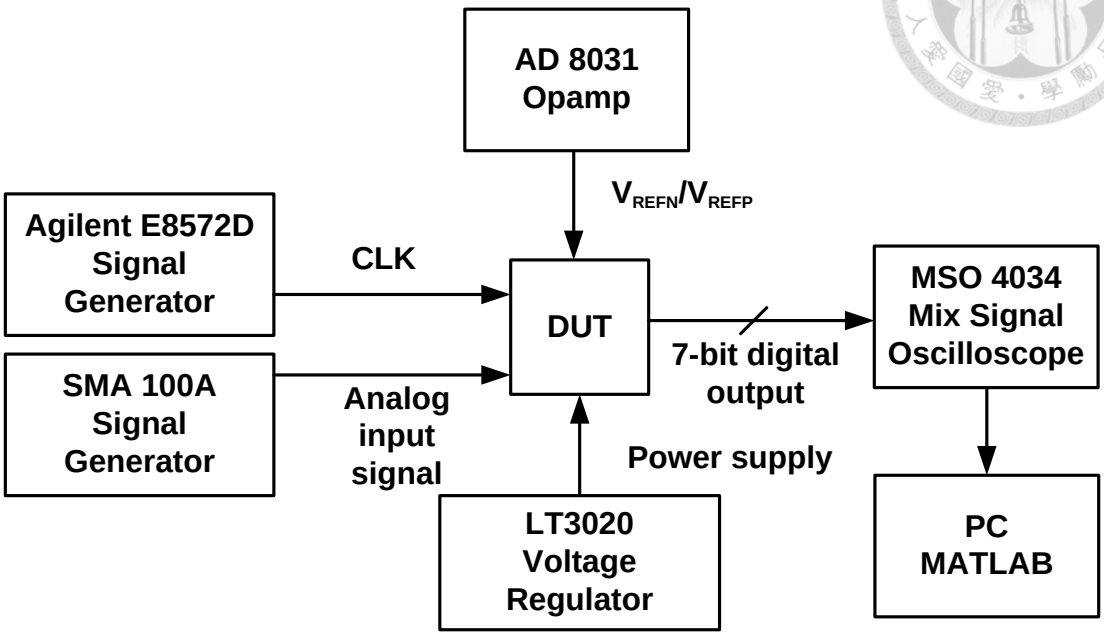

Fig. 5.9 Test setup

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(a)

(b)

(c)

Fig. 5.10 Photos of (a) E8257D, (b) SMA100, and (c) PPT-3615

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5.5 Measurement Results

Fig. 5.11 shows the die phot of the ADC fabricated in TSMC 40 nm CMOS 1P10M process. The chip area is 1500*850 μm^2 = 1.275 mm^2. The core circuit occupies an area of 780*250 μm^2 = 0.195 mm^2.

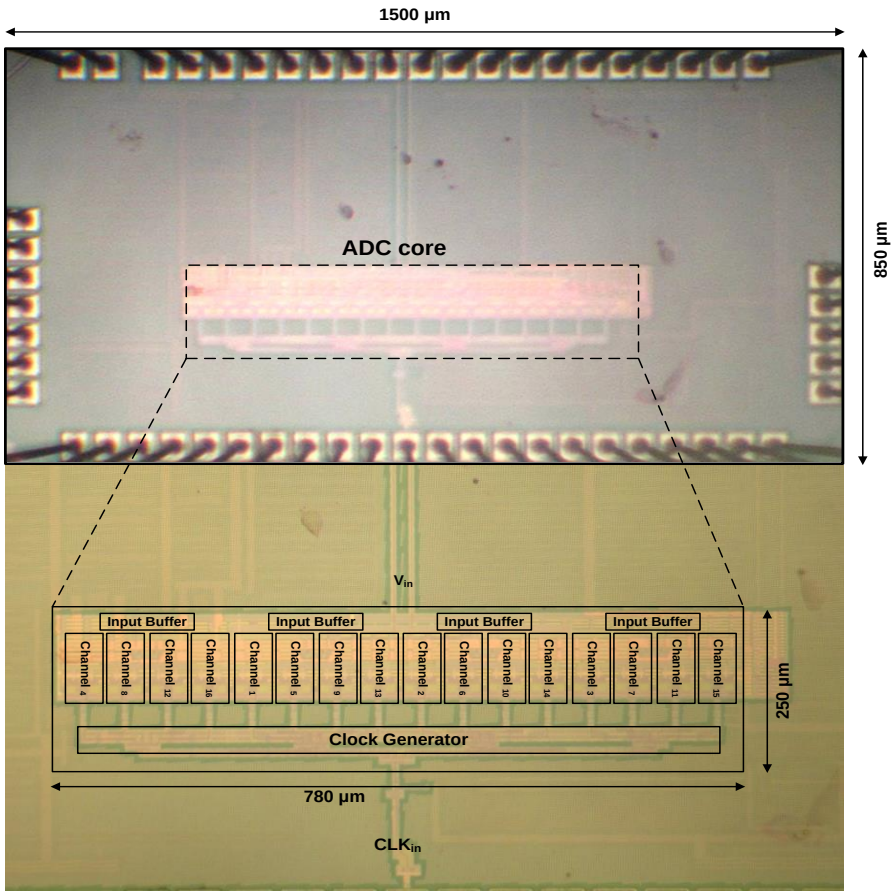

Fig. 5.11 Die photo of the time-interleaved ADC

5.5.1 Static Performance

Static performance of ADC is measured at 1.2 V supply voltage while sampling rate is 4 GS/s and input frequency is 50.78 MHz. Fig. 5.12 shows DNL and INL of the single-channel ADC. The DNL and INL are +0.15/-0.13 LSB and +0.14/-0.11 LSB. On the other hand, DNL and INL of the time-interleaved

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ADC are shown in Fig. 5.13. The DNL and INL of the time-interleaved ADC are +0.17/-0.29 LSB and +0.20/-0.18 LSB.

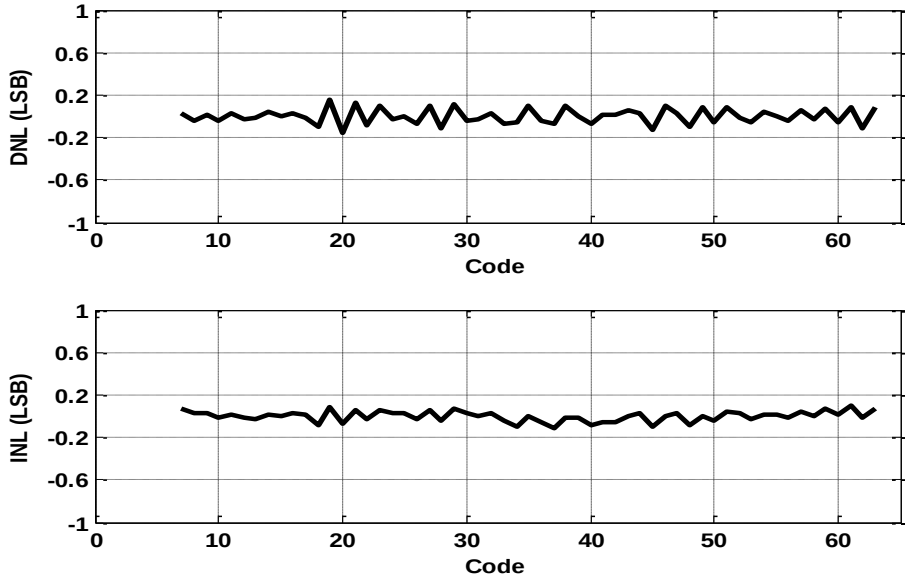

Fig. 5.12 DNL and INL of the single-channel ADC

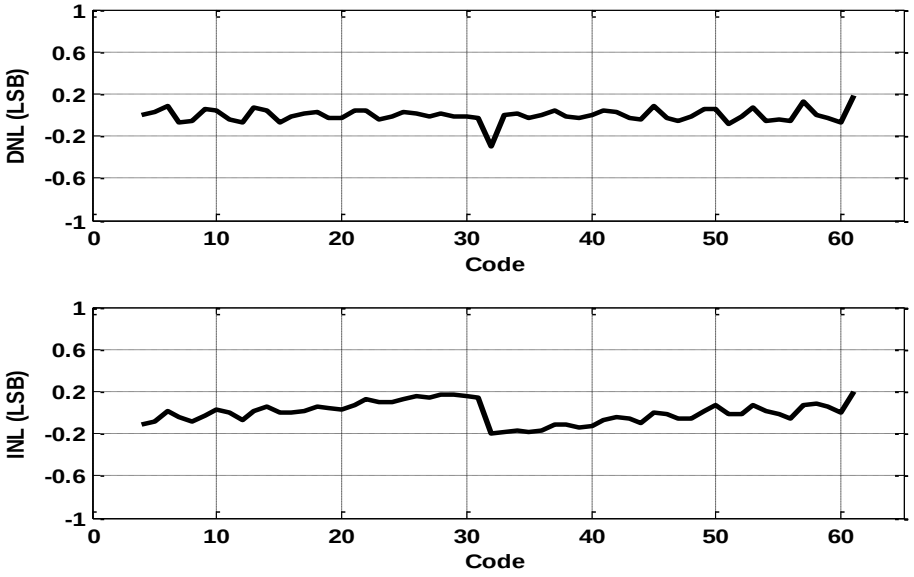

Fig. 5.13 DNL and INL of the time-interleaved ADC

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5.5.2 Dynamic Performance

Fig. 5.14 shows the 1024-point FFT spectrums with sampling rate, F_s of 4 GS/s and input frequency, F_{in} of 50.78 MHz. The SFDR and SNDR are 51.33 dB and 35.33 dB respectively. The maximal input frequency is limited by types of RF transformers. A RF transformer (JTX-4-10T+) is used to measure dynamic performance of ADC. Its input frequency range is from 50 MHz to 1 GHz [38]. On the other hand, RF transformers (TCM4-14+) and (TCM4-452X+) whose input frequency range are higher than 1 GHz [39], [40]. It is discussed in Section 5.6 because RF transformers (TCM4-14+) and (TCM4-452X+) cause harmonic distortion on the ADC.

With F_{in} near 1 GHz and F_s of 4.5 GS/s, the 1024-point FFT spectrums is shown in Fig. 5.15. Before offset and gain calibrations, SFDR and SNDR are limited to 29.37 dB and 24.50 dB. Tones caused by offset mismatch are around -30 dB to -40 dB and degrade performance. Offset and gain mismatches are corrected by the method in Section 3.3.1.2. After offset and gain calibrations, the SFDR and SNDR are improved to 41.04 dB and 32.15 dB. The output of ADC is decimated by 125.

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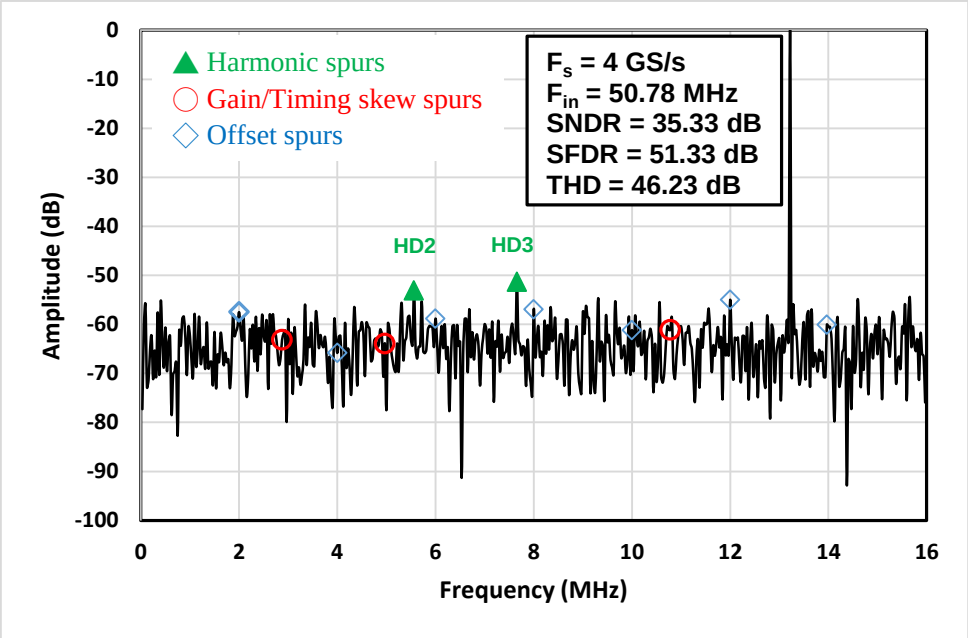
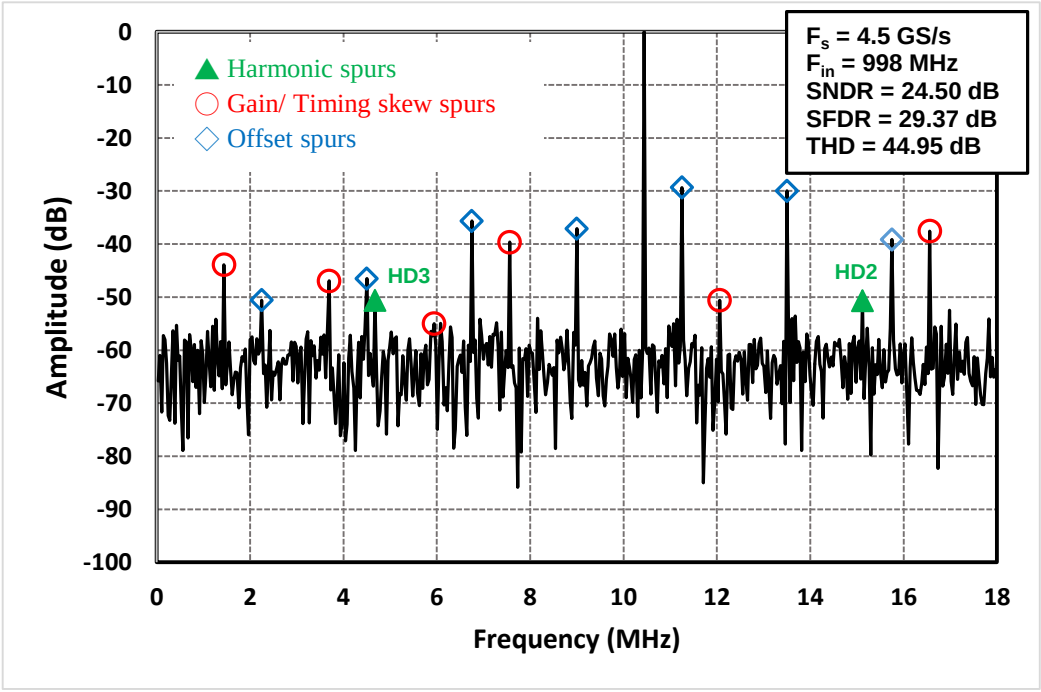


Fig. 5.14 FFT spectrum for F_{in} = 50.78 MHz (decimated by a factor of 125)



(a)

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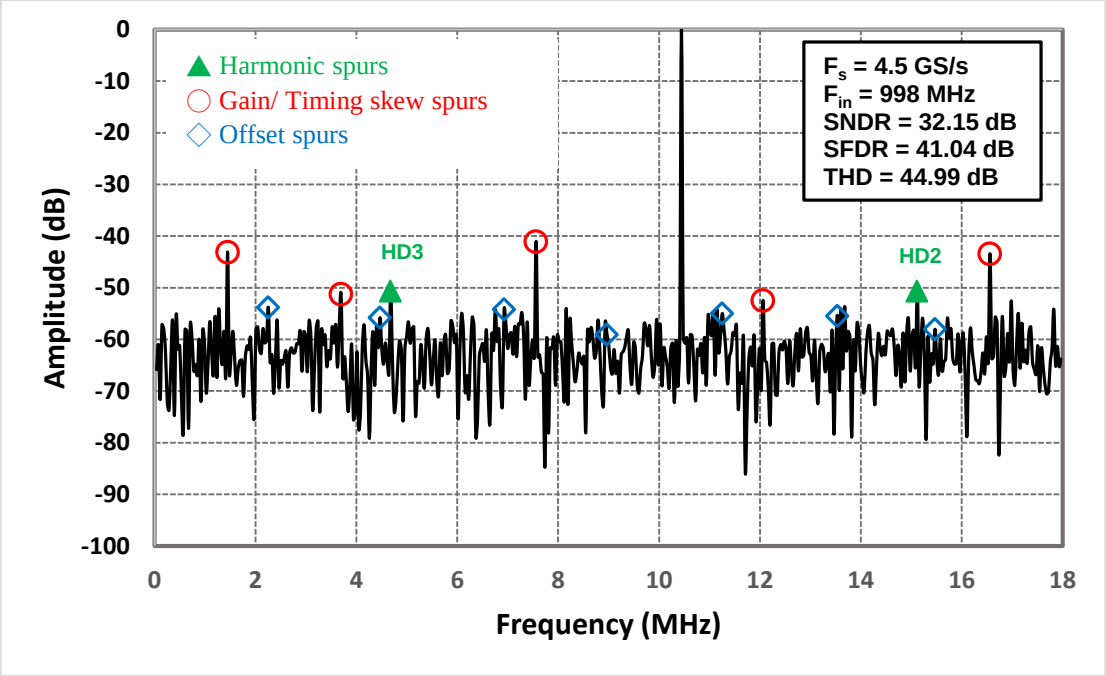

(b)

Fig. 5.15 FFT spectrum for F_{in} = 998 MHz (a) before, and (b) after offset and gain mismatch calibration (decimated by a factor of 125)

Fig. 5.16 illustrates the dynamic performance versus input frequency when F_s is 4.5 GS/s. SNDR stays above 32 dB up to F_{in} of 1 GHz. The definition of THD in Chapter 5 is a reciprocal of (2.4) to compare with SNDR and SFDR. Both SFDR and THD stay above 40 dB up to F_{in} of 1 GHz. SNDR and SFDR versus sampling frequency with F_{in} of 50 MHz is shown in Fig. 5.17. The SNDR maintains above 35 dB up to F_s of 5 GHz with F_{in} of 50 MHz.

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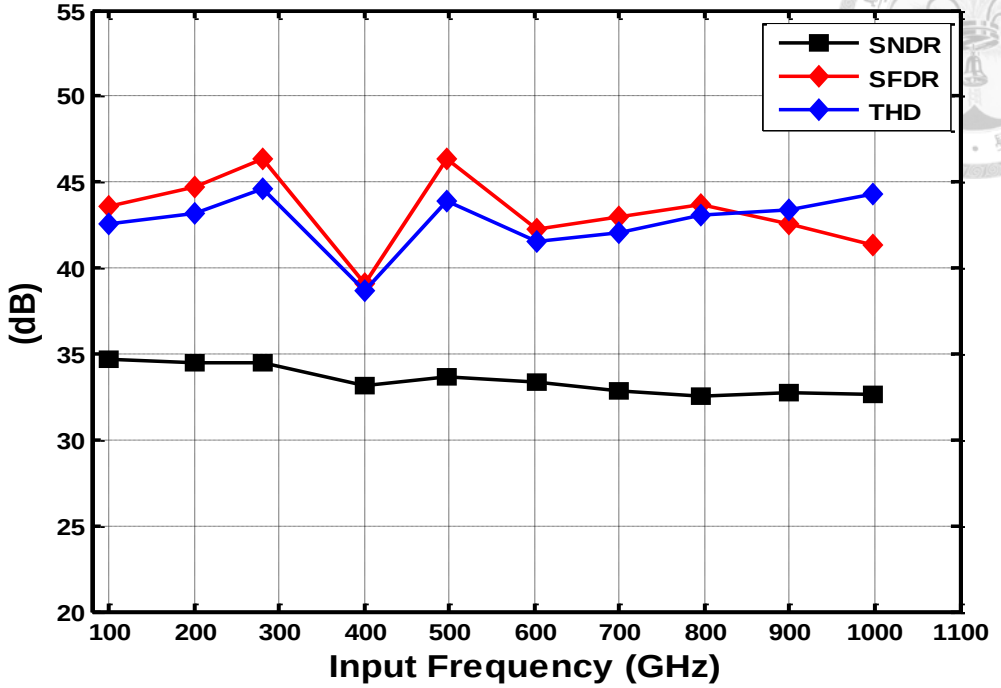

Fig. 5.16 SNDR, SFDR and THD versus input frequency at F_s = 4.5 GS/s

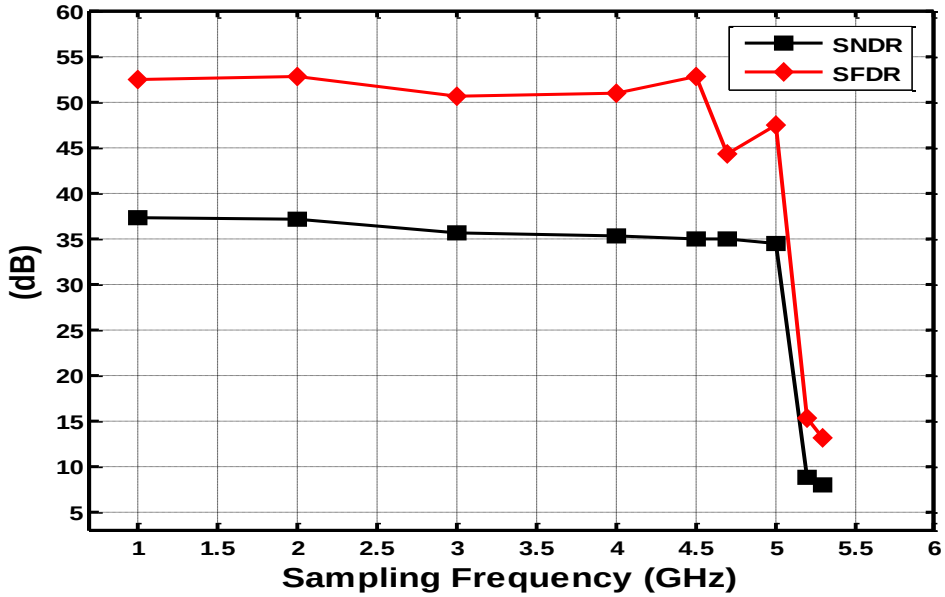

Fig. 5.17 SNDR and SFDR versus sampling frequency with F_{in} of 50 MHz

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5.6 Discussion

In this section, first, we discuss the effect on the dynamic performance of ADC with different RF transformers. Second, analysis of timing skew for simulation and measurement is discussed.

5.6.1 Dynamic performance with different RF transformers

Fig. 5.18 and Fig. 5.19 are the measurement when a RF transformer (TCM4-14+) is used. The input frequency range of a RF transformer (TCM4-14+) is from 200 MHz to 1400 MHz [39].

Fig. 5.18 shows the 1024-point FFT spectrums with sampling rate, F_s of 4 GS/s and input frequency, F_{in} of 1 GHz. SFDR and SNDR are 37.18 dB and 29.98 dB. THD is -36.9 dB. As described in Section 5.5.2, a RF transformer (JTX-4-10T+) whose input frequency range is from 50 MHz to 1 GHz [38]. When FFT is compared with that using a RF transformer (JTX-4-10T) at F_{in} of 1 GHz in Fig. 5.15 (b), the 2^{nd} harmonic tone increases 18 dB and becomes 37.18 dB, while THD becomes worse from 44.26 dB to 36.9 dB. It means that RF transformers (TCM4-14+) causes more harmonic distortion power and performance of ADC is limited. Fig. 5.19 shows SNDR, SFDR and THD when input frequency range is from 1 to 1.4 GHz. Although harmonic distortion degrades the dynamic performance, SNDR still maintains above 27 dB up to F_{in} of 1.4 GHz.

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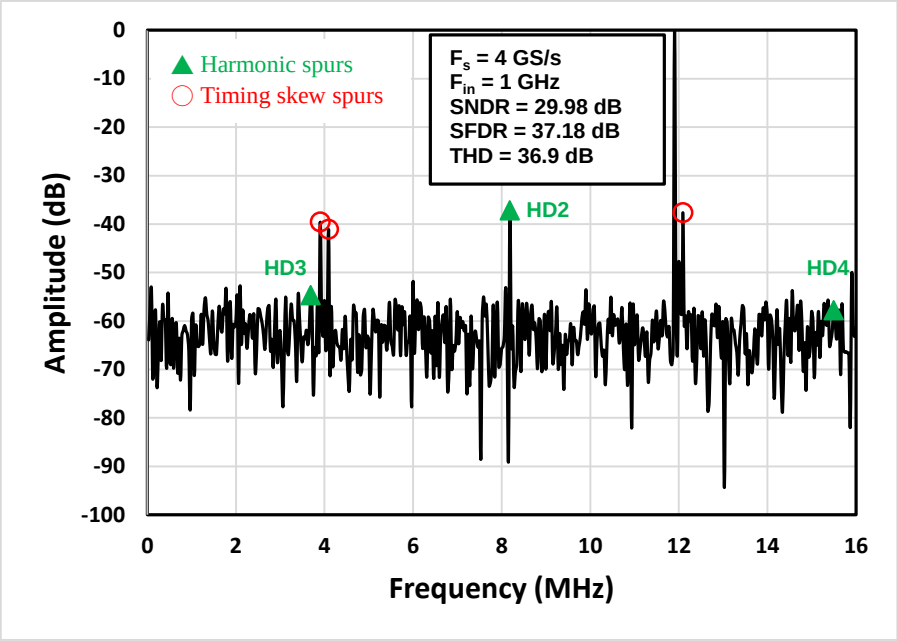

Fig. 5.18 FFT spectrum for F_{in} = 1 GHz with RF transformers (TCM4-14+)

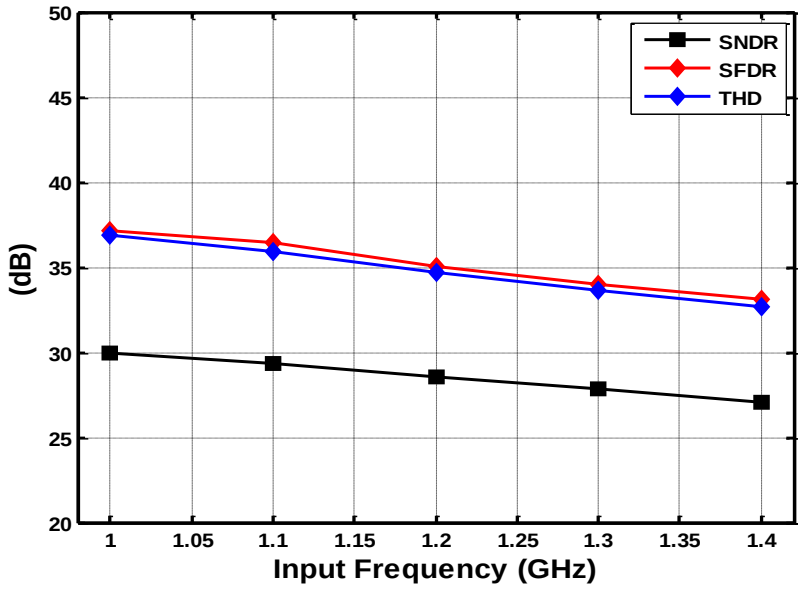

Fig. 5.19 SNDR, SFDR and THD versus input frequency range from 1 to 1.4 GHz

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The dynamic performance of ADC is presented in Fig. 5.20 when another RF transformer (TCM4-452X+) is used. The frequency range of a RF transformer (TCM4-452X+) is from 20 MHz to 4500 MHz [40].

As shown in Fig. 5.20 (a), in the time-interleaved ADC, when F_{in} is 707 MHz at F_s being 4 GS/s, the 2nd harmonic tone is -33.58 db and limits the SNDR to 29.26 dB and SFDR to 33.58 dB. In addition, THD is 33 dB, being the worst performance in three RF transformers. Fig. 5.20 (b) shows the FFT of single-channel at F_s being 4 GS/s and F_{in} being 707 MHz. The 2nd harmonic tone is -31.63 dB and also limits the SNDR to 28.91 dB and SFDR to 31.63 dB. When F_{in} is above 700 MHz, performance is even worse and SNDR is below 20 dB. Thus, F_{in} of 1 GHz is not discussed here.

Finally, we also use a double transformer providing differential input signal [37] to test whether harmonic tone can be improved. However, the result is nearly the same as the single transformer. A broadband power splitter PSPL5320B BALUN [41] provides the same function as a RF transformer. It may have lower harmonic distortion than RF transformers.

Therefore, we choose the measurement of ADC using a RF transformer (JTX-4-10T) under F_{in} of 1 GHz as a summary.

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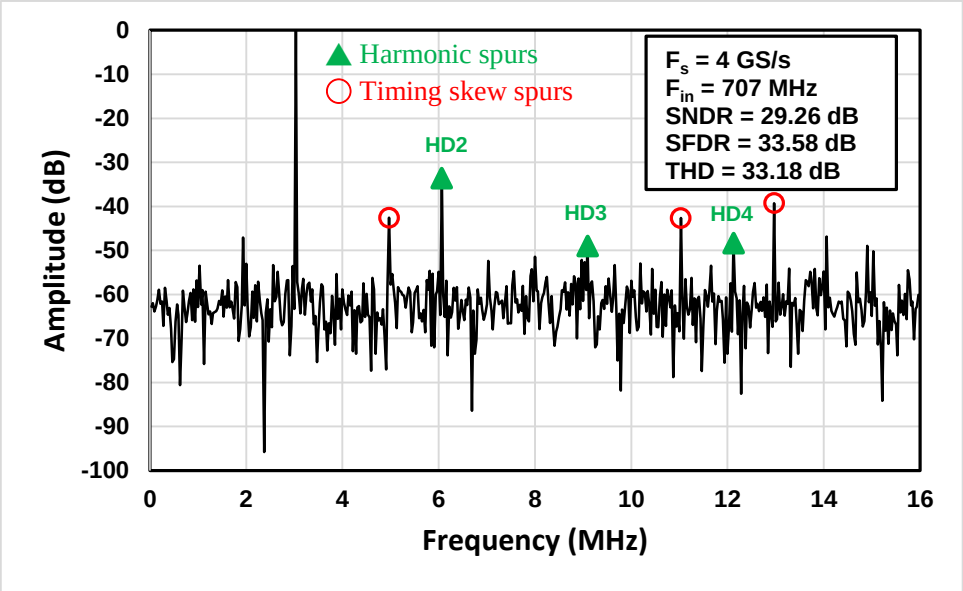
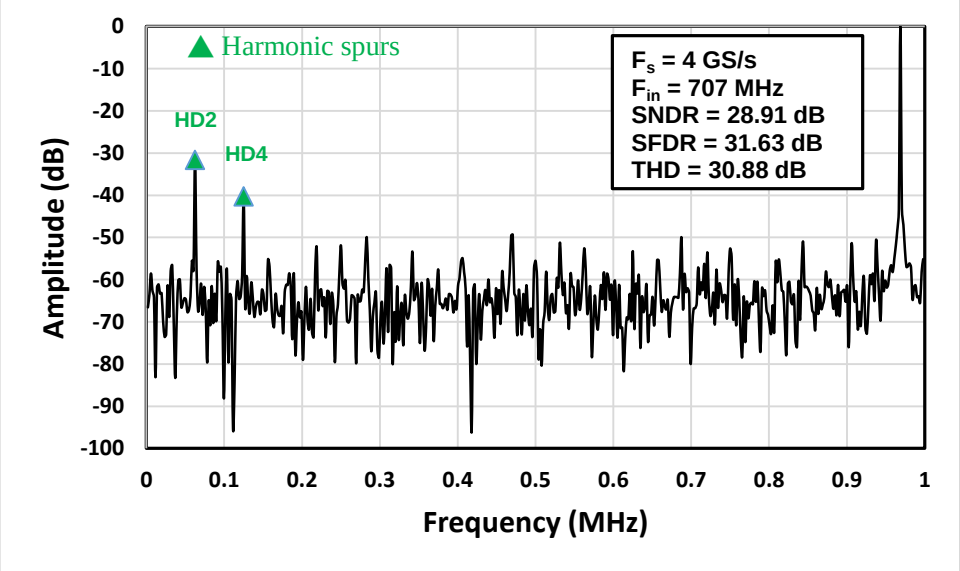


(a)



(b)

Fig. 5.20 FFT spectrum at F_{in} = 707 MHz (a) time-interleaved result (b) single-channel

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5.6.2 Analysis of timing skew for simulation and measurement

Timing skew for simulation and measurement is discussed as follows. First, we analyze how to obtain standard deviation of equal timing skew from FFT spectrum in measurement. There are two formulas of SNR_{skew} we use. One formula is from the definition of SNR in (2.3) plus the timing skew power. It is expressed as:

$$SNR_{skew(1)} = \frac{P_s}{P_q + P_{skew}} \tag{5.1}$$

where P_s is signal power, P_q is quantization noise power, and P_{skew} is timing skew power. P_s is $2^{2m-3}LSB^2$ and P_q is $\frac{1}{12}LSB^2$. As described in [8], P_{skew} is $\frac{(2^{m-1}LSB \times 2\pi f_{in}\sigma_t)^2}{2}$. This, (5.1) is written in another expression.

$$SNR_{skew(1)} = \frac{2^{2m-3}}{\frac{1}{12} + 2^{2m-1} \times \pi^2 f_{in}{}^2 \sigma_t{}^2} \tag{5.2}$$

where m is the resolution, f_{in} is input frequency, and σ_t is the standard deviation of timing skew.

According to [22], the other formula is expressed as

$$SNR_{\_skew(2)} = \frac{P_s}{P_q + 2^{2m-3} \times (\frac{9\pi^2 \sigma_t{}^2 f_{in}{}^2}{4})} = \frac{2^{2m-3}}{\frac{1}{12} + 2^{2m-3} \times (\frac{9\pi^2 \sigma_t{}^2 f_{in}{}^2}{4})} \tag{5.3}$$

From FFT spectrum of the measurement, we get values represents P_s, P_q, P_{skew} and these values are proportional to SNR_{skew}. If we find the ratio between formula and the measurement, σ_t is derived. For example, $P_s = 2.22 \times 10^8$, $P_q = 80909$ and $P_{skew} = 47394$ are from the FFT of measurement when F_{in} is 1 GHz. We obtain the following relationship between (5.2) and the measurement:

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$$\frac{2^{2m-3}}{\frac{1}{12}+2^{2m-1}\times\pi^2 f_{in}{}^2\sigma_t{}^2}=\frac{512}{\frac{1}{12}+11369\times10^{18}\sigma_t{}^2}=\frac{2.22\times10^8}{80909+47394} \quad (5.4)$$

where m=6 and $f_{in}=10^9$. Note that $\frac{1}{12}$ is the ideal quantization noise power of 6-bit resolution. However, P_q from the measurement is the quantization noise power adding other noise power. Thus, we take it into consideration and P_q is equal to 0.21 (ENOB=5.4b) from the measurement with low input frequency. Ideal $P_{q,}$ $\frac{1}{12}$ is replaced by 0.21 and (5.4) becomes

$$\frac{512}{0.21+11369\times10^{18}\sigma_t{}^2}=\frac{2.22\times10^8}{80909+47394} \quad (5.5)$$

Therefore, σ_t is obtained from $SNR_{skew(1)}$. Likewise, $SNR_{\_skew(2)}$ is used to calculate σ_t.

We substitute $SNR_{skew(1)}$ and $SNR_{\_skew(2)}$ into (5.5), and the range of σ_t in measurement is from 2.5 to 3.2 ps. However, the range of delay line in our design is only +1.8 ps as described in Section 4.2.4. Moreover, σ_t is calculated from timing skew in each channel in reality and the value of timing skew will be native and positive. The range of delay line cannot cover timing skew. Therefore, with F_{in} of 1 GHz, adjustment of delay line does not improve the SNDR which is limited by timing skew.

Second, post-layout simulation is checked to find the relationship between simulation and measurement. As described in Section 4.2.4, the C+CC post-layout simulation is calculated. Table 5-4 shows C+CC post-layout simulation of timing skew from adjacent channels. There are 16 values of timing skew and σ_t is 1.6 ps from these values. As shown in Fig. 4.13 (a), two stage of a clock generator have four ÷4 dividers. Values of timing skew in each ÷4 divider have nearly the same trend

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and we can divide these values of timing skew into 4 groups of timing skew.

Now, we restart to check σ_t through the consideration of parasitic resistors by R+C+CC post-layout simulation. Simulation of timing skew from adjacent channels are presented in Table 5-5. Maximum skew is 3.27/-3.58 ps and σ_t calculated from Table 5-5 is around 3.1 ps. From 4 groups of timing skew, we can divide these values into a trend: [-1, +3.2, -3.6, +1.2] ps. This trend of timing skew cause the spurs of timing skew occur as shown in Fig. 5.15 (b). There are three spurs of timing skew which all around -40 dB. The R+C+CC post-layout simulation result meets the measurement and notifies that R+C+CC post-layout simulation should be executed to ensure the range of delay line.

Table 5-4 C+CC post-layout simulation of timing skew from adjacent channels

	Group1		Group2		Group3		Group4	
Timing skew (ps)	dt_1	-0.55	dt_5	1.71	dt_9	-1.41	dt_{13}	0.49
	dt_2	-0.53	dt_6	1.69	dt_{10}	-1.43	dt_{14}	0.34
	dt_3	-0.55	dt_7	1.71	dt_{11}	-1.41	dt_{15}	0.04
	dt_4	-0.54	dt_8	1.67	dt_{12}	-1.35	dt_{16}	0.62

Table 5-5 R+C+CC post-layout simulation of timing skew from adjacent channels

	Group1		Group2		Group3		Group4	
Timing skew (ps)	dt_1	-0.99	dt_5	3.22	dt_9	-3.58	dt_{13}	1.22
	dt_2	-0.91	dt_6	3.26	dt_{10}	-3.44	dt_{14}	1.3
	dt_3	-1.15	dt_7	3.3	dt_{11}	-3.42	dt_{15}	1.78
	dt_4	-0.98	dt_8	3.27	dt_{12}	-3.6	dt_{16}	0.72

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Moreover, the different arrangement of timing skew in 4 group causes different variation on these three spurs of timing skew. Assume that 4 group timing skew are $\Delta_A, \Delta_B, \Delta_C, \Delta_D$ and their values are [-1, +3.2, -3.6, +1.2] ps respectively. If the arrangement of $\Delta_A, \Delta_B, \Delta_C, \Delta_D$ is changed, there will be totally six cases of arrangement as show in Table 5-6. Through MATLAB behavior, variation of three timing skew spurs in FFT is presented in Table 5-6. We conclude that there are three types of variation of timing skew spurs. The first type is case 1 and case 6. The measurement result is also this type. Spurs of three timing skew are all around -40 dB. Next, the second type is case 2 and case 4. In this situation, the amplitude of Spur 2 is around 35 dB and it is 8 dB higher than Spur 1 and Spur 3. The third type is case 3 and case 5. Spur 2 is around -65 dB and its amplitude is 28 dB lower than Spur 1 and Spur 3.

Table 5-6 Variation of timing skew spurs with different arrangement of timing skew

Case	Arrangement of timing skew	Spur 1 (dB)	Spur 2 (dB)	Spur 3 (dB)
1	$\Delta_A, \Delta_B, \Delta_C, \Delta_D$	-38.85	-40.62	-38.73
2	$\Delta_A, \Delta_B, \Delta_D, \Delta_C$	-44.18	-35.59	-43.32
3	$\Delta_A, \Delta_C, \Delta_B, \Delta_D$	-37.4	-64.67	-37.2
4	$\Delta_A, \Delta_C, \Delta_D, \Delta_B$	-43.23	-35.77	-43.64
5	$\Delta_A, \Delta_D, \Delta_B, \Delta_C$	-37.25	-66.18	-37.35
6	$\Delta_A, \Delta_D, \Delta_C, \Delta_B$	-39.17	-40.42	-41.44

Finally, besides the reconsideration of delay line, we try to reduce timing skew of the clock generator further. As shown in Fig. 4.13, the main source of timing skew is the layout routing that connects the output of first stage to the input of second stage in the clock generator. The layout routing

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includes clock phases Φ_{G1}~Φ_{G4}. Fig. 5.21 shows the floor plan of the clock generator. From this design, we increase routing length to make clock phases Φ_{G1}~Φ_{G4} have the same length. The length Φ_{G1}~Φ_{G4} is nearly 280 um.

However, we discover that if the routing length of Φ_{G1}~Φ_{G4} is compressed as short as possible, timing skew will decrease although Φ_{G1}~Φ_{G4} does not have the same length. Fig. 5.22 is the new floor plan of the clock generator. The length of Φ_{G1}~Φ_{G4} is reduced to 50 um. In addition, as shown in Fig. 5.23, routing of Φ_{G2}~Φ_{G3} are surrounded by a grounded shield consisting a higher and a lower metal layer to make Φ_{G1}~Φ_{G4} have the same parasitic capacitance. Table 5-7 shows the R+C+CC post-layout simulation of timing skew of the new version of layout. σ_t calculated from Table 5-7 is reduce to around 0.56 ps now.

In conclusion, through analysis between formulas and measurement, we obtain σ_t from measurement. Then, we restart to check post-layout simulation to ensure that the R+C+CC post-layout simulation meets the measurement. R+C+CC post-layout simulation should be executed to ensure the range of delay line. Finally, the new layout version of clock generator is tried to reduce timing skew.

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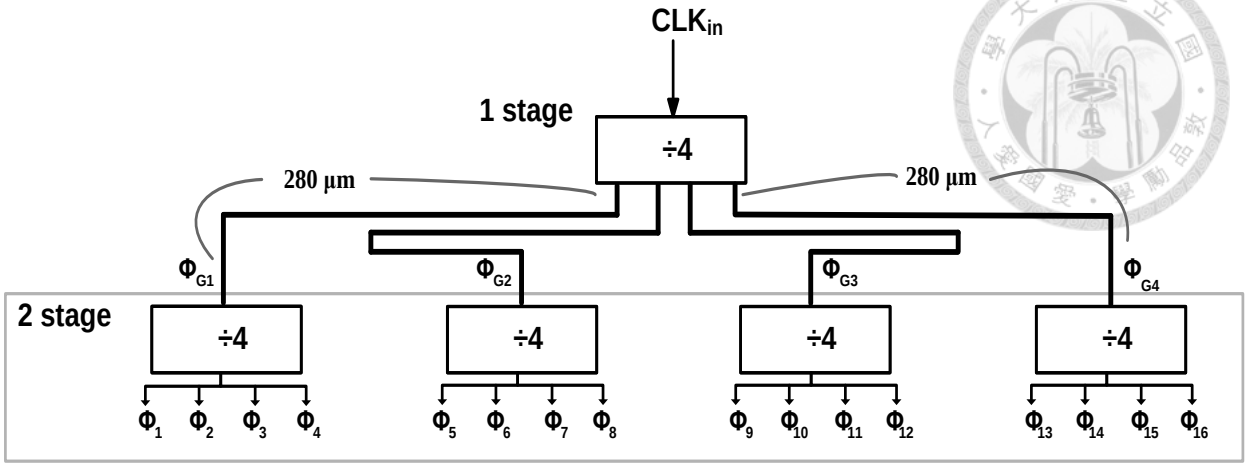

Fig. 5.21 Floor plan of the clock generator

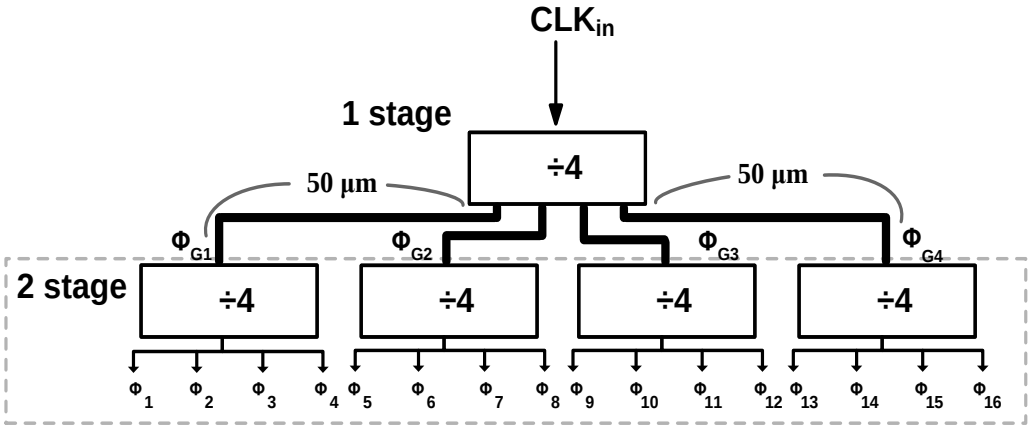

Fig. 5.22 New floor plan of the clock generator

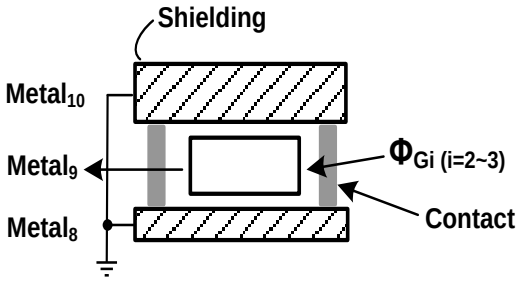

Fig. 5.23 Shielding a clock phases $\Phi_{Gi\ (i=2\sim3)}$

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Table 5-7 R+C+CC post-layout simulation of timing skew of the new version of layout

	Group1		Group2		Group3		Group4	
Timing skew (ps)	dt_1	0.005	dt_5	0.59	dt_9	-0.75	dt_{13}	0.26
	dt_2	0.0009	dt_6	0.71	dt_{10}	-0.75	dt_{14}	0.04
	dt_3	-0.0009	dt_7	0.69	dt_{11}	-0.79	dt_{15}	0.5
	dt_4	0.05	dt_8	0.74	dt_{12}	-0.82	dt_{16}	0.4

5.7 Summary

Table 5-8 shows the comparison with previous high-speed, low-to-medium resolution TI ADCs (with 6 – 8 bit resolution). Power consuming proportion is shown in Fig. 5.24.

Table 5-8 Time-interleaved ADC Comparison Table

Parameter	**This work**	JSSC 2012 [17]	ASSCC 2013 [34]	TVLSI 2014 [35]	TCAS-I 2015 [36]	JSSC 2016 [42]
Architecture	**TI-SAR**	TI-Subranging	FATI-SAR	TI-SAR	TI-SAR	TI-SAR
Technology (nm)	**40**	65	45	65	40 (LP)	65
Sample rate (GS/s)	**4.5**	2.2	2	2.5	2.64	5
# of channels	**16**	4	4	12	16	4
Supply Voltage (V)	**1.2**	1	1.2	1.2	1.2	1
Resolution (bit)	**6**	7	6	6	8	6
Power (mW)	**24.9**	40	14.4	22	39	5.5
$SNDR_{peak}$ (dB)	**35.1**	38.9	35.5	32	42.7	30.76
$SNDR_{Nyq.}$ (dB)	**32.2**(1)	38	33.1	31.9	37.9	30.25
FoM (fJ/c.-s.)	**159**(1)	280	195	270	230	39
Area (mm^2)	**0.2**	0.3	0.16	0.27	0.17	0.09

(1) SNDR under F_{in} of 1 GHz

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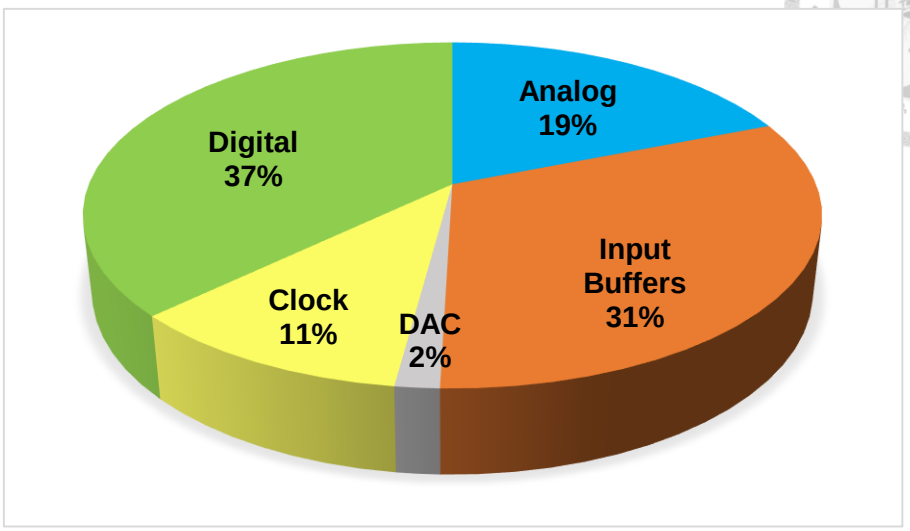

Fig. 5.24 Power consuming proportion of the proposed ADC

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Chapter 6

Conclusions

In this thesis, a 16-channel 6-bit 4.5Gs/s time-interleaved SAR ADC is realized in TSMC 40nm GP. Combining the front-end input buffers and the grouping technique into time-interleaved architecture, proposed ADC achieves the performance of high-speed sampling rate and high input bandwidth. Gain and offset mismatch between ADCs are calibrated in the digital domain. A zero-crossing detection technique is employed to correct timing skew mismatch. Asynchronous processing and monotonic capacitor switching technique used in the single-channel SAR ADC makes the sub-ADC high power-efficiency. AWCA technique solves the dynamic offset problem in the comparator of the sub-ADC.

The whole chip including pads occupies 1.275 mm^2 while area of core circuit is 0.195 mm^2. The measurement results show that DNL is +0.17/-0.29 LSB and INL is +0.20/-0.18 LSB at 4 GS/s with F_{in} of 50 MHz. SNDR and SFDR are 32.15 dB and 41.04 dB at 4.5 GS/s with 1 GHz input frequency by applying offset and gain calibrations. Timing-skew match is not improved because the range of delay line is insufficient. The power consumption is 24.9 mW at 1.2 V supply voltage. As a result, the FoM is 159 fJ/conversion-step.

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Chapter 7

Future Work

First, in order to make the performance of ADC not be limited by harmonic distortion when F_{in} is above 1 GHz, there are some methods which may improve the issue. First, different transformers and splitter should be tested. A broadband power splitter PSPL5320B BALUN [41] provides the same function as RF transformers. It may has lower harmonic distortion than RF transformers. Second, the operation of RF transformers may degrade due to input buffers with effect of bond wire, the low-dropout regulator is added to suppress bond-wire effect.

Second, when F_s of ADC requires operating above 5 GHz, some suggestions are provide. The input common mode of a clock buffer should be designed off-chip to avoid bond-wire effect. The low-dropout regulator would be added to make the power supply of a clock buffer clean. Moreover, if a differential clock generator is used, the frequency provided by an external signal generator will be half F_s of ADC and bond-wire effect will be halved.

Finally, for the calibration of timing skew, the estimated timing skew should take R+C+CC post-layout and the Monte Carlo simulation into consideration. And thus the simulated timing skew will fit the measure result. The total range of delay line should be over the $\pm 3\sigma$ of timing skew to ensure the range of calibration.

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