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Master Thesis

應用於穿戴式裝置之
極低電壓無線收發機

Ultra-low-voltage Wireless Transceiver for Wearable Applications

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口試委員會審定書

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本論文係王則惟君（R02943032）在國立臺灣大學電子工程學研究所完成之碩士學位論文，於民國 105 年 07 月 20 日承下列考試委員審查通過及口試及格，特此證明

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Ultra-low-voltage Wireless Transceiver for Wearable Applications

By
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THESIS

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To My Dear Family

謹獻給我的家人

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謝辭

碩士生涯即將告一段落，這三年來的點點滴滴難以一言道盡。從換實驗室到參加研究生協會以及小海豚舞蹈社，還有在碩士遇到了重要的人，即便最後無法畫上完美的句點，但內心卻是充滿對各位的感謝。

首先必須感謝父母對我的支持以及關心，在碩士生涯的途中曾遇過無數次的挫折，多虧了家人們的鼓舞以及建議才讓我能夠度過難關。

再來要感謝我的指導教授林宗賢博士這些年來的照顧，接納我這位原本不屬於這間實驗室的研究生，同時對於我們的課外活動也樂觀其成。在電路設計上時有突破性的觀點讓我受益良多，而且能夠容忍我時常犯的小錯誤，也給予了我許多的機會表現，讓我的碩士生涯充實有內涵。

感謝我的口試委員曾英哲博士、黃柏鈞教授、陳信樹教授對於論文呈現的提點，使我可以從別的角度審視自己的作品，彌補了許多曾被我遺漏的觀念細節。

感謝電二實驗室的各位成員，能與你們一同參與研究以及大大小小的活動是我的榮幸。感謝畢業學長蔡宜霖、王邦全、陳建佑、林君豫、邱俊元奠定了實驗室無線通訊電路的基礎，為我的低電壓無線傳輸電路題目解決了許多困難。感謝已畢業學長翁展翔的指導，雖然研究領域與我大相逕庭，但報告時的電路觀點時常令我收穫良多。謝謝邱茂菱學長幫忙處理實驗室網路的問題，我雖身為實驗室的網管卻能力不足，多虧了學長的幫助才能夠度過難關。涂智展學長時有的電路分析觀念總是能夠激發我更深層的思考，謝謝學長時常的教誨。感謝陳姿穎學姐平日的人生觀解析，我雖然不常跟妳聊天但是很多觀念我都認同只是我沒說出來而已。

感謝 100 級的學長姐對我的熱心關懷。還記得剛進實驗室時人生地不熟，多虧了陳奕竹學長一開始的熱情招呼，還有魏子安學長一直很想借我錢幫忙我。劉映辰學姐是清大時我就有耳聞的人物，原本以為會有距離感，但進來實驗室後發

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現出乎我意料地活潑，也幫了我許多忙，萬分感謝。雖然在實驗室不常看到徐健倫學長，但是覺得學長是冷面笑匠，可惜沒有能夠更進一步的認識。再來是感謝何明諺學長一同跟我去國家晶片研究中心審查，第一次去面審的我也因為有學長所以比較沒那麼害怕。最後當然是要謝謝周帝吉學長跟我一同畢業，因為有您的存在讓我碩士生涯的最後一段路不會寂寞。

感謝 101 級的學長姐對我的照顧。同時身兼網管以及雲端的曾意婷學姐實在太過強大，幫了我好多忙，可惜我連您的十分之一的戰力都沒繼承到，連兆軒科技的電話都忘記了。如果沒有葉姿妤學姐在國科會計畫上的幫助，我無法想像我的碩士生涯會因為這計畫過得多痛苦，也因為有您的無私奉獻，讓我理解到回饋實驗室學弟妹的重要性。盛允楨學長的口頭禪-不行了、不行了真的是太好笑，雖然說平時不講話看起來有些嚴肅，但是跟人交談的內容都很好笑，研究實力也有目共睹，然後不行了這句口頭禪我已經傳下去了，別擔心會失傳。李峯文學長是我在實驗室第一個看到的地縛靈，很難想像怎麼可以天天都那麼早來實驗室，然後會做研究又很會打籃球真的是很厲害。何冠霖學長在最後的研究戰力大爆發令我印象深刻，超強的每天行程就是一直用溫度箱量測、量測、量測。

感謝同屆伙伴們的陪伴，生活規律的陳冠中、我的大學同學-吳政輝、地縛靈二號黃偉翔、效率一哥呂季桓。雖然我們這屆的畢業時間幾乎不一致，彼此在實驗室的重疊時間也少，不過在我遇到困難需要解決的時候，你們往往有意無意間幫了我很多忙，謝謝了。

103 級的學弟們珍重再見，能夠看著你們成長是身為學長我的福氣，尤其是洪福聯學弟的轉變更是令人驚訝,只是口頭禪永遠都那幾個:啊我就是那麼廢啊！死定了老師又要找我了！每天做報告就飽了啊！又怪我了！一開始遇見你們的時候還覺得你們這屆很沉悶孤僻，應該是邊緣人，沒想到一個個都是神藏不露。有很會煮咖啡的王鈺凱學弟，還有打 LOL 會轉性的林奕辰學弟，以及很少在實驗室出現然後桌子很亂的李季安學弟。各位學弟加油，實驗室位子快要不夠坐了，趕快在今年好好打包把位子讓出來吧。

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一群神經病之 104 級的學弟，我在實驗室好歹也有一段時間，但是從來沒看過個性如此鮮明的一屆。陳友康是最奇特的一個，雖然電路實力很強，但真的是很白爛。王敦儒真是有夠天才，不管學什麼都有夠快，但是平常不講話看起來有距離感就是了。邱琛育學弟看起來很沒自信，可是身體卻出乎意外地壯，加油要有自信一點！時常去健身的林聖穎學弟待人很和善，說話也滿有禮貌的，雖然會抨擊我看美女圖，但念在是有事實的基礎上就不跟你計較了。很常被霸凌也很沒自信的就是林登凱學弟，你也要加油，不要臣服於友康的惡勢力底下。還有就是從別的實驗室轉來外表看起來很天兵，腦子更天兵會把自己反鎖在浴室的陳翰群學弟，話說我覺得學弟你應該很受女生們的歡迎，要好好把握這個優勢。最後就是承接我計劃的李忠容學弟，辛苦你了，學長我能夠留給你的東西不多，只能夠靠平常嘴泡來舒緩你的壓力，你要加油，實驗室無線通訊電路的未來在你身上。

不好意思 105 級的學弟妹們雖然我都看過，但名字卻還沒辦法完全記起來，所以我就不一個個點名了。我想對你們說的是，當年我大四的時候，你們才是剛進大學的新鮮人。如今你們已經大學畢業準備念碩一，但你們絕對見不到碩四的我。我真的很爽你們知道嗎？沒有啦！我開玩笑的，我只是想表達時間過得很快，你們要好好把握時間，好好享受接下來的碩士生涯吧。

研究生協會是我碩一參加的社團，會進入這個社團是受到戴瑋珊會長的引領，很開心可以遇到大家。曾友嶸學長十分多采多藝，而且在社會議題上的堅持令我佩服。程巾芳學姐唱歌很好聽，陳力葦同學跟我一樣大學都是外校，所以莫名的有話題，還有跟我同屆的盧潔人很和善笑笑地很好聊，祝妳未來研究順利。

最後的段落當然是要獻給最愛的小海豚舞蹈社。大學的時候我是空白人，從來沒想過上研究所後能夠有機會跳到自己喜歡的舞蹈，更別提自己會變成社團那麼重要的角色。礙於篇幅的關係，其實致謝只能夠打一頁但我現在已經超過了很不好意思，所以就沒辦法把所有人都打出來，因為那可能有一百人以上。回正題，我的大學課本現在有些在許凱傑學弟身上，曾經我是個課本不外借的人，不過現在的我不太一樣，因為我覺得你滿有前途的，所以可以不用急著還我沒關係，我

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相信那些書對你很有幫助。還有怪里怪氣的蔡丞昊學弟，莫名其妙變得很夯，不過念在你很有上進心這部分我就原諒你，看著你也進步了很多，我心中也是無限感慨，之後有空再一起練舞吧。再來是腹黑高欣妤學妹，外表看似清純善解人意，但其實是演技一流，感謝妳某段時間一直聽我抱怨跟崩潰，要加油！看到自己喜歡的對象的時候不要逃跑，真愛是值得追求的。我知道實驗室工作很忙，但也要記得休息，沒錯就是在說妳彭郁茹學妹，妳已經瘦成人乾了，壓力再大真的會不得了，要記得人生旅途上不是一昧地給自己壓力就算是成長喔。然後是身材一直維持不變的吳駿杰，我是認真地建議要好好運動練身體，不只是為了把舞跳好，也是為了身體的健康。還有在女生堆裡好像很吃香的洪詠翔學弟，但是好像有點毛手毛腳，可以的話請克制一下，不然有人會吃醋，這是善意的提醒喔，好啦我開玩笑的，祝福你變老人之後也不要鬆懈練舞，要好好地聽音樂，你的很多舞蹈動作如果真的有對到點是很不賴的。外表看似可愛無害但其實打人很痛的李家欣學妹請記得要好好收斂自己的殺氣，要不然會把喜歡妳的男生都嚇跑的，然後我也很感謝妳聽我訴苦，雖然妳那時整個人都笑到翻過去了，再來我覺得妳其實可以不用那麼焦慮，要能夠適時放下一些事情，不用力求完美，更不用因為自己做不到一些事情就否定自己，要相信自己是很棒的人！還有我的女兒張杏瑜學妹，妳也要好好地努力面對自己，但是切記別鑽牛角尖，要懂得接納自己的一切，唯有如此，才能夠放開心胸，以便應付未來遇到的種種困難。最後是萌萌的徐嘉琪學妹，感覺起來有點沒耐性有時講話會太直，但這看似是缺點的特性事實上也是妳的優點。要加油之後別把自己搞得太忙，雖然我還是覺得妳仍然會莫名其妙答應別人一堆事情就是了。然後感謝妳畢業舞會當天的陪伴，那是個令我難以忘懷的美好回憶。

三年前的我從沒想到三年後的今天可以得到了這麼多的東西，如果可以，我想再多打個十頁也不為過，真的是很謝謝各位了。

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摘要

穿戴型裝置近年來已經成為全球業界與消費者熱烈關切的議題。為了達到長時間操作的目的，低功率消耗將會是電路設計上最主要的考量之一。對於負責處理傳送/接收訊號的無線收發機來說，更會是設計上的一大挑戰。

本論文提出了一個具有高能量效率，操作在 0.5V 供應電壓環境下，使用注入式鎖定技巧之低功耗高效能無線收發機，調變方面採用差動式二元相位偏移(D-BPSK)。

接收機部分主要是利用注入式鎖定的技巧，當接收之輸入訊號相位產生變化時，震盪器的輸出振幅會產生暫時性的改變，即相位變化將透過注入式鎖定技巧轉換為震盪器的振幅變化來完成解調。此架構不需閉迴路系統來完成相位同步，可大幅簡化系統架構，進而降低功率消耗。本作品使用台積電 0.18 微米製程，系統功耗為 0.97 毫瓦，靈敏度為-45dBm，最大資料傳輸量為 10 Mbps，在此資料傳輸量下能量效率為 97 pJ/b。

發送機部分也是利用注入式鎖定技巧，低頻相位資訊會經由相位選擇器選取後注入高頻振盪器，當低頻的相位發生改變，高頻振盪器便會重新鎖定並且改變相位來完成調變。此架構因為不需產生高頻多相位的振盪訊號，因此可有效降低整體功率消耗。本作品使用台積電 0.18 微米製程之模型來進行模擬，整體系統功耗為 0.297 毫瓦，最大輸出功率為-9.7dBm，能量效率為 29.7 pJ/b，最大資料傳輸量為 10 Mbps，在此資料傳輸量下誤差向量幅度為 13%。

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Abstract

Wearable devices have been popular issues in recent years. Low power consumption is an important design target for the purpose of long-time usability. It's also an enormous challenge for wireless transceivers circuit design.

This thesis proposes an energy-efficient injection-locked transceiver which operates at 0.5V voltage supply. The D-BPSK modulation and demodulation are adopted for this system.

The proposed receiver adopts injection-locked technique to demodulate received data. The injection-locked oscillator detects the input phase information and reacts on its output amplitude. In this receiver, the closed loop topology is not required for phase synchronization, which simplifies receiver design and reduce power consumption. This work is fabricated in TSMC 0.18-μm CMOS technology. The total power consumption is 0.97 mW with the sensitivity is -45 dBm at 10-Mbps data rate. The equivalent energy efficiency is 97 pJ/b.

The injection-locked technique is adopted in the transmitter design to modulate date. The injection locked oscillator will re-lock to a new phase when the phase changes at low frequency carrier. High frequency multi-phase oscillator is not required in this architecture; therefore it will reduce total power consumption significantly. This work is simulated under TSMC 0.18-μm CMOS technology. The total simulated power consumption is 0.297 mW with 13% EVM at 10-Mbps data rate. The maximum output power is -9.7 dBm, and the energy efficiency is 29.7 pJ/b.

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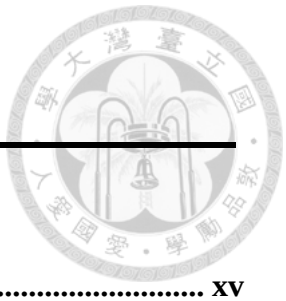

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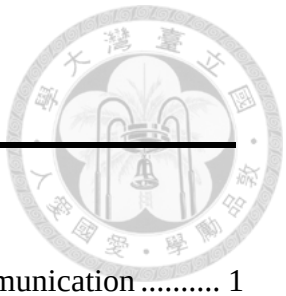

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Chapter 1 Introduction

1.1 Motivation

As the information and communication technology improve, the connection between people and the world become more flourishing than before. In consideration of security and health, the traditional devices such as cell phone with camera and long-distance transmission are forbidden in many places. Therefore, the IoT applications with short-distance communication are required in many fields. Fig. 1-1 shows the scenario of wearable mobile media for IoT application. This application composes of several biomedical sensor nodes to capture biomedical data and transmits it to nearby AP node by short-range wireless transmitter. A short-range wireless receiver is also required for wearable device to obtain information outside from AP node.

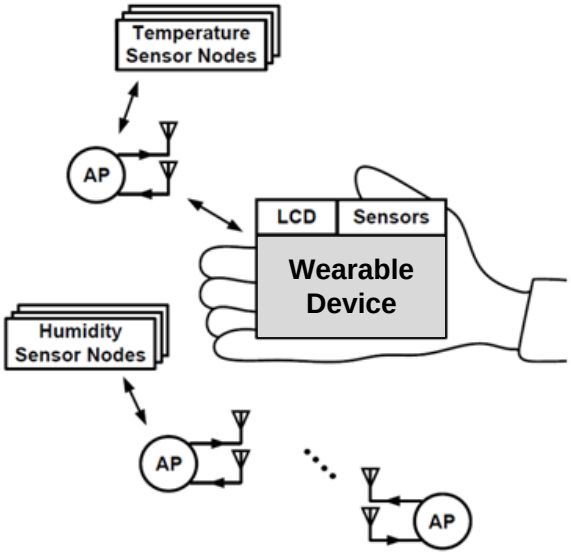

Fig. 1-1 Scenario of Wearable Mobile Device with Short-range Communication

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Since the wearable device is a mobile product, the long-time usability are significant important. In wireless wearable device, the power source for the whole system is energy harvesting circuits. Therefore, low power consumption is one of the major design concerns in the system. To integrate the whole system in low voltage is needed. On the other hand, the wearable device transmits and receives information though only several meters distance, so the specification of output power for transmitter and sensitivity for receiver are much relaxed.

1.2 Data-rate Requirement

The sufficient data rate is required for the transceiver. In consideration of transmitter, it's required to transmit biomedical information to AP node. As expressed in (1-1), data rate not only depends on the number of recording sensor (N_{sensor}) in wearable device, but also relies on the resolution of ADC (N_{bit}), and the sampling rate of ADC ($f_{sampling}$). Take an 1-lead electrocardiography (ECG) recording system which is integrated in wearable device node for example, and assume that a 10-bit ADC with 10-kHz sampling frequency is adopted. The uncompressed data rate will be 1×10k× 10=100 kbps. Nevertheless, if the transmitter is designed for more complex bio-signal recording such as 128-channel electroencephalography (EEG) monitoring, the required data rate could be up to 12.8 Mbps [1].

$$Data\ \ rate = N_{sensor} \times f_{sampling} \times N_{bit} \tag{1-1}$$

In view of several sensors in AP nodes, the wearable device node must receive huge information. In other word, the receiver in wearable device also requires high data rate specification as that of transmitter.

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1.3 Operation Frequency Band

Federal communications commission (FCC) established the Medical Implant Communication Service (MICS) and set aside 401 – 406 MHz spectrum. However either 100-kHz or 300-kHz channels is not sufficient for much sophisticate applications. Therefore FFC combined the 413-MHz to 457-MHz MHz band with the previous MICS band as the new Medical device Radio-communications Service (MedRadio) spectrum in 2011 [2]. The illustration of the spectrum allocation is shown in Fig. 1-2.

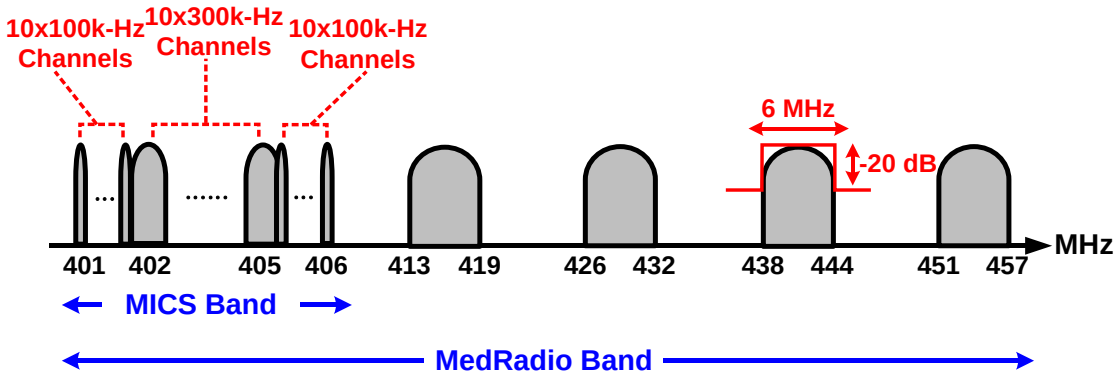

Fig. 1-2 MedRadio Band from 401 MHz to 457 MHz

MedRadio band is suitable for wearable application because of sufficient and the license is not required. Several symmetric transceivers aiming at MedRadio band have been published [1][3], achieving low-power performance but not operating efficiently.

1.4 Modulation Scheme

On-off keying (OOK) modulation is the special case of amplitude-shift keying (ASK), which is widely chosen for low-power systems due to the simplicity of circuit implementation [4]-[8]. Nevertheless, OOK modulation is susceptible to interference and the bandwidth efficiency is poor than that of phase-shift keying (PSK) or frequency shift keying (FSK). Therefore OOK is not suitable for wearable application due to its poor noise performance than that of FSK/PSK. Fig. 1-3 depicts the

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theoretical noise performance of the coherent FSK, non-coherent FSK, binary phase-shift keying (BPSK) and differential phase-shift keying (DPSK). Overall, the noise performance of PSK is superior to that of FSK. Hence it is easier to achieve energy-efficient transceiver with better sensitivity of receiver by implementing PSK modulation.

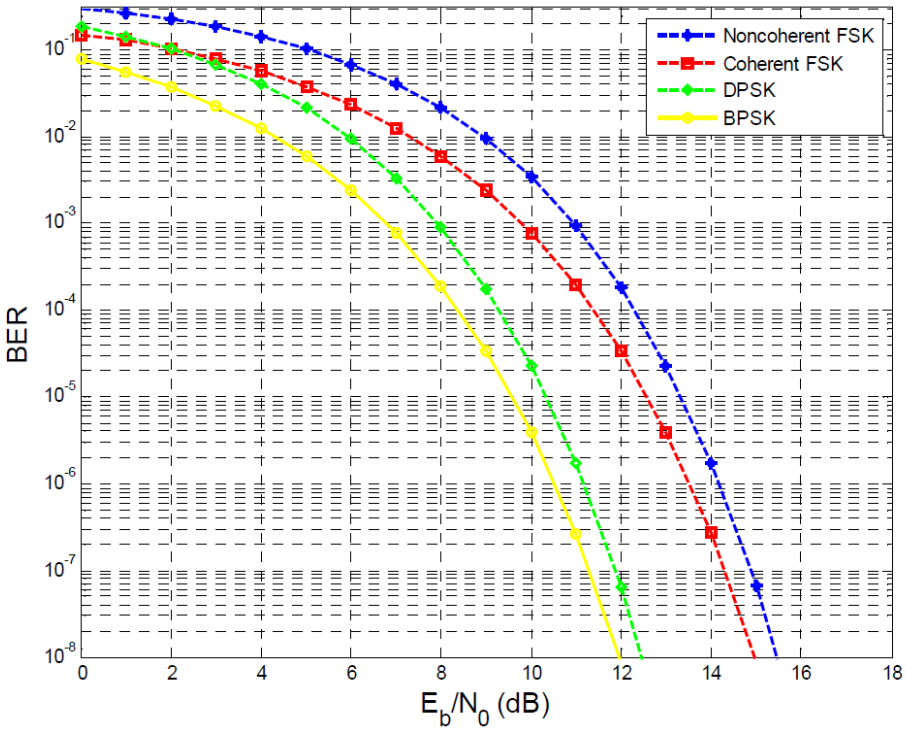

Fig. 1-3 BER versus Eb/No Graph

In low-power systems, the non-coherent demodulation such as DPSK demodulation is desirable because the phase-tracking loop is no longer needed for phase synchronization, which reduces power consumption [9]. Although the required SNR for demodulating non-coherent PSK carrier is higher than that of synchronized PSK demodulation, DPSK is an acceptable modulation based on simplified circuit architecture for low power specification.

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Differential phase shift keying such as D-BPSK is to deliver data by adding a relative phase change to the carrier signal rather than encode absolute phase for each baseband data. As shown in (1-2) and (1-3), extra 180° phase may be added to the current phase for transmitting a binary '1', and no extra phase change in carrier when transmitting a binary '0'.

$$s_0(t) = \begin{cases} A\cos(2\pi f_C t) \ , \ 0 \le t \le T \\ A\cos(2\pi f_C t) \ , \ T \le t \le 2T \end{cases} \ , \quad \textit{for binary } 0 \tag{1-2}$$

$$s_1(t) = \begin{cases} A\cos(2\pi f_C t) \ , \ 0 \le t \le T \\ A\cos(2\pi f_C t + \pi) \ , \ T \le t \le 2T \end{cases} \ , \quad \textit{for binary } 1 \tag{1-3}$$

In other word, the absolute phase information is no longer important compared with traditional phase modulation, which relaxes the circuit design requirement for transceiver. The implementation of differential encoder and decoder of D-BPSK is shown in Fig. 1-4.

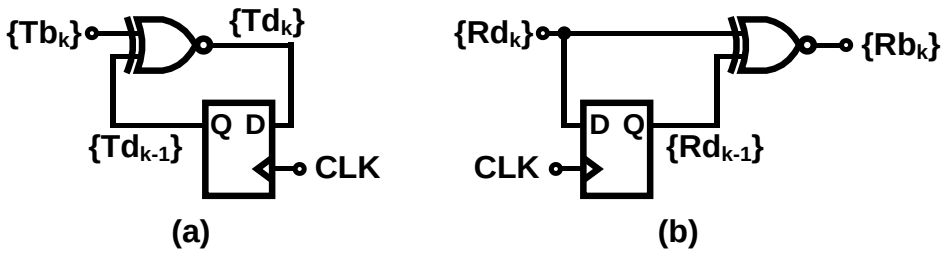

Fig. 1-4 Circuit implementation of (a) differential encoder (b) differential decoder

The differential encoding scheme is shown in Table 1-1. $\{Tb_k\}$ denotes the original data sequence for transmitting, $\{Td_k\}$ represents the encoded data sequence, and $\{\theta_k\}$ stands for the phase change of $\{Td_k\}$. The definition of $\{Td_k\}$is in (1-4).

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$$Td_k = \begin{cases} Td_{k-1}, & if \ \ Tb_k = 0 \\ \sim Td_{k-1}, & if \ \ Tb_k = 1 \end{cases} \quad (1\text{-}4)$$

Table 1-1 Illustration of differential encoding and decoding of BPSK

$\{Tb_k\}$	1	0	1	1	0	1	1	
$\{Td_{k-1}\}$	0	1	1	0	1	1	0	1
$\{Td_k\}$	1	1	0	1	1	0	1	
$\{\theta_k\}$	π	0	π	π	0	π	π	

1.5 Link Budget

The RF link budget has to be estimated in order to decide the specification of TRX front-end circuit [9]. The path loss due to signal propagation can be estimated by free-space loss equation shown in (1-5).

$$L_{path} = 20\log\left(\frac{4\pi d}{\lambda}\right) \quad (1\text{-}5)$$

λ is the wave-length, and d is the distance between the wearable device and AP node. If the operating frequency is 400 MHz and the distance is 5 meters, the path loss is about 38 dB.

$$P_{recieved} = P_{out} + G_{antenna} - L_{path} \quad (1\text{-}6)$$

In (1-6), P_{out} is the TX output power, and $G_{antenna}$ is the antenna gain of TX/RX. To meet the standard of Med-radio band, the TX output power is -10 dBm. Assume a

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chip antenna with -10-dBi antenna gain is adopted; as a result, for 5-meter distance, the received power is about -58dBm.

From the above calculation, the RX sensitivity, which is defined as detectable signal power for a certain BER of demodulated data [10][11] is -60 dBm.

1.6 Thesis Overview

This thesis presents the design of low voltage D-BPSK transceiver, including theoretical analysis, simulated and measured results.

Chapter 2 introduces the state-of-the-art low-power transceivers for WBAN applications, which covers traditional wireless transceivers and injection-locked-based transceivers.

Chapter 3 presents the proposed ultra-low-voltage D-BPSK receiver based on injection-locked technique, which includes the dynamic phase-to-amplitude conversion analysis.

Chapter 4 describes the proposed ultra-low-voltage D-BPSK transmitter. The theory of sub-harmonic injection-locked phase modulation for low-power consideration is also presented.

Finally, chapter 5 provides a conclusion and the future work.

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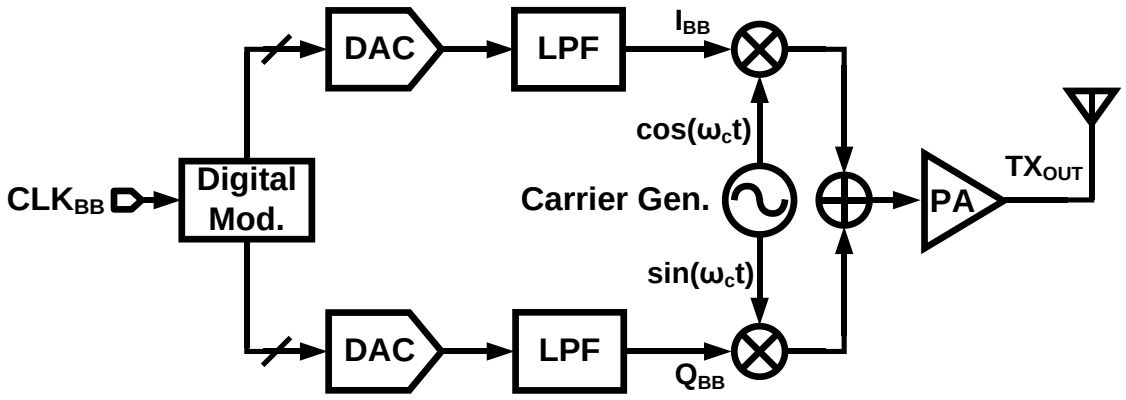
Chapter 2 Introduction to Low-Power Wireless Transceiver

2.1 General Architecture of Wireless Transceiver

Mixer-based transmitters are widely applied in many wireless systems [12]-[14]. As shown in Fig. 2-1, there are two common mixer-based architectures. The direct-conversion transmitter uses digital-to-analog converter (DAC) and mixers for transforming baseband data to analog format and performing up-conversion task. However, this topology suffers from injection pulling effect between power amplifier and carrier, so another type which adopts heterodyne topology for separating carrier frequency from the PA output spectrum by making the signal up-conversion in two steps had become popular. Nonetheless, these two topologies must deal with the trade-off between maximum data rate which is limited by the bandwidth of DAC and power consumption. Therefore, mixer-based transmitters are not appropriate choices for low-power applications.



(a)

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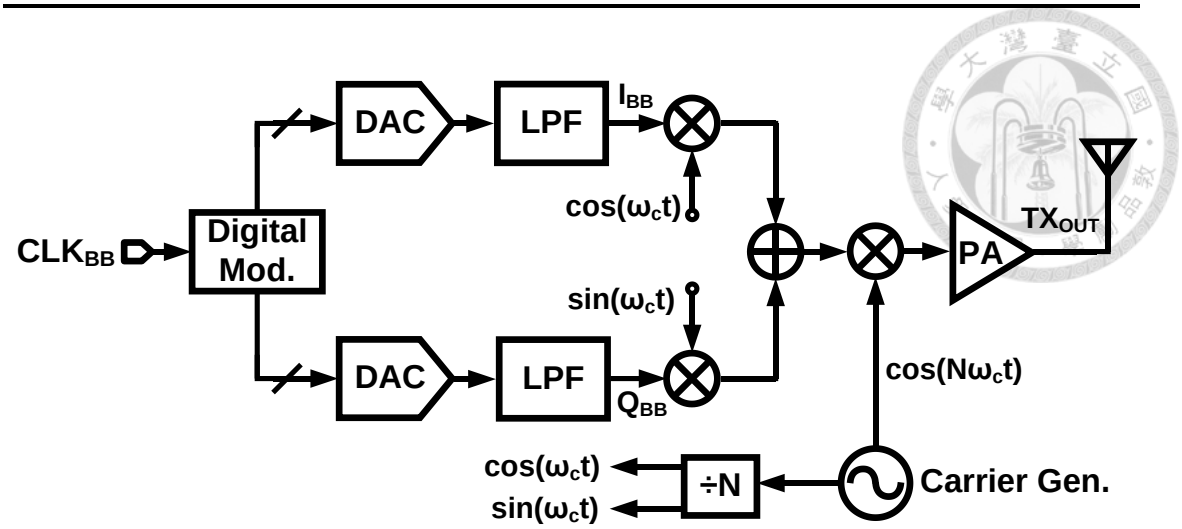

(b)

Fig. 2-1 Mixer-based Transmitter (a) Direct-conversion Transmitter [12] (b) Heterodyne Transmitter [13]

The PLL-based in-loop-modulation transmitter [15] is another common transmitter architecture. As depicted in Fig. 2-2, the digital data which is encoded by the digital baseband modulates the frequency divider to accomplish FSK modulation. This modulation requires phase-locked loop (PLL), which results in much higher power consumption. In addition, the limited data rate is the primary disadvantage due to the bandwidth of PLL. To sum up, the PLL-based topology is more suitable for narrow-band applications rather than high-energy-efficient ones.

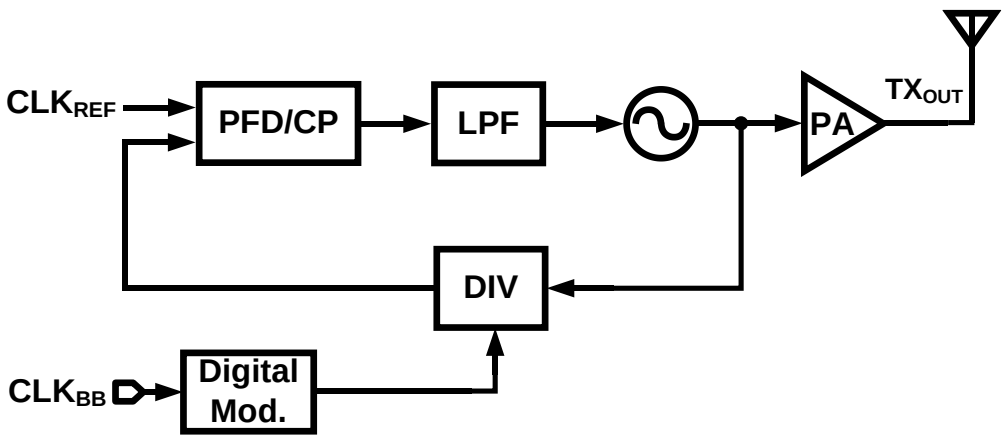

Fig. 2-2 PLL-based In-Loop-Modulation Transmitter

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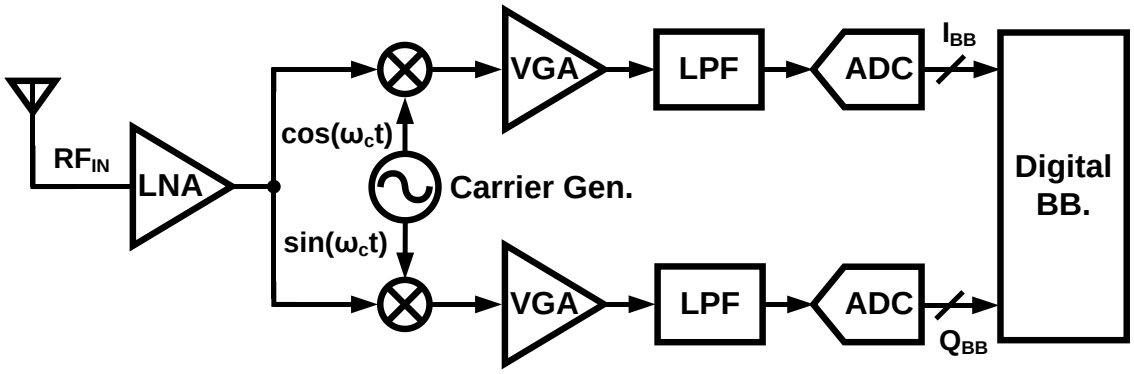
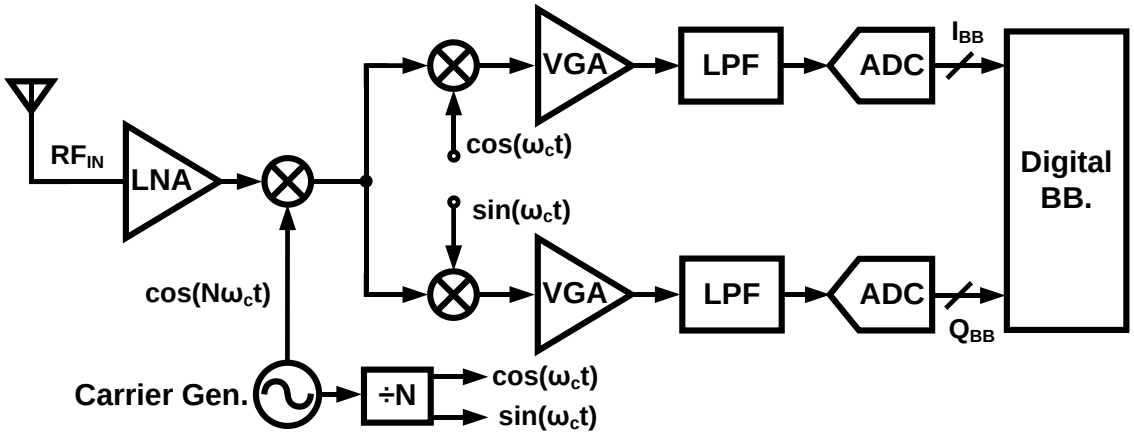
The direct-conversion receiver and heterodyne receiver shown in Fig. 2-3 play important parts in wireless communication. The former one solves the out-band interference problem and save intermediate frequency (IF) filter, but the carrier operating at higher frequency is needed in this receiver, which tightens total power budget. The latter one provides the two-step down-conversion facilitate. However, the non-zero IF down-conversion causes the image problem. Although these architectures are commonly used for different specification, power-hungry circuits such as ADCs and mixers are needed, which is the limitation for low-power system.



(a)



(b)

Fig. 2-3 Mixer-based Receiver (a) Direct-conversion Receiver [12] (b) Heterodyne Receiver [14]

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2.2 Low-Power Wireless Receiver

2.2.1 Super-Regenerative Receiver (SR RX)

The signal-regeneration characteristic of super-regenerative receiver (SR RX) is suitable for demodulating OOK and FSK signal while consumes little power [7][16][17]. Fig. 2-4 shows the basic operation of SR RX. The RF carrier which is amplified by LNA injects to a periodically quenched oscillator. Then, the envelope detector (ED) detects input-dependent envelope of oscillator whose output pulse width contains the data information.

The periodically quenched oscillator operate with heavy duty-cycled and RX only requires simple mechanism to demodulate data, which makes SR RX be a famous solution for low-power application. However, the worse frequency selectivity and the requirement of high-Q passive components limit the development of the SR RX.

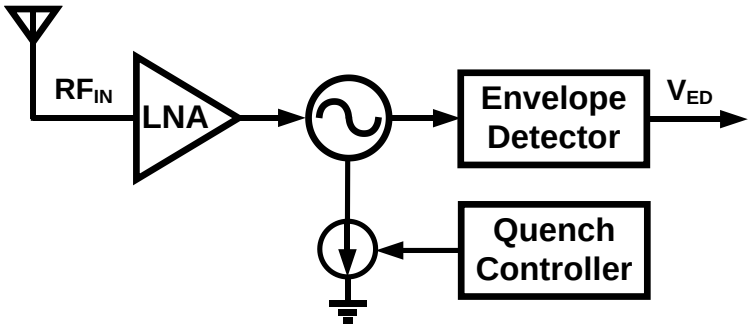

Fig. 2-4 Super-Regenerative Receiver

2.2.2 Injection-Locked-Based Receiver

Injection-locking phenomenon in an oscillator is commonly used for providing frequency division or LO generation. Moreover, the low-power receivers based on the

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injection-locked technique develops rapidly in recent years. Fig. 2-5 shows the block diagram and operation mechanism of the injection-locked BFSK receiver architecture [18]. The key point of the FSK demodulation capability is the frequency selectivity of the ILO. The ILO acts as a band-pass filter and it transforms frequency difference between RF data into amplitude difference. The envelope detector captures and recovers input-dependent amplitude information. The major drawback is the small amplitude difference (~2mV) converted from frequency difference, which implies wider frequency deviation, hence more bandwidth is needed. Therefore, injection-locked based FSK receiver suffers from poor bandwidth-efficient performance.

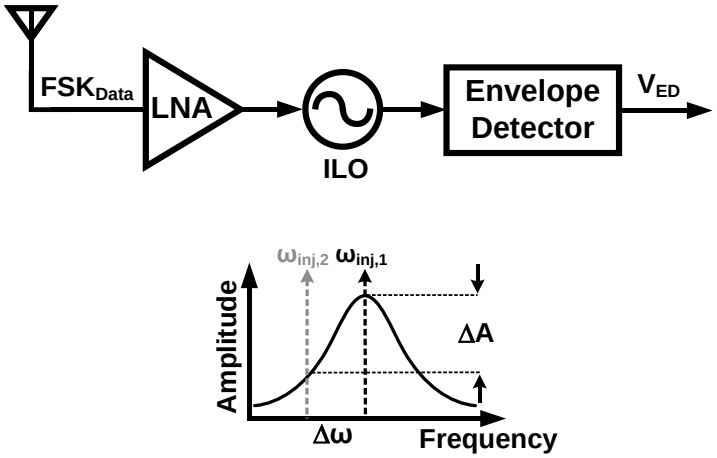

Fig. 2-5 Injection-Locked BFSK Receiver

The synchronization between receiver and transmitter is needed for PSK demodulation in traditional receiver. Non-linear BPSK demodulation schemes using injection-locking technique were proposed [19][20] recently, which consists of two super-harmonic injection-locked oscillators (SH-ILO) and an XOR gate as shown in Fig. 2-6. The principle of non-linear BPSK demodulator depends on the dynamics of two super-harmonic injection-locked oscillators. The BPSK modulated signal is injected to the two oscillators, which makes one of the oscillators obtain a phase lead, the other

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obtain a phase lag. Then an XOR operation combines the oscillator output. The circuit is well-suited to achieve low-power consumption as a result of simplified architecture and the oscillator running at one-half the input signal frequency.

When a BPSK modulated input signal is fed to the 2nd harmonic injection-locked oscillators, its output frequency is one-half of input frequency. If the oscillator is locked with no phase change, the phases of two injection-locked oscillators are the same, which makes the output of XOR produce 0. On the other hand, an 180° phase change of the BPSK modulated input signal leads to ±90° output phase (Δθ) change of the SH-ILOs as shown in (2-1).

$$\Delta\theta = \begin{cases} +90^{\circ}, \omega_{osc1} > \dfrac{\omega_{inj}}{2} = \omega_{in} \\ -90^{\circ}, \omega_{osc2} < \dfrac{\omega_{inj}}{2} = \omega_{in} \end{cases} \tag{2-1}$$

180° phase shift in the input signal results in 90° phase lag at the output of ILO_1 if $\omega_{osc1} < \omega_{in}$ and 90° phase lead at the output of ILO_2 if $\omega_{osc2} > \omega_{in}$. In short word, a total phase difference is 180° between ILO_1 and ILO_2, which makes output of XOR produce 1.

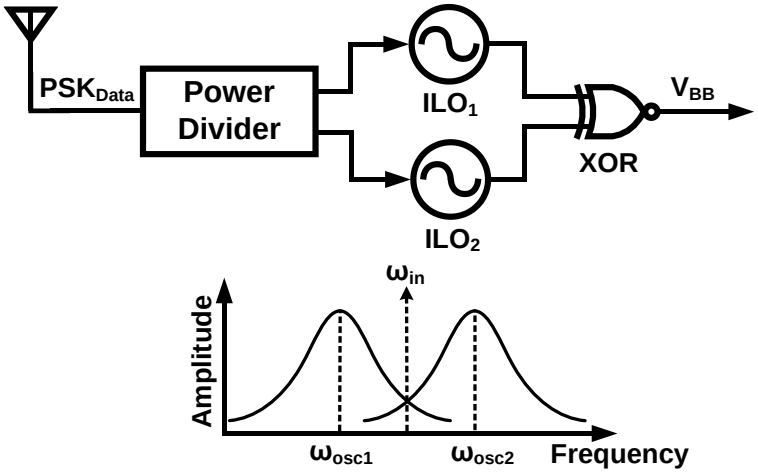

Fig. 2-6 Block diagram of the BPSK Demodulator/Receiver

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To prevent the pulling effect between two oscillators, the frequency separation between ILOs must be far enough, so that the required gain of RF front-end circuit must increase for larger injection power. Therefore, this type of receiver needs excess power for RF front-end circuit due to gain requirement. Furthermore, a tradeoff between frequency difference and data rate is significant. The pulling effect becomes severe if frequency difference decreases for data-rate requirement at fixed injection power. To sum up, this architecture is ill-suited to low-power applications at sub-GHz range.

2.3 Low-Power Wireless Transmitter

2.3.1 OOK Transmitter

The OOK transmitters are widely adopted in many low power systems [4]-[8]. The traditional implementation is to switch PA or carrier directly, which simplifies circuit architecture and relaxes system power budget. An injection-locked OOK transmitter was published to achieve higher energy efficiency, as briefly depicted in Fig. 2-8. However, the innate limit such as insufficient bandwidth efficiency burdens the usability of OOK transmitter for low-power and high-data-rate applications.

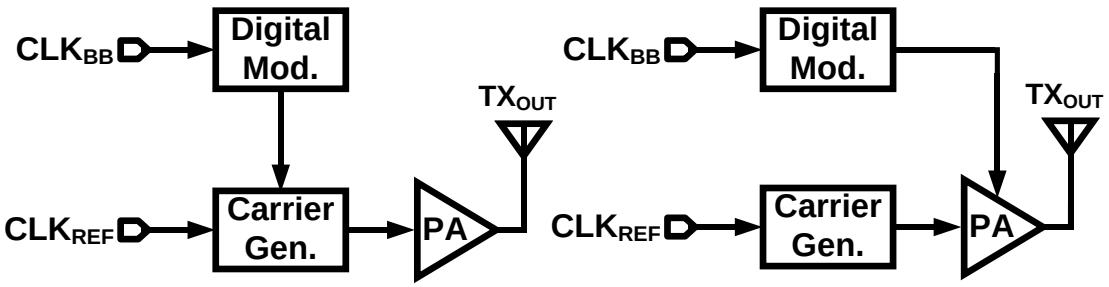

Fig. 2-7 System Architecture of OOK Transmitter

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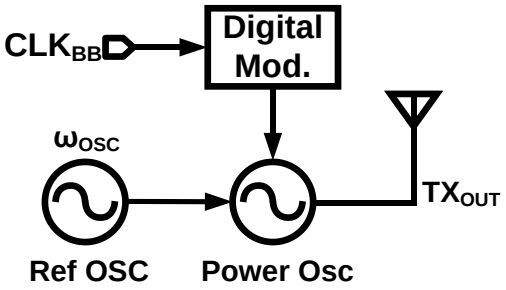

Fig. 2-8 Injection-Locked OOK Transmitter [4]

2.3.2 Phase-MUX-Based Transmitter

Phase-multiplexing (Phase-MUX) technique is greatly preferred in low-power PSK transmitter design recently [1]. The frequency carrier produces multi-phase information and is followed by a multiplexer. The encoded digital control signal modulates the multiplexer to switch the phase of carrier for accomplishing PSK modulation. This technique relaxes the trade-off between power and bandwidth, eliminating the power-hungry block such as mixer, LPF, and DAC. Nevertheless, the multi-phase carrier generators which operate at high frequency become the most power-hungry block in transmitter. Therefore, Phase-MUX based transmitter is an improper alternative for ultra-low-power applications.

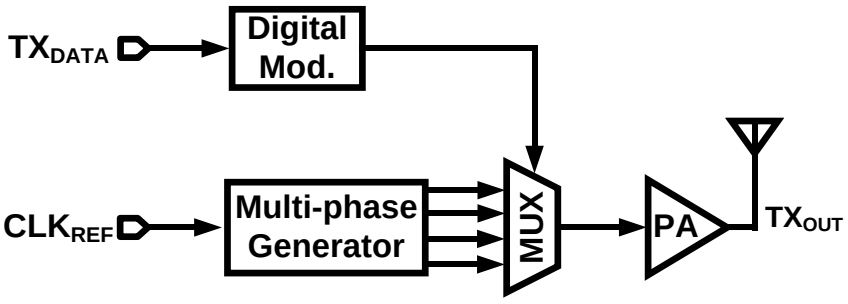

Fig. 2-9 Phase-MUX-Based Transmitter

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2.3.3 Injection-Locked Transmitter with Edge-Combining Technique

Injection-locked transmitter with edge-combining technique has been proposed to low-power FSK/PSK transmitters [7][21][22]. The injection-locked transmitter behaves as a first-order PLL, which the free-run frequency of oscillator could be locked to the n^{th} harmonic of the injection reference frequency [23]. Without any extra power-hungry part such as high-frequency divider, phase frequency detector (PFD), and charge pump (CP), so injection-locked oscillator (ILO) is energy-efficient circuit block to reduce power consumption.

Fig. 2-10 shows the system architecture of a low-power BFSK injection-locked transmitter for MICS/ISM band [21]. This transmitter achieves low-power performance through edge-combing technique. The edge combiner (EC) mixes low-frequency multi-phase signal to generate signals at RF frequency. Therefore, the power consumption is much less than the one of Phase-MUX based transmitter because most circuit block including multi-phase carrier operate at low frequency. Although this transmitter relaxes power budget, the FSK modulation suffer from poor spectrum efficiency comparing with that of PSK modulation.

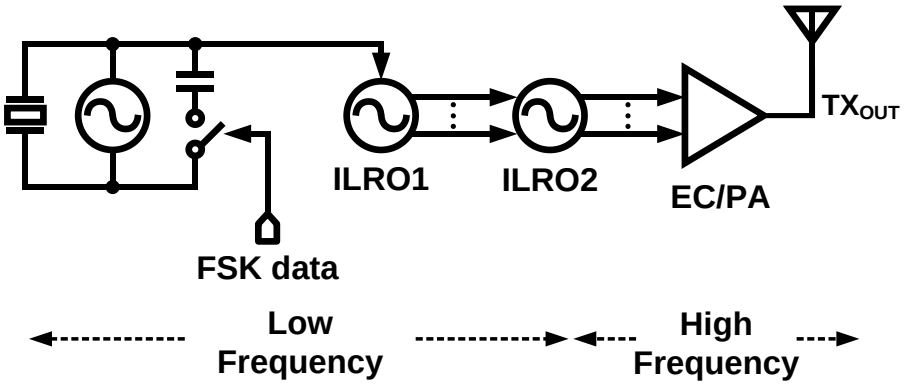

Fig. 2-10 Injection-Locked BFSK Transmitter with Edge-combining Technique

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In [22], a low-power BPSK injection-locked transmitter was presented for both low-power and excellent spectrum efficiency performance. It merges the advantage of phase multiplexer and edge-combining techniques as shown in Fig. 2-11. However there're several issues in this design. First, the number of combining path depends on the ratio between injected frequency and RF frequency. Even in simple phase modulation such as BPSK, it will require multi-path circuit due to the frequency difference between injected signal and RF carrier, which complicates the design. Furthermore, the spurs due to the phase mismatch of edge combiner will degrade spectrum performance. The phase calibration technique is needed to address this issue.

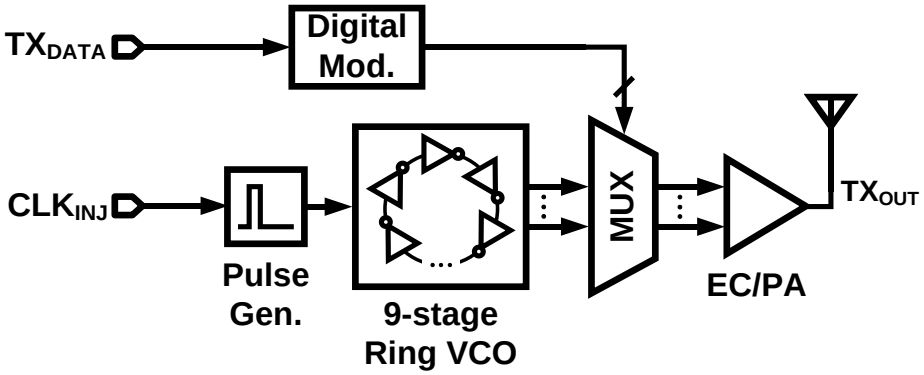

Fig. 2-11 Injection-Locked BPSK Transmitter with Edge-combining Technique

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Chapter 3 Proposed Low-Power Injection-Locked D-BPSK Receiver

3.1 Receiver Introduction

3.1.1 Injection-Locked LC Oscillator Theory

Injection-locked LC oscillator is commonly used for many low-power receivers [18]-[20]. The related theories about LC oscillator under injection were published in [24][25].

An injection-locking or pulling phenomenon occurs when a periodic signal feeds to an oscillator. If injection-locked frequency ω_{inj} is close to the free-running frequency ω_o, the output frequency will be locked to ω_{inj} and the current output I_t will be combined with input current I_{inj} and free-running current I_{osc} as shown in Fig 3-1.

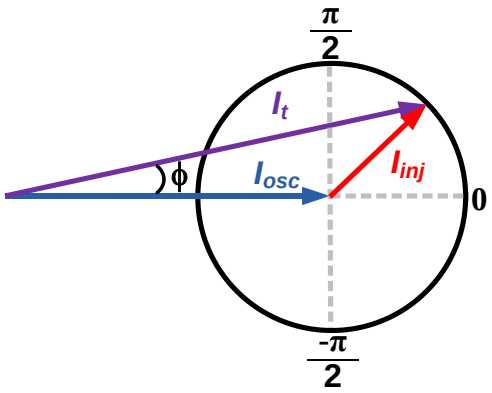

Fig. 3-1 Phasor diagram illustrating the phase difference between input signal and output signal in steady state (ϕ is the steady state phase difference between I_{osc} and I_t)

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The conceptual block diagram of an LC oscillator under injection is shown in Fig. 3-2, where the incoming voltage-domain signal (V_{inj}) is first converted to current domain signal (I_{inj}) by a transconductance stage, and then added with oscillator current (I_{osc}). The resultant current (I_t) is injected to a resonator whose central frequency is ω_o and converted back to voltage (V_{osc}) domain. The equations describing the injection-locking phenomenon under these conditions are derived in (3-1)-(3-9).

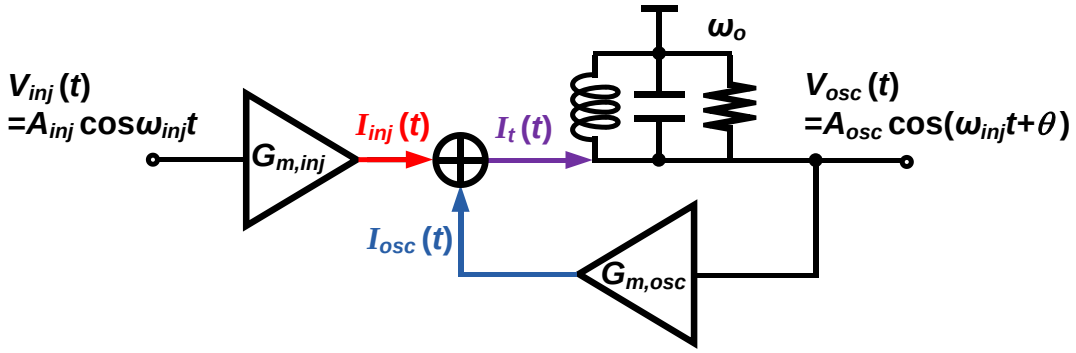

Fig. 3-2 Simplified circuit diagram of LC oscillator under injection

$$\begin{aligned} I_t(t) &= I_{inj}(t) + I_{osc}(t) = I_{Amp}cos(\omega_{inj} + \phi) \\ &= G_{m,inj}V_{inj}(t) + G_{m,osc}V_{osc}(t) \\ &= G_{m,inj}A_{inj}cos\omega_{inj}t + G_{m,osc}A_{osc}cos(\omega_{inj}t + \theta) \\ &= (G_{m,inj}A_{inj} + G_{m,osc}A_{osc}cos\theta)cos\omega_{inj}t \\ &\quad -(G_{m,osc}A_{osc}sin\theta)sin\omega_{inj}t \end{aligned} \tag{3-1}$$

From above equation, we can get the phase difference ϕ between I_t and I_{osc} is

$$Tan\phi = \frac{G_{m,osc}A_{osc}sin\theta}{G_{m,inj}A_{inj} + G_{m,osc}A_{osc}cos\theta} \tag{3-2}$$

I_t experiences a phase shift after passing through LC tank.

$$\begin{aligned} &V_{osc}(t) = V_{osc}cos(\omega_{inj} + \theta) \\ &\approx \left|Z(j\omega_{inj})\right| G_{m,osc}A_{osc}cos\left(\omega_{inj} + \phi + Tan^{-1}\left[\frac{2Q}{\omega_o}(\omega_o - \omega_{inj} - \frac{d\phi}{dt})\right]\right) \end{aligned} \tag{3-3}$$

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From (3-3), we observe the relationship between phase θ and phase ϕ with that

$$\theta = \phi + Tan^{-1}\left[\frac{2Q}{\omega_o}(\omega_o - \omega_{inj} - \frac{d\phi}{dt})\right] \tag{3-4}$$

The change rate of phase ϕ is close to that of phase θ.

$$\frac{d\phi}{dt} \approx \frac{d\theta}{dt} \tag{3-5}$$

Furthermore

$$\begin{aligned} Tan(\theta-\phi) &= \frac{G_{m,inj}A_{inj}sin\theta}{G_{m,osc}A_{osc}+G_{m,inj}A_{inj}cos\theta} = \frac{Ksin\theta}{1+Kcos\theta} \\ K &= \frac{G_{m,inj}A_{inj}}{G_{m,osc}A_{osc}} = \frac{I_{inj}}{I_{osc}} \end{aligned} \tag{3-6}$$

Under locked condition, the phase difference remain constant with time can derive the relationship between locking range ω_L and injection current ratio K from (3-4), (3-5), and (3-6).

$$\begin{aligned} \frac{d\theta(t)}{dt} &= \omega_o - \omega_{inj} - \frac{\omega_o}{2Q}Tan(\theta-\phi) \\ &= \omega_o - \omega_{inj} - \frac{\omega_o}{2Q}\frac{Ksin\theta}{1+Kcos\theta} = 0 \end{aligned} \tag{3-7}$$

Locking range is the difference between free-running frequency and injection frequency which can be computed as shown in (3-8).

$$\omega_o - \omega_{inj} = \frac{\omega_o}{2Q}\frac{Ksin\theta}{1+Kcos\theta} \tag{3-8}$$

The maximum locking range can be calculated by substituting θ [25], and we final get

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$$\omega_L = \omega_o - \omega_{injmax} = \frac{\omega_o}{2Q}\frac{K}{\sqrt{1-K^2}} \quad (3\text{-}9)$$

3.1.2 Injection-Locked Oscillator as Phase-to-Amplitude Converter

Envelope detection is widely applied in the non-coherent AM demodulation for its simplicity. The phase-to-amplitude conversion can be applied in order to demodulate the D-BPSK signal. Fig. 3-3 illustrates the operation of phase-to-amplitude conversion.

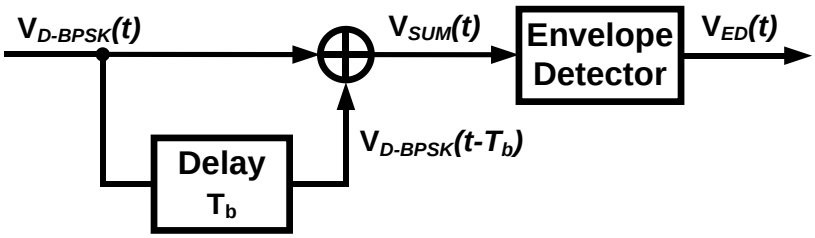

Fig. 3-3 Non-coherent DPSK detection using amplitude-to-phase conversion

This phase-to-amplitude conversion demodulates data by comparing the phase difference between received signal $V_{DPSK}(t)$ and former received signal $V_{DPSK}(t-T_b)$, where T_b is one-bit period.

Assume $V_{DPSK}(t)$ and $V_{DPSK}(t-T_b)$ are in-phase in initial status, the amplitude of $V_{SUM}(t)$ will increase due to the summation. On the other hand, the amplitude of $V_{SUM}(t)$ reduces due to the summation of two anti-phase signals $V_{DPSK}(t)$, $V_{DPSK}(t-T_b)$. Then the phase-to-amplitude information will be captured by envelope detector. Moreover, this method is not a proper choice for receiver at RF frequency, because an exact delay element is difficult to be accomplished without dramatically increasing power consumption.

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Instead a phase-to-amplitude conversion technique by using injection-locked oscillator is proposed in this work. Fig. 3-4 is a conceptual block diagram of phase-to-amplitude conversion by using an injection-locked LC oscillator. If the phase of input signal $I_{inj}(t)$ changes 180^{o}, the magnitude of $I_t(t)$ will decrease temporarily. The oscillator will return to the initial locked state after time duration. The behavior described above is a transient phenomenon. Therefore, the analysis of dynamic behavior of the ILO is needed.

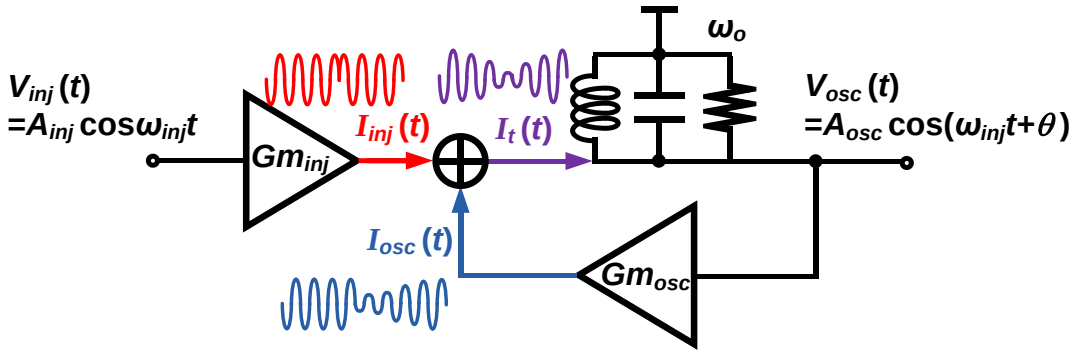

Fig. 3-4 Simplified circuit of Injection-locked LC oscillator as phase-to-amplitude converter

According to [26], the frequency settling behavior of an ILO is described by (3-10) and (3-11). θ_{SS} is the steady-state phase, and $\theta(0)$ is initial phase.

$$\frac{d\theta(t)}{dt} = \omega_o - \omega_{inj} - \omega_L sin(\theta(t)) \tag{3-10}$$

$$\omega_{osc}(t) = \omega_{osc} + \omega_L \{\theta_{SS} - \theta(0)\} e^{-\omega_L t} \tag{3-11}$$

The time constant is shown in equation (3-12).

$$\tau = \frac{1}{\omega_L} \tag{3-12}$$

Assume the locking time is approximately 4τ [26], and equation (3-12) shows that the locking range is inverse proportional to the locking time.

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The ILO converts relative phase information to amplitude variation depending on its transient behavior, that is to say, the ILO change state between the locked state and the state. Since the locking time is an important parameter on this receiver, and the detailed analysis such as relationship between locking time and circuit specification for receiver will be discussed in the following paragraphs.

3.2 System Architecture

3.2.1 The Proposed D-BPSK Receiver

The proposed architecture of the DPSK receiver, as shown in Fig. 3-5, is composed of a matching network, a low-noise amplifier (LNA), the multi-stage amplifier (Amp), a injection-locked oscillator (ILO), an envelope detector, and a data slicer.

LNA and the following multi-stage amplifier amplify the received D-BPSK signal (RF_{in}). Before injecting to the ILO, the amplified signal is converted from voltage domain to current domain by a transconductance stage. Therefore, the ILO performs dynamic phase-to-amplitude conversion, then the envelope detector extracts the amplitude information, and the received signal is therefore down-converted to baseband. Finally, data slicer recovers the analog signal to a digital output.

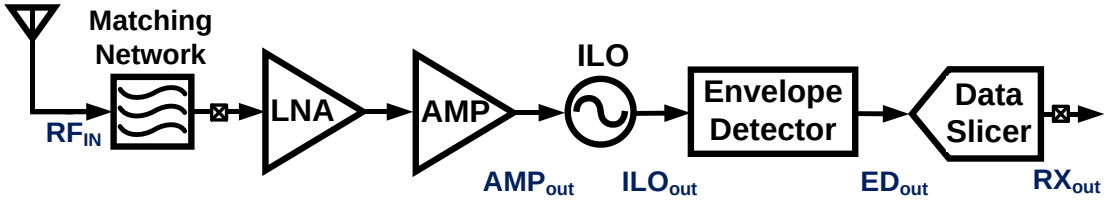

Fig. 3-5 Proposed DPSK Receiver with Phase-to-Amplitude Conversion

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3.2.2 Design Specifications of the Proposed Receiver

The sensitivity of RX is defined as detectable signal power for certain BER of demodulated data [11].

$$Sensitivity\,(\text{dBm}) = \text{N}_o + 10\log(B) + NF + SNR_{min} \tag{3-13}$$

N_0 is thermal-noise power in 1-Hz noise bandwidth, B is equivalent noise bandwidth, NF is noise figure of RX front-end circuit, and SNR_{min} is the minimal SNR required for DPSK demodulation. According to BER-to-SNR graph shown in Fig. 1-3, the minimal SNR of DSPK demodulation for 10^{-3} (0.1 %) BER is around 7 dB. Assume the sensitivity is equal to the received power calculated in Chapter 1.6, and the equivalent noise bandwidth is 10 MHz for high-data-rate application, we can determine the NF of front-end circuit is about 23 dB, which isn't a tight specification for receiver.

Another critical requirement is the front-end gain which affects the specification of maximal data rate for receiver. As mentioned in Chapter 3.1.1, demodulation is based on the transient characteristic of the ILO, so the locking time (4τ) must be less than data-transmitted time for successful demodulation..

$$T_S = 4\tau = \frac{4}{\omega_L} < T_b \tag{3-14}$$

Chapter 1.2 determines the maximum data rate requirement is 10 Mbps, in other word, the bit interval is 100ns. According to (3-14), the locking range ω_L of ILO must be larger than 2π*6.366 MHz. Chapter 3.1.1 analyzes the relationship between locking range and injection power ratio K. Substituting the design parameter ωo=405 MHz and Q is 7.6 into (3-9), the required injection ratio K can be estimated, which is about 0.83.

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The injection power ratio is determined by front-end gain A_{RF}, oscillator current I_{OSC}, and input signal V_{in} as depicted in (3-15).

$$K = \frac{I_{inj}}{I_{osc}} = \frac{V_{\text{in}} A_{RF} G_{m,inj}}{I_{osc}} \tag{3-15}$$

V_{in}=316 μV (-60 dBm) which is equal to the sensitivity, and assume the transconductance G_m=2 mA/V, I_{OSC} = 400 μA, the requirement of front-end gain is 151 (43dB).

To sum up, due to the injection-locking characteristic of LC-tank oscillator for dynamic phase-to-amplitude conversion, the requirement of maximal data rate determines the locking range and the front-end gain. Above analysis provides insights into the design of RX system. The specification of this work is shown in Table3-1 in the end.

Table 3-1 Designing Specifications of D-BPSK Receiver

Process	TSMC 0.18-μm CMOS
Supply Voltage	0.5 V
Operating Frequency	414 ~ 457 MHz
Data Rate	10 Mbps
Sensitivity	< -60 dBm
Modulation	D-BPSK
Power Consumption	< 0.5 mW
Energy Efficiency	< 50 pJ/b

doi:10.6342/NTU201602538

3.3 Circuit Implementation

3.3.1 Low Noise Amplifier and Multi-Stage Amplifier

LNA adopts the cascode common-source topology with Q-enhancement technique for increasing gain in ultra-low voltage design without consuming excess power as shown in Fig. 3-6. The C_S and L_G are off-chip element for an input matching network. Moreover, the input terminal of LNA is connected with ESD protection, which consists of 2 reverse-biased diodes. The source degeneration inductor is implemented by the bonding wire to save the area.

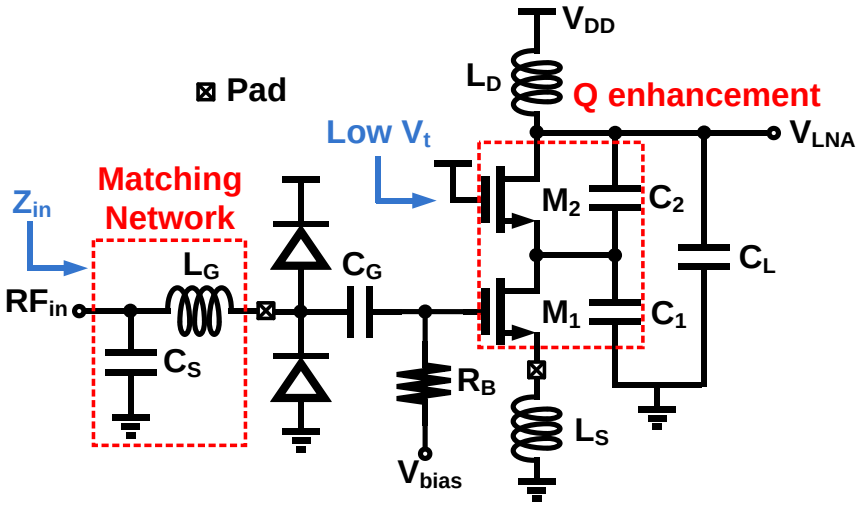

Fig. 3-6 Schematic of the Low-Noise Amplifier

The input impedance with matching network can be expressed as equation (3-16), where C_{GS} is the parasitic capacitance between gate terminal and source terminal.

$$Z_{in} = \frac{1}{1+s^2 L_G C_S}\left[\frac{g_{m1}L_s}{C_{GS1}} + s(L_s + L_G) + \frac{1}{sC_{GS1}}\right] \quad (3\text{-}16)$$

The additional off-chip matching network L_G and C_S makes input impedance matched to 50-Ω with practical values. Assume that L_s = 1 nH, C_{GS} = 100 fF and

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resonant frequency = 435 MHz, the values of L_G is 100 nH and C_S is about 20 pF by the simulation of smith chart.

Q-enhancement technique is adopted by using colpitts structure which forms positive feedback path for canceling the parasitic loss R_s of inductor L_D. The related formula is expressed in (3-17) and (3-18). This technique also affects the resonant frequency ω_o, so a large C_L is added for determining ω_o. To avoid an unstable LNA, the negative resistance R_N must be slightly smaller than R_s. Therefore, a high gain LNA with 15-dB voltage gain in ultra-low voltage environment is implemented. The final value of C_{GS} = 1 pF and C_{GS} = 1 pF with L_D = 40 nH and C_L = 1.5 pF.

$$R_N = -\frac{g_{m1}}{\omega^2 C_1 C_2} \approx R_S \tag{3-17}$$

$$\omega_o = \frac{1}{\sqrt{L_D\left(\frac{C_1 C_2}{C_1 + C_2} + C_L\right)}} \tag{3-18}$$

The multi-stage amplifier follows the LNA to provide additional gain for meeting the requirement analyzed in Chapter 3.2.2. The architecture composes of 3 cascade common-source amplifier. Each stage provides 15-dB voltage gain.

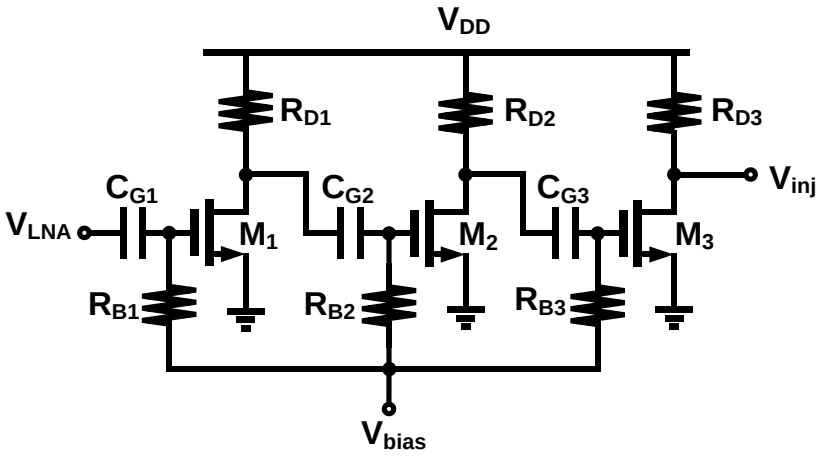

Fig. 3-7 Schematic of the Multi-Stage Amplifier

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The simulated S11 of LNA is shown in Fig. 3-8, which is around -14 ~ -33 dB under different corners. The central-frequency drift is solved by adjusting digital code of ILO. Fig. 3-9 shows overall voltage gain of front-end amplifier. The results under TT 27°, FF 0°, SS 80° are 58 dB, 64 dB, 43 dB, respectively.

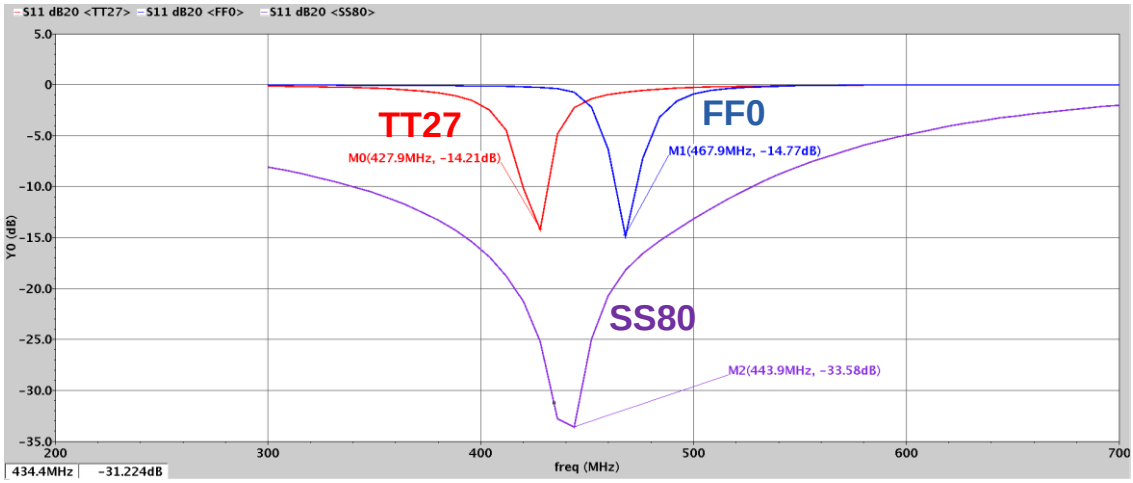

Fig. 3-8 Simulated S11 of LNA

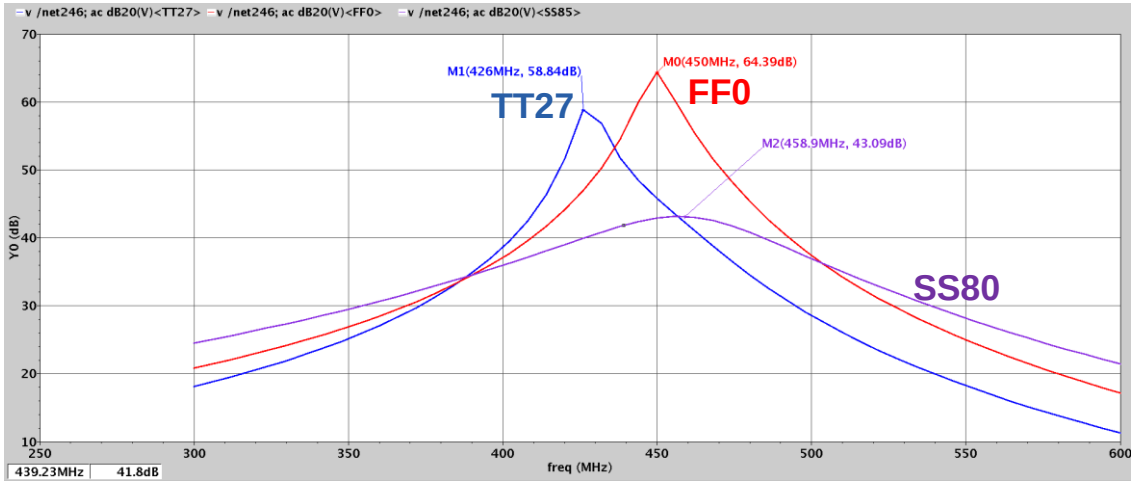

Fig. 3-9 Simulated overall voltage gain

The simulated noise figure of total amplifier which consists of LNA and AMP is shown in Fig. 3-10. The value is around 7 ~ 25 dB under different corners from 414 MHz to 457 MHz.

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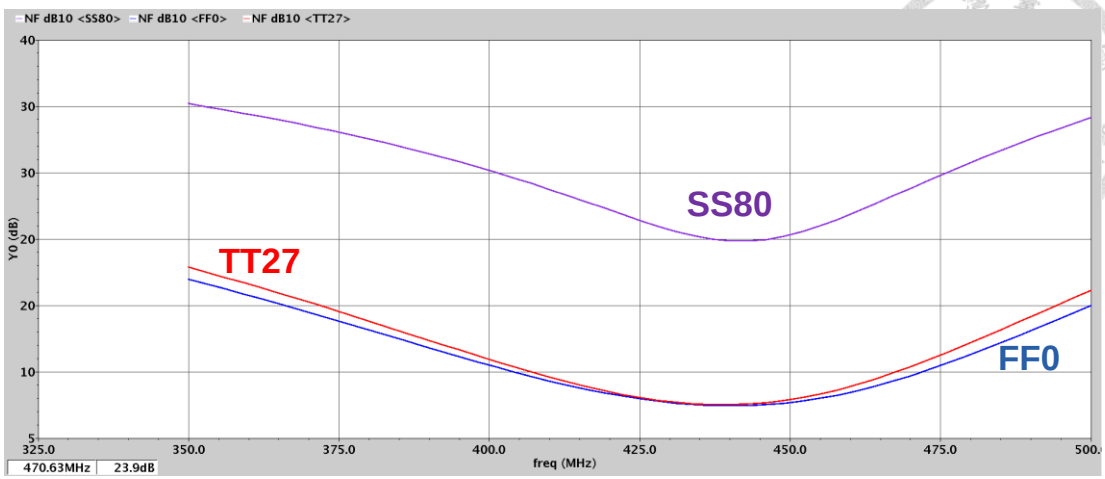

Fig. 3-10 Simulated overall noise figure

Table 3-2 Simulated characteristics of LNA and AMP @ TT27 °

Item	Value
Supply Voltage	0.5 V
Total Current	450 μA
Input Return Loss	-10 dB
Voltage Gain	46 dB
Noise figure	10 dB

3.3.2 Injection-Locked Dual-Conduction Oscillator

The schematic of injection-locked oscillator, composed of a digitally-controlled oscillator (DCO) and a G_m stage, is shown in Fig. 3-11. ILO adopts dual-conduction PN-complimentary LC-tank topology [27]. One main pair is used for sustaining class-C operation, while the other is an auxiliary pair with an added resistor R_S for minimizing total current consumption after overcoming start-up condition. A 4-bit programmable capacitor array with varactor is incorporated to compensate for the center frequency deviation due to PVT variations. The G_m stage (M_7, M_8) is designed to convert the input voltage signal to current format for injecting the oscillator. Due to the

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low-voltage operation (0.5 V), the replica-biasing circuit is used to provide a stable bias point. The transistor size and biasing condition is listed in Table 3-3.

Table 3-3 Transistor size and operating point of the G_m stage under corner TT27°

Device	W/L (μm/μm)	Current (μA)	g_m (μS)	g_o (μS)
$M_{1,2}$	20/0.18	118	1900	36.6
$M_{3,4}$	20/0.18	118	1900	36.6

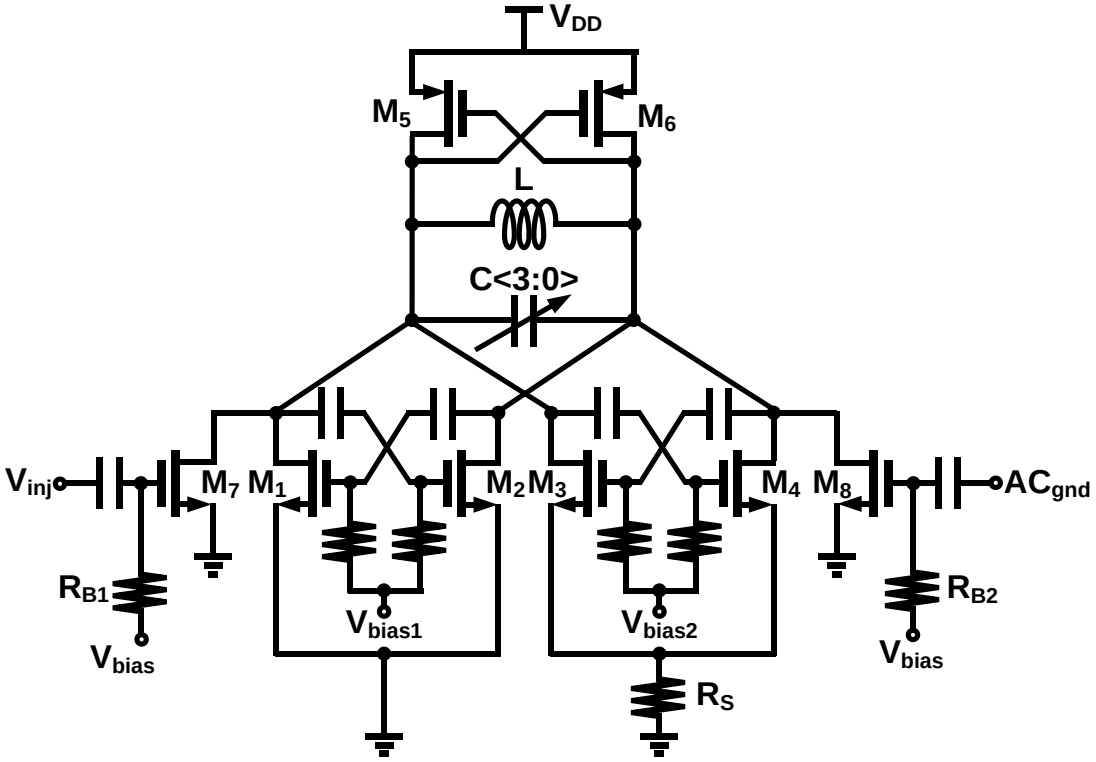

Fig. 3-11 Schematic of Dual-Conduction Digitally-Controlled Oscillator

Fig. 3-12 shows the simulated frequency tuning range of DCO by varying the varator tuning voltage at different digital code. The range covers from 430 to 460 MHz over different corners. With 4-bit capacitor array, DCO support the entire Med-radio band and ensure the flexibility of channel selection. The simulated phase noise at 100-kHz and 1-MHz offset from the carrier frequency is lower than -75 dBc/Hz and -110 dBc/Hz, respectively, as shown in Fig. 3-13. Table 3-4 summaries the simulated characteristic of the DCO.

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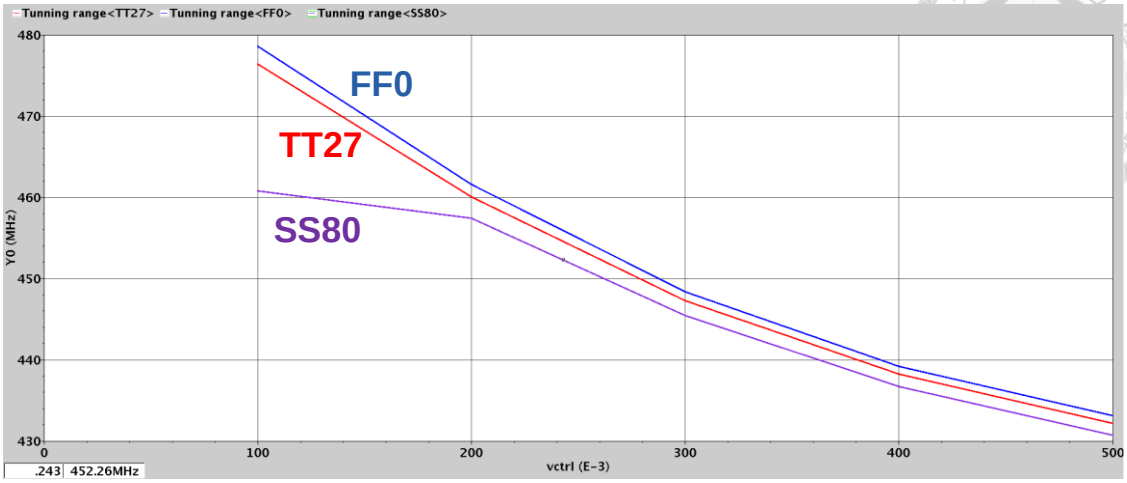

Fig. 3-12 Simulated analog frequency tuning range of DCO

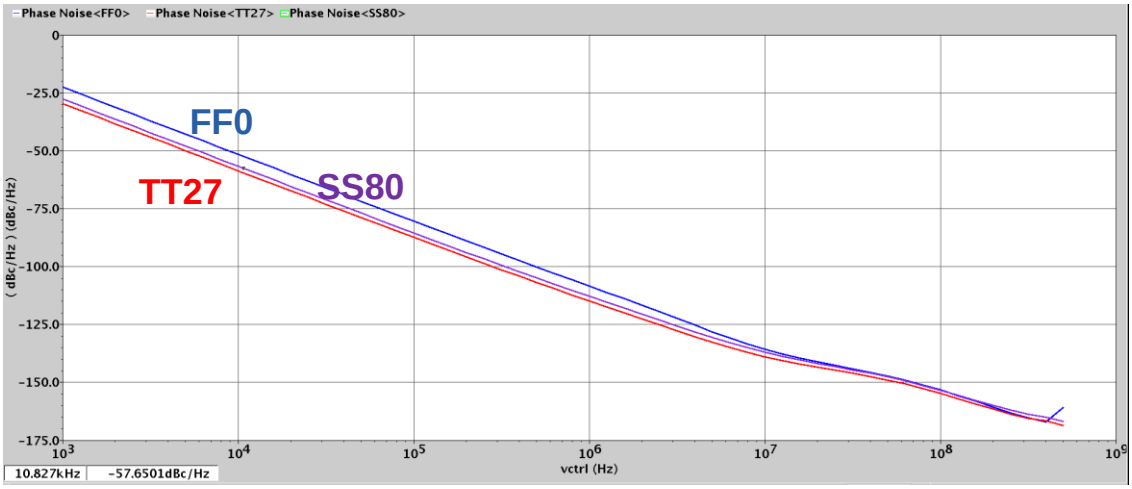

Fig. 3-13 Simulated phase noise of the DCO under different corners

Table 3-4 Simulated characteristics of the DCO @ TT27 °

Item	Value
Supply Voltage	0.5 V
Current	453 μA
Oscillation frequency	435 MHz
Phase Noise at 1 MHz	-110 dBc/Hz
Digital Control bits	4 bits
Total Tuning Range	60 MHz

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3.3.3 Baseband Circuits

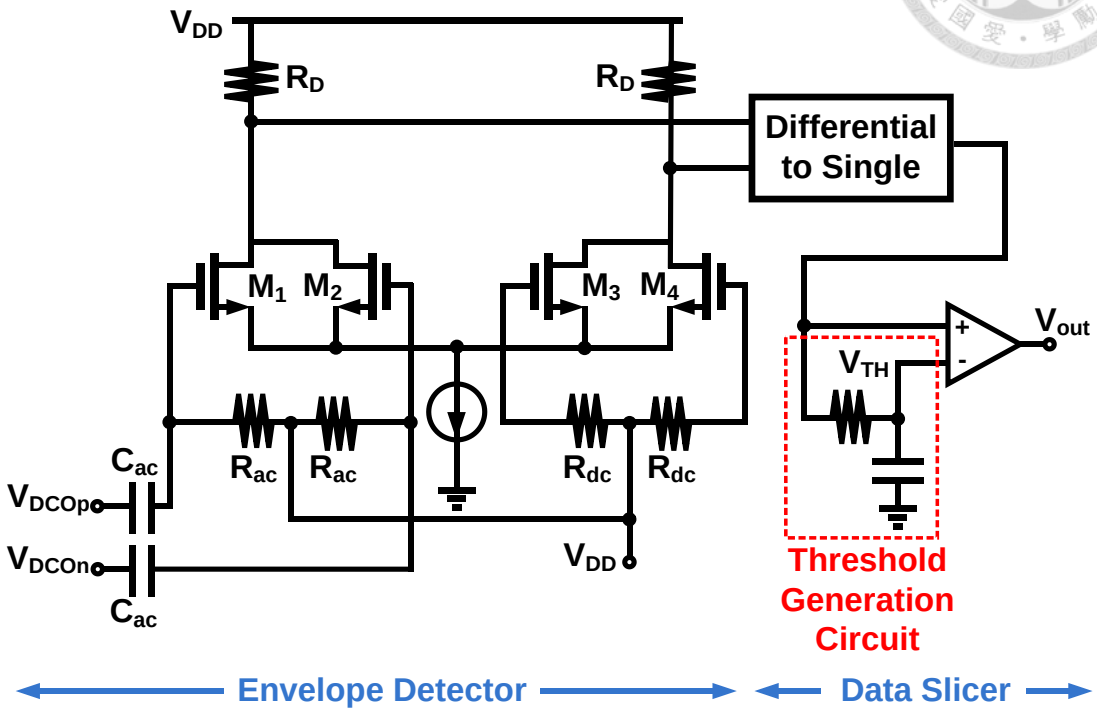

Fig. 3-14 Simplified baseband circuit

Fig. 3-14 shows the baseband circuits including an envelope detector and a data slicer. The envelope detector is realized as an active rectifier which feeds the data slicer to generate the raw data [28]. Since the envelope peak and valley levels will vary due to PVT variations, the threshold voltage of the slicer must be adaptively adjusted. This threshold voltage is generated by a low pass filter which has the ability to capture DC point of envelope waveform.

3.4 Simulation Results

The simulation results for total system are shown in Fig. 3-15 for the verification of theory analyzed in Chapter 3.1.2.

The data rate is 10 Mbps and the receiver demodulate D-BPSK encoded data to RZ data with input power is equal to -70 dBm.

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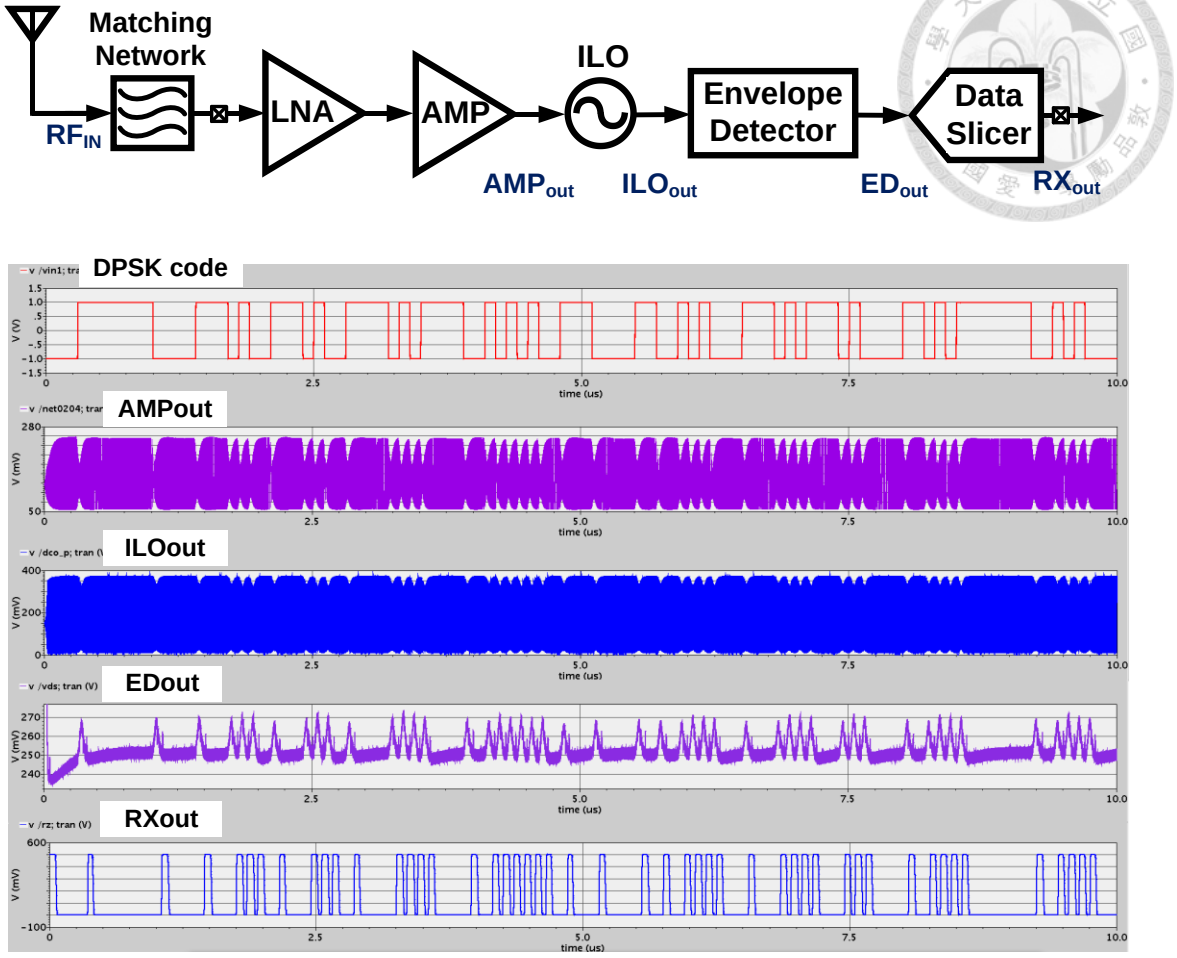

Fig. 3-15 Time diagram of Proposed RX

3.5 Experimental Results

3.5.1 Die Photo

This chip is fabricated in TSMC 0.18-μm CMOS 1P6M process and occupies a core area of 5.4 mm^2. As shown in Fig. 3-16, the whole system is divided into several blocks: low noise amplifier, injection-locked DCO, an envelope detector, and data slicer for producing RX output digital signal. Excepting for a 0.9-V supply used by output buffer for sufficient driving requirement of measurement, the supply for all the other blocks is 0.5 V. Besides, STC I/O PADS are applied to the interfaces of this die for ESD protection.

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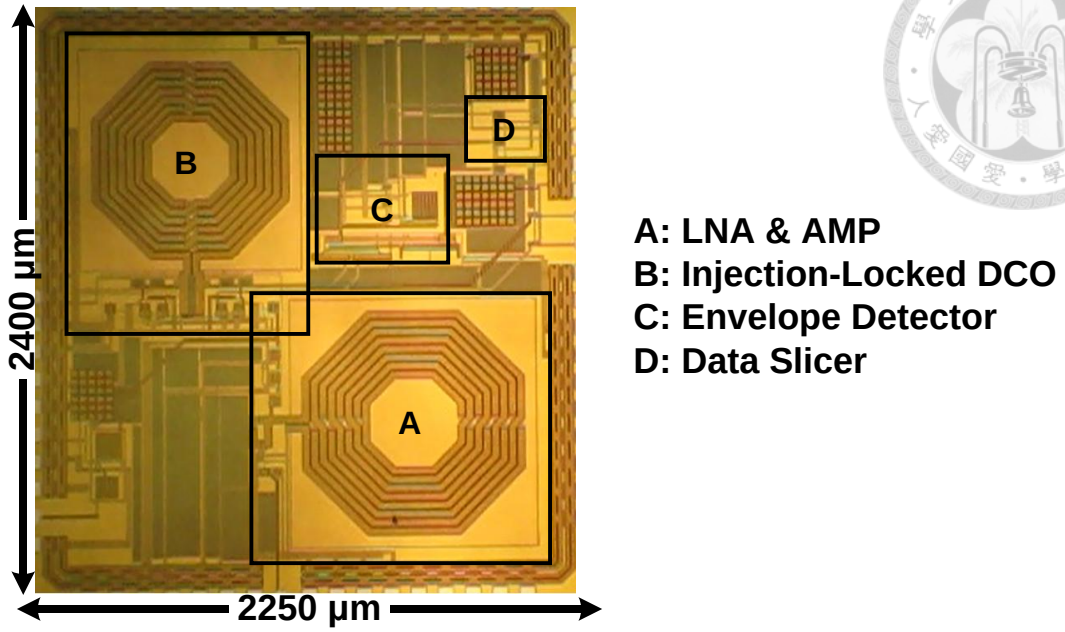

Fig. 3-16 Die Photo of the Proposed RX

3.5.2 Measurement Environment Setup

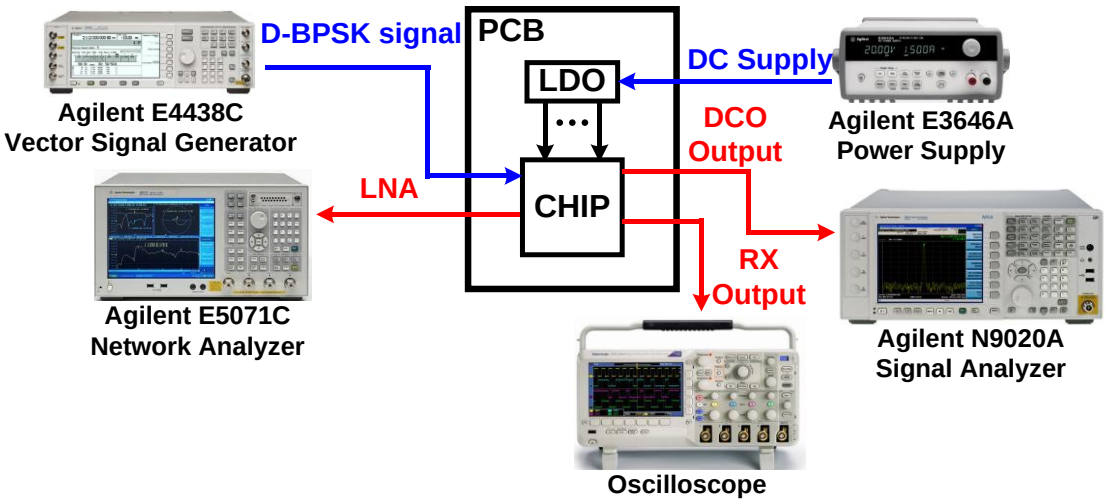

Fig. 3-17 Measurement Environment

The measurement environment setup is depicted in Fig. 3-17. Agilent E3646A power supply provides the dc supply for the LDO regulators which supply steady dc voltages on PCB. The network analyzer Agilent E5071C is utilized to measure the s-parameter of LNA, and oscilloscope is used for observing time-domain data.

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Moreover, signal analyzer Agilent N9020A measures the performance of DCO and the vector-signal generator Agilent E4438C provides D-BPSK modulation signal for testing.

3.5.3 PCB Design

A PCB is fabricated for testing and verifying the function of the proposed D-BPSK receiver, as shown in Fig. 3-18. There are two power domains on this PCB: a 0.9-V supply for supplying digital buffer, and a 0.5-V supply for core circuit. The 5-bit controlling signal tunes DCO free-run frequency. AC input/output signals, such as LNA output signal, input D-BPSK signal,, and DCO output signal, are connected through SMA terminals. The LNA matching network, composed of shunt capacitor and series inductor, is also welded on board.

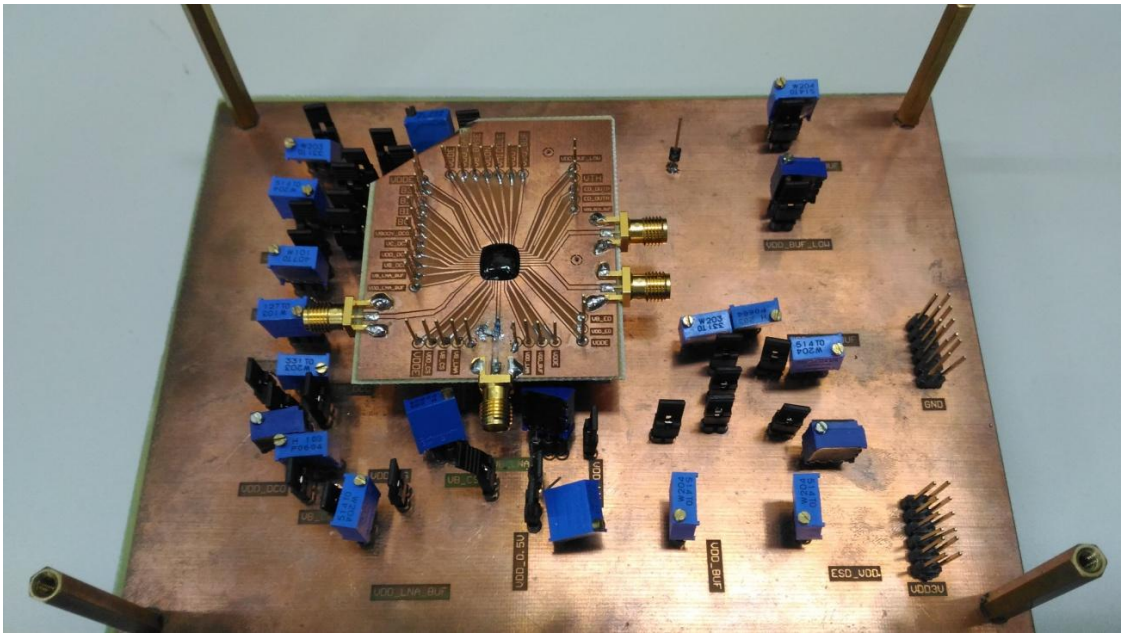

Fig. 3-18 PCB for Testing

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3.5.4 Measured Results

Fig. 3-19 shows the input-matching measurement for D-BPSK receiver with S11 is about -23.4 dB at 417MHz, and the bandwidth is larger than 10MHz.

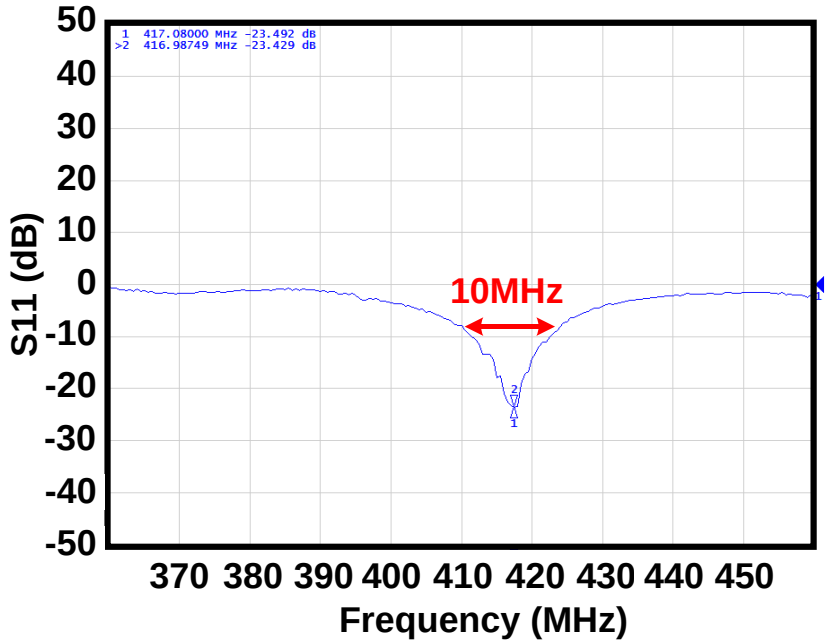

Fig. 3-19 Measured S11 Parameter

The measured phase noise of free-running DCO and injection-locked DCO are displayed in Fig. 3-20. As shown in the figure, the phase noise for injection-locked DCO is -91 dBc/Hz, -100 dBc/Hz, -111 dBc/Hz, and -114 dBc/Hz at frequency offset of 10 kHz, 100 kHz,1 MHz, and 10MHz. This measurement indicates that DCO phase noise is significantly improved by injection-locking technique.

The transmitted data generated from Agilent E4438C is in differentially encoded form. The ILO output experiences amplitude variation during every data transition of transmitted data. With the envelope detector and data slicer, the analog amplitude information is converted to a sequence of digital code, which is RZ data of RX output. For example, a sequence "01010101000000" is differentially encoded to

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"110011001111111", and this transmitted data is demodulated successfully with timing delay as shown in Fig. 3-21.

Fig. 3-22 depicted the measured relationship between bit error rate (BER) and input power, which indicate that the sensitivity is -45dBm at 10-Mbps.

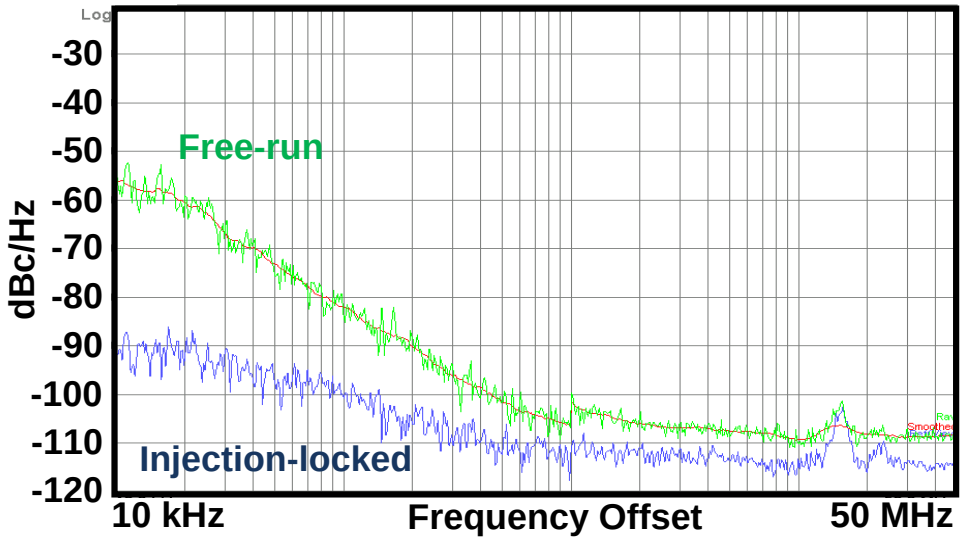

Fig. 3-20 Measured DCO Phase Noise

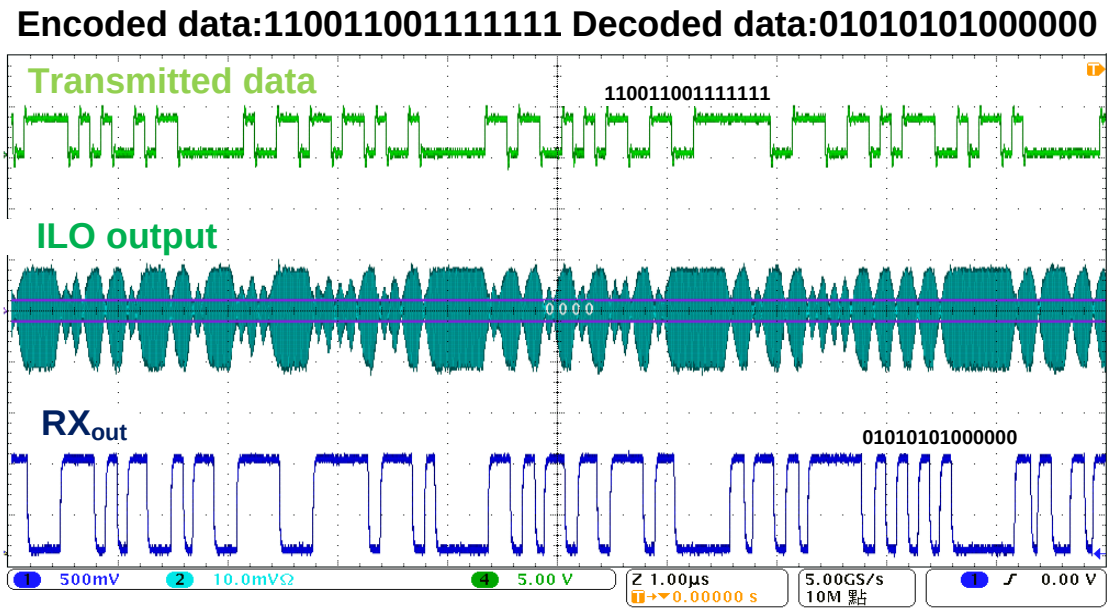

Fig. 3-21 Transient waveforms at 10-Mbps (Input power is -40 dBm)

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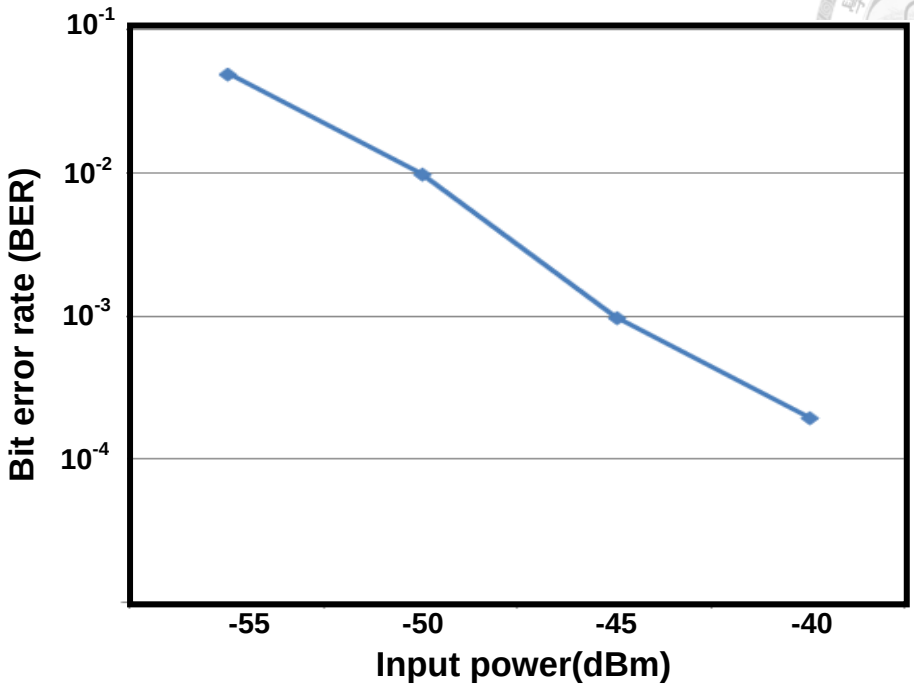

Fig. 3-22 BER Versus Input Power at 10-Mbps

Table 3-5 shows the detailed power breakdown of the proposed receiver. The total power consumption is 970 μW. Half of the power consumption is contributed by the RF front-end circuit. The baseband circuit (ED + Data Slicer) only consumes 45 μW.

Table 3-5 Power Breakdown of the D-BPSK RX

Circuit	**Power (μW)**
LNA+AMP	690
DCO	235
ED	40
Data Slicer	5
Total	**970**

Finally, Table 3-6 summarizes the performances of the proposed RX. By the comparison between the related works, it concludes that we proposed an ultra-low-voltage receiver with good energy efficiency.

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Table 3-6 Comparison Table of the Proposed RX

Reference	[9] VLSI'14	[19] T-MTT'11	[29] BioCAS'11	[30] ISOCC'14	**This Work**
Technology (nm)	180	90	180	110	**180**
Supply (V)	0.9	1.2	1.8	1.2	**0.5**
Modulation	D-BPSK	BFSK	OOK	OOK	**D-BPSK**
Freq. Band (MHz)	430	300	400	433	**414 ~ 454**
Data Rate (Mbps)	10	1	2	2	**10**
Power Con. (μW)	1770	120	590	750	**970**
Sensitivity (dBm)	-63	-34	-45	-50	**-45**
Energy/bit (pJ/bit)	177	120	295	375	**97**

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Chapter 4 Proposed Low-Power Injection-Locked D-BPSK Transmitter

4.1 Transmitter Introduction

4.1.1 Motivation

As discussed in Chapter 2.3 that many transmitters were published for low-power application. However energy-efficient transmitters with high data rate are much desired for short-range IoT applications in the future. Traditional injection-locked transmitter with edge-combing technique provides proper choice [21][22]. Nevertheless, the mismatch of edge combiner induces the spur issue in spectrum. To sum up, a low-power high-data-rate transmitter is needed to be proposed for addressing these issue.

4.1.2 Sub-harmonic injection-locked oscillator as phase modulator

The sub-harmonic injection-locked oscillator plays an important role on low-power transmitters. As depicted in Fig.4-1, the output phase noise of sub-harmonic injection-locked oscillator is dominated by that of input signal, where N is the frequency ratio between injection signal and free-running oscillator.

The equation (4-1) reveals that the phase-noise performance of the free-running DCO is not significantly important. However it depends on the phase-noise performance of input signal. According to the analysis in [23], the output phase noise of sub-harmonically injection-locked VCO is expressed in (4-1).

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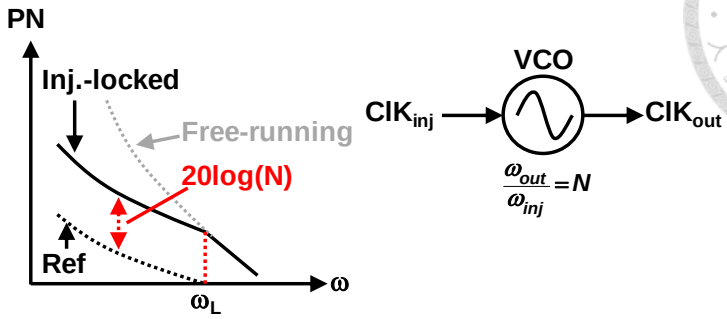

Fig. 4-1 Phase-Noise Behavior of a Sub-harmonically Injection-Locked VCO

$$L_{out} = L_{inj} + 20\log N \tag{4-1}$$

When sub-harmonic injection-locked oscillator is locked and return to steady state, the frequency of oscillator will oscillate at N times of the frequency of input injected signal. The relationship between phase and injected frequency is shown in (4-2). θ_{SS} is steady-state phase difference between input signal and oscillator signal, ω_L is locking range and ω_{osc} is free-running frequency. It reveals that phase difference is constant if the free-running frequency of oscillator is equal to N times input frequency of injected signal [26]. In other word, the phase of oscillator will track that of input injected signal when returning steady state.

$$\theta_{SS} = sin^{-1}(\frac{\omega_{osc} - N\omega_{inj}}{\omega_L}) \tag{4-2}$$

This property indicates that the phase modulator can be accomplished by a simple sub-harmonic injection-locked oscillator.

Assume the frequency ratio between injected frequency and oscillation frequency is an integer N. Equation (4-3) is derived for the phase relationship of oscillator and injected signal [23]. The change of phase for sub-harmonic injection-locked oscillator is N times the change of phase of input injected signal.

$$\Delta\theta_{osc} = N\Delta\theta_{inj} \tag{4-3}$$

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For an odd number N and assume only two phases, 0° and 180°, for injected signal, the equation (4-3) can be rewritten to (4-4).

$$\Delta\theta_{osc} = \begin{cases} 0^\circ, \Delta\theta_{inj} = 0^\circ \\ 180^\circ, \Delta\theta_{inj} = 180^\circ \end{cases} \quad (4\text{-}4)$$

It implies that low frequency multi-phase injected signals have the ability to modulate the high frequency oscillator rather than generating multi-phase oscillator for BPSK modulation at RF frequency.

Fig. 4-2 displays the operating principle of BPSK modulation. ($I_{inj,0}$) and ($I_{inj,\pi}$) represent 0° phase for symbol "0" and 180° phase for symbol "1" from baseband injected frequency. For transmitting symbol "0", a 0° input signal (right short solid line) is injected and the oscillator is locked to the same phase (right long solid line); on the other hand, the 180° input signal (left short dash line) is injected to drive oscillator to 180° phase (left long dash line) if transmitter delivers symbol "1".

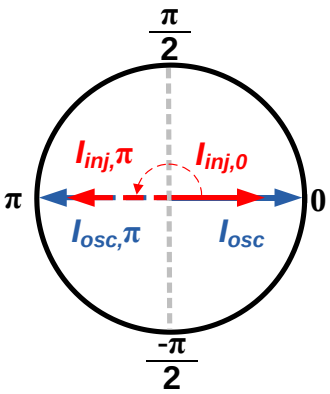

Fig. 4-2 The diagram of phase modulation by sub-harmonic injection technique

4.2 System Architecture

4.2.1 The Proposed D-BPSK Transmitter

The proposed architecture of the DPSK transmitter, as shown in Fig. 4-3, is composed of a single-to-differential buffer, a multiplexer (MUX), a pulse generator, an

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injection-locked ring oscillator (ILO), a PA, and a baseband circuit for D-BPSK encoding.

The single-to-differential buffer produces multi-phase information for MUX. Before injecting to the ILO, the signal is passing through the pulse generator for optimizing injection strength. The baseband circuit generates digital data to drive MUX and select correct phase signal. Therefore, the sub-harmonically injection-locked ring oscillator performs phase modulation. That is the the phase of ILO depends on the phase of injected signal as discussed in Chapter 4.1.2. Finally, power amplifier transmitted the modulated RF signal to output.

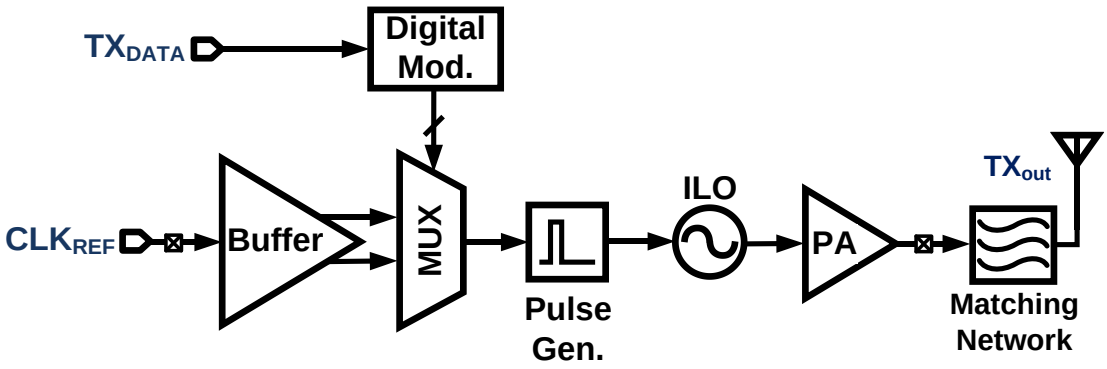

Fig. 4-3 Proposed DPSK Transmitter with Sub-harmonic Injection-Locked Modulation

4.2.2 Design Specifications of the Proposed Transmitter

Error vector magnitude (EVM) is defined as the deviation of the constellation points from their ideal positions [11].

The magnitude deviation ($\frac{\Delta A}{M}$) is small enough to be neglected when comparing with phase deviation in this work, the relationship between EVM and phase error can be expressed in (4-5) according to [32].

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$$EVM = \sqrt{\frac{\Delta A}{M} + {\theta_{err,rms}}^2} \approx \theta_{err,rms} \tag{4-5}$$

The main factor that affects EVM performance is the phase error caused by sub-harmonically injection-locked technique. As analyzed in Chapter 4.1.2, there's no phase error if the free-running frequency of oscillator is equal to N times input frequency of injected signal in ideal environment. However, the frequency mismatch due to the non-ideal effect in real circuit will induce the periodic phase error.

Equation (4-6) shows the connection between EVM and frequency deviation Δf, center frequency f_0 and N is the sub-harmonic injection ratio which affects the performance of EVM significantly [31].

$$EVM \approx \theta_{err,rms} = \sqrt{\frac{1}{T_{INJ}} \int_{T_{INJ}} \left(\theta_{err}(t)\right)^2 dt} = \frac{2\pi}{\sqrt{3}} \frac{N \cdot \Delta f}{f_0} \tag{4-6}$$

The improvement of EVM is by setting N as small as possible. However, it means that most circuit blocks operating at higher frequency, which consumes more power. That is to say, there is a trade-off lying between power and EVM. Therefore, the sub-harmonic injection ratio N is designed to be 9 in this proposed architecture.

To substitute the design parameter f_0 = 430 MHz, N is 9 and assume the worst frequency deviation Δf is 100 kHz , the EVM is smaller than 1% which obeys the specification for this target.

The injection spurs resulting from sub-harmonic injection-locked technique are discussed at [31], and (4-7) shows the connection to design parameter. The performance of spurs also depends on the sub-harmonic injection ratio.

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$$Spur(\text{dBc}) = 20\log(\frac{N \cdot \Delta f}{f_0}) \quad (4\text{-}7)$$

The level of spur is -33.58 dBc with the same parameters which are substituted into equation (4-6).

Another significant specification is maximum data rate which is dominated by locking range ω_L as discussed in Chapter 3.2.2. According to (3-14), the locking range ω_L of ILO must be larger than 2π*6.366 MHz if maximum data rate is 10 Mbps. This requirement of locking range for ring oscillator isn't a tight specification for transmitter.

The injection strength not only depends on the amplitude of injected signal but also the pulse width. In this system, the pulse width is only the designed parameter because the amplitude is rail to rail swing which is limited by voltage supply (0.5V).

Equation (4-8) shows the Fourier transform for a pulse with pulse width W= $D \cdot T_{INJ}$, which D is duty cycle for injected signal whose period is $T_{INJ,}$ and K_N represents the injection strength.

$$K_N = D \cdot T_{INJ} \frac{Sin(N\pi \cdot D)}{N\pi} \quad (4\text{-}8)$$

N, the sub-harmonic injection ratio is 9, and the maximum injection strength K_9 is obtained by setting duty cycle D is 1/18. It is the optimum value of pulse width for sub-harmonic injection oscillator.

To sum up, the maximum data rate determines the locking range of sub-harmonic injected oscillator. Not only EVM but also spur is affected by the sub-harmonic injection ratio mainly. Moreover, the injected pulse width is required to be designed carefully for maximum injection strength. Above analysis provides insights into the design of TX system. Finally, the specification of this work is shown in Table 4-1.

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Table 4-1 Designing Specifications of D-BPSK Transmitter

Process	TSMC 0.18-μm CMOS
Supply Voltage	0.5 V
Operating Frequency	414 ~ 457 MHz
Max Data Rate	10 Mbps
Pout	>-10 dBm
Modulation	D-BPSK
Power Consumption	< 0.3 mW
Energy Efficiency	< 30 pJ/b

4.3 Circuit Implementation

4.3.1 Pulse Generator

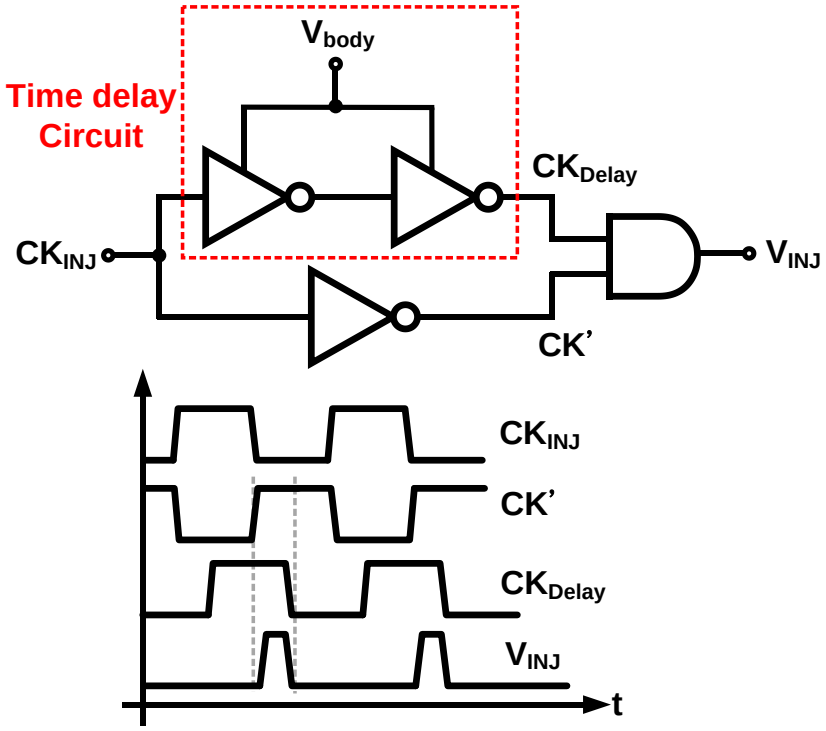

Fig. 4-4 Pulse Generator

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A pulse generator which is depicted in Fig. 4-4 is adopted for generating optimum injected pulse width from an external clock reference (CK_{INJ}) as mentioned in Chapter 4.2.2. The pulse width of the pulse generator can be tuned through modifying the time delay circuit with body-bias technique, and Fig. 4-5 displays the tuning range of pulse width, and the range is from 400 ps to 2.3 ns at different corner conditions.

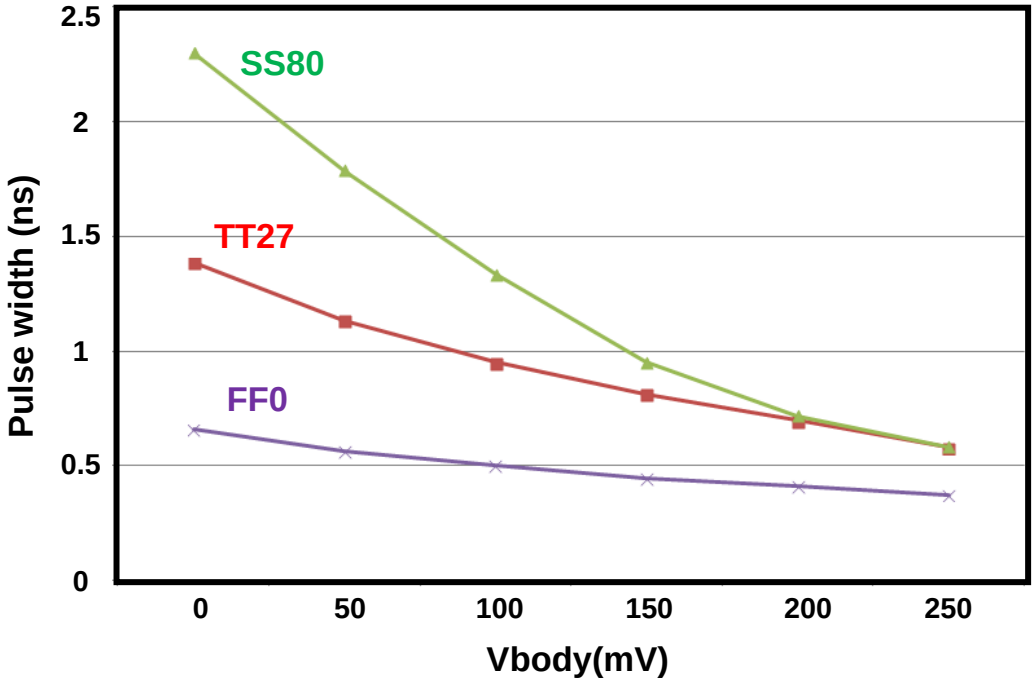

Fig. 4-5 The pulse width tuning range

4.3.2 Sub-harmonically Injection-Locked Ring DCO

Fig. 4-6 displays a 3-stage sub-harmonically single-ended injection-locked ring DCO in this work. The injection-locking technique is realized by shorting one of the stages to ground through an NMOS, and this would make the transition edge of V_{OSC} align with that of V_{INJ}. The output phase noise performance of a ring DCO can be improved effectively with sub-harmonic injection-locked technique as discussed in Chapter 4.1.2.

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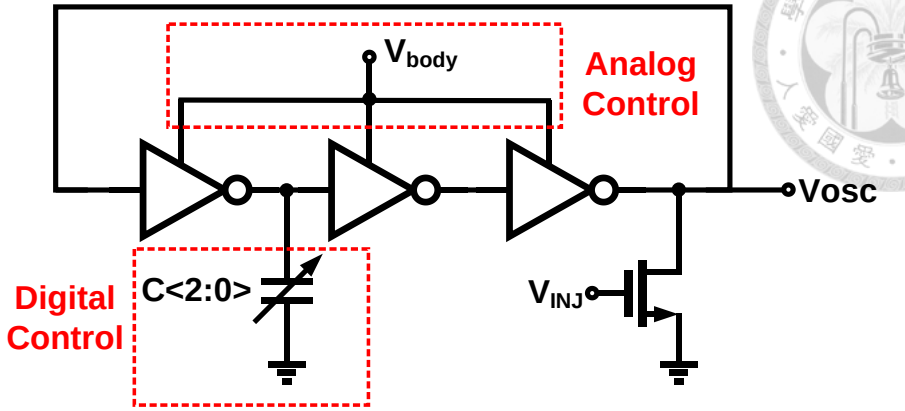

Fig. 4-6 Single-ended Sub-harmonic Injection-Locked Ring Oscillator

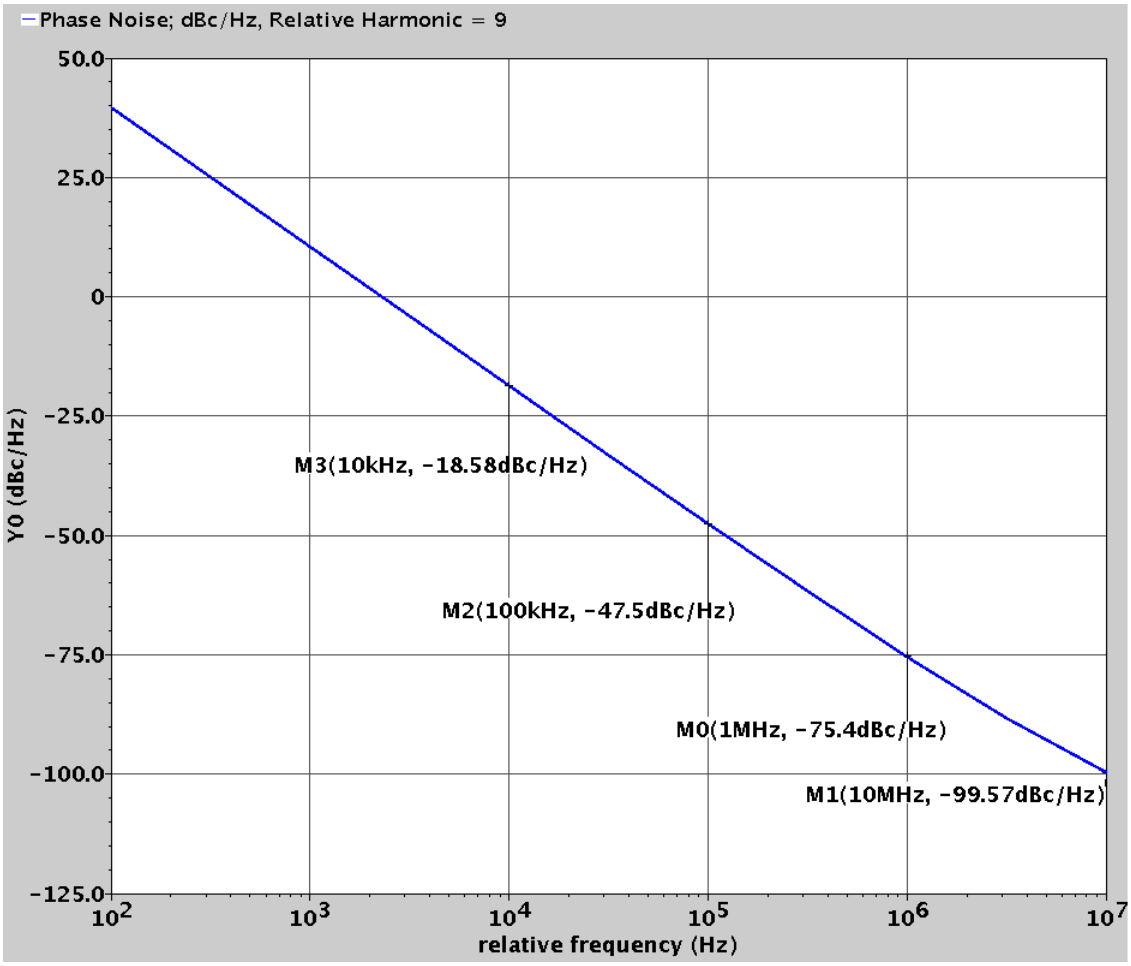

Fig. 4-7 Simulated Phase Noise of Ring Oscillator (Carrier@430MHz)

Fig. 4-7 displays the simulated phase noise of the single-ended injection-locked ring DCO under free-run conditions, and it is simulated under TT corner with 27°

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temperature. As the figure shows, the phase noise for free-run DCO is -18.58 dBc/Hz, -47.5 dBc/Hz, -75.4 dBc/Hz, and -99.57 dBc/Hz at frequency offset of 10 kHz, 100 kHz,1 MHz, and 10MHz. Table 4-2 summaries the simulated characteristic of the DCO.

Table 4-2 Simulated characteristics of the DCO @ TT27 °

Item	Value
Supply Voltage	0.5 V
Current	198 μA
Oscillation frequency	435 MHz
Phase Noise at 1 MHz	-99 dBc/Hz
Digital Control bits	3 bits
Total Tuning Range	70 MHz

4.3.3 Power Amplifier

To achieve low-power operation, the class-E power amplifier is adopted in ultra-low power supply (0.5V). An inverter inserted between DCO and PA acts as a buffer for the purpose of isolation. The detailed circuit implementation with the output impedance transformation is shown in Fig. 4-8.

The output 50-ohm matching at TX_{OUT} is accomplished by the tapped matching work which is composed of the choke inductor L and capacitors C_1, C_2. Assume the quality factor Q of inductor L is larger than 10, then the following approximation establishes the impedance transformation in equation (4-9), where R_L is output loading whose value is usually 50-ohm.

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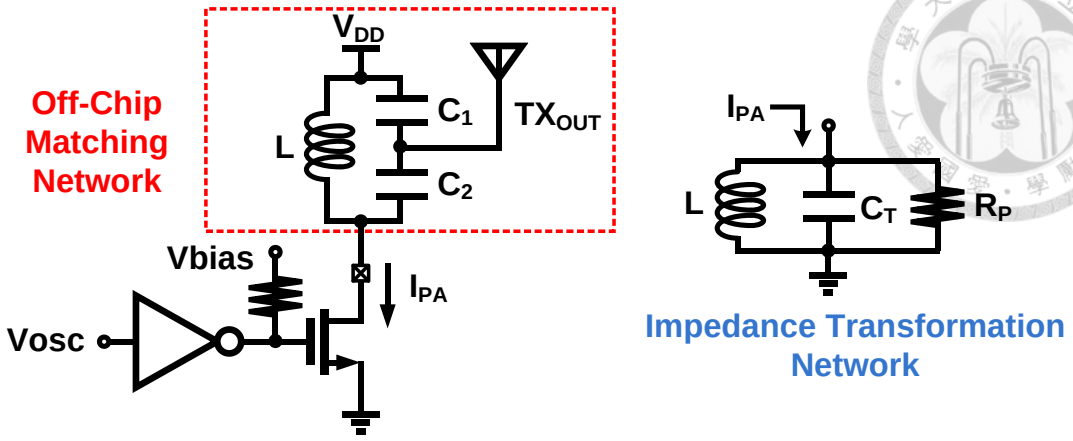

Fig. 4-8 Class-E Power Amplifier and Output Impedance Transformation Network

$$C_T \approx \frac{C_1 C_2}{C_1 + C_2} \quad , \quad R_P \approx \left(\frac{C_1 + C_2}{C_2}\right)^2 \cdot R_L \tag{4-9}$$

The tapped output matching network is simplified as a LC tank. The DC current (I_{PA}) required for a certain PA output power can be approximately estimated as follows.

$$V_{EC} \approx \frac{2}{\pi} I_{PA} R_P \tag{4-10}$$

Here, V_{EC} is the voltage amplitude on LC-tank loading, and the TX output is derived as equation (4-11). Given R_L = 50 ohms, C_1 = 10 pF, and C_2 = 4 pF, the required I_{PA} need to be larger than 295 μA for P_{OUT} larger than -10dBm.

$$TX_{OUT} \approx V_{EC} \frac{\frac{1}{sC_1} \parallel R_L}{\frac{1}{sC_2} + \left(\frac{1}{sC_1} \parallel R_L\right)} = \frac{2}{\pi} I_{PA} \frac{sR_L^2 (C_1 + C_2)}{sR_L C_2 + C_2 / (C_1 + C_2)} \tag{4-11}$$

The simulated result is displayed in Fig. 4-9. Under TT corner with 27° temperature the output power at TX_{OUT} is -12.02 dBm. The spur is smaller than

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-40dBm as discussed in Chapter 4.1.2. Table 4-3 summaries the simulated characteristic of the PA.

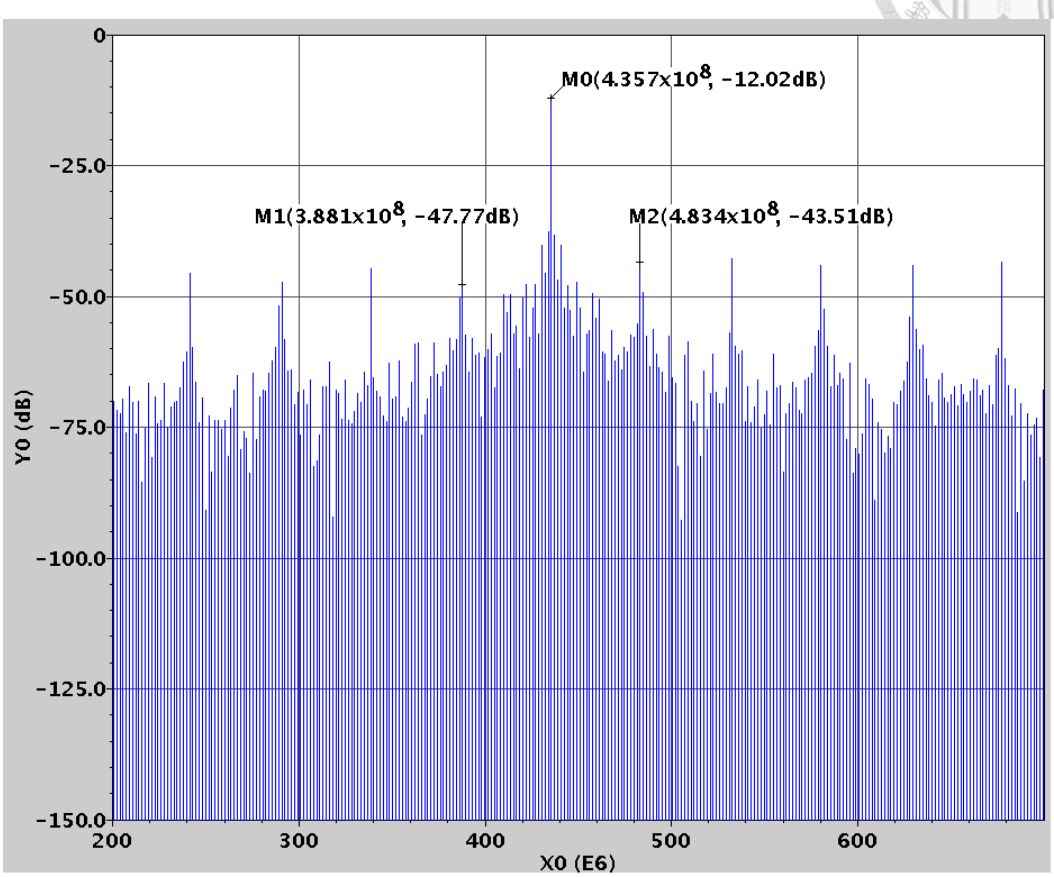

Fig. 4-9 PA Output Spectrum with injected signal

Table 4-3 Simulated characteristics of the PA @ TT27 ^{o}

Item	Value
Supply Voltage	0.5 V
Current	295 μA
Oscillation frequency	435 MHz
Max Pout	-9.7dBm
Efficiency	62.5%

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4.4 System Simulation Results

The system simulation results displayed in Fig. 4-10 verifies the sub-harmonic injected-locked modulation technique.

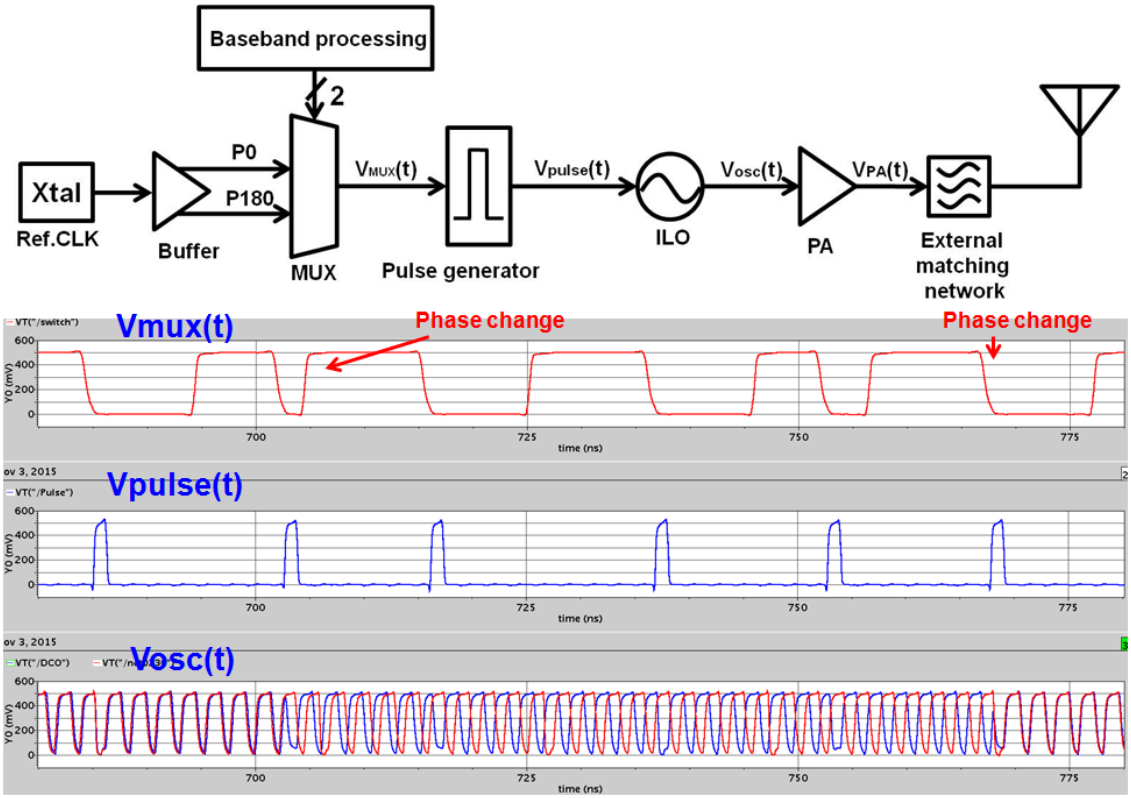

Fig. 4-10 Timing diagram of Proposed TX

4.5 Experimental Results

4.5.1 Die Photo

This chip is fabricated in TSMC 0.18-μm CMOS 1P6M process and occupies a core area of 0.8 mm^2. As shown in Fig. 4-11, the whole system is divided into several blocks: baseband circuit, injection-locked DCO, a pulse generator, and a power amplifier for transmitting TX output signal. The supply voltage for all blocks is 0.5 V.

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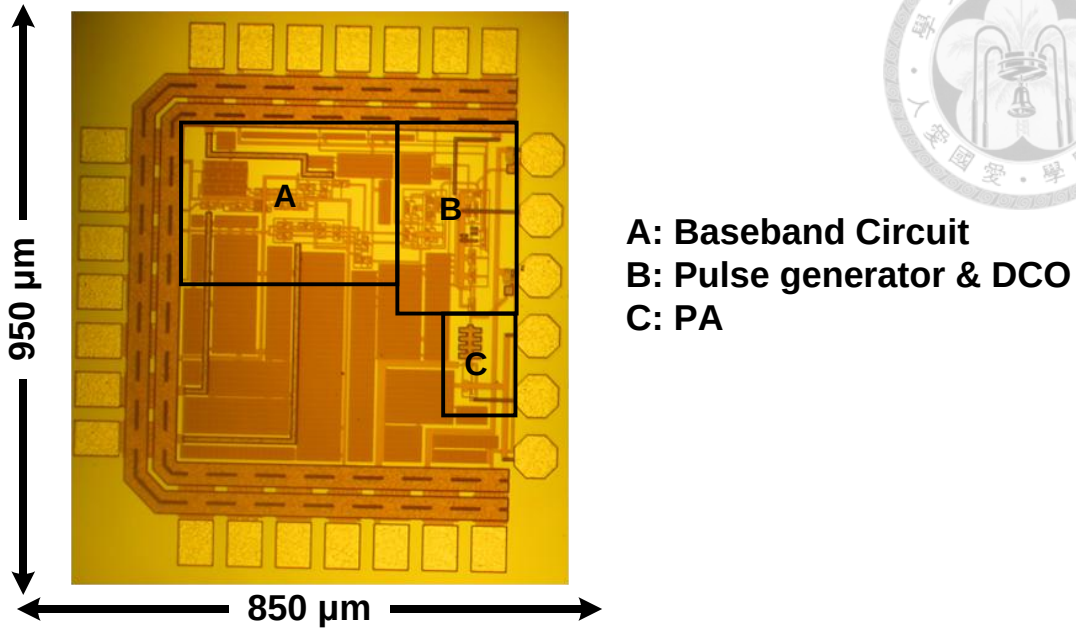

Fig. 4-11 Die Photo of the Proposed TX

4.5.2 Measurement Environment Setup

The measurement environment setup is depicted in Fig. 4-12. LDO regulators stabilize dc voltages which provided by Agilent E3646A power supply. Then, a R & S SML03 signal generator generates the 44.45 MHz injection signal, and an Agilent 33250A waveform generator provides the 10 MHz baseband data clock. Finally, signal analyzer (Agilent N9020A) measures the performance of the PA output signal.

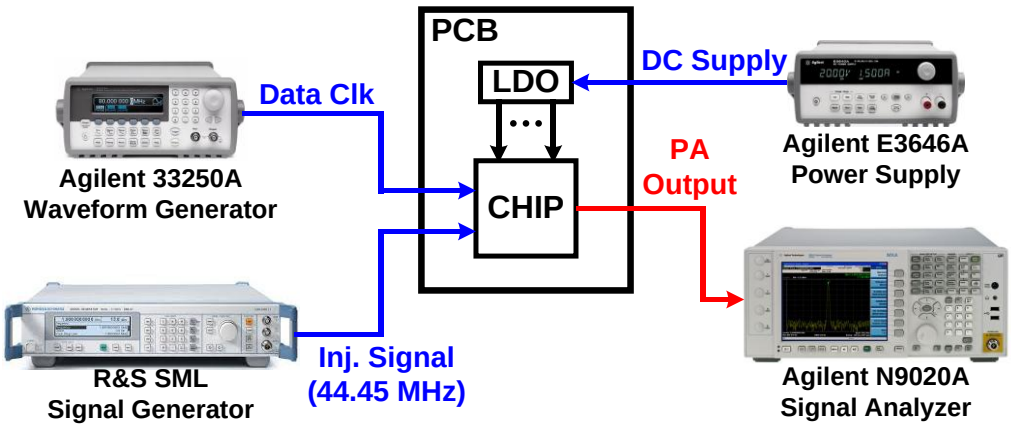

Fig. 4-12 Measurement Environments

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4.5.3 PCB Design

A PCB is fabricated for testing and verifying the function of the proposed D-BPSK transmitter as shown in Fig. 4-13. The 3-bit controlling signal with analog voltage tunes DCO free-run frequency. AC input/output signals, such as PA output signal, input clock signal, and baseband signal, are connected through SMA terminals. The PA matching network, composed of shunt capacitors and series inductor, is also welded on board.

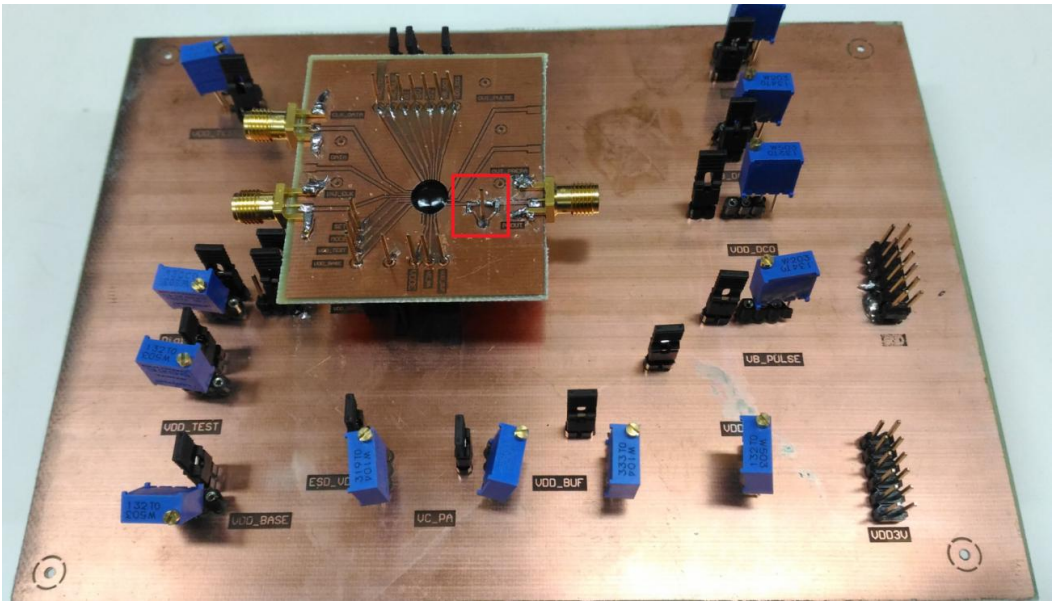

Fig. 4-13 PCB for Testing

4.5.4 Measured Results

Fig. 4-14 shows the measured TX output spectrum at 410 MHz, and the system output power is -18 dBm. Moreover the adjacent spur tone is less than -70 dBm. The relationship between frequency and output power is depicted in Fig 4-15. It indicate the output power remain -18 to -22dBm from 360MHz to 420MHz.

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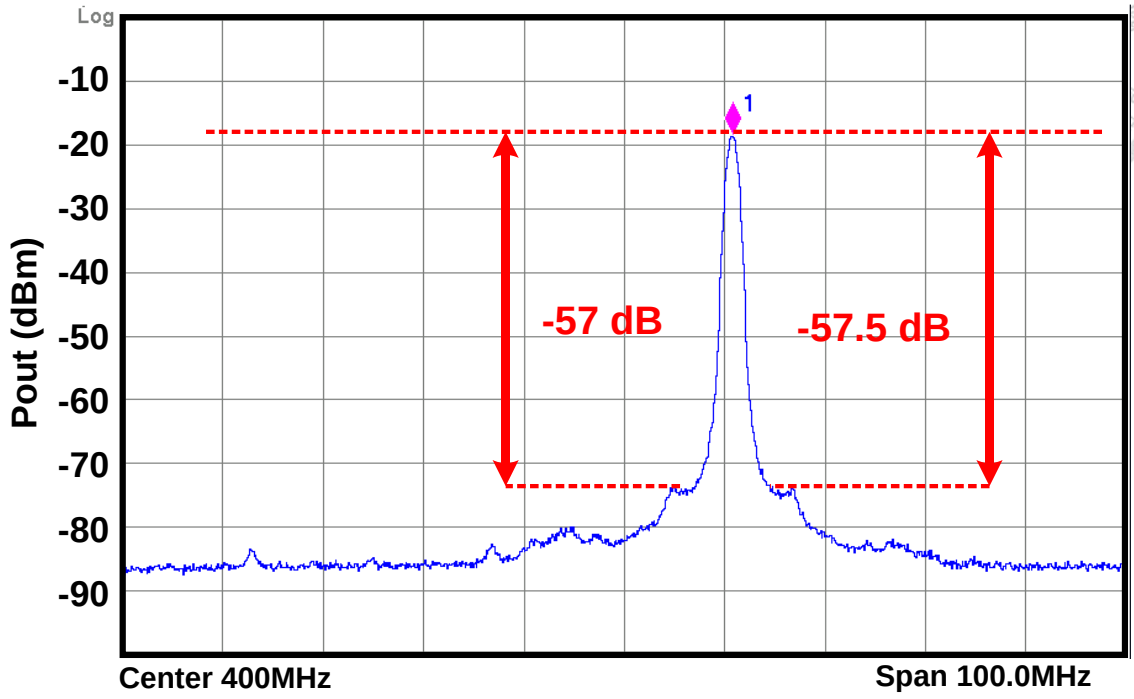

Fig. 4-14 TX Output Spectrum

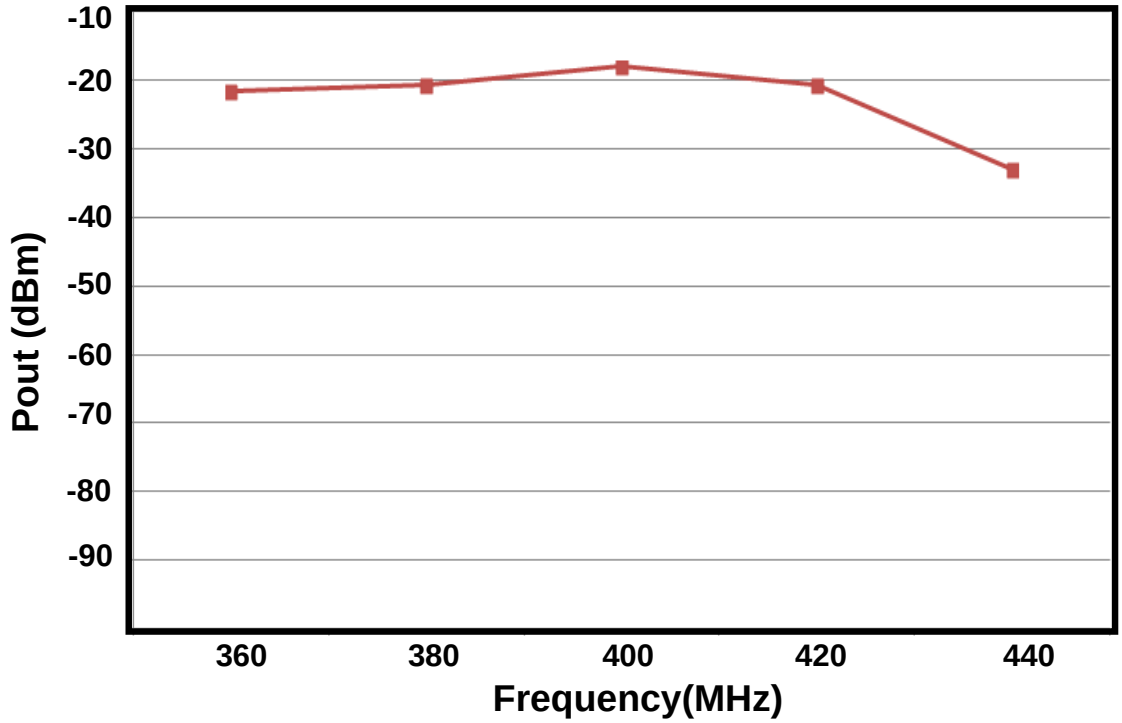

Fig. 4-15 TX Output Power versus Frequency

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TX free-running output waveform is displayed in Fig. 4-16. The peak to peak swing is about 74.4 mV. With output loading of 50-ohm, the output power is about -18dBm, which is similar value to that measured one by signal analyzer.

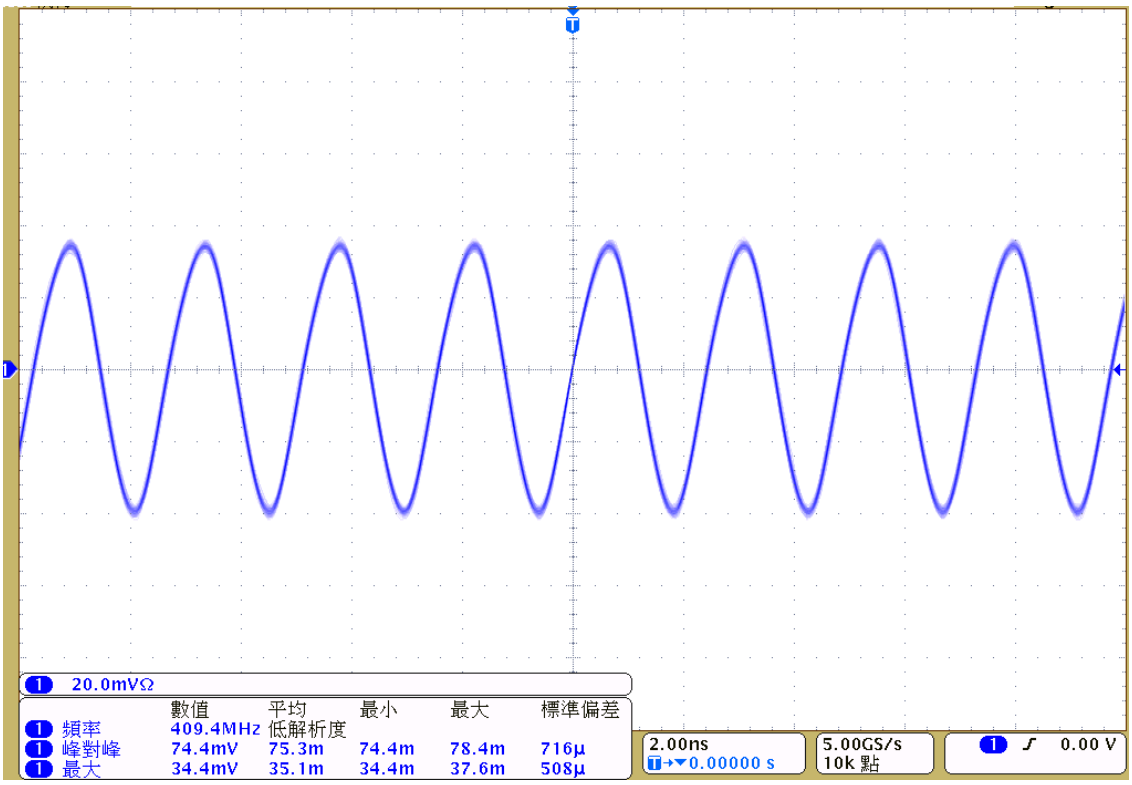

Fig. 4-16 TX free-running transient waveform

TX output phase noise under free-run ring DCO, injection-locked ring DCO is displayed in Fig. 4-17. This graph reveals that the phase noise of TX output carrier signal is dominated by injection-locked technique. However, this measurement indicates the injected strength is not enough, so the improvement of the phase noise is limited.

The phase modulation in this work is achieved by sub-harmonic injection-locked technique. In other word, the injection-locked step must be completed before performing phase modulation. However, the measurement in Fig. 4-17 shows that the injection does not function properly.

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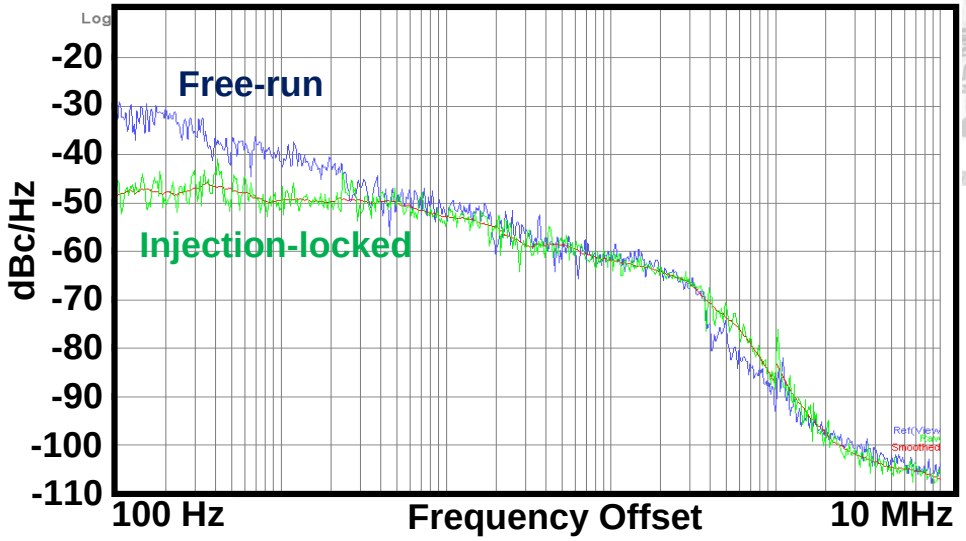

Fig. 4-17 Measured TX Output Phase Noise

Table 4-4 displays the detailed power breakdown of the proposed transmitter. The voltage supply is 0.5V for all blocks. Most power consumption is contributed by the power amplifier and DCO because those blocks operating at RF frequency. Nevertheless, the single-ended ring topology for oscillator and class-E PA reduce the total power consumption significantly. The measured value is only 331 μW.

Table 4-5 summarizes the simulated results of the proposed TX and the comparison to related works.

Table 4-4 Power Breakdown of the D-BPSK TX

Circuit	**Power (μW)**
Baseband Circuit	56
DCO	128
PA	147
Total	**331**

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Table 4-5 Comparison Table of the Proposed TX

Reference	[21] JSSC'11	[32] TMTT'12	[18] JSSC'11	**Simulated Result**	**Measured Result**
Technology (nm)	130	180	180	**180**	**180**
Supply (V)	1.2	1.4	0.7	**0.5**	**0.5**
Modulation	BFSK	QPSK	BFOK	**D-BPSK**	**D-BPSK**
Freq. Band (MHz)	400	915	920	**414 ~ 454**	**414 ~ 454**
Data Rate (Mbps)	0.2	100	5	**10**	**N/A**
Power Con. (μW)	90	5600	700	**294**	**331**
Pout (dBm)	-17	-3	-10	**-9.7**	**-18**
Energy/bit (pJ/bit)	450	560	140	**29.4**	**N/A**

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Chapter 5 Conclusions and Future Works

5.1 Conclusions

This thesis introduces ultra-low-voltage wireless transceiver for wearable applications. The dynamic phase-to-amplitude conversion by injection-locked oscillator diminishes power consumption of receiver. Furthermore, the transmitter with the sub-harmonically injection-locked ring oscillator performs phase modulation without power-hungry blocks such as multi-phase carrier generation.

Both transmitter and receiver adopt injection-locked technique and operate at 0.5 V for the purpose of high energy-efficient communication. The forward body bias skill is used for reducing threshold voltage in ultra-low-voltage environment. Besides, this technique can be utilized for the current tuning of transistor. Not only time-delay circuit but also voltage-controlled oscillators require body-bias skill.

5.2 Future Works

Recalling from the experimental results in chapter 3.5, the sensitivity of receiver does not meet the design of specification. To address the degraded sensitivity, a direct-tail injected oscillator with differential injected path can be adpoted.

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