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碩士論文

Graduate Institute of Communication Engineering
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Master Thesis

毫米波頻段放大器及功率放大器之共模穩定性研究

Research of Amplifiers and Common-mode Stability of Power Amplifiers at Millimeter-wave Frequencies

莊博翔

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中文摘要

本論文介紹一個製作於砷化鎵假型高速電子場效電晶體製程之低雜訊放大器、一個製作於互補式金屬氧化物半導體製程之開關鍵控調變器，以及一個製作於互補式金屬氧化物半導體製程之功率放大器。

首先為一個應用於第五代行動通訊之Q頻段低雜訊放大器以0.15微米砷化鎵假型高速電子場效電晶體製程設計與製作，此低雜訊放大器採用三級共源級的架構，第一共源級採用源級衰退技術以達到均衡的雜訊及增益表現，而第二、三共源級則是採用 RC 回授技術以達到寬頻表現，另外，放大器第三級前後之匹配網路採用 π 型匹配網路以達到寬頻的阻抗匹配。在第一次實驗結果後，電晶體模型不準確導致量測與模擬結果的不一致，在進一步討論與分析後提出模擬上的修正方法，修改晶片設計後再藉由第二次晶片製作及實驗結果驗證所提修正方法之正確性。此低雜訊放大器放大器達到優異的 3-dB 頻寬(24.7 至 40.0 GHz)以及平均增益(22.2 dB)表現，雜訊指數則在寬頻(27.9 至 40.0 GHz)下皆低於 3 dB。

之後描述一個應用於短距無線通訊之 60-GHz 頻段開關鍵控調變器以 90 奈米互補式金屬氧化物半導體製程設計與製作，此調變器結合了發射機中調變以及輸出放大之功能，進而達到在未來的應用上低複雜度與高效率的發射機架構。此調變器基於共源共柵架構，並採用在此提出的一基於變壓器之回授技術，此技術能提升調變器「開」狀態下的增益及輸出功率表現，以及「關」狀態下的隔離度表現，另外，為了降低基頻調變訊號輸入路徑上的 RC 常數以減輕高速率傳輸下基頻調變訊號的失真，該路徑透過一串接電感及到地電容的設計以達到所要目的。藉由採用基於變壓器之回授技術，此開關鍵控調變器於 60-GHz 達到優異的輸出 1-dB 功率壓縮點(7.0 dBm)、小訊號增益(10.2 dB)、以及「開-關」隔離度(45.4 dB)表現，在開關鍵控調變上，此調變器能達到 10 Gb/s 之傳輸速率，由於變壓器所需的低佈局空間優勢，加上僅需單一調變訊號輸入路徑，此調變器達到相當小的晶片佈局。

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最後則討論一個應用於短距無線通訊之 W 頻段功率放大器以 65 奈米互補式金屬氧化物半導體製程設計與製作，藉由於輸出端採用一基於變壓器之放射對稱功率結構，以達到低損耗及阻抗匹配上的不平衡，此二項參數皆在極高頻的功率放大器設計上有相當大的重要性。在第一次實驗後於毫米波頻段發現非預期的振盪現象，在討論以及多方面的穩定性分析後判斷為共模訊號下位於輸出級的不穩定現象，並提出針對輸出級前後採用的變壓器設計的電路修改方法，在不影響差動訊號下之阻抗匹配情況的前提下，消除共模訊號下之不穩定現象，經過在第二次晶片製作，實驗顯示非預期振盪之問題已解決，並驗證所提出修改方法的正確性。另外，亦討論了用於極高頻功率放大器電路設計時的變壓器模型問題。

關鍵字 – 砷化鎵假型高速電子場效電晶體、第五代行動通訊、低雜訊放大器、寬頻、Q 頻段、互補式金屬氧化物半導體、開關鍵控調變、調變器、功率放大器、發射機、共柵共源、變壓器回授、隔離度、60 GHz、V 頻段、功率結合結構、毫米波振盪現象、共源訊號不穩定現象、W 頻段。

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ABSTRACT

The thesis presents a GaAs pHEMT low noise amplifier, a CMOS on-off keying modulator, and a CMOS power amplifier.

Firstly, a Q-band low noise amplifier for fifth-generation communication applications is designed and realized in 0.15-μm GaAs pHEMT. The LNA consists of three common-source stages. Source degeneration is adopted at the first stage for a balanced noise and gain performance, and RC-feedback is adopted at the latter two stages for its wideband characteristics. In addition, π-type matching networks are used at the third stage for wideband impedance matching. Inaccurate device modeling caused disagreement between the measurement and simulation results of the original LNA. The modeling issues are discussed and analyzed, and corrections to the simulation setups are proposed and verified via the measurement results of a modified LNA in the second tape-out. The LNA exhibits wide 3-dB bandwidth from 24.7 to 40.0 GHz, with average gain of 22.2 dB. The noise figure is below 3 dB from 27.9 to 40.0 GHz, with average of 2.6 dB from 26 to 40 GHz.

Secondly, a 60-GHz OOK modulator for short range wireless communications is designed and realized in 90-nm CMOS. By combining the functions of modulation and output amplification in a single circuit, a transmitter of lower complexity and higher efficiency can be achieved for future applications. A novel transformer-feedback technique is proposed for the cascode-based modulator for improvements in output power, gain performances at on-state, and isolation performance at off-state. A data input network is designed to achieve low RC time constant, and avoids distortion of the baseband data signal at high data rates. With the proposed transformer-feedback technique, the modulator achieves an OP_{1dB} of 7.0 dBm, gain of 10.2 dB, and on-off isolation of 45.4 dB at 60 GHz. For OOK modulation, data rates of up to 10 Gb/s have been measured. Due to the compact transformer and the single modulation path required, the modulator achieves a compact layout footprint of 471 x 519 μm^2 with RF and DC pads included.

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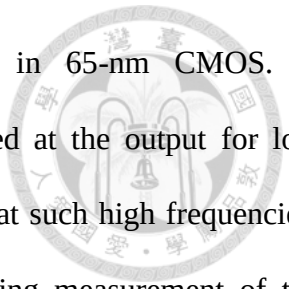

Finally, a W-band power amplifier is designed and realized in 65-nm CMOS. A transformer-based radial-symmetric power combining structure is adopted at the output for low insertion loss and matching imbalances, which are critical in PA designs at such high frequencies. Undesired oscillations at millimeter-wave frequency were observed during measurement of the original PA. Discussions and various stability analyses are performed to identify the issue as common-mode instabilities at the output stage. Modifications to the transformers at the output stage are proposed in order to eliminate the common-mode instabilities, without altering the impedance matching conditions in differential mode. The proposed modifications are verified through the absence of undesired oscillations during the measurement of a modified PA in the second tape-out. Modeling issues of high frequency transformer designs are also discussed.

Index Terms – GaAs pHEMT, fifth-generation (5G) communications, low noise amplifier, wideband, Q-band, CMOS, on-off keying (OOK), modulator, power amplifier, transmitter, cascode, transformer feedback, isolation, 60 GHz, V-band, power combining, millimeter-wave oscillation, common-mode instability, W-band.

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Chapter 1 Introduction

1.1 Backgrounds and Motivations

The fifth generation (5G) wireless communication has been the focus of interests in recent years. Compared to the current fourth generation long-term evolution (4G-LTE) configuration, 5G promises at least a tenfold increase in data rate, reaching the multi-Gb/s levels [1]-[2]. Higher carrier frequency bands, e.g., 28 GHz, 38 GHz, 60 GHz, etc., stood out as potential candidates as the required available bandwidth increase beyond 1 GHz. Under the same fractional bandwidth (FBW), a wider available bandwidth comes with having a higher carrier frequency. Furthermore, higher frequency bands lead to other benefits such as smaller physical footprints for the antenna and circuit components. The high free space loss and extra loss due to the oxygen absorbance peak at the 60-GHz band limit its applications to short-range, multi-Gb/s, device-to-device communications. The 38-GHz band is a valid candidate for 5G communication receiver applications.

As often the first component after the receiving antenna, the gain and noise figure performances of the LNA dominate the signal-to-noise ratio (SNR) of the overall receiver. III-V compound semiconductor technologies are often used in LNA designs for the high gain and low noise performances. GaAs-based HEMT has been a stable and mature technology for microwave applications with relatively low cost for the performance it provides. LNA designs using GaAs-based HEMT processes have been reported for satellite communications and radio astronomy applications [3]-[8], in which high sensitivity and good noise performance of the receiver are required. In chapter 2, a Q-band LNA with source degeneration and RC-feedback techniques for a balanced gain, low noise, and wideband performance in 0.15-μm GaAs pHEMT will be introduced.

In recent years, the demand for high data rates in wireless communications has brought increasing interests towards millimeter-wave frequencies. The 60-GHz band has stood out thanks to its wide unlicensed band. A wide available bandwidth means that multi-Gb/s communication is

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achievable even under the most basic, spectrally inefficient modulation schemes such as on-off keying (OOK). This result in a transceiver system with low complexity and DC power consumption, which is well suited for the short-range, multi-Gb/s communication applications targeted at mobile devices [21]-[28].

Switching-amplifier configuration of an OOK modulator operates by switching the output amplifier on/off in accordance with the baseband data signal [21]-[23], [32]-[33]. Modulation and amplification are performed by the same circuit, which only consumes DC power at on-states. This result in a transmitter of low DC power consumption and complexity. Critical performances of switching-amplifier configuration modulators are output power, gain, on-off isolation, and maximum data rate. Cascode circuit is commonly used for the switching-amplifier configuration. Modulation is performed by switching the gate bias of the common-gate device. However, due to leakage of the devices, cascode-based modulators often suffers from low on-off isolation. For OOK transmitters, higher SNR at the receiver end can be achieved by either increasing the output power, or minimizing leakage at off-state while maintaining gain at on-state, i.e., increasing on-off isolation. With the former often leads to high DC power consumption, improvement in on-off isolation is commonly pursued [22]-[28], [32]-[36]. In chapter 3, a 60-GHz cascode-based OOK modulator design with transformer feedback technique in 90-nm CMOS will be introduced. The technique improves the output power, gain performances at on-state, and isolation performance at off-state.

Wireless communications in millimeter-wave frequencies gain many interests in recent years due to the large available bandwidth and therefore higher data rates [39]-[47], [50]. Wireless systems designed at W-band benefit from having smaller circuit footprints and antenna sizes, with the short wavelength also provides potentials for imaging applications in area such as bio-medical research. Advanced nanoscale technologies such as 28, 40, and 65-nm CMOS processes have the advantage of higher gain and f_{max}/f_T, which are especially critical in amplifier designs at millimeter-wave frequencies. However, shorter gate-lengths lead to lower breakdown voltages,

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which in turn limit the supply voltage. This poses challenges to PA designs in achieving high levels of output power. Power combining is widely used for increasing the output power under low supply voltages [47]-[50]. Due to the short wavelength at millimeter-wave frequencies, the phase difference between combining paths becomes highly sensitive to any physical asymmetry of the power combining structure. Phase difference between combining paths degrades the combined power, and therefore the amplifier efficiency.

Binary power combining uses transmission lines for the purposes of both in-phase power combining and impedance matching. A wideband performance can often be achieved with careful design of the transmission lines [44]-[46], [50]. However, a large transformation ratio between the optimal impedance of the devices and the load impedance leads to longer transmission lines, and therefore higher insertion losses. Furthermore, transmission lines often take up large layout footprint, even at millimeter-wave frequencies. Transformer-based power combining has stood out in millimeter-wave PA designs recently [39], [48]-[49]. Transformers also serves the purposes of both in-phase power combining and impedance matching, but in a much more compact layout footprint than transmission lines. Since a large impedance transformation ratio does not necessarily translate to a large insertion loss of the transformer, the technique is especially suited for multi-way, high output power PA designs. In chapter 3, a W-band PA with a transformer-based, four-way, radial-symmetric power combining structure adopted at the output for low insertion loss and matching imbalances in 65-nm CMOS will be introduced.

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1.2 Literature Surveys

1.2.1 Q-band LNA

The gain and noise figure are the most critical performances of a LNA design. III-V compound semiconductor technologies are often used in LNA designs for the high gain and low noise performances. LNA designs using GaAs-based HEMT processes have been reported for satellite communications and radio astronomy applications [21]-[26], in which high sensitivity and good noise performance of the receiver are required. Table 1.1 summarizes the previously reported K- and Q-band LNA designs.

The LNA in [21] uses π-type matching network and compensated matching to achieve wideband performance. The LNAs in [22]-[26], [29], [32] show great gain and noise performance due to process advantages in 0.1-μm GaAs pHEMT, GaAs mHEMT, and InP HEMT. The LNAs in [28] and [31] show gain and low noise performances, but are narrowband designs. The low noise medium power amplifier (LNMPA) in [30] shows good gain, low noise, and wideband performances, but requires high DC power consumption for the output power performance. The 90-nm CMOS LNA in [33] shows low DC power consumption, but gain and noise performances are still inferior to LNAs in III-V compound semiconductor technologies.

In chapter 3, the proposed LNA is designed in 0.15-μm GaAs pHEMT process for its excellent device performances and low loss characteristics of passive components. Source degeneration, RC-feedback, and π-type matching network are used for high gain, low noise, and wideband performances.

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Table 1.1. Previously Reported K- and Q-band LNA designs.

Ref.	Technology	Freq. (GHz)	FBW (%)	Gain (dB)	Noise Figure (dB)	P_{DC} (mW)	Area (mm^2)
[3]	0.15-μm GaAs pHEMT	28.5-50.5	56	23	3.8	62.6	2x1.5
[4]	0.1-μm GaAs pHEMT	18.5-30	47	29	2.1	27	2x1
[5]	0.1-μm GaAs pHEMT	27-45	50	25	2.9	9	2x1
[6]	50-nm GaAs mHEMT	25-60	84	27.5	1.85	60	2x1
[7]	0.15-μm GaAs mHEMT	27.3-50.7	60	23.1	3.7	88	2x2
[8]	0.15-μm GaAs mHEMT	37-53.2	36	32.5	3.21	152	2x1
	0.15-μm GaAs mHEMT	32-50	44	29.5	2.8	140	2x1
[9]	0.12-μm GaN HEMT	33-41	22	15	3	280	1x0.7
[10]	0.1-μm GaAs HEMT	43-45	4.5	28	2.9	24	3.6x1.8*
[11]	0.2-μm InP HEMT	23-49	72	11	2.5	10	2.3x1.5
[12]	0.15-μm GaAs pHEMT	24-40	50	24	2.1	520	1.5x2.8
[13]	0.15-μm GaN T-gate DHFET	42-47	11	22	3.5	140	2.5x1.3
[14]	0.1-μm GaAs pHEMT	18-43	82	21.6	2.3	140	2x1
[15]	90-nm CMOS	30-42	33	18	5	18	0.6x0.48

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1.2.2 60-GHz OOK Modulator

Table 1.2 summarizes the previously reported silicon-based OOK modulator designs. Three configurations of an OOK transmitter are commonly used. In a switching-oscillator configuration, the oscillator is switched on/off in accordance with the baseband data signal [29]-[30]. Since there is no carrier signal generated at off-states, the configuration exhibits decent on-off isolation. However, the finite response time of the oscillator limits the maximum data rate. In the second configuration, a switch-like modulator is followed by the output amplifier [31]. Carrier signal from the oscillator is modulated before feeding into the output amplifier. Muti-Gb/s data rates are achievable using circuit structures such as shunt switches. However, switch-like modulators often suffers from low on-off isolation. In addition, the insertion loss of switch-like modulators often requires a buffer amplifier for compensation, which leads to more DC power consumption and circuit components. The third configuration is of a switching-amplifier, in which the output amplifier is switched on/off in accordance with the baseband data signal [21]-[23], [32]-[33]. Critical performances of switching-amplifier configuration modulators are output power, gain, on-off isolation, and maximum data rate. Due to leakage of the devices, cascode-based modulators often suffers from low on-off isolation. Current-reuse and dual modulation techniques [22], [32] and data-dependent impedance cell [33] have been introduced to improve the on-off isolation of cascode-based modulators. However, the techniques in [22], [32], [33] all required two baseband data inputs, which increase the transmitter complexity and DC power consumption. Furthermore, the transmission lines used in [22], [32] occupy large layout footprint. Other configurations include differential LO cancelation [24]-[25] and Gilbert cell topology [26]-[27], both of which suffers from high conversion loss. In addition, bulk-driven modulation with the dual feedthrough cancelation technique [28] shows limited output power.

In chapter 3, the proposed OOK modulator adopts a transformer-feedback technique for improvements in output power, gain performances at on-state, and isolation performance at off-state.

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The use of transformer means a compact layout footprint is possible. The proposed OOK modulator requires only a single baseband data input. Therefore, the transmitter complexity and power consumption can be reduced for future applications.

Table 1.2. Previously reported CMOS OOK modulators.

Ref.	Technology	Freq. (GHz)	Gain (dB)	OP_{1dB} (dBm)	On-Off Isolation (dB)	Data Rate (Gbps)	P_{DC} (mW)
[22]	90-nm CMOS	60	9.1	5.1	24.3	10.7	21.6
[25]	90-nm CMOS	45	0	-	55	5.5	6
[28]	65-nm CMOS	60	1	-	30.5	16	5
[29]	0.13-μm CMOS	45-46	-	-	> 50	1	-
[31]	90-nm CMOS	60	-6.6	-	26.6	8	0
[32]	90-nm CMOS	60	9.9	1.5	28.4	2	14.4
[33]	0.18-μm BiCMOS	60	11.5	-1.5	48.0	2.5	8.1
[35]	0.25-μm BiCMOS	60	-1.1	-	36	20	54.6

1.2.3 W-band PA

The low breakdown voltages of advanced nanoscale technologies limit the supply voltage, and poses challenges to PA designs in achieving high levels of output power. Power combining techniques have been proposed to increase the output power of millimeter-wave PA designs. Different combining structures often make tradeoffs between bandwidth, insertion loss, and layout footprint. A wide bandwidth PA is useful for the high speed and wide bandwidth data communications. It is also versatile to be used as a general purpose PA for different kind of systems. Table 1.3 summarizes the previously reported silicon-based W-band PA designs.

Transformer-based power combining is used in [39], [41], and [43]. The PAs in [39], [43] use cascode-based driver stages and common-source output stages, and cascode circuits are used for all

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three stages in [41]. The PAs in [39], [41], [43] show good output power performances. As a tradeoff, cascode circuits provide high gain, but require higher bias voltage. In addition, the transformer-based power combining in [39], [41], [43] exhibit limited bandwidths. The PA in [42] uses slow-wave coplanar waveguide lines for reducing substrate loss and shorter line length during impedance matching. However, the layout footprint is still large for the output power performance it provides. The PA in [44] is of three stage common-source design. By selection of high-pass and low-pass matching networks using thin-film micro-strip lines, the PA show wideband performance with a high output power. The PAs in [45]-[46] uses transmission lines for multi-way power combining with impedance transformation, as described in detail in [50]. The PAs in [45]-[46] show good output power and wideband performances. The large impedance transformation ratios lead to long transmission lines, which have large insertion loss and layout footprint.

The PA in [47] consists of three stages, with a single-ended first stage driving a two-stage balanced amplifier. Balanced structure is implemented via 90° couplers to double the output power, and improves the PA return loss. Cascode circuits are used for all three stages for high gain. However, thin-film micro-strip lines for matching and 90° couplers occupies large layout footprint.

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Table 1.3. Previously reported W-band PA designs in CMOS processes.

Ref.	Technology	Frequency (GHz)	3dB BW (GHz)	Gain (dB)	P_{sat} (dBm)	OP_{1dB} (dBm)	PAE_{peak} (%)	Area (mm^2)
[39]	65-nm CMOS	108	16	14.1	14.8	11.6	9.4	0.322
[40]	65-nm CMOS	109	13	17.8	9.6	8.3	10.4	0.136
[41]	65-nm CMOS	94	21	13	14	10.3	4	0.24
[42]	65-nm CMOS	100	21	13	10	6	7.3	0.33
[43]	65-nm CMOS	100	17	13.4	13.8	11.2	9.4	0.205
[44]	65-nm CMOS	90	27	12	14.8	12.5	8.7	0.28
[45]	65-nm CMOS	90	25	12.5	18	16.8	9	0.82
[46]	65-nm CMOS	140	30	15	13.2	9.9	14.6	0.38
		150		16	12.2	7.6	12.1	
[47]	90-nm CMOS	100	18	15	10	6	5	0.4

1.3 Contributions

This thesis presents a Q-band LNA for 5G wireless communication receiver applications in 0.15-μm GaAs pHEMT, 60-GHz OOK modulator for short range wireless communications in 90-nm CMOS, and a W-band PA. The major contributions of these researches are described as follows.

1.3.1 Q-band LNA in 0.15-μm GaAs pHEMT

The Q-band LNA is designed and realized in 0.15-μm GaAs pHEMT. The LNA consists of three common-source stages. Source degeneration is adopted at the first stage for a balanced noise and gain performance, which is critical to the performance of the LNA. RC-feedback is adopted at

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the latter two stages for its wideband characteristics. In addition, π-type matching networks are used at the third stage for wideband impedance matching. Device modeling issues caused disagreement between simulation and measurement results in the original LNA design. Corrections are proposed and applied to the simulation setups of a modified LNA design for a second tape-out using the same process. Agreement between measurement and simulation results of the modified LNA verifies the proposed corrections for applications in future designs. The LNA shows peak gain of 23.3 dB at 33.1 GHz, and the 3-dB bandwidth is 15.3 GHz from 24.7 to 40.0 GHz with average gain of 22.2 dB. The gain is 21.5 dB at 38 GHz, and has flatness of 22.3 ± 1 dB from 25.7 to 37.6 GHz. The input return loss is above 15 dB from 37.2 to 40.4 GHz, and the output return loss is above 15 dB from 34.4 to 39.4 GHz. The noise figure is below 3dB from 27.9 to 40.0 GHz. The noise figure has minimum of 2.2dB at 31.5 GHz, and average of 2.6 dB from 26 to 40 GHz.

1.3.2 60-GHz OOK Modulator in 90-nm CMOS

The 60-GHz OOK modulator is designed and realized in 90-nm CMOS. Based on a cascode circuit, the modulator combines the functions of modulation and output amplification, and only consumes DC power at on-states. This result in a transmitter of low DC power consumption and complexity. A transformer-feedback is proposed for cascode-based modulators for improvements in output power, gain performances at on-state, and isolation performance at off-state. A data input network is designed to achieve low RC time constant and avoids distortion of the baseband data signal. With the proposed transformer feedback technique, the modulator achieves an OP_{1dB} of 7.0 dBm, gain of 10.2 dB, and on-off isolation of 45.4 dB at 60 GHz. For OOK modulation, data rates of up to 10 Gb/s has been measured. The modulator has compact layout footprint measured at 471 x 519 μm^2 with RF and DC pads included.

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1.3.3 Common-mode stability of W-band PA in 65-nm CMOS

The W-band PA is designed and realized in 65-nm CMOS. The PA consists of three common-source stages with total gate-periphery ratio of 1:2:4. To achieve the targeted output power performance under the process limited supply voltage, four-way transformer-based power combining is adopted at the output. With single-to-differential transformers at the input and differential-to-single transformers at the output, the PA operates in differential mode internally. Neutralization technique can therefore be implemented via cross-coupled capacitors in order to improve the device gain and stability in differential mode. All impedance matching and power-combining/splitting are performed via transformers, which are carefully designed to have the self-resonant frequencies above the working frequencies at W-band.

Common-mode instability were discovered during measurement, and recreated in simulation through extensive bias-line and common-mode stability analyses. Modifications to the transformers are proposed to eliminate the common-mode instabilities, without altering the matching conditions in differential mode. The modification proved successful in the second tape-out. EM modeling issues of transformers at high frequencies of W-band is discussed. Despite the modeling issue, the proposed PA shows decent gain performance of 15.3 dB at 98 GHz with a 12 GHz 3-dB bandwidth. Large-signal performances is only comparable to previous works, with an OP_{1dB} of 8.2 dBm, P_{sat} of 11.2 dBm, PAE_{peak} of 4.2% at 98 GHz, and OP_{1dB} above 5.7 dBm across 90 to 104 GHz with peak OP_{1dB} of 8.2 dBm at 98 GHz.

1.4 Thesis Organization

The thesis is organized as follows.

In chapter 2, a Q-band LNA for fifth-generation (5G) communication applications in 0.15-μm GaAs pHEMT is designed, measured, and discussed. The LNA consists of three common-source

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stages, with source degeneration and RC-feedback techniques adopted at different stages. RC-feedback and π-type matching networks are adopted at the latter stages for wideband performance and gain flatness. Device modeling in simulation are discovered and analyzed. Corrections to the simulation setups are proposed and verified through experimental results in a second tape-out using the same process. This chapter describes the design procedure of the LNA, analyses and corrections applied to the simulation setups, and the experimental results.

In chapter 3, a 60-GHz OOK modulator for short range wireless communications in 90-nm CMOS is designed, measured, and discussed. Based on a cascode circuit, the modulator combines the functions of modulation and output amplification of an OOK transmitter. A transformer-feedback technique is proposed for cacode-based modulators to improve the output power, gain performances at on-state, and isolation performance at off-state. This chapter describes the OOK modulation schemes, analyses on the transformer-feedback technique, design procedure of the modulator, and the experimental results.

In chapter 4, a W-band PA in 65-nm CMOS is designed, measured, and discussed. A transformer-based radial-symmetric power combining structure is adopted at the output for low insertion loss and matching imbalances. Common-mode instabilities were observed and analyzed after the first tape-out. Modifications to the transformers are proposed to eliminate the common-mode instabilities, without altering the matching conditions in differential mode. The modifications proved successful in the second tape-out. Modeling issue of high frequency transformer designs is also discussed. This chapter describes the design procedure of the PA, analyses and discussions on common-mode instabilities, corrections to the transformers, and the experimental results.

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Chapter 2 A Q-band Low Noise Amplifier for Fifth-Generation Wireless Communication Receiver Applications in 0.15-μm GaAs pHEMT

In this chapter, a Q-band low noise amplifier (LNA) for fifth-generation (5G) communication applications designed and realized in 0.15-μm GaAs pHEMT is presented. The LNA consists of three common-source stages. Source degeneration is adopted at the first stage for a balanced noise and gain performance, which is critical to the performance of the LNA. RC-feedback is adopted at the latter two stages for its wideband characteristics. In addition, π-type matching networks are used at the third stage for wideband impedance matching. Device modeling issues caused disagreement between simulation and measurement results in the original LNA design. Corrections are proposed and applied to the simulation setups of a modified LNA design for a second tape-out. Agreement between measurement and simulation results of the modified LNA verifies the proposed corrections. The LNA exhibits wide 3-dB bandwidth from 24.7 to 40.0 GHz, with average gain of 22.2 dB. The noise figure is below 3 dB from 27.9 to 40.0 GHz, with average of 2.6 dB from 26 to 40 GHz.

2.1 Introduction

With the ever-increasing demands for high-speed wireless applications, the fifth generation (5G) wireless communication has been the focus of interests in recent years. Compared to the current fourth generation long-term evolution (4G-LTE) configuration, 5G promises at least a tenfold increase in data rate, reaching the multi-Gb/s levels [1]-[2]. Higher carrier frequency bands, e.g., 28 GHz, 38 GHz, 60 GHz, etc., stood out as potential candidates as the required available bandwidth increase beyond 1 GHz. Under the same fractional bandwidth (FBW), a wider available bandwidth comes with having a higher carrier frequency. However, the free space loss also increases with frequency. In a communication distance of 150 meters, the free space loss at the 38-GHz band is around 2.7 dB higher than 28-GHz. Nevertheless, the higher carrier frequencies lead to benefits such as smaller physical footprints for the antenna and circuit components, and a

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wider available bandwidth. On the other hand, the high free space loss and extra loss due to the oxygen absorbance peak at the 60-GHz band limit its applications to short-range, multi-Gb/s, device-to-device communications. The 38-GHz band is therefore chosen for the proposed LNA design for 5G communication receiver applications.

As often the first component after the receiving antenna, the gain and noise figure performances of the LNA dominate the signal-to-noise ratio (SNR) of the overall receiver. The gain should be high enough in order to mitigate the noise contributed by the latter components in the receiver. The noise figure should be low enough, as it will dominate the overall noise figure of the receiver. III-V compound semiconductor technologies are commonly used in LNA designs for the high gain and low noise performances. In spite the fact that InP-based HEMT devices exhibit better performances at millimeter-wave frequencies than GaAs-based HEMT devices, the latter has been a stable and mature technology for microwave applications with relatively low cost for the performance. LNA designs using GaAs-based HEMT processes have been reported for satellite communications and radio astronomy applications [3]-[8], in which high sensitivity and good noise performance of the receiver are required.

The 0.15-μm GaAs pHEMT process is chosen for the proposed Q-band LNA design for its excellent device performances and low loss characteristics of passive components. Table 2.1 lists the target performances of the proposed Q-band LNA. From 37.5 to 38.5 GHz, the gain of the LNA is required to be larger than 20 dB with in/output return losses better than 10/12 dB. The noise figure should be lower than 3 dB in the desired frequency band. The die size is limited to 1.5 x 1 mm^2 for better system integration.

Table 2.1. Target performances for the proposed Q-band LNA.

Frequency	**Gain**	**Noise Figure**	**In/Output Return Loss**	**Die Size**
37.5 – 38.5 GHz	> 20 dB	< 3 dB	> 10 / > 12 dB	1.5 x 1 mm^2

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2.2 Circuit Design

2.2.1 Bias Condition and Device Selection

The proposed Q-band LNA is designed in 0.15-μm GaAs pHEMT process (enhancement mode, PE15-00) provided by WIN Semiconductors. The noise measurement data of the devices provided by the foundry have a fixed drain-to-source voltage (V_{DS}) of 2.0 V, with varying current density (I_{DS}/gate-periphery) from 50 to 250 mA/mm. For accurate modeling of the device noise parameters in simulation, all V_{DS}'s in the proposed LNA is therefore fixed to 2.0 V. The scalable large-signal device model is used for DC simulation and initial assessment of small-signal performances. Foundry-provided small-signal measurement data of the devices is used later in the design process for more accurate modeling. Note that the simulation results shown in section 2.2.1 are performed using the CPW-configuration devices purely for demonstration purposes. Similar results can be attained using the MS-configuration devices.

Fig. 2.1 shows the simulated DC-IV curves of the device with gate-periphery of 2f x 25 μm. In order to have a low DC power consumption, four of the smallest device gate-peripheries available, i.e., 2f x 25 μm, 2f x 50 μm, 4f x 25 μm, and 4f x 50 μm, are nominated for comparison. Fig. 2.2 shows the simulated device g_m and NF_{min} versus the gate-to-source voltage (V_{GS}), and Fig. 2.3 shows the device g_m and I_{DS} versus V_{GS}. The device NF_{min} is the lowest at around V_{GS} = 0.55 V regardless of gate-periphery, i.e., at around the same current density for different gate-peripheries. At V_{GS} = 0.6 V, the device NF_{min} is less than 0.1dB higher than the lowest point, with 10% higher g_m. Considering the tradeoff between device DC power consumption, gain and noise performance, V_{GS} is set to 0.6 V. As can be seen in Fig. 2.3, the I_{DS} at V_{GS} = 0.6 V is around 50% of the I_{DS} at g_m peak, which is consistent with the experience in previous LNA designs [16].

Noise and small-signal performances of different device gate-peripheries are then compared under the selected bias condition of [V_{GS}, V_{DS}] = [0.6 V, 2.0 V]. Fig. 2.4 shows the simulated

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MSG/MAG and stability factor. Smaller total gate-periphery results in higher gain but lower stability. Device with the smallest gate-periphery of 2f x 25 μm has the highest MSG/MAG, but is potentially unstable, i.e., stability factor less than 1, at 38 GHz. Additional measures must therefore be adopted in order to stabilize the device if the 2f x 25 μm gate-periphery is to be used. Fig. 2.5 shows the simulated device NF_{min} from 26 to 40 GHz. The 2f x 25 μm and 4f x 25 μm devices have the lowest NF_{min}, with only small differences less than 0.1 dB from 26 to 40 GHz. Fig. 2.6 shows the input impedance for optimal noise matching (Z_{opt}) from 30 to 40 GHz. At around 38 GHz, the Z_{opt} of the 2f x 25 μm device is the closest to 50 Ω, which decreases the design difficulty and the impedance transformation ratio of the input matching network. A larger impedance transformation ratio requires longer transmission lines for matching, which lead to a larger insertion loss of the matching network. Insertion loss of the input matching network degrades both the gain and noise figure of the first stage, which are critical in LNA designs. Thus, considering all the performance comparisons mentioned above, the 2f x 25 μm device is selected for the proposed LNA design because of its well-suited performance and low DC power consumption.

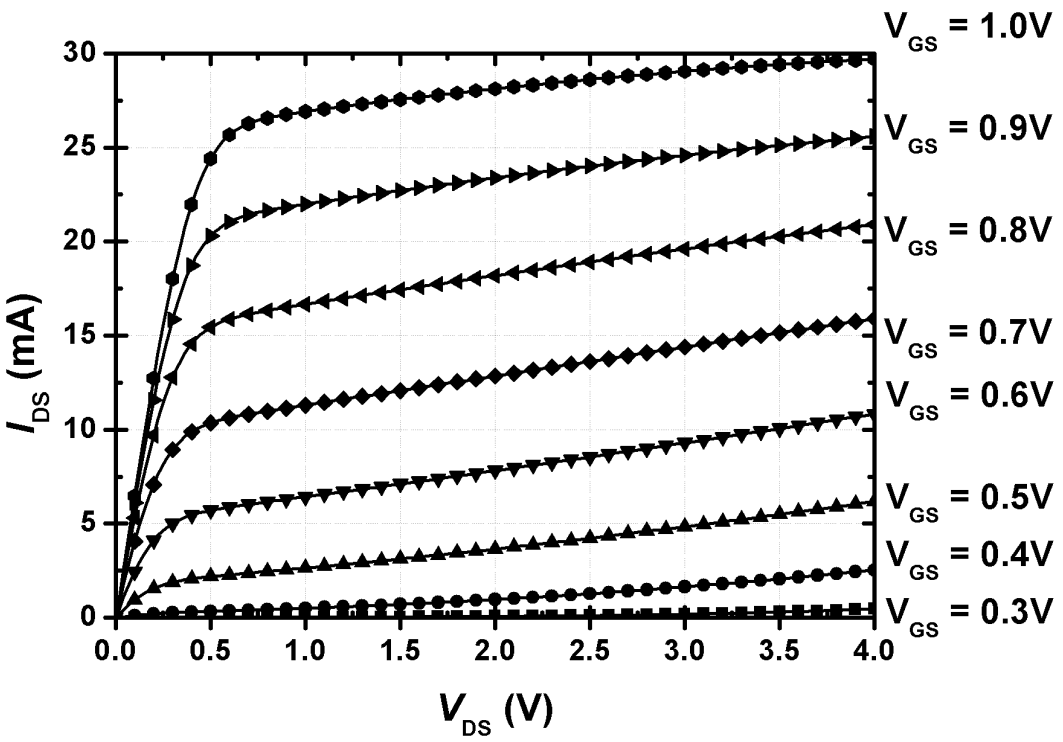

Fig. 2.1. Simulated DC-IV curves of the device with gate periphery of 2f x 25 μm.

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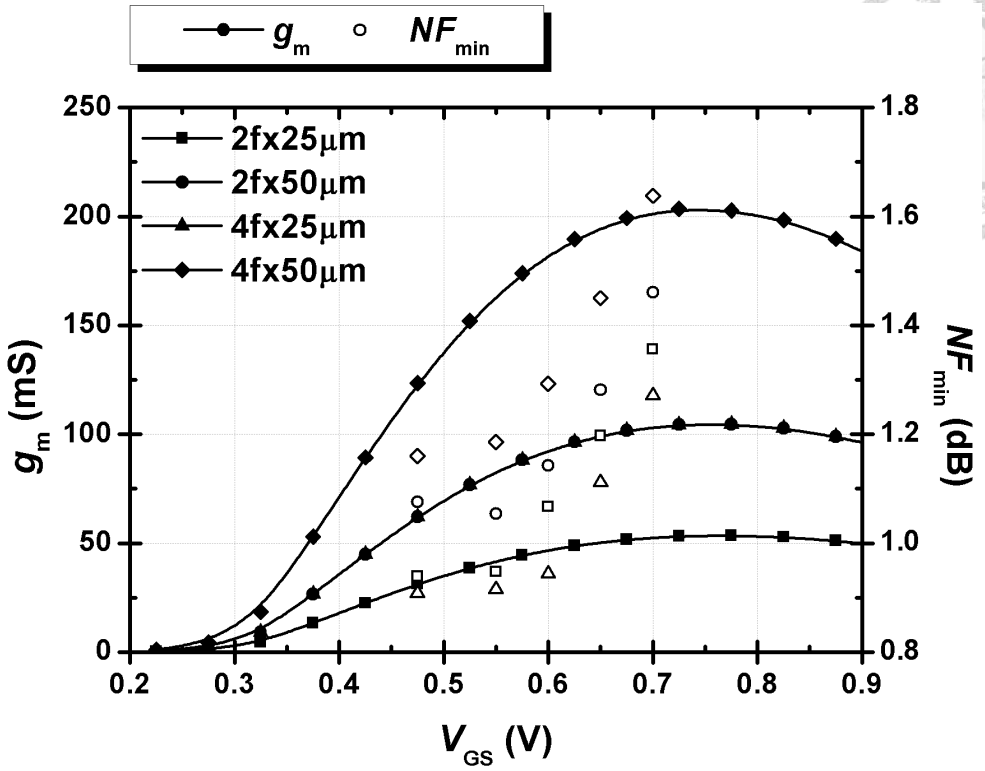

Fig. 2.2. Simulated g_m and NF_{min} of the devices with different gate-periphery configurations versus V_{GS} at V_{DS} = 2.0 V.

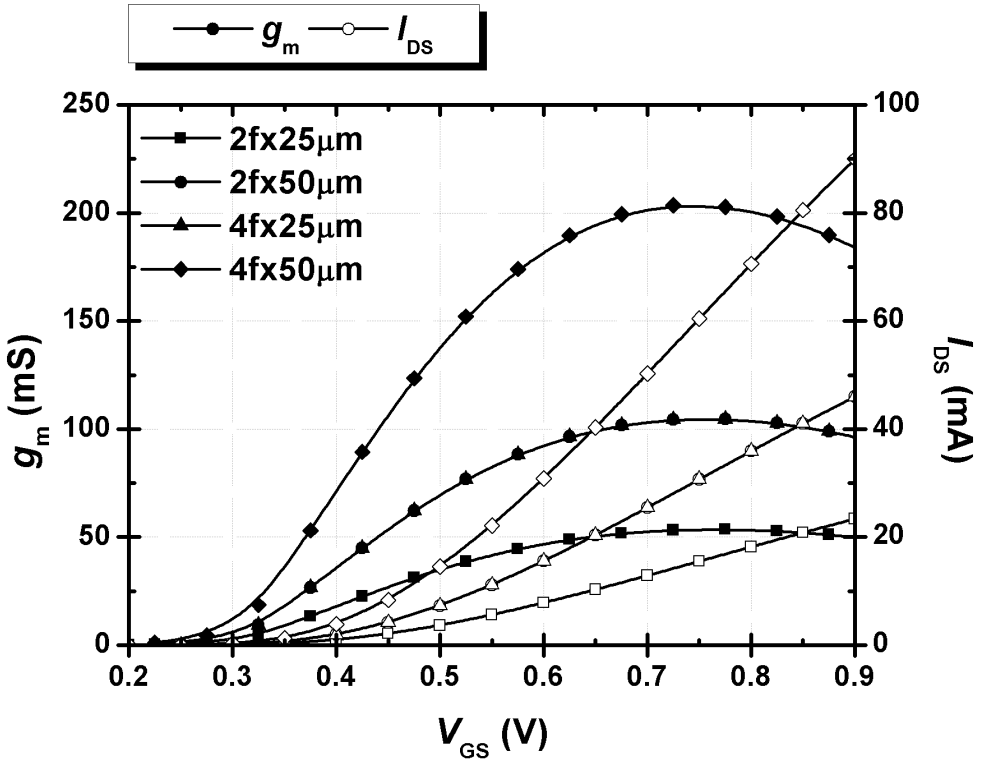

Fig. 2.3. Simulated g_m and I_{DS} of the devices with different gate-periphery configurations versus V_{GS} at V_{DS} = 2.0 V.

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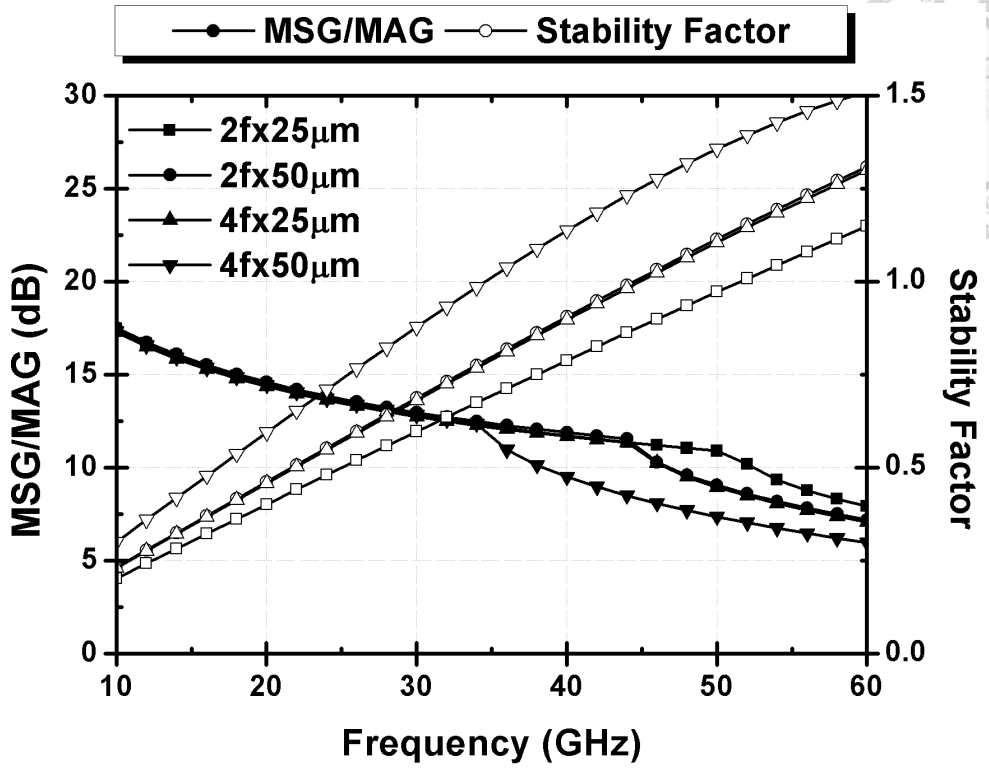

Fig. 2.4. Simulated MSG/MAG and stability factor of the devices with different gate-periphery configurations at [V_{GS}, V_{DS}] = [0.6 V, 2.0 V].

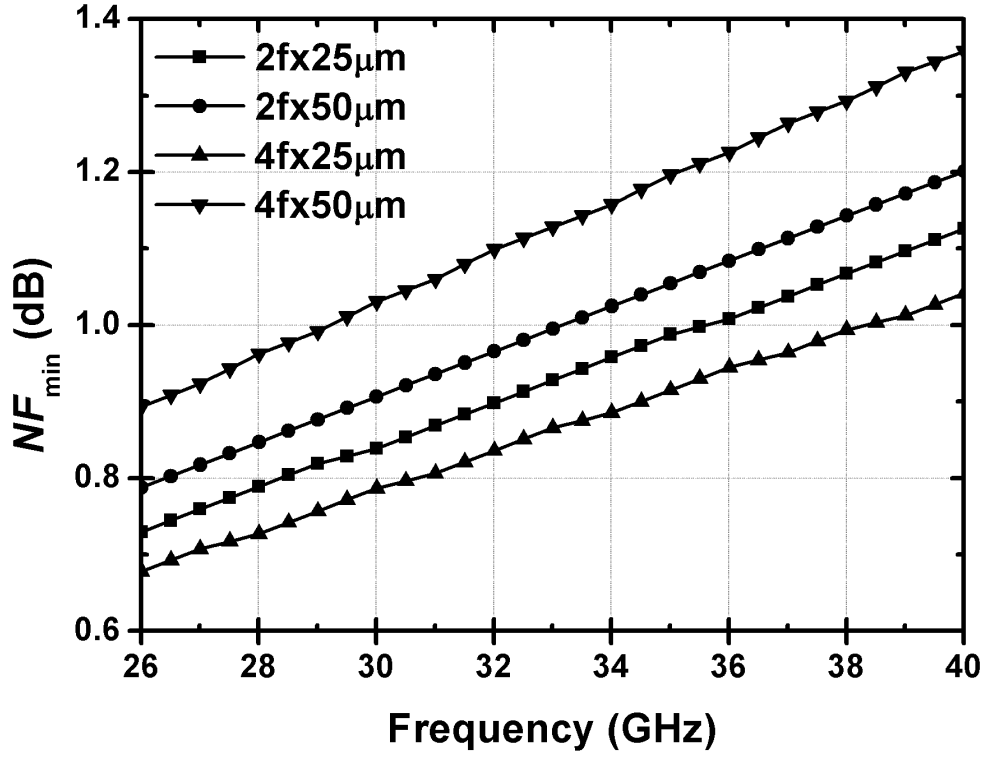

Fig. 2.5. Simulated NF_{min} of the devices with different gate-periphery configurations at [V_{GS}, V_{DS}] = [0.6 V, 2.0 V].

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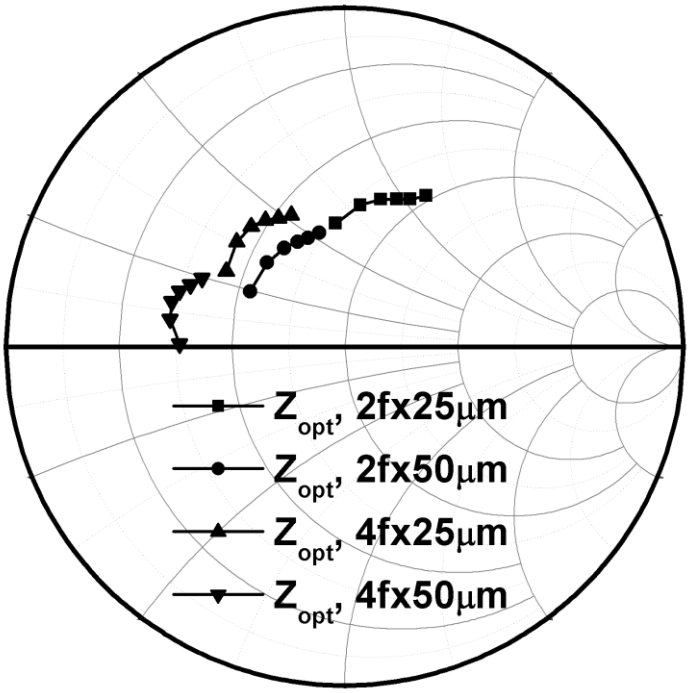

Fig. 2.6. Simulated Z_{opt} of the devices with different gate-periphery configurations at [V_{GS}, V_{DS}] = [0.6 V, 2.0 V].

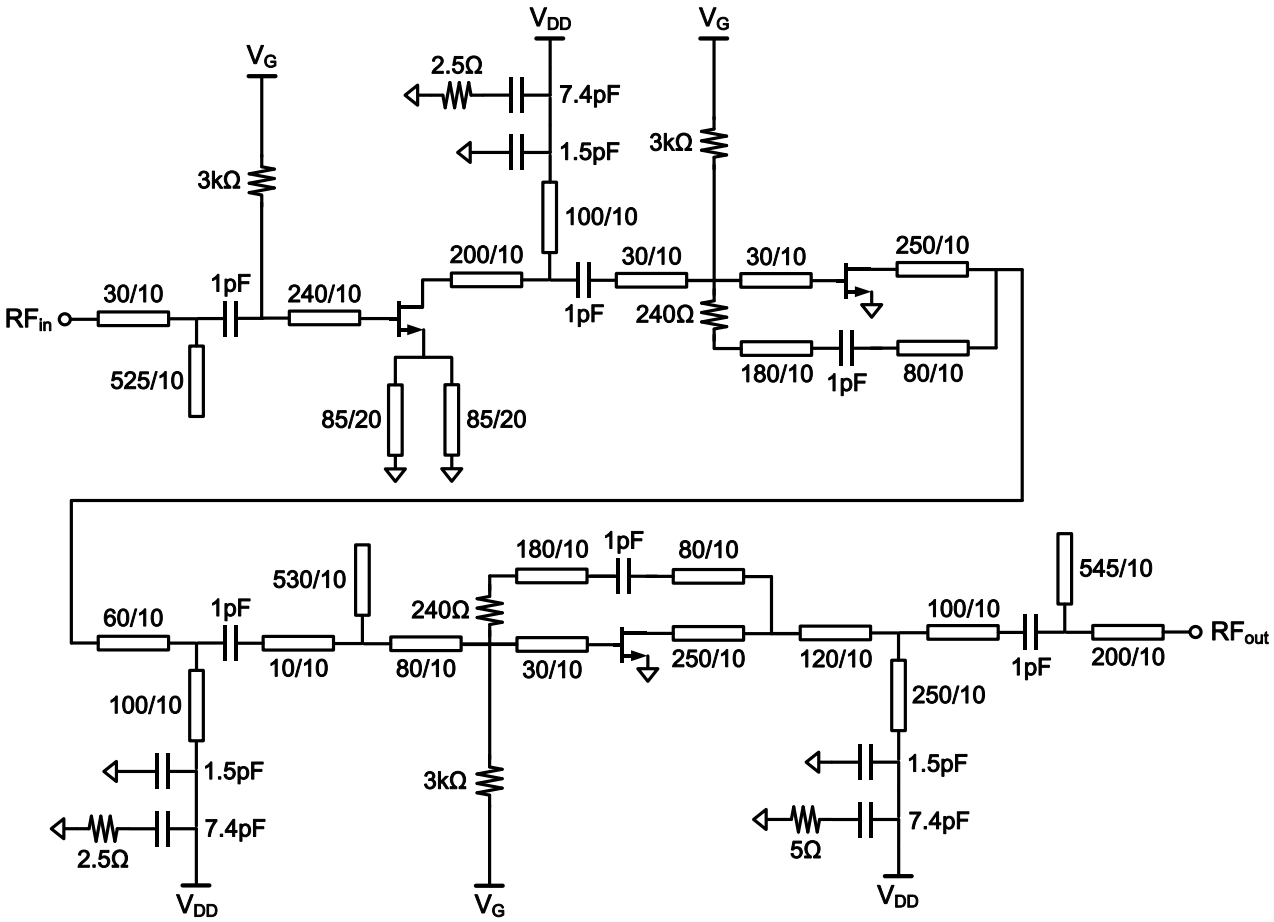

Fig. 2.7. Schematic of the proposed Q-band LNA.

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2.2.2 First Stage Design

Fig. 2.7 shows the schematic of the proposed Q-band LNA design. In an amplifier circuit with cascaded stages (or a system with cascaded components), the noise figure of amplifier circuit (or the overall system) can be expressed as

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \ldots \quad , \tag{2.1}$$

in which NF_n and G_n denote the noise figure and gain of the number *n* amplifier stage (or system component). Thus, the noise figure of an LNA design depends heavily on the noise figure and gain performances of its first stage. As mentioned in the previous section, additional measures are required to stabilize the selected 2f x 25 μm device. Source degeneration technique is known for its ability of narrowing the difference between input impedances for optimal noise (Z_{opt}) and gain ($Z_{in,conj}$) performances [17]. In other words, compromise in gain performance can be minimized when input is matched for optimal noise performance. Furthermore, an matching impedance closer to $Z_{in,conj}$ also translates to a better input return loss. For a symmetric layout, two identical transmission lines (TL_{deg}) terminated with backside-vias are used for source degeneration on CPW-configuration devices. Since the width of the TL_{deg}'s makes little difference to the device characteristics, the line width is set to 20 μm, same as the source metal width of the 2f x 25 μm device. Backside-vias at the end of the TL_{deg}'s provides source grounding for the device. The effective inductance of the backside-via model provided by the foundry is compared and verified with EM simulation.

Fig. 2.8 shows the simulated MSG/MAG and stability factor of the 2f x 25μm device with different lengths of the TL_{deg}'s ranging from 35 to 135 μm. The device is stabilized, i.e., stability factor ≥ 1, at 38-GHz for line lengths ≥ 85μm. The device MSG/MAG at 38 GHz for line length of 85 μm is 10dB and decreases as the length increases. Fig. 2.9 shows the simulated NF_{min} of the 2f x 25μm device with different lengths of the TL_{deg}'s. Device NF_{min} with different line lengths are

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nearly identical, which is to be expected as NF_{min} is only related to the device current and operation frequency. Fig. 2.10 shows the simulated device Z_{opt} and $Z_{in,conj}$ with different lengths of the TL_{deg}'s from 32 to 40 GHz. As can be seen, $Z_{in,conj}$ becomes closer to Z_{opt} and the difference between Z_{opt} and $Z_{in,conj}$ narrows as the line length increases. As mentioned above, this minimize the compromise in gain performance and help for a better input return loss, when the input is matched for optimal noise performance. Thus, considering all the performance comparisons mentioned above, a line length between 85 to 135 μm is to be selected. Since there is little to no difference in device NF_{min} and the difference in $Z_{in,conj}$ between line lengths of 85 μm and 135 μm is only minor, line length of 85 um with the highest MSG/MAG within the 85 to 135 μm range is the obvious choice for the maximum gain performance of the first stage.

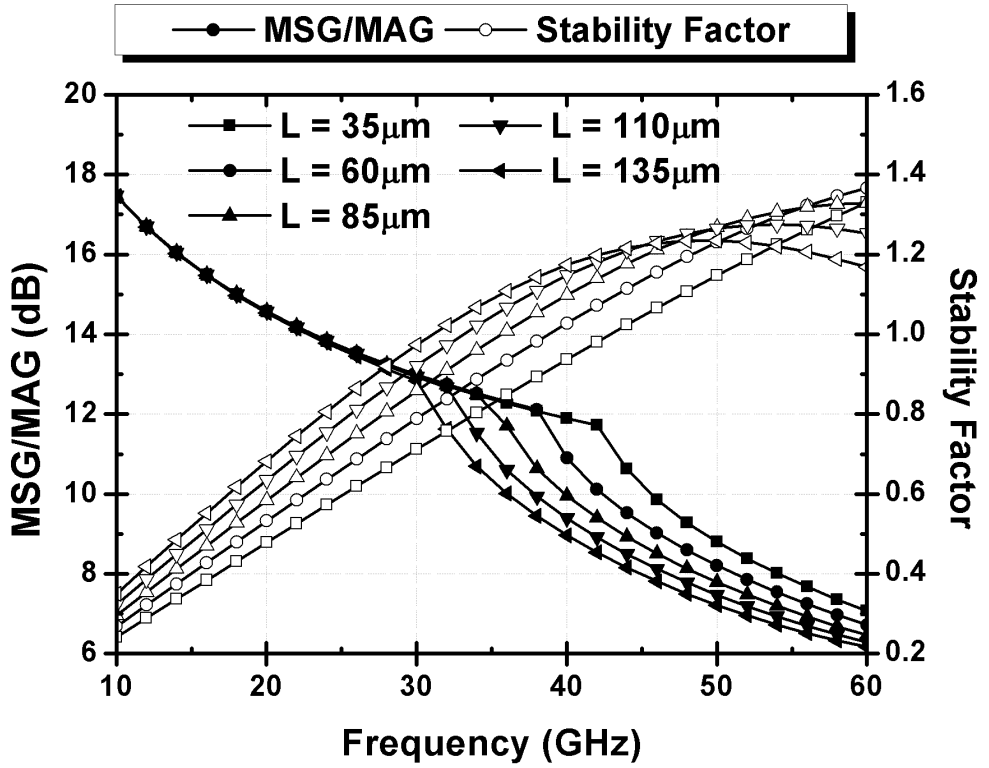

Fig. 2.8. Simulated MSG/MAG and stability factor of the 2f x 25 μm device with different lengths of TL_{deg}'s.

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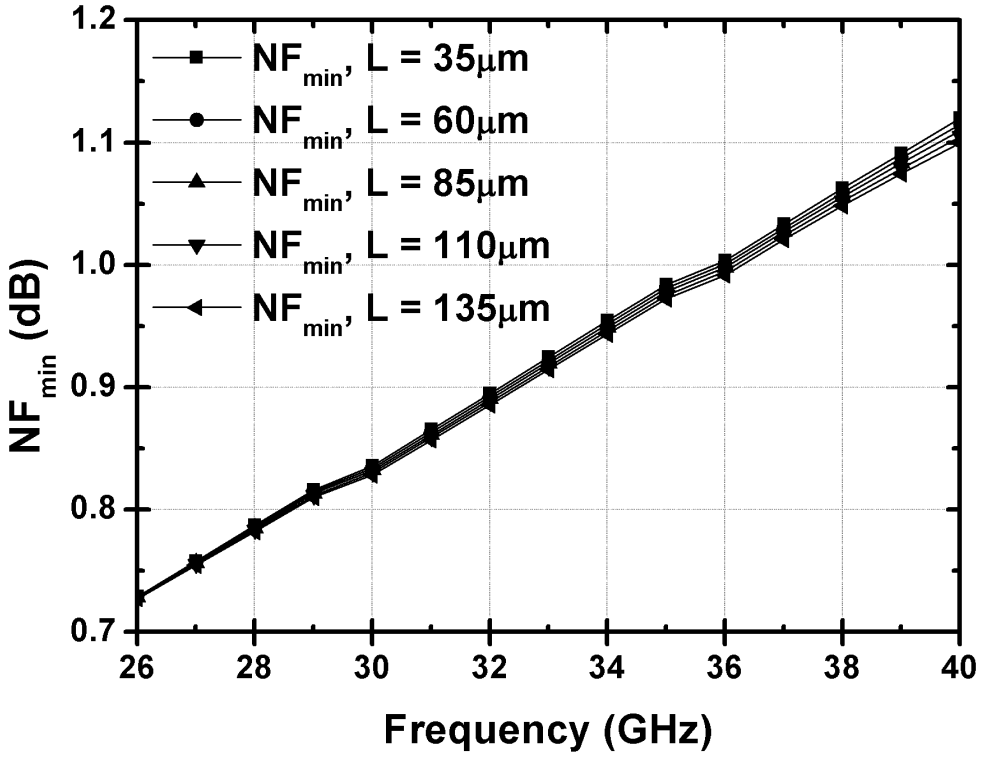

Fig. 2.9. Simulated NF_{min} of the 2f x 25 μm device with different lengths of TL_{deg}'s.

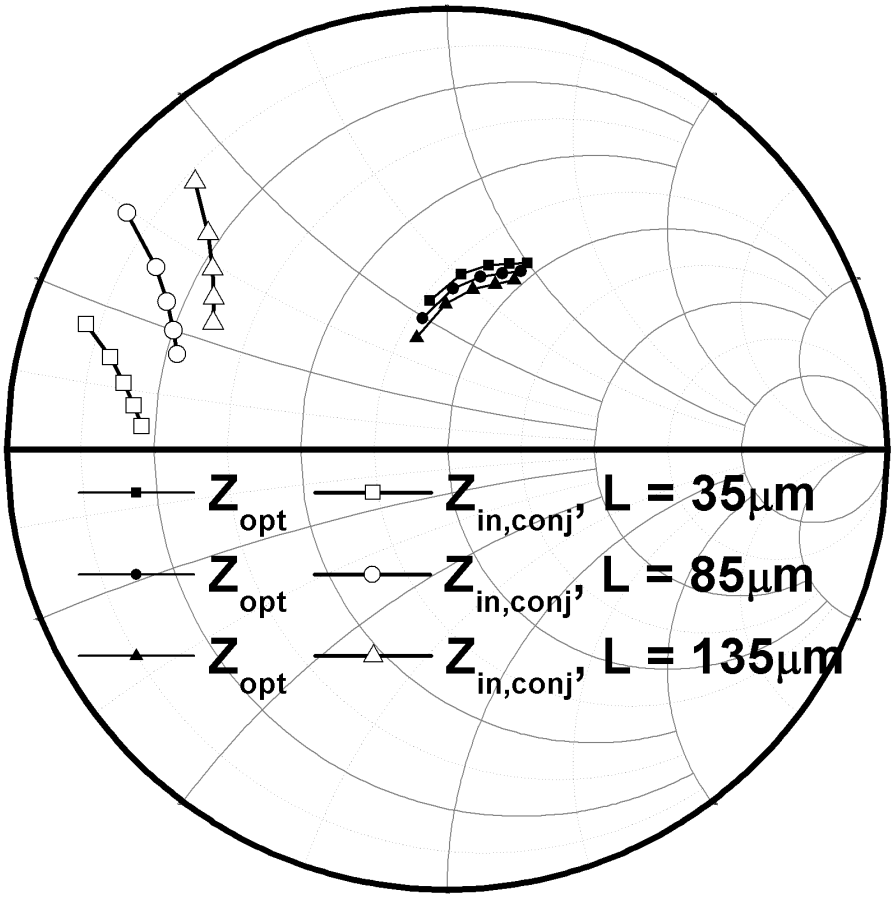

Fig. 2.10. Simulated Z_{opt} and $Z_{in,conj}$ of the 2f x 25μm device with different lengths of TL_{deg}'s.

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The input of the first stage is matched for optimal noise performance. As shown in Fig. 2.7, a T-type matching network is used for transferring the source impedance Z_S = 50 Ω to Z_{opt} of the first stage. The T-type input matching network consists of two series transmission lines and an open stub. The transmission lines are realized using double metal layers, i.e., metal 1 and 2 combined with via, in the 0.15-μm GaAs pHEMT process for lower insertion loss. Post-EM simulations of the first stage complete with the input matching network are performed with ideal output conjugate termination. Fig. 2.11 and 3.12 shows the simulated *S*-parameters and noise figure, respectively. The gain is 8.7 dB at 38 GHz, which is 1.9 dB lower than the device MSG/MAG. The input return loss is 13.7 dB at 38 GHz. The noise figure is 1.7 dB at 38 GHz, which is 0.6 dB higher than the device NF_{min}. Considering that the loss of the input matching network is around 0.4 dB at 38 GHz, the simulation results of the first stage indicates a well-designed noise matching and little compromise in gain and input return loss by adopting source degeneration. Note that MAG/MSG is used to evaluate the 0.4 dB loss of the passive input matching network at 38 GHz under matched conditions, i.e., excluding mismatch loss.

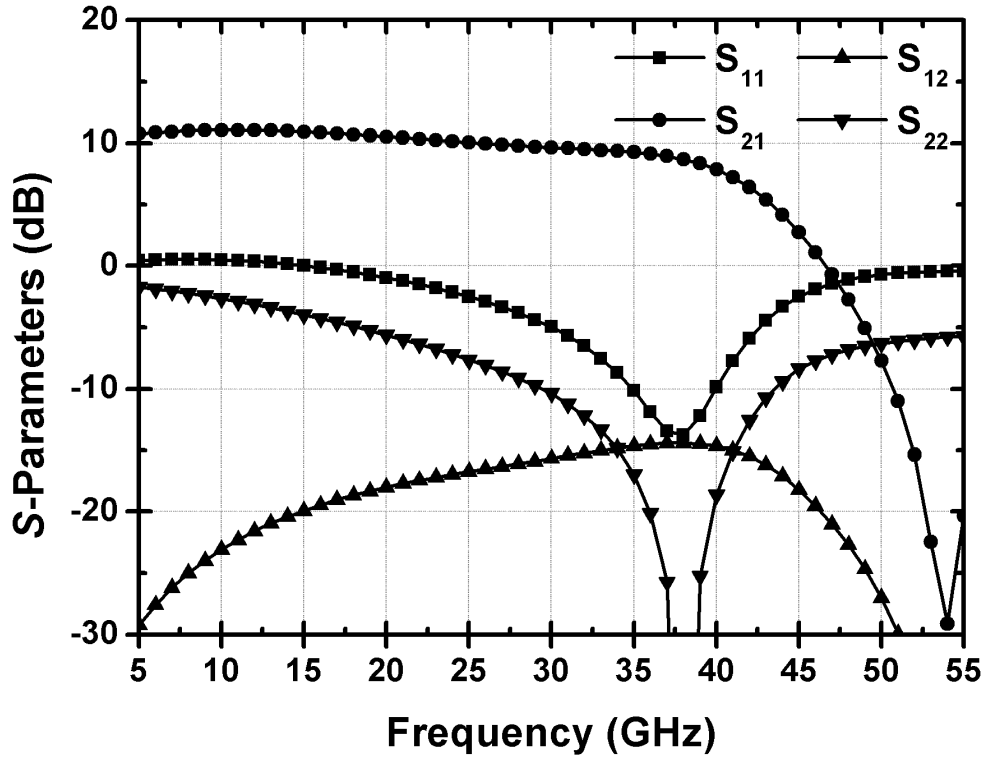

Fig. 2.11. Simulated *S*-parameters of the first stage complete with the input matching network.

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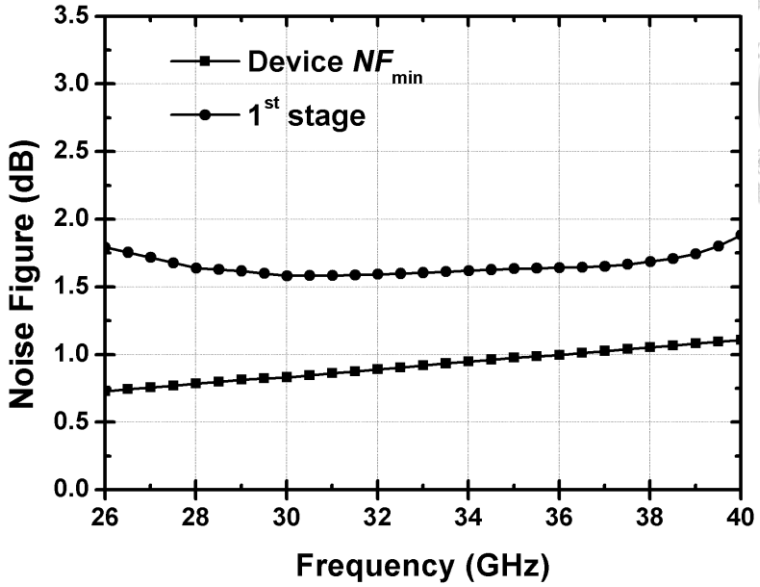

Fig. 2.12. Simulated noise figure of the first stage complete with the input matching network.

2.2.3 Second and Third Stage Design with Wideband Performance

From the simulated gain of 8.7 dB at 38 GHz provided by the first stage, an extra two common-source stages with the 2f x 25 μm device are required to achieve the target gain performance of 20 dB. From (2.1), the 8.7 dB gain of the first stage mitigates the increase in overall noise figure in adding the latter two stages. Therefore, impedance matching for optimal gain performance, i.e., simultaneous conjugate matching, is used at the latter two stages instead of noise performance. For stabilizing the 2f x 25 μm device, RC-feedback technique is adopted at the latter two stages for its wideband characteristics [18]-[19]. Fig. 2.13 shows the simulated MSG/MAG and stability factor of the 2f x 25 μm device with and without RC-feedback, in which the resistance and capacitance are 240 Ω and 1 pF, respectively. Note that MS-configuration of the 2f x 25 μm devices are used with RC-feedback, and additional micro-strip lines are required to form the feedback structure due to the physical layout of the device. The effect of the micro-strip lines are taken into account and modeled through EM simulation. The technique provides a much flatter MSG/MAG response around 38 GHz in addition to stabilizing the device. Note that despite the increase in stability factor, the device with RC-feedback is still potentially unstable above 33 GHz. Additional care is required during impedance matching to ensure no source/load impedance causes instability.

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Fig. 2.14 shows the simulated NF_{min} of the 2f x 25 μm device with and without RC-feedback. The device NF_{min} is 1.1 dB higher at 38 GHz with RC-feedback. Nevertheless, higher NF_{min} at the second stage is mitigated by the 8.7 dB gain provided by the first stage, and even more so at the third stage by the gain of the first two stages. Thus, the benefit of a wideband performance is considered more suited for this design.

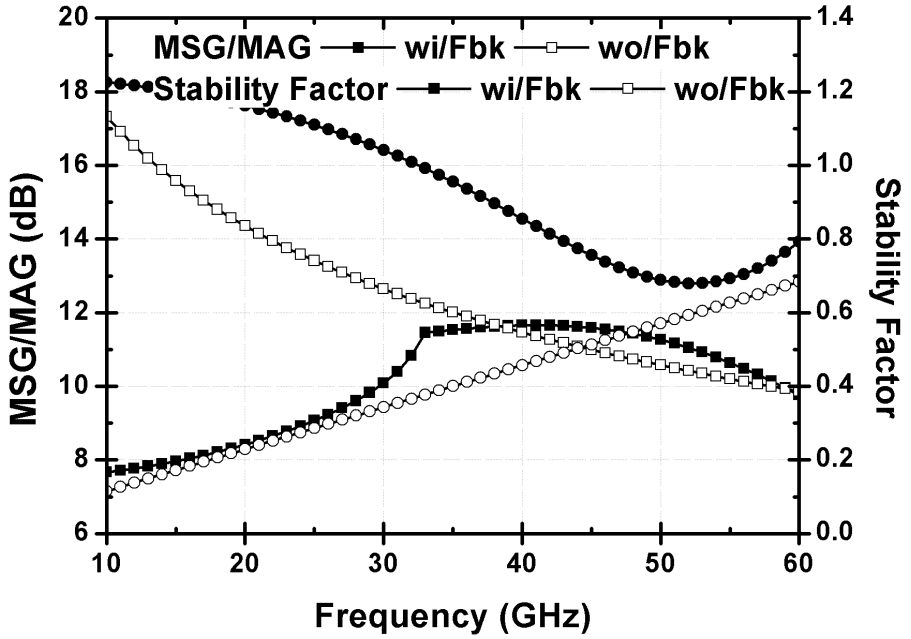

Fig. 2.13. Simulated MSG/MAG and stability factor of the 2f x 25 μm device with/without the proposed RC-feedback.

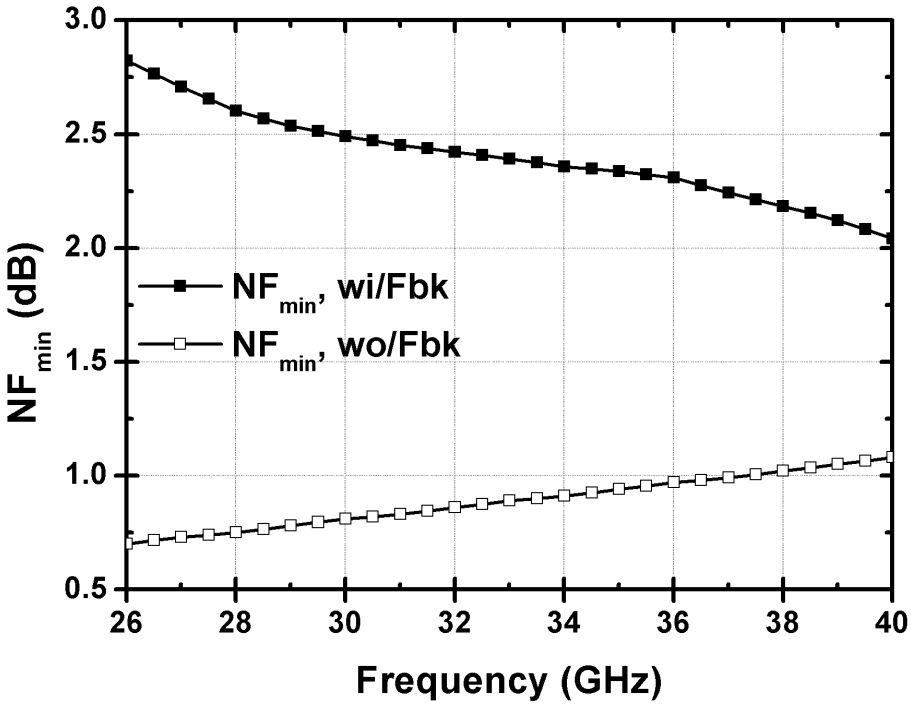

Fig. 2.14. Simulated NF_{min} of the 2f x 25 μm device with/without the proposed RC-feedback.

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As shown in Fig. 2.7, a T-type matching network is used for the inter-stage matching between the first and second stages, transferring the output impedance of the first stage Z_{out1} to $Z_{in2,conj}$. The T-type input matching network consists of two series transmission lines and a short stub. The transmission lines are realized using double metal layers in the 0.15-μm GaAs pHEMT process for lower insertion loss. Post-EM simulations of the first and second stages complete with the input and inter-stage matching networks are performed with ideal output conjugate termination. Fig. 2.15 and 3.16 shows the simulated *S*-parameters and noise figure, respectively. A wide 3-dB bandwidth of 17 GHz with good flatness is achieved. The gain is 19.4 dB at 38 GHz, which is 10.6 dB higher than the first stage. The noise figure is 2.0 dB at 38 GHz, which is 0.3 dB higher than the first stage. Considering that the loss of the inter-stage matching network is around 0.5 dB at 38 GHz, the simulation results stage indicates a well-designed gain matching and decent wideband performance by adopting RC-feedback. Note that MAG/MSG is used to evaluate the 0.5 dB loss of the passive inter-stage matching network at 38 GHz under matched conditions, i.e., excluding mismatch loss.

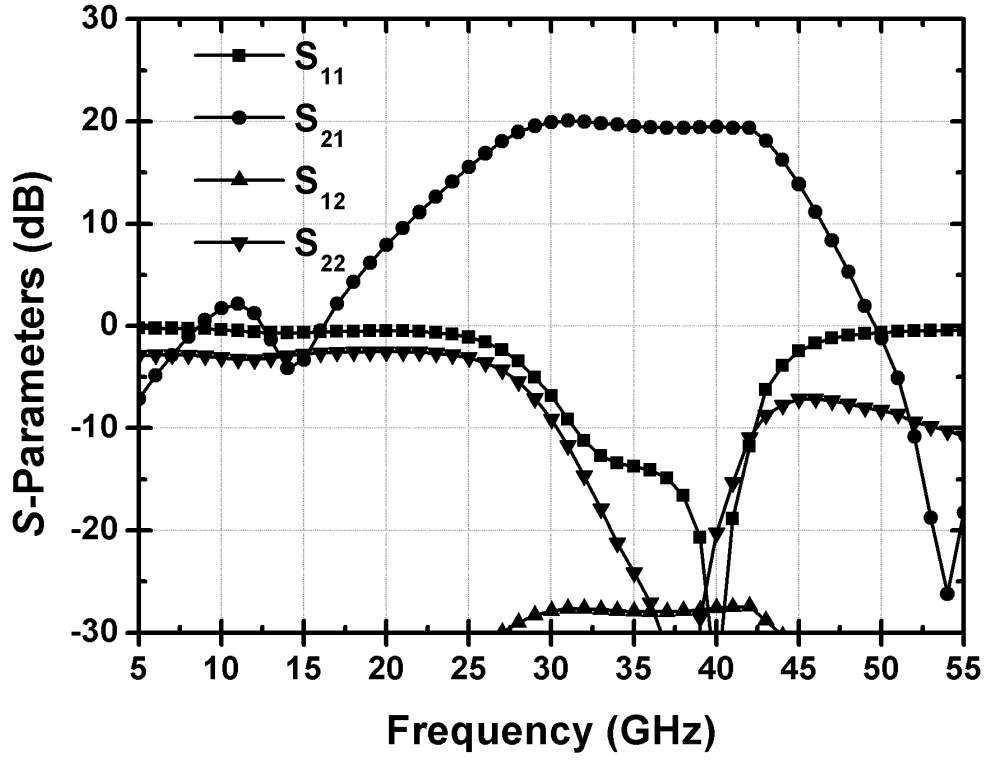

Fig. 2.15. Simulated *S*-parameters of the first and second stages complete with the input and inter-stage matching networks.

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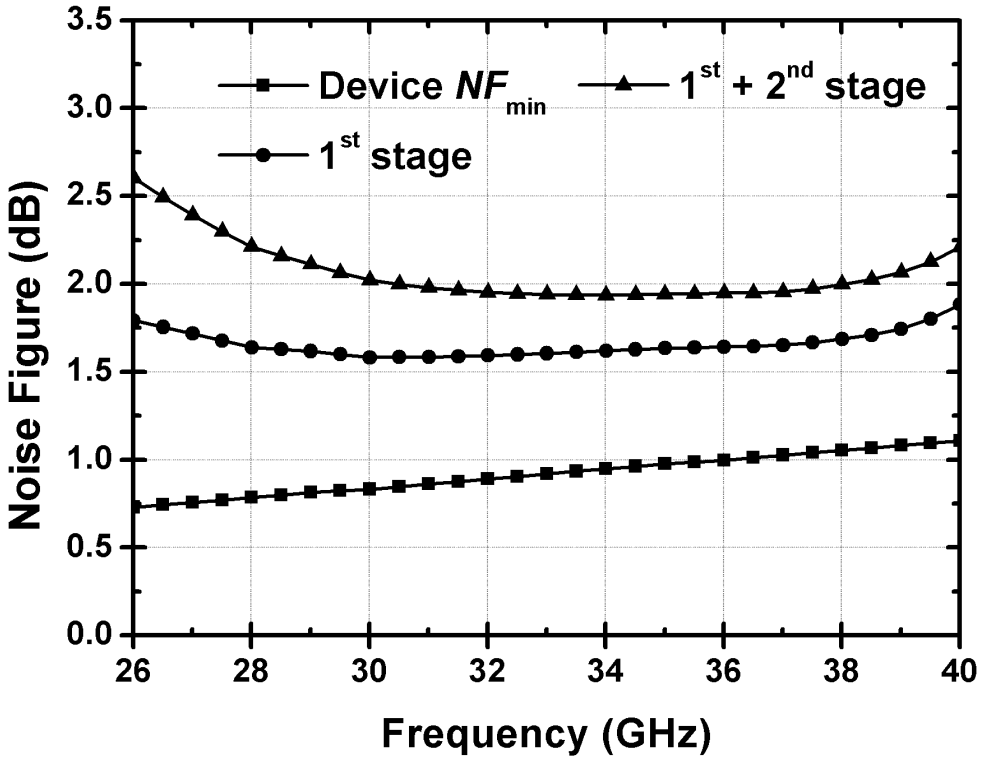

Fig. 2.16. Simulated noise figure of the first and second stages complete with the input and inter-stage matching networks.

As mentioned above, the noise performance of the third stage is of lower priority with the 19.4 dB gain provided by the first two stages, and the impedance matching is designed for optimal gain performance. As shown in Fig. 2.7, both the inter-stage matching between the second and third stages and the output matching are implemented using π-type matching networks for wideband performance. The two π-type matching networks both consists of two series transmission lines, a short stub, and an open stub for lower Q-factor during impedance transfer. The inter-stage matching involves impedance transfer from $Z_{out2,conj}^{*}$ to $Z_{in3,conj}$, and the output matching from $Z_{out3,conj}^{*}$ to Z_L = 50 Ω. The transmission lines are realized using double metal layers in the 0.15-μm GaAs pHEMT process for lower insertion loss.

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2.2.4 Simulation Results

All matching networks are realized using transmission lines and lump elements (MIM capacitors). The transmission lines are realized using double metal layers in the 0.15-μm pHEMT GaAs process for lower insertion loss. Large-scale EM simulations are performed for each of the matching networks. Fig. 2.17 to 3.20 shows the 3-D rendering of the matching networks used for EM simulations. Note that since the RC-feedbacks adopted at the second and third stages surround the device in the physical layout, the feedback structures are broken into smaller pieces for separate EM simulations.

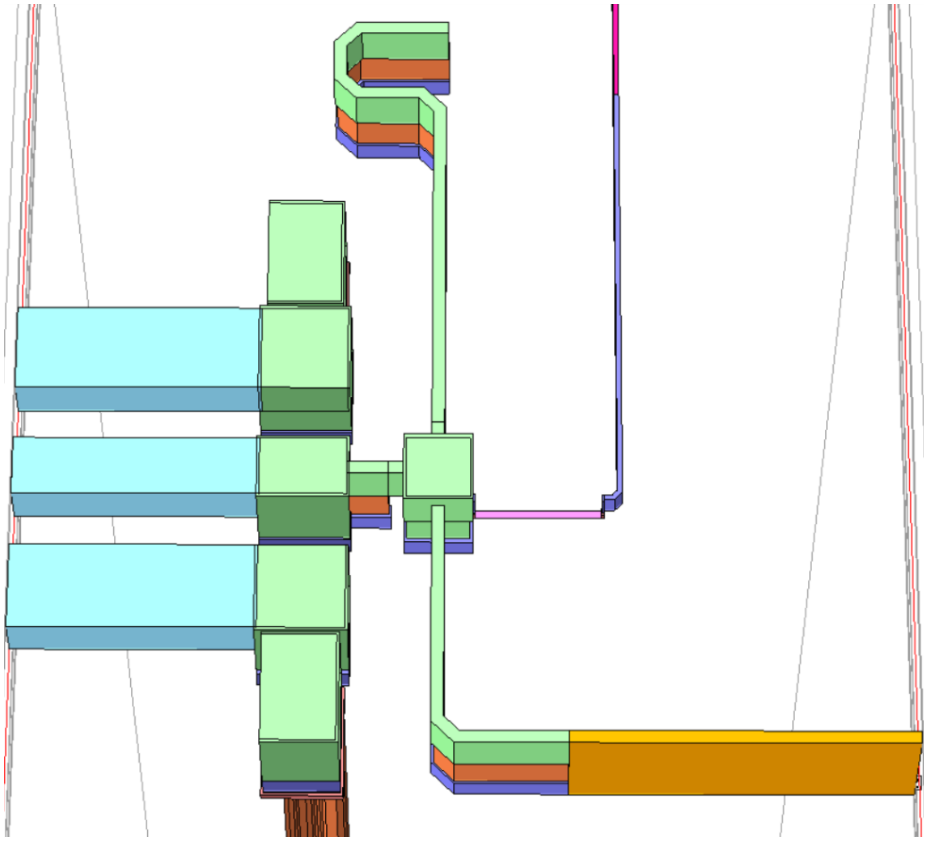

Fig. 2.17. 3-D rendering of the input matching network with the GSG RF pads used for EM simulation.

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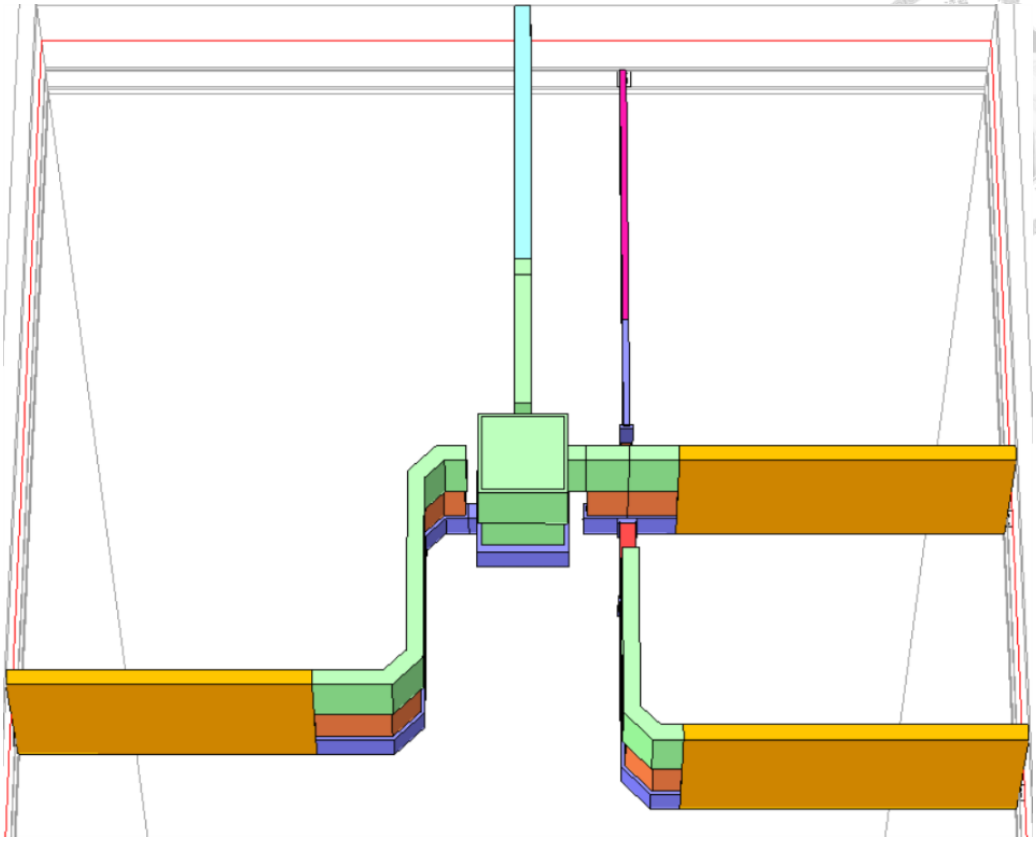

Fig. 2.19. 3-D rendering of the inter-stage matching network between the first and second stages used for EM simulation.

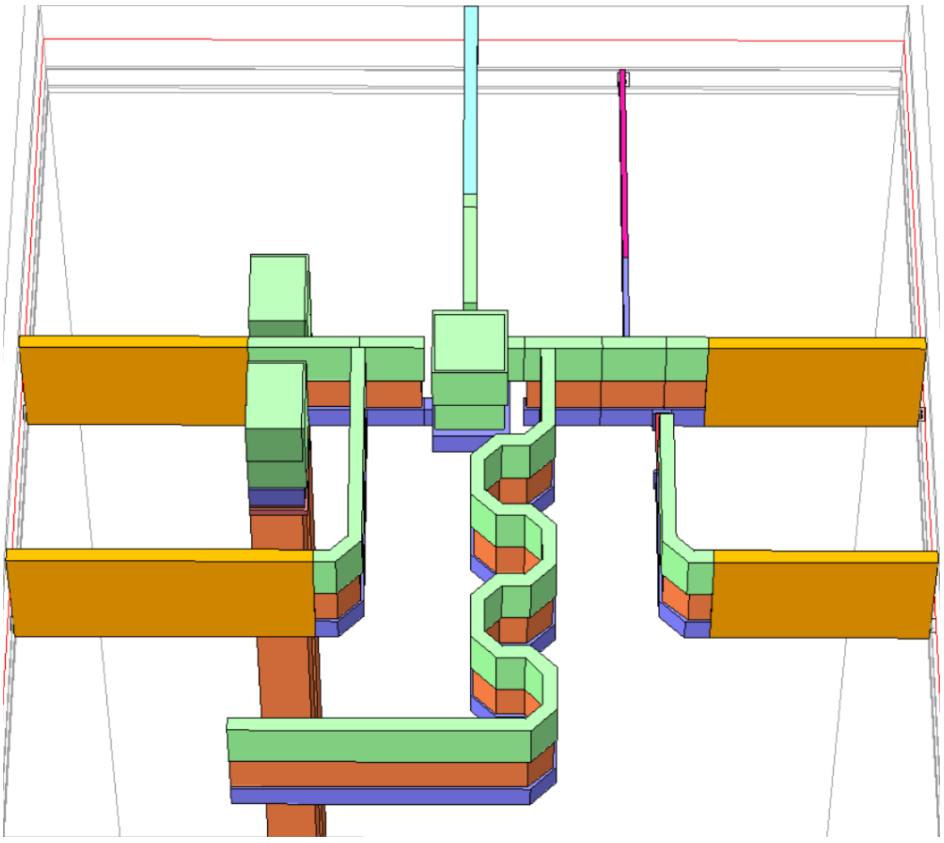

Fig. 2.18. 3-D rendering of the inter-stage matching network between the second and third stages used for EM simulation.

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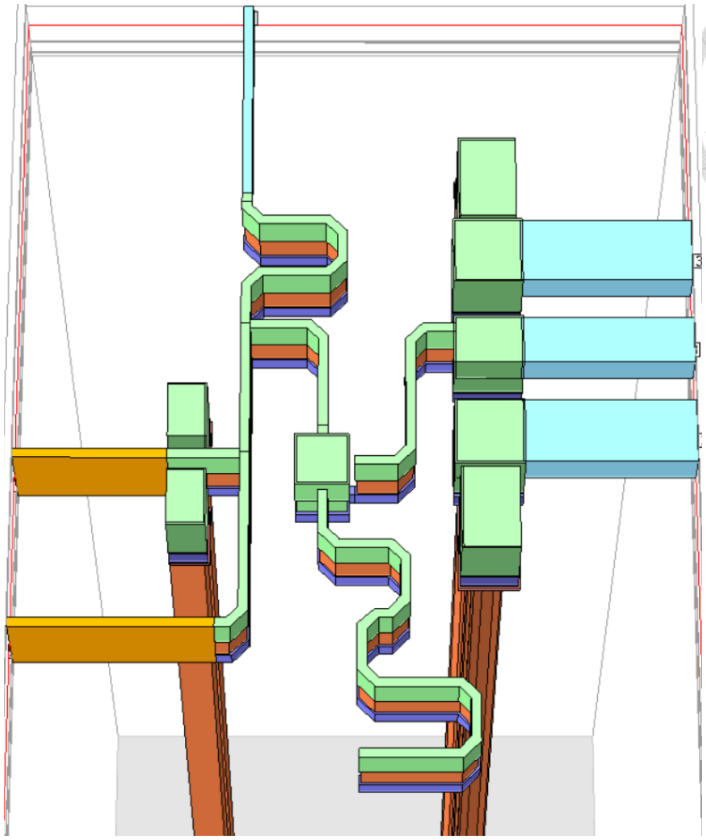

Fig. 2.20. 3-D rendering of the output matching network with the GSG RF pads used for EM simulation.

As mentioned in section 3.1, the bias conditions of the three stages are the same at [V_{GS}, V_{DS}] = [0.6 V, 2.0 V]. Since the 2f x 25um device is used for all three stages, the simulated I_{DS}'s of the three stages are the same at 8 mA. This result in an overall DC power consumption of 48 mW. Fig. 2.21 and 3.22 shows the post-EM simulated *S*-parameters and noise figure of the proposed Q-band LNA, respectively. The peak gain is 21.8 dB at 31.8 GHz, and the 3-dB bandwidth is 19.7 GHz from 23.7 to 43.4 GHz with average gain of 20.9 dB. The gain is 21.5 dB at 38 GHz, and has flatness of 21.5 ± 1 dB from 27.8 to 40.5 GHz. The input return loss is above 15 dB from 35.8 to 40.6 GHz, and the output return loss is above 15 dB from 36.1 to 39.9 GHz. The noise figure is below 2.5 dB from 27.7 to 40.0 GHz. The noise figure has minimum of 2.1 dB at 33.0 GHz, and average of 2.3 dB from 26 to 40 GHz. The post-EM simulation results meets the target performances listed in Table 2.1 with some margins.

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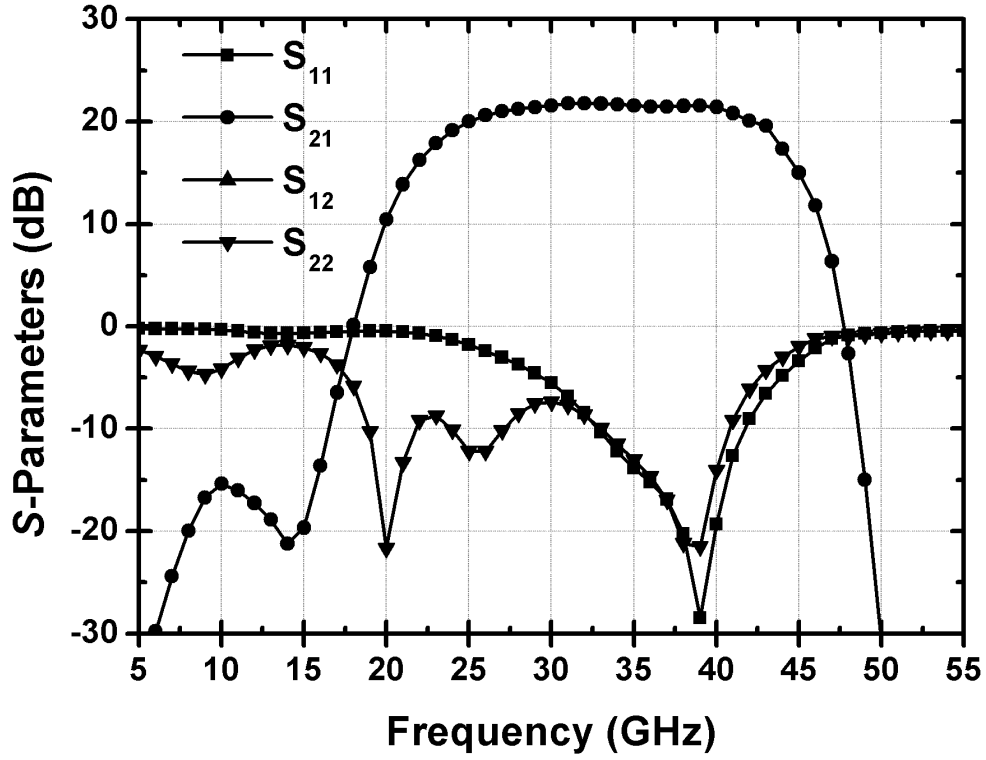

Fig. 2.22. Simulated *S*-parameters of the proposed Q-band LNA.

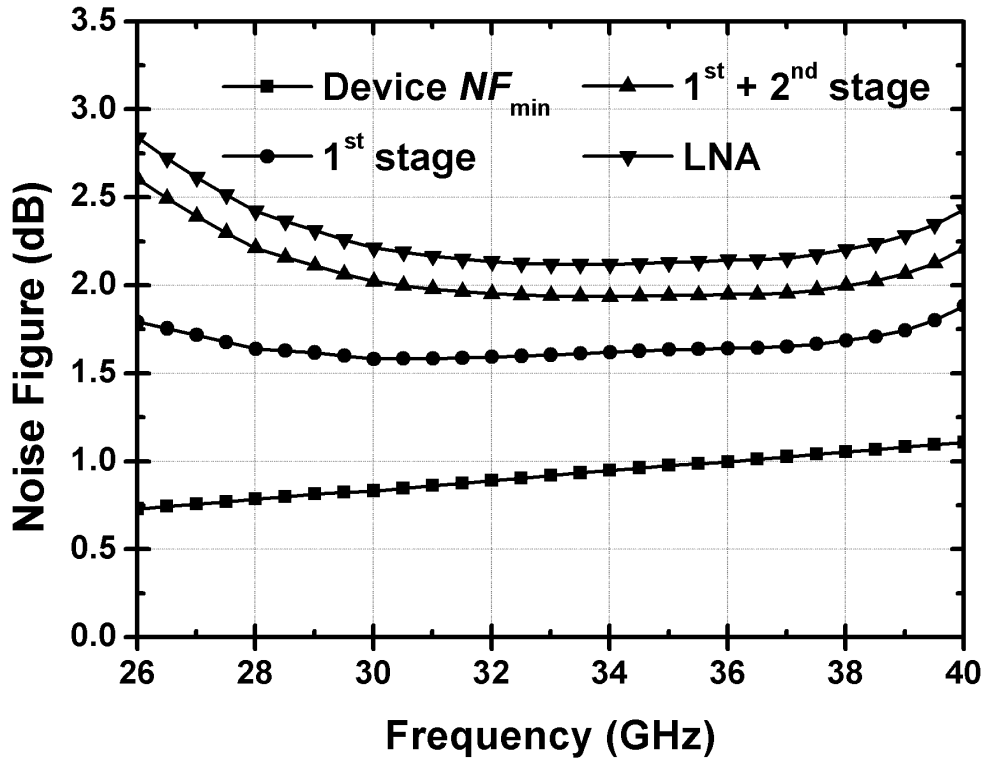

Fig. 2.21. Simulated noise figure of the proposed Q-band LNA.

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Fig. 2.23 shows the post-EM simulated stability factor of the proposed LNA. The stability factor is above 1 from 0 to 60 GHz, which indicates a stable design. Since the proposed LNA is of three-stage design, two cases of inter-stage stability analysis are required. In each case, the LNA is separated between the stages. This result in two two-port networks denoted as N_1 and N_2. For N_1, the set of terminations with unity magnitude at port 1, i.e., the border of the Smith chart, are mapped to port 2. The 1-to-2 mapped circles are therefore defined by the loci of terminations on port 1 as seen at port 2. The 1-to-2 mapped circles of N_1 are then compared with the source stability circles of N_2. Any overlapping between the circles at the same frequency indicates that for some $|\Gamma_{S1}| < 1$ will result in a $|\Gamma_{Out2}| > 1$. Similarly, the 2-to-1 mapped circles of N_2 are compared with the load stability circles of N_1. Any overlapping between the circles at the same frequency indicates that for some $|\Gamma_{L1}| < 1$ will result in a $|\Gamma_{In1}| > 1$. Fig. 2.24 and 3.25 shows the post-EM simulated inter-stage analyses. The circles in both cases are carefully checked to ensure no overlapping occurs at the same frequency.

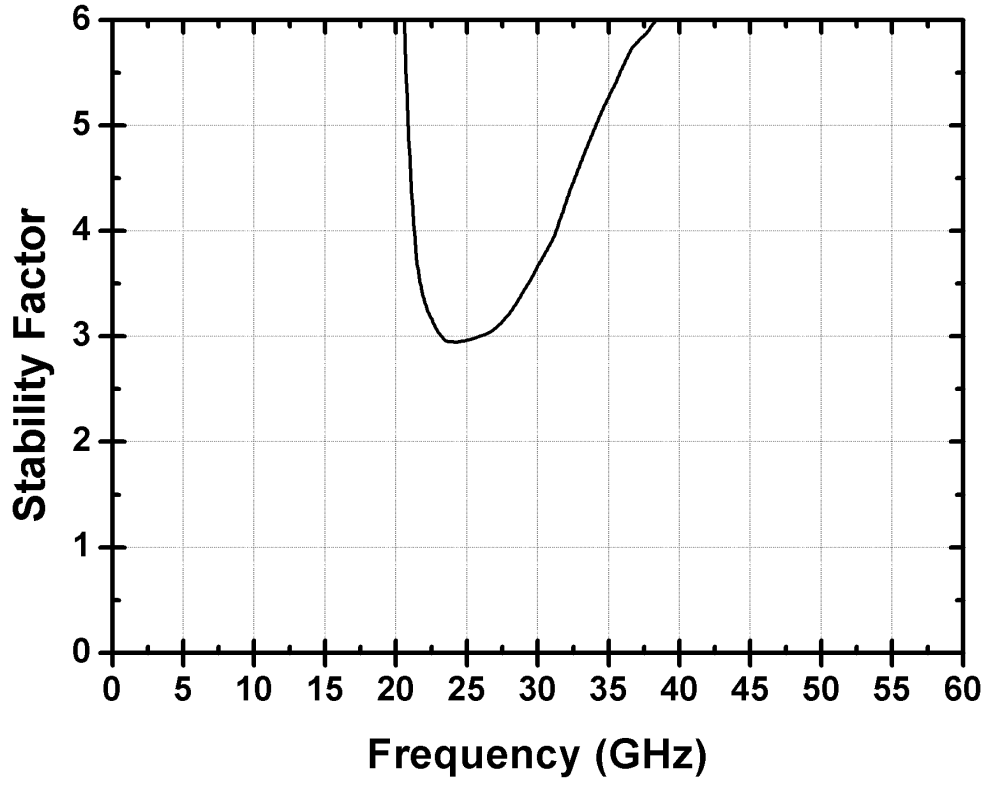

Fig. 2.23. Simulated stability factor of the proposed Q-band LNA.

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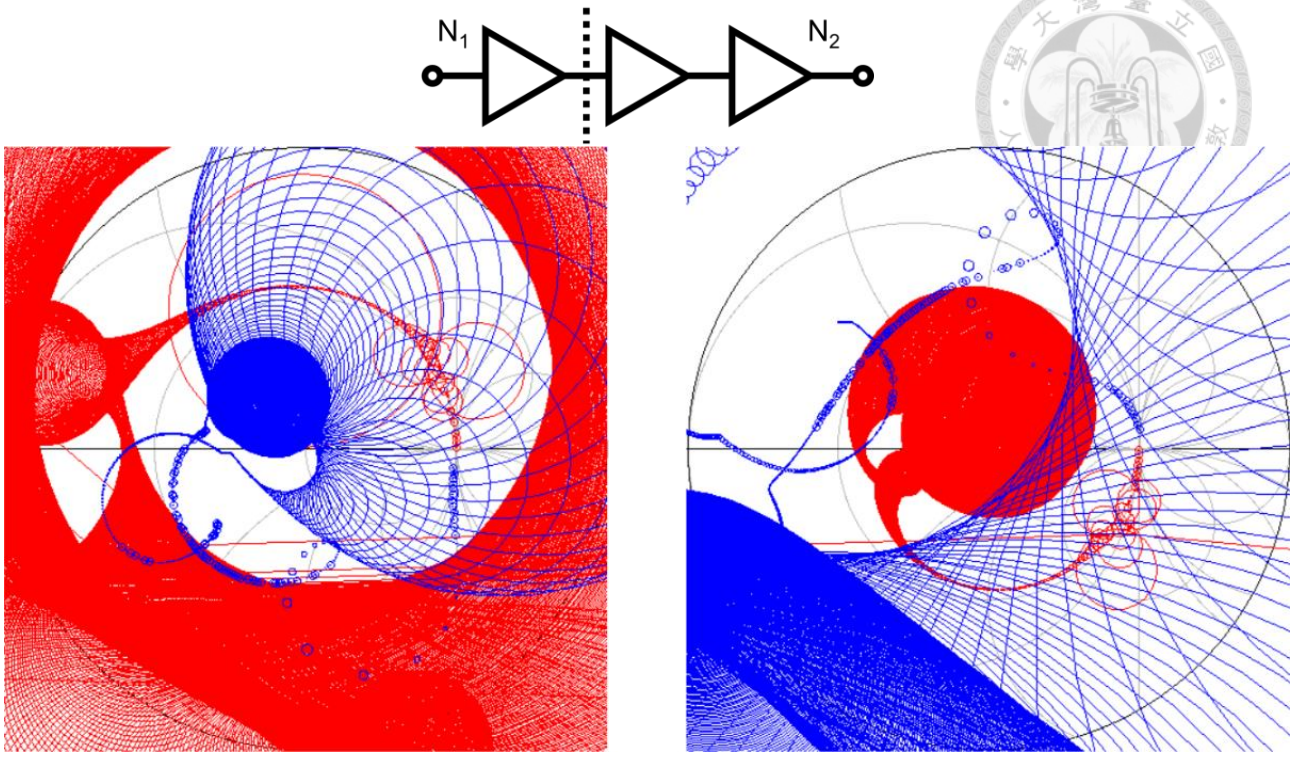
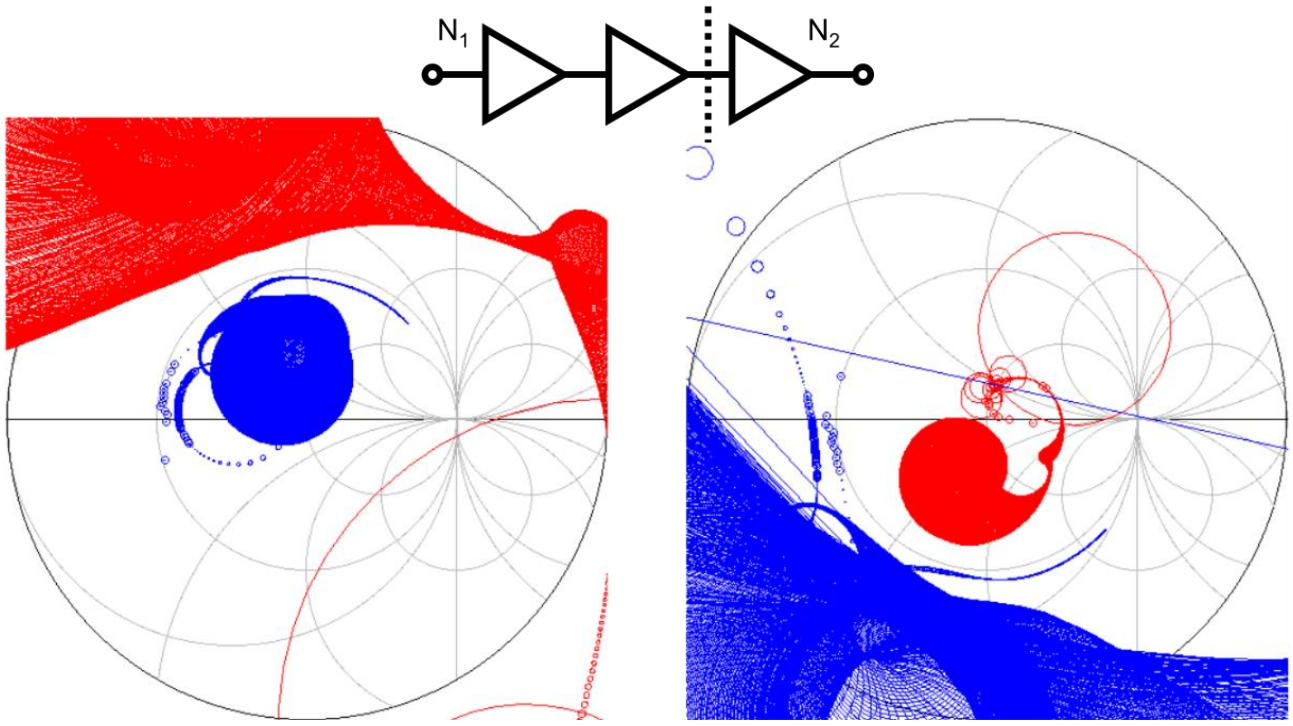


(a) (b)

Fig. 2.24. Simulated inter-stage stability analyses between the first and second stages, with (a) load stability circles of N_1 compared with 2-to-1 mapped circles of N_2, and (b) source stability circles of N_2 compared with 1-to-2 mapped circles of N_1.



(a) (b)

Fig. 2.25. Simulated inter-stage stability analyses between the second and third stages, with (a) load stability circles of N_1 compared with 2-to-1 mapped circles of N_2, and (b) source stability circles of N_2 compared with 1-to-2 mapped circles of N_1.

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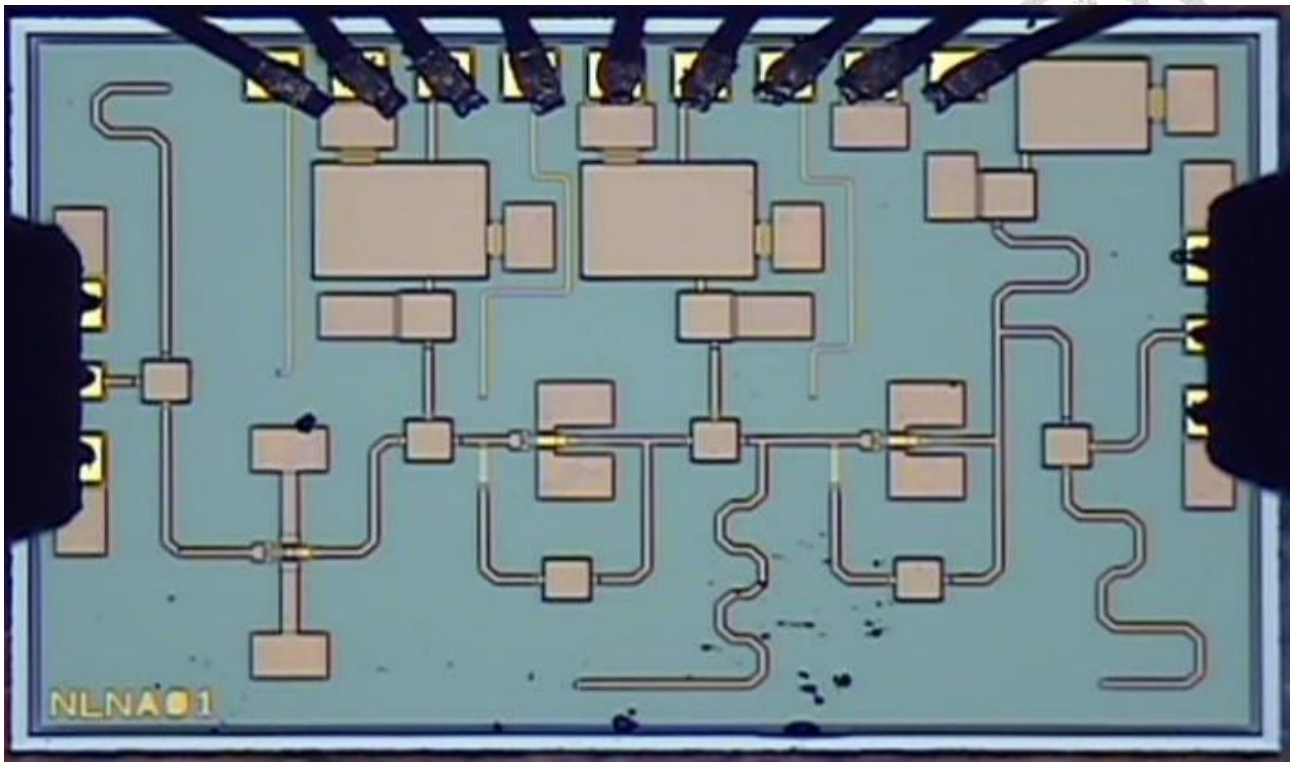

Fig. 2.26. Die photograph of the proposed Q-band LNA.

2.3 Experimental Results

The proposed Q-band LNA was designed and realized in 0.15-μm pHEMT GaAs process (PE15-00) provided by WIN Semiconductors. As shown in Fig. 2.26, the die size measures at 1.5 x 1 mm^2 with RF and DC pads included. Dice were mounted on PCB boards with bond-wires between die and PCB for DC application. Off-chip bypass networks were designed and implemented on PCB boards. All measurements were performed using on-wafer probing.

Table 2.2. Bias conditions during small-signal measurements of the proposed Q-band LNA.

	V_{GS} (V)		V_{DS} (V)	I_{DS} (mA)	
	Sim.	**Meas.**		**Sim.**	**Meas.**
1st stage	0.6	0.69	2.0	8.0	8.0
2nd stage	0.6	0.68	2.0	8.0	8.2
3rd stage	0.6	0.68	2.0	8.0	8.0

An Agilent N5245A PNA-X microwave network analyzer was used for small-signal and noise measurements. Table 2.2 shows the bias conditions during small-signal measurements. V_{GS}'s of all

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three stages were fine tuned during measurement for the I_{DS}'s to agree with simulation. The fine-tuned V_{GS}'s of all three stages are similar and around 0.08 V higher than simulation. The resulting bias condition listed in Table 2.2 with matched I_{DS}'s is used for small-signal and noise measurements. Fig. 2.27 shows the measured *S*-parameters of the proposed Q-band LNA compared with the simulation. The peak gain is 23.5 dB at 31.5 GHz, and the 3-dB bandwidth is 16.2 GHz from 24.1 to 40.3 GHz with average gain of 22.1 dB. The gain is 21.3 dB at 38 GHz, and has flatness of 22.5 ± 1 dB from 25.7 to 37.6 GHz. The input return loss is above 8 dB from 36.2 to 41.4 GHz, and the output return loss is above 15 dB from 33.4 to 39.3 GHz. Fig. 2.28 shows the measured noise figure of the proposed Q-band LNA compared with the simulation. The noise figure is below 3 dB from 27.8 to 39.8 GHz. The noise figure has minimum of 2.2 dB at 34.0 GHz, and average of 2.6 dB from 26 to 40 GHz. The proposed LNA successfully meets the target performances listed in Table 2.1 with some margins except for the input return loss, which will be discussed later.

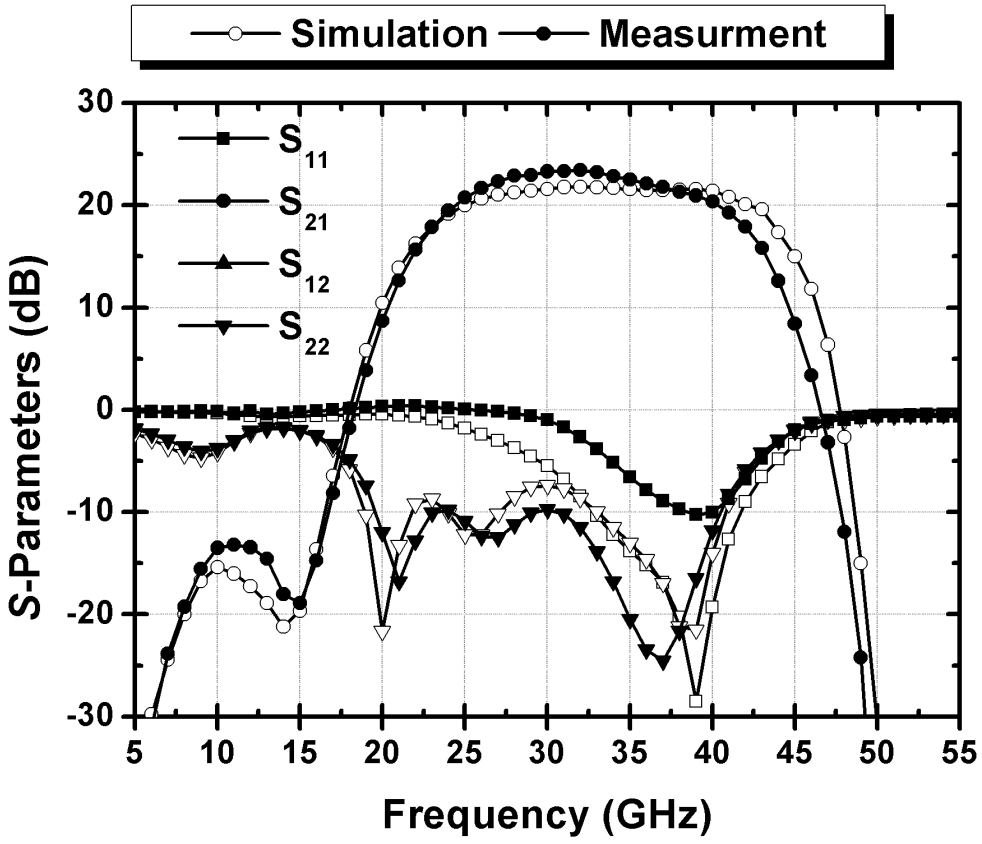

Fig. 2.27. Measured and simulated *S*-parameters of the proposed Q-band LNA.

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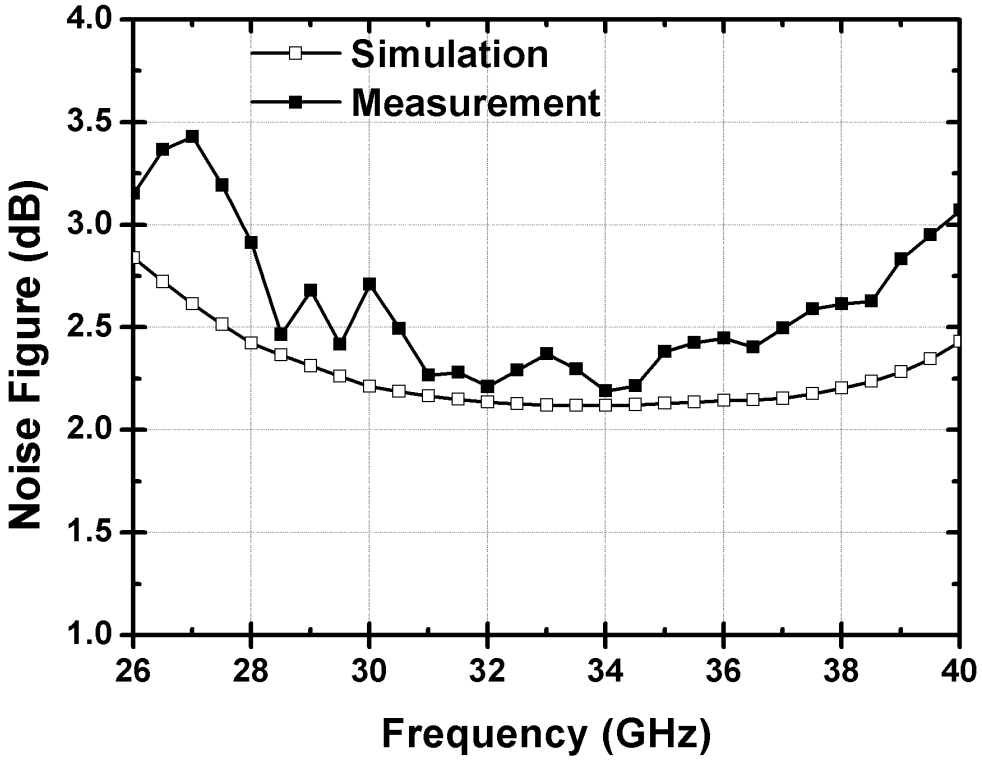

Fig. 2.28. Measured and simulated noise figure of the proposed Q-band LNA.

As shown in Fig. 2.27, the measured *S*-parameters agree well with simulation with the exception of S_{11}. Furthermore, the measurement results show a slight input return gain below 0.3 dB from 17.1 to 25.6 GHz. For the proposed LNA design, test circuits of the first and third stages were also designed and realized. Small-signal measurements of the test circuits were performed under the same bias conditions listed in Table 2.2. Fig. 2.29 shows the measured *S*-parameters of the first stage test circuit compared with the simulation. The measurement results show a slight input return gain and disagreement with simulation in S_{11}, which are similar to the case of the LNA. Fig. 2.30 shows the measured *S*-parameters of the third stage test circuit compared with the simulation. The measurement results agree well with simulation. Thus, the potential source of issue narrows down to the first stage. It is worth pointing out that from Fig. 2.29 and 3.30, the wideband performance by adopting RC-feedback and wideband matching in the latter stages is evident as the third stage test circuit shows a much wider 3-dB bandwidth and better gain flatness than the first stage.

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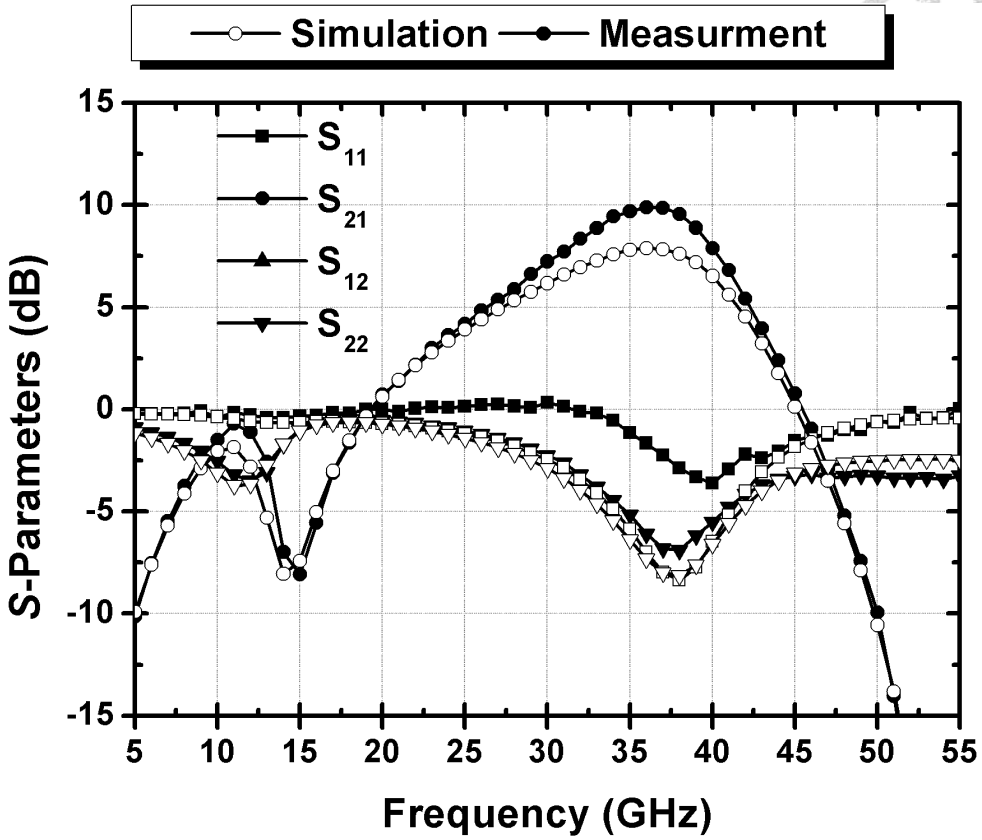

Fig. 2.30. Measured and simulated *S*-parameters of the first stage test circuit.

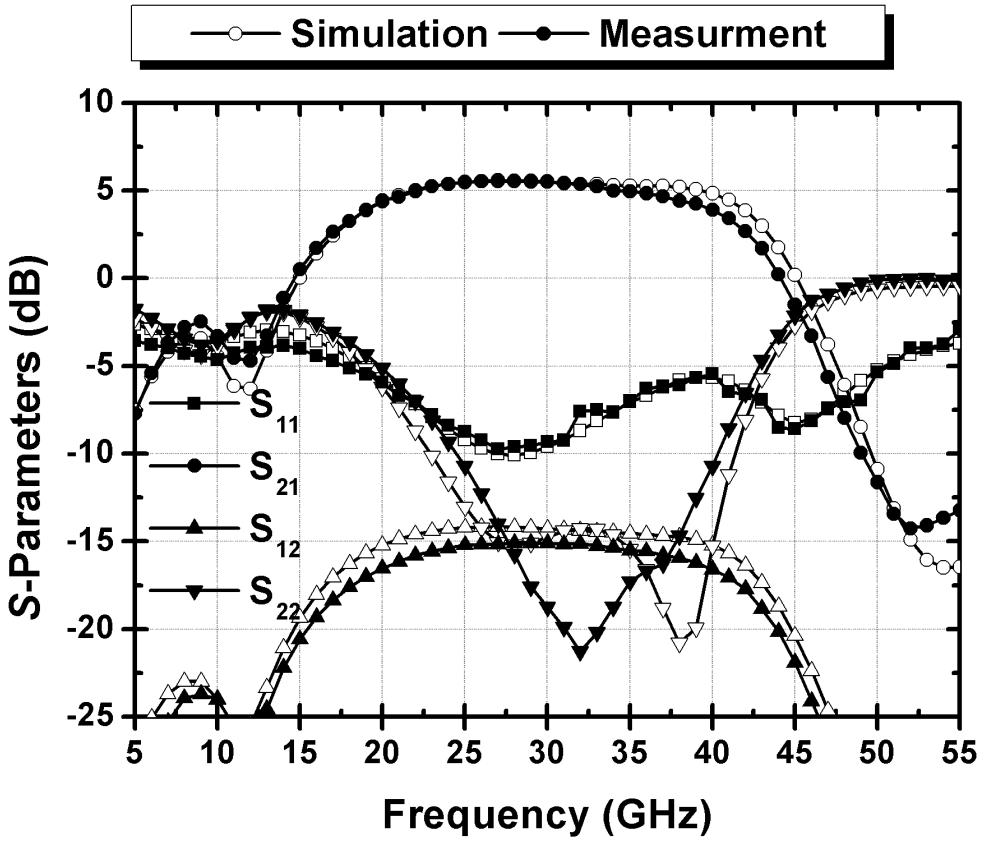

Fig. 2.29. Measured and simulated *S*-parameters of the third stage test circuit.

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2.4 Discussion and Second Tape-out

2.4.1 Modeling Issue of Device with Source Degeneration

As mentioned in section 2.3, the potential source of issue for the disagreement in S_{11} between measurement and simulation lies within the first stage. For the proposed LNA design, test-key of the device with source degeneration at the first stage, i.e., 2f x 25 μm CPW-configuration device with 85 x 20 μm TL_{deg}'s, was also designed and realized. Fig. 2.31 shows the die photograph of the test-key using TRL calibration. Small-signal measurements of the test-key were performed under the same bias conditions for the first stage listed in Table 2.1. The measurement results of the test-key are used to verify the accuracy of simulation. Fig. 2.32 shows the simulation setup in Agilent ADS for CPW-configuration device with TL_{deg}'s. The foundry-provided measurement data (in the form of ".s2p" files) is used for the 2f x 25 μm CPW-configuration device. Two TL_{deg}'s terminated with EM simulated backside-vias are attached to reference node of the device measurement data (".s2p" file).

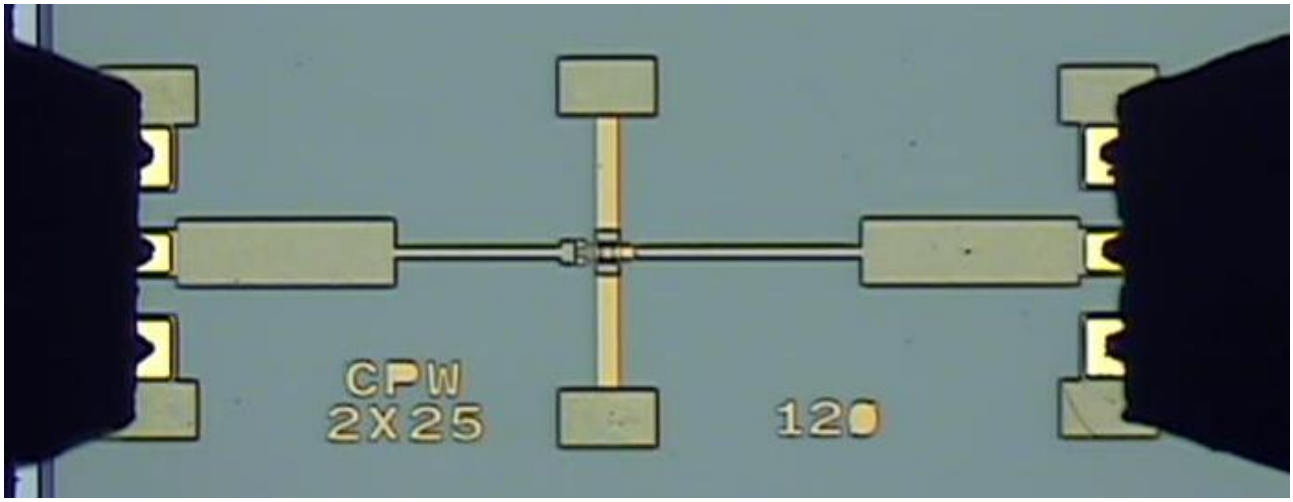

Fig. 2.31. Die photograph of the test-key for the 2f x 25 μm CPW-configuration device with 85 x 20 μm TL_{deg}'s.

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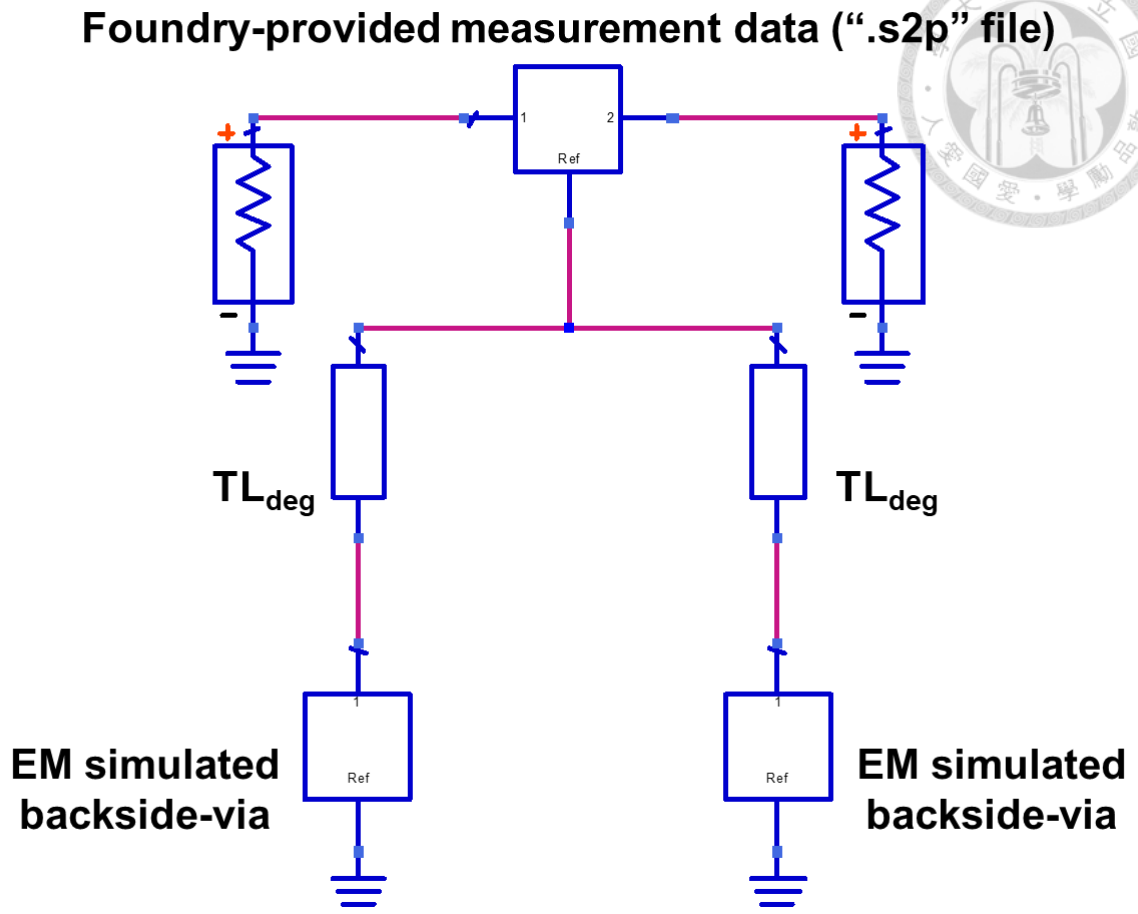

Fig. 2.32. Simulation setup for CPW-configuration devices with TL_{deg}'s in Agilent ADS.

Fig. 2.33 and 3.34 shows the magnitude (in dB) and phase of the measured *S*-parameters of the test-key compared with simulation, respectively. The measurement and simulation show disagreement in both magnitude and phase at 38-GHz, and the difference increases with frequency. This indicates an inaccurate modeling of the CPW-configuration device with TL_{deg}'s in simulation. The measurement result of the test-key is then swap into the simulation for the overall LNA instead of the foundry-provided measurement data for the first stage device. Fig. 2.35 shows the simulated *S*-parameters of the LNA with measured test-key as the first stage device. The simulation and measurement of the LNA agrees well, and further confirms the inaccuracy of foundry-provided measurement data.

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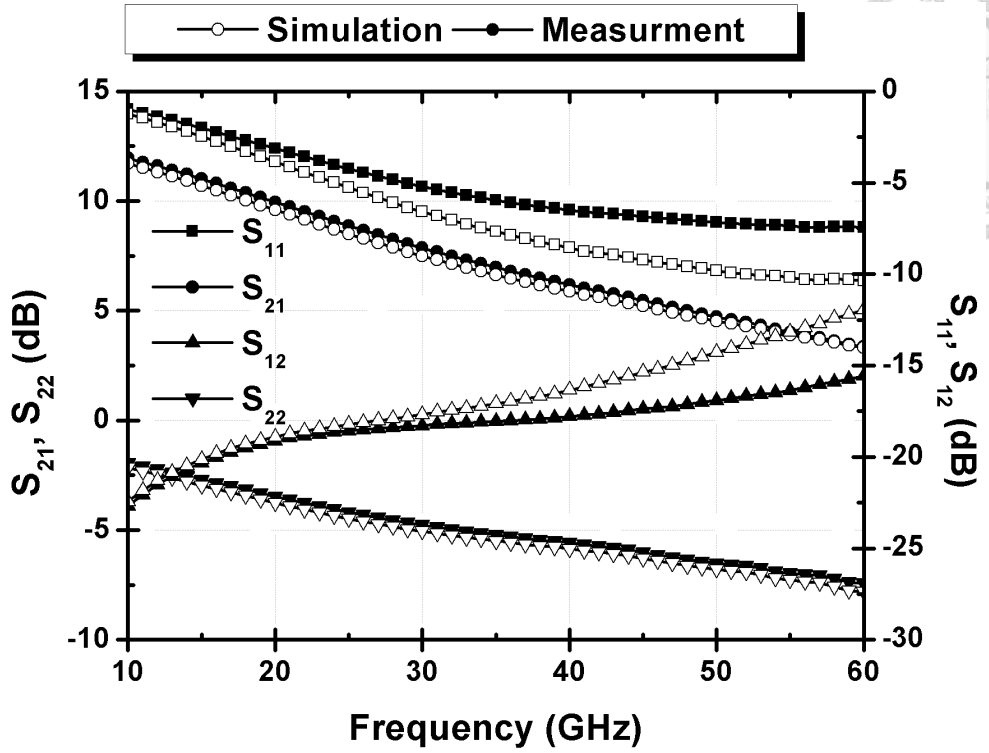

Fig. 2.33. Measured and simulated magnitudes (in dB) of the *S*-parameters of the 2f x 25 μm CPW-configuration device with 85 x 20 μm TL_{deg}'s.

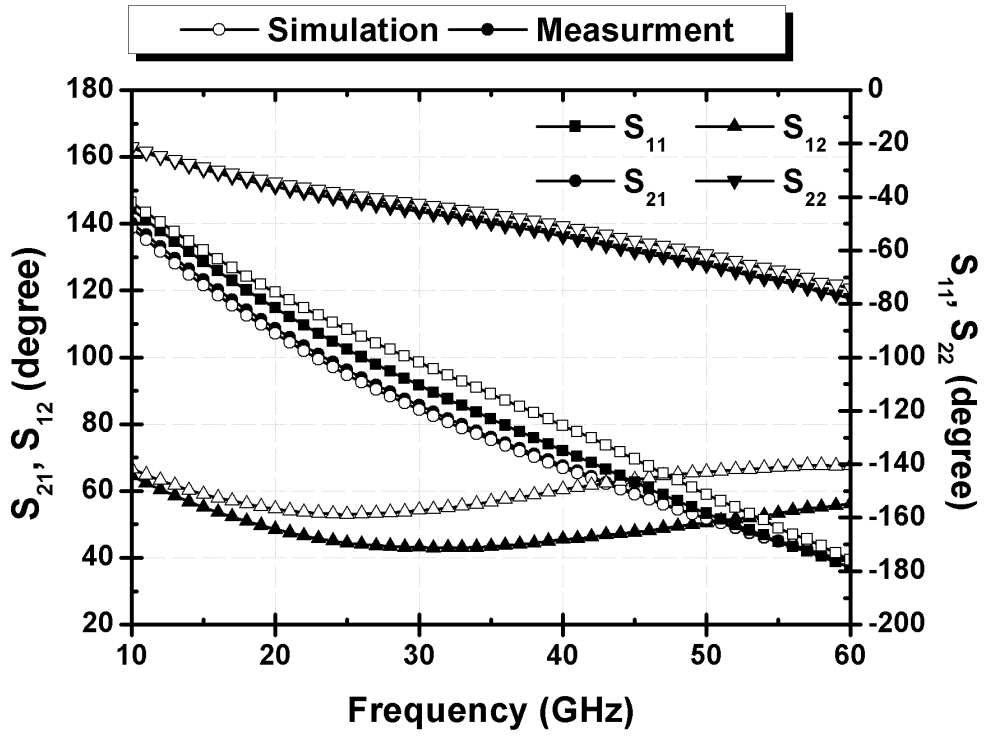

Fig. 2.34. Measured and simulated phases of the *S*-parameters of the 2f x 25 μm CPW-configuration device with 85 x 20 μm TL_{deg}'s.

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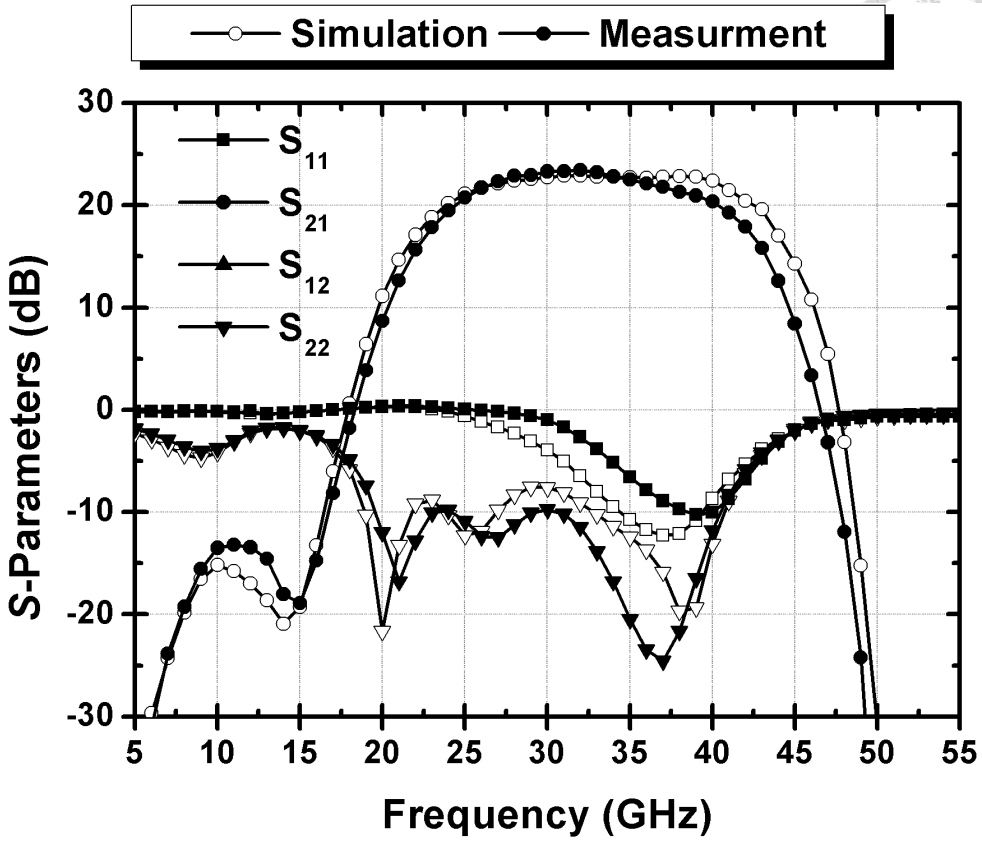

Fig. 2.35. Measured and simulated *S*-parameters of the proposed LNA. The measurement results of the test-key is used as the device at the first stage in the simulation, instead of the foundry-provided measurement data.

In order to enable an accurate and scalable design in the future using the same process, corrections to the simulation setup in Fig. 2.32 are required. With 85 x 20 μm TL_{deg}'s in the physical layout of the test-key, the TL_{deg}'s in the simulation are shortened by 60 μm to 25 x 20 μm. Fig. 2.36 and 3.37 shows the magnitude (in dB) and phase of the measured *S*-parameters of the test-key compared to simulation with the proposed correction, respectively. By shortening the length of TL_{deg}'s by 60 μm in simulation compared to the physical layout, the measurement and simulation show good agreement. The proposed correction is then applied to the simulation of the overall LNA. As shown in Fig. 2.38, *S*-parameters of the LNA with the corrected simulation shows good agreement with measurement. Thus, the proposed correction states that CPW-configuration devices with TL_{deg}'s L μm in length in physical layout should be simulated with TL_{deg}'s (L – 60) μm in length for accurate modeling.

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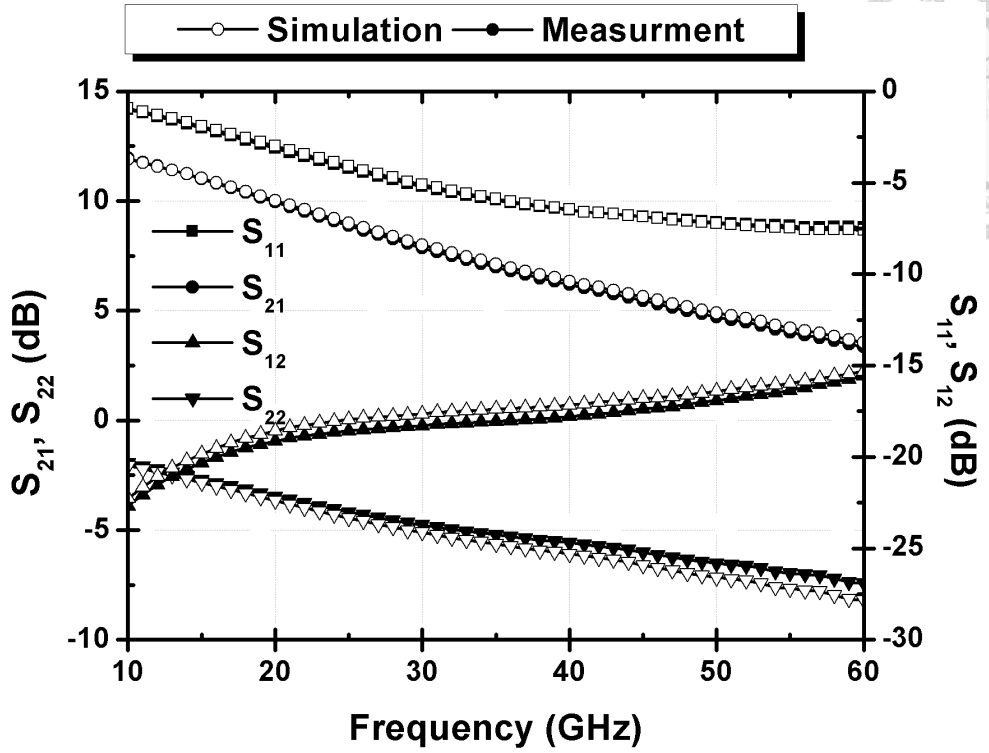

Fig. 2.36. Measured and simulated magnitudes (in dB) of the *S*-parameters of the 2f x 25 μm CPW-configuration device with 85 x 20 μm TL_{deg}'s. Length of the TL_{deg}'s in simulation is shortened by 60 μm to 25 μm.

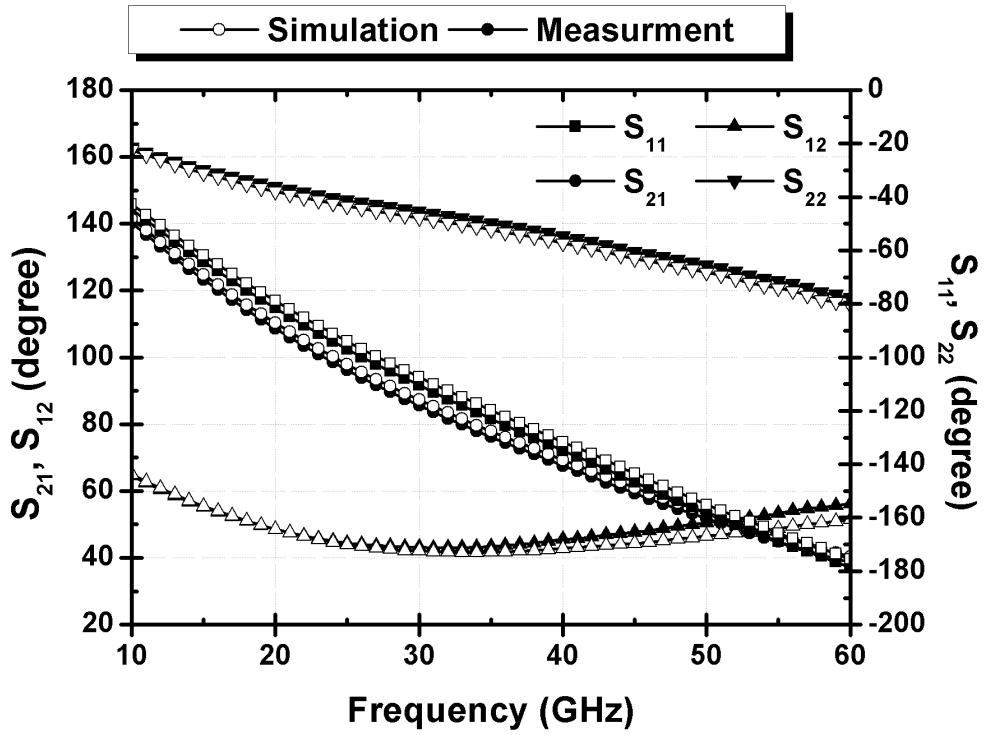

Fig. 2.37. Measured and simulated phases of the *S*-parameters of the 2f x 25 μm CPW-configuration device with 85 x 20 μm TL_{deg}'s. Length of the TL_{deg}'s in simulation is shortened by 60 μm to 25 μm.

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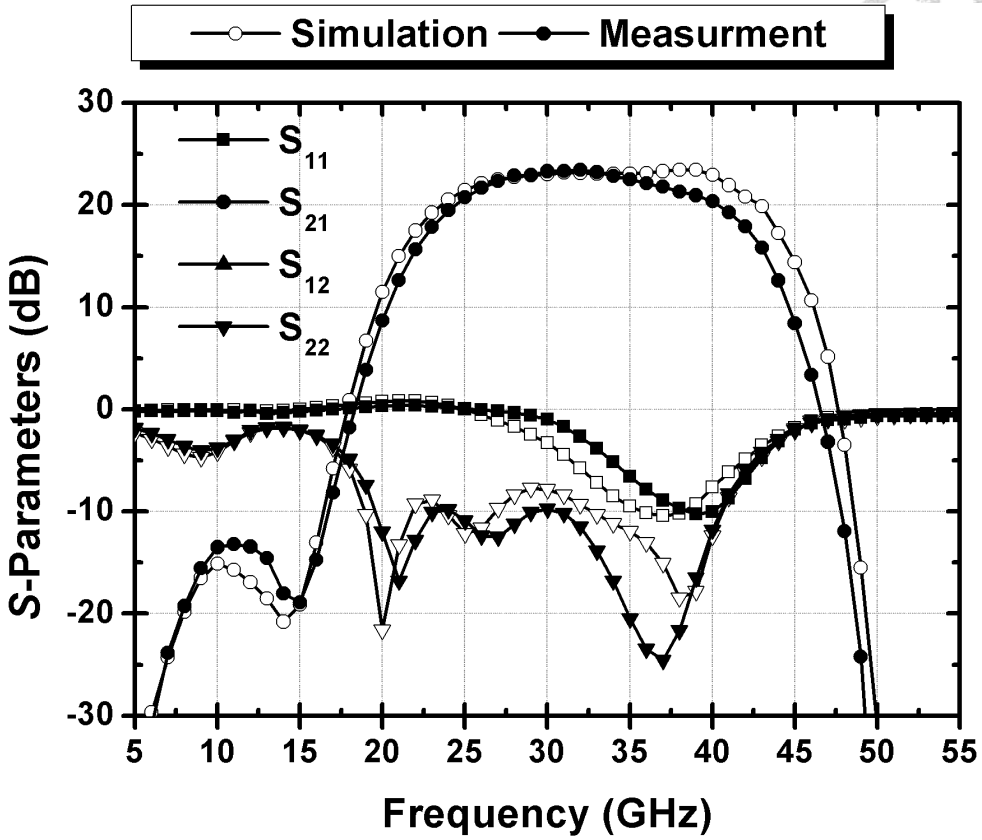

Fig. 2.38. Measured and simulated *S*-parameters of the proposed LNA, with the proposed correction applied in the simulation.

2.4.2 Design Modification and Second Tape-out

In order to eliminate the input return gain from 17.1 to 25.6 GHz of the original LNA design and verify the proposed correction in simulation, a modified LNA design was designed and realized in the same process for a second tape-out. The TL_{deg}'s of the first stage device is elongated by 40 μm to 125 μm, which corresponds to 65 μm in simulation with the proposed correction. Fig. 2.39 shows the simulated *S*-parameters of the modified LNA with the proposed correction. Assuming the proposed correction is verified, the input return gain is successfully eliminated with the small-signal performances mostly unchanged from the original LNA. Fig. 2.40 shows the simulated noise figure of the modified LNA with the proposed correction, which is nearly unchanged from the original LNA. This is to be expected as Fig. 2.9 and 3.10 show that the length of TL_{deg} has little effect on the device NF_{min} and Z_{opt}.

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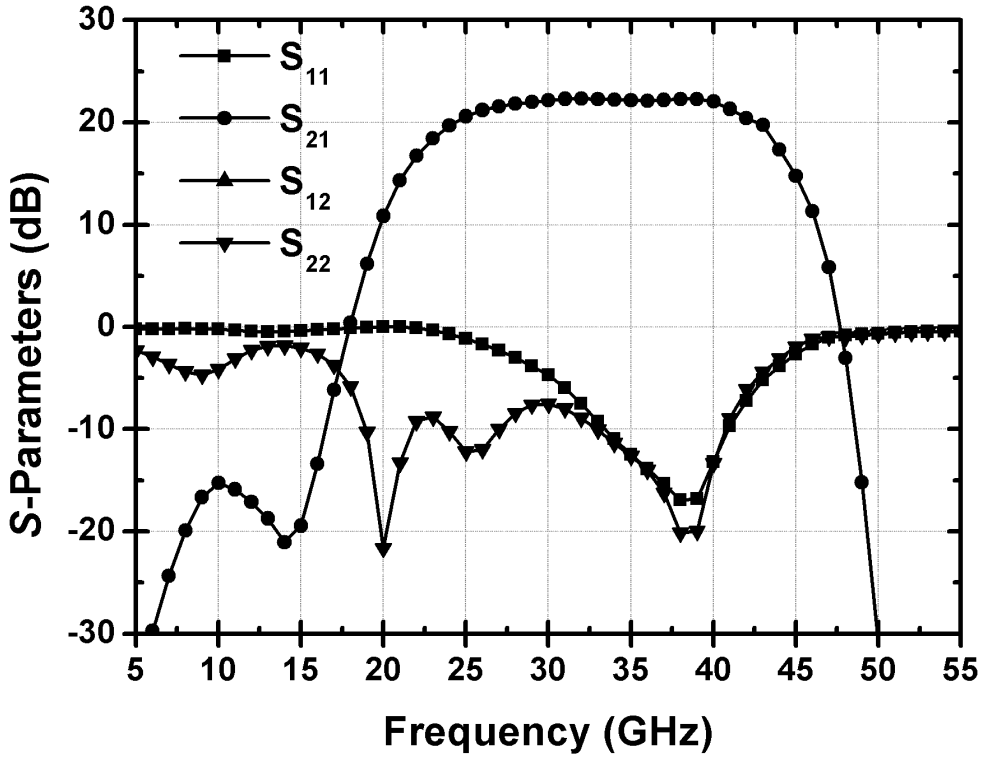

Fig. 2.39. Post-EM simulated *S*-parameters of the modified LNA with the proposed correction.

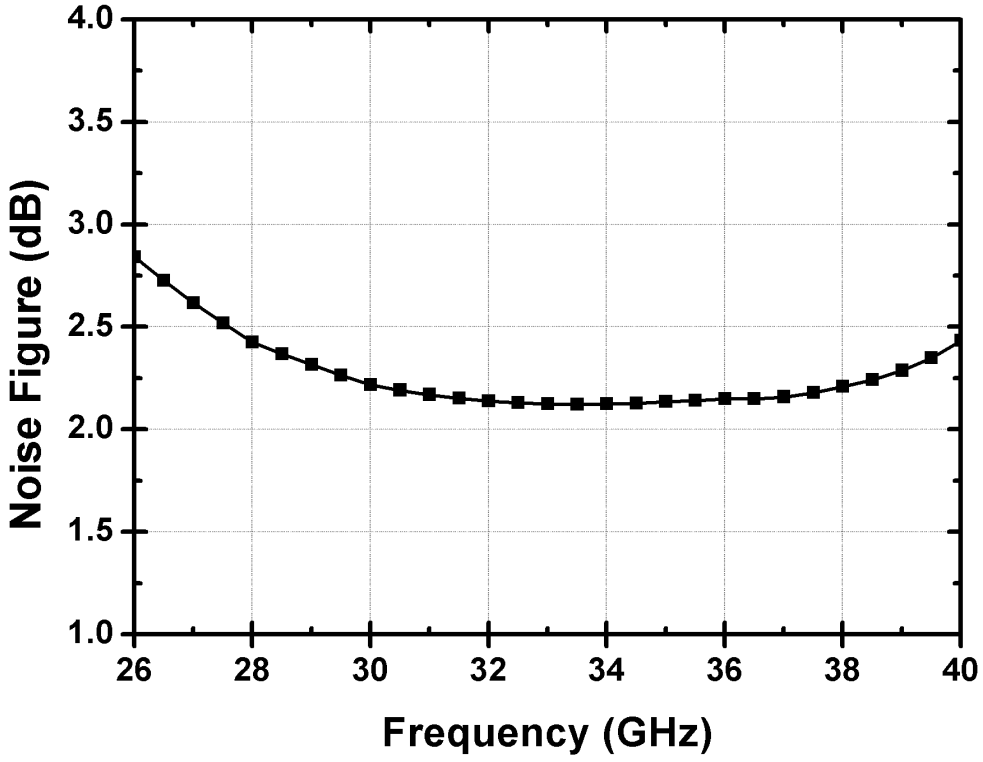

Fig. 2.40. Post-EM simulated noise figure of the modified LNA with the proposed correction.

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2.4.3 Experimental Results

The modified LNA with the proposed modification to the first stage was designed and realized in the second tape-out, using the same 0.15-μm GaAs pHEMT process provided by WIN Semiconductors. With the only change being the elongated TL_{deg}'s, other areas of the physical layout remained unchanged. Dice were mounted on PCB boards with bond-wires between die and PCB for DC application. Off-chip bypass networks were designed and implemented on the PCB board. All measurement were performed using on-wafer probing.

Table 2.3. Bias conditions during small-signal measurements of the proposed Q-band LNA.

	V_{GS} (V)		V_{DS} (V)	I_{DS} (mA)	
	Sim.	Meas.		Sim.	Meas.
1st stage	0.6	0.61	2.0	8.0	8.0
2nd stage	0.6	0.62	2.0	8.0	8.0
3rd stage	0.6	0.62	2.0	8.0	8.1

An Agilent N5245A PNA-X microwave network analyzer was used for small-signal and noise measurements. Table 2.3 shows the bias conditions during small-signal measurements. V_{GS}'s of all three stages were fine tuned during measurement for the I_{DS}'s to agree with simulation. The fine-tuned V_{GS}'s of all three stages are similar and around 0.02V higher than simulation. The resulting bias condition listed in Table 2.3 with matched I_{DS}'s is used for small-signal measurements. Fig. 2.41 shows the measured *S*-parameters of the modified LNA compared to the simulation with the proposed correction. The measurement and simulation with the proposed correction show good agreement including in S_{11}. As a result, the input return gain from 17.1 to 25.6-GHz found in the original LNA is successfully eliminated. Furthermore, the agreement between simulation and measurement results of the modified LNA in the second tape-out verify the proposed correction applied in simulation. The peak gain is 23.3 dB at 33.1 GHz, and the 3-dB bandwidth is 15.3 GHz from 24.7 to 40.0-GHz with average gain of 22.2 dB. The gain is 21.5 dB at 38 GHz, and has

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flatness of 22.3 ± 1 dB from 25.7 to 37.6 GHz. The input return loss is above 15 dB from 37.2 to 40.4 GHz, and the output return loss is above 15 dB from 34.4 to 39.4 GHz. Fig. 2.42 shows the measured noise figure of the proposed Q-band LNA compared with the simulation. The noise figure is below 3dB from 27.9 to 40.0 GHz. The noise figure has minimum of 2.2 dB at 31.5 GHz, and average of 2.6 dB from 26 to 40 GHz. The modified LNA successfully meets the target performances listed in Table 2.1 with some margins.

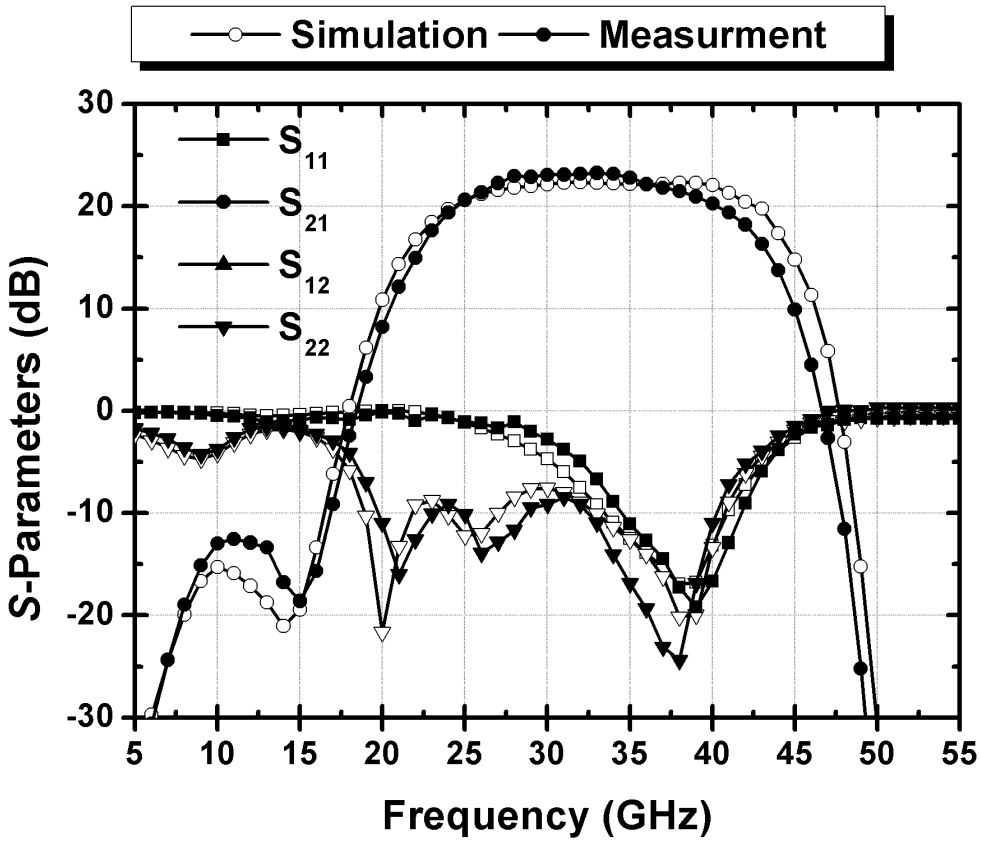

Fig. 2.41. Measured and simulated *S*-parameters of the modified LNA, with the proposed correction applied in the simulation.

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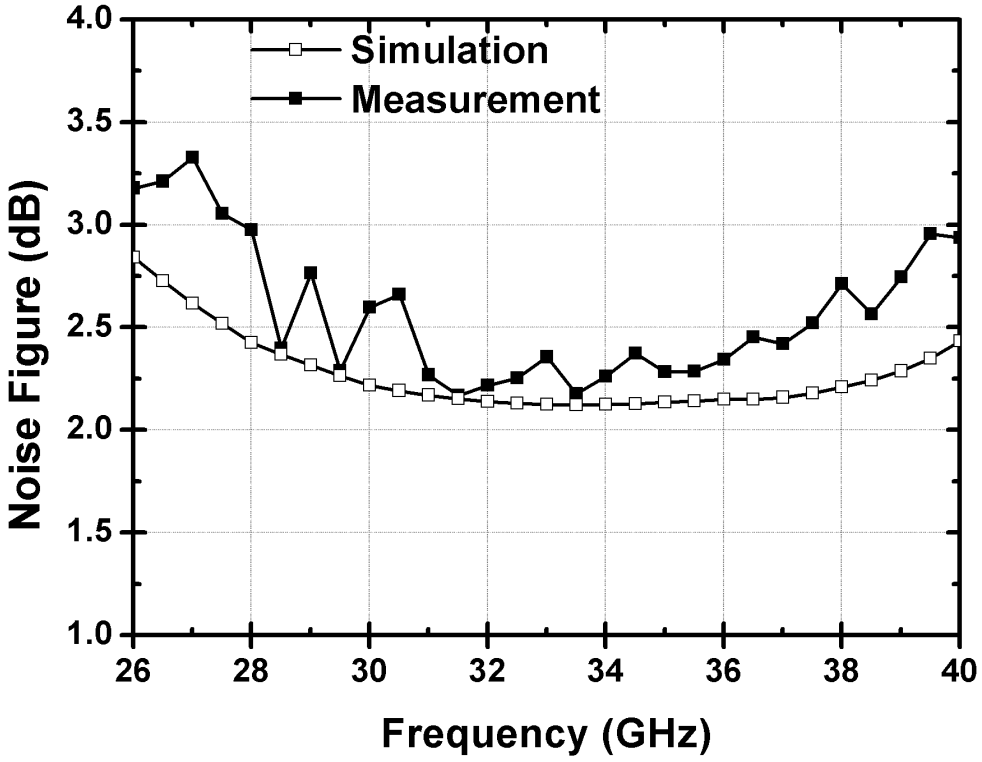

Fig. 2.42. Measured and simulated noise figure of the modified LNA, with the proposed correction applied in the simulation.

2.5 Summary

In this chapter, a Q-band LNA design for 5G receiver applications is proposed. Designed and realized in 0.15-μm pHEMT GaAs process, the proposed LNA consists of three common-source stages. Source degeneration technique using transmission lines (TL_{deg}) is adopted at the first stage for its ability of narrowing the difference between input impedances for optimal noise (Z_{opt}) and gain ($Z_{in,conj}$) performances. Thus, compromises in gain and input return loss can be minimized when input is matched for optimal noise performance. With the 8 dB gain of the first stage, noise performances of the latter stages have little impact on the noise figure of the LNA. RC-feedback technique is adopted at the latter two stages for the wideband performance it provides. All impedance matching are implemented using transmission lines. T-type matching networks are used at the first two stages, while π-type matching networks are used at the third stage for lower Q-factor during impedance transfer for a wideband performance.

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Measurement and simulation results of the proposed LNA show disagreement in S_{11}. In addition, the measurement results show a slight return gain from 17.1 to 25.6 GHz. From the measurement results of the test circuits and device test-key, the source of issue is narrowed down to the CPW-configuration device with TL_{deg}'s at the first stage. Inaccurate modeling in simulation causes the disagreement with measurement results. In order to enable an accurate and scalable modeling in simulation for future designs, correction to the simulation setups for CPW-configuration devices with TL_{deg}'s is proposed. Using the measurement results of the device test-key as a reference, the proposed correction requires a 60 μm shorter TL_{deg}'s in simulation compared to the physical layout. In order to eliminate the input return gain and verify the proposed correction, the proposed LNA is modified with elongated TL_{deg}'s at the first stage. The modified LNA is then implemented in the second tape-out using the same process. Measurement results of the modified LNA agrees well with simulation, and therefore verify the corrections made to simulation. The elongated TL_{deg}'s successfully eliminate the input return gain. As the final design, the modified LNA meets the target performances by some margin.

By adopting source degeneration at the first stage, the proposed LNA exhibits decent gain and input return loss, while the input impedance is matched for optimal noise performance. RC-feedback at the latter two stages and π-type matching networks contribute to a wide and flat gain across Q-band. The 3dB bandwidth is 15.3 GHz from 24.7 to 40.0 GHz with average gain of 22.2 dB. The gain is 21.5 dB at 38 GHz, and has flatness of 22.3 ± 1 dB from 25.7 to 37.6 GHz. The input and output return losses are above 15 dB from 37.2 to 40.4 GHz and 34.4 to 39.4 GHz, respectively. The noise figure is below 3 dB from 27.9 to 40.0 GHz, and has average of 2.6 dB from 26 to 40 GHz. Performance of LNAs can be evaluated via the figure-of-merit (FOM) [20] as

$$\text{FOM}=\frac{S_{21,\text{mag}} \times Bandwidth[\text{GHz}]}{\left(NF_{\text{mag}}-1\right)\times P_{\text{DC}}[\text{mW}]} \quad . \tag{2.2}$$

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Table 2.4 compares the proposed Q-band LNA with previously proposed K- and Q-band LNAs in III-V compound processes. The proposed Q-band LNA shows the highest FOM among the previous works using the same process in the same frequency band. References [4]-[6], [8], [10], and [11] show decent FOM due to process advantages in 0.1-μm GaAs pHEMT, GaAs mHEMT, and InP HEMT. The proposed Q-band LNA exhibits competitive wideband performance with high gain and low noise figure, in a low DC power consumption and compact layout footprint. Furthermore, the proposed LNA exhibits decent gain flatness of 22.3 ± 1 dB from 25.7 to 37.6 GHz.

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Table 2.4. Previously Reported K- and Q-band LNA designs.

Ref.	Technology	Freq. (GHz)	FBW (%)	Gain (dB)	Noise Figure (dB)	P_{DC} (mW)	FOM (GHz/mW)	Area (mm^2)
[3]	0.15-μm GaAs pHEMT	28.5-50.5	56	23	3.8	62.6	50.1	2x1.5
[4]	0.1-μm GaAs pHEMT	18.5-30	47	29	2.1	27	544.1	2x1
[5]	0.1-μm GaAs pHEMT	27-45	50	25	2.9	9	665.9	2x1
[6]	50-nm GaAs mHEMT	25-60	84	27.5	1.85	60	617.7	2x1
[7]	0.15-μm GaAs mHEMT	27.3-50.7	60	23.1	3.7	88	40.4	2x2
[8]	0.15-μm GaAs mHEMT	37-53.2	36	32.5	3.21	152	173.2	2x1
	0.15-μm GaAs mHEMT	32-50	44	29.5	2.8	140	126.6	2x1
[9]	0.12-μm GaN HEMT	33-41	22	15	3	280	0.9	1x0.7
[10]	0.1-μm GaAs HEMT	43-45	4.5	28	2.9	24	55.4	3.6x1.8*
[11]	0.2-μm InP HEMT	23-49	72	11	2.5	10	42.1	2.3x1.5
[12]	0.15-μm GaAs pHEMT	24-40	50	24	2.1	520	12.4	1.5x2.8
[13]	0.15-μm GaN T-gate DHFET	42-47	11	22	3.5	140	4.6	2.5x1.3
[14]	0.1-μm GaAs pHEMT	18-43	82	21.6	2.3	140	37.0	2x1
[15]	90-nm CMOS	30-42	33	18	5	18	19.5	0.6x0.48
This work	0.15-μm GaAs pHEMT	24.7-40.0	46	22.2	2.6	48	64.5	1.5x1

* estimated from the layout

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Chapter 3 A 60-GHz On-Off Keying Modulator with Transformer Feedback for Short Range Wireless Communications in 90-nm CMOS

In this chapter, a 60-GHz on-off keying (OOK) modulator with transformer feedback technique for high output power, gain, and on-off isolation performances designed and realized in 90-nm CMOS is presented. Based on a cascode circuit, the modulator combines the functions of modulation and output amplification of an OOK transmitter. With the proposed transformer feedback technique, the modulator achieves an OP_{1dB} of 7.0 dBm, gain of 10.2 dB, and on-off isolation of 45.4 dB at 60 GHz. For OOK modulation, data rates of up to 10 Gb/s has been measured. The modulator has die size measured at 471 x 519 μm^2 with RF and DC pads included.

3.1 Introduction

In recent years, the demand for high data rates in wireless communications has brought increasing interests towards millimeter-wave frequencies. The 60-GHz band has stood out thanks to its wide unlicensed band. Among the applications, a major focus has been on short-range, multi-Gb/s communications between mobile devices under simple modulation schemes. A wide available bandwidth means that multi-Gb/s communication is achievable even under the most basic, spectrally inefficient modulation schemes. On-off keying (OOK), as the simplest form of amplitude-shift keying (ASK), requires no additional circuit components for phase synchronization and frequency conversion. This result in a transceiver system with low complexity and DC power consumption, which is well suited for the short-range, multi-Gb/s communication applications targeted at mobile devices [21]-[28].

The power spectral density of OOK modulation is a sinc function centered at the carrier frequency with main lobe width of $2T_b$, in which T_b denotes the bit period. Therefore, data rates of up to half of the available bandwidth can be supported. With the common 9 GHz available bandwidth at the 60-GHz band in most countries, a maximum 4.5-Gb/s data rate is achievable by

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adopting OOK modulation.

Three configurations of an OOK transmitter are commonly used. In a switching-oscillator configuration, the oscillator is switched on/off in accordance with the baseband data signal [29]-[30]. Since there is no carrier signal generated at off-states, the configuration often exhibits decent on-off isolation. However, the finite response time of the oscillator to baseband data transitions often limits the maximum data rate. In another configuration, a switch-like modulator is followed by the output amplifier [31]. Carrier signal from the oscillator is modulated before feeding into the output amplifier. Muti-Gb/s data rates are often achievable using circuit structures such as shunt switches. However, switch-like modulators often suffers from low on-off isolation. Furthermore, the insertion loss of switch-like modulators often means adding a buffer amplifier for compensation, which leads to more DC power consumption and circuit components.

Switching-amplifier configuration of an OOK modulator operates by switching the output amplifier on/off in accordance with the baseband data signal [21]-[23], [32]-[33]. Modulation and amplification are performed by the same circuit, which only consumes DC power at on-states. This result in a transmitter of low DC power consumption and complexity. Critical performances of switching-amplifier configuration modulators are output power, gain, on-off isolation, and maximum data rate. Cascode circuit is commonly used for the switching-amplifier configuration. Modulation is performed by switching the gate bias of the common-gate device. However, due to leakage of the devices, cascode-based modulators often suffers from low on-off isolation.

For non-coherent OOK demodulation, the bit-error-rate (BER) is given by

$$\mathrm{BER} = \frac{1}{2}\exp\left(-\frac{E_\mathrm{b}}{2N_0}\right) + \frac{1}{4}\mathrm{erfc}\left(\sqrt{\frac{E_\mathrm{b}}{2N_0}}\right) \quad , \tag{3.1}$$

in which E_b denotes the average bit energy and N_0 the noise power spectral density [37]. Since the symbol rate equals to bit rate under binary modulations such as OOK, the ratio E_b/N_0 directly translates to the signal-to-noise ratio (SNR). For OOK transmitters, higher SNR at the receiver end

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can be achieved by either increasing the output power, or minimizing leakage at off-state while maintaining gain at on-state, i.e., increasing on-off isolation. With the former often leads to high DC power consumption, improvement in on-off isolation is commonly pursued [22]-[28], [32]-[36].

In this chapter, a 60-GHz cascode-based OOK modulator design with transformer-feedback technique is proposed. The technique improves the output power, gain performances at on-state, and isolation performance at off-state. Furthermore, the use of a transformer means a compact layout footprint is possible. While previously reported works [22], [32]-[33] often required two baseband data inputs to achieve improvements in on-off isolation, the proposed design requires only a single baseband data input. Therefore, the transmitter complexity and power consumption can be reduced for future applications.

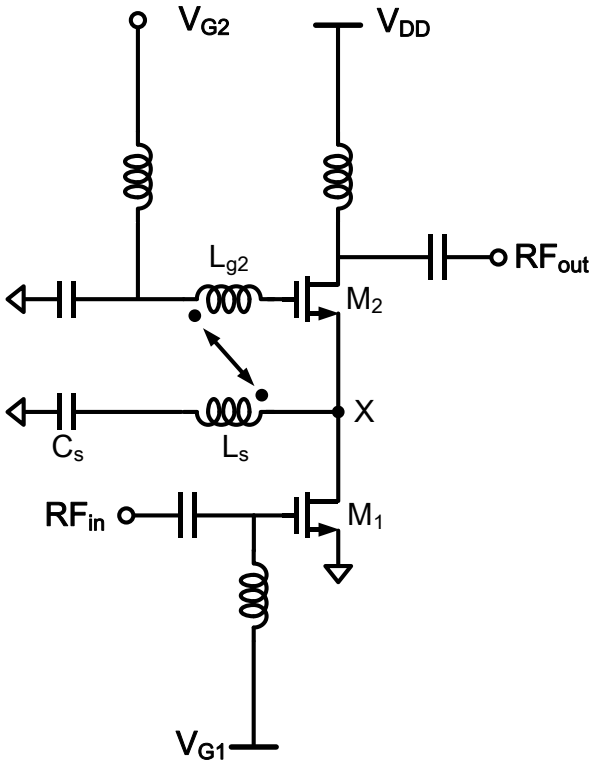

Fig. 3.1. Schematic of the proposed cascode-based transformer feedback technique.

3.2 Transformer Feedback in Cascode-Based Circuits

The proposed OOK modulator is based on a cascode circuit, upon which modulation is performed by switching the gate-bias voltage (V_{G2}) of the common-gate device, i.e., $V_{G2} = V_{G2,on}$ / 0

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V, in accordance with the baseband data being transmitted. Note that $V_{G2,on}$ is a pre-selected voltage considering the performances at on-state, as will be discussed in the section 2.3. In this section, a transformer feedback technique for cascode-based OOK modulators for improvements in output power, gain at on-state, and isolation at off-state is proposed. Transformer feedback technique for improvements in gain and noise performances in cascode-based low noise amplifier (LNA) design has been proposed in [38]. Fig. 3.1 shows the schematic of the proposed technique. The transformer consists of a shunt inductance L_s between the devices and a series inductance L_{g2} at the gate of the common-gate device with the coupling direction indicated by the arrow. In the proposed technique, L_s is a shunt as oppose to a series inductance as proposed in [26]. The configuration better suits the requirements of OOK modulator designs, as will be discussed shortly.

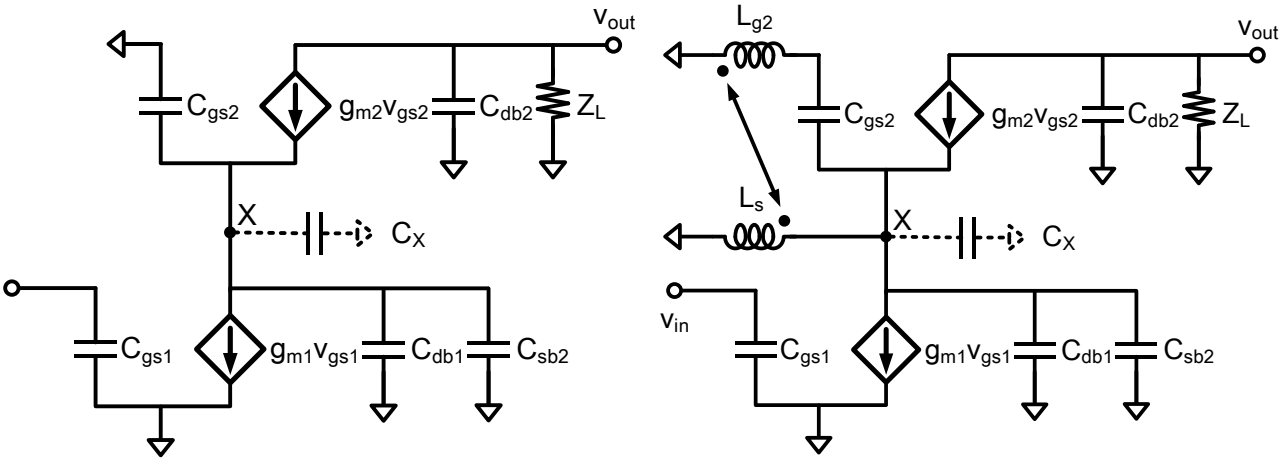

Fig. 3.2. Small-signal equivalent circuit models of a cascode circuit at on-state (a) without and (b) with the proposed transformer feedback.

3.2.1 On-state

Compared with single amplifier stages, cascode circuits have the advantage of better output power and gain performances. By stacking a common-gate device on top of a common source device, cascode circuits provide more headroom for the signal voltage swing. In other words, signal voltage swings of the common-source and common-gate devices can be superimposed for a larger voltage swing at the output. Therefore, any phase difference between the devices will significantly

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degrade the output power performance, as the voltage superimposition is not perfectly aligned. Meanwhile, a larger output impedance seen by the common-source device leads to higher voltage gain of cascode circuits. Therefore, parasitic effects that lowers the output impedance seen by the common-source device will degrade the gain performance.

Fig. 3.2(a) shows the small-signal equivalent circuit model of a cascode circuit at on-state. The parasitic capacitances from both the common-source (M_1 in Fig. 3.1) and common-gate (M_2 in Fig. 3.1) devices contributes to an effective shunt capacitance C_X at node X given by

$$C_X \approx C_{db1} + C_{sb2} + C_{gs2} \quad , \tag{3.2}$$

in which C_{db1} denotes the drain-to-body capacitance of M_1, C_{sb2} the source-to-body capacitance of M_2, and C_{gs2} the gate-to-source capacitance of M_2. The effect of C_X lowers the output impedance of M_1, and creates a phase difference between the signal voltage swings of the two devices. As mentioned before, this result in degraded output power and gain performances. As the frequency increases, especially into millimeter-wave frequencies, the effect of C_X becomes more prominent. The impedance at node X in turn becomes lower, and the phase difference becomes greater.

Fig. 3.2(b) shows the small-signal equivalent circuit model of a cascode circuit at on-state with the proposed transformer feedback. Here, L'_s and L'_{g2} denote the equivalent inductances of L_s and L_{g2} in Fig. 3.1 with the effect of transformer coupling considered, respectively. The admittance at node X is denoted as $G_X + jB_X$, which is given by

$$G_X = (1 - \frac{j\omega L'_{g2}}{j\omega L'_{g2} + \frac{1}{j\omega C_{gs2}}}) g_{m2} = (1 + \frac{\omega L'_{g2}}{-\omega L'_{g2} + \frac{1}{\omega C_{gs2}}}) g_{m2} \quad , \tag{3.3}$$

and

$$jB_X = \frac{1}{j\omega L'_{g2} + \frac{1}{j\omega C_{gs2}}} + \frac{1}{j\omega L'_s} + j\omega C_{sb2} + j\omega C_{db1} \quad . \tag{3.4}$$

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The conductance G_X at node X directly translate to the effective transconductance of M_2 seen by M_1. As can be seen from (3.3), the effective transconductance can be improved if the condition in

$$-\omega L'_{g2}+\frac{1}{\omega C_{gs2}}<0 \tag{3.5}$$

is satisfied.

To eliminate the effect of the parasitic shunt capacitance C_X, the admittance at node X should consists only the real part. In other words, the susceptance B_X has to be eliminated. From (3.4), we have

$$\begin{aligned} B_X &= -\frac{1}{\omega L'_{g2}-\frac{1}{\omega C_{gs2}}}-\frac{1}{\omega L'_s}+\omega C_{sb2}+\omega C_{db1} \\ &= -\frac{\omega(L'_s+L'_{g2})-\frac{1}{\omega C_{gs2}}-\omega(C_{sb2}+C_{db1})(\omega L'_{g2}-\frac{1}{\omega C_{gs2}})\omega L'_s}{(\omega L'_{g2}-\frac{1}{\omega C_{gs2}})\omega L'_s} \end{aligned}, \tag{3.6}$$

the numerator of which should equal to 0 for the effect of C_X to be eliminated. Thus, a careful designed transformer parameters consisting of inductances L_s, L_{g2}, and coupling coefficient K that satisfies the conditions in (3.5) and (3.6) should provide an improvement in output power and gain performances.

Fig. 3.3 shows the simulated MSG/MAG and stability factor of a cascode circuit at on-state with different configurations of the transformer. Device with 20f x 2 μm gate-periphery is used for both M_1 and M_2, and ideal inductors are used for the simulation. As can be seen, different transformer configurations provide varying improvements in both MSG/MAG and stability. The improvement in MSG/MAG increases with the transformer inductance, while the cascode circuit starts to exhibit potential instability at higher frequencies. This is due to the higher inductance of L_{g2} starts to appear as an open circuit at the gate of M_2 seen by the higher frequencies. Therefore, careful design during matching is required if larger inductances for the transformer are to be used.

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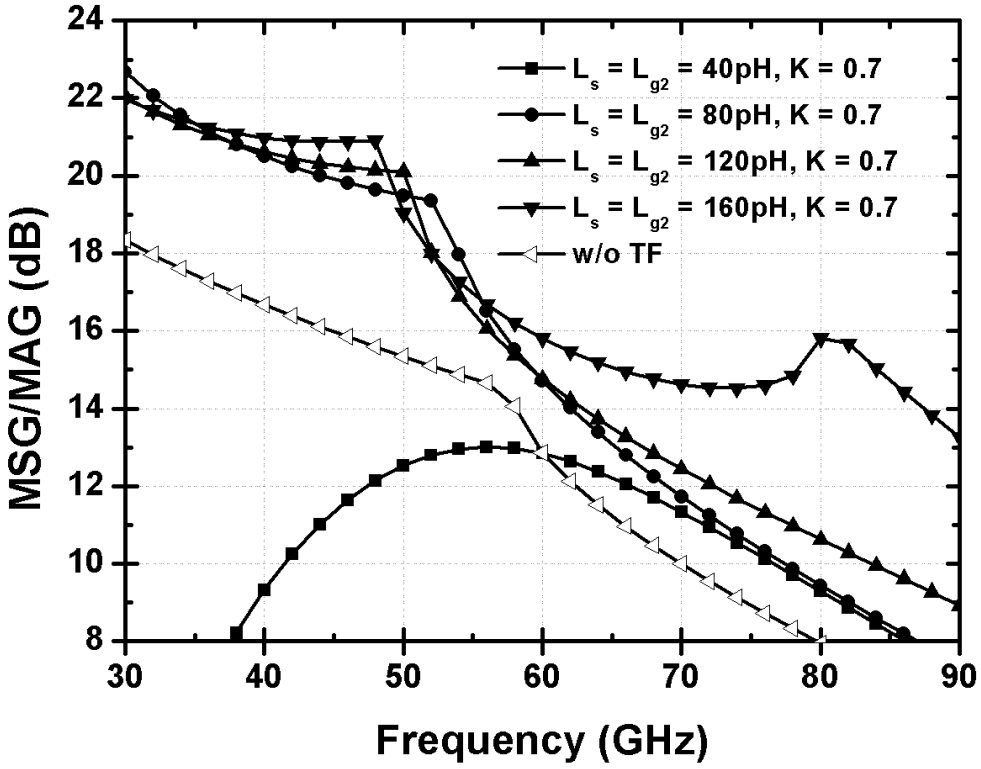
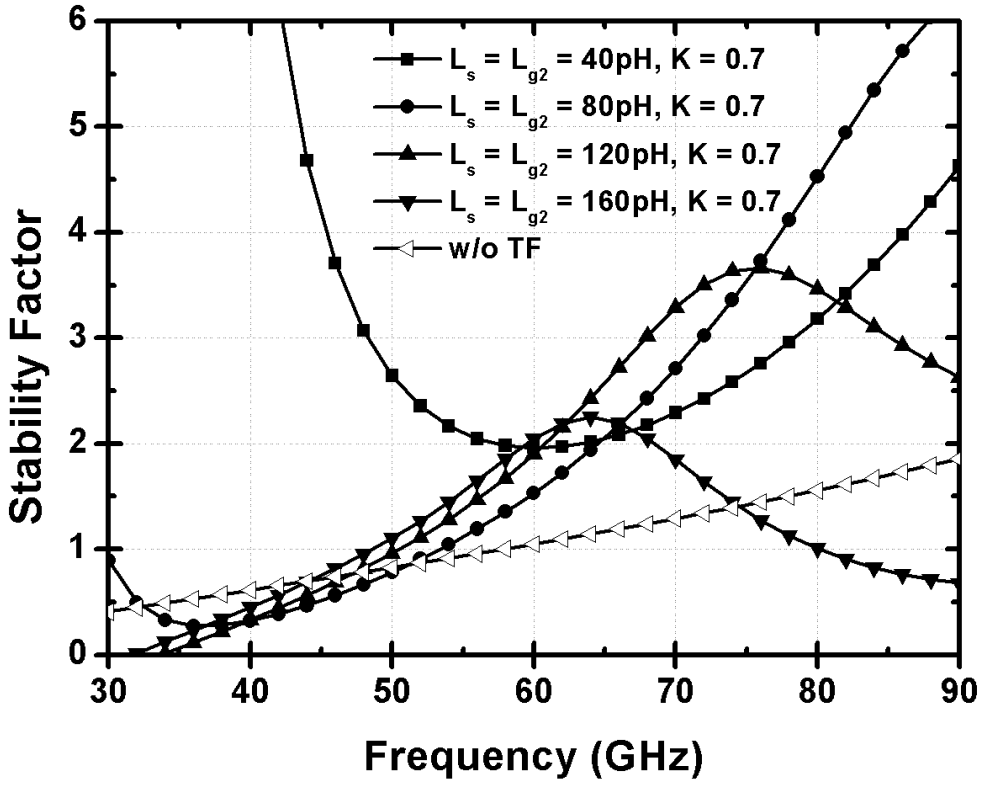


(a)



(b)

Fig. 3.3. Simulated (a) MSG/MAG and (b) stability factor of the cascode circuit with different configurations of the transformer.

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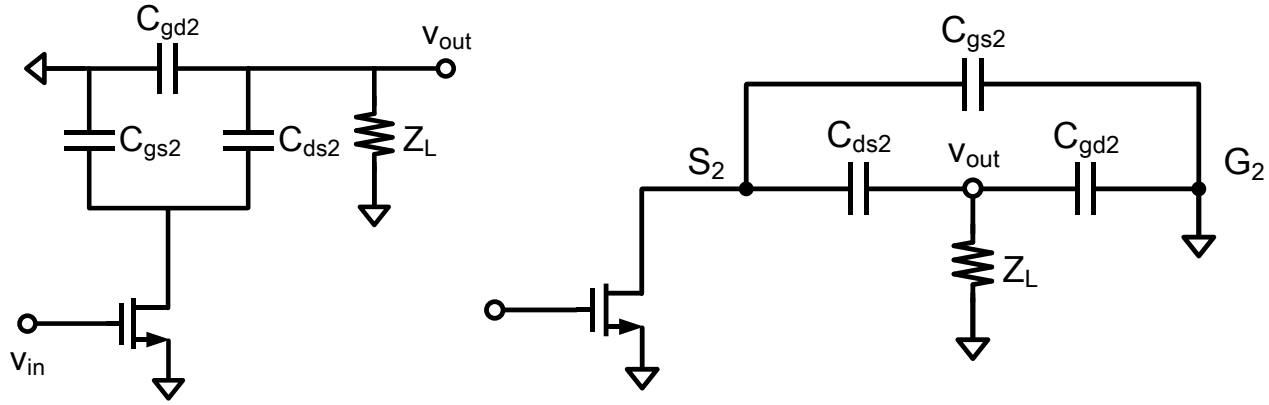
3.2.2 Off-state

Fig. 3.4(a) shows the small-signal equivalent circuit model of a cascode circuit at off-state, i.e., V_{G2} = 0 V. Since the improvement in isolation provided by the proposed transformer feedback focuses on the common-gate device (M_2), we omit the small-signal model of the common-source device (M_1) for clarity. At off-state, leakage signal from M_1 enters the source of M_2 towards the output. Improvement in isolation means minimizing the signal power at the output. For the purpose of an easier analysis, Fig. 3.4(b) shows a rearranged version of Fig. 3.4(a). From the symmetric nature of the small-signal model shown in Fig. 3.4(b), we first assume the same capacitance for C_{ds2} and C_{gd2}. As can be seen, if a signal of equal amplitude and 180° phase difference compared with the leakage signal, i.e., signal at node S_2, can be introduced at node G_2, signal amplitude at the output can be minimized.



(a) (b)

Fig. 3.4. Small-signal equivalent circuit models of a cascode structure at off-state.

Fig. 3.5 shows the small-signal equivalent circuit model of a cascode circuit at off-state with the proposed transformer feedback. The desired effect is realized by the opposite coupling direction of the proposed transformer. Although an assumption of equal capacitance for C_{ds2} and C_{gd2} was made earlier, careful design of the inductances L_s and L_{g2} can mitigate the capacitance difference and creates the desired 180° phase difference to the leakage signal. Since a larger coupling coefficient, i.e., K closer to 1, of the transformer directly translate to a signal magnitude at node G_2 closer to that of the leakage signal, a larger coupling coefficient directly benefits the isolation

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performance.

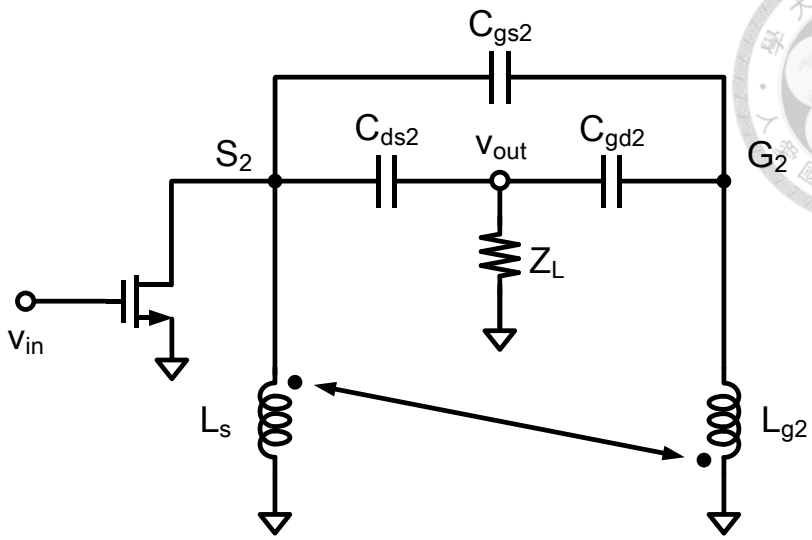

Fig. 3.5. Small-signal equivalent circuit model of a cascode structure at off-state with the proposed transformer feedback.

Fig. 3.6 shows the simulated phase difference between node S_2 and G_2 versus different input power levels (P_{in}) at 60 GHz. By adopting the transformer feedback, we successfully introduce a 180° phase difference between the nodes, and the phase difference is closer to 180° as the coupling coefficient increases. The phase difference remain relatively constant regardless of P_{in}. Fig. 3.7 shows the simulated signal power at S_2 and G_2 (in dBm) versus different P_{in} at 60 GHz. Varying the coupling coefficient makes little difference in signal power at S_2, which is nearly identical to the case without the transformer as expected. As mentioned above, the signal power at G_2 increases with the coupling coefficient. Fig. 3.8 shows the simulated signal power at the output node versus different P_{in} at 60 GHz. The signal power at output decreases as the coupling coefficient increases, and shows a linear behavior relationship. Thus, a larger coupling coefficient directly benefits the isolation performance regardless of P_{in} levels. For assessing isolation performance across different frequencies, –MSG/MAG (in dB) is used as a worst-case representation of isolation. Fig. 3.9 shows the simulated MSG/MAG of a cascode circuit at off-state with different transformer coupling coefficients. As expected, a larger coupling coefficient directly benefits the isolation performance. Furthermore, the improvement in isolation bandwidth is relatively wide with a broadband transformer.

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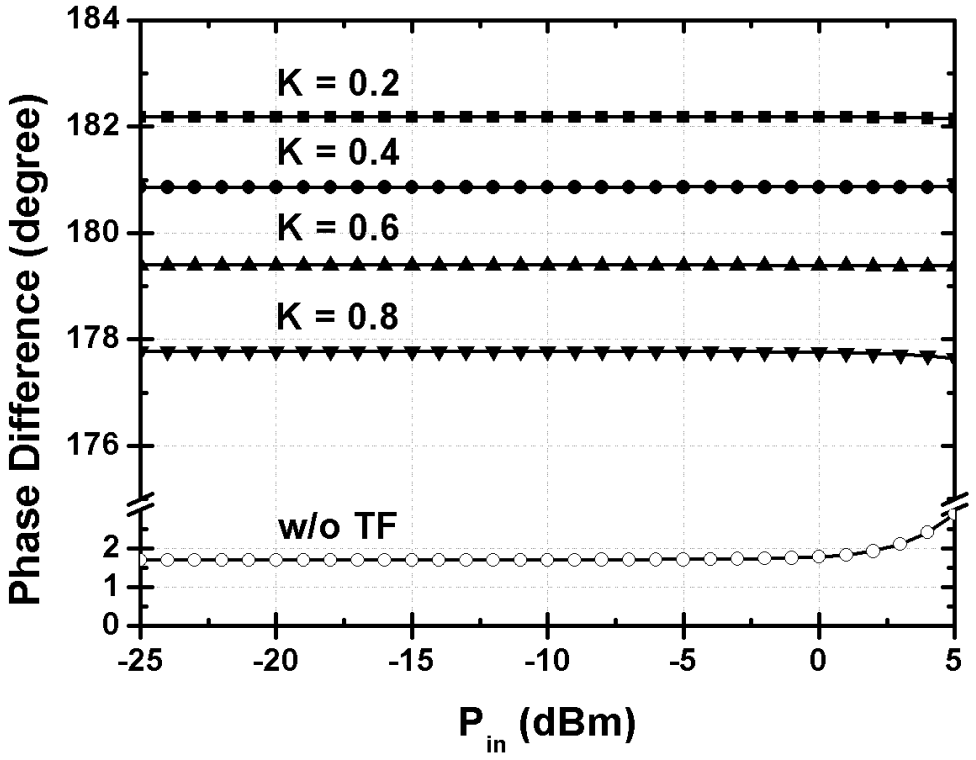

Fig. 3.6. Simulated phase difference between node S_2 and G_2 versus different P_{in} levels at 60 GHz.

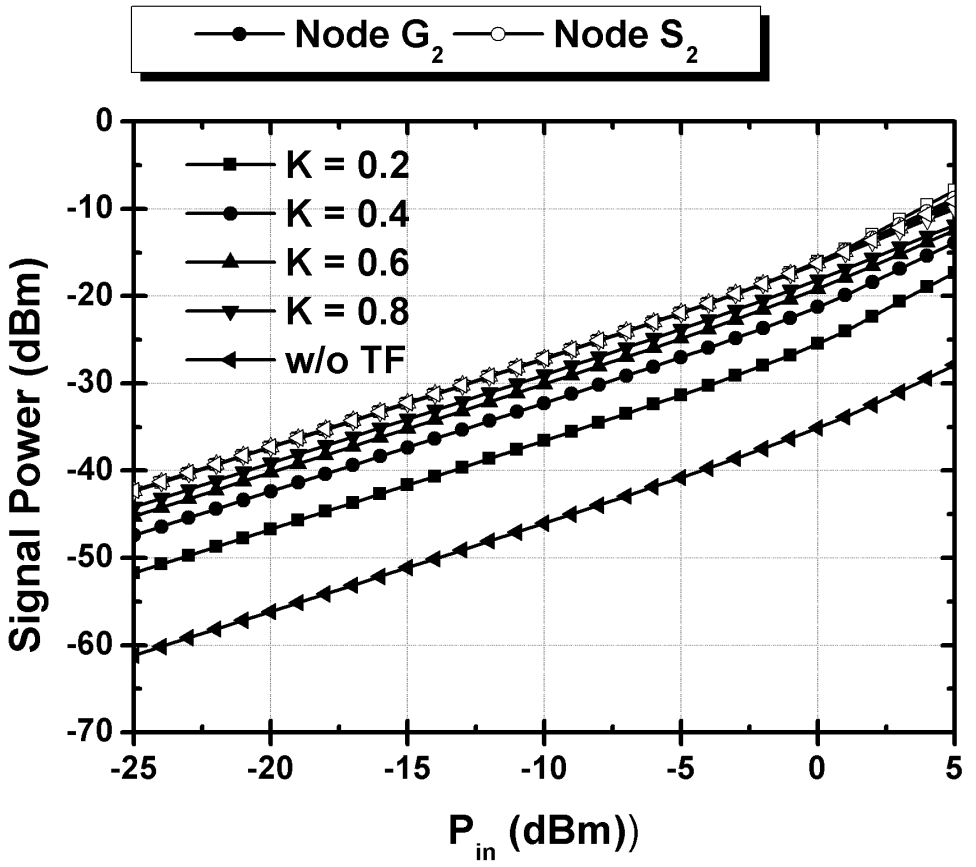

Fig. 3.7. Simulated signal power at S_2 and G_2 (in dBm) versus different P_{in} levels at 60 GHz.

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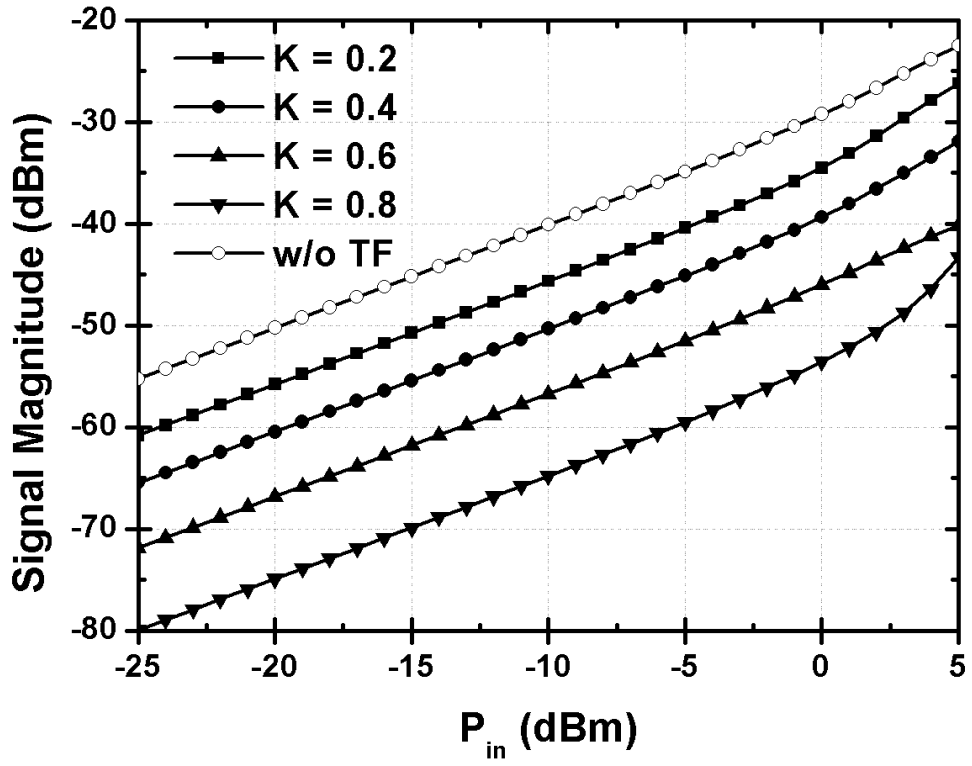

Fig. 3.8. Simulated signal magnitude at the output node (in dBm) at 60 GHz.

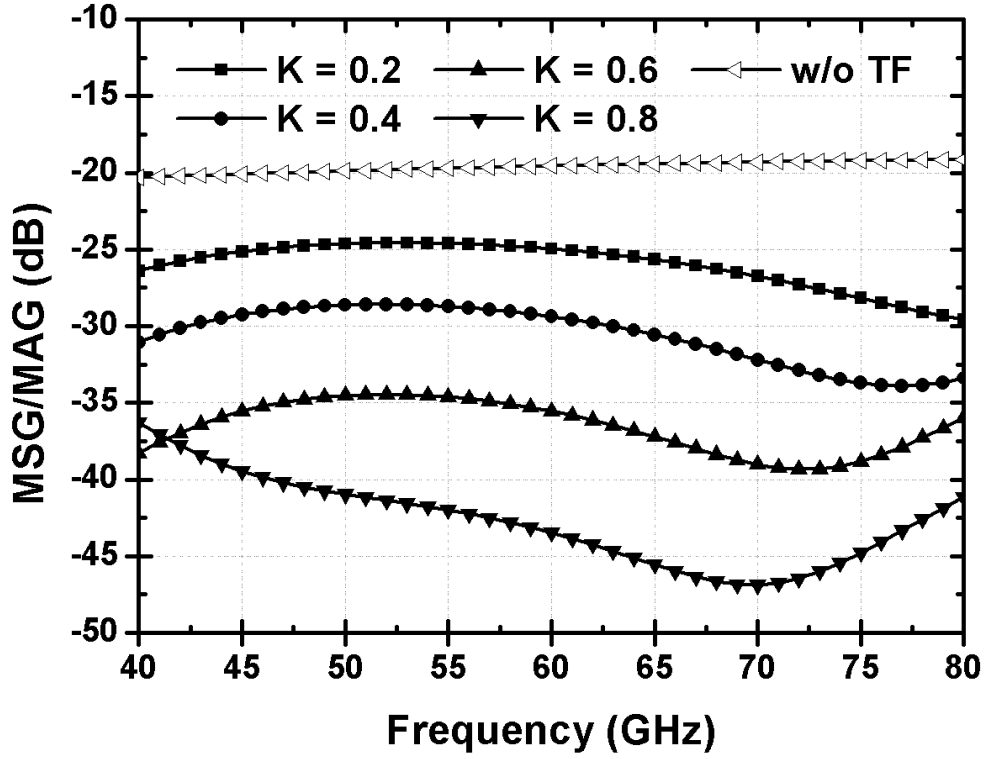

Fig. 3.9. Simulated MSG/MAG of a cascode circuit at off-state with different transformer coupling coefficients.

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3.3 Circuit Design

Fig. 3.10 shows the schematic of the proposed 60-GHz OOK modulator. The modulator is based on a cascode circuit consisting of a common-source device M_1 and a common-gate device M_2. The baseband data signal is applied to the gate of M_2, switching M_2 on/off, i.e., $V_{G2} = V_{G2,on}/0$ V, in accordance with the data sequence being transmitted. The proposed transformer feedback consists of a shunt inductor L_s at node X between the devices, and a series inductor L_{g2} at the gate of M_2.

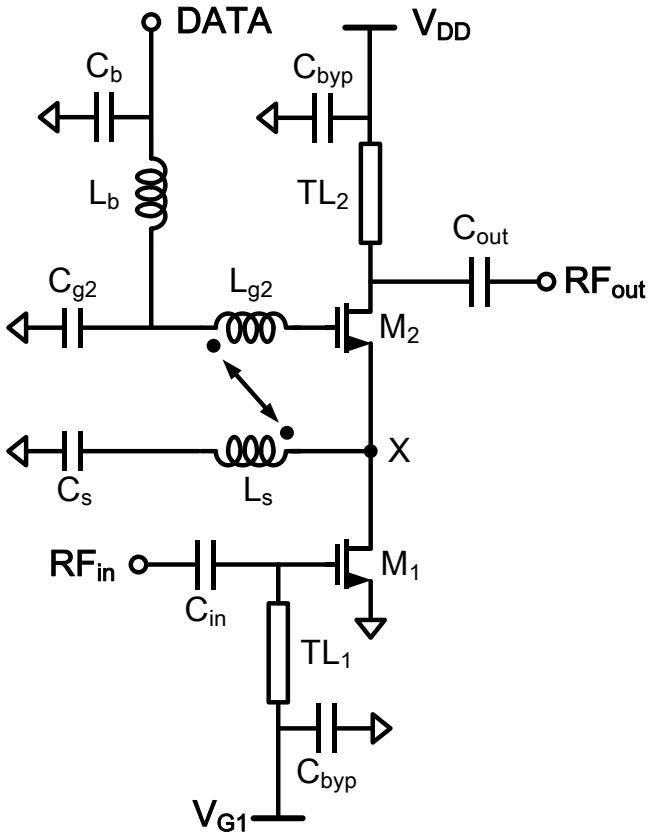

Fig. 3.10. Schematic of the proposed OOK modulator.

3.3.1 Bias Condition and Device Selection

As the proposed modulator combines the functions of modulation and output amplification, several tradeoffs have to be considered when selecting the desired device gate-periphery. Larger device gate-periphery comes with larger output power and stability, but lower gain and off-state

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isolation. Furthermore, since the gate parasitic capacitance of the device increases with gate-periphery, maximum data rate, i.e., the rate at which the device can be switched on/off, also suffers from selecting a large gate-periphery. Table 3.1 lists the critical and target performances of the proposed modulator.

Table 3.1. Target performance of the proposed modulator.

Frequency	**Gain**	**On-off isolation**	**OP_{1dB}**	**Data Rate**
60 GHz	8 dB	35 dB	6 dBm	8 Gb/s

Identical gate-peripheries and symmetric bias conditions, i.e., $V_{G2,on} = V_{G1} + V_{DD} / 2$, are assumed for M_1 and M_2 throughout the following process for simplicity of design. The saturated output power (P_{sat}) can be estimated using the load-line theory as

$$P_{sat} = \frac{1}{2} \times \frac{V_{max} - V_{min}}{2} \times \frac{I_{max}}{2}. \tag{3.7}$$

However, in the case of a cascode circuit, the estimation assumes ideal voltage superimposition between the two devices while any possible mismatch can degrade the output power. Furthermore, additional loss of the output matching network has to be considered. Fig 2.11 shows the DC-IV curves of the cascode circuit with two identical device gate-peripheries of 20f x 2 μm. From (3.7), a P_{sat} of around 9 dBm can be estimated at V_{DD} = 2.0 V, i.e., $V_{DS1} = V_{DS2}$ = 1.0 V. This provides enough margin for the targeted OP_{1dB} performance of 6 dBm. Fig 2.12 shows the g_m and I_{DS} of a 20f x 2 μm device in common-source configuration versus different V_{GS} at V_{DS} = 1.0 V. The device reached peak g_m at V_{GS} = 0.8 V. For a better performance at on-state, V_{GS} of both M_1 and M_2 are therefore set to 0.8 V, i.e., V_{G1} = 0.8 V, $V_{G2,on} = V_{G1} + V_{DD} / 2$ = 1.8 V. However, setting a relatively high $V_{G2,on}$ = 1.8 V means a peak-to-peak voltage ($V_{p\text{-}p}$) of 1.8 V is required of the baseband data signal to switch M_2 on/off. This potentially poses burden on the baseband circuit and may compromises the maximum data rate.

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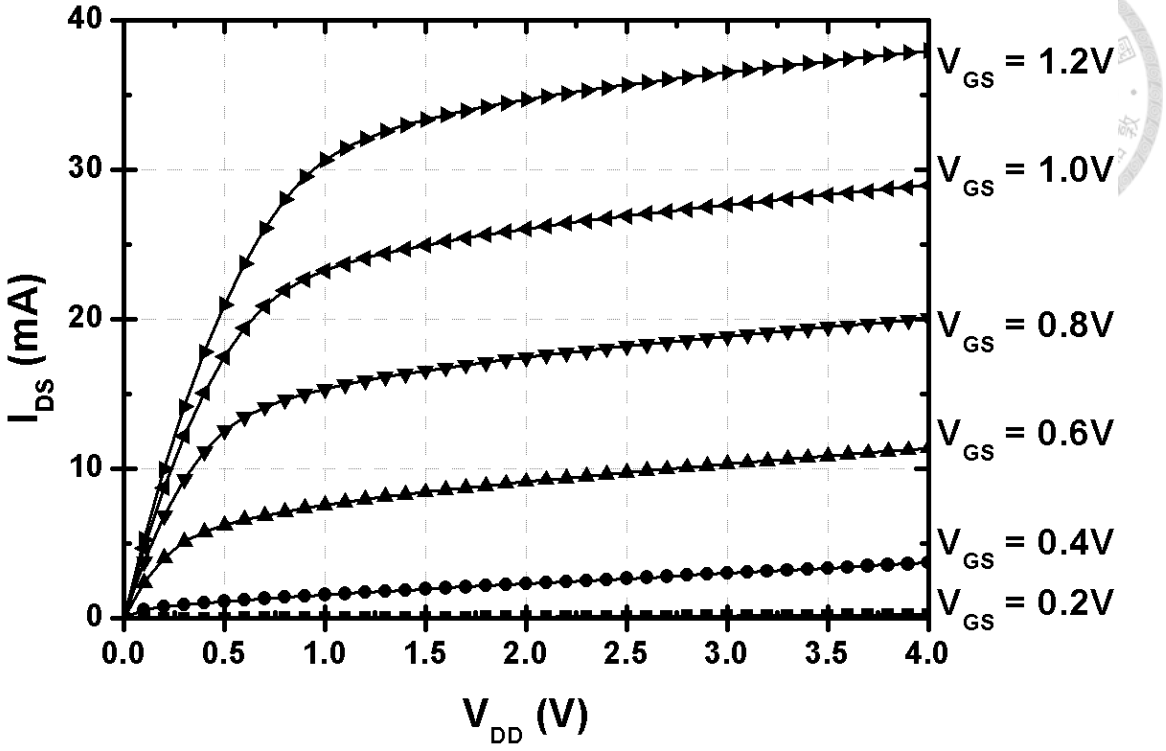

Fig. 3.11. Simulated DC-IV curves of the cascode circuit with two identical device gate peripheries of 20f x 2 μm.

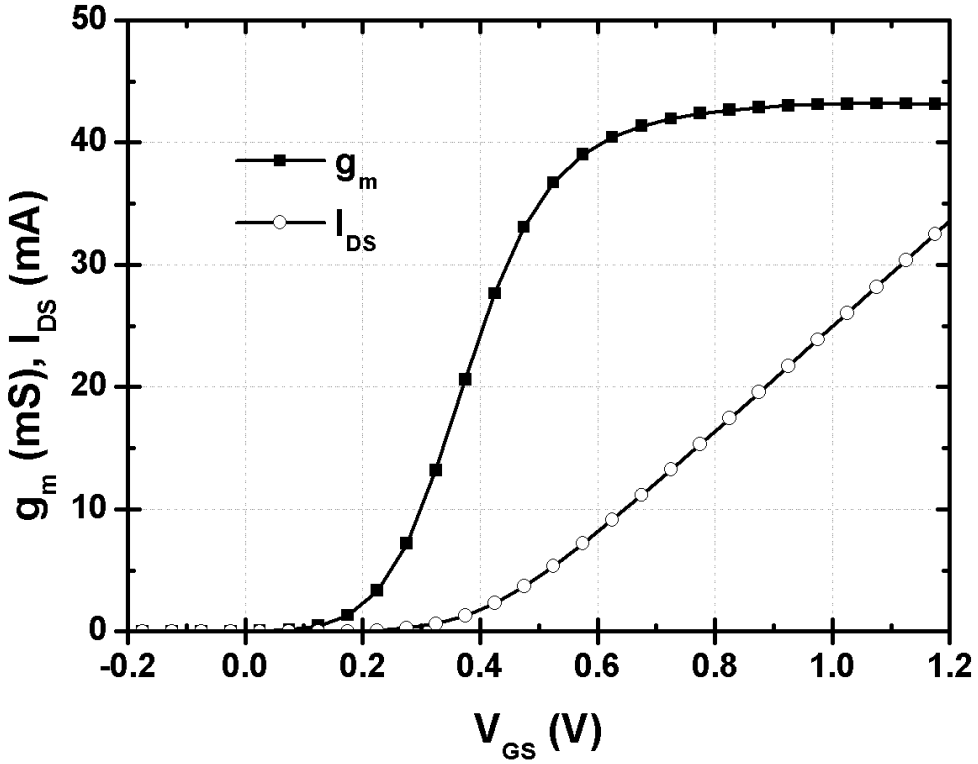

Fig. 3.12. Simulated g_m and I_{DS} of a 20f x 2 μm device in common-source configuration versus different V_{GS} at V_{DS} = 1.0 V.

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Different configurations of a total 40 μm gate-periphery is then compared at the selected bias condition of [V_{G1}, $V_{G2,on}$, V_{DD}] = [0.8 V, 1.8 V, 2.0 V]. Fig. 3.13 shows the simulated MSG/MAG and stability factor of the cascode circuit. Since both the gate parasitic capacitance and resistance effect the maximum data rate, 20f x 2 μm is preferred for its lower gate parasitic resistance over the 10f x 4μm configuration. The higher gain of 20f x 2μm is preferred over the 40f x 1μm. Since the selected cascode circuit with 20f x 2 μm device is potentially unstable at 60 GHz, a shunt capacitor C_{g2} of 150 fF is added to the gate of M_2. Fig 2.13 shows the simulated MSG/MAG and stability factor of the cascode circuit after the addition of C_{g2}.

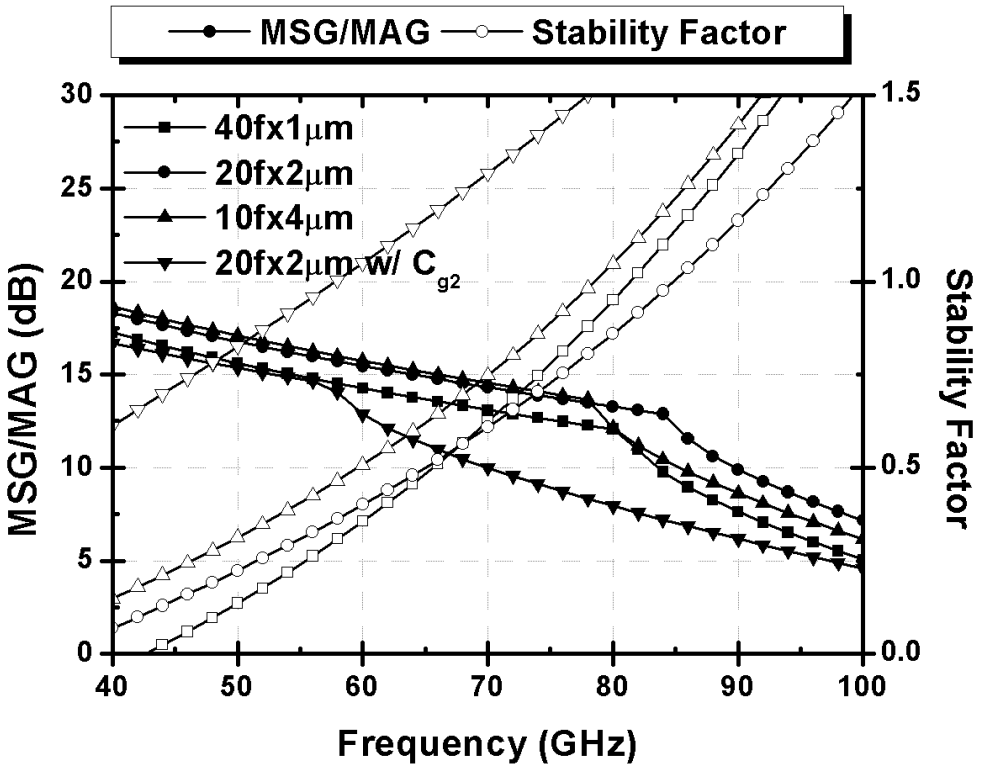

Fig. 3.13. Simulated MSG/MAG and stability factor of the cascode circuit with different configurations of a total 40 μm gate-periphery.

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3.3.2 Transformer Design

As discussed in section 3.2, a larger coupling coefficient of the transformer directly benefits the isolation performance at off-state, and also improves the output power and gain performances at on-state with careful design. Therefore, we assume a reasonable coupling coefficient of 0.65 during initial simulations using ideal inductors. Higher coupling coefficient is further pursued during the physical layout and EM simulations of the transformer, as will be discussed later in the section.

For assessing gain performance at on-state, we assume an initial inductance of 60 pH for the primary coil (L_s in Fig. 3.10), and varies the inductance of the secondary coil (L_{g2} in Fig. 3.10). Fig. 3.14 and Fig. 3.15 shows the simulated MSG/MAG and stability factor at of the cascode circuit on-state, respectively. The cascode circuit exhibits lower gain and higher stability at 60 GHz as L_{g2} increases, but the improvement in MSG/MAG by adopting the transformer feedback is present regardless of the inductance value. This indicates a decent choice of initial inductance 60 pH for L_s. An initial inductance of 60 pH is then assumed for L_{g2} with varying inductance of L_s. Fig. 3.16 and Fig. 3.17 shows the simulated MSG/MAG and stability factor at of the cascode circuit on-state, respectively. On the contrary, the cascode circuit exhibits lower gain and higher stability at 60 GHz as L_s decreases with the improvement in MSG/MAG still present.

For assessing isolation performance at off-state, we perform the same process for simulation as at on-state. –MSG/MAG (in dB) is used as a worst-case representation of isolation. Fig. 3.18 and Fig. 3.19 show the simulated MSG/MAG at off-state with varying inductances of L_{g2} and L_s, respectively. As discussed in section 3.2, the inductances of L_{g2} and L_s mitigates the capacitance difference between C_{ds2} and C_{gd2} to realize the desired 180° phase difference to the leakage signal. As can be seen, the case of [L_s, L_{g2}] = [60 pH, 80 pH] in Fig. 3.18 and [L_s, L_{g2}] = [40 pH, 60 pH] in Fig. 3.19 exhibits the best isolation performances. Therefore, in order to have a decent isolation performance at off-state, the inductance of L_{g2} needs to be slightly larger than L_s.

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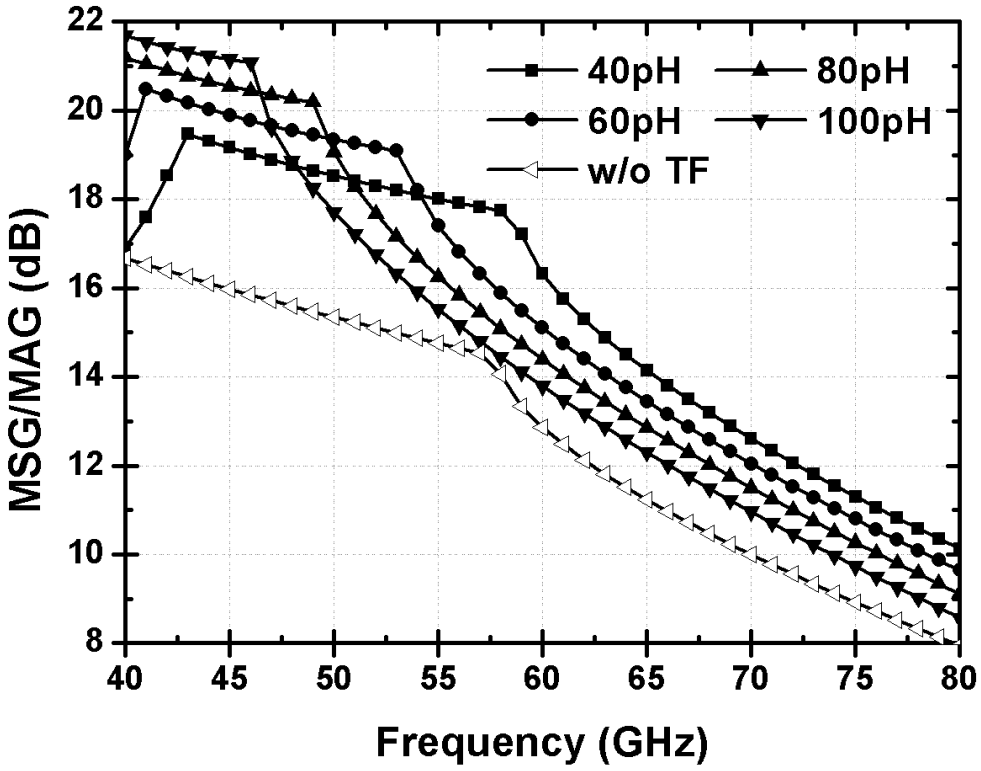

Fig. 3.14. Simulated MSG/MAG of the cascode circuit at on-state with fixed L_s = 60 pH and varying L_{g2} from 40 to 100 pH.

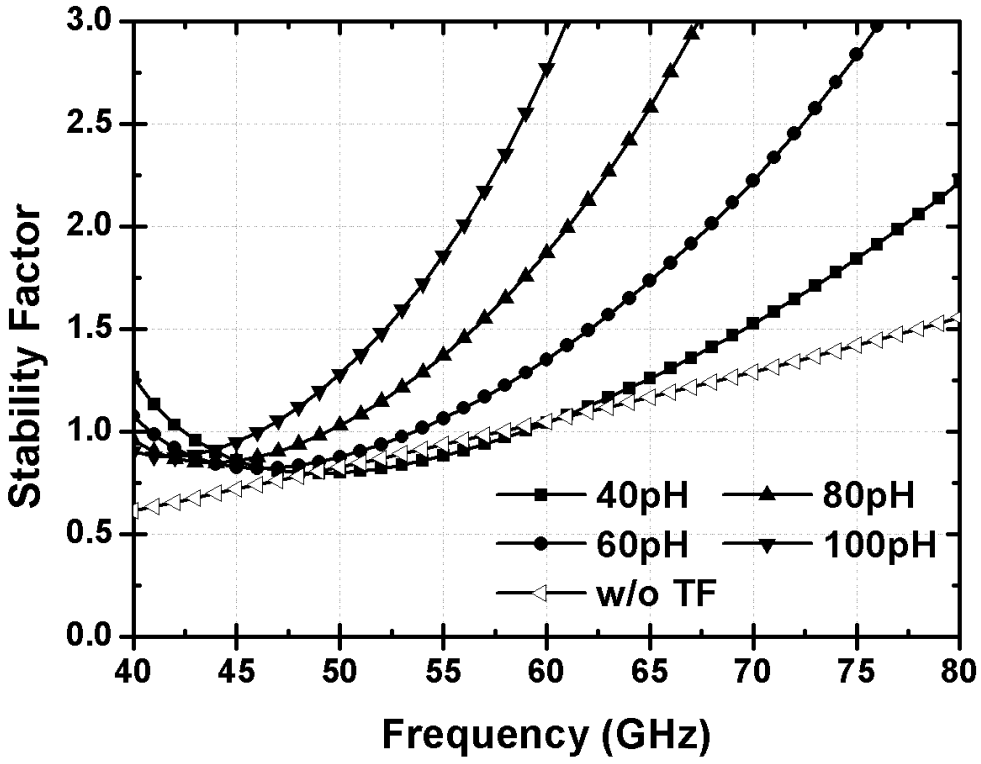

Fig. 3.15. Simulated stability factor the cascode circuit at on-state with fixed L_s = 60 pH and varying L_{g2} from 40 to 100 pH.

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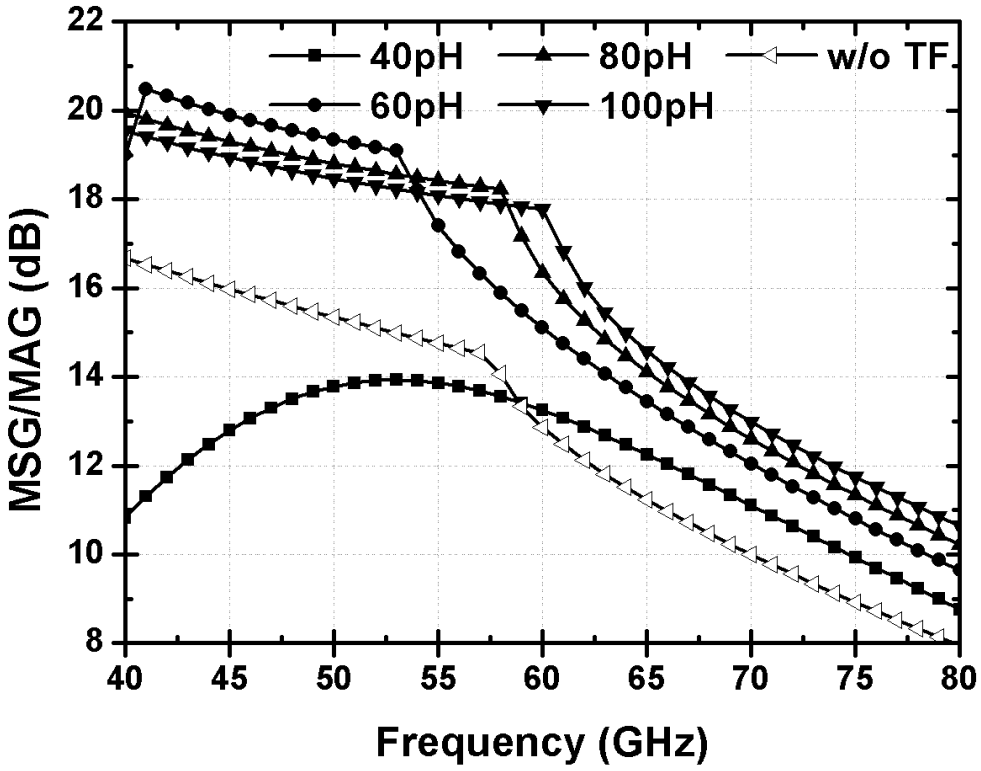

Fig. 3.16. Simulated MSG/MAG of the cascode circuit at on-state with fixed L_{g2} = 60 pH and varying L_s from 40 to 100 pH.

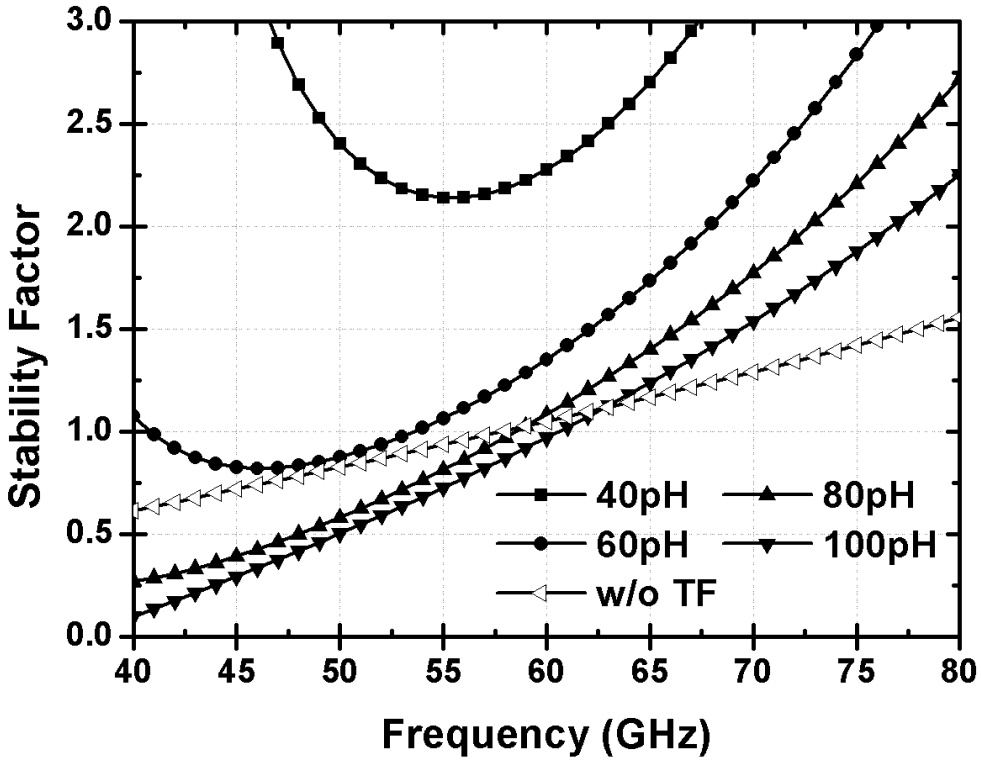

Fig. 3.17. Simulated stability factor of the cascode circuit at on-state with fixed L_{g2} = 60 pH and varying L_s from 40 to 100 pH.

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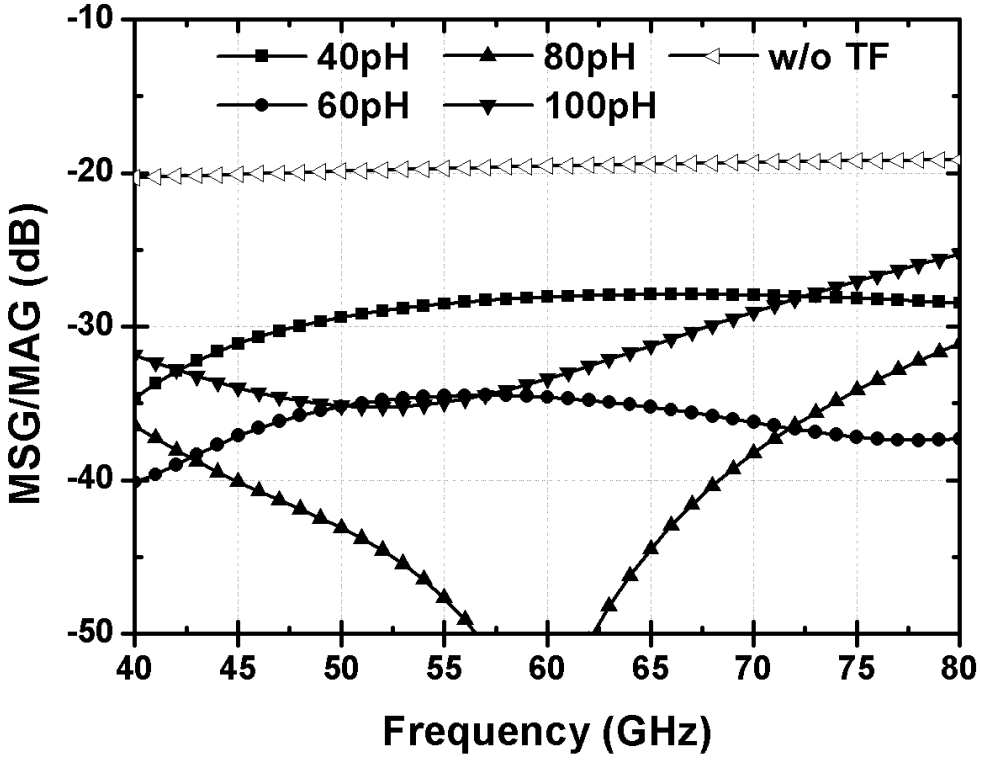

Fig. 3.18. Simulated MSG/MAG of the cascode circuit at off-state with fixed L_s = 60 pH and varying L_{g2} from 40 to 100 pH.

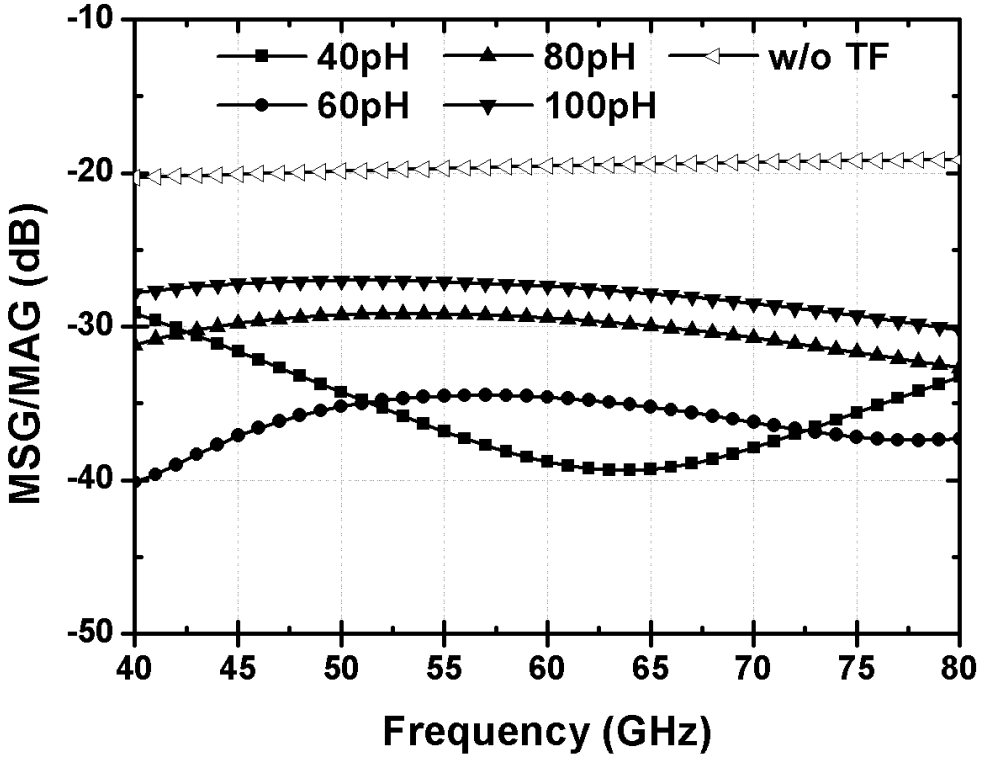

Fig. 3.19. Simulated MSG/MAG of the cascode circuit at on-state with fixed L_{g2} = 60 pH and varying L_s from 40 to 100 pH.

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From the above discussion, a transformer with L_s = 65 pH and L_{g2} = 70 pH is adopted for the proposed modulator for a balanced performances between on/off-state, and a compact physical layout. The transformer is realized using the metal-9 layer (top layer, 3.4-μm thick) for L_s, and metal-8 layer (0.85-μm thick) for L_{g2} in 90-nm CMOS process for low insertion loss. The ground plane (metal-1) underneath the transformer is removed to prevent undesired coupling of field. The two coils are physically identical with no offset in position for higher coupling coefficient. The in- and output of the primary and secondary coils are placed on the same side due to layout considerations. Fig. 3.20 shows the post-EM simulated parameters of the transformer. The inductances of the primary and secondary coils remain relatively constant from 40 to 80 GHz. The transformer exhibits a high and relatively constant coupling coefficient above 0.75 from 40 to 80 GHz. Fig. 3.21 and Fig. 3.22 shows the post-EM simulated performances of the cascode circuit at on- and off-states, respectively. At on-state, the transformer feedback improves both the circuit stability, and MSG/MAG by 3.5 dB at 60 GHz. At off-state, improvement in isolation is above 10 dB from 40 to 80 GHz. This result in a 13.5-dB improvement in on-off isolation at 60 GHz by adopting the transformer feedback technique.

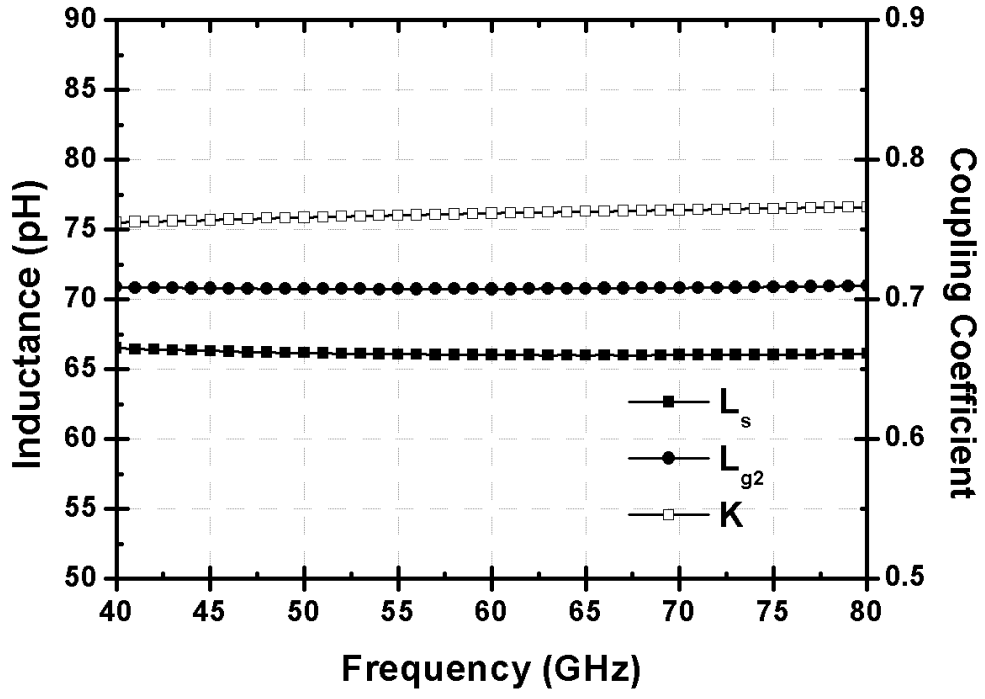

Fig. 3.20. Post-EM simulated parameters of the feedback transformer.

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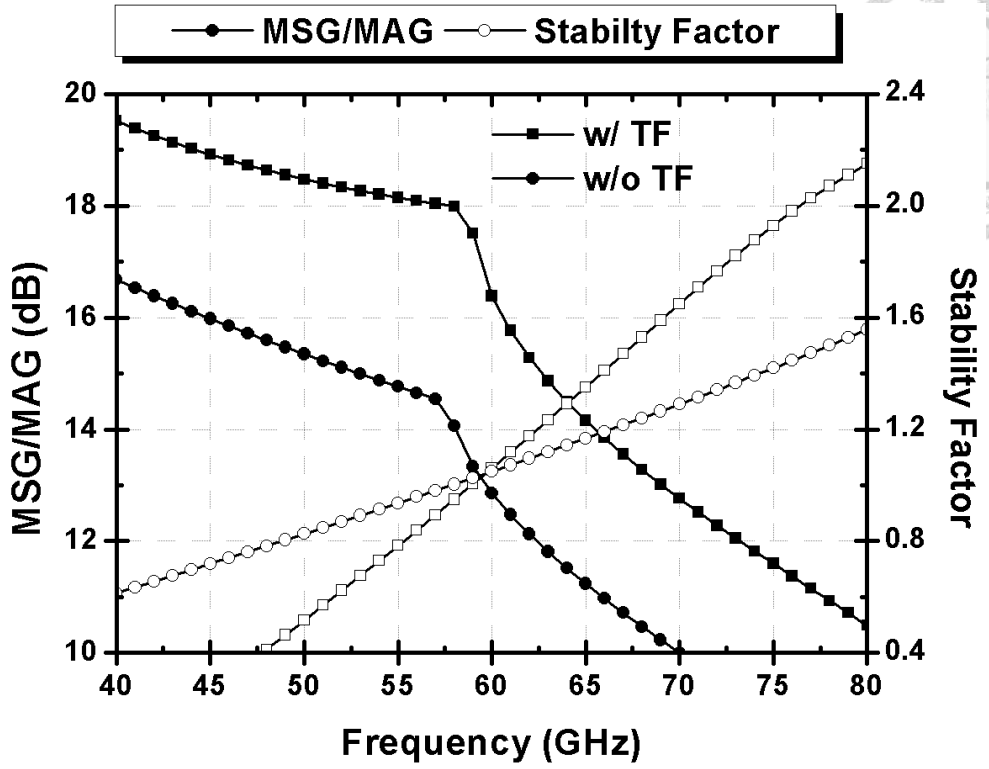

Fig. 3.21. Post-EM simulated MSG/MAG and stability factor of the cascode circuit with transformer feedback at on-state.

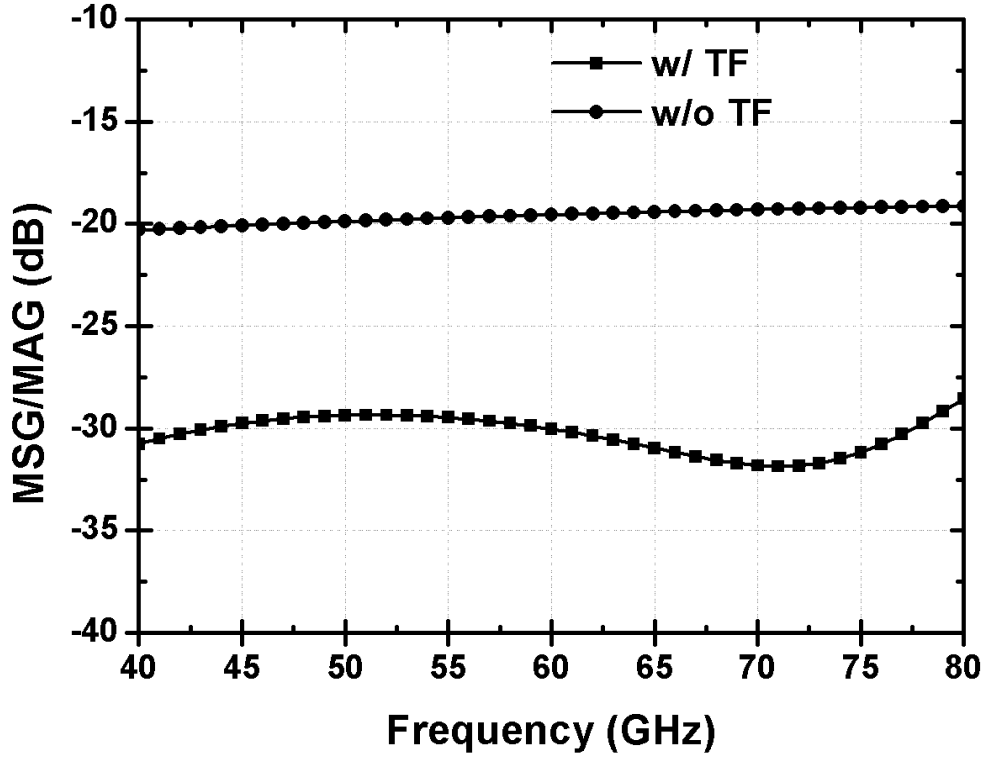

Fig. 3.22. Post-EM simulated MSG/MAG of the cascode circuit with transformer feedback at off-state.

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3.3.3 In/Output Matching and Baseband Data Input Network

Since the proposed modulator serves the role of an output amplifier at on-state, the in/output matching is designed as such. The output is matched for maximum P_{sat} and then input is matched for maximum gain, i.e., conjugate matching. As shown in Fig. 3.10, both in- and output matching networks are realized using a series capacitor and a short stub. Inter-digital capacitors composed of the top metal layers are used for the small capacitance required for matching. Bypass networks in the form of shunt MIM capacitors are placed at the end of the short stubs.

As shown in Fig. Fig. 3.10, the baseband data signal is applied to the gate of M_2. The time-constant (τ) at the baseband data input network is given by

$$\tau = RC = \frac{1}{2\pi f_c} \quad , \tag{3.8}$$

in which f_c denotes the cutoff frequency, R denotes the total resistance and C the total capacitance seen by the baseband data signal. A low cutoff frequency leads to distortion of the baseband data signal at higher data rates, and therefore limits the maximum data rate. The time-constant seen by the baseband data signal must be kept small for a higher maximum data rate. Therefore, the baseband data input network needs to provide not only an open circuit for the carrier frequencies, but also a low time-constant to the baseband data signal. Since using a large resistor for gate biasing results in a large time-constant, an inductor L_b with a bypass capacitor C_b is used instead to create an open-circuit for the carrier frequencies. Since C is often dominated by the gate parasitic capacitance of the device, the method greatly reduce the time-constant compared to using a resistor for gate biasing despite the added bypass capacitance of C_b.

3.3.4 EM Simulation

The physical layout around the devices of a cascode circuit often limits the possibility of including all the passive elements into a single run of EM simulation. However, since the proposed modulator requires relatively complicated physical layout around the devices including the feedback

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transformer, we manage to consider as much elements in a single run of EM simulation for accurate modeling of the passive elements. Fig. 3.23 shows the 3-D rendering of the area around the devices used for EM simulation, as indicated by the grey area in the schematic.

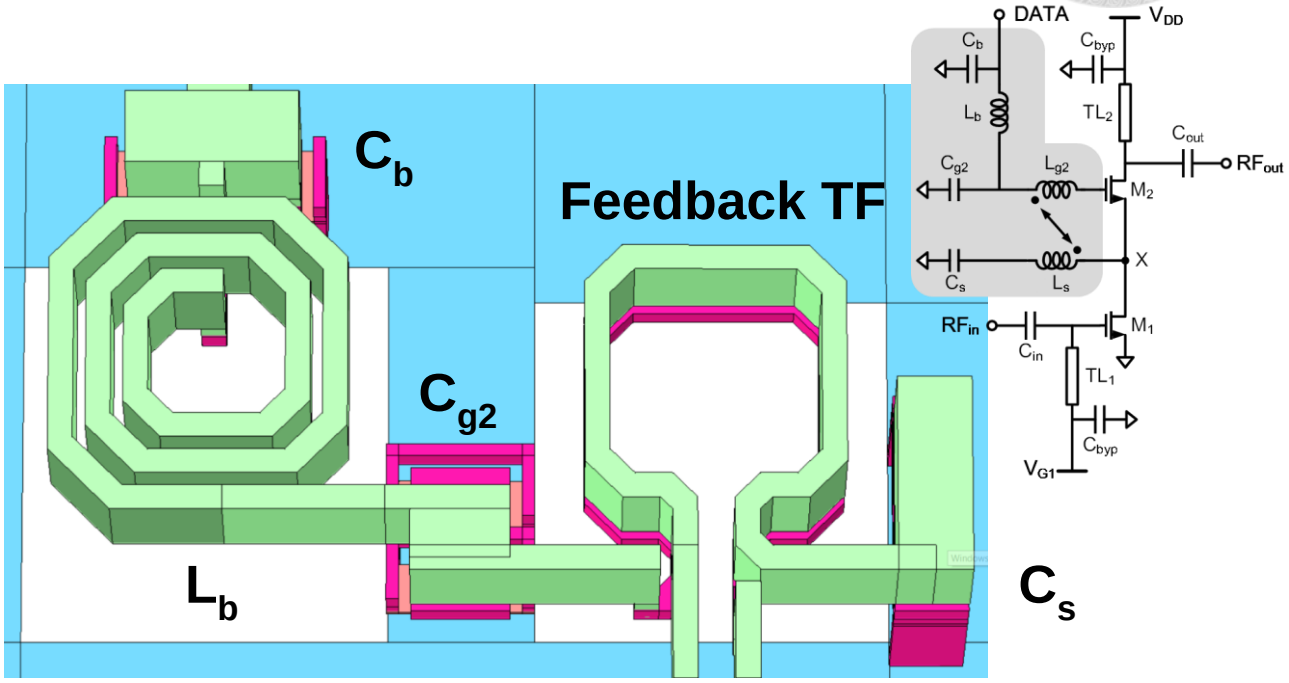

Fig. 3.23. 3-D rendering of the area around the devices used for EM simulation.

3.3.5 Simulation Results

Fig. 3.24 and Fig. 3.25 shows the post-EM simulated *S*-parameters of the proposed 60-GHz modulator at on- and off-states, respectively. At on-state, the modulator shows a 14 GHz 3-dB bandwidth from 52 to 66 GHz, and gain of 8.8 dB at 60 GHz. Both in- and output return losses are above 10dB from 57 to 63 GHz. Input return loss performance is slightly better than output, which is to be expected in PA designs. At off-state, the modulator shows isolation above 35 dB across 40 to 80 GHz, and isolation of 36 dB at 60 GHz. Both in- and output return losses are similar to that at on-state, with output return loss decreased slightly below 10 dB at 60 GHz. Similar behavior in in/output return loss between on- and off-states ensures the stability within the transmitter at either state of data transmission. From the on- and off-state performances, the modulator shows an on-off isolation of 44.8 dB at 60 GHz.

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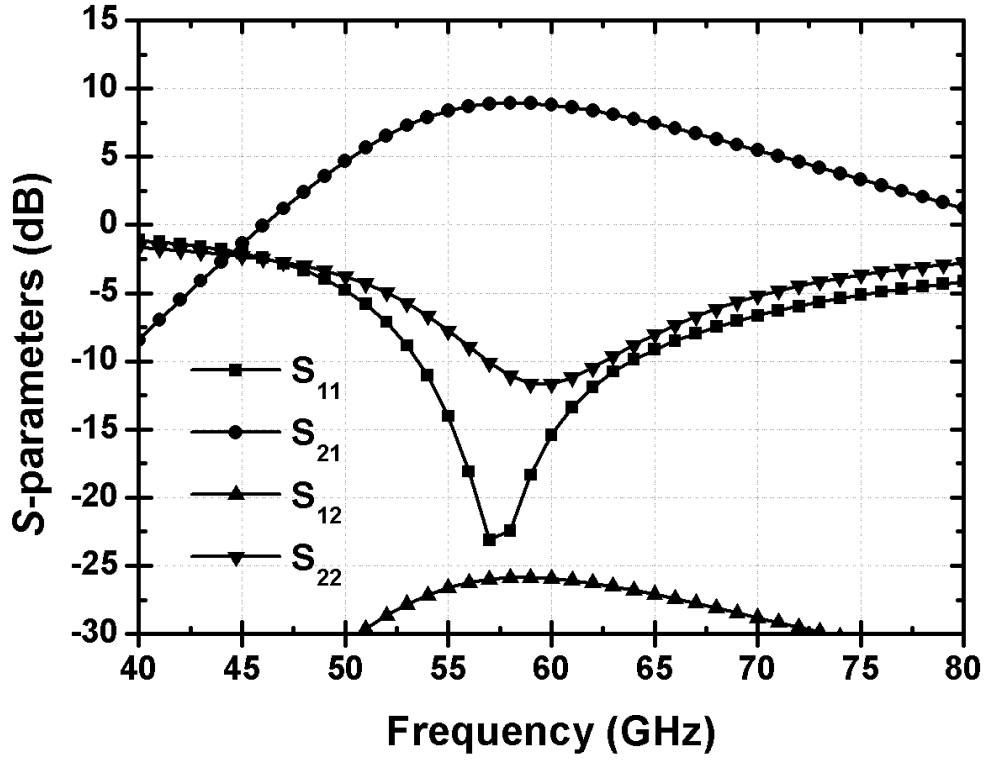

Fig. 3.24. Simulated *S*-parameters of the proposed modulator at on-state.

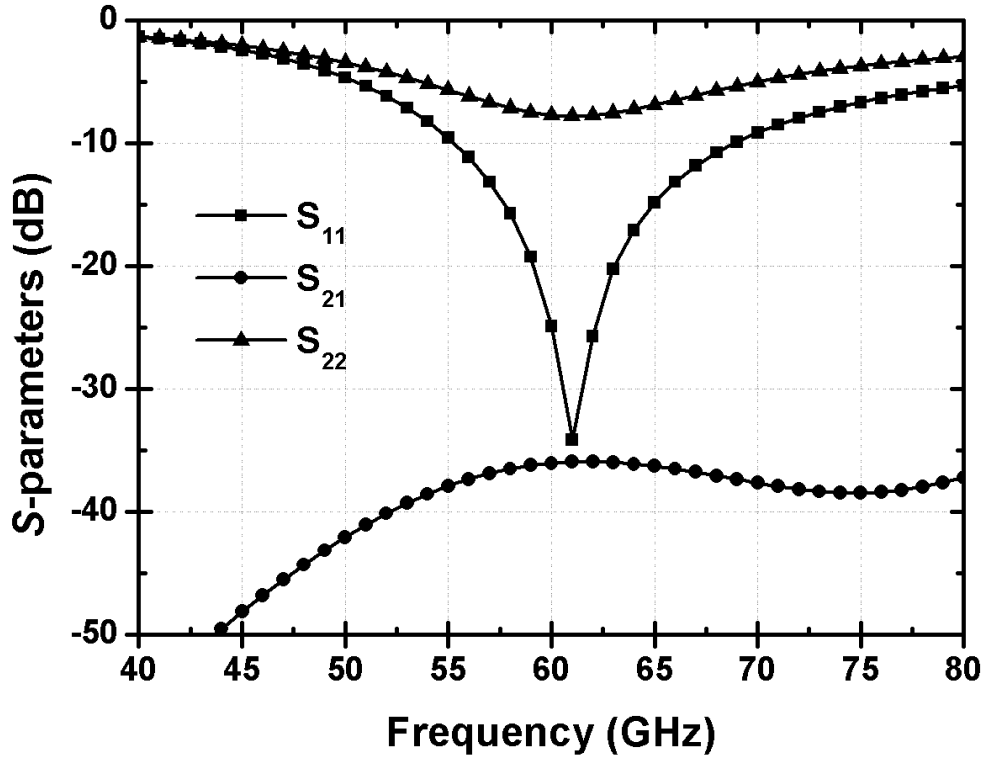

Fig. 3.25. Simulated *S*-parameters of the proposed modulator at off-state.

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Fig. 3.26 shows the post-EM simulated large-signal performances at on-state at 60 GHz. The modulator shows an OP_{1dB} of 6.2 dBm, P_{sat} of 8.4 dBm, and peak power-added-efficiency (PAE) of 14.2% at 60 GHz. Fig. 3.27 shows the post-EM simulated large-signal performances at on-state versus frequency. Across 56 to 64 GHz, the modulator shows OP_{1dB} above 5.8 dBm, P_{sat} above 7.8 dBm, and peak PAE above 12.2%. Furthermore, OP_{1dB} performance is above 5.5 dBm across 52 to 66 GHz.

Fig. 3.28 shows the post-EM simulated large-signal performances at off-state at 60 GHz. As can be seen, the isolation performance only degrades slightly at higher P_{in} levels. The modulator shows isolation > 35dB for P_{in} < 0 dBm, and isolation > 30 dB for P_{in} < 5 dBm. Compared with the on-state performances shown in Fig. 3.26, this means that the modulator can be driven at high P_{in} levels for output power performances at on-state, with little compromise in isolation performance at off-state.

Fig. 3.29 shows the post-EM simulated stability factor of the modulator. Stability factor above 1 across the frequencies indicates a stable design. Fig. 3.30 shows the post-EM simulated drain current (I_{DD}) and power consumption (P_{DC}) at on-state versus P_{in}, in which $P_{DC} = V_{DD}$ x I_{DD} = 2V x I_{DD}. The drain current and power consumption is around 17 mA and 34 mW across different P_{in} levels, respectively.

For modulation simulations, the P_{in} level at 60 GHz is set to -1 dBm, around the IP_{1dB} point at on-state. Fig. 3.31(a) to 3.34(a) shows the post-EM simulated output spectrum of the modulated signal. As mention in the introduction, the power spectral density of OOK modulation is a sinc function centered at the carrier frequency with main lobe width of $2T_b$, in which T_b denotes the bit period. As shown in the figures, the first nulls appear at [data rate]-GHz away from the 60 GHz carrier frequency at different data rates, indicating a successful modulation. Fig. 3.31(b) to 3.34(b) shows the post-EM simulated output waveform of the modulated signal. Data sequence of “1010” is used during simulation for demonstration purposes. We also include the output waveform of the

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modulator at on- and off-states in the figures. As can be seen, the modulated signal of a single bit, i.e., the shortest response time for data transition, can reach the output magnitude at on/off-state before falling/rising again at up to data rate of 10 Gb/s. This ensures that the modulator maintains the on/off-state performance of our design during modulation at the particular data rate. Fig. 3.35 to 3.38 show the simulated eye patterns of the OOK modulation. The baseband data input is of pseudo-random binary sequence (PRBS) data frame (2^{31} - 1) at data rates of 4.5 to 10 Gb/s. $V_{p\text{-}p}$ of the baseband data signal is set to 0 to $V_{G2,on}$, i.e., 0 to 1.8 V. For a better match of the conditions during measurement and future applications, the rise and fall times are set to 10% of T_b during simulation of the eye patterns. An ideal AM receiver is used for envelope detection at the output of the modulator. As can be seen, the rise and fall times of the eye patterns increase with higher data rates as expected. For the proposed modulator, , the simulated eye pattern up to the data rate of 10 Gb/s shows good opening, indicating a modulation index close to 1.

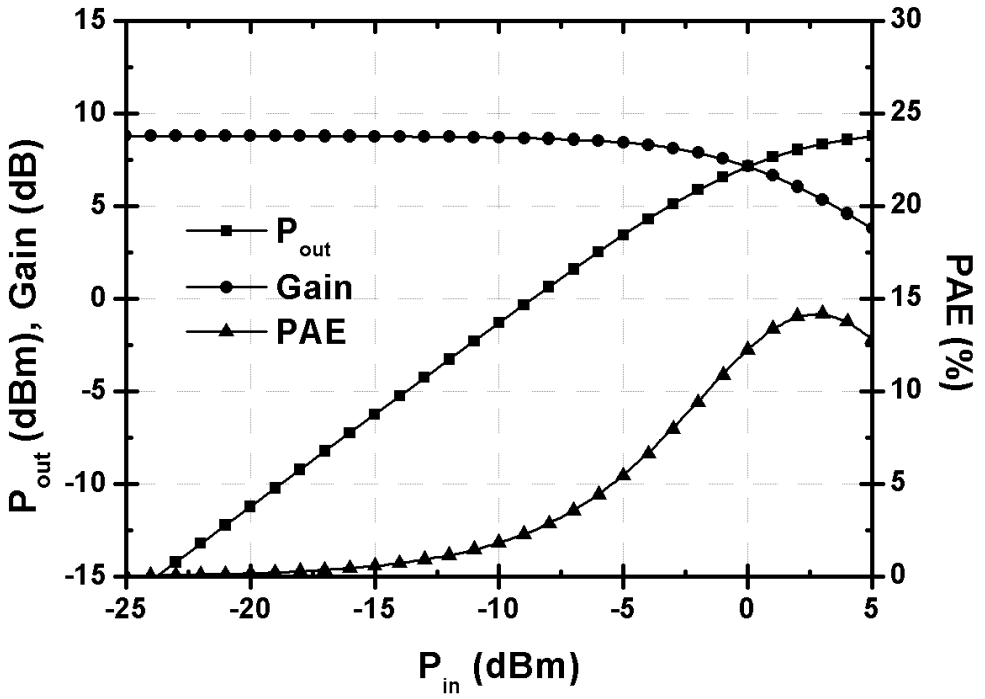

Fig. 3.26. Simulated large-signal performances of the proposed modulator at 60 GHz at on-state.

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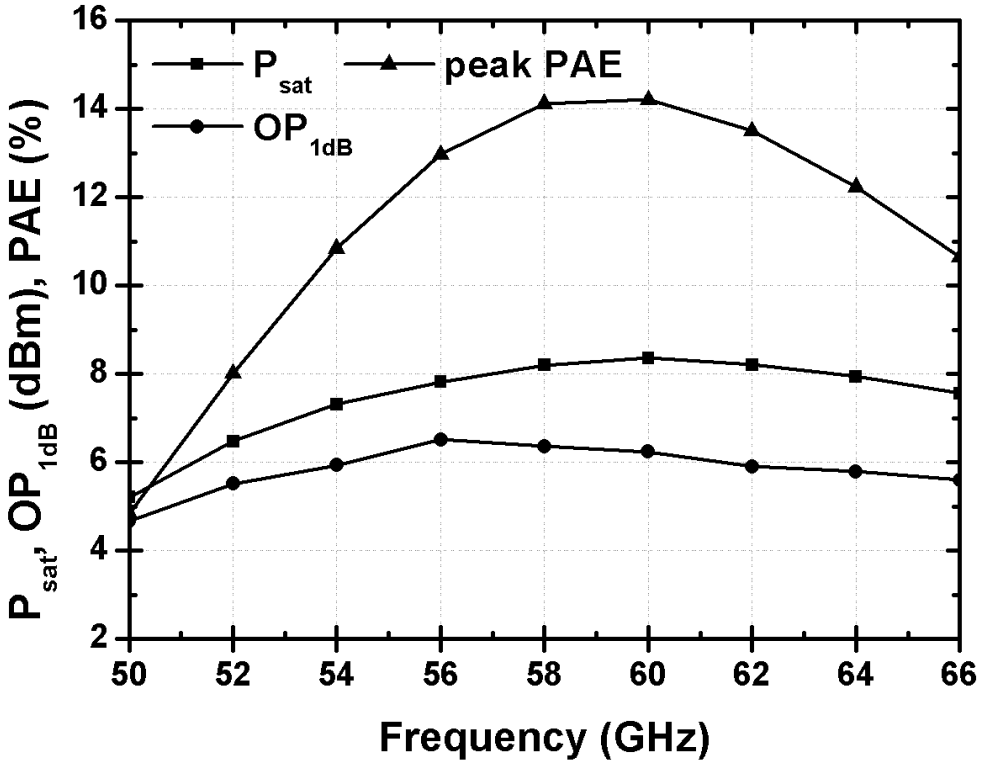

Fig. 3.27. Simulated large-signal performances of the proposed modulator at on-state versus frequency.

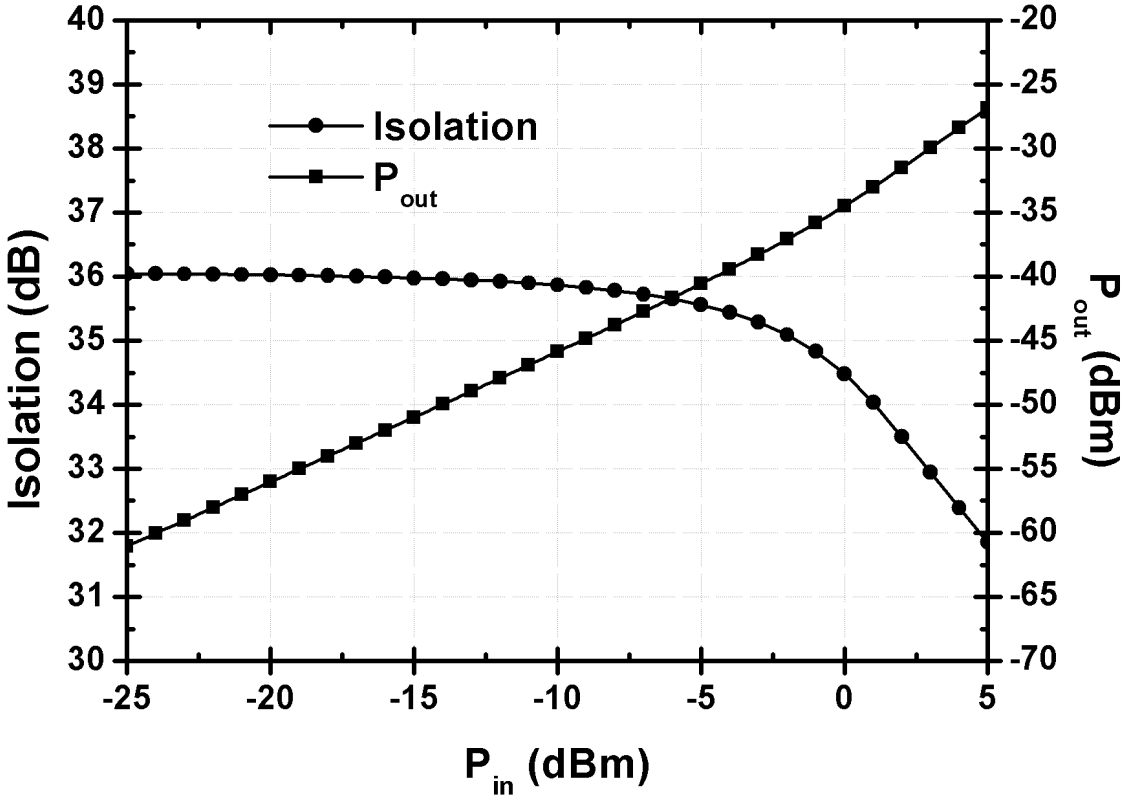

Fig. 3.28. Simulated large-signal performances of the proposed modulator at 60 GHz at off-state.

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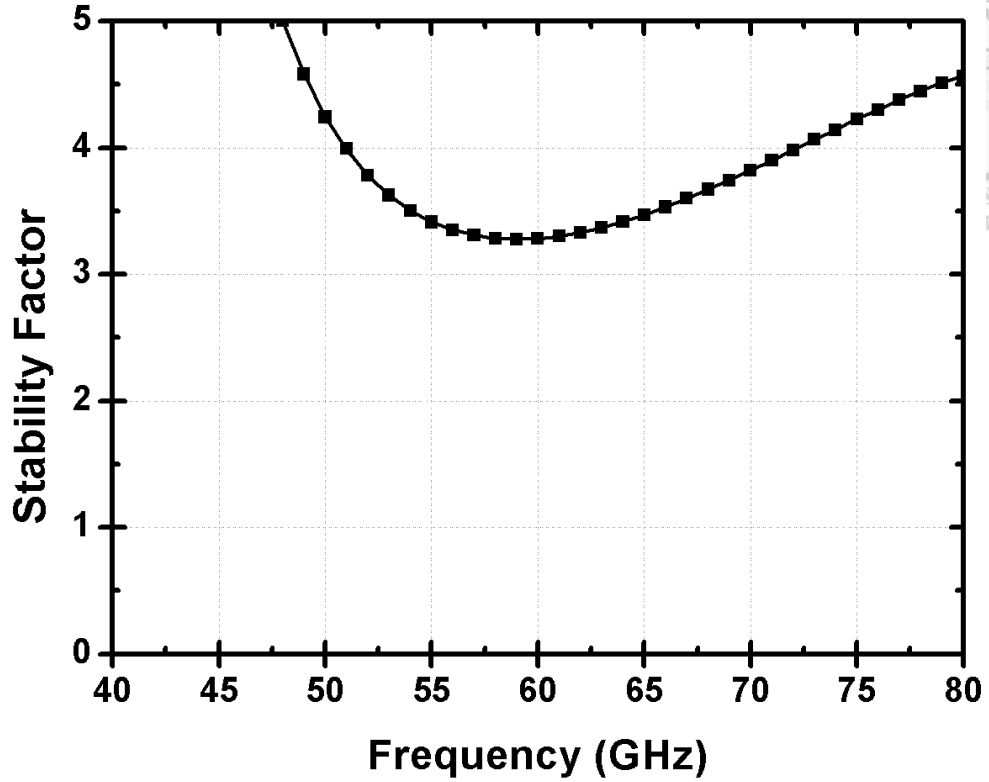

Fig. 3.29. Simulated stability factor of the proposed modulator at on-state.

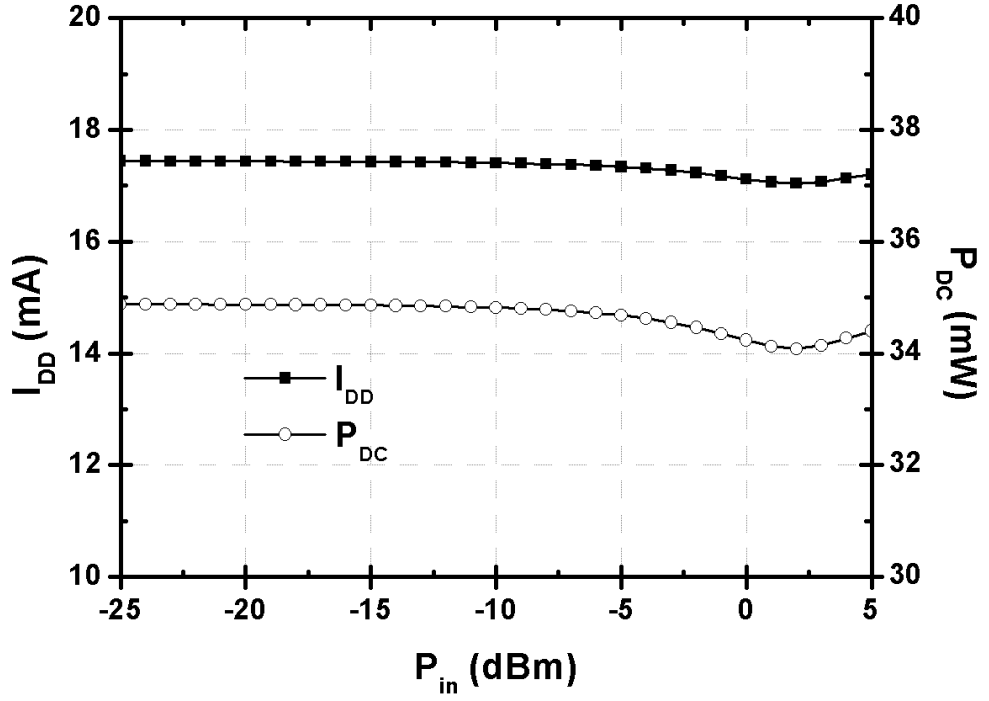

Fig. 3.30. Simulated drain current (I_{DD}) and power consumption (P_{DC}) at on-state versus P_{in}.

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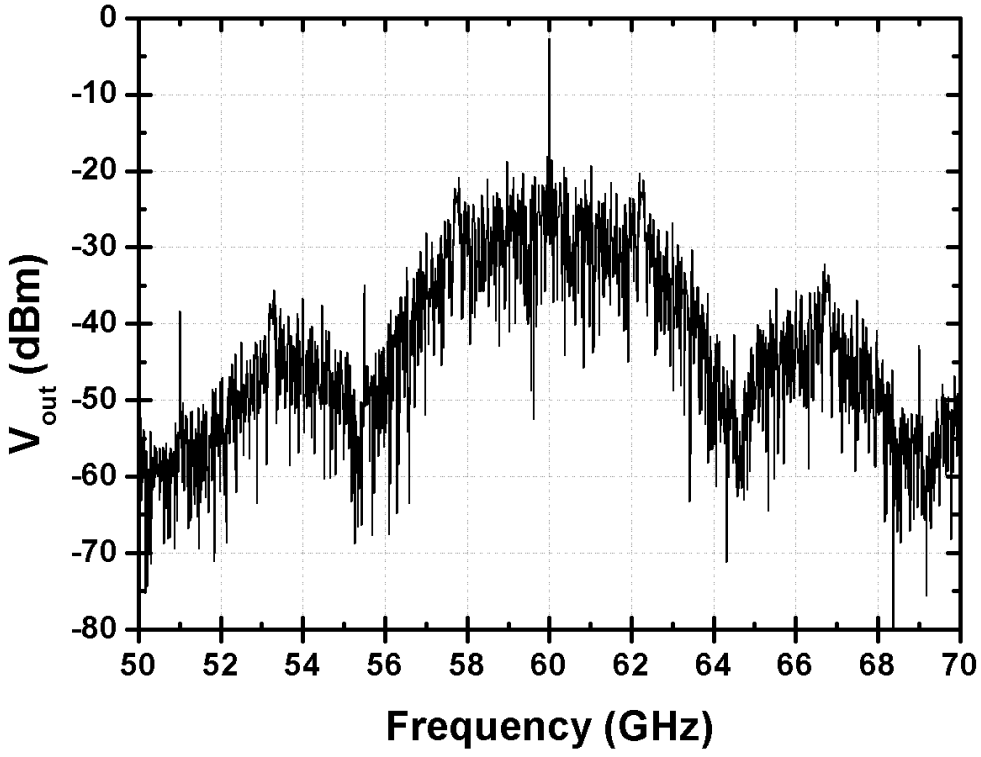
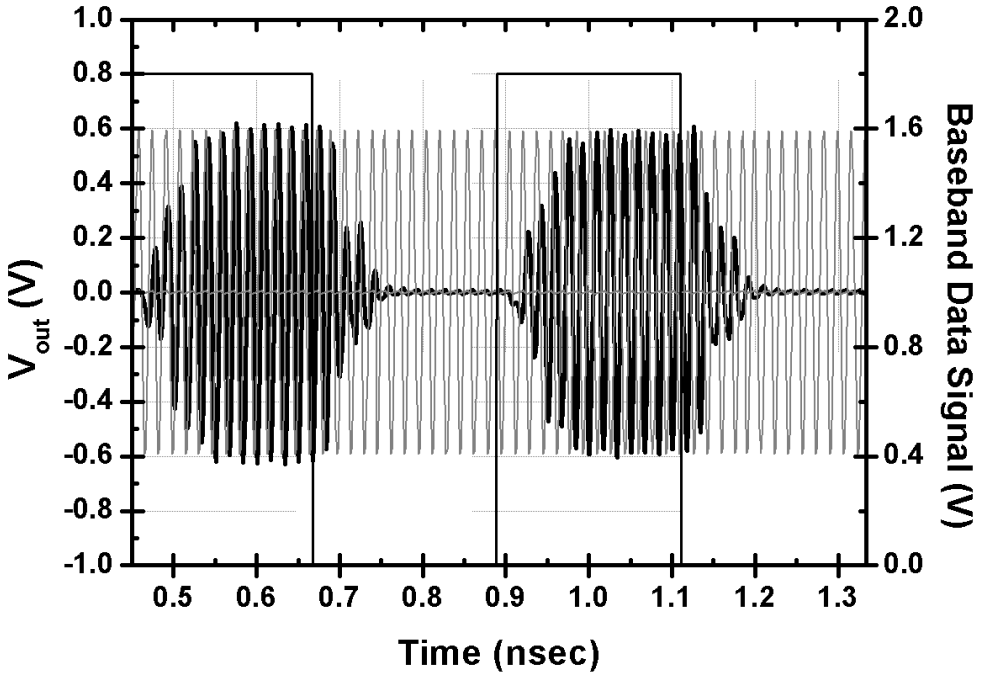


(a)



(b)

Fig. 3.31. Simulated output (a) spectrum and (b) waveform of the modulated signal at data rate of 4.5 Gb/s.

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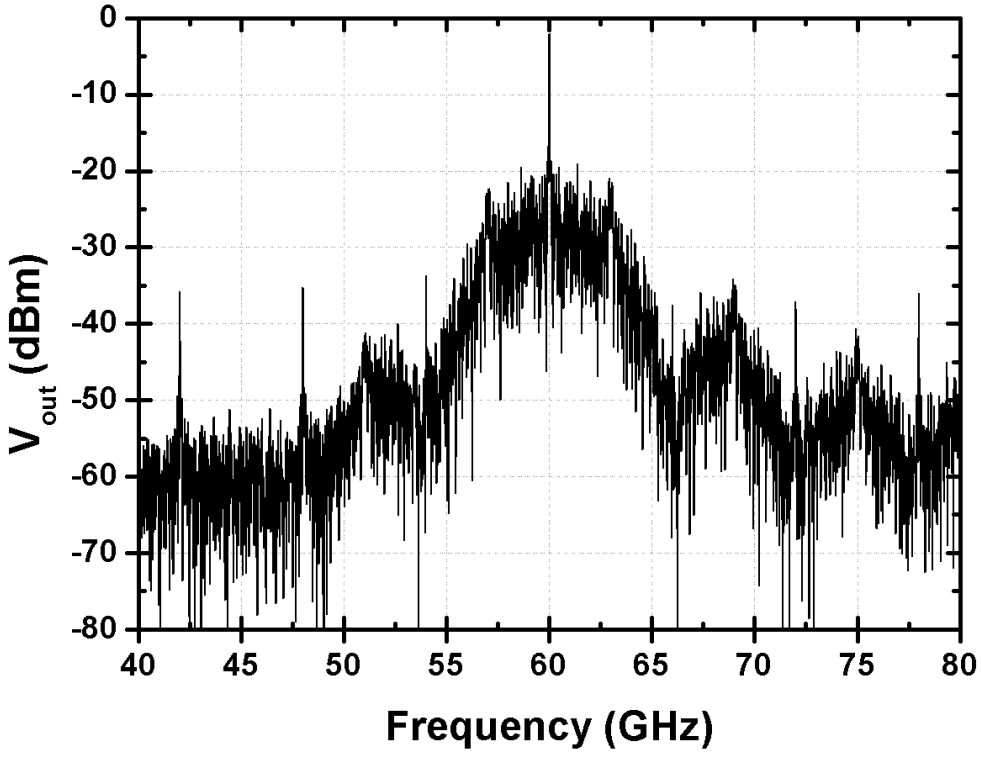
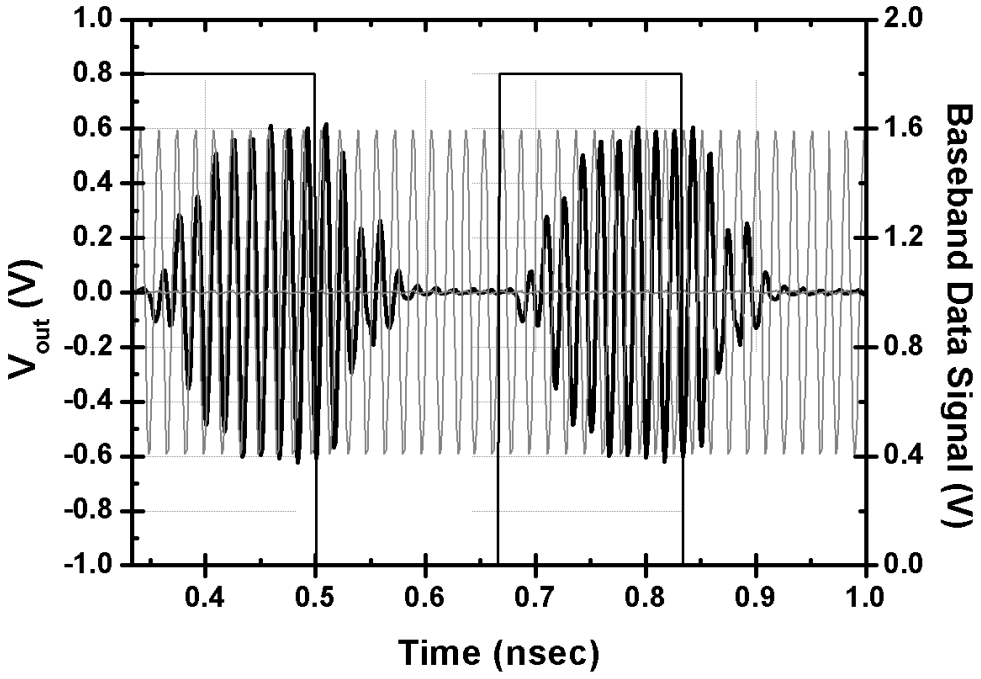


(a)



(b)

Fig. 3.32. Simulated output (a) spectrum and (b) waveform of the modulated signal at data rate of 6 Gb/s.

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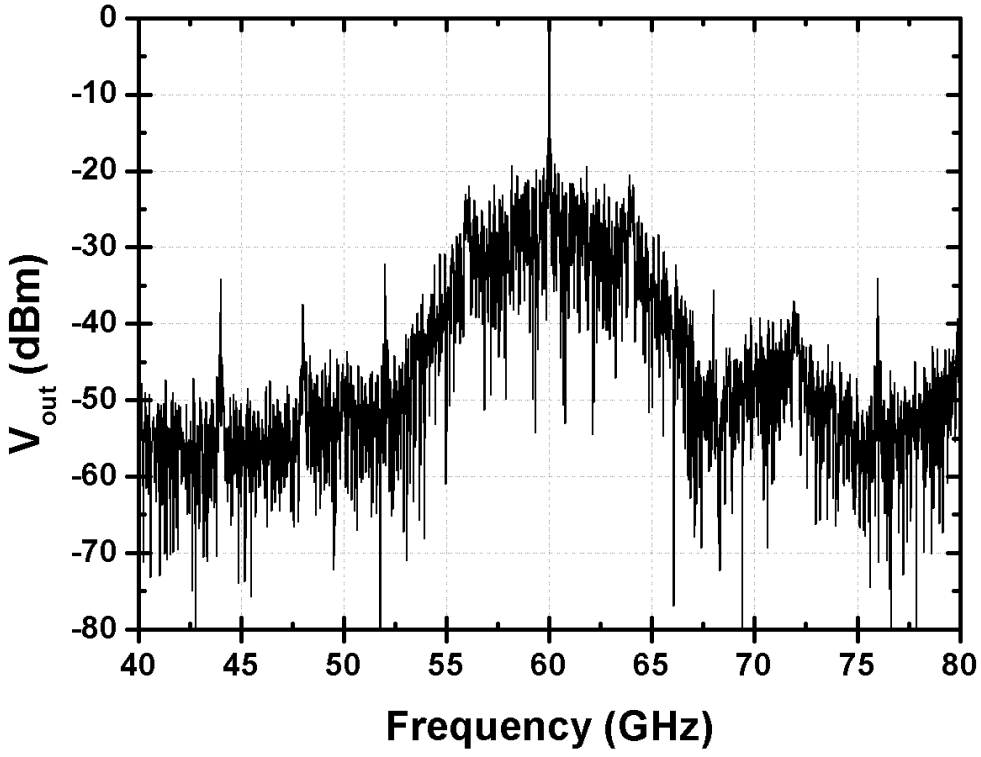
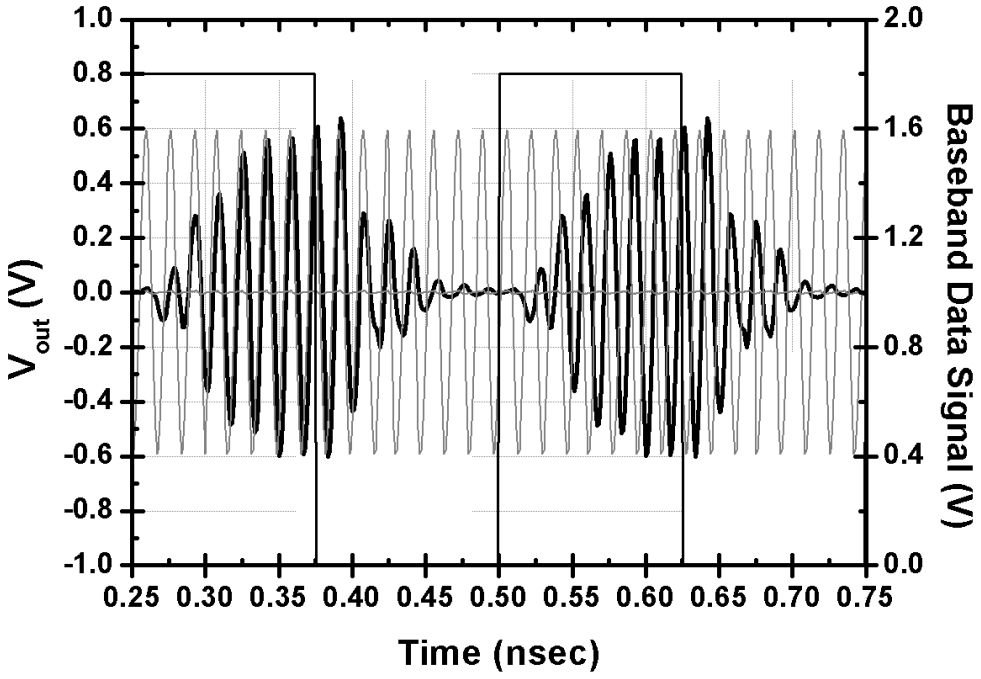


(a)



(b)

Fig. 3.33. Simulated output (a) spectrum and (b) waveform of the modulated signal at data rate of 8 Gb/s.

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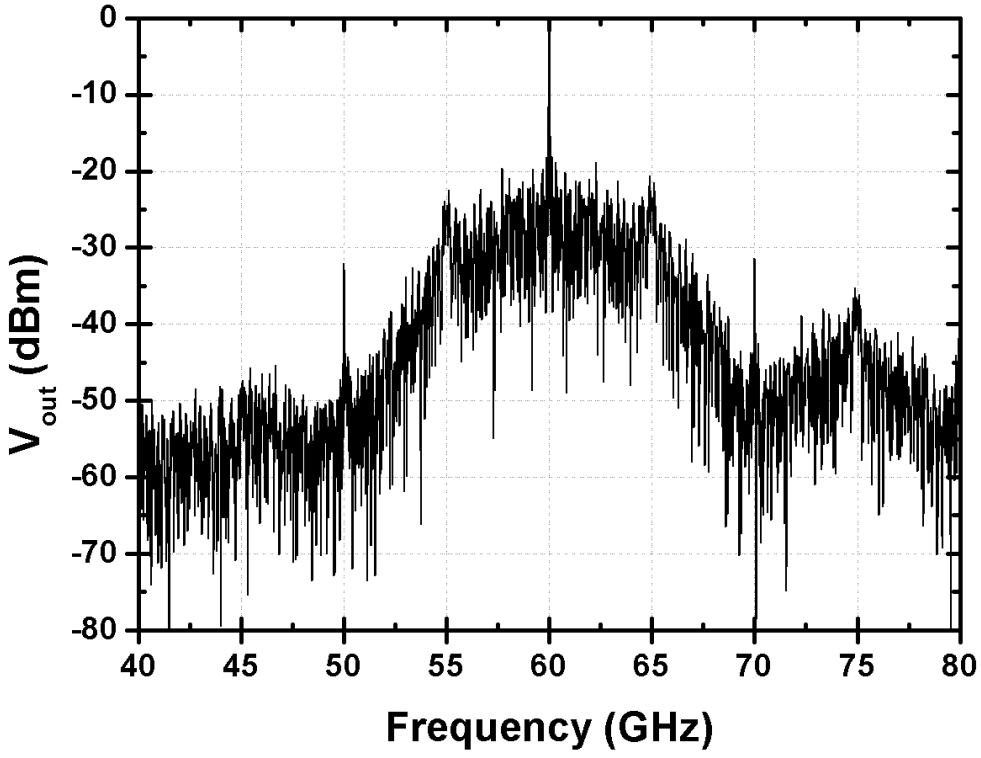
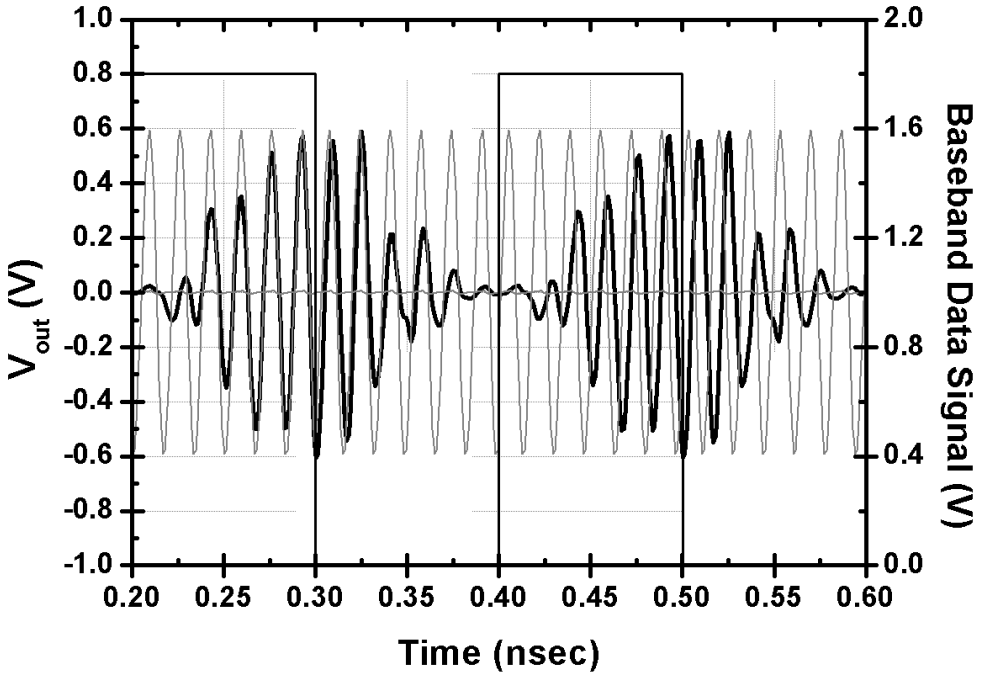


(a)



(b)

Fig. 3.34. Simulated output (a) spectrum and (b) waveform of the modulated signal at data rate of 10 Gb/s.

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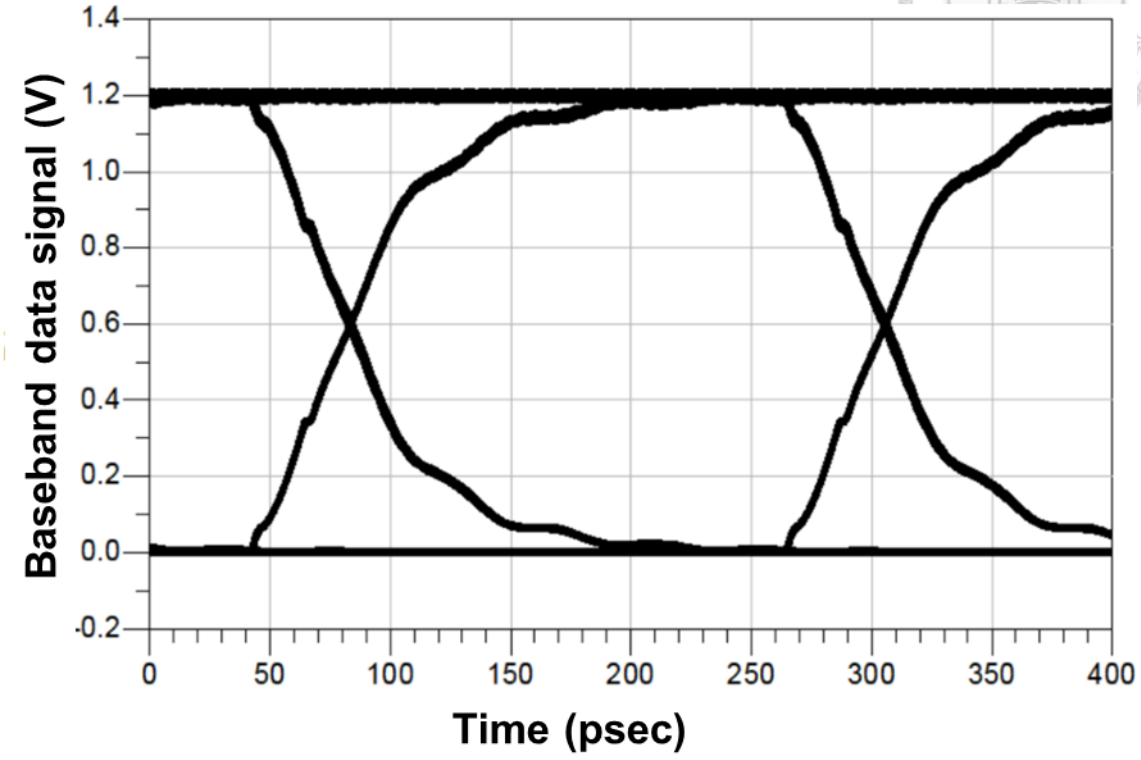

Fig. 3.35. Simulated eye pattern of the OOK modulation at data rate of 4.5 Gb/s.

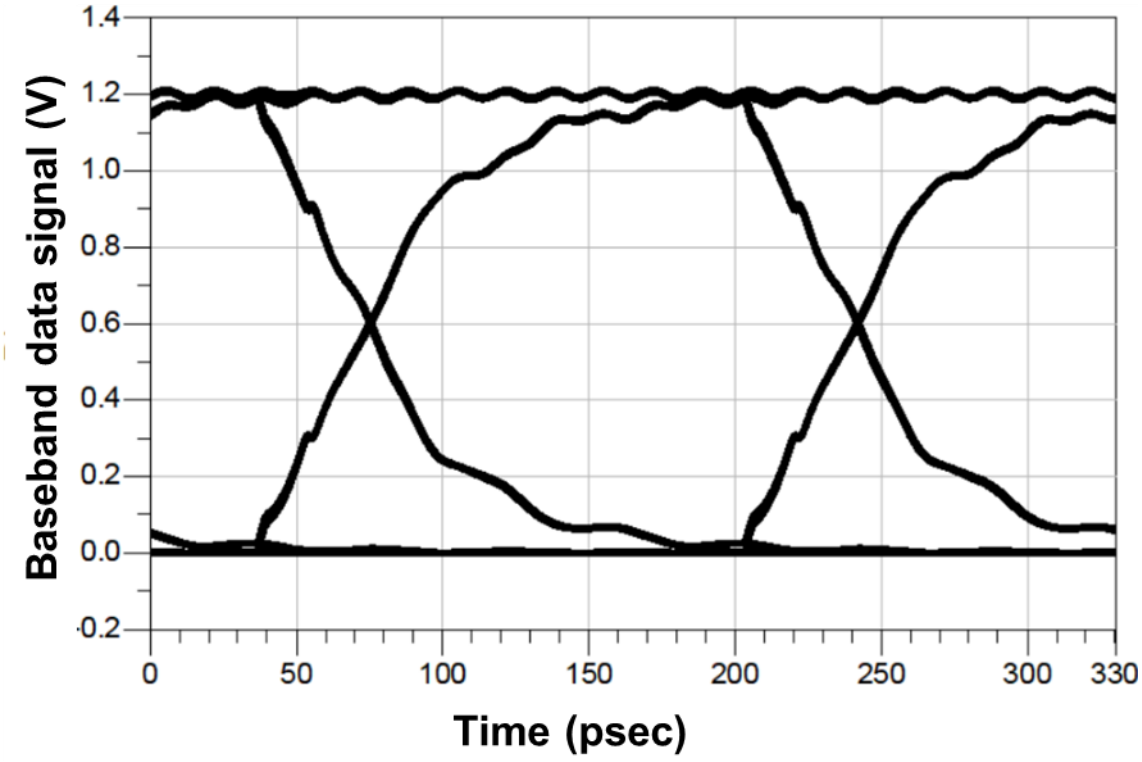

Fig. 3.36. Simulated eye pattern of the OOK modulation at data rate of 6 Gb/s.

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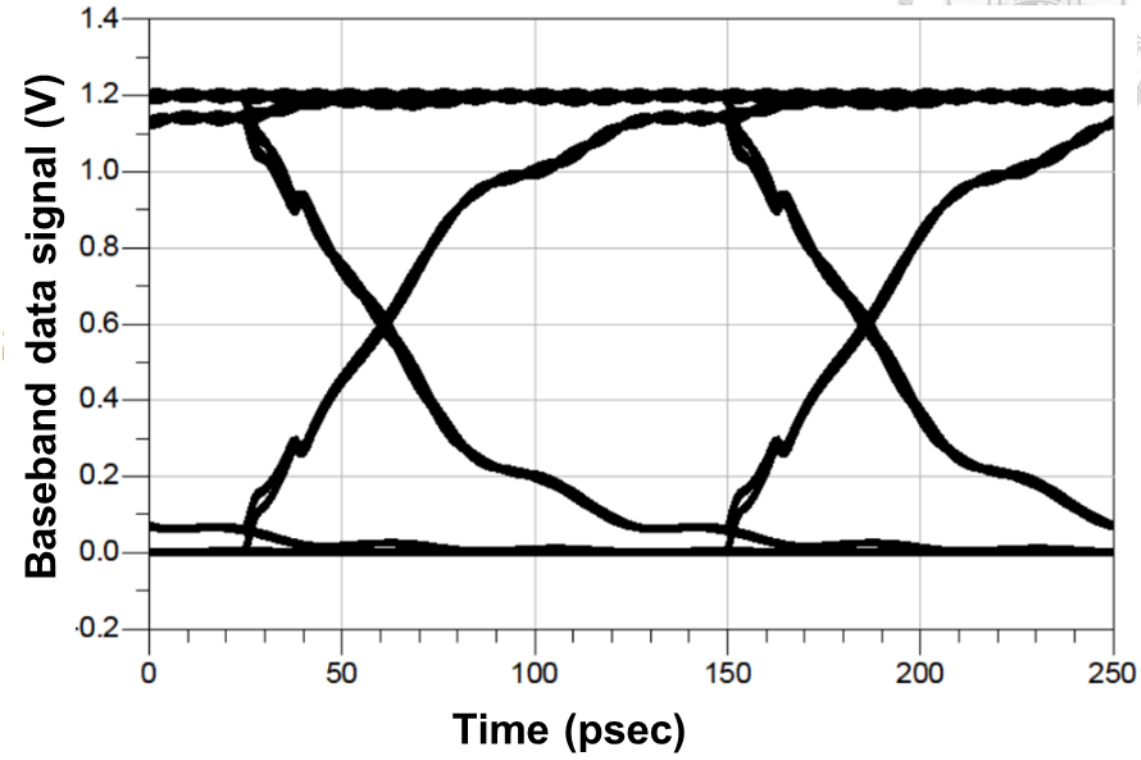

Fig. 3.37. Simulated eye pattern of the OOK modulation at data rate of 8 Gb/s.

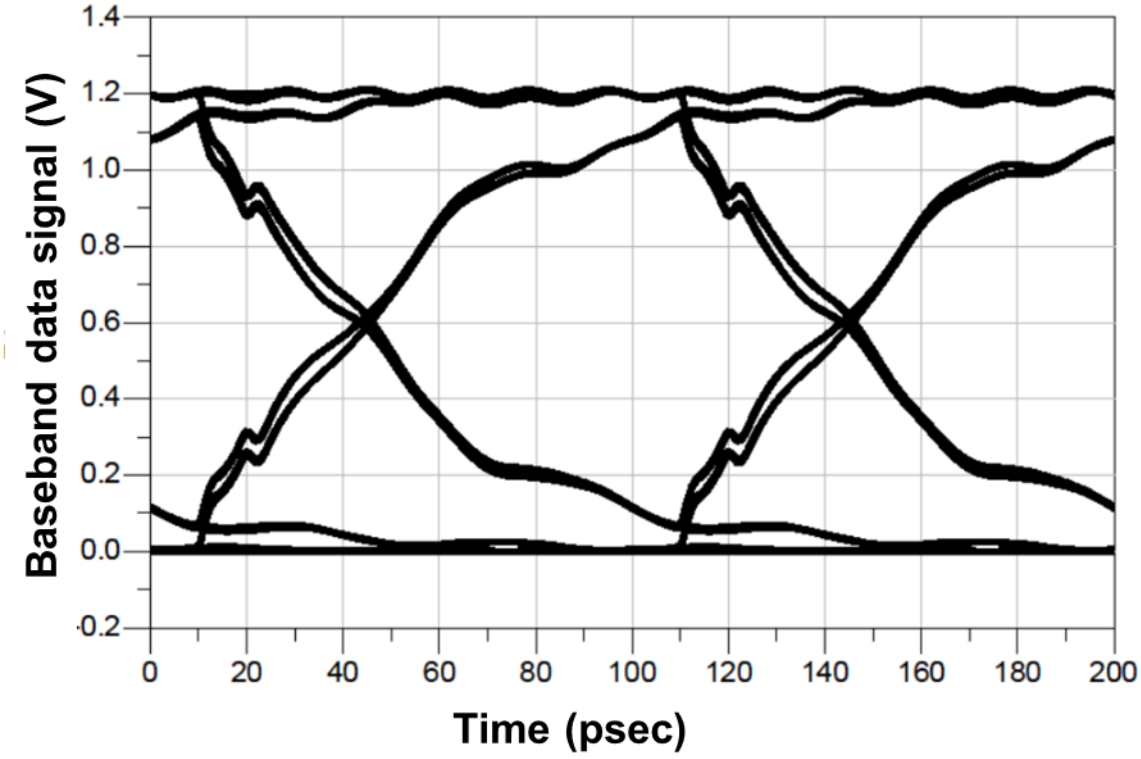

Fig. 3.38. Simulated eye pattern of the OOK modulation at data rate of 10 Gb/s.

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3.4 Experimental Results

The proposed design was fabricated in 90-nm CMOS process by TSMC. As shown in Fig. 3.39, the die size measures at 471 x 519 μm^2 with RF and DC pads included. Three GSG-configuration RF pads are used. Two on the left and right are used for RF (carrier) in and output, respectively. One on the top is used for baseband data input. Note that due to physical limitations of on-wafer probing, the chip size has to be increased with elongated 50-Ω transmission lines on both horizontal and vertical directions. An even smaller footprint of 261 x 469 μm^2 without RF and DC pads is possible for future applications in OOK transmitter designs. All measurements were performed via on-wafer probing.

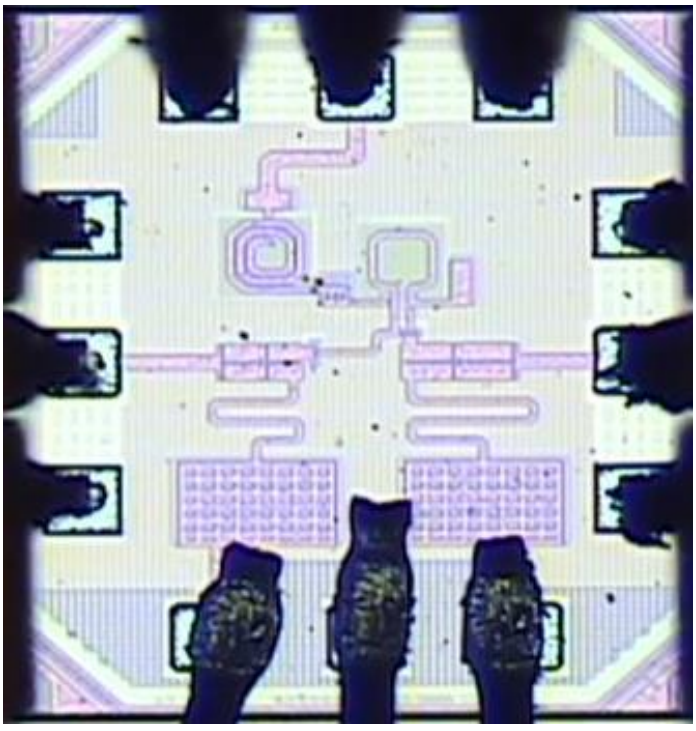

Fig. 3.39. Die photograph of the proposed OOK modulator.

3.4.1 On/Off-state Measurements

For on/off-state measurement, the GSG-configuration RF pad for baseband data input was used as DC pads instead. The chip was mounted on PCB board with bond-wiring for DC applications (V_{G1}, V_{G2} and V_{DD}). Off-chip bypass networks were designed and implemented on the PCB board.

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Table 3.2. Bias conditions during on/off-state small-signal measurements.

V_{G1}	V_{G2}	V_{DD}	I_{DS}	
			Simulation	**Measurement**
0.8 V	1.8 V	2.0 V	17 mA	17 mA
0.8 V	0 V	2.0 V	0 mA	0 mA

An Agilent E8361C network analyzer was used for small-signal measurements up to 67-GHz. Table 3.2 shows the bias conditions during small-signal measurements. Fig. 3.40 shows the measured and post-EM simulated *S*-parameters at on-state. The measurement result shows higher gain above 52 GHz but narrower bandwidth than the post-EM simulation. The measured gain at 60 GHz is 10.2 dB. Fig. 3.41 shows the measured and post-EM simulated *S*-parameters at off-state. The measured isolation ($-S_{21}$ in dB) agrees well with the post-EM simulation. The measured isolation at 60 GHz is 35.2dB. This results in a measured on-off isolation of 45.2 dB at 60 GHz. Both the measured S_{11} at on- and off-states does not agrees well with the post-EM simulation. This narrows the issue down to the input matching network. Since the input matching network consists of a series capacitor and a short stub, undesired variation of the capacitance is most likely the cause of issue.

For large-signal measurements, an Agilent E8257D signal generator and an Agilent 4419B power meter were used. Fig. 3.42 to 3.50 show the measured and post-EM simulated large-signal performances at on-state from 50 to 66 GHz. Fig. 3.51 shows the measured and post-EM simulated large-signal performances versus frequency. The measurement results show an OP_{1dB} of 7.0 dBm, P_{sat} of 8.9 dBm, and peak PAE of 18.4% at 60-GHz. As with the small-signal gain, the measurement results show slightly better large-signal performances than simulation above 52 GHz, but the difference is much smaller. Across 56 to 64 GHz, the measurement results show OP_{1dB} above 6dBm, P_{sat} above 7.8 dBm, and PAE_{peak} above 13.7%.

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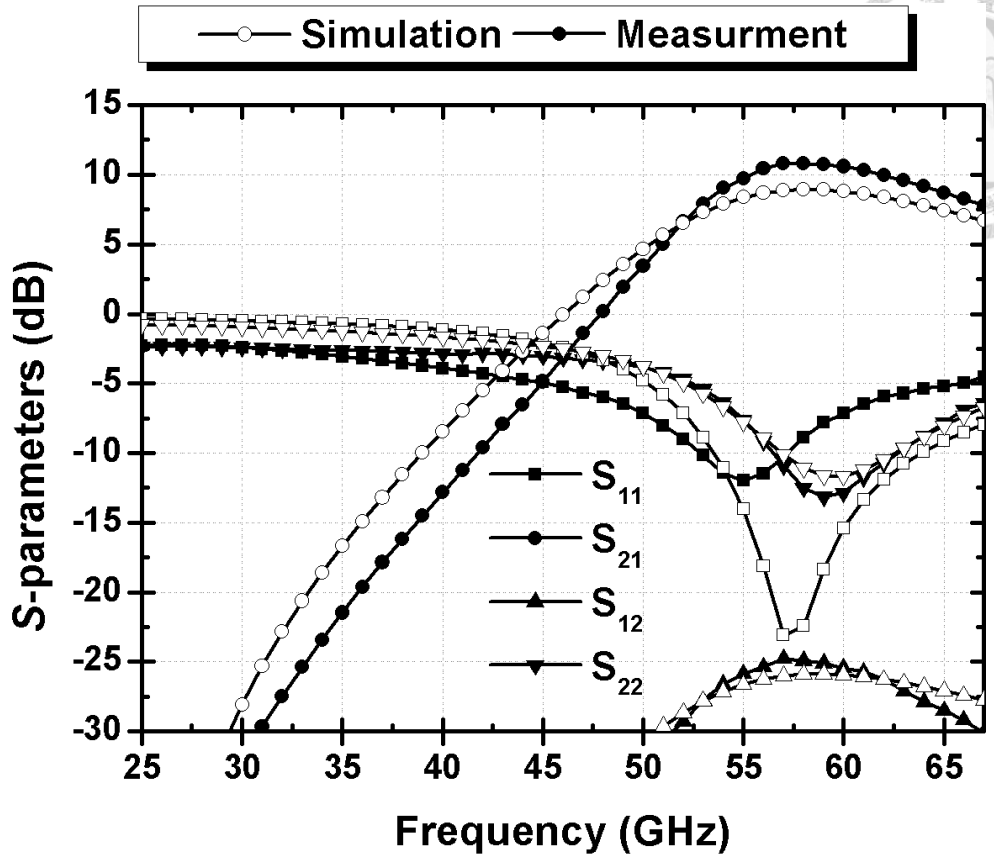

Fig. 3.40. Measured and simulated *S*-parameters of the proposed modulator at on-state.

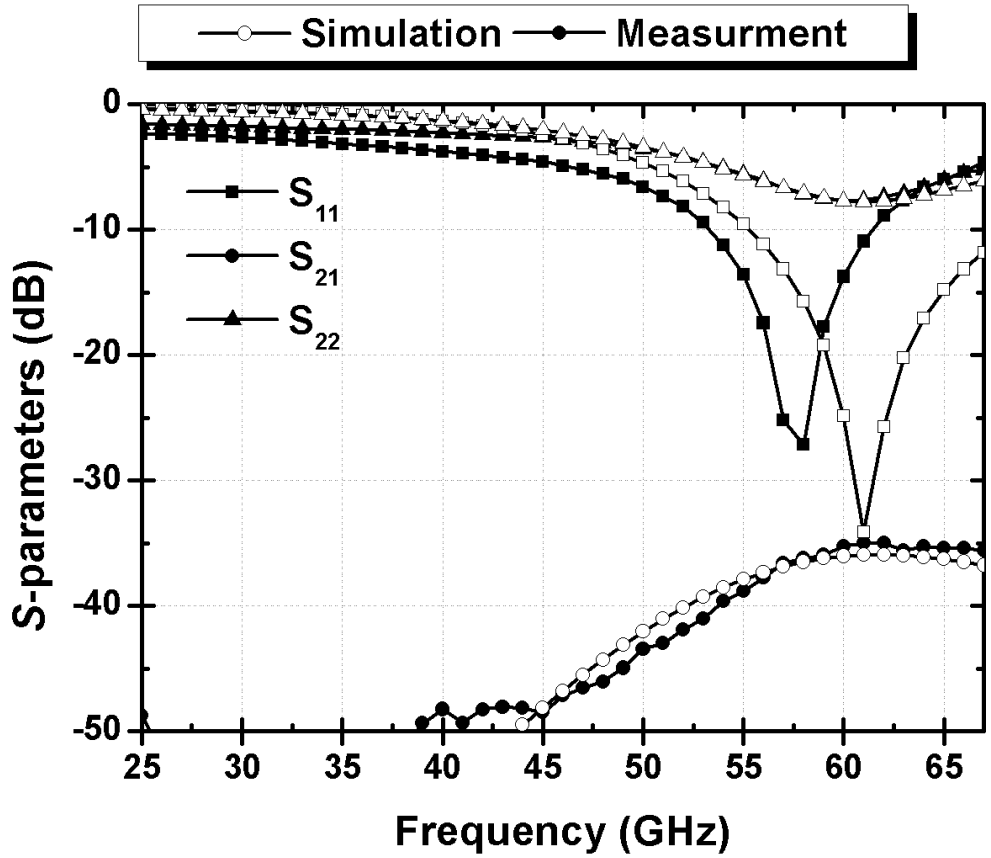

Fig. 3.41. Measured and simulated *S*-parameters of the proposed modulator at off-state.

doi:10.6342/NTU201900470

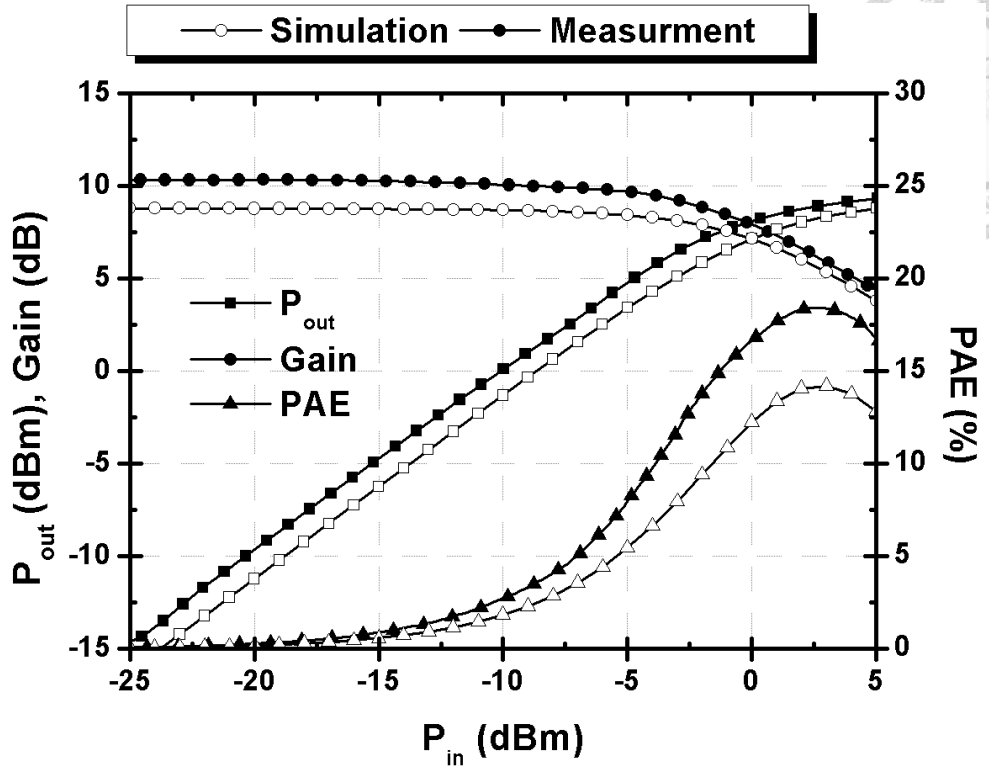

Fig. 3.42. Measured and simulated large-signal performances of the proposed modulator at on-state at 60 GHz.

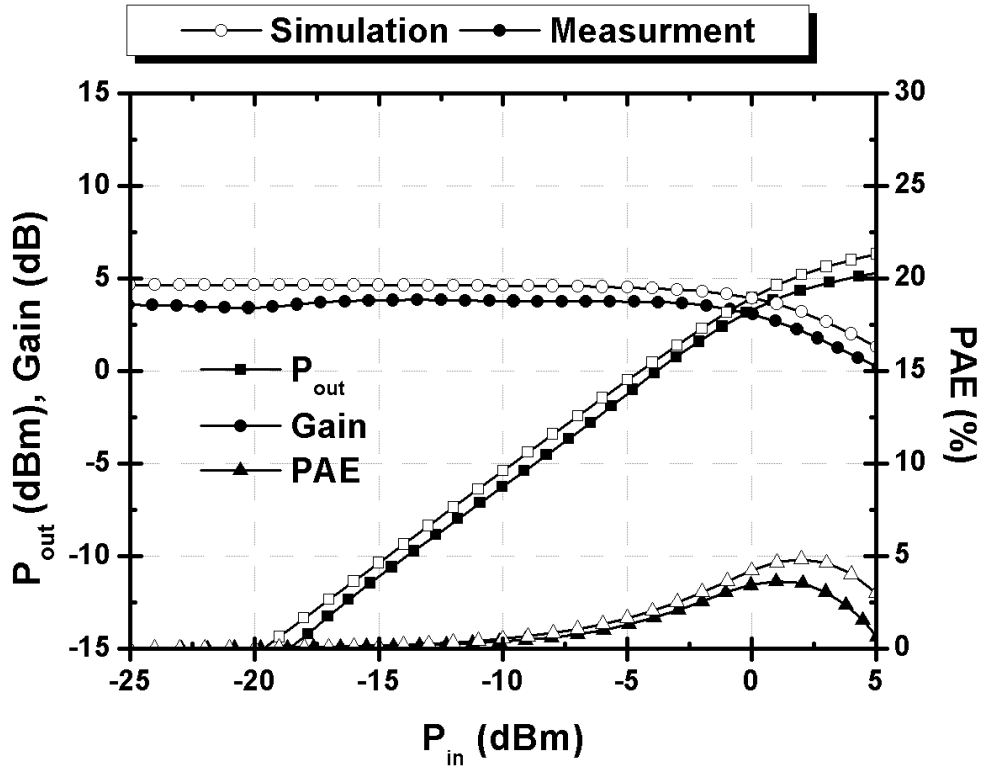

Fig. 3.43. Measured and simulated large-signal performances of the proposed modulator at on-state at 50 GHz.

doi:10.6342/NTU201900470

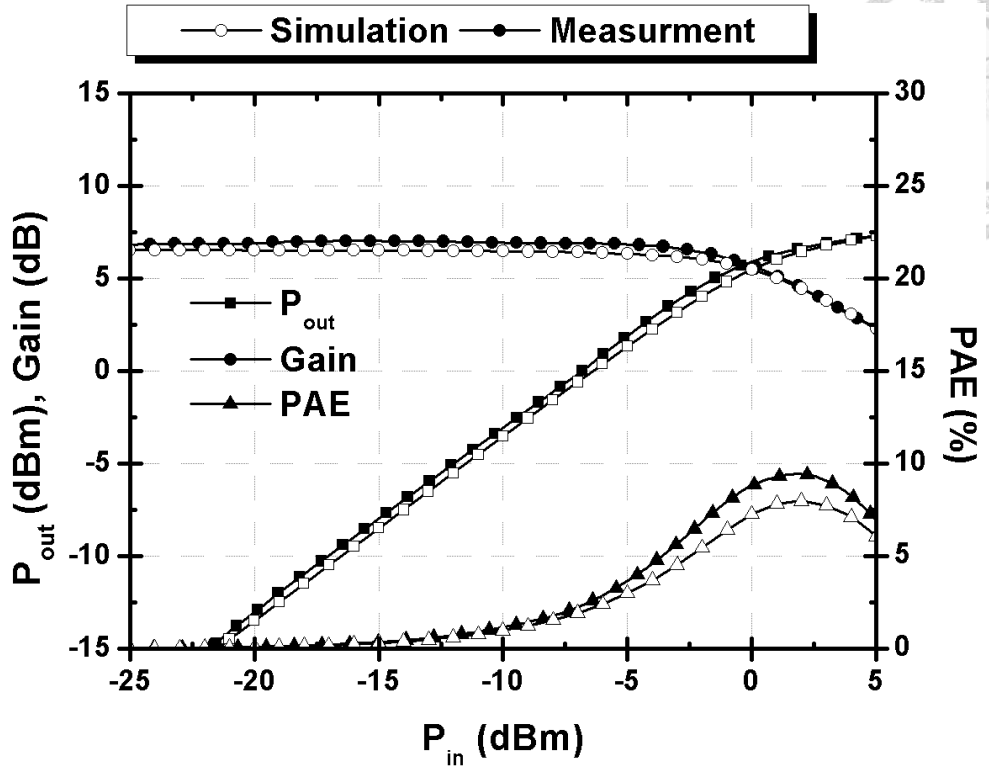

Fig. 3.44. Measured and simulated large-signal performances of the proposed modulator at on-state at 52 GHz.

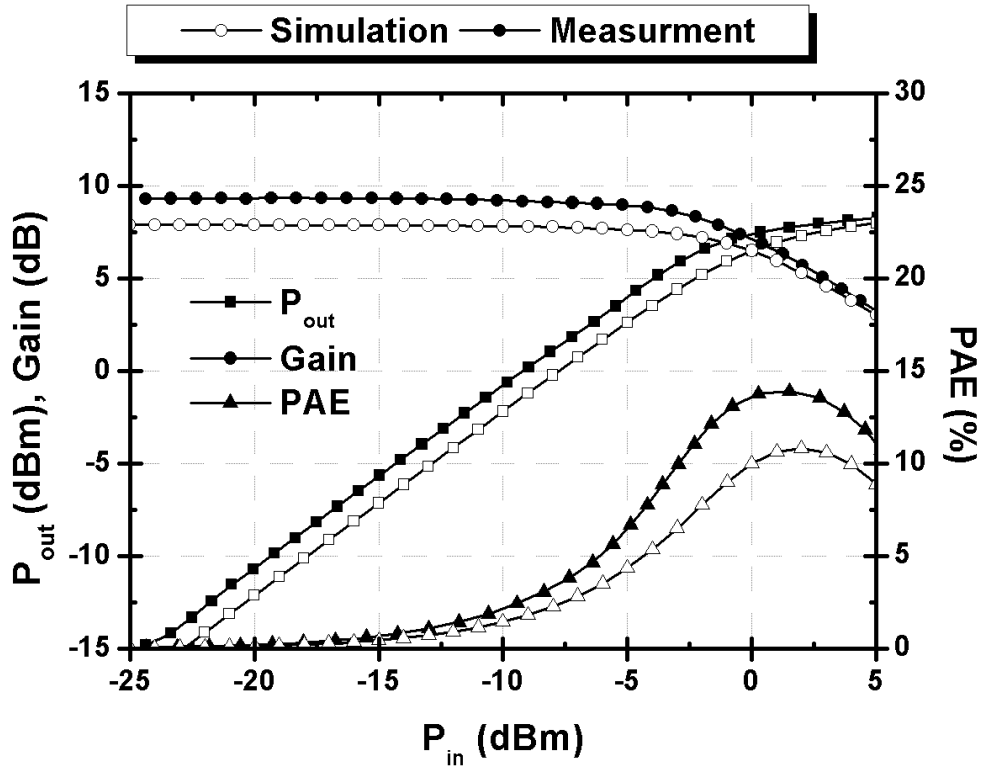

Fig. 3.45. Measured and simulated large-signal performances of the proposed modulator at on-state at 54 GHz.

doi:10.6342/NTU201900470

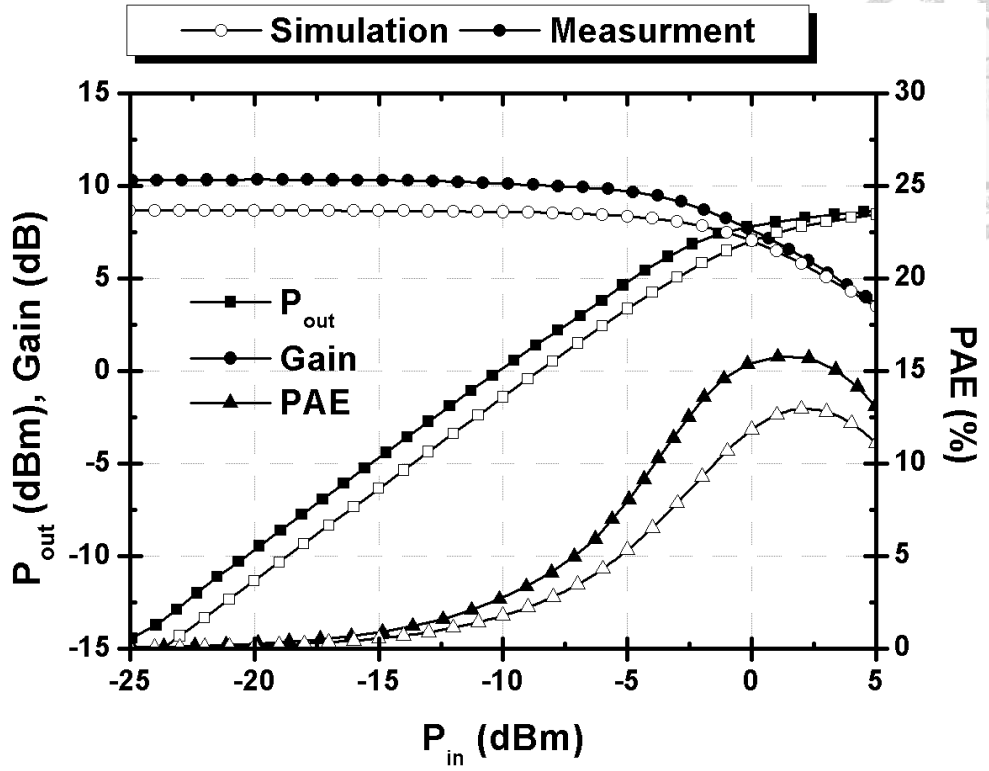

Fig. 3.46. Measured and simulated large-signal performances of the proposed modulator at on-state at 56 GHz.

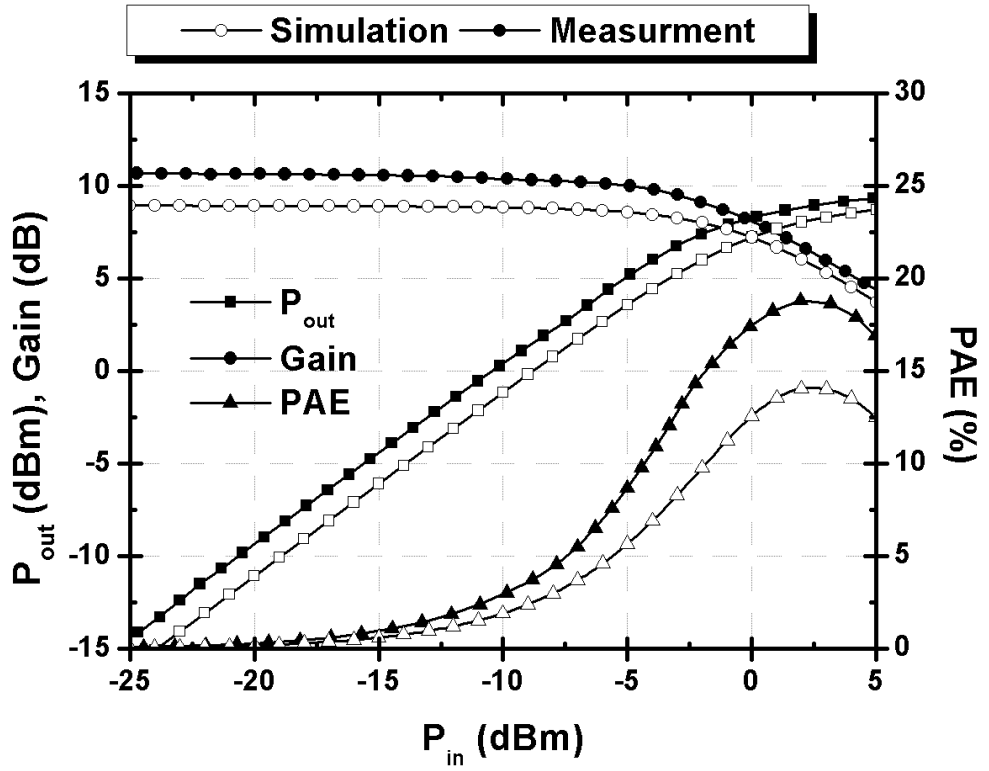

Fig. 3.47. Measured and simulated large-signal performances of the proposed modulator at on-state at 58 GHz.

doi:10.6342/NTU201900470

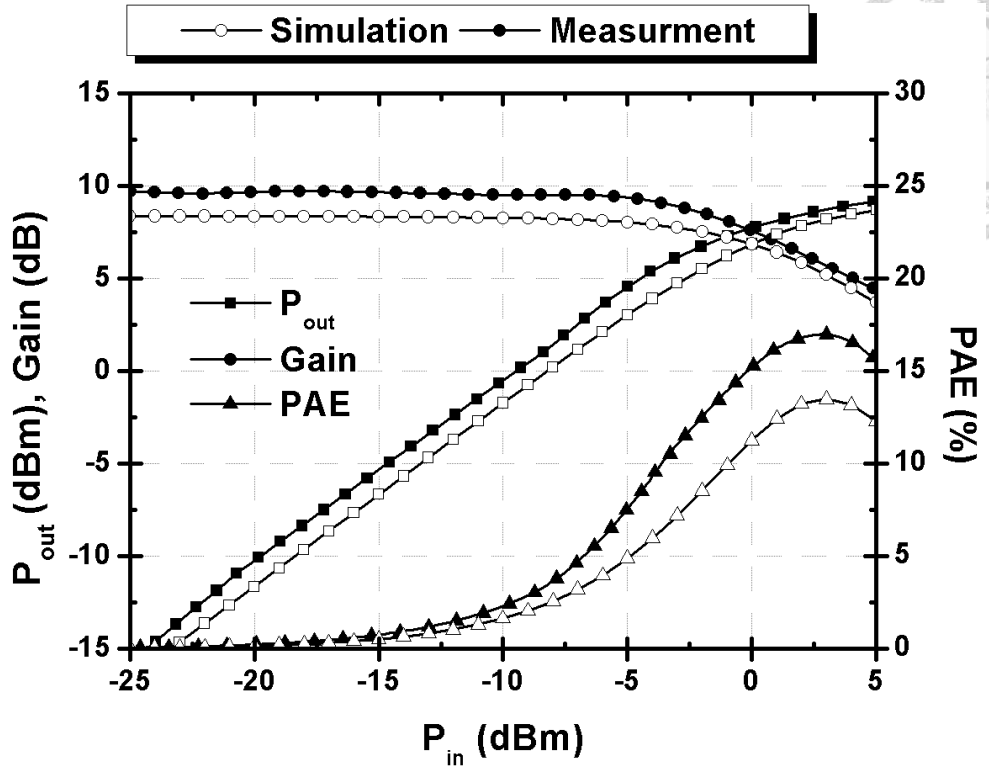

Fig. 3.48. Measured and simulated large-signal performances of the proposed modulator at on-state at 62 GHz.

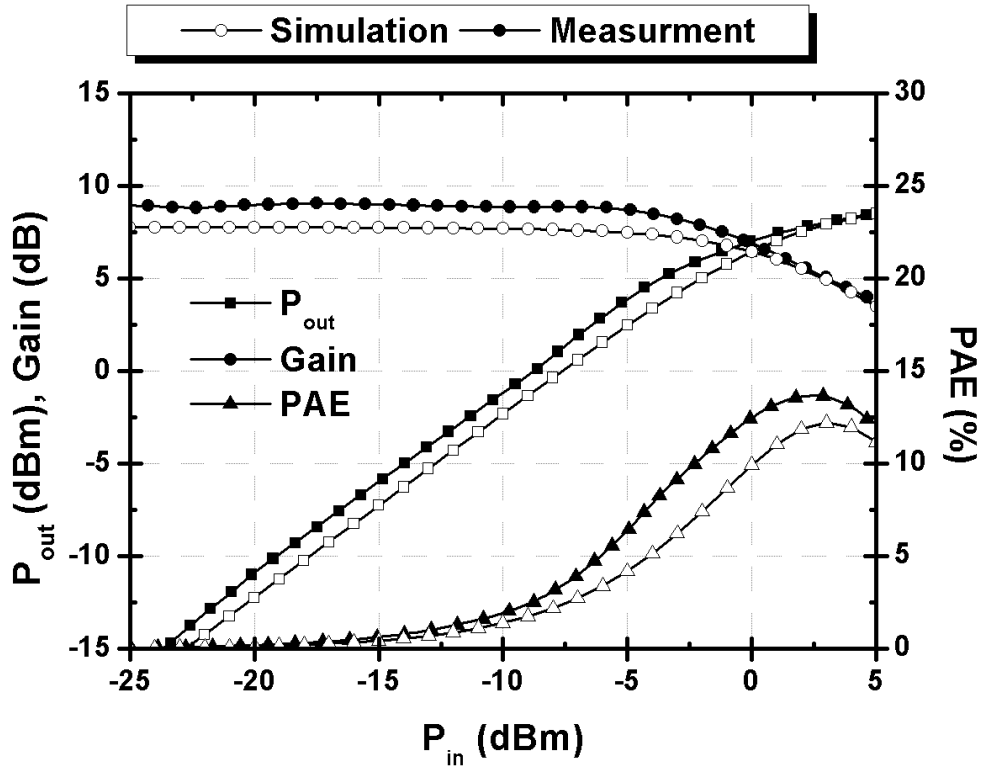

Fig. 3.49. Measured and simulated large-signal performances of the proposed modulator at on-state at 64 GHz.

doi:10.6342/NTU201900470

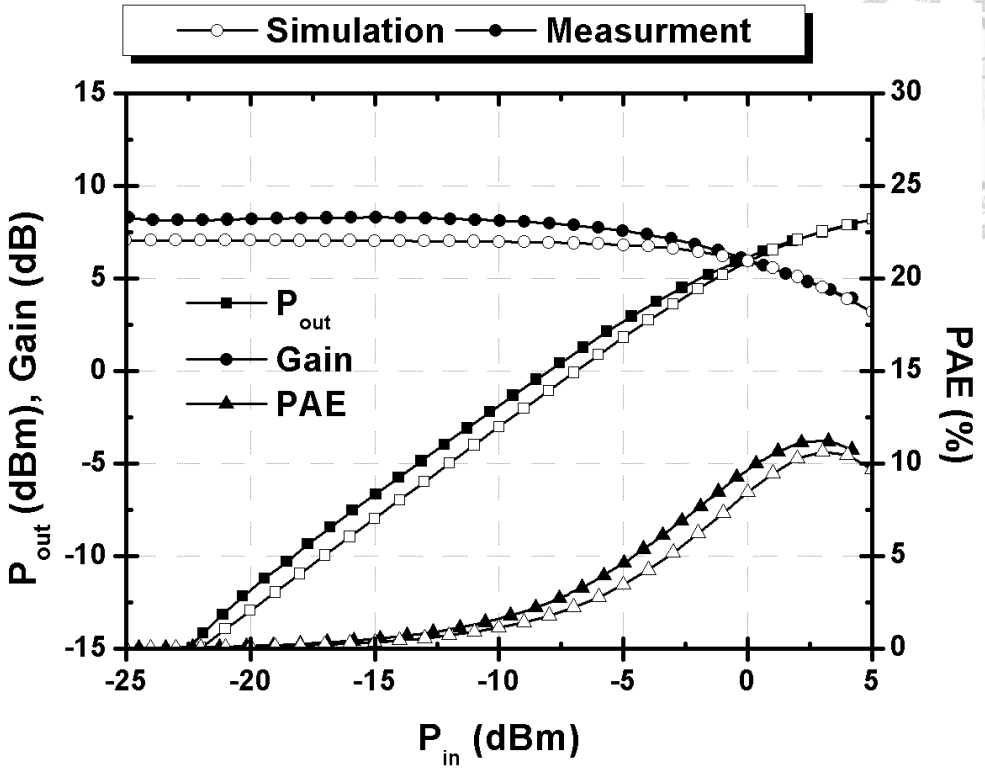

Fig. 3.50. Measured and simulated large-signal performances of the proposed modulator at on-state at 66 GHz.

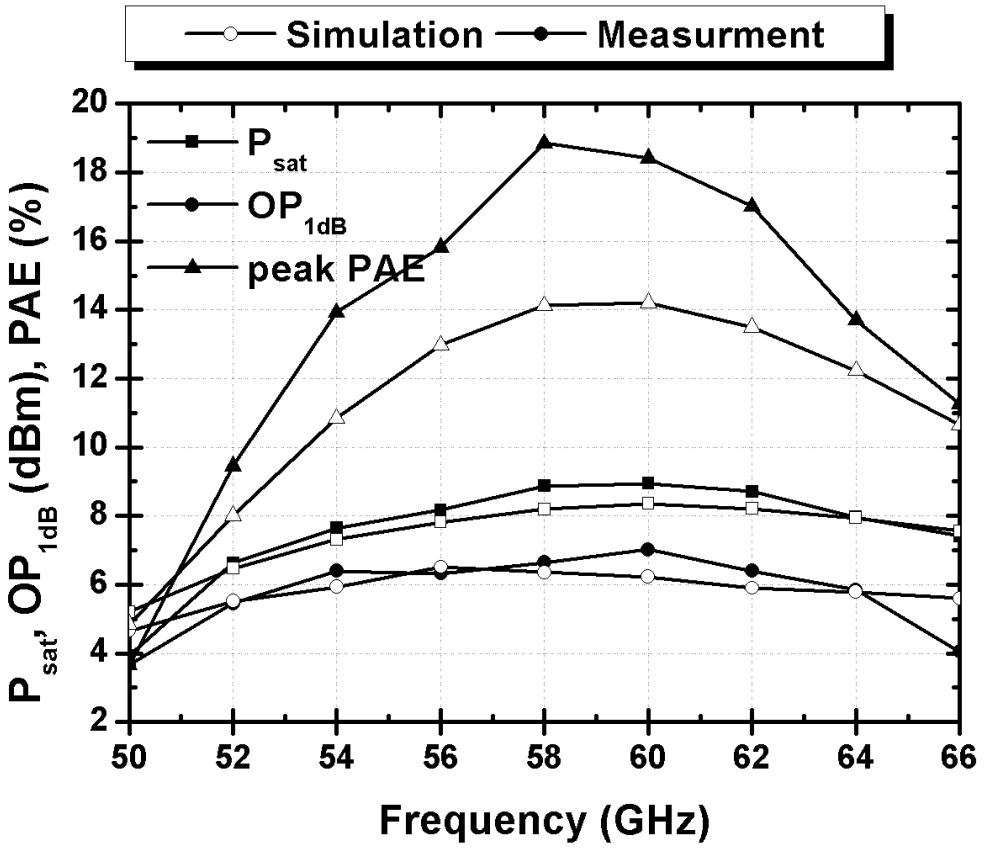

Fig. 3.51. Measured and simulated large-signal performances of the proposed modulator at on-state versus frequency.

doi:10.6342/NTU201900470

Fig. 3.52 shows the measured and post-EM simulated large-signal performances at off-state at 60-GHz. As can be seen, the measurement shows a constant P_{out} at P_{in} < 2.4 dBm, as opposed to the linear increase shown by the simulation. This is due to the limit in sensitivity of the Agilent 4419B power meter used for output power measurement. The P_{out} level (including the losses of the probe and cables) at P_{in} < 2.4 dBm is below the sensitivity of the meter, and therefore constant measured results are shown instead. Once P_{out} level is above the sensitivity of the meter at P_{in} > 2.4 dBm, the measurement and simulation start to show good agreement. The measurement shows isolation performance of > 30 dB for P_{in} < 5 dBm. Compared with the measured on-state performances shown in Fig. 3.38, this means that the modulator can be driven at high P_{in} levels for output power performances at on-state, with little compromises in isolation performance at off-state.

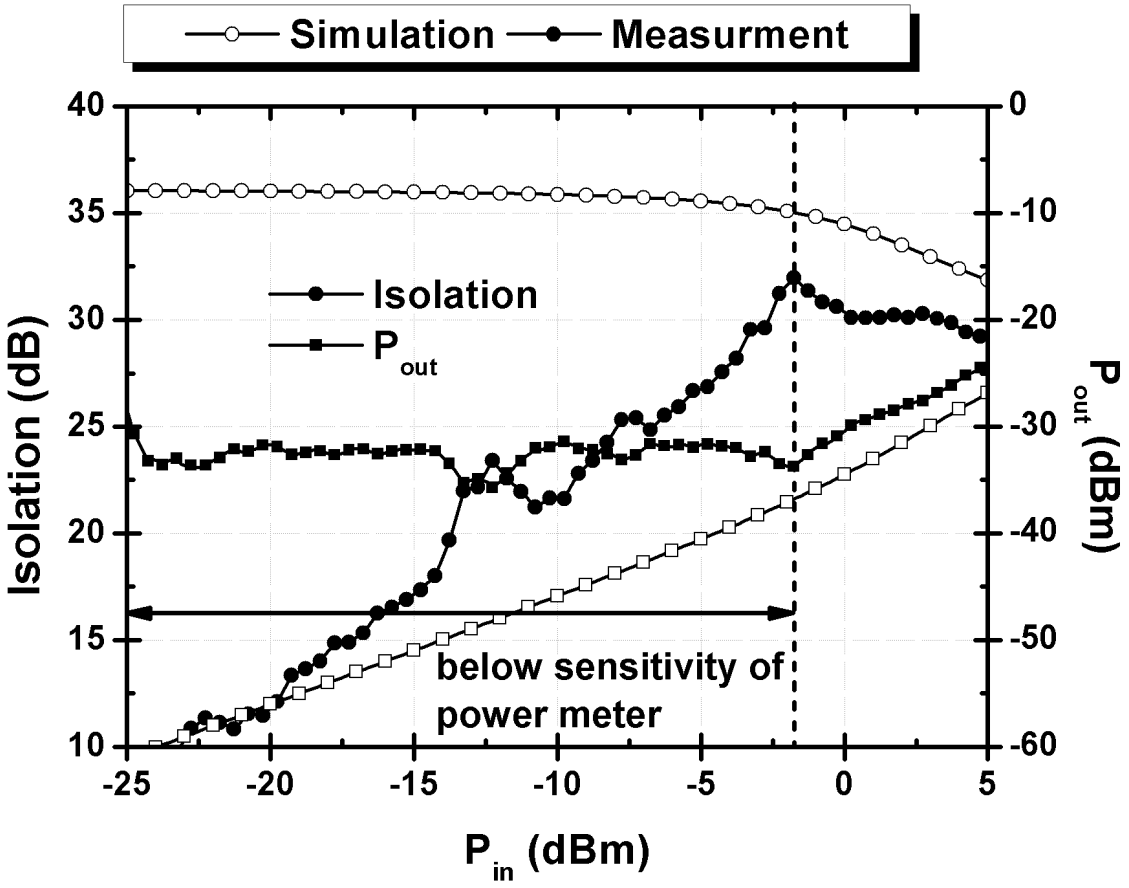

Fig. 3.52. Measured and simulated large-signal performances of the proposed modulator at off-state at 60 GHz.

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As mentioned in section 3.3, setting a relatively high $V_{G2,on}$ = 1.8 V means a $V_{p\text{-}p}$ of 1.8 V is required of the baseband data signal to switch the common-gate device on/off. This potentially poses burden on the baseband circuit and may compromises the maximum data rate. A lower $V_{G2,on}$ not only ease the burden on the baseband circuit, but also reduce the power consumption at on-state. Furthermore, a higher maximum data rate is also possible. Therefore, on-state performances of the proposed modulator under lower $V_{G2,on}$ = 1.6 V, 1.4 V, and 1.2 V were also measured.

Table 3.3 shows the bias conditions during the small-signal measurements. Fig. 3.53 to 3.55 show the measured and post-EM simulated *S*-parameters at on-state under different $V_{G2,on}$. As with the case under $V_{G2,on}$ = 1.8 V, the measured gain at 60 GHz is higher than simulation and the disagreement in S_{11} remains regardless of $V_{G2,on}$. Both the measured and simulated *S*-parameters show little difference between different $V_{G2,on}$. Gain at 60-GHz decrease only slightly with $V_{G2,on}$, but the measured gain still maintains at around 10 dB at 60 GHz under $V_{G2,on}$ = 1.2 V.

Fig. 3.56 to 3.58 show the measured and post-EM simulated large-signal performances at on-state under different $V_{G2,on}$ versus frequency. The measured and post-EM simulated output power level and efficiency decreases with $V_{G2,on}$. At 60 GHz, the measured OP_{1dB} is 7.0 dBm, 6.8 dBm, 5.6dBm, and 2.3dBm under $V_{G2,on}$ = 1.8 V, 1.6 V, 1.4 V, and 1.2V, respectively. The significant drop in output power level under lower $V_{G2,on}$ is due to the drop in device g_m, as can be seen from Fig. 3.12.

Table 3.3. Bias conditions during on/off-state small-signal measurements (continued).

V_{G1} (V)	V_{G2} (V)	V_{DD} (V)	I_{DS} (mA)	
			Simulation	**Measurement**
0.8	1.8	2.0	17	17
0.8	1.6	2.0	17	17
0.8	1.4	2.0	16	16
0.8	1.2	2.0	15	15
0.8	0.0	2.0	0	0

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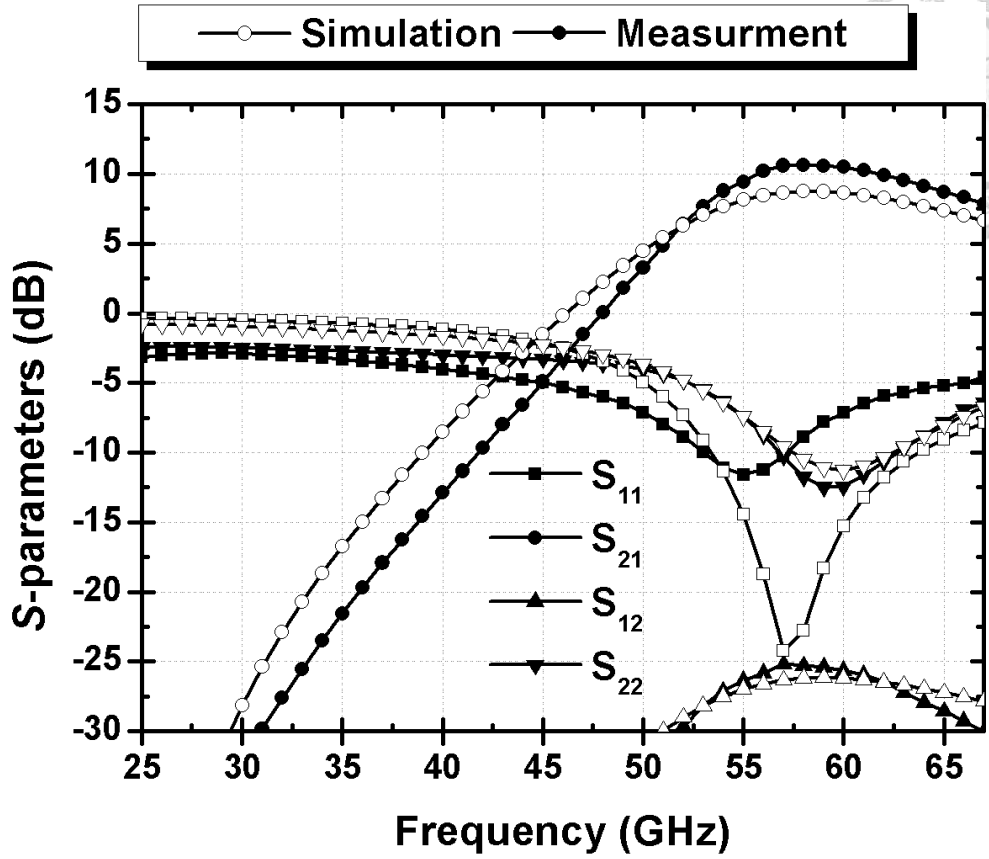

Fig. 3.53. Measured and simulated *S*-parameters of the proposed modulator at on-state with $V_{G2,on}$ = 1.6 V .

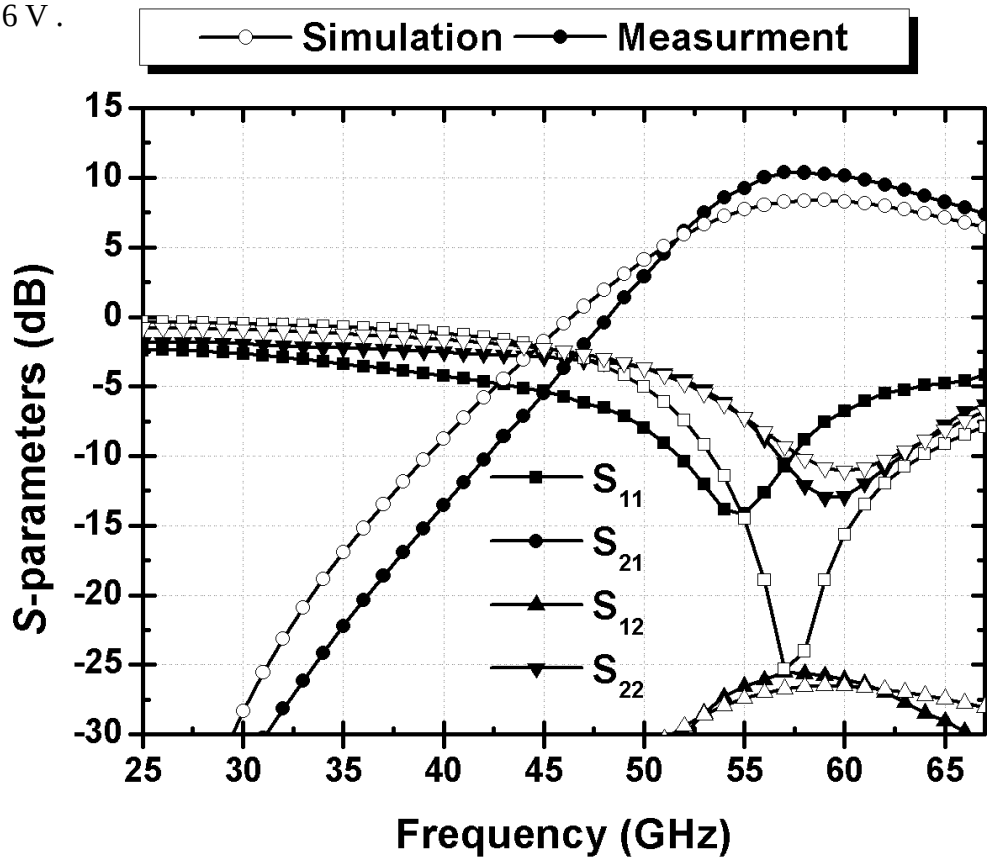

Fig. 3.54. Measured and simulated *S*-parameters of the proposed modulator at on-state with $V_{G2,on}$ = 1.4 V.

doi:10.6342/NTU201900470

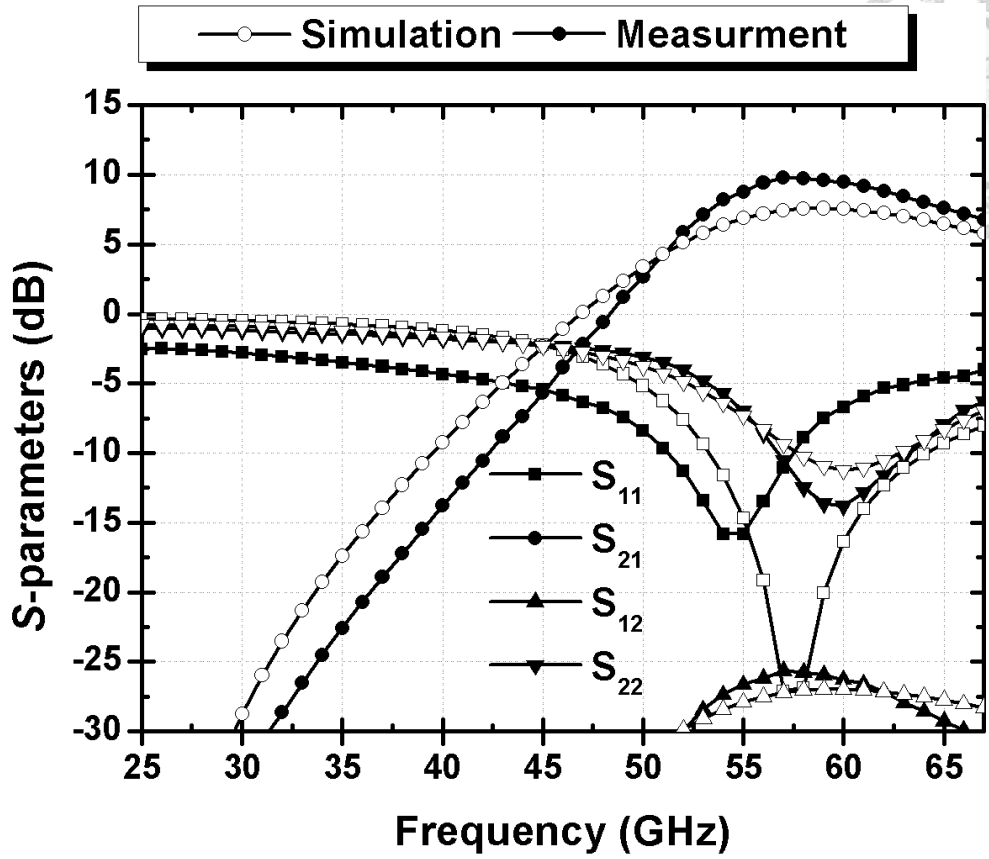

Fig. 3.55. Measured and simulated S-parameters of the proposed modulator at on-state with $V_{G2,on}$ = 1.2 V.

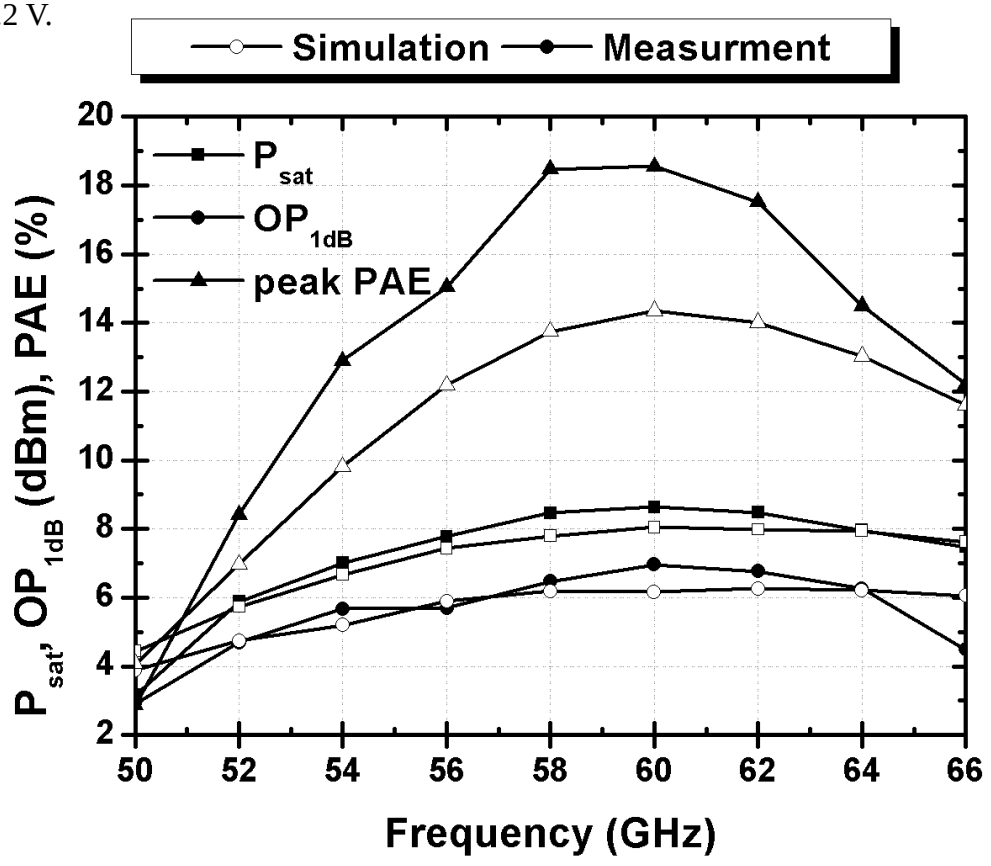

Fig. 3.56. Measured and simulated large-signal performances of the proposed modulator versus frequency with $V_{G2,on}$ = 1.6 V.

doi:10.6342/NTU201900470

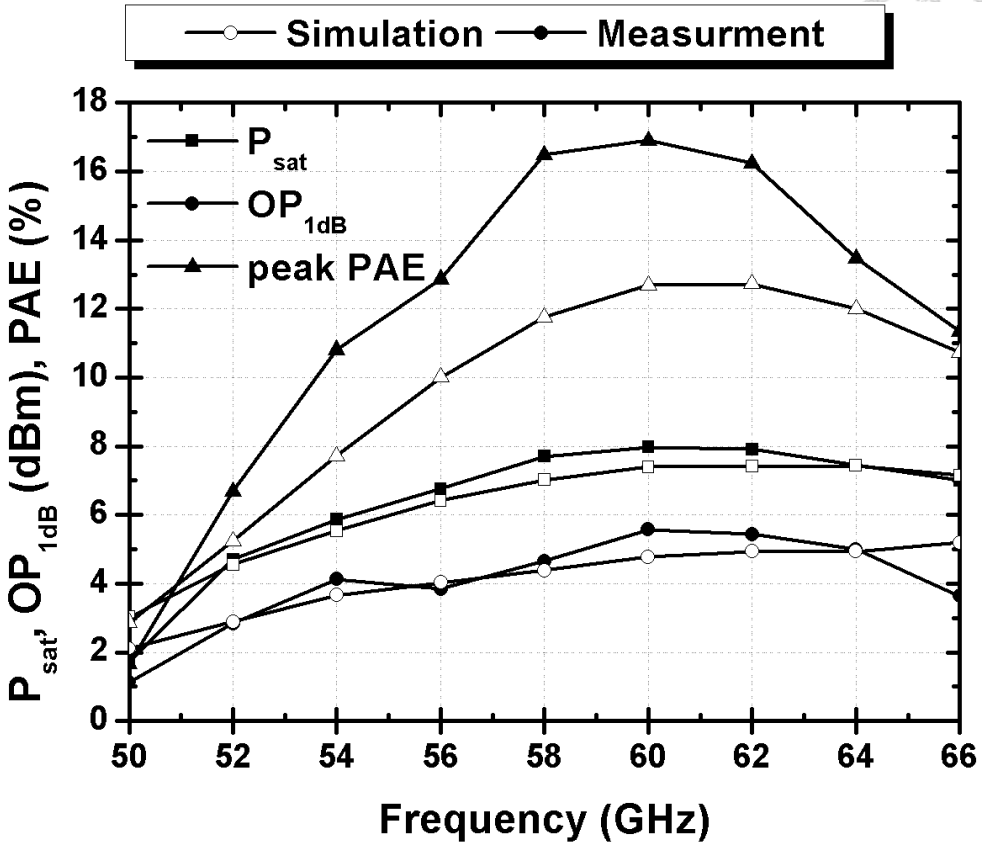

Fig. 3.57. Measured and simulated large-signal performances of the proposed modulator versus frequency with $V_{G2,on}$ = 1.4 V.

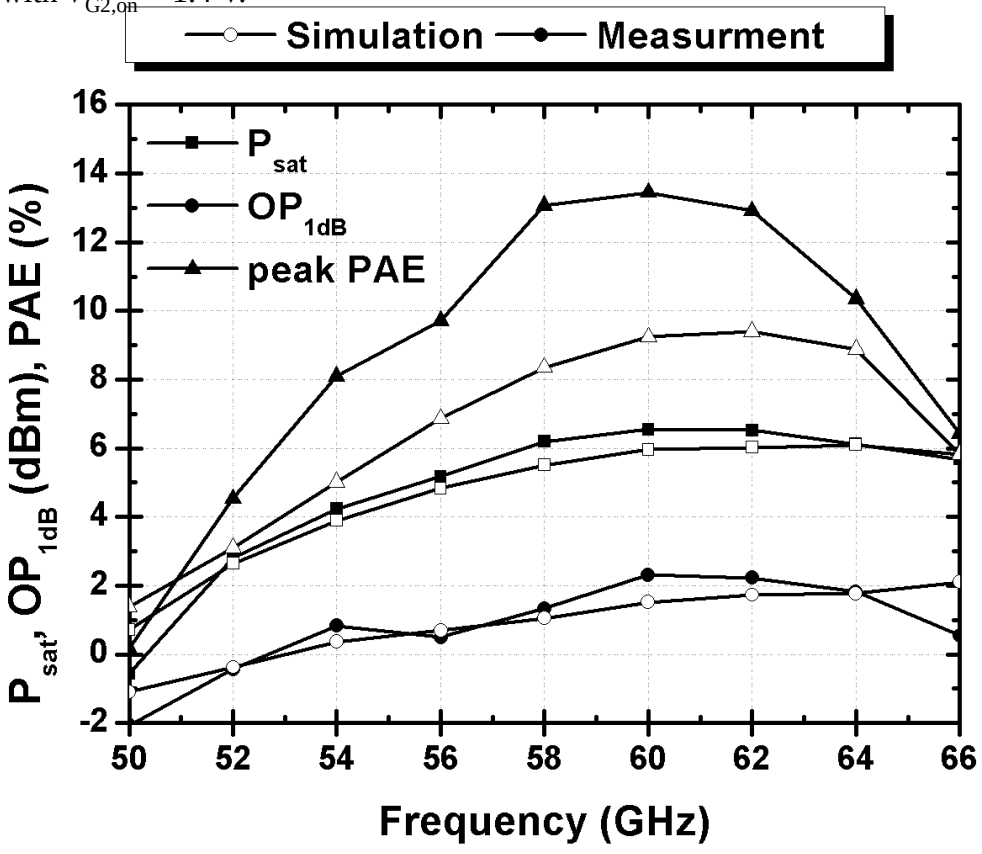

Fig. 3.58. Measured and simulated large-signal performances of the proposed modulator versus frequency with $V_{G2,on}$ = 1.2 V.

doi:10.6342/NTU201900470

3.4.2 Modulation Measurements

For modulation measurements, all RF in/output and baseband data inputs were performed using on-wafer probing. Dice were mounted on PCB boards with bond-wiring for DC applications (V_{G1} and V_{DD}). RF (carrier) input was generated using an Agilent E8257D analog signal generator. Baseband data input in the form of pseudo-random binary sequence (PRBS) data at various data rates was generated using an Anritsu MP1800A signal quality analyzer. The $V_{p\text{-}p}$ of the baseband data signal was set to 0 to $V_{G2,on}$, i.e., 0 to 1.8 V.

Fig. 3.59 shows the setup for modulation measurements in frequency-domain. The output spectrum was monitored using an Agilent E4448A spectrum analyzer with an Agilent 11974V mixer (50 to 75 GHz). Fig. 3.60 to 3.63 shows the measured output spectrum at various data rates. As can be seen, the first nulls appear at [data rate]-GHz from the 60 GHz carrier frequency, which indicates a successful modulation of the carrier signal.

Fig. 3.64 shows the setup for modulation measurements in time-domain. The output time-domain waveform was monitored using a Keysight DSAZ334A oscilloscope (with 50-GHz update). Note that due to the frequency limitation of the oscilloscope, carrier frequency of 50 GHz was used instead of 60 GHz for measurements in time-domain. Fig. 3.65 to 3.68 show the output waveform in the form of PRBS data at various data rates.

doi:10.6342/NTU201900470

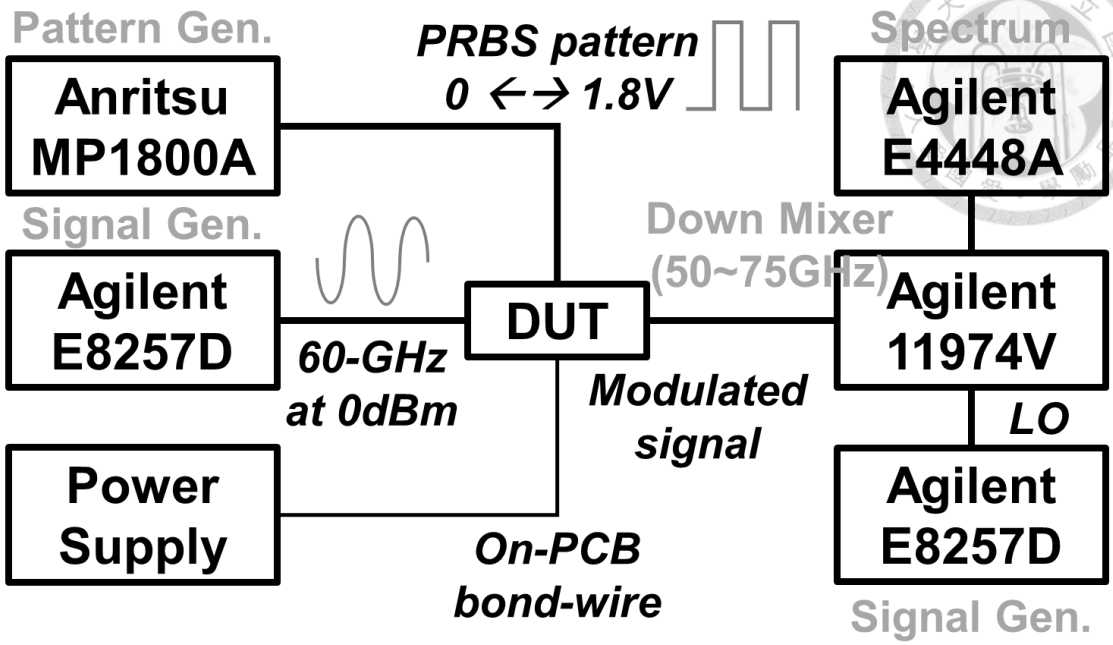

Fig. 3.59. Setup for modulation measurements in frequency-domain.

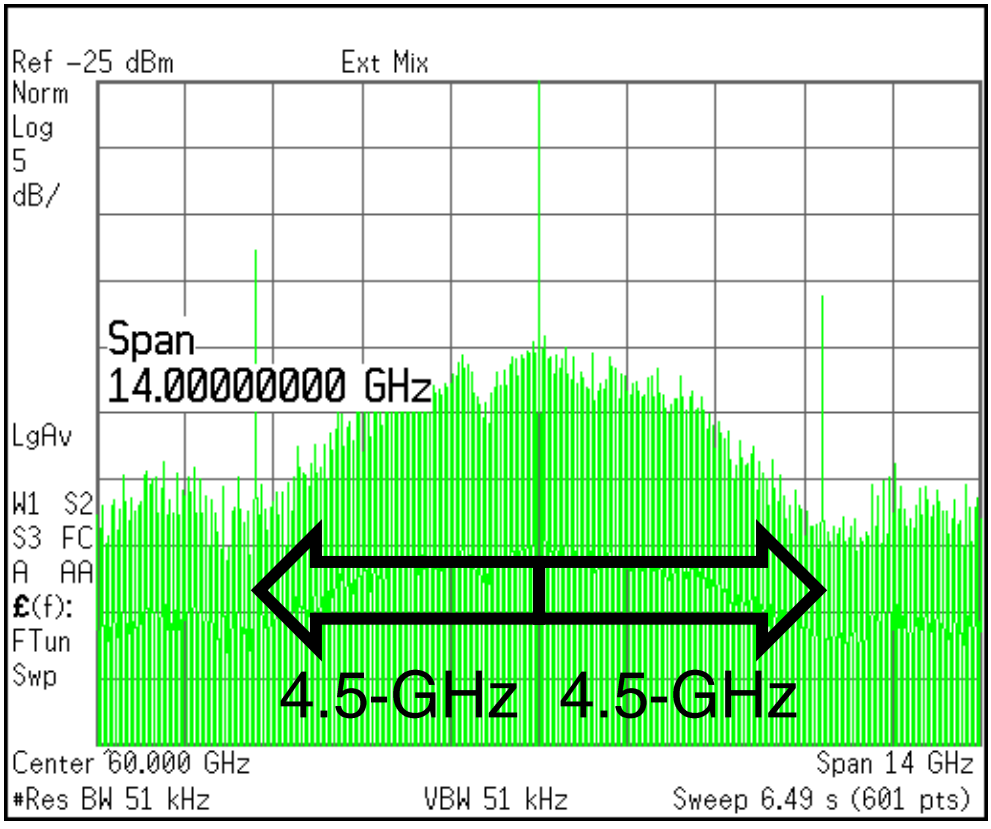

Fig. 3.60. Measured output spectrum of the modulated signal at data rate of 4.5 Gb/s.

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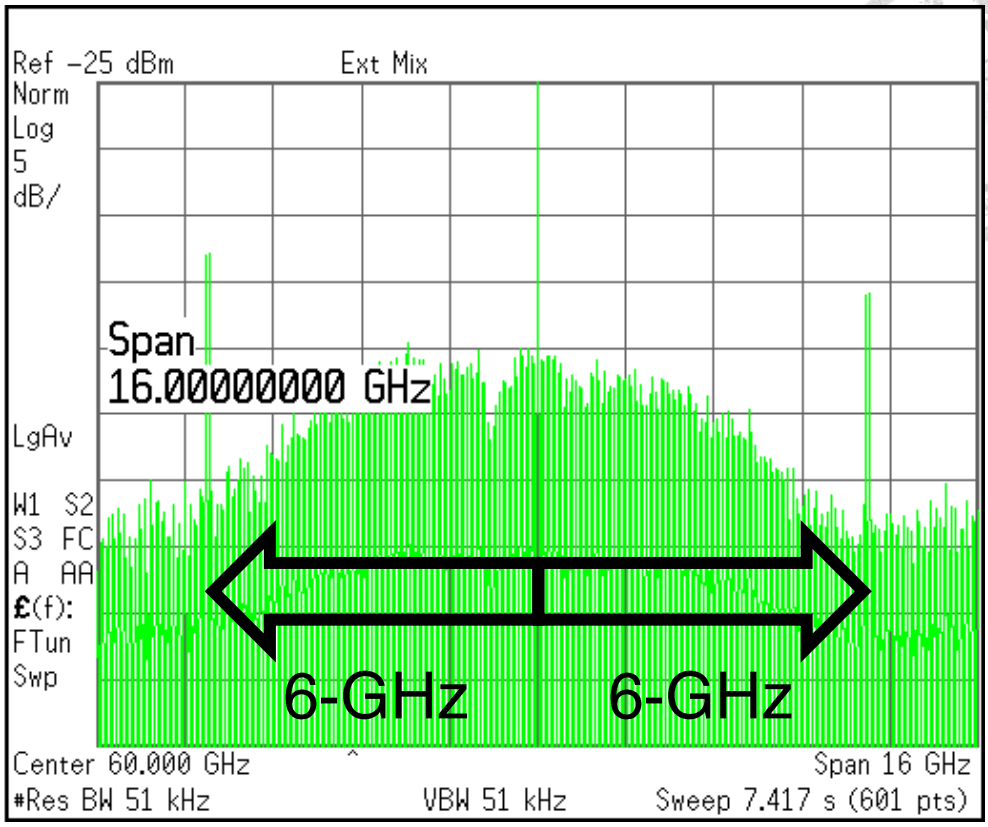

Fig. 3.61. Measured output spectrum of the modulated signal at data rate of 6 Gb/s.

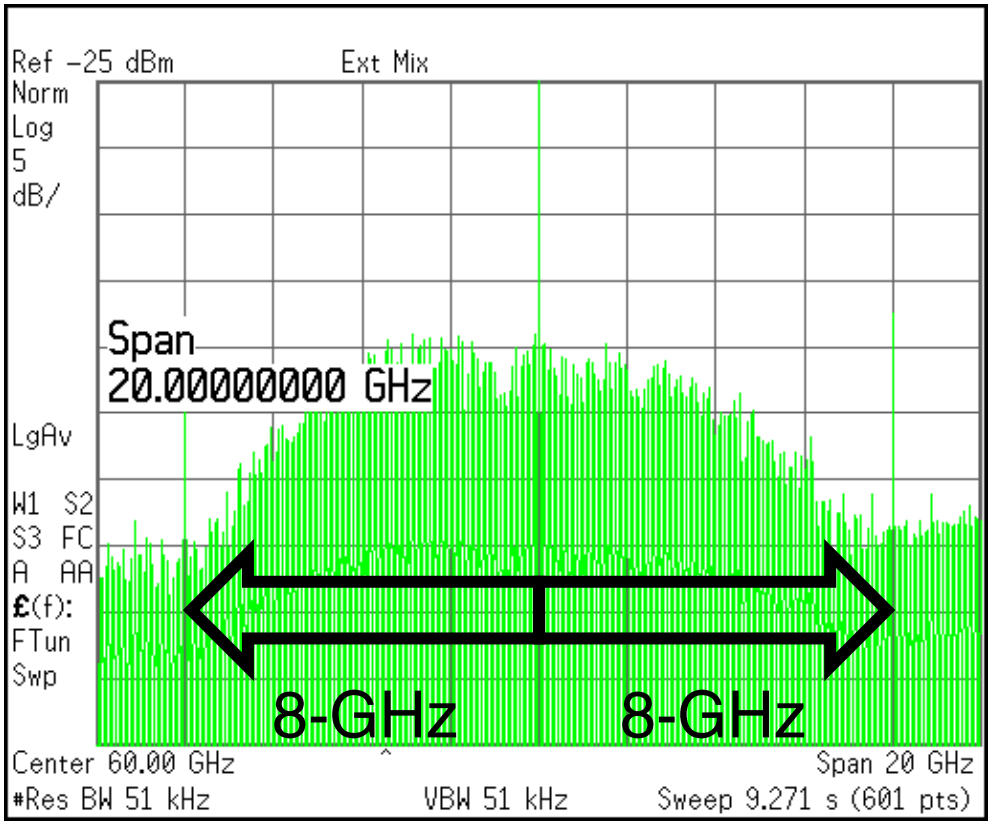

Fig. 3.62. Measured output spectrum of the modulated signal at data rate of 8 Gb/s.

doi:10.6342/NTU201900470

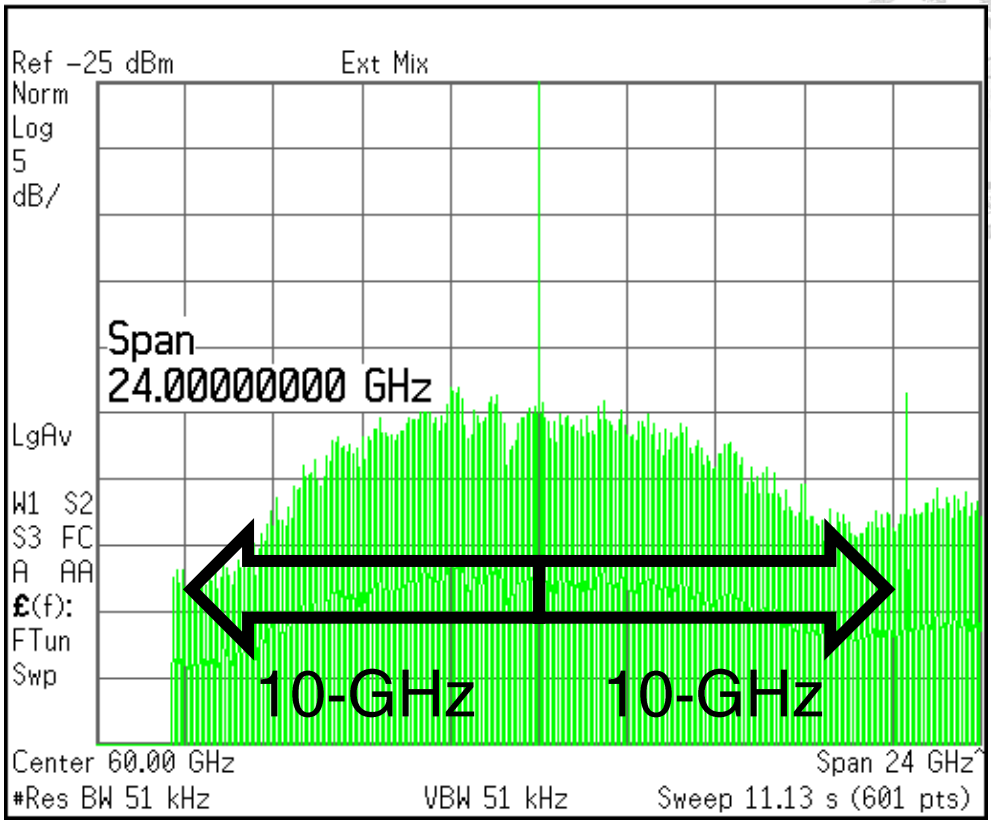

Fig. 3.63. Measured output spectrum of the modulated signal at data rate of 10 Gb/s.

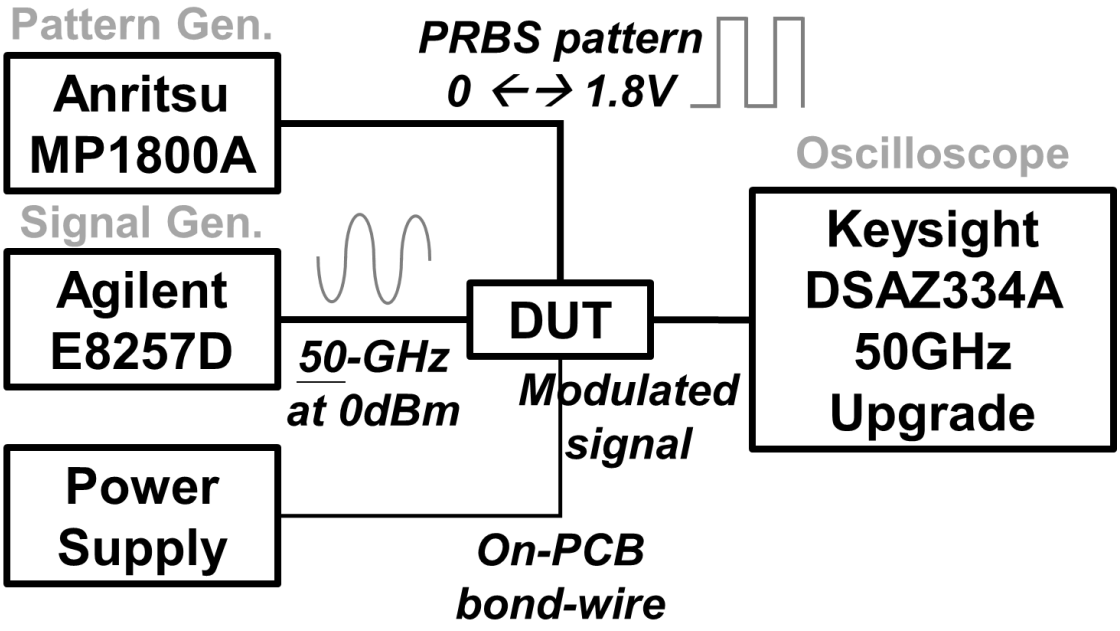

Fig. 3.64. Setup for modulation measurements in time-domain.

doi:10.6342/NTU201900470

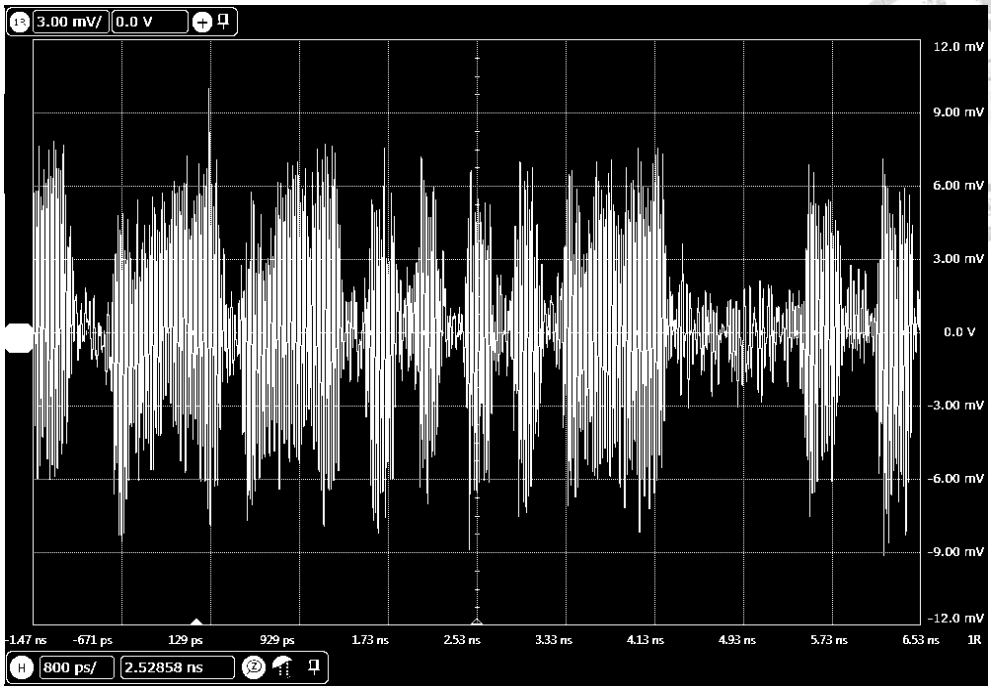

Fig. 3.65. Measured output waveform of the modulated signal at data rate of 4.5 Gb/s.

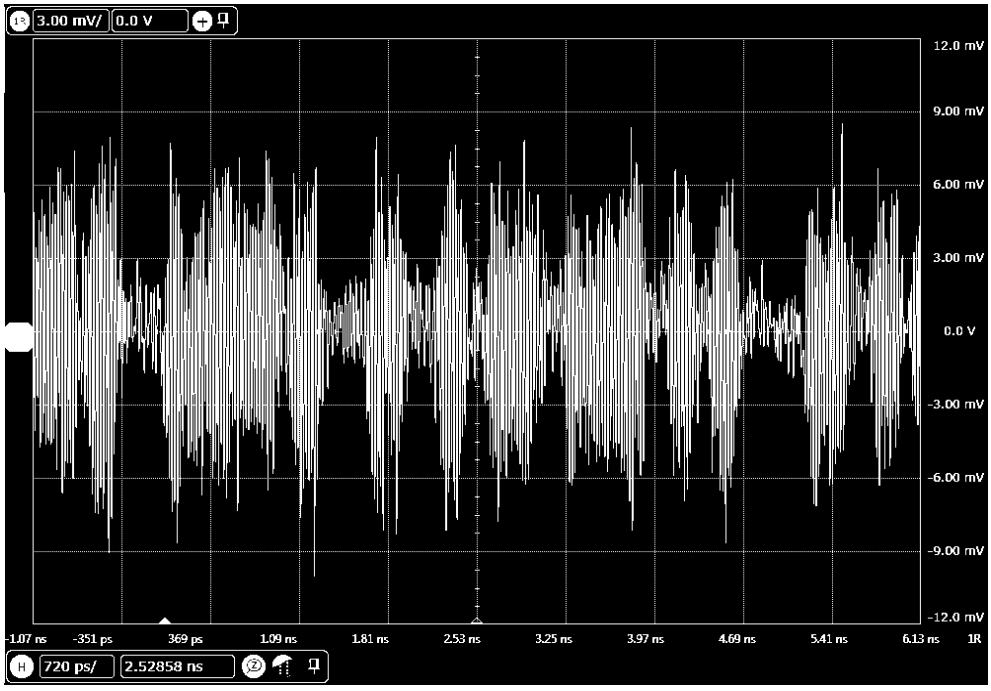

Fig. 3.66. Measured output waveform of the modulated signal at data rate of 6 Gb/s.

doi:10.6342/NTU201900470

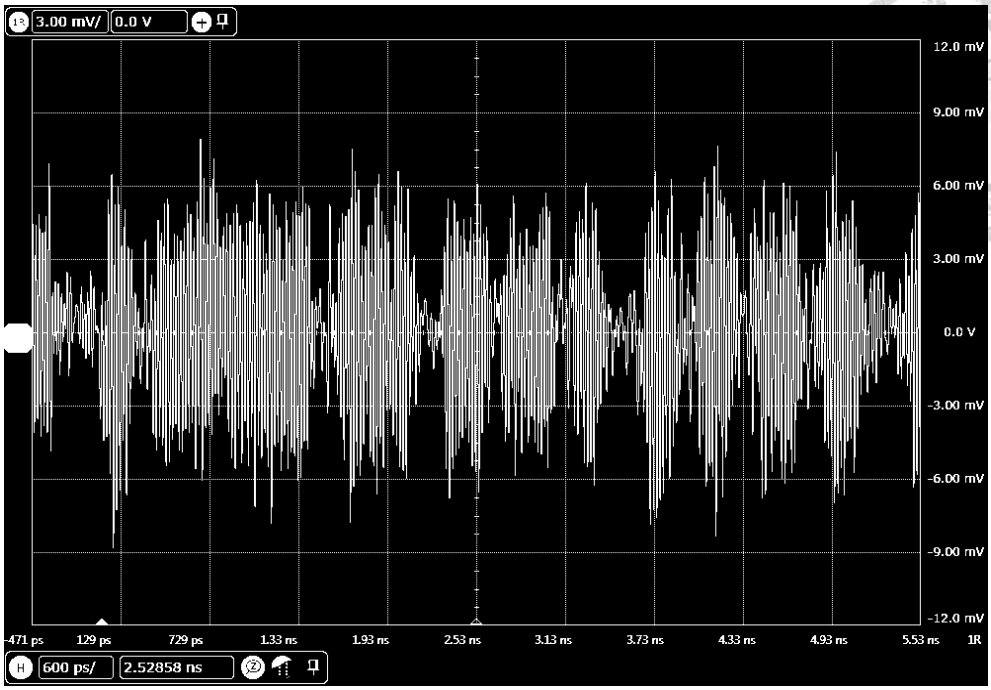

Fig. 3.67. Measured output waveform of the modulated signal at data rate of 8 Gb/s.

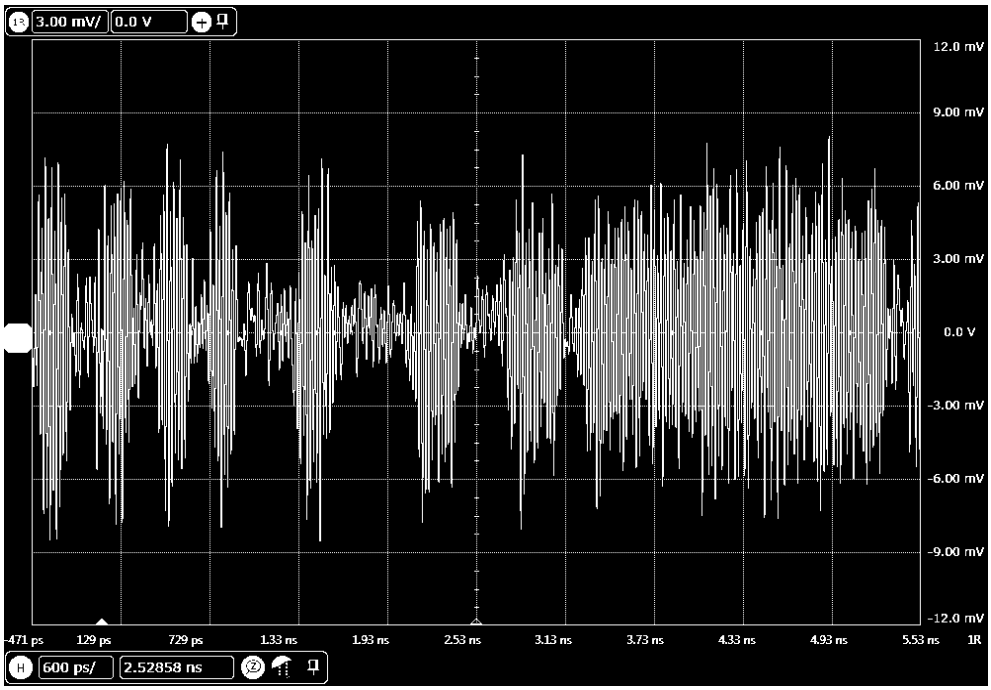

Fig. 3.68. Measured output waveform of the modulated signal at data rate of 10 Gb/s.

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3.5 Summary

In this chapter, a 60-GHz OOK modulator of the switching-amplifier configuration is proposed. By combining the functions of modulation and output amplification in a single circuit, a transmitter of lower complexity and higher efficiency can be achieved. The proposed modulator is based on a cascode circuit, in which modulation is performed by switching the common-gate device on/off. A cascode-based transformer-feedback technique is proposed for improvements in output power, gain performances at on-state, and isolation performance at off-state.

The proposed transformer feedback consists of a shunt inductor between the devices, and a series inductor at the gate of the common-gate device. At on-state, the effective inductances of the transformer eliminates the undesired effects caused by the parasitic capacitance of the devices. At off-state, coupling of the transformer enables the cancelation of the leakage signal by introducing a signal of similar magnitude and 180° phase difference. This results in improvements in performances at both on- and off-states. The transformer feedback technique has further benefits besides improvements in circuit performances. Compact physical layout of the proposed modulator can be achieved due to the small footprint of the transformer. A small core area of 261 x 469 μm^2 without RF and DC pads is possible for future applications in OOK transmitter designs. Furthermore, the transformer feedback brings the improvements at on- and off-states while requiring only a single baseband data input. This results in a lower requirement in baseband circuit components, and in turn a transmitter of lower complexity and power consumption.

While the modulator design is based on a high gate-bias of $V_{G2,on}$ = 1.8 V for optimum on-state performances, the proposed modulator maintains decent gain and on-off isolation performances with lower output power and efficiency under lower $V_{G2,on}$. Therefore, applications requiring lower $V_{p\text{-}p}$ of the baseband data signal or lower power consumptions can also be supported, with the tradeoff of a shorter transmission distance.

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For modulation, an inductor with a shunt capacitor is adopted for the baseband data input to provide isolation to the RF (carrier) frequencies instead of a large resistor. This effectively lowers the time-constant (τ) seen by the baseband data signal, and enables the modulator to achieve a maximum 10 Gb/s data rate.

As mentioned in section 2.1, the ratio E_b/N_0 between the average bit energy and the noise power spectral density directly translates to the SNR under binary modulations such as OOK, and is crucial to the bit-error-rate at the receiver end. Higher SNR at the receiver end can be achieved by increasing either the output power, or on-off isolation of the transmitter. Table 3.4 compares the proposed modulator with previous reported 60-GHz OOK modulators in CMOS processes. The propose modulator achieves the highest OP_{1dB} among the reported works, and has significant advantage in on-off performance compared to the works with OP_{1dB} greater than 0 dBm. On the other hand, the proposed modulator also has significant advantage in OP_{1dB} level over reported works with on-off isolation greater than 30 dB. Therefore, the proposed modulator proves to have state-of-the-art performance in terms of SNR, and greatly reduce the burden on the receiver to achieve a high bit-error rate. With a strong performance of maximum 10-Gb/s data rate, the proposed modulator achieves a state-of-the-art performance all-round.

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Table 3.4. Previously Reported OOK Modulator Designs in CMOS processes.

Ref.	Technology	Freq. (GHz)	Gain (dB)	OP_{1dB} (dBm)	On-Off Isolation (dB)	Data Rate (Gbps)	P_{DC} (mW)	Core Area (mm x mm)
[22]	90-nm CMOS	60	9.1	5.1	24.3	10.7	21.6	0.22 x 0.30*
[25]	90-nm CMOS	45	0	-	55	5.5	6	0.63 x 0.39*
[28]	65-nm CMOS	60	1	-	30.5	16	5	0.15 x 0.13*
[29]	0.13-μm CMOS	45-46	-	-	> 50	1	-	0.39 x 0.48^
[31]	90-nm CMOS	60	-6.6	-	26.6	8	0	0.61 x 0.30
[32]	90-nm CMOS	60	9.9	1.5	28.4	2	14.4	1.10 x 0.65*
[33]	0.18-μm BiCMOS	60	11.5	-1.5	48.0	2.5	8.1	0.40 x 0.28
[35]	0.25-μm BiCMOS	60	-1.1	-	36	20	54.6	0.20 x 0.65
This work	90-nm CMOS	60	10.2	7.0	45.4	10	34	0.26 x 0.47

* estimated from the layout

^ chip area with RF, DC pads, and the embedded VCO included

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Chapter 4 A Study on Common-mode stability of Millimeter-wave Power Amplifiers using a W-band Design in 65-nm CMOS Process

In this chapter, a W-band power amplifier (PA) with transformer-based impedance matching and power combining designed and realized in 65-nm CMOS process is presented. A transformer-based radial-symmetric power combining structure is adopted at the output for low insertion loss and matching imbalances, which are critical in PA designs at such high frequencies. Common-mode instabilities were observed and analyzed after the first tape-out. Modifications to the transformers are proposed to eliminate the common-mode instabilities, without altering the matching conditions in differential mode. The modifications proved successful in the second tape-out. Modeling issue of high frequency transformer designs is also discussed.

4.1 Introduction

Wireless communications in millimeter-wave frequencies gain many interests in recent years due to the large available bandwidth and therefore higher data rates [39]-[47], [50]. At the high frequencies of W-band, the short wavelength also provides potentials for imaging applications in area such as bio-medical research. Furthermore, wireless systems designed at W-band benefit from having smaller circuit footprints and antenna sizes. However, the low f_{max}/f_T of CMOS technologies is often the limiting factor of gain and output power performances in W-band transceiver designs.

4.1.1 Transformer-based Power Combining

Advanced nanoscale technologies such as 28, 40, and 65-nm CMOS processes has advantages of higher gain and f_{max}/f_T, which are especially critical in amplifier designs at millimeter-wave frequencies. However, shorter gate-lengths lead to lower breakdown voltages, which in turn limit the supply voltage. This poses challenges to PA designs in achieving high levels of output power. Power combining is widely used for increasing the output power under low supply voltages [47]-[50]. Due to the short wavelength at millimeter-wave frequencies, the phase difference

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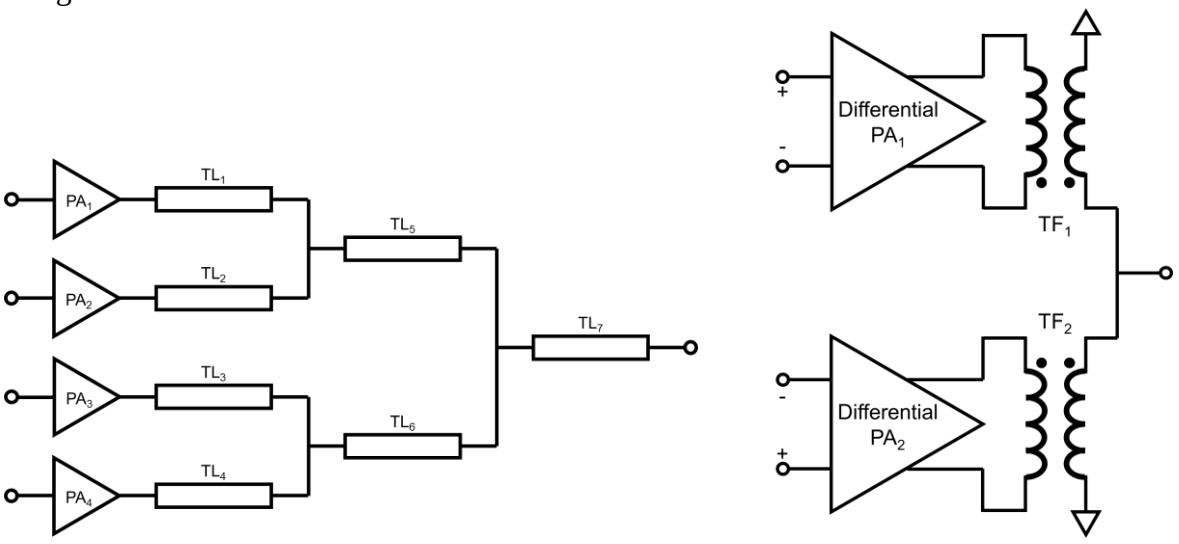
between combining paths becomes highly sensitive to any physical asymmetry of the power combining structure. Phase difference between combining paths degrades the combined power, and therefore the amplifier efficiency. Fig. 4.1 shows two commonly used structure for in-phase power combining in millimeter-wave PA designs. In Fig. 4.1(a), binary power combining uses transmission lines for the purposes of both in-phase power combining and impedance matching. A wideband performance can often be achieved with careful design of the transmission lines [44]-[46], [50]. However, a large transformation ratio between the optimal impedance of the devices and the load impedance leads to longer transmission lines, and therefore higher insertion losses. Furthermore, transmission lines often take up large layout footprint, even at millimeter-wave frequencies. In Fig. 4.1(b), transformer-based power combining has stood out in millimeter-wave PA designs recently [39], [48]-[49]. Transformers also serves the purposes of both in-phase power combining and impedance matching, but in a much more compact layout footprint than transmission lines. Since a large impedance transformation ratio does not necessarily translate to a large insertion loss of the transformer, the technique is especially suited for multi-way, high output power PA designs.



(a) (b)

Fig. 4.1. Commonly used power combining structures: (a) binary power combining (b) transformer-based power combining.

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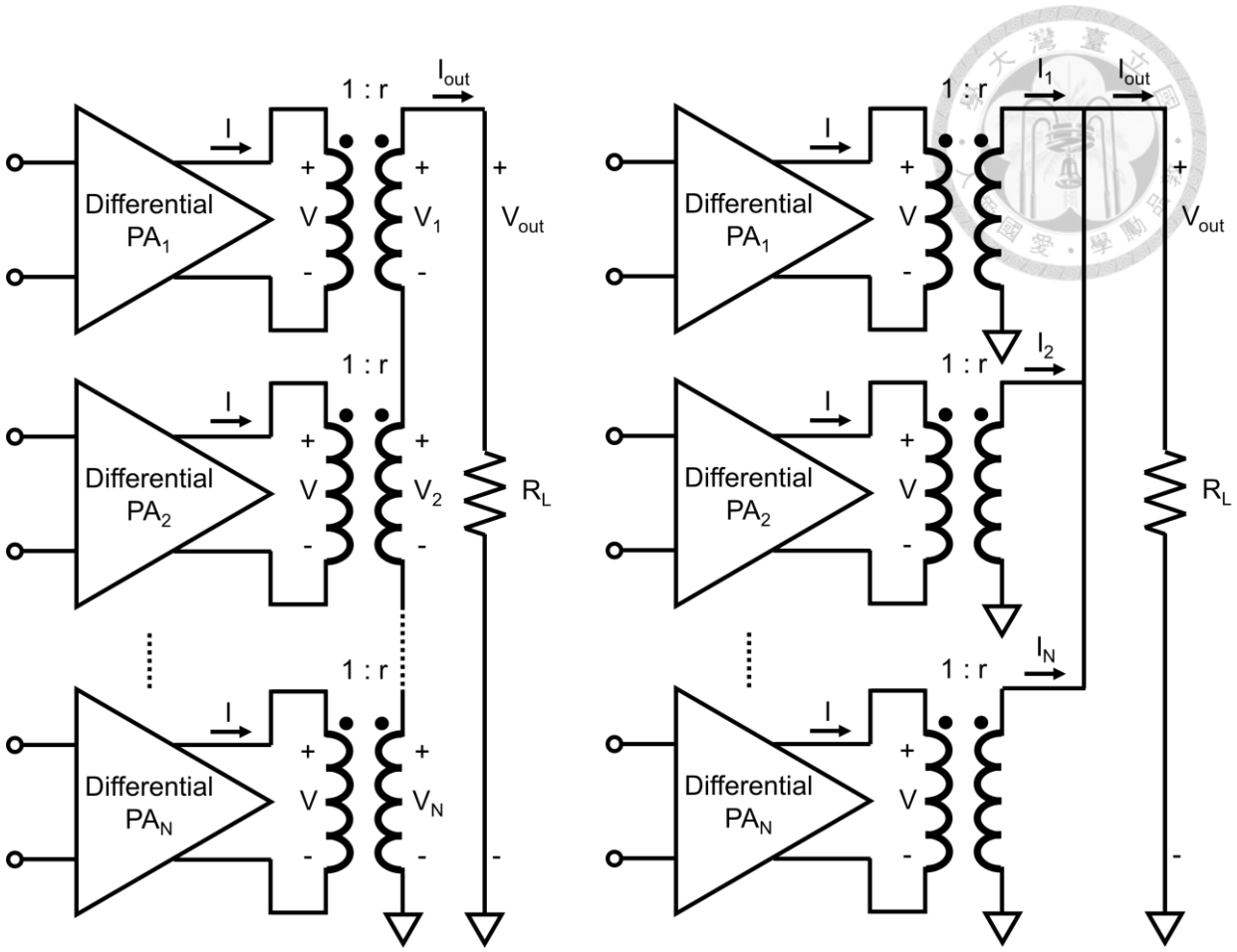

Fig. 4.2. Schematics of (a) voltage-combining configuration, and (b) current-combining configuration of transformer-based power combining.

Fig. 4.2 shows two different configurations of transformer-based power combining, in which power is combined through voltage- and current-combining, respectively. In Fig. 4.2(a), the voltage is combined by cascading the secondary coils of the transformers. The output voltage and current are given by

$$V_{\text{out}} = V_1 + V_2 + \ldots + V_N = N \cdot rV \quad , \tag{4.1}$$

and

$$I_{\text{out}} = \frac{1}{r} I \ , \tag{4.2}$$

in which N denotes the number of combining, V denotes the voltage across each of the primary coils, I denotes the current through each of the primary coils, and r denotes the inductance ratio between

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the secondary and primary coils. From (4.1) and (4.2), in order to transform the load impedance R_L to the optimum output impedance R_{opt} of the differential PA cell, the required impedance transformation ratio is given by

$$\frac{R_L}{R_{opt}} = \frac{V_{out} / I_{out}}{V / I} = r^2 N \quad . \tag{4.3}$$

Thus, transformers of inductance ratio

$$r = \sqrt{\frac{1}{N} \cdot \frac{R_L}{R_{opt}}} \tag{4.4}$$

is required.

In Fig. 4.2(b), the current is combined by connecting the output of the secondary coils. The output voltage and current are given by

$$V_{out} = rV \ , \tag{4.5}$$

and

$$I_{out} = I_1 + I_1 + \ldots + I_N = N \cdot \frac{I}{r} \quad . \tag{4.6}$$

From (4.5) and (4.6), in order to transform the output impedance R_L to the optimum output impedance R_{opt} of the device, the required impedance transformation ratio is given by

$$\frac{R_L}{R_{opt}} = \frac{V_{out} / I_{out}}{V / I} = \frac{r^2}{N} \quad . \tag{4.7}$$

Thus, transformers of inductance ratio

$$r = \sqrt{N \cdot \frac{R_L}{R_{opt}}} \tag{4.8}$$

is required.

From (4.4) and (4.8), the voltage-combining configuration has the advantage of a larger impedance transformation ratio for multi-way, i.e., $N \geq 2$, power combining. Transformers with turn ratios of 1:1 often meets the requirement of impedance transformation. On the other hand,

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transformers with $r > 1$ and often turn ratios of 2:1 are required if the current-combing configuration is to be used for multi-way power combining. This leads to more complexity and potentially more insertion loss in the transformer design.

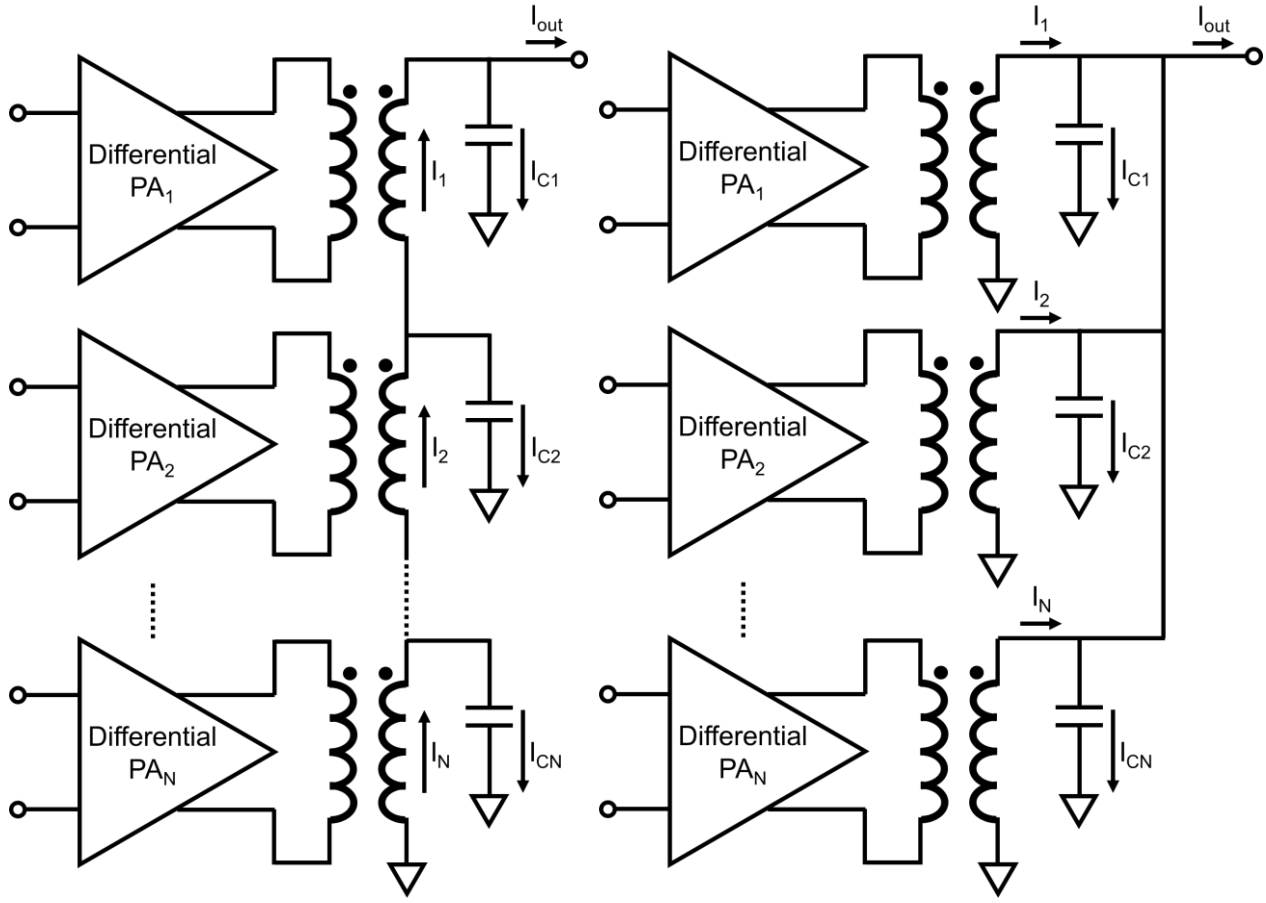

Fig. 4.3. Schematics of (a) voltage-combining configuration, and (b) current-combining configuration of transformer-based power combining, with the parasitic capacitances considered.

Fig. 4.3 shows the two configurations of transformer-based power combining with the shunt parasitic capacitances from the transformers considered. In the case of single-ended output, cascading of the transformer secondary coils in the voltage-combining configuration leads to a single current path at the output. With the shunt parasitic capacitances from the transformers, this leads to different impact from the leakage currents on each of the combining paths,

$$I_{out} = I_1 - I_{C1} = I_2 - I_{C2} - I_{C1} = I_N - I_{CN} - \ldots - I_{C1} \quad . \tag{4.9}$$

On the other hand, current is distributed evenly among the combining paths in the

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current-combining configuration. Therefore, while the leakage currents from the parasitic capacitances are still present, the symmetric nature of the configuration means the impacts on each of the combining paths are the same,

$$\frac{I_{out}}{N} = I_1 - I_{C1} = I_2 - I_{C2} = I_N - I_{CN} \quad . \tag{4.10}$$

Therefore, the impedance seen by each of the differential PA cells suffer greater imbalances in the voltage-combining configuration. The imbalance leads to different impedances seen by each differential PA cells and degrades the efficiency of power combining, which in turn degrades the output power and power-added-efficiency (PAE) performances of the overall PA. As the frequency and the number of combining paths increases, the effect of imbalance becomes more prominent. Thus, the current-combining configuration is more suited for multi-way PA designs at millimeter-wave frequencies. However, the low impedance transformation ratio is a tradeoff to be considered when adopting the current-combining configuration.

4.2 Circuit Design

The proposed W-band PA is targeted at saturated output power (P_{sat}) of 15 dBm at 110 GHz. To reach the target output power at W-band, multi-way power combining is required at the output.

4.2.1 Neutralization Technique

In PA designs, devices with relatively large gate-periphery are often used to achieve higher output power levels. However, the intrinsic gate-to-drain capacitance C_{gd} also increases with the device gate-periphery. A larger C_{gd} leads to worse reverse isolation of the device, which in turn degrades both gain and stability. Furthermore, the PAE of PA designs will suffer from poor gain performance of the output stage. As PA designs enter millimeter-wave frequencies, the effect of C_{gd} becomes more prominent.

Neutralization technique cancels the effect of intrinsic C_{gd} by introducing an equivalent negative capacitance $-C_N$ [51]. As shown in Fig. 4.4, the technique can be implemented using

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cross-coupled capacitors between the gate and drain of two devices in differential mode to eliminate the effect of C_{gd}. In addition to increased gain and stability, another benefit of adopting neutralization is that it makes little difference on the impedances for optimal large-signal performance of the devices. Therefore, the design of impedance matching networks will not be more complicated because of adopting the neutralization technique.

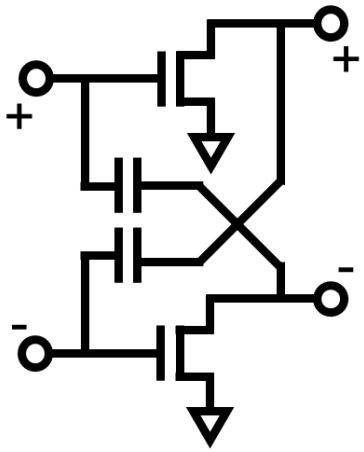

Fig. 4.4. Schematic of neutralization technique implementation in differential mode with cross-coupled capacitors between device gate and drain.

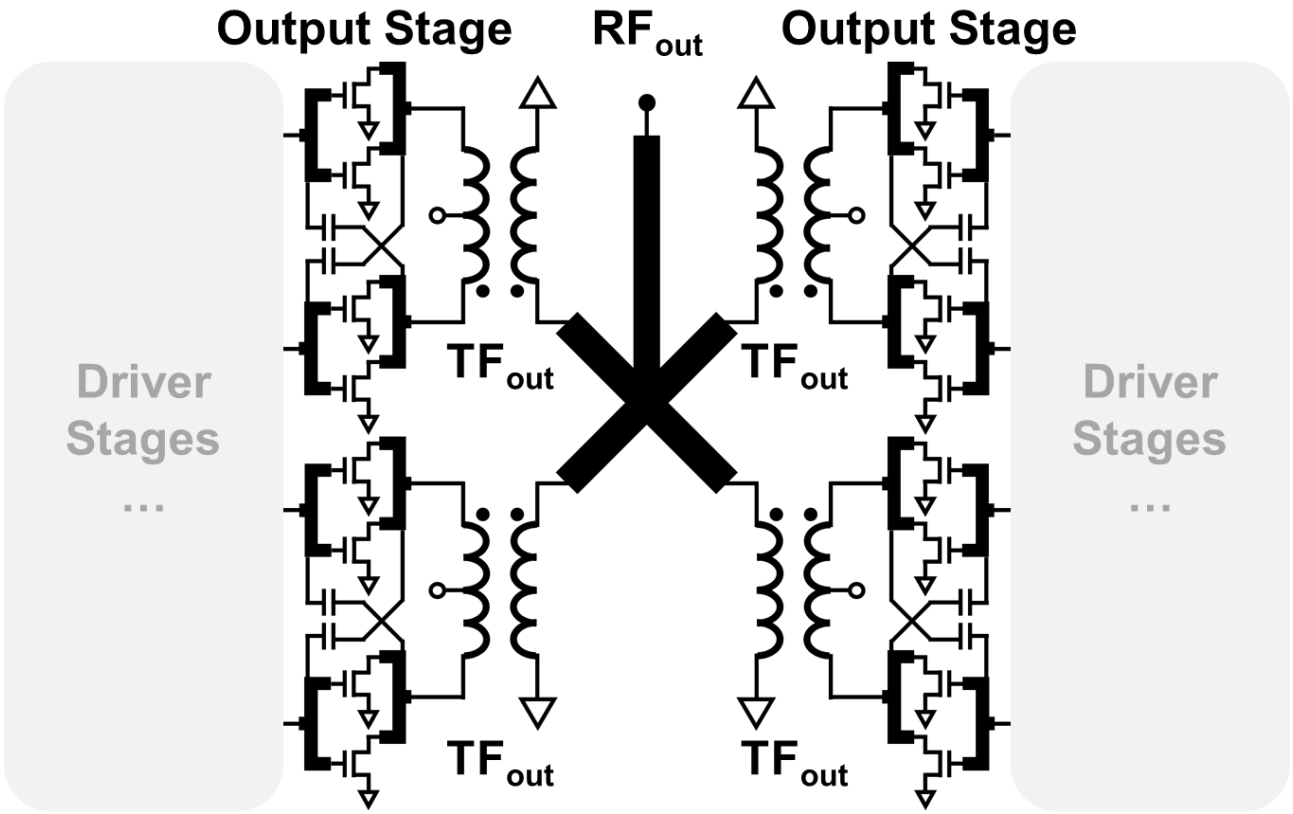

Fig. 4.5. Schematic of the output stage complete with the four-way transformer-based power combiner.

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4.2.2 Device Selection and Output Stage Design

In order to achieve the overall target P_{sat} of 15 dBm and have reasonable gain at the output stage, four-way transformer-based power combining is adopted at the output stage. As discussed in section 4.1, current-combining configuration is chosen since symmetric characteristic of the combiner is especially critical for PA designs with multi-way combining at such high frequencies. Fig. 4.5 shows the schematic of the output stage with the four-way transformer-based power combiner [48]. The output stage consists of four differential pairs, each of which consists of two common-source (CS) amplifier cells and cross-coupled neutralization capacitors. The P_{sat} of a single CS amplifier cell can be estimated using the load-line theory as

$$P_{sat} = \frac{1}{2} \times \frac{V_{max} - V_{min}}{2} \times \frac{I_{max}}{2} \quad . \tag{4.11}$$

At around 110 GHz, a 2 dB insertion loss is estimated for the four-way transformer-based combiner. Thus, a $P_{sat} \geq 8$ dBm from each of the eight CS amplifier cells is required to achieve the overall target P_{sat} of 15 dBm. Fig. 4.6 shows the DC-IV curves of the device with gate-periphery of 32f x 1μm. From (4.11), P_{sat} of around 8.5 dBm can be estimated at V_{DS} = 1.2 V, which provides enough margin for the 8 dBm target. Fig. 4.7 shows the g_m and I_{DS} of the 32f x 1 μm device versus V_{GS} at V_{DS} = 1.2 V . The device reaches peak g_m at V_{GS} = 0.8V, and therefore the bias condition is set to [V_{GS}, V_{DS}] = [0.8 V, 1.2 V].

Different configurations of a total 32-μm gate-periphery is then compared at the selected bias condition of [V_{GS}, V_{DS}] = [0.8V, 1.2V]. As can be seen in Fig. 4.8, the simulated MSG/MAG of two parallel-combined 16f x 1 μm devices is higher than a single 32f x 1 μm device. The parasitic capacitance is effectively reduced by splitting a single into two parallel-combined devices with half of the gate-peripheries, which leads to a higher MSG/MAG. Despite the benefit of a higher gain, further splitting of the devices leads to larger and more complicated physical layout. Therefore, the two parallel-combined 16f x 1 μm devices is used as the configuration for the eight CS amplifier

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cells of the output stage.

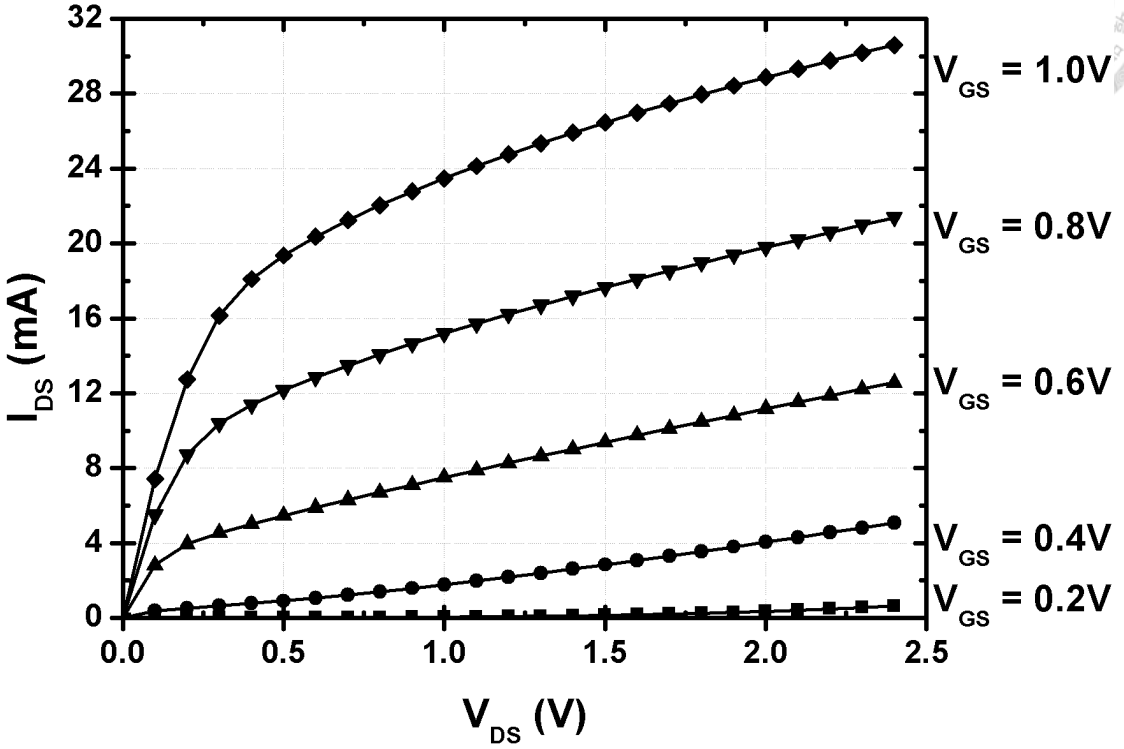

Fig. 4.6. Simulated DC-IV curves of the device with gate-periphery of 32f x 1 μm.

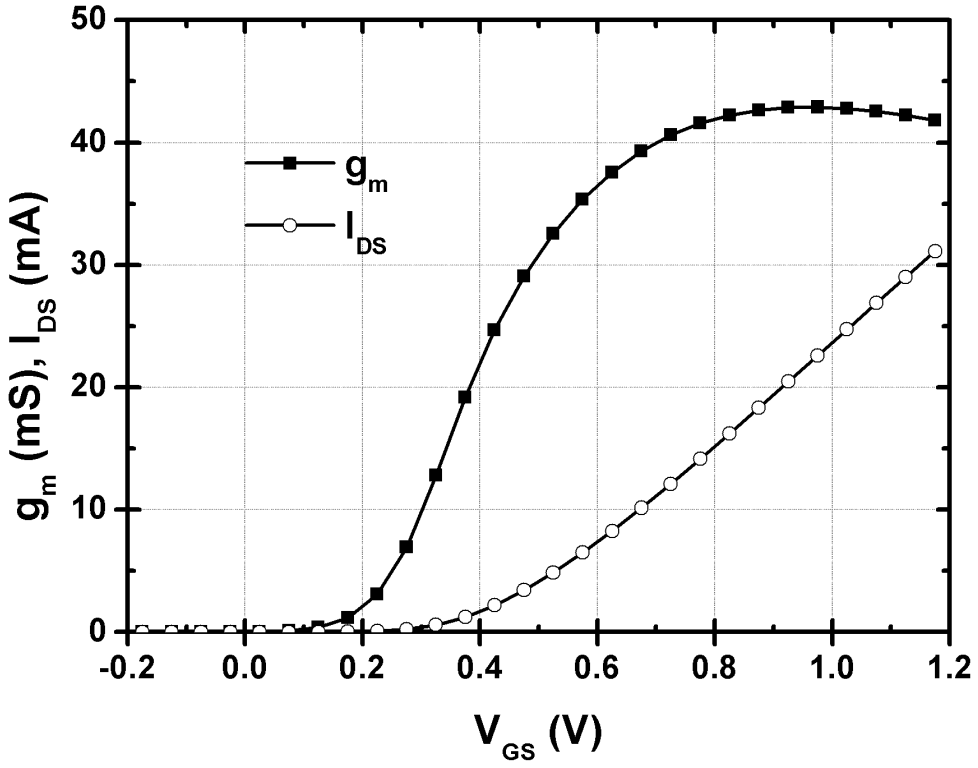

Fig. 4.7. Simulated g_m and I_{DS} of the 32f x 1 μm device versus V_{GS} at V_{DS} = 1.2 V.

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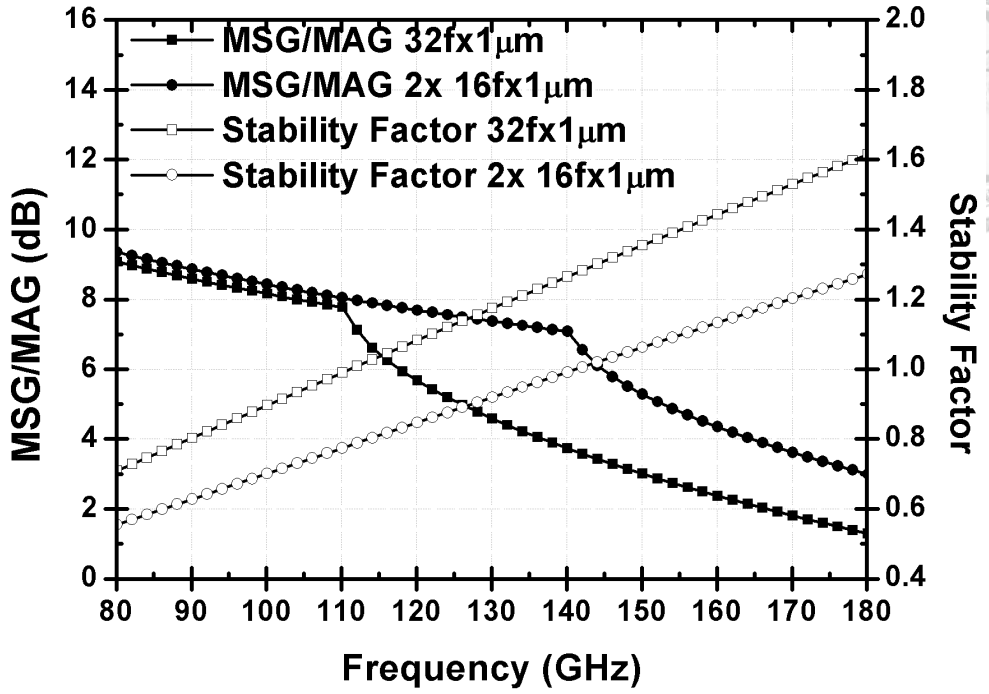

Fig. 4.8. Simulated MSG/MAG and stability factor of a single 32f x 1 μm device compared with two parallel-combined 16f x 1 μm devices.

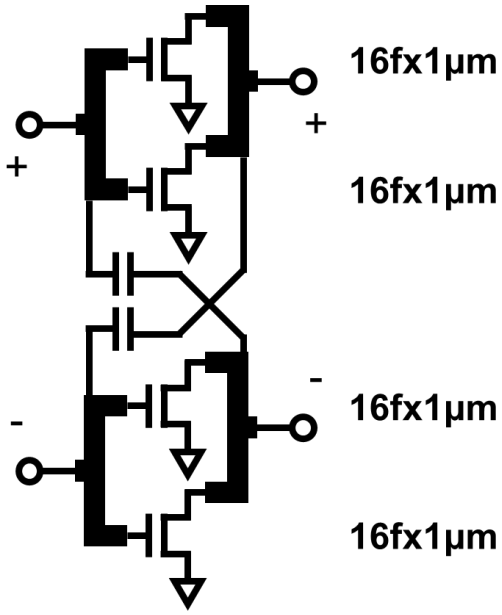

Fig. 4.9. Schematic of the output stage differential pair with four 16f x 1 μm devices.

Fig. 4.9 shows the circuit schematic of the differential pair used at the output stage. Two cross-coupled capacitances C_N are adopted for the neutralization technique. Fig. 4.10 shows the simulated MSG/MAG and stability factor of the differential pair at 110 GHz versus different values of C_N. The differential pair reaches maximum gain increase at C_N = 13.5 fF, and is most stable at C_N = 10 fF. Considering a potential ± 20% variation of capacitance during fabrication, C_N of 12 fF is

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chosen for added stability and 2 dB of gain improvement at 110 GHz. Multi-digit capacitors consisting of metal-7, 8, and 9 layers are used for the requirements of both a small 12 fF capacitance and a compact layout footprint. Since the physical layout of the differential pair around the devices is rather compact and complicated, results from the pre- and post-EM simulations may differ significantly. To avoid the time-consuming process of redesigning, EM simulations of the differential pair are performed before starting the design of matching networks. Fig. 4.11 shows the post-EM simulated MSG/MAG and stability factor of the differential pair. By adopting the neutralization technique, increase in stability and in the MSG/MAG at 110 GHz by 2 dB is achieved. The optimum load impedance $Z_{opt3,diff}$ for P_{sat} performance can be obtained through load-pull simulation. Fig. 4.12 shows the power contours of the post-EM simulated differential pair. The differential pair achieves P_{sat} of 11.5 dBm and PAE of 26.04% with optimum load impedance $Z_{opt3,diff}$ = 24.23 + j39.85 Ω at 110 GHz.

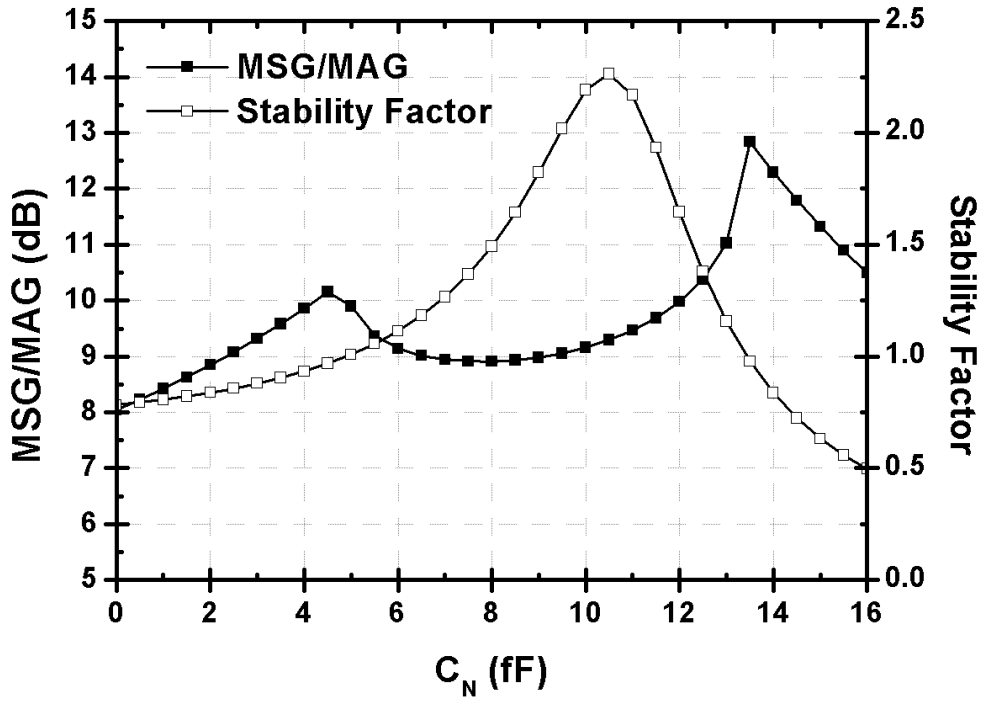

Fig. 4.10. Simulated MSG/MAG and stability factor of the output differential pair at 110 GHz versus different values of C_N.

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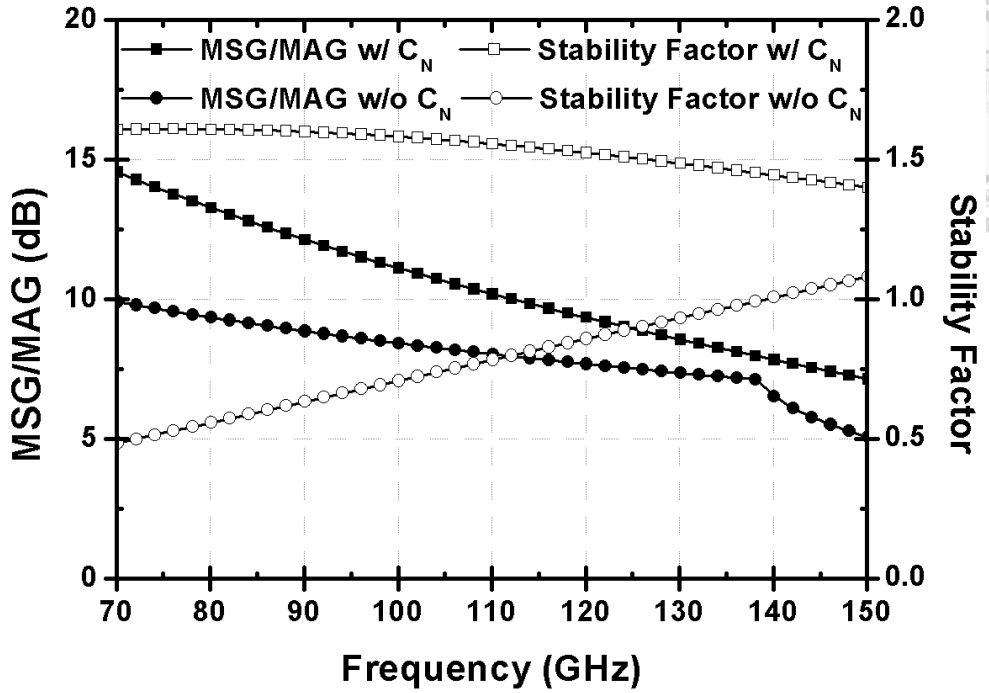

Fig. 4.11. Post-EM simulated MSG/MAG and stability factor of the output differential pair.

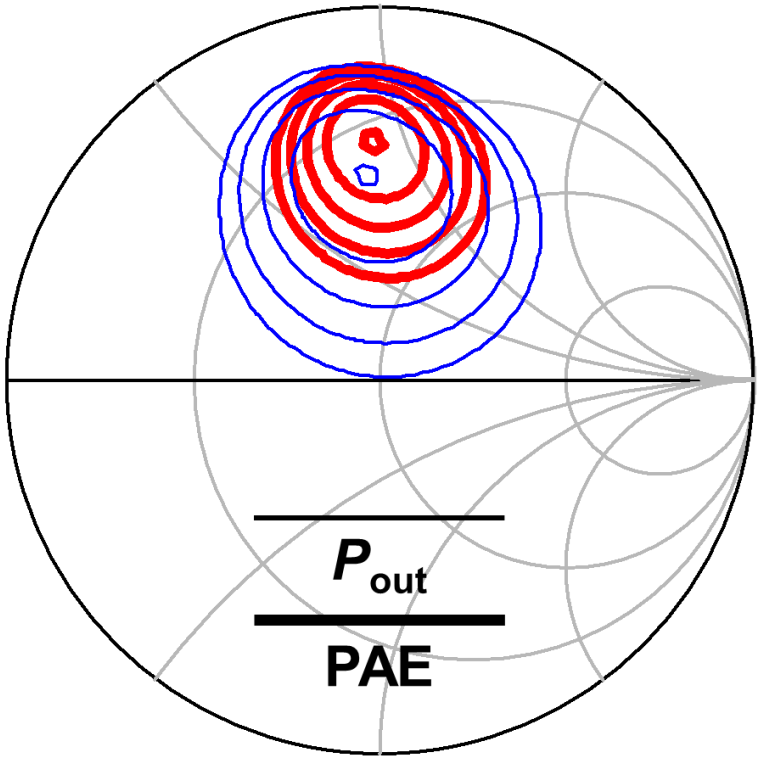

Fig. 4.12. Post-EM simulated power contours of the output differential pair.

As can be seen in Fig. 4.5, each differential pair is followed by a differential-to-single transformer to form the four-way power combining structure. Symmetrical 50-Ω micro-strip lines are used for in-phase power combining of the four transformers before connecting to the output

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through another 50-Ω micro-strip line. As previously reported in [48], the radial-symmetric configuration minimize the length and therefore the insertion loss of the micro-strip lines used for power combining during physical layout. This also result in the transfer of load impedance at the output, i.e., Z_L = 50 Ω, to 4 x 50 Ω seen by the transformers looking towards the output. To transfer 200 Ω to $Z_{opt3,diff}$ with the lower impedance transformation ratio of the current-combining configuration, transformers with 1:2 turn ratio and high coupling coefficients are required.

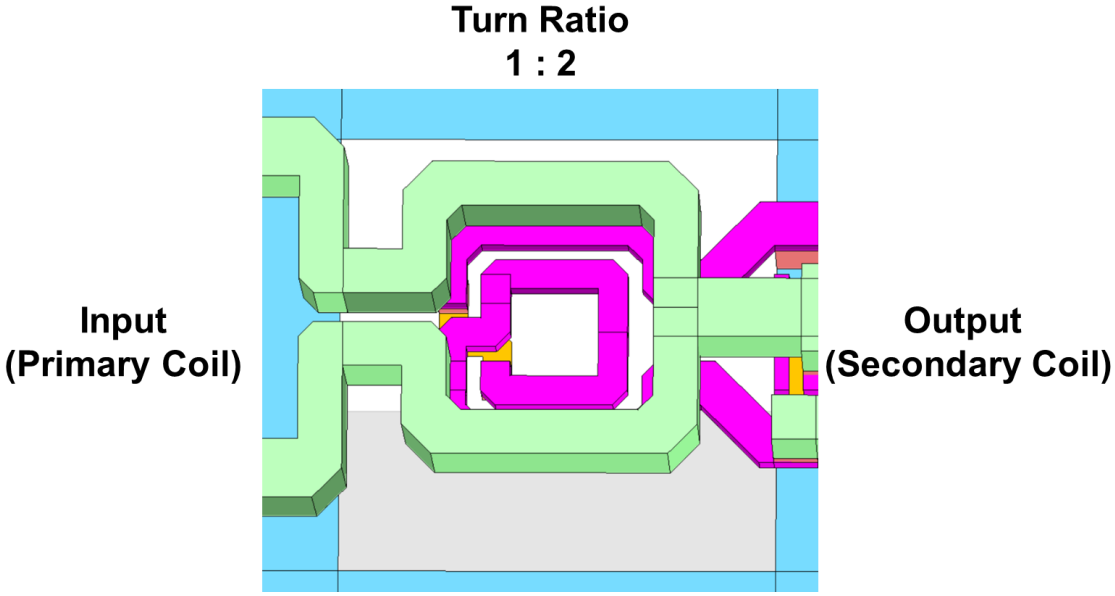

Fig. 4.13. 3-D rendering of the output transformer TF_{out} used for EM simulation.

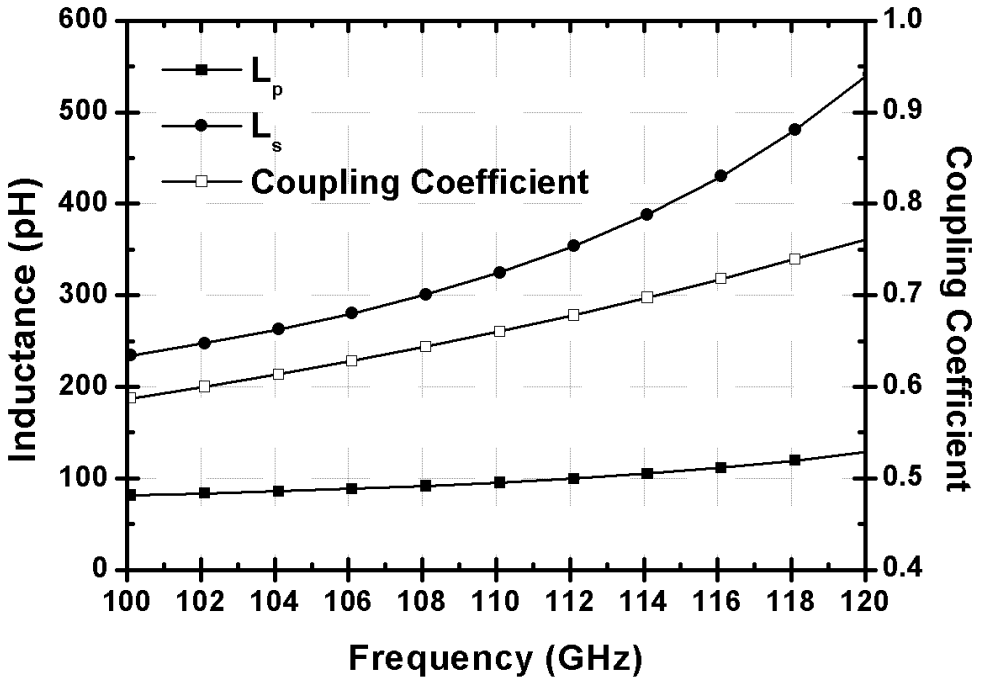

Fig. 4.14. Post-EM simulated parameters of the output transformer TF_{out}.

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Fig. 4.13 shows the 3-D rendering of the output transformer TF_{out} used for EM simulation. The transformer is realized using the metal-9 layer (top layer, 3.4-μm thick) for the primary coil, and metal-8 layer (0.9-μm thick) for the secondary coil in order to minimize the insertion loss. The ground plane (metal-1) underneath the transformer is removed to prevent undesired coupling of field. Fig. 4.14 shows the post-EM simulated parameters of TF_{out}. The 1:2 turn ratio enable an inductance ratio $r = L_s/L_p$ greater than 3 at 110 GHz. Together with a coupling coefficient of 0.66 at 110 GHz, the transformer design mitigates the low impedance ratio of the current-combining configuration. Since the center of the transformer primary coil is a virtual ground in differential mode, it also serves as bias-feeding point for drain voltage of the output stage devices ($V_{D,output}$). Center-tap shunt capacitors are adopted at the bias-feeding point to enforce the AC ground. This mitigates the phase and amplitude imbalances of the transformer, and suppresses any undesired common-mode signal. The adoption of center-tap capacitors are especially beneficial in inherently asymmetric transformer configurations such as differential-to-single or single-to-differential.

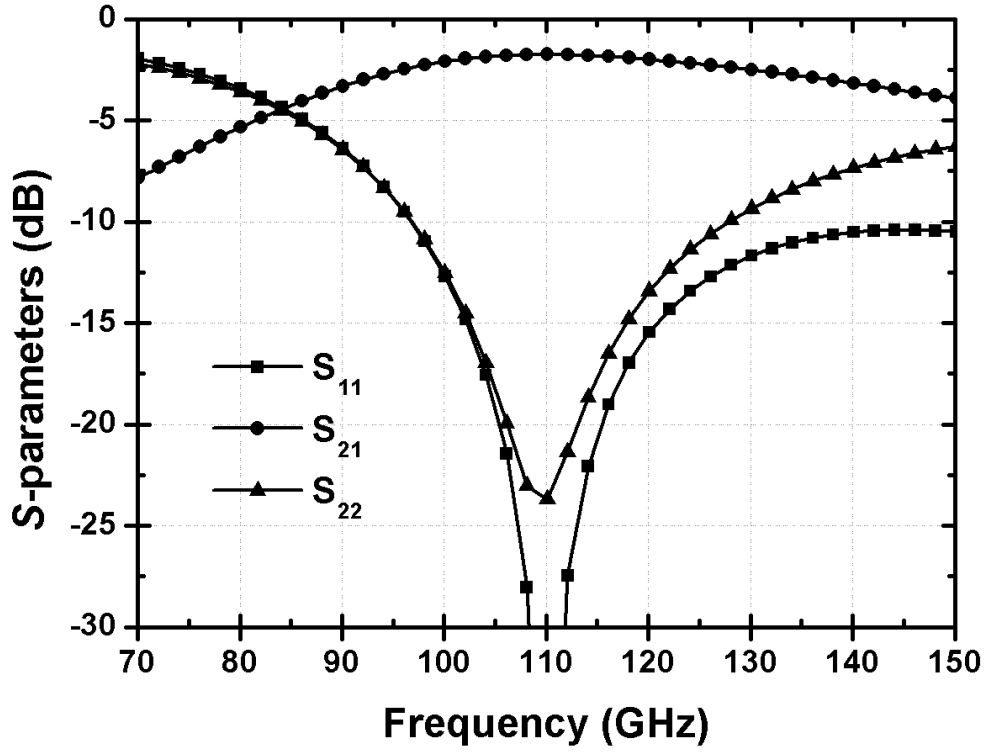

Fig. 4.15. Post-EM simulated *S*-parameters of the four-way transformer-based power combiner.

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Fig. 4.15 shows the post-EM simulated *S*-parameters of the four-way transformer-based power combiner. The combiner has insertion loss within 1.7 to 2 dB across 100 to 120-GHz, with the minimum loss of 1.7 dB at 110 GHz. In/output return loss larger than 10 dB indicates decent impedance matching across 100 to 120 GHz. Post-EM simulations of the output stage complete with the transformer-based power combiner are performed with ideal input conjugate termination. Fig. 4.16 and 4.17 shows the simulated *S*-parameters and large-signal performances at 110 GHz, respectively. The output stage has over 5 dB of gain across 90 to 120 GHz, with gain of 7.7 dB at 110 GHz and peak gain of 8 dB at 106 GHz. With P_{sat} of 15.4 dBm, PAE_{peak} of 14.8%, and OP_{1dB} of 12.8 dBm at 110 GHz, the output stage meets the target large-signal performance. Fig. 4.18 shows the simulated large-signal performances versus frequency. The output stage has P_{sat} above 14.9 dBm, PAE_{peak} above 13.2%, and OP_{1dB} above 12.8 dBm from 96 to 114 GHz. This indicates a wideband matching to the device optimal impedance provided by the transformer-based power combiner.

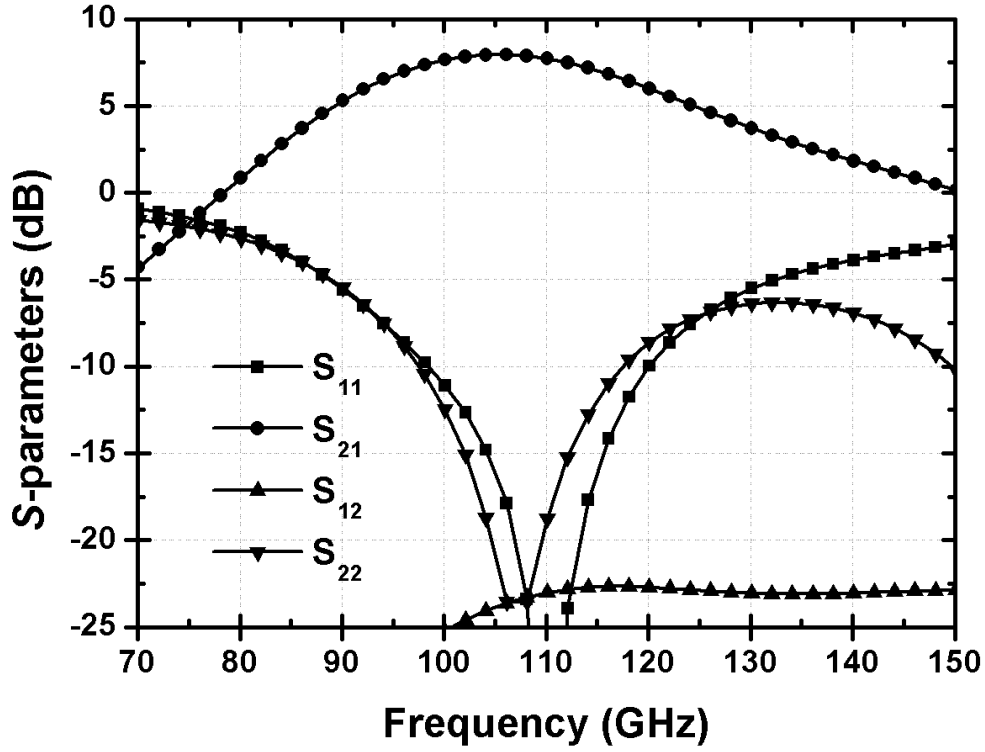

Fig. 4.16. Simulated *S*-parameters of the output stage complete with the four-way transformer-based power combiner.

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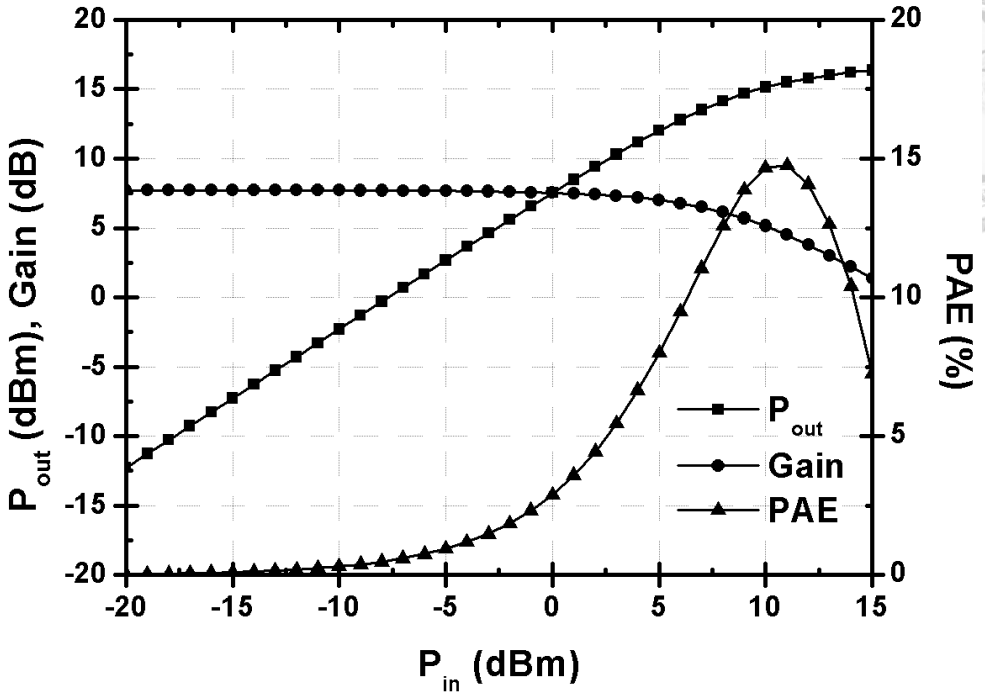

Fig. 4.17. Simulated large-signal performance at 110 GHz of the output stage complete with the four-way transformer-based power combiner.

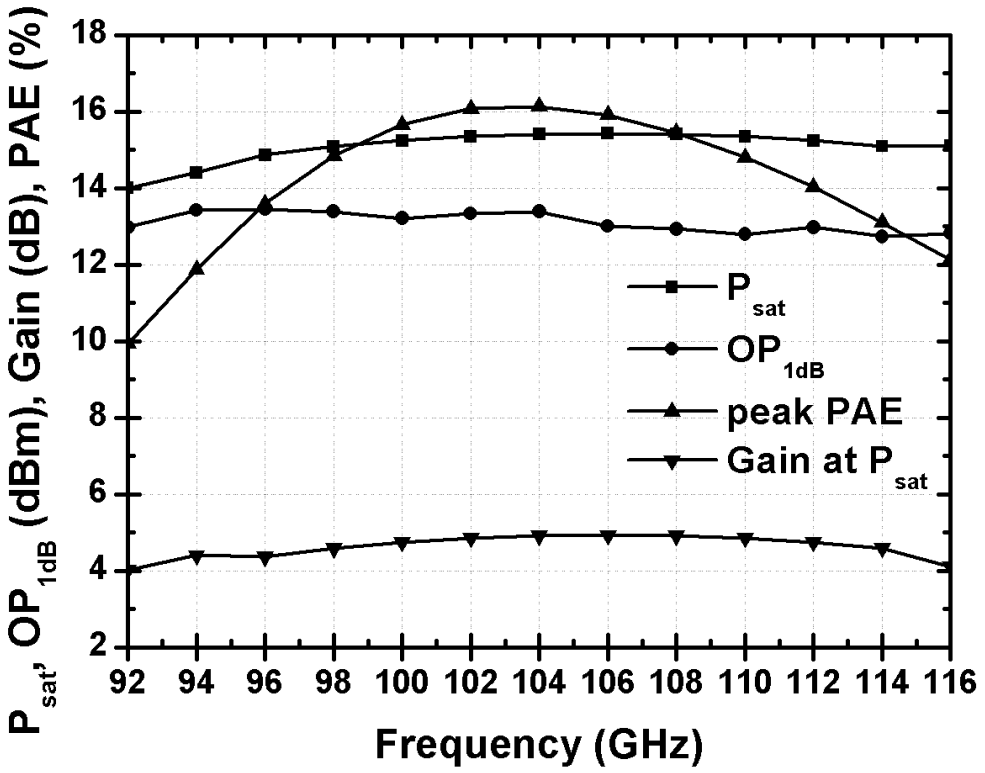

Fig. 4.18. Simulated large-signal performances versus frequency of the output stage complete with the four-way transformer-based power combiner.

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4.2.3 Second Driver Stage Design

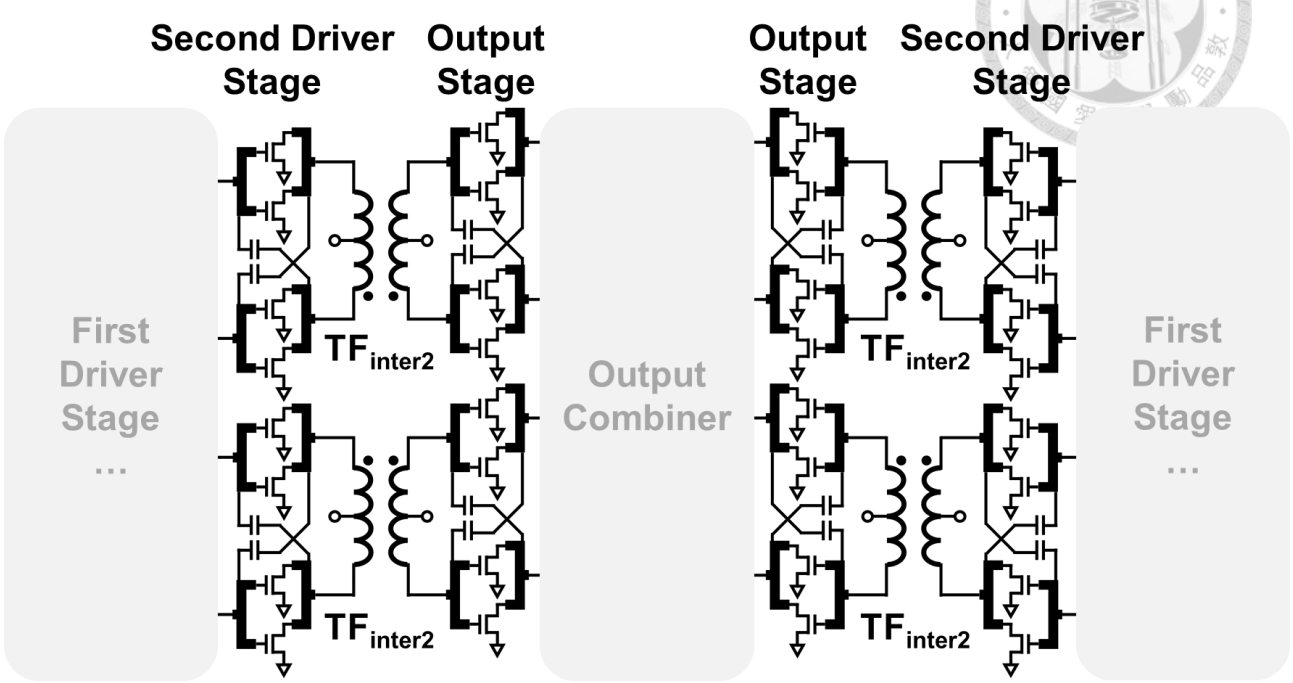

Fig. 4.19. Schematic of the second driver and output stages complete with the inter-stage matching network.

Fig. 4.19 shows the schematic of the second driver and output stages with the inter-stage matching network. For the second driver stage, the same differential pair configuration and bias condition of [V_{GS}, V_{DS}] = [0.8 V, 1.2 V] as in the output stage are used. Same number of four differential pairs are used for a one-to-one drive of the output stage. As mentioned above, simulation of the output stage shows an IP_{1dB} of 6.1 dBm and gain of 6.7 dB at the 1-dB compression point at 110 GHz. At around 110 GHz, a 2 dB insertion loss is estimated for the inter-stage matching network. Therefore, in order to maintain the overall large-signal performance, an $OP_{1dB} \geq 8.1$ dBm is required of the second driver stage. This means an $OP_{1dB} \geq 2.1$ dBm from each of the four differential pairs is required. Devices with gate-peripheries of 8f x 1 μm, i.e., half of the 16f x 1 μm output stage device, are used for the second driver stage. This result in a total gate-periphery ratio of 1:2 between the second driver and output stages.

Fig. 4.20 shows the simulated MSG/MAG and stability factor of the second driver stage differential pair at 110 GHz versus different values of C_N. C_N of 6 fF is chosen for the added

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stability and 3 dB of gain improvement at 110 GHz. EM simulations of the differential pair are also performed before design of the inter-stage matching network. Fig. 4.21 shows the post-EM simulated MSG/MAG and stability factor of the differential cell. By adopting the neutralization technique, increase in stability and the MSG/MAG at 110 GHz by 3 dB is achieved.

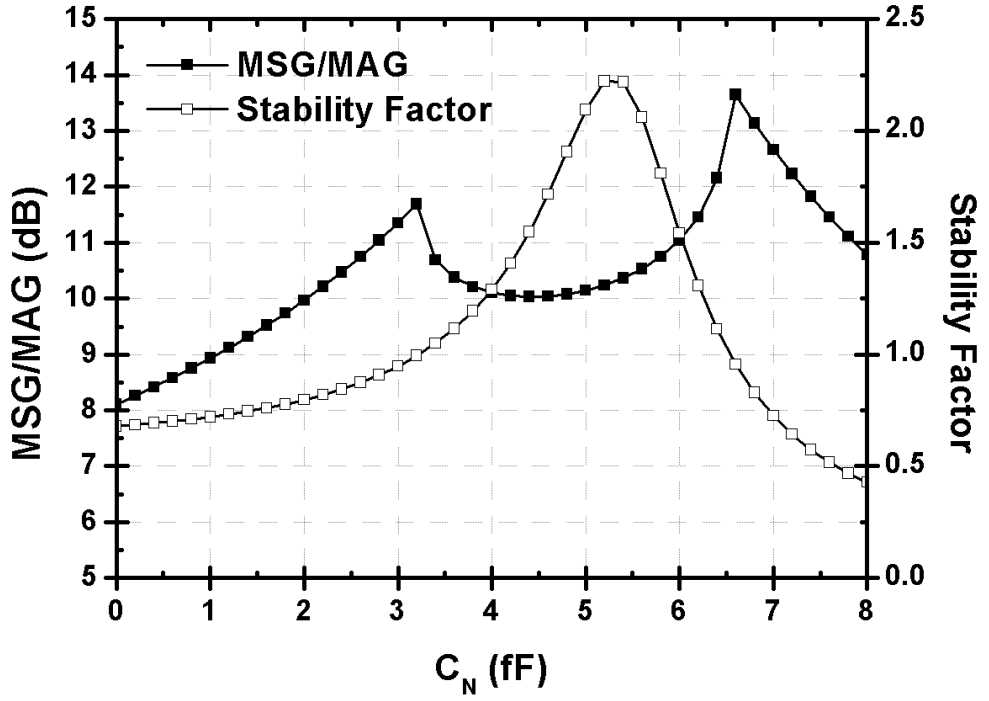

Fig. 4.20. Simulated MSG/MAG and stability factor of the second driver stage differential pair at 110 GHz versus different values of C_N.

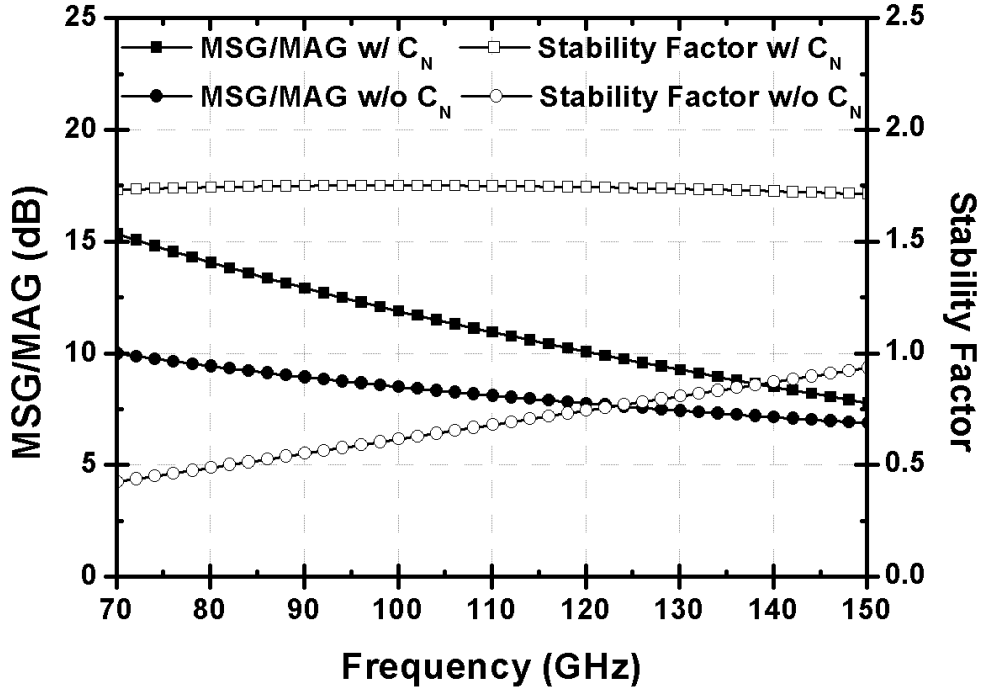

Fig. 4.21. Post-EM simulated MSG/MAG and stability factor of the second driver stage differential pair.

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Since the performance target is on OP_{1dB} for the second driver stage, load-pull simulations for OP_{1dB} performance is performed instead of for P_{sat}. Fig. 4.22 shows the power contours of the post-EM simulated differential pair. For a conservative design of the second driver stage, $Z_{opt2,diff}$ = 43.3 + j77.4 Ω is selected for the differential pair to achieve an OP_{1dB} of 4.9 dBm at 110-GHz. Therefore, the inter-stage impedance transfer results from the input impedance of the output stage differential pair $Z_{in3,diff}$ to $Z_{opt2,diff}$.

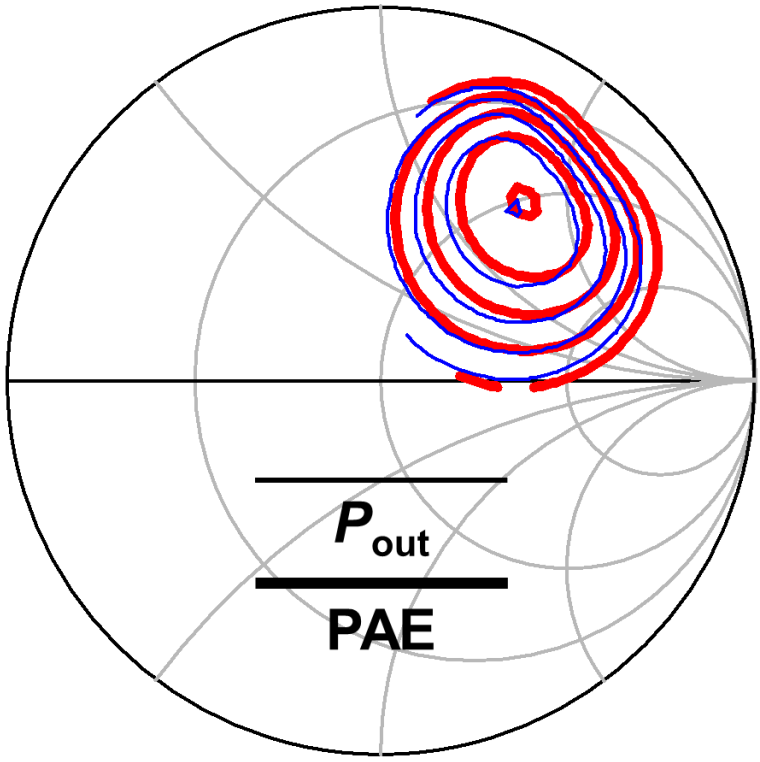

Fig. 4.22. Post-EM power contours of the second driver stage differential pair.

The inter-stage matching network is realized using differential-to-differential transformers. As in the output stage, the center of the transformer primary and secondary coils serve as bias-feeding points for $V_{D,driver2}$ and $V_{G,output}$, respectively. Center-tap capacitors are also adopted for improvements in differential transformer balance and suppressing undesired common-mode signals. Fig. 4.23 shows the 3-D rendering of the inter-stage transformer TF_{inter2} used for EM simulation. The impedance transfer from $Z_{in3,diff}$ to $Z_{opt2,diff}$ is achieved with a transformer of 1:1 turn ratio, which is realized using the metal-9 and -8 layers with the ground plane underneath removed. Fig.

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4.24 shows the post-EM simulated parameters of TF_{inter2}. The inductance ratio $r = L_s/L_p$ is slightly lower than 1 at 110-GHz, and the coupling coefficient is lower at 0.4 by design to achieve the desired inter-stage matching.

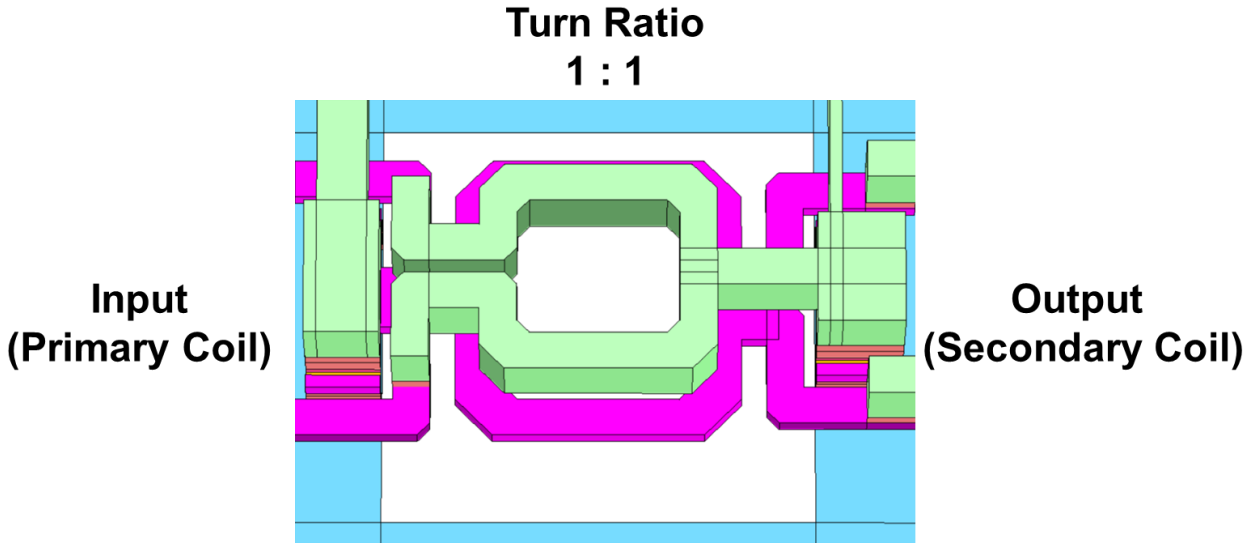

Fig. 4.23. 3-D rendering of the inter-stage transformer TF_{inter2} used for EM simulation.

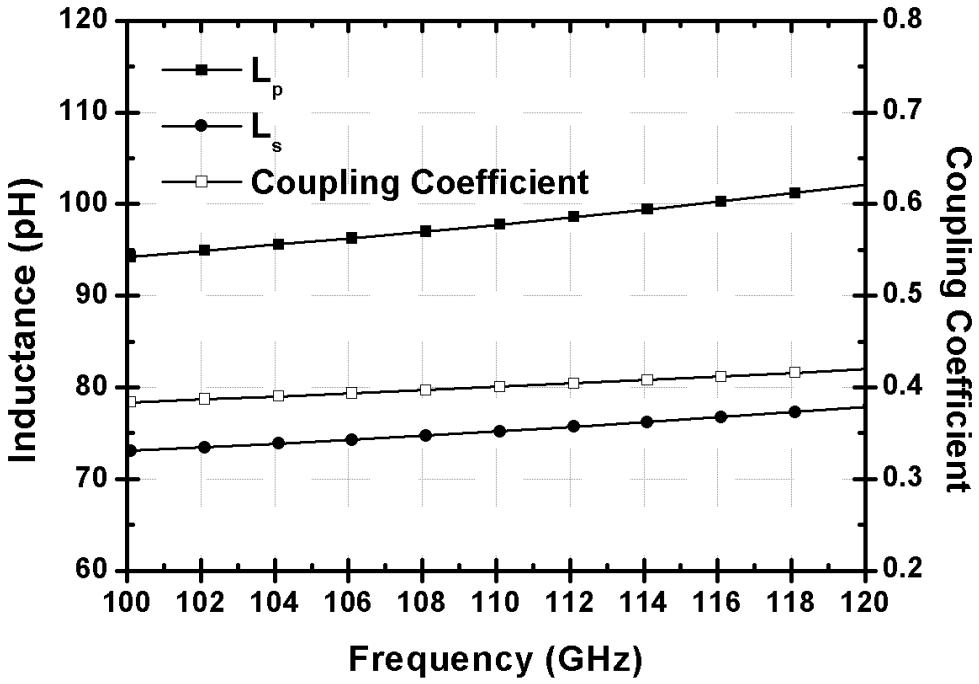

Fig. 4.24. Post-EM simulated parameters of the inter-stage transformer TF_{inter2}.

Post-EM simulation of cascading the second driver and output stages complete with inter-stage matching and output transformer-based power combiner is performed with ideal conjugate input termination. Fig. 4.25 and 3.26 shows the simulated *S*-parameters and large-signal performances at

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110 GHz, respectively. The second driver and output stages has over 10dB of gain across 92 to 120 GHz, with gain of 14.7 dB at 110 GHz and peak gain of 16.4 dB at 102 GHz. With P_{sat} of 15.7 dBm, PAE_{peak} of 12.2%, and OP_{1dB} of 11.9 dBm at 110 GHz, the second driver and output stages still meet the target large-signal performance. Fig. 4.27 shows the post-EM simulated large-signal performances versus frequency. As can be seen, the wideband large-signal performance of the output stage remains after the addition of second driver stage. The second driver and output stages has P_{sat} above 14.9 dBm, PAE_{peak} above 11.2%, and OP_{1dB} above 11.5 dBm across 96 to 114 GHz. Compared to the large-signal performance of the output stage, similar P_{sat} and OP_{1dB} performances indicates a successful drive of the output stage from the second driver stage. Only a slight peak PAE drop of around 2% across different frequencies also indicates a decent choice of device gate-periphery for the second driver stage.

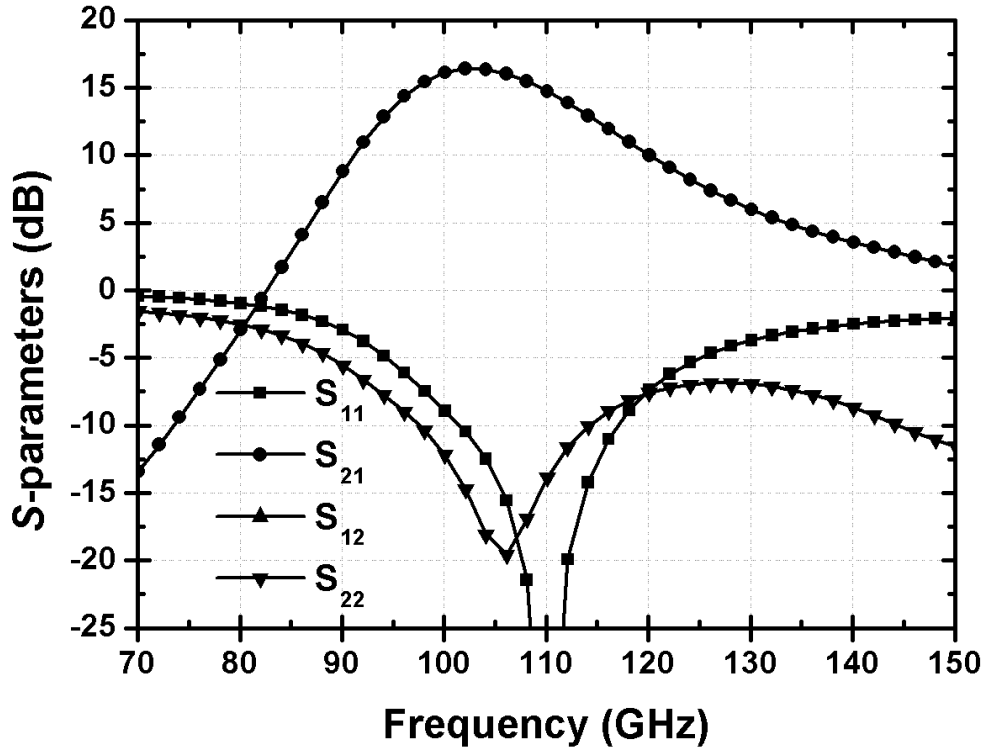

Fig. 4.25. Simulated *S*-parameters of the second driver and output stages complete with the inter-stage matching network and output transformer-based power combiner.

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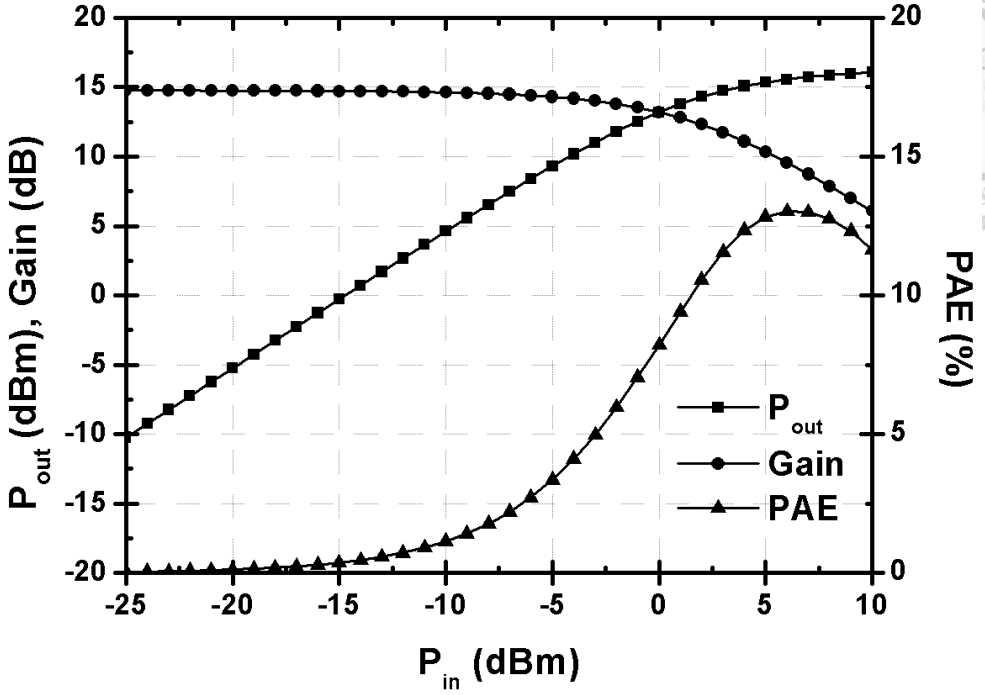

Fig. 4.26. Simulated large-signal performances at 110 GHz of the second driver and output stages complete with the inter-stage matching network and output transformer-based power combiner.

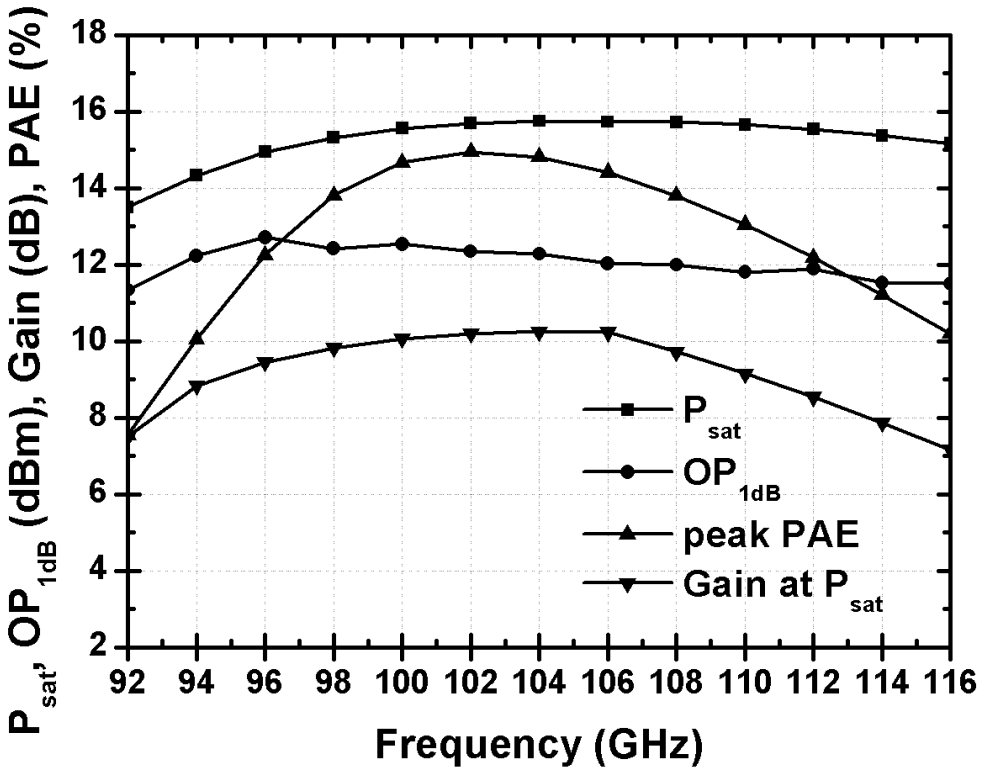

Fig. 4.27. Simulated large-signal performances versus frequency of the second driver and output stages complete with the inter-stage matching network and output transformer-based power combiner.

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4.2.4 First Driver Stage Design

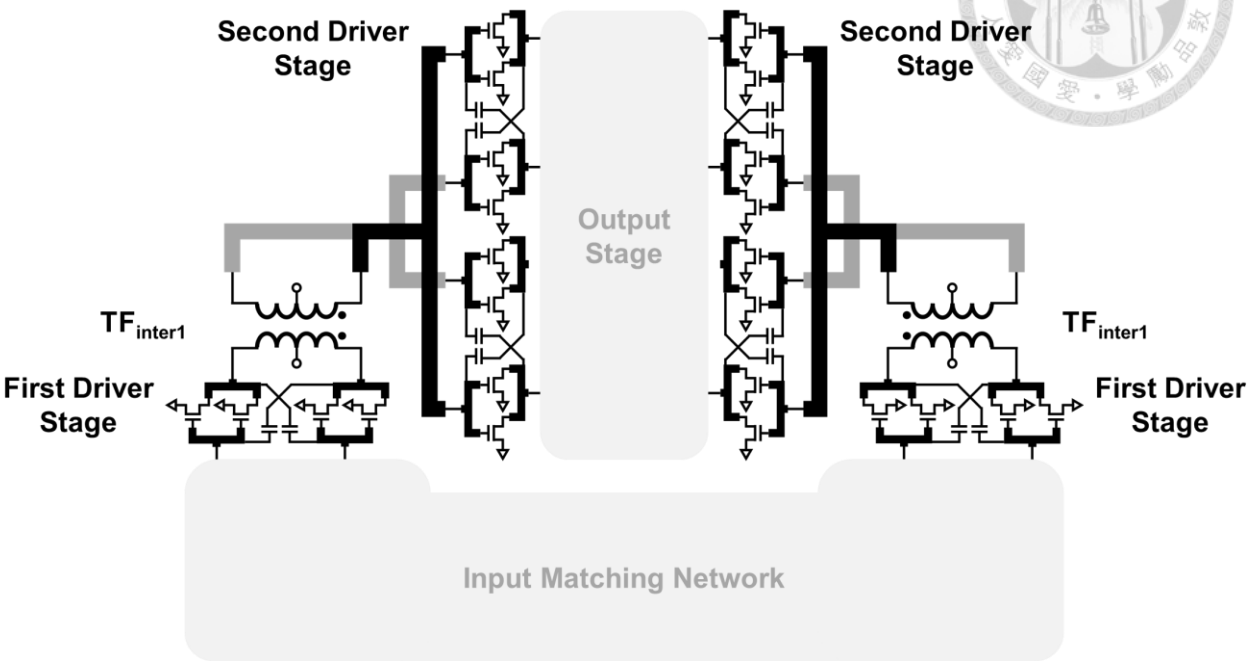

Fig. 4.28. Schematic of the first and second driver stages complete with the inter-stage matching network.

Fig. 4.28 shows the schematic of the first and second driver stages complete with the inter-stage matching network. For the first driver stage, the same differential pair configuration and bias condition of [V_{GS}, V_{DS}] = [0.8 V, 1.2 V] as in the latter stages is used. Two differential pairs are used for a one-to-two drive of the second driver stage. The same differential pair configuration with four 8f x 1μm device gate-peripheries as the second driver stage is used. This result in a total gate-periphery ratio of 1:2:4 between the first, second driver and output stages. To enable the halving of differential pair numbers from 4 to 2, input nodes of the second driver stage with the same polarity in differential mode are combined together through 50-Ω micro-strip lines. Micro-strip lines are carefully designed during physical layout to have equal lengths, ensuring that no additional phase difference between paths is introduced.

The inter-stage matching is designed for maximum gain performance, i.e., conjugate matching. Since the number of differential cell is halved, the matching involves impedance transfer from half of the input impedance of the second driver differential pair, i.e., 0.5 x $Z_{in2,diff}$, to the conjugate

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output impedance of the first driver differential pair $Z_{out1,diff}^{*}$.

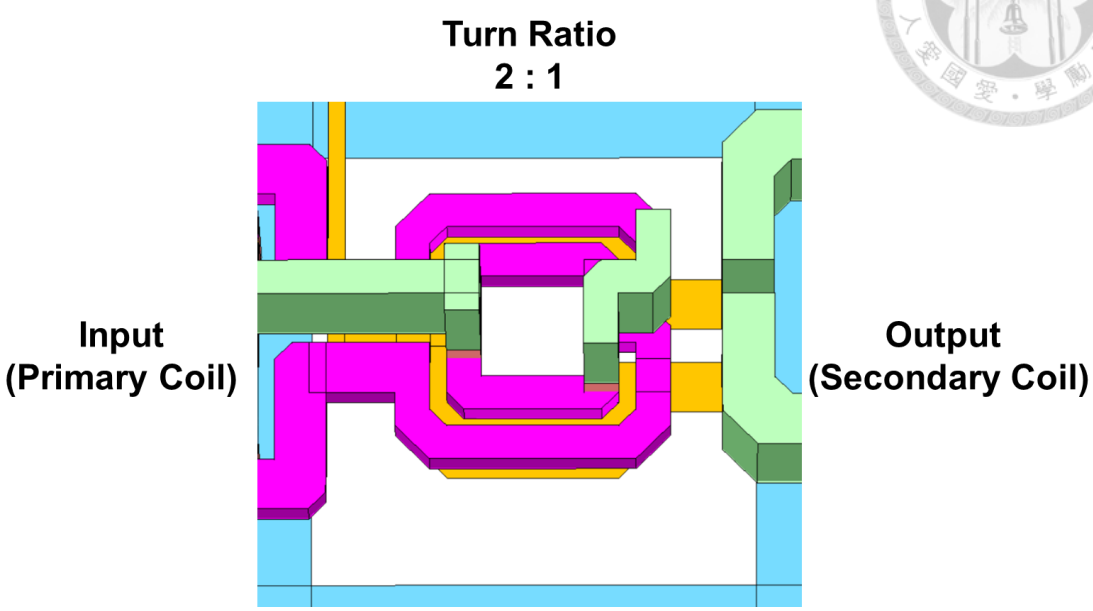

Fig. 4.29. 3-D rendering of the inter-stage transformer TF_{inter1} used for EM simulation.

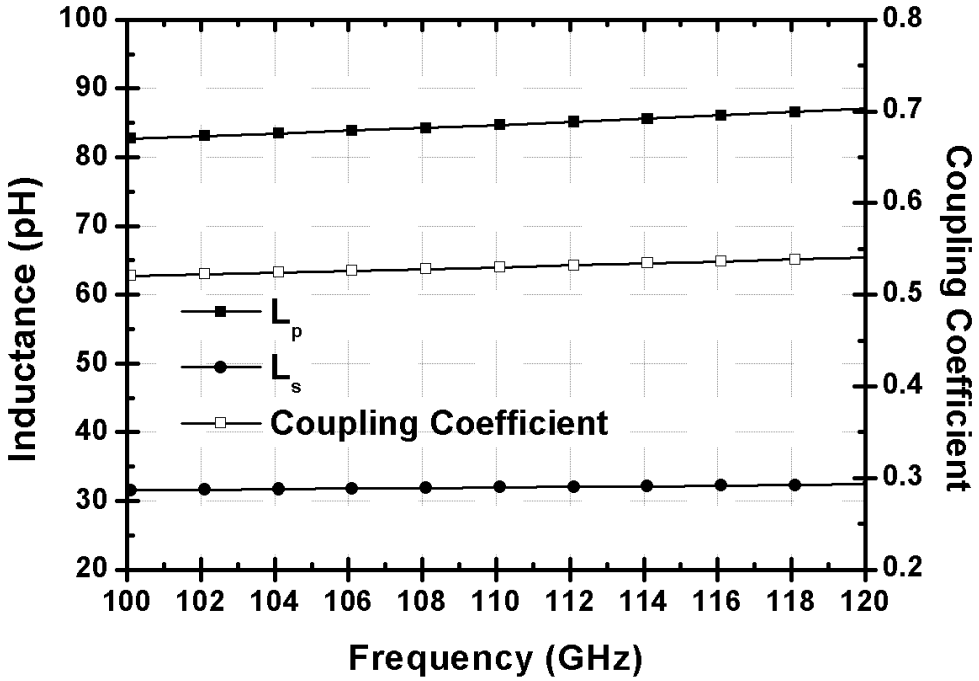

Fig. 4.30. Post-EM simulated parameters of the inter-stage transformer TF_{inter1}.

The inter-stage matching network is realized using differential-to-differential transformers. As in the latter stages, the center of the transformer primary and secondary coils serve as bias-feeding points for $V_{D,driver1}$ and $V_{G,driver2}$, respectively. Center-tap capacitors are also adopted for improvements in differential transformer balance, and suppressing undesired common-mode signals.

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Fig. 4.29 shows the 3-D rendering of the transformer TF_{inter1} used for EM simulation. The impedance transfer from 0.5 x $Z_{in2,diff}$ to $Z_{out1,diff}^{*}$ requires transformers with 2:1 turn ratio. The transformer with 2:1 turn ratio is realized using the metal-8 and metal-7 layers with the ground plane underneath removed. Fig. 4.30 shows the post-EM simulated parameters of TF_{inter1}. The 2:1 turn ratio enable an inductance ratio $r = L_s/L_p$ less than 0.5 at 110 GHz, meeting the requirement of matching 0.5 x $Z_{in2,diff}$ to $Z_{out1,diff}^{*}$.

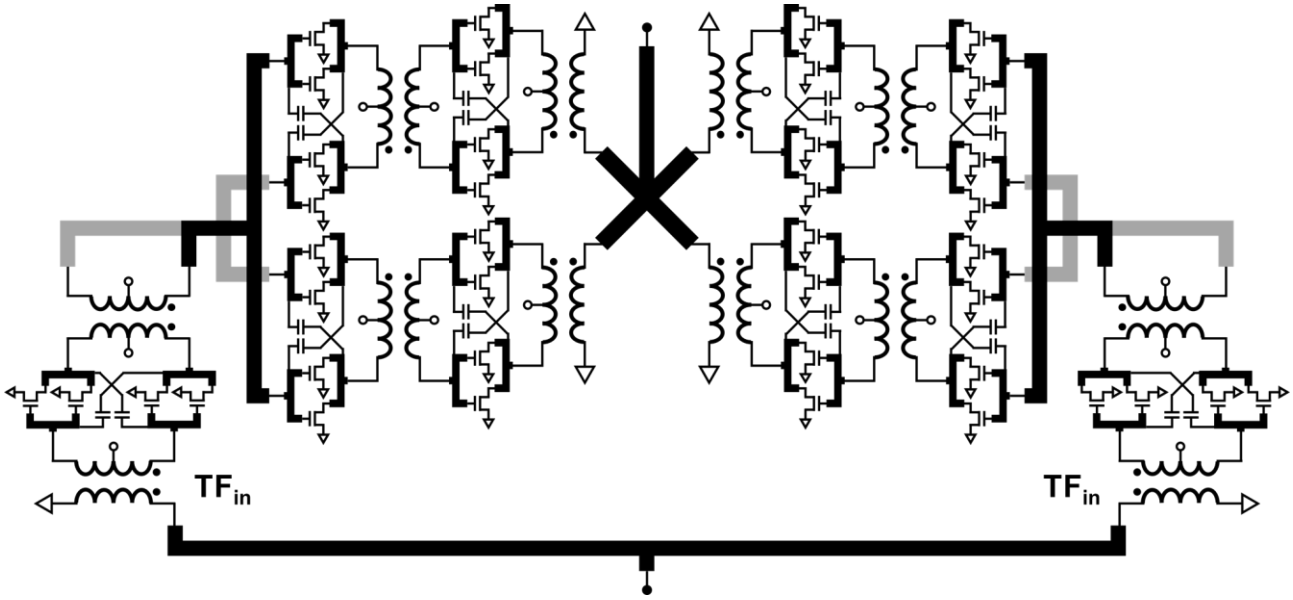

Fig. 4.31. Schematic of the proposed W-band PA.

Fig. 4.31 shows the complete circuit schematic of the proposed W-band PA. Similar to the output transformer-based power combiner, the input transformer-based matching network doubles as a power splitter between the two first driver stage differential pairs. Single-to-differential transformers are used between the single-ended input and the differential pairs. A short 50-Ω micro-strip line from the input before two symmetrical 50-Ω micro-strip lines are used for in-phase power splitting into the two single-to-differential transformers. Therefore, the source impedance at the input, i.e., Z_S = 50 Ω, transfers to a 2 x 50 Ω impedance seen by the transformers looking towards the input. To transfer 100 Ω to the conjugate input impedance of the differential cell $Z_{in1,diff}^{*}$ with the lower impedance transformation ratio of the current-combining (-splitting) configuration,

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transformers with 1:2 turn ratios and high coupling coefficients are required.

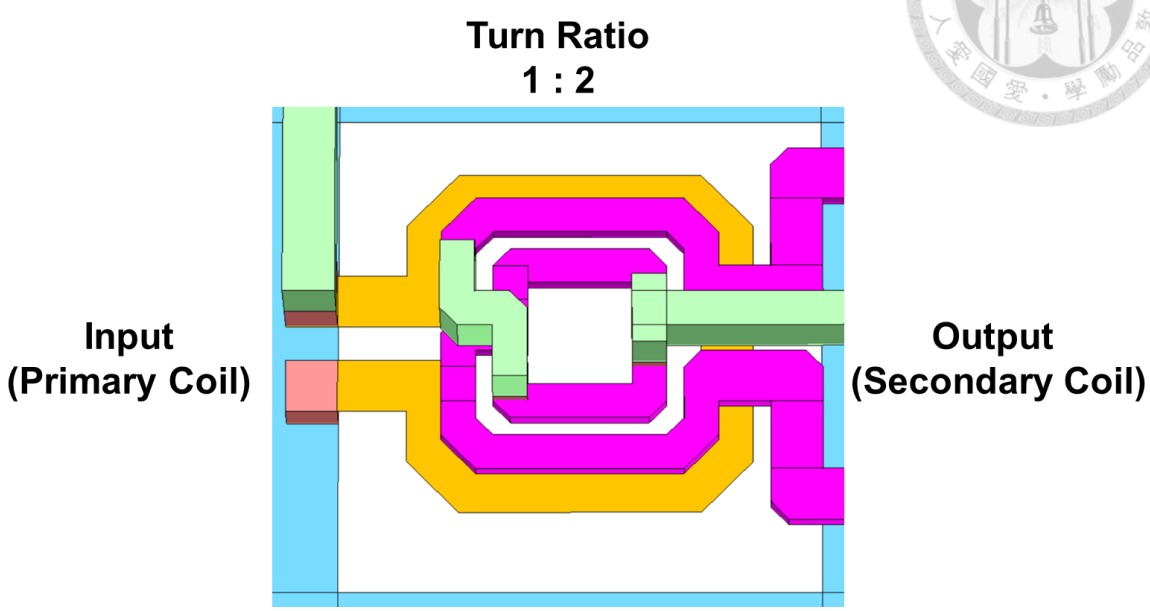

Fig. 4.32. 3-D rendering of the input transformer TF_{in} used for EM simulation.

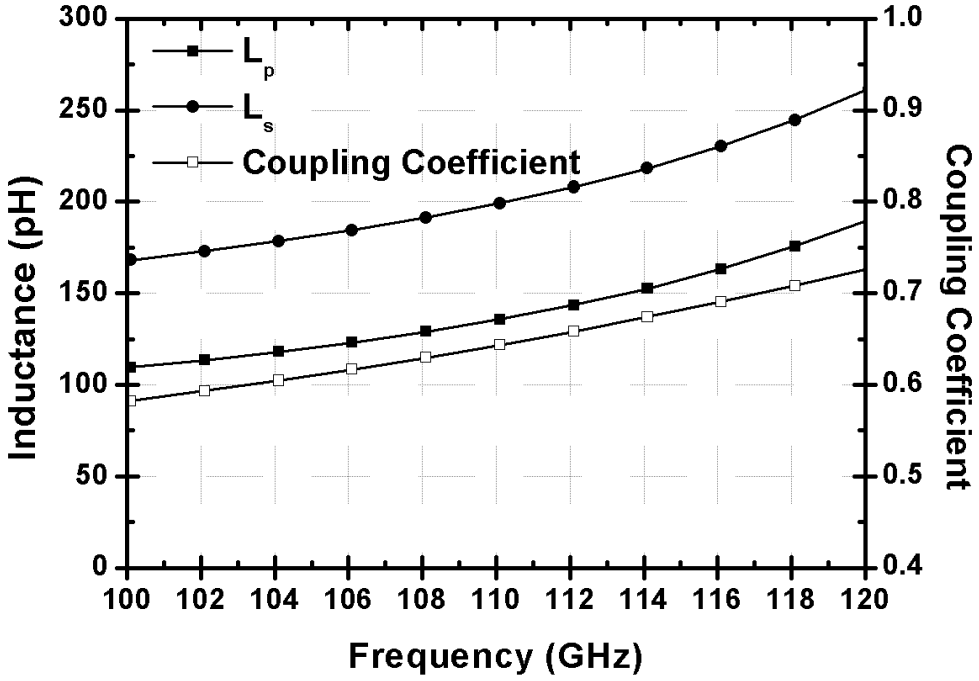

Fig. 4.33. Post-EM simulated parameters of the input transformer TF_{in}.

Fig. 4.32 shows the 3-D rendering of the transformer TF_{in} used for EM simulation. The transformer with 1:2 turn ratio is realized using the metal-8 and metal-7 layers with the ground plane underneath removed. Center of the transformer secondary coil serves as bias-feeding point for $V_{G,driver1}$. Center-tap capacitors are also adopted at the secondary coils for improvements in

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differential transformer balance, and suppressing undesired common-mode signals. Fig. 4.33 shows the post-EM simulated parameters of TF_{in}. The 1:2 turn ratio enable an inductance ratio $r = L_s/L_p$ greater than 1.5 at 110 GHz. Together with a coupling coefficient of 0.64 at 110 GHz, the transformer design mitigates the low impedance ratio of the current-combining (-splitting) configuration.

4.2.5 Simulation Results

Fig. 4.34 shows the post-EM simulated *S*-parameters of the proposed W-band PA. The PA has a 20 GHz 30-dB bandwidth with peak gain of 16.4 dB at 102 GHz, and gain of 14.4 dB at 110 GHz. The input return loss is above 10 dB from 108 to 126 GHz, and output return loss is above 10 dB from 98 to 114 GHz.

Fig. 4.35 to 4.39 shows the post-EM simulated large-signal performances of the proposed W-band PA from 104 to 116 GHz. The PA shows an OP_{1dB} of 11.3 dBm, P_{sat} of 15.0 dBm, and peak PAE of 9.65% at 110 GHz, which meet the targeted P_{sat} of 15 dBm. The P_{sat} and OP_{1dB} of the PA remain close to those of the output stage, indicating a decent design of the driver stages. The PAE of the PA inevitably drops slightly as compared with the output stage, mostly due to loss of the input and inter-stage matching networks. Fig. 4.40 shows the post-EM simulated large-signal performances versus frequency. From 94 to 114 GHz, the PA shows OP_{1dB} above 10.3 dBm, P_{sat} above 14.0 dBm, and peak PAE above 7.0%. Furthermore, P_{sat} performance is above 13.0 dBm across 92 to 116 GHz. The wideband large-signal performance of the output stage remains after the addition of the driver stages.

Fig. 4.41 shows the post-EM simulated drain currents (I_{DS}) of the three stages and power consumption of the PA (P_{DC}) versus P_{in}, in which $P_{DC} = V_{DD} \times I_{DS} = 1.2V \times (I_{DS1} + I_{DS2} + I_{DS3})$. The drain currents of the first driver, second driver, and output stages are around 35mA, 70mA, and 136mA across different P_{in} levels, respectively. The simulated drain currents are consistent with the 1:2:4 gate-periphery ratio between the three stages. P_{DC} is 288 mW at low P_{in} levels, and drops to

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around 280 mW approaching P_{sat} and PAE_{peak}. Fig. 4.42 shows the post-EM simulated stability factor of the PA. Stability factor above 1 across the frequencies indicates a stable design.

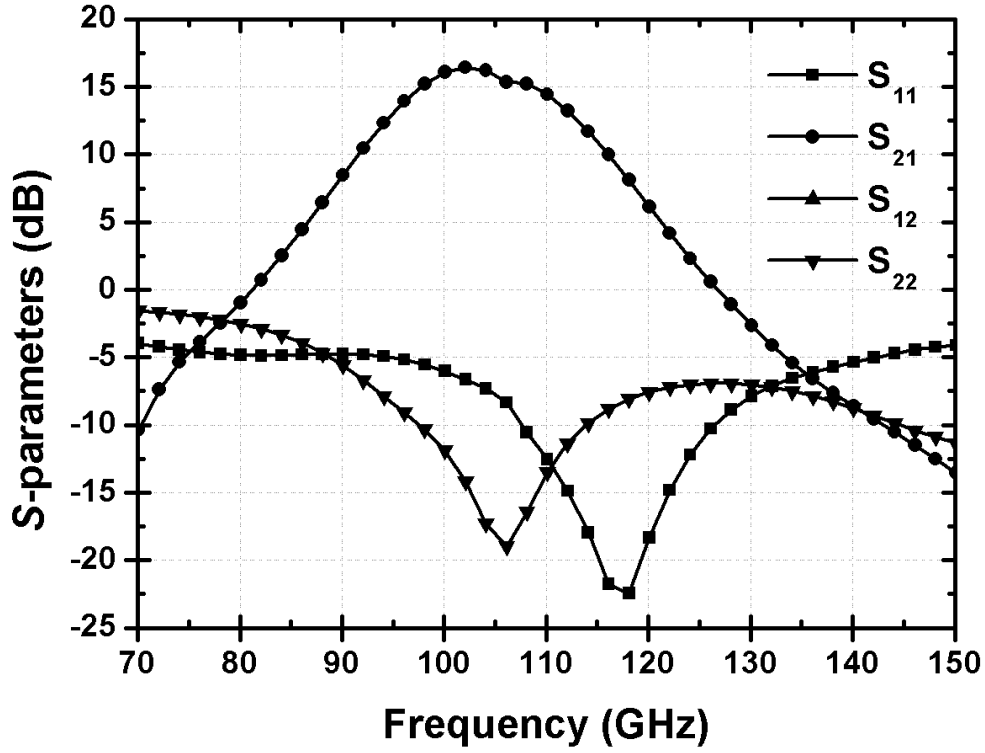

Fig. 4.34. Simulated *S*-parameters of the proposed W-band PA.

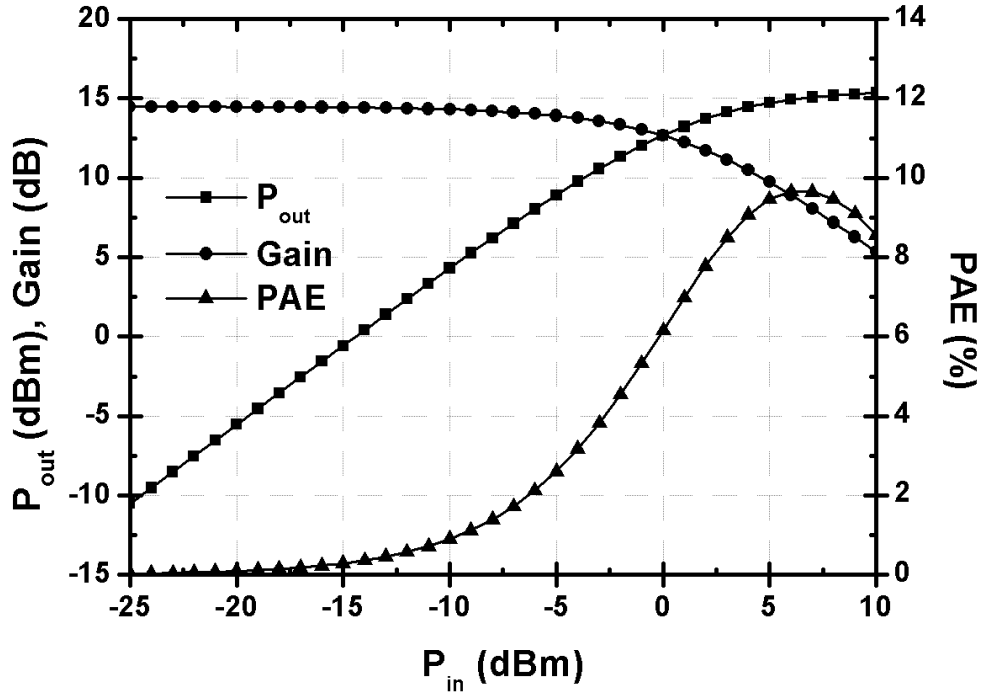

Fig. 4.35. Simulated large-signal performance at 110 GHz of the proposed W-band PA.

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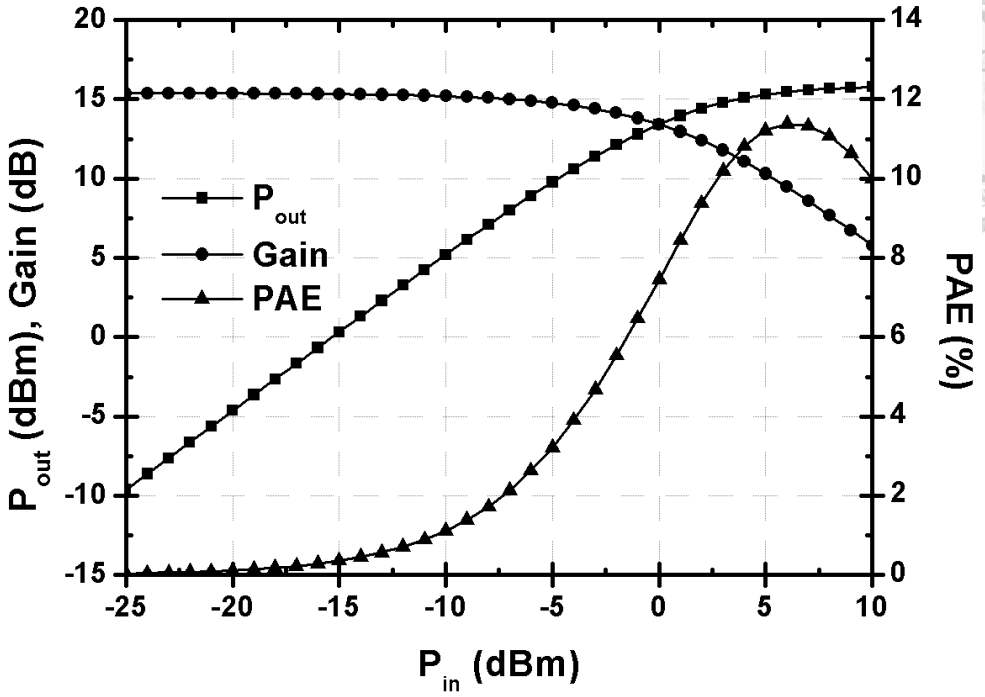

Fig. 4.36. Simulated large-signal performance at 106 GHz of the proposed W-band PA.

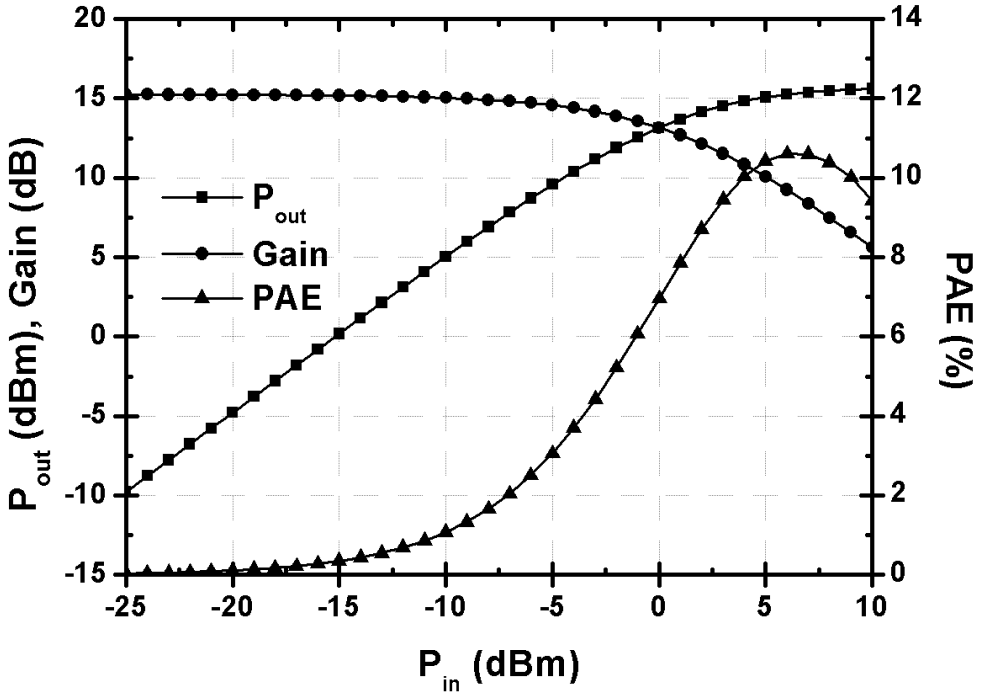

Fig. 4.37. Simulated large-signal performance at 108 GHz of the proposed W-band PA.

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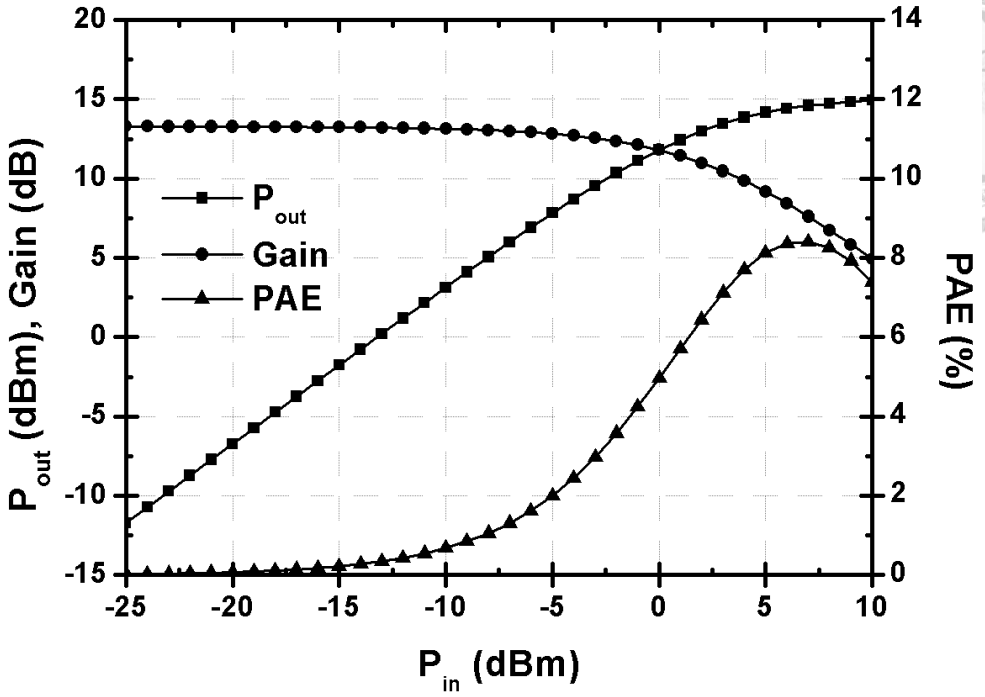

Fig. 4.38. Simulated large-signal performance at 112 GHz of the proposed W-band PA.

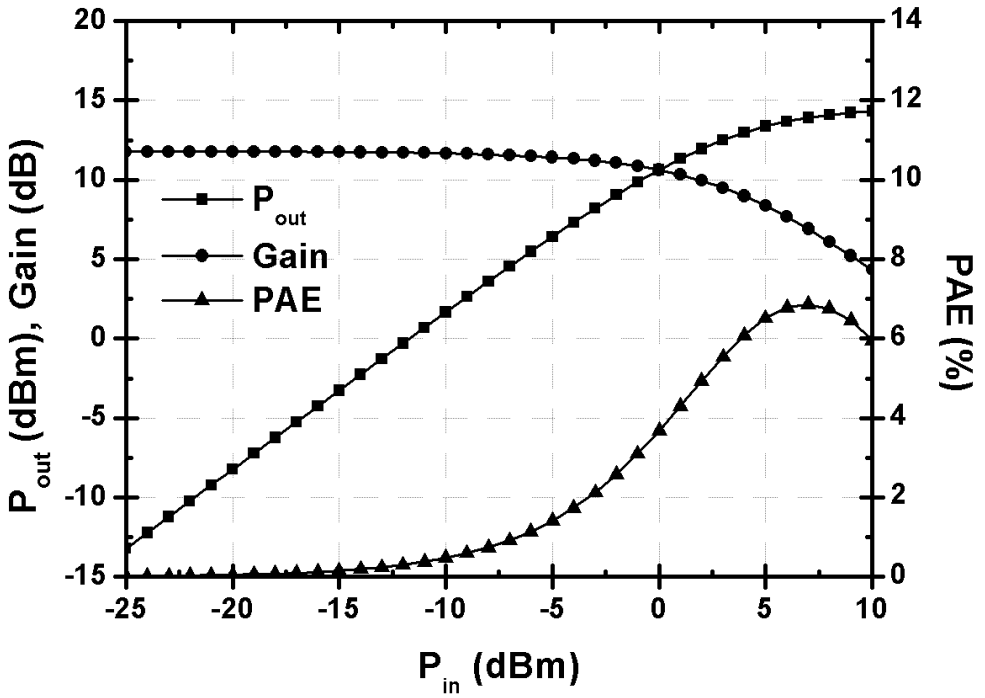

Fig. 4.39. Simulated large-signal performance at 114 GHz of the proposed W-band PA.

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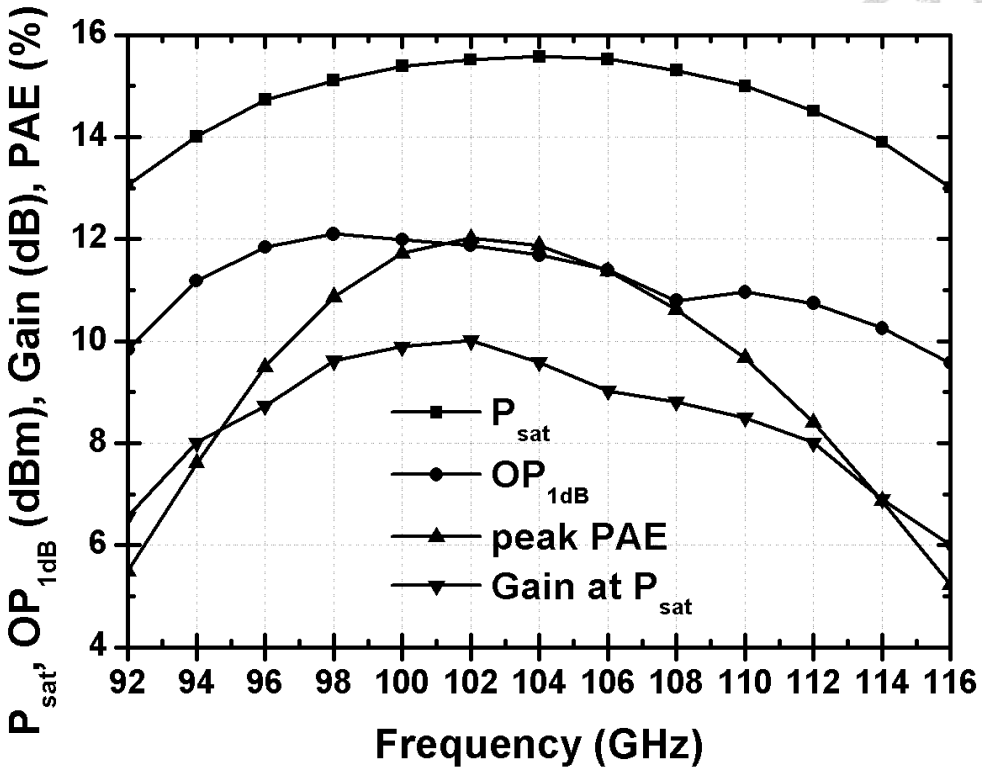

Fig. 4.40. Simulated large-signal performances versus frequency of the proposed W-band PA.

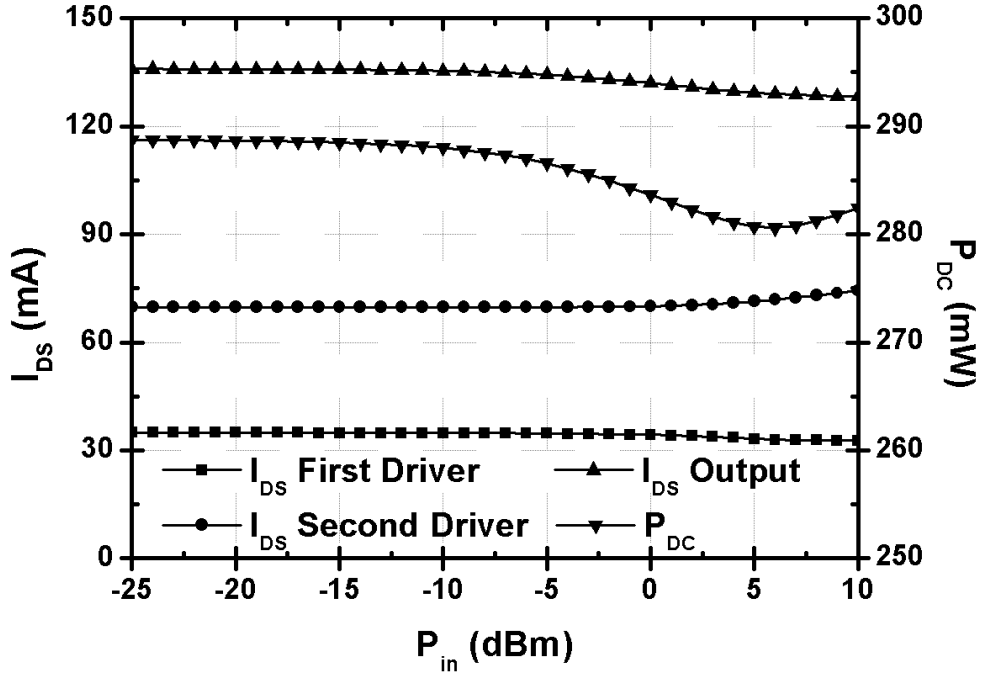

Fig. 4.41. Simulated I_{DS} of each stage versus P_{in} at 110 GHz of the proposed W-band PA.

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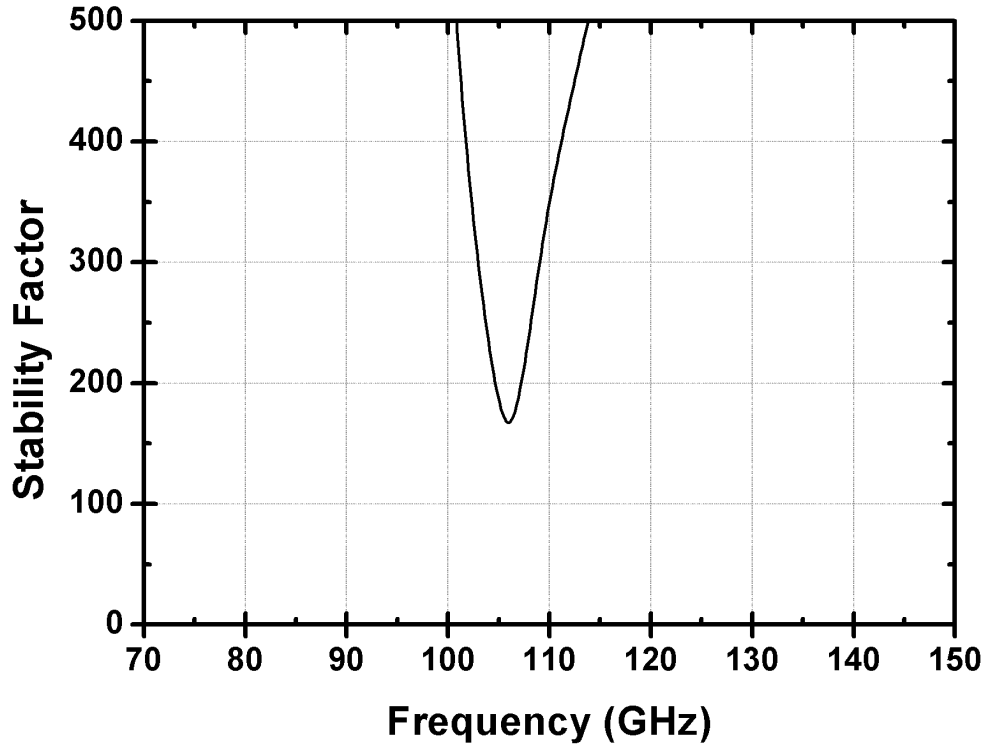

Fig. 4.42. Simulated stability factor of the proposed W-band PA.

4.3 Experimental Results

The proposed W-band PA design was fabricated in 65-nm CMOS process by TSMC. Fig. 4.43 shows the chip layout, in which ground and dummy cells are not shown for clarity. The die size measures at 910 x 460 μm^2 with RF and DC pads included. All measurements were performed via on-wafer probing. Dice were mounted on PCB boards with bond-wiring for bias applications. Off-chip bypass networks were designed and implemented on the PCB boards.

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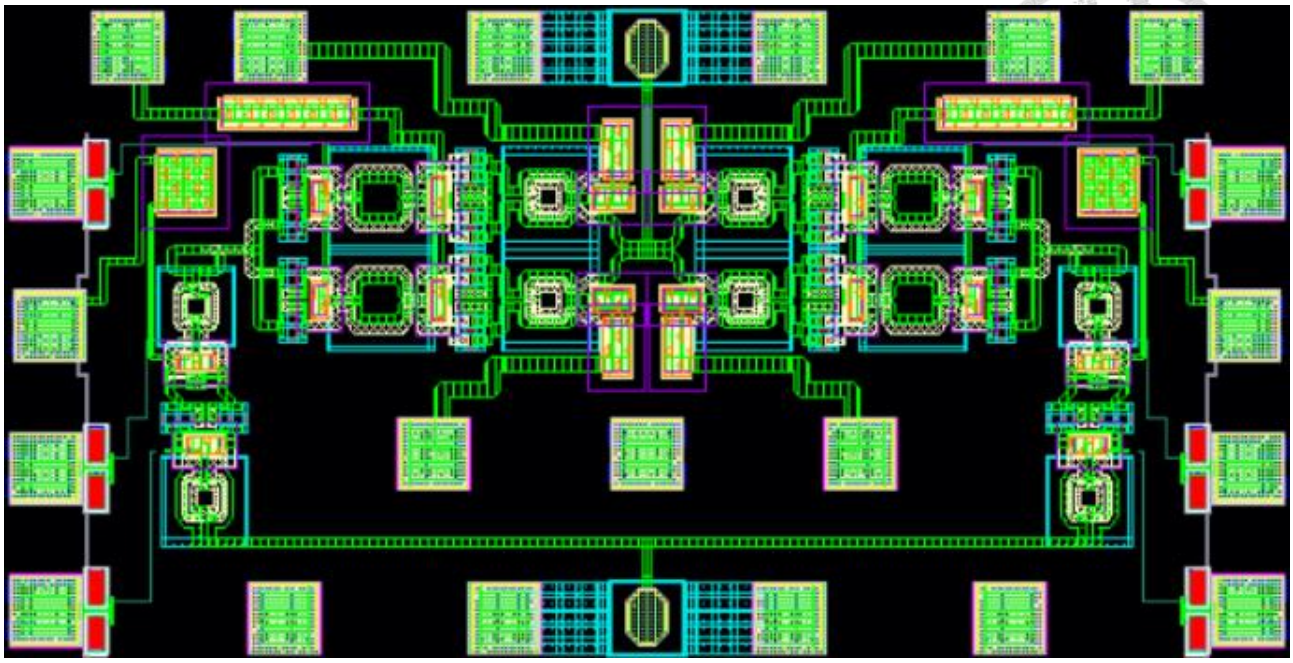

Fig. 4.43. Chip layout of the proposed W-band PA.

Table 4.1. Bias conditions during small-signal measurements.

	V_{GS} (V)		V_{DS} (V)	I_{DS} (mA)	
	Sim.	Meas.		Sim.	Meas.
1st driver stage	0.8	0.8	2.0	35	35
2nd driver stage	0.8	0.8	2.0	70	69
Output stage	0.8	0.8	2.0	136	151

An Agilent 8510C vector network analyzer was used for small-signal measurements up to 110 GHz. Table 4.1 shows the bias conditions during small-signal measurements. Measured I_{DS}'s of the first and second driver stages are consistent with simulation while measured I_{DS} of the output stage is around 10% larger than simulation, as will be discussed later in section 4.4. Fig. 4.44 shows the measured *S*-parameters of the proposed W-band PA. The measured S_{11} agrees well with simulation. However, both the measured S_{21} and S_{22} show a shift towards lower frequencies compared to simulation. The measurement shows a 12 GHz 3-dB bandwidth with peak gain of 11.2 dB at 96.5 GHz, compared to a 20 GHz 3-dB bandwidth with peak gain of 16.4 dB at 102 GHz in simulation. Measured gain at 110 GHz is only 2.3 dB, compared to a 14.4 dB in simulation.

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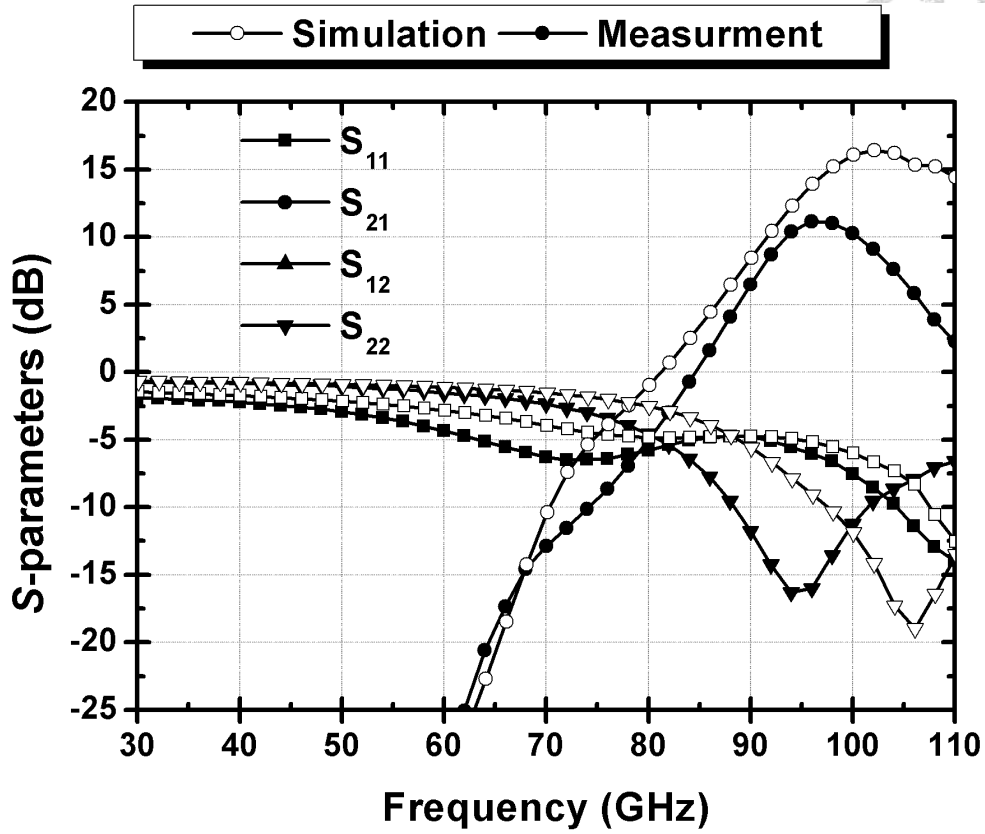

Fig. 4.44. Measured and simulated *S*-parameters of the proposed W-band PA.

Since the center frequency in terms of peak gain has shifted to 96 GHz from the small-signal measurement results, the large-signal measurement is performed at around 96 GHz instead of 110 GHz. Fig. 4.45 to 4.49 show the measured large-signal performances from 92 to 100 GHz. As can be seen, the measured large-signal performances at different frequencies all show rising gain up to certain P_{in} levels, before returning to typical class-A behavior, as will be discussed in section 4.4. Note that due to the output power limit of the measurement equipment, the P_{in} levels were only able to reach approximately to P_{sat} and PAE_{peak} at some frequencies. Despite the rising gain phenomena, approximated P_{sat} and PAE_{peak} from the measurement results still show disagreement and degradation compared with the simulation.

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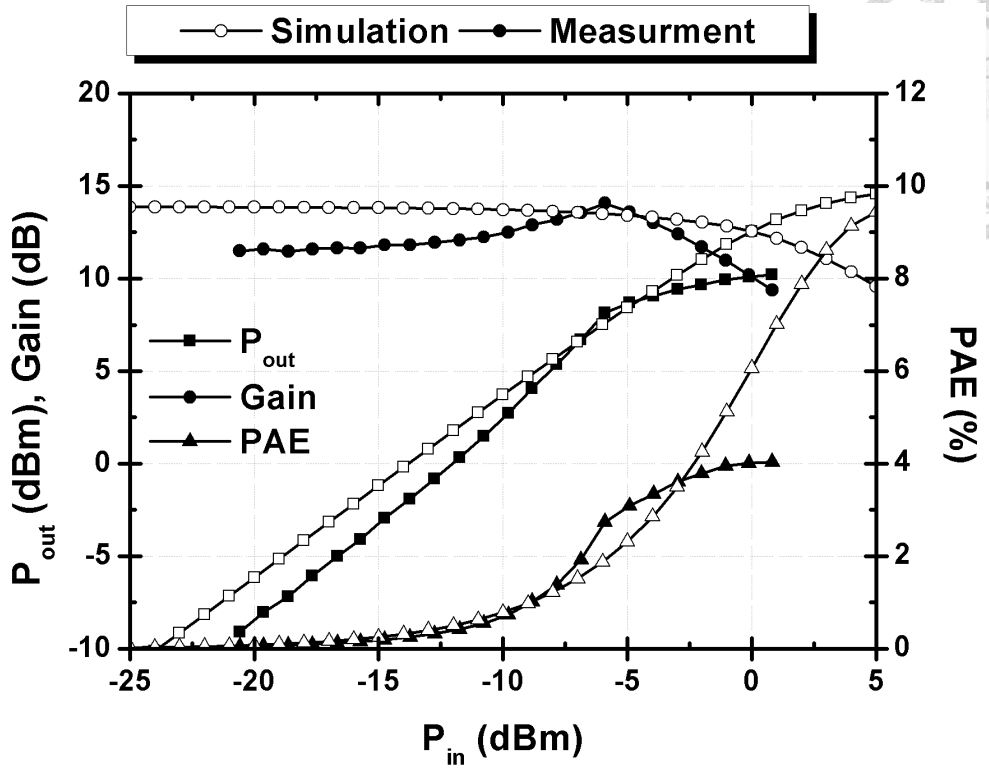

Fig. 4.45. Measured and simulated large-signal performance of the proposed W-band PA at 96 GHz.

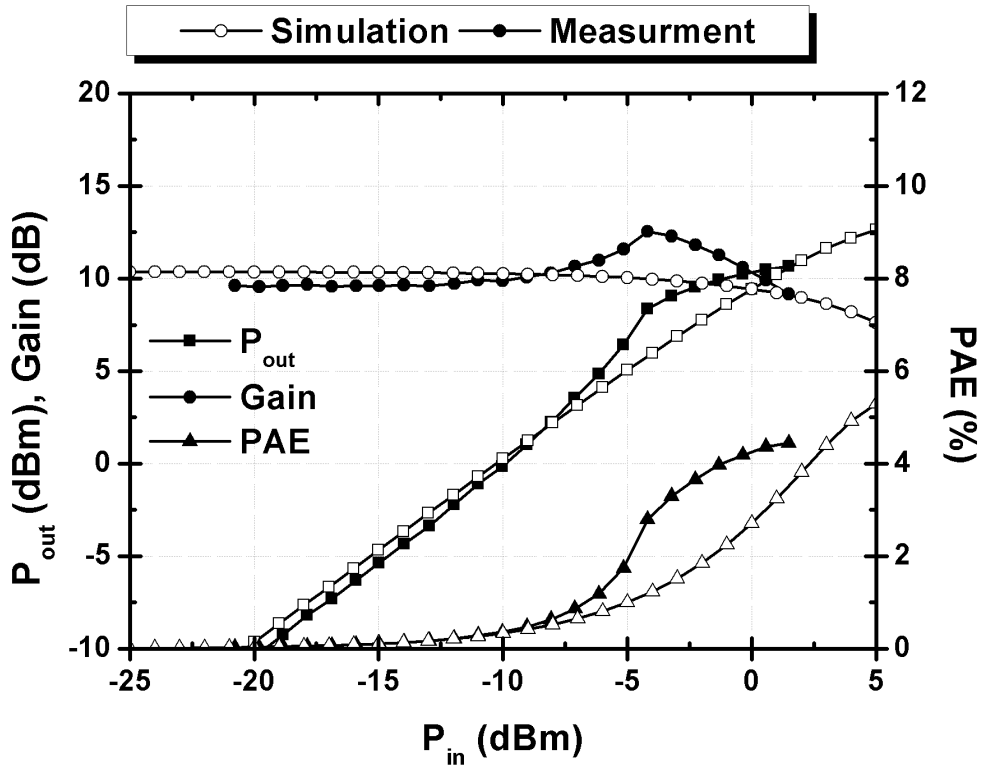

Fig. 4.46. Measured and simulated large-signal performance of the proposed W-band PA at 92 GHz.

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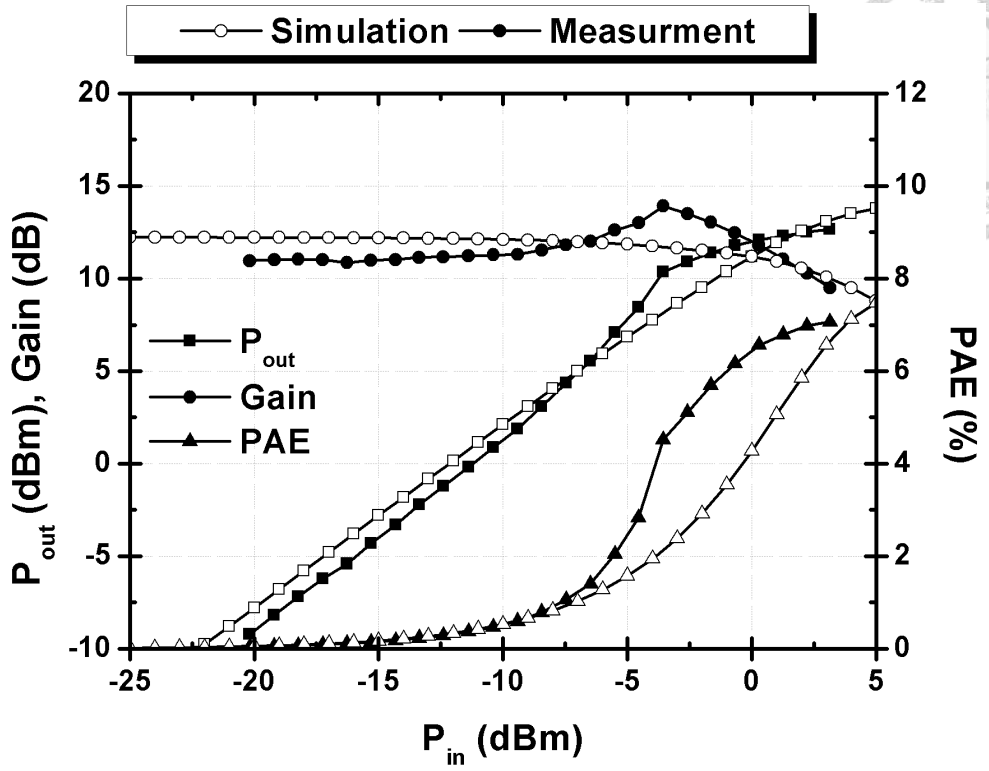

Fig. 4.47. Measured and simulated large-signal performance of the proposed W-band PA at 94 GHz.

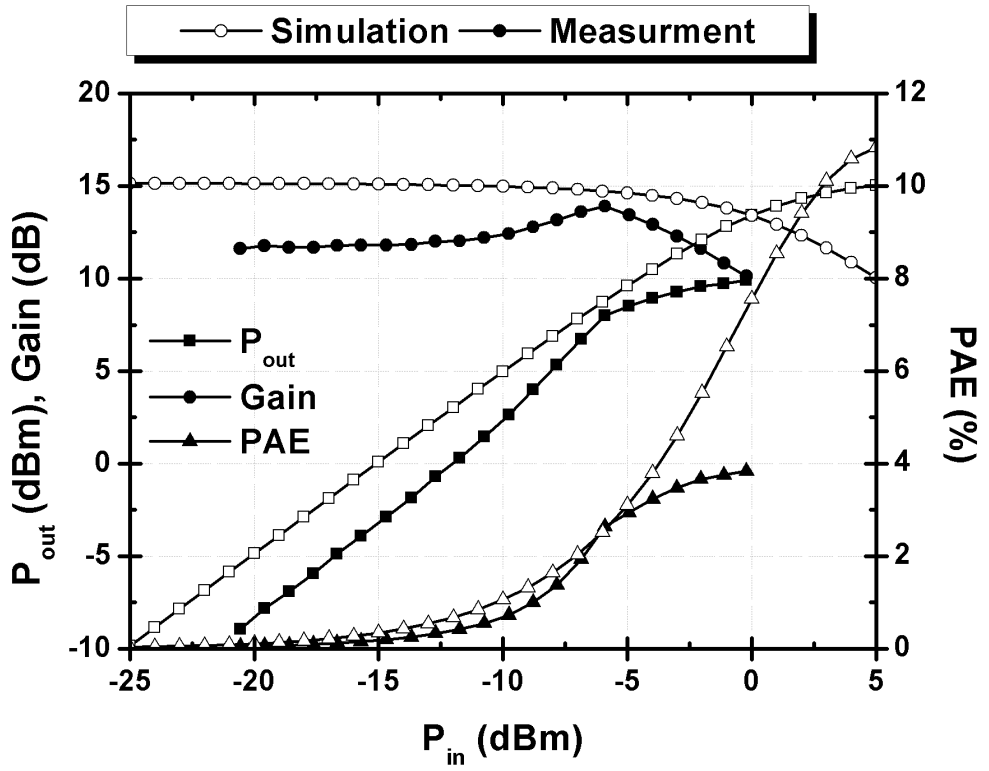

Fig. 4.48. Measured and simulated large-signal performance of the proposed W-band PA at 98 GHz.

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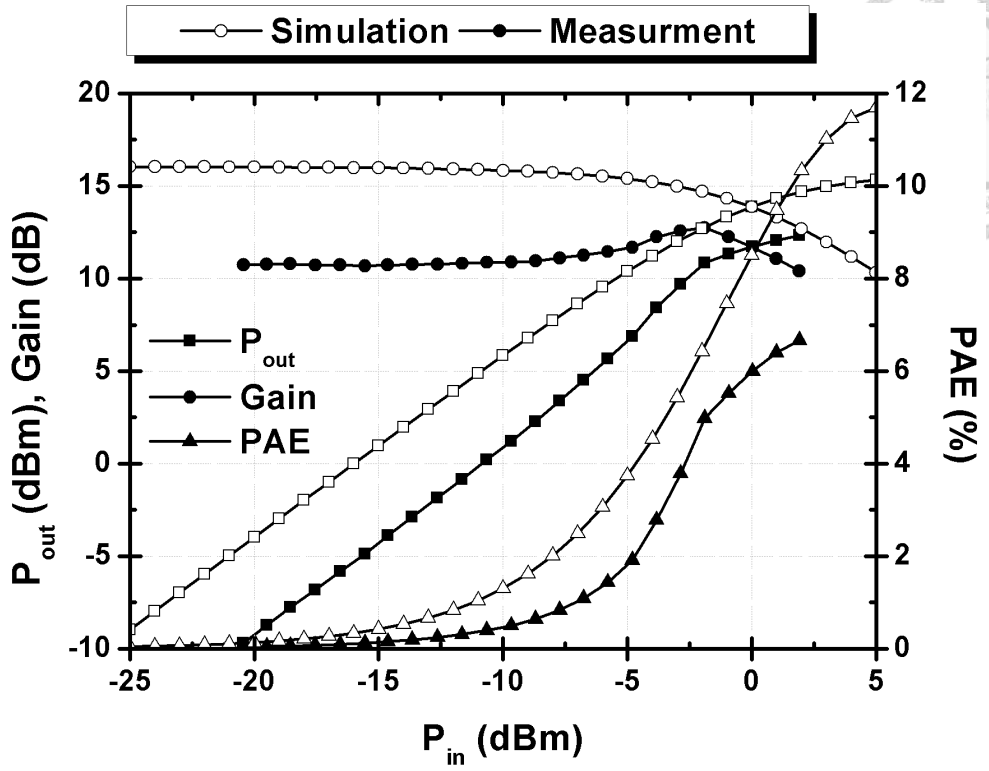

Fig. 4.49. Measured and simulated large-signal performance of the proposed W-band PA at 100 GHz.

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4.4 Discussion and Second Tape-out

4.4.1 Common-Mode Instability

Under identical setup used for small/large-signal measurements shown in section 4.3, undesired oscillations at around 47 GHz were also observed during measurement. An Agilent 8565EC spectrum analyzer was used for monitoring the output spectrum of the proposed PA. The PA was under the same bias conditions as in small/large-signal measurements with the input 50-Ω terminated. Fig. 4.50 shows the measured output spectrum with the oscillation at 47.24 GHz. The oscillation frequency varies only slightly between different dice measured. In order to identify the source of the oscillation, bias of different stages were turned off, i.e., V_{GS} = 0 V, to see whether the oscillation was still present. The oscillation remained present after turning off both the first and second driver stages. Therefore, source of the potential issue narrowed down to the output stage.

The oscillations at 47 GHz explain the 10% larger measured I_{DS} than simulation at the output stage, as listed in Table 4.1. As shown from Fig. 4.45 to 4.49, the measured large-signal performances at different frequencies all show rising gain up to certain P_{in} levels before returning to typical class-A behavior. The phenomena can also be explained by the oscillations at 47 GHz. As gain of the devices decrease with higher P_{in} levels, the instability condition and therefore power of the oscillation decreases. With lower oscillation power at higher P_{in} levels, gain of the PA rises and eventually returns to class-A behavior. As previously reported in [52], millimeter-wave oscillations in W-band PA designs are unlikely to be solved by off-chip bypass networks, but require further analyses and modifications to the circuit design.

As mentioned in section 4.3, the measured small- and large-signal performances do not agree well with simulation. The disagreement between small-signal measurement and simulation results is mainly in S_{21} and S_{22}. The cause of issue is therefore at the output stage. The transformer-based power combiner results in a more complicated layout design at the output than at the input.

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Inaccurate EM modeling of the complicated power combiner might cause the disagreement. On the other hand, the oscillation at 47 GHz are also coming from the output stage, and could also be the cause. A second tape-out in 65-nm CMOS was set for the proposed PA. To simplify the variables, the focus of the modifications is on eliminating the oscillation without altering the matching conditions of the original design. In order to verify the accuracy of EM simulations, test circuits base on the output transformer (TF_{out}) are also designed for the second tape-out.

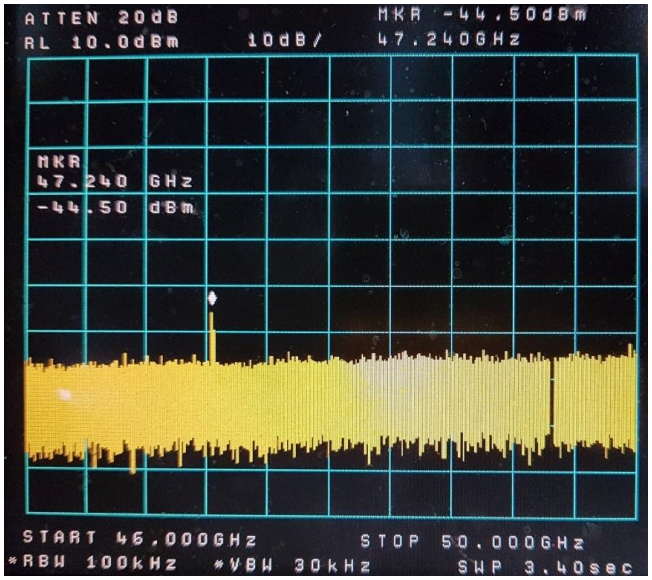

Fig. 4.50. Output spectrum of the proposed W-band PA showing an undesired oscillation at 47.24 GHz.

For bias-line stability analysis [53], port 1 and 2 are placed at the gate and drain bias-lines of the targeted amplifier stage, respectively. Both the in- and output of the overall circuit are 50-Ω terminated. Since the proposed PA is of left-right symmetry, the analyses can be performed on either half of the PA without loss of generosity. Fig. 4.51 shows the schematic of half the output stage with the bias networks, including the bypass capacitors and gate-bias resistor. Design of the output transformer-based combiner results in one gate bias-line (two combined in physical layout) and two drain bias-lines for each half of the output stage. There are therefore two cases with V_{G3} as port 1 and either of the V_{D3}'s as port 2. Fig. 4.52 shows the simulated stability factor of both cases. Stability factors of both cases exhibit sharp drops < 1, i.e., potential instability, at around 46.7 GHz, which are consistent with the oscillations at 47 GHz observed during measurement.

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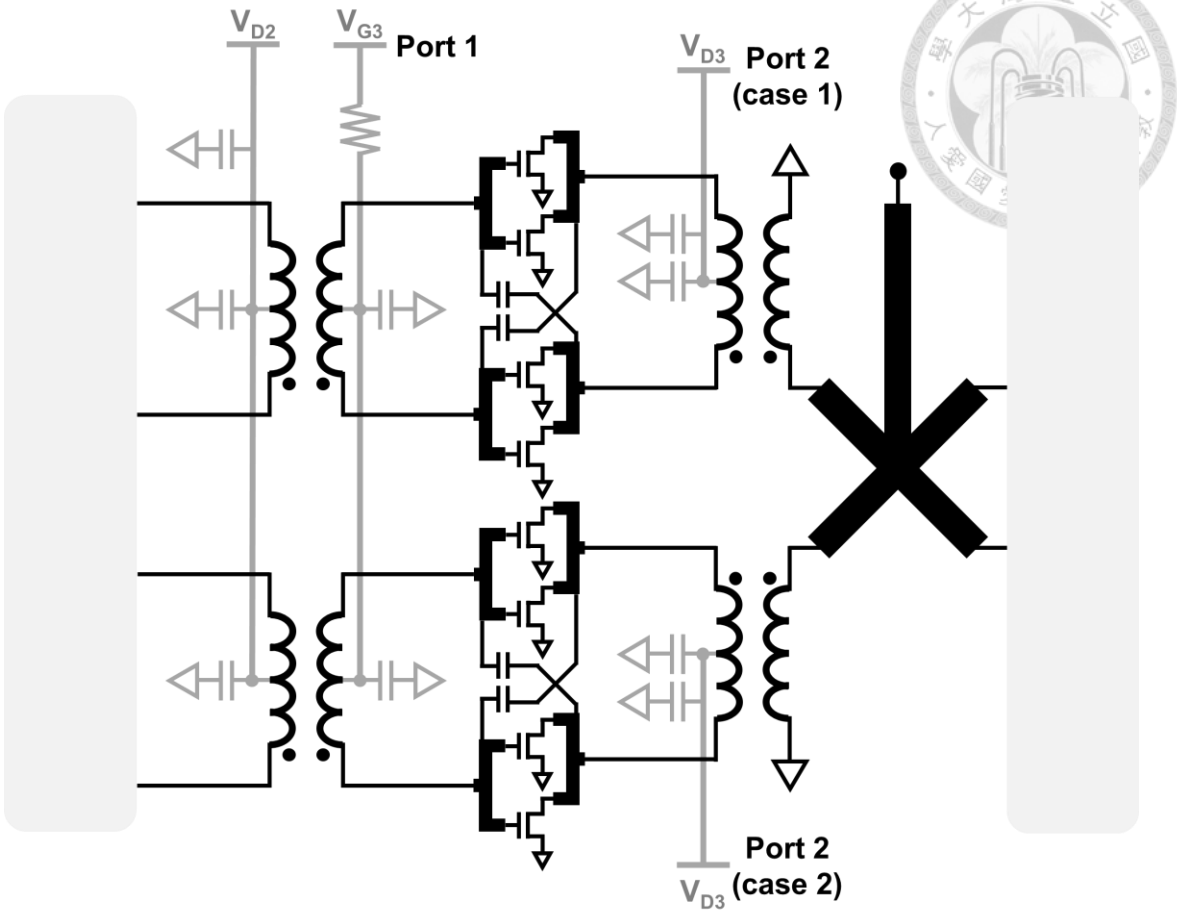

Fig. 4.51. Schematic of the simulation for bias-line stability analysis on the output stage.

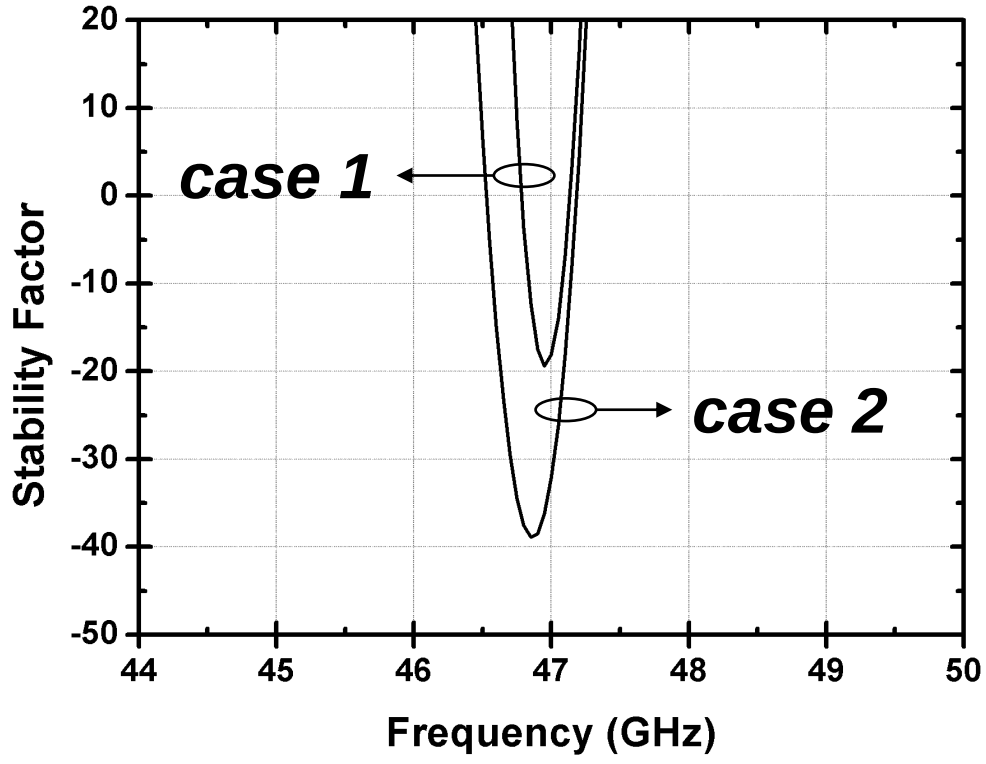

Fig. 4.52. Simulated stability factors from the two cases of bias-line analysis.

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As mentioned in section 4.2, all bias-feeding points of the proposed PA take advantage of virtual grounds at the center of differential transformers. Therefore, any undesired impedance fluctuations at the bias-lines will not be visible to the ideal differential-mode signal. However, any non-ideal, i.e., common-mode, signal component will be affected by impedance fluctuations at the bias-lines. Since bias-line stability analyses of the output stage indicates potential instability, the output stage complete with the inter-stage transformer TF_{inter2} and output transformer TF_{out} is further analyzed for common-mode stability. Fig. 4.53 shows the simulation setup, in which the two input (primary coil) nodes of TF_{inter2} are combined to ensure a common-mode operation. Since the bias network can be seen by the common-mode signal, the bypass capacitors and gate-bias resistor are included for common-mode stability simulations. As shown in Fig. 4.54, the simulated stability factor drops < 1 from around 43 to 56 GHz, which is consistent with the result of bias-line stability analysis.

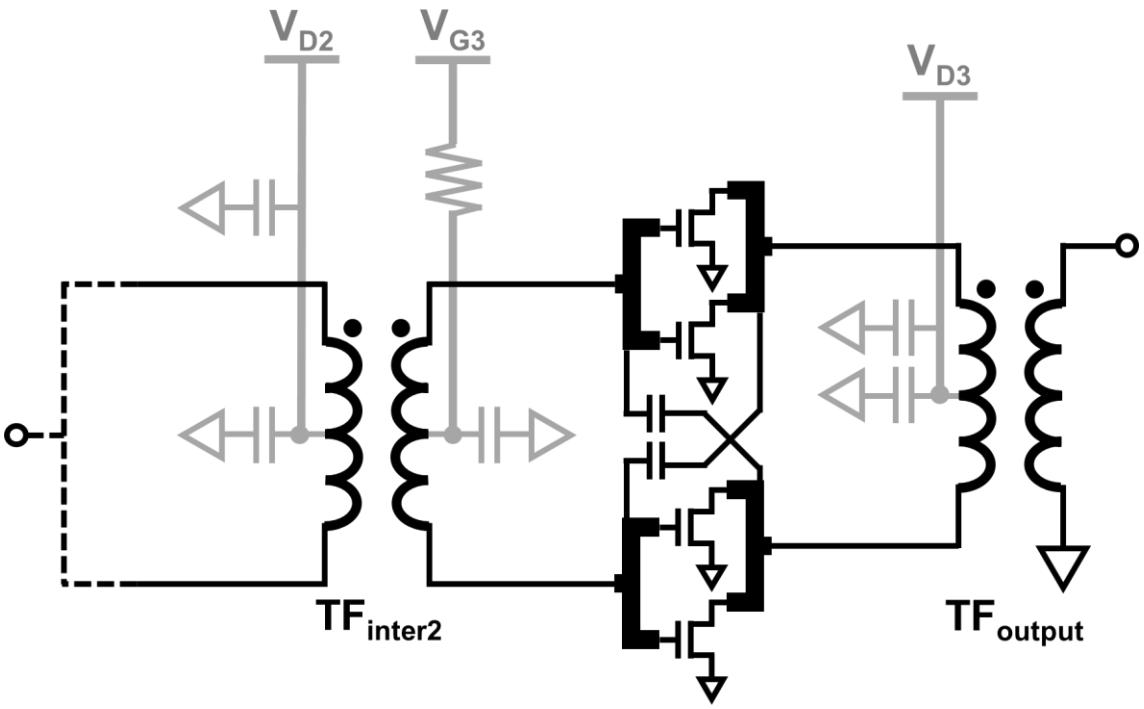

Fig. 4.53. Schematic of the simulation for the common-mode stability analysis of the output stage.

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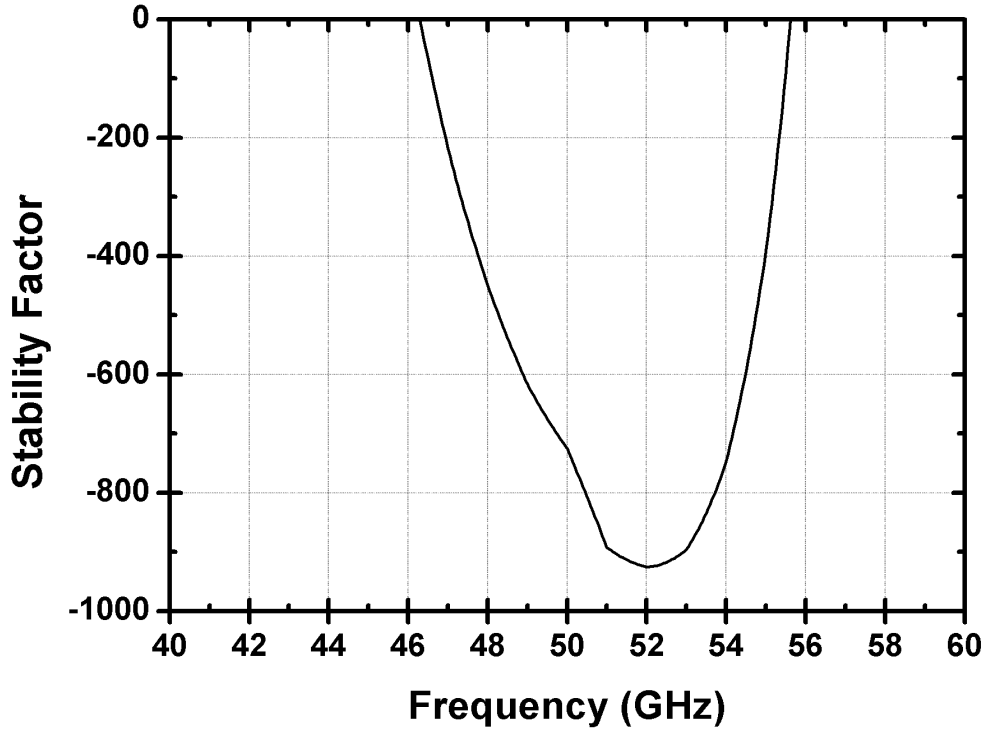

Fig. 4.54. Simulated stability factor of the common-mode stability analysis of the output stage.

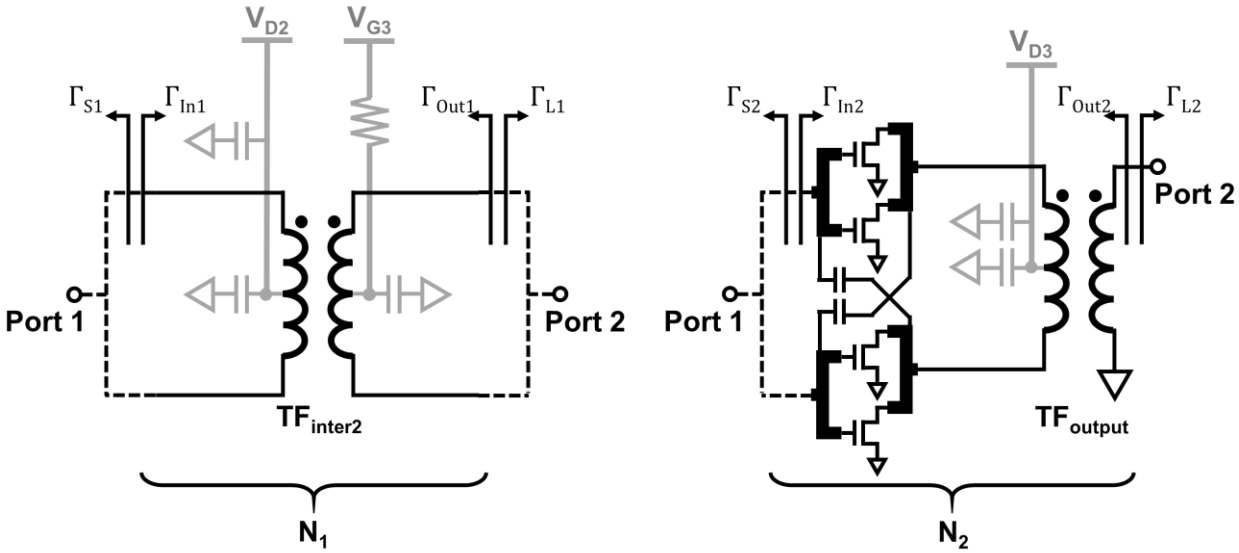

Fig. 4.55. Schematic of the simulation for the common-mode stability analysis of the output stage using stability circles.

The setup in Fig. 4.53 is separated for further stability analyses using stability circles. Fig. 4.55 shows the simulation setup, in which the setup in Fig. 4.53 is separated between TF_{iner2} and the output differential pair. Both the input (primary coil) and output (secondary coil) nodes of the

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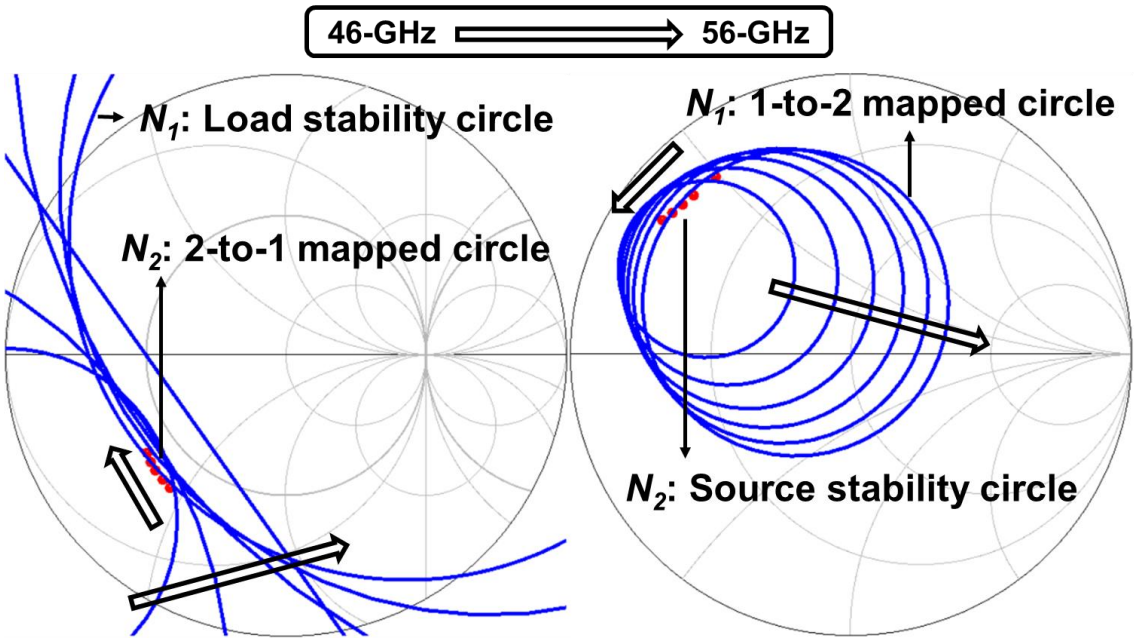
inter-stage transformer are combined to ensure a common-mode operation. The input nodes of the output stage differential pair are also combined to ensure a common-mode operation. This results in two two-port networks denoted here as N_1 and N_2. For N_1, the set of terminations with unity magnitude at port 1, i.e., the border of the Smith chart, are mapped to port 2. The 1-to-2 mapped circles are therefore defined by the loci of terminations on port 1 as seen at port 2. The 1-to-2 mapped circles of N_1 are then compared with the source stability circles of N_2. Any overlapping between the circles at the same frequency indicates that for some $|\Gamma_{S1}| < 1$ will result in a $|\Gamma_{Out2}| > 1$. Similarly, the 2-to-1 mapped circles of N_2 are compared with the load stability circles of N_1. Any overlapping between the circles at the same frequency indicates that for some $|\Gamma_{L1}| < 1$ will result in a $|\Gamma_{In1}| > 1$. Fig. 4.56 shows the simulated stability circles of N_1 and N_2 from 46 to 56-GHz with step of 2-GHz for clarity. As can be seen in Fig. 4.56(a), the 2-to-1 mapped circles of N_2 lies entirely within the load stability circles of N_1 from 46 to 50-GHz. In Fig. 4.56(b), the 1-to-2 mapped circles of N_1 lies entirely within the source stability circles of N_2 from 48 to 56-GHz. The simulation results both show consistent results with previous stability analyses.



(a) (b)

Fig. 4.56. Simulated stability circles from the common-mode stability analysis of the output stage.

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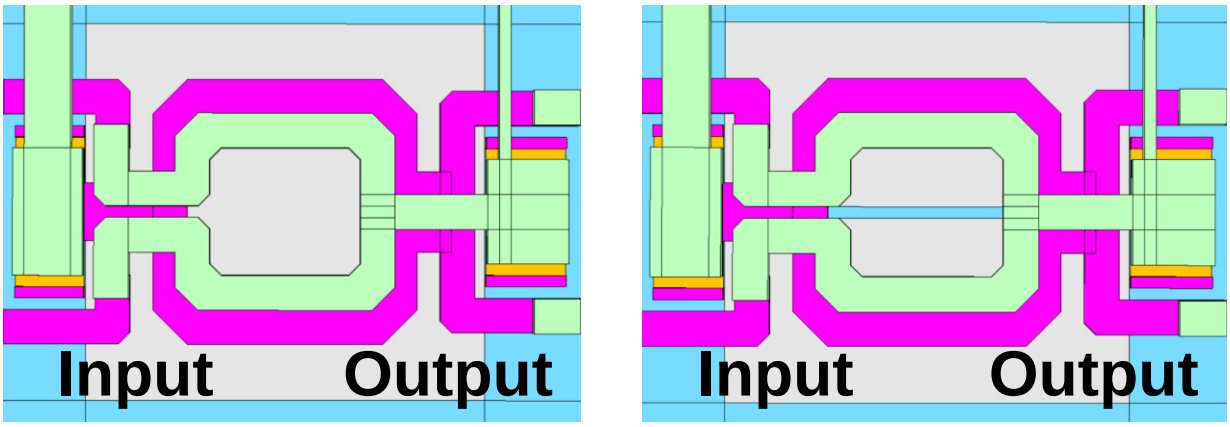
4.4.2 Design Modification

As mentioned above, the focus of the modifications is on eliminating the common-mode instability without affecting the matching conditions and circuit performance in differential mode. From the above analyses, the source of issue and therefore the potential candidates for modifications are transformers TF_{inter2}, and TF_{out}. To the differential-mode signal, the transformers before and after the modifications should provide identical matching conditions. On the other hand, the transformers after the modifications should alter the impedance seen by the common-mode signal, and therefore eliminate the instabilities.



(a) (b)

Fig. 4.57. Top views of the 3-D renderings of the inter-stage transformer TF_{inter2} (a) before and (b) after the proposed modification.

Fig. 4.57 shows the top views of the 3-D renderings of TF_{inter2} before and after the proposed modification. As can be seen, a metal strip of 2 μm width along the in/output direction is added to the middle of the ground (metal-1) plane underneath. Fig. 4.58 shows the post-EM simulated *S*-parameters of TF_{inter2} in common mode in both magnitude (in dB) and phase. For comparison, *S*-parameters without the proposed modification and with the added metal strip of different widths are shown here. As can be seen, the introduction of the metal strip of 2 μm width makes significant differences in impedances seen by the common-mode signal, and the effect becomes less prominent as the width of the metal strip increases to 6 μm. The decrease in $|S_{21}|$ indicates an increase in loss to the common-mode signal. Note that although the effect becomes more prominent as the frequency

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increases, *S*-parameters of only the targeted 40 to 60 GHz are shown here for clarity. On the other hand, Fig. 4.59 shows the post-EM simulated *S*-parameters of TF_{inter2} in differential mode in both magnitude (in dB) and phase. For comparison, *S*-parameters without the proposed modification and with the added metal strip of different widths are also shown here. As can be seen, regardless of the width of the metal strip, the addition of the metal strip makes little differences in impedances seen by the differential-mode signal throughout 0.01 to 200 GHz. Thus, the proposed modification to TF_{inter2} meets the requirement of altering the impedances seen by the common-mode signal, but not the ones seen by the differential-mode signal. Moreover, since the 2 μm width provides sufficient effect in common mode, 2 μm width is chosen for minimum modifications to the original design.

For an alternative approach, MAG/MSG is used to evaluate the loss of the transformer under matched conditions, i.e., excluding mismatch loss. Fig. 4.60 shows the MAG/MSG of TF_{inter2} in common and differential modes. As can be seen, the introduction of the metal strip increases the loss of TF_{inter2} in common mode by over 1 dB from 40 to 60 GHz. On the other hand, the introduction of the metal strip makes little difference to the loss of TF_{inter2} in differential mode. Nevertheless, the loss in differential mode still increases slightly with the width of the metal strip. Since the purpose of removing the ground plane underneath the transformer is to prevent undesired coupling of field, adding a wider metal strip makes the design less optimal in differential mode. Therefore, a 2-μm width is chosen for balance between eliminating instability in common mode and less additional loss in differential mode. The schematic in Fig. 4.55 is used for stability analysis after the modification to TF_{inter2}. Fig. 4.61 shows the simulated stability circles. In Fig. 4.61(a), the load stability circles of N_1 are pushed outside the Smith chart, and overlapping with the 2-to-1 mapped circles of N_2 is significantly reduced. However, overlapping still remains at 52 to 56 GHz. In Fig. 4.61(b), the 1-to-2 mapped circles of N_1 is shifted away from the source stability circles of N_2, and overlapping is also significantly reduced. However, overlapping also remains from 52 to 56 GHz. Therefore, further modifications are required to eliminate the instabilities.

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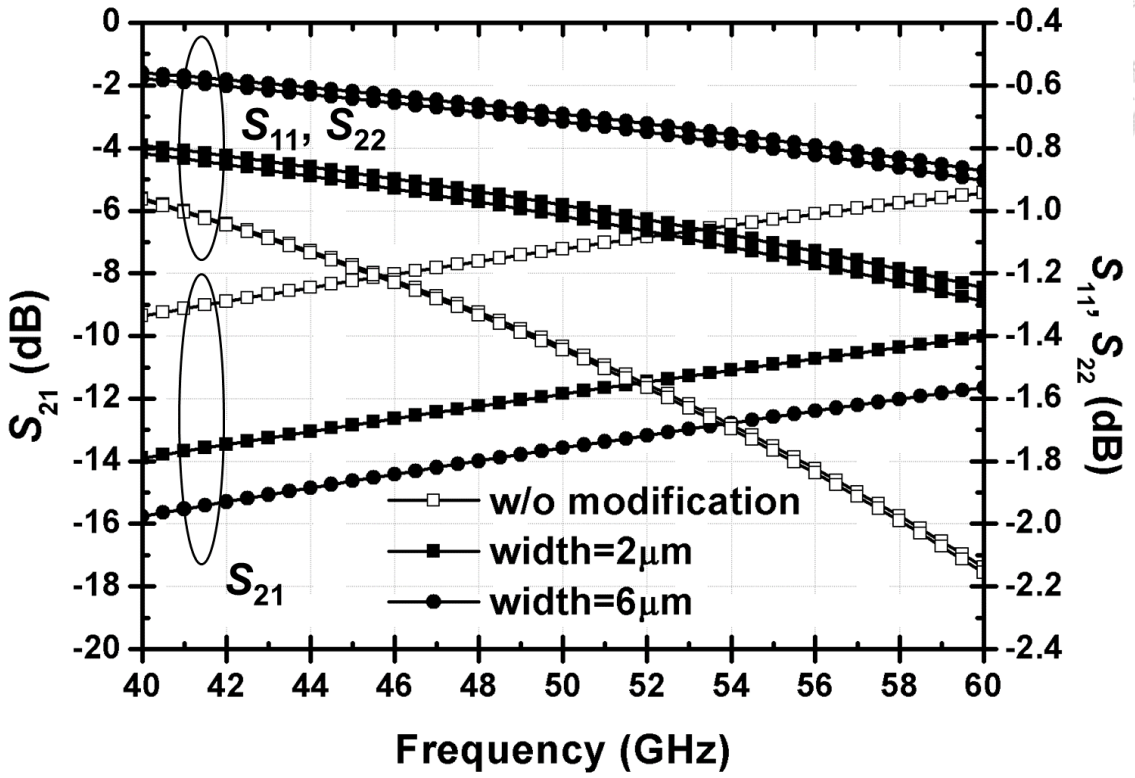
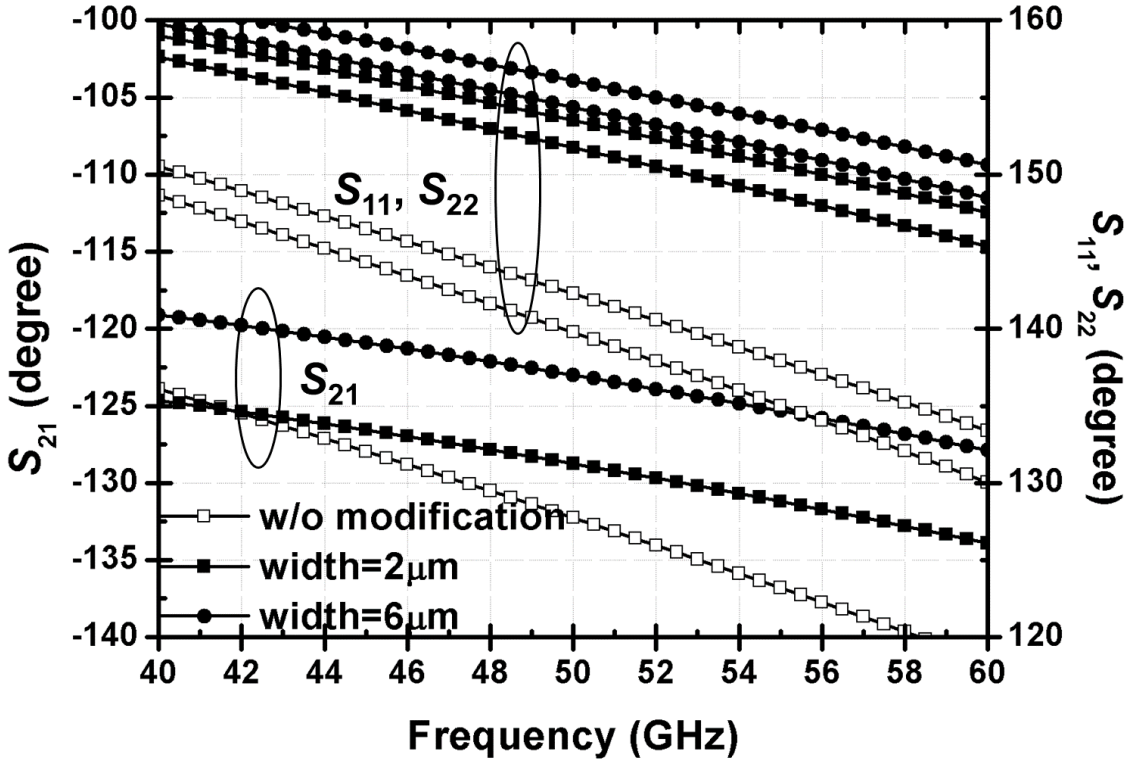


(a)



(b)

Fig. 4.58. Post-EM simulated *S*-parameters in common mode of the inter-stage transformer TF_{inter2} in (a) dB and (b) phase with/without the proposed modification.

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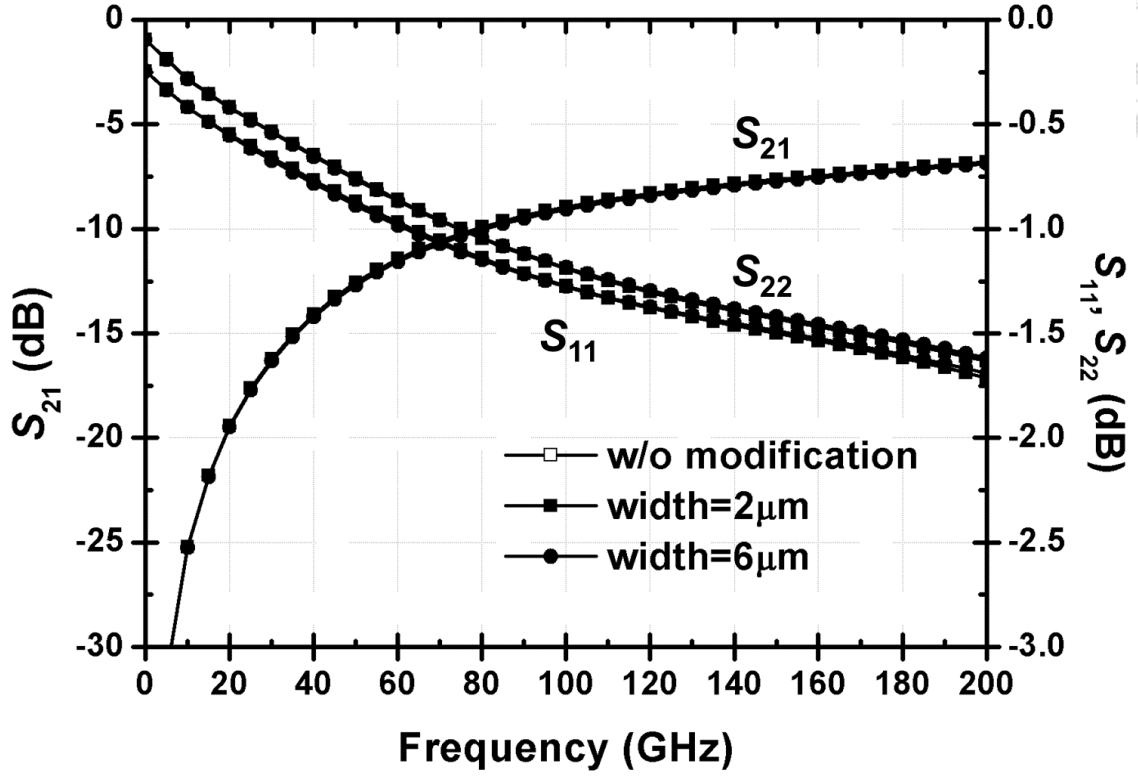
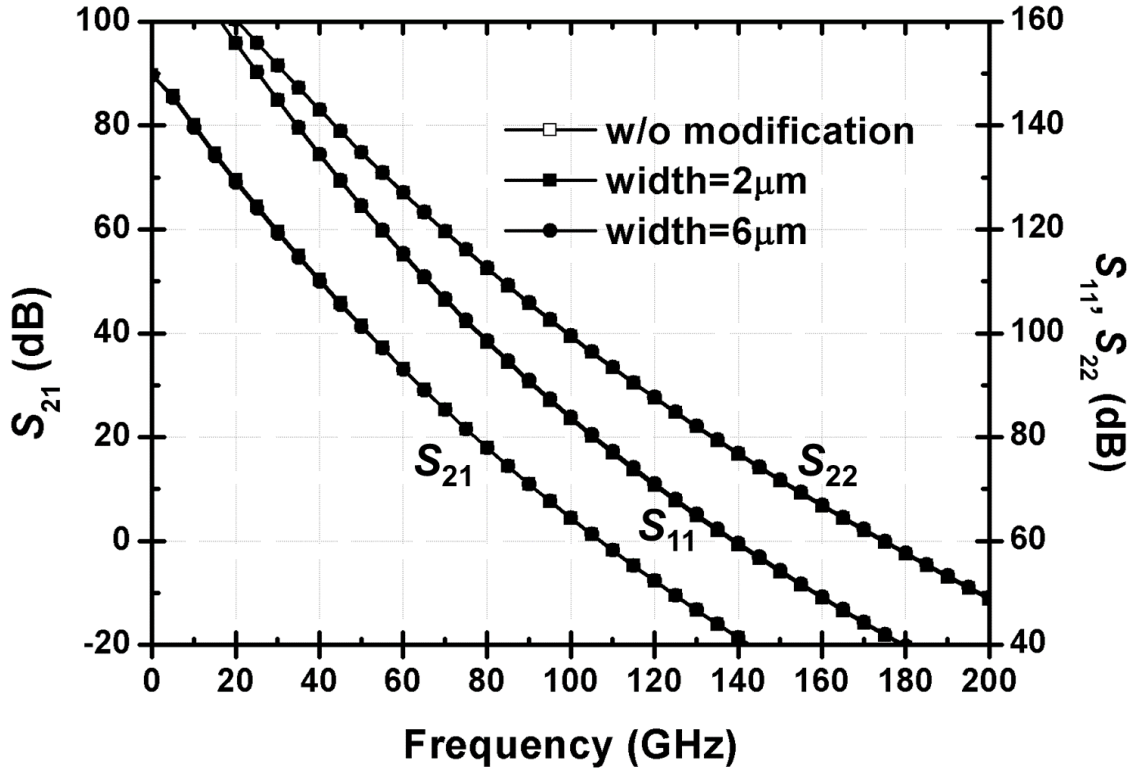


(a)



(b)

Fig. 4.59. Post-EM simulated *S*-parameters in differential mode of the inter-stage transformer TF_{inter2} in (a) dB and (b) phase with/without the proposed modification.

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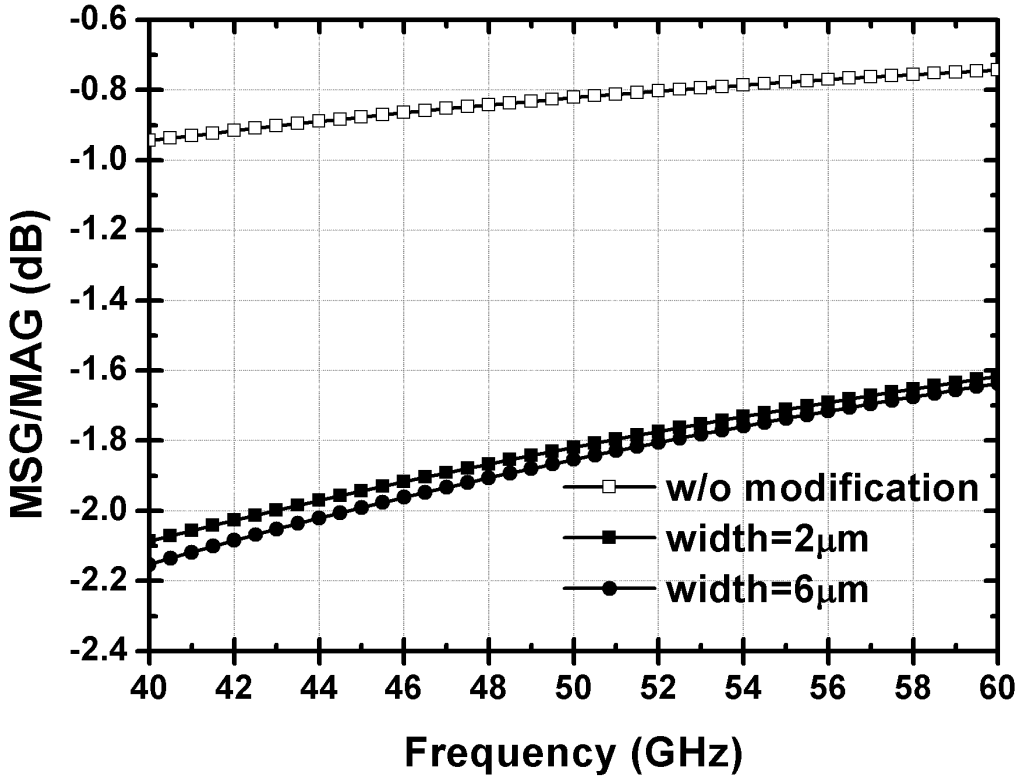
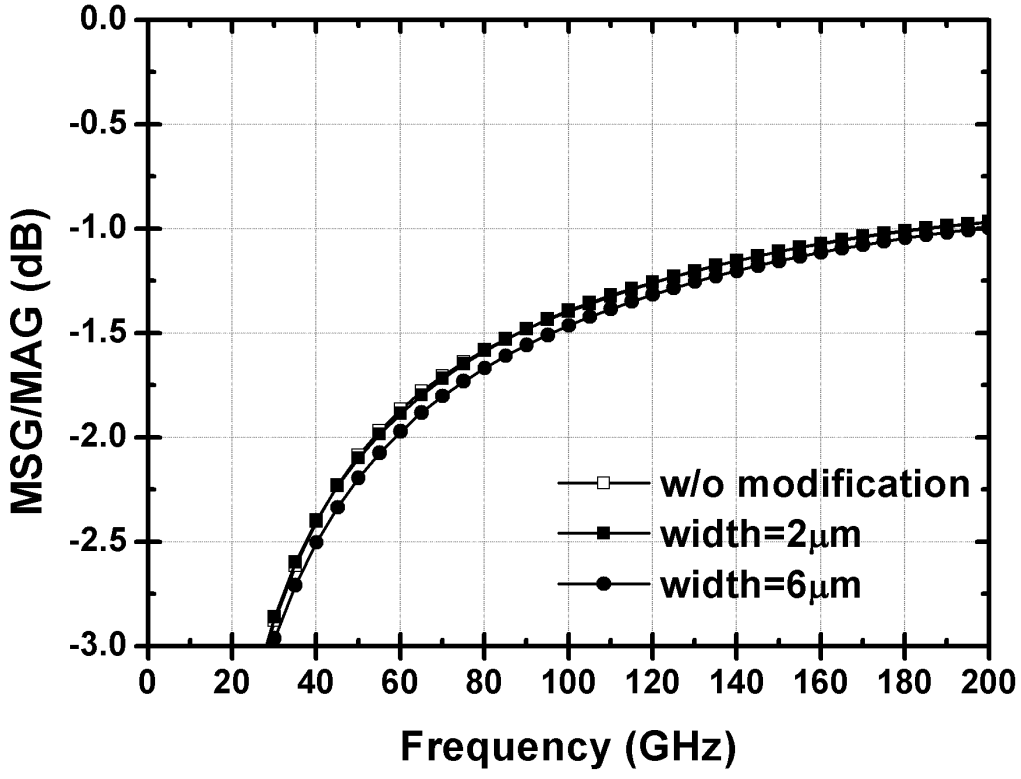


(a)



(b)

Fig. 4.60. Post-EM simulated loss of the inter-stage transformer TF_{inter2} using MSG/MAG in (a) common mode and (b) differential mode with/without the proposed modification.

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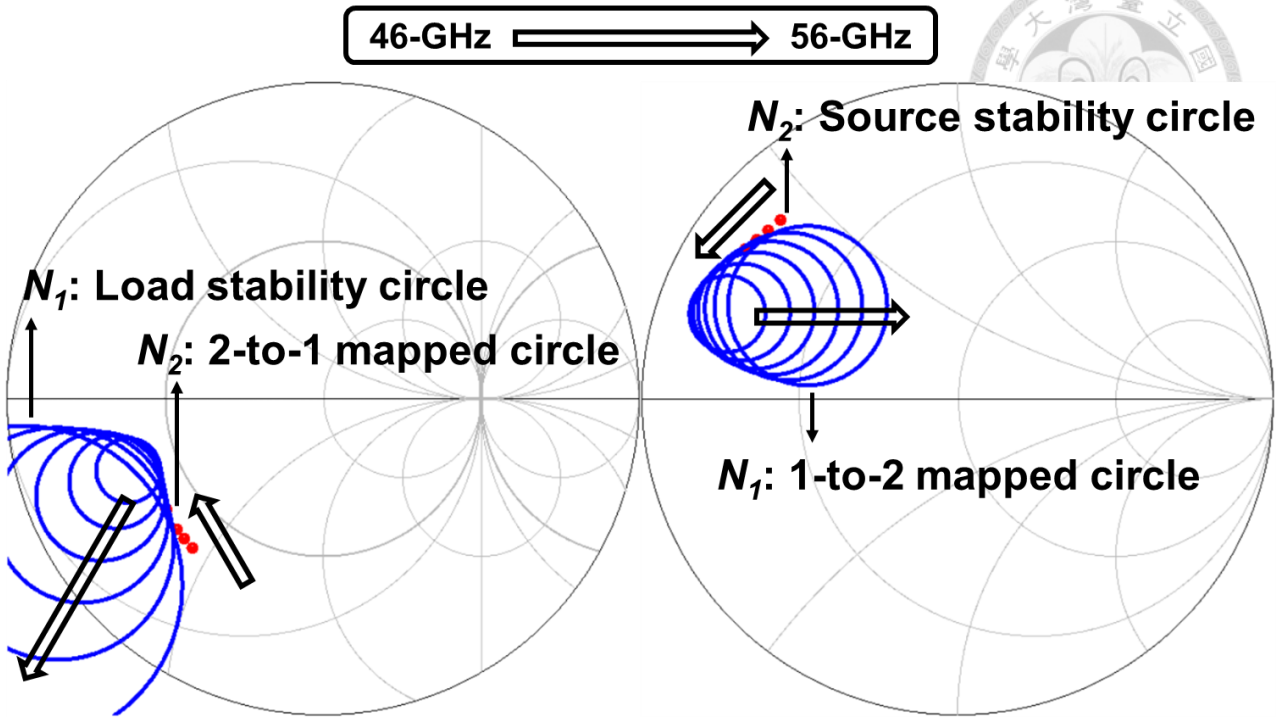
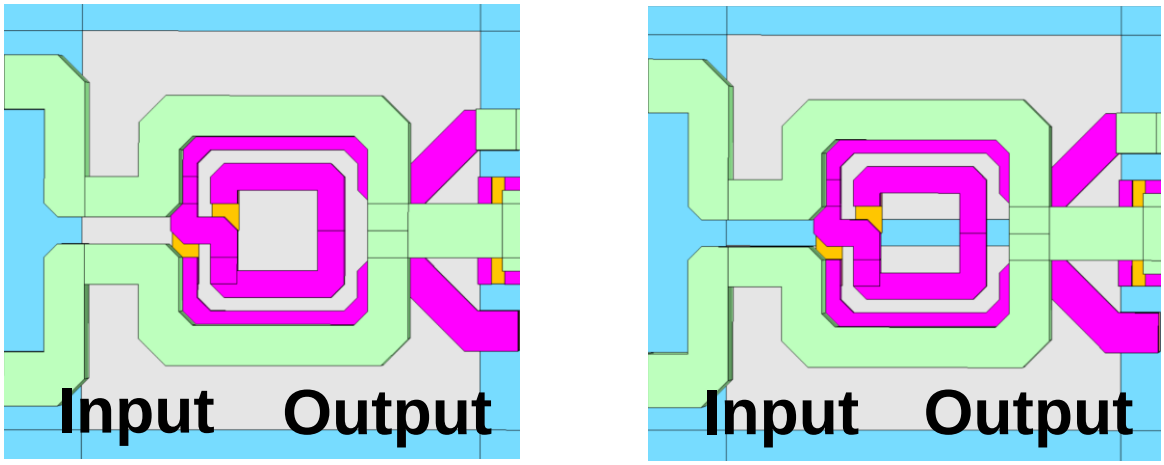


(a) (b)

Fig. 4.61. Post-EM simulated stability circles from the common-mode stability analysis of the output stage after the proposed modification to TF_{inter2}.



(a) (b)

Fig. 4.62. Top views of the 3-D renderings of the output transformer TF_{out} (a) before and (b) after the proposed modification.

Fig. 4.62 shows the top views of the 3-D renderings of TF_{out} before and after the proposed modification. As can be seen, a metal strip of 4 μm width along the in/output direction is added to the middle of the ground (metal-1) plane underneath. Fig. 4.63 shows the post-EM simulated *S*-parameters of TF_{out} in common mode in both magnitude (in dB) and phase. For comparison,

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S-parameters without the proposed modification and with the added metal strip of different widths are shown here. As can be seen, the introduction of the metal strip of 4 μm width makes significant differences in impedances seen by the common-mode signal, and the effect becomes less prominent as the width of the metal strip increases to 8 μm. The decrease in $|S_{21}|$ indicates an increase in loss to the common-mode signal. Note that since TF_{out} is of differential-to-single configuration, the differences made in common mode are mainly at the input (port 1). Though the effect becomes more prominent as the frequency increases, *S*-parameters of only the targeted 40 to 60 GHz are shown here for clarity. On the other hand, Fig. 4.64 shows the post-EM simulated *S*-parameters of TF_{out} in differential mode in both magnitude (in dB) and phase. For comparison, *S*-parameters without the proposed modification and with the added metal strip of different widths are also shown here. As can be seen, regardless of the width of the metal strip, the addition of the metal strip makes little difference in impedance seen by the differential-mode signal throughout 0.01 to 200 GHz. Thus, the proposed modification to TF_{out} also meets the requirement of altering the impedances seen by the common-mode signal, but not the ones seen by the differential-mode signal. Moreover, since the 4μm width provides sufficient effect in common mode, 4μm width is chosen for minimum modifications to the original design. The simulation setup in Fig. 4.55 is used for stability analyses after the modifications to both TF_{inter2} and TF_{out}. Fig. 4.65 shows the post-EM simulated stability circles. Compared with Fig. 4.61, Fig. 4.65(a) shows that the 2-to-1 mapped circles of N_2 are shifted further away from the load stability circles of N_1, and overlapping no longer exists. Similarly, Fig. 4.65(b) shows that the source stability circles of N_2 are shifted further away from the 1-to-2 mapped circles of N_1, and overlapping no longer exists.

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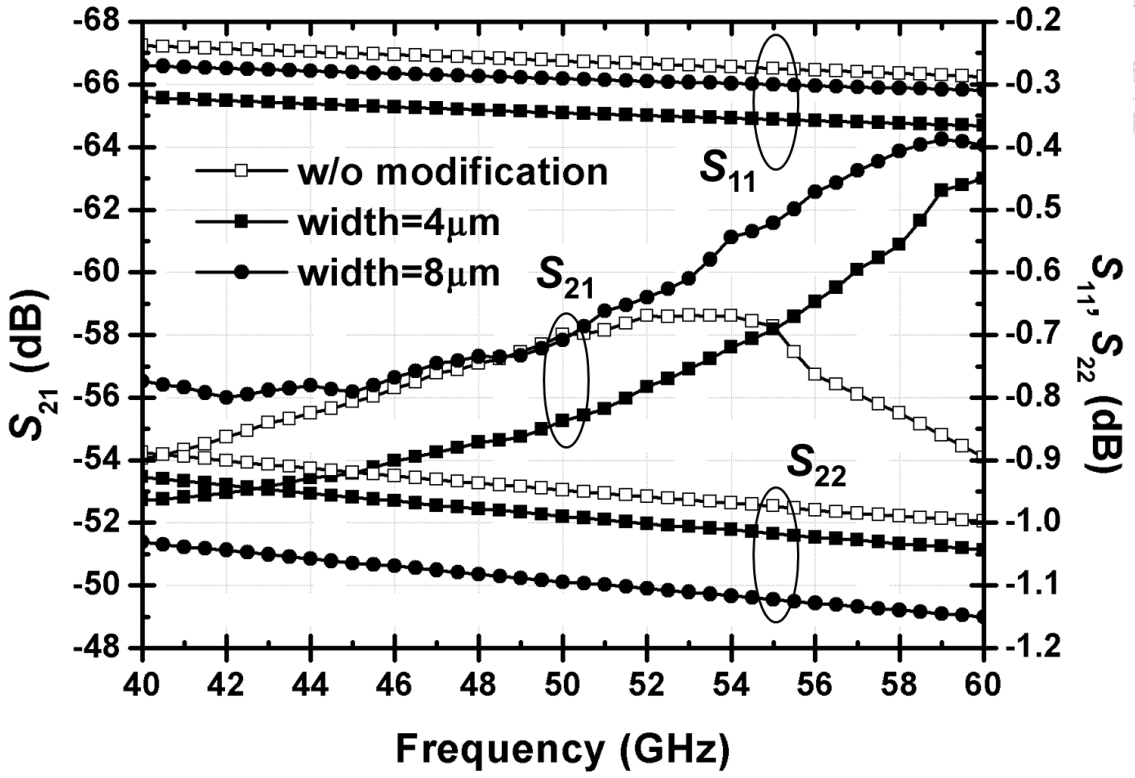
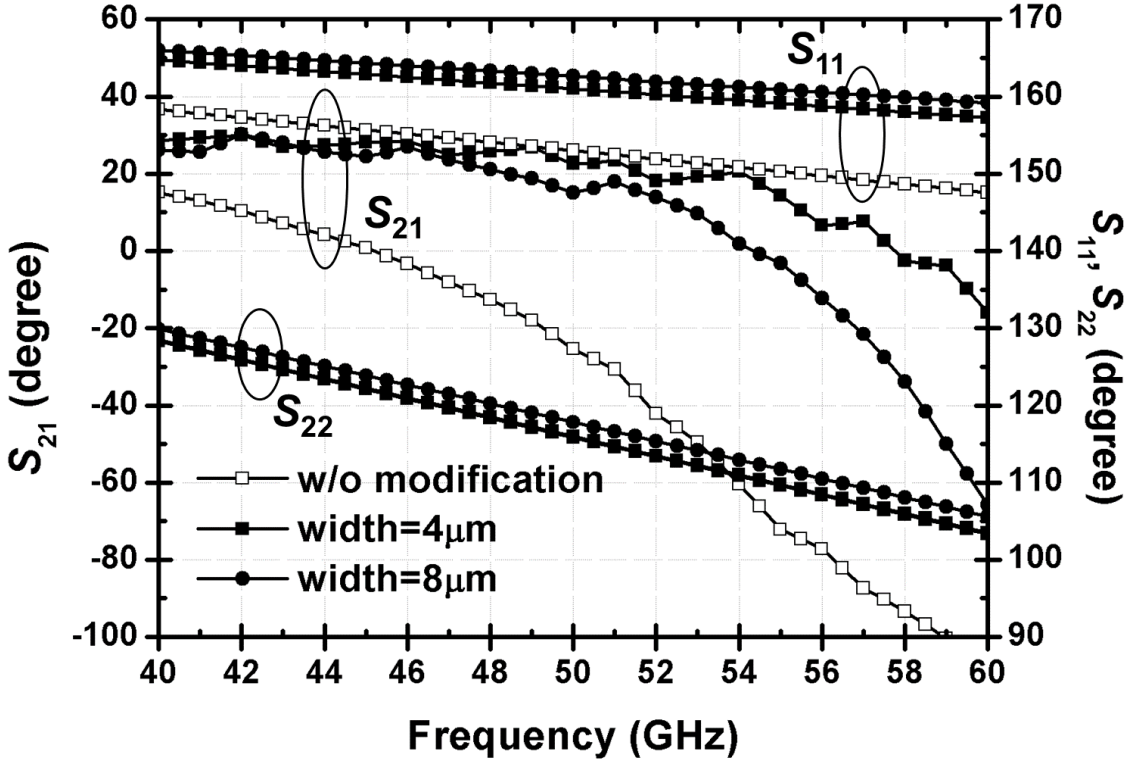


(a)



(b)

Fig. 4.63. Post-EM simulated *S*-parameters in common mode of the output transformer TF_{out} in (a) dB and (b) phase with/without the proposed modification.

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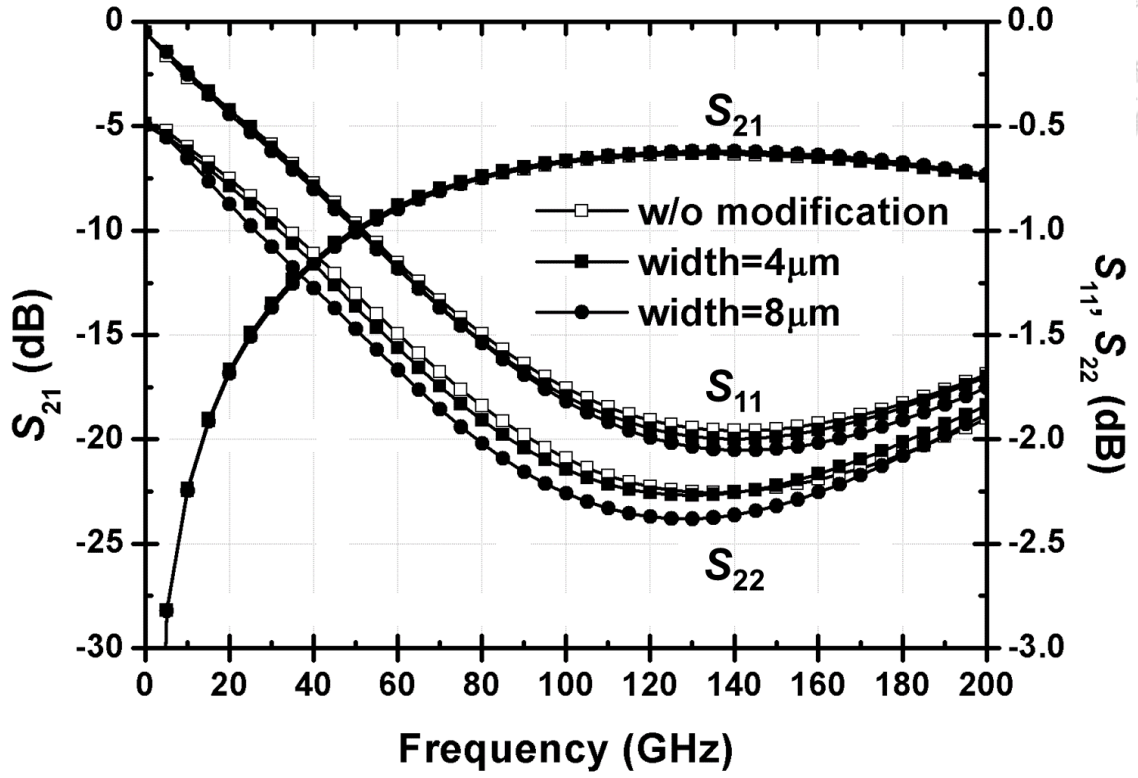
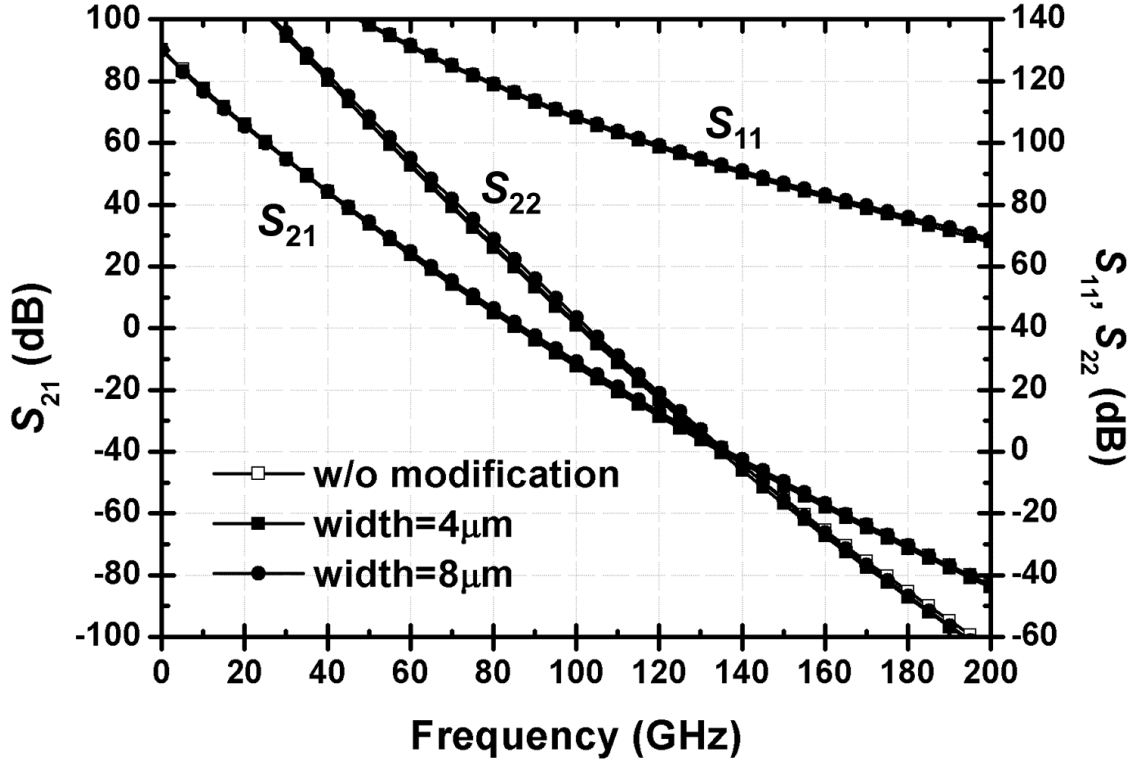


(a)



(b)

Fig. 4.64. Post-EM simulated *S*-parameters in differential mode of the output transformer TF_{out} in (a) dB and (b) phase with/without the proposed modification.

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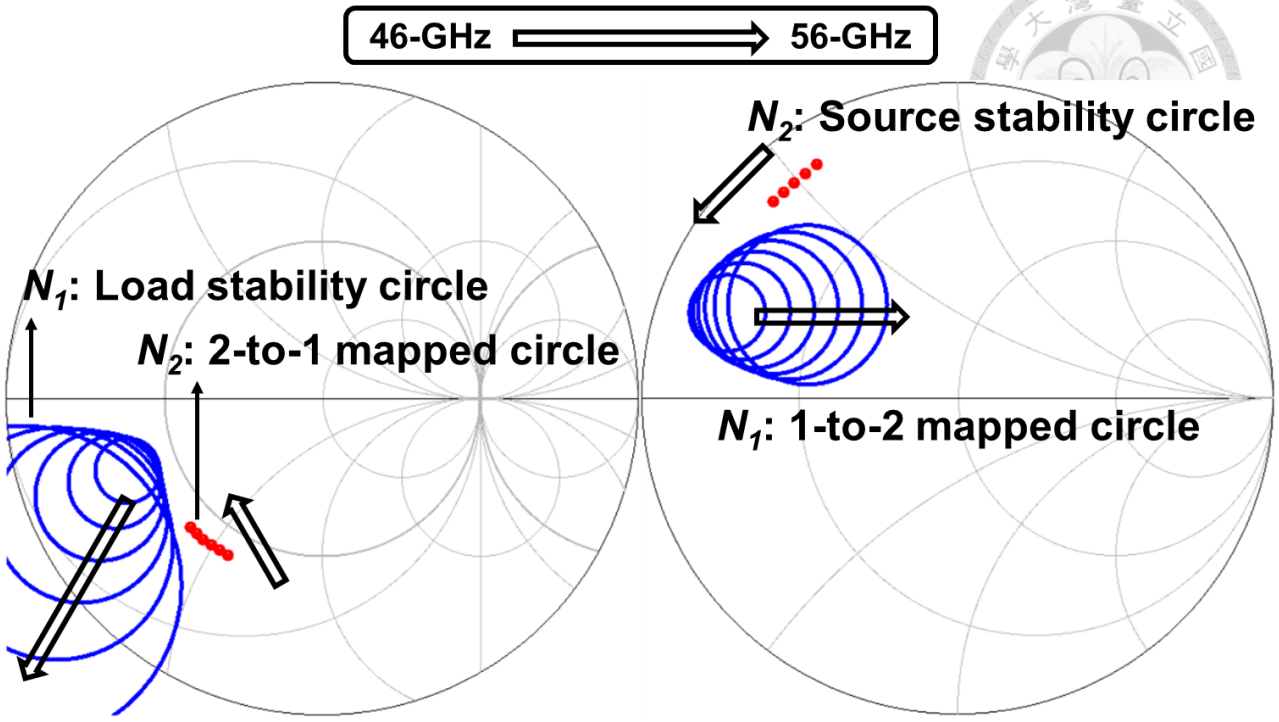

Fig. 4.65. Post-EM simulated stability circles from the common-mode stability analysis of the output stage after the proposed modifications to TF_{inter2} and TF_{out}.

In order to verify the proposed modifications to TF_{inter2} and TF_{out}, the common-mode stability analysis shown in Fig. 4.53 is revisited. Fig. 4.66 shows the simulated stability factor, in which the sharp drop < 1 is successfully eliminated. The bias-line stability analyses of the output stage are also performed. Fig. 4.67 shows the simulated stability factors, in which the sharp drops < 1 are also successfully eliminated. On the other hand, since the modifications has little effect on the matching conditions under differential-mode operations, the circuit performance remains unchanged. Fig. 4.68 and 4.69 shows simulated small-signal performance and large-signal performance at 110 GHz, respectively. As can be seen, both the small- and large-signal performances are unaffected by the modifications just as expected.

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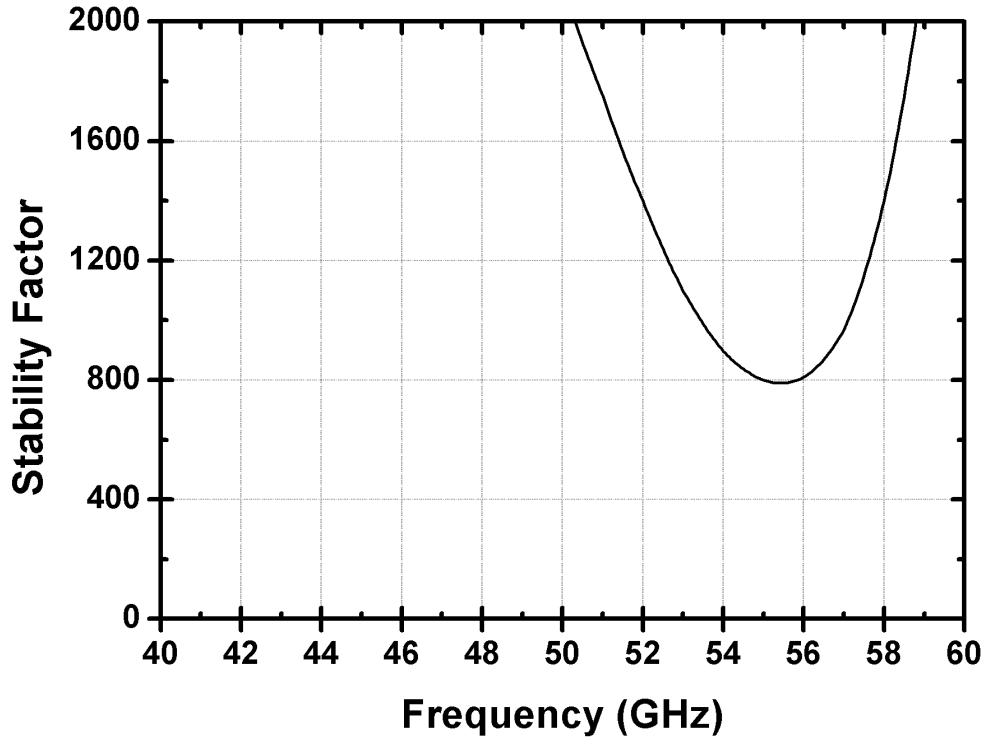

Fig. 4.66. Simulated stability factor of the common-mode stability analysis of the output stage after the proposed modifications to TF_{inter2} and TF_{out}.

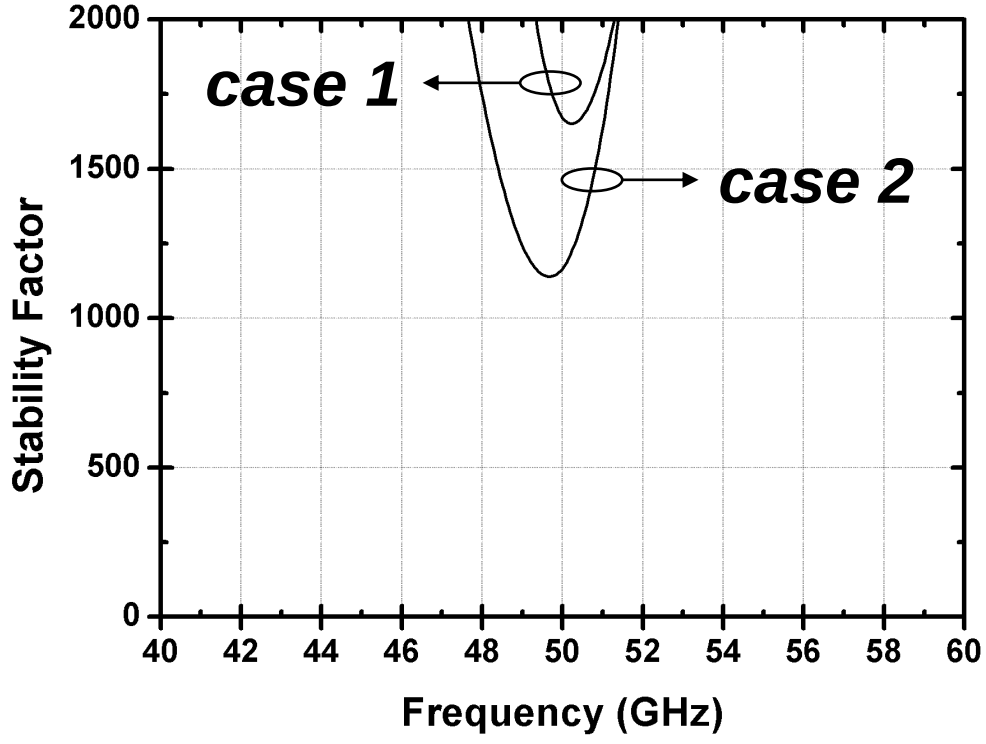

Fig. 4.67. Simulated stability factors from the two cases of bias-line analysis after the proposed modifications to TF_{inter2} and TF_{out}.

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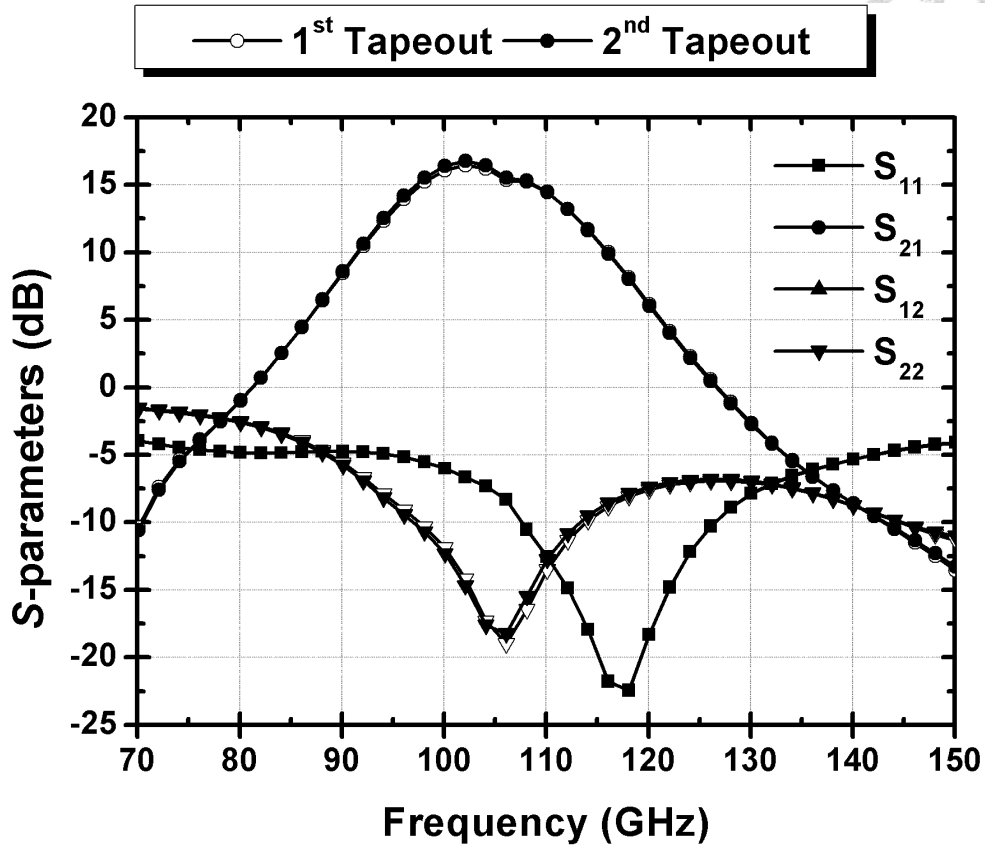

Fig. 4.68. Simulated *S*-parameters of the proposed W-band PA before (first tape-out) and after (second tape-out) the modifications.

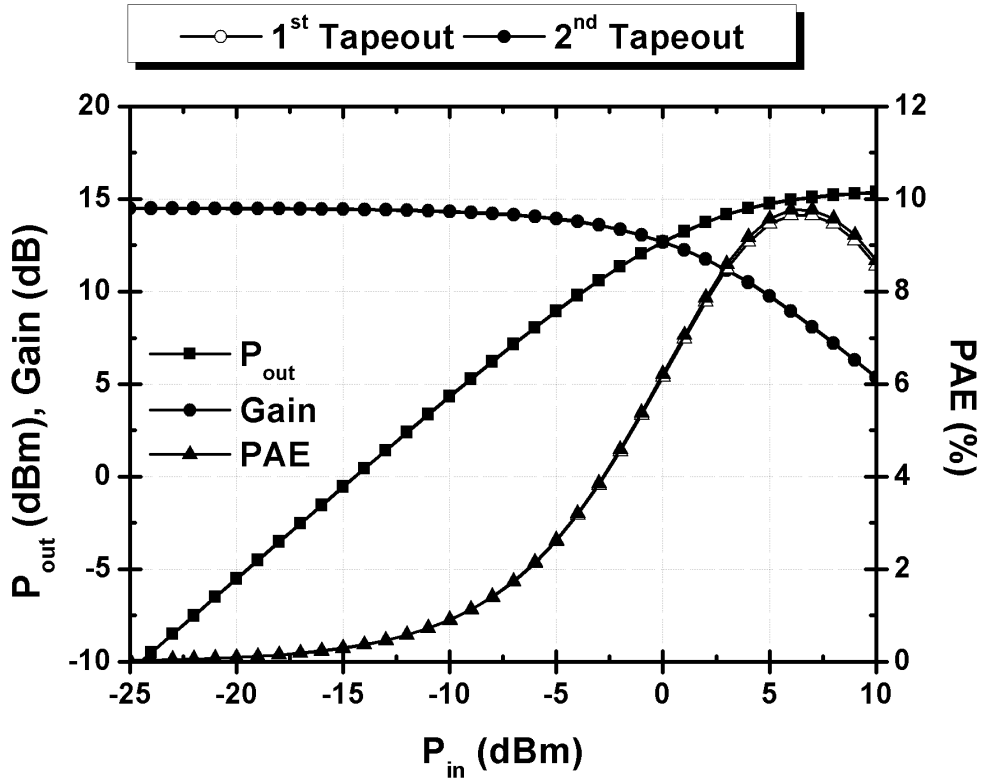

Fig. 4.69. Simulated large-signal performance of the proposed W-band PA at 110-GHz before (first tape-out) and after (second tape-out) the modifications.

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It is worth noting that although both gain and stability in differential mode are improved by adopting neutralization technique, the addition of the cross-coupled C_N's increases the equivalent C_{gd} of the devices in common mode. The common-mode gain and stability suffers as a result. Fig. 4.70 shows the common-mode MSG/MAG and stability factor of the output stage differential pair. Therefore, the aforementioned instability can also be eliminated by lowering the C_N values used in output stage. However, since the approach will degrade the circuit performance, stability, and alter the matching conditions in differential mode, it is considered as an alternative of lower priority.

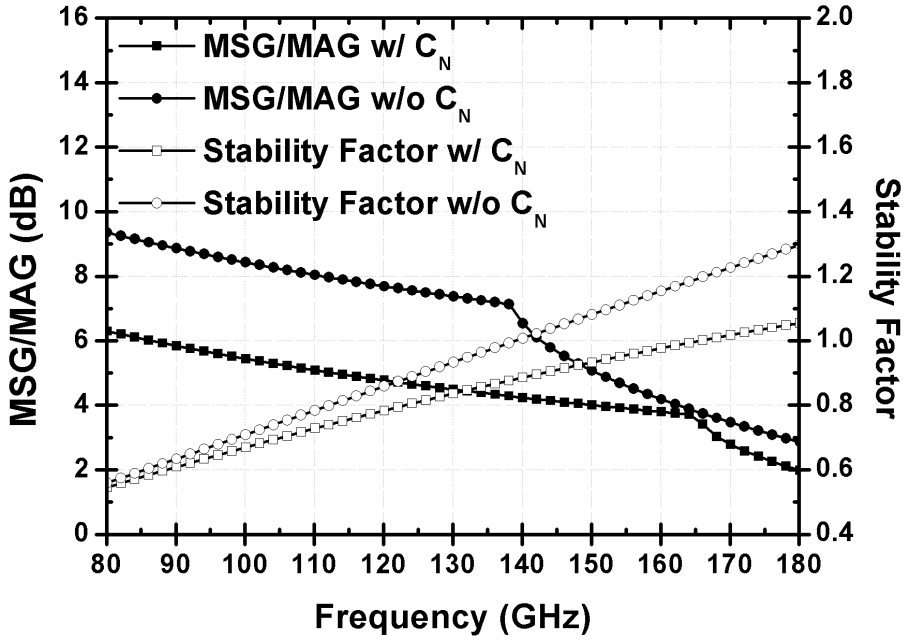
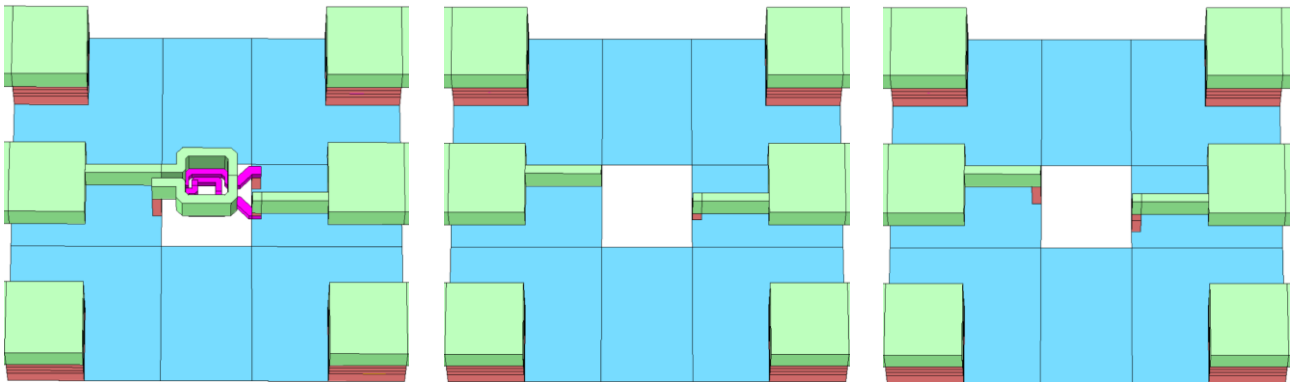


Fig. 4.70. Simulated common-mode MSG/MAG and stability factor of the output differential cell with/without C_N.



(a) (b) (c)

Fig. 4.71. 3-D renderings of the three components of the transformer test circuit: (a) TEST_CIRCUIT, (b) OPEN, and (c) SHORT.

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4.4.3 Transformer Test Circuit

Transformer test circuits are also designed and realized along with the PA for the second tape-out. Since the main purpose of the test circuit is to verify the modeling accuracy of the EM simulation for transformer designs at W-band, the differential primary coil of the transformer is made single-ended by grounding one of the input nodes for simple measurement and analysis.

In order to extract the small-signal performance of the transformer from the measurement results, open-short de-embedding is adopted for the test circuit. Fig. 4.71 shows the 3-D rendering of the three components of the test circuit, which are denoted from (a) to (c) as TEST_CIRCUIT, OPEN, and SHORT, respectively. TEST_CIRCUIT contains the transformer (device-under-test, DUT) connected to the two GSG RF pads through two micro-strip lines. OPEN and SHORT contains only the connecting micro-strip lines with open and short ends, respectively. Fig. 4.72 shows the basic concept of open-short de-embedding. Form the measurement results of the TEST_CIRCUIT, OPEN, and SHORT, the measured S-parameters of the DUT can be extracted. First, the pad capacitance, substrate resistance, and coupling between two ports of the TEST_CIRCUIT is removed by

$$Y'_{\mathrm{TEST}} = Y_{\mathrm{TEST}} - Y_{\mathrm{OPEN}} \quad . \tag{4.12}$$

Then, the pad capacitance, substrate resistance, and coupling between two ports of the SHORT is also removed by

$$Y'_{\mathrm{SHORT}} = Y_{\mathrm{SHORT}} - Y_{\mathrm{OPEN}} \quad . \tag{4.13}$$

Finally, the *S*-parameters of the DUT can be extracted by removing the self-inductance and resistance of the connecting micro-strip lines by

$$\begin{gathered} Z_{\mathrm{DUT}} = Z'_{\mathrm{TEST}} - Z'_{\mathrm{SHORT}} \\ Z_{\mathrm{DUT}} \rightarrow S_{\mathrm{DUT}} \end{gathered} \quad . \tag{4.14}$$

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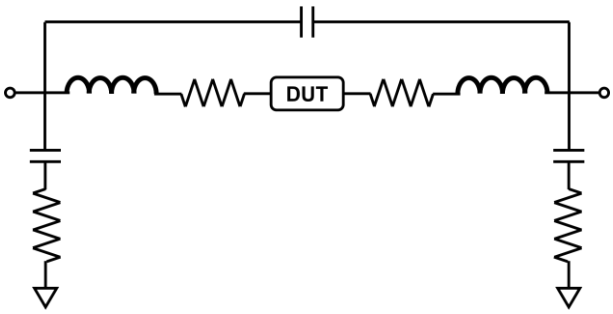
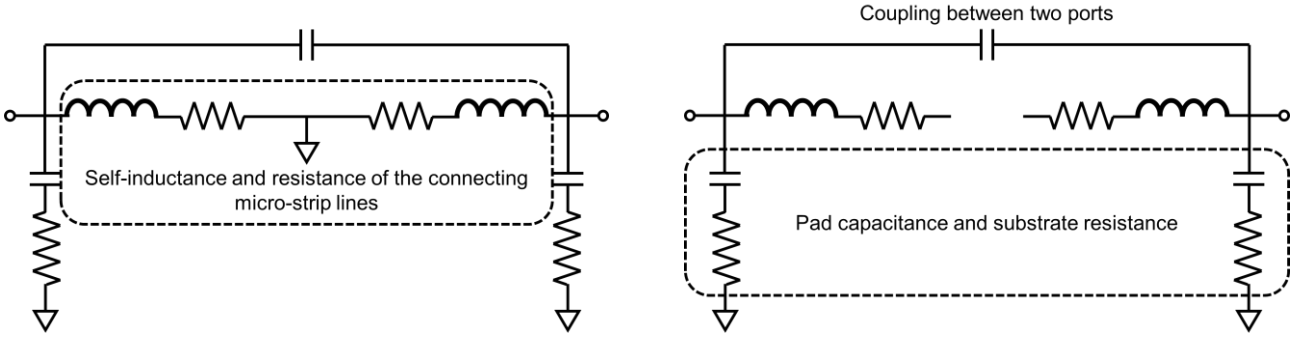


(a)



(b) (c)

Fig. 4.72. Basic concept of open-short de-embedding, with circuit schematics of (a) DUT, (b) SHORT, and (c) OPEN.

4.4.4 Experimental Results

For the second tape-out, the proposed W-band PA design was fabricated in the same 65-nm CMOS process by TSMC. Since the difference between the original and modified PA is only at the aforementioned modifications to the transformers, the chip layout remains mostly unchanged. All measurements were performed via on-wafer probing. Dice were mounted on PCB boards with bond-wiring for bias applications. Off-chip bypass networks were designed and implemented on the PCB boards.

Table 4.2. Bias conditions during small-signal measurements.

	V_{GS} (V)			V_{DS} (V)	I_{DS} (mA)		
	Sim.	**Meas.**			**Sim.**	**Meas.**	
1st driver stage	0.8	0.8	0.75	2.0	35	40.1	36.2
2nd driver stage	0.8	0.8	0.73	2.0	70	82.2	70.8
Output stage	0.8	0.8	0.71	2.0	136	168.5	137.7

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Table 4.2 shows two sets of bias conditions during small-signal measurements. First, the V_{GS}'s are matched with simulation at 0.8 V, the measured I_{DS}'s of three stages are all around 20% larger than simulation as a result. On the other hand, the measured I_{DS}'s of three stages can each be matched to simulation with lower V_{GS}'s. Since the difference in measured V_{GS} between each stage and simulation is rather small, the bias condition with matched I_{DS}'s is set for small- and large-signal measurements.

An Agilent 8565EC spectrum analyzer was first used for monitoring the output spectrum of the modified PA with the input 50-Ω terminated. The PA showed no undesired oscillations below 50 GHz, indicating a successful elimination of the common-mode instability at 47 GHz. An Agilent 8510C vector network analyzer was used for small-signal measurements up to 110 GHz. Fig. 4.73 shows the measured *S*-parameters of the modified PA in the second tape-out. The measured S_{11} agrees well with simulation. However, both the measured S_{21} and S_{22} show a shift towards lower frequencies compared to simulation. The measurement shows a 12 GHz 3-dB bandwidth with peak gain of 15.3 dB at 97 GHz, compared to a 20 GHz 3-dB bandwidth with peak gain of 16.4 dB at 102 GHz and gain of 14.4 dB at 110 GHz in simulation. Measured gain at 110 GHz is only 6.3 dB as a result.

Fig. 4.74 shows the measured *S*-parameters of the original and modified PA in the first and second tape-outs, respectively. The measurement results show almost identical results, aside from the modified PA showing a 4-dB increase in gain from 70 to 110 GHz and a slight increase in output return loss. From Fig. 4.73 and 4.74, eliminating the common-mode instability results in a 4 dB gain increase or otherwise rather similar measurement results. This indicates that the shifts in S_{21} and S_{22} toward lower frequencies compared with simulation are mostly due to inaccurate EM modeling, as will be discussed later.

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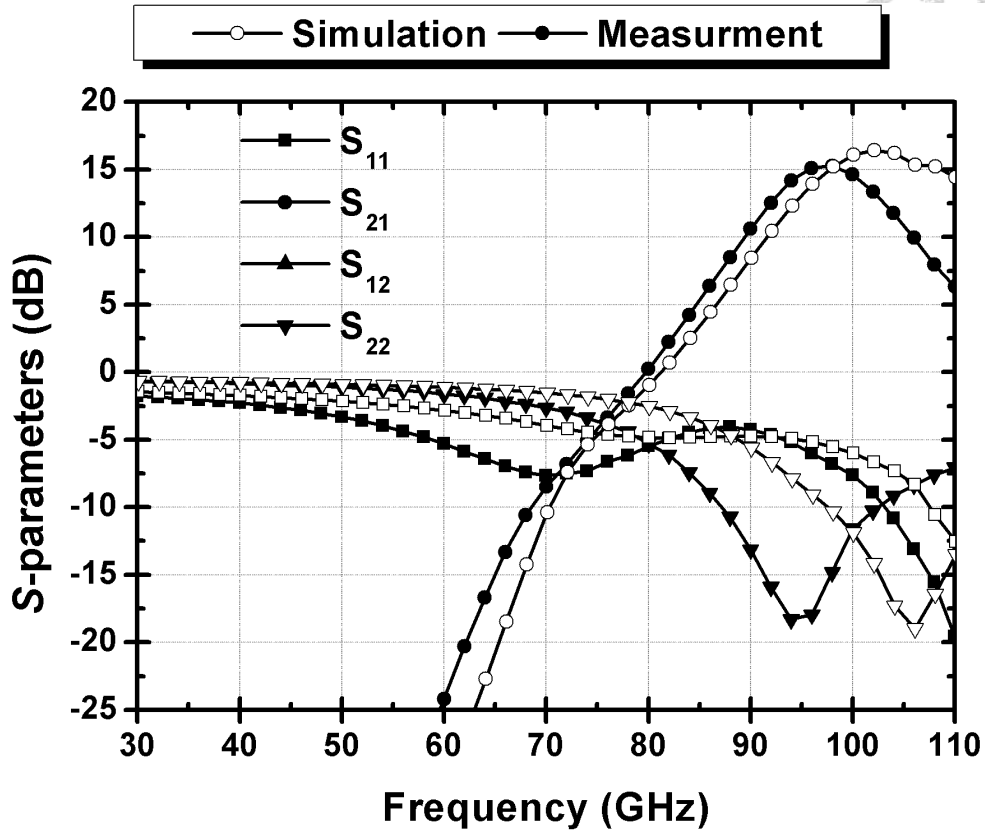

Fig. 4.73. Measured and simulated *S*-parameters of the modified PA in the second tape-out.

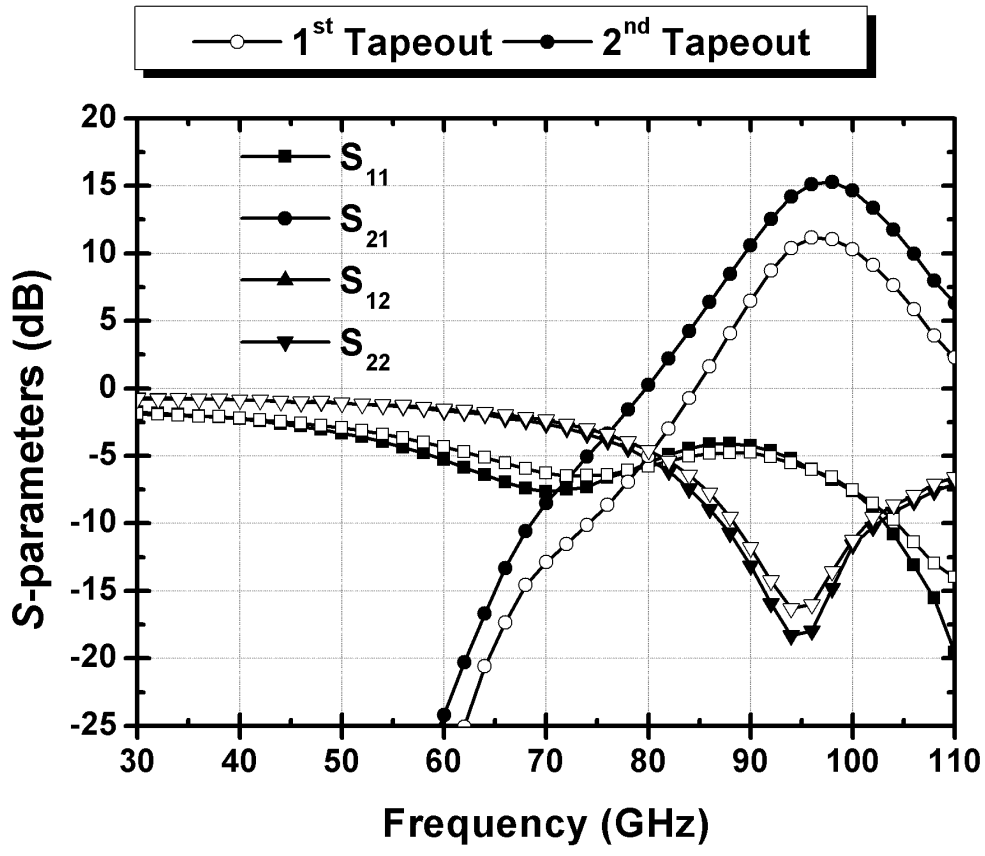

Fig. 4.74. Measured *S*-parameters of the modified and original PA in the two tape-outs.

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Since the center frequency in terms of peak gain has shifted to 98-GHz from the small-signal measurement results, large-signal measurements are performed at around 98 GHz instead of 110 GHz. Fig. 4.75 to 4.80 shows the measured large-signal performances from 92 to 102 GHz. As can be seen, because of eliminating the common-mode instability, the modified PA shows typical class-A behavior without the rising gain phenomena at low P_{in} levels. Note that due to the output power limit of the measurement equipment, the P_{in} levels were only able to reach approximately to P_{sat} and PAE_{peak} at some frequencies. As shown in Fig. 4.75, the modified PA shows an OP_{1dB} of 8.2 dBm, P_{sat} of 11.2 dBm, PAE_{peak} of 4.2% at 98 GHz.

Fig. 4.81 shows the measured OP_{1dB} versus frequency of the modified PA. The PA shows OP_{1dB} above 5.7 dBm from 90 to 104 GHz with peak OP_{1dB} of 8.2 dBm at 98 GHz. As can be seen from Fig. 4.75 to 4.81, despite the elimination of the common-mode instability, large-signal measurement results of the modified PA still show disagreement and degradation compared to simulation. This indicates an inaccurate modeling at the output end, as will be discussed later.

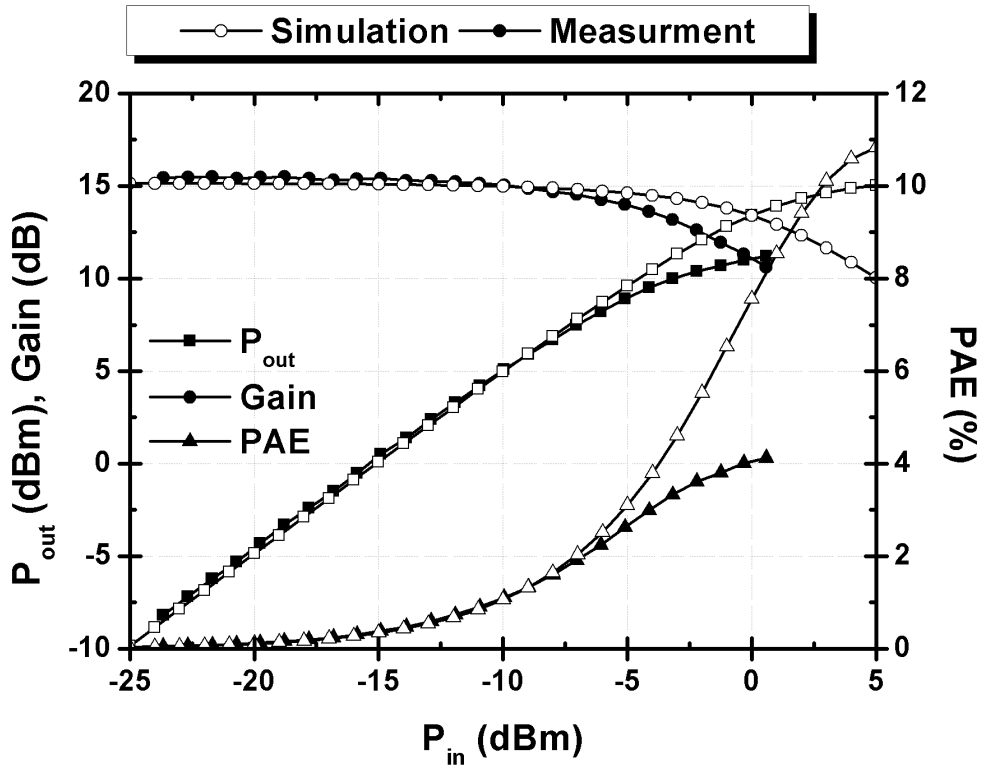

Fig. 4.75. Measured and simulated large-signal performance of the modified PA in the second tape-out at 98 GHz.

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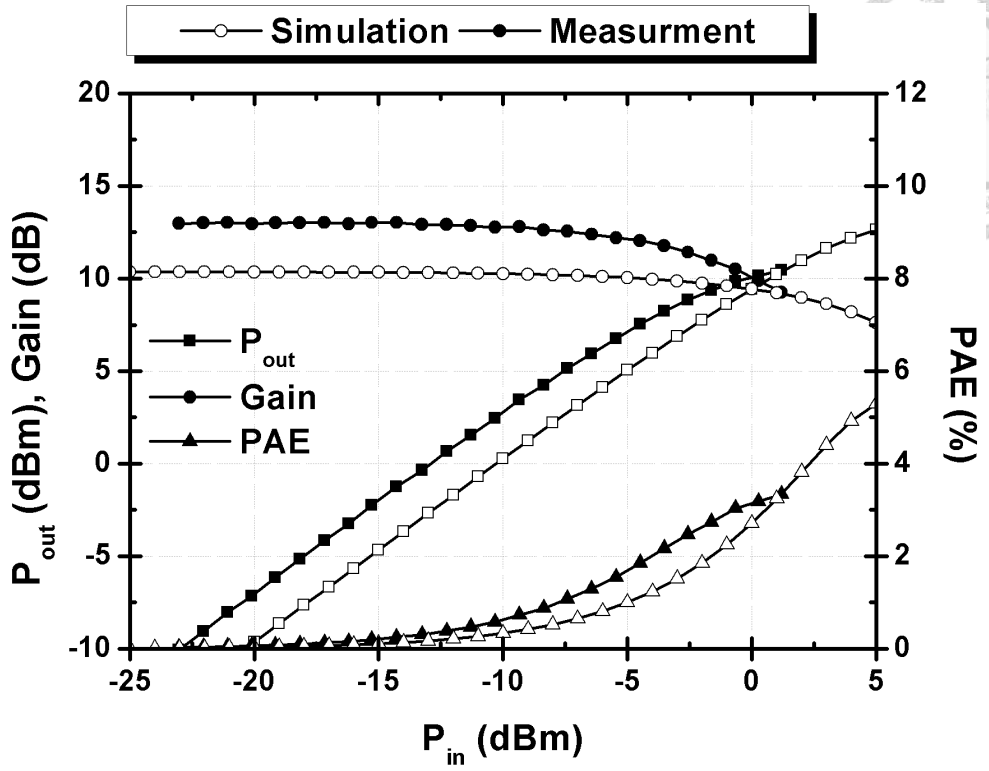

Fig. 4.76. Measured and simulated large-signal performance of the modified PA in the second tape-out at 92 GHz.

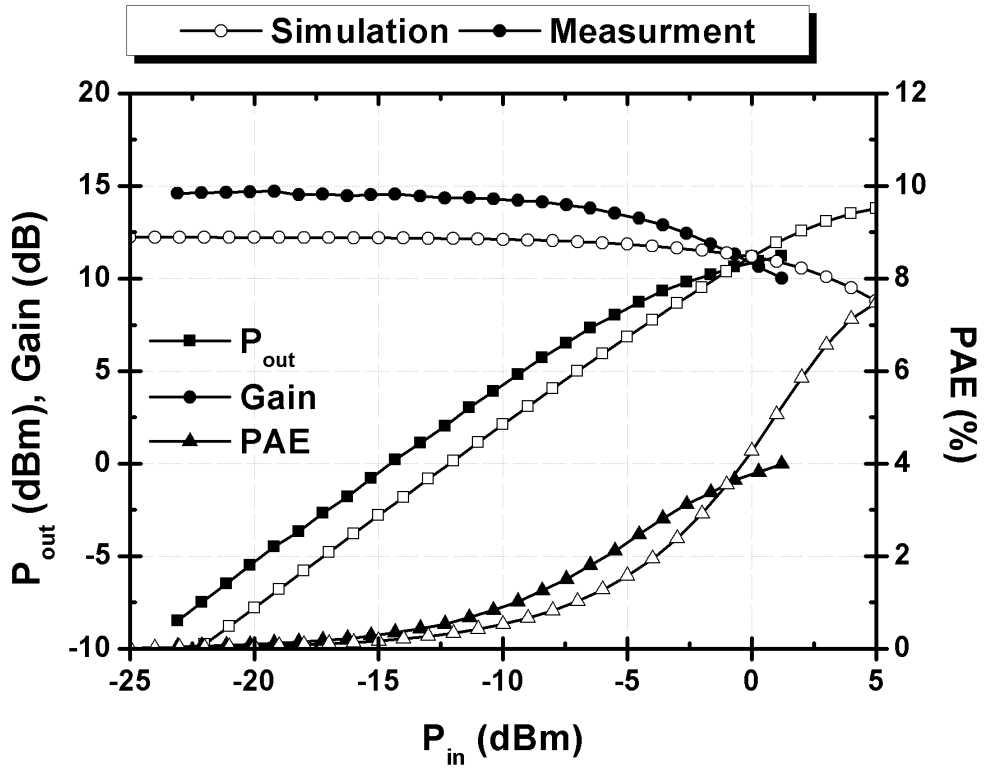

Fig. 4.77. Measured and simulated large-signal performance of the modified PA in the second tape-out at 94 GHz.

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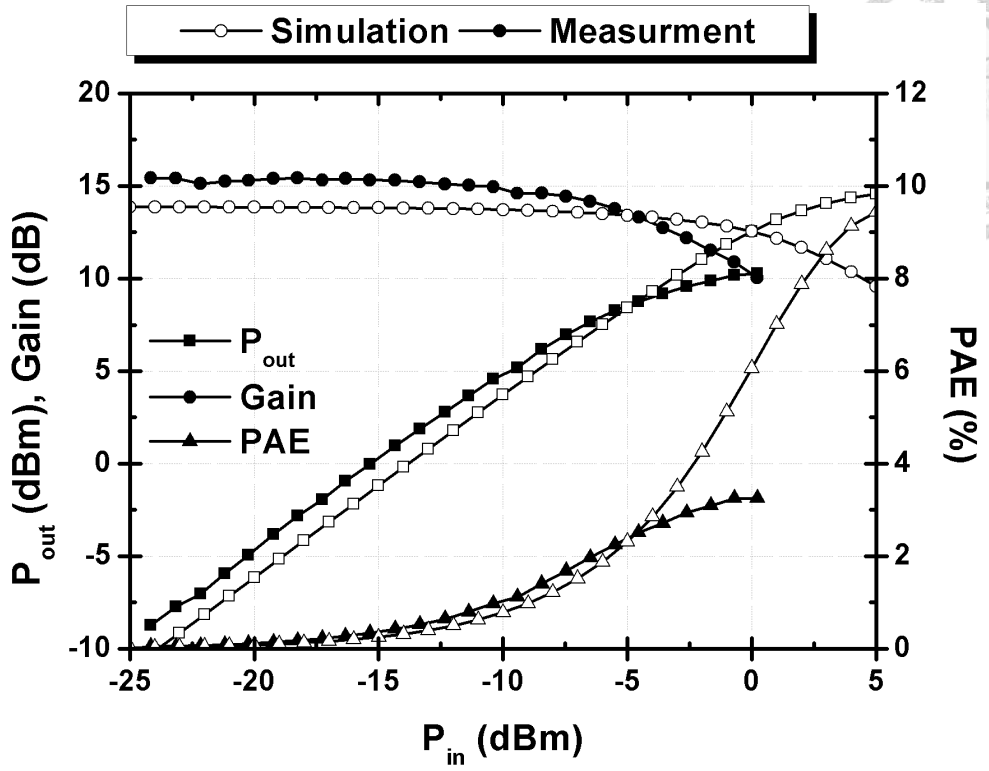

Fig. 4.78. Measured and simulated large-signal performance of the modified PA in the second tape-out at 96 GHz.

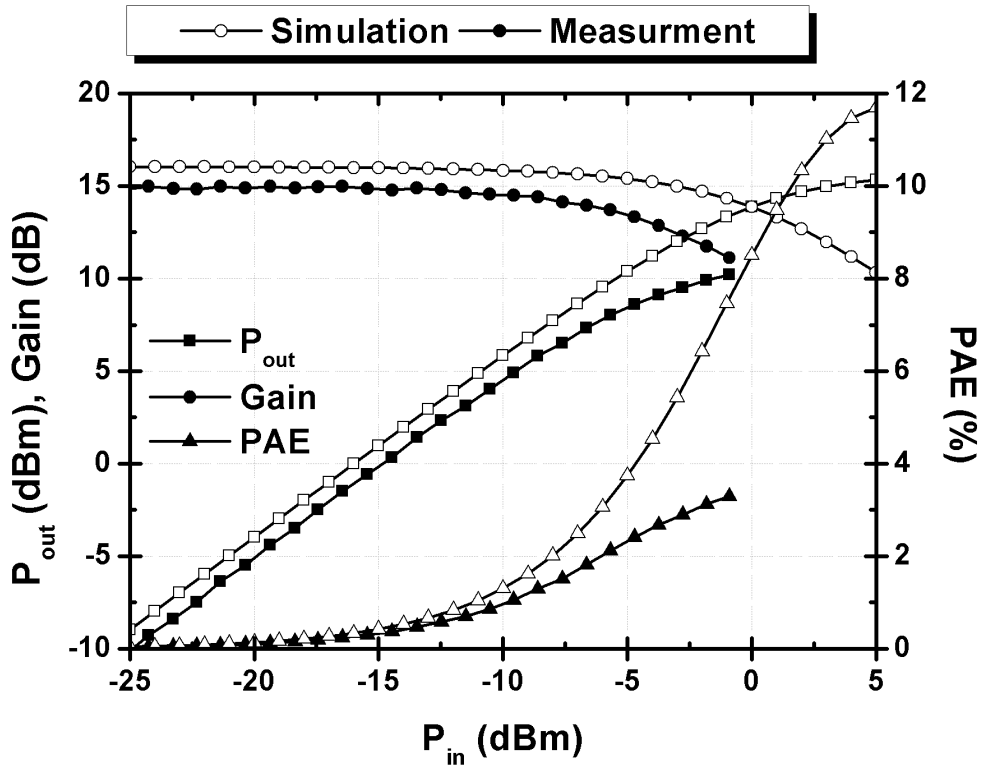

Fig. 4.79. Measured and simulated large-signal performance of the modified PA in the second tape-out at 100 GHz.

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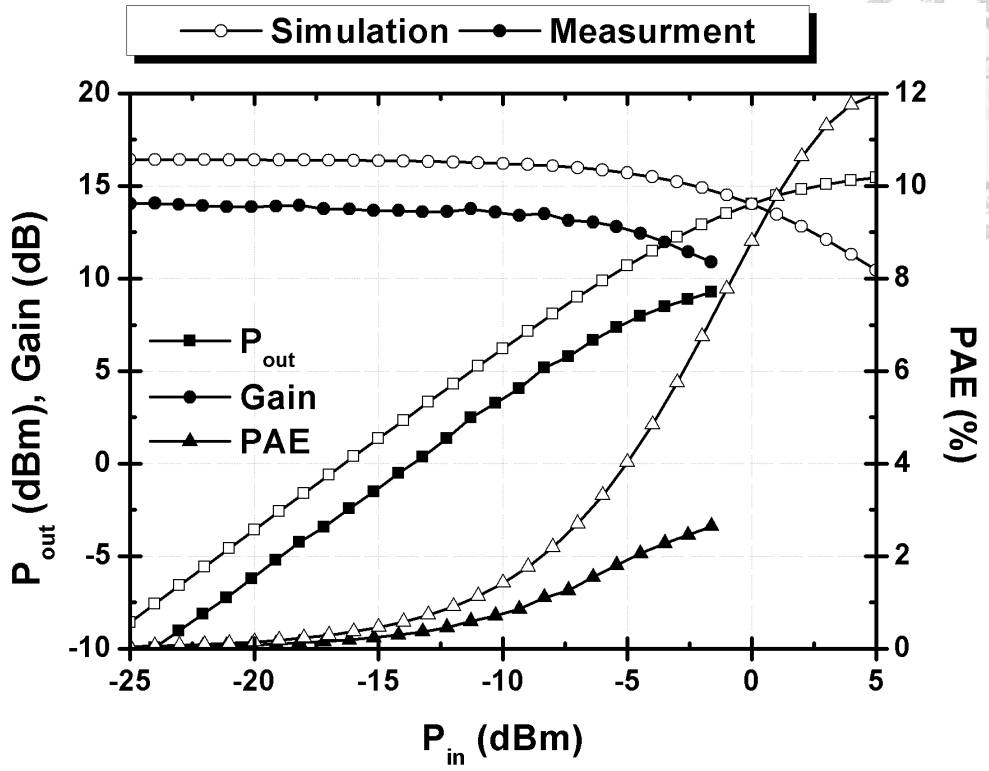

Fig. 4.80. Measured and simulated large-signal performance of the modified PA in the second tape-out at 102 GHz.

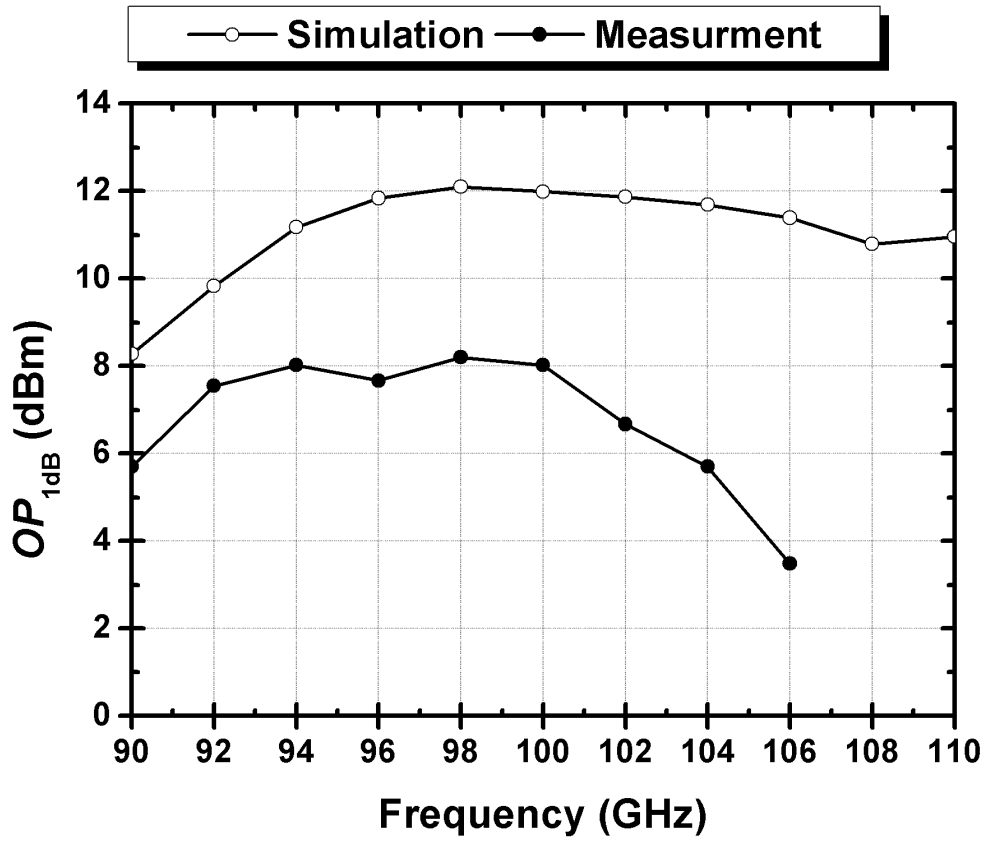

Fig. 4.81. Measured and simulated large-signal performances versus different frequencies of the modified PA in the second tape-out.

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Measurements of the transformer test circuits were all performed through on-wafer probing. An Agilent 8510C vector network analyzer was used for small-signal measurements up to 110 GHz. As mentioned in section 4.4.3, open-short de-embedding is adopted for the test circuit. Since de-embedding removes all the effects outside the DUT, the de-embedded measurement result is compared with the post-EM simulation result of the core transformer without the connecting micro-strip lines and GSG RF pads, as shown in Fig. 4.82. Fig. 4.83 and 4.84 show the measured and post-EM simulated magnitude (in dB) and phase of the *S*-parameters, respectively. Since the effect of parasitics becomes more prominent as the frequency increases, the difference between measurement and EM simulation in both magnitude and phase widens as the frequency increases. Nevertheless, the EM simulation still well models the measurement results up to 110-GHz, with magnitude difference less than 0.5 dB and phase difference less than 20° of the *S*-parameters at 110 GHz.

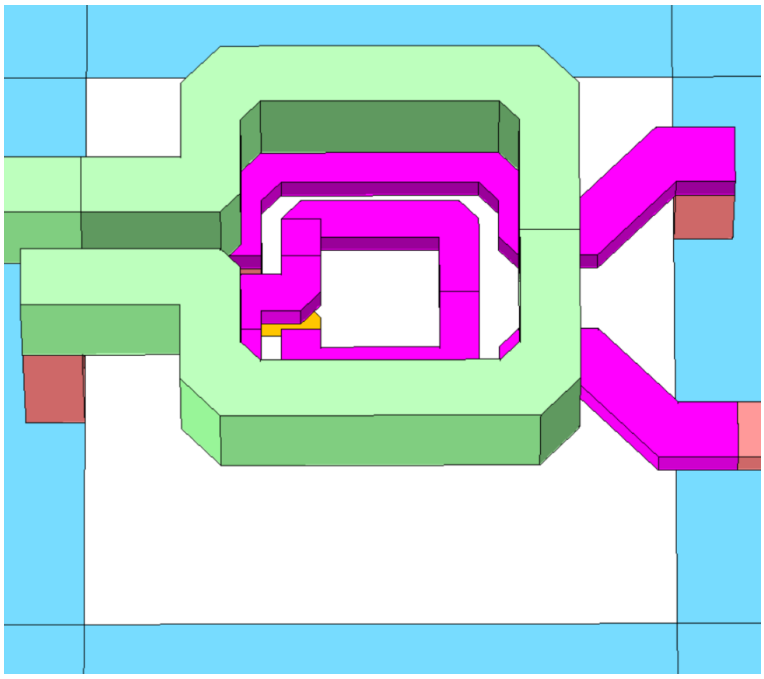

Fig. 4.82. 3-D rendering of the transformer test circuit (DUT only) used for EM simulation.

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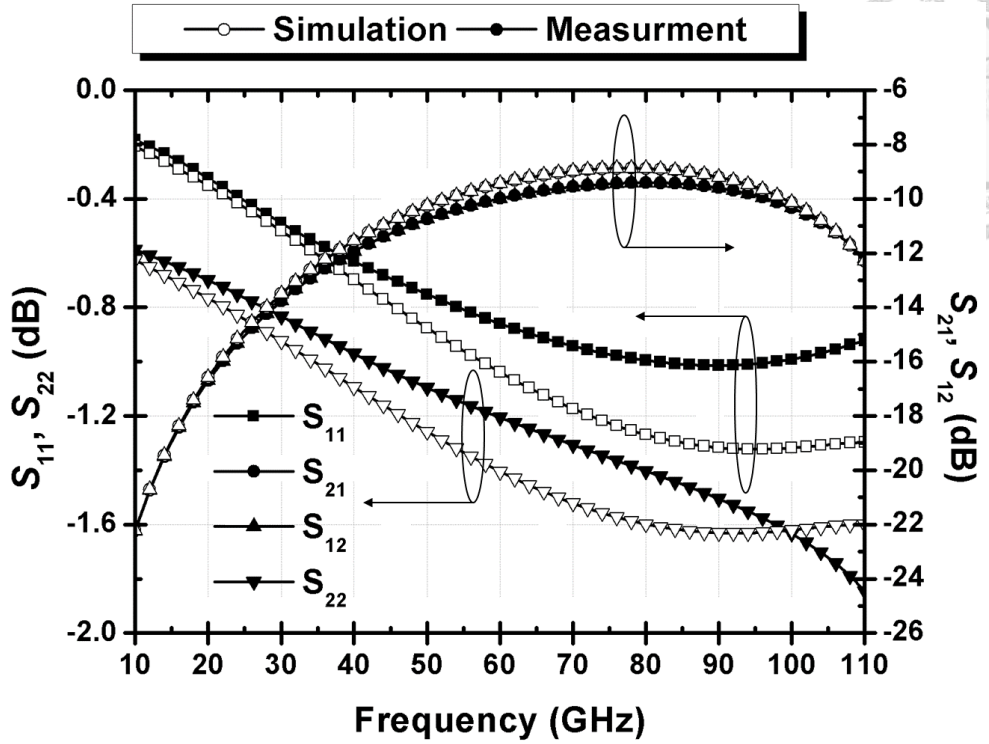

Fig. 4.83. Measured and simulated magnitude (in dB) of the *S*-parameters of the transformer test circuit.

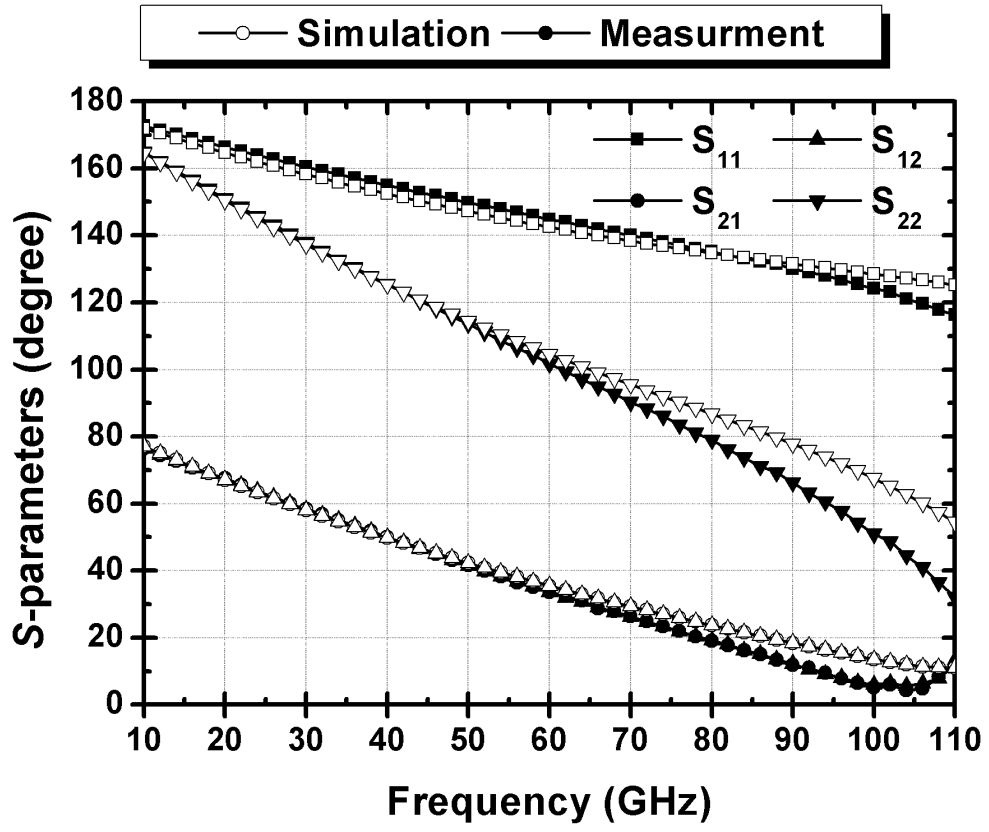

Fig. 4.84. Measured and simulated phase of the *S*-parameters of the transformer test circuit.

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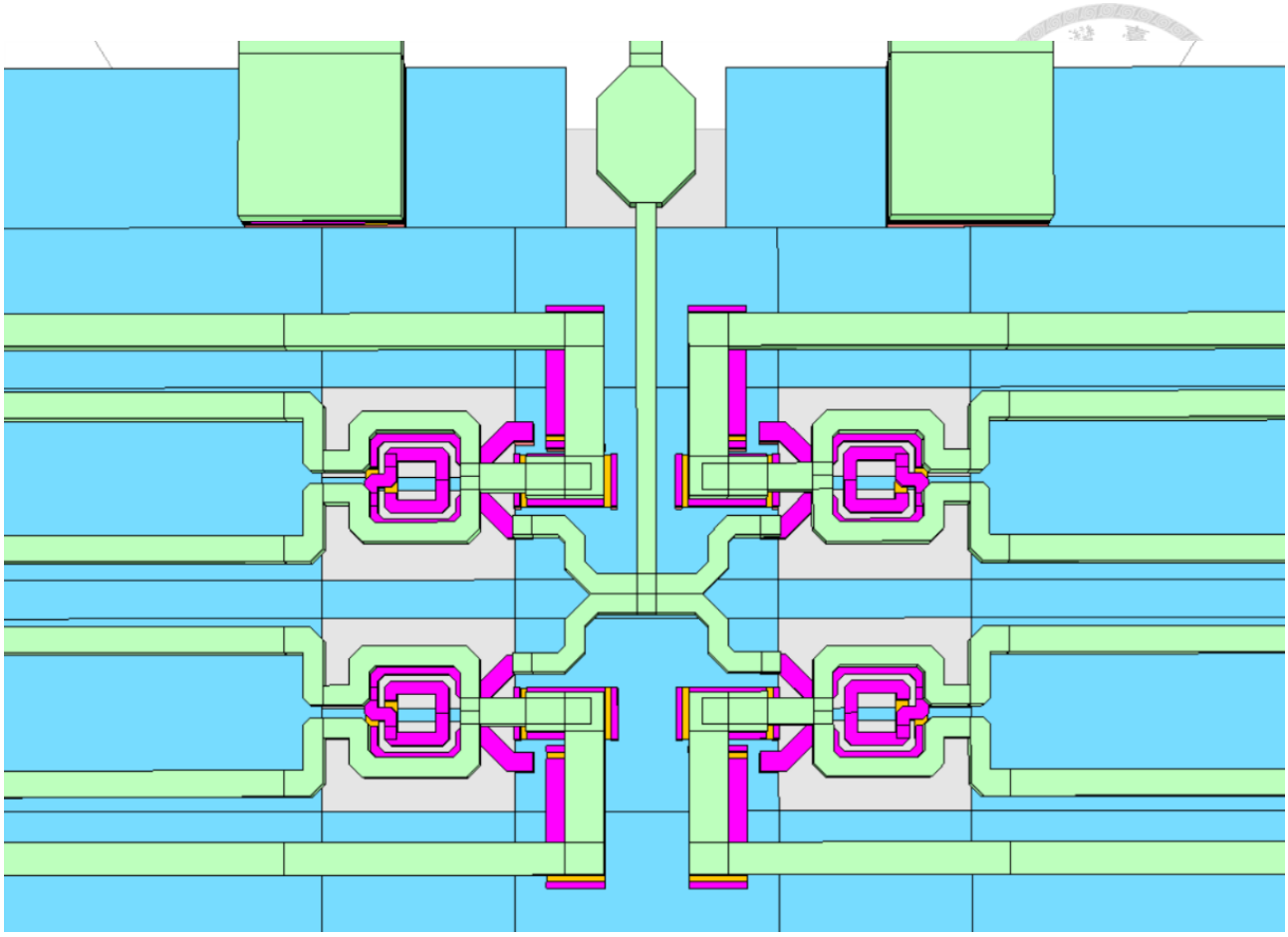

Fig. 4.85. 3-D rendering of the output transformer-based power combiner of the modified PA used for EM simulation.

As mentioned above, measurement of the modified PA in the second tape-out shows a successful elimination of the common-mode instability at 47 GHz. Nevertheless, the measurement and simulation results still disagree in both small- and large-signal performances. Measured small-signal performance shows shifts towards lower frequencies in S_{21} and S_{22} compared with simulation, but agrees well in S_{11}. Measured large-signal performances at different frequencies all show disagreement and degradation in OP_{1dB}, P_{sat}, and PAE_{peak} compared with simulation. These all indicate an inaccurate modeling at the output end. However, the agreement between measured and simulated S_{11} of the modified PA, and the results from the transformer test circuit both verify the modeling accuracy of the EM simulation.

Fig. 4.85 shows the 3-D rendering of the output transformer-based power combiner used for EM (Sonnet) simulation. The ground (metal-1) plane underneath each transformer is removed to

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prevent undesired coupling of field. With the compact layout of the four-way combiner, this results in an incomplete ground plane at the output end. The box wall represent ideal ground during EM simulation. With the perimeters of the ground plane attached to the box wall, the ideal ground in EM simulation is not fully representative of the real world condition. The difference is amplified by the high frequency of W-band and the incomplete ground plane at the output end. This result in disagreement between measurement and simulation results at the output end, i.e., small-signal S_{22} and large-signal performances.

4.5 Summary

In this chapter, a W-band PA with transformer-based impedance matching and power combining designed and realized in 65-nm CMOS process is presented. To achieve the targeted output power performance under the process limited supply voltage, four-way power combining is adopted at the output. With the radial-symmetric transformer-based power combiner, the insertion loss, layout footprint, and imbalance between combining paths can be minimized.

The proposed W-band PA consists of three stages with total gate-periphery ratio of 1:2:4. By having single-to-differential transformers at the input and differential-to-single transformers at the output, the PA operates in differential mode internally. Neutralization technique can therefore be implemented via cross-coupled capacitors in order to improve the device gain and stability in differential mode. All impedance matching and power-combining/splitting are performed via transformers, which are carefully designed to have the self-resonant frequencies above the working frequencies at W-band.

Measurement results of the PA show disagreement with simulation in both small- and large-signal performances. Undesired oscillations at around 47 GHz were observed during measurement. Through bias-line stability analyses, instabilities at around 47 GHz are also discovered in simulation. Further analyses show that the instability lies in common mode.

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Modifications to the transformers are proposed to eliminate the common-mode instabilities, without altering the matching conditions in differential mode. Metal strips added to the ground plane underneath the transformers effectively change the impedance in common mode, and in turn eliminate the instabilities. On the other hand, the impedance in differential mode is unchanged, and therefore the overall PA performance remain the same. The PA design with the proposed modifications was realized in the second tape-out. In order to verify the modeling accuracy of EM simulations, test circuits for the transformer used within the PA were also designed and realized in the second tape-out.

Measurement results of the modified PA in the second tape-out show a successful elimination of the undesired oscillation. This result in a 4dB gain increase compared with the original PA. However, the measurement results still show disagreement with simulation in both small- and large-signal performances. The small-signal measurement results show disagreement with simulation in S_{21} and S_{22}, but agrees well in S_{11}. The large-signal measurement results show significant drops in P_{sat}, OP_{1dB}, and PAE at various frequencies compared with simulation. These all indicate inaccurate modeling in simulation at the output of the PA.

Measurement results of the transformer test circuit shows agreement with simulation up to 110-GHz. With the agreement in small-signal S_{11} of the PA between measurement and simulation, this verifies the modeling accuracy of the EM simulation. However, the compact layout of the output transformer-based power combiner results in an incomplete ground plane at the output end. This result in inaccurate modeling from the EM simulation at the output, and therefore disagreement between measurement and simulation in small-signal S_{22} and large-signal performances. Table 4.3 shows previously proposed W-band PA designs realized in 65-nm CMOS process. Despite the aforementioned issue, the proposed PA shows decent gain performance of 15.3dB at 98-GHz with a 12-GHz 3dB bandwidth. Large-signal performances is only comparable to previous works, with an OP_{1dB} of 8.2 dBm, P_{sat} of 11.2 dBm, PAE_{peak} of 4.2% at 98 GHz, and OP_{1dB} above 5.7 dBm across

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90 to 104 GHz with peak OP_{1dB} of 8.2 dBm at 98 GHz.

Table 4.3. Previously Reported W-band PA Designs in CMOS processes.

Ref.	Technology	Frequency (GHz)	3dB BW (GHz)	Gain (dB)	P_{sat} (dBm)	OP_{1dB} (dBm)	PAE_{peak} (%)	Area (mm^2)
[39]	65-nm CMOS	108	16	14.1	14.8	11.6	9.4	0.322
[40]	65-nm CMOS	109	13	17.8	9.6	8.3	10.4	0.136
[41]	65-nm CMOS	94	21	13	14	10.3	4	0.24
[42]	65-nm CMOS	100	21	13	10	6	7.3	0.33
[43]	65-nm CMOS	100	17	13.4	13.8	11.2	9.4	0.205
[44]	65-nm CMOS	90	27	12	14.8	12.5	8.7	0.28
[45]	65-nm CMOS	90	25	12.5	18	16.8	9	0.82
[46]	65-nm CMOS	140	30	15	13.2	9.9	14.6	0.38
		150		16	12.2	7.6	12.1	
[47]	90-nm CMOS	100	18	15	10	6	5	0.4
This work	65-nm CMOS	98	12	15.3	11.2	8.2	4.2	0.419

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Chapter 5 Conclusions

Firstly, a Q-band LNA for 5G receiver applications is designed and realized in 0.15-μm pHEMT GaAs process. The proposed LNA consists of three common-source stages. Source degeneration technique using transmission lines (TL_{deg}) is adopted at the first stage for its ability of narrowing the difference between input impedances for optimal noise (Z_{opt}) and gain ($Z_{in,conj}$) performances. Thus, compromises in gain and input return loss can be minimized when input is matched for optimal noise performance. RC-feedback technique is adopted at the latter two stages for the wideband performance it provides. π-type matching networks are used at the third stage for lower Q-factor during impedance transfer for a wideband performance. Correction to the simulation setups for CPW-configuration devices with TL_{deg}'s is proposed. The 3-dB bandwidth is 15.3 GHz from 24.7 to 40.0 GHz with average gain of 22.2 dB. The gain is 21.5 dB at 38 GHz, and has flatness of 22.3 ± 1 dB from 25.7 to 37.6 GHz. The input and output return losses are above 15dB from 37.2 to 40.4 GHz and 34.4 to 39.4 GHz, respectively. The noise figure is below 3dB from 27.9 to 40.0 GHz, and has average of 2.6 dB from 26 to 40 GHz.

Secondly, a 60-GHz OOK modulator for short range wireless communications is designed and realized in 90-nm CMOS. By combining the functions of modulation and output amplification in a single circuit, a transmitter of lower complexity and higher efficiency can be achieved. The proposed modulator is based on a cascode circuit, in which modulation is performed by switching the common-gate device on/off. A cascode-based transformer-feedback technique is proposed for improvements in output power, gain performances at on-state, and isolation performance at off-state. For modulation, an inductor with a shunt capacitor is adopted for the baseband data input to provide isolation to the RF (carrier) frequencies instead of a large resistor. This effectively lowers the time-constant (τ) seen by the baseband data signal, and enables the modulator to achieve a maximum 10-Gb/s data rate. With the proposed transformer feedback technique, the modulator achieves an OP_{1dB} of 7.0 dBm, gain of 10.2 dB, and on-off isolation of 45.4 dB at 60 GHz. For

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OOK modulation, data rates of up to 10 Gb/s has been measured. The modulator has compact layout footprint measured at 471 x 519 μm^2 with RF and DC pads included.

Finally, a W-band PA is designed and realized in 65-nm CMOS. Four-way power combining is adopted at the output. With the radial-symmetric transformer-based power combiner, the insertion loss, layout footprint, and imbalance between combining paths can be minimized. The proposed PA consists of three stages with total gate-periphery ratio of 1:2:4.

Common-mode instability at around 47 GHz were observed during measurement. Through bias-line and common-mode stability analyses, instabilities at around 47 GHz are also discovered in simulation. Modifications to the transformers are proposed to eliminate the common-mode instabilities, without altering the matching conditions in differential mode. The PA design with the proposed modifications was realized in the second tape-out. In order to verify the modeling accuracy of EM simulations, test circuits for the transformer used within the PA were also designed and realized in the second tape-out.

The modified PA shows successful elimination of the undesired oscillation, and a 4-dB gain increase compared with the original PA. However, the measurement results still show disagreement with simulation in both small- and large-signal performances. Measurement results of the transformer test circuit shows agreement with simulation up to 110 GHz. With the agreement in small-signal S_{11} of the PA between measurement and simulation, this verifies the modeling accuracy of the EM simulation. Compact layout of the output transformer-based power combiner results in an incomplete ground plane at the output end. This result in inaccurate modeling from the EM simulation at the output, and disagreement between measurement and simulation in small-signal S_{22} and large-signal performances. Despite the aforementioned issue, the proposed PA shows decent gain performance of 15.3dB at 98 GHz with a 12 GHz 3-dB bandwidth. Large-signal performances is only comparable to previous works, with an OP_{1dB} of 8.2 dBm, P_{sat} of 11.2 dBm, PAE_{peak} of 4.2% at 98 GHz, and OP_{1dB} above 5.7 dBm from 90 to 104 GHz with peak OP_{1dB} of 8.2 dBm at 98 GHz.

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