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利用動態相位控制機制之快速鎖定全數位鎖相迴路

An All-Digital Phase-Locked Loop with Dynamic Phase Control for Fast Locking

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本論文係 莊昀蓁君（R97943006）在國立臺灣大學電子工程研究所 ICS 組完成之碩士學位論文，於民國 100 年 5 月 5 日承下列考試委員審查通過及口試及格，特此證明

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（指導教授）

系主任、所長

An All-Digital Phase-Locked Loop with Dynamic Phase Control for Fast Locking

By

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THESIS

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致謝

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To My Dear Family

謹獻給我的家人

摘要

本篇論文實現了一個利用動態時間窗來控制相位資訊的全數位鎖相迴路，實作上提出雙模式雙路徑的操作來達成快速鎖定與低時脈抖動的特性。補償相位的路徑利用動態改變除數的方式，而頻率的修正則由前饋路徑直接調變數位振盪器。除此之外，雙模式的設定使得迴路在鎖定後能切換至窄頻寬且妥善設計其阻尼係數。由於在鎖定過程中，鎖相迴路維持在一個較小的相位誤差，因此鎖定時間可有效地縮短；可程式化的數位濾波器設計也使得鎖定後的效能能夠獲得控制。在電路層面上，使用不對稱延遲單元減少在時序數位轉換器的功耗與面積，後端具有錯誤校正的編碼器可用來減輕時序放大電路的規格要求；數位振盪器的部分，則是選擇具有較細解析度與較佳相位雜訊之電感電容架構。因此，提出之系統架構可實現一低時脈抖動與快速鎖定的全數位鎖相迴路。

使用台積電 0.18 微米製程設計一應用於 2.4 GHz 頻帶之全數位頻率合成器。在 5-25 MHz 的跳頻距離下，鎖定時間皆小於 5 μs；中心頻率為 2.49 GHz 時，量測到的時脈抖動為 1.93 ps，相位雜訊於 100 kHz 與 1 MHz 頻率偏移下分別為-79.6 dBc/Hz 和-112.7 dBc/Hz，參考頻率突波於 5 MHz 頻率偏移下低於-50 dBc。整個鎖相迴路操作在 1.8 V 共花費 10.35 mA 電流，晶片面積為 1.8 mm^2。

Abstract

This thesis presents an all-digital phase-locked loop (ADPLL) featuring a dynamic phase compensation by a set of the auxiliary timing window. When frequency hopping occurs, the compensation scheme is implemented in both frequency and phase domain for fast settling. The detected phase error is continuously sent to the divider chain which changes the divider ratio, and directly modulates the frequency of the digital-controlled oscillator (DCO) through a digital feed-forward path at the same time. The proposed method allows the ADPLL maintaining a small phase error throughout the frequency acquisition process; thereby reducing setting time. Because of the switching mode operation, the mentioned techniques can solve the trade-off between low jitter and fast lock. An uneven-step time-to-digital converter (TDC) with an error correction encoder is implemented to relax circuit design and save power consumption. The DCO adopts the LC-based architecture because it has the finer tuning gain and better phase noise performance. The proposed ADPLL is implemented to optimize timing jitter and lock time.

The proposed technique is incorporated in the design of a 2.4 GHz ADPLL and fabricated in the TSMC 0.18 μm CMOS technology. With less than 5 μs lock time in hopping frequency from 5 MHz to 25 MHz, the measured rms jitter from a 2.49 GHz carrier is about 1.93 ps. The phase noise at 100 kHz and 1 MHz is -79.6 dBc/Hz and -112.7 dBc/Hz, respectively. The reference spur at 5 MHz offset is under -50 dBc. The whole circuit dissipates 10.35 mA from a 1.8 V supply and the chip area is 1.8 mm^2.

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Chapter 1
Introduction

1.1 Motivation

Frequency synthesizers are the key building blocks for most of modern electronics and communication systems, including radio receivers, mobile telephones, and satellite receivers. A typical wireless communication system incorporates a RF transceiver to convert a RF signal down to a base-band signal, or convert a base-band signal up to a RF signal. Therefore, a local oscillator (LO) is required in most RF transceivers. For different communication channels, the frequency of LO signal is demanded to be programmable, which is usually generated by phase-locked loop (PLL) based frequency synthesizer.

With the explosive growth of the wireless communication, the need has arisen to reduce cost and power consumption of mobile devices. The demand for high-level integration and maximal flexibility can be best achieved using a digital or digital-intensive approach. Considering the circuit design of system-on-chip (SoC) in the future deep sub-micron CMOS technologies, the integration of high performance analog synthesizers on the same silicon together with massive and high speed digital cores will become more and more challenging. In this sense, the robustness of the synthesizers against noise from the supplies or from the substrate will be a major issue. Therefore, the emerging of all-digital phase-locked loop (ADPLL) architectures is an important example for wireless applications [1]-[3].

The settling time of the frequency synthesizer is an important performance. For most time-division multiple access (TDMA) communication systems, the synthesizers have to switch to another frequency in a restricted time slot, otherwise it may degrade the data rate. On the other hand, the quality of the wireless communication is greatly affected by the performance of the frequency synthesizer, such as phase noise, spur performance, power consumption, and fabricated cost. In general, a small loop bandwidth PLL is needed to suppress the timing jitter, but it leads to a slow settling speed at the same time. For a conventional structure, it may fail to satisfy stringent communication specifications even if ADPLLs are a new trend.

The 2.4 GHz industrial, scientific and medical (ISM) band is widely used by various wireless systems, such as wireless local area network (WLAN), Bluetooth and Zigbee. In this thesis, a digital LC-PLL using dynamic phase control for 2.4 GHz ISM band application is presented. The goal is to deal with the trade-offs between settling time and jitter performance.

1.2 Thesis Overview

This thesis is composed of six chapters. In Chapter 2, the fundamental introduction in analog PLLs and ADPLLs will be shortly addressed. Furthermore, the building blocks and modeling of basic ADPLLs are illustrated. In Chapter 3, the proposed ADPLL is presented for fast locking without damaging its jitter performance. In this chapter, the proposed techniques are introduced and analyzed with the loop linear model and design considerations. Chapter 4 shows circuit implementations of the important building blocks. Chapter 5 shows measurement results of the proposed ADPLL as well as the comparison of conventional ADPLLs and this work. Finally, the conclusions and future work of this thesis are described in Chapter 6.

Chapter 2
Introduction to All-Digital Phase-Locked Loops (ADPLLs)

2.1 The Basics of Analog Phase-Locked Loop (PLL)

Based on the operation principle of a simple PLL [4], the charge pump PLL (CP PLL) is developed as shown in Fig. 2-1. It is the most popular way to synthesize the frequency in wireless communication. F_{REF} is input reference frequency and F_{FB} is the output frequency of voltage-controlled oscillator (VCO) divided by frequency divider, N. The phases of F_{REF} and F_{FB} are compared by phase/frequency detector (PFD) which estimates the time difference between their closest edges, and then the CP charge/discharge the low pass filter (LPF) according to the UP/DN pulse. The current pulse generated by CP is converted into the control voltage, V_{CTRL}, through the LPF. The main task of LPF is to suppress the glitches introduced by CP in every phase comparison. The loop automatically adjusts the VCO control voltage by the feedback mechanism. After the loop is locked, the output frequency is the multiple frequency of F_{REF}, which is

$$F_{OUT} = N \times F_{FB} = N \times F_{REF} . \quad (2\text{-}1)$$

As the nano-meter CMOS technology advances, a highly integrated system is required. However, the implementation of traditional RF and analog circuits is more complicated in the deep-submicron CMOS. Analog PLLs may encounter capacitor leakage, current mismatch, and limited dynamic range under low supply voltage, leading to higher noise floor and spurious tone. The design of a high performance

analog synthesizer becomes a big challenge in the future. Consequently, the digital-intensive approach can relax this situation and allow more digital switching noise to be coupled into the high precision analog section through the power supply network and the low resistance substrate.

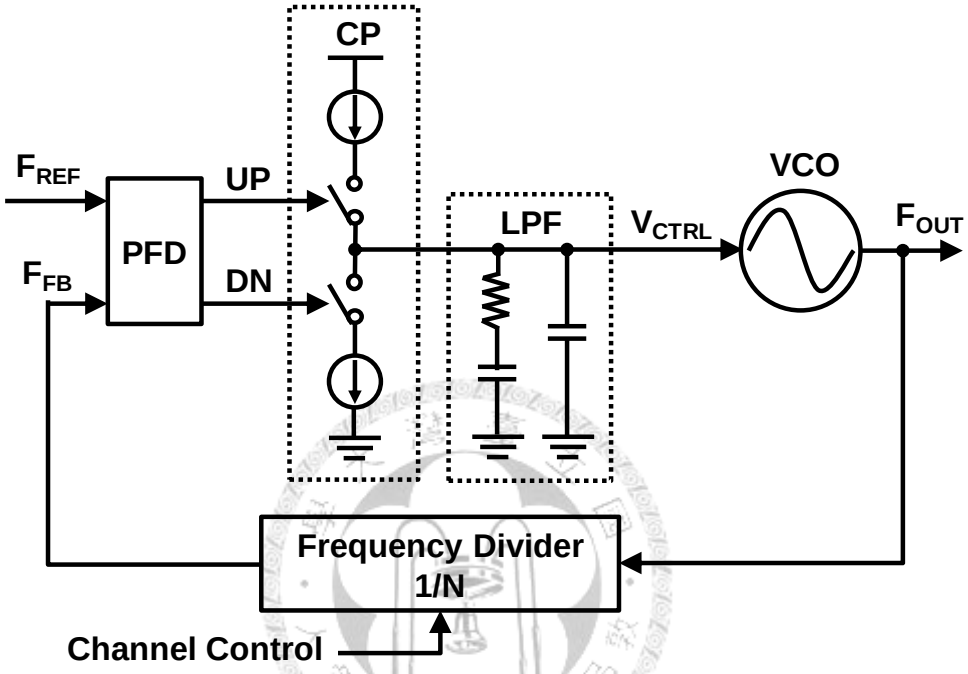


Fig. 2-1 The block diagram of a typical CP PLL.

There are many advantages in digital solution compared to analog one. The digital approach improves time-to-market due to reusable modules and portable process. The lack of on-chip passive components and analog functional blocks reduces sensitivity to process-voltage-temperature (PVT) variations. It brings major benefits of solving the design issues including current mismatch, capacitor leakage and shrunk dynamic range in analog implementation. Area occupation, possibly power consumption will be decreased. The production test of the synthesizer can be done using straightforward digital methods, like built-in self-test (BIST). The control signal in systematical calibration block can also be recorded and performed by an auxiliary memory since the digital nature of ADPLL. However, the digital approach of the frequency synthesizers

will face the problems about finite resolution and quantization error. In the next section, some of the state of the art ADPLLs will be illustrated.

2.2 State of the Art ADPLLs

In the 1970's, there are several papers about digital frequency synthesizers [5]-[7]. However, because of the lack of a practical low jitter digital-controlled oscillator (DCO), the achievable performance in digital PLLs were far away from those of the analog loops. In the 1980's, the development of the CP PLL with type-IV PFD, removed some limitations of prior analog PLLs based on the multiplier phase detector. This fact finally discarded the hopes of digital PLLs to catch up with the performances of analog ones. For all 80's and 90's high performance frequency synthesizers, they were almost implemented by the analog architecture. However, the attention of recent researches has moved into digital loops due to advanced processes. The current researches are studied on ADPLL which is a semi-analog system but all input/output control of building blocks defined as digital level. A digital loop has been proposed and implemented in [8]. The lack of a low jitter DCO has been overcome by connecting a digital-to-analog converter between the digital filter and a conventional analog VCO. The work [9] presents the architecture based on ΔΣ noise shaping which could achieve better performances in a discrete-time operation.

There are two alternatives of ADPLLs according to the existence of the divider block. First, the phase domain ADPLL without divider was reported in [10], which allows its loop control circuit to be implemented in a fully digital manner. Its block diagram is shown in Fig. 2-2 (a). The phase error is resolved by subtracting the integral and fractional timing information from reference phase. Due to the edge counting nature, the quantization resolution is limited by the DCO clock period. For wireless applications, a finer resolution is required. Therefore, a time-to-digital converter (TDC)

is achieved for the purpose of the fractional error correction. The reference phase is obtained by accumulating the frequency command word (FCW); the integral part is determined by counting the number of DCO rising edge while the fractional part measures the time difference between the reference clock and the next rising edge of the DCO clock. Then, the calculated amount is filtered by a digital loop filter (DLF). Finally, the output of DLF is fed to DCO to adjust the output frequency. Besides, it is important to deal with the accuracy of the DCO period normalization factor in TDC.

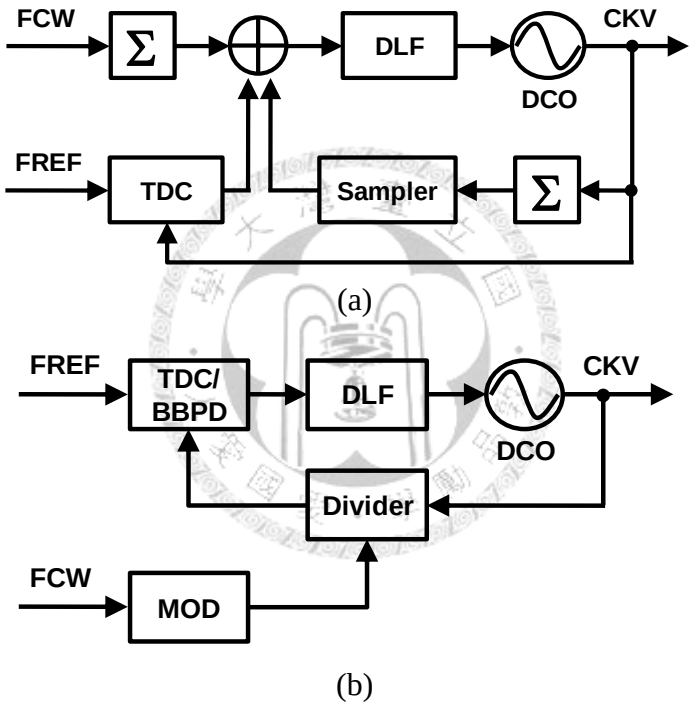


Fig. 2-2 Two alternatives of ADPLLs: (a) the ADPLL without divider, and (b) the ADPLL with divider.

Another ADPLL structure with divider is illustrated in Fig. 2-2 (b). According to the method of the phase sensing, the ADPLL with divider can be roughly classified into two categories. They are bang-bang based ADPLL for binary phase detection [11] and TDC based ADPLL for linear phase detection [12], respectively. These frames look understandable because the building blocks are converted from traditional analog PLLs. The phase error is digitized by the quantization circuit, such as bang-bang phase

detector (BBPD) or TDC. This digital output code is proportional to the phase error between the reference clock and feedback clock. After processed by DLF, the filtered value is sent to DCO monitoring the output drift in a negative feedback manner. The bang-bang based ADPLL only provides tri-state output which cannot reflect the magnitude of phase error. For this reason, the bandwidth and ability of the frequency tracking in TDC based ADPLL are better than bang-bang based ADPLL, but the TDC design is more sensitive to environment variation.

2.3 The Basics of ADPLL Building Blocks and Modeling

The major difference between analog PLL and ADPLL is the controlled interconnection. All of the control signals in analog PLL are processed in analog voltage and current domains. In an ADPLL, the control signals are processed by digital code. Because of the discrete-time operations and quantization effect, some modification and approximation are required to model an ADPLL in order to make the linear analysis method available [13].

The essential components of a TDC based ADPLL includes PFD, TDC, DLF, DCO and divider. The phase-domain model of a typical ADPLL is shown in Fig. 2-3. In the next section, the models of the building blocks are introduced step by step. Once the linear model is built, the stability and dynamic of the loop can be analyzed.

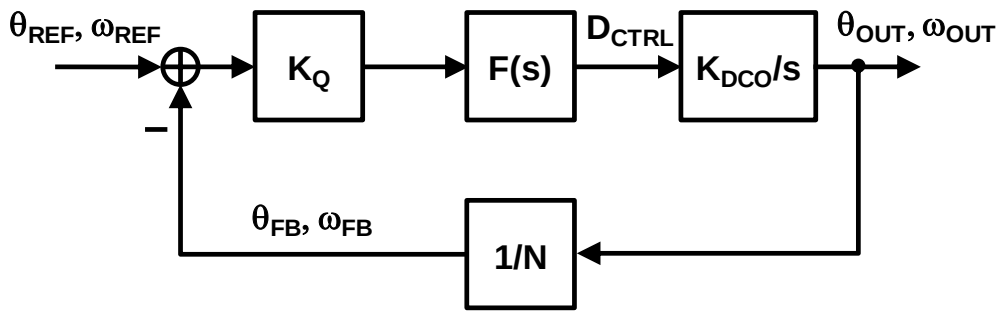
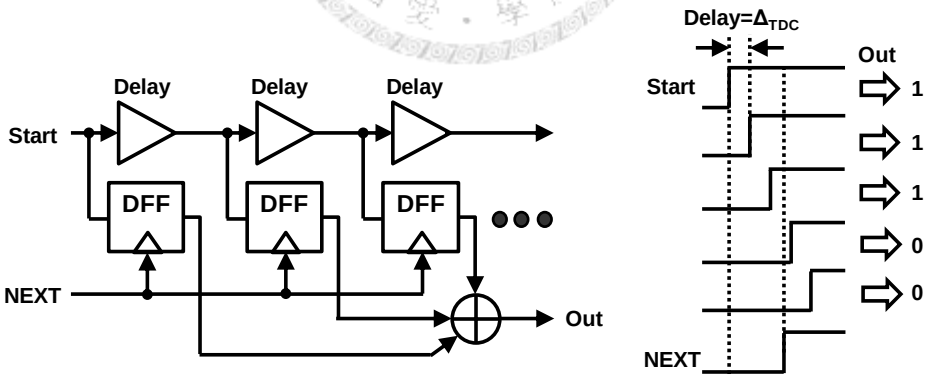


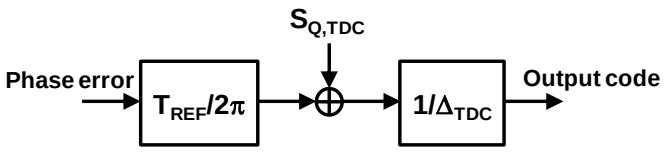
Fig. 2-3 The linear model of a typical ADPLL in phase domain.

2.3.1 Phase/Frequency Detector (PFD) and Time-to-Digital Converter (TDC)

The main purpose of a PFD is to detect the phase error between θ_{REF} and θ_{FB}. The phase-domain model can be simply expressed by a subtractor in Fig. 2-3. The phase error is distinguished by the timing difference of UP/DN pulse and then sent to the quantizer. Followed by a PFD, the TDC based quantizer is utilized. The conceptual structure and waveform is shown in Fig. 2-4 (a). A TDC, comprised of a chain of delay elements and the sum operator, counts the cell numbers of inverter delays in logic "high". The output from each inverter is an input to a register, which is clocked with the rising edge of a stop signal, *NEXT*. A thermometer code is then generated at the register output corresponding to the measurement interval between *Start* and *NEXT*. Finally, the equivalent binary code sends into DLF. The resolution of TDC is derived from an inverter delay, Δ_{TDC}. If the phase difference is much larger than the TDC resolution, the input-output characteristic of PFD/TDC is similar to the transfer curve in the analog-to-digital converter (ADC).



(a)



(b)

Fig. 2-4 The analysis of a classical delay-chain TDC in (a) the conceptual brief, and (b) the linear model.

The phase difference is converted to time domain by PFD and TDC. The linear model of a TDC has been shown in Fig. 2-4 (b), and the building block can be modeled as a gain plus quantization noise. Accordingly, the transfer function is

$$K_Q = \frac{T_{REF}}{2\pi\Delta_{TDC}}. \tag{2-2}$$

There are several sources which affect the performance of a TDC, including quantization error, linearity issue, and randomness due to thermal effect. In the closed-loop operation, the TDC quantization of timing estimation affects the phase noise at the ADPLL output. Similar to ADC quantization process calculations, the quantization noise of TDC can be derived from assuming the white noise with uniformly distributed as shown in [14]:

$$S_{Q,TDC}(s) = \frac{\Delta_{TDC}^2}{12}. \tag{2-3}$$

It is a low-pass transfer function from TDC noise. Therefore, the output phase noise introduced by the TDC is

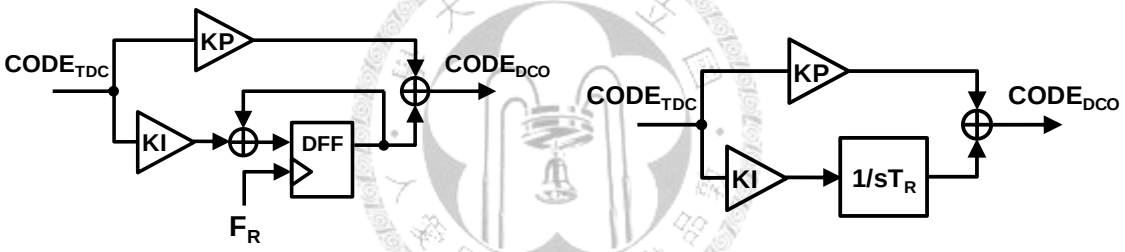
$$S_{\Phi,OUT}(s) = \frac{(2\pi\Delta_{TDC})^2}{12T_{REF}} \left| \frac{NG(s)}{1+G(s)} \right|^2, \tag{2-4}$$

where T_{REF} is the reference period, N is divider ratio, and $G(s)$ is the open loop gain of ADPLL. It reveals that the noise contribution from TDC could be minimized by improving the TDC resolution and increasing the sampling rate.

2.3.2 Digital Loop Filter (DLF) and Digital-Controlled Oscillator (DCO)

Choosing different DLF structures affect the type and order of ADPLL. The type-I PLL generally features faster dynamics, but the steady phase error does not go to zero in place of a constant amount which is proportional to the frequency offset.

Compared with the type-I first-order ADPLL by only a proportional gain in DLF, a type-II second-order ADPLL has the advantages of good DCO noise attenuation, small static phase error as the loop locked, and better design flexibility between bandwidth and tracking ability. Fig. 2-5 shows the block diagram of proportional-integral (PI) controller and s-domain linear model of DLF for a type-II second-order ADPLL. The integral path is made by a digital accumulator. In mathematical analysis, the integrator is replaced by $z^{-1}/1-z^{-1}$ in the z-domain model, and then converted into s-domain model using $s=F_R(z-1)$ with a reasonable assumption of the frequency much smaller than F_R [15]. In order to achieve more noise attenuation, a higher order ADPLL which cascades with a single-pole IIR filter can be chosen [13].



(a) (b)

Fig. 2-5 DLF for a type-II second-order ADPLL: (a) block diagram, and (b) Linear model.

DCO is a crucial building block in an ADPLL system. It converts control code to modulate the output frequency according to the phase error in PFD. The input-output characteristic curve is shown in Fig. 2-6.

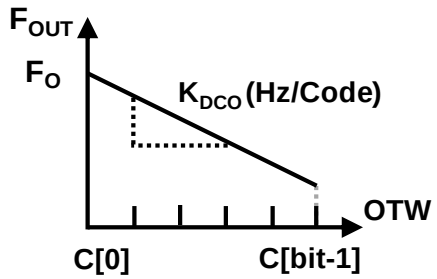


Fig. 2-6 Input-output characteristic of the DCO.

The relationship between the digital oscillator tuning word (OTW) and output frequency (F_{OUT}) can be expressed by

$$F_{OUT} = F_O + K_{DCO}OTW \ , \tag{2-5}$$

where F_O is the output free-running frequency of DCO when OTW is zero, and K_{DCO} is the gain of its transfer function.

In order to improve the frequency resolution in digital operation, a delta-sigma modulation (DSM) is implemented between a DLF and DCO. Finally, a DCO has two noise sources including nature noises (e.g., thermal noises and flicker noises of components (S_N) and additional noises derived from DSM (S_Q)). The s-domain linear model is shown in Fig. 2-7. The mathematical analysis will be described in 4.1.3 in detail.

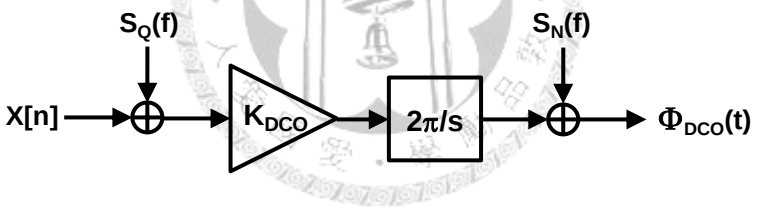


Fig. 2-7 Linear model of the DCO.

2.3.3 Divider

In time-domain, the gain of the frequency divider is simply a scale factor, *N*. However, the effect of the frequency division in the phase-domain is phase modulation. The phase of the input signal is modulated by a sinusoidal signal with the modulation frequency, ω_m, which is

$$\phi_{in}(t) = \omega_{in}t + \phi_d \ sin(\omega_m t) , \tag{2-6}$$

where ϕ_d is peak phase deviation magnitude of the input signal. According to the relationship between frequency and phase, the instantaneous frequency is the derivative of the input phase, and it can be expressed as

$$\omega_{inst}(t) = \frac{1}{2\pi}\frac{d\phi_{in}(t)}{dt} = \omega_{in} + \phi_d \omega_m \cos(\omega_m t). \quad (2\text{-}7)$$

After the divide ratio is specified by channel selection, the output frequency of the divider can be rewritten as

$$\omega_{div}(t) = \frac{\omega_{inst}}{N} = \frac{\omega_{in}}{N} + \frac{\phi_d \omega_m \cos(\omega_m t)}{N}. \quad (2\text{-}8)$$

Taking the integral value of ω_{div}, and then the phase of the output signal can be derived as follows:

$$\phi_{div}(t) = \int \omega_{div}(t)dt = \frac{\omega_{in} t}{N} + \frac{\phi_d \sin(\omega_m t)}{N} = \frac{\phi_{in}(t)}{N}. \quad (2\text{-}9)$$

Eq. (2-9) shows the input phase deviation magnitude is inversely proportional to the divide ratio, *N*. Besides, the modulation frequency, ω_m, is not influenced by the frequency divider. Eventually, the phase-domain transfer function of the frequency divider only behaves as a gain stage with value *1/N*.

On the other hand, the choosing of a different divider ratio is related to output noise performance. Phase noise is a critical specification in the local oscillator of radio systems. It is a ratio of noise power to output carrier power in a 1 Hz bandwidth at a given offset from the carrier. This performance typically bears on the receiver sensitivity. The total phase noise in a PLL can be expressed as [4]

$$L_{total} = L_{in\text{-}band} - 10\log f_{REF} - 20\log N, \quad (2\text{-}10)$$

where $L_{in\text{-}band}$ is the phase noise due to the synthesizer itself and f_{REF} is the input reference frequency.

2.4 Summary

This chapter introduced an overview of the basic principle of analog PLLs. The previous works of ADPLLs and their categories were first developed. The phase-domain formation of each building block for linear model analysis was finally derived.

Chapter 3

A Fast-Locking ADPLL using Dynamic Phase Control

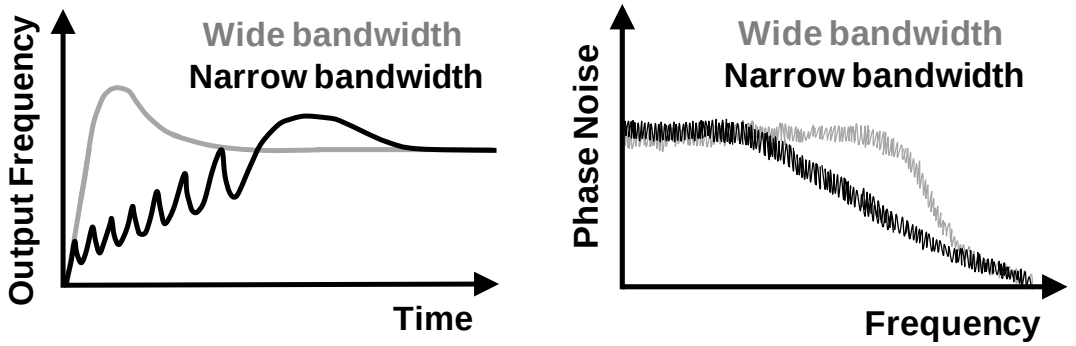
3.1 Introduction

PLL based frequency synthesizer is an essential component in wireless communication system. Many communication standards have stringent requirement on the settling time of frequency synthesizer. A typical PLL can be approximated as an under-damped second-order system. The settling time of PLL is governed by loop bandwidth and damping factor. We can express the settling time as below [16]:

$$t_s = \frac{-1}{\zeta \omega_n} ln\left(\frac{f_{tol}\sqrt{1-\zeta^2}}{N\Delta\omega} \right). \quad (3\text{-}1)$$

ζ is the damping factor, ω_n is the nature frequency, f_{tol} is frequency tolerance range, and N is divider ratio. From the equation shown, PLL settling time is inversely proportional to loop bandwidth. A simple way to increase PLL settling speed is to enlarge the loop bandwidth. However, there are some constrains on the choice of the loop bandwidth, because it will directly affect the phase noise and spurs performance.

Fig. 3-1 illustrates the settling time and phase noise under different loop bandwidths [17]. In addition to the design consideration, the loop bandwidth is limited by the stability requirement [18][19]. There exists a well-known rule of thumb in PLL, which is the loop bandwidth should be less than 1/10 of reference frequency. If the loop bandwidth is too wide, the PLL becomes less stable or even fails to lock.



(a) (b)

Fig. 3-1 The impacts of different loop bandwidths on (a) settling time, and (b) phase noise.

On the other hand, the multiplication of the DCO gain (K_{DCO}) and the proportional gain in DLF (*KP*) should be minimized under a given integral gain in DLF (*KI*) to achieve the best performance of an output jitter [20]. In frequency response, the magnitude of the transfer function will have the widest pass-band without any peaking when $\zeta = 0.707$. If the transfer function is modeled as *A(s)* (=*Vo(s)/Vin(s)*), the normalized peak value, M_p, is obtained by calculating the slope of *A(s)*,

$$M_p = \frac{A(j\omega_p)}{A_o} = \frac{1}{2\zeta\sqrt{1-\zeta^2}}. \tag{3-2}$$

A_o is the dc gain of the transfer function, ω_p denotes the frequency as the peaking happened, and ζ is the damping factor.

The variance of the long-term PLL absolute jitter is related to the phase noise as [21]

$$\sigma_{t,PLL}^2 = \frac{1}{(2\pi f_{out})^2} \int_{-f_o/2}^{f_o/2} S_{\phi,PLL}(f_m)\, df_m, \tag{3-3}$$

where f_{out} is the output frequency and $S_{\phi,,PLL}$ is the total phase noise in the system. It is straightforward to calculate the total output phase noise by summing the contributions

of the different noise sources. Assuming dominate noise from reference input, jitter performance will degrade with increasing loop bandwidth. More details about phase noise of an ADPLL will be described in Section 3.3.6.

With the increasing of the loop bandwidth for fast locking operation, the noises from PFD/TDC/Divider are much harder to be suppressed. It reveals that a wider loop bandwidth allows more noise and reference spurs to feed through to the output. But a scale-down loop bandwidth produces a phenomenon of cycle slipping because the loop excessively suppresses DCO modulation. For a smaller bandwidth design may make the system close to the instability limit, the jitter is also dramatically regenerated due to frequency peaking [20]. Thus, it is required to design a high-performance PLL based frequency synthesizer to make trade-offs between low jitter and fast lock.

To address those critical issues, an ADPLL with dynamic phase compensation is presented. The system is operated in dual switching manipulations which are frequency acquisition mode and phase tracking mode. Dual-path operations are implemented in feed-forward DCO modulating (frequency compensation path) and dynamic divider adjustment (phase compensation path). In order to verify the idea, the proposed ADPLL is realized at the 2.4 GHz band. Methods to relax design restrictions mentioned above will be described in this section.

3.2 Principle of the Proposed Method

In this section, we will introduce certain backgrounds, which are bandwidth switching and frequency presetting for reducing lock time. In addition, implemented topologies of feed-forward function and phase error compensation are introduced in the following. Both of them will be implemented in frequency acquisition mode.

3.2.1 Background

Bandwidth switching is the candidate architecture for improving settling time of PLL. Fig. 3-2 depicts a typical PLL which incorporates the bandwidth switching technique. The main idea is to widen loop bandwidth during the locking process and change the loop into a desired narrow bandwidth once the loop is approaching locked state. The architecture is implemented by increasing CP current into I_1+I_2. Meanwhile, for maintaining the loop stability, the resistance on LPF is reduced to $R_1//R_2$. Nevertheless, due to the loop stability effects, the improvement on locking speed will be restricted by the expanding ratio of loop bandwidth. The adjustable loop bandwidth can be done by dynamically adjusting the CP current, VCO gain, divide ratio, and filter parameters [16][22].

Another common design approach is frequency presetting by utilizing a lookup table [23][24]. Fig. 3-3 shows a sketch of this presetting frequency approach. The lookup table initially records all the proper configurations for each channel. When the frequency hopping occurs, this lookup table enables the PLL to preset the VCO into the desired output frequency according to the memorized configurations. A very fast settling time is then achieved since the output frequency is preset directly. However, it is difficult to generate an accurate lookup table, since the frequency setting configuration for each channel is sensitive to PVT variations. Consequently, this approach often requires complicated calibrations to realize such a lookup table.

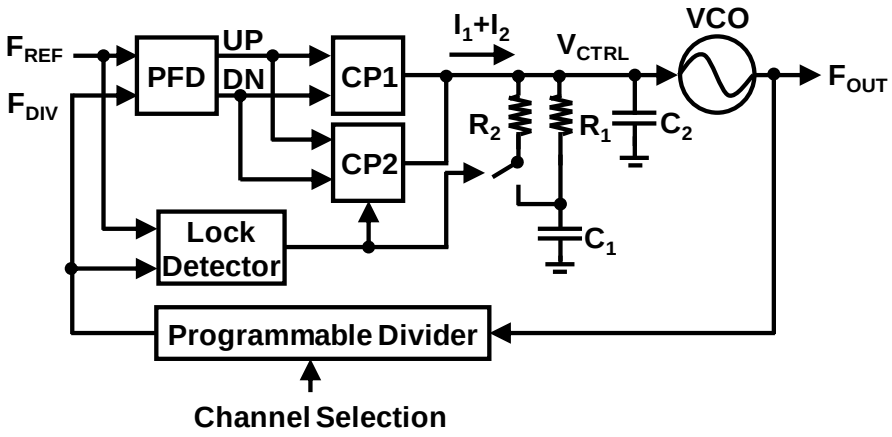


Fig. 3-2 Block diagram of a PLL with bandwidth switching method.

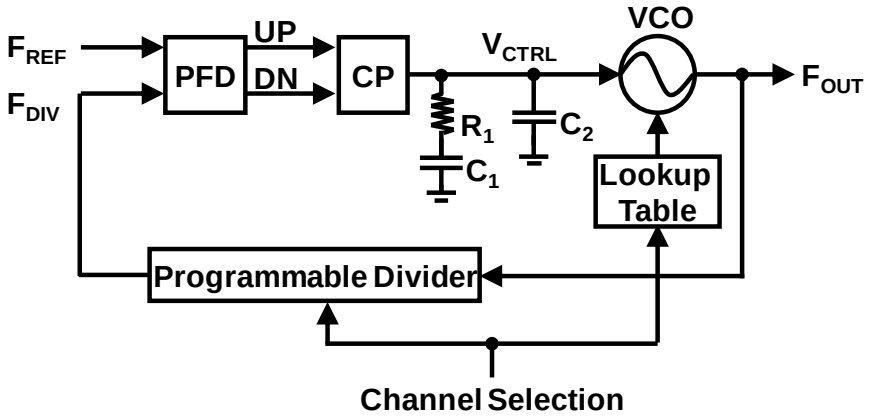


Fig. 3-3 Block diagram of a PLL with frequency presetting.

3.2.2 Phase Error Compensation

In locking process, the phase error accumulates rapidly on each reference cycle, because the phase error is the integration of frequency error. The locking features are conceptually shown in Fig. 3-4. The conventional transient process leads to a large phase error, which prevents the loop from being locked even though the output frequency at t_F is correct. With the increasing of the distance of hopping frequency, this phase error grows greatly. Hence, if the phase error can be continuously monitored and well-controlled, the lock time in extra phase tracking can be significantly reduced

(t_P<<t_C) [16]. This thesis implemented a phase error compensation technique that dynamically cancels integrated phase error during locking process.

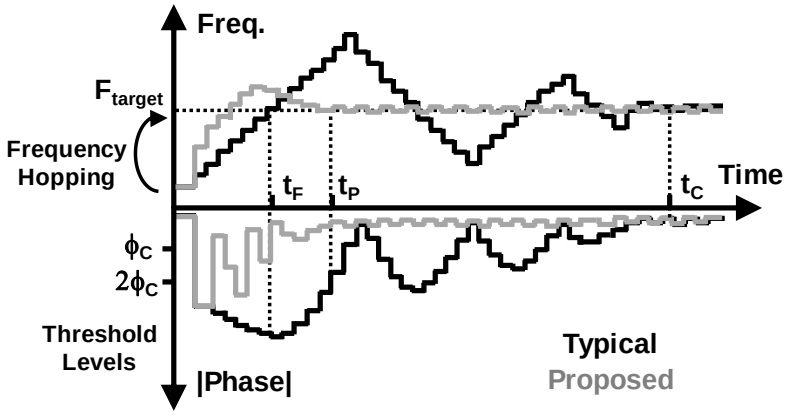


Fig. 3-4 Conceptual locking process in typical ADPLL and ADPLL with phase error compensation.

The phase error compensation is accomplished by altering the divider ratio of the programmable divider. The compensation principle is graphically illustrated in Fig. 3-5. For example, if the phase of F_{REF} leads F_{FB_LAG} by a threshold level at a particular cycle, the phase error may grow to a larger value in the next cycle. Thus, the divider ratio is reduced to *N-X*, where *X* depends on the phase error magnitude. On the other hand, if F_{FB_LEAD} leads F_{REF}, the divider ratio will be increased to *N+X*. According to the threshold levels, this procedure continues until the phase error at the PFD input is sufficiently small.

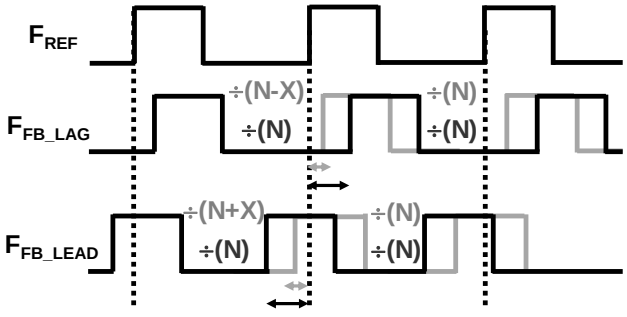


Fig. 3-5 The timing diagram of divider ratio modification for phase error compensation.

Because the operation of phase error compensation continuously reflects to PFD input, the shrunk phase information has a side effect on restricting DCO frequency update. Therefore, an auxiliary frequency modulation mechanism is required to extend loop bandwidth at the same time when phase error compensation technique is activated. When operating in frequency acquisition mode, both compensation of frequency calibration and phase error adjustment are automatically utilized according to the threshold level.

3.2.3 Proposed ADPLL Architecture

Fig. 3-6 depicts the architecture of the proposed ADPLL. An auxiliary TDC (ATDC) are implemented the timing window to detect the coarse range and polarity of phase error. Based on the amount of phase error, the adjustable delay cell of an ATDC generates corresponding thermometer codes, [S_2, S_1, S_0], which is sent into KI controller and programmable divider. The least significant bit (LSB) of ATDC, $S_{0,}$ is also an important mark to determine the loop operating in different modes. The system is operated in dual-mode which is frequency acquisition mode in binary detection and phase tracking mode in linear detection. We combine dual-path techniques of feed-forward frequency modulation and phase error compensation in frequency acquisition mode to achieve a fast-locking ADPLL. The system chose appropriate loop parameters to optimize damping factor for low-jitter performance. In the beginning of the locking process, the frequency acquisition mode is first activated and the main TDC (MTDC) circuit is modeled as a BBPD. A digital-controlled feed-forward function is used for modulating DCO frequency directly with the slash arrow and a dynamic divider adjustment in phase error compensation path is illustrated with the meshed arrow in Fig. 3-6.

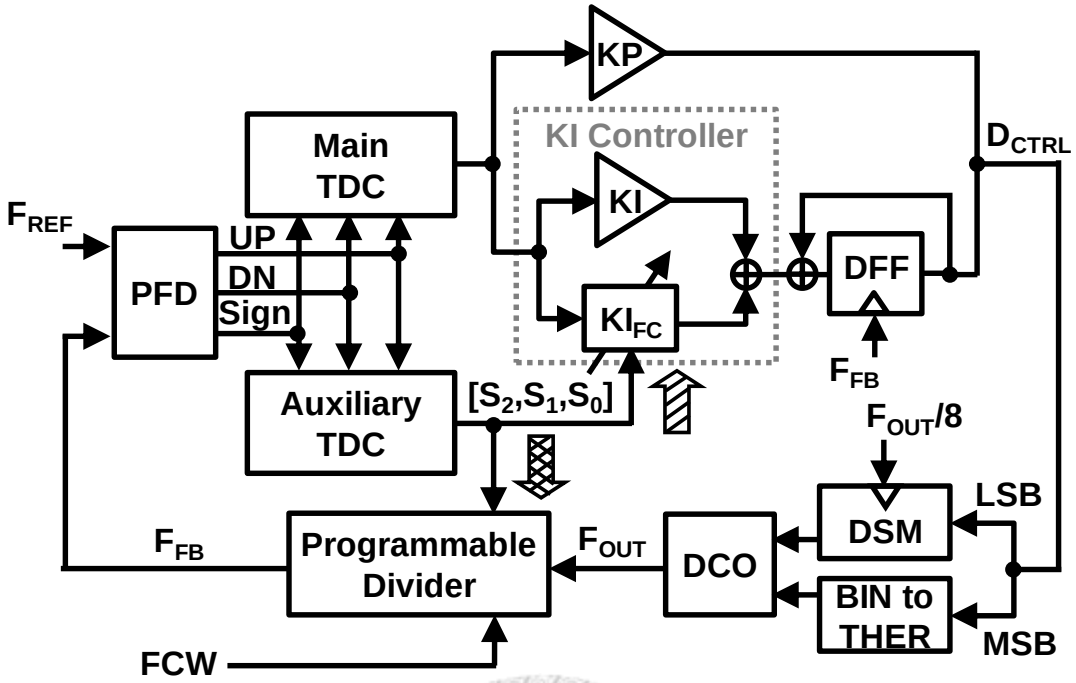


Fig. 3-6 The proposed dynamic phase control ADPLL.

It is known that the principle of typical PLL is to adjust the output frequency by detecting the phase error. Small phase error results in slow frequency switching. When the phase error compensation path is enabled, if phase error is reduced during each reference cycle, it may cause the control code (D_{CTRL}) changing slowly to correct the output frequency. To solve this problem, a feed-forward frequency compensation path is incorporated. The main signal path from MTDC to DLF becomes a binary detection without magnitude information of phase error, because the whole range of MTDC is designed smaller than the resolution of ATDC. Thus, it can inject extra gain to modulate DCO frequency by changing KI whenever the phase error compensation is applied, which effectively increases the speed of frequency acquisition. A flexible KI controller is implemented using shift registers and logic operators instead of multipliers. The compensated amount is based on ATDC output. More shift bits are applied if frequency error is large. Besides, the loop stability is not compromised in this structure because the compensation scheme effectively provides a zero in the loop

transfer function [16]. Finally, once this loop approaches locked state, the phase error is adequately small. The ATDC and the associated compensation paths are off. The loop returns to normal TDC based ADPLL operation.

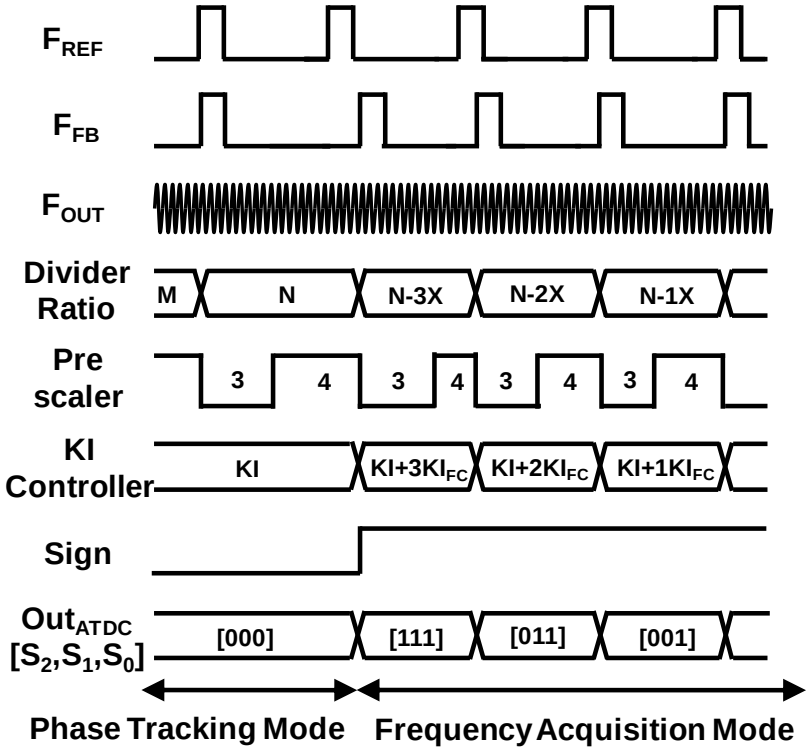


Fig. 3-7 Operation timing diagram of the proposed architecture.

Fig. 3-7 illustrates the operation timing diagram of the proposed method. Once the synthesizer changes to another channel and divide ratio alters from *M* to *N* (*N*>*M*), an equivalent phase error is generated due to frequency error. S_0 is a mode detection. The quantization feature of ATDC and *Sign* signal reflects phase error between F_{REF} and F_{FB}. According to the ATDC output, the divide ratio decreases and the next edge of F_{FB} arrives earlier to compensate the large phase error. At the same time, the frequency compensation gain, KI_{FC}, will be regulated by KI controller to speed up locking behavior. The two path compensations are terminated and system sets adapted *KP* and *KI* for a stable transfer function. Under this situation, the system maintains the phase

error small enough and the loop bandwidth is narrow without frequency peaking. Therefore, low-jitter characteristic can be realized in locked condition.

3.2.4 Control Mechanism of DLF

We propose a novel method to modulate DCO for frequency compensation with taking advantage of the feed-forward architecture. If the phase subtraction circuit in ADPLL is modeled as a BBPD, it can directly control *KI* in DLF to achieve an inherent compensation function instead of using original analog manners [30][31]. The mechanism has advantages of the digital programmable feature and saves an additional path. The gain of feed-forward frequency compensation will be analyzed in Section 3.3.1.

It is important to design proper loop parameters in order to achieve a low-jitter performance in fast-locking topology. In addition to realizing a frequency modulation path in the locking process, the mechanism of damping factor correction is needed in phase tracking mode. This correction circuit can be employed in the DLF block because of their digital nature in selecting filter parameters. For an expected bandwidth (ω_n), which is determined by *KI*, *KP* can be derived from closed loop transfer function by assuming $\zeta > 1$.

$$KP > \frac{2N\Delta_{MTDC}}{T_{REF}K_{DCO}}\omega_n, \tag{3-4}$$

where N is divider ratio; Δ_{MTDC} is MTDC resolution; T_{REF} is reference frequency; K_{DCO} is DCO gain. From this point of view, we can observe that there are a set of optimum loop parameters to meet a narrow bandwidth without frequency peaking for a low-jitter ADPLL in the locked state.

3.3 Linear Model Analysis of Proposed ADPLL

In this section, the calculation steps for the proposed ADPLL parameters are illustrated. First, the linear model in different modes which are frequency acquisition mode and phase tracking mode will be introduced. Then we briefly present stability, locking transient, output spur, phase noise, and jitter. Finally, we have an example to design the proposed architecture by behavior simulation tool.

3.3.1 ADPLL in Frequency Acquisition Mode

In the traditional analog PLL, signals between circuit blocks are continuous and linear. The s-domain linear analysis method is appropriate for this kind of system. But in the ADPLL, because of the discrete time operations and the quantization effect, in order to make the linear analysis method available, some modification and approximation are needed to model an ADPLL. The conversion between the s-domain and z-domain is shown in [13].

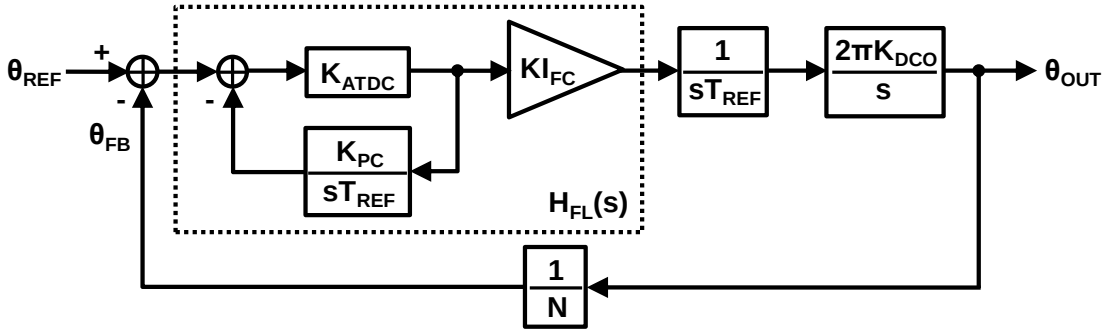


Fig. 3-8 The linear model of the proposed ADPLL in frequency acquisition mode.

As mentioned above, the frequency acquisition mode is first activated at the beginning of the locking process. In order to reduce the area and power of MTDC, the programmable ATDC is used to detect coarse phase error and compensate loop characteristic instantly. The overall equivalent model under the frequency acquisition mode is depicted in Fig. 3-8. The quantization noise of TDC and DCO are neglected in

this model. If the desired steady-state loop bandwidth is small, the *KP* and *KI* will be small. And we design the LSB of ATDC greater than the whole MTDC range. In a standard ADPLL architecture, the building blocks of phase quantizer and DLF can be ignored in the following analysis. $H_{FL}(s)$ describes the transfer function of the fast-locking module, which is expressed in (3-5),

$$H_{FL}(s) = \frac{sT_{REF}K_{ATDC}KI_{FC}}{sT_{REF} + K_{ATDC}K_{PC}}. \tag{3-5}$$

The transfer function of the coarse timing window is represented by K_{ATDC}, it can be modeled as $T_{REF}/2\pi\Delta_{ATDC}$, Δ_{ATDC} is the resolution of ATDC. The gain of phase error compensation is represented by $K_{PC}=2\pi T_{UT}/T_{REF}$, T_{UT} is the equivalent time of unit code change, $T_{UT}=N_{SH}T_{OUT}$ (N_{SH} represents the shift of divider ratio due to a unit code from ATDC). And the gain of KI controller is modeled as KI_{FC}. Hence, the open-loop transfer function can be derived as below:

$$\begin{aligned} H_{OPEN,FA}(s) &= \frac{\theta_{REF}(s)}{\theta_{FB}(s)} = H_{FL}(s)\cdot\frac{1}{sT_{REF}}\cdot\frac{2\pi K_{DCO}}{s}\cdot\frac{1}{N} \\ &= \frac{2\pi K_{ATDC}KI_{FC}K_{DCO}}{NT_{REF}}\frac{1}{s\left(s+\frac{K_{ATDC}K_{PC}}{T_{REF}}\right)}. \end{aligned} \tag{3-6}$$

Note that such compensation operation provides a zero at s=0 in the transfer function $H_{FL}(s)$, and it cancels out one pole at s=0. In addition, it is worth noting that the loop in frequency acquisition mode contains only a pole at the origin, which is unlike type-II PLL having two poles at s=0. The system is switched to type-I operation which features the fast lock characteristic.

The closed-loop transfer function can be derived as below:

$$H_{CLOSED,FA}(s)=\frac{\theta_{OUT}(s)}{\theta_{REF}(s)}$$
$$=\frac{2\pi K_{ATDC}KI_{FC}K_{DCO}}{T_{REF}}\cdot\frac{1}{s^2+s\frac{K_{ATDC}K_{PC}}{T_{REF}}+\frac{K_{ATDC}KI_{FC}K_{DCO}}{NT_{REF}}}. \quad (3\text{-}7)$$

By comparing with the 2nd order system closed-loop transfer function in control theory, both the damping factor (ζ_{FA}) and natural frequency ($\omega_{n,FA}$) are calculated by:

$$\zeta_{FA}=\frac{K_{PC}}{2T_{REF}}\sqrt{\frac{K_{ATDC}NT_{REF}}{KI_{FC}K_{DCO}}}, \quad (3\text{-}8)$$

$$\text{and}\quad \omega_{n,FA}=\sqrt{\frac{K_{ATDC}KI_{FC}K_{DCO}}{NT_{REF}}}. \quad (3\text{-}9)$$

Based on the above derived expressions, the behavior of the proposed ADPLL can be predicted and well-controlled by proper selections of loop parameters.

3.3.2 ADPLL in Phase Tracking Mode

After the initial frequency is locked roughly using the frequency acquisition mode, the architecture can be further simplified as a type-II second-order TDC based ADPLL in phase tracking mode. The s-domain linear model is shown in Fig. 3-9. According to the models of building blocks in 2.3, the open loop transfer function of proposed ADPLL in locked state is given by

$$H_{OPEN,PT}(s)=\frac{\theta_{REF}(s)}{\theta_{FB}(s)}=\frac{T_{REF}}{2\pi\Delta_{MTDC}}\cdot\frac{sT_{REF}KP+KI}{sT_{REF}}\cdot\frac{2\pi K_{DCO}}{s}\cdot\frac{1}{N}. \quad (3\text{-}10)$$

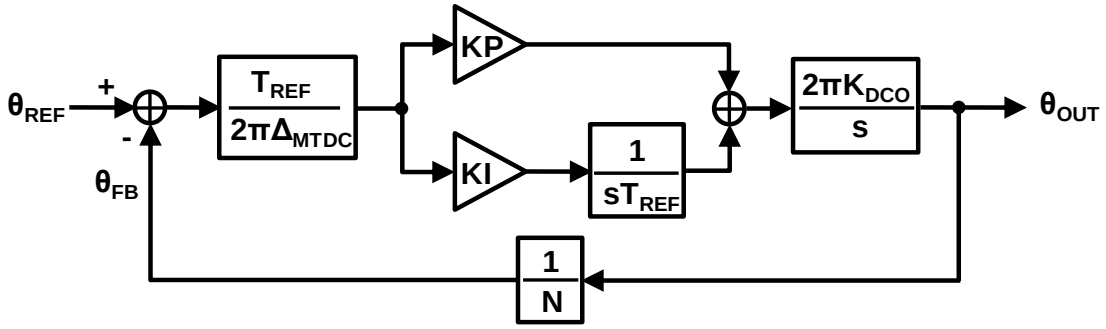


Fig. 3-9 The linear model of the proposed ADPLL in phase tracking mode.

On the other hand, the close loop transfer function can be calculated as

$$H_{CLOSED,PT}(s)=\frac{\theta_{OUT}(s)}{\theta_{REF}(s)}=\frac{\frac{KP\cdot KI\cdot K_{DCO}T_{REF}}{\Delta_{MTDC}}s+\frac{KI\cdot K_{DCO}}{\Delta_{MTDC}}}{s^2+\frac{KP\cdot KI\cdot K_{DCO}T_{REF}}{N\Delta_{MTDC}}s+\frac{KI\cdot K_{DCO}}{N\Delta_{MTDC}}}. \quad (3\text{-}11)$$

In this case, the damping factor (ζ_{PT}) and natural frequency ($\omega_{n,PT}$) in phase tracking mode are also derived by comparing with a standard 2nd order system closed-loop transfer function:

$$\zeta_{PT}=\frac{T_{REF}KP}{2}\sqrt{\frac{K_{DCO}}{N\cdot KI\cdot\Delta_{MTDC}}}, \quad (3\text{-}12)$$

$$\text{and}\quad \omega_{n,PT}=\sqrt{\frac{K_{DCO}KI}{\Delta_{MTDC}N}}. \quad (3\text{-}13)$$

Based on the numerical analysis and appropriate simplification between open loop and closed loop transfer function [32], we can derive unity gain bandwidth (ω_T) and phase margin (*PM*) from closed loop parameters:

$$\omega_{T,PT}=\omega_{n,PT}\sqrt{\left[\sqrt{4\zeta_{PT}^4+1}-2\zeta_{PT}^2\right]}, \quad (3\text{-}14)$$

$$\text{and}\quad PM_{PT}=\cos^{-1}\left[\sqrt{4\zeta_{PT}^4+1}-2\zeta_{PT}^2\right]. \quad (3\text{-}15)$$

Based on the definition of the closed loop -3dB bandwidth, $|H(j\omega_{-3dB})|=|H(j0)|/2$, we can realize the closed loop -3 dB bandwidth is

$$\omega_{-3dB,PT} = \omega_{n,PT}\sqrt{1+2\zeta_{PT}^2+\sqrt{2+4\zeta_{PT}^2+4\zeta_{PT}^4}}\ . \qquad (3\text{-}16)$$

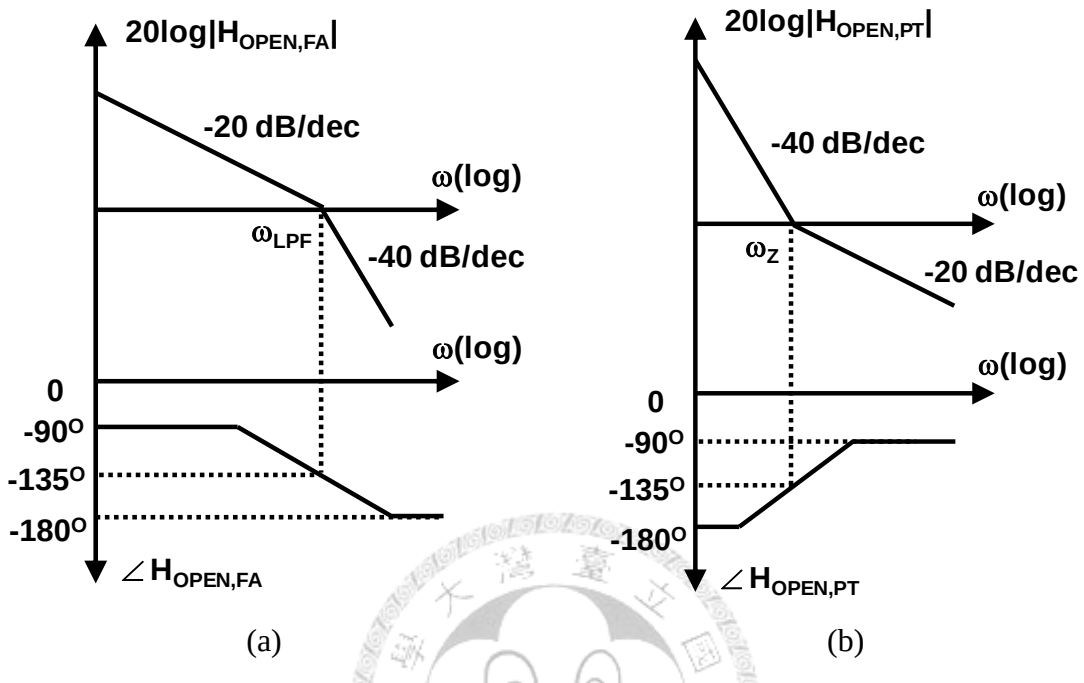
From an observation of mathematical analysis, we can find out that there are several parameters can be designed in an ADPLL. N and T_{REF} are determined by reference frequency and target frequency and they are always defined by specifications. Δ_{MTDC} and K_{DCO} are limited by the CMOS process without special techniques. Therefore, the *KI* and *KP* are the best candidates to characterize the system. It is easy to design different nature frequency and damping factor by selecting different combinations of *KP* and *KI*, because of the digital nature of DLF implementation. Not only the stability issue but also lock time and timing jitter will be affected due to a wrong parameter design. A damping factor around 0.707 is commonly used to get better performance. The larger *KP*/*KI* represents the better stability. The larger *KI* reveals the wider bandwidth under the same stability, but the larger *KP* induces larger steady state jitter.

3.3.3 Stability Analysis

For most fast-locking PLL, system stability should be carefully analyzed since the loop dynamic has been changed. To assure loop stability of the proposed approach, the analysis of the loop characteristic during frequency acquisition mode and locked state must be provided.

By utilizing the open loop transfer function (3-6), the bode plots of the magnitude and phase of the loop gain is obtained. As depicted in Fig. 3-10 (a), the loop gain begins from infinity at ω=0 and falls at a rate of -20 dB/dec for $\omega<\omega_{LPF}$ and at a rate of

-40 dB/dec thereafter. By analyzing the bode diagram, the phase margin in frequency acquisition mode can be obtained.



(a) (b)

Fig. 3-10 Bode plots in (a) frequency acquisition mode, and (b) phase tracking mode.

The stability behavior can also be analyzed by the root locus of their poles and zeros in the complex plane as the parameter $K=K_{ATDC}KI_{FC}K_{DCO}/NT_{REF}$ varies. From Eq. (3-6), the two poles of the closed-loop system are given by

$$s_{1,2}=\frac{-2\zeta\omega_n \pm \sqrt{4\zeta^2\omega_n^{\ 2}-4\omega_n^{\ 2}}}{2}=(-\zeta \pm \sqrt{\zeta^2-1})\omega_n . \qquad (3\text{-}17)$$

When K=0, the two poles lie on $s_1=-\omega_{LPF}=-K_{ATDC}K_{PC}/T_{REF}$ and s_2=0, and the damping factor (ζ) is infinity. As K increases, ζ decreases and the two poles move toward each other on the real axis. For ζ=1, the two poles are identical, $s_1=s_2=-\omega_{LPF}/2$. As K increases further, the two poles become complex and ζ drops which causes the loop become less stable.

On the other hand, the bode plot is obtained in Fig. 3-10 (b) by open loop transfer function (3-10) under phase tracking mode. The loop gain begins from infinity at ω=0

and changes a rate from -40 dB/dec to -20 dB/dec at $\omega=\omega_Z$. If the ω_Z is designed equal to the gain-crossover (0-dB) frequency, the phase margin is 45°.From Eq. (3-10), the zero frequency is derived by

$$\omega_z = \frac{KI}{KP \cdot T_{REF}}. \tag{3-18}$$

Thus, the phase margin in a locked state can be redefined by ω_Z and ω_T.

$$PM = tan^{-1}\left(\frac{\omega_T}{\omega_Z}\right). \tag{3-19}$$

3.3.4 Transient Behavior

Settling time is defined as the time at which the response settles to within some percentage of the final steady state value. Since the proposed ADPLL spends most time operating in frequency acquisition mode, it is reasonable to approximate the ADPLL settling time by analyzing the settling time of linear model in frequency acquisition mode described above. For $0<\zeta<1$, applying a $\Delta\omega$ step input as a certain hopping frequency, the output frequency is described according to Eq. (3-6),

$$\omega_{OUT}(s) = N \cdot \omega_{FB}(s) = N \frac{\omega_n^{\,2}}{s^2 + 2\zeta\omega_n s + \omega_n^{\,2}} \frac{\Delta\omega}{s}. \tag{3-20}$$

By applying the *inverse Laplace transform*, the time-domain response can be obtained:

$$\begin{aligned} \omega_{OUT}(t) &= L^{-1}\left\{\omega_{OUT}(s)\right\} \\ &= \left[1 - \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} sin(\omega_n\sqrt{1-\zeta^2}t + \theta)\right] N\Delta\omega \cdot u(t), \end{aligned} \tag{3-21}$$

$$\text{where} \quad \theta = tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right). \tag{3-22}$$

The frequency error can be expressed by

$$\Delta\omega_{OUT}(t)=\frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}}\sin(\omega_n\sqrt{1-\zeta^2}t+\theta)N\Delta\omega\cdot u(t). \tag{3-23}$$

The settling time can be approximated by finding the time when the value of $\Delta\omega_{OUT}$ remains within some percentage of its final value. That is,

$$\left|\Delta\omega_{OUT}(t_s)\right|=\left|\frac{e^{-\zeta\omega_n t_s}}{\sqrt{1-\zeta^2}}\sin(\omega_n\sqrt{1-\zeta^2}t+\theta)N\Delta\omega\cdot u(t)\right|. \tag{3-24}$$

$$\frac{e^{-\zeta\omega_n t_s}}{\sqrt{1-\zeta^2}}N\Delta\omega\le f_{tol}, \tag{3-25}$$

where f_{tol} (frequency tolerance range) is a given percentage of the locking frequency.

By calculating Eq. (3-25), the settling time can be derived by

$$t_s=\frac{-ln(\frac{f_{tol}\sqrt{1-\zeta^2}}{N\cdot\Delta\omega})}{\zeta\omega_n}=\frac{ln(\frac{\Delta\omega_{OUT}}{f_{tol}\sqrt{1-\zeta^2}})}{\zeta\omega_n}, \tag{3-26}$$

where $\Delta\omega_{OUT}$ is the frequency error that output frequency needs to change.

3.3.5 Output Spur

Under the assumption of narrow band frequency modulation, the power level of the spurious tones compared to the carrier can be approximated as [11]:

$$P_{spur}=20\log\left(\frac{1}{2}\beta\right)(dBc), \tag{3-27}$$

where β is the modulation index defined as the ratio of frequency deviation ($\Delta\omega$) to the frequency of modulation wave (ω_m) in a frequency modulation system when using a sinusoidal modulating wave. However, for a symmetric square wave with frequency of ω_m as the modulating input, it can be expressed in the following *Fourier series* representation:

$$g_{square}(t) = \sum_{n=1.odd}^{\infty} \frac{2}{\pi}\frac{1}{n} sin(n\omega_m t). \tag{3-28}$$

The modulation index of the nth harmonic for *Fourier series* decomposition of a square modulating wave becomes:

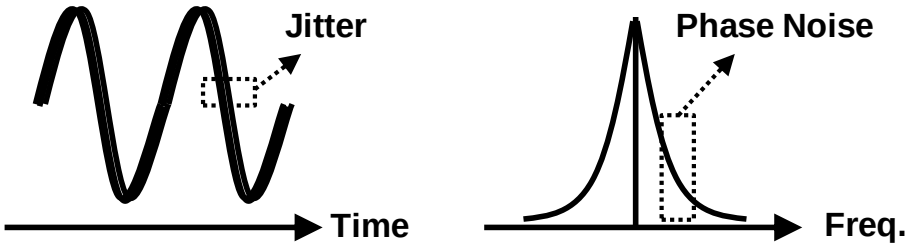
$$\beta_n = \frac{2}{\pi n}\frac{\Delta\omega_{pp}}{n\omega_m}, \tag{3-29}$$

where $\Delta\omega_{pp}$ is the peak to peak frequency deviation. It should be noted that in most cases, only the fundamental component (n=1) would really matter. The output clock of an ADPLL system is frequency modulated by a periodic control signal in locked state, leading to spurious tone emission. An inspection reveals that larger $\Delta\omega_{pp}$ and smaller ω_m will increase the power level of the spurs. But the analysis is performed under the noise-free assumption. In fact, the noise will randomize the spurious energy.

3.3.6 Phase Noise and Jitter

Phase noise and jitter performance are important indicators of the signal quality in a PLL system, which are determined by frequency domain and time domain, respectively. An ideal sinusoidal signal is shown in Fig. 3-11 (a). However, there are many issues in non-linearity and quantization error will cause non-ideal profile, which is illustrated in Fig. 3-11 (b). The real frequency spectrum resembles a skirt-like shape and the real DCO output waveform varying the zero-crossing points with time.

(a)



(b)

Fig. 3-11 The timing waveform and spectrum in different case: (a) ideal, and (b) real.

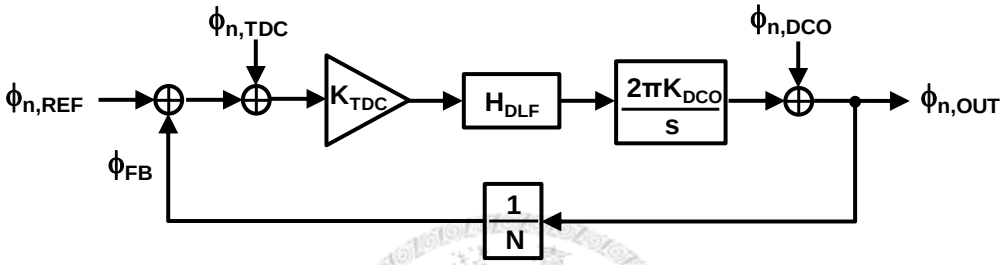


Fig. 3-12 The linear model of a ADPLL with internal and external noise sources.

In Fig. 3-12, the linear model of a tradition ADPLL is illustrated again including the internal and external noise sources. $\phi_{n,REF}$ is the phase noise from input reference clock, $\phi_{n,TDC}$ is the phase noise due to the quantization of TDC, and $\phi_{n,DCO}$ is the phase noise on the DCO output produced by itself. To find out the total output noise of the ADPLL, the expression of the power spectral density (PSD) of each noise source is required.

In this paragraph, we will separately introduce each generated noise in different building blocks. First, the phase noise PSD of the reference clock can be estimated according to the signal generator specifications. Secondly, the TDC is modeled as a linear block with a gain K_{TDC} ($=T_{REF}/2\pi\Delta_{TDC}$) and a quantization noise ($S_{Q,TDC} = \Delta^2_{TDC}/12$). Finally, the PSD of the noise from DCO will be derived. Consider the differential LC tank cross-coupled pair oscillator, the generated phase noise can be express as [33]

$$S_{\Phi,DCO}(\Delta f)=\frac{\bar{i_n^2}/\Delta f}{q_{max}^2}\frac{\Gamma_{rms}^2}{8\pi^2\Delta f^2}, \tag{3-30}$$

where $\bar{i_n^2}/\Delta f$ is the PSD of the equivalent parallel current noise, Γ_{rms} is the rms value of the impulse sensitivity function (ISF) associated with that noise source (Γ^2_{rms}=0.5 when the system output can be assumed to be a sinusoidal waveform), q_{max} is the maximum signal charge swing which is defined as the product of the tank capacitance and maximum signal swing $C_{tank}V_{swing}$, and Δf is the offset frequency from carrier. In a simplified stationary approach, the total noise power of the tank is mainly due to the cross-coupled transistor pair and the ohmic losses in the tank inductor:

$$\frac{\bar{i_n^2}}{\Delta f}\approx 2kT\gamma\mu_n C_{ox}\frac{W}{L}V_{ov}+\frac{4kT}{R_p}, \tag{3-31}$$

where R_p ($\approx 2\pi f_{osc}L_{tank}Q$) is the equivalent parallel resistance at the frequency of oscillation f_{osc}, T is the temperature, k is Boltzmann constant, μ_n is the mobility of the carriers in the channel, C_{ox} is the oxide capacitance per unit area, W and L are the width and length of the MOS transistor, V_{ov} is the gate drive of the MOS transistor, and γ is the channel length modulation coefficient.

From the model shown in Fig. 3-12, it is straightforward to calculate the total output phase noise by summing the contributions of the different noise sources:

$$S_{\Phi,ALL}(\Delta f)=$$
$$\left(S_{\Phi,REF}(\Delta f)+S_{\Phi,TDC}(\Delta f)\right)\left|\frac{NH(\Delta f)}{N+H(\Delta f)}\right|^2+S_{\Phi,DCO}(\Delta f)\left|\frac{N}{N+H(\Delta f)}\right|^2, \tag{3-32}$$

$$\text{where}\quad H(\Delta f)=\frac{K_{DCO}K_{TDC}}{j\Delta f}H_{DLF}(\Delta f). \tag{3-33}$$

In a more precise model of DLF, the output sequence is reconstructed by the zero-order-hold operation which can be expressed as a sinc function in frequency domain. Consequently, the frequency response of DLF is shown in [20]

$$H_{DLF}(f)=\frac{\sin\left(\frac{\pi f}{f_{REF}}\right)}{\left(\frac{\pi f}{f_{REF}}\right)}\left(KP+\frac{KI}{1-e^{-j2\frac{\pi f}{f_{REF}}}}\right)e^{-j\frac{\pi f}{f_{REF}}}. \tag{3-34}$$

On the other part of time domain measurement, jitter is defined as an important quality criterion. There are many previous works focus on finding a systematic relation between timing jitter and key design parameters like the reference frequency, output frequency, loop bandwidth, and power consumption [34]-[36]. The brief aims at defining a benchmark figure-of-merit (FoM) to evaluate the PLL jitter (σ_t) in relation to the consumed power (P),

$$FoM = 10\cdot log\left[\left(\frac{\sigma_t}{1s}\right)^2\cdot\frac{P}{1mW}\right]. \tag{3-35}$$

Jitter may result from phase noise or sidebands. Therefore, the supply/substrate noise, device noise, and periodic disturbance of control code will degrade jitter performance. However, the timing jitter can be broken down into two categories which are long-term jitter and short-term jitter. In the classification of short-term jitter, it has two types which are cycle-to-cycle jitter ($\Delta T_{cc,rms}$) and period jitter (ΔT_{rms}). From Eq. (3-36) and (3-37), the different definitions can be noticed.

$$\Delta T_{cc,rms}=\lim_{N\to\infty}\sqrt{\frac{1}{N}\sum_{n=1}^{N}\left(T_{n+1}^2-T_n^2\right)^2}, \tag{3-36}$$

$$\text{and}\quad \Delta T_{rms}=\lim_{N\to\infty}\sqrt{\frac{1}{N}\sum_{n=1}^{N}\Delta T_n^2}, \tag{3-37}$$

where T_{n+1} and T_n represent the period and next period, respectively. In [37], it derives a relationship between phase noise and cycle-to-cycle jitter assuming the PLL has a loop bandwidth, $2\pi f_u$.

$$\Delta T_{cc,rms} = \frac{1}{\sqrt{2\pi f_u}} S_\Phi(\Delta\omega)\frac{\Delta\omega}{\omega_o}, \tag{3-38}$$

where ω_o denotes the oscillation frequency, $S_\Phi(\Delta\omega)$ is the phase noise power at an offset frequency of $\Delta\omega$.

3.3.7 Design Example and Behavior System Simulation

In this thesis, a 2.4 GHz integer-N frequency synthesizer with dynamic phase compensation is realized. Since the transistor simulation usually takes very long time, it is inefficient and a waste of time to try the system behavior by transistor simulation. Therefore, it is recommended to simulate the behavior model by mathematical tools before performing the transistor simulation. To verify the correctness of the loop characteristic and loop parameters described above, the linear phase-domain model simulation should be taken firstly. Fig. 3-13 shows behavior model of the proposed ADPLL constructed by Matlab Simulink.

In this section, a design example of the proposed ADPLL with following specification has been shown:

- Reference frequency F_{REF} = 5 MHz
- Phase margin PM = 60°
- Unity gain bandwidth in phase tracking mode $F_{T,PT}$ = 80 kHz
- Unity gain bandwidth in frequency acquisition mode $F_{T,FA}$ = 300 kHz
- Divider ratio N= 480

- DCO gain K_{DCO} = 200 kHz/Code
- MTDC resolution Δ_{MTDC} = 5 ps

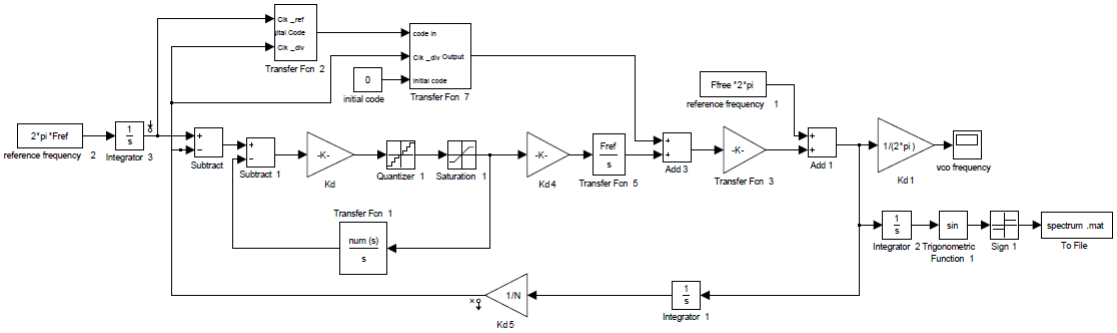


Fig. 3-13 Behavior model of the proposed ADPLL in Matlab Simulink.

To design the fast lock operation, the parameter analysis of the ADPLL in frequency acquisition mode must be applied. The open loop gain is given by Eq. (3-6), where the pole frequency (ω_p) is

$$\omega_p = \frac{K_{ATDC} K_{PC}}{T_{REF}}. \tag{3-39}$$

The phase margin of the system is given by

$$PM = 180^o - 90^o - tan^{-1}\left(\frac{\omega_{T,FA}}{\omega_p}\right), \tag{3-40}$$

where $\omega_{T,FA}$ is the unit gain frequency in frequency acquisition mode, and the relationship between $\omega_{T,FA}$ and ω_P is obtained as

$$\omega_{T,FA} = \omega_p \, tan(90^o - PM). \tag{3-41}$$

From the definition of unit gain frequency, a correlated formula can be defined as

$$\left| H_{OPEN,FA}(j\omega_{T,FA}) \right| = 1. \tag{3-42}$$

$$\left| \frac{2\pi K_{ATDC} KI_{FC} K_{DCO}}{N T_{REF}} \times \frac{1}{\left(-\omega_{T,FA}^2 + j\omega_{T,FA}\omega_p\right)} \right| = 1. \tag{3-43}$$

$$\omega_{T,FA}\sqrt{\omega_{T,FA}^{\ 2}+\omega_p^{\ 2}}=\frac{2\pi K_{ATDC}KI_{FC}K_{DCO}}{NT_{REF}}. \tag{3-44}$$

Replacing ω_p in Eq. (3-41) to (3-44), the parameter KI_{FC} and K_{ATDC} is obtained as

$$KI_{FC}=\frac{NK_{PC}\omega_{T,FA}\sqrt{1+(\tan(90^o-PM))^2}}{2\pi K_{DCO}}, \tag{3-45}$$

$$\text{and}\quad K_{ATDC}=\frac{T_{REF}\omega_{T,FA}}{K_{PC}(\tan(90^o-PM))}. \tag{3-46}$$

However, the limited number of ATDC bit leads to limited amount of compensation. Therefore, the larger frequency hopping distance, the more bits of ATDC output is needed [16]. In our application specification, it is reasonable to choose 3-stage ATDC. Thus, K_{PC} is limited by the circuit implementation and lacks of flexibility, so it is designed first and then calculate the other parameters, KI_{FC} and $K_{ATDC,}$ according to loop specification, $\omega_{T,FA}$ and phase margin.

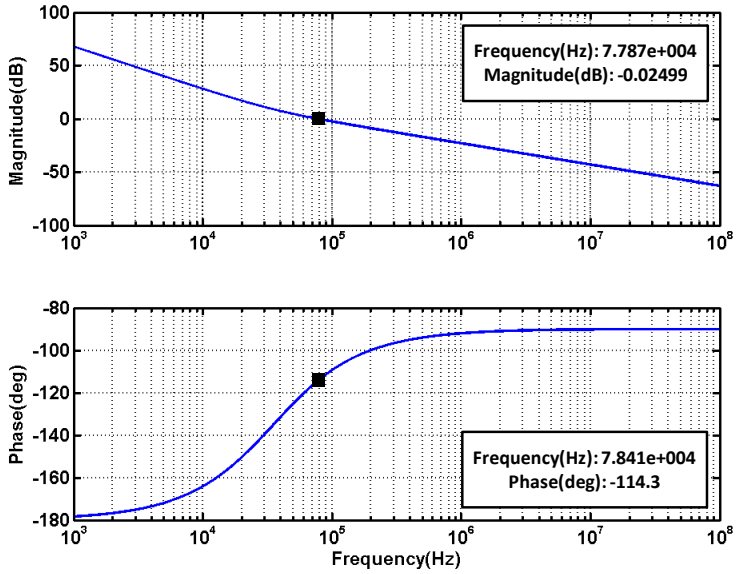
In the phase tracking mode, the standard PLL analysis is applied to calculate the design parameters of the ADPLL. Since the definition of unity gain bandwidth ($|H_{OPEN,PT}(j\omega_{T,PT})|$=1), the *KP* and *KI* can be found from Eq. (3-18) and (3-19):

$$KP=\frac{N\Delta_{MTDC}\omega_{T,PT}\sin(PM)}{T_{REF}K_{DCO}}, \tag{3-47}$$

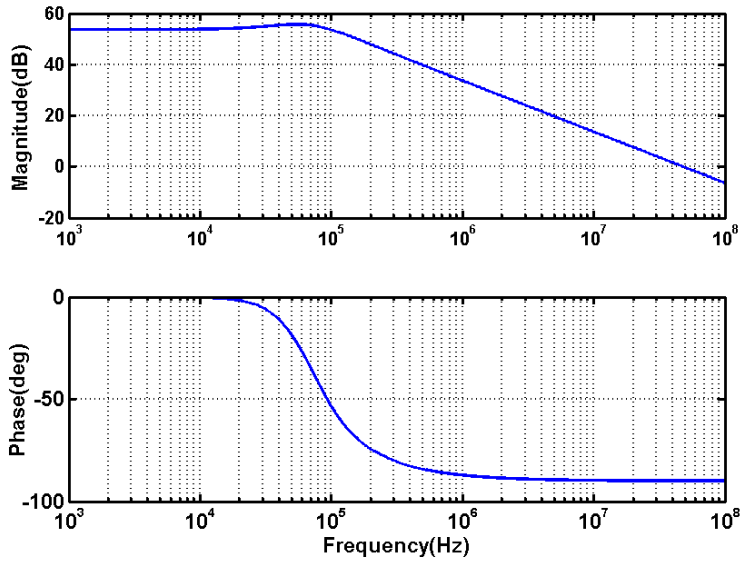
$$\text{and}\quad KI=\frac{\omega_{T,PT}T_{REF}KP}{\tan(PM)}. \tag{3-48}$$

For the 0.18 μm CMOS process, the delay of an inverter is about 30 ps. If we implement Vernier delay-chain TDC, the resolution of the MTDC can be design about 5 ps. Because of the application range and the PVT variations, a 8-bit DCO structure is selected for a reasonable DCO gain (K_{DCO}=200 kHz/Code). The corresponding loop parameters calculated by (3-45) and (3-46) is given by KI_{FC}=10.39≅$2^{3.5}$, K_{ATDC}=51.96 (Δ_{ATDC} =613 ps), K_{PC}=0.0125 (T_{UT}=400 ps). Considering a 8-bit DSM for DCO resolution enhancement, the value of the proportional gain *KP* and integral gain *KI* of DLF are found as *KP*=6.6864≅$2^{2.5}$ and *KI*=0.388≅$2^{-1.5}$ from Eq. (3-47) and Eq. (3.48), respectively. The Bode plot of the ADPLL is shown in Fig. 3-14. With the approximation of power of two, the gain of *KP* and *KI* is able to be implemented as a shifter instead of a multiplier.

In this work, the loop not only switches its bandwidth but also changes to type-I operation during the frequency acquisition mode. And it is known that type-I PLL achieves faster settling time than type-II [4]. Fig. 3-15 illustrates the transient simulation for various frequency hopping distances with Matlab Simulink. Fig. 3-16 illustrates the comparison of the locking behaviors between conventional ADPLL and fast-locking ADPLL with AHDL.



(a)



(b)

Fig. 3-14 Bode plot of the ADPLL in (a) open loop simulation, and (b) closed loop simulation.

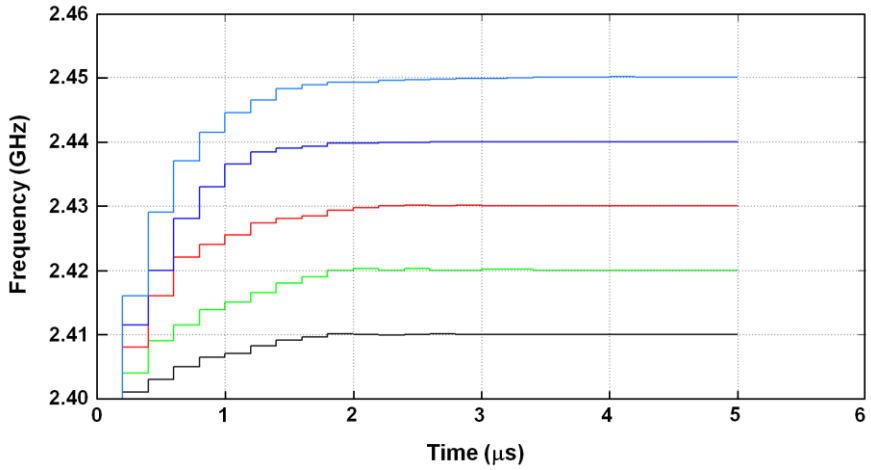


Fig. 3-15 Simulated locking behaviors for various frequency hopping distances.

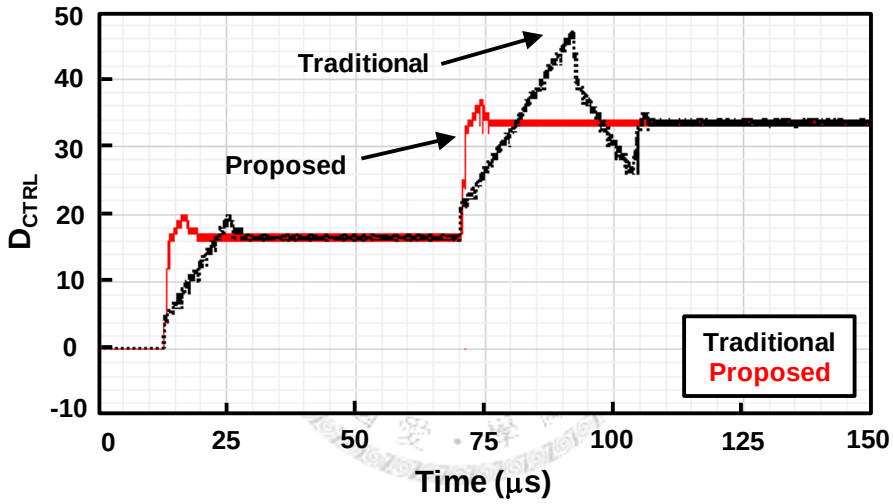


Fig. 3-16 Comparison of locking behaviors between traditional ADPLL and the proposed ADPLL under the same loop bandwidth and damping factor.

Chapter 4
Design and Implementation of the ADPLL

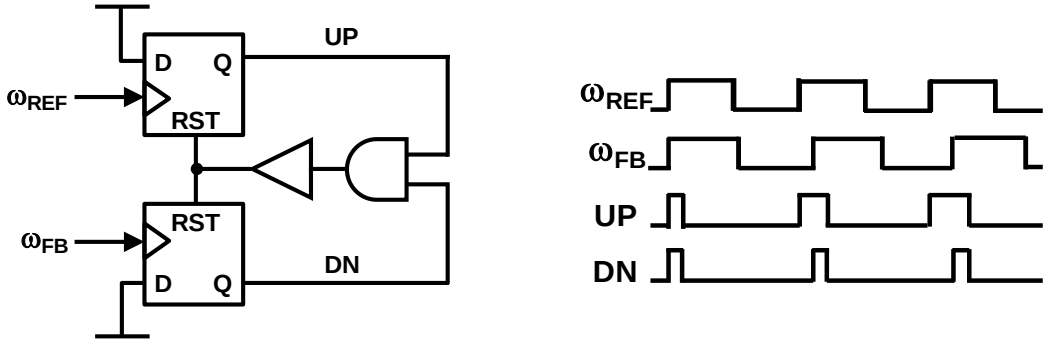
4.1 Circuit Implementations

In order to verify the proposed compensation technique, this work realized a 2.4 GHz low-jitter, fast-locking ADPLL. Fig. 3-6 shows the overall architecture of the proposed ADPLL. Basically, the structure is based on a conventional type-II second-order TDC based digital frequency synthesizer. The traditional phase quantizer is composed of a PFD, phase selector, and a 5-bit TDC (Main TDC, MTDC). The additional timing window is realized by a 3-stage TDC (Auxiliary TDC, ATDC). A first-order PI structure is implemented as a 16-bit DLF and the KI controller determines the frequency capture range. The system calibrates proper loop parameters in order to achieve a low-jitter performance. The DCO core is controlled by 8-bit most significant bit (MSB) output of the DLF and DCO resolution is enhanced by an 8-bit DSM. This section describes the key building blocks design. All the PFD/TDC, divider, DCO, and synthesis circuits are described in detail.

4.1.1 PFD and TDC

The PFD is used to detect the phase and frequency differences between the input reference clock and the feedback output signal of the divider. The circuit of PFD can be realized by various ways. Fig. 4-1 (a) shows a simple implementation consisting of two edge-triggered, resettable D flip-flops (DFF) with their D inputs tied to a logical "high". The DFF is triggered by the rising edge of ω_{REF} and ω_{FB}. Once both UP and DN become logical "high", the two DFFs are reset simultaneously. The related timing

diagrams are shown in Fig. 4-1 (b). The pulse width difference between signal UP and DN reflects the phase error. This information delivers to both MTDC and ATDC. The pulse hold time, which UP and DN are simultaneously in logical "high", is designed long enough to cover the whole MTDC delay range.



(a) (b)

Fig. 4-1 DFF based PFD (a) the block diagram, and (b) the timing diagram.

The 3-stage ATDC is implemented like to a coarse timing window. The main function of the 7-level quantizer is to sense the phase error and generate the proper control code to facilitate fast lock operation. Based on the concept of digital discriminator-aided phase detector (DAPD) described in [17], we design a programmable delay cell using current-controlled bias to cover a desired delay. Fig. 4-2 illustrates a simple current-controlled delay circuit chosen in this work. On the other hand, the proposed MTDC is based on a Vernier TDC with 5-bit uneven-step architecture. However, there are some considerations of the location of deadzone in the transfer curve between MTDC and ATDC. The characteristic curves are shown in Fig. 4-3. In a ATDC design, the deadzone locates on horizontal plane instead of the vertical plane in MTDC. The resolution in an ATDC must be greater than the whole cover range of MTDC for system stability, $\Delta_{ATDC} > (2^5-1)\Delta_{MTDC}$.

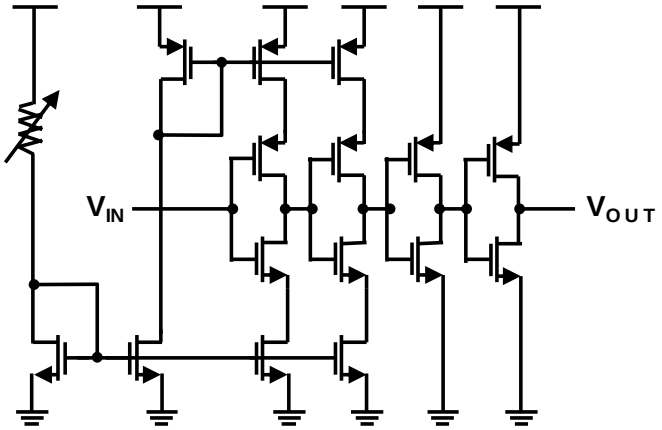


Fig. 4-2 The schematic of the current-controlled delay cell.

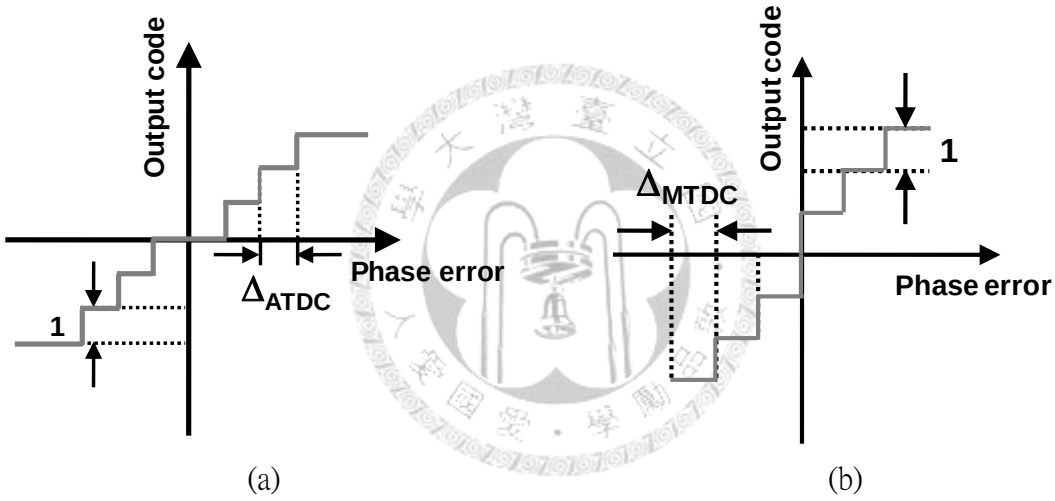
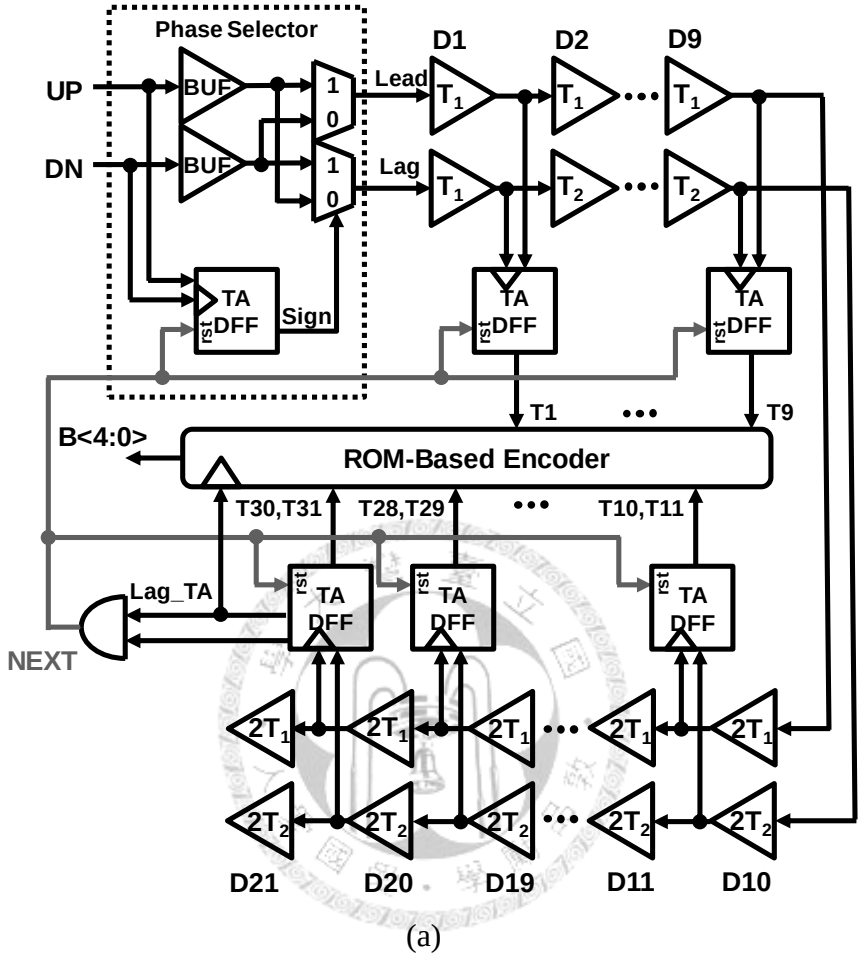


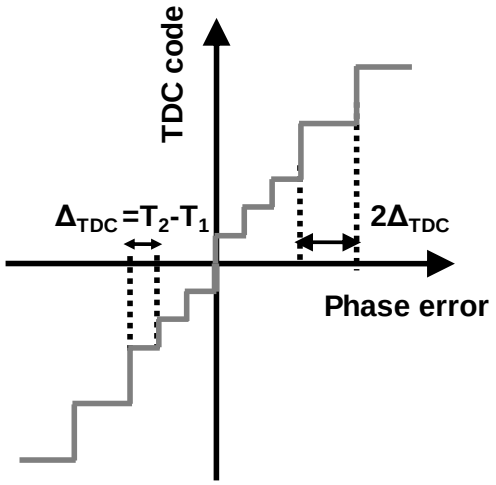
Fig. 4-3 The characteristic curves of (a) auxiliary TDC, and (b) main TDC.

Fig. 4-4 (a) shows the proposed structure of the MTDC circuit including a phase selector. The 5-bit Vernier TDC can only convert the phase difference to digital codes but cannot judge which one is lead or lag. Therefore, a phase selector is implemented to determine the phase relation between *UP* and *DN* and outputs a *Sign* signal to the MTDC [31]. The structure of the phase selector is shown in Fig. 4-4 (a) within a dotted box. It is composed of two multiplexers (MUXs), two buffers (BUFs), a time amplifier (TA), and a DFF. Before each phase comparison, the signal *NEXT* from the MTDC will reset the *Sign* signal to logical "high". If the *UP* signal leads, the decision circuit

(TA+DFF) outputs a logical "low" signal and vice versa. The delay circuit, BUF, is important in ensuring the *Sign* signal arrives earlier than *UP* and *DN*.



(a)



(b)

Fig. 4-4 An uneven-step Vernier TDC in (a) 5-bit architecture, and (b) a conceptual diagram for 3-bit TDC.

A Vernier architecture defines the resolution not by the absolute delay time of a unit cell, but the relative timing difference, which improves the effective resolution. As a result, two-path structure are required doubles power and area of inverter cells. In this work, an uneven-step TDC is implemented to relax this constraint. The transfer curve with a 3-bit uneven-step TDC for conceptual illustration is shown in Fig. 4-4 (b). The complete delay chain has been divided into two segments. The first segment has the shortest delay time cells, which determines the TDC quantization noise in the lock state. The inverter numbers of first segment are designed to cover sufficient delay range due to circuit PVT variation in steady state. The other segment uses cells of double delay time by adding load MOS capacitors to inverter output nodes. The uneven-step architecture extends the detection range, but it will not affect the phase noise performance and result in overall power savings. The circuit operation principle is as follows. The *Lead* signal from the phase selector is sent to the path consisting of T_1 delay cells and the *Lag* signal is sent to the path consisting of T_2 delay cells. The decision circuit detects that the *Lag* signal leads the *Lead* signal and converts the phase error between *Lead* and *Lag* into a set of digital codes with a resolution of Δ_{TDC} ($=T_2-T_1$). When the signals already cross the both delay lines, the *NEXT* signal will reset the phase selector.

Conventionally, a DFF is used as the phase decision circuit in a TDC to quantize the time difference of these two input pulses. To enhance the time resolution, the cascade inverter-based TA is adopted [31]. In our design, it can relax the design limited of TA with a modified ROM-based encoder which includes bubble error removal mechanism and avoiding metastability. The bubbles, or called sparkles, usually occur near the transition point of the thermometer code. In the conversion of thermometer to 1-of-N code, the bubble error can be removed by adding a three-input

NAND. On the other hand, an efficient technique by employing Gray coding as an intermediate step between the thermometer and binary codes can avoid metastability occurrence.

The input/output characteristic simulation result is shown in Fig. 4-5. The resolution of this MTDC is around 5 ps. From Eq. (2.4), the phase noise introduced by the TDC is –100.23 dBc/Hz.

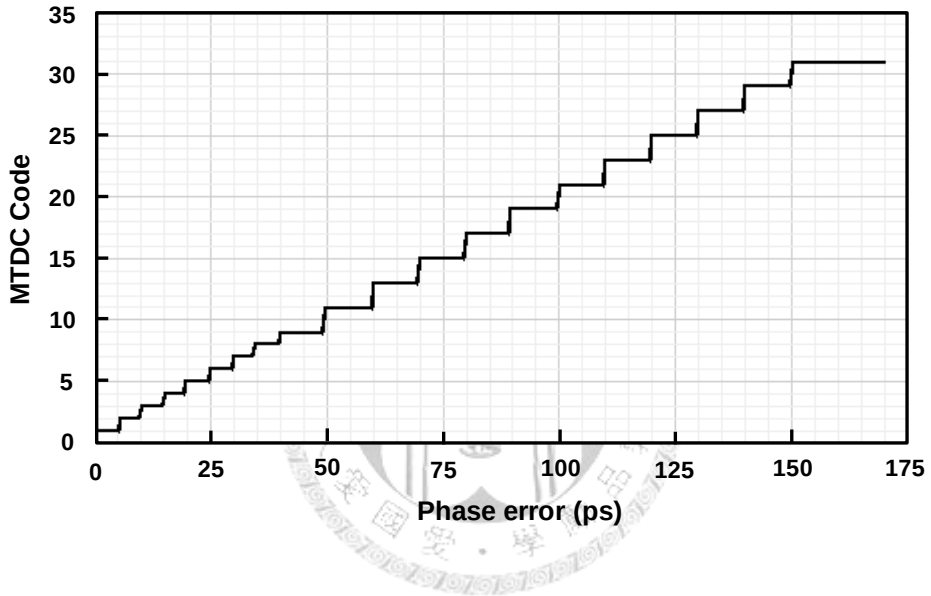


Fig. 4-5 The simulation result of 5-bit uneven-step TDC.

4.1.2 Divider

Based on the prior work [16], the multi-modulus divider is modified as shown in Fig. 4-6 in order to dynamically change the divide ratio to compensate phase error. It incorporates a shift register array and control logics. Rather than using the mode control signal to force the divider ratio, the shifter register array and control logic are employed following the digital code comparator to process this mode control signal (*MD1*). The control logic is formed by a MUX and a decoder. The MUX in the control logic would select one shifter output (C_1-C_6) as mode signal (*MD2*) according to the

ATDC results (OUT_{ATDC}) and *Sign* signal. Then, the generation of the ÷3/4 divider is controlled by this new mode control signal, *MD2*.

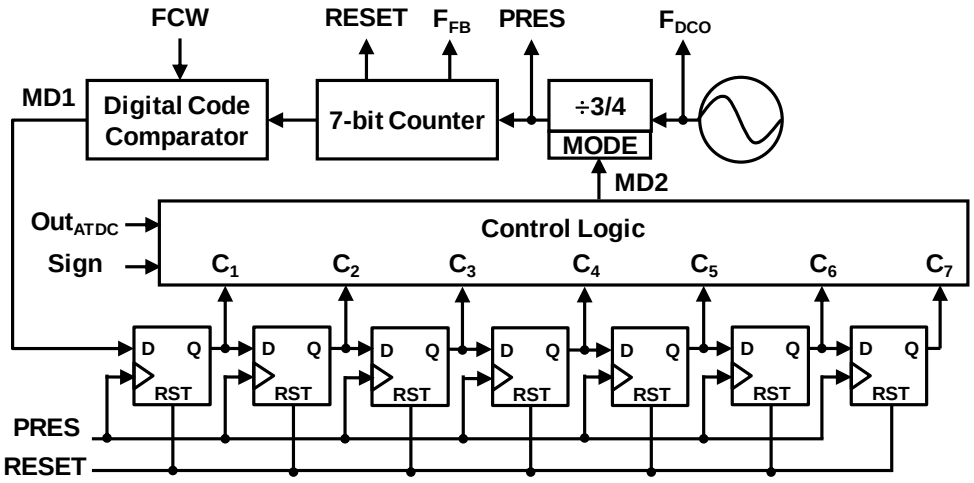


Fig. 4-6 Modified programmable divider for phase compensation purpose.

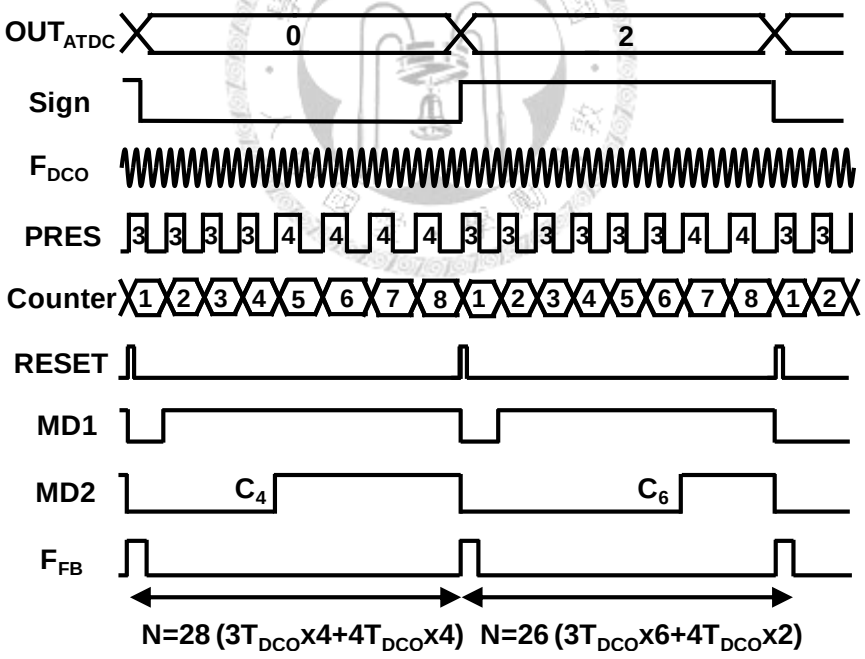


Fig. 4-7 The design of divider chain: an example illustrated by timing diagram with 3-bit counter.

An example of operation timing diagram is described in Fig. 4-7. For illustration purpose, this example uses a 3-bit counter as an example. First, the *RESET* signal would reset all registers; *MD1* and *MD2* are forced to logical "low". Then, the counter

begins to count the number of pre-scaler output, *PRES*. The signal *MD1* is switched to logical "high" when the counter reaches to "1". In the locked state, the control logic selects C_4 as *MD2* signal, and the dual-modulus performs both ÷3 and ÷4 for four times, which accomplishes a divide ratio of 28. When the fast-locking operation is activated, the divide ratio decreases by two via selecting C_6 as *MD2* signal. In general, the final divide ratio can be rewritten by

$$N = \left(\left(C_n + C_i\right)\times 3\right) + \left(2^k - \left(C_n + C_i\right)\right)\times 4, \tag{4-1}$$

where C_n is the additional amount in phase error compensation path and C_i is the shifted cycle number of mode control signal in the pre-scaler circuit.

For further lowering power dissipation, the ÷3/4 dual-modulus divider in this work is designed as Fig. 4-8 (a), which is improved from that presented in [17]. The main notion of this pre-scaler is to delay the signals, A_D-D_D, on the latched inverter path by half of the input clock and then to obtain a frequency-divided signal. The divide mode is forced by mode control signal, *MODE*. When the mode control signal is maintained as a logical 'high' signal, the delayed signal passes three latches instead of all latches as depicted in Fig. 4-8 (b) and results in a ÷3 mode. Otherwise, the M_N is turned on if the mode control signal translates into logical 'low'. The operated timing diagram under ÷4 mode is shown in Fig. 4-8 (c). When the C_D is logical 'high', the D_D will become logical 'low' at next rising edge of *IN*. Since D_D is logical 'low' and M_N is turned on, the *OUT* would be pulled up directly and the A_D then translates into logical 'low' at the same moment. Hence, one input cycle is swallowed and sequentially results in a ÷4 mode. The main challenge in this circuit is required to ensure a correct cycle-swallow behavior during the half of input cycle. To solve this issue, this work adds an extra transistor M_P. Since this M_P exists, the A_D can be continuously charged even input clock signal is raised. Thus, it can relax the timing constrain on the duty

cycle of input signal since this circuit has enough time to pull down A_D under the operation of ÷4 mode.

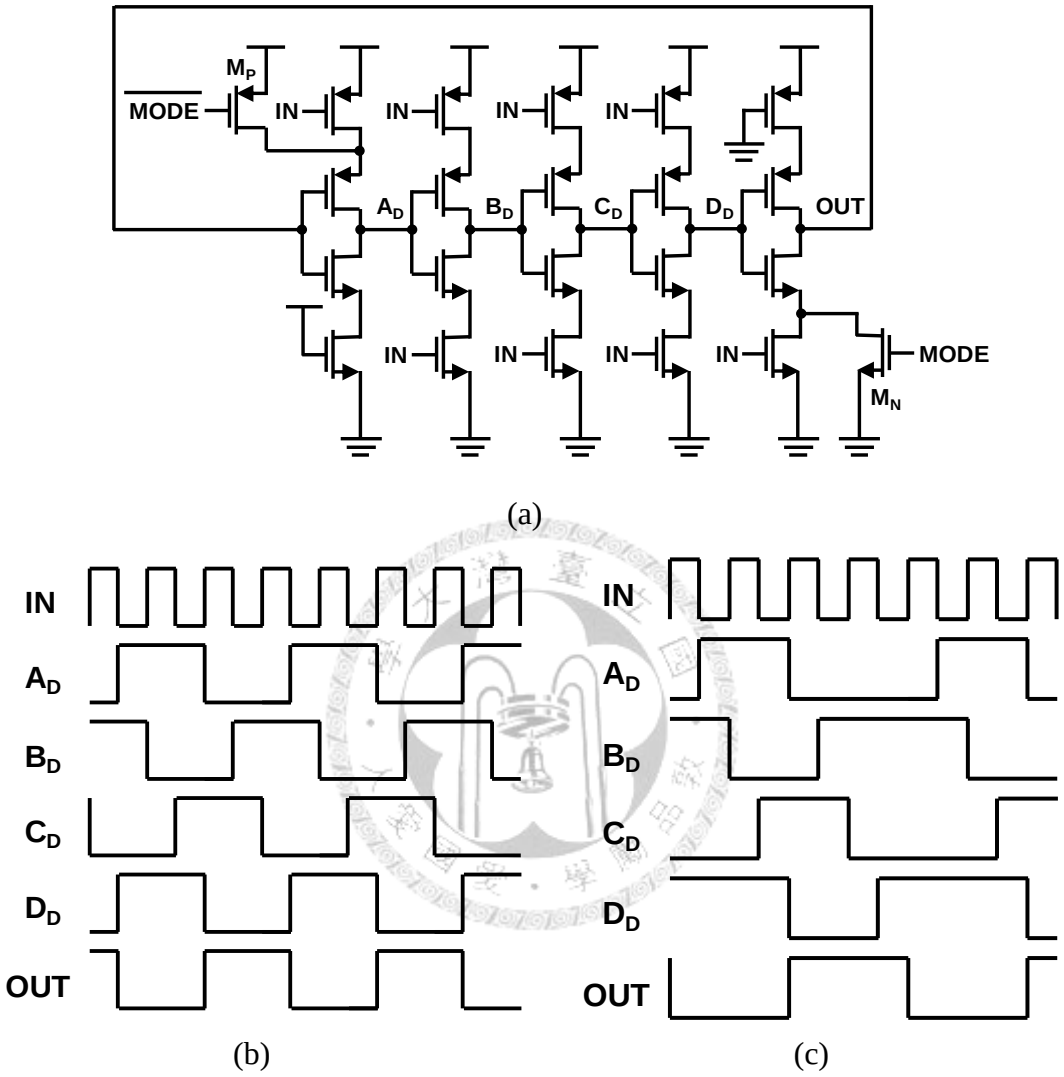
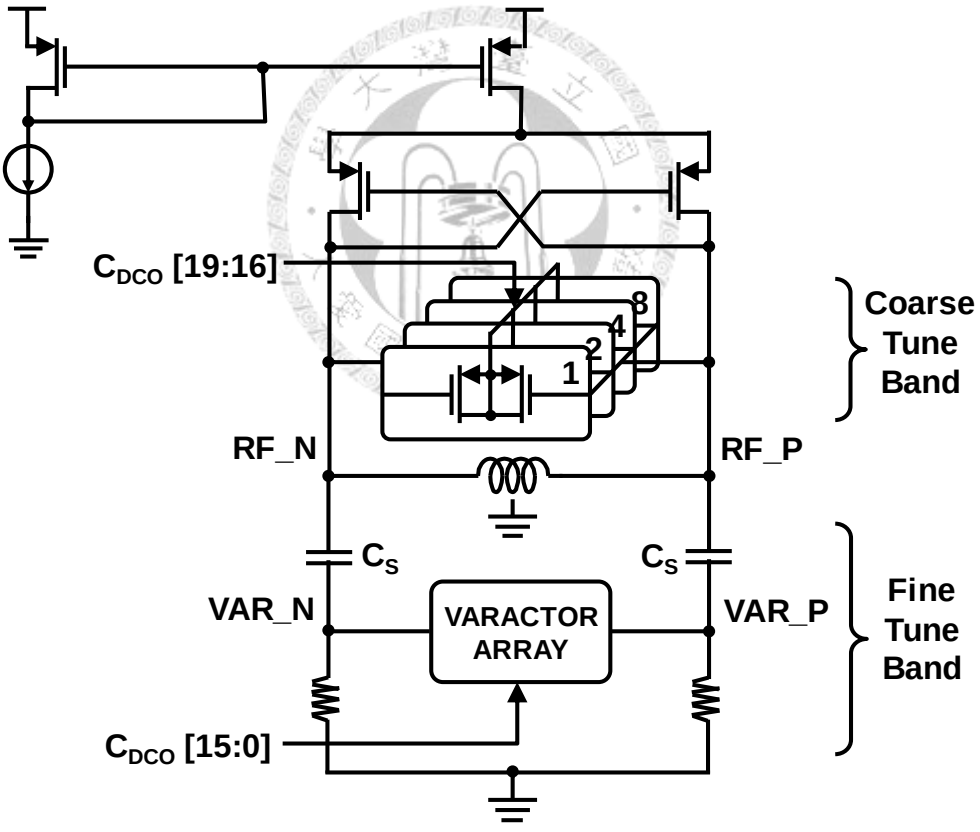


Fig. 4-8 The modified ÷3/4 dual-modulus divider: (a) the modified structure, (b) the operated timing diagram under ÷3 mode, and (c) the operated timing diagram under ÷4 mode.

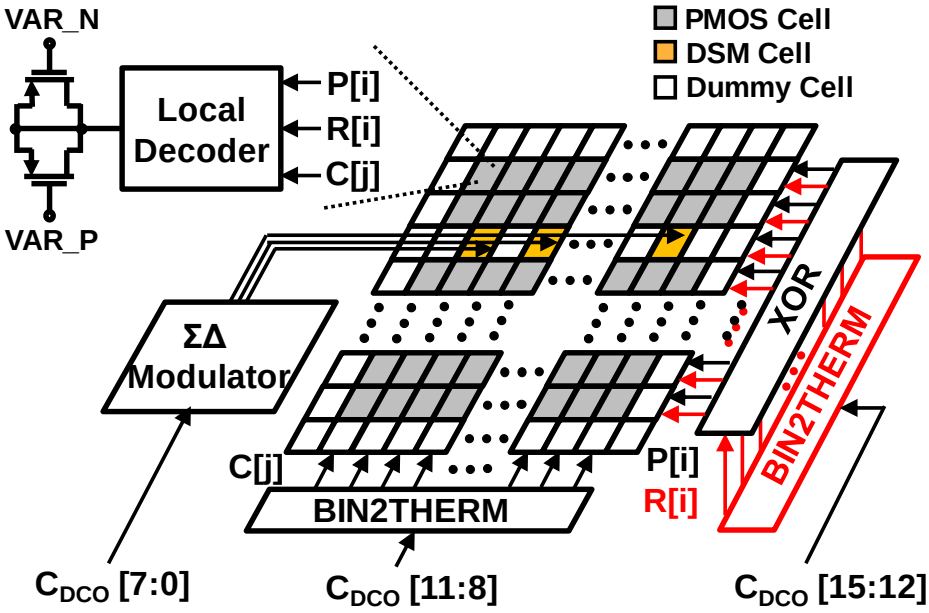
4.1.3 DCO

In this section, the design and implementation of the digital-controlled oscillator (DCO) will be illustrated. Without a doubt, DCO is the most critical component of the ADPLL. If the noise performance of free-running oscillator is extremely poor, it will not be possible to realize PLLs meeting reasonable performance specifications for

wireless applications. Two main approaches to realizing the DCO are discussed in [37]. The result selects the directly-digitalized oscillator instead of the hybrid approach (DAC+VCO) on account of issues of power and phase noise. For the consideration, the implemented block diagram of the LC-tank DCO system is shown in Fig. 4-9 (a). The DCO receives a 16-bits wide control word C_{DCO}[15:0] from the loop filter without the sign bit and delivers a differential signal with frequency around 2.4 GHz to the buffers. The only obviously disadvantage of the mechanism is the large occupied area. The integrated inductor and the tank varactor broken into a number of smaller units take the most of the area in LC-tank DCO.



(a)



(b)

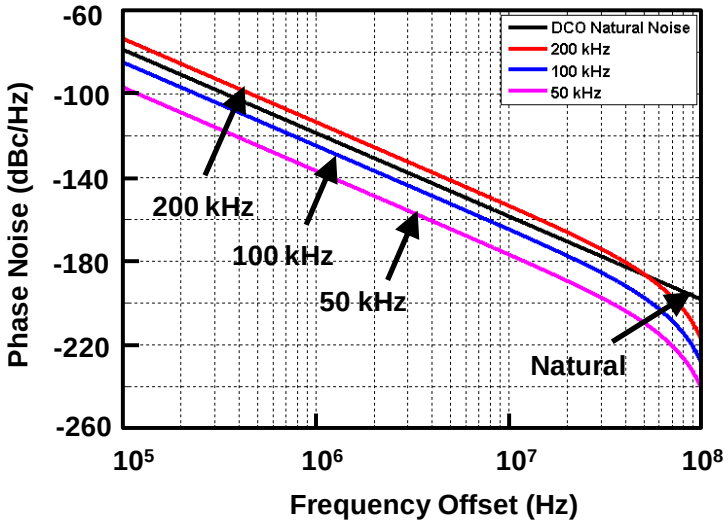
Fig. 4-9 Implemented block diagram of DCO system: (a) architecture, and (b) varactor array.

The topology incorporates a cross-coupled PMOS pair with a switched capacitor bank and a symmetrically laid out octagonal inductor. The cross-coupled pair forms a negative resistor to eliminate the parasitic resistors in capacitor and inductor. The reason of choosing PMOS as cross-coupled pair rather than NMOS is that PMOS pair has the benefit of less substrate noise coupling, because it resides in an N-well. In order to achieve a low phase noise performance, the inductor should have a high quality factor. Instead of two separate identical inductors, the symmetric with center-tapped inductor fabricated in TSMC 0.18 μm 1P6M process is chosen. In this work, a passive inductor with quality factor around 11 and the nominal bias current is 5 mA.

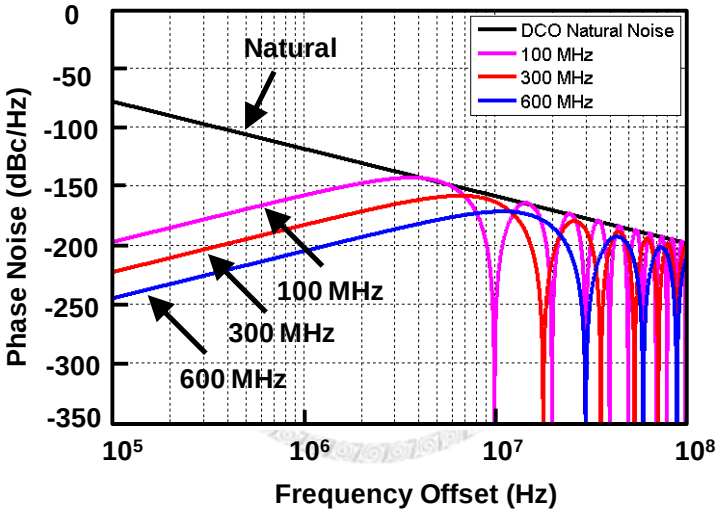
In the traditional voltage-controlled LC oscillator, frequency tuning is controlled by the effective tank capacitance with an analog control signal. The variable capacitor is typically implemented with p-n junction diodes or the MOS varactors which has a non-linear relationship between the capacitance and the tuning voltage. In the concept

of the digital tuning, the oscillator frequency is made to be proportional to the input digital control word C_{DCO}. To achieve digital tuning of the oscillation frequency, the varactor can be used but only two voltage levels are applied. In the implemented varactor array, PMOS with control signal short to drain and source is used as the inversion-mode bank and each unit operates in either high or low capacitance state. The fine frequency resolution in fine tune bank can be acquired by controlling the amount of the varactors in different states.

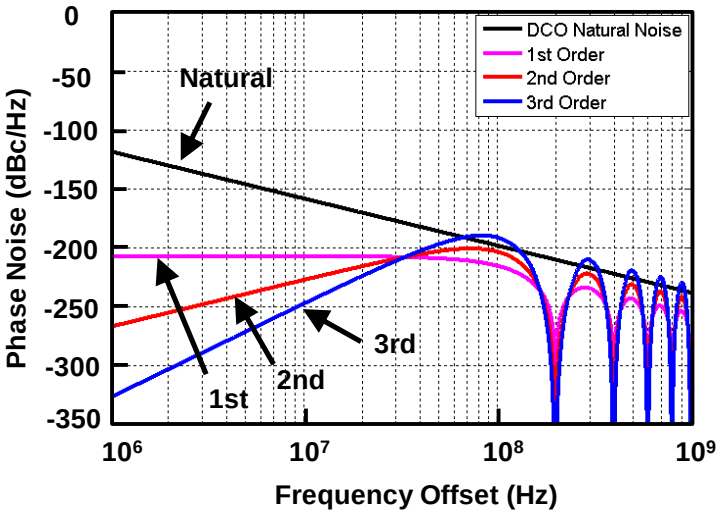
When implementing a DCO, the frequency range might drift due to the process variation, temperature, and some environmental factors. In order to lower the area and the parasitic capacitances of the varactor bank, the whole bank is divided into two different weighted sub-banks. The varactor bank incorporating 4-bits binary-weighted coarse tuning which has sixteen turning curves to cover the required tuning range and a 8-bits unity-weighted fine tuning to ensure linearity. The 4-bit DCO band selection is set by serial-in parallel-out (SIPO) from external tuning. As shown in Fig. 4-9 (b), the second bank arrangement would organize a matrix of 16X16 in order to optimize the layout matching. For fine frequency resolution, the size of the PMOS varactor is close to the minimum allowed by the technology. The gate terminals of the units are shorted together and AC coupled to the tank through a series capacitor, C_s. This parameter design is a trade-off between resolution and linearity. The binary weighted control code $C_{DCO}[15:8]$ is first converted to thermometer code and then the tuning information $R[15:0]$, $P[15:0]$ and $C[15:0]$ are latched to eliminate glitches due to different propagation times of the converters. It can save routing down to only 48 control lines by the local decoders ($R[i]+P[i]C[j]=1$). The similar topology and the dummy cells on the boundary of the array are taken in the literature [11].


DCO Natural Noise
200 kHz
100 kHz
50 kHz
200 kHz
100 kHz
50 kHz
Natural
Phase Noise (dBc/Hz)
Frequency Offset (Hz)

(a)


DCO Natural Noise
100 MHz
300 MHz
600 MHz
Natural
100 MHz
300 MHz
600 MHz
Phase Noise (dBc/Hz)
Frequency Offset (Hz)

(b)


DCO Natural Noise
1st Order
2nd Order
3rd Order
Natural
1st
2nd
3rd
Phase Noise (dBc/Hz)
Frequency Offset (Hz)

(c)

Fig. 4-10 Phase noise due to frequency quantization with (a) different frequency resolution step, (b) different dithering frequency of ΣΔ modulator, and (c) different order of ΣΔ modulator.

To have insight into the quantization effect on the DCO phase noise due to finite frequency resolution, the process can be modeled as an infinite-precision tuning signal added by an uniformly distributed random variable with white noise spectral characteristics [13] :

$$L_{Quantize}(\Delta f) = \frac{1}{12} \times \left(\frac{\Delta f_{res}}{\Delta f} \right)^2 \times \frac{1}{f_{REF}} \left(2sinc \frac{\Delta f}{f_{REF}} \right)^2 . \quad (4\text{-}2)$$

The output phase noise due to the finite quantization error can be expressed as above. Δf_{res} is the DCO quantization step which indicates the corresponding frequency deviation of one DCO control code. It can be seen that the output phase noise from quantization process can be reduced by increasing the DCO frequency resolution. The resulting phase noise must be contributed below the natural DCO phase noise resulted due to the finite quality factor of the LC tank and noise of active devices. And the phase noise of the LC tank oscillator can be expressed in Eq. (3-30). The phase noise spectrum due to frequency quantization is shown in Fig. 4-10 (a). This result suggests that the multiplication of DCO gain (K_{DCO}) should be design low enough. Finer resolution can be accomplished by means of high speed ΣΔ dithering with the equation, $\Delta f_{res,eq} = \Delta f_{res,d} / 2^{WF}$, where $\Delta f_{res,d}$ is the frequency step without utilizing dithering function and *WF* is the word length of the ΣΔ system.

Fig. 4-10 (b) shows the phase noise spectrum due to ΣΔ-shaped frequency quantization with different dithering frequency. The quantization noise energy induced by finite frequency step is moved toward the high frequency offset at the RF output

due to the noise shaping capability of the modulator. The phase noise spectrum due to the ΣΔ-shaped frequency deviation is

$$L_{\Delta\Sigma}(\Delta f) = \frac{1}{12} \times \left(\frac{\Delta f_{res}}{\Delta f} \right)^2 \times \frac{1}{f_{dth}} \times \left(2 \sin \frac{\pi \Delta f}{f_{dth}} \right)^{2n} . \quad (4\text{-}3)$$

where f_{dth} and n denote the sampling frequency and the order of the ΣΔ modulator, respectively. f_{dth} is normally much higher then f_{REF} and can be easily derived from DCO by dividing the DCO output signal. In consideration of speed requirements in fully synthesized digital logic, choosing a suitable specification for ΣΔ modulator. Fig. 4-10 (c) shows the phase noise spectrum due to ΣΔ-shaped frequency quantization with different order modulators.

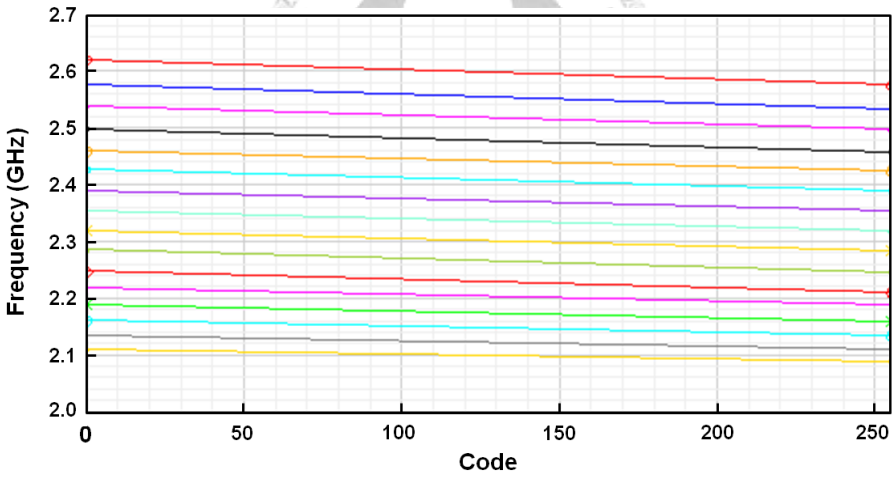


Fig. 4-11 The DCO tuning curves simulation results.

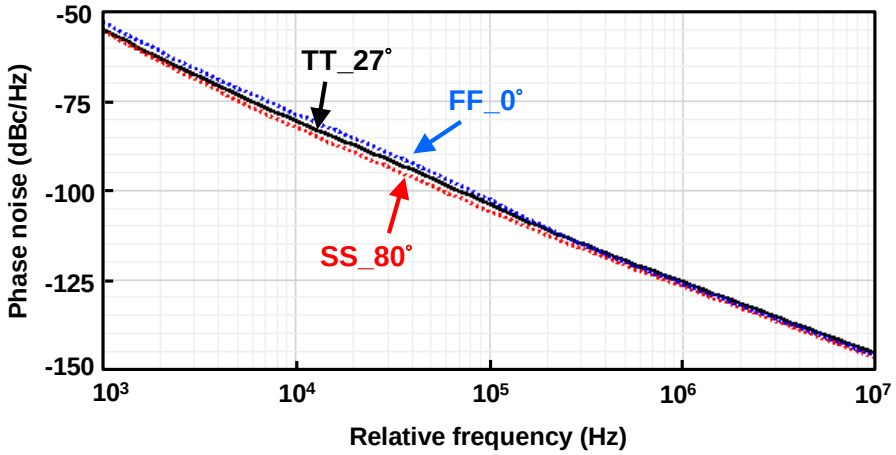


Fig. 4-12 DCO phase noise simulation results.

Fig. 4-11 depicts the post-simulated code vs. frequency characteristic using Cadence SpectreRF in TT corner. The other two extreme corners, SS and FF, are also simulated to make sure the operation frequency of DCO can work for 2.4 GHz ISM band application under PVT variation. Each band will overlap with the neighboring bands by at least 40%. The simulated gain of DCO is about 170 kHz/Code at TT corner. The design target in phase noise at 100 kHz and 1 MHz offset frequency is below -100 dBc/Hz and -125 dBc/Hz, respectively. The phase noise performance is simulated under different corners and parasitic capacitances are considered. The simulation results are shown in Fig. 4-12.

4.1.4 DLF and Delta-Sigma Modulator (DSM)

The DLF and DSM are synthesized by standard cells with Verilog code. The block diagram of the DLF is drawn in Fig. 4-13. The DLF is a programmable, discrete time PI filter that operates at the divided output clock frequency. The integral section of the loop filter accumulates the error coming from the MTDC multiplied by a dynamic gain controller based on output of ATDC. When the adder detects overflows or underflows, a corresponding signal is asserted, and the DCO control code maintains constant. The oscillator tuning word is split into two components, integer part and

fractional part. The integer part is thermometer-encoded to control the same size DCO varactors of an LC tank oscillator. The fractional part, on the other hand, employs a time-averaged dithering mechanism to further increase frequency resolution. The digital second-order MASH-type ΣΔ modulator architecture with a dithering input function is shown in Fig. 4-14.

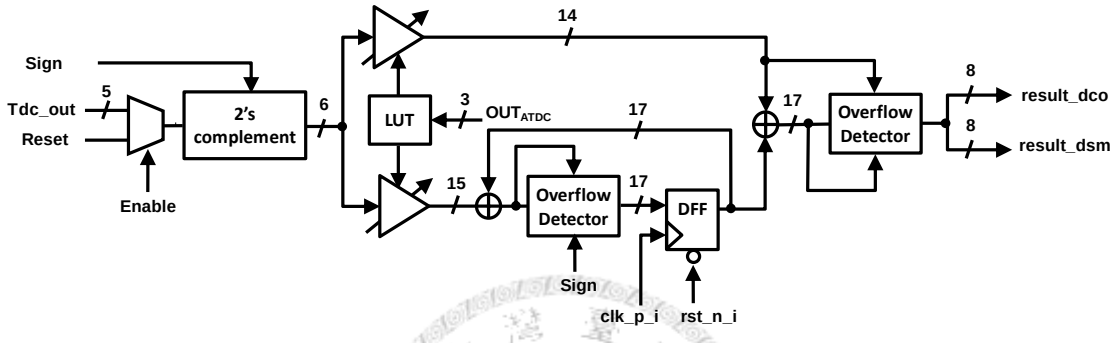


Fig. 4-13 Block diagram of the DLF for a type-II second-order ADPLL.

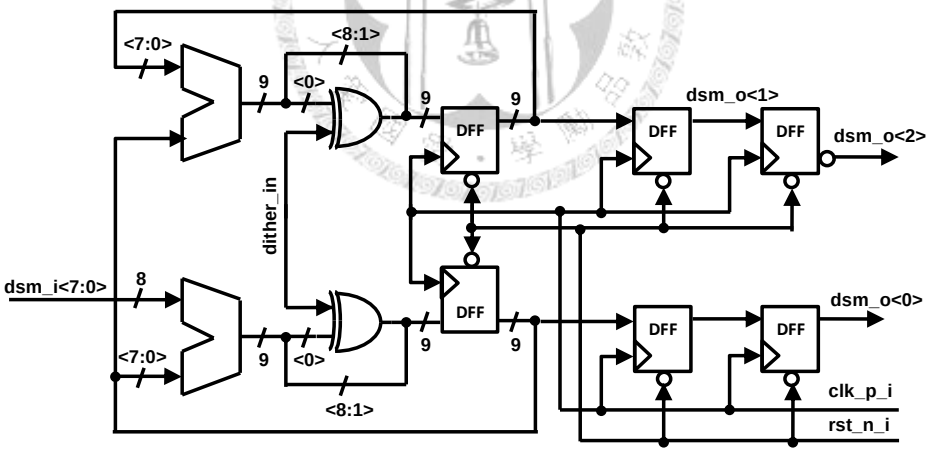


Fig. 4-14 Block diagram of the second-order MASH-II ΣΔ modulator.

Chapter 5

Experimental Results

5.1 Test Setup

Fig. 5-1 shows the testing environment to evaluate the transient and spectrum performance of the proposed ADPLL. Several regulators or batteries are adopted to provide DC biases. The single-ended output RF signal is fed into signal source analyzer (R&S FSUP26) to measure phase noise and spectrum, and signal source analyzer (Agilent E5052A) to measure transient locking behavior, and oscilloscope (Agilent 86100C) to measure timing jitter of this ADPLL.

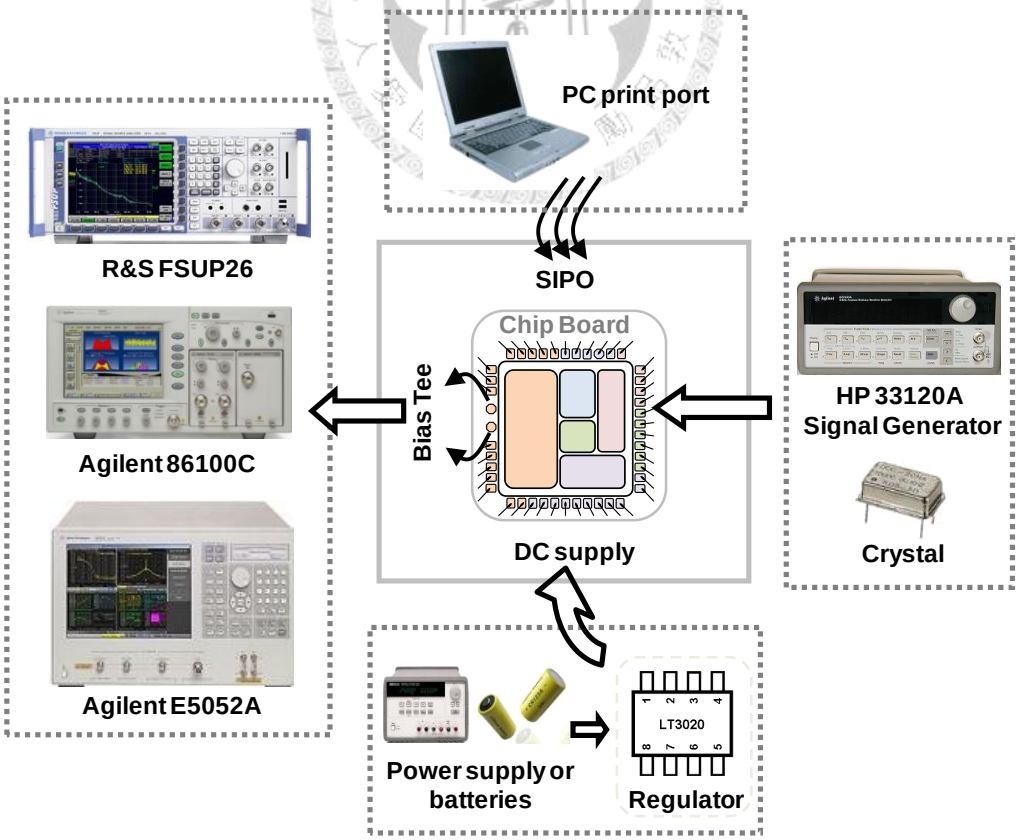


Fig. 5-1 Measurement setup.

5.2 Chip Pin Configurations and Printed Circuit Board Design

5.2.1 Chip Pin Configurations

Fig. 5-2 shows the pin configurations and the chip power-domain distribution. To alleviate unwanted noise coupling through power lines, there are five separate power domains in the chip: VCO, divider, PFD/ATDC, MTDC and synthesis domains.

Integrated circuits are susceptible to damaging electro-static discharge (ESD) pulses from the operating environment and peripherals; hence, ESD-protection PADs and power rings are integrated to protect the chip I/O interface. Fig. 5-3 displays the die photograph of this chip, which was fabricated in TSMC 0.18 μm 1P6M CMOS mixed-signal process. The chip including ESD-PADs occupies an area of 1370 μm × 1300 μm.

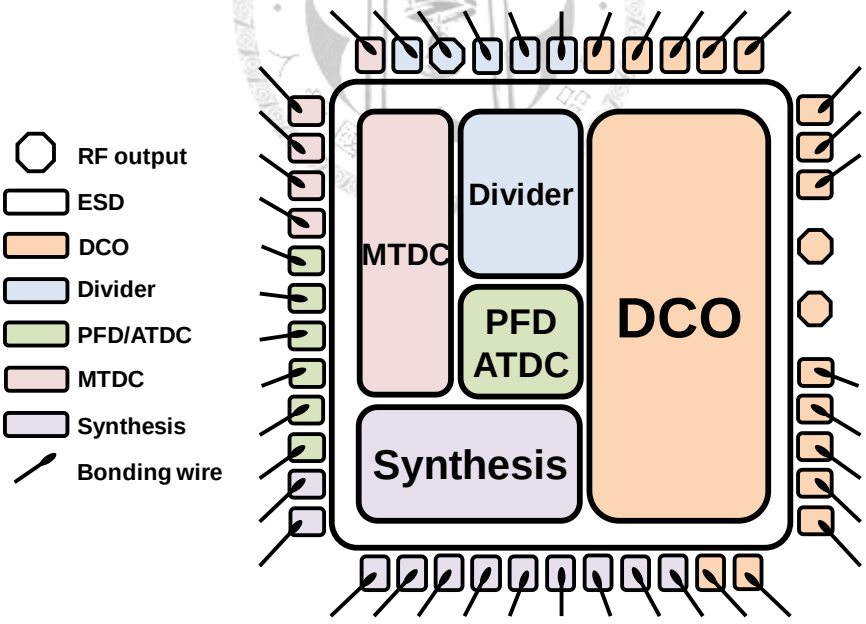


Fig. 5-2 Pin configurations and power domain diagram.

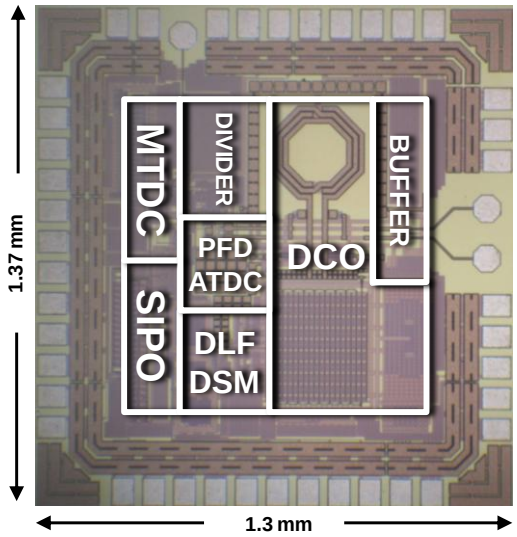
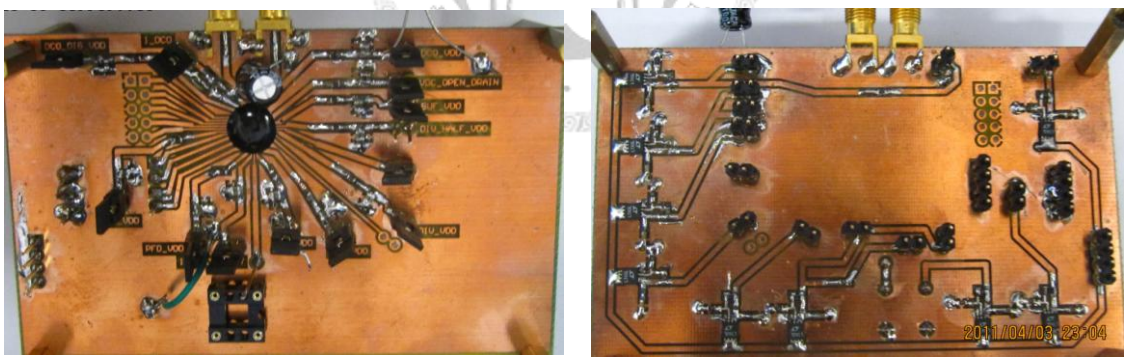


Fig. 5-3 Die photo of this work.

5.2.2 Printed Circuit Board (PCB) Design

Fig. 5-4 shows the fabricated PCB for measurement. A two-layer FR-4 glass-epoxy double-sided laminate (ε_r = 4.4) is used for the chip testing.



(a) (b)

Fig. 5-4 Fabricated PCB for measurement: (a) top view, and (b) bottom view.

The PCB design focuses on four issues: the separation of different power domains, the proper routing of RF signals, the convenience of chip function verification, and the reduction of noise coupling. First, the supply voltages or DC biases are generated by regulators as shown in Fig. 5-5. Further, the differential RF output signals are fed into

two balanced ports of an off-chip Bias Tee, and then the unbalanced port of the Bias Tee as an output is connected to a surface mount adaptor (abbr. SMA) for measurement. This single-ended RF signal on the board runs at frequencies around 2.4 GHz, and the width of this RF trace is designed to ensure 50 Ohms characteristic impedance.

5.3 The DC supply Regulator

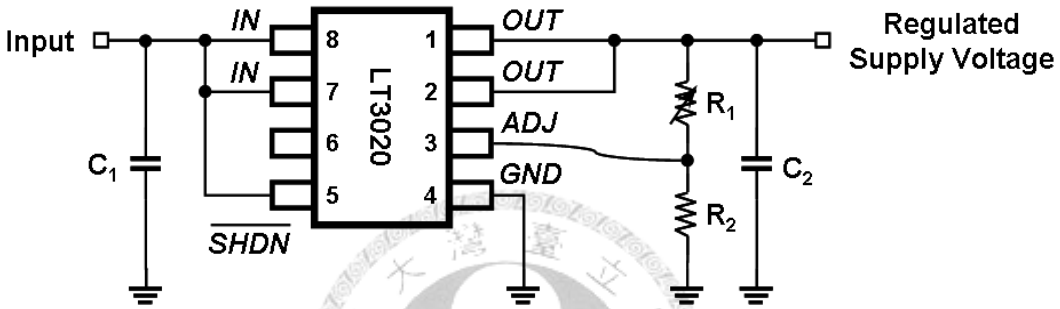


Fig. 5-5 Schematics of LT3020.

LT3020, as shown in Fig. 5-5, can provide a very low supply voltage, 200 mV. In addition, LT3020 can be used to provide a low noise voltage. The input bypass capacitor C_1 (minimum is 2.2 μF) is added for stability. The output capacitor C_2 is needed to stabilize loop response and to improve the transient response. With an unregulated 3 V voltage from Agilent E3646A, the regulated output voltage can also be adjusted by an external resistor divider, where R_1 is a variable resistor and R_2 is a fixed resistor with 20 kΩ resistance. Additionally, the quiescent current through this resistor divider is about 10 μA with a 1.8 V regulated output voltage.

5.4 Experimental Results

The proposed 2.4 GHz ADPLL was fabricated in a 0.18 μm CMOS process. The whole system consumes 10.35 mA from a 1.8 V supply. The DCO has a 4-bit switched-capacitor array to cover a frequency range from 2.39 GHz to 2.65 GHz. The gain of DCO is about 195 kHz/V.

5.4.1 Lock Time Measurement Results

In this work, two different locking modes, conventional type-II ADPLL and the proposed compensation technique, are incorporated into one chip to compare their settling time. Fig. 5-6 shows ADPLL settling behavior comparison under different locking methods based on the same loop bandwidth. The results are measured by monitoring the DCO output frequency to observe the locking process. The ADPLL steady-state loop bandwidth is chosen to be 100 kHz and the frequency hopping distance is 10 MHz in this example. Without any fast-locking technique, the conventional ADPLL takes around 270 μs. When the proposed technique is applied, the settling time is significantly reduced to about 5 μs, achieving more than 50×improvement of settling time over a typical ADPLL.

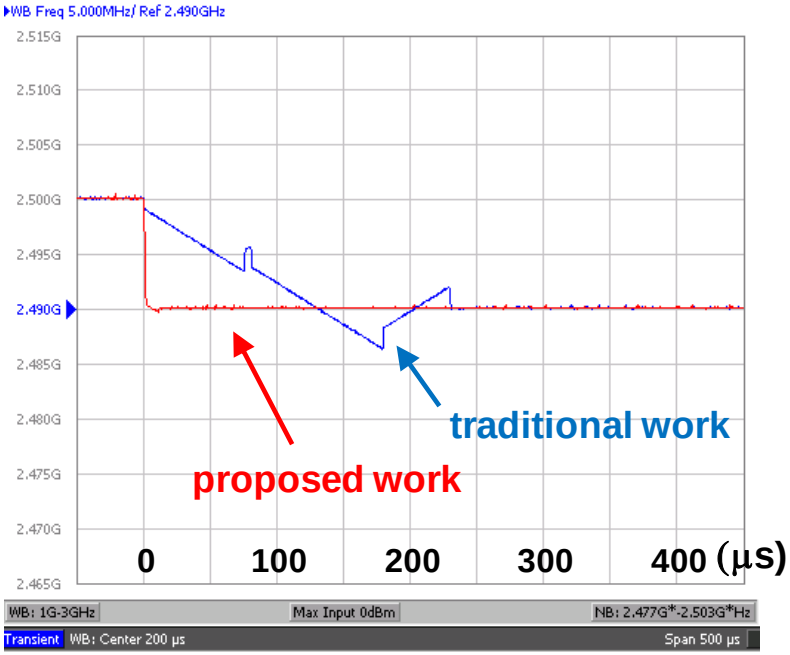


Fig. 5-6 The comparison on settling behavior under different approaches by monitoring DCO output frequency to settle within ±100ppm of desired frequency. (blue: traditional work, and red: proposed work).

Fig. 5-7 shows the settling process under different hopping frequency steps in the proposed ADPLL. The equivalent loop bandwidth during frequency acquisition mode is 300 kHz. As the hopping distance becomes larger, the integrated phase error at PFD input is increased. In the proposed method, a larger gain (KI_{FC}) in KI controller is applied, and then results in a sharper rise of the DCO control code. Meanwhile, the phase error is continuously compensated through adjusting the divide ratio. As the frequency is close to the desired target, the loop quickly converges since the phase error is kept small throughout the acquisition process. The fast-locking module is turned off when the loop is locked. Therefore, it does not affect the ADPLL noise performance.

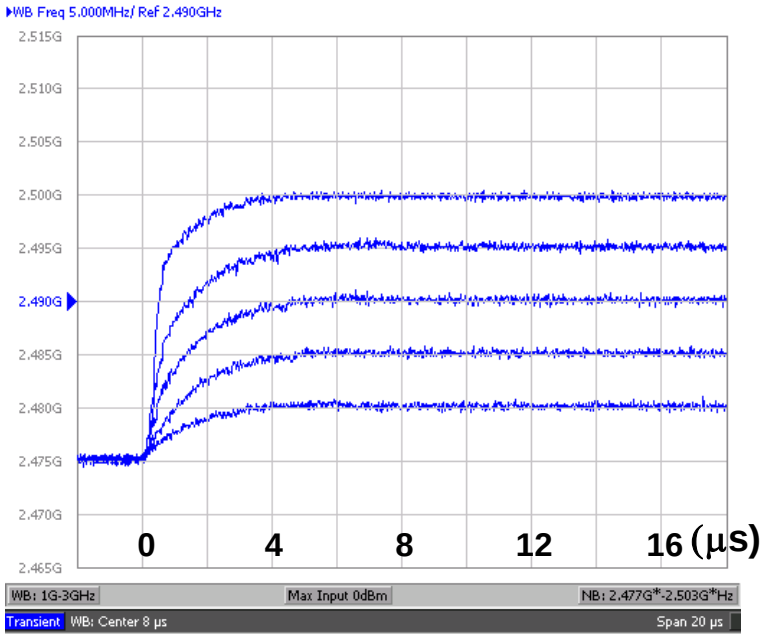


Fig. 5-7 The settling behavior under different hopping frequency by using the proposed dynamic phase control technique.

5.4.2 Timing Jitter Measurement Results

Fig. 5-8 is the jitter histogram of the output of the proposed ADPLL. It shows the peak-to-peak jitter is 1.92 ps at 2.49 GHz. Due to the higher multiplication number and the nonlinearity of DCO tuning curve, the low frequency component noise is higher, which leads to degradation of timing jitter. The jitter performance has an optimum design with a set of loop parameters (*KI*, KP_{opt}). While keeping *KI* constant, a smaller *KP* causes the frequency peaking in system spectrum which makes the rms jitter increase exponentially for $KP<KP_{opt}$. On the other hand, increasing *KP* value makes the loop dynamics to be dominated by the quantization step in the proportional gain, leading to linear increasing of the output jitter.

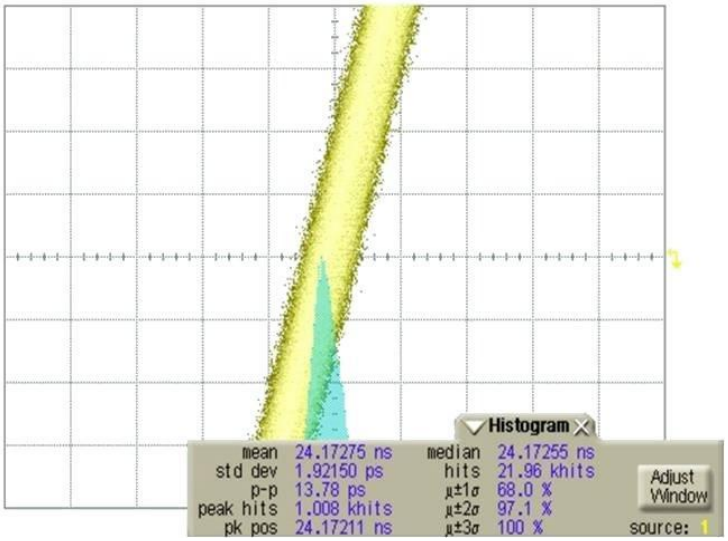


Fig. 5-8 The measured jitter histogram.

5.4.3 Phase Noise and Reference Spur Measurement Results

Fig. 5-9 shows the measured phase noise at 2.49 GHz. At 100 kHz and 1 MHz offset frequencies, the phase noise is -79.6 dBc/Hz and -112.7 dBc/Hz, respectively. The VCO dissipates 4.97 mA. Fig. 5-10 shows the PLL output spectrum at 2.49 GHz with a reference frequency of 5 MHz. With a loop bandwidth of 100 kHz, the reference spurs are lower than -50 dBc.

The phase noise is degraded as compared with the pre-simulation result. Better phase noise value is obtained for higher output frequency where the varactor banks are in low capacitance mode. When the MOS in the varactor bank enters invertion mode, the energy loss due to the effective resistance of channel and metal connections would increase. Thus, the quality factor of the LC tank reaches its minimum value at high capacitance state when the output frequency is the lowest. Others possible reasons are that the dithering frequency is not high enough and non-ideal layout.

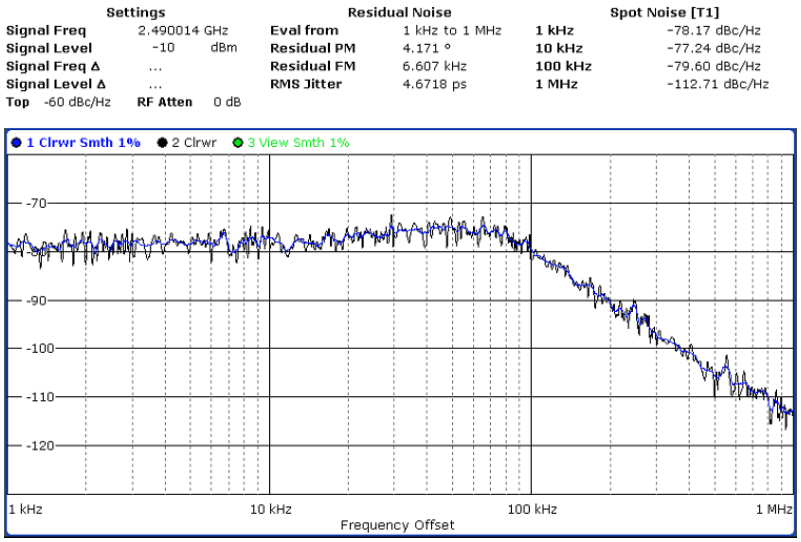


Fig. 5-9 The measured phase noise at 2.49 GHz output frequency.

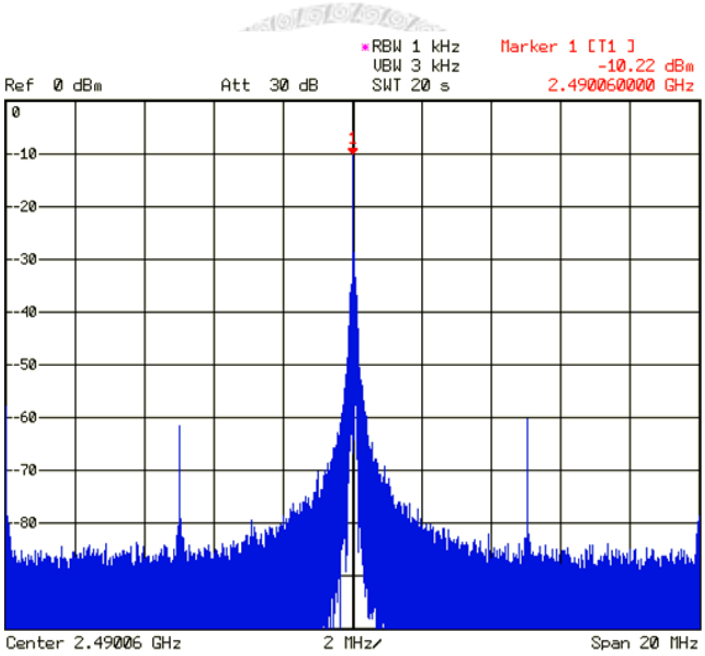


Fig. 5-10 The measured output spectrum at 2.49 GHz output frequency.

5.5 Summary of Measured Results

Table 5-1 summaries the measured performance summary and Table 5-2 summarizes the ADPLL performance and compares with the state of the art in the literature. The proposed architecture manifests the low-jitter, fast-locking ADPLL in highest multiplication factor.

Table 5-1 Measured performance summary

Process	TSMC 0.18 μm 1P6M CMOS	
Supply Voltage	1.8 V	
Output Frequency	2.39 GHz ~ 2.56 GHz	
Reference Frequency	5 MHz	
Tuning Gain of DCO	195 kHz/V	
Loop Bandwidth	100 kHz	
Phase Noise	-79.60 dBc/Hz at 100 kHz	
	-112.71 dBc/Hz at 1 MHz	
Reference Spurs	< -50 dBc	
Chip Area	1.37 mm × 1.30 mm	
Current Consumption	DCO	4.97 mA
	Divider	2.14 mA
	MTDC	0.20 mA
	PFD+ATDC	0.91 mA
	DLF+DSM	2.13 mA
	Total	10.35 mA
Timing Jitter	1.92 ps_{rms}	
Settling Time	Conventional	270 μs
	This Work	5 μs

Table 5-2 ADPLL performance comparison

Process	This work	JSSC'10 [38]	ISSCC'10 [39]	ISSCC'08 [40]	ISSCC'06 [41]
Process (nm)	180	130	65	130	180
Supply (V)	1.8	1.2	1.1	1.5	1.8
Output freq. (GHz)	2.49	1.35	3	3.67	2.4
Divider ratio	498	27	120	74	N.A
Lock time (μs)	5	7.5	N.A.	20	N.A.
RMS jitter (ps)	1.92	3.7	1.4	N.A.	3.29
Power (mW)	18.63	16.5	10.23	39	25
FoM	-221.63	-216.46	-226.98	N.A.	-215.68

$FoM = 10\log\left[\left(\frac{\sigma_t}{1s}\right)^2 \cdot \left(\frac{P}{1mW}\right)\right]$ from Eq. (3-35).

Chapter 6
Conclusions and Future Work

6.1 Conclusions

In this thesis, a proposed ADPLL with dynamic phase compensation is implemented to optimize lock time. The adjustment mechanism of loop filter parameters to prevent frequency peaking phenomenon is employed in locked state. The scheme proves fast locking speed without degrading jitter performance by switching appropriate modes. This technique utilizes a programmable timing window to modify divider ratio. The uneven-step TDC with modified encoder relaxes the design limit effectively and the LC-based DCO prototype earns the finer tuning gain and phase noise performance. These techniques are incorporated in the design and are successfully demonstrated in this work. Finally, this paper presents a 2.4 GHz all-digital frequency synthesizer with less than 2 ps rms jitter and less than 5 μs locking time.

6.2 Future work

The work can be applied to a higher order ADPLL system with a single-pole IIR filter for the superior spectrum performance. In order to keep the ΣΔ-shaped frequency quantization noise lower than the DCO intrinsic noise, the dithering frequency needs to be sufficiently high. Besides, the DCO band selection and loop parameter control circuit must be auto-calibrated. The proposed approach can be easily ported to other advanced CMOS processes. Thus, the power consumption can be scaled down.

References

[1] R. B. Staszewski, D. Leipold, K. Muhammad, and P. T. Balsara, "Digitally Controlled Oscillator (DCO)-Based Architecture for RF Frequency Synthesis in A Deep-Submicrometer CMOS Process," *IEEE Trans. Circuits Syst. II*, vol. 50, no.11, pp. 815–828, Nov. 2003.

[2] R. B. Staszewski et al., "All-Digital PLL and Transmitter for Mobile Phone," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2469–2482, Dec. 2005.

[3] C.-M. Hsu, M. Z. Straayer, and M. H. Perrott, "A Low-Noise Wide-BW 3.6-GHz Digital ΔΣ Fractional-N Frequency Synthesizer with A Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," *IEEE J. Solid-State Circuits*, vol. 43, pp. 2776–2786, Dec. 2008.

[4] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2000.

[5] N. A. D'Andrea and F. Russo, "A Binary Quantized Digital Phase Locked Loop: A Graphical Analysis," *IEEE Trans. on Communications*, vol. 26, pp. 1355-1364, Sep. 1978.

[6] S. C. Gupta, "Status of Digital Phase Locked Loops," *Proceedings of the IEEE*, vol. 63, pp. 291-306, Feb. 1975.

[7] W. Lindsey and C. Chie, "A Survey of Digital Phase-Locked Loops," *Proceedings of the IEEE*, vol. 69, pp. 410-431, Apr. 1981.

[8] I.-C. Hwang, S.-H. Song, and S.-W. Kim, "A Digitally Controlled Phase-Locked Loop with A Digital Phase-Frequency Detector for Fast Acquisition," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1574-1581, Oct. 2001.

[9] W. Bax and M. Copeland, ”A GMSK Modulator using A ΣΔ Frequency Discriminator-Based Synthesizer," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1218-1227, Aug. 2001.

[10] R. B. Staszewski et al., “All-Digital Phase-Domain TX Frequency Synthesizer for Bluetooth Radios in 0.13μm CMOS,” *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 272-273, Feb. 2004.

[11] N. D. Dalt, E. Thaller, P. Gregorius, and L. Gazsi, “A Compact Triple-Band Low-Jitter Digital LC PLL with Programmable Coil in 130-nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 40, pp.1482-1490, Jul. 2005.

[12] P. Lu and H. Sjöland, “A 5GHz 90-nm CMOS All Digital Phase-Locked Loop,” *IEEE A-SSCC*, pp. 65-68, Nov. 2009.

[13] R. B. Staszewski and P.T. Balsara, “All-Digital Frequency Synthesizer in Deep-Submicron CMOS,” JOHN WILEY & SONS, INC., 2006.

[14] C.- M. Hsu, "Techniques for High-Performance Digital Frequency Synthesis and Phase Control," PhD Thesis, Massachusetts Institute of Technology, Sep. 2008.

[15] J. Dorsey, Continuous and Discrete Control Systems, Mc Graw Hill.

[16] Y.-H. Huang, "A Dynamic Phase Error Compensation Technique for Fast-Locking Phase-Locked Loops," MS Thesis, National Taiwan University, Sep. 2009.

[17] W.-H. Chiu, Y.-H. Huang, and T.-H. Lin, “A Dynamic Phase Error Compensation Technique for Fast-Locking Phase-Locked Loops,” *IEEE J. Solid-State Circuits*, vol. 45, pp. 1137-1149, Jun. 2010.

[18] F. M. Gardner, "Charge-Pump Phase-Lock Loops," *IEEE Trans. on Communications*, vol. 28, pp. 1849-1858, Nov. 1980.

[19] M. V. Paemel, "Analysis of A Charge-Pump PLL: A New Model," *IEEE Trans. on Communications*, vol.42, pp. 2490 –2498, Jul. 1994.

[20] S.-Y. Yang, "A 10GHz, Fast-Locking All-Digital Frequency Synthesizer," MS Thesis, National Chiao-Tung University, Nov. 2008.

[21] X. Gao, E. A. M. Klumperink, P. F. J. Geraedts, and B. Nauta, "Jitter Analysis and A Benchmarking Figure-of-Merit for Phase-Locked Loops," *IEEE Trans. Circuits Syst. II*, vol. 56, no. 2, pp. 117–121, Feb. 2009.

[22] C.-Y. Yang and S.-I. Liu, "Fast-switching Frequency Synthesizer with A Discriminator-Aided Phase Detector," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1445-1452, Oct. 2000.

[23] X. F. Kuang and N. J. Wu, "A Fast-settling PLL Frequency Synthesizer with Direct Frequency Presetting," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 741-742, Feb. 2006.

[24] S. Shin, K. Lee, and S.-M Kang, "4.2mW CMOS Frequency Synthesizer for 2.4GHz ZigBee Application with Fast Settling Time Performance," *Microwave Symposium Digest*, pp. 411-414, Jun. 2006.

[25] R.-J. Yang and S.-I. Liu "A 40-550 MHz Harmonic-Free All-Digital Delay-Locked Loop using A Variable SAR Algorithm" *IEEE J. Solid-State Circuits*, vol. 42, no. 2, Feb. 2007.

[26] L. Wang, L. Liu, and H. Chen "An Implementation of Fast-Locking and Wide-Range 11-bit Reversible SAR DLL," *IEEE Trans. Circuits Syst. II*, vol. 57,

no. 6, Jun. 2010.

[27] A. Yamagishi, M. Ishikawa, T. Tsukahara, and S. Date, “A 2-V 2-GHz Low-Power Direct Digital Frequency Synthesizer,” *IEEE J. Solid-State Circuits*, vol. 33, pp. 210-217, Feb. 1998.

[28] A. Rofougaran et al., “A Single-Chip 900 MHz Spread-Spectrum Wireless Transceiver in 1-μm CMOS. I. Architecture and Transmitter Design,” *IEEE J. Solid-State Circuits*, pp. 515-533, Apr. 1998.

[29] W. Chaivipas and A. Matsuzawa, "Analysis and Design of Direct Reference Feed-Forward Compensation for Fast-Settling All-Digital Phase-Locked Loop", *IEICE Trans. Electron*, vol. E90-C, no.4, pp. 793-801, Apr. 2007.

[30] P.-Y. Wang, J.-H. C. Zhan, H.-H. Chang, and H.-M. S. Chang, "A Digital Intensive Fractional-N PLL and All-Digital Self-Calibration Schemes," *IEEE J. Solid-state Circuits*, vol. 44, no. 8, pp. 2182-2192, Aug. 2009.

[31] S.-Y. Lin, "All-Digital Spread Spectrum Clock Generators," MS Thesis, National Taiwan University, Jan. 2009.

[32] A. Hajimiri and T. H. Lee, “Design Issues in CMOS Differential LC Oscillators,” *IEEE Journal Solid-State Circuits*, vol. 34, pp. 717-724, 1999.

[33] D. C. Lee, “Analysis of Jitter in Phase-Locked Loops,” *IEEE Trans. Circuits Syst. II*, vol. 49, no. 11, pp. 704–711, Nov. 2002.

[34] R. C. H. Beek, E. A. M. Klumperink, C. S. Vaucher, and B. Nauta, “Low-Jitter Clock Multiplication: A Comparison between PLLs and DLLs,” *IEEE Trans. Circuits Syst. II*, vol. 49, no. 8, pp. 555–566, Aug. 2002.

[35] M. Mansuri and C.-K. K. Yang, “Jitter Optimization Based on Phase-Locked Loop Design Parameters,” *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1375–1382, Nov. 2002.

[36] B. Razavi, "Prospects of CMOS Technology for High-Speed Optical Communication Circuits," *IEEE J. Solid-State Circuits*, vol. 37, no. 9, pp. 1135-1145, Sep. 2002.

[37] J. A. Tierno, A. V. Rylyakov, and D. J. Friedman, “A Wide Power Supply Range, Wide Tuning Range, All Static CMOS All Digital PLL in 65 nm SOI,” *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 42-51, Jan. 2008.

[38] D.-S. Kim, H. Song, T. Kim, S. Kim, and D.-K. Jeong, "A 0.3–1.4 GHz All-Digital Fractional-N PLL With Adaptive Loop Gain Controller," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2300-2311, Nov. 2010.

[39] W. Grollitsch, R. Nonis, and N. Da Dalt, "A 1.4ps$_{rms}$-Period-Jitter TDC-Less Fractional-N Digital PLL with Digitally Controlled Ring Oscillator in 65nm CMOS" *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 478–480, Feb. 2010.

[40] C.-M. Hsu, M. Z. Straayer, and M. H. Perrott, “A low-noise, wide-BW 3.6 GHz digital fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation,” *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 340–341, Feb. 2008.

[41] M. Brownlee, P. K. Hanumolu, K. Mayaram, and U.-K. Moon, "A 0.5 to 2.5 GHz PLL with Fully Differential Supply-Regulated Tuning," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 588-589, Feb. 2006.