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設計與分析應用於毫米波寬頻高功率 GaAs 功率放大器與補

償電感之分布式主動變壓器 CMOS 功率放大器

Design and Analysis of Millimeter-wave Wideband High-Power GaAs

Power Amplifier and Distributed Active Transformer CMOS Power

Amplifier with Inductive Compensation

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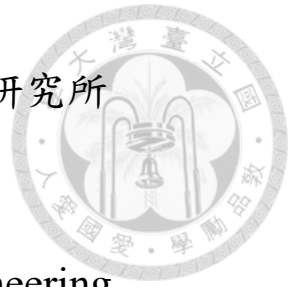
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Amplifier and Distributed Active Transformer CMOS Power Amplifier with
Inductive Compensation

本論文係 傅資皓 (D08942005) 在國立臺灣大學電機資訊學院電信工程學研究所完成之博士學位論文，於民國 113 年 12 月 19-20 日承下列考試委員審查通過及口試及格，特此證明。

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中文摘要



本論文針對第五代行動通訊 (5G) 中的毫米波寬頻功率放大器進行創新設計與深入分析，提出了多項創新架構與方法，以提升頻寬、輸出效率及輸出功率。在頻寬提升方面，本研究深入探討了博德法諾頻寬限制理論，並結合磁耦合諧振器與基於變壓器的雙調諧匹配網路，深入分析不同網路的頻寬提升與轉阻比例限制。針對 GaAs pHEMT 功率放大器，本研究提出一種創新的多諧振匹配網路架構，該架構結合了雙頻匹配的概念，能同時提升頻寬與轉阻比率。在設計實現上，成功達成 24 至 32 GHz 的寬頻操作，並在量測中實現 29.6 dBm 的峰值輸出功率及平均 30% 的功率附加效率 (PAE)。此外，針對 CMOS 功率放大器，提出一種新型的電感性補償分布式主動變壓器 (Distributed Active Transformer, DAT) 架構，能有效應用於超寬頻操作，涵蓋 31 至 65 GHz 的頻率範圍，同時解決阻抗匹配與寄生效應的設計挑戰。量測結果驗證了本研究所提出設計的有效性，成功達成 31 至 65 GHz 的寬頻操作，並在量測中實現 20.6 dBm 的峰值輸出功率及平均 15% 的功率附加效率。展現其在高效能毫米波功率放大器中的卓越表現。本研究不僅為毫米波功率放大器設計提供了關鍵技術突破，也為未來 5G 與 6G 無線通信技術的發展奠定了堅實的基石，展現出極具潛力的應用價值。

關鍵字：CMOS、GaAs、寬頻、功率放大器、分布式主動變壓器、多階匹配網路

ABSTRACT



This thesis explores innovative designs of millimeter-wave broadband power amplifiers (PAs) for 5G communications, enhancing bandwidth, efficiency, and output power. It investigates the Bode-Fano limitation for bandwidth improvement and combines magnetic-coupled resonators with transformer-based dual-tuned matching networks. A novel multi-resonant matching network for GaAs pHEMT PAs achieves 24–32 GHz bandwidth, 29.6 dBm peak output power, and 30% power-added efficiency (PAE). For CMOS PAs, an inductive-compensated distributed active transformer (DAT) supports 31–65 GHz ultra-broadband operation, resolving impedance matching and parasitic challenges. Measurement results validate the proposed designs' performance, offering significant advancements for high-efficiency millimeter-wave PAs. This research establishes a solid foundation for future 5G and 6G wireless communication systems.

Index terms – CMOS, GaAs, wide-band, PA, DAT, multi-resonance matching network

CONTENTS



誌謝	iii
中文摘要	v
ABSTRACT	vi
CONTENTS	vii
LIST OF FIGURES	x
LIST OF TABLES	xvii
Chapter 1 Introduction	1
1.1 Background and Motivation [1]	1
1.2 System Level Requirements and Challenges [78]-[79]	2
1.3 Contribution [13],[77]	8
1.4 Thesis Organization	9
Chapter 2 Bandwidth Enhancement Techniques for mm-Wave Power Amplifiers	11
2.1 Introduction	11
2.2 Gm-stage analysis [2],[77]	12
2.2.1 Weak Inversion (WI) [2]	13
2.2.2 Strong Inversion (SI) [2]	14
2.2.3 Velocity Saturation (VS) [2]	15

2.2.4	Performance and Frequency Response [2]	16
2.2.5	Maximum Oscillation Frequency [77]	16
2.3	Bandwidth Enhancement Techniques [78]	17
2.3.1	RLC Tank and Bode-Fano Limit [80]	18
2.3.2	Magnetically Coupled Resonators [6]-[7]	20
2.4	Transformer-Based Doubly-Tuned Matching Network [63],[81]	22
2.5	Extended Matching Network [12]-[13]	28
2.6	Summary.....	33
Chapter 3	Millimeter-wave Wideband High-power GaAs pHEMT Power Amplifier	35
3.1	Introduction	35
3.2	Circuit Design.....	37
3.2.1	Power-stage and proposed multi-resonance matching network	37
3.2.2	Driver-Stage and Matching Network	46
3.2.3	Circuit Schematic and Simulation Results	51
3.3	Measurement Results.....	64
3.4	Summary.....	71
Chapter 4	Millimeter-wave Wideband CMOS Power Amplifier Using Inductive- Compensation Distributed Active Transformer	74
4.1	Introduction	74

4.2	Transformer-Base Power Combining Structure	76
4.2.1	Transformer-Base Parallel/Series Combining Architecture	77
4.2.2	Transformer-Base Parallel/Series Combining Architecture	79
4.2.3	Proposed Novel DAT Series Combining Architecture	83
4.3	Circuit Design.....	88
4.3.1	Power Stage and Output Power Combiner Design.....	89
4.3.2	Driver Stage and ISMN2	97
4.3.3	Buffer Stage and ISMN1	99
4.3.4	IMN	101
4.3.5	Stability Check	103
4.4	Measurement Results.....	112
4.4.1	Small-Signal S-Parameter Measurement.....	113
4.4.2	Large-Signal Measurement.....	114
4.5	Summary.....	120
Chapter 5	Conclusion.....	124
Appendix		127
REFERENCE		131
PUBLICATIONS LIST		139

LIST OF FIGURES



Fig. 1.1 5G MMW system spectrum.	1
Fig. 1.2 5G mmW, (a) high linearity requires communication and (b) FMCW simple system block.	4
Fig. 1.3 System architectures, (a) wideband and (b) multi-band PA.	5
Fig. 1.4 Conventional wideband techniques, (a) distributed PA [71]-[72], (b) balanced PA [73]-[74], (c) staggered PA [75], and (d) high-order network PA [60]-[62].	6
Fig. 2.1 Common source (CS) amplifier, IDS versus VGS plot.	13
Fig. 2.2 AC model of CS amplifier.	13
Fig. 2.3 RLC filter schematic.	18
Fig. 2.4 Simplified amplifier circuit model.	18
Fig. 2.5 MCR schematic.	20
Fig. 2.6 Simple matching schematic of the transformer-base 2-stage amplifier.	22
Fig. 2.7 Doubly-tuned Matching Network.	23
Fig. 2.8 Typical situation in the output matching of amplifier.	24
Fig. 2.9 Low-Qs case equalized model.	26
Fig. 2.10 Typical situation in the interstage matching of amplifier.	27
Fig. 2.11 Doubly-tuned matching network with T and π model equivalent.	29

Fig. 2.12 Extended T-model matching network.	32
Fig. 2.13 Bandwidth comparison of LC, 4th and 6th order T-model-based matching network.	32
Fig. 3.1 Transistor size 1600 $\mu\text{m gm}$ performance.	40
Fig. 3.2 Reference [26], (a) Dual-band matching network and its L-type equivalent circuits at (b) low frequency (f_1), and (c) high frequency (f_2).	42
Fig. 3.3 Proposed high-impedance-transformation-ratio of multi-resonance matching network	43
Fig. 3.4 Impedances of the proposed high-impedance-transformation-ratio multi-resonance matching network and the forbidden region of ref [26]	44
Fig. 3.5 S-parameters of the MCR and the proposed multi-resonance matching network.	44
Fig. 3.6 28 GHz power performance with OMN.	45
Fig. 3.7 Power budget of the proposed wideband high-power PA.	46
Fig. 3.8 Inter-stage matching network of the proposed wideband high-power PA.	47
Fig. 3.9 Input-stage matching network of the proposed wideband high-power PA.	48
Fig. 3.10 Simulated insertion loss of the interstage and input matching networks of the proposed PA.	49



Fig. 3.11 Complete schematic of the proposed wideband-high-power PA.....	50
Fig. 3.12 Complete layout of the proposed wideband-high-power PA.....	51
Fig. 3.13 Simulated S-parameter of the proposed wideband-high-power PA.....	51
Fig. 3.14 Complete layout of the proposed wideband-high-power PA ($2.4 \times 1.1 \text{ mm}^2$).	54
Fig. 3.15 Simulated S-parameter of the proposed wideband-high-power PA.....	55
Fig. 3.16 Simulated large signal of the proposed wideband-high-power PA.....	56
Fig. 3.17 Stability check of circuit.	61
Fig. 3.18 Stability check of inter-stage from 0.1-50 GHz.	61
Fig. 3.19 Stability check of the testing line from bias.	62
Fig. 3.20 Stability check of input pulse-testing.....	62
Fig. 3.21 Stability check of bias port pulse-testing.	63
Fig. 3.22 Stability check of OscTest.	63
Fig. 3.23 Proposed wideband HPA chip photo	64
Fig. 3.24 Measured and simulated S-parameters.....	65
Fig. 3.25 Measured and simulated large signal results at 24/26/28/32 GHz.	66
Fig. 3.26 Measured and simulated Psat and PAE results with different frequencies....	66
Fig. 3.27 Measured and simulated OP _{1dB} with different frequencies.....	67
Fig. 3.28 Measured and simulated OIP3 at 28 GHz.....	67



Fig. 3.29 Measured modulation results at (a) 24 GHz, (b) 28 GHz, (c) 30 GHz, and (d) 32 GHz.....	69
--	----

Fig. 3.30 Measured EVM results.....	70
-------------------------------------	----

Fig. 4.1 Schematics of transformer-based (a) parallel and (b) series power combining networks with parasitic capacitors C_p	77
---	----

Fig. 4.2 (a) m-way power combiner, (b) equivalent network of m-way power combiner when $V_1=V_2=\dots=V_m$, and (c) 2-way series power combiner and its equivalent circuit.....	79
--	----

Fig. 4.3 Simulated (a) amplitude and phase difference, (b) PCEFF and combining loss of the series power combining architecture with 20-fF C_p as shown in Fig. 4.1(b).	81
--	----

Fig. 4.4 Equivalent circuit of the traditional DAT with main parasitic effects	84
--	----

Fig. 4.5 (a) Traditional and (b) proposed DAT architectures and equivalent parasitic capacitors.	84
---	----

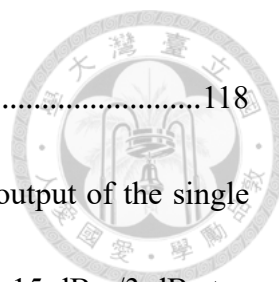
Fig. 4.6 Proposed inductive-compensation simulated equivalent schematic.	85
---	----

Fig. 4.7 Proposed compensated inductor value from 50 – 250 pH (a) PCEFF, (b) amplitude difference, and (c) phase difference.	86
---	----

Fig. 4.8 Proposed compensated inductor Q-factor effect.	87
--	----

Fig. 4.9 Proposed PA schematic.....	88
Fig. 4.10 Proposed PA power-stage (a) combined line layout with the neutralization capacitors, and (b) maximum and stability k-factor	90
Fig. 4.11 Proposed PA's power contours and PAE contours at 35/45/55/65 GHz after extracted C_{DEV}	91
Fig. 4.12 Proposed PA output matching network (OMN) (a) schematic, and (b) the equivalent matching network ($m=2$)	93
Fig. 4.13 OMN shown in Fig. 4-12(b) bandwidth analysis of Z_{in} with different C_o	93
Fig. 4.14 Proposed PA's power combining OMN (a) EM layout, (b) S-parameters results with EM	95
Fig. 4.15 Comparison of the large-signal performance between traditional DAT and proposed DAT, (a) at 60 GHz, (b) PAE and P_{sat} at 30-80 GHz.	96
Fig. 4.16 (a) EM layout and (b) EM simulated S-parameters of the ISMN2.	98
Fig. 4.17 (a) EM layout and (b) EM simulated S-parameters of the ISMN1	100
Fig. 4.18 (a) EM layout and (b) EM simulated amplitude and phase differences of the power splitter	101
Fig. 4.19 (a) EM layout and (b) EM simulated S-parameters of the IMN	102
Fig. 4.20 Stability check of ISMN1 from 0.1-90 GHz	104
Fig. 4.21 Stability check of ISMN2 from 0.1-90 GHz	105

Fig. 4.22 Stability check of input pulse-testing	105
Fig. 4.23 Stability check of bias port pulse-testing with two cases of OMN	106
Fig. 4.24 Stability check of bias port pulse-testing in case-I of transient and frequency test.....	106
Fig. 4.25 Stability check of bias port pulse-testing in case-II of transient and frequency test.....	106
Fig. 4.26 Stability check of OscTest in (a) case-I, and (b) case-II.	107
Fig. 4.27 Stability check of bias port with output port isolation.	107
Fig. 4.28 Stability check of SProbePair.....	108
Fig. 4.29 Complete layout of the proposed PA.	111
Fig. 4.30 Proposed PA's chip photograph.....	112
Fig. 4.31 Measurement setup.....	113
Fig. 4.32 Proposed PA's chip photograph.....	114
Fig. 4.33 Measured and simulated large-signal performances of the proposed PA at 30/40/60/65 GHz under 1.2 V V_{DD}	115
Fig. 4.34 Measured large-signal performances versus frequency of the proposed PA from 30 to 67 GHz.	116
Fig. 4.35 Simulated (a) I_d and g_m versus V_g , and (b) I_d versus input power (P_{in}) with	



different V_g of a single device	118
Fig. 4.36 Simulated (a) voltage swing and (b) current swing at the output of the single side devices under 1.2-V V_d and 0.8-V V_g , with P_{in} =-15~15 dBm/3 dB step	119
Fig. 4.37 Simulated and measured DC current with different P_{in} at 30-65 GHz.....	119
Fig. 4.38 Measured EVM of the designed PA using 64-QAM signal with 100 Msys/s at 40 GHz and 60 GHz.	120
Fig. 4.39 Measured EVM of the designed PA using 64-QAM signal with 200 Msys/s at 40 GHz and 60 GHz.	120

LIST OF TABLES



Table 3.1 The power performance results with the total width of 1600 μm at 28 GHz.. 40

Table 3.2 Values of equivalent model and device of the proposed PA..... 52

Table 3.3 Performance comparison with previously published wideband and high-power
PAs. 72

Table 4.1 Comparison with previously published wideband and V-band PAs 123



Chapter 1 Introduction

1.1 Background and Motivation [1]

With the rapid advancement of wireless communication systems in recent years, numerous innovative applications have emerged, including virtual reality (VR), the Internet of Things (IoT), autonomous driving, and even radar-based solutions. These technologies demand significantly higher data rates, lower latency, and more reliable connections, driving the need for more advanced communication infrastructure. To meet these challenges, fifth-generation (5G) networks have been developed, offering higher data throughput, ultra-reliable low-latency communication (URLLC), and the ability to connect massive numbers of devices simultaneously.

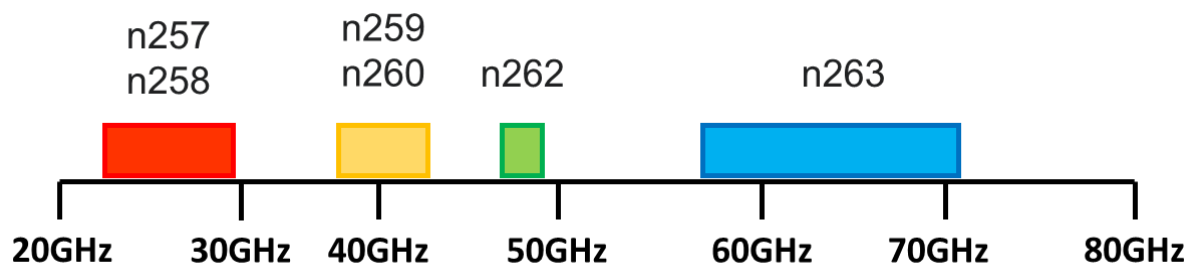


Fig. 1.1 5G MMW system spectrum [1].

A critical feature of 5G is its use of the millimeter-wave (mmWave) spectrum, which provides a much wider bandwidth than previous generations, enabling faster data transmission and supporting more connected devices. As global 5G deployment expands, with many countries allocating spectrum across a wide range of frequencies from sub-1



GHz to mmWave bands, as shown in Fig. 1.1, the potential for new applications continues to grow. In addition to supporting immersive VR experiences, smart city infrastructure via IoT, and the precise communication required for autonomous driving, 5G also enables radar applications, particularly in automotive systems. 5G radar can be used for object detection, distance measurement, and speed determination in autonomous vehicles, further broadening the scope of its impact.

Consequently, research into RF circuit design for the 5G NR-FR2 frequency bands has become increasingly critical. The mmWave spectrum poses unique challenges, such as higher signal attenuation and the need for highly efficient power amplifiers and low-noise receivers, demanding innovative circuit designs. My research aims to tackle these challenges by optimizing RF circuits for high-frequency operation, ensuring robust performance for communication and radar applications. The successful optimization of RF circuits could significantly enhance the performance and reliability of 5G networks, thereby revolutionizing the telecommunications and technology industry.

1.2 System Level Requirements and Challenges [78]-[79]

One of the most critical challenges in designing 5G mmWave communication systems is the significant increase in path loss as transmission frequency rises. To mitigate

this, advanced techniques like antenna arrays and beamforming are employed to enhance antenna directivity and improve signal transmission and reception without mechanical movement. Phased array systems, for example, enable higher directivity but at the cost of increased power consumption and more complex thermal management, especially in large-scale multiple-input multiple-output (MIMO) systems.

5G systems utilize advanced modulation schemes, such as multi-level quadrature amplitude modulation (M-QAM), to further improve spectrum efficiency, including higher-order variants like 64-QAM and 256-QAM. While these schemes enable higher data throughput, they impose stricter signal quality requirements, particularly in signal-to-noise ratio (SNR) and bit-error-rate (BER). As the modulation order increases, so does the required SNR, adding considerable pressure on system components, particularly the power amplifier (PA).

The PA is a critical component in 5G mmWave systems, ensuring the transmitted signals maintain high linearity and efficiency. Given the high-order modulation schemes used in 5G, such as 64-QAM and 256-QAM, the PA must operate across a wide dynamic power range while minimizing distortion. For example, 64-QAM requires the PA to handle a power range of 16.9 dB without introducing significant amplitude modulation (AM-AM) or phase modulation (AM-PM) distortion. This demand for high linearity and

efficiency makes PA design one of the most critical challenges in 5G systems, as highlighted in Fig. 1.2(a), illustrating the high linearity requirements of a typical 5G communication system. Another critical application of PAs is in frequency-modulated continuous-wave (FMCW) radar systems, which are used for applications like autonomous driving and advanced radar solutions. As depicted in Fig. 1.2(b), FMCW systems rely heavily on stable, high-power signal output, making the PA essential in ensuring performance and reliability.

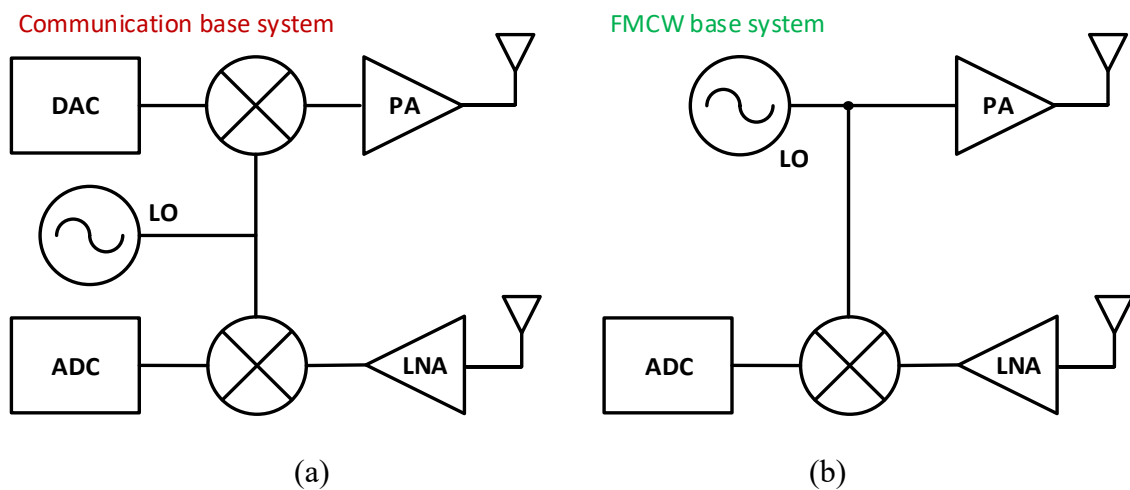


Fig. 1.2 5G mmW, (a) high linearity requires communication and (b) FMCW simple system block.

PA design has two primary architectural approaches: wideband and multi-band. Wideband PAs are designed to cover multiple frequency bands with a single front end, offering simplicity, cost, and compact advantages, as shown in Fig. 1.3(a). These systems are ideal for applications requiring broad frequency coverage but not necessarily the

highest performance. On the other hand, multi-band PAs employ separate front-ends and amplifiers for each frequency band, providing superior performance, especially in applications requiring precise control and high efficiency across multiple bands, like Fig. 1.3(b) shown. However, multi-band systems have increased complexity, power consumption, and physical size.

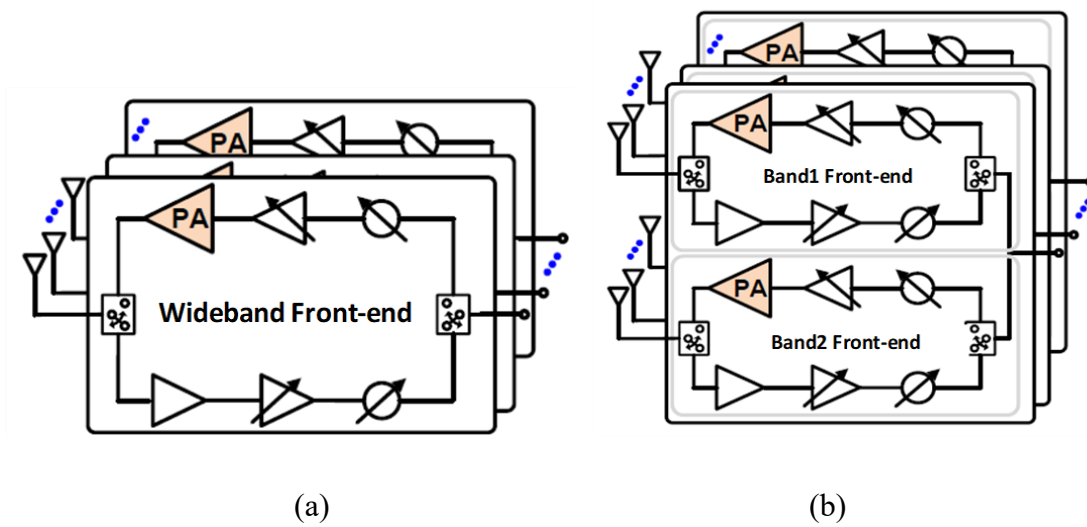


Fig. 1.3 System architectures, (a) wideband and (b) multi-band PA.

As the number of PA elements increases in systems like massive MIMO, power consumption and heat dissipation challenges become even more critical. While broadband PA systems are generally more energy-efficient, they may not provide the high performance needed for multi-band or high-frequency applications. Though offering better performance, multi-band systems consume more power and generate more heat, requiring advanced thermal management solutions and power management strategies.

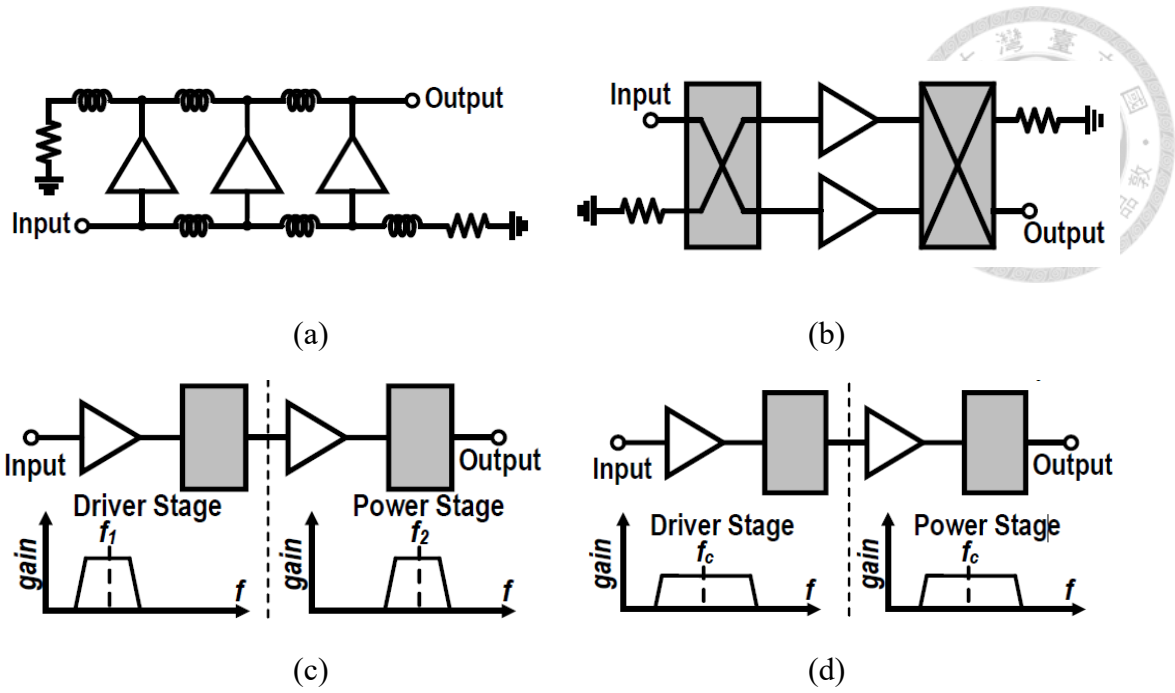


Fig. 1.4 Conventional wideband techniques, (a) distributed PA [71]-[72], (b) balanced PA [73]-[74], (c) staggered PA [75], and (d) high-order network PA [60]-[62].

Modern wireless communication systems, particularly emerging 5G mmWave networks, demand PAs capable of delivering wideband operation, high efficiency, and compact integration. However, designing a PA that simultaneously addresses these often-competing requirements remains a significant challenge. Various broadband PA topologies have been explored to tackle these issues, each offering distinct advantages and facing inherent trade-offs.

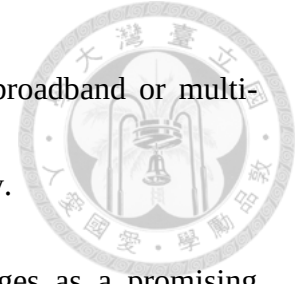
For instance, the distributed PA architecture achieves ultra-wide bandwidth by distributing multiple transistor stages along a transmission line, as shown in Fig. 1.4(a). This ensures gain and output power performance across an extensive frequency range. Nevertheless, this approach tends to be area-intensive and suffers from limited efficiency

due to the complexity of the signal distribution network [71]-[72]. Similarly, Fig. 1.4(b) shows the balanced PA topology leverages 90-degree hybrid couplers to maintain wideband response and can offer improved efficiency under power back-off conditions [73]-[74]. However, its lossy hybrid network and relatively large footprint hinder efficiency and compactness.

Another approach, the staggered PA, employs multiple gain stages tuned at slightly offset frequency bands, as shown in Fig. 1.4(c). While it enables wideband coverage within a smaller chip area, the staggered arrangement inherently limits achievable gain, efficiency, and overall output power, ultimately constraining its applicability in modern high-power systems [75]. In contrast, high-order network PAs utilize carefully designed impedance transformation networks to balance bandwidth, efficiency, and area, as shown in Fig. 1.4(d) [60]-[62]. Although such configurations may exhibit noticeable gain ripple, they provide a practical means of meeting system requirements without resorting to overly complex distribution networks or large device footprints.

In summary, designing 5G mmWave communication systems requires addressing both system-level challenges, such as overcoming high-frequency transmission losses and improving spectrum efficiency, and component-level challenges, such as optimizing PA performance. The PA plays a pivotal role in balancing trade-offs between linearity and efficiency, mainly when supporting advanced modulation schemes. As the capabilities

and requirements of 5G evolve, successful PA design—whether broadband or multi-band—directly influences overall system performance and reliability.



Considering these factors, the high-order network PA emerges as a promising solution in the 5G mmWave context. This topology can help ensure that next-generation PA designs meet the stringent demands of modern communication systems by delivering an acceptable balance among bandwidth, efficiency, linearity, and device footprint. Consequently, the research presented in this work focuses on developing and optimizing a high-order network PA architecture to support the evolution of 5G mmWave technologies.

1.3 Contribution [13],[77]

This article presents significant advancements in the design of wideband, high-efficiency power amplifiers (PAs) for high-frequency communication systems. It first establishes a strong conceptual and technical foundation through a detailed analysis of fundamental PA cell structures and various wideband architectures. It thoroughly explores bandwidth extension methods, efficiency optimization, and device technology.

Building on these insights, a new wideband PA design is introduced that achieves a notable output power of 29 dBm, showcasing how innovative multi-band matching techniques can effectively broaden operational bandwidth without sacrificing too much

efficiency. Moreover, this design leverages a highly compact layout, resulting in excellent power density that further enhances performance [13].



In addition, the article proposes an innovative distributed active transformer (DAT) architecture, delivering improved power-combining efficiency across a wide frequency range [77]. The architecture incorporates a DAT approach with minimized transformer dimensions, leading to superior power density across a wide frequency range. By integrating this DAT approach, the design enhances overall performance, helping to address the stringent demands of future high-frequency applications. Collectively, these contributions push the boundaries of existing PA technologies and provide valuable frameworks and methodologies for guiding future research and development in high-frequency RF front-end systems.

1.4 Thesis Organization

In Chapter 2, this thesis begins with a comprehensive analysis of power amplifier (PA) cells and various wideband architectures.

In Chapter 3, this thesis introduces a novel wideband high-efficiency PA design. Modifying a dual-band matching architecture significantly expands operational bandwidth while maintaining high efficiency. The proposed PA delivers an output power of 29 dBm, making it suitable for demanding high-frequency applications. The design

methodology is detailed, including the advanced matching networks, and minimizing losses. Simulation results and experimental validations demonstrate the effectiveness of the design.

In Chapter 4, this thesis presents an innovative distributed active transformer (DAT) architecture for power combining. This DAT enhances combining efficiency in the high-frequency range of 31–65 GHz and achieves ultra-wideband operation. With an average output power exceeding 19 dBm, the architecture offers significant advantages for high-frequency wideband applications. We discuss the design principles of the DAT, highlighting the unique transformer configurations and the use of differential signaling. Performance evaluations, including simulations and practical implementations, validate the superiority of the proposed architecture.

Chapter 2 Bandwidth Enhancement Techniques for mm-Wave Power Amplifiers



2.1 Introduction

CMOS technology scaling enables faster transistors at each process node, facilitating the design of mm-Wave analog circuits. However, this scaling brings challenges along with the advantages. The reduction in breakdown voltage necessitates a corresponding decrease in supply voltage, which imposes constraints on linearity, device stacking, and achievable signal-to-noise ratio (SNR). Additionally, the back-end-of-line (BEOL) metal layers become thinner and closer to the substrate, exacerbating the impact of interconnect losses and parasitic. In many ways, mm-wave design differs significantly from traditional RF design at lower frequencies. For example, capacitors in RF circuits typically exhibit higher quality factors than inductors, and on-chip transmission lines are generally impractical due to long wavelengths. In contrast, at mm-wave frequencies, the design landscape changes completely. As a result, innovative design approaches are required to overcome these challenges.

When considering Gallium Arsenide (GaAs) technology, the situation shifts somewhat. GaAs offer higher electron mobility and greater breakdown voltage, making them well-suited for high-frequency performance in the mm-wave range. Although GaAs may not provide the same level of integration as CMOS and comes with higher

manufacturing costs, it excels in applications requiring higher linearity and efficiency. In mm-wave designs, GaAs can handle higher power levels more effectively while mitigating interconnect losses and parasitic effects. As a result, GaAs remains a preferred option in specific mm-wave applications, mainly where high power and linearity are essential.

This chapter will explore device transconductor detail and the matching networks of bandwidth enhancement and impedance transformation.

2.2 Gm-stage analysis [2],[77]

Transistors operate as transconductors by converting voltage differences between the gate and source into a proportional current flow between the drain and source. This functionality is crucial in analog circuits, RF amplifiers, and high-frequency designs. Fig. 2.1 shows the transistor can operate in three main regions: weak inversion (WI), strong inversion (SI), and velocity saturation (VS), each with distinct characteristics that impact transconductance, speed, and power efficiency [2]. Understanding the behavior of these regions in both CMOS and GaAs technologies is essential for optimizing high-performance circuits, and the AC model of the common source PA is shown in Fig. 2.2 [77].

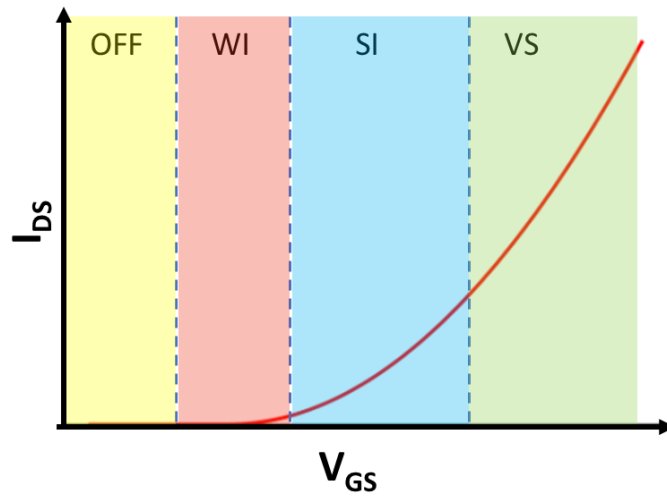


Fig. 2.1 Common source (CS) amplifier, I_{DS} versus V_{GS} plot.

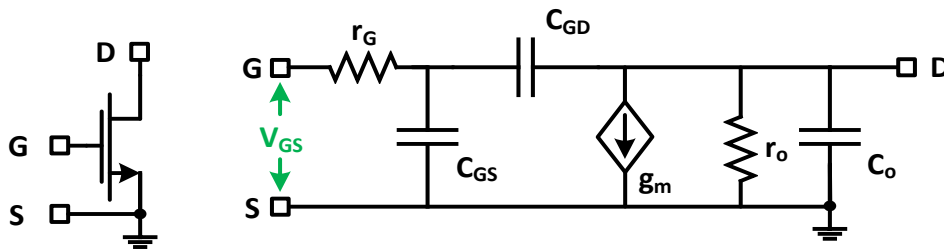


Fig. 2-2 AC model of CS amplifier [77].

2.2.1 Weak Inversion (WI) [2]

In the weak inversion region, also known as the subthreshold region, the MOS transistor operates with very low gate-source voltage (V_{GS}), where the current flows due to diffusion rather than drift. The drain current exhibits an exponential dependence on V_{GS} , which is given by [2]

$$I_{DS,WI} = I_0 e^{\frac{V_{GS}}{nV_T}}, \quad (2.1)$$

where I_0 is a process-dependent constant, V_T is the thermal voltage, and n is the

subthreshold slope factor. In this region, the transconductance is expressed as [2]

$$g_{m,WI} = \frac{I_{DS}}{nV_T}. \quad (2.2)$$

The exponential behavior of g_m in WI leads to very low power consumption, making this region favorable for ultra-low-power applications. CMOS transistors operating in this region are highly efficient in terms of power but have lower transconductance than SI and VS regions. GaAs transistors, typically used in high-speed applications, rarely operate in this region due to their higher power consumption profiles. However, they can still offer benefits in low-power analog designs if needed.

2.2.2 Strong Inversion (SI) [2]

As the gate voltage V_{GS} increases, the transistor transitions into the strong inversion region. Here, the current conduction is dominated by drift, and the drain current follows a quadratic relationship with V_{GS} , as shown as [2]

$$I_{DS,SI} = K' \frac{W}{L} (V_{GS} - V_T)^2. \quad (2.3)$$

In this region, the transconductance g_m is described by

$$g_{m,SI} = K' \frac{W}{L} 2(V_{GS} - V_T). \quad (2.4)$$

The strong inversion region is crucial for achieving higher current levels and better linearity, making it ideal for analog amplification. CMOS technology excels in SI, particularly for low-power, high-linearity designs. GaAs transistors, such as HEMTs (High Electron Mobility Transistors), also perform well in SI, but due to their higher



mobility, they can offer superior performance in terms of transconductance, making them suitable for high-frequency applications such as RF and mm-Wave circuits.

2.2.3 Velocity Saturation (VS) [2]

The transistor enters the velocity saturation region as V_{GS} increases beyond the strong inversion region. In this regime, the carrier velocity saturates due to high electric fields, limiting the increase in drain current. The current in VS is linearly dependent on $(V_{GS} - V_T)$ and is given by [2]

$$I_{DS,VS} = WC_{OX}v_{sat}(V_{GS} - V_T) . \quad (2.5)$$

The corresponding transconductance g_m is [2]

$$g_{m,VS} = WC_{OX}v_{sat} . \quad (2.6)$$

Transconductance becomes independent of V_{GS} in velocity saturation and is mainly determined by the device's physical properties, such as gate capacitance C_{OX} and carrier saturation velocity v_{sat} . CMOS transistors experience velocity saturation at shorter channel lengths, limiting performance at very high frequencies. Nevertheless, aggressive scaling of CMOS technology allows for maintaining high-speed performance, albeit with increased power dissipation. On the other hand, GaAs transistors, with their higher v_{sat} , maintain better performance even under velocity saturation, making them more suitable for ultra-high-frequency designs like millimeter-wave circuits.



2.2.4 Performance and Frequency Response [2]

The different operating regions of a transistor significantly affect its frequency response. The cut-off frequency f_T , which indicates the frequency where the current gain equals one, is a key performance metric. The cut-off frequency differs in each region [2]:

- In weak inversion:

$$f_{T, WI} = \frac{\mu}{2\pi L^2} e^{\frac{V_{GS}}{nV_T}}. \quad (2.7)$$

- In strong inversion:

$$f_{T, SI} = \frac{\mu}{2\pi L^2} (V_{GS} - V_T). \quad (2.8)$$

- In velocity saturation:

$$f_{T, VS} = \frac{v_{sat}}{2\pi L}. \quad (2.9)$$

For CMOS, scaling down the channel length L improves the cut-off frequency, particularly in velocity saturation. However, this comes at the cost of increased power dissipation and reduced output resistance. With their inherent high carrier mobility and saturation velocity, GaAs transistors exhibit higher f_T and maintain better frequency performance, even with larger channel lengths.

2.2.5 Maximum Oscillation Frequency [77]

Another critical figure of merit is the maximum oscillation frequency f_{MAX} , which represents the frequency where the power gain equals one. It is influenced by parasitic elements such as gate and drain resistances, and it is given by [77]

$$f_{MAX} = \frac{1}{2} \sqrt{\frac{g_m}{(C_{gs} + C_{gd})C_{gd}r_G}} \approx \frac{f_T}{2} \sqrt{\frac{r_o}{r_G}}, \quad (2.10)$$



where r_o is the output resistance and r_G is the gate resistance.

For CMOS, minimizing parasites such as gate resistance r_G is crucial for maintaining a high f_{MAX} . GaAs devices benefit from lower parasitic resistances and capacitances, resulting in higher f_{MAX} , making them preferable for high-frequency applications like 5G, mm-wave, and high-speed analog systems.

In summary, each operating region—weak inversion, strong inversion, and velocity saturation—offers distinct trade-offs regarding power consumption, transconductance, and frequency performance. CMOS transistors are versatile and efficient for lower-power and general-purpose applications, whereas GaAs transistors are optimized for high-frequency, high-performance designs. By understanding the characteristics of each region, designers can make informed choices to optimize transconductance and frequency response for specific applications.

2.3 Bandwidth Enhancement Techniques [78]

Here, it delves into the fundamentals of filters and introduces design techniques to enhance bandwidth, moving closer to the Bode-Fano limit. It strongly emphasizes filter topologies that facilitate relatively easy implementation with on-chip components and have demonstrated state-of-the-art performance at millimeter-wave frequencies.



2.3.1 RLC Tank and Bode-Fano Limit [80]

In an RLC tank circuit, the RC low-pass filter can be modified to achieve a band-pass response by adding an inductor L . This transforms the circuit's cutoff frequency to $\omega_0 = 1/\sqrt{LC}$, as illustrated in Fig 2.3 [3]. The inductor and capacitor resonate at this resonant frequency f_0 , and the tank impedance reduces to the equivalent load resistance R_T . The quality factor Q of the filter is given by [80]

$$Q = \frac{Im(Z)}{Re(Z)} = \omega_0 R_T C. \quad (2.11)$$

This configuration allows for signal amplification at mm-wave frequencies, but the achievable -3 dB bandwidth is limited by the RC product. One way to broaden the bandwidth is by introducing an equivalent parallel resistor, which, while reducing the Q -factor, results in additional trade-offs in efficiency.

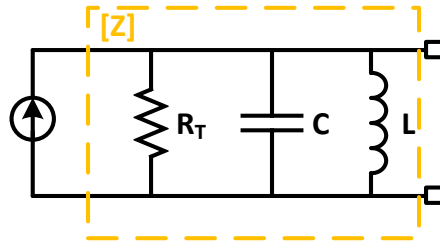


Fig. 2.3 RLC filter schematic.

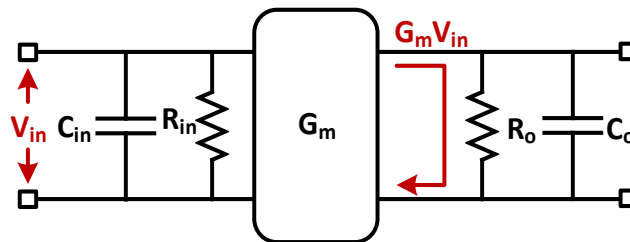
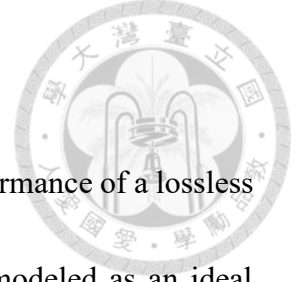


Fig. 2.4 Simplified amplifier circuit model.



The Bode-Fano criterion provides theoretical limits on the performance of a lossless filter with a parallel RC load. For a mm-Wave CMOS amplifier modeled as an ideal transconductance G_m with a parallel RC input and output impedance, as shown in Fig 2.4 [4], the Bode-Fano limit dictates that the in-band ripple and reflection coefficient Γ_{in} relate as

$$\int_0^{\infty} \ln \left(\frac{1}{|\Gamma_{in}(\omega)|} \right) d\omega \leq \frac{\pi}{RC}. \quad (2.12)$$

Furthermore, the reflection coefficient magnitude is close to the ripple as [5]

$$|\Gamma_{in}| = \sqrt{1 - \frac{1}{Ripple}}. \quad (2.13)$$

This criterion implies that achieving a broader passband bandwidth comes at the expense of a larger ripple in the filter's response. High-quality factors are more challenging to attain compared to lower values, especially in advanced technologies where increasing finger lengths can lead to a higher input/output capacitance, thereby impacting R_{in} and the achievable bandwidth.

The Chebyshev filter is a practical approximation of the band-pass filter under the Bode-Fano limit. While higher-order filters offer advantages, the complexity and limited feasibility of on-chip implementation restrict their application in modern technology. At mm-wave frequencies, filter designs using RLC tanks achieve gain-bandwidth

enhancements while balancing efficiency and design complexity, aiming to approximate the theoretical Bode-Fano limit. This approach demonstrates the potential of RLC-based filters to meet state-of-the-art performance in mm-wave IC applications.



2.3.2 Magnetically Coupled Resonators [6]-[7]

In wideband design, a multi-order matching network is essential for achieving wide bandwidth and improved impedance matching across a broad frequency range. Multi-order matching network uses multiple paths or elements to distribute and manage energy flow, enhancing performance by reducing reflections and improving signal transfer efficiency. The Magnetically Coupled Resonator (MCR) design is a well-approach [6-7]. It leverages magnetic coupling between resonators to create multiple resonant peaks, and this method is precious in applications requiring consistent performance across a wide frequency spectrum.

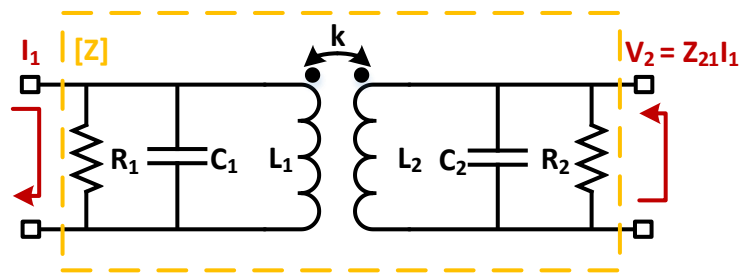
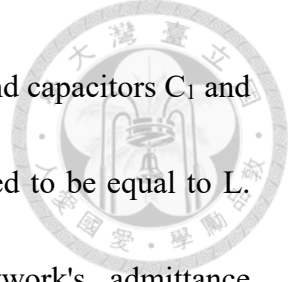


Fig. 2.5 MCR schematic.

The schematic of the MCR is shown in Fig. 2.5. It couples the two RLC tanks by



using a transformer, where both resistors R_1 and R_2 are equal to R , and capacitors C_1 and C_2 are equal to C . Additionally, the inductors L_1 and L_2 are assumed to be equal to L .

Using the transformer's Y-parameter model, the two-port network's admittance parameters can be derived. The self-admittances Y_{11} and Y_{22} are

$$Y_{11} = Y_{22} = \frac{1}{R} + \frac{1}{sL(1-k^2)} + sC, \quad (2.14)$$

where s is the complex frequency variable, and k is the coupling factor of the transformer.

The mutual admittance $Y_{21}=Y_{12}$ is

$$Y_{12} = Y_{21} = \frac{k}{sL(1-k^2)}. \quad (2.15)$$

The transimpedance of the two-port network, Z_{21} , is

$$Z_{21} = \frac{-s\omega_0^3 kQR}{[Qs^2 + s\omega_0 + Q(1+k)\omega_0^2][Qs^2 + s\omega_0 + Q(1-k)\omega_0^2]}, \quad (2.16)$$

where

$$\omega_0 = \frac{1}{\sqrt{L(1-k^2)C}}, \quad (2.17)$$

and

$$Q = \frac{R}{\omega_0 L(1-k^2)} = \omega_0 RC. \quad (2.18)$$

Assuming a high-quality factor, the two complex poles of Z_{21} are

$$\omega_L = \frac{1}{\sqrt{L(1+k)C}}, \quad (2.19)$$

and

$$\omega_L = \frac{1}{\sqrt{L(1-k)C}}. \quad (2.20)$$

Increasing the magnetic coupling coefficient k results in a wider band-pass

bandwidth, but it also increases the Q-factor of the filter, leading to a greater in-band ripple.



2.4 Transformer-Based Doubly-Tuned Matching Network [63],[81]

In RF circuit design, transformers play a crucial role in achieving efficient impedance matching across various stages of the network. As shown in Fig. 2.6, transformers are widely employed in input, interstage, and output networks, offering inherent impedance transformation capabilities. This lets designers match impedances between different circuit sections, ensuring maximum power transfer and minimal signal loss. An essential consideration in transformer-based matching networks is the incorporation of parasitics into the design. By embedding parasitic elements, such as those found in ladders or doubly-tuned networks [8]-[9], designers can achieve a more accurate and high-performance design.

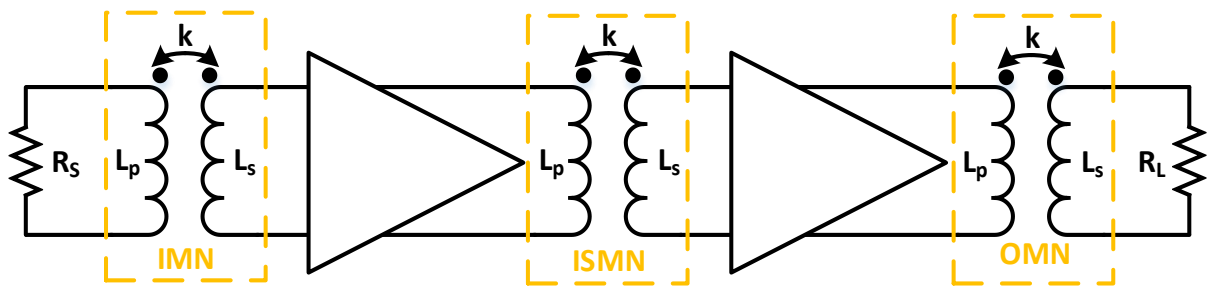


Fig. 2.6 Simple matching schematic of the transformer-base 2-stage amplifier.

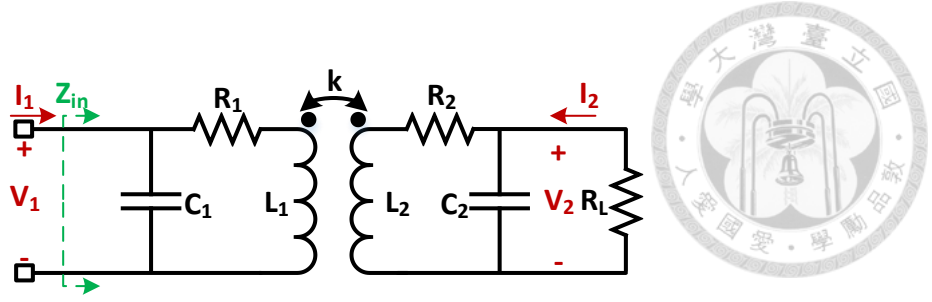


Fig. 2.7 Doubly-tuned matching network.

The doubly-tuned matching network, as illustrated in Fig. 2.7, offers a sophisticated approach to impedance transformation by utilizing two magnetically-coupled LC tanks, which form a fourth-order resonator. When the shunt capacitors C_1 and C_2 are significant, these networks become doubly tuned, allowing for more flexible control over impedance characteristics. The two resonate frequencies of the tank can be defined by

$$\omega_1 = \frac{1}{\sqrt{L_1 C_1}}, \quad (2.21)$$

and

$$\omega_2 = \frac{1}{\sqrt{L_2 C_2}}. \quad (2.22)$$

Moreover, the quality factor of the tank can be defined by

$$Q_1 = \frac{\omega L_1}{R_1}, \quad (2.23)$$

and

$$Q_2 = \frac{\omega L_2}{R_2}. \quad (2.24)$$

A critical factor in the performance of doubly-tuned networks is the loading effect of the load resistance R_L on the reactive components, quantified by the quality factor Q_S ,



which can be defined by

$$Q_s = \left(\frac{1}{\sqrt{1-k^2}} \right) \left(\frac{R_L}{\sqrt{L_2/C_2}} \right). \quad (2.25)$$

When Q_s is high, the network exhibits transformer behavior with two parallel resonances.

Conversely, a low Q_s results in a single resonance, characteristic of impedance inverter behavior. Additionally, the behavior of the network depends on the ratio ξ of the LC products of the coupled tanks, which influences the resonance frequencies and overall performance. Here, the ratio of the LC products of the coupled tanks is

$$\xi = \frac{\omega_1^2}{\omega_2^2} = \frac{C_2 L_2}{C_1 L_1}. \quad (2.26)$$

In the high Q_s case, the two parallel resonance frequencies are

$$\omega_L = \left\{ \frac{1 + \xi - \sqrt{(1 + \xi)^2 - 4\xi(1 - k^2)}}{2(1 - k^2)} \right\} \omega_2^2, \quad (2.27)$$

and

$$\omega_H = \left\{ \frac{1 + \xi + \sqrt{(1 + \xi)^2 - 4\xi(1 - k^2)}}{2(1 - k^2)} \right\} \omega_2^2. \quad (2.28)$$

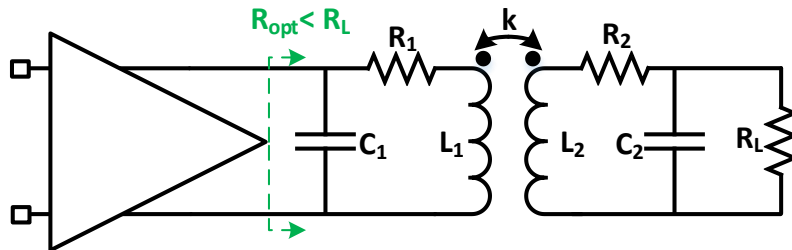


Fig. 2.8 Typical situation in the output matching of amplifier.



We usually use the high Q_s case for the output-matching network of amplifier design [10], and the schematic is shown in Fig. 2.8. The matching network parallel resonance frequencies in two different ξ cases are

$$\omega_L = \begin{cases} \frac{\omega_2}{\sqrt{1+|k|}}, & \xi = 1 \\ \omega_1, & \xi \ll 1 \end{cases}, \quad (2.29)$$

and

$$\omega_H = \begin{cases} \frac{\omega_2}{\sqrt{1-|k|}}, & \xi = 1 \\ \omega_2 \sqrt{\frac{1+k^2\xi}{1-k^2}}, & \xi \ll 1 \end{cases}. \quad (2.30)$$

Here, the impedance transformation ratio of the matching network is

$$\frac{Z_{in}}{Z_L} \cong \frac{1}{A^2}, \quad (2.31)$$

and transformed factor A are

$$A_L \cong \begin{cases} n, & \xi = 1 \\ n * k, & \xi \ll 1 \end{cases}, \quad (2.32)$$

and

$$A_H \cong \begin{cases} -n, & \xi = 1 \\ -n/(k\xi), & \xi \ll 1 \end{cases}, \quad (2.33)$$

where the turn ratio n is L_2/L_1 .

After introducing the high Q_s case, in cases where the quality factor Q_s is low, doubly-tuned networks exhibit unique behaviors that differ from their high- Q_s counterparts. As shown in Fig. 2.9 [11], when Q_s is low, the capacitance C_2 becomes



negligible because it is effectively shunted by a low load resistance R_L . This simplification causes the network to degenerate, resulting in a single parallel resonance at the frequency ω_s , which can be defined as

$$\omega_s = \frac{\omega_1}{\sqrt{1 - k^2}}. \quad (2.34)$$

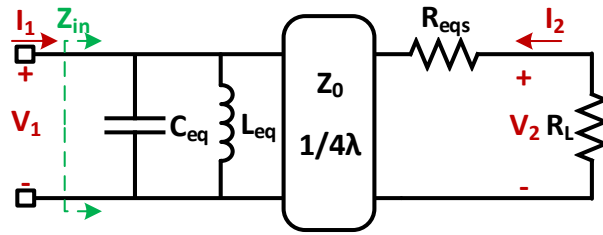


Fig. 2.9 Low-Qs case equalized model.

Near resonance, the circuit functions as an impedance inverter. This behavior is characterized by the input impedance $Z_{in}(\omega_s)$, which can be expressed as

$$Z_{in}(\omega_s) = \frac{(Z_0)^2}{R_L + R_{eqs}}, \quad (2.35)$$

and

$$Z_0 = \frac{\omega_s L_2 (1 - k^2)}{n * k}. \quad (2.36)$$

The equivalent series tank of loss resistance and the equivalent model are

$$R_{eqs} = \left(\frac{k^2 + \frac{Q_2}{Q_1}}{k^2} \right) R_2, \quad (2.37)$$

$$C_{eq} = C_1, \quad (2.38)$$



and

$$L_{eq} = (1 - k^2)L_2, \quad (2.39)$$

where Z_0 and R_{eqs} represent effective impedance and equivalent resistance parameters, respectively. This configuration allows for efficient impedance inversion, simplifying impedance transformation within the network.

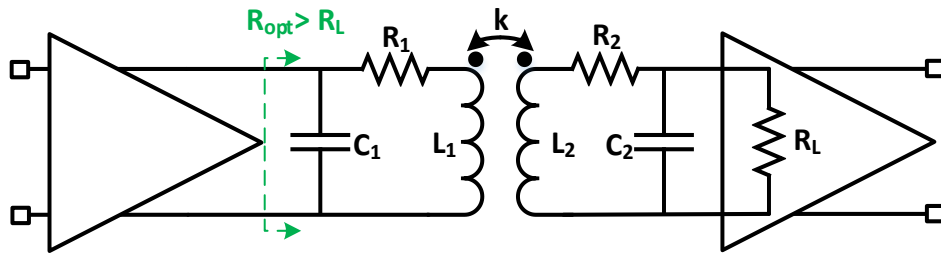


Fig. 2.10 Typical situation in the interstage matching of amplifier.

In practical applications, particularly in inter-stage matching networks, the low- Q_s configuration often emerges due to the combination of large inductors and small load resistances R_L . As shown in Fig. 2.10, this results in an effective impedance similar as

$$R_{opt} \cong \frac{(Z_0)^2}{R_L}, \quad (2.40)$$

a characteristic of low- Q_s circuits. Here, the equivalent resistance R_{eqs} can be shown as

$$R_{eqs} = n \left(\frac{\sqrt{R_{opt} R_L}}{Q_2} \right) \left(\frac{k^2 + \frac{Q_2}{Q_1}}{k(1 - k^2)} \right). \quad (2.41)$$

It can be minimized by carefully selecting parameters such as the turns ratio n and optimizing the magnetic coupling coefficient k . Minimizing R_{eqs} is essential for



enhancing network efficiency and achieving the desired impedance transformation. The optimal value of magnetic coupling k plays a crucial role, as it directly impacts R_{eqs} and, thus, the overall performance of the inter-stage matching network. By adjusting these parameters, designers can balance the trade-offs between inductor size, coupling, and network losses.

2.5 Extended Matching Network [12]-[13]

The design of RF impedance matching networks often requires impedance transformers, especially in applications that demand broadband performance. However, in III-V semiconductor processes, such as GaAs (gallium arsenide), there are significant design challenges due to the limited availability of metal layers. Unlike CMOS technology, which typically offers multiple layers of metal interconnects, III-V processes have fewer metal layers available. This limitation makes it difficult to design efficient monolithic transformers with good magnetic coupling.

To address these challenges, equivalent models such as the T-model and the π -model are often used to replicate the behavior of transformers in RF designs. These equivalent models simplify the design, reduce physical complexity, and provide a practical solution for implementing impedance-matching networks without relying on actual magnetic transformers.

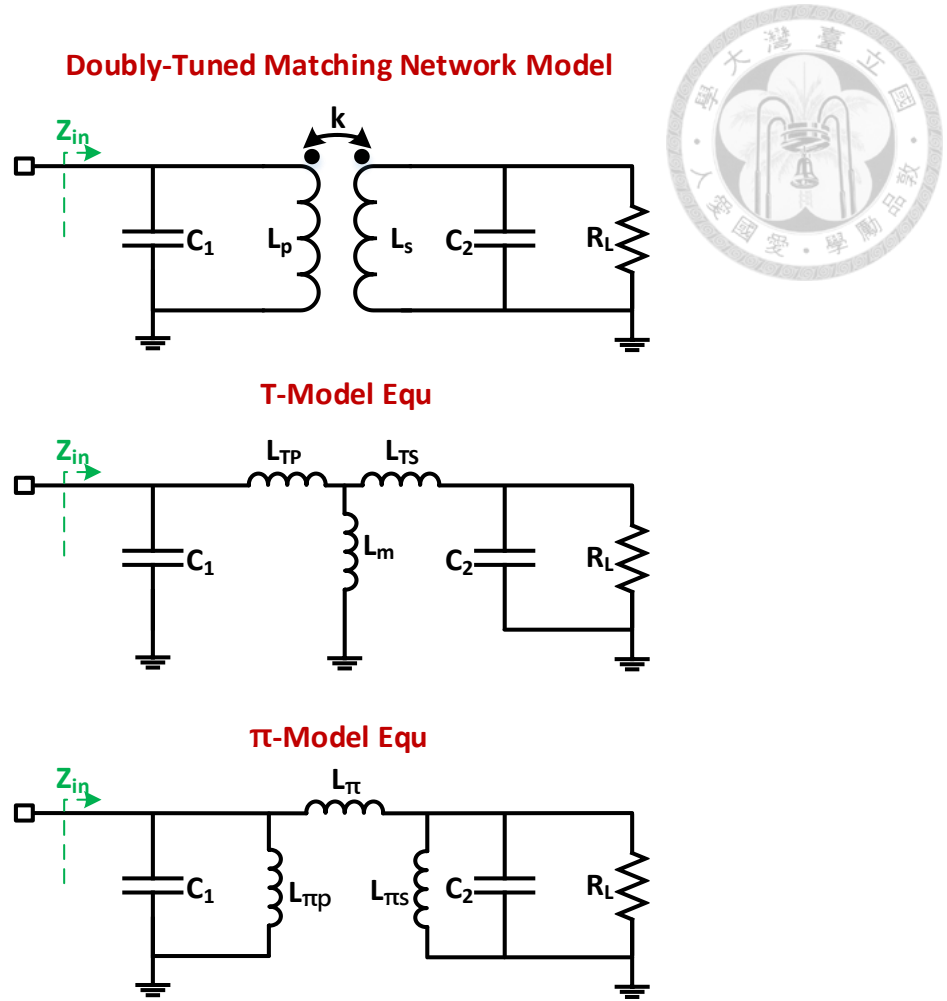
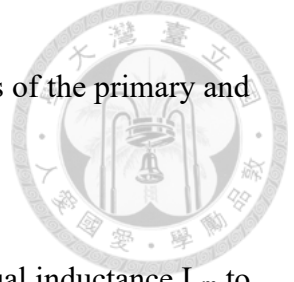


Fig. 2.11 Doubly-tuned matching network with T and π model equivalent [12].

The equivalent models—T-model and π -model—represent the behavior of the transformer by using lumped components, such as inductors and capacitors, making them easier to implement in III-V processes. The models can effectively transform impedance, allowing the output stage to achieve the desired broadband characteristics.

Mutual inductance L_m is a key parameter in these models, representing the coupling behavior between the inductors L_p and L_s . The equation can be characterized as

$$L_m = k\sqrt{L_p L_s}, \quad (2.42)$$



where k is the coupling coefficient, and L_p and L_s are the inductances of the primary and secondary coils, respectively.

The T-model equivalent uses the inductances L_{TP} , L_{TS} , and mutual inductance L_m to replicate the transformer behavior. The capacitors C_1 and C_2 provide resonance, which helps with impedance matching over a wide frequency range. The impedance transformation achieved using this model ensures that the desired impedance Z_{in} matches the load impedance R_L effectively across the operating frequency band.

The inductances for the T-model equivalent are given by

$$L_{TP} = L_p - L_m, \quad (2.43)$$

and

$$L_{TS} = L_s - L_m. \quad (2.44)$$

The π -model equivalent uses inductances $L_{\pi p}$, $L_{\pi s}$, and an inductor L_π to perform impedance transformations like the T-model. The capacitors C_1 and C_2 are placed differently than the T-model, but they still provide the necessary resonant properties for impedance matching.

The inductances for the π -model equivalent are given by

$$L_{\pi p} = \frac{L_p L_s - L_m^2}{L_s - L_m}, \quad (2.45)$$

$$L_{\pi s} = \frac{L_p L_s - L_m^2}{L_p - L_m}, \quad (2.46)$$

and

$$L_{\pi} = \frac{L_p L_s - L_m^2}{L_m}. \quad (2.44)$$

For several reasons, using equivalent models such as T and π models is highly advantageous in III-V semiconductor technologies. Since III-V processes offer fewer metal layers, using actual monolithic transformers would increase the physical size and add design complexity. Equivalent models, on the other hand, use simple inductors and capacitors that can be implemented easily with the available process technologies.

The T-model and π -model provide an effective means to achieve broadband impedance matching. The equivalent models can be optimized to achieve wideband matching performance by tuning the inductance and capacitance values, essential for high-frequency applications like power amplifiers. By using equivalent models, designers can avoid the complexities of magnetic coupling between physical transformers. Instead, they can use well-defined lumped components whose values are easier to adjust and control during the design and manufacturing. Fig. 2.12 shows the co-work references schematic [13], providing the design of a 6th-order matching network based on the T-model. In this design case, when the Z_{in} is $25 \Omega \parallel 290 \text{ fF}$, and the RL is 50Ω , three types of matching networks of the bandwidth are shown in Fig. 2.13. The proposed 6th-order extended MCR matching network will improve by 10 % compared to the MCR network.

In RF circuit design for III-V semiconductor processes, using equivalent models such as the T-model, π -model, and extended T/ π model provides a practical solution for

achieving impedance transformation without relying on physical transformers. These models reduce the complexity of design, make it easier to fabricate matching networks, and ensure broadband performance, which is essential for many high-frequency applications. The formulations for these models are derived based on mutual inductance and coupling between inductors, allowing the behavior of the transformer to be captured effectively in the absence of complex multi-layer metal structures.

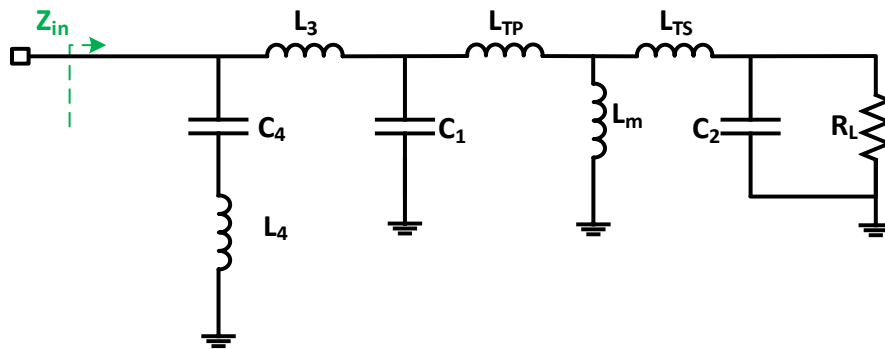


Fig. 2.12 Extended T-model matching network [13].

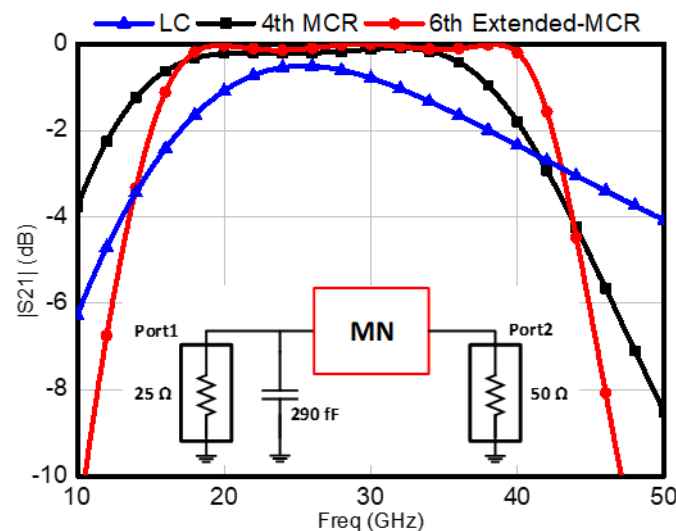


Fig. 2.13 Bandwidth comparison of LC, 4th and 6th order T-model-based matching network [13].

2.6 Summary



Chapter II focuses on enhancing bandwidth in mm-wave power amplifiers, beginning with the implications of CMOS technology scaling, which allows faster transistors but introduces challenges such as reduced breakdown voltage, limiting linearity, and overall circuit performance. The chapter elaborates on the three main transistor operating regions—weak inversion, strong inversion, and velocity saturation—and how each affects high-frequency circuits' power, speed, and efficiency. It then explores bandwidth enhancement techniques, starting with RLC tank circuits and applying the Bode-Fano limit to balance bandwidth and efficiency while minimizing losses. MCR is introduced as an effective method for achieving wide bandwidth and impedance matching through magnetic coupling, creating multiple resonant peaks that help maintain performance across a broader frequency range. Transformer-based doubly-tuned matching networks are analyzed for their role in impedance transformation, with detailed discussion on high-Qs and low-Qs scenarios, illustrating their impact on resonance behavior and impedance matching efficiency. The chapter concludes by presenting extended matching networks, including T-model and π -model equivalents, beneficial for III-V semiconductor processes with limited metal layers. These models simplify impedance transformation without relying on physical transformers, offering practical solutions for achieving wideband impedance matching and optimizing mm-

wave power amplifier performance.



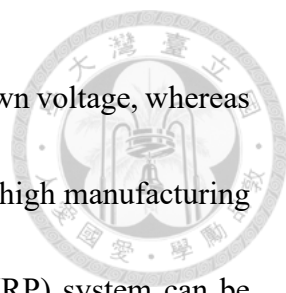
Chapter 3 Millimeter-wave Wideband High-power GaAs pHEMT Power Amplifier



3.1 Introduction

In recent years, wireless communication technology has rapidly evolved to meet the growing demand for higher data rates in emerging applications. The lower-frequency spectrum below 6 GHz has become increasingly congested, prompting a global shift towards utilizing millimeter-wave frequencies to develop 5G and 6G communication systems [13]-[42]. As part of the Beyond 5G (B5G) and 6G landscape, satellite communications have gained significant attention, with certain frequency bands overlapping with the Ka-band used for 5G. This overlap provides diverse applications, including backup data communication, environmental monitoring, disaster prevention, and maritime IoT. Companies like SpaceX [41] and Amazon [42] are deploying low Earth orbit satellites, enhancing accessibility in the market. Power amplifiers (PAs) are critical in wireless communications, ensuring signal integrity in long-distance and high-interference environments. High-power, high-efficiency broadband PAs are crucial to meeting modern communication systems' increasing complexity and performance requirements.

Various millimeter-wave PAs for 5G/6G applications have been developed using CMOS/SiGe [31]-[32], [36]-[41], GaN HEMT [18], and GaAs HEMT processes. CMOS



PAs are constrained by limited output power due to their low breakdown voltage, whereas GaN HEMT PAs, although capable of high output power, come with high manufacturing costs. A cost-effective high equivalent isotropic radiated power (EIRP) system can be achieved using GaAs PAs, leveraging power combining and beamforming techniques. The growing interest in wideband and dual-band PA design for covering global 5G/6G operating bands has led to numerous developments aimed at K-/Ka-band applications.

To achieve wideband or dual-band characteristics, various techniques have been explored, including tunable and reconfigurable matching networks, coupled resonators, and concurrent matching networks [14]-[16], [19]-[20], [23]. While effective in achieving broadband capabilities, the harmonic and radio stub matching technique poses significant challenges for high-power PAs due to high impedance transformation ratios. The magnetically coupled resonator (MCR) matching technique [7] offers impressive broadband performance but with inherent trade-offs between bandwidth and frequency response ripple. A magnetically and capacitively coupled resonator (MCCR) matching architecture was also introduced to improve broadband performance [20], yet both approaches struggle with implementing high-power PAs due to their limitations in impedance transformation ratios.

Here presents an innovative approach for wideband GaAs high-power PA (HPA) designs. For the wideband HPA, a multi-resonance matching network with a high

impedance transformation ratio is proposed to achieve wideband performance. The proposed wideband HPA achieves 28.5 dBm P_{sat} from 24 to 32 GHz.

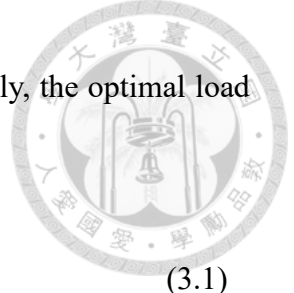


3.2 Circuit Design

The primary objective of PA design is to achieve maximum linear output power and high linearity. To reach these goals, common-source PA can utilize the transconductance model and load line matching. By understanding these concepts, designers can effectively optimize PA performance and select appropriate parameters and circuit architectures during the design process. The transistor is typically viewed as a current source with a controllable transconductance. The transconductance model provides a nonlinear current response that operates within two main regions: the cutoff region and the open channel region. The current is zero when the gate bias voltage is below the threshold voltage (V_{TH}). Once the gate bias exceeds the threshold voltage, the current increases proportionally with the gate voltage. To maintain the linear operation of the output current, the amplifier is usually biased at a quiescent current (I_Q) positioned at the midpoint of the maximum current (I_{max}). This design ensures that the amplifier operates within its linear range, reducing distortion and preserving signal linearity.

3.2.1 Power-stage and proposed multi-resonance matching network

In PA design, load line matching is a crucial factor. By selecting an appropriate load



impedance (R_{opt}), optimal linear output can be achieved. Theoretically, the optimal load impedance is defined as

$$R_{opt} = \frac{V_{DD}}{I_{max}/2}. \quad (3.1)$$

This equation ensures that voltage and current swings simultaneously reach their maximum linear values. When the amplifier's voltage swings from 0 to V_{DD} and the current swings from 0 to I_{max} , the amplifier attains the maximum linear range, thereby avoiding signal clipping or nonlinear distortion. Load line matching enables the amplifier to operate within its linear capacity, delivering higher output efficiency and stable performance.

However, the knee voltage (V_{knee}) limits the output voltage swing in practical circuits. The knee voltage is the boundary voltage that separates the linear region from the saturation region of the transistor. As the voltage approaches V_{knee} , the transistor's linear range diminishes, restricting the maximum output voltage swing. Consequently, the calculation for optimal load impedance must consider the impact of the knee voltage. With the knee voltage considered, the formula for optimal load impedance is modified as

$$R_{opt} = \frac{V_{DD} - V_{knee}}{I_{max}/2}. \quad (3.2)$$

The presence of the knee voltage directly affects the maximum linear output power, which can be expressed as

$$P_{out} = \frac{(V_{DD} - V_{knee})^2}{2R_{opt}}. \quad (3.3)$$

This equation illustrates the impact of the knee voltage on output power and highlights the importance of selecting an appropriate load impedance to optimize both amplifier linearity and output power. The knee voltage reduces the available power range, particularly in advanced processes where the knee voltage is a significant portion of the supply voltage, making its effect more pronounced.

In the power amplifier (PA) design, achieving a target output power of 30 dBm was critical. Using a WIN process with $V_{DD}=5$ V, $V_{DD,MAX}=10$ V, and $V_{knee}=1$, we determined that an optimal load impedance R_{opt} of $8\ \Omega$ was required. The transistor size was calculated to be approximately $1600\ \mu\text{m}$ to deliver the required current for maintaining linearity and output power, ensuring that the PA meets both power and efficiency specifications. Fig. 3.1 shows the transistor's transconductance with $V_{DD}=5$ V.

After examining several transistor configurations shown in Table 3.1, it was determined that using four transistors in parallel, each with a gate width of $100\ \mu\text{m}$, achieved satisfactory Class A operation. With a gate bias of $V_g=-0.5$ V and a drain bias of $V_{DD}=5$ V, this setup produced a power-added efficiency (PAE) of 51.9% and a saturation output power (P_{sat}) of around 30.6 dBm. Moreover, the optimized load impedance ($Z_{opt}=3.5+j4.9\ \Omega$) was less than the calculated R_{opt} , indicating this configuration was efficient for high-power operation.

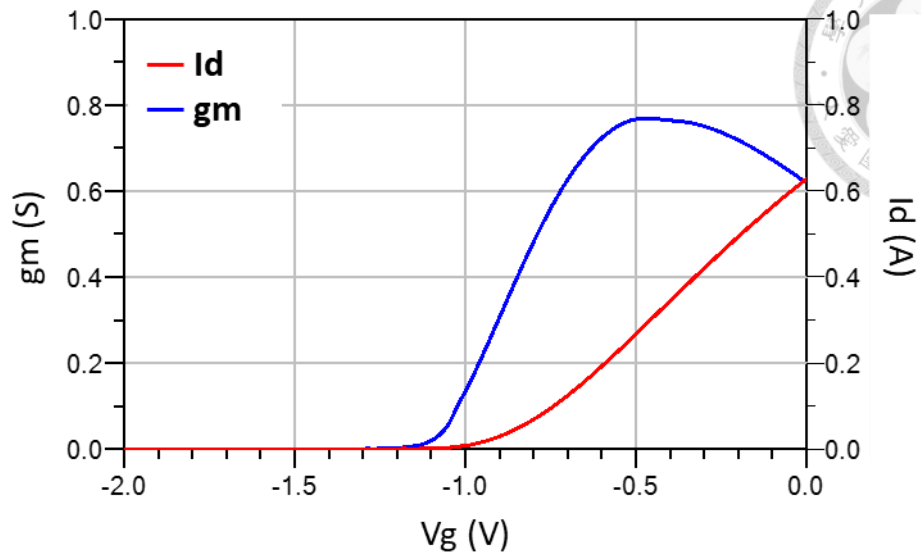


Fig. 3.1 Transistor size 1600 μm performance.

Table 3.1 The power performance results with the total width of 1600 μm at 28 GHz.

Size (μm)	V_g (V)	Gain (dB)	PAE (%)	P_{sat} (dBm)	Z_{opt} (Ω)
4*100//4	-0.5V	6.3	51.9	30.4	3.5+j4.9
8*50//4	-0.5V	6.3	41.3	30.1	2.6+j3.4
8*100//2	-0.5V	5.5	41.4	29.5	5.7+j0.4

For the power stage, the total gate periphery was set at 1600 μm by using four transistors with a 100 μm gate width each. Adding an odd-mode resistor and optimizing

output power with load-pull techniques showed that Z_{opt} of $3.9+j0.05 \Omega$ was obtained under a Class A bias condition at 28 GHz. However, it was observed that under these conditions, the MCR T-model resulted in an inductor (L_m) larger than required for the bandwidth, rendering the T-type matching network impractical. Consequently, the MCR-based design did not apply to this high-power amplifier.

In high-power amplifier design, the dual-band matching network offers a solution for high-impedance transformation over a broad bandwidth, as shown in Fig. 3.2. This network utilizes two L-type equivalent circuits to address matching requirements at different frequency bands, particularly at low frequency (f_1) and high frequency (f_2), enabling dual-band characteristics. The design equations for the matching network allow for the calculation of the required inductance and capacitance values for each stage as

$$\frac{1}{\omega_{f1}L_p} - \omega_{f1}C_p = \frac{1}{\omega_{f1}L_{f1}}, \quad (3.4)$$

$$\omega_{f2}C_p - \frac{1}{\omega_{f2}L_p} = \omega_{f2}C_{f2}, \quad (3.5)$$

$$\frac{1}{\omega_{f1}C_s} - \omega_{f1}L_s = \frac{1}{\omega_{f1}C_{f1}}, \quad (3.6)$$

$$\omega_{f2}L_s - \frac{1}{\omega_{f2}C_s} = \omega_{f2}L_{f2}, \quad (3.7)$$

where $\omega_{f1} = 2\pi f_1$ and $\omega_{f2} = 2\pi f_2$.

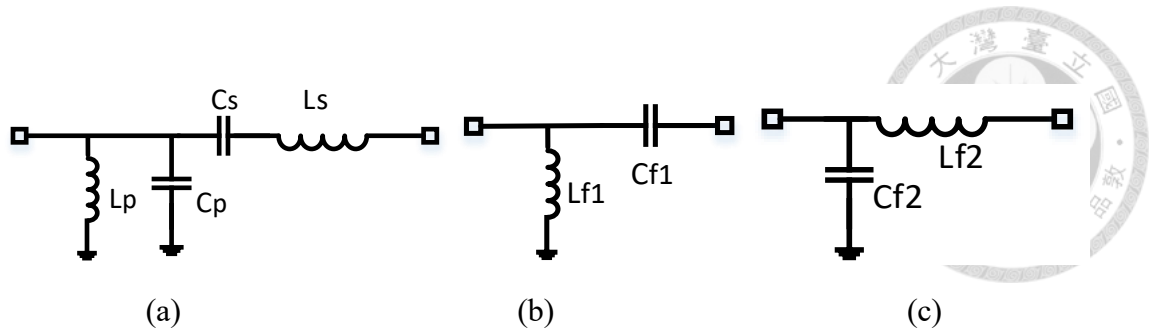


Fig. 3.2 Reference [26], (a) Dual-band matching network and its L-type equivalent circuits at (b) low frequency (f_1), and (c) high frequency (f_2).

The dual-band network enables precise impedance matching within specific dual-frequency ranges through these equations. However, the inductance and capacitance combinations in the L-type matching circuit exhibit forbidden regions shown in Fig. 3.4, making it unsuitable for achieving high impedance transformation rates. To overcome the limitations of the traditional MCR model, Fig. 3.3 shows the proposed multi-resonance matching network to provide a broader impedance transformation range, covering frequencies from 24 to 32 GHz. Cause this circuit is a single-end design, we need to check the odd mode stability issue using the binary combining network. Here, we add the odd mode stability resister in the combining network. The result of odd mode stability is shown in Fig. 3.4. After adding the odd mode resister, the full band stable factor will be over 1. This network extends the effective bandwidth through a multi-stage configuration of inductors and capacitors, as shown in Fig. 3.5, with the trans-impedance given by

$$Z_{2I} = \frac{\omega C_2 L_1}{jL_3 C_1 C_2 C_3 (L_1 + L_2) \omega^4 - j(C_2 C_3 L_3 + ((C_1 + C_2) C_3 + C_1 C_2)(L_2 + L_1)) \omega^2 + j(C_2 + C_3)} \quad (3.8)$$

This multi-resonance architecture identifies two main pole frequencies by adjusting the system's characteristic roots, ensuring the network's bandwidth requirements are within the operating range. The results demonstrate that this design can maintain a high impedance transformation ratio between 21 and 33 GHz. Fig. 3.6 illustrates the advantages of the multi-resonance matching network over the conventional MCR method, providing a broader matching bandwidth.

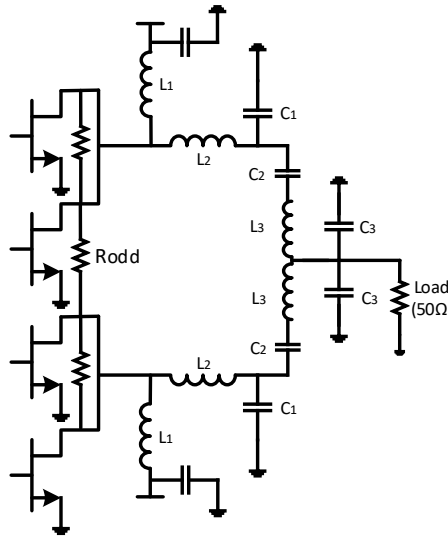


Fig. 3.3 Proposed high-impedance-transformation-ratio of the multi-resonance matching network.

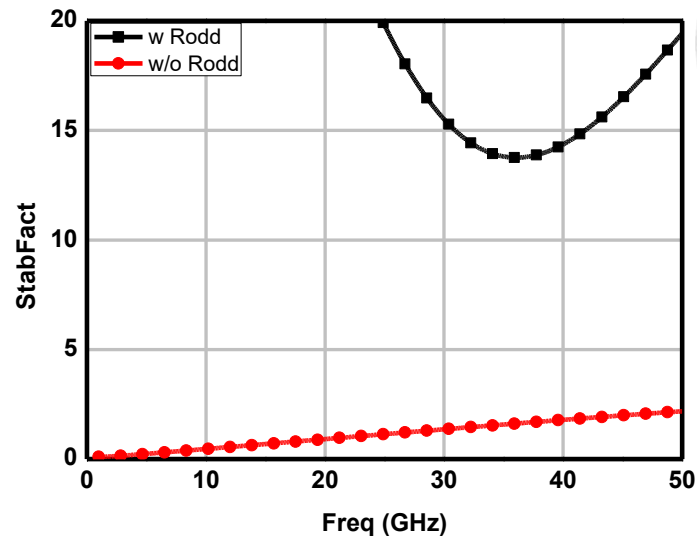


Fig. 3.4 Odd mode stability simulation after adding odd mode resistor.

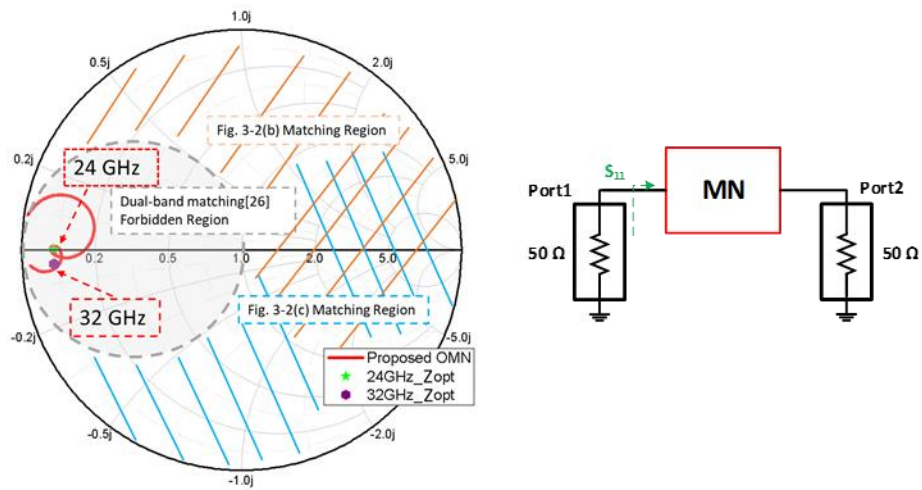


Fig. 3.5 Impedances of the proposed high-impedance-transformation-ratio multi-resonance matching network and the forbidden region of ref [26].

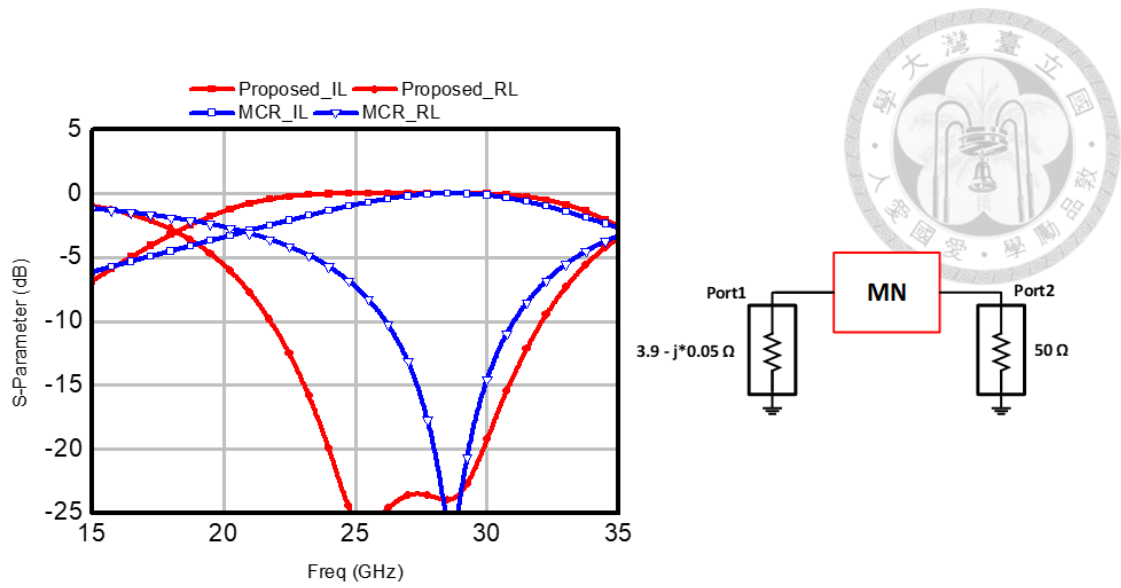


Fig. 3.6 S-parameters of the MCR and the proposed multi-resonance matching network.

Furthermore, large-signal characteristics at different frequencies indicate that, after the output stage matching EM results as shown in Fig.3.7, the maximum PAE occurs at input powers of 23 dBm for 28 GHz, respectively. The corresponding maximum PAE values are 37.9 %, with output powers of 29.9 dBm. This analysis suggests that approximately 22.5 dBm of drive power is required for the output stage to achieve maximum PAE at these frequencies. Accounting for an estimated inter-stage matching loss of 2 dB, the driver stage must deliver an output power over 24.5 dBm to ensure sufficient drive for the output stage, achieving optimal efficiency and performance.

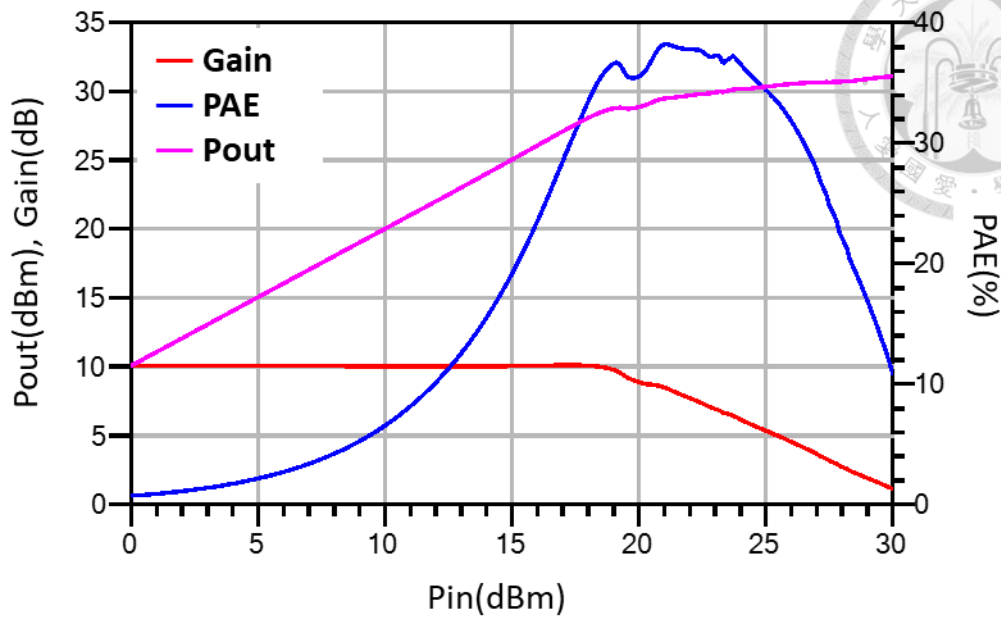


Fig. 3.7 28 GHz power performance with OMN.

3.2.2 Driver-Stage and Matching Network

The driver stage in this design has an output of 24.5 dBm, with an OP_{1dB} (Output Power at 1 dB Compression Point) that exceeds 24.5 dBm, ensuring the driver operates with sufficient headroom to maintain linearity and gain stability. This power level feeds into the inter-stage matching network, which introduces a 2 dB loss, reducing the signal to 22.5 dBm before it enters the power stage. Fig. 3.8 shows the power budget of the proposed PA.

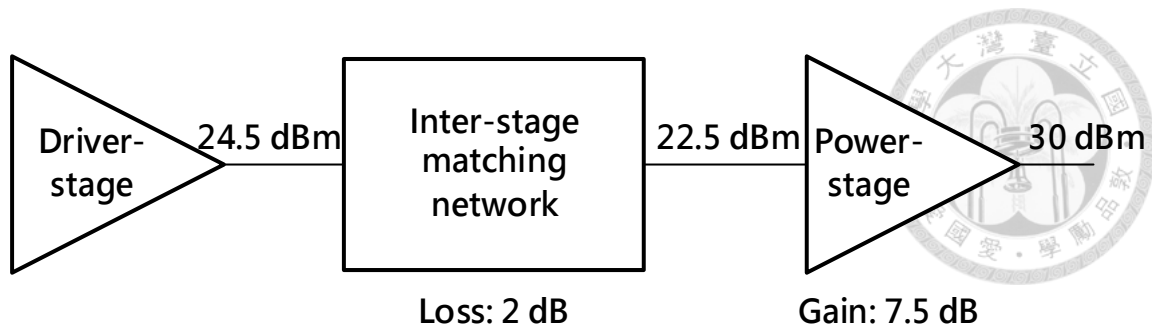


Fig. 3.8 Power budget of the proposed wideband high-power PA.

This design selected transistors with a total gate width of $800\ \mu\text{m}$ ($4 \times 100\ \mu\text{m}$), operating at $V_{\text{DD}} = 5\ \text{V}$ and $I_{\text{ds}} = 78.5\ \text{mA}$. This configuration provides adequate power to drive the subsequent stages without pushing the device into non-linear regions, particularly at higher frequencies. To mitigate instability across the operational frequency band, an RC stabilization circuit was incorporated, as shown in Fig. 3.10, providing a steady response throughout the frequency range.

Fig. 3.9 shows that an asymmetric MCR architecture was utilized for inter-stage matching. The distinct characteristic of this network is its high-quality factor on the right side, which connects to the high-impedance input of the power stage, contrasted with a low-quality factor on the left side. This asymmetry is essential for balancing the design's bandwidth and efficiency. Since transistors exhibit their maximum gain at lower frequencies, they inherently behave like a low-pass filter, which constrains higher-

frequency performance. Therefore, the inter-stage matching network was configured to create a high-pass response, helping extend the amplifier's effective operating range by compensating for the inherent low-pass behavior of the transistors.

The broadband S-parameter response achieved through this network, as shown in Fig. 3.10, demonstrates the network's ability to handle a wide frequency range, essential for ultra-wideband performance. The insertion loss graph illustrates the efficiency of both the input matching network (IMN) and inter-stage matching network (ISMN), showing minimal loss across the desired frequency band, with some minor losses at the extremes.

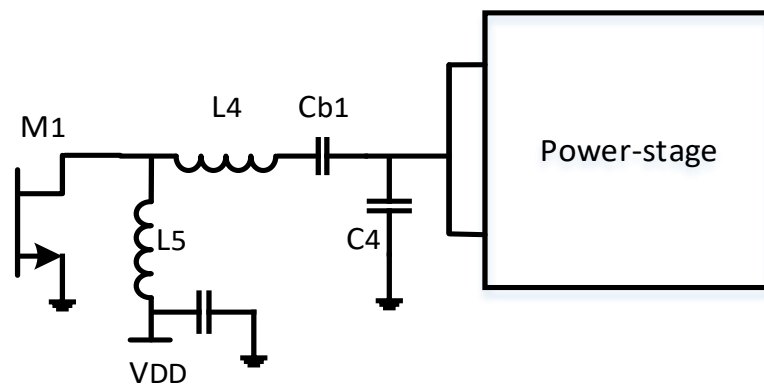


Fig. 3.9 Inter-stage matching network of the proposed wideband high-power PA.

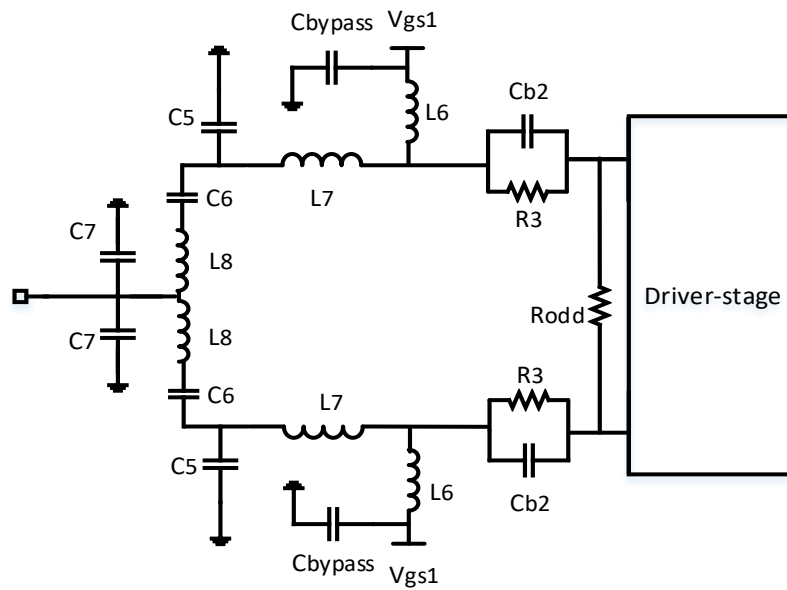


Fig. 3.10 Input-stage matching network of the proposed wideband high-power PA.

The input matching circuit, shown in Fig. 3.10, utilizes a band-pass filter structure comprising a multi-stage LC network and an RC stabilization component. This design and the conjugate matching at the input transistor maintain a flat gain profile and meet the amplifier's broadband requirements. A parallel resistor in the primary matching network helps lower the Q factor, widen the bandwidth, and reduce input return losses, improving overall broadband performance. Moreover, the RC stabilization branch effectively suppresses low-frequency oscillations by introducing damping through the resistor, while the capacitor ensures higher-frequency signals pass with minimal

attenuation. This approach enhances system stability at lower frequencies without significantly degrading the amplifier's maximum gain at the desired operating bandwidth.

In summary, the driver-stage matching network and inter-stage matching architecture ensure stability, broadband matching, and effective power transfer between stages, ultimately leading to a balanced design that maximizes gain and efficiency across the operational frequency range.

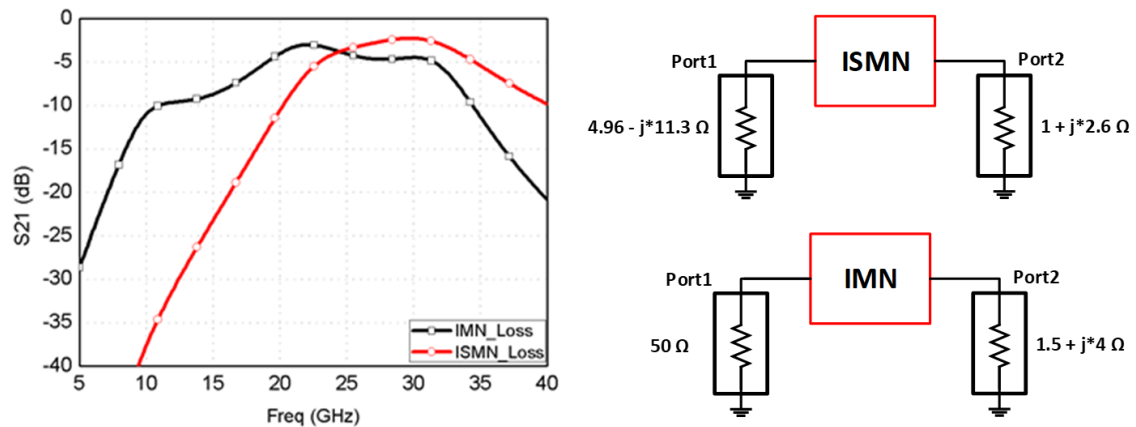


Fig. 3.11 Simulated insertion loss of the interstage and input matching networks of the proposed PA.

3.2.3 Circuit Schematic and Simulation Results

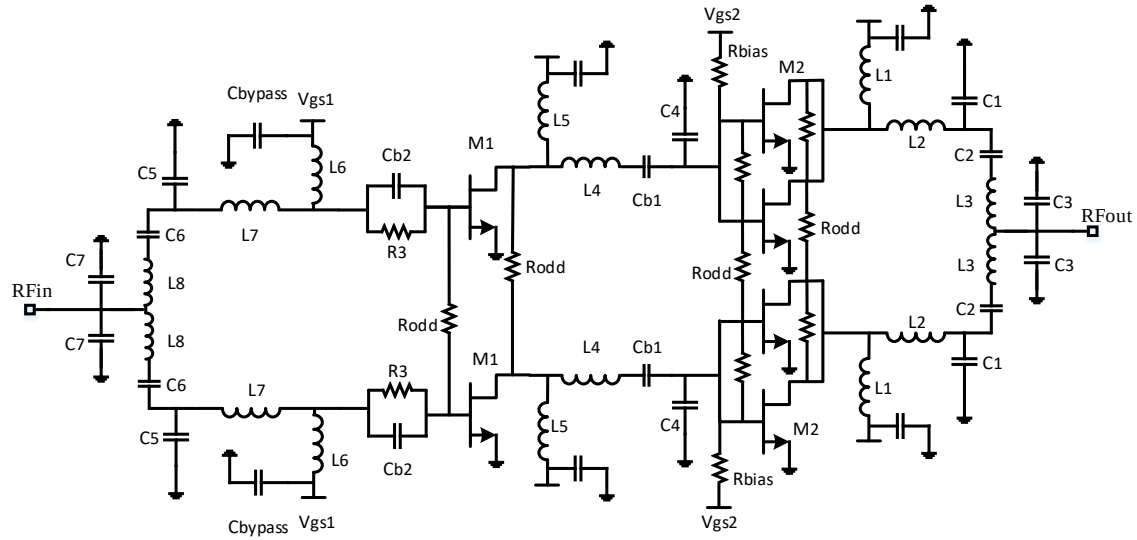


Fig. 3.12 Complete equivalent elements schematic of the proposed wideband-high-power PA.

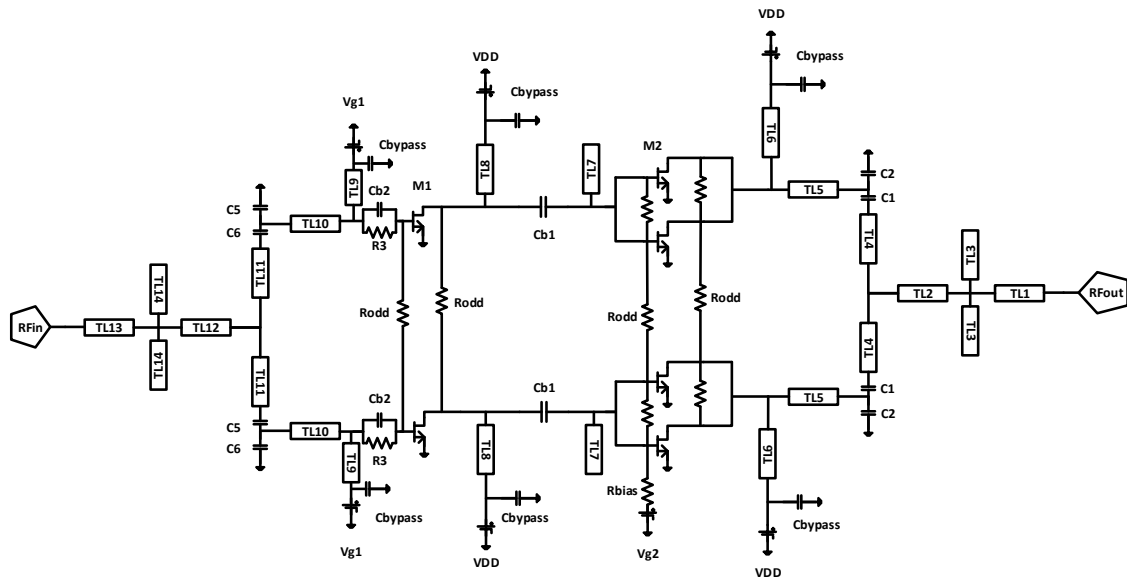
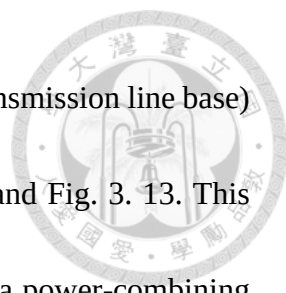


Fig. 3.13 Complete schematic of the proposed wideband-high-power PA.

Table 3.2 Values of equivalent model and device of the proposed PA.

Element	Value	Element	Value
M_1	4x100 μ m	R_3	48 Ω /60 Ω
M_2	4x100 μ m	R_{odd}	20 Ω
V_{DD1}	5V	$L_1/L_2/L_3/L_4$	54.6pH/35.3pH/412pH/15pH
I_{D1}/V_{gs1}	78.5mA/-0.65V	$C_1/C_2/C_3$	0.53pf/0.24pf/0.11pf
I_{D2}/V_{gs2}	271mA/-0.5V	$L_5/L_6/L_7/L_8$	105pH/148pH/40pH/360pH
C_{b1}/C_{b2}	1.2pF/0.47pF	$C_4/C_5/C_6/C_7$	0.2pF/0.59pF/0.25pF/0.17pF
Element	Value (WxL)	Element	Value (WxL)
TL ₁	40×25 μ m	TL ₈	30×120 μ m
TL ₂	40×165 μ m	TL ₉	15 ×580 μ m
TL ₃	80×390 μ m	TL ₁₀	30×40 μ m
TL ₄	40× 364 μ m	TL ₁₁	30×260 μ m
TL ₅	40×40 μ m	TL ₁₂	30× 150 μ m
TL ₆	40×830 μ m	TL ₁₃	30×20 μ m
TL ₇	30× 405 μ m	TL ₁₄	45× 470 μ m



The equivalent elements schematic and complete schematic (transmission line base) of the proposed wideband-high-power PA are shown in Fig. 3. 12 and Fig. 3. 13. This design incorporates a two-stage common-source configuration with a power-combining structure to enhance power handling and bandwidth. To ensure stability across both stages, RC parallel networks are implemented, as well as odd-mode resistors to stabilize odd-mode oscillations. The amplifier employs transistors of $4 \times 100 \mu\text{m}$ dimensions with a combined width of $1600 \mu\text{m}$ and $800 \mu\text{m}$ for power and driver-stage, operating at a drain voltage of 5V. The driver stage is biased at 78.5 mA to maintain linearity and prevent compression, while the power stage is set at 271 mA for high-output efficiency. In microwave circuit design, a transmission line can be treated as an equivalent combination of lumped inductors and capacitors due to its distributed inductance and capacitance. By considering each small segment of the line to represent a series inductance and parallel capacitance, we can approximate the overall electrical behavior of the line at specific frequencies or electrical lengths with a simpler lumped-element model. This equivalence is particularly useful in practical designs because short transmission-line sections can replace discrete inductors or capacitors, reducing component count, board space, and unwanted parasitic effects. Additionally, Table 3.2 details the transistor sizes, element values, and biasing conditions.

The layout of the PA, as shown in Fig. 3.14, occupies an area of $2.4 \times 1 \text{ mm}^2$. In addition to impedance matching, output matching uses the multi-resonance of the matching network to maintain the wideband power performance and match the high impedance transformer ratio about R_{opt} to R_L . The equivalent MCR structures in the inter-stage networks facilitate power division and combination. This symmetrical MCR layout minimizes phase and amplitude imbalances, critical for maintaining broadband performance. Double metal transmission lines handle currents up to $10 \text{ mA}/\mu\text{m}$, ensuring robustness under high power. Furthermore, $30\text{-}\mu\text{m}$ wide transmission lines are used for the dynamic drain bias lines to support the current needs of both stage transistors.

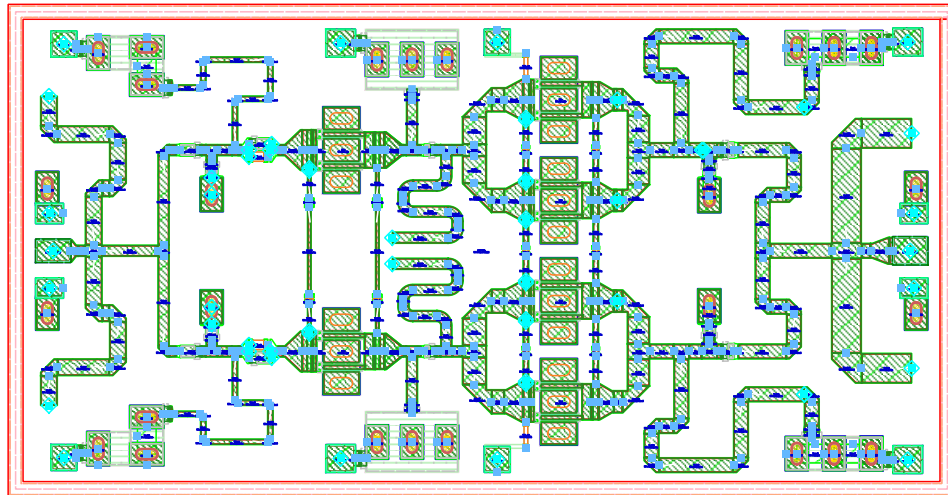


Fig. 3.14 Complete layout of the proposed wideband-high-power PA ($2.4 \times 1.1 \text{ mm}^2$).



A. Small-signal simulation

The simulated S-parameters of the proposed wideband high-power PA, shown in Fig. 3.15, show that the peak small-signal gain, S_{21} , achieves approximately 15 dB around 23.5 to 32 GHz. The input reflection coefficient, S_{11} , remains below -5 dB across a broad frequency range from 23.5 GHz to 33 GHz, indicating good input matching. The output reflection coefficient, S_{22} , is below -5 dB over the same frequency span, with dips around 23 GHz and 34 GHz, reflecting output matching characteristics.

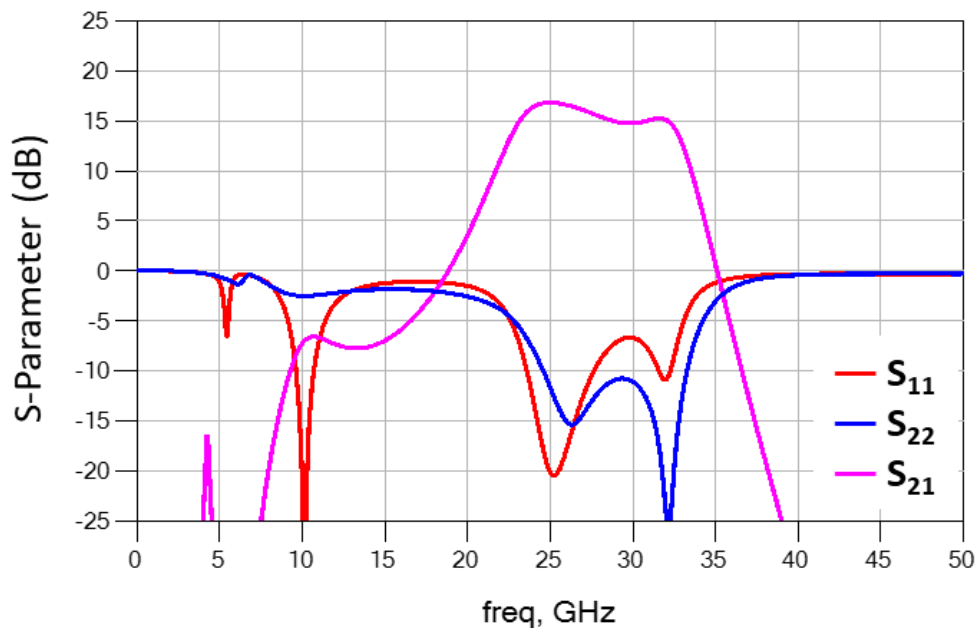


Fig. 3.15 Simulated S-parameter of the proposed wideband-high-power PA.

B. Large-signal simulation

Based on the large-signal simulation results, the power amplifier demonstrates

excellent performance across the 24 to 32 GHz frequency range. The simulated saturated output power is around 30 dBm, with a slight peak near 28 GHz. The power-added efficiency (PAE) reaches a maximum of over 32% around 26 GHz but gradually decreases to about 28% toward the edges of the frequency range. The simulated 1 dB output compression point (OP_{1dB}) remains around 28 dBm, indicating stable linear performance. These results highlight the power amplifier's good power efficiency and saturated power over a wide frequency range, as shown in Fig. 3.16.

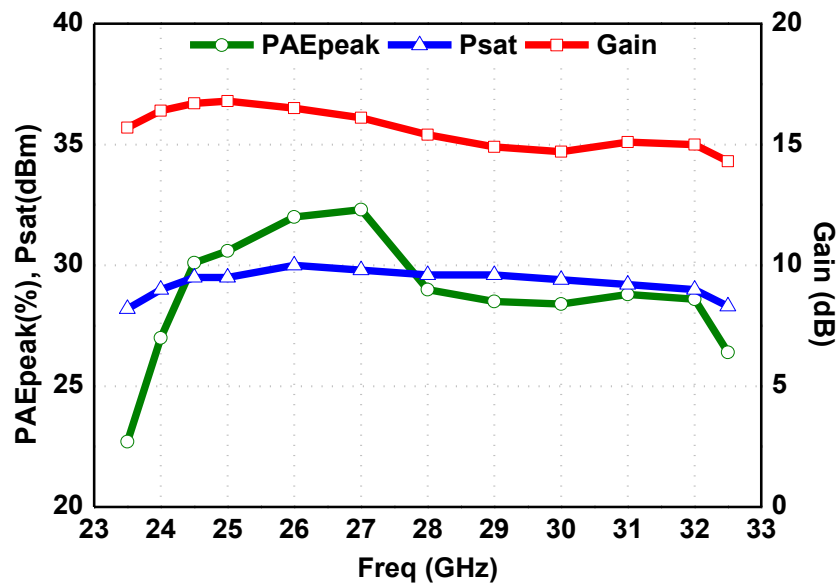


Fig. 3.16 Simulated large signal of the proposed wideband-high-power PA.

C. Stability simulation

Stability testing is essential to ensure circuit stability under various operating



conditions and frequencies, particularly in power amplifiers, RF, or microwave circuits, especially in evaluating bias and inter-stage matching. Fig. 3.17 shows an effective testing procedure that sequentially uses the Mapping Circle method, infinite transmission line simulation, input, and bias pulse injection to comprehensively assess circuit stability. Each of these steps provides specific insights into the circuit's behavior, helping to identify potential instability issues and ensuring reliable operation under real-world conditions.

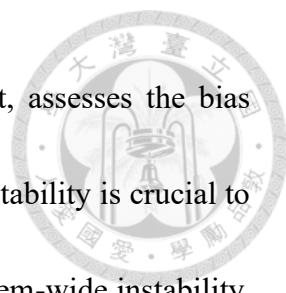
The first step in stability testing is to use the Mapping Circle method to analyze inter-stage stability, as shown in Fig. 3.18. This graphical tool evaluates the interactions between stages at different frequencies and power levels. The Mapping Circle method is advantageous in identifying stable and unstable regions during variations in gain or phase, which is especially critical in designs with high gain or multiple amplification stages where inter-stage stability is highly sensitive. This method allows designers to assess whether the circuit maintains stability across all operational bandwidths and power ranges. The Mapping Circle also helps detect frequency points that could lead to parasitic oscillations. Scanning across frequencies shows the circuit's response to inter-stage impedance matching, which helps prevent high-frequency parasitic oscillations and ensures robust performance.

Following the Mapping Circle test, the second step involves adding an infinite



transmission line to the bias supply path for bias line simulation. This step aims to replicate real-world conditions within the bias supply path, including transmission delay and parasitic effects. The infinite transmission line simulates these effects, such as delay, inductance, and parasitic characteristics, which can cause reflections or mismatches, potentially leading to instability, especially in high-frequency environments. High-frequency oscillations and parasitic behaviors are often exacerbated by parasites within the bias path. By simulating a realistic bias supply environment, this approach allows engineers to preemptively detect and mitigate bias design issues that may lead to intermittent oscillations, ensuring the circuit's stability under high-frequency operating conditions, and the result is shown in Fig. 3.19.

The third step involves injecting a pulse signal at the input to simulate sudden load changes and further assess circuit stability. Input pulse testing mimics instantaneous voltage or current changes, forcing the circuit to transition states rapidly and testing its transient response. Stability testing examines the circuit's steady-state performance and its behavior during transients. This pulse test helps observe whether oscillations, overshoots, or other instabilities arise in response to sudden input changes. This is particularly critical in real-world scenarios with unexpected load shifts, as the circuit must be capable of adapting swiftly and restoring a stable state, and the result is shown in Fig. 3.20.



The fourth step, using pulse signal injection at the bias input, assesses the bias circuit's recovery capability under transient conditions. Bias circuit stability is crucial to overall circuit stability since an unstable bias supply can lead to system-wide instability. The pulse injection emulates sudden changes in the bias supply, allowing engineers to observe whether the bias circuit can recover quickly and maintain stable voltage. This method effectively tests the bias path's responsiveness, ensuring that transient variations in bias supply do not compromise the stability of the overall circuit, and the result is shown in Fig. 3.21.

After completing all previous stability evaluations, an oscillator test (OscTest) is performed to further examine potential hidden oscillations within the circuit. As shown in Fig. 3.22, OscTest is used by inserting a test point in the suspected feedback path to break the original closed loop, measure the open-loop S-parameters, and observe the loop gain and phase to determine whether the circuit satisfies the Barkhausen oscillation condition. At some frequency, the open-loop gain is greater than or equal to 1 (0 dB), and the total phase shift is 0° (or an integer multiple of 360°). Its theoretical foundation is based on the Barkhausen and Nyquist criteria commonly used in control theory and high-frequency circuit design, meaning that the system may exhibit self-oscillation if its loop gain and phase simultaneously reach critical values. In the simulation, one can judge oscillation risk by checking whether $\text{dB}(S(2,1))$ and $\text{arg}(S(2,1))$ cross 0 dB and 0°



simultaneously, supplemented by indicators like StabFact to inspect negative resistance phenomena. Because OscTest can “open up” the feedback network in complex circuits for focused examination of loop gain, it is widely used in RF and microwave power amplifiers, oscillators, and other high-gain circuits to screen and prevent potential parasitic oscillations quickly. In this design, the results in Fig. 3.22 confirm no additional oscillation risks are observed. This indicates that the circuit remains stable under the tested conditions even after this final analysis step.

This comprehensive testing procedure examines circuit stability across inter-stage interactions, bias supply conditions, and dynamic responses, ensuring that the circuit remains stable under actual operating conditions, whether during sudden load changes, non-ideal biasing, or high-frequency environments. Identifying potential stability issues and helping to optimize design, these testing methods contribute to achieving greater circuit reliability and robustness.

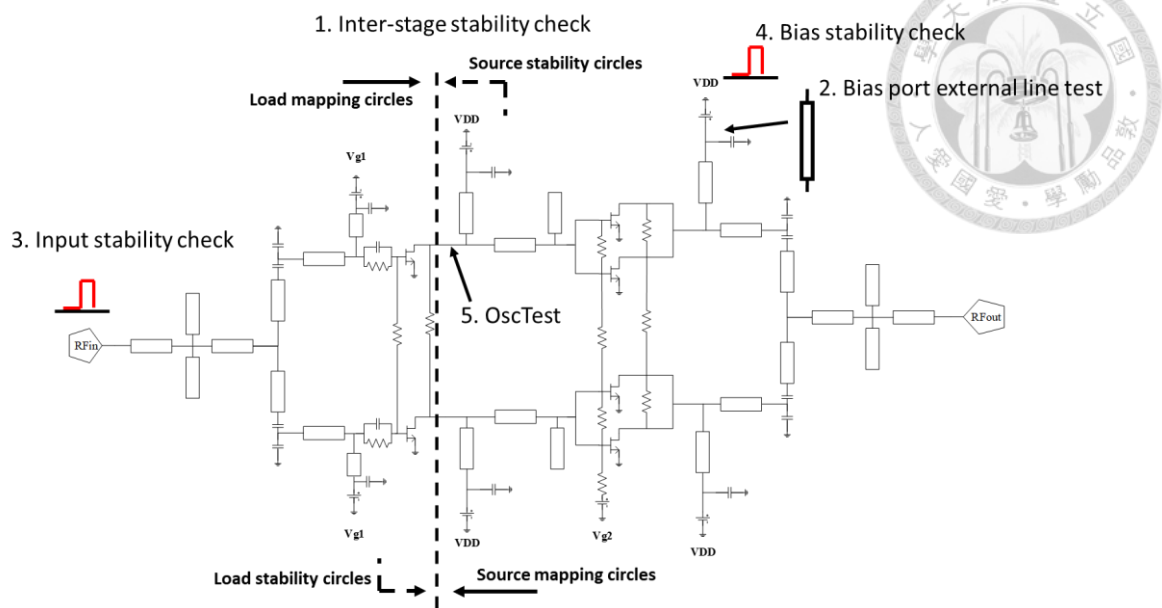


Fig. 3.17 Stability check of circuit.

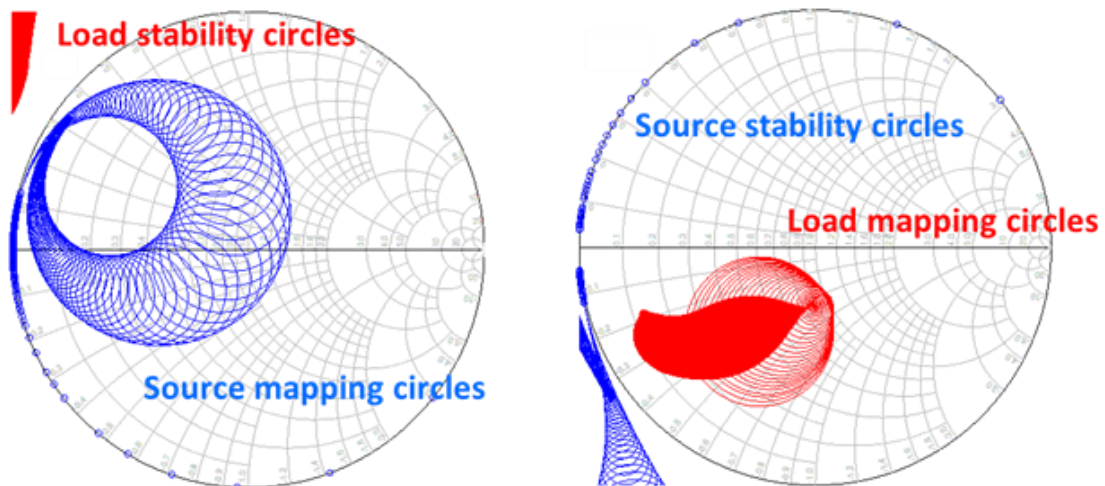


Fig. 3.18 Stability check of inter-stage from 0.1-50 GHz.

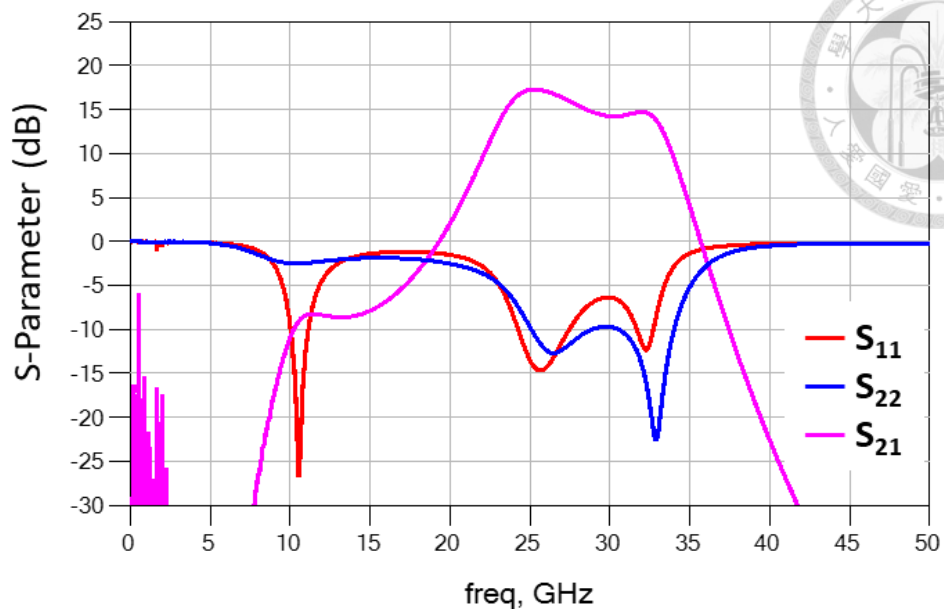


Fig. 3.19 Stability check of the testing line from bias.

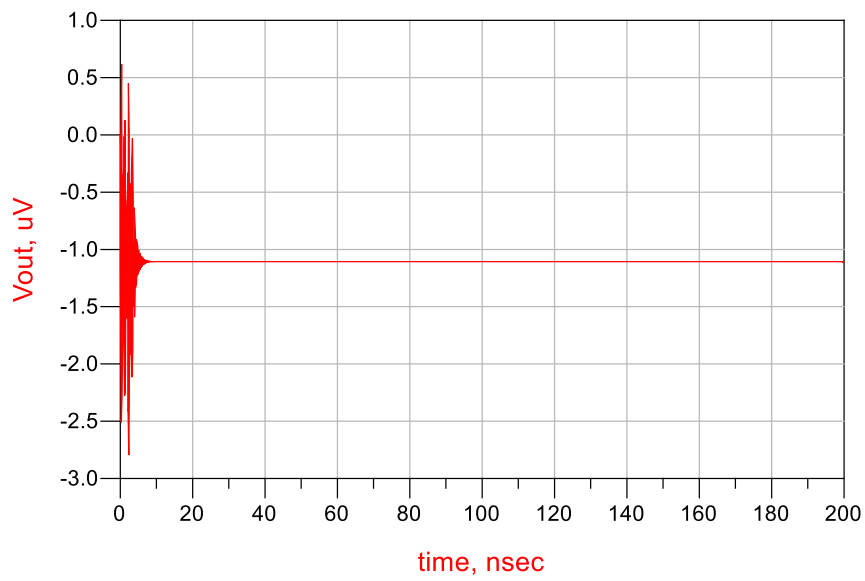


Fig. 3.20 Stability check of input pulse-testing.

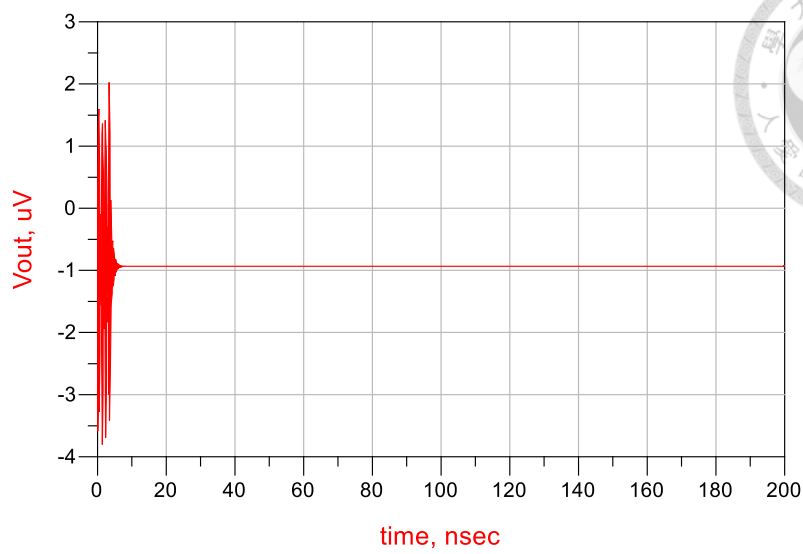


Fig. 3.21 Stability check of bias port pulse-testing.

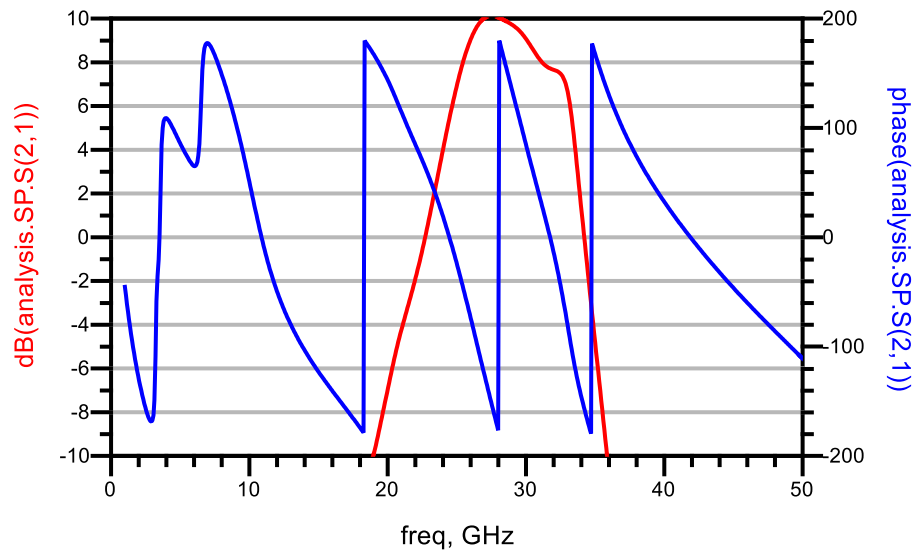


Fig. 3.22 Stability check of OscTest.

3.3 Measurement Results

The high-performance wideband HPA (High Power Amplifier) is depicted in Fig. 3.23, with a final layout optimized using EM (Electromagnetic) analysis. The chip measures $2.4 \times 1.1 \text{ mm}^2$, indicating a compact design tailored for integration in advanced systems. The measurements were conducted using GSG (Ground-Signal-Ground) probes with a $100 \text{ }\mu\text{m}$ pitch, ensuring precise connections and accurate signal transfer. Additionally, the RF pad effects were comprehensively included in both simulation and measurement, improving the results' reliability by closely matching real-world operating conditions.

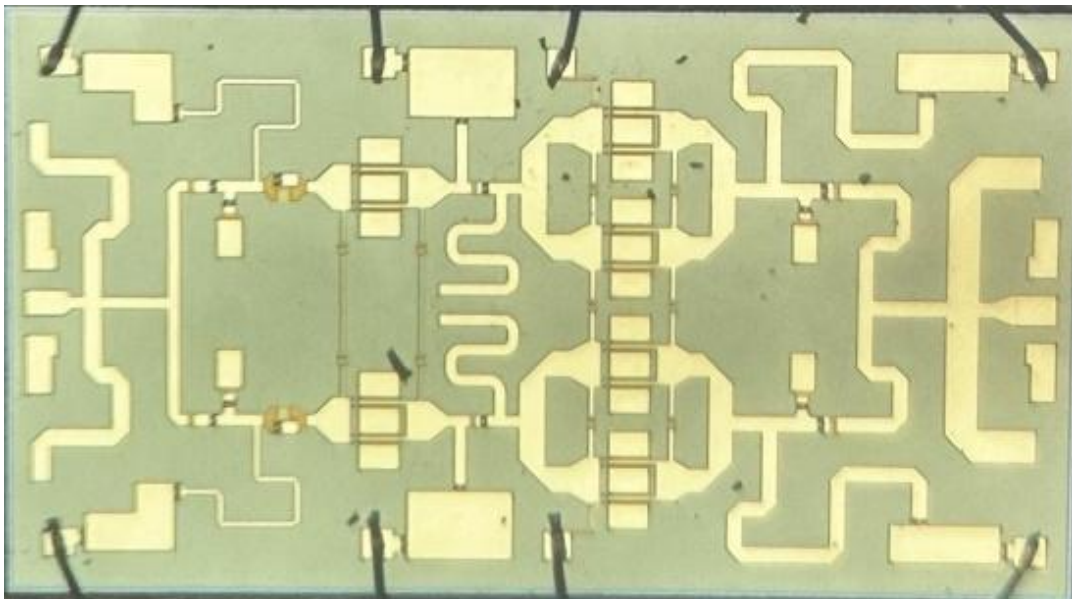


Fig. 3.23 Proposed wideband HPA chip photo ($2.4 \times 1.1 \text{ mm}^2$).

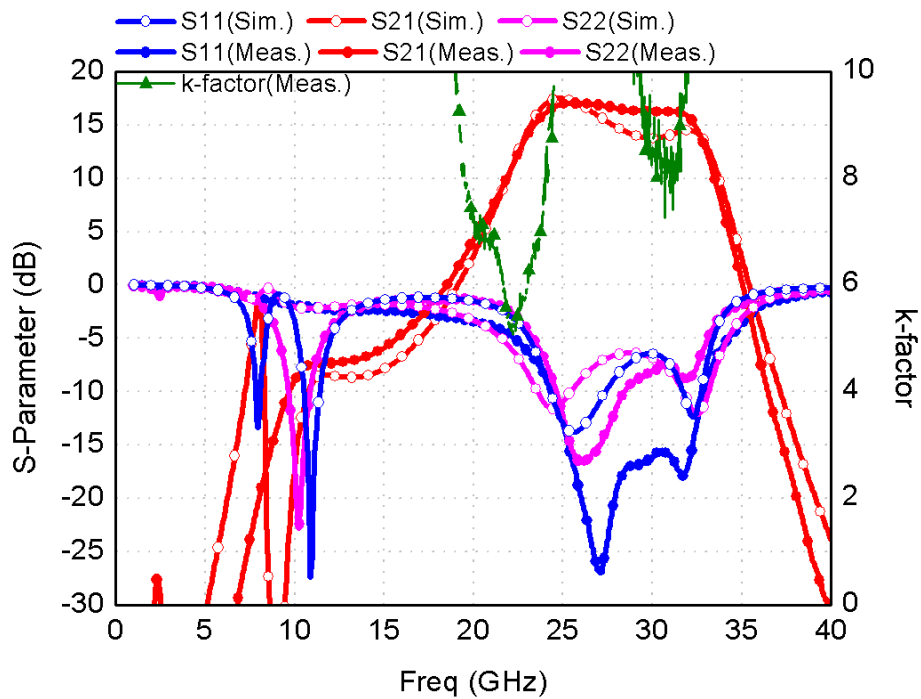


Fig. 3.24 Measured and simulated S-parameters.

Fig. 3.24 illustrates the measured and simulated S-parameters of the wideband HPA. Notably, the small-signal gain over the 24–32 GHz frequency range remains above 15 dB, averaging around 16.5 dB. This consistency in gain is essential for applications requiring stable amplification across a wide bandwidth. The input and output return losses below 3 dB confirm the amplifier's low reflection levels, ensuring efficient power transfer. The stability factor (k-factor) is measured above 1 across the entire band, ensuring stable operation without the risk of oscillations. Discrepancies between simulations and measurements are primarily due to inaccuracies in the transistor models provided in the fabrication process, while passive component models exhibit fewer errors. As a result, the

errors in the input and output reflection coefficients remain low.

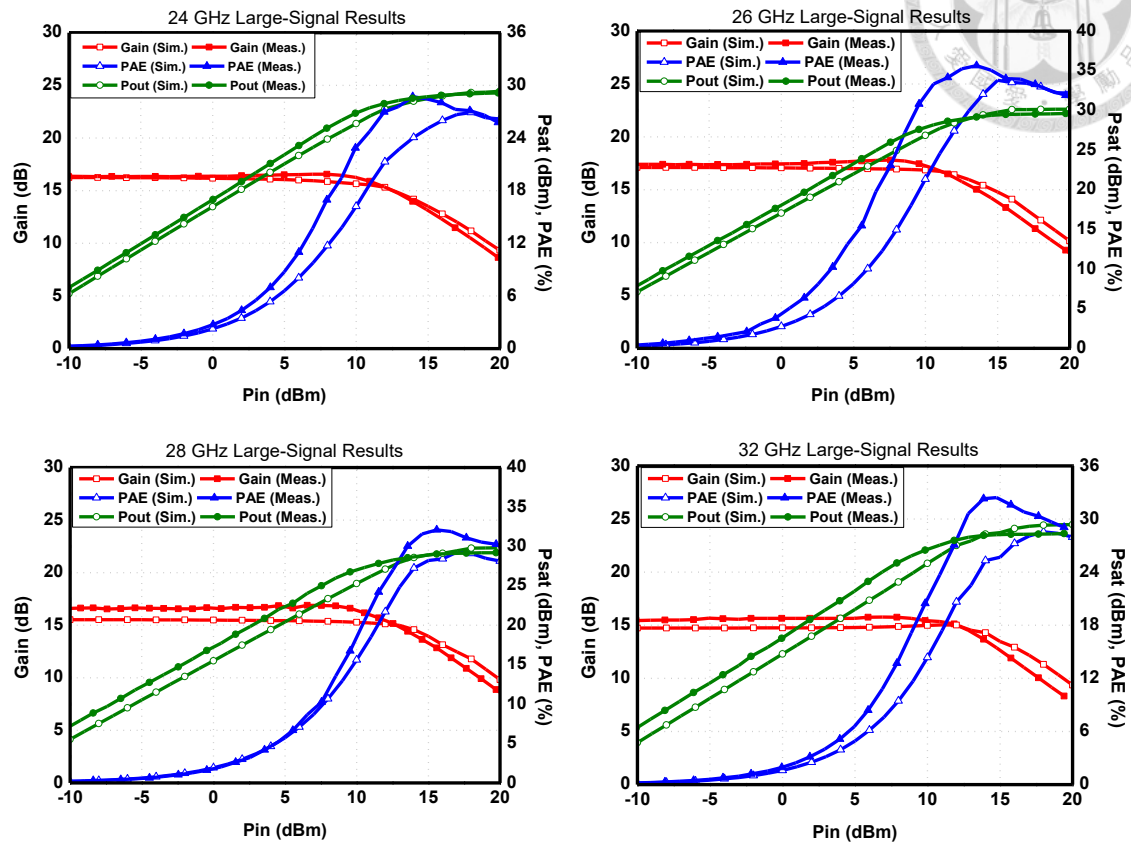


Fig. 3.25 Measured and simulated large signal results at 24/26/28/32 GHz.

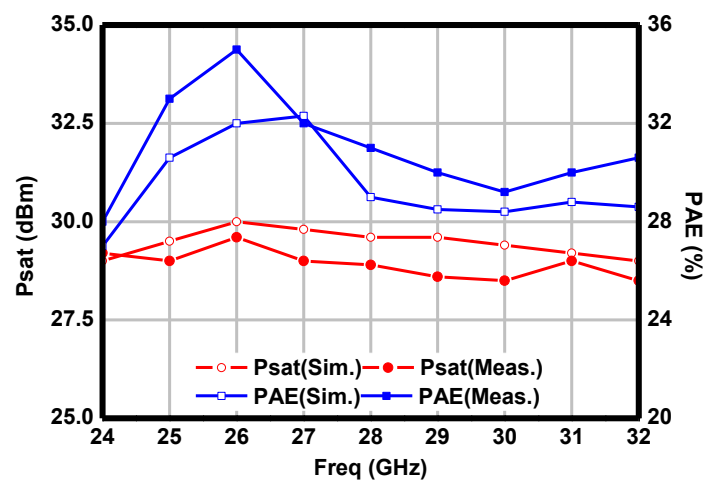


Fig. 3.26 Measured and simulated Psat and PAE results with different frequencies.

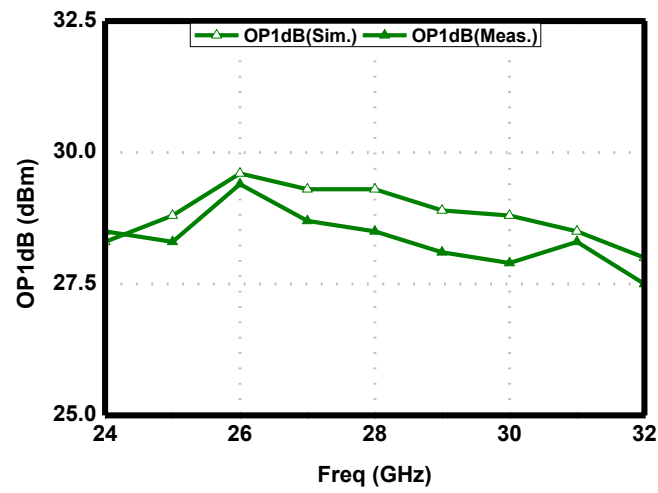


Fig. 3.27 Measured and simulated OP_{1dB} with different frequencies.

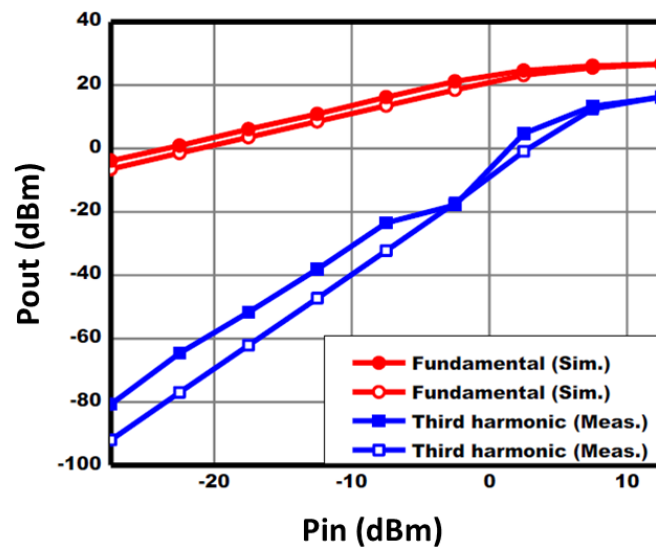
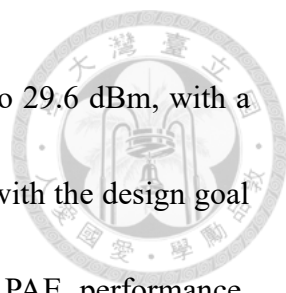


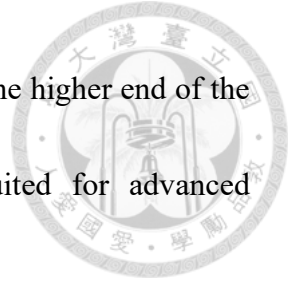
Fig. 3.28 Measured and simulated OIP3 at 28 GHz.

In Fig. 3.25, Fig. 3.26, and Fig. 3.27, the large-signal performance of the HPA is detailed, with both measured and simulated results for P_{sat} , PAE, and OP_{1dB} across the

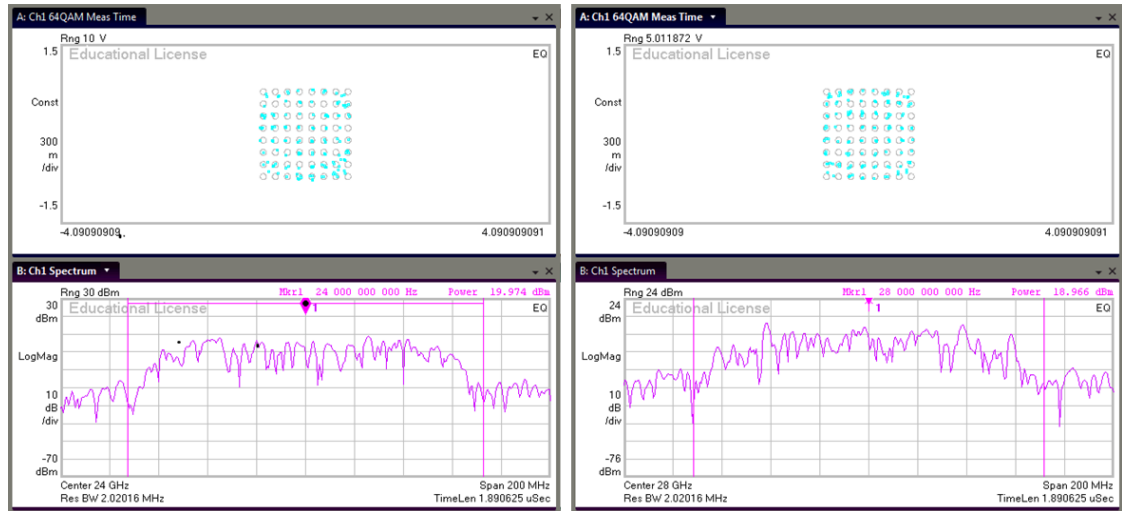


frequency range. The HPA shows output power ranging from 28.5 to 29.6 dBm, with a peak power of 29.6 dBm at 26 GHz. This high output power aligns with the design goal of maximizing signal strength for demanding applications. The PAE performance, peaking at 33% at 26 GHz, averages around 30% across the entire band, showing that the amplifier maintains good efficiency across the operating range. Additionally, the OP_{1dB} exceeds 27 dBm at 24–32 GHz, confirming that the HPA can handle high input powers with minimal gain compression, suitable for linear and non-linear applications. Two-tone signals with a 5 MHz spacing are input into the proposed PA to measure the power of both the fundamental and third-harmonic frequencies. Fig. 3.28 illustrates the simulated and measured power levels of the fundamental and third-order harmonic signals as a function of the input power. At a frequency of 28 GHz, the PA achieves a simulated Output Third-Order Intercept Point (OIP3) of 39 dBm and a measured OIP3 of 35.5 dBm.

Fig. 3.29 shows the 100 MHz symbol rate modulation results at 24/28/30/32 GHz, and Fig. 3.30 showcases the EVM (Error Vector Magnitude) performance of the broadband HPA under a 100 MHz 64-QAM (Quadrature Amplitude Modulation) signal at various frequencies. The amplifier achieves better than -25 dB EVM across the frequency band, with an average output power exceeding 22.7 dBm. This low EVM value demonstrates the HPA's ability to handle complex modulated signals with high fidelity, crucial for high-data-rate applications. At 24 and 26 GHz, the HPA delivers an average

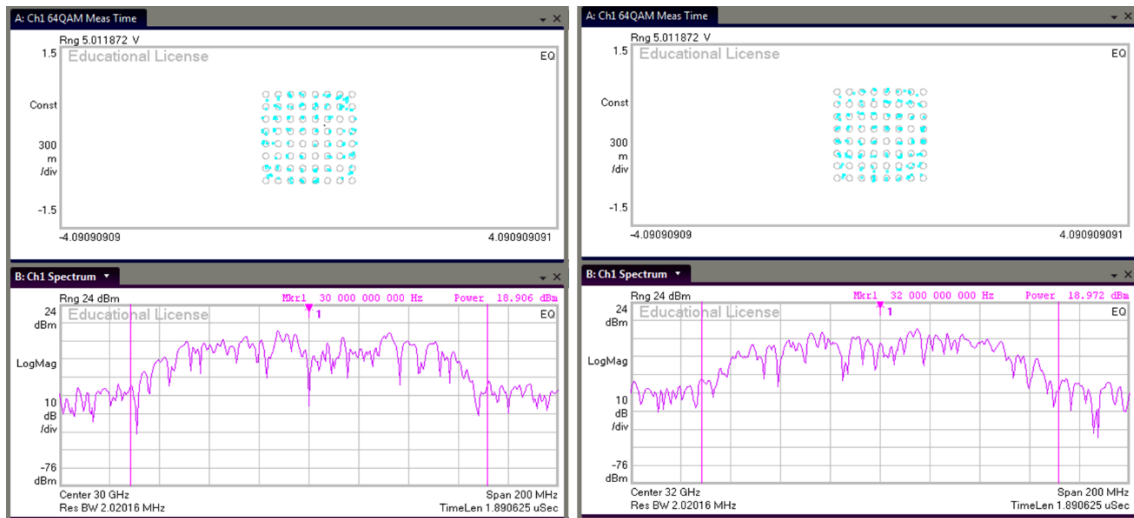


output power above 24.1 dBm, affirming its robust performance in the higher end of the band. This characteristic suggests that the amplifier is well-suited for advanced communication systems operating in challenging spectral conditions.



(a)

(b)



(c)

(d)

Fig. 3.29 Measured modulation results at (a) 24 GHz, (b) 28 GHz, (c) 30 GHz, and (d) 32 GHz.



In conclusion, the wideband HPA achieves a commendable balance between high output power, efficiency, and linearity over a broad frequency range. The measured results align closely with simulations, validating the design approach and the EM analysis used. This HPA could be a promising candidate for applications that require wideband operation, high linearity, and efficient power handling, such as in next-generation wireless communication systems and millimeter-wave technologies.

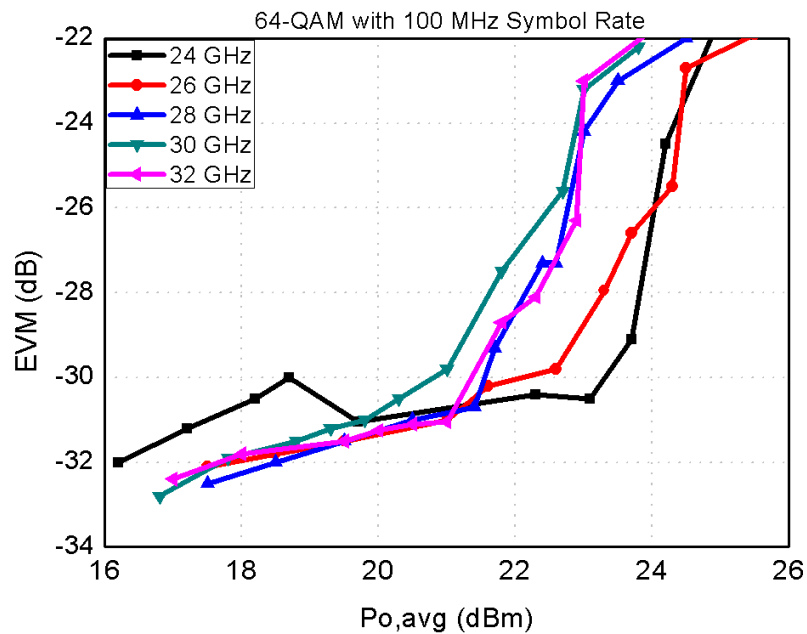


Fig. 3.30 Measured EVM results.

3.4 Summary

The K/Ka-band power amplifier designs proposed in this study, the wideband high-power amplifier (HPA), have been compared with previously published designs. In Table 3.3, our designs demonstrate significant advantages regarding FoM1 and FoM2, particularly in balancing bandwidth and output power. This advantage is further attributed to the multi-stage matching output network proposed in this work, enabling a design that achieves both wideband performance and a high impedance transformation ratio.

Compared to SiGe and CMOS processes, GaAs technology offers higher power density. The proposed designs, implemented with a 0.15 μm GaAs pHEMT process, achieve relatively high-power densities of 345 mW/mm^2 , ensuring substantial output power within a compact chip area. Additionally, HPA designs in this study show competitive performance in gain and peak power added efficiency (PAE) relative to other published designs that utilize Doherty or MCCR topologies. Within the covered frequency ranges, the proposed amplifiers achieve peak PAE values of 33%, comparable to or better than similar designs.

Our designs also demonstrate excellent wideband performance, meeting the high-frequency demands of 5G and 6G applications by covering frequency ranges from 24 to 32 GHz. This bandwidth range represents a clear advantage over most previous works focusing on narrower bandwidths. As a result, the proposed designs exhibit superior

bandwidth and output power performance compared to similar configurations in terms of process and topology.



Furthermore, using a 0.15 μm GaAs pHEMT process helps reduce fabrication costs and enhances the potential for large-scale production, making the designs suitable for 5G and 6G wireless communication systems. In summary, the PA designs presented in this work exhibit outstanding performance metrics in gain, power density, wideband capability, and peak PAE, surpassing or matching the designs in the existing literature. This makes our designs highly valuable for high bandwidth and output power applications.

Table 3.3 Performance comparison with previously published wideband and high-power PAs.

Ref	Process	Topology	Frequency (GHz)	Gain (dB)	Bias (V)	P_{sat} (dBm)	Peak PAE (%)	Chip area (mm ²)	Power density (mW/mm ²)	FOM ¹	FOM ²
12 ¹ TMTT [7]	0.15- μ m GaAs pHEMT	1-stage MCR	17-35 (69%)	9	4	23	40	1.5	560	79.3	87.8
16 ¹ CSICS [15]	0.15- μ m GaAs pHEMT	1-stage Stacked-FET	27-33 (20%)	12	12	28.5	38.4	0.88	800	85.9	82.4
18 ¹ TMTT [19]	0.15- μ m GaAs pHEMT	2-stage Doherty	28.5-31.5 (10%)	10.5	4	27	38	4.59	110	82.7	73.3
20 ¹ IMS [21]	0.15- μ m GaAs pHEMT	3-stage MCCR	20-30 (40%)	23.4	5	23	19.4	1.05	190	87.1	91.2
21 ¹ MWCL [22]	0.15- μ m GaAs pHEMT	2-stage Doherty	21-25 (17.3%)	10	5	30	37	3.79	263	82.9	80.4
22 ² ACCES S [23]	0.15- μ m GaAs pHEMT	2-stage Stacked-FET	28 / 38 (14%/10%)	18.5 / 18	10	28.5 / 28.3	39 / 36	4.59	154	91.8	85.8
21 ¹ TCSSII [36]	0.13- μ m SiGe BiCMOS	2-stage Doherty	24-29.5 (20.4%)	15.9	4	21.2	27	0.29	454	80.3	77.8
21 ¹ TCSSII [37]	28-nm CMOS	Active Capacitance	21.8-30 (31.7%)	21.2	2.2	20.3	33	0.189	529	85.3	86.4
21 ¹ TCSSII [38]	65-nm CMOS	Cascode Doherty	28	20.4	2	17.5	27	0.35	160	81.2	74.8
23 ¹ TCSSII [39]	45-nm SOI CMOS	2-stage LMB A	40	16.8	2	25.1	27.9	1.92	168	88.4	76.4
Co-work[13]	0.15- μ m GaAs pHEMT	2-stage UWB MPA	24-39 (47.6%)	17	5	24.5	31	2	140	86.5	90.3
This work [13]	0.15- μ m GaAs pHEMT	2-stage HPA	24-32 (28.5%)	17	5	29.6	33	2.64	345	90.3	90.5

Power density: P_{sat} / Area .
FOM¹: $\text{Gain(dB)} + P_{sat}(\text{dBm}) + 20\log(\text{Freq. (GHz)}) + 10\log(\text{PAE}_{max}(\%))$.
FOM²: $\text{Gain(dB)} + P_{sat}(\text{dBm}) + 20\log(\text{BW}(\%)) + 10\log(\text{PAE}_{max}(\%))$.

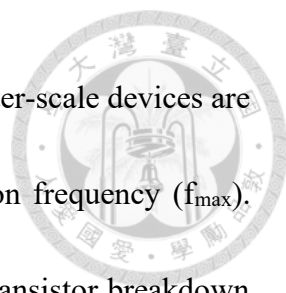
Chapter 4 Millimeter-wave Wideband CMOS Power Amplifier Using Inductive-Compensation Distributed Active Transformer



4.1 Introduction

Broadband and multiband 5G millimeter-wave (mm-wave) systems operating in the Frequency Range 2 (FR2) band, spanning 24.25 to 71 GHz (n257-n263), are expected to deliver multi-gigabit-per-second (mGb/s) data rates. Various countries have adopted different FR2 bands to establish their 5G wireless networks [1]. In the United States, the Federal Communications Commission (FCC) has included 37.6-38.6 GHz and 47.2-48.2 GHz in its spectrum allocation, while Japan is developing technical rules for licensed spectrum in the 37-43.5 GHz range. Moreover, the FCC released regulations for short-range detection in the industrial, scientific medical (ISM) band (57-71 GHz) in July 2023 [44]. The 60 GHz band is further divided into 57-64 GHz and 64-71 GHz segments, supporting WiGig Channels 1-3. These frequency bands align with the European Telecommunications Standards Institute's (ETSI) EN305 and EN550 standards, enhancing cross-network compatibility. Deploying such systems is expected to support economic 5G international and cross-network roaming and a wide range of application scenarios.

The PA plays a crucial role in the transmitter front end by determining the overall



radio frequency output power. In the design of 60 GHz PAs, nanometer-scale devices are typically employed to achieve higher gain and maximum oscillation frequency ($f_{\max}$). However, shrinking the gate length of these devices decreases the transistor breakdown voltage, thereby limiting the supply voltage (V_{DD}) [45]-[56]. Power combining techniques overcome this limitation and achieve higher output power with a low V_{DD} . One straightforward approach is binary direct connecting, which uses equal-phase combination through transmission lines (TLs) that serve both power combining and impedance matching. However, using TLs in high combining numbers occupies a large chip area.

Alternatively, Wilkinson power combiners use quarter-wavelength TLs and resistors to achieve good input/output return loss and isolation, but they require additional matching networks, adding complexity and chip area. Transformer-based power combining has become popular in recent mm-wave designs, particularly for V-band CMOS PAs. Transformers facilitate impedance transformation to the optimum level and provide compactness and low insertion loss for high-output-power PAs with low optimum impedance. Transformers can also supply DC power through a center tap, simplifying the power delivery without needing extra matching circuits. However, transformers can increase routing complexity in the DC bias path compared to other methods.

Stacking architectures provide another approach to increasing output power by



allowing multiple transistors to share the voltage stress, reducing the need for complex matching networks [50], [53], [54]. Despite their benefits, stacking introduces significant parasitic effects, such as increased capacitance and inductance, which limit bandwidth and complicate achieving wideband performance. Moreover, stacking requires a higher supply voltage, often incompatible with the rest of the system, leading to power supply design, system integration, and thermal management challenges.

This work proposes a V-band three-stage PA using a voltage power combiner. The design integrates a series power combiner structure with enhanced power combining efficiency. By incorporating a compensation network, we mitigate parasitic effects and achieve a substantial impedance transformation ratio, allowing efficient transfer of high load resistance (R_L) to low optimal resistance (R_{opt}) at high frequencies. The proposed PA demonstrates a saturated output power (P_{sat}) of 20.6 dBm and a peak power-added efficiency (PAE) of 16.7% at 60 GHz, providing superior wideband performance compared to other voltage-combined V-band PAs.

4.2 Transformer-Base Power Combining Structure

The transformer-based power combiner can generally be categorized into parallel (current) combining and series (voltage) combining, distinguished by the output combining method. This section will cover the impedance turn ratio, the parasitic effects

of the combining ratios, and the structural modifications involved.

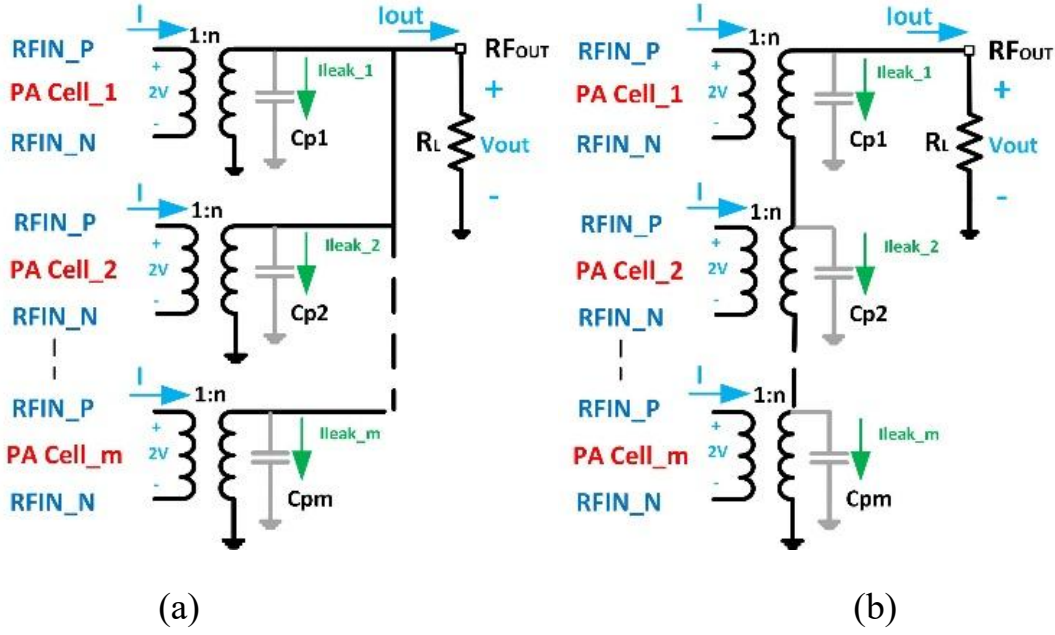


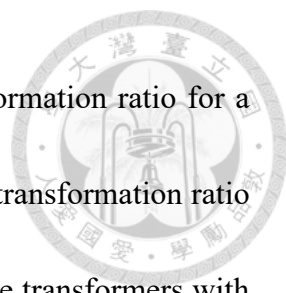
Fig. 4.1 Schematics of transformer-based (a) parallel, and (b) series power combining networks with parasitic capacitors C_p .

4.2.1 Transformer-Base Parallel/Series Combining Architecture

The parallel combining architecture, responsible for merging currents, is illustrated in Fig. 4.1(a) [49-50][53][55]. An ideal m -way differential parallel-type combiner facilitates the transfer of optimal load resistance from the load to the output. This can be expressed as [49]

$$R_{opt} = \frac{V}{I} = \frac{V_{out}/2n}{nI_{out}/m} = \frac{m}{2n^2} R_L, \quad (4.1)$$

where n represents the ratio of the primary inductor L_p to the secondary inductor L_s , m is the combining cell count, and R_{opt} represents the effective single-ended resistance



observed at each input port of the combiner. The impedance transformation ratio for a parallel-type combiner is $2n^2/m$. In cases where a high impedance transformation ratio is required for the PA design, it becomes necessary to utilize multiple transformers with $n > 1$ in the TF-based parallel-type combiner.

Alternatively, the series combining architecture, which merges voltages, is depicted in Fig. 4-1(b) [56]. An ideal m -way differential series-type combiner transfers the optimum load resistance from the load to the output according to the following relationship:

$$R_{opt} = \frac{V}{I} = \frac{V_{out}/2nm}{nI_{out}} = \frac{1}{2mn^2} R_L. \quad (4.2)$$

Therefore, the required R_{opt} can be adjusted by the parameter m of the transformer to ensure R_L is matched. As Equation suggests, an m -way series combiner achieves an impedance transformation ratio of $2mn^2$. This allows the series combiner to perform substantial impedance transformation, effectively reducing a high R_L to a low R_{opt} . However, in single-ended output configurations, parasitic effects, including variable leaking currents, can exacerbate imbalances at higher frequencies. To mitigate these issues, this article proposes a compensated approach that addresses the unbalanced outcomes caused by parasitic effects. This enhancement ultimately enables a high-efficiency power combiner design with a high impedance transformation ratio.

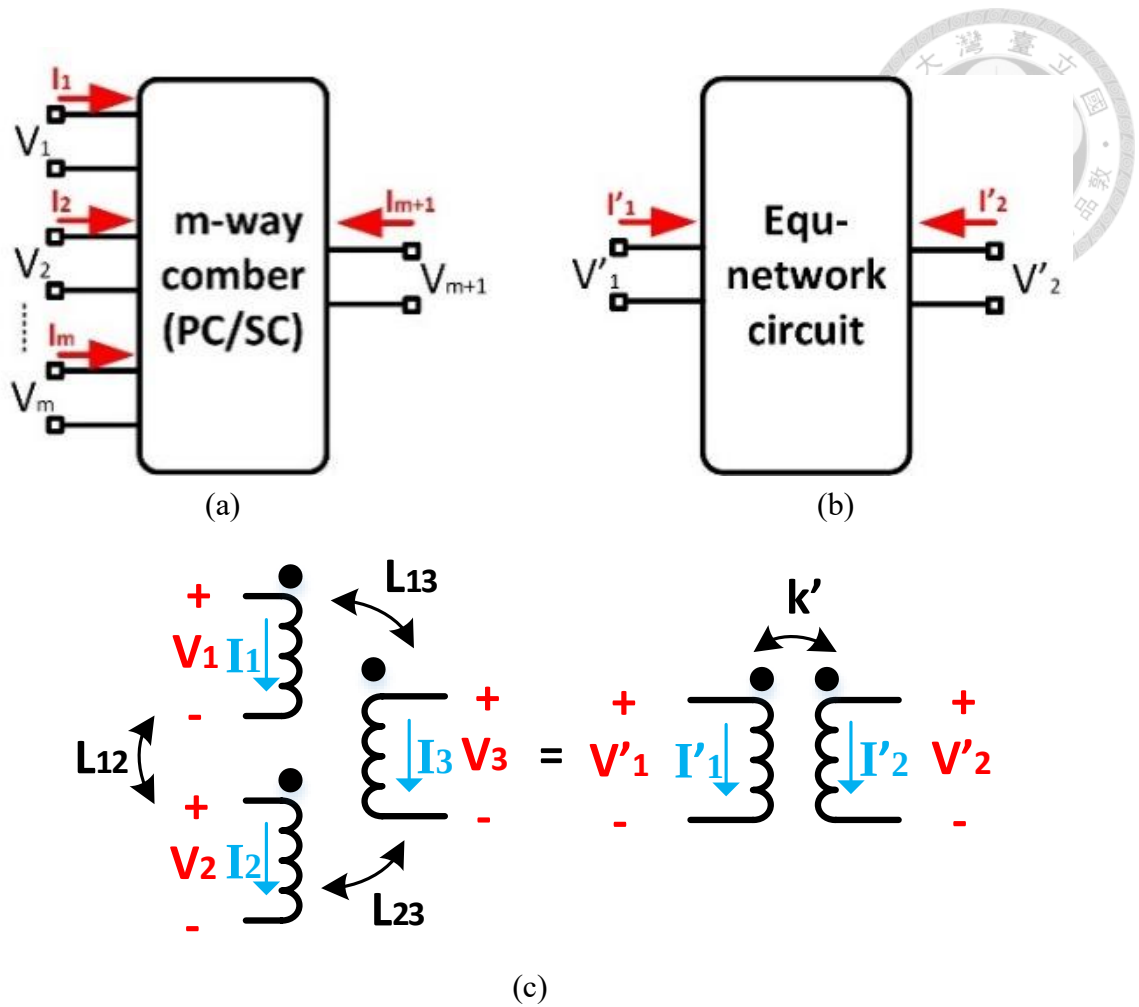


Fig. 4.2 (a) m-way power combiner, (b) equivalent network of m-way power combiner when $V_1=V_2=\dots=V_m$, and (c) 2-way series power combiner and its equivalent circuit.

4.2.2 Transformer-Base Parallel/Series Combining Architecture

Before addressing parasitic effects, a multi-channel power combiner can be represented as shown in Fig. 4.2(a), consisting of m input ports and one output port, forming an m-way network. The current matrix can be represented by a Y-parameter matrix along with a voltage matrix, as shown in [57]

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{m+1} \end{bmatrix} = \begin{bmatrix} y_{11} & \cdots & y_{1,m+1} \\ y_{21} & \cdots & y_{2,m+1} \\ \vdots & \vdots & \vdots \\ y_{m+1,1} & \cdots & y_{m+1,m+1} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_{m+1} \end{bmatrix}. \quad (4.3)$$



If all input port voltages of the m-way combiner are equal ($V_1 = \dots = V_m = V$), the Eq.

(4.3) can be simplified as

$$\begin{bmatrix} I'_1 \\ I'_2 \end{bmatrix} = \begin{bmatrix} y'_{11} & y'_{12} \\ y'_{21} & y'_{22} \end{bmatrix} \begin{bmatrix} V'_1 \\ V'_2 \end{bmatrix}, \quad (4.4)$$

where I'_1 is the sum of I_i ($i = 1, \dots, m$), $I'_2 = I_{m+1}$, $V'_1 = V$, and $V'_2 = V_{m+1}$. The

equivalent circuit calculated by Eq. (4.4) is shown in Fig. 4.2(b). If this simplified formula

is equivalent to a two-way TF-based combiner, it can be modified to represent the

inductance matrix of the transformer network, as shown in Fig. 4-2(c), assuming $V_2 = V_3$

and $I_2 = I_3$, as [58]

$$\begin{bmatrix} V'_1 \\ V'_2 \end{bmatrix} = \begin{bmatrix} L'_1 & L'_M \\ L'_M & L'_2 \end{bmatrix} \begin{bmatrix} I'_1 \\ I'_2 \end{bmatrix}, \quad (4.5)$$

where $I'_1 = 2I_1$, $I'_2 = I_3$, $L'_1 = (L_{11} + L_{21})/2$, $L'_2 = L_{33}$, and $L'_M = L_{13}$. The coupling

factor and quality factor of a single inductor on the primary winding can then be defined

as

$$k' = \frac{L'_M}{\sqrt{L'_1 \times L'_2}}, \quad (4.6)$$

and

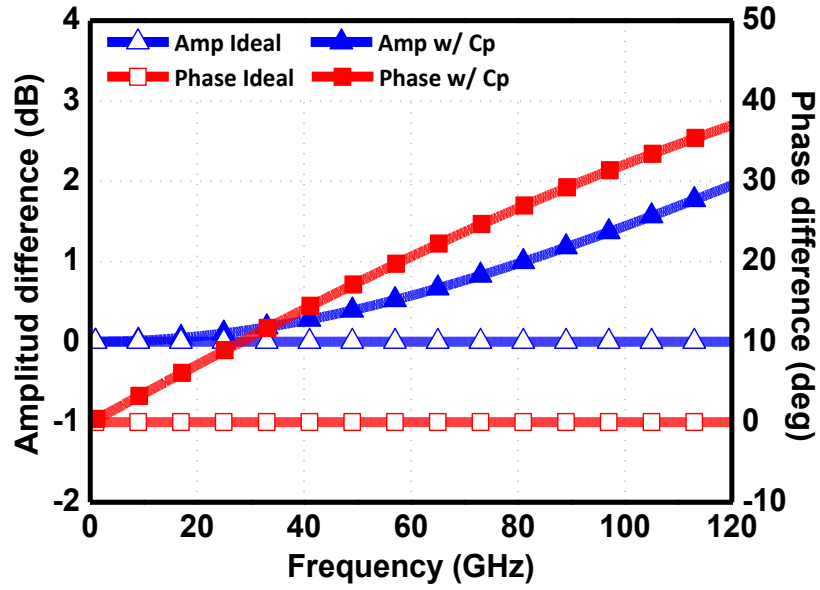
$$Q'_1 = \frac{\omega L'_1}{r'_1} > Q_1 = \frac{\omega L_{11}}{r_1}, \quad (4.7)$$

where r'_1 represents half of the secondary inductor's resistance. Since the coupling

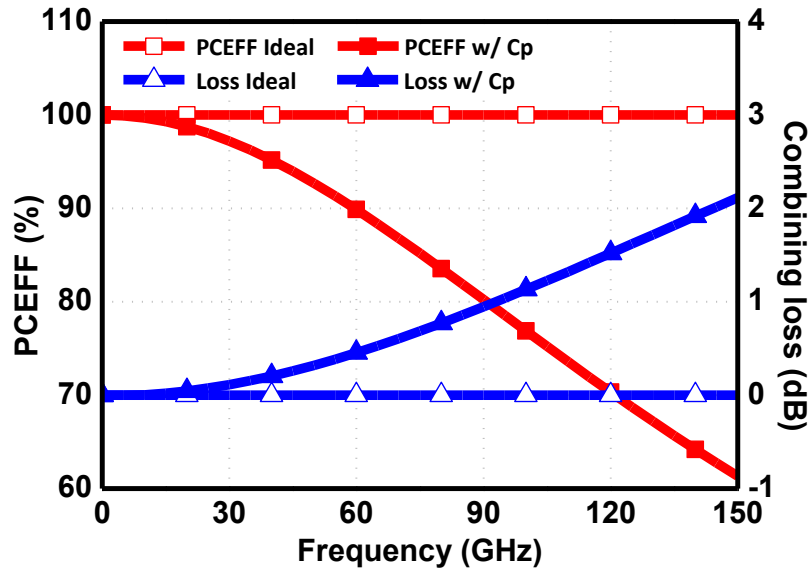
factor and quality factor have been established, the passive efficiency η of the transformer

combiner can be defined as shown in [59]

$$\eta = \frac{1}{1 + \frac{2}{Q_1 Q'_2 k'^2} + 2 \sqrt{\left(1 + \frac{1}{Q_1 Q'_2 k'^2}\right) \times \frac{1}{Q_1 Q'_2 k'^2}}} \quad (4.8)$$



(a)



(b)

Fig. 4.3 Simulated (a) amplitude and phase difference, (b) PCEFF and combining loss of the series power combining architecture with 20-fF C_p as shown in Fig. 4.1(b).



The passive combining efficiency η of the power combiner is determined solely by the transformer's coupling and quality factors. Here, we define the power-combining efficiency (PCEFF) of an m -way combiner as

$$PCEFF (\%) = \frac{P_{out,Load}}{m \times P_{in,cell}} \times 100\% . \quad (4.9)$$

As discussed in [49], parasitic effects generally do not affect the parallel combining architecture since the leakage currents do not produce phase and amplitude imbalances during combination, which makes it widely used up to the V-band frequencies. However, parasitic capacitance can lead to leakage current asymmetry in the series combining architecture, resulting in inconsistencies in phase and amplitude along the combination path, especially at higher frequencies, which negatively impacts the combining efficiency.

Fig. 4.3 illustrates the series-combining architecture from Fig. 4.1(b), assuming $n=1$, $m=2$, and 20 fF of parasitic capacitance C_p , while disregarding the self-resonant frequency. It demonstrates how parasitic effects impact the phase and amplitude differences, power loss, and combining efficiency. For a two-way series power-combining architecture with parasitic capacitance considerations, the passive efficiency η_c of the transformer combiner can be rewritten as

$$\eta_c = \eta \times \left(\frac{1}{2} + \frac{|X_{cap}|}{R_{Load} + 2 * |X_{cap}|} \right), \quad (4.10)$$

where $X_{cap}=1/\omega C_p$ represents the reactance of the parasitic capacitance. This equation highlights that the combining efficiency deteriorates significantly at higher frequencies,

consistent with the degradation in PCEFF at higher frequencies depicted in Fig. 4.3.



4.2.3 Proposed Novel DAT Series Combining Architecture

Given the preceding analysis, it is evident that the parallel architecture yields favorable results. However, challenges arise when a high-output power PA operates at 60 GHz or beyond, where the reduction in R_{opt} increases the transformer's turn ratio n , thus escalating the parasitic capacitance between the primary and secondary inductors. This increase can align the self-resonant frequency with the operational frequency, adding complexity to the design.

We propose a modified DAT architecture for series power combiners to address these parasitic effects. This novel design mitigates parasitic effects and is optimized for compact areas, making it suitable for high-frequency, high-output power PA applications. By incorporating parasitic effect compensation, the DAT architecture is well-suited to high-frequency matching designs, enhancing overall efficiency. Fig. 4.4 illustrates the equivalent circuit of a traditional DAT architecture with primary and secondary parasitic capacitors, C_m , representing the coupling capacitance between these sides, primarily responsible for imbalance [67],[71].

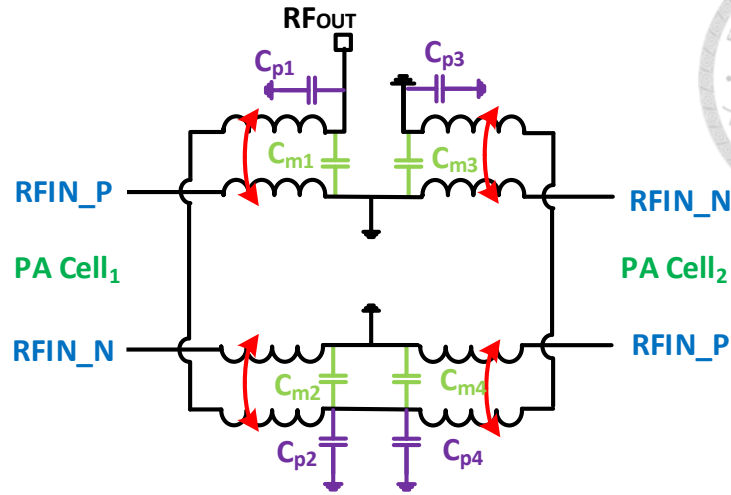


Fig. 4.4 Equivalent circuit of the traditional DAT with main parasitic effects

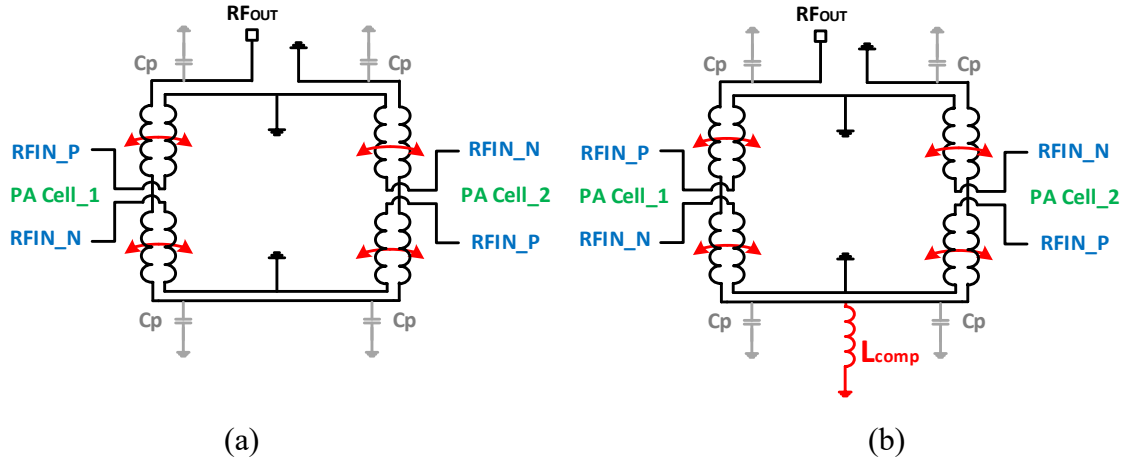


Fig. 4.5 (a) Traditional and (b) proposed DAT architectures and equivalent parasitic capacitors.

As shown in Fig. 4.5(a), the quiescent current demand on the primary and secondary sides under high secondary-side current conditions requires a thicker metal layer, leading to elevated parasitic capacitance on the secondary side. In this configuration, capacitors C_{p2} and C_{p4} contribute most significantly to the imbalance of the secondary side, connected to AC ground as shown. This design, illustrated in Fig. 4.5(b), is enhanced with a compensation inductor to absorb parasitic capacitance, resulting in improved



performance, as demonstrated by the equivalent model in Fig. 4.6.

The proposed compensation inductance L_{comp} for optimal performance is calculated as

$$L_{comp} (H) = \frac{1}{\omega^2 \times 2 \times C_p}, \quad (4.11)$$

where ω is the operating frequency. The transformer's passive efficiency can be redefined

with η_{comp} as

$$\eta_{comp} = \eta \times \left(\frac{1}{2} + \frac{|X_p|}{R_{Load} + 2 * |X_p|} \right), \quad (4.12)$$

where

$$|X_p| = \frac{|X_{Lcomp}|}{1 - 2 \left(\frac{|X_{Lcomp}|}{|X_C|} \right)}. \quad (4.13)$$

Here, X_p is the parallel reactance of the parasitic and compensated inductors, and

$$X_{Lcomp} = \omega L_{comp}.$$

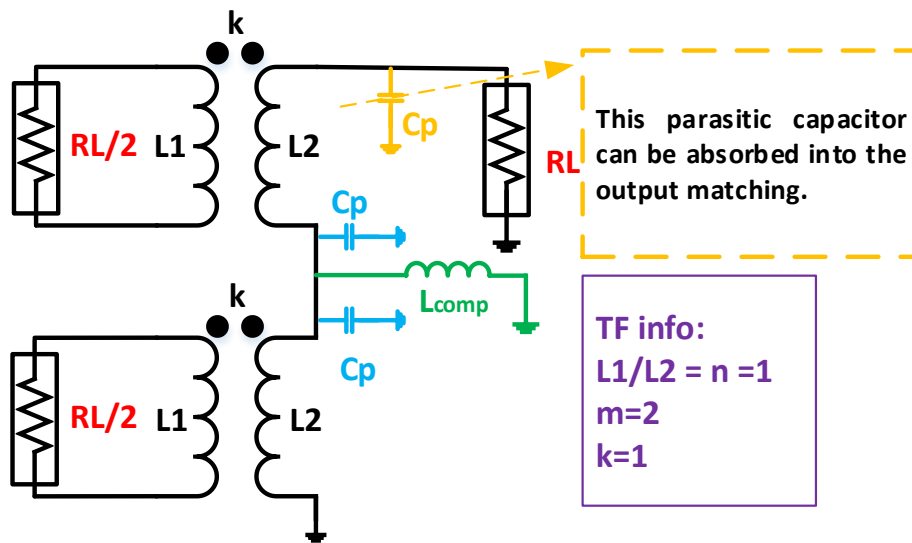
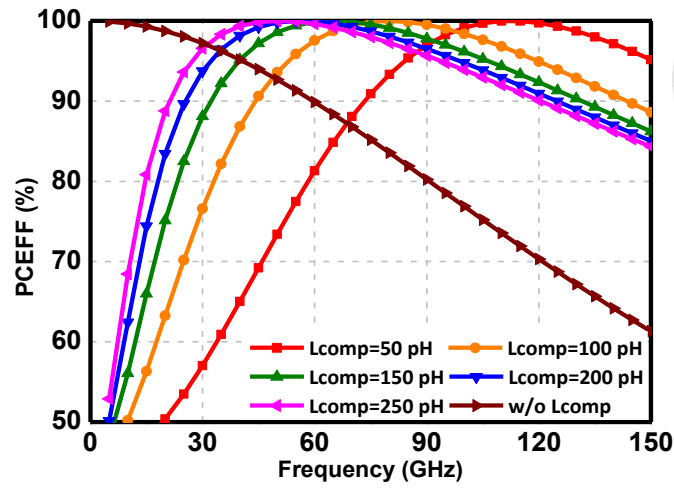
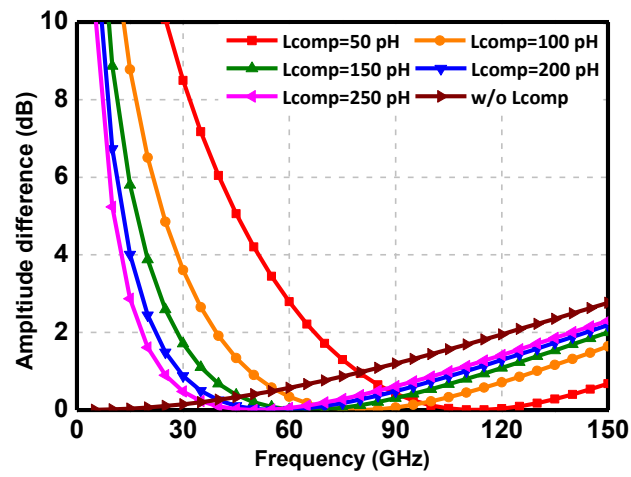


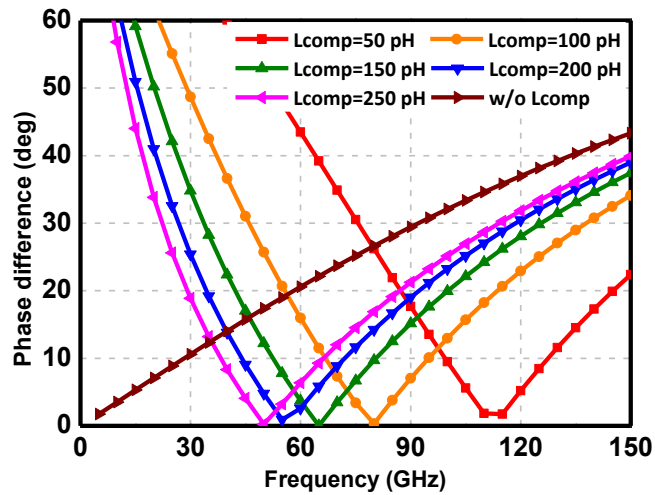
Fig. 4.6 Proposed inductive-compensation simulated equivalent schematic.



(a)



(b)



(c)

Fig. 4.7 Proposed compensated inductor value from 50 – 250 pH (a) PCEFF, (b) amplitude difference, and (c) phase difference.

By selecting $1/(2\omega^2 C_p)$, X_p approaches infinity at ω , resulting in a nearly ideal $\eta \approx \eta_{comp}$. The calculated efficiency demonstrates that the compensated inductor resonates with the parasitic capacitor, achieving passive efficiency close to 100 % at 55 GHz with a 200 pH inductor, as shown in Fig. 4.7(a). This high efficiency confirms the design's robustness against parasitic capacitance, which creates a high impedance at the parasitic capacitor's operating frequency.

The proposed technique is validated in Fig. 4.7(b) and 4.7(c), highlighting the amplitude and phase symmetry improvements in two-way combinations. Fig. 4.8 further illustrates the Q-factor of the compensated inductor, demonstrating that efficiencies stabilize when Q_{comp} exceeds 10. Therefore, the conventional transformer-based series combining architectures also benefit from this compensation method.

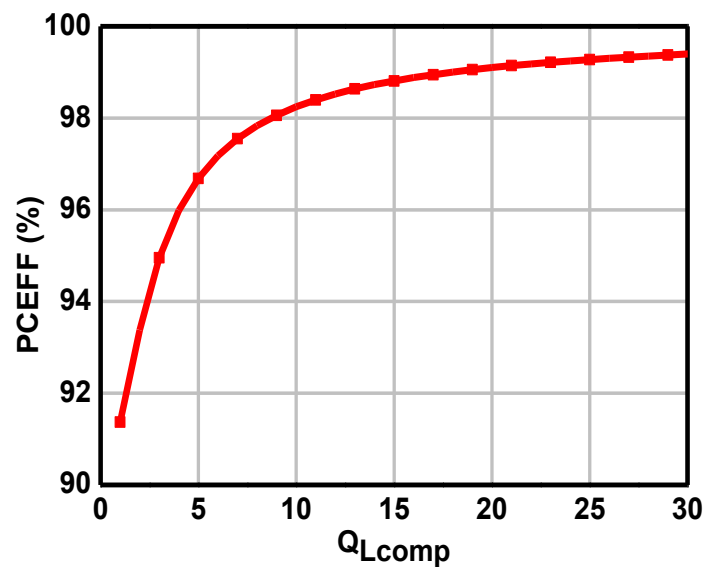
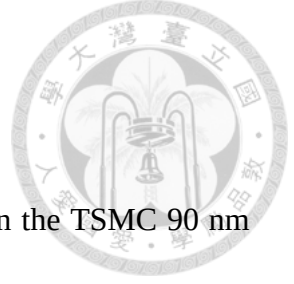


Fig. 4.8 Proposed compensated inductor Q-factor effect.



4.3 Circuit Design

The proposed PA is specifically designed for implementation in the TSMC 90 nm CMOS GUTM process, which includes the use of 6 metal layers (6M_x), 1 metal layer (1M_z), and 1 ultra-thick metal layer (1UTM), though the AP layer is not available in this process. This V-band PA operates with a supply voltage of 1.2 V to optimize the P_{SAT} and PAE, enhancing performance in high-frequency applications. The circuit architecture of the proposed PA is depicted in Fig. 4.9 and consists of a multi-stage design. It includes two differential power cells, two differential driver cells, and two differential buffer cells. This design follows a two-way DAT approach with voltage-based power combining, crucial for efficient power delivery at millimeter-wave frequencies.

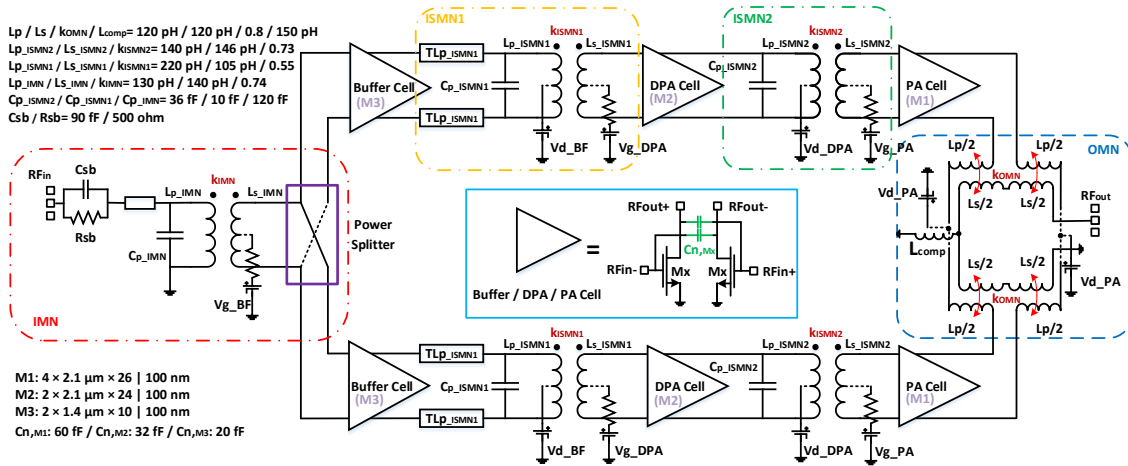


Fig. 4.9 Proposed PA schematic.



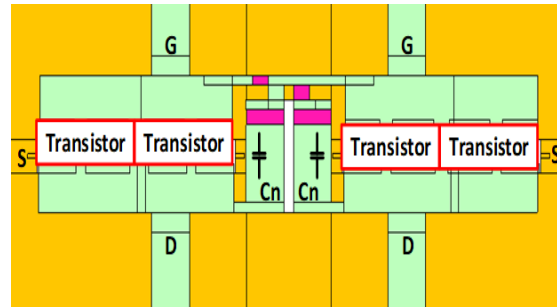
The input splitter employs a two-way current splitting architecture to manage signal distribution, ensuring the input power is evenly distributed across the amplifier stages. Each stage—the power, driver, and buffer cells—adopts a pseudo-differential common-source topology, which effectively combines the benefits of differential signaling with simplified circuitry. This topology is further enhanced by incorporating a neutralization technique, as referenced in [67], which aims to mitigate parasitic capacitances and improve the stability and gain of the amplifier. The two-way DAT used in the PA design serves as a power-combining network, efficiently combining the output power from multiple amplifier stages into a single-ended output. This approach is advantageous in V-band PAs because it supports higher output power, improves impedance matching, and reduces the effects of parasitic elements.

The combination of two-way DAT and pseudo-differential architecture enables the proposed PA to achieve high performance at V-band frequencies, making it suitable for applications requiring compact, high-efficiency CMOS solutions at millimeter-wave frequencies.

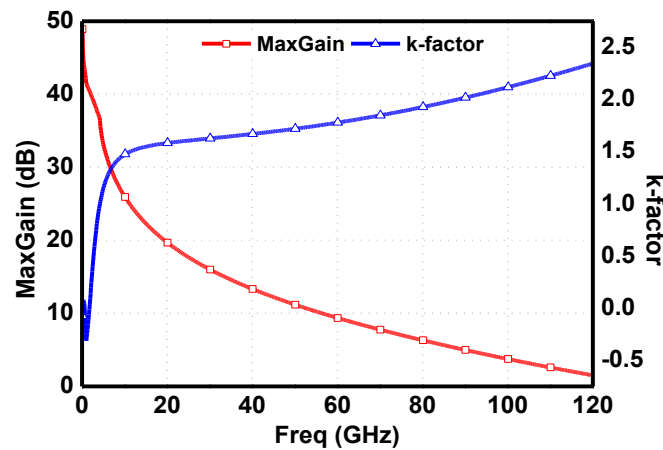
4.3.1 Power Stage and Output Power Combiner Design

The proposed V-band PA aims for a broad saturated output power of approximately

20 dBm. A two-way power combining approach is utilized to achieve this after compensating for the combiner's inherent power loss. This design yields a power cell maximum output of approximately 21.5 dBm, factoring in combiner losses.



(a)



(b)

Fig. 4.10 Proposed PA power-stage (a) combined line layout with the neutralization capacitors, and (b) maximum and stability k-factor.

To boost gain in the V-band, the PA adopts a Class-A bias with a 1.2-V supply voltage and a gate bias $V_{GS} = 0.8$ V. This biasing minimizes non-linearities, addressing issues associated with second-and third-order transconductance (g_{m2} and g_{m3}) distortions. A transistor with a total gate width of 218 μm provides sufficient current for this design,

with the $f_t / f_{\max}$ of 150 GHz / 145 GHz and a transconductance efficiency of 1.062 S/mm, balancing between gain maximization and current density reliability.

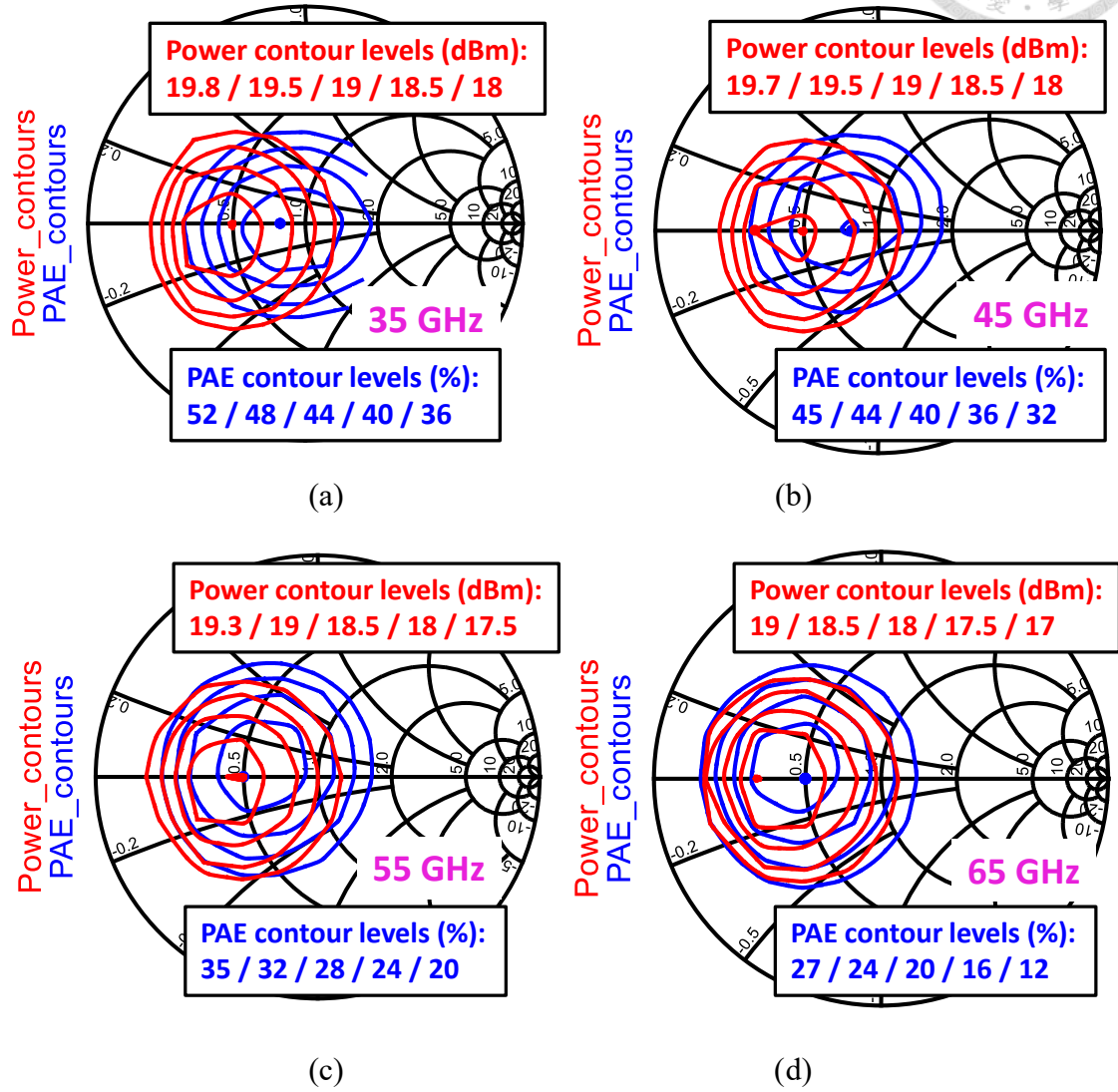


Fig. 4.11 Proposed PA's power contours and PAE contours at 35/45/55/65 GHz after extracted C_{DEV} .

To enhance gain, parallel combining mitigates the transistor's input capacitance (C_{gs}), and each differential cell is structured to dimensions of $4 \times 2.1 \mu\text{m} \times 26$ fingers. The chosen transistor size ensures maximum gain and current density reliability. A

neutralization capacitor, C_n , of 60 fF, is included to optimize maximum stable gain (MSG) and maximum available gain (MAG), achieving a stability factor $K > 1$ across the operational bandwidth, as depicted in Fig. 4.10(b).

The next step involves determining the optimal load R_{opt} for power delivery, estimated using load-line theory and validated through load-pull simulations. After identifying the parasitic capacitance (C_{DEV}) of 245 fF in the one-way differential power cell EM layout shown in Fig. 4.10(a), an optimized load impedance (Z_{opt}) of 25 Ω is derived to achieve maximum PAE. The extracted C_{DEV} capacitance supports the wideband matching requirements of the transformer-based network, and the power and PAE contours result at 35/45/55/65 GHz are shown in Fig. 4.11(a)-(d).

The output matching network (OMN), illustrated in Fig. 4.12(a), employs a two-way series power combining architecture. This design features an innovative compensation inductor (L_{comp}), tailored to resonate with C_p for broadband performance. The multi-channel combination formula outlined in Section 4.2.1 helps simplify the two ways of power combining output structure, as depicted in Fig. 4.12(b). Transformer characteristics, with $L_p = L_s = 120$ pH and a coupling coefficient $k = 0.8$, are optimized to maintain low insertion losses across a wide bandwidth.

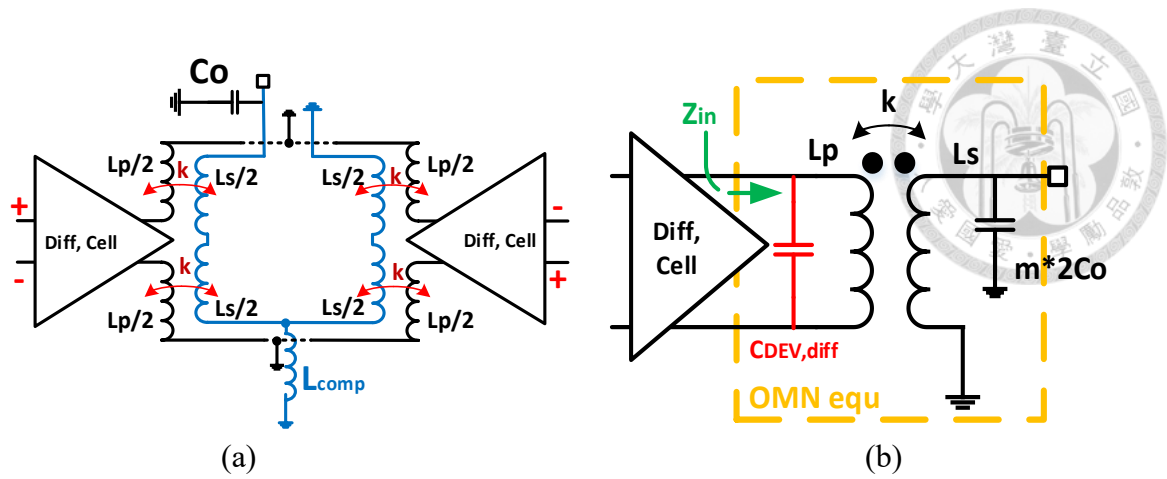


Fig. 4.12 Proposed PA output matching network (OMN) (a) schematic, and (b) the equivalent matching network ($m=2$).

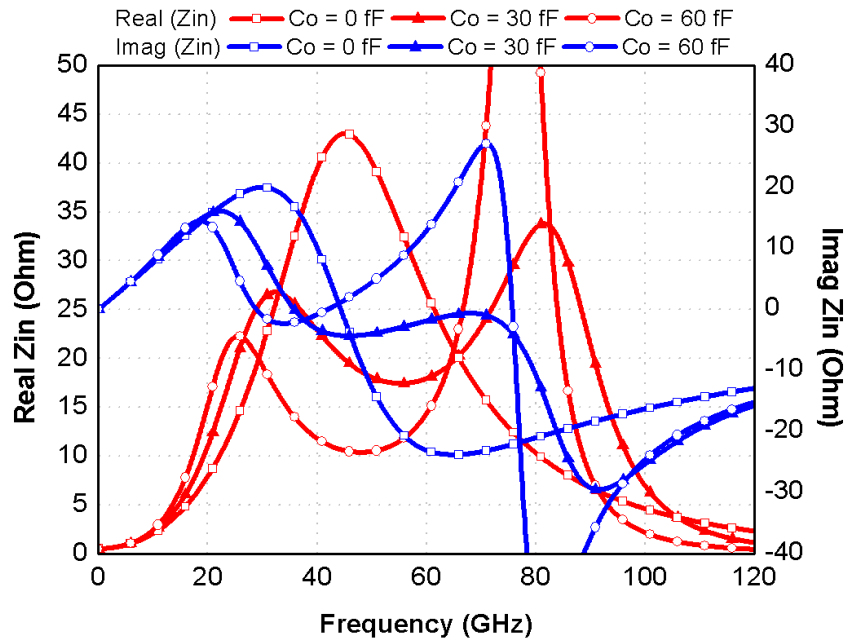


Fig. 4.13 OMN shown in Fig. 4-12(b) bandwidth analysis of Z_{in} with different C_o .

The impedance transformation using the OMN circuit, shown in Fig. 4.13 for impedance Z_{in} , demonstrates effective broadband response with flattened real and imaginary components. The impedance analysis incorporates the resonate capacitor C_o , with values varying from 0 to 60 fF, to optimize the impedance bandwidth. The resulting wideband matching characteristics of the OMN circuit are derived using the following



formulas, based on the Y-matrix as

$$Z_{in} = \frac{Y_{22}Z_L + 1}{(Y_{11}Y_{22} - Y_{12}Y_{21})Z_L + Y_{11}}, \quad (4.14)$$

where

$$Y_{11} = j\omega C_{DEV} + \left[\frac{1}{j\omega L_m(1 - k^2)} \right], \quad (4.15)$$

$$Y_{21} = Y_{12} = \frac{1}{\left[j\omega L_m \left(1 - \frac{1}{k^2} \right) \right]}, \quad (4.16)$$

$$Y_{22} = j\omega 2mC_o + \left[\frac{1}{j\omega L_s(1 - k^2)} \right], \quad (4.17)$$

$$Lm = k\sqrt{L_P L_S}. \quad (4.18)$$

The resonant frequencies for the network, evaluated based on the Y matrix, are given by

$$\omega_{p1} = \sqrt{\frac{\varphi_B - \varphi_C}{\varphi_A}}, \quad (4.19)$$

$$\omega_{p2} = \sqrt{\frac{\varphi_B + \varphi_C}{\varphi_A}}, \quad (4.20)$$

where

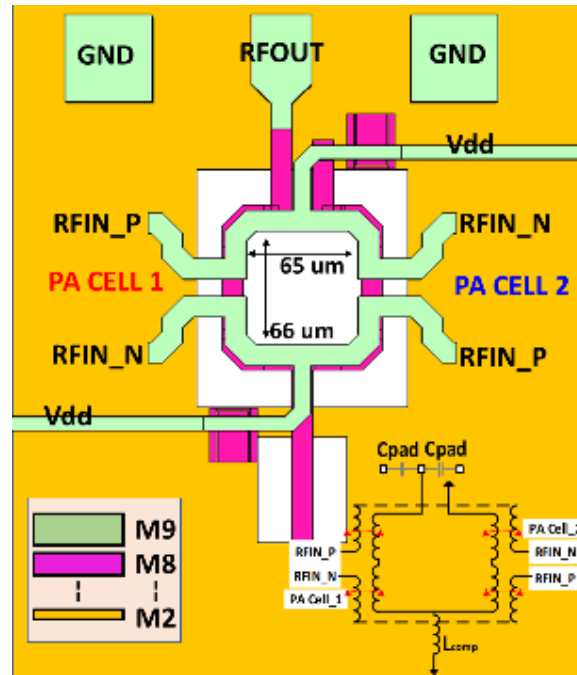
$$\varphi_A = 8C_{DEV}C_o(L_P L_S - L_m^2), \quad (4.21)$$

$$\varphi_B = L_P C_{DEV} + 4L_S C_o, \quad (4.22)$$

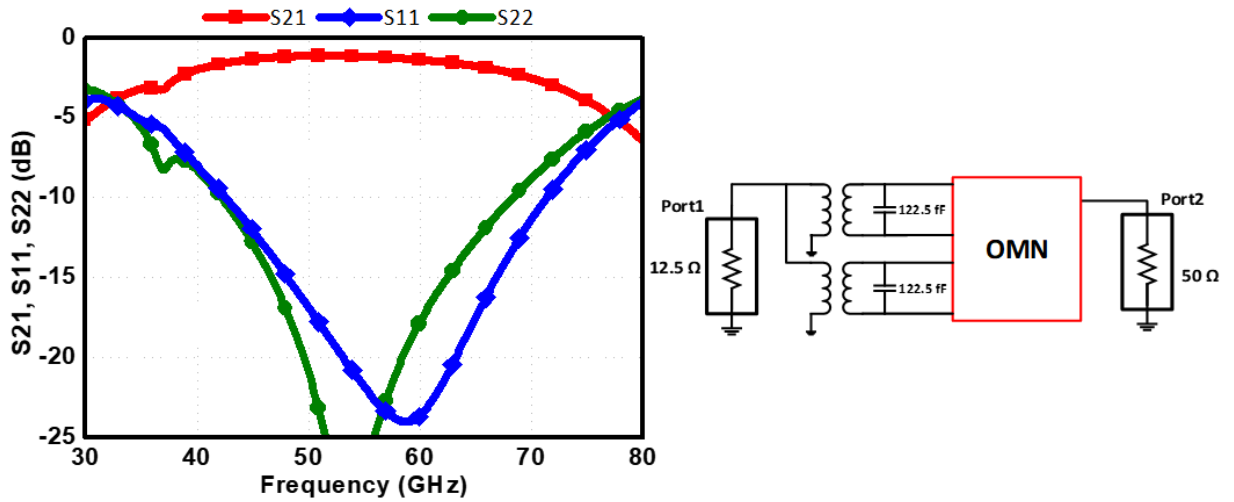
$$\varphi_C = \sqrt{\varphi_B^2 - 2\varphi_A}. \quad (4.23)$$

For the broadband matching requirements, C_o is selected as 30 fF, as shown in Fig. 4.13, which provides an impedance response optimized for a wide bandwidth. Since the

parasitic capacitance C_{pad} of the RF PAD is approximately 30 fF, and it is the same as the requirement of C_o , this effect is absorbed into the designed wideband matching.



(a)



(b)

Fig. 4.14 Proposed PA's power combining OMN (a) EM layout, (b) S-parameters results with EM.

The EM layout simulation of the OMN shown in Fig. 4.14(a) confirms that insertion loss is under 3 dB from 35 to 70 GHz, with a minimum loss of 1.23 dB at 57 GHz, achieving return losses below 10 dB from 43 to 67 GHz, indicating effective broadband matching and power combining, as shown in Fig. 4.14(b).

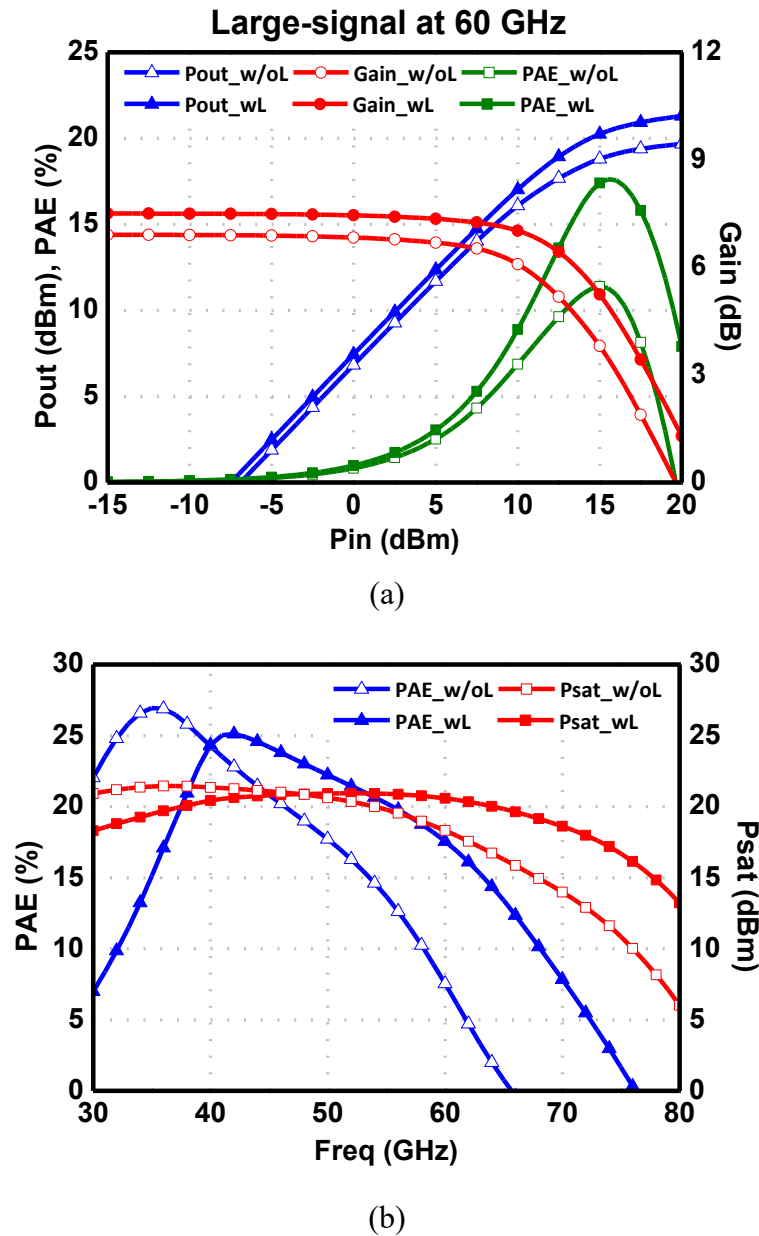


Fig. 4.15 Comparison of the large-signal performance between traditional DAT and proposed DAT, (a) at 60 GHz, (b) PAE and P_{sat} at 30-80 GHz.

Finally, Fig. 4.15(a) presents large-signal characteristics at 60 GHz, where the proposed architecture demonstrates an improvement in PAE by 9% and a P_{sat} increase of 1.4 dB over traditional designs. Fig. 4.15(b) illustrates how the architecture with L_{comp} compensation enhances high-frequency performance, maintaining bandwidth and efficiency, thus confirming the design's suitability for wideband applications.

4.3.2 Driver Stage and ISMN2

To ensure the proposed PA maintains its P_{sat} , each unit in the differential driver stage is designed to achieve a one-way output power at 1 dB compression point ($OP_{1\text{dB}}$) of at least 15 dBm. The driver stage operates in Class-A mode, matching the configuration and bias voltage of the output stage to maintain linearity. Due to the insertion loss in the second inter-stage matching network (ISMN2), depicted in Fig. 4.16(a), the driver stage dimensions are scaled to $2 \times 2.1 \mu\text{m} \times 24$, which is approximately 2.16 times the size of the power stage unit. A neutralization capacitor of 32 fF improves gain and stability in the driver stage, achieving a final $OP_{1\text{dB}}$ of 16.5 dBm in a one-way configuration. Following load-pull simulations, an optimized load impedance Z_{opt} of 60 GHz is derived, achieving a differential impedance of $30 + j27 \Omega$ for optimal matching. Among them, $L_{\text{p_ISMN2}}$ is 140



pH, L_{s_ISMN2} is 146 pH, the coupling factor is 0.73 and matched with 36 fF C_{p_ISMN2} for driver-stage to power-stage power matching.

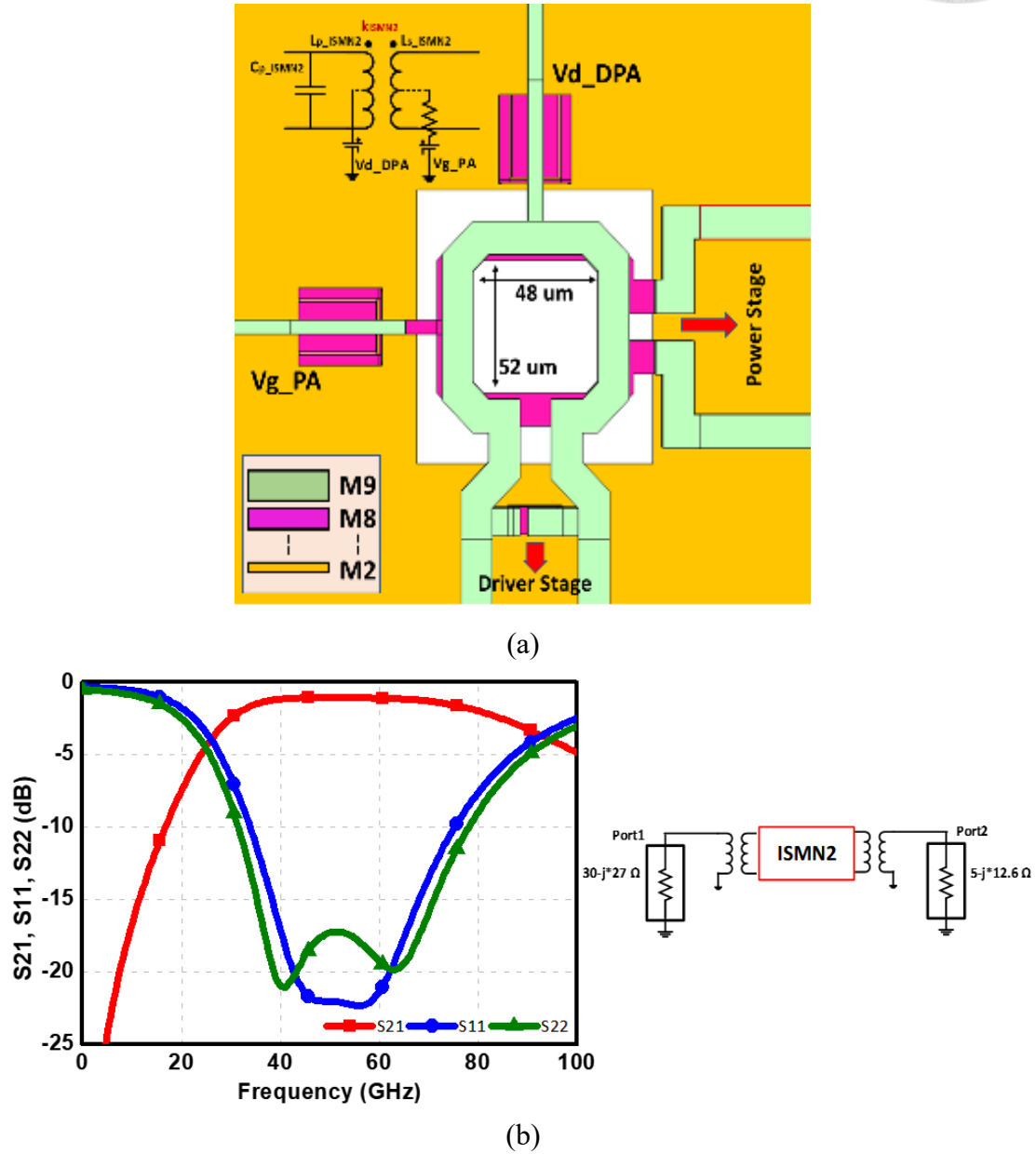


Fig. 4.16 (a) EM layout, and (b) EM simulated S-parameters of the ISMN2.

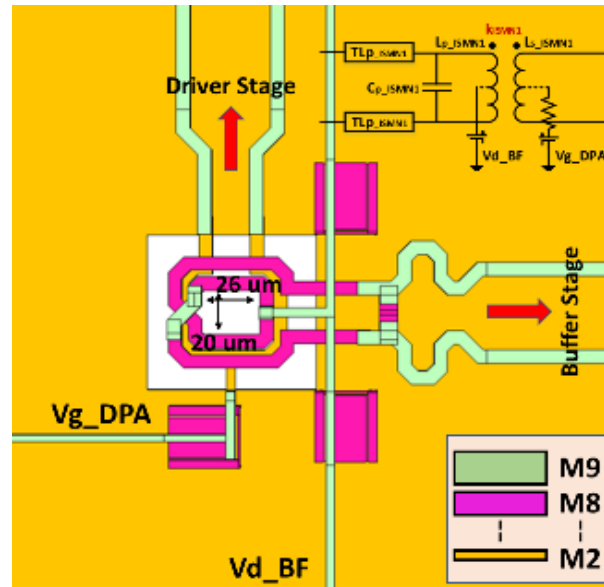
Fig. 4.16(b) shows the EM-simulated S-parameters for ISMN2, confirming that the matching loss remains under 1.2 dB across the desired frequency range, highlighting ISMN2's ability to provide effective inter-stage matching and sufficient driving capability to the output stage.

4.3.3 Buffer Stage and ISMN1

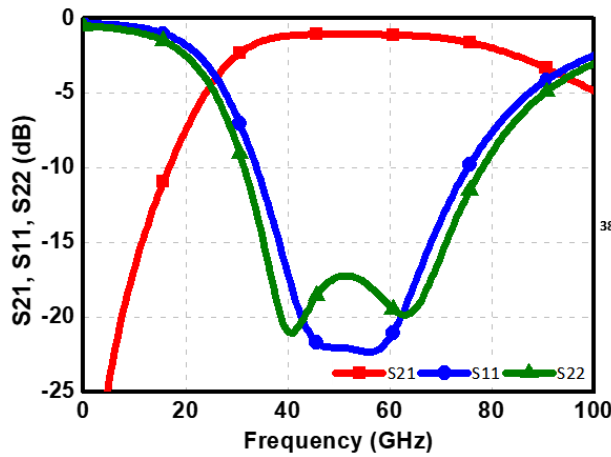
An additional buffer stage amplifier is integrated to enhance the overall gain to 20 dB at the target frequency range. This buffer employs a differential common-source topology and operates in Class-A mode with a gate voltage $V_{GS} = 0.8$ V and a supply of 1.2 V. As shown in Fig. 4.17(a), the transistor configuration uses $2 \times 1.4 \mu\text{m} \times 10$ for optimized performance. A neutralization capacitor C_n of 20 fF further enhances stability and gain. The impedance matching network, ISMN1, where adjustments are made using $80 \mu\text{m}$ 57Ω transmission lines (TLP_ISMN1) and a capacitor C_{p_ISMN1} of 10 fF to satisfy the target impedance transformation for optimal frequency response. Additionally, the inductor values $L_{p_ISMN1} = 220$ pH, and $L_{s_ISMN1} = 105$ pH with a coupling factor 0.52 are chosen to match the driver stage impedance. Fig. 4.17(b) presents the S-parameters of ISMN1, illustrating that the matching loss remains below 2 dB within the operational



frequency range, verifying the buffer stage's ability to maintain sufficient gain transfer to the output stage.



(a)



(b)

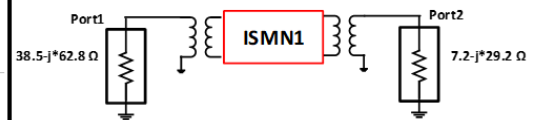
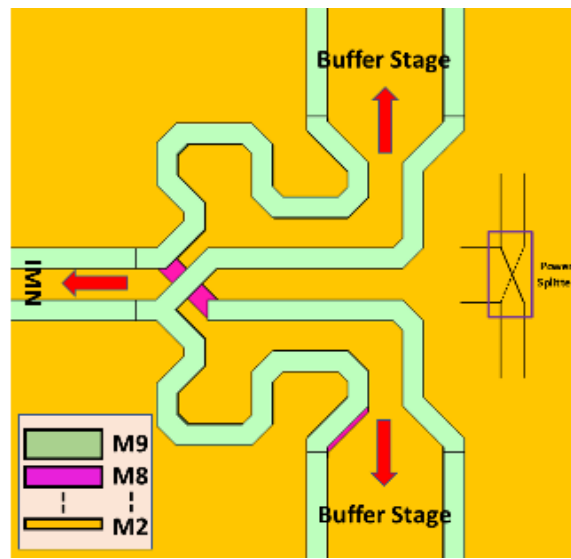
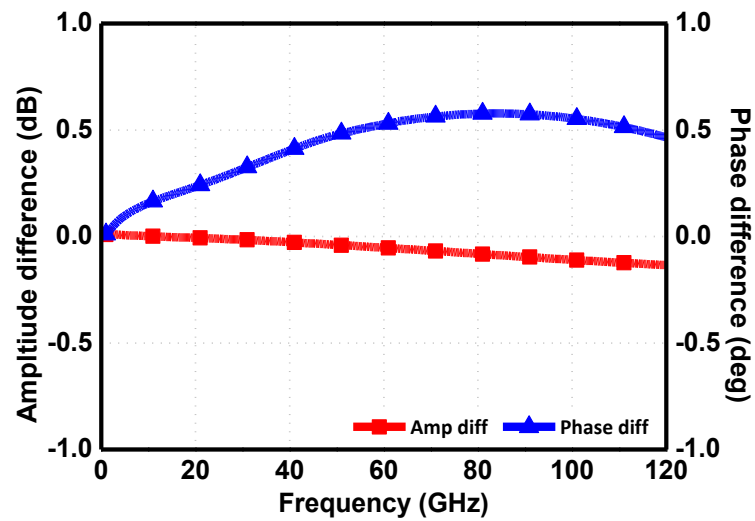


Fig. 4.17 (a) EM layout and (b) EM simulated S-parameters of the ISMN1.



(a)

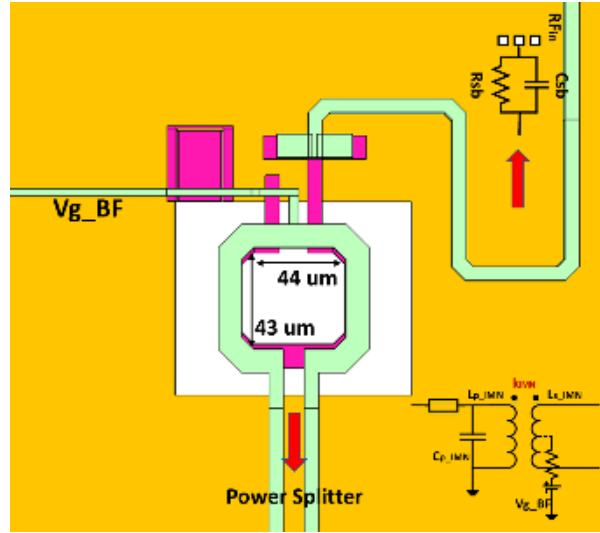


(b)

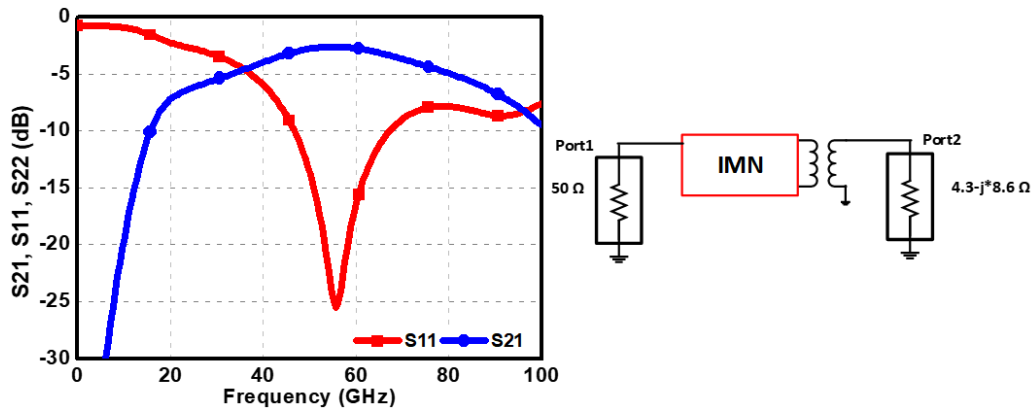
Fig. 4.18 (a) EM layout and (b) EM simulated amplitude and phase differences of the power splitter.

4.3.4 IMN

For the input matching network (IMN), a differential parallel power divider is employed to maximize efficiency and minimize spatial footprint, as shown in Fig. 4.18(a).



(a)



(b)

Fig. 4.19 (a) EM layout and (b) EM simulated S-parameters of the IMN.

The power splitter in the IMN design ensures minimal phase and amplitude discrepancies between output branches, with an inherent 0.3 dB loss due to wiring, as depicted in Fig. 4.18(b). A balun is an integrated post-splitter to perform impedance matching for the input, comprising L_{p_IMN} at 130pH, L_{s_IMN} at 140 pH, and a coupling factor of 0.74. A fine-tuning capacitor C_{p_IMN} of 120 fF ensures accurate frequency

response, while additional components, including a 90 fF capacitor and 500- Ω resistors, provide low-frequency stability.



The final matching architecture is shown in Fig. 4.19(a), with the corresponding S-parameters in Fig. 4.19(b) demonstrating that the overall IMN loss remains around 3.5 dB across the target frequency range, confirming its effectiveness in providing input matching within the operating bandwidth.

4.3.5 Stability Check

In the stability assessment of the proposed PA design, various configurations and setups were tested to ensure robust performance across a broad frequency range. This testing focused particularly on the inter-stage matching networks (ISMN1 and ISMN2) and the output matching network (OMN), with additional attention given to the influence of bias port placement on stability. Starting with ISMN1 and ISMN2, stability circles were plotted for each network across the 0.1 to 90 GHz frequency range, as shown in Figs. 4.20 and 4.21. These figures include source and load stability circles and mapping regions where the circuits maintain stable operation. Both ISMN1 and ISMN2 showed no signs of instability across the operational bandwidth, confirming their ability to reliably transfer signals between stages without introducing oscillations or other undesirable effects. Fig.

4.22 demonstrates the input pulse-testing stability check for transient response. The output voltage is observed over time after a pulse is applied to the input. This test evaluates the circuit's ability to handle sudden changes in input without oscillations or overshoots. The flat response of V_{out} suggests that the circuit is resilient to transient inputs, indicating that the ISMN1 and ISMN2 are both stable under varying signal conditions, which is essential for real-world operations where signal dynamics are not always constant.

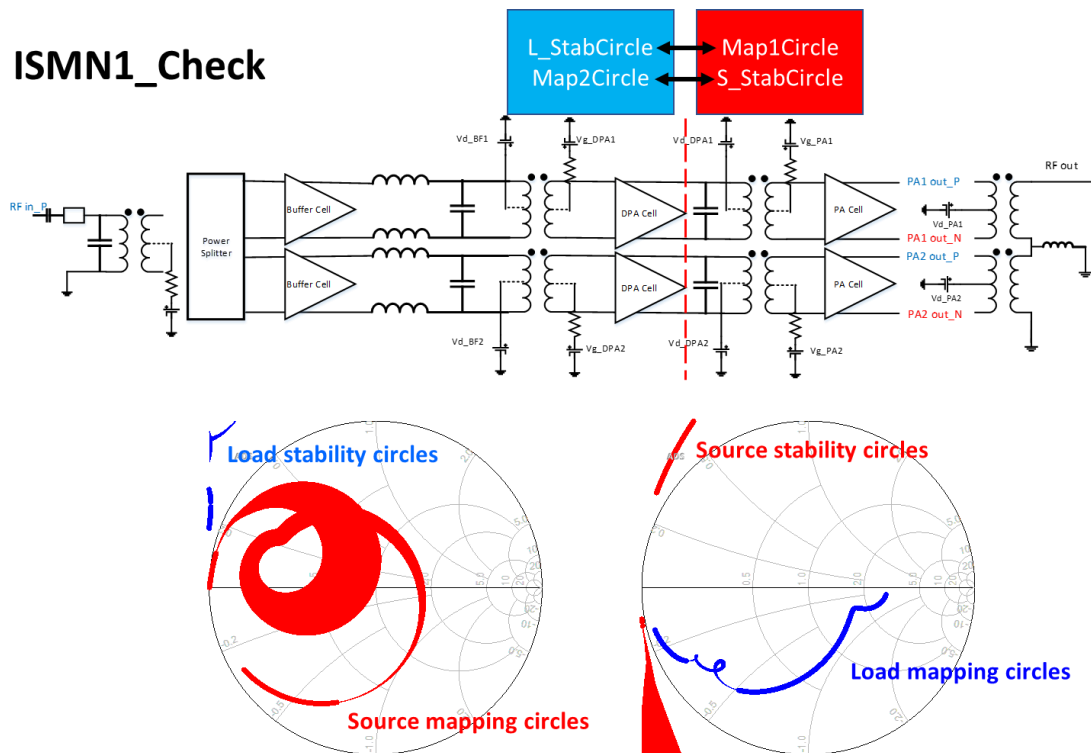


Fig. 4.20 Stability check of ISMN1 from 0.1-90 GHz.

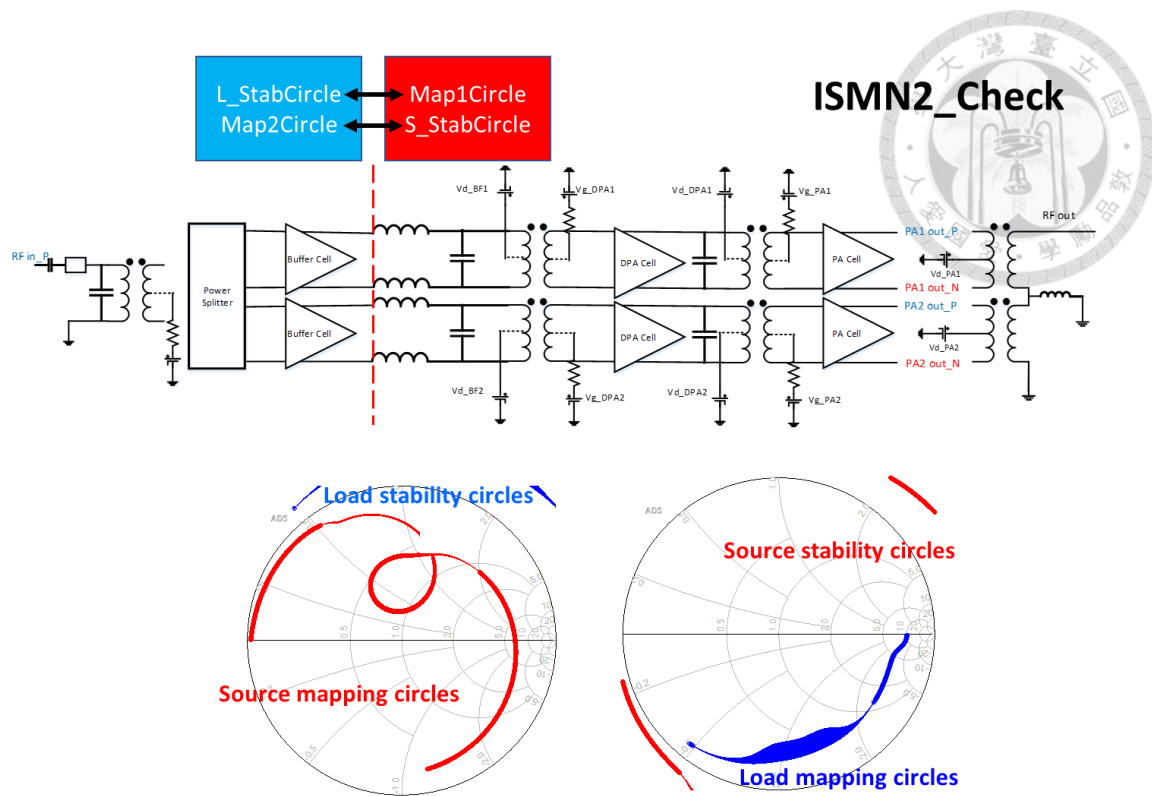


Fig. 4.21 Stability check of ISMN2 from 0.1-90 GHz.

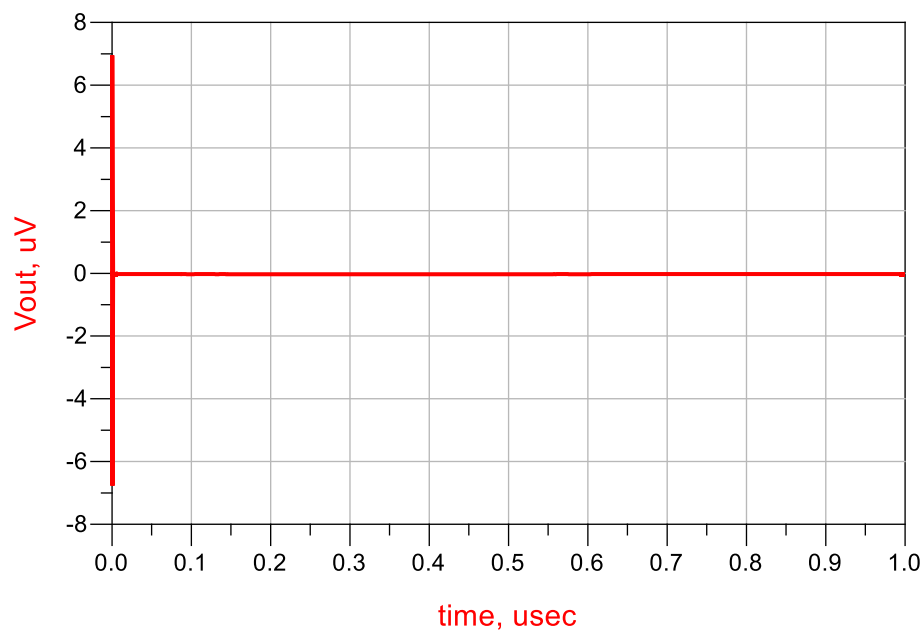


Fig. 4.22 Stability check of input pulse-testing.

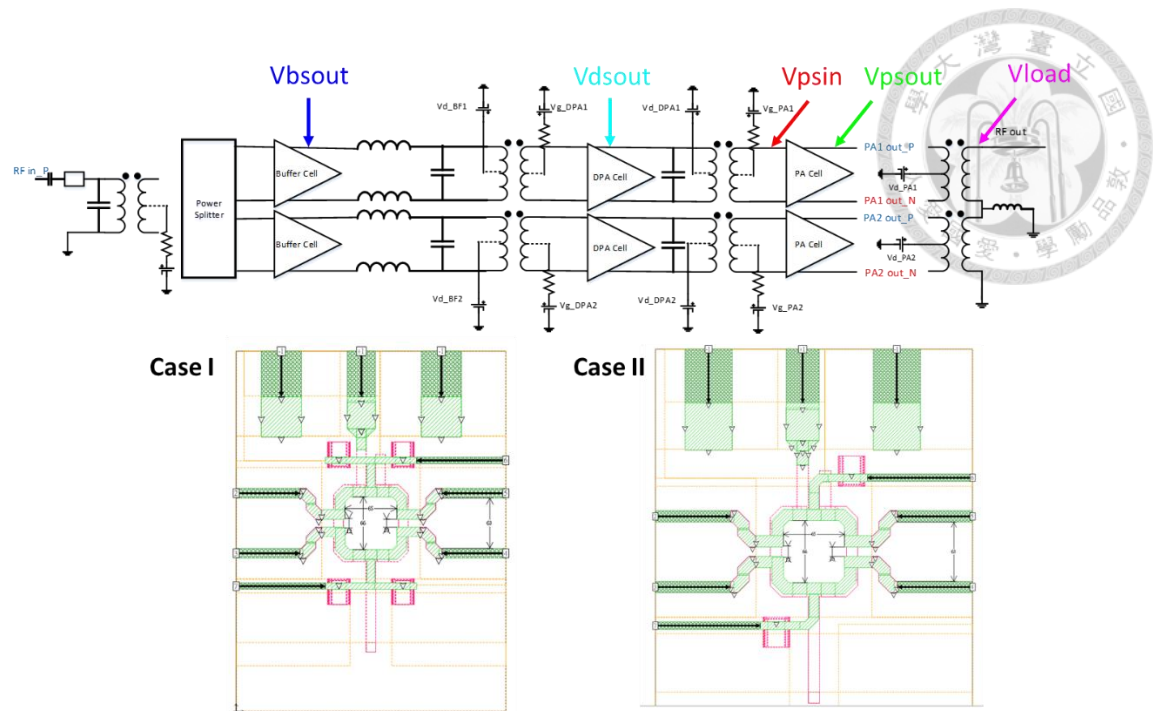


Fig. 4.23 Stability check of bias port pulse-testing with two cases of OMN.

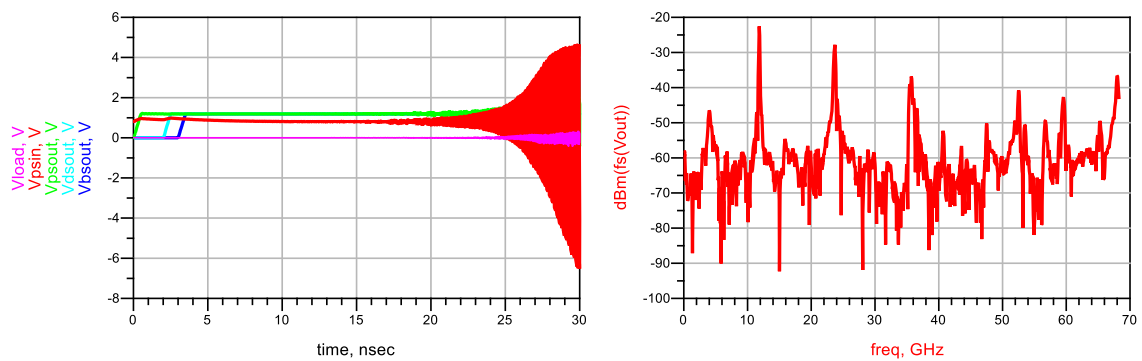


Fig. 4.24 Stability check of bias port pulse-testing in case-I of transient and frequency test.

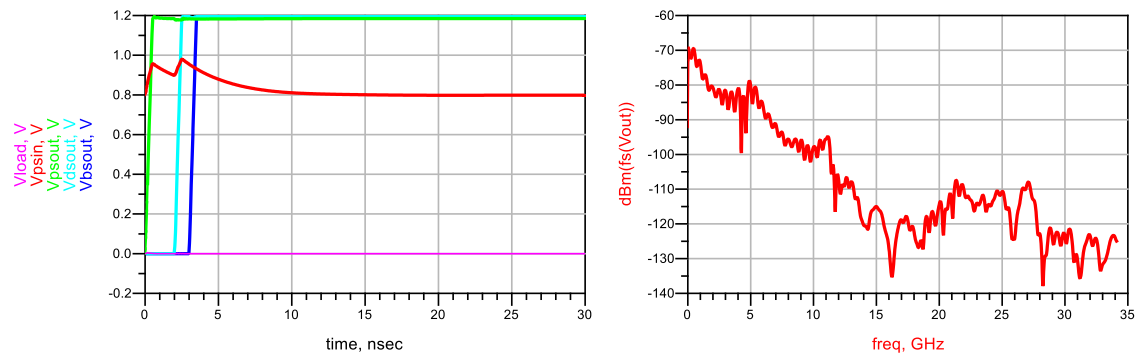


Fig. 4.25. Stability check of bias port pulse-testing in case-II of transient and frequency test.

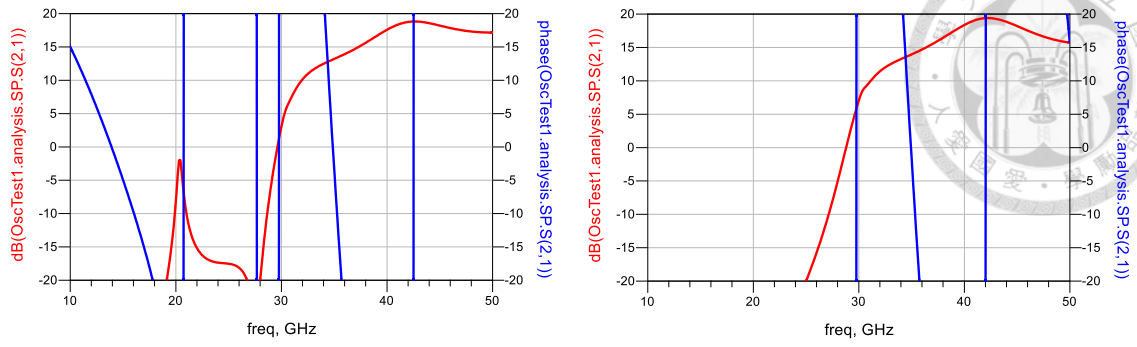


Fig. 4.26. Stability check of OscTest in (a) case-I, and (b) case-II.

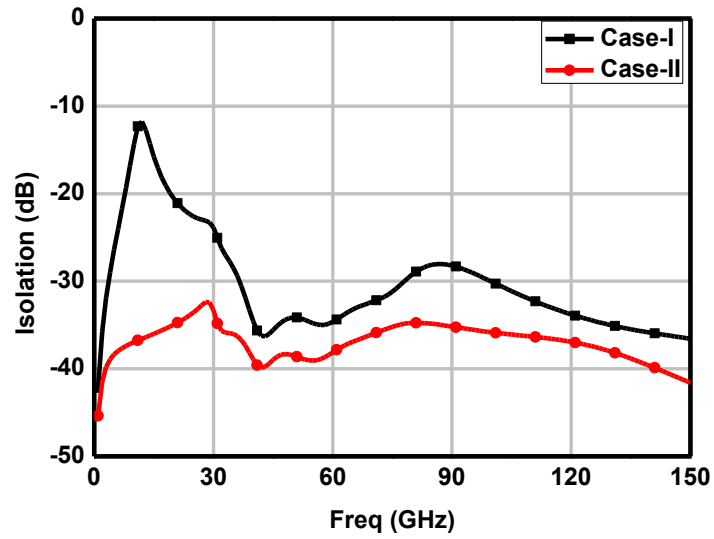


Fig. 4.27. Stability check of bias port with output port isolation.

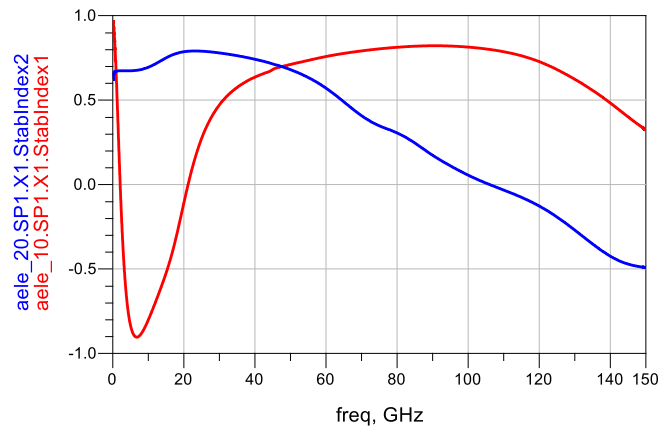


Fig. 4.28. Stability check of SProbePair.

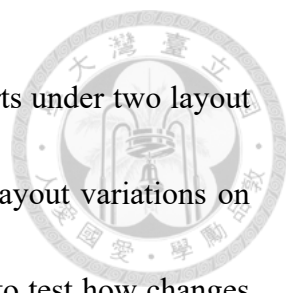


Fig. 4.23 initiates the stability exploration of the OMN bias ports under two layout configurations, labeled Case I and II, to understand the impact of layout variations on overall stability. In each configuration, the OMN layout is adjusted to test how changes in bias port positioning affect stability. This flexibility in layout allows for potential optimization in space usage and design improvements without compromising stability. This is particularly important for high-frequency designs where minor changes can have significant effects. The stability analysis continues in Fig. 4.24 and Fig. 4.25, where transient and frequency domain responses are examined to assess these configurations' more profound stability impact. In Case I (Fig. 4.24), oscillations were observed under certain frequency conditions with bias ports closer to the RF output. This indicates potential instability caused by coupling between the bias lines and RF output path, highlighting the risk of instability due to direct interaction between bias and RF signals. At the same time, we can also use the oscillation test to check whether the circuit will satisfy the Barkhausen stability criterion. Fig. 4.26(a) shows that Case-I will have 0 dB and 0 phase at 30 GHz, showing a certain degree of self-oscillatory risk.

In contrast, Case II (Fig. 4.25) positions the bias ports in a relatively asymmetrical layout, reducing their proximity to the RF output. This configuration demonstrated stable behavior across time and frequency domains with no oscillatory effects. Fig. 4.26(b) shows that Case-II hasn't 0 dB and 0 phase at full band, showing the circuit is safe.

Another stability check is the isolation test, testing the V_{DD} bias port with output port isolation. In Fig. 4.27, the isolation is poor in Case-I at 12 GHz, and this simulation is also the same as the transient test frequency results, and Case-II can obtain a full band of over 20 dB.

After the above stability checks, the common mode stability check is also important for differential circuits. The SProbePair is commonly used to analyze the differential and common-mode stability of differential circuits by breaking the circuit into “virtual” single-ended paths for measurement. This approach allows for evaluating potential feedback gains or reflection coefficients along various paths. Specifically, the Smith chart for $\Gamma_1 \times \Gamma_2 = \text{StabIndex1}$, and $\Gamma_3 \times \Gamma_4 = \text{StabIndex2}$ represents the stability characteristics of the circuit. Here, Γ_1 , Γ_2 , Γ_3 , and Γ_4 correspond to the reflection coefficients measured by the four probes (Probe1, Probe2, Probe3, Probe4) inserted by the SProbePair, typically representing unstable paths such as the differential input pair or specific feedback routes. $\Gamma_1 \times \Gamma_2$ quantifies the potential instability when both paths interact, especially in circuits with coupled feedback. If $|\Gamma_1 \times \Gamma_2| < 1$ ($\text{StabIndex1} < 1$), the paths are stable and do not pose a risk of oscillation. Conversely, $|\Gamma_1 \times \Gamma_2| > 1$ indicates a risk of oscillation, necessitating design adjustments. Fig. 4.28 shows that StabIndex1 and StabIndex2 of 4 probes are all below 1, which means the circuit common mode is stable.

The findings suggest that the asymmetric bias layout effectively mitigates the risk of



instability, providing a more robust design. Consequently, the final PA design adopts the more stable, asymmetric bias configuration from Case II, which, despite its slight deviation from symmetry, achieves reliable stability while maintaining the intended performance characteristics. This decision balances stability requirements and performance, ensuring the PA design remains resilient in high-frequency applications. Consequently, as Case II shows, the final design adopts the more stable, relatively asymmetric bias configuration to achieve reliable stability. While this layout is less symmetrical, the impact on overall performance is negligible, allowing the PA to maintain its intended characteristics while enhancing stability. This choice balances symmetry and practical stability requirements, ensuring the PA remains stable in high-frequency applications.

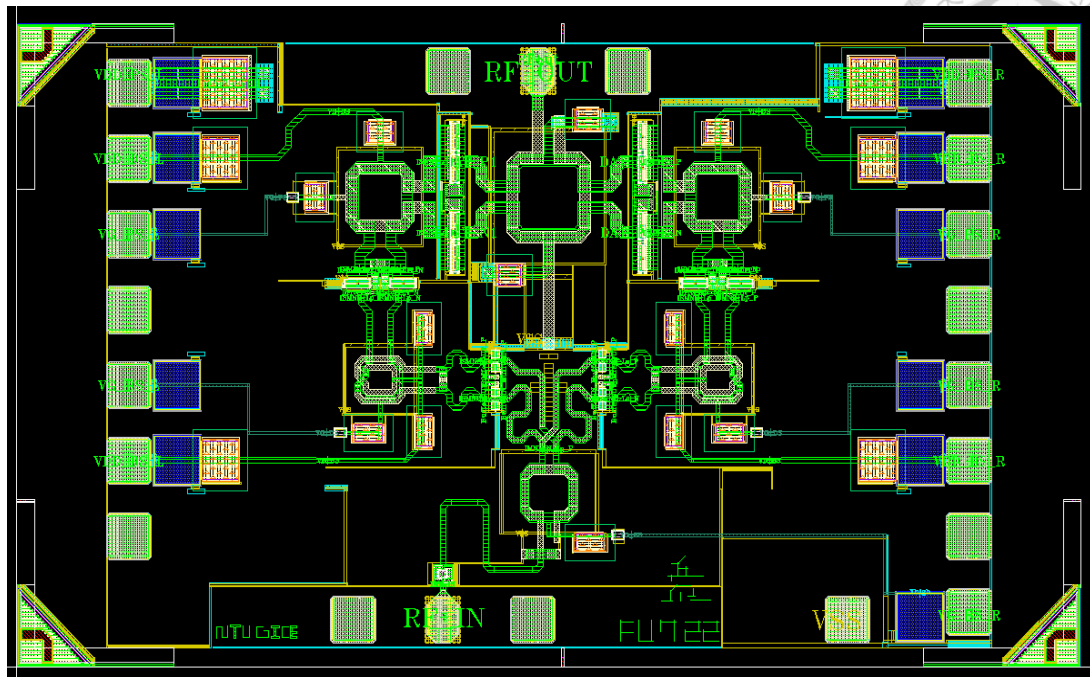


Fig. 4.29 Complete layout of the proposed PA ($1.186 \times 0.6805 \text{ mm}^2$).

Fig. 4.29 presents the complete layout of the proposed PA, integrating all stages and matching networks (ISMN1, ISMN2, IMN, and OMN) into a cohesive design. This layout demonstrates careful placement and interconnection strategies that minimize parasitic effects and optimize stability. The structure has been arranged to ensure that all stability requirements are met across the frequency range, as confirmed by the preceding stability analyses.

4.4 Measurement Results



The prototype PA was fabricated using a 90-nm bulk CMOS process, as shown in Fig. 4.30. It occupies a core area of 0.202 mm², with the total chip size, including the dicing street, 0.806 mm². Ground-signal-ground (GSG) probes were used to access the RF input and output pads, while wire bonding connected the DC pads to a printed circuit board (PCB). The PA operated at a supply voltage V_{DD} of 1.2 volts, with quiescent currents of 50 mA, 180 mA, and 386 mA for the first, second, and third stages, respectively, during measurement, which aligned with simulation results.

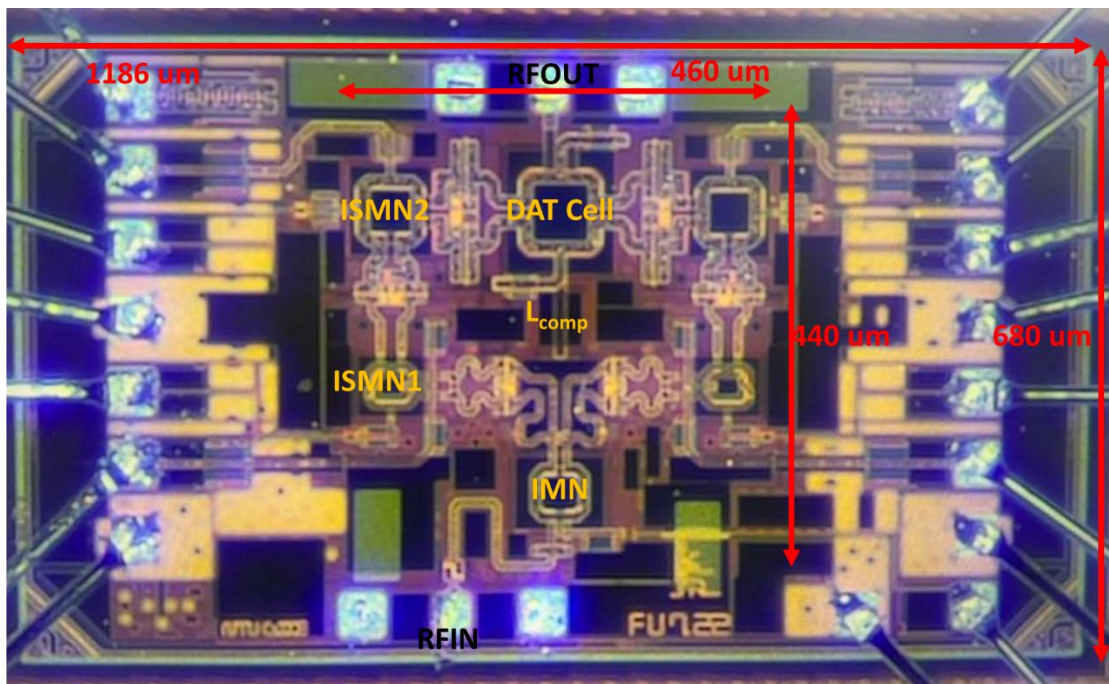


Fig. 4.30 Proposed PA's chip photograph (1.186×0.6805 mm²).

The PA's S-parameters were measured from 10 MHz to 67 GHz using a Keysight E8361A vector network analyzer. Large-signal performance in the 30–67 GHz range was assessed using a Keysight E8257D analog signal generator. Power measurements were conducted using a Keysight E4448A PSA for the 30–50 GHz range and an Anritsu MS2760A for 50–67 GHz. The schematic of the measurement setup is shown in Fig. 4.31.

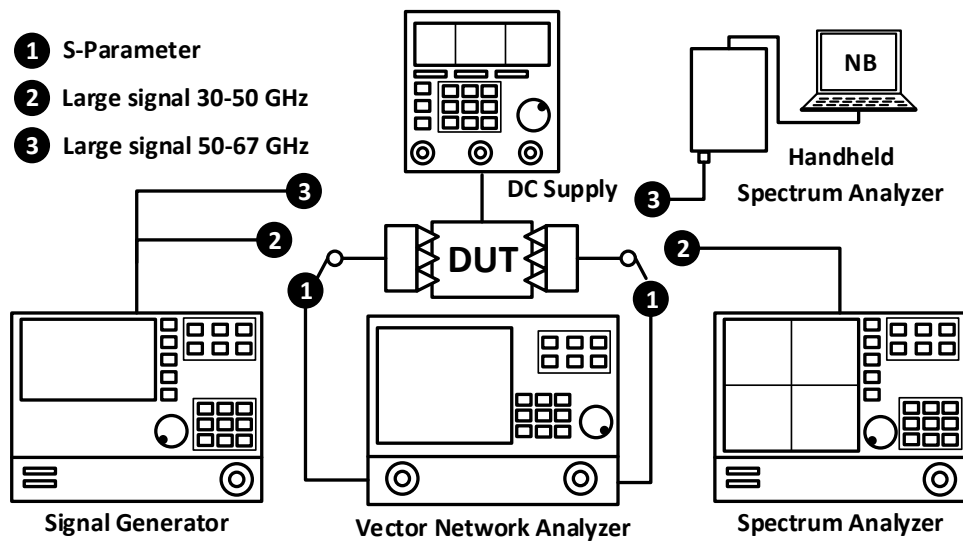


Fig. 4.31 Measurement setup.

4.4.1 Small-Signal S-Parameter Measurement

The comparison of the simulated and measured S-parameters of the PA over a frequency range from 10 MHz to 67 GHz is illustrated in Fig. 4.32. The measured results indicate that the proposed PA achieves an impressive 3 dB bandwidth spanning over 35

GHz, specifically from 31 GHz to 66 GHz, resulting in a fractional bandwidth (FBW) of 77%. At its peak frequency of 58 GHz, the PA reaches a significant gain of 21.6 dB. The gain remains stable within a ± 1 dB range across frequencies from 43 GHz to 65 GHz. The output return loss exceeds 10 dB over the frequency range from 52.5 GHz to 62 GHz, while the input return loss exceeds 5 dB across this same frequency span.

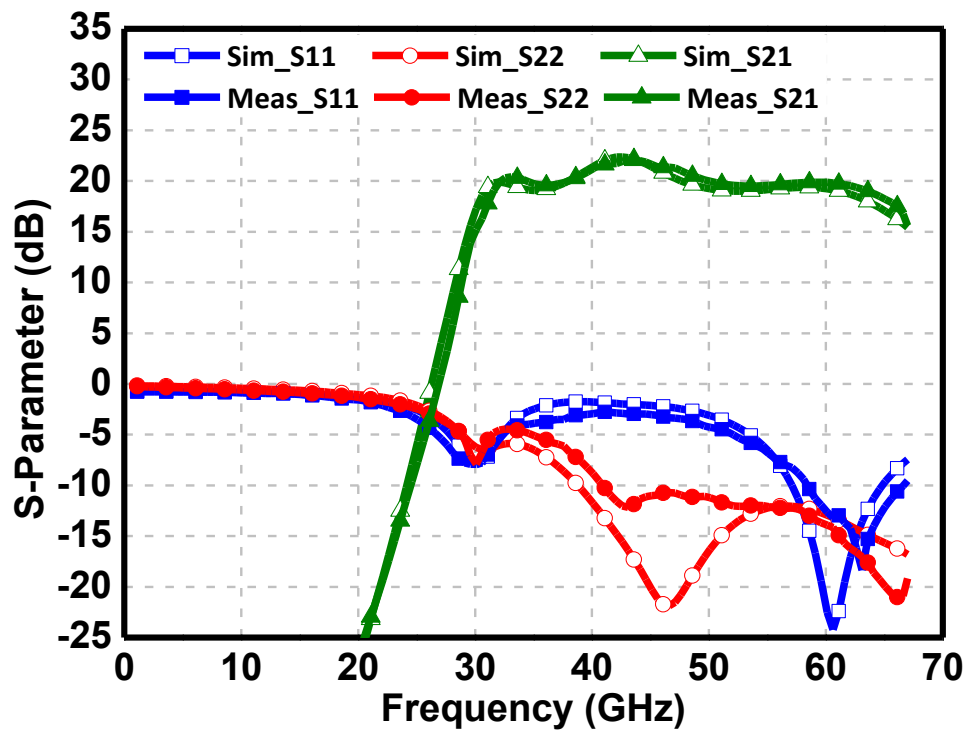


Fig. 4.32 Proposed PA's chip photograph.

4.4.2 Large-Signal Measurement

Fig. 4.33 presents the large-signal characteristics of the proposed 1.2 V PA at frequencies of 30, 40, 60, and 65 GHz, compared with simulation results. The measured P_{SAT} values are 16.3, 19.3, 20.2, and 19.6 dBm, with corresponding PAE_{max} of 6.8%,

14.6%, 16.7%, and 13%, respectively. Measurements were performed from 30 to 67 GHz at a 1.2 V supply voltage to evaluate and validate the PA's bandwidth under large-signal conditions.

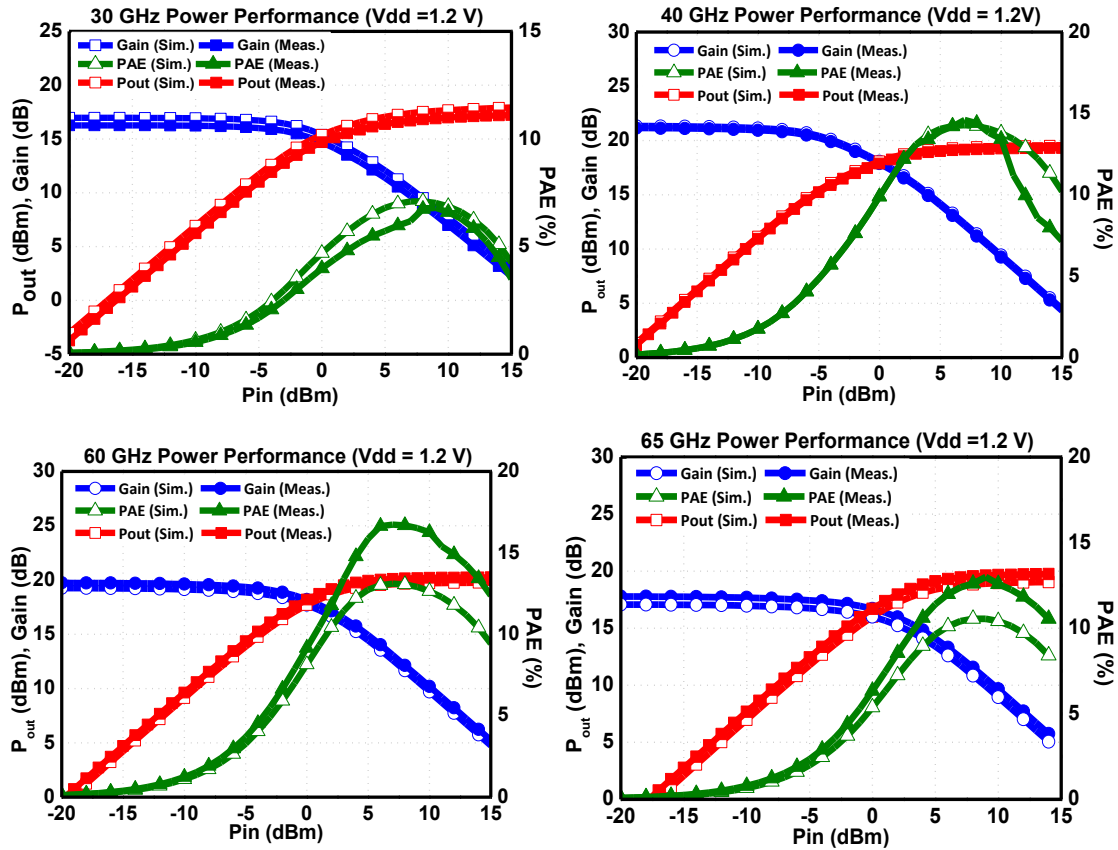


Fig. 4.33 Measured and simulated large-signal performances of the proposed PA at 30/40/60/65 GHz under 1.2 V V_{DD} .

These measurements, including P_{SAT} , PAE_{max} , and OP_{1dB} , are compared with simulation results in Fig. 4.34. Within the 32 to 66 GHz frequency range, the proposed PA demonstrates a P_{SAT} of 19.5 ± 1 dBm, a PAE_{max} of $13.7 \pm 3\%$, and an OP_{1dB} of 17 ± 1.2 dBm.

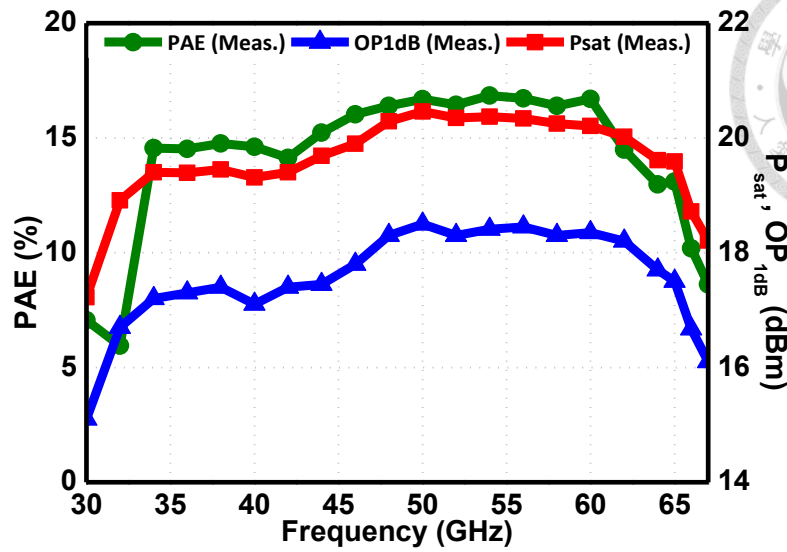


Fig. 4.34 Measured large-signal performances versus frequency of the proposed PA from 30 to 67 GHz.

According to Cripps (RF Power Amplifiers for Wireless Communications, pp. 60–63), the knee voltage effect refers to the nonlinearity that arises when the output voltage approaches a critical low level. At this point, the drain current no longer increases linearly with decreasing drain-source voltage, leading to current compression. Fig. 4.35 demonstrates how varying gate voltages (V_g) affect gain and drain current (I_d). Fig. 4.35(a) shows the simulated I_d and g_m versus V_g , and Fig. 4.35(b) demonstrates the I_d versus input power with different V_g of a single transistor. For lower bias conditions ($V_g = 0.2\sim 0.6$ V), the I_d increases with the input power (P_{in}). However, the I_d decreases with the P_{in} first and then rises at the high P_{in} . We think the knee voltage effect may cause it.

Fig. 4.36 shows the simulated voltage and current swings at the output of the single

side devices of our PA under 1.2-V V_{DD} and 0.8-V V_g , with $P_{in} = -15 \sim 15$ dBm/3 dB step.

As observed, the voltage and current swings increase with input power. In Fig. 4.36(a), voltage swings in areas A and B are symmetrical at low input power, but waveform A is compressed with a higher input power. It is because the lower end of the voltage swing reaches the knee voltage threshold, limiting current growth in area A, as shown in Fig. 4.36(b). Thus, the knee voltage effect imposes a lower limit on the voltage waveform, causing current compression.

The measured drain current at high input power levels is lower than the simulated values, which can be attributed to the knee voltage compression effect. This phenomenon, which is more pronounced than initially anticipated, exacerbates current compression. Notably, this current compression's reduced DC power consumption leads to a higher measured PAE than the simulated values. This is illustrated in Fig. 4.37, highlighting the discrepancy between the measured and simulated drain currents across the 30–65 GHz frequency range. The knee voltage compression limits the drain current's growth under high input power conditions, enhancing efficiency by reducing overall current consumption.

Fig. 4.38 and 4.39 show measurement results using 100 MHz and 200 MHz 64-QAM modulated signals. At 40 GHz, the PA achieves average output powers of 12.3 dBm and 11.6 dBm with an EVM_{rms} of -25 dB, while at 60 GHz, it delivers average output



powers of 11.8 dBm and 11.1 dBm.

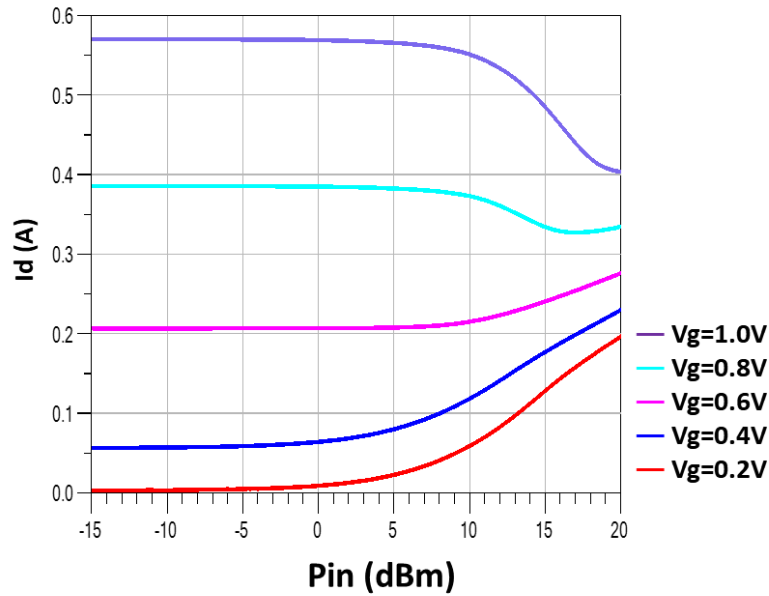
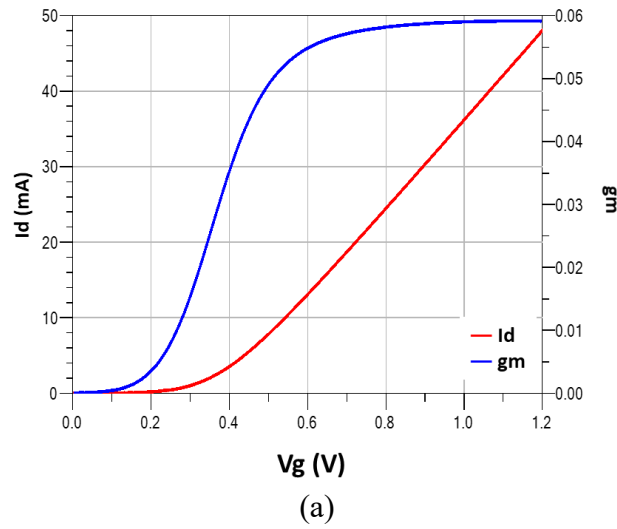
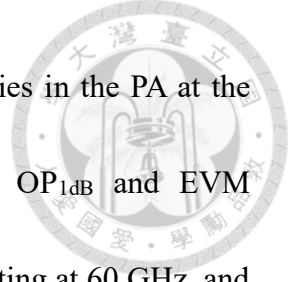


Fig. 4.35 Simulated (a) I_d and g_m versus V_g of a single device, and (b) I_d versus input power (P_{in}) with different V_g of power-stage device.

At 60 GHz, the P_{sat} is 20 dBm; however, the OP_{1dB} decreases by 2 dB. When measuring EVM to meet the minimum requirements, there is a further reduction of 6 dB, resulting in the usable efficiency being nearly 10% less than P_{sat} . This decrease in



efficiency can be attributed to several factors: increased nonlinearities in the PA at the higher frequency of 60 GHz, which adversely affect both the OP_{1dB} and EVM performance. Higher losses, reduced efficiency of components operating at 60 GHz, and the need to back off the PA's operating point from its P_{sat} to meet stringent signal integrity requirements.

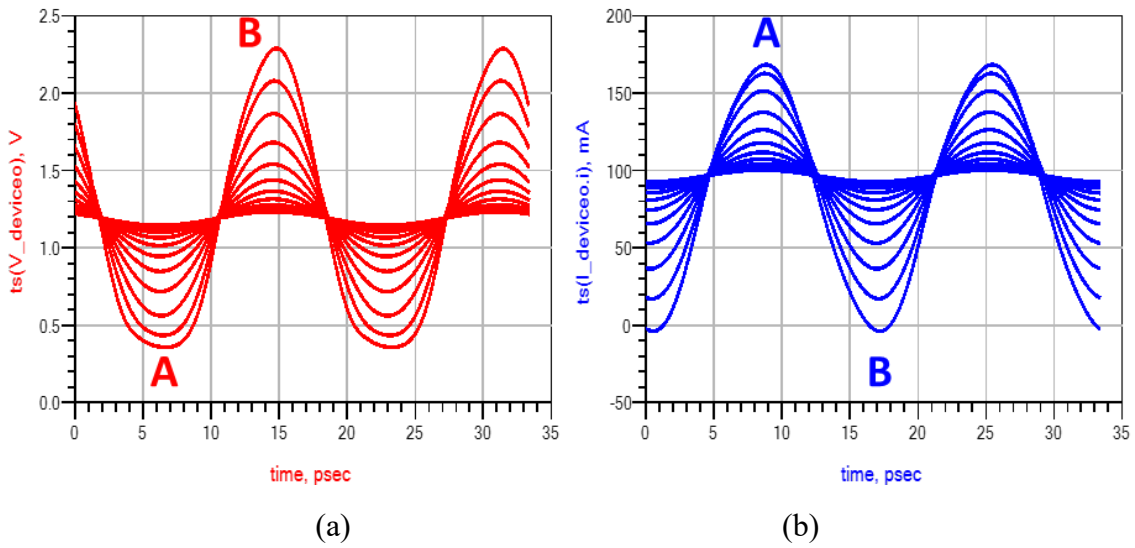


Fig. 4.36. Simulated (a) voltage swing and (b) current swing at the output of the single side devices under 1.2-V V_d and 0.8-V V_g , with $P_{in}=-15\sim15$ dBm/3 dB step.

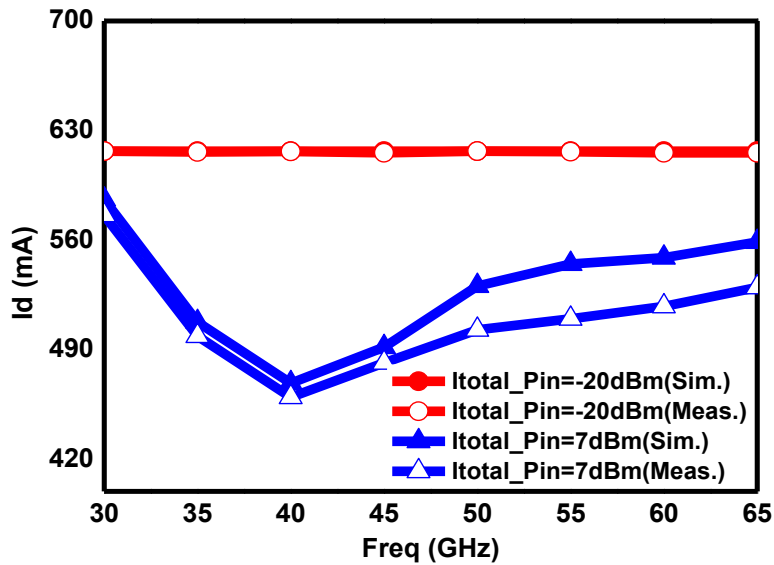


Fig. 4.37 Simulated and measured DC current with different P_{in} at 30-65 GHz.

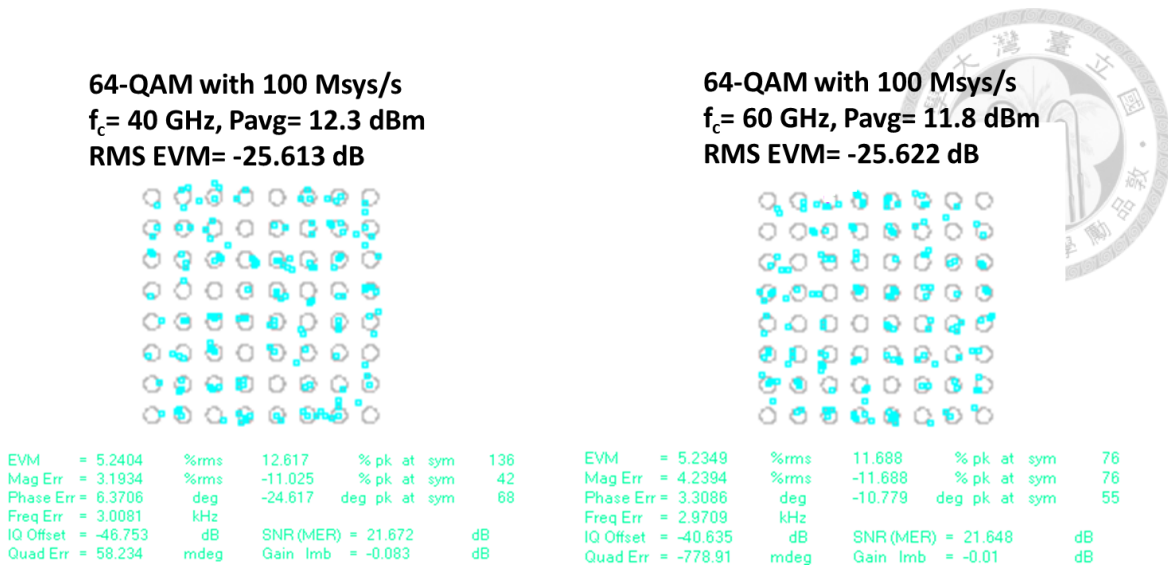


Fig. 4.38 Measured EVM of the designed PA using 64-QAM signal with 100 Msys/s at 40 GHz and 60 GHz.

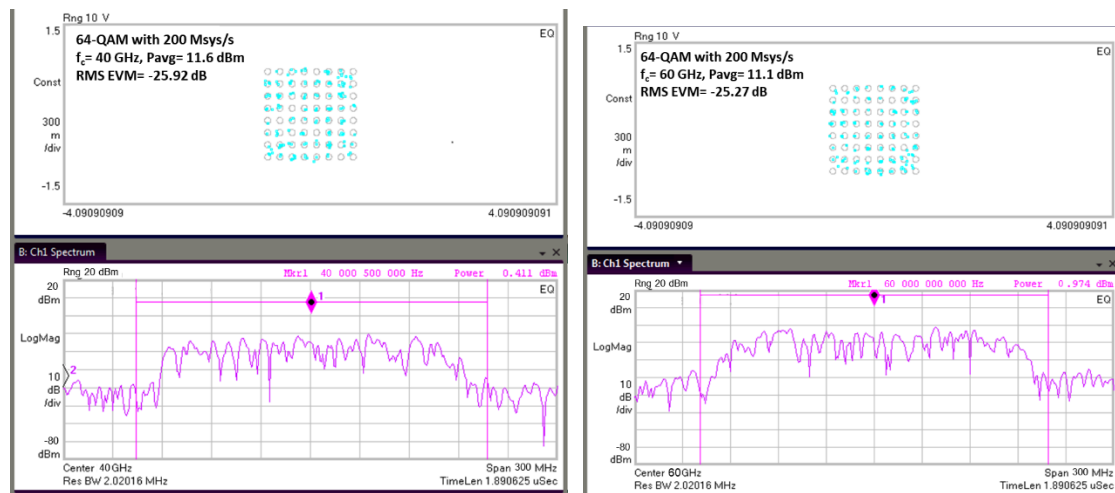
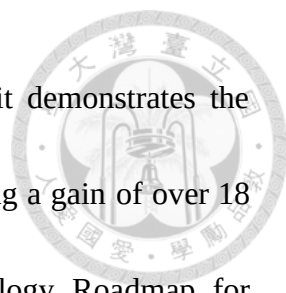


Fig. 4.39 Measured EVM of the designed PA using 64-QAM signal with 200 Msys/s at 40 GHz and 60 GHz.

4.5 Summary

Table 4.1 summarizes recent advancements in PAs with P_{SAT} above 16 dBm in the V-band or those with wideband performance implemented in CMOS processes. Compared with previously reported power-combined PAs, the proposed PA offers the



highest fractional bandwidth (FBW). Excluding stacked designs, it demonstrates the highest power density at 60 GHz in bulk CMOS processes, achieving a gain of over 18 dB. By utilizing the guidelines set by the International Technology Roadmap for Semiconductors (ITRS), the design addresses Figures of Merit (FoM₁) to maximize FBW (FoM₂). Notably, the proposed PA outperforms recent PAs in FoM₂, surpassing results achieved with silicon-on-insulator (SOI) processes [56].

The PA design in [56] stands out in terms of FoM₁ because it uses a 45 nm SOI CMOS process, which reduces combiner loss compared to bulk CMOS. However, in wideband scenarios [66], [68], [69], [70], other designs maintain high FBW, gain-bandwidth product (GBW), and FoM₂ values. Additionally, PAs reported in [45], [46], [47], [51], [54], require larger chip areas, resulting in reduced power density compared to the proposed PA. The novel PA architecture in this work enhances series combining efficiency by leveraging voltage-connecting and DAT structures, as discussed in [46], [48], [52]. Consequently, the proposed PA achieves superior power efficiency, with a P_{SAT} of 20.6 dBm and a high PAE at 60 GHz.

This paper introduces a pioneering 90-nm CMOS V-band PA design that employs a unique transformer combiner using the DAT structure. This combiner integrates high-power cells efficiently, preserving passive efficiency to enhance output power. The

design also optimizes layout, impedance matching, and parasitic parameters. Key performance metrics include a P_{SAT} of 20.6 dBm, a gain of 21.1 dB, a power density of 459.3 mW/mm², and a fractional bandwidth of 77.4%. The innovative DAT-based transformer combiner allows for design flexibility, enabling the development of cost-effective, high-efficiency, and highly integrated millimeter-wave PAs, supporting future demands for high-power CMOS designs in the millimeter-wave range.

Table 4.1 Comparison with previously published wideband and V-band PAs.

Ref	Process	Freq (GHz)	Topology	V _{DD} (V)	Gain (dB)	P _{sat} (dBm)	OP _{1dB} (dBm)	PAE _{max} (%)	Core Area (mm ²)	3 dB Bandwidth (GHz) / (%) *	Power Density (mW/mm ²)	GBW	FoM ₁	FoM ₂
[45]	65 nm CMOS	64	3-stage CS 32-way DSPC	1.2	16.3	23.2	19.6	10	2.04	25.1 / 41.8	104.8	164	85.7	118
[46]	40 nm CMOS	60	4-stage CS 4-way DAT	1.2	29	22.6	17	7	2.16	7 / 11.6	84.2	197.3	95.6	116.9
[47]	90 nm CMOS	60	2-stage CS 2-way Wilkinson-PC	1.2	20.6	19.9	18.2	14.2	1.67	8 / 12.9	58.7	85.7	87.6	109.8
[48]	65 nm CMOS	60	4-stage CS 4-way DAT	1.2	26.6	17.5	14.3	10.3	0.32	16 / 27.3	175.7	342.1	89.8	118.5
[49]	90 nm CMOS	60	3-stage CS 4-way Radial-PC	1.2	20.1	20.6	17.6	20.3	0.43	24.5 / 46.5	265.8	247.8	89.3	122.7
[50]	90 nm CMOS	58	2-stage stack 2-way PPC	2.4	19.6	22.2	19.7	17.8	0.26	8.8 / 16.3	628.6	84	89.6	113.8
[51]	55 nm CMOS	60	4-stage CS 32-way HPC	1.2	21.9	25	21.7	11	1.77	5 / 8.4	178.7	62.2	92.9	111.4
[52]	28 nm CMOS	81	3-stage CS 2-way DAT	0.9	12.2	12.2	-	12	0.178	16.1 / 20	92	65.2	73.3	99.3
[53]	65 nm CMOS	60	3-stage CS/cascode 4-way Radial-PC	2.4	29.7	23.7	19.9	22	0.65	7 / 11.8	359	213.8	102.4	123.8
[54]	45 nm CMOS SOI	60	1-stage cascode 8-way cascaded-DAT	2.2	24.7	30.1	25.4	20.8	6.6	9 / 15.2	155	154.6	103.5	127.1
[66]	22 nm CMOS SOI	58	1-stage CS Class-J/F	1.1	15.1	14.3	10.6	42.3	0.0198	12.1 / 20.1	1359.4	68.8	80.9	107
[68]	28 nm CMOS	32	2-stage Cascode+CS Feedback linearizer	1.8 / 1	20.5	20.3	19	33.6	0.106	24.1 / 75.3	1010	255	86.2	124
[61]	28 nm CMOS	43	2-stage Cascode+CS 2-way SPC	0.9	20.8	15.9	11.1	18.4	0.16	28 / 65.1	243	307	82	118
[69]	45 nm CMOS SOI	37	2-stage Cascode+CS Compensated Balun	2 / 1	20.5	20	18.9	38.7	0.21	17.6 / 52.6	476	186	87.7	122
This work	90 nm CMOS	60	3-stage CS 2-way DAT	1.2	21.1	20.6	17	16.7	0.202	35 / 77.4	568.4	397.3	89.5	127.3

*Fractional bandwidth, CS: common source, DSPC: direct-shunt power combining, PPC: parallel power combining,

HPC: hybrid power combining, SPC: series power combining

FoM₁ (ITRS) = P_{sat} (dBm) + Gain (dB) + 20log [Freq (GHz)] + 10log [PAE_{max} (%)]

FoM₂ = P_{sat} (dBm) + Gain (dB) + 20log [Freq (GHz)] + 10log [PAE_{max} (%)] + 20log [FBW (%)]

Chapter 5 Conclusion



This thesis comprehensively explores mmWave PA designs optimized for high-frequency wireless communication applications, focusing on addressing the challenges posed by 5G and beyond. The study has systematically tackled the critical aspects of PA design, including bandwidth enhancement, power efficiency, and implementing innovative combining techniques to improve performance. The research is divided into three core chapters, each contributing significant insights and advancements in PA technology.

Chapter II investigated various bandwidth enhancement techniques crucial for mmWave PA performance. The challenges introduced by RLC tank circuits and the Bode-Fano limit, techniques such as MCR were presented to achieve wideband impedance matching, and extended matching network models like the T and π configurations were discussed, showing their practical utility in III-V semiconductor processes with limited metal layers.

Chapter III focused on designing a high-power GaAs PA in the K/Ka-band tailored for the demands of 5G/6G applications. A novel multi-stage matching network was introduced, explicitly designed to achieve wideband performance and a high impedance transformation ratio. This multi-resonance architecture employed sequential inductors and capacitors, allowing for effective impedance matching over a broad frequency range

from 24 to 32 GHz while maintaining the necessary high impedance transformation ratio. The results demonstrated substantial improvements in power density, gain, and peak power-added efficiency (PAE), underscoring the GaAs process's value in compact, high-power mmWave amplifier design.

Chapter IV introduced a novel DAT architecture for mmWave applications optimized for high efficiency and wide bandwidth. This design incorporated a two-way series power-combining architecture and an innovative compensation inductor, which was critical in reducing phase and amplitude imbalances in the combining path caused by parasitic effects. Using L_{comp} to counteract parasitic capacitances, the DAT achieved improved efficiency and impedance power matching across a frequency range from 31 to 65 GHz. The measured results confirmed excellent performance, with a P_{SAT} of approximately 20 dBm and high power-added efficiency, positioning this architecture as a robust solution for high-frequency communication systems.

In conclusion, this thesis contributes significant advancements to mmWave PA design, establishing new methodologies for bandwidth enhancement, power efficiency, and transformer-based combining techniques. The findings presented across these chapters strongly align with the evolving requirements of next-generation wireless communication systems, including the 5G and 6G standards. The proposed designs deliver high performance and efficiency and pave the way for further innovations in

achieving robust, wideband, and high-power PAs for future mmWave applications.



Appendix



1. Stability simulation: SProbePair vs Mapping and Stability circle

SProbePair and Load/Source (L/S) Stability with Mapping Circle offer distinct approaches tailored to different circuit design and analysis stages when evaluating transistor stability. SProbePair is ideal for scenarios where the preceding and succeeding circuit stages are already defined. It enables direct measurement and assessment of the transistor's S-parameters and stability under the specific load conditions of the finalized circuit. This method is relatively swift and provides results that closely mirror the transistor's performance in its intended application. In contrast, Load/Source Stability with Mapping Circle takes a more comprehensive approach by scanning the entire Smith Chart for possible reflection coefficients at the load or source terminals. This technique delineates potentially unstable regions by plotting stability circles, making it particularly useful during the initial design phases or when verifying unconditional stability is critical. While SProbePair may indicate that a transistor is stable under specific load or source conditions, L/S Stability with Mapping Circle can reveal instability across a broader range of impedance scenarios. Conversely, if L/S Stability with Mapping Circle confirms unconditional stability, it inherently assures that the transistor will remain stable under any specific load or source condition examined by SProbePair. Therefore, L/S Stability with Mapping Circle provides a more exhaustive stability analysis, ensuring robustness

across diverse operating environments, whereas SProbePair offers targeted insights aligned with a particular circuit configuration.



2. Stability simulation: OscTest

The **ADS OscTest** feature is designed to assess the stability of complex circuits by strategically inserting test points into suspected feedback paths, effectively breaking the original closed-loop configuration. This allows for the measurement of open-loop S-parameters and the examination of loop gain and phase to determine if the circuit meets the Barkhausen oscillation criteria: specifically, that at a certain frequency, the open-loop gain is greater than or equal to 1 (0 dB) and the total phase shift is 0° (or an integer multiple of 360°). The theoretical foundation of OscTest is rooted in control theory and the widely used Barkhausen and Nyquist stability criteria in high-frequency circuit design. According to these principles, the system may exhibit self-sustained oscillations if both the loop gain and phase reach their critical values simultaneously. In simulations, OscTest evaluates the risk of oscillation by observing whether the magnitude $\text{dB}(S_{21})$ and the phase $\arg(S_{21})$ concurrently cross 0 dB and 0° , respectively, while also utilizing indicators such as StabFact to detect the presence of negative impedance phenomena. By effectively "opening" the feedback network within a complex circuit and focusing on the loop gain, OscTest is particularly valuable for quickly screening RF and microwave

power amplifiers, oscillators, and various high-gain circuits. This ensures the rapid identification and prevention of potential parasitic oscillations, thereby enhancing the reliability and performance of high-frequency electronic designs.



3. Section III - multi-resonance matching network, design concepts:

The design of the output matching network for a multi-resonance matching system begins with determining the desired transformation ratio. The Magnetic Coupled Resonator (MCR) T-model was initially employed to achieve this matching. However, it was discovered that the mutual inductance (L_m) is influenced by the primary inductance (L_p), the secondary inductance (L_s), and the bandwidth (defined by parameter k). This dependency led to the model collapsing and generating a negative inductance, making the MCR T-model unsuitable for the application. Consequently, the design approach was shifted to a dual-mode matching network. Unfortunately, due to the presence of the Forbidden region, the dual-mode network could not match the intended impedance. Recognizing that a four-stage matching network could not meet the requirements, the decision was made to incorporate two additional stages into the matching network design. This architecture achieves a high transformation ratio. However, the components' quality factor (Q) influences the matching paths, meaning the solution cannot be guaranteed as optimal. Nonetheless, the resulting design is a valuable reference and inspiration for

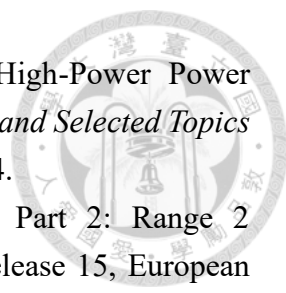
future matching network developments.





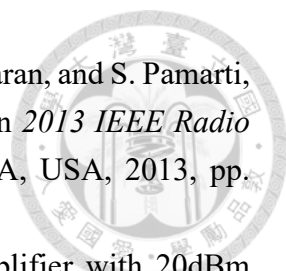
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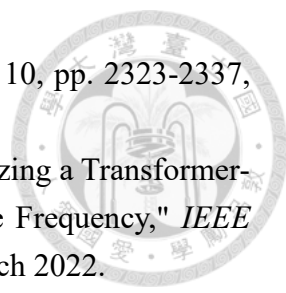
- [1]. Qualcomm, "Global update on 5G spectrum," Dec. 2020. [Online]. Available:
https://www.qualcomm.com/content/dam/qcommmartech/dmassets/documents/20200625_mipi_-_5g_spectrum_-_dean_brenner_4.pdf
- [2]. W.M.C. Sansen, Analog Design Essentials, vol. 859 (Springer Science and Business Media, Berlin, 2007)
- [3]. T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, 2nd ed. Cambridge: Cambridge University Press, 2003.
- [4]. A. Mazzanti and A. Bevilacqua, "On the Phase Noise Performance of Transformer-Based CMOS Differential-Pair Harmonic Oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 9, pp. 2334-2341, Sept. 2015.
- [5]. A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2259-2268, Dec. 2004.
- [6]. M. Vigilante and P. Reynaert, "20.10 A 68.1-to-96.4GHz variable-gain low-noise amplifier in 28nm CMOS," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2016, pp. 360-362.
- [7]. P. -C. Huang, Z. -M. Tsai, K. -Y. Lin and H. Wang, "A 17–35 GHz Broadband, High-Efficiency PHEMT Power Amplifier Using Synthesized Transformer Matching Technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 1, pp. 112-119, Jan. 2012.
- [8]. J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 9, pp. 1368-1382, Sept. 2000.
- [9]. N. M. Nguyen and R. G. Meyer, "Si IC-compatible inductors and LC passive filters," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 4, pp. 1028-1031, Aug. 1990.
- [10]. J. Zhao, M. Bassi, A. Bevilacqua, A. Ghilioni, A. Mazzanti and F. Svelto, "A 40–67GHz power amplifier with 13dBm PSAT and 16% PAE in 28 nm CMOS LP," in *ESSCIRC 2014 - 40th European Solid-State Circuits Conference (ESSCIRC)*, Venice Lido, Italy, 2014, pp. 179-182.
- [11]. J. S. Park and H. Wang, "A Transformer-Based Poly-Phase Network for Ultra-Broadband Quadrature Signal Generation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 12, pp. 4444-4457, Dec. 2015.
- [12]. T. Guillod, F. Krismer, and J. W. Kolar, "Magnetic equivalent circuit of MF transformers: modeling and parameter uncertainties," *Electrical Engineering*, vol. 100, pp. 2261-2275, May 2018.
- [13]. Z. -H. Fu, M. -X. Li, T. -G. Ma, C. -S. Wu and K. -Y. Lin, "Millimeter-Wave GaAs

- 
- Ultra-Wideband Medium Power Amplifier and Broadband High-Power Power Amplifier for 5G/6G Applications," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 14, no. 1, pp. 111-121, March 2024.
- [14]. User Equipment (UE) Radio Transmission and Reception; Part 2: Range 2 Standalone, document 3GPP TS 38.101-2, Version 15.12.0, Release 15, European Telecommunications Standards Institute, Jan. 2021. [Online]. Available:
https://www.etsi.org/deliver/etsits/138100_138199/13810102/15.12.00_60/ts_13810102v151200p.pdf
- [15]. D. P. Nguyen, T. Pham, B. L. Pham, and A. -V. Pham, "A High-Efficiency High Power Density Harmonic-Tuned Ka Band Stacked-FET GaAs Power Amplifier," in *2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Austin, TX, USA, 2016, pp. 1-4.
- [16]. N. Hosseinzadeh and A. Medi, "Wideband 5 W Ka-Band GaAs Power Amplifier," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 8, pp. 622-624, Aug. 2016.
- [17]. A. Alizadeh, M. Frounchi and A. Medi, "On Design of Wideband Compact-Size Ka/Q-Band High-Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 6, pp. 1831-1842, June 2016.
- [18]. G. Lv, W. Chen and Z. Feng, "A Compact and Broadband Ka-band Asymmetrical GaAs Doherty Power Amplifier MMIC for 5G Communications," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, Philadelphia, PA, USA, 2018, pp. 808-811.
- [19]. D. P. Nguyen, J. Curtis and A. -V. Pham, "A Doherty Amplifier with Modified Load Modulation Scheme Based on Load–Pull Data," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 1, pp. 227-236, Jan. 2018.
- [20]. P. Neininger, L. John, P. Brückner, C. Friesicke, R. Quay, and T. Zwick, "Design, Analysis and Evaluation of a Broadband High-Power Amplifier for Ka-Band Frequencies," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, Boston, MA, USA, 2019, pp. 564-567.
- [21]. J. Zhang, T. Wu, L. Nie, D. Wei, S. Ma, and J. Ren, "A 20-30 GHz Compact PHEMT Power Amplifier Using Coupled-Line Based MCCR Matching Technique," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, Los Angeles, CA, USA, 2020, pp. 956-959.
- [22]. C. Ramella, V. Camarchia, A. Piacibello, M. Pirola, and R. Quaglia, "Watt-Level 21–25-GHz Integrated Doherty Power Amplifier in GaAs Technology," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 5, pp. 505-508, May 2021.
- [23]. Y.-F. Tsao, H.-S. Hsu, J. Würfl, and H.-T. Hsu, "Dual-Band Power Amplifier Design

- at 28/38 GHz for 5G New Radio Applications," *IEEE Access*, vol. 10, pp. 77826-77836, 2022.
- [24]. Z. Sun, Z. Liu, T. Wu, H. Yu, Y. Chen, and S. Ma, "A 33-37GHz Two-Path Power Amplifier with >18-dB Gain and 26.7-dBm Psat in 150nm GaAs Process," in *2022 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia)*, Shenzhen, China, 2022, pp. 64-67.
- [25]. H. W. Bode, *Network Analysis and Feedback Amplifier Design.*, Princeton, 1945, [Online]. Available: https://ia601702.us.archive.org/30/items/dli.ernet.15701/15701Network%20Analysis%20And%20Feedback%20Amplifier%20Design_text.pdf
- [26]. G. Lv, W. Chen, X. Chen, and Z. Feng, "An Energy-Efficient Ka / Q Dual-Band Power Amplifier MMIC in 0.1- μ m GaAs Process," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 6, pp. 530-532, June 2018.
- [27]. C. R. Chappidi and K. Sengupta, "Globally Optimal Matching Networks with Lossy Passives and Efficiency Bounds," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 1, pp. 257-269, Jan. 2018.
- [28]. B.-W. Huang, Z.-H. Fu, and K.-Y. Lin, "A 28/39 GHz Dual-Band Power Amplifier Using Optimal Matching Contour in GaAs pHEMT," in *2021 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Hualien, Taiwan, 2021, pp. 1-3.
- [29]. B.-W. Huang, Z.-H. Fu, and K.-Y. Lin, "A Millimeter-Wave Ultra-Wide Band Power Amplifier in 0.15- μ m GaAs pHEMT for 5G Communication," in *2022 Asia-Pacific Microwave Conference (APMC)*, Yokohama, Japan, 2022, pp. 97-99.
- [30]. I. Huang et al., "A 29.6 dBm 29-GHz Power Amplifier for Satellite and 5G Communications Using 0.15- μ m GaAs p-HEMT Technology," in *2018 Asia-Pacific Microwave Conference (APMC)*, Kyoto, Japan, 2018, pp. 986-988.
- [31]. H. Jia, C. C. Prawoto, B. Chi, Z. Wang, and C. P. Yue, "A Full Ka-Band Power Amplifier With 32.9% PAE and 15.3-dBm Power in 65-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 9, pp. 2657-2668, Sept. 2018.
- [32]. G. Cho and S. Hong, "Ka-Band CMOS Power Amplifier Based on Transmission Line Transformers with Single-Ended Doherty Network," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 11, pp. 1223-1226, Nov. 2021.
- [33]. S. Srivastava and P. P. Dash, "Non-Orthogonal Multiple Access: Procession towards B5G and 6G," in *2021 IEEE 2nd International Conference on Applied Electromagnetics, Signal Processing, & Communication (AESPC)*, Bhubaneswar, India, 2021, pp.
- [34]. S. D. L, R. Dilli and K. M, "Statistical Modelling of Massive MIMO Channel at

- 
- FR2 Frequency Bands for B5G Networks," in *2023 International Conference on Advances in Intelligent Computing and Applications (AICAPS)*, Kochi, India, 2023, pp. 1-5
- [35]. N. Hasegawa, Y. Nakamoto, T. Hirakawa, and Y. Ohta, "Function Expansion of B5G/6G Mobile Base Stations for Wireless Power Transfer," in *2022 Asia-Pacific Microwave Conference (APMC)*, Yokohama, Japan, 2022, pp. 348-349.
- [36]. D. Wang, W. Chen, X. Chen, X. Liu, F. M. Ghannouchi, and Z. Feng, "A 24-29.5 GHz Voltage-Combined Doherty Power Amplifier Based on Compact Low-Loss Combiner," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 7, pp. 2342-2346, July 2021.
- [37]. J. Lee and S. Hong, "A 24–30 GHz 31.7% Fractional Bandwidth Power Amplifier with an Adaptive Capacitance Linearizer," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 4, pp. 1163-1167, April 2021.
- [38]. C. Yu, J. Feng, and D. Zhao, "A 28-GHz Doherty Power Amplifier with a Compact Transformer-Based Quadrature Hybrid in 65-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 8, pp. 2790-2794, Aug. 2021.
- [39]. L. Chen, L. Chen, Z. Ge, Y. Sun, and X. Zhu, "A 40-GHz Load Modulated Balanced Power Amplifier Using Unequal Power Splitter and Phase Compensation Network in 45-nm SOI CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 8, pp. 3178-3186, Aug. 2023, doi: 10.1109/TCSI.2023.3282731.
- [40]. L. Chen, L. Chen, H. Zhu, R. Gómez-García, and X. Zhu, "A Wideband Balanced Amplifier Using Edge-Coupled Quadrature Couplers in 0.13- μm SiGe HBT Technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 2, pp. 631-641, Feb. 2023.
- [41]. L. Chen, H. Liu, J. Hora, J. A. Zhang, K. S. Yeo, and X. Zhu, "A Monolithically Integrated Single-Input Load-Modulated Balanced Amplifier with Enhanced Efficiency at Power Back-Off," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 5, pp. 1553-1564, May 2021.
- [42]. SpaceX [Online]. Available: <https://www.spacex.com/>
- [43]. Amazon [Online]. Available: <https://www.amazon.com/>
- [44]. Federal Communications Commission, "FCC Empowers Short-Range Radars in the 60 GHz Band," Aug. 2023. [Online]. Available: <https://www.federalregister.gov/documents/2023/07/24/202315367/fcc-empowers-short-range-radars-in-the-60-ghz-band>.
- [45]. Y. -H. Hsiao, Z. -M. Tsai, H. -C. Liao, J. -C. Kao and H. Wang, "Millimeter-Wave CMOS Power Amplifiers with High Output Power and Wideband Performances," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 12, pp. 4520-4533, Dec. 2013.

- 
- [46]. F. Shirinfar, M. Nariman, T. Sowlati, M. Rofougaran, R. Rofougaran, and S. Pamarti, "A fully integrated 22.6dBm mm-Wave PA in 40nm CMOS," in *2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Seattle, WA, USA, 2013, pp. 279-282.
- [47]. C. Y. Law and A. -V. Pham, "A high-gain 60GHz power amplifier with 20dBm output power in 90nm CMOS," in *2010 IEEE International Solid-State Circuits Conference -(ISSCC)*, San Francisco, CA, USA, 2010, pp. 426-427.
- [48]. J. -A. Han, Z. -H. Kong, K. Ma, and K. S. Yeo, "A 26.8 dB Gain 19.7 dBm CMOS Power Amplifier Using 4-way Hybrid Coupling Combiner," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 1, pp. 43-45, Jan. 2015.
- [49]. C. -F. Chou, Y. -H. Hsiao, Y. -C. Wu, Y. -H. Lin, C. -W. Wu and H. Wang, "Design of a V-Band 20-dBm Wideband Power Amplifier Using Transformer-Based Radial Power Combining in 90-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4545-4560, Dec. 2016.
- [50]. W. -C. Sun and C. -N. Kuo, "A 19.1% PAE, 22.4-dBm 53-GHz Parallel Power Combining Power Amplifier with Stacked-FET Techniques in 90-nm CMOS," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, Boston, MA, USA, 2019, pp. 327-330.
- [51]. L. Zhang, K. Ma, and H. Fu, "A 60-GHz 32-Way Hybrid Power Combination Power Amplifier in 55-nm Bulk CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 2, pp. 613-627, Feb. 2023.
- [52]. D. Pan et al., "A 77-GHz Power Amplifier with Digital Power Control for Multi-Mode Automotive Radar in 28-nm Bulk CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 3, pp. 875-879, March 2023.
- [53]. Y. Chang, Y. Wang, C. -N. Chen, Y. -C. Wu and H. Wang, "A V-Band Power Amplifier With 23.7-dBm Output Power, 22.1% PAE, and 29.7-dB Gain in 65-nm CMOS Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 11, pp. 4418-4426, Nov. 2019.
- [54]. H. T. Nguyen, D. Jung and H. Wang, "4.9 A 60GHz CMOS Power Amplifier with Cascaded Asymmetric Distributed-Active-Transformer Achieving Watt-Level Peak Output Power with 20.8% PAE and Supporting 2Gsym/s 64-QAM Modulation," in *2019 IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, 2019, pp. 90-92.
- [55]. S. V. Thyagarajan, A. M. Niknejad and C. D. Hull, "A 60 GHz Drain-Source Neutralized Wideband Linear Power Amplifier in 28 nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 8, pp. 2253-2262, Aug. 2014.
- [56]. D. Zhao and P. Reynaert, "A 60-GHz Dual-Mode Class AB Power Amplifier in 40-

- 
- nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2323-2337, Oct. 2013.
- [57]. V. -S. Trinh and J. -D. Park, "An 85-GHz Power Amplifier Utilizing a Transformer-Based Power Combiner Operating Beyond the Self-Resonance Frequency," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 3, pp. 882-891, March 2022.
- [58]. J. Ho and H. -W. Tsao, "CMOS Power Amplifier with Novel Transformer Power Combiner," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 7, pp. 2365-2369, July 2023.
- [59]. I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Distributed active transformer-a new power-combining and impedance-transformation technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 316-331, Jan. 2002.
- [60]. W. Zeng, L. Gao, N. Sun, H. Xu, Q. Xue and X. Zhang, "25.2 A 19.7-to-43.8GHz Power Amplifier with Broadband Linearization Technique in 28nm Bulk CMOS," in *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp. 372-374.
- [61]. M. Vigilante and P. Reynaert, "A Wideband Class-AB Power Amplifier With 29–57-GHz AM–PM Compensation in 0.9-V 28-nm Bulk CMOS," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1288-1301, May 2018.
- [62]. H. Jia, C. C. Prawoto, B. Chi, Z. Wang, and C. P. Yue, "A Full Ka-Band Power Amplifier With 32.9% PAE and 15.3-dBm Power in 65-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 9, pp. 2657-2668, Sept. 2018.
- [63]. A. Bevilacqua and A. Mazzanti, "Doubly-Tuned Transformer Networks: A Tutorial," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 2, pp. 550-555, Feb. 2021.
- [64]. C. Xing et al., "Analysis and Design of Broadband, Transformer Based Matching Network," in *2020 IEEE 15th International Conference on Solid-State & Integrated Circuit Technology (ICSICT)*, Kunming, China, 2020, pp. 1-4.
- [65]. H. Asada, K. Matsushita, K. Bunsen, K. Okada, and A. Matsuzawa, "A 60GHz CMOS power amplifier using capacitive cross-coupling neutralization with 16 % PAE," in *2011 6th European Microwave Integrated Circuit Conference*, Manchester, UK, 2011, pp. 554-557.
- [66]. M. Cui, J. Wagner, and F. Ellinger, "A Class-J/F 60 GHz Power Amplifier with 42.3% Power Added Efficiency in FDSOI CMOS," in *2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Washington, DC, USA, 2024, pp. 123-126.
- [67]. Y. Zhao and J. R. Long, "A Wideband, Dual-Path, Millimeter-Wave Power Amplifier With 20 dBm Output Power and PAE Above 15% in 130 nm SiGe-BiCMOS," *IEEE*

- Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 1981-1997, Sept. 2012.
- [68]. W. Zeng et al., "A Compact 19.7- to 43.8-GHz Power Amplifier With 20.3-dBm Psat and 35.5% PAE in 28-nm Bulk CMOS," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 8, pp. 2455-2468, Aug. 2024.
- [69]. F. Wang and H. Wang, "24.6 An Instantaneously Broadband Ultra-Compact Highly Linear PA with Compensated Distributed-Balun Output Network Achieving >17.8dBm P1dB and >36.6% PAEP1dB over 24 to 40GHz and Continuously Supporting 64-/256-QAM 5G NR Signals over 24 to 42GHz," in *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2020, pp. 372-374.
- [70]. L. Zhang et al., "A Compact 140-GHz Power Amplifier With 15.4-dBm Psat and 14.25% Peaking PAE in 28-nm Bulk CMOS Process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 5, pp. 3016-3030, May 2024.
- [71]. W. Zhang, Z. Lin, H. Tao and H. Meng, "A 2–18 GHz Dual-Mode GaN Power Amplifier Based on Distributed Structure," *IEEE Microwave and Wireless Technology Letters*, vol. 34, no. 6, pp. 651-654, June 2024, doi: 10.1109/LMWT.2024.3392153.
- [72]. Y. Zhang and K. Ma, "A 2–22 GHz CMOS Distributed Power Amplifier With Combined Artificial Transmission Lines," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 12, pp. 1122-1124, Dec. 2017, doi: 10.1109/LMWC.2017.2750416.
- [73]. C. -C. Lin, C. -H. Yu, H. -C. Kuo and H. -R. Chuang, "Design of 60-GHz 90-nm CMOS balanced power amplifier with miniaturized quadrature hybrids," in *2014 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*, Newport Beach, CA, USA, 2014, pp. 52-54, doi: 10.1109/PAWR.2014.6825723.
- [74]. G. Diverrez, E. Kerhervé and A. Cathelin, "A 24-31GHz 28nm FD-SOI CMOS Balanced Power Amplifier Robust to 3:1 VSWR for 5G Application," in *2022 52nd European Microwave Conference (EuMC)*, Milan, Italy, 2022, pp. 496-499, doi: 10.23919/EuMC54642.2022.9924331.
- [75]. G. Lee, J. Lee, J. Park and S. Hong, "A 24-30GHz Wideband Power Amplifier with High-Coupling-Coefficient Transmission Line Transformer and Staggered Tuning," in *2022 14th Global Symposium on Millimeter-Waves & Terahertz (GSMM)*, Seoul, Korea, Republic of, 2022, pp. 12-14, doi: 10.1109/GSMM53818.2022.9792329.
- [76]. B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2011.
- [77]. Z. -H. Fu, J. -W. Ye, H. Liang, and K. -Y. Lin, "Millimeter-Wave Wideband CMOS Power Amplifier Using Inductive-Compensation Distributed Active Transformer,"

- IEEE Transactions on Microwave Theory and Techniques*, doi:10.1109/TMTT.2024.3520211.
- [78]. M. Vigilante and P. Reynaert, *5G and E-Band Communication Circuits in Deep-Scaled CMOS*. Cham, Switzerland: Springer, 2018. doi: 10.1007/978-3-319-72646-5.
- [79]. H. S. Ruiz and R. B. Pérez, *Linear CMOS RF Power Amplifiers: A Complete Design Workflow*. New York, NY, USA: Springer, 2014. doi: 10.1007/978-1-4614-8657-2.
- [80]. A. Mazzanti, A. Bevilacqua, "On the phase noise performance of transformer-based CMOS differential-pair harmonic oscillators," *IEEE Trans. Circuits Syst I: Regular Pap*, 62(9), 2334–2341.
- [81]. A. Mazzanti and A. Bevilacqua, "Second-Order Equivalent Circuits for the Design of Doubly-Tuned Transformer Matching Networks," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 12, pp. 4157-4168, Dec. 2018, doi: 10.1109/TCSI.2018.2846029.

PUBLICATIONS LIST



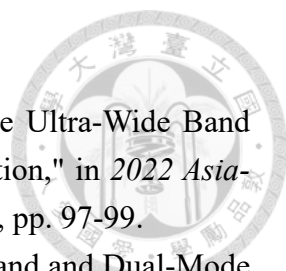
Journal Paper:

- [1]. **Z. -H. Fu**, M. -X. Li, T. -G. Ma, C. -S. Wu and K. -Y. Lin, "Millimeter-Wave GaAs Ultra-Wideband Medium Power Amplifier and Broadband High-Power Power Amplifier for 5G/6G Applications," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 14, no. 1, pp. 111-121, March 2024.
- [2]. S. -W. Wu, **Z. -H. Fu**, C. -S. Shen, K. -Y. Lin and S. -Y. Chen, "A beam-switching planar antenna module with 360° in-plane coverage for drone collision avoidance radar," *IEICE Transactions on Communications*, doi: 10.23919/transcom.2024EBP3076.
- [3]. **Z. -H. Fu**, J. -W. Ye, H. Liang, and K. -Y. Lin, "Millimeter-Wave Wideband CMOS Power Amplifier Using Inductive-Compensation Distributed Active Transformer," *IEEE Transactions on Microwave Theory and Techniques*, doi:10.1109/TMTT.2024.3520211.

Conference Paper:

- [4]. P. -W. Wu, J. -W. Ye, **Z. -H. Fu**, Y. -T. Chang and K. -Y. Lin, "A Wideband Bi-Directional Active Mixer for 5G Millimeter-Wave Applications," in *2024 IEEE/MTT-S International Microwave Symposium (IMS)*, Washington, DC, USA, 2024, pp. 170-173.
- [5]. Y. -S. Lai, **Z. -H. Fu**, J. -W. Ye, C. -S. Wu and K. -Y. Lin, "28 GHz GaAs pHEMT High-Efficiency Power Amplifier Using Multi-Section Transmission-Line Power Combining/Matching Technique," in *2024 IEEE/MTT-S International Microwave Symposium (IMS)*, Washington, DC, USA, 2024, pp. 827-830.
- [6]. Y. -S. Lai, J. -W. Yei, **Z. -H. Fu** and K. -Y. Lin, "A CMOS Low Noise Amplifier with Gm-boosting Technique for Multi-band 5G Systems," in *2023 Asia-Pacific Microwave Conference (APMC)*, Taipei, Taiwan, 2023, pp. 351-353.
- [7]. P. -W. Wu, J. -W. Yei, **Z. -H. Fu**, Y. -T. Chang and K. -Y. Lin, "A Wideband GaAs pHEMT LNA Multi-band 5G mmW Communication," in *2023 Asia-Pacific Microwave Conference (APMC)*, Taipei, Taiwan, 2023, pp. 348-350.
- [8]. C. -C. Chen, J. -W. Yei, **Z. -H. Fu** and K. -Y. Lin, "High-Power and Small-size CMOS T/R Switch Using Stacked Inductor," in *2023 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Cairns, Australia, 2023, pp. 32-34.
- [9]. W. -C. Lee, **Z. -H. Fu**, J. -W. Yei and K. -Y. Lin, "Wideband 5-bit Vector-sum Phase Shifter for 5G Millimeter-wave Applications," in *2023 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Cairns, Australia,

2023, pp. 35-37.

- 
- [10].B. -W. Huang, **Z. -H. Fu** and K. -Y. Lin, "A Millimeter-Wave Ultra-Wide Band Power Amplifier in 0.15- μ m GaAs pHEMT for 5G Communication," in *2022 Asia-Pacific Microwave Conference (APMC)*, Yokohama, Japan, 2022, pp. 97-99.
- [11].B. -W. Huang, **Z. -H. Fu** and K. -Y. Lin, "A 28/38 GHz Dual-Band and Dual-Mode CMOS Power Amplifier Using Constant Optimal Load Impedance Method," in *2022 Asia-Pacific Microwave Conference (APMC)*, Yokohama, Japan, 2022, pp. 100-102.
- [12].B. -W. Huang, **Z. -H. Fu** and K. -Y. Lin, "A 28/38 GHz Dual-Band and Dual-Mode CMOS Power Amplifier Using Constant Optimal Load Impedance Method," in *2022 Asia-Pacific Microwave Conference (APMC)*, Yokohama, Japan, 2022, pp. 100-102.
- [13].Y. -S. Lai, **Z. -H. Fu** and K. -Y. Lin, "Dual-input LNA for Switchable Dual-circular Polarization Satellite Receiver," in *2021 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Hualien, Taiwan, 2021, pp. 1-3.
- [14].Z. -J. Huang, **Z. -H. Fu**, B. -. W. Huang, Y. -T. Lin, K. -Y. Kao and K. -Y. Lin, "A Millimeter-Wave Dual-Band Class-F Power Amplifier in 90 nm CMOS," in *2020 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Hiroshima, Japan, 2020, pp. 70-72.