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雙延遲路徑的環型振盪器與多相位補償之除小數頻率合成器

The Design and Analysis of Dual-Delay Path Ring Oscillators and a Multiphase Compensation Method for Fractional-*N* Frequency Synthesizers

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本論文係陳兆人君（R94943109）在國立臺灣大學電子工程所完成之碩士學位論文，於民國 97 年 7 月 17 日承下列考試委員審查通過及口試及格，特此證明

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THESIS

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總算畢業了~~~! \^o^/ 能夠完成這篇論文，首先要感謝李泰成老師的指導。這三年來李泰成老師總以最專業嚴謹的態度指導我，使我在專業知識以及作研究的態度上都有長足的進步 <(_ _)> 。也誠摯的感謝曹恆偉教授、楊清淵教授、林宗賢教授，他們寶貴的建言使得這篇論文可以順利的完成。

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To My Family

摘要

環型振盪器(ring oscillators)和頻率合成器(frequency Synthesis)廣泛的被應用於許多通訊系統，比如時脈產生器(clock generator)或是迴路內之調變器(in-loop modulator)。此篇論文分別介紹了雙延遲路徑的環型振盪器(dual-delay path ring oscillators)以及多相位補償之除小數頻率合成器(multiphase compensation method for fractional-*N* frequency synthesizers)。

環型振盪器廣泛的被應用於時脈產生器或是頻率合成器當中。為了增加振盪頻率，雙延遲路徑的環型振盪器經常被使用以提升其最高振盪頻率。在四級雙延遲路徑的差動環型振盪器中(differential 4-stage dual-delay path ring oscillator)，被發現有兩種振盪模式，它們分別為：差動式振盪模式(differential mode oscillation)以及共模式振盪模式(common mode oscillation)。當振盪器運做於差動式振盪模式下時，延遲元件(delay cell)輸出差動波形(differential output waveforms)。而當振盪器運做於共模式振盪模式時，延遲元件則輸出同相位波形(in-phased output waveforms)。除此之外，兩種振盪模式之振盪頻率也不同。這樣的情形會造成時脈產生器或是頻率合成器無法正常運作。為了對雙延遲路徑的環型振盪器有更深入的了解，我們用數學分析推導以及實作量測來解析四級雙延遲路徑的差動環型振盪器的兩種振盪模式。此四級雙延遲路徑的差動環型振盪器佔用了 $58 \times 41\mu m^2$ 之晶片面積，實現在 0.18 μm CMOS 製程中。在差動式振盪模式下，所量測的輸出頻率範圍為 1.77 GHz ~ 1.92 GHz，並且消耗 13 mW 及使用 1.8 V 之供給電壓。而在共模式振盪模式下，所量測的輸出頻率範圍為 1.01 GHz ~ 1.055 GHz，並且消耗 10 mW 及使用 1.8 V 之供給電壓。

具有高效能之頻率合成器在許多通訊系統中，比如 WCDM 之傳輸接收器(transceivers)或迴路內調變器，扮演著重要的角色。在本篇論文當中提出了一多相位補償之除小數頻率合成器。為了改善電路元件中因不匹配而產生之非理想效應，提出了一延遲線路(delay line)和一包含了動態器件匹配技術(dynamic element matching technique)和再量化之三角積分調變器(re-quantized Σ-Δ modulator)的數位控制電路(digital control circuit)。此多相位補償之除小數頻率合成器操作在 2.11 GHz 到 2.17 GHz 之時脈，佔用了 0.92 × 1.15 mm^2 之晶片面積，實現在 0.18 μm CMOS 製程中。在所提出之架構中，於距離 2.14-GHz 輸出 10-MHz 頻帶處的量化誤差消減了 10 dB。所須鎖定時間少於 25 μsec。

關鍵字: CMOS RF、環型振盪器、三角積分調變器、除小數頻率合成器、鎖相迴路、除頻器、相位雜訊、量化誤差消減、WCDMA。

Abstract

Ring oscillators and frequency synthesis are widely employed in communication systems, such as clock generators or in-loop modulators. In this thesis, a dual-delay path ring oscillator and a multiphase compensation method for fractional-*N* frequency synthesizer are covered.

Ring oscillators are widely used in clock generators and frequency synthesis. To increase the oscillation frequencies, dual-delay path ring oscillators are often implemented to explore the maximum frequency levels. Two oscillation modes have been found in differential four-stage dual-delay path ring oscillators, one named differential mode oscillation and the other named common mode oscillation. In differential mode oscillation, a single delay cell contains differential output waveforms, but in common mode, the output waveforms are in-phased. In addition, the oscillation frequencies of the two oscillation modes are not the same either. These problems might spoil the function of the clock generators and frequency synthesis. For more insight of dual-path ring oscillators, mathematical analysis and

demonstrations including the two oscillation mode in a differential four-stage dual-delay path ring oscillator is presented. A differential four-stage dual-delay path ring oscillator is fabricated in a 0.18-μm CMOS technology with an active area of 58×41 μm^2. The measured tuning range is from 1.77 GHz to 1.92 GHz in differential mode oscillation which consumes 13 mW from a 1.8-V power supply, and from 1.01 GHz to 1.055 GHz in common mode oscillation that consumes 10 mW from a 1.8-V power supply.

High performance frequency synthesis is required in communication systems such as WCDMA transceivers or in-loop modulation systems. In this thesis, a Σ-Δ fractional-*N* frequency synthesizer with a multiphase compensation method is proposed. To resolve the problem brought by nonidea effect such as delay unit mismatch and gain error, a proposed delay line structure and a digital control circuit including dynamic element matching techniques and a re-quantized Σ-Δ modulator is presented. A frequency synthesizer operating from 2.11 GHz to 2.17 GHz, is fabricated in a 0.18-μm CMOS technology with an area of 0.92×1.15 mm^2. Power consumption is 27.2 mW from 1.8-V power supply. The proposed architecture suppresses the quantization noise of a 2.4-GHz output at 10-MHz frequency offset by 10 dB. The settling time is less than 25 μsec.

Keywords: CMOS RF, ring oscillator, delta-sigma modulator, fractional-N frequency synthesizers, phase-locked loop (PLL), frequency dividers, phase noise, quantization noise suppression, WCDMA.

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Chapter 1

Introduction

1.1 Motivation and Research Goals

The rapid growth of network communication has greatly increased the demand for low-cost and high-performance systems in recent years. Ring oscillators have been widely employed in clock generators and frequency synthesis for their small die size and multiphase outputs. To increase the oscillation frequencies, dual-delay path ring oscillators are often implemented to explore the maximum frequency levels. However, there are two oscillation modes in four-stage dual-delay path ring oscillators, which might spoil the function of the clock generators and frequency synthesis. For more insight of dual-path ring oscillators, mathematical analysis and demonstrations including the two oscillation mode in a four-stage dual-delay path ring oscillator is presented.

High performance frequency synthesis that requires high-loop bandwidth and low output

phase noise, low spurious tones are demanded by many systems, such as WCDMA transceivers or in-loop modulation systems. Although, Σ-Δ fractional-*N* frequency synthesis resolves the trade-off between loop bandwidth and input reference frequency, the high-pass quantization noise still limits the performance. Further, quantization noise suppression methods such as multiphase compensation or DAC compensation causes in-band noise and spurious tones due to nonideal element mismatch. To overcome these problems, a multiphase compensation method with dynamic element matching technique in a Σ-Δ fractional-*N* frequency synthesizer is proposed.

1.2 Thesis Overview

This thesis is divided into five chapters. In Chapter 2, an overview of conventional ring oscillators is introduced, including the small-signal linear model approximation of ring oscillators and the criterion of oscillation. Further, a linear model of fractional-*N* frequency synthesis and a brief introduction of the concept of quantization noise suppression are also given in this chapter.

A dual-delay path ring oscillator is presented in Chapter 3. The oscillation frequency increment due to additional-delay paths in ring oscillators is firstly derived. Further, the

two oscillation mode in differential four-stage dual-delay path ring oscillators is analyzed and demonstrated.

Chapter 4 interprets the architecture of the proposed Σ-Δ fractional-*N* frequency synthesizer. Basic concept about the multiphase compensation method is firstly provided. Nonideality about the multiphase element mismatch is also discussed. To solve the nonideal effects, a delay line structure and digital control circuit with dynamic element matching technique are proposed. Behavioral model and analysis are also given. Experimental results are provided in the end of this chapter

Finally, conclusions of this work are drawn in Chapter 5.

Chapter 2

Basic Concepts

This chapter introduces an overview of ring oscillators and Σ-Δ fractional-*N* frequency synthesizers, including multi-stage noise shaping (MASH) Σ-Δ modulators, a linear model for fractional-*N* frequency synthesizers and the concept of quantization noise suppression.

2.1 Ring Oscillators

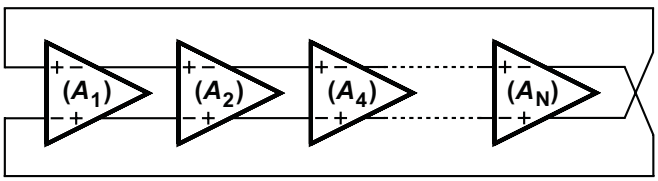


Figure 2.1 A conventional differential *N*-stage ring oscillator

Figure 2.1 shows a conventional differential *N*-stage ring oscillator, a ring oscillator consists of a number of gain stages in a loop. The oscillation frequency is determined as $1/(2NT_d)$, where N is the number of stages and T_d is the large signal delay time of a delay

cell.

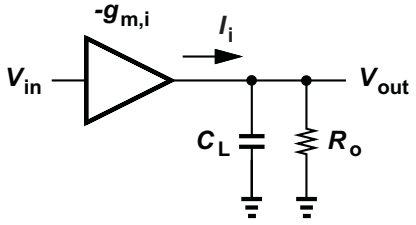


Figure 2.2 Half circuit small-signal model of a delay cell.

Figure 2.2 shows the half circuit small-signal linear model approximation of a single-delay cell in figure 2.1. V_{in} and V_{out} are the input and output signals, respectively. $g_{m,i}$ represents the transconductance of the input device, I_i is the output current of the input device which flows through the loadings C_L and R_o, where C_L and R_o represents the total capacitance and the equivalent resistance at the output node, respectively. The transfer function $H(j\omega)$ between V_{in} and V_{out} of a delay cell can be derived as

$$H(j\omega) = \frac{V_{out}}{V_{in}} = - g_{m,i} \cdot \frac{R_o}{1+j\omega R_o C_L}, \tag{2.1}$$

and

$$\angle H(j\omega) = - \pi - tan^{-1}(\omega R_o C_L). \tag{2.2}$$

According to Barkhausen criterion of oscillation [1], the ring oscillator would oscillate if open loop has unity voltage gain, i.e.,

$$\left|H(j\omega)\right|^N = 1 \Rightarrow \left(\frac{g_{m,i} \cdot R_o}{\sqrt{1+(\omega R_o C_L)^2}} \right)^N = 1, \tag{2.3}$$

and have a phase shift of 2π or a multiple of 2π. For a *N*-stage ring oscillator in a stable oscillation state, each stage contributes a same amount of phase shift. Furthermore, let $-(\pi+\phi)$ represent the phase shift of a single stage (2.2), the total phase shift around the loop will be $-(\pi+\phi)N = -2n\pi$ if *N* is an odd number, or $-(\pi+\phi)N-\pi = -2n\pi$ if *N* is even, where *n* is a positive integer. Thus

$$\phi = tan^{-1}(\omega_{osc} R_o C_L) = \frac{\pi}{N}. \tag{2.4}$$

Therefore, the oscillation frequency can be expressed as

$$\omega_{osc} = \frac{tan(\frac{\pi}{N})}{R_o C_L}. \tag{2.5}$$

By combing (2.3) and (2.5), the criterion for oscillation can be rewritten as

$$g_{m,i} \cdot R_o = sec\left(\frac{\pi}{N}\right) \tag{2.6}$$

In summary, a N-stage ring oscillator must satisfy the conditions in (2.4) and (2.3), and the oscillation frequency will be as derived in (2.5). If the number of stages in the ring increases the oscillation frequency decreases, shown in (2.5). It should be noted, the derivation so far is a first-order linear approach. In real circuits, as the oscillation amplitude increases the oscillator leaves its linear region and becomes a nonlinear system. Since the equivalent output resistance, loading capacitance and the transconductance all varies during transient, the oscillation frequency no longer matches equation (2.5) but equals to the large-signal value $1/(2NT_d)$. However, rather than the absolute oscillation frequency, we can capture the tendency of oscillation frequency with respect to N, R_o and C_L in real circuits.

2.2 Σ-Δ Fractional-*N* Frequency Synthesizers

2.2.1 Multi-Stage Noise Shaping (MASH) Σ-Δ Modulators

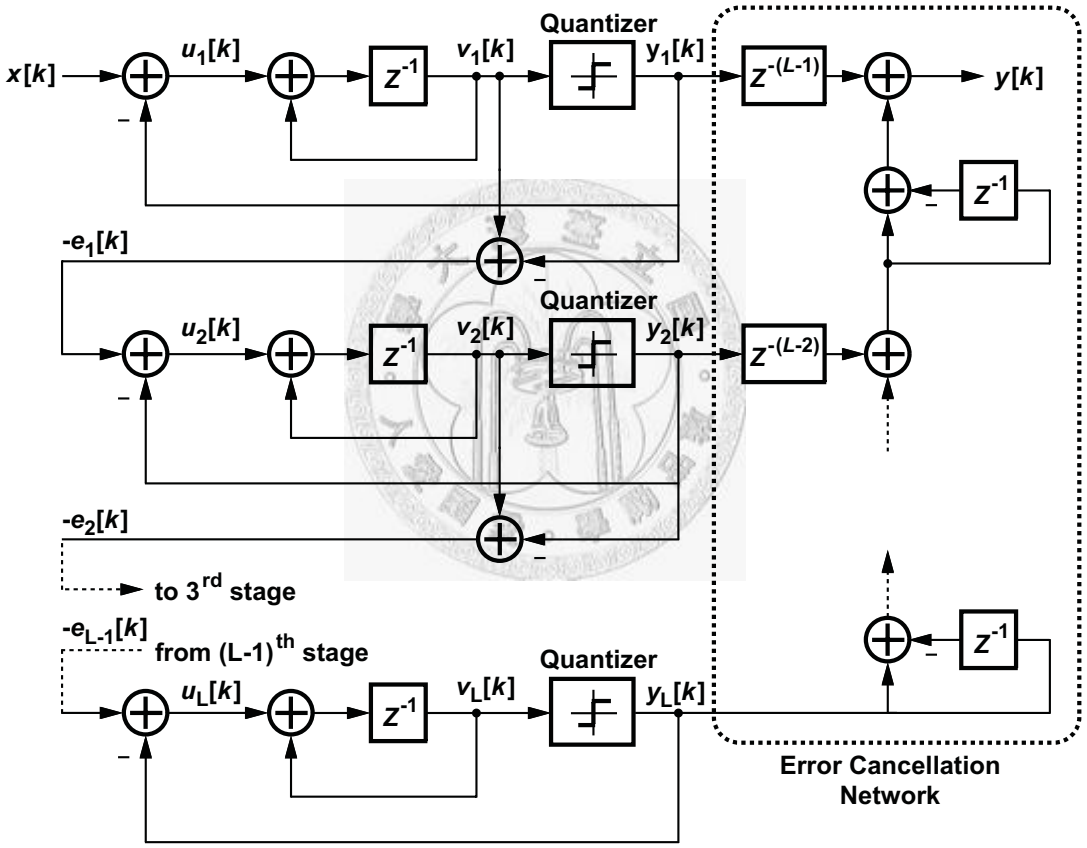


Figure 2.3 A high-order MASH Σ-Δ modulator.

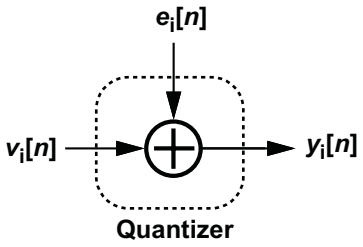


Figure 2.4 Equivalent model of a quantizer.

Recently, fully digital Σ-Δ modulators have become the main building blocks in Σ-Δ fractional-*N* frequency synthesizers for divider control. Σ-Δ modulators can be classified into two main categories [2] [3]. One of them is single-loop type Σ-Δ modulators, and the other is multi-stage noise shaping Σ-Δ modulators or MASH. MASH structure enables higher-order modulators without reducing the dynamic range, while in single loop type modulators, higher-order modulators requires careful design on signal condition around the loop for stability consideration, which in turn reduces the input dynamic range. Figure 2.3 shows an example of a L^{th}-order MASH structure [4]. The input and output signals are represented by *x[k]* and *y[k]*, respectively. $u_i[k]$, $v_i[k]$ and $y_i[k]$ are the intermediate node signals. In figure 2.4, shows an equivalent linear model of the quantizers in figure 2.3. Quatizaers are now represented as the addition of $v_i[k]$ with an error term $e_i[k]$, where $e_i[k]$ represents the error sequence by quantization. Now, from figure 2.3, the output signal *y[k]* can be derived as

$$\begin{aligned} y(z) &= x(z)\cdot z^{-L} + e_1(z)\cdot(1-z^{-1})\cdot z^{-(L-1)} + (-e_1(z)\cdot z^{-1} + e_2(z)\cdot(1-z^{-1}))\cdot z^{-(L-2)}\cdot(1-z^{-1}) + \cdots \\ &\quad \cdots + (-e_{L-1}(z)\cdot z^{-1} + e_L(z)\cdot(1-z^{-1}))\cdot(1-z^{-1})^{L-1} \\ &= x(z)\cdot z^{-L} + e_L(z)\cdot(1-z^{-1})^L \\ &= x(z)\cdot H_s(z) + e_L(z)\cdot H_n(z) \end{aligned}, \quad (2.6)$$

$H_s(z)$ and $H_n(z)$ represents the signal transfer function (STF) and noise transfer function (NTF), respectively. From (2.6), since $H_s(z)$ equals to unity, the output signal is shown to contain the input signal plus an error term. The output error term is the quantization error $e_L(z)$ shaped by the filter $(1-z^{-1})^L$. By assigning $q(z)=e_L(z)H_n(z)$, the power spectrum density of the output quantization noise S_q can be derived

$$S_q(f) = S_{e_L}(f)\cdot\left|(1-e^{-j2\pi fT})^L\right|^2 = S_{e_L}(f)\cdot(2\sin(\pi fT))^{2L}. \quad (2.7)$$

if the πf is small and $1 << T$, (2.7) can be further written as

$$\begin{aligned} S_q(f) &= S_{e_L}(f)\cdot(2\pi fT)^{2L} \\ &= 20\cdot L\cdot\log_{10}2\pi Tf + 10\cdot\log_{10}S_{e_L}(f) \end{aligned}. \quad (2.8)$$

Several assumptions were made about the quantization error e_L [4]. Ideally, e_L is white and uniformly distributed between 0 and 1, and can be modeled as an additive white noise with magnitude 1/12. Thus the power spectrum density of e_L can be described as

$$S_{e_L}(e^{j2\pi fT}) = \frac{1}{12}\cdot \tag{2.9}$$

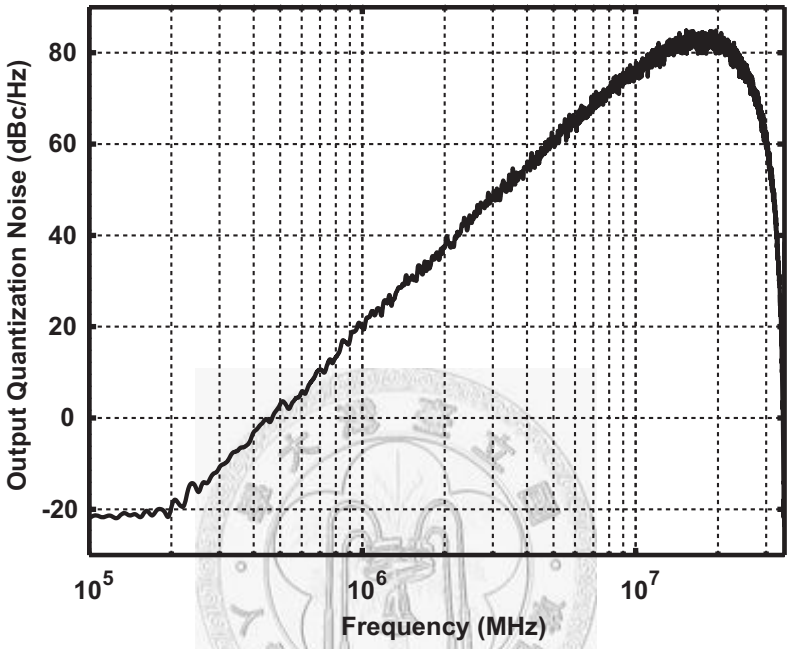


Figure 2.5 Output quantization noise of a 3rd-order MASH 1-1-1.

From (2.8) and (2.9), the output quantization noise *q(z)* is found to have of a 20L dB/decade slope in spectrum at low offset frequencies. In figure 2.5, shows the simulation results of the output quantization noise spectrum S_q of a 3rd-order MASH 1-1-1 modulator, with dc input and T = 28.6 nsec (inverse of 35 MHz). A 60 dB/decade noise increment can be clearly observed. The simulation is executed in a behavioral model implemented in CPPsim [5].

2.2.2 A Linear Model for Fractional-*N* Frequency Synthesizers

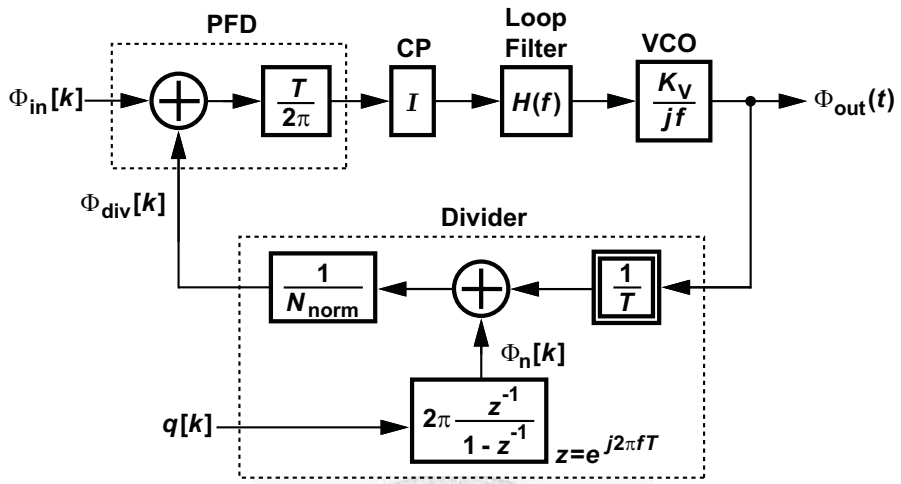


Figure 2.6 A linear model for fractional-*N* frequency synthesizers.

Traditional models of PLL analysis assumes a static divide value, which is not straightforward for fractional-*N* synthesizers since their divide value dynamically changes according to the output of Σ-Δ modulators. In [6], a linear model for fraction-*N* synthesizer especially Σ-Δ types has been analyzed and demonstrated, shown in figure 2.6. Effect of quantization noise as well as the influence of various noise sources on the frequency synthesizer phase noise can be analyzed by this linear model.

In figure 2.6, *T*, *I* and K_{vco} represents the period of the input reference clock, the gain of the charge pump and the gain of the voltage control oscillator (VCO), respectively. *H(f)* is the loop filter constructed of either passive or active devices. Further, $\Phi_{out}(t)$ represents the

phase deviation at the frequency synthesizer output. To be noted, this is not the exact phase of the output, which is

$$2\pi \cdot f_{\text{nom}} \cdot t + \Phi_{\text{out}}(t). \tag{2.10}$$

In further discussions the nominal phase $2\pi f_{\text{nom}}t$ will not be included, since it is the phase deviation that we are interested in. Furthermore, with considering the sampling characteristic of the divider, $\Phi_{\text{div}}[k]$ represents the phase deviation of the divider output. Similarly, $\Phi_{\text{in}}[k]$ represents the phase deviation of the input reference clock which equals to $\Phi_{\text{in}}(kT)$. Moreover, $q[k]$ represents the output quantization noise produced by the Σ-Δ modulator that causes incremental change in the frequency of the divider output

$$f_{\text{div}} = \frac{f_{\text{vco}}}{N[k]} = \frac{f_{\text{vco}}}{N_{\text{nom}} + q[k]}, \tag{2.11}$$

$N[k]$ is the division value of the divider, and N_{nom} is the nominal division value [6]. f_{vco} and f_{div} represents the out frequency of VCO and divider, respectively. By integrating $q[k]$ results to the phase deviation value $\Phi_{\text{n}}[k]$ caused by output quantization noise. Indicated in figure 2.6, the operation of the divider, on one hand samples the continuous-time signal $\Phi_{\text{out}}(t)$, and on the other hand integrates the output quantization noise $q[k]$ of Σ-Δ

modulator. Then by adding the sampled value with the integrator output together and divide by N_{nom}, results to the feedback signal $\Phi_{div}[k]$. Finally by figure 2.6 the open-loop transfer function *A(f)* can be expressed as

$$A(f)=\frac{\Phi_{div}}{\Phi_{ref}}=\left(\frac{1}{2\pi}\right)I\cdot H(s)\left(\frac{K_{VCO}}{jf}\right)\left(\frac{1}{N_{nom}}\right). \tag{2.12}$$

Since there is a *jf* term in the denominator of *A(f)*, it has a low pass nature with infinite gain at dc. With (2.12) the closed-loop transfer function *G(s)* can be written as

$$G(f)=\frac{\Phi_{out}}{\Phi_{ref}}=\frac{A(f)}{1+A(f)}. \tag{2.13}$$

G(f) equals to 1 at dc and approximates 0 as frequency increase infinitely, this implies that *G(f)* is a low-pass filter.

2.2.3 Effect of Various Noise Sources in Frequency Synthesizers

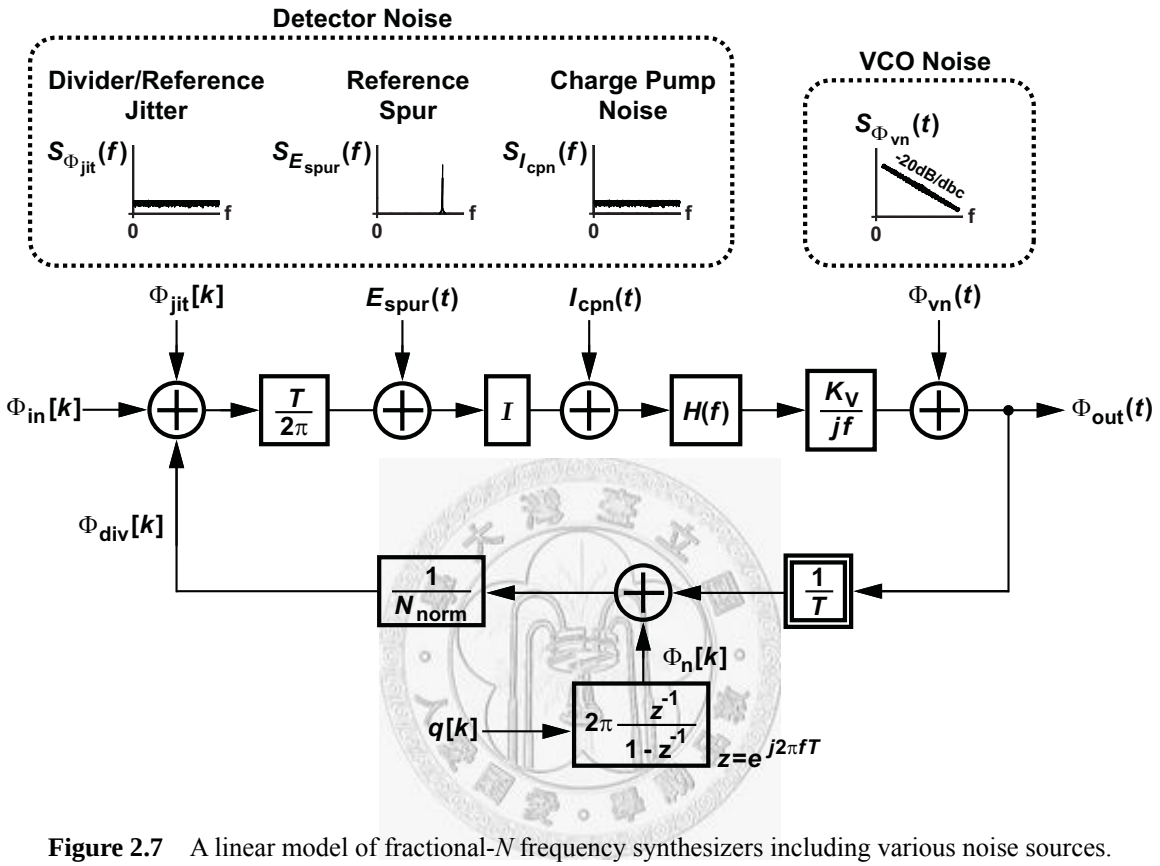


Figure 2.7 A linear model of fractional-*N* frequency synthesizers including various noise sources.

Indicated in figure 2.7, besides quantization noise there are other noise sources in a PLL based frequency synthesizers such like divider/reference jitter, $\Phi_{jit}[k]$ corresponds to noise-induced variations in the transition time of the input reference clock or divider output signal. Periodic reference spur, $E_{spur}(t)$ caused by current mismatch in charge pump or other affect such as charge injection and charge sharing. Charge pump noise, $I_{cp}(t)$ induced by the transistors that construct the charge pump circuit. Finally, VCO noise, $\Phi_{vn}(t)$

caused by intrinsic noise of the VCO and voltage noise at the output of the loop filter.

As shown in figure 2.7, the noise sources have been lumped up into two categories, VCO noise and detector noise. This comes from the reason that divider/reference jitter, reference spur and charge pump noise all interacts with a low pass filter to the frequency synthesizer output. On the contrary VCO noise interacts with a high pass filter to the frequency synthesizer output.

From (2.13) and figure 2.7, the detector noise, VCO noise and their effect on the frequency synthesizer output can be derived as follow

$$S_{\Phi_{out}}(f)\Big|_{\text{Detector Noise}} = S_{\Phi_{out}}(f)\Big|_{\text{Divider/Reference jitter}} + S_{\Phi_{out}}(f)\Big|_{\text{Reference Spurs}} + S_{\Phi_{out}}(f)\Big|_{\text{Charge Pump}}, \quad (2.14)$$

where

$$\begin{cases} S_{\Phi_{out}}(f)\Big|_{\text{Divider/Reference Jitter}} = \left|T \cdot N_{\text{nom}} \cdot G(f)\right|^2 S_{\Phi_{jit}}(f) \\ S_{\Phi_{out}}(f)\Big|_{\text{Reference Spurs}} = \left|2\pi \cdot N_{\text{nom}} \cdot G(f)\right|^2 S_{E_{spur}}(f) \\ S_{\Phi_{out}}(f)\Big|_{\text{Charge Pump}} = \left|\frac{2\pi N_{\text{nom}}}{I} \cdot G(f)\right|^2 S_{I_{cpn}}(f) \end{cases}. \quad (2.15)$$

and

$$S_{\Phi_{out}}(f)\Big|_{\text{VCO Noise}} = \left|1 - G(f)\right|^2 S_{\Phi_{vn}}(f). \tag{2.16}$$

Further, from (2.7), (2.13) and figure 2.7, the effect of Σ-Δ modulator output quantization noise on the frequency synthesizer output can be obtained as

$$\begin{aligned} S_{\Phi_{out}}(f)\Big|_{\text{Quantization Noise}} &= \frac{1}{T}\cdot\left|T\cdot G(f)\right|^2\left|2\pi\frac{e^{-j2\pi fT}}{1-e^{-j2\pi fT}}\right|^2 S_q(f) \\ &= \frac{1}{T}\cdot\left|T\cdot G(f)\right|^2\cdot(2\pi)^2\cdot\left(2sin(\pi fT)\right)^{2(L-1)} S_{e_L}(f) \end{aligned} \tag{2.17}$$

Shown in (2.17), the effect of output quantization noise of an L^{th}-order Σ-Δ modulator on the synthesizer output reduces in order by one. This come form the integrating operation of divider. Finally, the total output noise can be derived by summing up (2.14), (2.16) and (2.17)

$$S_{\Phi_{out}}(f)\Big|_{\text{Total Noise}} = S_{\Phi_{out}}(f)\Big|_{\text{Detector Noise}} + S_{\Phi_{out}}(f)\Big|_{\text{VCO Noise}} + S_{\Phi_{out}}(f)\Big|_{\text{Quantization Noise}}. \tag{2.18}$$

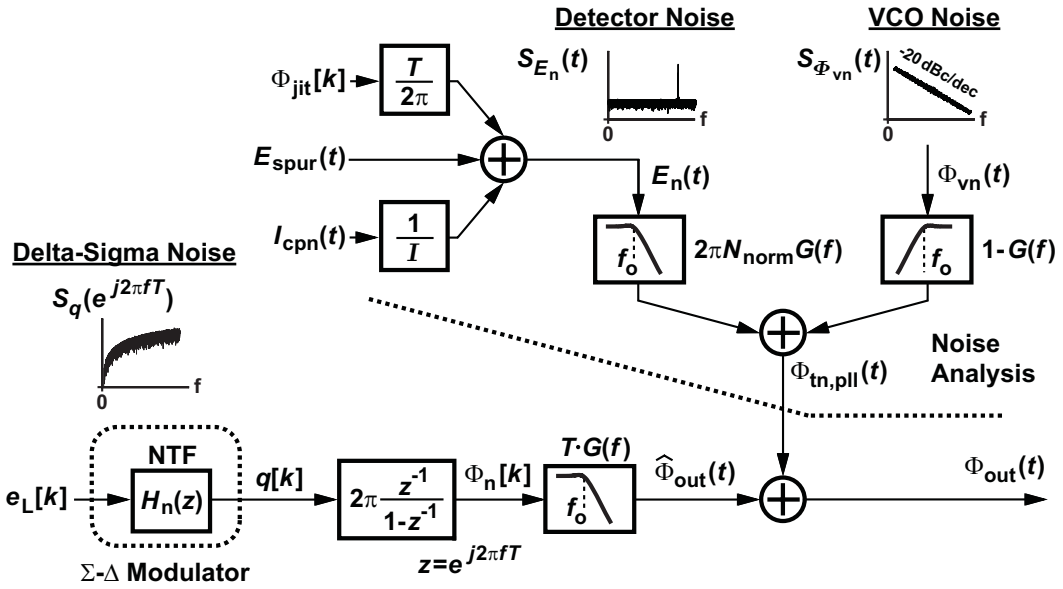


Figure 2.8 A parameterized model of a Σ-Δ synthesizer.

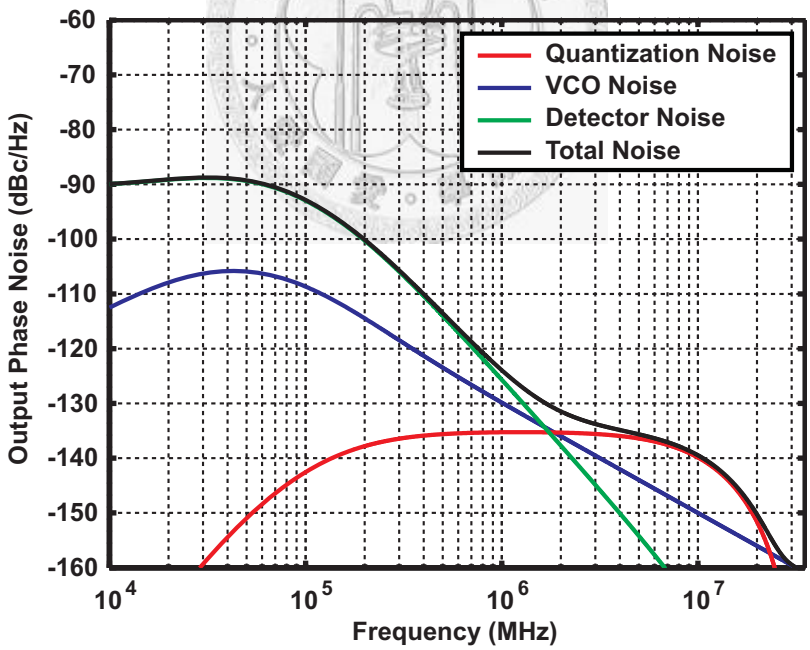


Figure 2.9 Output phase noise of a frequency synthesizer.

Figure 2.8 shows a parameterized model of Σ-Δ fractional-*N* frequency synthesizers,

including quantization noise, VCO phase noise and detector noise and their effect on the frequency synthesizer phase noise performance. With the aid of various noise spectrum derived earlier, figure 2.9 shows an example of a frequency synthesizer output phase noise diagram. A frequency synthesizer with 70 kHz bandwidth and 35 MHz input reference clock is examined. In figure 2.9, the blue line represents the impact of VCO noise at the synthesizer output, by modeling VCO noise as a -20 dB/decade slope curve with a spot noise of -130 dBc/Hz at 1 MHz offset frequency. The actual VCO deviates from the -20 dB/decade rolloff at low frequencies due to 1/f noise, and at high frequencies due to a finite noise source. The green line represents the detector noises, in this example reference spurs is neglected and the detector noise is modeled as a -90 dBc white noise. As mentioned before the detector noise interacts with a low pass filter before reaching the synthesizer output. Shown in figure 2.9, the influence of detector noises dominates at low offset frequencies, and the influence of VCO and quantization noise dominates at high offset frequencies.

2.2.4 Concept of Quantization Noise Compensation

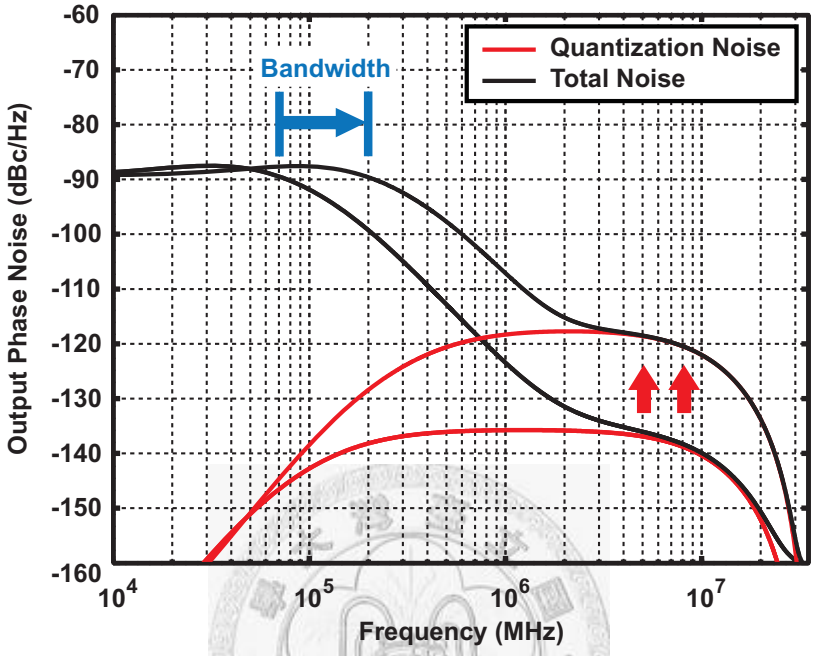


Figure 2.10 Quantization noise increment due to increased bandwidth.

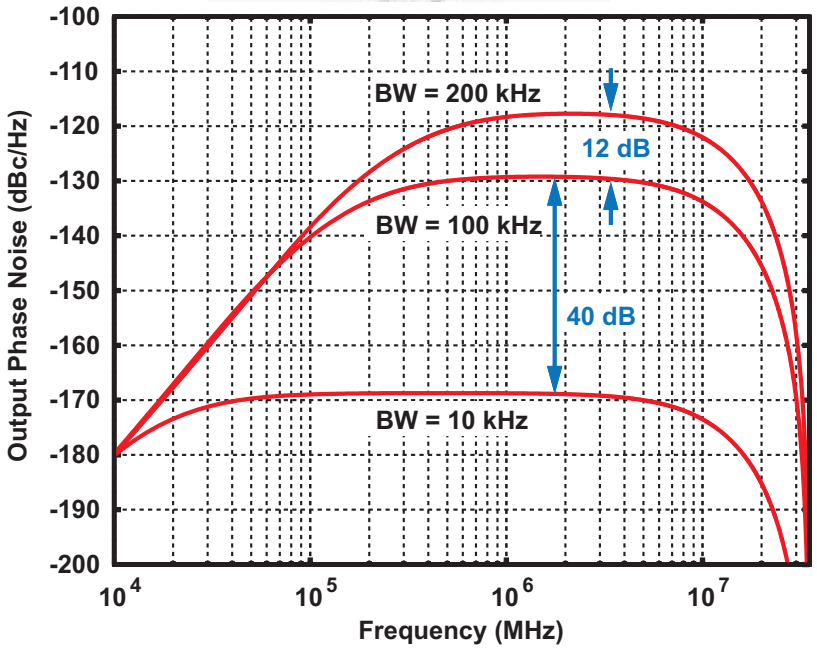


Figure 2.11 Synthesizer output quantization noise with BW=10 kHz, BW=100 kHz and BW=200 kHz.

Figure 2.10 shows an example of the effect of 3^{rd}-order MASH modulator output quantization noise on frequency synthesizer output phase noise, while increasing the loop bandwidth of frequency synthesizer. The input reference clock is 35 MHz, VCO noise model and detector noise model are the same as those applied in figure 2.9. As shown in figure 2.10, the quantization noise increases with a 40 dB/decade slope at low offset frequencies. With an increment in bandwidth from 70 kHz to 200 kHz which is about 0.45 decade, causes an increment in quantization noise of about 0.45 (decade) $\times$ 40 (dB/decade) = 18dB. Moreover, in frequency synthesizers that utilizes 2^{nd}-order MASH modulator, the quantization noise increases with a 20 dB/decade slope at low offset frequencies on the synthesizer output. Thus, increasing bandwidth from 70 kHz to 200 kHz, causes quantization noise to rise of about 0.45 (decade) $\times$ 20 (dB/decade) = 9 dB. Note in figure 2.10, only the quantization noise and the total noise curves are depicted, detector noise and VCO noise are not shown for clearance. Figure 2.11 shows the effect of quantization noise on frequency synthesizer output with difference loop bandwidths.

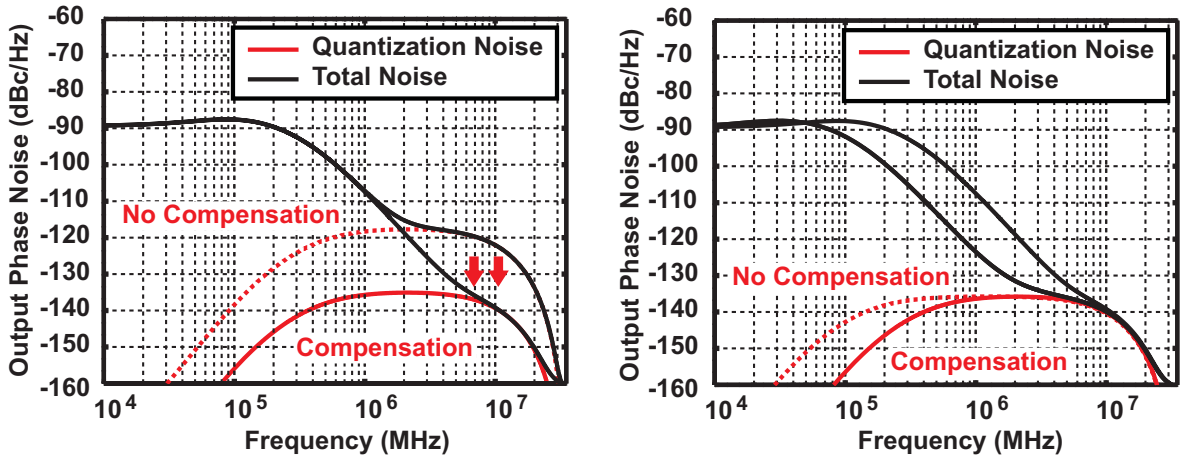


Figure 2.12 (a) Quantization noise reduction due to compensation. (b) Comparison between low bandwidth synthesizer and high bandwidth synthesizer with quantization noise compensation method.

In applications such as WCDMA or in-loop modulation systems that require large-loop bandwidth frequency synthesizers, the quantization noise might spoil the phase noise performance at high offset frequencies. For this reason, several researches have been reported to compensate the quantization noise [7]-[14]. Figure 2.12(a) shows an example of ideally reducing quantization noise due to DAC or multiphase compensation methods. As indicated in figure 2.12(b), an 18 dB reduction on quantization noise, enables the loop bandwidth to increase from 70 kHz to 200 kHz, without spoiling phase noise performance at high offset frequencies. However, nonideal effect such as element mismatch in the compensation circuit causes in-band noise and spurious tones. To overcome these problems, a multiphase compensation Σ-Δ fractional-*N* frequency synthesizer with

dynamic element matching (DEM) techniques for mismatch linearization is proposed in chapter 4.

Chapter 3

The Design and Analysis of Dual-Delay Path Ring Oscillators

This chapter introduces the design and analysis of dual-delay path ring oscillators. With mathematical analysis, the oscillation frequency increment due to additional-delay paths is derived. Further, the two oscillation mode in differential four-stage dual-delay path ring oscillators is analyzed and demonstrated.

3.1 Introduction

Ring oscillators have been widely employed in most of clock generators and frequency synthesis for their useful features such as small die size, multiphase outputs, as well as easy integration in a standard CMOS process. Because the oscillation frequency of ring oscillators is determined by the propagation delay time of each delay cells, single-loop ring oscillators lack for high oscillation frequency. Several techniques have been reported to

explore the maximum frequency levels of ring oscillators, such as sub-feedback loops [15], output-interpolation methods [16], multiple-feedback loops [17] and dual-delay paths [18]-[20].

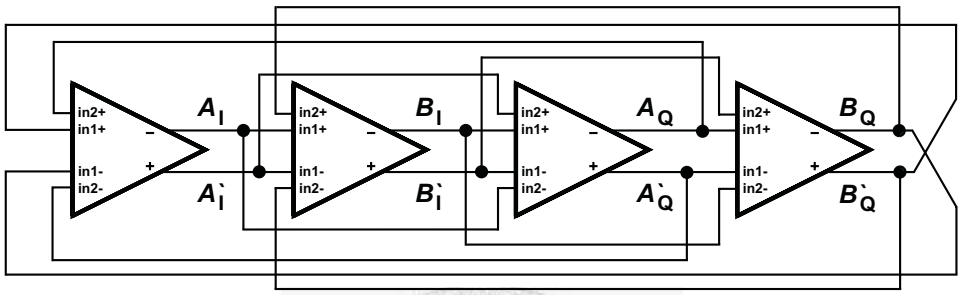
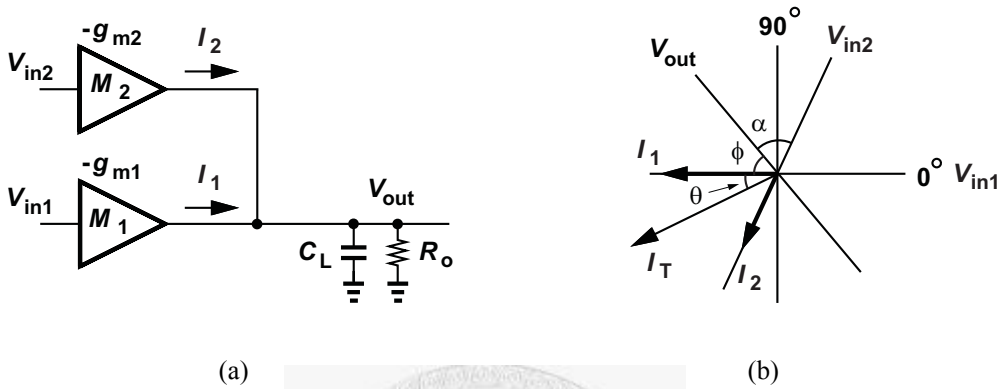


Figure 3.1 A differential four-stage dual-delay path ring oscillator.

In this work, a differential four-stage dual-delay path ring oscillator, in figure 3.1, was implemented for its high oscillation frequencies and its improvement of phase noise performance. However, there happens to be two operation modes in the oscillator, named differential-mode oscillation and common-mode oscillation. The initial conditions affect the operation of the dual-delay path ring oscillator. The main difference of the two operation modes is the output waveform characteristic. Instead of typical differential output signals, the outputs of a delay cell becomes in-phased. Furthermore, the oscillation frequency in either mode is different.

3.2 Oscillation Frequency in Multiple-Delay Path Ring Oscillators



(a) (b)

Figure 3.2 (a) Half circuit small-signal model of a dual-delay path delay cell. (b) The phasor diagram of the signals V_{in1}, V_{in2}, V_{out} and currents I_1, I_2.

Figure 3.2(a) shows the half circuit small-signal model of a delay cell in dual-delay path ring oscillators. Dual-delay path means both the additional-delay path and the main-delay path exits in the same ring oscillator. The additional-delay path should be introduced in a way which decreases the delay time of a single delay cell, as a result the oscillation frequency increases. The inverters M_1 and M_2 are the input devices of the main-delay path signal V_{in1} and the additional-delay path signal V_{in2}, respectively. g_{m1} and g_{m2} represent the transconductance of the inverters M_1 and M_2, respectively. C_L and R_o represent the total loading capacitance and the equivalent output resistance at the output node, respectively. I_1

and I_2 are the output currents of the inverters M_1 and M_2, respectively. The phasor diagram of the voltage signals V_{in1}, V_{in2}, V_{out} and currents I_1, I_5 in a stable oscillation state is illustrated in figure 3.2(b) [21]. The phase of V_{in1} is set as zero for the reference. The phase of V_{out} with respect to V_{in1} is $-(\pi+\phi)$, where $\phi=\pi/N$ in a N-stage ring oscillator. The phase of V_{in2} with respect to V_{out} is α. I_T is the vector summation of I_1 and I_2. The resultant phase of I_T yields θ degree phase difference with respect to I_1 and is indicated in figure 3.2(b).

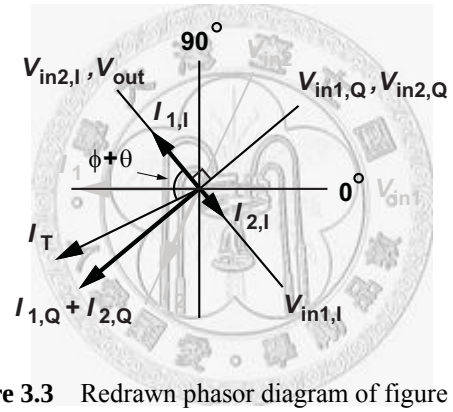


Figure 3.3 Redrawn phasor diagram of figure 3.2(b).

Figure 3.3 is the redrawn phasor diagram of figure 3.2(b). The main-delay path signal V_{in1} is splitted into two signal components $V_{in1,I}$ and $V_{in1,Q}$, where $V_{in1,I}$ is in parallel with V_{out} and in orthogonal to $V_{in1,Q}$. The relation of $V_{in1,I}$ and $V_{in1,Q}$ with respect to V_{in1} can be expressed as

$$\begin{cases} V_{in1,I} = V_{in1} \cdot e^{-j\phi} \cdot cos\phi \\ V_{in1,Q} = V_{in1} \cdot e^{j(\pi/2-\phi)} \cdot sin\phi \end{cases}. \tag{3.1}$$

Similarly, the additional-delay path signal V_{in2} is also splitted into two signal components $V_{in2,I}$ and $V_{in2,Q}$, where $V_{in2,I}$ is in parallel with V_{out} and in orthogonal to $V_{in2,Q}$. The relation of $V_{in2,I}$ and $V_{in2,Q}$ with respect to V_{in2} can be expressed as

$$\begin{cases} V_{in2,I} = V_{in2} \cdot e^{j\alpha} \cdot cos\alpha \\ V_{in2,Q} = V_{in1} \cdot e^{-j(\pi/2-\alpha)} \cdot sin\alpha \end{cases}. \tag{3.2}$$

The transfer function $H(j\omega)$ between V_{in1} and V_{out} of a single stage delay cell can be found as follows. The output signal V_{out} can be described as

$$V_{out} = I_T \cdot (R_o // C_L), \tag{3.3}$$

where $(R_o//C_L)$ is the output node loading. The equivalent output current I_T can be derived as

$$\begin{aligned} I_T &= I_1 + I_2 \\ &= -V_{in1} \cdot \sqrt{g_{m1}^2 + g_{m2}^2 + 2g_{m1}g_{m2}cos(\pi-\alpha-\phi)} \cdot e^{j\theta}, \end{aligned} \tag{3.4}$$

By combing (3.3) and (3.4), the transfer function $H(j\omega)$ can be written as

$$H(j\omega) = \frac{V_{out}}{V_{in1}} = -\sqrt{g_{m1}^2 + g_{m2}^2 + 2g_{m1}g_{m2}cos(\pi - \alpha - \phi)} \cdot e^{j\theta} \cdot \frac{R_o}{1 + j\omega R_o C_L} \tag{3.5}$$

$$\angle H(j\omega) = -\pi - (tan^{-1}(\omega R_o C_L) - \theta). \tag{3.6}$$

According to Barkhausen criterion of oscillation [1], the ring oscillator would oscillate if loop has unity voltage gain, i.e.,

$$|H(j\omega)| = 1 \Rightarrow \frac{\sqrt{g_{m1}^2 + g_{m2}^2 + 2g_{m1}g_{m2}cos(\pi-\alpha-\phi)} \cdot R_o}{\sqrt{1 + (\omega R_o C_L)^2}} = 1 \tag{3.7}$$

and have a phase shift of 2π or a multiple of 2π. Thus, from (3.6) the oscillation frequency can be expressed as

$$\omega_{osc} = \frac{1}{R_o C_L} \cdot tan(\phi + \theta), \tag{3.8}$$

with further derivation the oscillation frequency can be rewritten as

$$\omega_{osc} = \frac{1}{R_o C_L} \cdot \frac{g_{m1}sin\phi + g_{m2}sin\alpha}{g_{m1}cos\phi - g_{m2}cos\alpha} = \frac{1}{R_o C_L} \cdot \frac{g_{m1,Q} + g_{m2,Q}}{g_{m1,I} - g_{m2,I}}, \tag{3.9}$$

where $g_{m1,I}$, $g_{m1,Q}$ equals to $g_{m1}cos\phi$ and $g_{m1}sin\phi$, respectively. And $g_{m2,I}$, $g_{m2,Q}$ equals to $g_{m2}cos\alpha$ and $g_{m2}sin\alpha$, respectively. Combing (3.7) and (3.9), the criterion for oscillation becomes

$$(g_{m1,I} - g_{m2,I}) \cdot R_o = 1$$

or

$$g_{m1,I} \cdot (R_o // \frac{1}{g_{m2,I}}) = 1 \cdot \tag{3.10}$$

In summary, a *N*-stage ring oscillator must satisfy the conditions in (3.7) or (3.10), and have an open loop phase shift of 2π or a multiply of 2π, then the oscillation frequency will be as derived in (3.9). As shown, if the number of stages in the ring increase, the terms $g_{m1,I}$ raises and $g_{m1,Q}$ lowers causing oscillation frequency to decrease. Further, illustrated in (3.9) and (3.10) if $\alpha<\pi/2$ the term $g_{m2,I}$ will be positive and behaves like diode connection transistors which is equivalent to a positive resistance in parallel with R_o at the output node, thus reduces the total resistance and increases the oscillation frequency. On the other hand, if $\alpha>\pi/2$ the term $g_{m2,I}$ will be negative and behaves like negative-coupled resistance, thus increases the total output resistance and reduces the oscillation frequency. In order to achieve higher oscillation frequency by means of the additional-delay paths, by

solving

$$\frac{g_{m1}sin\phi + g_{m2}sin\alpha}{g_{m1}cos\phi + g_{m2}cos\alpha} > \frac{g_{m1}sin\phi}{g_{m1}cos\phi}, \tag{3.11}$$

we find α must be less than π-ϕ.

Moreover, to achieve the optimal oscillation frequency due to additional-delay paths in a *N*-stage ring oscillator, indicated in (3.9), the denominator should be minimized and the numerator should be maximized, simultaneously. Therefore, optimum value for $g_{m2,I}$ and $g_{m2,Q}$ must be chosen without conflicting the criterions for oscillation. From (3.10), the minimum value for the denominator value equals to 1, therefore

$$g_{m2,I\_max} = \frac{1}{R_o} + g_{m1,I}. \tag{3.12}$$

Also indicated in (3.10), $g_{m2,Q}$ does not effect the oscillation criterion, thus if $g_{m2,Q}$ increases the numerator value increases, and if there is no change on the output loadings the oscillation frequency increases as well. However, in real circuits as $g_{m2,Q}$ increases the parasitic capacitors C_L also increases, eventually limits the oscillation frequency. Thus a optimum value g_{m2,Q_max} should be chosen without significant change on the output

loadings. Now by the values g_{m2,I_max} and g_{m2,Q_max}

$$g_{m2} = \sqrt{g_{m2,I\_max}^2 + g_{m2,Q\_max}^2} \tag{3.13}$$

and

$$\alpha = tan^{-1}\left(\frac{g_{m2,Q\_max}}{g_{m2,I\_max}}\right). \tag{3.14}$$

Note, g_{m2} stands for the transconductance strength of the additional-delay path device, and the phase α determines the way to inject the additional signal into the delay cell. One may question on how to find the additional signal V_{in2} which has a α phase difference with respect to the output signal V_{out} in a N-stage ring oscillator. This could be attained by introducing multiple-delay path delay cells, for example triple-delay path delay cells, which vector summation equivalent meats the results obtained in (3.13) and (3.14).

3.3 Two Operation Modes in Dual-Delay Path Ring Oscillator

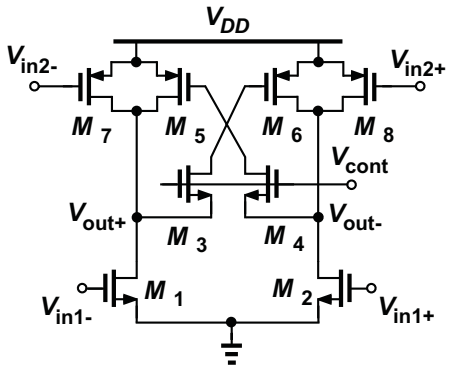
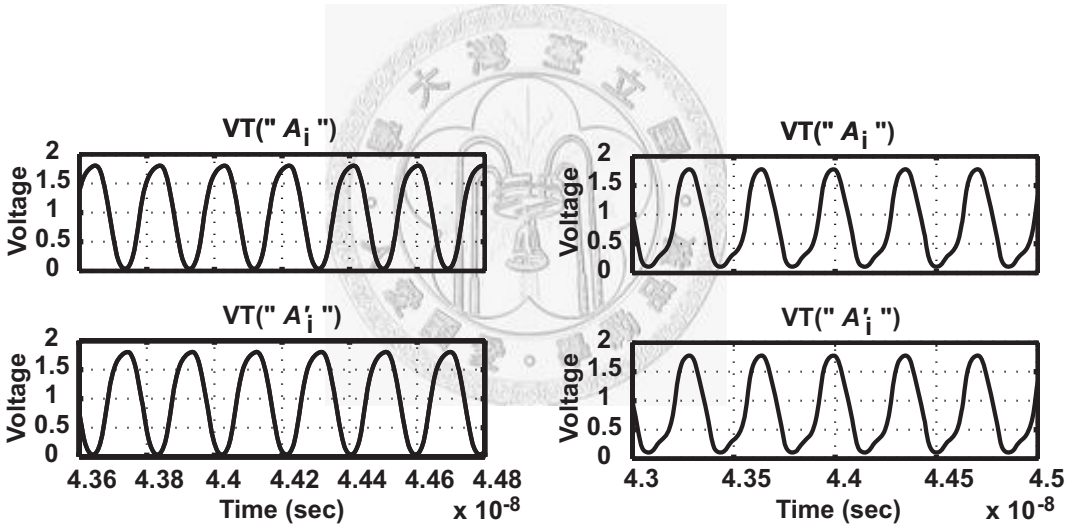


Figure 3.4 Schematic of a delay cell in dual-delay path ring oscillators.



(a) (b)

Figure 3.5 Simulated output wave forms of a dual-delay path ring oscillator. (a) Differential-mode oscillation.

(b) Common-mode oscillation.

The circuit implementation of a delay cell in dual-delay path ring oscillators is shown in figure 3.4 [19] [20]. As mentioned before, the initial conditions affect the operation mode

of the ring oscillator. There are two oscillation modes in a differential four-stage dual-delay path ring oscillator, referred as differential-mode oscillation and common-mode oscillation, respectively. In differential mode, the output waveforms of a delay cell are differential, shown in figure 3.5(a). On the contrary, in common mode the output waveforms become in-phased as indicated in figure 3.5(b). Besides the difference in output waveforms, the oscillation frequency of the two oscillation modes differs as well. In the following context, the oscillation frequency and oscillation criterion of both modes will be analyzed and derived.

3.3.1 Differential-mode oscillation

Consider the circuit in figure 3.4. Transistors $M_{1,2}$ and $M_{7,8}$ are the input devices of the main-delay path signals and the additional-delay path signals, respectively. M_5 and M_6 constitute a CMOS latch, M_3 and M_4 tune the gate voltage of M_5 and M_6 and limit the differential driving strength. Specifically, when V_{cont} is high, the effective strength of the latch becomes strong, and it resists the voltage switching in the differential delay cell. Consequently, the delay time increases. The latch path formed by M_5 and M_6 generates full switching rail-to-rail output waveforms. This type of ring oscillator exhibits better phase-noise performance since the transistors periodically turns on and off which reduces

the noise generated from them [19]. Furthermore, larger output amplitude corresponds to better noise performance as well.

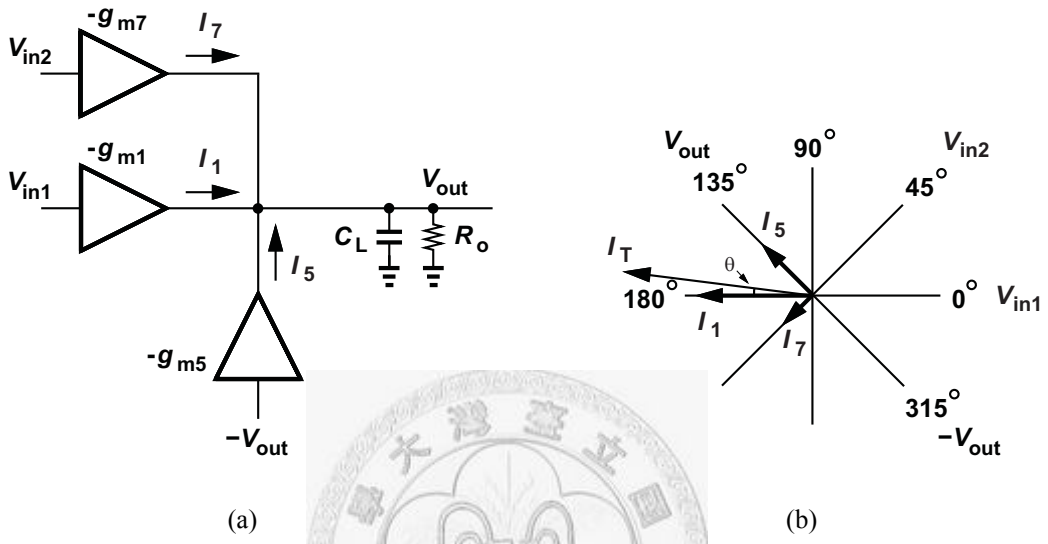


Figure 3.6 (a) Simple half circuit small-signal model of the delay cell. (b) The phasor diagram of the signals V_{in1}, V_{in2}, V_{out} and currents I_1, I_5, I_7.

Figure 3.6(a) shows the simple half circuit small-signal model of the delay cell in figure 3.4. To simplify the analysis, transistors M_3 and M_4 are neglected and not included in this model. g_{m1}, g_{m5} and g_{m7} represent the transconductance of M_1, M_5 and M_7, respectively. C_L and R_o are the loadings at the output node. V_{in1}, V_{in2} and V_{out} are the main input signal, additional input signal and output signal of the delay cell, respectively. I_1, I_5 and I_7 are the drain currents of the transistors M_1, M_5 and M_7, respectively. The phasor diagram of the signals V_{in1}, V_{in2}, V_{out} and currents I_1, I_5, I_7 in a stable oscillation state is illustrated in figure

3.6(b). Refer to the parameters in section 3.2, g_{m7} represents g_{m2} and N equals to 4 here. The phase ϕ equals to $\pi/4$, and the phase α equals to $\pi/2$. Thus from (3.1), $V_{in1,I}=V_{in1}e^{-j(\pi/4)}cos(\pi/4)$, $V_{in1,Q}=V_{m1}e^{j(\pi/4)}\ sin(\pi/4)$, hence $g_{m1,I}=g_{m1}cos(\pi/4)$, $g_{m1,Q}=g_{m1}sin(\pi/4)$. Further, from (3.2), $V_{in2,I}= V_{in2}e^{j(\pi/2)}cos(\pi/2)$, $V_{in2,Q}= V_{in2}sin(\pi/2)$, hence $g_{m7,I}=g_{m7}cos(\pi/2)$, $g_{m7,Q}= g_{m7}sin(\pi/2)$. Furthermore, the phase θ represents the phase difference of I_T with respect to I_1, where I_T is the vector summation of I_1, I_5 and I_7. Now, the transfer function $H(j\omega)$ between V_{in1} and V_{out} of the single stage delay cell in figure 3.6(a) can be derived as

$$H(j\omega)=\frac{V_{out}}{V_{in1}} = -\sqrt{g_{m1}^2+g_{m5}^2+g_{m7}^2+g_{m1}g_{m5}cos\,\pi/4+g_{m1}g_{m7}cos\,\pi/4}\cdot e^{j\theta}\cdot\frac{R_o}{1+j\omega R_oC_L}, \quad (3.15)$$

The oscillation frequency can be found as

$$\omega_{osc}=\frac{1}{R_oC_L}\cdot\frac{g_{m1}+\sqrt{2}\cdot g_{m7}}{g_{m1}+\sqrt{2}\cdot g_{m5}}, \quad (3.16)$$

moreover the criterion for oscillation is expressed as

$$\frac{g_{m1}\cdot\left(R_o \,//\, \frac{-1}{g_{m5}}\right)}{\sqrt{2}} = 1. \tag{3.17}$$

In summary, a four-stage ring oscillator requires equation (3.17) to be satisfied, and the oscillation frequency will be as derived in (3.16). The g_{m7} term in (3.16) corresponds to the frequency increment due to the additional-delay path. To be noted, g_{m5} corresponds to the strength of CMOS latch, as mentioned before if the latch becomes strong the delay time increases thus reduces the oscillation frequency, this can be interpreted in (3.16) as well.

3.3.2 Common-mode oscillation

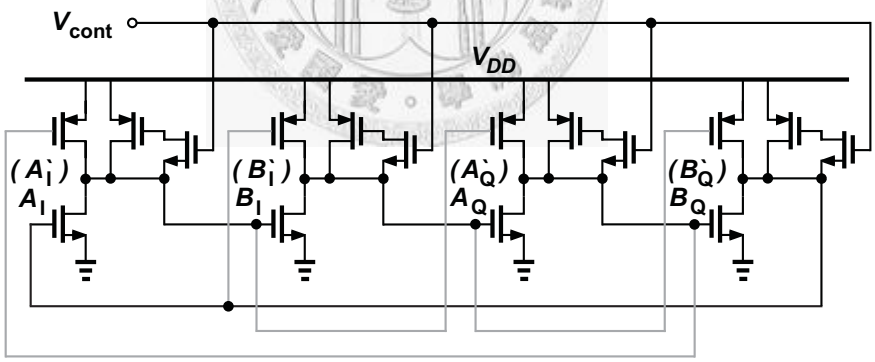


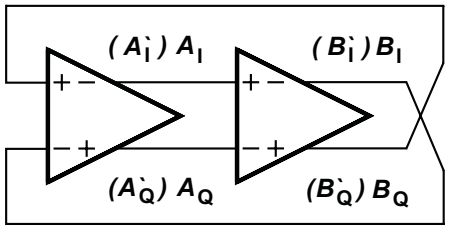
Figure 3.7 Schematic of the differential four-stage dual-delay path ring oscillator in common-mode oscillation.

In dual-delay path ring oscillators under common-mode oscillation the output waveform of each delay cell becomes in-phased instead of differential phased. As illustrated in figure 3.5(b), the output waveforms A_I and $A`_I$ of figure 3.1 are in-phased, so are $B_I$ and $B`_I$, A_Q

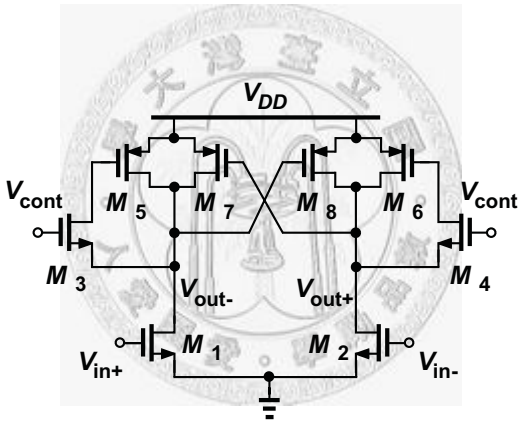
and $A`_Q$, $B_Q$ and $B`_Q$. Refer to the delay cell schematic in figure 3.4, we expect the CMOS latch constructed by M_5 and M_6 to drive the delay cell outputs differentially. However in common mode each delay cells are found to be in-phased instead of differential phased, thus suppose the latching part of the delay cell is not working properly and a new main-delay path dominates the oscillation. In figure 3.7, the scheme of the differential four-stage dual-delay path ring oscillator operating in common mode is shown. We omitted the other half circuit since the outputs of each delay cells are in-phased and the other half circuit operates in a complete same manner.

Figure 3.7 can be further represented as figure 3.8. Where figure 3.8(a) shows a differential two-stage ring oscillator, the schematic of each delay cell block is shown in figure 3.8(b). Here we find a differential four-stage dual-delay path ring oscillator operating in common mode is equivalent to a differential two-stage ring oscillator with no additional-delay paths. The internal nodes in figure 3.1 are indicated in figure 3.8(a). Note in figure 3.8(b), the transistors M_5 and M_6 constructs diode connection and is equivalent to a positive resistance. But shown in figure 3.4, they construct a CMOS latch which is equivalent to a negative resistance in differential-mode oscillation. Moreover in figure 3.8(b), the transistors M_7 and M_8 constitute a CMOS latch but in differential-mode oscillation they constitute the additional-delay paths. Now, by applying the first-order

small-signal model, the oscillation frequency and oscillation criterion of the two-stage ring oscillator can be derived.

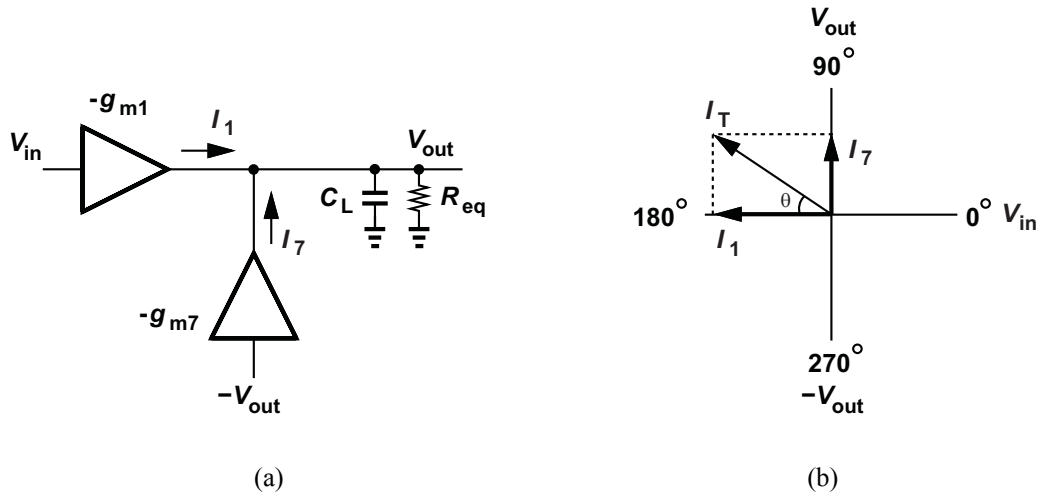


(a)



(b)

Figure 3.8 (a) A differential two-stage ring oscillator. (b) Schematic of the delay cell.



(a) (b)

Figure 3.9 (a) Simple half circuit small-signal model of a delay cell. (b) The phasor diagram of the signals V_{in}, V_{out} and currents I_1, I_7.

Figure 3.9(a) is the simple half circuit small-signal model of the delay cell shown in figure 3.8(b). Transistors M_3 and M_4 are neglected and not included in this model for simplicity. g_{m1} and g_{m7} represent the transconductance of M_1 and M_7, respectively. R_{eq} represents the total equivalent output resistance at the output node, which includes the transistors drain resistance R_o in parallel with the diode connection resistance $1/g_{m5}$ presented by $M_{5,6}$. C_L represents the total loading capacitance at the output node. V_{in} and V_{out} are the input and output signal of a single delay cell. I_1 and I_7 are the drain currents of the two transistors M_1 and M_7, respectively. The phasor diagram of the signals V_{in}, V_{out} and currents I_1, I_7 in stable oscillation state is illustrated in figure 3.9(b). Refer to the parameters in section 3.2, since there is no additional-delay path in the two-stage ring

oscillator, g_{m2} equals to 0. Further, N equals to 2 and ϕ equals to $\pi/2$ here. Thus from (3.1), $V_{in1,I}=V_{in1}e^{-j(\pi/2)}cos(\pi/2)$, $V_{in1,Q}= V_{in1}sin(\pi/2)$, hence $g_{m1,I}= g_{m1}cos(\pi/2)$, $g_{m1,Q}= g_{m1}sin(\pi/2)$. Furthermore, θ represents the phase difference of I_T with respect to I_1, where I_T is the vector summation of I_1 and I_7. Now, the transfer function $H(j\omega)$ between V_{in} and V_{out} of the single stage delay cell in figure 3.9(a) can be derived as

$$H(j\omega)=\frac{V_{out}}{V_{in}}=-\sqrt{g_{m1}^2+g_{m7}^2}\cdot e^{j\theta}\cdot\frac{R_{eq}}{1+j\omega R_{eq}C_L}, \tag{3.18}$$

where $R_{eq}=R_o//(1/g_{m5})$. The oscillation frequency can be obtain as

$$\omega_{osc}=\frac{1}{R_{eq}C_L}\cdot\frac{g_{m1}}{g_{m7}}, \tag{3.19}$$

moreover the criterion for oscillation is expressed as

$$g_{m7}\cdot R_{eq}=1. \tag{3.20}$$

In summary, a two-stage ring oscillator requires equation (3.20) to be satisfied, and the oscillation frequency will be as derived in (3.19). To be noted, the g_{m7} term corresponds to

the strength of CMOS latch constructed by the transistors M_7 and M_8, in figure 3.8(b). As mentioned before if the latch becomes strong the delay time increases thus reduces the oscillation frequency, this can be interpreted in (3.19) as well.

Finally, from the above derivation, the frequency and oscillation criterion of both oscillation modes in a differential four-stage ring oscillator has been derived. It should be noted here, depending on the initial conditions and components in the system, the dual-delay path ring oscillator can generate a steady-state oscillation in either differential mode or common mode, even without the CMOS latch circuit constructed by M_5 and M_6, in figure 3.4. In order to insure a particular oscillation mode the system must satisfy two conditions [22]. First, it should have enough energy to force the system outside its initial region of attraction. The second condition is that the energy should be applied in such a way that the nonlinear dynamical system moves towards the intended steady-state stable mode. Therefore, if we wish to operate the oscillator in the differential mode, we can either apply initial conditions in the system or design the components in the oscillator to prevent common-mode oscillation. From (3.20), if the value $g_{m7}R_o$ is designed to be less than unity, common-mode oscillation will never occur. However, to insure $g_{m7}R_o$ less than unity g_{m7} will be small, but shown in (3.16), smaller g_{m7} reduces the oscillation frequency in differential-mode oscillation. Another choice is to design the circuit to have much larger

loop gain in differential mode than in common mode at the oscillation frequency of each case, from (3.15) and (3.18) that is

$$\frac{g_{m1}\cdot\left(R_o \,//\, \frac{-1}{g_{m5}}\right)}{\sqrt{2}} >> g_{m7}\cdot\left(R_o \,//\, \frac{1}{g_{m5}}\right). \tag{3.21}$$

In practice, 5 to 10 times for the ratio of the differential-mode to common-mode loop gain should be sufficient to ensure differential-mode oscillation.

3.4 Simulation and Experimental Results

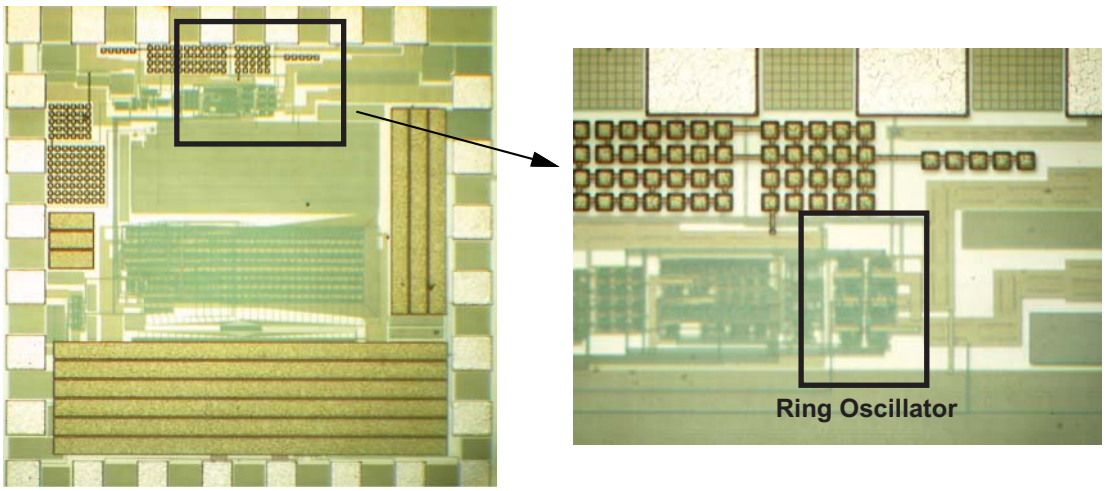
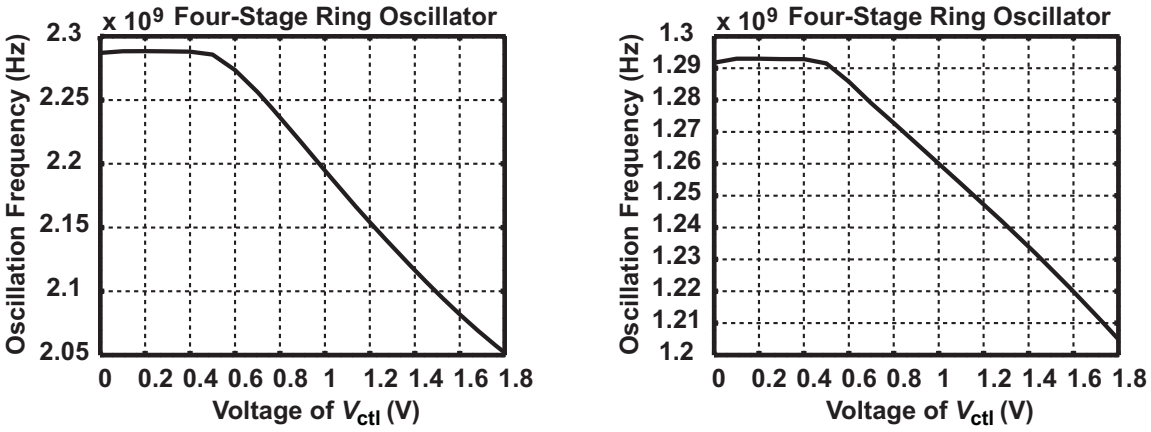


Figure 3.10 Microphotograph of the fabricated differential four-stage dual-delay path ring oscillator.

A differential four-stage dual-delay path ring oscillator was designed and fabricated in a 0.18-μm CMOS technology. Figure 3.10 shows the die photo of the fabricated circuit. The schematic of delay cells are the same as those shown in figure 3.4. Table 3.1 presents the sizes of each transistors in a delay cell. The post-simulation tuning characteristics of the dual-delay path ring oscillator operating in differential-mode oscillation and common-mode oscillation are shown in figure 3.11(a) and 3.11(b), respectively.

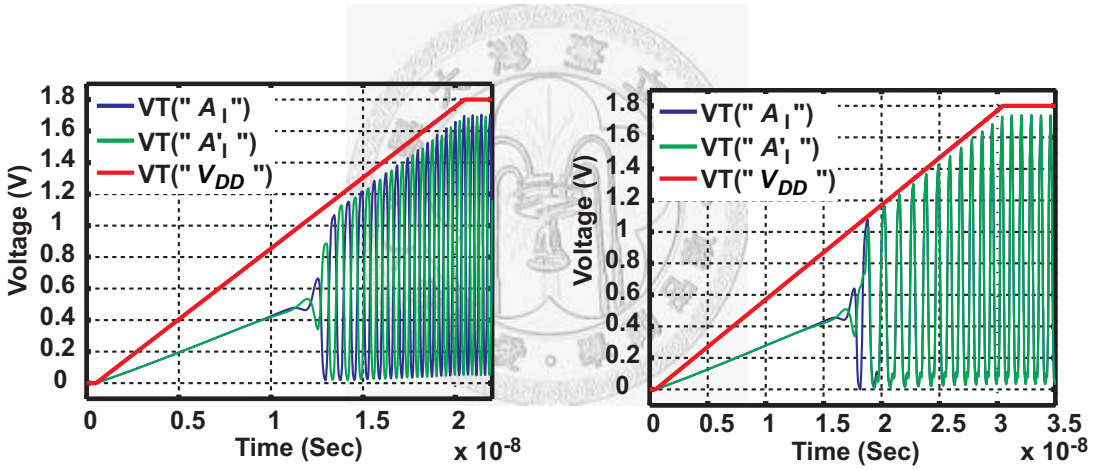
Dual-Delay Path Ring Oscillator (μm)	
M_1, M_2	15 / 0.37
M_3, M_4	10.2 / 0.18
M_5, M_6	0.9 / 0.18
M_7, M_8	27 / 0.36

Table 3.1 Transistors size.



(a) (b)

Figure 3.11 Simulated tuning range. (a) Differential-mode oscillation. (b) Common-mode oscillation.



(a) (b)

Figure 3.12 Post-simulation results (a) Fast V_{DD} start up process. (b) Slow V_{DD} start up process.

To investigate the two oscillation modes, note the fabricated dual-delay path ring oscillator does not contain an initial condition start up circuit. Thus, in order to specify a specific oscillation mode, during testing we apply different ramping on V_{DD} start up. In normal, while the power supply turns on, V_{DD} will not be in high potential immediately,

instead the potential shows a gradually ramp up characteristic. Post simulation results of two different V_{DD} start up process, is shown in figure 3.12. In this work if the V_{DD} ramp up slope is larger than $1.8V/25nsec$ as shown in figure 3.12(a) the ring oscillator enters differential mode. On the other hand, if the slope is less than $1.8V/25nsec$ the ring oscillator enters common mode, figure 3.12(b).

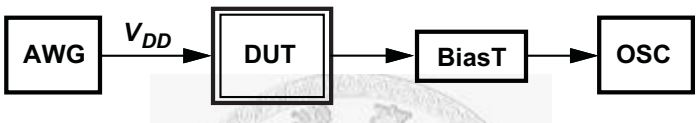
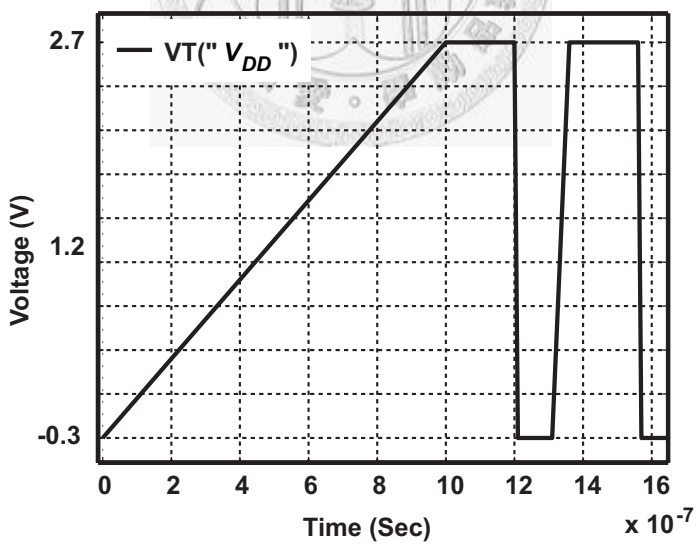
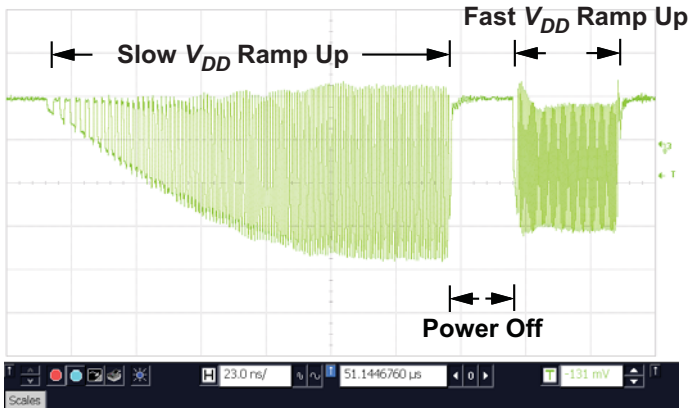


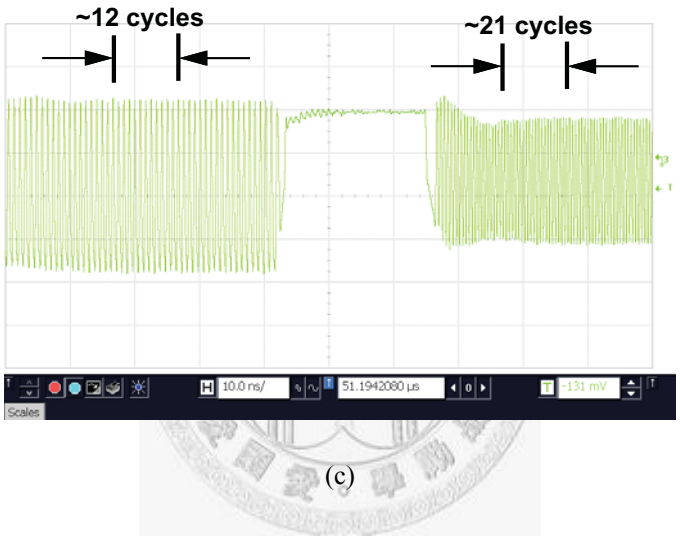
Figure 3.13 Measurement setup.



(a)



(b)



(c)

Figure 3.14 (a) The sequential V_{DD} signal with slow ramp up slope and fast ramp up slope. (b) Measured output waveform of the ring oscillator. (b) Zoom in of the output waveform.

The measurement setup is illustrated in figure 3.13. In order to control the V_{DD} start up process an arbitrary waveform generator (AWG) was applied as the power supply. A demonstration of two oscillation modes is shown in figure 3.14. A sequential V_{DD} signal containing a slow ramp up slope followed by a fast ramp up slope is applied to the ring oscillator, figure 3.14(a). The measured output waveforms are shown in figure 3.14 (b) and

(c). Note, indicated in figure 3.14(c) the oscillation frequency in slow V_{DD} start up is about half the frequency than in fast V_{DD} start up, in which the oscillator operates in common mode and differential mode, respectively. The measured tuning characteristics of the fabricated dual-delay path ring oscillator are shown in figure 3.15(a) and (b). Moreover, the measured ring oscillator output spectrum and phase noise performance are shown in figure 3.16 and figure 3.17. Table 3.2 summarizes the measurement results.

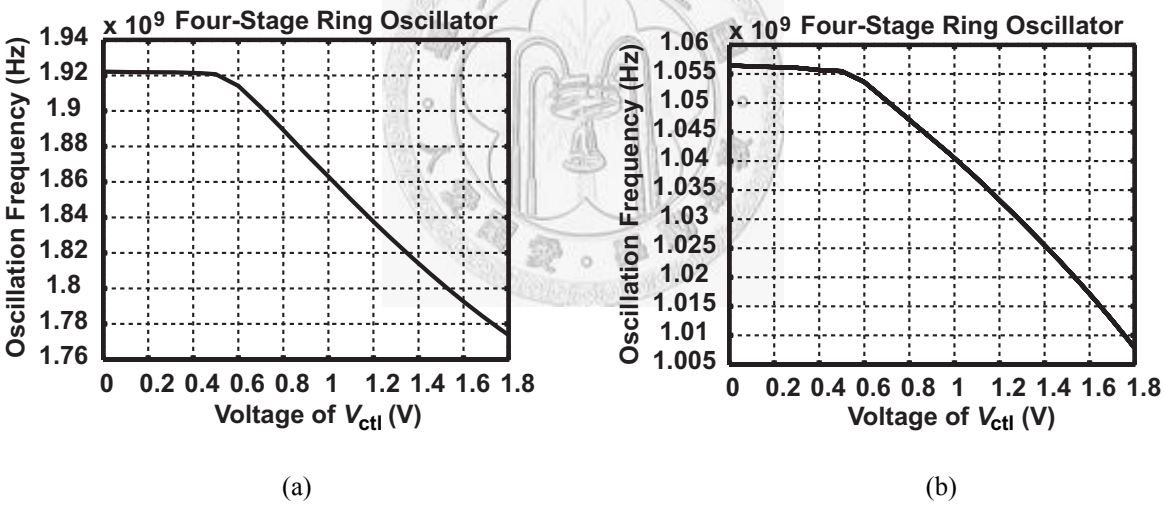
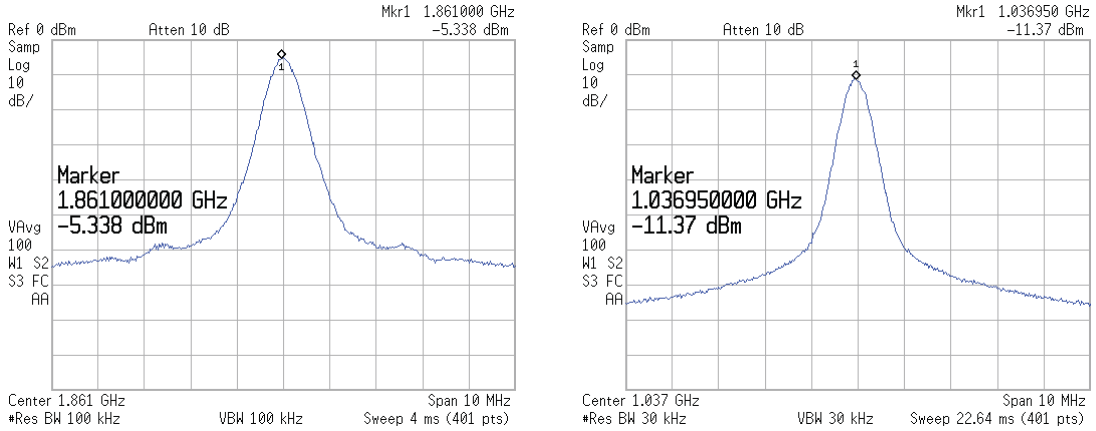
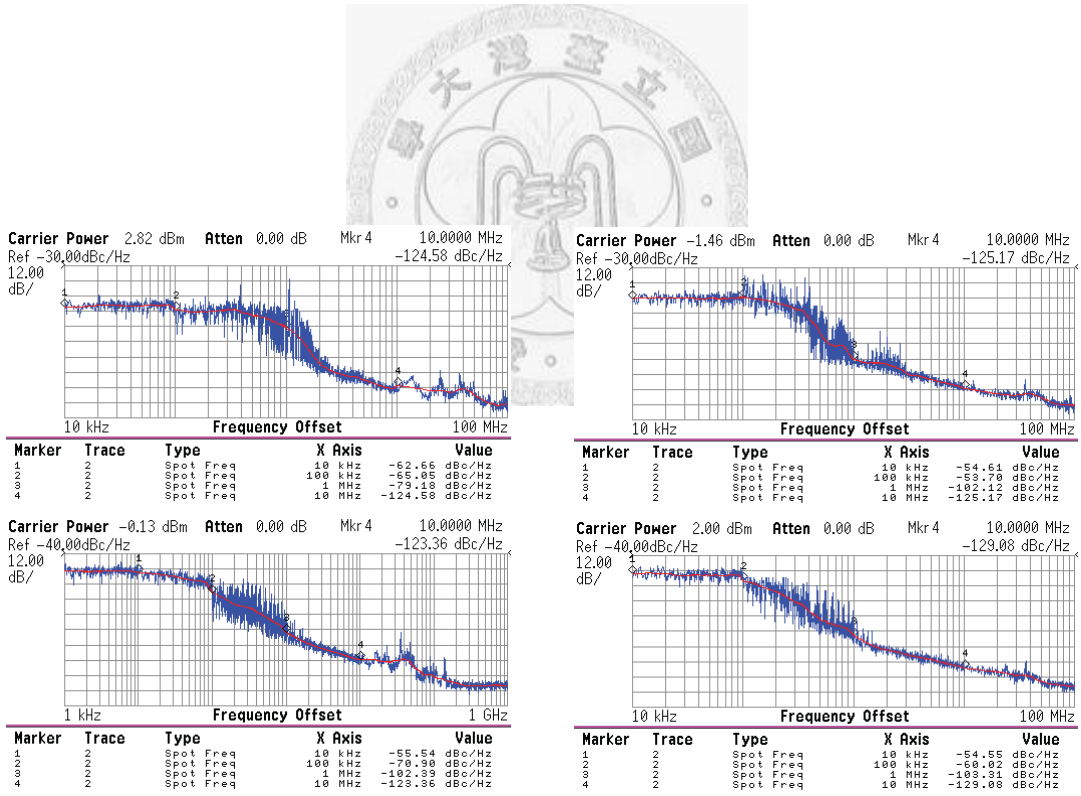


Figure 3.15 Measured tuning range. (a) Differential-mode oscillation. (b) Common-mode oscillation.



(a) (b)

Figure 3.16 Measured output spectrum. (a) Differential-mode oscillation. (b) Common-mode oscillation.



(a) (b)

Figure 3.17 Measured output phase noise. (a) Differential-mode oscillation. (b) Common-mode oscillation.

Technology	0.18-μm CMOS	
Active Area	58×41 μm^2	
Supply	1.8 V	
	Differential Mode	Common Mode
Oscillation frequency	1.77 GHz ~ 1.92 GHz	1.01 GHz ~ 1.055 GHz
Phase Noise @ 1MHz	-102 dBc/Hz	-103 dBc/Hz
Power (with buffer)	~ 13 mW	~ 10 mW

Table 3.2 Performance summary of experimental results.

3.5 Conclusion

Dual-delay path ring oscillators are often implemented to obtain higher oscillation frequencies in ring oscillators. However, there happens to be dual operation modes in differential 4-stage dual-delay path ring oscillators. The initial conditions affect the operation of the ring oscillator. The main difference of the two oscillation modes is the output waveform characteristic. Instead of typical differential outputs, the outputs of a delay cell become in-phased. Furthermore, the oscillation frequency in either mode may not be the same. In this work, analysis and demonstration of the two oscillation mode is presented, showing how a second mode happens and how to prevent its occurrence.

Chapter 4

A Multiphase Compensation Method with Dynamic Element Matching Technique in Σ-Δ Fractional-N Frequency Synthesizers

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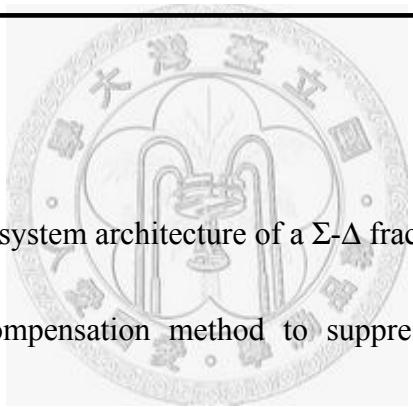


This chapter introduces the system architecture of a Σ-Δ fractional-*N* frequency synthesizer, including a multiphase compensation method to suppress the Σ-Δ modulator output quantization noise, and dynamic element match techniques for mismatch linearization.

4.1 Introduction

PLL-based frequency synthesizers are widely used in communication systems. Fractional-*N* frequency synthesizers are used rather than integer-*N* frequency synthesizers because of the relaxed tradeoffs between frequency resolution and loop bandwidth. In high-frequency resolution applications, integer-*N* frequency synthesizers lack for large

loop bandwidth which limits the settling speed and in-band VCO phase noise performance. On the contrary, fractional-*N* frequency synthesizers are able to resolve these problems, by allowing fractional divisions, high-frequency reference clock, high resolution, and larger loop bandwidth frequency synthesizers can be employed.

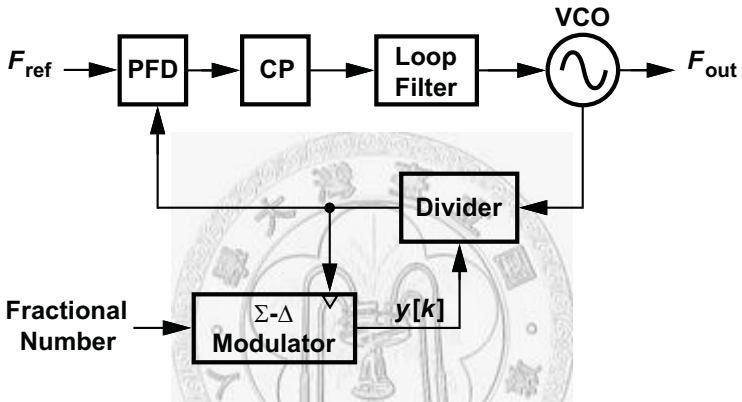


Figure 4.1 A conventional Σ-Δ fractional-*N* frequency synthesizer.

Figure 4.1 shows the diagram of a conventional Σ-Δ fractional-*N* frequency synthesizer [2] [3] [23]. The fractional division is often based on a Σ-Δ modulator and multi-modulus dividers. The Σ-Δ modulator produces a sequence of integer numbers whose mean is equal to the fractional number. The sequential integer numbers controls the division of the divider so that the desired fractional ratio is obtained. The deviation between the integer number and the fractional number is called quantization noise which has a high-pass feature in frequency domain [4], and often dominates at high offset frequencies. By

reducing the loop bandwidth, high-pass quantization noise can be suppressed, but this conflicts the advantage in using fractional-*N* synthesizers, which is to increase loop bandwidth. There are several methods to compensate the quantization noise, such methods include DAC compensation [7] [8], multiphase compensation [9]-[11], PFD/DAC compensation [12], and compensation based on 1/1.5 dividers [13].

Most of the reported multiphase compensation methods are based on ring VCO [9] [11] or delay-locked loop (DLL) [14] and a Σ-Δ modulator or counter. The main purpose of these designs is to reduce the quantization noise by generating multiphase fractional divisions. However, nonideal effect such as multiphase mismatch or gain error causes serious problems like in-band noise and spurious tones.

In this work, to suppress the quantization noise, a multiphase compensation method based on delay-locked loop and a proposed delay line structure are implemented for the advance of no pulse amplitude problem that occurs in DAC compensation methods [7] [8] [12]. In the proposed delay line structure, dynamic element matching (DEM) techniques [24] [25] are introduced to improve frequency synthesizer phase noise due to the timing mismatch in the delay line units. A 200-kHz bandwidth Σ-Δ fractional-*N* frequency synthesizer operating at the frequency of 2.14 GHz with a 35-MHz input reference clock is

built for demonstration.

4.2 Architecture of the Σ-Δ Fractional-*N* Frequency Synthesizer

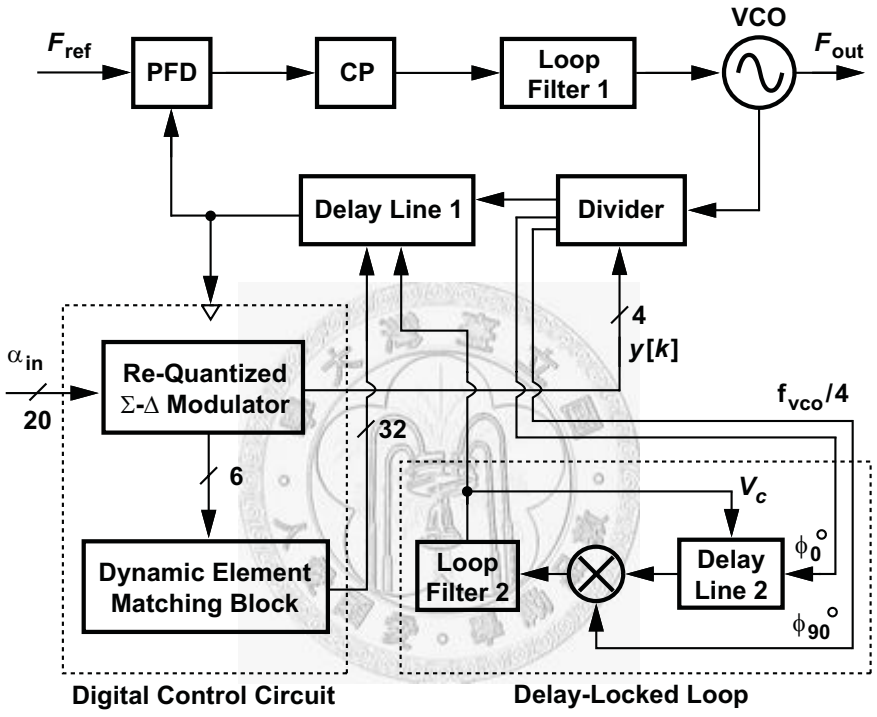


Figure 4.2 Proposed frequency synthesizer architecture.

Figure 4.2 depicts the architecture of the proposed Σ-Δ fractional-*N* frequency synthesizer. The delay-locked loop and delay line 1 are employed for multiphase compensation that suppresses the quantization noise. Rather than generating all the multiphase signals in advance [9] [11] [14], the proposed delay line 1 structure generates specific phased signal only when it is needed.

The digital control circuit contains two main building blocks. The first one is a re-quantized Σ-Δ modulator [8], which contains two Σ-Δ modulators and is employed to resolve the nonideal effect of delay time gain error in delay units and simultaneously generates the specific fractional division. The second one is the dynamic element matching block, which contains DEM algorithms for mismatch linearization. Details of the proposed frequency synthesizer will be discussed in the followings.

4.2.1 Delay-Locked Loop and Delay Lines

The proposed fractional-*N* frequency synthesizer employs a third-order Σ-Δ modulator. Therefore, second-order quantization noise will be induced to the frequency synthesizer through the operation of divider [6]. In order to extend the loop bandwidth to 200-kHz, a reduction of 18 dB in quantization noise will be required to attain the same noise level as a 70-kHz bandwidth frequency synthesizer at 10-MHz frequency offset [8]. In multiphase compensation frequency synthesizers, to reduce the quantization noise of 18 dB, a least delay time of $T_{vco}/8$ is required. Some methods such like ring VCO [9] [11] or delay-locked loop [14] has been employed to realize this small delay interval. In this work, a delay-locked loop is employed to generate the $T_{vco}/8$ delay time.

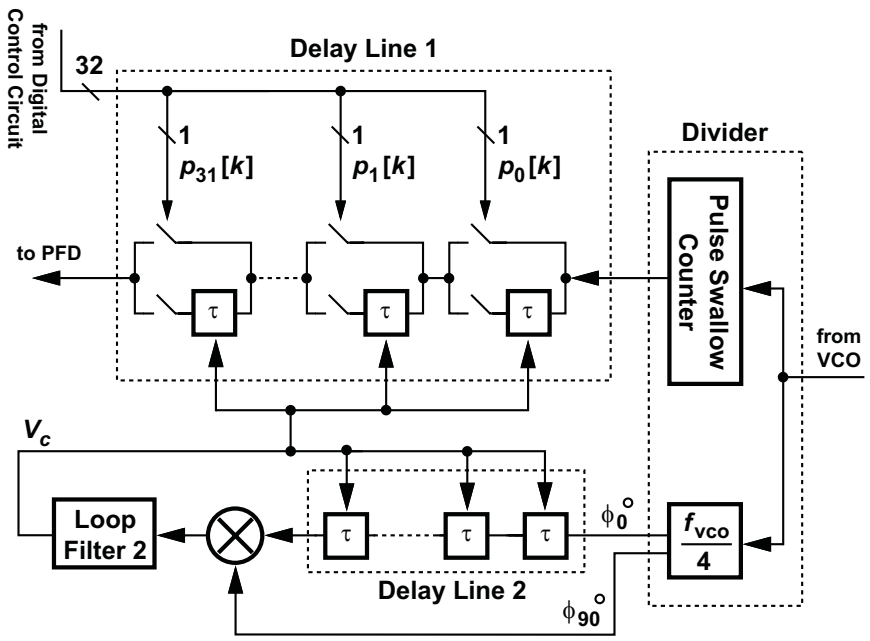
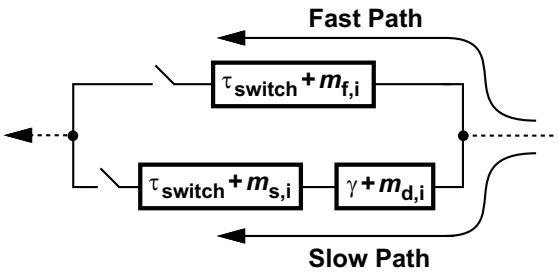


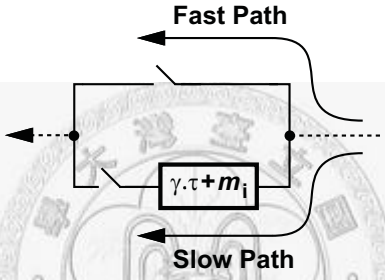
Figure 4.3 Proposed delay-locked loop and delay line 1 structure.

Figure 4.3 depicts is the proposed delay-locked loop and delay line 1 structure. The high-frequency signal of VCO output is first divided by four to achieve the two quadrature signals ϕ_0^o and ϕ_{90}^o, which has 90-degree phase difference. With quarter-rate operation frequency, the power consumption of the delay-locked loop could be highly reduced. The ϕ_0^o signal then enters the delay line 2 and compares its phase with ϕ_{90}^o at the phase frequency detector. The purpose of the 90-degree phase difference is to reduce the needed numbers of delay units. For example, if the two input signals of delay-locked loop are in-phased, 32 delay units are needed to maintain a delay time of $T_{vco}/8$ in each delay units. However, only 8 delay units are required for a pair of 90-degree phase difference input

signals.



(a)



(b)

Figure 4.4 Nonideal model of subcircuits in delay line 1. (a) Mismatch in slow path and fast path. (b) Mismatch considered only in delay unit.

While the delay-locked loop is under locked condition, each delay unit in delay line 2 has a delay time τ equal to $T_{vco}/8$. With replica delay units, this delay time is mapped to the delay units in delay line 1 by voltage control signal V_c. The structure of delay line 1 is depicted in figure 4.3. Delay line 1 can be divided into 32 subcircuits, where each of them contains two switches and a delay unit. The reason for 32 subcircuit will be derived in the following context. Shown in figure 4.3, input signals passes through each subcircuit either by the fast path or slow path controlled by the signal $p_i[k]$. If $p_i[k]$ equals to 1, the input

signal passes the i^{th} subcircuit through slow path. On the other hand, if $p_i[k]$ equals 0, the input signal passes the i^{th} subcircuit through fast path. Thus the multiphase signals can be generated through this topology specifically by the control signals $p_i[k]$ that is produced from digital control circuit.

Ideally, the delay time of a subcircuit will increase with an additional time τ while switching from fast path to slow path. However, nonideal effect such as mismatches and propagation delays in switches or delay units should be considered. Figure 4.4(a) shows a nonideal model of a subcircuit in delay line 1. τ_{switch} represents the propagation delay of the switches. $m_{f,i}$ and $m_{s,i}$ are the mismatch factors of the two switches. Further, τ represents the ideal delay time of a delay unit equal to those in delay-locked loop, and $m_{d,i}$ represents the mismatch factor in the delay unit. Though various mismatch and parasitic propagations exists in real circuits, only the delay time difference between slow path and fast path is considered. That is, the additional delay time while switching from fast path to slow path

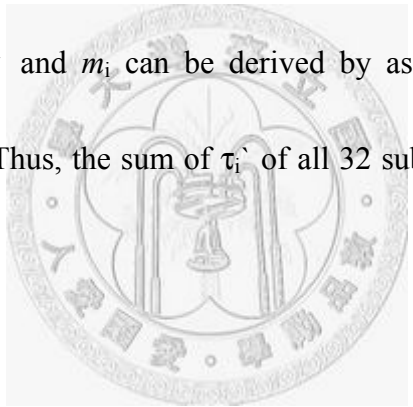
$$\begin{aligned} \tau_i` &= (\tau_{switch} + m_{s,i} + \gamma + m_{d,i}) - (\tau_{switch} + m_{f,i}), \\ &= \tau + (m_{d,i} + m_{s,i} - m_{f,i}) \end{aligned} \tag{4.1}$$

where $\tau_i`$ represents the delay time difference of a nonideal subcircuit. From (4.1), a

mismatch term contributed by nonideal effects in addition to the ideal delay time can be observed. Now, (4.1) can be rewritten as

$$\tau_i` = \gamma \cdot \tau + m_i, \tag{4.2}$$

where the two delay time difference in (4.1) and (4.2) are the same, but the effect of delay mismatches are now represented by means of a gain error factor γ and a new mismatch factor m_i. The values of γ and m_i can be derived by assuming the sum of $m_i`$ of all subcircuits equals to zero. Thus, the sum of $\tau_i`$ of all 32 subcircuits in delay line 1 can be obtain as



$$\sum_{i=1}^{32} \tau_i` = 32 \cdot \gamma \cdot \tau \cdot \tag{4.3}$$

And the gain error factor γ can be derived as

$$\gamma = \frac{\sum_{i=1}^{N} \tau_i`}{32 \cdot \tau} \cdot \tag{4.4}$$

By substituting (4.4) into (4.2) the mismatch factor m_i within each subcircuit can be obtain

as

$$m_i = \tau_i` - \left(\frac{\sum_{i=1}^{N}\tau_i`}{32 \cdot \tau}\right) \cdot \tau \cdot \quad (4.5)$$

Note that the gain error and mismatch factor in (4.4) and (4.5) can also be related to the parameters in (4.1). Figure 4.4(b) shows the simplified mismatch model of a subcircuit. The effects of various mismatch sources in the subcircuit are now equivalently comprehended inside the delay unit. This simplification leads to an equivalent model of the nonideal effect by means of gain error and mismatches. Analysis of nonideal effects on frequency synthesizer phase noise performance will be further derived in the following sections.

4.2.2 Re-Quantized Σ-Δ Modulator

In the proposed frequency synthesizer, a re-quantization Σ-Δ modulator is implemented to control the divider and delay line 1 for deriving both accurate fractional division and low quantization noise. The reason to use re-quantized Σ-Δ modulator technique rather than the more general technique, multiphase fractional division [9]-[11], is that the former can

achieve high pass noise shaped characteristic on delay unit gain error, while in the latter one, delay unit gain error acts like random noise in the frequency synthesizer that causes in-band noise and spurious tones at the synthesizer output. The effect of delay unit gain error on the frequency synthesizer output utilizing either technique is discussed below.

A. Multiphase Fractional Division Technique

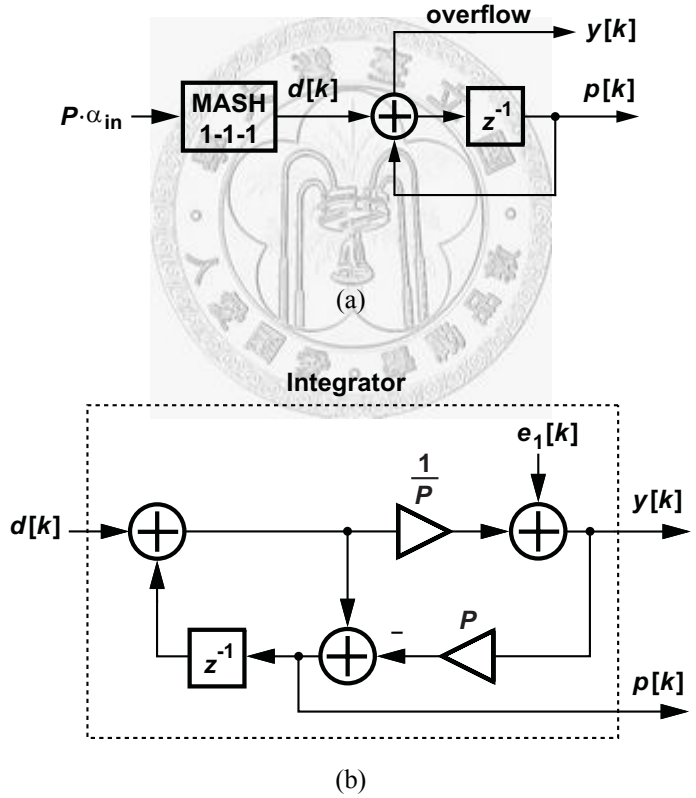


Figure 4.5 (a) Architecture of a multiphase fractional division modulator. (b) Linear model of the integrator.

In general, multiphase fractional division modulators are constructed with a single Σ-Δ modulator followed by an integrator, as shown in figure 4.5(a). The carry out signal *y[k]*

controls the divider to produce a division value $N+y[k]$. Note that the operation of the integrator is equivalent to a first-order error-feedback Σ-Δ modulator [26], indicated in figure 4.5(b), where $e_1[k]$ represents the quantization error of the error-feedback modulator. Further, the reason for the multiply factors $1/P$ and P is because the overflow signal occurs each time the integrator exceeds P, which is defined as T_{VCO}/τ. Now, the relationship between MASH 1-1-1 modulator signal $d[k]$ and $y[k]$, can be described as

$$\begin{aligned} y[k] &= \frac{1}{P} \cdot d[k] + \left(e_1[k] - e_1[k-1]\right) \\ &= \frac{1}{P} \cdot \left(P \cdot \alpha_{in} + Q_3[k]\right) + \left(e_1[k] - e_1[k-1]\right) \end{aligned}, \tag{4.6}$$

where $Q_3[k]$ is the output quantization noise of the third-order MASH 1-1-1 modulator which has a third-order noise shaped characteristic. In (4.6), a fractional division α_{in} plus an error term controls the division of divider. The error term in $y[k]$ causes a phase deviation at the output of the divider and is derived as

$$\Phi_n`[k] = \frac{2\pi}{P \cdot N_{nom}} \cdot \sum_{i=0}^{k} \left[Q_3[i] + P \cdot \left(e_1[i] - e_1[i-1]\right) \right], \tag{4.7}$$

where N_{nom} represents the nominal division value of divider [6]. Furthermore, in figure 4.5(a) the signal $p[k]$ decides the number of subcircuits in delay line 1 to operate by its

slow path. Thus if the delay units contain a gain error factor γ, a total additional delay time $\tau \cdot \gamma \cdot p[k]$ is contributed by delay line 1. The total additional delay time can be equivalently converted into an additional phase expression

$$\begin{aligned} \Phi_{\text{delay line 1}}[k] &= \frac{2\pi}{T_{\text{VCO}} \cdot N_{\text{nom}}} \cdot \gamma \cdot \tau \cdot p[k] \\ &= \frac{2\pi}{P \cdot N_{\text{nom}}} \gamma \cdot \left(-P \cdot e_1[k]\right) \end{aligned}, \tag{4.8}$$

where $p[k]$ equals $-P \cdot e_1[k]$, as shown in figure 4.5(b). By summing (4.7) and (4.8), a total phase deviation contributed by divider and delay line 1 is obtained as

$$\begin{aligned} \Phi_n[k] &= \frac{2\pi}{P \cdot N_{\text{nom}}} \cdot \left\{ \sum_{i=0}^{k} \left[Q_3[i] + P \cdot \left(e_1[i] - e_1[i-1] \right) \right] + \gamma \cdot \left(-P \cdot e_1[k] \right) \right\}. \\ &= \frac{2\pi}{P \cdot N_{\text{nom}}} \cdot \left\{ \sum_{i=0}^{k} \left(Q_3[i] \right) + (1-\gamma) \cdot P \cdot e_1[k] \right\} \end{aligned} \tag{4.9}$$

Now the power spectral density of the phase deviation can be written as

$$S_{\Phi_n}(f) = \left(\frac{2\pi}{P \cdot N_{\text{nom}}} \right)^2 \cdot \left[\left(\frac{1}{2\sin(\pi f T)} \right)^2 \cdot S_{Q_3}(f) \cdot + (1-\gamma)^2 \cdot P^2 \cdot S_{e_1}(f) \right] \cdot \tag{4.10}$$

Ideally, quantization error is uniform distributed between 0 and 1, and are modeled as an

additive white noise source so that their power spectrum is flat with magnitude 1/12 [6]. Thus, (4.10) can be rewritten as

$$S_{\Phi_n}(f)=\left(\frac{2\pi}{P\cdot N_{\text{nom}}}\right)^2\cdot\frac{1}{12}\cdot\left[\left(2sin(\pi fT)\right)^4+\left(1-\gamma\right)^2\cdot P^2\right]\cdot \tag{4.11}$$

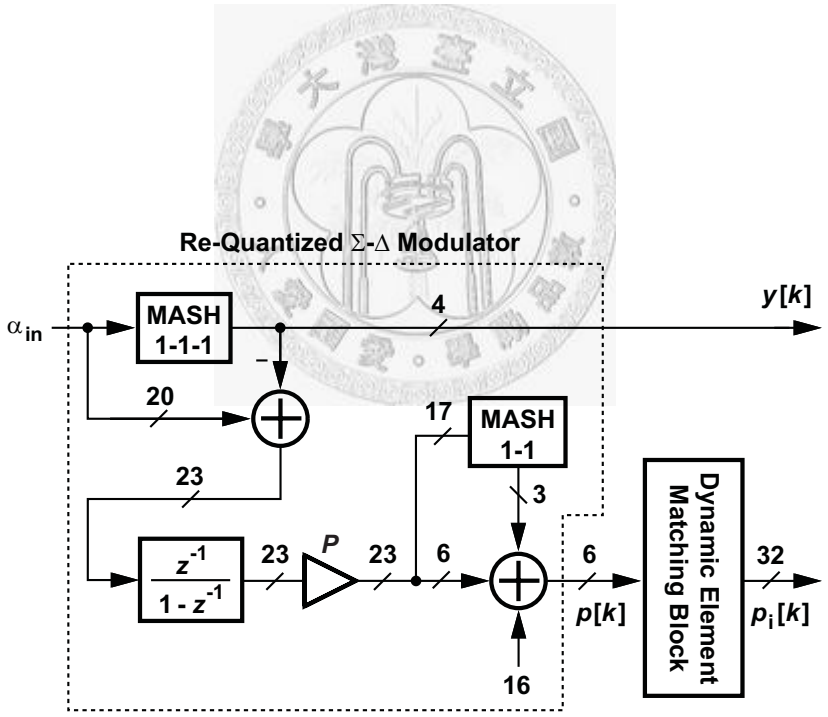
The power spectrum of phase deviation contains two noise components. One is caused by the quantization noise with a shaping factor $sin(\pi fT)^4$. As shown in (4.11), compared to the frequency synthesizers with no multiphase compensation, a $(1/P)^2$ or $20\cdot\log_{10}P$ (dB) reduction in power can be achieved. The other component is caused by gain error in delay units, the noise power spectrum caused by gain error shows a flat noise characteristic.

Finally, the effect of phase deviation caused by gain error in delay units to the frequency synthesizer output in multiphase fractional division techniques can be calculated as

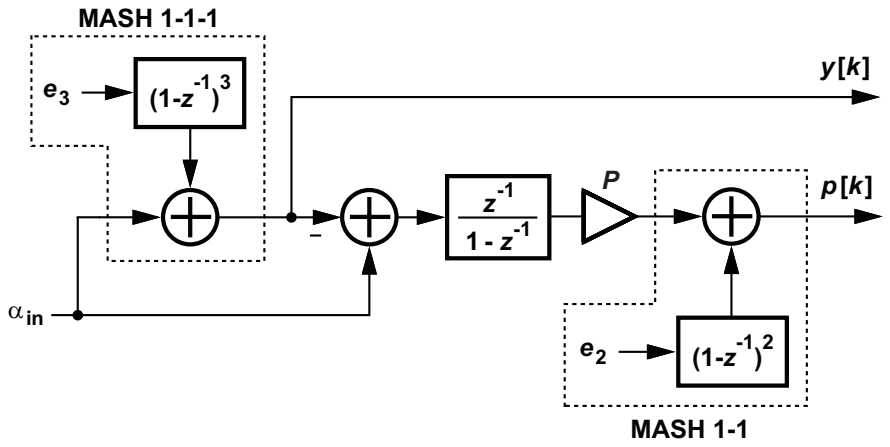
$$S_{\Phi_{\text{out}}}(f)\Big|_{\text{Gain Error}}=\frac{1}{T}\cdot\left|T\cdot N_{\text{nom}}\cdot G(f)\right|^2\cdot\left(\frac{2\pi}{P\cdot N_{\text{nom}}}\right)^2,\quad \cdot\frac{1}{12}\cdot\left[\left(1-\gamma\right)\cdot P\right]^2 \tag{4.12}$$

where T and $G(f)$ represents the input reference clock period and the closed-loop transfer function of the frequency synthesizer, respectively [6].

In summary, from (4.12) the effect of delay unit gain error equivalently introduces a flat noise into the frequency synthesizer that causes low-passed noise at the synthesizer output. Moreover, the assumption of $e_1[k]$ as an additional white noise may not be sufficient because the quantization error of a first-order MASH structure often shows a periodic feature. Thus, in addition to in-band noise, spurious tones will also occur at the frequency synthesizer output.



(a)



(b)

Figure 4.6 (a) Architecture of the proposed digital control circuit with re-quantized Σ-Δ modulator. (b) Linear model of the re-quantized Σ-Δ modulator.

B. Re-Quantized Σ-Δ Modulator Technique

Figure 4.6(a) shows the proposed digital control circuit diagram with re-quantized Σ-Δ modulator. Two MASH Σ-Δ modulators are constructed in the re-quantized modulator, where the first one is a third-order MASH 1-1-1 modulator and the second one is a second-order MASH 1-1 modulator. A 20-bit fractional word is applied to the MASH 1-1-1 modulator, and the output *y[k]* controls the divider to produce a division value *N+y[k]*, where

$$y[k] = \alpha_{in} + Q_3[k] \cdot \tag{4.13}$$

$Q_3[k]$ is the same as those defined previously, which represents the output quantization noise caused by MASH 1-1-1 modulator and has a third-order noise shaped characteristic. In (4.13), a fractional word α_{in} plus an error term controls the division of divider. The error term in $y[k]$ causes a phase deviation at the output of the divider that can be derived as

$$\Phi_n`[k] = \frac{2\pi}{N_{nom}} \cdot \sum_{i=0}^{k} (Q_3[i]) \cdot \tag{4.14}$$

Shown in figure 4.6(a), the output of MASH 1-1-1 is subtracted with the input fractional word α_{in} to obtain $-Q_3[k]$. The subtracted value is then integrated to achieve the summation term in (4.14) but with negative polarity. Ideally, if this negative term can be applied to compensate (4.14) by controlling the amount of additional delay time in delay line 1, quantization error effect could be totally eliminated. However, since MASH 1-1-1 is operated with a 20-bit fractional division, a unit delay time τ of $T_{VCO}/2^{20}$ would be required. If the VCO operates at a frequency of 2.14 GHz for example, a unit delay time of 0.000446 psec would be needed. Such a delay-locked loop and delay line 1 would be infeasible for any available technologies. In the proposed work, an 18-dB reduction is required for our frequency synthesizer, which is equivalent to 1/8 reduction on quantization error or suppressing the 3 MSBs of the quantization error, thus an unit delay time of 58.4 psec is

needed, which is designed in our delay-locked loop and delay line 1. The remaining 17-bit errors will be truncated by means of the MASH 1-1 modulator.

The output of integrator is then multiplied by *P*, which is defined previously as the ratio between T_{VCO} and unit delay time τ, and is equal to 8 in this work. Note that a multiplication of 8 can be derived easily by shifting the binary word 3 bits leftward. The multiplied signal is then divided into two components, an integer component of 6 bits and a fractional component of 17 bits, respectively. The 17-bit fractional component is re-quantized by a second-order MASH 1-1 Σ-Δ modulator. Finally, the output signal *p[k]* is constructed by adding the 6-bit integer component with the output of the second Σ-Δ modulator. As shown in figure 4.6(a), an integer number of 16 is also added to *p[k]*. This is to insure the output signal *p[k]* to be positive, since in PLL based frequency synthesizers, a constant delay time added on the feedback signal to PFD would not affect the performances of the synthesizer. Note, the number 16 is determined through simulation results, this will be explained later with the discussion of the number of delay units needed in delay line 1.

Figure 4.6(b) shows the linear model of the re-quantized Σ-Δ modulator. The output signal *p[k]* decides the number of subcircuits in delay line 1 to pass its input signal through

slow path. If the delay units are ideal, a total additional delay time $\tau \cdot \gamma \cdot p[k]$ can be achieved by delay line 1. The total additional delay time can be equivalently converted into an additional phase expression

$$\begin{aligned} \Phi_{\text{delay line 1}}[k] &= \frac{2\pi}{P \cdot N_{\text{nom}}} \cdot \gamma \cdot p[k] \\ &= \frac{2\pi}{P \cdot N_{\text{nom}}} \cdot \gamma \cdot \left(P \cdot \sum_{i=0}^{k} (-Q_3[i]) + Q_2[k] \right) \end{aligned} , \tag{4.15}$$

where $Q_2[k]$ represents the output quantization noise caused by the MASH 1-1 modulator which has a second-order noise shaped characteristic. By summing (4.14) and (4.15), a total phase deviation contributed by divider and delay line 1 can be calculated as

$$\Phi_n[k] = \frac{2\pi}{P \cdot N_{\text{nom}}} \cdot \left\{ P \cdot (1-\gamma) \cdot \sum_{i=0}^{k} Q_3[i] + \gamma \cdot Q_2[k] \right\} \cdot \tag{4.16}$$

Therefore, the power spectral density of the phase deviation can be written as

$$S_{\Phi_n}(f) = \left(\frac{2\pi}{P \cdot N_{\text{nom}}} \right)^2 \cdot \frac{1}{12} \cdot (2\sin(\pi f T))^4 \left[\gamma^2 + (1-\gamma)^2 \cdot P^2 \right] \cdot \tag{4.17}$$

In (4.17), the power spectrum of phase deviation also contains two noise components, such as (4.11), one caused by quantization noise and the other caused by delay unit gain error.

However, in (4.17), both components are shaped by the filter $sin(\pi fT)^4$. While in (4.11), with multiphase fractional division technique, delay unit gain error generates flat noise in the frequency synthesizer.

Finally, the effect of phase deviation caused by delay unit gain error to the frequency synthesizer output in re-quantized Σ-Δ modulator technique can be calculated as

$$S_{\Phi_{out}}(f)\Big|_{\text{Gain Error}} = \frac{1}{T}\cdot\left|T\cdot N_{\text{nom}}\cdot G(f)\right|^2\cdot\left(\frac{2\pi}{P\cdot N_{\text{nom}}}\right)^2\cdot \left(2sin(\pi fT)\right)^4\cdot\frac{1}{12}\cdot\left[(1-\gamma)\cdot P\right]^2 \quad (4.18)$$

According to (4.17) and (4.18) the effect of delay unit gain error equivalently introduces a white noise filtered by a second-order high-pass filter on the frequency synthesizer output. Compared with the results in (4.11) and (4.12) using multiphase fractional division technique, the in-band noise and spurious tones can thus be avoided.

Now, the number of subcircuits needed in delay line 1 to produce proper additional delay intervals is analyzed. The number of subcircuit needed is directly proportional to the quantization error caused by the first Σ-Δ modulator MASH 1-1-1, which causes phase deviation at the divider output, and inverse proportional to the delay time of a unit delay

element, that is

$$T_{VCO} \cdot N_{nom} \cdot \frac{(\Phi_n`[k]_{max} - \Phi_n`[k]_{min})}{2\pi} \cdot \frac{1}{\tau} \cdot = P \cdot N_{nom} \cdot \frac{(\Phi_n`[k]_{max} - \Phi_n`[k]_{min})}{2\pi} \tag{4.19}$$

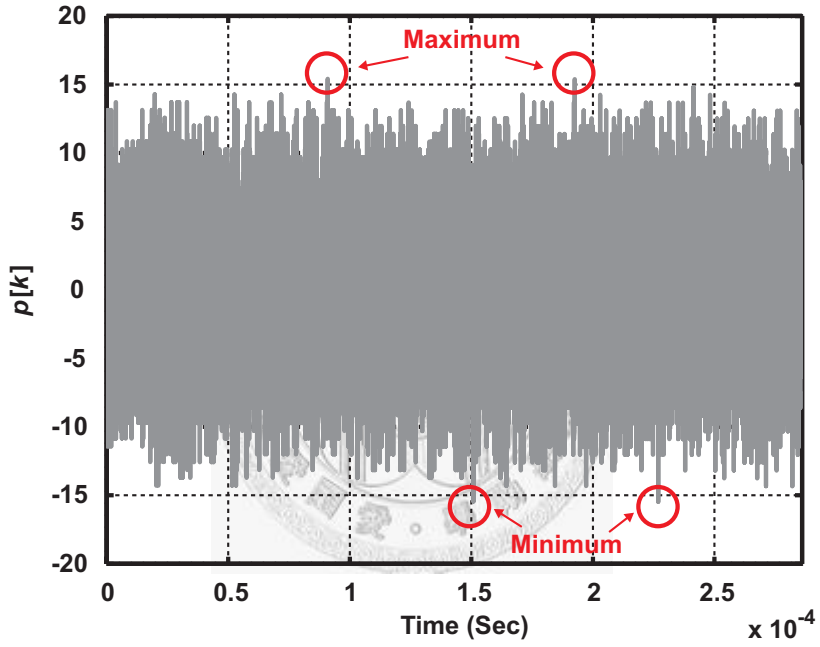


Figure 4.7 Behavioral simulation result of re-quantized Σ-Δ modulator output signal *p[k]*, without adding constant integer 16.

However, the exact number should be obtained through behavioral simulation, and observing the dynamic range of the output signal *p[k]*. Figure 4.7 shows the behavioral simulation results of a re-quantized Σ-Δ modulator. The output signal *p[k]* is in the range of +16~-16 without adding the constant number 16 previously mentioned. Thus, 32

subcircuits are required in delay line 1 for multiphase compensation utilizing the re-quantized Σ-Δ modulator proposed in figure 4.6(a).

4.2.3 Dynamic Element Matching Technique

Refer to the subcircuit model shown in figure 4.4(b), ideally all the delay units are equal with a delay time τ, but due to mismatches, they have a random distribution. To simplify the analysis, only the effect of delay mismatch m_i is considered. During each reference cycle, certain amount of subcircuits in delay line 1 is selected. The selected subcircuits operate with its slow path which contributes an additional delay time for compensating the quantization noise. A mismatch value *m[k]* can be defined as the deviation time from the ideal delay time at the output of delay line 1. Thus, *m[k]* can be equivalently derived by summing up all m_i of the delay units in each selected subcircuit. A simplest way of choosing the subcircuits is by thermometer code. Therefore, the mismatch value at the delay line 1 output can be described as

$$\begin{aligned} m[k] &= \sum_{i=0}^{p[k]-1} p_i[k] \cdot m_i \\ &= \sum_{i=0}^{p[k]-1} m_i \end{aligned}, \qquad (4.20)$$

where $p_i[k]$ is a one-bit signal that controls the i^{th} subcircuit in delay line 1, and has the value of either 0 or 1. If $p_i[k]$ equals to 0, the subcircuit operates with its fast path, on the other hand, if $p_i[k]$ equals to 1, the subcircuit operates with its slow path. Assume $p[k]$ is a random number, and the multiphase mismatch value $m[k]$ in (4.20) can be modeled as a random process with white noise spectrum. Thus, the noise power caused by multiphase mismatch of delay line 1 can be obtained as

$$S_m(f) = \left(\frac{2\pi}{8 \cdot N_{nom}} \cdot \frac{\sigma_m}{T_{VCO}/8} \right)^2 = \left(\frac{2\pi}{N_{nom}} \cdot \frac{\sigma_m}{T_{VCO}} \right)^2, \tag{4.21}$$

where σ_m represents the standard diviation of $m[k]$. And the effect of mismatch noise to the frequency synthesizer output can be derived as

$$\begin{aligned} S_{\Phi_{out}}(f)\Big|_{\text{Mismatch Noise}} &= \frac{1}{T} \cdot \left| T \cdot N_{nom} \cdot G(f) \right|^2 S_m(f) \\ &= \frac{1}{T} \cdot \left| T \cdot N_{nom} \cdot G(f) \right|^2 \cdot \left(\frac{2\pi}{N_{nom}} \cdot \frac{\sigma_m}{T_{VCO}} \right)^2 \end{aligned} . \tag{4.22}$$

From (4.22), if the subcircuits are chosen by thermometer code, the mismatch noise $m[k]$ in spectrum will be a flat noise that causes in-band noise and spurious tones at the frequency synthesizer output.

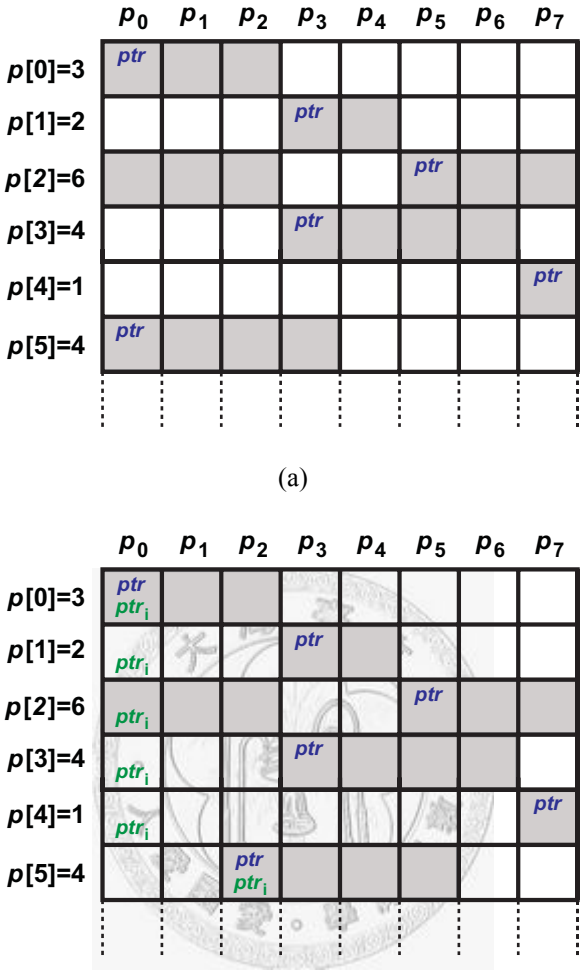


Figure 4.8 (a) Example of data weighted averaging algorithm. (b) Example of data weighted averaging algorithm with increased index.

Dynamic element matching is a technique for oversampled digital to analog converters to improve their linearity. The purpose of DEM is to select elements such that mismatch noise can be pushed away to high offset frequency where it can be removed by filtering. As shown in figure 4.2 and figure 4.3, in the proposed multiphase compensation frequency

synthesizer with delay line 1, DEM techniques can be employed to select the subcircuit in delay line 1 to push the mismatch noise to high offset frequencies.

Many DEM algorithms, including random selection, individual level averaging, data weighted averaging [25], and segmented encoder [27], were reported. In the proposed frequency synthesizer, a DEM technique utilizing data weighted averaging (DWA) is employed to yield a first-order shaping of the mismatch noise. In figure 4.8(a), the selection of the subcircuits in DWA is shown. For convenience, eight subcircuits are used in this example. During each clock cycle, a number of subcircuit corresponding to the input code *p[k]* is selected clockwise, starting from the position indicated by a pointer *ptr*, with $0 \leq ptr < L$, where L is the number of subcircuits in delay line 1. At each clock cycle, the pointer is updated by incremented modulo L with the input code. On the next cycle, the selection will start from the new position of the pointer. The concept is to select all the delay units in the fasted way, since the sum of the mismatch of all delay units is zero. This ensures the low frequency noise components to be minimized. Mathematically, the mismatch noise *m[k]* due to DWA selection can be expressed as [24] [25]

$$\begin{aligned} m[k] &= \sum_{i=0}^{ptr[k]-1} m_i - \sum_{i=0}^{ptr[k-1]-1} m_i \\ &= IM[ptr[k]] - IM[ptr[k-1]] \end{aligned} \quad . \tag{4.23}$$

The function *IM[ptr]*, called integral mismatch, corresponds to the mismatches of the delay units accumulated along the array up to the position of the pointer. Now the power spectrum of the mismatch noise in (4.23) can be written as

$$S_{\mathrm{m}}(f)=\left(2sin(\pi fT)\right)^2\cdot\left(\frac{2\pi}{N_{\mathrm{nom}}}\cdot\frac{\sigma_{\mathrm{m}}}{T_{\mathrm{VCO}}}\right)^2\cdot \tag{4.24}$$

Where, the integral mismatch function *IM[ptr]* is assumed to be white random process with a standard deviation σ_{m}. Therefore, the effect of mismatch noise to the frequency synthesizer output can be derived as

$$S_{\Phi_{\mathrm{out}}}(f)\Big|_{\text{Mismatch Noise}}=\frac{1}{T}\cdot\left|T\cdot N_{\mathrm{nom}}\cdot G(f)\right|^2\left(2sin(\pi fT)\right)^2\cdot\left(\frac{2\pi}{N_{\mathrm{nom}}}\cdot\frac{\sigma_{\mathrm{m}}}{T_{\mathrm{VCO}}}\right)^2\cdot \tag{4.25}$$

While DWA has the advantage of noise shaping the spectrum of delay mismatches, it also creates spurious tone. A $F_{\mathrm{ref}}/2$ tone has been observed in behavioral simulations. This fractional tone occurs because the average number of subcircuits selected to operate with slow path in a reference cycle is $L/2$. Thus, all subcircuits in delay line 1 will be selected once in an average of two reference cycles. Further, since the sum of the mismatch of all delay units is zero, a periodic mismatch noise of period $2T_{\mathrm{ref}}$ occurs.

To resolve this problem, a simple modification in DWA mechanism has been presented, named data weighted algorithm with increased index (DWA_{inc}). In figure 4.8(b), the selection of the subcircuits in DWA_{inc} is shown. The algorithm of DWA_{inc} is similar to DWA. In addition to the pointer *ptr*, another pointer ptr_i is applied, same with $0 \leq ptr_i < L$. Initially, ptr_i is set to zero, during each clock cycle, if *ptr* is not equal to ptr_i, the subcircuit selection will be the same as DWA. But if *ptr* equals to ptr_i at the beginning of a clock cycle, a random number will be assigned to both *ptr* and ptr_i, and the subcircuit selection will continue by the new *ptr*. For example, in figure 4.8(b), initially both *ptr* and ptr_i are 0, the selection starts from the subcircuit p_0 and proceeds in a rotational manner such as DWA. However, in the fifth clock cycle, the subcircuit selection ends at p_7 and sets *ptr* to zero. Therefore, at the beginning of the sixth clock cycle an equivalent value of *ptr* and ptr_i is detected, thus a new random value 2 is assigned to them and the subcircuit selection proceeds from p_2. In behavioral simulation, great reduction on the $F_{ref}/2$ tone has been detected, with the expense of little in-band noise increment compared to DWA. But still much lower than those with no dynamic element match technique applied.

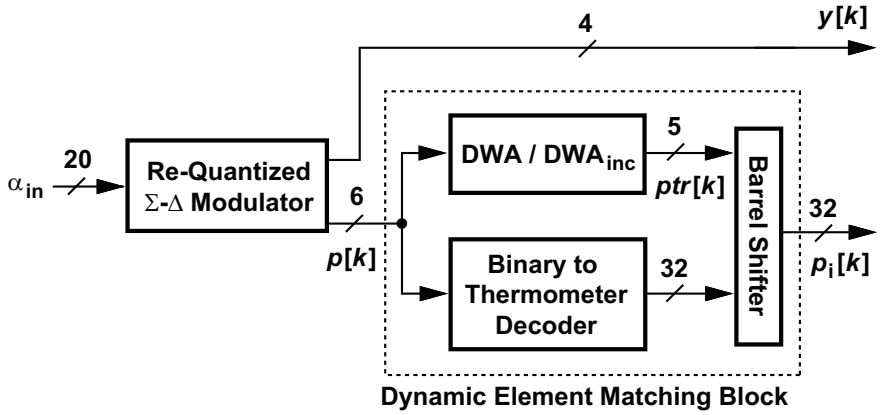


Figure 4.9 Architecture of the proposed digital control circuit with DEM block.

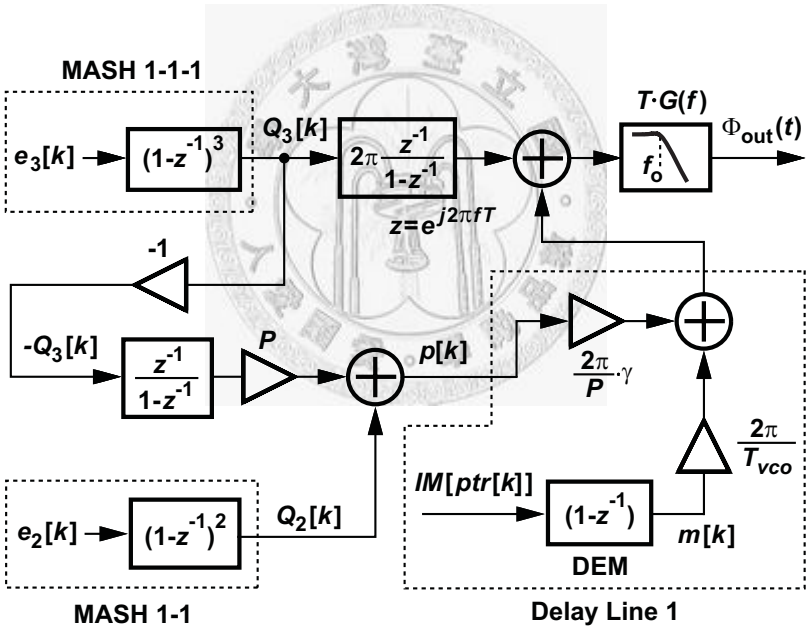


Figure 4.10 Linear model of a multiphase compensation Σ-Δ frequency synthesizer.

Figure 4.9 shows the proposed digital control circuit with DEM block. The two DEM algorithms, DWA and DWA_{inc} are both built in the digital control circuit. Finally, figure 4.10 shows a linear model of multiphase compensation Σ-Δ fractional-*N* frequency

synthesizers, including the effect of quantization noise, multiphase mismatch and delay unit gain error.

4.3 Behavioral Simulation

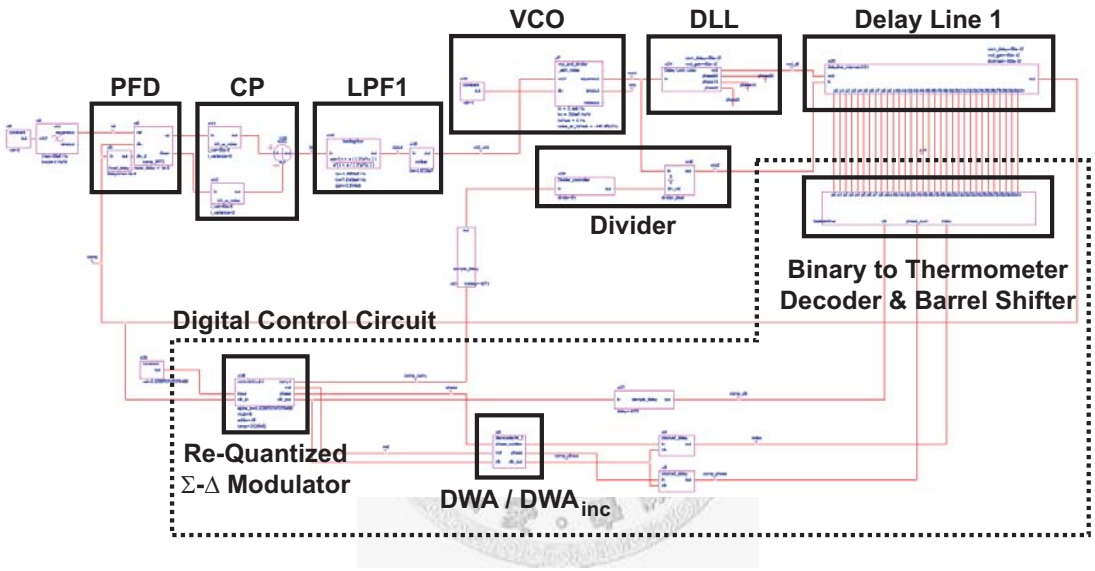


Figure 4.11 Behavioral model of the proposed multiphase compensation Σ-Δ fractional-*N* frequency synthesizer.

In order to verify the quantization noise suppression method proposed, a multiphase compensation Σ-Δ fractional-*N* frequency synthesizer was constructed in CPPsim [5] for behavioral simulation, shown in figure 4.11. Table 4.1 shows a summary of the designed loop parameters. VCO and detector noise sources are not considered in the behavioral simulation. Figure 4.12 depicts the simulation results of the frequency output phase noise, with and without multiphase compensation method applied. As shown, with ideal delay

units an 18-dB quantization noise reduction can be achieved.

Fractional-*N* Frequency Synthesizer Parameters	
Reference Frequency	35 MHz
Output Frequency	2.11GHz – 2.17GHz
Loop Bandwidth	200 KHz
Charge Pump Current	50 μA
VCO Gain	200 MHz/V

Table 4.1 Frequency synthesizer parameters.

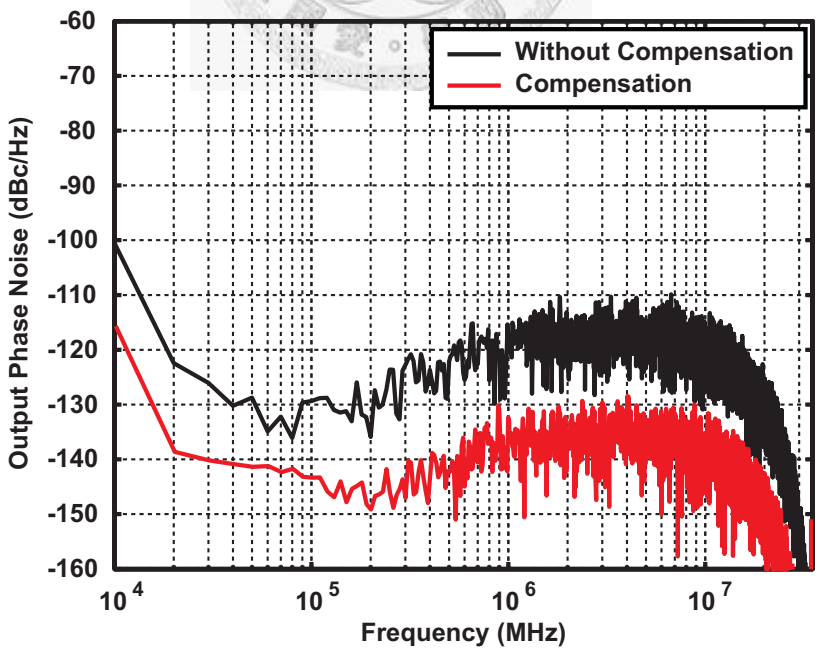


Figure 4.12 Multiphase compensation with ideal delay units.

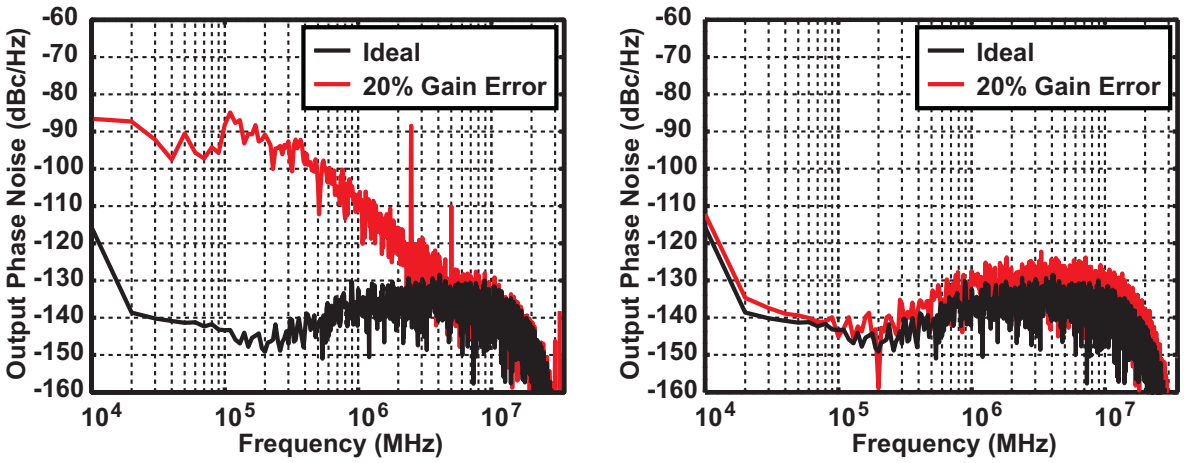


Figure 4.13 Multiphase compensation with 20% gain error in delay units.

Figure 4.13 depicts the simulation results of the frequency output phase noise, with 20% gain error in delay units, where γ= 80% and mismatch values m_i are set to 0. In figure 4.13(a), shows the results of a frequency synthesizer utilizing multiphase fraction division modulator as the control of divider and delay line 1 to produce fractional divisions. In-band noise and spurious tones due to delay cell gain error can be shown evidently, which was also derived in (4.11) and (4.12). On the contrary, figure 4.10(b) depicts the resultant output phase noise utilizing re-quantized Σ-Δ modulator in the frequency synthesizer. As mentioned in (4.17) and (4.18), delay cell gain error contributes noise power with second-order noise shaping characteristic in the frequency synthesizer.

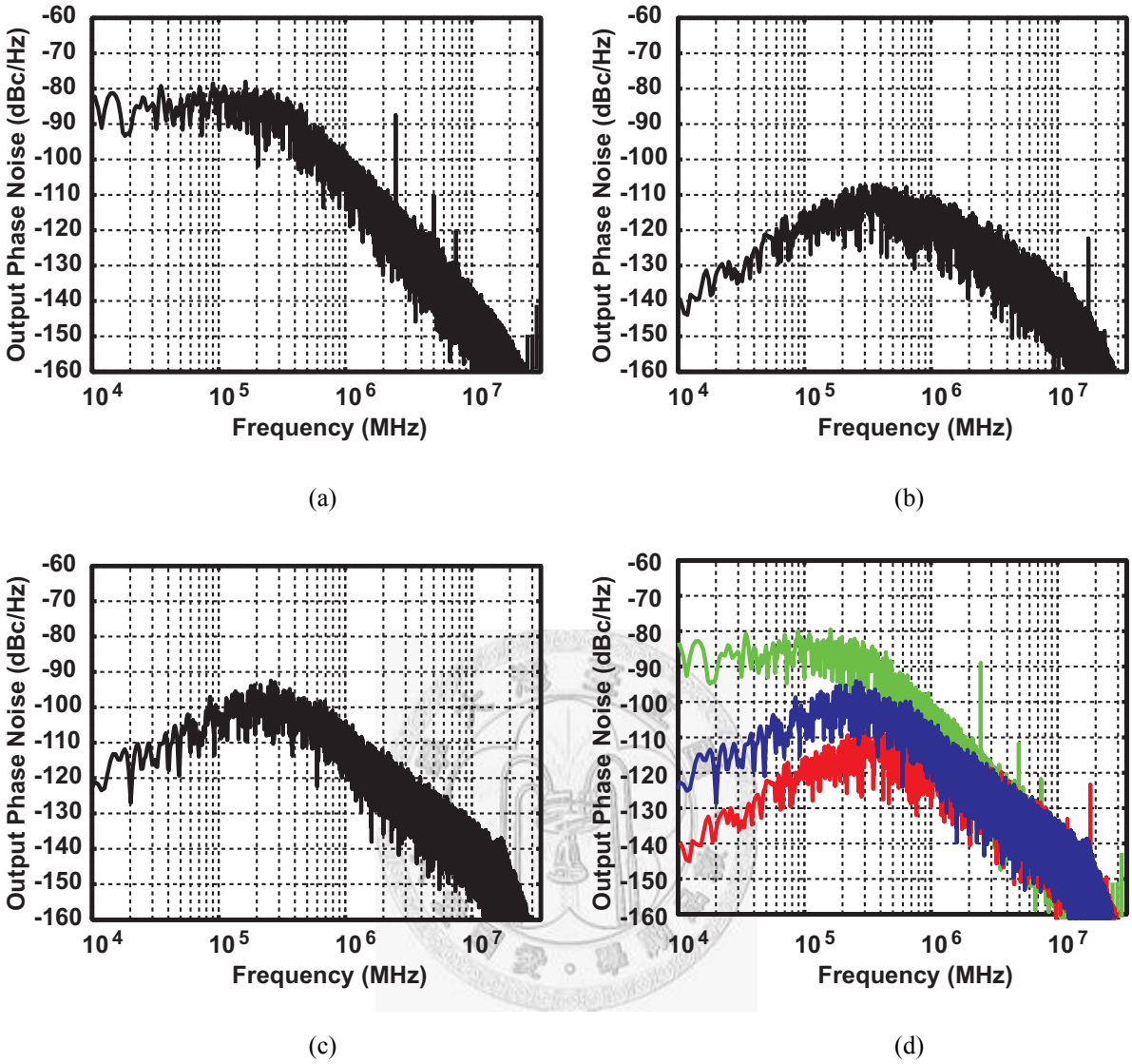


Figure 4.14 Multiphase compensation with multiphase mismatch $\sigma_m/\tau = 40\%$. (a) Thermometer code applied. (b) DWA technique applied. (c) DWA_{inc} technique applied. (d) Comparison of the three subcircuit selection techniques.

Figure 4.14 depicts the simulation results of the frequency synthesizer output phase noise, with multiphase mismatch. The mismatch values m_i are assigned by random numbers with 0 mean and $\sigma_m/\tau = 40\%$, where σ_m represents the standard deviation of the mismatch values. The gain error factor γ is set to 1. In figure 4.14(a), the output phase

noise without DEM techniques is depicted, where thermometer code are applied for subcircuit selection. As derived in (4.22), in-band noise and spurious tones occur at the synthesizer output. Figure 4.14(b) and 4.14(c) shows the output phase noise with DWA and DWA_{inc} activated, respectively. As mentioned in (4.24) and (4.25), with DWA technique applied for subcircuit selection the mismatch noise yields a first-order noise shaped characteristic thus reduces the in-band noise. However, a fractional tone at the frequency offset $F_{ref}/2$ will occur. By applying DWA_{inc} technique the $F_{ref}/2$ tone can be greatly reduced with a little expense of increasing in-band noise, but still much lower than those in figure 4.14(a), where thermometer code is applied for subcircuit selection. Finally, the comparison of the three subcircuit selection techniques is depicted in figure 4.14(c).

4.4 Circuit Implementation

This frequency synthesizer is implemented in a 0.18-μm CMOS technology, targeting the WCDMA specifications. All the blocks shown in figure 4.2 except the loop filter capacitors are implemented on-chip. Table 4.1 shows the designed loop parameters.

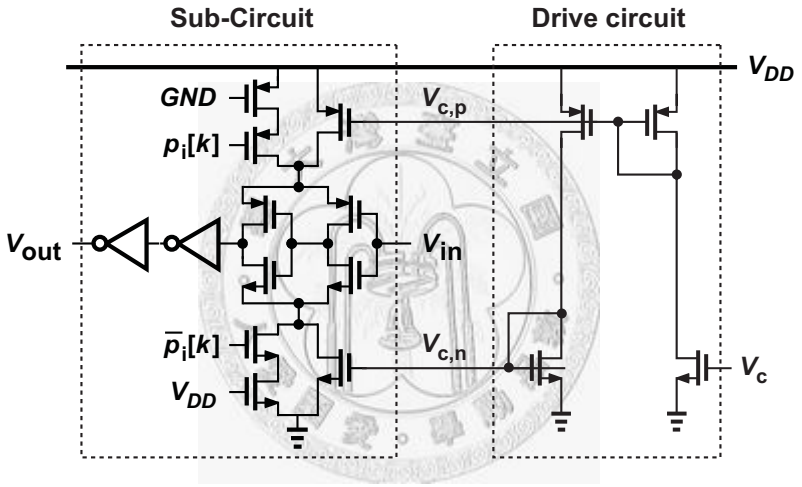


Figure 4.15 Schematic of the i^{th} subcircuit in delay line 1, and the driver circuit.

4.4.1 Subcircuits in Delay Line 1

An example of a subcircuit in delay line 1 is shown in figure 4.15. The subcircuit is implemented to generate the additional delay time τ. The selection of fast path and slow path is by setting $p_i[k]$ to 0 and 1, respectively. The delay line 1 consists of 32 subcircuits.

The delay units in delay line 2 of delay-locked loop shown in figure 4.2 are also constructed by the subcircuit in figure 4.15. Delay line 2 consists of 16 subcircuits, the 16 subcircuits are divided into two groups, each of which consists 8 subcircuits cascaded in line. The subcircuits in the first line operate by slow path, and input a 0-degree signal of a period $T_{VCO}/4$. The subcircuits in the second line operate by fast path, and input a 90-degree signal of a period $T_{VCO}/4$. The output signals of the two lines compare their phases at the phase frequency detector. Ideally, when delay-locked loop is in locked condition, the delay time difference between slow path and fast path of all subcircuits will be τ, or equivalently $T_{VCO}/8$.

The delay time of each subcircuit in both delay line 1 and delay line 2 are set the same by sharing the same voltage control signal V_c.

4.4.2 Divider

Shown in figure 4.16, the core of the frequency divider is a pulse-swallow divider. The pulse-swallow divider consists of a dual-modulus prescaler, a fixed-ratio program counter and a programmable swallow counter. The prescaler is built with current-mode logic (CML), and the other two counters are built with static CMOS logic. The output of the

prescaler drives a level shifter buffer to produce rail-to-rail signals for the following stages. The overall divide ratio is equal to *NP*+*S*. In this work, N=4, P=14, S=1~16, so the total divided ratio can be varied from 57 to 72.

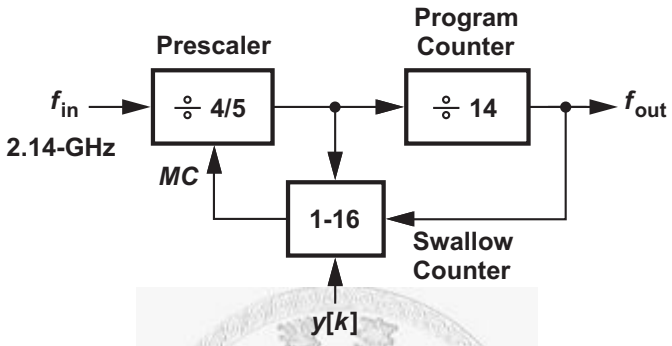


Figure 4.16 Architecture of the multi-modulus divider.

A divided-by-4 circuit consist of TSPC flip-flops is also implemented in the divider, and is not depicted in figure 12. The purpose of the divided-by-4 circuit is to generate two quadrature signals with a period of $T_{VCO}/4$ for the delay-locked loop inputs.

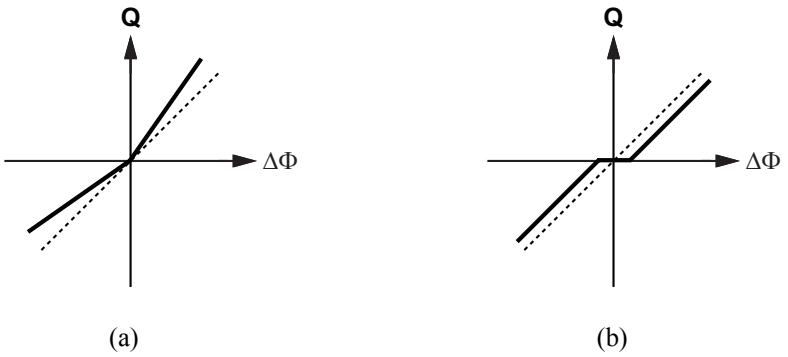


Figure 4.17 PFD-CP nonlinear I/O characteristic. (a) Current source mismatch. (b) Dead zone.

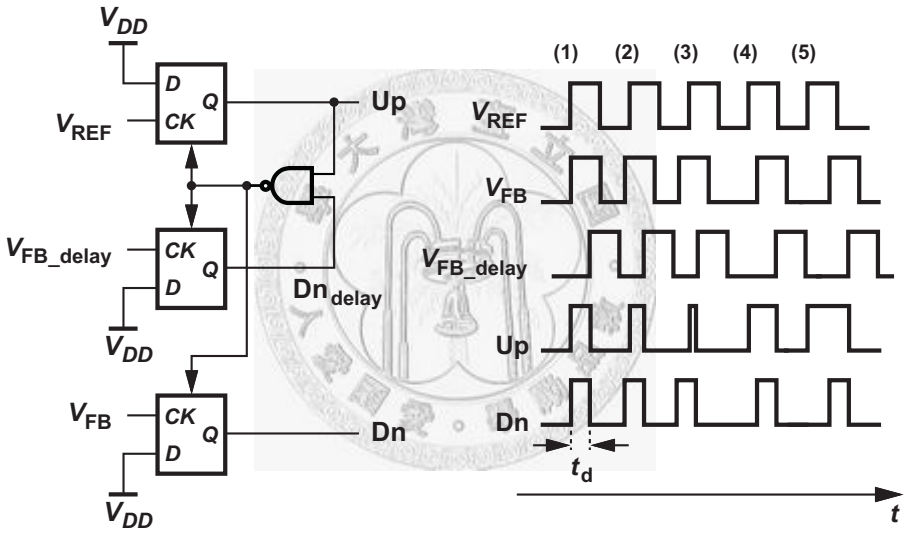


Figure 4.18 Architecture of phase frequency detector, and the constant current pulse circuit.

4.4.3 Phase-Frequency Detector (PFD)

Besides the nonideal effect of multiphase mismatch, nonlinearity in the PFD-CP I/O characteristic also increases in-band noise and spurious tone. Typical PFD-CP nonlinearity shown in figure 4.17, include current source mismatch between up and down currents, and

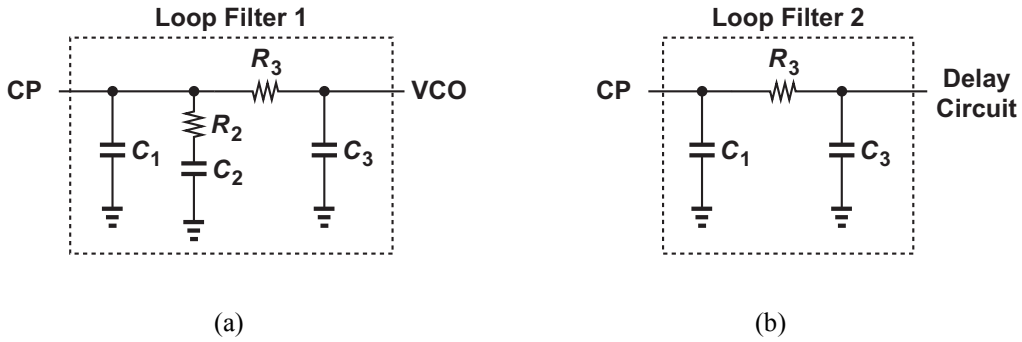
dead zone. The solid lines represent nonlinear circuit, and the dashed lines represent the idea ones. Q and $\Delta\Phi$ represents the amount of charge injected into the loop filter and input phase error of PFD-CP, respectively. To resolve the nonlinearity problem, a simple way is to inject a dc current into the loop filter. This forces the lock point of the PLL no longer at 0-degree of phase error and, thus, the residual nonlinearity near 0-degree phase error can be avoided. However, the method of injecting dc current into the loop filter increases the reference spurs.

Another solution is by the injection of periodic current pulses into the loop filter. The ideal is to yield a constant down current pulse, and allow the width of the up current pulses to vary with the input phase error. By this method, the operation of PFD-CP can be forced outside the nonlinear region. Figure 4.18 shows the proposed modified PFD architecture and the timing diagram of the signals in the PFD-CP in locked condition. The *Up* and *Dn* signals controls the up and down currents of CP, respectively. As shown, an additional D-Flip-Flop (DFF) is introduced. Unlike conventional tri-state PFD, in the proposed circuit, the DFF reset signal is controlled by the signals *Up* and Dn_{delay}, when both of them are high, the output of the NAND logic becomes low and the three DFF are reset. On the contrary, in conventional tri-state PFD the reset signal is controlled by the signals *Up* and *Dn*. The Dn_{delqy} signal is triggered by the rising edge of input signal $V_{\text{FB\_dely}}$. A delay line

circuit which is not depicted in figure 4.18, generates V_{FB_delay} which is a replica of V_{FB} with the delay time t_d. The combination of V_{FB} and V_{FB_delay} guarantees a constant down current periodically injected to the loop filter with a pulse width of t_d. The delay time t_d is designed long enough to force the PFD away from its nonlinear region.

4.4.4 VCO

The VCO is built with a negative-g_m CMOS LC oscillator, consisting of a differential spiral inductor and two MOS varactors. To have wide tuning range and small VCO gain, coarse digital tuning is provided by 3-bit binary weighted switching MIM capacitors, the capacitors values are 200 pF, 400 pF, and 800 pF. The VCO is designed to provide tuning range over a 0.4-1.4V range with a nominal K_{VCO} of 200 MHz/V.



(a) (b)

Figure 4.19 (a) Third-order passive loop filter of frequency synthesizer. (b) Second-order passive loop filter of delay-locked loop.

4.4.5 Loop Filter

A third-order passive loop filter is implemented as the frequency synthesizer loop filter, shown in figure 4.19(a). The loop filter components are as follows: C_1 = 30 pF, C_2 = 422 pF, C_3 = 3 pF, R_2 = 7.5 KΩ, and R_3 = 4.5 KΩ, of which R_2, C_1, and 15 pF of C_2 are off-chip. The remaining of 15 pF of C_2 is on chip to help reduce the voltage variation caused by fast charge pump current switching through the inductive bond wires. Given that the VCO gain is 200 MHz/V, the divider modulus is around 61, and the charge pump current is 50μA, the proposed frequency synthesizer bandwidth is approximately 200KHz.

Another second-order passive loop filter, which is fabricated on-chip, is constructed as the DLL loop filter, shown in figure 4.19(b). The loop filter components are as follows: C_1 = 1 pF, C_2 = 1 pF, and R_2 = 1 KΩ.

4.5 Experimental Results

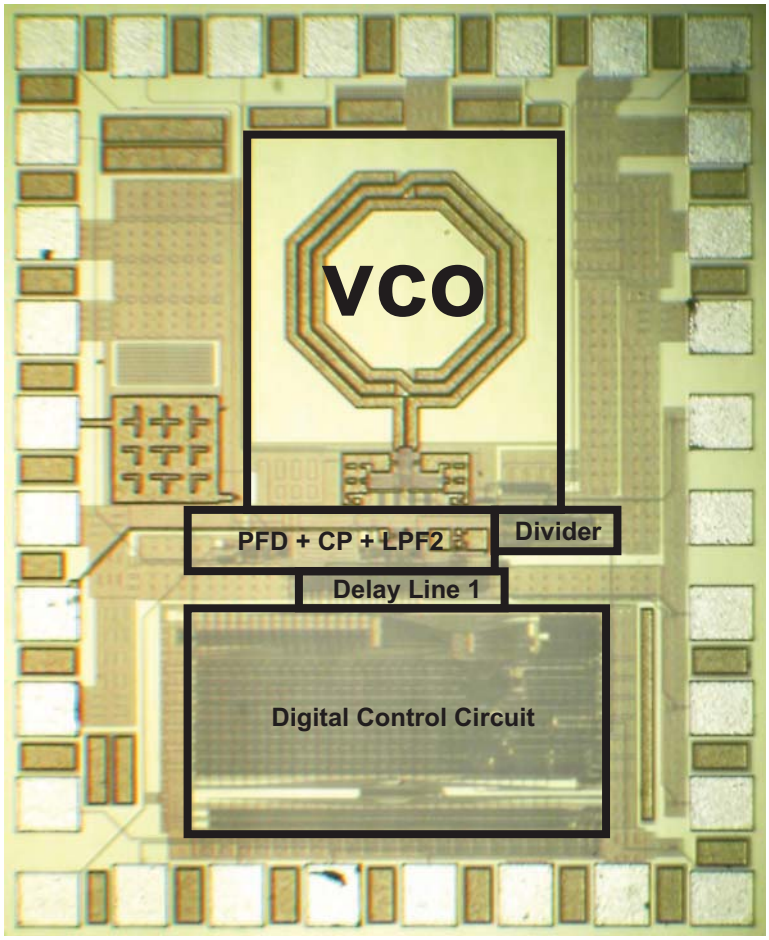


Figure 4.20 Die photo of the frequency synthesizer.

The proposed frequency synthesizer is fabricated in a 0.18-μm CMOS technology. The die photo of the chip is shown in figure 4.20. The die area is 0.92 mm × 1.15 mm (1 mm^2) including the measurement pads. The chip is tested on an evaluation printed circuit board. The total power consumption is 27.2 mW. All digital control signals are supplied through the three-wire serial interface, and the reference frequency used is 35 MHz.

The frequency synthesizer is tested in four different operation modes: without multiphase compensation method, multiphase compensation without DEM techniques, multiphase compensation with DWA and, multiphase compensation with DWA_{inc}, respectively. Figure 4.21 shows the frequency synthesizer output spectrum in locked condition. Figure 4.22 shows the synthesizer output phase noise, with and without multiphase compensation. As shown in figure 4.22, with quantization noise compensation technique, a 10-dB reduction of phase noise at the offset frequency of 10 MHz from a 2.14 GHz carrier signal can be achieved. The 10-dB reduction rather than an 18-dB reduction is caused by the high noise floor at 10 MHz frequency offset rather than the quantization noise.

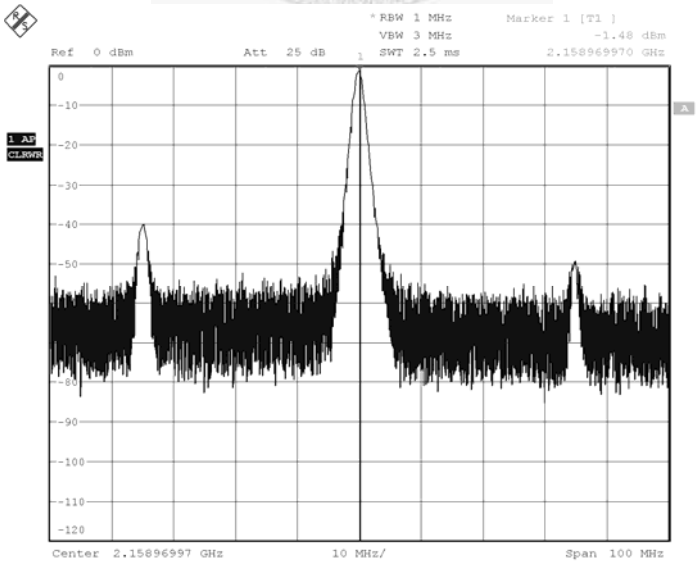


Figure 4.21 Output spectrum of the frequency synthesizer.

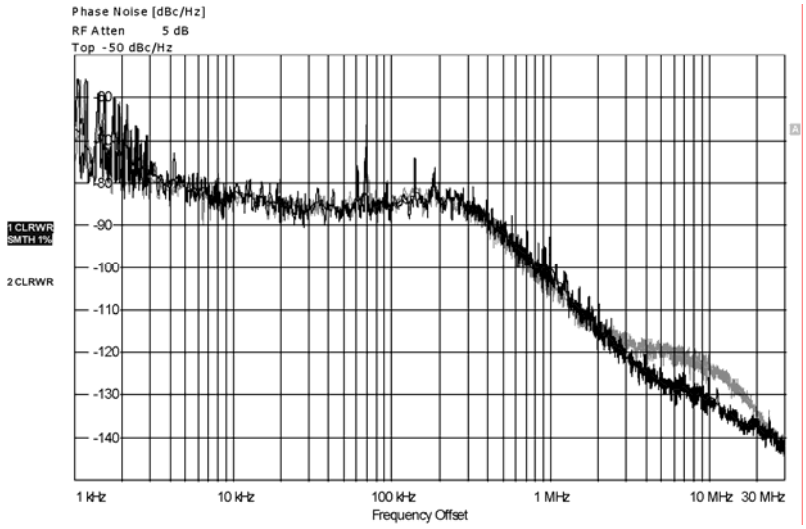
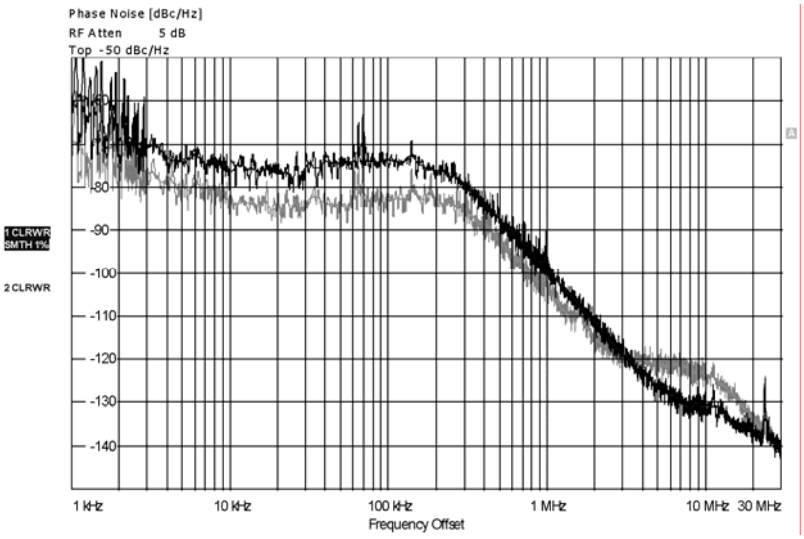


Figure 4.22 Phase noise measurement results, without multiphase compensation (light) and with multiphase compensation (dark) and.

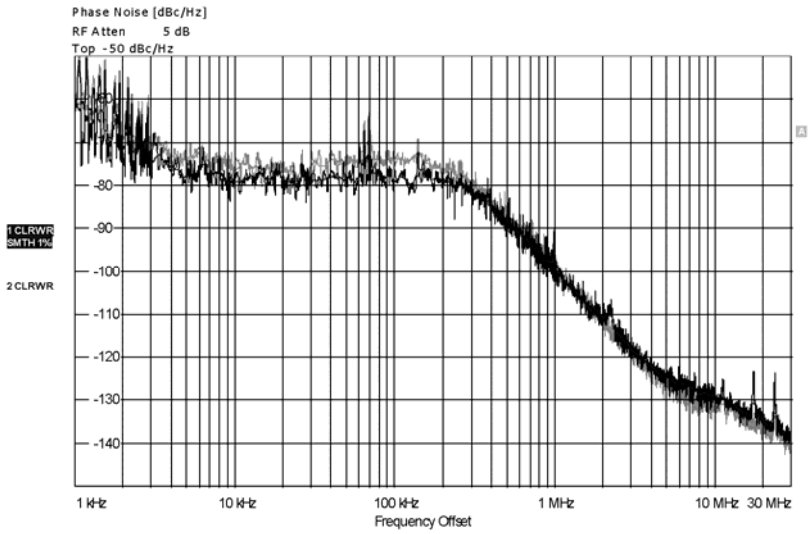
For the measurement results of multiphase compensation method with DEM techniques activated and deactivated, the measured in-band noise floor is -82 dBc/Hz for all three compensation modes. These measurement results correspond to an amount of up to 40% delay mismatches. Therefore, possible noise sources, such like noise from CP current source, nonlinear PFD+CP I/O characteristic and, digital circuit noise, might have been folded back to low offset frequencies and thus dominates the in-band noise.

Although the in-band noise now dominates by various noise sources rather than multiphase mismatch, in order to demonstrate the effect of DEM techniques, the measured

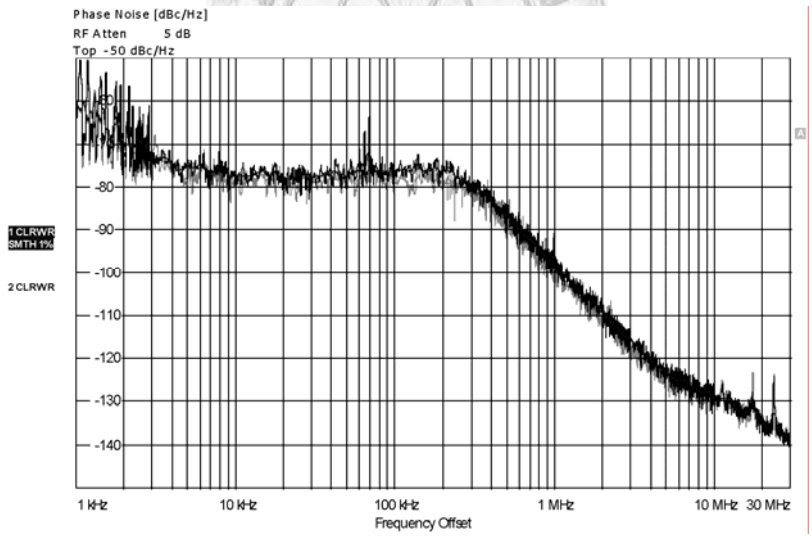
phase noise performance improvement can be observed by manually setting signal V_c=0.7. Note, in ordinary, V_c is generated by the locked delay-locked loop. The idea here is to manually lower the potential of V_c to increase the delay time mismatches, which has been verified in transistor-level simulations. Shown in figure 4.23(a), 10-dB in-band noise increment due to multiphase compensation without DEM technique is detected compared to the case with no compensation applied. In figure 4.23(b), shows a 4-dB in-band noise reduction due to DWA technique compared to the case with no DEM technique applied. Also, a fractional tone $f_{fref}/2$ appears when DWA is activated. Finally, in figure 4.23(c), compared to DWA a little in-band noise increment is shown in DWA_{inc} technique with a 7-dB suppression on the $f_{fref}/2$ tone. Table 4.2 summaries the measured performances.



(a)



(b)



(c)

Figure 4.23. Measurement results of output phase noise, with V_c manually set to 0.7 V. (a) No compensation applied (light) and, compensation applied without DEM technique (dark). (b) Compensation applied without DEM technique (light) and, Compensation applied with DWA technique (dark). (c) Compensation applied with DWA technique (light) and, Compensation applied with $\mathrm{DWA}_{\mathrm{inc}}$ technique (dark).

Technology	0.18-μm CMOS
Chip Size	0.92×1.15 mm^2
Supply	1.8 V
Oscillation frequency	1.77 GHz ~ 1.91 GHz
Frequency Step Size	4 Hz
Power Consumption	27.2 mW
Output Phase Noise	-82 dBc/Hz @ 10 kHz
(without compensation)	-84 dBc/Hz @ 100 kHz
	-103 dBc/Hz @ 1 MHz
	-122 dBc/Hz @ 10 MHz
Output Phase Noise	-82 dBc/Hz @ 10 kHz
(with compensation)	-84 dBc/Hz @ 100 kHz
	-103 dBc/Hz @ 1 MHz
	-132 dBc/Hz @ 10 MHz
Bandwidth	250 kHz
Lock Time	< 25 μsec
Reference Spur	-40 dBc

Table 4.2 Measured performance summary.

4.6 Conclusion

In this work, a multiphase quantization noise suppression technique for fractional-*N* frequency synthesizers is proposed and demonstrated in 0.18-μm CMOS technology. The experimental results show the out-of-band phase noise contributed by the modulator is reduced by 10 dB, where the out-of-band phase is dominated by the quantization noise. The phase noise cancellation technique relaxes the fundamental tradeoff between phase noise and bandwidth in conventional fractional-*N* frequency synthesizers and does not

require tight component matching. The measurement results show -82 dBc/Hz in-band phase noise within the loop bandwidth of 200 kHz, and -103 dBc/Hz and -132 dBc/Hz out-of-band phase noise at 1 MHz and 10 MHz offset from a 2.14 GHz center frequency. The lock time is less than 25 μs.

Chapter 5

Conclusions

5.1 Conclusions

A dual-delay path ring oscillator is implemented. The oscillation frequency increment due to additional-delay paths in ring oscillators is derived. The two oscillation mode in differential four-stage dual-delay path ring oscillators is analyzed and demonstrated. The main difference of the two oscillation modes is the output waveform characteristic. Instead of typical differential outputs, the outputs of a delay cell become in-phased. Furthermore, the oscillation frequencies in the two oscillation modes are shown to be different. This dual-delay path ring oscillator is implemented by a 0.18-μm CMOS technology with an active area of 58×41 μm^2.

A multiphase quantization noise suppression technique for fractional-*N* frequency synthesizers is proposed. A re-quantized Σ-Δ Modulator is implemented to overcome the

nonidea effect of delay units gain error. Dynamic element matching techniques are also employed for element mismatch linearization. The phase noise cancellation technique relaxes the fundamental tradeoff between phase noise and bandwidth in conventional fractional-*N* frequency synthesizers and does not require tight component matching. This frequency synthesizer is implemented by a 0.18-μm CMOS technology with an area of 0.92 × 1.15 mm^2.

Bibliography

[1] A. B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*, Ch. 11, New York, Wiley Interscience, 1984.

[2] B. De Muer and M. Steyaert, "A CMOS Monolithic ΣΔ-Controlled Fractional-*N* Frequency Synthesizer DCS-1800," *IEEE J. Solid-State Circuits*, vol. 37, pp. 835-844, July 2002.

[3] W. Rhee, B. Song, and A. Ali, "A 1.1 GHz CMOS Fractional-*N* Frequency Synthesizer with A 3-b Third-Order ΣΔ Modulator," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1453-1460, Oct. 2000.

[4] M. Kozak and ˙I. Kale, "Rigorous Analysis of Delta–Sigma Modulators for Fractional-*N* PLL Frequency Synthesis," *IEEE Trans. Circuits Syst. I*, vol. 51, pp. 1148-1162, June 2004.

[5] M. Perrott, "Fast and Accurate Behavioral Simulation of Fractional-*N* *F*requency Synthesizers and Other PLL/DLL Circuits," in *Proc. IEEE 39th Annu. Design Automation Conf.*, 2002, pp. 498–503.

[6] M. H. Perrott, M. D. Trott, and C. G. Sodini, "A Modeling Approach for Σ-Δ

Fractional-*N* Frequency Synthesizers Allowing Straightforward Noise Analysis," *IEEE J. Solid-State Circuits*, vol. 37, pp. 839-849, Aug. 2002.

[7] E. Temporiti, G. Albasini, I. Bietti, R. Castello, and M. Colombo, "A 700-kHz Bandwidth ΣΔ Fractional Synthesizer With Spurs Compensation and Linearization Techniques for WCDMA Applications," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1446-1454, Sep. 2004.

[8] S. Pamarti, L. Jansson, and I. Galton, "A Wideband 2.4-GHz Delta-Sigma Fractional-*N* PLL With 1-Mb/s In-Loop Modulation," *IEEE J. Solid-State Circuits*, vol. 39, pp. 49-62, Jan. 2004.

[9] C.-H. Park, O. Kim, and B. Kim, "A 1.8 GHz Self-Calibrated Phase-Locked Loop with precise I/Q Matching," *IEEE J. Solid-State Circuits*, vol. 36, pp. 777-783, May 2001.

[10] T. Riley and J. Kostamovaara, "A Hybrid Fractional-*N* Frequency Synthesizer," *IEEE Trans. Circuits Syst. II*, vol. 50, pp. 176-180, Apr. 2003.

[11] C.-H. Heng, B.-B. Song, "A 1.8-GHz CMOS Fractional-*N* Frequency Synthesizer with Randomized Multiphase VCO," *IEEE J. Solid-State Circuits*, vol. 38, pp. 848-854, June 2003.

[12] S. E. Meninger and M. H. Perrott, "A Fractional-*N* Frequency Synthesizer Architecture Utilizing a Mismatch Compensated PFD/DAC Structure for Reduced Quantization-Induced Phase Noise," *IEEE Trans. Circuits Syst. II*, vol. 50, pp.

839-849, Nov. 2003.

[13] Y.-C. Yang, S.-A. Yu, Y.-H. Liu, T. Wang, and S.-S. Lu, “A Quantization Noise Suppression Technique for ΔΣ Fractional-*N* Frequency Synthesizers,” *IEEE J. Solid-State Circuits*, vol. 41, pp.2500-2511, Nov. 2006.

[14] W. Rhee and A. Ali, “An On-Chip Phase Compensation Technique in Fractional-*N* Frequency Synthesis,” in *Proc. IEEE ISCAS*, vol. 3, July 1999, pp. 363-366.

[15] L. Sun, T. Kwasniewski, and K. Iniewski, “A Quadrature Output Voltage Controlled Ring Oscillator Based on Three-Stage Subfeedback Loops,” in *Proc. IEEE ISCAS*, vol. 2, 1999, pp. 176-179.

[16] Y. Sugimoto and T. Ueno, “The Design of a 1V, 1GHz CMOS VCO Circuit with In-Phase and Quadrature-Phase Outputs,” in *Proc. IEEE ISCAS*, vol. 1, June 1997, pp. 269–272.

[17] D. Y. Jeong, S. H. Chai, W. C. Song, and G. H. Cho, “CMOS Current-Controlled Oscillators Using Multiple-Feedback Loop Architectures,” in *IEEE Intl. Solid-State Circuits Conf. on Dig. Tech. Papers*, Feb. 1997, pp. 386–387.

[18] C. H. Park and B. Kim, “A Low-Noise, 900-MHz VCO in 0.6-*um* CMOS,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 586–591, May 1999.

[19] S. J. Lee, B. Kim, and K. Lee, “A Novel High-Speed Ring Oscillator for Multi-phase Clock Generation Using Negative Skewed-Delay Scheme,” *IEEE J. Solid-State*

Circuits, vol. 32, pp. 289–291, Feb. 1997.

[20] Yalcin Alper Eken, and John P. Uyemura, “A 5.9-GHz Voltage-Controlled Ring Oscillator in 0.18-um CMOS,” *IEEE J. Solid-State Circuits*, vol. 39, no. 1, January 2004.

[21] J. T. Hwang, S. H. Woo, J. Y. Ryu, K. Lee, and G. H. Cho, "New High Performance and Wide Range Tunable Two-Stage 3GHz CMOS RF Hetero-Linked Oscillators," in *European Solid-State Circuits Conf. (ESSCIRC)*, pp. 354- 357, September 1999.

[22] A. Goel and H. Hashemi, “Frequency Switching in Dual-Resonance Oscillators,” *IEEE J. Solid-State Circuits*, vol. 42, no. 3, March 2007.

[23] T. A. Riley, M. Copeland, and T. Kwasniewski, “Delta-Sigma Modulation in Fractional-*N* Frequency Synthesis,” *IEEE J. Solid-State Circuits*, vol. 28, pp. 553-559, May 1993.

[24] R. K. Henderson and O. J. A. P. Nys, “An Analysis of Dynamic Element Matching Techniques in Sigma-Delta Modulation,” in *Proc. IEEE ISCAS*, vol. 1, May 1996, pp. 231-234.

[25] R. K. Henderson and O. J. A. P. Nys, “Dynamic Element Matching Techniques with Arbitrary Noise Shaping Function,” in *Proc. IEEE ISCAS*, vol. 1, May 1996, pp. 293-296.

[26] M. Kozak and I. Kale, “A Pipelined Noise Shaping Coder for Fractional-*N* Frequency

Synthesis," *IEEE Trans. Instrum. Meas.*, vol. 50, pp. 1153-1161, Oct. 2001.

[27] I. Galton, "Spectral Shaping of Circuit Errors in Digital-to-Analog Converters," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 808-817, Oct. 1997.

[28] B. Razavi, *Design of Analog CMOS Integrated Circuirs*, McGraw-Hill, 2001.

[29] B. Razavi, *RF Microelectronics*, Prentice Hall, 2003.

[30] B. Razavi, *Design of Integrated Circuits for Optical Communications*, 1st Ed., McGraw-Hill, 2003.

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