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高頻CMOS鎖相迴路之設計與實現

Design and Implementation of High-frequency CMOS Phase-locked Loops

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本論文係黎信志君（r95943026）在國立臺灣大學電子工程所研究所完成之碩士學位論文，於民國 97 年 7 月 30 日承下列考試委員審查通過及口試及格，特此證明

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系主任、所長

Design and Implementation of High-frequency CMOS Phase-locked Loops

By

Sin-Jhih Li

THESIS

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誌謝

又到了鳳凰花開的時節。經過了兩年的努力，終於完成了這本碩士論文。即將，就要揮別了台大殿堂，進入到人生的下一個階段。

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摘要

本篇論文主題主要在介紹高頻鎖相迴路的設計與實作。論文中討論了數個方法以改善在高頻鎖相迴路中時脈擾動的情形。論文共分為六個章節，首先第一章對此篇論文作概略性的介紹，第二章則回顧鎖相迴路的背景知識。

第三章提出了一個使用多重相位控制的鎖相迴路架構。藉由此架構可有效抑制壓控震盪器控制電壓上來自參考時脈的週期性擾動，進而減少時脈鎖定時的擾動現象。此迴路架構使用了 0.18-μm 標準互補式金氧半導體製程加以實現，同時量測結果也會於本章呈現。

第四章將實現一個雙迴路的鎖相迴路架構。此架構可等效上減少迴路濾波器所需要的電容面積，故有助於單晶積體電路的整合。由於來自晶片外的元件雜訊減少了，時脈鎖定時的雜訊擾動現象也能因此有所改善。此鎖相迴路設計使用了 0.18-μm 標準互補式金氧半導體製程實作並且加以量測。

第五章將討論一個 30-GHz 的鎖相迴路設計。此設計採用了改良式的 Colpitts 壓控震盪器以減少壓控震盪本身所產生雜訊並使用了 regenerative 除頻器來增加如此高速下時脈信號的除頻範圍。此章將詳述此 30-GHz 鎖相迴路之設計流程與模擬結果。

Abstract

This thesis illustrates the implementation of the high frequency phase-locked loops (PLLs). In order to reduce the output jitter, several strategies are presented, which are suitable for high speed PLL design. The thesis is organized as six chapters. The first chapter is the introduction. In chapter 2, the background knowledge for the PLL design is overviewed.

In chapter 3, a PLL with multi-phase control architecture is proposed. Since the proposed architecture effectively suppresses the ripple of the controlled voltage, the jitter resulted from the reference feedthrough is decreased. The circuit is implemented with 0.18-μm CMOS technologies and the measured resulted is also included in this chapter.

In chapter 4, a PLL with a compact loop filter is presented. The presented architecture is well suited for the implementation of fully integrated PLLs since the required capacitance in the loop filter can be substantially reduced. The jitter performance will be improved because of the absence of offchip components. The circuit is also realized with 0.18-μm CMOS process and the measured resulted is also included in this chapter.

In chapter 5, a PLL operated at 30-GHz is designed and simulated. The modified Colpitts VCO is adopted for the reduction of the VCO noise. A regenerative frequency divider is also employed to widen the dividable range at such high frequency. The design process and the simulation results will be illustrated in this chapter.

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Chapter1

Introduction

1.1 Motivation

The concept of phase locking was invented in 1932 by the British researchers. The phase-locked loop (PLL) serves the task of a signal generator that has a connected relation to the frequency and phase of a reference signal. The phase-locked loop is basically a negative feedback system. By applying the frequency and phase comparison with the reference signal, the phase-locked loop responds to both the frequency and phase of the inputs and automatically adjusts the voltage-controlled oscillator in order to achieve coherence.

PLLs have been widely used in telecommunications, computers, radio, and other electronic applications. For examples, with generation of a purified clock signal, the PLL recovers the signal from a noisy communication channels by retiming or distribute clock timing pulses. Besides, based on the concept of the PLL, frequency synthesizers are developed and play critical building components in the wireless transceivers. In the wire communications, such as SONET, Fiber Channel, and Gigabit Ethernet, clock and data recovery circuits also usually involves the PLL concept.

The advances in silicon integrated circuits technology have enabled chip realization using CMOS technology. In order to arrive at highly integration and low cost, the use of silicon technologies attracts great attention in recent years. However, PLLs implemented with CMOS technology suffer not only from the phase noise of the voltage-controlled oscillator (VCO) but also the severe substrate noise which can not be reduced even with huge power consumption. Especially, any noise generated from other circuits would couple through the conductive substrate to the VCO and degrades the phase noise, hence leading to poor jitter performance. Although large separation from noise source and guard rings help to reduce substrate coupling, the effectiveness is restricted because of the consideration of the compact layout area in practice. Furthermore, with the continuous growth of the operating speed and the trend of the low supply voltage, the necessary wider tuning range leads to inevitable higher VCO gain, which also poses challenges in the circuit design.

1.2 Thesis Overview

In this thesis, the analysis, design and experimental verification of high frequency and low jitter PLLs are presented. The circuits are fabricated in 0.18-μm CMOS technology and the experimental results are illustrated as well. The thesis is organized as follows.

In Chapter 2, the background of the phase-locked loop is given. First of all, an overview of the PLL will be given. Second, the building blocks of a PLL would be introduced and illustrated, including the phase and frequency detector and the voltage-controlled oscillator, the loop filter and the frequency divider. The jitter generation mechanism will also be analyzed in the end.

In Chapter 3, a PLL architecture utilizing the multiphase controls is proposed to

improve the jitter and phase noise performance. The principle and the circuit design flow are illustrated. Using standard 0.18-μm CMOS process, a 10-GHz PLL is implemented for demonstration with 1.8-V supply voltage. The measurement results are described in the end.

In Chapter 4, a PLL with dual path controls is presented. With this dual-path control architecture, a compact loop filter can be achieved. Therefore, the filter noise resulted from off-chip components can be effectively eliminated, leading to a reduced timing jitter. Implemented with standard 0.18-μm CMOS technology, a 10-GHz PLL is realized. The measurement results are also given finally.

In Chapter 5, a high-frequency 30-GHz PLL is designed and analyzed for the standard 0.18-μm CMOS technology. In this design, the modified Colpitts VCO is adopted to decrease the VCO noise contribution. The inductive peaking regenerative frequency divider is used at the first stage to operate at high frequency while maintaining the wide dividable range. The simulation results are also presented in this chapter.

Based on all the discussions in previous chapters, a conclusion is given in Chapter 6.

Chapter 2

Background

In this chapter, fundamental theories are introduced for the phase-locked loop (PLL). The essential building block and their operations will be illustrated. Besides, the loop transfer function and jitter generation mechanisms are also included.

2.1 Basic Concepts of the PLL

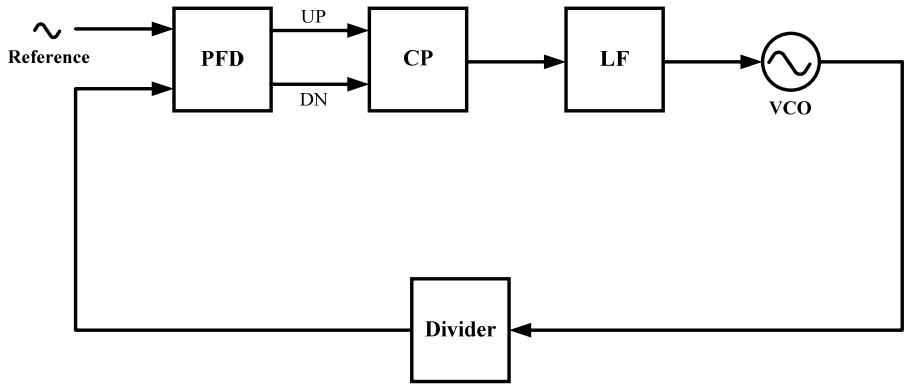


Fig. 2.1 The general PLL architecture.

A phase-locked loop (PLL) is a negative feedback loop which enables the local oscillator maintaining fixed frequency and phase in comparison with the input reference clock signal. A general PLL architecture is shown in Fig. 2.1, which consists of a phase

and frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a frequency divider. The PFD produces UP and Down pulses according to the phase and frequency difference between the reference signal and the divided VCO signal. The charge pump then transfers the pulses into current flowing into the loop filter. The loop filter produces a control voltage to adjust the frequency of the VCO and thereby achieves phase and frequency locking.

2.2 Building Blocks of the PLL

In this section, basic building blocks of a PLL are described. The operation principles and the functions are also included in this section. In the end, the jitter definition and analysis will be given.

2.2.1 The Phase and Frequency Detector (PFD) and the Charge Pump (CP)

A phase detector (PD) is a form of phase comparators which detects the phase difference between two different input signals and produces an output proportional to the phase difference. The PD converts the phase error presented to it into a voltage domain, which in turn is converted by a charge pump into correction error currents. Typically, the two inputs correspond to the two different signals, one from a voltage-controlled oscillator (VCO) and another from some external reference source. The mathematic relationship can be expressed as:

$$V_{out} = K_{PD} \cdot \Delta\phi \tag{2.1}$$

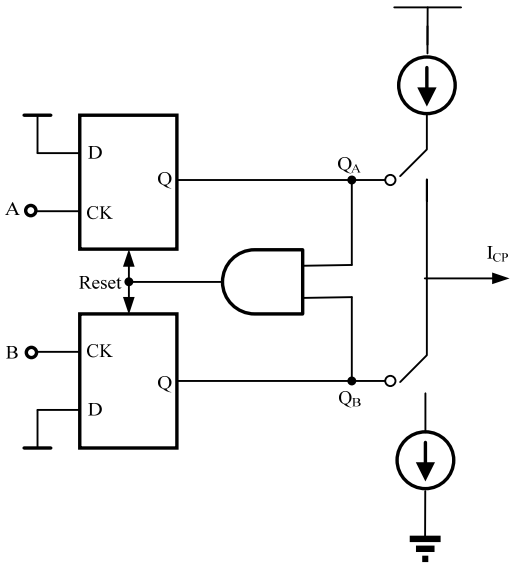


Fig. 2.2 The schematic of the phase and frequency detector.

Where V_{out} means the output voltage, and $\Delta\phi$ is the phase difference between the two input signals. In practice, a phase frequency detector (PFD) is usually adopted in the PLL implementation [1], [2]. The PFD is typically accompanied with a charge pump to transfer the phase domain signal into the current domain signal. The PFD not only compares the phase difference but also the frequency difference, thus increases the PLL locking range. The typical PFD, which consists of two D-type flip flops (DFFs) and an AND gate, accompanied with the charge pump is depicted in Fig. 2.2. The PFD is implemented with an edge-triggered sequential machine, which is only sensitive to rising/falling edges. Its timing diagram is demonstrated in Fig. 2.3(a) and (b). When the input signal A is leading the input signal B, the output signal Q_A continues to generate pulses whose width is proportional to the phase difference between the input signals A and B. If the input signal B is lagging the input signal B, then the output signal Q_B continues to generate pulses whose width proportional to the phase difference between the input signals A and B. The Q_A and Q_B signals are utilized as the indications as “Up” and “Down” signals. The PFD has infinite locking range of the phase and frequency as shown in Fig. 2.3(c) and is widely used in nowadays PLL implementations.

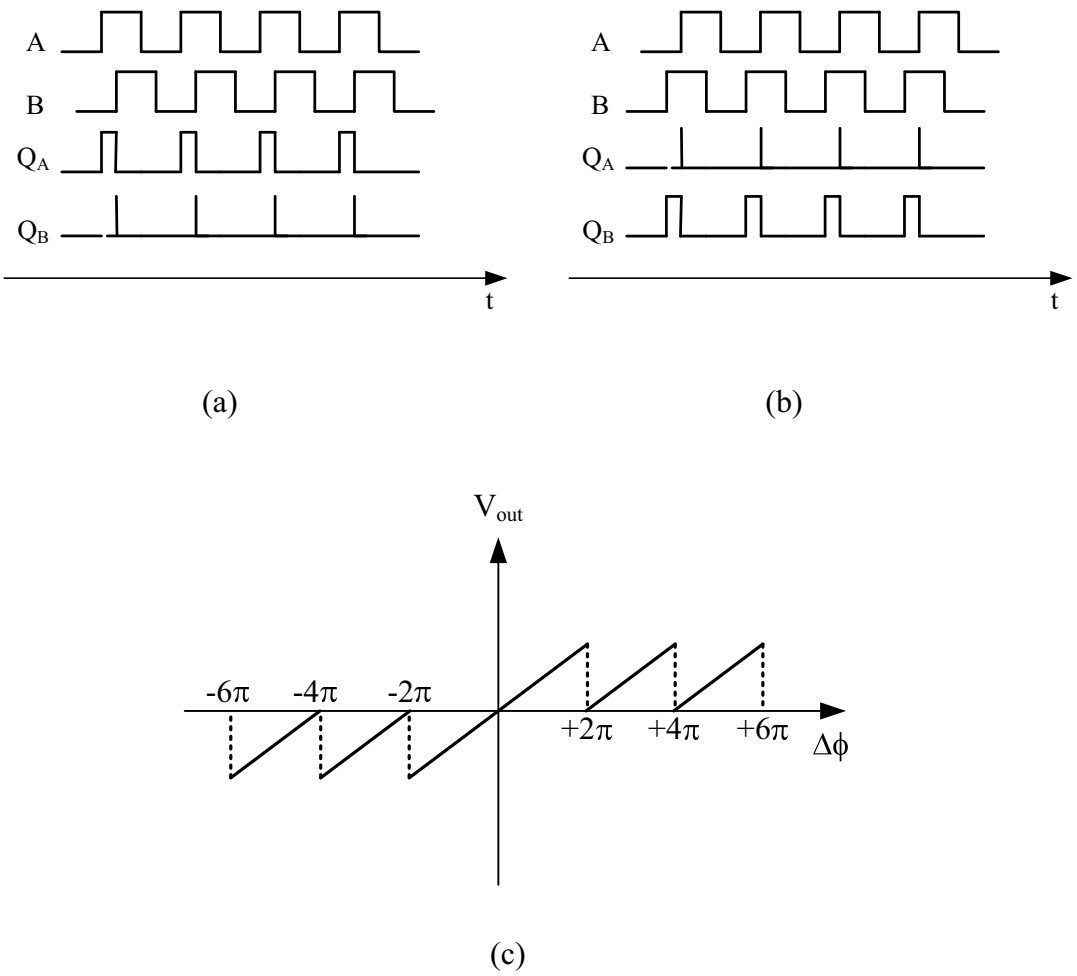


Fig. 2.3 (a) Q_A leads Q_B. (b) Q_A lags Q_B. (c) The acquisition range of the PFD.

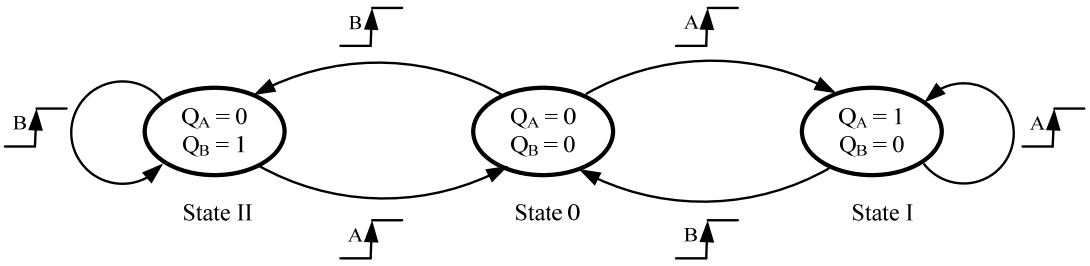


Fig. 2.4 The state diagram of the PFD.

The operations of the PFD can be expressed as a state diagram shown in Fig. 2.4. There are three states in this state diagram: state 0: $Q_A = Q_B = 0$; state I: $Q_A = 1$ and $Q_B = 0$; state II: $Q_A = 0$ and $Q_B = 1$. State I suggests that Q_A leads Q_B and State II suggests that

Q_A lags Q_B. Combined with charge pump, the transferring relation can be expressed as:

$$I_{pump} = I \cdot \frac{\Delta\phi}{2\pi} \tag{2.2}$$

2.2.2 Voltage-Controlled Oscillator (VCO)

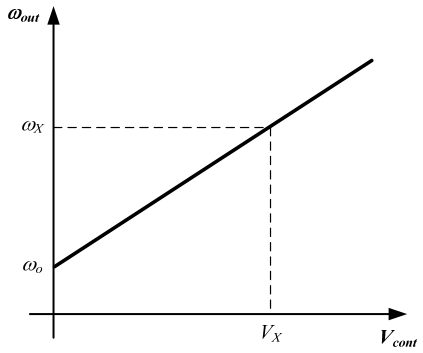


Fig.2.5 The VCO transferring curve.

VCO is a clock source whose output frequency is adjusted according to the controlled voltage. An ideal VCO is a circuit whose output oscillation frequency is a linear function of its control voltage:

$$\omega_{out} = \omega_o + K_{vco} V_{cont}. \tag{2.3}$$

Where the ω_o is the free-running oscillation frequency and the K_{vco} represents the gain of the VCO. The transfer characteristic of the VCO is depicted in Fig. 2.5. The excess output phase of VCO can be expressed as:

$$\phi_{out} = K_{vco} \int V_{cont} dt \tag{2.4}$$

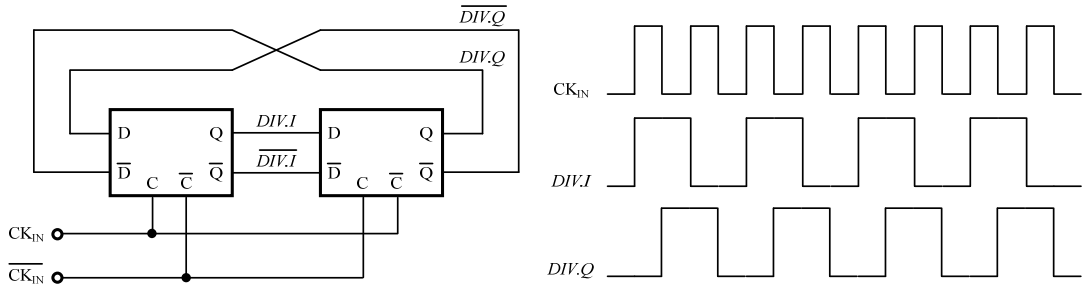
Thus, the Laplace-domain phase relationship is:

$$\phi_{out}(s) = K_{vco} \frac{V_{cont}(s)}{s} \tag{2.5}$$

As the supply voltage shrinks down and the VCO frequency increases, the inevitable large gain of the VCO degrades the VCO phase noise and jitter performance.

Therefore, the design the VCO in the high frequency applications is still a critical issue today.

2.2.3 Frequency Divider (FD)



(a) (b)

Fig. 2.6 (a) The flipflop-based divide-by-2 circuit (b) The waveforms of the divider

Frequency divider (FD) is utilized in the feedback path of the PLL to provide a multiplied frequency relationship between the reference clock and the output VCO signal. The divide-by-2 circuit is typically incorporated after the VCO. The schematic of the D-flipflop-based divide-by-2 circuit and its waveform are depicted in Fig. 2.6. The divide-by-2 circuit involves a single master-slave flipflop in a negative feedback loop and generates the 0° and 90° divided signals inherently.

2.3 The Linear Model for the PLL

A linear phase-domain model of a PLL is illustrated in Fig. 2.7. The open-loop gain can be expressed as:

$$G(j\omega) = \frac{I_p K_{vco} F(j\omega)}{j2\pi\omega} \tag{2.6}$$

A simple second-order PLL loop with the loop filter consisting of a resistor in series of a

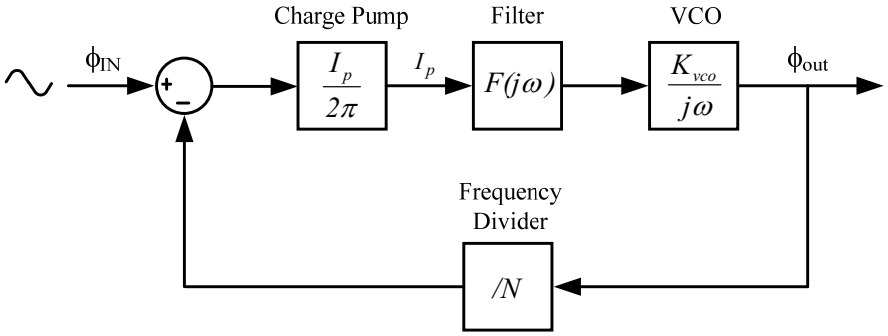


Fig. 2.7 The linear model of the PLL.

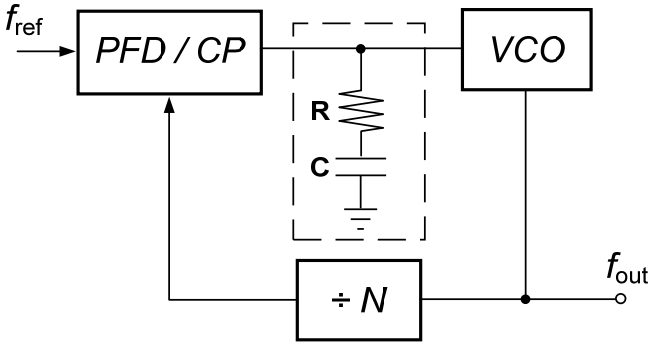


Fig 2.8 The second-order PLL.

capacitor is shown in Fig. 2.8. The current from the charge pump causes the controlled voltage to adjust the oscillation frequency of the VCO. The transfer function of the loop filter can be expressed as:

$$F(s) = R + \frac{1}{sC} \tag{2.7}$$

The loop filter contributes a pole and a zero at the origin and the frequency of 1/RC respectively. The total open loop transfer function can be shown as:

$$G(s) = \frac{I_p}{2\pi} F(s) \frac{K_{vco}}{s} \frac{1}{N} = \frac{I_p K_{vco}(1 + sRC)}{NCs^2} \tag{2.8}$$

Thus the entire PLL loop has two poles at the origin and a zero at *1/RC*. The loop is

unconditionally stable. However, the I-R voltage drop resulted from the resistor R will disturb the controlled voltage and degrade the output clock performance severely, as shown in Fig. 2.9.

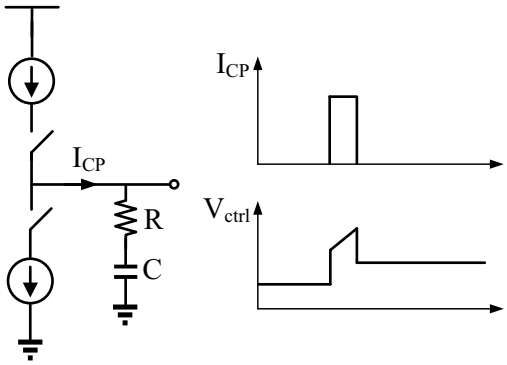


Fig. 2.9 The I-R drop in the second-order PLL.

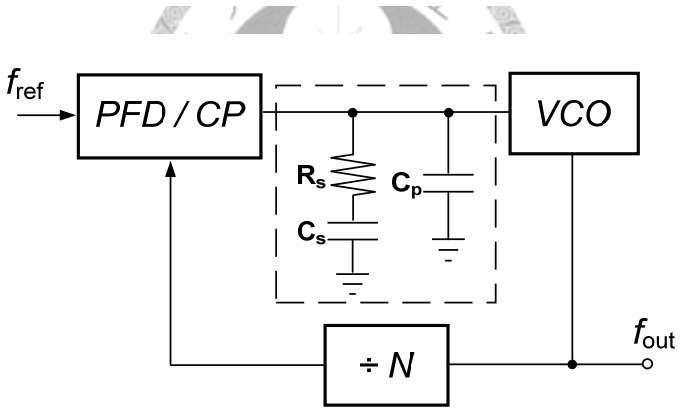


Fig. 2.10 The third-order PLL.

In order to solve this problem, a second capacitor is usually added in parallel to suppress the initial step, as shown in the Fig. 2.10. Therefore, the loop filter now is of second order, leading to a third-order PLL and yielding to the stability issue [3]. The loop filter transfer function can be shown as:

$$\frac{V}{I}(j\omega) = F(j\omega) = \frac{1}{C_1 + C_2} \frac{s\tau_2 + 1}{s(s\tau_1 + 1)} \tag{2.9}$$

where $$\tau_1 = R_s \frac{C_s C_p}{C_s + C_p} \quad and \quad \tau_2 = R_s C_s \tag{2.10}$$

and the open-loop transfer function is then expressed as:

$$G(j\omega) = \frac{-I_p K_{vco}(1 + j\omega\tau_2)}{2\pi\omega^2 C_p N(1 + j\omega\tau_1)} \frac{\tau_1}{\tau_2} \tag{2.11}$$

The maximum phase margin can be derived as:

$$\phi_p = tan^{-1}(\omega_c \tau_2) - tan^{-1}(\omega_c \tau_1) \tag{2.12}$$

$$\omega_c = \frac{1}{\sqrt{\tau_1 \tau_2}} \tag{2.13}$$

ω_c is the cutoff frequency or the unity-gain frequency. A parameter γ can be defined to indicate the maximum phase margin:

$$\gamma \equiv \frac{\omega_c}{\omega_z} = \frac{\omega_p}{\omega_c} \tag{2.14}$$

Table 2.1 shows different γ value and the corresponding maximum phase margin.

Table 2.1 The maximum phase margin vs. γ

γ	Max. phase margin
1	0°
2	36.9°
3	53.1°
4	61.9°
5	67.4°
6	71°

However, the closed-loop transient and frequency response will be relative

unchanged with C_p much smaller than C_s.

Moreover, a third pole can even be added to further filter and smooth the controlled voltage [4], [6], as shown in Fig.2.11. In such case, thee loop phase margin is somehow

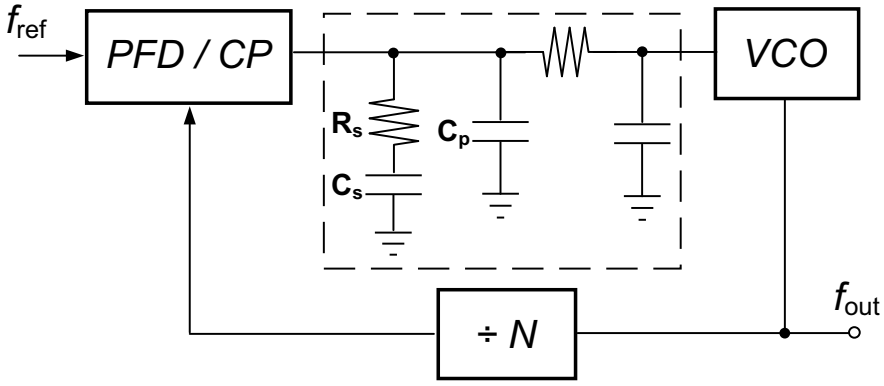


Fig. 2.11 The forth-order PLL.

sacrificed and the stability issue has to be treated carefully.

2.4 Jitter

The time-domain behavior of phase noise represents the extent to which the zero crossings of a signal are disturbed and thus a critical issue in the high-speed applications. The deviation of the zero crossings from their ideal position in time domain is called jitter.

In order to quantify jitter, the deviation of each positive/negative transition point of CK_{out} from its corresponding point of the ideal signal CK_{ref} is shown in Fig. 2.12. A very large number of jitter should be measured since its random characteristics. The root mean square value of absolute jitter can be expressed as [1]:

$$\Delta T_{abs,rms} = \lim_{N\to\infty} \frac{1}{N}\sqrt{\Delta T_1^2 + \Delta T_2^2 + \Delta T_3^3 + \cdots + \Delta T_N^2} \tag{2.15}$$

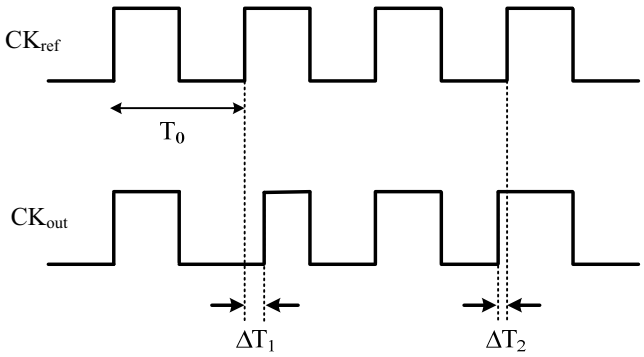


Fig. 2.12 The timing diagram of absolute jitter.

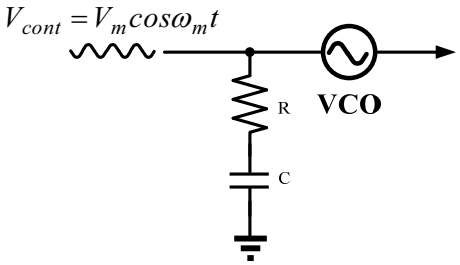


Fig 2.13 Ripple due to reference feedthrough.

The reference feedthrough is one of the major jitter sources in the PLL. The reference feedthrough is always resulted from the charge pump current mismatch and UP and DOWN pulse skew. The ripple on the controlled line directly modulates the oscillation frequency, thus leading to undesirable jitter.

For the simplicity of jitter quantification [5], [6], suppose a periodic ripple $V_m cos\omega_m t$ on the controlled line, as shown in Fig. 2.13, the excessive phase is given by:

$$\Delta\phi(t) = \int_0^t K_{vco} V_m cos\omega_m \tau \, d\tau = \frac{K_{vco} V_m}{\omega_m} sin\omega_m t. \tag{2.16}$$

It should be noticed the absolute jitter is the deviation of the zero-crossing point of the output clock:

$$\Delta T(t) = \frac{\Delta\phi(t)}{N\omega_m} = \frac{K_{vco}V_m}{N\omega_m^2}\sin\omega_m t \tag{2.17}$$

where N denotes the divider ratio. For large divide ratio N, the rms jitter can be expressed as:

$$(\Delta T)_{rms}^2 = \frac{\omega_m}{2\pi}\int \frac{K_{vco}^2}{N^2\omega_m^4}\sin^2\omega_m t\, dt \tag{2.18}$$

It follows that

$$(\Delta T)_{rms} = \frac{K_{vco}V_m}{\sqrt{2}N\omega_m^2}. \tag{2.19}$$

Also the peak-to-peak jitter can be calculated as

$$(\Delta T)_{pp} = \frac{2K_{vco}V_m}{N\omega_m^2} \tag{2.20}$$

Equation (2.19) and (2.20) indicated that the jitter resulting from the reference feedthrough is proportional to the ripple amplitude V_m and inverse proportional to square of the ripple frequency.

Chapter 3

A Low-Jitter 10-GHz Phase-Locked Loop with the Multi-Phase Control

In this chapter, a novel phase-locked loop (PLL) architecture suitable for high-speed data link applications is presented. By employing multi-phase control in the distributed phase/frequency detectors (PFD) and charge pumps, the ripple on the controlled signal of the voltage-controlled oscillator (VCO) is effectively suppressed, leading to significant suppression in the peak-to-peak jitter at the PLL output. In addition, as the phase and frequency detection are decomposed in the circuit implementation, the in-band phase noise and jitter associated with the frequency dividers can be further reduced, leading to enhanced output characteristics especially for high-frequency PLL designs. Using a 0.18-μm CMOS process, the proposed circuit is realized for demonstration.

3.1 Introduction

Owing to the strong demands in data communications and multi-media applications, broadband services based on fiber-optical networks have been deployed at an unprecedented rate all over the world. Provided the unparalleled advantages in terms

of fabrication cost, power dissipation and ease of system integration, the CMOS technology provided by the foundries is considered the most promising candidate for the circuit implementation. Therefore, tremendous efforts have been made to realize fully integrated CMOS transceivers operating at a data rate of 10-Gb/s or even 40-Gb/s [6]-[11].

As an essential building block for the transmitting and the receiving ends, a phase-locked loop (PLL) is widely utilized in a high-speed data link to provide the required timing clock. With recent advances in the semiconductor process technology, deep-submicron CMOS transistors with extremely high cut-off frequencies are commercially available. CMOS PLLs operated for an output frequency from tens of gigahertz up to 50 GHz have been successfully demonstrated [6]-[11], [13], [14]. However, limited by the noise characteristics, driving capability and substrate losses, most of the high-frequency PLL designs suffer from severe problems with the output jitter. To overcome the limitations imposed on the circuit performance, a novel PLL architecture with distributed phase/frequency detector (PFD) and charge pump (CP) is presented in this work. By employing a multi-phase control scheme in the loop, significant reduction in the output jitter can be achieved. Based on the proposed circuit techniques, a 10-GHz PLL is implemented in a 0.18-μm CMOS process for demonstration.

The remainder of this chapter is organized as follows. Section 3.2 describes the proposed architecture and operating principles of the PLL. Circuit design and experimental results of the 10-GHz PLL are presented in Section 3.3 and 3.4, respectively, followed by concluding remarks in Section 3.5.

3.2 The Proposed PLL Architecture

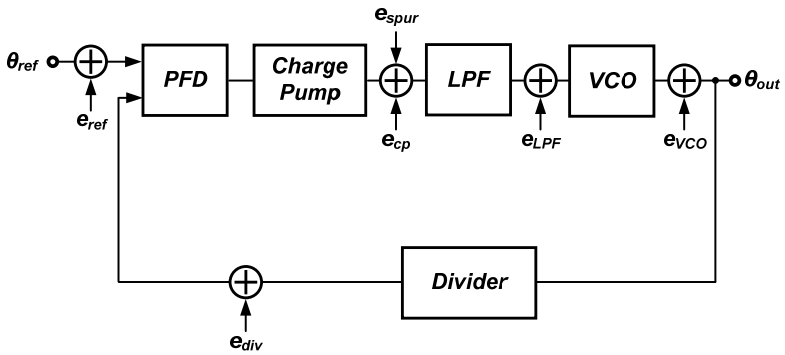


Fig. 3.1 The conventional third-order PLL architecture.

TABLE 3.1

Various Noise Sources in the Simple Noise Model of the PLL

Symbol	Meaning	The Cause
e_{ref}	reference jitter	noise-induced variations in the transition time of the reference output waveform
e_{cp}	charge pump noise	devices in the charge pump
e_{LPF}	filter noise	resistors in the loop filter
e_{VCO}	VCO noise	devices in the VCO
e_{div}	divider jitter	noise-induced variations in the transition time of the divider output waveform
e_{spur}	reference feedthrough	mismatch from the PFD and charge pump

In order to have better understanding on the origin of the output jitter, a simplified circuit model based on a conventional third-order PLL architecture is illustrated in Fig. 3.1 while the description of the individual noise sources are summarized in Table 3.1.

Among the noise sources involved in the loop, the reference feedthrough e_{spur} is typically considered one of the most dominant factors in the circuit implementations.

3.2.1 Distributed PFD and CP with Multi-Phase Control

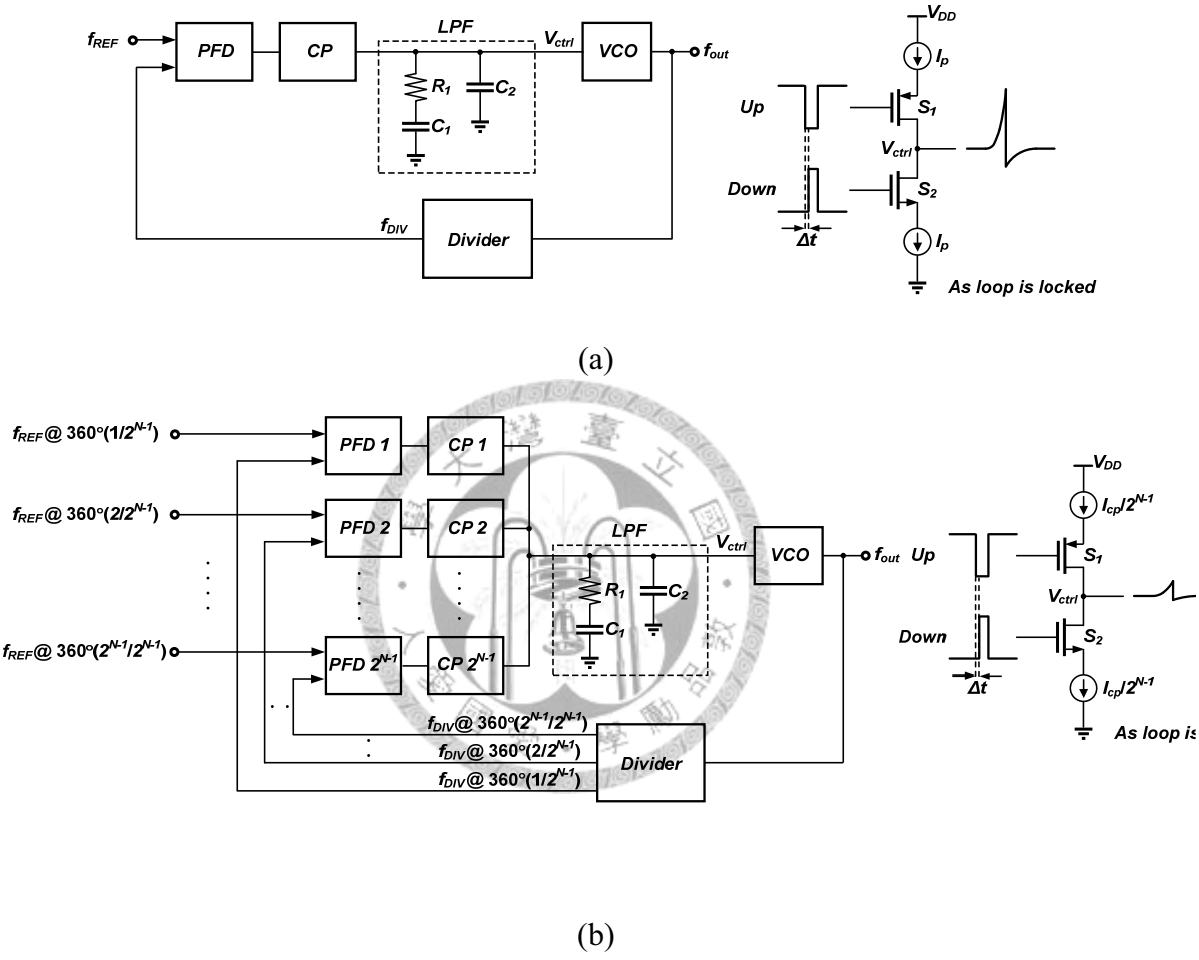


Fig. 3.2 (a) The conventional and (b) the proposed architectures of the third-order PLL.

For a conventional PLL circuit with phase locked to the input reference, the up and

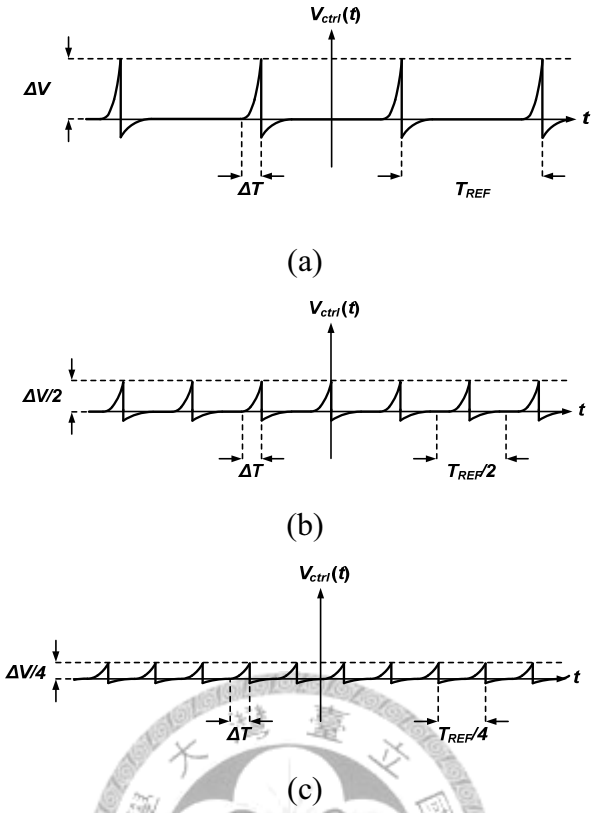


Fig. 3.3 The waveforms on the controlled line for (a) $2^{N-1} = 1$, (b) $2^{N-1} = 2$ and (c) $2^{N-1} = 4$.

down pulses are still generated by the PFD for every phase comparison instant. Ideally, the up and down pulses should be properly aligned and have identical waveforms in the opposite polarity, resulting in a stationary controlled voltage and stable output frequency for the VCO circuit. However, as the mismatch in the operation of the PFD and CP is taken into account, a more practical presentation of the PLL and the associated controlled voltage are illustrated in Fig. 3.2(a). It is noted that, as the pulse skew and mismatch in charging and discharging current exist, voltage fluctuation in the VCO controlled line is thus introduced. As a result, timing jitter appears at the PLL output, which may lead to an elevated bit error rate (BER) in a high-speed data link.

In order to achieve enhanced performance in the timing jitter, a novel architecture with distributed PFD and CP is proposed. The block diagram is illustrated in Fig. 3.2(b)

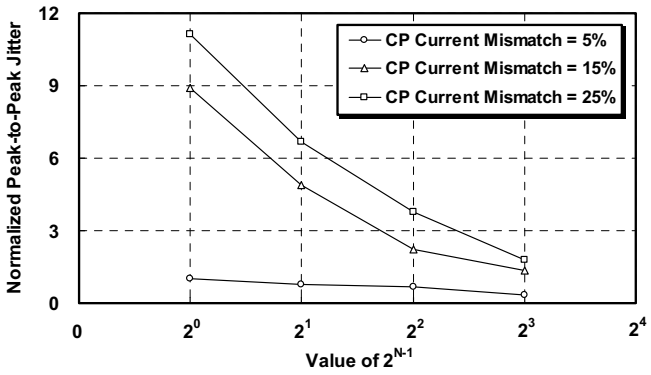


Fig. 3.4 The simulated normalized peak-to-peak jitter of the topology in Fig. 2(b) with the sweep of 2^{N-1}.

where 2^{N-1} identical PFD and CP cells are placed in parallel to perform the phase locking. As multiple phases are provided by the reference and the divided signals, phase detection is thus carried out by the PFD cells each generating its own up and down pulses with equally spaced time intervals. Assuming that the loop is locked, a conceptual illustration of the waveforms on the VCO controlled line is shown in Fig. 3.3 for various numbers of distributed cells. It is noted that, as more cells are incorporated in the PLL, the frequency of the charging/discharging operation increases while each CP current decreases. Consequently, the fluctuation on the controlled voltage is effectively suppressed.

To simplify the analysis on the timing jitter, the voltage fluctuations as shown in Fig. 3.3 are approximated by triangular waveforms. The peak-to-peak jitter for 2^{N-1} distributed PFD and CP cells has the relationship as follow:

$$(Jitter)_{pp} \propto \frac{\Delta V \Delta T}{2^N} \tag{3.1}$$

Reduced peak-to-peak jitter can be achieved by increasing the number of the distributed cells in the PLL architecture. However, the hardware overhead as well as the

circuit complexity also increases accordingly. Finally, instead of the reference feedthrough, other noise sources may become dominant factors in contributing to the output jitter. Based on behavior simulations for the third-order PLL, the peak-to-peak jitters versus the number of distributed cells are illustrated in Fig. 3.4 for various CP mismatch currents. As indicated in the simulation results, the proposed technique provides effective jitter suppression especially when significant mismatch is presented in the CP currents. In consideration of the performance enhancement and design complexity, an optimum cell number of 4 is employed in the proposed PLL design.

3.2.2 Decomposition of Frequency and Phase Detection

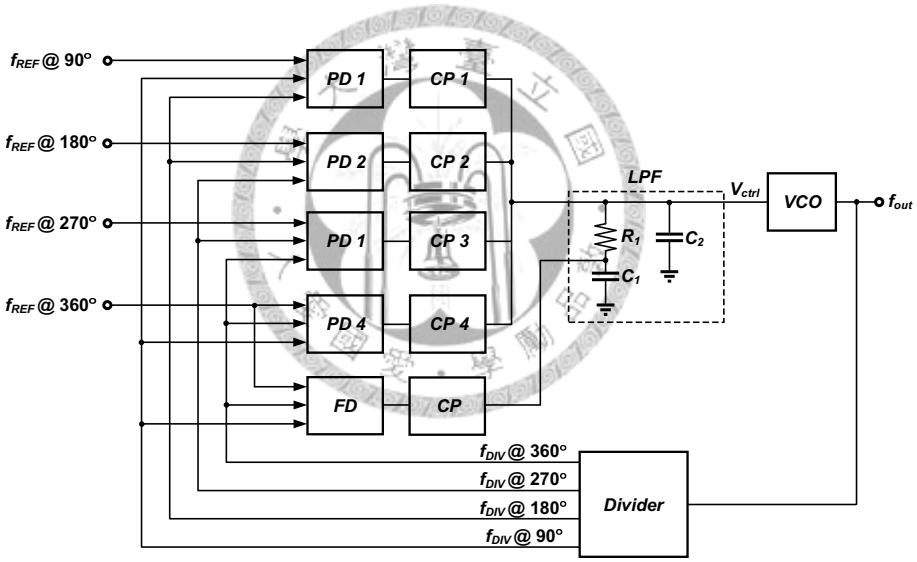
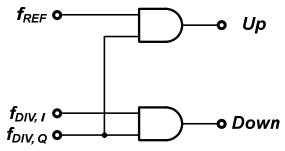


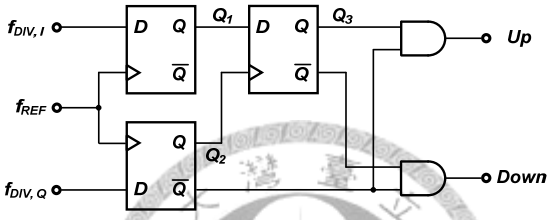
Fig. 3.5 The proposed architecture of the PLL while the phase and frequency detections are decomposed.

In conventional PLL designs, the tri-state DFF-based PFD is widely used to perform phase and frequency detection. Due to the inherently slow response of the internal feedback loop, the allowable input frequency of such PFD is severely limited [15]. As a low-frequency reference is adopted, frequency dividers with a high dividing

ratio are typically required to generate the divided signal for phase locking. The noise sources contributed by the increasing number of the divider stages tend to elevate the in-band phase noise and timing jitter at the PLL output [16] and the performance degradation manifests itself as the output frequency increases. To overcome such



(a)



(b)

Fig. 3.6 The architectures of (a) the PD and (b) the FD employed in this design.

limitations, a circuit technique was proposed to decompose the frequency and phase detection [6], [13] in the circuit implementation. By adopting the design concept, a modified block diagram for the PLL circuit is demonstrated in Fig. 3.5 where a frequency detection module is separated from the distributed phase detection cells. During the acquisition, the frequency detector (FD) is activated, driving the VCO towards the desirable frequency. Finally, the phase locking is achieved by the distributed phase detector (PD) and CP. Note that the FD automatically disables itself when the loop is locked. As a result, its influence on the timing jitter can be neglected.

Fig. 3.6 shows the circuit schematic of FD and PD employed in the PLL design. Since only simple logic operations are utilized, the limitations on the operating speed

are alleviated, allowing a high-frequency signal as the input reference. Consequently,

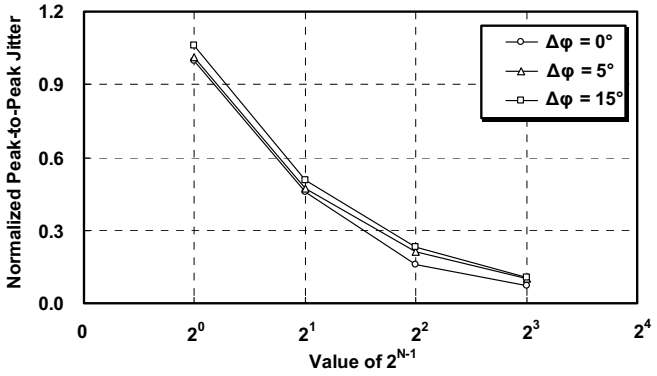


Fig. 3.7 The simulated normalized peak-to-peak jitter of the topology in Fig. 5 with the sweep of 2^{N-1}.

the increase in the phase noise and output jitter resulted from the additional divider stages can be generally prevented. Note that, in the PD/FD decomposition technique, the circuit operation requires quadrature phases for the divided signal. Therefore, it can be incorporated with the proposed distributed architecture without additional hardware overhead. To evaluate the output characteristics, behavior simulations were performed based on the PLL architecture as shown in Fig. 3.5. The simulated peak-to-peak jitters for various phase errors are illustrated in Fig. 3.7. It is indicated that effective jitter suppression can be achieved by the proposed techniques even at the presence of phase error for the quadrature signal generation.

3.3 Circuit Implementation

Using a 1P6M 0.18-μm CMOS process, a 10-GHz low-jitter PLL is implemented based on the proposed architecture. With a device layout optimized for the RF performance, the n-channel MOSFET in a deep n-well exhibits a cutoff frequency f_T up to 50 GHz. As for the on-chip passive components, a top AlCu metallization with a

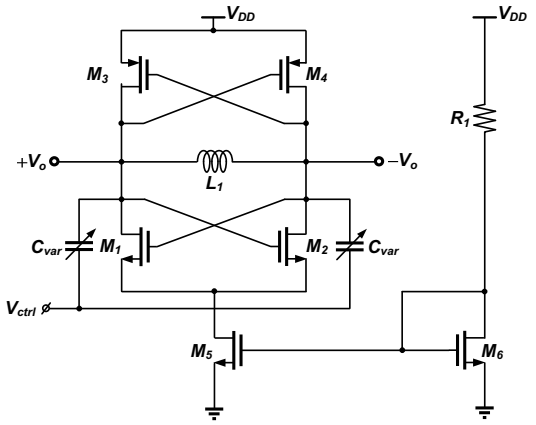


Fig. 3.8 The VCO employed in this work.

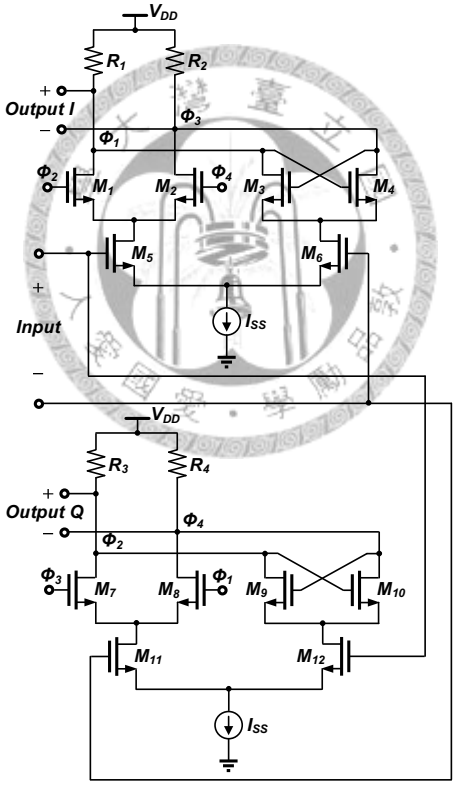
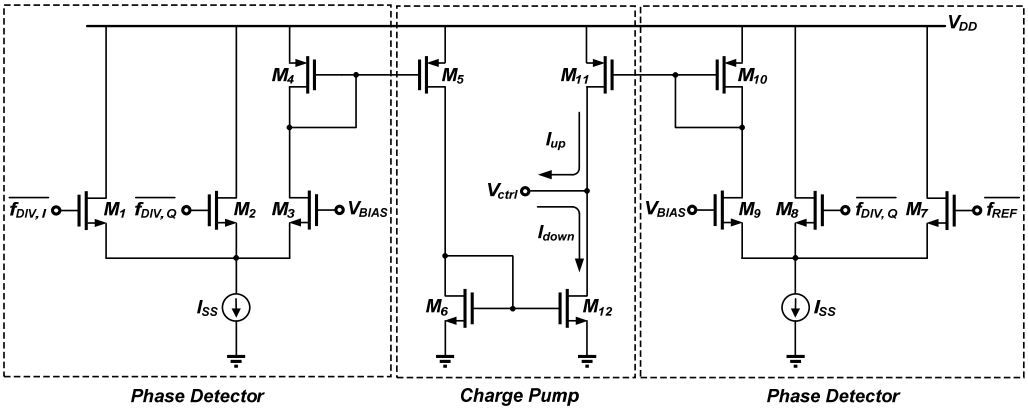
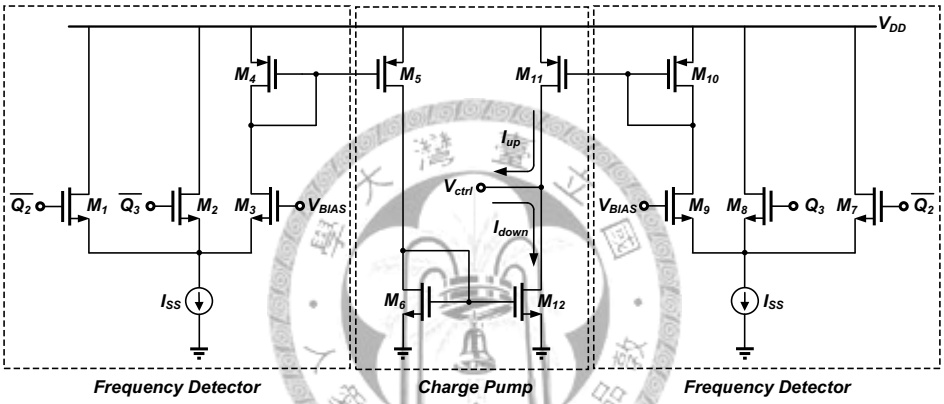


Fig. 3.9 The divide-by-two frequency divider using the current-mode logic.

thickness of 2 μm and a MIM structure with oxide intermetal dielectric are provided in this technology.



(a)



(b)

Fig. 3.10 The adopted (a) PD with the charge pump and (b) FD with the charge pump.

Fig. 3.8 shows the circuit schematic of the 10-GHz VCO based on a LC-tank cross-coupled topology. Due to the use of the complementary inverters, the losses from the tank are compensated by the transconductance of both NMOS and PMOS transistors for high-frequency oscillation. Furthermore, as the output waveforms exhibits more symmetric rise and fall times, the VCO phase noise can be reduced, leading to lower timing jitter for the PLL circuit. In order to maximize the Q-factor of the tank, a symmetric layout style is utilized for the on-chip spiral inductors while the frequency

tuning is provided by AMOS varactors in this particular design.

In the proposed PLL architecture, the required frequency and phase detections are performed by separated building blocks, allowing the application of a high-frequency signal as the reference. For an input reference in the vicinity of 650 MHz, the required ratio for frequency division is 16 which is realized by cascading four divide-by-two

TABLE 3.2

The Logic Control of the I_{up} and I_{down} for the PD

Phase Detector			
$\overline{f_{DIV,I}}$	$\overline{f_{DIV,Q}}$	I_{up}	I_{down}
0	0	—	On
1	0	—	Off
0	1	—	Off
1	1	—	Off
$\overline{f_{REF}}$	$\overline{f_{DIV,Q}}$	I_{up}	I_{down}
0	0	On	—
1	0	Off	—
0	1	Off	—
1	1	Off	—

stages. In consideration of the operating frequency and quadrature output phases, a current-mode-logic (CML) topology is adopted for the divide-by-two circuits. The circuit schematic is shown in Fig. 3.9 where two CML latches are connected with a negative feedback. It is noted that, as the operating frequency monotonically decreases along the divider chain, the bias current and the load resistance of the CML stage can be

properly scaled to reduce the power consumption while maintaining the desirable voltage swing at the output.

Based on the architecture provided in Fig. 3.6, the implementation of the PD and FD are illustrated in Fig. 3.10 [6]. Note that, in order to minimize the noise contribution and dc power, the charge pump circuit is emerged with the PD and FD in this particular design. The operations of the PD and FD cells with respect to the input signals are summarized in Table 3.2 such that phase locking can be achieved at the desired output frequency. As the PLL jitter is vulnerable to the current mismatch in the CP, the channel length of the current mirrors has to be chosen carefully such that the errors resulted from the finite output resistance is minimized. By taking the tradeoff between current mismatch and operating speed into consideration, a channel length of 0.7 μm is adopted for the design of the current mirrors in the CP circuit.

3.4 Experimental Results

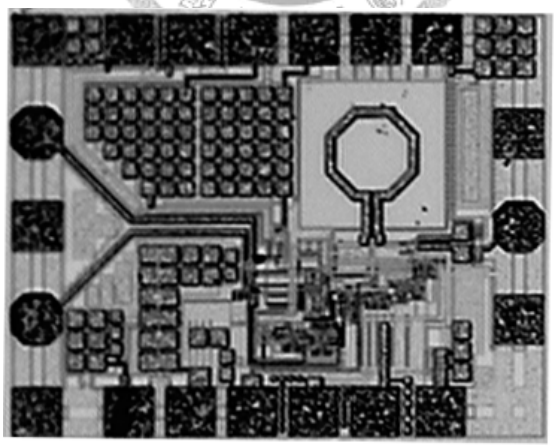


Fig. 3.11 The microphotograph of the fabricated PLL.

Fig. 3.11 shows the microphotograph of the fabricated circuit with a chip area of 0.86×0.68 mm^2 including the pads while the second-order loop filter is realized by

off-chip components. For desirable closed-loop behavior, the values of the off-chip components R_1, C_1 and C_2 are 230 Ω, 1 nF and 21 pF, respectively, in this particular

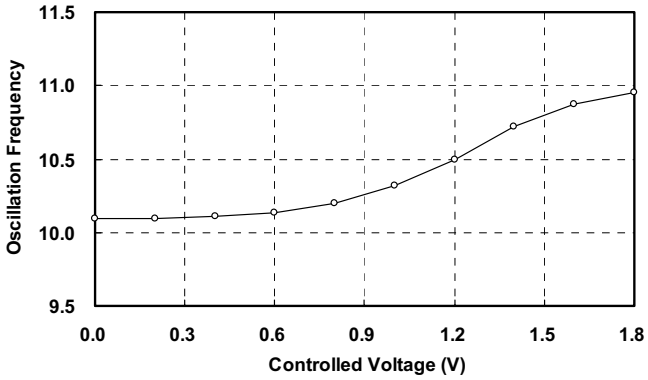


Fig. 3.12 The measured oscillation frequency of the VCO.

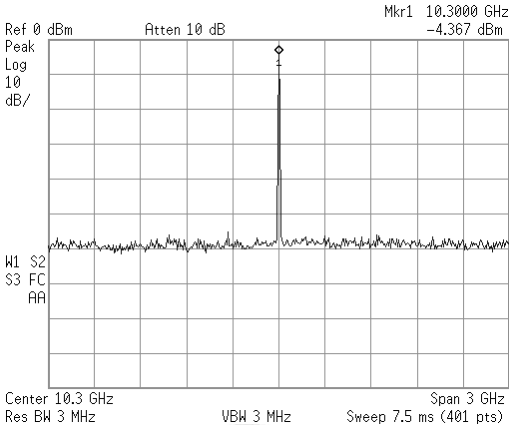


Fig. 3.13 The measured output spectrum of the fabricated circuit.

design. To characterize the performance of the PLL, the fabricated chip was mounted on a FR4 test board with SMA connectors.

Operated at a supply voltage of 1.8 V, the PLL consumes a dc power of 113 mW. Before evaluating the PLL performance, the open-loop VCO was firstly characterized and the measured results are shown in Fig. 3.12. As the controlled voltage sweeps from 0 to 1.8 V, the VCO output frequency varies from 10.1 to 11 GHz, exhibiting a tuning range of 8.5% and an average K_{VCO} of 500 MHz/V. Operating at an oscillation

frequency of 10.3 GHz, the output power of the VCO is -4 dBm.

For closed-loop operations, phase locking is achieved by the PLL over the entire

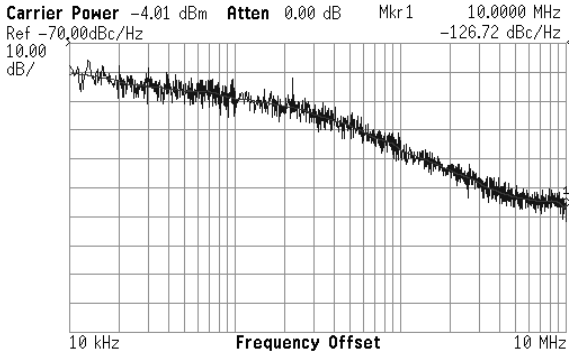


Fig. 3.14 The measured close-in output spectrum of the fabricated circuit.

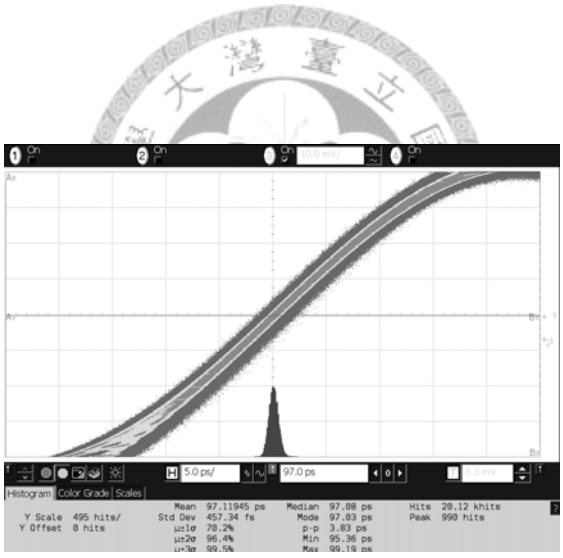


Fig. 3.15 The measured jitter histogram of the fabricated circuit.

VCO tuning range. With an input reference of 644 MHz, the measured output spectrum of the PLL at 10.3 GHz is shown in Fig. 3.13 while the close-in phase noise is illustrated in Fig. 3.14. At an offset frequency of 10 MHz, the measured phase noise at the PLL output is -126.7 dBc/Hz. By using an Agilent DSO80404B oscilloscope, the measured jitter histogram of the PLL circuit at an output frequency of 10.3 GHz is

shown in Fig. 3.15, indicating peak-to-peak and rms jitter of 3.83 and 0.46 ps, respectively. The performance of the proposed PLL circuit is summarized in Table 3.3.

TABLE 3.3

The Performance Summary of the 10-GHz PLL

Specifications	Unit	This Work	[10]	[18]
Technology	—	0.18-μm CMOS	0.18-μm CMOS	0.25-μm SiGe BiCMOS
Frequency	GHz	10.6	10.0	10.0
Supply Voltage	V	1.8	1.8	3.3
Power Consumption	mW	113	—	—
Locking Range	GHz	10.1 ~ 11	—	—
Peak-to-Peak Jitter	ps	3.83	6.5	4.8
RMS Jitter	ps	0.46	0.6	0.4

3.5 Conclusion

In this paper, circuit techniques for the design of low-jitter PLLs are presented. With the distributed PFD and CP cells and the multi-phase control scheme in the proposed architecture, the voltage fluctuation on the controlled signal of the VCO can be effectively suppressed. By decomposing the FD and PD in the circuit design, dividers with high division ratios can be prevented, eliminating additional noise sources for frequency division. Using a 0.18-μm CMOS process, a PLL circuit with low

peak-to-peak and rms jitters is successfully realized at 10 GHz for demonstration.

Chapter 4

A 10-GHz Phase-Locked Loop with a Compact Loop Filter

In this chapter, a 10-GHz phase-locked loop (PLL) is presented. By introducing a novel dual-path control in the PLL architecture, the capacitance in the low-pass filter can be effectively reduced for monolithic integration while maintaining the required loop bandwidth. As a result, the filter noise resulted from off-chip components is thus eliminated, leading to a reduced timing jitter. In addition, due to the use of decomposed phase and frequency detection, the timing jitter can be further suppressed at the PLL output without sacrificing the operating frequency range. Based on the proposed techniques, a 10-GHz PLL is implemented in a 0.18-μm CMOS process. Consuming a dc power of 113 mW from a 1.8-V supply, the fabricated circuit demonstrates a locking range from 10.1 to 11 GHz.

4.1 Introduction

Due to the device scaling in the fabrication technology, deep-submicron CMOS transistors capable for high-speed operations are commercially available. Recently, phase-locked loops (PLLs) operating at microwave and millimeter-wave frequencies have been demonstrated in standard CMOS processes provided by the foundry [11], [14], [19]. In the circuit implementations, most of the RF and mixed-signal building blocks are monolithically integrated. However, as the bandwidth is limited by the phase noise and stability issues, large capacitances are typically required in the loop filter, making it virtually impossible for single-chip system integration. In order to overcome such limitations, techniques have been proposed for the PLL circuits by employing Miller capacitor multipliers [20], [21], dual-path control [12], [22]-[24] and feed-forward strategy [25], [26]. However, as additional active devices are incorporated in the loop, these circuits suffer from significant timing jitter, especially when operating at higher frequencies. In this work, a novel PLL architecture is presented. With the modified dual-loop control and the decomposition of phase and frequency detection, fully integrated PLL is possible to be implemented without large capacitance in the loop filter while maintaining low timing jitter at the output waveforms.

The remainder of this chapter is organized as follows. Section 4.2 describes the proposed PLL architecture. Circuit design and experimental results of the 10-GHz PLL in 0.18-μm CMOS are presented in Section 4.3 and 4.4, respectively. In Section 4.5, concluding remarks are finally provided.

4.2 The Proposed PLL Architecture

4.2.1 Compact-Loop-Filter Technique

Fig. 4.1 depicts the block diagram of a conventional third-order PLL which consists of a voltage-controlled oscillator (VCO), a frequency divider, a phase/frequency detector (PFD), a charge pump (CP), and a second-order low-pass filter (LPF). Typically, the loop gain of the third-order PLL is given by

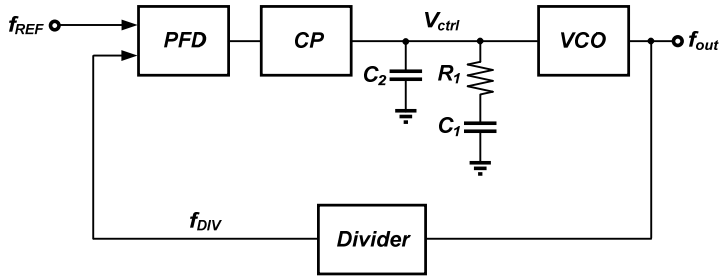


Fig. 4.1 The conventional third-order phase-locked loop.

$$G(s) = \frac{I_{cp} K_{vco} (1 + s\tau_2)}{s^2 C_2 N (1 + s\tau_1)} \cdot \frac{\tau_1}{\tau_2} \tag{4.1}$$

where I_{cp} is the charge pump current, K_{vco} is the gain of the VCO, and N represents the division ratio of the frequency divider. Note that the time constants are determined by the design values of the passive components as

$$\tau_1 = R_1 \left(\frac{C_1 C_2}{C_1 + C_2} \right) \tag{4.2}$$

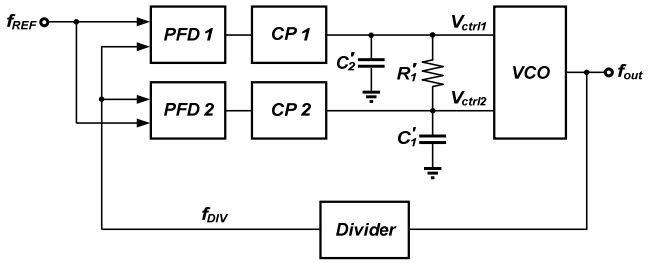
$$\tau_2 = R_1 C_1 \tag{4.3}$$

For a PLL circuit, the system stability is commonly evaluated by the phase margin. In order to facilitate the derivations, the loop gain in (4.1) is represented by a function of frequency as

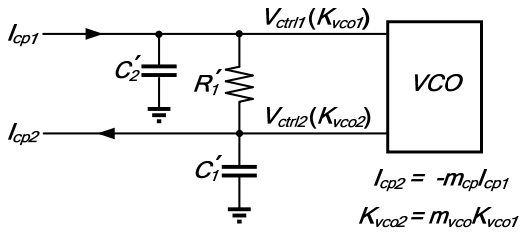
$$G(j\omega) = \frac{-I_{cp}K_{vco}(1+j\omega\tau_2)}{\omega^2 C_2 N(1+j\omega\tau_1)} \cdot \frac{\tau_1}{\tau_2} \tag{4.4}$$

Based on the frequency response, the maximum phase margin is given by

$$\phi_p(\omega_c) = \tan^{-1}(\omega_c\tau_2) - \tan^{-1}(\omega_c\tau_1) \tag{4.5}$$



(a)



(b)

Fig. 4.2. (a) The proposed architecture of the third-order phase-locked loop. (b) The illustration of the proposed technique to reduce the loop capacitors.

with a cutoff frequency

$$\omega_c = 1/\sqrt{\tau_1\tau_2} \tag{4.6}$$

On the contrary, as the values of the cutoff frequency ω_c and the phase margin ϕ_p are specified in a PLL design, the circuit parameters τ_1 and τ_2 are simply

$$\tau_1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_c} \tag{4.7}$$

$$\tau_2 = \frac{1}{\omega_c^{\,2}\tau_1} \tag{4.8}$$

Meanwhile, the required capacitance values for C_1 and C_2 in the loop filter are given by

$$C_1 = (\frac{\tau_2}{\tau_1} - 1)C_2 \tag{4.9}$$

$$C_2 = \frac{I_{cp}K_{vco}}{\omega_c^{\,2}N} \cdot \frac{\tau_1}{\tau_2} \cdot \sqrt{\frac{1+(\omega_c\tau_2)^2}{1+(\omega_c\tau_1)^2}} \tag{4.10}$$

In consideration of in-band phase noise and stability issues, the loop bandwidth in conventional PLL designs is limited within a few MHz. Therefore, the capacitance values of C_1 and C_2 are in the order of micro to nano farad, making it impractical to realize the loop filters with on-chip passive components.

To effectively reduce the capacitance value in the loop filter, a PLL architecture with a dual-loop control scheme is presented in this work. The block diagram of the proposed PLL is shown in Fig. 4.2(a). For better understanding the operation of the PLL, a conceptual illustration of the VCO controlled signals is depicted in Fig. 4.2(b). When the loop is locked, a charging/discharging current I_{cp2} is provided to the loop filter, generating a voltage signal V_{ctrl2} to control the VCO output frequency through a gain of K_{VCO2}. Meanwhile, a charging/discharging current I_{cp1} of the opposite polarity is also injected to the loop filter while the resulting signal V_{ctrl1} is utilized for VCO control with a reduced gain K_{VCO1}. Based on the superposition principle, the controlled voltages are given by

$$V_{ctrl1} = I_{cp1}\frac{1+C_1'R_1's}{s[C_1'C_2'R_1's+(C_1'+C_2')]} - I_{cp2}\frac{1}{s[C_1'C_2'R_1's+(C_1'+C_2')]} \tag{4.11}$$

$$V_{ctrl2} = I_{cp1}\frac{1}{s[C_1'C_2'R_1's+(C_1'+C_2')]} - I_{cp2}\frac{1+C_2'R_1's}{s[C_1'C_2'R_1's+(C_1'+C_2')]} \tag{4.12}$$

.

Assuming that $I_{cp2} = -m_{cp}I_{cp1}$ and $K_{vco2} = m_{vco}K_{vco1}$, the loop gain of the dual-loop PLL can be expressed as

$$G^{'}(s) = \frac{1}{N}(V_{ctrl1} \cdot \frac{K_{vco1}}{s} + V_{ctrl2} \cdot \frac{K_{vco2}}{s})$$

$$= \frac{I_{cp1}K_{vco1}}{s^2 N} \cdot \frac{(C_1^{'} - m_{vco}m_{cp}C_2^{'})R_1^{'}s + (1-m_{cp})(1+m_{vco})}{C_1^{'}C_2^{'}R_1^{'}s + (C_1^{'} + C_2^{'})} \quad (4.13)$$

With $C_1^{'} >> m_{vco}m_{cp}C_2^{'}$, the loop gain is approximated by

$$G^{'}(s) \approx \frac{I_{cp1}K_{vco1}}{s^2 N} \cdot \frac{C_1^{'}R_1^{'}s + (1-m_{cp})(1+m_{vco})}{C_1^{'}C_2^{'}R_1^{'}s + (C_1^{'} + C_2^{'})}$$

$$= \frac{I_{cp1}K_{vco1}(1+s\tau_2^{'})}{s^2 C_2^{'} N(1+s\tau_1^{'})} \cdot \frac{\tau_1^{'}}{\tau_2^{'}} \quad (4.14)$$

where

$$\tau_1^{'} = R_1^{'}(\frac{C_1^{'}C_2^{'}}{C_1^{'} + C_2^{'}}) \quad (4.15)$$

$$\tau_2^{'} = \frac{R_1^{'}C_1^{'}}{(1-m_{cp})(1+m_{vco})} \quad (4.16)$$

Again, for the evaluation of the phase margin, the frequency response of (4.14) is given by

$$G^{'}(j\omega) = -\frac{I_{cp1}K_{vco1}(1+j\omega\tau_2^{'})}{\omega^2 C_2^{'} N(1+j\omega\tau_1^{'})} \cdot \frac{\tau_1^{'}}{\tau_2^{'}} \quad (4.17)$$

Similarly, for given cutoff frequency $\omega_c^{'}$ and phase margin $\phi_p^{'}$, the time constants τ_1 and τ_2 can be expressed as

$$\tau_1^{'} = \frac{\sec\phi_p^{'} - \tan\phi_p^{'}}{\omega_c^{'}} \quad (4.18)$$

$$\tau_2^{'} = \frac{1}{\omega_c^{'2}\tau_1^{'}} \quad (4.19)$$

Therefore, the design values for the capacitances in the loop filter are given by

$$C_1^{'} = [\frac{\tau_2^{'}}{\tau_1^{'}}(1-m_{cp})(1+m_{vco}) - 1]C_2^{'} \quad (4.20)$$

$$C_2' = \frac{I_{cp1}K_{vco1}}{\omega_c'^2 N} \cdot \frac{\tau_1'}{\tau_2'} \cdot \sqrt{\frac{1+(\omega_c'\tau_2')^2}{1+(\omega_c'\tau_1')^2}} \tag{4.21}$$

Assuming that the cutoff frequency and phase margin remain the same while $K_{vco1} + K_{vco2} = K_{vco}$ and $I_{cp1} = I_{cp}$ in the circuit implementation, the required capacitance values in (4.20) and (4.21) are much smaller than those in (4.9) and (4.10). As a result, a fully integrated can be realized by employing the proposed dual-loop control in the PLL architecture.

4.2.2 PD/FD Decomposition

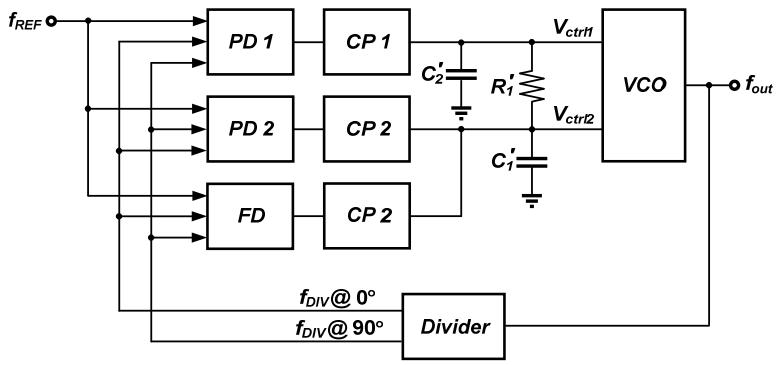
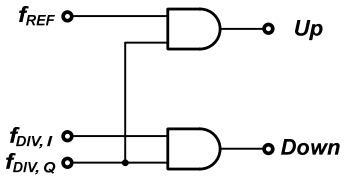


Fig. 4.3. The proposed architecture of the phase-locked loop while the phase/frequency detection is decomposed.

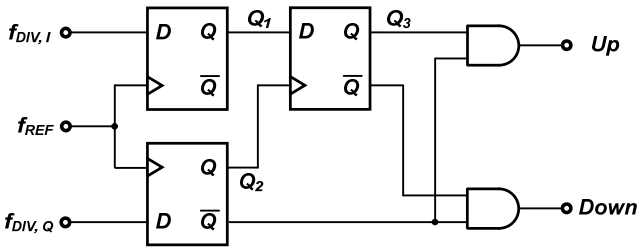
Conventionally, the tri-state D-flipflop based PFD is widely used in PLL designs. With the internal feedback loop, the operating frequency of such PFD is severely limited [15]. In order to ensure accurate phase and frequency detection, a low-frequency signal is typically utilized as the input reference while frequency dividers are adopted at the output of the VCO to generate a divided waveform to perform phase locking. As the application frequency increases, the dividing ratio for frequency division increases accordingly. The additional divider stages contribute to remarkable noise and timing jitter [16], degrading the output characteristics of the PLL circuit.

In order to overcome the design limitations, a concept of PDF decomposition [6],

[13] is adopted in this work. By replacing the PFD with separated loops for frequency and phase detection, the block diagram of the proposed dual-loop PLL is depicted in Fig. 4.3. During the locking transient, the additional frequency detection loop detects the frequency difference and provides a charging/discharging current to the loop filter. Through the controlled signal V_{ctrl2}, the VCO output is driven such that the frequency of the divided signal approaches to that of the input reference. Once the loop



(a)



(b)

Fig. 4.4 The architectures of (a) the PD and (b) the FD employed in this design.

is locked, the frequency detection loop automatically disables itself. As a result, the timing jitter due to the disturbance of the frequency detection loop can be generally eliminated at the PLL output.

In the proposed PLL architecture, the required phase and frequency detection can be realized by the circuits as shown in Fig. 4.4. Since only simple logic gates and D-flipflops are involved in the circuit implementations, the speed bottleneck associated with the conventional PFD is thus removed. As a result, a high-frequency signal can be

utilized as the input reference to reduce the number of the cascaded divider stages, leading to desirable PLL characteristics in terms of phase noise and timing jitter.

4.2.3 Design Tradeoff

With the dual-path control scheme, the capacitance values in the loop filter of conventional PLLs can be effectively reduced. Provided a phase margin of 68°, the required capacitance for various loop bandwidths are evaluated and summarized in Table 4.1. In this particular case where $m_{cp} = 0.8$ and $m_{vco} = 3$, the capacitance values can be reduced by four to five times by utilizing the proposed PLL architecture.

TABLE 4.1

THE LOOP CAPACITORS OF THE CONVENTIONAL AND PROPOSED PLLS FOR DIFFERENT LOOP BANDWIDTHS

	Conventional PLL		Proposed PLL	
Loop Bandwidth (kHz)	C_1 (nF)	C_2 (nF)	C_1' (nF)	C_2' (nF)
10	15670	615.5	3100	153.9
50	627	24.6	124	6.2
100	156.7	6.2	31	1.5
500	6.3	0.25	1.2	0.06
1000	1.6	0.06	0.31	0.015
5000	0.06	0.002	0.012	0.0006

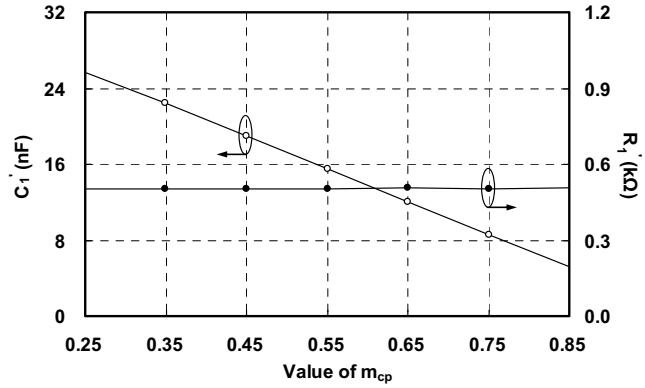


Fig. 4.5. The simulated C_1' and R_1' with the sweep of m_{cp} for a fixed m_{vco}.

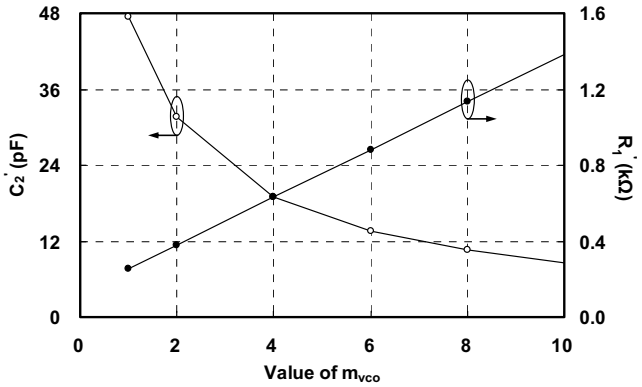


Fig. 4.6. The simulated C_2' and R_1' with the sweep of m_{vco} for a fixed m_{cp}.

To have better understanding on the proposed technique, design tradeoffs for the circuit parameters are illustrated. With a loop bandwidth of 700 kHz and phase margin of 84°, the calculated values of C_1', C_2' and R_1' versus the CP current ratio m_{cp} are illustrated in Fig. 4.5. For simplicity, a fixed gain ratio m_{vco} of 3 is utilized in the calculation. As indicated in (4.21), the value of C_2' does not change significantly with m_{cp}. However, the required capacitance C_1' is strongly influenced by the CP current ratio. By increasing the design parameter m_{cp}, the value of C_1' can be effectively reduced. It is noted that, in practical circuit implementations, the current ratio m_{cp} is

limited by the transient response of the system. If m_{cp} is excessively large, the loop characteristics are thus dominated by I_{cp2}, which may lead to difficulties for the PLL to be locked. Alternatively, with a fixed m_{cp} of 0.7, the calculated resistance and capacitance for the loop filter are demonstrated in Fig. 4.6. On the contrary, as the VCO gain ratio m_{vco} increases, C_1' is virtually unchanged while the value of C_2' decreases. To sustain the required loop bandwidth, the resistance R_1' also increases with m_{vco}. As additional thermal noise is contributed by R_1', the timing jitter at the output waveforms is at stake. Therefore, the design parameters, especially for m_{cp} and m_{vco}, have to be chosen carefully in the proposed PLL architecture for optimum circuit performance.

4.3 Circuit Implementation

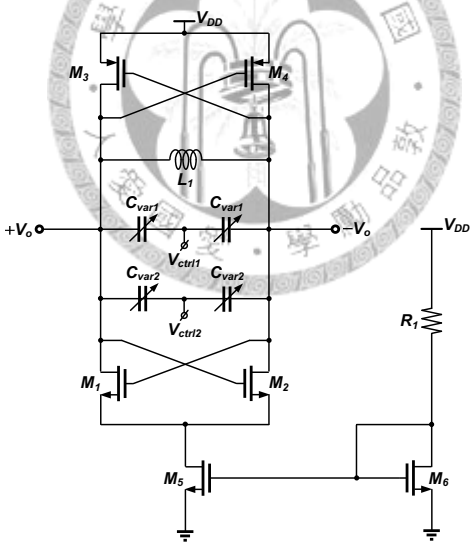


Fig. 4.7 The VCO employed in this work.

Based on the proposed circuit architecture, a 10-GHz PLL is realized in a 1P6M 0.18-μm CMOS process provided by the foundry. With device layout optimized for the

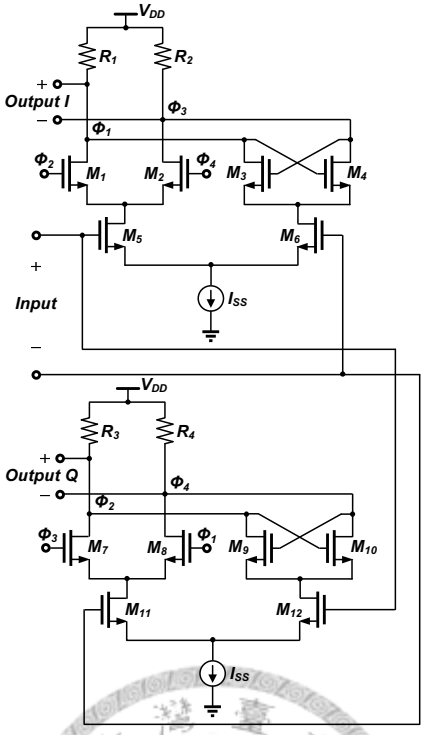
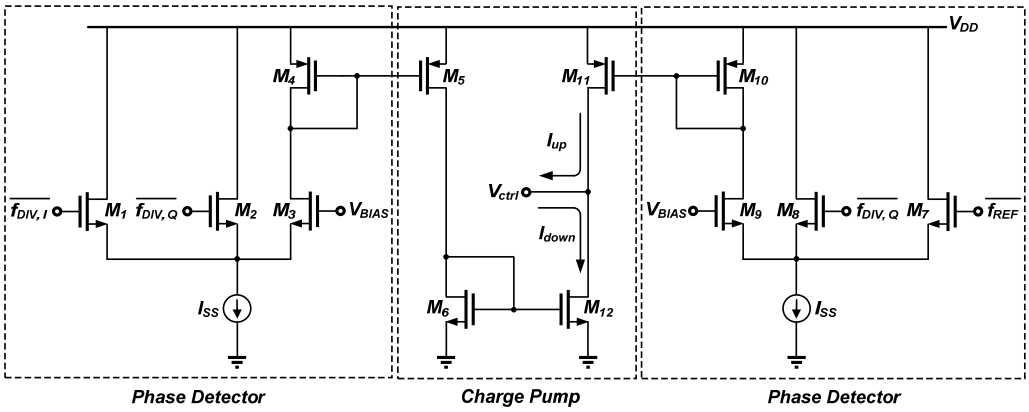


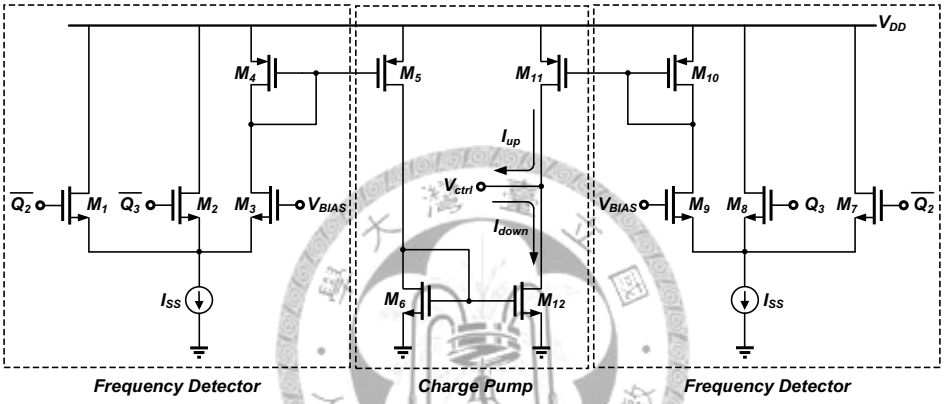
Fig. 4.8 The divide-by-two frequency divider using the current-mode logic.

RF performance, the n-channel MOSFET in a deep n-well exhibits a cutoff frequency f_T up to 50 GHz. As for the on-chip passive components, a top AlCu metallization layer with a thickness of 2 μm and the MIM structure with oxide intermetal dielectric are provided in this technology.

With the dual-path control in the proposed architecture, the required capacitance values in the loop filter can be effectively reduced, making it possible for the implementation of fully integrated PLLs. Due to the absence of off-chip components, the noise presented in the VCO controlled line is eliminated. As a result, lower timing jitters can be achieved at the output waveforms of the PLL circuits. Based on the derivations in Section 4.2, the PLL characteristics are strongly influenced by the circuit parameters m_{cp} and m_{vco}, which are 0.7 and 3, respectively, in this particular design.



(a)



(b)

Fig. 4.9. The adopted (a) PD with the charge pump and (b) FD with the charge pump.

For the VCO operating at the 10-GHz frequency band, a LC-tank circuit topology with complementary cross-coupled pairs is employed. Fig. 4.7 shows the circuit schematic of the VCO. As the transconductances of the NMOS and PMOS devices are utilized to compensate for the losses from the tank, the power consumption required for sustained oscillation is thus reduced. Furthermore, due to the use of complementary circuit topology, more symmetric waveforms are presented at the VCO output. The up-conversion of the 1/f noise can be generally minimized, leading to lower close-in phase noise for the VCO and enhanced output characteristics for the PLL [17]. To facilitate the dual-path control scheme, the frequency tuning is achieved by V_{ctrl1} and V_{ctrl2} while the desirable m_{vco} is realized by properly selecting the device sizes for C_{var1}

TABLE 4.2

The Logic Control of the I_{up} and I_{down} for the PD

Phase Detector			
$\overline{f_{DIV,I}}$	$\overline{f_{DIV,Q}}$	I_{up}	I_{down}
0	0	—	On
1	0	—	Off
0	1	—	Off
1	1	—	Off
$\overline{f_{REF}}$	$\overline{f_{DIV,Q}}$	I_{up}	I_{down}
0	0	On	—
1	0	Off	—
0	1	Off	—
1	1	Off	—

and C_{var2}.

By adopting the PFD decomposition technique in the PLL design, the frequency of the input reference can be increased to minimize the number of the divider stages. For an input reference of 643.75 MHz, the required dividing ratio to generate the low-frequency replica signal is 16. In consideration of the operating speed and the quadrature output phases, the frequency division is provided by four divide-by-two stages in cascade, each consisting of a current-mode-logic (CML) D-flipflop with a negative feedback. Fig. 4.8 shows the schematic of the divide-by-two circuit. It is noted that, as the operating frequency monotonically decreases along the divider chain, the

bias current and the load resistance of the CML stages are properly scaled such that the power consumption can be minimized while maintaining the desirable voltage swing at the output.

Based on the block diagram in Fig. 4.4, the implementations of the PD and FD are illustrated in Fig. 4.9. In order to minimize the noise contribution and power consumption, the charge pump is incorporated with the PD and FD in this design. The operations of the PD and FD cells with respect to the input signals are summarized in Table 4.2 to perform the phase locking at the desired output frequency. As the PLL output characteristics are vulnerable to current mismatch in the CP, the channel length of the current mirrors has to be chosen carefully such that the errors resulted from the finite output resistance is minimized. By taking the tradeoff between current mismatch and operating speed into consideration, a channel length of 0.7 μm is adopted for the design of the current mirrors in the CP circuits.

4.4 Experimental Results

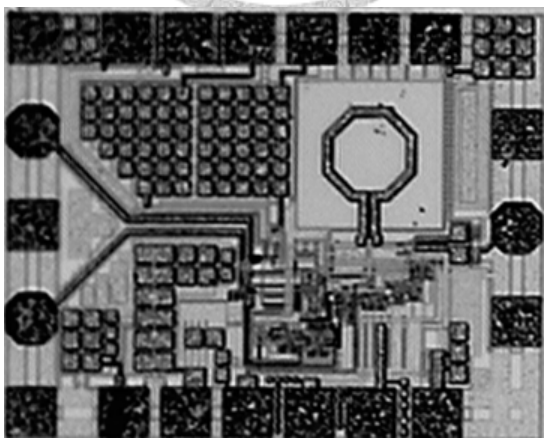


Fig. 4.10. The microphotograph of the fabricated PLL.

Fig. 4.10 shows the microphotograph of the fabricated circuit with a chip area of 0.86×0.68 mm^2 including the pads. In order to characterize the performance of the PLL

circuit, the chip was mounted on a FR4 test board with SMA connectors.

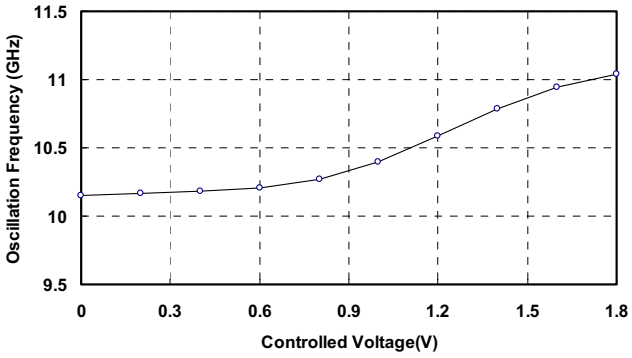


Fig. 4.11. The measured oscillation frequency of the VCO.

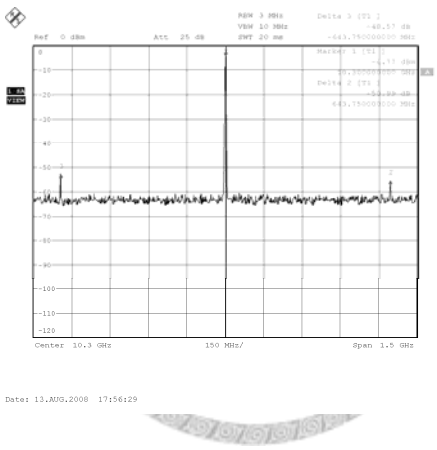


Fig. 4.12. The measured output spectrum of the fabricated circuit.

Operated at a supply voltage of 1.8 V, the overall power dissipation of the PLL including the buffers is 113 mW. Before measuring the performance of the PLL, the open-loop VCO was firstly characterized. Fig. 4.11 shows the measured output characteristic of the VCO. By sweeping the controlled voltage of the VCO from 0 to 1.8 V, the oscillation frequency varies from 10.1 to 11 GHz, exhibiting a frequency tuning range of 8.5% and an average gain (K_{VCO}) of 500 MHz/V. At an output frequency of

10.3 GHz, the VCO demonstrates an output power of -4.77 dBm.

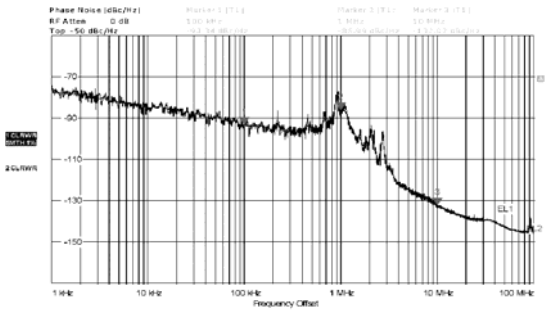


Fig. 4.13. The measured close-in output spectrum of the fabricated circuit.

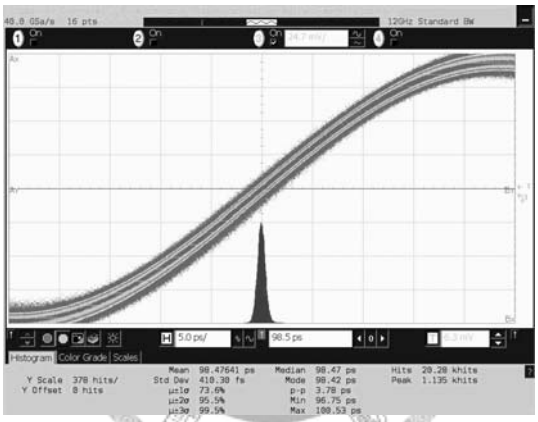


Fig. 4.14. The measured jitter histogram of the fabricated circuit.

The performance of the closed-loop PLL is then evaluated. With a reference frequency of 643.75 MHz, the measured output spectrum of the loop locked at 10.3 GHz is shown in Fig. 4.12. The close-in output spectrum of the fabricated circuit is shown in Fig. 4.13, indicating a phase noise of -132 dBc/Hz at an offset frequency of 10 MHz. By using an Agilent DSO80404B oscilloscope, the measured jitter histogram is shown in Fig. 4.14. As the PLL operates at an output frequency of 10.3 GHz, the peak-to-peak and rms jitters are 3.78 and 0.41 ps, respectively. The performance of the proposed PLL circuit is summarized in Table 4.3.

TABLE 4.3

The Performance Summary of the 10-GHz PLL

Specifications	Unit	This Work
Technology	—	0.18-μm CMOS
Frequency	GHz	10.3
Supply Voltage	V	1.8
Power Consumption	mW	113
Locking Range	GHz	10.1 ~ 11
Peak-to-Peak Jitter	ps	3.78
RMS Jitter	ps	0.41

4.5 Conclusion

This paper presents a 10-GHz PLL with a compact low-pass filter in a standard 0.18-μm CMOS process. By employing a dual-path topology for the VCO controlled signals, the required capacitance in the loop filter can be substantially reduced while maintaining the desirable loop bandwidth. In addition, the PFD decomposition technique is also adopted such that the noise contributed by the frequency dividers can be minimized. The proposed circuit architecture is well suited for the implementation of fully integrated PLLs with reduced peak-to-peak and rms jitters at microwave and millimeter-wave frequencies.

Chapter 5

A 30-GHz Phase-Locked Loop

In this chapter, a 30-GHz phase-locked loop is presented. The PLL is designed and implemented with CMOS 0.18-μm process. The modified Colpitts VCO is employed for the reduction of the phase noise and the inductive peaking regenerative frequency divider is used to enhance the dividable range while operate at high frequency. The simulation demonstrates that the phase noise of the adopted 30-GHz VCO is below -105 dBc/Hz at 1MHz frequency offset and the PLL exhibits reference spur of -74 dBc.

5.1 Introduction

The PLL is the key component in the communication transceiver. In the contemporary PLL design and implementation, speed and noise are always two crucial issues to be traded off. As the process advances, higher VCO gain is inevitable with reasonable tuning range because of the increased operating frequency and the shrunk supply voltage. High VCO gain may even degrade system performance because the clock period is already comparable to the jitter in high speed applications.

Recently, many high speed PLL designs have been presented [12], [27], [28], but

they usually require high supply voltages and large power consumption. In this chapter, a high frequency 30-GHz PLL designed with 0.18-μm CMOS technology is illustrated. The design concentration is focused on the reduction of the noise contribution of the VCO in the PLL since the VCO is one of the major noise sources.

5.2 Architecture

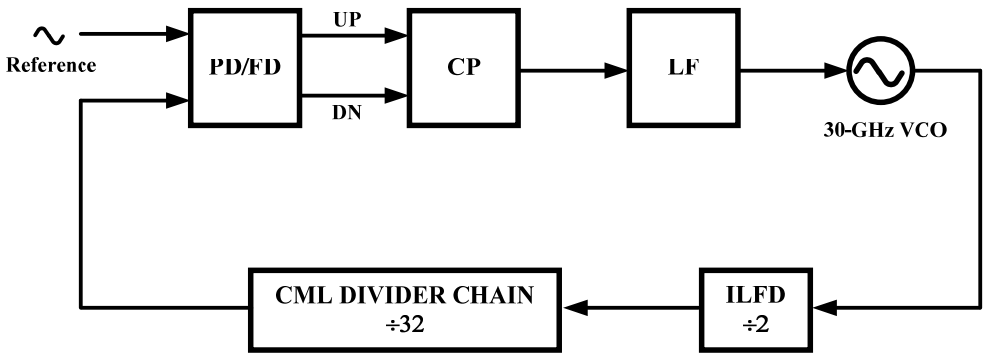


Fig. 5.1 The 30-GHz PLL architecture.

The 30-GHz PLL consists of a PD/FD, charge pumps, a second-order loop filter, a VCO, an injection-locked frequency divider (ILFD), and a chain of current-mode logic (CML) dividers. The first divide-by-2 stage is implemented with the regenerative injection-locked frequency divider due to its high operation frequency. As for the latter stages of dividers, which operate at relatively low frequency, the CML-based frequency divider is employed for wider tuning range and area saving. The modified Colpitts VCO is adopted to achieve improved phase noise. The PFD is also decomposed to the PD and FD to minimize jitter while keeping a wide acquisition range [6].

5.3 Circuit Implementation

5.3.1 The Modified Colpitts VCO

The schematic of the adopted VCO is shown in Fig. 5.2 [29]. Due to the inherently low flicker noise compared with the nMOS counterpart [30], the cross-coupled pair and the tail current transistor are realized by pMOS devices. In addition, a modified differential Colpitts architecture is adopted to reduce the phase noise at the VCO output.

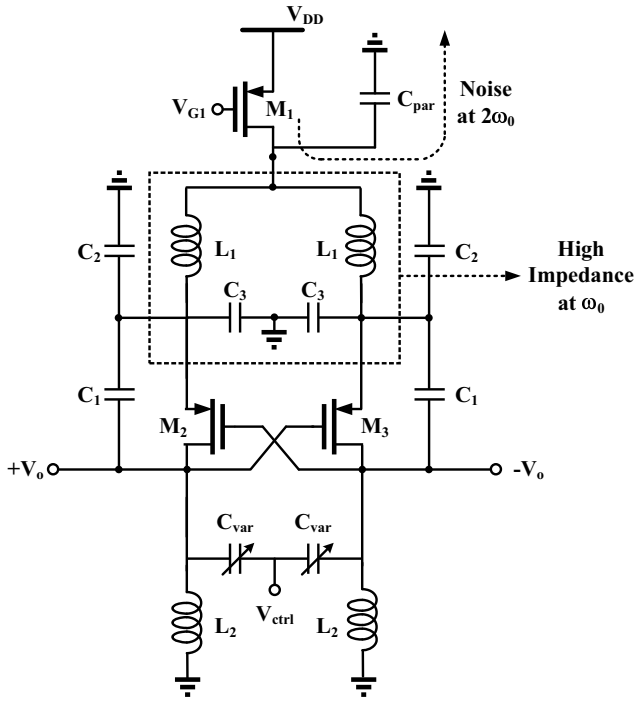


Fig. 5.2 Schematic of the adopted VCO.

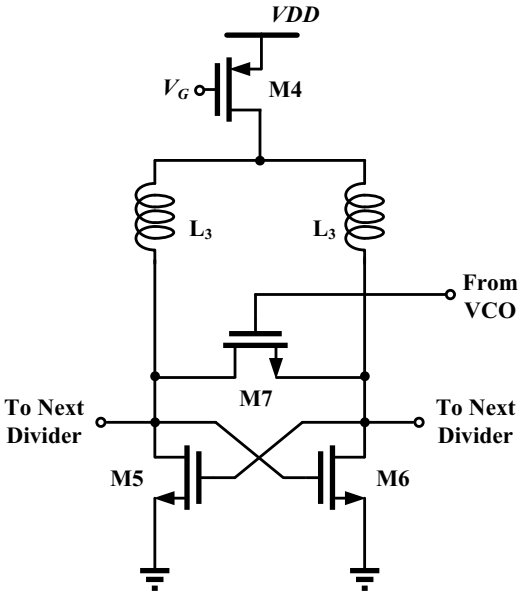
Typically, the Colpitts oscillator possesses better noise characteristics accompanied by relatively stringent startup conditions, especially at higher frequencies. In order to alleviate such limitations, the g_m-boosting technique [31] is introduced in this design. As indicated in Fig. 5.2, the equivalent admittance by looking into the drain terminals of the cross-coupled pair is approximated by

$$Y_{in} = -\frac{g_m \omega^2 C_2 (2C_1 + C_2)}{g_m^2 + \omega^2 (C_1 + C_2)^2} + j\frac{\omega^3 C_1 C_2 (C_1 + C_2) - g_m^2 \omega C_2}{g_m^2 + \omega^2 (C_1 + C_2)^2} \quad (1)$$

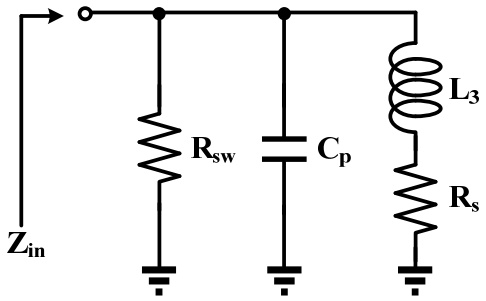
where g_m means the transconductance of the cross-coupled pair. The negative conductance is increased by a factor of $(2 + C_2/C_1)$ compared with conventional Colpitts oscillators [30]. Hence, the equivalent transconductance of the cross-coupled pair can be effectively enhanced, resulting in more relaxed startup conditions and reduced power dissipation for the VCO design. It is noted that, similar to a Colpitts oscillator, the proposed VCO also benefits from the desirable cyclostationary noise properties [32] with superior performance in terms of the phase noise. Furthermore, because of the use of on-chip inductance and the in-phase relationship established by the capacitive feedback, the drain and source voltages swing above the supply voltage and below the ground potential.

In the VCO topology, the bias current is defined by the tail transistor M_1 to achieve the stable output power level. However, the thermal noise contributed by the tail transistor at the second harmonic frequency may lead to the VCO phase noise degradation. In order to suppress the noise contribution from the tail transistor, a noise-filtering technique [33] is also employed in this VCO design with the adoption of the LC-network L_1 and C_3. As the inductor L_1 resonates with C_3 at the oscillation frequency ω_0, the fundamental operation of the VCO is not influenced by the additional filtering network. On the other hand, with the high impedance provided by L_1 at the second harmonic frequency, the thermal noise from the tail transistor is directed to the low-impedance path provided by the parasitic capacitance, leading to improved VCO performance in terms of the output phase noise.

5.3.2 Regenerative Frequency Divider



(a)



(b)

Fig. 5.3 (a) Schematic and (b) simplified circuit model of the injection-locked frequency divider.

In order to facilitate high-frequency operations at 30 GHz, the first divide-by-2 circuit can be implemented with the injection-locked frequency divider, as illustrated in Fig. 5.3(a), where the direct signal injection is provided through the switching transistor M7. Given that the free-running frequency of the LC-tank cross-coupled pair is approximately half of the input frequency, a divided signal appears at the output under

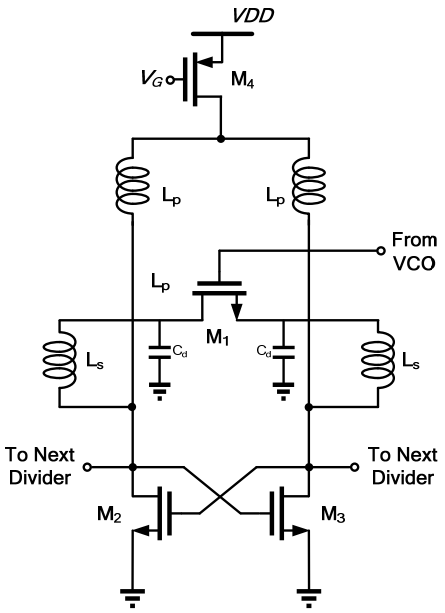


Fig. 5.4 Circuit schematic of the regenerative frequency divider.

injection-locked conditions. Typically, the injection-locked divider exhibits unparalleled advantages for the high operating frequency and low power consumption. However, the inferior input locking range is the serious concern in practical circuit implementation. The limited locking range due to the high-Q resonators makes it difficult to cover the frequency tuning range of the VCO under process and temperature variations. The input locking range is inversely proportional to the Q factor of the tank. Supposed the losses from the inductors and the capacitors are negligible compared with the on resistance of M7, the simplified circuit is employed for the analysis purpose, as shown in Fig 5.3(b). The Q factor of the tank can be given by

$$Q \approx \frac{R_{sw}}{\omega_r L_3} = \frac{\sqrt{C_p / L_3}}{2\mu_n C_{ox}(W/L)_7 (V_{G7} - V_{S7} - V_{th})} \tag{2}$$

where R_{sw} is the on resistance of the switching resistor, C_p is the equivalent shunt capacitance, and ω_r is the resonant frequency of the tank. It is noted that the value of R_{sw}

decreased as the gate bias of M7 increased, leading to a poor quality factor of the tank.

In order to achieve wider locking range for the injection-locked divider, the regenerative frequency divider has been presented without using varactors for frequency tuning [34]. Fig. 5.4 depicts the 30-GHz regenerative frequency divider with the series-peaking technique. The series-peaking inductors effectively enhance the loop gain and thus increase the voltage amplitude at the drains of the switching transistor. The simulation results indicate the tuning range is widen indeed.

5.4 Simulation Results

5.4.1 The behavior model simulation

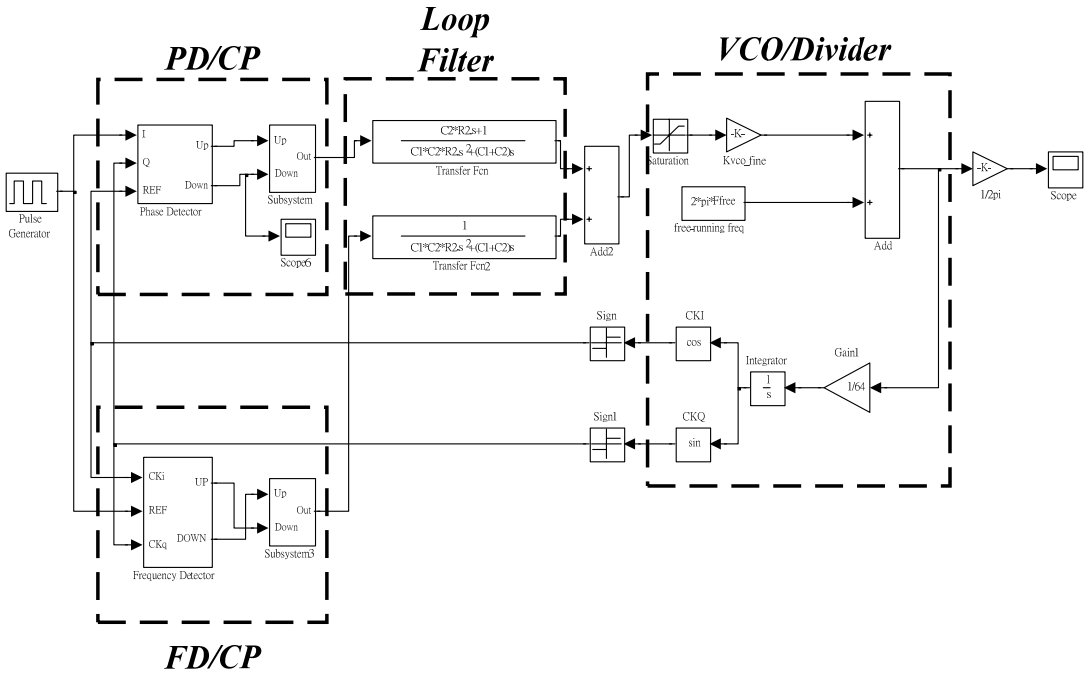


Fig. 5.5 The behavior model for the 30-GHz PLL.

Fig. 5.5 shows the linear behavior simulation model used in this design. With the wide loop bandwidth, the PLL locks to the desired frequency in several μs according to

the behavior simulation results. The PD and FD are realized by ideal digital D-flipflops and the VCO is modeled as an ideal linear frequency integrator. The loop filter is designed as a second-order filter, as shown in Fig. 5.7, the design value is shown as Table. 5.1. The loop bandwidth is designed as 1MHz and the phase margin is 68°.

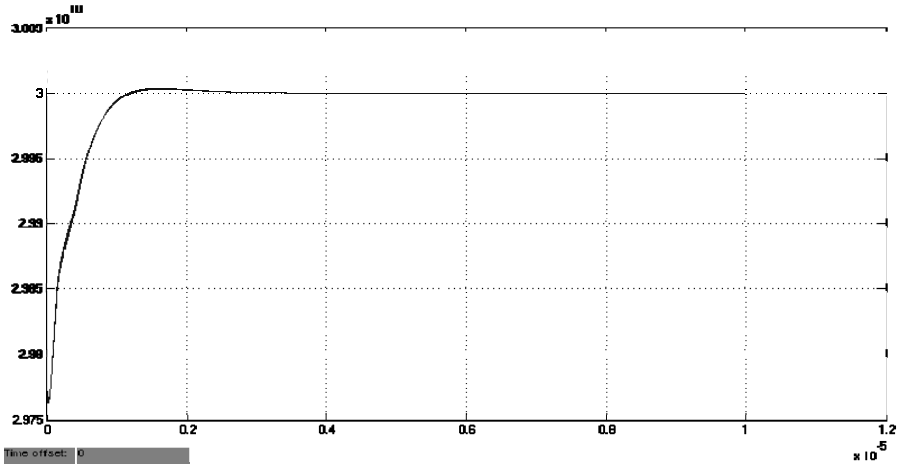


Fig. 5.6 The locking process of the behavior model.

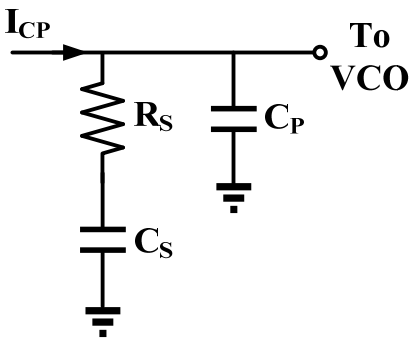


Fig. 5.7 The second-order loop filter in this design.

Table 5.1
The design value of the loop filter.

Rs	4.64k
Cs	176.33pF
Cp	6.9pF
Bandwidth	1MHz
Phase margin	68°

5.4.2 The modified Colpitts VCO and the regenerative frequency divider

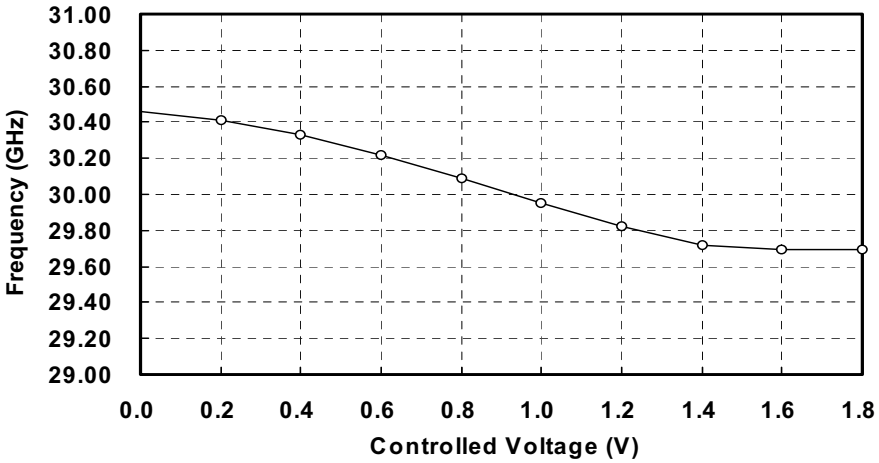


Fig.5.8 The simulated tuning range of the VCO.

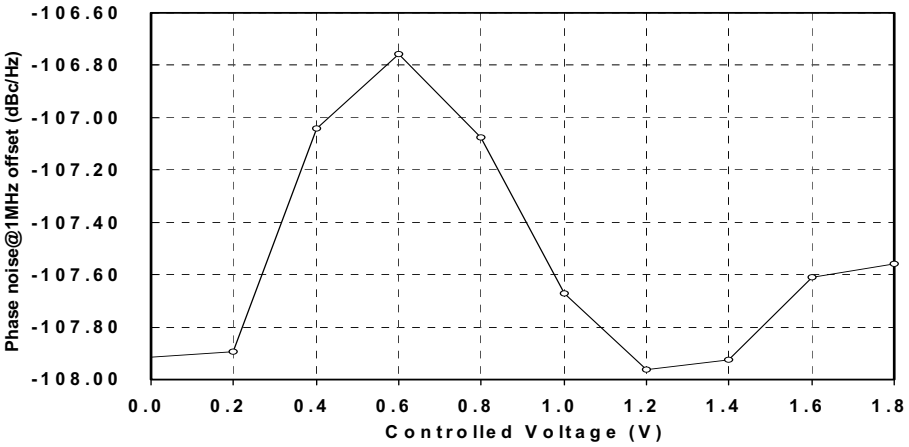


Fig. 5.9 The simulated phase noise at 1MHz offset.

Fig. 5.8 shows the simulation results for the tuning range of the VCO in this design. The corner and simulation temperature are set to TT25° at the 1.8V supply voltage. Even with 10% variation, the tuning range is still above 700MHz and the phase noise of the VCO is always below -105 dBc/Hz according to the simulation results. As for the

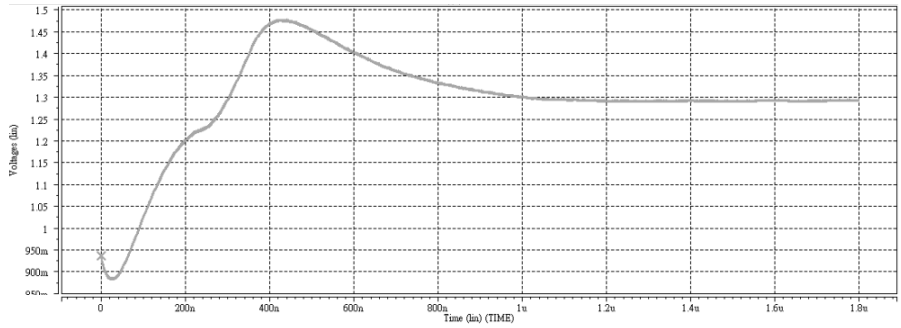


Fig. 5.10 The locking process of the 30-GHz PLL.

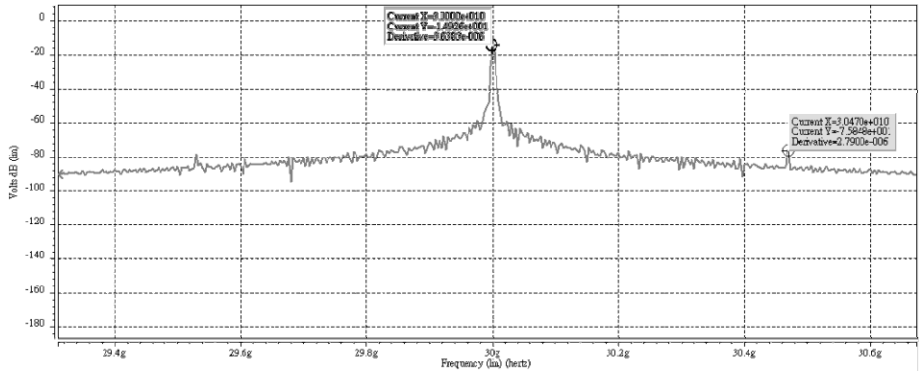


Fig. 5.11 The frequency spectrum of the output clock.

regenerative frequency divider, the dividable range is wider than 8GHz with different corner and temperature variations for 0dBm input power, which is much larger than the tuning range of the VCO. Fig. 5.10 shows the circuit-level locking process. The FFT of the clock signal under locked condition is shown in Fig. 5.11, which indicates the reference spur is about -74 dBc. The simulated performance summary is concluded in Table. 5.2 and Fig. 5.12 exhibits the layout of the PLL.

5.5 Conclusion

Table. 5.2

The 30-GHz PLL performance summary.

Technology	TSMC 0.18um CMOS
Frequency range	29.69 GHz ~ 30.46 GHz
Division	64
Reference Spur	-74.35dBc
Avg. VCO Gain	455 (MHz/V)
Charge Pump Current	100 uA
Phase Margin	68°
Loop BW	1MHz
Power consumption	124mW
Chip area	0.813 × 0.826 mm^2

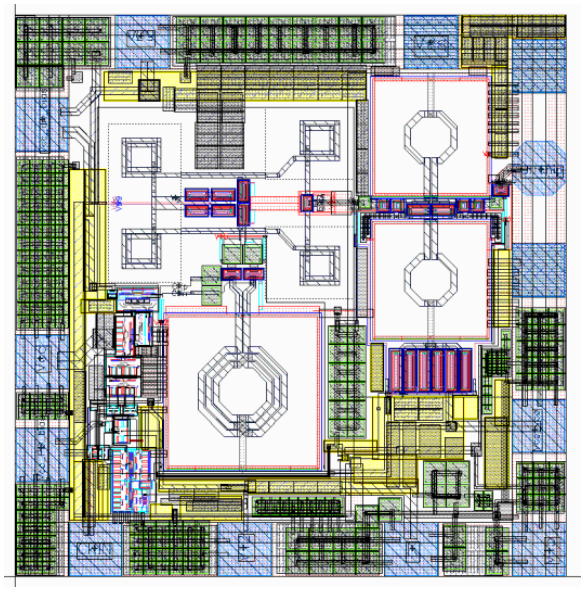


Fig. 5.12 The layout of the 30-GHz PLL design.

The design and analysis of a low-noise 30-GHz PLL has been presented in this chapter. With the implementation of the modified Colpitts architecture, the phase noise of the VCO is effectively suppressed. The first divider stage is implemented with the regenerative injection-locked divider to ensure a wide tuning range at the high operating frequency and resist the process variations. Simulation results exhibit the reference spur of approximately -74dBc. The power consumption is 124 mW from a supply voltage of 1.8V.

Chapter6

Conclusion

In this thesis, three high-frequency PLLs are demonstrated. In chapter 3, a high-frequency PLL with the multi-phase control architecture are proposed to solve the reference feedthrough issue. By employing multi-phase control in the distributed phase/frequency detectors (PFDs) and charge pumps, the ripple caused from the reference feedthrough on the controlled signal of the voltage-controlled oscillator (VCO) is effectively reduced. The multi-phase control architecture is demonstrated in a 10-GHz PLL and realized by standard 0.18-μm CMOS technology. The measured results indicate that the peak-to-peak and rms jitters are 3.83 and 0.46 ps, respectively.

A high-frequency PLL with dual-path loop architecture is also presented in chapter 4. By introducing a dual-path control in the PLL, the required capacitance in the low-pass filter can be effectively reduced, making it possible to integrate the capacitor into the fabricated chip. The jitter performance of the PLL would be improved because the filter noise from the off-chip component is decreased. Moreover, the phase and frequency detections are further decomposed to minimize the jitter while maintaining a wide operation range. Implemented in a standard 0.18-μm CMOS process, the measured results indicate that the peak-to-peak and rms jitters are 3.44 and 0.42 ps, respectively.

Conclusion

Chapter 5 presents a 30-GHz PLL. The phase noise of the VCO is improved by employing the modified Colpitts VCO with positive capacitor feedback to relax the oscillation startup condition at such high frequency. Also, the first stage of the frequency divider is implemented with the regenerative inductive peaking divider which provides high-speed frequency division at low power consumption with a broad tuning range. According to the simulation results, the VCO shows -105 dBc/Hz phase noise at 1 MHz offset and the locked PLL output signal exhibits approximately -74 dBc of the reference spur.

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