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於玻璃基板與塑膠基板上製作
高效能氧化鋅薄膜電晶體

High Performance ZnO Thin Film Transistors
on Both Glass and Plastic Substrates

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高效能氧化鋅薄膜電晶體
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本論文係 劉建承 君（R94941024）在國立臺灣大學光電工程學研究所完成之碩士學位論文，於民國九十六年七月十七日承下列考試委員審查通過及口試及格，特此證明

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謝　誌

今年早春特地赴會椰林大道上的杜鵑花季，她們仍然開得那麼理直氣壯，頗有「乃校」之風；荏苒光陰，幾場梅子雨，幾件羽毛衣，回首兩年多在台大的研究生涯，也曾經如此理直氣壯，漸漸，卻也學會真正用心傾聽。

由衷感謝指導老師黃建璋博士在學術研究上的悉心引導，不僅在研究主題上給予精闢的指導及見解，也讓我有機會參與資策會無線網路感測的計畫，從中學習到天線傳播的相關理論；另外，在協助帶領大學部光電實驗的電光調變器實驗中，也學到不少有趣的應用，這趟碩士班的學涯，收穫良多。也感謝口試委員陳奕君教授以及陳敏璋教授不吝指教，而讓這本論文更具完整性。

由衷感謝 402 實驗室的所有夥伴們。和育昇一起分享討論實驗、製程、原理以及女人，挑燈夜戰馬力歐賽車為的是那些令人又愛又恨的data；和下巴、子樸、子揚、志豪共度豬羊變色的那些夜晚；和成熟穩重的旻諺哥以及倜儻瀟灑萬人迷小銘討論深奧的物理；兩位博班學長正彬哥、柯董真是實驗室活力的泉源；還有可愛的學弟們孟倫、振印、弘憲、雨儀、原禎，光中、世驊、小潘、宏禮，你們讓 402 充滿了無盡的歡笑。

由衷感謝方瑜老師，弭平了我左腦和右腦的齟齬，讓我的生活不致分裂而得以發展更完整的性靈。或快或慢，或理性或感性，或邏輯或用情...；學會用我的兩種步伐，陪著我平穩前進。學會不偏廢任一種心智，隨心所欲，隨緣立善，「妻子」和「情人」一樣，都得用力珍惜。

也感謝在台北求學階段一路相伴的所有好朋友：口條清晰報新聞的專家「查爾頓」，適合當聊天系藝人的「大柔」學妹，走音救星吉他手「小綿羊」，十年深厚交情小吃攤正妹「花枝」和「米粉」，遠在溫哥華的重量級笑話高手「鄧弼」，聊心事的話匣子「痞堅」，未來的大作家「志摩」弟，大學麻吉「國勳」、「家豪」、「譽達」、「奕寰」...，族繁不及備載；和你們一起朝馳江皐，夕濟西澨，上山下海，放任我們的年少輕狂於歌聲笑語中，我們一起拼湊的燦爛時光，都將積澱在我的漫漫長夜裡。

最大的感謝要獻給老爸、老媽，你們無怨悔的支持以及全然的信任，使我可以安心地去實踐我的志願及夢想；夜闌人靜時，憶起老爸的千萬交代「要活得快樂」，竊想有這麼開明的父母親，人生就足以快活了。小時候住在家裡面，長大了之後，我的家，反而住進了我裡面，如影隨形。

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2007 年 7 月 25 日於台北長興街

Abstract

This thesis focuses on two aspects of ZnO thin film transistors, the ZnO-TFTs fabricated on glass substrates and the flexible ZnO-TFTs fabricated on polymer substrates.

The first part demonstrates a high-performance enhancement-mode ZnO TFT on a glass substrate. Before realizing the TFT device, the characteristics of ZnO thin films are examined to find out the optimal deposition conditions. The ZnO thin film is deposited by RF magnetron sputtering with the presence of O_2 at low deposition rate and low temperature. The I_{DS} of the ZnO-TFT on glass substrates is as high as 1 mA when biased at the saturation region V_{DS} = 10-20 V and V_{GS} = 5 V without any post thermal anneal. The I_{on}/I_{off} ratio is 3×10^6. We believe the results are among the best ZnO TFTs ever obtained.

The second part focuses on the flexible ZnO-TFT on PET (polyethylene terephthalate) substrates. All the patterns are defined by standard photolithography with only two steps in order to reduce the distortion of PET substrates. The ZnO thin film is deposited by RF magnetron sputtering at low temperature in presence of O_2. The gas flow ratio of Ar to O_2 is based on the optimal conditions obtained in the case of the ZnO-TFTs on glass substrates. Titanium is also employed in substitution for ITO as the source and the drain layers to improve the electrical performance. The I_{DS}–V_{DS} curves along with optical transmission of the whole TFT are presented.

摘 要

本論文研究製作於玻璃基板與塑膠基板上之氧化鋅薄膜電晶體的特性。

在實現薄膜電晶體元件之前，本文首先探討氧缺陷對氧化鋅薄膜導電特性的影響，藉由濺鍍沉積氧化鋅薄膜時控制 Ar 和 O_2 的比例，以及利用氧電漿對氧化鋅薄膜表面進行處理，以獲得最佳製備氧化鋅薄膜的成長環境。根據此最佳化條件，本研究在玻璃基板上製作出高效能增強型氧化鋅薄膜電晶體，在 V_{DS}=10–20，V_{GS}=5V 的偏壓下，操作電流可高達 1mA，開關電流比可達 3×10^6，是目前氧化鋅薄膜電晶體的研究工作中，效能表現最好之一。

本文進一步探討製作於塑膠基板上之氧化鋅薄膜電晶體的特性。採用兩步驟的黃光製程，以防止塑膠基板在化學溶劑中產生變形；而受限於塑膠基板的玻璃轉換溫度，所有薄膜均在室溫下濺鍍成長，氧化鋅的成長條件是利用玻璃基板上的最佳結果。另外，採用金屬鈦作爲汲極和源極，以改善接觸電阻。塑膠基板上之氧化鋅薄膜電晶體的電特性曲線和可見光穿透率均本文中亦有論及。

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High Performance ZnO Thin Film Transistors on Both Glass and Plastic Substrates

Chapter 1
Introduction

In 1962, P. K. Weimer presented the first thin-film transistor (TFT) with a micro-crystalline cadmium sulfide semiconducting channel layer, an evaporated gate dielectric, and gold source, drain, and gate contacts [1].

In 1988, when a 14-in active-matrix (AM) TFT display was demonstrated, the electronics industries then recognized that the dream of a wall-hanging television had become a reality, thus promoting liquid crystal display (LCD) manufacturers to the "major leagues" in the electronics industry [2]. The TFT technology figured as a brilliant technology for active-matrix liquid-crystal displays (AM-LCD) with the advent of amorphous or poly-crystalline silicon as the semiconducting channel material. Nevertheless, the opaque Si-based TFTs curtailed the aperture ratio of conventional TFT-LCDs. Transparent thin film transistors thus emerged as the new focus for TFT-LCDs.

The candidates in the transparent electronics field have been mainly with respect to oxide semiconductors such as zinc oxide, tin dioxide, indium zinc oxide, etc. **This thesis in the first place is devoted to the discussion of the development of fabricating zinc oxide thin film**

transistors on glass substrates.

The cathode ray tube (CRT) and AM-LCD recently celebrated their 100th and 25th anniversary, respectively [3]. The arrival of portable electronic devices has put a premium on durable, lightweight, and inexpensive display component, which triggers the research on flexible electronics. Moreover, flexible display technology enables flexible electronics devices such as electronic papers (e-paper) to be “green” products in substitution for paper. As we know it, “Greenhouse Effect” concerns all human beings in the global world in the 21st century. Fig. 1.1 shows some display application of flexible electronics [4].

The convergence of state-of-the-art technologies (substrates, conducting layers, barrier layers, electro-optic materials, thin film transistor technologies, and manufacturing process) is accelerating the flexible flat panel display concept closer to commercial reality. **The thesis secondly investigates the characteristics of flexible zinc oxide thin film transistors on a polymer substrate.**

This thesis is organized as follows.

Chapter 2 “*Literature Review and Theory*” provides background information including overviews of transistors, previous work both in the Si-based and transparent TFT fields for a comparison of the work presented in this thesis, material properties, substrate properties, and sputtering technology background.

Chapter 3 “*Fabrication of ZnO TFTs on a Glass Substrate*” consists of

device fabrication procedures for glass substrates and describes results obtained with regard to the ZnO TFTs developed in this work.

Chapter 4 "*Fabrication of ZnO TFTs on Plastic Substrates*" consists of device fabrication procedures for polymer substrates and presents the results obtained with regard to the ZnO TFTs developed in this work.

Chapter 5 "*Conclusions and Recommendations for Future Work*" consists of a summary of the conclusions drawn from the experiments performed in this thesis and recommendations for future work on ZnO-TFTs fabricated on both glass and plastic substrates.

Fig. 1.1 (a)

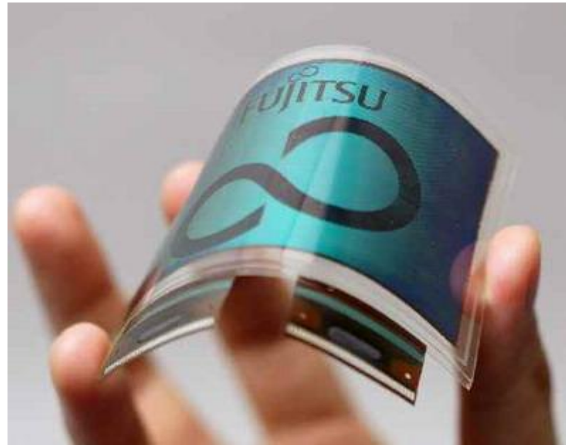

Fig. 1.1 (b)

Fig. 1.1 (c)

Fig. 1.1 (d)

Figure 1.1 (a) ~ (d) The display application of flexible electronics. (a) Fujitsu e-paper. (b) An e-paper newspaper. (c) E-papers look like real sheets of paper. (d) A foldable display.

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[1] P. K. Weimer. “The TFT – A new thin film transistor”, Proceeding of the IEEE, 1962.

[2] H. Kawamoto, “The history of liquid-crystal displays”, Proceeding of the IEEE, 2002.

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Chapter 2

Literature Review and Theory

2.1 Transistors

2.1.1 Working principles of field-effect transistors

The field-effect transistor (FET) is a type of transistors and depends on an electric field to control the shape and hence the conductivity of a channel in a semiconductor material. An FET with electrons flowing in the channel in semiconductor is so called an "n-channel" FET and likewise a 'p-channel' FET with holes flowing in the channel. Fig. 2.1(a) and (b) demonstrates the two kinds of FETs, i.e. n-channel FET and the p-channel FET respectively. The FET controls the flow of carriers by affecting the size and shape of a conductive channel created and influenced by voltage applied across the gate and source terminals.

FETs can also be categorized by the structure. Three mostly known may be "junction field-effect transistor" (JFET), "thin film transistor" (TFT) and "metal-oxide-semiconductor field-effect transistor" (MOSFET). MOSFET is theoretically stated as follows to form a basic concept of operation principles of FETs.

An n-channel MOSFET (NMOS) along with the device structure is shown in Fig. 2.2.

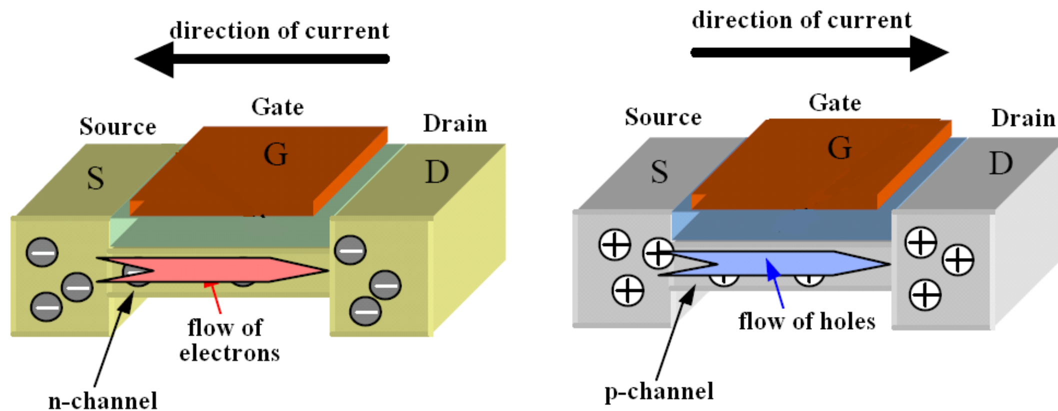


Figure 2.1 FETs: (a) n-channel FET; (b) p-channel FET.

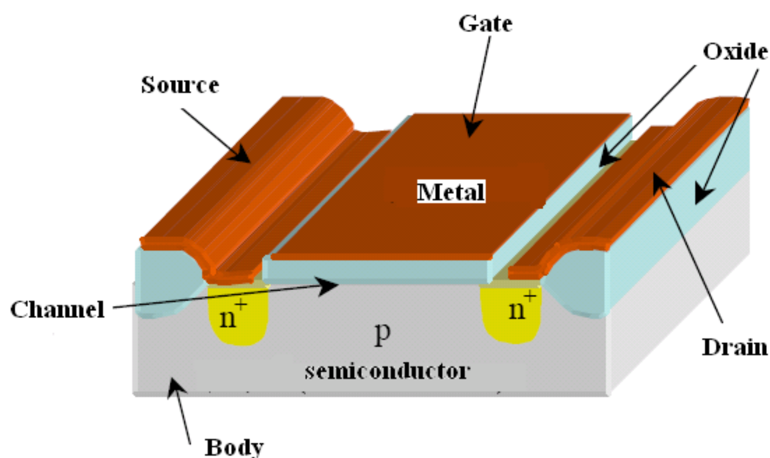
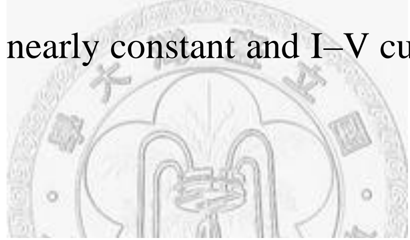
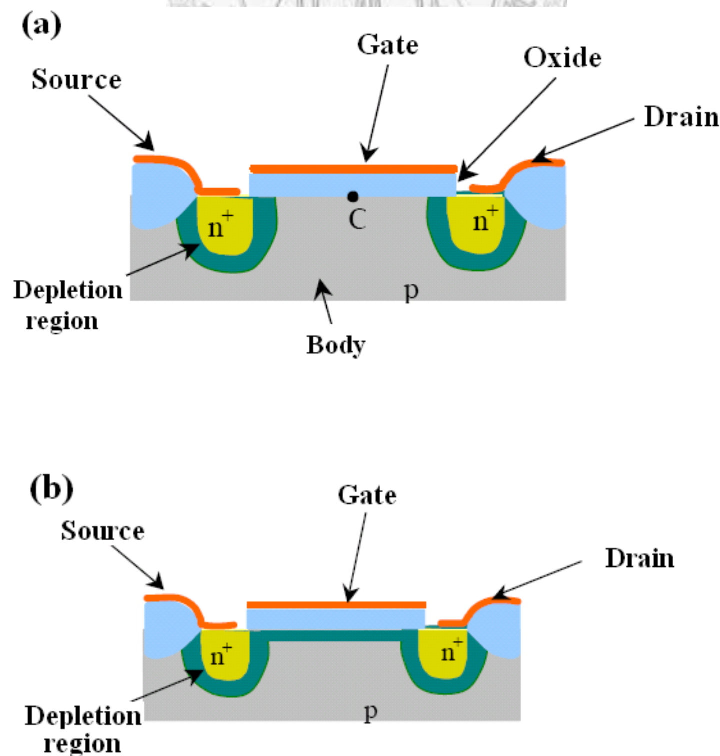


Figure 2.2 Structure of NMOS.

In the first instance, consider the case the voltage between source and drain (V_{DS}) is quite small compared to the voltage between source and gate (V_{GS}). When gate is at zero bias (relative to source), the n^+-p-n^+ structure can be seen as a reverse cascade of two *pn* junction diodes and no current flows through the path; NMOS is cut-off, as illustrated in Fig. 2.3 (a). As applying a small positive voltage to gate, the majority carriers (holes) in *p*-type semiconductor will be repelled and then the depletion region forms in the surface of *p*-type semiconductor, as illustrated in Fig. 2.3(b). Once

gate voltage achieves the threshold voltage (V_{th}), the inversion layer (channel) exactly appears in the surface of *p*-type semiconductor and the minority carriers (electrons) start to accumulate in the channel, as illustrated in Fig. 2.3(c). With increasing gate voltage, the number of accumulating electrons increases while the depletion region almost remains constant, as illustrated in Fig. 2.3(d). Fig. 2.4 shows the output characteristics (I_D–V_{DS} curves at different gate bias) mentioned above. The uniform distribution (since $V_{GS} \approx V_{DS}$) of electrons results in the same effective channel thickness (t) everywhere so the resistance described by $R_{DS}=\rho L/Wt$ (ρ for resistivity of p-type semiconductor, L for channel length, W for channel width) is nearly constant and I–V curves looks almost linear or ohmic.





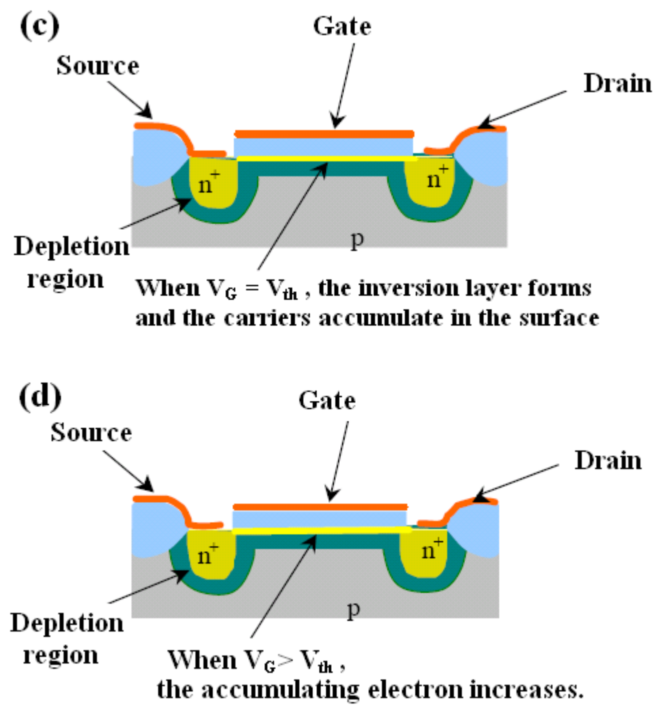


Figure 2.3 The depletion region and the channel at different gate bias. (a) V_G=0, (b) V_G<V_{th}, (c) V_G= V_{th}, (d) V_G>V_{th}.

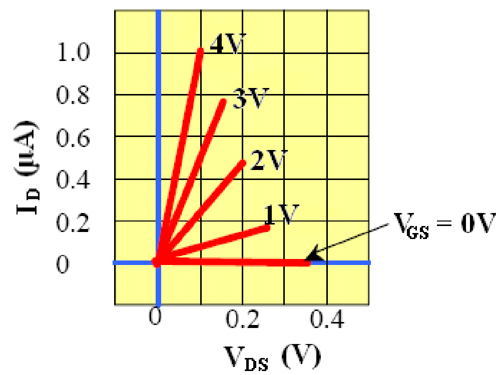


Figure 2.4 Output characteristics when V_{DS} is quite small.

What if V_{DS} increases? If V_{DS} increases, V_{GD} becomes smaller than V_{GS} and thus the channel thickness begins to be asymmetric. From Fig. 2.5 (a), it is obviously seen that the channel thickness beside drain is

thinner than that beside source. Because of the reduction of the average channel length, the resistance rises and hence the I–V curve starts bending downwards. When V_{DS} achieves V_{Dsat} (onset of saturation), the inversion layer beside drain disappears and the channel beside drain is exactly pinched off, as illustrated in Fig. 2.5(b). Beyond V_{Dsat}, the pinched-off length of the channel slightly increases ($\Delta L << L$) and depletion region between drain and channel comes into being, as illustrated in Fig. 2.5 (c).

To furthermore explain the saturated behavior beyond V_{Dsat}, point *X* is defined as the place where the inversion layer exactly disappears when $V_{DS} > V_{Dsat}$, as seen in Fig. 2.5 (c). By definition, V_{GX} is always equal to V_{th} and is independent of V_{DS}. Therefore, V_{XS} is also independent of V_{DS}. In addition, the effective channel length and the carrier (electrons) concentration both are less affected by V_{DS} since $\Delta L << L$. As a result, I_D remains constant when $V_{DS} > V_{Dsat}$.

The typical output characteristics of NMOS are shown in Fig. 2.6 with three marked points (a), (b), and (c) corresponding to Fig 2.5 (a), Fig 2.5 (b) and Fig 2.5 (c), respectively.

Since the channel of NMOS is enhanced to be active by applied gate voltage, such NMOS is an enhancement-mode FET. On the contrary, the channel of depletion-mode FETs is depleted to be inactive by applied gate voltage.

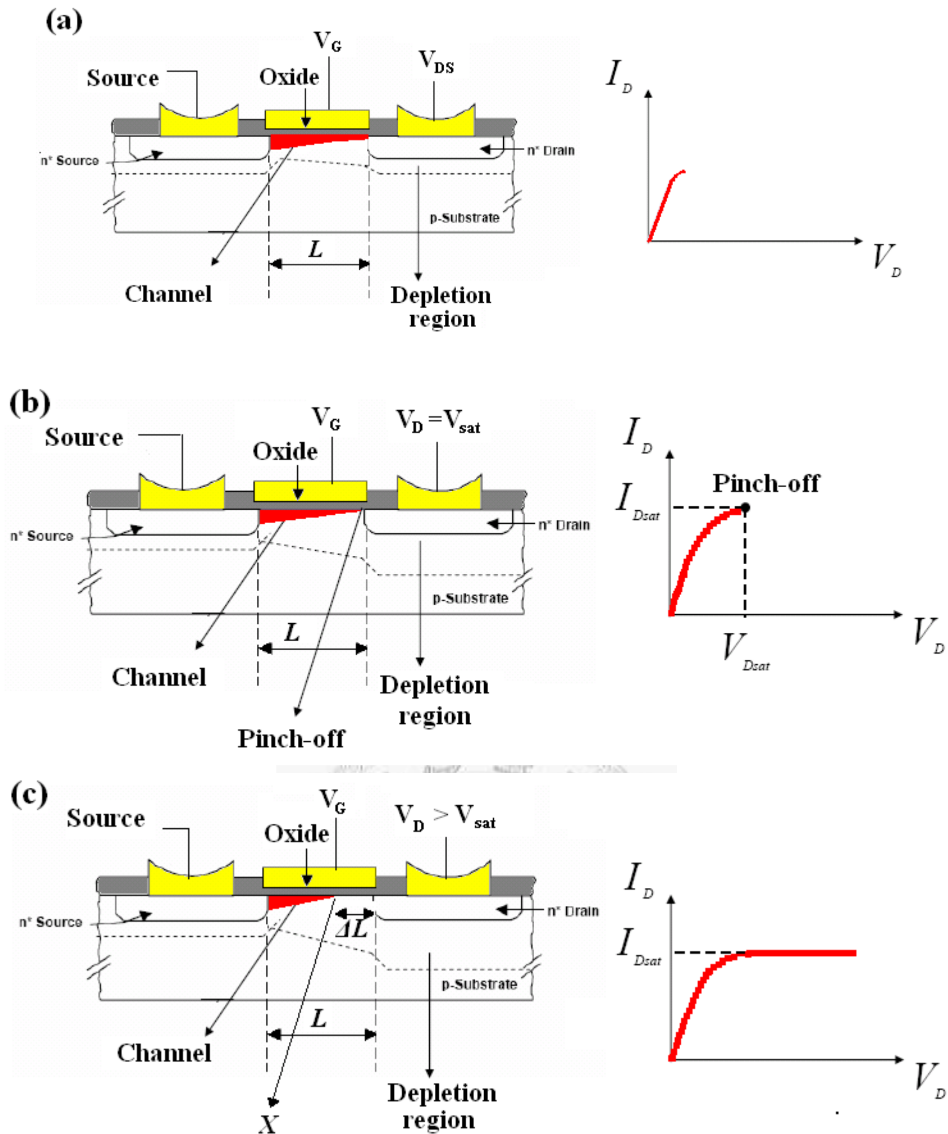


Figure 2.5 Variation of channel and depletion region at a constant V_G when (a) $V_{DS} < V_{Dsat}$; (b) $V_{DS} = V_{Dsat}$; (c) $V_{DS} > V_{Dsat}$.

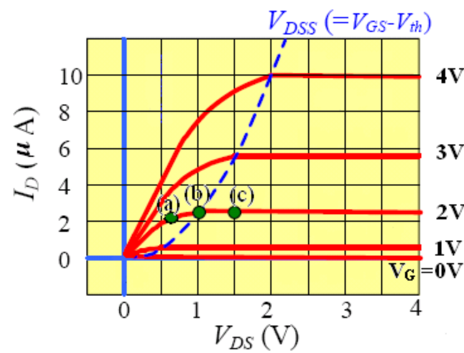


Figure 2.6 Output characteristics.

The current-voltage relationship can be expressed as follows [1]. In the non-saturation region, we will obtain

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}[2(V_{GS} - V_{th})V_{DS} - V_{DS}^2] \quad \dots\dots\dots\dots 2\text{-}1$$

and, in the saturation region, we will have

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{th})^2 \dots\dots\dots\dots\dots\dots\dots 2\text{-}2$$

where μ_n is the mobility of the electrons in the inversion layer

and,

$$C_{OX} = \frac{\epsilon_{OX}}{t_{OX}} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots 2\text{-}3$$

where ϵ_{OX} is the permittivity of the oxide and t_{OX} is the thickness of the oxide.

2.1.2 Operation of thin film transistors

The operation of TFT and MOSFET is similar in that the current from the source to the drain is modulated by the applied gate electric field. Current modulation in a TFT or a MOSFET can be explained if the metal-oxide-semiconductor (MOS) part of the TFT is considered as a capacitor [2].

Fig. 2.7 shows the cross-section and energy band diagrams of a MOS capacitor with an n-type semiconductor. Fig. 2.7 (b) shows the equilibrium state, without gate bias applied, for an ideal case in which no charge is present in the insulator or at the insulator/semiconductor interface so that the energy bands are flat.

A positive voltage applied to the gate electrode, as shown in Fig. 2.7 (c), causes the energy bands to bend downwards, hence increasing the electron concentration at the insulator-semiconductor interface. The interface is therefore more conductive than the bulk of the semiconductor. This mode of operation in which majority carriers, electrons in this case, accumulate at the insulator-semiconductor interface and give rise to the channel current is denoted as the accumulation-mode operation. When a small to moderate negative voltage is applied to the gate electrode, majority carrier electrons are repelled from the insulator-semiconductor interface so that a depletion layer is formed. When a larger negative voltage is applied the gate, as shown in Fig. 2.7 (d), the depletion layer reaches a maximum thickness after which minority carriers, holes in this case, form a conductive channel at the insulator-semiconductor interface. This conductive channel gives rise to what is denoted inversion-mode operation,

since the conductivity type is inverted with respect to the semiconductor bulk. MOSFETs usually operate in inversion-mode whereas TFTs operate in accumulation-mode.

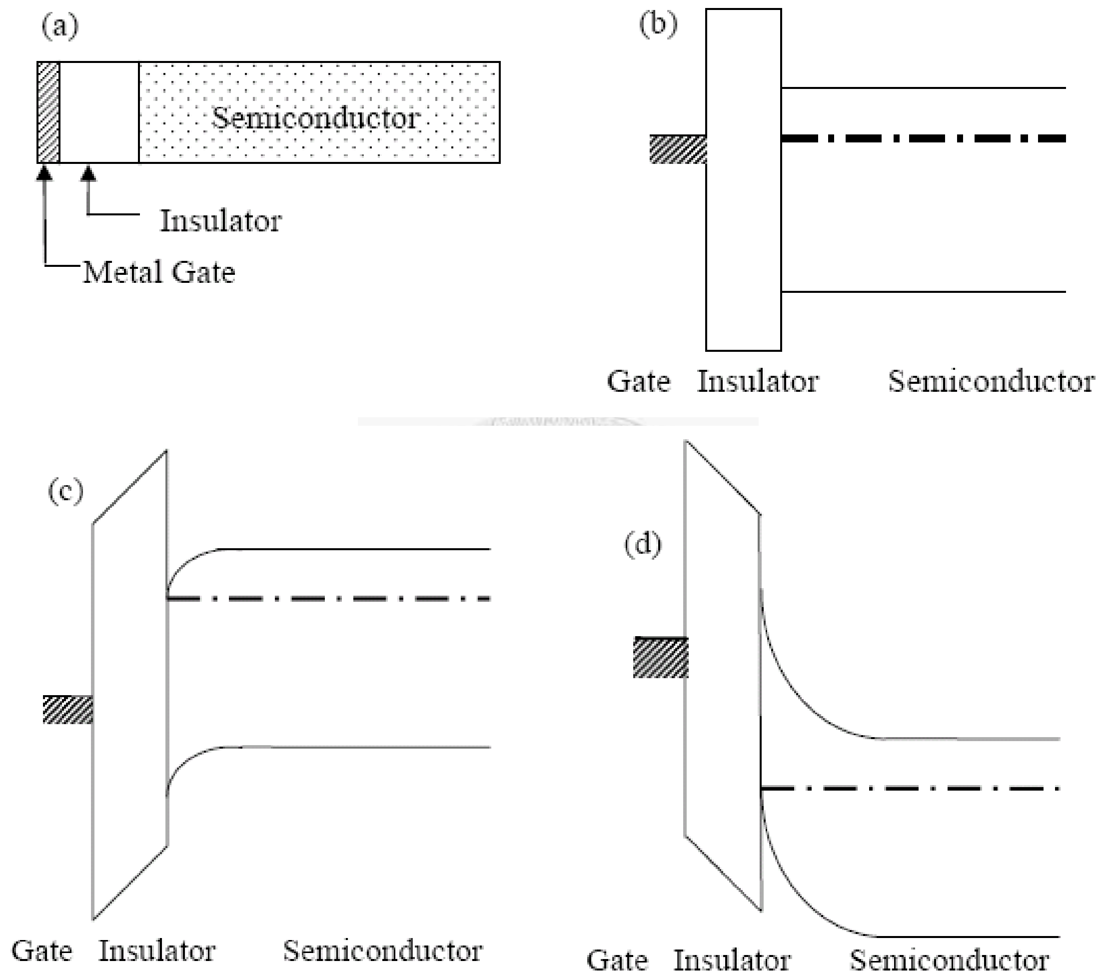


Figure 2.7 (a) The cross-section of a MOS capacitor and corresponding energy band diagrams for several biasing conditions: (b) equilibrium, (c) accumulation ($V_{GS} > 0$ V), and (d) inversion ($V_{GS} < 0$ V).

Figure 2.8 shows a three terminal n-channel TFT for accumulation-mode operation. A positive voltage is applied to the gate electrode to attract electrons to the insulator-semiconductor interface and

forms an accumulation layer. The drain electrode is biased positively with respect to the source to attract electrons from the accumulation channel. At zero or small positive voltages applied to the drain electrode, the accumulation layer formed, as shown in Fig. 2.8 (a), is uniform from the source end to the drain end of the channel. At a small drain voltage, the TFT operates as resistor where the drain current (I_D) increases linearly with increase in the drain voltage (V_{DS}). However, at slightly larger drain voltages, the linear dependence of I_D on V_{DS} changes to a quadratic dependence on V_{DS}. This entire regime of TFT operation, where I_D increases with increasing V_{DS}, is called triode or pre-pinch-off. As V_{DS} is further increased, the effective voltage between the gate and drain (V_{GD}) decreases, which decreases the electron concentration at the drain end of the accumulation layer. The drain voltage, at which the accumulation channel is fully depleted of electrons, is called the pinch-off voltage and is denoted as V_{Dsat}. When $V_{DS} \geq V_{Dsat}$, drain voltage has no effect on I_D so that the drain current saturates. This is referred to as the post-pinch-off regime, and is shown in Fig. 2.8 (b).

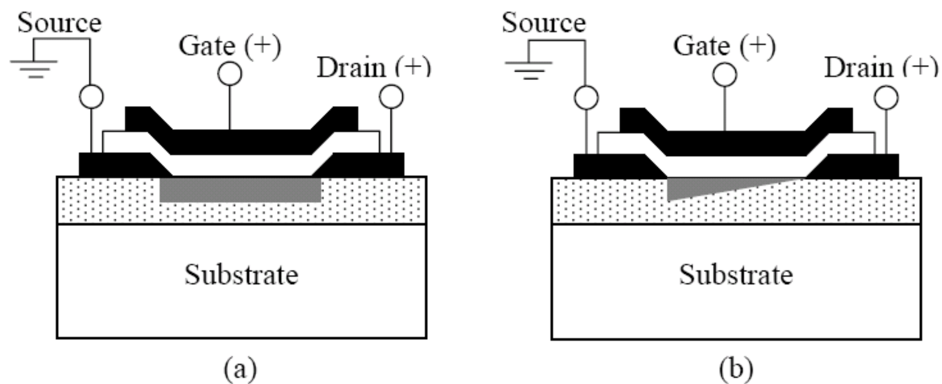


Figure 2.8 An n-channel accumulation-mode TFT operating in (a) pre-pinch-off and (b) post-pinch-off regime.

Depending on the gate voltage required to form an accumulation layer, a TFT can be classified as either an enhancement-mode or a depletion-mode device. In enhancement-mode operation of an n-channel TFT, a positive voltage must be applied to the gate electrode to create an accumulation layer at the insulator-semiconductor interface. For depletion-mode operation, the accumulation layer is already present at zero gate voltage. Thus, for an n-channel TFT, a negative gate voltage has to be applied to deplete the accumulation channel and turn the device off. Therefore, an enhancement-mode device is a "normally-off" device, whereas a depletion-mode device is "normally on". In an ideal TFT model in which traps are neglected, the TFT would be a depletion-mode device because of the presence of zero-bias carriers (bulk carriers) available for current conduction. However, the presence of empty traps, which must be filled with carriers prior to the formation of the accumulation layer, gives rise to enhancement-mode operation of the TFT [3].

2.1.3 Si-based thin film transistors

The structure of conventional a-Si TFTs for commercial TFT-LCDs is illustrated as Fig. 2.9. Typically, there are five to seven steps to make commercial a-Si TFTs and the flow of the fabrication process is also outlined in the inset of Fig. 2.9 [4].

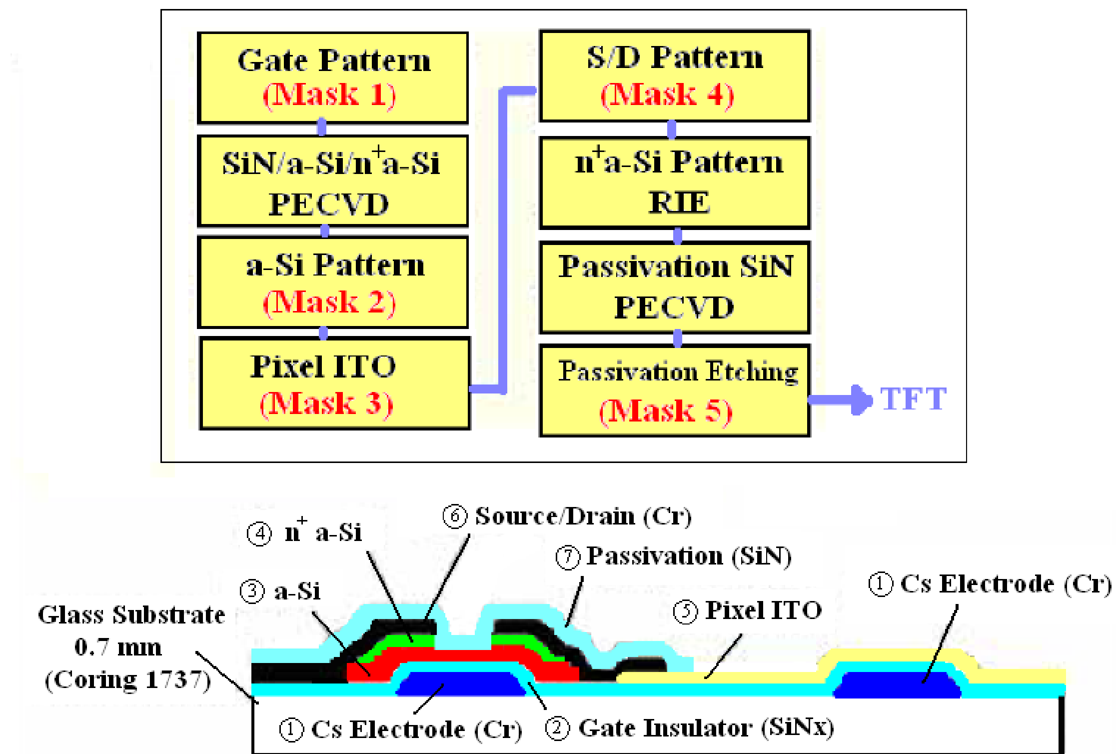


Figure 2.9 Structure of an a-Si TFT and in the inset, the flowchart outlines the processes for making an a-Si TFT array using a bottom-gate TFT structure and an independent storage capacitor.

Obviously, there are significant differences between the structure of a MOSFET and a TFT. Fig. 2.10 shows typical cross-sectional views of a MOSFET and a TFT.

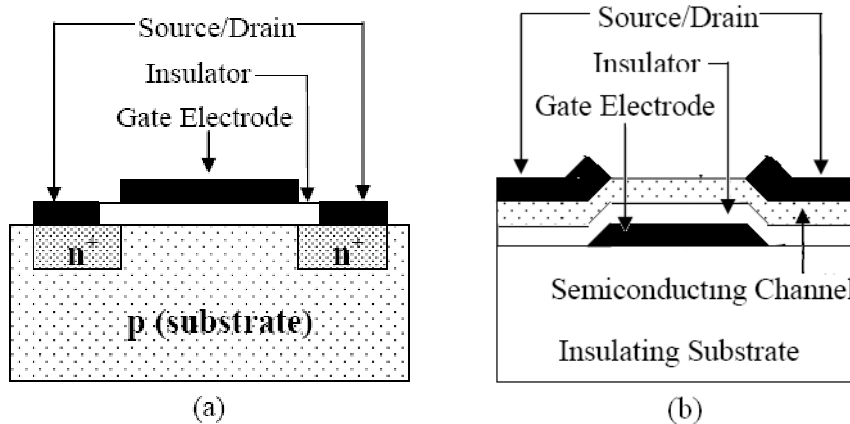


Figure 2.10 Cross-sectional view of a (a) MOSFET and (b) TFT.

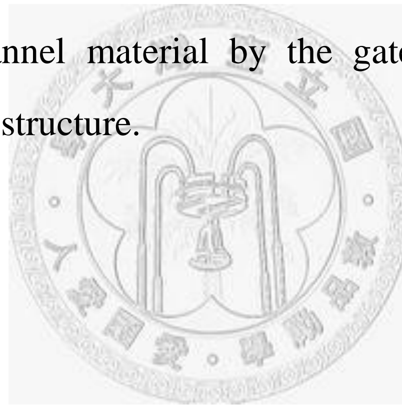
As evident from Fig. 2.10, the substrate of a TFT is an insulating material, while the substrate of a MOSFET is a semiconductor material (p-type) of opposite polarity as the source and drain diffusions (n-type). Source and drain contacts to the semiconducting channel material are injecting contacts to the channel in a TFT structure, instead of ohmic contacts to a pn junction as in a MOSFET.

Four TFT device structures are possible, as indicated in Fig. 2.11, and are categorized as staggered or coplanar. In a staggered configuration, as shown in Figs. 2.11 (a) and 2.11 (c), the source/drain contacts are on opposite sides of the channel from the insulator, whereas in a coplanar configuration, as shown in Figs. 2.11 (b) and 2.11 (d), the source/drain contacts and the insulator are on the same side of the channel. Both the staggered and the coplanar configurations can further be classified as bottom-gate and top-gate structures. A bottom-gate TFT, also referred to an inverted TFT, has the gate insulator and gate electrode located beneath the channel, as shown in Figs. 2.11 (a) and 2.11 (b). In a top-gate device,

as shown in Figs. 2.11 (c) and 2.11 (d), the channel is covered by a gate insulator and gate electrode.

The coplanar structure is popular in polycrystalline silicon TFTs, whereas staggered structures are commonly used in amorphous silicon TFTs. The inverted, staggered structure is the most popular amorphous silicon TFT structure, because it gives the best transistor characteristics and offers significant process latitude [5].

Top-gate TFTs are usually fabricated with an aluminum gate since gate deposition is one of the last deposition steps in the fabrication process of this type of TFT, after which no high temperature processing is required. Passivation of the channel material by the gate insulator is an added advantage of a top-gate structure.



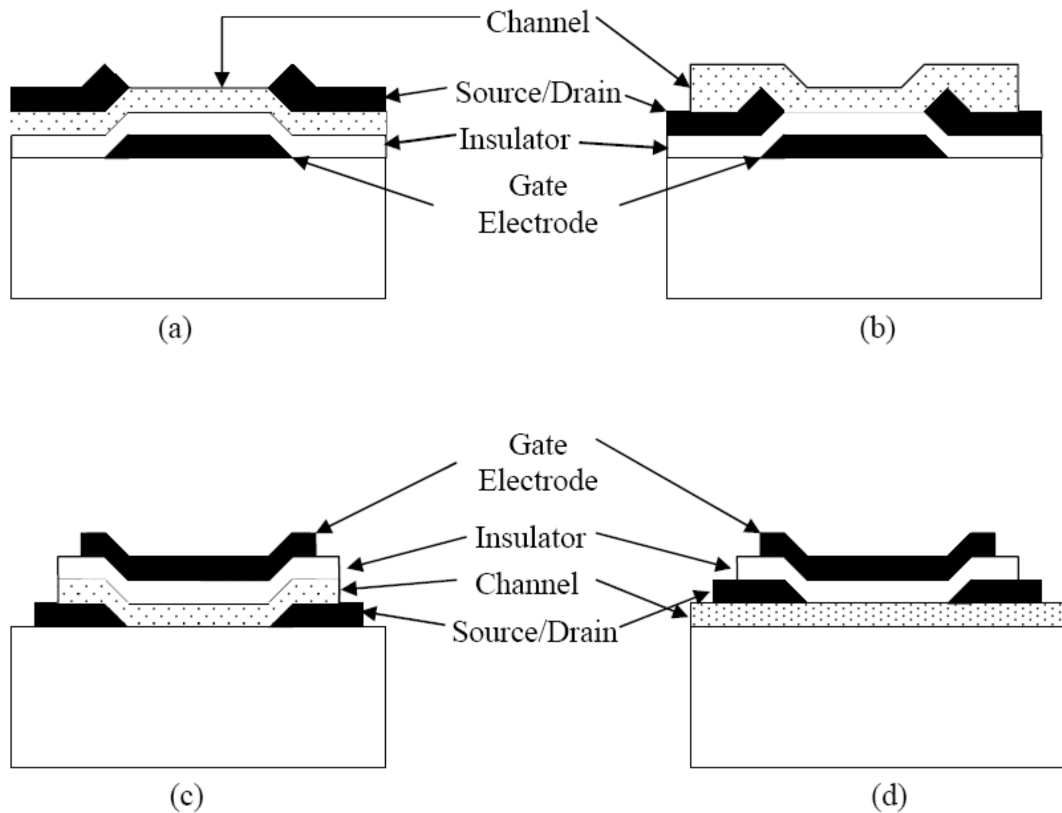


Figure 2.11 Four thin-film transistor configurations: (a) staggered bottom-gate, (b) coplanar bottom-gate, (c) staggered top-gate, and (d) coplanar top-gate.

As for the performance of a-Si TFTs reported so far, the field-effect mobility reaches from 0.1 to 2 cm^2/Vs and the threshold voltage ranges from 2 to 10 V [6-9]. For polysilicon TFTs, the reported mobility can achieve as high as 50 cm^2V/s and its threshold voltage is about 1V [10]. However, the fabrication temperature and the opacity of Si-based TFTs limit the possibilities of applications for transparent and/or flexible electronics.

2.1.4 Oxide-semiconductor-based thin film transistors

The development of transparent and/or flexible electronics motivates the studies on oxide semiconductor materials such as ZnO [11], SnO_2 [12], IGZO (indium gallium zinc oxide) [13], and IZO (indium zinc oxide) [14]. Despite the amorphous structure of these materials, they attract attention mainly due to high electron mobility. Some examples already produce devices with field-effect mobilities reaching above 50 cm^2/Vs and on-off ratio of 10^{-6} to10^{-7} [11-14].

Table 2.1 summarizes the work regarding wideband gap semiconductors for use as TFTs [12], for this work is directly relevant to the research reported in this thesis.

The use of ZnO channel in the field effect transistor as one of the *majority* carrier devices has been demonstrated in 1968 with using a bulk single crystal [15]. Notably, it's the *majority* carrier that transports in the channel and no inversion layer is induced by applied gate voltage in the cases of ZnO-based TFTs.

Table 2.1 Wide band gap-based TFTs, processing methods employed, and electrical performance characteristics for several different channel materials. The maximum processing temperature, deposition method, mobility, drain current on-to-off ratio, and threshold voltage are included.

Channel Material	Max. Proc. Temp. (℃)	Dep. Method	Mobility (cm^2/Vs)	On-Off Ratio	Threshold Voltage (V)	Ref.
ZnO	Room Temp	RFS[a]	2	10^6	0	[16]
ZnO	300	PLD[b]	7	10^7	0	[17]
ZnO	450	PLD	0.97	10^5	-1	[18]
ZnO	700	IBS[c]	2.5	10^7	10-20	[19]
ZnO	700	SC[d]	0.2	10^7	10-20	[20]
(Zn,Mg)O	600	PLD	5.32	10^3	3	[21]
SnO_2		PLD	5	2	-2	[22]
IZO	600	RFS	45-55	10^6	-20 ~ -10	[14]
ZTO	600	RFS	20-50	10^7	-5 ~ +5	[23]
IGZO	Room Temp	PLD	5.6	10^3	1.6	[13]

[a] radio frequency sputtering

[b] pulsed layer deposition

[c] ion beam sputtering

[d] spin coating

2.1.5 Flexible thin film transistors

There are three main choices for flexible substrates, which include polymeric, thin glass and steel foil. As far as roll-up, lightweight, impact resistance, and cost are concerned, polymeric substrates are the first choice. A number of issues are discussed for TFTs on polymeric substrates. Process temperature limitations as a function of polymer type is one of the biggest challenges since polymers undergoing deformation at high temperature conditions invalid the TFTs. The detailed properties of some polymeric substrates are expounded in section 2.3.2.

The popular materials nowadays for channel layer are *a*-Si, pentacene (organic), and oxide semiconductor such as ZnO. *a*-Si deposited at limited low temperature achieves poor crystallization and hence quite low mobility, usually less than 2 cm^2/Vs. Post-approaches like thermal annealing are needed to improve the electrical performance of *a*-Si TFTs on plastic. As for organic materials, the low mobility and poor reliability restrain its development while organic TFTs (OTFTs) need lower process temperature.

Amorphous and polycrystalline ZnO can be obtained by sputtering at room temperature with high mobility. In addition, the carrier concentration can be engineered by controlling the dopants or the O_2 presence. Fig. 2.12 shows the material properties of indium-gallium-zinc oxide (IGZO) system [26].

Table 2.2 summarizes the representative work of flexible TFTs on plastic to date, kinds of popular materials and common substrates included.

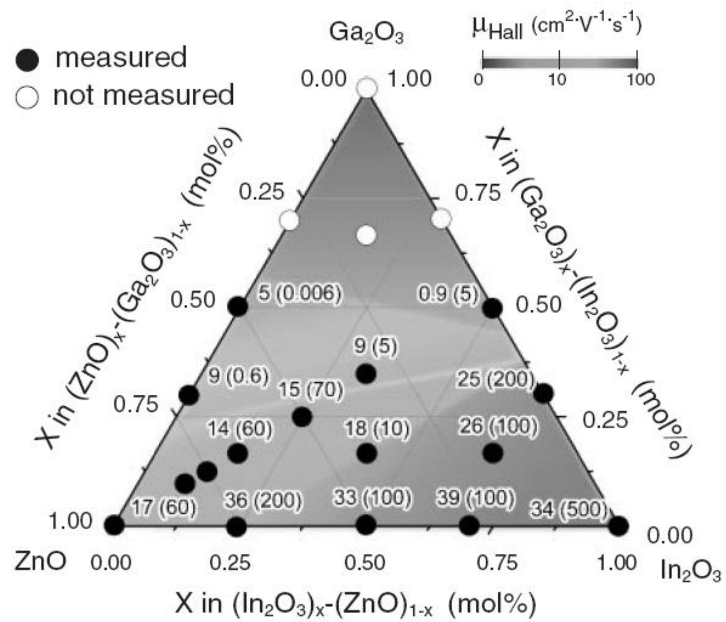


Figure 2.12 Material properties of IGZO system. Room temperature Hall mobility and carrier concentration as functions of chemical composition. Values outside and inside parentheses show Hall mobility in cm^2/Vs and carrier concentration in 10^{18} cm^{-3}, respectively.

Table 2.2 Flexible TFTs on plastic, substrate, processing methods employed, and electrical performance characteristics for several different channel materials. The maximum processing temperature, deposition method, mobility, drain current on-to-off ratio, and threshold voltage are included.

Channel Material	Substrate[i]	Max. Proc. Temp. (℃)	Dep. Method	Mobility (cm^2/Vs)	On-Off Ratio	Threshold Voltage (V)	Ref.
a-Si:H	PEN	120	PECVD[e]	0.8	10^6-10^7	4.5	[24]
a-Si:H		180	PECVD	0.8~1	10^6	3	[25]
a-IGZO	PET	Room Temp	PLD	10	10^6	1.3	[26]
ZnO	PI	Low Temp	RFS	50	10^5	3.2	[27]
ZTO	PI	300	RFS	14	10^6	-8.8	[28]
Pentacene	PEN		TE[g]	0.67	10^4	-0.88	[29]
CNT[h]		Room Temp	IP[f]	47,662	1.08	-2.5	[30]

[e] plasma-enhanced chemical deposition

[f] inject printing

[g] thermal evaporation

[h] carbon nanotube

[i] also see section 2.3.2

2.2 Property of Materials

2.2.1 Zinc Oxide (ZnO)

ZnO material has drawn much attention recently for its good optical and electrical properties. With such potential advantages as wide bandgap (3.4eV), large exciton binding energy (60meV), high Hall mobility and so on, ZnO is widely studied in various fields such as thin film transistors, transparent conducting electrodes, varistors, ultraviolet emitting diodes, etc. Besides, ZnO even becomes a popular material for commercial cosmetic products and sunglasses because of its capability of absorption of ultraviolet light.

The property of ZnO is listed in Table 2.3 [31]. Because the bandgap of ZnO is 3.4eV, ZnO is transparent in the visible light. Transparent oxide semiconductor materials make possible replacement of opaque Si as channel layer of TFTs and improvement of aperture ratio of TFT-LCD. ZnO is a promising candidate among these oxide semiconductors. Furthermore, polycrystalline ZnO thin film can be achieved at lower growth temperature by methods of sputtering, pulsed laser deposition, chemical vapor deposition, molecular beam epitaxy, and inkjet printing, etc. Better crystallization means higher mobility and hence higher operating current. In these respects, ZnO is more attractive and feasible than organic- or Si-based TFTs when cheap and/or transparent substrates made of glass or polymer are chosen.

ZnO crystallizes with the wurtzite structure is shown in Fig. 2.13.

Table 2.3 Properties of ZnO

Property	Value
Crystalline	Hexagonal
Lattice parameter at 300K:	
a	3.252 Å
c	5.313 Å
c/a	1.602 Å (1.633 for ideal hexagonal structure)
Density	5.606 g/cm^3
Stable phase at 300K	Wurtzite
Melting point	1975℃
Thermal conductivity	0.6, 1–1.2
Linear expansion coefficient (/℃)	*a*: 6.5×10^{-6}
	c: 3.0×10^{-6}
Static dielectric constant	8.656
Refractive index	2.008, 2.029
Energy gap	3.4eV, direct
Intrinsic carrier concentration	$< 10^6$ cm^{-3}
Exciton binding energy	60 meV
Electron effective mass	0.24
Electron Hall mobility at 300K for low n-type conductivity	200 cm^2/Vs
Hole effective mass	0.59
Hole Hall mobility at 300K for low p-type conductivity	5–50 cm^2/Vs

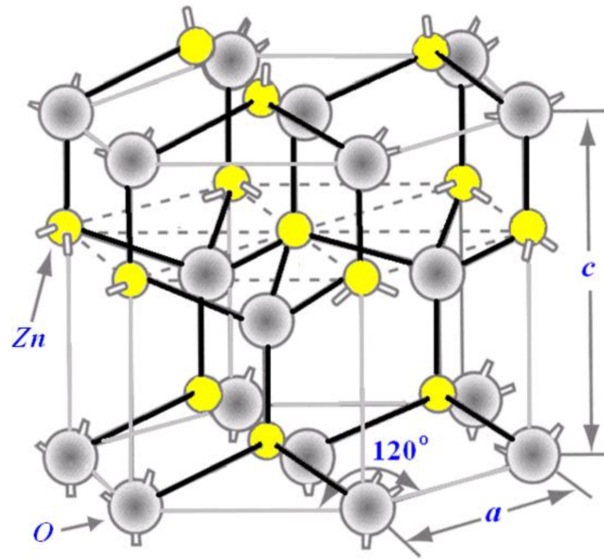


Figure 2.13 Crystal structure of wurtzite ZnO.

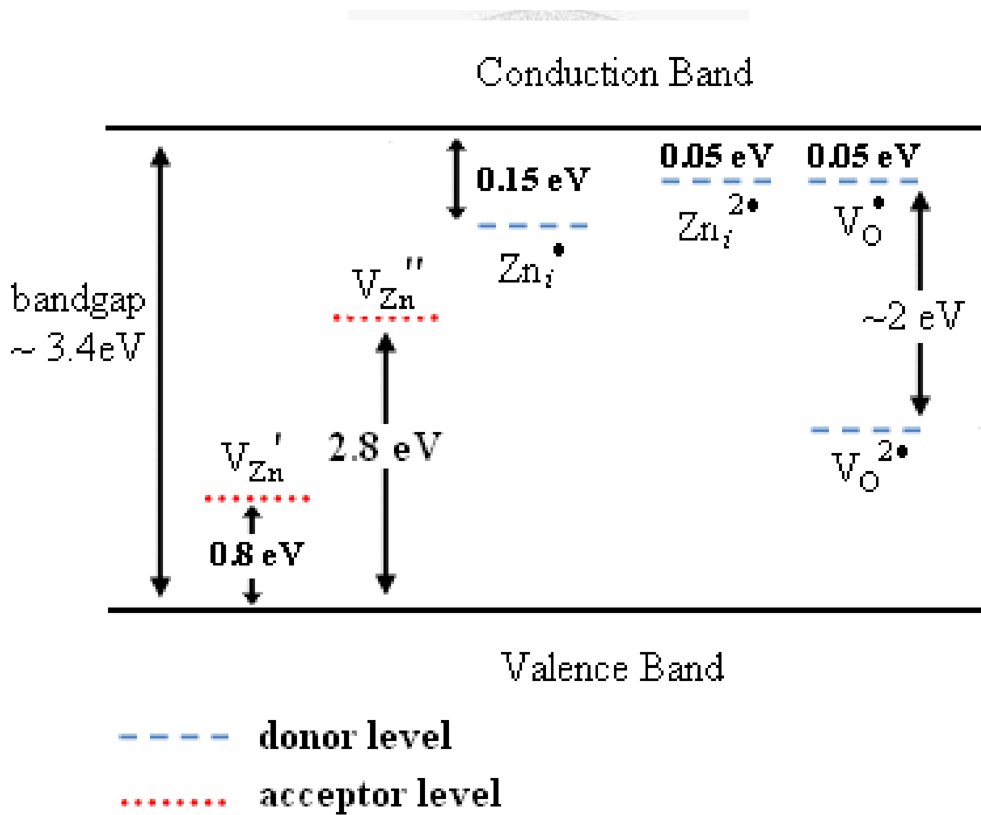


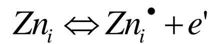
Figure 2.14 Energy levels of native defects in ZnO. The donor defects are $Zn_i^{2\bullet}$, $Zn_i^{\bullet}$, Zn_i, $V_O^{2\bullet}$, $V_O^{\bullet}$, V_O and the acceptor defects are V_{Zn}'', V_{Zn}'.

For n-type ZnO, it's considered that zinc interstitials (Zn_i) and oxygen vacancies (V_O) act as donors and may account for the n-channel behavior [27]. The model that Zn_i and V_O are indentified as dominant donors in ZnO however is challenged by some novel theory and experiment [32], but others find the amount of O_2 when depositing ZnO film does affect the conductivity and carrier concentration of ZnO. The reaction of defects in ZnO is listed in Table 2.4 and the related ionization energy is diagramed in Fig. 2.14 [33].

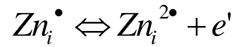
Table 2.4 (a) For crystal MX, the symbols are defined as:

M_M	M atom on M site
X_X	X atom on X site
M_i	M atom on interstitial site
X_i	X atom on interstitial site
N_M	Impurity N on M site
V_M	Vacancy on M site
V_X	Vacancy on X site
V_i	Vacant interstitial site
e'	Electron in conducting band
$h^{\cdot}$	Hole in valence band

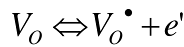
Table 2.4 (b) Reactions of defect ionization in ZnO



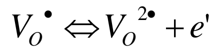
$$Zn_i \Leftrightarrow Zn_i^{\bullet} + e'$$



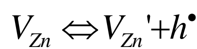
$$Zn_i^{\bullet} \Leftrightarrow Zn_i^{2\bullet} + e'$$



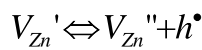
$$V_O \Leftrightarrow V_O^{\bullet} + e'$$



$$V_O^{\bullet} \Leftrightarrow V_O^{2\bullet} + e'$$



$$V_{Zn} \Leftrightarrow V_{Zn}' + h^{\bullet}$$



$$V_{Zn}' \Leftrightarrow V_{Zn}'' + h^{\bullet}$$

The two mechanisms for explaining the behavior of *n*-type ZnO are also stated in detail by *Richard A. Swalin* [34]. The symbols of the following equations have been defined in Table 2.4.

(a) Formation of anion vacancies with complete ionization of anion vacancy donors according to the following reaction:

$$\mathrm{O_O} = \frac{1}{2}\mathrm{O_2}(g) + \mathrm{V_O^{\bullet}} + e' \quad \text{.......................……2.4}$$

where $\mathrm{V_O^{\bullet}}$ is a singly ionized oxygen vacancy and e' is an electron in conducting band. (The symbol [•] indicates the “hole-character” of the defect). Oxygen vacancies form a shallow electron donor level close (~0.05 eV) to the conduction band and are readily ionized near room temperature, contributing free electrons. This reaction can undergo further ionization with liberation of another electron into the conduction band [27]; that is,

$$\mathrm{O_O} = \frac{1}{2}\mathrm{O_2}(g) + \mathrm{V_O^{2\bullet}} + 2e' \quad \text{.........................…2.5}$$

(b) Formation of ionized cation interstitials according to the following reaction:

$$\mathrm{Zn(g)} = \mathrm{Zn}_i^{\bullet} + e' \quad \text{......................................2.6}$$

Physically, this corresponds to transferring a neutral zinc atom from the vapor phase to an interstitial position. Interstitial cations tend to act as donors and, in this case, since the donor level (~0.05 eV) lies so close to the conduction band, the interstitials would be completely ionized. There could be a second ionization step according to:

$$\mathrm{Zn}_i^{\bullet} = \mathrm{Zn}_i^{2\bullet} + e' \quad \text{......................................2.7}$$

The equilibrium constants for the processes (a) and (b) are:

$$\mathrm{K_a} = \mathrm{p}_{O_2}^{\frac{1}{2}} \cdot [V_O^{\bullet}][e'] \quad \text{..2.8}$$

$$\mathrm{K_b} = \frac{[Zn_i^{\bullet}][e']}{\mathrm{p}_{Zn}} \quad \text{..2.9}$$

The quantities p_{O_2} and p_{Zn} are not independent of each other, since for the reaction for the formation of ZnO,

$$\mathrm{Zn(s)} + \frac{1}{2}\mathrm{O_2(g)} = \mathrm{ZnO(s)} \quad \text{.................................2.10}$$

there is an equilibrium constant

$$\mathrm{K} = \mathrm{p}_{Zn} \cdot \mathrm{p}_{O_2}^{\frac{1}{2}} \quad \text{......................................2.11}$$

yielding

$$\mathrm{KK_b} = [Zn_i^{\bullet}][e']\mathrm{p}_{O_2}^{\frac{1}{2}} \quad \text{..................................2.12}$$

If p_{O_2} decreases, $[e']$ increases and thereby so is the conductivity σ.

Further evidence concerning the nature of the defect structure comes from self-diffusion studies of Zn in ZnO. From these studies it is found that the diffusion coefficient is very high. The activation energy for the diffusion of Zn in ZnO is 0.55 eV, or 53KJ/g-atom. This value is too low for diffusion by a vacancy mechanism. The only way to explain this fast diffusion is to postulate the existence of interstitial Zn, therefore giving support to alternative (b) above. Since interstitial Zn ions are produced in concentration equal to the electron concentration,

$$[\mathrm{Zn}_i^{\bullet}] = [e'] \quad \text{..2.13}$$

thus, the conductivity

$$\sigma \propto [e'] \propto \mathrm{p}_{O_2}^{-1/4} \quad \text{..2.14}$$

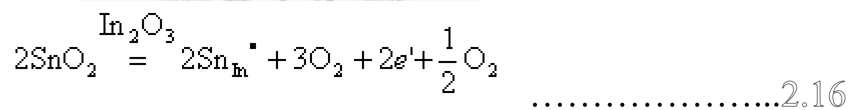
2.3.2 Indium Tin Oxide (ITO)

So far, the most widely used materials for transparent conducting oxides (TCO) are zinc oxide(ZnO), tin oxide(SnO_2), and indium oxide (INO). Compared to ZnO, SnO_2, and INO, tin-doped indium oxide (ITO) has lower electrical resistivity (about $10^{-4}\,\Omega$ cm) and higher optical transparency (above 85% at 550 nm) . As a result, ITO is more and more significant in the field of display devices, photovoltaic cells, and opto-electronic devices.

As an *n*-type degenerate semiconductor with wide bandgap (3.5 eV ~ 4.3 eV) and high work-function (4.5 eV ~ 5.3 eV), the mechanisms of conductive ITO can be attributed to tin dopants and oxygen vacancies. The two reactions are described as follows [35]:

$$O_O = \frac{1}{2}O_2(g) + V_O^{2\bullet} + 2e' \quad \text{2.15}$$

and



$$2SnO_2 \overset{In_2O_3}{=} 2Sn_{In}^{\bullet} + 3O_2 + 2e' + \frac{1}{2}O_2 \quad \text{2.16}$$

where $Sn_{In}^{\bullet}$ denotes the Sn^{+4} which replaces In^{+3} site in In_2O_3 crystal. The rest symbols in these expressions are same as what have been defined in section 2.2.1.

One oxygen vacancy donates two electrons as donors. In addition, since the atom size and mass of tin dopant close to what of indium, it's possible for Sn^{+4} to replace In^{+3} and then a free electron is formed as a donor. The cubic bixbyite structure of In_2O_3 crystal (of ITO crystal as well) is illustrated in Fig. 2.15.

The need for ITO thin film had led to the development of various deposition techniques. Both vacuum techniques, e.g. evaporation and sputtering, and non-vacuum techniques, e.g. sol-gel and ink-jet printing. Among numerous methods, magnetron sputtering can deposit films over large areas at higher deposition rate than conventional evaporation and it needs lower fabrication temperature than evaporation. Magnetron sputtering is rationally considered to be one of the best methods for preparing ITO films. High quality ITO films grown by magnetron sputtering have already been reported since 1990's [36].

The properties of sputtered ITO are proven to be quite sensitive to sputtering environment, such as substrate temperature [37], target-to-substrate distance [38], pressure of oxygen and/or hydrogen [39], RF power [40], and post-deposition annealing treatment [41].

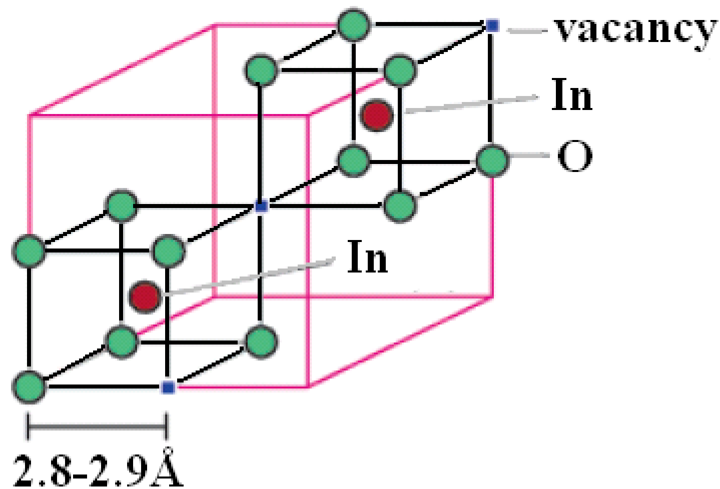


Figure 2.15 A simplified section of the unit cell of In_2O_3 (ITO, as well). The distance between the oxygen atoms varies between 2.8 and 2.9 Å

2.2.3 Insulating materials

The performance of a TFT is also related with the insulating layer, which can be explained from equation 2-1, 2-2 and 2-3. From equation 2-3, higher dielectric constant leads to larger capacitance and hence the TFTs can operate in ON and OFF states distinguishably; that is, high current for ON state and low current for OFF state. The dielectric constants of the most commonly used insulating materials are listed in Table 2.5. Those materials with dielectric constants higher than that of SiO_2 are termed "high-*k*" materials.

Table 2.5 Dielectric constants of various insulating materials. Permittivity of free space ε_0 is 8.85419×10^{-12} C^2/Jm

Material	Dielectric constant
SiO_2	3.9
Si_3N_4	7
Al_2O_3	9
Y_2O_3	15
La_2O_3	30
TiO_2	80
HfO_2	25
ZrO_2	25
Ta_2O_5	26

2.3 Property of Substrates

2.3.1 Glass substrate

The glass substrates for fabrication of TFTs have to satisfy the following demands.

(1) To be alkali-free to prevent alkali ions from diffusing into TFT arrays.

(2) High resistance to chemical solutions such as etchant, developer and cleanser.

(3) Low coefficient of thermal expansion (CTE).

(4) Good Flatness and Surface Quality

Table 2.6 [42] summarizes the characteristics of some glass substrates produced by the main producer in the global world.

Among these glass substrate, Corning 1737 and Corning 7359 are very popular for fabrication of TFTs in lab stage. Table 2.7 provides the property of Corning 1737 [43].

Table 2.6 Property of glass substrates produced by famous producer in the global world.

Producer	Products	Density (g/cm^3)	Strain Point (℃)	CTE (Multiply by 10^{-7}cm/cm/℃)
Corning	Eagle 2000	2.370	668	32.5
	1737	2.545	666	37.8
	7059	2.752	593	46.6
Asahi	AN-100	2.506	670	35.5
	AN-635	2.77	635	48
NEG	OA-2	--	--	--
	NA-10	2.511	651	36.6
NHT	NA-45	--	--	--
	NA-35	2.500	650	36.7
POI	POI	<2.500	645	32~37

Table 2.7 Property of Corning 1737.

Glass Code: Corning		1737
Type		Alkali Free Borosilicate
Color		Clear
Principal Use		Optics & electrical substrates
Thermal Expansion Multiply by 10^{-7}cm/cm/℃	0 - 300℃.	37.6
Viscosity Data	Strain point ℃.	**666**
	Annealing point ℃.	721
	Softening point ℃.	975
Density g/cm^3		2. 54
Log_{10} of Volume Resistivity ohm/cm.	250℃	13.5
Dielectric Properties (1 KHz 20℃)	Dielectric constant	5.7
	Loss factor %	.10
Refractive index @ 589 nm		1. 518
Transmittance (t=0.7mm)		~70% (320 nm) ~90% (360 nm) >90% (380-2600 nm)

2.3.2 Polymer substrates [44]

The plastic films that have been given serious consideration as flexible substrate for flexible electronics are show in Fig. 2.16, their abbreviations, glass transition temperature and crystallization included. The glass transition temperature limits the thermal budget of fabrication of electronic devices.

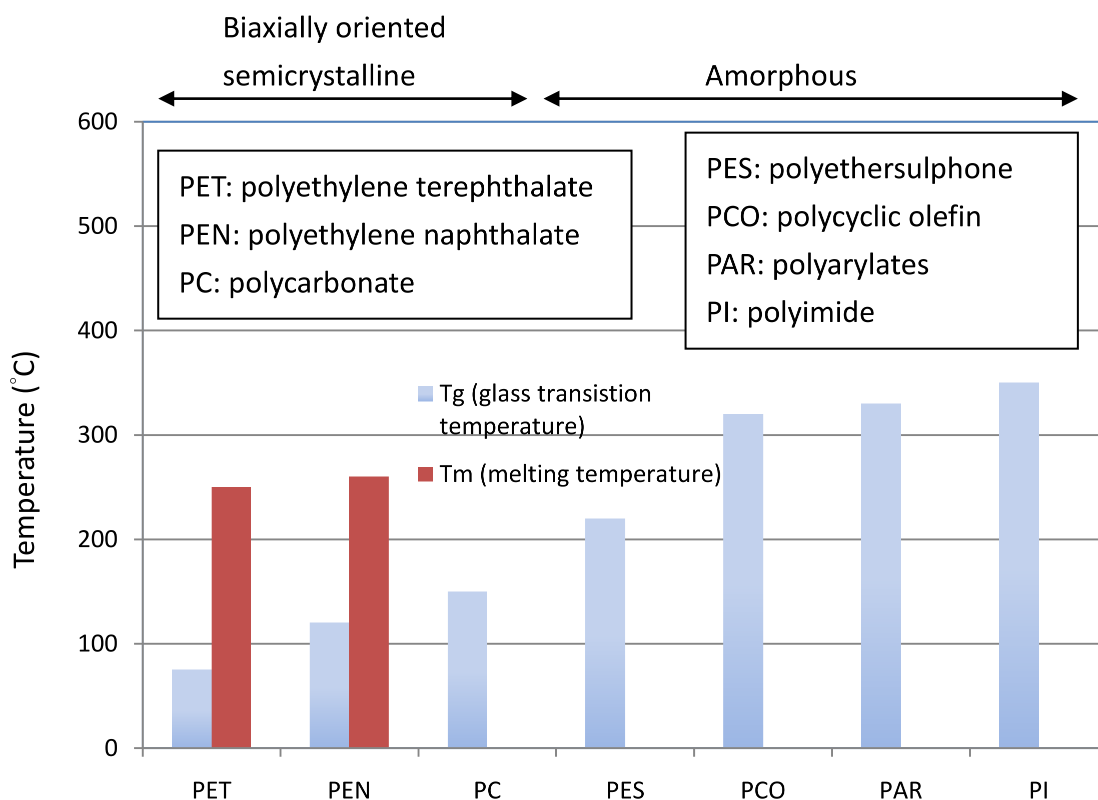


Figure 2.16 Comparison of a range of plastics by glass transition.

The clarity of the film is important for transparent electronics. A total light transmission (TLT) of >85% over 400–800 nm is typical of what is required for this application. All the base films described above meet this criterion, except for PI which is yellow; see table 2.8.

A wide range of solvents and chemicals can be used when fabricating

electronic devices on polymer substrates. Amorphous polymers in general have poor solvent resistance compared to semicrystalline polymers; see table 2.9. This deficiency is overcome by the application of a hardcoat layer (e.g. SiO_2, SiN_x etc.) double-side coated to the polymer films, which significantly improves the solvent and chemical resistance.

Table 2.8 Basic properties of plastic films used for base substrates. (Note: The information in this table is taken from different datasheets and should only be taken as illustrative.)

	PET	PEN	PC	PES	PAR	PCO	PI
CTE (-55 to 85 ℃) ppm/℃	15	13	60-70	54	53	74	17
Transmission at 400–700nm (%)	>85	>85	>90	90	90	91.6	yellow
Water absorption (%)	0.14	0.14	0.2-0.4	1.4	0.4	0.03	1.8
Young's modulus (GPa)	5.3	6.1	1.7	2.2	2.9	1.9	2.5
Tensile strength (MPa)	225	275	NA	83	100	50	231

Table 2.9 Solvent resistance of polymer substrates.

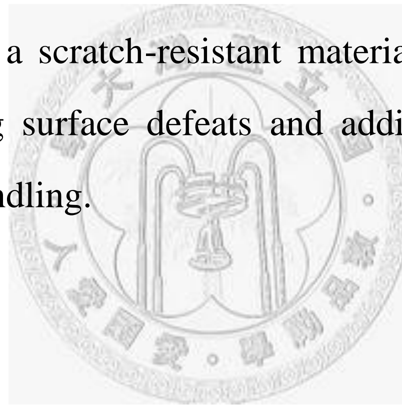
	Unit	PEN	PET	PC	PES
Ketone	Acetone	Good	Good	Fair	No good
	MEK	Good	Good	Fair	-
Alcohol	Methanol	Good	Good	Good	-
	Ethanol	Good	Good	Good	Good
	Isopropanol	Good	Good	Good	-
	Butanol	Good	Good	Good	-
Ester	Ethyl acetate	Good	Good	Fair	Good
Hydrocarbon	Formalin	Good	Good	No good	-
	Tetrachroloethane	Good	Good	-	Good
Acid	10% HCl	Good	Good	-	Good
	10% HNO_3	Good	Good	-	Good
	10% H_2SO_4	Good	Good	-	Good
	Acetic acid	Good	Good	-	-
Alkali	10% NaOH	Good	Fair	-	Good

Polymers absorb water and oxygen and the amount of water and oxygen they absorb can have a very detrimental effect on both substrate and electronic devices. In principle, a perfect layer of silica only a few nanometers thick should reduce the diffusion of water and oxygen to acceptable levels (just as the 2–3 nm native oxide layer on silicon wafers protects the wafer surface from further oxidation) although in practice thin film coatings can have defects that provide easy paths for water and oxygen molecules to penetrate. This particularly retards the progress of organic electronic devices in that they require water vapor transmission rate of $<10^{-6}$ g/m^2 per day and oxygen transmission rates of $<10^{-5}$ mL/m^2 per day and no base polymer at present meets these extremely demanding

requirements.

The surface smoothness and cleanliness of the flexible substrates are essential to ensure the integrity of subsequent layers such as barrier and conductive coatings. With PET and PEN films, improvements in surface quality can be achieved through control of recipe and film process. This is demonstrated in Fig. 2.17 [45], which highlights the substantial reduction of surface defect peaks with two different grades of PEN film.

The surface defects which remain in the Teonex Q65, in Fig. 2.17 (b), however, are still detrimental to the performance of thin overlying layers. To remove them entirely requires the application of a coating layer, typically comprised of a scratch-resistant material. This acts to smooth over all the underlying surface defeats and additionally help to prevent surface scratches on handling.



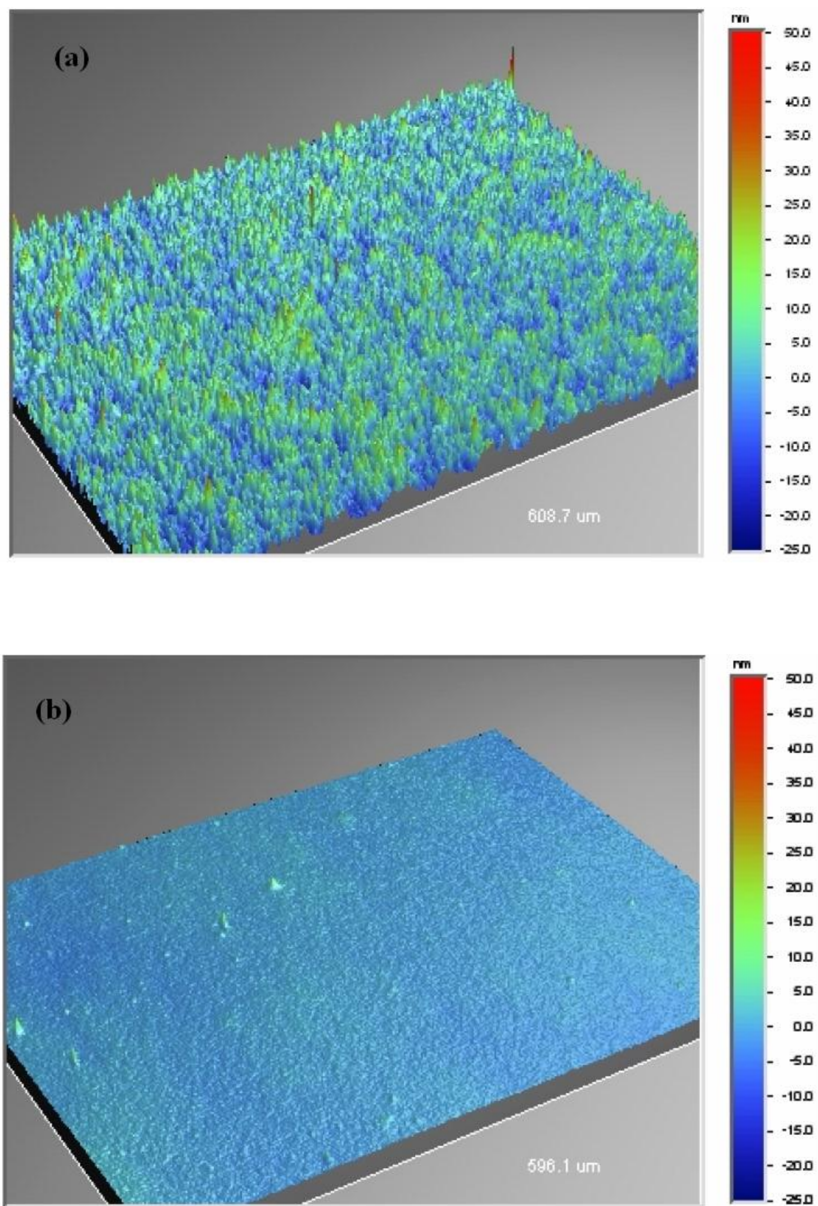


Figure 2.17 Surface roughness of (a) Teonex Q83 and (b) Teonex Q65, films produced by DuPont.

2.4 Plasma reaction and sputtering [46]

Plasma is typically a partially ionized gas and is considered to be a distinct state of matter, in contrast to gases because of its unique properties. The reactions to form plasma in a vacuum system include dissociation, excitation, ionization and glow discharge. For gas X_2, the reactions can be expressed as follows:

$$e^- + X_2 \rightarrow 2X + e^- \quad \text{(dissociation)} \ldots\ldots 2.17$$

$$e^- + X \rightarrow X^* + e^- \quad \text{(excitation)} \ldots\ldots 2.18.1$$

$$e^- + X_2 \rightarrow X_2^* + e^- \quad \text{(excitation)} \ldots\ldots 2.18.2$$

$$e^- + X_2 \rightarrow X_2^+ + 2e^- \quad \text{(ionization)} \ldots\ldots 2.19$$

$$e^- + X_2 \rightarrow X_2^+ + 2e^- \quad \text{(glow discharge)} \ldots\ldots 2.20$$

in which electrons emitted by two parallel electrode plates under DC or AC bias collide with the gas X_2 to form plasma.

Plasma generation requires electrons with high kinetic energy K:

$$K = F \cdot d = q \cdot E \cdot \lambda = q \cdot \frac{V}{d_e} \cdot \lambda \quad \ldots\ldots 2.21$$

where E is electric field, λ is mean free path, V is electrode voltage and de is electrode distance. Thus, plasma is generated in high voltage bias to increase V and in low pressure to increase λ. Take argon (Ar) for example; the process of plasma generation can be conceptually diagramed as in Fig. 2.18.

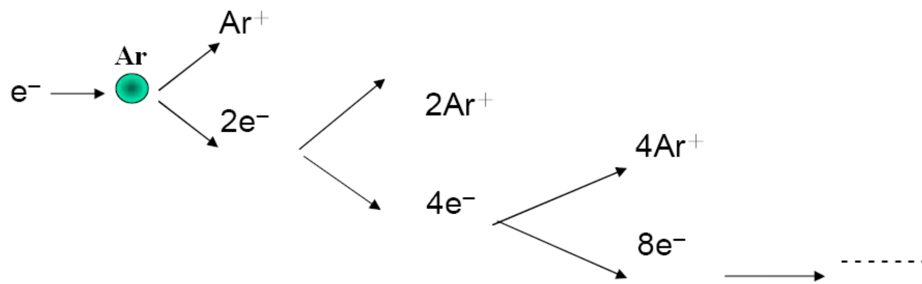


Figure 2.18 The process of Ar plasma generation.

Bombarded by accelerating ions with high energy in the plasma, the surface particles of target are then sputtered and deposit on the substrate. (Reference [47] detailed the mechanism of nucleation and growth of thin film.)

The two electrode plates of DC sputter have to be conductors or the charges will accumulate on the non-conductive plates and then the plasma reaction will stop. AC sputter can prevent charges from accumulating on the electrode plates by changing the electrode polarity periodically. Therefore, DC sputter is suitable for sputtering conductive material such as metal while AC sputter is suitable for both conductive and insulating material such as SiO_2. The lowest frequency for AC sputter must be higher than 100 Hz to maintain plasma reaction. The AC sputter system of which frequency is 13.56 MHz is called an RF (radio frequency) sputter. In RF case, the electrons obtain kinetic energy through oscillation in the field.

An RF magnetron sputter system applies a magnetic field so that electrons can accelerate electrons and increase collision of electrons with gases in a helix path between electrode plates, as illustrated in Fig. 2.19.

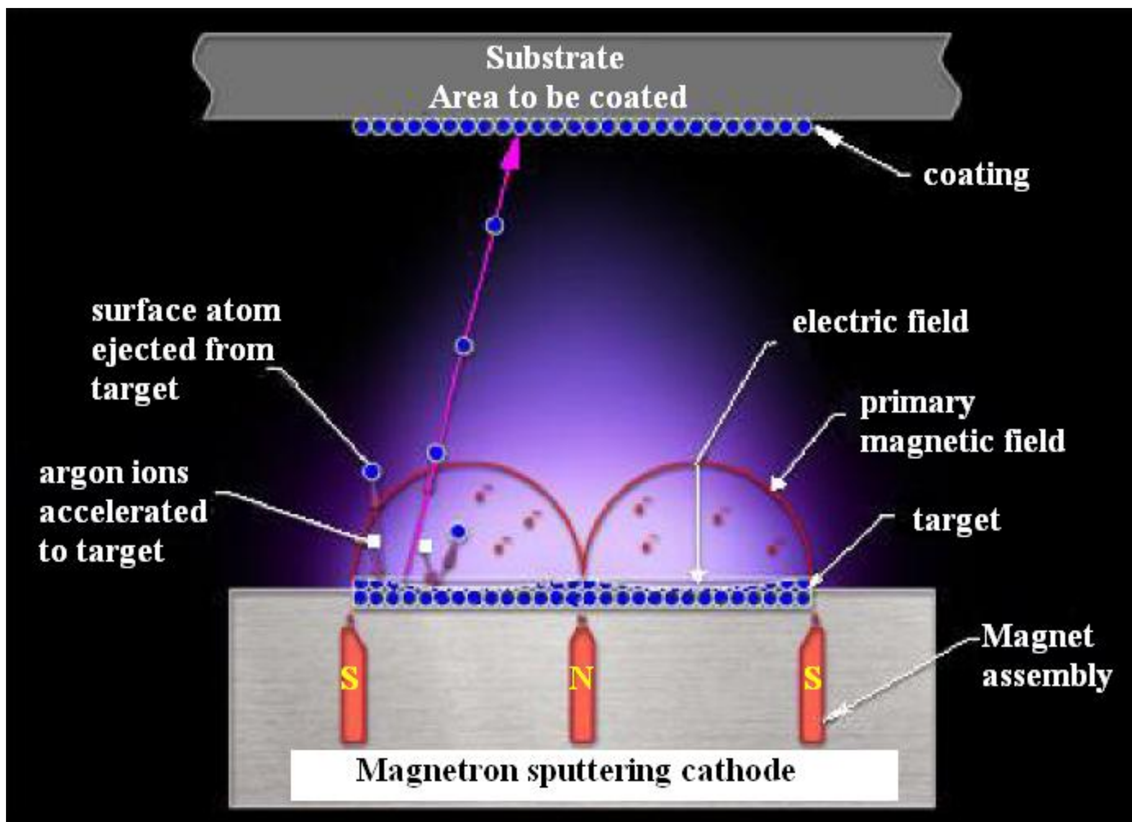


Figure 2.19 Magnetron sputtering.

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Chapter 3

Fabrication of ZnO TFTs on a Glass Substrate

3.1 Fabrication process

Fig. 3.1 schematically illustrates the structure of a ZnO-TFT on a glass substrate in this work. As illustrated, a top-gate and staggered layout is adopted with the insulator area cladding the entire channel area.

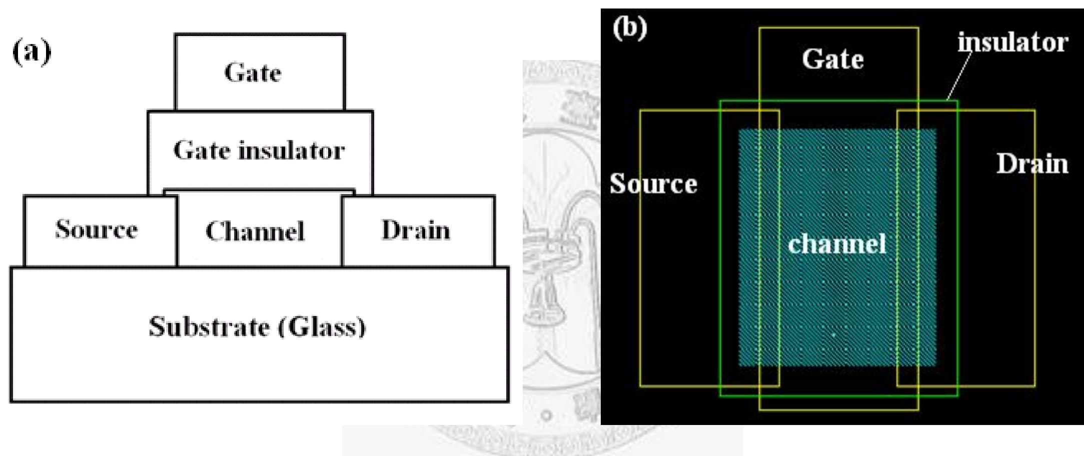
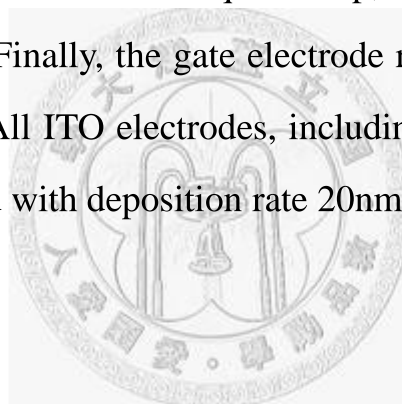


Figure 3.1 The structure of the ZnO-TFT on a glass substrate. (a) A schematic cross-sectional view of TFT structure. (b) A perspective from top view.

Fig. 3.2 shows the flowchart of fabricating a ZnO-TFT on a glass. The sophisticated processing began with ultrasonic cleaning of glass substrates in acetone, methanol and DI (de-ionized) water successively, each for 10 minutes. The glass substrate was then blanket-sputtered with a highly transparent, *n*-type indium tin oxide (ITO). The ITO source and

drain regions were then defined by standard photolithography and wet-etched in HCl/H_2O_2. Then, ZnO channel layer was deposited by RF magnetron sputtering in presence of Ar and O_2. (The optimal flow ratio of Ar to O_2 is examined before fabricating TFT devices. See section 3.2.1.) The purpose of oxygen gas was to moderate the carrier density of the ZnO layer so that enhancement-mode TFTs could be obtained. During the deposition, the wafer holder in sputter system was attached to a water running pipe to remove the generated heat. Moreover, the deposition rate was adequately kept to mitigate the particle bombardment for better polycrystalline quality. In the subsequent step, SiO_2 layer was sputtered as the gate insulator. Finally, the gate electrode region was coated with a sputtered ITO layer. All ITO electrodes, including source, drain and gate contacts, were sputtered with deposition rate 20nm/min.



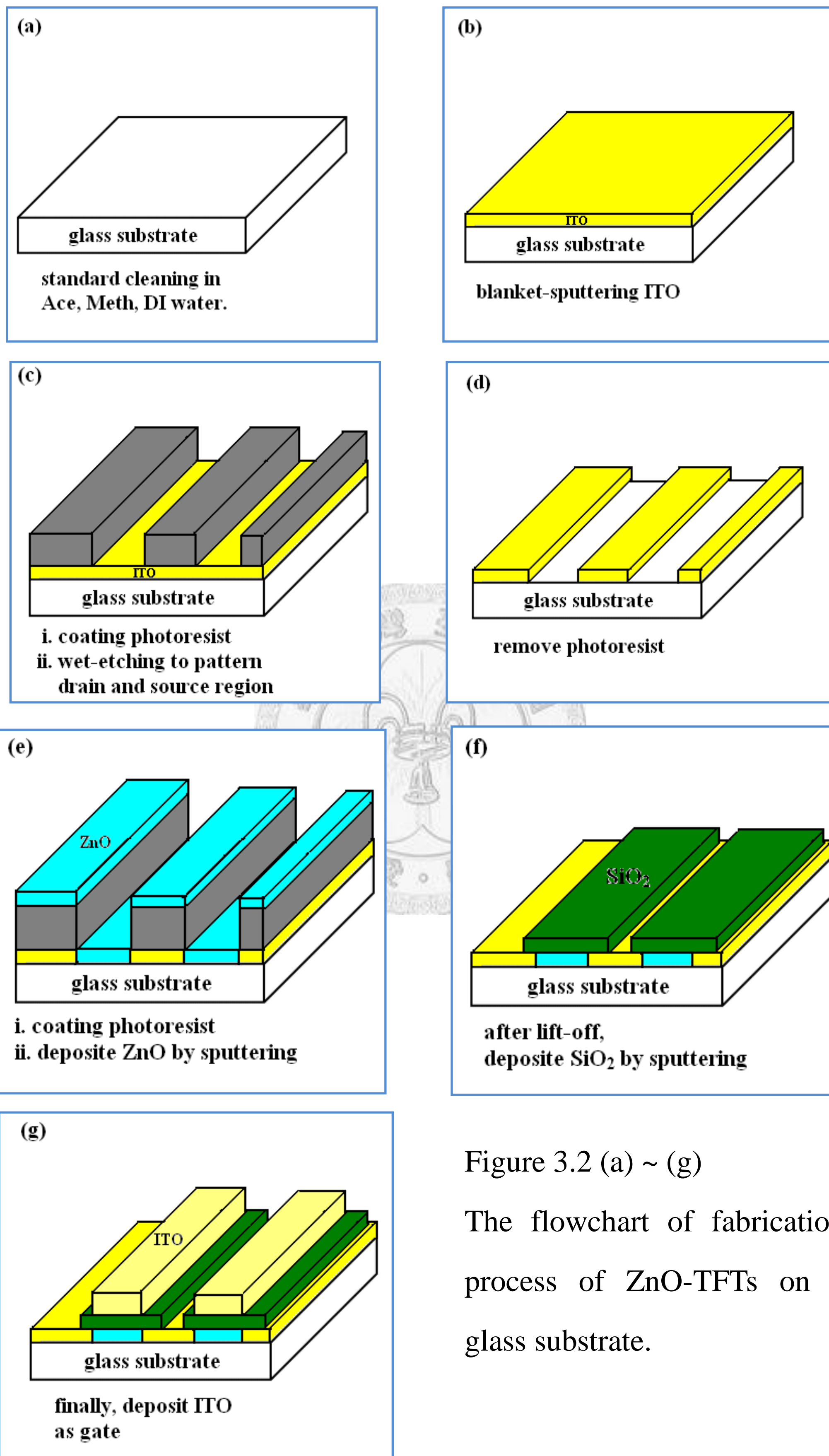


Figure 3.2 (a) ~ (g)

The flowchart of fabrication process of ZnO-TFTs on a glass substrate.

3.2 Results and analysis

3.2.1 Quality of ZnO thin films

The quality of ZnO thin films critically determines the performance of TFTs. Two methods employed to engineer the conductivity of ZnO thin films. One is controlling the gas flow ratio of Ar to O_2 in sputter system and the other is to post-passivate the surface of ZnO thin films by O_2 plasma treatment.

The effect of the gas flow ratio of Ar to O_2 in sputter system is *firstly* investigated. ZnO thin films grown in three conditions, labeled as ZNO-A, ZNO-B, and ZNO-C, are examined with XRD and AFM measurement. Table 3.1 lists the conditions of ZNO-A, ZNO-B, and ZNO-C. The results corresponding to each condition are shown in Fig. 3.3 and Fig. 3.4. The TFTs with ZNO-A, ZNO-B, and ZNO-C as channel layers are labeled as TFT-A, TFT-B, and TFT-C, respectively. The current-voltage relationship of the TFTs is shown in Fig. 3.5.

Table 3.1 ZnO thin films grown in three conditions.

Labels of ZnO films	ZNO-A	ZNO-B	ZNO-C
Ar : O_2	14 : 0	14 : 1	14 : 2
Labels of the TFTs	TFT-A	TFT-B	TFT-C

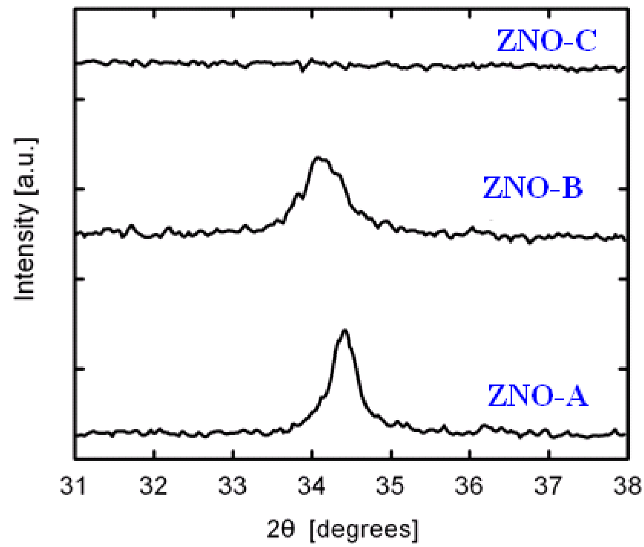


Figure 3.3 XRD data of ZNO-A, ZNO-B and ZNO-C.

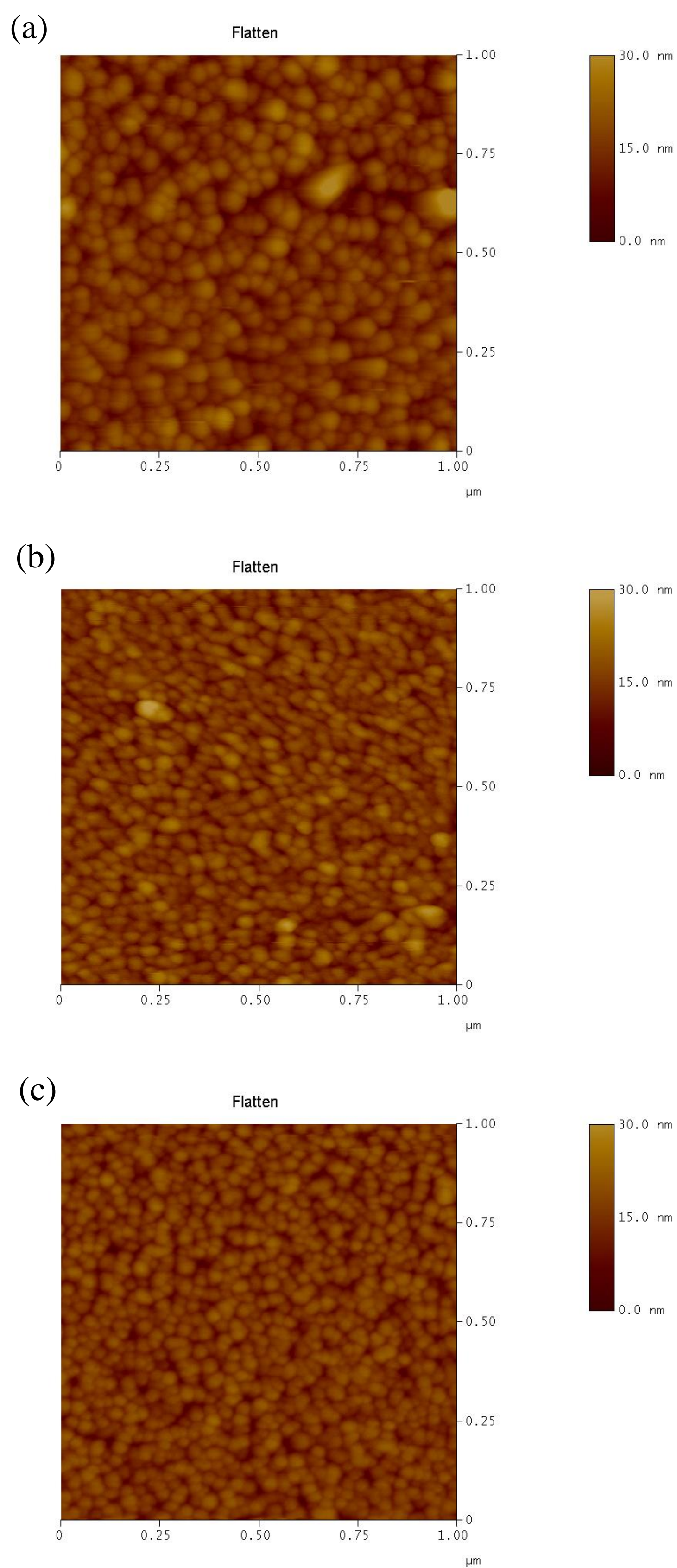


Figure 3.4 AFM images of (a) ZNO-A, (b) ZNO-B and (c) ZNO-C.

Fig. 3.5 (a) TFT-A

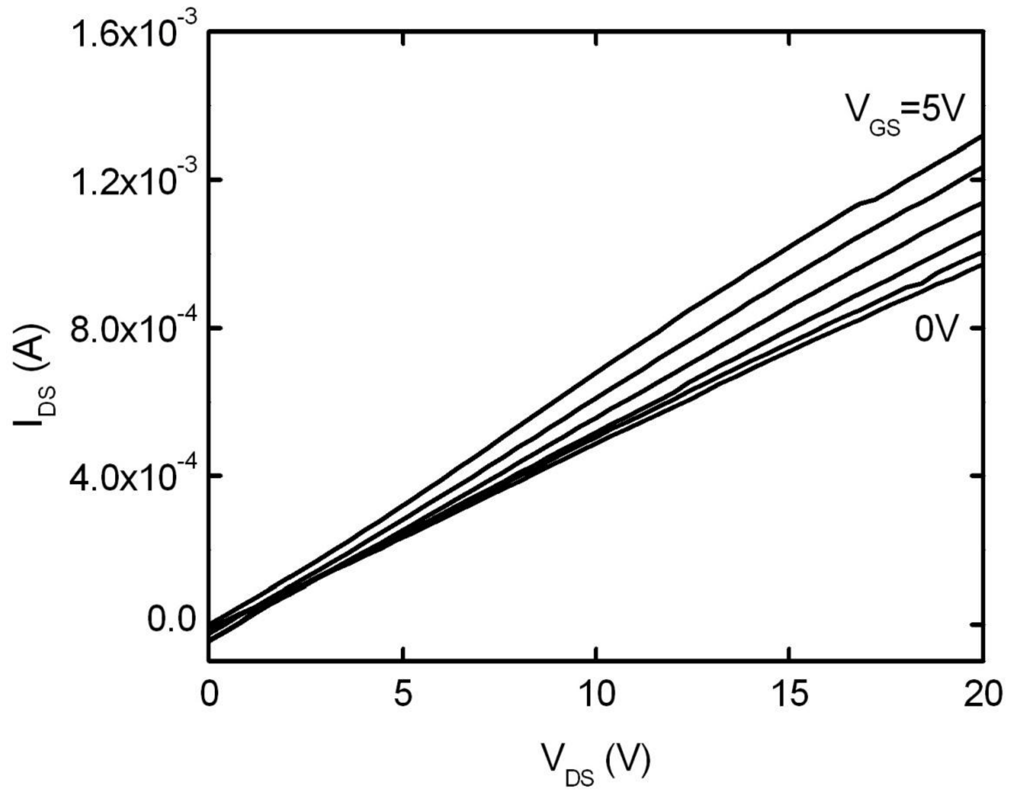


Fig. 3.5 (b) TFT-B

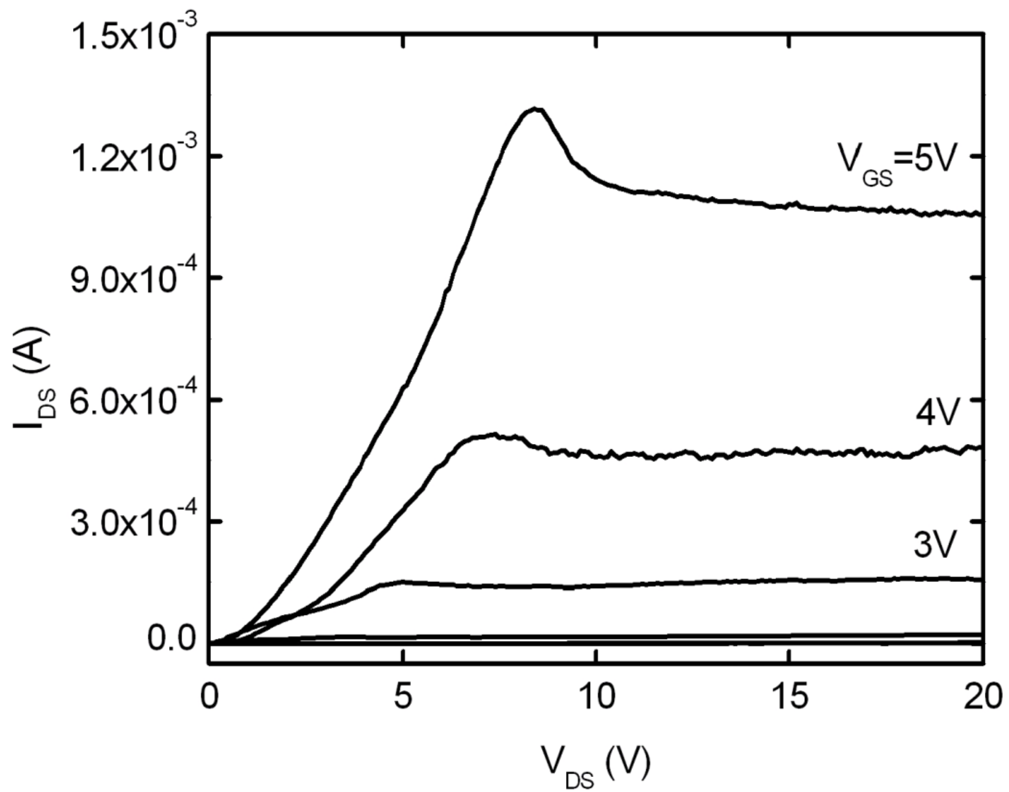


Fig. 3.5 (c)　TFT-C

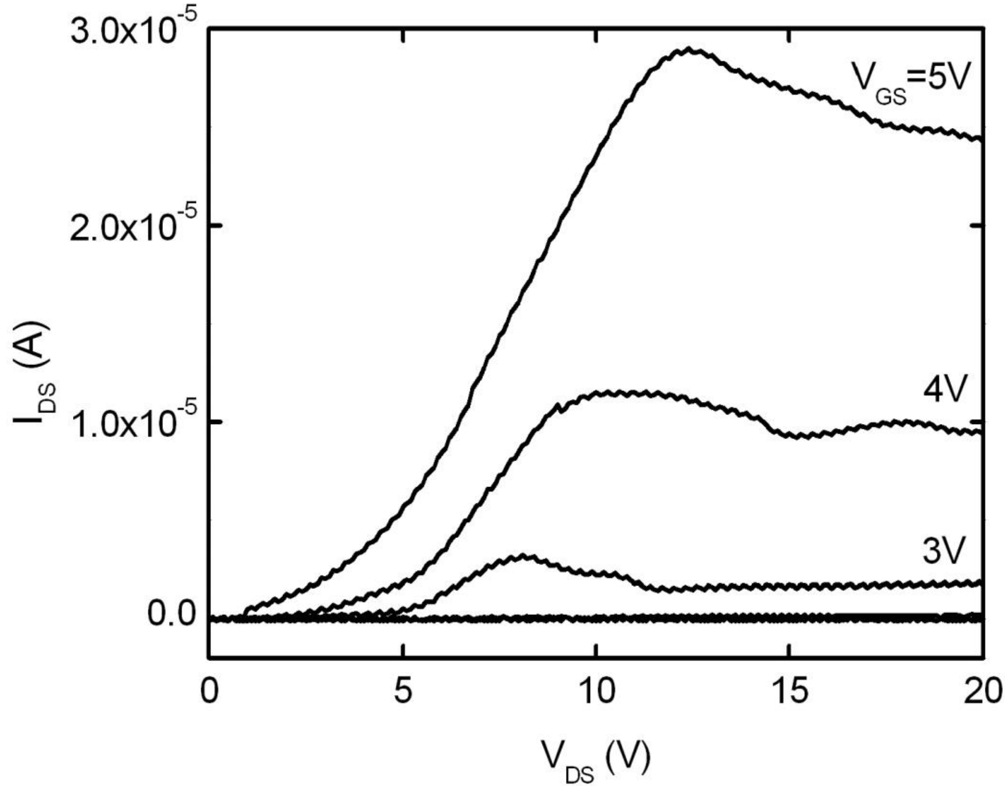


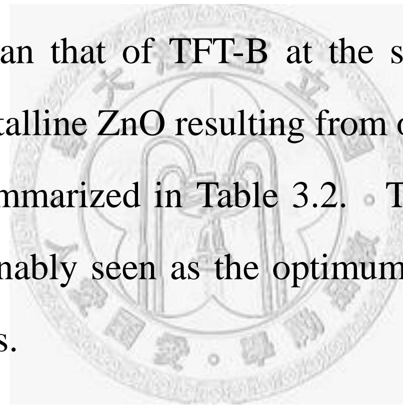
Figure 3.5　I-V curves of the TFTs with (a) ZNO-A, (b) ZNO-B, and (c) ZNO-C as channel layers, respectively.

In general the presence of O_2 in depositing ZnO thin films disturbs the lattice of ZnO crystal, which is evidently seen in Fig 3.3 in that ZNO-C has the lowest peak whereas ZNO-A has the highest peak with the narrowest FWHM (full width at half maximum) of 0.4 degree. Fig. 3.4 indicates larger grain size of ZNO-A than that of ZNO-B and ZNO-C, which again implies better crystallization of ZNO-A.

As for the performance of the TFTs with ZNO-A, ZNO-B, and ZNO-C as channel layers, TFT-A behaves like a perfect resistor without pinched-off channel, which can be attributed to thick equivalent thickness

(t) of effective channel inheriting the better crystalline ZnO. In addition, without presence of O_2 in depositing ZnO channel layer of TFT-A, the amount of oxygen vacancies in the channel of TFT-A is expected to be many. The drain voltage therefore seems powerless to pinch off the *very conductive* channel and the I-V curves do not tend to bend downwards as V_{DS} increases.

TFT-B and TFT-C both act like a transistor with linear and saturation regions because their channels are *not* too conductive to be pinched off. This can be proven by smaller grains seen in Fig. 3.4 (b) and (c), as well as lower peaks seen in Fig. 3.3 for ZNO-B and ZNO-C. However, the I_{DS} of TFT-C is much less than that of TFT-B at the same bias, which can be attributed to worse crystalline ZnO resulting from overdose of O_2.



The results are summarized in Table 3.2. The ratio "14:1" of Ar to O_2 for ZNO-B is reasonably seen as the optimum for fabricating the ZnO TFTs on glass substrates.

Table 3.2 Summary of the results obtained in various ratios of Ar to O_2.

Ar(sccm) : O_2(sccm)		**14 : 0**	**14 : 1**	**14 : 2**
Labels of ZnO films		ZNO-A	ZNO-B	ZNO-C
XRD	Peak (002)	highest	high	X
	FWHM	0.4°	0.98°	X
AFM (grain size)		large	medium	small
Labels of the TFTs		TFT-A	TFT-B	TFT-C
Saturated I_{DS} (V_{GS}=5V, V_{DS}=20V)		X	~1mA	~25uA

The *second* method used to modulate the conductivity of ZnO thin films is post-passivation by O_2 plasma. The experiment is designed as Table 3.3. ZnO thin films subject to O_2 plasma passivation in four conditions, labeled as ZNO-P, ZNO-Q, ZNO-R, and ZNO-S, are examined with XRD and AFM measurement. The results corresponding to each condition are shown in Fig. 3.6, Fig. 3.7, and Fig. 3.8. The TFTs with ZNO-P, ZNO-Q, ZNO-R, and ZNO-S as channel layers are labeled as TFT-P, TFT-Q, TFT-R, and TFT-S, respectively. The current-voltage relationship of the TFTs is shown in Fig. 3.9.

Table 3.3 ZnO thin films post-passivated in four conditions.

Duration (second)	0	150	300	600
Labels of ZnO films	ZNO-P	ZNO-Q	ZNO-R	ZNO-S
Labels of the TFTs	TFT-P	TFT-Q	TFT-R	TFT-S

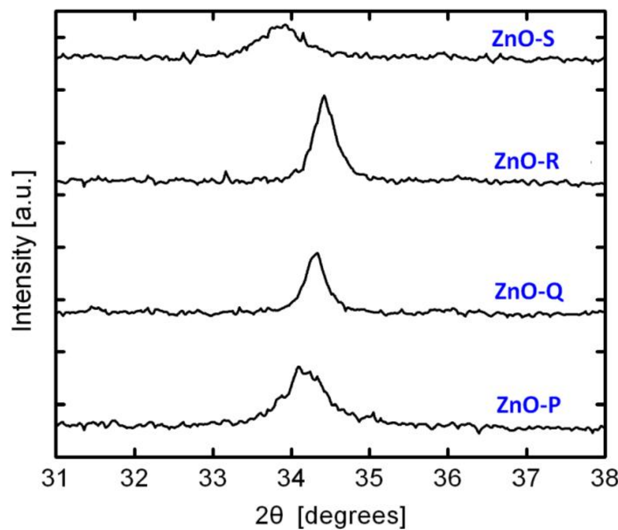


Figure 3.6 XRD data of ZNO-P, ZNO-Q, ZNO-R, and ZNO-S.

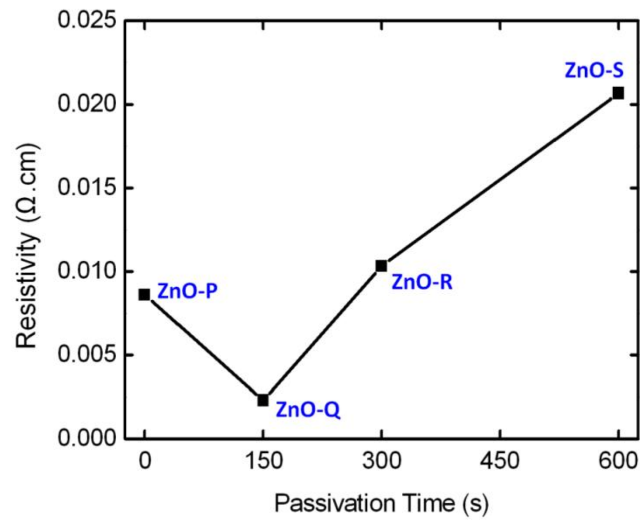
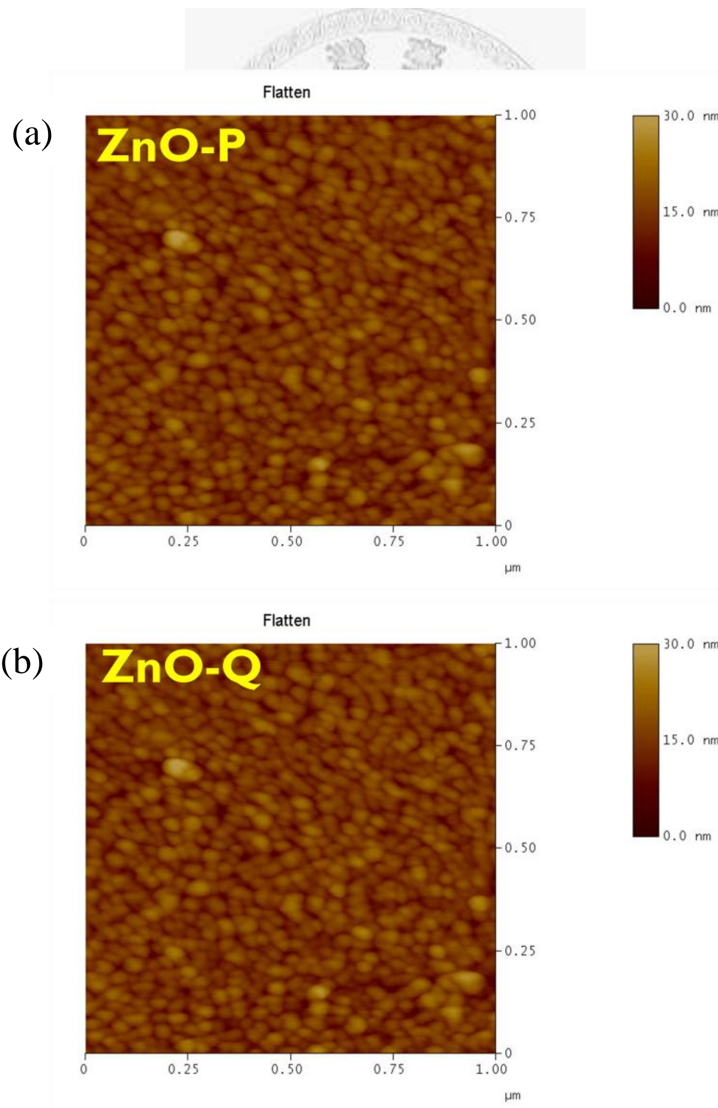


Figure 3.7 Resistivity of ZNO-P, ZNO-Q, ZNO-R, and ZNO-S.



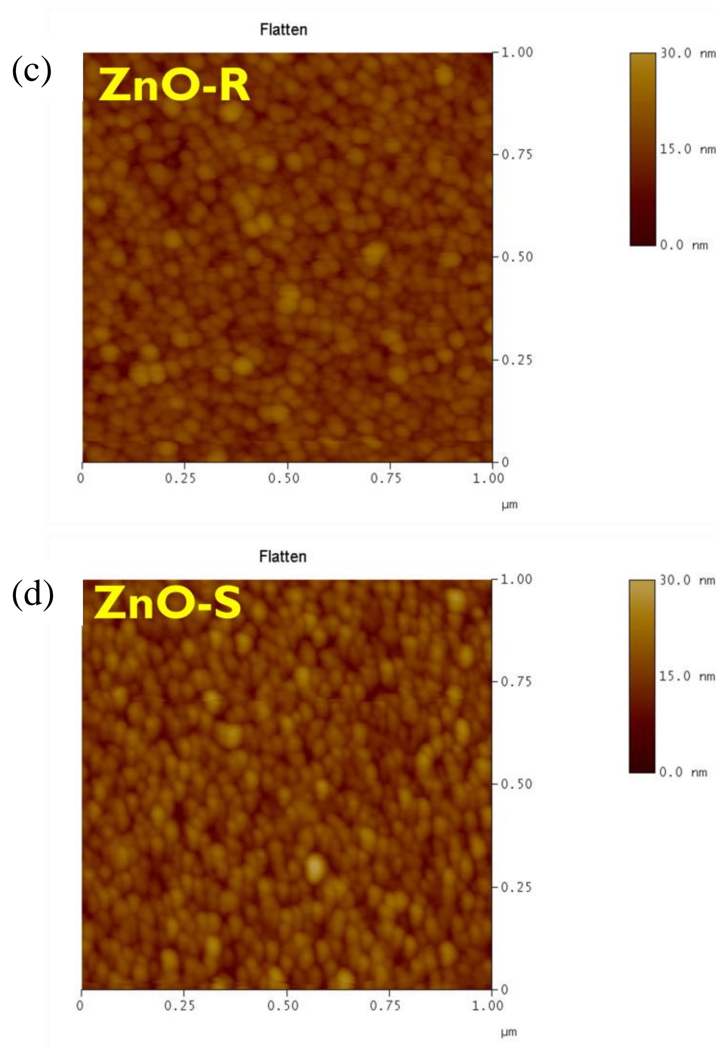


Figure 3.8 AFM images of (a) ZNO-P, (b) ZNO-Q, (c) ZNO-R, and (d) ZNO-S.

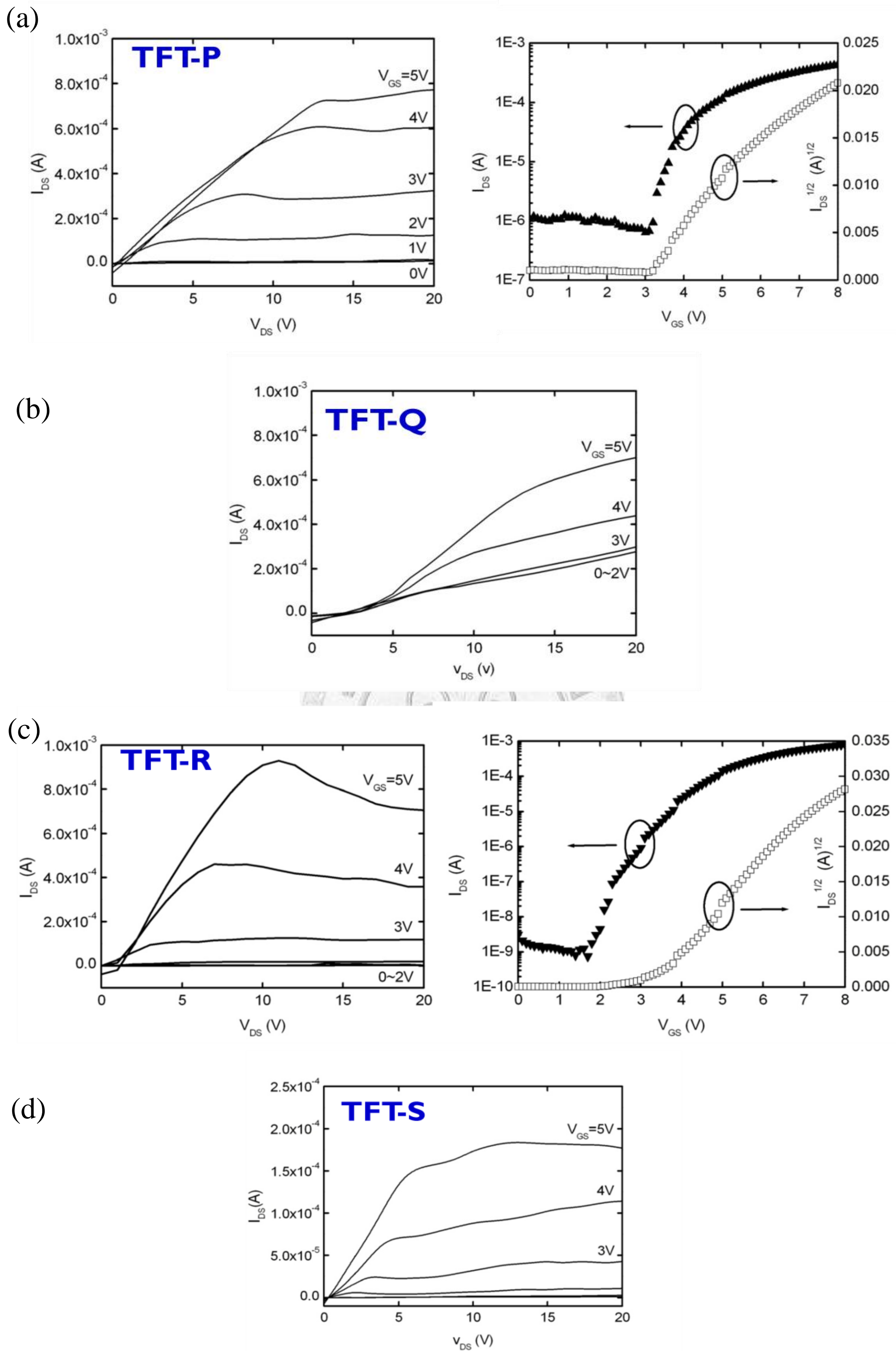


Figure 3.9 I-V curves of the TFTs (a) TFT-P, (b) TFT-Q, (c) TFT-R, and (d) TFT-S. For TFT-P and TFT-R, the transfer curves are included.

Compared with ZNO-P, ZNO-Q has lower resistivity since the plasma ions initiate bombarding the surface during 150 seconds and thus the amount of oxygen vacancy increases. Hereafter, the O_2 plasma starts to compensate the oxygen vacancy so ZNO-R with 300-second treatment has larger resistivity than ZNO-P and ZNO-Q. ZNO-S has much higher resistivity because of few oxygen vacancies. In addition, the structure of ZNO-S, which undergoes overdoing plasma treatment, has been damaged. This can be proven in XRD data where the peak of ZNO-S has shifted to 33.9° whereas the peaks of ZNO-P, ZNO-Q, and ZNO-R locate around the c-plane angle 34.2°.

The AFM images of ZNO-P, ZNO-Q, ZNO-R, and ZNO-S show similar grain size, which indicates the post-passivation does not affect the amorphous structure of ZnO thin films.

As for the performance of the TFTs with ZNO-P, ZNO-Q, ZNO-R, and ZNO-S as channel layers, TFT-Q does not show distinguishable saturation region. TFT-Q has so conductive channel that the gate electric field cannot effectively control the carrier distribution of the channel. TFT-S, on the other hand, has too high resistivity so its operating current is curtailed. TFT-P and TFT-R both act like a good transistor with linear and saturation regions and it can be concluded that the ZnO films (ZNO-P and ZNO-R) with resistivity about 0.01 Ωcm can fulfill good transistor performance. However, the on-off ratio of TFT-P is less than that of TFT-R at the same bias.

The results are summarized in Table 3.4. The duration “300 seconds”

for ZNO-R is also reasonably seen as the optimum for fabricating the ZnO TFTs on glass substrates.

Table 3.4 Summary of the results obtained in various duration of O_2 plasma treatment

Duration (sec)		**0**	**150**	**300**	**600**
Labels of ZnO films		ZNO-P	ZNO-Q	ZNO-R	ZNO-S
XRD	Peak (002)	lower	lower	highest	lowest
	FWHM	1.05°	0.43°	0.44°	1.17°
AFM (grain size)		small	small	small	small
Labels of the TFTs		TFT-P	TFT-Q	TFT-R	TFT-S
I_{DS} (V_{GS}=5V, V_{DS}=15V)		~0.8mA	~0.6mA	~0.8mA	~0.18mA
On-off Ratio		2.83×10^{2}	--	1.47×10^{6}	--
V_{th} (V)		3.1	--	3	--
Field-Effect Mobility (cm^2/Vs)		239.1	--	391.6	--

However, the method of surface passivation by O_2 plasma may cause unwanted extra defects in the surface by kinetic plasma ions and the non-uniform distribution of carrier concentration of the channel so controlling the gas flow ratio of Ar to O_2 in sputter system to engineer the conductivity of ZnO thin films is much more recommended.

3.2.2 Performance of the ZnO-TFTs

Based on the optimum ratio “14:1” of Ar to O_2, the ZnO-TFTs fabricated with various dimensions of the channel layers are labeled in Table 3.5, which also includes the TFTs with the specific treatments to the channel layers and the TFTs with post-annealing. The I-V curves of all these TFTs are shown in Fig. 3.10 (a) ~ 3.10 (o), respectively and each I_{DS} is recorded in Table 3.5 as well.

Table 3.5 The ZnO-TFTs fabricated in various conditions and their related performance I_{DS} and On-off ratio included.

Label	Channel dimension: Width / Length (μm / μm)	Substrate temperature when depositing ZnO (°C)	Characteristic	
			I_{DS} (mA) (at V_{GS}=5V, V_{DS}=20V)	On-off ratio
TFT-A63	600 / 300	Room temperature	0.48	4.1×10^{5}
TFT-A83	800 / 300	Room temperature	0.5	2.6×10^{4}
TFT-A03	1000 / 300	Room temperature	1.1	3.6×10^{6}
TFT-B63	600 / 300	150	0.8	4.0×10^{3}
TFT-B83	800 / 300	150	1.1	2.7×10^{6}
TFT-B03	1000 / 300	150	1.2	8.6×10^{2}

Label	Channel dimension: Width / Length (μm / μm)	Post-annealing temperature (°C)	Characteristic	
			I_{DS} (mA) (at V_{GS}=5V, V_{DS}=20V)	On-off ratio
TFT-PA63	600 / 300	200	0.23	3.9×10^{1}
TFT-PA83	800 / 300	200	0.35	2.6×10^{2}
TFT-PA03	1000 / 300	200	0.3	1.0×10^{2}
TFT-P2A63	600 / 300	400	0.33	3.5×10^{2}
TFT-P2A83	800 / 300	400	1.2	3.9×10^{2}
TFT-P2A03	1000 / 300	400	1.1	5.8×10^{1}
TFT-P3A63	600 / 300	600	0.1	2.1×10^{1}
TFT-P3A83	800 / 300	600	0.08	-
TFT-P3A03	1000 / 300	600	0.25	-

Fig. 3.10 (a)

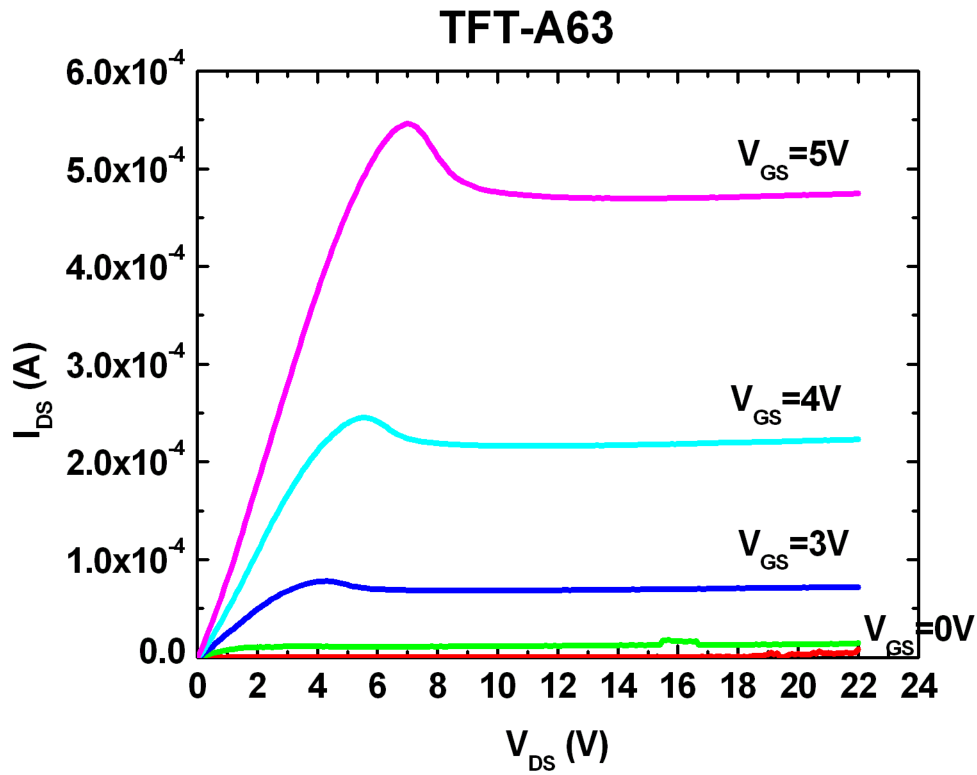


Fig. 3.10 (b)

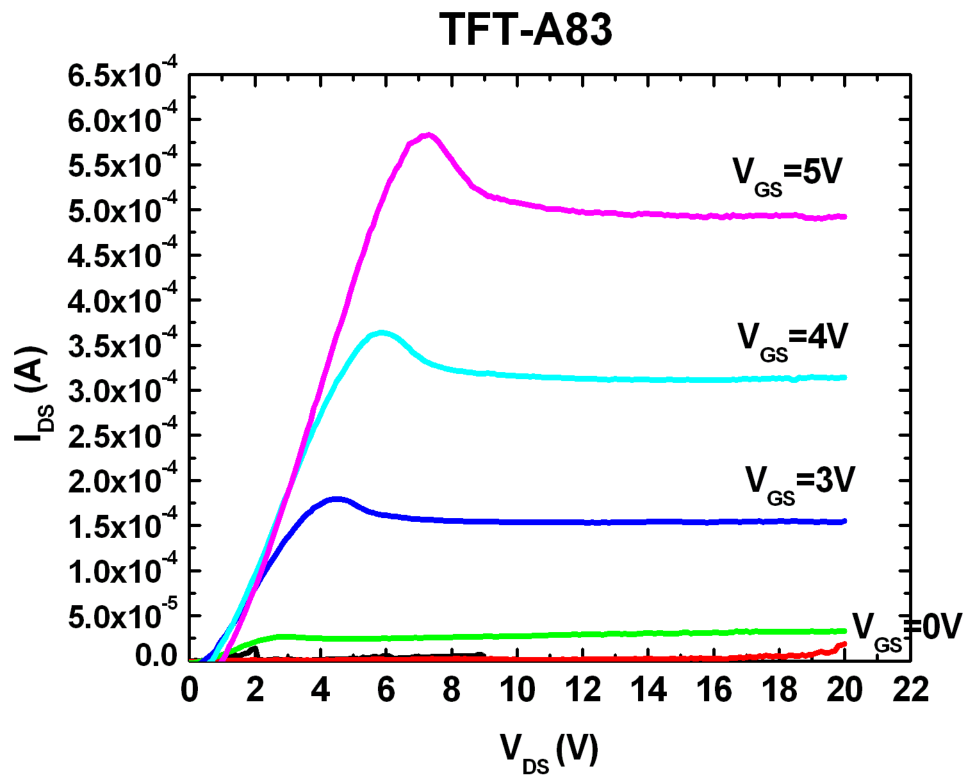


Fig. 3.10 (c)

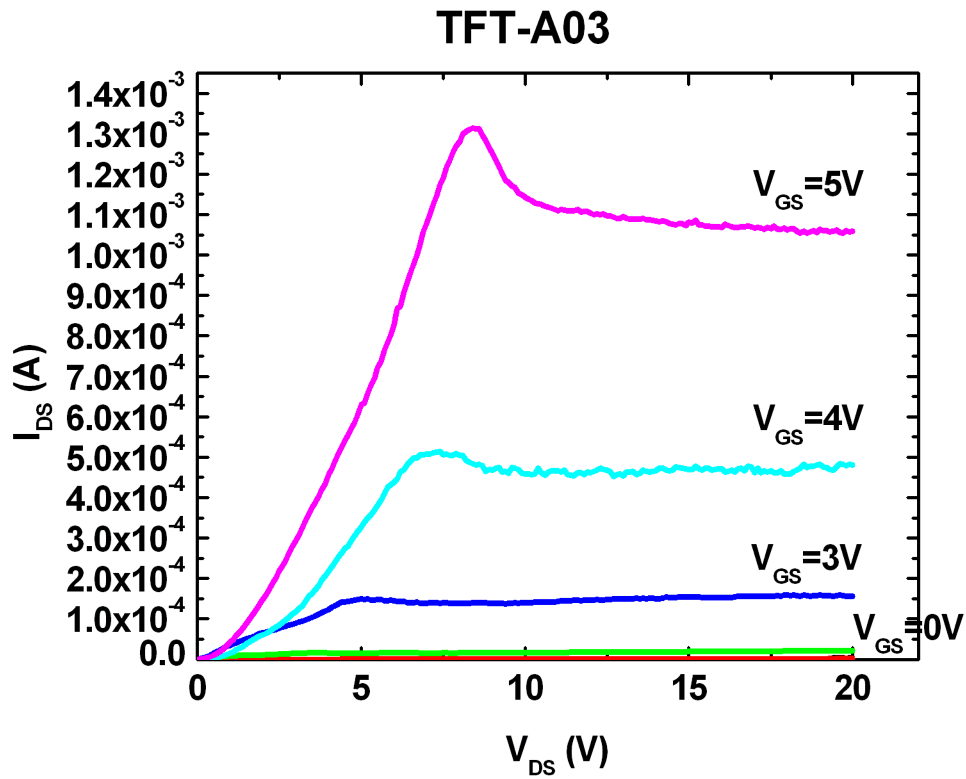


Fig. 3.10 (d)

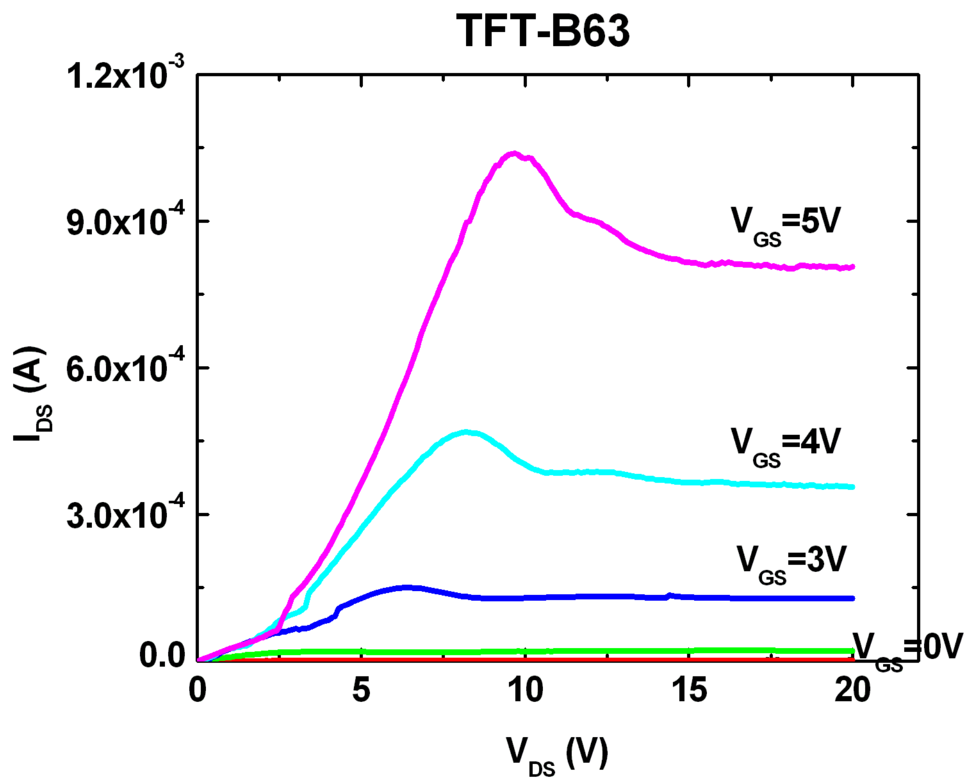


Fig. 3.10 (e)

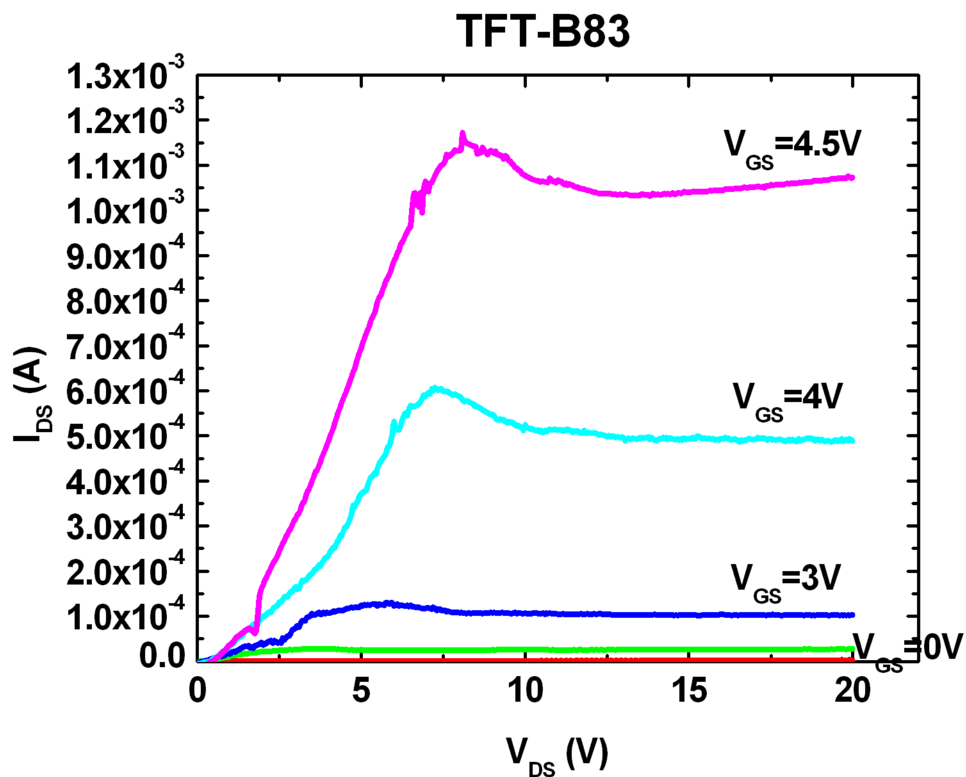


Fig. 3.10 (f)

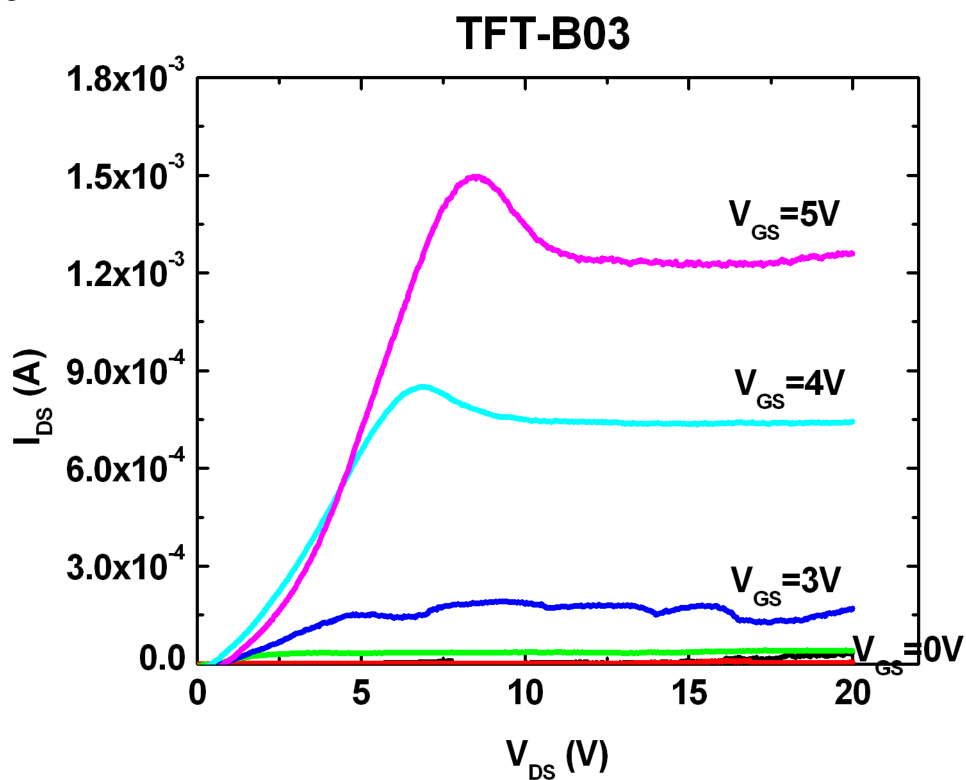


Fig. 3.10 (g)

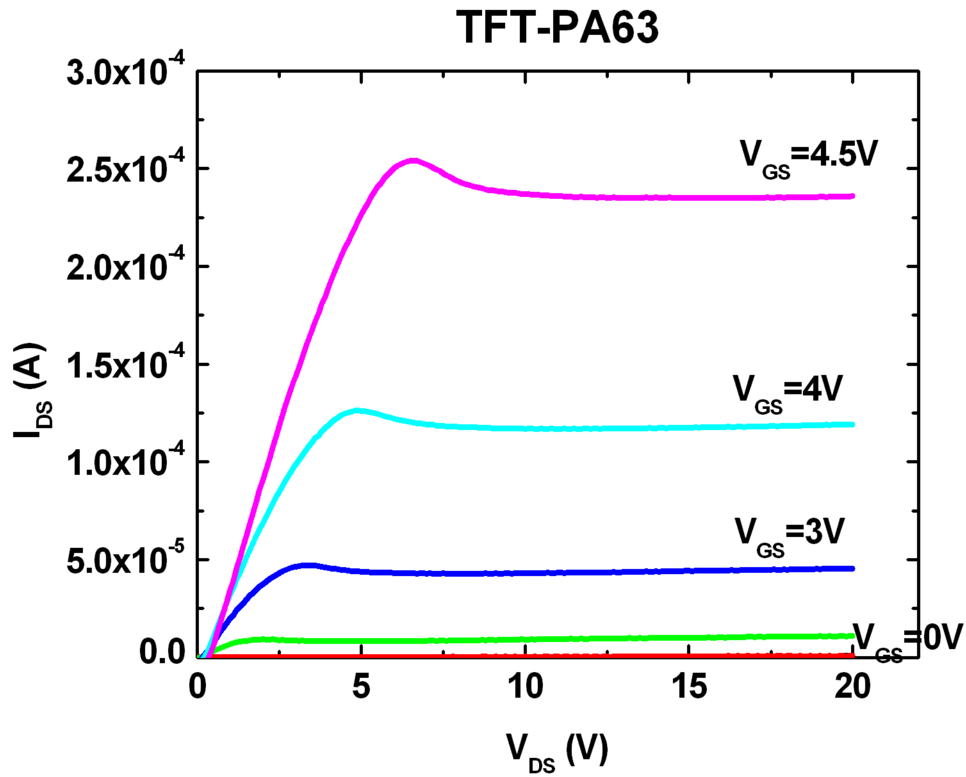


Fig. 3.10 (h)

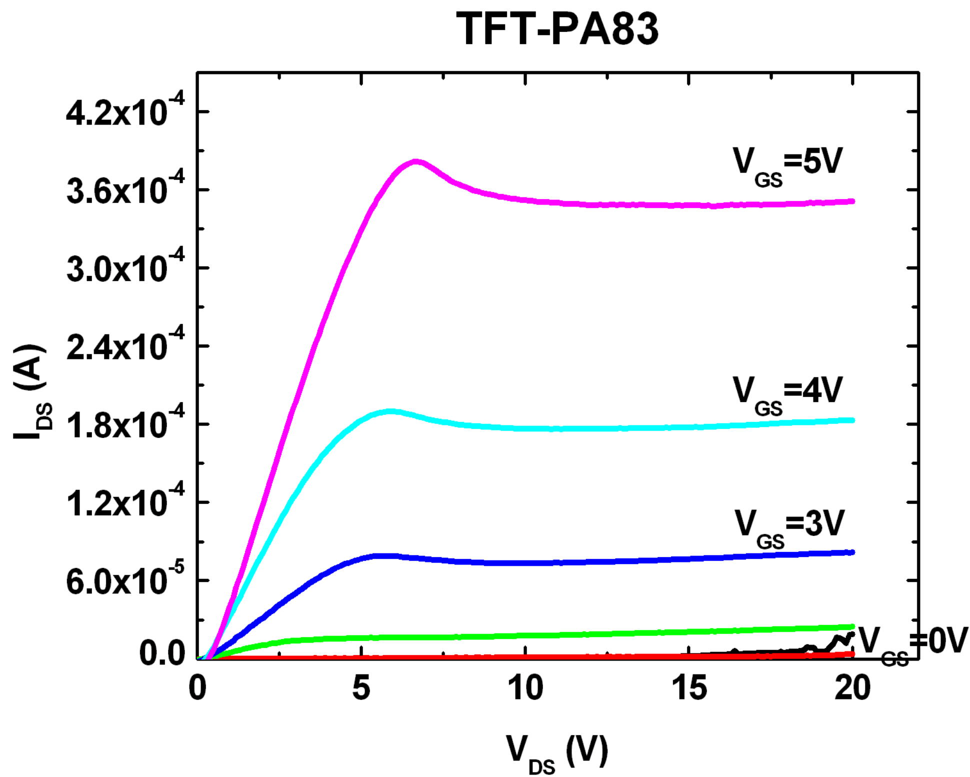


Fig. 3.10 (i)

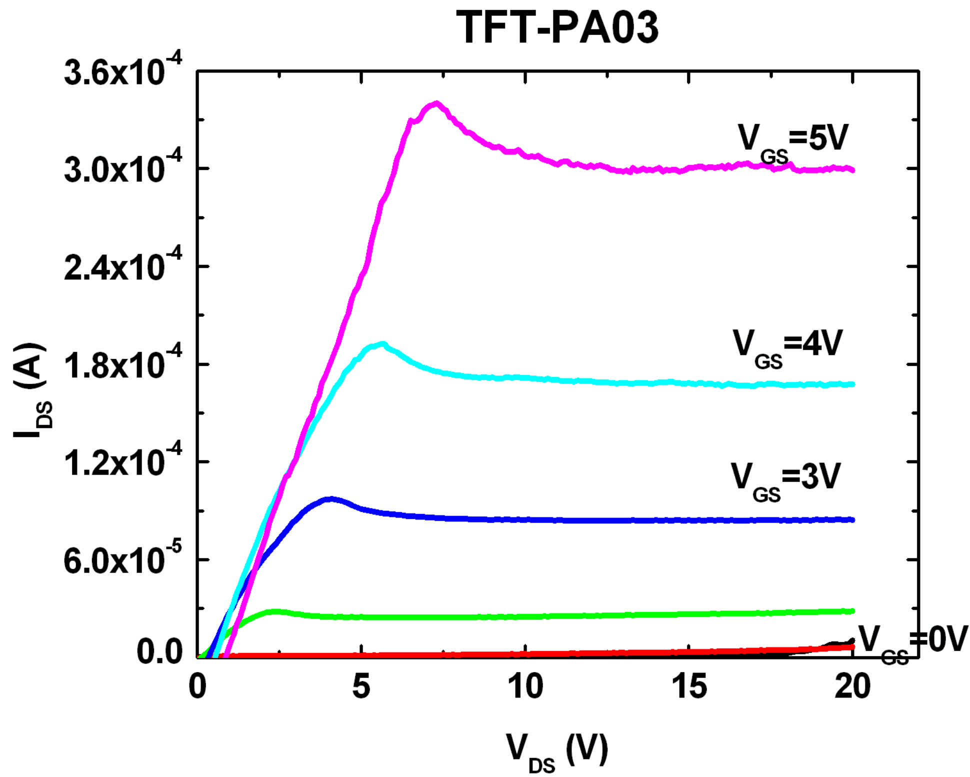


Fig. 3.10 (j)

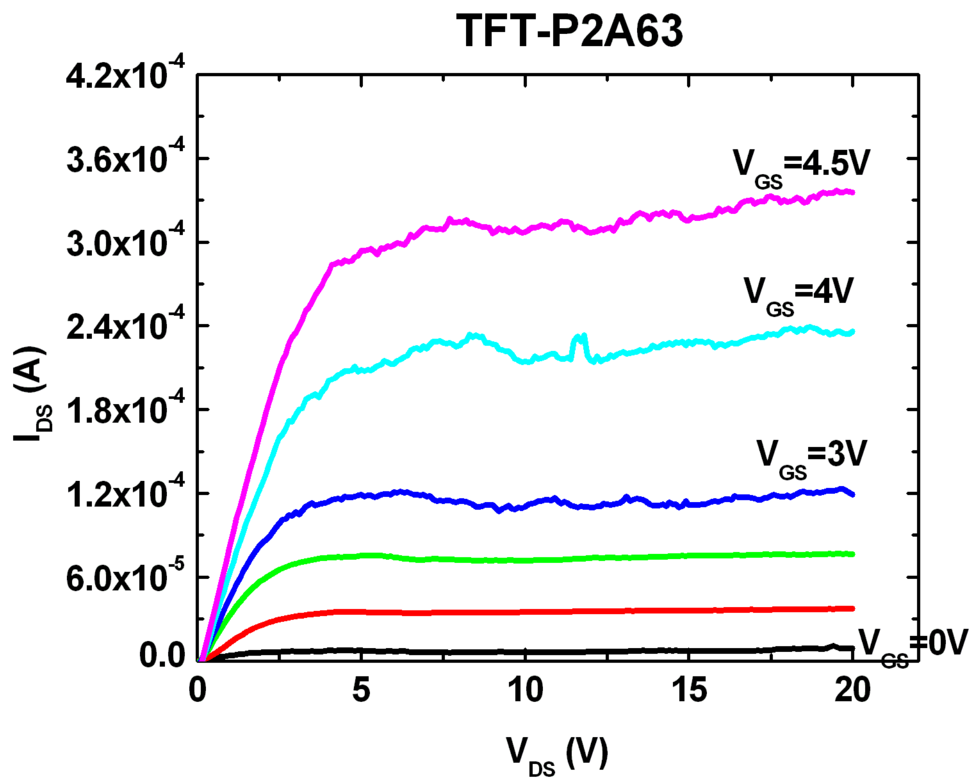


Fig. 3.10 (k)

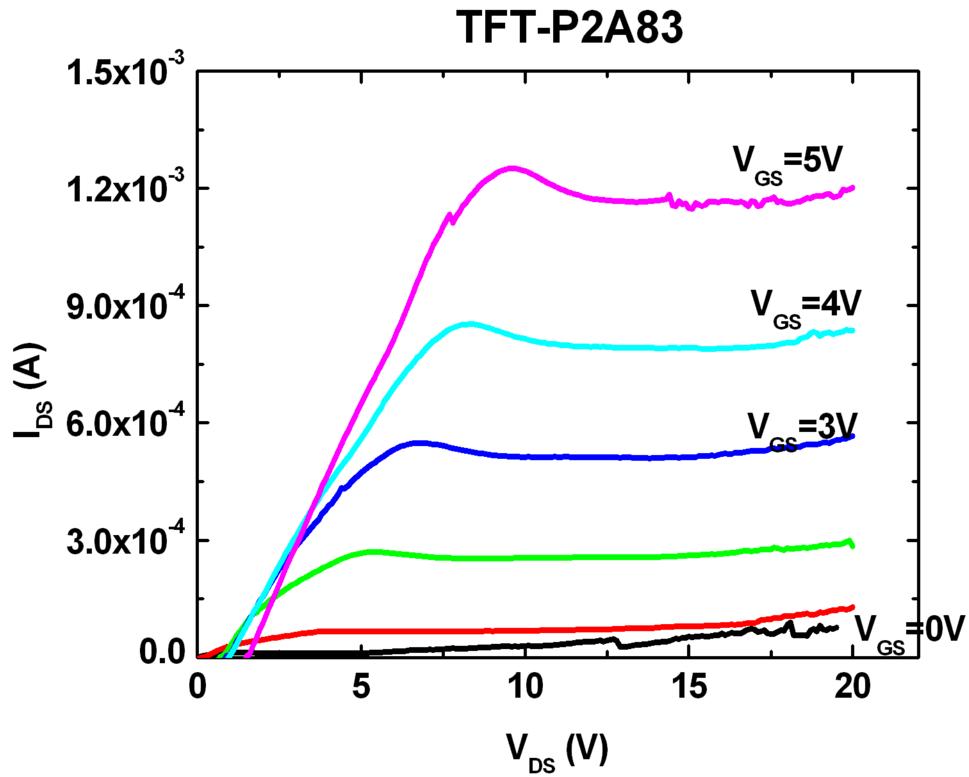


Fig. 3.10 (*l*)

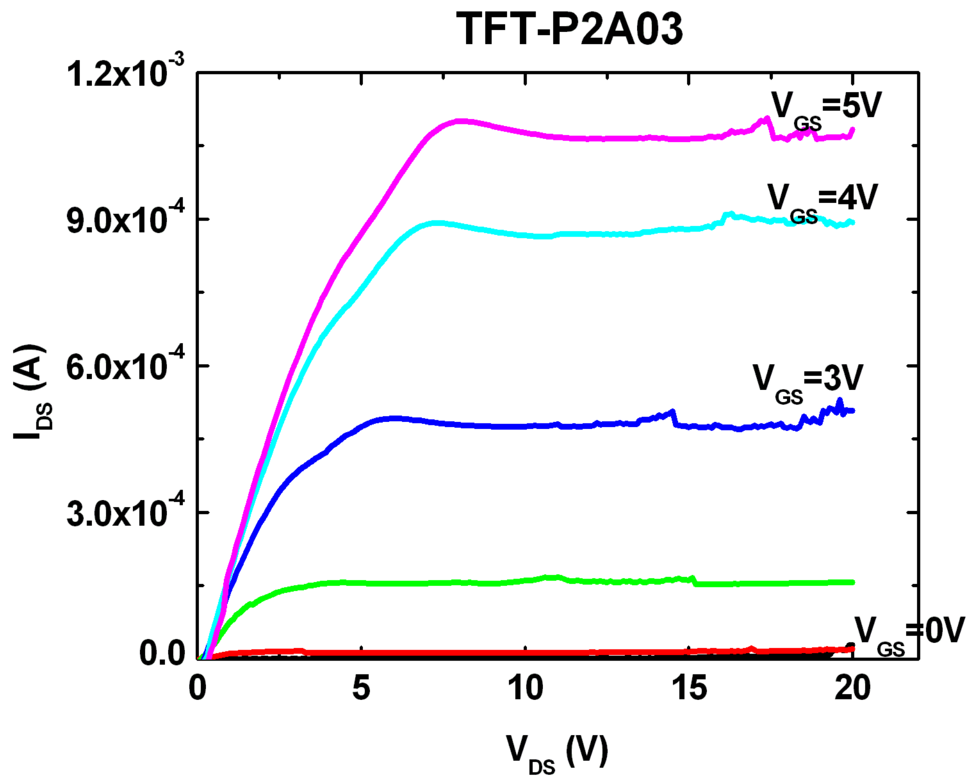


Fig. 3.10 (m)

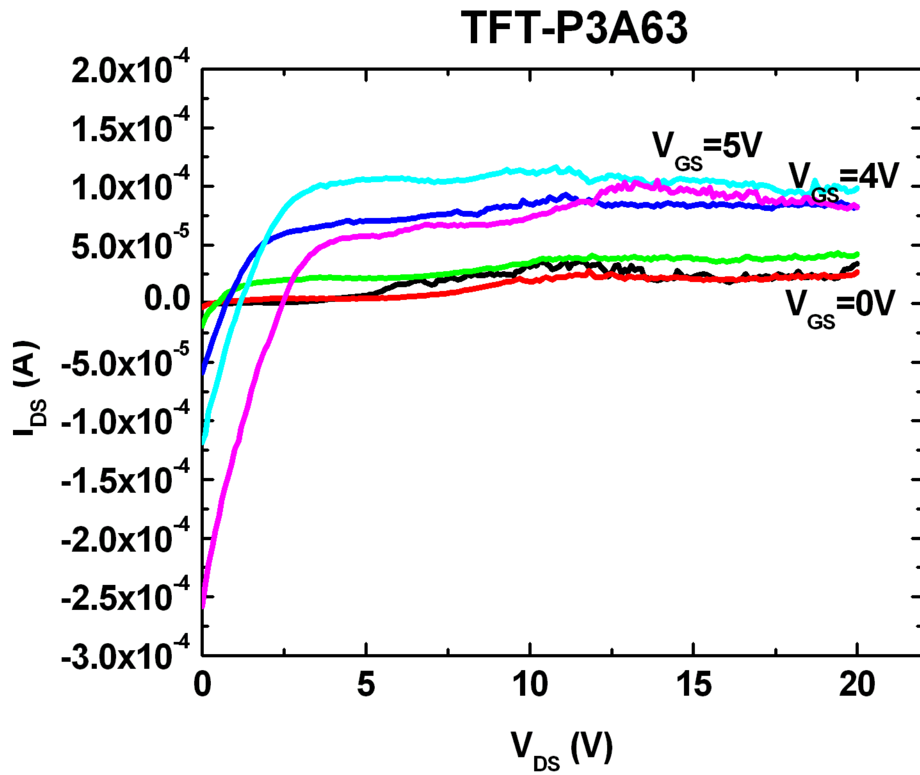


Fig. 3.10 (n)

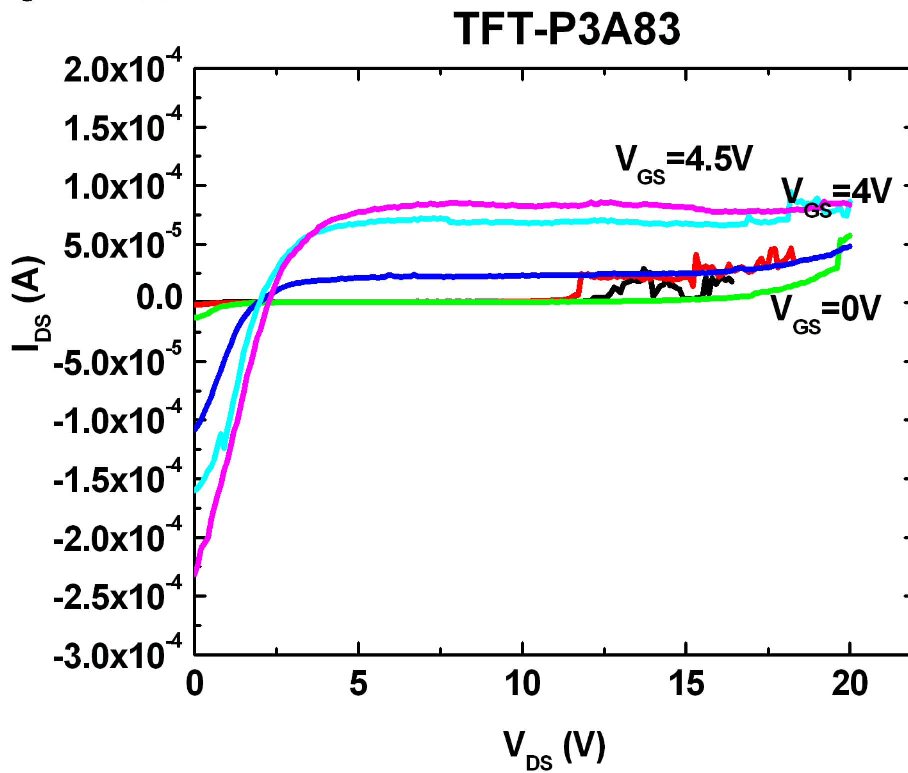


Fig. 3.10 (o)

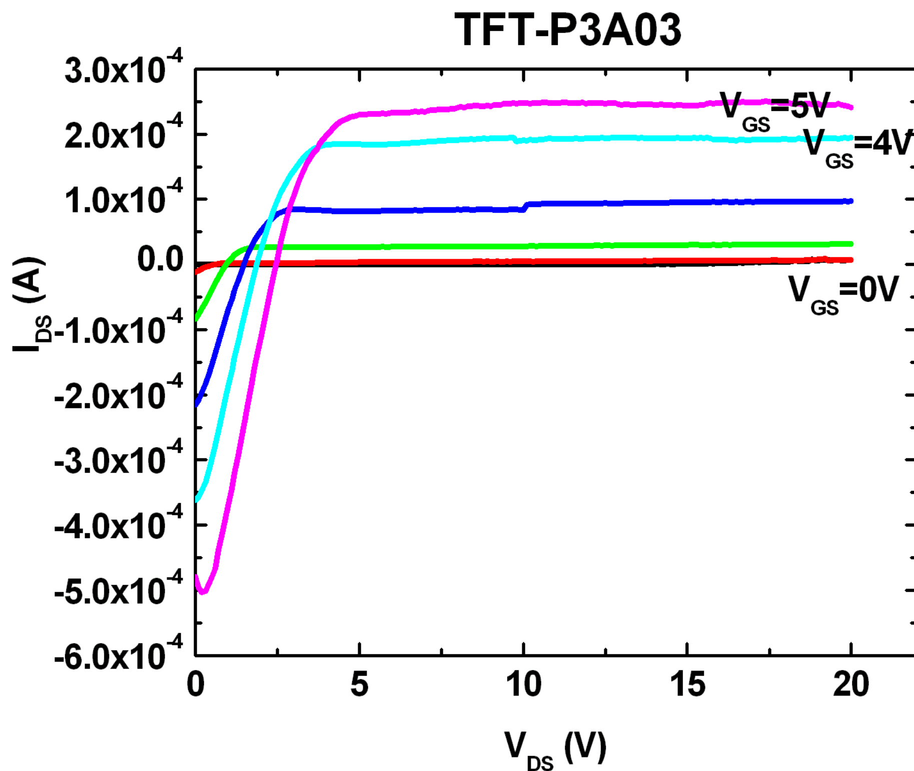


Figure 3.10 (a) ~ (o) The I-V curves of the ZnO-TFTs fabricated in various conditions as listed in table 3.2.

From above results, some important observations are concluded as follows:

1. As the ratio of width to length increases, the I_{DS} at the same bias increases, apparently seen in "TFT-A63, TFT-A83, TFT-A03" and "TFT-B63, TFT-B83, TFT-B03." This substantially agrees with equation 2-2 given in section 2.1.1.
2. Generally, the I_{DS} of the ZnO-TFTs without post-annealing can achieve as large as 0.5 to 1.2 mA. However, it's observed that an overshoot at the onset of saturation region obviously exists in Fig. 3.10 (a), (b), (c), (d), (e), and (f). A comparison of a ZnO-TFT

and a NMOS can help explain the overshoot in the I-V curves of the ZnO-TFTs, as illustrated in Table 3.6. The depletion region appears right after the channel of the NMOS has been pinched off; hereafter, most of excess V_{DS} is applied to the depletion region so the channel remains unchanged as $V_{DS} > V_{Dsat0}$ and hence the I_{DS} remains constant. Unlike the NMOS, the ZnO-TFT has no intrinsic depletion region between the junction of the drain (ITO) and the channel (ZnO); therefore, after the channel of the ZnO-TFT has been pinched off, the bulk ZnO reappears in the junction of the drain and the channel as $V_{DS} > V_{Dsat0}$. Because the bulk ZnO is less conductive, the I_{DS} begins to descend as $V_{Dsat0} < V_{DS} < V_{Dsat1}$. When the region of the reappearing bulk ZnO is large enough to be capable of taking most of excess V_{DS}, the channel can be unchanged and thus the I_{DS} remains constant; this happens as $V_{DS} > V_{Dsat1}$.

3. The I-V curves of the ZnO-TFTs with post-annealing show significant leakage currents (at $V_{DS} = 0$ and $V_{GS} = 5V$), especially in Fig. 3.10 (m), (n) and (o). The leakage currents can be attributed to the destroyed insulator because the metal atoms, such as indium or tin, with high kinetic energies may diffuse into the insulating layer. The transistor behaviors extremely degenerate when annealing temperature exceeds 400°C because atoms with overly high kinetic energies crash the quality of TFTs.
4. The I_{on}/I_{off} ratios range from 10^3 to 10^6 so the ZnO-TFTs have potential to drive AM-LCD (active matrix liquid crystal display).

Table 3.6 The comparison of the channel behaviors and corresponding I-V curves of an NMOS and a ZnO-TFT.

$V_{GS}>V_{th}$	NMOS		ZnO-TFT	
	channel	I-V curve	channel	I-V curve
$V_{DS} < V_{Dsat0}$	channel, depletion region, n^+, n^+, p	I_{DS}, V_{Dsat0}, V_{Dsat1}, V_{Dsat2}	channel, bulk ZnO, ITO, ITO	I_{DS}, V_{Dsat0}, V_{Dsat1}, V_{Dsat2}
$V_{DS} = V_{Dsat0}$	channel, depletion region, n^+, n^+, p	I_{DS}, V_{Dsat0}, V_{Dsat1}, V_{Dsat2}	channel, bulk ZnO, ITO, ITO	I_{DS}, V_{Dsat0}, V_{Dsat1}, V_{Dsat2}
$V_{DS} > V_{Dsat0}$	channel, depletion region, n^+, n^+, p	I_{DS}, V_{Dsat0}, V_{Dsat1}, V_{Dsat2}	channel, bulk ZnO, ITO, ITO	I_{DS}, V_{Dsat0}, V_{Dsat1}, V_{Dsat2}
$V_{DS} > V_{Dsat1}$	channel, depletion region, n^+, n^+, p	I_{DS}, V_{Dsat0}, V_{Dsat1}, V_{Dsat2}	channel, bulk ZnO, ITO, ITO	I_{DS}, V_{Dsat0}, V_{Dsat1}, V_{Dsat2}

3.2.3 Performance of the best ZnO-TFT

This section is meant to detail the characteristic of *the best* ZnO-TFT ever obtained in my work.

The current-voltage characteristics were measured by using an Agilent 4155C. Measurements were performed in dark to avoid light induced photo currents. The I_{DS}-V_{DS} curves of the ZnO-TFT before alloy are showed in Fig. 3.7 (a). The I_{DS} is 1.06 mA at the bias condition V_{GS}= 5 V and V_{DS}= 20 V. The enhancement-mode ZnO thin film transistor implies that the power dissipation can be minimized when the device is normally-off, making it suitable for applications which power consumption is a concern. Fig. 3.7 (b) shows the transfer characteristics and the gate leakage current. The I_{on}/I_{off} ratio, calculated from the drain current at its maximum and minimum value, is 3×10^{6}. The gate leakage current is smaller than 3×10^{-8} A within V_{GS} less than 7V, which is attributed to a high-quality SiO_2 gate insulting layer during device fabrication. Furthermore, the threshold voltage, determined from the $(I_{DS})^{1/2}$-V_{GS} curve, is around 1.7V. The low threshold voltage ensures that ZnO TFT circuits be operated at a low voltage and thus low power consumption can be satisfied.

To reduce the contact (drain-channel, and source-channel) resistance, the sample was then subject to 200°C, 15-minute rapid thermal process in N_2. The electrical characteristics are revealed in Fig. 3.8. The currents in the saturation region in Fig. 3.8 (a) show little difference from those before alloy, indicating that the carrier mobility in the ZnO layer is not much affected by the alloy condition. The slopes of I_{DS}-V_{DS} curves in the

triode region are much more linear and the overshoot at the onset of saturation region is suppressed for devices after alloy. The improvement of the device performance is attributed to a better contact condition between source/drain ITO and the ZnO layer. As for the transfer characteristics, the I_{on}/I_{off} ratio becomes 3×10^{4} and the gate leakage current increase to 2×10^{-7} A at V_{GS} = 7V after thermal anneal.

Fig. 3.7 (a)

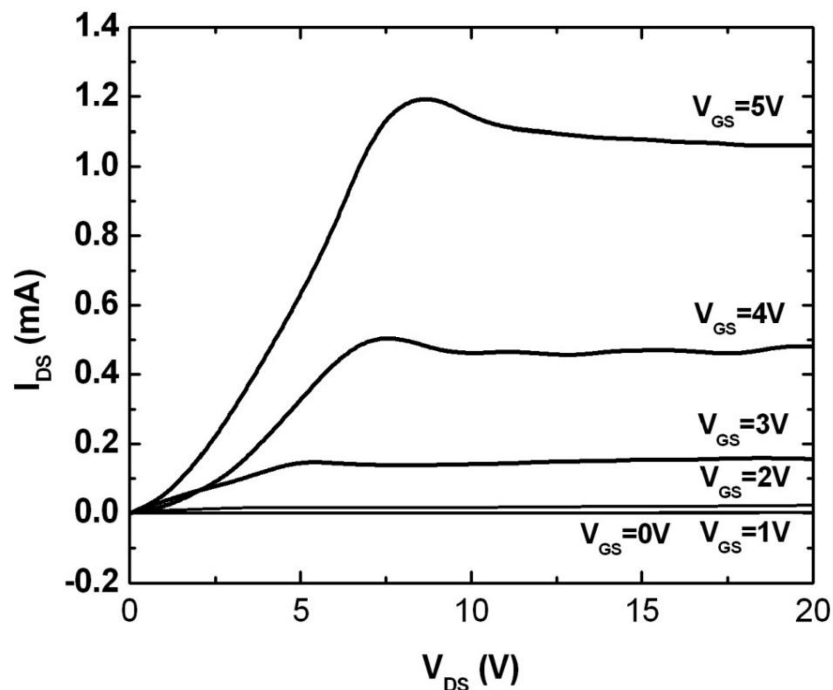


Fig. 3.7 (b)

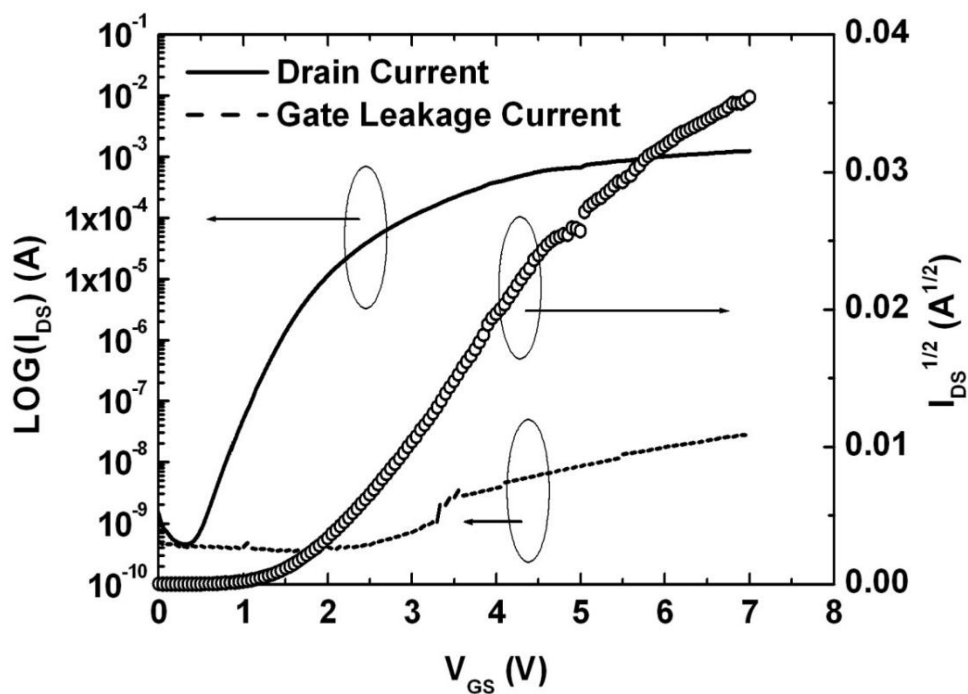


Figure 3.7 Electrical characteristics of the best ZnO-TFT before alloy. (a) I_{DS} - V_{DS} curves. (b) Log scale I_{DS} and I_{GS} as a function of V_{GS} at V_{DS}=20V, and the $(I_{DS})^{1/2}$-V_{GS} curve for determining the threshold voltage.

Fig 3.8 (a)

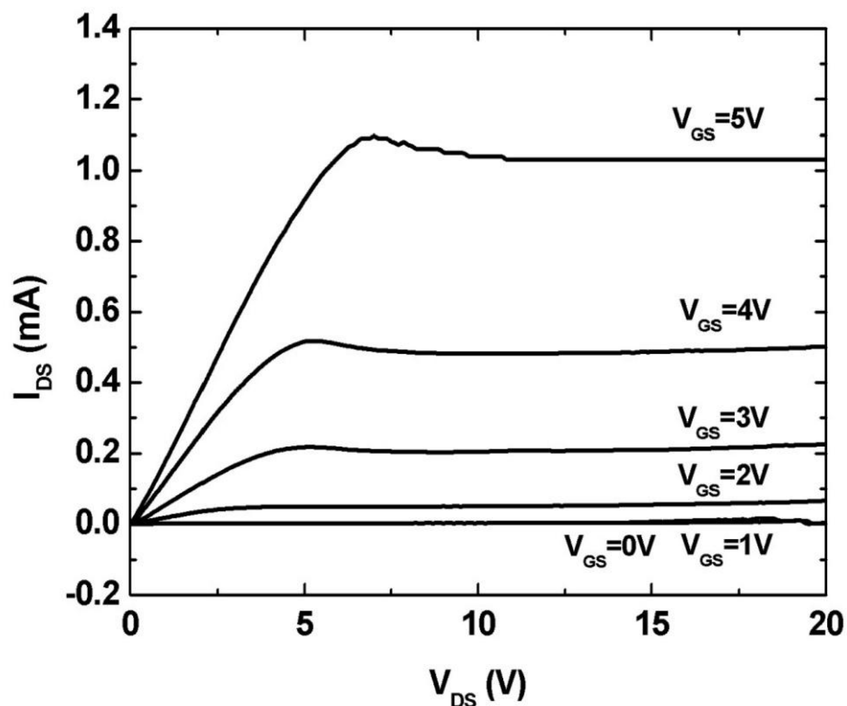


Fig 3.8 (b)

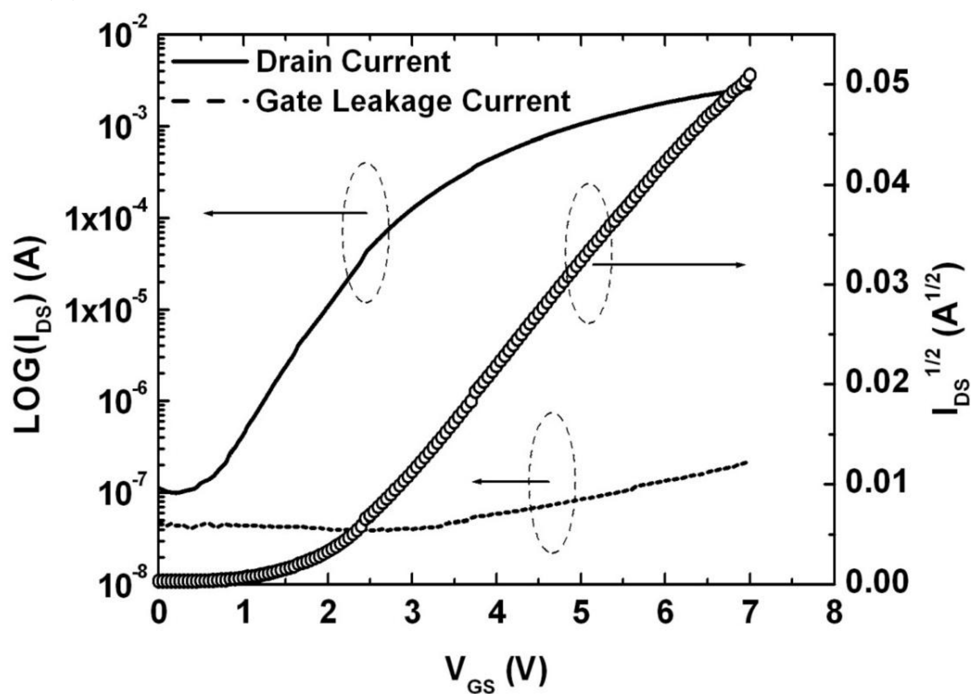


Figure 3.8 Electrical characteristics of the best ZnO-TFT subject to rapid thermal process in N_2. (a) I_{DS} - V_{DS} curves. (b) Log scale I_{DS} and I_{GS} as a function of V_{GS} at V_{DS}=20V, and the $(I_{DS})^{1/2}$-V_{GS} curve.

Chapter 4

Fabrication of ZnO TFTs on Plastic Substrates

4.1 Fabrication process

Fig. 4.1 schematically illustrates the structure of a ZnO-TFT on a plastic substrate in this work. As illustrated, a top-gate and staggered layout is adopted with the channel, gate insulator and gate having the same dimensions.

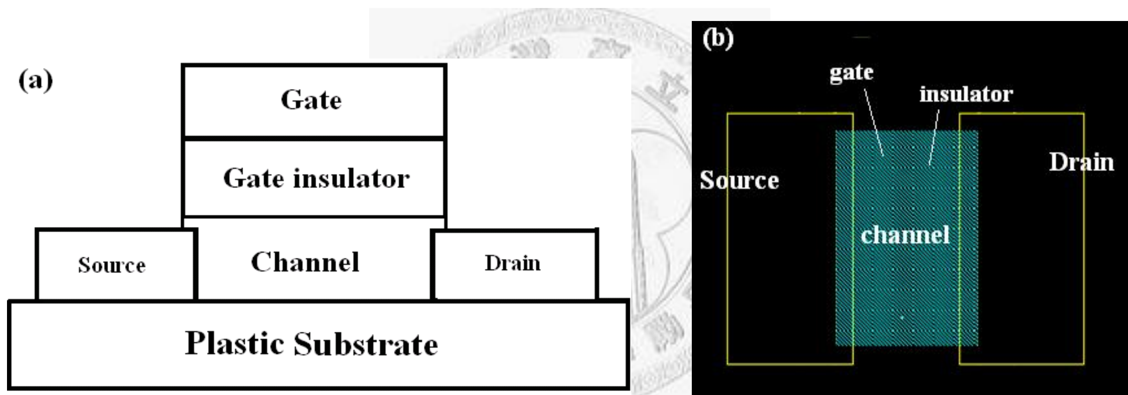


Figure 4.1 The structure of the ZnO-TFT on a plastic substrate. (a) A schematic cross-sectional view of TFT structure. (b) A perspective from top view.

Fig. 4.2 shows the flowchart of fabricating a ZnO-TFT on PET (polyethylene terephthalate) substrate. Based on the sophisticated processing developed in chapter 3, the processing for the flexible ZnO-TFT began with ultrasonic cleaning of the PET substrate in acetone and isopropanol successively, each for 10 minutes. Before growth of all thin-film layers, the PET substrate was spin-coated with SiO_2 sol-gel to

form planarization layer and then was heat-stabilized to enhance its operating temperature and meanwhile to dry out. The SiO_2 layer also helps adhesion of the ZnO channel layer. The source and drain regions were firstly defined by standard photolithography and then were deposited with *titanium* (Ti) at room temperature. Using Ti in substitution for transparent ITO is meant to improve the conductivity of the source and drain in that ITO deposited at room temperature would have a large resistivity which could give rise to an extremely low I_{DS}.

To avoid the deformation of the PET substrate, the deposition rate was kept relatively slower than 20nm/min which is the case in chapter 3. In addition, slower deposition rate could mitigate the particle bombardment for better polycrystalline quality. During the deposition, the wafer holder in sputter system was attached to a water running pipe to remove the generated heat, again helping avoid deformation of the PET substrate.

The second step of photolithography was introduced to define the channel region. After the deposition of the ZnO layer by RF magnetron sputtering in the presence of Ar and O_2, a SiO_2 layer as gate insulator was straightforward deposited onto ZnO layer since the SiO_2 layer and the ZnO layer were designed with the same dimensions. The gas flow ratio of Ar to O_2 was the same optimum as that in chapter 3. Finally, an ITO layer as gate electrode was also straightforward deposited onto the SiO_2 layer. In this way, the ZnO-TFT on the plastic substrate can be realized by only two-step photolithography so as to moderate the distortion of substrate. The channel width and length were 600 μm and 300 μm, respectively, yielding a width-to-length ratio of 2.

All thin-film layers of the ZnO-TFT on a PET substrate were deposited under room temperature.

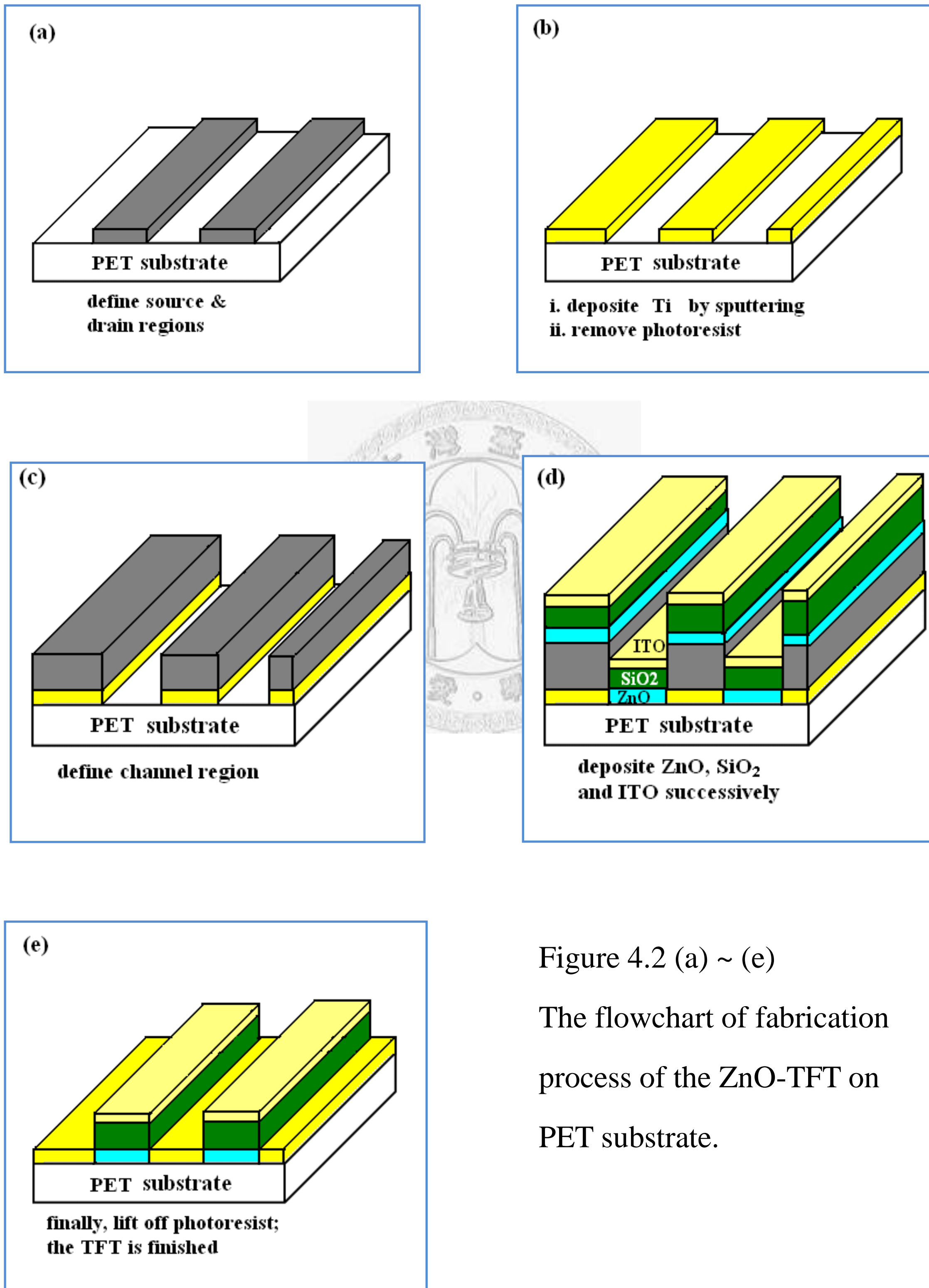


Figure 4.2 (a) ~ (e)
The flowchart of fabrication process of the ZnO-TFT on PET substrate.

4.2 Results and analysis

4.2.1 Using **ITO** as the source and drain

Fig. 4.3 shows the I-V curves of the ZnO-TFT on a PET substrate (labeled with “TFT-FS63”) with the source and drain using ITO deposited at room temperature. The analysis is as follows:

1. When the V_{DS} is in the interval of 0V to 3V, the I_{DS} is extremely small. This may be attributed to the ITO drain and source with large sheet resistances. The source and drain are not good conductors and reduce the current from the drain to the source.
2. When the V_{DS} is in the interval of 3V to 15V, the I-V curves are in the linear region.
3. When the V_{DS} is in the interval of 15V to 20V, the I-V curves tend to bend downwards but do not show a good saturated behavior. The I_{DS} is 70μA when V_{DS}=20V and V_{GS}=4V. The amorphous ZnO on a polymer substrate leads to smaller I_{DS}. The lattice mismatch is expected to be critical between organic (PET) and inorganic (ZnO) materials.
4. The ratio of I_{on} to I_{off} is calculated to be 10.

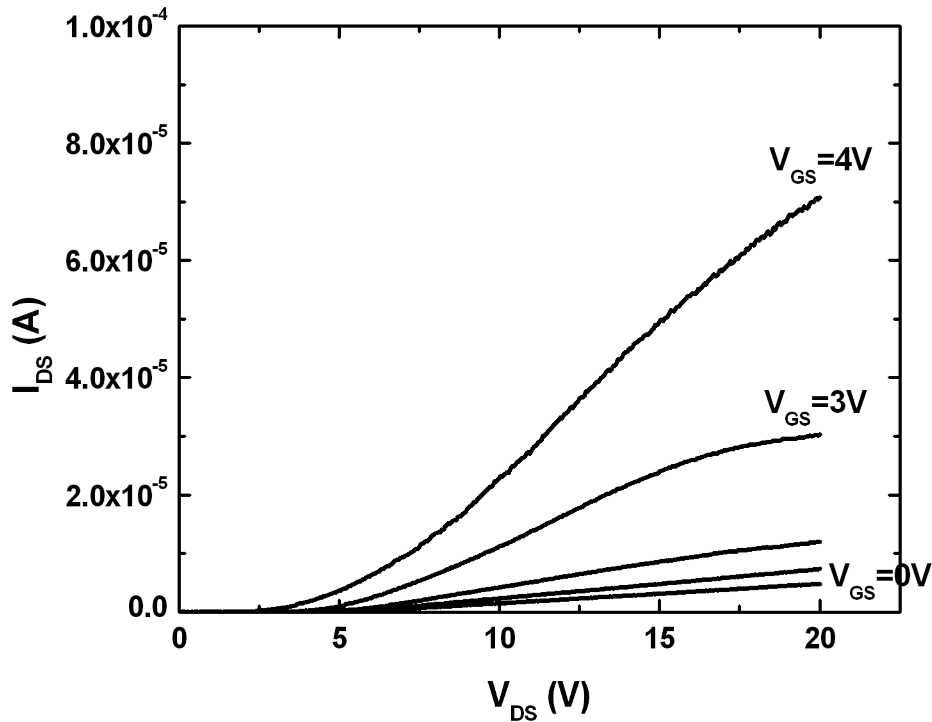


Figure 4.3 The I_{DS}-V_{DS} curves of the ZnO-TFT on a PET substrate, using ITO as the source and drain. The I_{DS} is 70μA when biased at V_{DS}=20V and V_{GS}=4V.

Fig. 4.4 shows the optical transmission spectra for the ZnO-TFT on a PET substrate in the wavelength range between 300 and 1400 nm. The average optical transmission of the entire TFT in the visible range of the spectrum is about 82% while the transmission at 550 nm (maximum sensitivity for human eyes) is 88%. The average optical transmission of the PET substrate in the visible part of the spectrum is about 89%, indicating 7% transmission losses resulted from the ZnO-TFT device.

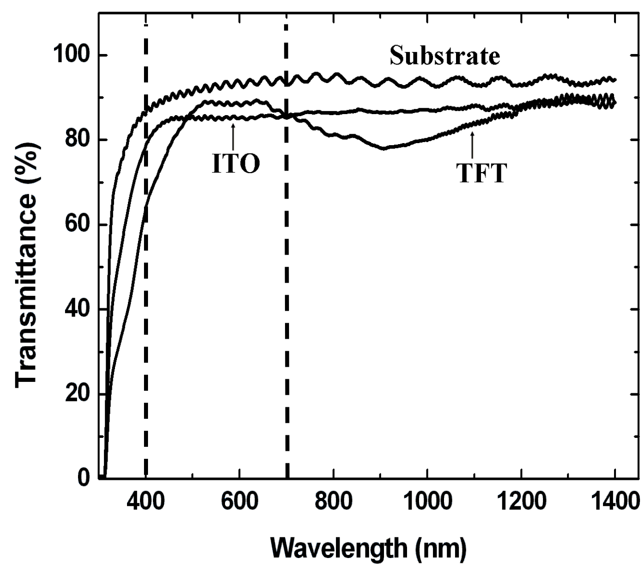


Figure 4.4 Transmittance as a function of wavelength for the ZnO TFT on a PET substrate.

4.2.2 Using **Ti** as the source and drain

Fig. 4.5 shows the I-V curves of the ZnO-TFT on a PET substrate (labeled with "TFT-FM63") with the source and drain using Ti deposited under room temperature. The analysis is as follows:

1. The I_{DS} in Fig. 4.5 is not as extremely small as that in Fig. 4.3 when the V_{DS} is in the interval of 0V to 3V. The empoly of metal Ti indeed reduces the sheet resistance of the source and drain. The source and drain are now good conductors and reduce the current from the drain to the source although the transparency is sacrificed.
2. When the V_{DS} is in the interval of 0V to 4V, the I-V curves are in the triode region.
3. When the V_{DS} is in the interval of 3V to 4V, the I-V curves tend to bend downwards and the I_{DS} starts to saturate; however, when the V_{DS} is above 8V, the I_{DS} fails to saturate. The I_{DS} is 50μA when V_{DS}=12V and V_{GS}=3V. The amorphous ZnO on a polymer substrate leads to smaller I_{DS}. The lattice mismatch is expected to be critical between organic (PET) and inorganic (ZnO) materials.
4. The ratio of I_{on} to I_{off} is calculated to be 5.

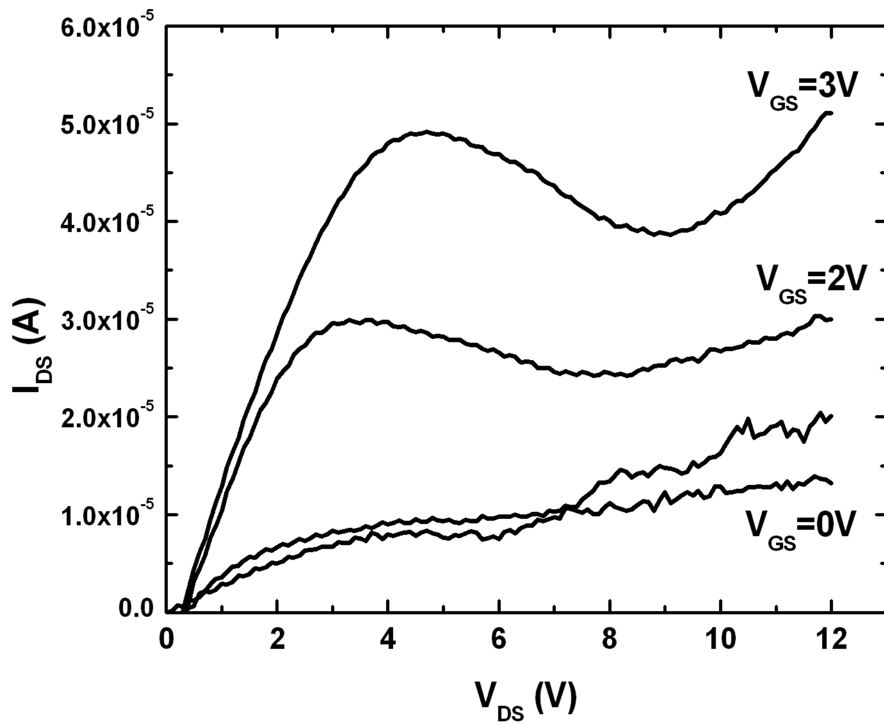


Figure 4.5 The I_{DS}-V_{DS} curves of the ZnO-TFT on a PET substrate, using Ti as the source and drain. The I_{DS} is 50μA when biased at V_{DS}=12V and V_{GS}=3V.

Chapter 5

Conclusions and Recommendations for Future Work

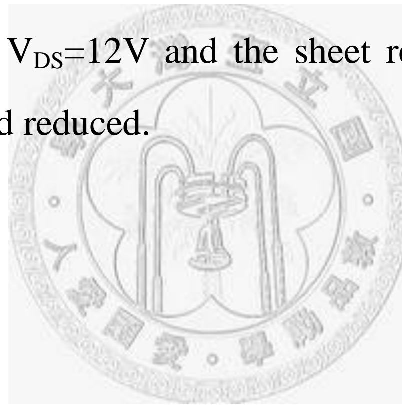
5.1 Conclusions

This thesis focuses on two parts of ZnO thin-film transistors, ZnO-TFTs fabricated on glass substrates and ZnO-TFTs fabricated on PET substrates. Conclusions related to these two parts are summarized as follows.

First, for glass substrate, the high-performance enhancement-mode ZnO TFT on a glass substrate is demonstrated. Before fulfilling the ZnO-TFTs on glass substrate, two methods (controlling gas flow ratio of Ar to O_2 and post-passivation by O_2 plasma) are employed to engineer the conductivity of ZnO thin films and the characteristics of ZnO thin films are examined by XRD and AFM measurements. The optimum condition for growing ZnO thin films helps carry out the high-performance ZnO-TFTs. Before contact alloy, the I_{DS} achieves as high as 1 mA when biased at the saturation region V_{DS} = 10-20 V and V_{GS} = 5 V. The I_{on}/I_{off} ratio is 3×10^6. The source and drain contacts are improved after 200˚C, 15-minute alloy. The slopes of I_{DS}-V_{DS} curves in the triode region are much more linear and the overshoot at the onset of saturation region is reduced. The fabrication steps developed and the ZnO TFTs performance in this work are suitable for AMLCD applications. It's believed that the results are among the best ZnO TFTs ever obtained.

Second, for polymer substrate, two kinds of ZnO-TFTs fabricated on

PET substrates at low temperature are demonstrated with ITO and Ti as the source and drain contacts, respectively. ITO is replaced by Ti to improve electrical performance whereas the trade-off is the transparency. All the patterns of the ZnO-TFTs on PET substrates are defined by only two steps of standard photolithography in order to reduce substrates' distortion. Using ITO as the source and drain contact, the I_{DS} is 70μA under a bias condition V_{GS}=4V and V_{DS}=20V while high sheet resistances exist in ITO layers. The average optical transmission of this TFT structure in the visible range of the spectrum is about 82% while the transmission at 550 nm is 88%. With Ti as the source and drain, the I_{DS} is 50μA under a bias condition V_{GS}=3V and V_{DS}=12V and the sheet resistances of source and drain contacts are indeed reduced.



5.2 Recommendations for future work

The purpose of this section is to summarize recommended directions of future work based on findings presented in this thesis.

1. More work should be undertaken to stabilize the performance of ZnO-TFTs on both glass and plastic substrates. Since the carrier transportation of undoped *n*-type ZnO mainly relies on the intrinsic "defects" such as oxygen vacancies and the defect concentration is accessible to ambient currents, the issues on the reliability and stability of ZnO-TFTs deserve furthermore investigation. ZnO doped with gallium and/or indium is a suggestion in that the "dopants" instead of defects serve as donors.
2. Device dimensions can be reduced. The work presented in this thesis utilized large device dimensions (hundreds of micrometers) to ease device fabrication. Layout optimization and decreasing device size can be deliberated for enhancing electrical performance.
3. The characteristics of polymer substrates deeply influence the performance of flexible ZnO-TFTs. Finding a polymer substrate with better surface morphology and higher glass transition temperature enables high-performance flexible ZnO-TFTs.
4. The interface states existing between the organic polymer substrate and the inorganic ZnO semiconducting layer constraint the operating current of flexible ZnO-TFTs. Methods of growing better polycrystalline ZnO on polymer substrates should be taken into account.

This work demonstrates the feasibility of ZnO-TFTs on glass and polymer substrates. Further work should be pursued to develop the viability of commercial industry. The era of transparent and/or flexible electronics turns out to be just around the corner.