國立臺灣大學電機資訊學院電信工程學研究所
碩士論文

Graduate Institute of Communication Engineering

College of Electrical Engineering & Computer Science

National Taiwan University

Master Thesis

毫米波多埠切換器與功率放大器之研製

Design of Millimeter-Wave Multiple-Port Switches and

Power Amplifier

賴瑞彬

Ruei-Bin Lai

指導教授: 王暉 博士

Advisor: Huei Wang, Ph.D.

中華民國 98 年 6 月

June, 2009

國立臺灣大學碩士學位論文
口試委員會審定書

毫米波多埠切換器與功率放大器之研製
Design of Millimeter-Wave Multiple-Port Switches and Power Amplifier

　　本論文係 賴瑞彬 君（R96942008）在國立臺灣大學電信工程學研究所、所完成之碩士學位論文，於民國九十八年六月二十七日承下列考試委員審查通過及口試及格，特此證明

口試委員：

_____（簽名）
　　　　　（指導教授）

_____　　_____

_____　　_____

_____

系主任、所長 _____（簽名）

致 謝

　　能夠完成這本論文，首先我要感謝我的指導教授，王暉老師。自大三下修了王老師的專題研究，至今共三年半的時間，我在王老師身上學到的不只是專業知識，更重要的是待人處世以及解決問題該有的方法與態度。除了在王老師身上學到的東西，也很感謝王老師一直以來給我機會參加研究、推薦我參加各種獎項，讓我在精神與生活上都能夠得到肯定與幫助。

　　同時要感謝的是，在我剛進入這個實驗室，給我指導良多的蔡作敏博士。蔡博士在學術上的熱忱、對實驗室的奉獻、個性上的耿直、對學問深入思索的態度，一直是我學習的榜樣。無論如何，蔡學長等同是我在研究上的啟蒙導師，我對他有無限的感激。

　　接著感謝我的口試委員，林坤佑教授、蔡作敏博士、張志揚教授、陳咨呁博士，感謝你們在口試時提醒我的不足之處，以及讓我深入思考研究上沒注意到的問題，使本論文得以更加完善。

　　此外我要感謝這個實驗室的同仁，包含了許多學長、同學。感謝陳重均學長，背負著畢業壓力，卻還是給我支援、協助我量測、在我不知所措時告訴我要把事情一件件完成。感謝趙世峰學長，沒有學長的幫助以及校稿，我無法完成多埠切換器的論文。感謝小郭(哲嘉)學長，學長總是很有條理的安排著和我量測的事情，讓我能夠如期的完成論文的進度。感謝紅郭(京霖)學長，學長總是很熱忱的幫助別人，用心思考別人遇到的問題，在量測上也不遺餘力的奉獻自己的時間給別人。感謝李杰穎學長，帶我進入這個實驗室，開始了我的研究生涯。感謝野口(陳仲豪)，和我一起進入這個實驗室，當初我們一起探索這個新世界。感謝我的實驗室同學好夥伴，超哥(林介安)、SOSO(高堃堯)、鄭伊佐、鬆餅(紀秉松)、冠哥(林士凱)、蔡宜倩、呂彥儒，我們一起經歷了這兩年研究與修課的歲月。也感謝其他電波組的好夥伴，我們時常一起打球、一起分享電波組的八卦及生活點滴，白羊(莊皓翔)、星星憨(楊星瀚)、藍洵、貓哥(謝易展)、豪哥(張家豪)、蕭偉成、香派(白英碩)、王澤宇、紀凱程。還要感謝辛苦的網

管，陳君朋學長，在我人生感到迷惑時給我提點。還有已經畢業的實驗室學長姐，小雷(雷明峰)、吳佩熹、老江(江昱嫻)。一起去亞特蘭大開會以及遊走東京的郭爸(哲均)、航航(翁榆航) 、爽年(任勇年)、黃智宇。感謝我的大學同學，無論在我傷心難過或是快樂時都給我支持，留級(劉佶)、小黃(翊鑫)、江媽(怡萱)、老大(王尚平)、海參(陳凱昇)、中國風(鐘國峰)、阿冗(曾鈺翔)、阿土(陳祥麟)。

還有我要感謝提供我在生活以及求學上補助的單位，陳安泰醫師在研究上給予我的肯定，行天宮在我碩二以後提供我定期的補助，讓我減輕在外租屋生活的壓力。細數之下，我要感謝的的人真的是太多了。

最後，我要感謝我的家人，感謝我的父母，在求學路上一直給予我支持，我常常因為壓力而在家庭產生負面的情緒，想想我真不是一個好孩子，總讓您們包容我；也感謝我的兩位兄長，有你們在，我才能安心的離開父母在外求學。

我還是得要感謝一個人，好燙(皓棠)，從大學到研究所，一共陪我經歷了四年的歲月。曾經，我們一起成長、一起歡笑、一起難過，我不是個成熟的人，總是讓妳受到委屈；感謝妳這四年的包容，因為有妳在，讓我安心地朝自己的目標前進，因為有妳，讓我在人生感到徬徨時而變得積極，也在我因為投入研究而與外界隔絕時還是陪在我身邊，雖然遺憾的是我們沒能夠走完這段路。希望我們再見面時，我們都能更加懂得愛與珍惜。

中文摘要

本論文包含毫米波單刀雙擲切換器、多埠切換器與中等功率放大器的研究。

本論文的第一部分說明射頻切換器的基本概念，進而展示兩個使用互補式金屬氧化半導體(CMOS)製程的毫米波單刀雙擲切換器。這兩個毫米波單刀雙擲切換器是使用濾波器整合的方式來設計。使用濾波器的方式來設計，不但可使切換器的濾波效果更顯著，也可以提升阻抗匹配以及較好的隔離度。使用互補式金屬氧化半導體製程是現今整合系統於晶片上的趨勢。本論文中的第一個單刀雙擲切換器使用65奈米CMOS製程，在40到80 GHz的頻率之間，其置入損耗的量測值在3至5 dB之間，而隔離度則優於20 dB。另一個單刀雙擲切換器係使用90奈米的CMOS製程製作，在60到110 GHz的頻率之間，其置入損耗的量測值在3至4 dB之間，而隔離度則優於25 dB；就我們所知，後者是目前最高頻的CMOS切換器。

本論文的第二部份提出一個方法去分析毫米波多埠切換器的架構。這個分析方法是將多埠切換器架構中的通道路徑做一個簡化模型來做數學分析，而此簡化模型也適用於分析任一種多埠切換器架構。本論文實現了兩個使用砷化鎵高速場效電晶體(GaAs HEMT) 60 GHz的多埠切換器來驗證此分析方法。實驗結果與分析相當吻合。

第三部份首先介紹微波功率放大器的基本設計步驟，然後研製了一個使用65奈米CMOS的60 GHz 中等功率放大器。此60 GHz功率放大器的最高增益為14.5 dB而飽和功率則為9.5 dBm.

Abstract

This thesis includes the design of millimeter-wave SPDT switches, multiple-port switches, and a medium power amplifier.

The first part of the thesis focuses on the basics about how to design RF switches, and then demonstrates two MMW SPDT switches in CMOS process. These two MMW SPDT switches were designed by filter-integrated method. To integrate a switch with filter response can get sharper frequency response and enhance isolation. The CMOS process was adopted since the system on chip (SoC) is a trend in CMOS. One SPDT switch was designed in 65 nm CMOS, and it has an insertion loss about 3-4.5 dB and an isolation better than 20 dB in 40-80 GHz. The other SPDT switch was designed in 90 nm CMOS, and it has an insertion loss of 3-4 dB and isolation better than 25 dB in 60-110 GHz. To our knowledge, it is the highest frequency CMOS MMIC switch.
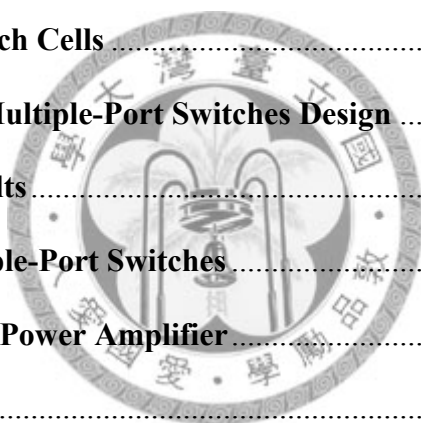
The second part presents a new method to analyze the topology of MMW multiple-port switches. The proposed method is suitable to analyze arbitrary multiple-port switch topology. This method is based on a simplified model of a through path of a multiple-port switch topology. Two 60 GHz multiple-port switches in GaAs HEMT process are demonstrated to verify this analysis. Good agreement with the analysis and the measured results are achieved.

The third part presents a 60-GHz medium power amplifier in 65 nm CMOS process. This PA demonstrates a peak gain of 14.5 dB and saturation power of 9.5 dBm.

Contents

List of Figures

List of Tables

Chapter 1 Introduction

1.1   Motivation

The developments of millimeter-wave communication systems have increased rapidly in recent years. To realize the wider bandwidth and higher data rate, performance of components of the RF front end should be enhanced as well. Switches control the signal path of wireless transceivers and should have enough power handling to transmit the output power from the power amplifier to transmission channel. Besides, to integrate a system on chip (SoC), the design using CMOS process is a trend. Therefore, the design of power amplifier in CMOS is also an important topic.

A beamformer system using multiple antennas both at the transmitter and receiver can improve the efficiency of the spectrum greatly by spatial multiplexing [17]–[20]. In a beamformer system, the design of the multiple-port switch is important.

Power amplifiers using GaAs HEMTs can achieve high performance, but it is difficult to integrate GaAs-based components with baseband circuits. Higher-level integration of wireless transceiver is a trend. CMOS process is suitable and high-level integration on chip. However, nanometer CMOS with lower breakdown voltage causes the poor power handling capability of the device.

Researches about multiple-port switches and CMOS power amplifiers are conducted in this thesis.

1.2   Literature Survey

This literature surveys including radio frequency switches and MMW power amplifiers.

1.2.1 Radio Frequency Switches

RF switches are important components in the wireless communication systems. To design RF switches below 20 GHz, the series or series shunt switches [21] are suitable. Besides, power performance of RF switches are important, since the RF switches should have enough power handling capability to transmit the signal from power amplifiers. In higher frequency, the output power of power amplifiers is usually below 20 dBm, and hence, the power performance of MMW switches is not difficult to achieve.

To achieve the design around 20 GHz, one might use inductors to cancel the parasitic capacitance at desired frequency, but it also leads to a narrow band characteristics. Switches using traveling concept can achieve broadband characteristics [25]. Switches using impedance transformation technique [27] can achieve better isolations, but they cause more insertion loss, and the more insertion loss will make the noise figure of receivers increase and attenuate the output power of transmitters. Filter-integrated switches [31]-[32] can achieve better performances such as better return losses, isolations, and sideband rejection for the undesired bands.

Table 1.1

SUMMARY OF THE PERFORMANCE AND FEATURES FOR PREVIOUSLY REPORTED PASSIVE

HEMT MMIC SWITCHES

Technology	Design Approach	Frequency (GHz)	Insertion Loss (dB)	Isolation (dB)	I/O	Ref.
HEMT	Resonant, series	94	1.6	22.5	SPST	[28]
HEMT	Resonant, series	55 ~ 63	< 3.2	>23	SPDT	[29]
HJFET	Series resonant, shunt	57 ~ 61	3.9 ~ 5	>30	SPDT	[30]
HEMT	λ/4, shunt	42 ~ 46	< 1.6	>30	SPDT	[33]
HEMT	Impedance transformation network, shunt	53 ~ 61	< 4	>30	SPDT	[27]
HEMT	Traveling wave concept	70 ~ 102	3.9 ~ 5.5	>30	SPQT	[34]
HEMT	Series	1 ~ 6	1.2 ~ 1.7	>20	Multiple-port	[39]
HEMT	Filter-integrated	38 ~ 42	< 4	>25	Multiple-port	[43]

Table 1.1 summarizes the previously reported performances and features of passive MMIC HEMT switches. There are few researches about multiple-port switches 10 GHz [39], because the simply shunt-series switch cell can still function well in this frequency range. To design MMW multiple-port switches, there are many constraints due to the high frequency characteristics. Resonant-type SPDT switch shows a narrow band in the *V*-band [29], and another SPDT switch shows an insertion loss of 4 dB [30].

1.2.2 Millimeter-Wave Power Amplifiers

CMOS power amplifier is a hot research topic in these years since it is still the bottleneck for the integration of a wireless transceiver. In past years, people use GaAs process to achieve high power performance in MMW frequency. Compared with GaAs process, the higher loss on silicon substrate, low supply voltage, and poor power handling capability make the design of power amplifier in CMOS a big challenge. Besides, the behavior of passive elements in CMOS process cannot be predicted precisely. The reported 60-GHz power amplifiers are summarized in table 1.2. Power amplifiers in [48] and [50] show poor gain and the poor gain will make the power amplifiers difficult be used in practical wireless transceivers. The power amplifier in [51] has a gain less than 10 dB regardless of an output power of 10 dBm. The power amplifier in [52] has a gain better than 10 dB but only has an output power of 6 dBm. Power amplifiers in [54] and [55] both shows a gain better than 20 dB and a saturation power better than 10 dBm, but theses two power amplifiers consume a great quantity of power.
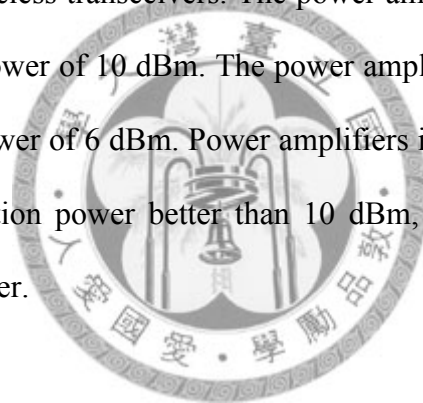
1.3   Contributions

In this thesis, the first filter-integrated SPDT switch using CMOS process is implemented. The high insertion loss due to silicon substrate is the challenge in the design of CMOS switches. A 60-GHz SPDT FIS in 65 nm CMOS process is implemented first and it has a size of 0.25 mm by 1.5 mm. This SPDT switch has an insertion loss of 3 dB at 60 GHz, and its isolation is about 23 dB. Furthermore, a 60 to 110 GHz SPDT FIS in 90 nm CMOS is also demonstrated. It has an insertion loss less than 4 dB and an isolation better than 25 dB in 60-110 GHz.

Table 1.2

SUMMARY OF THE PERFORMANCE OF REPORTED 60-GHZ POWER AMPLIFIER IN CMOS

PROCESS

Process	Topology	DC Biasing	V_{ds}	Frequency (GHz)	Power Gain (dB)	Saturation Power(dBm)	Ref.
65 nm CMOS	1-stage, CS	23mA, 1.2V	1V	62	4.5	9	[48]
90 nm CMOS	3-stage, CS	26.5mA, 1.5V	1.5V	60	4.7	9.3	[50]
90 nm CMOS	2-stage, CS	23mA, 1V	1V	57	9.8	10	[51]
90 nm CMOS	2-stage CC, 1-stage CS	30mA, 1.5V	1.5V	60	14	6	[52]
90 nm CMOS	3-stage cascode	100 mA, 1.8V	0.9V	60	30	13.8	[54]
90 nm CMOS	DAT combing + 3-stage, cascode	153 mA, 1.8V	0.9V	60	26	14.5	[55]

The second part of this thesis is the topic of topology analysis and design of multiple-port switches in GaAs PHEMTs. GaAs HEMTs have good power handling capability and the loss of GaAs substrate is relatively lower than CMOS process, and therefore, GaAs HEMTs are suitable to

be used for the multiple-port switch. An approach to analyze arbitrary topologies of multiple-port switch is proposed, and an analytic expression of the insertion loss, isolation, and bandwidth of each topology can be derived by this proposed approach. In this thesis, two multiple-port switches are demonstrated. The first one is composed of distributed switch cells, and the other is composed of filter-integrated switch cells. The cell based on the distributed type should have wider bandwidth than filter-integrated switch cells. However, from the experimental results, the multiple-port topology using filter-integrated switch cells has wider bandwidth than the multiple-port topology using distributed type. This can also validate the proposed analysis. The proposed analysis makes the conclusion that the limitation of multiple-port switches is determined by its topology, since the limitation of the topology of the multiple-port switch with distributed switch cells has narrower bandwidth. Two designs are presented in this thesis. The first multiple-port switch is formed by the net type topology and based on distributed switch cells. It has a size of 2.0 mm by 1.5 mm. The insertion loss is about 4-5 dB in 48-65 GHz, and its isolation is better than 25 dB. The other multiple-port switch is formed by the ring-binary topology and based on filter-integrated switch cells. It has a size of 2.5 mm by 2.0 mm. The insertion loss is about 3-4.5 dB in 43-66 GHz, and its isolation is better than 30 dB. Both multiple-port switches have input P_{1dB} better than 17 dBm due to the limitation of our power source under measurement.

The third part is a 60 GHz power amplifier in 65 nm CMOS process. This power amplifier was designed based on cascading three stages of cascode amplifiers. This power amplifier has a size of 0.55 mm by 0.64 mm. It has a peak power gain of 14.5 dB at 57 GHz and a gain better than 10 dB in 51-61 GHz. The saturation output power is 9.5 dBm at 57 GHz.

1.4 Organization of the Thesis

This thesis is organized as follows:

In chapter 2, some basic switch design approaches and the principles of switches from low frequency to MMW frequency are summarized.

In chapter 3, the basic theory about microwave filters are introduced. From the filter composed of basic lumped elements to transmission lines. After that, the concept of combination of transmission lines and switches is introduced. Finally, a SPDT switch in 65 nm CMOS and SPDT switch in 90 nm CMOS are demonstrated.

In chapter 4, the analysis of different multiple-port switch topologies is conducted.

In chapter 5, the experiment of two multiple-port switches is conducted to verify the analysis in chapter 4.

In chapter 6, a 60-GHz power amplifier in 65 nm CMOS process is demonstrated.

Finally, the conclusion of this thesis is drawn in chapter 7.
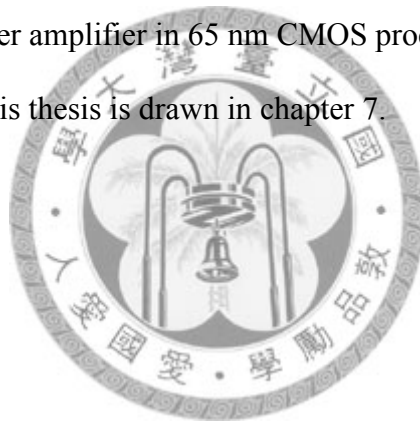
Chapter 2 Basics of Radio Frequency Switches

2.1   Introduction [21]-[23]

Radio frequency (RF) switch plays a key role in wireless transceivers. As shown in Fig. 2.1, RF switches control the path that a transceiver transmits or receives RF signals. Switches have two mainly concerned specifications: insertion loss and isolation. A switch with good insertion loss would not attenuate signals too much. A switch with good isolations can block signal leakage from transmitter to receiver.

For single-pole-double-throw (SPDT) switches terminated with Z_0 as in Fig. 2.2, the input impedance of the through-state path should be

$$Z_{Thru} = Z_0 \tag{2.1}$$

Besides, the input impedance of the isolated path should satisfy

$$Z_{ISO} \rightarrow \infty \tag{2.2}$$
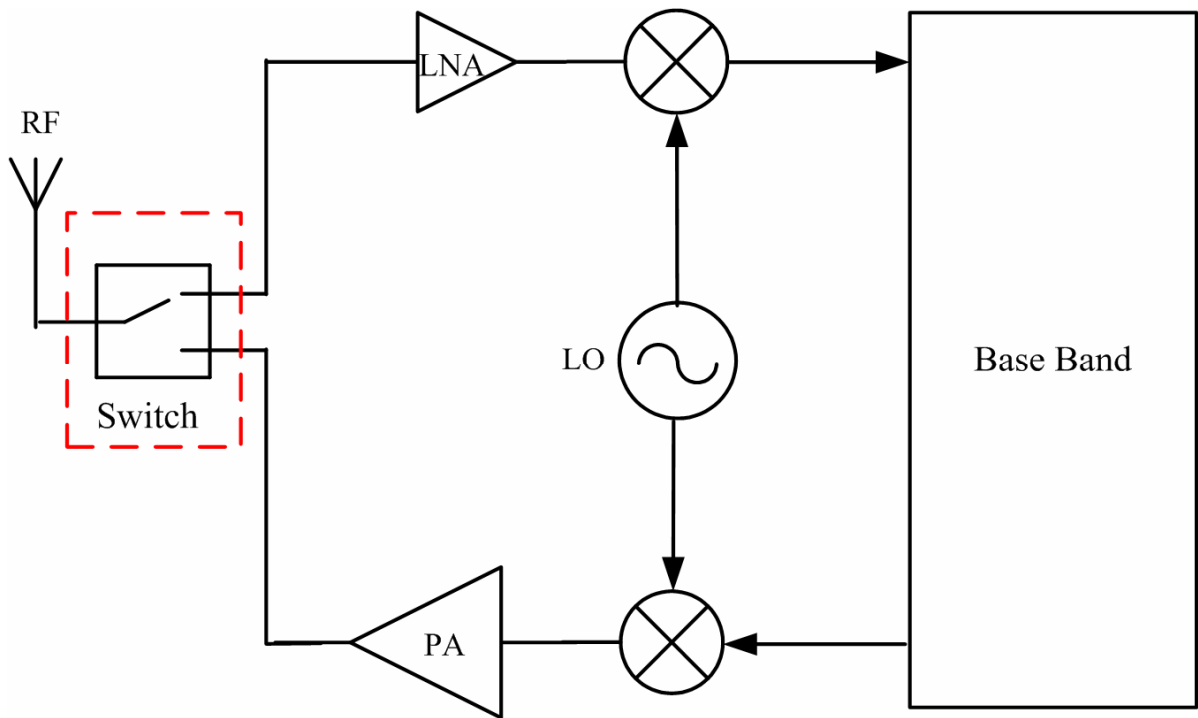
Fig. 2.1. Typical BPSK RF transceiver.
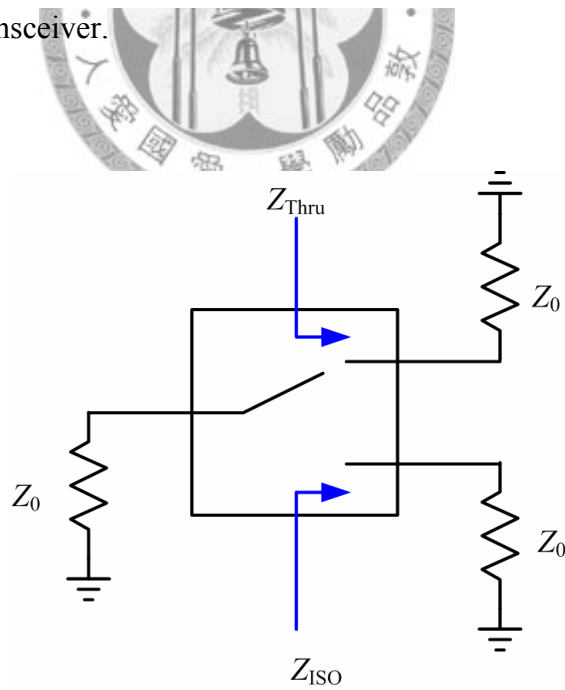
Fig. 2.2. A SPDT switch terminated with Z_0.

Eq. (2.1) means that the through-state path transfers maximum power from the input port to through port, and Eq. (2.2) means that infinite impedance is required to block signal leakage to the isolated port. It should be noted that it is infinite impedance instead of low impedance. If the isolated path is composed of low impedance technique such as shunt transistors, there should be an impedance transformer to transform low impedance to high impedance, for example, quarter-wave length transmission lines. This concept is important and will be used in following sections.

2.2   Series-Shunt Switches [21]-[23]
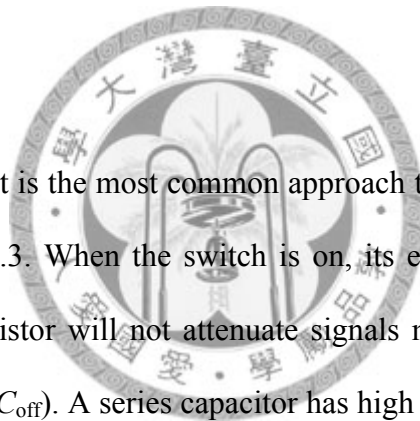
Series, shunt, or series-shunt is the most common approach to design RF switches. A common series switch is shown in Fig. 2.3. When the switch is on, its equivalent circuit is a series small resistor (R_{on}), and this small resistor will not attenuate signals much. When the switch is off, its equivalent circuit is a capacitor (C_{off}). A series capacitor has high pass characteristic, and thus it can block low frequency signal effectively. However, when the frequency goes higher, the isolation of the series switch degrades significantly.

A common shunt switch is shown in Fig. 2.4. When the switch is on, its equivalent circuit is a shunt capacitance (C_{off}), and this shunt capacitance has a low pass characteristic. As the operating frequency goes higher, the shunt impedance goes lower, and this makes high frequency signals leaks to ground. When the shunt switch is off, its equivalent circuit is a shunt resistor (R_{on}). This shunt resistor is of low impedance, and it drags signals to ground for isolation.
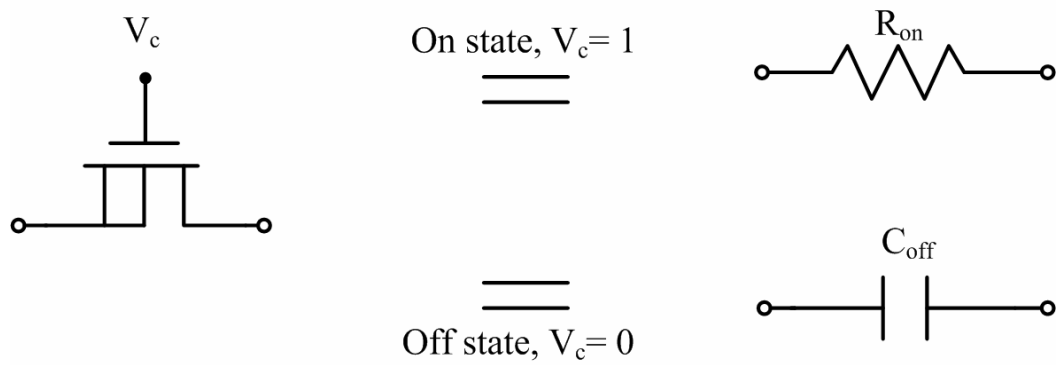
Fig. 2.3. Series switch and its equivalent circuit.
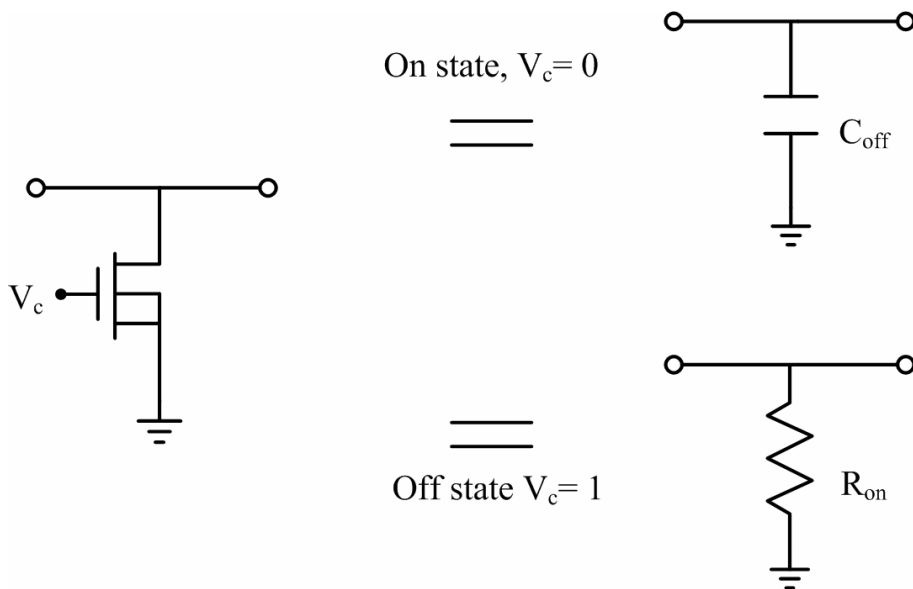
Fig. 2.4. Shunt switch and its equivalent circuit.

A series-shunt switch is shown in Fig. 2.5. It is a combination of series switch and shunt switch. When this series-shunt switch is off, both the series capacitor and shunt resistor enhance isolation much better. On the other hand, when the switch is on, the switch has more loss than the above mentioned switches. Regardless of this drawback, this kind of switch improves isolation greatly and thus it is much more useful in RF transceivers. Furthermore, the 3-dB bandwidth of this series-shunt switch locates at

11
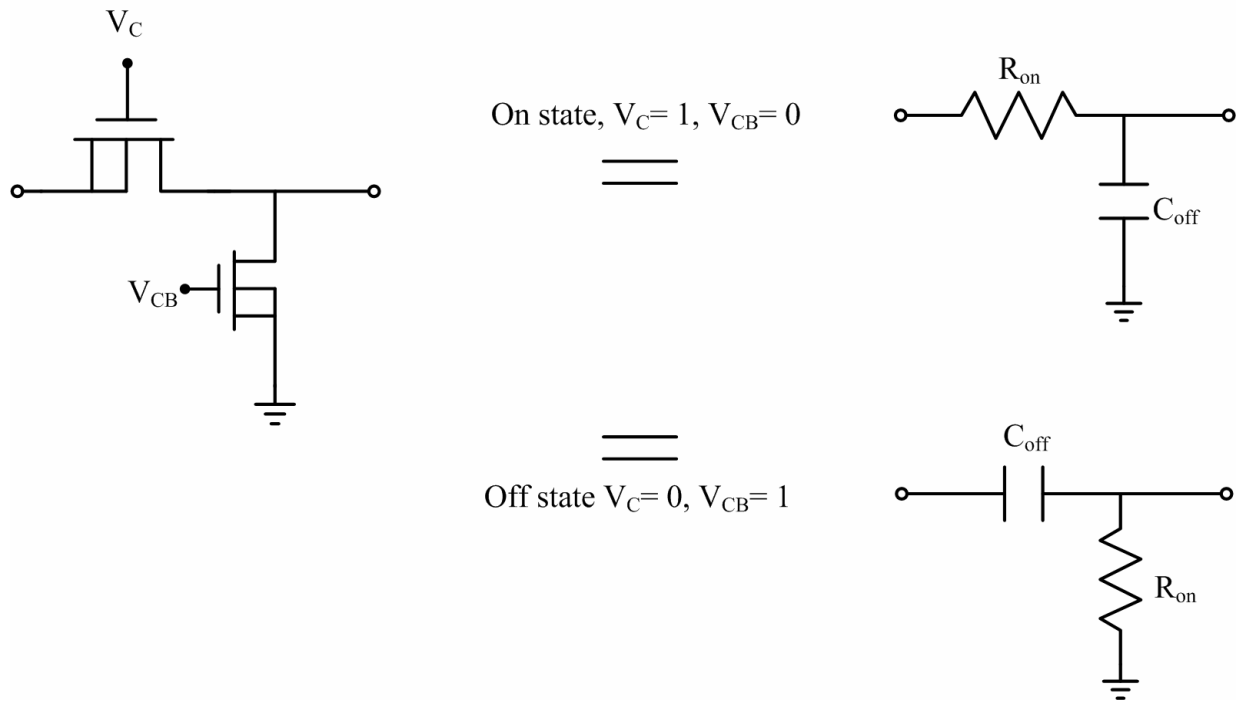
Fig. 2.5. A series-shunt switch, and its equivalent circuit.

$$f_{3-dB} = \frac{1}{2\pi R_{on} C_{off}} \tag{2.3}$$
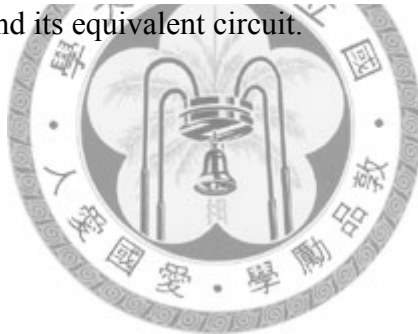
All the mentioned switches in this section are used for low frequency. The following sections introduce switched used in microwave or MMW frequency range.

2.3 Resonant-type Switches [28]-[30]
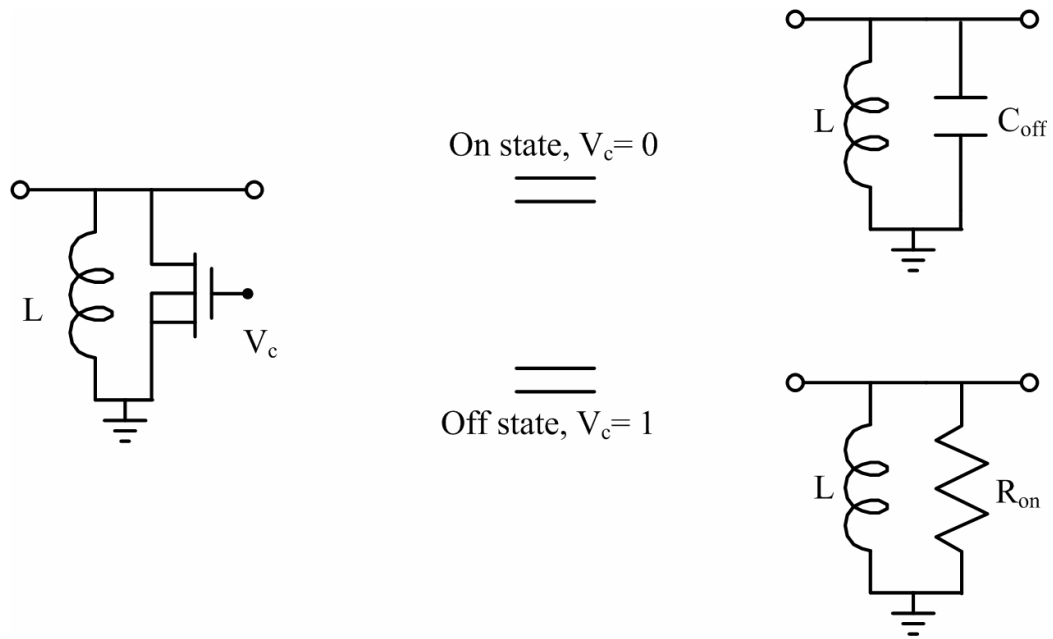
Fig. 2.6. Shunt type of a parallel resonator using a transistor.
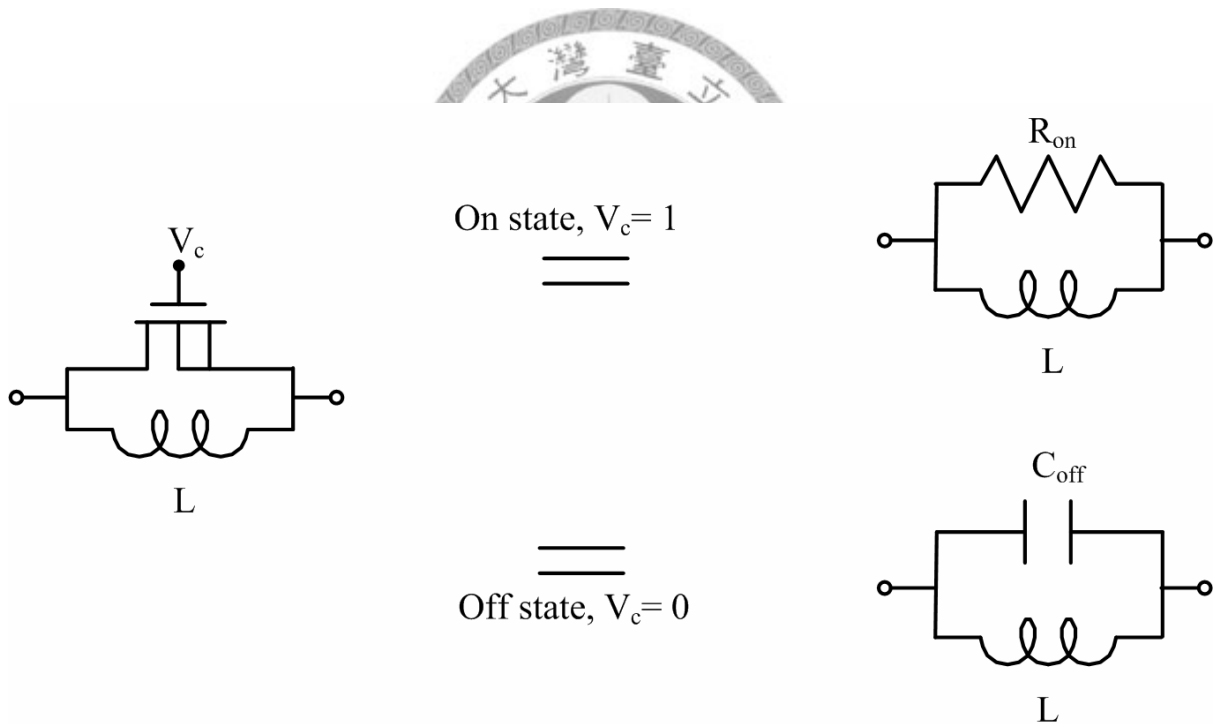
Fig. 2.7. Series type of a parallel resonator using a transistor.

Resonant-type switches are one of the most popular switches in microwave or MMW frequency range. There are two commonly used resonant-type switches: one is to shunt a parallel resonator as in Fig. 2.6 and the other is to series a parallel resonator as in Fig. 2.7. A typical parallel

resonator is composed of one inductor parallel with one capacitor. When a transistor is off, it behaves like a capacitor, and we can use this capacitive characteristic to shunt an inductor to compose a parallel resonator as in Fig. 2.6 and Fig. 2.7.

These resonant-type switches can operate at any center frequency

$$f_0 = \frac{1}{2\pi L C_{off}} \tag{2.4}$$

However, there must be some constraints. First, the value of C_{off} has a certain range in each process. Besides, there is certain range of the value of inductors in practical design.

2.4   Distributed Switches [25]

Distributed switches are one of the most commonly used techniques because the characteristic of broad bandwidth. A distributed cell is shown in Fig. 2.8. When it is at on state, the transistor can be modeled as a capacitor. Therefore, the series L and the shunt C_{off} form an artificial transmission line. To make a through-state path, this artificial transmission line should be operated with characteristic impedance of Z_0.

$$Z_0 = \sqrt{\frac{L}{C_{off}}} \tag{2.5}$$

It can be noticed that if the value of inductors and the value of capacitors do not change with frequency, this through state can operate with infinite bandwidth. When the transistor is on, it
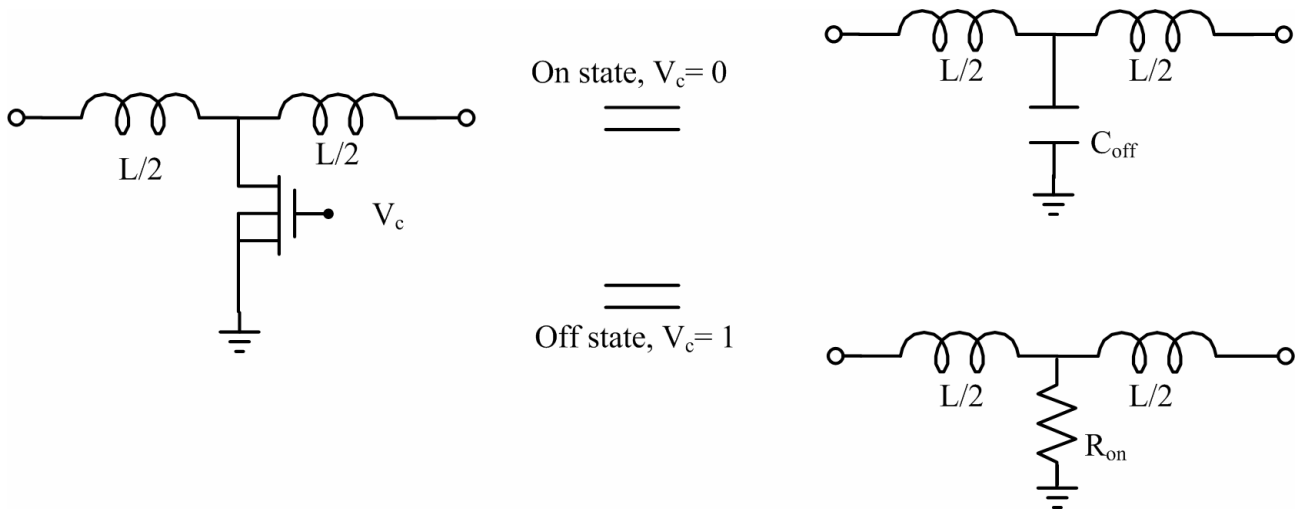
Fig. 2.8. A distributed switch and its equivalent circuit.

behaves like a small resistor. Therefore, the signal is pull to ground. To form a SPDT switch or a multiple-port switch, there must be one impedance transformer such as a quarter-wavelength transmission line before this isolated path, and the bandwidth of this impedance transformer is the limit of the bandwidth of a SPDT switch or a multiple-port switch.

Besides, there is a bandwidth limitation of a realized inductor because of self-resonant frequency. In MMW circuit design, a transmission line with high characteristic impedance Z_c and electrical length of θ can behave like an inductor, and thus, inductors in Fig. 2.8 can be replaced by a transmission line which satisfies

$$\frac{L}{2} = Z_c \tan \theta \tag{2.6}$$

Although θ changes with frequency to make the limitation of bandwidth, the bandwidth of switches composed of transmission lines is usually enough in realistic application.

15

Chapter 3 Millimeter-Wave Filter-Integrated SPDT Switch

3.1   Introduction

MMW SPDT switches are one of the key components in RF front end. Low insertion loss, high isolation, and required power handling are important characteristics of a switch. Besides, in a communication system, a filter is often necessary to filter unwanted band. A switch and a filter can be merged into one single circuit [1]. This concept is used to design a 60-GHz SPDT switch in 65nm technology.

This chapter first introduces some kinds of microwave filters, and then the theory of filter-integrated switches is introduced. Finally, a V-band SPDT switch using 65nm CMOS technology and a 60-110GHz SPDY switch using 90 nm CMOS technology will be presented.

3.2   Basic Concepts of Filter-Integrated Switches [15]

This section is composed of three subsections to let readers understand the principle of filter-integrated switches easier.

3.2.1 Synthesis of Microwave Filters [2]-[3]

Microwave filters can be composed of T-sections of *L-C*, or π-sections of *L-C*. By cascading more T-sections or π-sections to synthesize a microwave filter, the sharper frequency response can be achieved to reject undesired band better. Some specific values of *L-C* can synthesize specific types of filters, such as Chebyshev filters or maximally flat filters. Chebyshev filters are also called equal ripple filters, because the transmission coefficient of them has equal ripple in desired band. The transmission coefficient of maximally flat filters is flat in its desired band. Besides, Chebyshev filters have sharper frequency response than maximally flat filters.

Low pass prototypes of microwave filters are shown in Fig. 3.1. Fig. 3.1(a) is a prototype of low pass filter, and it begins with a shunt capacitor. Fig. 3.1(b) is another prototype of low pass filter, and it begins with a series inductor. We denote the *L* and *C* in Fig. 3.1 as L_k and C_k, respectively. The values of L_k and C_k can be found by tables in microwave engineering books or microwave filter books such as [2],[3]. For a low pass filter, the design value of indeed inductor and capacitor can be found by

$$L_k' = \frac{R_0 L_k}{\omega_c} \tag{3.1}$$

$$C_k' = \frac{C_k}{R_0 \omega_c} \tag{3.2}$$

ω_c is the cutoff frequency and R_0 is the referenced impedance. Both ω_c and R_0 are given by the designer. Therefore, the designers only have to decide the order of the filter, cutoff frequency, and referenced impedance, and then the design of a low pass filter is finished.
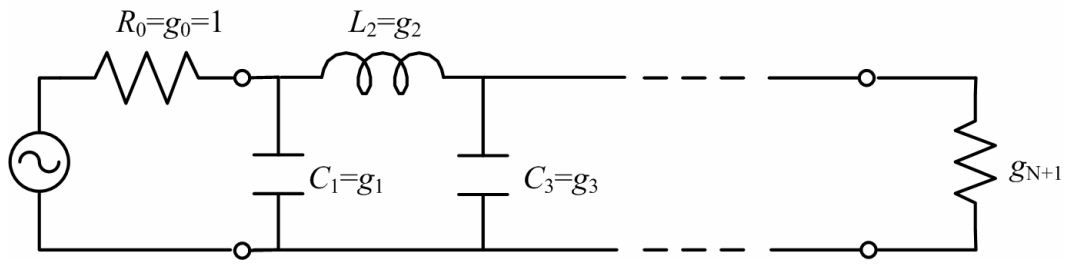
(a)
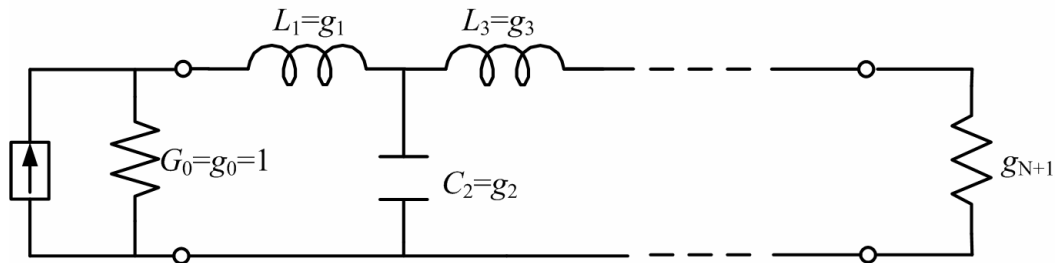
(b)

Fig. 3.1. Basic prototypes of low pass filters. (a) Prototype beginning with a shunt element. (b) Prototype beginning with a series element.

The design procedure described above can be also used to high pass filters and low pass filters by some transformation. For high pass filter, frequency ω should be substituted by $-\omega_c/\omega$. By doing so, the inductor in the prototype of a low pass filter will be replaced by a capacitor, and the capacitor will be replaced by an inductor.

For band pass filter, frequency ω should be substituted by $\dfrac{\omega_0}{\omega_2 - \omega_1}\left(\dfrac{\omega}{\omega_0} - \dfrac{\omega_0}{\omega}\right)$, where ω_0 denotes the center frequency and ω_0 is the arithmetic mean of ω_1 and ω_2. By using the above relationship, this will make the inductor in low pass prototype replaced by an inductor series with a
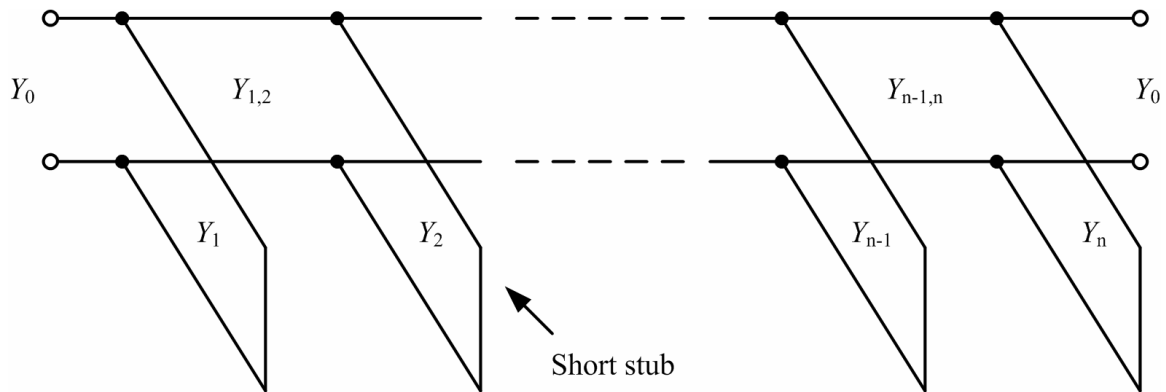
Fig. 3.2. A band pass filter composed of quarter-wavelength transmission lines.

capacitor, and the capacitor in low pass prototype replaced by a capacitor parallel with an inductor.

3.2.2 Transmission Line Integrated Filters [6]

In microwave frequency, the behavior of a transmission line can be viewed as an inductor or capacitor upon the length and termination. Therefore, there must be a transformation of transmission lines with inductors or capacitors. According to the previous subsection, the proper value of inductors and capacitors can form a microwave filter, and hence, proper transmission lines can similarly form a microwave filter. A transformation called Richard's transformation [3] can be used to prove the above described contents.

A microwave filter composed of shorted quarter-wavelength transmission lines will be introduced in this section. This kind of filter can be synthesized by short-circuited stubs of quarter-wavelength

Short-circuited stubs of quarter-wavelength replace the shunt element in Fig. 3.1(a), and series quarter-wavelength transmission lines replace the series elements in Fig. 3.1(a). Fig. 3.2 is the

transmission line integrated filter, and the lengths of all the transmission lines are quarter-wavelength.

$$\theta = \frac{\pi}{2}\left(1 - \frac{FBW}{2}\right)$$

$$h = 2$$

$$\frac{J_{1,2}}{Y_0} = g_0 \sqrt{\frac{hg_1}{g_2}}$$

$$\frac{J_{n-1,n}}{Y_0} = g_0 \sqrt{\frac{hg_1 g_{n+2}}{g_0 g_{n-1}}}$$

$$\frac{J_{i,i+1}}{Y_0} = \frac{hg_0 g_1}{\sqrt{g_i g_{i+1}}} \quad \text{for } i = 1 \text{ to } n-1$$

$$Y_1 = g_0 Y_0 \left(1 - \frac{h}{2}\right) g_1 \tan\theta + Y_0 \left(N_{1,2} - \frac{J_{1,2}}{Y_0}\right)$$

$$Y_n = Y_0 \left(g_n g_{n+1} - g_0 g_1 \frac{h}{2}\right) \tan\theta + Y_0 \left(N_{n-1,n} - \frac{J_{n-1,n}}{Y_0}\right)$$

$$Y_i = Y_0 \left(N_{i-1,i} + N_{i,i+1} - \frac{J_{i-1,i}}{Y_0} - \frac{J_{i,i+1}}{Y_0}\right) \quad \text{for } i = 2 \text{ to } n-1 \tag{3.3}$$

$$Y_{i,i+1} = Y_0 \left(\frac{J_{i,i+1}}{Y_0}\right) \quad \text{for } i = 1 \text{ to } n-1$$

, where FBW is the ratio of bandwidth to center frequency.

Eq. (3.3) is very useful to synthesize a filter of quarter-wavelength transmission lines. The designer only has to decide FBW and calculate the value of characteristic admittance of each stub, and then the design of a filter is finished.
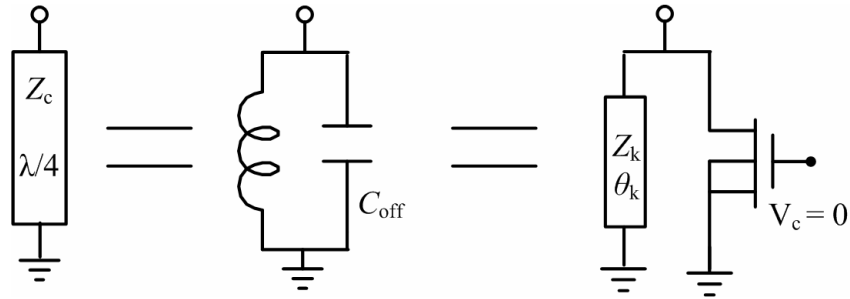
Fig. 3.3. Equivalent circuit of a shunt quarter-wavelength transmission line, it can be further synthesized with an off-state transistor.
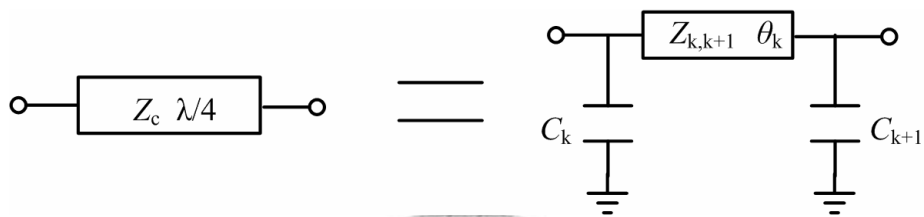
Fig. 3.4. Equivalent circuit of a series quarter-wavelength transmission line.
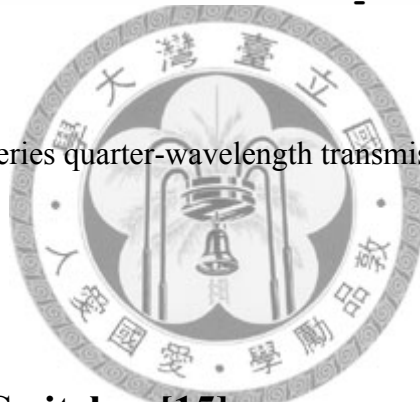
3.2.3 Filter-Integrated Switches [15]

The concept of filter-integrated switches was developed in [1]. Furthermore, the reduced-size version is further studied in [4]. The design principle of filter-integrated switches is based on the filter of quarter-wavelength short stubs. Since each quarter-wavelength short stub can be modeled as one inductor parallel with a capacitor near the center frequency of quarter-wavelength as in Fig. 3.3. Therefore, the shunt quarter-wavelength short stub can be replaced by an off-state transistor parallel with one high impedance ($Z_k > Z_c$) short stub whose length is shorter than quarter-wavelength. Furthermore, since the equivalent circuit of one series quarter-wavelength transmission lines can be modeled as one two shunt capacitors with one series high impedance

transmission line less than quarter-wavelength as in Fig. 3.4 [5]. Therefore, the reduced-sized version of filter-integrated switches can be designed by combining the equivalent shunt C_k and C_{k+1} into the off-state transistors. Hence, the electrical length of series transmission lines can be reduced.

3.3 Circuit Implementation of V-band Filter-Integrated SPDT Switch in 65 nm CMOS Process

Before designing an RF switch, the choice of technology is considered first. The performance of the switch implemented in different processes is mainly dependent on the resistance of on-state transistor and the capacitance and resistance of off-state transistor. To compare the technologies fairly, the device size of each process is chosen to have the same resistance of the on-state transistor. Therefore, the process with smaller capacitance and larger resistance of off-state transistor is the one can operate higher frequency and can achieve better performance for the design of switches. The input impedance of on-state and off-state transistors for 0.18 μm, 90 nm, and 65 nm CMOS are shown in Fig. 3.5. To achieve the on-state resistance the same for each process, the total gate width of the NMOS of 0.18 μm CMOS is chosen as 96 μm, the total gate width of the NMOS of 90 nm CMOS is chosen as 60 μm, and the total gate width of the NMOS of 65 nm CMOS is chosen as 88 μm. On this condition, the value of off-state capacitance at 60-GHz is 68.1 fF, 43.3 fF, and 39.5 fF for 0.18 μm, 90 nm, and 65 nm CMOS, respectively. If the switch is designed to operate at the same center frequency with the same isolation, the process with longer gate length will provide the insertion loss with narrower bandwidth due to the larger off-state capacitance in longer gate length process. Besides, it can be seen from Fig. 3.5(b) that the resistance of the off-state NMOS for each

process is very close to each other, and this means that the loss of switches in each process will be dominated by the loss of passive components such as inductors and thin-film microstrip lines. Furthermore, realized inductors and thin-film microstrip lines can only operate below their self-resonant frequency, and the self-resonant frequency is dependent on each process. For a switch operating at 100 GHz, the self-resonant frequency of passive components of the corresponding process should be higher than 100 GHz.

Fig. 3.6 shows the schematic of the designed 60-GHz SPDT switch. This switch is based on the filter-integrated type. All the transmission-lines in Fig. 3.6 are thin-film microstrip lines. The series-shunt approach only functions well in low frequency. The resonant approach can be used in MMW frequency, but it can only cover the band near the center frequency. Although distributed switches have the broadest bandwidth, it is necessary to shunt more transistors than the filter-integrated type, and hence it causes more insertion loss.
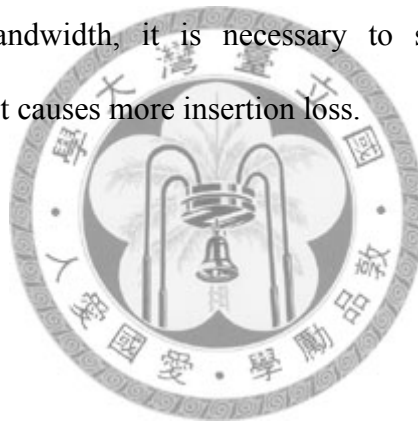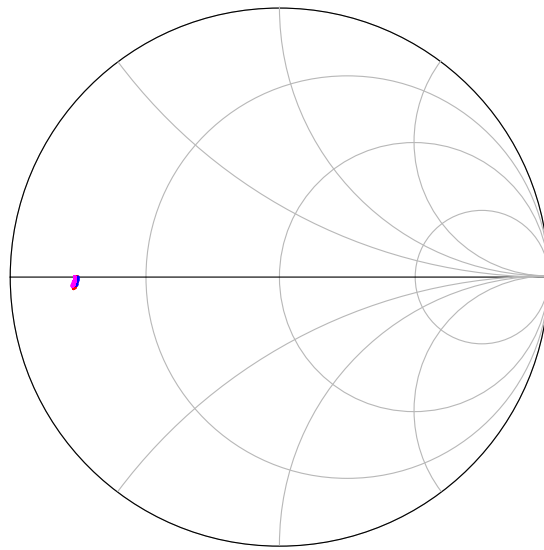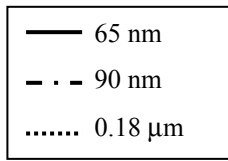
freq (1.000GHz to 100.0GHz)

(a)
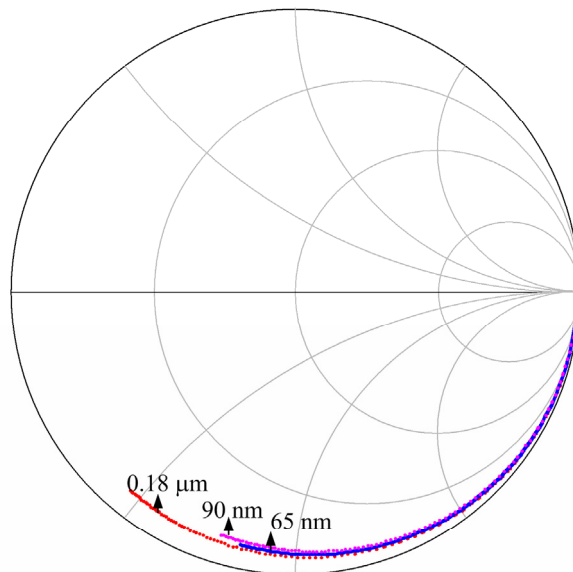
freq (1.000GHz to 100.0GHz)

(b)

Fig. 3.5. (a) The input impedance of on-state transistors for 0.18 μm, 90 nm, and 65 nm CMOS. (b) The input impedance of on-state transistors for 0.18 μm, 90 nm, and 65 nm CMOS.
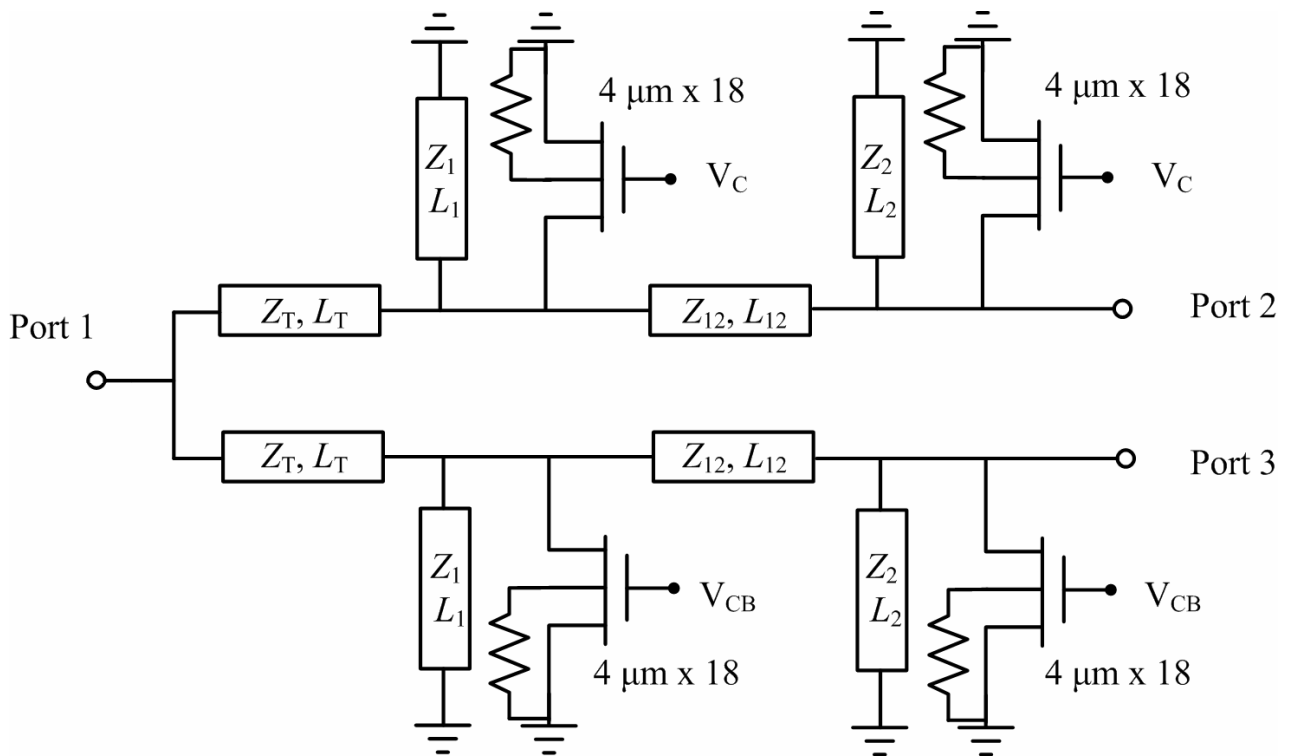
Fig. 3.6. Circuit schematic of a 60-GHz SPDT switch.
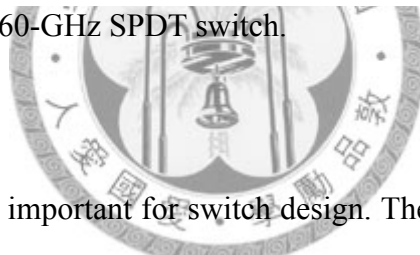
The choice of device size is important for switch design. The larger device has larger parasitic capacitors but smaller parasitic resistors. The smaller device has smaller parasitic capacitors but larger parasitic resistors. Since the through state of filter-integrated switches is composed of shunt off-state transistors, the higher parasitic capacitors reduce the bandwidth. Besides, the smaller shunt resistors can lead to better isolation since the function of isolation is by transforming low impedance to high impedance. The smaller the resistor locates at the right side of Smith chart, the higher impedance is achieved after quarter-wavelength transformation. Therefore, the larger device with smaller resistors can provide better isolation. There is trade off between larger devices and smaller devices.
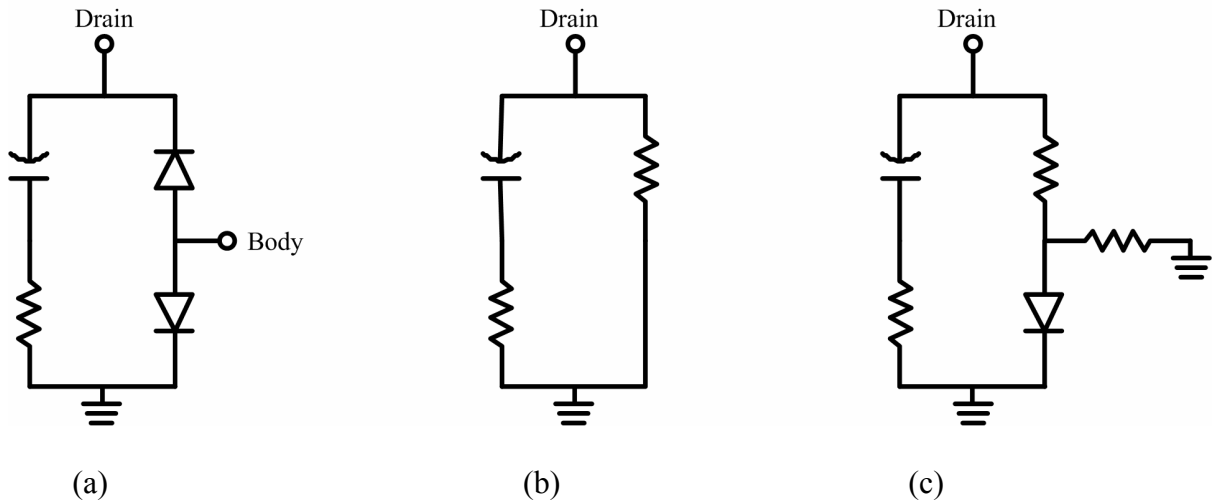
Fig. 3.7. (a) The simplified model of a shunt off-state MOSFET. (b) The simplified model of a shunt off-state MOSFET without body-floating. (c) The simplified model of a shunt off-state MOSFET with body-floating.

The large-signal simplified models for a shunt off-state MOSFET can be modeled as in Fig. 3.7 [7]. If the bulk of the shunt transistor is connected to ground, the simplified model is as shown in Fig. 3.7(b). If the bulk of the shunt transistor is connected to a large resistor, the simplified model is as shown in Fig. 3.7(c). Without body-floating, the diode between the body and the source is shorted, and hence, the current can flow from ground to drain through only one diode which is modeled as a resistor as in Fig. 3.7(b). With body-floating, the current from ground has to flow through the large resistor to drain as in Fig. 3.7(c). Therefore, under the same voltage swing at the drain, the current of the MOSFET with body-floating is less, and this leads to the equivalent impedance of a shunt MOSFET with body-floating higher. The results can be seen from Fig. 3.8(b). The power handling of a shunt MOSFET is mainly dependent on the pinch-on voltage V_B of the parasitic diodes [7]. Besides, if the bulk is floating and connected to a negative voltage $-V_{bias}$, the voltage swing at the drain of a shunt MOSFET can go from $-V_B$ to $-(V_B + V_{bias})$. Therefore, the technique body-floating with negative bias at the bulk can improve the power handling and the insertion loss of a shunt-type switch.

Fig. 3.8 shows the impedance of passive NMOS. S_{11} and S_{22} is the impedance of device *with* a

large resistor between source and body for on-state and off-state, respectively. S_{33} and S_{44} is the impedance of device *without* a large resistor between source and body for on-state and off-state, respectively. From this comparison in Fig. 3.8, we can know if there is a large resistor between source and body, the parasitic resistors of off-state transistors can be reduced. In our simulation based on the circuit in Fig. 3.6, the design with a large resistor between source and body can improve insertion loss better than 1 dB as shown in Fig. 3.9. Besides, due to adding a large resistor does not have much impact on on-state of transistors as in Fig. 3.8(b), the simulated isolation of the switch with large resistor is close to that without large resistor as shown in Fig. 3.9 (b).

In Fig. 3.6, Z_T is chosen for 50-Ω, and hence the width is about 7 μm for 65 nm CMOS technology. Z_1, Z_2, and Z_{12} should be chosen for high impedance in CMOS, but the width of 4 μm can only achieve about 60-Ω; therefore, the widths are all 4 μm. The width smaller than 4 μm causes very high loss, and that is why the narrower width of thin-film microstrip line is not used. L_T is about quarter-wavelength to achieve impedance transformation. L_1, L_2, and L_{12} are chosen to meet the condition to design a 3rd filters as described in the previous sections. These lines behave like inductors because of high impedance. The 3rd filter-integrated switch has three shunt resonators. Two resonators are composed of the shunt off-state transistors with L_1 and L_2 at the through arm. The other is composed by the isolated arm which is formed by quarter-wavelength with on-state transistors.

m1 60 GHz Impedance = 50 * (0.172 - j8.502E-4)

freq (1.000GHz to 100.0GHz)

S(1,1), S(2,2): w/o body-floating

S(3,3), S(4,4): with body-floating

(a)

m1 S22 60.00GHz impedance = 50 * (0.255 - j1.440)

m2 S44 60.00GHz impedance = 50 * (0.089 - j1.624)

freq (1.000GHz to 100.0GHz)
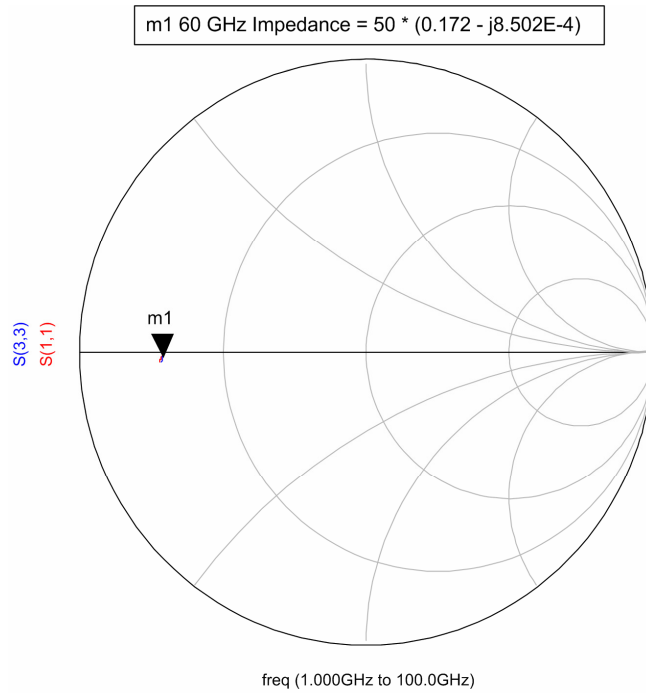
Fig. 3.8. The impedance of a passive NMOS in 65 nm CMOS. (a) On-state passive NMOS. (b) Off-state passive NMOS.
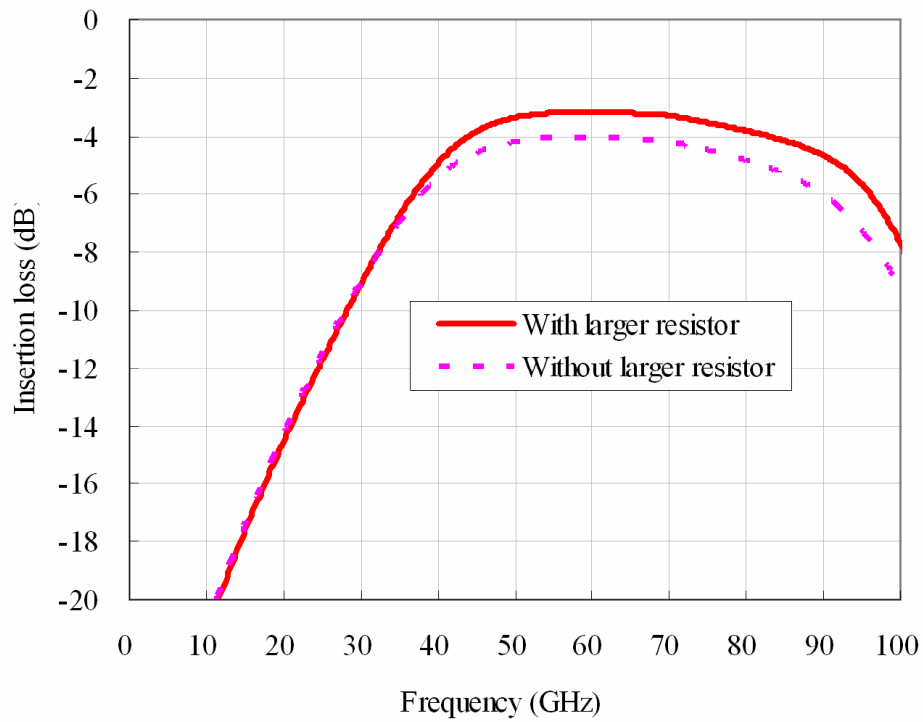
(a)
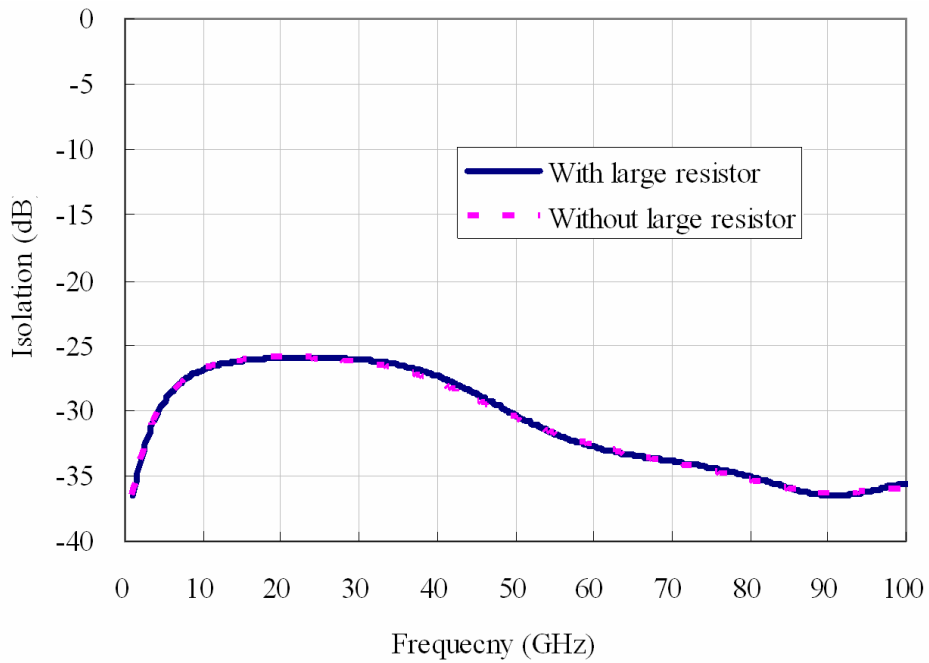
(b)

Fig. 3.9. Simulated with and without large resistor between source and body. (a) Insertion loss, (b) isolation.

29

Antenna

Tx   Rx
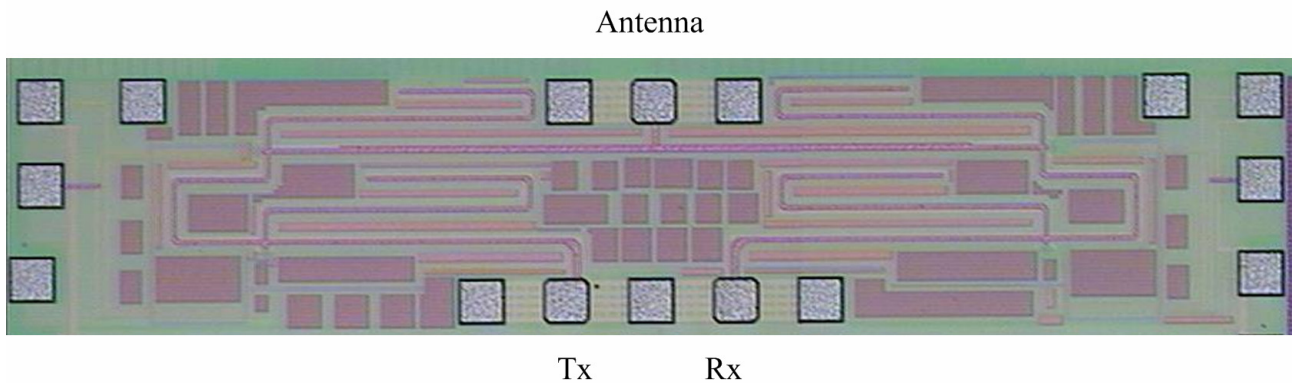
Fig. 3.10. The chip photo of 60-GHz SPDT filter-integrated switch. The chip size is 1500 μm x 250 μm.

3.4 Experimental Results of V-Band SPDT Switch in 65 nm CMOS
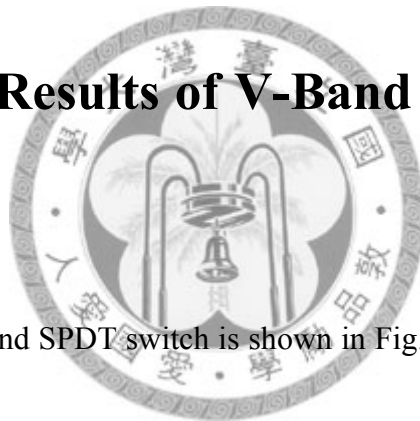
The chip photo of this V-band SPDT switch is shown in Fig. 3.10. The chip size is 1500 μm x 250 μm.

This SPDT switch is measured via on-wafer probing. Anritsu 37397D network analyzer is used to measure the S-parameters below 65 GHz. The simulated and measured insertion losses are shown in Fig. 3.11. The measured insertion loss quite agreed with simulated insertion loss. The insertion loss is about 3.2-4.5 dB in 40-80 GHz. The measured return loss is shown in Fig. 3.12. The measured return loss is better than 10 dB in 40-90 GHz. The measured isolation is about 20-27 dB in 40-80 GHz as shown in Fig. 3.13. There are some differences between the measured isolation and simulated isolation. If a small resistor about 5 ohm is added in the on-state of NMOS, the simulated isolation will become about 25 dB. The reason why the measured isolation cannot fit with simulated isolation might be the underestimate parasitic resistor of the NMOS in 65 nm CMOS.

The measured insertion loss versus input power at 60 GHz is shown in Fig. 3.14. There is no obviously 1–dB insertion loss compression point. The measured isolation versus input power at 60 GHz is shown in Fig. 3.15. There is also no power compression point for isolation.

Fig. 3.11. Simulated and measured insertion loss of 60-GHz SPDT switch.

Fig. 3.12. Simulated and measured return loss of 60-GHz SPDT switch.
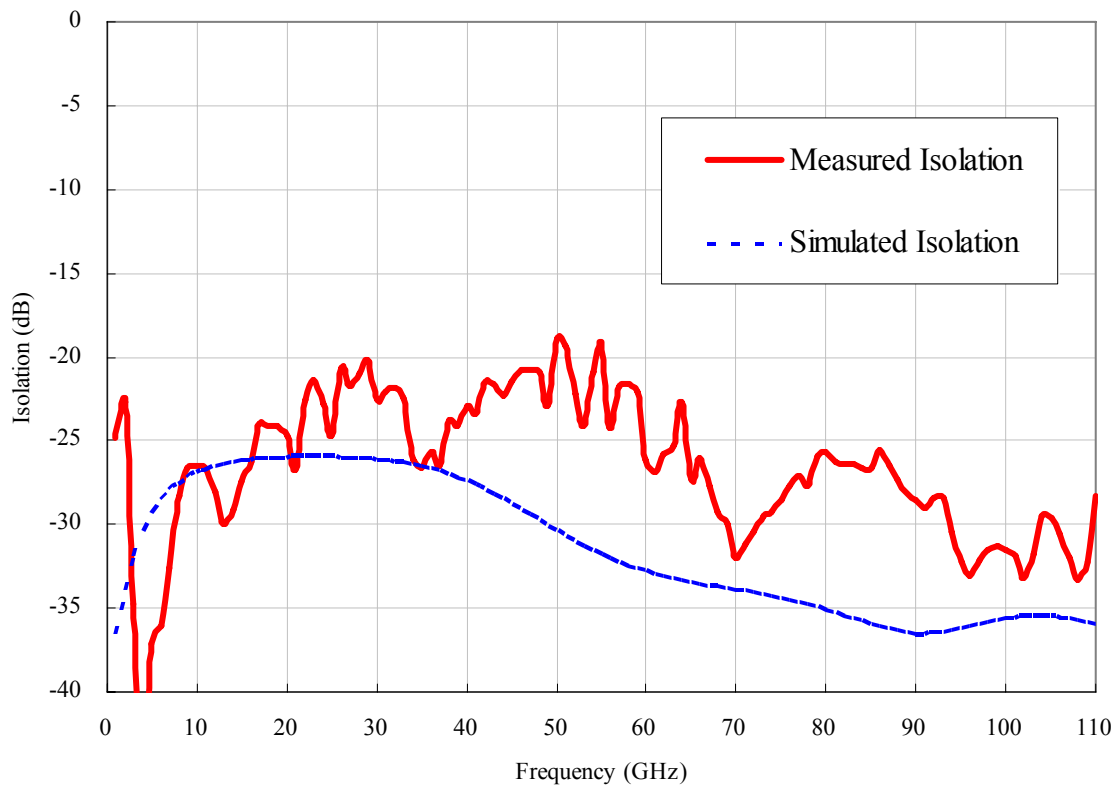
Fig. 3.13. Simulated and measured isolation of SPDT switch.
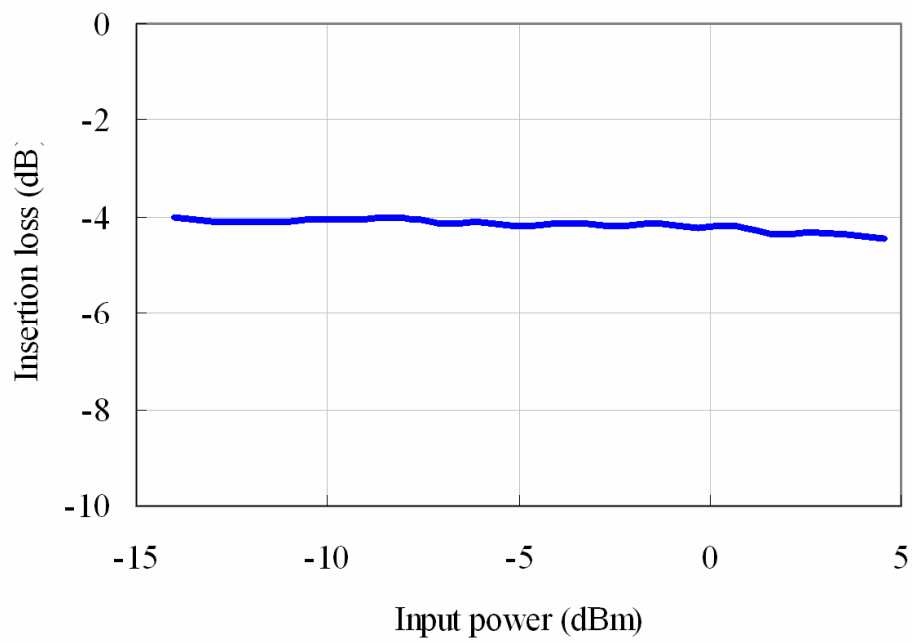
Fig. 3.14. Measured insertion loss versus input power.
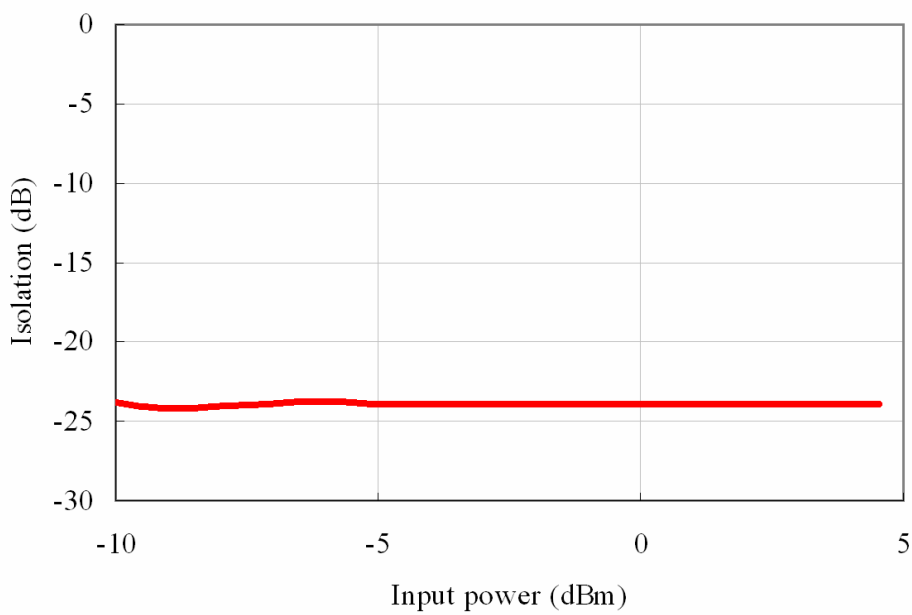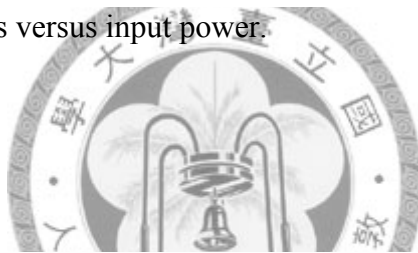
Fig. 3.15. Measured isolation versus input power.
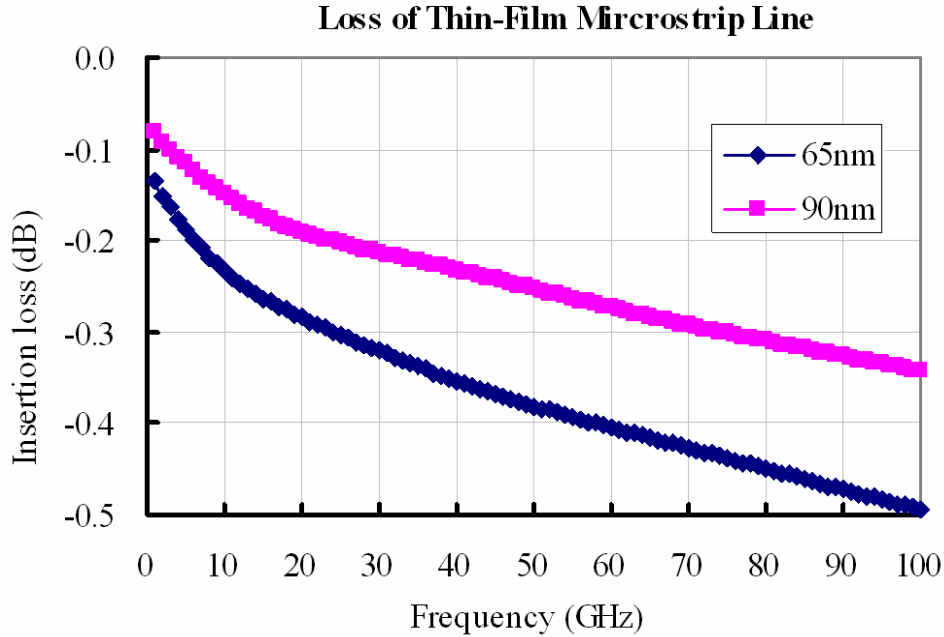
Fig. 3.16. Comparison of the loss of thin-film microstrip lines in 65 nm CMOS and 90 nm CMOS.

3.5 Circuit Implementation of 60 to 110 GHz SPDT Switch in 90 nm CMOS

In fact, the architecture of the 60 to 110 GHz SPDT switch using 90 nm CMOS is similar to Fig. 3.6 except that the device sizes are 4 µm x 16 for 90 nm CMOS. The input impedance of the NMOS with and without body-floating is shown in Fig. 3.17.

The body-floating technique is also adopted to design this SPDT switch due to the benefits discussed in section 3.3. The resistance of on-state NMOS is chosen for 9 ohm to achieve an isolation of 30 dB in simulation. The capacitance of off-state NMOS is 0.435 pF. The lengths of thin-film microstrip lines in this switch are centered at 80 GHz. The width of 50-ohm thin-film microstrip lines in 90 nm CMOS is 10 µm. The comparison between the loss of 50-ohm thin-film

microstrip lines in 65 nm CMOS and that of 90 nm CMOS is shown in Fig. 3.16. Since the lower

loss in 90 nm CMOS, it is more suitable to use 90 nm CMOS to design passive RF elements

including switches.

m1   80.00GHz   impedance = 50 * (0.187 − j0.048)

S(1,1), S(2,2): w/o body-floating

S(3,3), S(4,4): with body-floating

S(3,3)
S(1,1)

m1

freq (1.000GHz to 150.0GHz)

(a)

m1 S22 80.00GHz impedance = 50 * (0.114 − j0.901)

m2 S44 80.00GHz impedance = 50 * (0.090 − j0.910)
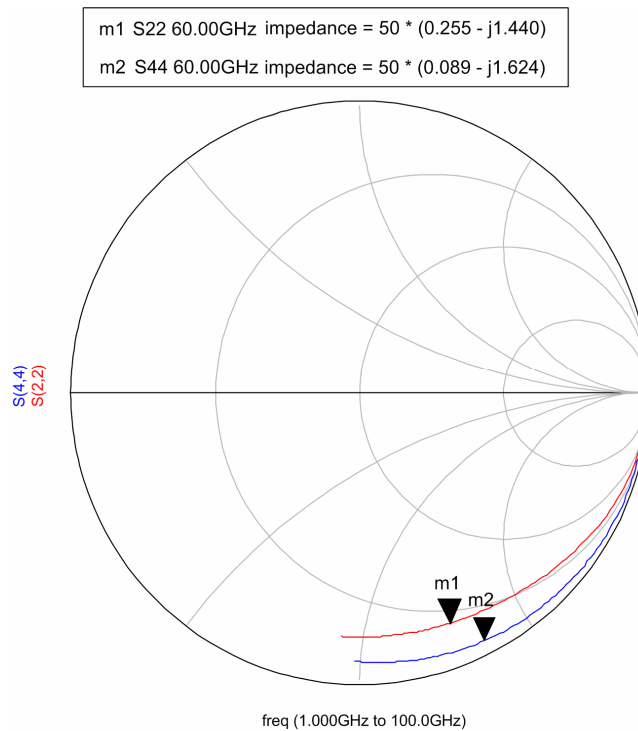
S(4,4)
S(2,2)

m2

freq (1.000GHz to 150.0GHz)
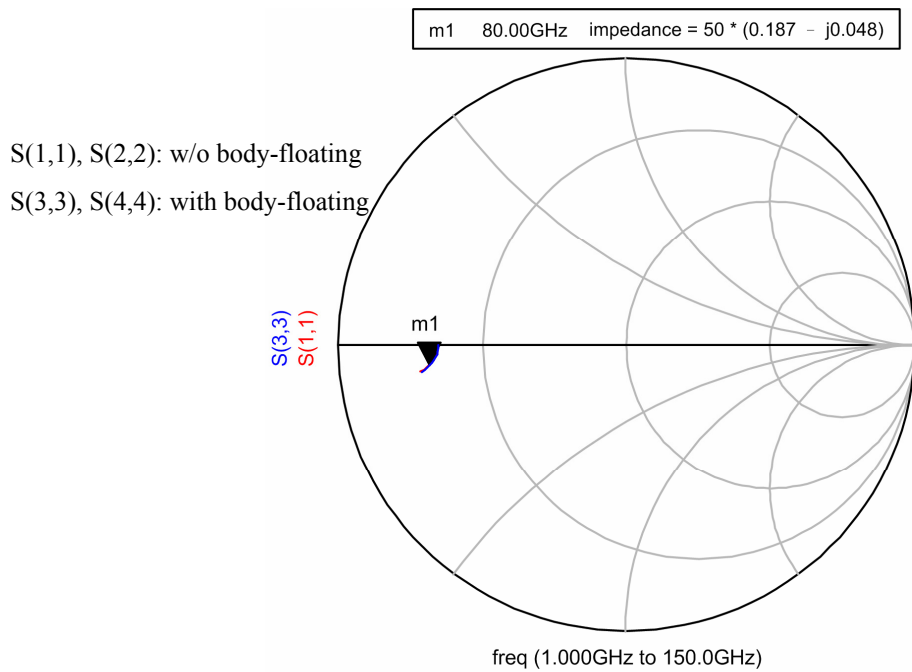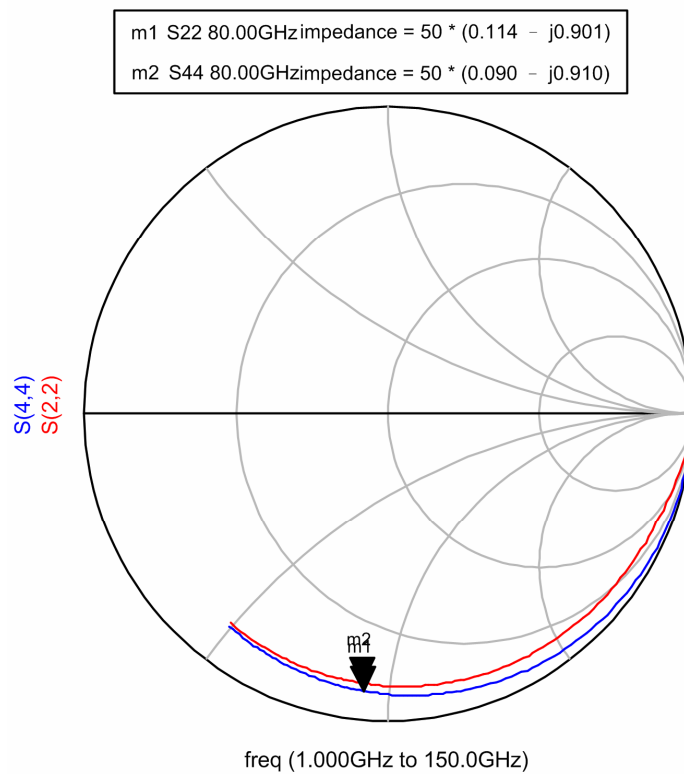
(b)

Fig. 3.17. The impedance of a passive NMOS in 90 nm CMOS. (a) On-state passive NMOS. (b) Off-state passive NMOS.

37
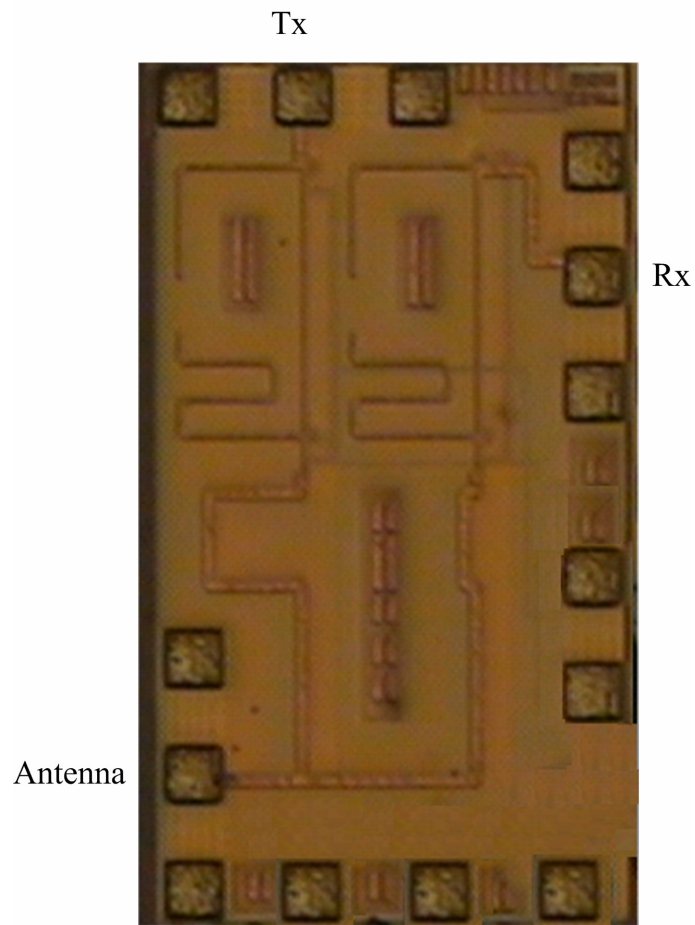
Fig. 3.18. The chip photo of the 60-110 GHz SPDT switch with a size of 400 μm x 750 μm.

3.6 Experimental Results of 60 to 110 GHz SPDT Switch in 90 nm CMOS

The chip photo of this 60-110 GHz SPDT switch in 90 nm CMOS is shown in Fig. 3.18. The chip size is 400 μm x 750 μm.

This SPDT switch is measured via on-wafer probing. Anritsu 37397D network analyzer is used to measure the S-parameters below 65 GHz. The simulated and measured insertion losses are

shown in Fig. 3.19. The measured insertion loss quite agreed with simulated insertion loss. The insertion loss is about 3-4 dB in 60-110 GHz. The measured return loss is shown in Fig. 3.20. The measured return loss is better than 10 dB in 50-110 GHz. The measured isolation is better than 25 dB in DC-110 GHz as shown in

Fig. 3.21. The measured isolation also quite agreed with simulated isolation. The reason of the difference between the measured isolation and simulated isolation above 65 GHz is due to the precision of calibration for the band of 65-110 GHz. The measured power performance at 75 GHz of this 60-110-GHz SPDT switch is shown in Fig. 3.22, and the power performance of 1-dB compression point appears about P_{in} = 10.5 dBm.

The data above 110 GHz cannot be measured due to the limitation of the instruments. However, the 110-150-GHz frequency response can be predicted by simulation, and the simulated insertion loss goes more than 4 dB at 115 GHz.
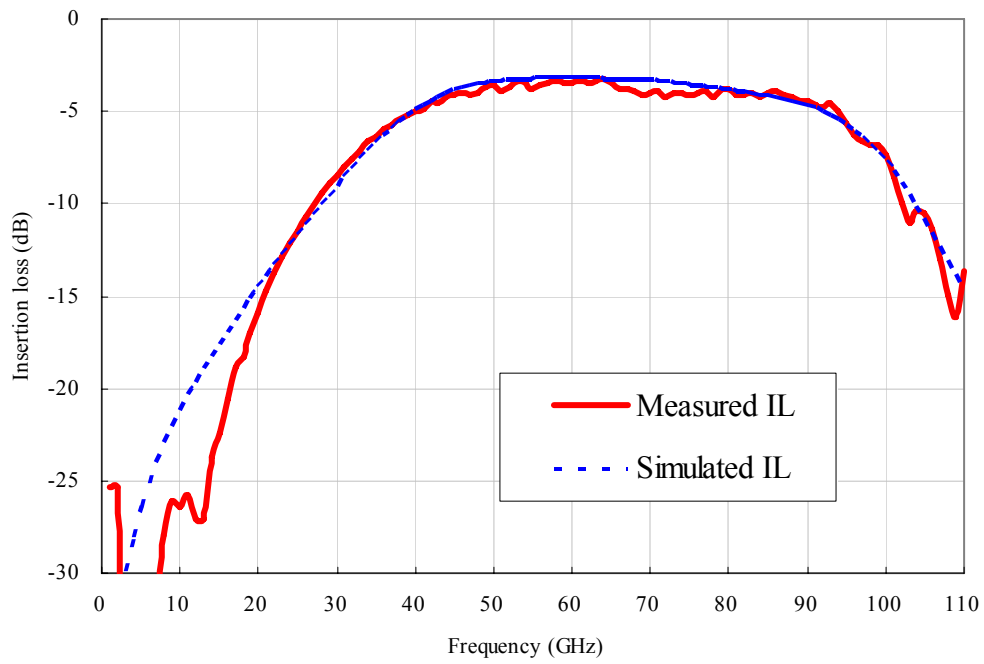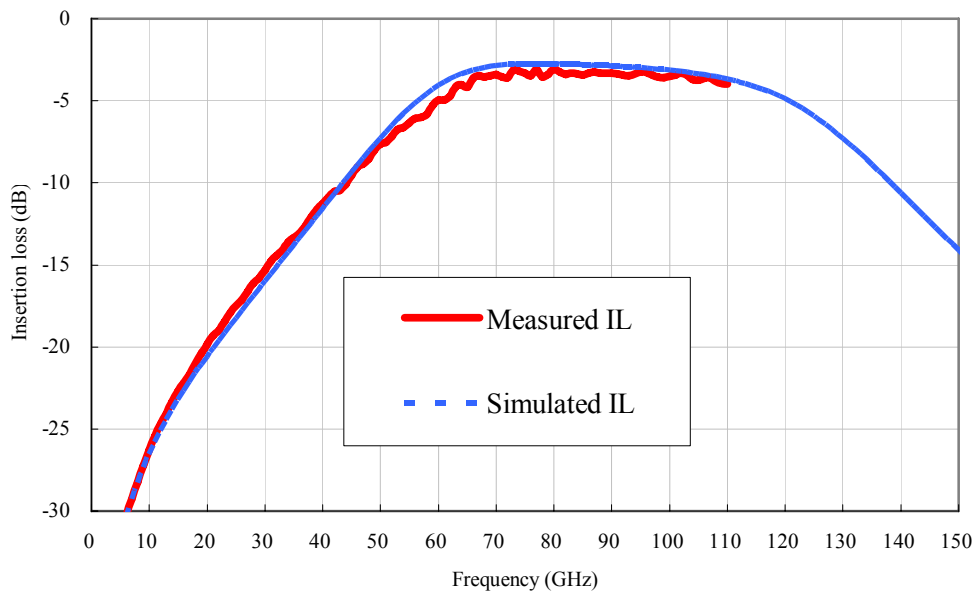
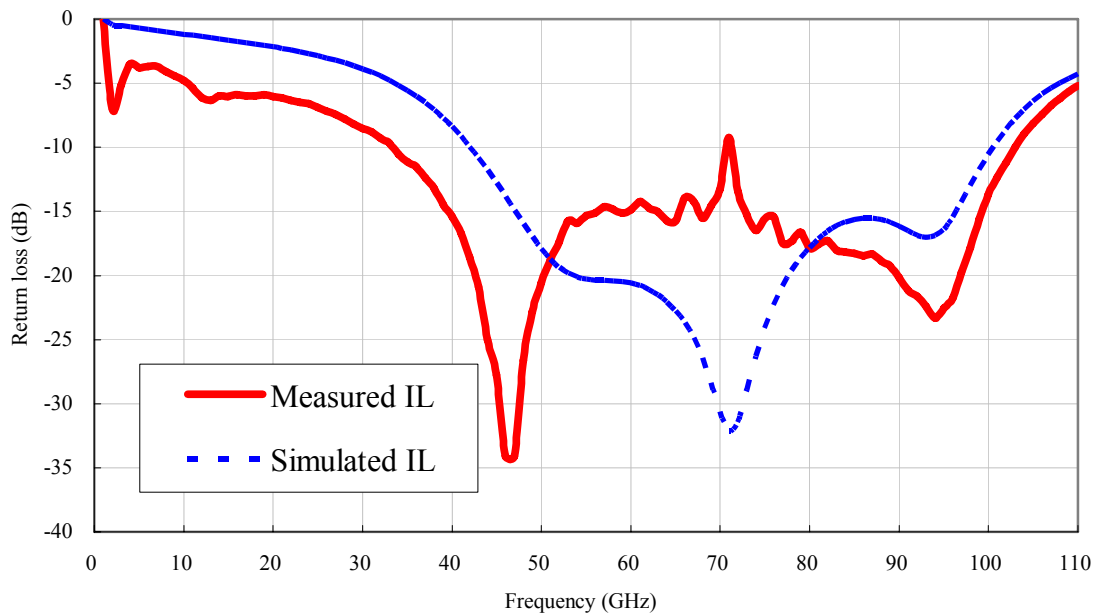Fig. 3.19. Simulated and measured insertion loss of 60-110 GHz SPDT switch.
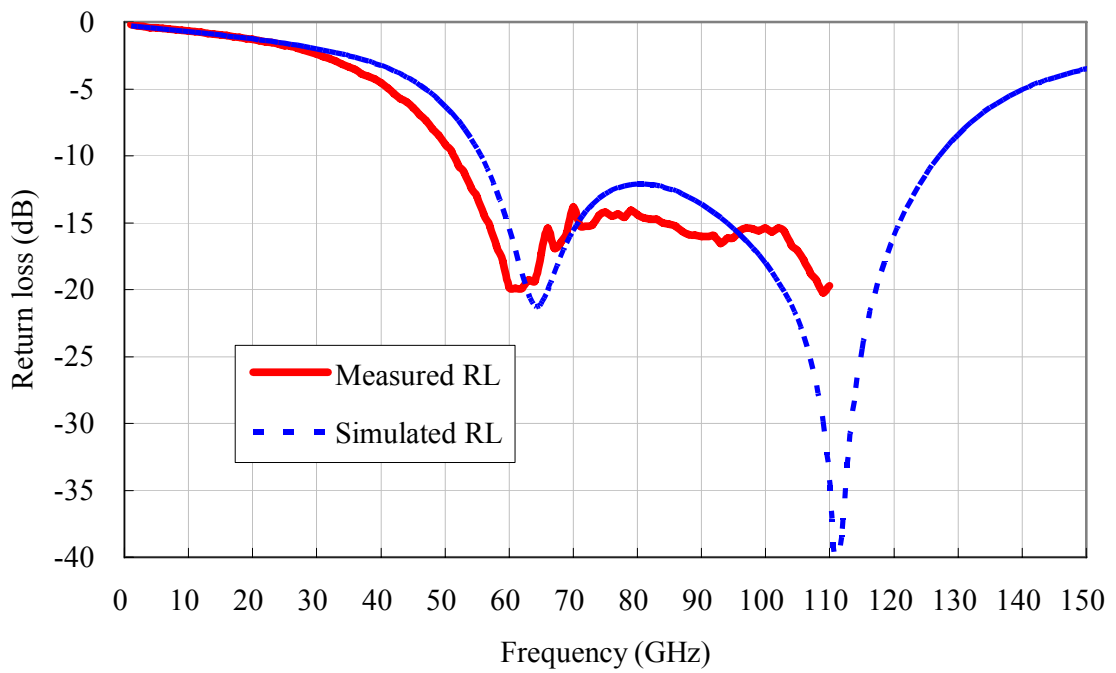
Fig. 3.20. Simulated and measured return loss of 60-110 GHz SPDT switch.
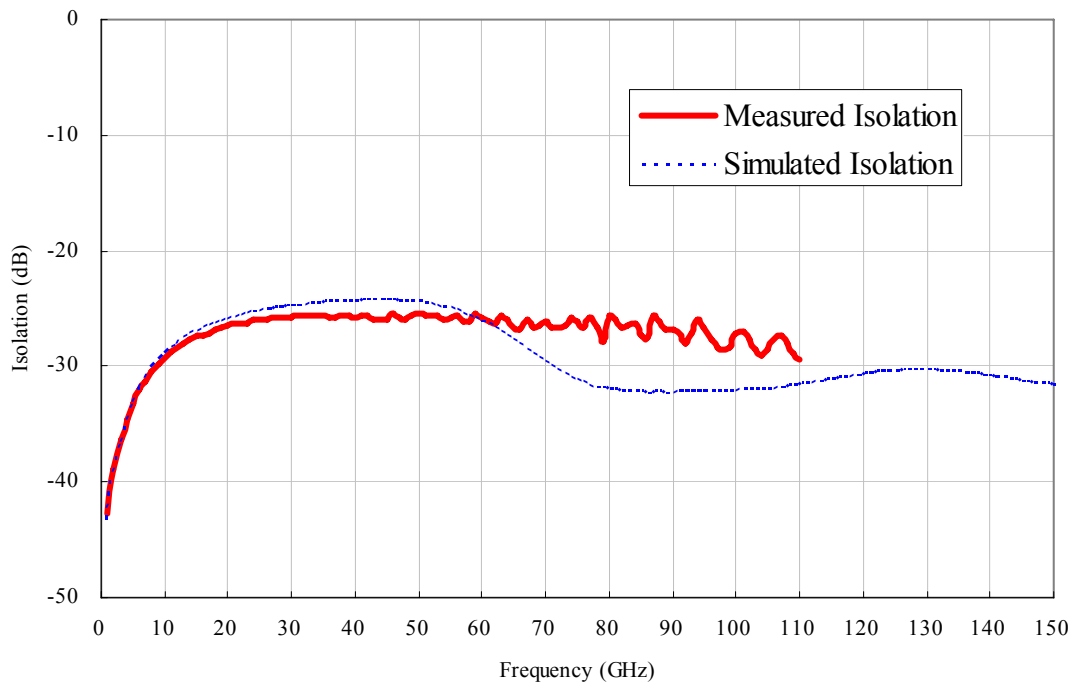
Fig. 3.21. Simulated and measured isolation of 60-110 GHz SPDT switch.
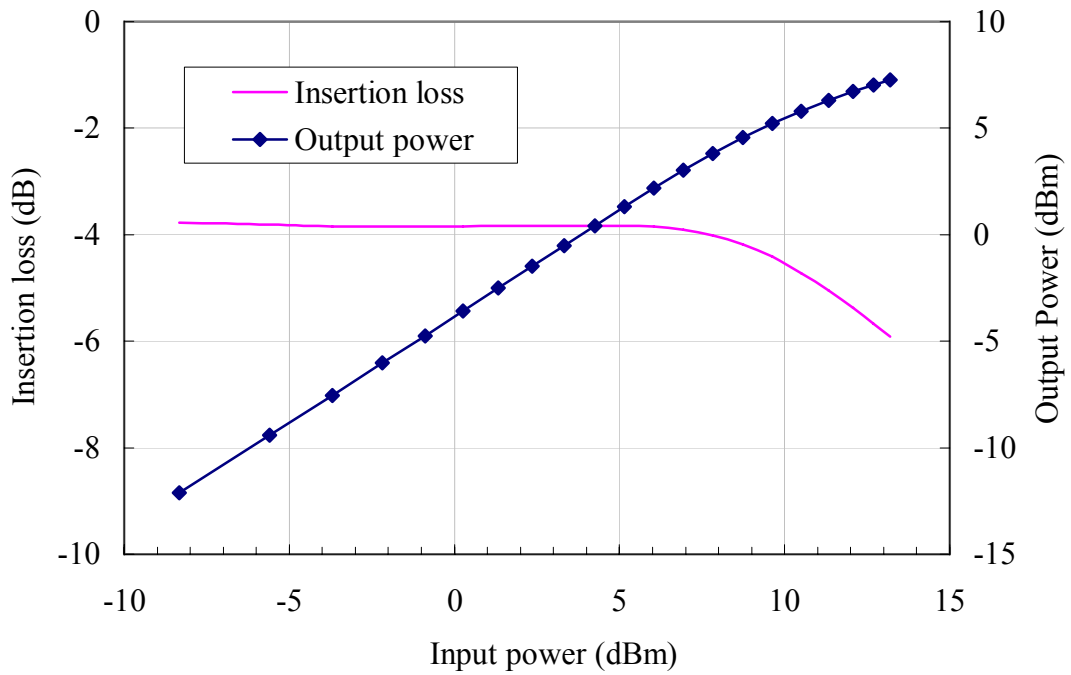
Fig. 3.22. Measured power performance at 75 GHz of 60-110 GHz SPDT switch.

3.7 Summary

The MMW SPDT switch using 65 nm CMOS process is demonstrated in this chapter. There is quite agreement between the measured results and simulated results. The insertion loss is about 3.2-4.5 dB in 40-80 GHz. The return loss is quite good and it is better than 10 dB in 40-80 GHz, since the filter-integrated switch topology can provide good matching. The isolation is about 20-27 dB in 40-80 GHz. There is no power compression point for insertion loss and isolation even the input power is 5 dBm.

Besides, the 60-110 GHz SPDT using 90 nm CMOS process is also demonstrated in this chapter. There is also a quite agreement between the measured results and simulated results. The insertion loss is about 3.0-4.0 dB in 60-110 GHz. The return loss is quite good and it is better than 10 dB in 50-110 GHz, since the filter-integrated switch topology can provide good matching. The isolation is better than 25 dB in DC-110 GHz. This switch is the highest frequency CMOS SPDT switch reported to date.

The comparison of CMOS switches is shown in Table 3.1. The SPST switch in 65 nm CMOS [8] shows good performance, but the design approach of simply shun transistors can only be used in SPST switch design. It can be observed that the 90 nm filter-integrated SPDT switch in this thesis has the highest operating frequency and has very good performance. Besides, since the passive components (thin-film microstrip lines) have higher loss in 65 nm CMOS than 90 nm CMOS in our simulation, it might be better to design passive RF components in 90 nm CMOS.

Table 3.1

SUMMARY OF THE PERFORMANCE OF REPORTED SWITCHES IN CMOS PROCESS

Technology	Design Approach	Frequency (GHz)	Insertion Loss (dB)	Isolation (dB)	I/O	Ref.
65 nm CMOS	Shunt	DC-94	1.6	19-30	SPST	[8]
90 nm CMOS	Traveling wave concept	50~94	<3.3	>27	SPDT	[9]
130 nm CMOS	Transmission-line integrated	57~66	4.5~5.8	24~26	SPDT	[10]
180 nm CMOS	Traveling wave concept	DC~50	<6	>38	SPDT	[11]
90nm CMOS	LC-tuned	24	3.5	22	SPDT	[12]
130 nm SiGe	Transmission-line integrated	51~78	2~2.7	>25	SPDT	[13]
130 nm CMOS	Series-shunt	33~43	<3	>25	SPDT	[14]
0.15 um GaAs HEMT	Filter-integrated	42~67	<2.5	>27	SPDT	[15]
0.15 um GaAs HEMT	Filter-integrated	40~60	<1.5	>22	SPDT	[16]
90nm CMOS	**Filter-integrated**	**65~110**	**3-4**	**>25**	**SPDT**	**This work**
65 nm CMOS	**Filter-integrated**	**40~80**	**3.2~4.5**	**>20**	**SPDT**	**This work**

Chapter 4 Topology Analysis of Millimeter -Wave Multiple-Port Switches

4.1 Introduction

RF switches are important components in the front end of the RF transmit/receive (T/R) communication systems to control microwave signals. Recently, the importance of wireless service has increased rapidly, and higher network capacity with better performance is required. A beamformer system using multiple antennas both at the transmitter and receiver can improve the efficiency of the spectrum greatly by spatial multiplexing [17]–[20]. In a beamformer system, it is important to have a good multiple-port switch.

There are many approaches to design a passive field-effect transistor (FET) switch. For the frequency below 20 GHz, switches using series or shunt HEMTs (or FETs) in [21]–[23], and traveling-wave concepts in [24] are reported with good performances. In the millimeter-wave (MMW) frequency range, the traveling-wave concept is usually used to realize wideband switches [25], [26]. Switches using the impedance transformation technique are reported with good isolation [27], but they show narrowband performances and occupy a large chip area. MMW switches based on resonant-type structures or filter-integrated switches are reported with good performances in [28]–[32]; however, they are still narrowband designs. Nevertheless, most of the above-mentioned switches [21], [22], [25]–[30], [33]–[36] and switch products [37], [38] are single-pole–multiple-throw (SPMT) designs, and there are only a few studies that discuss multiple-port switches [39]–[43].

Multiple-port switches in series-shunt topology were reported with good performances below 10 GHz [39]–[41]. Multiple-port switches using microelectromechanical system (MEMS) technology presented good performances to around 20 GHz [42], but the MEMS process is not compatible to most monolithic microwave integrated circuit (MMIC) processes and the high voltage of the MEMS switch makes it not easy to use in real applications. A multiple-port bandpass filter-integrated switch is reported in [43], but it is designed for narrow bandwidth.

In this chapter, we have categorized MMW multiple-port switch topologies. The formulations of the bandwidth, insertion loss, and isolation with respect to different topologies are also derived. Based on the analysis, the limitations of RF performances of multiple-port switches are mostly dominated by their topologies instead of the unit switch cell. It means that once the topology is selected, the performances can be predicted according to the derived equations.

4.2　Introduction　to　Different　Type　Multiple-Port Topologies
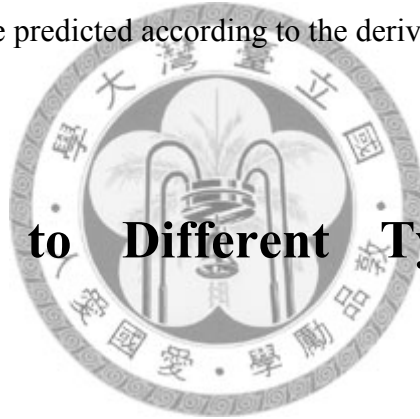
Fig. 4.1 shows four types of topologies of MMW multiple-port switches with two inputs and four outputs. For a signal flow from multi-input to multi-output, binary-tree logic is intuitively considered, and the topology is shown in Fig. 4.1(a). In [41], a matrix type structure was used to realize an $n \times m$ switch. Similarly, a matrix topology can be used to form a multiple-port switch, as shown in Fig. 4.1(b). A net-type multiple-port topology is proposed in Fig. 4.1(c). Another topology to implement a multiple-port switch is a ring-binary type, which is shown in Fig. 4.1(d). Compared with the binary-tree topology in Fig. 4.1(a), the ring-binary type has the advantage of its simple control logic to control the signal flow [39].

4.3 Analytical Derivation of Insertion Loss of Multiple-Port Topologies

In order to analyze these four types of topologies in Fig. 4.1, we construct equivalent-circuit models to investigate the insertion loss and bandwidth performances in the thru-state. Simply a series, shunt, or series/shunt HEMT design approach is not suitable for a high-frequency switch. Fig. 4.2 shows a block diagram for the on state of the unit switch, and the equivalent-circuit model for the off state of the unit switch. For MMW passive HEMT switch design, a quarter-wavelength transmission line is needed to transform an off-state single-pole–single-throw (SPST) switch from low impedance into high impedance for blocking the RF signal [25]–[27], [29], [30], [33], [34]. Therefore, the quarter-wavelength transmission lines are included in the unit switches, as shown in the equivalent-circuit model of Fig. 4.2(b).

(a)

(b)

(c)
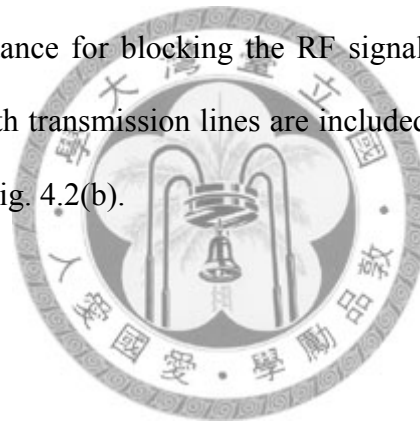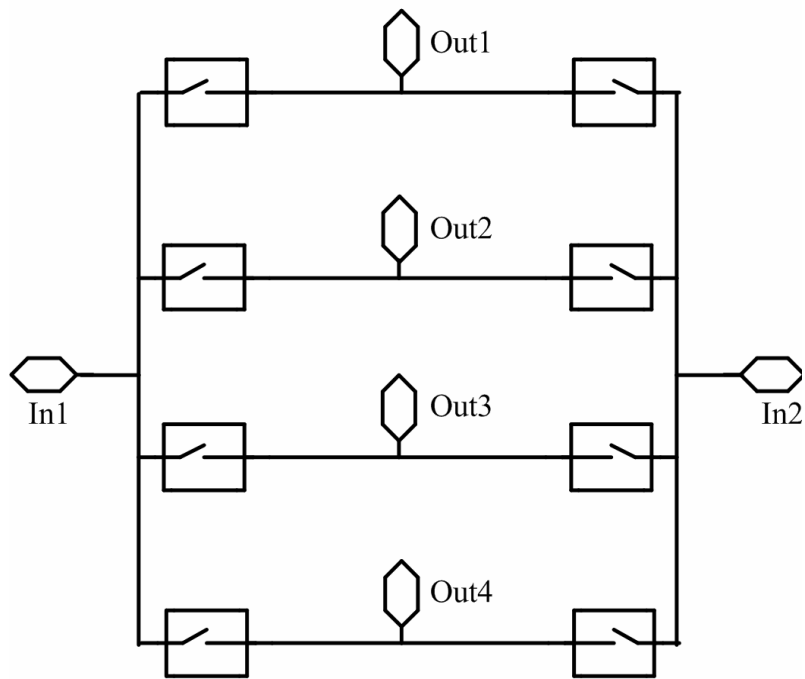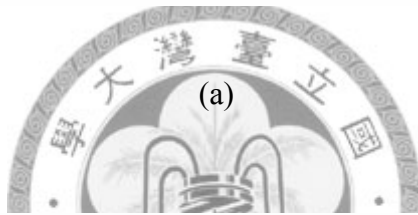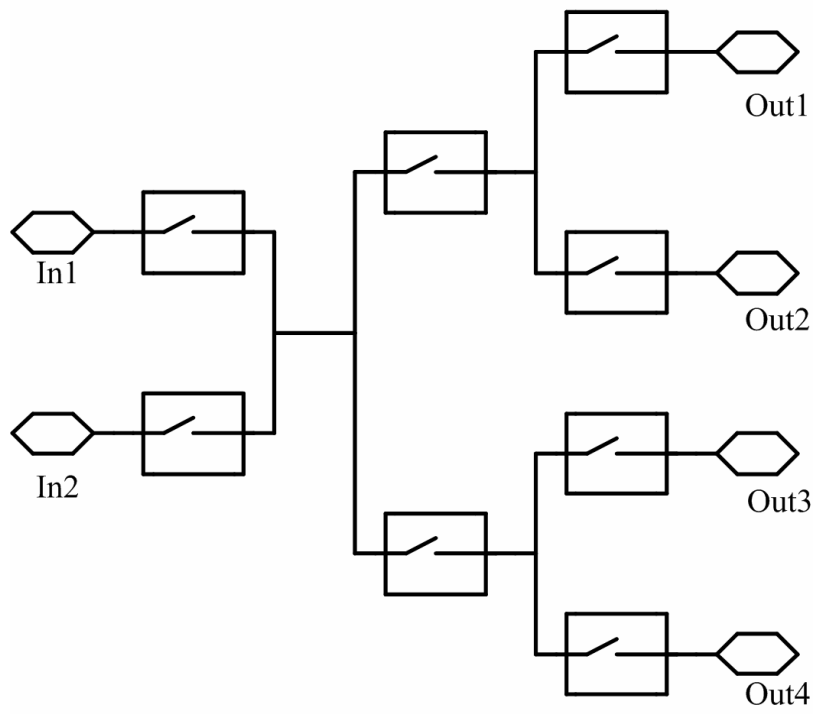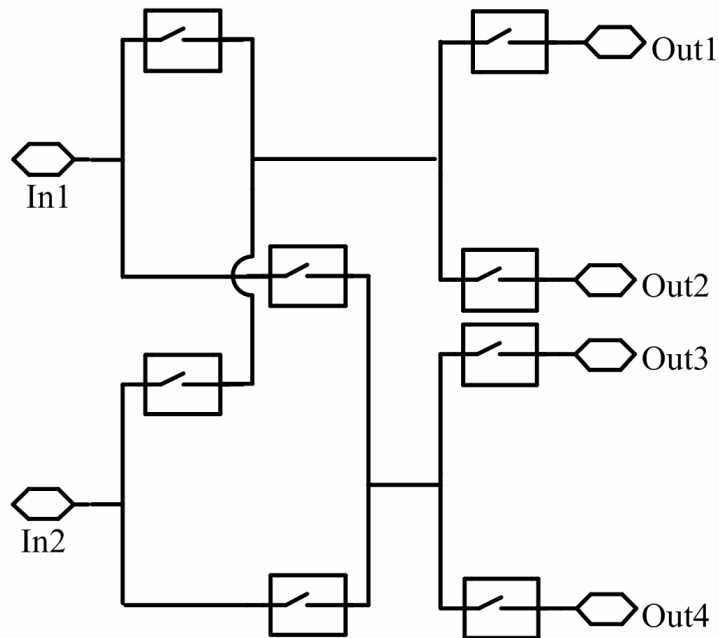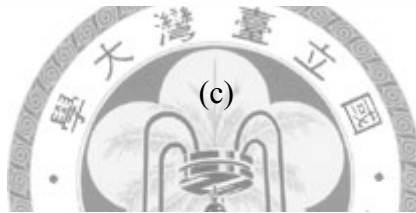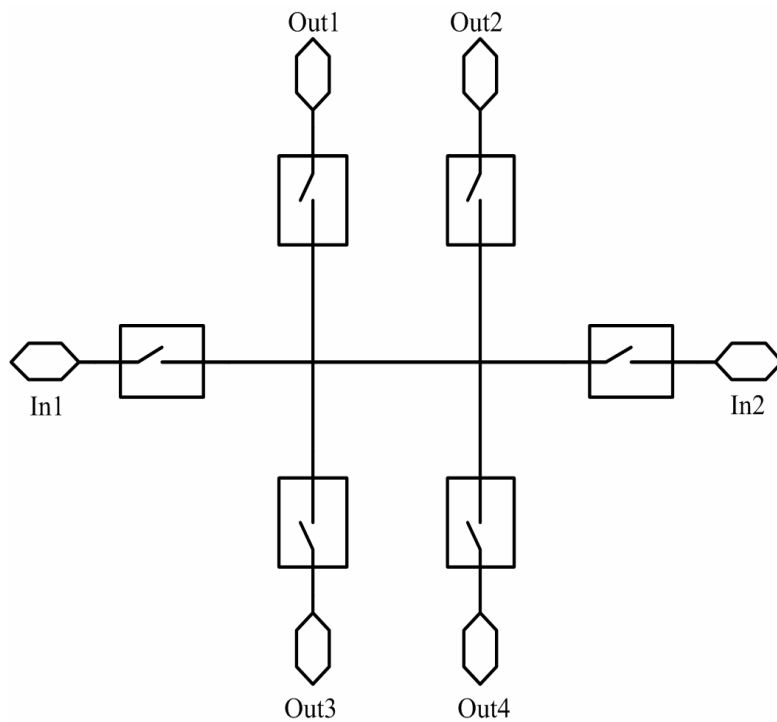
(d)

Fig. 4.1. Four types of multiple-port switch topology. (a) Binary-tree type. (b) Matrix type. (c) Net type. (d) Ring-binary type.

<div align="center">(a)   (b)</div>
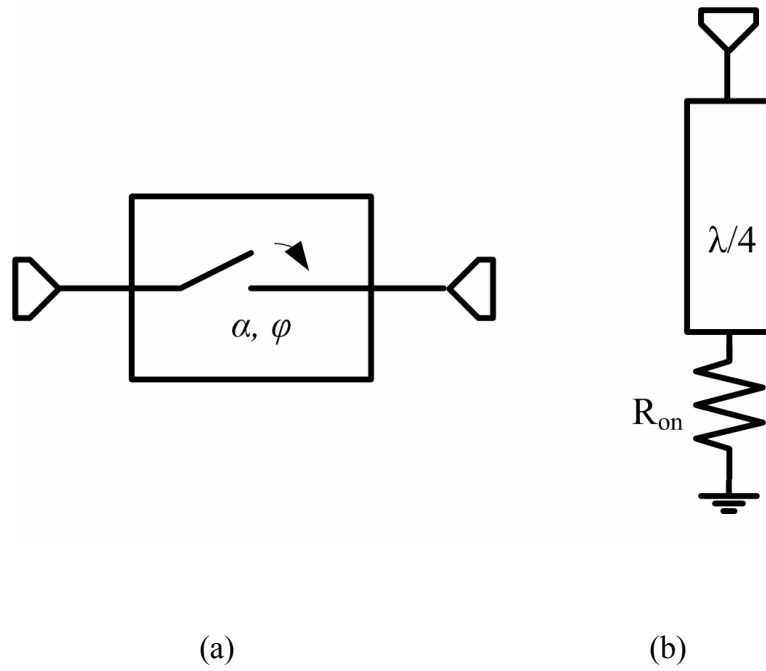
Fig. 4.2. (a) Block diagram for the on state of the unit switch. (b) Equivalent-circuit model for the off state of the unit switch.

Based on the unit switch defined above, the off-state unit switch is modeled as a quarter-wavelength transmission line connected by a small resistor with a parasitic inductor so we model a though path between the input port and output port of these four types of topologies, as shown in Fig. 4.3. In order to simplify the analysis, we ignore the parasitic inductor of on-state HEMTs. Since the unit switch is designed with the same characteristics, the behavior of each on-state unit switch is modeled as the loss of $\alpha(f, C_{off})$ caused by the SPST switch and electrical delay of ϕ, where f denotes frequency; furthermore, the input and output match of a unit switch is assumed perfect for simplicity.

The binary-tree type is analyzed first. The transmission coefficient, denoted as $S_{21,a}$ of that, can be derived as
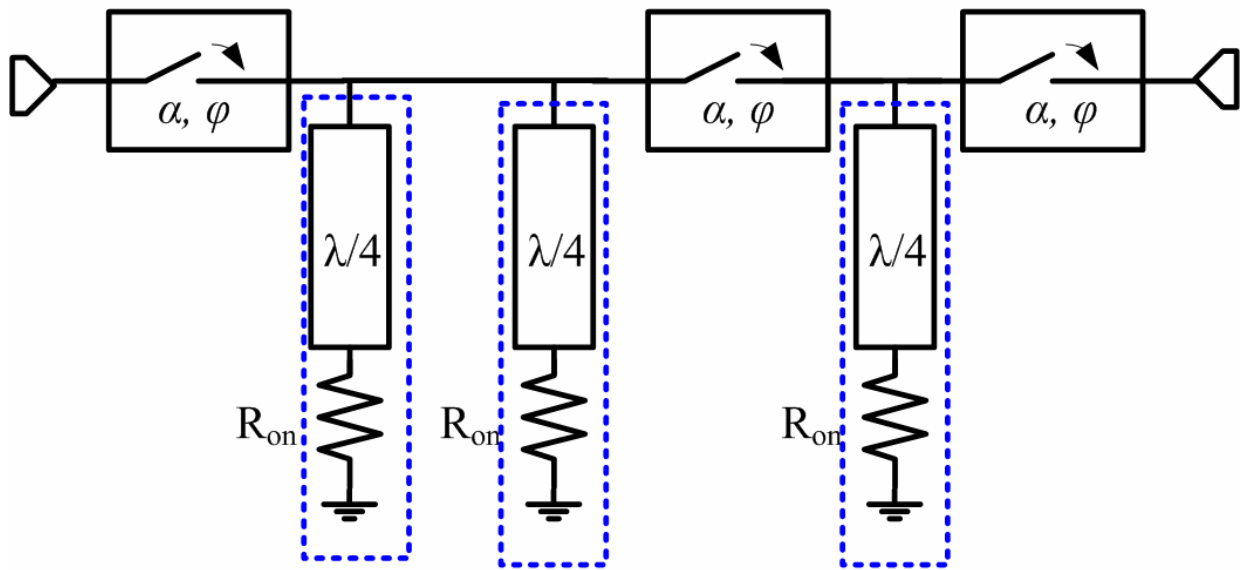
(a)
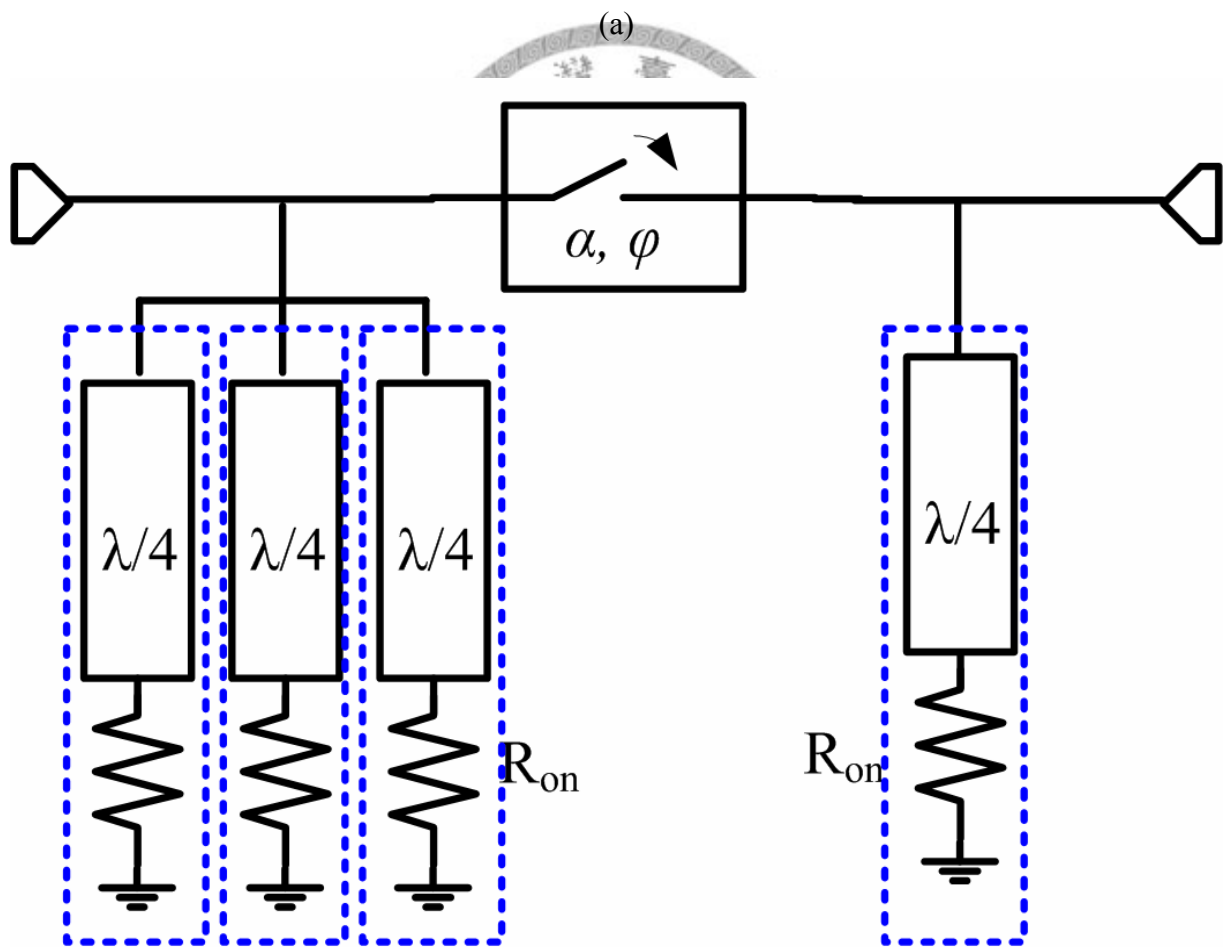
(b)
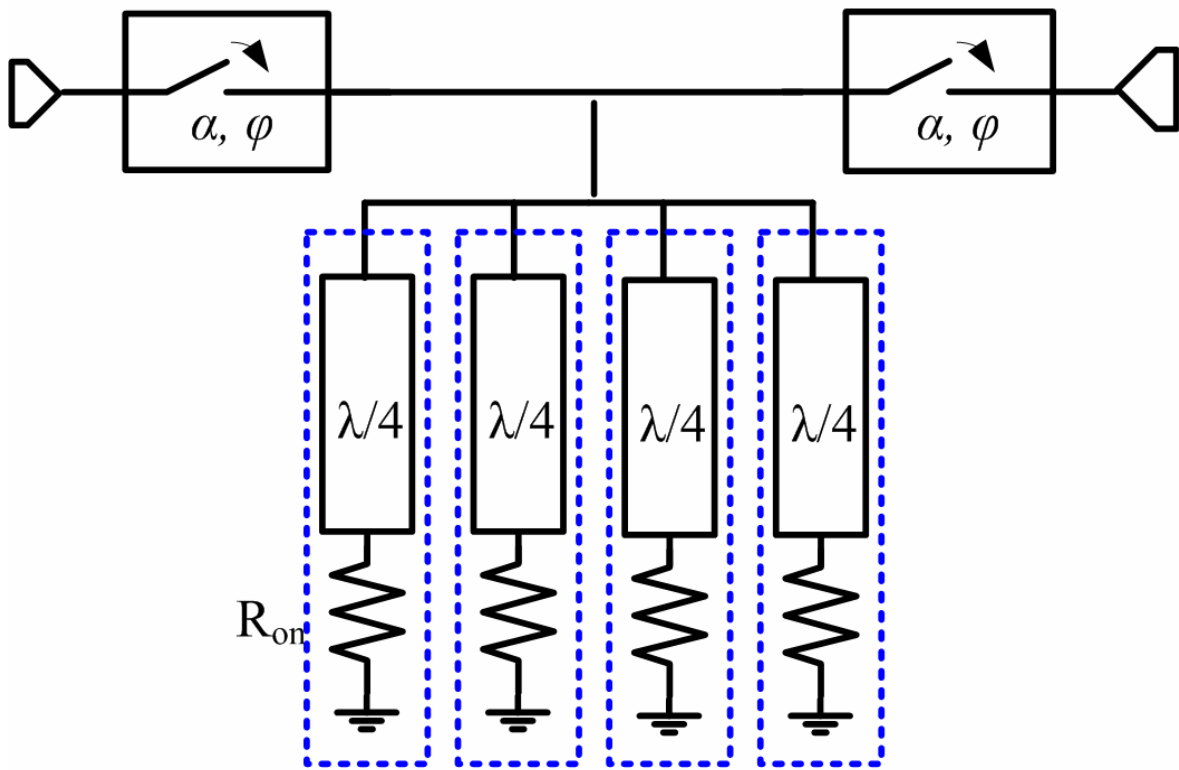
(c)
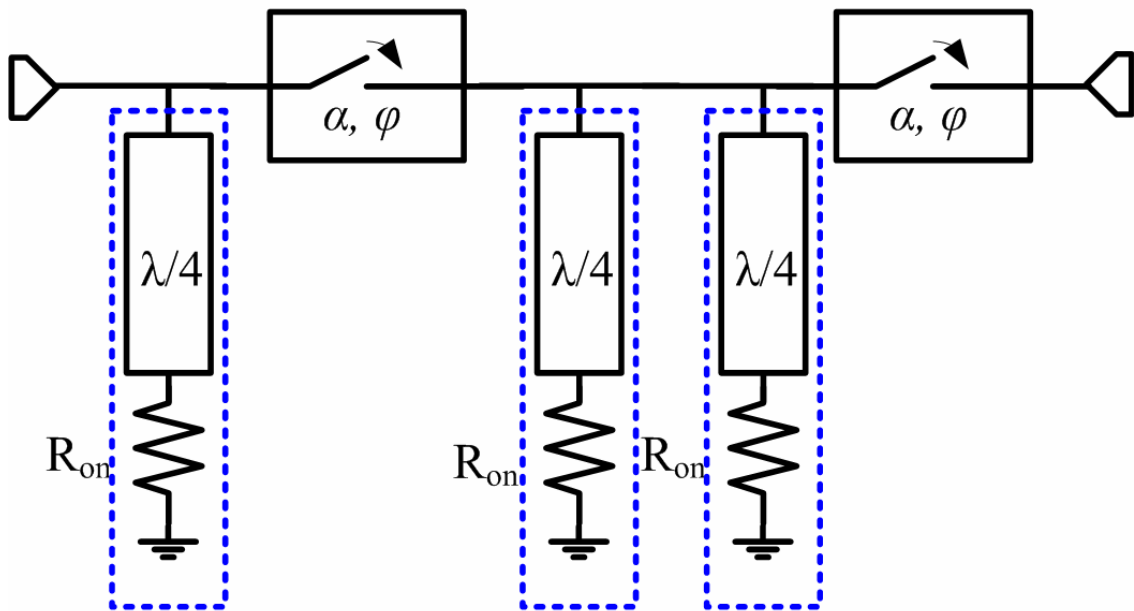
(d)

Fig. 4.3 Equivalent circuit models of a through path for: (a) binary-tree type, (b) matrix type, (c) net type, and (d) ring-binary type.

$$S_{21,a}=\alpha(f,C_{off})e^{-j\phi}\times\frac{2(r_{on}+j\tan\theta)}{2r_{on}+2+j(2+2r_{on})\tan\theta}\times\alpha(f,C_{off})e^{-j\phi}\times\frac{2(r_{on}+j\tan\theta)}{2r_{on}+1+j(1+r_{on})\tan\theta}\times\alpha(f,C_{off})e^{-j\phi} \qquad (4.1)$$

where r_{on} denotes the R_{on} normalized by the referenced impedance of $Z_0 = 50\Omega$.

The electrical length of the quarter-wavelength transmission line for center frequency f_0 can be represented by

$$\theta = \frac{\pi}{2}\times\frac{f}{f_0} \qquad (4.2)$$

The magnitude of the transmission coefficient of the binary-tree-type topology can be derived as

$$|S_{21,a}|=|\alpha(f,C_{off})|^3\frac{\sqrt{r_{on}^2+\tan^2(\frac{\pi}{2}\times\frac{f}{f_0})}}{\sqrt{(r_{on}+1)^2+(1+r_{on})^2\tan^2(\frac{\pi}{2}\times\frac{f}{f_0})}}\times\frac{2\sqrt{r_{on}^2+\tan^2(\frac{\pi}{2}\times\frac{f}{f_0})}}{\sqrt{(2r_{on}+1)^2+(2+r_{on})^2\tan^2(\frac{\pi}{2}\times\frac{f}{f_0})}} \qquad (4.3)$$

Similarly, the magnitude of the transmission coefficient of matrix type ($S_{21,b}$) is obtained as

$$|S_{21,b}|=|\alpha(f,C_{off})|\frac{2\sqrt{r_{on}^2+\tan^2(\frac{\pi}{2}\times\frac{f}{f_0})}}{\sqrt{(2r_{on}+3)^2+(2+3r_{on})^2\tan^2(\frac{\pi}{2}\times\frac{f}{f_0})}}\times\frac{2\sqrt{r_{on}^2+\tan^2(\frac{\pi}{2}\times\frac{f}{f_0})}}{\sqrt{(2r_{on}+1)^2+(2+r_{on})^2\tan^2(\frac{\pi}{2}\times\frac{f}{f_0})}} \qquad (4.4)$$

and the magnitude of the transmission coefficient of net type ($S_{21,c}$) is

$$|S_{21,c}| = |\alpha(f, C_{off})|^2 \frac{\sqrt{r_{on}^2 + \tan^2(\frac{\pi}{2} \times \frac{f}{f_0})}}{\sqrt{(r_{on} + 2)^2 + (1 + 2r_{on})^2 \tan^2(\frac{\pi}{2} \times \frac{f}{f_0})}} \tag{4.5}$$

The magnitude of the transmission coefficient of ring-binary type ($S_{21,d}$) is

$$|S_{21,d}| = |\alpha(f, C_{off})|^2 \frac{2\sqrt{r_{on}^2 + \tan^2(\frac{\pi}{2} \times \frac{f}{f_0})}}{\sqrt{(2r_{on} + 1)^2 + (2 + r_{on})^2 \tan^2(\frac{\pi}{2} \times \frac{f}{f_0})}} \times \frac{\sqrt{r_{on}^2 + \tan^2(\frac{\pi}{2} \times \frac{f}{f_0})}}{\sqrt{(r_{on} + 1)^2 + (1 + r_{on})^2 \tan^2(\frac{\pi}{2} \times \frac{f}{f_0})}} \tag{4.6}$$

From (4.3)–(4.6), we can find that the insertion loss can be represented as a general form

$$|S_{21}| = |S_{21,SPST}(f, C_{off})| \times |S_{21,topology}(R_{on}, \theta)| \tag{4.7}$$
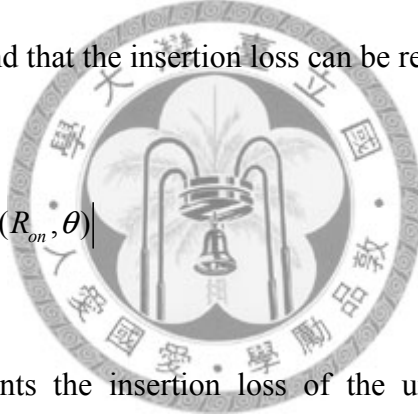
where $|S_{21, SPST}(f, C_{off})|$ represents the insertion loss of the unit switch, and the second term $|S_{21, topology}(R_{on}, \theta)|$ stands for the loss caused by the loading effect according to different topologies described in Fig. 4.1(a)–(d), respectively.

The insertion loss $|S_{21, SPST}(f, C_{off})|$ in each topology from SPST switches is directly proportional to the number of unit switches along a through path from input port to output port. There are three unit switches along a through path for the binary- tree type; the matrix type has one, the net type has two, and the ring-binary type has two unit switches along a through path, respectively. It is observed that the matrix type has the lowest loss from unit switches and the binary-tree type suffers the most. However, the insertion loss resulted from the loading effect $|S_{21, topology}(R_{on}, \theta)|$ cannot be ignored. The switch with larger transistors can suppress the loading effect better because of the smaller parasitic resistor, but the performance of a unit switch would degrade

due to the larger parasitic capacitor. To suppress insertion loss for each topology, we can choose the proper device size to compensate the loss caused by the unit switches and loading effect.

To summarize insertion losses for the four types of multipleport switches, the loss of a unit switch $|S_{21, \text{SPST}} (f, C_{\text{off}})|$ is denoted by α (dB), and we denote β_n as the loading effect $|S_{21, \text{topology}} (R_{\text{on}}, \theta)|$ of shunt n (n = 1,2,3,4) quarter-wavelength transmission lines in decibels, respectively. β_2 is approximately $2\beta_1$, β_3 is approximately $3\beta_1$, and β_4 is approximately $4\beta_1$.

4.4 Analytical Derivation of Bandwidth of Multiple-Port Topologies

The frequency response of an SPST switch can usually cover many octave bandwidths [25], and the restriction of the bandwidth of a multiple-port switch is mainly dominated by its topology. Therefore, in the derivation, it is assumed that the loss of a SPST switch is constant over the band. Hence, the 1-dB bandwidth can be determined by solving

$$\left| S_{21,topology} (R_{on}, \theta) \right|^2 = 0.8 \tag{4.8}$$

The 1-dB bandwidth of each topology is defined as

$$\text{BW} = f_2 - f_1 \tag{4.9}$$

where f_2 denotes the upper 1-dB frequency and f_1 denotes the lower 1-dB frequency.

Since the imperfect normalized resistor r_{on} is much less than 1, to simplify the analysis, we

ignore the high-order terms of r_{on}. By substituting (4.3) into (4.8), the 1-dB bandwidth of the binary-tree type is obtained as follows:

$$\text{BW}_a = 2f_0\left(1-\frac{2}{\pi}\tan^{-1}\left[\frac{5+18r_{on}+\sqrt{25+188r_{on}}}{2(1-12r_{on})}\right]^{1/2}\right) \tag{4.10}$$

Similarly, the 1-dB bandwidths of other topologies are

$$\text{BW}_b = 2f_0\left(1-\frac{2}{\pi}\tan^{-1}\left[\frac{10+28r_{on}+\sqrt{110+448r_{on}}}{2(1-16r_{on})}\right]^{1/2}\right) \tag{4.11}$$

$$\text{BW}_c = 2f_0\left(1-\frac{2}{\pi}\tan^{-1}4\sqrt{\frac{1+r_{on}}{1-16r_{on}}}\right) \tag{4.12}$$

$$\text{BW}_d = 2f_0\left(1-\frac{2}{\pi}\tan^{-1}\left[\frac{5+18r_{on}+\sqrt{25+188r_{on}}}{2(1-12r_{on})}\right]^{1/2}\right) \tag{4.13}$$

From (4.10)–(4.13), the 1-dB bandwidths of binary-tree type (BW_a) and ring-binary type (BW_d) are the same.
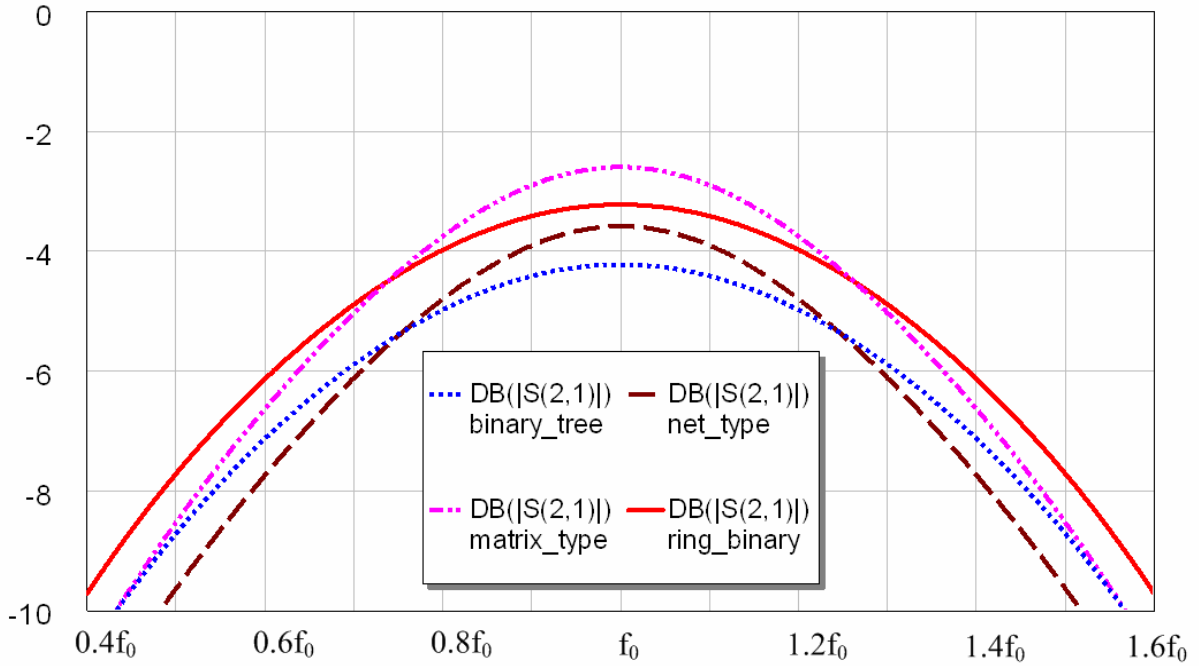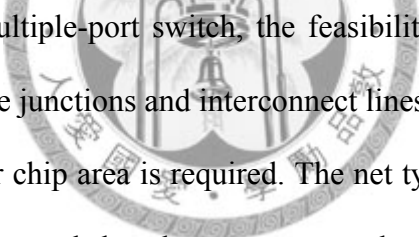
Fig. 4.4. Calculated frequency responses with respect to different topologies

Frequency responses of different topologies for insertion loss and bandwidth according to (4.3)–(4.6) are plotted in Fig. 4.4. It is noted that, in Fig. 4.4, R_{on} is set to be 5Ω in solving these equations, which is reasonable for an MMW switch in the GaAs HEMT process [25]. The loss α of each unit switch is mainly affected by off-state capacitances of HEMTs. In solving these equations, α is assumed to be 1 dB by considering that the reasonable C_{off} in the GaAs HEMT process [25] would lead to such an amount loss. From Fig. 4.4, we observe that the matrix type has the lowest insertion loss, and the binary-tree type has the highest insertion loss. The bandwidth of the binary-tree type and ring-binary type are better than the other two topologies. Owing to the severe loading effects, the bandwidths of the net type and matrix type are narrower than those of the other two types.

56

4.5   Isolations of Multiple-Port Topologies

Isolations can be approximately decided by the number of off-state unit switches that a signal undergoes from input port to output port, and this approximate evaluation would help a lot when we design switches. For the binary-tree type, the number of off-state unit switches between each port is one, two, or three. We denote the isolation that an off-state unit switch can provide as *ISO* (dB).

4.6   Summary of Topology Analysis

To implement a realistic multiple-port switch, the feasibility of layout should also be taken into consideration. There are more junctions and interconnect lines for binary-tree type, matrix type, and ring-binary type, and a larger chip area is required. The net type would be more compact since there is only a junction. It is observed that the net-type topology needs the least number of unit switches, only six, and the other topology requires eight unit switches.

Table 4.1 shows the comparison between different multiple-port switch topologies. Insertion loss, isolation, bandwidth, and the required number of unit switches are summarized. Each topology has its own merits. Since good isolation is much easier to achieve than low insertion loss, regardless of the greatest isolation of binary-tree type, we can find that the ring-binary-type topology is optimal for a broadband and low-loss multiple-port switch design. For narrowband multiple-port switch design, the net-type topology is adopted since the reduced number of composed unit switches would make this multiple-port switch much more compact than others.

Table 4.1

SUMMARY OF DIFFERENT MULTIPLE-PORT SWITCH TOPOLOGY

Topology	Binary-tree	Matrix type	Net type	Ring-binary
Insertion loss	$3\alpha + 3\beta_1$	$\alpha + 4\beta_1$	$2\alpha + 4\beta_1$	$2\alpha + 3\beta_1$
Isolation	*ISO*, 2×*ISO*, or 3×*ISO*	*ISO*	*ISO*	*ISO*, or 2×*ISO*
1-dB bandwidth	Broad (50%)	Narrow (30%)	Narrow (30%)	Broad (50%)
Number of unit switches	8	8	6	8

Chapter 5 Design of Millimeter-Wave Multiple-Port Switches

In this chapter, two MMW multiple-port switches using net-type topology and ring-binary-type topology, respectively, are realized to verify the analysis in chapter 4. The net-type multiple-port switch is designed by Dr. Shih-Fong Chao and the ring-binary-type multiple-port switch is designed by the author of this thesis.

5.1   MMIC Process
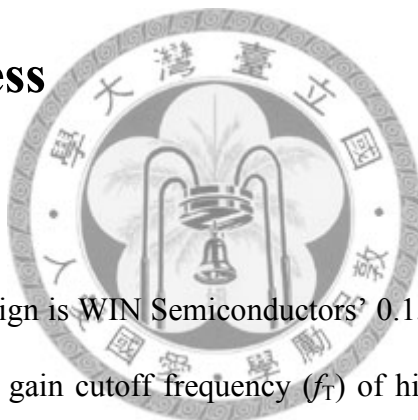
The process used in this design is WIN Semiconductors' 0.15- μm GaAs pHEMT. The HEMT device has a typical unit current gain cutoff frequency (f_T) of higher than 85 GHz and maximum oscillation frequency (f_{max}) of higher than 120 GHz at 1.5-V drain bias with peak dc transconductance (G_m) of 495 mS/mm [44]. The gate–drain breakdown voltage is approximately 10 V, and the gate-to-source voltage at peak transconductance at 1.5-V drain–source voltage is 0.45 V.

These HEMTs are biased in the passive mode, and we model their passive small-signal equivalent circuit as on state and off state. The on-state model is represented as an inductor series with a resistor, and the off-state model is represented as an inductor series with a resistor and capacitor [27]. The gate of the on-state HEMT is biased at 0 V, and the gate of the off-state HEMT is biased at 3 V.

5.2 Design of Unit Switch Cells

The distributed unit switch with wideband characteristics [25] and a filter-integrated unit switch [32] are used for discussion in this section. A circuit schematic of the distributed unit switch is shown in Fig. 5.1. When the HEMTs are turned off, the periodically loaded off-state capacitor along with the inductive transmission line form an artificial transmission line of 50Ω to pass the RF signal. When the HEMTs are turned on, the input node presents a low impedance. To form a multiple-port switch, a 50-Ω quarter-wavelength transmission line is needed to connect at the front of each SPST cell to transform from low impedance to high impedance at the isolated arm.

Fig. 5.2 shows the schematic of a unit filter-integrated switch. The filter-integrated unit switch contains two HEMTs, two short stubs, and an interconnect transmission lines. At V_g = -3 V, the shunt HEMTs are turned off, the short stubs are designed to resonate with the capacitance of the off-state HEMT to let the RF signal pass. At V_g = 0 V, the shunt HEMTs are turned on, a low-impedance value will be seen from the input, and a quarter-wavelength transmission line section will be needed to transform from low to high impedance when being isolated. This filter-integrated unit switch is designed as the maximally flat type filter of third order.
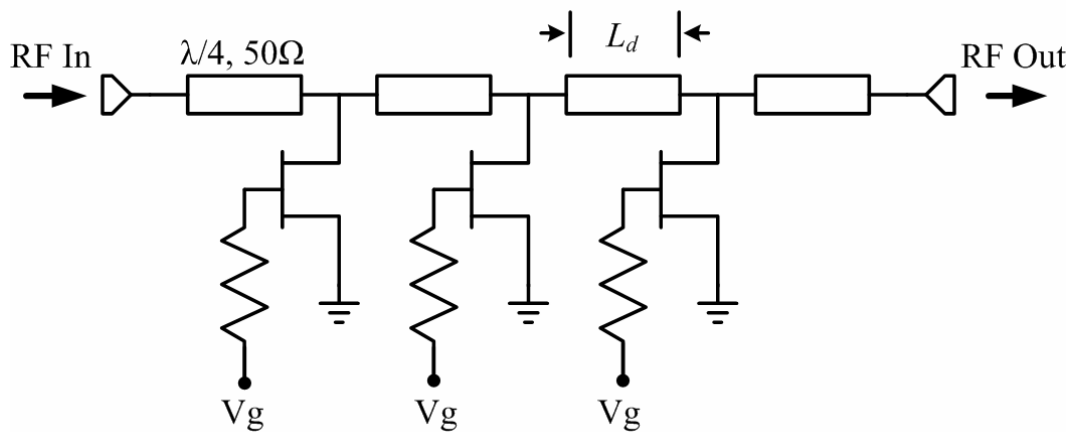
Fig. 5.1. Circuit schematic of a distributed unit switch.
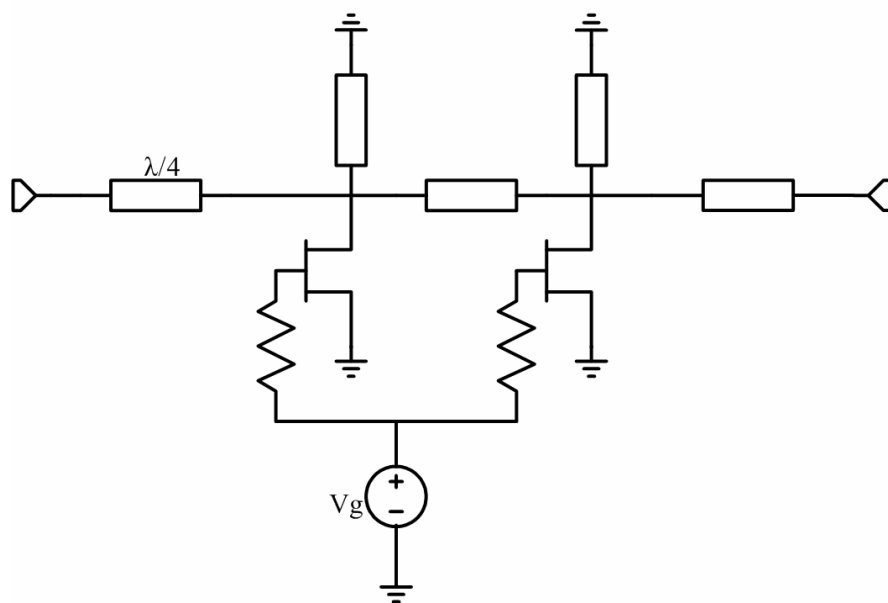
Fig. 5.2. Circuit schematic of a filter-integrated unit switch.

The distributed unit switch is designed with characteristics of insertion loss of 0.75–1 dB and isolation better than 25 dB, and the filter-integrated switch with characteristics of insertion loss of 0.5–1 dB and isolation better than 30 dB. Since there is loading effect, β_1 is approximately 0.5 dB, β_2 is approximately 1 dB, and β_4 is approximately 2 dB.

Based on the topology discussion for net type and ring-binary type in chapter 4, insertion

losses of the six-port switch are expected at approximately 3.5–4 and 3–3.5 dB, respectively. Isolations of two switches are expected better than 25 and 30 dB, respectively.

5.3   Millimeter-Wave Multiple-Port Switches Design

Based on the unit switches designed above, we substitute the distributed-type and filter-integrated unit switches into the topology of net type and ring-binary type, respectively, in order to verify the performances of a multiple-port switch, which can be predicted by both its topology and the unit switch as the analysis we have proposed.

Fig. 5.3 shows the circuit schematic of the 60-GHz net-type six-port switch, which is formed by distributed-type SPST switches, and it was designed by Dr. Shih-Fong Chao [45]. The six SPST switches are combined via a symmetric six-way matching junction to form a six-port switch. At the isolated ports, the HEMTs at the isolated arms are turned on, and will show a low impedance value at the interface of the six-way junction. The low impedance will be transformed into high impedance at the center of the matching junction to block the RF signal. At the thru-ports, the shunt HEMTs at the thru-arm are off. The off-state capacitors then periodically load the inductive transmission line (linewidth = 10 μm) at an optimal length (L_d = 108 μm) to form an artificial transmission line of 50 Ω. The RF signal will then pass through the input thru-port to the output thru-port via the six-way matching junction. The six-way matching junction is formed by six 50-Ω transmission lines with taper shape at the connected interface to reduce the discontinuity effects. The advantage of the proposed multiple-port switch is that each port of the six ports could be an input port or an output port. The concept can also be applied to design switches with a different number of ports. Compared with the multiple-port switch formed by directly connecting the single-pole–double-throw (SPDT) ones, the other advantage of using a six-way matching junction
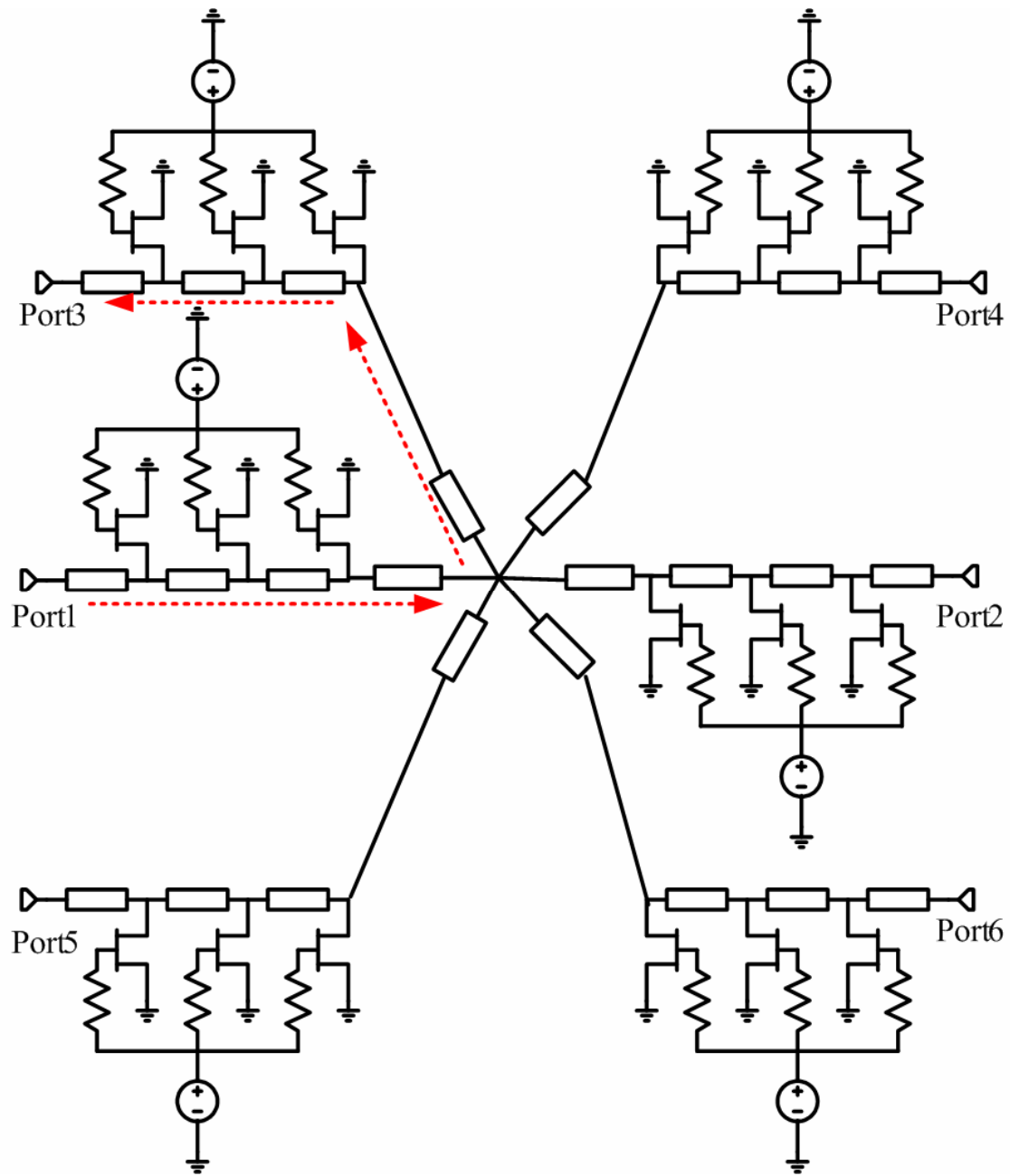
Fig. 5.3. Schematic of MMW multiple-port switches: net-type topology based on distributed switches.

is that the total chip size can be significantly reduced.

Fig. 5.4 shows the schematic of the 60-GHz six-port switch using a ring-binary topology with filter-integrated unit switches. In this design, since each unit switch consists of only two HEMTs less than three HEMTs of the distributed-type switch, the insertion loss can be reduced. Moreover,
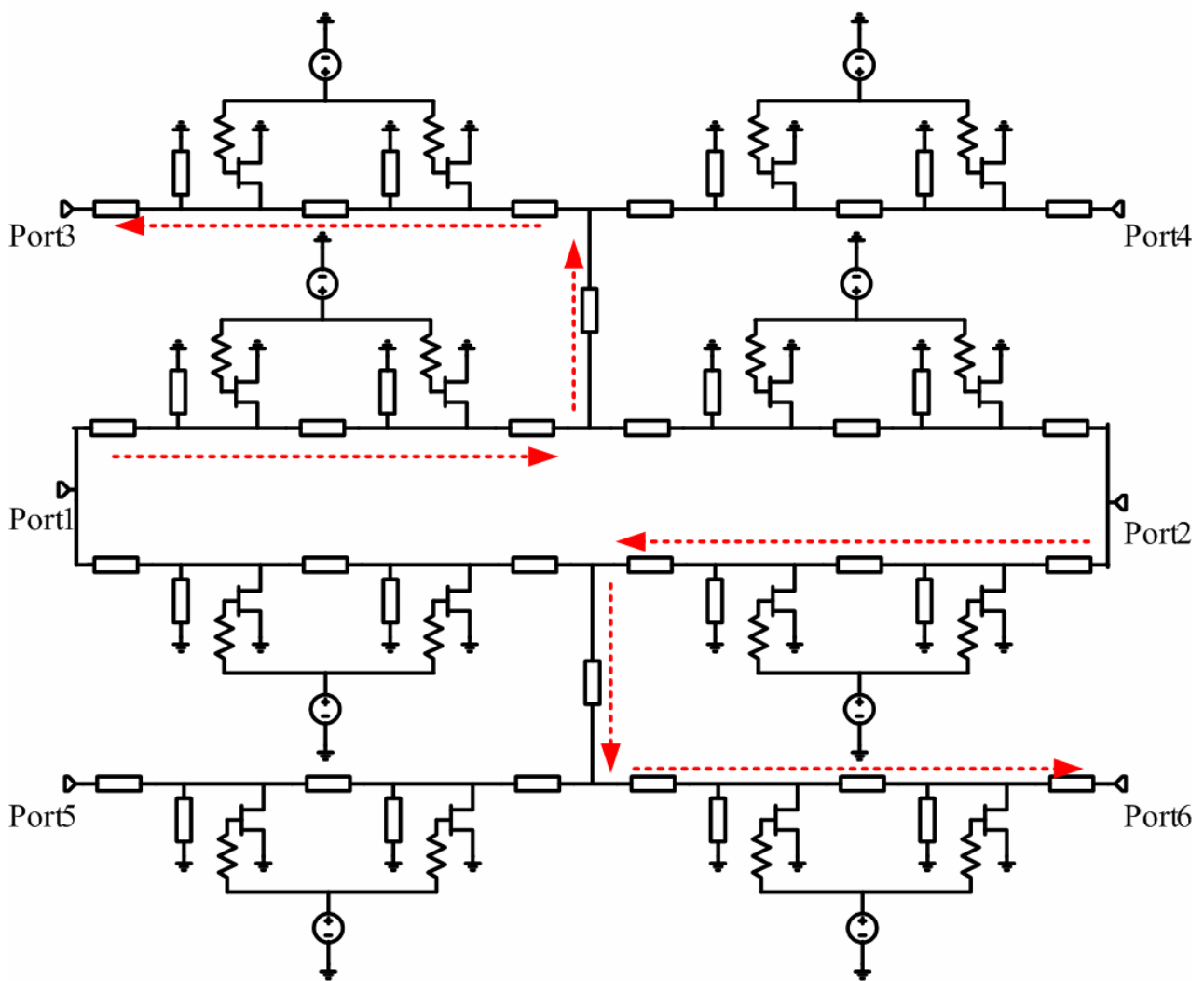
Fig. 5.4. Schematic of MMW multiple-port switches: binary-ring topology based on filter-integrated switches.

the filter-integrated switch can provide better isolation than that of the distributed-type switch at the same number of stages. Thus, the two-stage filter-integrated switch provides better insertion loss and isolation. Although the control logic in Fig. 5.4 is more complex than in Fig. 5.3, this six-port switch can also function as two independent SPDT switches simultaneously.

Fig. 5.5 shows chip photographs of these two six-port switches. Fig. 5.5(a) is the distributed-type switch, which has a chip size of 2.0×1.5 mm^2. The filter-integrated switch is shown in Fig. 5.5(b), and the chip size is 2.5×2.0 mm^2.

5.4   Experimental Results

The two multiple-port switches are measured via on-wafer probing. An HP8510 network analyzer is used to measure the S-parameters below 50 GHz with an additional V-band test set for 50–75 GHz. It is noted that since there two ports are on the same side of the chip, it is difficult to terminate all the measuring port with 50-Ω during testing. Thus, some isolated ports were left open during testing. In fact, the isolated ports that were left open will not affect the other ports under measuring because the high impedance of the un-terminated ports will be isolated by the shunt small on-state resistors on the isolated arm.

Consider the net-type six-port switch in Fig. 5.5(a), due to its physical layout, two different insertion losses will be obtained at the output ports (S_{31}, S_{41}). The measured insertion loss and input return loss when port1 and port3 are in the on state (S_{31} and S_{11}) are shown in Fig. 5.6(a), and the measured insertion loss and input return loss when port 1 and port 4 are in the on state (S_{41} and S_{11}) are shown in Fig. 5.6(b). he measured insertion losses at thru-ports are 4–5 dB in 48–65 GHz. The measured isolations of the isolated ports are shown in Fig. 5.6(c).Except for port 3 and port 4 which are measured as thru ports, the other ports are measured as isolated ports. Therefore, three kinds of isolations (S_{21}, S_{51}, and S_{61}) were measured, and the measured results are shown in Fig. 5.6(c). The discontinuous measured points at 50 GHz are due to the measurement instrument which has to be operated in DC-50 GHz and 50-75 GHz separately.

The measured results of the ring-binary-type multiple-port switch are shown in Fig. 5.7. The through path is port1 to port3. Therefore, S_{31} is the insertion loss, and the other port to port transmission coefficients are isolations. The measured insertion loss (S_{31}) is 3–4.5 dB with isolation
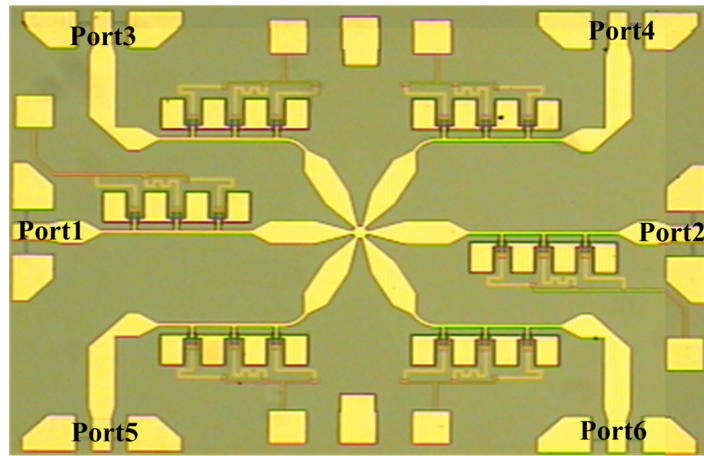
(a)
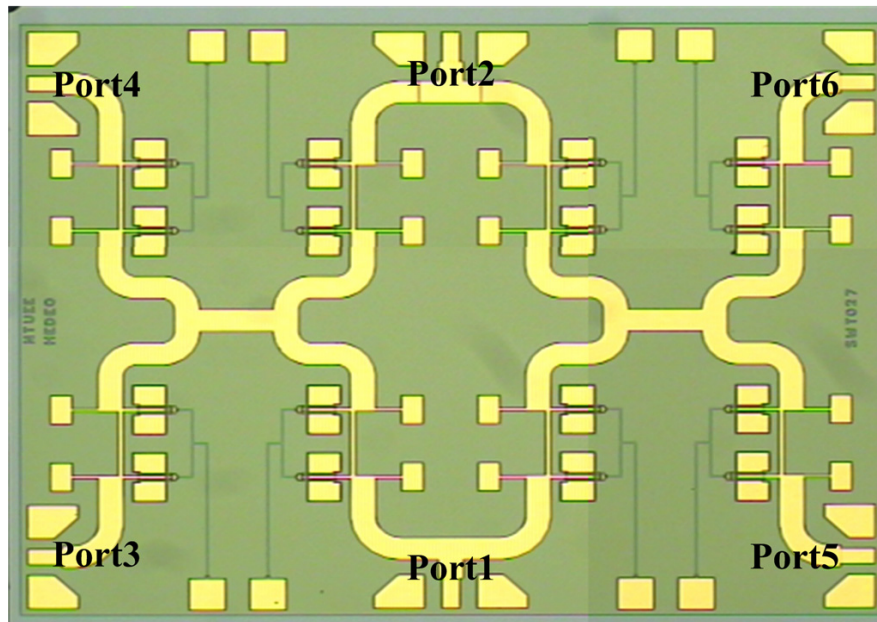
(b)

Fig. 5.5. Chip photograph of the six-port switches. (a) Net-type topology with a size of 2.0×1.5 mm^2. (b) Ring-binary topology with a size of 2.5×2.0 mm^2.

better than 30 dB at 43–66-GHz. Since a filter-integrated unit switch is used to implement in this topology, a filter-like frequency response of return losses can be observed in Fig. 5.7 (b). Similarly, three kinds of isolations (S_{21}, S_{41}, and S_{51}) were measured, and the measured results are shown in Fig. 5.7 (c)

Comparing the measured data with the calculated results shown in Table 4.1, it can be

observed that the distributed unit switch is designed with an insertion loss α of 0.75–1 dB, isolation *ISO* better than 25 dB, and the loading effect ($4\beta_1$) in the net-type topology is approximately 2 dB. Therefore, in the net-type topology, the insertion loss is expected to be approximately 3.5–4 dB with isolations better than 25 dB, and 1-dB bandwidth is expected to be 30%. Furthermore, the filter-integrated unit switch is designed with characteristics of loss α of 0.5–1 dB, isolation *ISO* better than 30 dB, and the loading effect ($3\beta_1$) is approximately 1.5 dB. For the same reason, in the ring-binary-type topology, the insertion loss is expected to be approximately 3–3.5 dB with isolations better than 30 dB, and 1-dB bandwidth is expected to be approximately 50%. The measured results agree well with the predicted results from (4.3)–(4.13).

We also tried to measure the power compression performances of the switches. The performances of P_{out} versus P_{in} were measured using a *V*-band power source and power sensor. Due to the limitation of our input power source, the maximum input power is 17 dBm at 60 GHz as shown in Fig. 5.8. However, the power compression is not observed for both the switches under 17-dBm input power. There are about 2-dB differences between simulation and the measured data. The simulation for power performance in Fig. 5.8 is based on the large signal model provided by the foundry. However, there is much difference between the simulated and measured power because the passive mode of both the large-signal model and small-signal model provided by the foundry are not accurate enough. Therefore, we generated the small signal model based on the measured device S-parameters instead, for our simulation.

These measured results show that when a unit switch is designed, the limitation of performance of a multiple-port switch will be affected significantly by its topology. From the measured results of the net-type six-port switch, the bandwidth and insertion loss are significantly degraded compared with an SPDT switch. This is mainly due to the loading effects of the four isolated arms. The imperfect open of the four parallel isolated arms will absorb some RF power from the thru-ports, and the imperfection becomes more severe when the frequency deviates much

further from the center frequency. Consequently, the RF bandwidth will be narrower. To resolve the loading problem of a net-type six-port switch, several T-junctions are used to replace the six-way matching junction of the net-type switch. The advantage of using a T-junction is that there will be only one isolated arm loaded at each junction; therefore, the loading effect could be significantly reduced. However, the overall circuit size will be increased, as can be observed from Fig. 5.5(a) and (b).

Table 5.1 summarizes the previously reported performances and features of passive MMIC HEMT switches. A resonant-type SPDT switch shows a narrow band in the *V*-band [29], and another SPDT switch shows an insertion loss of 4 dB [30], but our six-port switch shows almost the same insertion loss and wider bandwidth compared with that in [27]. A 1–6-GHz multiple-port switch is also reported using ring-binary topology [29]. However, the synthesis method cannot easily be implemented in MMW frequency.

(a)

(b)

69

(c)
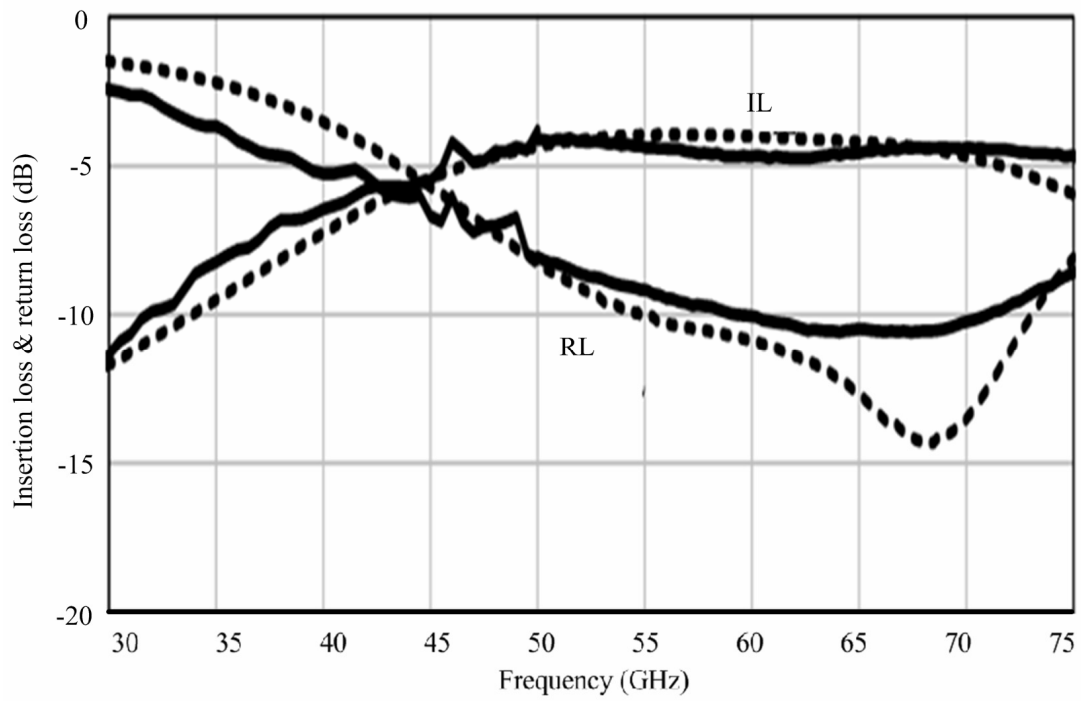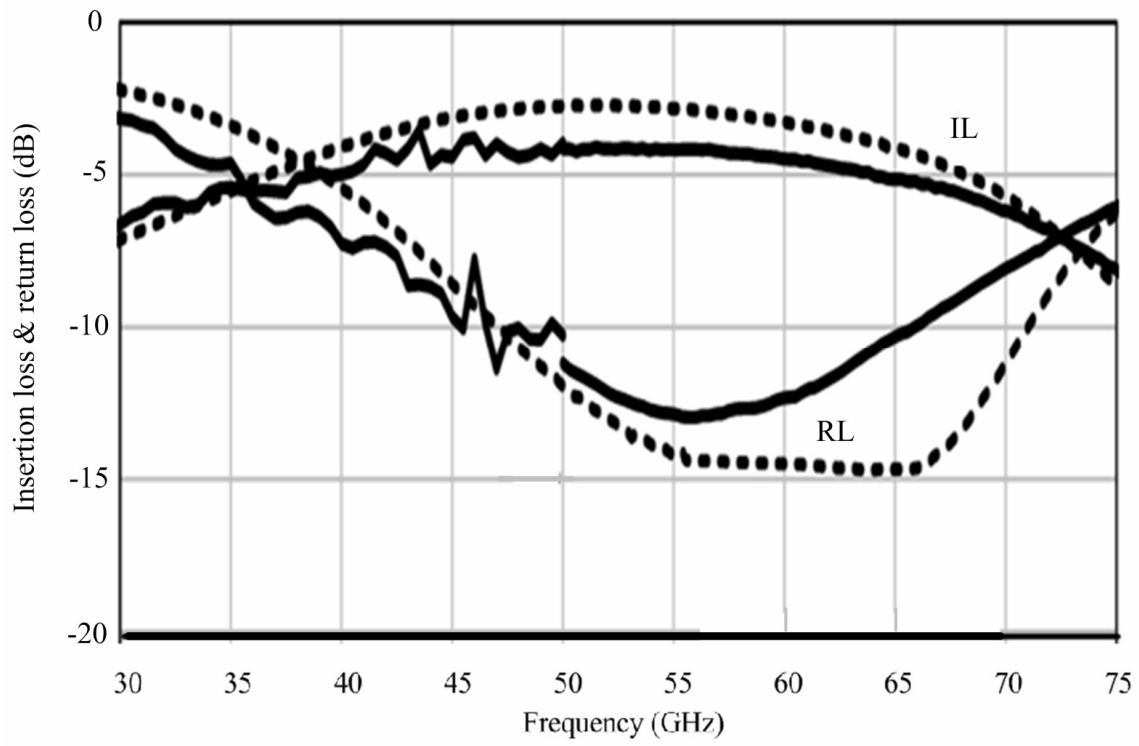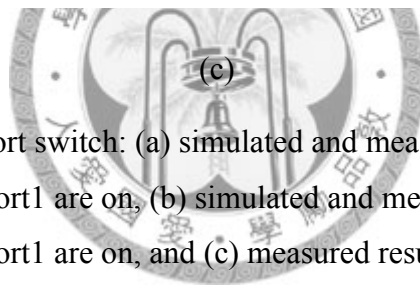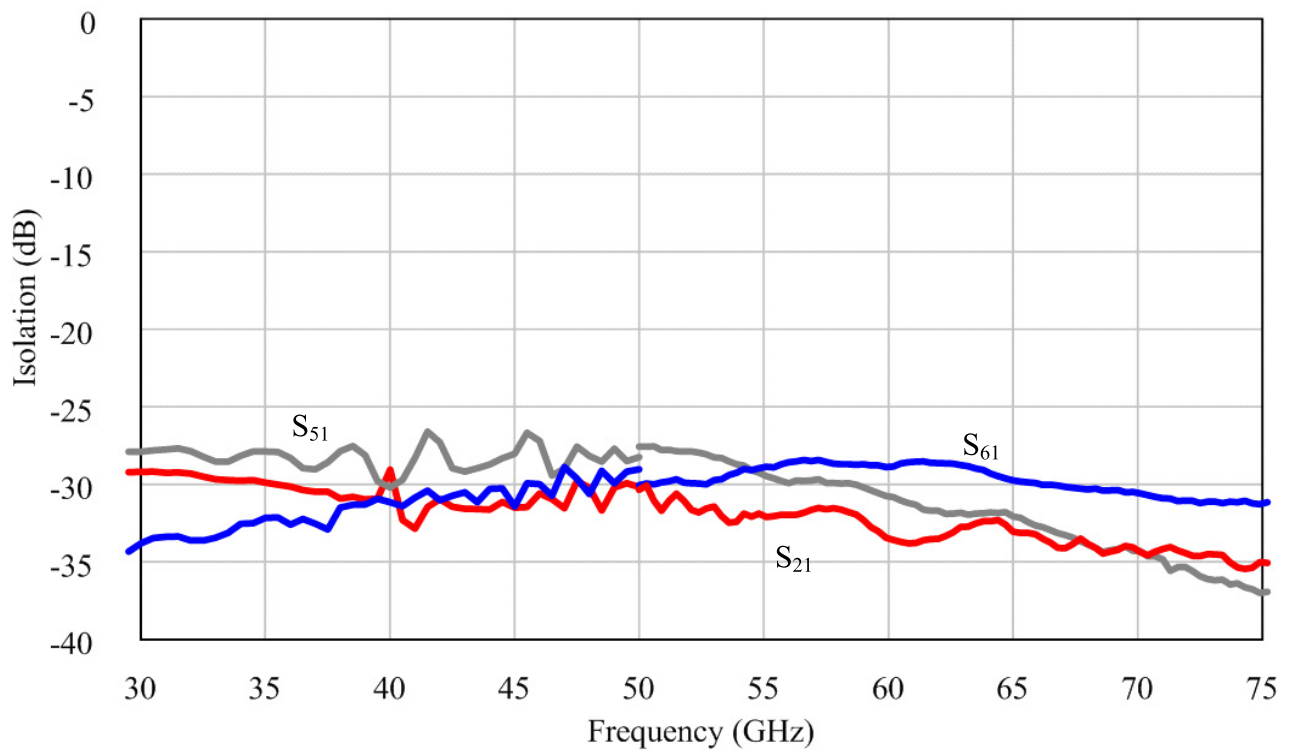
Fig. 5.6. The net type multiple-port switch: (a) simulated and measured results of the insertion loss and return loss when port3 and port1 are on, (b) simulated and measured results of the insertion loss and return loss when port4 and port1 are on, and (c) measured results of port to port isolations.

(a)

(b)

71

(c)
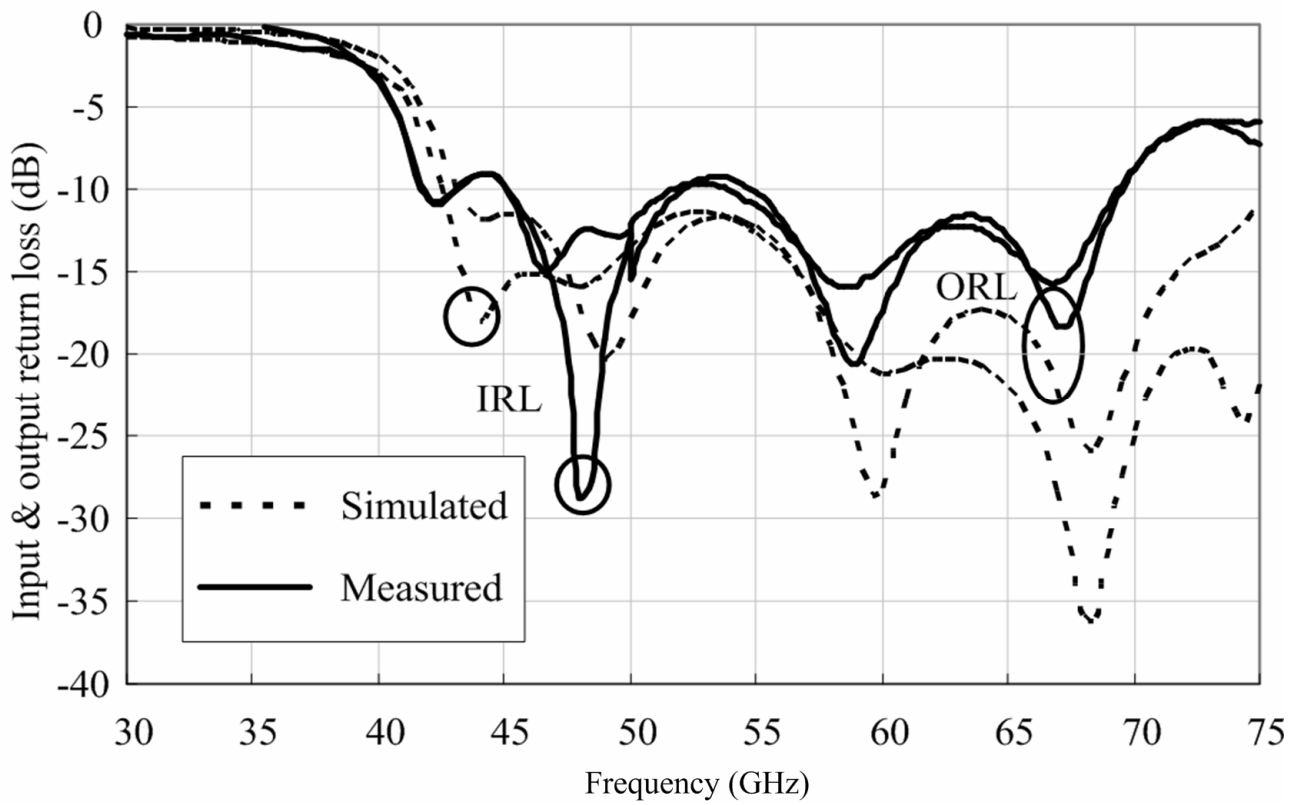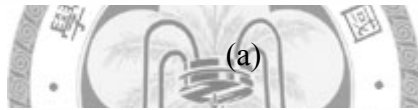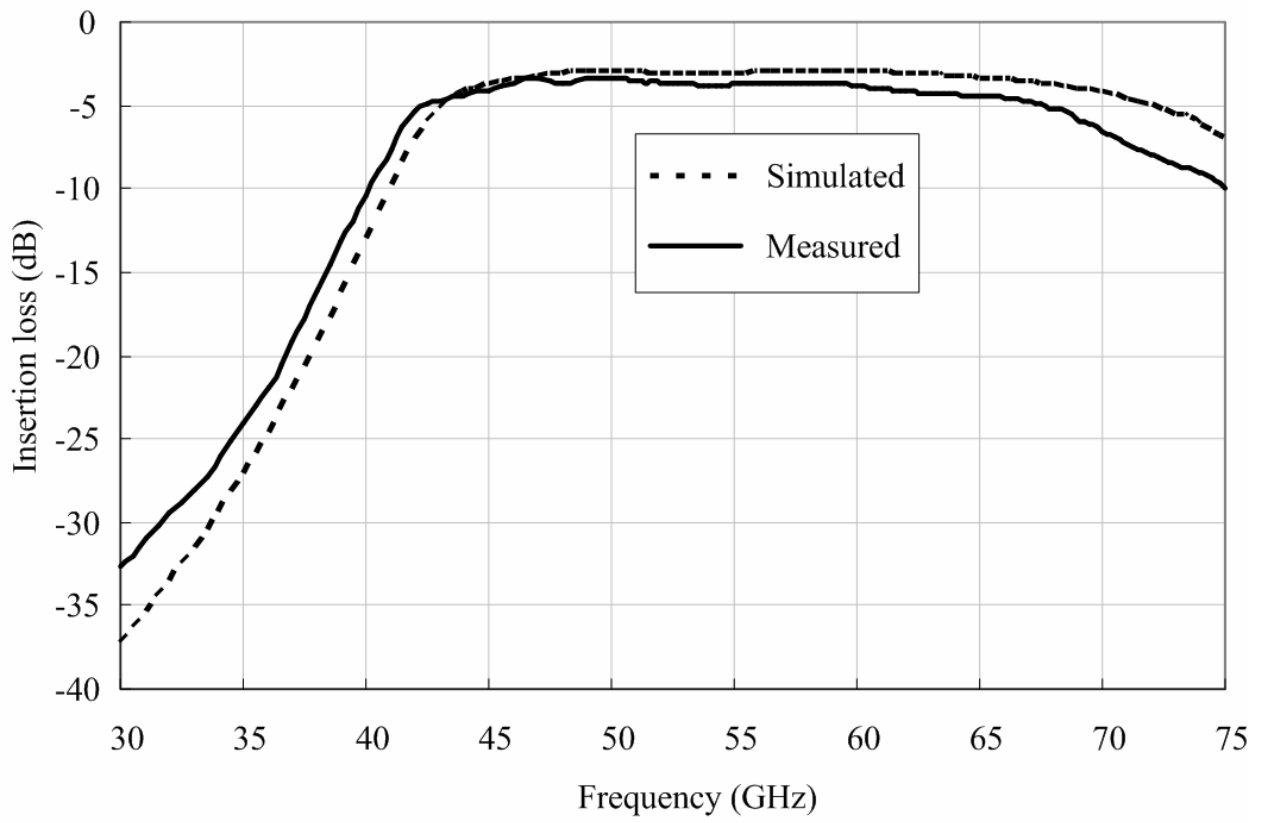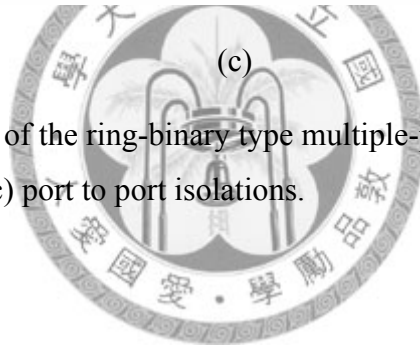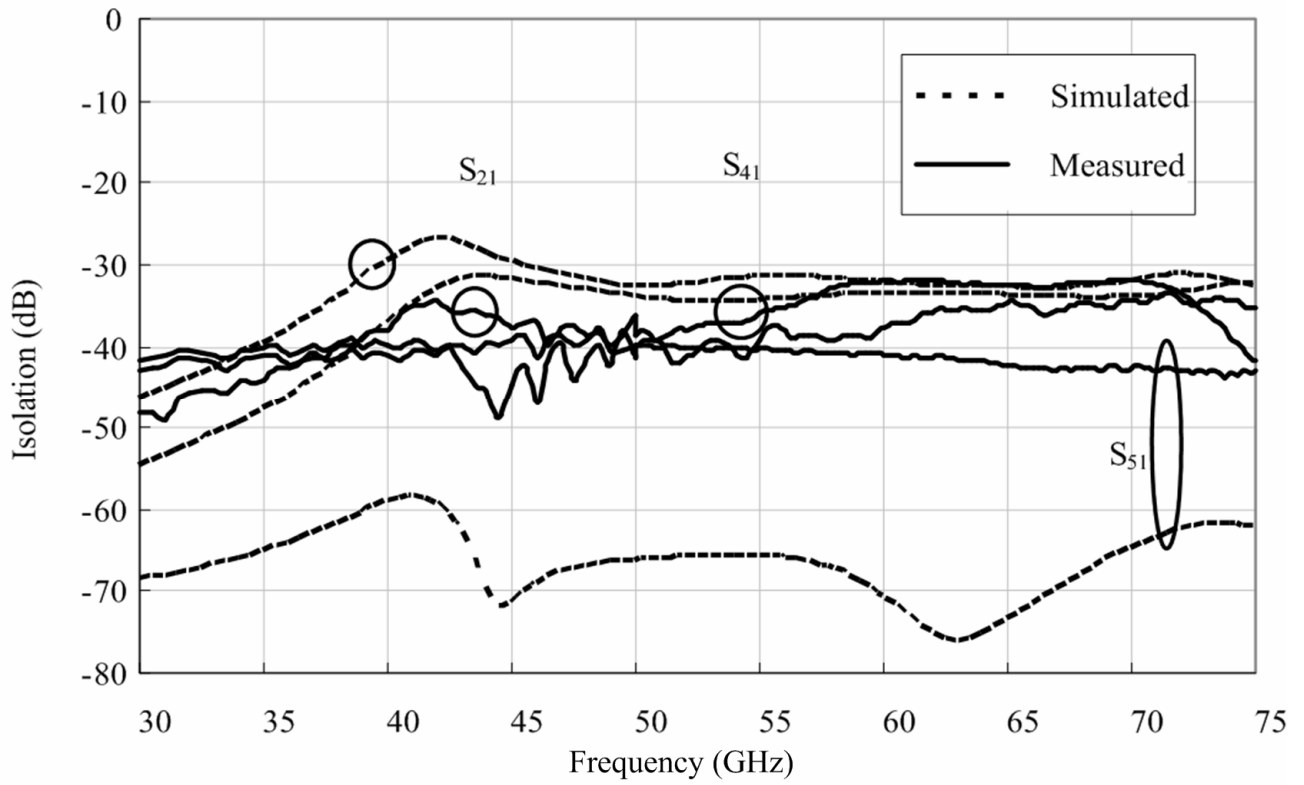
Fig. 5.7 Simulated and measured of the ring-binary type multiple-port switch. (a) Insertion loss, (b) input /output return losses, and (c) port to port isolations.
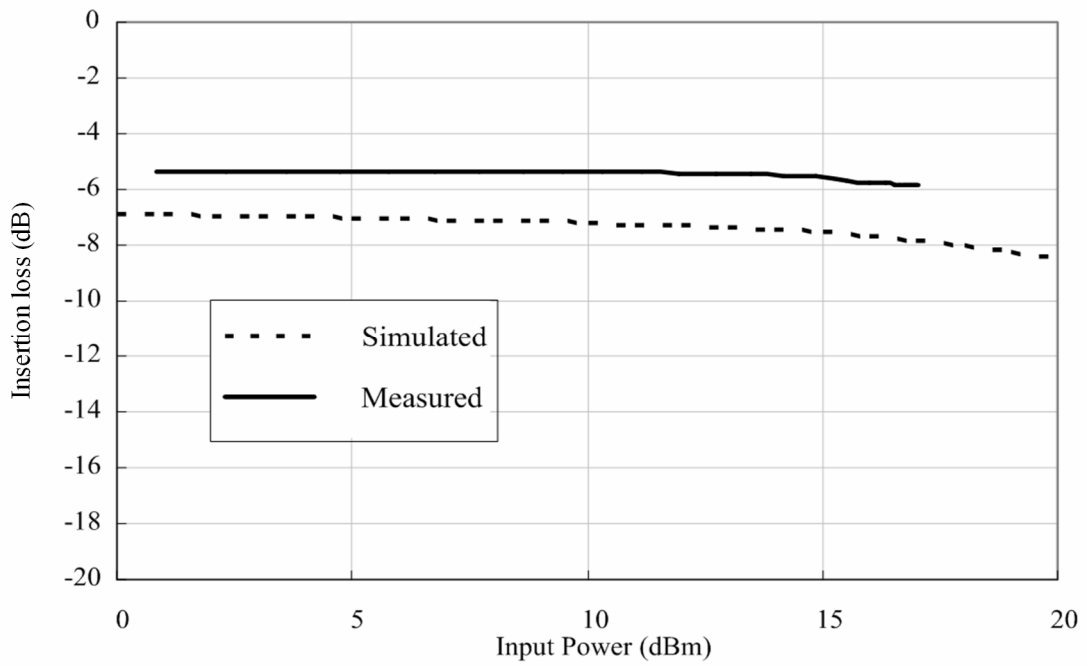
(a)
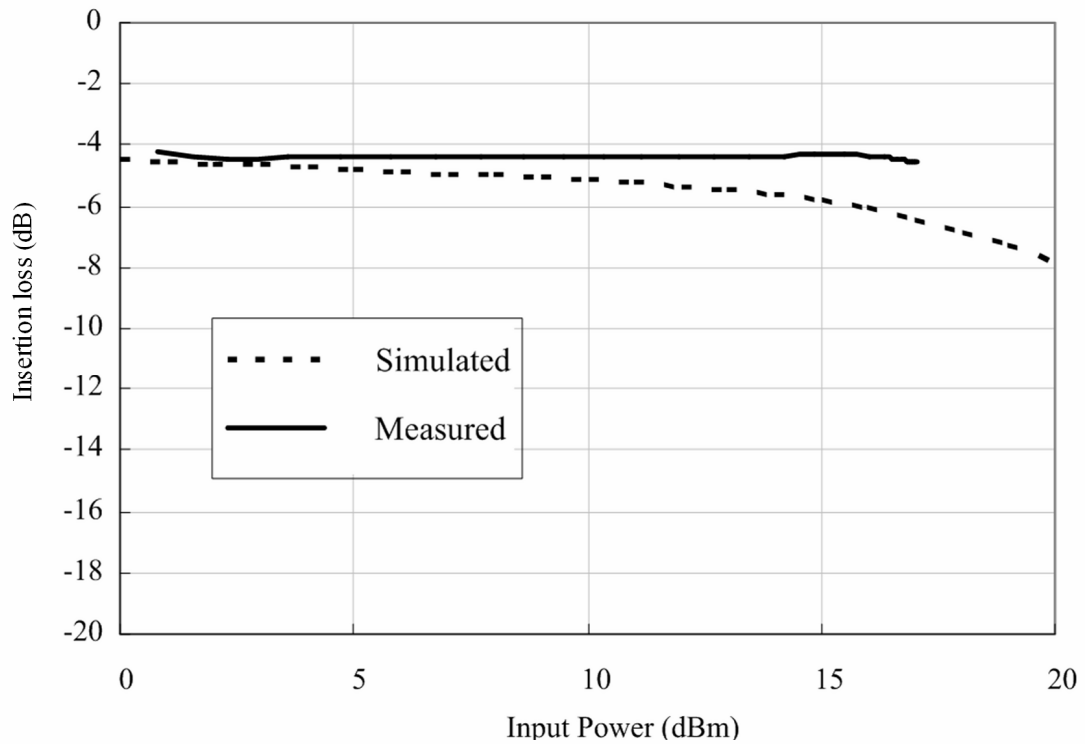
(b)

Fig. 5.8. Simulated and measured insertion loss versus input power at 60 GHz of (a) net-type multiple-port switch, and (b) ring-binary multiple-port switch.

5.5 Summary of Multiple-Port Switches

Different MMW multiple-port switch topologies have been discussed and studied in this chapter. The equations used to predict the performances with respect to different topologies have also been derived. Based on the equations, the insertion losses, isolations, and bandwidth could be analyzed. Besides six-port switches, the analysis also provides the design guideline to design a multiple-port switch in MMW frequency. Two 60-GHz MMIC six-port switches using different topologies have been designed to verity this design approach. The net-type six-port switch has an insertion loss of 4–5 dB with isolation better than 25 dB from 48 to 65 GHz. The other ring-binary-type six-port switch shows an insertion loss of 3–4.5 dB with isolation better than 30 dB in 43–66 GHz. To the best of our knowledge, these two circuits are the first MMIC multiple-port switches demonstrated over 50 GHz.

Table 5.1

Technology	Design Approach	Frequency (GHz)	Insertion Loss (dB)	Isolation (dB)	I/O	Ref.
HEMT	Resonant, series	94	1.6	22.5	SPST	[28]
HEMT	Resonant, series	55 ~ 63	< 3.2	>23	SPDT	[29]
HJFET	Series resonant, shunt	57 ~ 61	3.9 ~ 5	>30	SPDT	[30]
HEMT	λ/4, shunt	42 ~ 46	< 1.6	>30	SPDT	[33]
HEMT	Impedance transformation network, shunt	53 ~ 61	< 4	>30	SPDT	[27]
HEMT	Traveling wave concept	70 ~ 102	3.9 ~ 5.5	>30	SPQT	[34]
HEMT	Series	1 ~ 6	1.2 ~ 1.7	>20	Multiple-port	[39]
HEMT	Filter-integrated	38 ~ 42	< 4	>25	Multiple-port	[43]
HEMT	**Traveling wave concept**	**48 ~ 65**	**4 ~ 5**	**>25**	**Multiple-port**	**This work**
HEMT	**Filter-integrated**	**43 ~ 66**	**3 ~ 4.5**	**>30**	**Multiple-port**	**This work**

Chapter 6 V-band Medium Power Amplifier

6.1   Introduction

Today, the demand of millimeter-wave (MMW) wireless communication systems increases rapidly due to the capability of high data transmission rate, and it makes the design of 60 GHz transceiver an important topic [47]-[49].

To design MMW circuits, GaAs HEMT can achieve high performance, but it is hard to integrate and thus leads to high cost. To achieve low cost, higher integration of wireless transceiver is a necessary trend.   CMOS process is the suitable choice for low cost and high integration. Due to the high operating frequency of MMW circuits, the unit current gain frequency f_T of devices is often regarded as an index for MMW circuits design. Nanometer order CMOS process with higher f_T is capable to operate at MMW frequency; on the other hand, the characteristic of nanometer process with lower drain to source voltage makes these devices poor power handling. Therefore, for System-on-Chip (SoC) transceiver circuits, integration of CMOS PA is the bottleneck due to the poor power handling capability.

Recently, several CMOS 60 GHz power amplifiers have been reported [48], [50]-[52]; from those experimental results, it can be known that power amplifiers in 65 nm CMOS [48] show worse power performance than those in 90 nm CMOS [51]. However, digital circuit takes great advantage in deep sub-micron process such as saving power, higher speed, smaller chip area for low cost, and e.t.c. Therefore, to integrate RF blocks with digital circuits for low cost, design of power amplifiers in 65 nm or in further nanometer process becomes an important issue in the future.
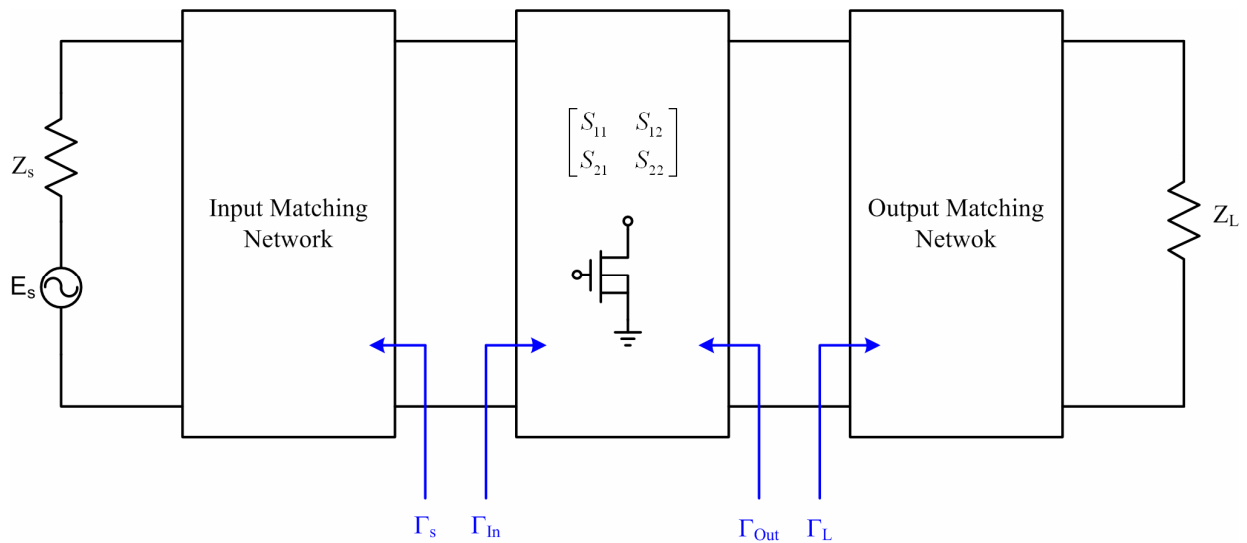
Fig. 6.1. Two-port microwave network.

The only reported 60-GHz power amplifier in 65 nm CMOS shows good power performance; however, it has only 4.5-dB power gain [48], and thus it needs several buffer amplifiers to achieve the link budget for practical 60-GHz wireless transceivers. In this chapter, a power amplifier with power gain better than 10 dB and 9.5-dBm saturation power is demonstrated. Because of the higher gain, it is more functional in 60-GHz transceivers.

6.2 Basic Concepts of Power Amplifiers [46]

Before designing a power amplifier, fundamental concept of microwave amplifiers is presented first. Consider Fig. 6.1, it is a standard two-port microwave network, and it consists of a source E_s with source impedance Z_s, load impedance Z_L, input matching network (Γ_s), output matching network (Γ_L), and one transistor with 2×2 scattering matrix. The transducer power gain of this two-port network is given by:

$$G_T = \frac{1 - |\Gamma_s|^2}{|1 - \Gamma_{In}\Gamma_s|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \qquad (6.1)$$

, or

$$G_T = \frac{1 - |\Gamma_s|^2}{|1 - S_{11}\Gamma_s|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{Out}\Gamma_L|^2} \qquad (6.2)$$

Γ_{In} and Γ_{Out} are given as follows:

$$\Gamma_{In} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \qquad (6.3)$$

$$\Gamma_{Out} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \qquad (6.4)$$

In microwave amplifier design, to achieve the maximum *gain* from source to load, this two-port network needs to satisfy simultaneously complex conjugate matching:

$$\begin{cases} \Gamma_s = \Gamma_{In}^* \\ \Gamma_L = \Gamma_{Out}^* \end{cases} \qquad (6.5)$$

When a microwave network delivers maximum gain from source to load, it does not mean that maximum *power* is delivered to load. The maximum power delivered to load occurs when Γ_L equals to the best load impedance, and the best load impedance varies according to different transistors. The best load impedance can be found by load-pull simulation. After Γ_L is chosen, Γ_L is dealt with

as a constant, and the next step is to design input matching network so that

$$\Gamma_s = \Gamma_{In}^* = \left(S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right)^* \tag{6.6}$$

And the power gain of this power amplifier is:

$$G_P = \frac{1}{\left|1 - \Gamma_{In}\right|^2} \left|S_{21}\right|^2 \frac{1 - \left|\Gamma_L\right|^2}{\left|1 - S_{22}\Gamma_L\right|^2} = f(S_{2\times2}, \Gamma_L) \tag{6.7}$$

A microwave power amplifier can be designed by the described steps. The next section presents the design of 60-GHz power amplifier.

6.3 Design of V-band Medium Power Amplifier

This chip was fabricated in standard bulk 65 nm 1P9M process. This process is with one poly layer for the gates of CMOS transistors, and nine metal layers with ultra-thick metal top metal of 3.4 μm to minimize the RF signal loss. The thin-film microstrip line for this circuit design is composed of signal line realized by the top metal (M9) and the ground plane realized by the bottom metal (M1). Fig. 6.2 shows the simulated insertion loss of thin-film microstrip lines in 65nm CMOS and 90 nm CMOS both with length of 500 μm and characteristic impedance of 50 Ω (width = 7 μm for 65nm CMOS and width = 10 μm for 90 nm CMOS) to compare the passive elements used in these two processes fairly. We can observe that the loss of the thin-film microstrip line in 65 nm is

Loss of Thin-Film Mircrostrip Line
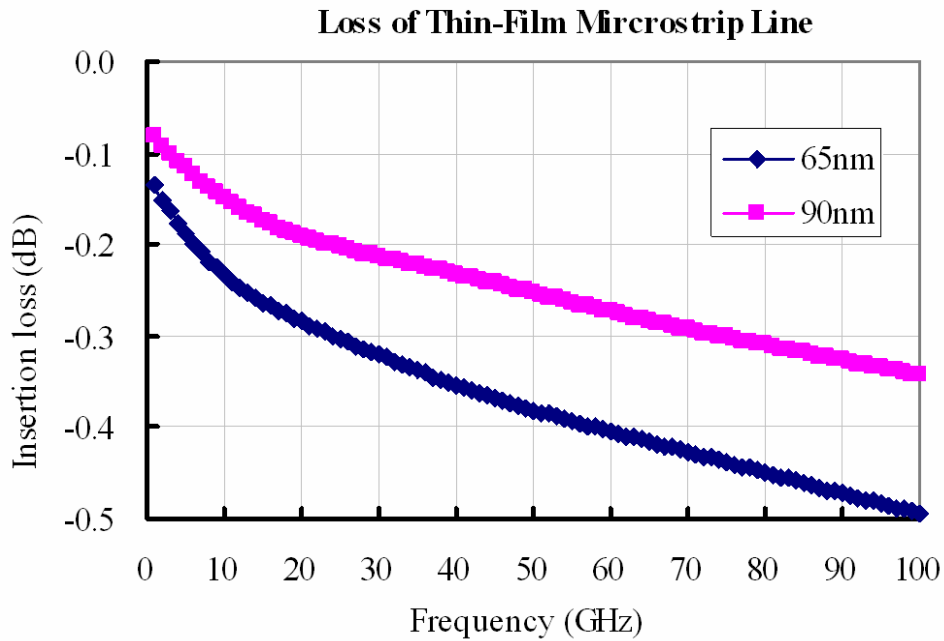
Fig. 6.2. Simulated insertion loss of the thin-film microstrip line with length of 500 μm and characteristic impedance of 50 ohm.

higher than that in 90 nm CMOS in Fig. 6.2 because of the thinner dielectric in 65 nm process. Therefore, the design of amplifiers in 65 nm process encounters much more loss to degrade the gain and output power. The metal-insulator-metal (MIM) capacitor between metal 8 and metal 7 was also used in this design.

To design a power amplifier, the device size of the output stage is most important. A small device size can operate with higher gain due to less parasitic capacitance to degrade the gain at MMW frequency, but it cannot deliver good output power. On the other hand, a large device can deliver good output power, but the gain at MMW frequency is degraded heavily. Thus, the choice of output stage device size between larger size and smaller size should be made carefully. The device size of output stage in this power amplifier is NMOS of the total gate width of 160 μm and finger of 32.

Fig. 6.3 shows the schematic of this 60-GHz power amplifier. This power amplifier is composed of cascading three stages of cascode amplifiers. The cascode amplifier architecture is

adopted to boost the gain and power of each stage, since the common source structure of the NMOS of the total gate width of 160 μm and finger of 32 only has G_{max} only 4 dB, and the matching thin-film microstrip line must degrade the gain heavily.

To achieve higher output power and enough gain, the device size of the output stage is chosen that the G_{max} of the cascode structure of the output stage is 8 dB as shown in Fig. 6.4. Consider the chosen device size of the output stage, load-pull simulation for power match and complex conjugate simulation for gain match were conducted as in Fig. 6.5. From Fig. 6.5, we can observe that the best location for power match in Smith chart is close to complex conjugate point at 60 GHz. Furthermore, due to the locations of them are both in the left upper part of Smith chart, it means that simply a short stub will be quite suitable to make the matching transform of 50-Ω load to the location between power contour and complex conjugate point to balance power and output return loss. Therefore, the output matching was completed by simply a short stub as shown in Fig. 6.3.

The first stage device of the cascode amplifier is NMOS of the total gate width of 20 μm with 5 fingers. The second stage device is NMOS of the total gate width of 80 μm with 20 fingers. The output stage device is NMOS of the total gate width of 160 μm with 32 fingers. This means the chosen device ratio is 1:4:8 for power, because in our simulation, the first, the second, and the output stage shows the gain about 7 dB, 7 dB, and 4 dB, respectively. This device ratio makes sure that each stage can have enough gain to drive the next stage. Each stage is operated under 2 V supply with 1 V drain to source voltage, and the current of the output stage is 54 mA. Fig. 6.6 is the chip photo of this power amplifier, and it is with the size of 0.35 mm^2.
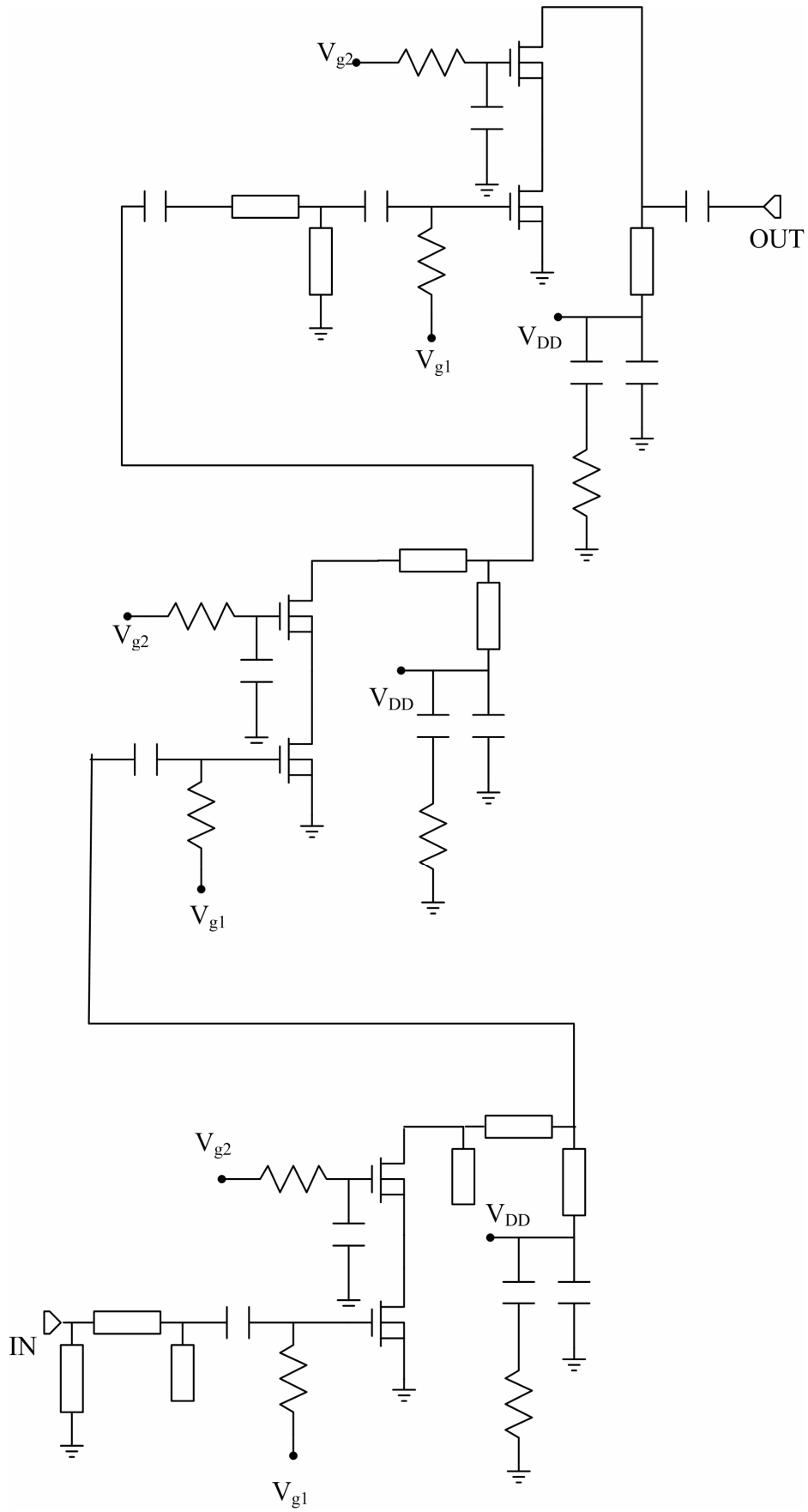
Fig. 6.3. Circuit schematic of the 60-GHz PA.
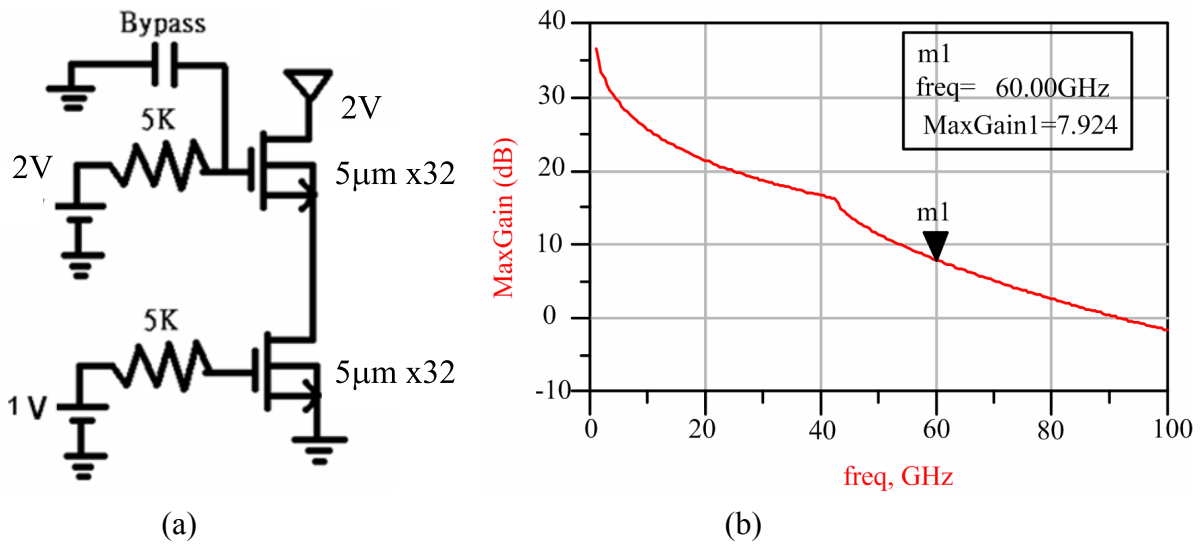
Fig. 6.4. Device selection of output stage. (a) Output stage structure, and (b) G_{max} of the output stage.
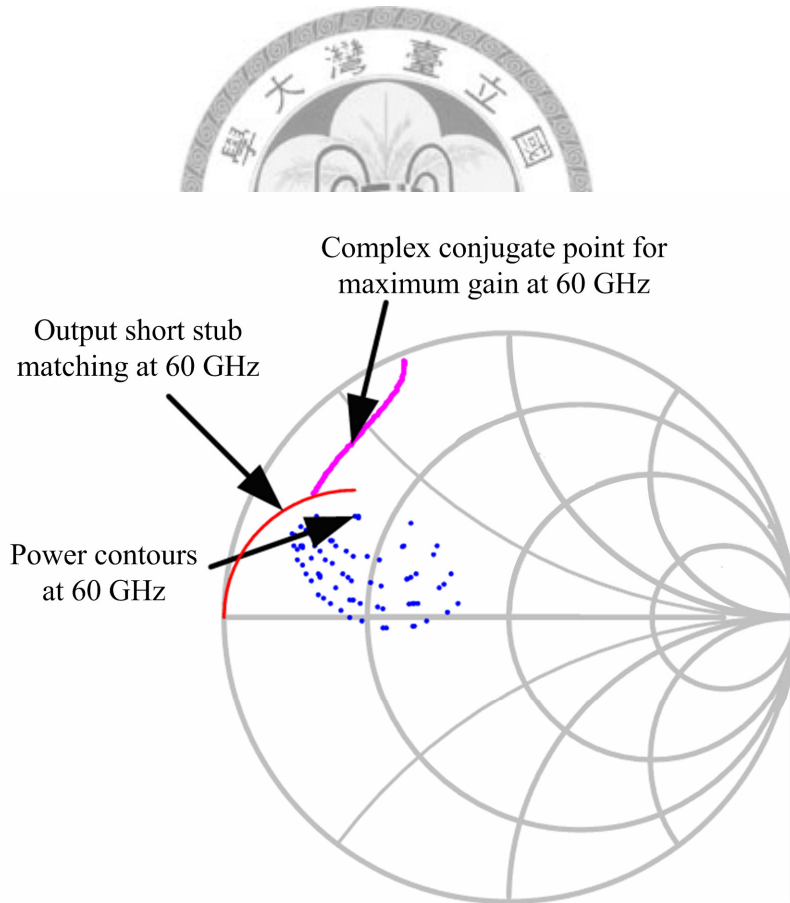
Fig. 6.5. Power contours, complex conjugate point, and output short stub matching at 60 GHz.

6.4　Experimental Results

This 60-GHz CMOS power amplifier was measured on-wafer probing. An HP8510 network analyzer is used to measure the S-parameters with an additional V-band test set. This circuit was biased at $V_{DD} = 2V$, and each device has 1-V drain to source voltage to make sure that each chip is with good yield. In our measurement, this bias condition does not make any chip beak down.

Fig. 6.7 shows the preliminary simulated and measured S-parameters for this 60-GHz power amplifier. There is about 4 GHz frequency shift between simulated and measured S-parameters. Besides, the measured gain is lower than the simulated gain by 5 dB. After the layout and the simulation file were checked and they were consistent, it was guessed that the parasitic capacitance of the model of the NMOS is underestimated, since the device size in the design of PA is relatively larger and the model of the larger device is usually not precise as the smaller one. After adding C_{gs}, C_{gd}, and C_{gs} of the order of 10 fF to compensate the underestimated parasitic capacitance of NMOS, the re-simulated results compared with measured results are shown in Fig. 6.8. The simulated input return loss and output return loss are quite similar to the measured results. However, the measured gain is still less than the simulated gain about 3.5 dB. This PA has a measured peak gain of 14.7 dB at 56 GHz, and the gain over 10 dB for 51-61 GHz. In addition, it has minimum input return loss and output return loss of 18 dB and 22 dB, respectively. The input return loss is better than 10 dB in 52-66 GHz, and the output return loss is better than 10 dB in 50-58 GHz.

Fig. 6.9 shows the simulated and the measured output powers versus the input powers at 60 GHz, and it shows that this PA has the measured saturation output power about 9.5 dBm. Besides, this PA still has the measured gain over 10 dB when measured output power is 5 dBm. Since the

measured gain is less than the simulated gain about 3 dB, the measured power is also less than the simulated power by the same quantity. Because the measured return losses achieve good agreement with simulated return losses and the shape of the simulated gain and the measured gain are similar, maybe some losses are underestimated in passive components. Another possibility is that since the PA requires larger devices, the parasitics or g_m of models of larger devices might not be accurate.

However, the power performance of 1-dB compression point appears about $P_\mathrm{out} = 2$ dBm, because regardless of the feature of high gain of cascode amplifier structure, its 1-dB gain compression point appears earlier than the common source amplifier architecture.
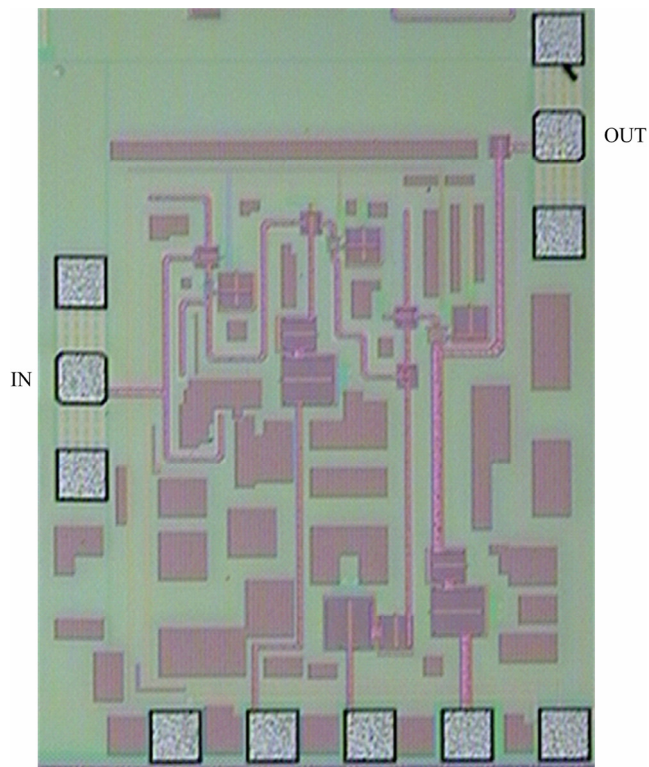
Fig. 6.6. Chip photo of 60-GHz power amplifier. It is with a size of 550 µm × 640 µm.
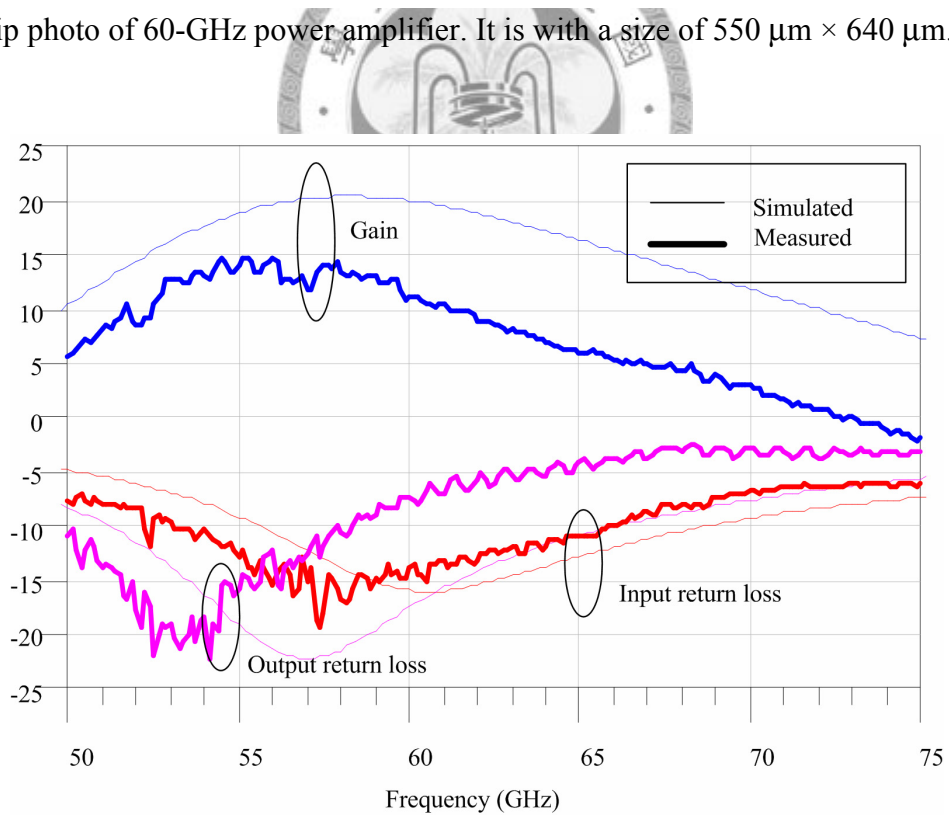
Fig. 6.7. Simulated and measured *S*-parameters of 60-GHz PA.
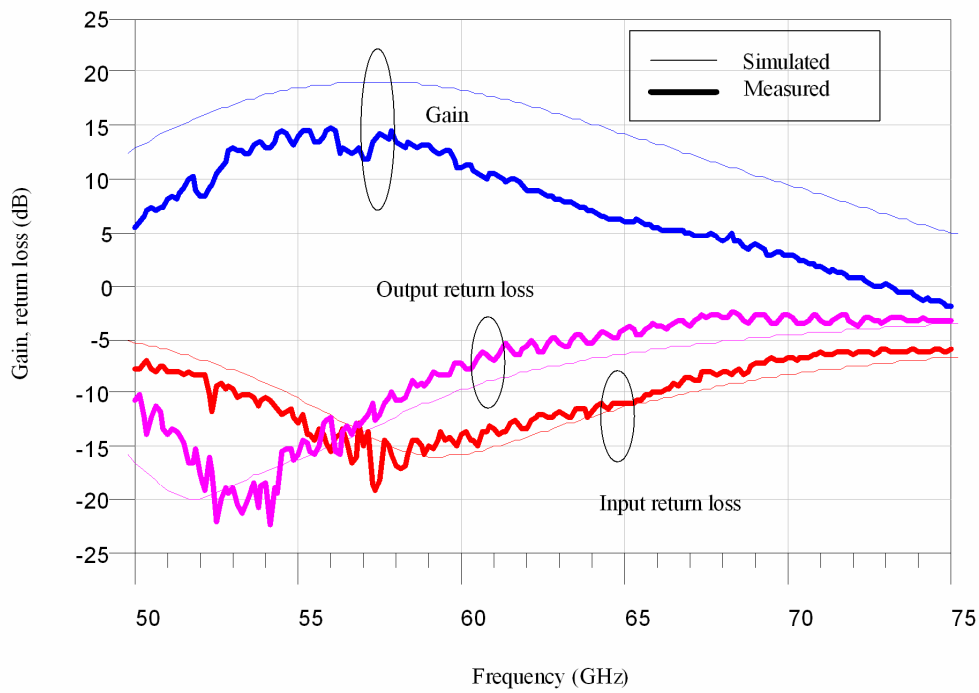
Fig. 6.8. Re-simulated and measured *S*-parameters of the 60-GHz PA.
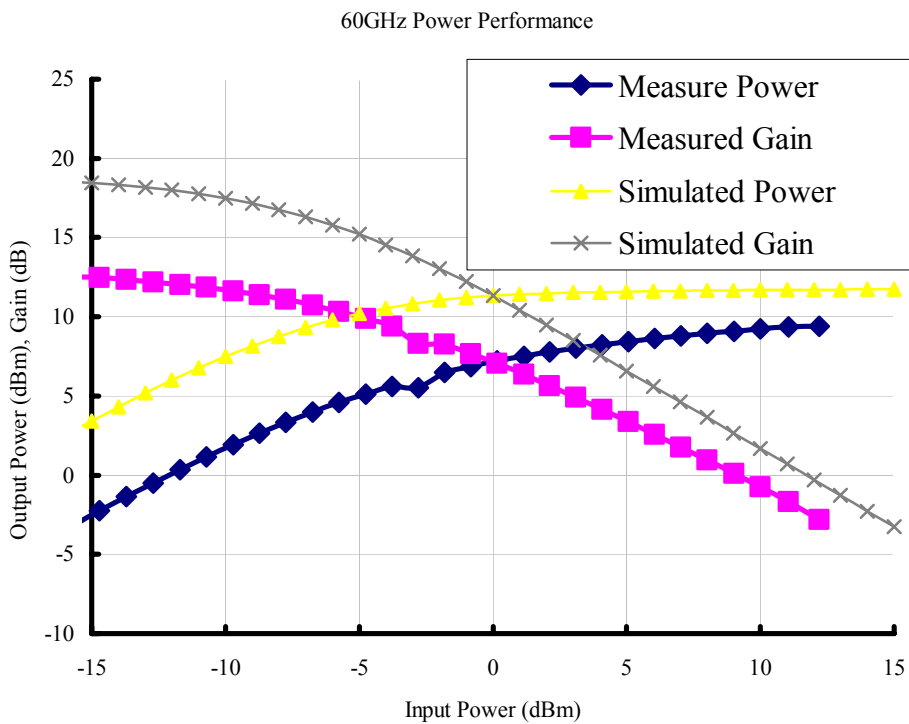
Fig. 6.9. Re-simulated and measured power performance of 60-GHz power amplifier.

6.5   Summary

The reported CMOS 60-GHz power amplifiers are summarized in Table 6.1. It can be seen that the power amplifier in this chapter has the relatively high gain and good power performance than other published data [48], [50]-[55]. Another to mention is that the PA in this design consumes much more power consumption than other works, because the threshold voltage is much higher in 65 nm and leads to higher current. This would be a challenge for mixed-mode circuit design.

This chapter introduces the design procedure of a PA. After that, it demonstrates a high gain 60-GHz power amplifier in 65 nm CMOS process, and it achieves a peak gain of 14.7 dB and a saturation power of 9.5 dBm.

Table 6.1

Process	Topology	DC Biasing	V_{ds}	Frequency (GHz)	Power Gain (dB)	Saturation Power(dBm)	Ref.
65 nm CMOS	3-stage, cascode	88mA, 2V	1V	57	14.5	9.5	This work
65 nm CMOS	1-stage, CS	23mA, 1.2V	1V	62	4.5	9	[48]
90 nm CMOS	3-stage, CS	26.5mA, 1.5V	1.5V	60	4.7	9.3	[50]
90 nm CMOS	2-stage, CS	23mA, 1V	1V	57	9.8	10	[51]
90 nm CMOS	2-stage CC, 1-stage CS	30mA, 1.5V	1.5V	60	14	6	[52]
90 nm CMOS	3-stage cascode	100 mA, 1.8V	0.9V	60	30	13.8	[54]
90 nm CMOS	DAT combing + 3-stage, cascode	153 mA, 1.8V	0.9V	60	26	14.5	[55]

Chapter 7 Conclusions

First, this thesis describes the fundamental concepts of RF switches, and then demonstrates the most common used SPDT switch block in wireless transceivers. The filter-integrated design approach is adopted due to the good matching and better isolation. Two MMW SPDT switches are demonstrated in this thesis. The 90 nm CMOS SPDT switch is the highest frequency one in our knowledge. The SPDT switch in 65 nm CMOS, it has an insertion loss about 3.2-4.5 dB and an isolation better than 20 dB in 40-80 GHz. The SPDT switch in 90 nm CMOS, and it has an insertion loss of 3-4 dB and isolation better than 25 dB in 60-110 GHz.

Furthermore, the method of analysis of multiple-port switches is demonstrated in this thesis. This method can provide a guideline for MMW designers to choose suitable topology for multiple-port switches to enhance the bandwidth efficiency, instead of tuning the topology blindly. Besides, the multiple-port switches were fabricated to verify the proposed analysis. The net-type multiple- port switches in this thesis has an insertion loss of 4-5 dB and isolation better than 25 dB in 48-65 GHz, and the ring-binary type multiple-port switch in this thesis has an insertion loss of 3-4.5 dB and isolation better than 30 dB in 43-66 GHz

Finally, the 60 GHz PA in 65 nm CMOS is demonstrated. The PA has a saturation power of 9.5 dBm and a gain better than 10 dB for standard application of 60 GHz radio.

References

[1] Z. M. Tsai, M. C. Yeh, M. F. Lei, H. Y. Chang, C. S. Lin, and H. Wang, "FET-integrated CPW and the application in filter synthesis design method on traveling-wave switch above 100 GHz," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 5, pp. 2090–2097, May 2006.

[2] David M. Pozar, *Microwave Engineering*, Willey, 2003.

[3] P.I. Richard, "Resistor-transmission line circuits," *Proc. of the IRE*, vol. 36, pp. 217-220, February 1948.

[4] J. Lee, R.-B. Lai, C.-C. Chen, K.-Y. Lin, and H. Wang, "Low insertion loss single-pole-double-throw reduce-sized quarter-wavelength band-pass filter-integrated-switch", accepted by *IEEE Trans. Microw. Theory Tech.*

[5] T. Hirota, A. Minakawa and M. Muraguchi " Reduced-Size Branch-Line and Rat-Race Hybrids for Uniplanar MMIC's," *IEEE trans. Microwave Theory and Tech.*, vol. 38, no. 3, March. 1990, pp. 270-275.

[6] Jia-Sheng Hong, M. J. Lancaster, *Microstrip Filters for RF/Microwave Applications*, John Wiley & Sons, Inc, 2001.

[7] Y. Jin, and C. Nguyen, "Ultra-compact high-linearity high-power fully integrated DC-20 GHz 0.18 μm CMOS T/R switch," *IEEE trans. Microwave Theory and Tech.*, vol. 55, no. 1, Jan. 2007, pp. 30-36.

[8] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A 94GHz SPST switch in 65nm bulk CMOS," *IEEE CSICS*, Oct. 2008, p.p.1-4.

[9] S. F. Chao, H. Wang, C.-Y. Su, and J. G. J. Chern, "A 50 to 94-GHz CMOS SPDT switch using traveling-wave concept," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 2, pp. 130–132, Feb. 2007.

[10] C. M. Ta, E. Skafidas, and R. J. Evans, "A 60-GHz CMOS transmit/receive switch," *IEEE*

RFIC, June 2007, p.p. 725-728.

[11]   M. C. Yeh, Z. M. Tsai, and H. Wang, "A miniature DC-to-50 GHz CMOS SPDT distributed switch," *IEEE European Microwave Conference Proceedings*, Paris, France, Oct. 2005.

[12] P. Park, D. H. Shin, J. J. Pekarik, M. Rodwell and C. P. Yue, "A high-linearity, LC-tuned, 24-GHz T/R switch in 90-nm CMOS, " *IEEE RFIC*, June 2008, p.p. 369-372.

[13] K. Lam, H.Ding, X. Liu, Bradley A. Orner, J. Rascoe, B. Dewitt, E. Mina, and B. Gaucher, "Wideband millimeter wave PIN diode SPDT switch using IBM 0.13μm SiGe technology," *IEEE EuMIC*, Oct. 2007, p.p. 108-111.

[14] B.-W. Min, and G. M. Rebeiz, "Ka-band low-loss and high-isolation switch design in 0.13-μm CMOS," *IEEE Trans. Microwave Theory Tech.*, vol. 56, no.6, pp. 1364-1371, June., 2008.

[15] Z. M. Tsai, Y. S. Jiang, J. Lee, K. Y. Lin, and H. Wang, "Analysis and design of bandpass single-pole–double-throw FET filter-integrated switches," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 8, pp. 1601–1610, Aug. 2007.

[16] Jeffrey Lee, R.-B. Lai, C.-C. Chen, C.-S. Lin, K.-Y. Lin, C.-C. Chiong, and H. Wang, "Low insertion-loss single-pole–double-throw reduced-size quarter-wavelength HEMT bandpass filter integrated switches," *IEEE Trans. Microwave Theory Tech*., vol. 56, no.12, pp. 3028-3038, Dec., 2008.

[17] G. Grosskopf, R. Eggemann, H. Ehlers, A. Kortke, B. Kuhlow, G. Przyrembel, D. Rohde, and S. Zinal, "Maximum directivity beam-former at 60 GHz with optical feeder," *IEEE Trans. Antennas Propag.*, vol. 51, no. 11, pp. 3040–3046, Nov. 2003.

[18] G. Grosskopf, R. Eggemann, S. Zinal, B. Kuhlow, G. Przyrembel, D. Rohde, A. Kortke, and H. Ehlers, "Photonic 60-GHz maximum directivity beam former for smart antennas in mobile broadband communications," *IEEE Photon. Technol. Lett.*, vol. 14, no. 8, pp. 1169–1171, Aug. 2002.

[19] J.-Y. Park, Y. Wang, and T. Itoh, "A 60 GHz integrated antenna array for high-speed digital

beamforming applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2003, vol. 3, pp. 1677–1680.

[20] S.-S. Jeon, J.-Y. Park, Y. Wang, and T. Itoh, "A broadband beam-former for millimeter-wave systems using sub-band sampling," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2003, vol. 1, pp. 579–582.

[21] S. G. Houng, T. Tsukii, and M. J. Schindler, "60–70 dB isolation 2–19 GHz MMIC switches," in *Gallium Arsenide Integr. Circuit Symp.*, 1989, pp. 173–176.

[22] N. Imai, A. Minakawa, and H. Okazaki, "Novel high isolation FET switches," *IEEE Trans. Microw. Theory Tech.*, vol. 44, no. 5, pp. 685–691, May 1996.

[23] Q. Li and Y. P. Zhang, "CMOS T/R switch design: Towards ultra-wideband and higher frequency," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 563–570, Mar. 2007.

[24] K.-H. Pao, C.-Y. Hsu, H.-R. Chuang, C.-L. Lu, and C.-Y. Chen, "A 3–10 GHz broadband CMOS T/R switch for UWB applications," in *1st Eur. Microw. Integr. Circuits Conf.*, 2006, pp. 452–455.

[25] K. Y. Lin, W. H. Tu, P. Y. Chen, H. Chen, H. Wang, and R. B. Wu, "Millimeter-wave MMIC passive HEMT switches using traveling-wave concept," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 8, pp. 1798–1808, Aug. 2004.

[26] S. F. Chao, H. Wang, C.-Y. Su, and J. G. J. Chern, "A 50 to 94-GHz CMOS SPDT switch using traveling-wave concept," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 2, pp. 130–132, Feb. 2007.

[27] K. Y. Lin, Y. J. Wang, D. C. Niu, and H. Wang, "Millimeter-wave MMIC single-pole-double throw passive HEMT switches using impedance-transformation networks," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 4, pp. 1076–1085, Apr. 2003.

[28] H. Takasu, F. Sasaki, H. Kawasaki, H. Tokuda, and S. Kamihashi, "*W*-band SPST transistor witches," *IEEE Microw. Guided Wave Lett.*, vol. 6, no. 9, pp. 315–316, Sep. 1996.

[29] G. L. Lan, D. L. Dunn, J. C. Chen, C. K. Pao, and D. C. Wang, "A high performance V-band monolithic FET transmit-receive switch," in *IEEE Microw. Millimeter-Wave Monolithic Circuits Symp. Dig.*, Jun. 1988, pp. 99–101.

[30] M. Madihian, L. Desclos, K. Maruhashi, K. Onda, and M. Kuzuhara, "A sub-nanosecond resonant-type monolithic T/R switch for millimeter-wave systems applications," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 7, pp. 1016–1019, Jul. 1998.

[31] Z. M. Tsai, M. C. Yeh, M. F. Lei, H. Y. Chang, C. S. Lin, and H. Wang, "FET-integrated CPW and the application in filter synthesis design method on traveling-wave switch above 100 GHz," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 5, pp. 2090–2097, May 2006.

[32] Z. M. Tsai, Y. S. Jiang, J. Lee, K. Y. Lin, and H. Wang, "Analysis and design of bandpass single-pole–double-throw FET filter-integrated switches," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 8, pp. 1601–1610, Aug. 2007.

[33] D. L. Ingram, K. Cha, K. Hubbard, and R. Lai, "*Q*-band high isolation GaAs HEMT switches," in *IEEE GaAs Integr. Circuits Symp. Dig.*, Orlando, FL, Nov. 1996, pp. 289–292.

[34] S.-F. Chao, Z.-M. Tsai, K.-Y. Lin, and H. Wang, "Compact -band SPQT switch using traveling wave concept," in *Proc. Eur. GAAS Conf.*, Paris, France, Oct. 2005, pp. 357–360.

[35] J. Smuk and M. Shifrin, "Monolithic GaAs multi-throw switches with integrated low-power decoder/driver logic," in *Proc. IEEE Radio Freq. Integ. Circuits*, Jun. 1997, pp. 47–50.

[36] J. Lee, C. H. Je, S. Kang, and C.-A. Choi, "A low-loss single-pole six-throw switch based on compact RF MEMS switches," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 11, pp. 3335–3344, Nov. 2005.

[37] Peregrine Semiconduct., San Diego, CA, "Datasheet for PE4283," 2005. [Online]. Available: http://www.peregrine-semi.com/

[38] Hittite Microwave Corporation, Chelmsford, MA, "Datasheet for HMC322," 2007. [Online]. Available: http://www.hittite.com/ index.cfm

[39] C.-H. Lee, B. Banerjee, and J. Laskar, "Novel T/R switch architectures for MIMO applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2004, pp. 1137–1140.

[40] A. Poh and Y. P. Zhang, "Design and analysis of transmit/receive switch in triple-well CMOS for MIMO wireless systems," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 3, pp. 458–466, Mar. 2007.

[41] H. Kamitsuna, Y. Yamane, M. Tokumitsu, H. Sugahara, and M. Muraguchi, "A miniaturized wideband 4 2 4 switch matrix IC using four InP-HEMT SP4T switches," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2005, 4 pp.

[42] G.-L. Tan, R. E. Mihailovich, J. B. Hacker, J. F. DeNatale, and G. M. Rebeiz, "Low-loss 2-and 4-bit TTD MEMS phase shifters based on SP4T switches," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 1, pp. 297–304, Jan. 2003.

[43] S.-F. Chao, C.-C. Kuo, Z.-M. Tsai, K.-Y. Lin, and H. Wang, "40-GHz MMIC SPDT and multiple-port bandpass filter-integrated switches," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 12, pp. 2691–2699, Dec. 2007.

[44] *WIN Semiconductors GaAs 0.15 μm pHEMT Model Handbook*. Taipei, Taiwan, R.O.C.: WIN Semiconduct., 2003.

[45] R.-B. Lai, S.-F. Chao, Z.-M. Tsai, Jeffrey Lee, and H. Wang, "Topology analysis and design of passive HEMT millimeter-wave multiple-port switches," *IEEE Trans. Microwave Theory Tech.*, vol. 56, no.7, pp. 1545-1554, July, 2008.

[46] Guillermo Gonzalez, *Microwave transistor amplifiers – analysis and design*, 2nd ed., Prentice Hall.

[47] S. Reynolds, et. al., "Second Generation Transceiver Chipset Supporting Multiple Modulations at Gb/s data rates", *IEEE BCTM*, pp. 192-197, October 2007

[48] Alberto Valdes-Garcia, Scott Reynolds, and Jean-Oliver Plouchart, "60 GHz transmitter circuits in 65nm CMOS," in *IEEE Radio Freq.Integr. Circuit Symp.*, Jun. 2008, pp. 641–644.

[49] Stephane Pinel, Saikat Sarkar, Padmanava Sen, Bevin Perumana, David Yeh, Debasis Dawn, Joy Laskar, "A 90nm CMOS 60GHz Radio," in *IEEE Int. Solid-State Circuits Conf.*, Feb. 2008, pp. 130-131.

[50] T. Yao et. al., "60-GHz PA and LNA in 90nm RF-CMOS", *IEEE RFIC*, June 2006

[51] B. Heydari, et. al., "A 60 GHz Power Amplifier in 90nm CMOS Technology", *IEEE CICC*, pp. 769-772, Sept. 2007.

[52] M. Khanpout, et. al. "A high-gain, low-noise, +6dBm PA in 90nm CMOS for 60-GHz Radio", *IEEE CSICS*, pp. 121-124, Oct. 2007

[53] Y.-S. Jiang, Z.-M. Tsai, J.-H. Tsai, H.-T. Chen, and H. Wang, "A 86 to 108 GHz amplifier in 90 nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 2, pp. 124–126, Feb. 2008.

[54] J.-L Kuo, Z.-M. Tsai, K.-Y Lin, and H. Wang, "A 50 to 70 GHz power amplifier using 90 nm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 1, pp. 45–47, Jan. 2009.

[55] Yung-Nien Jen, Jeng-Han Tsai, Tian-Wei Huang, and Huei Wang, "A V-band fully-integrated CMOS distributed active transformer power amplifier for 802.15.TG3c wireless personal area network applications," *IEEE CSICS*, pp. 1-4, Oct. 2008.

Publication List

Journal Papers

1. R.-B. Lai, S.-F. Chao, Z.-M. Tsai, Jeffrey Lee, and H. Wang, "Topology analysis and design of passive HEMT millimeter-wave multiple-port switches," *IEEE Trans. Microwave Theory Tech.***,** vol. 56, no.7, pp. 1545-1554, July, 2008.

2. Jeffrey Lee, R.-B. Lai, C.-C. Chen, C.-S. Lin, K.-Y. Lin, C.-C. Chiong, and H. Wang, "Low insertion-loss single-pole–double-throw reduced-size quarter-wavelength HEMT bandpass filter integrated switches", *IEEE Trans. Microwave Theory Tech.***,** vol. 56, no.12, pp. 3028-3038, Dec., 2008.

Conference Papers

1. Jeffrey Lee, R.-B. Lai, K.-Y. Lin, C.-C Chiong, and H. Wang, "A Q-band low loss reduced-size filter-integrated SPDT switch using 0.15-μm MHEMT technology," *IEEE MTT-S Int. Microw. Symp.***,** 2008.