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透過表面改質工程提高二維錫鹵化物鈣鈦礦電晶體的性能和穩定性及其對光記憶行為的影響

Enhancing Performance and Stability of Two-Dimension Tin Halide Perovskite Transistors Through Surface Engineering and Its Impact on Photomemory Characteristics

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Enhancing Performance and Stability of Two-Dimension Tin Halide Perovskite Transistors Through Surface Engineering and Its Impact on Photomemory Characteristics

本論文係趙奕翔君(R10524101)在國立臺灣大學化學工程學系所完成之碩士學位論文，於民國 112 年 7 月 13 日承下列考試委員審查通過及口試及格，特此證明。

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誌謝

不知不覺就逼近了畢業這一天，回顧這片校園的點點滴滴，突然很不捨這裡的人事物，他們佔據了我生命的一大篇章，也在其中教會了我許多人生哲理，回顧我大學生涯，在系籃和課業中盡力保持平衡，而在升碩班口試時，卻因為遲到被取消資格，最後又筆試正取一考回來，上了碩班選教授太慢，差點找不到教授收留，在因緣際會下我得知闕老師還剩一個名額，最後才進來，從大肆就開啟我的研究之路，在這個載浮載乘的人生中向前走，能到現在已經算是奇蹟了。

回顧碩班這兩年，在明筠學姊提早畢業後，我必須要在這裡獨立自主，我認為我是幸運的，第一，錫鈣鈦礦電晶體不好做，處於萌芽階段，因為它的高門檻，相對的屬於論文好發的階段，第二，雪梨大學的淳皓學長因疫情被多留在我們實驗室好幾個月，他在我新手時期不吝嗇地給予我許多幫助，第三，闕老師不斷的開會，盯著我們的進度，雖然有時候會覺得壓力很大，但也是因為這樣，我才會有論文發表，這也是以前的我無法想像的，這些巧合同時發生，才造就了我現在在這裡，成功永遠不是靠自己一個人的努力。

我想先改謝我自己，在課業和研究上我都沒有放棄，也有盡力做到最好，其次我要感謝我爸媽，他們懂得不多，也不富有，但他們很努力栽培我，再來我要感謝闕老師，他帶領我進入研究的世界，工作態度和待人處事也讓我很敬佩，我也感謝同屆的世峰、稟翔和實驗室的所有人，我很喜歡實驗室的氛圍，他們讓我從原本封閉的人格變得奔放，這個改變我一生的歷程是讓我覺得最難得的，當然還有跟我一起去澳洲待了 16 天的明軒，和每次都帶我去同輻測數據的炯翰，他們在我心中是一道明燈，最後還有沒有辦法一起走到最後的柔安，謝謝她陪我度過大半的碩班，希望往後彼此都將安好。

熬了六年，終於登出台大啦!!!!!!!!!!!!!!!!!!!!!!!!

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摘要

近十年來，金屬鹵化物鈣鈦礦因其具高吸收係數、低激子結合能和長載流子壽命，在半導體領域引起了極大的關注。這些特性使其適用於電子元件發展，如鈣鈦礦太陽能電池(PVSC)、鈣鈦礦發光二極體(PeLED)、鈣鈦礦場效應電晶體(PeFET)等。然而，鉛基鈣鈦礦總是被批評具高環境毒性，同時，由於鉛具有相對高的有效載子質量，導致鉛基鈣鈦礦電晶體的載子遷移率普遍偏低。因此，有越來越多的研究將鉛替換成錫，並致力於開發二維錫基鹵化物鈣鈦礦電晶體，其中最著名的體系為苯乙基錫碘化銨 (PEA_2SnI_4)，其具有適當的能隙並在室溫下可展現較高的載子遷移率。然而，錫基鹵化物鈣鈦礦具有較快的結晶速率，造成其製備薄膜質量較低，同時，Sn^{2+}在含氧環境中容易氧化成 Sn^{4+}，限制了其廣泛應用性。在此，我們採用了界面工程改善二維錫基鈣鈦礦的膜況，減少缺陷並提高空氣穩定性，最終也證明這些改質可以同時提高電晶體元件的性能與穩定性。

在第二章中，我們使用了 PEAI/FPEAI 對 PEA_2SnI_4 薄膜進行表面鈍化處理，大大的提高了鈣鈦礦場效電晶體的性能和穩定性。鈍化過程中引起的表面再結晶增加了晶粒尺寸減少表面缺陷，同時，PEA^+和 $FPEA^+$陽離子團上的氮原子可與 Sn^{2+}形成路易斯酸鹼對有效減少 Sn 空缺數量，進而改善膜況。此外，表面鈍化可以 p 型摻雜 PEA_2SnI_4 薄膜，促進鈣鈦礦與電極之間更好的能級匹配，實現高效的電荷傳輸。PEAI 和 FPEAI 表面鈍化的元件測得的最大載子遷移率(μ_h)有明顯的增加，分別為 2.15 和 2.96 $cm^2\,V^{-1}\,s^{-1}$，遠高於對照組的 μ_h (0.76 $cm^2\,V^{-1}\,s^{-1}$)。此外，這些疏水的鈍化劑還能夠起到保護 PEA_2SnI_4 薄膜的作用，減緩空氣水氧引起的降解，這一個論點乃是透過 XPS、UV 和 XRD 等分析來證明。此外，鈣鈦礦薄膜中缺陷的減少間接提高了元件的閘極偏壓穩定性。最後，我們證明了鈣鈦礦場應效電晶體的非揮發性光記憶行為，並利用它們來製作鈣鈦礦場效應電晶體式的記憶體。總結來說，PEAI/FPEAI 的表面鈍化不僅降低了鈣鈦礦薄膜的表面缺陷數量、提高環境

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穩定性，同時還增強了元件的光響應電流。我們的研究成果凸顯了表面鈍化在提高鈣鈦礦場效電晶體的性能和穩定性方面的幫助，這對於先進光電元件的發展有重要的影響。

在第三章中，我們通過旋塗法製備了 TEA_2SnI_4 的二維錫鹵化物鈣鈦礦薄膜。我們首先比較了 PEA_2SnI_4 和 TEA_2SnI_4 的光學性質、膜況和能階。接下來，我們將 TEA_2SnI_4 應用於場效應電晶體元件並發現其最大載子遷移率可達 2.48 $cm^2 V^{-1} s^{-1}$，高於先前的 PEA_2SnI_4 體系，同時也是目前所有 TEA_2SnI_4 相關論文中最高的報導值。此結果可能來自於 TEA_2SnI_4 與金電極有更好能級匹配或是 TEA^+陽離子團較高之介電常數。我們目前正針對這個具有更高載子遷移率的二維錫基鹵化物鈣鈦礦體系進行添加劑與表面改質工程等，以期在未來達到更理想的性能。

Keywords: 二維錫鈣鈦礦、表面鈍化、介面工程、場效應電晶體、光記憶體

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Abstract

Organic-inorganic metal halide perovskites have attracted a great deal of interest in the semiconductor field in the last decade due to their high absorption coefficients, low exciton binding energy, and long carrier lifetime. These properties make them suitable for electronic applications such as perovskite solar cells (PVSC), perovskite light emitting diodes (PeLED), perovskite field effect transistors (PeFET), etc. Among these, two-dimensional organic-inorganic metal halide perovskites are potential candidates for transistor applications because of their quantum effects and high structural stability. However, lead-based perovskites have long been criticized for their high toxicity to the environment. Meanwhile, the effective mass of the carriers is relatively large and their carrier mobility in transistors is low. Therefore, many studies have replaced lead with tin and worked on two-dimensional (2D) tin halide perovskites-based transistors, such as phenethylammonium iodide (PEA_2SnI_4). They have a suitable band gap and high mobility. However, excessively fast crystallization rate for tin-based perovskites contributes to low quality morphology. Also, the easy oxidation from Sn^{2+} to Sn^{4+} in the environment limits their wide applicability. Herein, we used an interfacial engineering approach to improve morphology, reduce defect density, and improve the air stability of 2D tin perovskites. The results further demonstrate that this modification method improves the performance

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of 2D tin perovskite transistors and enhances their air stability at the same time.

In **Chapter 2**, we have shown that surface passivation of PEA_2SnI_4 films with PEAI/FPEAI significantly improves the performance and stability of the derived perovskite transistors. Surface recrystallization induced by surface passivation further reduces surface defects and increases grain size. The electron-donating pairs of nitrogen atoms on PEA^+ and $FPEA^+$ form Lewis acid-base pairs with Sn^{2+} and reduce Sn vacancies, resulting in improve films. Additionally, these passivators are able to p-dope the PEA_2SnI_4 films, promoting better energy-level alignment with the electrodes and enabling efficient charge transfer. The PEAI- and FPEAI-passivated devices showed a significant increase in maximum hole mobility (μ_h) of 2.15 and 2.96 $cm^2\ V^{-1}\ s^{-1}$, respectively, exceeding the value (0.76 $cm^2\ V^{-1}\ s^{-1}$) of the control device. These hydrophobic passivators also provided protection against ambient air-induced degradation of PEA_2SnI_4 film, as evidenced by XPS, UV, and XRD analyses. Moreover, they enhanced the gate bias stability of the devices by reducing defects in the perovskite films. Ultimately, we demonstrate the non-volatile photomemory behavior of perovskite transistors and leverage them for perovskite-transistor-based memories. In conclusion, surface passivation with PEAI/FPEAI not only reduces surface defects and improves the air stability of perovskite films, but also improves the photoresponse of the devices.

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Overall, this work highlights the importance of surface passivation in enhancing the performance and stability of perovskite transistors, which is of great importance for the development of advanced optoelectronic devices.

In **Chapter 3**, we fabricated 2D tin halide perovskite films of TEA_2SnI_4 by spin-coating. And we first compared the optical properties, morphology, and energy level of PEA_2SnI_4 and TEA_2SnI_4. Next, we applied TEA_2SnI_4 to transistor devices with a maximum hole mobility of 2.48 $cm^2 V^{-1} s^{-1}$. This mobility is not only higher than that of PEA_2SnI_4 in our experiment, but also is the highest of all TEA_2SnI_4-related studies reported to date. This result could result from a better energy alignment or a higher dielectric constant of the TEA^+ spacers. My group are currently working on additive and surface modification engineering for this 2D tin system with higher carrier mobility to achieve better performance in the future.

Keywords: Two dimension tin halide perovskite、Surface passivation、Surface engineering、Field effect transistor、Photomemory

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Table Captions

Table 2.1 Film Thickness before and after surface passivation.

Table 2.2 TRPL lifetime fitting results for the studied three films.

Table 3.1 The transistor device performance data for TEA_2SnI_4 and PEA_2SnI_4.

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Figure Captions

Figure 1.1 Schematic illustration for 2D perovskites, 3D perovskites, and mixed dimensional perovskites in terms of optoelectronic properties and stability.[1]

Figure 1.2 Structures for ⟨100⟩-oriented 2D perovskites. (a) Ruddlesden–Popper phase with staggered layer stacking. (b) Dion-Jacobson phase with eclipsed layer stacking. (c) Alternating cations in the interlayer phase with staggered layer stacking along the *b*- and eclipsed along the *a*- axis.[2]

Figure 1.3 Four device architectures for OFETs: (a) Top-contact bottom-gate structure; (b) Bottom contact bottom-gate structure; (c) Top-contact top-gate structure; (d) Bottom-contact top-gate structure.[3]

Figure 1.4 (a) Schematic diagram of the bottom contact device showing unfilled region near the source and drain contact edges. (b) schematic of the bottom contact device showing different region of pentacene morphology. Scanning electron micrograph of pentacene on gold contact (c) near gold contact edge on SiO_2, (d) far away from gold contact edge on SiO_2 and (e) on gold contacts.[4]

Figure 1.5 (a) Schematic structure of a field-effect transistor and applied voltages: L = channel length; W = channel width; V_{ds} = drain voltage; V_g = gate voltage; V_{th} = threshold

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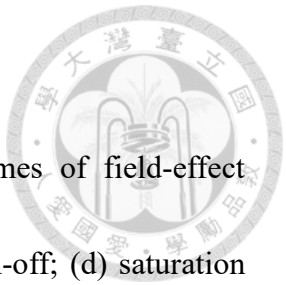

voltage; I_{ds} = drain current. (b-d) Illustrations of operating regimes of field-effect transistors: (b) linear regime; (c) start of saturation regime at pinch-off; (d) saturation regime and corresponding current-voltage characteristics.[5]

Figure 1.6 a) Output characteristics (sweeping V_{DS} while V_{GS} = const.) for an ideal field-effect transistor b) transfer characteristics (sweeping V_{GS} while V_{DS} = const.) in the saturation regime ($V_{DS} > V_{GS}-V_{th}$) semilog and square-root plot to extract the transistor parameters.[6]

Figure 1.7 Historical reported 2D tin perovskite FETs performance. The same color marking represents the same laboratory group. The FETs structure, the journal publication, and the modification method are also highlighted in the graph.

Figure 1.8 Device architectures of the phototransistor memory: a) channel-only, b) channel with photogate, c) photochromic channel devices, and devices with d) inactive polymer, e) blocked floating gate, f) floating gate, g) photoactive polymer, and h) organic molecule-based electrets.[7]

Figure 1.9 The mechanism process of photo-assisted programming and electrical erasing via tunnelling-effect of the photonic memory transistor device.[8]

Figure 1.10 Research objectives of **Chapter 2**.

Figure 2.1 The main figure of contents of this chapter.

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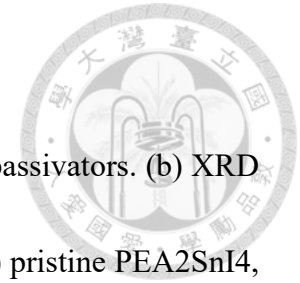

Figure 2.2 (a) Schematic device structure with the studied surface passivators. (b) XRD patterns and (c-e) SEM images (under x 10000 magnification) of (c) pristine PEA2SnI4, (d) PEAI-passivated, and (e) FPEAI-passivated films. (f) UV-vis absorption spectra, (g) PL emission spectra, and (h) TRPL spectra of the pristine and PEAI/FPEAI-passivated films.

Figure 2.3 GIWAXS pattern of the PEA2SnI4 film.

Figure 2.4 KPFM spectroscopy for (a) pristine PEA2SnI4, (b) PEAI-passivated, and (c) FPEAI-passivated films. (d) UPS spectroscopy and (e) the corresponding energy level schematic for the studied three films.

Figure 2.5 Tauc plot and band gap calculation for (a) the pristine PEA2SnI4 film and (b) PEAI- and (c) FPEAI-passivated PEA2SnI4 film.

Figure 2.6 XRD patterns of (a) pristine PEA2SnI4, (b) PEAI-passivated, and (c) FPEAI-passivated films at different air exposure times. (d) Normalized absorption intensity (relative to the absorption intensity of the fresh state) at 610 nm in Figure S4 for different air exposure times. XPS of Sn 3d core peaks performed on (e) fresh films and (f) films exposed to air for 60 minutes. In the stability test, samples were stored at air-conditioned temperature of 22 oC with a relative humidity of 50-70%.

Figure 2.7. XRD patterns of the fresh (a) pristine PEA2SnI4, (b) PEAI-passivated, and

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(c) FPEAI-passivated films.

Figure 2.8 The contact angle of (a) pristine PEA2SnI4, (b) PEAI-passivated, and (c) FPEAI-passivated films.

Figure 2.9 UV-Vis spectra of (a) pristine PEA2SnI4, (b) PEAI-passivated, and (c) FPEAI-passivated films at different air exposure times.

Figure 2.10 XPS of fluorine 1s core peak performed on the FPEAI passivated film.

Figure 2.11 Transfer curves of (a) the pristine device, (b) the PEAI device, and (c) the FPEAI device. (d) Output curve of the PEAI device. (e) Mobility statistics of the studied FET devices on ten different devices. (f) Normalized mobility variations as a function of aging time in ambient air.

Figure 2.12 Output curves for (a) the pristine device and (b) the FPEAI device.

Figure 2.13 Historical reported 2D tin perovskite FETs performance. The same color marking represents the same laboratory group. The numbering beside the point corresponds to the reference below.

Figure 2.14 Transfer curve of the FET device with pure solvent-treated perovskite film.

Figure 2.15 (a-c) The transfer curves and (d-f) the corresponding square roots of drain currents of (a,d) the pristine device, (b,e) the PEAI device, and (c,f) the FPEAI device for different aging times in ambient air.

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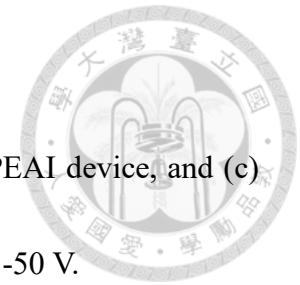

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Figure 2.18 Illustration of the mechanism of electron-hole pair generation and recombination processes in the perovskite films with and without surface passivation.

Figure 3.1 The chemical structure of cation spacer PEA^+ and TEA^+.

Figure 3.2 The SEM surface morphology of 2D tin perovskite (a) PEA_2SnI_4 and (b) TEA_2SnI_4.

Figure 3.3 (a) The UV-vis absorption spectra and (b) PL emission spectra of two 2D tin perovskite materials.

Figure 3.4 Tauc plot from UV-vis for (a) PEA_2SnI_4 and (b) TEA2SnI4. The XRD crystallinity data for 2D tin PEA2SnI4 and TEA_2SnI_4.

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Figure 3.5 (a) The UPS energy level for PEA2SnI4 and TEA_2SnI_4. (b) The illumination of energy level for PEA_2SnI_4 and TEA_2SnI_4

Figure 3.6 The transfer characteristic for PEA2SnI4 and TEA2SnI4 transistor device.

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Chapter 1

Introduction

1.1 Introduction of Organic-Inorganic Hybrid Perovskite

Over the past few decades, perovskite crystals have emerged as highly promising optoelectronic materials due to their high absorption coefficients, high mobility, high diffusion length and low temperature solution processability.[9] The combination of these excellent properties makes perovskite materials suitable for optoelectronic device applications such as photovoltaics, light-emitting diodes, lasers, field-effect transistors, and even phototransistors.[10-13] As shown in **Figure 1.1**, perovskites can be classified as two-dimensional, three-dimensional, and quasi-two-dimensional depending on their chemical structure and composition.[1]

The most widely studied and applied structures are three-dimensional perovskite crystals. The general formula for unit crystals is ABX_3, where A+ are cations, small enough to be embedded in the unit crystal, such as Cs^+, $CH_3NH_3^+$ (MA^+), and $CH(NH_2)_2^+$ (FA^+). B^{2+} are group IV A metal cations, such as Ge^{2+}, Pb^{2+}, and Sn^{2+}. x^- are halide atoms, such as Cl^-, Br^-, and I^-. They form the cornor-sharing $[BX_6]^{4-}$ of the octahedral crystal structure. The optoelectronic properties occur on these crystal structures. Three-dimensional perovskites are widely used in solar cells due to their high absorption

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coefficient, tunable band gap and high carrier lifetime[14]. These properties make them suitable for further studies in the laboratory. However, oxygen and moisture can easily hydrolyze perovskite crystals into chemical ions and create trap states and pinholes in the films[15]. Moreover, when bias voltage is added, these ions further lead to ion migration, which makes the internal structure electrically unstable.[16] Finally, thermal stability also needs to be enhanced prior to industrial applications.

One method to solve the stability problem is to add organic cations to the precursor solution. Organic cations can separate inorganic crystals into hybrid organic-inorganic layers to form a two-dimensional perovskite structure. Large organic cations are believed to help stabilize the crystal structure and are thought to prevent oxygen and moisture from intruding into the perovskite structure.[17] Although the organic cations are considered to be insulating, the selection of cations can drastically affect the properties of two-dimensional perovskites. i) Cationic ligands can affect not only the bond angle of metal-halide - metal (M-X-M), but also the bond length of metal-halide (M-X). They both influence the deformation and tilting of the crystal. (ii) Different cation spacers have different dielectric constants, leading to different quantum confinement, which can change the exciton binding energy (E_b). (iii) The length and hydrophobicity of the cation spacers can show different protective effects. [2]

Compared with three-dimensional perovskites, two-dimensional perovskites confine

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the current to a two-dimensional plane, avoiding additional ion migration and facilitating the application in field-effect devices. As shown in **Figure 1.2**, for <001>-oriented two-dimensional perovskites, the phases can be classified as Ruddlesden-Popper (RP), Dion-Jacobson (DJ) and alternating cations in interlayer space (ACI) according to the type of cations. For RP phase species, the cations contain +1 coordination number and only one nitrogen atom cooperates with the halide to form a hydrogen bond. On the other side of the molecule, they align with neighboring cation molecules via van der Waals interactions. For the DJ phase two-dimensional perovskite, the cation has two nitrogen atoms with a coordination number of +2 on each side and two hydrogen bonds with the halide. Compared to the RP phase, the d-spacing of the DJ phase is usually smaller. Without van der Waals interactions, the DJ phase is potentially more stable. For the ACI phase, the two cations enter the crystal together and alternate with each other. So far, only the guanidinium group can be used as a template structure.[2]

1.2 Two-Dimensional Tin based perovskite

In the early research, Pb^{2+} based perovskite has been widely used in perovskite solar cell (PSC). 3D lead perovskite has suitable bandgap for solar energy application and thus starts a new chapter for high performance PSC research. However, the toxicity of lead heavy metal to the environment has continuously increased the attention. One of the

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solutions to this method is to replace lead by other metal like tin (Sn) and Germanium (Ge). Among them, Sn has stood out for outstanding property such as smaller radius (1.18Å) compare to Pb (1.19Å). This makes them easily fit into the crystal structure with no barrier.[18] Additionally, smaller atomic mass for Sn than Pb can enhance charge carrier mobility and decrease the Frölich interaction.[19] All these properties is excellent for further electronic application.

Although Sn is a potential candidate for lead perovskite replacement, the easily oxidation problem seriously limits the tin perovskite development in commercialization. Compare with three dimensions structure, the two dimensions structure can greatly improve the tin perovskite degradation rate. The large spacer cations can block moisture and oxygen and thus protect the bulk perovskite layer. However, the insulating properties and larger exciton binding energy restrict their application in perovskite solar cell.[20] However, the reduced ion migration and fixed charge transfer direction makes it appropriate for FET application.

During spin-coating process, the precursor solution can reach super saturation state and form perovskite polycrystal. The procedure of crystal growth contains two states: nucleation and crystal growth. Tin is suffered from rapid crystal growth before nucleation, resulting in bad morphology.[21] To address the rapid crystallization the stability issue, many studies use various additive and surface or bulk passivation. On the one hand, the

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lone pair electron on additive can capture Sn^{2+} ion, slowing down crystal growth rate.[22] On the other hand, the passivation methods can effectively reduce the defect or trapping states, increasing the carrier lifetime. For 2D tin halide perovskite, the polycrystal growth begins from the surface between air/precursor interface and align orderly to the bottom.[23] The 2D tin perovskite can have more widely application once these problems are solved.

1.3 Perovskite Field-Effect Transistors

1.3.1 PeFET Configuration

A field effect transistor is a basic three-terminal electronic device (gate, source and drain) that controls electrical switching by gate voltage modulation. typically, transistor device consists of four parts: a gate, a dielectric layer, a semiconductor active layer, and an electrode. The gate can be either highly doped silicon or a metal that conducts electricity. The dielectric layer directly separates the active layer from the gate. Traditionally, silicon oxide (SiO_2) has been chosen as the dielectric layer. However, low dielectric constants increase the operating gate voltage, which can lead to severe leakage currents. To address these issues, higher dielectric constant materials such as hafnium oxide (HfO_2) or aluminum oxide (Al_2O_3) have recently been chosen to replace silica.[24]

Depend on the order of four layers, the structure of FET can be classified to top gate

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/bottom gate (TG/BG) and top contact/bottom contact (TC/BC), as shown in **Figure 1.3**.[3] Based on the fabricated configuration, the performance of the transistor varies depending on the resistance of the interface layer. The bottom gate device structure allows for better film quality between the active and dielectric layers. However, direct exposure of the active layer to oxygen and moisture may induce rapid degradation of the fragile material. In contrast, TG can completely protect the active layer, but the quality of the interface between the dielectric and active layers may be inferior to that of the BC structure.[25]

Some studies have focused on the comparison between bottom contact and top contact.[26] Structural differences have many implications for their electrical performance and manufacturing difficulty. tc transistors are easier to fabricate because the metal can be deposited on the active layer through a shadow mask. For BC transistors, the semiconductor layer should be spin-coated onto the metal. In this process, the precursor solvent can damage the metal layer to some extent, resulting in poor conductivity or pattern distortion. As shown in **Figure 1.4**, there are usually unfilled areas in the corners of the metal surface. the morphology of the semiconductor layer will differ. For TC structures, the SiO_2 layer has a lower surface energy and therefore a better morphology and thus a larger grain size. In contrast, depositing the active layer on the BC structure on the metal surface results in a smaller and amorphous grain configuration.

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These properties make BC less conductive than TC. [4]

1.3.2 PeFET Working Principle

Before mentioning the working mechanism of a transistor, some relevant transistor parameters must be understood. The channel length (L) represents the distance between the source and the drain, usually a few hundred microns. The channel width (W) is the width of the area between the source and the drain, usually between a few hundred microns and a few millimeters. The capacitance (C) of the dielectric layer determines the operating voltage. For thin or high dielectric layer materials, low operating voltages are effective in reducing leakage currents and saving energy. [27]

Unipolar transistor devices can be divided into p-channel and n-channel depending on whether the charge carrier is a hole or an electron. For bipolar transistors, both holes and electrons can be transported. The gate voltage creates a potential between the source and drain to induce an accumulated charge carrier. At the same time, the drain voltage must be present during operation. When the applied gate voltage exceeds the threshold voltage (V_{th}) to accumulate sufficient carriers, the drain current switches from the off to the on state.

When measuring the FET output characteristic, the process can be classified to four stages: (i) Initial, (ii) Linear region, (iii) Depletion region, and (iv) Saturation region, as

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shown in **Figure 1.5**. At the Initial region, there is no bias voltage applied. At the linear region state, voltage between source and drain (V_{ds}) is smaller than V_g, so the charge carriers are comparatively uniformly distributed but still show linear gradient. When Vg higher than V_{th} ($V_g - V_{th} > 0$), there are sufficient carriers at the active channel. At the Depletion region, Vds gradually increase to the point $V_{ds} = V_g - V_{th}$, this point is called pinch-off point. The electric field cannot accumulate additional carriers anymore. At the saturation region, the same effect occurs and the depletion region area increase. The drain current (I_{ds}) is saturated and cannot increase even higher V_{ds} is driven.[5]

The electronic performance consists of saturation or linear mobility, the illumination is in **Figure 1.6**, and the equation is shown below:

$$\mu_{lin} = \frac{\partial I_{ds}}{\partial V_g} \cdot \frac{L}{WCV_{ds}}$$

$$\mu_{sat} = \frac{2L}{WC}\left(\frac{\partial I_{ds}^{\frac{1}{2}}}{\partial V_g}\right)^2$$

The on/off ratio for drain current is also an important parameter. It is widely accepted that the on/off current ratio should exceed 10^3 to qualified as a transistor. Additionally, the Subthreshold Swing (SS) can show the steepness of channel current. Smaller SS means the device can quickly switch from off to on state. SS can also be used to evaluate the trapping density at the semiconductor and dielectric layer interface. The equation is below:

$$SS = \frac{\partial V_g}{\partial (log I_{ds})}$$

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1.3.3 Two-Dimensional Tin Based Perovskite Transistor Historical Performance

The most widely used two-dimensional perovskite in transistor devices is PEA_2SnI_4. PEA_2SnI_4 has a proper band gap of 2 eV and an exciton binding energy (190 meV) four times higher than the three-dimensional structure due to quantum confinement effects.[28] Quantum confinement contributes to some extent to the stability of perovskites, as localized charges can lead to instability in materials with low exciton binding energies. PEA^+ also benefits from its benzene ring, which is thought to increase crystallinity. The 2D crystal demonstrates the parallel orientation with substrate (00l), which can be proved by X-ray Diffraction (XRD) and Grazing-Incidence Wide-Angle X-ray Scattering (GIWAXS).[23]

As shown in the **Figure 1.7**, back in 1999, the first 2D PEA_2SnI_4 perovskite transistor was reported by Kagan. et al. They used the TC/TG structure and solution process to fabricate the device. The hole mobility reaches 0.6 $cm^2V^{-1}s^{-1}$.[29] In 2001, the same group grew single crystal of m-Fluoro-Phenethylammonium tin iodide (m-$FPEASnI_4$) and fabricated polycrystal perovskite transistor for BC/BG device. The mobility reached between 0.2 to 0.6 $cm^2V^{-1}s^{-1}$.[30] In 2002, melted process perovskite transistor onto SiO_2/Polyimide was fabricated and reached hole mobility 2.6 $cm^2V^{-1}s^{-1}$. Polyimide can effectively enhance the crystallinity. [31] In 2004, Matsushima. et al reported vacuum vapor deposition process to fabricate PEA_2SnI_4 TC/BG device and the

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mobility reached 0.78 $cm^2V^{-1}s^{-1}$.[32] There is a large time interval until 2016, Adachi and his collaborators restudied the field and published three papers about modification of TC/TG PEA_2SnI_4 transistor. The first is the interface engineering of Self-Assembled Monolayer (SAM) and MoO_x to reduce the dielectric/semiconductor and semiconductor/electrode interface. The mobility reached incredible 15 $cm^2V^{-1}s^{-1}$.[33] By increasing the device dimensions to long channel length (L=400 μm), the contact resistance greatly reduced and the hole mobility reached record 26 $cm^2V^{-1}s^{-1}$.[34] In 2017, Chen, et al applied PEA_2SnI_4 in TG/BC phototransistor and performance reached 10^4 A W^{-1} to very weak visible light and their mobility reached 1.2 $cm^2V^{-1}s^{-1}$.[35] In 2018, Wang et al. applied ferroelectric polymer poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) as dielectric layer. Although the mobility is only 0.02 $cm^2V^{-1}s^{-1}$, the high photoresponse and high detectivity makes it suitable for phototransistor application.[36] Since 2019, Noh Yong Young and his groups has done a series of research in 2D PEA_2SnI_4 transistors. The modification includes changing solvent to DMSO, Chlorobenzene (CB) and additive like urea, Copper iodide salt (CuI),and Sn powder etc.[22, 37-39] These operations are nothing else but trying to reduce oxidation rate of Sn^{2+} and slow down the tin crystal growth for better morphology insurance. They usually combined PEA_2SnI_4 transistors to invertor and thus expand the application. Nowadays, they gradually focus on tin perovskite transistor but different structure (3D/quasi-2D).[40, 41] The fabrication

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principle is more complicating and harder to control. In contrast, Feng Teng and his group has also published a serios papers on PEA_2SnI_4. They have tried to adding lead into tin to make mixed $PEA_2Pb_xSn_{1-x}I_4$.[42] Although the mobility is lower, the greatly increase in stability cannot be neglected. They also replaced traditional SiO_2 dielectric layer with poly(vinyl alcohol) (PVA) modified by cross-linking (CL) poly(4-vinylphenol) (PVP) as gate dielectrics (PVA/CL-PVP). Changes in the dielectric layer can effectively reduce the interfacial trap state while maintaining flexibility in transistor fabrication.[43] In conclusion, despite the difficulties in fabricating tin perovskite systems, tin perovskite transistors have attracted interest from the early days.

Perovskite transistors have attracted more attention from their early state. Recently, more and more research has attempted to change PEA^+ to other cationic spacers. In 2022 and 2023, Wang et al. reported 2-thiopheneethylammonium (TEA+) as a spacer to form TEA_2SnI_4.[44, 45] In contrast to PEA^+, TEA^+ has a thiophene moiety that can develop interactions between π-π stacking. Due to the smaller d-spacing, the quantum confinement effect is not as strong as in PEA^+ and the band gap is smaller. However, the hole mobility in the TEA^+ system is higher and shows faster charge transport properties.[46] Recently, Feng Teng and his group reported the first DJ-phase two-dimensional perovskite ($BDASnI_4$) transistor using 1,4-butanediamine (BDA). Without van der Waals interaction between cation spacer, $BDASnI_4$ is more stable and thus high

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performance.[47]

In conclusion, although two-dimensional tin perovskite has been developed since 1999, there are still many researchers attracted by its high performance in transistors or phototransistors. It is a potential material that may even be commercialized at some point, as the oxidation problem has been solved.

1.4 Memory Device

1.4.1 Photomemory configuration

Photomemory devices have nearly the same structure as a conventional transistor. However, one or more additional charge or polarization storage layers are typically deposited between the semiconductor and the dielectric layer as illustrated in **Figure 1.8**. The charge storage behavior can modulate the electrical transmission, resulting in more pronounced hysteresis or threshold voltage shifts in the transmission characteristics. These characteristics can be used to evaluate the performance of the memory device. Depending on the material of the charge storage layer, transistor memory can be divided into three types: (i) ferroelectric, (ii) floating-gate, and (iii) polymer electret transistor memory. Ferroelectric gates and polymer electret have the potential to achieve high doping-density, reversible, and nonvolatile modulation of channel carriers through their polarization. It can significantly change the electronic, optical and structural property of

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memory device. However, ferroelectric gates and polymer electrets materials must be robust and stable for charge storage to reduce operating voltage with low leak current. Floating gate is a charge storage layer which consists of a tunneling dielectric layer and charge storage layer. It has the advantages including low leakage current, fast read/write speed, and low operating voltage for low operation voltage. The materials for floating gate can be metal nanoparticles (NPs), inorganic quantum dot or organic NPs. [8]

1.4.2 Photomemory working principle

As shown in **Figure 1.9**, the single transistor can process at least two stable memory states for the photomemory device. The two states can be modulated through electric stimuli or light illumination. These two methods can adjust the conductance states within the semiconducting channel. In the writing step, electric or light stimuli can prompt charge carriers to be stored in storage layer. In the erasing step, electric or light can be used to erase the storage charge. The memory device should be operated stably between two steps. The most obvious conductance change can be seen from V_{th} change. V_{th} is the minimum gate voltage required to induce enough carrier in the channel between source and drain. The charge in trapping states in the storage layer can have the intrinsic electric field. This will inevitably influence the carrier induced when adding the gate voltage. The V_{th} shift is the most pronounce phenomenon to determine the memory performance

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because it can display the extent of charge being trapped by bulk dielectric layer or the dielectric/semiconducting layer. The V_{th} variation when operating is defined as memory window. In photomemory, the memory window is defined in on state current ratio variation induced by traps without gate bias. Another index to evaluate the operational durability is writing (programing)-reading-erasing-reading (WRER) switching stability, which examines the device capability to maintain current on/off ratio after alternative switching states. The more stable for the memory device, the more cycles number of WRER can operated. [7, 8]

1.5 Research Objectives

Two dimensions perovskite PEA_2SnI_4 has a high potential for further transistor application. However, tin perovskite still exists some challenges like: (i) Too fast crystallization. (ii) Easily oxidation in atmosphere. For the problem of excessively fast crystallization, many studies have adopted additive engineering. These additives may have long pairs on specific atom, which can capture Sn^{2+} and therefore slow down the crystallization rate. Some additives would have the antioxidation property or be reduced reagent. For the problem of easy oxidation, some studies adopt surface passivation method to cover the perovskite surface. However, there is no surface passivation applied in transistors.

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In **Chapter 2**, we demonstrate that surface passivation of PEA_2SnI_4 films greatly improves the performance and stability of the derived perovskite transistors. Surface passivators, phenethylammonium iodide (PEAI) and 4-fluorophenethylammonium iodide (FPEAI), are shown to passivate surface defects in PEA_2SnI_4 films and to increase the grain size by surface recrystallization. In addition, they p-dope the PEA_2SnI_4 film to form a better energy-level alignment with the electrodes and promote charge transport properties. As a result, the FPEAI-passivated devices can exhibit four times higher mobility (2.96 $cm^2 V^{-1} s^{-1}$) than the control one (0.76 $cm^2 V^{-1} s^{-1}$) while the ambient and gate bias stability are greatly improved. Finally, we show that these perovskite transistors display non-volatile photomemory characteristics and that surface passivation increases the photoresponse of the device as it reduces the surface defects on the perovskite film; however, it reduces the charge retention time due to the reduced trap density in the perovskite film. The whole contents and concepts are illustrated in **Figure 1.10**.

In **Chapter 3**, We substitute the original PEA^+ spacer with TEA^+. We investigate the surface morphology, optical properties, and energy level differences of the two two-dimensional tin perovskites. At the end of this chapter, we apply both perovskites to transistor devices. We found that TEA_2SnI_4 has a higher mobility, which may be due to its better energy level alignment with the gold electrode, or it may be that TEA^+ has a larger dielectric constant. Whatever the fact, we can further modify TEA_2SnI_4 on the basis

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of the basic data by these known methods.

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Figures

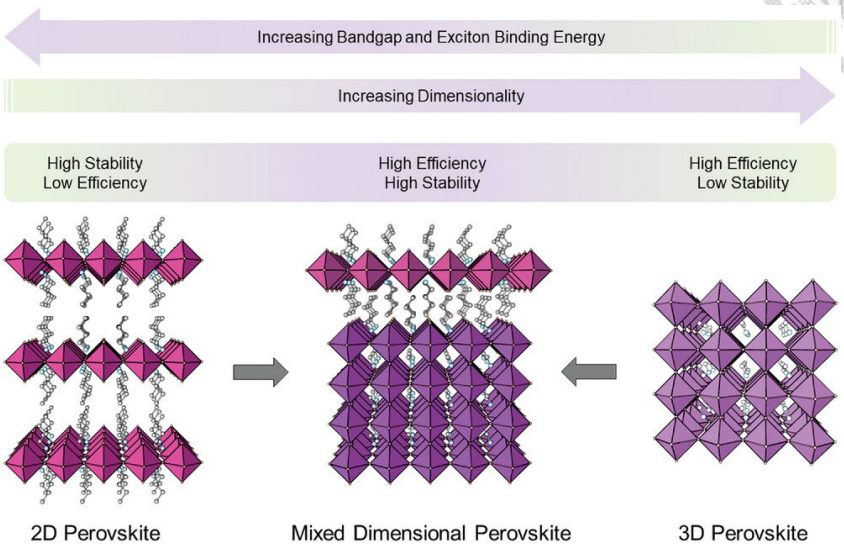

Figure 1.1 Schematic illustration for 2D perovskites, 3D perovskites, and mixed dimensional perovskites in terms of optoelectronic properties and stability.[1]

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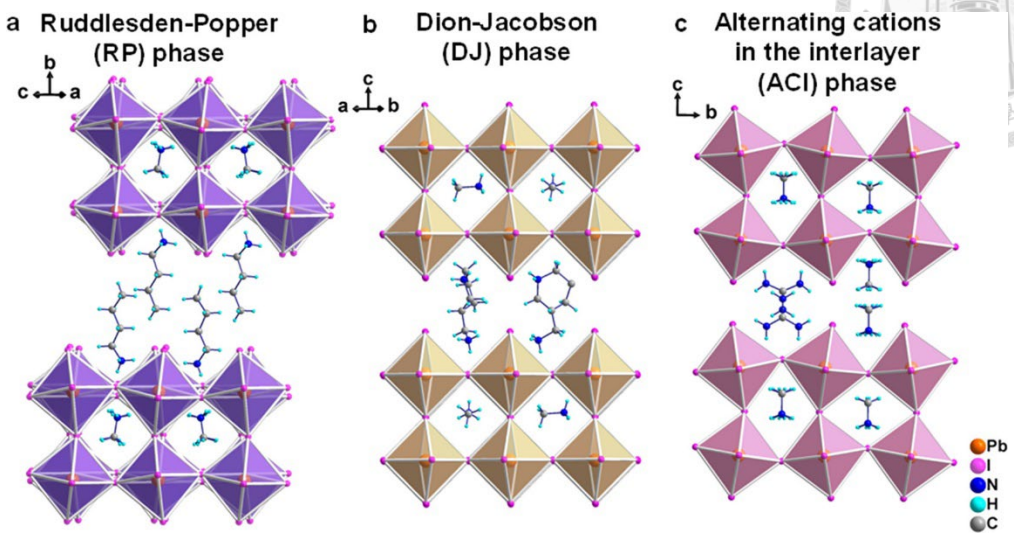

Figure 1.2 Structures for ⟨100⟩-oriented 2D perovskites. (a) Ruddlesden–Popper phase with staggered layer stacking. (b) Dion-Jacobson phase with eclipsed layer stacking. (c) Alternating cations in the interlayer phase with staggered layer stacking along the *b*- and eclipsed along the *a*- axis.[2]

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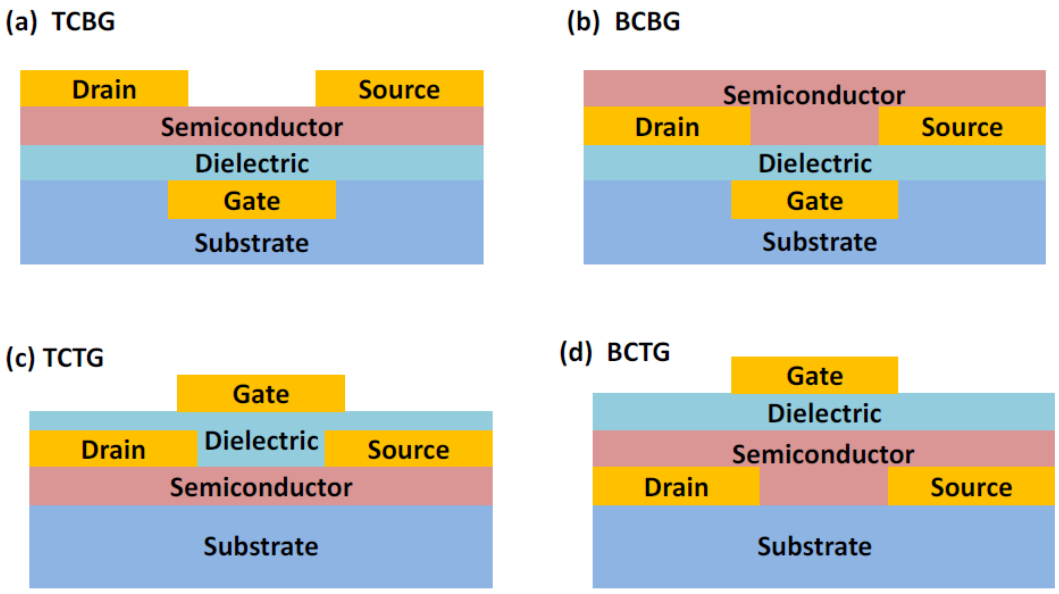

Figure 1.3 Four device architectures for FETs: (a) Top-contact bottom-gate structure; (b) Bottom contact bottom-gate structure; (c) Top-contact top-gate structure; (d) Bottom-contact top-gate structure.[3]

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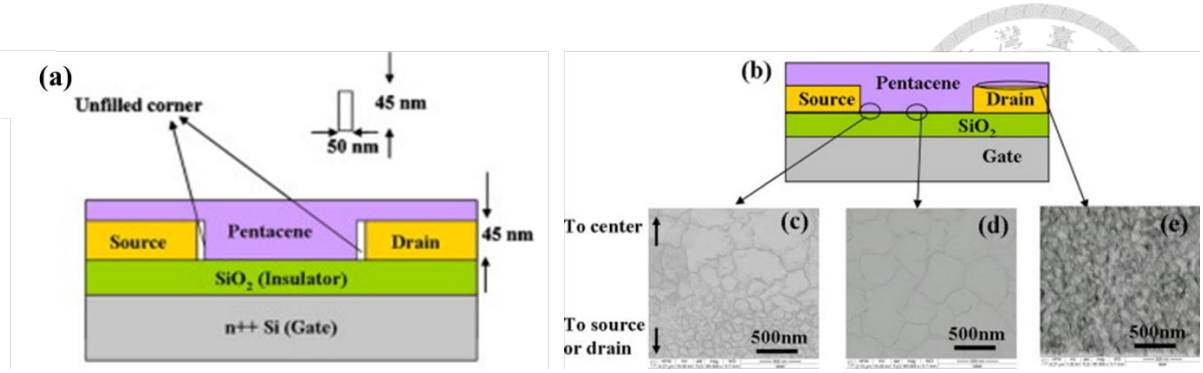

Figure 1.4 (a) Schematic diagram of the bottom contact device showing unfilled region near the source and drain contact edges. (b) schematic of the bottom contact device showing different region of pentacene morphology. Scanning electron micrograph of pentacene on gold contact (c) near gold contact edge on SiO_2, (d) far away from gold contact edge on SiO_2 and (e) on gold contacts.[4].

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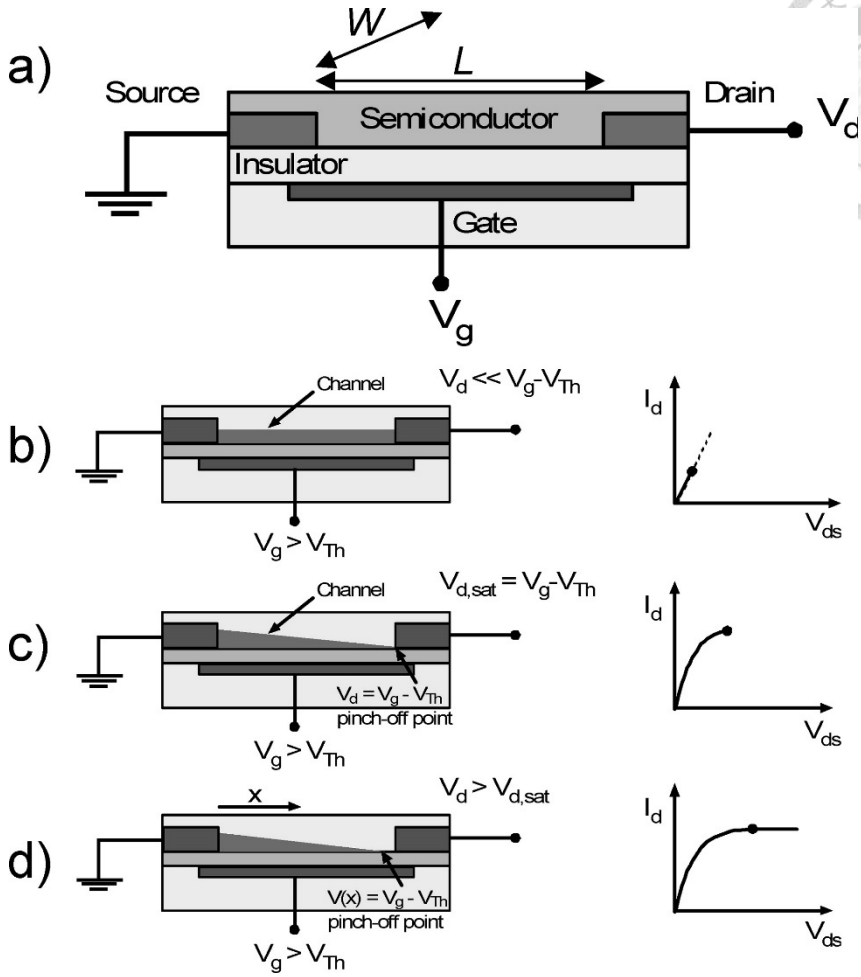

Figure 1.5 (a) Schematic structure of a field-effect transistor and applied voltages: L = channel length; W = channel width; V_{ds} = drain voltage; V_g = gate voltage; V_{th} = threshold voltage; I_{ds} = drain current. (b-d) Illustrations of operating regimes of field-effect transistors: (b) linear regime; (c) start of saturation regime at pinch-off; (d) saturation regime and corresponding current-voltage characteristics.[5]

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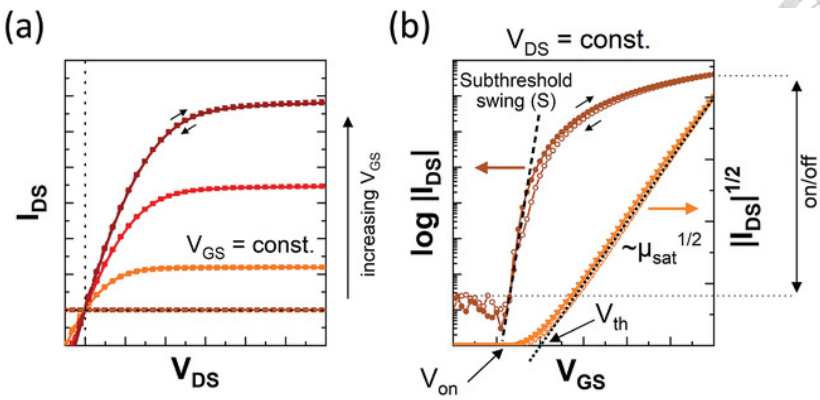

Figure 1.6 a) Output characteristics (sweeping V_{DS} while V_{GS} = const.) for an ideal field-effect transistor b) transfer characteristics (sweeping V_{GS} while V_{DS} = const.) in the saturation regime ($V_{DS} > V_{GS}-V_{th}$) semilog and square-root plot to extract the transistor parameters.[6]

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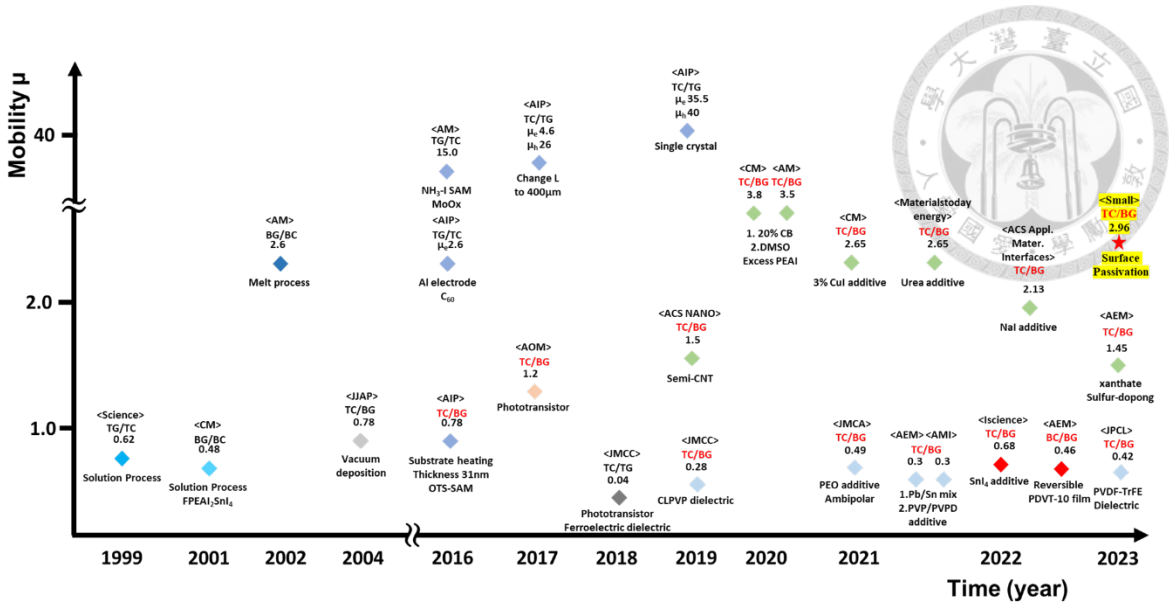

Figure 1.7 Historical reported 2D tin perovskite FETs performance. The same color marking represents the same laboratory group. The FETs structure, the journal publication, and the modification method are also highlighted in the graph.

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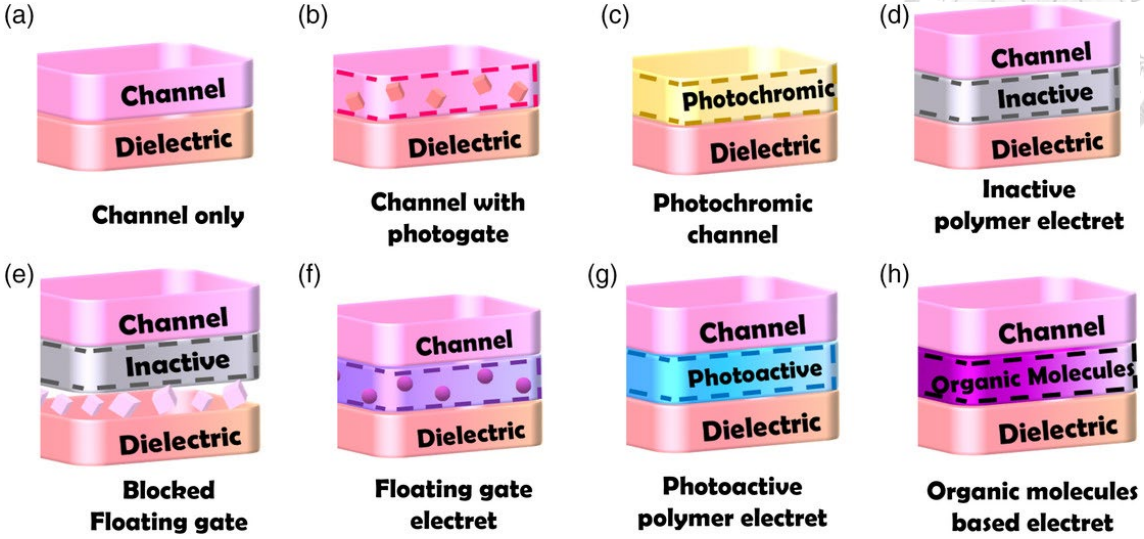

Figure 1.8 Device architectures of the phototransistor memory: a) channel-only, b) channel with photogate, c) photochromic channel devices, and devices with d) inactive polymer, e) blocked floating gate, f) floating gate, g) photoactive polymer, and h) organic molecule-based electrets.[7]

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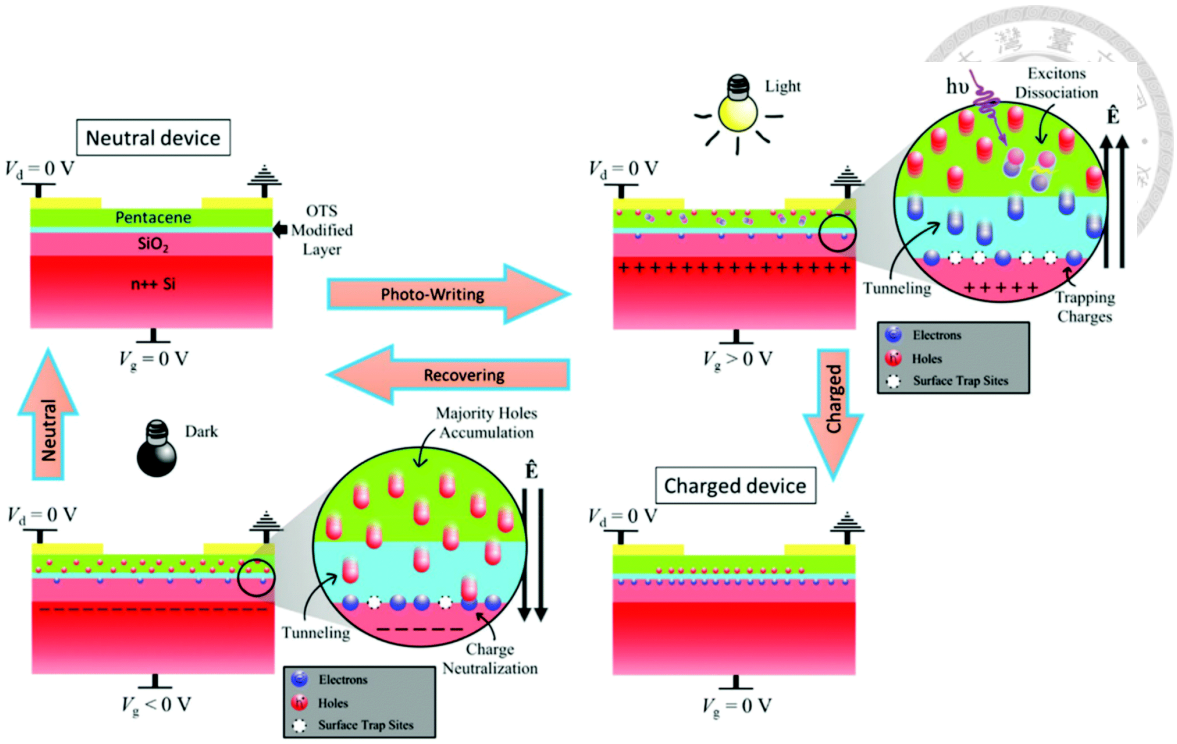

Figure 1.9 The mechanism process of photo-assisted programming and electrical erasing via tunnelling-effect of the photonic memory transistor device.[8]

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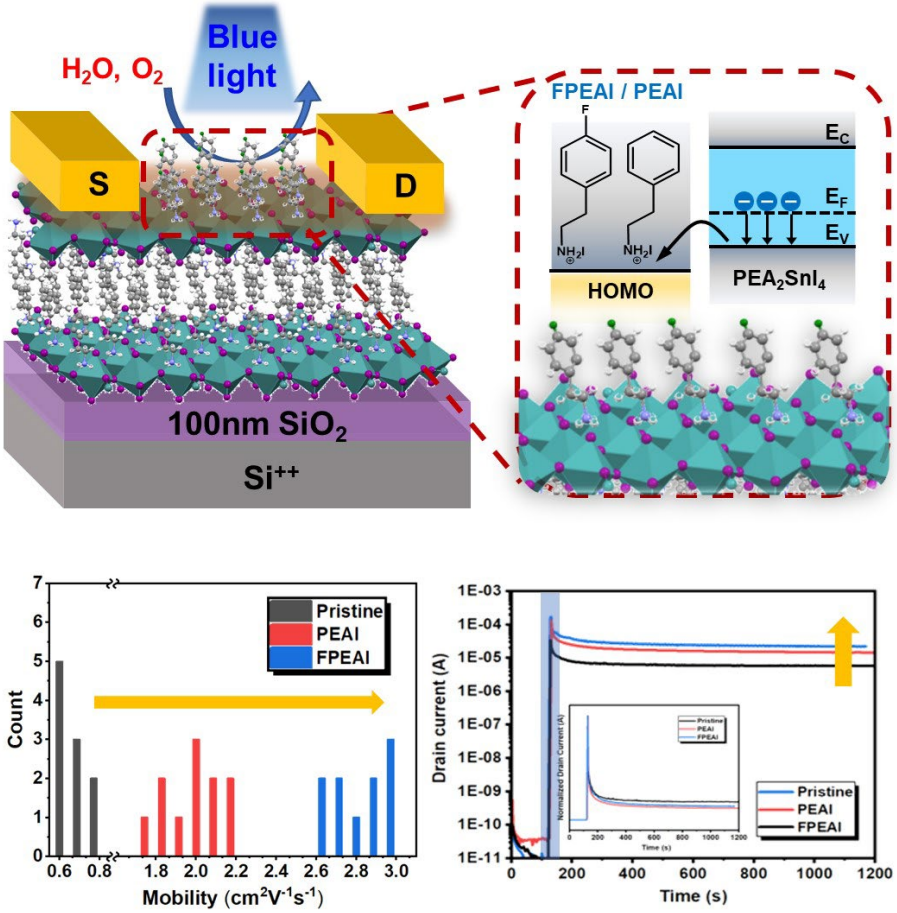

Figure 1.10 Research objectives of **Chapter 2**.

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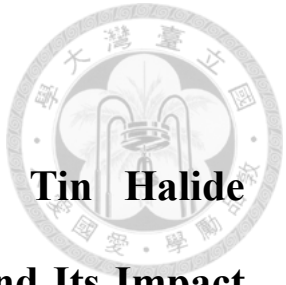

Chapter 2

Performance Enhancement of Lead-Free 2D Tin Halide Perovskite Transistors by Surface Passivation and Its Impact on Non-Volatile Photomemory Characteristics

2.1 Introduction

In the past decade, metal halide perovskites (MHPs) have received significant attention due to their outstanding optoelectronic properties such as tunable band gap, long carrier diffusion length, high absorption coefficient, and low-temperature solution processability.[48-51] Moreover, the low intrinsic carrier effective mass in MHPs has led to their previously unprecedented performance in device applications such as solar cells, light-emitting diodes, and lasers.[52-55] Notably, the application of MHPs in field-effect transistors (FETs) has also attracted increasing attention recently.[6, 56, 57] On the one hand, the FET is a remarkable plateau for studying the charge transport properties of semiconductors under gate modulation; on the other hand, it plays a crucial role in the modern semiconductor industry. Thus, the development of high-performance perovskite transistors is of great economical value.

In the early period, the evolution of perovskite transistors was mainly based on Pb-

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based three-dimensional perovskite systems, such as methylammonium lead iodide ($MAPbI_3$).[58, 59] Soon after, it was found that the significant ion migration in three-dimensional perovskite systems resulted in serious screening effects, which hindered the observation of charge transport behavior.[60, 61] This led to the fact that most three-dimensional perovskite transistors could only operate at low temperatures and in ion-suppressed environments. [60, 61] Moreover, the high effective mass of charge carriers in Pb-based halide perovskites exacerbates charge transport difficulties, resulting in low mobility and critical issues such as instability and toxicity.[62] One solution to these issues is to substitute Pb^{2+} in perovskites with Sn^{2+} since the ionic radius of Sn^{2+} is similar to that of Pb^{2+} (Sn: 1.18 Å, Pb: 1.19 Å), but its smaller atomic mass increases charge carrier mobility and reduces Frölich interactions.[22, 63, 64] Another approach is to incorporate large organic cations to replace methylammonium (MA^+) cations and form two-dimensional perovskite systems. Compared to their three-dimensional counterparts, the layered structure of two-dimensional perovskites can alleviate the negative impact of ion migration.[65] In addition, the presence of bulk organic cations can impose a quantum confinement effect that limits the transport of charge carriers to controlled directions, thereby reducing scattering.[66] Based on the aforementioned principles, two-dimensional tin iodide perovskites have emerged as a promising material system for transistor applications. By replacing the Pb^{2+} ion with Sn^{2+} and incorporating large

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organic cations to form a two-dimensional structure, the detrimental effects of ion migration and high carrier effective mass in three-dimensional perovskite systems can be mitigated, leading to improved charge carrier mobility and reduced scattering. Moreover, the hydrophobicity of the organic cations can enhance the environmental stability of the material.[17, 67, 68]

Overall, the development of two-dimensional tin iodide perovskites represents an important advancement in the field of perovskite transistors and holds great potential for future technological applications.[69] The current state of the art in FET applications involves the use of two-dimensional phenylethylammonium iodide (PEA_2SnI_4) as the primary material. The highly ordered crystal arrangement of PEA2SnI4, facilitated by the π-π stacking between phenylethylammonium (PEA^+) cations, allows for desirable p-type charge transport behavior.[28] The first transistor utilizing PEA_2SnI_4, with a reported hole mobility (μh) of 0.62 $cm^2 V^{-1} s^{-1}$, employed a bottom-gate/top-contact (BG/TC) structure and utilized a typical spin-coating technique to prepare the perovskite layer.[29] Despite the promising results of the PEA_2SnI_4 transistor with a BG/TC structure, progress was halted until 2016, when Adachi et al. introduced a self-assembled monolayer (SAM) at the interface between the PEA_2SnI_4 layer and substrate. This SAM effectively improved the crystal orientation of the perovskite layer and enabled the demonstration of a two-dimensional perovskite transistor with a top-gate/top-contact TG/TC structure, which

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achieved a hole mobility (μ_h) as high as 15 $cm^2\ V^{-1}\ s^{-1}$.[28] The promising result of performance achieved by Adachi et al. using a self-assembled monolayer (SAM) at the PEA_2SnI_4/substrate interface has reignited interest in the development of perovskite transistors.

Despite the advancements in Sn-based perovskite transistors, they have been plagued by an inherent issue of easy oxidation from Sn^{2+} to Sn^{4+}, leading to undesirable p-doping and instability.[70] To tackle this problem, a plethora of studies have been conducted to improve the morphology and stability of perovskite films.[71] As an example, Teng et al. synthesized mixed Sn-Pb perovskites ($PEA_2Sn_xPb_{1-x}I_4$) taking into account the superior air, humidity, and light stability of Pb^{2+} over Sn^{2+}.[42] However, this approach resulted in a low μh value of 0.02 $cm^2\ V^{-1}\ s^{-1}$. Noh et al. recently introduced NaI into PEA_2SnI_4, which not only suppressed the oxidation of Sn^{2+} but also increased the grain size and passivated iodine vacancies at the grain boundaries.[42] Consequently, their findings demonstrated that the addition of 1 vol% NaI to the PEA_2SnI_4 transistor resulted in an increase in μh to 2.13 $cm^2\ V^{-1}\ s^{-1}$, as well as lower hysteresis and greater bias stability.[72] With the increasing number of these studies, the potential of 2D Sn-based perovskite transistors can be envisioned once the issues of stability are resolved.

As evident from the aforementioned enhancements, passivating the grain boundaries on the surface of perovskites is the most effective method of preventing degradation, as

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the surface is highly susceptible to defect formation. In reality, surface passivation of this kind has already been extensively implemented in perovskite solar cells and light-emitting diodes to enhance both their performance and stability.[71] As an example, You et al. utilized phenethylammonium iodide (PEAI) to post-treat the surface of $FA_{1-x}MA_xPbI_3$, which resulted in the highest recorded performance for perovskite solar cells at that time. They also showed that the PEAI existed as π-π stacked organic salts, rather than forming 2D PEA_2PbI_4 on the film's surface.[73] The aforementioned research team also used trioctylphosphine oxide (TOPO) to post-treat the surface of quasi-2D perovskites, which resulted in the highest recorded luminescence performance at that time.[74] The aforementioned findings clearly illustrate how surface passivation can enhance the performance of perovskite materials. Nevertheless, as of yet, the effectiveness of this approach has not been examined in perovskite transistors.

In this study, we conducted a systematic investigation of the effectiveness of surface passivation in improving the performance of 2D Sn-based perovskite transistors. We utilize PEAI and 4-fluorophenethylammonium iodide (FPEAI) as surface passivation agents for PEA_2SnI_4 and examine their impact on the charge transport characteristics and stability of the material, as illustrated in **Figure 2.1**. PEAI was selected due to its compatibility with the 2D framework and its role as one of the constituent precursors of PEA_2SnI_4. FPEAI, on the other hand, has stronger hydrophobic properties compared to

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PEAI and is expected to provide better protection against oxygen and moisture, thereby enhancing the ambient stability of PEA_2SnI_4 films.[75] Our findings indicate that both PEAI and FPEAI effectively passivate surface defects in PEA2SnI4 films and enhance charge transport properties. This is attributed to the electron-donating electron on nitrogen atoms in PEA^+ and $FPEA^+$ acting as Lewis bases to stabilize Sn^{2+} and decrease Sn vacancies. Additionally, it is noteworthy that these passivating agents have a p-doping effect on PEA_2SnI_4, which lowers the charge injection barrier with the Au electrode. Consequently, the use of PEAI and FPEAI as passivators resulted in a significant increase in the maximum μ_h of the devices, with values of 2.15 $cm^2\ V^{-1}\ s^{-1}$ and 2.96 $cm^2\ V^{-1}\ s^{-1}$, respectively, surpassing the control device value of 0.76 $cm^2\ V^{-1}\ s^{-1}$. In addition, our study shows that the bulky hydrophobic passivators, PEAI and FPEAI, act as a barrier to prevent the intrusion of oxygen and moisture, which significantly slows down the degradation of PEA_2SnI_4 and enhances its stability under ambient conditions. Additionally, the passivation of defects in the perovskite film by these passivators also contributes to improving the gate bias stability of the devices. In addition to their improved performance and stability, we found that PEA_2SnI_4 FETs with PEAI and FPEAI passivation exhibit non-volatile photomemory characteristics. This suggests that these devices have potential as perovskite-transistor-based memories. Perovskite-transistor-based memories have advantages over traditional perovskite-based floating-gate photo-

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memories because they do not require complex heterostructures and have better energy band alignment. Furthermore, these memories offer the ability to simultaneously transport and store charges, and the fabrication process is simpler.

2.2 Experimental Section

2.2.1 Materials

All reagents and solvents were purchased from Acros Organics, Tokyo Chemical Industry, Alfa Aesar, Sigma-Aldrich, and Lumtech Inc., and used as received without further purification.

2.2.2 Precursor Solution Preparation and Device Fabrication

The precursor solution of 2D PEA_2SnI_4 (with a concentration of 0.16 M) is prepared by dissolving PEAI and SnI_2 at a molar ratio 2:1 in DMF/DMSO with a volume ratio of 1:1. The solution was placed at room temperature for 30 min and then filtered by a 0.22 μm PTFE filter. A bottom-gate/top-contact transistor device was fabricated in this study for testing the transistor performance. The device was built on a highly n-doped Si substrate with a 100 nm SiO_2 gate dielectric layer (C_i = 29 nF cm^{-2}). The substrate was first cleaned with diluted detergent, deionized water, acetone, isopropanol, and toluene for 5 min in sequence, and then dried with a nitrogen gun and treated with plasma for 30

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min. Afterward, the PEA_2SnI_4 film was spin-coated onto the substrate at 4000 rpm for 50 s in an N_2-filled glovebox, followed by annealing at 100 °C for 10 min. Precursor solutions of the passivation layers were prepared by dissolving 0.5 mg/mL PEAI and FPEAI in a mixed solvent of IPA/Tol with a molar ratio of 1:12, respectively. The passivation layer was spin-coated onto the perovskite layer at 5000 rpm for 30 s, followed by annealing at 100 °C for 5 min. Finally, 50-nm contact gold electrodes were thermally deposited under a high vacuum (10^{-6} torr) through a shadow mask with defined channel length (L) and width (W) of 50 and 1000 μm, respectively. According to the saturation region of a transistor device, the field-effect mobility (μ) and the threshold voltage (V_{th}) can be determined using the following equation:

$$I_{ds} = \frac{W}{2L}\mu C_i(V_{gs} - V_{th})^2$$

where I_{ds} and V_{gs} were the source-to-drain currents and the source-gate voltage, respectively, and C_i was the capacitance of the 100 nm-SiO_2 gate dielectric layer (C_i = 29 nF cm^{-2}) that was measured per unit area.

2.2.3 Characterizations

SEM images were taken using Nova™ NanoSEM 230 field-emission SEM. XRD patterns were measured using Rigaku SmartLab SE. The absorption spectra were measured using Hitachi U-4100 UV–visible spectrophotometer. The film thickness was

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measured by Optical Thickness Meter. PL and TRPL spectra were recorded using a spectrometer (iHR320, HORIBA) coupled with a Hamamatsu C10910 streak camera and an M10913 slow single-sweep unit in the National Synchrotron Radiation Research Center (NSRRC, Taiwan) of TPS 23A section. Composition analysis was performed using X-ray photoelectron spectroscopy (XPS) PerkinElmer PHI 5400 equipped with a monochromatized Al Kα X-ray photon discharge lamp. The values of work function (WF) and valence band maximum (VBM) were determined using ultraviolet photoemission spectroscopy (UPS) with He I (photon energy = 21.20 eV) as the excitation source. Energy gaps were calculated from the Tauc plots under the assumption of direct bandgap. KPFM measurements were performed using a commercial AFM instrument (Bruker Innova) and using an aluminum-coated Si tip with a 7 nm radius of curvature. The FET performance was characterized using a Keithley 4200-SCS semiconductor parameter analyzer (Tektronix) in an N_2-filled glove box at room temperature under dark conditions. The photoresponse of the transistor device was recorded by illuminating the device with 405 nm wavelength irradiation light with an intensity of 30 mW. The processing conditions for a cycling test consist of sequential photo-driven programming (exposure to a 405 nm laser for 3 s), reading (V_g = 0 V for 10 s), electrical-driven erasing (V_g = -50 V for 3 s), and reading (V_g = 0 V for 5 s). The drain current is measured at a fixed V_{ds} of -50 V. In all stability test, samples were stored at air-conditioned temperature of 22 ºC

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with a relative humidity of 50-70%.

Kelvin probe force microscopy (KPFM) measurement. The y-axis in **Figure 2.4a-c** is the contact potential difference (CPD), which is the difference in the work function between the metal tip and the sample. It can be defined as $(\Phi_{tip} - \Phi_{sample})/e$, where Φ_{tip} and Φ_{sample} represent the work function of the metal tip and the sample, respectively All the measurement was conducted using the same metal tip and, therefore, Φ_{tip} is constant in all the measurements. As a result, CPD can be used to directly define the sample's work function. A lower CPD value represents a higher work function of the sample.

2.3 Result and Discussion

2.3.1 Basic Properties of PEAI/FPEAI-Passivated PEA_2SnI_4 Films

The main objective of our study, as shown in **Figure 2.2a**, was to examine how the surface passivation of PEA_2SnI_4 with PEAI and FPEAI would affect the performance and stability of the resulting BG/TC FETs. We aimed to understand the impact of these passivators on the material and device properties. We chose PEAI and FPEAI as surface passivators because they exhibit strong compatibility with the 2D framework of PEA_2SnI_4 and form strong interactions with the perovskite lattices, as has been previously reported in the literature.[73] Additionally, the highly hydrophobic properties of PEAI and FPEAI can effectively block the intrusion of moisture and oxygen, forming a protective layer on

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the surface of the PEA_2SnI_4 films, which can greatly enhance the ambient stability of the perovskite-based devices. In the Experimental Section, we provide a comprehensive description of the procedures used to prepare PEA_2SnI_4 films and perform surface passivation. It should be noted that the thickness of the passivation layer was limited to 5 nm or less to prevent an increase in the hole injection barrier at the interface between the perovskite and metal, as both PEAI and FPEAI are insulating materials. In the first step, the impact of surface passivation on the crystallinity of the PEA_2SnI_4 film was verified. **Figure 2.2b** demonstrates the X-ray diffraction (XRD) patterns of the PEA_2SnI_4 films with and without surface passivation. As can be seen in the figure, all the films exhibited a sharp peak at 5.4 degrees, corresponding to the (001) plane of PEA2SnI4 perovskite, and a weak peak at higher angles, corresponding to the (002) plane reflection. The higher intensity observed in the XRD pattern after passivation indicates an enhancement in crystallinity. The high intensity of the characteristic peaks in the XRD patterns suggests that the perovskite film has a highly ordered structure with an interlayer distance of approximately 16 Å, which is indicative of a layer-by-layer structure parallel to the substrate.[33] The Grazing-Incidence Wide-Angle X-ray Scattering (GIWAXS) pattern of the pristine PEA_2SnI_4 film is shown in **Figure 2.3**, which clearly shows an intense (002) signal along the q_z direction. This indicates that the film has a high level of crystallinity and is oriented parallel to the substrate, which confirms the results obtained from

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XRD.[23] In summary, the XRD and GIWAXS results indicate that the surface passivation did not negatively impact the crystallinity of the PEA_2SnI_4 films. The appearance of a peak at 4.7° in the XRD pattern indicates the presence of PEAI/FPEAI on the surface of the PEA_2SnI_4 film, confirming the successful attachment of the passivation layer.

Next, the surface morphology of these films was examined using scanning electron microscopy (SEM), as shown in **Figure 2.2c-e**. In the pristine film, we observed a complete grain size of approximately 20 μm with well-defined grain boundaries. In contrast, the films that were passivated with PEAI/FPEAI showed a significant increase in grain size and a reduction in the number of grain boundaries. Grain boundaries are often associated with defects, so minimizing their presence can help to decrease trap-assisted charge recombination.[76] The reason for the larger grain size seen in the passivated films is thought to be due to the surface recrystallization induced by PEAI/FPEAI. During this process, the PEAI/FPEAI interacts with any remaining unreacted Sn^{2+} cations, leading to an enlargement of the grains.[77]

Once we had examined the crystalline properties of the films, we proceeded to analyze their optical characteristics. **Figure 2.2f** shows the UV-Vis absorption spectra of the films. The UV-Vis absorption spectra of the pristine PEA_2SnI_4 film reveals three distinct peaks at 420 nm, 520 nm, and 625 nm. These peaks correspond to high-energy

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exciton transitions, intra-band transition processes, and intrinsic band-edge excitons, respectively.[78] The intensity of these absorption peaks decreases after surface passivation, and this effect is related to the thickness of the films. The passivation solvent used in the process etches away the top layer of defective surface and then stabilizes the Sn^{2+} underneath using PEA^{+}/$FPEA^{+}$. This process further decrease the film thickness, which is shown in the **Table 2.1.** Nonetheless, the overall absorption profiles of the films remain similar, indicating that their bulk crystal structures are comparable. **Figure 2.2g** displays the steady-state photoluminescence (PL) spectra of the films, which exhibit only one emission peak at 625 nm. This is because the emission of free excitons and the self-trapped emission overlap at room temperature.[79] An important observation is that the passivated film displays a significantly stronger PL peak than the pristine film. This can be attributed to the decrease in defects that occur after passivation, which consequently lowers the occurrence of non-radiative charge recombination. In perovskite structures, defects are known to generate intermediate states within the band gap, leading to thermal relaxation following the absorption of excitation light.[77, 80] The PEA_2SnI_4 film has both deep defects (such as Sn vacancies) and shallow defects (such as PEA and I vacancies and interstitials) present on its surface. Additionally, the presence of dangling bonds in the Sn atoms is also an important type of defect state.[81] When the PEA_2SnI_4 film undergoes surface treatment with PEAI/FPEAI, the vacant positions of both PEA

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and I can be occupied, and the unpaired electrons in the Sn^{2+} atoms can be neutralized by the lone pairs of amino groups present in PEAI/FPEAI.[82]

In order to gain more insight into the behavior of carriers within these films, the researchers conducted time-resolved photoluminescence (TRPL) measurements, and the corresponding findings are presented in **Figure 2.2h**. To determine the carrier lifetime, a biexponential function was used for fitting purposes:

$$I(t) = A_1\, exp\left(-\frac{t}{\tau_1}\right) + A_2\, exp\left(-\frac{t}{\tau_2}\right)$$

The biexponential function used to fit the carrier lifetime comprises of two components. The first component, τ_1, represents the rapid initial decay of carriers during the charge extraction process. The second component, τ_2, represents the slower decay that is dominated by nonradiative recombination at the bulk or interface of the channel layer.[83, 84]As presented in **Table 2.2**, there is a slight difference in the value of τ_1 when comparing the perovskite on glass slides without electrodes used for TRPL measurements. In this case, the rapid extraction of carriers from the perovskite to the electrode (τ_1) can be disregarded.[83, 84] Nevertheless, both films treated with PEAI/FPEAI exhibit significantly higher τ_2 values (1.35-1.36 ns) in comparison to the untreated film (1.06 ns). The observed increase in carrier lifetime implies that nonradiative recombination occurring at surface or channel defects can be mitigated. This is particularly advantageous for enhancing the charge transport characteristics of the film.

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2.3.2 Changes in Energy Levels and Ambient Stability

To investigate whether surface passivation has an effect on the energy levels of the PEA_2SnI_4 films, we conducted measurements on the work function of the films using a Kelvin probe force microscope (KPFM). More details on the measurements can be found in the Supporting Information, and the corresponding results are presented in **Figure 2.4a-c**. The results clearly indicate a sharp drop in the contact potential difference (CPD) value after surface passivation. In fact, the CPD values of the PEAI/FPEAI-passivated films were nearly 500 mV lower than that of the untreated PEA_2SnI_4 film. As a lower CPD value corresponds to a higher work function, these findings suggest that both PEAI and FPEAI can p-dope PEA_2SnI_4 to increase its work function.[85]

To confirm the potential p-doping effects of PEAI/FPEAI, we performed ultraviolet photoelectron spectroscopy (UPS) analysis on the films. The resulting Fermi level and valence band of each film were determined through its cut-off region, as shown in **Figure 2.4d.** In our previous analysis, we estimated the band gap of each film by constructing a Tauc plot (**Figure 2.5**) from its UV-Vis absorption spectra. Our findings revealed that all three films, irrespective of their passivation status, exhibit a similar band gap of approximately 1.97 eV. This is due to the identical bulk quantum confinement of the organic cations in the film.[86] **Figure 2.4e** presents a schematic representation of the

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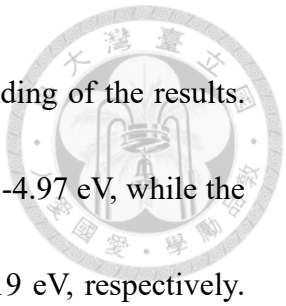

calculated energy levels for each film to provide a clearer understanding of the results. The valence band maximum (VBM) of the pristine PEA_2SnI_4 film is -4.97 eV, while the values for the PEAI- and FPEAI-passivated films are -5.05 and -5.19 eV, respectively. Since the VBM is primarily determined by the Sn 5s and I 5p orbitals,[85] the presence of iodide-rich passivators (PEAI and FPEAI) results in a reasonable downshift of the VBM values in the passivated perovskite films. It is worth noting that the VBM values of the PEAI/FPEAI-passivated films with respect to the Fermi level are smaller (0.62-0.63 eV) than the value of the pristine film (0.71 eV) (**Figure 2.4d**). This indicates that the passivated perovskite films have improved p-type characteristics in comparison to the pristine film. This is due to the increased bulk hole concentration resulting from the facilitated transfer of electrons from the perovskite to the surface passivator.[87] It is important to note that the energy levels of the FPEAI-passivated film are deeper compared to the PEAI-passivated film. This can be attributed to the presence of the fluorine atom in FPEAI, which has a strong electron-withdrawing property. This property enhances the transfer of electrons, leading to further downshifts in the energy levels of the passivated perovskite films.[85] Based on the KPFM and UPS results, it can be concluded that the surface passivation of PEAI/FPEAI induces p-doping in the PEA2SnI4 film. The enhanced p-type characteristics of the passivated films are expected to improve the hole transport in the resulting FET devices by reducing the hole injection barrier at the

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perovskite/Au interface, as illustrated in **Figure 2.4e**. As widely acknowledged, Sn-based perovskites are prone to degradation and oxidation in the presence of air. Research has indicated that when photoexcited, PEA_2SnI_4 can become unstable and donate electrons to physically adsorbed oxygen molecules, resulting in the formation of superoxide (O^{2-}).[88] Moisture present in the air can further react with the perovskite film, leading to its hydrolysis into PEAI and SnI_4.[89] Given that the surface passivators being studied are hydrophobic in nature, we proceeded to examine how effective they are in slowing down the penetration of oxygen and moisture into the passivated films. To investigate this, we analyzed the XRD patterns of unpassivated PEA_2SnI_4 and passivated PEAI/FPEAI films under different durations of air exposure, as illustrated in **Figure 2.6a-c**. The peak at 5.4° was enlarged to better visualize any changes in the peak, and the XRD data of the fresh films were also shown for comparison (**Figure 2.7**). The XRD patterns of the pristine PEA_2SnI_4 film show a significant decay in peak intensity at 5.4° when exposed to air for more than 60 minutes. This decay is accompanied by an increase in peak intensity at 4.7°, which corresponds to the formation of PEAI. These changes are attributed to the degradation of the $[SnI_6]^{4-}$ layer caused by oxidation, as mentioned previously. In contrast to the pristine film, the passivated films demonstrated almost no change in their XRD patterns regardless of the air exposure time, indicating higher stability in ambient conditions. This can be attributed to the improved hydrophobic properties of the

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passivated films. The contact angle measurements (shown in **Figure 2.8a-c**) revealed that the PEAI- and FPEAI-passivated films had higher contact angles than the pristine film, indicating that they had a lower affinity for water and better resistance to water intrusion, thereby retarding perovskite degradation.[90] The result indicates that the passivation of the PEA_2SnI_4 film surface is effective in improving the stability of the film in ambient conditions.

We further investigated the changes in the optical absorption of the films over time. **Figure 2.9a-c** shows that the peak intensity at 610 nm gradually decreased with prolonged air exposure time for all films, but at different rates. To better illustrate the difference in degradation rates, the normalized absorption intensity at 610 nm, relative to the absorption intensity in the fresh state, is shown for different air exposure times in **Figure 2.6d.** The normalized absorption intensity at 610 nm for films with different air exposure times shows that the degradation of the pristine film is the fastest, with the light absorption intensity decreasing to nearly half after 75 minutes of air exposure. In contrast, the PEAI/FPEAI-passivated films retained about 60% of their initial absorption intensity, indicating the effectiveness of the surface passivation layer in slowing down degradation.

X-ray photoelectron spectroscopy (XPS) measurements were conducted on both fresh and air-exposed films to further verify the protective effect of the passivation layer. The core level spectra of Sn $3d_{3/2}$ and Sn $3d_{5/2}$ at 485.5 and 494 eV, respectively, were

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observed in all fresh films, as shown in **Figure 2.6e**. These two valence-state peaks were deconvoluted, and an additional shoulder peak at a lower binding energy was also observed for the pristine film, which was attributed to undercoordinated Sn in the oxidation state denoted as $Sn^{\delta<2+}$.[24, 91] However, this peak was significantly reduced or almost disappeared after PEAI/FPEAI passivation, suggesting that surface passivation can prevent the oxidation of Sn^{2+}. Moreover, the intensity ratio of Sn^{2+}:Sn^{4+} increased from 78:16 in the pristine film to 93:3 in the PEAI-passivated film and 94:6 in the FPEAI-passivated film. These findings indicate that surface passivation can not only enhance the crystallinity of the perovskite film but also improve its stability by inhibiting the oxidation of Sn^{2+}. The detection of a fluorine 1s signal on the FPEAI-passivated film surface further confirms the presence of FPEAI passivation (**Figure 2.10**). After exposure to air for 60 minutes (**Figure 2.6f**), it was observed that the content of Sn^{4+} and $Sn^{\delta<2+}$ increased in all films due to interactions with oxygen and/or water. However, when comparing the intensity of $Sn^{\delta<2+}$:Sn^{2+}:Sn^{4+} before and after aging, it was evident that the passivated films displayed better ambient stability. This is because the nitrogen atom in PEAI/FPEAI possesses a lone pair of electrons that can form Lewis acid-base pairs with the Sn atom, thus stabilizing it and preventing the oxidation of the perovskite surface.

2.3.3 FET Performance, Ambient Stability, and Gate Bias Stability

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In the final part of the study, the researchers made FET devices from the three different perovskite films and conducted measurements to investigate their charge transport properties. The devices were named pristine, PEAI, and FPEAI, and their transfer curves are presented in **Figure 2.11a-c**, while the corresponding output curves are shown in **Figure 2.11d** (for the PEAI device) and **Figure 2.12** (for the pristine and FPEAI devices). Details of the device fabrication and measurements can be found in the Experimental Section of the paper. Consistent with previous studies in the literature, the devices demonstrated typical p-type transport properties, and their relevant performance parameters are listed in **Table 2.3**.[92] The absence of zigzag structures and the smoothness observed in the transfer curves of our fabricated devices indicate their high quality and reliability. Furthermore, the threshold voltage (V_{th}) of our devices is lower than what has been previously reported in the literature, which suggests that our films have fewer self-doped states and a better quality overall.[37]

The maximum hole mobility (μ_h) of the PEAI and FPEAI devices were found to be 2.15 $cm^2 V^{-1} s^{-1}$ and 2.96 $cm^2 V^{-1} s^{-1}$, respectively, which is almost four times higher than the pristine PEA2SnI4 device with a μ_h of 0.76 $cm^2 V^{-1} s^{-1}$. The mobility statistics of 10 different devices are shown in **Figure 2.11e**, where both the PEAI and FPEAI devices exhibit higher mobility than the pristine device. Remarkably, our champion device shows one of the best performance values reported for 2D tin perovskite FETs to date, as

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summarized in **Figure 2.13**. Interestingly, we observed that the on/off current ratio of the FPEAI device is higher than that of the PEAI device, although the hysteresis is reduced, indicating fewer traps inside. This suggests that the presence of fluorine atoms not only blocks moisture as mentioned before, but also has a positive effect on the perovskite lattice, enhancing charge transport. It seems that the fluorine atoms play a role in stabilizing the lattice, leading to improved device performance. The passivators used in this study not only improve device performance by introducing p-doping effects but also by improving the alignment of energy levels between the perovskite and the electrodes. As a result, we observe significantly higher on-currents in the PEAI and FPEAI devices compared to the pristine device (as shown in **Figure 2.11a-c**), while their off-currents remain similar. This suggests that the facilitated hole transport plays a major role in improving the device performance. Having a high on/off current ratio is desirable for FET devices. To confirm that the improved performance is due to the PEAI/FPEAI passivation and not the antisolvent cleaning, we fabricated a FET device using a perovskite film treated only with pure solvent, and compared its performance to the passivated devices. The transfer curve of this device is presented in **Figure 2.14** and its performance is summarized in **Table 2.3** as well. The results show that the pure solvent-treated device had poor performance, with lower μ_h and increased hysteresis, indicating that pure solvent cleaning has a negative impact on device performance. This confirms the effectiveness of

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PEAI/FPEAI passivation in improving device performance.

As previously mentioned, the surface passivation significantly improves the environmental stability of the PEA_2SnI_4 film. To investigate this further, we compared the environmental stability of the fabricated FET devices. Specifically, the FET devices were removed from the N_2-filled glovebox, stored in ambient air for a certain period, and then returned to the glovebox for performance measurements. The results, presented in **Figure 2.15**, clearly show the dynamic process of oxygen doping in the variation of the transfer curves, highlighting the degradation of the device performance over time. To better illustrate the differences in aging behavior between the devices, we plotted the changes in mobility as a function of air exposure time in **Figure 2.11f**. As expected, the pristine device exhibited the fastest degradation rate, with a steep linear decline in mobility that resulted in a drop to half of its initial value after only 30 minutes of air exposure, and a drop to one-tenth after 75 minutes. In contrast, the PEAI and FPEAI devices showed significantly slower rates of mobility decline, with both maintaining about half of their initial mobility values after 75 minutes of air exposure. This highlights the advantage of surface passivation in enhancing the ambient stability of the devices, as the PEAI and FPEAI passivators effectively mitigate the impact of ambient oxygen on the perovskite film. Overall, these findings provide further evidence of the effectiveness of surface passivation in improving the performance and stability of perovskite-based

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FET devices.

Aside from ambient stability, another critical factor for practical applications is the long-term stability of the devices under gate modulation. This is essential in ensuring high device quality and minimizing degradation over time.[40] In this regard, we examined the transfer curves of the devices for various bias times at a fixed gate bias (Vg) of -50 V, and the results are shown in **Figure 2.16**. The V_{th} shift versus gate bias time is plotted in **Figure 2.17a**, and it is evident that with increasing gate bias time, V_{th} gradually shifts to a more negative direction. This shift is caused by an increasing number of carriers that are trapped in the channel layer and/or the channel/dielectric interface due to the defects generated by perovskite degradation.[40] The accumulation of trapped carriers in the channel layer and/or channel/dielectric interface changes the energy band of the FET devices, which in turn requires a higher gate bias voltage (V_g) to release them.[56] The data shown in **Figure 2.17a** indicate that the PEAI and FPEAI devices experience significantly smaller V_{th} shifts compared to the pristine device as the gate bias time increases. This suggests that the passivation process is effective in reducing the number of defects present in the devices, resulting in fewer trapped carriers and therefore smaller changes in the energy band. These findings support the earlier observations on the trap-filling effect of surface passivation and highlight its importance in improving the stability of the FET devices.

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2.3.4 Phototransistor Characteristics

Perovskites have been recognized as highly efficient components for converting light into electrical energy for a while now.[93] Given their demonstrated superior charge transport properties, we proceeded to study and compare the photoresponse of these three devices. We also examined the ability of these devices to retain their performance over time by subjecting them to 3 seconds of blue light (405 nm and 30 mW) irradiation, and the outcomes are presented in **Figure 2.17b**. As can be observed from the results, all three devices displayed a significant increase in current at V_g = 0 V and V_d = -50 V after being exposed to light. This effect is attributed to the strong photosensitivity of PEA_2SnI_4, which generates a large number of photoexcited excitons that dissociate into electrons and holes. Additionally, the impressive long-term retention of the PEA_2SnI_4 FETs, which persisted for at least 1200 seconds and potentially even longer, highlights their non-volatile photomemory characteristics.[35] Interestingly, the devices that underwent passivation exhibited greater on-currents compared to the pristine device following irradiation, indicating a higher dissociation rate of excitons in the passivated perovskite films. This improvement is attributed to the reduction of defects present on the perovskite surface, as well as improved energy level alignment at the electrode interfaces, which was previously discussed.

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As the non-volatile memory features were observed in all three devices, we proceeded to evaluate their retention properties, which are presented in **Figure 2.17c**. To simplify the comparison, the peak on-currents of each device were normalized and overlapped. Furthermore, we applied a biexponential function [Eq. (1)] to fit the charge retention lifetime of each device, which allowed us to clarify their charge storage capability. The τ_{avg} value was then calculated using a specific equation:

$$\tau_{avg} = \frac{\sum_i A_i \tau_i}{\sum_i A_i}$$

The results are presented in **Figure 2.17c**, where it can be observed that the τ_{avg} value of the pristine device is higher than that of the PEAI and FPEAI devices. This suggests that the pristine device has a slower charge recombination rate, which is indicative of a higher concentration of deep defects in the PEA_2SnI_4 film.

To better understand the differing electron storage behaviors observed in these devices, we propose several potential mechanisms, which are illustrated in **Figure 2.18**. When subjected to blue light irradiation, a large number of photo-induced hole-electron pairs are generated and dissociated. The photo-generated holes travel to the electrode, while the electrons become trapped by defects present in the perovskite film, such as Sn vacancies or PEA/I vacancies and interstitials. Furthermore, the energy level mismatch at the interface between the perovskite and electrode can indirectly create charge trapping sites, which can lead to non-radiative recombination.[94] Consequently, in the pristine

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device, there is a greater occurrence of non-radiative recombination taking place on the surface of the perovskite film. Conversely, with PEAI and FPEAI serving as passivators, the holes are able to travel across the electrode interface more smoothly due to an improved energy level alignment. After the light irradiation is removed, the photo-generated holes and trapped electrons recombine, resulting in a decrease in the transient current. However, since the pristine PEA_2SnI_4 device contains deeper trapped states, a greater number of trapped electrons are stabilized in these states. Consequently, the hole current is sustained and the recombination process is delayed in the case of the pristine film. This leads to a longer hole carrier lifetime compared to the other two devices, as shown in the table included in **Figure 2.17c**. In summary, passivation with PEAI/FPEAI enhances the photoresponse of the perovskite transistor by reducing the defects present on the perovskite film surface; however, the pristine device exhibits a longer charge retention time due to the higher trap density in the perovskite film.

The switching stability of the tin perovskite photomemory was thoroughly assessed using the photon writing-reading electrical erasing-reading (WRER) technique, as presented in **Figure 2.17d**. All three devices demonstrated reversible switching behaviors between the on and off states, exhibiting rapid responses from 10^{-9} to 10^{-5} under illumination. It is noteworthy that the passivated devices, i.e., the PEAI and FPEAI devices, exhibited higher on-currents and thus higher conductivity than the pristine device,

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while their off-currents remained similar, leading to higher on/off current ratios as depicted in **Figure 2.17f**. It is particularly worth mentioning that the FPEAI device outperformed the other two devices, delivering the highest photoresponse. This can be attributed to the higher stability and better energy alignment achieved by the fluorinated PEAI passivation layer. Therefore, this study demonstrates that the WRER technique is a reliable tool for evaluating the switching stability of tin perovskite photomemory devices, and the passivation layer can significantly enhance their performance and stability. In order to evaluate the stability of the tin perovskite photomemory devices, WRER cycling loops were performed on devices that were exposed to ambient air for 15 minutes. The results, shown in **Figure 2.17e**, indicate that the devices experienced varying degrees of degradation after exposure to air, with an increase in both on- and off-currents. This can be attributed to the doping effect of oxygen in the ambient air, which induces more hole carriers by oxidizing Sn^{2+} to Sn^{4+}. Interestingly, the PEAI and FPEAI devices showed smaller increases in off-current and higher on-currents compared to the pristine device, resulting in larger on/off current ratios than the fresh devices (**Figure 2.17f**). This suggests that proper doping of the perovskite film can enhance the photomemory performance for passivated devices. Importantly, the comparison in **Figure 2.17f** also highlights the improved air stability with less off-current increment after passivation, providing further evidence for the stability enhancement.

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2.4 Conclusion

In this study, we have shown that passivating the surface of PEA_2SnI_4 films with PEAI/FPEAI significantly improves the performance and stability of the associated perovskite transistors. This was achieved by reducing surface defects and increasing the grain size, which was accomplished through surface recrystallization. The electron-donating pairs of nitrogen atoms on PEA^+ and $FPEA^+$ acted as Lewis bases to stabilize Sn^{2+} and reduce Sn vacancies, resulting in a more stable film. Additionally, these passivators were able to p-dope the PEA_2SnI_4 film, promoting better energy-level alignment with the electrode and enabling efficient charge transfer. Overall, this work highlights the importance of surface passivation in enhancing the performance and stability of perovskite transistors, which has significant implications for the development of advanced optoelectronic devices. The PEAI- and FPEAI-passivated devices demonstrated a significant increase in the maximum hole mobility (μ_h), with values of 2.15 and 2.96 $cm^2\ V^{-1}\ s^{-1}$, respectively, compared to the control device, which had a μ_h of only 0.76 $cm^2\ V^{-1}\ s^{-1}$. These hydrophobic passivators also provided protection against ambient air-induced degradation of the PEA_2SnI_4 film, as evidenced by XPS, UV, and XRD analysis. Moreover, they enhanced the gate bias stability of the devices by reducing defects in the perovskite film. Ultimately, we showcase the non-volatile photomemory behavior of the perovskite transistors and leverage them for perovskite-transistor-based

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memories. Moreover, surface passivation with PEAI/FPEAI not only decreases the surface defects and improves the air stability of the perovskite film, but also enhances the photoresponse of the device. However, it comes at a cost of reduced charge retention time caused by the reduction of trap density.

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Figures

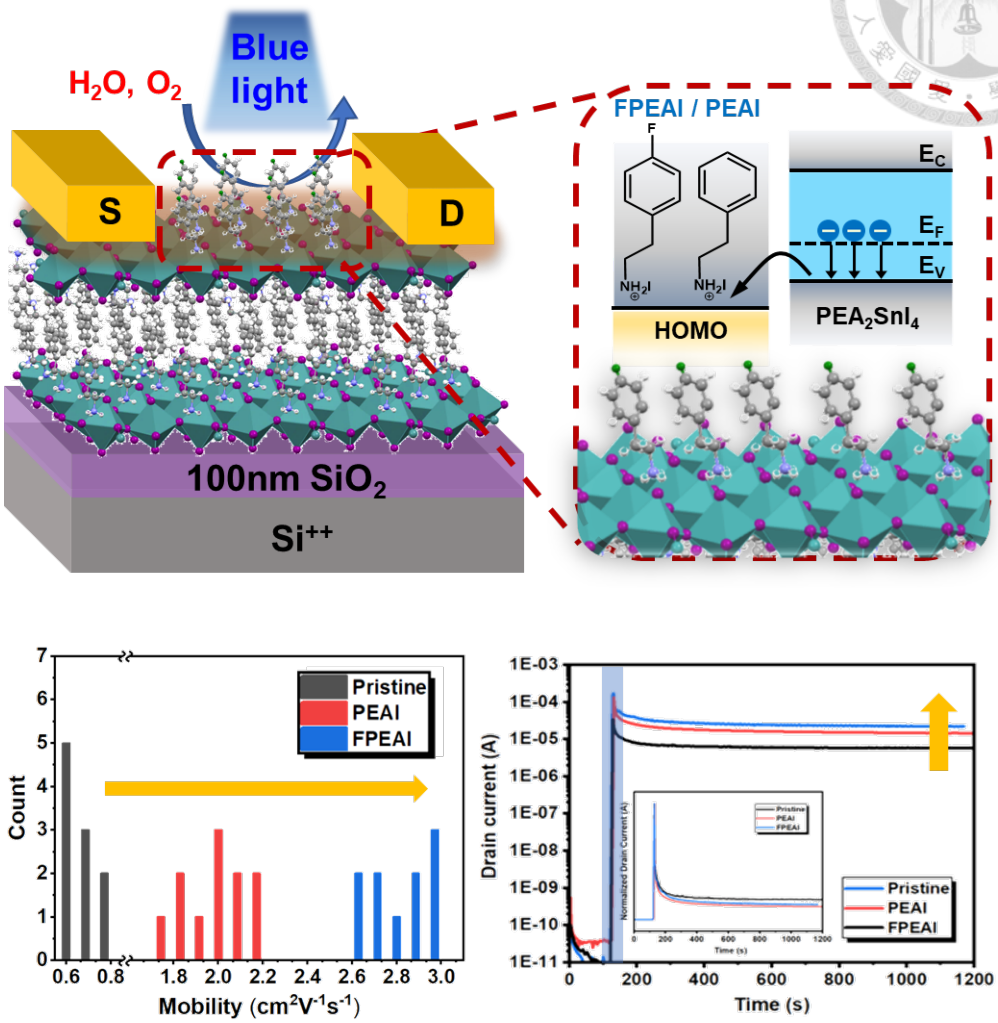

Figure 2.1 The main figure of contents of this chapter.

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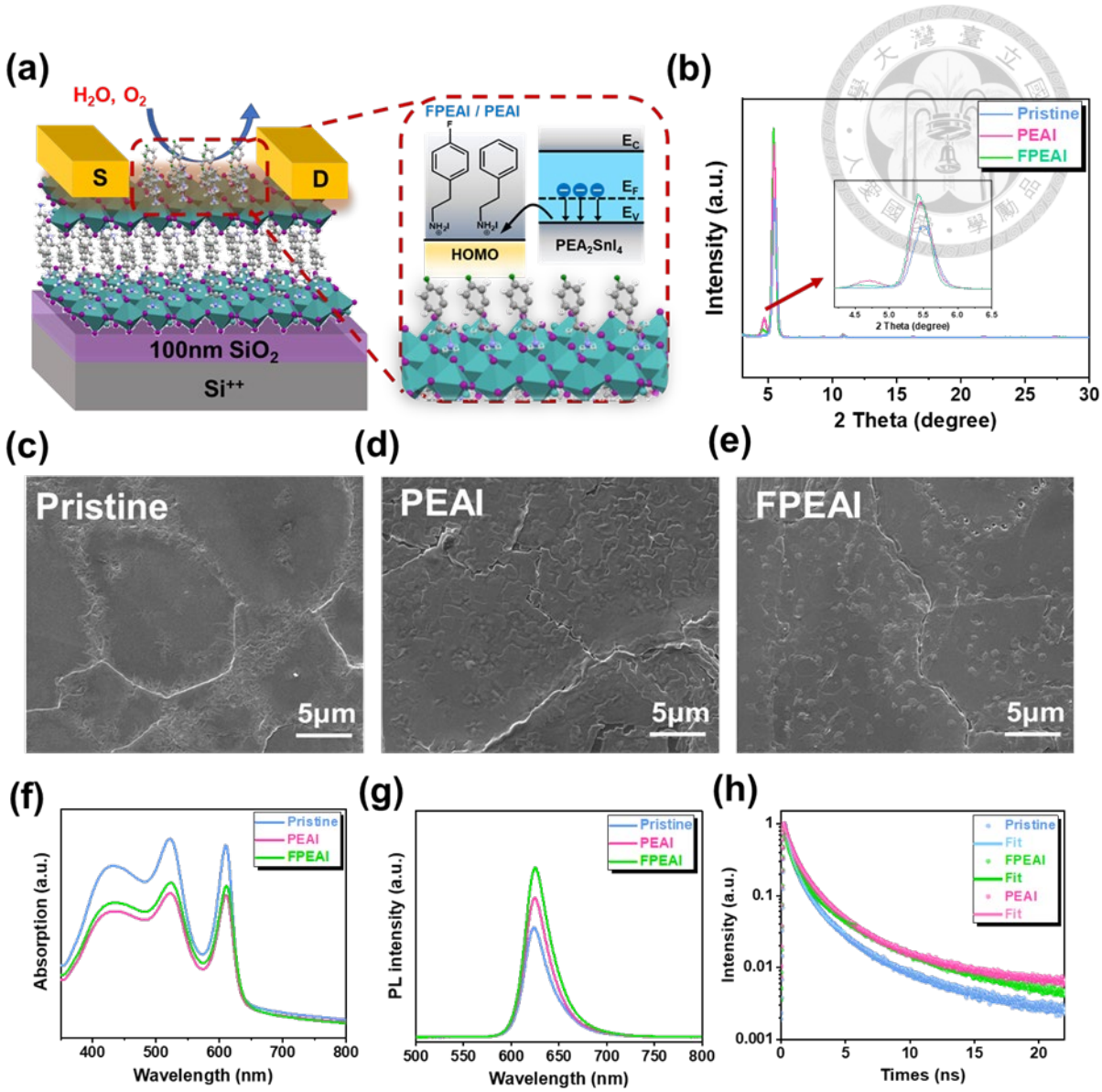

Figure 2.2 (a) Schematic device structure with the studied surface passivators. (b) XRD patterns and (c-e) SEM images (under x 10000 magnification) of (c) pristine PEA_2SnI_4, (d) PEAI-passivated, and (e) FPEAI-passivated films. (f) UV-vis absorption spectra, (g) PL emission spectra, and (h) TRPL spectra of the pristine and PEAI/FPEAI-passivated films.

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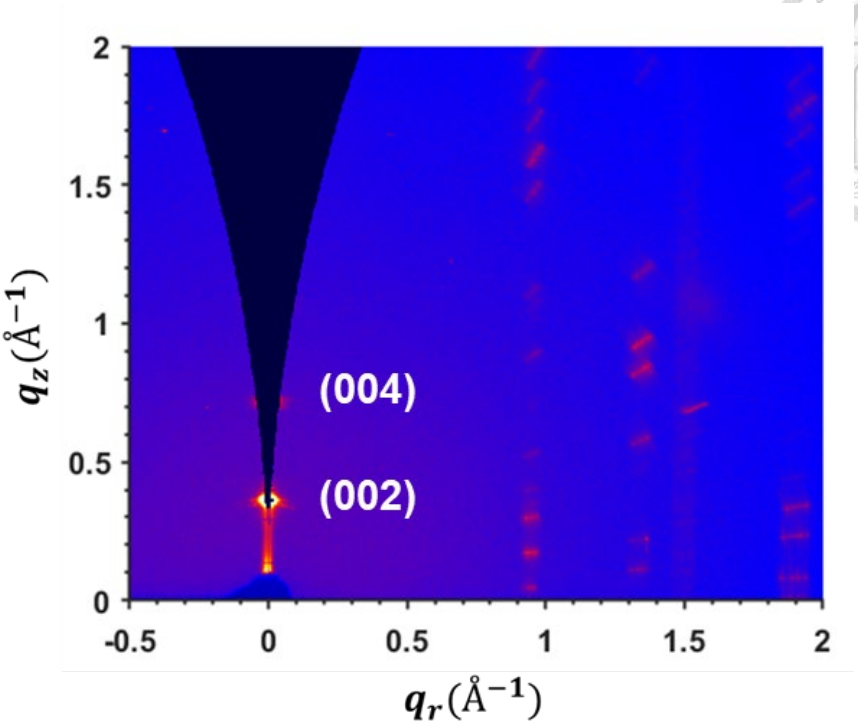

Figure 2.3 GIWAXS pattern of the PEA_2SnI_4 film.

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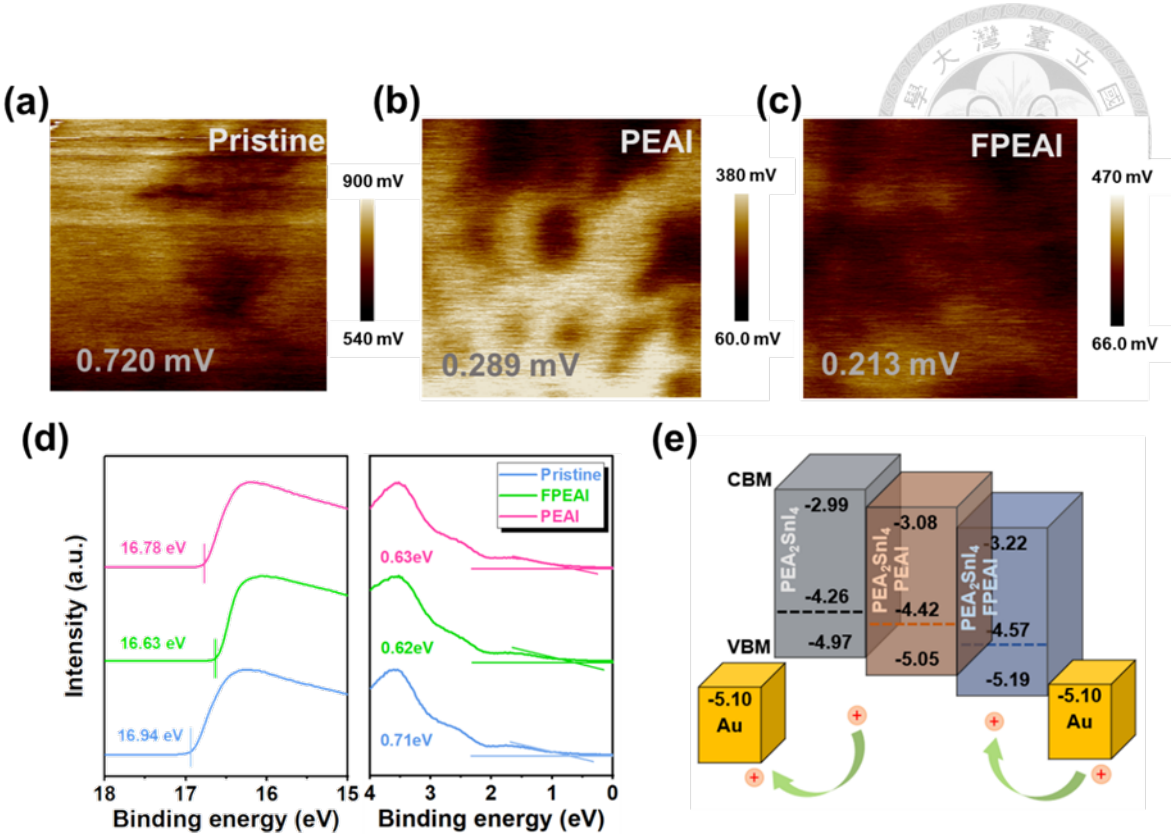

Figure 2.4 KPFM spectroscopy for (a) pristine PEA_2SnI_4, (b) PEAI-passivated, and (c) FPEAI-passivated films. (d) UPS spectroscopy and (e) the corresponding energy level schematic for the studied three films.

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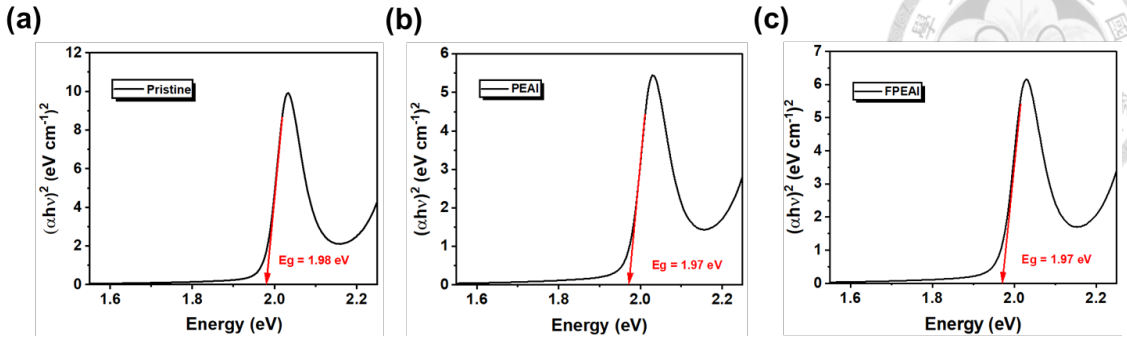

Figure 2.5 Tauc plot and band gap calculation for (a) the pristine PEA_2SnI_4 film and (b) PEAI- and (c) FPEAI-passivated PEA_2SnI_4 film.

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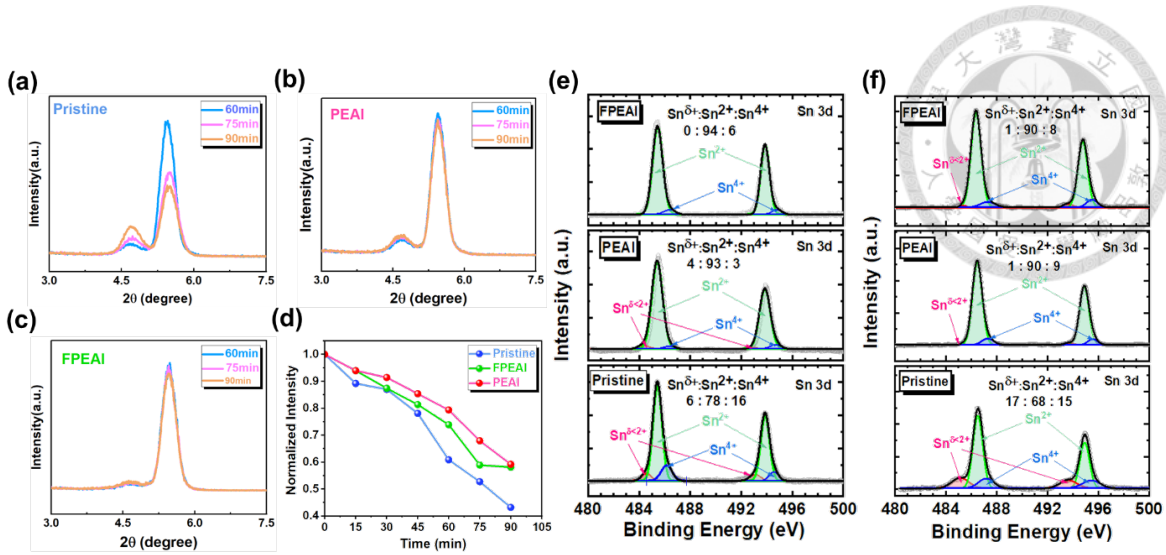

Figure 2.6 XRD patterns of (a) pristine PEA_2SnI_4, (b) PEAI-passivated, and (c) FPEAI-passivated films at different air exposure times. (d) Normalized absorption intensity (relative to the absorption intensity of the fresh state) at 610 nm in Figure S4 for different air exposure times. XPS of Sn 3d core peaks performed on (e) fresh films and (f) films exposed to air for 60 minutes. In the stability test, samples were stored at air-conditioned temperature of 22 °C with a relative humidity of 50-70%.

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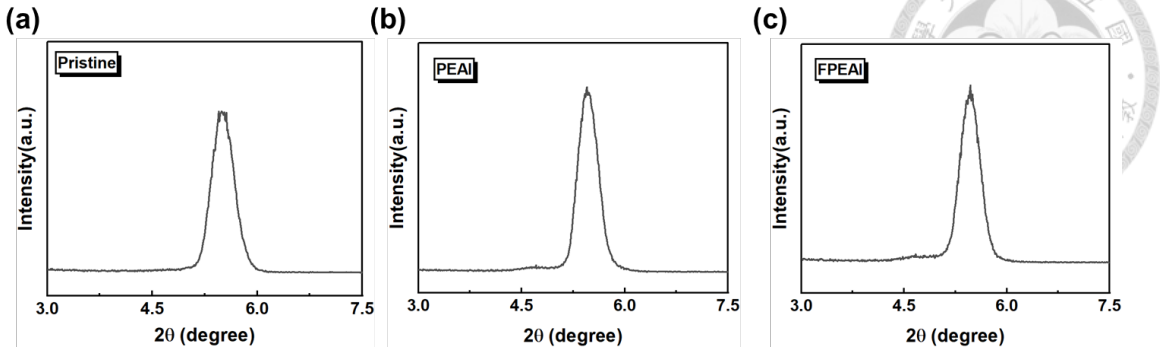

Figure 2.7 XRD patterns of the fresh (a) pristine PEA_2SnI_4, (b) PEAI-passivated, and (c) FPEAI-passivated films.

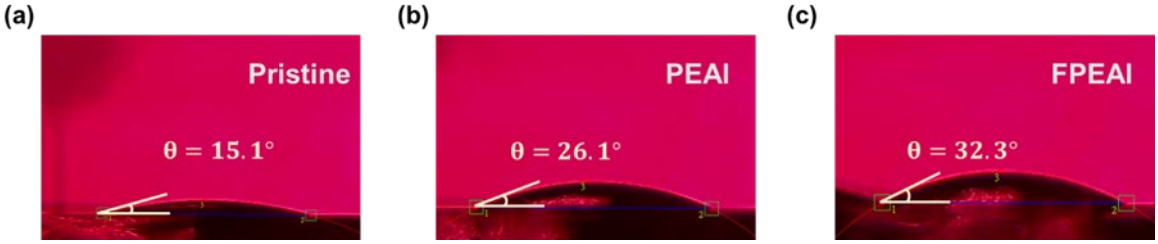

Figure 2.8 The contact angle of (a) pristine PEA_2SnI_4, (b) PEAI-passivated, and (c) FPEAI-passivated films.

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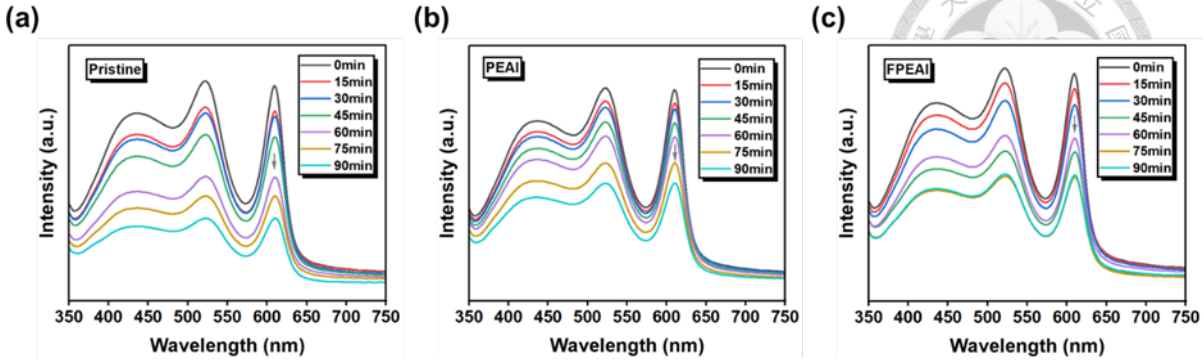

Figure 2.9 UV-Vis spectra of (a) pristine PEA_2SnI_4, (b) PEAI-passivated, and (c) FPEAI-passivated films at different air exposure times.

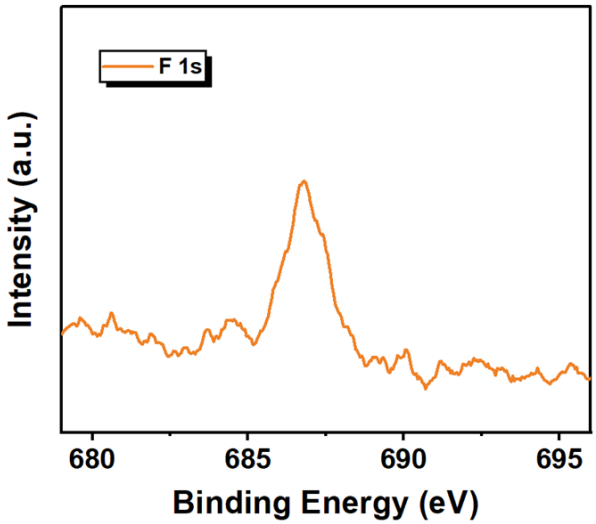

Figure 2.10 XPS of fluorine 1s core peak performed on the FPEAI passivated film.

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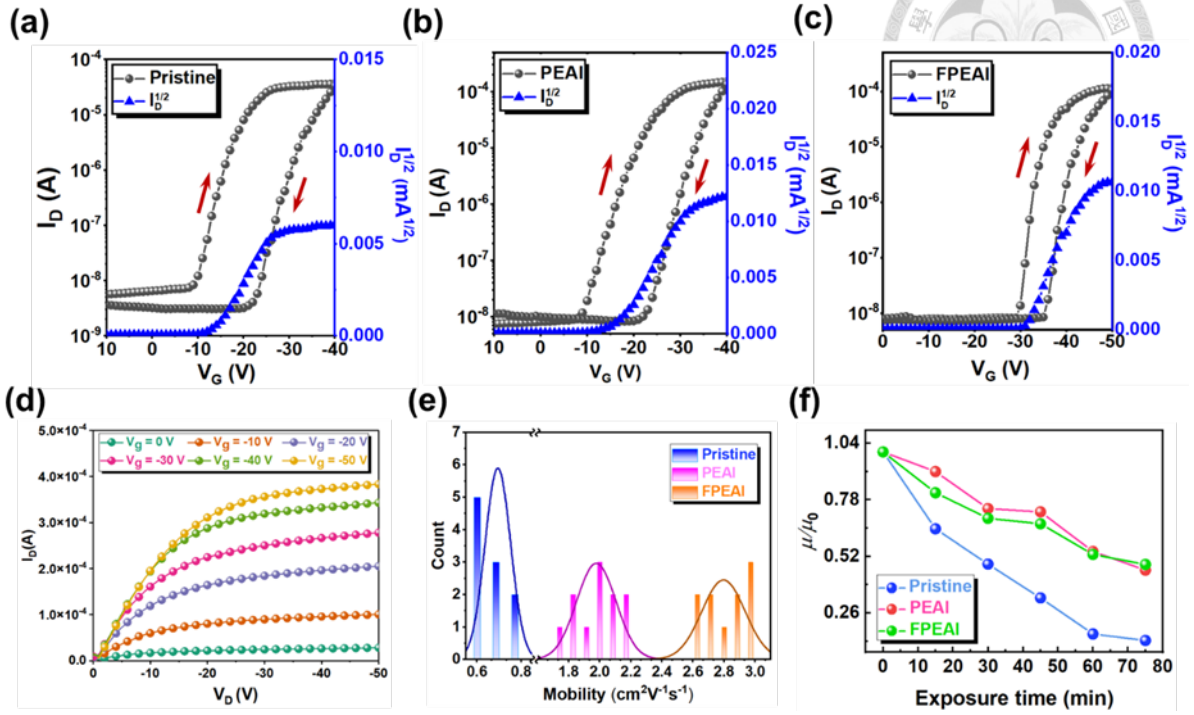

Figure 2.11 Transfer curves of (a) the pristine device, (b) the PEAI device, and (c) the FPEAI device. (d) Output curve of the PEAI device. (e) Mobility statistics of the studied FET devices on ten different devices. (f) Normalized mobility variations as a function of aging time in ambient air.

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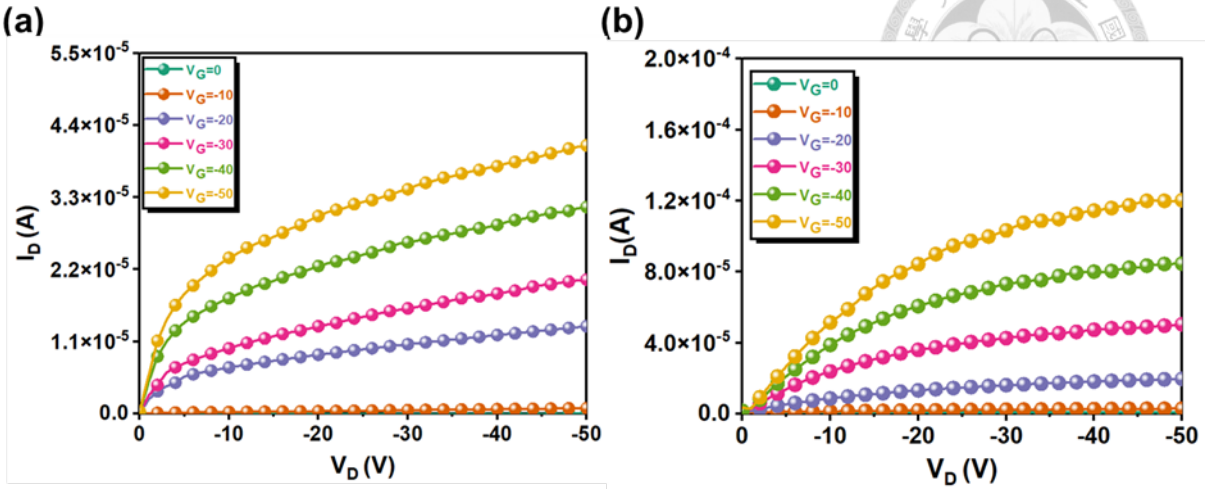

Figure 2.12. Output curves for (a) the pristine device and (b) the FPEAI device.

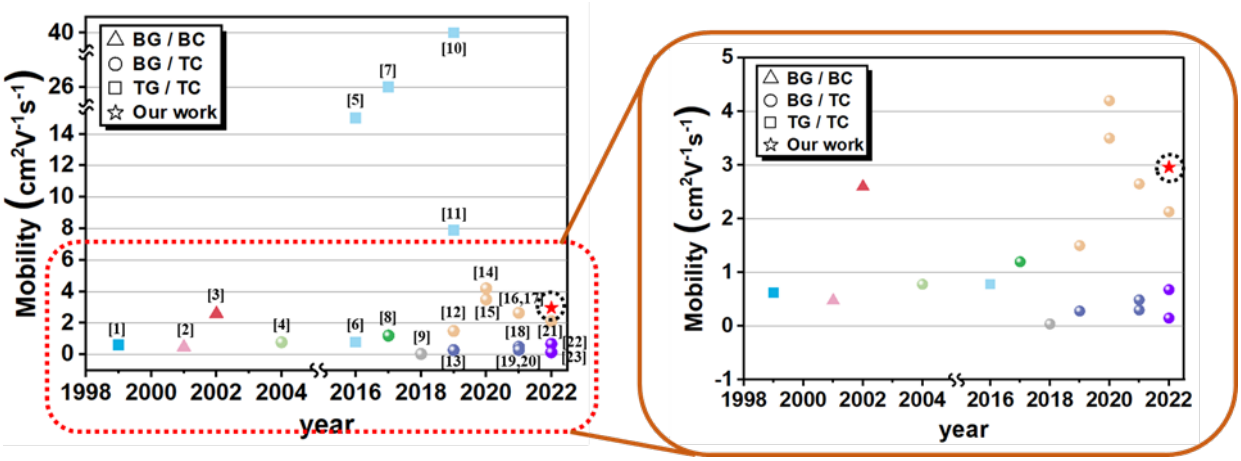

Figure 2.13. Historical reported 2D tin perovskite FETs performance. The same color marking represents the same laboratory group. The numbering beside the point corresponds to the reference below.

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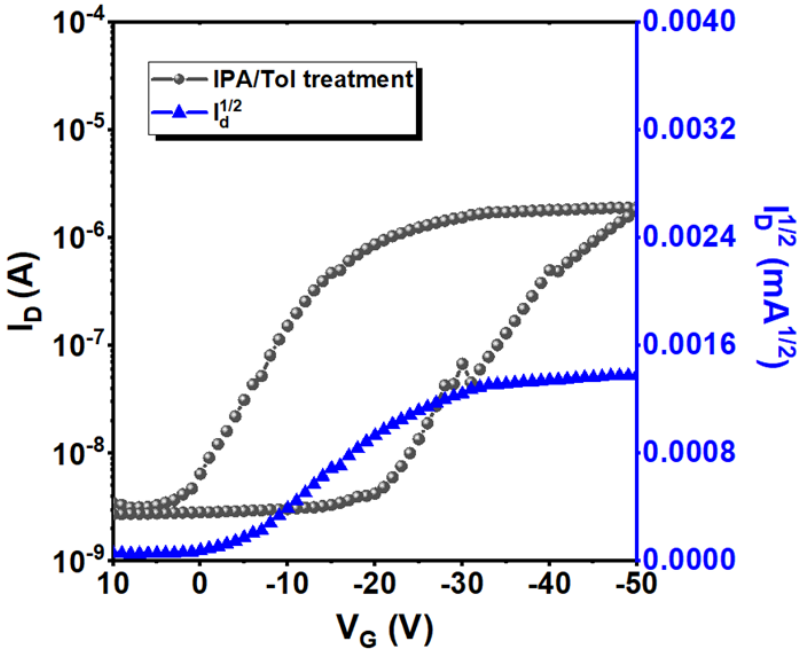

Figure 2.14 Transfer curve of the FET device with pure solvent-treated perovskite film.

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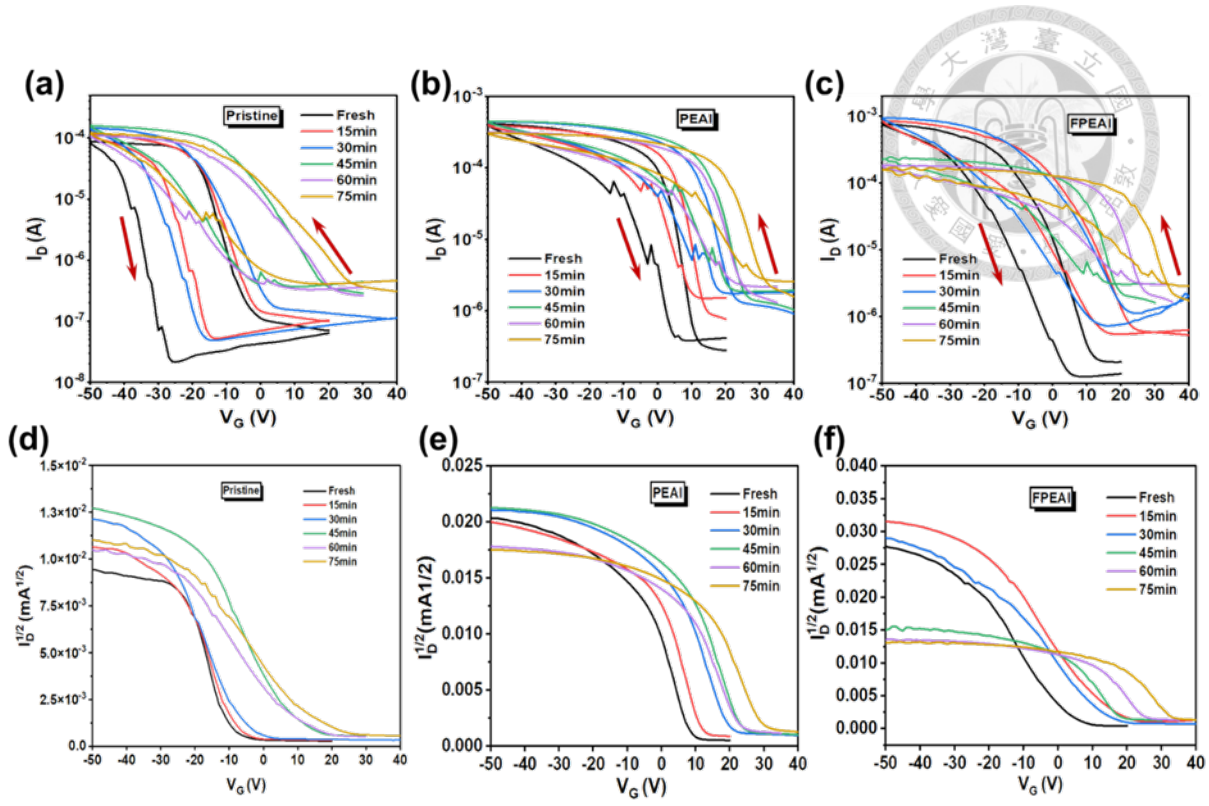

Figure 2.15 (a-c) The transfer curves and (d-f) the corresponding square roots of drain currents of (a,d) the pristine device, (b,e) the PEAI device, and (c,f) the FPEAI device for different aging times in ambient air.

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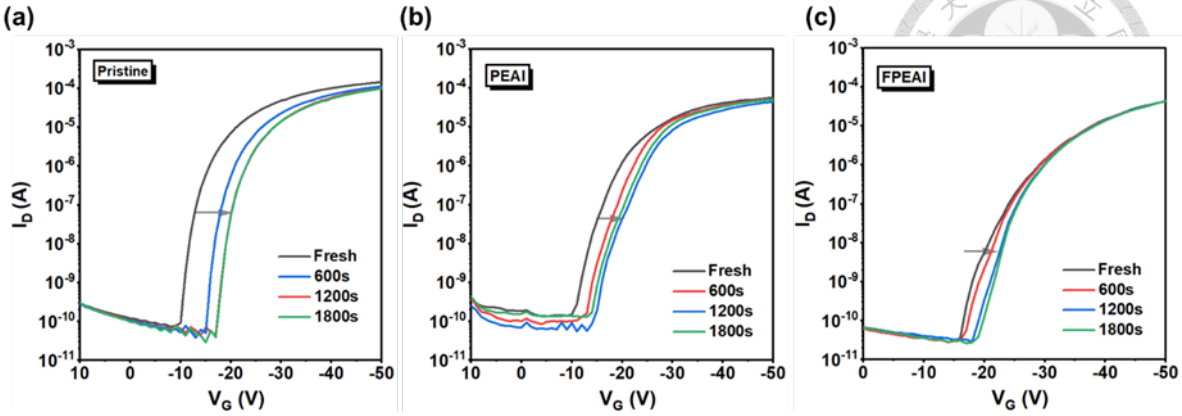

Figure 2.16 The transfer curves of (a) the pristine device, (b) the PEAI device, and (c) the FPEAI device for different bias times at a fixed gate bias (V_g) of -50 V.

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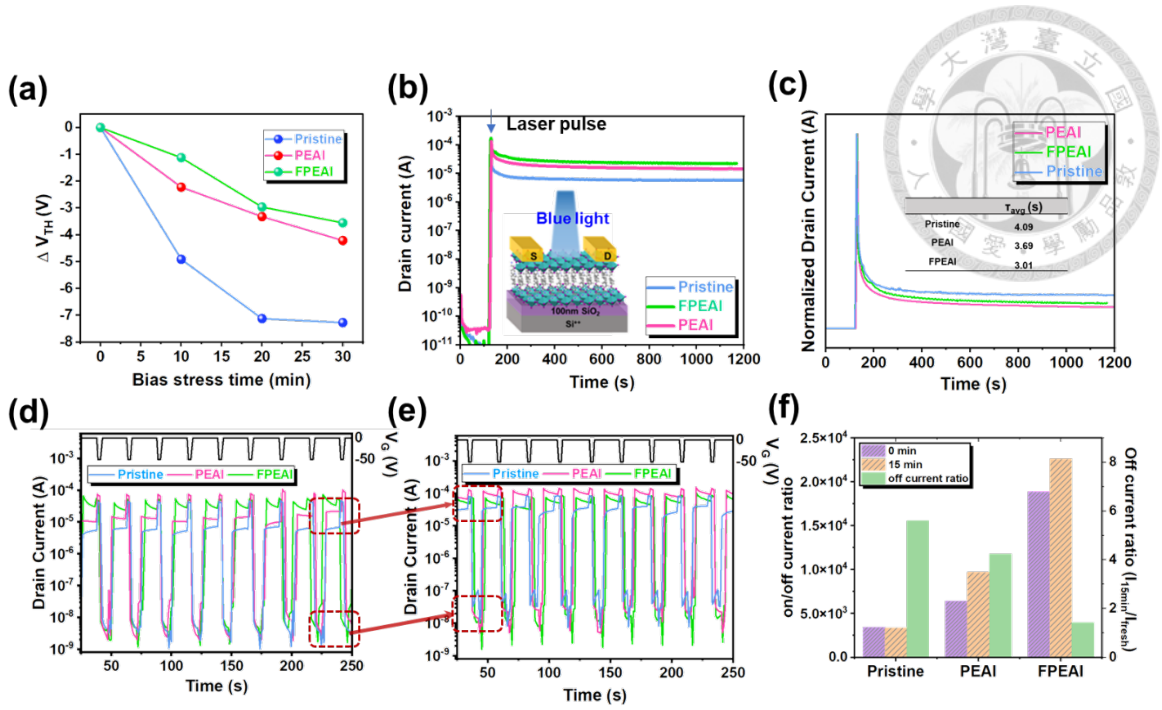

Figure 2.17 (a) V_{th} shift versus gate bias time of the studied devices at a fixed gate bias (V_g) of -50 V. (b) Chang in device drain current after irradiation with a 405 nm laser, measured under a V_g of 0 V. (c) Normalized drain current in (b) to compare the charge carrier lifetime. The insert shows the fitted data. WRER switching tests of (d) the fresh devices and (e) the devices exposed to ambient air for 15 minutes. (f) Bar charts of the on-off current ratios and off-current ratios between 15min and fresh for the studied devices.

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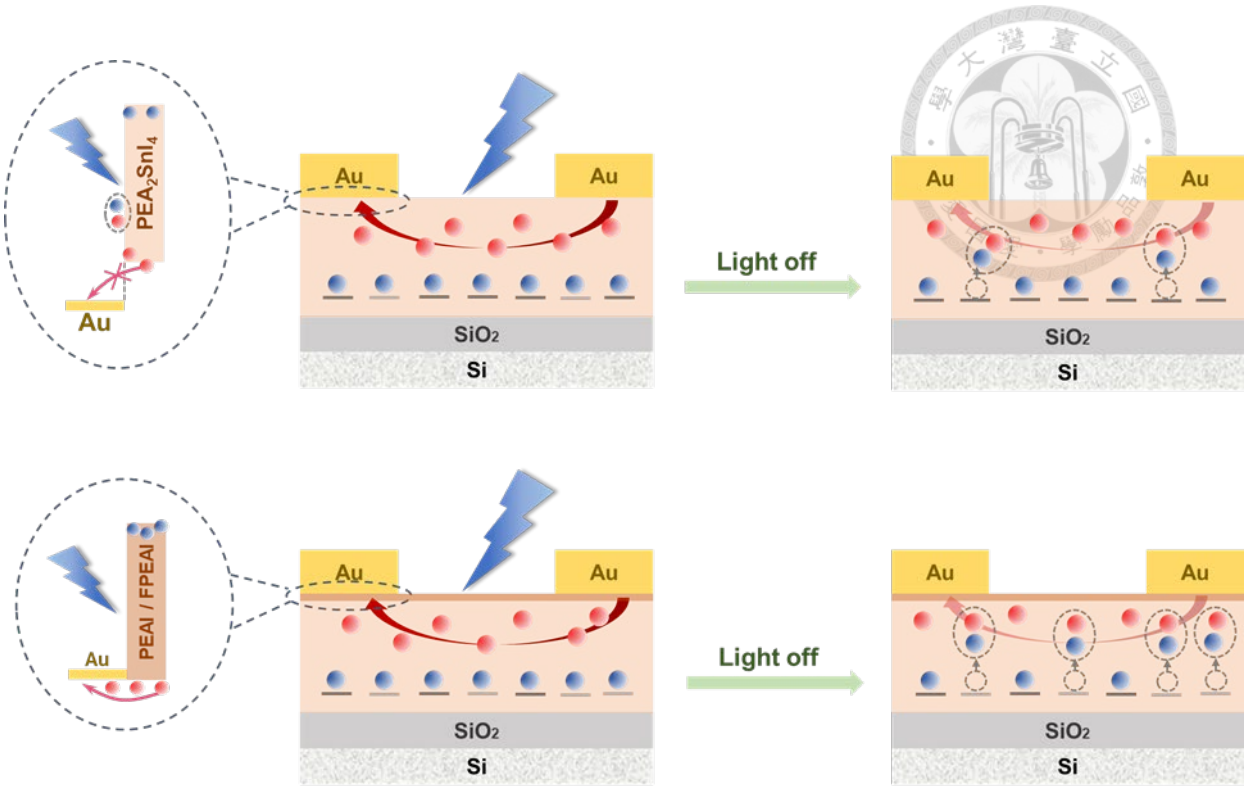

Figure 2.18 Illustration of the mechanism of electron-hole pair generation and recombination processes in the perovskite films with and without surface passivation.

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Tables

Table 2.1 Film Thickness before and after surface passivation.

Thickness (nm)	Region 1	Region 2	Region 3	Average
Pristine	70.1	92.6	88.7	83.8
PEAI	59.8	71.1	70.6	67.2
FPEAI	60.8	60.1	64.2	61.7

Table 2.2 TRPL lifetime fitting results for the studied three films.

TRPL	τ_1 (ns)	τ_2 (ns)
Pristine	0.25	1.06
PEAI	0.25	1.35
FPEAI	0.36	1.36

Table 2.3 Device performance of the fabricated FET devices.

	Maximum μ_h [$cm^2V^{-1}S^{-1}$]	Average μ_h [$cm^2V^{-1}S^{-1}$]	I_{on}/I_{off}	V_{th} [V]	Contact Angle (°)
Pristine	0.76	0.68 ± 0.07 (0.74)	(9.43 ± 1.9) x 10^3	-13.9 ± 4.1	15.1
PEAI	2.15	1.88 ± 0.14 (2.02)	(1.0 ± 0.1) x 10^4	-3.64 ± 22.7	26.1
FPEAI	2.96	2.70 ± 0.02 (1.88)	(2.69 ± 1.6) x 10^4	-27.5 ± 4.4	32.3
IPA/Tol	3.58 x 10^{-2}	3.48x10^{-2}	7.2x10^2	-3.35	

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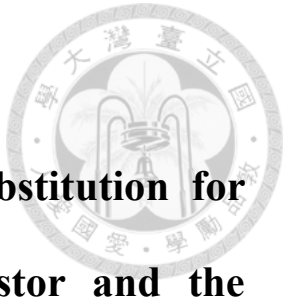

Chapter 3

Improving Performance by Cation Spacer Substitution for Two-Dimension Tin Halide Perovskite Transistor and the Properties Comparison Between TEA_2SnI_4 and PEA_2SnI_4

3.1 Introduction

Two dimensions lead-free metal halide perovskite like phenylethyl ammonium tin iodide (PEA_2SnI_4) has been an impressive candidate for transistors since its first application back to 1999.[29] Compared to their 3D counterpart, the 2D metal halide perovskite has the cation spacer which therefore exhibits some excellent properties such as higher exciton binding energy (E_b), less ion migration, and more stable environment stability. The 2D perovskite displays a self-assembled quantum well structure, where the inorganic layer functions as a quantum well, and the spacer cation layer acts as a quantum barrier. Moreover, the perovskite alignment is parallel to the substrate, which restrains the charge transport direction to one plane, significantly decreasing the probability of charge carriers trapped.

Speaking of the cation spacer, the organic cation can modulate the orbital overlap between metal and halide. Therefore, it can influence not only the metal-halide-metal

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bond angle and the metal-halide bond length. Additionally, there are some factors that cation spacer can affect the perovskite characteristics. First, it can affect the octahedral distortion and the metal-halide-metal crystal tilting depending on the hydrogen bonding force intensity between halide and ammonium group. Second, the exciton binding energy (E_b) can be tuned by the spacer dielectric constant. Higher dielectric constant means lower dielectric mismatch between organic and inorganic layer and therefore lower E_b.[6]

PEA_2SnI_4 has been widely studied for high mobility transistors device. However, there is still a bottleneck for its maximum mobility cannot breakthrough 5 $cm^2\ V^{-1}\ s^{-1}$ steadily. Therefore, there have been some studies attempting to substituting for other cation spacer. In 2023, Feng Teng and his group substitute PEA^+ to Dion–Jacobson spacer 1,4-butanediammonium (BDA^+) and produce $BDASnI_4$. Without the van der Waals gap to Ruddlesden–Popper (R–P) counterpart, the structural stability can improve and stronger interlayer electronic coupling between I-I through shorten interlayer distance. Therefore, the out-of-plane charge transport can be improved, which has long been criticized in 2D perovskite transistors.[27] In 2020, Zhan'ao Tan and his group succeeded in producing new 2D material 2-thiopheneethylammonium tin iodide perovskite (TEA_2SnI_4) by spin-coating method and applied it in PeLED. In their research, they studies the morphology, optical properties, energy structure, and trap densities. The champion device can reach luminance to 322 cdm^{-2} and external quantum efficiencies

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0.62%.[95] In 2022, Tomasz Marszalek and his coworkers further applied TEA_2SnI_4 to transistors device and reach 0.34 $cm^2\ V^{-1}\ s^{-1}$ by hot-casting method.[44] At the next year, the same group further modified the device by pentanoic acid addition and reached hole mobility to 0.7 $cm^2\ V^{-1}\ s^{-1}$.[45] These research demonstrates that cation spacer substitution has been a popular study objective to improve the PeFET device.

Herein, we attempt to repeat the 2D tin halide perovskite TEA_2SnI_4 and its transistor application. We have been achieving the transistor maximum hole mobility 2.48 $cm^2\ V^{-1}\ s^{-1}$. This mobility is the highest among all the TEA_2SnI_4 related papers and also higher than PEA_2SnI_4 in our experiment. The optical properties, morphology, and device performance were compared between PEA_2SnI_4 and TEA_2SnI_4.

3.2 Experiment Section

3.2.1 Materials

Materials. 2-thiophene-ethylammonium (TEAI) was bought from Greatcell Solar. Tin iodide (SnI_2, 99.99%)、Phenethylammonium iodide (PEAI, 98%), and solvent including dimethylformamide (DMF, 99.8%) and dimethyl sulfoxide (DMSO, ≥ 99.9%) were purchased form Sigma-Aldrich and used without further purification.

3.2.2 Precursor Solution Preparation and Device Fabrication

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The precursor solution of 2D PEA_2SnI_4 (with a concentration of 0.16 M) is prepared by dissolving PEAI and SnI_2 at a molar ratio 2:1 in DMF/DMSO with a volume ratio of 1:1. The solution was placed at room temperature for 30 min and then filtered by a 0.22 μm PTFE filter. The precursor solution of 2D TEA_2SnI_4 with concentration 0.10M is prepared by dissolving TEAI and SnI_2 at a molar ratio 2:1 in pure DMSO. A bottom-gate/top-contact transistor device was fabricated in this study for testing the transistor performance. The device was built on a highly n-doped Si substrate with a 100 nm SiO_2 gate dielectric layer (Ci = 29 nF cm^{-2}). The substrate was first cleaned with diluted detergent, deionized water, acetone, isopropanol, and toluene for 5 min in sequence, and then dried with a nitrogen gun and treated with plasma for 30 min. Afterward, the PEA_2SnI_4 film was spin-coated onto the substrate at 4000 rpm for 50 s. The TEA2SnI4 film was spined coated onto the substrate at 4000rpm for 60 s. They were annealed for 100ºC 10min after coating process. Finally, 50-nm contact gold electrodes were thermally deposited under a high vacuum (10^{-6} torr) through a shadow mask with defined channel length (L) and width (W) of 50 and 1000 μm, respectively. According to the saturation region of a transistor device, the field-effect mobility (μ) and the threshold voltage (V_{th}) can be determined using the following equation:

$$I_{ds} = \frac{W}{2L}\mu C_i(V_{gs} - V_{th})^2$$

where I_{ds} and V_{gs} were the source-to-drain currents and the source-gate voltage,

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respectively, and C_i was the capacitance of the 100 nm-SiO_2 gate dielectric layer (C_i = 29 nF cm^{-2}) that was measured per unit area.

3.2.3 Characteristic

SEM images were taken using Nova^{TM} NanoSEM 230 field-emission SEM. XRD patterns were measured using Rigaku SmartLab SE. The absorption spectra were measured using Hitachi U-4100 UV–visible spectrophotometer. PL was measured using Fluorolog-3 Spectrofluorometer. The values of work function (WF) and valence band maximum (VBM) were determined using ultraviolet photoemission spectroscopy (UPS) with He I (photon energy = 21.20 eV) as the excitation source. Energy gaps were calculated from the Tauc plots under the assumption of direct bandgap. The FET performance was characterized using a Keithley 4200-SCS semiconductor parameter analyzer (Tektronix) in an N_2-filled glove box at room temperature under dark conditions.

3.3 Result and Discussion

3.3.1 Morphology and Optical properties

The chemical structure of cation spacer TEA+ and PEA+ are shown in **Figure 3.1.** **Figure 3.2** shows SEM morphology between PEA_2SnI_4 and TEA_2SnI_4. Under the same magnification, PEA_2SnI_4 displays tattered crystal-like morphology. On the contrary,

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TEA_2SnI_4 demonstrates larger grain size and therefore fewer grain boundary, which is benefit to device performance because grain boundaries are usually seen as trap states. The UV absorption and PL emission spectra are shown in **Figure 3.3a-b**. For both the PEA_2SnI_4 and TEA_2SnI_4 films, there are three main absorption peaks in UV spectra. That is, 429nm for high-energy exciton transition energy level; the 525 nm absorption peaks can be assigned to intraband charge transfer between organic spacer and inorganic crystal layers, whereas the large absorption peak at 612nm is attributed to intrinsic band-edge exciton absorption peaks.[96] Form the PL spectra, the red shift can be observed between PEA_2SnI_4 (623 nm) and TEA_2SnI_4 (633nm), and this phenomenon comes from the bandgap difference. Comparing to PEA_2SnI_4 (1.98 eV), TEA_2SnI_4 (1.93 eV) has smaller band gap, and this is proved by the Tauc plot (**Figure 3.4a-b**) calculated from UV spectra. The crystal structure spectra is identified by XRD and the difference between two materials is shown in **Figure 3.4c**. To compare the main peak of (002), the two theta between 3 to 8 degree is magnified. The main peak position difference is attributed to the d-spacing difference. TEAI has shorter d-spacing between inorganic layer than PEAI cation spacer. The shorter d-spacing decreases the inorganic layer, which may increase orbital overlapped I-I atoms in adjacent inorganic layer.

3.3.2 Energy Level Difference and Device Performance

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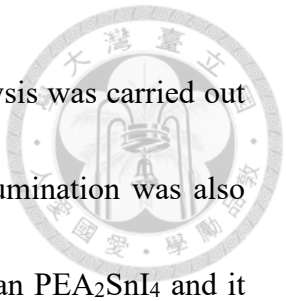

To identify the energy level difference for two films, UPS analysis was carried out for two films and the result was shown in **Figure 3.5a** and the illumination was also shown in **Figure 3.5b**. The work function for TEA_2SnI_4 is lower than PEA_2SnI_4 and it more close to the work function of gold electrode. This can potentially enhance the transistor performance for lower energy barrier.

To explore their application in transistors of two materials, we adopted 2D perovskite as active layer in transistor device. The transfer characteristic is shown in **Figure 3.6**. They show similar transfer characteristic curve and similar hysteresis, but the mobility for TEA_2SnI_4 is a little higher for better energy alignment with Au electrode. The related device performance is shown in **Table 3.1**.

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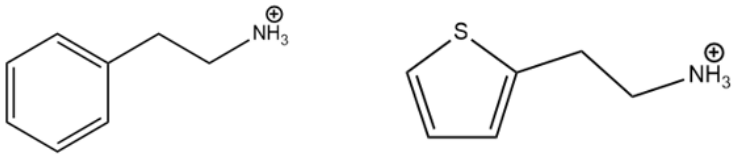
Figures



PEA$^+$ **TEA$^+$**

Figure 3.1 The chemical structure of cation spacer PEA^+ and TEA^+.

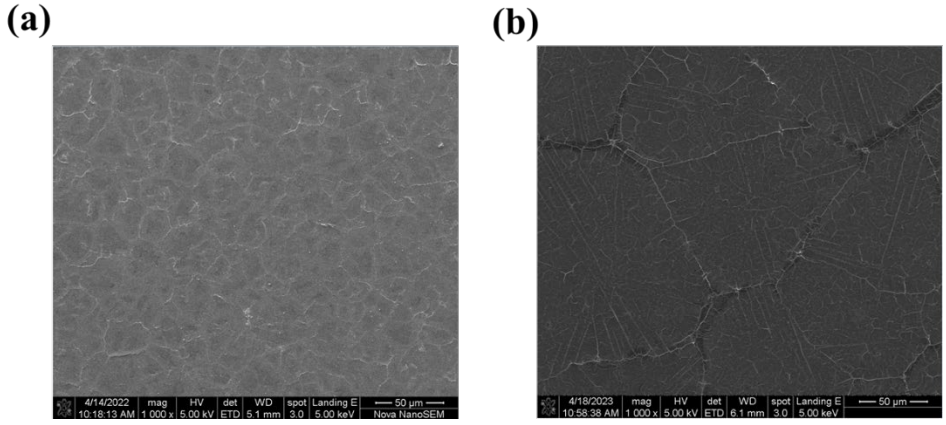


Figure 3.2 The SEM surface morphology of 2D tin perovskite (a) PEA_2SnI_4 and (b) TEA_2SnI_4.

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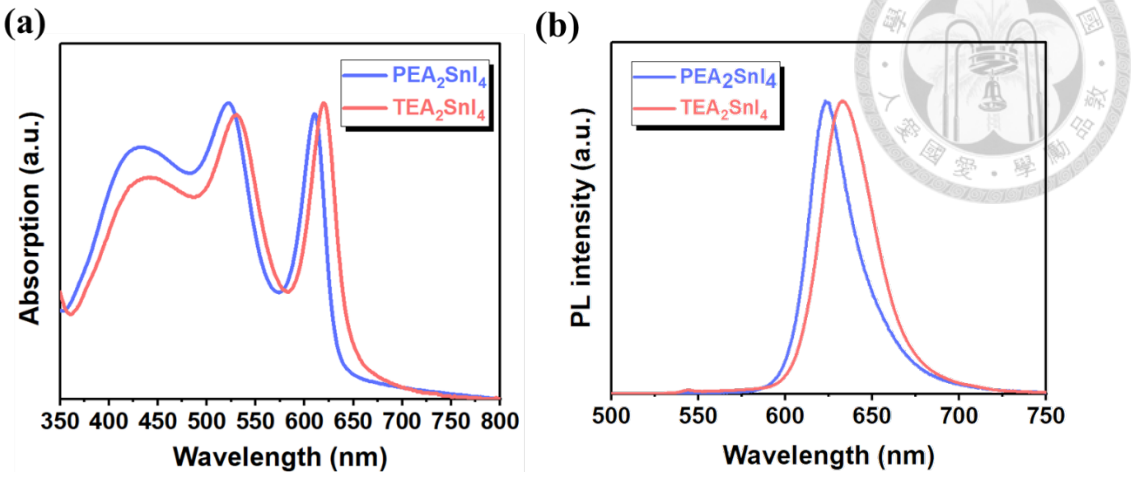

Figure 3.3 (a) The UV-vis absorption spectra and (b) PL emission spectra of two 2D tin perovskite materials.

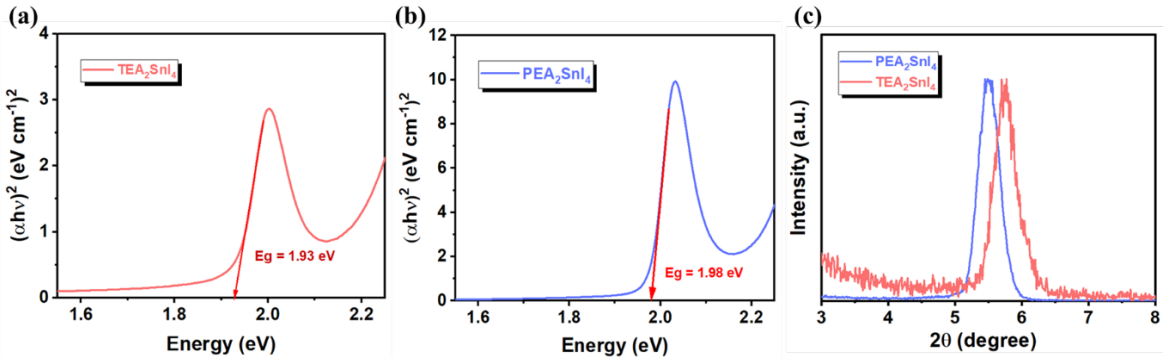

Figure 3.4 Tauc plot from UV-vis for (a) PEA_2SnI_4 and (b) TEA_2SnI_4. The XRD crystallinity data for 2D tin PEA_2SnI_4 and TEA_2SnI_4.

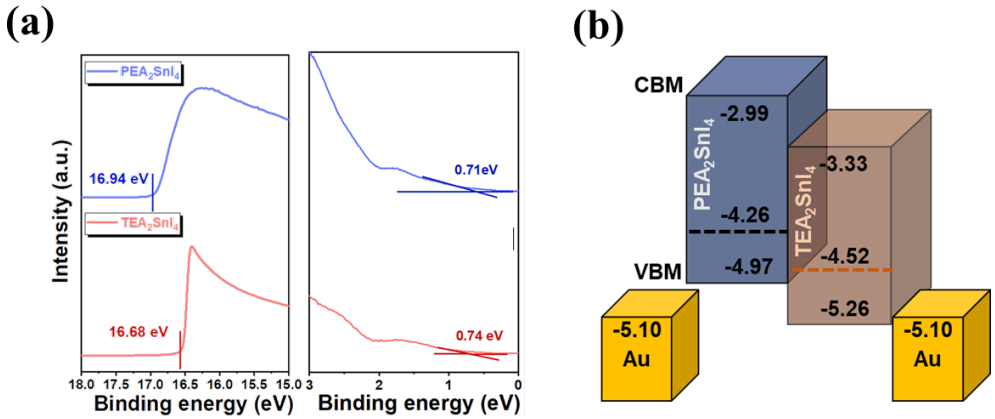

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Figure 3.5 (a) The UPS energy level for PEA_2SnI_4 and TEA_2SnI_4. (b) The illumination of energy level for PEA_2SnI_4 and TEA_2SnI_4

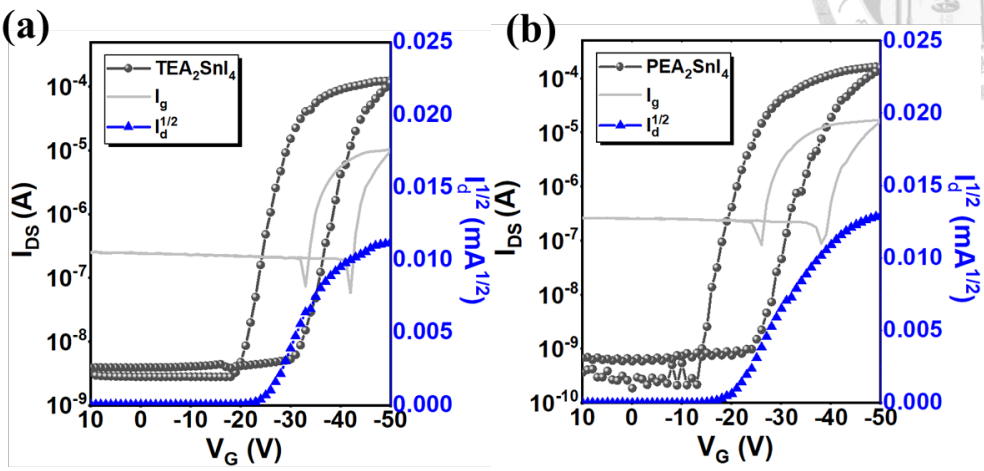

Figure 3.6 The transfer characteristic for PEA_2SnI_4 and TEA2SnI4 transistor device.

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Tables

Table 3.1 The transistor device performance data for TEA_2SnI_4 and PEA_2SnI_4

	Highest μ_h [$cm^2V^{-1}S^{-1}$]	Average μ_h [$cm^2V^{-1}S^{-1}$]	Ion/Ioff	Vth [V]
TEA_2SnI_4	**2.48**	**2.32**	**$4.5x10^4$**	**-25.2**
PEA_2SnI_4	**1.75**	**1.62**	**$9.0x10^5$**	**-20.4**

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Chapter 4

Conclusion and Future work

In conclusion, we succeeded in fabricating the high performance 2D tin halide perovskite PEA_2SnI_4 transistor. Tin perovskite has long been criticized for not only the oxidation problem but also the overfast crystal growth before nucleation. To resolve the easily oxidation problem, we have applied the surface passivation method to protect the perovskite active layer, which is proved to reduce the perovskite degradation rate. As for the overfast nucleation problem, we can adopt lots of strategies like additive engineering, dielectric/semiconductor surface engineering by other chemical materials. We can substitute the material of dielectric layer to high-k material to decrease the operation voltage for saving energy. If we want to further decrease ion movement to reduce hysteresis, we can change the length of cation spacer because longer cation spacer can increase the barrier for vertical ion transport. However, these ideas should be further researched and experiment to be realized.

In **Chapter 2**, we have shown that passivation of the surface of PEA_2SnI_4 films with PEAI/FPEAI can significantly improve the performance and stability of the associated perovskite transistors. This is achieved by reducing surface defects, increasing grain size through surface recrystallization, and p-doping the perovskite film as well. Electron-

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donating nitrogen atoms on PEA^+ and $FPEA^+$ act as Lewis bases to stabilize Sn^{2+} and reduce Sn vacancies, resulting in more stable films. In addition, these passivators are able to p-dope the PEA2SnI4 films, promoting better energy level alignment with the electrodes and achieving efficient charge transfer. Overall, this work highlights the importance of surface passivation in improving the performance and stability of perovskite transistors, which is important for the development of advanced optoelectronic devices. Devices passivated by PEAI and FPEAI showed a significant increase in maximum hole mobility (μ_h) with values of 2.15 and 2.96 $cm^2\ V^{-1}\ s^{-1}$, respectively, compared to control devices, which had μ_h of only 0.76 $cm^2\ V^{-1}\ s^{-1}$. These hydrophobic passivators also provided protection against ambient air-induced degradation of the PEA_2SnI_4 films, which was demonstrated by XPS, UV, PL, and XRD analyses. In addition, they improve the gate bias stability of the devices by reducing defects in the perovskite films. Finally, we demonstrate the nonvolatile optical memory behavior of perovskite-based transistors and use it for perovskite-based memories. In addition, surface passivation with PEAI/FPEAI not only reduces surface defects and improves the air stability of perovskite films, but also improves the photoresponse of the devices.

In **Chapter 3**, we replaced the original PEA^+ spacer with TEA^+. We investigate the surface morphology, optical properties, and energy level differences of the two two-dimensional tin perovskites. At the end of this chapter, we applied both perovskites to

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transistor devices and found that TEA_2SnI_4 has a higher mobility, which may be due to its better energy level alignment with the gold electrodes, or it may be that the dielectric constant of TEA^+ is larger. In conclusion, we can further modify TEA_2SnI_4 with these additives or passivation methods based on the fundamental data.

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