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碩士論文

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Master Thesis

一個僅 200nA 靜態電流且使用十二奈米鰭式電晶體的被動漣波導通關斷控制降壓型轉換器

A 200 nA Quiescent Current Buck Converter with Passive Ramp On-Off-Time Control in 12 nm FinFET

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中文摘要

這篇論文介紹了一種純 NMOS 電晶體功率級(power stage)、被動式斜率補償(Passive ramp)、導通-關斷時間控制(on-off-time control)且靜態電流(quiescent current)僅有 200 nA 的降壓轉換器(buck converter)。在設計中，還有一種被稱為深度睡眠(deep sleep mode)的模式，可以在必要時將除了少數主要比較器與少數偏壓電路之外的整個控制電路群關閉。使用被動式斜率補償也規避了相較於傳統上較為耗電的斜率產生器。這些功能最佳化了此電路的靜態電流，甚至在極低負載中(ultra-light load)有一半以上的功率損耗是來自於製程上無法避免的漏電。在小訊號分析中，由輸出電感與輸出電容產生的複數極點(LC complex pole)會被被動式斜率補償中的前饋(feed forward)機制解耦(decouple)。我們也設計了一個較低頻寬的迴路，用來做直流偏壓消去(DC offset cancellation)。它能夠在不影響暫態響應的同時，決定的整個電路的頻寬與穩定度。這種雙迴路(dual loop)能夠同時保證輸出電壓的穩定與快速的暫態響應。為了達成 200 nA 靜態電流的目標，我們設計了一個帶隙參考電壓(bandgap reference)，它會在深度睡眠模式時切換到低漏電採樣模式(low leakage sample and hold)，使其可以僅在極短時間內運作，常時保持關閉，使其平均功耗降到極低。在負載暫態響應方面，我們提出了一種創新的導通-關斷時間控制(on-off-time control)的控制法，可以在導通時間控制(on-time control)與關斷時間控制(off-time control)自動且順暢的切換，使得導通時間與關閉時間皆能隨著負載變化而自由延展。

所提之晶片原型採用台積電 12nm CMOS 製程，並且在包含了功率級與引腳的同時僅僅占用 0.36 mm^2 的面積。純 NMOS 電晶體功率級與共封裝的去彈跳電路(debouncing circuit)與靴帶式電路(bootstrap circuit)表現出僅有 35 mOhm 的導通電阻(R_{dson})。在模擬中顯示，切換頻率最高為 4.8 MHz、僅有 200 nA 的靜態電流且在負載從 10 μA 到 2 A 皆有大於 90%的效率。而在 1 μA 與 500mA 的負載瞬態響應中，所提出的導通-關斷時間控制達成 23 mV/ 17 mV 的過衝/下衝，與 800-

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ns 的安定時間。這個降壓轉換器架構最初由蔡杰儒學長提出並由我進行電路設計與實現。

關鍵詞—直流-直流轉換器，降壓轉換器，導通-關斷時間控制，被動式斜率補償，純 NMOS 電晶體功率級，低靜態電流，直流偏壓消去

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Abstract

This thesis presents a 200nA quiescent current, pure NMOS power stage, passive ramp (PSR) on-off-time controlled buck converter for a modern mobile silicon-on-chip (SoC) for a longer battery life. In the design, there's a mode called deep sleep mode (DSM) that only the main comparator is alive in the whole circuit. Passive ramp modulation also plays an important role to prevent the conventional power-hungry ramp generator. These functions extremely improve the quiescent current to a new level. Eventually more than half of the power consume is leakage current. In a small signal analysis scheme, the LC complex poles are decoupled by the feedforward component benefit from PSR modulation. I also design an extra loop with relatively low bandwidth for DC correction. It also defines the bandwidth of the whole loop but not affecting the modulator gain. This dual loop scheme ensures the stable output voltage DC level and the fast transient speed, simultaneously. To achieve 200nA quiescent current, I also design a bandgap reference that can be totally shut down with a low leakage sample and hold technique. For load transient response, an innovative on-off-time control scheme is proposed. The modulation of this control switched between on-time and off-time control, smoothly and automatically.

The proposed chip prototype is fabricated in TSMC 12nm CMOS process and only occupies 0.36mm^2 with the power stage and pads. An N-FinFET power stage with co-package designed debounce circuitry and bootstrap circuit performs a 35 mOhm R_{dson} with all trace resistance. It shows a 4.8MHz switching frequency, 200nA quiescent current, and a loading range from 10μA to 2A with > 90% efficiency in simulation. The proposed passive ramp constant-on-off time controller achieves a 23 mV/ 17 mV undershoot/overshoot voltage with 800 ns settling time with a 1 μA to 500 mA loading step. The architecture of the buck converter was initially proposed by Senior Scholar

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Chieh-Ju Tsai and subsequently, I undertook the circuit design and implementation.

Keywords—DC-DC Converter, buck converter, on-off-time control, passive ramp, N-FinFET power stage, low I_q, DC cancellation loop

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Chapter 1 Introduction

1.1 Background

Nowadays, modern mobile phones are frequently equipped with high refresh rate displays and always-on-display features, necessitating DC-DC buck converters to have a high level of efficiency across a wide range of load conditions, including ultra-light loads. Additionally, the increasing number of computing cores in mobile devices creates more stringent load transient requirements for buck converters. As a result, there is a demand for a buck converter that can achieve fast dynamic response and high efficiency concurrently across a wide range of loads.

1.2 Prior works

Fig. 1.1 shows prior art buck converters that operate over a range of a few microamperes to one ampere [1-4]. [1] and [2] use an on-off-time control scheme with a calculated off-time period to eliminate the need for a zero current detection circuit and achieve >80% efficiency for ultra-light loads from 10 microamperes to about 10 milliamperes. However, these converters only operate in discontinuous conduction mode (DCM), leading to poor transient response and a narrow range of loads that are not suitable for modern mobile systems. [3] uses a hysteretic control scheme with excellent load transient response from light (~milliampere) to heavy (ampere) loads, but the power-hungry control loop circuitry results in a large quiescent current, limiting the converter's ability to operate at ultra-light loads with high efficiency. [4] tries to combine all these techniques by manually switching modes to achieve efficiency from 10 μA to about 100 mA. However, this approach requires an external mode selection signal to determine the operating mode of the converter, resulting in a non-smooth mode

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transition. The complex circuitry also leads to poor efficiency due to large leakage and quiescent current.

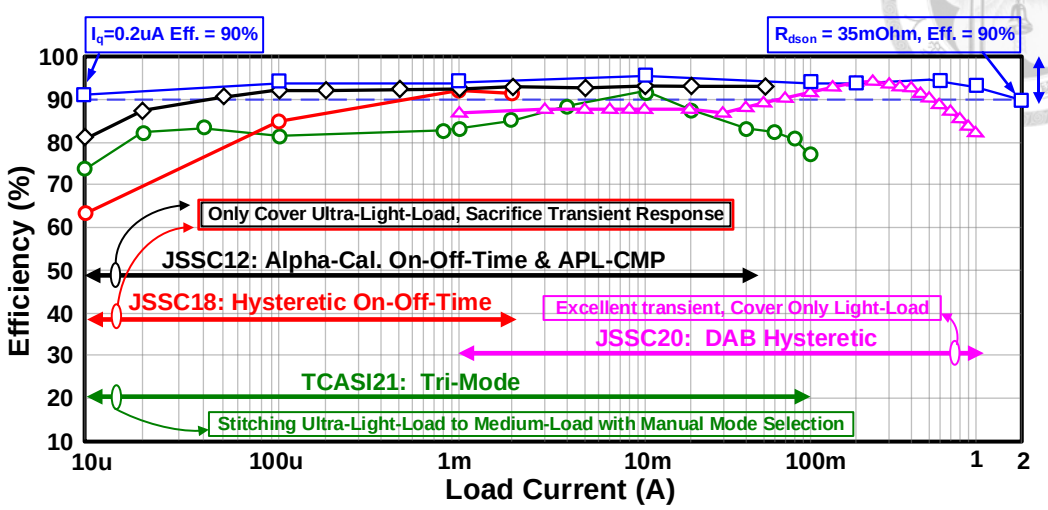

Fig. 1.1 Efficiency survey of priors and the design target of this work [1 - 4].

1.3 Chip Design goal

The design target of this chip is to achieve >90% efficiency over a range of 10 μA to 2 A. For ultra-light loads (10 μA to a few mA), theoretical analysis shows that converters with a quiescent current <200 nA can meet the 90% efficiency requirement. The team proposes a passive-ramp on-off-time control scheme in that only the main comparator is alive when operating in DCM to optimize the quiescent current. The bias circuitry (such as the bandgap reference) is also halted using a low leakage sampling mechanism. For heavy load conditions (1 A to 2 A), an all N-FinFET switch with a co-package designed debouncing circuit and the bootstrap circuit has a 35 mOhm on-resistance to achieve 90% efficiency in the buck converter. Additionally, the controller extends the on-time during large load step events to minimize undershoot/overshoot of the output voltage. The comparator also adjusts its biasing current based on the operating condition to shorten the reaction time from DCM to continuous conduction mode (CCM).

In conclusion, the proposed buck converter demonstrates exceptional performance

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with a high-efficiency rate exceeding 90% and a minimal quiescent current of 200nA over a current range of 10 μA to 2 A. It also showcases low levels of undershoot and overshoot at 23 mV and 17 mV respectively and has a fast settling time of 800ns in response to loading changes from 1 μA to 500 mA. The N-FinFET power stage, which is integrated with a co-packaged debounce circuitry and bootstrap circuit, provides low resistance with 35 mOhm Rdson. The architecture of the buck converter was initially proposed by Senior Scholar Chieh-Ju Tsai and subsequently, I undertook the circuit design and implementation.

1.4 Analog Characteristics of 12nm FinFET Process

There are several notable advantages of utilizing the 12nm FinFET process in the design of a buck converter. The devices' characteristics, such as unity gain frequency, Rdson, and mismatches, exhibit significant improvements when compared to the standard 0.18 um process. These enhancements enable the design of circuits with broader bandwidths, and reduces area requirements, and facilitate the design of analog circuits during the pre-simulation stage.

However, it is important to consider that the parasitic resistances and capacitances of the routing traces in the 12nm FinFET process are substantially larger compared to the 0.18 um process. This poses challenges during the layout phase. In fact, I had to redesign several circuits due to the negative impact of routing-induced degenerations in order to meet the design objectives.

In conclusion, the overall characteristics of devices in the 12nm FinFET process are excellent, but the parasitic effects of the routing traces are significant. I recommend estimating the parasitic resistances and capacitances in advance during the pre-simulation phase to avoid repeated modifications to the transistor sizes of circuits.

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1.5 Thesis Outline

Chapter 2 will showcase a comprehensive overview of the functional diagram of the proposed buck converter. The proposal integrates several innovative features, and their cooperative operations will be elucidated. Furthermore, I will conduct a detailed analysis of the advantages and disadvantages associated with these innovations.

Chapter 3 will provide a comprehensive account of the key subcircuits of the buck converter, encompassing detailed explanations of their timing or function diagrams and transistor-level designs. Additionally, I will substantiate the benefits of the subcircuits through simulation.

Chapter 4 will demonstrate the overall advantages of the buck converter by presenting simulation results and measurement data and analyzing the performance discrepancies between these two approaches.

Chapter 5 illustrates the conclusion and future works.

Chapter 2 Proposed converter and Control Scheme

2.1 Full Architecture

Fig. 2.1 depicts the overall architecture of the proposed passive ramp on-off-time control buck converter. It is fabricated in TSMC 12nm CMOS process. The overall die area is 0.36 mm2 with ESD pads. This control mechanism is inspired by the conventional ripple-based on-time control [11-14] and incorporates four innovations: passive ramp, DC cancellation loop, on-off-time control, and all N-FinFET power stage co-design with the package. Additionally, Figure 2.2 displays the co-package design of the debouncing circuitry, along with the corresponding layout photo.

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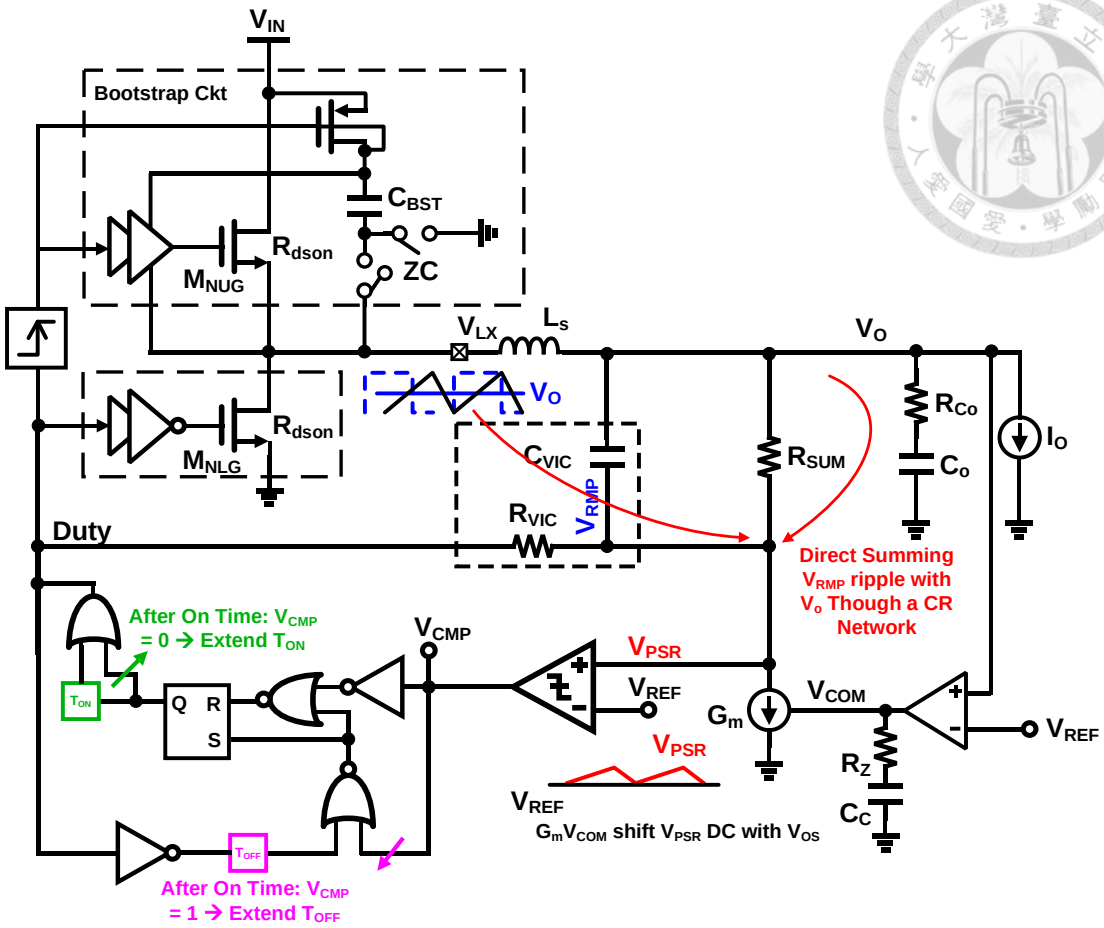

Fig. 2.1 The overall architecture of proposed passive-ramp on-off-time controlled buck converter

To begin with, the modulation ramp of the proposed converter is based on a passive network comprised of R_{VIC}, C_{VIC}, and R_{SUM}. The passive ramp V_{PSR} is contributed by the duty cycle in-phase component DV_{IN} summed with the output voltage V_O component to prevent sub-harmonic oscillation during CCM. As entering DCM [18], the VPSR signal is equal to the output voltage. If there is any V_O perturbation, the ramp signal will react to the diversification of V_O immediately.

Secondly, an additional DC cancellation loop is incorporated to mitigate the offset error during CCM, and it is made by two error amplifiers, R_Z and C_C. The loop comprises two error amplifiers, RZ and CC, which use negative feedback to adjust the DC value of the VPSR signal. This loop does not affect the controller's load transient

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response. Thus, a narrow loop bandwidth DC servo loop with offset cancellation is designed. In addition, the whole servo loop can be shut down during DCM to save power.

Thirdly, the proposed on-off-time control scheme automatically switches between on-time control and off-time control based on the duty cycle. The conventional on-time control [7] is less stable and has poor noise immunity when operating at a high duty cycle due to the vanished value of the modulation ramp. Another benefit is that it allows the converter to extend its duty cycle when a large load step event occurs by entering off-time control. This mechanism also prevents the common instability issue observed in traditional on-time control by transitioning to off-time control during high duty cycle conditions. Additionally, the on-off-time control scheme is capable of sleeping all circuitry excluding the main comparator and reference circuit. A bandgap reference leverages the low leakage sample-and-hold technique to reduce the sleep state circuit to only a main comparator.

Finally, a customized all N-FinFET power stage including the power FET, driving circuitry, and co-package designed bootstrap and debouncing circuit are adopted with a 35mOhm R_{dson} to guarantee efficient power delivery while heavying loading. Furthermore, the N-FinFET scheme performs a low leakage behavior than the traditional P-N FETs scheme. In summary, the four innovations ensure efficient and robust performance across ultra-light to heavy loads and load transients, respectively.

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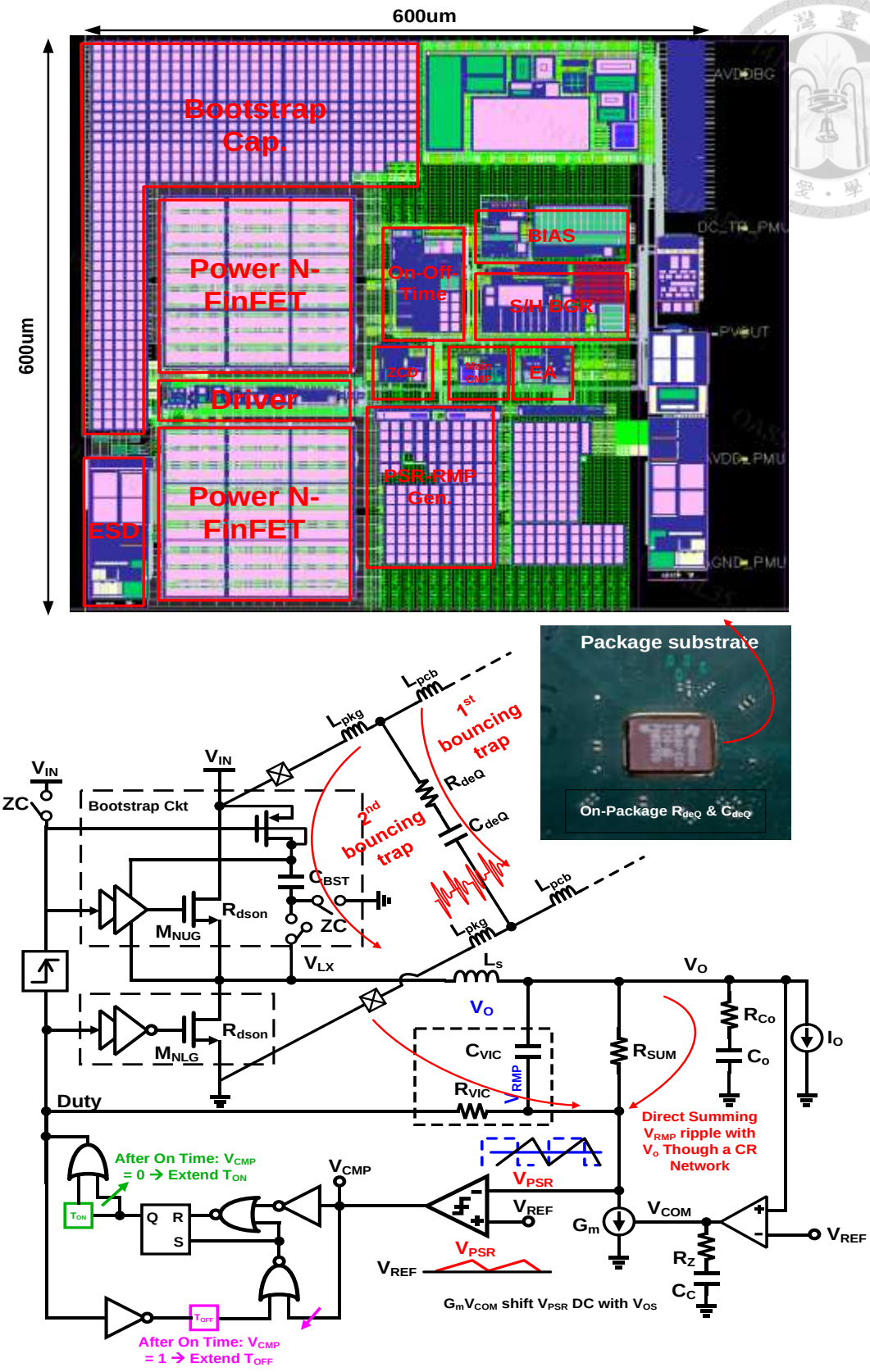

Fig. 2.2 The co-package design of the debouncing circuitry, along with the corresponding layout photo.

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2.2 ALL N-FINFET Power stage Co-Design with Package

Fig. 2.3 depicts the characteristics of leakage and R_{dson} in the 12nm FinFET devices. The N-FET's R_{dson} is 1.5 times lower than that of PFET and utilizing N-FET on the upper switch minimizes conduction loss and improves efficiency in the heavy load scenario. Furthermore, the leakage of N-FET is 1000 times lower than that of P-FET, which significantly enhances the efficiency in ultra-light load conditions. This is a crucial advantage and the primary reason for us to adopt the all N-FinFET power stage.

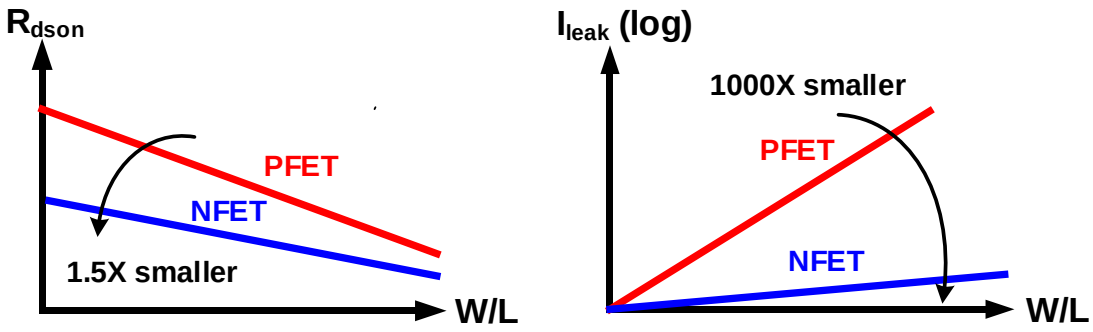

Fig. 2.3 R_{dson} and I_{leak} between P-FET and N-FET

The FinFET device is relatively vulnerable and sensitive to bouncing schemes, and even a rapid voltage jump could result in substantial long-term degradation. To prevent any significant cross-voltage, especially in heavy load scenarios, I have incorporated a debouncing RC network into the substrate of the package. Additionally, the bootstrap circuitry can reduce voltage bouncing even further. Fig. 2.4 shows the full picture of the debouncing loops and components. Out of these components, resistor R_{DEQ} and capacitor C_{DEQ} are situated on the package's substrate for the off-chip 1st bouncing trap, while resistor R_{BST} and capacitor C_{BST} are implemented on the chip itself for the 2nd bouncing trap.

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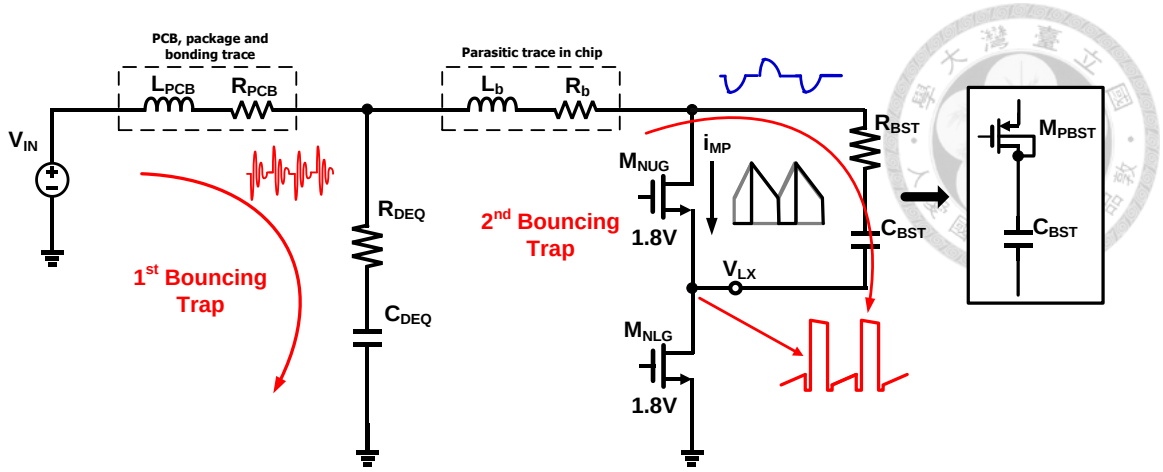

Fig. 2.4 The debouncing components and loops to protect the sensitive FinFET device

The effect of the debouncing components on the substrate is proven by simulation in Fig. 2.5 and Fig. 2.6. Fig 2.5 shows that the highest cross-voltage on the upper gate is up to 4.3V without 1st bouncing trap. Fig 2.6 shows that the highest cross-voltage on the upper gate decreases to 3V with 1st bouncing trap.

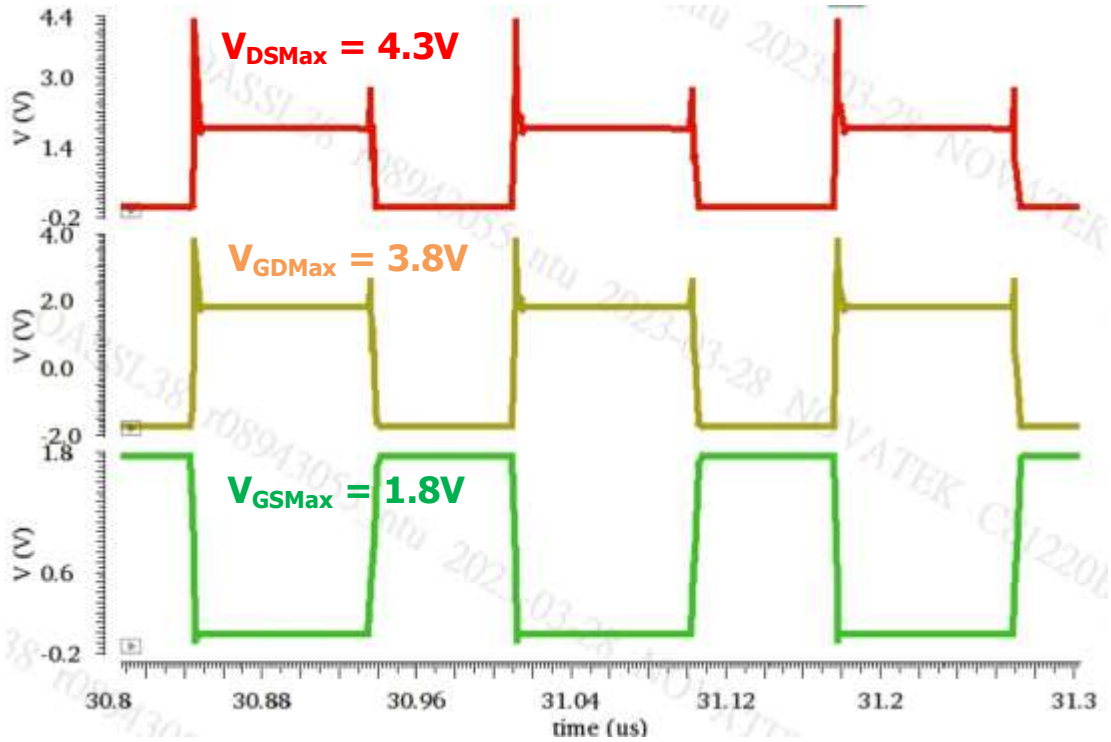

Fig. 2.5 The bouncing scheme without the 1st bouncing trap

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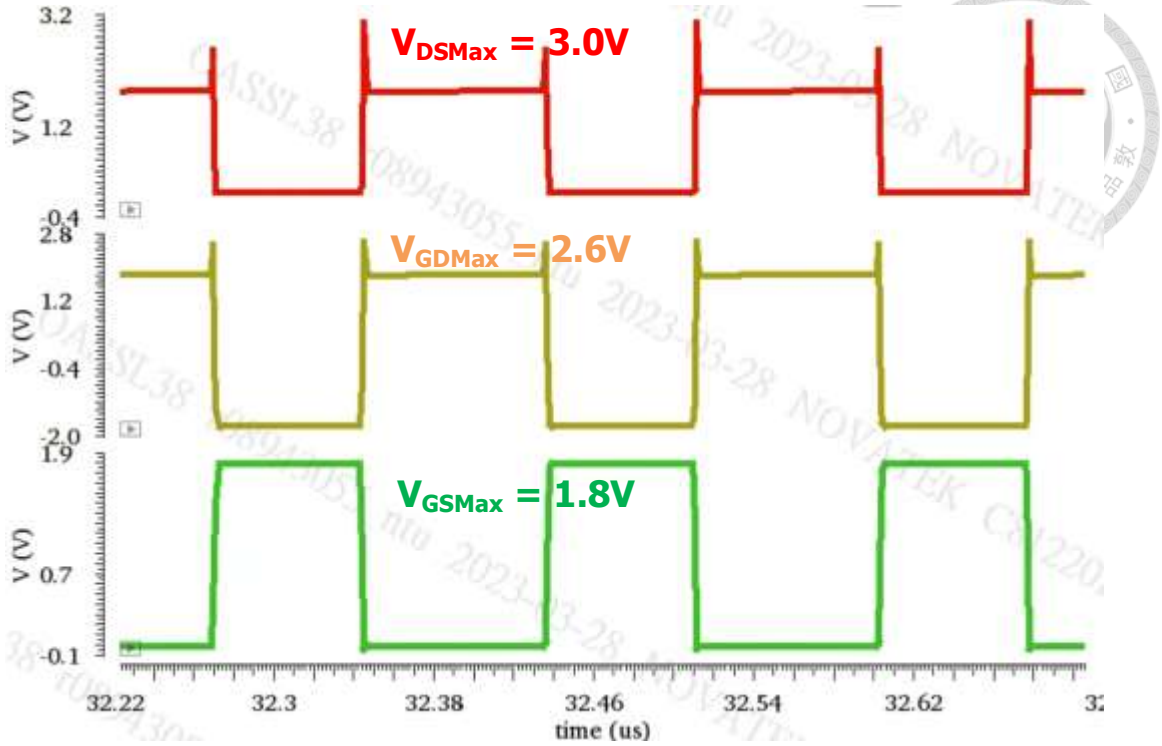

Fig. 2.6 The bouncing scheme with the 1st bouncing trap

2.3 Control loop

This section depicts the overall block diagram of the passive ramp on-off-time control loop. The ramp voltage (V_{PSR}) and reference voltage (V_{REF}) are directly connected to the main comparator for modulation. Three components, namely, V_{PSR} signal, output voltage (V_O), duty times V_{IN} (DV_{IN}), and G_mV_{COM}, form the signal. As previously stated, the duty cycle in-phase component DV_{IN} is utilized to avoid sub-harmonic oscillation during CCM, and the output voltage component V_O enhances the transient speed [15, 16, 20]. The third component, G_mV_{COM}, is generated by the DC cancellation loop [17], which shifts the DC voltage of V_{PSR} to fix the output voltage V_O at a specific voltage level V_{REF}. Fig. 2.7 shows the detailed interactions and connections of the passive ramp, DC cancellation loop, and the on-off-time control scheme.

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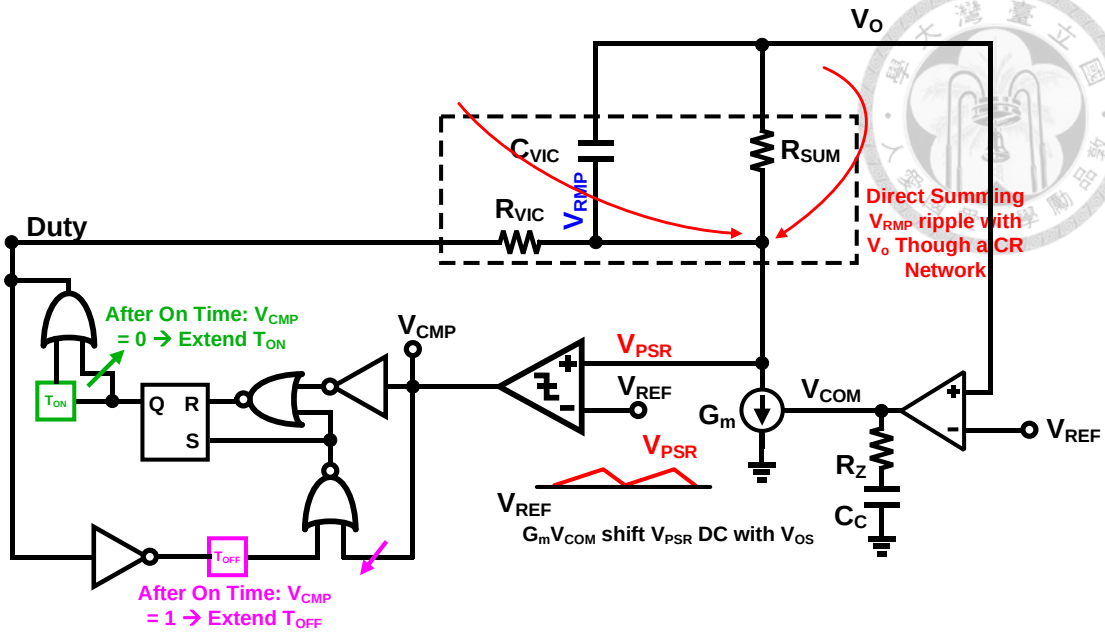

Fig. 2.7 Detailed interactions and connections of the passive ramp, DC cancellation loop and the on-off-time control scheme.

Fig 2.8 shows the block diagram of the on-off-time control scheme. It is composed of a comparator, 2 pulse generators, and some logic gates. A comparator is responsible for comparing two input signals and producing the output signal V_{CMP}. The pulse generator produces on-time and off-time pulses for the Duty signal to activate the duty cycle. There is also something special to make the on-off-time control work. Typically, the conventional architecture of the on-time control incorporates the off-time generator with the on-time control loop, utilizing the off-time generator as insurance against false triggering during the boundary of duty on and duty off. However, on-time control has its limitations, particularly in high-duty-cycle situations, where it can easily become unstable. Therefore, I have designed a new architecture that can operate in both on-time control and off-time control, in both static states and transient states. The solution involves creating an additional loop for off-time control. I bring the off-time generator out of the on-time control loop and feed the signal DUTY as its input. The off-time

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generator is triggered by DUTY and outputs the signal TOFF to the PSRCOOT LOGIC, forming a complete extra loop for the off-time control. Because the stability of the off-time control improves as the duty cycle increase. This solution significantly optimizes stabilization in high-duty-cycle situations and allows the duty cycle to be fully open, with nearly 100% duty. Furthermore, for transient states, the design reserves both extended on-time control and extended off-time control, as the loading current increases and decreases, respectively.

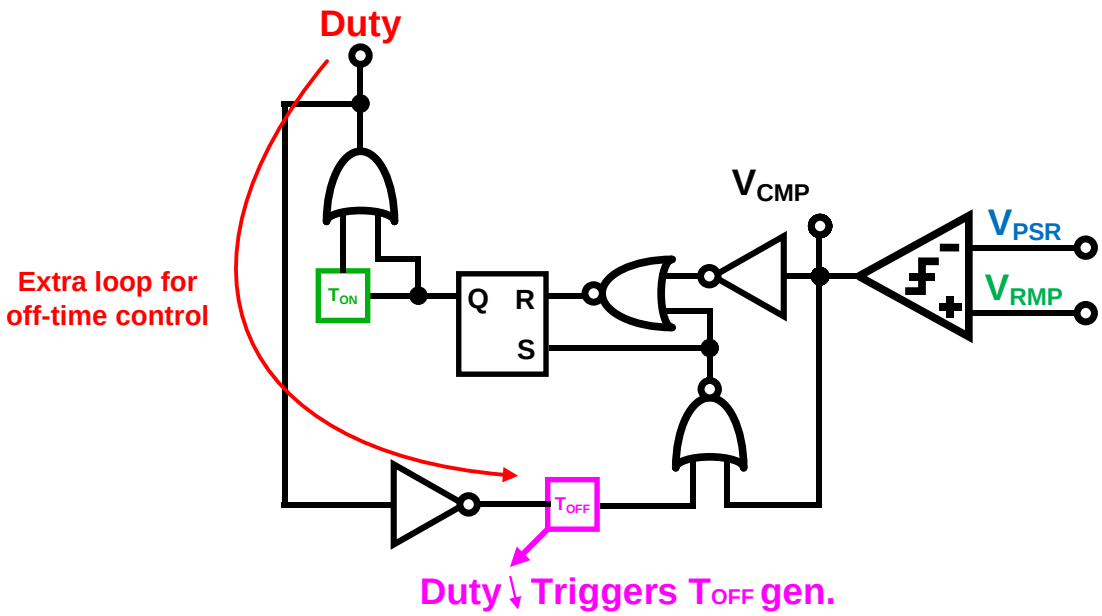

Fig. 2.8 The block diagram of the on-off-time control scheme.

A completed timing diagram of the on-off-time control scheme is shown in Fig. 2.9. There are two static states, which are on-time control and off-time control, in the on-off-time control modulation. The modulator automatically operates in on-time or off-time mode itself by the modulation signal. The Duty cycle on duration is equal to T_{ON} with a logic OR gate operation of the time duration of $V_{PSR} < V_{REF}$ as the equation in Fig. 4. On the other hand, the Duty cycle off duration is equal to T_{OFF} with a logic OR gate operation of the time duration of $V_{PSR} > V_{REF}$. With a low-duty cycle operation, the voltage level of V_{PSR} is higher than V_{REF} most of the time, and the converter is

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operated in on-time control mode. When the valley of V_{PSR} intersects with V_{REF}, the main comparator output transits to low voltage and triggers the on-off-time generator. Thus, a minimum on-time T_{ON} is produced. At the end of T_{ON}, a minimum off-time T_{OFF} is introduced as shown at the button left of Fig. 4. Since the V_{PSR} signal is still larger than V_{REF}, the off-time duration will extend. In contrast to the on-time control, when the converter operates with a high-duty cycle, it is the off-time control. All the operation is similar to on-time control with little difference. Now the modulation waveform is based on the peak of V_{PSR} intersecting with V_{REF}, and the on-time will extend.

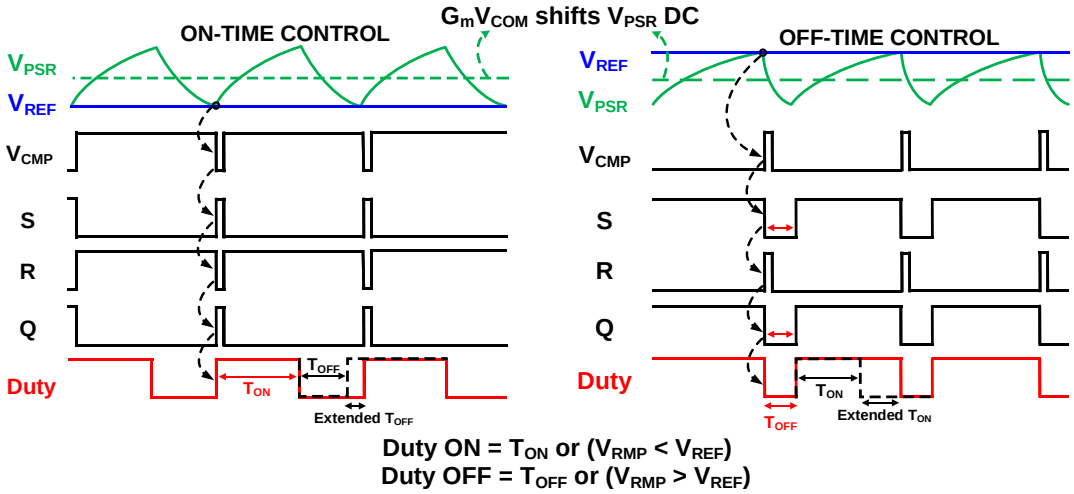

Fig. 2.9 A completed timing diagram of the on-off-time control scheme

Fig. 2.10 and Fig 2.11 show the load transient simulated results that explain all the benefits of this control scheme. In Fig. 2.10, at first, loading with an ultra-light load condition (1 μA), the control performs the DCM function that shut down everything and only the comparator is alive with a tiny bias current. The reference voltage is sampled with a low-leakage sample and hold circuit. This extremely reduces the quiescent current to only 200 nA. The converter is operated at on-time control because $V_{RMP} > V_{REF}$. As the loading current I_{LAOD} increase, V_{PSR} goes down immediately. It makes the V_{PSR} lower than V_{REF} and forces it to enter the off-time control that automatically extends the T_{ON} length. When V_{PSR} approaches V_{REF}, it settles for a while

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and switches back to on-time control. In the end, the modulation back to $V_{PSR} > V_{REF}$, and the converter stabilizes in the on-time control mode. The voltage drop during load transient is 23 mV with about 800 ns settling time. In Fig. 2.11 the loading decrease from 500 mA to 1 μA. The converter mode remains unchanged with on-time control and reduces its switching frequency. Other operations within DCM are similar to that in Fig. 5. (a), and the only difference is that T_{OFF} is extended instead of T_{ON}. The overshoot during load transient is 17 mV with about 200 ns settling time.

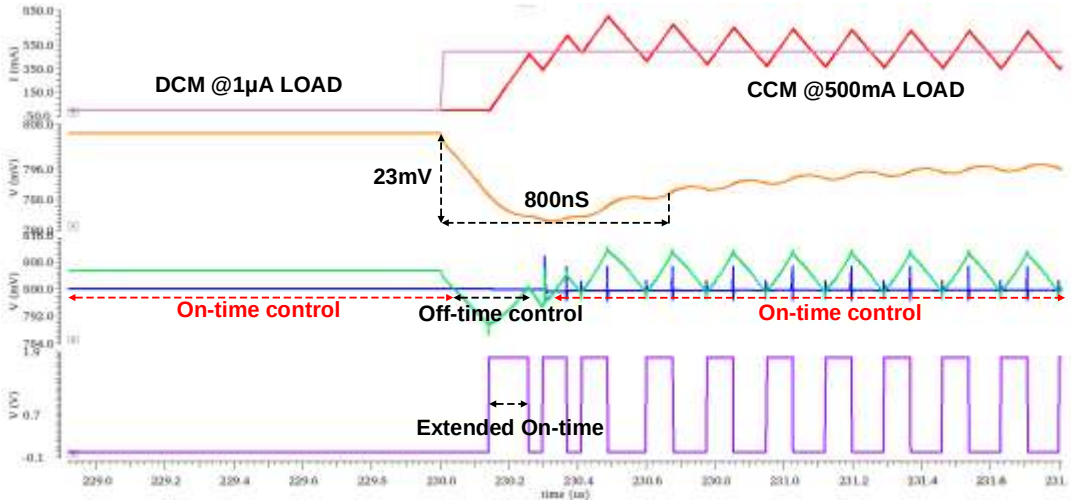

Fig. 2.10 Load transient, I_{Load} from 1 μA to 500 mA.

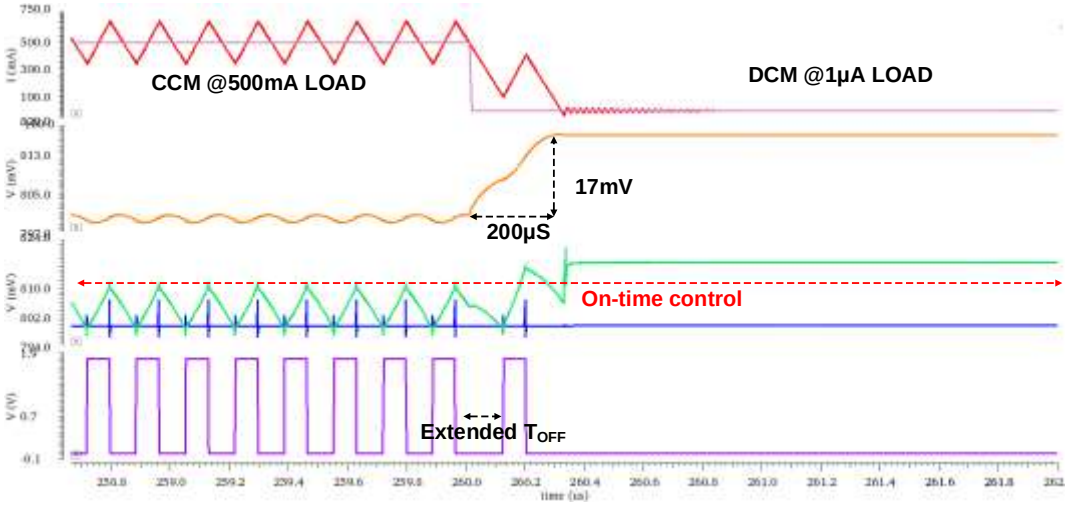

Fig. 2.11 Load transient, I_{Load} from 500 mA to 1 μA.

In conclusion, the proposed passive ramp on-off-time control achieves fast transient speed from DCM to CCM, due to the smooth transition between on-time

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control mode and off-time control mode. Furthermore, the DCM function that only the comparator is alive dramatically improves the efficiency during the ultra-light load.

2.4 Stability analyzation for Control loop

In the proposed control loop, I have combined two distinct loops, namely the passive component loop and the DC cancellation loop, to generate the passive ramp signal, V_{PSR}. I recognize that a voltage mode control buck converter lacking any compensation is an unstable system with 2 LC complex poles. A simplified transfer function for this system is depicted in Figure 2.12.

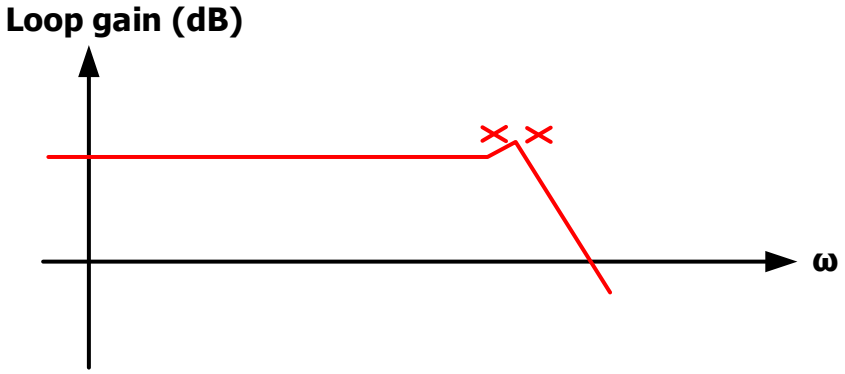

Fig. 2.12 A simplify transfer function for a closed loop buck converter without any compensation.

Consequently, I have designed the passive component loop to generate a passive ramp signal, which comprises the duty cycle in-phase component DV_{IN} added to the output voltage V_O component. This passive ramp technique effectively decouples the LC complex poles, leading to system stability. Figure 2.13 illustrates a simplified transfer function for a ripple-based control closed-loop buck converter incorporating the passive component compensation loop.

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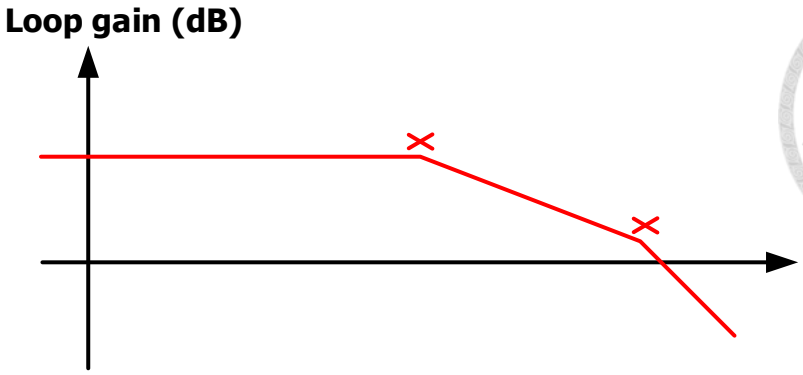

Fig. 2.13 A simplify transfer function of a ripple-based control closed loop buck converter with the passive component compensation loop.

Nonetheless, a passive component compensation loop alone is insufficient to guarantee precise DC output voltage. Therefore, I have designed an additional DC cancellation loop to ensure accuracy. To achieve this, I have controlled the transconductance (G_m) of the error amplifier and the value of the capacitor C_C in Fig. 2.6 to create an extremely low bandwidth, thereby ensuring that the loop gain of the system is a single pole system within the bandwidth. These two loops have been combined to form the control loop. Fig. 2.14 illustrates a simplified transfer function for the proposed control loop.

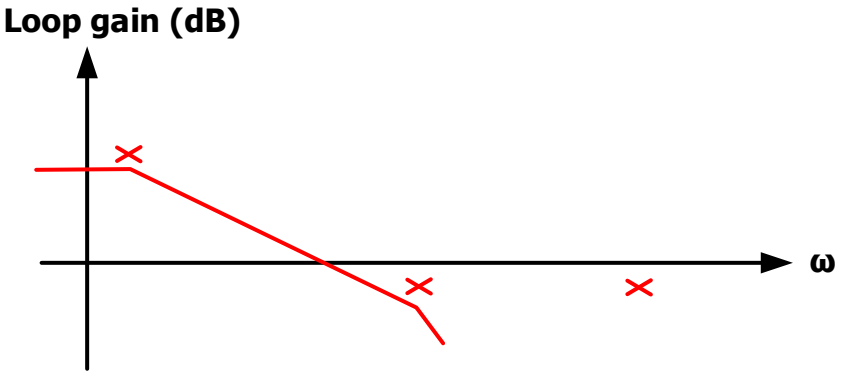

Fig. 2.14 A simplify loop gain transfer function for the proposed control loop

As concerned, it might be a risk for us to make the loop bandwidth extremely low by adding a low-frequency pole from the additional DC cancellation loop. The load transient speed of the buck converter might be significantly restricted. However, the

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concern is a fault, and the key factors of the load transient speed are the modulator to output gain GVC and the output impedance ZO. Both of these 2 factors are not affected by the DC cancellation loop and its low-frequency pole, which ensures the proposed control loop still remains the fast transient speed from the passive component loop. The simplified bode plots of GVC and ZO are shown in Fig. 2.15 and Fig. 2.16 respectively.

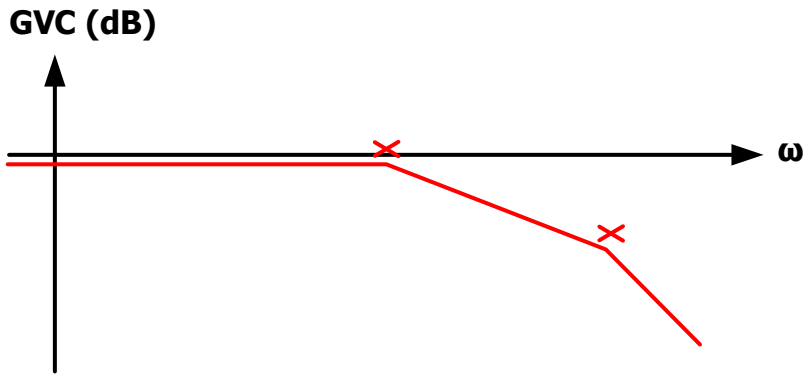

Fig. 2.15 A simplified controller to output gain GVC for the proposed control loop

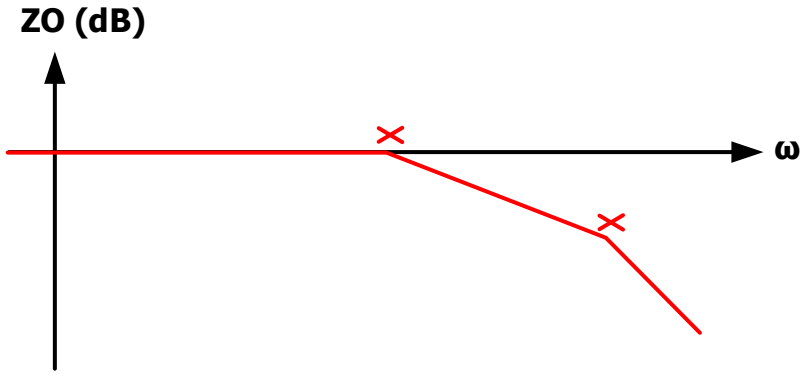

Fig. 2.16 A simplified output impedance GVC of the proposed control loop

A simulated bode plot result of the loop gain for the proposed control loop is shown in Fig 2.17. The cross symbol marks the pole made by the DC cancellation loop. The simulated bode plot results of the GVC and ZO for the proposed control loop are shown in Fig 2.18. and Fig 2.19. The cross symbols mark the pole decouple by the passive component compensation loop.

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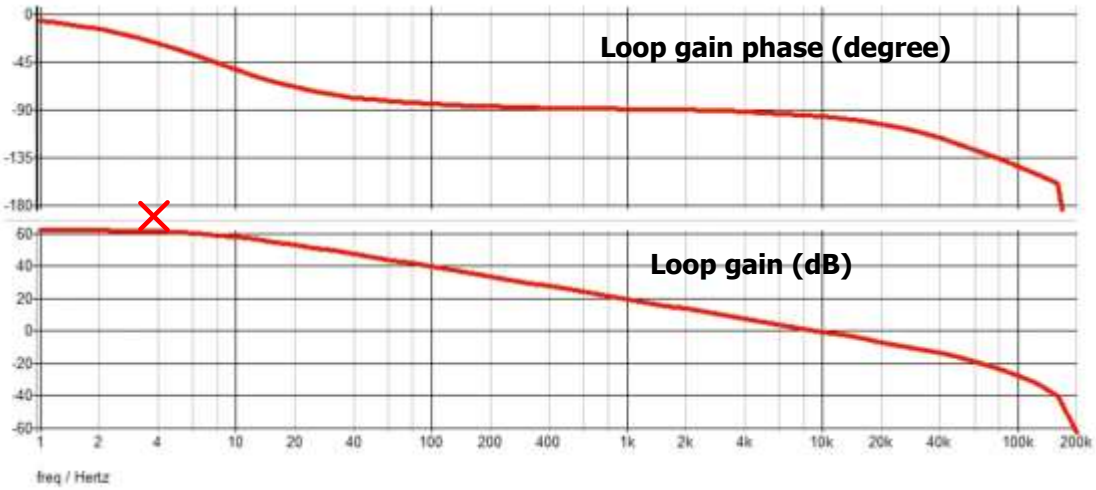

Fig. 2.17 Simulated bode plot of the loop gain

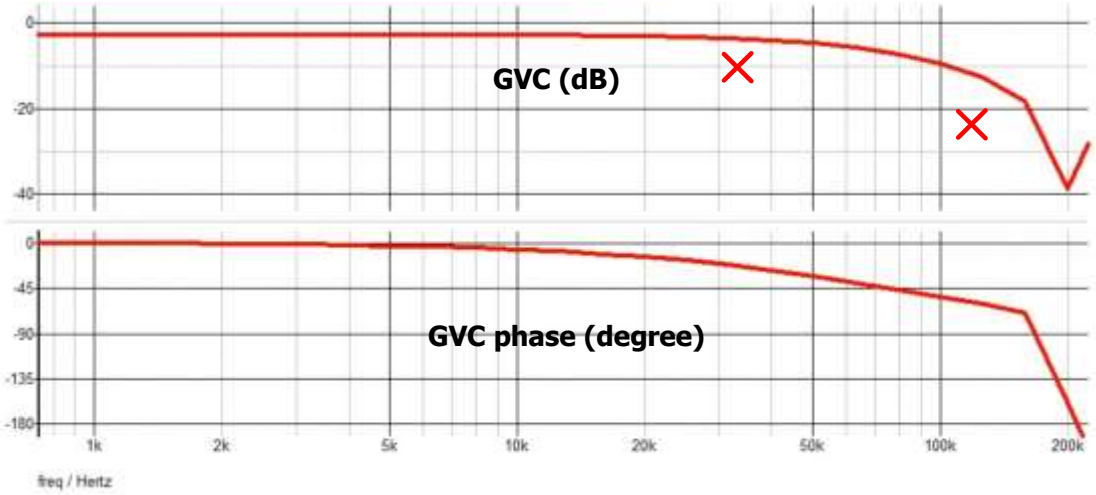

Fig. 2.18 Simulated bode plot of the modulator to output gain GVC

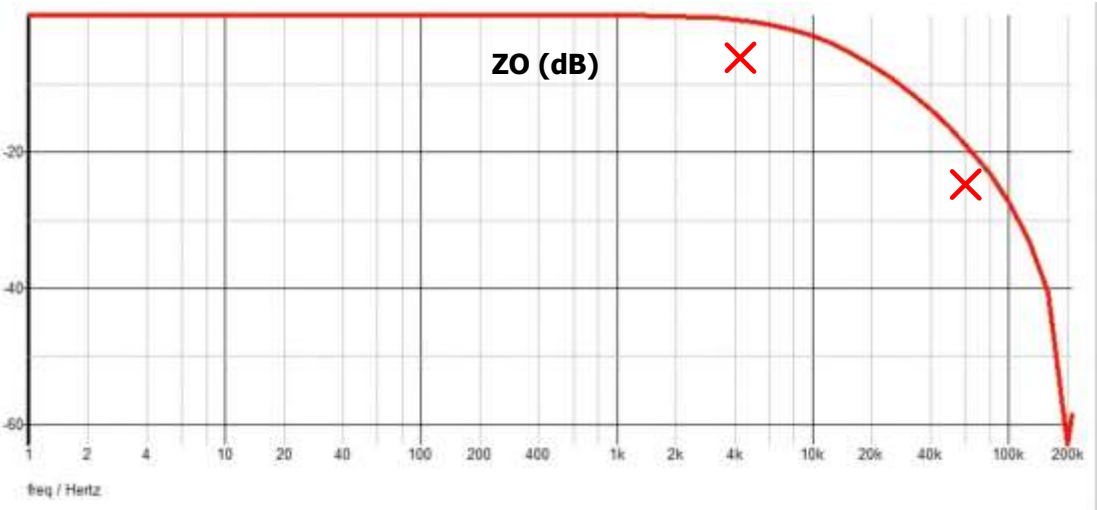

Fig. 2.19 Simulated bode plot of the output impedance ZO

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Chapter 3 Key Subblocks

3.1 Power stage and bootstrap circuit

The proposed buck converter utilizes an all N-FinFET power stage, which has a 1.5 times lower R_{dson} and a 1000 times lower leakage current compared to PFETs, in order to improve performance. Thus, a bootstrap circuit and level shifter are necessary. The level shifter generates a 2 times V_{IN} voltage to deliver the DUTY signal to the upper gate driver. The whole picture of the power stage and bootstrap circuit includes a dead-time generator (t_{dead}), a level shifter, two gate drivers, two power FETs, and several switches, as shown in Fig. 3.1.

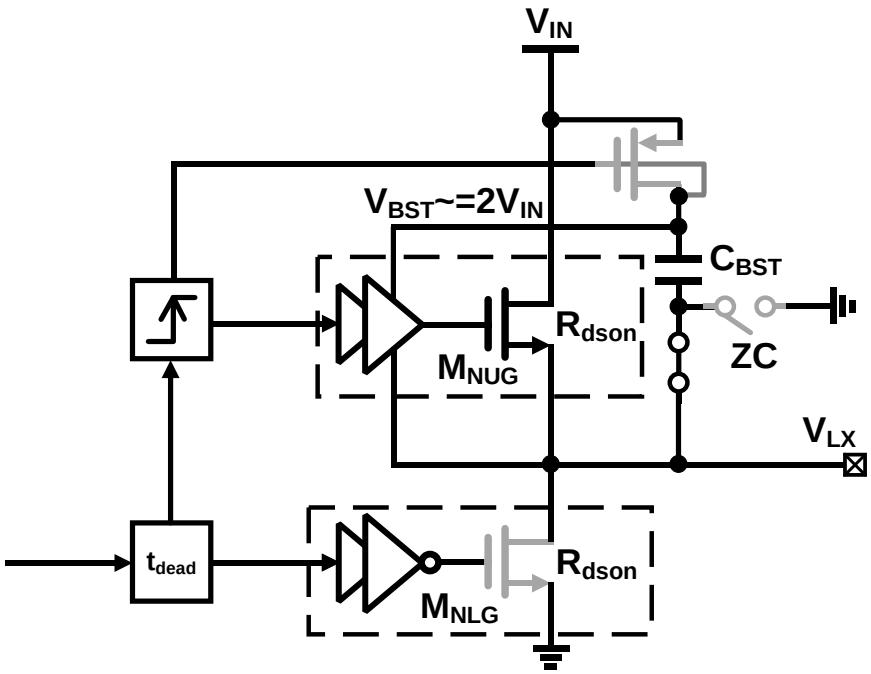

Fig. 3.1 The whole picture of the power stage and bootstrap circuit.

During continuous conduction mode (CCM), there are two states: T_{ON} (upper gate turn on) and T_{OFF} (bottom gate turn on). In the T_{ON} state, as shown in Fig. 3.2, when the DUTY signal goes from ground to V_{IN}, the t_{dead} circuit produces two non-overlapping signals for the level shifter and bottom gate driver. The bottom gate driver receives a pull-down voltage and turns off the bottom gate, while the pull-up voltage is

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delivered to the level shifter, which generates a $2V_{IN}$ voltage level for the upper gate driver to turn on the upper gate. As the upper gate turns on, the voltage of V_{LX} increases from ground to V_{IN} and pulls the voltage of V_{BST} up to $2V_{IN}$, supplying power to the upper gate driver through the capacitor C_{BST}. When the DUTY signal goes from V_{IN} to ground, as shown in Fig. 3.3, it enters the T_{OFF} state. Similarly, the t_{dead} circuit produces two non-overlapping signals, but a pull-up voltage is sent to the bottom gate driver to turn it on while a pull-down voltage is delivered to the level shifter, which brings the voltage down to ground and turns off the upper gate and turns on the bootstrap charging switch M_{BST}. As the upper gate is off and the bottom gate is on, the voltage of V_{LX} decreases from V_{IN} to ground, allowing the bootstrap capacitor C_{BST} to be charged to the voltage level of V_{IN} again, compensating for the power loss to the upper gate driver during the T_{ON} state.

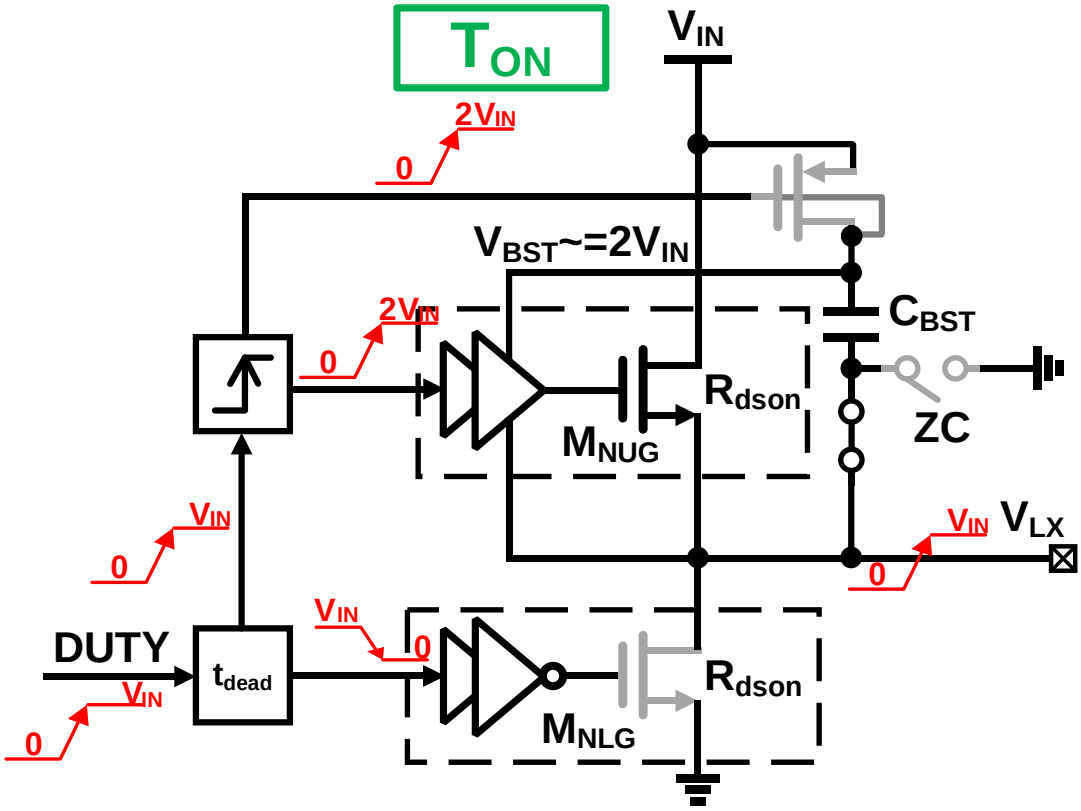

Fig. 3.2 Operation diagram of T_{ON} state.

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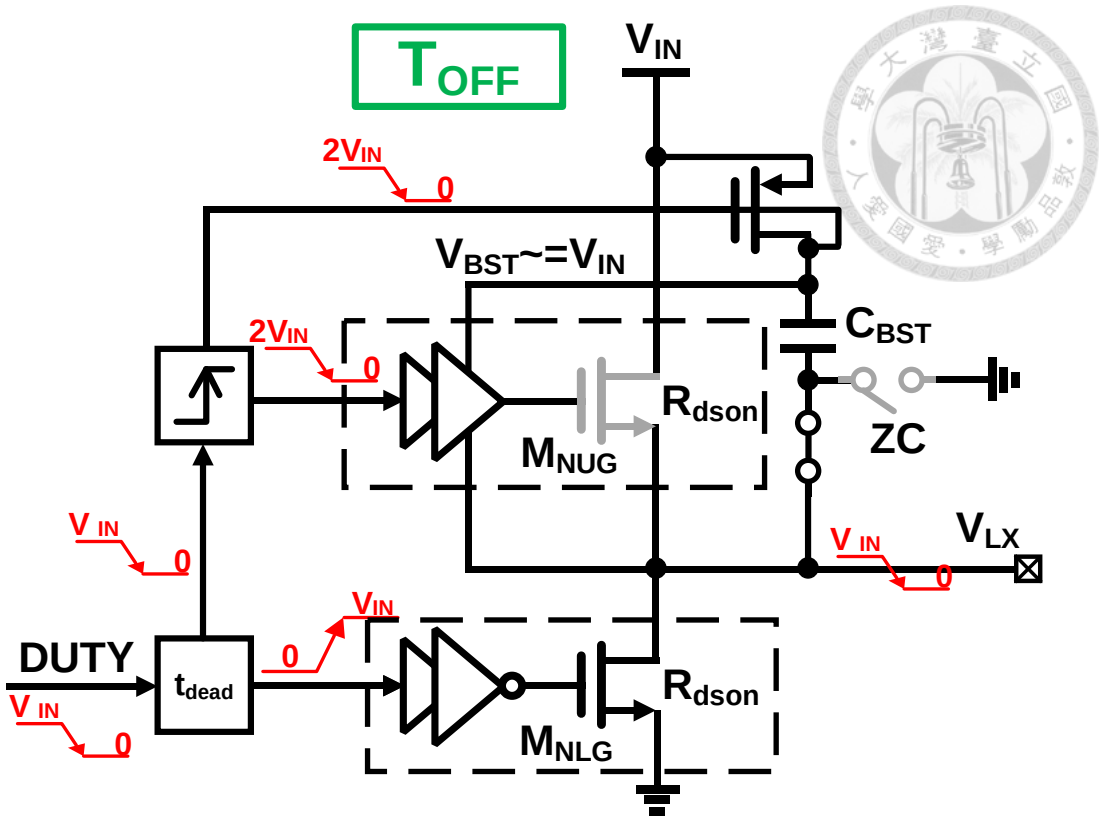

Fig. 3.3 Operation diagram of T_{OFF} state.

During discontinuous conduction mode (DCM), there is only one state, the ZC state, where both the upper gate and bottom gate are turned off. As shown in Fig 3.4, Once the zero-current signal ZC goes high to V_{IN}, the DUTY signal will always be at a low voltage level, causing the t_{dead} circuit to turn off the bottom gate. As both gates are turned off, the voltage of V_{LX} will be tied to V_O, disrupting the cross voltage of the bootstrap capacitor C_{BST}. To prevent this, switches S_{LX} and S_{ZC} are added to the bootstrap circuit. During CCM, S_{LX} is always on and S_{ZC} is always off. Once the ZC signal goes high, S_{LX} is turned off to prevent the V_O signal from affecting the cross voltage of C_{BST}, and S_{ZC} is turned on to charge the cross voltage of C_{BST} to V_{IN}.

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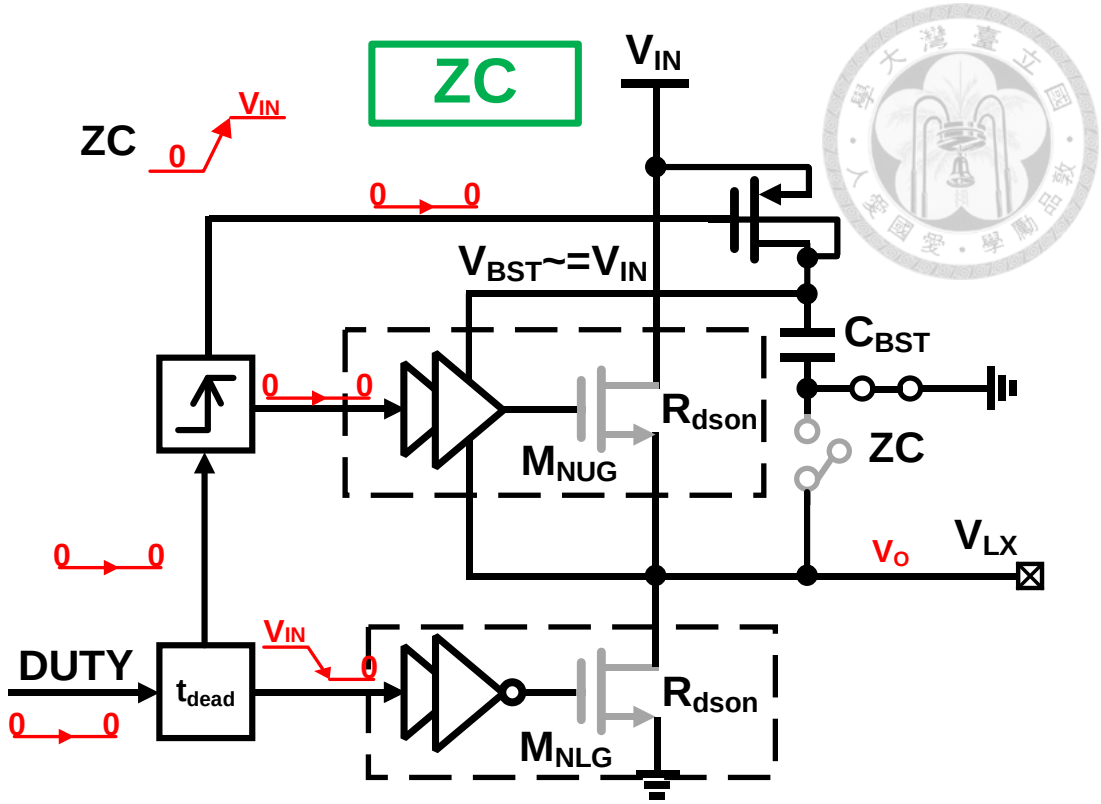

Fig. 3.4 Operation diagram of ZC state.

The transistor level of the level shifter is shown in Fig. 3.5. It consists of a non-overlapping circuit, two capacitors (C_{BA} and C_B), 1 PFET (M_P), and 4 NFETs (M_{NX}, M_{NX1}, M_{N1}, M_{N2}). The non-overlapping circuit produces non-overlapping opposite signals V_{DA} and V_{DB} to prevent overvoltage ($2V_{IN}$) on M_P during the transition. M_{NX} and M_{NX1} ensure the charge path for C_B and C_{BA}, respectively. M_P delivers the $2V_{IN}$ voltage level to the output during the T_{ON} state. M_{N1} pulls the voltage down to ground during the T_{OFF} state, and M_{N2} blocks the $2V_{IN}$ overvoltage for M_{N1} during the T_{ON} state. The body of M_P, M_{N1}, and M_{N2} are tied to the source, and the body of M_{NX} and M_{NX1} are tied to the drain to prevent overvoltage.

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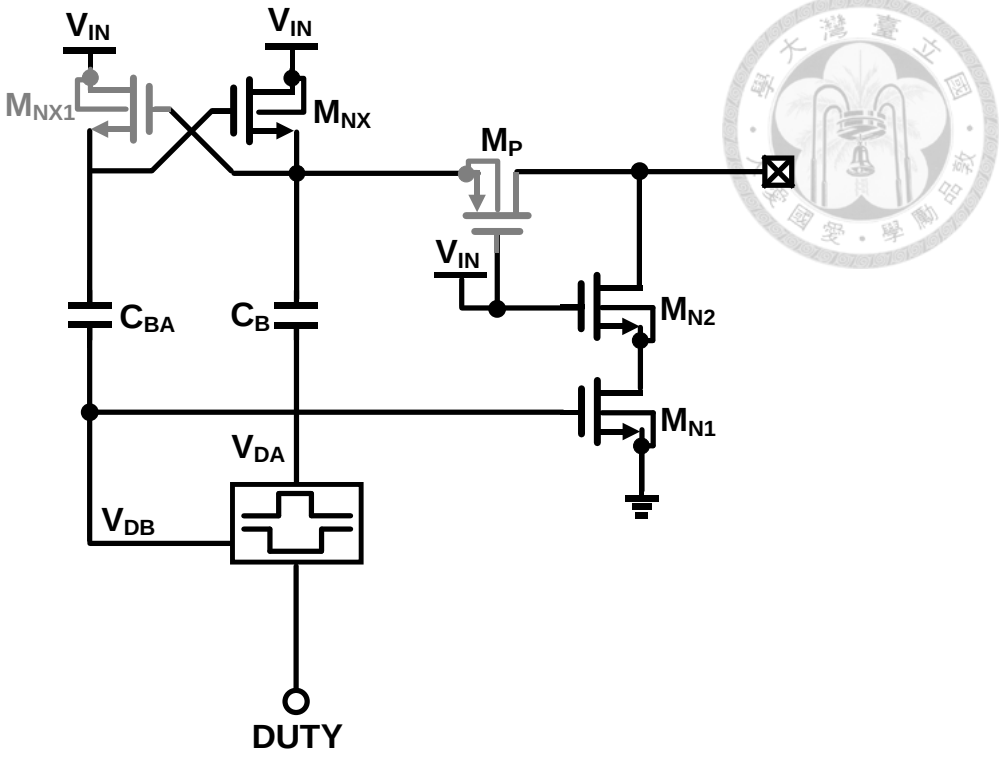

Fig. 3.5 The transistor level of the level shifter.

Fig. 3.6 shows a detailed operation diagram of the power stage and bootstrap circuit with the level shifter. In conclusion, the proposed all N-FinFET power stage has a 35 mOhm R_{dson} and a few nano-ampere leakage current, which optimizes the efficiency of the converter under both heavy loading and ultra-light load conditions.

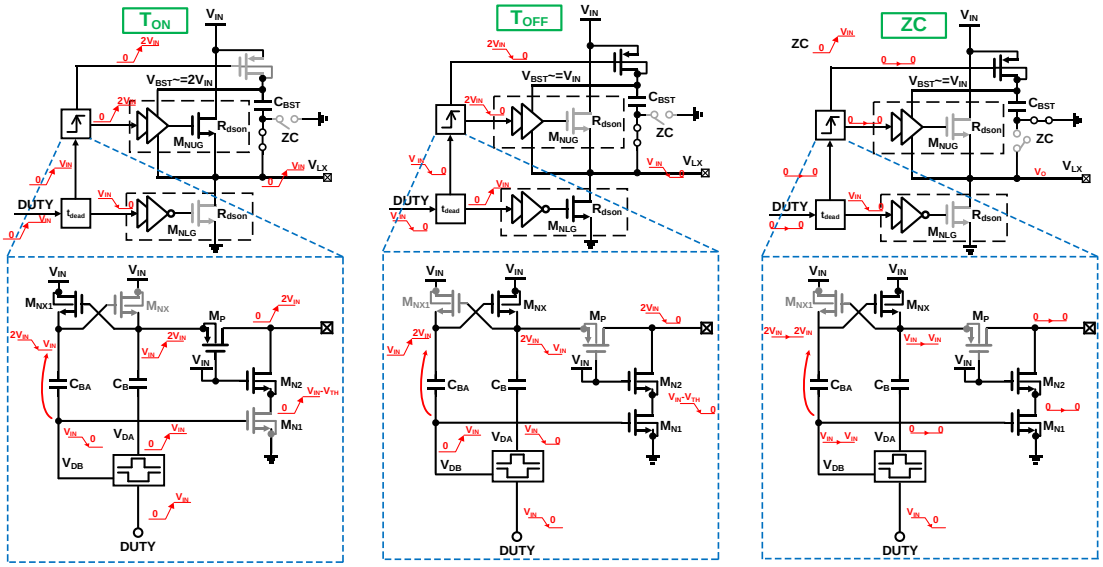

Fig. 3.6 A detailed operation diagram of the power stage and bootstrap circuit.

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3.2 The DC cancellation loop with auto-zero technique

As a power converter utilizing ripple-based control, there is a common problem with DC offset due to the lack of adjustment of the ramp voltage during modulation with the reference voltage. To address this issue, I have devised a solution in the form of a DC offset cancellation loop. This loop serves to adjust the ramp voltage to an appropriate level and ensure that the output voltage level V_O is locked into the reference voltage V_{REF}. A simplified signal diagram of the proposed DC cancellation scheme is shown in Fig. 3.7. Prior to the cancellation, the ramp voltage V_{PSR}' had a faulty phase, resulting in an offset in the output voltage V_O. The proposed DC cancellation loop shifts the phase of V_{PSR} to cancel the offset voltage on V_O and ensures the accurate output voltage level.

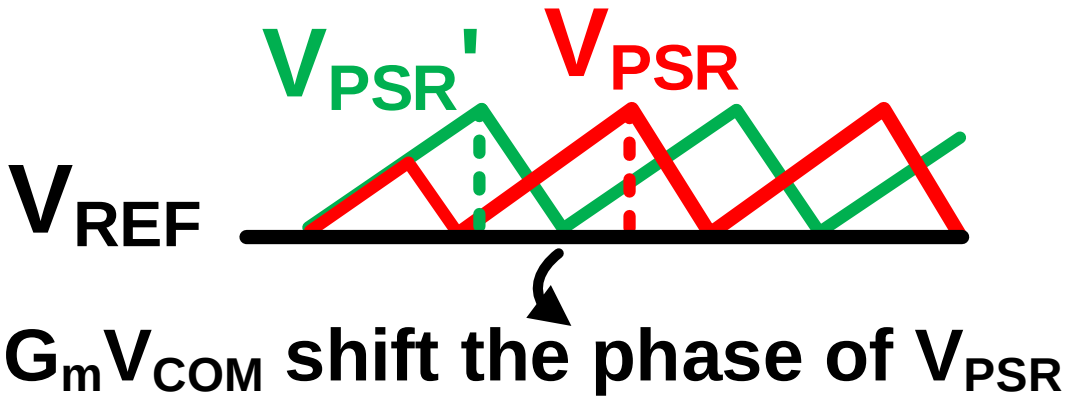

Fig. 3.7 A simplified signal diagram of the proposed DC cancellation scheme

Fig. 3.8 displays the detailed architecture of the DC cancellation loop. The loop comprises an error amplifier with an auto-zero technique followed by a normal error amplifier. To reduce the offset voltage in the amplifier, an additional offset cancellation technique is necessary. There exist two conventional methods for eliminating the error amplifier's offset voltage, namely chopping, and auto-zeroing. Chopping necessitates two choppers, a low-pass filter, and an extra 50% duty-cycle clock generator for

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operation, which would consume a substantial amount of power. Conversely, the auto-zeroing technique only requires a few switches to function. The disadvantage of auto-zeroing is that the operation diagram may restrict the transient speed. Nonetheless, the DC offset cancellation loop is designed to be a very low bandwidth circuit, and speed is not a significant concern. The additional clock generator for the chopping technique may consume more power and complicate the circuit. After assessing the pros and cons of each technique, I have chosen to utilize the auto-zeroing technique as it meets the requirements flawlessly. The DC cancellation loop is composed of 2 error amplifiers, the switches, and a capacitor for the auto-zeroing technique.

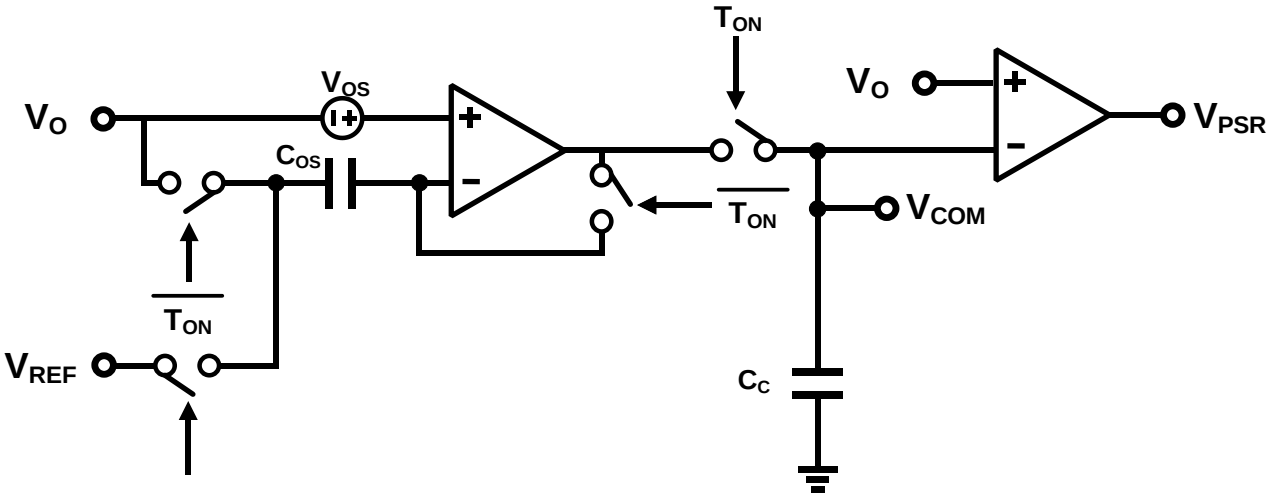

Fig. 3.8 The whole architecture of the DC offset-cancelation loop

The proposed auto-zeroing technique in the DC cancellation loop consists of two phases: the T_{ON} phase and the T_{OFF} phase. During the T_{ON} phase, the first error amplifier operates to fine-tune the voltage level to V_{COM}, which is then restored by the capacitor C_C. In the T_{OFF} phase, the first error amplifier is disconnected from the DC cancellation loop and performs offset cancellation, while the V_{COM} restored in C_C during the T_{ON} phase serves as the output of the first error amplifier. Fig. 3.9 illustrates the operation diagram during both the T_{ON} and T_{OFF} phases.

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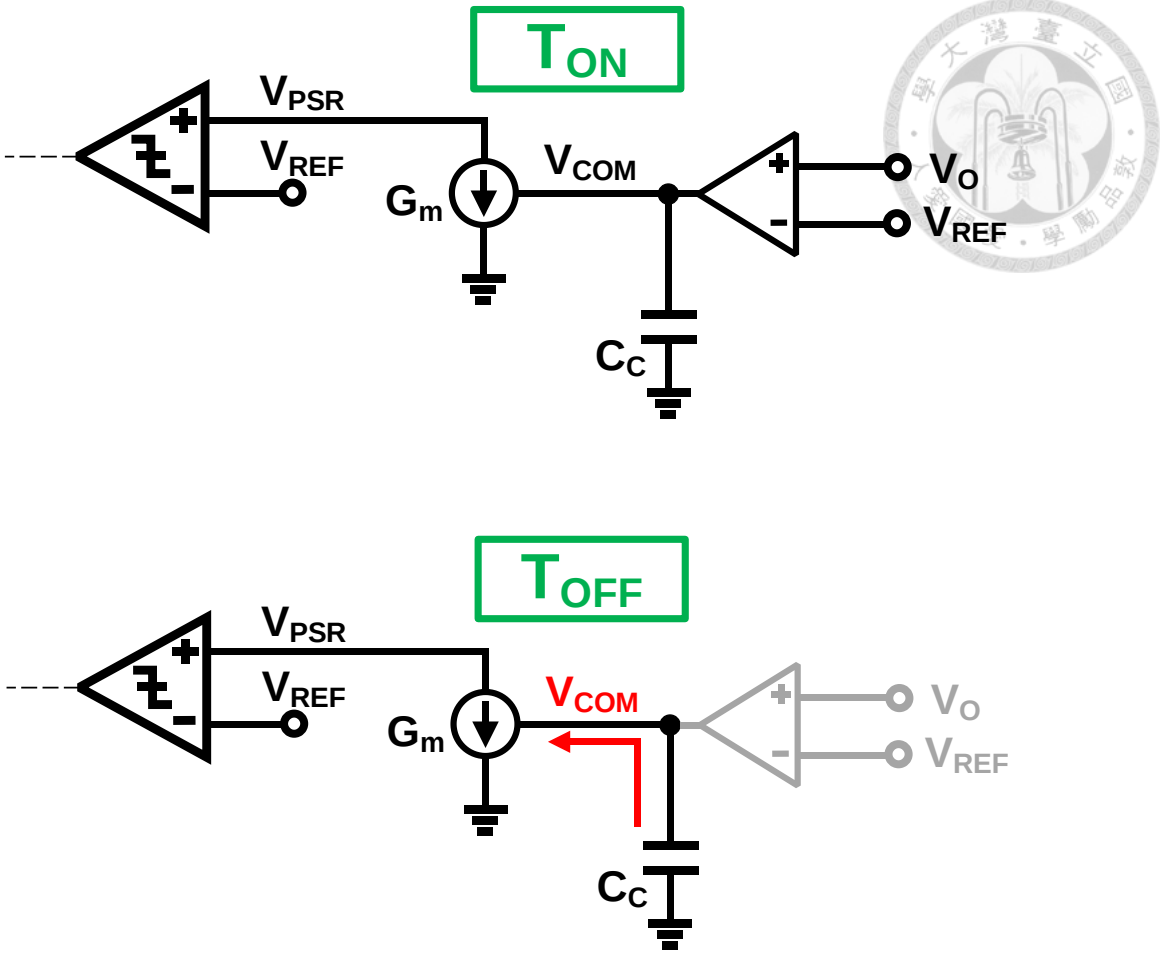

Fig. 3.9 The operation diagram of T_{ON} and T_{OFF} state.

The detailed operation and the equivalent circuit of two phases are shown in Fig. 3.10 During the T_{ON} phase, the voltage level of the signal DUTY is high and the circuit is connected to the system loop. The negative feedback theory ensures that the two input terminals are virtually shorted, satisfying equation 1 ($V_O + V_{OS} = V_{REF}$ + the cross voltage of C_{OS}). The voltage level of V_O on capacitor C_C is also restored due to the negative feedback of EA_2.

In the T_{OFF} phase, the voltage level of the signal DUTY is low, and the circuit is connected to its own inner closed loop. Like the T_{ON} phase, the negative feedback theory ensures a virtual short between the input terminals, satisfying equation 2 ($V_O + V_{OS} = V_O$ + the cross voltage of C_{OS}). Substituting the cross voltage of $C_{OS} = V_{OS}$ into

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equation 1 allows for the cancellation of V_{OS} on both sides. Therefore, the equation $V_O = V_{REF}$ is guaranteed. The voltage level of V_{COM} is also maintained at V_O during the T_{OFF} phase for the general operation of the system. Upon the end of the T_{OFF} phase, the cross voltage of C_{OS} is maintained at V_{OS} for offset cancellation as the T_{ON} phase begins. This effectively eliminates the offset voltage caused by the mismatch of the amplifier.

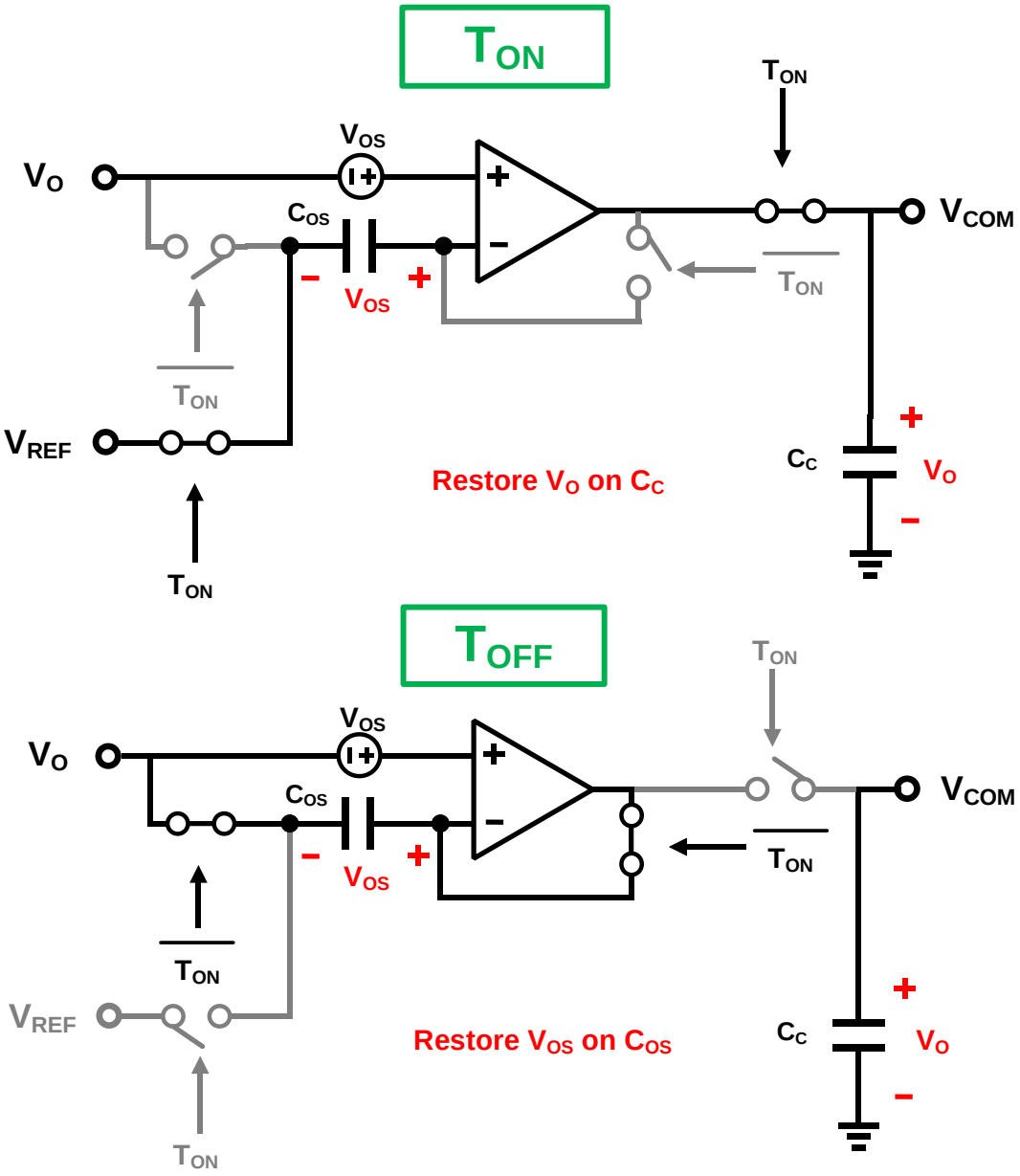

Fig. 3.10 The detailed operation and the equivalent circuit of T_{ON} and T_{OFF} state.

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3.3 Ultra-low quiescent current bandgap reference voltage

The proposed bandgap reference has been designed to maintain a stable and accurate reference voltage, while minimizing average current consumption, in response to the requirement for low quiescent current in DCM. To accomplish this objective, I have devised a bandgap reference that can be entirely switched off, thereby reducing the circuit's average current. The detailed schematic in transistor level of the proposed bandgap is depicted in Fig. 3.11 and is comprised of three main components. The timing logic generates the necessary digital timing signals. Subsequently, the bandgap core generates the accurate reference voltage and delivers it to the reference capacitor C_{REF}. The low leakage sample and hold circuit is responsible for maintaining a stable voltage over a prolonged period.

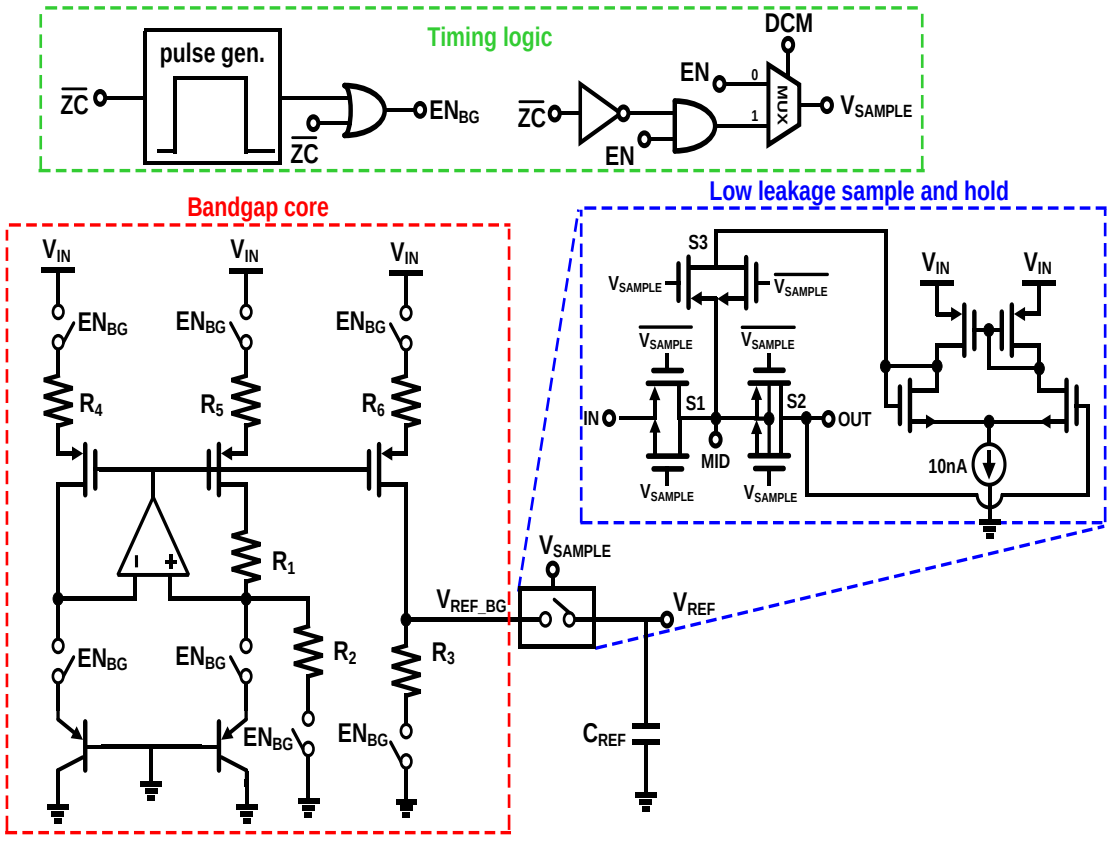

Fig. 3.11 The detailed schematic in transistor level of the proposed bandgap reference

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Fig. 3.12 and Fig 3.13 present a comprehensive timing diagram and its logic gates for the complete sample and hold scheme. During DCM, the bandgap reference functions in a sample and hold mode. Upon activation, it triggers the pulse generator and generates the enable signal for the bandgap core (EN_{BG}). Initially, the bandgap core settles without the reference capacitor (1st settling), and the subsequent sample and hold circuit retains the previous reference voltage level. When the enable signal (EN_{BG}) goes low, the sample signal (V_{SAMPLE}) goes high, and the subsequent circuit commences sampling the updated reference voltage (V_{REF}) (2nd settling). The sampling process (2nd settling) concludes when the enable signal (EN_{BG}) goes low and retains the reference voltage (V_{REF}) until the next sampling phase. Due to the complete shutdown and restart of the bandgap core, the voltage overshoot during 1st settling is considerably larger than that in 2nd settling. By rendering the 1st settling independent of the reference capacitor, I can expedite the settling process, reduce the overshoot in the reference voltage (V_{REF}), and stabilize it during the 2nd settling. This is the operating mechanism during DCM. In CCM, the bandgap reference operates continuously, and the sampling signal (V_{SAMPLE}) remains at a high voltage level throughout.

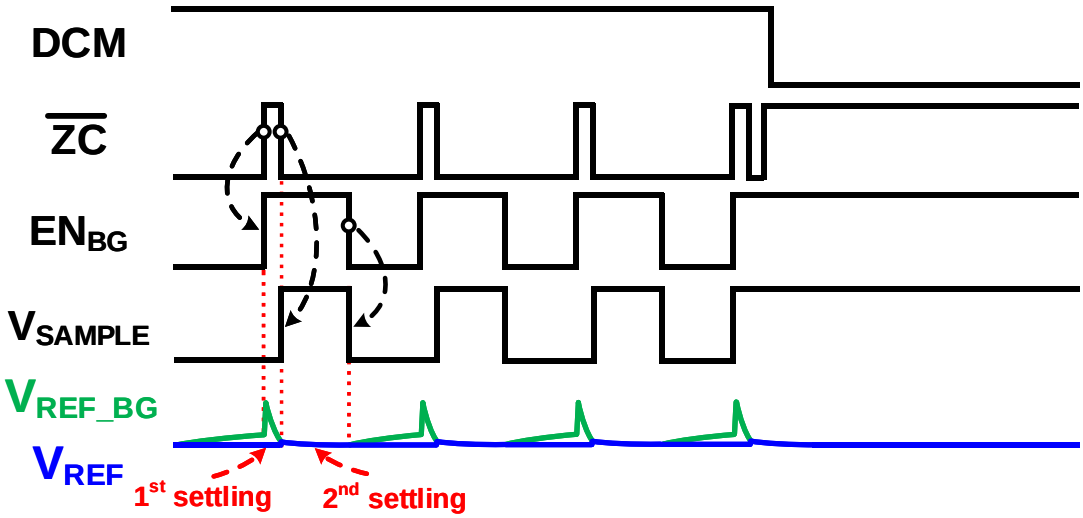

Fig. 3.12 Timing diagram of the proposed bandgap reference

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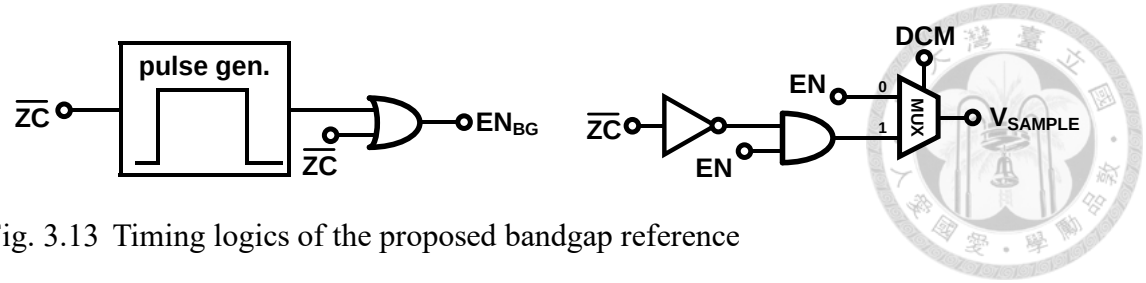

Fig. 3.13 Timing logics of the proposed bandgap reference

In order to generate an accurate voltage for the system, I have employed the conventional current mode bandgap core along with some techniques. As illustrated in Fig. 3.14, the resistors (R_1-R_6) situated between the current mirror and V_{IN} are utilized for source degeneration. In general, there is a trade-off between bandwidth and mismatch. However, the source degeneration technique serves as an effective solution for balancing these two parameters. Therefore, I have adopted this technique to ensure the bandgap core's accuracy and speed, thereby enabling the generation of a stable reference voltage within a period of $1/F_{SW}$.

Another technique utilized in this bandgap core for achieving faster start-up speed and lower quiescent current is power gating. The power gating switches, which are controlled by the enable signal EN_{BG}, play a pivotal role in this technique. These switches store the nodal voltage during operation and retain it when the bandgap core is shut down. This results in a slight reduction in the start-up period, meeting the requirement for switching. Additionally, the original current leakage of the resistors was relatively high and did not align with the design objective. However, by introducing power gating switches between V_{IN} and the resistors, I were able to significantly reduce the current leakage.

There is one further difference between the proposed bandgap core and the conventional version. The conventional current mode bandgap may become deadlocked during start-up due to its bistable characteristic, requiring the addition of an extra start-up circuit to prevent the deadlocked scheme. However, the inclusion of an extra start-up circuit would consume additional power and increase the average current to the

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system. Consequently, I remove the resistor connected to the negative input of the operational amplifier and transform the bandgap core into a monostable system.

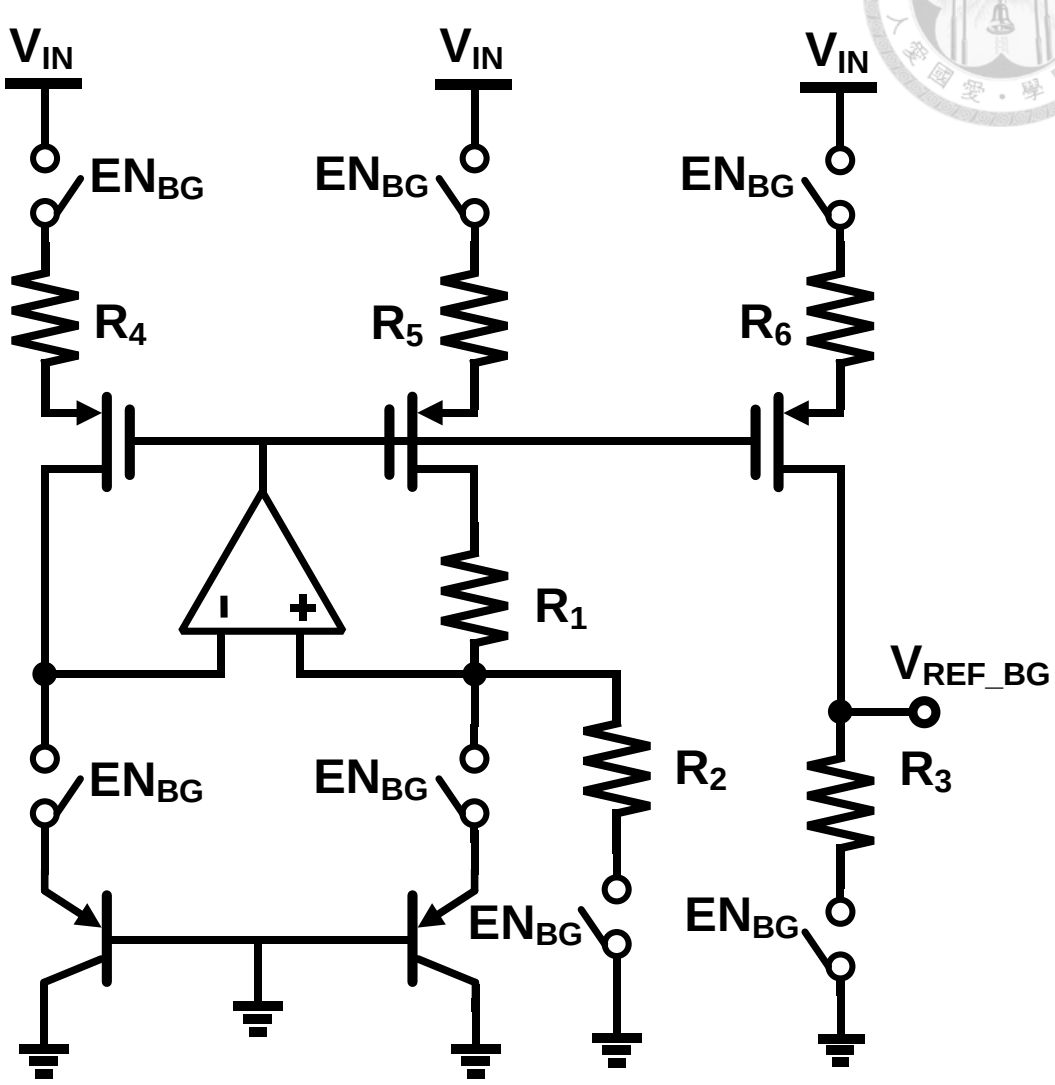

Fig. 3.14 The detailed transistor-level schematic of the bandgap core

Fig. 3.15 shows the transistor-level schematic of the low leakage sample and hold circuit. The design requires a stable reference voltage in DCM. When the load is down to a few microamperes, the switching frequency is only a few kilohertz. As a result, I need a sample and hold circuit with a longer hold time. The conventional sample and hold circuit cannot hold the output voltage for a long time and keep it stable due to issues with source-drain, source-body, and drain-body leakage. The low leakage sample and hold circuit is made up of 3 switches (S1, S2, S3) and a simple amplifier with a low

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bias current. During the sampling phase, S1 and S2 are closed and S3 is open, so the input signal is connected to the output directly. During the holding phase, S1 and S2 are open and S3 is closed. The amplifier continuously closes the voltage gap between MID and OUT, which greatly reduces the source-drain leakage in S2. In addition, the body-source tie in S2 leads to a significant reduction in source-body and drain-body leakage. As shown in Fig. 3.16, the low leakage sample and hold technique reduce the leakage voltage level from 100 mV/ms to 0.43 mV/ms, almost 200 times less compared to the conventional sample and hold circuit.

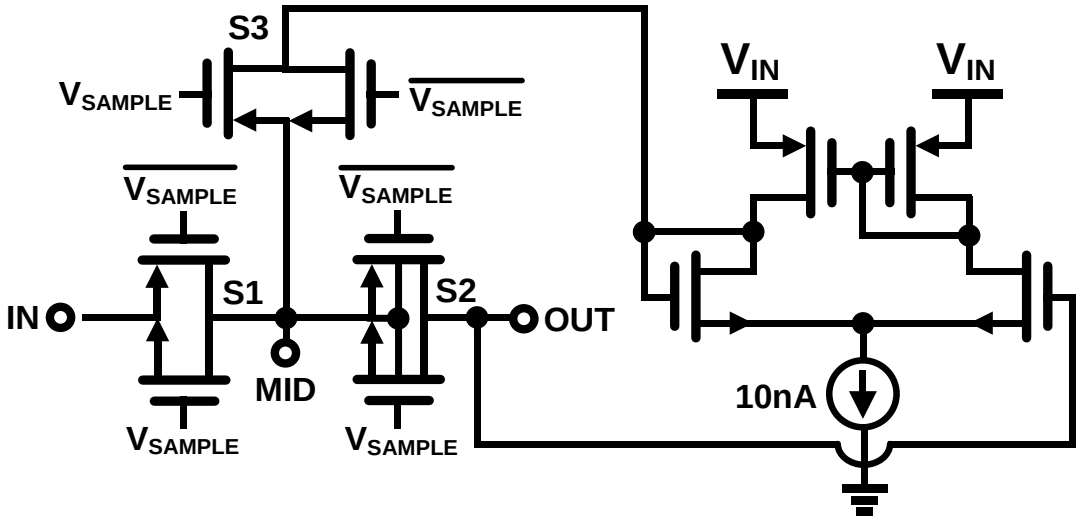

Fig. 3.15 The transistor-level schematic of the low leakage sample and hold circuit

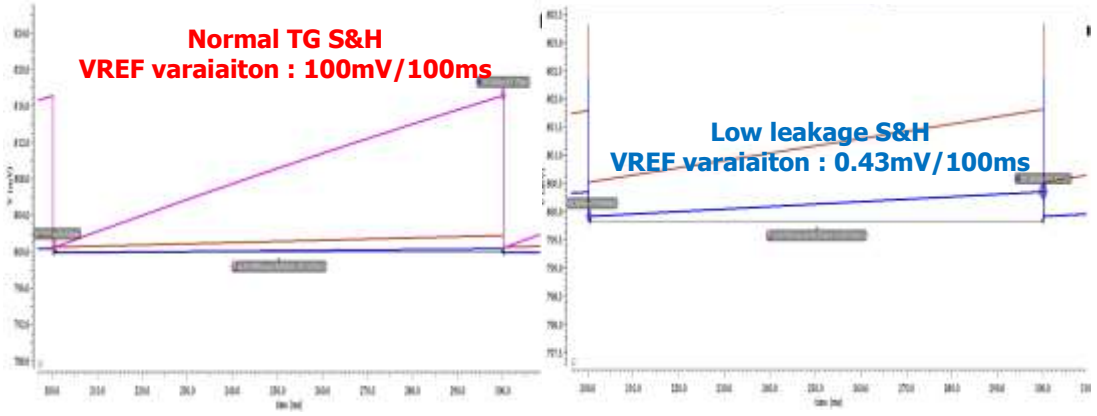

Fig. 3.16 A comparison is made between the normal sample and hold circuit and the low leakage sample and hold with regards to the variations of reference voltage

Fig. 3.17 – Fig. 3.19 shows the further Monte-Carlo simulation of the proposed

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bandgap reference. Ultimately, I have successfully developed a current mode bandgap reference that features minimal mismatch, a stable reference voltage (3σ ~= 1.5%), an extremely low quiescent current (20 nA), and low leakage holding, all of which perfectly aligns with the design objectives.

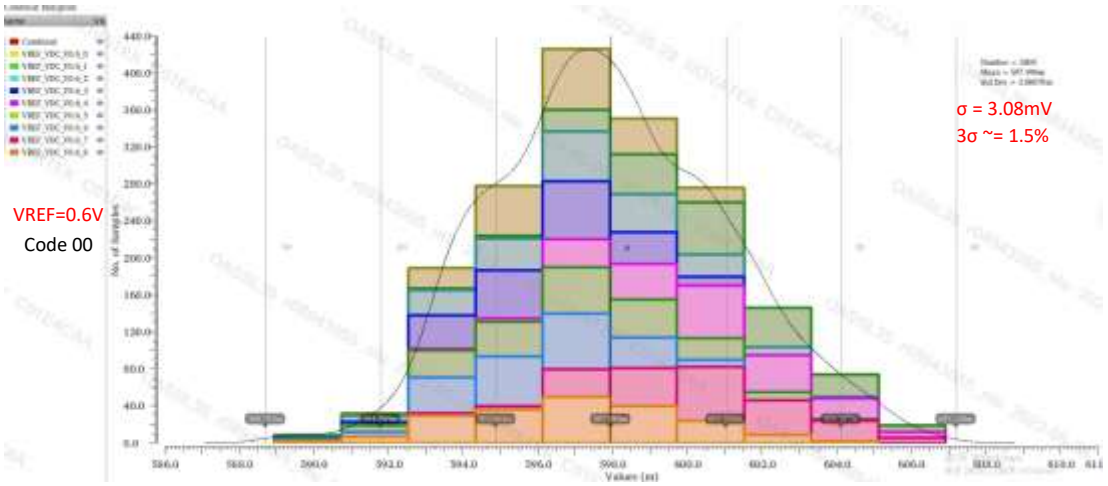

Fig. 3.17 Sweep temp: -40°~120°, V_{IN}:1.6V~2V, all corners, for V_{REF} = 0.6V

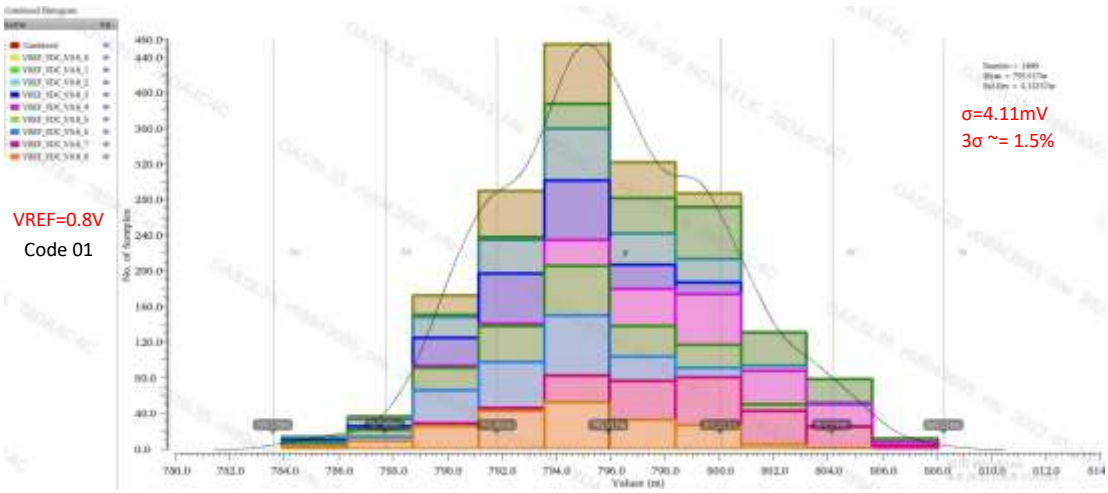

Fig. 3.18 Sweep temp: -40°~120°, V_{IN}:1.6V~2V, all corners, for V_{REF} = 0.8V

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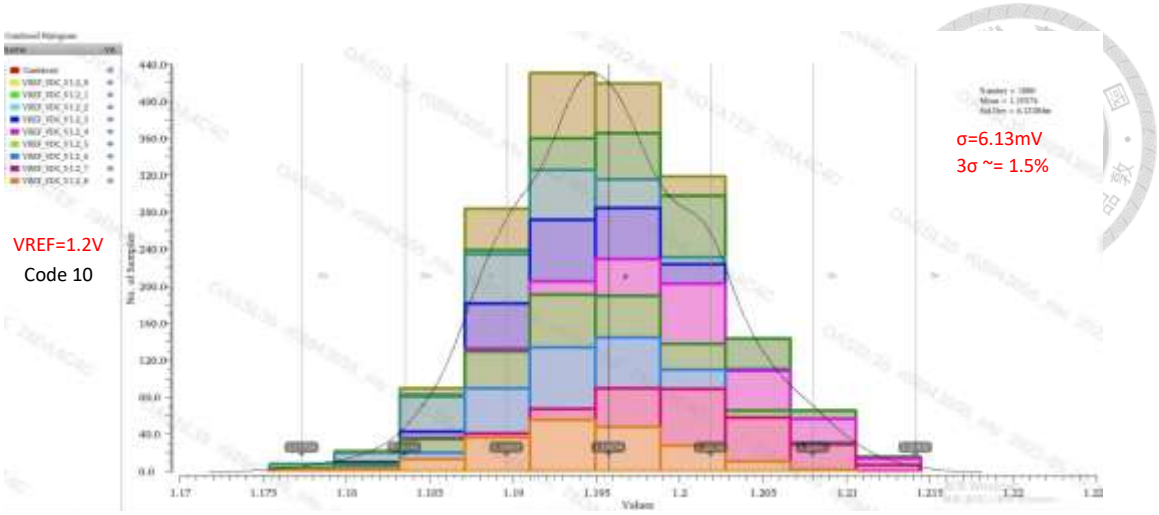

Fig. 3.19 Sweep temp: -40°~120°, V_{IN}:1.6V~2V, all corners, for V_{REF} = 1.2V

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3.4 10nA Constant gm circuit

I adopt a conventional constant gm along with a specialized soft-start technique. It produces a few 10 nA biasing current for the main comparator and a low-leakage sample-and-hold circuit for the bandgap reference. Additionally, it includes soft-start circuitry for the entire system. The whole architecture is shown in Fig. 3.20.

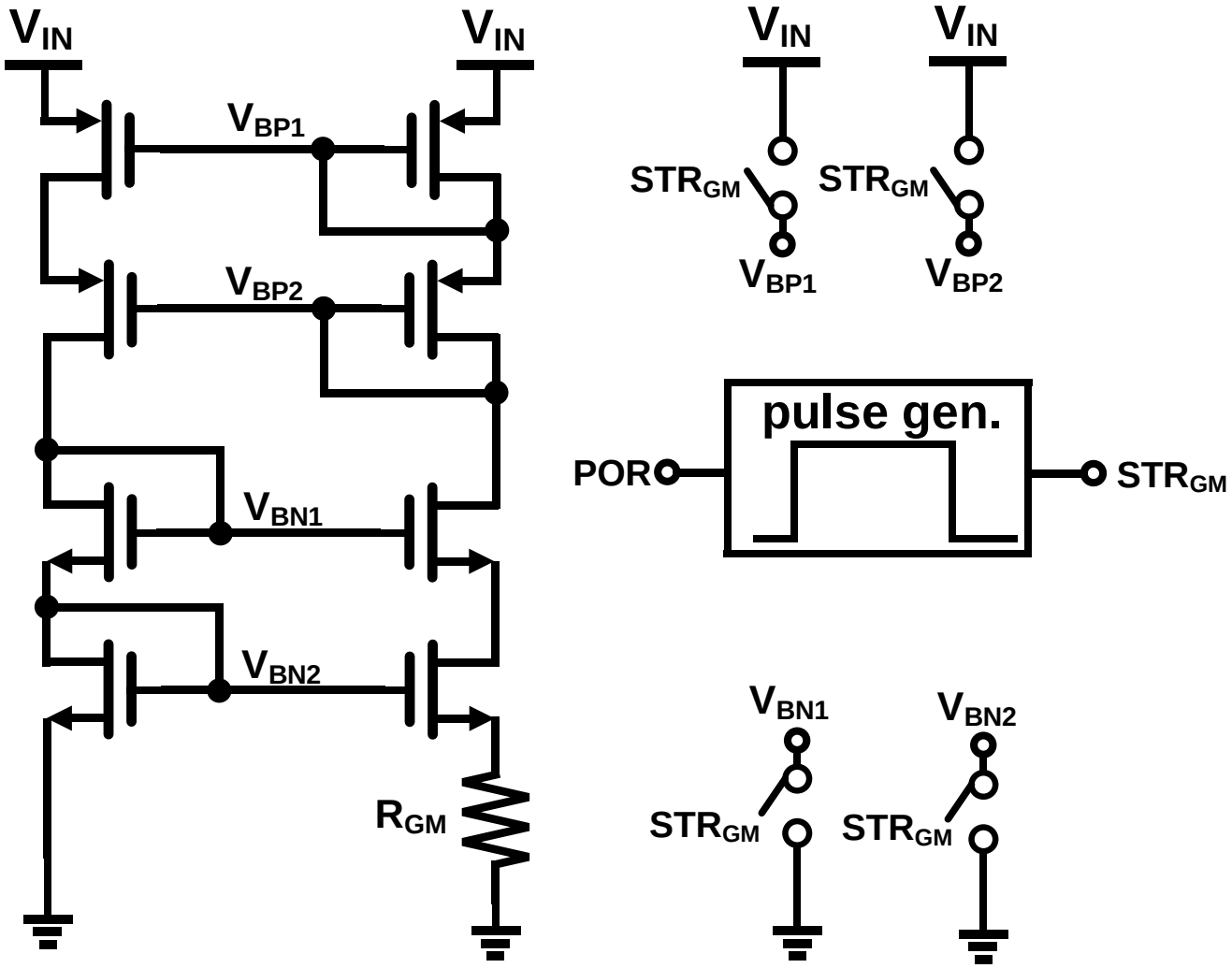

Fig. 3.20 Proposed constant gm in transistor level

Fig. 3.21 displays a comprehensive operational diagram. As V_{IN} rises from GND to VDD, the POR signal pulls up. This signal initiates the pulse generator, generating a soft start signal STR_{GM}. Subsequently, STR_{GM} activates all soft start switches for approximately 100 ns, raising V_{BP1} and V_{BP2} to V_{IN} and V_{BN1} and V_{BN2} to GND, respectively. This avoids the constant gm's deadlock state from start-up, and effectively

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prevents static power consumption from the conventional constant gm soft-start circuit.

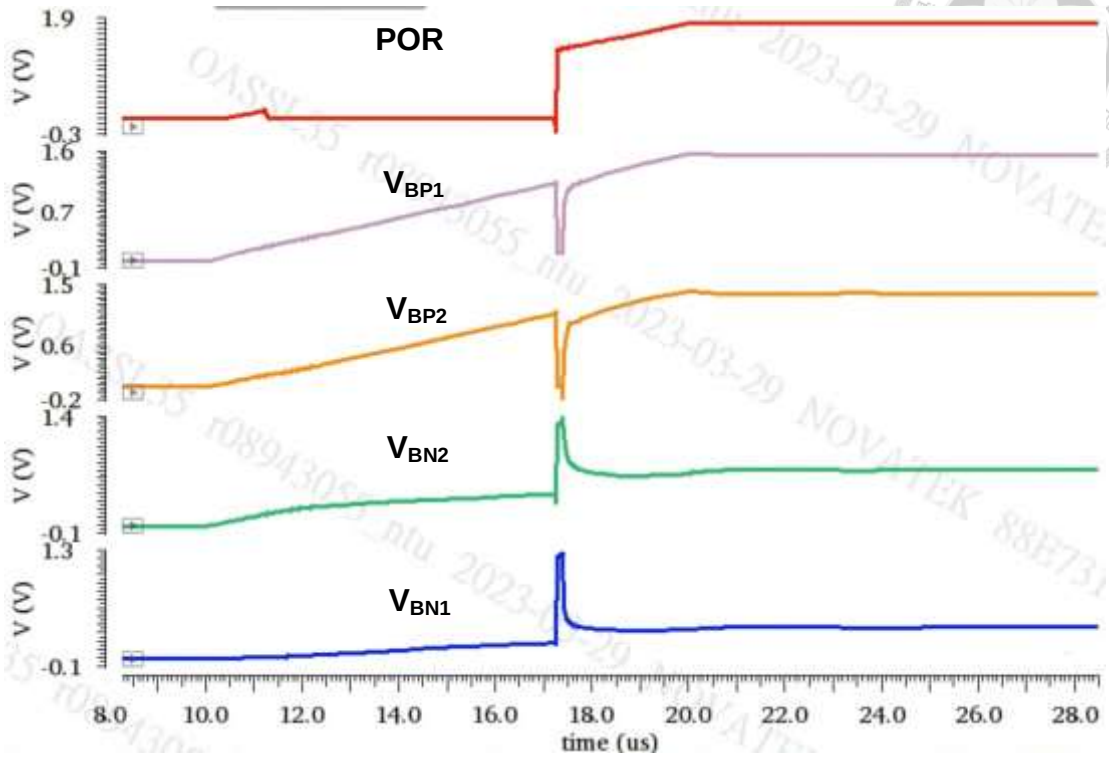

Fig. 3.21 Soft-start operation diagram of the proposed constant gm

3.5 Adaptive dead-time generator

Regarding dead-time management, it is insufficient to rely on a simple fixed dead-time generator for the proposed buck converter since a wide range of output inductor and capacitor values can be used, resulting in variations in driver delay and non-ideal effects. Therefore, an adaptive dead-time structure, depicted in Fig. 3.22, is utilized to accommodate the need for adjusting the length of dead-time.

The proposed adaptive dead-time generator is constructed using amounts of logic gates and a transmission gate. To prevent issues related to shoot-through, I must avoid the occurrence of both the upper gate and the lower gate being turned on simultaneously. For the dead-time of the upper gate signal V_{UG}, it is imperative that it goes high only after the lower gate signal V_{LG} has gone low. To achieve this, an AND gate is employed, and one of its inputs is connected to the opposite voltage level of V_{LG}. Regarding the

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dead-time of the upper gate signal V_{LG}, a similar structure is used. However, due to the following bootstrap circuitry, the upper gate signal is transferred to a voltage domain that is twice V_{IN}, which results in an additional delay for turning on/off the upper gate. This delay can cause the shoot-through issue, which can reduce efficiency and even cause damage to the power FETs. As a solution, a V_{LX} sensing loop is necessary.

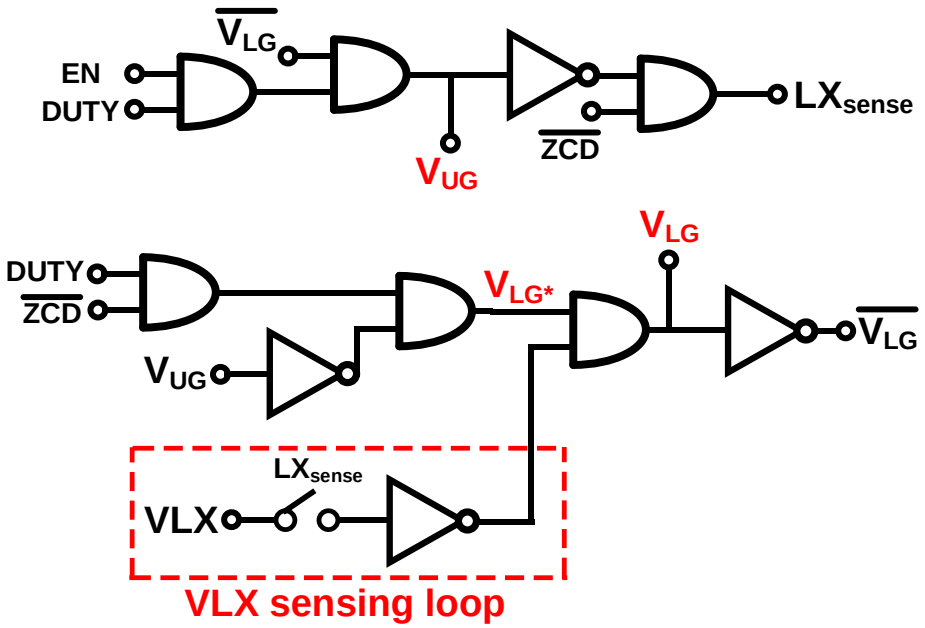

Fig. 3.22 Full structure of the adaptive dead-time generator

Fig. 3.23 displays a comprehensive operation diagram of the proposed adaptive dead-time generator. As the duty signal goes high, it triggers V_{UG} to go high, and the upper gate is turned on, causing the voltage level between power FETs VLX to become V_{IN}. Conversely, as the duty signal goes low, it triggers the signal V_{LG*} to go high, which turns on the VLX sensing loop. The design of the VLX sensing loop ensures that when the VLX goes low to ground which indicates that the upper gate is completely turned off, the loop releases a high voltage level and pulls the signal VLG to V_{IN}. As a result, the signal buffered by the following gate driver, V_{UG_DRIVER} and V_{LG_DRIVER} become not overlap. This technique effectively prevents most of the shoot-through issues.

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In summary, I have developed an adaptive dead-time generator that can handle a wide range of output inductor and capacitor values with a VLX sensing technique.

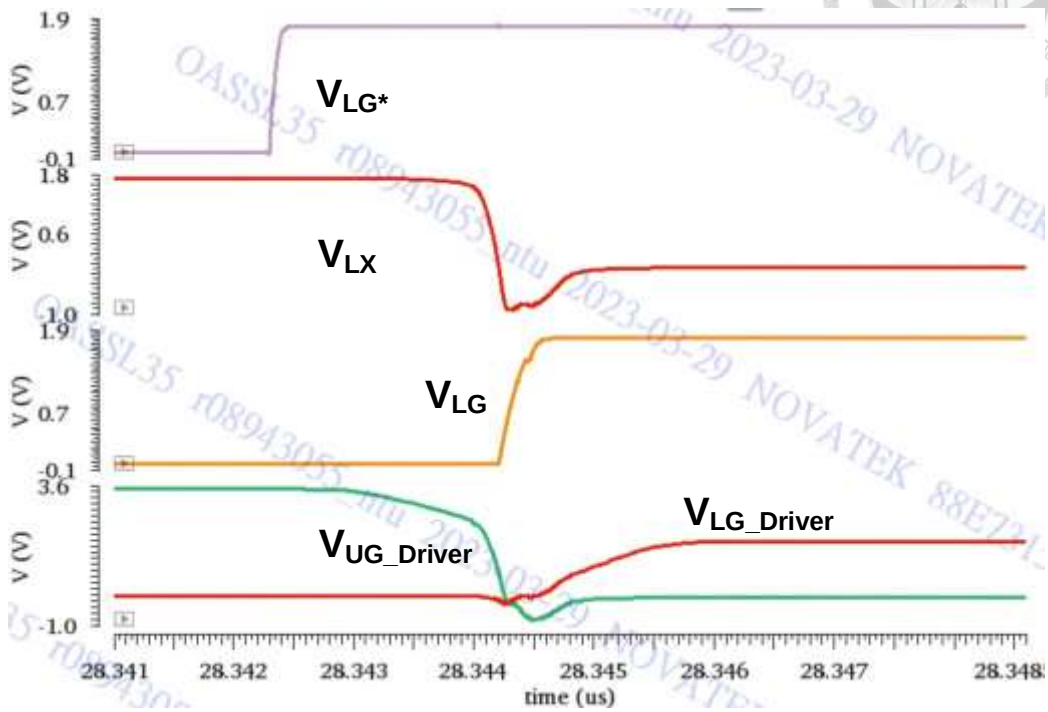

Fig. 3.23 A comprehensive operation diagram of the proposed adaptive dead-time generator.

3.6 Main comparator

I have introduced a specialized comparator that adheres to a wide loading range design with three specific biasing loops for CCM and DCM. The comparator's primary structure comprises a 2 stages dynamic comparator with three distinct biasing loops. To prevent subharmonic issues during CCM, the main comparator's response time must be shorter than the minimum T_{OFF}. In contrast, for DCM, the entire comparator's power consumption should not exceed an average of 100 nA to achieve the low quiescent current objective. I have also incorporated a current boost loop to further reduce the main comparator's response time for improved performance. Please refer to Fig. 3.24 for a complete view of the architecture in the transistor level.

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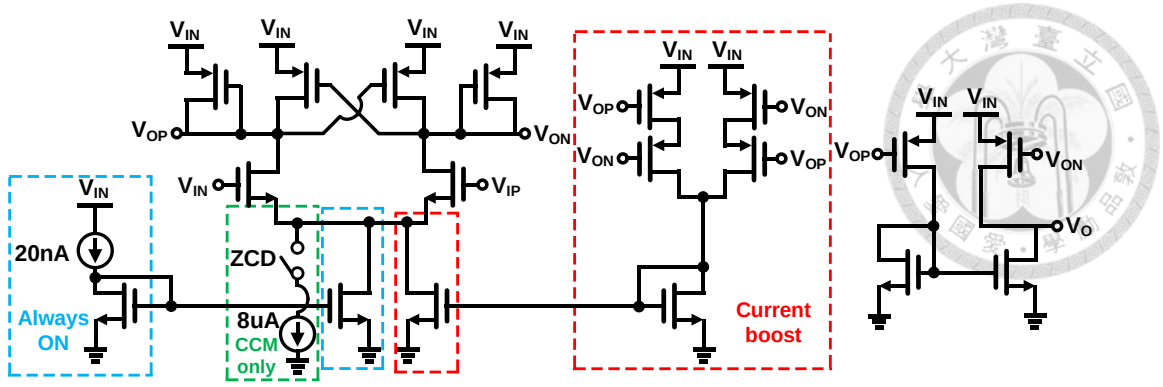

Fig. 3.24 The whole architecture of the proposed comparator in transistor level.

To shorten the comparator's response time during CCM, I activate the CCM only 8uA bias. As previously mentioned, the main comparator's response time must be faster than the minimum T_{OFF}, which is calculated as $1/F_{SW} * (C_{OFF}/(C_{ON}+C_{OFF}))$. In the design, F_{SW} = 4.8 MHz and C_{ON}/C_{OFF} = 3, resulting in a T_{OFF} period of approximately 50ns. Figure. 3.23 depicts the simplified circuit during CCM. By adding an 8 μA bias to the tail current bias, I attain a reaction time lower than 50 ns across all corners during CCM.

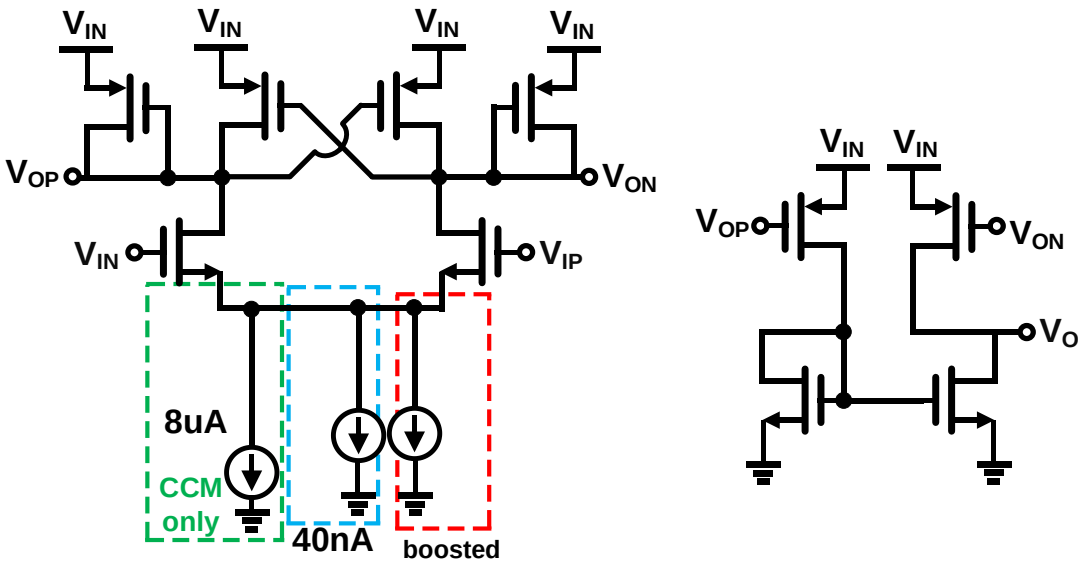

Fig. 3.25 The simplified comparator circuit during CCM.

To reach the target of a total quiescent current of 200 nA during DCM, I must minimize the averaging current. As shown in Fig 3.26, the 8 μA bias used in CCM is not utilized during DCM and there is only a single 40 nA tail current bias for the entire

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circuit. The current boost loop remains active during DCM to enhance the long reaction time without significantly increasing the average current.

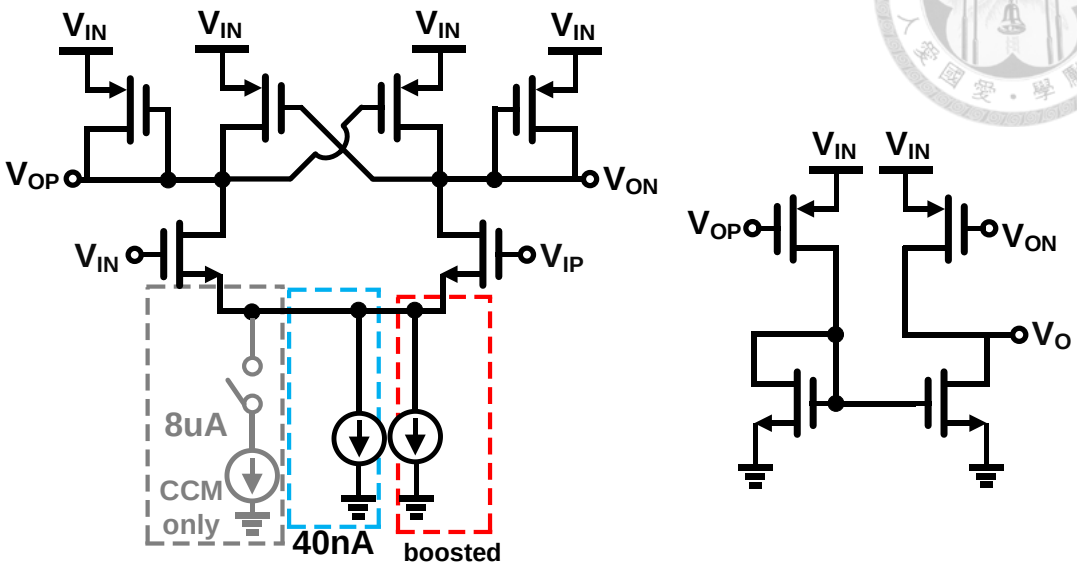

Fig. 3.26 The simplified comparator circuit during DCM.

The current boost biasing loop is illustrated in Fig. 3.27. For most comparators, including the dynamic comparator, there is typically a tradeoff between biasing current and reaction time (bandwidth). More power consumption leads to faster reaction times. However, the biasing current does not have to be fixed, and the comparator only operates when the input voltages (VIN and VIP) are near each other. Hence, I introduce the current boost biasing loop, which is solely active during transitions, and adds an additional bias current that only marginally increases the average current in most scenarios.

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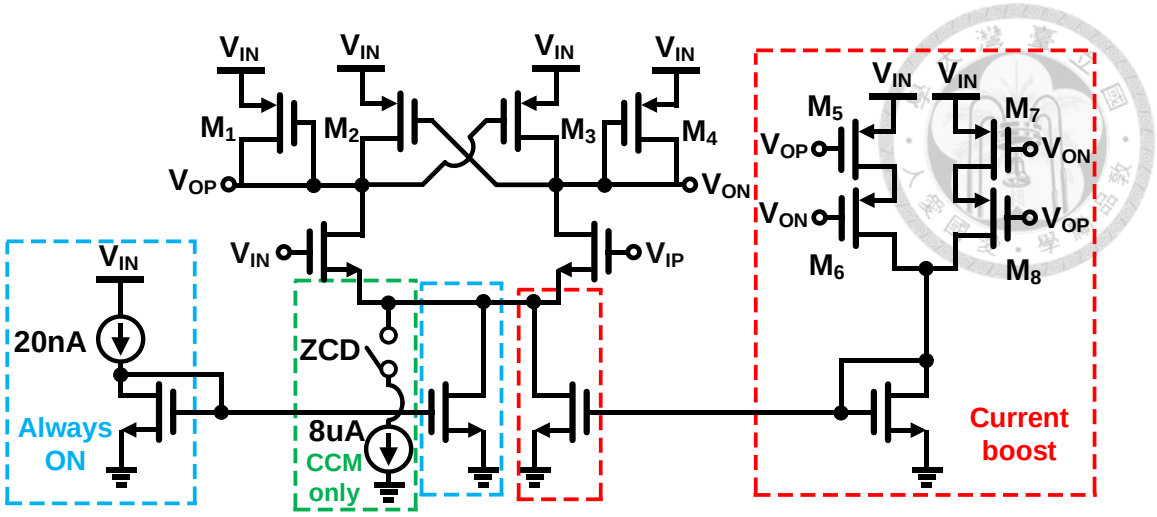

Fig. 3.27 The simplified comparator circuit for current boost biasing loop.

Presented here in Fig. 3.28 and Fig. 3.29 are the operation diagrams of the current boost loop for CCM and DCM, respectively. Normally, signals VOP and VON have the opposite voltage level as V_{IN} or GND. The current boost circuit (M_5-M_8) acts as switches, which remain off due to the opposite voltage polarity between V_{OP} and V_{ON}. During a transition period, when V_{IN} reaches V_{IP}, V_{OP} and V_{ON} also converge, rendering them non-digital signals. Consequently, the high-side transistors (M_1-M_4) switch to current bias when V_{OP} equals V_{ON}. V_{OP} and V_{ON} become the voltage bias of the temporary current mirror (M1-M4), while the current boost circuit (M_5-M_8) becomes a current source, and the increased current value is proportional to the original tail current. The subsequent current mirrors replicate this current to the original loop and add to the tail current. This produces a temporary increase in the operating current during the transition, resulting in a considerably shortened reaction time, with negligible overall average power consumption increase.

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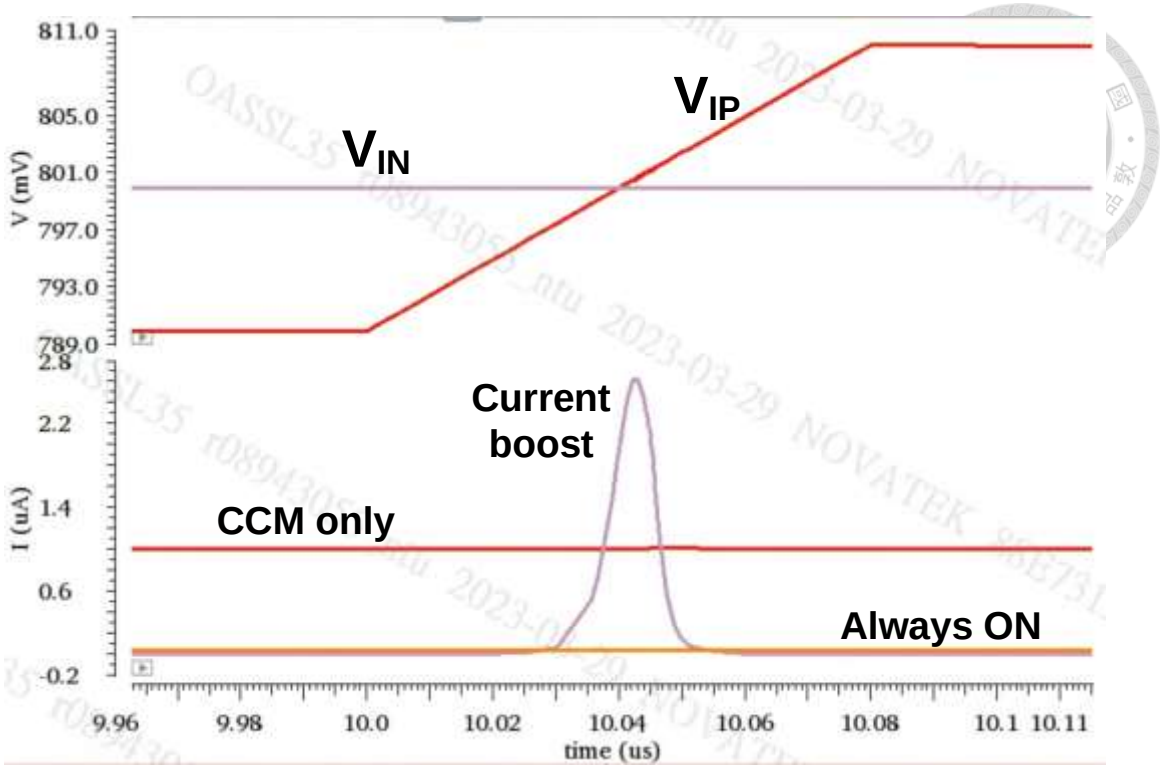

Fig. 3.28 Operation diagrams of the current boost loop for CCM.

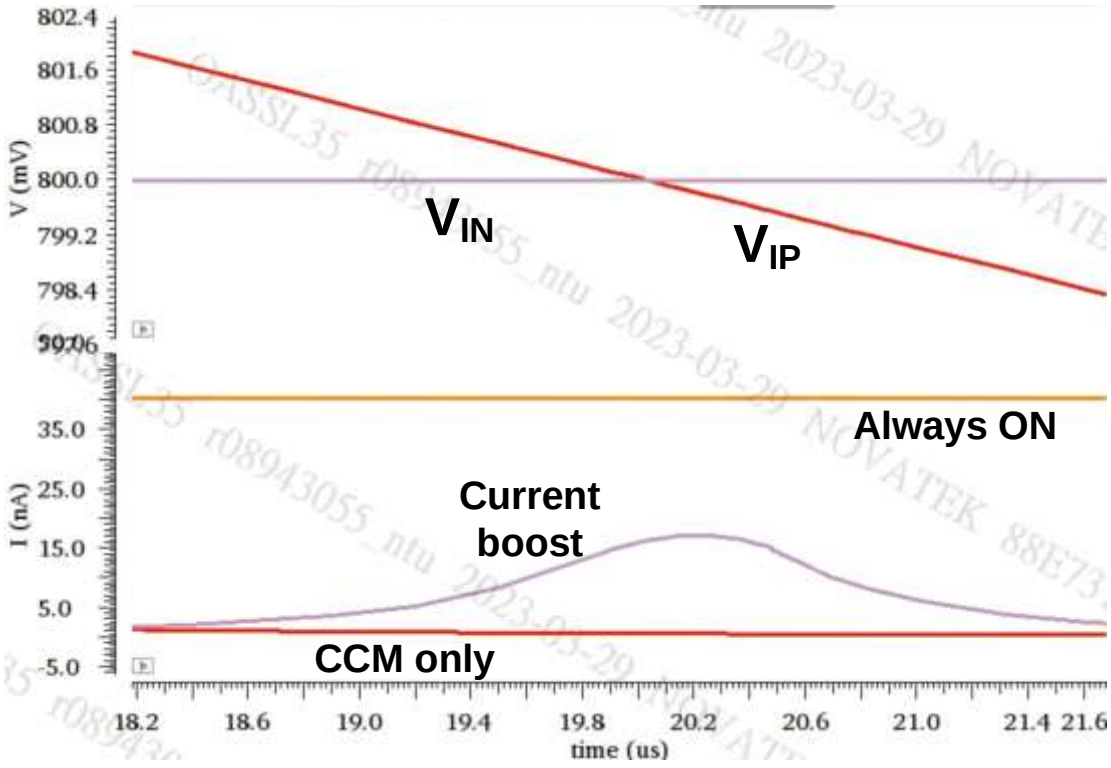

Fig. 3.29 Operation diagrams of the current boost loop for DCM.

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In conclusion, I introduce a comparator that conforms to a wide loading range design with three specific biasing loops during CCM and DCM. I achieve both low reaction time in CCM and low quiescent current in DCM. Furthermore, I have further reduced the reaction time during both CCM and DCM with the current boost biasing loop. The design resulted in improved performance, as demonstrated by the transistor-level architecture presented in Fig. 3.24

Chapter 4 Simulations and Measurements

4.1 Chip Overview

Fig. 4.1 depicts the chip layout photograph, while Fig. 4.2 displays the die photograph of the proposed 200 nA quiescent current N-FinFET power stage buck converter with passive ramp on-off-time control, which was fabricated in TSMC 12nm and occupies only 0.36mm2, including the power stage and pads. Additionally, there are four capacitors in parallel off-chip debouncing components on the substrate.

Regarding the power supply, a single power supply can be used to connect VDDP and VDDA, with VDDP supplying power to the power stage and VDDA supplying power to the controller. However, to obtain more precise experimental data, VDDP and VDDA are connected to different power supplies to separately record their power consumption.

There are three types of pins in the chip, control pins, digital outputs, and analog outputs. The pin diagram is shown in Fig. 4.3 – Fig. 4.4 and Table 4.1 shows the PIN configuration.

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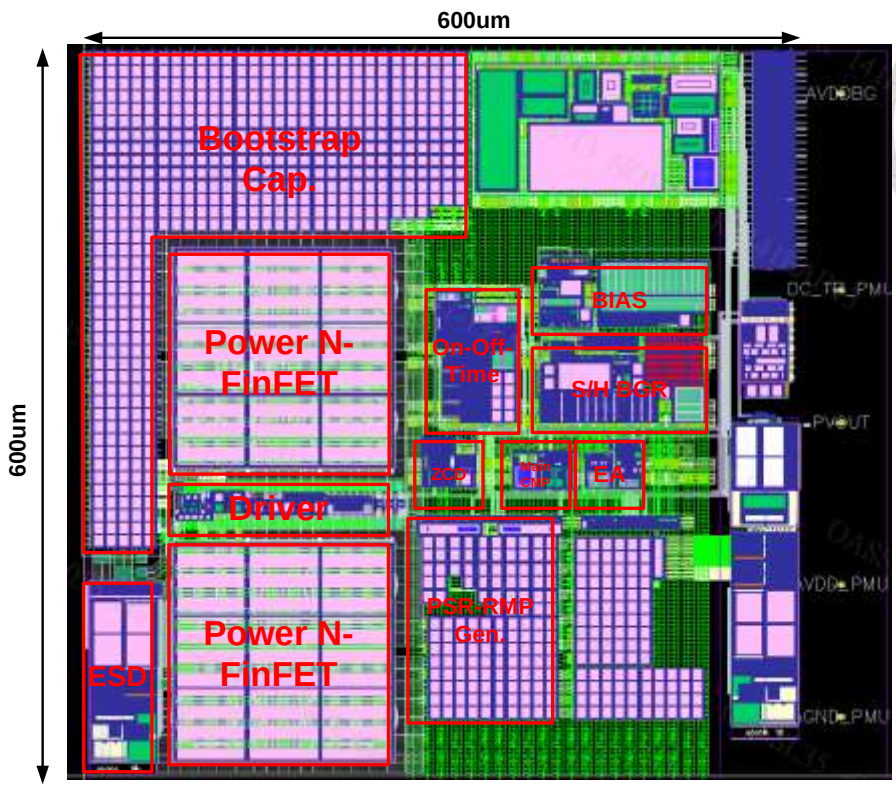

Fig. 4.1 Chip layout photograph

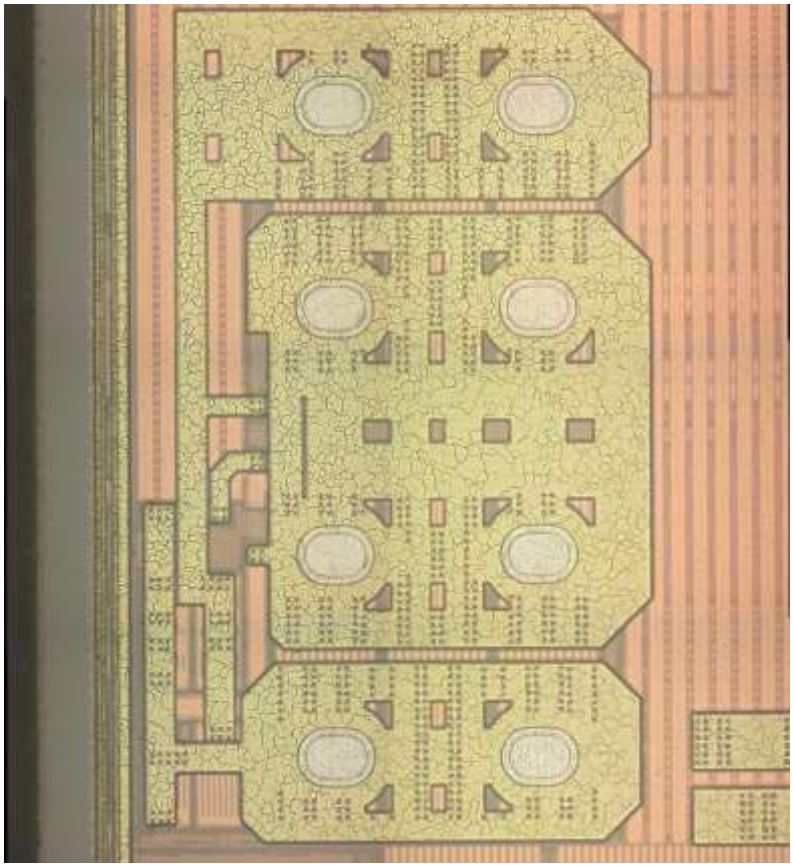

Fig. 4.2 Die photograph

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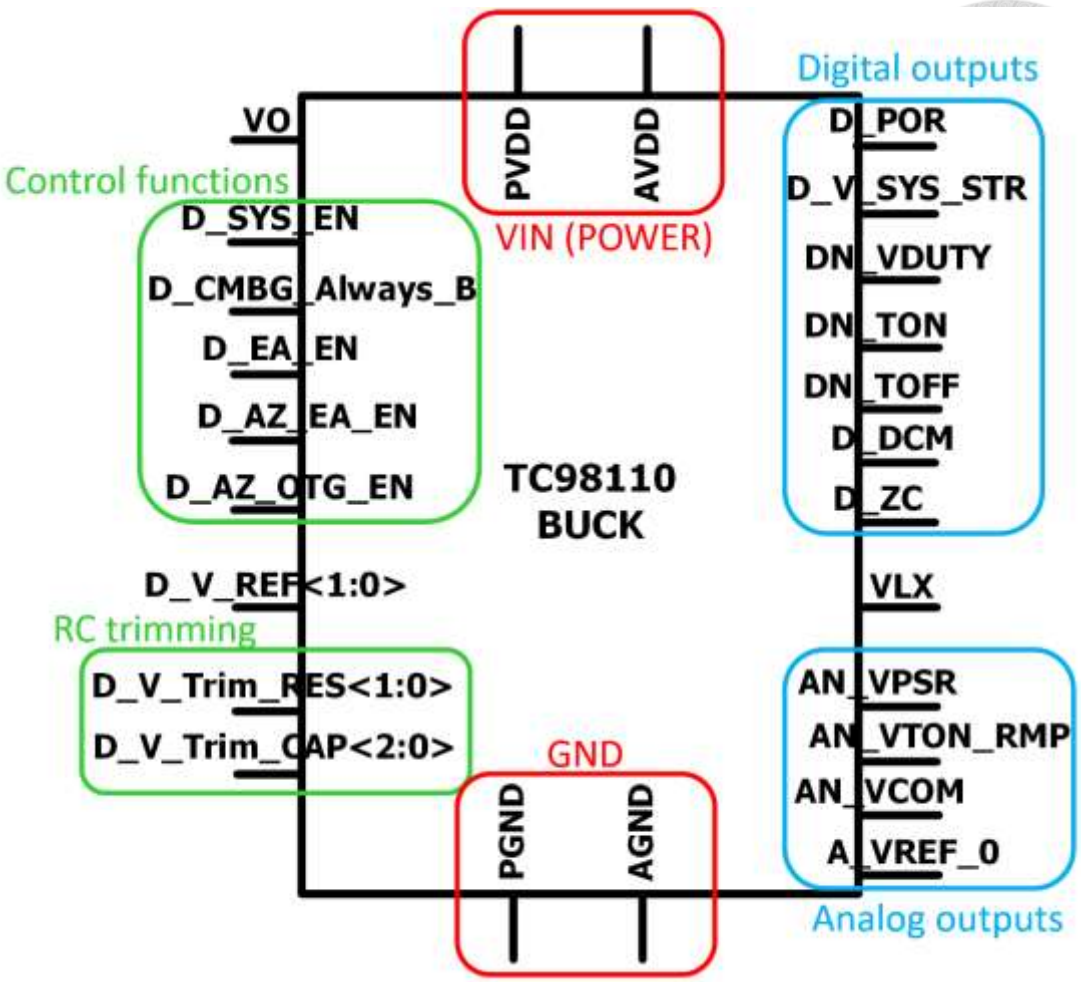

Fig. 4.3 Pin diagram (1)

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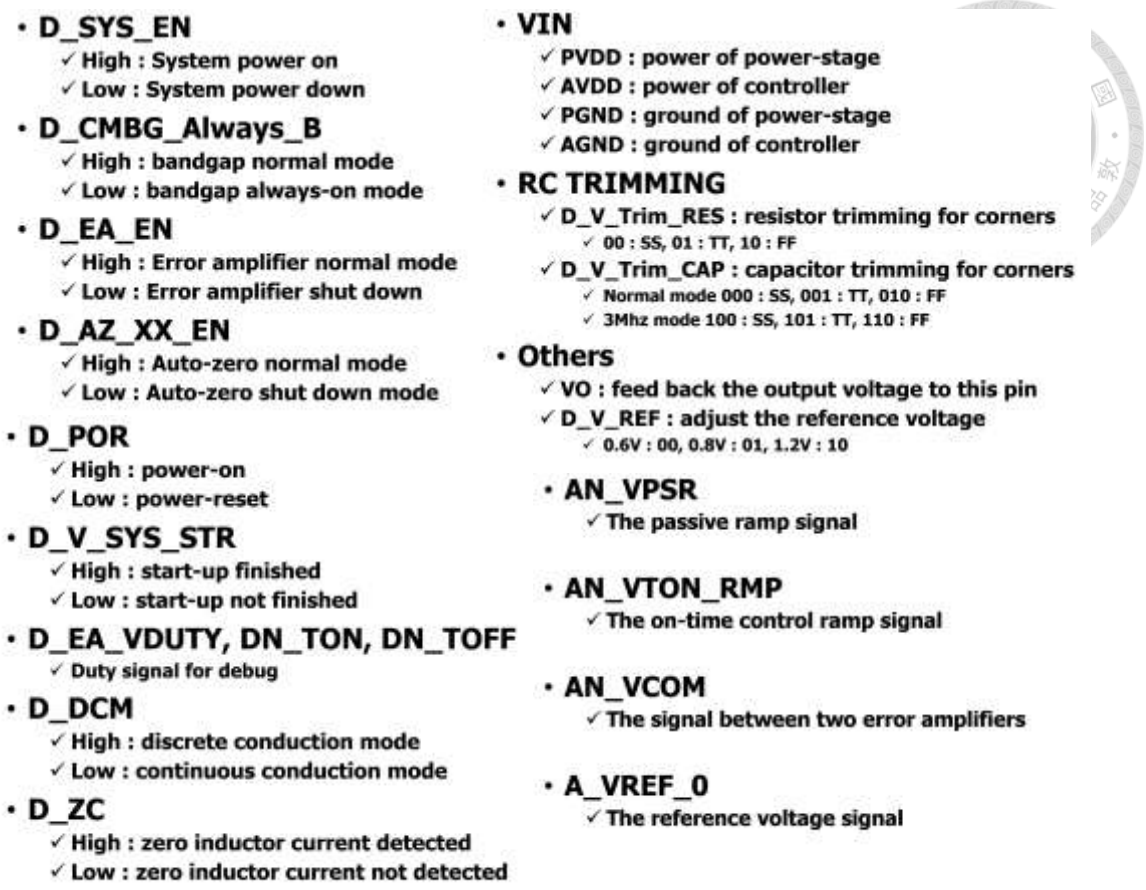

Fig. 4.4 Pin diagram (2)

TABLE 4.1 PIN configuration

PIN	Name	PIN	Name	PIN	Name
PIN 1	PVDD	**PIN 10**	D_AZ_OTG_EN	**PIN 19**	D_V_SYS_STR
PIN 2	AVDD	**PIN 11**	D_V_Trim_RES<0>	**PIN 20**	DN_VDUTY
PIN 3	PGND	**PIN 12**	D_V_Trim_RES<1>	**PIN 21**	DN_TON
PIN 4	AGND	**PIN 13**	D_V_Trim_CAP<0>	**PIN 22**	DN_TOFF
PIN 5	VO	**PIN 14**	D_V_Trim_CAP<1>	**PIN 23**	D_DCM
PIN 6	D_SYS_EN	**PIN 15**	D_V_Trim_CAP<2>	**PIN 24**	D_ZC
PIN 7	D_CMBG_Always_B	**PIN 16**	D_V_REF<0>	**PIN 25**	VLX
PIN 8	D_EA_EN	**PIN 17**	D_V_REF<1>		
PIN 9	D_AZ_EA_EN	**PIN 18**	D_POR		

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4.2 Simulation and Measurement result

Fig. 4.5 shows the V_{IN}: 1.8 V to V_O: 0.8 V efficiency simulation and measurement result with C_O = 4.7 µF, I_L = 100 nH, and I_{LOAD} from 1 µA to 1.5 A in the TT corner. The boundary of CCM and DCM is around I_{LOAD} = 400mA. Quiescent current is 200nA. The decrease in efficiency observed between simulation and measurement can be attributed to the presence of parasitic resistance in the package and PCB bonding. The estimated value of this parasitic resistance is 200 milliohms. The subsequent analysis will eliminate the impact of the parasitic resistance on the measurement results, enabling a fresh comparison with the simulation results.

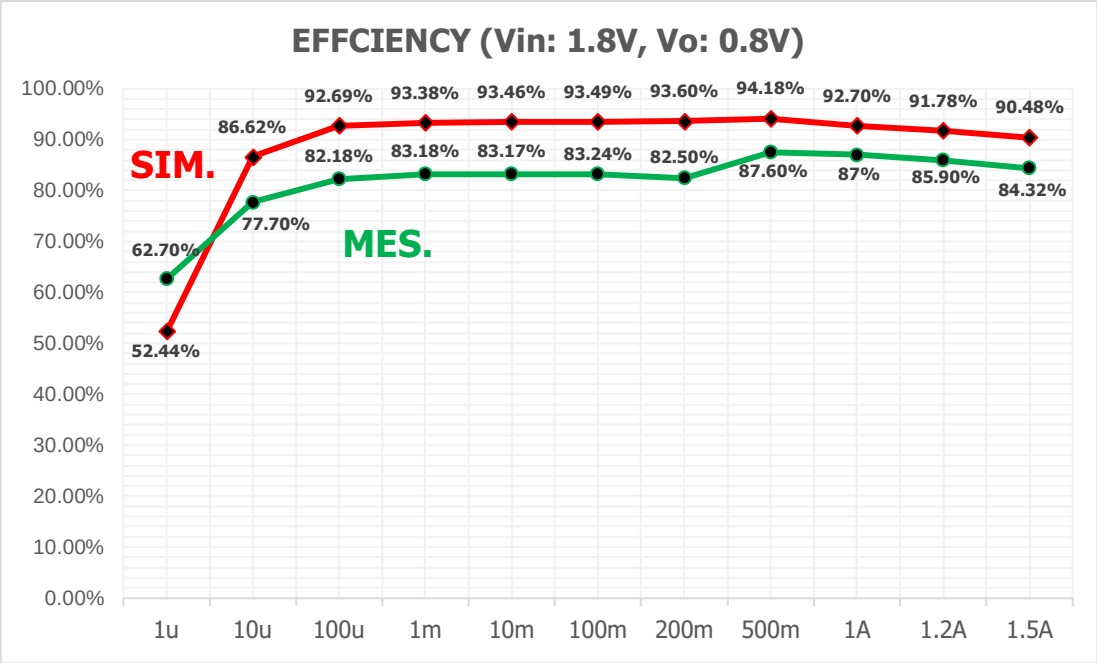

Fig. 4.5 Efficiency of simulations and measurements with V_{IN}: 1.8 V to V_O: 0.8 V and I_{LOAD} from 1 µA to 1.5 A

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Fig. 4.6 shows the V_{IN}: 1.6 V to V_O: 1.2 V efficiency simulation and measurement result with C_O = 4.7 µF, I_L = 100 nH, and I_{LOAD} from 1 µA to 1.5A in the TT corner. The boundary of CCM and DCM is around I_{LOAD} = 400mA. Quiescent current is 200nA. The decrease in efficiency observed between simulation and measurement can be attributed to the presence of parasitic resistance in the package and PCB bonding. The estimated value of this parasitic resistance is 200 milliohms. The subsequent analysis will eliminate the impact of the parasitic resistance on the measurement results, enabling a fresh comparison with the simulation results.

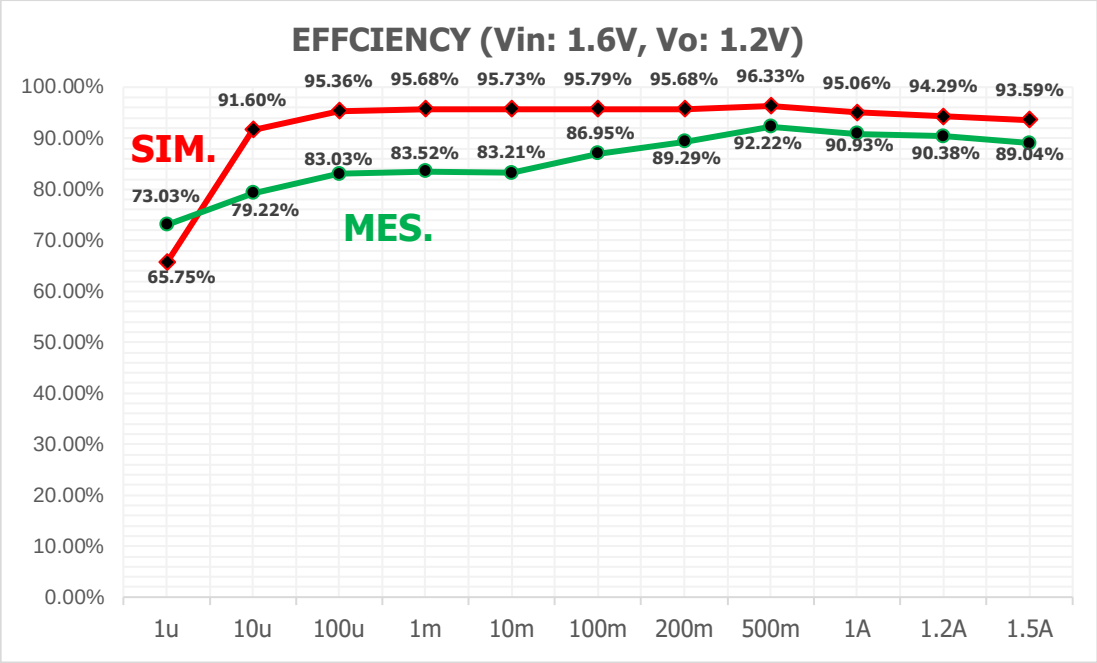

Fig. 4.6 Efficiency of simulations and measurements with V_{IN}: 1.6 V to V_O: 1.2 V and I_{LOAD} from 1 µA to 1.5 A

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Fig. 4.7 shows the V_{IN}: 2 V to V_O: 0.6 V efficiency simulation and measurement result with C_O = 4.7 µF, I_L = 100 nH, and I_{LOAD} from 1 µA to 1.5 A in the TT corner. The boundary of CCM and DCM is around I_{LOAD} = 400mA. Quiescent current is 430nA. The decrease in efficiency observed between simulation and measurement can be attributed to the presence of parasitic resistance in the package and PCB bonding. The estimated value of this parasitic resistance is 200 milliohms. The subsequent analysis will eliminate the impact of the parasitic resistance on the measurement results, enabling a fresh comparison with the simulation results.

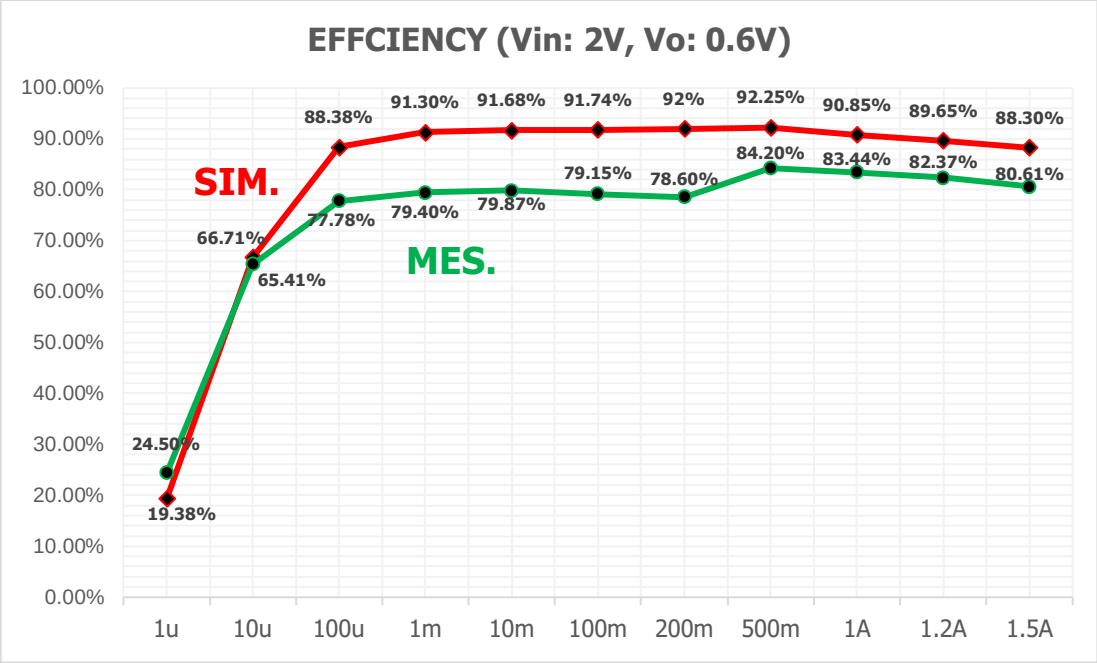

Fig. 4.7 Efficiency of simulations and measurements with V_{IN}: 2 V to V_O: 0.6 V and I_{LOAD} from 1 µA to 1.5 A

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Fig. 4.8 - 4.10 show the new efficiency comparisons between simulation and measurement results without the 200 milliohms parasitic resistance.

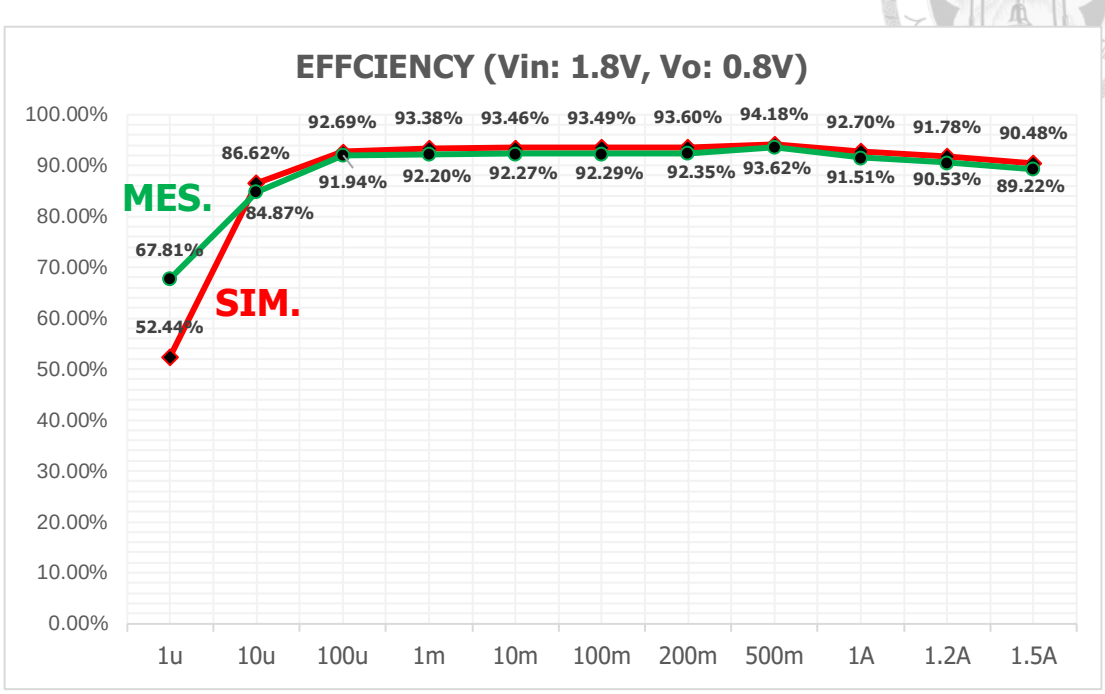

Fig. 4.8 The new efficiency of simulations and measurements with V_{IN}: 1.8 V to V_O: 0.8 V and I_{LOAD} from 1 μA to 1.5 A

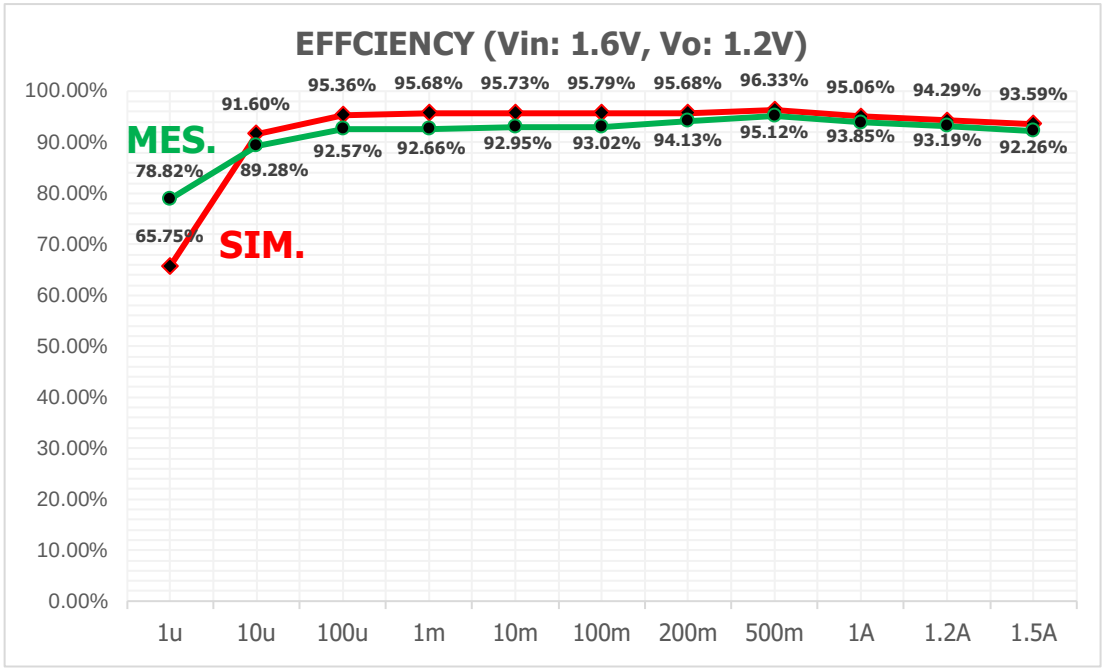

Fig. 4.9 The new efficiency of simulations and measurements with V_{IN}: 1.6 V to V_O: 1.2 V and I_{LOAD} from 1 μA to 1.5 A

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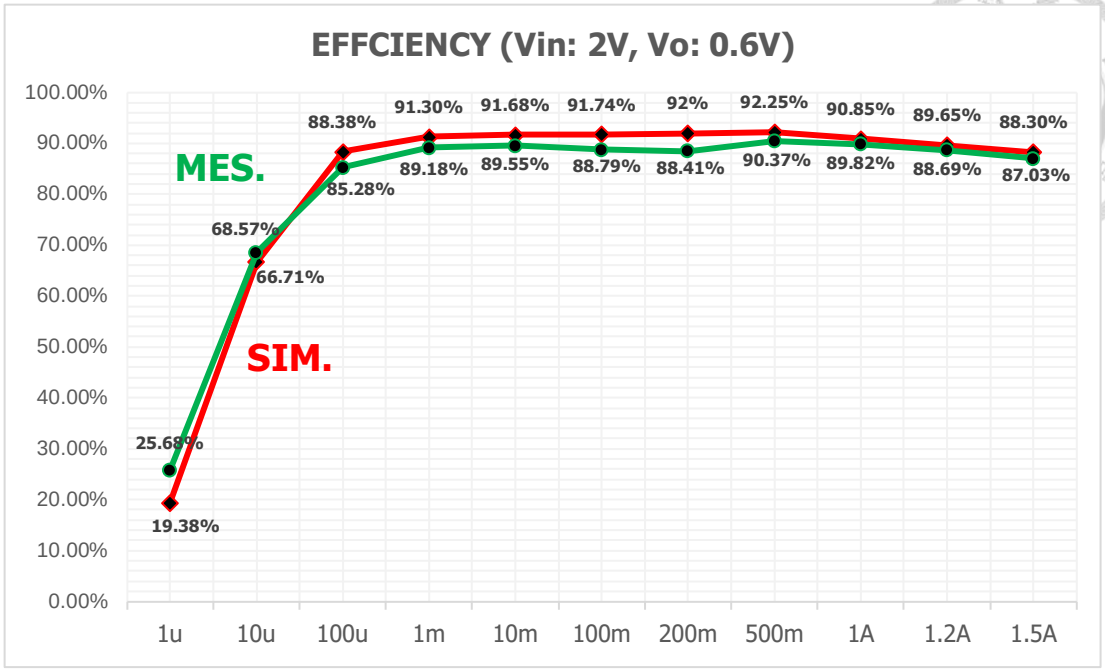

Fig. 4.10 The new efficiency of simulations and measurements with V_{IN}: 1.6 V to V_O: 1.2 V and I_{LOAD} from 1 μA to 1.5 A

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Fig. 4.11 shows the load transient simulation result with C_O = 4.7 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V and I_{LOAD} from 1 µA to 500 mA. As the current loading I_{LOAD} increases from 1 µA to 500 mA, it draws current from the output capacitor C_O causing a drop in the output voltage V_O before the inductor current I_L can respond. There are several factors that affect the speed at which I_L can catch up with I_{LOAD}. In the design, the primary factor is the delay of the main comparator. In DCM, I have significantly reduced the biasing current of the main comparator. As a result, it takes a considerable amount of time for the comparator to respond in DCM, as opposed to CCM. This delay leads to a longer I_L response time in DCM compared to CCM.

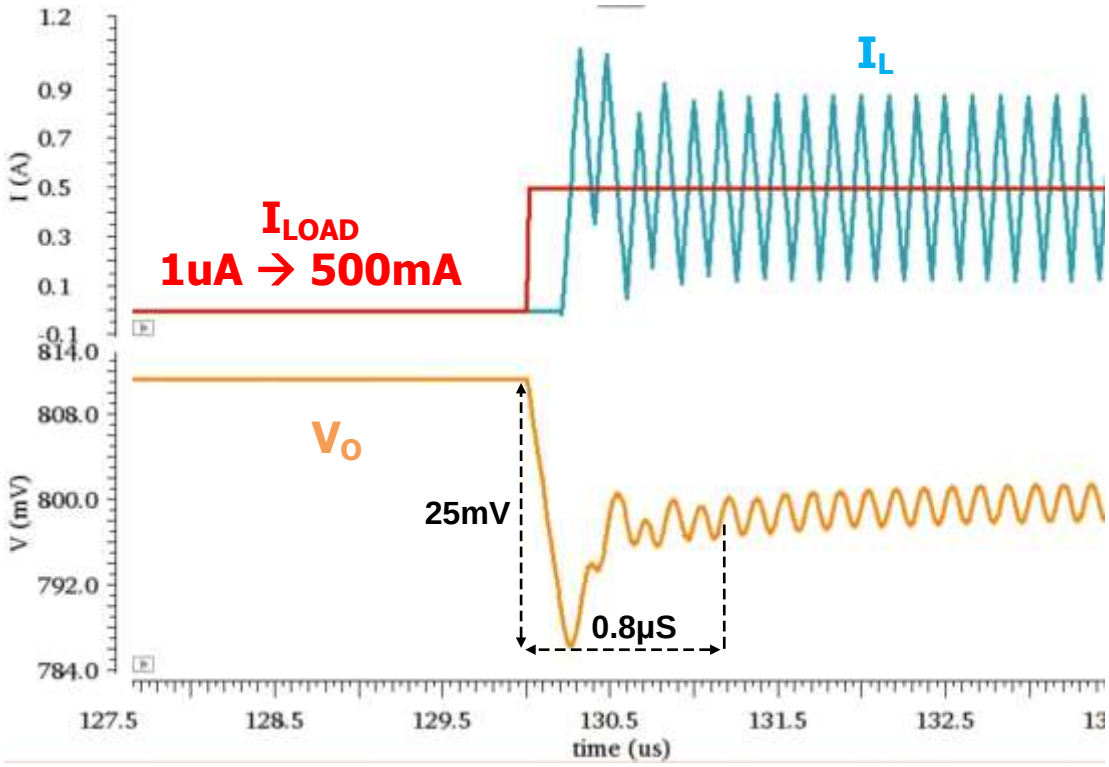

Fig. 4.11 Load transient simulation result with C_O = 4.7 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V and I_{LOAD} from 1 µA to 500 mA

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Fig. 4.12 shows the load transient simulation result with C_O = 4.7 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V and I_{LOAD} from 500 mA to 1 µA. As the current loading I_{LOAD} decreases from 500 mA to 1 µA, it charges current to the output capacitor C_O causing a rise in the output voltage V_O before the inductor current I_L can respond. There are several factors that affect the speed at which I_L can catch up with I_{LOAD}. In the design, the primary factor is the delay of the main comparator. In CCM, I have significantly increased the biasing current of the main comparator. As a result, it takes a short amount of time for the comparator to respond in CCM, as opposed to DCM. This delay leads to a shorter I_L response time in CCM compared to DCM.

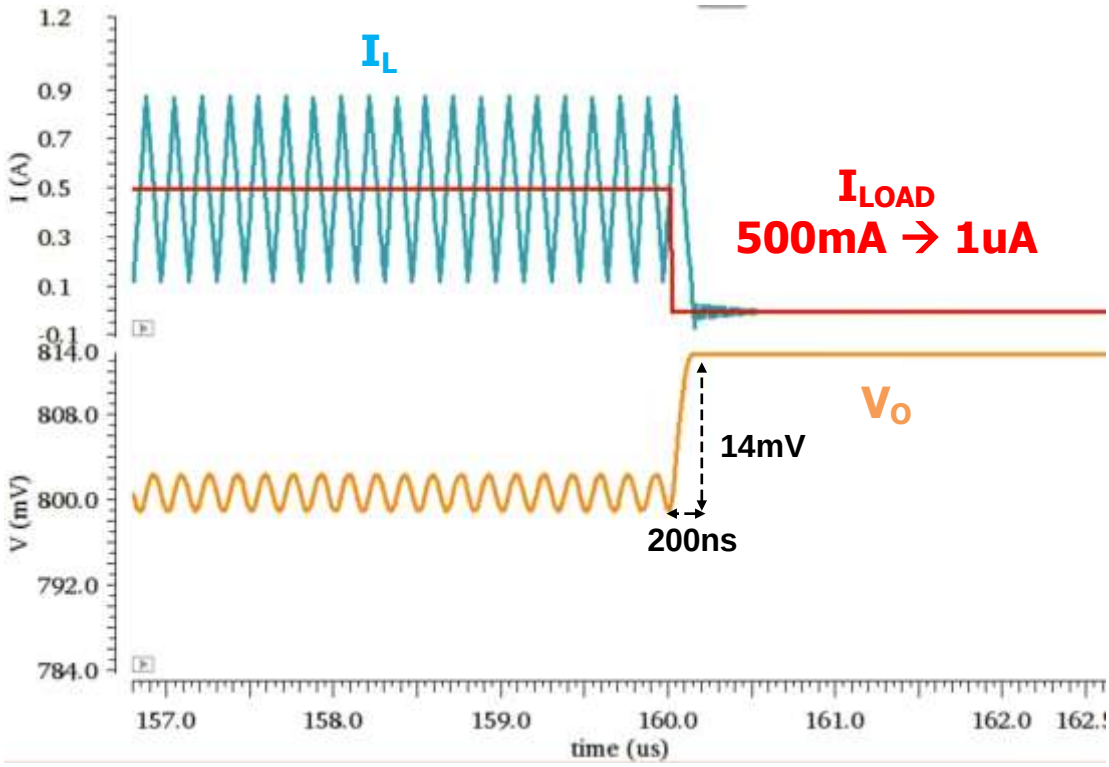

Fig. 4.12 Load transient simulation result with C_O = 4.7 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V and I_{LOAD} from 500 mA to 1 µA

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Fig. 4.13 shows the load transient simulation result with C_O = 4.7 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V and I_{LOAD} from 1 µA to 1A. As the current loading I_{LOAD} increases from 1 µA to 1 A, it draws current from the output capacitor C_O causing a drop in the output voltage V_O before the inductor current I_L can respond. There are several factors that affect the speed at which I_L can catch up with I_{LOAD}. In the design, the primary factor is the delay of the main comparator. In DCM, I have significantly reduced the biasing current of the main comparator. As a result, it takes a considerable amount of time for the comparator to respond in DCM, as opposed to CCM. This delay leads to a longer I_L response time in DCM compared to CCM.

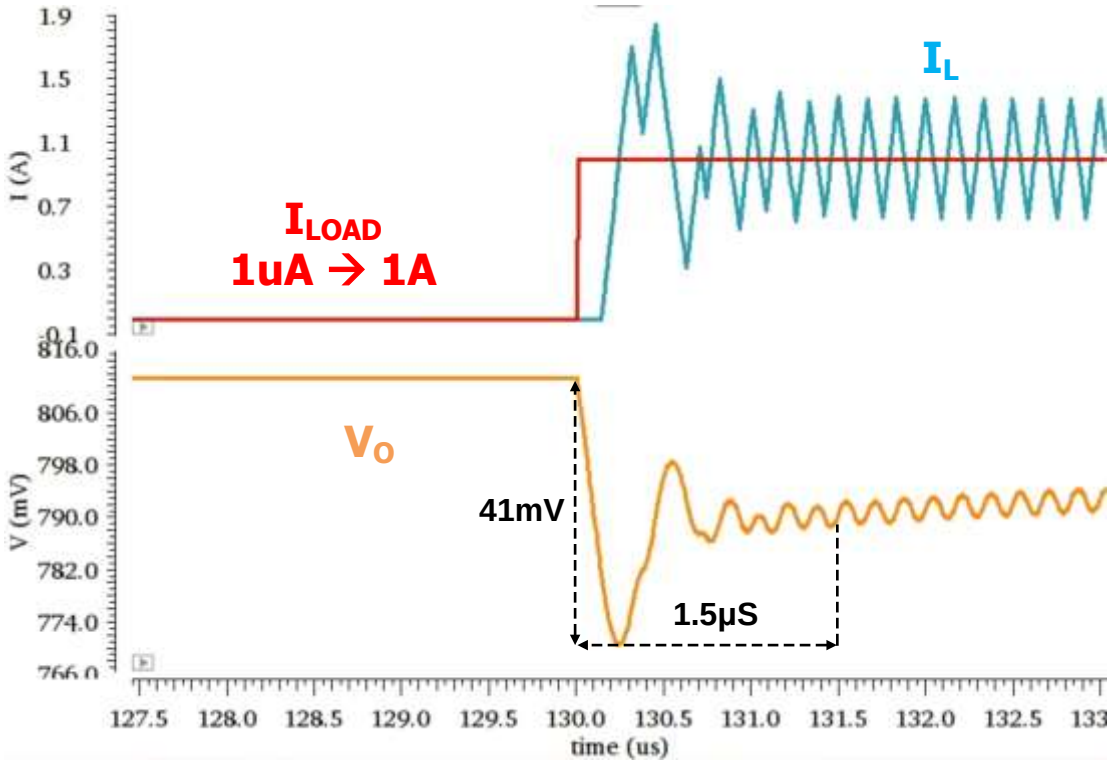

Fig. 4.13 Load transient simulation result with C_O = 4.7 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V and I_{LOAD} from 1 µA to 1 A

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Fig. 4.14 shows the load transient simulation result with C_O = 4.7 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V, and I_{LOAD} from 1 A to 1 µA. As the current loading I_{LOAD} decreases from 1 A to 1 µA, it charges current to the output capacitor C_O causing a rise in the output voltage V_O before the inductor current I_L can respond. There are several factors that affect the speed at which I_L can catch up with I_{LOAD}. In the design, the primary factor is the delay of the main comparator. In CCM, I have significantly increased the biasing current of the main comparator. As a result, it takes a short amount of time for the comparator to respond in CCM, as opposed to DCM. This delay leads to a shorter I_L response time in CCM compared to DCM.

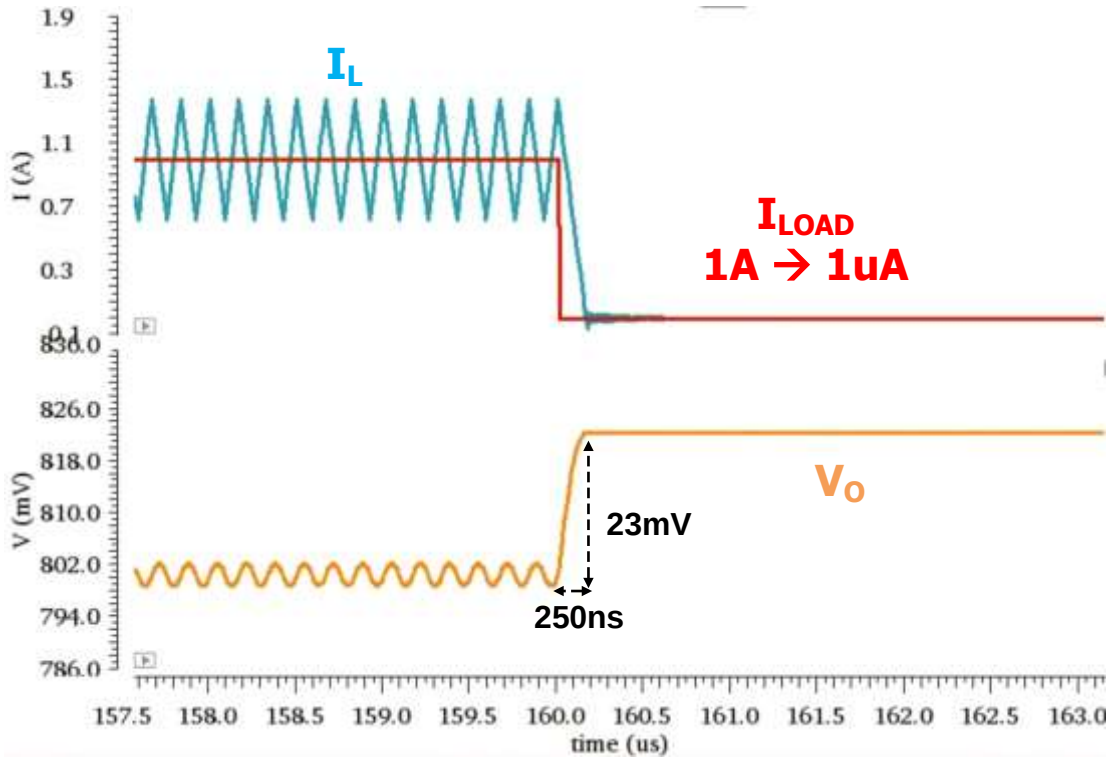

Fig. 4.14 Load transient simulation result with C_O = 4.7 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V and I_{LOAD} from 1 A to 1 µA

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Fig. 4.15 shows the load transient measurement result with C_O = 14.1 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V, and I_{LOAD} from 1 µA to 500 mA to 1 µA. The measurement result shows a 41 mV undershoot with a 1 µs settling time and a 20 mV overshoot with a 380 ns settling time. The larger overshoot is a direct consequence of the longer delay in the comparator. Despite the efforts to improve the comparator's speed during CCM by increasing its power consumption, its operation during DCM remains unaltered due to the requirement to maintain a quiescent current goal of 200 nA.

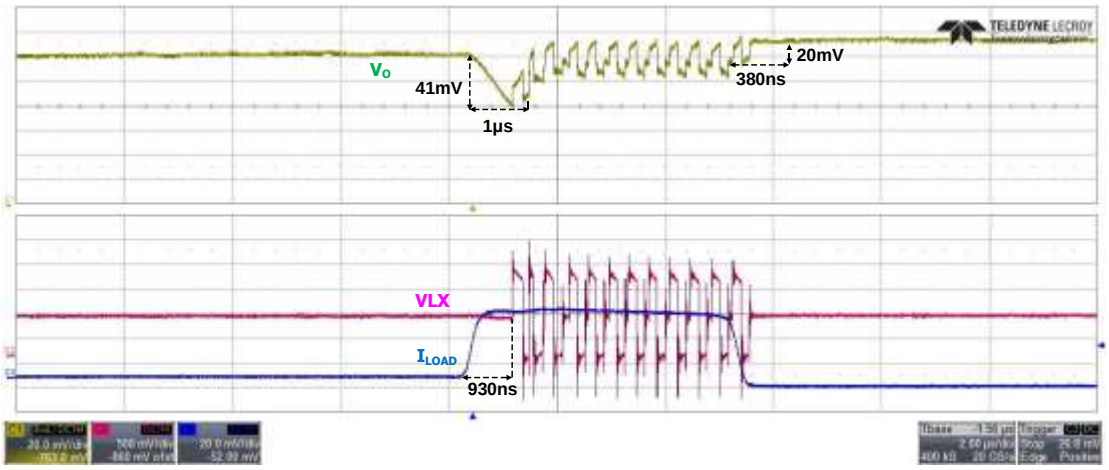

Fig. 4.15 Load transient measurement result with C_O = 14.1 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V, and I_{LOAD} from 1 µA to 500 mA to 1 µA.

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Fig. 4.16 shows the load transient measurement result with C_O = 14.1 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V, and I_{LOAD} from 1 µA to 1 A to 1 µA. The measurement result shows a 78.4 mV undershoot with a 1.5 µs settling time and a 40 mV overshoot with a 500 ns settling time. The larger overshoot is a direct consequence of the longer delay in the comparator. Despite the efforts to improve the comparator's speed during CCM by increasing its power consumption, its operation during DCM remains unaltered due to the requirement to maintain a quiescent current goal of 200 nA.

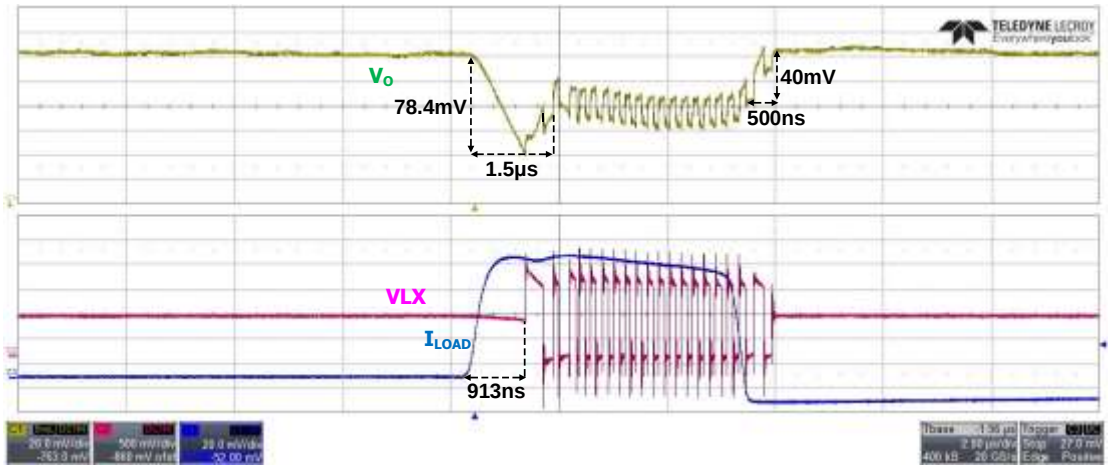

Fig. 4.16 Load transient measurement result with C_O = 14.1 µF, I_L = 100 nH, V_{IN}: 1.8 V to V_O: 0.8 V, and I_{LOAD} from 1 µA to 1 A to 1 µA.

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Fig. 4.17 shows the seamless load transition simulation result of V_{IN}: 1.8 V to V_O: 0.8 V and I_{LOAD} from 1 μA to 1.5 A to 1 μA. As seen in Fig 4.14. There are no subharmonic or any other form of oscillations present in any static loads within the design. Furthermore, there are no subharmonic or any other form of oscillations even in the boundary condition of CCM and DCM in the design.

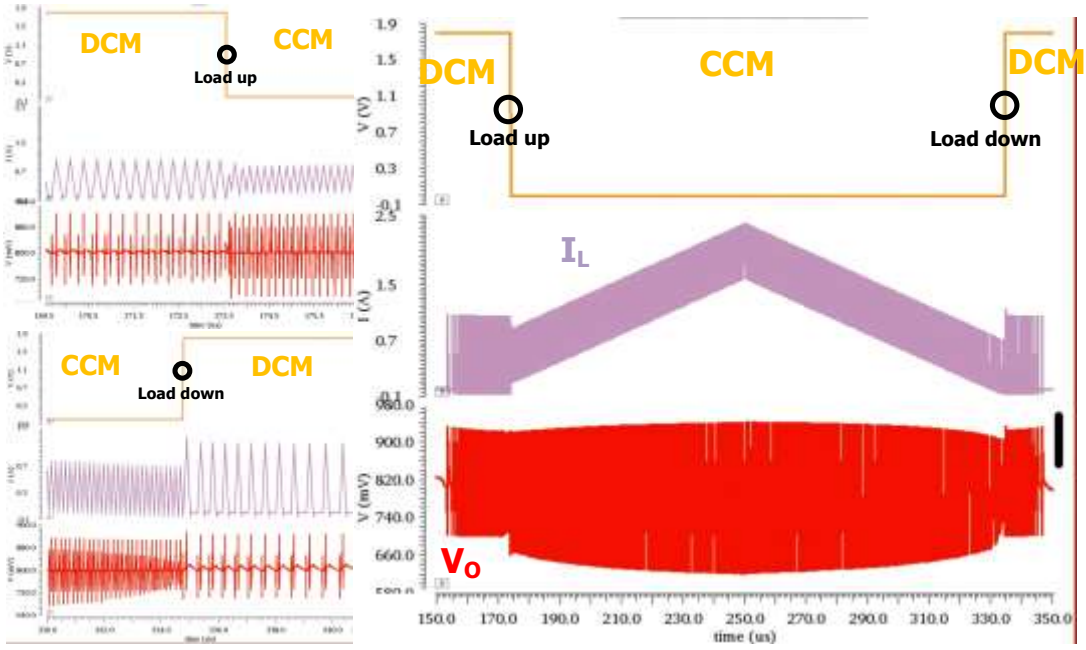

Fig. 4.17 The simulation result of V_{IN}: 1.8 V to V_O: 0.8 V and I_{LOAD} from 1 μA to 1.5 A to 1 μA.

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Chapter 5 Conclusions and Future works

5.1 Conclusions

The simulated efficiency from 1 μA to 2 A is shown in Fig. 10. The efficiency is larger than 90% from 10 μA to 2A, that is precisely meets the design target. The quiescent current breakdown is also shown in Fig. 10. The main comparator contributes 62 nA, which dominates the efficiency loss at ultra-light-load. The bias current and bandgap reference consume 53 nA and 33 nA, respectively. Almost all quiescent current of these two circuits is contributed by the leakage current. All the simulation is at a junction temperature of 60 degrees. The comparison table is shown in TABLE 5.1. The design performs the widest loading dynamic range larger than 90% efficiency, which is 10 μA to 2A. As a result, this design achieves the best FoM2 [6][7]. The transient response is superior to all the other low quiescent current designs [1][2][4][5], and close to the fast transient design [3]. In conclusion, this design breaks the design trade-off between low quiescent current and fast dynamic response.

This thesis presents a 200 nA quiescent current, 4.8 MHz FSW, all N-FinFET power stage buck converter with passive ramp (PSR) on-off-time control. The proposed design achieves the widest loading current dynamic range of efficiency > 90% without sacrificing the load transient response. So, it is suitable for the present advance SoC. The co-package designed all N-FinFET power stage ensures a 35 mOhm ultra-low Rdson and low leakage. The control scheme combines all the benefits of conventional on-time control and off-time control. A load transient response simulation achieves a 23 mV/ 17 mV undershoot/overshoot voltage with 800 ns settling time with a 1 μA to 500 mA loading step.

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TABLE 5.1 Comparison table

			JSSC12 [1]	JSSC18 [2]	JSSC20 [3]	TCAS-I21 [4]	TPEL21 [5]	This work
Technology			250nm CMOS	130nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS	12nm FinFET
Control Scheme			Dynamic-On-Off-Time	COT	DAB Hysteretic	Tri-Mode AOT	AOT	PSR-COOT
V_O (V)/V_{IN} (V)			1 / 1.2 – 2.5	1.2 / 1.8 – 3.3	0.5 – 2.5 / 3 – 5	1.6 / 2.2 – 4.7	1.8 / 2.1 – 5.5	0.6 – 1.2 / 1.6 – 2
F_{SW}			Dynamic	Dynamic	10MHz	CCM: 4MHz, DCM: Dynamic	CCM: 2MHz, DCM: Dynamic	CCM: 4.8MHz, DCM: Dynamic
L_S (μH) / C_O (μF)			3.3 / 4.7	18 / 0.056	0.2 / 2	4.7 / 4.7	2.2 / 10	0.24 / 4.7
Chip Area (mm²)			0.39	0.14	0.175	0.55	1.092	0.36
$I_{O,MIN}$ - $I_{O,MAX}$			1μA - 50mA	0.1μA - 2.65mA	1mA – 1A	1μA – 100mA	1μA – 0.3A	1μA – 2A
I_q (μA)			0.181	0.44	N.R.	0.49	0.24	0.2
Peak Efficiency			95%	91.8%	91%	92.1%	95.8%	95%
Efficiency > 90% Loading Range			20μA – 50mA 2500 X	100μA – 2.65mA 26.5 X	0.1A – 0.4A 4 X	4mA – 40mA 10 X	10μA – 300mA 30000 X	10μA – 2A 200000 X
Load-Transient	$\Delta I_{O,MAX}$ (A)		200μA → 10mA	100nA → 2.65mA	0 → 1A	5uA → 8mA	10mA → 300mA	1μA → 0.5A
	Step-Up	ΔV_O (mV) / Δt_s (μs)	N.R.	20 / 0.6	31 / 0.247	48 / 8	50 / 30	23 / 0.8
	Step-Down	ΔV_O (mV) / Δt_s (μs)	N.R.	20 / 0.6	60 / 0.387	26 / 2.6	48 / 24	17 / 0.2
FoM_1 (μs/A²-%) [6]			N.R.	967	0.0027	108.6	3.6	0.0072
FoM_2(pA) [4]			4.16	26.8	N.R.	6.5	0.89	0.11

+: $FoM_1 = \frac{\Delta t_{s,up}}{Peak-Efficiency \times \Delta I_{O,MAX} \times I_{O,MAX}}$, ++: $FoM_2 = \frac{I_{O,\min}}{I_{O,\max}} \times \frac{I_q}{Eff.@10\mu A}$; smaller values are better

N.R. = Not report

5.2 Future works

1. The floor plan of the pads is arranged too closely, resulting in a limited reduction of the parasite resistance caused by the via issue on the substrate. Nevertheless, increasing the distance between the pads can help decrease the parasite resistance on the main power loop.

2. The fabrication of the 12nm FinFET is both expensive and difficult to obtain. Despite its advantages in certain analog characteristics, it is not a cost-efficient option for developing a power converter. However, based on the ideas presented in this thesis, it is feasible to implement a similar system using the 0.18 μm process, which is more affordable and accessible.

3. The detailed derivation of the on-off-time control with the DC cancellation loop is not included in this thesis. The reason for this omission is due to the inherent challenges

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and complexities involved, which surpass my current capabilities. Nonetheless, including the detailed derivation of the transfer function would lend greater credibility to the overall structure.

4. Measurement can only be done in Novatek Microelectronics Corporation. A detailed and further measurement result would be done and complemented.

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