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應用於下世代生醫檢測與邏輯之互補式金屬氧化物半導體整合微/奈米流道細胞/電化學感測及互補式場效電晶體

CMOS-integrated Cellular/Electrochemical Micro/nanofluidics and CFET (Complementary FET) for Next-generation Biosensing and Logic

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中文摘要

本論文包含三個部分：用於細胞檢測的 CMOS 嵌入式微流道系統、用於電化學感測的 CMOS 晶片上電極開發以及 CFET 元件的製作。

首先，我們提出了一種新穎的 CMOS 嵌入式微流道平台，該平台具有晶片上阻抗感測電極和三維微/奈流體學，適用於下一代 POC 診斷設備。該平台採用單步驟後 CMOS 濕刻蝕刻製程，透過去除 CMOS 後端製程走線（BEOL），由金屬來形成中空流體通道。通過提高水力壓力來優化蝕刻過程，從而將蝕刻速率提高了 10 倍。為了研究各種流體通道的可行性，我們設計了多種具有不同功能的通道幾何形狀，對應日益增長的微流道技術與元件。為了晶片上電極進行阻抗感測，我們探索了各種策略，並提出了“通孔”電極，在保持檢測能力的同時亦維持其完整性。我們還研究了平台的長期穩定性，並展示了使用不同濃度離子溶液進行阻抗感測的有效性。此外，我們還設計了一個跨阻放大器，使用串接電流再利用放大器作為類比前端電路，製作了我們提出的高度 CMOS 整合的微流道系統的原型。

其次，我們展示了用於電化學感測的 CMOS 片上電極的開發。我們採用化學鍍膜和蒸鍍沉積的過程在鋁墊層上製作金層。通過這樣的技術開發，我們成功地將微電極陣列與 CMOS 晶片整合。為了驗證我們感測電極的功能，我們使用卡那霉素之適體進行分子感測。結果與商業電極的結果相似，因此可證明其功能。

最後，我們介紹了一種新的製程技術，用於實現 CFET 結構。我們採用薄膜轉移技術來製作堆疊通道結構，無需進行複雜的磊晶生長和晶圓鍵合。透過使用氦離子束微影技術，我們成功地將元件的關鍵尺寸縮小到 50 奈米以下。

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Abstract

This thesis contains three parts: a CMOS-embedded microfluidics system for cell detection, CMOS-integrated on-chip electrode development for electrochemical sensing, and the fabrication of a CFET device.

To begin with, we present a novel CMOS-embedded microfluidics platform that features on-chip impedance-sensing electrodes, and 3D micro/nanofluidics suitable for next-generation point-of-care (POC) diagnostic devices. The platform uses a single-step post-CMOS wet-etching process to create hollow fluidic channels by removing CMOS back-end-of-line (BEOL) routing metals. The etching process is optimized by improving the etching rate by 10× through hydraulic pressure. To investigate the feasibility of a variety of fluidic channels, we design several channel geometries of different functions, corresponding to more and more emerging microfluidics techniques. To integrate on-chip electrodes for impedance sensing, we explore various strategies and present "via" electrodes that maintain their integrity in the etching process while preserving detection sensitivity. We also investigate the long-term reliability of the platform and demonstrate the efficacy of impedance sensing using ionic solutions of varying strengths. We also design a transimpedance amplifier employing a cascode current-reuse amplifier as an analog front-end circuit to make the prototype of our proposed highly CMOS-integrated microfluidics system.

Secondly, we demonstrate the development of CMOS on-chip electrodes for electrochemical sensing. We adopt the process of both ENIG and evaporator deposition to make a gold layer onto the aluminum pad layer. With such process development, we successfully integrate a microelectrode array with a CMOS chip. To verify the

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functionality of our sensing electrodes, we use kanamycin aptamer to conduct molecular sensing. The results are consistent with the data from commercial electrodes.

In the last, we introduce a novel fabrication technique to realize the CFET architecture. We use membrane transfer techniques to make the stacked channel structure without complex epitaxial growth and wafer bonding. By using helium ion beam lithography, we successfully shrink the device's critical size to below 50nm.

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Chapter 1 Introduction

Complementary metal oxide semiconductor (CMOS) technique has been well-developed and mass-produced for decades. As further development goes on, there are some emerging terms for those advanced technology roadmaps, like “More Moore”, “Beyond CMOS”, and “More than Moore” [1]. Fig. 1 demonstrates the trend of the above-mentioned roadmap. It’s not only the “size shrinking” for devices that we focus on like before, but the innovative technology and architecture. To be more exact, people aim to both make the existing technology combined with novel applications in a multi-disciplinary way. For example, there are plenty of CMOS-integrated MEMS for biomedical and radio-frequency sensors used in disease monitoring, agriculture screening, and the electric vehicle industry. With such integration and new application, it gains us more profit and novel experience even using traditional semiconductor technologies, which is shown in the regime of “More-than-Moore”. In addition to the development of emerging applications, innumerable researchers are finding the possible solutions for the next-generation technologies needed for those much more advanced calculations for artificial intelligence. Energy consumption, calculation efficiency, and the device footprint are all critical factors for development. Thus, a great number of burgeoning technologies are proposed based on either in novel physical domain domains device architecture, like two-dimensional materials including graphene, transition-metal dichalcogenide monolayer, quantum computing, three-dimensional electronics, and a variety of emerging memory including ferroelectric RAM (FeRAM), resistive RAM (ReRAM) and magnetic RAM (MRAM). All the above can be referred to as “More-Moore” and even “Beyond CMOS”, which ultimately revolutionize the traditional CMOS

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regime. In the following, we focus on the regimes of “More-than-Moore” and “More-Moore”.

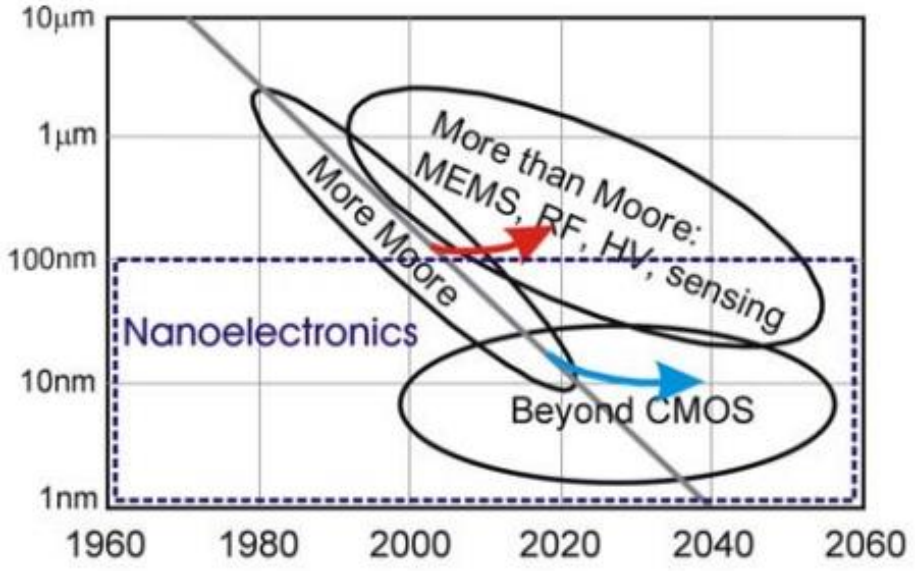

Fig. 1. The evolution of electronic devices with the size shrinking [1].

1.1 More-than-Moore

The term is referred to as "More-than-Moore" (MtM) due to the added functionality. To put it differently, this is a trend that focuses on expanding the functionality of semiconductor-based devices beyond digital capabilities. These additional functions contribute to making electronic systems smaller but do not necessarily have the same scaling rate as digital functionality. The additional functions include analog and mixed-signal processing, the incorporation of passive components, high-voltage components, micro-mechanical devices, sensors and actuators, and microfluidic devices that enable biological functions. These functions complement digital signal and data processing and allow for interaction with the outside world through transductions including actuators and sensors. It is important to note that the "More-than-Moore" technologies do not compete with digital trends described by Moore's Law but rather enable the integration of both

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digital and non-digital functionalities into compact systems. This integration will be the key driver for a wide range of applications in various fields such as communication, automotive, environmental control, and healthcare. Fig. 2 presents the dual trends in the development of the semiconductor industry. The horizontal direction is the development of diversification, which focuses on non-digital content.

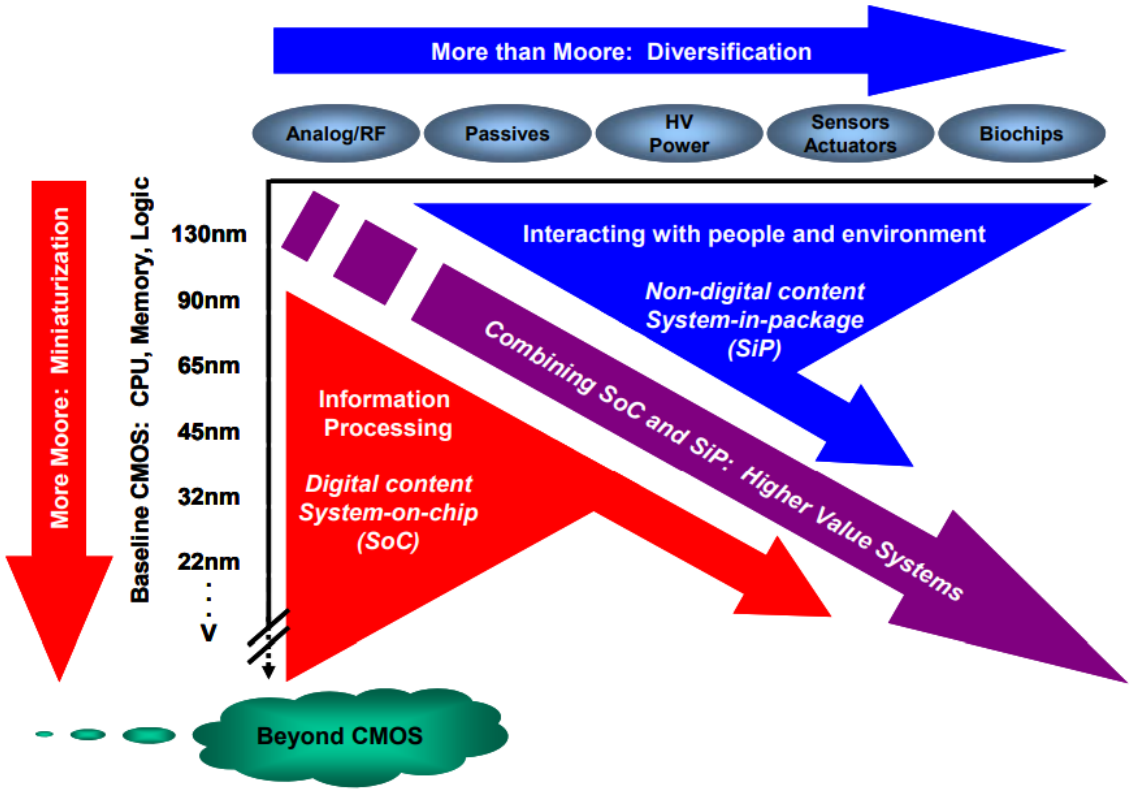

Fig. 2. A dual trend in the International Technology Roadmap for Semiconductors (ITRS): miniaturization and functional diversification [2].

1.2 More-Moore

Compared to the “More-than-Moore”, “More-Moore” pertains to the persistent reduction of the physical characteristics of digital functionalities such as logic and memory storage, with the aim of enhancing density (reducing cost per function) and improving performance (speed and power). More-Moore targets bringing performance,

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power, area, and cost value for node scaling every 2−3 years. The below reports the goal written in International Roadmap for Devices and Systems (IRDS): [3]

(P)erformance: >10% more operating frequency at scaled supply voltage

(P)ower: >20% less energy per switching at a given performance

(A)rea: >30% less chip area footprint

(C)ost: <30% more wafer cost – 15% less die cost for scaled die.

However, as we reach atomic dimensions, geometrical scaling faces physical limitations and the concept of equivalent scaling begins to be adopted. To put it differently, even though we make an all-out effort to diminish the size of a single device by either more advanced lithography techniques like EUV, high NA, and E-beam, there will still be an ultimate limitation as the device's channel is close to the scope of several atoms. As a result, it's intuitive to develop the above target trends in a different way, which is to build up toward the third dimension. Taking the same size of a device footprint can offer more area efficiency and integration possibility for future. Fig. 3 shows the roadmap of device architecture and ground rules for continuing the More-Moore regime. We can see that the architecture will contain two tiers from 2028, which is an unprecedented commercial structure. Under such novel architecture, it's not only the device progress that matters, but the design is also an absolutely different framework. That is, we should take advantage of this thought by proposing a new fabrication methodology or a new logic design for the standard cell library and PnR (place and route). By the co-optimization from both devices and circuits, the More-Moore vision can be realized and pushed further.

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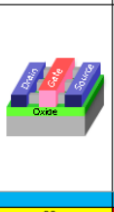
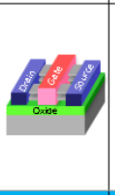
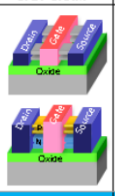
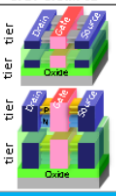
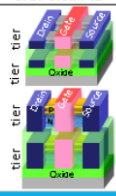
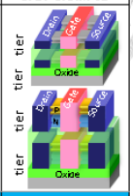
YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4	G38M16/T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
						
LOGIC DEVICE GROUND RULES						
Mx pitch (nm)	32	24	20	16	16	16
M1 pitch (nm)	32	23	21	20	19	19
M0 pitch (nm)	24	20	16	16	16	16
Gate pitch (nm)	48	45	42	40	38	38
Lg: Gate Length - HP (nm)	16	14	12	12	12	12
Lg: Gate Length - HD (nm)	18	14	12	12	12	12
Channel overlap ratio - two-sided	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	6	6	5	5	4	4
Spacer k value	3.5	3.3	3.0	3.0	2.7	2.7
Contact CD (nm) - finFET, LGAA	20	19	20	18	18	18
Device architecture key ground rules						
Device lateral pitch (nm)	24	26	24	24	23	23
Device height (nm)	48	52	48	64	60	56
FinFET Fin width (nm)	5.0					
Footprint drive efficiency - finFET	4.21					
Lateral GAA vertical pitch (nm)		18.0	16.0	16.0	15.0	14.0
Lateral GAA (nanosheet) thickness (nm)		6.0	6.0	6.0	5.0	4.0
Number of vertically stacked nanosheets on one device		3	3	4	4	4
LGAA width (nm) - HP		30	30	20	15	15
LGAA width (nm) - HD		15	10	10	6	6
LGAA width (nm) - SRAM		7	6	6	6	6
Footprint drive efficiency - lateral GAA - HP		4.41	4.50	5.47	5.00	4.75
Device effective width (nm) - HP	101.0	216.0	216.0	208.0	160.0	152.0
Device effective width (nm) - HD	101.0	126.0	96.0	128.0	88.0	80.0
PN seperation width (nm)	45	40	20	15	15	10

Fig. 3. Device architecture and ground rules roadmap for logic devices [3].

1.3 Research motivation

The research motivation of this thesis is to explore and develop both the More-than-Moore and More-Moore regimes. To begin with, we aim to deal with the issue of CMOS-integrated biomedical applications. With the advancement of sequencing technology, the field of medicine has focused on personalization, prediction, participation, and prevention. This has led to the development of "precision" medicine. However, current methods for diagnosis, monitoring, and tracking post-treatment progress still rely on complex and time-consuming procedures like blood analysis, biopsy, and medical imaging. This leads to delays in decision-making and treatment adjustments. For instance, in chemotherapy, the conventional method of determining drug dosage is primarily based on cancer stage and basic patient information such as age, gender, and body surface area, without considering individual pharmacokinetics (PK) which greatly impacts treatment

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effectiveness. There is a need for a technology that can measure drug concentration frequently from a patient's blood in less than 15 minutes in a point-of-care setting. Unfortunately, existing laboratory assays like ELISA or LC-MS take hours, making closed-loop therapy impossible. Cancer patients undergoing chemotherapy and/or radiotherapy require weekly blood tests to avoid low counts in white blood cells, red blood cells, and platelets. This necessitates weekly hospital visits, causing discomfort and inconvenience. Consequently, a technology that enables at-home cell detection would be highly desirable. To tackle these challenges, this proposal seeks to create point-of-care (PoC) devices and systems that combine CMOS integrated circuit design and microfluidics. This will allow for both single-cell detection and biomolecule sensing in a small, portable, and affordable platform that is easy to use.

It’s been decades for researchers to develop such fields. Yet, most of the previous research used CMOS and bio-related modules separately. In other words, they designed a variety of circuit architectures for biosensing performance, like lower noise and higher data rate, while their bio-targets and sensors/actuators are separately assembled. For example, microfluidics is an essential component for developing point-of-care bioengineering; however, most of the progress is in the scope of using PDMS (Polydimethylsiloxane) mold and bulk equipment. Herein, we aspire to expand the system-on-chip (SOC) further by designing a platform integrating both CMOS chips and microfluidics.

Likewise, the electrochemical sensing techniques also demand highly integrated, which means it’s desired to make the chemical reaction and sensing function on a single CMOS chip. Therefore, we try to develop the CMOS on-chip micro-electrodes in this work. Using such architecture, we aim to use aptamer, a single-strand DNA, as a sensing medium to screen the drug concentration. Furthermore, we also plan to integrate the above

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CMOS-embedded microfluidics with aptamer sensor applications, like selective immobilization or multiplex sensing technique.

Last but not least, we explore 3D electronics for developing the next-generation logic device. As the More-Moore trend goes, critical size shrinking becomes much more challenging than before. Thus, developing the device toward three-dimensional architecture is a promising solution. In this work, we target to adopt a low-cost fabrication method to realize the CFET structure, which is to stack the NMOS or PMOS to each other.

1.4 Thesis structure

There are six chapters in this thesis. The structure of this thesis is as follows: Chapter 1 gives the introduction to the concept of More-than-Moore and More-Moore regimes. Chapter 2 goes through the CMOS-embedded microfluidics for cell detection as a realization of More-than-Moore. It covers the design, fabrication, and system integration along with measurement results in this part. Chapter 3 describes the CMOS on-chip electrode development for the aptamer sensing technique. We demonstrate the fabrication and testing results by an on-chip electrode of 100μm ×100μm. Chapter 4 presents the fabrication of advanced technology beyond the 3nm node for the More-Moore regime. Finally, Chapter 5 and 6 is the conclusion and future work section. We summarize the thesis and give the future research design or direction to improve the work.

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Chapter 2 CMOS-embedded microfluidics

2.1 Research background

2.1.1 Micro/nanofluidics and lab-on-a-Chip

Microfluidics is a field to investigate and realizes the manipulation of fluids in micrometer-level dimensions. Microfluidics has been developed and explored in various fields including biomedical, physics, chemistry, and even microelectronics for these two decades.[4] Several characteristics and issues dominate in these fields, like laminar flow, fluidics resistance, and diffusion. It can be used for drug delivery, cellular biosensor, DNA analysis, and a myriad of lab-on-chip devices by exploiting the unique physical properties of fluids under such a scale. Fig. 4 shows the global microfluidics markets from 2021 to 2030. We can see the market growth of microfluidics due to the benefits of low-volume sample analysis, in-vitro diagnostics, and high-throughput screening methodologies, which indicates that microfluidics development and integrations are promising and important techniques.

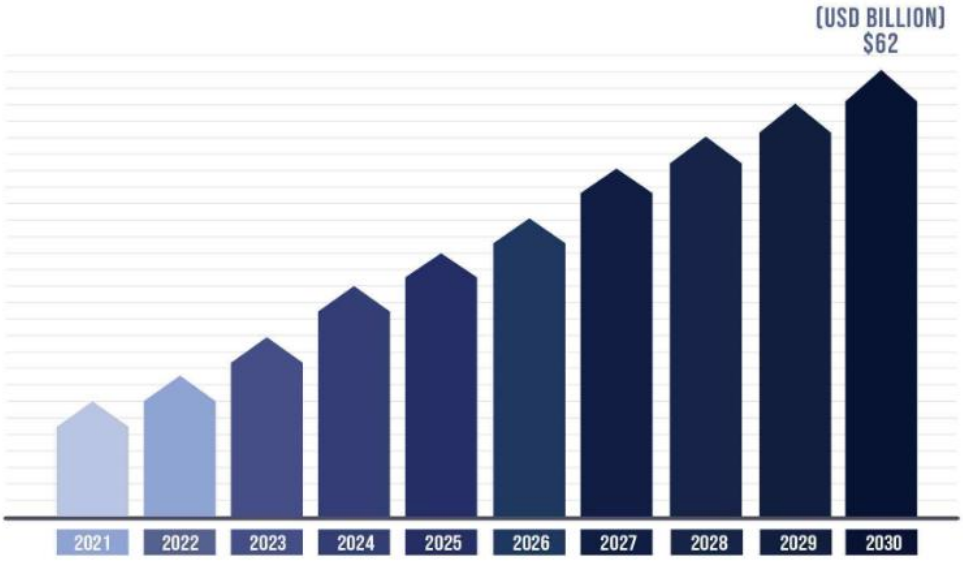

Fig. 4. Global Microfluidics Markets 2021-2030 [5].

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Even smaller than microfluidics techniques, the field of nanofluidics is in the domain of several nanometer scales, which brings us more novel properties that can't be seen at the microfluidics level. For example, R. B. Schoch et al. have one review paper to introduce the transportation phenomenon in the nanofluidic dimension, including electrokinetic effects in nanochannels, exclusion-enrichment effect, and concentration polarization at the interface.[6] To further explore plenty of characteristics and advantages, it's crucial to develop not only robust fabrication processes but an integrated system or device for further application and analysis purposes.

"Lab-on-a-chip (LOC)" is a concept for integrating several components with laboratory functions, utilizing a small number of samples and highly compacted integration to realize a variety of manipulations and analyses. It transforms the conventional methodology from some bulky equipment and laborious work to a much more compact platform that is highly integrated for biomedical, mechanical, and electrical blocks. Fig. 5 illustrates the concept of lab-on-a-chip. It contains various structures to carry out the functions like sample collection, mixing, filtering, and so on.

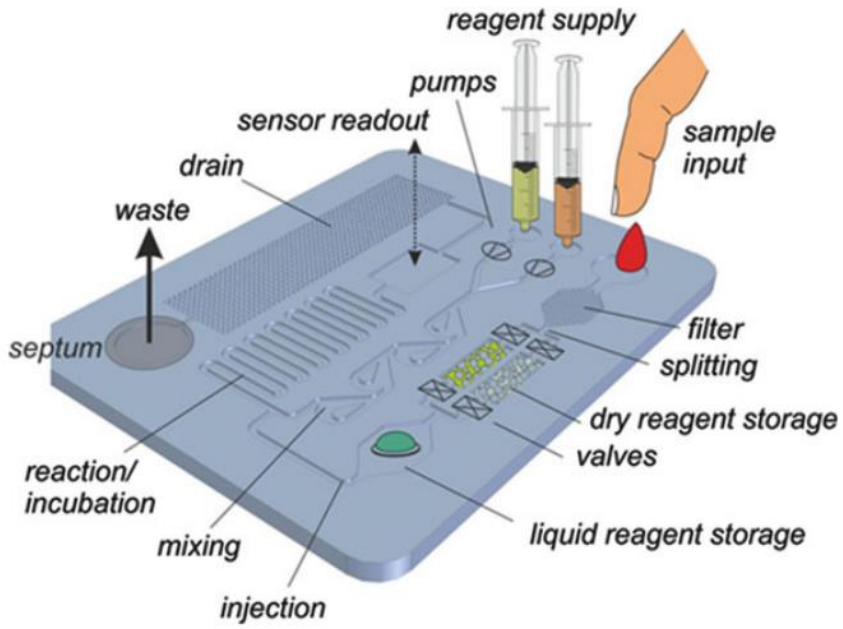

Fig. 5. Lab-on-a-Chip devices for point-of-care applications [7].

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2.1.2 Integration of CMOS chip and micro/nanofluidics

Fig. 6 depicts several blocks contain in a LOC integration. We can generally classify those blocks into three main functions: actuation, sensing, and read-out. The actuation part is to generate some stimulation in the sample, either in electrical or mechanical ways. The sensing part is to get the property variation including electrical, optical, magnetic, and so on the signal. And the readout includes several circuit blocks like analog front-end amplification, power management, wireless communication, and some signal processing units. To achieve lab-on-a-chip integration, we can benefit from the advantages of the CMOS chip, which enables us to get a small footprint and reader-less system integration.

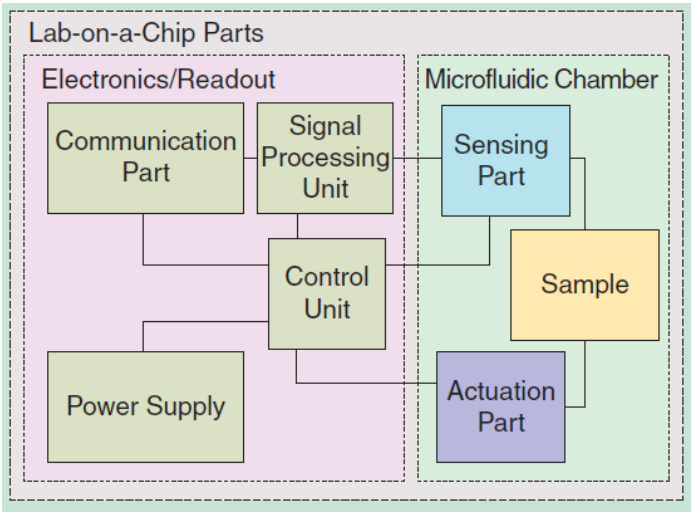

Fig. 6. LOC blocks [8].

Among these parts shown in Fig. 6, there are two higher-level domains which are electronics/readout and microfluidics existing on a LOC. Integrating millimeter-size CMOS chips with micro/nanofluidics has gained significant interest as it offers the potential for reader-less operation. In addition, embedding CMOS electronics near the samples-to-be-detected improves the accuracy as the unwanted routing parasitics can be largely eliminated.

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Generally, the integration of fluidics and CMOS electronics is often accomplished using a modular assembly approach. For ample, Y. Huang's work, it demonstrates the integration of microfluidics and CMOS IC by a method that is compatible with the chip and multiple fluidic channels. The approach is realized with polyimide, epoxy, SU8 photoresist, and a tube.[9] In J. C. Chien's work, it shows a CMOS flow cytometry platform with an oscillator-based sensor. And it makes use of epoxy, glass slide, and PDMS for the integration of chip and fluidic components.[10] Yet, these methods have limitations due to the achievable level of alignment accuracy, thus limiting fluidic design options. To be more clear, the alignment may work for a 50-μm dimension but not for narrower ones like below 10μm. Fig. 7 shows the illustration of the above works.

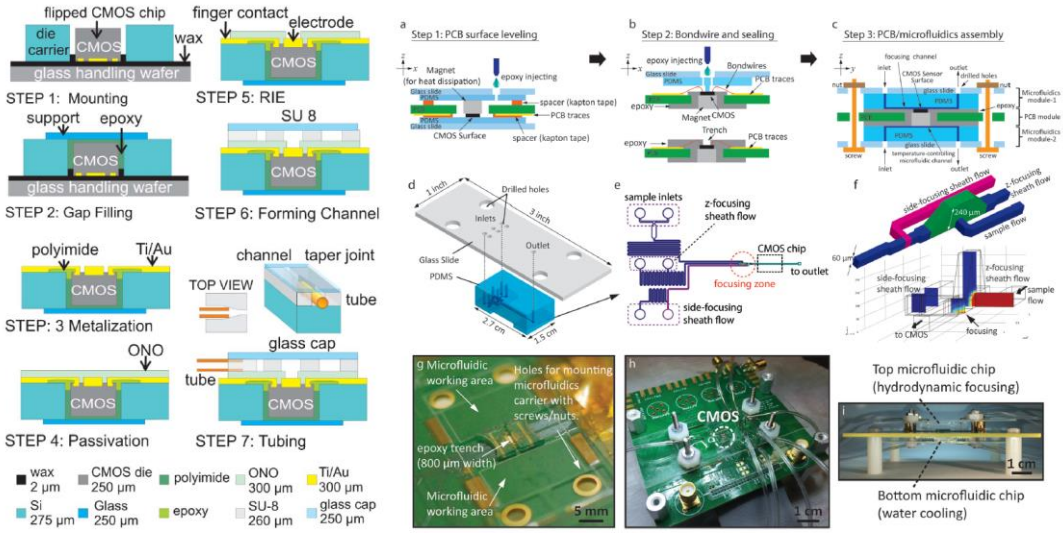

Fig. 7. The CMOS/microfluidics integration methodology from [9](left) and [10](right).

For the sake of better alignment and lower pick-up noise from the sensing module to the reader, some works have tried to develop the platforms which combine these two parts together. Generally speaking, there are three main types of channel formation methodology: (1) wafer bonding, (2) Nano-imprint, and (3) sacrificial etching as shown in Fig. 8.

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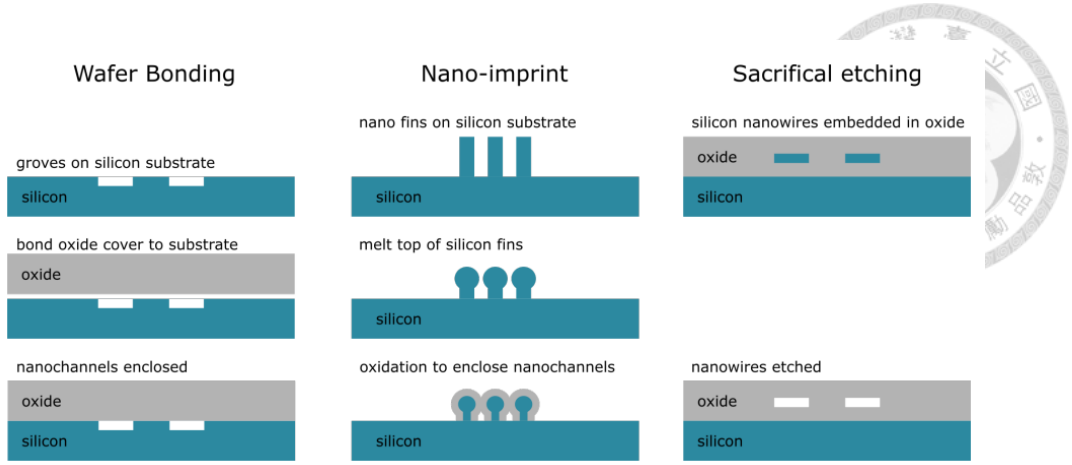

Fig. 8. Comparison of three general fabrication methods for micro/nanochannels [11].

The bonding of two inflexible materials via wafer bonding needs high-temperature annealing to achieve a strong bond, but often suffers from issues such as leakage and yield problems. In addition, the process cost of wafer-bonding is also higher than other techniques. The nano-imprint technique employs a high-power laser to melt the entrance of silicon slit structures and seal the nanochannels, but we need to concern that the high temperature involved could potentially compromise the control of structural integrity. Noting that both wafer bonding and nano-imprint techniques require direct operations on substrate wafers, which are incompatible with CMOS processes. The sacrificial etching method utilizes either solution-based or gas-based etchant to remove the sacrificial part of the device, then it forms a channel space. Admittedly, sacrificial etching may encounter limited efficacy at the nanometer scale due to difficulties in solvent diffusion and the elimination of reaction by-products. Yet, it allows us to integrate with CMOS chips through a simpler process.

The following are some previous works for the integration of fluidic channels to either the CMOS chip or compatible semiconductor standard process. C. Wang *et al's* work [12], involves a wafer-scale bottom-up fabrication technique that uses etching to create nanoscale hollow channels in a patterned silicon layer inside silicon oxides. This method

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was demonstrated with the detection of stretched DNA using a laboratory microscope, but its compatibility with standard CMOS processes is limited by its complex fabrication flow. F. Hjeij *et al* [13] use deep reactive ion etching (RIE) to create open fluidic channels on a BiCMOS chip, taking advantage of ion-etching selectivity to trap single cells with dielectrophoresis. Fig. 9 and Fig. 10 show the process flow and device cross-section of C. Wang *et al's* work and F. Hjeij *et al's* work respectively.

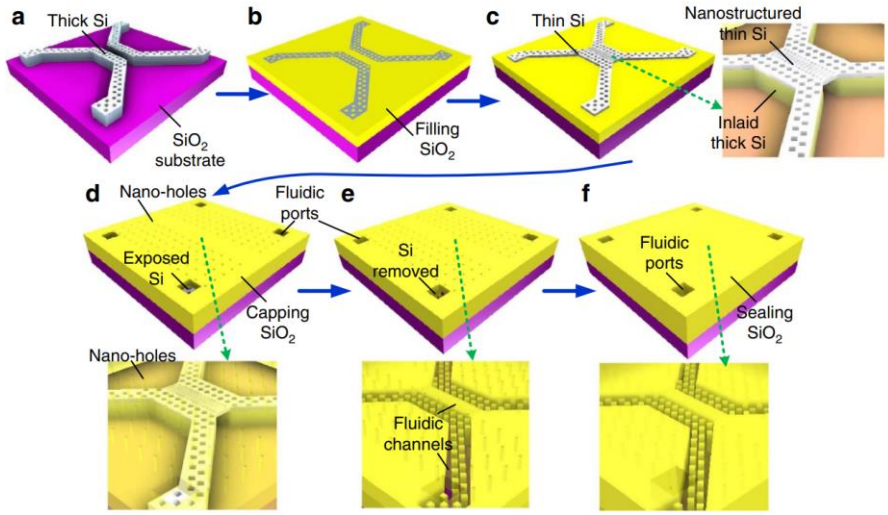

Fig. 9. Wafer-level fabrication of nanofluidic channels based on the gas-phase etching [12].

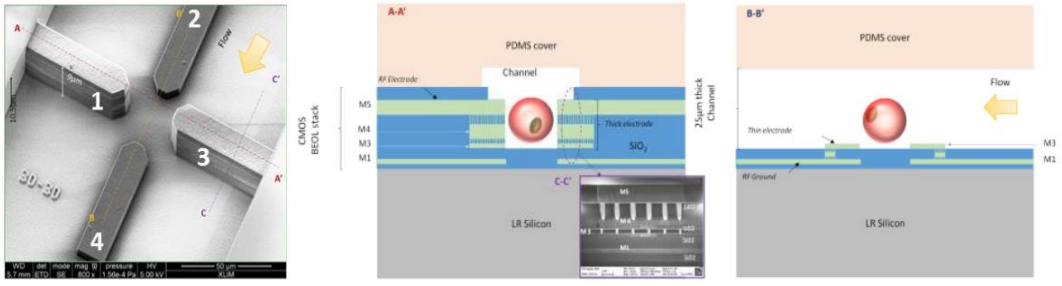

Fig. 10. Cross-section of the microfluidic channel after deep reactive ion etching [13].

Rasmussen *et al* [14] use a combination of gas and liquid-based etching to remove polysilicon and metal routings from a 2.0-μm CMOS chip, creating channels with depths

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ranging from 0.5 to 100 μm, and integrating on-chip thermopiles for a liquid flow rate sensor. In H. Meng's thesis [11], it introduces nanofluidics on CMOS photodetectors by sacrificing a thin polysilicon layer, but the process requires deep reactive ion-etching to create access through the passivation, which may result in uncontrolled over-etching. Fig. 11 and Fig. 12 show the process flow and device cross-section of A. Rasmussen *et al*'s work and H. Meng's work respectively.

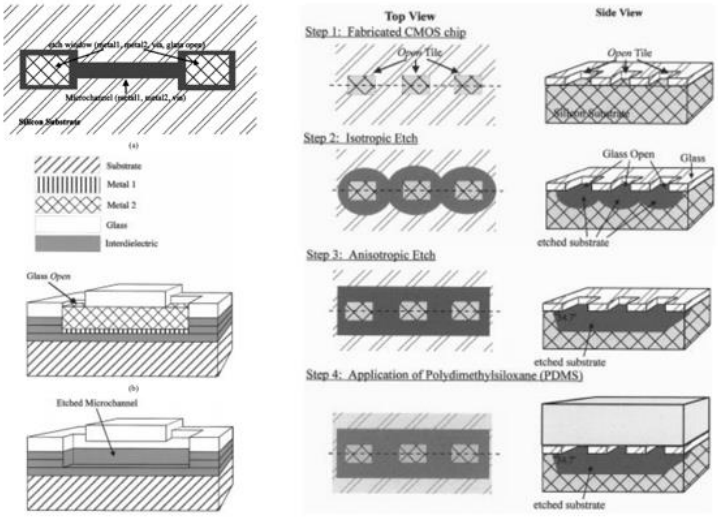

Fig. 11. BEOL post-processed by gas-based and liquid-based wet etch [14].

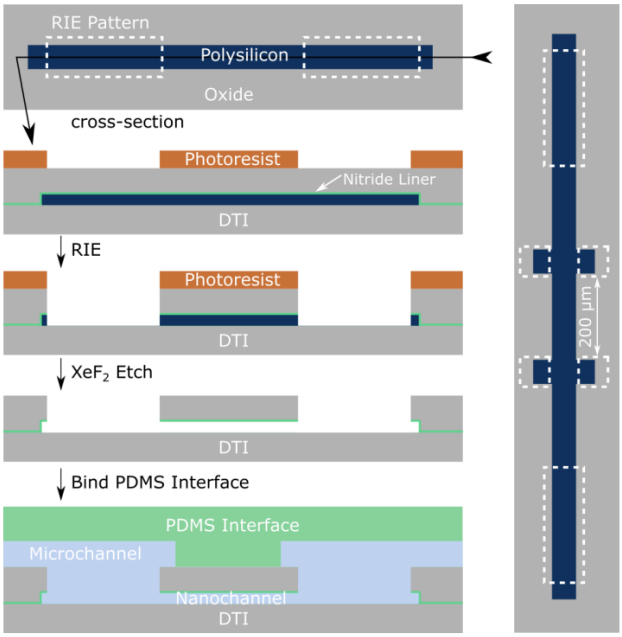

Fig. 12. Illustration of using the polysilicon as a sacrificial layer for nanochannels [11].

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2.1.3 Cell detection methodology

Detection and quick identification of small organisms like bacteria or pathogens have been critical processes in preventing human illness or environmental pollution. As time goes by, the development of detection methodology and tools is unceasingly progressed. In this subsection, we will introduce several kinds of the cell detection method.

Traditionally, the most prevailing and established method is colony counting and culturing. Relying on direct culturing in the petri-dish, the process contains several steps requiring a laboratory environment and materials. As shown in Fig. 13, it presents the needed procedure for culturing from our lab. Using this *in vitro* method, we need to prepare the chemicals, like the broth and also have to wait for quite a bit of time for the growth of our targeted bio-sample. As a result, this culturing-based assay is less convenient and laborious for our detection purpose.

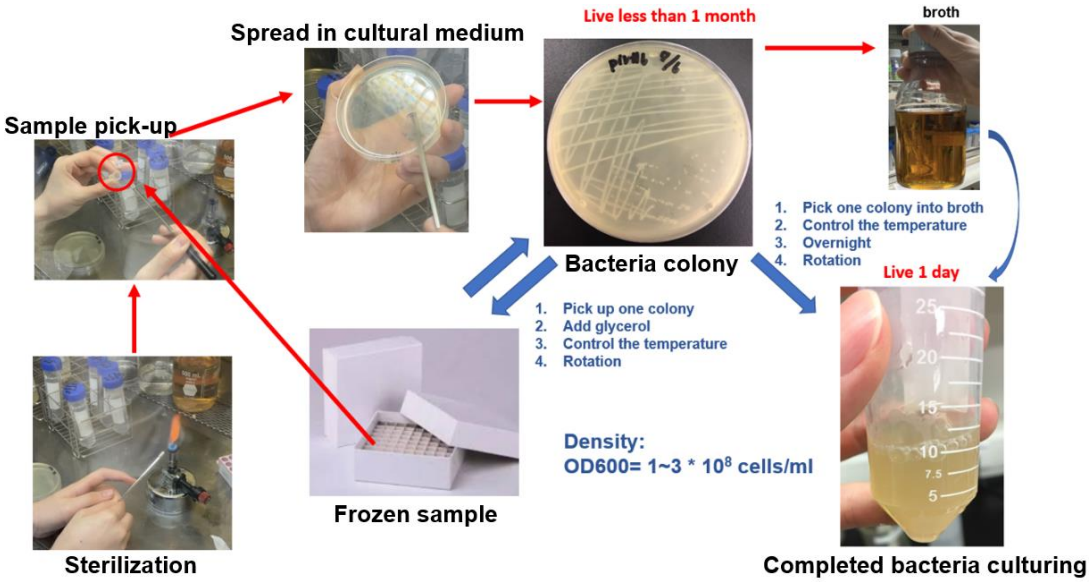

Fig. 13. Illustration of colony counting and culturing process in our laboratory.

Another biological method is called polymerase chain reaction (PCR). PCR is a technique using nucleic acid amplification, which means that we can rapidly produce abundant of a specific segment of DNA. This technique is relatively fast and inexpensive,

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and it allows us to do bacteria or virus detection and other diagnoses of genetic disorders. As shown in Fig. 14, PCR mainly contains three phases: denaturation, primer annealing, and primer extension. High temperatures exceeding the melting point of DNA are used to separate the specific double-stranded DNA. After that, the DNA is purified and subjected to an extension phase with the help of primers and an enzyme capable of polymerization at high temperatures. This leads to the formation of new double-stranded DNA, which acts as a target for the next cycle, resulting in exponential amplification. The primers are extended in the 5' to 3' direction by a polymerase enzyme to overlap the copies of the original template. After again and again repeating, there will be multiple DNS segments produced.

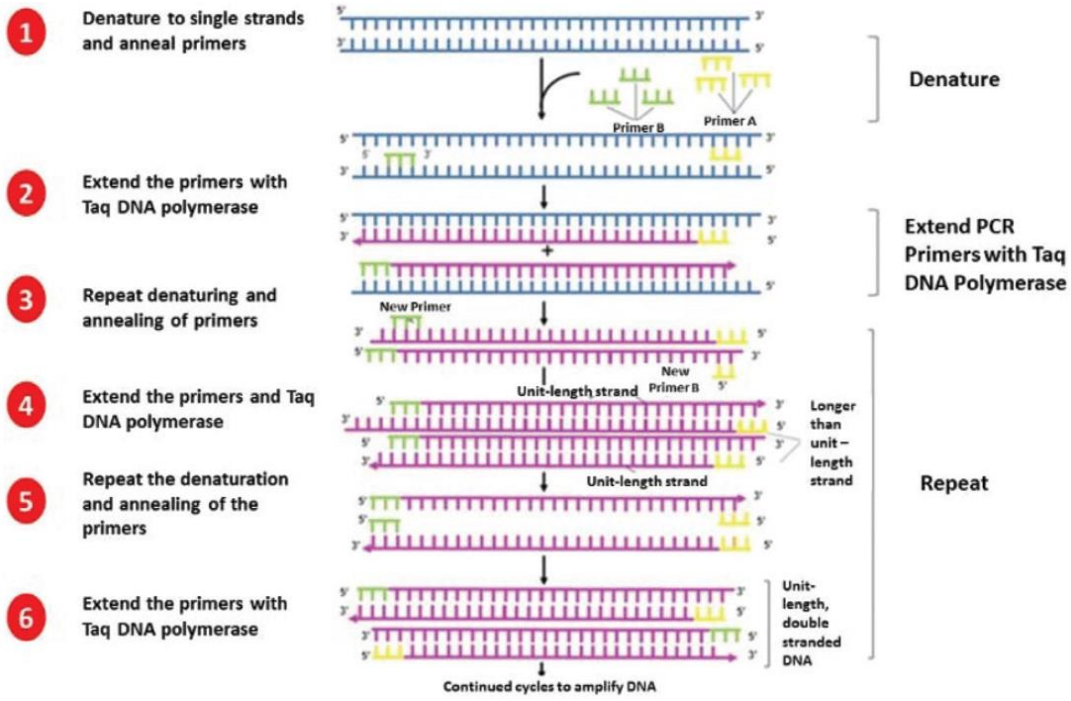

Fig. 14. Schematic representation of a PCR cycle [15].

The main disadvantages of the above two techniques are requiring considerable amounts of laboratory equipment and time. In addition, they are also highly sensitive to contamination. In the following, we are going to introduce a technique, flow cytometry,

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for cell/particle detection with higher throughput and it is less susceptible to the contamination of bio-samples.

Flow cytometry is a speedy method for examining individual cells or particles that are suspended in a salt-based solution and are moving past one or more lasers. Traditionally, flow cytometry is optical-based, which utilizes a laser or other light source to perform the detection. This technology assesses each particle based on its visible light scatter and fluorescence parameters. The visible light scatter is measured in two ways: forward scatter (FSC) which can give an idea of the particle's size and side scatter (SSC) which indicates the particle's internal complexity or granularity, measured at a 90° angle. The instrument setup is shown in Fig. 15. In addition to the optical-related systems, like lasers and FSC/SSC detectors, there is also a fluidic system for hydrodynamic focusing to generate the sheath flow.

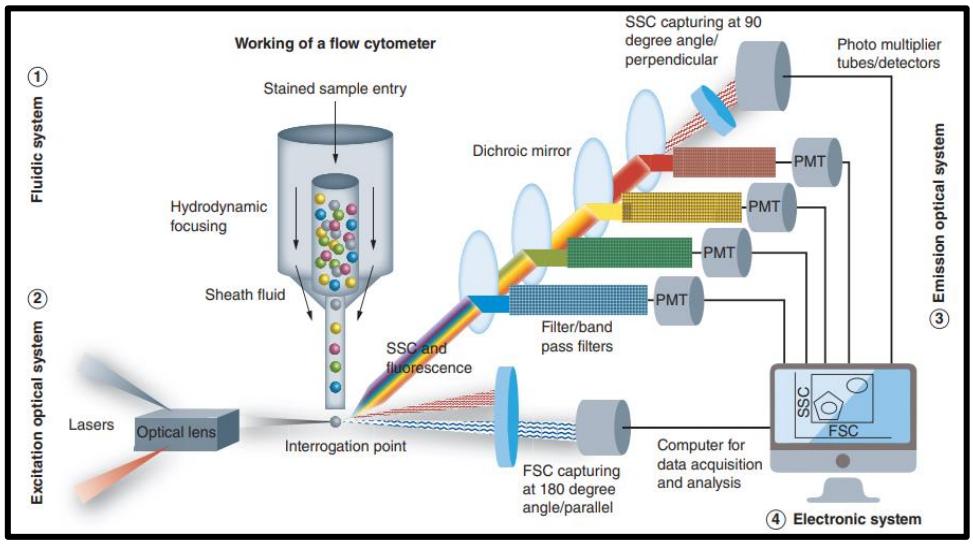

Fig. 15. Optical flow cytometry schematic [16].

Flow cytometry is an influential technology with widespread applications in various fields, including immunology, virology, and molecular biology. It enables the simultaneous identification of mixed groups of cells obtained from blood and other liquid-based biological samples that can be separated into individual cells. In addition to

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analyzing cell populations, flow cytometry is commonly used for separating cells into homogeneous groups for further analysis downstream. Yet, the main disadvantage of optical flow cytometry is the complex optics, and this complexity makes it difficult to be further miniaturized into a portable in-vitro detecting device.

Impedance-based flow cytometry is a promising technique for cell detection but without the complex instruments mentioned above. Coulter established Coulter's principle in 1948 by showing that tiny openings could be used to identify cell suspensions. The schematic of the Coutler counter technique is shown in Fig. 16. This technique relies on impedance and it allows for critical cell counting functions including measuring the size and quantity of biological cells. Because cells have poor conductivity, when a liquid containing cells is drawn through the small hole from the inlet to the outlet, the resistance between two electrodes is altered, and an immediate voltage pulse signal is produced that indicates the number and size of cells.

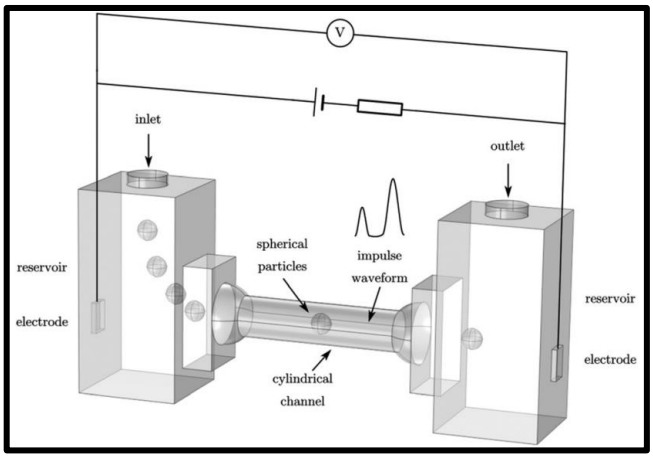

Fig. 16. Schematic of Coutler counter technique [17].

With the advancement of CMOS technology, the impedance analyzer using a CMOS circuit becomes a potentially promising technique. Most impedance cytometry studies have concentrated on measuring frequencies ranging from kHz to MHz, with a focus on determining characteristics such as cell size, membrane capacitance, and cytoplasm conductivity. The equivalent circuit model of a cell is shown in Fig. 17(a). We can

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simplify the cell model into the components of several resistance and capacitance, including the contribution from the cytoplasm and cell membrane. In addition, there are also channel resistance/capacitance and the double-layer capacitance formed in the solution. Fig. 17(b) illustrates the sample (small particles or cells) flowing through the parallel electrodes. They generate electric field perturbation as they flow through, then we can extract these signals for detection purposes. And Fig. 17(c) shows the source-differential impedance cytometry architecture, which is extended from the schematic in Fig. 17(b).

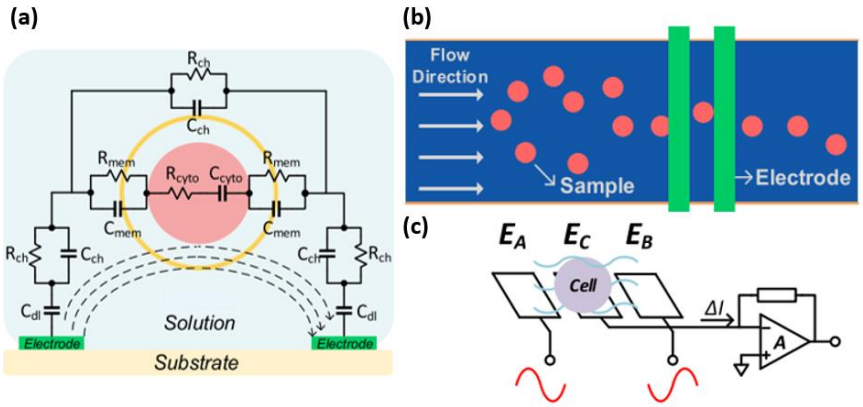

Fig. 17. (a) The equivalent circuit model of a single cell. (b) The top-view illustration of electrodes. (c) The topology of source-differential impedance cytometry [18].

Without baseline current cancellation, the current output from single-ended and single-source differential approaches can mix small cell-induced changes with a large baseline current, using up most of the input dynamic range of the downstream measurement electronics for the baseline channel signal. This can limit the achievable measurement sensitivity for the small cell signal and the usable gain. Therefore, the source-differential measurement is preferred compared to single-ended and single-source differential approaches.

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After knowing the concept of impedance-based flow cytometry using CMOS, we are going to introduce the common blocks for the detecting function. As shown in Fig. 18, there are five most common blocks in this standard architecture: voltage source, electrodes, transimpedance amplifier, mixer, and filter. The input voltage signal passes through the electrodes and is perturbed by particles on the received current, then the transimpedance amplifier will amplify this stimulation into voltage. This voltage will be demodulated by local oscillator (LO) signals and generate in-phase and quadrature-phase demodulated signals. Lastly, these two signals are filtered by a low-pass filter to remove the unwanted tones generated by the mixer. (Fig. 18)

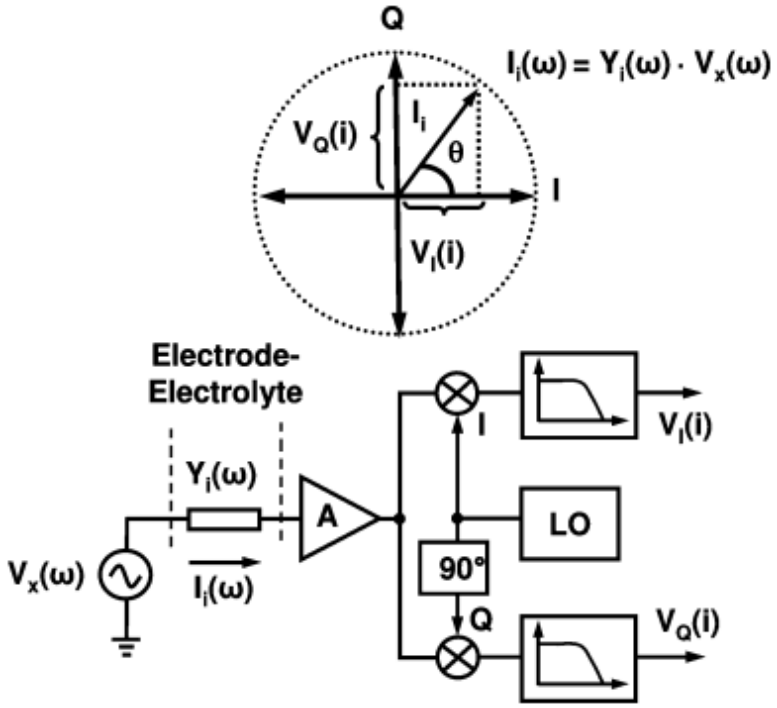

Fig. 18. Standard architecture for the impedance measurement [19].

2.2 Research motivation

Microfluidics devices have been developed for Point-of-Care (PoC) applications. In addition, integrating millimeter-size CMOS chips with microfluidics has gained significant interest as it offers the potential for reader-less operation. It's also beneficial

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to the pick-up noise consideration if we can make the microchannel adjacent to our sensing circuit. In this work, we aim to develop a system integrated the microfluidics and CMOS chips. Starting from the layout design, we utilize the back-end-of-line (BEOL) as the microchannel embedded in the CMOS chip. To develop a such platform, we investigate the etching process, channel geometry, sensing electrodes, and circuit integration respectively. The ultimate goal is to realize a highly integrated system combining microfluidics parts and analog front-end circuits for in-vitro biosensing purposes.

2.3 Proposed system concept

Inspired by the above pioneer works and our research motivation, we present a CMOS-embedded 3D micro/nanofluidics for biosensing in advanced CMOS technology. The device illustration is shown in Fig. 19. Compared to the conventional CMOS Lab-on-Chip systems where the fluidics and the electronics are modularly integrated together, the proposed method utilizes the metallization in the back-end-of-line (BEOL) of a CMOS process to create fluidic channels of desired geometry followed by a one-step wet etching process. As such, hollow channels are formed within the passivation and the inter-metal dielectrics of a CMOS die and the samples can be in closer interface with the detection electronics. Table 1 lists the comparison of this work to previous ones. Most of the previous works only focus on either the micro-channel formation or the circuit design for cell detection; however, in our work, we aim to develop both of them to get a highly integrated platform. Fig. 20 shows the die photos of our proposed architecture. Those structures and circuits will be introduced in the latter sections.

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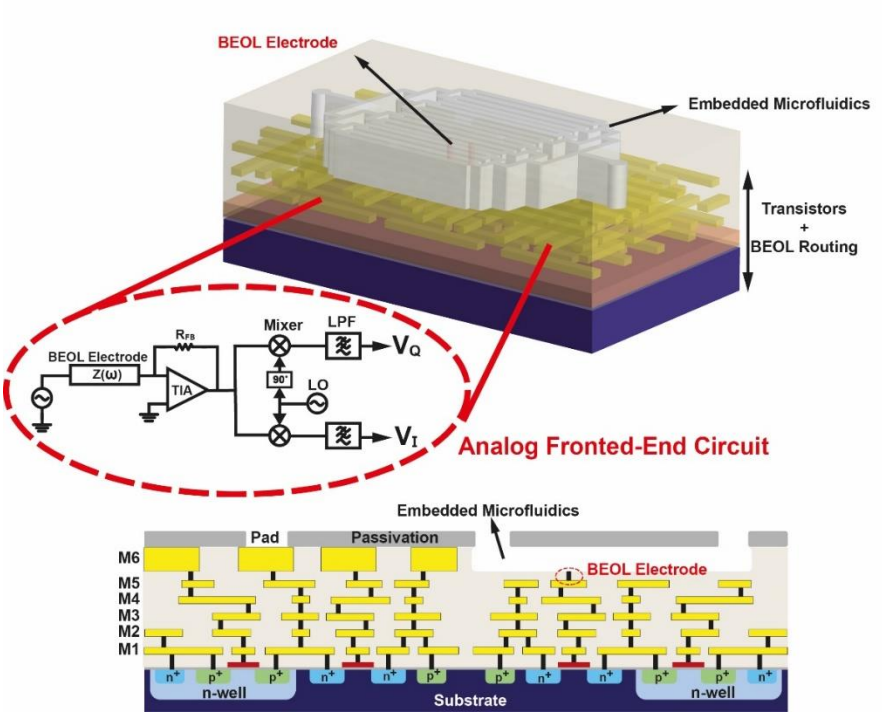

Fig. 19. Our proposed device illustration and the cross-section view of embedded microfluidics in a traditional CMOS device.

Table 1 Comparison table of this work and previous works.

	Our work & [15]	[12]	[16]	[17]	[18]	[19]
Technology	**180nm**	2μm	BiCMOS	90nm	Wafer-level	180nm
Process	**Top-down BEOL wet etch**	Top-down hybrid etch	Wafer-bonding	Top-down RIE + poly-Si dry etching	Bottom-up deposition/lithography/etching	SU8 lithography
Applications	**Impedance sensing /Cell detection**	Flow rate sensing	Fluid differentiation	photodiode	DNA manipulation	Beads detection
On-chip/off-chip channel	**On-chip**	On-chip	On-chip	On-chip	Off-chip	Off-chip
Channel area (Minimum)	**1 μm * 6 μm**	50 μm * 100 μm	375 μm * 700 μm	100 nm * 8 μm	42 nm * 5 nm	50 μm * 40 μm
AFE circuits	**TIA Gain: 120dB Bandwidth: 1MHz Input-referred noise: 0.39nArms**	N/A	VCO-based dielectric sensor 120GHz	N/A	N/A	TIA + Mixer Gain: 60dB Bandwidth: 40MHz Input-referred noise: 6pArms

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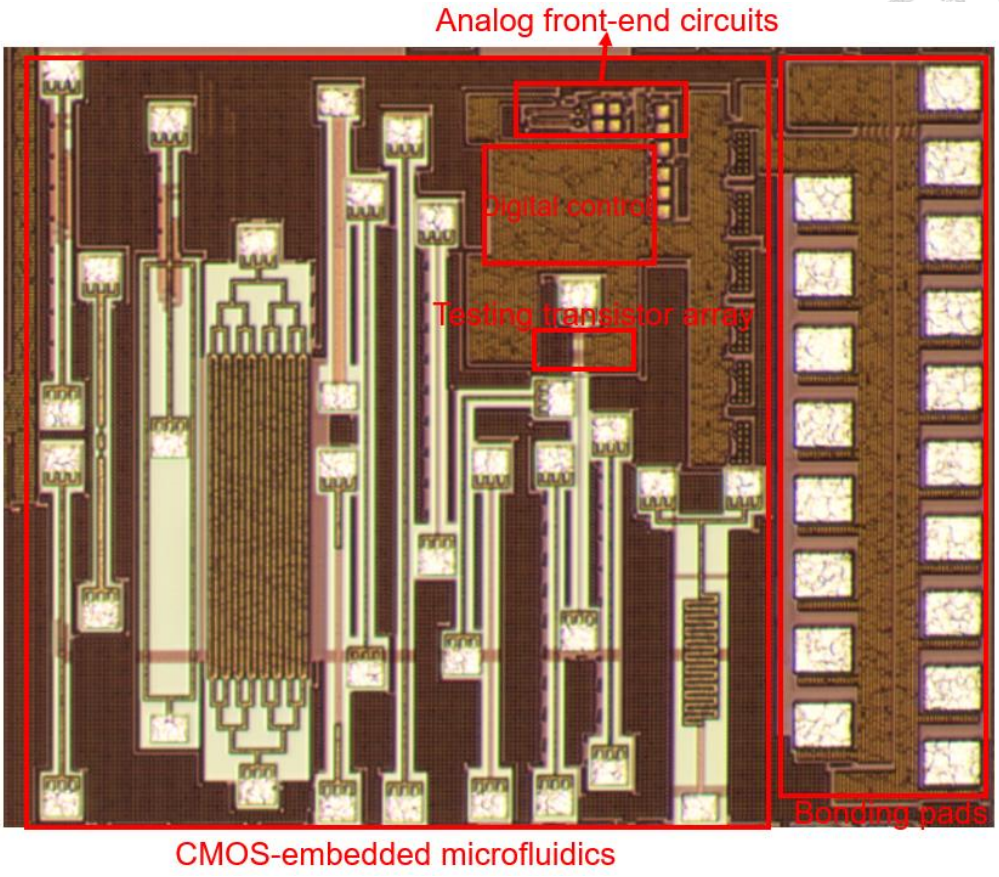

Fig. 20. Die photo of the proposed architecture.

2.4 BEOL etching process

2.4.1 Etching in bulk solution

To simplify the post-processing cost and complexity, we adopt a single-step wet-etching process. Fig. 21 shows the concept of our proposed post-processing. The implementation flow starts with the layout of the fluidic structures using metal and pad layers. The designer has the freedom to choose channel widths and gaps as long as they meet the foundry design rules; on the other hand, the channel height is generally fixed by the chosen CMOS technology and the metal layers. After chip fabrication, we sacrifice these metals by immersing the chips in metal etchants at an elevated temperature (65℃). We call this step “bulk etching” to compare with “localized etching”, which will be

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discussed in the next section. Noting that we need to cover the bond pads on the chip to protect them from being etched at the same time. In the meanwhile, to prevent the possible attack from the etchant, we further prevent bond pads from touching the etchant by suspending them on a PDMS. In this way, we can make sure the bond pads' quality without concerning long etching time. The experimental setup photo for the initial bulk etching is shown in Fig. 22.

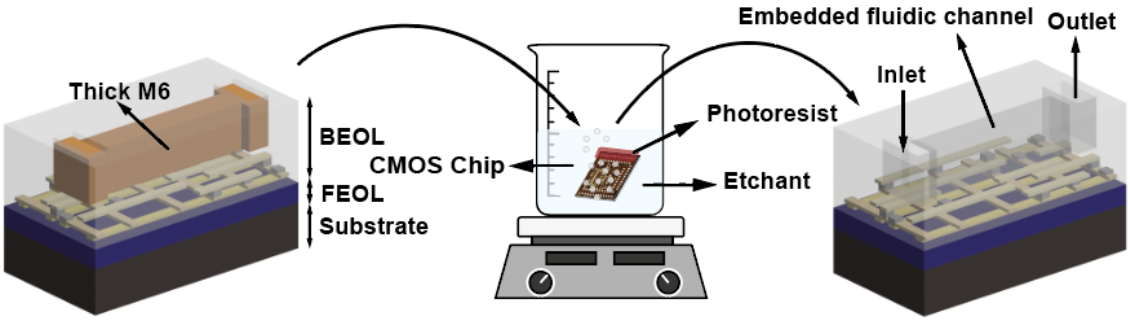

Fig. 21. The illustration of our proposed post-processing method.

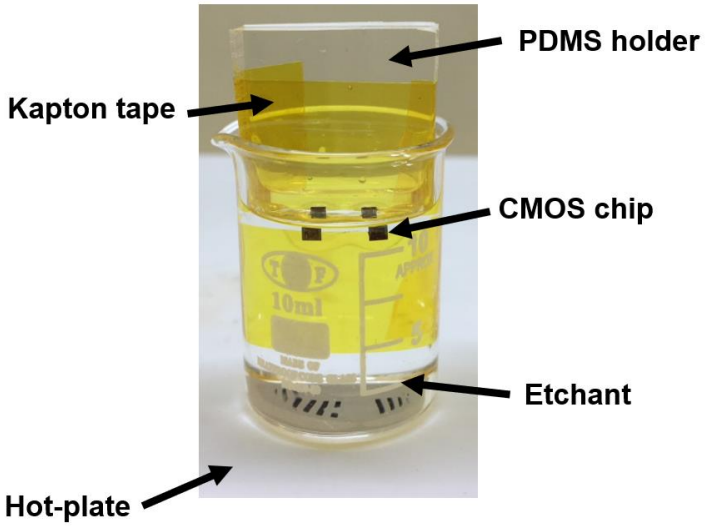

Fig. 22. The setup for bulk-solution etching.

2.4.2 Optimized etching process

The choice of etchant for metal materials varies depending on the metal type. We conducted a comprehensive study to identify the factors affecting the etch rates, including the type of etchant acid, etching temperature, agitation, and hydraulic pressure.

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Our experiment showed that replacing the commercial aluminum etchant (Type A aluminum etchant from Sigma Aldrich) with a copper etchant based on phosphoric acid and hydrogen peroxide (Cu-129 copper etchant from Chemleader Corporation) can reduce the time required for the complete removal of M6 aluminum by 5×at 65°C without stirring. In our specific channel geometry (described in Section 2.5), we found that the etchant diffusion and replenishment rates at the etch fronts were the limiting factors rather than temperature and agitation. To overcome this issue, we modified our testing setup to include hydraulic pressure. We planarized the chip surface using biocompatible epoxy (Epotek 302-3M) (described in Section 2.7.3), covered it with a PDMS with a 2-mm wide well, and inserted a syringe with a blunt needle after infusing the etchants. The etching was done at room temperature, and this approach improved the overall etch rate for a straight channel by 10×. Importantly, this method completely removes the aluminum to form a 16-channel, 6-μm wide, 760-μm long microfluidic structure, which was previously unremovable even after weeks of immersion in etchants. The total etch time was approximately 24 hours. This structure represents a crucial step towards the high-throughput processing of high-volume bio-samples. (Fig. 23)

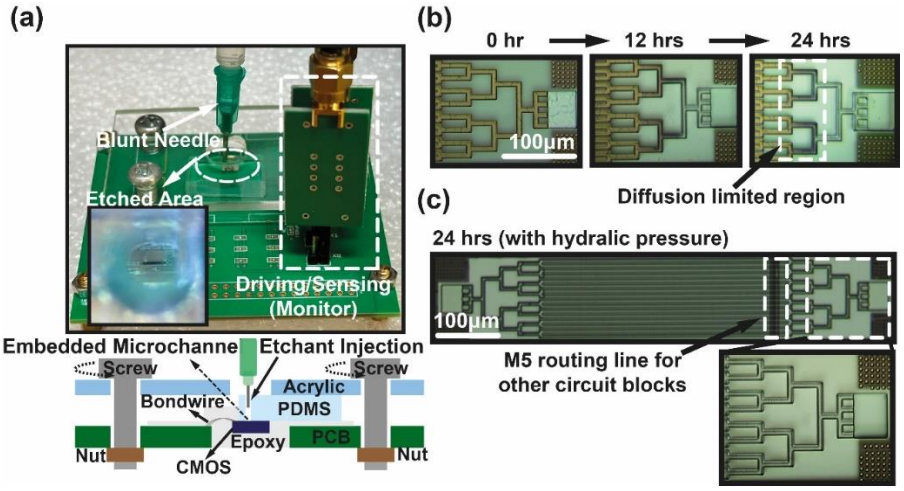

Fig. 23. (a) The setup for applying hydraulic and its cross-section view. (b) The optical images show the unsuccessful removal of the on-chip metal routing using an aluminum

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etchant. There are no significant changes in the structure beyond 24hrs. (c) Successful formation of 16-channel microfluidics with Cu-129 copper etchant.

2.5 Passive structures

This section introduces the passive structures involved in our 180-nm technology layout design. The structures include those structures for etch rate investigation by various width straight lines; the multi-channel structures are included for high-volume bio-samples delivery; 3D-stacked structures are explored to find the possibilities of further sensing architecture, like nanopore scheme; a width-varying structure is for resistive pulse sensing (RPS); the sheath flow focusing feature is investigated; and lastly, a serpentine structure is also surveyed for the micromixer.

2.5.1 Straight line channel with various sizes

To understand the etching feasibility, we drew a variety of straight-line structures with different line widths in the M5 and M6 layers. Fig. 24 shows two layout structures tested for this purpose, which are 420μm long and 4μm wide in M5 and M6 layers. The summary of etch rate for each geometry is shown in Table 2. This survey is executed under bulk aluminum etchant at 65°C and without any additional hydraulic pressure. Though it was done before etching optimization, we could conclude that all these simple structures (straight-line) can be etched away under the technology-specific design rules for both M6 & M5.

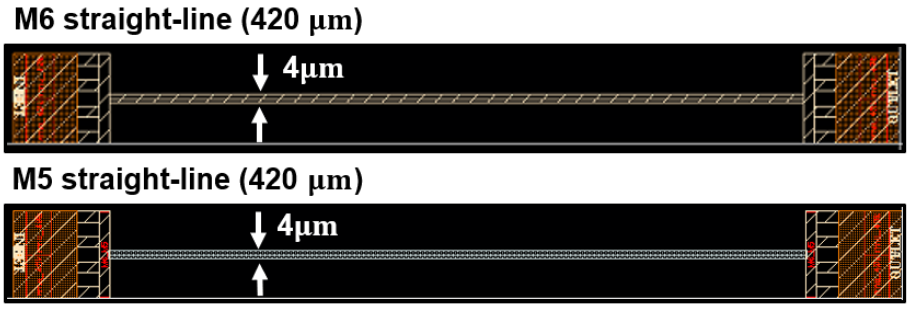

Fig. 24. The layout of two straight-line structures in M6 & M5.

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Table 2 The etch rate of different channel geometries.

Component	Etch rate
Width: 2.6μm ; length: 420μm (M6)	9.84 μm/hr
Width: 2.6μm ; length: 600μm (M6)	11.68 μm/hr
Width: 4μm ; length: 420μm (M6)	9.85 μm/hr
Width: 6μm ; L: 850μm (M6)	12.56 μm/hr
Width: 1μm ; length: 420μm (M5)	9.83 μm/hr
Width: 2.6μm ; length: 420μm (M5)	10.25 μm/hr
Width: 4μm ; length: 420μm (M5)	9.27 μm/hr

2.5.2 Multiple-channel splitter

It is common to use a splitter to divide the flow of fluids in microfluidics systems. For example, a multiple-channel splitter is an important functional structure to increase the sample capacity and further reduce costs for Enzyme-linked immunosorbent assay (ELISA) [20]. We investigated the feasibility of combining this feature into our CMOS chip by 4-channel and 16-channel structures. Fig. 25 demonstrates the etching status of a 4-channel structure. Surprisingly, the etching shows an anisotropic property. This anisotropicity will have a great impact on the integration of sensing electrodes and fluidics channels. We describe this phenomenon more in Section 2.4.2. In addition, we inject 1μm beads as a proxy for cells and observe successful flowing without clogging. (Fig. 26)

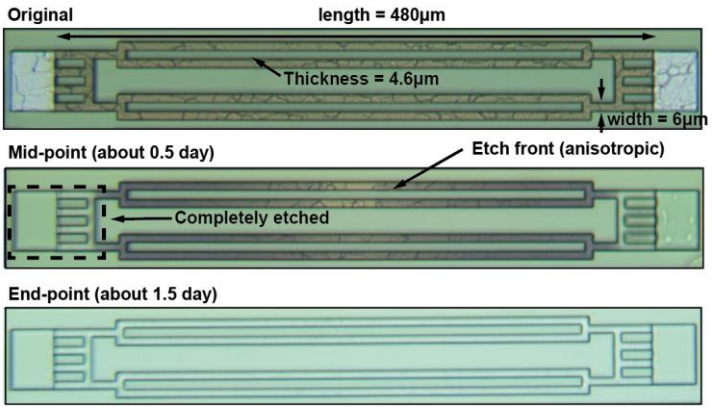

Fig. 25. Etching status of multiple-channel structures under an optical microscope.

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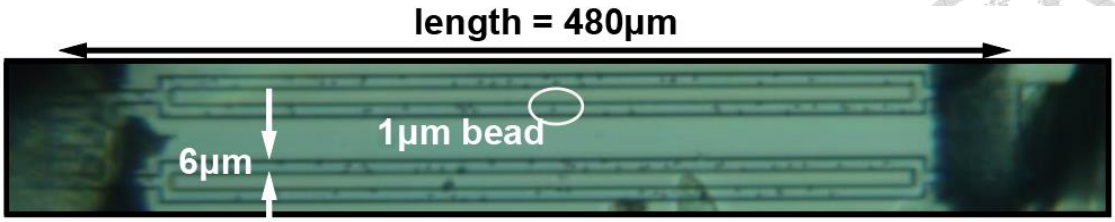

Fig. 26. Functional verification using 1μm beads.

In addition to the 4-channel splitter, we also explored the feasibility of a 16-channel one. As described in Section 2.1.2, it's not feasible to use our original etching method to successfully form a complete-etched 16-channel splitter. We need to adopt the method of etching along with hydraulic pressure to conquer the etchant diffusion limitation in the etch front. Fig. 27 shows the results of using the above-mentioned etching method. We can see the completely etched microchannel.

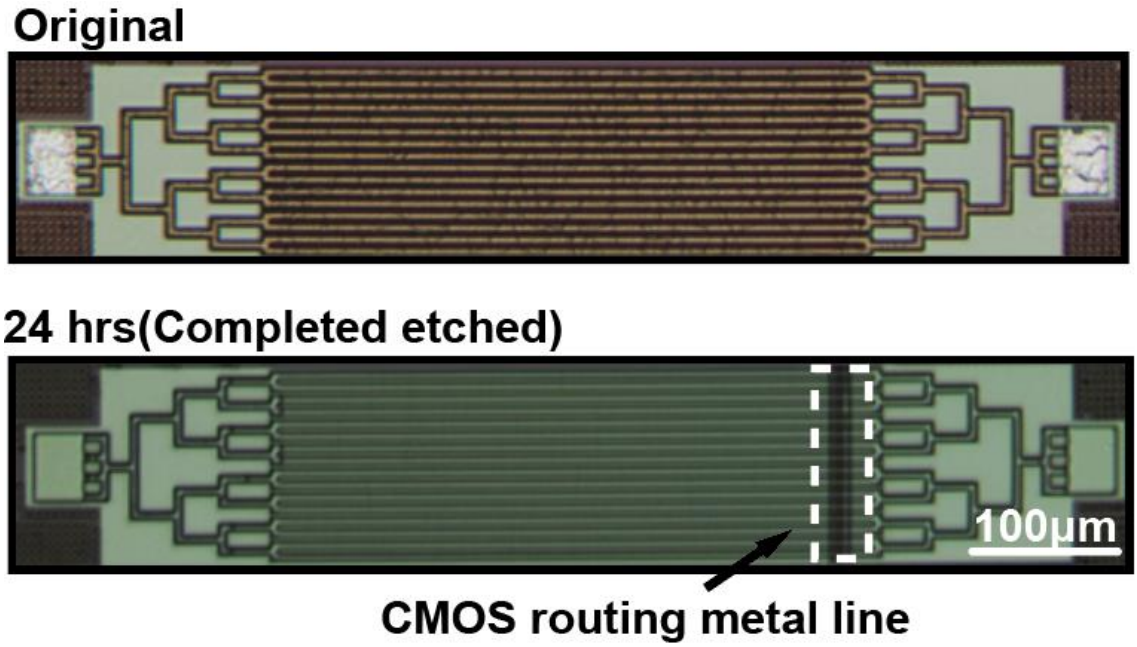

Fig. 27. The before and after optical image of a 16-channel splitter.

2.5.3 3D fluidic channel by the stacked metal layer

This study aims to explore the possibility of making the microchannel down to lower metal layers. In this case, it's potential to develop the device incorporating a "nanopore-

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like” device by the via structure. There has been significant interest in using nanopore sensors to detect individual nucleic acids and proteins at a high throughput rate, without requiring chemical labels or complicated optical equipment [21]. There is a published patent related to the combination of nanochannel in a CMOS chip for single molecule sensing. The patent is a perforated metal oxide semiconductor (MOS) structure that can be used to detect single biomolecules, viruses, or single cells. This structure includes a nanochannel that runs through a sensing region, allowing a solution containing particles to pass through the perforated MOS sensor. The structure also has first and second terminals that can measure electrical parameters that indicate changes in the electrical characteristics of the solution as the particle moves through the perforated MOS structure [22].

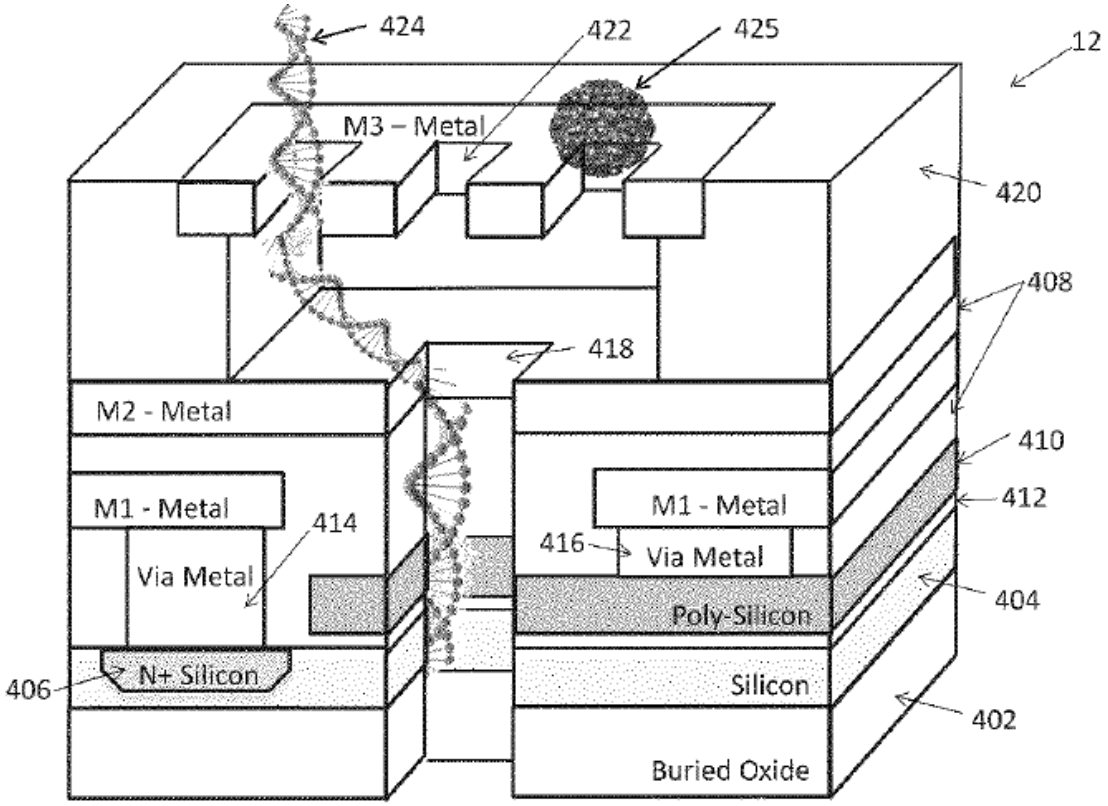

Fig. 28. The proposed device concept of perforated MOS structure for single biomolecule detection.

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In our testing structure, we use a stacked structure from M6 to the M1 layer to see the etching feasibility. Fig. 29 demonstrates the optical image of a multi-layer structure and the cross-section illustration, which ranges from M6 to M1. It is noteworthy that the CMOS vias with a dimension of 260 × 260 nm^2 can be eliminated down to the lower metal layer using the aluminum etchant. Furthermore, the copper etchant also shows a higher etch rate by 5× and an even greater ability to remove the metals completely with a sharper line edge, as shown in Fig. 30.

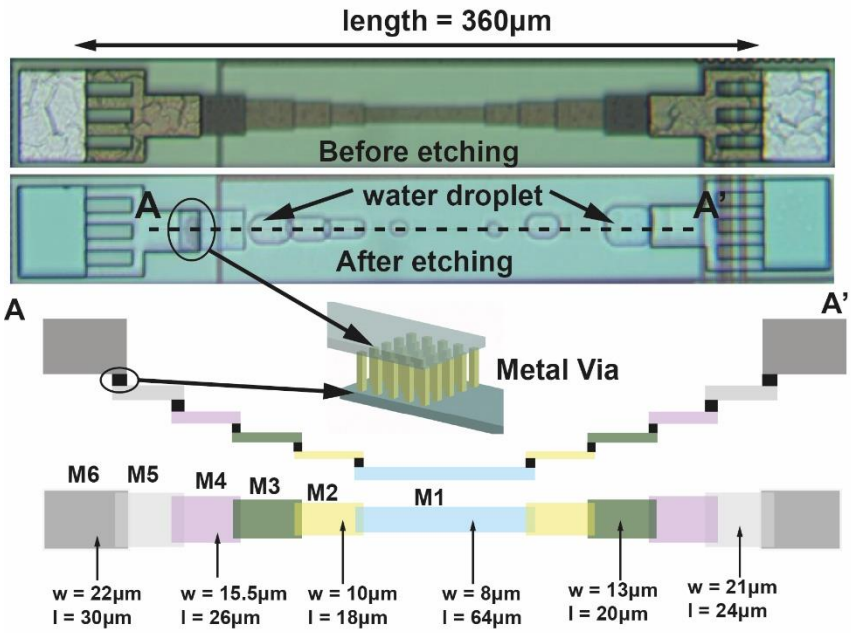

Fig. 29. 3D fluidics using multi-layer metallization.

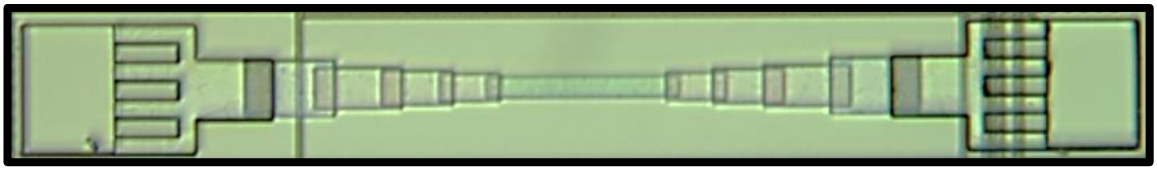

Fig. 30. The same 3D stacked structure etched by the copper etchant.

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2.5.4 Resistive pulse sensing channel

This component is a channel with varying widths that are specifically designed for resistive pulse sensing (RPS). Similar to the concept mentioned above for the nanopore device, RPS is a method used to detect and measure the size of particles that are flowing through the channel by analyzing changes in ionic resistances when a particle passes through the narrow section of the channel[23]. To implement RPS, two-channel segments that are 2.6μm wide and 10μm long are incorporated into a fluidic channel that is 10μm wide. Fig. 31 shows that the metallic elements have been fully removed.

Fig. 32 shows the testing schematic. Two 250-μm diameter Ag/AgCl electrodes are inserted at both the inlet and the outlet, and the DC ionic resistance across the fluidic channel is measured through a transimpedance amplifier (IV204F3) at a gain of 4MΩ. A flowing particle/bacterium through the constriction zones creates an increase in the ionic resistance, and is registered as voltage pulses whose pulse-widths depend on the flowing velocity. The setup and measurement results will be discussed in Section 2.8.

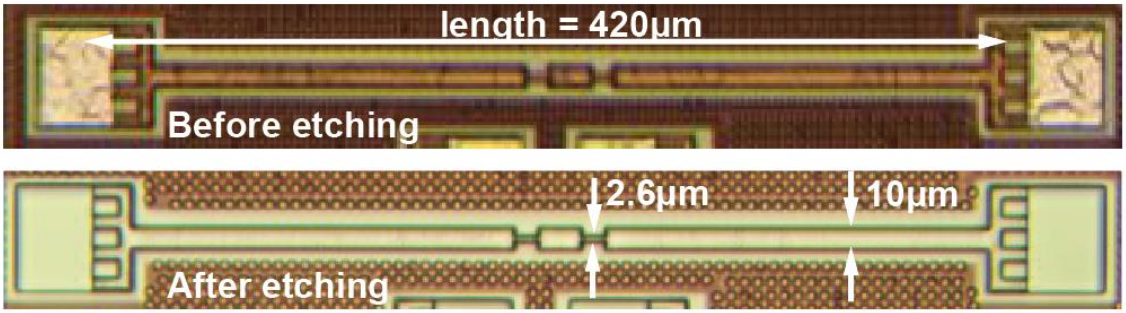

Fig. 31. A width-varying channel for resistive pulse sensing (before and after etching).

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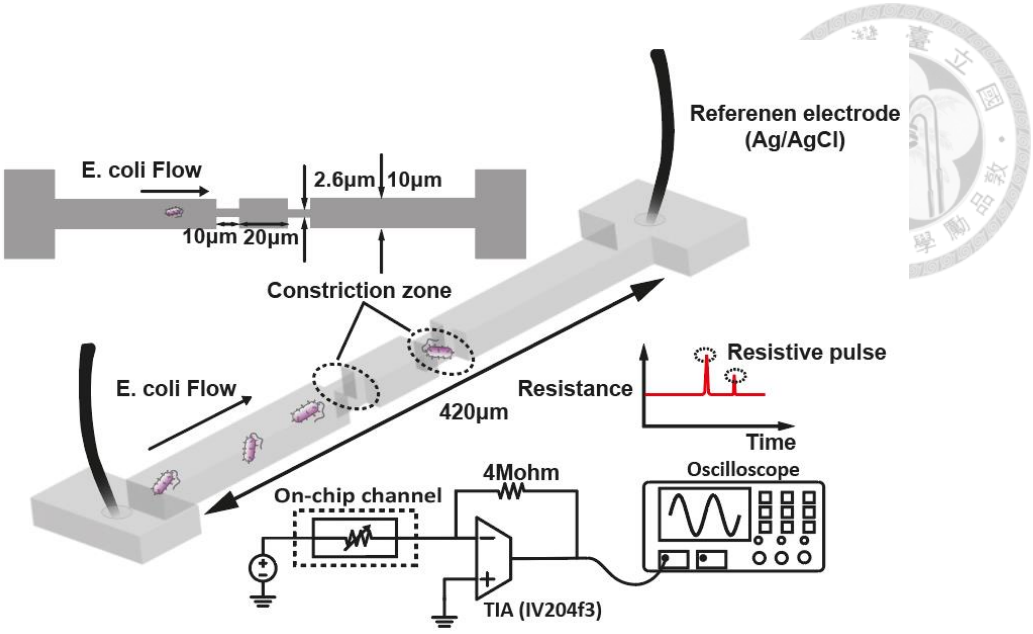

Fig. 32. Resistive pulse sensing system schematic and its sensing mechanism.

2.5.5 Sheath flow channel

Concentrating particles into a narrow stream is often a required step before counting, detecting, and sorting them. Microfluidic devices employ different methods to focus particles, and these methods can be categorized into two types: sheath flow focusing and sheath-less focusing. Sheath flow focusers use one or more fluids to surround the particle suspension and compress it, resulting in the concentration of the suspended particles. To combine this feature with our CMOS-embedded microfluidics, we explored the device shown in Fig. 33. In our experiments, there was a bottleneck in the etching process. Fig. 34 illustrates the etch rate difference existing in the sheath channels and the main channel. With such a difference, the sensing electrodes will be damaged before the hollow channels are formed. This issue may be addressed by opening some intermediate pads for the etching efficiency of long channels, and they will be sealed by PDMS as fluidics flow through.

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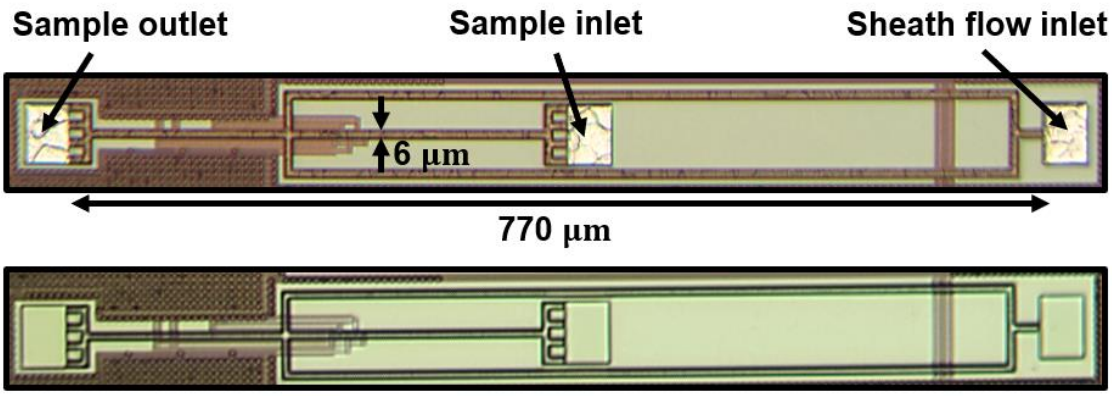

Fig. 33. The fluidics channel with sheath flow inlet (before and after etching).

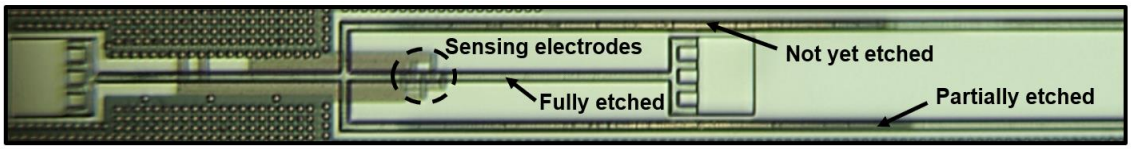

Fig. 34. The etch rate difference lying in the sheath channel and the main channel.

2.5.6 Serpentine channel

Micromixers are essential parts of microfluidic systems and come in various forms. An efficiently designed micromixer has the potential to decrease both the analysis duration and the space required for a lab-on-a-chip system. In microchannels, the small size and low flow velocity result in low Reynolds numbers, and there are no significant macroscopic turbulent fluctuations in the mixed fluid sample at the microscopic scale. Fig. 35 shows the overall structure of the micromixer from [24]. The T-micromixer was used as a basis to create the geometric models, which include two inlets, a structural design area, and an outlet. Based on the analysis in [21], the square-wave micromixer is more effective at mixing due to its sharper turns and longer flow path compared to the multi-wave micromixer and zigzag micromixer. Therefore, we adopt this structure as our on-chip micromixer.

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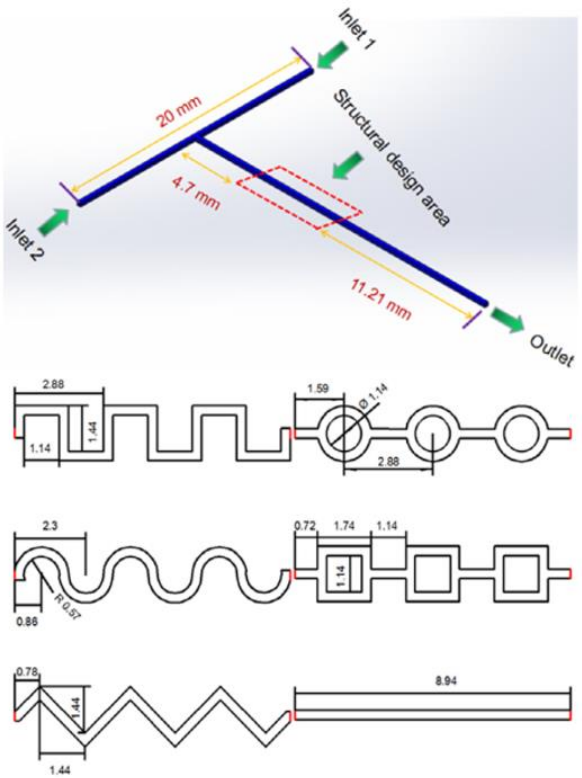

Fig. 35. Schematic diagrams of the micromixers structural design [24].

Fig. 36 shows the optical images of our proposed serpentine micromixer. We use M6 to M4 to prolong the mixing path. Yet, due to the longer path and multi-layer, the pressure drop in the microchannel was too large to make the etchant continue etching. So from the photo, we can observe the partially etched region even etched several weeks. To cope with this issue, we may test the feasibility and efficiency of this concept without multi-layer, so that the microchannel can be successfully formed.

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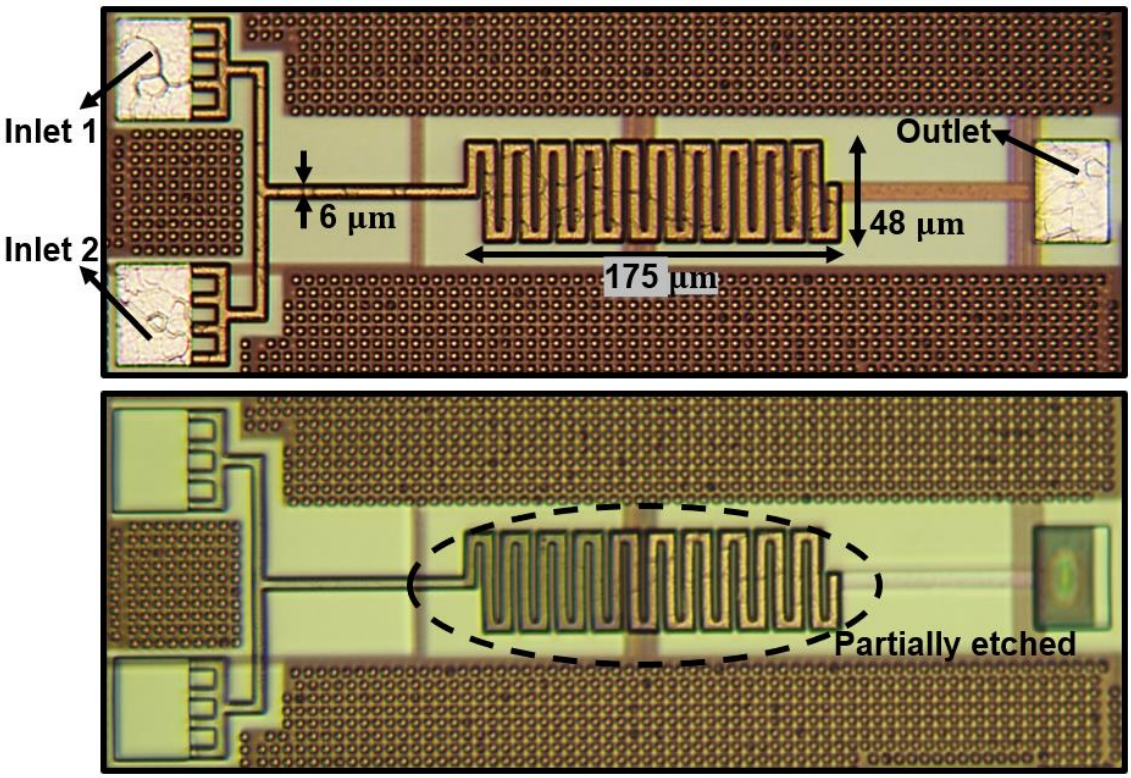

Fig. 36. The serpentine micromixer structure (before and after etching).

2.6 Active testing blocks

This section describes the testing blocks that are not just passive channels but are designed for electrical measurements and sensing. It includes: on-chip sensing electrodes, a transistor array with different device parameters, a shift register, and a transimpedance amplifier as an analog front-end.

2.6.1 Embedded sensing electrodes

Incorporating electrodes into our chip-embedded microfluidics is essential for sensing applications. In this regard, we have explored three different electrode configurations (Fig. 37). The first approach involves placing the electrodes on the same metal layer as the fluidic channel but without direct contact with it. While this approach separates the

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formation of the channel from the embedded electrodes, there is a significant limitation in sensing sensitivity due to the gap between the electrodes and the fluidic channel. Our analysis indicates that a 2.5 μm gap can reduce sensitivity from 69.6% to 10 ppm (as seen in Fig. 37(a)). An alternative method is to position the contact electrodes in the same layer as the fluidic channel and place the junction in the center of the inlet and outlet. However, this approach is not feasible due to a non-uniform etching phenomenon that creates a shallow passageway at the ceiling of the M6 layer, followed by downward etching (as shown in Fig. 38(a)), which removes all the electrodes before the hollow channel is formed. To overcome this issue, we developed the third electrode configuration, taking advantage of the etching behavior and using M56 "vias" as sensing electrodes (as shown in Fig. 37(b) and Fig. 38(b)). The vias are located at the bottom of the fluidic channel and remain protected until the aluminum is removed. Noted that vias are typically made of compound metals such as tungsten and have been previously studied as sensing electrodes for pH sensors.

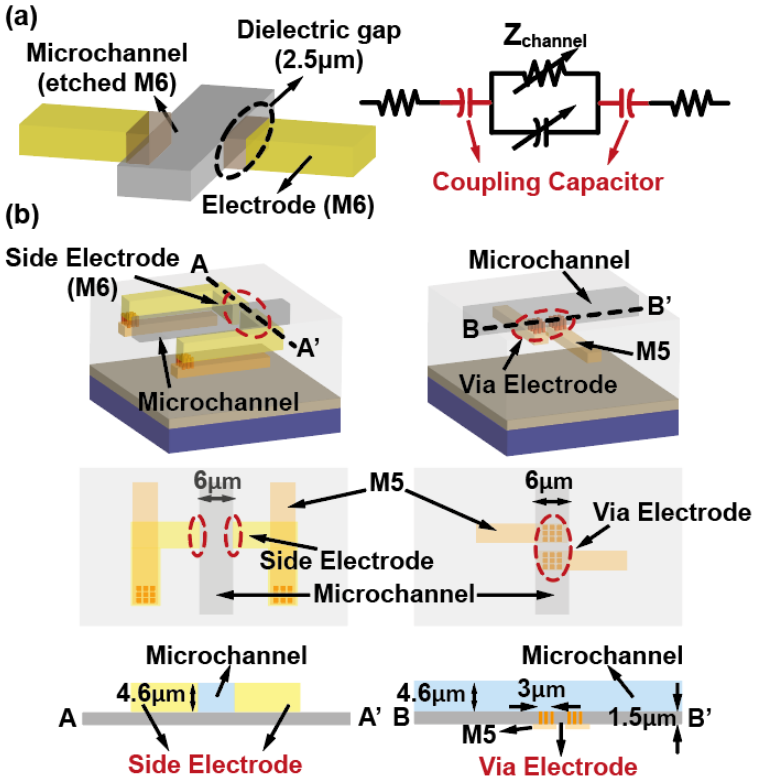

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Fig. 37. (a) Non-contact electrode configuration. The sensitivity is degraded due to the presence of the coupling capacitors. (b) Two contacting electrode configurations: transverse “side” electrodes and the bottom “via” electrodes.

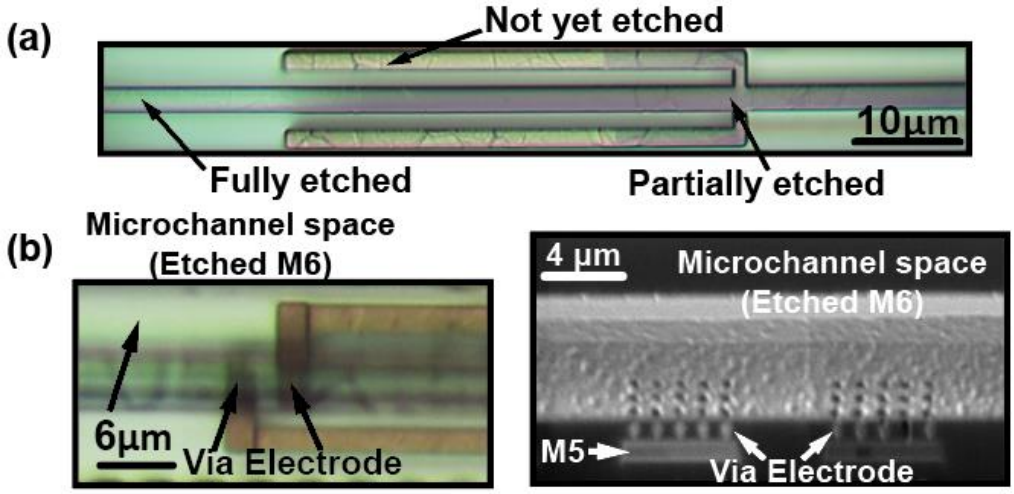

Fig. 38. (a) The image of the side-electrodes fluidic structure. This image shows that the removal of routing aluminum is highly non-uniform. (b) The optical image and SEM images (tilted by 30°) of the via electrodes.

2.6.2 Transistor array

We study the impact of etchants on the transistor characteristics after prolonged immersion of the CMOS chip in the etchant medium. This is crucial to validate the feasibility of future fluidics/electronics integration. The schematic of those transistor array testing is shown in Fig. 39. There are sixteen transistors in total, which are all NMOS with two sizes (4μm/1μm and 4μm/0.18μm); in addition to the size difference, we also explored the lower and higher threshold voltage devices, which are NMOS2v and PMOS3v. Those switches are implemented with 8μ/0.18μ NMOS. The Id-Vg and Id-Vd curves are shown in Section 2.8.1.

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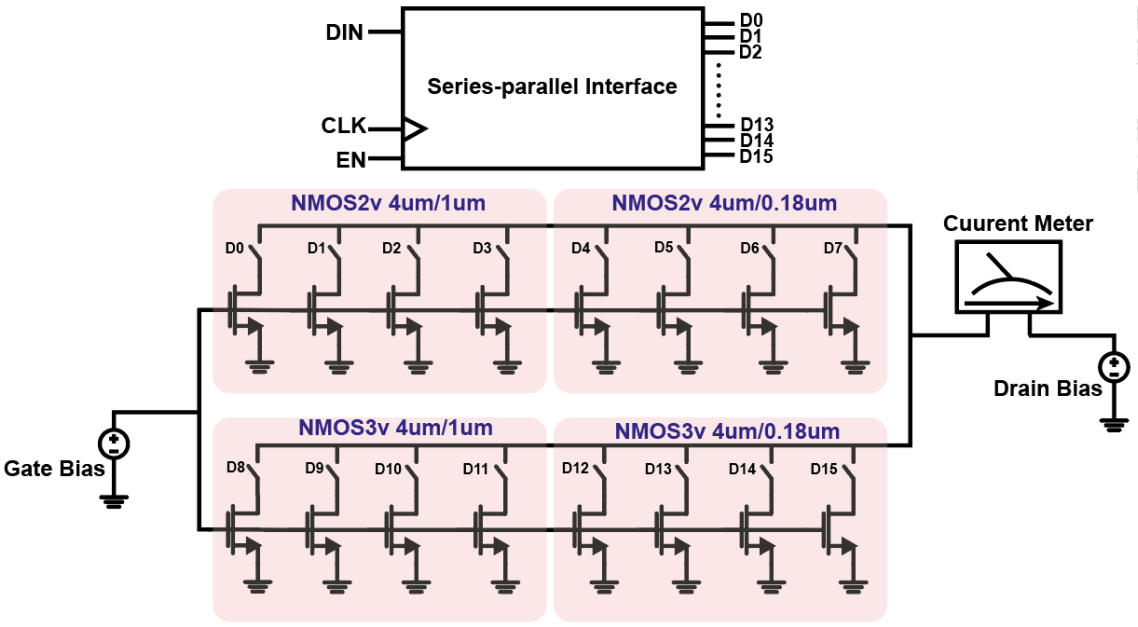

Fig. 39. Schematic of transistor array for device characteristic testing after the etching process.

2.6.3 Transimpedance amplifier sensing chain

The whole signal chain is shown in Fig. 40. As a proof of concept, we started by integrating parts of blocks for the sensing chain. In this chip, we implemented a transimpedance amplifier as the preliminary testing circuit, integrated with the embedded microfluidic channels.

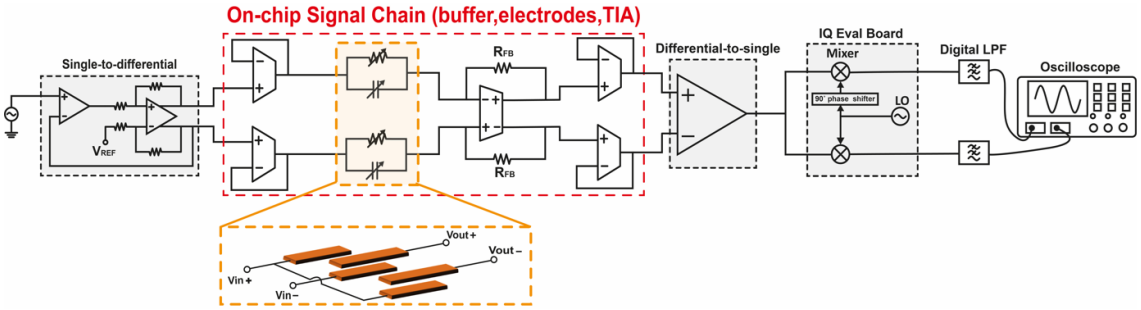

Fig. 40. The sensing chain for impedance analysis.

A system's performance depends on various factors, including power, noise, gain, area, and swing, and there is a trade-off between these factors. The front-end amplifier plays a

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significant role in determining the overall noise of a sensor read-out system. To ensure that the noise is kept below a specific target, a substantial amount of power should be used in the first stage. One way to minimize thermal noise is by biasing input transistors in weak inversion or even deep subthreshold region, which can maximize gm/ID [25]. Moreover, the current-reuse structure [26], has become widely utilized in biomedical applications. The current-reuse amplifier faces two main limitations - restricted output swing and limited open-loop gain. While techniques such as cascoding transistors can enhance the gain, the overall peak-to-peak output swing will remain restricted to $6V_{od}$ below VDD.

For applications involving electrochemical analysis, a wide frequency range from 1 Hz to 1 MHz is necessary to examine the behavior of the system, making the dynamic range a crucial specification. On the other hand, impedance-based flow cytometry requires real-time measurements and operates at one or two fixed frequencies to evaluate particular physical properties of cells instantly. In this case, noise performance is more significant as the size of cells is small compared to the channel.

To cancel the baseline current as described in Section 1.1.3, we adopt source-differential architecture as our sensing analog front-end. We aim to make the bandwidth 1MHz and gain 1MΩ; meanwhile it should be a low-noise design. The TIA employs a current-reuse cascode amplifier (Fig. 41). The simulation results are shown in Table 3.

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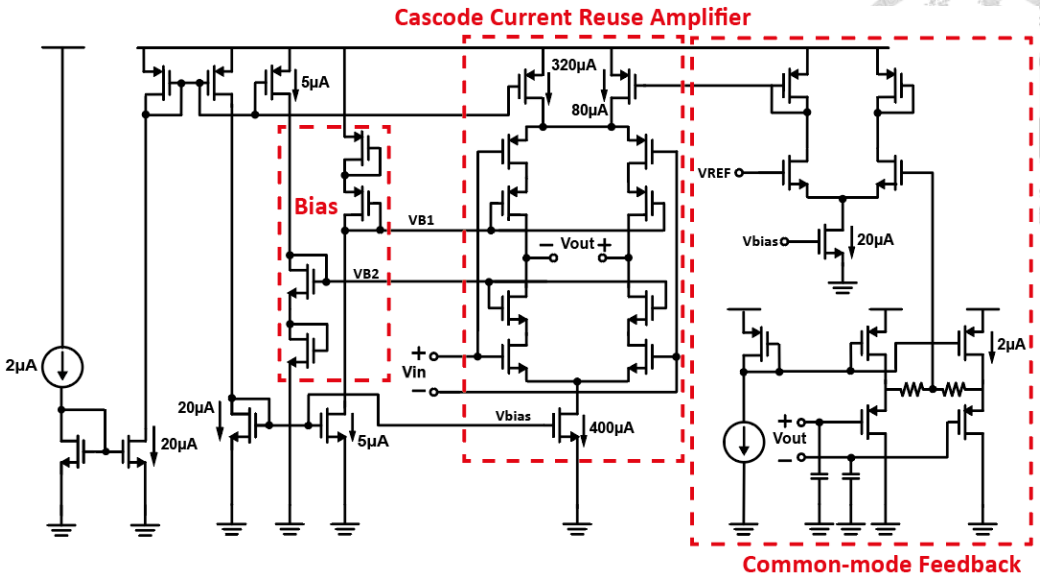

Fig. 41. Cascode current-reuse amplifier.

Table 3 On-chip TIA simulation results.

Parameter	Result
DC gain	126 dB
Bandwidth	1.5 MHz
Input-referred noise	0.39 nArms
Phase margin	75.3°
Linear dynamic range	-300~300 nA

To begin with, we estimated the impedance variation modeled by a simplified approximation. We see the microchannel as a bulk resistor and took the value of 30mS/cm for the conductivity of 20× SSC. The calculated results of the volume and resistance changes from various sizes of particles are shown in Fig. 42. Our target sensing cell is E. Coli, which is in the size of about 2μm, so the pinpoint is on 2μm-diameter.

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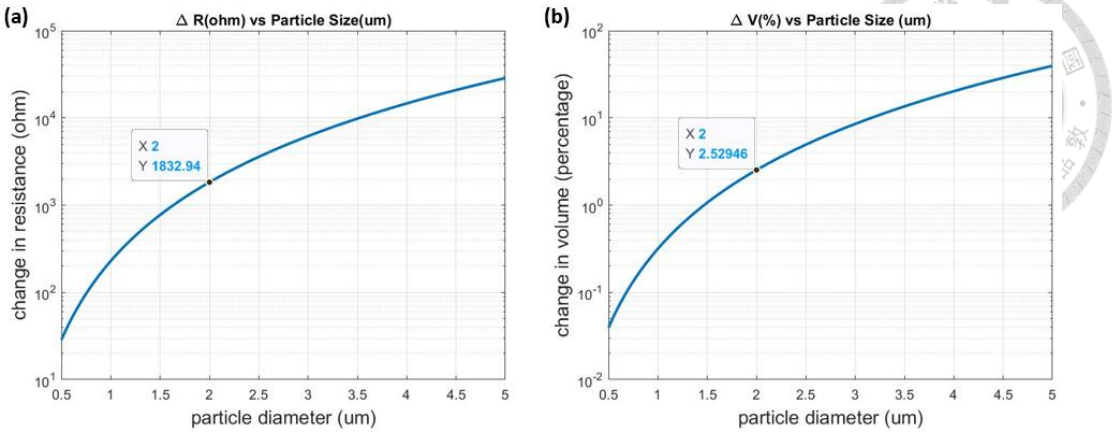

Fig. 42. Preliminary estimation for the perturbation based on the conductivity and the electrode geometry.

The impedance model of sensing electrodes is illustrated in Fig. 43. We assume the bacteria's effect is the variation of channel resistance. Fig. 44 demonstrates the simulation results of extracted signals as the impedance is perturbed by particles flowing through the channel. Assuming the impedance change by 2.5%, then the estimated peak-to-peak signal will be about 150mV.

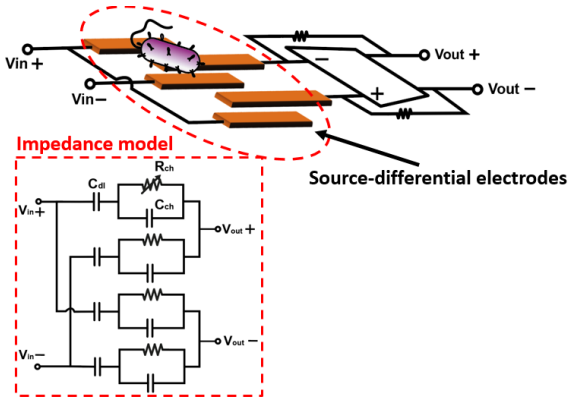

Fig. 43. Schematic of impedance model.

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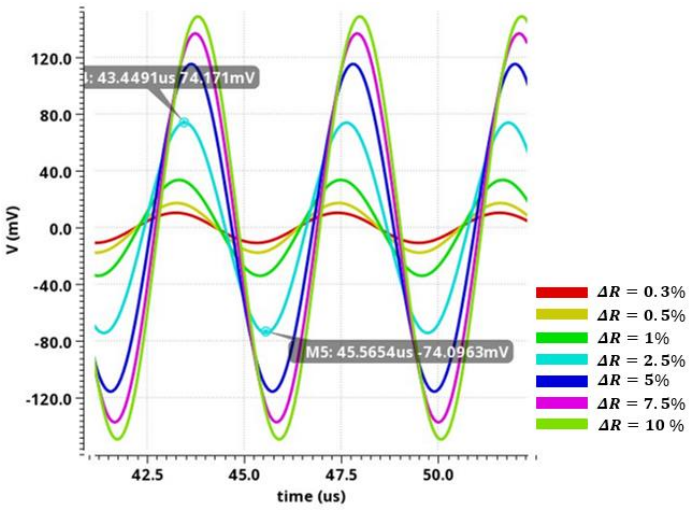

Fig. 44. Impedance model simulation for estimating the order of extracted signal.

2.7 System integration and packaging

The PCB design for the above testing circuits was implemented by Altium Designer. We used the mother-board and daughter-board as two separate modules for the convenience of post-processing and soldering works, which means that we can do any packaging test on the daughter-board without any concern about the soldered IC consumption. The former contains most of the commercial IC for different functions, and the latter contains mainly contains our CMOS chips. The main signal chain for impedance analysis is shown in Fig. 45. In the mother board, there are three blocks for the main signal chain: single-to-differential stage (OPA1177 & AD8476) to convert the input signal for the differential input of on-chip TIA, instrumental amplifier as differential-to-single stage (AD8231) to convert the output signal from on-chip TIA for the single input of I/Q demodulation evaluation board, and the buffer (OPA4354) before entering I/Q demodulation evaluation board. In addition to the main signal chain blocks, there are also LDOs (low-dropout regulators) for plenty of power supplies and one level-shifter for the VDD level tuning from 3.3V (FPGA)/ 5V (Arduino UNO) to 1.8V (on-chip circuits). The overall 3D layout view of the mother-board and daughter board is demonstrated in Fig.

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46. There are some criteria as we designed this PCB. Our on-chip testing circuit is a differential transimpedance amplifier, so it's required to make all the wires of differential signals match each other. The Tx/Rx SMA should be close to the header as possible to minimize the cable and wire length (Under the premise of without affecting the connection of the 40-pin header for the mother-board and daughter-board connection). We also set enable/disable for each IC we used and made them programmable architectures if possible for ease of debugging. In addition to the above, we added 10μF/1μF/100nF decap to all the supply voltage and bias voltage pins for stabilizing the voltage. Last but not least, we used the ground plane for proper isolation between the signal lines to avoid measuring the fringing capacitance between two wires.

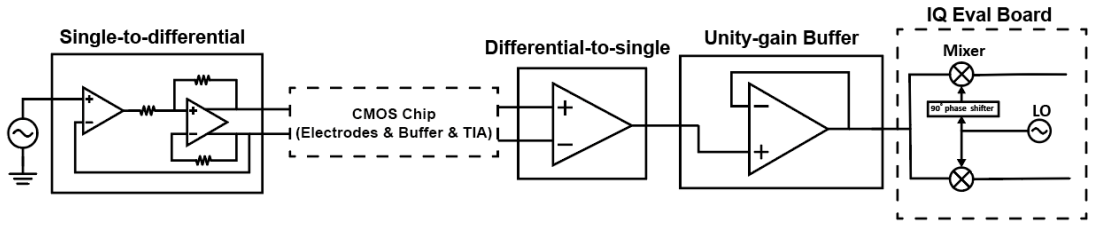

Fig. 45. The block diagram of the main signal chain. Blocks in the solid box are on-board, and those in the dashed line are off-board.

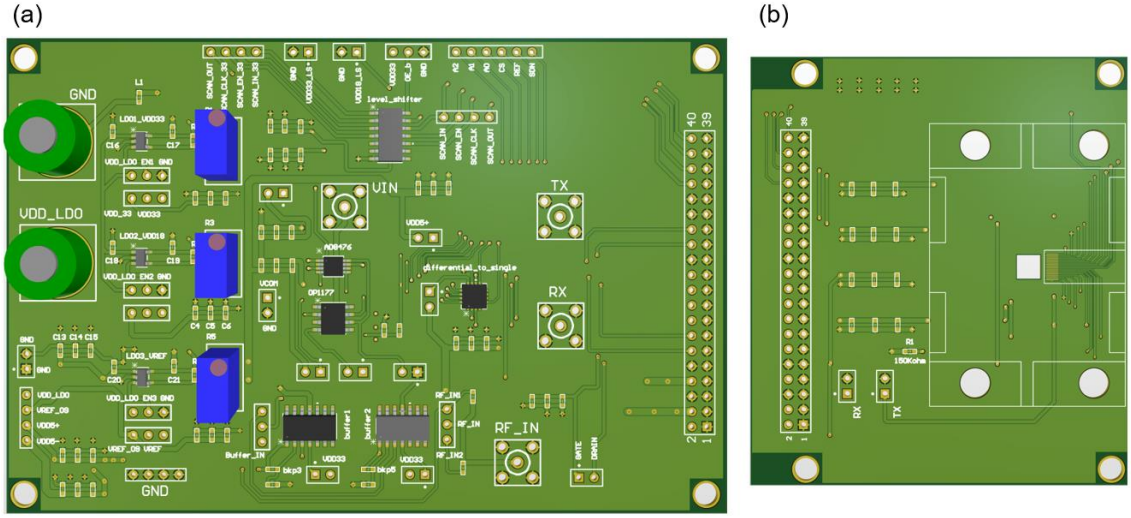

Fig. 46. 3D layout view of (a) mother-board and (b) daughter-board.

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After introducing the components on the mother-board and the criteria we followed, we'll discuss some concepts for the daughter-board. We see the daughter-board as a consumable, so we don't put many components on it except those decaps, two pins for probing, and one resistor for bias. In addition, there is one drilled square hole for the post-processing of packaging using epoxy, which will be discussed in Section 3.3 for more details. Furthermore, four drilled holes are for M5 screws as part of the later integration of the microfluidics module. Finally, both mother-board and daughter-board have holes around each corner for the copper pillar foundation.

2.7.1 Microfluidics preparation

For the accurate delivery of fluid into the on-chip channel, we designed the film mask for the fabrication of the PDMS mold. To well match the inlet and outlet with our layout, we used AutoCAD to define each spacing and area then drew the mask layout as shown in Fig. 47.

The geometries are mainly decided by how to avoid any overlapping of the channel across two different on-chip channels. If there is overlapping, the liquid will flow through unexpected channels without control. From Fig. 47 below, we can see that those structures are all single-ended instead of traditional fluidic channels, which must contain an inlet and outlet in one structure.

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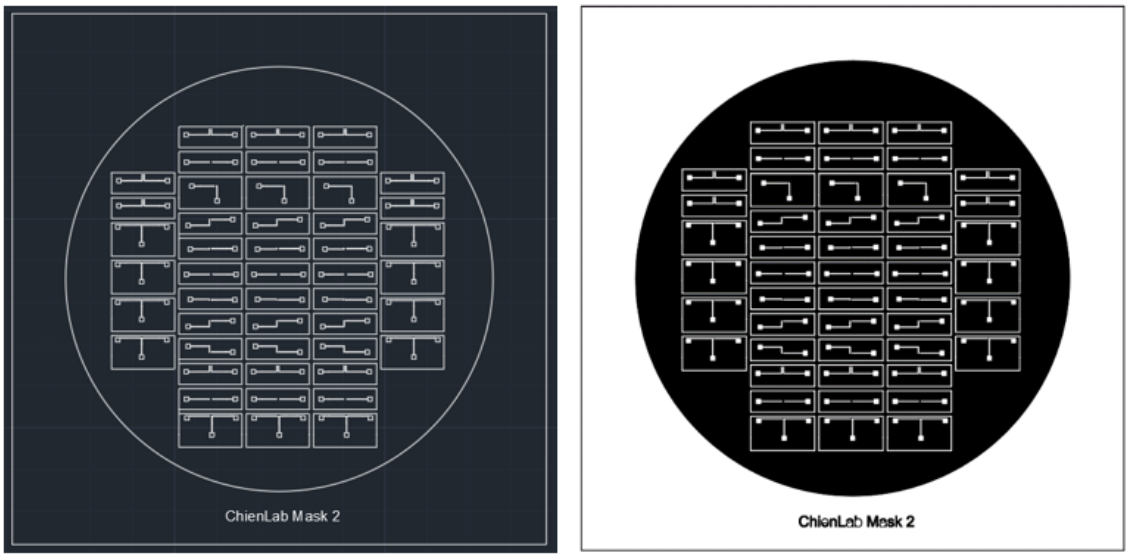

Fig. 47. The film mask layout designed by AutoCAD (The left is the AutoCAD image, and the right is the real film mask layout image).

2.7.2 SU-8 lithography

After getting the designed mask, the next step is to fabricate the mold for PDMS the microfluidics channel by SU8 photolithography. We used SU8-2050 for our wafer patterning. The process flow is shown in Fig. 48. We start the process with piranha cleaning to ensure the wafer surface's quality. That is, we can avoid defects or bad adhesion by adopting piranha cleaning.

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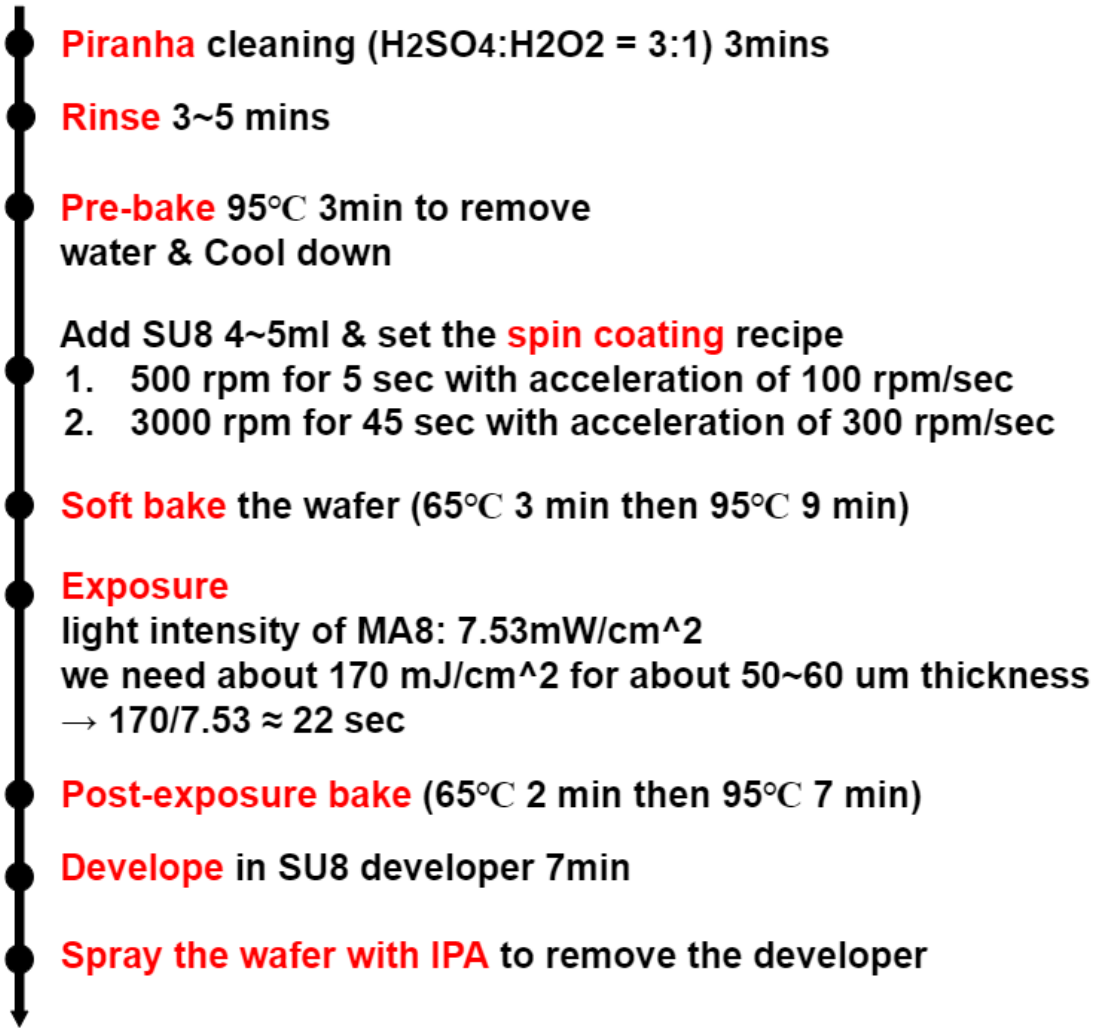

Fig. 48 The process flow and parameters for SU-8 microfluidics fabrication.

After rinsing to remove all residue of piranha, we prebake the wafer 95℃ for 3 mins to thoroughly remove the moisture from the wafer surface. Then, standard lithography processes including spin coating, soft-bake, hard-bake (post-exposure bake), and development are executed step-by-step. Lastly, use IPA to remove the developer and rinse the wafer with water. Fig. 49 demonstrates the images of steps in the whole process flow. And Fig. 50, shows the results of our SU8 patterns on a silicon wafer. We can see the single-ended pattern for the well-defined fluidic channel. After preparing all the needed materials mentioned above, we are ready to make the PDMS fluidic channels.

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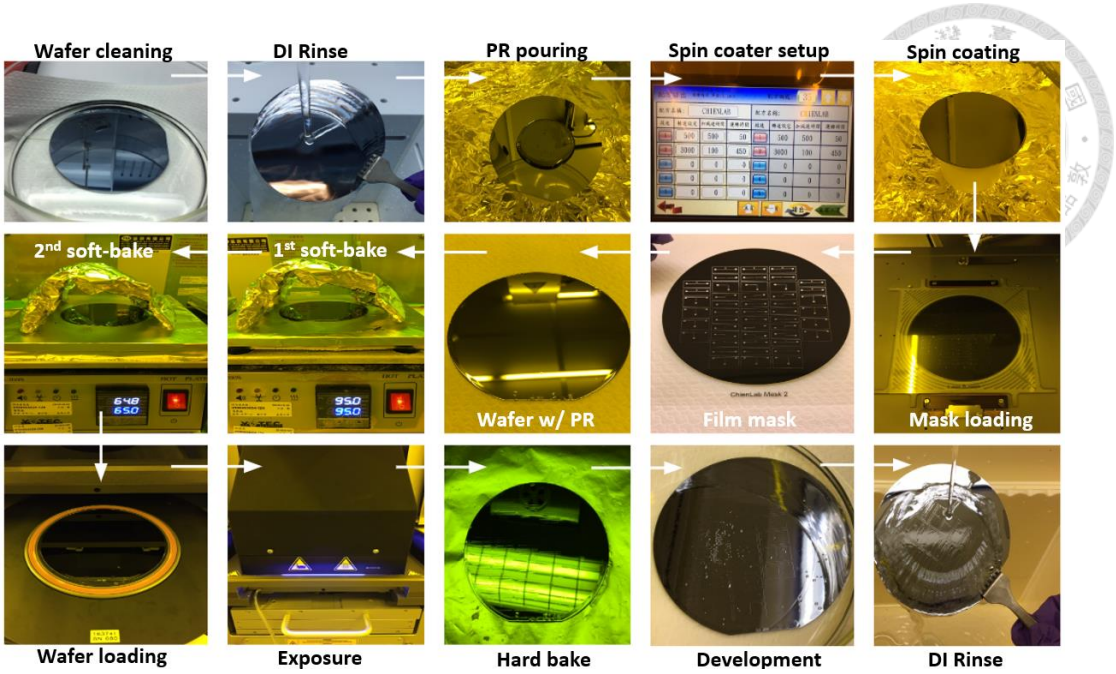

Fig. 49. Photos of each step in the SU-8 lithography process.

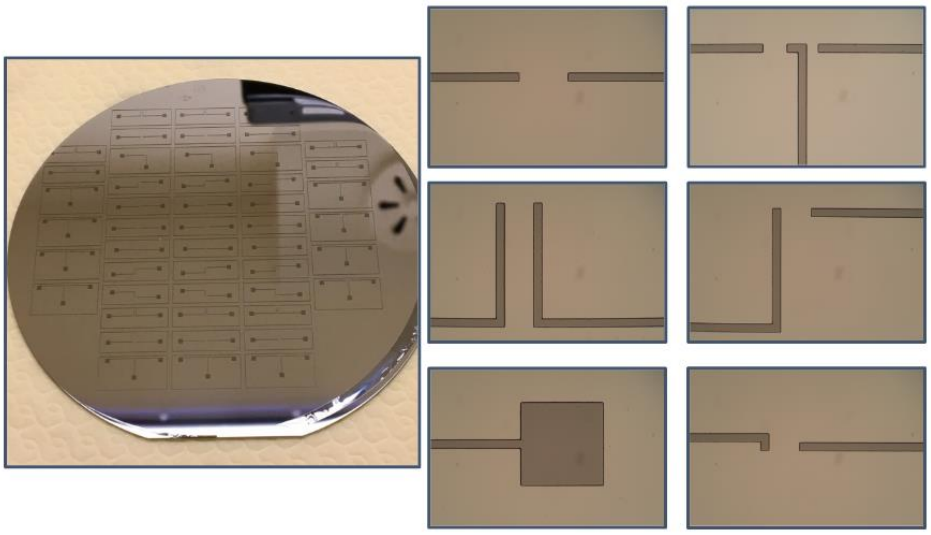

Fig. 50. The fabricated wafer and OM images of our designed pattern.

2.7.3 CMOS with epoxy packaging

In this paragraph, we will introduce the whole process flow of the CMOS packaging using biocompatible epoxy (Epo-Tek 302-3M). The overall packaging process involves two parts: (1) 1st part for CMOS chip and PCB modules co-planarization and (2) 2nd part for bond-wire protection. In the first part, we start with using multiple layers of Kapton tapes to stick on the PCB, so that they can act as spacers for later epoxy flow between

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PDMS and PCB. The second step is to make the chip lie on a PDMS slab and use mechanical force to bind the PDMS and PCB by binder clips. Lastly, after we confirm the placement of our chip, we use a needle to give stress from the backside of the chip to the chip's surface, so that we can make sure that the tightness of the PDMS surface and chip top surface. After completing the above preparations, we inject epoxy from a drilled hole on PCB and then wait for the solidification. The planarization is followed by the integration of PDMS, acrylic board, screws, and nuts for the final packaging. Finally, the whole packaging setup will be like Fig. 51(a). It shows the epoxy-packaged CMOS chip along with PCB. And the usage of the acrylic board, screws, and nuts is for the PDMS integration. We need to exert a strong enough force to avoid liquid leakage from the PDMS and PCB interface. In Fig. 51(a), we can also see the inlet and outlet with tubes for solution delivery. The red and blue dyes are for the recognition of the solution replacement procedure. Note that for the embedded electrodes sensing test, we used a reservoir to carry different solutions for the ease of sample replacement. (Fig. 51(b))

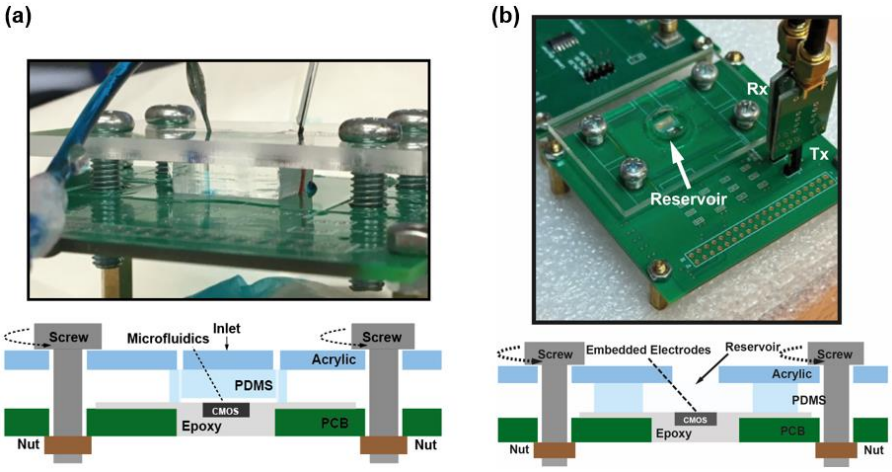

Fig. 51. The packaging of the fluidics system for (a) normal fluid delivery and (b) a reservoir for embedded electrodes sensing purposes.

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2.7.4 Electrical module integration

The instrumental module integration for the on-chip transimpedance amplifier (TIA) circuit is shown in Fig. 52. The PCBs are introduced in section 3.1. AD8339 is an evaluation board containing double-balanced Gilbert mixers to perform IQ demodulation functions. We use Digilent Analog Discovery2 and Arduino UNO as the two main microcontrollers. They offer SPI control and supply voltages for the evaluation board of IQ demodulation and several signals, like RF_IN and the signals for on-chip scan-chain (serial-in, parallel-out). The Keysight E36313A and Picoscope 5444D are the power supply for LDO and the oscilloscope for output signal monitoring respectively.

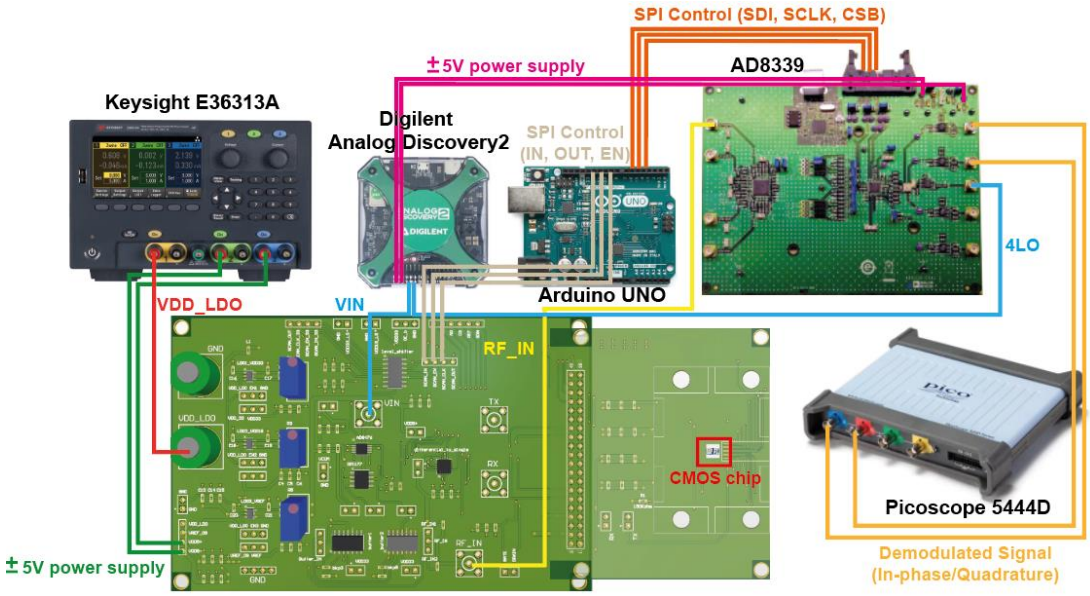

Fig. 52. The connection between each module for measurement integration.

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In this paragraph, we present some measurement results of the impedance analyzer module introduced above. Fig. 53 shows the measurement results of the input signal (241kHz, green wave) and demodulated signals (1kHz, blue and red curves). The conversion gain is about 0.85, which is consistent with the datasheet. The noise measurement is shown in Fig. 56, which shows 0.44mV as the input-referred noise and it's about 4× larger than the nominal value. The reasons may come from the non-ideal noise shielding setup for the measurement, so the noise of the power-line and instruments will also come into play. Fig. 55 demonstrates the dynamic range testing results of the impedance analyzer signal chain. Its dynamic range is about 200mV and the gain will be reduced by about 20% as the input is beyond this range. Lastly, Fig. 56 presents the functionality measurement of the digital control for the serial peripheral interface (SPI) programmed by an Arduino UNO.

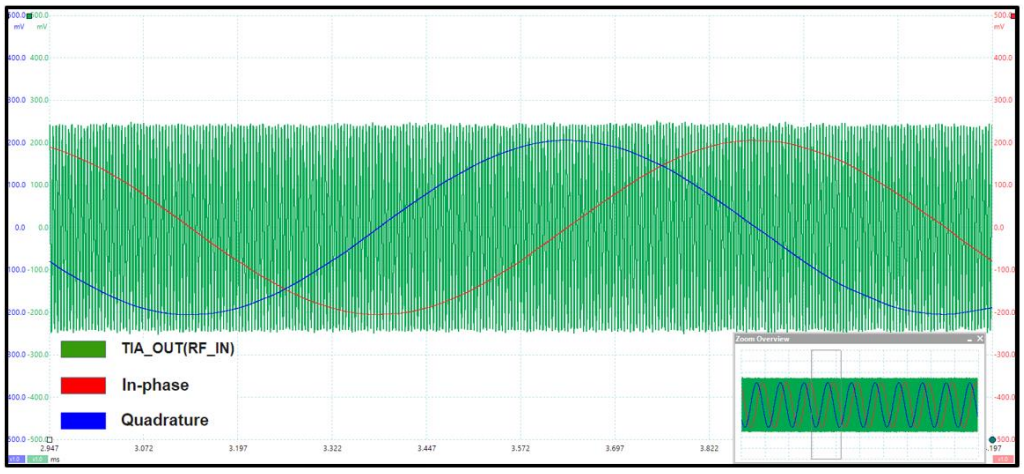

Fig. 53. Function verification of I/Q demodulation board.

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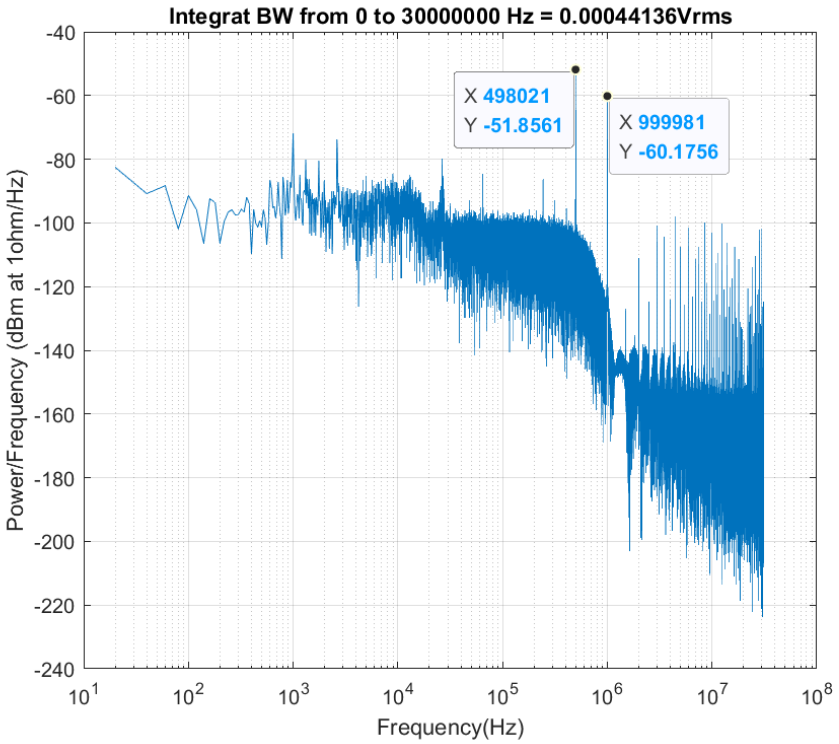

Fig. 54. The noise power spectral density of the impedance analyzer.

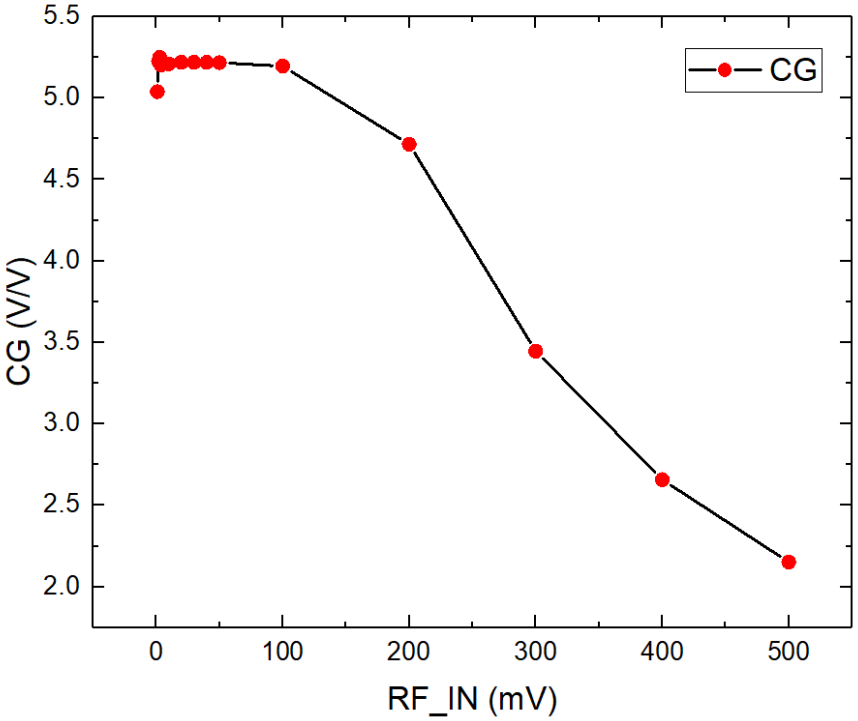

Fig. 55. The dynamic range testing of impedance analyzer signal chain.

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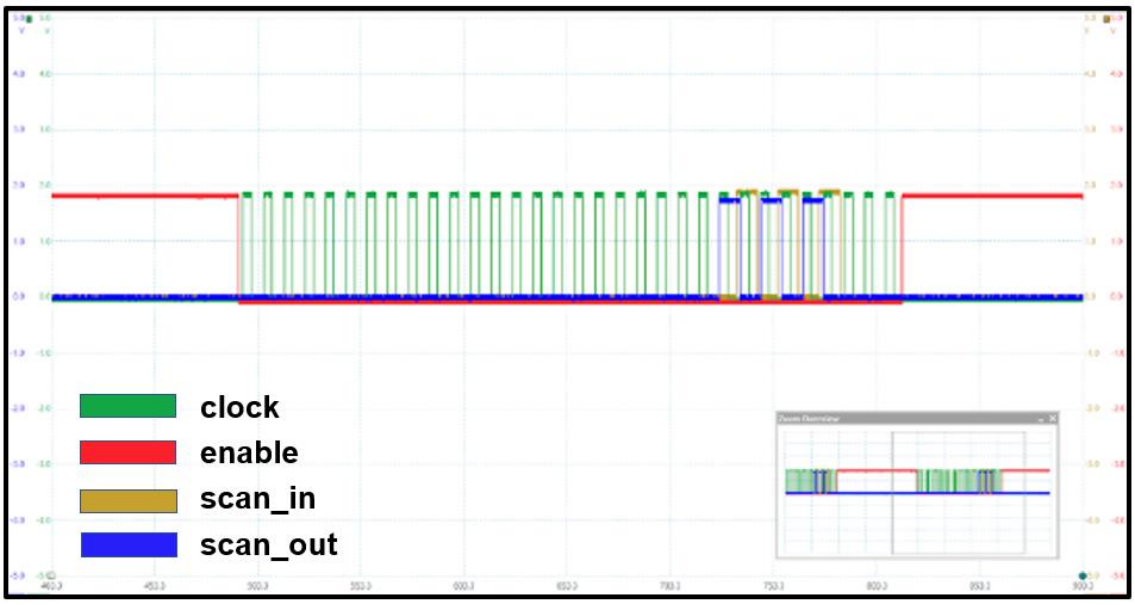

Fig. 56. Digital control verification.

2.8 Measurement results and discussion

2.8.1 Transistor function verification after long-term etching

To verify that our proposed etching process will not damage the on-chip circuits, we used a transistor array to investigate the effect on the device properties as discussed in Section 2.3.2. We utilized Arduino UNO to program the 18-bit series-parallel interface for the switches to decide which current branch to probe. Fig. 57 shows the results of NMOS2v (4μm/0.18μm) transistor Id-Vg curve before and after the etching process. We observed that after immersion in the etchant one day, the transistor's electrical characteristics are almost the same. The average error value is 1.5% compared to the sample without the etching process. The etching time of our regular on-chip fluidic channel geometry is less than 24 hours, so the comparison result demonstrates the feasibility of this process flow.

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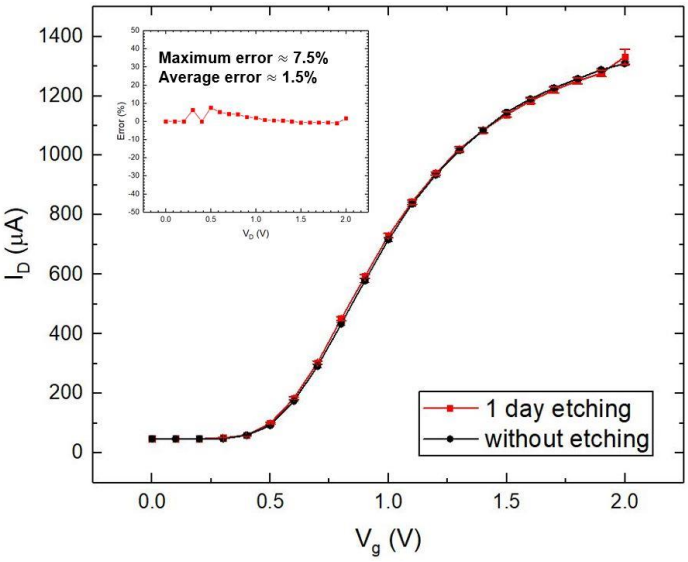

Fig. 57. NMOS2v (4μm/0.18μm) Id-Vg comparison before and after etching.

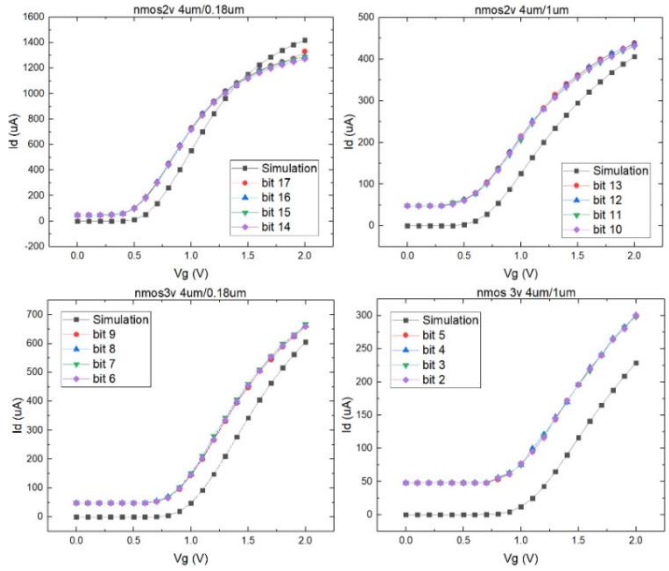

Fig. 58. The Id-Vg comparison between measurements and simulations for different transistor sizes.

In addition to the comparison of before and after etching, Fig. 58 presents the comparison of simulations and measurements between each device size. From the results, we can see there is a relatively constant gap between them. We attributed this to the issue of instrument error because there was 50μA current reading on the panel. We

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also used the Id-Vd curve to see if there is still this offset and the result is shown in Fig. 59, which also shows a relatively constant gap in between.

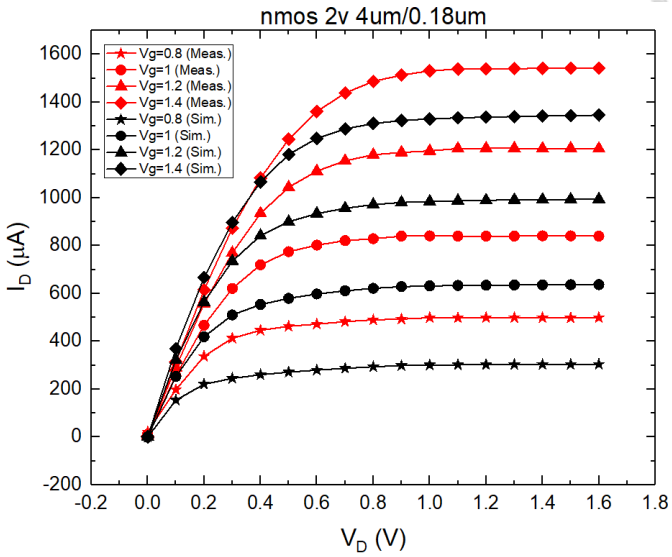

Fig. 59. The Id-Vd comparison between measurement and simulation.

In addition to the analog properties of the transistor discussed above, we also investigated the functionality of the digital block after the etching process. Fig. 60 shows the diagram of a 32bits shift register, which is made up of D flip-flops.

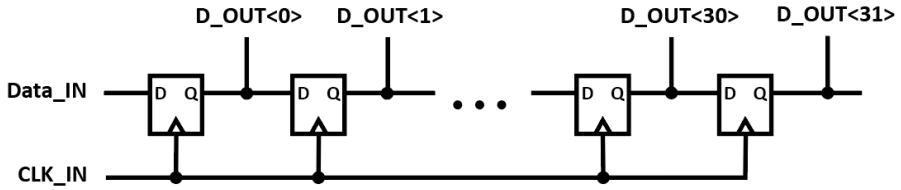

Fig. 60. The diagram of 32bits shift register.

From Fig. 61, we can see that the bit sequence of the shift register won't be affected by the etchant. It demonstrates that the Data-IN and Data-OUT are consistent, just with an unavoidable timing error of less than one clock. Therefore, based on all the above results, we can conclude that our circuits can sustain the etching process without observable damage to the characteristics and functions.

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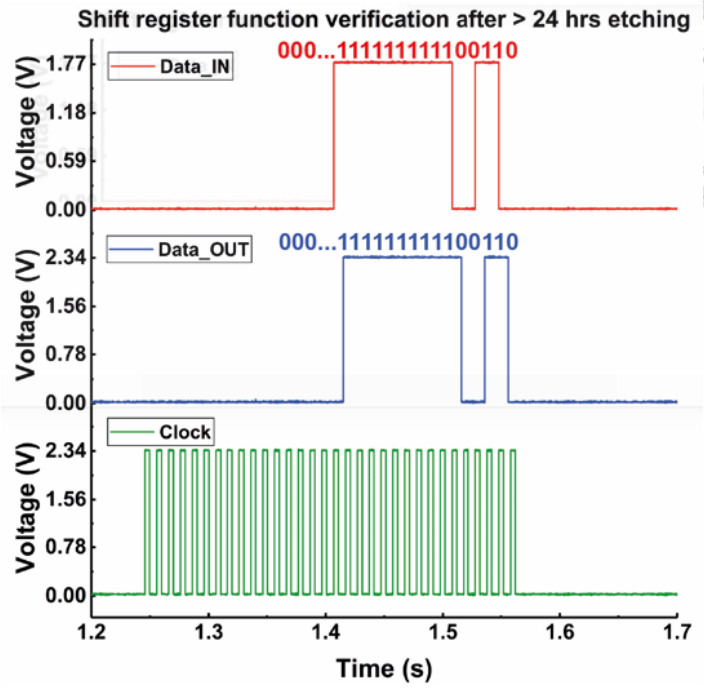

Fig. 61. The demonstration of shift register functionality after 1-day etching.

2.8.2 Resistive pulse sensing

We use our CMOS-embedded microfluidics technology, to conduct RPS on bacteria cells. The ionic resistance of the fluidic channel is measured through a transimpedance amplifier (IV204F3) with a gain of 4MΩ. When a particle flows through the constriction zones, it causes an increase in the ionic resistance, which is registered as voltage pulses. The pulse widths vary depending on the velocity of the flowing particle.

The setup for resistive pulse sensing (RPS) is shown in Fig. 62. First, we use biocompatible epoxy (Epo-Tek 302-3M) to surround and planarize our CMOS chip into a printed circuit board (PCB) (as presented in section 3.3). Next, we sandwich a sample-delivering PDMS between the PCB and an acrylic board. The PDMS is molded from a SU-8 patterned silicon wafer having wide channels (as presented in section 3.2) that overlay with the pads of the fluidic structures. The electrodes for RPS are inserted into

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the Tygon tubing through catheters. All measurements are performed inside a Faraday cage to minimize environmental noise, including those from the 60-Hz power lines.

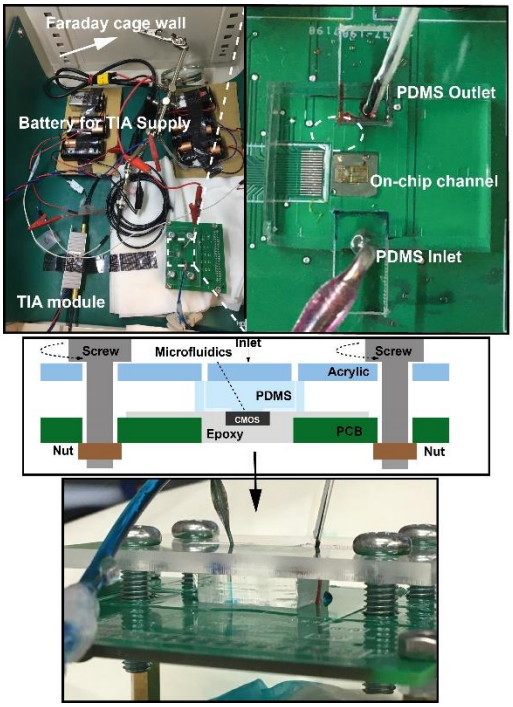

Fig. 62. The setup for RPS measurement.

Fig. 63 shows the RPS results from flowing 1-μm diameter polystyrene beads (Fig. 63(a)) and E. Coli cells (strain pir-116) (Fig. 63(b)) in PBS medium. The particle entering the two constriction zones blocks the ionic flows, elevates the channel resistance, and causes a current reduction. Each pair of pulsing signals in the time-domain waveforms represents one particle flowing through the two constriction zones. The measured pulse width is ~80 μsec, corresponding to 125 mm/sec flow velocity.

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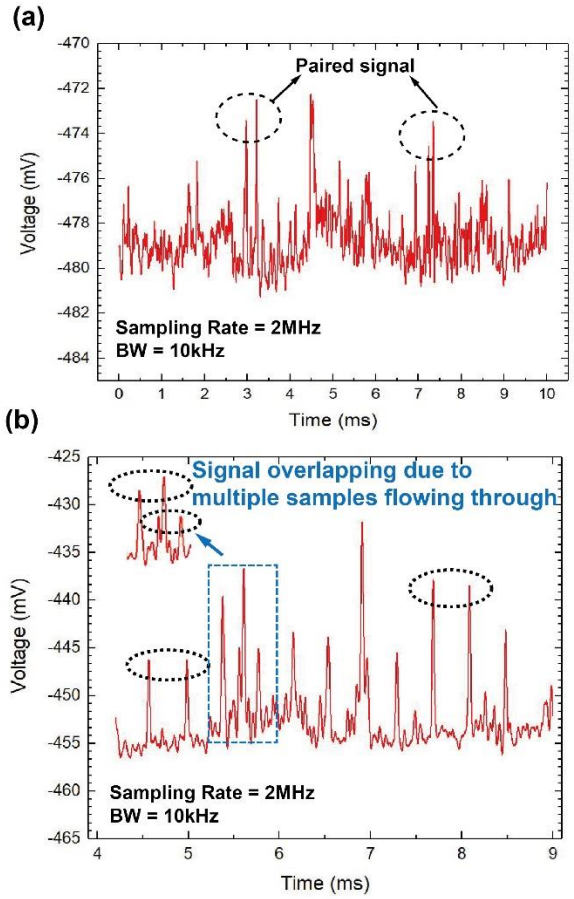

Fig. 63. Resistive pulse sensing (RPS) of (a) 1-μm beads and (b) E. Coli bacteria cells.

2.8.3 Real-time monitoring for embedded sensing electrodes

To avoid excessive etching or damage to the via electrodes, we continuously monitor the impedance between the two electrodes in real time. As shown in Fig. 64(a), we have a schematic and an equivalent circuit model. Initially, both electrodes are connected by the metallic channel, and the impedance is mainly determined by the on-chip routings to pads. After the etching process is completed, the two electrodes are separated. Fig. 38(d) presents the optical microscopy (OM) and scanning electron microscopy (SEM) images of the via electrodes after the channel has been formed. To ensure the integrity of the electrodes, we have chosen an impedance threshold of 1MΩ in our experiments. The

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etching process is carried out in three phases due to the change in dominant impedance contribution, as depicted in Fig. 64(b).

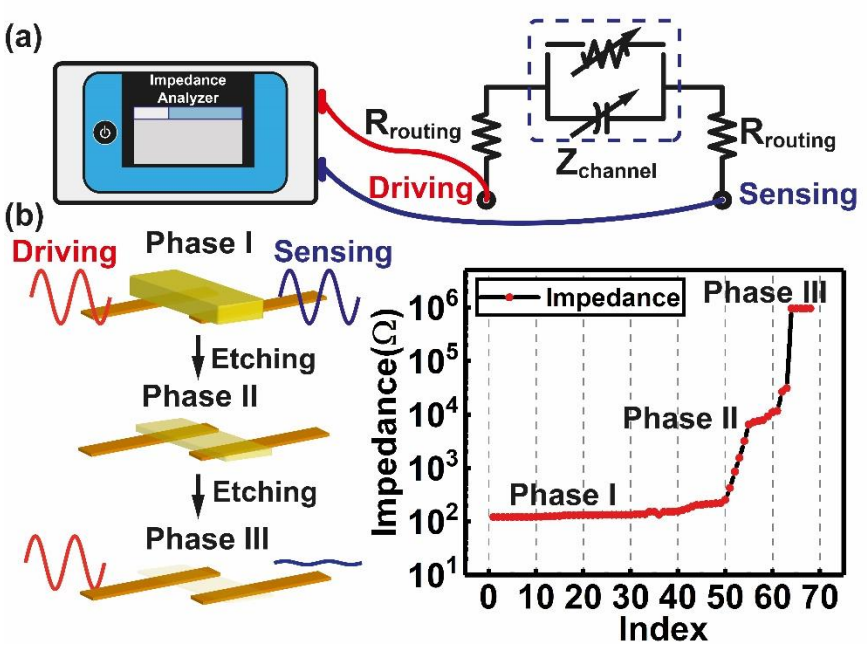

Fig. 64. (a) The equivalent circuit model measured by an impedance analyzer for real-time monitoring of the etching status. (b) The changing impedance at different etching phases.

2.8.4 Impedance sensing demonstration

To showcase our technology, we conducted an experiment where we measured the impedance of saline-sodium citrate (SSC) buffer solutions with different strengths using our on-chip via electrodes and a Palmsens 4 impedance analyzer. In Fig. 65(a), we present the measured impedances (|Z|) at 1 MHz for ionic strengths ranging from 1× to 20× (where 20× buffer includes 3.0 M of NaCl and 0.3 M of sodium citrate at pH = 7.0). The data obtained from our on-chip via electrodes correlates well with the results obtained from off-chip Ag/AgCl electrodes, and the data is reproducible.

We also investigated the durability of our via-electrodes during continuous measurement interrogations. Fig. 65(b) illustrates the impedance measured in 20× SSC

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buffer for a duration exceeding 12 hours. The results indicate a drift of 20 ohm/hr, which we consider negligible, especially when compared to our intended point-of-care applications, where the measurements will mostly be completed within 0.5 hours.

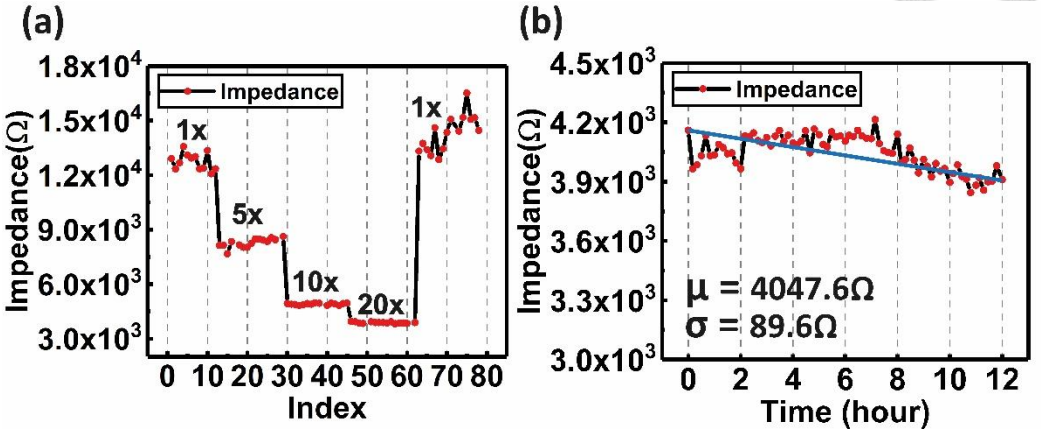

Fig. 65. (a) The measurement of SSC buffer at different ionic strengths. (b) A long-term study of electrodes reliability.

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Chapter 3 CMOS-integrated micro-electrode for aptamer sensing

3.1 Research background

3.1.1 Aptamer-based electrochemical biosensing

The aptamer-based electrochemical biosensor, which is an electrochemical biosensor that utilizes synthetic nucleic acid aptamers, is a useful tool for detecting the presence and concentration of target molecules in complex samples, such as whole blood. Aptamers can be engineered into molecular "switches" that undergo reversible structure-switching upon target binding, as illustrated in Fig. 66. Electrochemical detection is achieved by using conjugated redox reporters (such as methylene blue) that are tagged onto the aptamers. As the tagged aptamers undergo conformational changes upon target binding, the efficiency of electron transfer between the redox reporter and gold electrode surface also changes, leading to different current levels that are proportional to the target concentration. The electrode surface is further protected with 6-mercapto-1-hexanol to prevent non-specific binding. Aptamer-based biosensors offer real-time detection without requiring additional reagents, making them suitable for long-term in vivo therapeutic drug monitoring.

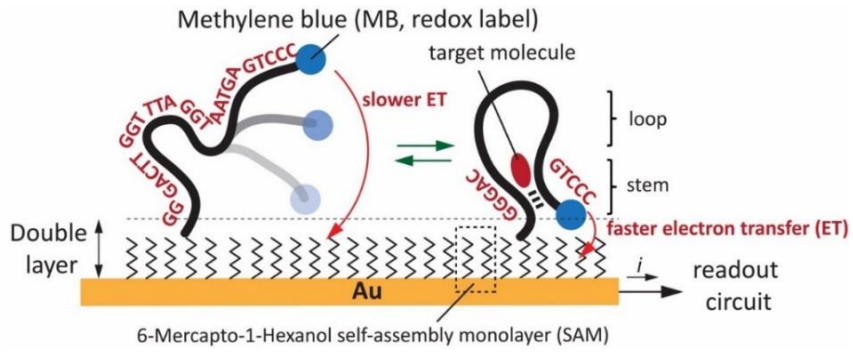

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Fig. 66. Operation of structure-switching aptamer with and without the presence of the target molecule [27].

To detect electrochemical signals, a three-electrode system is commonly used, which includes a working electrode (WE), a reference electrode (RE), and a counter electrode (CE). An aptamer-based biosensor typically uses this system, and Fig. 67 displays the standard current readout circuit. The WEs are immobilized with aptamers, whose potential is determined by VREF. A potentiostat composed of VDAC and A1 is used to control the solution's potential through the RE and carry out square-wave voltammetry (SWV), as shown in Fig. 67. SWV is preferred over cyclic voltammetry (CV) because it separates the non-Faradaic currents from the desirable Faradaic components, allowing for higher current resolution and improved sensitivity. Fig. 68 presents an example of an SWV voltammogram that demonstrates how the peak current is proportional to the target molecule's concentration.

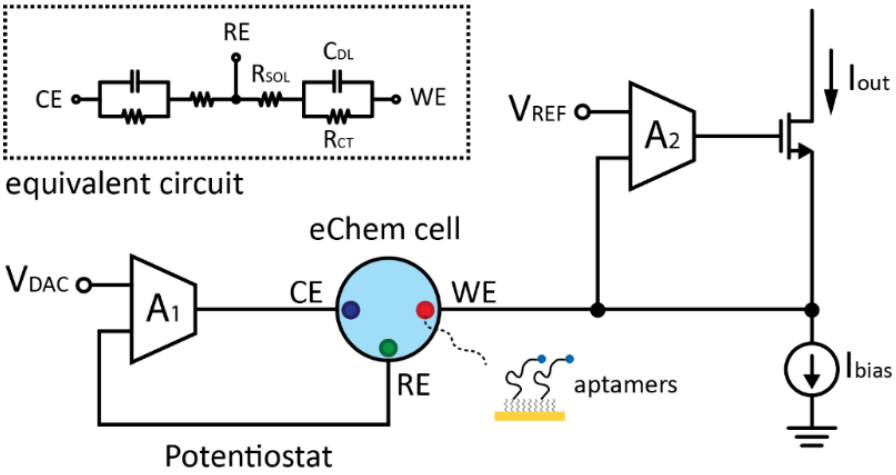

Fig. 67. Conventional control and readout circuits for aptamer biosensors [27].

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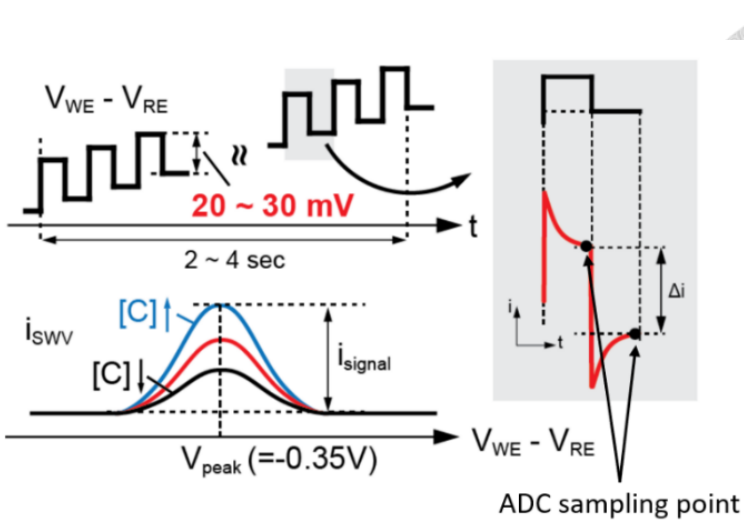

Fig. 68. Illustration of square-wave voltammetry operation [27].

3.1.2 CMOS-based microelectrode array

Currently, the most widely accepted method for investigating cell electrophysiology in preclinical drug discovery is the PATCH clamp. However, because this technique is time-consuming, researchers have developed passive and active multi-electrode arrays (MEAs) to increase the speed of extracellular in vitro measurements. CMOS-based microelectrode array has been developed in these decades. [2, 27-41] It can be used to conduct multisite extracellular recordings on electrogenic mediums, like neurons and muscle cells. Furthermore, they are employed in the areas of biosensing and neuroscience to investigate the basics of learning processes, mental illnesses, and aging, to evaluate the performance of electrogenic cells in vitro, and to screen for pharmaceutical agents. Fig. 69 and Fig. 70 show two examples of system-on-chip (SOC) with a microelectrode array for in vitro electrogenic cell screening.

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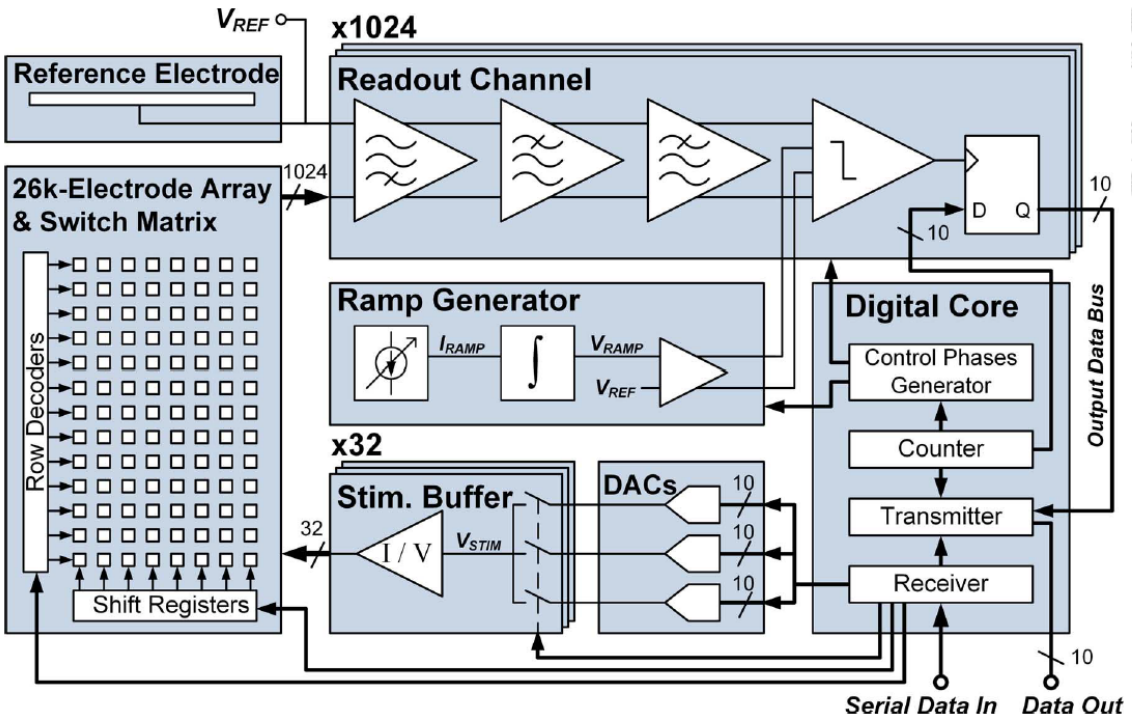

Fig. 69. Architecture of the CMOS microelectrode array chip. [28]

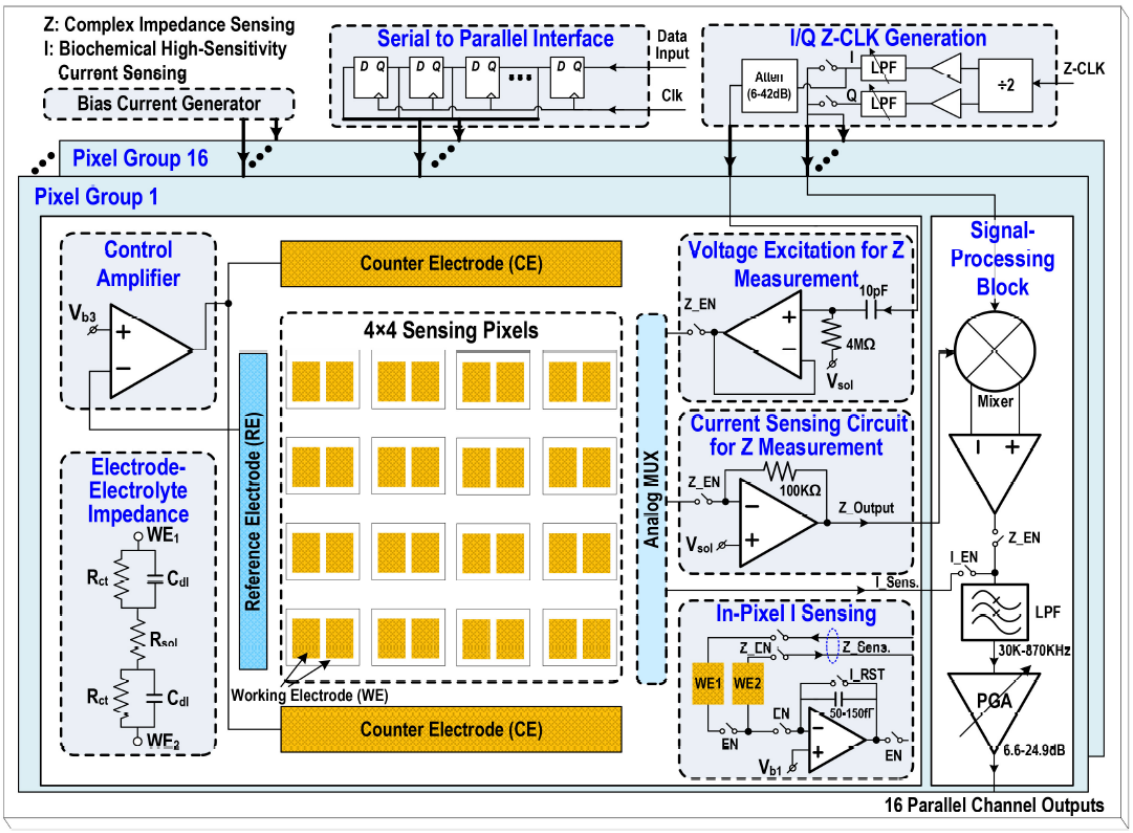

Fig. 70. Chip architecture of the joint electrochemical and impedance sensor array. [32]

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3.1.3 On-chip electrode fabrication methodology

To enhance their biocompatibility and ensure their durability over extended biological experiments, the on-chip electrodes present in CMOS ICs produced by foundries require surface modifications. This is particularly essential for contact-based sensing approaches, as the on-chip electrodes are typically composed of Aluminum (Al), which is the top metal layer in a standard CMOS chip. When exposed to regular cell culture media and buffer solutions, these electrodes may easily react and become damaged in a short amount of time, making them degraded or even unusable permanently. As a result, additional post-processing steps are required to make them suitable for long-term use.

Most electrochemical techniques utilize gold as the sensing electrodes because of its stability and compatibility with bio-measurement. There are two main methods to fabricate the on-chip electrode array: plating-based and deposition-based. The former has the advantages of a simpler process and lower cost because it doesn't require mask design and the expensive gold evaporation slug. Yet, the plating quality is hard to control, including uniformity and purity. Fig. 71 shows a comparison table from [35], which maintains that it's superior to use the electroless-plating technique to fabricate the electrodes. By contrast, though the latter requires a more complex process flow, it forms the gold layer of higher quality.

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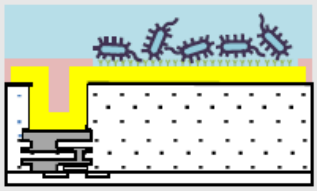
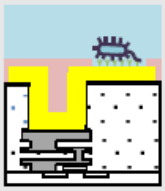
	Contact photolithography (Conventional)		Electron-beam lithography (Conventional)		Electroless plating (This work)	
Structure						
Production equipment	Big, Expensive	×	Big, Expensive	×	Tabletop size, Cheap	O
Mask	Mask needs to be aligned	×	Mask doesn't need to be aligned	△	Mask doesn't need to be aligned (self-alignment)	O
Miniaturization limit	Accuracy of mask production (about several μm)	×	Accuracy of electron-beam exposure	△	Standard CMOS process (about 0.02μm)	O
Trench structure (For high-sensitivity)	Additional process is required	×	Additional process is required	×	Additional process is not required	O

Fig. 71. Comparison of the fabrication methodologies for forming the gold electrode. [35]

Fig. 72 demonstrates the electrode degradation by the reaction of uncovered defects with the solution on a plated chip. As a result, it's worthwhile to use the deposited method despite the higher cost. Fig. 73 shows two works using deposition for the gold electrode. Both of them remove the aluminum layer first, then use the via, which is mainly made of tungsten. The other methodology is shown in Fig. 74. This method doesn't remove the aluminum layer. Instead, it uses zincation to modify the surface material to zinc, which acts as a protective layer for aluminum and removes the native oxide. (Fig. 72)

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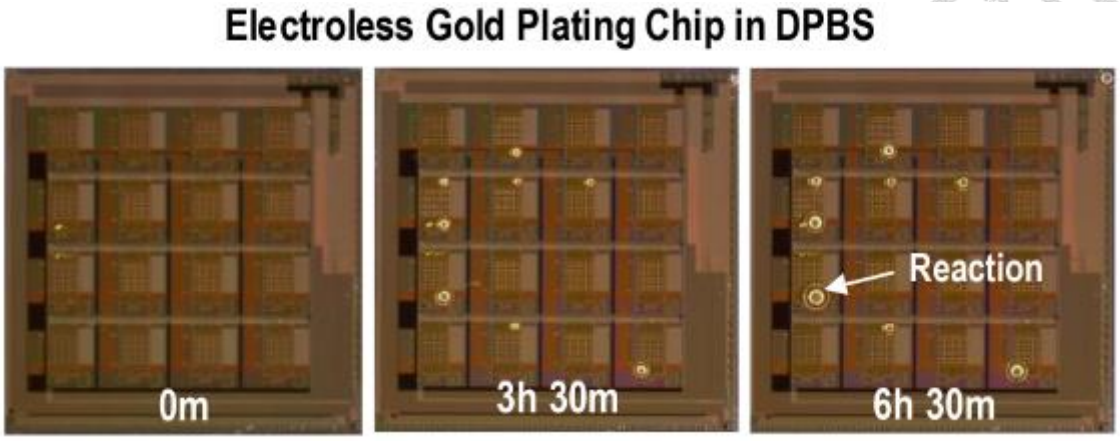

Fig. 72. The image of electrode degradation due to the non-uniformity of the electroless-plating method. [32]

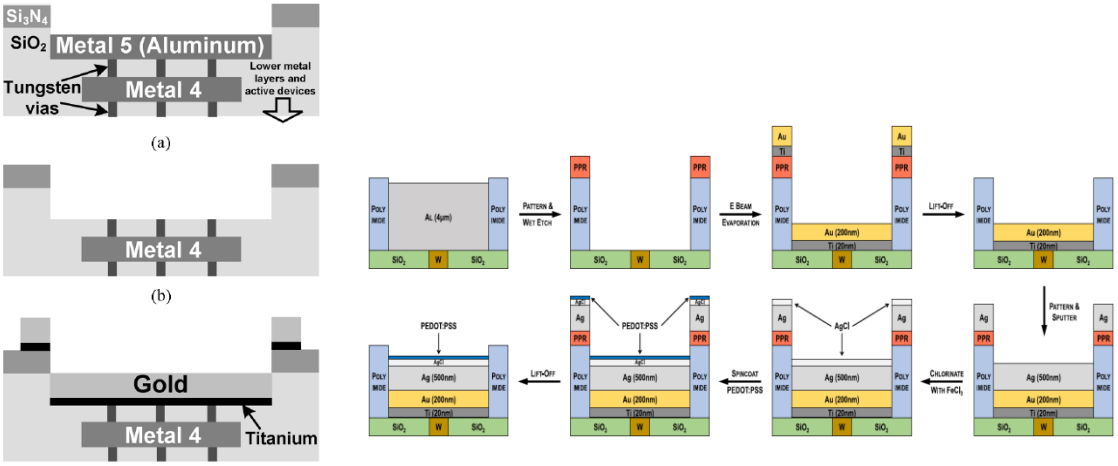

Fig. 73. Process illustration of aluminum removal followed by gold deposition. [32, 42]

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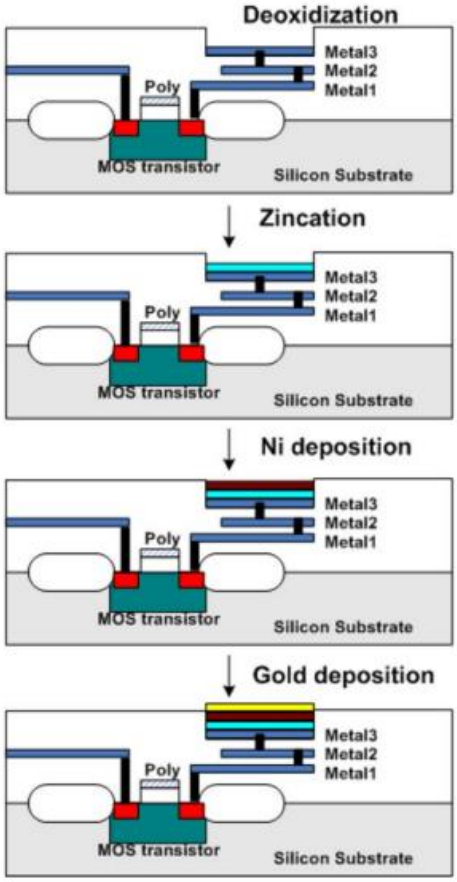

Fig. 74. Process illustration of electroless-plating followed by gold deposition. [43]

3.2 Sensing verification by off-chip electrodes

Prior to the CMOS on-chip electrodes development, we used two kinds of devices for preliminary testing. The first one is commercial electrodes from Vida BioTechnology. We drew the electrode's layout of various sizes, to test the signal change due to electrode size scaling. Then, we made a device that is fabricated by an E-gun evaporator for depositing gold in the cleanroom. With this prototype, we validated that the fabricated gold sensing film from our process is compatible with aptamer-based electrochemical sensing purposes.

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3.2.1 Commercial electrodes

To begin with, we use commercial plating electrodes to investigate the functionality of our aptamer-based electrochemical sensing setup. Fig. 75 is the setup photo, which shows the three-electrode electrochemical sensing technique including WE/RE/CE. The testing result is shown in Fig. 76. A detailed description of square-wave voltammetry can be referred to [27].

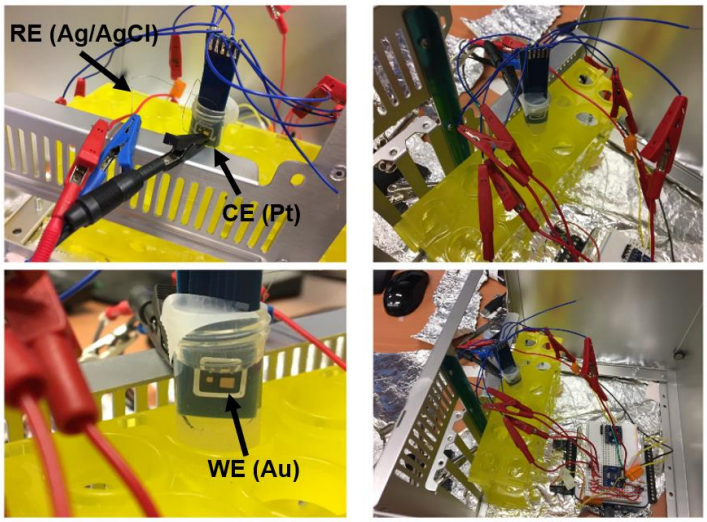

Fig. 75. The measurement setup using commercial electrodes.

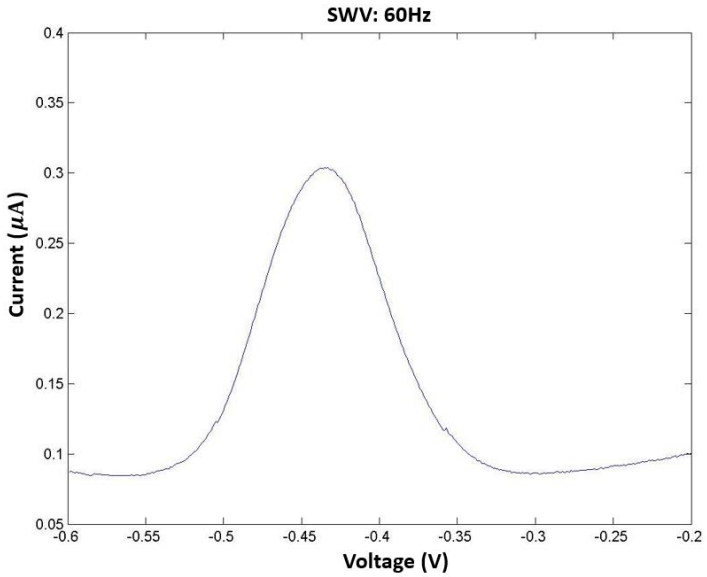

Fig. 76. Measurement results of SWV 60Hz for kanamycin aptamer.

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3.2.2 Deposited electrode by E-gun evaporator

With the validation of our aptamer functionality and workable setup, we investigate the electrode property using the evaporator-deposited gold in the cleanroom. The device fabrication is based on lift-off for the Ti/Au(15nm/200nm) layers. The measurement setup and the measured curve are both consistent with the result using commercial electrodes. We also performed SWV 60Hz to kanamycin aptamer by injecting 0.036V amplitude stimulation and sweeping from -0.7V to 0.1V. The only difference is the electrode size. (Fig. 77)

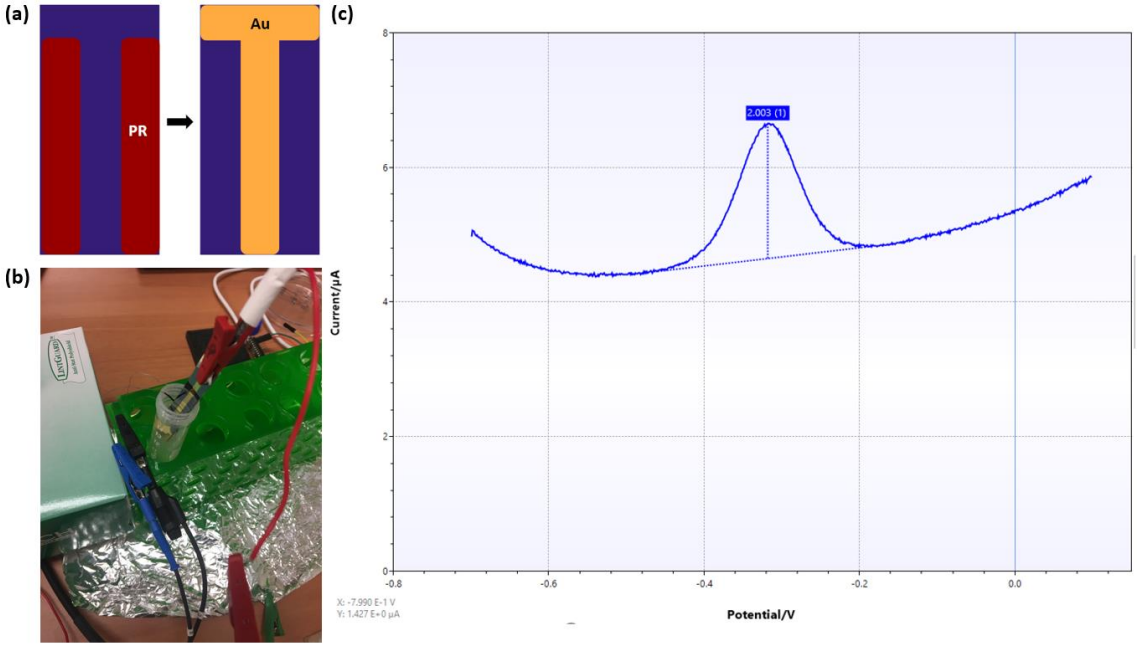

Fig. 77. (a) The illustration of our preliminary testing device. (b) The measurement setup. (c) The measurement result of SWV60Hz using kanamycin aptamer.

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3.3 CMOS on-chip microelectrodes

Fig. 78 shows the die photo of our proposed architecture. It contains the CMOS-integrated microelectrode array blocks and the CMOS-embedded microfluidics block. The fabrication of will be introduced below and the CMOS-embedded microfluidics are discussed in Chapter 2.

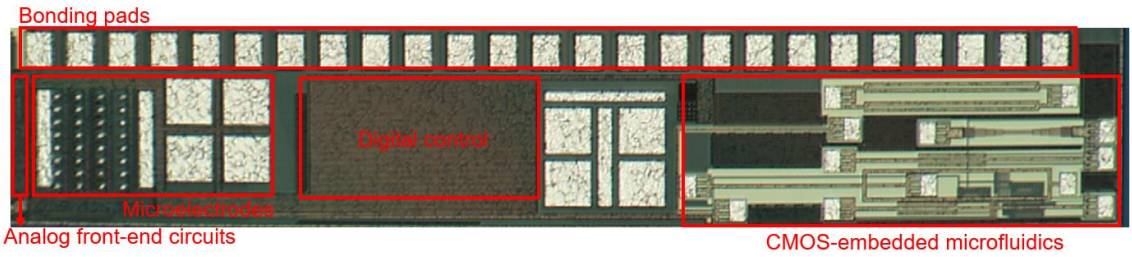

Fig. 78. The die photo of our proposed architecture.

3.3.1 Fabrication flow

We develop the CMOS on-chip electrodes based on the methodology mentioned in Fig. 74 because we found that the via can be damaged by aluminum etchant indeed after our experiments. The developed process flow is shown in Fig. 79. Note that we followed the zincation process published in [35]. Fig. 80 shows the optical microscopic image of our on-chip electrodes including 10μm and 100μm widths.

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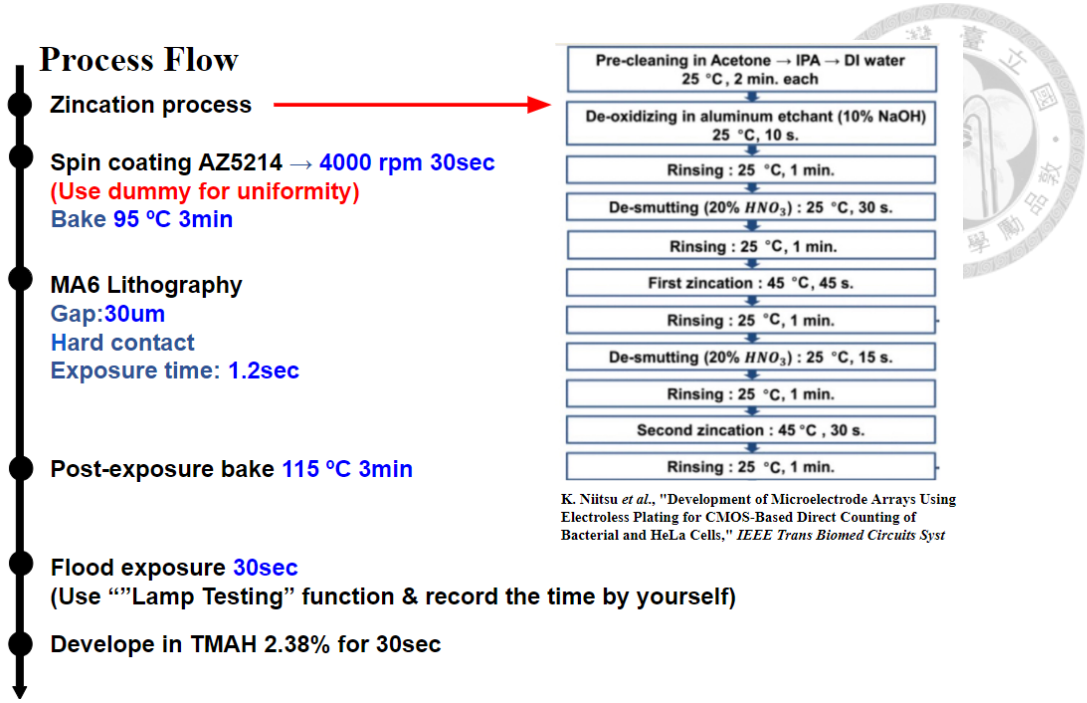

Fig. 79. The process flow for CMOS on-chip electrode.

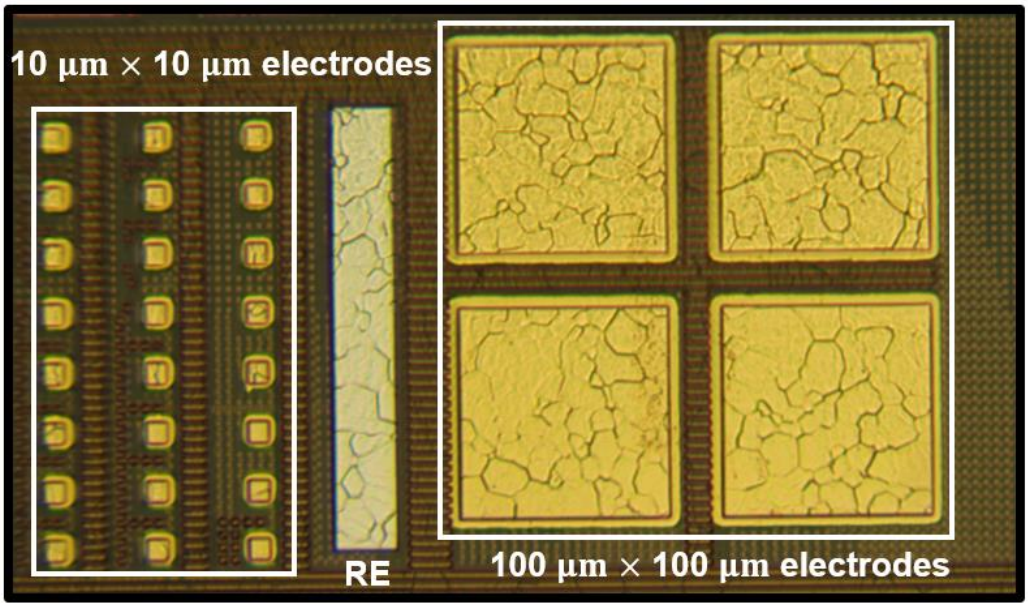

Fig. 80. The OM image of fabricated on-chip electrodes.

3.3.2 Measurement results

We used the 100µm-width electrode for verification. The measured device and the curves are shown in Fig. 81. We also performed SWV 60Hz to kanamycin aptamer by

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injecting 0.036V amplitude stimulation and sweeping from -0.7V to -0.2V. From the results, we got the peak signal 3nA and confirmed the functionality of our fabricated on-chip electrodes even though there was one failed electrode shown in the result, which is a yield rate issue caused by post-processing failure or sample contamination. The peak signal 3nA is much lower than all the above-reported values, like 2μA from our "bulk electrode" using a silicon wafer as a substrate. This huge difference comes from the area scaling. To be more exact, the aptamer density of our electrodes was decided by the bio-sample concentration, which was all the same. Yet, the signal amplitude is proportional to the electrode size, which contributes to different surface double-layer capacitance, aptamer amount, and the target sensing area. Thus, the value we measured was much lower.

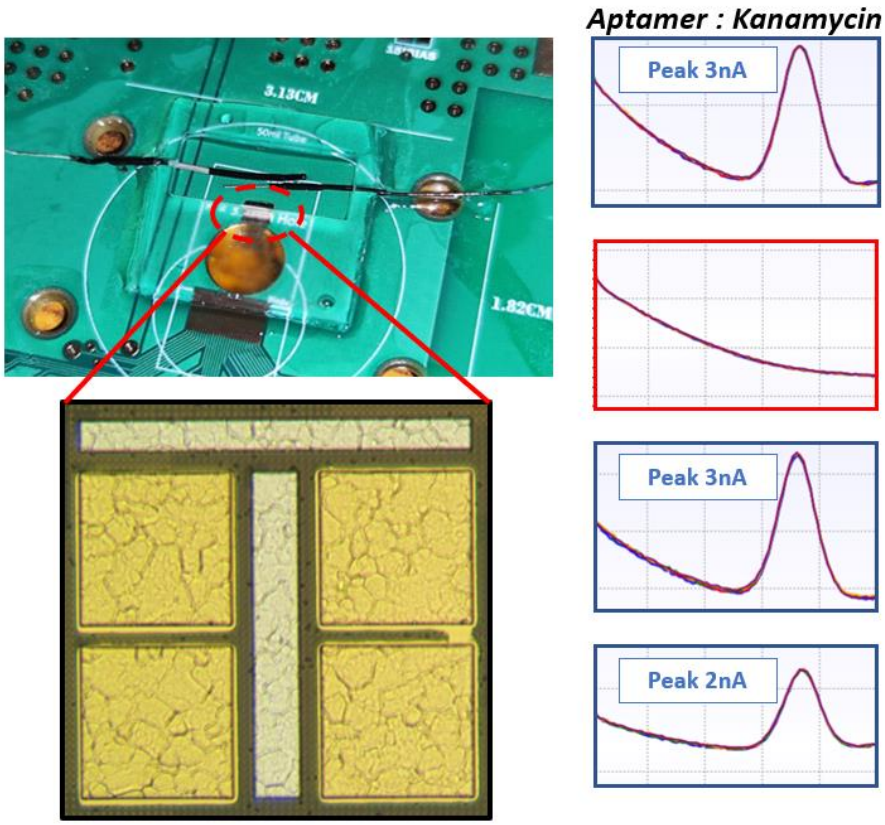

Fig. 81. Measurement results for on-chip electrode verification.

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Chapter 4 3D-stacked Electronics Device Fabrication

4.1 Research background

4.1.1 3D electronics

To continue the More-Moore progress year by year, there is a promising candidate to realize further technology node development —3D electronics. We can divide the domain of 3D electronics into three areas: transistor level, standard-cell level, and the packaging level. (Fig. 82) Firstly, the transistor level refers to those novel devices like stacked nanosheet gate-all-around (GAA) devices. We make the transistor itself into 3-dimension, which means the z-axis, by stacking the channel. Secondly, the standard-cell-level 3D integration is to re-design the traditional standard cell, like inverter, NAND, and NOR, to stack on the z-axis. Different from the transistor-level, which is a single transistor, 3D stacking on a standard cell requires to concern much more aspects including the place and route. Lastly, the packaging-level 3D electronics tend to realize the system-on-chip (SOC). There will be a variety of blocks integrated by TSVs or interposers. (It's generally called 2.5D within this regime. The full 3D integration should rely only on a package substrate.)

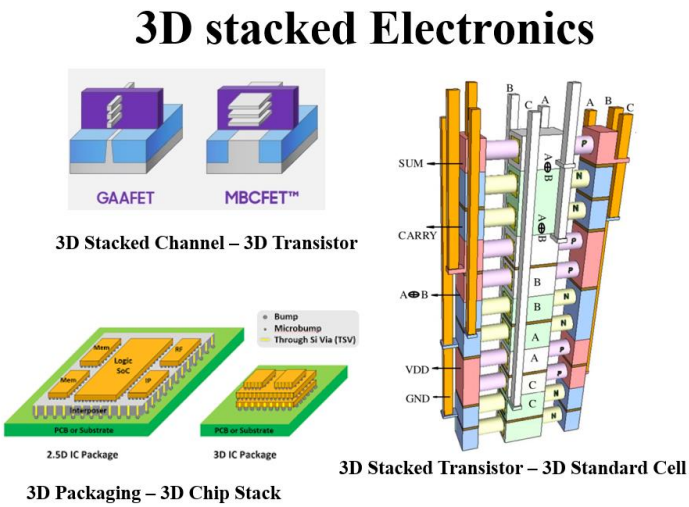

Fig. 82. 3D stacked electronics in three regimes.

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4.1.2 Complementary field-effect transistor (CFET)

The fundamental concept of Complementary FET (CFET) is to stack nFET and pFET on each other (Fig. 83), which enables the area scaling. Using the complementary nature of CMOS logic, which means the input signal for both n and p-type are the same, we can make their gates "common" to get a new routing thinking. This 'folding' of the nFET and pFET eliminates the n-to-p separation bottleneck, reducing the cell area footprint. The concepts mentioned above are in the framework of design technology co-optimization (DTCO) (Fig. 84). In the DTCO framework, we need to co-optimize the fabrication techniques with the design requirement. Therefore, with the CFET concept, we need not only the advanced process, but the new floorplan of layout, routing, and even the EDA tools that are required to progress together.

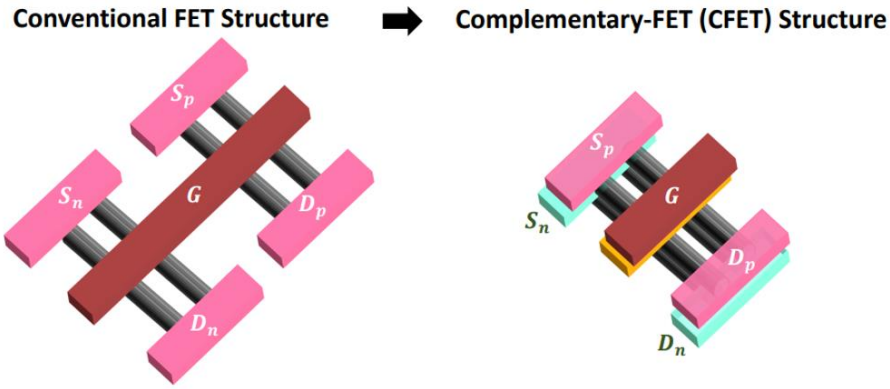

Fig. 83. The concept of CFET. NFET and PFET are stacked on each other [44].

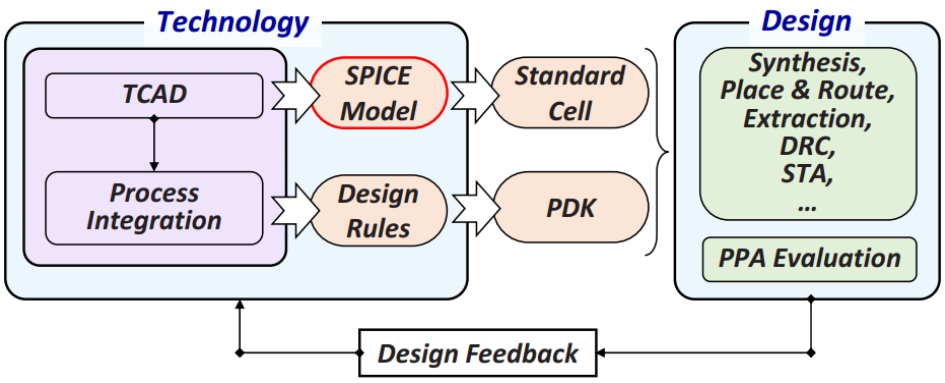

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Fig. 84. DTCO flow for new devices.

4.1.3 CFET fabrication methodology

In this paragraph, we will review some papers from Taiwan Semiconductor Research Institute (TSRI), Imec, and Intel. Based on the work of these well-known research teams, we will know the process flow and challenges of CFET fabrication.

In TSRI's works, they adopted two different fabrication methodologies. [45, 46] Firstly, they demonstrated a CFET inverter on a stacked poly-Si nanosheet structure. Fig. 85(a) shows the process flow of their work and the architecture of the CFET. Combining alpha-Si deposition and thin-down with dry etch, they used poly-Si as channel material and take the sequential method, which means they finished the first NMOS layer and then do the PMOS part on it, with PECVD oxide as the spacer. Fig. 85(b) shows the SEM images of the devices. We can see the area reduction compared to conventional CMOS. From the cross-section TEM and EDS image (Fig. 85(c)), we can see the conformal distribution of Al_2O_3 (high-k) and Ti (using TiN as a metal gate).

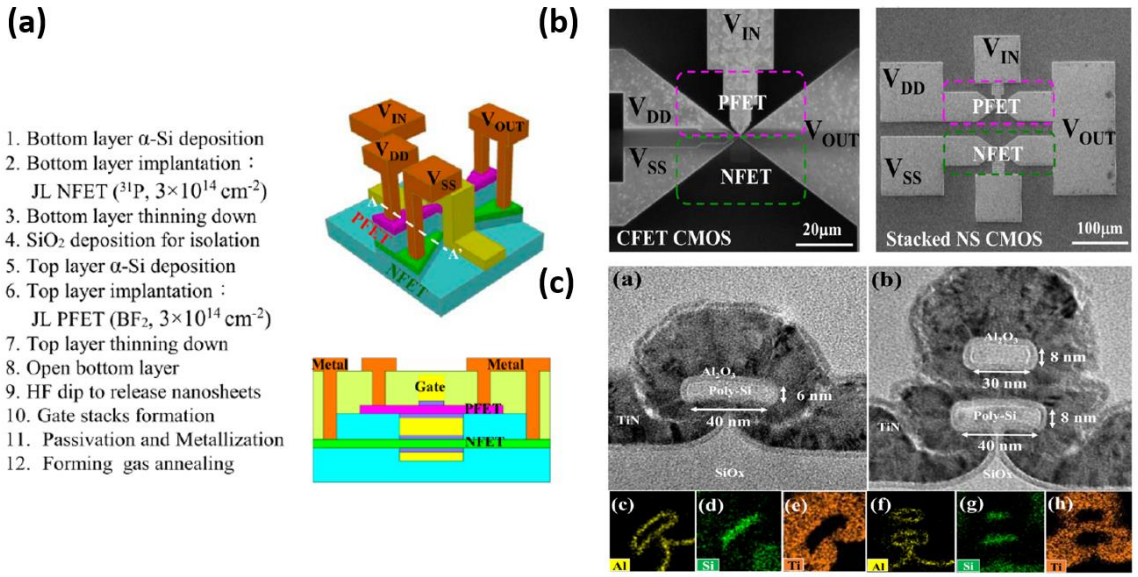

Fig. 85. (a) The process flow and the structure of CFET. (b) The SEM top-view image of CFET and conventional device. (c) The TEM and EDS image of CFET of single nanosheet and stacked [46].

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Different from the process above, TSRI also used another method to realize the CFET structure. Compared to the sequential processes mentioned above, they took the wafer bonding technique, which enhanced the device performance but at a higher cost. They proposed a low-temperature hetero-layers bonding technique to enable the Ge channel to bond onto single crystal Si wafers. Fig. 86(a) shows the process flow of LT-HBT. With ALD oxide, PECVD oxide, Ge epitaxy, and the help of deep RIE and annealing, they get the wafer of heterogeneous structure for the following process (Fig. 86(b)). Then, after the wafer preparation, it's followed by the fabrication steps similar to those mentioned in the previous paper. [46]

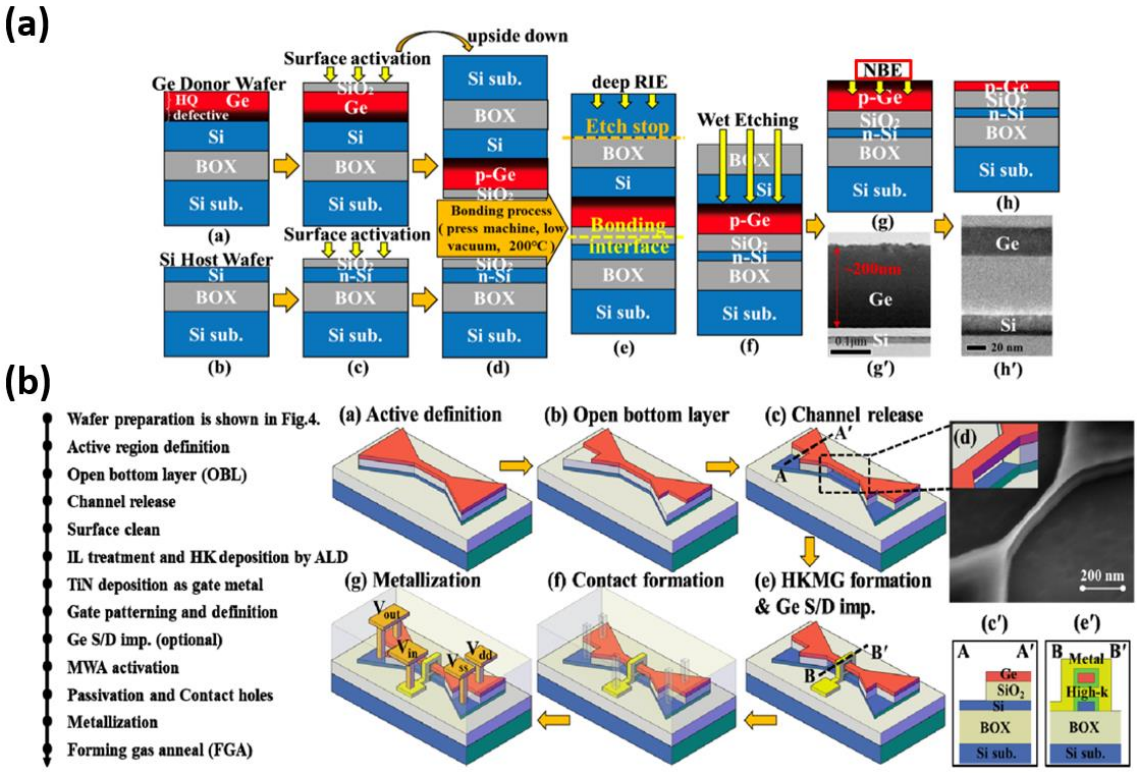

Fig. 86. (a) Low-temperature hetero-layers bonding (LT-HBT) process flow. (b) Schematics and process flow of CFET device. [47]

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In Imec's work, they used a monolithic CFET process, which is more cost-effective. With such a method, the separation between NMOS and PMOS can be smaller so that it can reduce the parasitics and provide higher performance gains. There are six critical modules for the whole fabrication: fin/dummy gate, gate spacer, inner spacer, bottom epi, bottom contact/NP isolation, and top epi/contact. (Fig. 87) In this work, they successfully demonstrate a 3D monolithic integration of CFET architecture, which contains a bottom PMOS finFET and a top NMOS nanosheet FET.

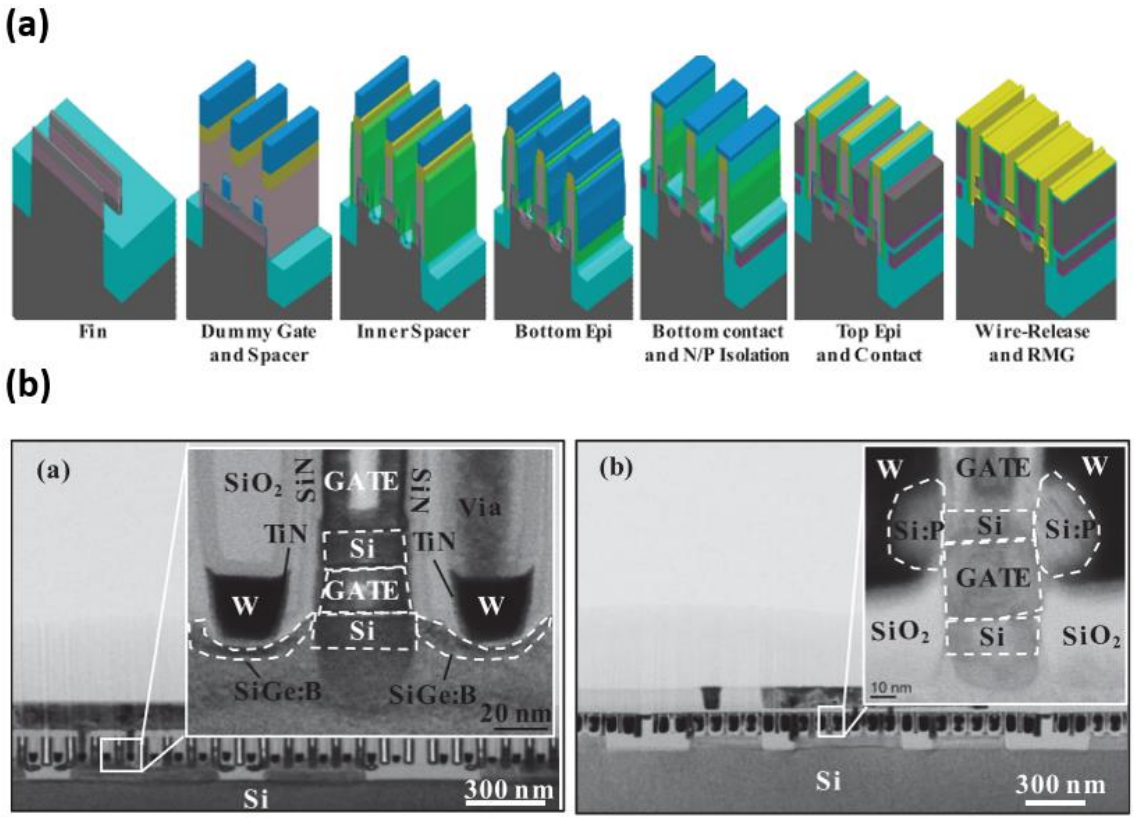

Fig. 87. (a) Schematic of the critical steps in CFET fabrication. (b) TEM cross-section view of bottom PMOS finFET (left) and top NMOS nanosheet FET (right).

In Intel's work, they proposed a self-aligned structure (which is similar to the concept of CFET) integrating the vertically stacked dual source/drain EPI process and dual metal gate process. Fig. 88 shows the whole process flow and architecture of the device. First, they grow epitaxial Si/SiGe superlattice deposition on a 6nm ultra-thin body SOI wafer.

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Then selective growth of phosphorous-doped Si and boron-doped SiGe (Fig. 89(a)) was done to build up the CFET structure. In addition, to adjust the V_T for NFET and PFET, they did a dual metal gate process, using different work function metals (Fig. 89(b)).

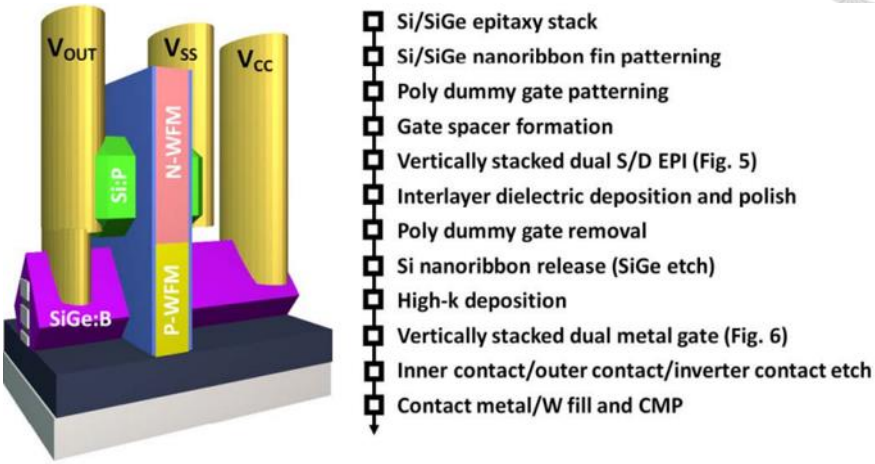

Fig. 88. 3D schematic diagram of the stacked structure and the whole process flow. [48]

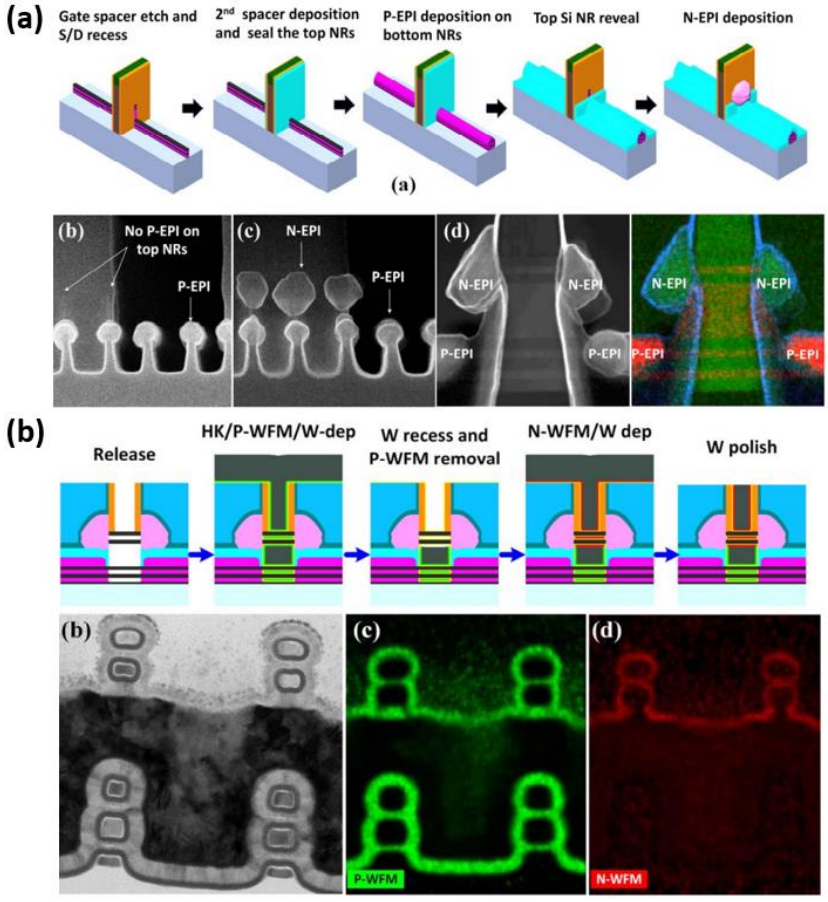

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Fig. 89. (a) Detailed process flow of dual S/D EPI process. (b) Detailed process flow of stacked dual metal gate process. [48]

4.2 Proposed novel CFET process flow

In our work, we aim to develop a lower-cost fabrication suitable for academic research, instead of using complex epitaxial growth or wafer bonding techniques. For these purposes, we utilize the membrane transfer technique for the fabrication of CFET architecture. Membrane transfer has the merits of we can easily get single crystalline silicon for our device; in addition, the less complicated process makes it more cost-efficient. The process flow and schematics are shown in Fig. 90. Starting from a silicon-on-insulator (SOI) wafer, we pattern it with undercut holes for the etchant to flow through and undercut the buried-oxide layer. After the undercut process, we pick up the suspended membrane by a PDMS stamp, then we can transfer the single-crystal silicon membrane to another substrate. By doing so, the stacked structure of Si/SiO2/Si can be formed.

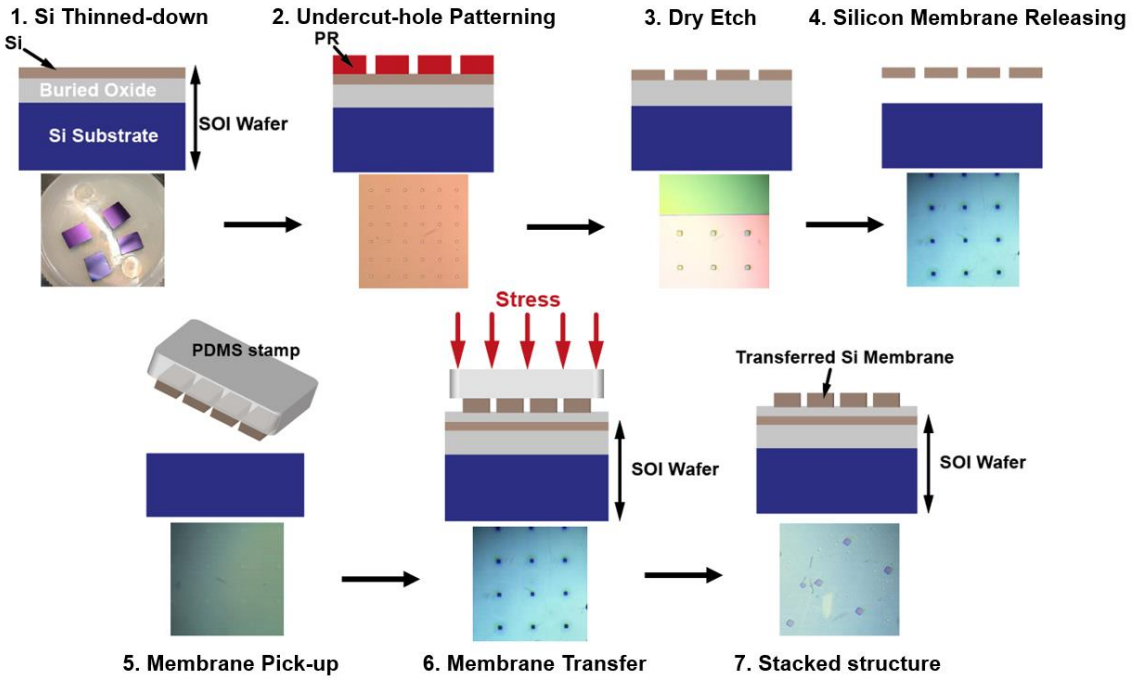

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Fig. 90. The process flow and schematic with corresponding OM images for the membrane transfer process (modified from [49]).

With such a stacked structure, the next step is to do lithography for device pattern definition. In this work, we use helium ion beam lithography for several critical steps due to its smaller critical dimension, higher resolution, and capability for higher device density. During the whole process of the CFET device using our proposed process flow, we need to use HIB lithography to cover six steps: alignment marker formation, blocking layer for ion implantation, active channel region definition, common-gate definition, and via opening and M0 interconnection. The key process steps are presented in Fig. 91.

To form the stacked structure with both p and n-type doped silicon, we use chromium as a hard mask to block the undoped channel region. We use phosphorous (P) and difluoro boron (BF_2) as n-type and p-type implantation sources respectively. The implantation parameters and expected profile are simulated by Sentaurus TCAD.

After the formation of such a stacked structure, we use chromium as a hard mask again to define the active region and perform CF_4-based dry-etch to create the device unit. Then open the bottom silicon layer for separating the Vss and Vdd connection. Channel suspension is done by diluted HF (DHF) wet etch, followed by the high-k metal gate (HKMG) using atomic layer deposition (ALD) and gate definition using HIB. After the above process flow, the gate-all-around architecture can be formed. (Fig. 92)

Common-drain formation is realized by a high aspect ratio common via dry etching and deposition of Ti as n-type work function metal and Ni as p-type work function metal. (Fig. 93) Lastly, do another HIB lithography to create the device interconnection and the probing pad. Going through all the above process steps, we can have a CFET prototype based on the membrane transfer technique.

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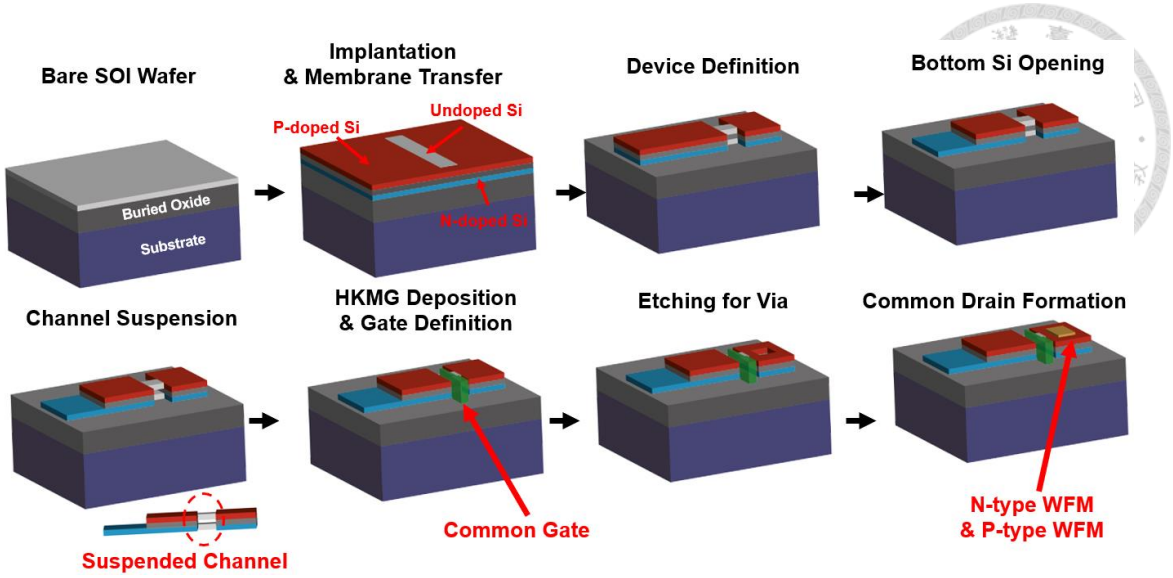

Fig. 91. Key process flow of our proposed CFET device (modified from [49]).

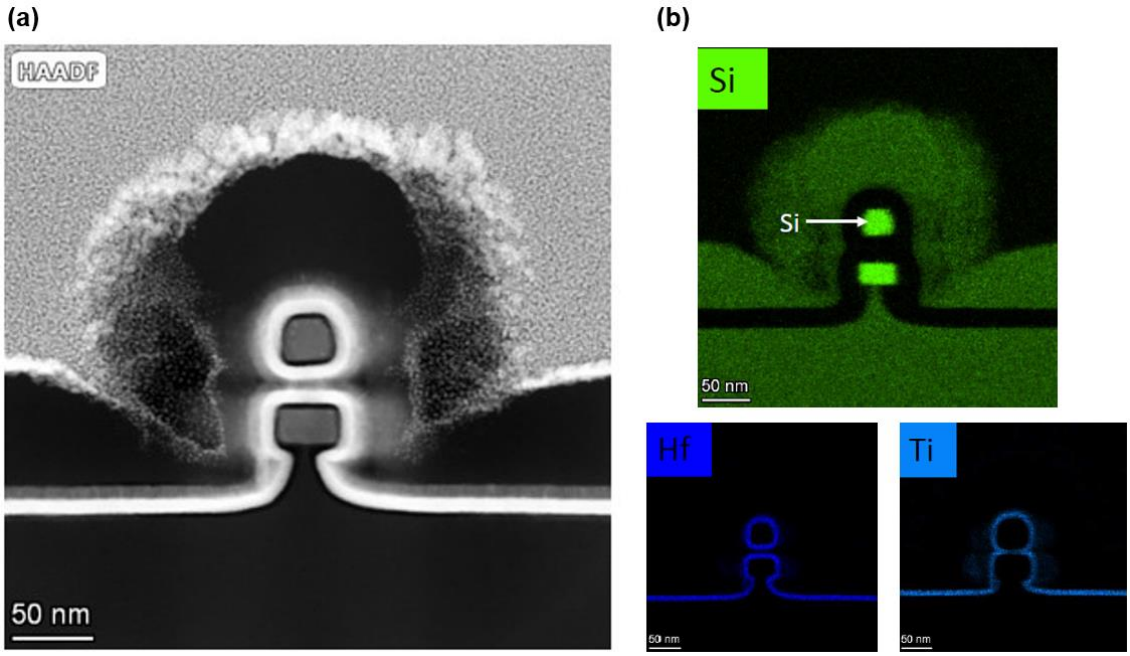

Fig. 92. TEM results after HKMG formation. It shows a typical GAA structure realized by the membrane transfer technique.

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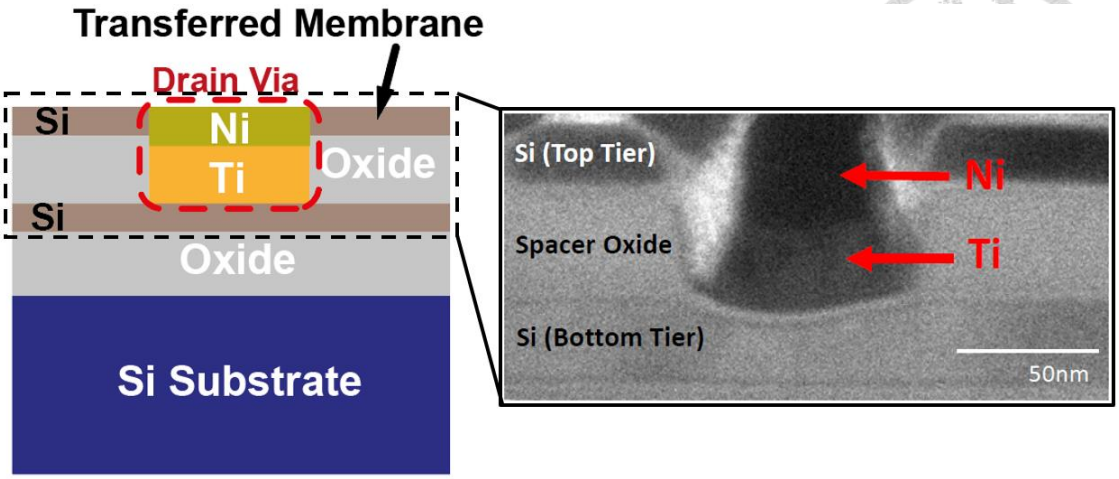

Fig. 93. Common-drain formation with different types of metal work function (modified from [49]).

4.3 Declaration

All the experimental results presented here are just for thesis completeness purposes. The publication right totally belongs to Prof. Tzu Hsuan Chang's lab. We won't publish these results or use them for other cooperative/commercial purposes.

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Chapter 5 Conclusion

We develop the CMOS-integrated system and device; in addition, we also introduce a feasible technique to realize the CFET structure. In the first part, the research showcases a micro/nanofluidics platform that is embedded in CMOS chips and suitable for next-generation lab-on-a-chip devices. The fabrication of sub-10-μm fluidic channels using a single-step wet-etching technique was achieved by sacrificing the BEOL metallization, resulting in a low-cost and scalable process. This work involves the optimization of creating microfluidics from CMOS BEOL. A process was developed that involves replacing aluminum etchants with phosphoric acids and introducing hydraulic pressure to enhance etchant replenishing rates. Various fluidic structures were demonstrated including straight-line, multi-channel splitter, 3D fluidics channel, resistive pulse sensing channel, sheath flow, and serpentine micromixer. The impact of etchants on transistors and circuits was studied, which proves the feasibility of this wet-etching process. To build up the whole integrated system, this work also establishes the process flow for SU-8 microfluidics fabrication in the clean room. Furthermore, resistive pulsing sensing was successfully used to detect a single E. Coli cell. Additionally, on-chip contacting “via” electrodes were proposed for impedance-sensing purposes, utilizing the observed anisotropic etching phenomenon. The sensing functionality and reliability of the on-chip electrodes were verified by measuring saline solutions.

In the second part, we demonstrate the on-chip electrodes for aptamer-based electrochemical sensing. By using ENIG and E-gun evaporator deposition process, we successfully perform the sensing functionality of CMOS on-chip electrodes.

Lastly, we introduce a process to fabricate vertically stacked gate-all-around

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complementary FET (CFET) with membrane printing techniques. In the experiment, we successfully realize GAA channels wrapped by conformal HfO_2/TiN, and we also fabricate the common-via for the drain with different work function metals.

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Chapter 6 Future work

For the CMOS-embedded microfluidics part, we plan to integrate "active" sensor front-end circuits for a complete system demonstration in the future. The goal is to develop a fully-integrated system incorporating fluidics and electronics on the same CMOS chip. In addition to the integration of active circuits, we also aim to address those issues mentioned in Chapter 2 for those passive structures, so that we can realize a multi-functional microfluidics design on our CMOS chip. Overall, this work showcases a promising technology with potential for various applications in the field of lab-on-a-chip devices.

For the CMOS-integrated electrochemical sensing electrode part, we need to further increase the yield rate. Also, we aim to integrate not only the gold electrode as WE, but the platinum and Ag/AgCl for CE and RE respectively. Once the on-chip electrode fabrication is mature, the next step is to make the microelectrode array more compact and high-density and add more analog-front-end circuit parts for SoC realization. Moreover, we also aim to combine CMOS-embedded microfluidics with aptamer applications, such as flowing the bio-samples with multiple on-chip channels in parallel to realize a multiplex immobilization.

For CFET fabrication, we need to continue the development of a full CFET device for the following electrical characteristic verification. For now, we just realize the GAA structure and other individual testing, like common-via structure, contact resistance, and the interconnect. Therefore, the result is to combine these processes and successfully make a CFET device for beyond the 3nm technology node.

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