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Master Thesis

主動箝位電流饋入型雙主動橋式轉換器之雙向控制策略

Bidirectional Control Strategy for Active-clamp Current-fed Dual Active Bridge Converters

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國立臺灣大學碩士學位論文
口試委員會審定書

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本論文係 葉昶均 君（學號 R09921034）在國立臺灣大學電機工程學系完成之碩士學位論文，於民國 111 年 6 月 29 日承下列考試委員審查通過及口試及格，特此證明。

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摘要

本論文提出一個適用於主動箝位電流饋入型雙主動橋式轉換器(Active-clamped current-fed dual active bridge, AC-CFDAB)的雙向控制策略，透過雙重相位移的控制實現雙向能量傳輸，並擁有比現行調變方式更好的換向暫態，同時也可以讓電路操作在當前輸出功率下的最大效率點。

AC-CFDAB 的低壓側漣波小且可以達到雙向能量傳輸，非常適合用於電池儲能應用於低壓側電源的場合。然而，現階段對於實現軟切換的開關調變方法研究多只適用於單向的能量傳輸，雙向操作需要涉及兩個不同控制方法的轉換，若是兩個控制方式差異過大，換向瞬間的暫態突波會十分明顯，嚴重時會損壞整體電路。

本文首先提出一個可以實現雙向能量傳輸的修改型雙重相位移的開關調變方式，由於在雙向操作時並不需要變換調變方式，可以大幅降低改變功率流向操作時的暫態突波。同時只要設定足夠的停滯時間，全部的開關都可以實現零電壓切換。此外，雙重相位移也提供更高的控制自由度，除了傳輸能量之外，轉換效率也有機會被提升。本論文透過對雙重相位移的解耦合與相關分析，提出可以達到最大效率操作點的雙向控制策略。

為了驗證所提控制策略的正確性，本論文實作一組 48V/400V, 720W 的原型電路。電腦模擬與實驗結果皆符合驗證所提控制策略的正確性。

關鍵字: 主動箝位電流饋入型雙主動橋式轉換器，雙重相位移控制，零電壓切換，最大效率追蹤

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ABSTRACT

This thesis proposes a bidirectional control strategy for the active-clamped current-fed dual active bridge(AC-CFDAB) converter. By controlling the dual phase-shifts, the bidirectional power transmission can be achieved, the bidirectional transient is better than conventional modulation methods, and the maximum efficiency point can be tracked.

The AC-CFDAB converter has the small low-voltage-side current ripple and the ability of bidirectional power transmission, which is very suitable for energy storage applications. However, research of soft switching modulation method listed in literature only focus on the unidirectional power transmission. Two different modulation methods are required to achieve the bidirectional power transmission. Usually, an obvious current spike will be generated during the transition of the two modulation mothods. In the worst case, the converter may be damaged.

This thesis first proposes a modified dual-phase-shift modulation(MDPSM) method for the bidirectional operation of the AC-CFDAB. Since there is no change of the modulation method for MDPSM, the current spike of the bidirectional operation transient can be mitigated dramatically. Also, the zero-voltage-switching feature for all the switches can be achieved by adding the proper deadtime. Additionally, the control of dual-phase-shift provides an additional degree of freedom to control, so that improve the efficiency of the converter. In this thesis, the proposed MDPSM is used to realize the maximum efficiency tracking of the converter.

To validated the performance of the proposed MSPSM modhod, a 48V/400V, 720W AC-CFDAB prototype is built and tested. Computer simulations and experiment results are provided to the performance of the AC-CFDAB with the proposed MDPSM method.

Keywords: dual active bridge converter, daul-phase-shift control, zero voltage switching, maximum efficiency point tracking

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Chapter 1 Introduction

1.1 Background

Nowadays, the necessity for renewable energy is gradually increasing. Due to the instability of renewable energy, battery energy storage systems(BESSs) are developed to increase the stability of the systems [1] - [5]. To transfer the energy between BESS and the DC bus, bidirectional dc-dc converters(BDCs) are brought into focus in recent years [6] - [10].

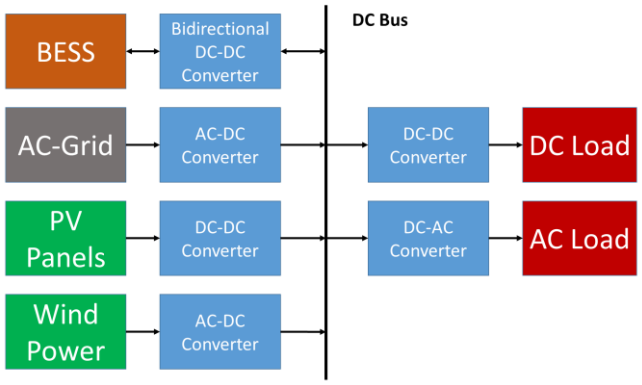

Fig. 1.1 DC microgrid system.

There are many topologies of BDCs, such as bidirectional buck converter [11], bidirectional buck-boost converter [12], bidirectional Ćuk converter [13], and so on. To assure more safety and the higher voltage gain ratio, isolated bidirectional dc-dc converters(IBDCs) are also considered. The conventional topologies of IBDCs include bidirectional push-pull converter [14], bidirectional flyback converter [15], dual half bridge converter [16], and dual active bridge(DAB) converter [17]. Among all topologies above, DAB converter is a popular choice with many advantages. For instance, the isolated topology of DAB provides higher safety than non-isolated BDCs, and DAB has

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the wider voltage gain ratio compared to the dual half bridge converter. The transformer in DAB can be regarded as a resonant tank, which can achieve soft switching in some cases and increase efficiency [18]. With these features above, DAB converters have attracted a lot of attention in BESS [19].

DAB has two types by its sources. One is the voltage-fed (VF) DAB with two voltage sources. There is a lot of research about VFDAB. In [20] – [23] propose several modulation methods, namely single–phase-shift(SPS) control, extended-phase-shift(EPS) control, dual-phase-shift(DPS) control, and triple-phase-shift(TPS) control. To enhance the ability of soft switching, modified topologies are considered in [24] – [26]. However, VFDAB generates the huge input current ripple, which is harmful to batteries. In BESS, another type of DAB, named current-fed (CF) DAB, is always applied [27].

The topology of CFDAB includes one current source and one voltage source. With this topology, the current ripple can be smaller than VFDAB, which is more suitable in BESS. However, a new challenge caused by the imbalance current is a crucial issue for CFDAB. In [28], several modified topologies, such as L-L type CFDAB and active-clamped(AC) CFDAB, are studied. Also, a naturally-clamped method is introduced in [29]. Compare to all the solutions above, AC-CFDAB is a popular choice with the benefit of the simple and easy-controlled topology.

1.2 Paper Review and Motive

Most of the research about AC-CFDAB focuses on the soft switching modulation method. In [30], a primary-side modulation method is provided to achieve zero-voltage switching(ZVS) for all primary-side switches in buck operation. Regarding the use of IGBTs, a ZVZCS primary-side modulation method for buck operation is given in [31]. And [32] and [33] propose a synchronous rectified ZVZCS modulation method for buck

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operation and a ZVS modulation method for boost operation. New ZVS modulation methods for buck and boost operation respectively are proposed in [34].

However, soft switching modulation methods proposed in [30] – [34] are just suitable for only buck or boost mode. For the bidirectional operation which involving in switching between buck and boost modes, two different modulation modes should be used. Bad switching transient, named the bidirectional transient, would be generated if the difference between buck and boost modulation methods is huge, which would be harmful to the circuit [34].

In this thesis, the bidirectional transient is improved by proposing a new bidirectional modulation method, named modified dual-phase-shift modulation(MDPSM). ZVS for all switches can also be achieved with proper setting. To regard more the efficiency, a maximum efficiency point tracking strategy(MEPT) is proposed based on MDPSM. With this strategy, a high-efficiency bidirectional power flow can be realized.

1.3 Outline

This thesis is organized into six chapters. Each chapter is introduced in the following.

In Chapter 2, AC-CFDAB is first introduced, including its topology and conventional modulation methods. Then, MDPSM, which can improve the bidirectional transient, is proposed. In addition, steady-state analysis and bidirectional transient are analyzed in the following sections.

In Chapter 3, the power efficiency is taken into account. MEPT based on MDPSM is proposed. The equations of efficiency are first introduced, followed by the introduction of MEPT. The design process is shown in the last section.

In Chapter 4, the hardware implement of rated 720W AC-CFDAB is introduced.

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Details of the hardware circuit and the DSP program are shown in this chapter.

In Chapter 5, simulation and experiment results are shown. Steady-state waveform of MDPSM, bidirectional transient of MDPSM, and MEPT are verified and discussed in this chapter.

In Chapter 6, the conclusion and the major contribution are summarized. The future works are also listed in this chapter.

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Chapter 2 MDPSM for AC-CFDAB

In this chapter, details of the AC-CFDAB are introduced. In section 2.1, some basic information about AC-CFDAB is reviewed. Section 2.2 introduces the new proposed modified dual-phase-shift modulation(MDPSM) for AC-CFDAB, followed by the power transmission analysis in section 2.3. In section 2.4, the analysis of the bidirectional operation transient is in the end.

2.1 Introduction to AC-CFDAB

In this section, some crucial information including the topology and conventional modulation methods of AC-CFDAB is introduced. In subsection 2.1.1, the topology for AC-CFDAB is introduced. And the existing modulation methods are mentioned in subsection 2.1.2.

2.1.1 AC-CFDAB Topology

AC-CFDAB is composed of two active bridges, a large low-voltage-side inductor, L_{LV}, an active clamp circuit, and a transformer. The detailed topology for AC-CFDAB is shown in Fig. 2.1.

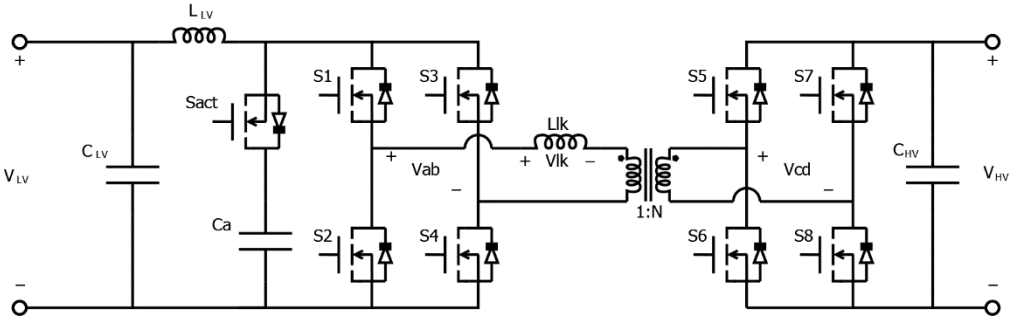

Fig. 2.1 Topology of a AC-CFDAB converter.

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The two voltage sides can be classified into “low-voltage-side(LVS)” and “high-voltage-side(HVS)” by the voltage. In general, LVS is always the current-fed side with a LVS inductor, L_{LV}, and the active clamp circuit. The main reason is that batteries prefer to lower voltage and lower current ripple side. In addition, the voltage-side is always in HVS.

After defining the voltage sides, operation modes are defined by the power flow. “Buck operation” means that the power flow is from HVS to LVS, while “boost operation” means that the power is transferred from LVS to HVS. Bidirectional operation means that the operation is changing from buck operation to boost operation or boost operation to buck operation.

S_1~S_4 are named LVS switches(S_{LV}), while S_5~S_8 are called HVS switches(S_{HV}). In S_{LV}, upper and lower arm switches can turn on simultaneously to provide a current path for L_{LV}. However, S_{HV} should prevent that from shoot-through. Also, some key waveforms of S_{LV} and S_{HV} are different, so they are discussed separately in this thesis.

In S_{HV}, “leading-leg” and “lagging-leg” can be defined by the sequence of the turn-on time. For instance, in the positive half cycle, S_5 turns on earlier than S_8, so S_5 is the leading-leg switch, $S_{\mathrm{HV,lead}}$, and S_8 is the lagging-leg switch, $S_{\mathrm{HV,lag}}$. In this thesis, S_5 and S_6 are defined to the leading-leg switches, whereas S_7 and S_8 are the lagging-leg switches.

An active clamp circuit is composed of a switch, S_{act}, and a capacitor, C_{a}. The main purpose of active clamp circuit is to absorb the imbalance current between L_{LV} and L_{lk}. It can be found that when S_{LVs} turn on, L_{LV} and L_{lk} are connected together. To prevent from the huge voltage spike by the imbalance current, the active clamp circuit should be

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placed.

An AC-CFDAB also contains a transformer. The main purpose of the transformer is to isolate the two voltage sides and enhance the voltage gain. In the following analysis, the leakage inductor, L_{lk}, and magnetic inductor, L_m, are taken into consideration. And the voltages of each side, V_{ab} and V_{cd}, play important roles in MDPSM.

2.1.2 Existing Modulation Methods

With the previous introduction of AC-CFDAB, it can be found that control methods for S_{LVs} and S_{HVs} are different. Upper and lower arms of S_{LVs} are able to turn on together due to the current-fed topology in LVS, so the common control method for S_{LVs} is the duty cycle control. However, since HVS is voltage-fed, upper and lower arms of S_{HVs} should prevent from shoot-through. The common control method for S_{HVs} is the phase shift control. With duty cycle control for LVS and phase shift control for HVS, there are some modulation methods for the two voltage sides to control the power flow of AC-CFDAB.

The modulation method, named ZVZCS modulation, is early proposed in [30] – [33]. In ZVZCS modulation, only one-voltage-side switches are controlled, while the other voltage side switches just provide the current path through their body diodes. For example, only S_{LVs} are controlled in boost mode, while S_{LVs} are the only control parameters in buck mode. The features of ZVZCS modulation are that soft-switching can be achieved in all controlled switches. In buck mode, ZCS can be achieved in $S_{HV,lag}$, and ZVS can be achieved in $S_{HV,lead}$ and S_{act}. In boost mode, ZVS can be achieved in all S_{LVs} and S_{act}. The key waveform of the ZVZCS modulation is shown in Fig. 2.2.

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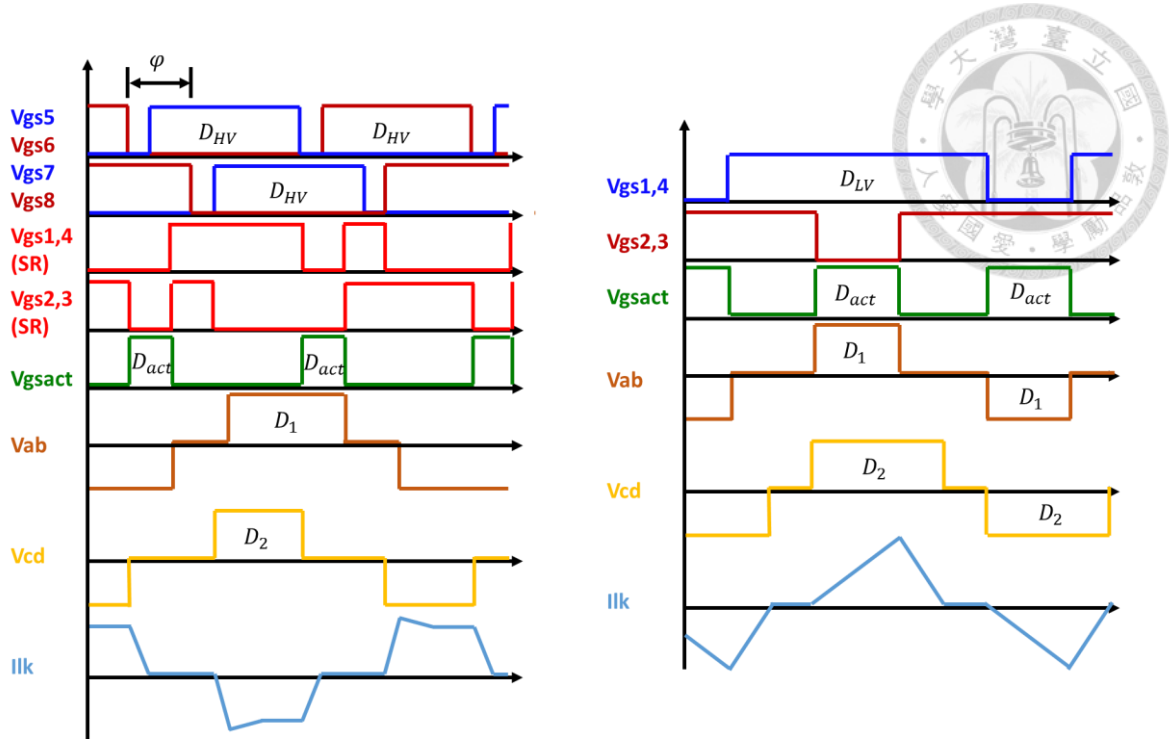

(a) Buck mode. (b) Boost mode.

Fig. 2.2 Key waveform in ZVZCS modulation.

In order to pursue higher efficiency, synchronous rectified(SR) technology is applied. However, to prevent from shoot-through with S_{act}, ZVZCS modulation has some limits in realizing SR. Some switches should turn on and turn off twice in a period, which is complex to generate switching signals. In [34], a secondary-side modulation(SSM) is proposed to solve this problem. In SSM, all of the switches, including S_{LV} and S_{HV}, are controlled, and the power flow is controlled by the HVS phase shift. Also, all switches can achieve ZVS with proper deadtime. The key waveform of SSM is shown in Fig. 2.3. However, the challenge in commuting operation is discussed in [34]. The main reason is that the control methods for switches are a little different between buck and boost modes, which causes poor transient when changing two different operation modes. To solve this problem, MDPSM is proposed in the next section.

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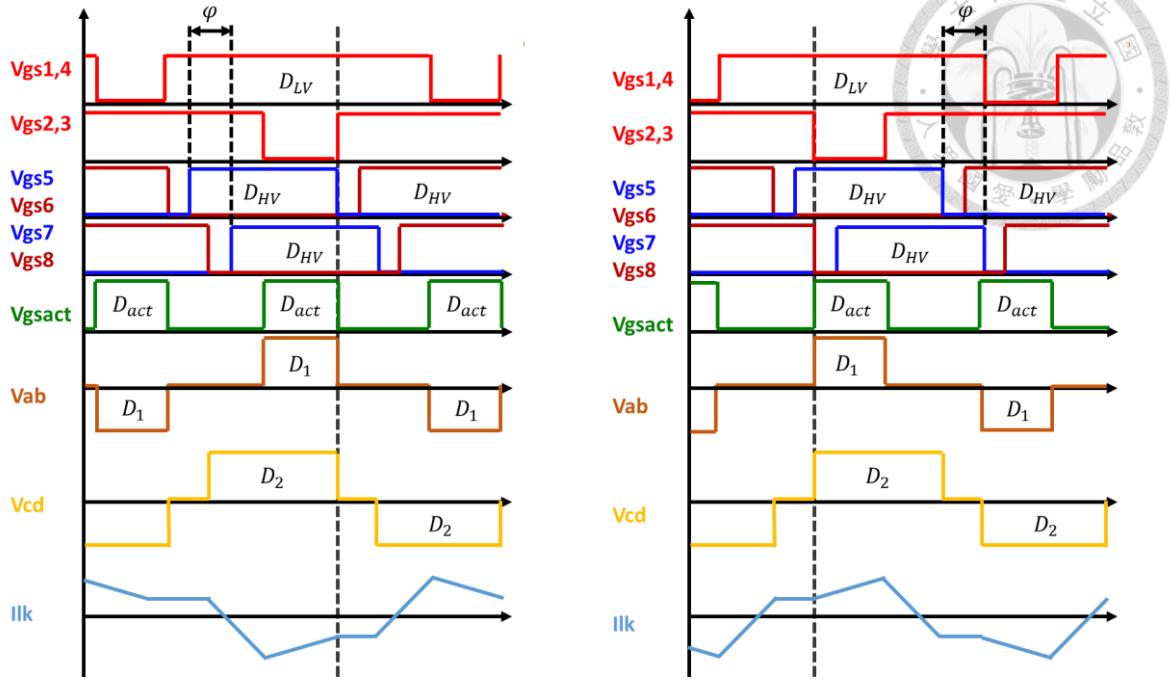

(a) Buck mode. (b) Boost mode.

Fig. 2.3 Key waveform in SSM.

2.2 Modified Dual Phase Shift Modulation

Dual Phase Shift Modulation (DPSM) is a very popular modulation method for VFDAB. The earliest concept of DPSM is first proposed in [35], and is used in VFDAB in [36]. The main concept of DSPM is that the total circuit is controlled by two phase shift, phase shift of S_{HV} and phase shift between S_{LV} and S_{HV}. This concept is also used to CFDAB in [37], but hasn't been used to AC-CFDAB at present.

In this section, Modified Dual Phase Shift Modulation (MDPSM), based on conventional DPSM, for AC-CFDAB is proposed. The feature of MDPSM is that it can achieve bidirectional operation without setting buck and boost modes dividedly, so bidirectional transient can be obviously improved. In subsection 2.2.1, the details of the modulation are introduced. Circuit operation is illustrated in subsection 2.2.2, power transmission is analyzed in subsection 2.2.3, and the ZVS condition is discussed in

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subsection 2.2.4.

2.2.1 Modulation Method

In this subsection, the switch modulation of MDPSM is proposed. The modulation of each part is introduced in the following.

(a) LVS modulation

In S_{LVs}, the duty cycles of S_{LVs}, D_{LV}, are all the same and fixed. S_{LVs} have the same switching status with the diagonal switches and 180° phase difference between the adjacent switches. That is, S_1 turns on and off together with S_4, and has 180° phase difference with S_2 and S_3. Also, in order to provide a continuous current path in LVS, D_{LV} should be larger than 0.5, which generates a period named "overlapping region" that all S_{LVs} turn on. Besides, the "non-overlapping region" is the period that just two S_{LVs} turn on.

S_{act} should turn on to absorb imbalance current in the non-overlapping region because L_{LV} and L_{lk} are connected together in that region. And S_{act} must turn off in the overlapping region to prevent the active clamp capacitor, Ca, from shoot-through.

V_{ab} is generated by LVS modulation. Fig. 2.4 shows the key LVS waveform of MDPSM. The duty cycle of V_{ab}, D_1, is the period of the non-overlapping region, where LVS is connected with the active clamp circuit. Also, V_{ab} can be expressed as (2.1).

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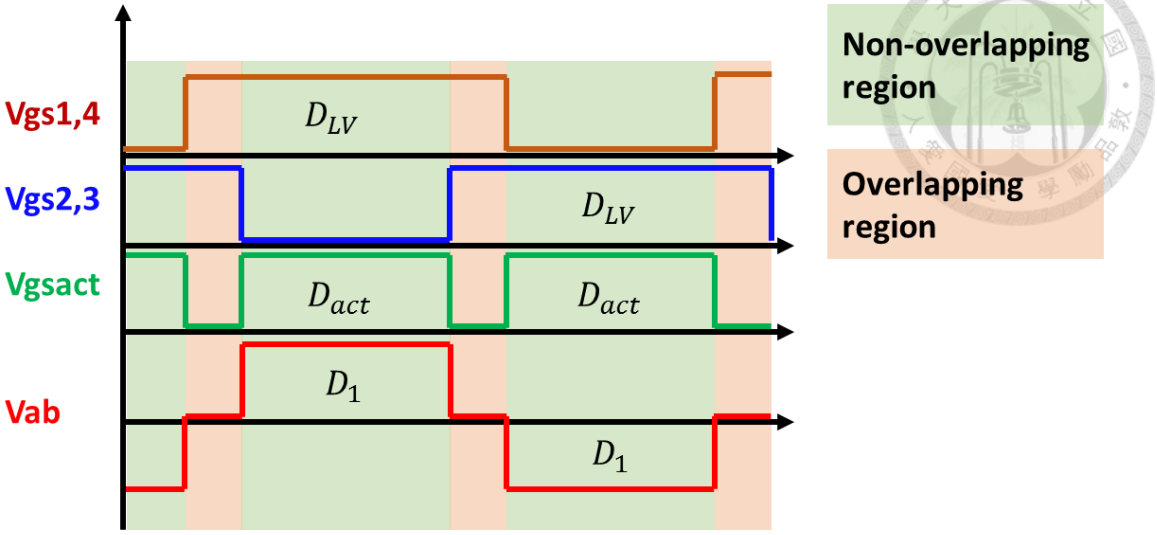

Fig. 2.4 Key LVS waveform in MDPSM.

$$V_{ab} = \begin{cases} V_{ca}, & non-overlapping\ region \\ & (positive-half-cycle) \\ 0, & overlapping\ region \\ -V_{ca}, & non-overlapping\ region \\ & (negative-half-cycle) \end{cases} \quad (2.1)$$

(b) HVS modulation

S_{HVS} have the same and fixed duty cycle as 0.5 ideally, but HVS deadtime(D_{ds}) are always set to achieve ZVS in MDPSM. The upper arm switches should have 180° phase difference with the lower arm switches to prevent from shoot-through. The phase between leading-leg switch S_5 and lagging-leg switch S_8 is named as "HVS phase shift". The region between the turn-on time of S_5 and S_8 is called the "phase-shift region", while the other period is named the "non-phase-shift region".

V_{cd} is generated by HVS modulation. Fig. 2.5 shows the key HVS waveform of MDPSM. The duty cycle of V_{cd}, D_2, is the period of the non-phase-shift region, where HVS is connected with the HVS source. In addition, V_{cd} can be expressed as (2.2).

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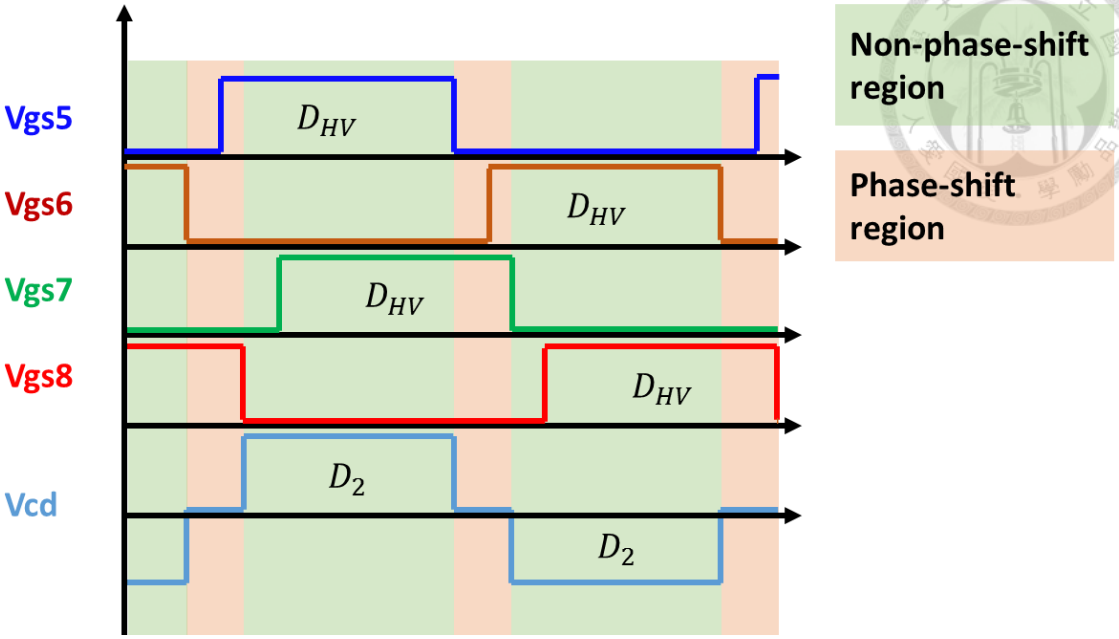

Fig. 2.5 Key HVS waveform in MDPSM.

$$V_{cd} = \begin{cases} V_{HV}, & non-phase-shift\ \ region \\ & (positive-half-cycle) \\ 0, & phase-shifted\ \ region \\ -V_{HV}, & non-phase-shift\ \ region \\ & (negative-half-cycle) \end{cases} \quad (2.2)$$

(c) LVS-HVS Modulation

Fig. 2.6 shows the modulation of two voltage-side. The phase-shift between the rising edge of V_{cd} and V_{ab} is defined as φ_{HL}, which is a control parameter in MDPSM. In addition, D_2, the duty cycle of V_{cd} is also a control parameter. From the perspective of the controlled switches, φ_{HL} is the phase-shift between the falling edge of S_1 and S_8, and D_2 is 0.5 minus HVS phase-shift. That is, two phase-shifts are controlled in MDPSM. In order to simplify the control, the two phase-shifts are decoupled. In MDPSM, φ_{HL} is used to control the transfer power, and D_2 is used to control the efficiency.

In MDPSM, some limits are set to realize some features. First, φ_{HL} must be larger

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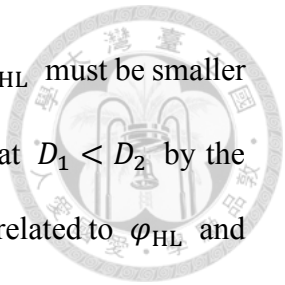

than 0 and V_{ca} must larger than $\frac{V_H}{N}$ to ensure ZVS for S_{act}. Also, φ_{HL} must be smaller than $D_2 - D_1$ to ensure ZVS for S_{LVs}. That is, it can be derived that $D_1 < D_2$ by the limit of φ_{HL}. With this setting, the transmission power is negative correlated to φ_{HL} and the bidirectional power transmission can be realized.

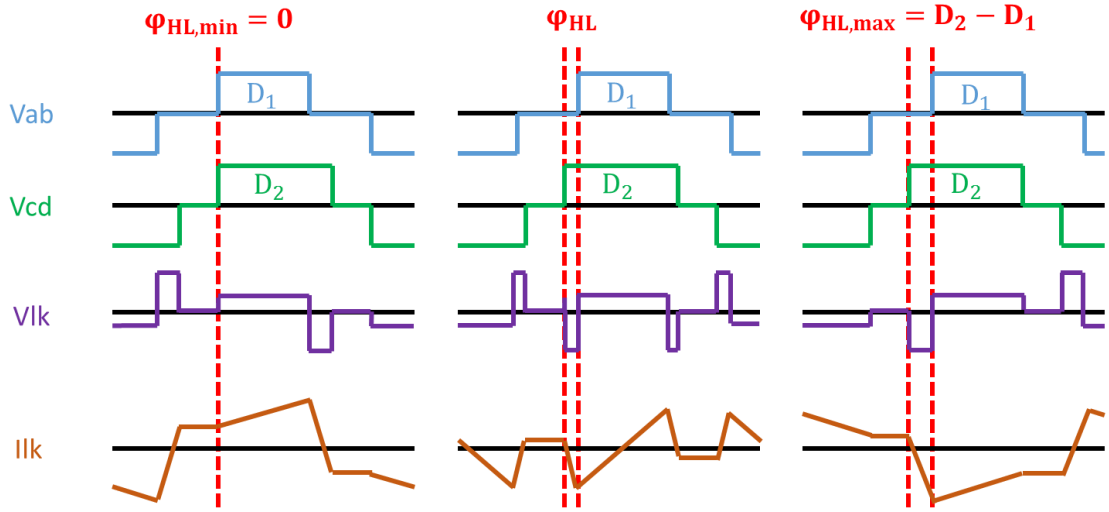

Fig. 2.6 Key waveform in MDPSM.

2.2.2 Circuit Operation

In this subsection, the circuit operation of MDPSM method is illustrated. There are four modes in a half cycle. The current paths of buck operation are shown in Fig. 2.7 - Fig. 2.10, and Fig. 2.11 – Fig. 2.14 show the current paths of boost operation. The detail analyses of the positive-half-cycle buck operation are shown first.

(a) Mode I.

Mode I begins as one $S_{HV,lead}$ (S_6 in this case) turns off and ends when one S_{LV} group (S_2 and S_3 in this case) turns off. The total period of this mode is $\varphi_{HL}T_s$. All S_{LVs} and the other $S_{HV,lead}$ (S_5 in this case) all turn on in this mode. One $S_{HV,lag}$ (S_8 in this case) can achieve ZVS turn-on with the proper setting of the deadtime. The detailed

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current paths are illustrated in Fig. 2.7.

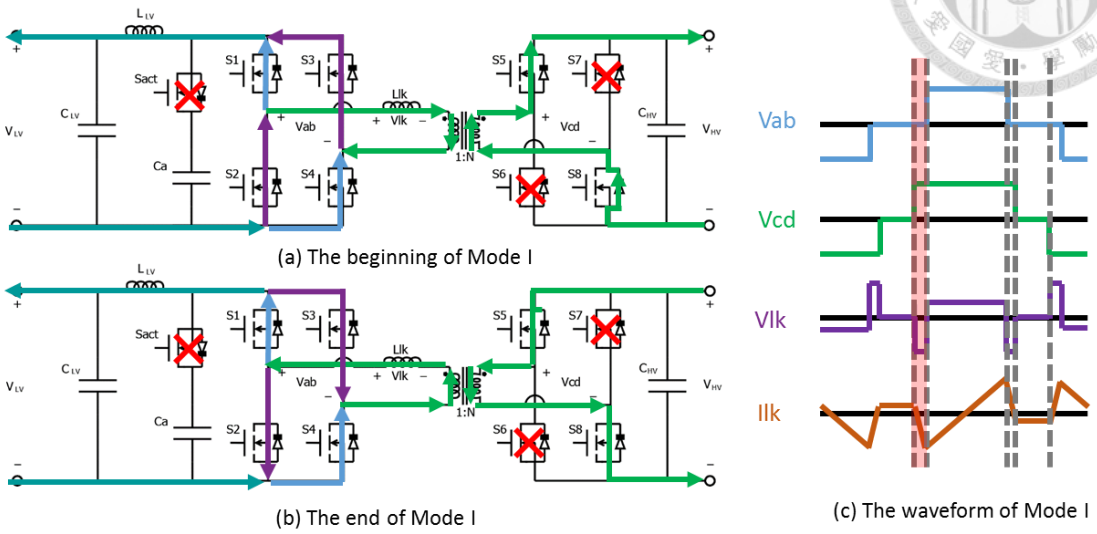

Fig. 2.7 Mode I in buck operation.

After S_6 turns off, the HVS current is forced to discharge the parasitic capacitor, C_{ds8}. If S_8 turn on after having already been discharged, that is, the proper deadtime of S_8 is set, S_8 can achieve ZVS turn-on.

To obey the Kirchhoff's Current Law(KCL), (2.3) and (2.4) can be written. It can be found in (2.4) that the imbalance current of I_{L} and I_{Lk} freewheels in S_{LVs}. Because this imbalance current is not involved in the power transmission, it can also be named "circulating current". In the light load case, circulating current plays an important role in the total power loss.

$$\begin{cases} I_L = I_{S1} + I_{S2} \\ I_{Lk} = I_{S1} - I_{S2} \end{cases} \tag{2.3}$$

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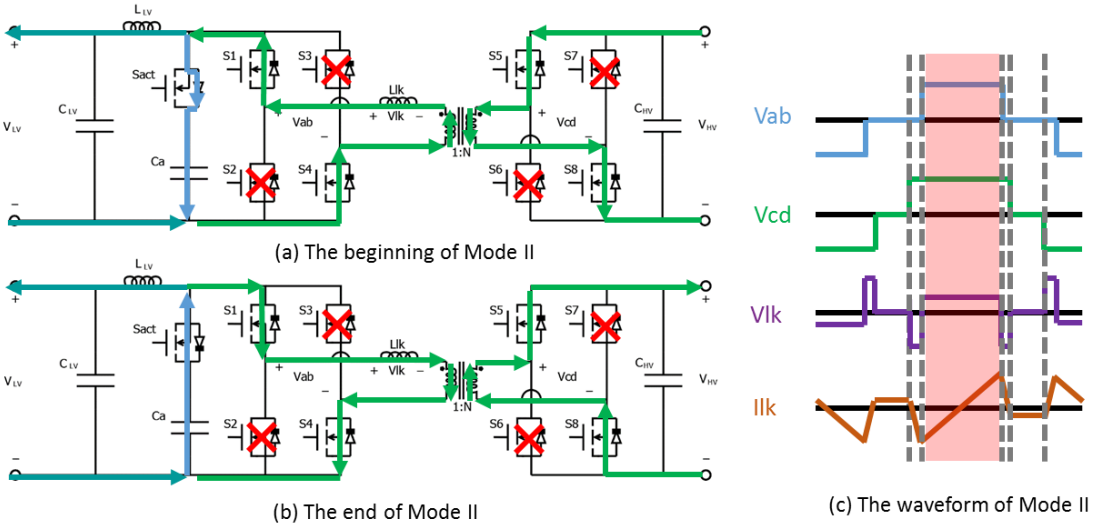
$$\begin{cases} I_{S1} = \dfrac{I_L + I_{Lk}}{2} = I_L - \dfrac{I_L - I_{Lk}}{2} \\ I_{S2} = \dfrac{I_L - I_{Lk}}{2} \end{cases} \tag{2.4}$$

Also, in this mode, the voltage of L_{LV} is equal to V_{LV}, and V_{lk} is equal to $-\frac{V_{\mathrm{H}}}{N}$. I_{lk} decreases gradually and finally commute, which is related to the ZVS for S_{act} in the next mode.

(b) Mode II.

Mode II begins as S_{LV} group (S_2 and S_3 in this case) turns off and ends when S_{act} turns off. The total period of this mode is $D_{\mathrm{act}}T_{\mathrm{s}}$ (also D_1T_{s}). It is the non-overlapping region defined in the last section. S_1, S_4, S_5 and S_8 all turn on in this mode, while S_2, S_3, S_6 and S_7 all turn off. S_{act} can achieve ZVS turn-on with proper setting of the deadtime. The detail current paths are in Fig. 2.8.



(a) The beginning of Mode II

(b) The end of Mode II

(c) The waveform of Mode II

Fig. 2.8 Mode II in buck operation.

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After (S_2, S_3) turn off, the circulating current in S_{LVs} is eliminated. The imbalance current of L_{LV} and L_{Lk} flows into the active clamp circuit. At the same time, the charge in $C_{\mathrm{ds,act}}$ is discharged. If the proper deadtime of S_{act} is set, ZVS of S_{act} can be achieved.

In this mode, the voltage of L_{LV} is equal to V_{Ca}, and V_{lk} is equal to $V_{\mathrm{ca}} - \frac{V_{\mathrm{H}}}{N}$. Because V_{ca} is larger than $\frac{V_{\mathrm{H}}}{N}$ in MDPSM, I_{lk} keeps increasing and finally changes its direction in this mode, which is related to the ZVS of some LVS switches in Mode III.

This mode is the only mode that the power is transferred to the load. In steady-state, the average of active clamp current, I_{act}, is equal to zero, so the average of I_{lk} is the average value of I_{L} in this mode .

(c) Mode III.

Mode III begins as S_{act} turns off and ends when one $S_{\mathrm{HV,lead}}$ (S_5 in this case) turns off. The total period of this mode is $\varphi_{H\mathrm{L}}{}'T_{\mathrm{s}}$. Switches S_1, S_4, S_5 and S_8 all turn on in this mode, while S_{act}, S_6, and S_7 all turn off. One S_{Lv} group (S_2 and S_3 in this case) can achieve ZVS turn on in this mode with proper deadtime. The detailed current paths are in Fig. 2.9.

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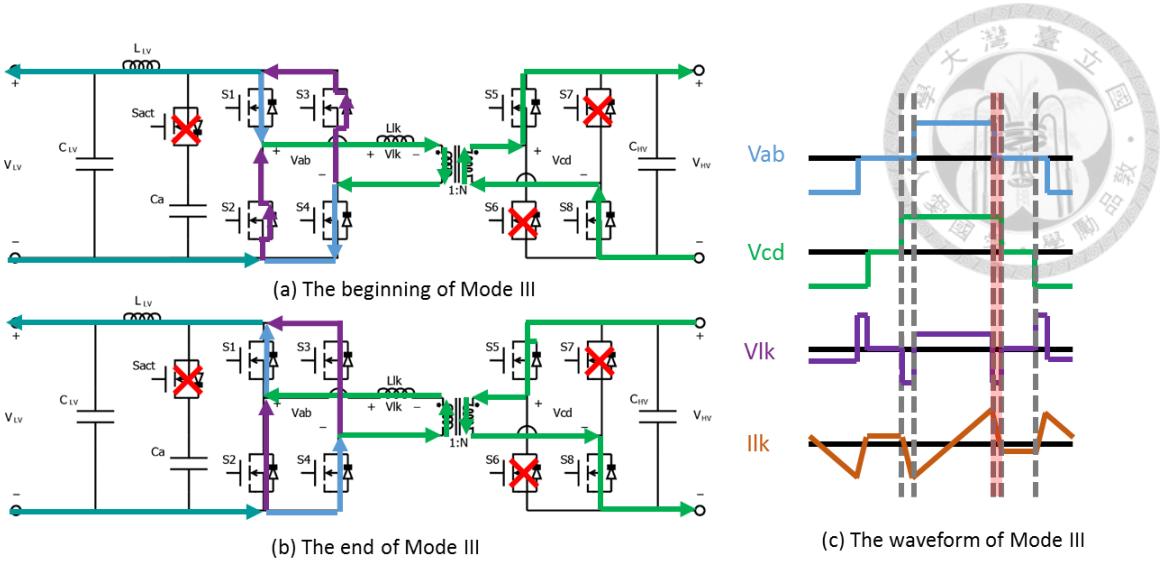

Fig. 2.9 Mode III in buck operation.

After S_{act} turns off, the imbalance current of I_{L} and I_{Lk} becomes the circulating current in S_{LVs} and flows into S_2 and S_3. The charges of C_{ds2} and C_{ds3} are discharged in this mode. If the property deadtime of S_2 and S_3 are set, both switches can achieve ZVS.

In this mode, the voltage of L_{LV} is equal to V_{LV}, and V_{lk} is equal to $-\frac{V_{\mathrm{H}}}{N}$. I_{lk} keeps decreasing and finally change its direction in this mode, which is related to the ZVS of the S_6 in Mode IV.

(d) Mode IV.

Mode IV begins as one $S_{\mathrm{HV,lead}}$ (S_5 in this case) turns off and ends when one $S_{\mathrm{HV,lag}}$ (S_8 in this case) turns off. The total period of this mode is $(0.5-D_2)T_{\mathrm{s}}$. S_1~S_4 and S_8 all turn on in this mode, and the other $S_{\mathrm{HV,lead}}$ (S_6 in this case) can achieve ZVS turn on with the proper deadtime. The detailed current paths are in Fig. 2.10.

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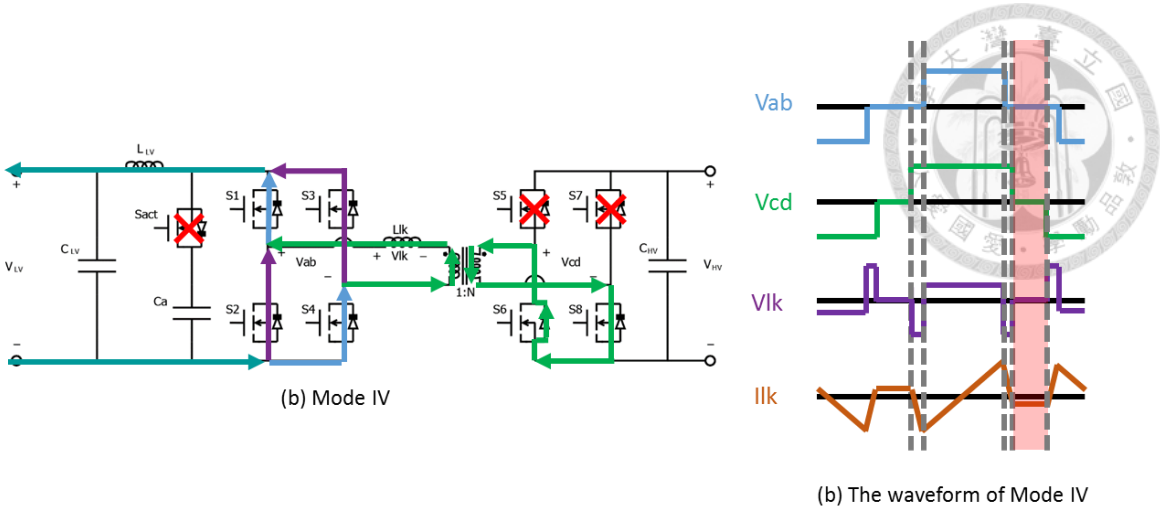

Fig. 2.10 Mode IV in buck operation.

After S_5 turns off, the HVS leakage current flows into S_6. Also, the charge of C_{ds6} is discharged in this mode. If the property deadtime of S_6 is set, ZVS can be achieved.

In this mode, the voltage of L_{LV} is equal to V_{LV}, and V_{lk} is equal to 0, so I_{lk} doesn't change. And the direction of the leakage current plays a role in the ZVS for S_7 in the other half cycle.

(e) Boost operation case.

The previous analysis is all for buck operation. Because the concept of boost operation is similar to buck operation, the directions of current flows in boost operation are almost the same as the buck operation. Fig. 2.11 ~ Fig. 2.14 show the detailed waveforms in boost operation. Note that some periods of the mode are different with buck operation.

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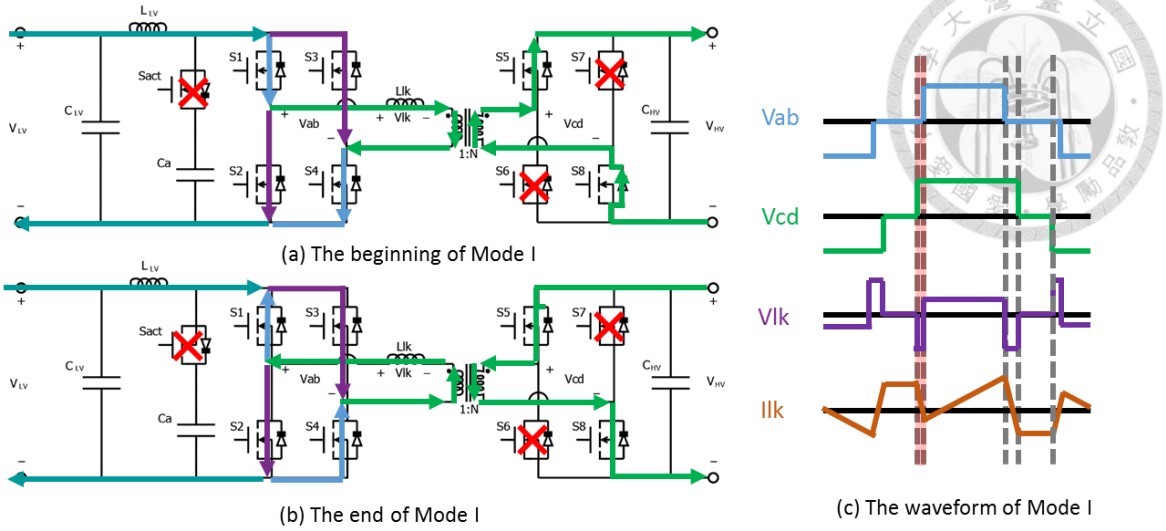

Fig. 2.11 Mode I in boost operation.

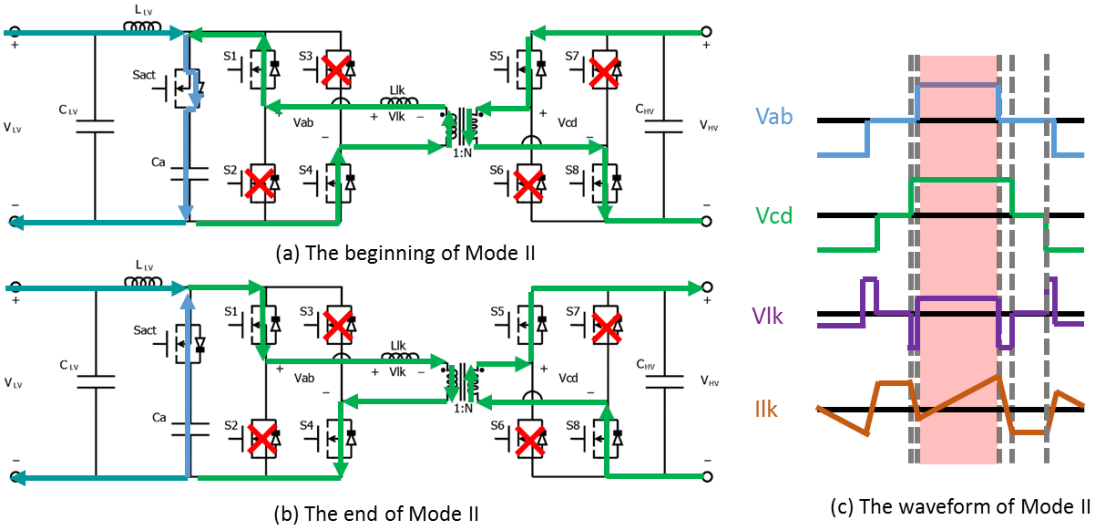

Fig. 2.12 Mode II in boost operation.

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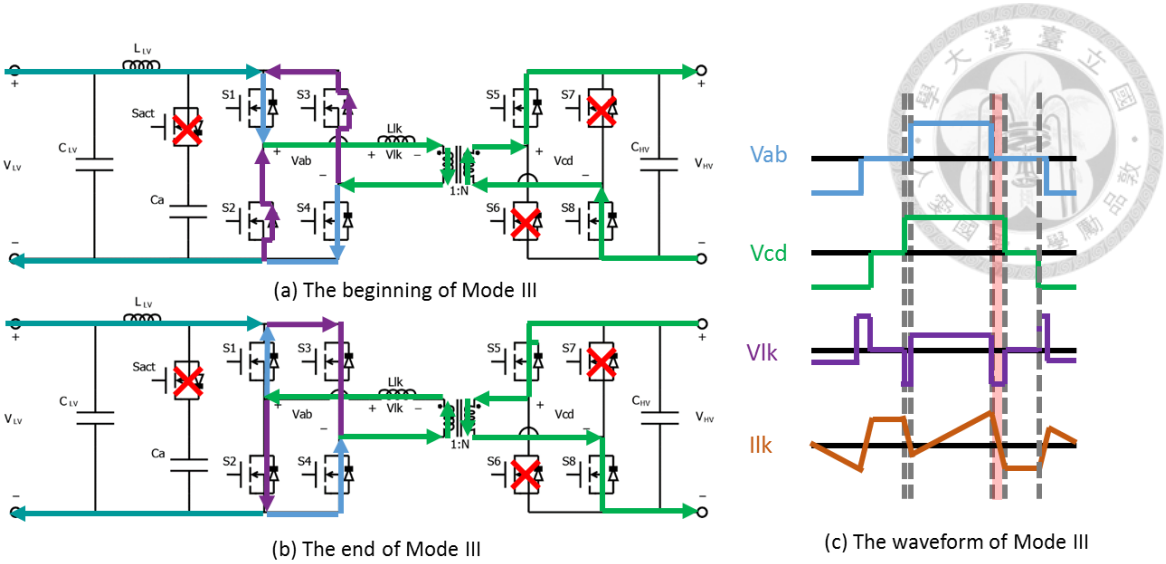

Fig. 2.13 Mode III in boost operation.

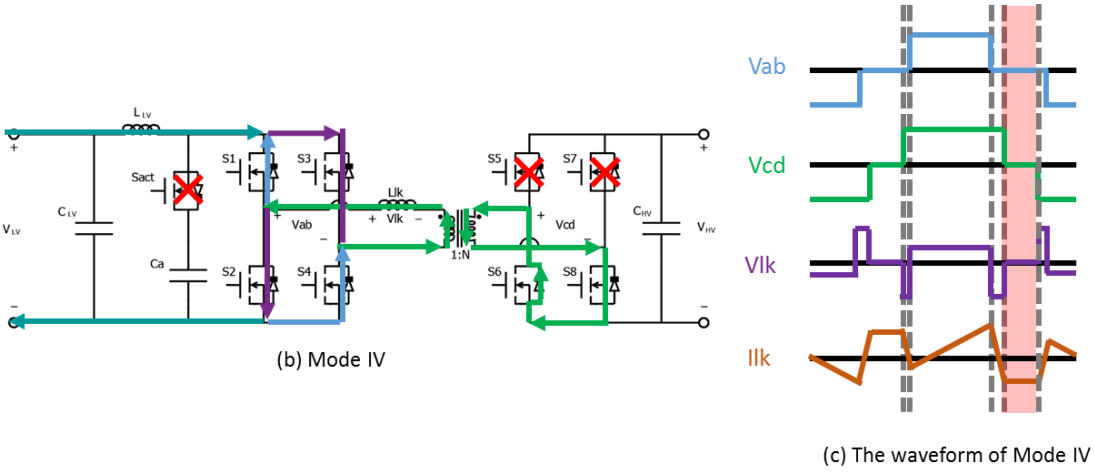

Fig. 2.14 Mode IV in boost operation.

2.2.3 ZVS Condition

In section 2.2.2, it is proved that ZVS can be achieved by setting the proper deadtime of switches. In this subsection, details about the deadtime setting are introduced.

(a) Definition of variables.

D_{td1} and D_{td2} are the time delays set in the non-overlapping region. D_{td1} means

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the time delay between the beginning of the non-overlapping region and the rising edge of D_{act}, while D_{td2} means the time delay between the falling edge of D_{act} and the end of the on-overlapping region. D_{td1} can be regard as the deadtime of S_{act}, and D_{td2} can be seen as the deadtime of S_{LVs} In addition, $D_{d,lead}$ is the deadtime of $S_{HV,lead}$, while $D_{d,lag}$ is the deadtime of $S_{HV,lag}$. Fig. 2.15 illustrates the deadtime setting of each switch.

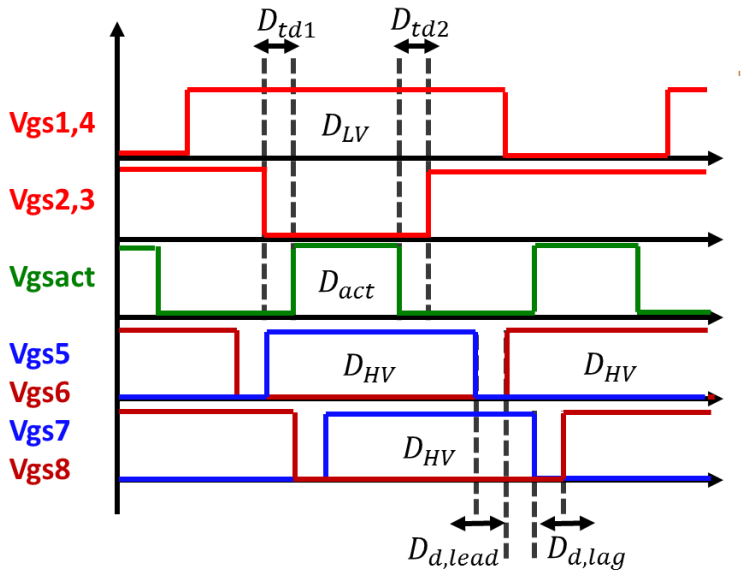

Fig. 2.15 Deadtime setting in MDPSM.

$I_{act,max}$ is the maximum current from the active clamp capacitor. It is related to the ZVS condition of S_{act} and can be derived by (2.5).

$$I_{act,max} = \frac{V_{ca} - \frac{V_H}{N}}{L_{lk}} \frac{D_{act} T_s}{2} = \frac{D_{act} T_s (V_{ca} - \frac{V_H}{N})}{2 L_{lk}} \tag{2.5}$$

I_{lk_4} is the leakage current in Mode IV. Because V_{lk} is equal to 0 in Mode IV, the

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leakage current doesn't change in the ideal case. It is related to the ZVS condition of the HVS switches. By (2.28) and (2.31), (2.6) can be derived.

$$I_{lk\_4} = \frac{T_s}{2L_{lk}}\left(D_2\frac{V_H}{N} - D_{act}V_{ca}\right) \tag{2.6}$$

$I_{lm,max}$ is the maximum magnetic current of the transformer. If the magnetic inductor of the transformer is considered, $I_{lm,max}$ is applied to modify some equations. The value of $I_{lm,max}$ is shown in (2.7).

$$I_{lm,max} = \frac{V_H D_{act} T_s}{2NL_k} \tag{2.7}$$

(b) Equation for minimum deadtime.

Fig. 2.16 is the equivalent circuit of the resonant discharging model. The differential equation can be written as (2.8) and the general solution is (2.9). With the initial condition of V_{ds0} and I_{ds0}, the particular solution can be shown in (2.10).

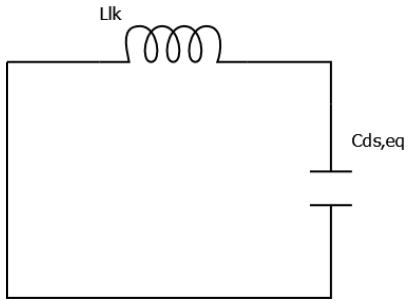

Fig. 2.16 Equivalent resonant model.

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$$\begin{cases} V_{\mathrm{ds}}(t) = L_{\mathrm{lk}} \dfrac{dI_{\mathrm{ds}}(t)}{dt} \\ I_{\mathrm{ds}}(t) = -C_{\mathrm{ds,eq}} \dfrac{dV_{\mathrm{ds}}(t)}{dt} \end{cases} \tag{2.8}$$

$$V_{ds}(t) = C_1 \, sin\left(\frac{t}{\sqrt{L_{lk}C_{ds,eq}}}\right) + C_2 \, cos\left(\frac{t}{\sqrt{L_{lk}C_{ds,eq}}}\right) \tag{2.9}$$

$$V_{ds}(t) = -I_{ds0}\sqrt{\frac{L_{lk}}{C_{ds,eq}}} \, sin\left(\frac{t}{\sqrt{L_{lk}C_{ds,eq}}}\right) + V_{ds0} \, cos\left(\frac{t}{\sqrt{L_{lk}C_{ds,eq}}}\right) \tag{2.10}$$

To simplify the calculation, small-angle approximations (2.11) can be applied because the period of resonant is larger than the deadtime. And the simplified equation is (2.12), the minimum duty of deadtime, $D_{deadtime,min}$, can be calculated by (2.13).

$$\begin{cases} \sin(\theta) \approx \theta & ,when \;\; \theta \;\; small \\ \cos(\theta) \approx 1 - \dfrac{\theta^2}{2} \approx 1 & ,when \;\; \theta \;\; small \end{cases} \tag{2.11}$$

$$V_{\mathrm{ds}}(t) \approx V_{ds0} - \frac{I_{ds0}}{C_{\mathrm{ds,eq}}} t \tag{2.12}$$

$$D_{deadtime,min} \approx \frac{C_{\mathrm{ds,eq}} * V_{ds0}}{I_{ds0} * T_s} \tag{2.13}$$

(c) ZVS condition of each switch.

In the previous part, the equation of $D_{deadtime,min}$ is derived. To calculate the ZVS condition, that is, $D_{deadtime,min}$, some crucial variables need to be found.

In S_{act}, the ZVS turn-on timing is in Mode II, where the imbalance current between

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I_L and I_{lk} charges two S_{LVs} and discharges S_{act} simultaneously in the beginning. So the $C_{\mathrm{ds,eq}}$ must be the sum of the three parasitic capacitors, V_{ds0} is the voltage of active clamp capacitor, and I_{ds0} is the imbalance current between I_L and I_{lk}, that is, $I_{act,max}$.

In S_{LV}, the ZVS turn-on timing is in Mode III, where the imbalance current between I_L and I_{lk} discharges two S_{LVs} and charges S_{act} simultaneously in the beginning. So the $C_{\mathrm{ds,eq}}$ must also be the sum of the three parasitic capacitors, V_{ds0} is the voltage of the active clamp capacitor, and I_{ds0} is $I_{act,max}$, too.

In $S_{HV,lead}$, the ZVS turn-on timing is in Mode IV, where the HVS leakage current discharges one $S_{HV,lead}$ and charges one $S_{HV,lag}$ simultaneously in the beginning. So the $C_{\mathrm{ds,eq}}$ must also be the sum of the two parasitic capacitors, V_{ds0} is the voltage of HVS source, and I_{ds0} is I_{lk_4} in the previous analysis.

In $S_{HV,lag}$, the ZVS turn-on timing is in Mode I, where the HVS leakage current charges one $S_{HV,lead}$ and discharges one $S_{HV,lag}$ simultaneously in the beginning. So $C_{\mathrm{ds,eq}}$, V_{ds0}, and I_{ds0} of $S_{HV,lag}$ are same as $S_{HV,lead}$.

Table 2.1 organizes all variables of ZVS condition for each switch. $D_{deadtime,min}$ can be calculated by (2.13), and is listed in (2.14) ~ (2.17).

Table 2.1 Variables of ZVS condition for each switch.

	Turn-on timing	$\boldsymbol{C_{\mathrm{ds,eq}}}$	$\boldsymbol{V_{ds0}}$	$\boldsymbol{I_{ds0}}$
$\boldsymbol{S_{act}}$	Mode II	$C_{ds,act} + 2C_{ds,LV}$	V_{ca}	$I_{act,max}$
$\boldsymbol{S_{LV}}$	Mode III	$C_{ds,act} + 2C_{ds,LV}$	V_{ca}	$I_{act,max}$
$\boldsymbol{S_{HV,lead}}$	Mode IV	$2C_{ds,HV}$	V_H	I_{lk_4}
$\boldsymbol{S_{HV,lag}}$	Mode I	$2C_{ds,HV}$	V_H	I_{lk_4}

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$$D_{td1,min} = \frac{3C_{ds,act}V_{ca}}{I_{act,max}T_s} \tag{2.14}$$

$$D_{td2,min} = \frac{3C_{ds,act}V_{ca}}{I_{act,max}T_s} \tag{2.15}$$

$$D_{d,lead,min} = \frac{C_{ds,equ}V_{ds0}}{I_{lk_4}} = \frac{2C_{ds,HV}V_H}{I_{lk\_4}} \tag{2.16}$$

$$D_{d,lag,min} = \frac{C_{ds,equ}V_{ds0}}{I_{lk_4}} = \frac{2C_{ds,HV}V_H}{I_{lk\_4}} \tag{2.17}$$

(d) ZVS condition for nonideal transformer

In the previous analysis, the transformer is supposed to be ideal with infinity L_m. However, due to the limit of the material, L_m could not be regarded as infinity in some design cases. The effect of L_m is discussed in this part.

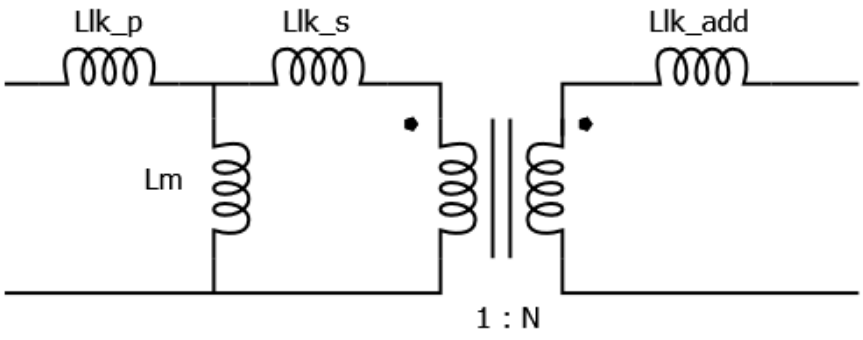

Fig. 2.17 Nonideal transformer circuit.

Fig. 2.17 shows the nonideal model of the transformer circuit. $L_{lk,p}$ and $L_{lk,s}$ are

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the leakage inductors of primary and secondary sides, L_m is the magnetic inductor of the transformer, and $L_{lk,add}$ is the additional inductor to increase the equivalent leakage inductor. Because the analysis of this nonideal model is too complex to analyze, the model should be modified by ignoring some effects. Fig. 2.18 shows the modified nonlinear model. In this model, it is supposed that $\frac{L_{lk,add}}{N^2} \gg L_{lk,p}$ and $L_{lk,eq}$ can be calculated by (2.18). With the modified model, the following analysis can be much easier.

$$L_{lk,eq} = L_{lk,p} + L_{lk,s} + \frac{L_{lk,add}}{N^2} \tag{2.18}$$

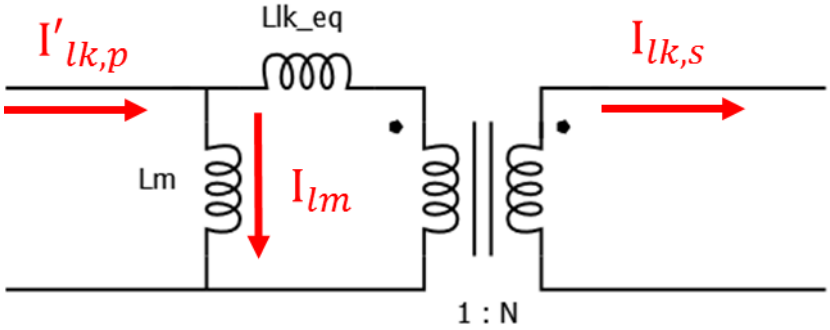

Fig. 2.18 Modified nonideal transformer circuit.

If the L_m is considered, (2.19) can be written by KCL. It can be found that the value of the primary-side leakage current is enhanced. The LVS ZVS condition considered this effect is rewritten as (2.20) ~ (2.22).

$$I'_{lk,p} = I_{lm} + I_{lk,s} * N \tag{2.19}$$

$$I'_{ac,max} = I_{ac,max} + I_{lm,max} \tag{2.20}$$

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$$D'_{td1,min} = \frac{3C_{ds,act}V_{ca}}{I'_{act,max}T_s} \tag{2.21}$$

$$D'_{td2,min} = \frac{3C_{ds,act}V_{ca}}{I'_{act,max}T_s} \tag{2.22}$$

2.3 Power Transmission Control

In this section, the power transmission of MDPSM is analyzed.

The transmission power, P_{T}, can be expressed as (2.23).

$$P_{\mathrm{T}} = \int_0^{T_s} V_{ab}(t)I_{lk}(t)dt = 2V_{ca}\int_0^{D_1T_s} I_{lk}(t)dt \tag{2.23}$$

Assume L_{LV} is large enough to ignore the current ripple, (2.23) can be written as (2.24) because the average leakage current is equal to I_L in Mode II.

$$P_{\mathrm{T}} = 2D_1V_{ca}I_L \tag{2.24}$$

(a) Calculation for V_{ca}.

V_{ca} can be derived by the voltage-second balance of L_{LV}. The voltage-second balance of L_{LV} can be listed as (2.25), and V_{ca} in (2.26) can be solved by (2.25).

$$\int_0^{T_s} V_{L_{LV}}(t)dt = V_{ca} * (2D_1T_s) - V_{LV}T_s = 0 \tag{2.25}$$

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$$V_{ca} = \frac{V_{LV}}{2D_1} \tag{2.26}$$

(b) Calculation for I_L.

In the previous analysis, it can be found that I_L is the average leakage current in Mode II. To express the time equation of I_{lk}, the slope of I_{lk} is first calculated by (2.27).

$$V_{Llk} = L_{lk}\frac{dI_{lk}}{dt} \tag{2.27}$$

Because V_{Llk} and L_{lk} are known in each mode, the slope can be expressed as (2.28). Also the equation of $I_{lk}(t)$ can be derived as (2.29). Also, φ'_{HL} can be calculated as (2.30) by other time constants.

$$\frac{dI_{lk}(t)}{dt} = \begin{cases} -\dfrac{\mathrm{V_H}}{\mathrm{NL_{lk}}} & ,T_0 \le t < T_1(\text{Mode I}) \\ \dfrac{\mathrm{V_{ca}} - \dfrac{\mathrm{V_H}}{\mathrm{N}}}{\mathrm{L_{lk}}} & ,T_1 \le t < T_2(\text{Mode II}) \\ -\dfrac{\mathrm{V_H}}{\mathrm{NL_{lk}}} & ,T_2 \le t < T_3(\text{Mode III}) \\ 0 & ,T_3 \le t < \dfrac{T_s}{2}(\text{Mode IV}) \end{cases} \tag{2.28}$$

$$I_{lk}(t) = \begin{cases} I_{lk}(T_0) - \dfrac{V_H}{NL_{lk}}t, & T_0 \le t < T_1 \\ I_{lk}(T_1) + \dfrac{V_{ca} - \dfrac{V_H}{N}}{L_{lk}}(t - T_1), & T_1 \le t < T_2 \\ I_{lk}(T_2) - \dfrac{V_H}{NL_{lk}}(t - T_2), & T_2 \le t < T_3 \\ I_{lk}(T_3), & T_3 \le t < \dfrac{T_s}{2} \end{cases} \tag{2.29}$$

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$$\varphi'_{HL} = 0.5 - \varphi_{HL} - D_1 - (0.5 - D_2) = D_2 - D_1 - \varphi_{HL} \tag{2.30}$$

Considering the symmetry of the positive and negative half-cycle (2.31), $I_{lk}(t)$ in Mode II can be expressed by (2.32). And I_L can be calculated by averaging the leakage current in Mode II (2.33).

$$I_{lk}(T_0) = -I_{lk}(T_3) \tag{2.31}$$

$$I_{lk_{ModeII}}(t) = \frac{T_s}{2L_{lk}N}[(D_2 - 2\varphi_{HL})V_H - ND_1V_{ca}] + \frac{NV_{ca} - V_H}{L_{lk}N}(t - T_1) \tag{2.32}$$

$$I_L = \int_{T_1}^{T_2} I_{lk_{ModeII}}(t)dt = \frac{T_sV_H}{2L_{lk}N}(D_2 - 2\varphi_{HL} - D_1) \tag{2.33}$$

(c) Power transmission and voltage gain.

Combine (2.24), (2.26), and (2.32), the power transmission can be expressed as (2.34):

$$P_{\mathrm{T}} = P_{\mathrm{L}} = V_L I_L = \frac{T_sV_LV_H}{2L_{lk}N}(D_2 - 2\varphi_{H\mathrm{L}} - D_1) \tag{2.34}$$

Because V_L is fixed by the voltage source, I_L is also regard as the control target of the transfer power. Also, it can be found in (2.34) that the output power range is wider in controlling $\varphi_{H\mathrm{L}}$ than controlling D_2, so $\varphi_{H\mathrm{L}}$ is suitable for controlling transfer power by (2.35) , and D_2 is suitable to control other target, namely efficiency, in MDPSM.

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$$\varphi_{HL} = \frac{D_2 - D_1}{2} - \frac{L_{lk} N I_L}{T_s V_H} \tag{2.35}$$

Fig. 2.19 shows the transfer power in MDPSM. Because the transfer power is proportional to I_L and I_L is related to φ_{HL}, the bidirectional operation can be achieved by changing the value of φ_{HL}, which leads to the better transient than applying two different modulation methods.

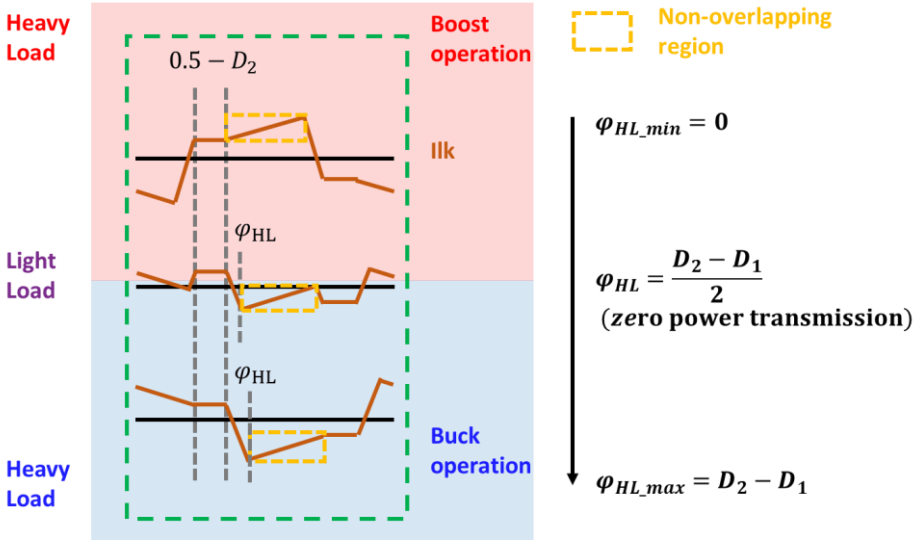

Fig. 2.19 Power transmission in MDPSM.

By (2.34), the voltage gain in buck mode, M_{buck}, can be derived as (2.36) by considering LVS load, R_{buck}, and the voltage gain in boost mode, M_{boost}, can be derived as (2.37) by considering HVS load, R_{boost}.

$$M_{buck} = \frac{V_L}{V_H} = \frac{2 L_{lk} N}{T_s R_{buck} (D_2 - 2\varphi_{HL} - D_1)} \tag{2.36}$$

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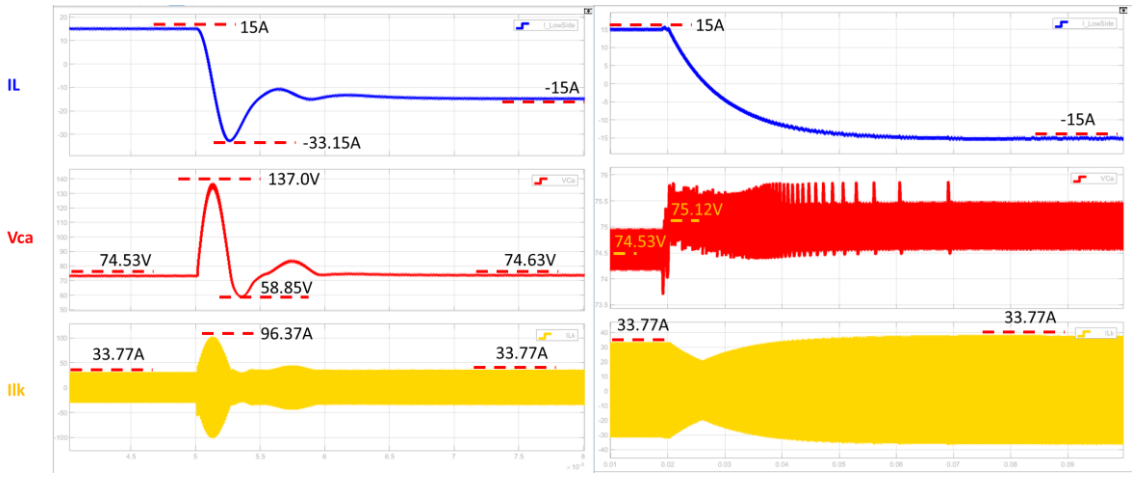
$$M_{boost} = \frac{V_H}{V_L} = \frac{T_s R_{boost}(D_2 - 2\varphi_{HL} - D_1)}{2L_{lk}N} \quad (2.37)$$

2.4 Bidirectional Transient Response

In section2.2, MDPSM is proposed to improve the bidirectional transient compared to SSM. In this section, the waveforms of bidirectional transient responses are shown.

Fig. 2.20 shows the bidirectional transient response of 720W boost-buck operation. It can be found that in SSM, the overshoot of I_L is about 60.5%, while in MDPSM, the overshoot can be eliminated with proper control of φ_{HL}. Also, the spike of V_{ca} and I_{lk} decline obviously in MDPSM. The result shows that the Bidirectional transient response of MDPSM is improved in boost-buck operation.



(a) SSM (b) MDPSM

Fig. 2.20 Bidirectional transient response of boost-buck operation.

Fig. 2.21 shows the bidirectional transient response in 720W buck-boost operation. Same as boost-buck operation, it can be found that the overshoot in I_L decreases in MDPSM. In addition, the spike in V_{ca} and I_{lk} can be improved in MDPSM. With the

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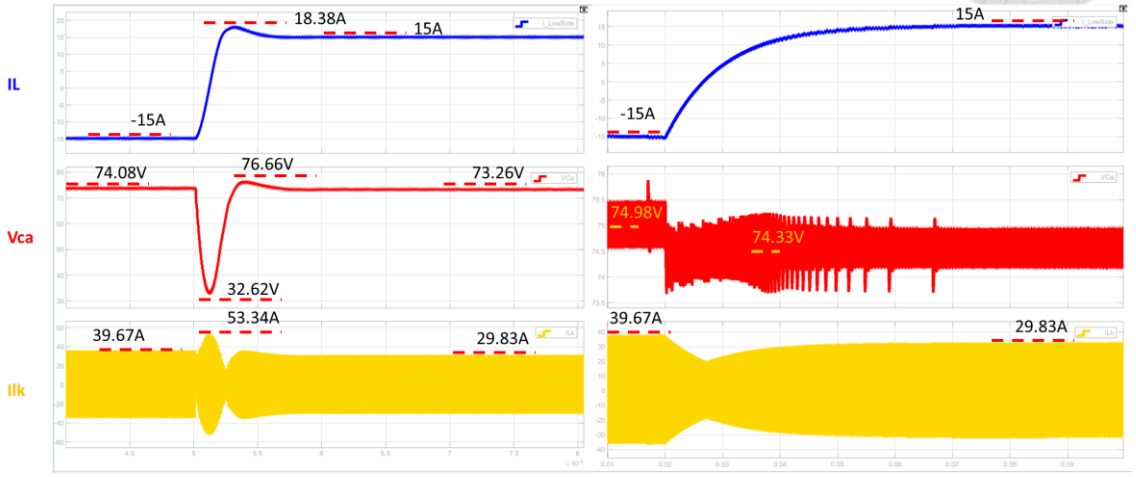
cost of higher setting time, MDPSM has lower spike and higher security than SSM in buck-boost operation.



(a) SSM (b) MDPSM

Fig. 2.21 Bidirectional transient response of buck-boost operation.

The concept of the bidirectional transient improvement can be shown in Fig. 2.22. Fig. 2.22 shows the difference of I_{lk} between SSM and MDPSM. The horizontal red frame shows the boost mode in SSM, while the horizontal blue frame is the buck mode in SSM. In addition, the vertical green frame illustrates the waveform in MDPSM.

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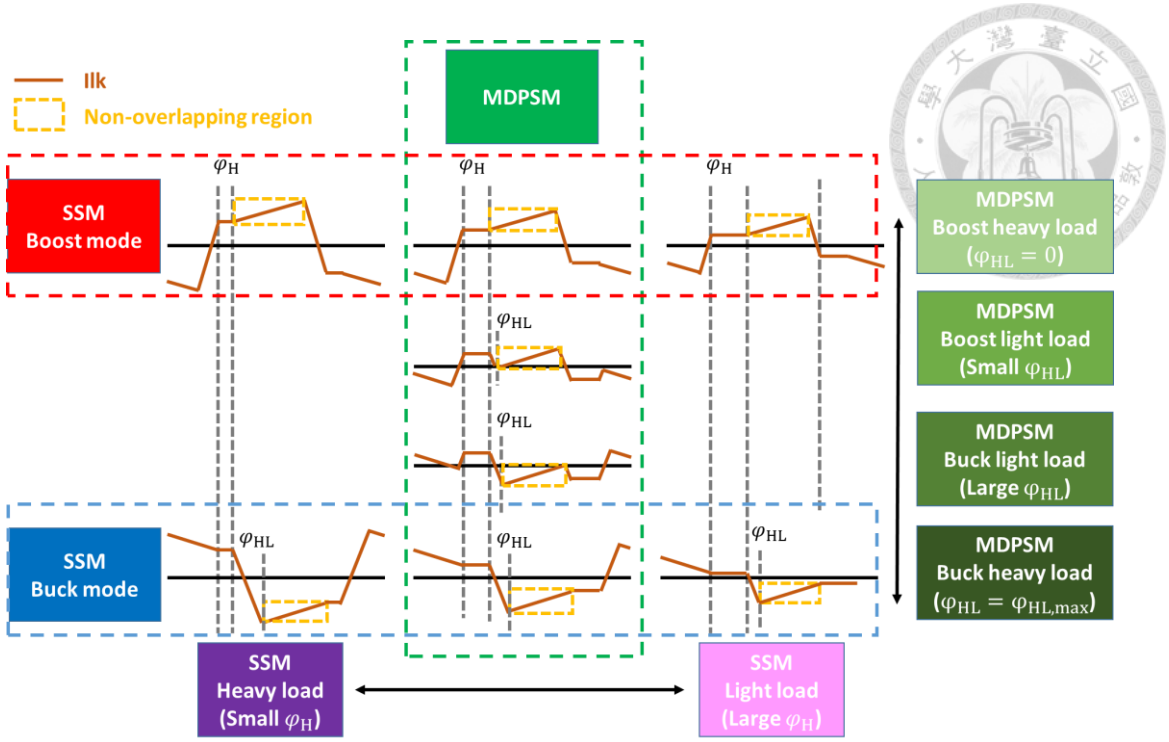

Fig. 2.22 Leakage current waveform between SSM and MDPSM.

In Fig. 2.22, it can be found that the waveform of SSM is the full-load case in MDPSM. The difference between SSM and MDPSM is that SSM is controlled by HVS phase shift, φ_H with fixed φ_{HL}, while MDPSM is controlled by φ_{HL} with fixed φ_H. Though the control parameters of SSM and MDPSM are different, the analysis of SSM can be regard as the full-load case in MDPSM.

Then, the buck-boost operation in SSM can be seen as suddenly change the value of φ_{HL} from minimum to maximum, while maximum to minimum in boost-buck operation. That is, the huge bidirectional transient is generated by heavily changing φ_{HL}. However, in MDPSM, smooth change of φ_{HL} can be achieved with proper control, which leads to better bidirectional transient.

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Chapter 3 Power Efficiency Improvement

In Chapter 2, MDPSM that can improve the bidirectional operation transient is proposed. MDPSM uses two phase-shifts, namely φ_{HL} and D_2, to control the switches. φ_{HL} is used to control the transfer power and the detailed analysis is introduced in section 2.3. In this chapter, the other phase shift, D_2, is taken into account to improve the total power efficiency, and a control strategy for D_2, MEPT, is proposed.

Efficiency equations are provided in section 3.1. A maximum efficiency point tracking strategy(MEPT) for D_2 is proposed in section 3.2 to improve the power efficiency. Details of designing the system parameter are finally introduced in section 3.3.

3.1 Efficiency Equation

Equations of efficiency are shown in this section. The transfer power of AC-CFDAB can be calculated by (2.34). If the power loss, P_{loss}, in (3.1) is considered, the equation becomes (3.2), where P_{sw} means the total switching loss, P_{con} means the total conduction loss, P_{core} means the total core loss, P_{copper} means the total copper loss of the magnetic components, P_{ESR} means loss caused by the ESR. The detailed equations of each power loss term are provided in the following.

$$P_{loss} = P_{sw} + P_{con} + P_{core} + P_{copper} + P_{ESR} \tag{3.1}$$

$$\eta = \begin{cases} \dfrac{P_L - P_{loss}}{P_L}, & P_L \geq 0 \\ \dfrac{|P_L|}{|P_L| + P_{loss}}, & P_L < 0 \end{cases} \tag{3.2}$$

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(a) RMS current equations.

The root-mean-square(RMS) values of current play important roles in P_{con}, P_{copper}, and P_{ESR}. In this part, some key RMS current values in Fig. 3.1 are calculated.

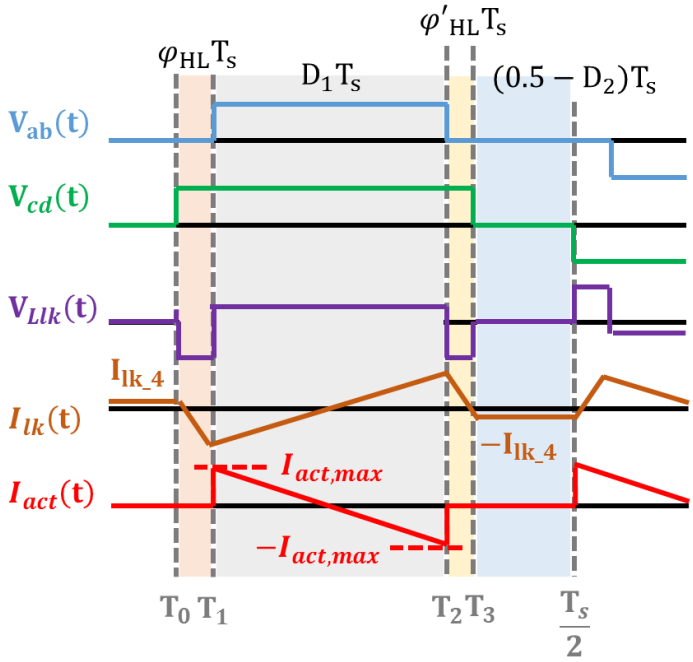

Fig. 3.1 Related waveform in efficiency equation.

The RMS value of the leakage current, $I_{lk,rms}$, is calculated first. The leakage current value of each timing, $I_{lk}(t)$, is shown in (2.29). The leakage current values at the beginning of every mode are listed in (3.3) ~ (3.6).

$$I_{lk}(T_0) = I_{lk_4} = \frac{T_s}{2L_{lk}}\left(D_2\frac{V_H}{N} - D_1V_{ca}\right) \tag{3.3}$$

$$I_{lk}(T_1) = \frac{T_s}{2L_{lk}}\left[(D_2 - 2\varphi_{HL})\frac{V_H}{N} - D_1V_{ca}\right] \tag{3.4}$$

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$$I_{lk}(T_2) = \frac{T_s}{2L_{lk}}\left[(D_2 - 2\varphi_{HL} - 2D_1)\frac{V_H}{N} + D_1 V_{ca}\right] \tag{3.5}$$

$$I_{lk}(T_3) = -I_{lk_4} = -\frac{T_s}{2L_{lk}}(D_2\frac{V_H}{N} - D_1 V_{ca}) \tag{3.6}$$

Suppose I_L is well controlled, φ_{HL} can be written as (2.35), then the RMS value can be calculated by (3.7).

$$I_{lk,rms} = \sqrt{\begin{array}{l} -\left(\frac{{T_s}^2 V_H}{3N{L_{lk}}^2}\right){D_2}^3 + \left(\frac{{T_s}^2 V_H}{4N^2{L_{lk}}^2}\right)(V_H + 2D_1 N V_{ca}){D_2}^2 \\ \hline -\left(\frac{D_1{T_s}^2 V_H V_{ca}}{2N{L_{lk}}^2}\right)D_2 + \frac{D_1 V_{ca}}{6V_H{L_{lk}}^2}\left[(1-2D_1)D_1{T_s}^2 V_H V_{ca} + 12{I_L}^2{L_{lk}}^2 N\right] \end{array}} \tag{3.7}$$

The RMS value of active clamp current, $I_{act,rms}$, is related to the loss of the active clamp circuit. The time equation of I_{act} can be expressed in (3.8) and its RMS value can be calculated by (3.9).

$$I_{act_{Mode\ II}}(t) = I_{act,max} - 2I_{act,max}\frac{t}{D_1 T_s} \tag{3.8}$$

$$I_{act,rms} = \sqrt{\frac{1}{\frac{T_s}{2}}\int_0^{D_1 T_s} {I_{act_{Mode\ II}}}^2(t)dt} = \left(V_{ca} - \frac{V_H}{N}\right)\frac{D_1 T_s}{2L_{lk}}\sqrt{\frac{2D_1}{3}} \tag{3.9}$$

(b) Switching loss term.

The total switching loss includes turn-on loss, $P_{sw,r}$, and turn-off loss, $P_{sw,f}$ with

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every switch (expressed as $P_{sw,x}$ for switch x). The switching transient behavior refers to [38] and shows in Fig. 3.2, where t_{on} and t_{off} can be calculated by (3.10) and (3.11) from [38], V_{TH} is the threshold voltage, and V_{gp} is the voltage of Millar Plateau.

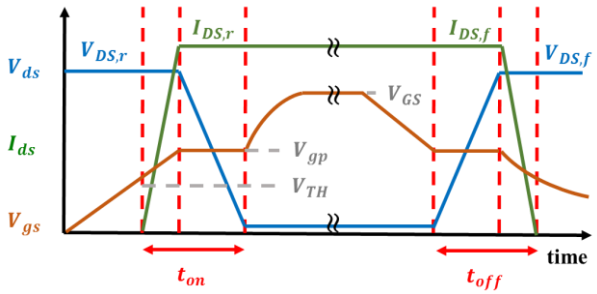

Fig. 3.2 Switching transient behavior in [38].

$$t_{on} = R_G C_{iss} \ln\left(\frac{V_{GS} - V_{TH}}{V_{GS} - V_{gp}}\right) + R_G C_{gd} \frac{V_{DS,r}}{V_{GS} - V_{gp}} \tag{3.10}$$

$$t_{off} = R_G C_{iss} \ln\left(\frac{V_{gp}}{V_{TH}}\right) + R_G C_{gd} \frac{V_{DS,f}}{V_{gp}} \tag{3.11}$$

The total switching loss term can be expressed by (3.12), where $V_{DS,x}$ and $I_{DS,x}$ can be found in Table 3.1.

$$P_{sw} = \sum_x \frac{1}{2}\left(V_{DS,r,x} I_{DS,r,x} t_{on,x} f_{sw} + V_{DS,f,x} I_{DS,f,x} t_{off,x} f_{sw}\right) \tag{3.12}$$

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Table 3.1 Details of switching loss term variables.

Switch	$V_{DS,r,h}$	$I_{DS,r}$	$V_{DS,f}$	$I_{DS,f}$
S_{act}	V_{ca}	$-I_{ac,max}$	V_{ca}	$I_{ac,max}$
S_{LV}	V_{ca}	$-\frac{I_{ac,max}}{2}$	V_{ca}	$\frac{I_{ac,max}}{2}$
$S_{HV,lead}$	V_H	$-\frac{I_{lk\_4}}{N}$	V_H	$\frac{I_{lk\_4}}{N}$
$S_{HV,lag}$	V_H	$-(\frac{I_{lk\_4}}{N}-\frac{V_H D_d T_s}{N^2 L_{lk}})$	V_H	$\frac{I_{lk\_4}}{N}$

$V_{DS,r,h}$ means $V_{DS,r}$ in the hard-switching case. To consider the ZVS condition, $V_{DS,r}$ value can be calculated by (3.13).

$$V_{DS,r,x}=\begin{cases}V_{DS,r,h,x}, & if\ I_{DS,r,x}\geq 0\\ V_{DS,r,h,x},*\ (1-\frac{D_{d,x}}{D_{d,min,x}}), & if\ I_{DS,r,x}<0,\ D_{d,x}<D_{d,min,x}\\ 0, & if\ I_{DS,r,x}<0\ ,\ D_{d,x}\geq D_{d,min,x}\end{cases} \quad (3.13)$$

(c) Conduction loss term.

The conduction loss term can be divided into three groups (S_{act}, S_{LV} and S_{HV}) and shown by (3.14), where $R_{on,x}$ means the on-resistance of each switch and can be found in the datasheet.

$$P_{con}=\sum_x {I_{rms,x}}^2 R_{on,x}=P_{con,act}+P_{con,LV}+P_{con,HV} \quad (3.14)$$

$P_{con,act}$ can be easily calculated by (3.9) and is equal to (3.15).

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$$P_{con,act} = {I_{rms,act}}^2 R_{on,act} \tag{3.15}$$

$P_{con,LV}$ can be calculated by equivalencing LVS turn-on resistances. In subsection 2.2.2, it can be found that I_L flows into four S_{LVs} in Mode II, while flows into two S_{LVs} in other modes. The equivalent resistance of S_{LVs} can be expressed as (3.14) and the conduction loss in S_{LVs} is shown in (3.17).

$$R_{on,LV,eq} = \frac{R_{on,LV} * (0.5 - D_1) + 2R_{on,LV} * D_1}{0.5} = (1 + 2D_1)R_{on,LV} \tag{3.16}$$

$$P_{con,LV} = {I_L}^2 R_{on,LV,eq} = (1 - 2D_1){I_L}^2 R_{on,LV} \tag{3.17}$$

$P_{con,HV}$ can also be calculated by equivalencing HVS turn-on resistances. In subsection 2.2.2, it can be observed that HVS current, $\frac{\mathrm{I_{lk}}}{N}$, flows into two S_{HVs} all the time. The total conduction loss of HVS switches can be written as (3.18).

$$P_{con,HV} = (\frac{I_{lk,rms}}{N})^2 2R_{on,HV} \tag{3.18}$$

(d) Core loss term.

The core loss term is generated by the magnetic components. The conventional calculation process includes three steps. The first step is to calculate the maximum flux density, $\mathrm{B_{max}}$, by Faraday's Law (3.19), where A_e means the effective core cross-section area. The second step is to calculate core loss per volume, $\mathrm{P_v}$, by Steinmetz's equation (3.20), where k, a, and b are called the "Steinmetz's coefficients". In the end,

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the core loss can be calculated by (3.21), where l_e means the magnetic path length

$$V = N * A_e \left| \frac{dB}{dt} \right| \tag{3.19}$$

$$P_V = k f^a {B_{max}}^b \tag{3.20}$$

$$P_{core} = \sum_x P_{V,x} A_{e,x} l_{e,x} \tag{3.21}$$

(e) Copper loss term.

The copper loss term is generated by the magnetic components, too. The general form of the copper loss is (3.22), where the RMS current value of L_{LV} is I_L. The RMS current value of the transformer is equal to $I_{lk,rms}$ or $\frac{I_{lk,rms}}{N}$, depending on the direction of the resistance. The resistance of a wire can be calculated by the resistance equation (3.23), where ρ means the resistivity of the wire, l means the length of the wire, and A means the cross-section area of the wire.

$$P_{copper} = \sum_x {I_{rms,x}}^2 R_{wire,x} \tag{3.22}$$

$$R_{wire} = \rho \frac{l}{A} \tag{3.23}$$

(f) ESR loss term.

The ESR loss term is generated by the ESR of the active clamp capacitor, C_a, and

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can be calculated by (3.24).

$$P_{ESR} = {I_{act,rms}}^2 ESR_{act} \tag{3.24}$$

3.2 Maximum Efficiency Point Tracking Strategy

In this section, the analysis between the efficiency and D_2 is introduced and maximum efficiency point tracking strategy(MEPT) is proposed. In subsection 3.3.1, operation region of D_2 is analyzed, and the efficiency analysis with all operation region is shown in subsection 3.3.2. Finally, the strategy scheme is shown in subsection 3.3.3.

3.2.1 Operation region

In the beginning, the operation region of D_2 is analyzed. The maximum and minimum values of D_2, $D_{2,max}$ and $D_{2,min}$, are estimated in this subsection.

$D_{2,max}$ is analyzed first. To achieve ZVS for $S_{HV,lead}$ in Mode IV, the period of Mode IV, $0.5 - D_2$, must be larger than D_d. That is, $D_{2,max}$ can be expressed as (3.25).

$$D_{2,max} = \ 0.5 - D_d \tag{3.25}$$

$D_{2,min}$ can be calculated in the following rules. There are two limits for $D_{2,min}$. The final value of $D_{2,min}$ must consider the both two limits.

The first limit of $D_{2,min}$ is from the minimum value of $\varphi_{HL}{}'$. The minimum value of D_2 in this case can be expressed as $D_{2,min1}$. $\varphi_{HL}{}'$ can be derived by (2.30), and φ_{HL} in (2.12) can be substituted by (2.35) if the output power is well controlled. The substituted equation is (3.26). Because $\varphi_{HL}{}'$ is the period of Mode III, the time must be

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longer than D_{td2} to assure the ZVS for the S_{LVs}. So $\varphi_{HL}{}' = D_{td2}$, and $D_{2,min,1}$ is shown in (3.27).

$$\varphi'_{HL} = \frac{D_2 - D_1}{2} + \frac{L_{lk} N I_L}{T_s V_H} \tag{3.26}$$

$$D_{2,min1} = D_1 + 2D_{td2} - \frac{2L_{lk} N I_L}{T_s V_H} \tag{3.27}$$

The other limit of $D_{2,min}$ is from the minimum value of φ_{HL}. The minimum value of D_2 in this case can be expressed as $D_{2,min2}$. Because φ_{HL} should be larger than 0 in MDPSM, (3.28) can be derived by (2.35).

$$D_{2,min2} = D_1 + \frac{2L_{lk} N I_L}{T_s V_H} \tag{3.28}$$

The minimum value of D_2 is limited by the above two equations, the final value of $D_{2,min}$ is in (3.29).

$$D_{2,min} = \max(D_{2,min1}, D_{2,min2}) \tag{3.29}$$

Fig. 3.3 shows the operation region of D_2. MDPSM operates in the blue area. It can be found that the wider operation region is in the lighter load case. Also, If the setting of D_2 is out of the analytical region, the circuit would loss ZVS and the operation is not included in MDPSM.

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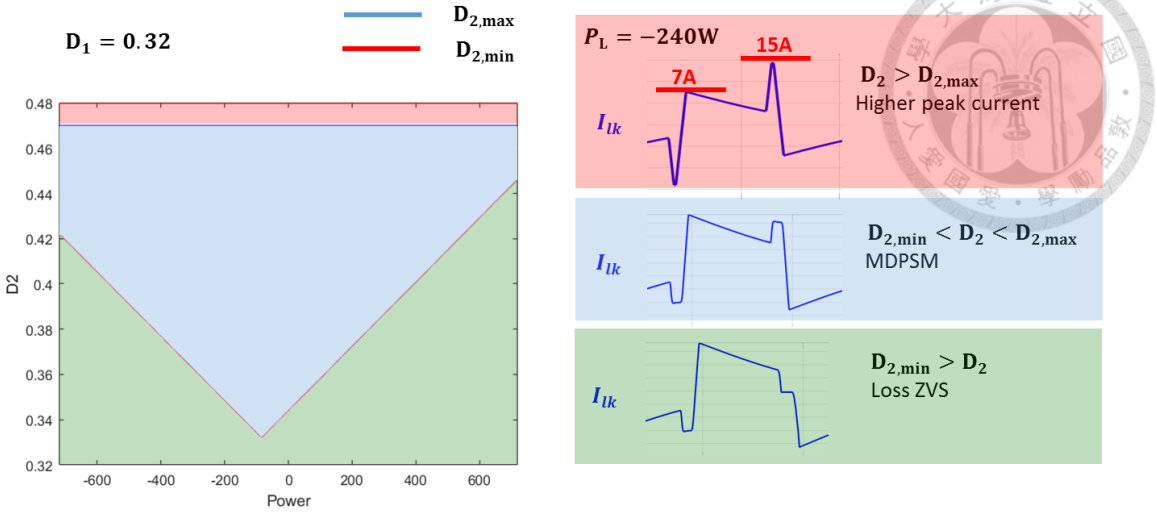

Fig. 3.3 Operation region of D_2.

3.2.2 Efficiency Analysis

In section 3.1, it can be found in (3.1) that the power efficiency is composed of five power loss terms. The relationship between D_2 and each power loss is introduced in the following.

P_{sw} term can be calculated by (3.12). It can be found that the turn-off switching loss is positively correlated to I_{lk_4}, while the turn-on switching loss is negative correlated to $P_{sw,f}$. Because I_{lk_4} is also positively correlated to D_2 and ZVS can be achieved when D_2 is large, P_{sw} term is positively correlated to D_2 when operating in ZVS, while the relationship between D_2 and P_{sw} term depends on cases.

P_{con} term can be calculated by (3.14). The equation of $I_{lk,rms}$ is shown in (3.7) and is negatively correlated to D_2 with the system parameters in this thesis.

P_{core} term is calculated by (3.21). The flux density of the transformer is negatively correlated to D_2. By (3.20), it can be found that P_{core} is negatively correlated to D_2.

P_{copper} term is also related to $I_{lk,rms}$, which is positively correlated to D_2. So P_{copper} is positively correlated to D_2.

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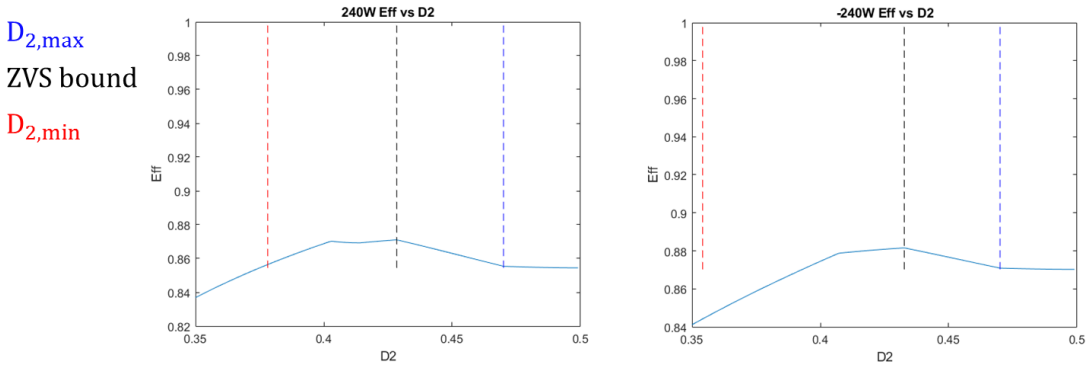
P_{ESR} term is only related to $I_{act,rms}$, which is not related to D_2. So the change of D_2 doesn't influence the value of P_{ESR}.

With the analyses above, it can be concluded that D_2 is related to efficiency. Because P_{sw} and P_{con} play dominant parts in the total power loss, the effect of P_{core} can be neglected in the analysis. It can be found that the power efficiency is negatively correlated to D_2 when operating in ZVS. When losing ZVS, the relation between D_2 and the efficiency depends by the case.

Fig. 3.4 - Fig. 3.6 show the relationship between D_2 and total efficiency. It can be found that power efficiency is indeed negatively correlated to D_2 when operating in ZVS. While losing ZVS, the relationship is not positively or negative correlated to D_2 for sure. For instance, in 480W boost case, the efficiency is negatively correlated to D_2, while the efficiency is positively correlated to D_2 in Fig. 3.5.



(a) 240W boost operation. (b) -240W buck operation.

Fig. 3.4 Relationship between D_2 and efficiency with 240W case.

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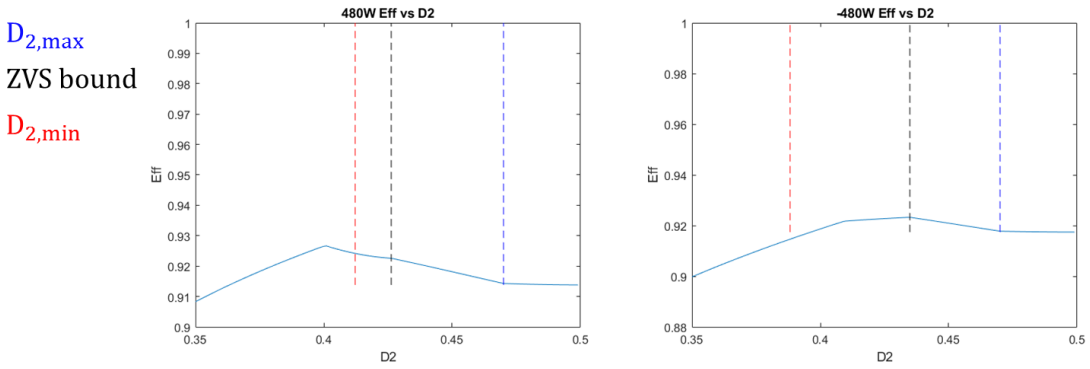
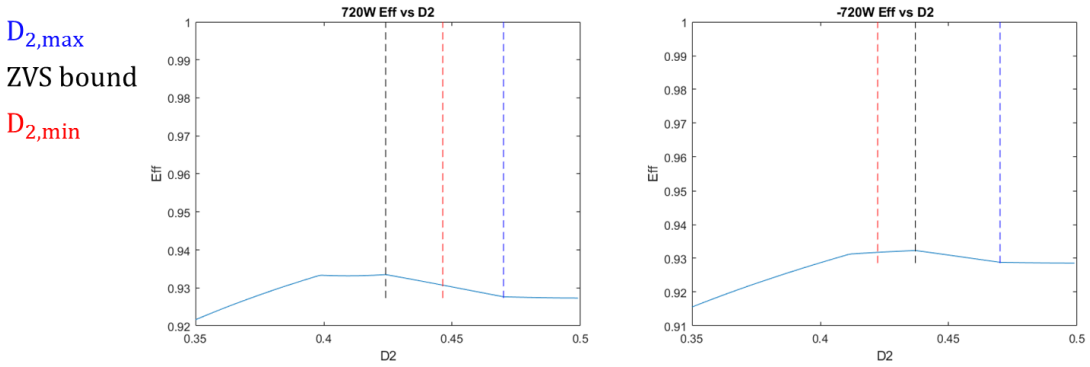


(a) 480W boost operation. (b) -480W buck operation.

Fig. 3.5 Relationship between D_2 and efficiency with 480W case.



(a) 720W boost operation. (b) -720W buck operation.

Fig. 3.6 Relationship between D_2 and efficiency with 720W case.

3.2.3 Strategy Scheme

In subsection 3.2.2, a crucial conclusion that the total power efficiency is related to D_2 can be made. To track the maximum efficiency point of D_2, MEPT based on MDPSM is proposed. The detail of MEPT shows in the following.

Fig. 3.7 shows the control scheme for MEPT. In MDPSM, the transfer power is controlled by φ_{HL}, named "I_L control loop". The maximum efficiency point can be tracked by D_2, that is, controlled by "efficiency control loop". Because the calculation of the maximum efficiency point is too complex to finish in the microcontroller, the

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maximum efficiency point can be traced by some control methods, such as “perturb and observe method”. The details of each control loop are shown in the following.

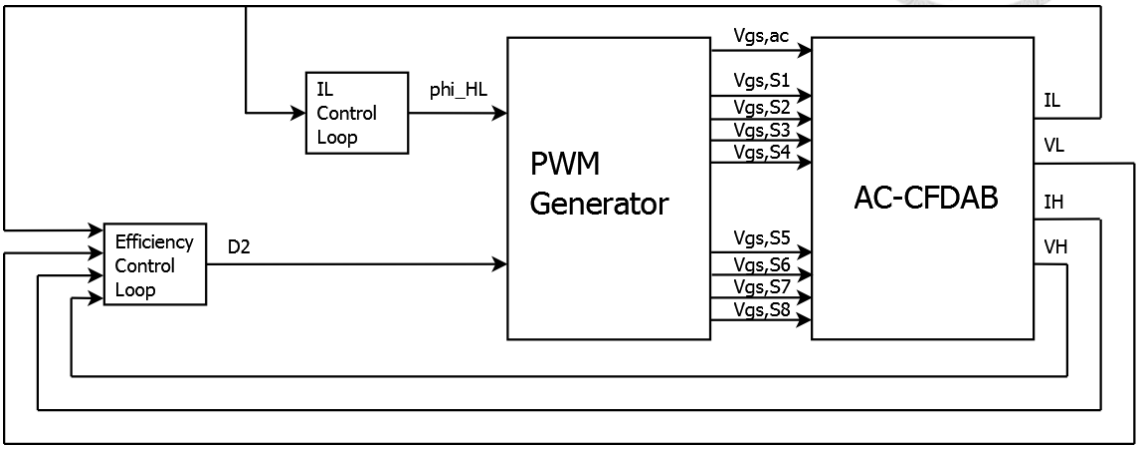

Fig. 3.7 Control scheme for MEPT.

(a) I_L control loop

In I_L control loop, the transfer power can be controlled by φ_{HL}, so I_L is sensed in this control loop and a PI controller is set to control φ_{HL}. The detail control scheme is shown in Fig. 3.8.

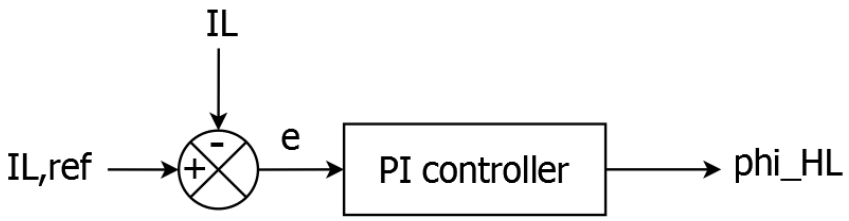

Fig. 3.8 Control scheme for IL control loop.

(b) Efficiency control loop

In efficiency control loop, the relationship between D_2 and the efficiency is used. The control parameter of this control loop is D_2. To track the maximum efficiency point,

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the “perturb and observe method” is applied to find the maximum efficiency point. Also, in order to ensure the power transmission is correct before perturbing, this control loop should start perturb only when the steady-state of the I_L control loop is achieve. That is, the speed of this control loop should be slower than the I_L control loop.

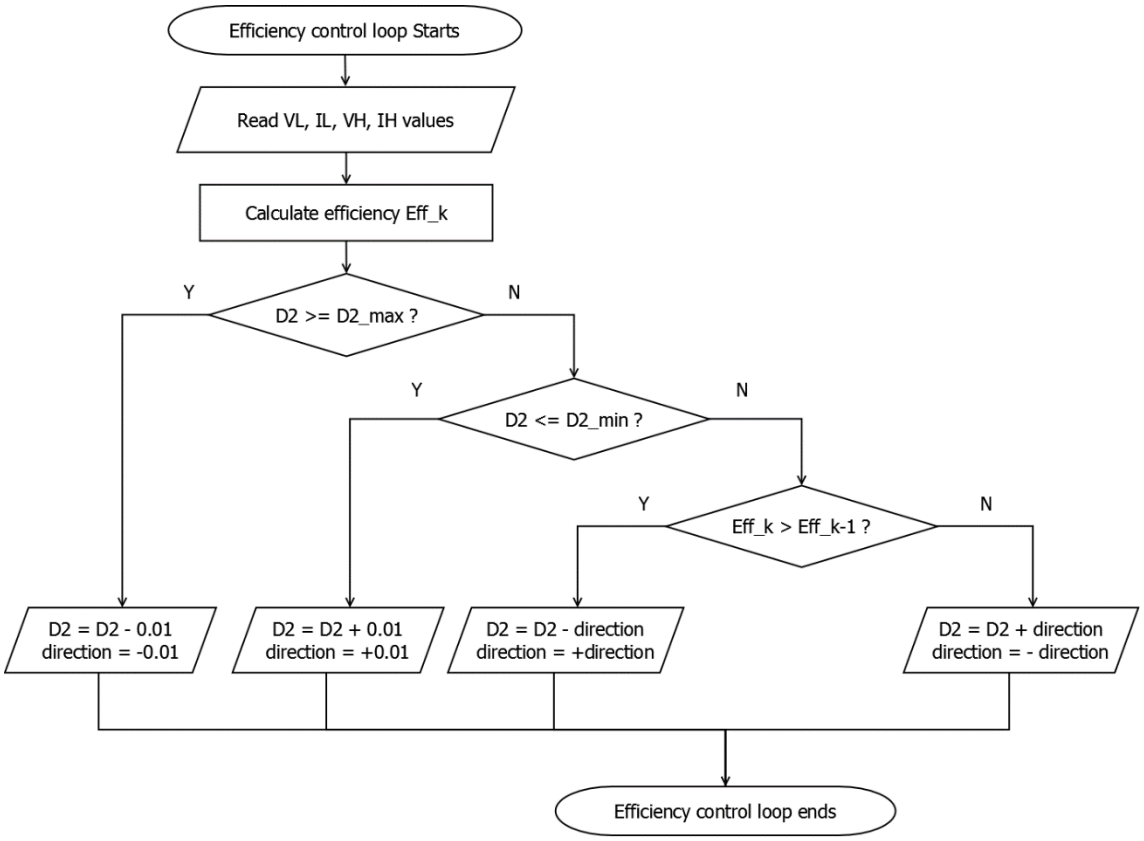

Fig. 3.9 Control flowchart for efficiency control loop.

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3.3 Parameter Design

In this section, the design process of some system parameters is provided as follows.

(a) Design of D_1

D_1 , namely D_{act} in the active clamp circuit, is a parameter related to the range of φ_{HL} and P_f. The design process of D_1 refers to [34]. In [34], D_1 is set to be 0.4 in SSM. However, in MDPSM, the output power range is twice wider than SSM, which means that D_1 should be smaller than 0.4 to realize the wider power range. So D_1 is set to be 0.32.

(b) Design of $D_{2,open}$

$D_{2,open}$ is also a parameter related to the transfer power. By (2.31), it can be found that the larger D_2 can generate wider output power range. To realize the maximum transfer with fixed D_1, $D_{2,open}$ should be set to 0.5-D_d. In this case, $D_{2,open}$ is set to 0.47.

(c) Design of the transformer

The system parameters in the transformer, namely N and L_{lk}, play important roles in the value of I_{lk} and I_L. In MDPSM, N_{min}, the minimum value of N, can be designed first due to the setting of $V_{ca} \geq \frac{V_H}{N}$, where V_{ca} can be calculated in (2.26). However, it can be found in (2.14) that the value of $V_{ca} - \frac{V_H}{N}$ is related to the ZVS condition of S_{act}. To ensure the ZVS operation of S_{act}, the exact value of N is set to be 1.25*N_{min}. Then, L_{lk} can be designed by (2.31). In this case, N is set to be 6.75 and L_{lk} is set to be 2.02μH.

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Chapter 4 Hardware Implementation

In this chapter, a rated 720W AC-CFDAB converter is designed to verify MDPSM and MEPT. The hardware circuit is introduced first in section 4.1, followed by details of DSP program in section 4.2.

4.1 Hardware Design

In this section, the hardware design of an AC-CFDAB is introduced. The power stage circuit includes the power board and the driver board circuit. The control stage circuit contains sensor circuits and a microcontroller. The specification is in Table 4.1. The detail of designing the hardware circuit is introduced in this section.

Table 4.1 System specification.

Rated Power	720W
LVS Voltage	48V
HVS Voltage	400V
Switching Frequency	100kHz
LVS Switching Node Duty (D_1)	0.32
LVS Inductor (L_{LV})	135μH
Transformer Turning Ratio (N)	6.75
Transformer Leakage Inductor (L_{lk})	2.02μH
Active Clamp Capacitor (C_a)	20μF
LVS Deadtime Ratio (D_{td1}, D_{td2})	0.02
HVS Deadtime Ratio ($D_{d,lead}$, $D_{d,lag}$)	0.03

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4.1.1 Power Stage Circuits

The power stage contains a LVS power board, a HVS power board, driver boards, and a transformer. Each of them is introduced in the following.

(a) Power boards.

In the LVS power board, there are a LVS capacitor, a LVS inductor, an active clamp circuit, and a full-bridge circuit. Fig. 4.1 shows the detail of the LVS power board.

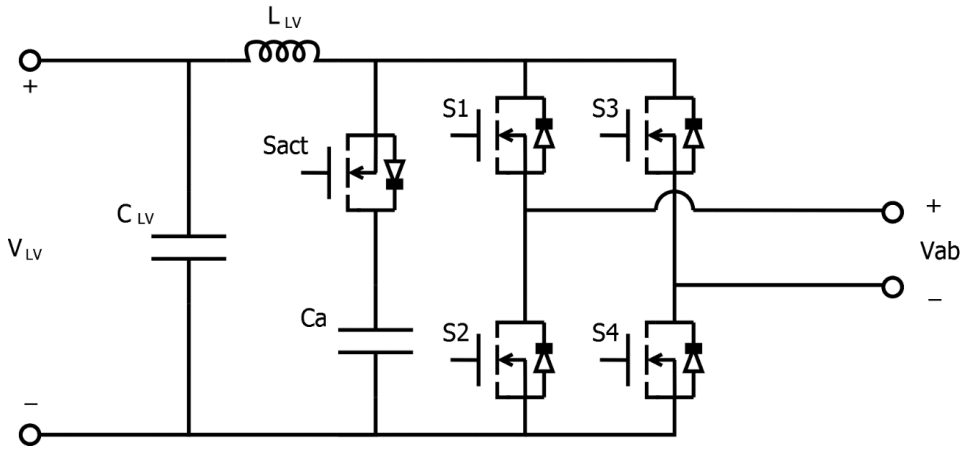

Fig. 4.1 LVS power board.

The main purpose of the LVS capacitor, C_{LV}, is to stabilize the LVS voltage, V_{LV}, so a 470uF/450V electrolytic condenser, whose capacitance is higher than other type of capacitors, is chosen.

The LVS inductor, L_{LV}, plays an important role in decreasing the LVS current ripple. In this circuit, a 135uH inductor is chosen. Consider the core saturation and winding turns, two high flux core CH572060 are applied to realize L_{LV}.

The active clamp capacitor, C_a, is a key component in the active clamp circuit. The capacitance of C_a is related to the voltage ripple of V_{ca}, which is supposed to be a constant in the previous analysis and the transient time in load change. Take both the

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factors into consideration, a 20uF capacitor is chosen. In addition, because active clamp is a crucial part in this circuit, a film capacitor is applied to ensure the stability in the experiment.

Cool MOSFETs are chosen in the active clamp switch, S_{act}, and full-bridge switches, $S_1 \sim S_4$. Cool MOSFET has lower on-resistance than convention MOSFET and is also cheaper than the wide-band-gap(WBG) MOSFET. It is a popular choice in the low voltage case. Due to the same maximum voltage and compatibility of the driver circuit, the Cool MOSFET IRFP4868PBF is chosen in all switches in the LVS power board.

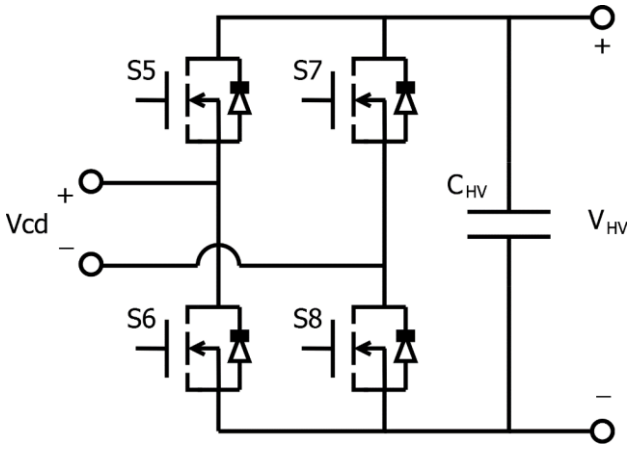

Fig. 4.2 HVS power board.

Fig. 4.2 shows the detail of the HVS power board. There are a full-bridge circuit and a HVS capacitor, C_{HV}, in the HVS power board.

Same as C_{LV}, C_{HV} is applied to stabilize the HVS voltage, V_{HV}, so a 470uF/450V electrolytic condenser is also chosen.

The power loss of HVS switches plays a crucial role in the total power loss. Because of the high maximum voltage, the withstand voltage of HVS switches must be higher than

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LVS switches. However, it is a tradeoff between the withstand voltage and the turn–on resistance. Higher withstand voltage leads to higher turn-on resistance, which causes higher power loss. To decrease the power loss, WBG switches are chosen in this case. WBG MOSFETs have the higher bandgap and higher withstand voltage than conventional MOSFETs, which is popular in high voltage cases. In HVS power board, SiC MOSFETs, which are suitable for the high power case, H1M065F050 are chosen.

(b) Driver boards.

Fig. 4.3 and Fig. 4.4 are the circuit of LVS and HVS driver boards. Driver IC UCC21530 is chosen to drive both Cool MOSFETs and SiC MOSFETs. UCC21530 is an isolated dual-channel gate driver from TEXAS INSTRUMENTS. It has the proper output range (25V to -5V) and enough driver current (source current 4A/ sink current 6A) that is very suitable for both Cool MOSFETs and SiC MOSFETs. The details of the driver board designs are in the following.

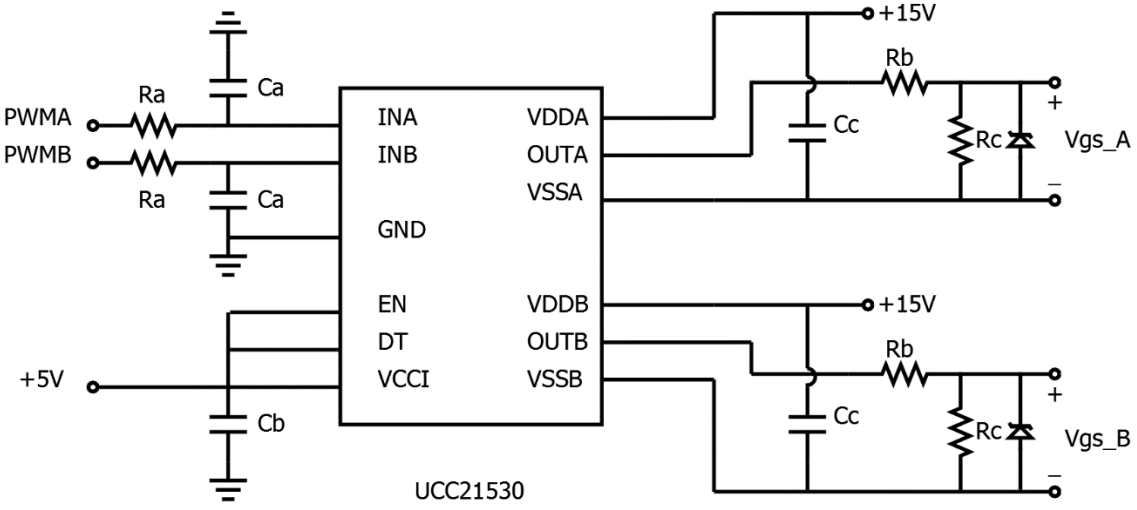

Fig. 4.3 LVS driver board.

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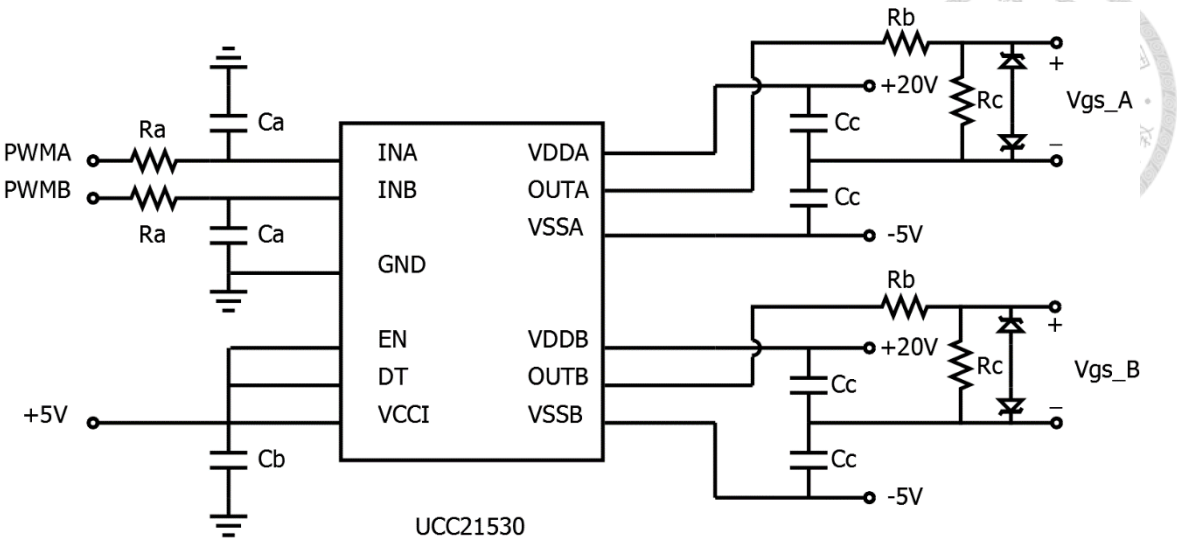

Fig. 4.4 HVS driver board.

R_a and C_a form a RC low-pass filter to decrease the influence of the input noise. The cutoff frequency of the filter is in (4.1). In this case, the cutoff frequency is set to be 100MHz.

$$f_{cutoff} = \frac{1}{2\pi RC} \tag{4.1}$$

EN and DT pins are two functions of this driver IC. EN pin is related to the output channel. If EN is high, both output channel A and B are enable. While both output channel are disable as EN pulling low. DT pin is the dead time function pin. If deadtime resistor, R_{DT}, is placed between DT pin and GND pin, the output signal deadtime(ODT) is set by (4.2) . If two output signal is overlapped, the DT function needs to be disable with DT pin connecting with VCCI pin. In this case, EN function must be enable and DT function must be enable, so both pins are connecting with VCCI pin.

$$ODT(in\ \ ns) = 10 * R_{DT}(\text{in } \text{k}\Omega) \tag{4.2}$$

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R_b and C_c play an important role in the process of driving MOSFETs. The design process refers to [39] and the related model is in Fig. 4.5. The resistors and capacitors can be designed by (4.3) ~ (4.5), where $R_{G,min}$ is the additional gate resistor, $C_{o+,min}$ is the minimum output capacitor for positive driver source, $C_{o-,min}$ is the minimum output capacitor for negative driver source, V_{gate+} is the output positive gate voltage, V_{gate-} is the output negative gate voltage, I_{source} is the peak source current of the driver, $R_{G,MOSFET}$ is the gate resistor of the MOSFET, Q_{gate} is the total driving power of the MOSFET, V_{drop} is the output voltage drop.

In this case, R_G, which is R_b in Fig. 4.3 and Fig. 4.4, is selected to be 5.1Ω, C_{o+} and C_{o-}, which are C_c in Fig. 4.3 and Fig. 4.4, are selected to be 10.22uF.

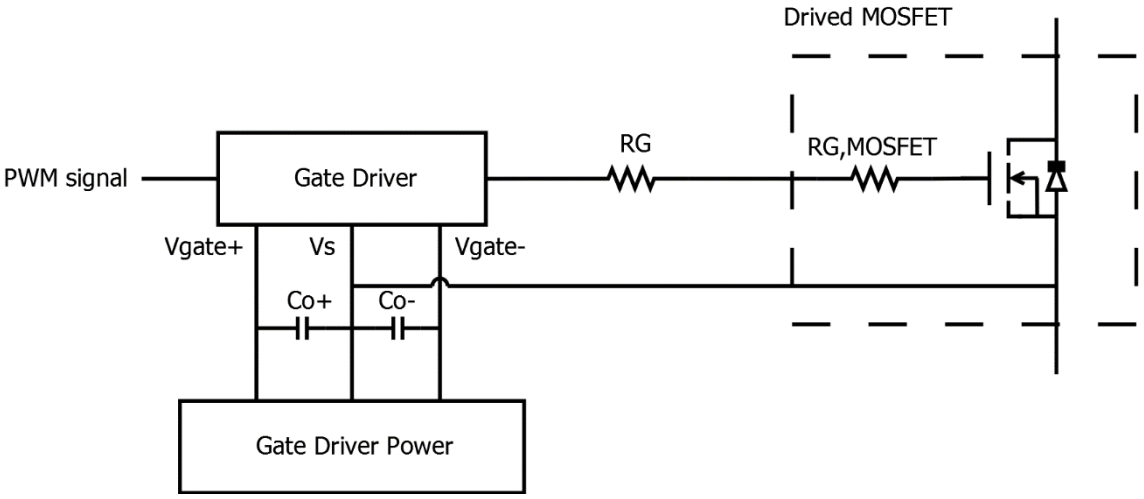

Fig. 4.5 Driver circuit model in [39].

$$R_{G,min} = \frac{V_{gate+}}{I_{source}} - R_{G,MOSFET} \tag{4.3}$$

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$$C_{o+,min} = \frac{2 * Q_{gate} * V_{gate+}}{{V_{gate+}}^2 - (V_{gate+} - V_{drop})^2} \quad (4.4)$$

$$C_{o-,min} = \frac{2 * Q_{gate} * V_{gate-}}{{V_{gate-}}^2 - (V_{gate-} - V_{drop})^2} \quad (4.5)$$

The main purpose of R_c is to ensure the low voltage level when open loop. Its resistance should not be too small to influence the driving ability, so in this case R_c is chosen to be 10kΩ.

(c) Transformer design

The transformer isolates the switching node voltage, V_{ab} and V_{cd}. Its leakage inductor, L_{lk}, and magnetic inductor, L_m, play crucial roles in power transmission and ZVS condition. Also, in MDPSM, V_{ca} must be larger than $\frac{V_H}{N}$. With the limit above, the detailed parameter is set in Table 4.2. To consider the core saturation, EE65 material is chosen in this circuit.

Table 4.2 Transformer parameter.

$\boldsymbol{L_{lk,LV}}$	2.02 **μ**H
$\boldsymbol{L_{m,LV}}$	66 μH
$\boldsymbol{N}$	6.75
$\boldsymbol{R_{copper,LVS}}$	0.006Ω
$\boldsymbol{R_{copper,HVS}}$	0.018Ω

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4.1.2 Control Stage Circuits

The control stage circuits contain a microcontroller and sensing circuits. In order to calculate the total efficiency, voltages and currents from LVS and HVS should be sensed. However, some output voltages of sensing components are too high for the microcontroller, so some additional circuits are applied to transfer the sensing signal. In this section, the detailed design of the control stage circuit is shown.

(a) Voltage sensing circuits

Voltage sensing circuits consist of two operational amplifiers, TL084, some voltage-divided resistors and some filter resistors and capacitors. These sensor circuits measure LVS and HVS voltage respectively. The topologies of LVS and HVS voltage sensing circuits are both the same and are shown in Fig. 4.6. A total voltage sensing circuit can be divided into a voltage divider circuit, a differential amplifier circuit, a Sallen-Key filter and a voltage protection circuit, all of which are introduced in the following.

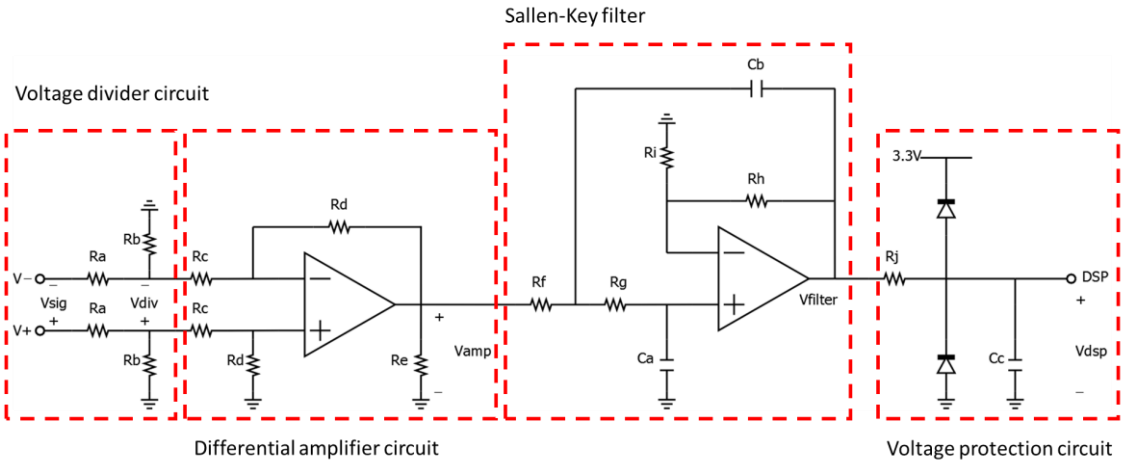

Fig. 4.6 Voltage sensing circuit.

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The voltage divider circuit transfers the input sensor signal, V_{sig}, into V_{div} by a simple resistor divider. To take the next stage resistor, R_c, into consideration, the overall transfer function is (4.6).

$$\frac{V_{div}}{V_{sig}} = \frac{R_b // R_c}{R_a + R_b // R_c} = \frac{R_b R_c}{R_a R_b + R_b R_c + R_a R_c} \tag{4.6}$$

The differential amplifier circuit uses an operational amplifier to transfer the sensing voltage. The transfer function of this circuit is (4.7).

$$\frac{V_{amp}}{V_{div}} = \frac{R_d}{R_c} \tag{4.7}$$

The Sallen-Key lowpass filter is a second-order active filter. The original transformer function is (4.8). To simplify the analysis, let $R_i \ll R_h$, (4.8) can be rewritten as (4.9). And the cutoff frequency can be calculated by (4.10). To filter the 100kHz switching frequency, the cutoff frequency is set to be 6.28kHz. The design parameters of the filter are shown in Table 4.3.

$$\frac{V_{filter}}{V_{amp}} = \frac{R_i + R_h}{R_i} \frac{\frac{1}{R_f R_g C_a C_b}}{s^2 + s\left(\frac{R_f + R_g}{R_f R_g C_b} - \frac{R_h}{R_i R_g C_a}\right) + \frac{1}{R_f R_g C_a C_b}} \tag{4.8}$$

$$\frac{V_{filter}}{V_{amp}} \approx \frac{\frac{1}{R_f R_g C_a C_b}}{s^2 + s\frac{R_f + R_g}{R_f R_g C_b} + \frac{1}{R_f R_g C_a C_b}} \tag{4.9}$$

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$$f_{cutoff,filter} \approx \frac{1}{2\pi\sqrt{R_f R_g C_a C_b}} \quad (4.10)$$

Table 4.3 Design parameters of Sallen-Key filter.

R_f	R_g	R_h	R_i	C_a	C_b
10kΩ	10kΩ	1Ω	1000Ω	0.1μF	0.1μF

The voltage protection circuit includes a first-order RC lowpass filter with 10kHz cutoff frequency and two voltage limit diodes. The diodes limit the maximum output voltage to 3.3V, which is the maximum input ADC voltage for DSP, and the minimum output voltage to 0V, which is the minimum input ADC voltage for DSP.

(b) Current sensing circuit.

The main purpose of current sensor circuits is to sense the LVS and HVS current from power boards. Current sensing circuits are composed by a hall sensor, a differential amplifier circuit, a Sallen-Key lowpass filter, and a voltage protection circuit. The topology of current sensing circuits is shown in Fig. 4.7. Each of the circuits is introduced in the following.

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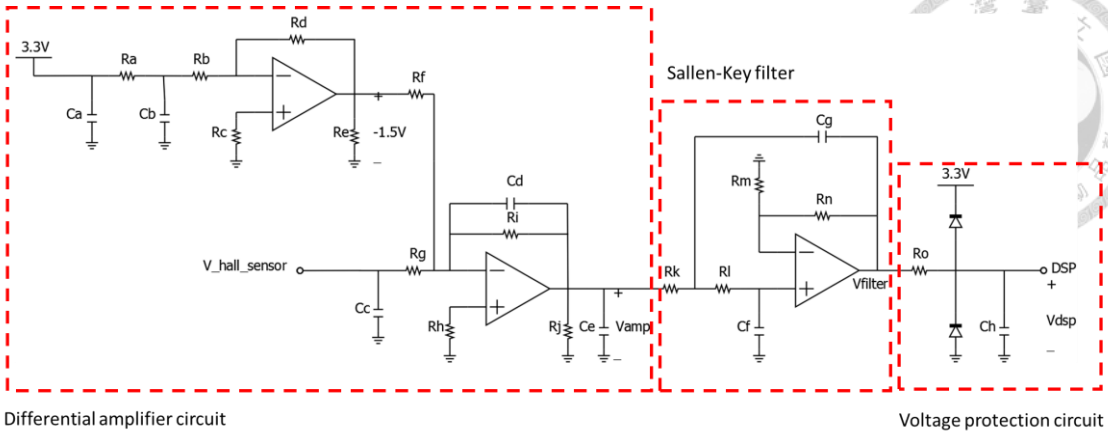

Fig. 4.7 Current sensing circuit.

HX-25P is a hall sensor from LEM Inc. The nominal RMS measuring current is ±25A and the maximum peak measuring current is ±75A, which is suitable for the LVS power board. The relationship of the output measuring voltage is (4.11).

$$V_{out}(in\ \ Volt) = I_{in}(in\ \ Ampere) * \frac{4}{75} \tag{4.11}$$

HX-05P is a hall sensor from LEM Inc., too. It has the ±5A nominal RMS current and the ±15A maximum peak current, which is fit the specification for the HVS power board. The relationship of the output measuring voltage is (4.12).

$$V_{out}(in\ \ Volt) = I_{in}(in\ \ Ampere) * \frac{4}{15} \tag{4.12}$$

The differential amplifier circuits consist of two operation amplifiers, TL032 and TL034. The hall sensor output voltage is amplified and level-shifted here. The voltage range is transferred from (-4V, 4V) into (0V, 3V), which is fit for the DSP. The level-

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shifted voltage, -1.5V, is generated by a front-end differential amplifier with the relationship in (4.13). In this case, R_a and R_d are set as 10kΩ and R_b is set as 12kΩ to generate the -1.5V level-shifted voltage, which is used to enhance the voltage level of the output voltage of hall sensor. The total relationship of the differential amplifier circuits is in (4.14).

$$V_{-1.5V} = -V_{3.3V} * \frac{R_d}{R_a + R_b} \tag{4.13}$$

$$V_{amp} = -V_{\_hall\_sensor} * \frac{R_i}{R_g} + 1.5V * \frac{R_f}{R_g} \tag{4.14}$$

The Sallen-Key filter in the current sensing circuits is the same as in the voltage sensing circuits. It is an active second-order low-pass filter. In this case, the cutoff frequency is set as 6.28kHz to filter the switching frequency 100kHz. The detail parameter design is in (4.8)~ (4.10) and Table 4.3.

The voltage protection circuit ensures the maximum and minimum input voltage for the DSP. It contains two diodes and a low-pass filter to protect the DSP.

(c) Microcontroller.

In the control board, DSP TMS320F28335 from TEXAS INSTRUMENTS is chosen to be the microcontroller in the experiment. The features and specifications are listed below:

(1) 150MHz System Clock.

(2) 32-bit CPU with high performance.

(3) 3.3V I/O ports.

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(4) Enhanced-PWM (EPWM) Modules with 18 channels.

(5) 12-bit Analog-to Digital-Conversion (ADC) with 16 channels.

(6) Code Composer Studio IDE development supported.

(7) 256K*16 Flash.

The 150MHz system clock provides enough resolution in the experiment with 100kHz switching frequency. The high performance CPU makes the real-time closed-loop control possible. 3.3V I/O ports are fit for the driver IC UCC21530. Many useful blocks in EPWM modules, such as Action Qualifier (AQ) and Dead Band (DB) blocks, play crucial roles in the setting of phase-shifted. The ADC modules in TMS320F28335 realize ADC interrupts. The Code Composer Studio (CCS) IDE make the DSP easier to use. In conclusion, DSP TMS320F28335 is very suitable for this experiment.

4.2 DSP Program

In this section, the DSP program for the AC-CFDAB maximum efficiency MEPT control strategy is introduced. The total programs contain a main program and interrupt functions. The detail introduction and control flowcharts are introduced in the following.

4.2.1 Main Program

The control flowchart for the main program includes initialization functions and protection functions. The details of the control flowchart are illustrated in Fig. 4.8.

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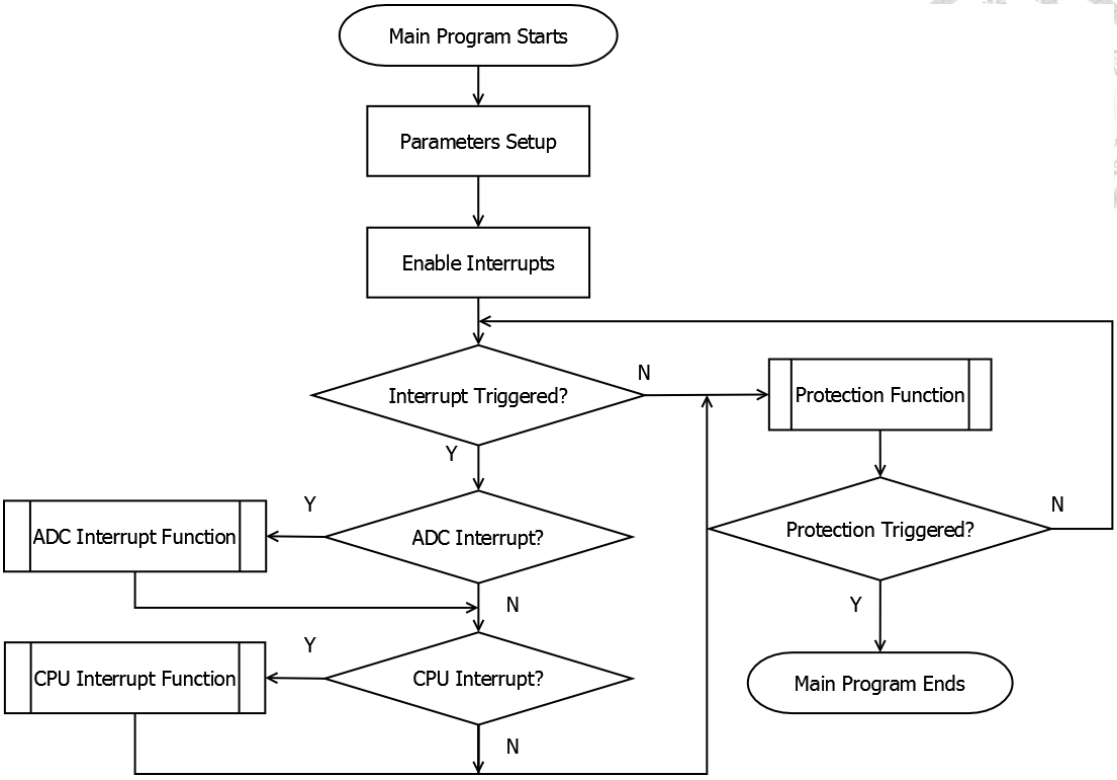

Fig. 4.8 Control flowchart for main program.

As the DSP is powered, some crucial system variables and control parameters are initialized. That is, GPIO modules, EPWM modules and ADC modules are completely set in this time. Some GPIO ports are set to enable EPWM output. EPWM modules are set to be 100kHz and enable DB functions. ADC modules are set to be 100kHz and enable ADC interrupt. Also, control parameters, such as PID control parameters, are set in this time.

After well initializing all the settings, the interrupt setting is initialized. In this case, ADC interrupt function and CPU interrupt function are initialized. The ADC interrupt is triggered by EPWM6 module, while the CPU interrupt frequency is set to be 100kHz.

After enabling the interrupt, Peripheral Interrupt Expansion (PIE) block is applied to manage all the interrupt requests. According to the PIE Vector Table, the priority of the ADC interrupt is higher than the CPU interrupt. That is, if PIE block receives both the

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ADC and CPU interrupt requests, ADC interrupt is enabled first.

The protection function monitors voltages and currents from LVS and HVS. The details are shown in Fig. 4.9. If any of the terms exceeds the limit, the Sys_Fault_code is set to be higher than 0, then the DSP output signals are shut down to protect the circuit.

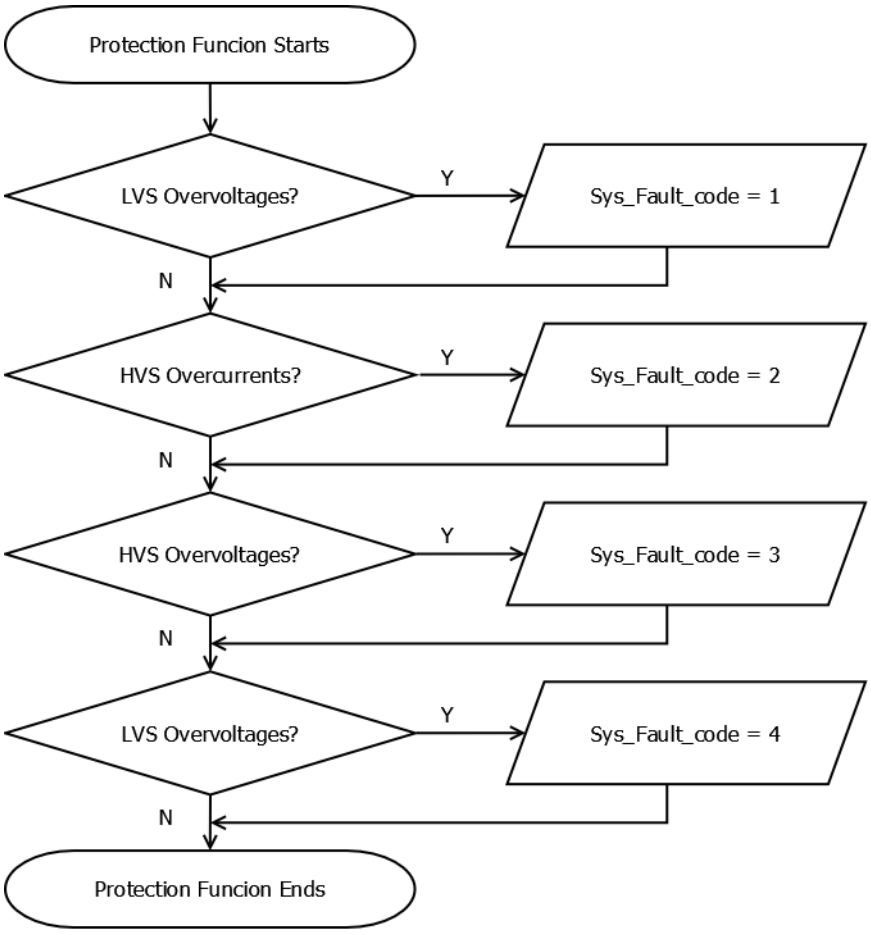

Fig. 4.9 Control flowchart for protection function.

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4.2.2 Interrupt Functions

The interrupt functions in this control strategy contain ADC interrupt function and CPU interrupt function. Both of them are introduced in the following.

(a) ADC Interrupt Function

The control flowchart for ADC interrupt function is shown in Fig. 4.10. ADC interrupt function is triggered by EPWM6 module, whose frequency is same as the switching frequency, 100kHz.

In ADC interrupt function, voltages and currents from each voltage side are read by the ADC module. ADC module provides 12-bit sample-and-hold channels, that is, input voltage ranged from 0V to 3V is converted into the digital value ranged from 0 to 4096 in DSP. With proper regulation, corrected voltages and currents can be derived.

With the read voltage and current values, the efficiency of the AC-CFDAB can be calculated. The efficiency is used in the efficiency control loop.

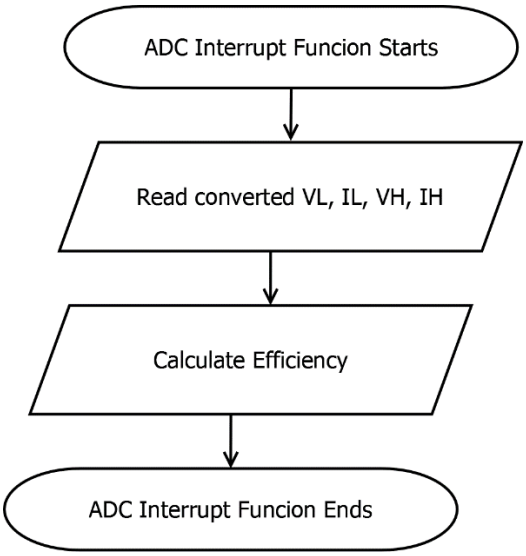

Fig. 4.10 Control flowchart for ADC interrupt function.

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(b) CPU Interrupt Function

The control flowchart for the CPU interrupt function is shown in Fig. 4.11. CPU interrupt is triggered by the system clock, timer_0 module, with 100kHz triggered frequency.

In the CPU interrupt function, four GPIO values, GPIO16, GPIO18, GPIO20 and GPIO22, are read in the beginning. The four GPIO values are controlled by the DIP switches in the control board. Each of them implies different operation. GPIO16 value controls the EPWM output. GPIO18 value decides whether operating in buck operation or not, which is switched in the MEPT transient experiment. GPIO20 value decides whether the I_L is controlled or not. If I_L is controlled, the value of I_L is read and PI control is used to decide the φ_{HL} value. While φ_{HL} is derived by (2.35) if I_L is in open-loop control. GPIO22 value decides whether the efficiency control loop is set or not. If the efficiency control is set to be open, D_2 is set to be 0.47 all the time. While perturb and observe method is used in the efficiency control loop.

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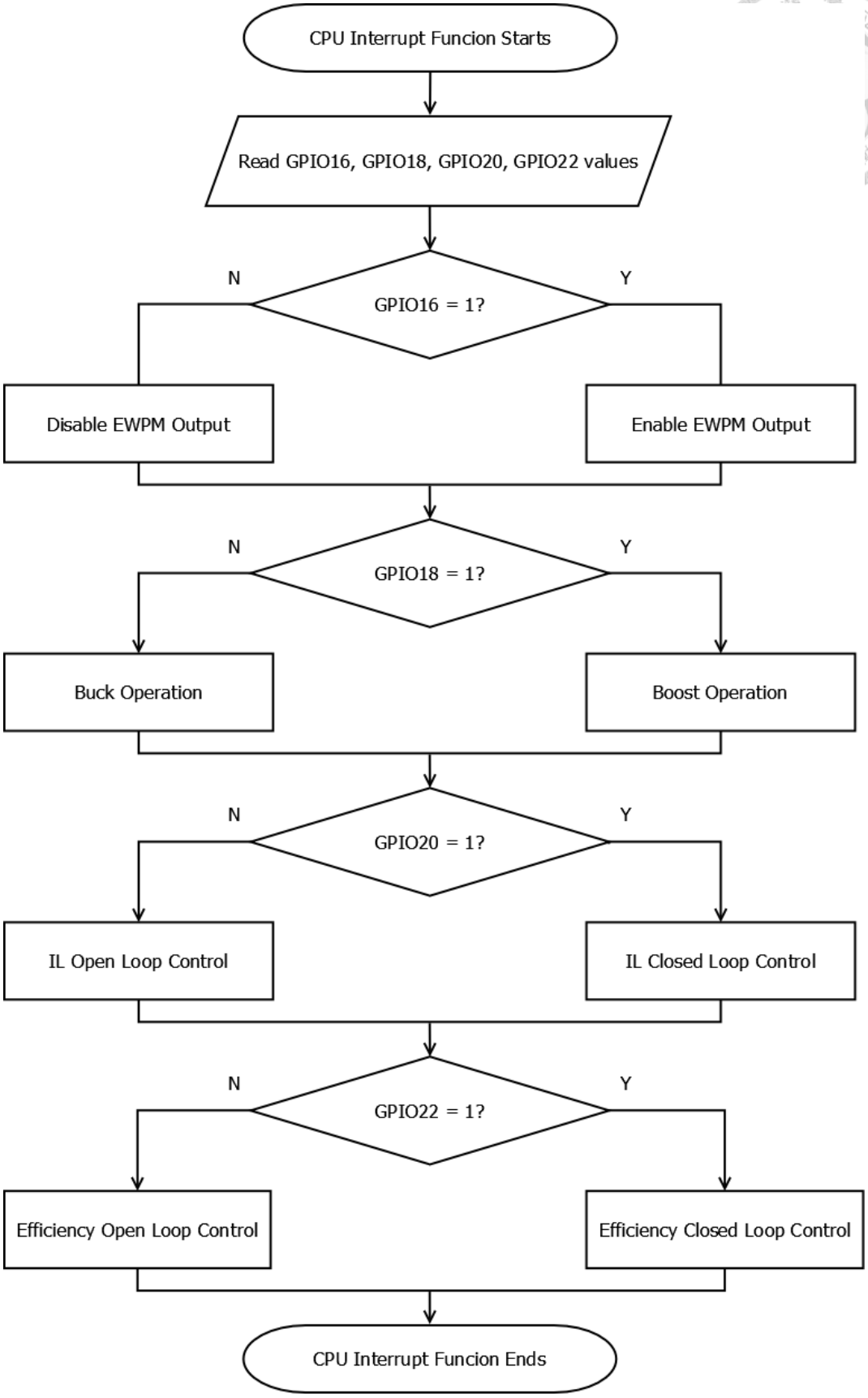

Fig. 4.11 Control flowchart for CPU interrupt function.

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Chapter 5 Simulation and Experimental Verification

In previous chapters, MDPSM and MEPT are proposed. In this chapter, some simulations and experiments are done to verify the feasibility. The detailed test environment is introduced in section 5.1, and each test condition is verified individually in section 5.2 to section 5.4.

5.1 Test Environment

In this section, the test condition and the verification terms are introduced.

All simulations are done by Matlab/Simulink or Simplis, and the test environment of all experiments is shown in Fig. 5.1. DC Power Supply EA-PSI 9500-30 form the Elektro-Automatik (EA) is chosen to be the LVS power source due to its 400V/30A output rating, while Programmable DC Source 62100H-600S from Chroma is chosen to be the HVS power source due to its 600V/17A output rating. The hardware circuit is introduced in the chapter 4 and the photo is shown in Fig. 5.2.

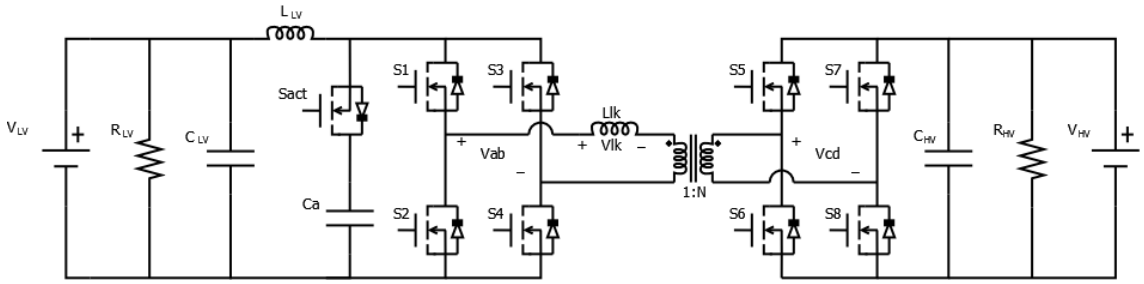

Fig. 5.1 Test environment of the experiment.

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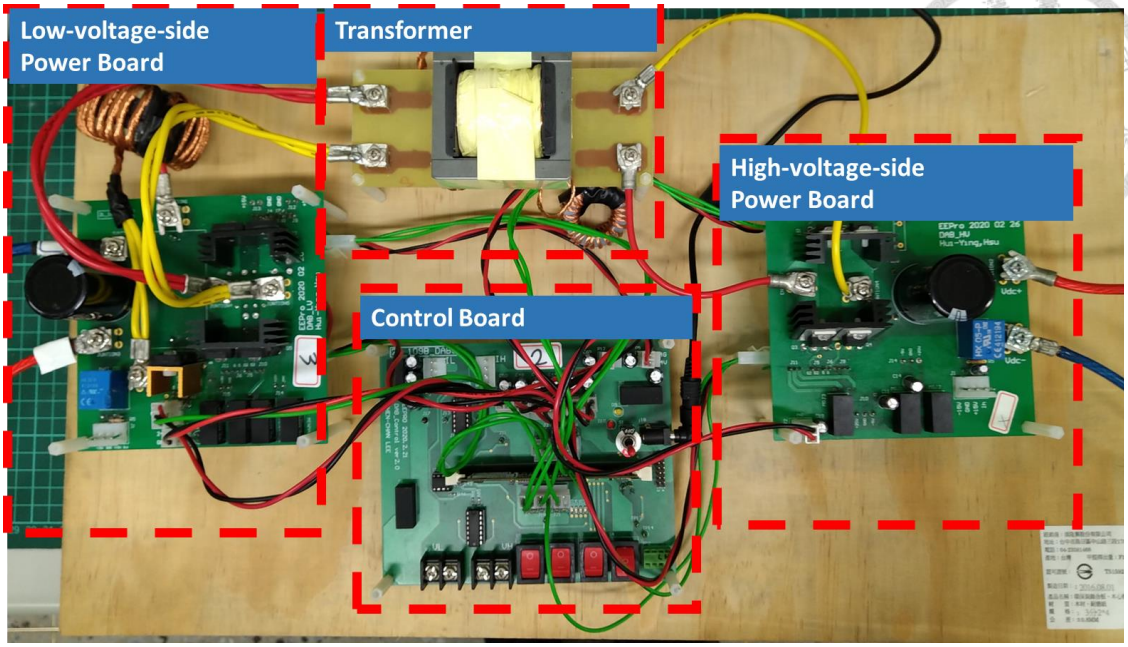

Fig. 5.2 Photo of the hardware circuit.

To verify the previous analysis, full load case, middle load case, and light load case are set. The full load case is set according to the maximum rated transfer power, ±720W. In the full load case, I_L is equal to ±15A. The middle load case is set as the transfer power is ±480W, that is, ±10A for I_L. The light load case is chosen to be ±240W with ±5A for I_L. In the following verification, the above three load cases are all set in the three verification terms.

With the designed power rating and system parameters, some modulation parameters can be set by previous equations. In the following part, D_1 is equal to 0.32, $D_{2,open}$ is equal to 0.47, D_{td1} and D_{td2} are both 0.02, and $D_{d,lead}$ has the same value, 0.03, as $D_{d,lag}$.

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5.2 Steady-state Waveforms

In Chapter 2, the theoretical analysis show that MDPSM can achieve bidirectional operation and ZVS for proper deadtime. These two features are first verified. The simulations and experiments of each load case are done in this section.

In the steady-state waveforms of MDPSM, φ_{HL} can be observed by V_{ab} and V_{cd} with the unit of ratio, power transmission can be recognized by I_L, and the circuit operation can be corresponded by I_{Lk}. All of the six load cases are done in this section. And the error is defined by (5.1).

$$Error = \left|\frac{Theoritical\ \ value - Measure\ \ value}{Measure\ \ value}\right| * 100\% \tag{5.1}$$

In the ZVS waveforms of MDPSM, the V_{gs} and V_{ds} values of each switch are measured. Because the symmetry operation of positive-half-cycle and negative-half-cycle, the simulations only show half of the switches. The ZVS waveforms of each switch are shown in the experiment results.

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(a) -240W case

Fig. 5.3 shows the steady-state simulation waveform of -240W case. The simulation is done by Simplis and all of the system parameters are same as the hardware circuit. The steady-state result of the hardware experiment is shown in Fig. 5.4.

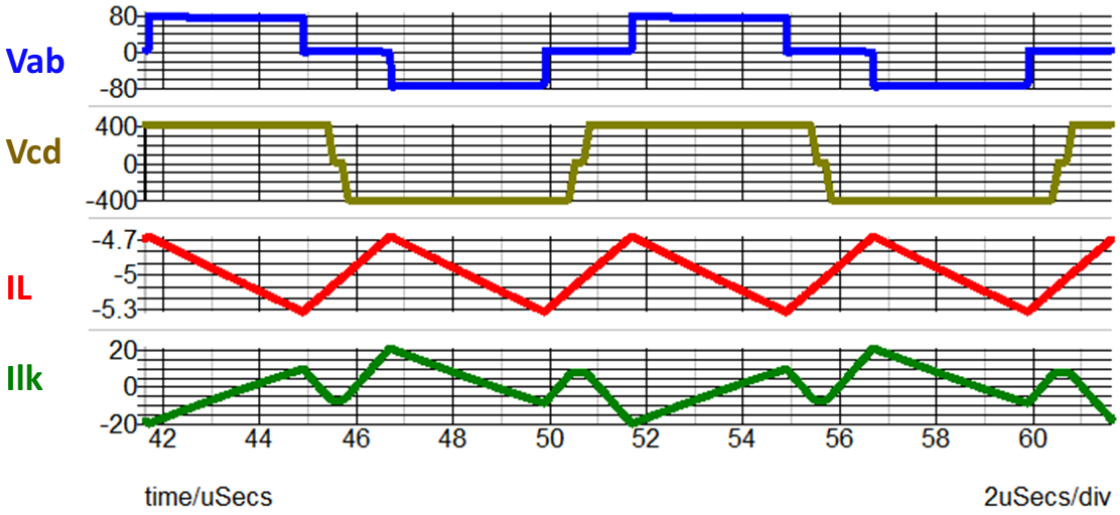


Fig. 5.3 Simulation result of -240W steady-state waveform.

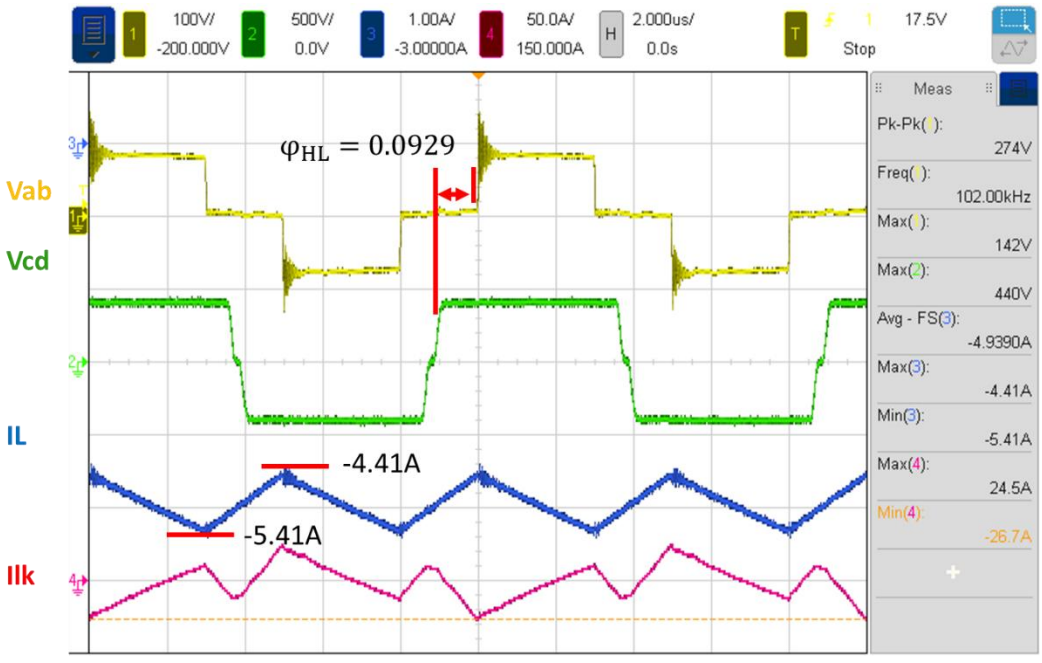


Fig. 5.4 Experiment result of -240W steady-state waveform.

doi:10.6342/NTU202202177

The key value of steady-state results are listed in Table 5.1. Theoretical equation of I_L is (2.32), and the theoretical value of φ_{HL} can be derived by (2.35). The errors of I_L from simulation and experiment are both less than 1.5% and the errors of φ_{HL} are both less than 1.5%, which shows that the theoretical equation is very closed to simulation and experiment results in -240W case.

Table 5.1 Comparing steady-state results in -240W case.

	$I_L(A)$	$Error_{IL}$	φ_{HL}	$Error_{\varphi_{HL}}$
Theoretical equation	-5		0.0921	
Simulation result	-5.01	0.2%	0.0932	1.18%
Experiment result	-4.93	1.42%	0.0929	0.86%

To verify the feasibility of ZVS turn-on, deadtime of each switch are all set properly by the previous ZVS condition equations. The feasibility of ZVS is first verified by simulation in Fig. 5.5. The active clamp switch, S_{act}, one LVS switch, S_1, one HVS leading-leg switch, S_5, and one HVS lagging-leg switch, S_8, are shown in simulation. It can be observed that all of the switches achieve ZVS in simulation. To further verify the feasibility of ZVS, experiment results are shown in Fig. 5.6 and Fig. 5.7. It is clear by the results of experiment that all of the switches operate in ZVS. Note that the turn-off spikes in S_{act} and S_{LV} are caused by the oscillator between $C_{ds,LV}$ and active clamp ESL, which is not simulated in Simplis.

doi:10.6342/NTU202202177

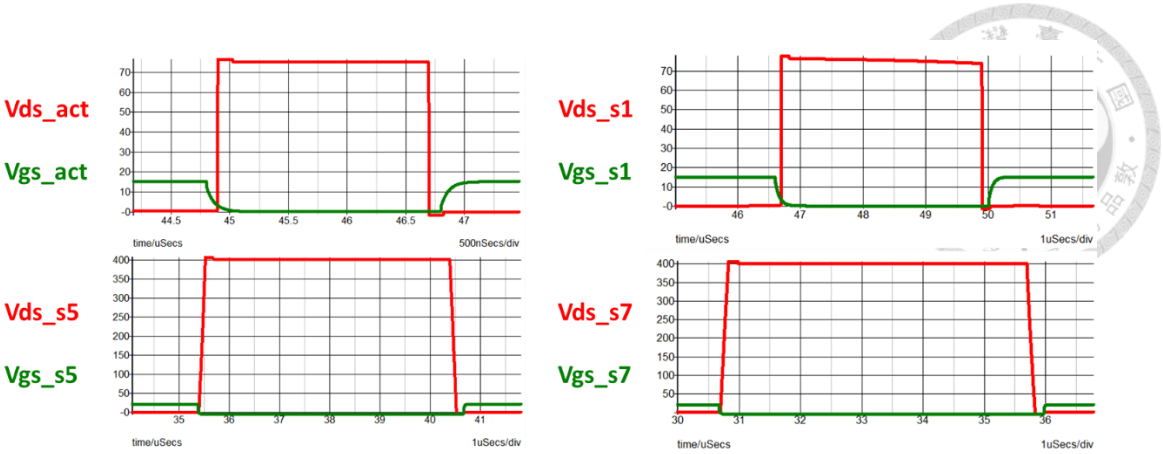


Fig. 5.5 Simulation result of -240W ZVS waveform.

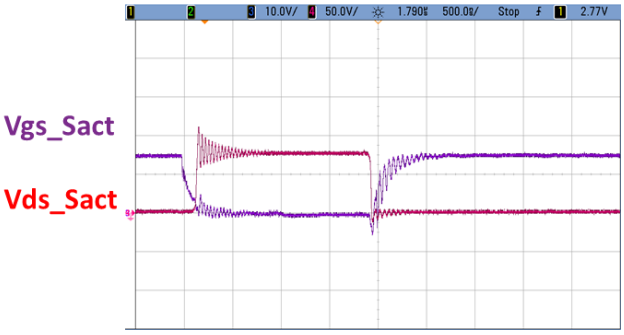


Fig. 5.6 Experiment result of -240W Sact ZVS waveform.

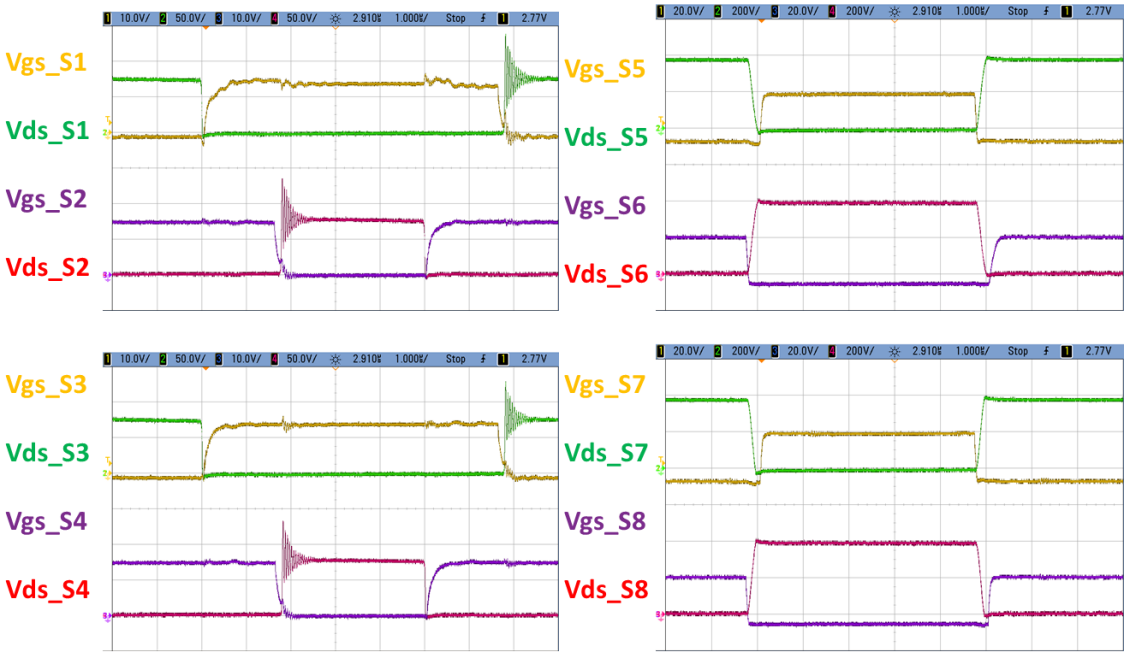


Fig. 5.7 Experiment result of -240W SLV and SHV ZVS waveform.

doi:10.6342/NTU202202177

(b) -480W case

Fig. 5.8 shows the steady-state simulation waveform of -480W case. The simulation is done by Simplis and all of the system parameters are same as the hardware circuit. The steady-state result of the hardware experiment is shown in Fig. 5.9.

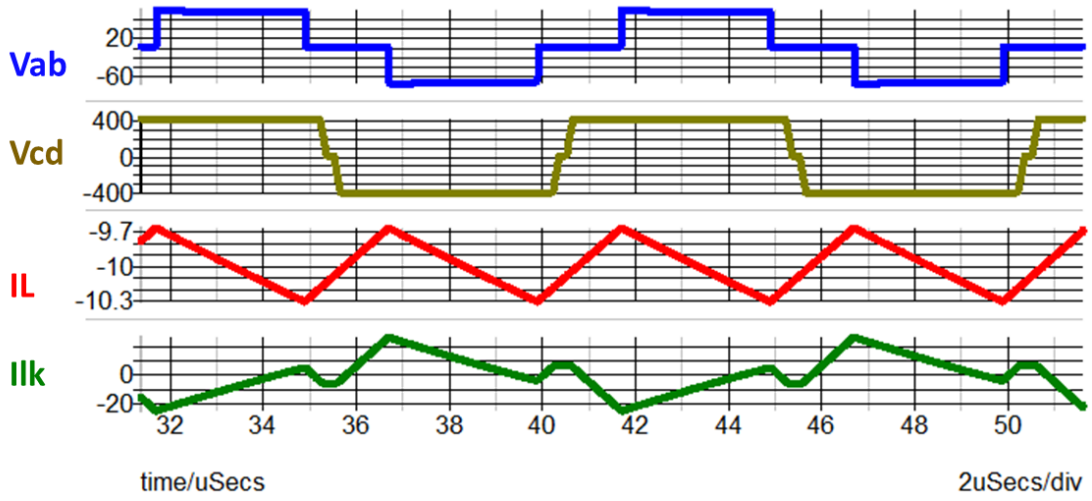


Fig. 5.8 Simulation result of -480W steady-state waveform.

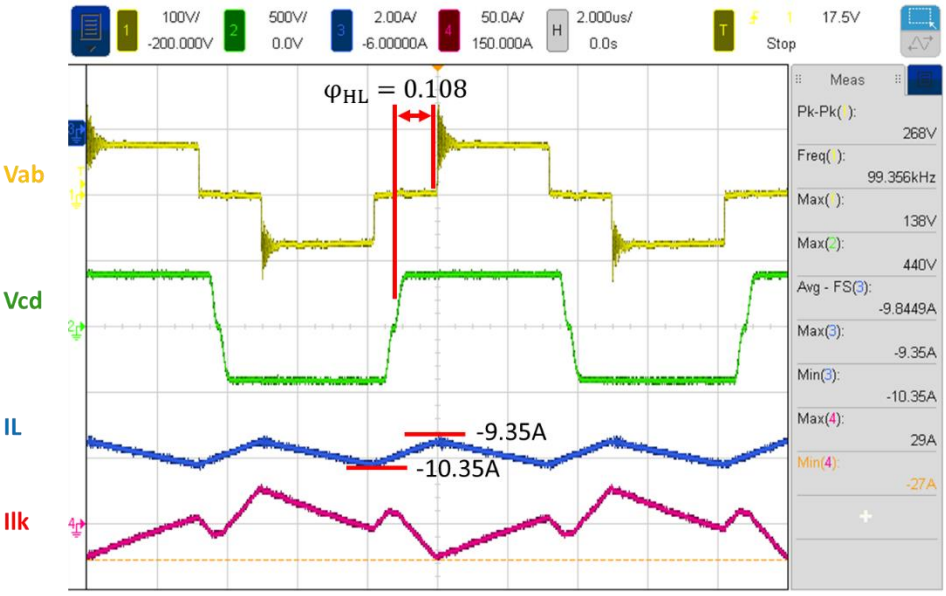


Fig. 5.9 Experiment result of -480W steady-state waveform.

doi:10.6342/NTU202202177

The key waveform of steady-state results are listed in Table 5.2. Theoretical equation of I_L is (2.32), and the theoretical value of φ_{HL} can be derived by (2.35). The errors of I_L from simulation and experiment are both less than 2% and the errors of φ_{HL} are both less than 2%, which shows that the theoretical equation is very closed to simulation and experiment results in -480W case.

Table 5.2 Comparing steady-state results in -480W case.

	I_L(A)	$Error_{IL}$	φ_{HL}	$Error_{\varphi_{HL}}$
Theoretical equation	-10		0.1091	
Simulation result	-9.99	0.1%	0.1108	1.53%
Experiment result	-9.84	1.62%	0.1080	1.02%

To verify the feasibility of ZVS turn-on, deadtime of each switch are all set properly by the previous ZVS condition equations. The feasibility of ZVS is first verified by simulation in Fig. 5.10. The active clamp switch, S_{act}, one LVS switch, S_1, one HVS leading-leg switch, S_5, and one HVS lagging-leg switch, S_8, are shown in simulation. It can be observed that all of the switches achieve ZVS in simulation. To further verify the feasibility of ZVS, experiment results are shown in Fig. 5.11 and Fig. 5.12. It is clear by the results of experiment that all switches operate in ZVS. Note that the turn-off spikes in S_{act} and S_{LV} are caused by the oscillator between $C_{ds,LV}$ and active clamp ESL, which is not simulated in Simplis.

doi:10.6342/NTU202202177

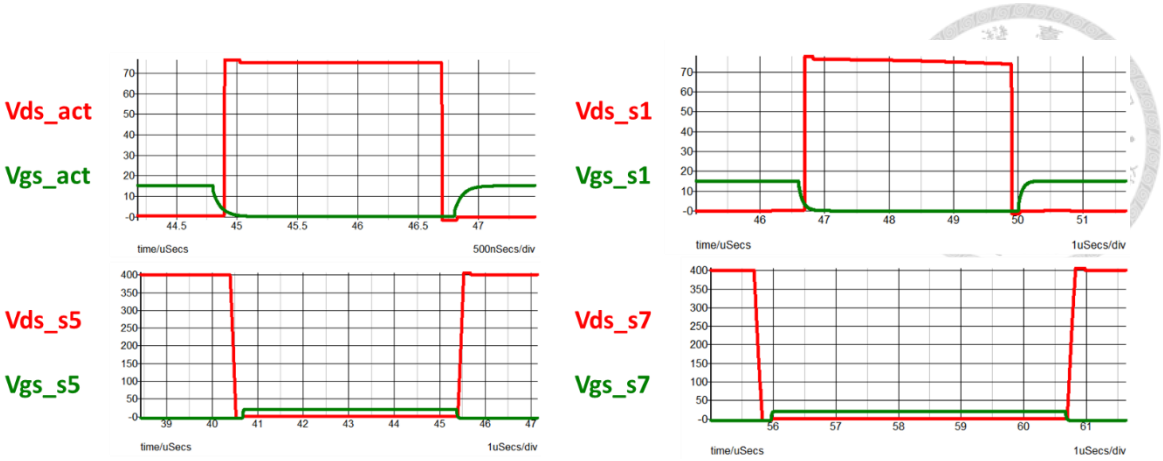


Fig. 5.10 Simulation result of -480W ZVS waveform.

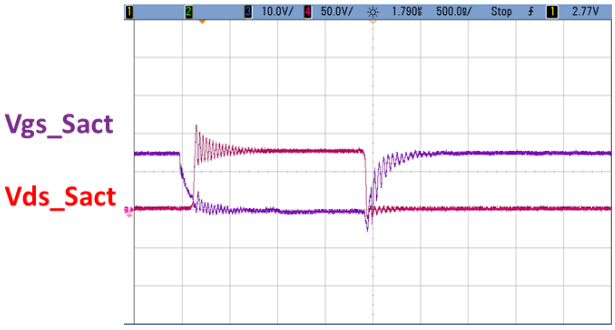


Fig. 5.11 Experiment result of -480W Sact ZVS waveform.

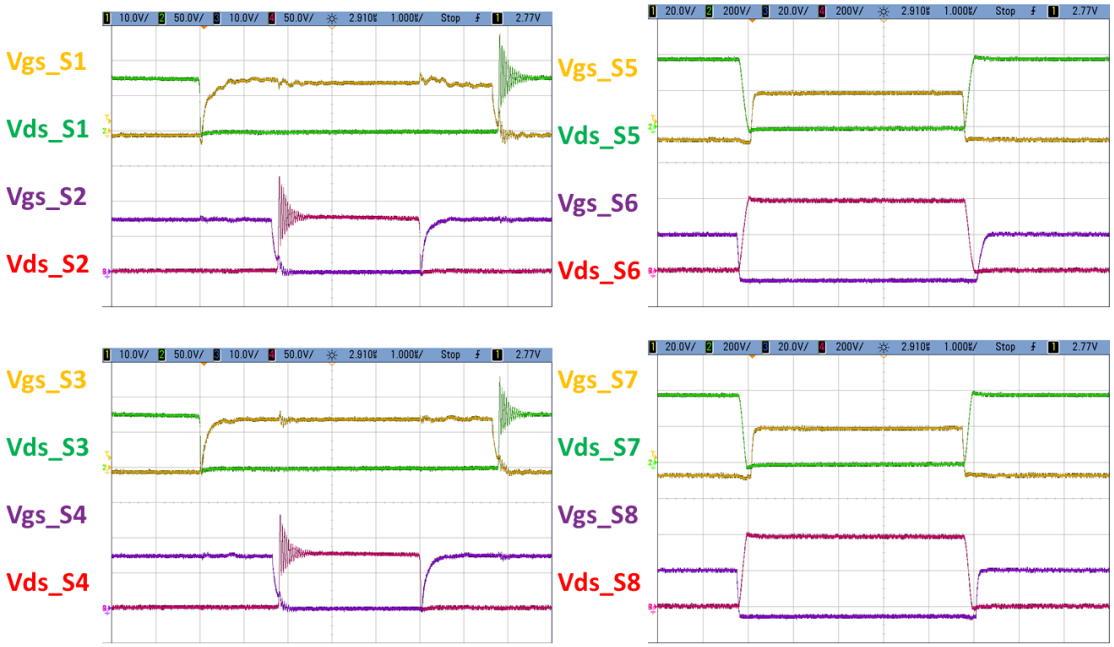


Fig. 5.12 Experiment result of -480W SLV and SHV ZVS waveform.

doi:10.6342/NTU202202177

(c) -720W case

Fig. 5.13 shows the steady-state simulation waveform of -720W case. The simulation is done by Simplis and all of the system parameters are same as the hardware circuit. The steady-state result of the hardware experiment is shown in Fig. 5.14.

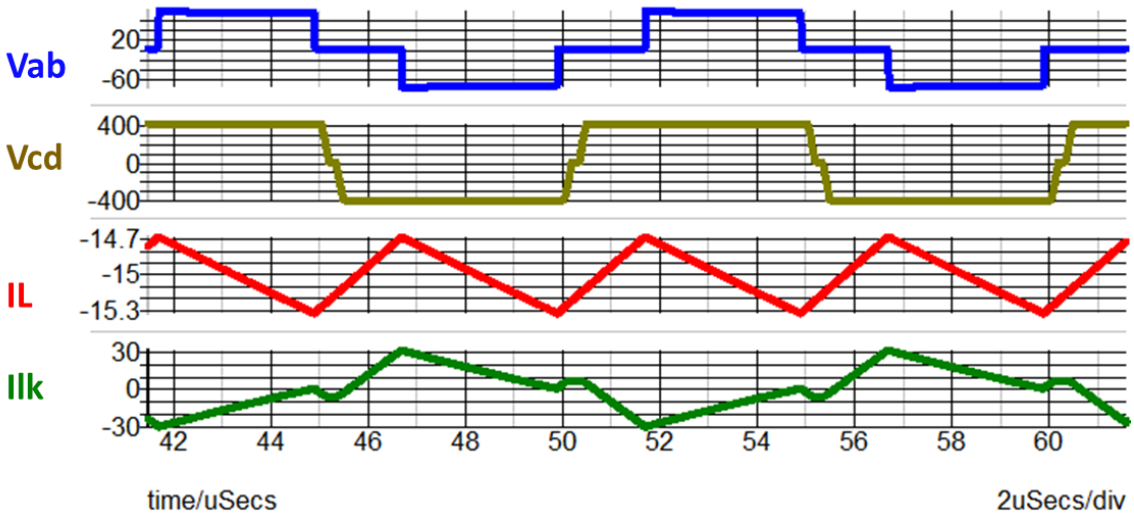


Fig. 5.13 Simulation result of -720W steady-state waveform.

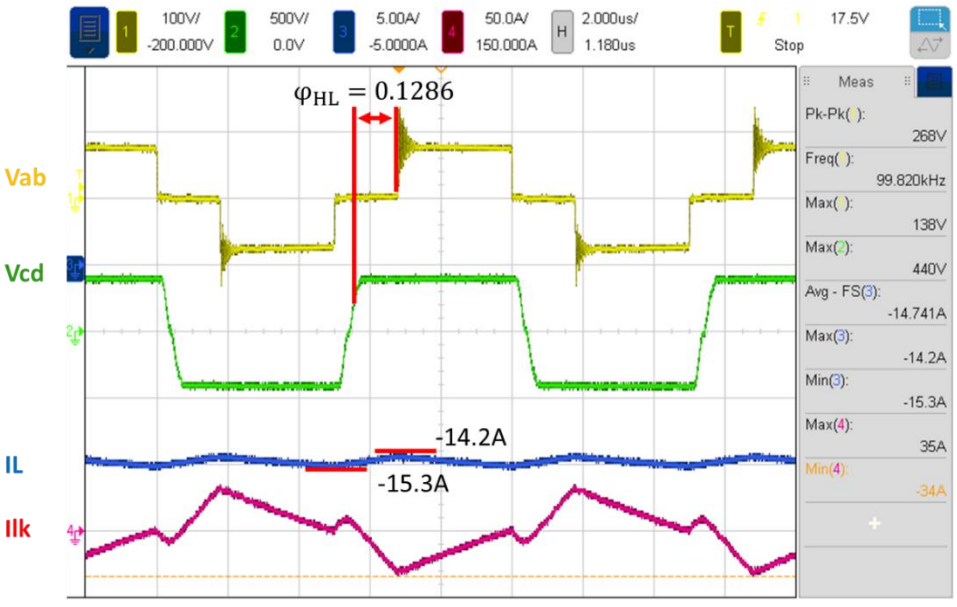


Fig. 5.14 Experiment result of -720W steady-state waveform.

doi:10.6342/NTU202202177

Comparing steady-state results are listed in Table 5.3. Theoretical equation of I_L is (2.32), and the theoretical value of φ_{HL} can be derived by (2.35). The errors of I_L from simulation and experiment are both less than 2% and the errors of φ_{HL} are both less than 2%, which shows that the theoretical equation is very closed to simulation and experiment results in -720W case.

Table 5.3 Comparing steady-state results in -720W case.

	I_L(A)	$Error_{IL}$	φ_{HL}	$Error_{\varphi_{HL}}$
Theoretical equation	-15		0.1262	
Simulation result	-15.02	0.13%	0.1286	1.87%
Experiment result	-14.74	1.76%	0.1286	1.87%

To verify the feasibility of ZVS turn-on, deadtime of each switch are all set properly by the previous ZVS condition equations. The feasibility of ZVS is first verified by simulation in Fig. 5.15. The active clamp switch, S_{act}, one LVS switch, S_1, one HVS leading-leg switch, S_5, and one HVS lagging-leg switch, S_8, are shown in simulation. It can be observed that all of the switches achieve ZVS in simulation. To further verify the feasibility of ZVS, experiment results are shown in Fig. 5.16 and Fig. It is clear by the results of experiment that all of the switches operate in ZVS. Note that the turn-off spikes in S_{act} and S_{LV} are caused by the oscillator between $C_{ds,LV}$ and active clamp ESL, which is not simulated in Simplis.

doi:10.6342/NTU202202177

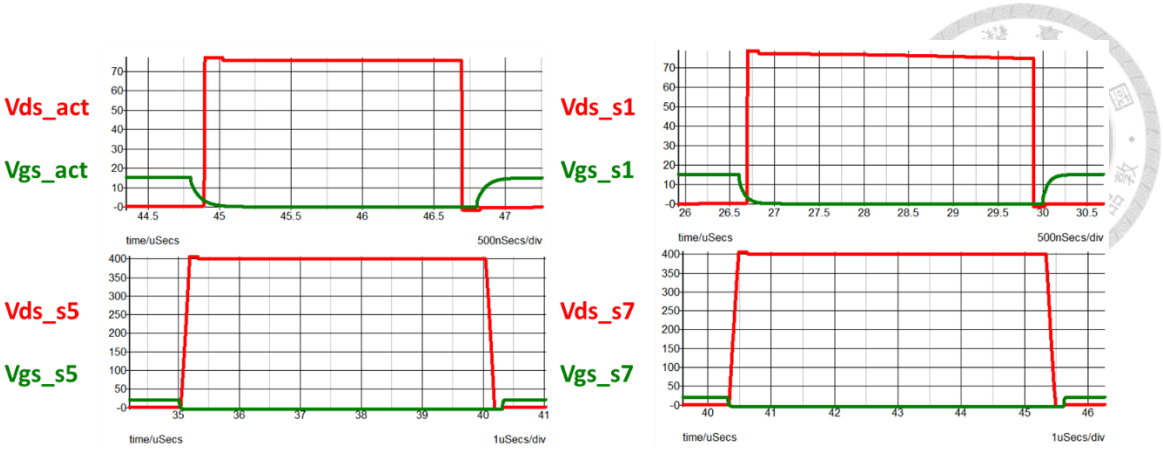


Fig. 5.15 Simulation result of -720W ZVS waveform.

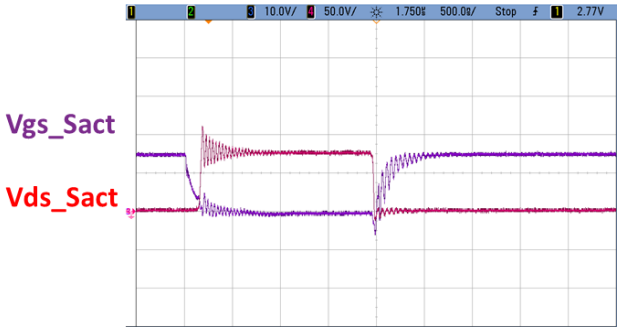


Fig. 5.16 Experiment result of -720W Sact ZVS waveform.

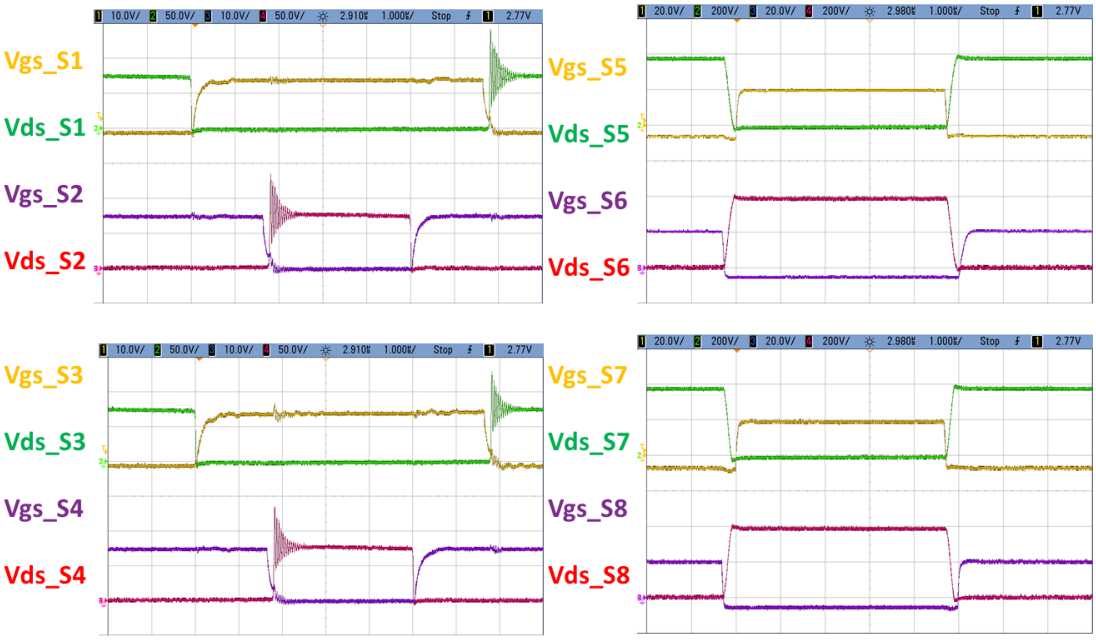


Fig. 5.17 Experiment result of -720W SLV and SHV ZVS waveform.

doi:10.6342/NTU202202177

(d) 240W case

Fig. 5.18 shows the steady-state simulation waveform of 240W case. The simulation is done by Simplis and all of the system parameters are same as the hardware circuit. The steady-state result of the hardware experiment is shown in Fig. 5.19.

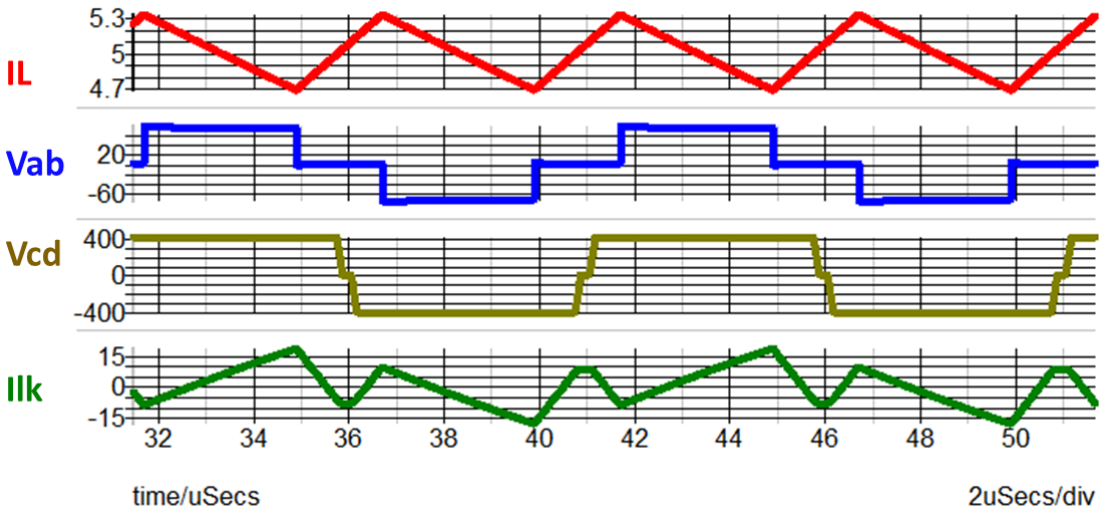


Fig. 5.18 Simulation result of 240W steady-state waveform.

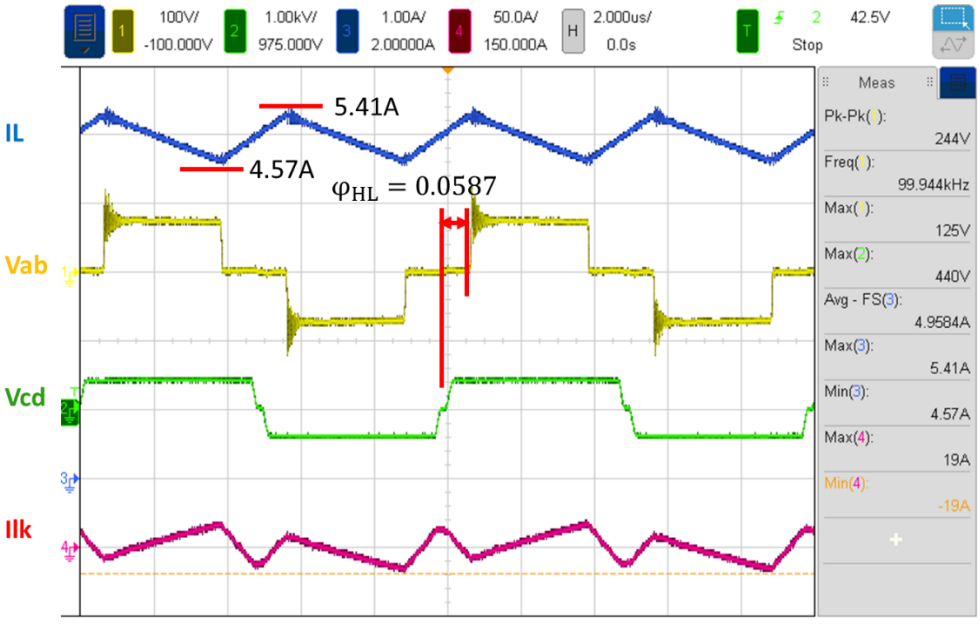
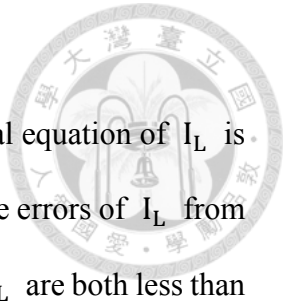


Fig. 5.19 Experiment result of 240W steady-state waveform.

doi:10.6342/NTU202202177



Comparing steady-state results are listed in Table 5.4. Theoretical equation of I_L is (2.32), and the theoretical value of φ_{HL} can be derived by (2.35). The errors of I_L from simulation and experiment are both less than 1% and the errors of φ_{HL} are both less than 1.5%, which shows that the theoretical equation is very closed to simulation and experiment results in 240W case.

Table 5.4 Comparing steady-state results in 240W case.

	I_L(A)	$Error_{IL}$	φ_{HL}	$Error_{\varphi_{HL}}$
Theoretical equation	5		0.0579	
Simulation result	5.01	0.20%	0.0582	0.52%
Experiment result	4.96	0.81%	0.0587	1.36%

To verify the feasibility of ZVS turn-on, deadtime of each switch are all set properly by the previous ZVS condition equations. The feasibility of ZVS is first verified by simulation in Fig. 5.20. The active clamp switch, S_{act}, one LVS switch, S_1, one HVS leading-leg switch, S_5, and one HVS lagging-leg switch, S_8, are shown in simulation. It can be observed that all of the switches achieve ZVS in simulation. To further verify the feasibility of ZVS, experiment results are shown in Fig. 5.21 and Fig. 5.22. It is clear by the results of experiment that all of the switches operate in ZVS. Note that the turn-off spikes in S_{act} and S_{LV} are caused by the oscillator between $C_{ds,LV}$ and active clamp ESL, which is not simulated in Simplis.

doi:10.6342/NTU202202177

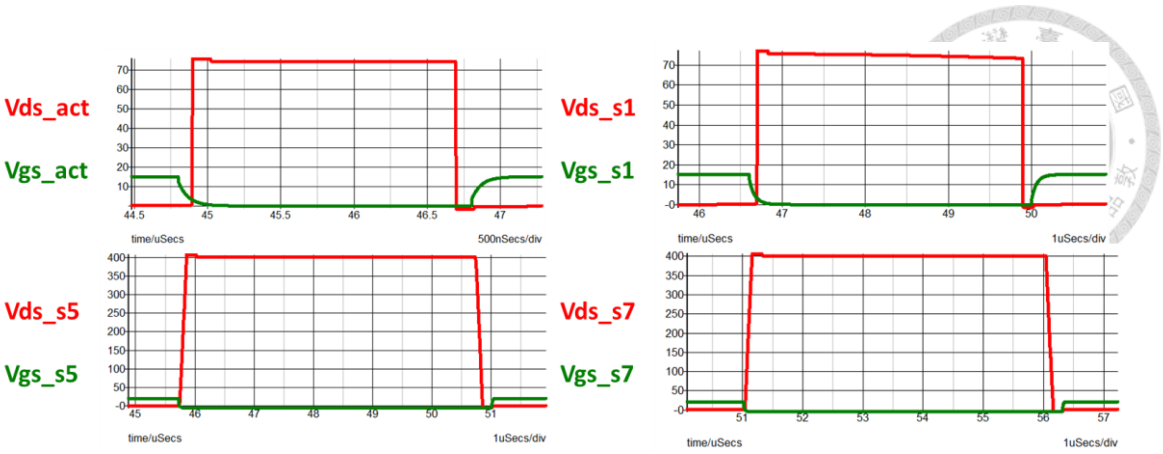


Fig. 5.20 Simulation result of 240W ZVS waveform.

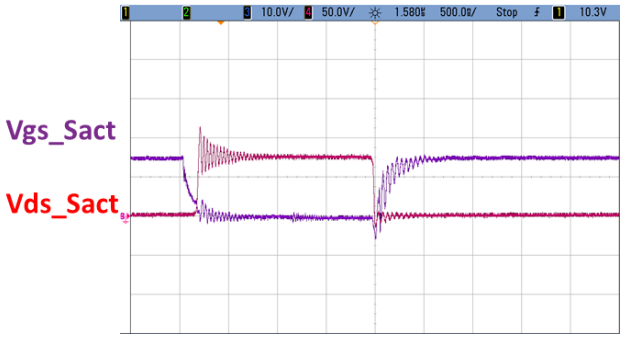


Fig. 5.21 Experiment result of 240W Sact ZVS waveform.

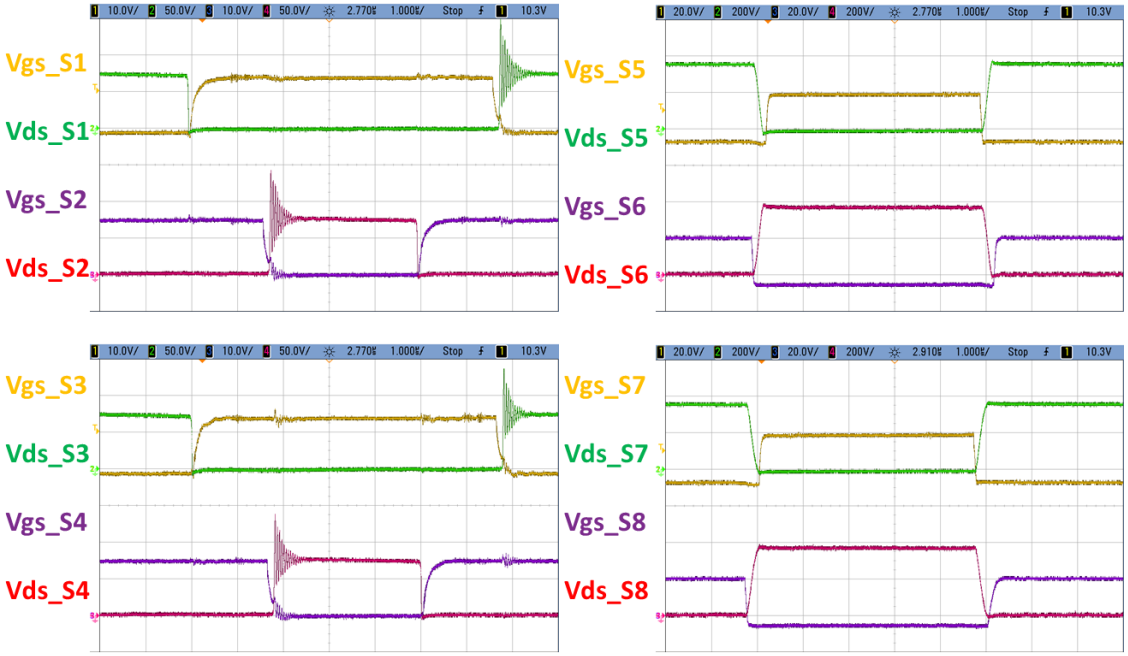


Fig. 5.22 Experiment result of 240W SLV and SHV ZVS waveform.

doi:10.6342/NTU202202177

(e) 480W case

Fig. 5.23 shows the steady-state simulation waveform of 480W case. The simulation is done by Simplis and all of the system parameters are same as the hardware circuit. The steady-state result of the hardware experiment is shown in Fig. 5.24.

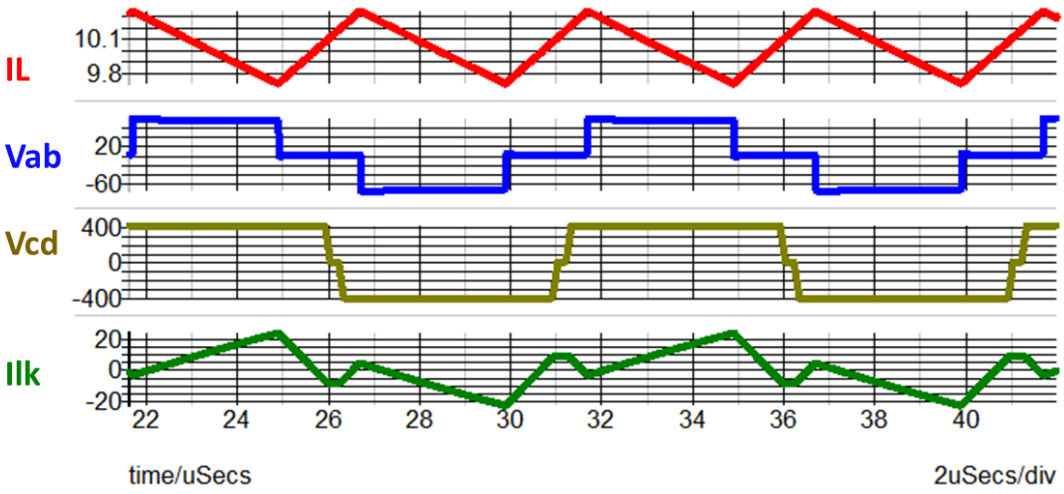


Fig. 5.23 Simulation result of 480W steady-state waveform.

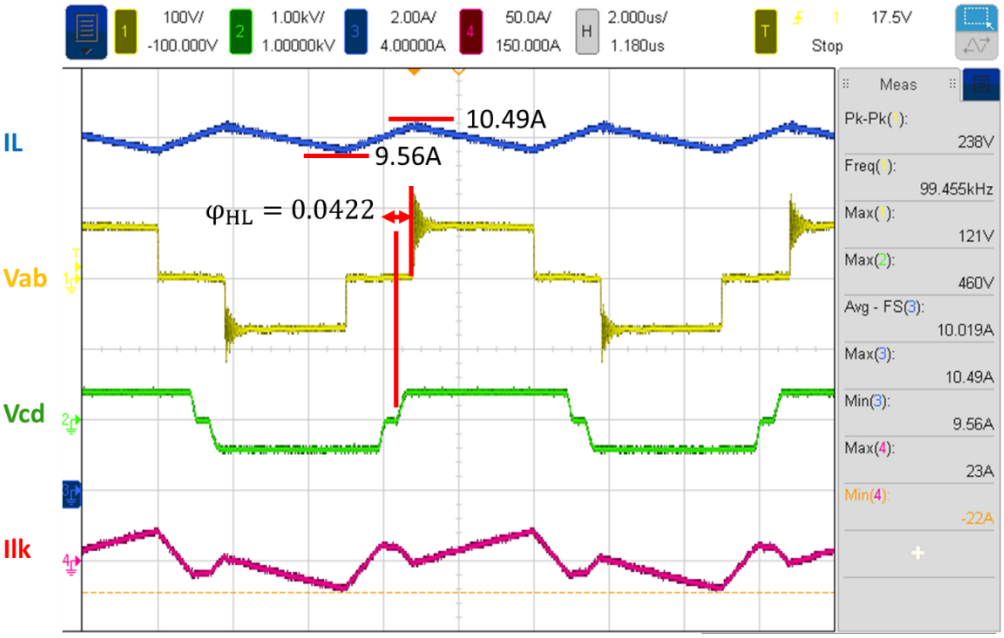


Fig. 5.24 Experiment result of 480W steady-state waveform.

doi:10.6342/NTU202202177

Comparing steady-state results are listed in Table 5.5. Theoretical equation of I_L is (2.32), and the theoretical value of φ_{HL} can be derived by (2.35). The errors of I_L from simulation and experiment are both less than 0.5% and the errors of φ_{HL} are both less than 3.5%, which shows that the theoretical equation is very closed to simulation and experiment results in 480W case.

Table 5.5 Comparing steady-state results in 480W case.

	I_L(A)	$Error_{IL}$	φ_{HL}	$Error_{\varphi_{HL}}$
Theoretical equation	10		0.0409	
Simulation result	10.02	0.20%	0.0408	0.25%
Experiment result	10.02	0.20%	0.0422	3.08%

To verify the feasibility of ZVS turn-on, deadtime of each switch are all set properly by the previous ZVS condition equations. The feasibility of ZVS is first verified by simulation in Fig. 5.25. The active clamp switch, S_{act}, one LVS switch, S_1, one HVS leading-leg switch, S_5, and one HVS lagging-leg switch, S_8, are shown in simulation. It can be observed that all of the switches achieve ZVS in simulation. To further verify the feasibility of ZVS, experiment results are shown in Fig. 5.26 and Fig. 5.27. It is clear by the results of experiment that all of the switches operate in ZVS. Note that the turn-off spikes in S_{act} and S_{LV} are caused by the oscillator between $C_{ds,LV}$ and active clamp ESL, which is not simulated in Simplis.

doi:10.6342/NTU202202177

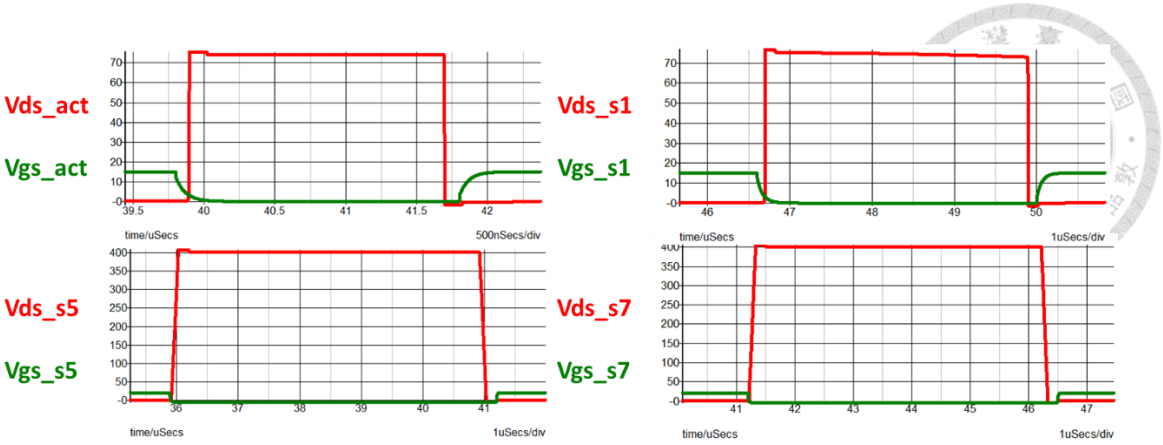


Fig. 5.25 Simulation result of 480W ZVS waveform.

Fig. 5.26 Experiment result of 480W Sact ZVS waveform.

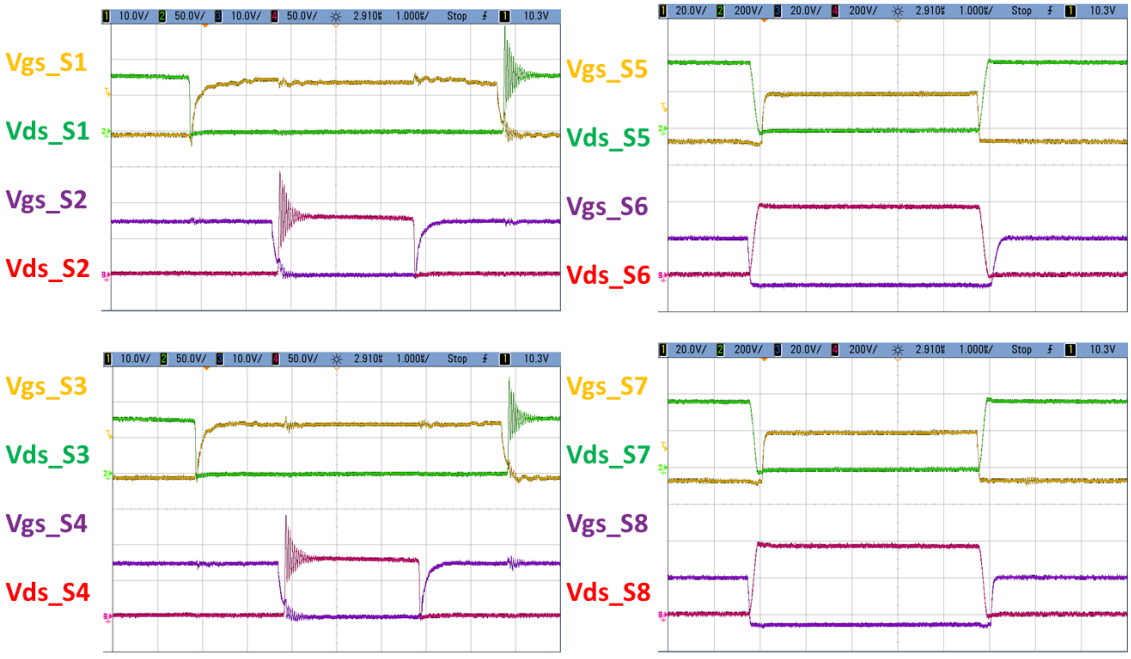


Fig. 5.27 Experiment result of 480W SLV and SHV ZVS waveform.

doi:10.6342/NTU202202177

(f) 720W case

Fig. 5.28 shows the steady-state simulation waveform of 720W case. The simulation is done by Simplis and all of the system parameters are same as the hardware circuit. The steady-state result of the hardware experiment is shown in Fig. 5.29.

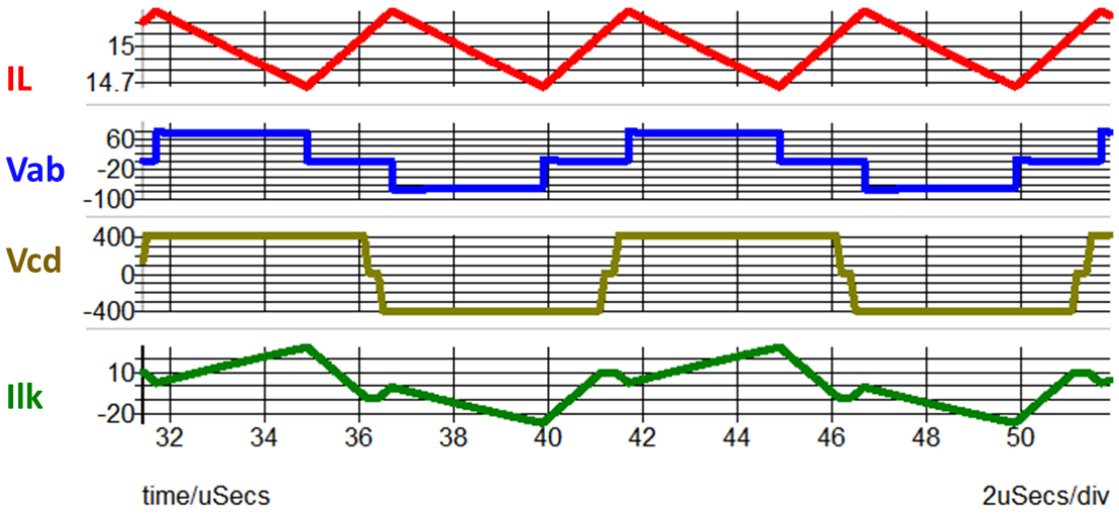


Fig. 5.28 Simulation result of 720W steady-state waveform.

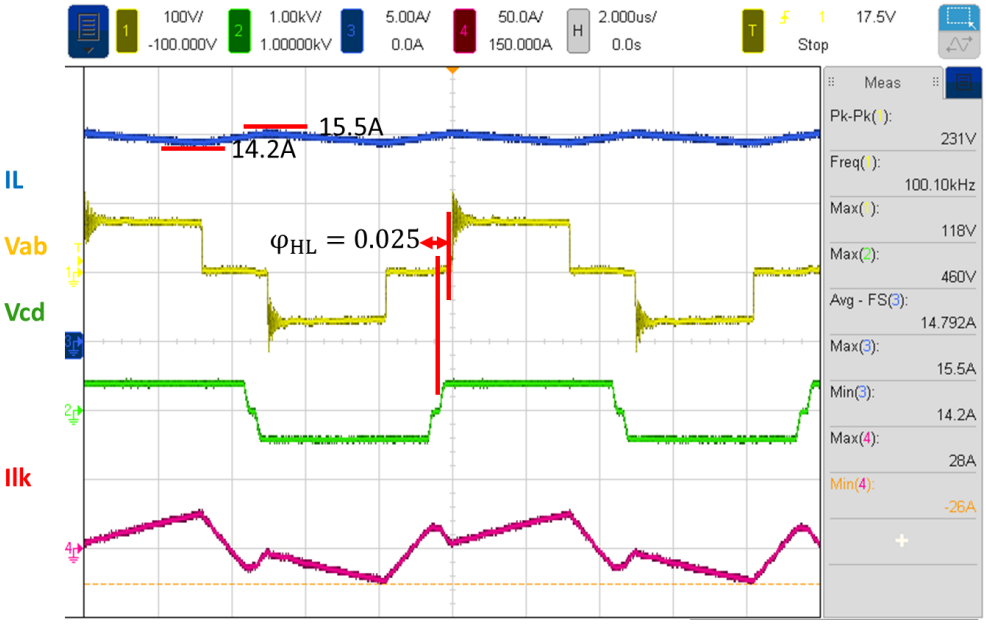


Fig. 5.29 Experiment result of 720W steady-state waveform.

doi:10.6342/NTU202202177

Comparing steady-state results are listed in Table 5.6. Theoretical equation of I_L is (2.32), and the theoretical value of φ_{HL} can be derived by (2.35). The errors of I_L from simulation and experiment are both less than 1.5% and the errors of φ_{HL} are both less than 5%, which shows that the theoretical equation is very closed to simulation and experiment results in 720W case.

Table 5.6 Comparing steady-state results in 720W case.

	I_L(A)	$Error_{IL}$	φ_{HL}	$Error_{\varphi_{HL}}$
Theoretical equation	15		0.0238	
Simulation result	14.97	0.20%	0.0237	0.42%
Experiment result	14.79	1.42%	0.0250	4.80%

To verify the feasibility of ZVS turn-on, deadtime of each switch are all set properly by the previous ZVS condition equations. The feasibility of ZVS is first verified by simulation in Fig. 5.30. The active clamp switch, S_{act}, one LVS switch, S_1, one HVS leading-leg switch, S_5, and one HVS lagging-leg switch, S_8, are shown in simulation. It can be observed that all of the switches achieve ZVS in simulation. To further verify the feasibility of ZVS, experiment results are shown in Fig. 5.31 and Fig. 5.32. It is clear by the results of experiment that all of the switches operate in ZVS. Note that the turn-off spikes in S_{act} and S_{LV} are caused by the oscillator between $C_{ds,LV}$ and active clamp ESL, which is not simulated in Simplis.

doi:10.6342/NTU202202177

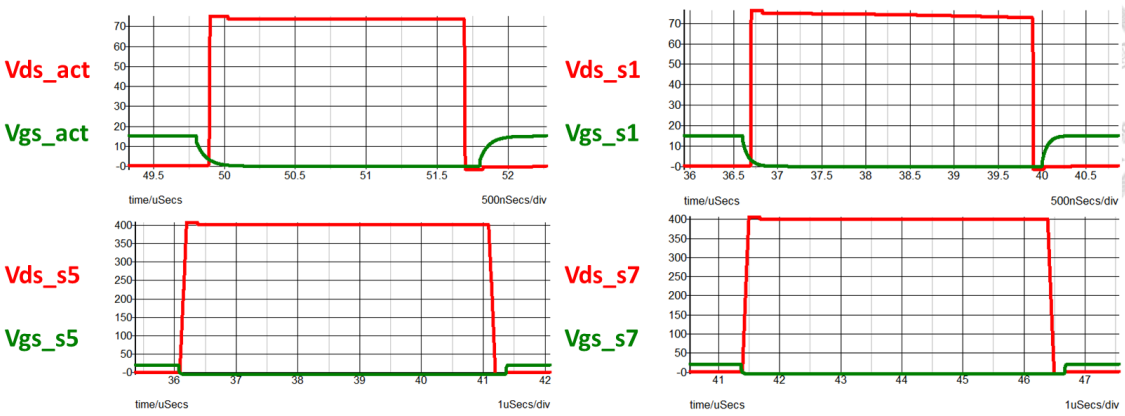


Fig. 5.30 Simulation result of 720W ZVS waveform.

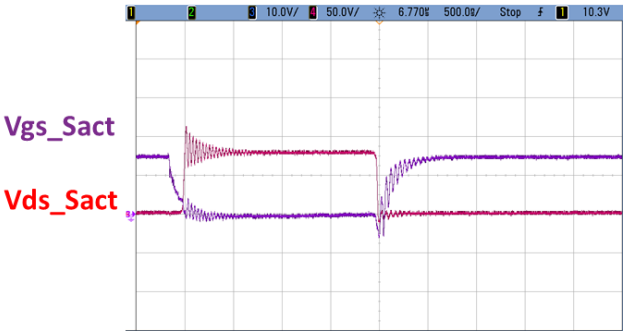


Fig. 5.31 Experiment result of 720W Sact ZVS waveform.

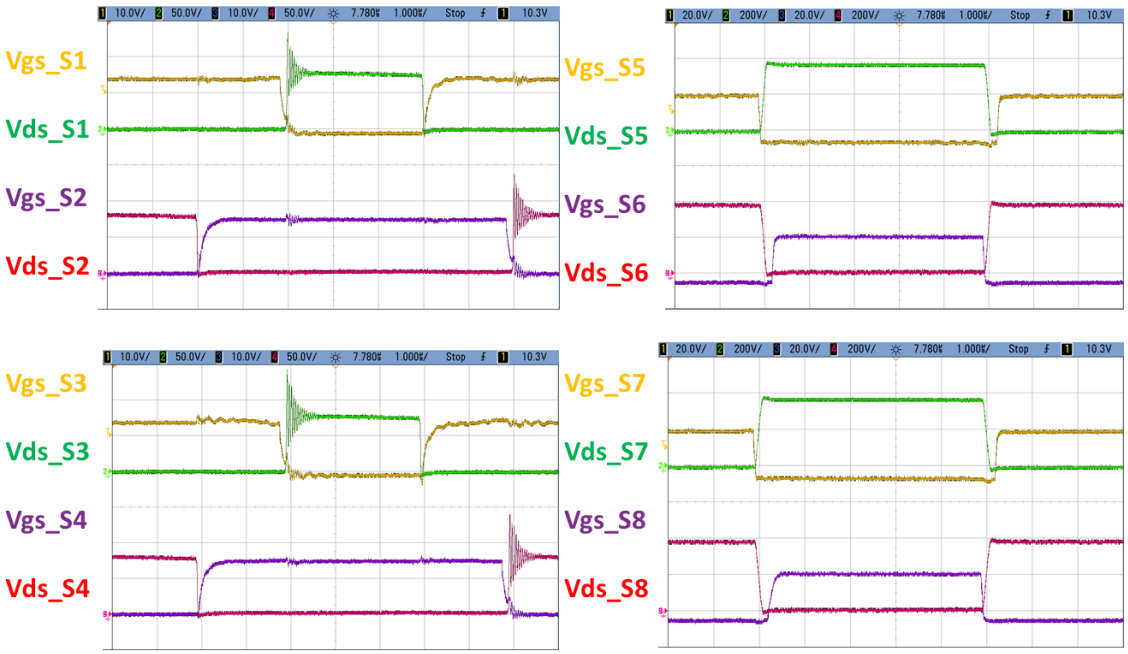


Fig. 5.32 Experiment result of 720W SLV and SHV ZVS waveform.

doi:10.6342/NTU202202177

5.3 Bidirectional Transient Response

After verifying the flexibility of MDPSM in steady-state, the bidirectional transient, which is one of the feature in MDPSM, should be focused, too. In this section, buck-boost and boost-buck operations for each load case are all done. Overshoots of I_L, V_{ca}, and I_{Lk} are concerned, too. To well control the power flow, a PI controller is applied. The detailed control parameters are listed in Table 5.7.

Table 5.7 Contol parameters of the PI controller.

	Kp	Ki
Value	$-5 * 10^{-5}$	-0.625

In [34], it is mentioned that the bidirectional transient of SSM is too heavy to harm the circuit in experiment. In this section, the experiment of SSM is not done. Only the experiment of MDPSM is done to verified the feasibility of bidirectional operation.

doi:10.6342/NTU202202177

(a) 240W Case

Fig. 5.33 shows the simulation results of 240W case, and Fig. 5.34 shows the experiment results. It can be found that the results are a little different between simulations and experiments. The reason is that the parasitic effects are hard to fully model in simulations. But, it can be found that the overshoots of I_L are 20.6% and 10.01% separately from buck-boost and boost-buck operation. And the drops of V_{ca} and I_{Lk} are not obvious in both operation. The bidirectional transients are acceptable and harmless for the hardware circuit.

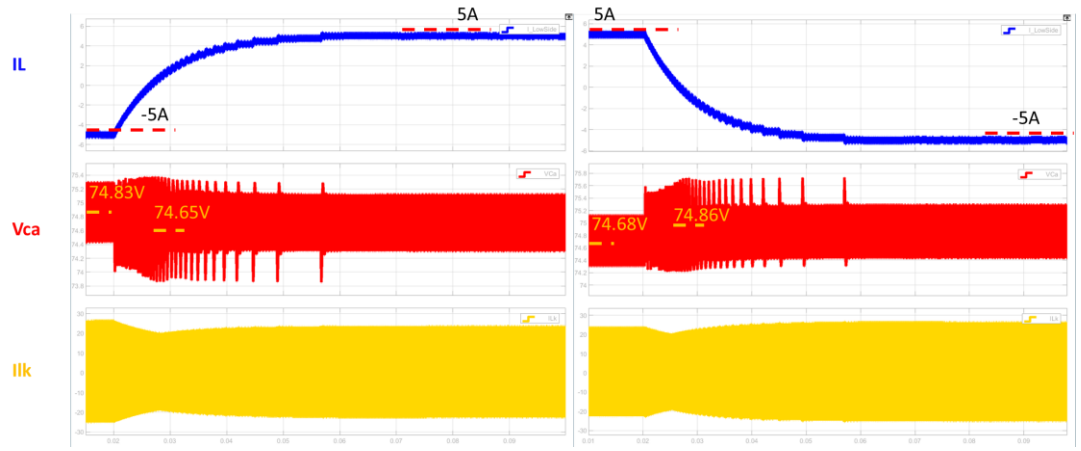
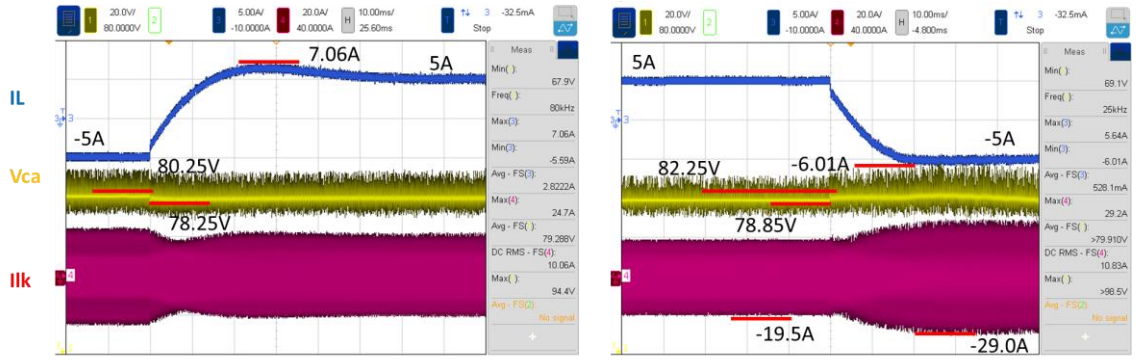


Fig. 5.33 Simulation result of 240W bidirectional transient.



(a) Buck – boost operation. (b) Boost – buck operation.

Fig. 5.34 Experiment result of 240W bidirectional transient.

doi:10.6342/NTU202202177

(b) 480W Case

Fig. 5.35 shows the simulation results of 480W case, and Fig. 5.36 shows the experiment results. Identically, the results are a little different, which is caused by the parasitic effects. By the experiment results, it can be found that the overshoots of I_L are 20% and 10% separately from buck-boost and boost-buck operation. Overshoots of V_{ca} and I_{Lk} are small in both operation. The bidirectional transients are acceptable and harmless for the hardware circuit in both cases.

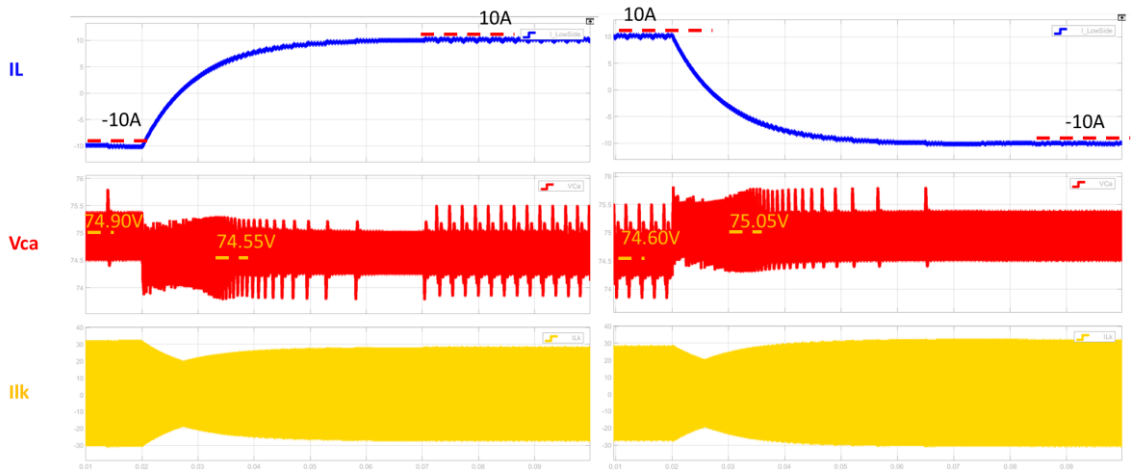
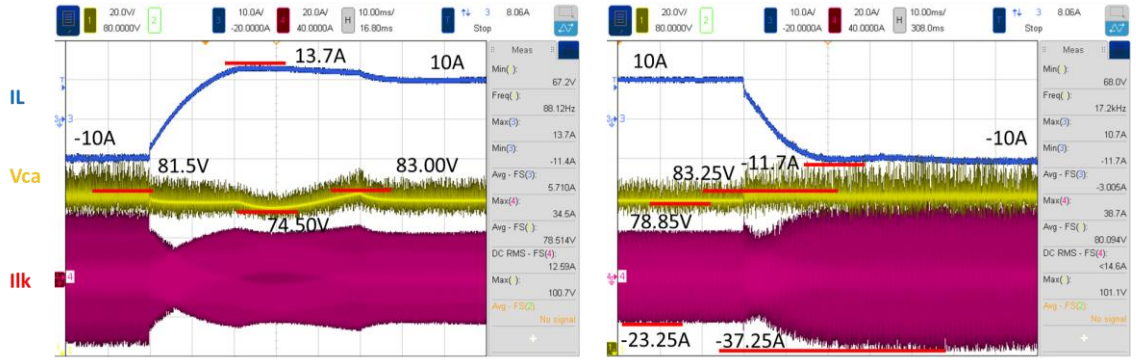


Fig. 5.35 Simulation result of 480W bidirectional transient.



(a) Buck – boost operation. (b) Boost – buck operation.

Fig. 5.36 Experiment result of 480W bidirectional transient.

doi:10.6342/NTU202202177

(c) 720W Case

Fig. 5.37 shows the simulation results of 720W case buck-boost and boost-buck operations, and Fig. 5.38 shows the experiment results. Because the incomplete model of the parasitic effects, the results are a little different. In the experiment results, it can be found that the overshoots of I_L are 20% and 10% separately from buck-boost and boost-buck operation, and the drops of V_{ca} and I_{Lk} are small in this case. The results show that the bidirectional transients are acceptable for this circuit in the full-load case.

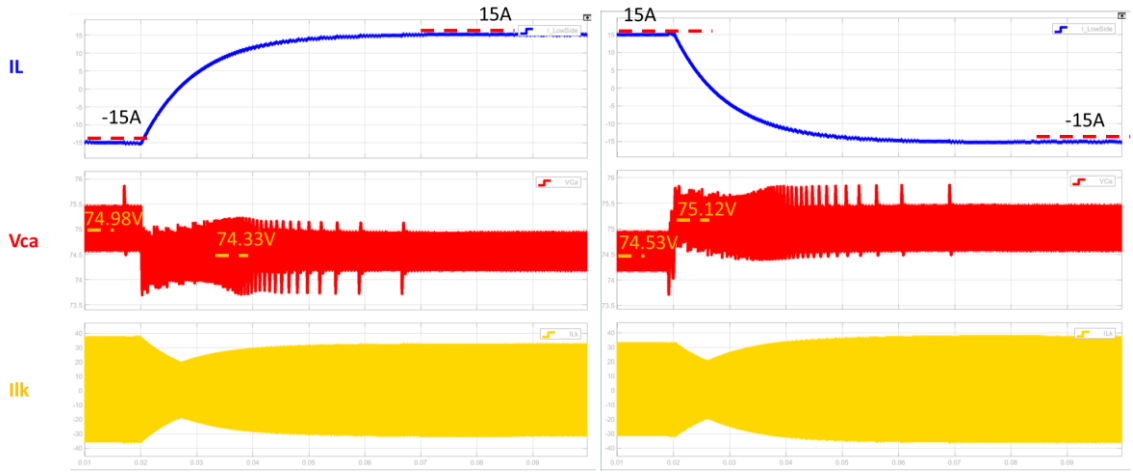
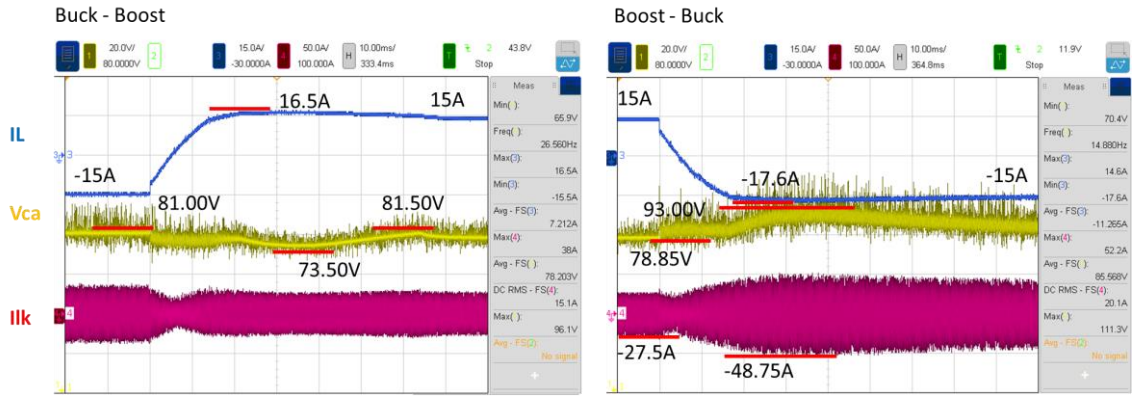


Fig. 5.37 Simulation result of 720W bidirectional transient.



(a) Buck – boost operation. (b) Boost – buck operation.

Fig. 5.38 Experiment result of 720W bidirectional transient.

doi:10.6342/NTU202202177

5.4 Maximum Efficiency Point Tracking Strategy

After fully verification the steady-state and transient response of MDPSM, MEPT should be verification finally. In this section, MEPT is verified with different load cases. I_L is controlled by φ_{HL} in I_L control loop, D_2 is controlled in the efficiency control loop by the perturb and observe method.

In the experiment, to make sure that I_L control loop is well-controlled in steady-state, the period of efficiency control loop is set much larger than I_L control loop with 0.21s. In addition, to verify the tracking of maximum efficiency point, efficiencies of each operation point are also measured. To strike a balance between the resolution and the measured data points, the perturbation of efficiency control loop is finally set to be 0.01.

Because D_2 is hard for the scope to measure directly by V_{cd}, the experimental value of D_2 is demoed by the converted voltage, $V_{converted}$. The realtime value of D_2 is first converted into the duty cycle of one EPWM channel in DSP, and the high resolution mode from the scope is used to filter the EPWM frequency, then $V_{converted}$, the converted voltage from D_2, can be record in the scope. The relationship between D_2 and $V_{converted}$ is shown in Table 5.8. In the following, $V_{converted}$ is shown and the exact values of D_2 are also marked.

Table 5.8 Relationshiop between D2 and converted voltage.

D_2	0.47	0.46	0.45	0.44	0.43	0.42	0.41	0.40
$V_{converted}$	2.4V	2.2V	2.0V	1.8V	1.6V	1.4V	1.2V	1.0V

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(a) -240W Case

Fig. 5.39 shows the experiment result of -240W efficiency control loop. The initial value of D_2 is 0.47, and the perturbation of D_2 is 0.01. It can be found that D_2 keeps the value of 0.45 and 0.43 in the steady-state.

To ensure that the maximum efficiency point is tracked, the efficiencies with different D_2 are measured in Fig. 5.40 by the power meter. Fig. 5.40 indicates that 0.44 is the maximum efficiency point of D_2. The final efficiency of -240W in the maximum efficiency control strategy is 86.295%.

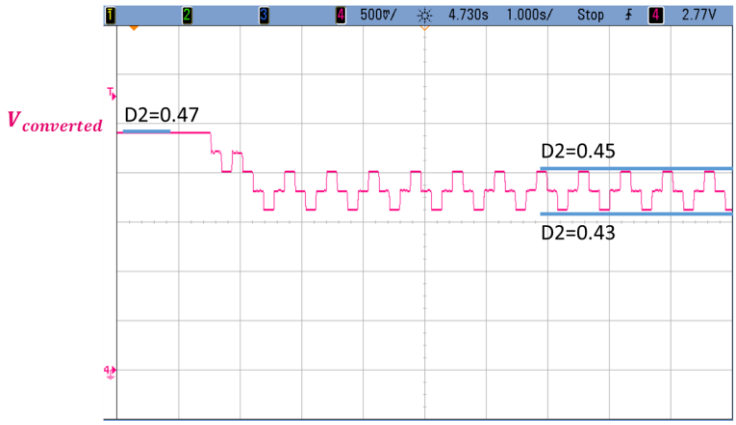

Fig. 5.39 Experiment results of -240W efficiency control loop.

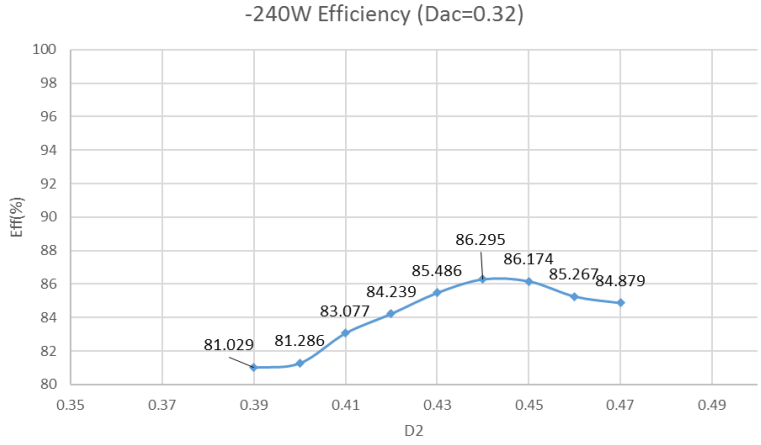

Fig. 5.40 Efficiency versus D2 chart in -240W case.

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(b) -480W Case

Fig. 5.41 shows the experiment result of -480W efficiency control loop. The initial value of D_2 is 0.47, and the perturbation of D_2 is 0.01. It can be found that D_2 keeps the value of 0.46 and 0.44 in the steady-state.

To ensure that the maximum efficiency point is traced, the efficiencies with different D_2 are measured in Fig. 5.42 by the power meter.

Fig. 5.42 indicates that 0.45 is the maximum efficiency point of D_2. The final efficiency of -480W in the maximum efficiency control strategy is 89.86%.

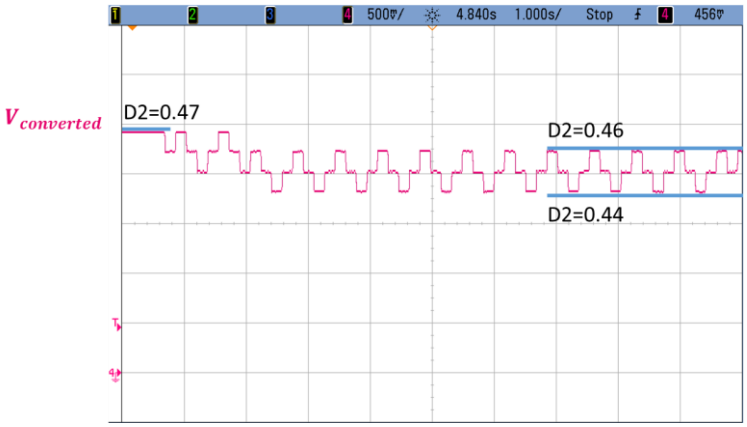

Fig. 5.41 Experiment results of -480W efficiency control loop.

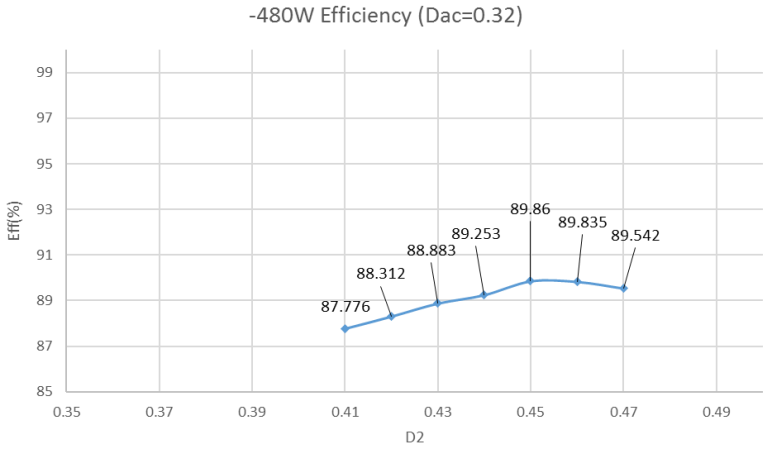

Fig. 5.42 Efficiency versus D2 chart in -480W case.

doi:10.6342/NTU202202177

(c) -720W Case

Fig. 5.43 shows the experiment result of -720W efficiency control loop. The initial value of D_2 is 0.47, and the perturbation of D_2 is 0.01. Because the range of D_2 is from 0.47 to 0.46, the result of the perturb and observe method keeps in 0.47 and 0.46.

The efficiencies with different D_2 can be measured in Fig. 5.44 by the power meter. Fig. 5.44 indicates that 0.46 is the maximum efficiency point of D_2. The final efficiency of -720W in the maximum efficiency control strategy is 90.824%.

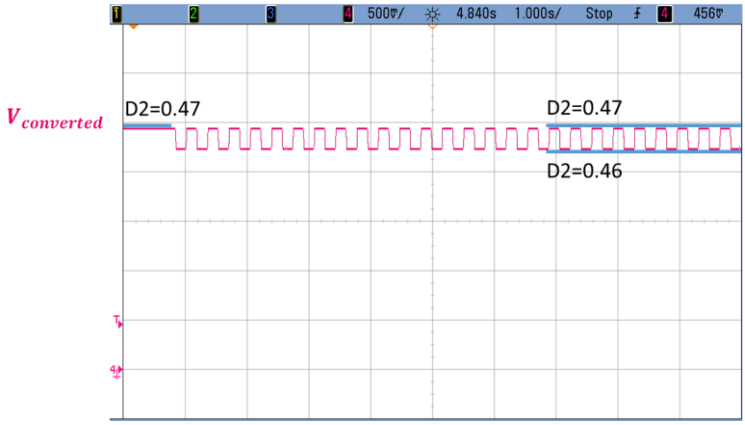

Fig. 5.43 Experiment results of -720W efficiency control loop.

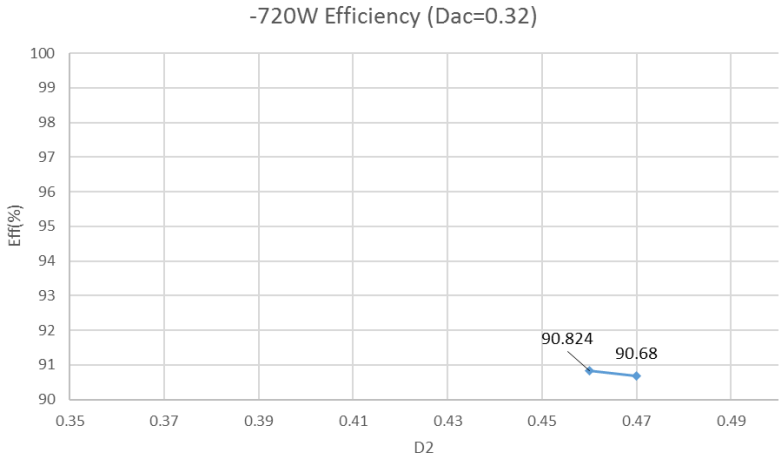

Fig. 5.44 Efficiency versus D2 chart in -720W case.

doi:10.6342/NTU202202177

(d) 240W Case

Fig. 5.45 shows the experiment result of 240W efficiency control loop. The initial value of D_2 is 0.47, and the perturbation of D_2 is 0.01. It can be found that D_2 keeps the value of 0.43 and 0.41 in the steady-state.

To ensure that the maximum efficiency point is traced, the efficiencies with different D_2 are measured in Fig. 5.46 by the power meter. Fig. 5.46 indicates that 0.42 is indeed the maximum efficiency point of D_2. The final efficiency of 240W in the maximum efficiency control strategy is 86.81%.

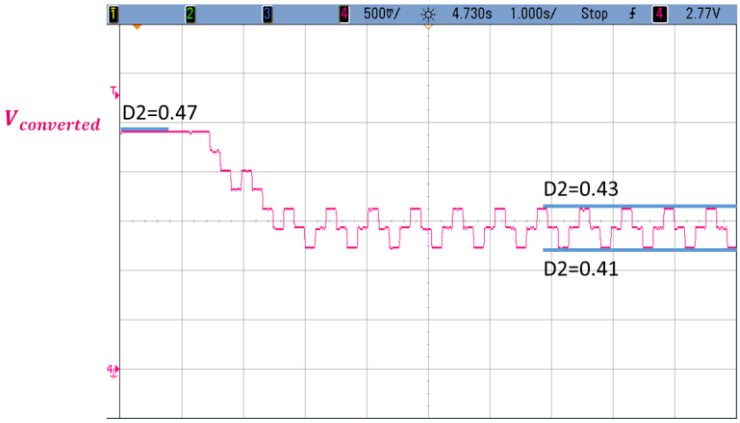

Fig. 5.45 Experiment results of 240W efficiency control loop.

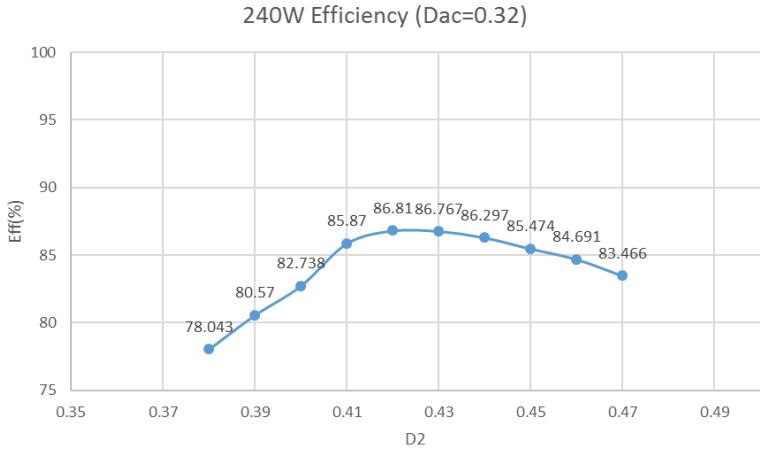

Fig. 5.46 Efficiency versus D2 chart in 240W case.

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(e) 480W Case

Fig. 5.47 shows the experiment result of 480W efficiency control loop. The initial value of D_2 is 0.47, and the perturbation of D_2 is 0.01. It can be found that D_2 keeps the value of 0.43 and 0.42 in steady-state, which is different from other cases. The reason is that the maximum efficiency point is in the lower bound of D_2.

To ensure that the maximum efficiency point is traced, the efficiencies with different D_2 are measured in Fig. 5.44 by the power meter. Fig. 5.44 indicates that 0.43 is the maximum efficiency point of D_2. The final efficiency of -480W in the maximum efficiency control strategy is 91.929%.

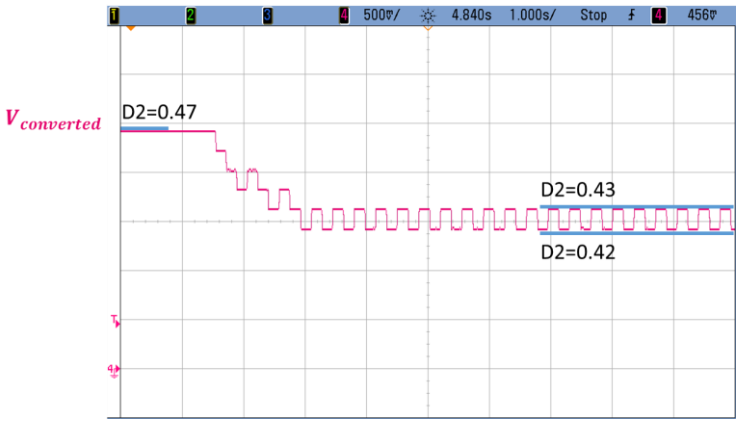

Fig. 5.47 Experiment results of 480W efficiency control loop.

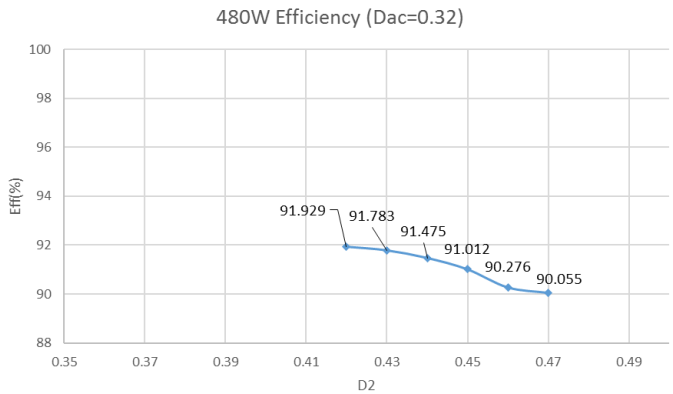

Fig. 5.48 Efficiency versus D2 chart in 480W case.

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(f) 720W Case

Fig. 5.49 shows the experiment result of 720W efficiency control loop. The initial value of D_2 is 0.47, and the perturbation of D_2 is 0.01. Because the range of D_2 is from 0.47 to 0.46, the result of the perturb and observe method keeps at 0.47 and 0.46.

To ensure that the maximum efficiency point is traced, the efficiencies with different D_2 are measured in Fig. 5.50 by the power meter. Fig. 5.50 indicates that 0.46 is the maximum efficiency point of D_2. The final efficiency of -720W in the maximum efficiency control strategy is 91.363%.

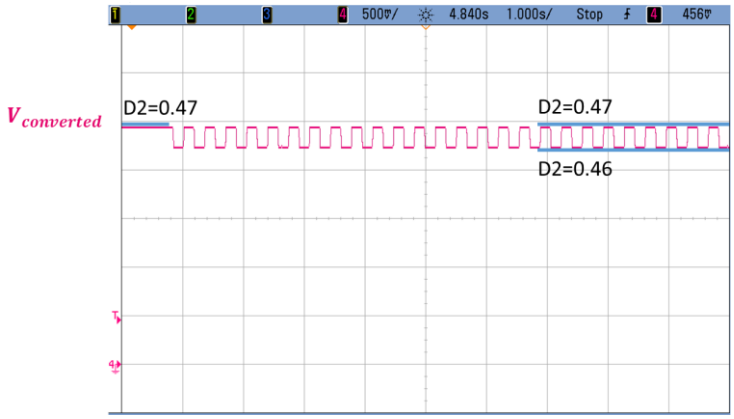

Fig. 5.49 Experiment results of 720W efficiency control loop.

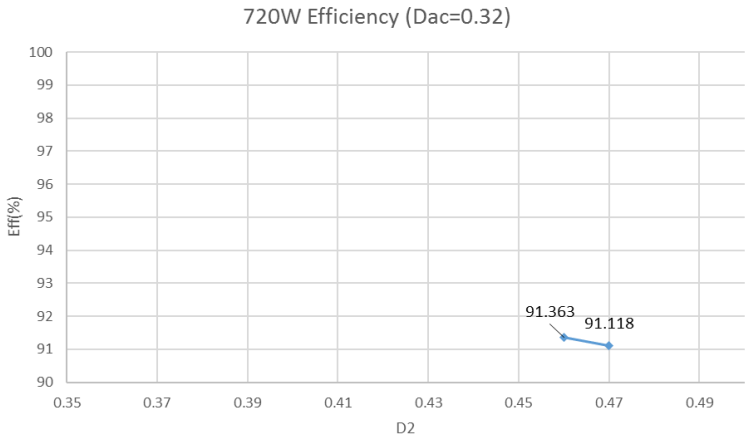

Fig. 5.50 Efficiency versus D2 chart in 720W case.

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Chapter 6 Conclusion and Future Work

6.1 Summary

Modified dual phase shift modulation(MDPSM) for active-clamped current-fed dual active bridge(AC-CFDAB) converter is proposed in this thesis. To control the efficiency, maximum efficiency point tracking strategy(MEPT) is also proposed. The conclusions are summarized in the following:

1. Conventional modulation methods, including ZVZCS modulation and secondary-side modulation(SSM), are introduced and their advantages and disadvantages for them are discussed.
2. MDPSM is proposed and analyzed. The main features of MDPSM are bidirectional power transmission, ZVS for all switches, and improvement for bidirectional transient.
3. MEPT is proposed and analyzed. Power efficiency increases by adjusting the duty cycle of the high-voltage-side switching node voltage.
4. The design process of system parameters, such as transformer and duty cycles, is provided, and the efficiency equations are listed in this thesis.
5. A rated 720W AC-CFDAB converter is realized, and the details of the hardware circuit are provided.
6. Some functions are verified, including steady-state waveform, bidirectional transient, and MEPT, with 240W, 480W, and 720W load cases.

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6.2 Future Works

Some suggested research topics and future works are listed as follows:

1. The small-signal model for MDPSM is not analyzed in this thesis. To discuss more the stability, the compensator designed by the small-signal model can be adapted in future works.
2. The improvement of bidirectional transient just illustrated by the simulations, the quantitative analysis of the response can be considered in future works.
3. The design process in this thesis refers to the process of the conventional modulation method, the optimized design process for MDPSM can be analyzed and adapted in future works.
4. MEPT just takes the duty cycle of high-voltage-side switching node voltage into account, the duty cycle of low-voltage-side switching node voltage can be analyzed in future works.
5. Perturb and observe method is applied in the efficiency control loop. Other methods to trace the maximum efficiency point can be discussed in future works.
6. The research in this paper focuses on the fixed input voltage, the floating input voltage case can be considered in future works.

doi:10.6342/NTU202202177

REFERENCES

[1] P. K. Pathak and A. R. Gupta, "Battery Energy Storage System," 2018 4th International Conference on Computational Intelligence & Communication Technology (CICT), 2018, pp. 1-9, doi: 10.1109/CIACT.2018.8480377.

[2] N. Kawakami and Y. Iijima, "Overview of battery energy storage systems for stabilization of renewable energy in Japan," 2012 International Conference on Renewable Energy Research and Applications (ICRERA), 2012, pp. 1-5, doi: 10.1109/ICRERA.2012.6477391.

[3] N. Chatrung, "Battery Energy Storage System (BESS) and Development of Grid Scale BESS in EGAT," 2019 IEEE PES GTD Grand International Conference and Exposition Asia (GTD Asia), 2019, pp. 589-593, doi: 10.1109/GTDAsia.2019.8715953.

[4] M. Stecca, L. R. Elizondo, T. B. Soeiro, P. Bauer and P. Palensky, "A Comprehensive Review of the Integration of Battery Energy Storage Systems Into Distribution Networks," in IEEE Open Journal of the Industrial Electronics Society, vol. 1, pp. 46-65, 2020, doi: 10.1109/OJIES.2020.2981832.

[5] P. F. Ribeiro, B. K. Johnson, M. L. Crow, A. Arsoy and Y. Liu, "Energy storage systems for advanced power applications," in Proceedings of the IEEE, vol. 89, no. 12, pp. 1744-1756, Dec. 2001, doi: 10.1109/5.975900.

[6] W. C. Liao et al., "Study and implementation of a novel bidirectional DC-DC converter with high conversion ratio," 2011 IEEE Energy Conversion Congress and Exposition, 2011, pp. 134-140, doi: 10.1109/ECCE.2011.6063760.

[7] K. N. Hasan, M. E. Haque, M. Negnevitsky and K. M. Muttaqi, "Control of energy storage interface with a bidirectional converter for photovoltaic systems," 2008 Australasian Universities Power Engineering Conference, 2008, pp. 1-6.

doi:10.6342/NTU202202177

[8] W. T. Yan, L. S. Yang, C. M. Hong, T. J. Liang, J. F. Chen and H. T. Yang, "Fuel cell and battery hybrid supplied power system," 2008 International Conference on Electrical Machines and Systems, 2008, pp. 2676-2680.

[9] R. Hidalgo-León et al., "A survey of battery energy storage system (BESS), applications and environmental impacts in power systems," 2017 IEEE Second Ecuador Technical Chapters Meeting (ETCM), 2017, pp. 1-6, doi: 10.1109/ETCM.2017.8247485.

[10] M. T. Lawder et al., "Battery Energy Storage System (BESS) and Battery Management System (BMS) for Grid-Scale Applications," in Proceedings of the IEEE, vol. 102, no. 6, pp. 1014-1030, June 2014, doi: 10.1109/JPROC.2014.2317451.

[11] H. Matsuo and F. Kurokawa, "New Solar Cell Power Supply System Using a Boost Type Bidirectinal DC-DC Converter," in IEEE Transactions on Industrial Electronics, vol. IE-31, no. 1, pp. 51-55, Feb. 1984, doi: 10.1109/TIE.1984.350020.

[12] F. Caricchi, F. Crescimbini, G. Noia and D. Pirolo, "Experimental study of a bidirectional DC-DC converter for the DC link voltage control and the regenerative braking in PM motor drives devoted to electrical vehicles," Proceedings of 1994 IEEE Applied Power Electronics Conference and Exposition - ASPEC'94, 1994, pp. 381-386 vol.1, doi: 10.1109/APEC.1994.316373.

[13] R. D. Middlebrook, S. Cuk and W. Behen, "A new battery charger/discharger converter," 1978 IEEE Power Electronics Specialists Conference, 1978, pp. 251-255, doi: 10.1109/PESC.1978.7072361.

[14] M. Dantas, F. Oliveira, L. Albuquerque, I. Freitas and R. Andersen, "A Hybrid Bidirectional Push-Pull DC-DC Converter with a Ladder Switched-Capacitor Cell," 2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern

doi:10.6342/NTU202202177

Power Electronics Conference (COBEP/SPEC), 2019, pp. 1-6, doi: 10.1109/COBEP/SPEC44138.2019.9065614.

[15] K. Venkatesan, "Current mode controlled bidirectional flyback converter," 20th Annual IEEE Power Electronics Specialists Conference, 1989, pp. 835-842 vol.2, doi: 10.1109/PESC.1989.48567.

[16] Hui Li, Fang Zheng Peng and J. S. Lawler, "A natural ZVS medium-power bidirectional DC-DC converter with minimum number of devices," in IEEE Transactions on Industry Applications, vol. 39, no. 2, pp. 525-535, March-April 2003, doi: 10.1109/TIA.2003.808965.

[17] S. A. Gorji, H. G. Sahebi, M. Ektesabi and A. B. Rad, "Topologies and Control Schemes of Bidirectional DC–DC Power Converters: An Overview," in IEEE Access, vol. 7, pp. 117997-118019, 2019, doi: 10.1109/ACCESS.2019.2937239.

[18] B. Zhao, Q. Song, W. Liu and Y. Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter for High-Frequency-Link Power-Conversion System," in IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 4091-4106, Aug. 2014, doi: 10.1109/TPEL.2013.2289913.

[19] S. Yao, G. Liu, Y. Zhao, Z. Zhu and B. Zhao, "Optimal control strategy of dual-active-bridge converter for battery energy storage system," 2014 China International Conference on Electricity Distribution (CICED), 2014, pp. 1220-1224, doi: 10.1109/CICED.2014.6991901.

[20] S. Inoue and H. Akagi, “A bidirectional isolated dc-dc converter as a core circuit of the next-generation medium-voltage power conversion system,” IEEE Trans. Power Electron., vol. 22, no. 2, pp. 535–542, Mar. 2007.

[21] B. Zhao, Q. Yu, and W. Sun, “Extended-phase-shift control of isolated bidirectional dc-dc converter for power distribution in microgrid,” IEEE Trans. Power Electron.,

doi:10.6342/NTU202202177

vol. 27, no. 11, pp. 4667–4680, Nov. 2012.

[22] T. Hirose and H. Matsuo, “A consideration of bidirectional superposed dual active bridge dc-dc converter,” in Proc. 2nd IEEE Int. Symp. Power Electron. Distrib. Generation Syst., 2010, pp. 39–46.

[23] F. Krismer and J. W. Kolar, “Accurate small-signal model for the digital control of an automotive bidirectional dual active bridge,” IEEE Trans. Power Electron., vol. 24, no. 12, pp. 2756–2768, Dec. 2009.

[24] X. Li and A. K. S. Bhat, “Analysis and design of high-frequency isolated dual-bridge series resonant dc/dc converter,” IEEE Trans. Power Electron., vol. 25, no. 4, pp. 850–862, Apr. 2010.

[25] W. Chen, P. Rong, and Z. Y. Lu, “Snubberless bidirectional DC-DC converter with new CLLC resonant tank featuring minimized switching loss,” IEEE Trans. Ind. Electron., vol. 57, no. 9, pp. 3075–3086, Sep. 2010.

[26] J. H. Jung, H. S. Kim, M. H. Ryu, and J. W. Baek, “Design methodology of bidirectional CLLC resonant converter for high-frequency isolation of dc distribution systems,” IEEE Trans. Power Electron., vol. 28, no. 4, pp. 1741–1755, Apr. 2013.

[27] P. Xuewei and A. K. Rathore, "Novel bidirectional snubberless soft-switching naturally clamped zero current commutated current-fed dual active bridge (CFDAB) converter for fuel cell vehicles," 2013 IEEE Energy Conversion Congress and Exposition, 2013, pp. 1894-1901, doi: 10.1109/ECCE.2013.6646939.

[28] K. Wang, C. Y. Lin, L. Zhu, D. Qu, F. C. Lee and J. S. Lai, "Bi-directional DC to DC converters for fuel cell systems," Power Electronics in Transportation (Cat. No.98TH8349), 1998, pp. 47-51, doi: 10.1109/PET.1998.731056.

[29] X. Pan, H. Li, Y. Liu, T. Zhao, C. Ju and A. K. Rathore, "An Overview and

doi:10.6342/NTU202202177

Comprehensive Comparative Evaluation of Current-Fed-Isolated-Bidirectional DC/DC Converter," in IEEE Transactions on Power Electronics, vol. 35, no. 3, pp. 2737-2763, March 2020, doi: 10.1109/TPEL.2019.2931739.

[30] J. A. Sabate, V. Vlatkovic, R. B. Ridley and F. C. Lee, "High-voltage, high-power, ZVS, full-bridge PWM converter employing an active snubber," [Proceedings] APEC '91: Sixth Annual Applied Power Electronics Conference and Exhibition, 1991, pp. 158-163, doi: 10.1109/APEC.1991.146157.

[31] Jung G. Cho, Geun H. Rim and F. C. Lee, "Zero voltage and zero current switching full bridge PWM converter using secondary active clamp," PESC Record. 27th Annual IEEE Power Electronics Specialists Conference, 1996, pp. 657-663 vol.1, doi: 10.1109/PESC.1996.548651.

[32] Kunrong Wang, F. C. Lee and J. Lai, "Operation principles of bi-directional full-bridge DC/DC converter with unified soft-switching scheme and soft-starting capability," APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.00CH37058), 2000, pp. 111-118 vol.1, doi: 10.1109/APEC.2000.826092.

[33] Kunrong Wang, Lizhi Zhu, Dayu Qu, H. Odendaal, J. Lai and F. C. Lee, "Design, implementation, and experimental results of bi-directional full-bridge DC/DC converter with unified soft-switching scheme and soft-starting capability," 2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018), 2000, pp. 1058-1063 vol.2, doi: 10.1109/PESC.2000.879959.

[34] 許蕙瀅（2021）。二次側調變方法之主動箝位電流饋入式雙主動橋式轉換器。國立臺灣大學電機工程學研究所碩士論文，台北市。

[35] Zhiliang Zhang and Xinbo Ruan, "A novel double phase-shift control scheme for

doi:10.6342/NTU202202177

full-bridge three-level converter," Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005., 2005, pp. 1240-1245 Vol. 2, doi: 10.1109/APEC.2005.1453162.

[36] H. Bai and C. Mi, "Eliminate Reactive Power and Increase System Efficiency of Isolated Bidirectional Dual-Active-Bridge DC–DC Converters Using Novel Dual-Phase-Shift Control," in IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 2905-2914, Nov. 2008, doi: 10.1109/TPEL.2008.2005103.

[37] S. Bal, D. B. Yelaverthi, A. K. Rathore and D. Srinivasan, "Improved Modulation Strategy Using Dual Phase Shift Modulation for Active Commutated Current-Fed Dual Active Bridge," in IEEE Transactions on Power Electronics, vol. 33, no. 9, pp. 7359-7375, Sept. 2018, doi: 10.1109/TPEL.2017.2764917.

[38] Brown, J. (n.d.), *Power MOSFET Basics: Understand-ing Gate Charge and Using It To Assess Switching Performance*, Vishay Siliconix, 2016.

[39] Laszlo Balogh, *Fundamentals of MOSFET and IGBT Gate Driver Circuits.* Texas Instruments, 2018.

[40] Texas Instruments, “TMS320F2833x, TMS320F2823x Digital Signal Controllers (DSCs),” F28335 datasheet, Feb. 2021.

doi:10.6342/NTU202202177