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微波選擇性摻雜劑激活機制的發現及其在實現重 n 型摻雜矽接面穩定性的作用

Discovery of a novel microwave-selective dopant activation mechanism and its role in junction stability for highly n-doped silicon

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誌謝

首先感謝李世光教授和許聿翔教授，他們給予我自由和寬廣的博士研究工作空間，並即時審閱研究進度並提出建議，確保了研究成果的質量。特別是，他們對提交給期刊的手稿進行非常詳細和嚴格的審查。另外我也特別感謝李教授太太 Julie Lee 神速又詳細到每一細節的論文審閱功力令人配服, 如果沒有老師們設定的高標準，就不可能完成具體且嚴謹的研究工作。老師們親切博學嚴謹的治學態度著實令我打從內心尊敬, 很慶幸自己能有這樣的際遇跟隨一流的學者耳濡目染。儘管矽半導體產業已經是一項成熟的技術，但關於選擇性摻雜劑激活機制的發現和它解決長久以來重 n 型摻雜矽接面熱穩定性問題所展現的潛能仍是令人鼓舞的劃時代發現。它為退火技術開闢了新思路，並激勵未來的研究人員思考如何有效地應用熱處理和非熱的能量耦合方式來克服材料退火面臨的熱預算相容性問題。這漫長的六年的研究生過程可以說是轟轟烈烈，期間還歷經不可思義的跨國公司與學校合作。我與台積電林佑明博士四年多的一百多次白板討論，我從完全無法解釋到逐漸勾勒出實現低溫回火實驗結果背後的涵義。我通過與應用材料公司科學家 Hans-Joachim Ludwig Gossmann 的討論，他建議我聯繫在西班牙專門研究密度泛函理論 (DFT) 計算的 Lourdes Pelaz 教授。 Lodures 教授的“DFT”計算證實了不穩定的低階磷空位簇 P_nV (n=1-3) 恰巧都具非消失偶極矩，而穩定的 P_4V 是非極性的且沒有偶極子。該計算結果強化了我提出的選擇性摻雜劑退火模型，另外通過與中央大學溫偉源教授使用 XRD 和正電子湮沒技術，本研究能夠表徵退火前後 Si：P 應變遷移並驗證空位分佈變化以支持我提出的選擇性摻雜激活模型的合理性也是跨校合作的團隊精神的表現.康奈爾大學教授 James C Hwang 根據微波腔中感受器裝置的位置及其相對於諧振腔的臨界尺寸對微波場的分佈進行了建模得出在三重平行基座之間建立駐波的能力是將微波能量有效地耦合到矽晶格中的非活性摻雜劑結構的關鍵。 我對這些西方學者深厚學問與合作時展現開闊的心胸充滿配服與感激, 沒有他們在理論計算上的支援這牽連龐大的複雜工作不可能完成。最後謝謝家人特別是養育我的父母親以及太太其禎在背後的體諒與包容讓我毫無懸念得以完成具體且重要的半導體研究成果。

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中文摘要

在現代 CMOS 3D 晶體管架構、FinFET 和環柵 (GAA) 納米片晶體管中，源漏形成需要原位重摻雜外延矽層來滿足器件性能要求。然而，在過去 30 年中，眾所周知，施者(donor)在高摻雜半導體中往往會失活。當矽中的施者濃度高於 2 x 10^{20} at/cm^3 時，將漸漸開始觀察到施者的失活並導致電導率下降。相關研究工作表明施者喜好以圍繞空缺(Vacancy)組態出現, 而根據摻雜濃度的高低施者失活機制是由於低階 PV 通過遷移和動態聚集（D_nV，n=1-4）轉變為更高階 P_2V、P_3V. 甚至在濃度高到 1 x 10^{21} at/cm^3 可進一步轉化為 P_4V 等施者空位簇 (donor-vacancy cluster)。這是由於其負形成能 P_3V 和 P_4V 在熱力學上是較有利的配置。因此，Si 中的施者濃度越高，其表現出的熱穩定性越低，這造成可用的自由載流子濃度因此受到限制並且不能隨著供體化學濃度的增加而增加。現代 FinFET 和環柵(GAA)納米片晶體管結構的源漏極中使用的典型磷濃度通常高於 2 x 10^{21} at/cm3，因此源漏結存在嚴重的熱穩定性問題。然而，據目前所知，儘管施者失活的機制透過過去四十年各方研究已得到完整的理解, 但到目前為止，施者失活仍被視為熱回火的本徵問題因此還沒有關於這種現像是否可以得到緩解和解決的討論。雖然通過最先進的閃光或激光退火進行額外的外延後摻雜劑活化是目前增加活化摻雜劑的唯一方法，但其回火後活化摻雜劑的熱穩定性問題仍然存在。本研究的目的是進一步揭示供體失活的機制並提供有關施者空位簇 (D_nV) 的更有用的電子特性，以便能鑒往知來可以開發一種替代退火解決方案，該解決方案不僅可以激活摻雜劑，還可以解決熱穩定性問題。通過從頭計算(ab initio calculation)，我發現了施者空位簇更多有用的電子特性，如偶極矩、晶格振動頻率和形成能。本研究逐步應用這些特性之間的關係來開發實用的退火解決方案，以克服長期存在的供體失活問題並將早期關於供體失活機制的研究，即磷空位簇（P_nV，n＝1-4）動態聚集形成模型擴展到 P_nV 偶極矩的從頭計算。結合已知的 P_nV 形成能，理論計算證明熱不穩定的低階 P_nV（n＝1-3）總具有非零偶極矩而熱穩定的高階 P_nV 則不具有淨偶極矩. 這個特別偶極矩分佈可被用於透過與震盪電場選擇性的交互作用實現選擇性摻雜劑激活。通過穩定和不穩定摻雜劑-空位簇之間的偶極矩區別，本研究嘗試開發一種能量選擇

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性相互作用退火方法來實現高 n 摻雜 Si 的熱穩定結(Junction)。選擇性摻雜劑激活工藝方案的實施有望通過消除不穩定的 P_nV 來實現回火後只存在熱穩定的 P_4V 從而實現穩定結。但對於擇性摻雜劑激活所需震盪電場邊界條件並非簡單可得，本研究將通過引入各種感受器(susceptor)配置來探索各種微波腔設置，以探索在低於 700 攝氏度的最佳感受器配置下選擇性摻雜劑激活是否可被實現，在最佳感受器配置找到之後再根據微波腔中感受器設置的位置及其相對於諧振腔的臨界尺寸對微波場的分佈進行了建模。 得出的結論是，在三重平行感受器基座之間建立駐波的能力是將微波能量有效耦合到矽晶格中的非活性摻雜劑結構的關鍵。最後，通過涉及霍爾測量、二次離子質譜 (SIMS) 和 XRD 以及正電子湮沒技術的薄膜表徵技術，以實驗與分析方法驗證選擇性摻雜激活的機制。

關鍵字：施者失活、摻雜劑空位簇、微波回火、熱穩定結、摻雜劑激活、施者、磷空位簇、外延矽、退火

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ABSTRACT

In modern CMOS 3D transistor architectures, FinFETs, and gate-all-around (GAA) nanosheet transistors, source-drain formation requires in-situ heavily doped epitaxial silicon layers to meet device performance requirements. However, it has been known for the past 40 years that donors tend to be deactivated in highly doped Si. When the donor concentration of phosphorus in silicon is higher than 2 x 10^{20} at/cm^3, deactivation of the donors will start to be observed and lead to a decrease in conductivity. Relevant research has shown that donors prefer to move toward and form a structure around vacancies. At the doping concentration of 2 x 10^{20} at/cm^3, through the migration and dynamic aggregation of donors and vacancies, the deactivation mechanism can asymptotically transform donors into PV pairs, P_2V, and higher-order P_3V, etc. P_3V can be further converted into donor vacancy clusters such as P_4V at concentrations up to 1 x 10^{21} at/cm^3. This effect is due to the negative formation energy, which leads to the thermodynamically favorable configuration of P_3V and P_4V. Therefore, the higher the donor concentration in Si, the lower its thermal stability. This results in the available free carrier concentration being thus limited and challenging to increase with increasing donor chemical concentration. Typical phosphorous concentrations used in the source-drain of modern FinFET and gate-all-around (GAA) nanosheet transistor structures are typically higher than 2 x 10^{21} at/cm^3, so the source-drain junction has serious thermal stability issues. To the best of our knowledge, although the mechanism of donor inactivation has been well understood through tremendous studies over the past four decades, donor deactivation has so far been regarded as an inherent problem of thermal annealing. Thus, no discussion existed on whether this phenomenon can be alleviated and resolved. Although additional post-epitaxial dopant activation by state-of-the-art flash or laser annealing is currently the

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only way to increase activated dopants, the problem of thermal stability of their post-annealing activated dopants persists. This study aims to reveal the mechanism of donor deactivation further and to investigate more useful electronic properties of donor vacancy clusters (D_nV_s) so that an alternative annealing solution beyond existing ones based purely on thermal effects can be developed. It not only activates dopants but also addresses long-term thermal stability issues associated with thermal-based annealing. Through ab initio calculations, several important electronic properties of donor-vacancy clusters, such as dipole moment, lattice vibrational frequency, and formation energy, are revealed in this work. The relationship between these properties will be used to develop practical annealing solutions to overcome the long-standing problem of donor deactivation. This work extended an earlier study on the mechanism of donor inactivation, namely the dynamic aggregation formation model of phosphorus-vacancy (P_nV, n = 1-4) clusters, to calculate P_nV dipole moments. Combining with the known P_nV formation energies, theoretical calculations have demonstrated that thermally unstable lower-order P_nV_s (n = 1-3) always have a non-zero dipole moment while thermally stable higher-order P_nV s do not have a net dipole moment. Particularly, the distribution of this dipole moment can be used to achieve selective dopant activation through selective interaction with Microwave oscillating electric fields. Due to the clear difference between stable and unstable dopant-vacancy clusters, I am trying to develop an energy-selective interaction annealing method to achieve thermally stable junctions of highly n-doped Si. Interaction of microwave electric fields with polar phosphorus vacancy clusters (P_nV) is expected to eliminate unstable low-order P_nV (n=1-3) structures, which are the major contribution to the de-activation process. As a result, the typical donor deactivation phenomenon can be effectively suppressed. However, the oscillating electric field boundary conditions required for selective dopant activation are not readily available. Various microwave

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cavity setups are explored by introducing various susceptor configurations to choose the optimal susceptor configuration. After finding the optimal susceptor configuration, selective dopant activation is successfully achieved. A model is also built for the microwave field distribution according to the location and dimension of the susceptor set in the microwave cavity. It is concluded that the ability to establish standing waves between triple-parallel pedestals is the key to the efficient coupling of microwave energy into inactive dopant structures in the silicon lattice. Finally, Hall measurements, secondary ion mass spectrometry (SIMS) and XRD, and positron annihilation techniques are applied for characterizations. It is experimentally and analytically verified to support the mechanism of selective doping activation.

Keywords: donor deactivation, dopant vacancy clusters, microwave annealing, thermally stable junctions, dopant activation, donors, phosphorus vacancy clusters, epitaxial Si:P, annealing

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Chapter 1 Introduction

In recent decades, the semiconductor industry has developed a new generation of CMOS scaling processes every two years, with each generation reducing the minimum structure size by a factor of about 0.7 to achieve an improvement in area size of about 0.5. The innovation of squeezing more and more transistors onto a chip has resulted in doubling the number of transistors every two years (see Figure 1.1 and Figure 1.2)[1, 2] and maintaining the pace of Moore's Law [3]. However, due to the higher process complexity and the larger number of photomask steps, the development time for the latest technology generations, e.g., 5 nm and beyond, has taken longer than the normal two-year pace. Nevertheless, the 5-nm and 4-nm technologies used in iPhones offer above-average transistor density improvement, allowing us to increase transistor density at a rate that doubles approximately every two years.

The impact of these remarkable scaling technologies of CMOS on human civilization can be seen from the most advanced electronic products in the market. For example, the Apple's M1 Ultra (two dies in one chip) commercial dual-chip microprocessor based on ARM has reached 114 billion, as shown in Table 1. The system was manufactured using TSMC's 5nm semiconductor manufacturing process [4, 5]. As shown in Figure 1.3, the power efficiency of the CPU and GPU of the M1 Ultra used in Studio 2022 MAC can be improved by a factor of 10 compared to the best products at that time. The largest number of transistors on an IC chip so far in 2020 is a deep learning engine, Cerebras' Wafer Scale Engine 2. It uses design strategies to bypass any non-running cores on the device, enabling up to 2.6 trillion MOSFET chips. This unique chip is manufactured by TSMC using a 7nm FinFET process [6]-[10]. These amazing achievements illustrate how innovation in manufacturing processes for further CMOS scaling is impacting modern

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microelectronics and changing the real world. This dissertation, "Discovery of a novel microwave-selective dopant activation mechanism and its role in junction stability of highly n-doped silicon," is part of the effort to further scaling CMOS technology. This dissertation presents the problems of the dopant activation mechanism in CMOS scaling technology, explains how to obtain useful step-by-step hints from a long-standing problem, and uses the experience accumulated by the predecessors to discover the microwave-selective dopant activation mechanism to solve the problem.

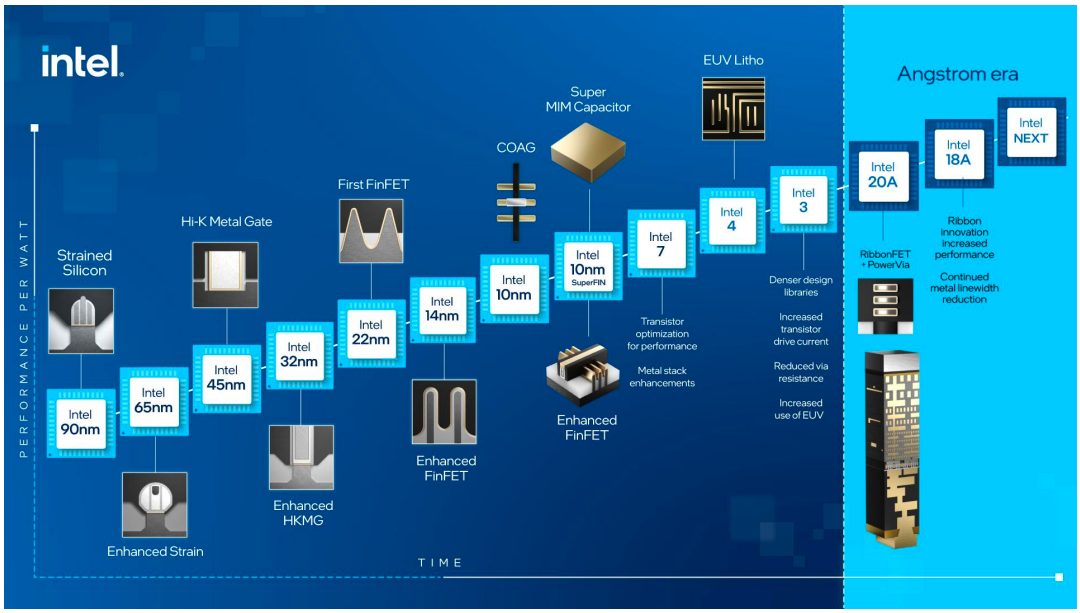

Figure 1.1 Transistor evolution from Intel's past 90nm technology node to the future evolution of the Angstrom era. This is mainly due to technological innovations such as high-k dielectric and metal gate technology, FinFET 3D transistors, GAA nanosheet transistors, and strained silicon, through which Intel can keep up with the rhythm predicted by Moore's Law. [1]

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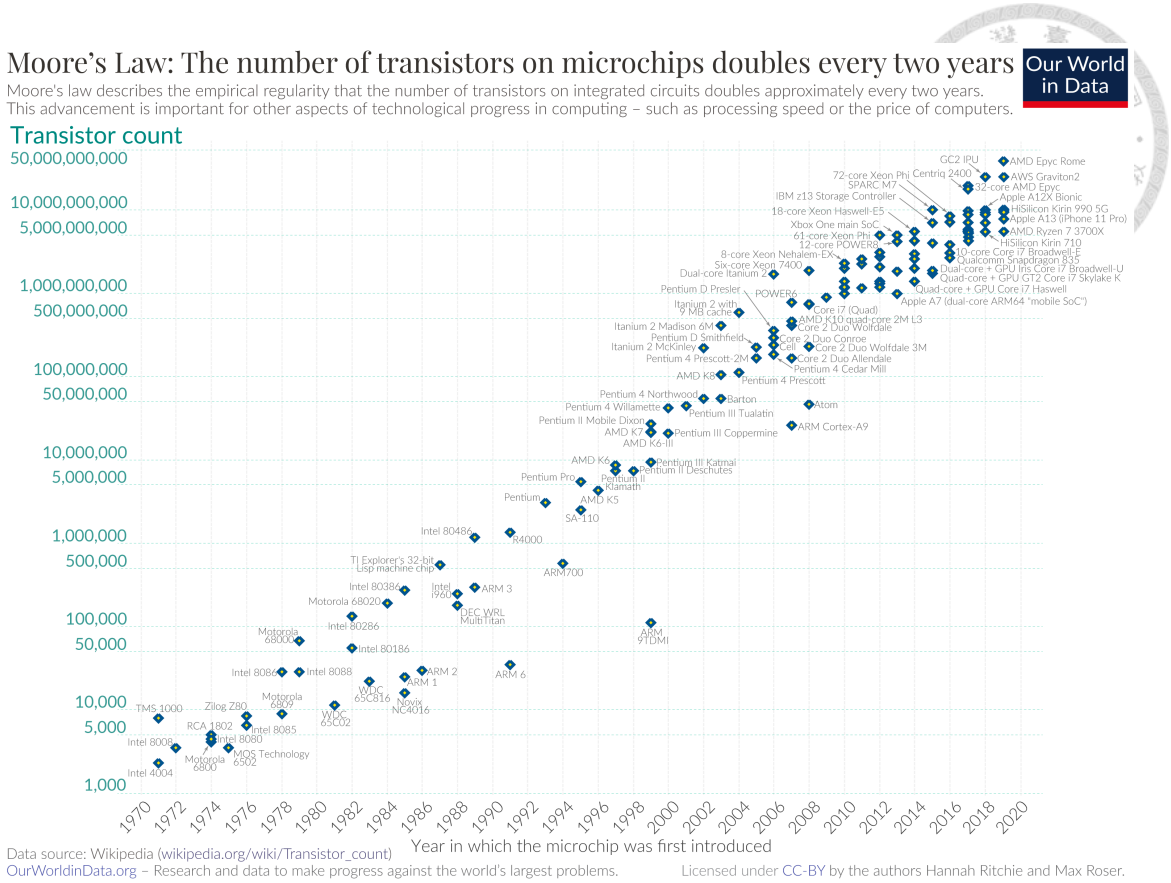

Figure 1.2 Moore's Law Transistor Count 1970-2020. As shown, the transisror count is double for every two years [2].

Year	Component	Name	Number of MOSFETs (in billions)
2022	microprocessor (commercial)	Apple M1 Ultra	114 (dual die in same chip) 1140 億
2022	GPU	Nvidia H100	80
2020	DLP	Colossus Mk2 GC200	59.4
2020	any IC chip	Wafer Scale Engine 2	2600 (one wafer one die) 26000 億
2019	any IC chip	Samsung's V-NAND chip	2000 (stack)

Table 1.1 As of 2022, the transistor count in commercially available chips including microprocessor, GPU, deep learning processor (DLP) and memory [4]–[10]

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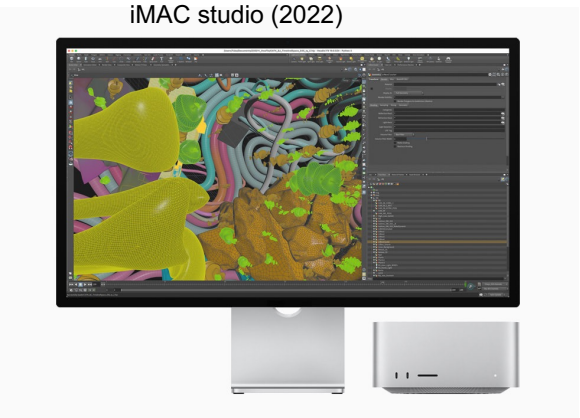

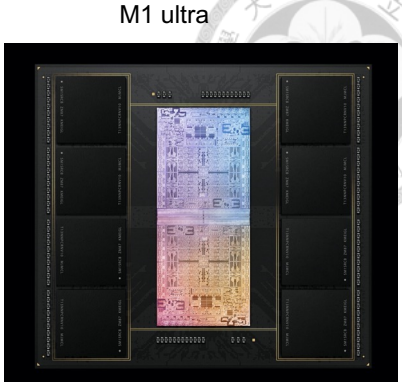

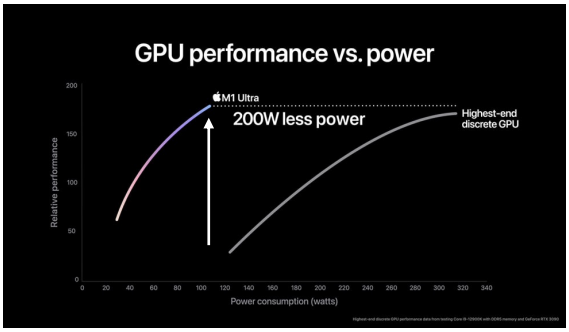

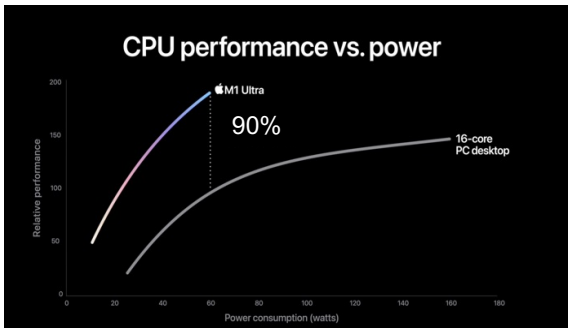

Figure 1.3 Released in 2022, the M1 Ultra combines two M1 Max chips in the same package to drive the MAC studio. M1 Ultra, M1 Max, and M1 vary widely in size and transistor cell count. For example, the original M1 chip used only about 16 billion transistors, while the single chip with dual dies design gives the M1 Ultra 114 billion transistors. It was 10 times more energy efficient than the best chips at the time [4, 5].

The silicon-based semiconductor manufacturing technology on which CMSO scaling relies is the origin of today's digital economy. Advanced chips have been the foundation for technological innovations such as artificial intelligence (AI) and next-generation wireless communication technologies through continuous development over the past few decades. High-speed electronic circuits on a chip wafer depend on the concentration of free charge carriers in CMOS transistors. Increasing free carrier concentration at Si junctions requires high concentrations of electroactive dopants,

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usually determined by doping and annealing techniques. However, the introduction of transistors with three-dimensional (3D) nanostructures such as nanowires and nanosheets [13, 14] creates new challenges in forming impurity-doped regions. With the downsizing of CMOS to the 16-nm technology node, transistor structures have evolved from planar transistor structures to 3D FinFET transistor structures to meet performance requirements. Since the 2-nm technology node, 3D transistor structures have evolved to nano-sheet transistor structures that enable further scaling of CMOS. These 3D transistor structures require new source-drain formation techniques (Figure 1.4) to achieve abrupt control of the doping profile to meet short channel requirements while maintaining low series resistance, including source-drain (Rsd) and contact resistance (Rcsd).

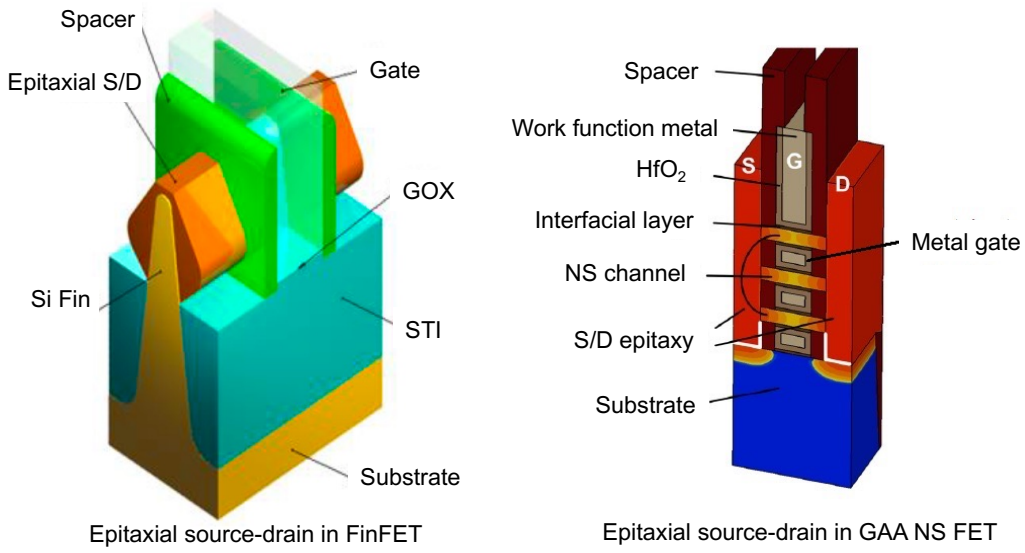

Figure 1.4 The epitaxial source-drain structure in FinFET and gate-all-around (GAA) nano-sheet transistor structures [13, 14].

Recessed source-drain and heavily doped epitaxial SiP techniques were introduced [15]- [18]. However, heavily doped epitaxial Si:P with phosphorus concentrations higher than 1 x 10^{21} at./cm^3 exhibits severe donor stability problems, requiring post-annealing to

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activate the doping. Post-epitaxial Si:P annealing techniques with millisecond annealing, such as flash annealing or laser annealing techniques with a time scale of micro- or nanoseconds, can promote dopant activation. However, these activated dopants are usually thermally unstable. This problem of inherent donor stability is a long-standing issue in semiconductor applications and leads to temperature limitations in subsequent CMOS fabrication processes after the S/D dopant activation annealing process.

Therefore, in this dissertation, an alternative annealing technique will be developed to solve the abovementioned high-temperature annealing problems. I started with an overview of low-temperature microwave annealing to improve the compatibility of the annealing technique with the materials used in modern CMOS fabrication. From today's scientific perspective, low-temperature targets for dopant activation are largely unphysical and unrealistic. This is because dopant activation is thermally based. Regardless of how heat is generated, they end up the same way in the physical world. The new low-temperature dopant activation method will run into the typical problems of inadequate dopant activation and damage repair, which are still essentially the same as with conventional rapid thermal annealing. However, relying on intuition alone, without a deep understanding of physics, one is sometimes free from the constraints of one's mind, which knows no barriers. This effect sometimes offers a new way to get in touch with a new physical world. This study aimed to achieve an R_s-X_j value comparable to conventional millisecond annealing at temperatures below 700 °C to avoid diffusion of dopants. This was finally completed after a lengthy study of overseas annealing devices and numerous experiments with various microwave cavity setups. This work has shown that microwaves can effectively activate doping of highly doped Si:P at temperatures below 700 °C when an optimal tri-parallel susceptor setup and sample configuration are used. Compared to the prior art, the obtained flat junctions were shown for the first time

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to provide the high carrier concentration that MSA processes can typically achieve at temperatures above 1100 °C. In addition, microwave annealed junctions show excellent thermal stability at a moderate heat budget of 700 °C.

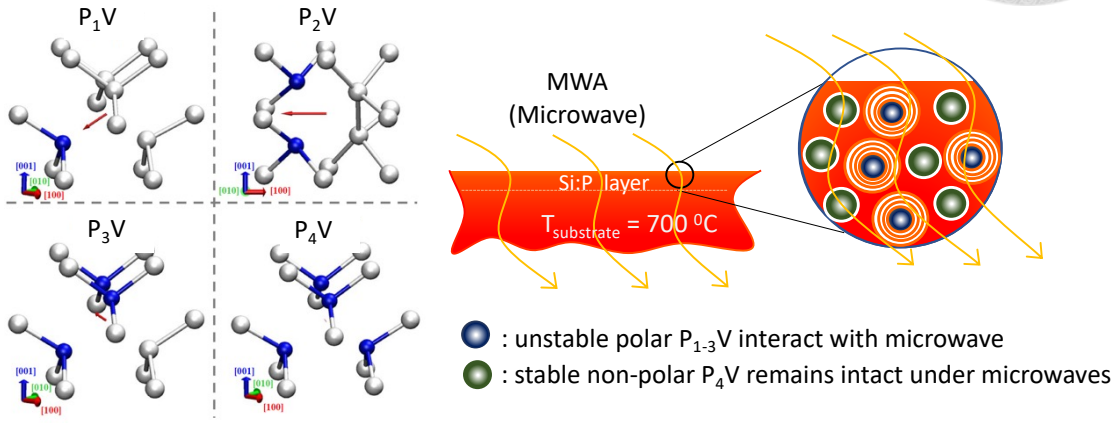

Figure 1.5 The net atomic dipole moment orientation of the P_nV complex is indicated by the red arrow in the center of the atomic structure. The white spheres are Si atoms, and the dark (blue) spheres are P atoms. Only atoms up to the second vacancy neighbor are shown for better visibility, and the net dipole is centered on the vacancy. The bonding of dangling bonds around vacancies in P_2V can be clearly seen in this representation. The right inset depicts microwaves achieving selective dopant activation through energy coupling directly to non-vanishing dipole moments in P_nV (n = 1-3). This contrasts with non-selective dielectric heating that supports the bulk temperature of the sample.

However, this result has long puzzled us since conventional RTA annealing at or near 700 °C is unlikely to activate the heavily doped epitaxial Si:P, but rather deactivate the phosphorus (the donor). This implies that dopant activation must occur by mechanisms other than thermal effects. Through further investigation of the donor deactivation mechanism and additional ab initio calculations, it's found that the known dopant-vacancy clusters (P_nV, n = 1-4) that dominate the donor deactivation mechanism have

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individually different thermal stabilities and dipole moments. The thermally unstable P_nV (n=1-3) show a nonzero dipole moment dependence, while the thermally stable P_4V shows no dipole moment. Taking advantage of the different electronic properties of stable P_4V and unstable $P_{1-3}V$, this study aims to explain the annealing mechanism as a possible selective annealing scheme that can selectively activate thermally unstable P_nV structures (n = 1 -3) (Figure 1.5). Thus, the obtained annealed junction is thermally stable, and the heavily doped junctions can withstand the thermal budget (~ 600 - 700 degrees C) of other processes after the subsequent source-drain annealing process. In short, by discovering a novel phenomenon of selective dopant activation, efficient activation of dopants in highly n-doped silicon can be achieved at lower temperatures below 700 °C with stable junctions.

Chapter 1 overviews how CMOS scaling has enabled transistor density and count over the past few decades and the practical implications. This chapter presents the motivation for this study and the explanation of how to address the typical problem of donor deactivation and how to achieve thermal stability in highly n-doped silicon. Donor deactivation is a long-standing problem in the semiconductor industry.

Chapter 2 discusses Moore's Law and its lofty insights into doubling the number of transistors on a chip every two years. Direct CMOS scaling is an important approach to implementing Moore's Law, and it continues to this day. CMOS scaling gradually leads to short-channel effects due to shortened gate length, or drain-induced barrier low (DIBL) effects. Short-channel effects are a fundamental problem that must be overcome by introducing 3D transistor structures such as FinFETs and gate-all-around (GAA) nanosheet transistors. The 3D transistor architecture revolutionizes the formation of source-drain junctions. In the past, the ion implantation technology used in planar transistor structure for a long time can no longer effectively distribute the dopant in the source-drain of the Fin structure due to the shadowing effect. The shadow effect is created

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by the polysilicon gate of the 3D CMOS structure and the photoresist thickness required for the implanted photo process. The S/D of 3D transistor structures is formed by two-stage steps of S/D groove process and CVD in-situ doped Si epitaxy process. Chapter 3 begins with an introduction to design considerations for source-drain epitaxy, including electrical conductivity, abrupt dopant distribution, and strain-engineered material properties that induce channel strain and enhance carrier mobility. Doped Si:P formation processes, such as those produced by chemical vapor deposition, are introduced. It then describes the donor deactivation issues associated with highly doped epitaxial Si:P and the requirements for post-epitaxial Si:P annealing processes. It is concluded that while millisecond annealing can satisfy the requirements for dopant activation and abrupt transition, the obtained junction is thermally unstable. This background motivated this work to investigate a new dopant activation technique that targets additional thermal stability requirements in addition to the basic dopant activation and abrupt junction requirements. At the end of this chapter, preliminary results of microwave annealing are briefly presented , which not only show that excellent dopant activation and abrupt junctions can be achieved at 680 °C are only possible with millisecond annealing at 1150 °C, but also show additional unique advantages in stabilizing junctions. Based on the collected data, it is suspected that the thermal stability advantage may be due to the non-vanishing dipole moment associated with the unstable donor vacancy clusters and their selective interaction with microwaves . This motivated us to perform ab initio calculations to reveal more useful electronic properties such as formation energies, electron density plots, and dipole moments of donor vacancy clusters. Chapter 4 provides an initial overview of previous research efforts to understand the mechanisms of donor deactivation. This work extends from the ab initio work of our earlier predecessors to our calculations of lattice vibrational modes and dipole moments of P_nV to exploit their properties for

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selective dopant activation, to be mentioned later. Chapter 5 gives a comprehensive insight into the interaction of microwaves with matter and silicon. This involves thermal and non-thermal effects. In terms of thermal effect, it is divided into conduction heating and dielectric heating. Dielectric heating involves dielectric losses due to all the different charge polarization phenomena. This knowledge helps us explain how microwaves couple energy with epitaxial Si:P layers and bulk silicon substrates. Next, this paper shows how microwave annealing systems can be explored and optimized to achieve the desired selective doping activation. By distinguishing between polar and non-polar P_nVs, this study experimented with microwave cavity setups, including various parallel pedestal setups, and ultimately found that dopants can be activated at temperatures below 700 °C. After the breakthrough of low temperature doping activation technology, it was verified that the junction realized by low temperature microwave doping activation technology showed unexpected thermal stability advantages, which is also a breakthrough in this research era. Finally, this work is devoted to understanding the origin of low-temperature microwave tempering and thermal stability. It first introduces the formation energies and dipole moments of vacancy dopant clusters and their junctions to build a model of selective dopant activation, including how microwaves select coupling energies to nonpolar P_nV for low-temperature annealing and thermal stability. Chapter 6 summarizes the observations and points out that some mysteries remain in explaining how energy couples to P_nV. Suggested research priorities for future interested researchers are also presented..

The related research results of this dissertation work have been previously published in two journals: “Tsai, *et al.* (2021). Achieving junction stability in heavily doped epitaxial Si: P. Materials Science in Semiconductor Processing, 127, 105672.” and “Tsai, C. H.,et al. (2022). Efficient and stable activation by microwave annealing of nanosheet

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silicon doped with phosphorus above its solubility limit. Applied Physics Letters, 121(5), 052103.” This diserttation has cited both papers and obtained permission to reuse content. Reuse permissions have been placed in the appendix.

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Chapter 2 CMOS Scaling

2.1 Technology scaling and its limits

T The history of lithography has been related to shortening the wavelength of the light source, starting with the earliest lasers, through ArF and KrF, excimer lasers, and, more recently, extreme ultraviolet (EUV) lasers. This has played an important role in promoting the continuous development of CMOS scaling. However, lithography is generally expected to encounter obstacles to spatial resolutions beyond the sub-five nanometers. Although this application is still far away, the industry will consider other alternative light/energy sources of shorter wavelengths, such as electron beams or X-rays to achieve spatial resolution requirements.

CMOS scaling limitations in the nanometer range may come from the laws of physics. An example is when the source-drain ratio is very close (currently estimated to be 7nm), the carriers in the channel reach the ballistic limit; in this case, due to the short stroke. The carrier velocity reaches saturation velocity, causing the channel to drive current to advance, reach the limit and cannot ascend. The problem is that CMOS scaling will likely last at least 20 years before encountering a similarly more drastic revolutionary change. While the physical limit is often discussed, it is far from it. The evolution of transistor structure innovations from planar structures to 3D gate-all-around (GAA) transistor structures shows that the semiconductor industry is still very effectively following Moore's Law, overcoming various engineering bottlenecks, driving CMOS miniaturization, and deepening human civilization. In this chapter, the theory of CMOS scaling and the relationship between short-channel effects and innovations in 3D transistor structures that require new source-drain formation techniques in high-n-doped

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silicon technology are described in detail. Dopant activation issues related to high n-doped silicon are the focus of the remainder of this article.

2.1.1 CMOS scaling theory

In general, insights from "Moore's Law" [19-30] refer to the periodic and continuous scaling of the three-dimensional physical feature size of silicon-based complementary metal-oxide-semiconductor (CMOS) transistors through semiconductor design and fabrication. This theory of deep insight and huge vision has been the main driving force behind the production of today's complex electronic device technology. The scaling theory proposed by Dennard et al. in 1972 started this success story [31]. Although ten years later, the semiconductor industry began to practice this theory in CMOS transistors. From then to today, the semiconductor industry has integrated more and more transistors into a single integrated circuit (IC) chip. Even more surprising, the actual evolution of CMOS scaling is consistent with Gordon E. Moore's 1965 predictions. That is, the total number of transistors that can be integrated into a chip, or so-called chip transistor density, doubles approximately every two years [32] without a corresponding significant increase in chip cost.

Mead [33] and Dennard [23] had the foresight in the early 1970s that MOS transistor structures could be scaled to smaller physical sizes. Their proposed scaling theory describes explicitly strategies and methods for scaling metal-oxide-semiconductor field-effect transistors (MOSFETs) to continue the goals of increasing transistor area density, transistor performance, and reducing chip power consumption. The central idea calls for scaling the transistor’s gate length, gate width, gate oxide thickness, and supply voltage by the same ratio and increasing the channel doping by the inverse of the same ratio (see Figure 2.1). The overall expected equivalent result would be a chip with a smaller area,

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higher drive current transistors, and lower parasitic capacitance for lower power consumption. Despite the shrinking size, the theoretical design of scaling keeps the field strength in the MOS transistor constant across technology nodes. So the original design of scaling theory is constant field scaling. Therefore, constant field scaling requires lowering the supply voltage at each technology node. When transistor fabrication technology arrived in the 1980s, the constant-field scaling strategy was replaced by the new constant-voltage scaling thinking. In constant voltage scaling, only all dimensions of the MOSFET are scaled "s" times, but the supply voltage and terminal voltage are controlled unchanged during transistor scaling. Therefore, the electric field inside the device does not remain constant but increases from generation to generation. Until the early 1990s, gate dielectric TDDB and increased channel hot-carrying currents caused excessive power dissipation and heating when the electric field was increased. In severe cases, field-induced aging inside the device could cause serious product safety problems. Therefore, in the 1990s, constant field scaling was applied to technical scaling. This classic scaling theory was used successfully by the industry before the 130nm generation in the early 2000s.

Device or circuit parameter	Scaling factor
Device dimension *tox, L, W*	$1/\kappa$
Doping concentration *Na*	κ
Voltage *V*	$1/\kappa$
Current *I*	$1/\kappa$
Capacitance $\varepsilon A/t$	$1/\kappa$
Delay time/circuit *VC/I*	$1/\kappa$
Power dissipation/circuit *VI*	$1/\kappa 2$
Power density *VI/A*	1

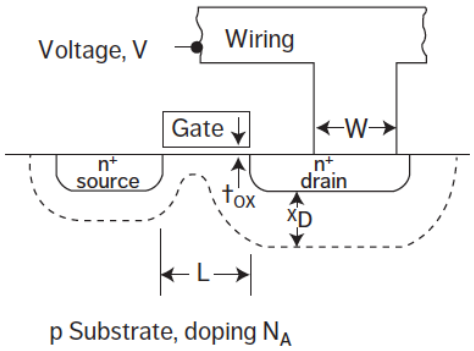

Figure 2.1 Classical MOSFET scaling as described by Robert Dennard [33, 34]

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2.1.2 Moore's Law

"Moore's Law" is famous because its scale scaling theory accurately predicts the practice and application of CMOS fabrication in transistor scaling. Intel co-founder Gordon Moore predicted in 1965 that chip improvements would allow processor speed and overall processing performance to double every two years. Unlike general physics, Moore's Law is purely a phenomenological observation until 2022. It has been accurate for 57 years. Moore's Law has become an evolutionary guide for computer processor manufacturing. Figure 2.2 shows its validity until today [34]. Thanks to Moore's Law, iPhones, iMAC, and various other devices are steadily improving. While it's intuitive that Moore's Law can't go on forever, predictions of the limits of size reduction have proven to be the most insightful horizons.

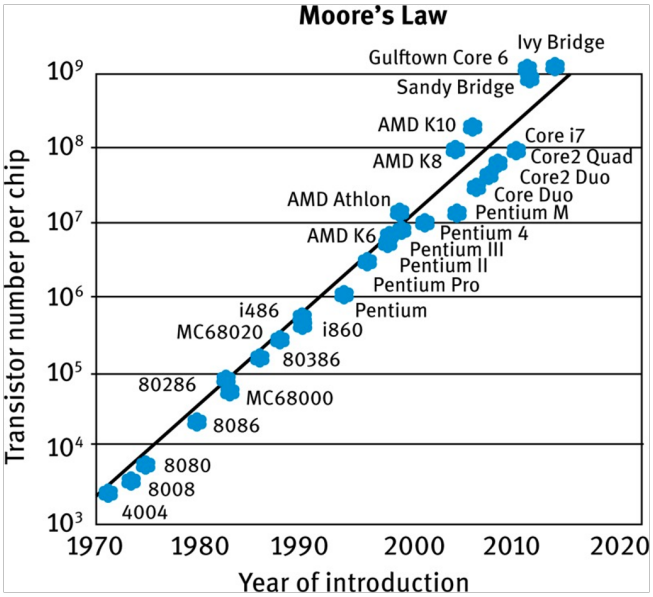

Figure 2.2 "Moore's Law" was a far-reaching and dynamic observation made by Intel co-founder Gordon Moore in 1965, and the law was slightly revised in 1975. The graph shows that it is still accurate until 2020 [34]

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2.1.3 Scaling to the limits

Although the practice of scaling CMOS transistors has repeatedly surpassed some of the "wall barrier" predictions reported in [35], persistent pessimists still believe that it will fail in the nanoscale world. They often cite that CMOS transistors are approaching the physical boundaries of atomic and quantum mechanics [36]. Furthermore, it is worrying that the device itself cannot continue to operate stably and explore its limitations from an economic and technical point of view. The important challenges that may be the main obstacles to further scaling of CMOS are divided into five main parts, which are summarized as follows [37]:

Physical size scaling brings challenges: As devices shrink, tunneling and short-channel leakage currents will become more and more serious, which will affect and limit the performance of CMOS devices, especially the power consumption part.

Materials Science Challenge: The first is that dielectric materials, such as high-k materials for gate stack applications and very low-k materials for back-end (BEOL), cannot provide the required insulation while maintaining electrical properties. The second is that wiring materials such as copper, cobalt, and tungsten cannot provide reliable conduction for continuous scaling. These all rely on materials science innovations to overcome the above challenges.

Power Consumption and Heat Disspitation Challenges: This is because transistor scaling drives the rapid increase in the number of transistors per unit area integrated with technology, resulting in greater power consumption and higher heat dissipation. Inherent transistor leakage and advanced packaging play a key role in dealing with power and dissipation issues.

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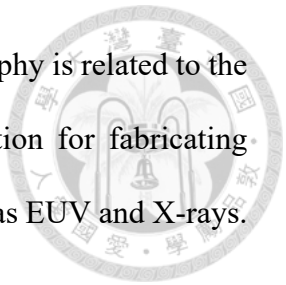

Lithography Technical Challenges: The bottleneck in lithography is related to the ability to provide sub-optical wavelength (e.g. sub-10 nm) resolution for fabricating CMOS devices. This relies on the development of light sources such as EUV and X-rays.

Cost and Economic Challenges: This is mainly due to rising production, manufacturing, and testing costs, which can become unaffordable from an economic point of view. As CMOS shrinks to the 2nm node, few players can afford the investment cost and risk..

However, apparently from the past to 2022, and 15 years from 2022, the above challenges do not appear to be any fundamental constraints preventing Moore's Law from characterizing integrated circuits. With endless device scaling, the complexity of semiconductor process technology continues to increase. This phenomenon acts as the "innovation engine" that drives Moore's Law [38]. For the past 20 years, the semiconductor industry has been developing next-generation process technologies. Each generation shrinks minimum feature sizes (such as Polygate-to-Polygate pitch and Fin-to-Fin pitch) by about 0.7, achieving an area scaling improvement of approximately 0.5x (see Figure 2). Recently, the increase in the complexity of scaling transistors has been accelerating. Advanced process technologies have extremely small feature sizes that require multiple exposures (multiple patterns) or EUV to reproduce these features on silicon accurately. With the advancement of technology nodes, the application of EUV [39]-[42] has gradually expanded from Back-End-of-Line (BEOL) to Middle-End-of-Line (MEOL) and is also widely used in Front-End-of-Line at 3nm and 2nm nodes. Line (FEOL). In addition, the evolution of transistors from planar transistor structures to 3D FinFET and nanosheet transistor structures [42]-[44] has further enhanced gate-to-channel control, and these technologies play a key role in enabling smaller size and higher

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performance devices. Recent generations of technology, such as the sub-5nm node, took slightly longer than the normal two-year cadence. Nonetheless, semiconductor fabrication techniques have provided rapid, periodic improvements in transistor density, allowing us to increase transistor density.

Even if Moore's Law does not end in the next 15 years, the scientific community has long proposed several alternative material solutions in addition to Si materials to extend the life of CMOS scaling once Si reaches its performance limit. For example, two-dimensional materials (2DM) that are atomically monolayer thick have caused a great research boom in the past two decades to overcome the degradation of carrier mobility when the thickness of Si is reduced below 5 nm. Its unique electronic, thermal, and mechanical properties make 2DM an alternative possible approach to fabricate new complementary metal oxide semiconductor (CMOS) and CMOS devices [45]–[47].

2.1.4 The effect of scaling on the circuit performance

Transistor scaling is the primary method for implementing high-performance logic and memory devices. A 30% shrink per technology node for CMOS shrink will ultimately result in a 30% reduction in parasitic capacitance and doubling the device density before the gate length reaches its limit. This ultimately results in a 40% increase in clock frequency while significantly reducing power consumption and active power per conversion by roughly 60% and 50%, respectively.

With the industry's aggressive scaling of CMOS technology to improve performance, overcoming the detrimental short-channel effect (SCE) derived from shrinking channel lengths to reduce device leakage has been the focus of MOSFET scaling [48, 49]. As the channel length shrinks, this indirectly decreases gate-to-channel controllability due to increased charge sharing from source/drain, the so-called drain-induce-barrier-lowing (DIBL) effect. The progress of the introduction of new materials, the innovation of

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transistor structures and related processes such as lithography, etching, and thin film deposition process continue to achieve this goal [48,49].

2.2 Short channel effects

In CMOS transistors, the short-channel effect is evident when the channel length in the MOSFET is scaled down close to the depletion width of the source and drain junctions [50-52]. With aggressive technology scaling to improve performance, addressing the detrimental short-channel effects (SCE) caused by shrinking channel lengths has been a focus of MOSFET scaling. The introduction of the 3D FinFET transistor structure at the 16nm technology node is mainly to overcome this short-channel effect caused by CMOS scaling. These effects include drain-induced barrier reduction, velocity saturation, quantum confinement, and hot carrier degradation. Since their introduction in 1959, field-effect transistors (FETs) have been built primarily in the silicon plane. In 2012, at the 20nm node, to maintain the scaling path of Moore's Law, especially in suppressing the short channel problem, the industry made the first transition from "planar" MOSFET to Fin Field Effect Transistor (FinFET) architecture. Additionally, in 2020, to continue enabling CMOS scaling and overcoming the SCE, the semiconductor industry has migrated from FinFET to gate-all-around(GAA) nanosheet transistor structures [53, 54] at the 2nm technology node.

2.2.1 The “short channel” definition

Lg is often used to denote the physical length of a CMOS transistor. The actual length of channel L is not equal to Lg, but Lg minus the gate and S/D overlap width. The overlap width of gate and S/D is derived from dopant diffusion and thus its control is related to the epitaxial S/D and annealing process. The gate lengths Lg > L and L always track Lg

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(Figure 2.3(a)). Still, the difference (Lg - L) cannot be precisely quantified because the asymptotic profile of the lateral doping profile has no well-defined interface. The term short channel effect originates because CMOS scaling all involves more or less channel length scaling. And every channel length reduction always brings unwanted effects such as DIBL.

2.2.2 Drain-induced-barrier-lowering (DIBL)

Drain-Induced Barrier Lowering (DIBL) is a special effect that occurs only in short channels with high drain voltages. Simply put, short channel lengths lead to crosstalk between source and drain. This can be explained by the fact that when a high positive voltage is applied to the drain, the depletion region formed around the drain and its thickness extends into the channel region , resulting in less charge near the gate requiring a smaller inversion voltage. The whole effect can also be explained by shortening the equivalent channel length and thus lowering the threshold voltage (Vt). The decrease in Vt is due to the penetration of the channel by the high drain electric field at high drain voltages, thus reducing the barrier height of the channel carriers (Figure 2.3) [55]. As a result, the injected carriers from the source to the channel increase significantly and lead to undesirable off-leakage currents. This threshold voltage effect is negligible for long-channel devices. To improve gate control of an increasingly shorter channels, the semiconductor industry has migrated from single-gate planar transistor structures to 3D transistor structures with multiple gates to enhance short-channel control.

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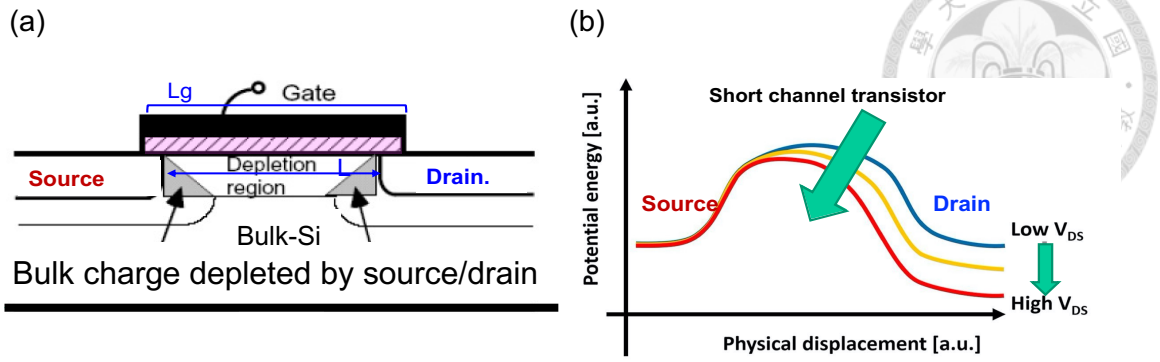

Figure 2.3 Illustration of drain-induced-barrier-lowering (DIBL) [55]

Innovations in transistor architectures, such as FinFETs and gate-all-around (GAA) nanosheet FETs, can reduce the DIBL effect due to a higher level of gate control over the channel. This control comes from the fact that the potentially depleted region is bounded by the fin itself and does not extend into the body. FinFETs or GAA FETs are based on gates surrounding the transistors' source/drain and body regions (diffusions). Instead of just penetrating from the top like a planar gate, the channel can fully be depleted because the electric field is in all directions, including the top and sides of a FinFET or all around the GAA. This allows for better current control and maximizes channel controllability. The result is high power efficiency. The difference between FinFETs and GAA FETS transistor structures is shown in Figure 2.4 [53, 54].

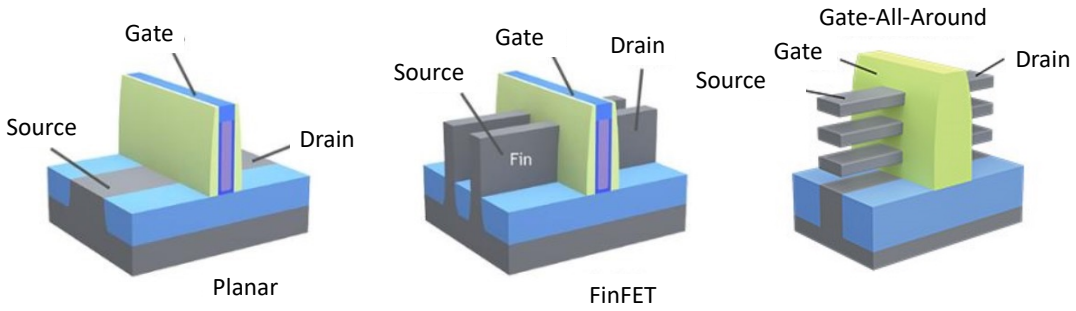

Figure 2.4 FinFET vs gate-all-around (GAA) nano-sheet transistor [53, 54].

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2.3 3D FinFET and Nano-Sheet-Transistor structures

In a FinFET structure, the channel between the source and drain is fin-shaped. Compared to planar transistors, the gates are in contact with the fins on both sides and on the upper side, respectively, thus providing better control over the channel formed within the fins, so FinFETs greatly help with current leakage [56]-[58]. Since then, FinFET fin heights have increased to achieve higher device drive currents in the same footprint. This is significantly different from today's designs, where the gate stack is placed directly over the channel region. A larger area must be occupied in the planar structure to amplify the drive current through the gate width.

However, the increase in the height of the fin makes the formation of the source-drain junction impossible [59]-[61]. Due to the shadowing effect caused by the narrow Gate-to-Gate and Fin-to-Fin spacing, the directly radiated ions can only radiate orthogonally from a zero-degree angle. However, a fin height of about 50 nm cannot be achieved by ion implantation alone because the lateral ion distribution will be too large, and the ratio of the vertical to the lateral depth of ions is about two to one, resulting in a short channel problem [59], [62]- [64]. Section 2.4 will review and discuss the shadowing effect [59]-[61] of oblique ion implantation in 3D transistor structures.

The FinFET roadmap appears to be running out of steam as scaling technology is pushed beyond 3nm [66]-[68]. The widely adopted technology beyond FinFETs will be stacked nanosheet gates all around transistors. The gate all around or GAA transistor is an improved transistor structure where the gate contacts the channel from top & bottom, left, and right in four directions for a more aggressive transistor scaling application [69]-[73]. Such transistors are called gate-all-around nano-sheet-transistor field-effect

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transistors (GAA NS FETS), and different variants of structures have been proposed [74, 75].

Early developments in GAA devices employed vertically stacked nanosheets. The number of nanosheets depends on the transistor application. Power-saving applications typically require only two sheets, while high-speed applications require three to four sheets. They consist of individual horizontal sheets surrounded by gate material on all sides. It achieves better-improved channel control than the tri-gate control of FinFETs. While FinFETs require multiple fins side-by-side to achieve net higher currents, the current-carrying capacity of GAA transistors is increased by stacking multiple nanosheets vertically, with the gate material wrapped around the channel. The CD width and thickness of the nanosheets can be flexibly adjusted and scaled according to the desired electrical properties of the selected components [76, 77]. However, as with fins, sheet widths and pitches will continue to shrink as technology evolves and our ability to print finer feature sizes continues to improve. At extreme scale conditions, the sheets may be about the same width as they are thick, in which case their structures would resemble nanowires.

It is worth noting that nanosheets may be conceptually simple in structure, but they pose great challenges to conventional CMOS fabrication processes [75, 78]. GAA nano sheet fabrication begins with the deposition of periodic superlattice SiGe/Si layers. Depending on the number of silicon sheets required, for example, three sheets require three periodically stacked SiGe/Si to be patterned (Figure 2.5). Due to etch-induced patterning effects, different sheet CD thicknesses are often observed at the top and bottom and cause severe device variation problems. Nano sheets FET fin patterning techniques are very similar to FinFETs, except that the inner spacers must be recessed in the SiGe

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section before forming. The inner spacer CD is used to isolate the source-drain (S/D) from the gate, and it determines the overlap length between the gate and the S/D. Physically, it controls the source-drain extension dopant profile as well as the metal gate CD width. Electrically, it affects the series resistance and short-channel control performance because CD couples to the metal gate CD. That is, internal spacers play a very central role in nanosheet fabrication. Other processes, such as S/D epitaxy, also face challenges of the ground area is getting smaller, which the epitaxy often is smaller and affects the S/D conductivity.

After FinFET, GAA transistors possibly evolve into nanowires [79,80]. According to the currently available roadmap, these GAA-like structures will continue to be used in entire 3D transistor technology nodes. Transistor structures have undergone a long evolution from early planar structures to FinFET, GAA nanosheets. Those researchers who pioneered transistor innovations in the early days will be thrilled and honored with the impact they brought to the evolution of semiconductor manufacturing and deepening human civilization. People look forward to seeing what new end applications and capabilities will come with gate-all-around transistors.

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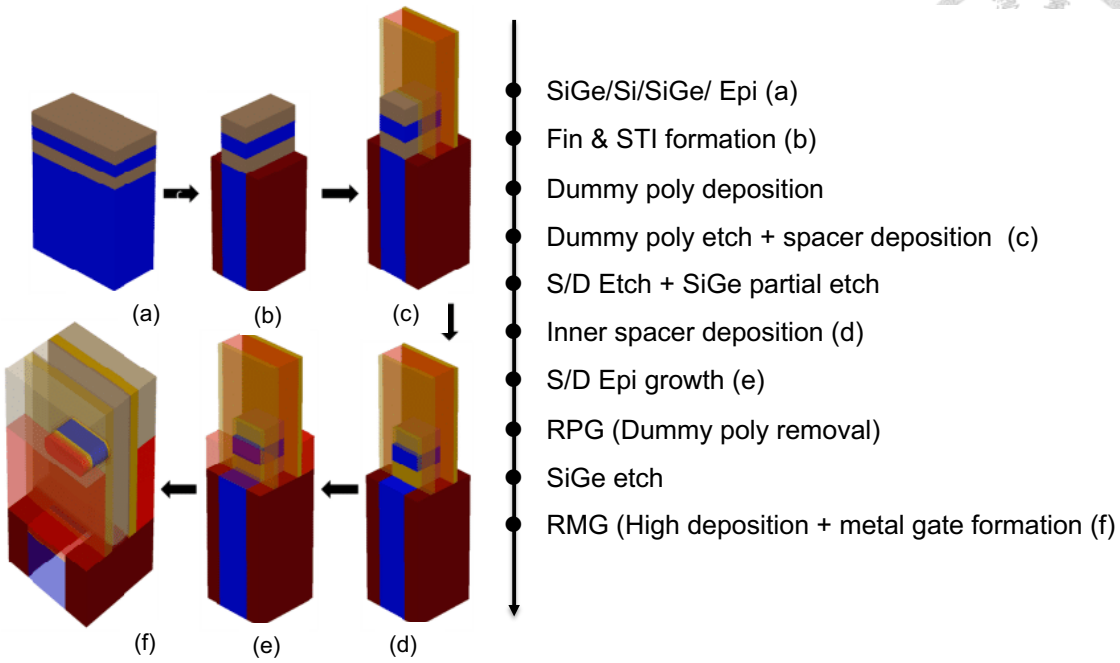

Figure 2.5 NSFET process flow. (a) to (b) periodic Si/SiGe superlattice deposition and fin patterning, (c) to (e) polysilicon deposition and patterning followed by internal spacer etch and formation, (e) source-drain epitaxy formation, (f) Deposition of high-k dielectric and metal gate after etch process to remove polysilicon dummy gate. [75, 78].

In addition to GAA nanosheets, transistor structures such as GAA forksheet and more advanced complementary field effect transistor (CFET) architectures have been developed in recent years. As shown in Figure 2.6, the Imec roadmap showcases more than a decade of continuous logic expansion based on innovations in new transistor structures. At the N2 technology node, Imec demonstrated the transition to Gate-All-Around (GAA) nanosheets. Samsung is introducing GAA nanosheets for its 3nm node, and Intel and TSMC announced GAA nanosheets for 2nm (Intel 20A). After two generations of nanosheets, Imec transitioned to Forksheet. Fork sheets are a variant of nanosheets that reduce the orbital height of the battery. Two generations after Forksheet, Imec introduced CFETs. Intel and TSMC also have a lot of forward-looking evaluation

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work going on with CFETs.

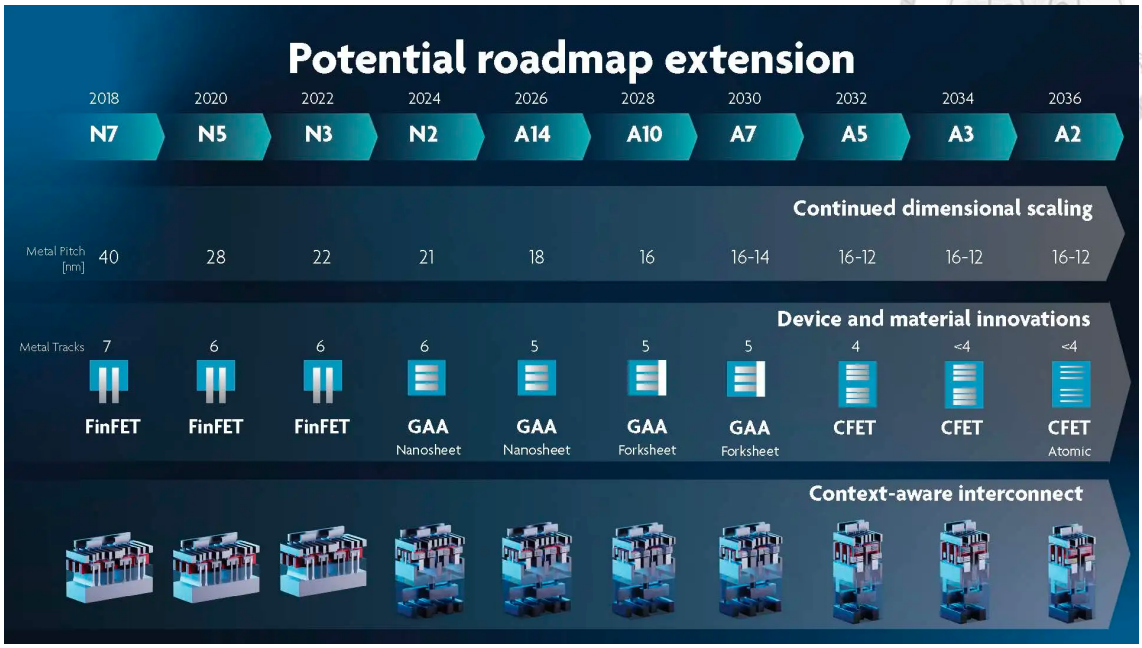

Figure 2.6 IMEC CMOS scaling technology roadmap presented by IMEC CEO Luc Van den hove at Marriott Marquee's technology forum (2022)

2.4 Challenge of junction formation in 3D structure devices

The 3D nature of FinFET and GAA transistor structures all present a unique set of manufacturing issues that can make yielding these devices challenging. This is especially true for extension implants that are in place before the formation of the nitride spacer, as shown in Figure 2.7(a), (b) [81,82]. In planar devices, extension implants are achieved by implanting dopants on both sides of the gate electrode at a 90-degree angle to the silicon surface (see Figure 2.7(a)). However, since the Fin channel in a FinFET device is perpendicular to the silicon surface, this methodology is not an option to avoid lateral over-diffusion. Instead, an angled implant is used, usually at a steep angle to the top and sides of the fin, as shown in Figure 2.5(b), 2.5(c). The problem with extension at such a steep angle is that a large percentage of the dopant is not retained on the fin but bounces

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off. The relationship between the extended implant angle and the dopant remaining on the sidewalls is shown in Figure 2.5(d). As shown in this figure, the steeper the implant angle, the less dopant remains on the sidewalls of the fin.

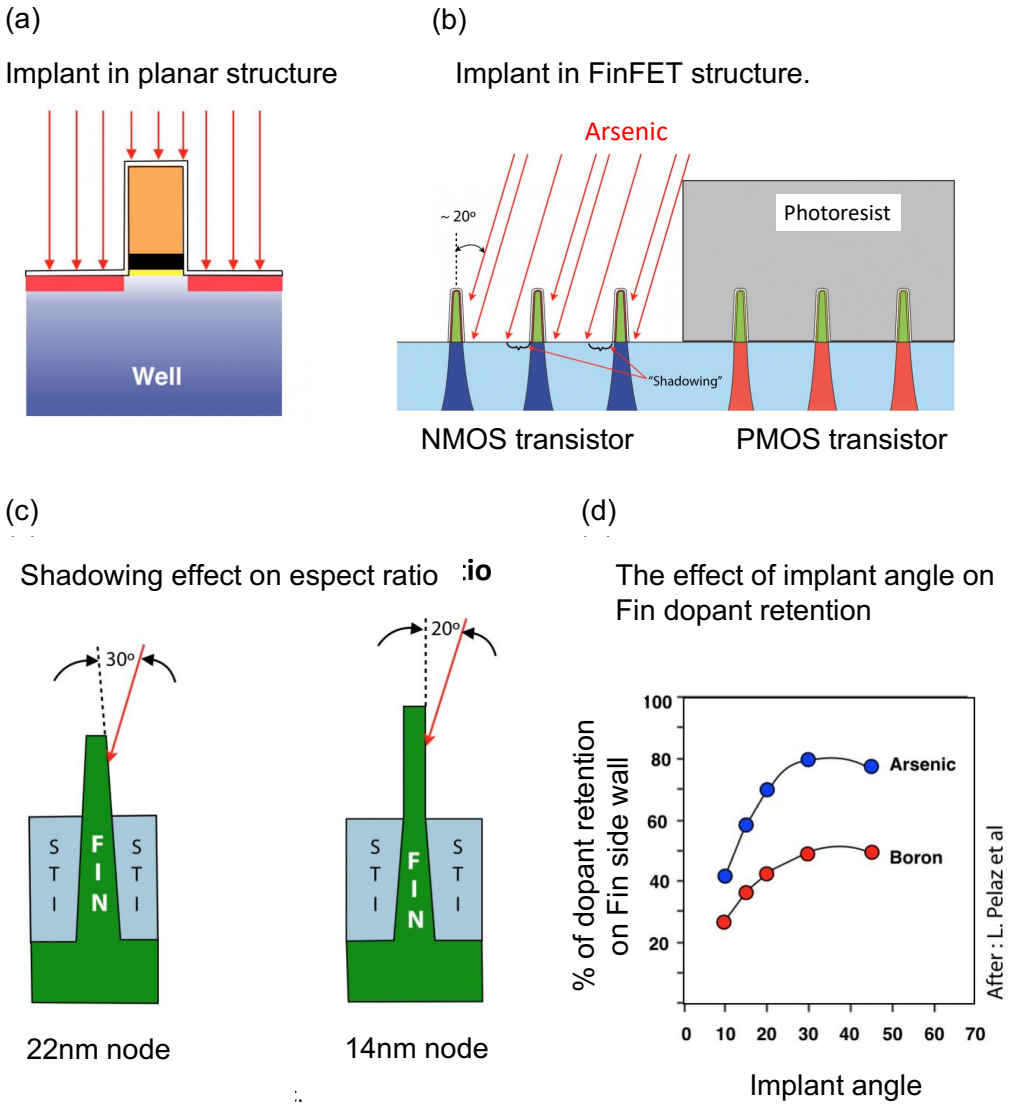

Figure 2.7 Ion implant shadowing effect (a) conventional extended ion implantation in planar transistor structure, (b) angled ion implantation in FinFET structure due to shadowing effect of 3D fin structure and additional photoresist height, (c) the shadowing effect on the shape of the fin and the aspect ratio of the trench, (d) The effect of implantation angle on fin dopant retention [81, 82].

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The shadowing problem can still be overcome by force in early FinFET architectures. This is because the fins were sloped and the fin-to-fin and gate-to-gate pitch was large enough, which increased the incidence angle of the implant and allowed more dopants to remain on the sidewalls of the fins. However, at nodes after 10nm, the fins are tall and vertical, the fin-fin-gate spacing is smaller, and the traditional conformal Fin implantation method is no longer used. Ion implantation is used primarily for source-drain surface contact implantation, a high surface dopant for contact silicidation. Only zero-degree tilt angle implants are required for these applications [83, 84]. Due to the high doping concentration of the contact surface, the Schottky barrier height between the metal and the doped silicon can be lowered, thereby reducing the contact resistance.

Because of this fundamental implant shadowing problem starting from the 16nm technology node, the formation process of the source-drain junction has been changed from traditional ion implantation to recessed source-drain followed by in-situ doped epitaxial source-drain. The epitaxial source-drain process solves the problem of doping abrupt and shadow effects, and the application has been expanded to all FinFET technology nodes. After the 3nm node, one will still see epitaxial source-drain processes continue to be used for nanosheet transistor nodes with shared source-drain structures and multi-channel architectures. Below I discuss the use of epitaxial source-drain in advanced 3D transistor structures.

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Chapter 3 Selective Epitaxial Si:P Source-Drain Formation in 3D CMOS Transistor Structures

This chapter will consider the design required for NMOS epitaxial S/D in transistor performance improvement. This would include stressor and highly conductive epitaxial source-drain formation, with highly doped epitaxial Si:P being our choice. Next, the recessed source-drain process required prior to selective epitaxial deposition is described. Then the selective epitaxial Si:P growth method is introduced , mainly including cyclic deposition etching (CDE) and co-flow deposition and etching gas selective epitaxial growth (SEG). Finally, this work will demonstrate dopant-activation annealing with microwave-selective dopant activation versus state-of-the-art millisecond annealing and discuss their present differences. It is demonstrated that the dopant stability of microwave annealed samples shows significantly more stable results than millisecond annealing. In subsequent chapters, the underlying physical mechanisms for the stability of microwave annealed samples are discussed step-by-step.

3.1 The design consideration of epitaxial S/D for NMOS

CVD epitaxy has been used in semiconductor manufacturing for decades to create the perfect crystalline substrate layer upon which to build semiconductor devices [85, 86]. However, since the 40nm technology node, CVD epitaxy has been further applied, such as CVD epitaxy SiGe with in-situ doping of boron [87]-[89]. It not only creates a conductive source layer but also create a stressor layer at the source-drain at the same

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time. This innovative process technology provides advanced CMOS transistors with junctions with excellent doping abruptness, providing excellent short-channel control. In addition, by exploiting the lattice mismatch of Si and Ge, controlling the Ge% in Si can provide compressive stress to the transistor channel [87, 88], thereby significantly improving carrier mobility. This dominant PMOS boron-doped source-drain stressor design continues to be used in the latest technology nodes. Similar doped stressor concepts from the 20nm technology node have been extended to NMOS applications. Initially, the material was CVD epitaxial Si:P [89, 90]. However, its material properties differ from epitaxial Si:Ge:B. For example, the lattice mismatch between Si and P is relatively small, so even if the donor P concentration is as high as 4 x 10^{21} at./cm^3, the strain induced by Si:P on the channel is less pronounced [91, 92].

Furthermore, at high P concentrations (>1 x 10^{21}/cm^3), it begins to exhibit the typical donor deactivation problem [93, 94], which limits the activated P to 2 x 10^{20} at./cm3 at most regardless of the increase in the chemical concentration of P. Nevertheless, this dual epitaxial S/D design has played a key role in enabling advanced CMOS device performance improvements over the past decade. It will continue to be used in current and upcoming technology nodes. This section focuses on the design consideration of epitaxial S/D for NMOS.

Strained silicon technology has been a key technology in maintaining the momentum of semiconductor scaling. Implementing embedded source-drain stressors increases overall transistor performance by stressing the channel and thereby increasing channel mobility [95, 96]. This, in turn, results in a reduction in channel resistance. Although effective strain enhancement techniques can greatly enhance the performance of pMOS devices, nMOS transistor performance is difficult to improve by similar methods due to

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limited material properties. Such as high-strain compressive contact etch stop layers (CESL) or by embedding epitaxial Si1-xGex layers in the S/D regions of the device [97]-[99]

This is because it is very difficult to obtain an effective stress liner with intrinsic tensile stresses above 2GPa. Furthermore, it turns out that the realization of Si:C stressors in the S/D region of nMOS transistors is very challenging, as the epitaxial growth of Si:C realized is rarely documented in the literature [100]-[103]. Alternative methods such as carbon implantation and annealing techniques to form Si:C layers are rare [104, 105]. One of the main difficulties with Si:C stressor S/D formation is that only a very limited amount of alternative carbon (1.2%) can be put into these epitaxial Si lattices before C precipitation is observed. Therefore, the stressor cannot be obtained because the desired lattice mismatch is insufficient. Furthermore, in-situ co-doping of n-type dopant and C in epitaxial silicon processes to achieve high conductivity stressor source-drain is challenging because C and P compete to remain in the same lattice location during epitaxial processes. Thus, epitaxial NMOS Si:C:P or Si:P S/D still cannot achieve similar SiGe strain engineering to improve channel resistance. Unless channel strain can be better achieved through changes in transistor structure, such as gate-ring nanosheet transistor [106, 107].

Due to the lack of stress required for channel strain engineering, epitaxial source-drain improvements to overall transistor performance will have to consider series resistive elements involving source-drain extension dopant profiles, source-drain body resistance, and metal silicide/source-drain contacts resistance. The series resistance component of the device using the epitaxial S/D must be similar or even lower compared to the non-epitaxial device. Assuming that the device fabrication process flow for the epitaxial S/D

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and non-epitaxial reference devices are similar (except for the source-drain modules), the potential difference in the series resistance may arise from the source-drain sheet resistance, silicide, and contact resistance. Therefore, careful optimization of the Si:P epitaxy process, appropriate layer stacks for dopant profile control, and high in-situ P doping levels are critical for successfully integrating Si:P source-drain. The success criteria are that the epitaxial Si:P is implemented to ensure the source-drain extension dopant profile remains diffusion-free for short channel control requirements. The net dopant activation after annealing is significantly better than the as-deposited epitaxial film, and the contact resistance can benefit from heavily doped Si:P and reduce significantly.

Additionally, the epitaxial process must exhibit perfect selectivity to ensure that the Si:P growth was only ideally located in the desired recessed source-drain regions. Next, the details of the process to achieve selective epitaxy are described, including groove and epitaxy processes. Details of the Si:P epitaxy process used for this work and the prospect of different process options were presented in detail. These included different methods to obtain selectivity (co-flow versus cyclic deposition/etch), different precursors for silicon, carbon and phosphorus source gases, and different etch source gases. The material characterization data and the correlation between the electrical and material properties of the Si:P layer were discussed.

3.2 Recessed source-drain

In a planar transistor structure, the source-drain vertical region is defined by the dopant profile created by ion implantation and post-implantation annealing. The dopant

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profile is mainly controlled by the ion implantation energy, dose, and annealing thermal budget for dopant activation. For highly scaled 3D FinFET and NSFET transistor structures, the source-drain regions (Figure 3.1, Figure 3.2) are defined as three critical dimensions. It includes the spacing between parallel polysilicon gates that determine the S/D length, and the fin width that affects the final lateral extent of the epitaxy /D. In contrast, the S/D recess defines the S/D depth (see Figure 3.1(a)) [108, 109]. In addition to these three key dimensions affecting S/D volume, other key metrics, such as proximity to the gate edge, *i.e.* gate-to-source-drain overlap control, are decisive factors affecting the trade-off between SCE control of Ion-enhanced performance of transistors and devices. It is worth noting that in nanosheet transistors, the S/D recess depth should consider not only the volume size but also the leakage caused by parasitic planar transistors located under the nanosheet transistors (see Fig. 3.2(b), (c)). Proper isolation between the S/D and channel of the parasitic planar transistor will help reduce leakage [110, 111].

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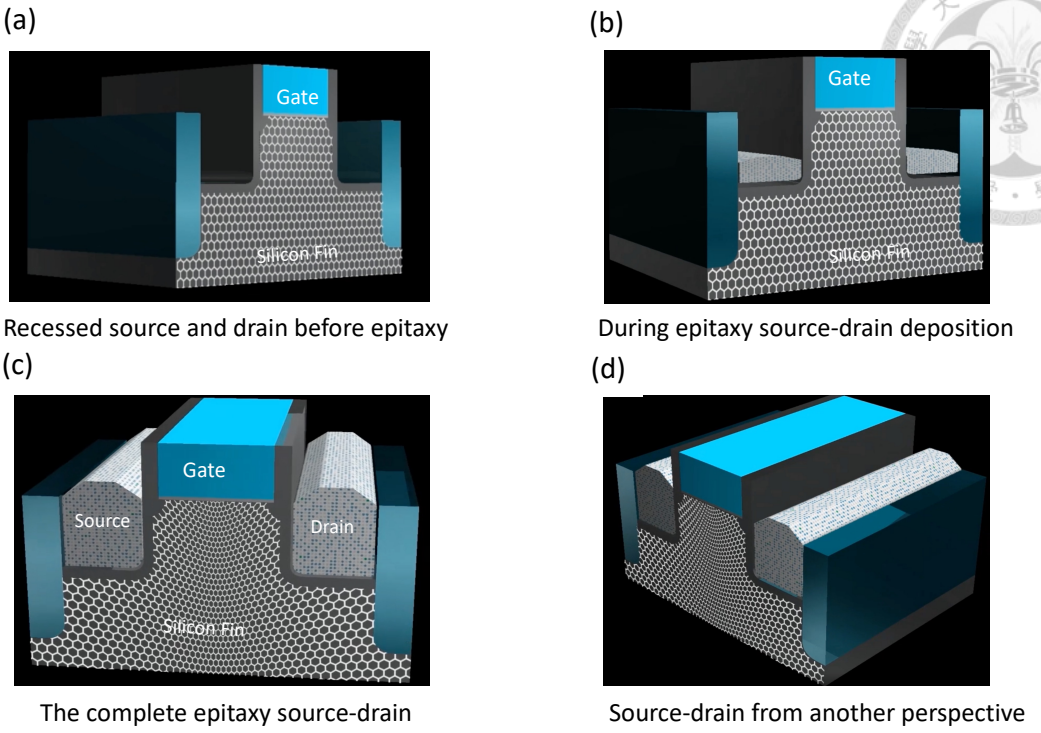

Figure 3.1 Recess and epitaxial source-drain process sequence in a cross-sectional view along the channel. (a) Recessed fin in the source-drain region, (b) Epitaxial source-drain during growth, (c) and (d) Full epitaxial source-drain after process operation in different views [112].

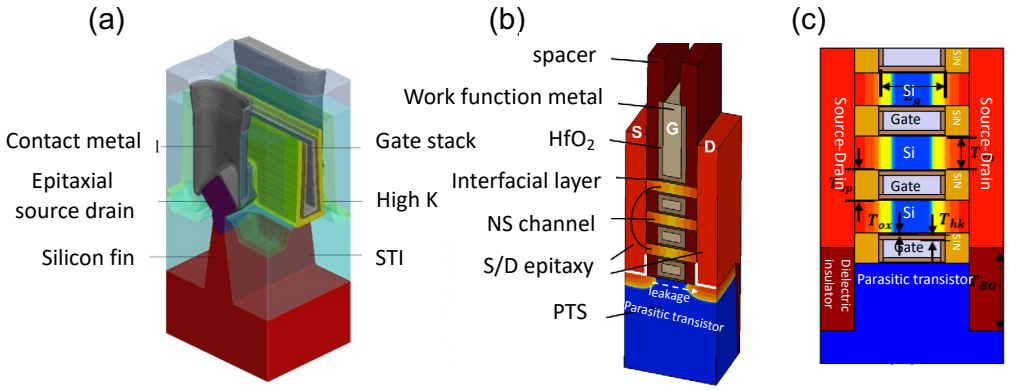

Figure 3.2 (a) source-drain epitaxy formed by recessed fins in a FinFET structure, (b) source-drain epitaxy shared by three nanosheet channels in a nanosheet transistor structure, (c) NSFET source-drain with dielectric insulator at the bottom to prevent leakage of parasitic transistors [113].

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3.3 Selective epitaxial Si:P growth

As CMOS scaling transitions from 2D to 3D transistors, such as FinFET and Nano-Sheet-Transistor, shrinking transistor source/drain (S/D) contact area can reduce S/D parasitic resistance more challenging because the parasitic resistance becomes comparable (or even higher) to the channel resistance itself. The heavier phosphorus in-situ doped silicon epitaxial film on the S/D region is critical to provide abrupt junctions to control short-channel effects and reduce parasitic resistance in nMOSFET transistors [114]-[116]. In addition to low S/D contact resistance, heavily doped Si:P can induce tensile strain in the channel to enhance electron channel mobility in 3D nMOSFET transistors. In-situ doped Si:P epitaxy processes are known to provide high tensile strain in the channel because the lattice constant of the Si:P lattice structure is slightly smaller than that of pure silicon. Substitution of higher phosphorus concentrations above 6% at lattice sites results in higher tensile strain and electron mobility. Considering series resistance and mobility requirements, the phosphorus concentration in selective Si:P films is typically higher than 2 × 1021 at/cc. In our work, selective Si:P epitaxial thin film growth was used for high phosphorus concentration (3×10^{21} at/cc) and high tensile strain (equivalent to ~1.9 at% Csub in Si:CP).

After the source-drain recess process in CMOS structures, the exposed transistor structure includes Si material and other dielectric layers, such as SiN as gate sidewall spacers and SiO2 as silicon trench isolation. Since only the source and drain Si regions are required for Si:P deposition, the Si:P epitaxy process is a selective deposition that only deposits on the source and drain Silicon regions. This selective epitaxial SI:P deposition was performed on an Applied Materials Centura® RP Epi system (Figure 3.3) [117] using disilane (Si_2H_6) dichlorosilane (DCS, SiH_2Cl_2), phosphine (PH_3), and

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hydrochloride (HCl) gases.

The AMAT Epi Centura chamber is bounded by upper, and lower clear quartz domes (light grey) clamped to a metal base plate due to the compression seal of the metal ring (dark grey). Therefore, the tightness of the chamber is ensured, and the vacuum degree of the cavity can reach the base pressure in the mTorr range and the leakage rate of several tens of mTorr/min. The wafers were placed horizontally on a SiC-coated graphite plate and spun at 30 rpm during growth to improve thickness uniformity. The reactive gaseous precursors are transported in laminar flow (arrows) through a quartz insert above the wafer surface. Their thermal decomposition was achieved using two sets of 20 kW lamps. Among the reaction gas, disilane and dichlorosilane provide Si sources. PH3 gas offers phosphorus donors in the epitaxial Si:P layer. Co-flow HCL gas as etches gas is for selective deposition purposes. The epitaxial growth temperature and pressure are at 650 °C and 300 mTorr, respectively.

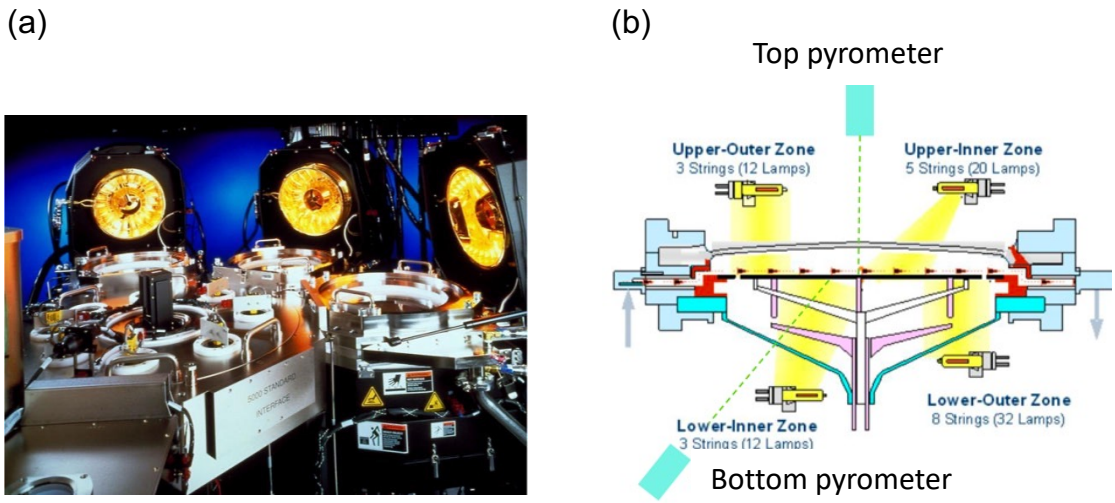

Figure 3.3 AMAT Epi xP Centura epitaxy (a) system and (b) process chambers [117].

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3.4 Epitaxial Si:P sample preparation

In Sections 3.5 and 3.4, a portion of text and graphics have been previously published in [120], the reprint permission can be found in appendix . A 300 mm p-type silicon wafer with a resistivity of 8-12 Ωcm was sent to a reduced pressure chemical vapor deposition (CVD) chamber to grow 30 nm thick, lightly doped (2 x 10^{20} at./cm^3), and heavily doped (3 x 10^{21} at./cm^3) epitaxial Si:P films. The CVD Si:P deposition process uses hydrochloric acid (HCL), dichlorosilane (DCS), and phosphine (PH_3) as precursors for chemical reactions. The CVD epitaxial process is performed at a temperature and pressure of 650 °C and 300 mTorr, respectively [3]. The epitaxial growth rate of epitaxial Si:P on bare Si is slow, about 70 nm/hr. Rapid thermal annealing (RTA) for dopant activation and dopant stability testing can be run from 600 – 950 °C (Helios® _XP RTP, Mattson Technology). MSA performed in milliseconds at 1150 °C (flash lamp annealing, DNS LA-3000F) was used as a competitive reference for the MWA process. For the MWA process at DSG, the cavity susceptor setup was configured with different impurity-doped susceptors and performed with various microwave power 12 kW, 14 kW, and 15 kW. The microwave annealing process time was 110 s - 300 s..

3.5 Dopant activation annealing

For heavily doped epitaxial Si:P, the P concentration is as high as 3 x 10^{21} at./cm^3, the activated dopant stays at 2 x 10^{20} at./cm^3 and does not increase with the P chemical concentration. Therefore, post epitaxial Si:P dopant activation annealing is required. To address the donor stability issues associated with millisecond annealing, in addition to millisecond annealing, I also tried another microwave annealing as an experimental control. It was observed that in our susceptor design, microwave power setting and the sample configuration in the susceptor are critical to find efficient dopant activation results.

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Among the samples used, efficient dopant activation at temperatures below 700°C can only be achieved by finding the optimal microwave annealing (MWA) cavity settings and choosing the optimal distance for the small spacing between the susceptors. In this section, only the preliminary results of our findings are presented. The exact mechanism of microwave-sample-sensor interaction is described in detail in later sections.This work demonstrated that MWA can produce MSA-like activation at temperatures below 700 °C under optimal receptor configuration. To study the evolution of dopant activation of Si:P samples before and after annealing, Sheet resistance was measured by four-point probe and doped carrier concentration by Hall effect measurement (Hall 8800, Swin). The atomic distribution was characterized by high-resolution secondary ion mass spectrometry (SIMS) (Physical Electronics ADEPT-1010).

The goal of source-drain junction engineering for advanced transistor structures such as sub-3 nm gate-all-around (GAA) FET technology nodes is to achieve the lowest possible sheet resistance R_{sh} and the shallowest possible junction depth X_j. Earlier studies of MWA for dopant activation have yielded R_sh-X_j results comparable to the isothermal rapid thermal annealing (RTA) process [118]. However, MWA is still essentially a bulk heating and a long thermal-based annealing process (>100 s), so the realized R_{sh}-X_j is limited by the thermal budget and cannot match the state-of-the-art millisecond annealing process [119]. To overcome this thermal budget limitation, this work aims to achieve dopant activation through possible direct energy coupling with inactive dopant structures at temperatures below 700 °C. This initial study experimented with various susceptor setups in the cavity to achieve this goal. Figure 3.4(a) shows the optimal three-parallel pedestal setup in the MWA chamber, including the sample holder and susceptor holder. The susceptor consists of a doped silicon substrate coated with a silicon carbide layer.

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During MWA, the temperature of the susceptors rises to the target range, so the susceptors essentially become metallic and act as shunt capacitors, with each susceptor being controlled at a specific spacing of 5 mm from the sample. This configuration results in a uniform electric field perpendicular to the target sample surface. In contrast, in a conventional setup without this susceptor configuration, the electromagnetic fields of microwaves are expected to be randomly oriented. The triple-parallel-susceptor configuration is critical to tune the area and sample temperature to reach the threshold, enabling efficient direct energy coupling for selective dopant activation. Figure 3.4(b) shows the resistivity as a function of annealing duration [120]. The resistivity of the as-deposited Si:P is 0.35 mΩ-cm (black symbols), It decreases monotonically with increasing processing time at a constant MWA power of 14 kW. At the same time, the substrate temperature is maintained at 680 °C (by pyrometer) . Resistivity as low as 0.16 mΩ-cm (blue symbols) was obtained after 300 s in MWA. The Rsh trend of Si:P in TPS-MWA process is very different from that in RTA annealing. Using an RTA process (red circles in Fig. 3.4(a)), its thermal budget can equivalent to MWA at the same substrate temperature. The resistivity increases monotonically with time. It indicates dopant deactivation. This suggests that the dopant activation achieved in the MWA process is not due to purely thermal effects. Furthermore, TPS-MWA-treated Si:P samples may be thermally stable.

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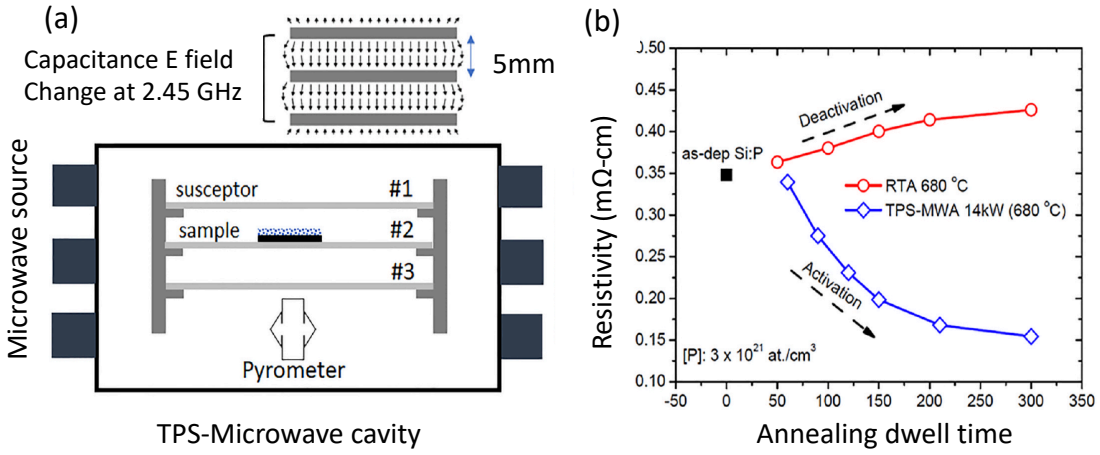

Figure 3.4 (a) Susceptor setup in a microwave cavity using a triple-susceptor (TPS) configuration where the sample is placed on the middle susceptor with a controlled spacing 5 mm. The inset depicted the E-field distribution between susceptor plates. (b) The resistivity of Si:P was measured as a function of the annealing time at 680 °C at RTA and MWA at 14 kW [120].

Although high-temperature millisecond thermal annealing has traditionally been employed to increase the level of dopant activation in heavily n-doped Si. However, these activated dopants tend to be thermally unstable upon subsequent milder thermal treatments (600 - 700 °C) such as RTA. This unstable junction problem is especially pronounced at high doping concentrations. To better understand the effect of dopant concentration on the deactivation behavior, Figure 3.5(a) shows the evolution of the resistivity of Si:P during thermal annealing sequences with different phosphorus concentrations [120]. At lower [P] = 2×10^{20} at/cm^3, the resistivity remains unchanged before and after the thermal sequence, indicating relatively stable dopant incorporation into the Si lattice.

Conversely, at higher [P] > 5×10^{20} at/cm^3, the resistivity of Si:P first decreases after

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MSA annealing due to dopant activation. However, after the subsequent RTA treatment, the resistivity increased dramatically due to the deactivation of the dopant. The above observations suggest that although higher [P] Si:P exhibits a significantly reduced resistivity after MSA, the effect of donor deactivation may lead to a higher final resistivity after RTA. In other words, activated dopants in highly n-doped silicon are not thermally stable after millisecond annealing.

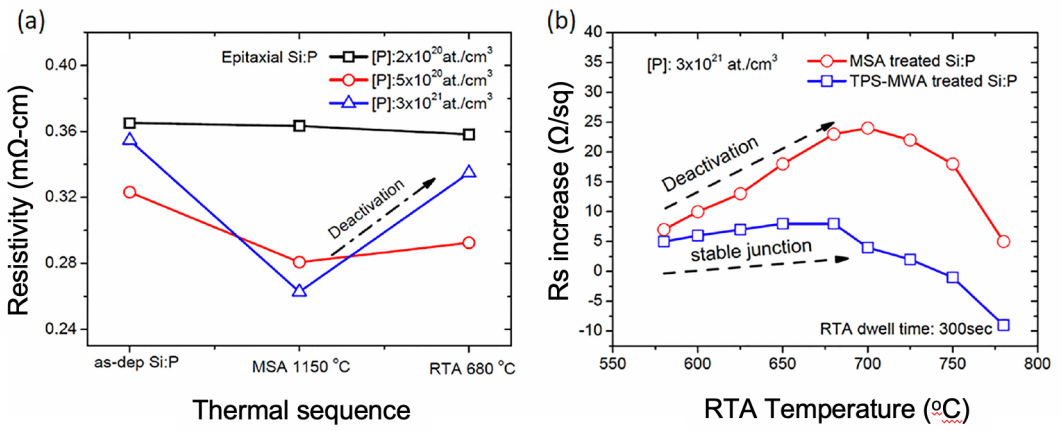

Figure 3.5 (a) Variation of resistivity of Si:P substrates with thermal annealing sequence at different phosphorus concentrations. (b) Sheet resistance (R_{sh}) increase of Si:P samples correlates with RTA annealing temperature for two different activation processes: TPS-MWA and MSA [120].

In order to verify the thermal stability benefits of MWA annealed samples, a thermal budget representative of semiconductor thermal processing must be selected for thermal stability testing. The option is that MWA annealed samples are placed at 600-780 °C for 300 seconds for thermal stability and deactivation testing. As shown in Figure 3.5(b), the samples after microwave annealing showed relatively small changes in Rsh in the RTA temperature range up to 700 °C. In contrast, the changes in Rsh for samples annealed after

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MSA increased with increasing RTA temperature. It increases monotonically up to 700 °C and reaches the maximum Rsh value. The above observations suggest that TPS-MWA produces a more thermally stable junction, which is attributed to less dopant deactivation. Hall measurements were used to verify this effect to obtain the carrier concentration in these samples. As shown in Figure 3.6(a) [120], the Si:P samples subjected to MSA 1150 °C and RTA thermal cycling showed fewer carriers, or more pronounced donor deactivation, according to the sheet resistance behavior. In particular, the samples annealed by LTA at a higher temperature of 1225 °C showed significant donor deactivation (~78%), where the free carrier concentration decreased from supersaturation of 8.9×10^{20} to $1.9 \times \_10^{20}/cm^3$. In contrast, for the TPS-MWA annealed samples, the deactivation is only 5% at 4×10^{20} at./cm3, resulting in a much higher carrier concentration after post-heat treatment than the MSA and LTA counterparts.

One of the key metrics for Si:P annealing is dopant diffusion, which needs to be kept to a minimum to achieve a sharp box-like profile. ToF-SIMS analysis was used to study the doping profile after TPS-MWA, as shown in Figure 3.6(b) [120]. The results show that MSA and TPS-MWA have almost no diffused junction at a doping concentration of 2×10^{20} at./cm^3, increasing dopant activation rather than dopant diffusion. The phosphorus distribution of the TPS-MWA samples showed a less sharp transition than the MSA annealed samples at concentrations below 6 x 10^{19} at./cm^3. This slight dopant diffusion is thought to be due to the migration of mobile dopant-vacancy clusters (P_1V and P_2V) during the isothermal annealing at 680 °C under MWA [121, 122]. The above observations suggest that the available pathways for dopant deactivation in Si:P are different for MWA annealed samples compared to LSA and MSA.

The difference in the performance of MWA and MSA annealed samples in terms of

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thermal stability motivated our interest in investigating the physics behind the annealing mechanism. During MSA and LTA annealing, UV-Vis and NIR radiation from Xeon lamps and CO2 lasers are absorbed by the Si:P layer through the band gap and/or free carrier absorption, suggesting that this annealing is an inherently non-selective interaction effect. That is, the coupling between light energy and D_nV(n-1-4) is not particularly preferred for any D_nV configuration. Low-order P_nV defects are generated during thermal annealing of heavily doped Si:P by MSA or LTA. Larson et al. [122] showed that the annealing of vacancy-phosphorus pairs can form new defects associated with P_2V clusters. Ranki et al. [123] observed that although vacancies can be dissolved from P_nV at high temperatures, upon cooling, the vacancies are quenched into P_3V clusters during the cooling process.

It seems that much more is needed to know about the electronic properties of D_nV and how they relate to each other to understand the physics behind thermal stability. In the next chapter (Chapter 4), ab initio calculations will be used to calculate a complete D_nV electronic property, including formation energies, electron density maps, dipole moments, and local lattice vibrational modes. These electronic properties of D_nV will help to piece together the relationship between the kinetics of D_nV formation and D_nV thermodynamics and suggest why MWA and MSA exhibit different thermal stability.

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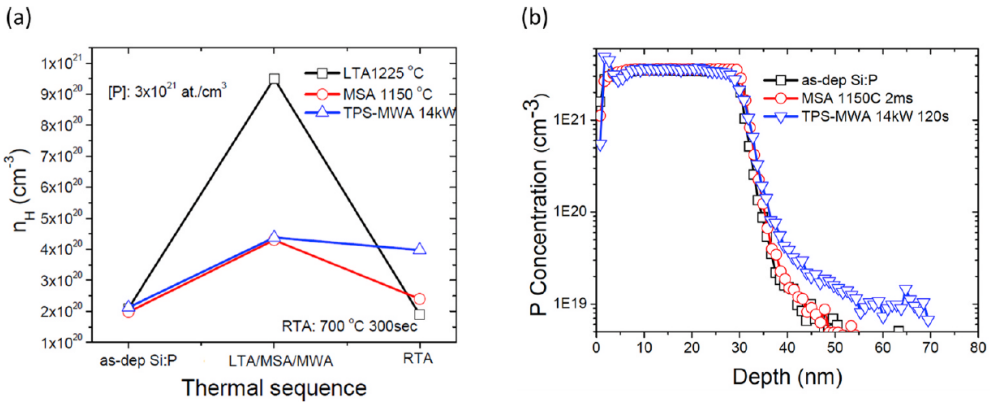

Figure 3.6 (a) Changes of free carrier concentration before and after heat treatment of heavily doped Si:P layer with P concentration of 3 x 10^{21}at./cm^3. (b) Phosphorus SIMS profiles in the epitaxial Si:P film after various annealing conditions [120].

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Chapter 4 Electronic properties of inactive dopant structures

The ab initio calculations presented in this chapter are based on collaborative work with Professor Lourdes Pelaz of the University of Valladolid. The simulation results used in this dissertation were done by Professor Lourdes. The text and figures have previously been published in [120] and [188] and reproduced in this dissertation under permission as shown in Appendix.

4.1 Ab Initio Calculations

For the ab initio simulations, Prof. Lourdes' team used the Vienna ab initio Simulation Package (VASP) [124, 125], using the projector augmented wave (PAW) method [126] and the PBE-PAW pseudopotential [127]. Defects were embedded in cubic supercells with 216 Si atoms. A Si atom was removed from the cell to create a vacancy (V) or replaced by P to include substitutional P atoms. Atom positions were relaxed using a conjugate gradient algorithm until the force acting on each atom was less 0.01 eV $Å^{-1}$. The volume of the cubic simulation cells was also modified so that the absolute value of the external pressure was lower than 0.05 kBar. Periodic boundary conditions were applied in the three spatial directions. This simulation used a 450 eV plane-wave kinetic energy cut off and a 4×4×4 Γ-centered Monkhorst-Pack k-point mess [128] to sample the Brillouin zone. Only neutral defects are considered in our calculations.

The simulation used the CHARGEMOL program [129]-[131] to evaluate the dipole moments of P_nV complexes from the electronic density distribution obtained in VASP. This program computes Density Derived Electrostatic and Chemical (DDEC) net atomic

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charges and atomic multipoles for periodic and non-periodic systems, which has been proven to describe many different systems [132, 133] properly.

The simulation work also evaluated the local vibrational modes (LVMs) and their frequencies of P_nV complexes as the eigenvectors and eigenvalues, respectively, of the Hessian matrix. Since this is a very demanding calculation, Professor Lourdes only displaced atoms up to a second neighbor distance from the vacancy (as LVMs are localized around the atoms of the complex). Atoms that were allowed to move in this calculation are those shown in Fig. 6. These calculations considered a convergence energy threshold of 10^{-8} eV for the electron step size in relaxation.

4.2 Energetic characterization

The simulation analyzed the atomic configurations schematically shown in Figure 4.1. They include the monovacancy (V) configuration and P_nV complexes with n=1 to 4, where P atoms are placed at neighboring lattice sites around the vacancy position. Professor Lourdes considered two different symmetry configurations for the vacancy: D2d symmetry (as it corresponds to the lower energy Si vacancy configuration for the neutral charge state [134]), and Td symmetry (as it corresponds to the Si vacancy configuration with a trapped positron [135]).

The formation energy of complexes shown in Figure 4.1 was calculated as indicated in Eqs. 1 and 2, where Ps refers to the substitutional P atom. Obtained energies are summarized in Table 4.1

$$E_{P_s}^{f} = E_T(cSi_{215}P_S) - E_T(cSi_{216}) \quad (1)$$

$$E_{P_nV}^{f} = E_T(P_nV) - \left\{\frac{215}{216}E_T(cSi_{216}) + nE_{P1}^{f}\right\} \quad (2)$$

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Formation energies of Table 4.1 agree with previous theoretical calculations [134], [136]-[138]. Better agreement is found when a similar simulation set up as the one used in the present work is employed [138]. At the same time, slight differences in energies arise when the simulation cell size is different (64 atoms c-Si simulation cells are used in Refs. [136,137]), or a different energy reference for evaluating the formation energy of complexes is employed [137]. Nevertheless, the large stability of P_4V is a common trend in the present and previous theoretical calculations.

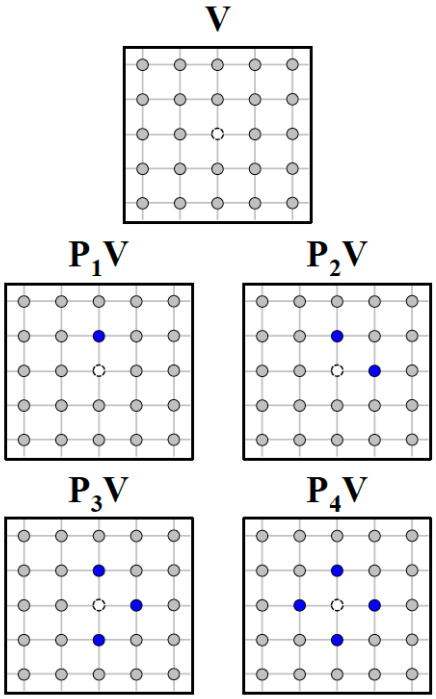

Figure 4.1 Schematic representation of the structures considered in *ab initio* calculations. Si atoms are represented with light grey circles, P atoms with dark gray (blue) circles, and vacancies with white circles [120].

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Defect	Formation energy
V (D_{2d})	3.63 eV
V (T_d)	3.87 eV
P_1V	2.52 eV
P_2V	1.00 eV
P_3V	0.10 eV
P_4V	-1.43 eV

Note: energies of the other P_n clusters shown in the report of full ab initio calculations can also be included

Table 4.1 D_nV Formation energy of studied complexes from Eq.(2) [120].

4.3 Electronic density distribution of P_nV clusters

The simulation work evaluated the electronic density distribution in the atomic configurations considered. The result represented in Figure 4.2 is the electronic density plots of valence electrons for the Si vacancy in D2d and Td symmetry configurations and c-Si for comparison. She chose an electronic density reference level of 0.036 $Å^{-3}$ (white color in figures) to separate regions with low electronic density (blue regions), from areas with high electronic density (red regions). Thus, visual inspection makes it easy to identify the electronic density plot of c-Si atomic positions. Dark blue dots correspond to core regions of atoms as only valence electrons. Light blue regions represent interstitial spaces, intense red regions represent atomic bonds. In addition, with this color scale light blue regions in c-Si (Figure 4.2(a)) match the maximum positron density regions (not shown) calculated in Ref. [134].

In the case of D2d vacancy configuration (Figure 4.2(b)), there are some atomic rearrangements of neighboring Si atoms. Dangling bonds surround the vacancy bonds in two pairs, which makes Si atoms move out of the plotted plane, and the corresponding dark blue dots do not appear in the representation. For the Td vacancy configuration (Figure 4.2(c)), Professor Lourdes superimposed the positron density (dashed contours,

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with a contour spacing of 0.01 Å-3) and the positions of neighboring Si atoms (black circles) calculated in Ref. [135]. As expected, the higher positron density is at the vacancy location, corresponding to an electron density of ~0.06 Å-3 in our calculations. Small differences in black circles and blue dots in Fig. 2.c (which indicate atomic positions) are due to the fact the positron interaction is considered to relax the vacancy structure in Ref. [135]. Thus, electronic density plots can be used to visualize empty spaces in the atomic structure (corresponding to low electronic density regions) where positrons can be trapped.

The electron density map for the valence electrons of the P_nV complex is shown in Figure 4.3. Since P atoms have 5 valence electrons, their location corresponds to the intense red regions indicated by black dashed circles in Figure 4.3. As in the case of the D2d vacancy configuration of Figure 4.2(c), there are some atomic rearrangements of dangling bonds around the vacancy in P_2V (Figure 4.3(b)), which makes Si atoms move out of the plotted plane and the corresponding dark blue dots do not appear in the representation. It can be seen from Figure 4.3 that there is a lower electronic density at the vacancy region as more P atoms are in the complex (bluer region at the surroundings of the vacancy position). To quantify this effect, the simulation work evaluated the average electronic density as a function of the distance to the initial vacancy position ((0,0) position in Figures. 4.2 and 4.3), which is represented in Figure 4.4 for the case of Td vacancy (as it is the vacancy configuration when a positron is trapped) and P_nV complexes. It can be seen from Figure 4.4 that there are lower electronic densities at the vacancy position as more P atoms are incorporated into the complex. In addition, the low electronic density region extends further for P_3V and P_4V complexes, indicating a larger open volume space for positron trapping as P components in P_nV complexes increase, which has been suggested to occur in Ge:P [139].

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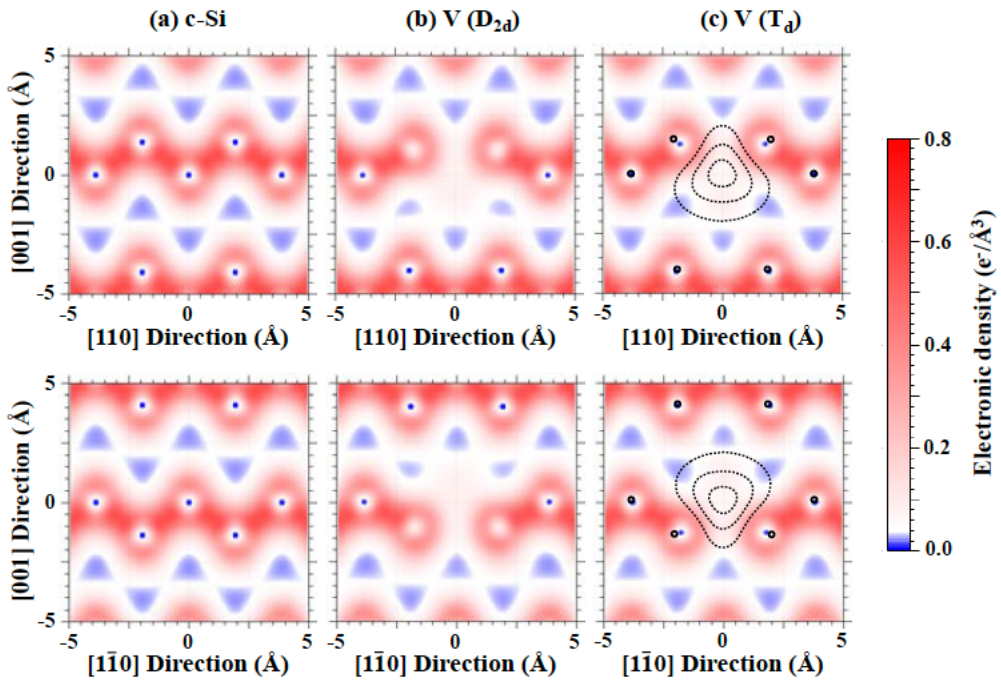

Figure 4.2 Electronic density plots of valence electrons for c-Si and the Si vacancy in D2d and Td symmetry. The origin of the graph is at the very center of the graph, corresponding to the position of the vacancy before the atomic configuration is relaxed. The dark blue dots correspond to the core regions of the atoms, the light blue regions represent the interstitial spaces of the structure, and the dark red regions are the atomic bonds. The black circles and dashed outlines in (c) represent atomic positions and positron density, respectively, taken from Ref. [120, 135]

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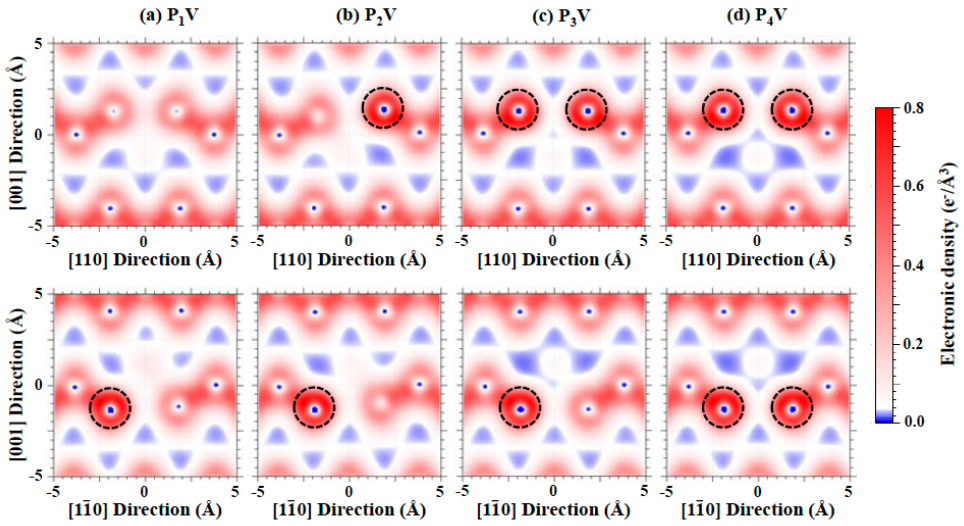

Figure 4.3 Electronic density plots of valence electrons for P_nV complexes. As in Fig. 1, the origin of plots is located at the center of the plot and corresponds to the position of the vacancy before relaxing the atomic configuration. The same color scale as in Fig. 1 is used. Black dashed circles indicate the location of P atoms [120].

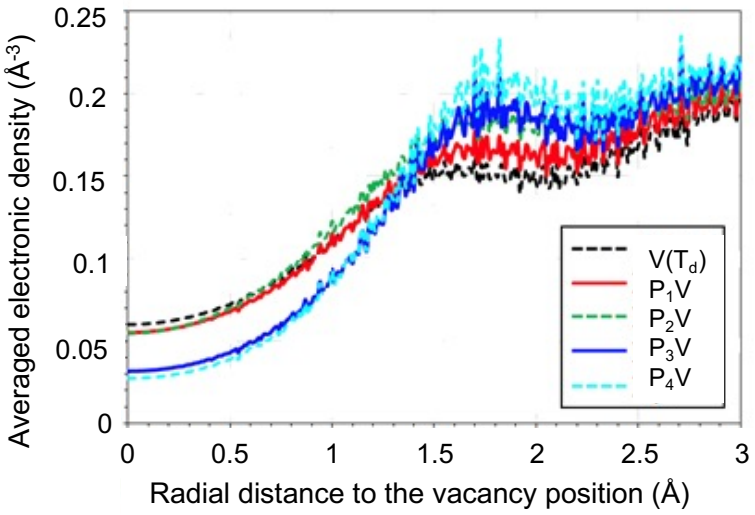

Figure 4.4 Averaged electronic density as a function of the vacancy position for T_d vacancy configuration and P_nV complexes [120].

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4.4 Dipole moment calculations

The net atomic charges within a simulated cell containing P_nV complexes are represented in Figure 4.5a. This analysis shows that P atoms have the larger positive charge values in the simulation cell (intense red atoms in Figure 4.5a), while first Si neighbors of P atoms have the larger negative charge values (intense blue atoms in Figure 4.5a). This charge distribution around P_nV complexes results in the net dipole moments whose magnitude are summarized in table 4.2, and whose orientation is represented in Figure 4.5b Due to the symmetry of the charge distribution in P_4V complex observed in Figure 4.5a its net dipole moment is negligible. This is not the case of the other P_nV complexes, where the dipole moment points in the direction of P atoms towards their first Si neighbors. This dipole moment can couple to external electric fields, which would induce charge oscillations that eventually would result in localized atomic movements in the vicinity of P_nV complexes with net dipole moment.

These electrical induced atomic movements might couple with the local vibrational modes (LVMs) of P_nV complexes by using an external electric field resonant with the LVMs.

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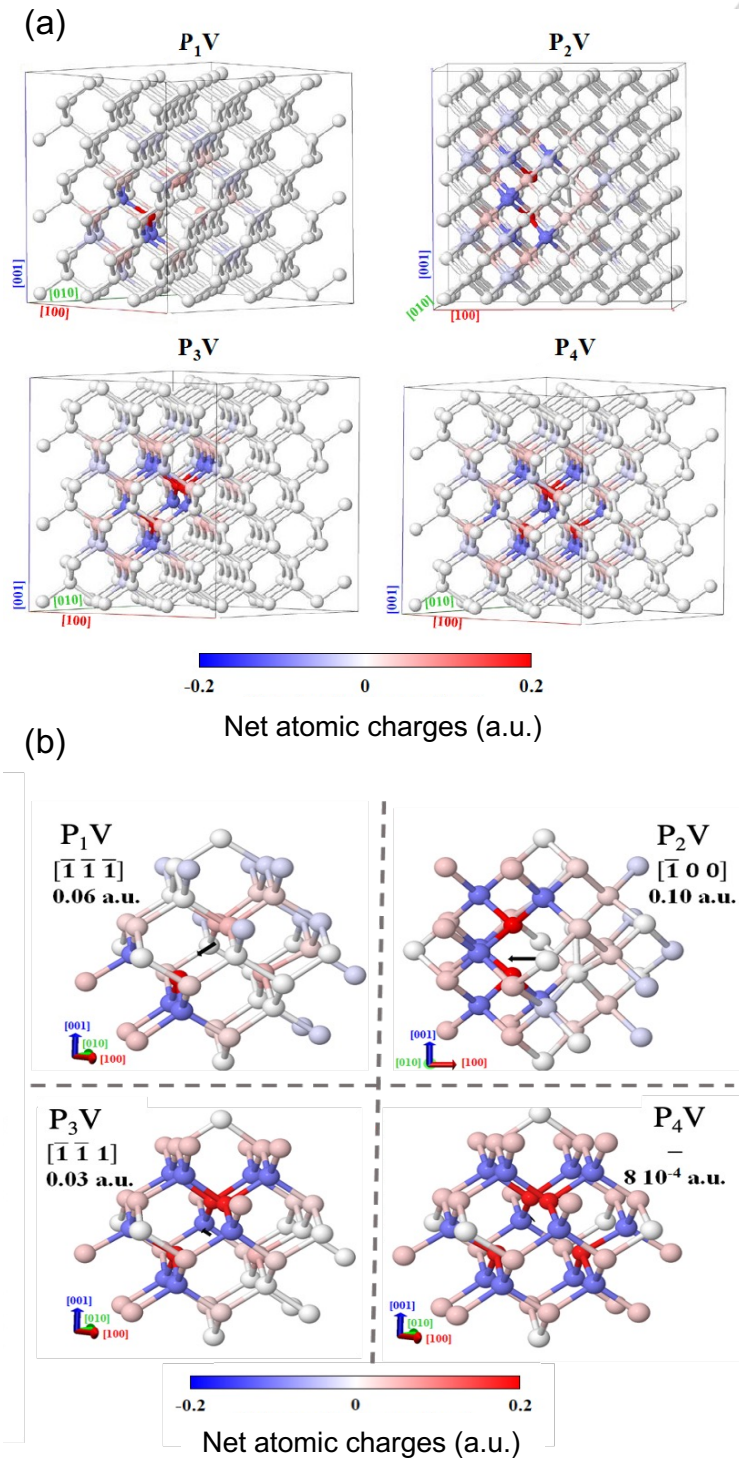

Figure 4.5 Net atomic charges in simulation cells containing the P_nV complexes obtained from the electronic density distribution using CHARGEMOL program [120].

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Defect	Net atomic dipole moment (a.u.)	Direction
P_1V	0.06	$[\bar{1}\,\bar{1}\,\bar{1}]$
P_2V	0.10	$[\bar{1}\,0\,0]$
P_3V	0.03	$[\bar{1}\,\bar{1}\,1]$
P_4V	$8\ 10^{-4}$	-

Table 4.2 Net atomic dipole moment of P_nV complexes evaluated from the electronic density distribution. Dipole moments are in atomic units (a.u.) [120].

4.5 Lattice vibrational mode calculations

To explore the possibility of microwave resonant coupled with lattice vibrational modes (LVMS), the frequencies of LVMS and its P_nV clusters were initially evaluated. Each computed LVM was characterized by a frequency (ω_{LVM}) and a displacement of atoms ($\overrightarrow{\Delta r_{LVM}^{l}}$) around their equilibrium position ($\vec{r}_l$). Among all the calculated LVMs, those whose atomic displacements are highly aligned with the direction of the net dipole moment are of interest. For this purpose, the projection of all atomic displacements of each LVM ($\overrightarrow{\Delta r_{LVM}^{l}}$) were added into the unit vector along the dipole moment direction ($\overrightarrow{u_d}$) as indicated in Equation (3)

$$A_{LVM} = \sum_l \left| \overrightarrow{\Delta r_{LVM}^{l}} . \overrightarrow{u_d} \right| \qquad (3)$$

Larger ALVM values indicate a higher degree of alignment between the dipole moment directions and those atomic displacements on the LVM under consideration. Among the highly aligned LVMs, LVMs were found to be present in all P_nV clusters (n = 1-3) in the frequency bins 5.5-5.75 THz and 10.6-10.8 THz (Table 4.3 and Fig. 4.6), which is consistent with their net dipole moments are aligned. Therefore, if these highly aligned LVMs can be excited, external electric fields with these frequencies will selectively more efficiently induce local atomic motions near the PnV clusters. A direct

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resonant interaction between the 2.45 GHz microwave and LVM (THz) is unlikely due to the huge order-of-magnitude difference in frequency. In other words, the dipole moment-microwave coupling can be considered as the main possible interaction in the MWA process. Therefore, this dissertation work believes there are athermal interactions other than local vibrational modes in the Si lattice to achieve dipole-resonant or efficient non-resonant coupling with microwaves. However, observing such low energy states in the silicon lattice structure is difficult because the energy spacing is too small to obtain discrete lines. A more detailed study of the properties of this resonant mode or the alternative athermal microwave effect [140]-[145] is beyond the scope of this paper. It is worthy of continued exploration by future researchers.

doi:10.6342/NTU202204032

P_1V	P_2V
1 f = 13.197074 THz;	1 f = 13.342765 THz;
2 f = 13.190843 THz;	2 f = 13.191411 THz;
3 f = 13.189412 THz;	3 f = 12.971731 THz;
4 f = 12.735586 THz;	4 f = 12.907728 THz;
5 f = 12.731886 THz;	5 f = 12.867239 THz;
6 f = 12.40679 THz;	6 f = 12.828067 THz;
7 f = 11.862156 THz;	7 f = 12.195928 THz;
8 f = 11.792124 THz;	8 f = 12.13864 THz;
9 f = 11.689315 THz;	9 f = 11.83076 THz;
10 f = 10.859752 THz;	10 f = 11.690865 THz;
11 f = 10.821686 THz;	11 f = 10.955534 THz;
12 f = 10.779073 THz;	12 f = 10.875088 THz;
13 f = 10.778354 THz;	13 f = 10.847102 THz;
14 f = 10.743765 THz;	14 f = 10.844571 THz;
15 f = 10.741868 THz;	15 f = 10.81337 THz;
16 f = 10.67022 THz;	16 f = 10.748639 THz;
17 f = 10.619467 THz;	17 f = 10.704287 THz;
18 f = 10.618016 THz;	18 f = 10.683311 THz;
19 f = 10.599809 THz;	19 f = 10.67464 THz;
20 f = 10.590963 THz;	20 f = 10.602302 THz;
21 f = 10.589535 THz;	21 f = 10.550182 THz;
22 f = 10.486026 THz;	22 f = 10.545948 THz;
23 f = 10.484757 THz;	23 f = 10.439943 THz;
24 f = 10.448567 THz;	24 f = 10.427589 THz;
25 f = 10.264237 THz;	25 f = 10.419261 THz;
26 f = 10.262787 THz;	26 f = 10.353991 THz;
27 f = 10.215816 THz;	27 f = 10.293062 THz;
28 f = 10.112512 THz;	28 f = 10.211886 THz;
29 f = 10.051256 THz;	29 f = 10.142866 THz;
30 f = 9.940816 THz;	30 f = 10.118223 THz;
31 f = 9.935491 THz;	31 f = 10.0603 THz;
32 f = 9.896336 THz;	32 f = 10.030261 THz;
33 f = 9.895976 THz;	33 f = 9.983432 THz;
34 f = 9.624008 THz;	34 f = 9.857049 THz;
35 f = 9.401891 THz;	35 f = 9.205305 THz;
36 f = 9.240627 THz;	36 f = 9.11219 THz;
37 f = 5.719458 THz;	37 f = 6.041947 THz;
38 f = 5.700658 THz;	38 f = 6.030172 THz;
39 f = 5.692095 THz;	39 f = 5.788885 THz;
40 f = 5.657336 THz;	40 f = 5.760298 THz;
41 f = 5.572127 THz;	41 f = 5.652337 THz;
42 f = 5.571071 THz;	42 f = 5.63432 THz;
43 f = 5.374978 THz;	43 f = 5.535592 THz;
44 f = 4.553837 THz;	44 f = 5.501739 THz;
45 f = 4.448177 THz;	45 f = 5.496043 THz;
46 f = 3.979203 THz;	46 f = 5.363003 THz;
47 f = 2.269556 THz;	47 f = 5.017986 THz;
48 f = 1.011962 THz;	48 f = 4.458984 THz;

Table 4.3 Local vibration modes for P_1V and P_2V. Only atoms up to 2nd neighbors of the vacancy were moved to evaluate the Hessian matrix (16 atoms in total, which are represented in the dipole analysis plots). This table shows the obtained frequencies.

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P_3V	P_4V
1 f = 13.453994 THz;	1 f = 13.086869 THz;
2 f = 13.45256 THz;	2 f = 13.085566 THz;
3 f = 13.017252 THz;	3 f = 13.083592 THz;
4 f = 13.016521 THz;	4 f = 13.013397 THz;
5 f = 12.889684 THz;	5 f = 13.012772 THz;
6 f = 12.795232 THz;	6 f = 12.928945 THz;
7 f = 12.661607 THz;	7 f = 12.927812 THz;
8 f = 12.661394 THz;	8 f = 12.927615 THz;
9 f = 11.81654 THz;	9 f = 11.970855 THz;
10 f = 11.582364 THz;	10 f = 11.729083 THz;
11 f = 11.581853 THz;	11 f = 11.727427 THz;
12 f = 11.11035 THz;	12 f = 11.72698 THz;
13 f = 10.797344 THz;	13 f = 10.852821 THz;
14 f = 10.791561 THz;	14 f = 10.764987 THz;
15 f = 10.79117 THz;	15 f = 10.764505 THz;
16 f = 10.702194 THz;	16 f = 10.764017 THz;
17 f = 10.660193 THz;	17 f = 10.659991 THz;
18 f = 10.659462 THz;	18 f = 10.659883 THz;
19 f = 10.600787 THz;	19 f = 10.65868 THz;
20 f = 10.593057 THz;	20 f = 10.572847 THz;
21 f = 10.592818 THz;	21 f = 10.57131 THz;
22 f = 10.538467 THz;	22 f = 10.520641 THz;
23 f = 10.517555 THz;	23 f = 10.520262 THz;
24 f = 10.517331 THz;	24 f = 10.5196 THz;
25 f = 10.413064 THz;	25 f = 10.487351 THz;
26 f = 10.412899 THz;	26 f = 10.487034 THz;
27 f = 10.256657 THz;	27 f = 10.486769 THz;
28 f = 10.189753 THz;	28 f = 10.261987 THz;
29 f = 10.171262 THz;	29 f = 10.261846 THz;
30 f = 10.170647 THz;	30 f = 10.206268 THz;
31 f = 10.164506 THz;	31 f = 10.205648 THz;
32 f = 10.108211 THz;	32 f = 10.20519 THz;
33 f = 10.108107 THz;	33 f = 10.082349 THz;
34 f = 9.973731 THz;	34 f = 10.081654 THz;
35 f = 9.887436 THz;	35 f = 10.081069 THz;
36 f = 9.887116 THz;	36 f = 9.939746 THz;
37 f = 5.787 THz;	37 f = 5.801555 THz;
38 f = 5.785713 THz;	38 f = 5.798488 THz;
39 f = 5.769497 THz;	39 f = 5.79735 THz;
40 f = 5.560131 THz;	40 f = 5.725372 THz;
41 f = 5.559744 THz;	41 f = 5.72351 THz;
42 f = 5.534425 THz;	42 f = 5.6374 THz;
43 f = 5.479777 THz;	43 f = 5.527604 THz;
44 f = 5.478678 THz;	44 f = 5.527159 THz;
45 f = 5.468571 THz;	45 f = 5.52458 THz;
46 f = 5.078492 THz;	46 f = 5.186513 THz;
47 f = 5.077182 THz;	47 f = 5.185438 THz;
48 f = 3.907066 THz;	48 f = 5.181417 THz;

Table 4.3b Local vibration modes for P_3V and P_4V. Only atoms up to 2nd neighbors of the vacancy were moved to evaluate the Hessian matrix (16 atoms in total, which are represented in the dipole analysis plots). This table shows the obtained frequencies.

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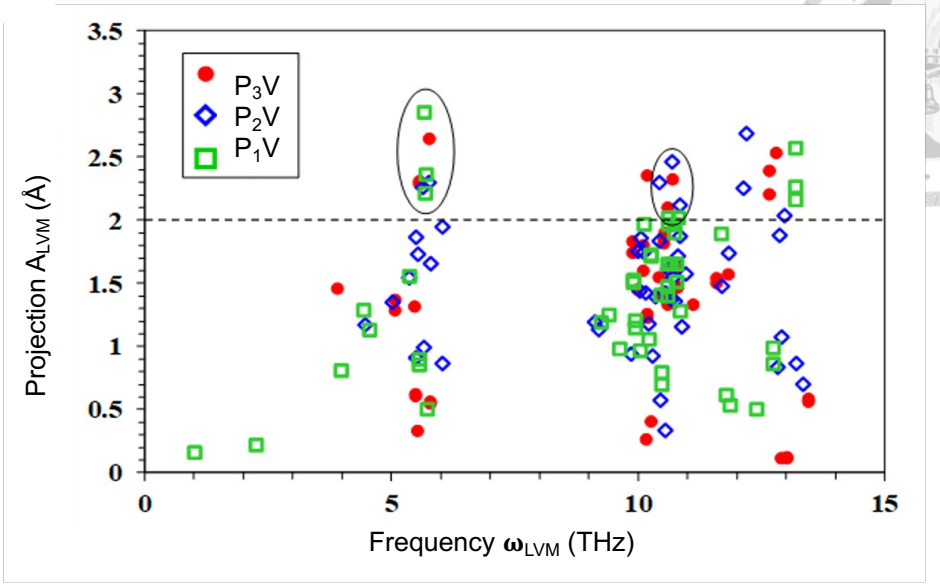

Figure 4.6 Mechanism of direct energy coupling and selective dopant activation. Projection of atomic displacements of LVMs calculated from Eq. (1) as a function of their frequency for P_1V-P_3V clusters. The horizontal dashed line indicates the threshold used to select highly aligned LMVs with the corresponding net dipole moment direction. Circles show those highly aligned LVMs with similar frequencies.

4.6 Dynamical donor-vacancy clustering phenomena in highly n-doped silicon

A clear conclusion can be drawn from the calculation results : thermodynamics favors the vacancy aggregation of P atoms in the form of P_nV complexes or the attachments of P atoms to microvoids compared to the isolated quadruple coordination configuration. In other words, P-doped Si is always metastable at all doping levels. It is only possible to have electroactive P in n-doped Si due to kinetic limitations of activated P migration to stable P_nV. Such dynamic donor-vacancy clustering phenomena have been observed in heavily doped silicon, and the underlying atomic-scale processes have been well

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described [146, 147]. Earlier researchers have demonstrated extensive first-principles calculations. In particular, Ramamoorthy *et.al.* found that vacancies (V), DV pairs, D_2V clusters, and higher-order D_nV clusters played distinct roles in the observed dopant deactivation, reactivation, and anomalous diffusion. The high-order D_nV is formed from low-order mobile AsV clusters in "pre-percolation" patches with very high doping concentrations and produces fast donor clusters at moderate temperatures.

Rankie et al [147, 148] further showed that vacancy-donor pairs (DVs) migrate at temperatures around 450 K, converting to D_2V defects. In the case of the doping concentration was high enough, these defects became D_3V around 700 K. They further demonstrated that these D_3V defects were annealed at 1100 K. These results indicated that D_3V was the dominant vacancy defect in the D_nV distribution in doped Si with a P concentration of 2 x 10^{20} at./cm^3, which presented in concentration-dependent dopant electrical deactivation. In the epitaxial SiP of this study, the P concentration is 3 x 10^{21}at./cm^3, which can be expected more favorable for the further conversion of D_3V to the more stable D_4V. These observations are the basis for modern rapid annealing process technology design. The rapid annealing process utilizes D_nV to dissociate at high temperature for dopant activation and immediate quench to avoid D_nV re-aggregation during cooling process. The evolution of modern dopant-activated annealing from seconds to shorter times of milliseconds, microseconds, and even nanoseconds is based on this kinetic theory of D_nV formation and dissociation.

Although the rapid annealing process can simultaneously provide a high degree of dopant activation and avoid dopant diffusion, the inevitable subsequent thermal treatment still leads to the deactivation of the donor in a non-equilibrium state. The dopant activation in heavily doped Si:P results from the breakdown of vacancy-donor complexes formed at a lower temperature. This work first considered the destruction of P vacancies

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by removing one phosphorus atom from the cluster, that is, the binding energy of each P atom. Early ab-initio calculation [149] showed that the energy required is comparable regardless of the cluster type. The energy is 1.2 eV for the evolution of P_nV to $P_{(n-1)}V$ (n=1,2,3,4), that is, PV($PV \rightarrow P + V$), P_2V($P_2V \rightarrow P + PV$), P_3V($P_3V \rightarrow P + P_2V$) and P_4V($P_4V \rightarrow P + P_3V$). This is particularly important because it would indicate that upon a fast MSA annealing at a temperature above 1100 °C, the net effect of the activation process is to reduce the population of P_4V clusters. Still, thermally unstable PV, P_2V, P_3V vacancy-dopant clusters will always be present after the anneal [146]-[148]. During the cooling down process from the annealing temperature or upon a subsequent thermal with a moderate thermal budget, these unstable D_nV (n<4) could act as origin or precursors for the generation towards stable but inactive P_4V clusters, leading to the electrical donor deactivation phenomenon as shown in Figure 3.5(b). It is these unstable $D_{n-1}V$ media that remain in the junction after annealing, enhancing the aggregation kinetics required for D_nV formation at moderate temperatures ranging from 600 to 700 °C.

4.7 Selective dopant activation through polar- D_nV structures by Microwave annealing

In Section 4.4, the simulation works demonstrate the existence of electric dipole moments associated with various P-vacancy clusters (P_nV) by performing ab initio calculations. Figure 4.5(a) shows the net atomic charge within a simulated cell containing P_nV complexes. This analysis shows large positive charge values associated with the P atoms in the simulated cells (intense red atoms in Figure 4.5(a)) and large negative charge values at nearby Si (blue atoms in Figure 4.5(a)). This charge distribution around the P_nV complex results in a net dipole moment. Their sizes are summarized in Table 4.2, and

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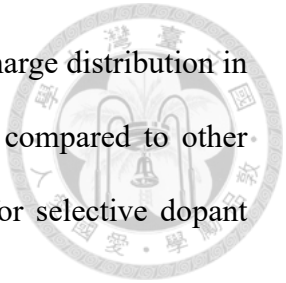

their orientations are shown in Figure 4.5(b). The symmetry of the charge distribution in the stable P_4V complex results in a negligible net dipole moment compared to other unstable polar P_nV (n = 1-3) complexes. This provides the basis for selective dopant activation.

Through direct energy coupling between the dipole moment and the microwave external electric field, non-vanishing dipoles in less stable P_nV clusters can be used to eliminate these P_nV clusters in microwave annealing selectively. On the other hand, microwaves do not affect the relatively stable P_4V clusters due to the lack of a permanent dipole moment. This would result in a unique P_nV distribution dominated by stable P_4V, in strong contrast to MSA annealing, where unstable D_nV is always present.

As a result of the above observations, the evolution of vacancy defects in heavily doped Si:P in different activation annealing processes, MWA and MSA was compared and summarized in (Fig. 4.7). For thermal anneal by MWA at a substrate temperature of 680 °C, the polar-P_nV defects are dissociated through a non-thermal interaction with the MW electromagnetic field, while the non-polar P_4V remains intact. The long duration (~300 sec) of MWA ensures that most of the low order polar P_nV would undergo this MW interaction and become dissociated and activated. The mobile vacancy could migrate to Si surface and disappear from there. Furthermore, the lower substrate temperature (680 °C) in MWA is an advantage in preventing further D_nV reclustering (donor deactivation) during the cooling down period. The above unique selective interactions between P_nV and MW result in a P_4V dominant population and lower vacancy concentration in Si:P after MWA. As a result, the combined effect led to a thermally stable dopant configuration to resist de-activation upon subsequent thermal processes. In contrast, the high peak temperature MSA with millisecond anneal pulse duration activates the dopant through a non-selective dissociation of P_nV. Deactivation could occur during the cooling down

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period from high temperatures (>1000 °C) and limit the highest level of activation that could be accomplished. Consequently, MSA results in P_nV configuration with a wide distribution of n=1-4, and vacancies in Si:P. Upon subsequent thermal agitation, the Si:P is readily deactivated due to P_nV cluster formation from $P_{n-1}V$. Our study shows that the well-known problem of the donor deactivation limitation in the semiconductor industry can be overcome by eliminating the low-order donor vacancy cluster distribution within the heavily doped Si layer.

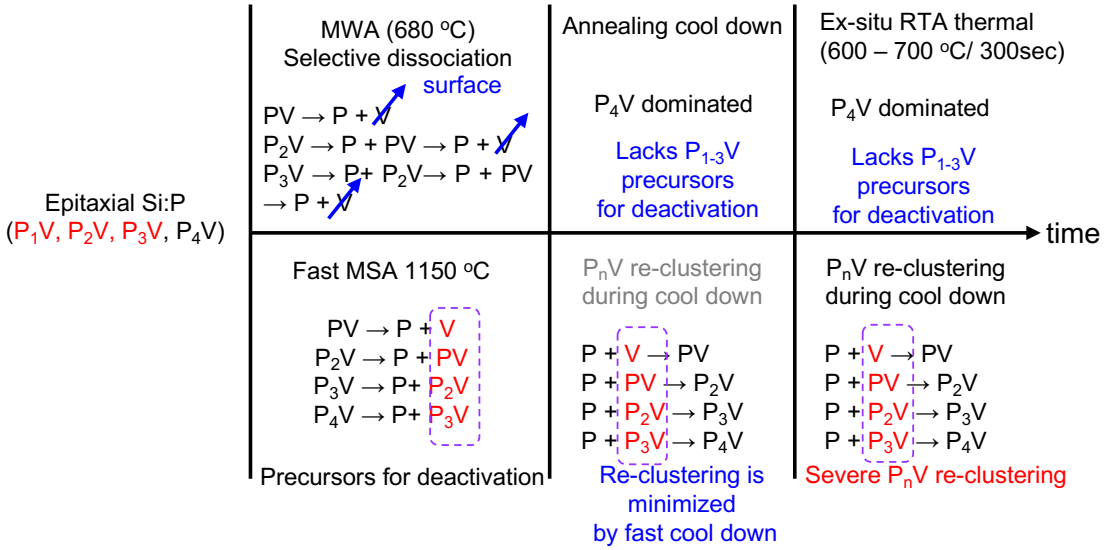

Figure 4.7 Comparison of reaction mechanisms during MWA annealing and MSA annealing in highly doped Si. MWA enables the selective dissociation of lower order and unstable P_nV (n=1-3), leaving behind an electrically activated isolated P and P_4V vacancy complex that leads a stable junction. Fast MSA generates lower order P_nV during the annealing process at leak temperature, the available low order P_nV in doped Si serves as the precursor for continue P deactivation during cooling down process or upon a moderate RTA thermal budget.

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Chapter 5 Susceptor-assisted Microwave Selective Dopant Activation Annealing

Long wavelength base microwave heating is one of the electrothermal heating techniques. Electrothermal heating techniques include induction heating, radio frequency heating, direct resistance, or infrared heating, all of which are specific to the broad electromagnetic spectrum, as shown in Figure 5.1. The main advantages of microwaves for traditional industrial processing are fast heat transfer, simultaneous volumetric and selective heating, and compact equipment.

Microwaves are rarely used in silicon semiconductor processes in materials processing. This has to do with how little is known about how doped silicon interacts with microwaves. Unlike conventional thermal annealing, one usually only needs to focus on the thermal budget, i.e. how fast the annealing technique can ramp up to the target temperature and how fast it can ramp down. In contrast, according to the energy coupling mechanism, the microwave annealing process is not necessarily continuous. Still, it may be discrete in this study and the interaction between some specific materials and microwaves. The interaction of microwaves with silicon can generally be divided into thermal and non-thermal parts. Depending on the material's electrical conductivity, thermal effects can be further divided into two main microwave heating processes: dielectric polarization losses and ohmic conduction losses. The non-thermal effect is what this study try to explore to understand if it can reach conventional high-temperature millisecond dopant activation but at a much lower temperature. Based on the structure of the inactive dopant associated with the non-vanishing dipole moment learned in section 4.4, and its relatively small concentration of less than 6% in the silicon lattice. The

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possibility of having a non-thermal coupling of microwave energy to achieve epitaxial SiP selective dopant activation was investigated.

5.1 Motivation of dopant activation by microwave annealing

For microwaves, the differences in frequency and wavelength of microwaves cause vastly different interactions with matter compared to rapid thermal annealing (RTA) and millisecond annealing (MSA) light sources, which are primarily in the ultraviolet, visible, and short infrared ranges (Figure 5.1)[150]. The complex multiple interaction mechanisms between microwave and matter is much more complicated than the interaction dominated by thermal effects, so it is rarely used in the semiconductor industry.

Historically, the trend in dopant activation annealing has evolved from furnace annealing to RTA spike annealing, and various versions of millisecond annealing (MSA, flash or laser annealing) or even nanosecond annealing (NSA) [151]-[154]. Although all of these methods have been successfully applied to source/drain annealing for decades, they are accompanied by a number of problems that limit CMOS fabrication yields. In addition to the aforementioned donor deactivation problem, both RTA and MSA suffer from the "patterning effect" [155]–[159]. The local temperature of the annealed layer depends on the local reflectivity or emissivity of the patterned structure.

The pattern effect results from the thermalization mechanism by which the laser or lamp transfers the deposited energy to the processed wafer surface. As shown in Figure 5.2, RTA, MSA, and laser annealing (LSA) are based on brief but very intense exposure to shortwave radiation. Millisecond annealing with a thermal diffusion length of 100 um cannot flatten the local temperature difference if the variation in intra-die reflectivity exceeds 100 um. In this case, it usually see local temperature changes occur. For longer RTA processing times of more than a few seconds, the lateral thermal diffusion is in

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millimeters scale, based on which local reflectance changes are significant, and the spatial extent exceeds millimeters, RTA will observe a pattern loading effect caused by local reflectance variation. Briefly, a large chip area with area dimensions greater than 2 cm by 2cm often see annealing pattern loading effects due to more likely large-scale local reflectance variations.

Unlike lamp- or laser-based RTA and MSA systems, the long wavelengths of cm-scale microwaves make them immune to pattern effects. In the following sections, I will step-by-step through the fundamentals of microwave heating, and then describe the microwave optimization setup, including the susceptor set and microwave power within the cavity, to demonstrate MWA's comparable dopant activation performance to MSA, but with excellent stability.

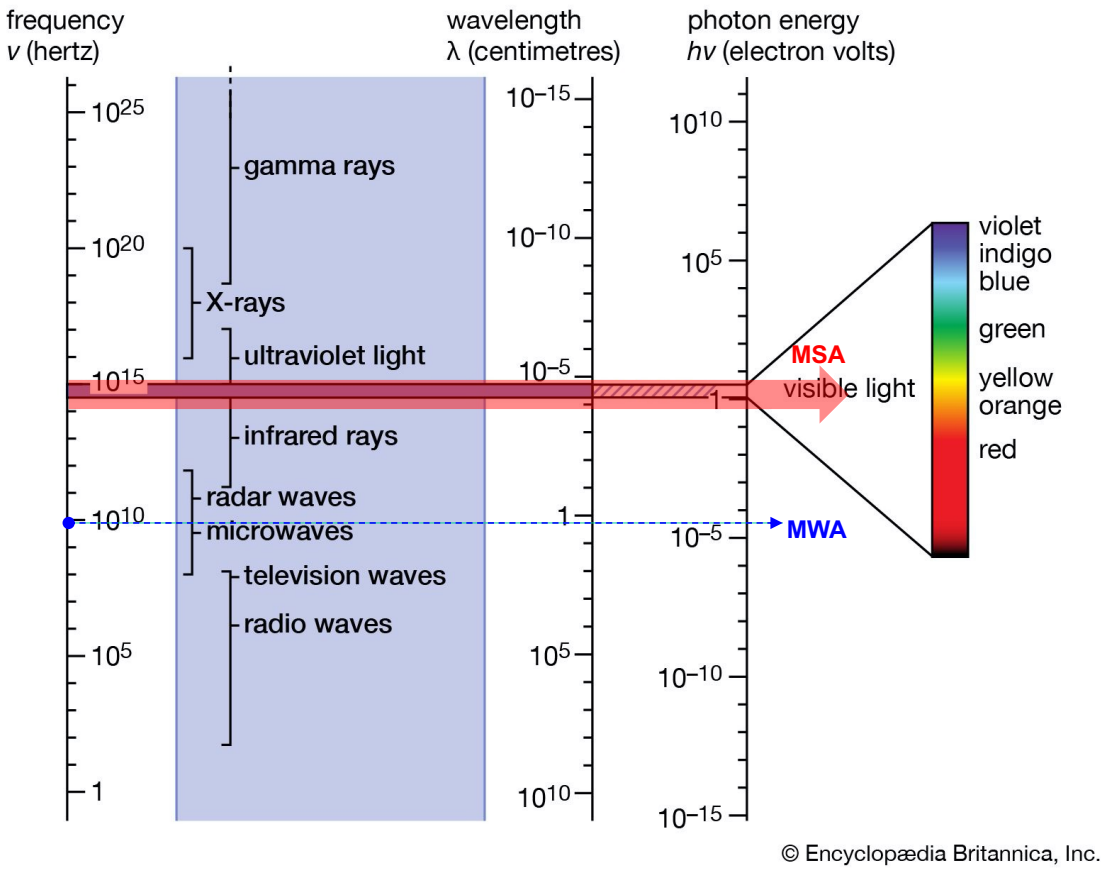

Figure 5.1 The electromagnetic spectrum covers radio waves, microwaves, infrared,

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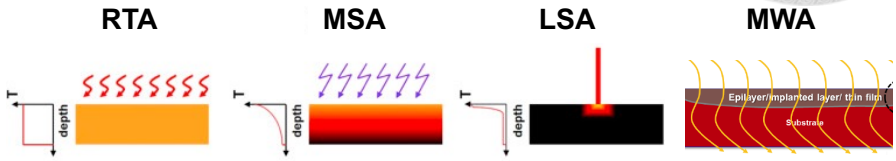
ultraviolet, X-rays, and gamma rays. The narrow range of visible light is between IR and UV and is shown enlarged on the right [150].



Technical spec	RTA	MSA	LSA	Microwave
Wafer T (front side/backside)	whole wafer is heated	near surface ~ 200 μm	near surface <1um μm	whole wafer+ local selective
Dwell time	>1 sec	0.1 ms ~ 10 ms	1 μs ~ 400 μs	50 ~ 300 sec
Annealing T	u to 1250 deg C	up to 1250 deg C	up to 1300 deg C	up to 700 deg C
Energy source	tungsten-halagen	Xeon arc lamps	CO2 laser or diode laser	2.45 GHz mangetron
EM wave spectrum	visible to 2 μm	250-900 nm	CO2 laser: 10.56 μm diode laser: 810 nm	12.2 cm

Figure 5.2 Temperature and thermal budget comparisons for various annealing techniques, including MWA, RTA, selective-MWA, MSA (LSA)

.

5.2 The interaction of microwave with Si

Microwaves interact with matter through the E component of the microwave electric field and the H component of the magnetic field (Figure 5.3). As mentioned previously, the basic interaction mechanism between Si and microwave is mainly divided into thermal and non-thermal effects. Thermal effects are subclassified into two main microwave heat-generating processes: dielectric polarization and ohmic conduction losses. For heavily doped epitaxial Si:P, the three interaction mechanisms of conduction loss, dielectric loss, and thermally coexist when interacting with microwaves.

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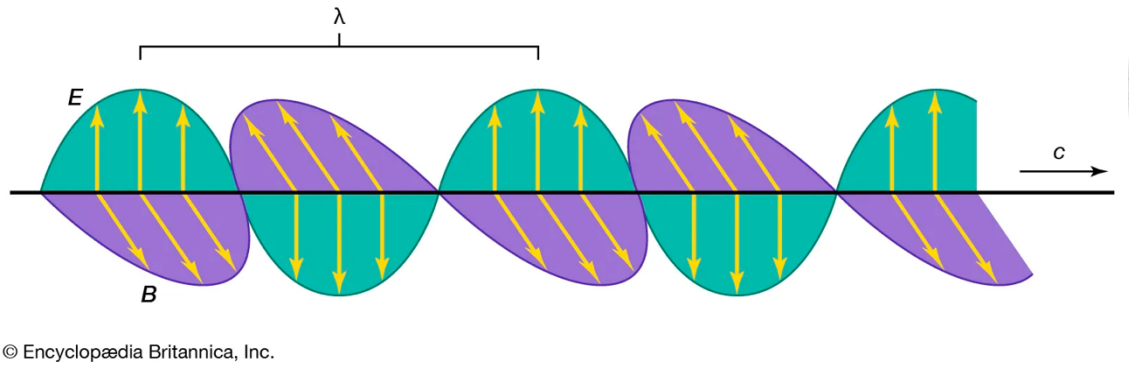

Figure 5.3 The electromagnetic field is represented by the electric field E vector and the magnetic field B vector are perpendicular to each other and perpendicular to the direction of propagation [150].

Conductive heating: Heavily doped Si:P becomes more conductive when heated, and the microwave oscillation propagating through Si:P induces the contribution of surface eddy currents to generate conduction losses is to be expected. When an eddy current flows through a near Si:P surface, the quantity of heat produced in it is directly proportional to (1) the square of the current (2) The resistance of the Si:P (3) the time for which the current flows [160]-[162]. Therefore, it is expected that the conduction heating can be influenced by Si:P layer thickness, the dopant concentration in Si:P, and the substrate temperature.

Dielectric heating: Dielectric heating is an electric field heating process that increases the temperature of a dielectric (non-conductive) material by applying an alternating electric field, such as microwaves or radio frequency [163]-[165]. Unlike traditional thermal annealing heating, which requires a "heat" source, dielectric heating is an innovative process that does not require a "heat" source, such as a tungsten halogen lamp or Xeon arc lamp. Dielectrics are insulators and have very poor electrical conductivity concerning electrical current. Since the Si:P layer is semiconducting, conductive and

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dielectric heating were considered since the SiP layer is composed of basic atoms through covalent bonds. When the external field is not present, any charged entities within the material are randomly positioned in it. But when the charged entities of the dielectric, such as constituent atoms or molecules, are all placed in the electric field in the presence of an external field, their negatively charged electrons and positively charged cores are slightly separated by polarization and acquire a dipole moment. As the fields alternate, the polarization directions of the dipoles also alternate. Charged entities push, pull, and collide with other molecules during translation or vibration, distributing energy to neighboring atoms in the material and generating heat loss. Depending on the conductivity σ of the Si:P layer and the microwave frequency, e.g. $\sigma \ll \omega\varepsilon$ (where $\varepsilon = \varepsilon r'' \varepsilon 0$), then conduction heating is negligible and dielectric heating becomes the dominant mechanism for energy loss.

Nonthermal annealing effect: Athermal effects increase the thermal energy of a material due to dielectric heating or conductive heating. The so-called "athermal" effect refers to the fact that the microwave energy is directly coupled to the energy mode within the molecule or lattice and does not increase the thermal energy of the material to cause a temperature change. The non-thermal efficiency can generally be attributed to the increased probability of microwave interaction with special bonds (such as dipoles formed by donor vacancy clusters) and the decreased activation energy, thereby enhancing the bonding reaction with the help of the microwave field [166]-[170]. In this work, since the concentration of inactive donor vacancy clusters (D_nV) of Si:P is less than 6%, the microwave-P_nV energy coupling can be expected to be athermal effect , that is, the P_nV -microwave energy coupling does not change the Si substrate temperature. Non-thermal effects in solids are still part of an ongoing debate and need to be further

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investigated.

This research work considered that these three microwave interaction mechanisms must occur simultaneously during the Si:P microwave annealing process. Therefore, each interaction must be controllable to satisfy fundamental junction requirements such as abrupt doping profile, doping activation comparable to MSA, and stable junction. Since dielectric heating is a heating effect, the temperature must not exceed 700 $^{\circ}C$ to avoid any unwanted dopant diffusion. Theoretically, we also need to understand that in the absence of non-thermal effects on dopant activation, dielectric heating by microwave annealing at around 600 to 700 °C will only deactivate the dopant without increasing the amount of dopant activation. It is attributed to the non-selective and bulk heating nature. This suggests that the microwave cavity setup is required to achieve a process scheme that allows dielectric heating and non-thermal annealing effects to coexist. As shown in the following sections, experimental results show that this optimal microwave setting is not easily attainable. It requires the accumulation of long periods of trial and error to optimize the microwave setting.

Unlike non-thermal annealing effects, dielectric heating has a fairly complete theoretical basis for understanding. There are three basic types of polarization in the interaction of electromagnetic waves with solids (Figure 5.4) [169], which are frequency-dependent and cause losses. Previous studies have shown that dipole polarization dominates around the electromagnetic wave frequency of 10^{10} Hz in semiconductor silicon, which is the fundamental mode of energy coupling in semiconductor microwave heat loss [172]-[187]. Atomic polarization is responsible for frequency losses up to 10^{13} Hz in the far infrared; electrons vibrating around the nucleus produce electron polarization losses in the ultraviolet at 10^{15} Hz [187]. For epitaxial Si:P heating

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applications, the interaction mechanism may be more complex due to the inactive dopant structure in the silicon lattice, which involves overlying the silicon lattice structure and phosphorus vacancy clusters and activated P in the lattice. Furthermore, substrate resistivity and dielectric constant may vary with dopant concentration. Therefore, we can expect that it will be difficult to fully understand the interaction between microwaves and doped Si:P until concrete results are obtained experimentally. Nonetheless, what has been learned from standard microwave dielectric heating can still provide insights that may be useful for exploratory work on microwave applications in silicon. With a fundamental understanding of dielectric heating, it would be helpful to predict possible microwave-silicon interaction mechanisms and optimize the microwave cavity setup by repeating the dopant activation test until the desired result is achieved.

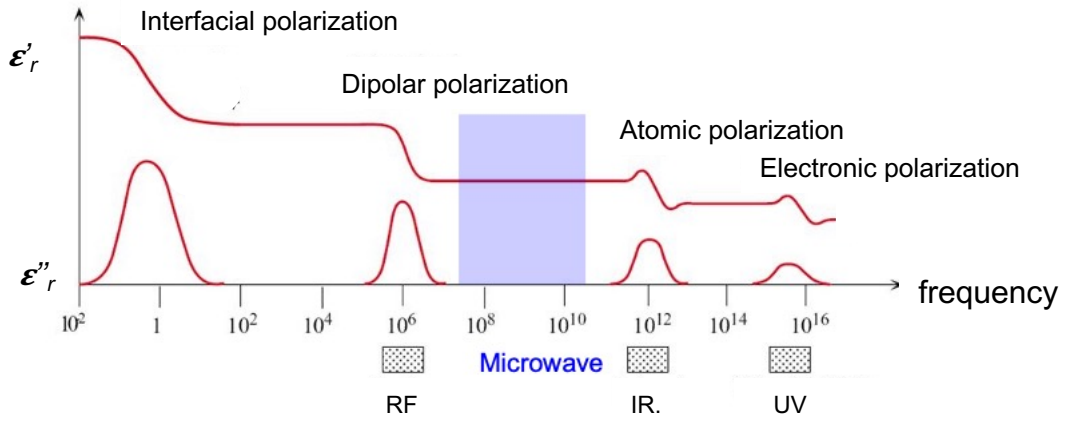

Figure 5.4 "Electromagnetic wave frequency" dependent dielectric polarization mechanism. In the presence of interfacial, orientational dipolar, ionic, and electronic polarization mechanisms, the frequencies of the real and imaginary parts of the permittivity. [171].

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5.3 Dielectric heating

Dielectrics are basically insulators in nature and have very poor ability to conduct electrical current. It has been found that every substance in nature is composed of molecules with atoms as basic particles. Microwave dielectric heating occurs when a material placed in an alternating electric constant contains atomic charges that are polarized by an electric field. The polarization cannot catch up with the rapid reversal of the electric field. Electrons, atoms, dipoles, and interfaces are separate components that add up to form the total polarization. Electronic polarization occurs when electrons rearrange near a particular nucleus. The uneven distribution of charges within a molecule leads to a joint displacement of atomic nuclei, known as atomic polarization. The electric field of the permanent dipole results in dipole polarization. Interface polarization occurs when charges accumulate at the interface.

However, due to their fast polarization and depolarization response timescales (10^{-9} seconds faster than microwave frequencies), electron and atomic polarization cannot produce dielectric loss effects. Since the radiated electric field of electromagnetic waves is in an oscillatory state, the time scales associated with orientation and disorientation phenomena depend on the response time of the polarization exhibited by the material properties. The dynamic response of electron and ion (atomic) polarization and depolarization is extremely fast, at least one hundred times faster than dipole. Compared with the orientation or disorientation of permanent dipoles, it is virtually a temperature-independent phenomenon.

Orientation or dipole polarization is the most common and important heating mechanism at the microwave frequency of 2.45 GHz. For example, under the rapidly oscillating field of microwaves, the permanent dipoles of typical solvent molecules

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rearrange. The frequency of rearrangements is 10^9 times per second [158]. In each case, it failed to do so when the solvent polar molecules tried to rearrange under the raoid oscillating electric field to keep themselves in the same phase. This in turn results in translation or vibration within the polar molecules, which ultimately generates heat through friction.

Although the term heating is used, Dielectric heating behaves very differently from conventional heating that relies on a "heat source." Dielectric heating generally refers to radio frequency and microwave frequency heating. Microwaves and radio frequencies are both forms of EM wave energy, but not "heat sources". They are only converted into heat when interacting with the material. Dielectric heating is different from conduction heating caused by induced currents in conductive media. Based on the electrical conductivity of the material and the excitation frequency of the incident electromagnetic wave, it can be judged which heating mechanism is dominant.

Microwave radiation has the advantage of coupling energy directly into the dielectric volume. In contrast, standard RTA heating requires heat to diffuse from the outer surface layer of the medium into the medium, as shown in Figure 5.5. As the microwaves pass through the semiconductor medium, they will interact with charged entities in the silicon and inactive dopant structures in the dopant medium. These interactions usually take the form of heat generation. As heat through dielectric and magnetic losses in the volume V, the energy dissipated can be expressed as:

$$P = \int_V \sigma \langle \overline{E}^2 \rangle dV \tag{5-1}$$

where $< \overline{E}^2 >$ is the root mean square (RMS) value of the alternating microwave electric field.. The dielectric constant of a material can be expressed as:

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$$\varepsilon = \varepsilon' - i\varepsilon''$$

The first term is the real part, representing the degree of the microwave penetrating the material, which is in phase with the microwave electric field. The 2nd term is the imaginary par, representing the material's ability to absorb microwave energy and turn it into heat, which is out of phase with the microwave electric field E. The ohmic dissipation dominates for materials with high electrical conductivity and ε' ~1. The loss tangent [173]-[176] is given by tan $\delta = \varepsilon r''/\varepsilon r'$. The dielectric loss tangent (tan δ) of a material represents the quantitative dissipation of electrical energy due to total different physical interaction processes such as conduction heating, dielectric heating, and losses from any other nonlinear operations (Figure 5.6).

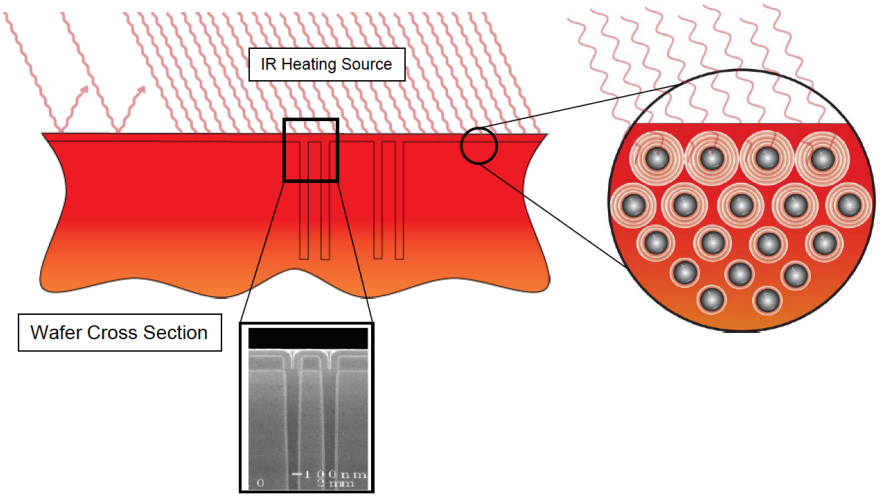

Figure 5.5 RTA heating, heating is limited by thermal diffusivity and surface temperature.

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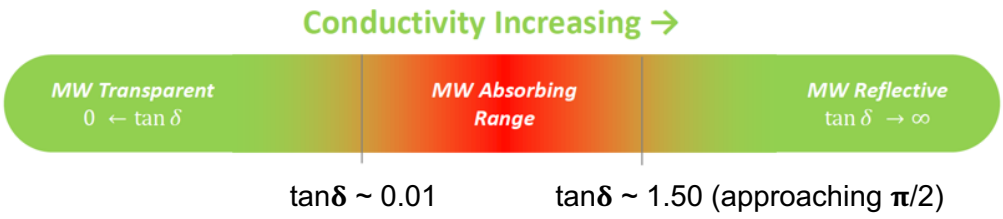

Figure 5.6 Loss factor-dependent microwave absorption, microwaves are highly absorbed in materials with loss factors between 0.01 and 1.5, below 0.01 microwaves penetrate the material, above 1.5, microwaves are reflected from the material

In dielectric heating, heat is generated by the interaction of microwaves with the material. Therefore, it is intuitive that the E-field strength is related to the power loss of the material. The power density produced per unit volume can be written as:

$$Q = \omega \cdot \varepsilon_r'' \cdot \varepsilon_0 \cdot E^2$$

where ω denotes the angular frequency of the microwave, ε_r'' denotes the loss factor and is a measure of the extent to which a substance undergoes microwave dissipation or loss, ε_0 is the permittivity (dielectric constant) of free space and E is the intensity of the microwave electric field . In this study, ω is fixed because the magnetron output frequency is 2.45 GHz, and the microwave power controls the electric field strength E. In the case where the conductivity σ of the material is very small and the selected microwave frequency is too high, this makes the conductivity σ much smaller than ωε, where $\varepsilon=\varepsilon_r''\varepsilon_0$, and the conduction heating contribution can be neglected . In this case, dielectric heating is the main mechanism by which electromagnetic field energy is lost to the medium. In this diserttation, microwave power has been known to be one of the key factors for interacting with inactive dopant structures in the Si:P layer . From the above equation, it can be understood that when the power is increased to above 10 kW, the electric field

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strength changes, but directly increasing the power is not the most effective way to increase the electric field strength. Depending on the boundary conditions set by the microwave cavity and susceptor configuration, the E-field distribution can be designed as a standing wave with resonance assistance. The advantage is to obtain a much higher (> 100X) E field intensity but avoid excessive power losses in the material, which can bring the temperature into an undesired state. This feature is also one of the main differences compared to traditional short wavelength base thermal annealing..

In this section, I have introduced that based on the material charge entity in the material structure, when microwaves are applied, the material may go through a phase or phases or multi-polarization phenomena at the same time. Since then, the total polarization term Ptotal is often used in interacting materials with microwaves. P is always contributed by four polarization mechanisms, including atomic polarization, electron polarization, dipole polarization, and space charge polarization. The correlation can be written as: $P_{total} = P_{atomic} + P_{electronic} + P_{dipolar} + P_{space\ charge}$.

All the different polarization mechanisms were summarized in Figure 5.8. They are the mechanisms by which microwave energy can be converted into heat in the material during the interaction process and will be explained below:

Electron Polarization: In the presence of an external electric field, this polarization effect occurs in all atoms because the electron cloud always orbits the nucleus. The nucleus and the center of gravity of the orbital electron cloud are displaced from each other, forming a very small dipole with little polarization effect (Figure 5.7(a)). This reaction is non-selective in the doped silicon lattice structure and is the bulk heating mechanism of the carrier silicon substrate.

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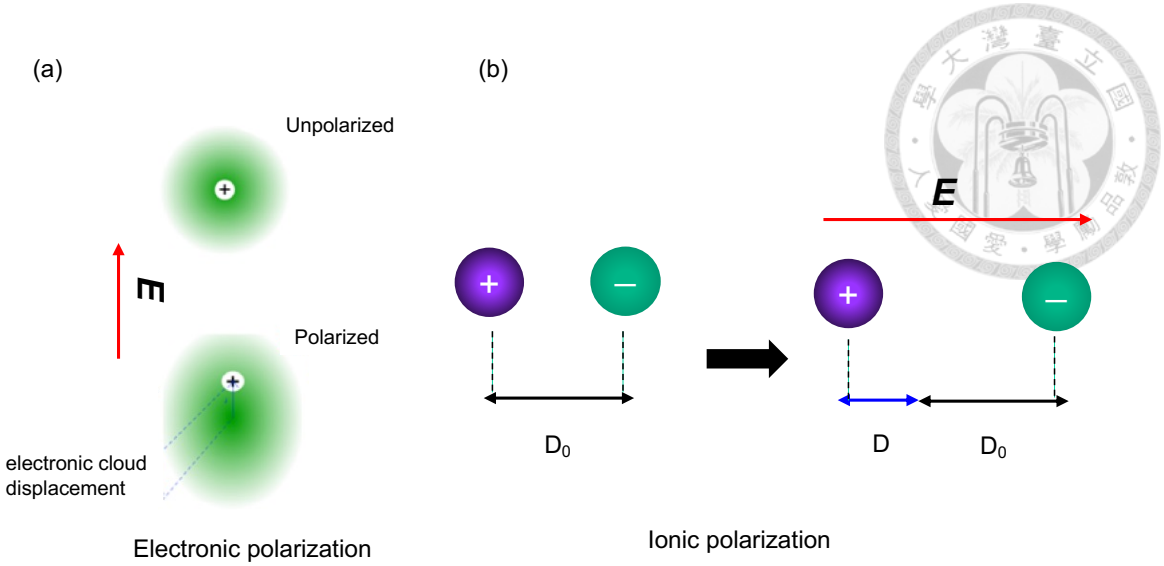

Figure 5.7 Different polarization mechanisms; (a)Electronic polarization and (b) ionic polarization under external electric field

Ionic polarization: In typical ceramic material ionic solids, the ionically bonded ions are arranged in lattice symmetry and thus have negligible polarization. However, when an electric field is applied to an ionic solid, its constituent cations and anions are attracted in opposite directions due to their opposite polarities (Figure 5.7(b). This produces relatively large ionic displacements (compared to electron displacements), which is why ceramics commonly used in capacitors have high dielectric constants. In the discussion in Section 4.4, it was mentioned that the inactive dopant in doped Si has a non-net-zero polarization dipole moment in the lattice. Once an electric field is applied, relatively large ion displacements can theoretically be produced. Although this results in a locally high dielectric constant in the doped silicon, since the unactivated dopants only make up less than 6% of the silicon lattice, there is no significant thermal effect on the substrate to affect temperature. This work classify this effect as a non-thermal effect with efficient local energy coupling. Although there is a lack of physical descriptions of non-thermal effects in the literature, a later discussion will show that the selective dopant activation

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phenomena are based on such non-thermal effects.

Dipole (or directional) polarization: When an external electric field is applied to a composite material containing permanent dipoles, these permanently polar molecules realign with the electric field. The associated hysteresis and intermolecular collisions lead to dielectric heating during realignment in response to alternating electric fields.

Most microwave heating effects observed in solvent systems arise through dipole polarization. For example, the different electronegativity of individual atoms in an aqueous solution causes the water molecule to have a permanent dipole moment. When exposed to external microwaves, these dipoles are very sensitive to microwaves and will try to quickly align with the changing direction of the electric field by rotating. This dynamical switching rearrangement with electric field alignment is fast for free molecules, but in liquids, the presence of other molecules prevents the instantaneous alignment. As a result, the responsiveness of the dipole to the field is limited, which affects how the molecule behaves under electric fields of different frequencies.

When using frequencies lower than microwaves, the dipoles can have sufficient time to respond in-phase to the microwaves. In this case, even polar molecules can carry some energy through the oscillating E-field and lose some energy during minor collisions. Still, the net thermal effect is limited and negligible. This is not the case when frequencies are higher than microwave frequencies. In this case, the dipole is completely unable to oscillate with the E-field, so it behaves as if there is no E-field there, so no energy coupling occurs and no heat is generated.

When microwave frequencies lying between these two extreme frequencies are considered , i.e. frequencies comparable to those of the dipole response time. The applied microwave frequency gives the dipole sufficient time to respond to the oscillating electric field and causes the dipole to rotate. However, microwave frequencies are fast enough

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that the rotation cannot fully follow the field, creating a lag. This means that there is a phase difference between the oscillation of the electric field and the rotation of the dipole. This phase difference originates from the drag factor (intermolecular collision and friction) of the dipole rotation, resulting in the energy loss of the dipole.

Interface polarization: This is the least intuitive polarization phenomenon. Space charge polarization usually occurs at material structure boundaries. For example, defects within the material or different material-material interfaces. When an external E-field is applied, these charges may move freely until they see obstacles such as defects and interface boundaries. The space charge follows the oscillation and gradually builds up a net charge in the local barrier region (defect or any interface), leading to an unbalanced charge polarization.

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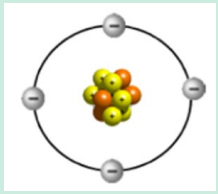
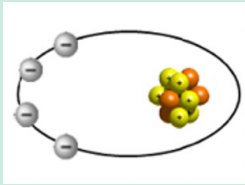
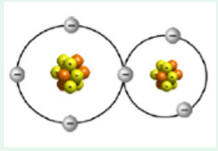
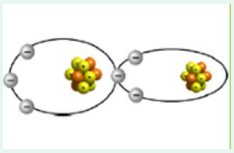
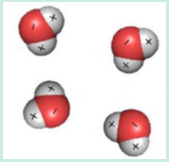
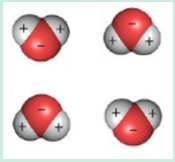
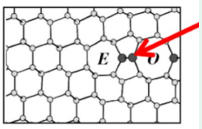
No E Field	Local E Field	Description
		**Electron polarization:** Electron polarization is possible as long as atoms are present. Atoms consist of a nucleus (positively charged) and a cloud of orbiting electrons (negatively charged). Therefore, under the oscillating E-field, it is easy to see the possible relative displacement between the nucleus and the electron cloud due to their different polarities. Therefore, we can expect the covalent electrons in the covalent bond to have a greater response to the oscillating E field compared to the rigid ionic bond. This is why covalently structured materials are often associated with high dielectric constants.
		**Ionic Polarization:** This only occurs in ionic solids with ionic bonding structures. It is natural to think that each pair of ionic bonds already carry a permanent dipole moment. However, the symmetrical structure of the ionic crustal structure makes the permanent dipole moments cancel each other out and cannot generate non-zero dipole moments. In the E field, positively charged cations and negatively charged anions will slightly deviate from their original stable positions in the absence of an external field, resulting in a net dipole moment
		**Dipolar Polarization:** Dipole polarization requires the pre-existence of permanent dipoles in the material. Under the action of the oscillating E-field, the dipole will react with the microwave oscillation, but with a phase lag. The phase lag arises from all the drag factors that drag the dipole to motion. These drag factors cause the phase difference between the E-field oscillations and the dipole rotation to generate heat in the material.
		**Space Charge Polarization (Interfacial):** This involves the accumulation of free charges at the defect region, the phase boundary at the material interface. Also known as Maxwell-Wagner polarization. This is the basis for selective heating using microwaves

Figure 5.8 Dielectric heating polarization mechanisms in dielectric solid

From the previous introduction to dielectric heating, we can understand that microwave interaction can always generate heat in a dielectric substance regardless of the dielectric polarization mechanism. This means that if microwaves can interact with doped silicon, heat and thermal effects are always generated on the Si substrate, with the same results as conventional RTA thermal annealing, which is not what I want. As mentioned earlier, this work will investigate whether non-thermal effects coexist with thermal effects through all possible experimental methods, providing the desired selective dopant activation results and achieving good dopant thermal stability through athermal energy coupling. Below I begin by describing how the cavity settings was tuned by continuously changing the microwave experiments until the optimal microwave cavity settings was found to achieve

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the desired selective dopant activation results.

5.4 Suscetpor-assisted microwave annealing

In the past, microwave processing based on energy-efficient volumetric heating has achieved great success. Compared with traditional furnaces and tungsten-halogen RTA heating, the microwave heating process can generate heat from the inside of the object (Figure 5.9(a)). It overturns the traditional furnace's or RTA's outside-in heat transfer limitation (Figure 5.9(b)) and can achieve the required heating faster than traditional furnaces.

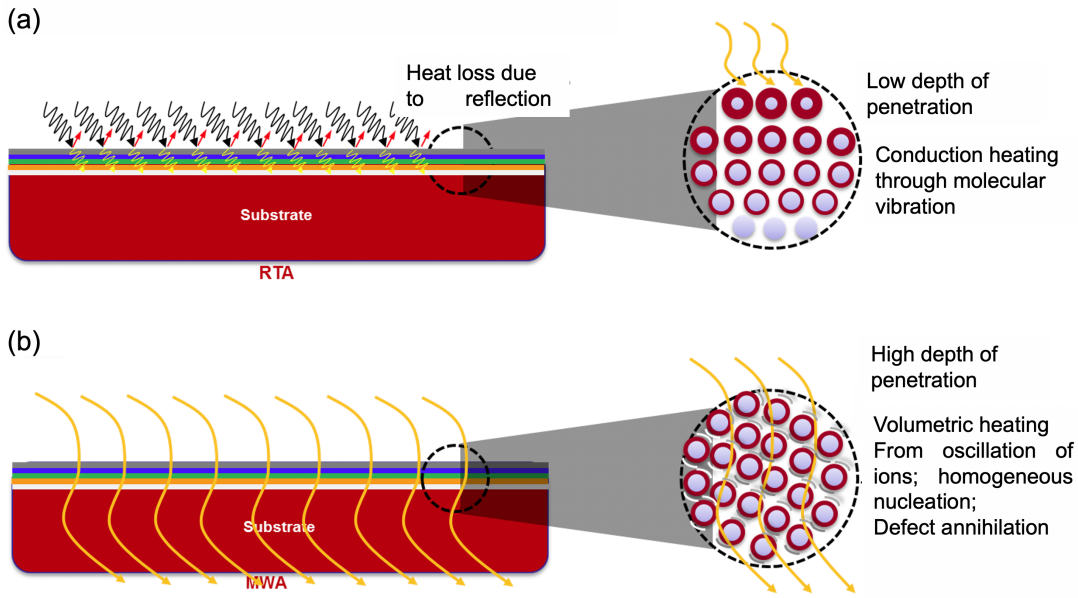

Figure 5.9 (a). Conventional rapid thermal annealing (RTA) heating feature, heating is limited by thermal diffusivity and surface temperature, (b) Microwave volume heating, heat is generated from inside the object.

Commonly used susceptors can further accelerate microwave processing by providing bidirectional heating while reducing heat loss from the material's surface. Furthermore,

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the susceptor's fast initial heating assist function becomes a key factor because the microwave can still handle poorly absorbing materials such as Si. Not only can the susceptor be used for preheating applications, in some cases, the susceptor can be appropriately configured to produce a specific field distribution, allowing the field interaction of the material to achieve high efficiency at the desired background temperature. However, the progress of susceptor-assisted microwave processing is mainly based on experimental trials, and our study is no exception. In the following, this work will demonstrate through experiments that microwaves cannot interact significantly with doped silicon until an optimized susceptor material is found.

Depending on the sample's dielectric properties of microwave annealing applications, the sample can be placed in a cavity for direct microwave coupling through typical dielectric heating mechanisms. The proposed materials for direct microwave energy coupling are those with dielectric constants and high dissipation factors.

On the other hand, when the material dielectric constant is low and tends not to interact with microwaves, preheat assistance is required to increase the dielectric constant or loss factor. According to different preheating methods, microwave annealing can be divided into intrinsic and extrinsic microwave hybrid annealing.

The susceptor-assisted microwave just mentioned belongs to the intrinsic microwave heating because preheating is based on the interaction of microwaves and susceptors. For extrinsic hybrid microwave annealing, it requires a secondary energy source, such as an infrared heating element used in conjunction with microwave annealing. Both intrinsic and extrinsic auxiliary heating help to increase the temperature, and they change the dielectric properties of the material, thereby enabling the material to absorb microwave energy.

Therefore, unlike the conventional thermal-based annealing approach, which relies

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only on conductive/radiative heating for temperature control, our goal for the susceptor design in the Microwave cavity is to achieve an optimum configuration for dopant activation at a temperature below 700 °*C*. An upper-temperature limit is required because dopants readily diffuse at temperatures above 700 °*C*.

This is achieved by varying designs and configurations of the susceptor and carefully optimizing the susceptor loss factors, area, and distance from the sample. The microwave annealing module including nine Magnetrons, and each magnetron has a corresponding wave guide to guide EM waves into the microwave cavity (Figure 10(a)). Inside the cavity is a folder to fold the various susceptor setups into one or multiple pieces with coupon samples sitting on it. Before, during, and post the microwave annealing process, the N2 gas is used for pre-purge, process gas, and post-purge, as depicted in Figure 10(b). Figure 10(c) shows the typical temperature vs. process time plot.

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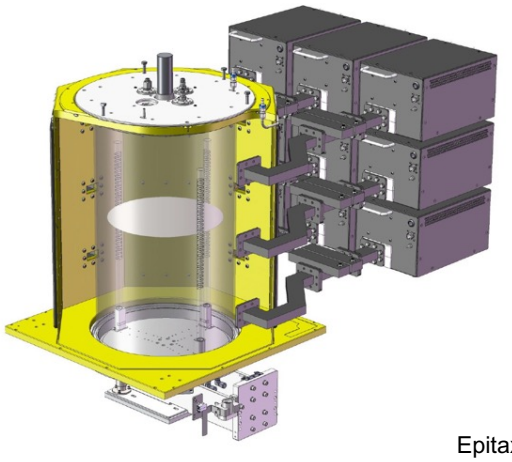
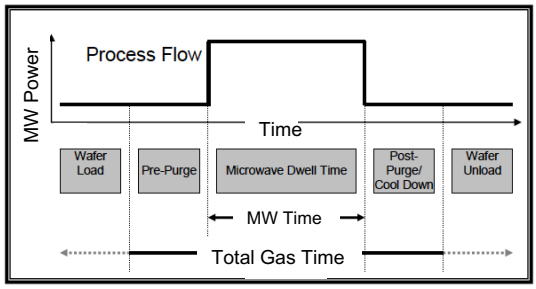
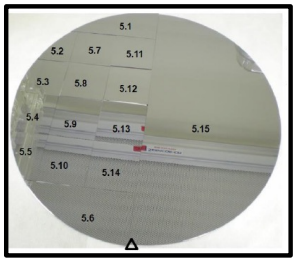
(a)



(b)



Epitaxial Si:P with
[P] 3 x 10^{21} at./cm^3



Run	Sample	Process Pressure	Purge Time	Pre-Purge Ambient	Process Ambient	Ramp Up/Down	Unload Temp
9 => 13	Pieces	ATM	300 sec	N2 5 SLM	N2 5 SLM	None	150 C

(C)

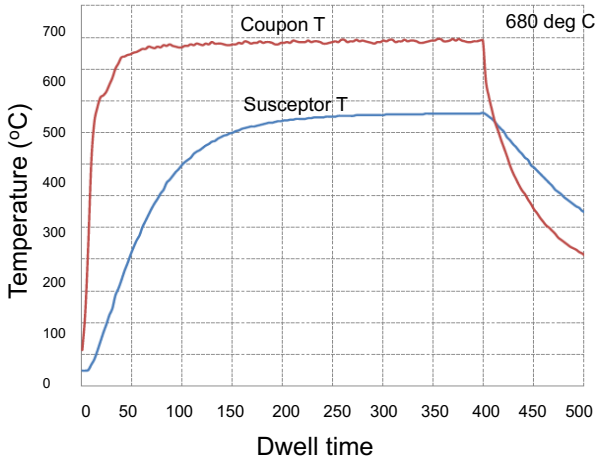


Figure 5.10 Microwave annealing process, (a) Microwave annealing modules, nice magnetron, and the corresponding wave guide are shown, (b) The N2 ambient gas used in the annealing process, (c) The typical temperature vs. dwell time of microwave annealing process.

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Among all configurations explored (see Figure 11) in the 1st trial run, the best anneal conditions were achieved using a triple-parallel-susceptor (TPS) setup. The design intent of such TPS configuration is twofold: firstly, to create an intensified oscillating E field in between susceptors, where the field is maximum between the boundaries of top and bottom susceptors; and secondly, to alter the temperature of the sample; which are two keys to achieve the threshold of effective energy coupling with inactive dopant structures in Si:P film.

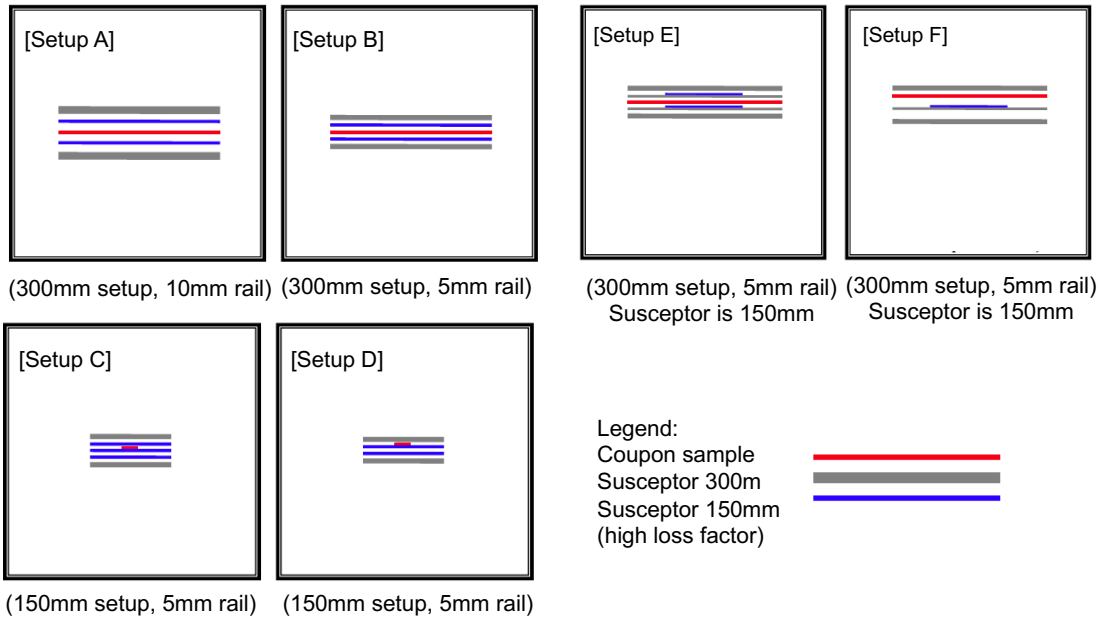

Figure 5.11 First trial run of the MWA cavity setup. A, B, and C-type susceptors have different area sizes and impurity doping degrees. Susceptors and samples of various sizes have undergone trial runs.

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Coupon	Configuration Susceptor	MW (%/sec)	Coupon T	Rs Pre	Rs post	MW reaction
HCKZA060TMB2	A 300mm/10mm	800/300	584.6	224	237	weak
HCKZA058TMB2	A 300mm/10mm	800/1200	619.4	228	248	weak
BFQ0T243SJC3	A 300mm/10mm	800/300	593	413	426	weak
BFQ0T242SJC1	A 300mm/10mm	800/1200	620.6	431	433	weak
HCKZA051TMB0	B 300mm/5 mm	800/300	624.2	232	246	weak
FDKUD100TMA0	B 300mm/5 mm	800/1200	633.8	239	255	weak
BFQ0T241SJF2	B 300mm/5 mm	800/300	629	427	423	weak
BFQ0T240SJB0	B 300mm/5 mm	800/1200	633.8	415	429	weak
5.9	C 150mm/5mm	700/60	529.4	260	246	weak
5.1	**C 150mm/5mm**	**700/90**	**589.4**	**253**	**169**	**Significant**
5.11	**C 150mm/5mm**	**700/120**	**625.4**	**254**	**147**	**Significant**
5.7	**C 150mm/5mm**	**700/300**	**669.8**	**235**	**91**	**Significant**
5.8	D 150mm/5mm	700/300	659	248	187	medium
HCKZA060TMB2	E 150mm/5mm	700/300	656.6	236	192	medium

Table 5.1 First microwave annealing (MWA) trial run results. A, B, C type susceptors are different in area size and impurity doping level. C-type susceptor of 150 mm and a sample-to-susceptor distance of 5 mm provided the best interaction with microwaves, as Rs before and after MWA showed the most significant changes.

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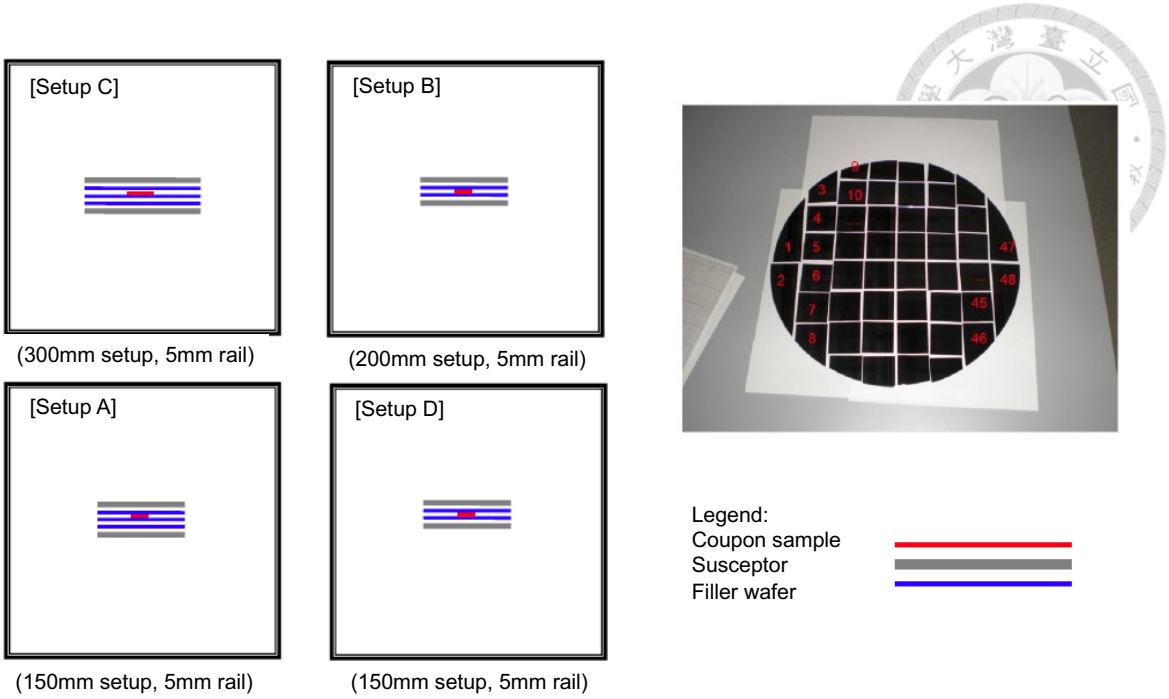

Figure 5.12 Second trial run MWA cavity setup. Use only C-bases of different area sizes. Samples are placed on pedestals of different area sizes. Also shows the area size of the test sample.

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Coupon	Configuration Susceptor	MW (%/sec)	Coupon T	Rs Pre	Rs post	MW reaction
S3-11	C 300mm	700/90	523.4	226	221	Weak
S3-13	C 300mm	700/120	571.4	240	232	Weak
S3-14	C 300mm	700/150	606.2	231	220	Weak
S3-19	C 300mm	700/180	620.6	245	231	Weak
S3-20	C 300mm	700/210	641	240	226	Weak
S3-21	C 300mm	700/300	657.8	232	215	Weak
S3-22	B 200mm	700/90	542.6	229	224	Significant
S3-27	B 200mm	700/150	615.8	247	196	Significant
S3-28	B 200mm	700/300	666.2	228	133	Significant
S3-29	**C 150mm**	**700/90**	**591.8**	**231**	**162**	**Significant**
S3-30	**C 150mm**	**700/150**	**651.8**	**242**	**131**	**Significant**
S3-35	**C150mm**	**700/300**	**677**	**234**	**91**	**Significant**
S3-36	D 150mm	700/90	596.6	235	225	Weak
S3-37	D 150mm	700/150	649.4	243	204	Weak
S3-38	C 150mm	600/90	570.2	239	201	Weak
S3-18	**C 150mm**	**600/150**	**631.4**	**225**	**162**	**Significant**
S3-26	**C 150mm**	**600/300**	**659**	**225**	**119**	**Significant**

Table 5.2 Second trial run MWA results. The results confirmed that a C-type susceptor of 150 mm and a sample-to-susceptor distance of 5 mm were revalidated to provide the best interaction with microwaves, as Rs before and after MWA showed the most significant changes.

The first and the second trial runs by varying the susceptor design, including the susceptor loss factor, the size of the area, and its distance from the sample. Our trial-and-error approach to annealing conditions concluded that using a unique triple-parallel pedestal configuration with a 5mm spacing design was optimal for the SiP layer-microwave interaction, as shown in Figure 5.13.

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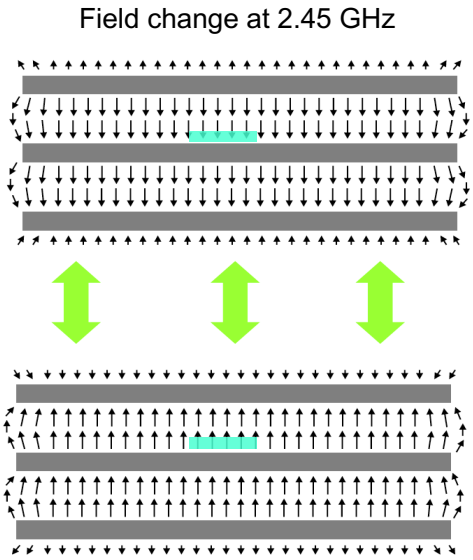

Figure 5.13 Optimized microwave cavity setup for activation of heavily doped Si:P dopants. The sample sits in a triple-parallel-susceptor is shown.

The interaction of epitaxial Si:P layers with microwaves is clearly affected by various susceptor settings and sample configurations. This can be judged from the change of resistance value before and after microwave annealing as shown in Table 5.1 and Table 5.2. This can be inferred by letting the epitaxial Si:P layer interact directly with microwaves without using a susceptor. In this case, the Si-substrate supported Si:P layer cannot show interaction with microwaves due to the low loss factor of the Si substrate. This has been verified in our earlier experiments. However, even when placing a specimen sample on a single susceptor, it still does not cause too significant interaction for the following reasons. For a single susceptor, even though it can increase the loss factor of the Si:P sample by susceptor-assisted heating, the E-field concentration distribution over the sample is still not effectively enhanced. Thus the E-field energy cannot be effectively coupled with the inactive donor structures in the Si:P layer. The first run of susceotir configuration D revealed a weakness like this.

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Furthermore, a single susceptor creates a fundamental problem of inhomogeneity of eddy current induction. This comes from the fact that once the susceptor preheats the Si:P layer, it becomes more conductive and the interaction with microwaves becomes more conductive heating dominated, which can cause eddy currents to build up at the edges of the sample resulting in uneven heating. With a triple parallel inductor configuration, the eddy current-induced non-uniformity that occurs in a single susceptor configuration (Figure 5.14) can be resolved by a vertical oscillating field (Figure 5.15). However, significant microwave interactions with Si:P samples cannot be guaranteed even with a triple-parallel-susceptors configuration. This is due to the following reasons. First, the doping level in the susceptor not only affects the conductivity of the susceptor, leading to dielectric heating or Joule heating (conduction heating) dominated effects and affects the susceptor and sample temperature. In addition, it also affects the capacitive oscillation E-field established between the susceptors (Figure 5.15). The specific doping in the C-type susceptor shows its clear advantage in energy coupling, as it can show the most pronounced microwave interaction with Si:P at an optimal susceptor-to-sensor spacing of 5 mm as compared with other susceptor configurations. Two trial runs have verified this (Figure 5.11 and Figure 5.12). Finally, it is unclear why sample and susceptor area sizes also play an important role in microwave interactions. This study suspects that the size of the base/sample area within 300mm may affect the base heating temperature due to radiation loss. This needs to be further investigated in future research work.

Then, through the boundary conditions formed by the cavity and the susceptor, the simulation results of the electric field between the susceptors are obtained. It is confirmed that the triple-parallel-layer susceptor configuration is indeed conducive to establishing an effective electric field distribution for microwaves and Si:P layers to be effective energy coupling.

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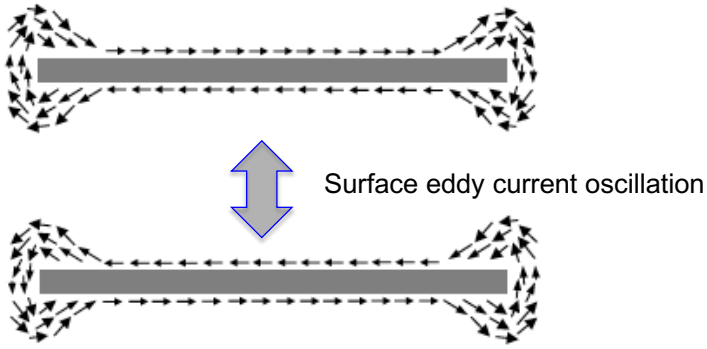

Figure 5.14 Single susceptor configuration, Surface eddy currents are generated by conductive Si:P layers placed on a single susceptor configuration. When Si:P becomes more conductive by indirect or direct heating, it will reach a conductive heating regime and induce surface eddy currents.

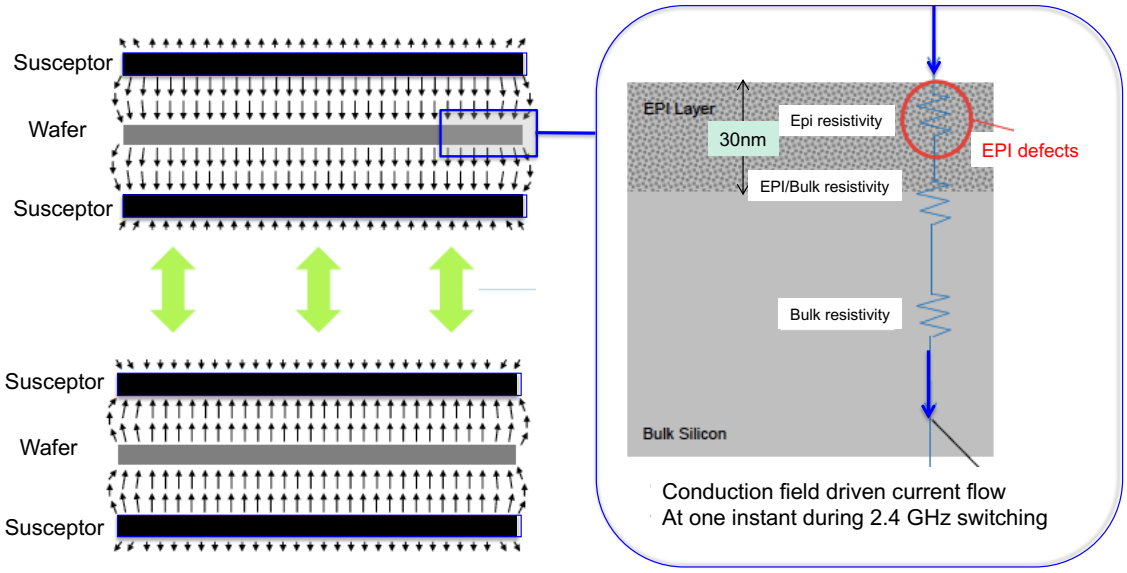

Figure 5.15 Capacitive oscillatory fields established between triple parallel susceptor configurations. During switching at 2.45 GHz, the conducted field drives the current to flow for an instant.

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5.5 Simulation of the electric field distribution in the cavity

The simulation of the E-field distribution in the microwave cavity is based on collaborative work with Professor James C Hwang and his team at Cornell University. The simulation results shown in section 5.5 and 5.6 were reproduced from [Tsai, C. H., Savant, C. P., Asadi, M. J., Lin, Y. M., Santos, I., Hsu, Y. H., ... & Hwang, J. C. (2022). Efficient and stable activation by microwave annealing of nanosheet silicon doped with phosphorus above its solubility limit. Applied Physics Letters, 121(5), 052103.] [188], with the permission of AIP Publishing". As previously described, This work obtained optimal annealing conditions by trial and error by varying different susceptor designs, including susceptor loss factor, area size, and distance from the sample. I thus decided to use a unique triple-parallel-susceptor configuration for the best microwave annealing conditions. The optimal design and use of the optimal susceptor spacing of 5mm are shown in Figure 5.16(a) [188]. This optimal design of the susceptor configuration in the microwave cavity was used for dopant activation below 700 $^{\circ}C$ to avoid excessive diffusion. The microwave field distribution within the cavity was simulated by full-wave electromagnetic modeling using a commercial software package (COMSOL Multiphysics Modeling Software31,32) to assess the importance of the susceptor design for microwave interactions. As shown in Figure 5.16(b) [188], The simulation results fond that the lowest standing wave of microwave radiation exists around 12.241 GHz, corresponding to the 5th harmonic of the 2.45 GHz baseline frequency. At this frequency, the electric field is highly concentrated within the susceptor gap, and its amplitude is 100 times greater than outside the susceptor gap. Notably, the optimal inter-susceptor distance is frequency dependent and is critical for optimal field strength within the receptor. As shown in Figure 16(b), the field distribution of the 5th harmonic in the cavity changes dramatically when

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the fundamental microwave frequency is moved away from 2.45 GHz (Figure 5.16(c)). This optimized susceptor configuration is critical to achieve dopant activation performance comparable to state-of-the-art high temperature (>1100°C) MSA processes, but at a much lower background temperature than MSA, below 700°C.

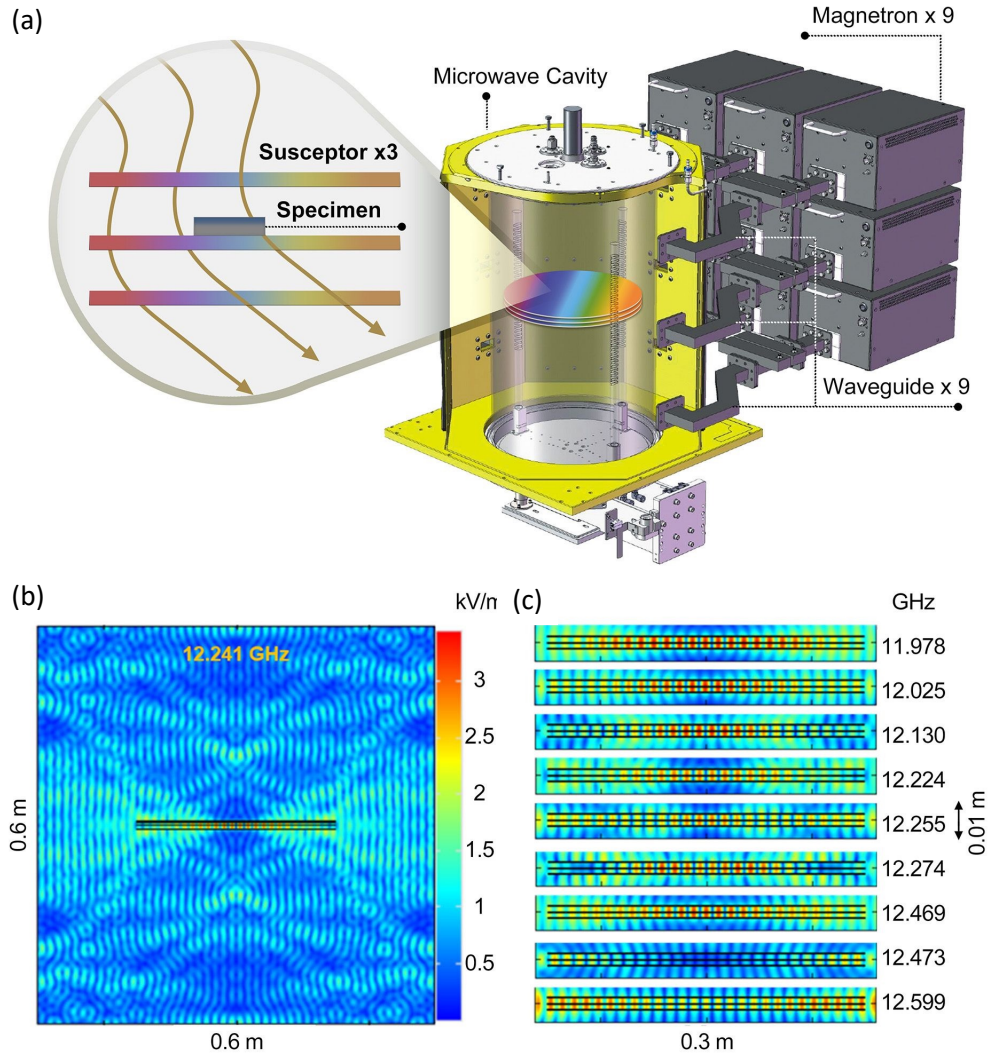

Figure 5.16 Optimization of susceptor setup in microwave cavity, (a). Optimized triple parallel base setup with 5mm spacing between them, (b). E-field distribution for resonance at 12.241 GHz (5th harmonic of 2.45 GHz), (c). E-field distribution for eigenmodes around 12.241 GHz [188].

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5.6 Selective dopant activation phenomena

Chapter 3 demonstrates the activation of Si:P dopants by microwave annealing results in equivalent dopant activation by MSA annealing with excellent thermal stability. Chapter 4 demonstrates the existence of dipole moments for unstable donor vacancy clusters using ab initio calculations. In this chapter, using simulations it is known that the field distribution between the susceptors is a standing wave distribution caused by resonant waves. Based on all this valuable information, experiments were conducted to identify the selective coupling of microwave energy indeed causes the dopant activation observed during microwave annealing to polar and inactive P_nV structures within the lattice.

To examine the selective dopant activation effect of susceptor-assisted MWA annealing, epitaxial Si:P films at a high doping limit ([P]= 3 x 10^{21} at./cm^3, as-deposited thickness = 30nm) were used for the investigation of ultra-shallow junctions properties. Figure 5.17(a) shows sheet resistance and junction depth, as determined by high-resolution SIMS profile (Figure 5.17(b)), of the Si:P film under various TPS-MWA anneal conditions, including MSA as reference. The standard four-point probe method measures sheet resistance (Rsh). The junction depths (X_j), defined at a dopant concentration of 1.0x10^{20} /cm3, show that the dopant diffusion was insignificant (i.e. below 5nm at 15kW) for MWA conditions explored here. The junction abruptness is 3.9 to 5nm/dec, calculated by the slope between 1.0x10^{21} to 1.0x10^{20} at./cm^3, comparable to the MSA process. The above results show that a susceptor-assisted MWA process can achieve the same excellent dopant profile control using state of a art MSA process.

It is worth noting that the shallow junction achieved by either MWA or MSA as demonstrated in Figure 5.17(a) is especially attractive for aggressive device scaling,

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which requires lower R_{sh} for a given X_j [188]. Figure 5.17(a) shows that MWA process of 12kW matches the R_{sh}-X_j performance of the MSA process, whereas the microwave power setting of 15kW achieved a lower R_{sh} but with a slightly extra dopant diffusion. For a given X_j, it was observed that MWA could achieve lower R_{sh} than from the MSA process. The R_{sh}-X_j advantage offers an annealing solution for scaled nano-devices such as nanowire and nano sheet where dopant activation is needed under a limited thermal budget.

To understand the microwave interactions with electrically inactive P dopants, HRXRD measurements were carried out on the Si:P sample to study the tensile strain evolution in epitaxial Si:P films, particularly in the form of P_nV clusters (n = 1, 2, 3 or 4),. Earlier research showed that the tensile stress developed in the Si:P layer is actually due to the donor vacancy cluster P_4V structures in Si lattice [189]. In general, the strain results from a lattice mismatch and can be contributed by other P_nV clusters. The XRD patterns of the heavily doped Si:P layers after different thermal annealing are shown in Fig. 5.17(c). This indicates that the peak shifts to lower 2theta after MWA annealing, i.e. closer to the maximum peak of Si, which indicates a reduction in tensile strain. Compared to MSA-treated samples, the MWA sample exhibits more strain relaxation (see Fig. 5.17(c)) [188], suggesting even without increasing the thermal energy. Microwave energy can efficiently couple to energy modes within the inactive lattice structure in Si:P, leading to dopant activation. Annealing at a higher MWA power can increase activation, as indicated by more pronounced strain reductions from the XRD intensity peak shift.

It has been observed that activation in an epitaxial Si:P sample is typically associated with the dissolution of P_nV clusters, and this can be characterized by positron annihilation spectroscopy (PAS) [190]-[192]. In PAS, the S-W plot allows the identification of the annihilation sites. S-parameters are spectral features produced by annihilating positrons

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and valence electrons from vacancy defects. It represents the main shape of the spectrum. Vacancy defects with higher electron density appear with narrower spectra. So the width of the S-parameter distribution can represent the DnV distribution. On the other hand, the W parameter represents the spectral wing that annihilates the core electron. Figure 5.17(d) compares a S-W plot for as-deposited and MWA annealed Si:P samples [188]. The MWA sample showed a lower S value at the S-W turning point, indicating a reduction of vacancy defects in Si:P layer. This result agreed with similar S-parameter reduction in Si:P by applying laser annealing as reported by Dhayalan et al [193]. This indicates that although the background lattice temperature of the MWA process 680 °C was much lower than that of the MSA process 1150 °C, effective dopant activation can occur through the dopant-vacancy cluster dissolution process.

The predicted thermal stability was verified by subjecting the post-MWA and post-MSA annealed Si:P samples to various RTA thermal budgets with respect to the same 300 sec dwell time. The resistivity changes before and after RTA annealing determined the amount of the dopant deactivation. As shown in Figure 5.18(a), the post-MWA annealed samples exhibited relatively small and stable resistivity changes after experiencing a thermal budget of 600 to 700 °C for 300 s. Whereas for the samples annealed via high temperature and very short time MSA, the resistivity change increases monotonically with increasing thermal budget from 600 to 700 °C. At 700 °C the sample reaches the maximum resistivity change and dopant deactivation. (Figure 5.18(b)) [188]. The above observations support the hypothesis that the superior thermal stability features after MWA annealing are due to a different P_nV distribution dominated by the P_4V. Based on the positron lifetime spectroscopy experiment [194]-[197], it was shown that P_nV (n=1-3) vacancy clusters start to form above 800K (~ 530 °C). Still, these clusters become unstable and dissociate when temperature increase above 1000 K (730 °C). In the first

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order, this explains the resistivity change observed in MSA sample during subsequent RTA thermal. The resistivity rise around ~ 600 °C and reach Rs maximum at ~ 700 °C due to dopant deactivation (P_nV formation) [194]-[197]. The resistivity decreases when anneal temperature exceeds 700 °C because of the re-activation from P_nV dissociation. However, MWA samples exhibit much less resistivity increase than the MSA counterpart up to 700 °C, indicating inhibited formation of P_nV cluster and a more stable P-dopant configuration.

In the selective dopant activation process as demonstrated above, the average temperature of samples was maintained at 680 °C, which can be attributed to the background dielectric heating within bulk. Obviously, this background temperature cannot account for the observed dopant activation. Efficient microwave energy coupling must exist to explain the achieved dopant activation that could match or outperform MSA. Since a long microwave wavelength at 10 cm meter means it is weak in photon energy (~ 10^{-5} eV) and cannot directly break covalent bonds within donor vacancy cluster. Therefore the non-vanishing dipole moment of P_nV could mediate the interaction with microwave. The efficient microwave energy transfer possibly relies on the dipole resonant coupling of the external electric field to a lattice mode of the polar-P_nV clusters.

In conclusion, this work has demonstrated that the direct energy coupling effects during microwave annealing can be achieved with the assistance of an optimal triple-parallel pedestal setup and optimal sample configuration. This work proposed a selective dopant activation model to explain the efficient dopant activation achieved at a low temperature of 680 °C. At a background temperature of 680 °C, an athermal direct energy coupling effect exists between the microwave and the inactive dopant structure. The unstable deactivated dopant structure $P_{1\text{-}3}V$ carries a non-vanishing dipole moment and acts as a media for microwave direct energy. The activation thus achieved is only in the presence

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of a P_4V-dominated distribution of P_nV. Thus, it exhibits excellent thermal stability, as the precursors $P_{1\text{-}3}V$, which are required for P_nV clustering kinetics, have mostly been annealed by selective activation. By ab initio calculations, theoretical evidence is provided for the existence of a non-vanishing dipole moment in P_nV. Furthermore, by providing HRXRD and PAS evidence, the microwave energy coupling of P_nV with non-vanishing dipole moment is supportive. Therefore, it is believe that the discovery of selective dopant activation is a new milestone that brings dopant activation from traditional hot alkaline annealing into another entirely new era.

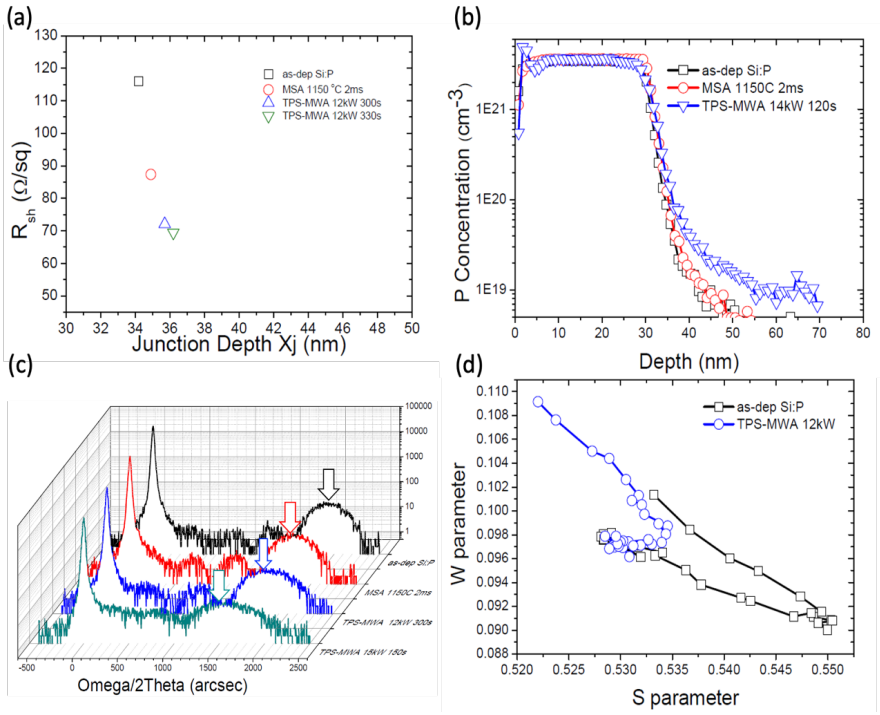

Figure 5.17 Dopant activation characterization. (a) Rsh-Xj plot of epitaxial Si:P film under various annealing conditions and (b) The corresponding Phosphorus SIMS profile in the epitaxial Si:P film. (c) HRXRD curves of epitaxial Si:P film annealed under various annealing conditions. (d) Vacancy defect state of S-W plot with positron energy as a running parameter for as-deposited Si:P and MWA annealed samples. The sharp turning point shifts to a smaller S-parameter value indicating a decrease in dopant vacancy clusters (P_nV) [188].

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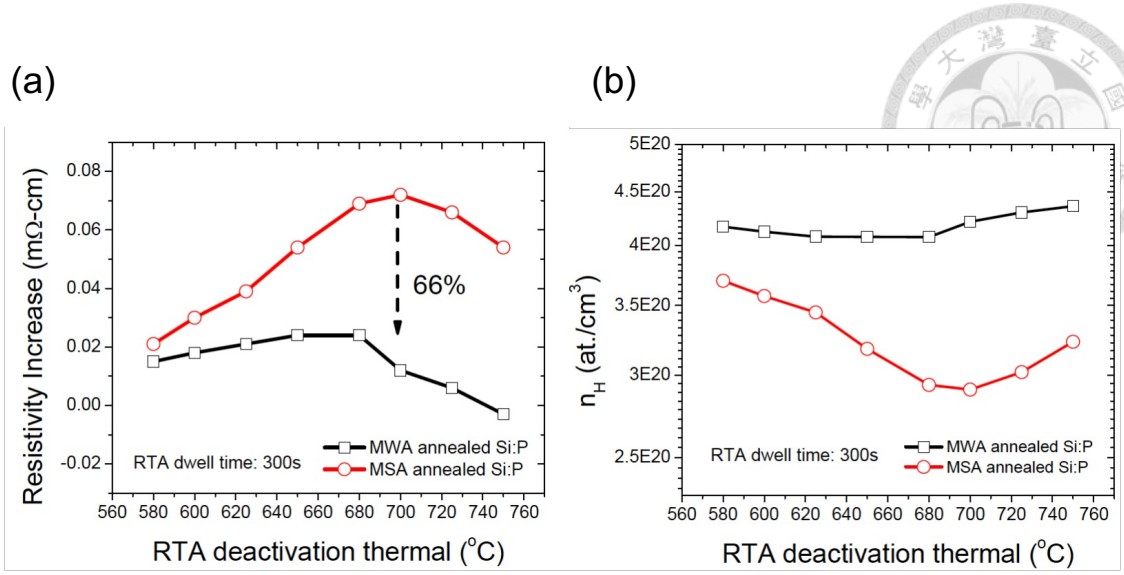

Figure 5.18 Characterization of dopant deactivation by (a) resistivity change and (b) free carrier concentration as a function of RTA temperature [188].

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Chapter 6 Conclusion

6.1 Summary of research work

In conclusion, this study presents that the fundamental donor deactivation issue created by a thermal base annealing (e.g., state-of-the-art millisecond annealing (MSA, LSA) is due to the kinetic limitation of dopant cluster defect activation. The dopant activation is accompanied by unstable dopant cluster defects generation. The unstable defects residues in post-MSA annealed samples could play a precursor role for further deactivation by turning into the thermodynamically favored donor-vacancy defects configuration upon subsequent moderate thermal budget. This deactivation phenomenon is nearly universal and exists in both MSA annealed and as-grown heavily n-doped Si. As a contrast, the innovation of selective dopant activation through a microwave-dopant defect direct energy coupling could effectively control the unstable defects distribution and resolve the typical donor deactivation issue. This work has demonstrated that by enabling optimal susceptor and sample configurations, the MWA process enables us to obtain unique interactions with in situ doped epitaxial Si:P layers at an unprecedented temperature range for semiconductor applications below 700 °C. For the first time, susceptor-assisted MWA provided the desired R_{sh}-X_j performance beyond the results of other MSA and RTA methods and effectively demonstrated donor deactivation inhibition. In this work, a model based on clusters of donor vacancies (DnVs) was proposed to explain the experimental results. Ab initio work by Prof. Lourdes found that low-order unstable donor vacancy clusters (P_nV, n=1-3) all have non-zero dipole moments, while the stable doped vacancy cluster P_4V has no dipole moment. Under selective microwave annealing, these unstable donor-vacancies clusters (P_nV, n=1-3) are eliminated by annealing and dissociation, resulting in a specific distribution of inactive donor structures

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dominated by clusters of higher-order and stable dopant vacancies (P_4V). Due to the elimination of the unstable P_nV(n = 1-3) cluster mediator factor, these thermally stable P_4V-dominated inactive donor structures impose a greater constraint on the kinetics required to form P_nV clusters (n = 1-4). It ultimately achieves thermal stability breakthrough of heavily n-doped Si. This suggests that eliminating the unstable donor vacancy cluster ($P_{1-3}V$) distribution within the heavily n-doped silicon layer is critical for overcoming typical donor deactivation problems and achieving stable junctions. Figure 6.1 summarizes and describes the kinetic and thermodynamic differences in dopant activation for selective microwave annealing (MWA) and millisecond annealing (MSA) for heavily doped epitaxial SiP. Finally, this study concludes that the phenomenon of donor inactivation inhibition observed in this work is not limited to phosphorus in Si. This selective dopant activation discovery should apply to all n-type doping (As, Sb) and other materials besides Si semiconductors, such as Ge and SiGe. According to the PRL and PRB literature, As and Sb donor inactivation follows a similar donor vacancy clustering model. The kinetics of D_nV clustering and the thermodynamics of D_nV formation are the same.

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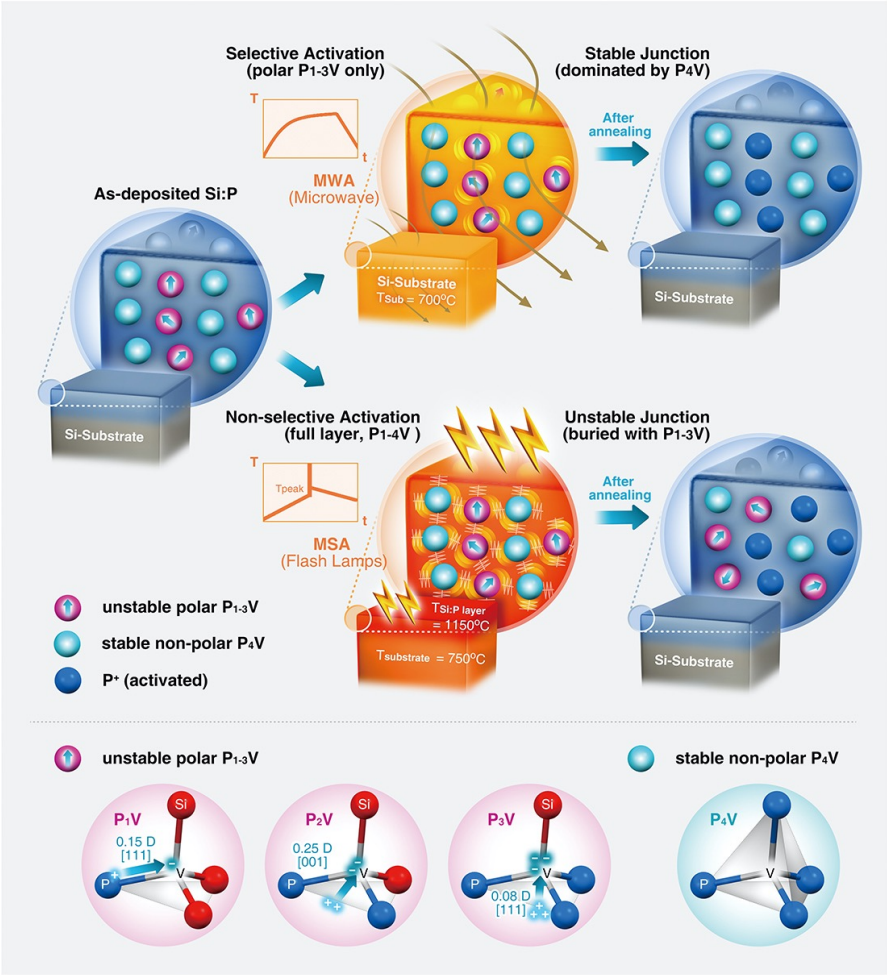

Figure 6.1 Kinetic differences in dopant activation during and after selective microwave annealing (MWA) and millisecond annealing (MSA) Kinetic differences in dopant activation during and after selective microwave annealing (MWA) and millisecond annealing (MSA)

6.2 Future work

After a lengthy trial and error in this study, it was able to find the optimal susceptor configuration to achieve the phenomenon of selective dopant activation in highly n-doped Si. However, during MWA annealing, the microwave energy is coupled not only to the polar P_nVs, but also to the heated Si lattice structure through dielectric heating, resulting in the substrate background temperature. In our cavity and susceptor setup and microwave

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power range around 12-15 kW, the optimal dopant activation temperature is limited to 700 °*C*, because annealing at temperatures above 700 °*C* may cause unwanted dopant diffusion and enhance the kinetics of D_nV re-clustering. This suggests that improving the selectivity of the coupling of microwave energy to the P_nV and Si lattices is required to enable dopants at lower temperatures below 700 °C if the activation and thermal stability of the dopants are to be further improved. This may require a redesign of the microwave cavity using optimized susceptor materials and configurations to generate alternating standing wave distributions that improve the energy coupling efficiency between microwave energy and inactive donor vacancy clusters. Furthermore, This work has not yet understood the threshold condition for microwaves to efficiently couple to the non-vanishing dipoles of D_nV. This requires more theoretical research to reveal more of the physics behind it.

On the other hand, in the local vibration mode (LVM) study, the simulation results show that in the frequency intervals 5.5-5.75 THz and 10.6-10.8 THz, there are LVMs in all P_nV clusters (n=1-3), which are aligned with their net dipole moments. However, the microwave frequency range used in this work is 2.45 GHz, so a direct resonant interaction between the 2.45 GHz microwave and the LVM is unlikely. Furthermore, other energy couplings, such as rotational and translational modes, are impossible due to the solid material nature. In other words, the dipole moment-microwave coupling can be considered the main interaction in the MWA process. Therefore, this work supports the notion that athermal interactions other than local vibrational modes exist in the silicon lattice to achieve dipole resonance coupling with microwaves. A more detailed study of the properties of this resonant mode or the alternative non-thermal microwave effect remains to be explored for future research work.

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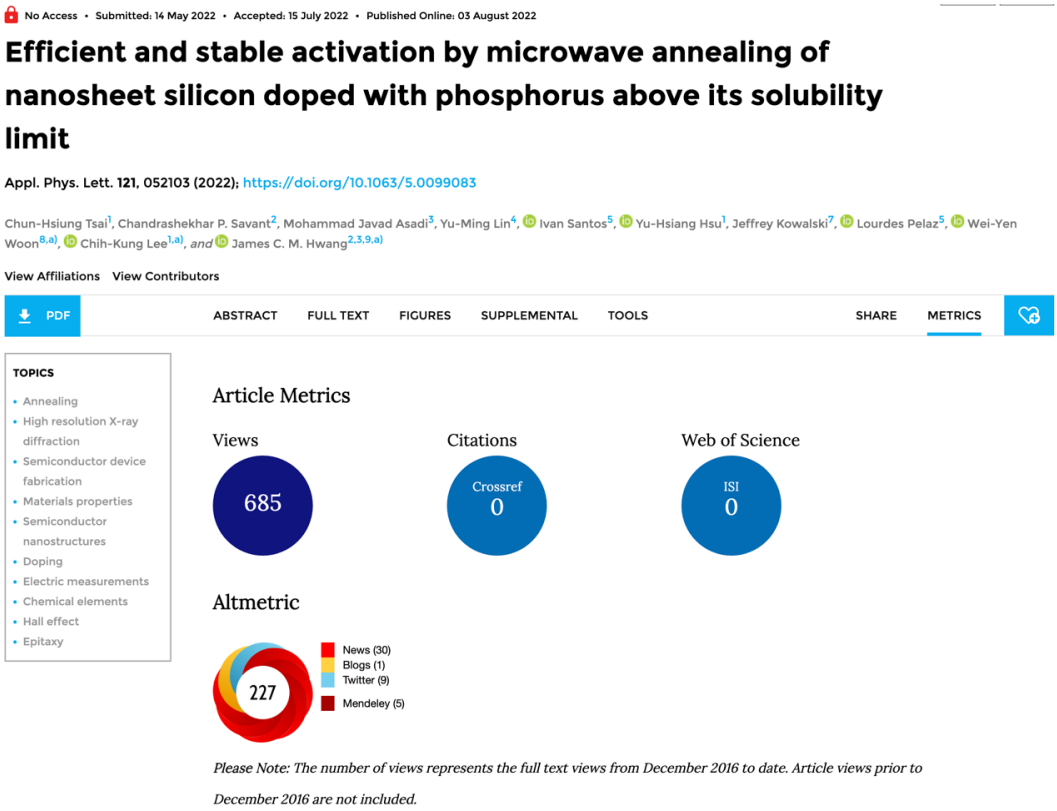

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Efficient and stable activation by microwave annealing of nanosheet silicon doped with phosphorus above its solubility limit

Appl. Phys. Lett. **121**, 052103 (2022); https://doi.org/10.1063/5.0099083

Chun-Hsiung Tsai[1], Chandrashekhar P. Savant[2], Mohammad Javad Asadi[3], Yu-Ming Lin[4], Ivan Santos[5], Yu-Hsiang Hsu[1], Jeffrey Kowalski[7], Lourdes Pelaz[5], Wei-Yen Woon[8,a)], Chih-Kung Lee[1,a)], *and* James C. M. Hwang[2,3,9,a)]

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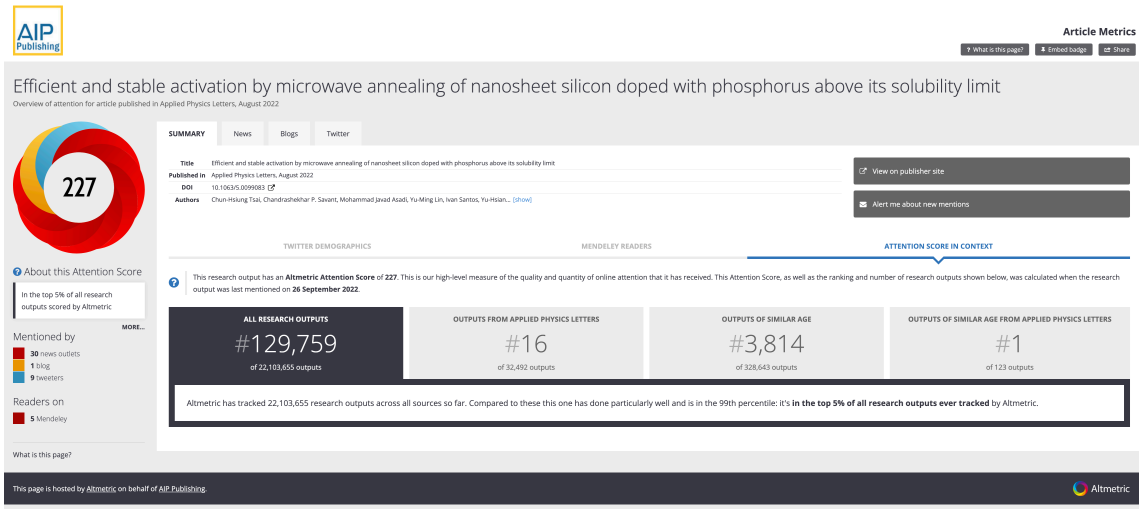

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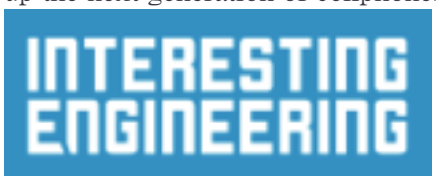

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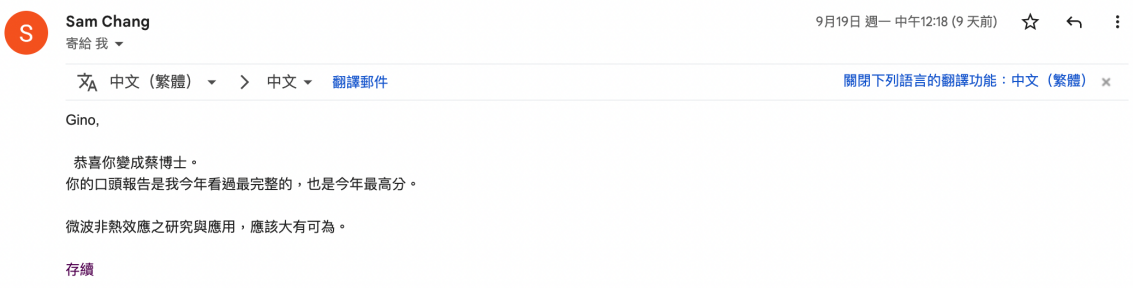

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