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Master Thesis

高頻氮化鋁銦鎵/氮化鎵高電子遷移率電晶體之模擬分析與優化

Simulation analysis and optimization of high-frequency AlInGaN/GaN HEMTs

劉昀皓

Yun-Hao Liu

指導教授: 吳育任 博士

Advisor: Yuh-Renn Wu Ph.D.

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摘要

在本篇論文中，透過分析實驗已有的氮化鎵氮化鋁鎵之高電子遷移率電晶體的數據，提出優化的磊晶結構及元件表現。在分析實驗數據中，發現元件的二維電子氣濃度與短通道效應以及 T 型閘極的電容效應會限制元件的操作頻率。由於氮化鋁銦鎵作為元件能障層能產生較大的二維電子氣同時避免晶格不匹配，因此我們透過模擬不同氮化鋁銦鎵的組成，找出在晶格不匹配影響較小下能提供最高二維電子濃度的組成。而短通道效應的問題我們採用縮短元件通道的厚度以及氮化鋁鎵背屏障層來提升閘極對通道的控制。T 型閘極的電容效應我們藉由改善 T 型閘極結構與鈍化層來降低。根據以上方法，我們提出了優化後的磊晶結構。在結果中，透過模擬我們提出的磊晶結構，找出在閘極長度為 60 奈米時，元件能有最高 f_T，並討論接觸電阻與薄膜電阻的影響，以及分析不同介電系數的鈍化層在高頻元件的應用。最後，我們通過模擬評估元件能達到 f_T/f_{max} 為 186/339 GHz 在閘極長度為 60 奈米。

關鍵字：氮化鎵、高電子遷移率電晶體、背屏障層 、氮化鋁銦鎵、高頻元件

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Abstract

This paper proposes the optimized epitaxial structure and device performance by analyzing the experimental data of AlGaN/GaN high electron mobility transistors (HEMTs). In analyzing the experimental data, it is found that the two-dimensional electron gas (2DEG) density, the short-channel effects of the device, and the capacitance effect of the T-type gate limit the operating frequency of the device. Since AlInGaN as a device energy barrier layer can generate more two-dimensional electron gas and avoid lattice mismatch. Therefore, by simulating different compositions of AlInGaN, we find the composition that provides the highest 2DEG with less effect of lattice mismatch. For the problem of the short channel effect, we use shrinking the thickness of the device channel and the AlGaN back barrier to improving the gate-to-channel control. The capacitance effect of the T-gate is reduced by improving the T-gate structure and passivation layer. According to the above methods, we propose an optimized epitaxial structure. In the results, by simulating our proposed epitaxial structure, it is found that the device can have the best f_T

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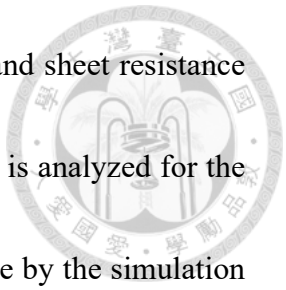

when the gate length is 60 nm. The influence of contact resistance and sheet resistance is discussed. The passivation layer with different dielectric constants is analyzed for the application of high-frequency devices. Finally, we evaluate the device by the simulation to achieve f_T/f_{max} 186/339 GHz at a gate length of 60 nm.

Keywords: GaN, High electron mobility transistor, Back barrier, AlInGaN, High frequency device.

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Chapter 1

Introduction

1.1 Background

In recent years, with the increasing development of the high-tech industry, the progress of communication technology is changing with each passing day, and it also covers most of human life. The general level includes smart cities, transportation, etc., and the personal level has work, intelligent life, leisure, etc. However, the current technology is still unable to satisfy human beings. For example, automatic driving of vehicles on flat roads will require a large amount of road data. At this time, the transmission speed of the communication network will play a vital role. The network transmission speed is fast enough. Only then can the vehicle obtain enough information to drive on a flat road. Therefore, we must further develop communication technology and enter the era of 5G and 6G to make life more convenient in the future. The next-generation high-frequency 5G technology has gradually entered commercialization from the experimental stage, and wireless communication technology is developing toward higher speed and broader bandwidth. However, the mid-to-low frequency bands with more spectrum utilization are already quite crowded,

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so the mid-to-high frequency millimeter wave (mmWave) will be the trend of future development. Under the development trend of 5G, energy saving and higher frequency operating conditions are led, and the semiconductor materials used in power amplifiers have also changed. Wide Band Gap semiconductor materials silicon carbide (SiC) and gallium nitride (GaN) has leaped to the table because of their outstanding physical properties. Taking GaN as an example, this material has a large energy gap (3.4 eV), a collapse electric field (3.3 MV/cm), and a high thermal conductivity (1.3 W/cm-k), so GaN is more suitable for high-power components [14]. At the same time, due to the spontaneous polarization effect of the AlGaN/GaN heterojunction structure, a two-dimensional electron gas (2DEG) is formed at the junction, and its channel has extremely high electron concentration, electron mobility, and electron saturation. Therefore, GaN also has excellent development in high-frequency devices.

The application level of III-V compound semiconductors is widely used in radio frequency communication devices, high-power devices, optical devices, etc., have become the research field of the vigorous development of the semiconductor industry [15].

1.2 The property of GaN and the development status of GaN-HEMTs

Traditional semiconductor silicon (Si) and gallium arsenide (GaAs) are common materials for high frequency (3G, 4G) applications, but their breakdown field is smaller than GaN and SiC. As shown in 1.1, GaN and SiC can withstand a larger breakdown field and have a larger saturated velocity. Therefore, compared with Si and GaAs, if GaN and SiC are used, the performance of output power can be improved. Although SiC has better

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Table 1.1: Comparison of material properties [1, 12, 13].

Properties\Material	Si	GaAs	InP	SiC	GaN
Bandgap (E_g) (eV)	1.1	1.42	1.35	3.26	3.4
Electron mobility (cm^2/Vs)	1500	8500	5400	700	1000-2000
Saturated electron velocity ($10^7 cm/s$)	1	1.3	1	2	2.5
Breakdown field (MV/cm)	0.3	0.4	0.5	3	3.3
Thermal conductivity (W/cm·K)	1.5	0.5	0.7	3.7	1.3

thermal conductivity, the carrier mobility of SiC is low, and it is much more difficult in epitaxial technology. Compared with SiC, GaN is easier to form a heterojunction structure with other nitride alloys, thus making GaN easier to apply in the design of high electron mobility transistors (HEMTs).

Due to the wide bandgap properties of GaN, GaN devices have a lower intrinsic carrier concentration. Therefore, under high temperatures, the leakage current of GaN devices in reverse bias can be significantly smaller than that of Si devices. In addition, GaN also has good thermal conductivity. Therefore, GaN is very suitable as a high-power device material.

GaN is a wurtzite structure. It can be separated into Ga-face and N-face according to different growth methods. Figure 1.1 shows the schematic diagram of its structure. The advantage of GaN mainly lies in the special polarization effect of group-III nitrides, which can be divided into spontaneous polarization and piezoelectric polarization. When nitrogen and gallium atoms do not overlap to form a dipole due to the misalignment of the charge centers, and the polarization direction is determined by the surface atoms, it is a spontaneous polarization effect. On the other hand, when the group-III nitrides of the two heterostructures are stacked, a strain is generated in the upper layer due to lattice

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mismatch. When the lattice constant of the upper layer material is smaller than that of the lower layer, the tensile strain would be generated, and the polarization direction would be negative piezoelectric polarization. The schematic diagram of the structure is shown in figure 1.2. Due to the polarization difference, the spontaneous and piezoelectric polarization fields at the AlGaN/GaN heterostructure interface can generate the 2DEG, shown in figure 1.2. As shown in figure 1.3, when comparing the conduction band diagrams simulated with and without polarization, it is clear that polarization affects the behavior of AlGaN/GaN heterostructures. When considering polarizations, the heterojunction conduction band edge is positioned 0.25 eV below the Fermi level, resulting in an extremely high electron density. However, when polarizations are ignored, the conduction band energy at the heterojunction is 0.87 eV above the Fermi level, which is 1.12 eV high energy than in the case of incorporating polarizations. As a result, the electron density is zero at the heterojunction, meaning there is no 2DEG. It demonstrates that even in AlGaN/GaN heterostructures without a doped AlGaN layer, the effect of polarizations may result in the generation of high-density 2DEG. In the AlGaN/GaN heterostructure common to GaN-HEMTs, there is no need to fabricate regions of high doping concentration. Therefore, the effects of ionized scattering can be reduced to form channels with high concentration and mobility. High electron mobility, high breakdown field, and high output power make GaN a candidate for a new generation of high-frequency and high-power semiconductors.

GaN-HEMTs have significantly developed in recent years, and most use AlGaN as the barrier layer because the heterostructure epitaxial technology is relatively mature. However, the lattice mismatch between AlGaN and GaN makes it impossible to increase the polarization field of AlGaN/GaN by increasing the Al composition to increase the

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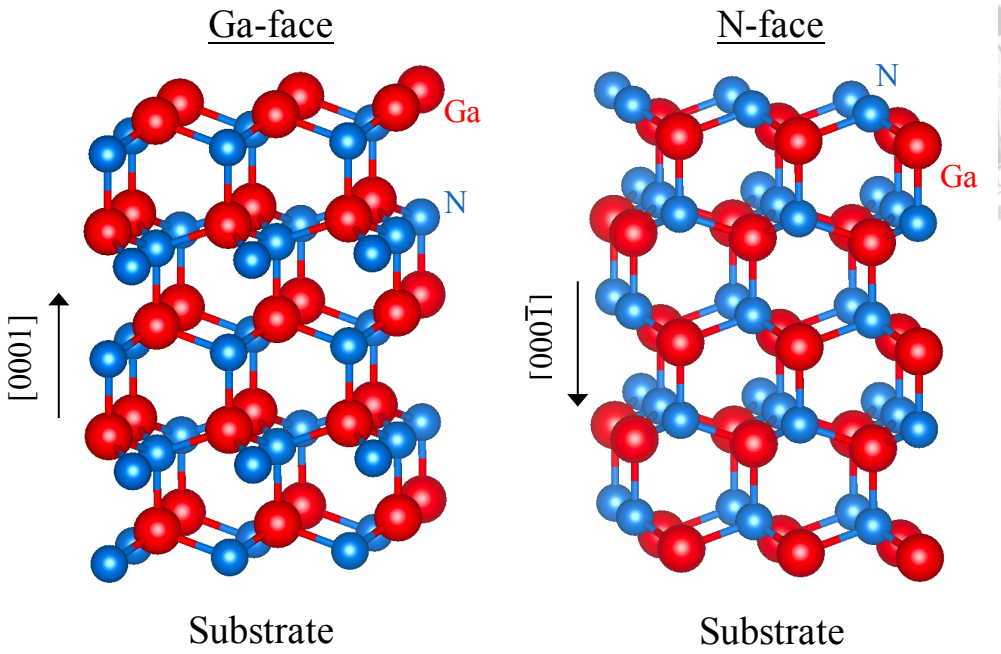

Figure 1.1: Different polarities (Ga- and N-faced) of wurtzite GaN [1].

2DEG concentration, so that the 2DEG concentration of the AlGaN/GaN heterostructure is limited. When the Al composition of AlGaN exceeds 30%, defects due to lattice mismatch may be a pivotal mechanism to degrade device characteristics. So thick enough AlGaN is needed to generate enough 2DEG. However, as the gate length of devices is scaled down to push higher operation frequency, the problem of short-channel effects(SCEs) becomes more severe. A thick AlGaN barrier layer would significantly reduce the gate control of the channel in the case of a short gate length. To overcome the lattice mismatch problem of AlGaN/GaN heterostructures, InAlN and InAlGaN have recently been investigated as new barrier layers because their spontaneous polarization is much higher, which can yield higher 2DEG density and allow thinner layers of barrier layer compared to AlGaN. Ronghua Wang et al. fabricated lattice-matched InAlN/AlN/GaN HEMTs on a SiC substrate, which achieved the f_T of 210 GHz with a 60 nm gate length [20]. However, compared to AlGaN/GaN HEMTs, the InAlN growth has a miscibility gap in the AlN-InN phase diagram [21], which results in lower mobility in the 2DEG due to higher

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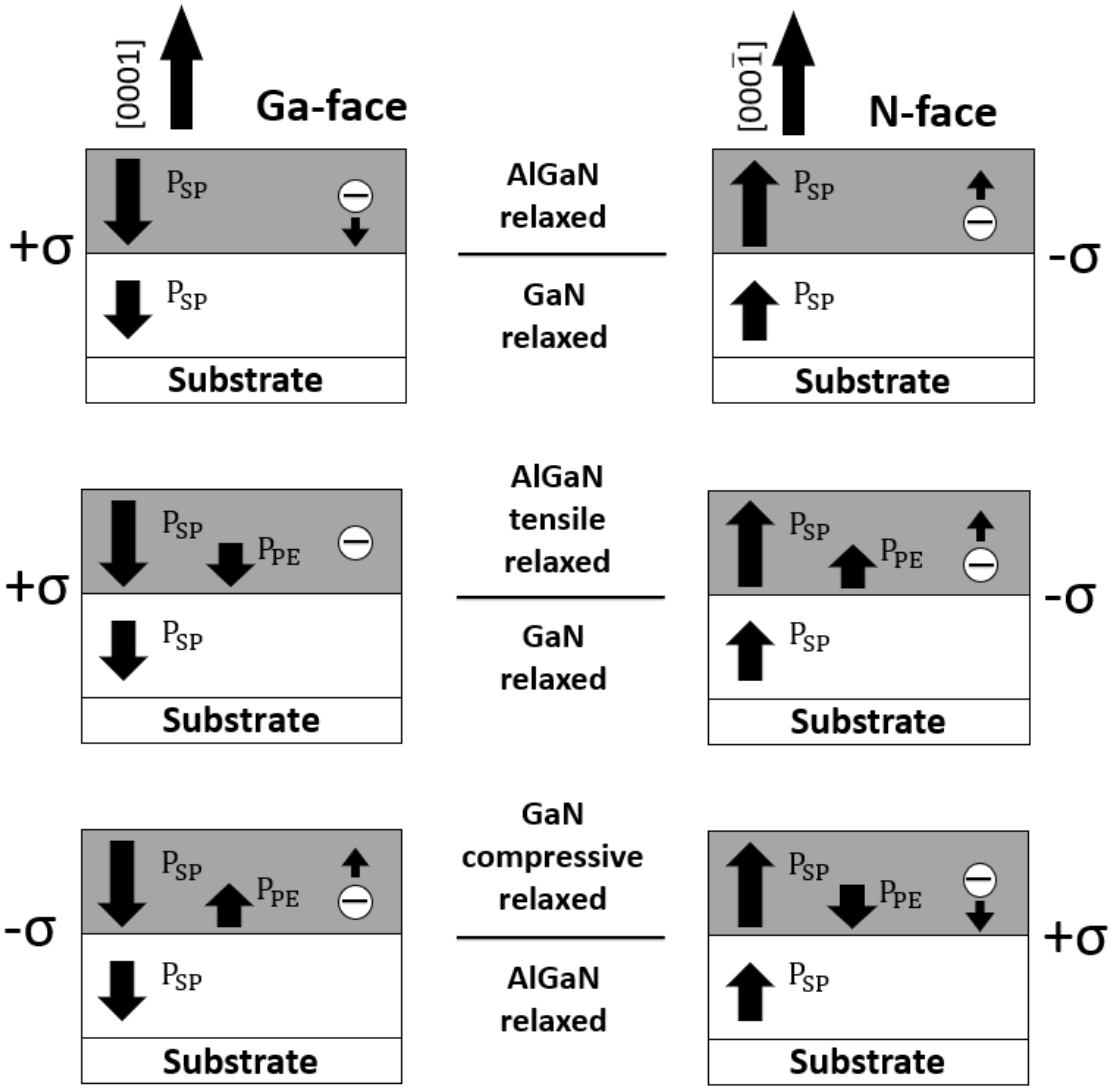

Figure 1.2: Different polarities (Ga- and N-faced) of wurtzite GaN [2].

Table 1.2: Comparison of AlInGaN/GaN HEMTs performance.

Reference	Substrate	L_g (nm)	f_T (GHz)	f_{max} (GHz)	$I_{d,max}$ (A/mm)
IEEE Electron Device Lett'11[16]	SiC	66	220	60	2.1
Phys. Status Solidi'13[17]	SiC	26	317	49	2.2
IEEE Electron Device Lett'13[18]	SiC	40	230	300	1.8
Phys. Status Solidi'16[5]	SiC	100	102	130	1.8
Appl. Phys. Express'17[19]	SiC	50	182	402	2.22

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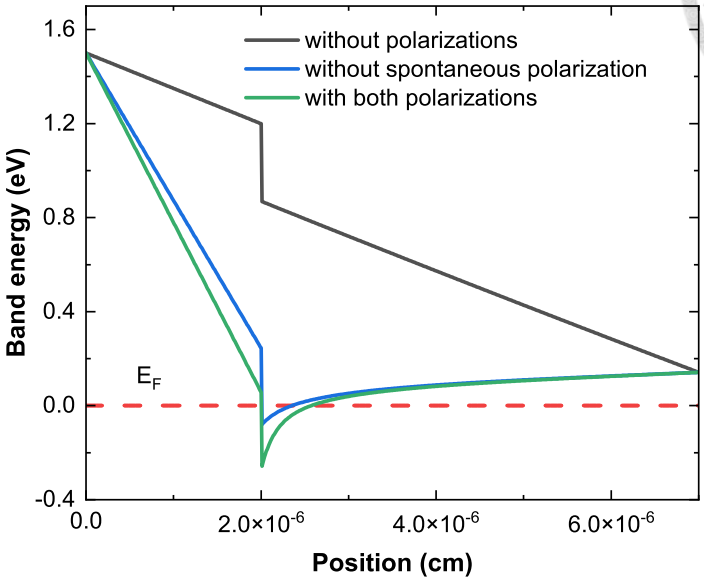

Figure 1.3: Conduction band edges for a $Al_{0.265}Ga_{0.735}N$/GaN heterostructure with and without polarizations [3].

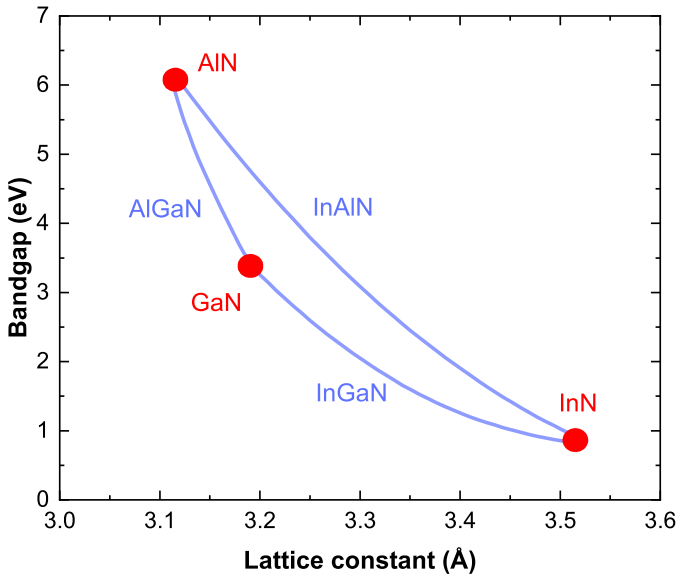

Figure 1.4: Wurtzite GaN, AlN, and InN and their alloys bandgaps against their lattice constants at 300 K [4, 5].

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roughness and alloy scattering [22]. Fortunately, quarternary InAlGaN can independently adjust the lattice constant and the bandgap to avoid immiscibility in AlN, InN, and GaN. It allows for the development of a high-quality barrier layer with a high Al composition, leading to high charge density and mobility. Figure 1.4 presents we can optimize the InAlGaN barrier layer by adjusting the composition of different AlN, GaN, and InN. Ronghua Wang et al. fabricated a quarternary barrier InAlGaN/AlN/GaN HEMTs on SiC substrate with regrown ohmic contacts and T-gates. The 40nm-long gate device showed f_T/f_{max} of 220/300 GHz [18]. It attributed a high electron mobility μ_e = 1770 cm^2/Vs which was higher than μ_e = 1300 cm^2/Vs of InAlN/GaN HEMTs [20].

The high-frequency characteristics of AlInGaN/GaN components are listed in table 1.2, which shows that they have good characteristics in the world, but there is still room for development.

1.3 Thesis overview

This paper is divided into six chapters. Chapter 1 is the introduction, which introduces the development of communication technology and GaN. The advantages of material properties and the motivation of this thesis are briefly described. Chapter 2 is the research method, which introduces the equations and principles used in the simulation in this thesis. Chapter 3 is to fit the experimental measurement data and analyzes the problem of the experimental epitaxial structure. Chapter 4 is about the optimization of the epitaxial structure. Through the problems found in the third chapter, the adjustment of the epitaxial structure is carried out. Chapter 5 is the electrical analysis of the components. Through epitaxial structure designed in chapter 4, the results are discussed for gate length, contact

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resistance sheet resistance, low/high-k passivation, and f_{max}. Chapter 6 is the conclusion of this thesis and future research directions.

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Chapter 2

Methodology for two dimensional simulation

To model the HEMTs accurately, we must consider all the physical mechanisms of the device. In this chapter, we will introduce the simulation method of the device.

2.1 2D Poisson and drift-diffusion equation

The 2D finite element Poisson and drift-diffusion charge control solver developed in our laboratory is used to simulate the electrical properties of devices such as band diagram, carrier distribution, $I-V$ curve, and so on in HEMTs [23, 24]. The Poisson equation solves the potential caused by a given charge.

$$\nabla(\epsilon\nabla V) = n - p + N_A^+ - N_D^- + N_{trap}^{\pm} + \rho_{pol}, \tag{2.1}$$

V is the band potential of the device, ϵ is the dielectric constant of the material, N_A^+ is the activated acceptor concentration, and N_D^- is the activated donor concentration. n and p

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are the electron carrier concentration and the hole carrier concentration, respectively. ρ_{pol} is the density of polarization charges.$N_{trap}^{\pm}$ is acceptor-like donor-like trap concentration.

$$N_A^- = \frac{N_A}{1 + 4exp((E_v - E_{fp} + E_{act})/k_B T)}, \tag{2.2}$$

$$N_D^+ = \frac{N_D}{1 + 2exp((E_{fn} - E_c + E_{act})/k_B T)}, \tag{2.3}$$

$$n = \int_{E_c}^{\infty} \frac{N_{dos}(E)dE}{1 + exp(E - E_{fn})/k_B T}, \tag{2.4}$$

$$n = \int_{-\infty}^{E_v} \frac{N_{dos}(E)dE}{1 + exp(E_{fp} - E_v)/k_B T}, \tag{2.5}$$

$$N_{trap}^{\pm} = \frac{N_{trap}}{1 + exp(E_v - E_f + E_{trap})/k_B T}, \tag{2.6}$$

$N_{dos}(E)$ is the density of states for the conduction band or valence band. E_c and E_v are the conduction band and the valence band, respectively. E_{fn} and E_{fp} are the quasi-Fermi levels of electron and hole, respectively. The drift-diffusion equation is used to describe the carrier transport of the device.

$$J_n = \mu_n n \nabla V + q D_n \nabla n, \tag{2.7}$$

$$J_p = \mu_p p \nabla V - q D_p \nabla p, \tag{2.8}$$

$$D = \frac{\mu k_B T}{q}, \tag{2.9}$$

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J_n and J_p are the electron and hole current densities, respectively. μ_n and μ_p are the mobility of electron and hole, respectively. D_n and D_p are diffusion coefficients of electron and hole, respectively.

2.2 Carrier transport model in GaN-HEMTs

The transistor relies on the electric field to drive the flow of carriers, and a large electric field is often generated in HEMTs, so the carrier transport model must consider the change of the carrier mobility with the electric field. Otherwise, the simulated current will be different from the actual current. The situation is very different. For this reason, we also use the Monte Carlo program to calculate the change of electron mobility and electric field so that the evolution of electron mobility and electric field can be considered in Poisson and drift-diffusion solver. Figure 2.1 shows the relationship between electric field and velocity by the Monte Carlo program.

Traps have a great influence on the electrical properties of GaN-HEMTs. The 2DEG is formed by polarization and surface trap in the AlGaN/GaN heterojunction, and under high power operation, the surface trap traps the electron resulting in a decrease in channel 2DEG concentration and the reduction of the channel current. In addition, the buffer trap also affects the breakdown voltage and buffer leakage current of the device. Therefore we apply traps on the surface and the buffer to simulate the trapping effect of GaN-HEMTs. Figure 2.2 shows a schematic diagram of the surface trap and buffer trap in AlGaN/GaN HEMT.

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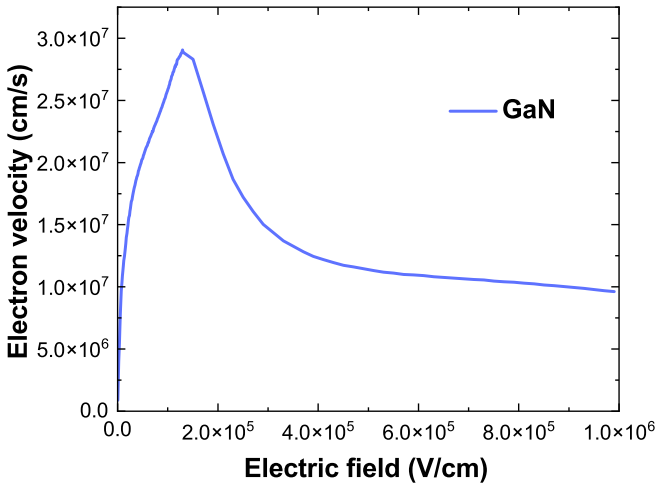

Figure 2.1: The relationship between electron velocity and electric field of GaN at 300K.

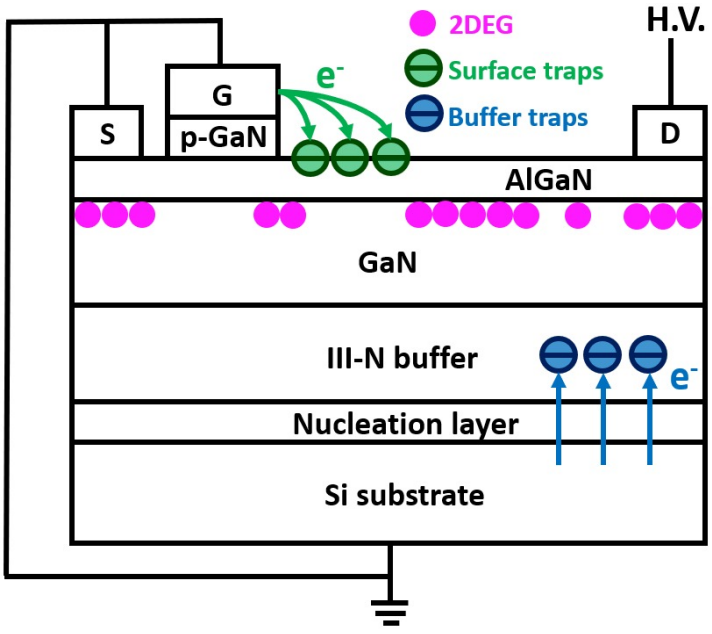

Figure 2.2: Schematic of the surface and buffer trapping mechanisms in GaN-HEMTs [6].

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2.3 Thermal model in GaN-HEMTs

HEMTs are often used in high-power device applications, so the thermal energy generated inside the device will increase the internal temperature. At this time, the mobility will decrease due to the high temperature, and the number of carriers will also change due to the high temperature. Without evaluating the effect of the internal temperature of the device, it may deviate significantly from the actual situation. Therefore, we add calculations to the thermal model to make the simulation results more realistic. The following equation can be used to determine the heat diffusion equation in a steady state

$$-\nabla \cdot (\kappa \nabla T) = \vec{E} \cdot \vec{J}, \tag{2.10}$$

where κ is thermal conductivity and T is temperature. $\vec{E}$ is electric field and $\vec{J}$ is current density. $\vec{E} \cdot \vec{J}$ is represented as heat source. Equation (2.10) may be solved to determine the temperature profile of the device. The temperature dependent mobility can be solved by the following equation

$$\mu(T) = \mu(T_0) \cdot \left(\frac{T}{T_0}\right)^{\alpha}, \tag{2.11}$$

$\mu(T)$ is the temperature-dependent mobility. $\mu(T_0)$ is the mobility in 300 K. T and T_0 are the temperatures of the device, and the room temperature, which is 300 K. α is the mobility temperature coefficient. Figure 2.3 shows the influence of adding thermal simulations on electrical properties.

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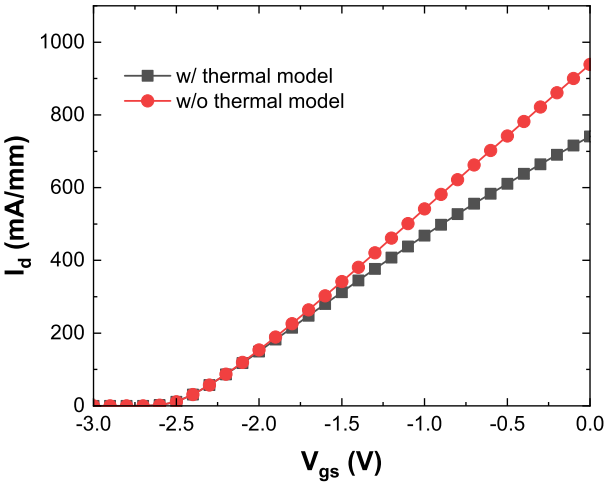

Figure 2.3: DC characteristics of GaN-HEMTs structure with and without thermal model [7].

2.4 Simulation flow chart

The simulation model is shown in figure 2.4. The 2D Poisson and drift-diffusion solver solve the above equations self-consistently by Gummel's iteration.

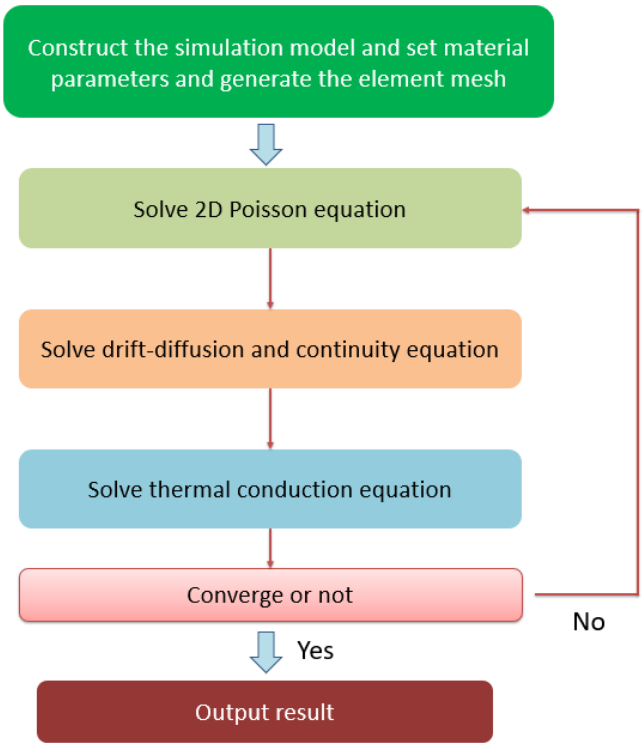

Figure 2.4: Flowchart of the simulation model.

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Chapter 3

Experiment

We first fit the experimental data, establish a device model, and verify whether the simulation method is correct. Then optimize the device structure and material to improve the device performance.

3.1 Fitting experimental data

This epitaxial structure and measurement data are provided by WIN semiconductors. First, we establish a preliminary device model according to the epitaxial structure provided by the experiment. And set the model size according to the mask design. As shown in figure 3.1, the structure on the SiC substrate consists of an 18 nm thick AlGaN barrier layer with a 26.5% Al composition, an 800 nm thick undoped GaN channel, a 2.5 nm thick GaN cap, and a 410 nm thick Si_3N_4 passivation layer. The source field plate (SFP) is 1.72 μm. The distance between the gate to source (L_{gs}) and gate to drain (L_{gd}) are 1 μm and 3 μm, respectively. Figure 3.2 shows the T-gate structure and the gate length (L_g) is 250 nm.

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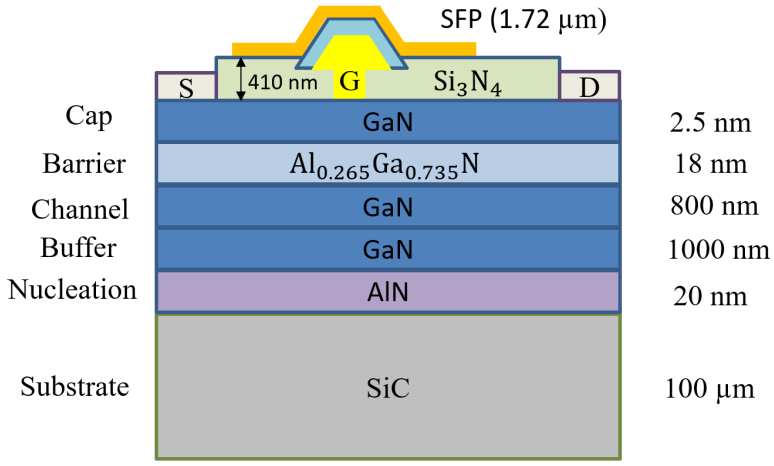

Figure 3.1: Epitaxial structure of experiment provided by WIN semiconductors.

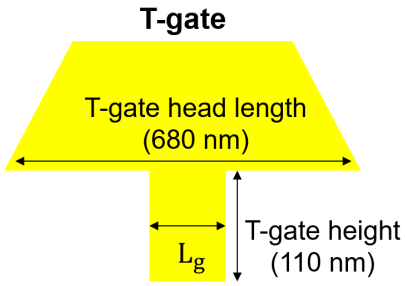

Figure 3.2: Schematic of T-gate.

Using the values of R_c and R_s obtained from the experimentally measured Transfer Length Method (TLM) data, we can extract the simulation parameters by simulating the same epitaxial structure, such as mobility and impurity density under drain and source contact, trap density and impurity density of capping layer, the low field mobility of the channel and so on. After the parameters are obtained, the output and transfer characteristics and RF characteristics under the long gate length in the experiment are fitted to fit the characteristics of threshold voltage (V_{th}), maximum drain current, f_T, etc., and take out thermal model parameters.

Figure 3.3 is the result of the simulated TLM measurement. By calculating the resistance of the different distances from the source to the drain, We can obtain almost the same R_c and R_s as the experimental measurements shown in the table 3.1.

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Table 3.1: Comparison of experimental and simulated TLM results.

	R_c (Ω·mm)	R_s (Ω/sq)
Experiment	0.3	475
Fitting	0.33	470

Figure 3.4 shows the result of our fitting of the experimental V_{th}. We first simulated the characteristics of $I_d - V_{gs}$ according to the structure in figure 3.1 and found that the simulated V_{th} was inconsistent with the experiment. We consider that the leakage current is too large, so we add Carbon(C) doping to the buffer layer to prevent buffer leakage current. However, the buffer leakage current is still quite large, as shown in the red line in figure 3.4. We speculate that the undoped channel thickness of the actual device is not as shown in figure 3.1. Therefore, we reduce the channel thickness by C-doped to fit the experimental V_{th}. When the channel thickness is reduced to 100 nm, the simulated V_{th} will match the actual measurement result as the green line in figure 3.4.

Figure 3.5 shows the equivalent device structure after V_{th} fitting, which will be used for simulation later.

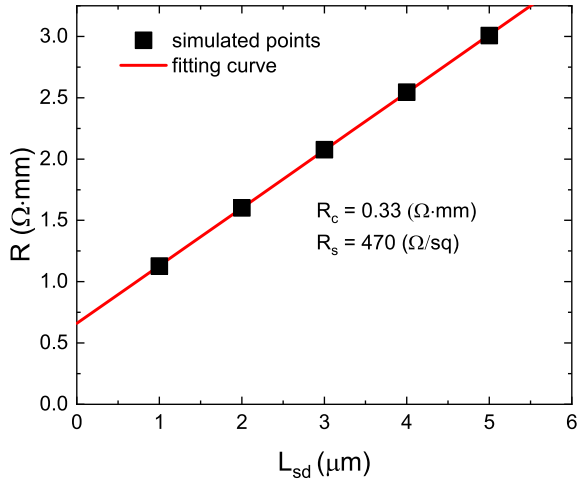

Figure 3.3: TLM simulation results.

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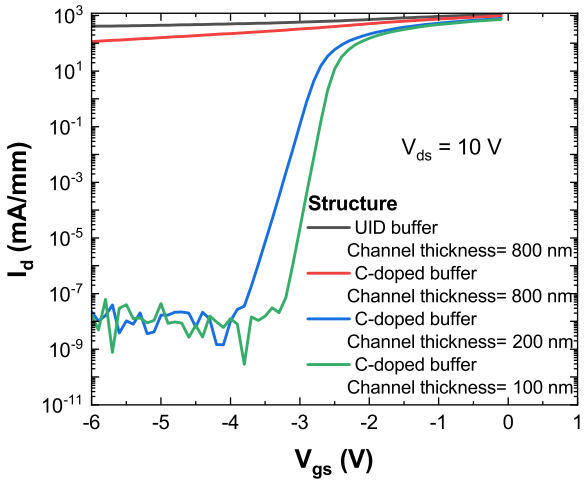


Figure 3.4: Threshold voltage fitting results.

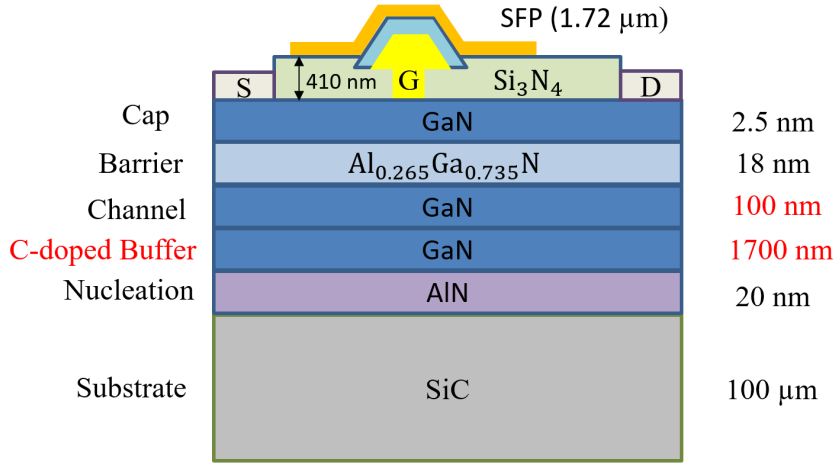
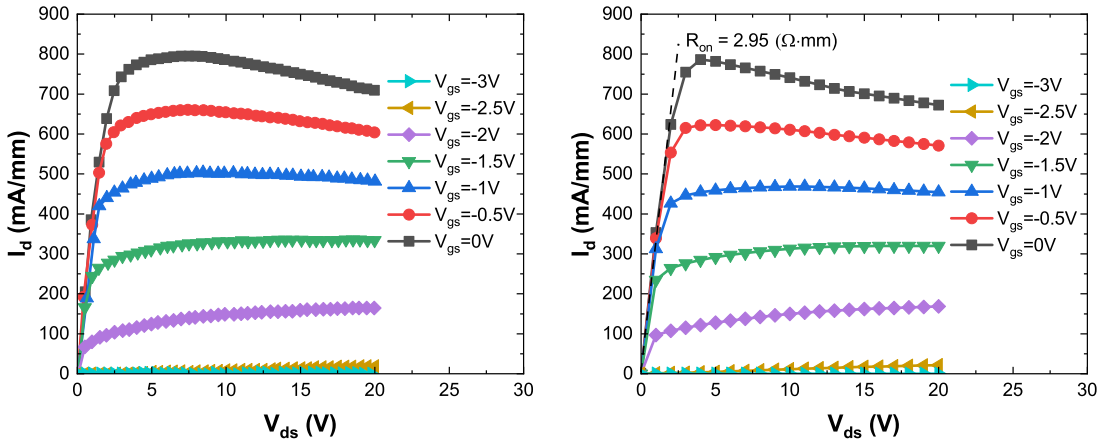


Figure 3.5: Schematic of the device structure after V_{th} fitting.



(a) (b)

Figure 3.6: I–V output characteristic of (a) experimental data from WIN semiconductors (b) simulation.

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Figure 3.6 is the experimental and simulated $I_d - V_{ds}$ curve. The R_{on} of the experimental data is about 2.5 Ω·mm, slightly lower than the 2.95 Ω·mm calculated by the simulation. And the I_d of the experimental measurement is 700 mA/mm higher than the simulated 673 mA/mm at V_{gs}=0 V and V_{ds}=20 V. We consider that it is possible that the simulated field-dependent mobility model is different from the actual mobility. Except for the above points, the overall simulated $I_d - V_{ds}$ curve is consistent with the experimental data. As shown in figure 3.6(b), it can be seen that there is a negative g_{ds} under large bias voltage, which is caused by the thermal effect by adding the thermal model, which has the same trend as the experimental data.

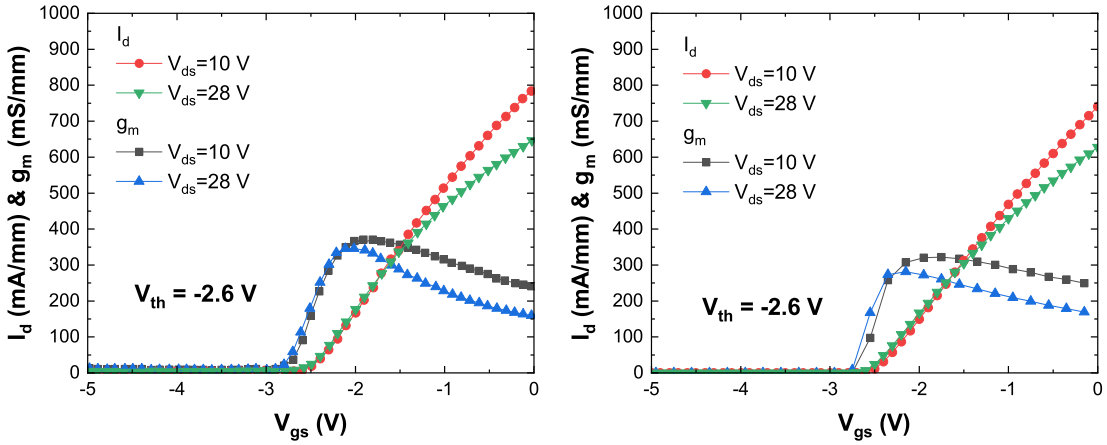

Figure 3.7: Transfer characteristics of (a) experimental data from WIN semiconductors (b) simulation.

As shown in Figure 3.7, the experimental and simulated V_{th} are both -2.6 V. The g_m can be written as

$$g_m = \frac{\partial I_d}{\partial V_{gs}}. \tag{3.1}$$

The g_m of the experimental data is 370 mS/mm, and the simulated g_m is 340 mS/mm at V_{ds}=10 V. The reason for this is presumably due to the difference in field-dependent mobility. The g_m at V_{ds}=10 V higher than V_{ds}=28 V in figure 3.7. Because high V_{ds} leads to higher device temperature, mobility would drop, and I_d and g_m would decrease.

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From figure 3.6 and figure 3.7, our simulation results are almost the same as the experimental data, thus verifying the credibility of our simulation.

3.2 Scale down of gate length

The gate length directly affects the size of C_g, because it is like a parallel plate capacitance under the gate, and the capacitance of the parallel plate is proportional to the capacitance area, so the shorter the gate length can make the C_g smaller, and more favorable the performance of f_T. And f_T can be calculated with the following equation

$$f_T = \frac{g_m}{2\pi C_g}, \tag{3.2}$$

current gain cutoff frequency (f_T) represents the frequency at which the current gain of the device is one, which is a factor used to determine the high frequency characteristics of the device. As mentioned above, to get high f_T, we reduce the gate length. However, f_T does not increase with decreasing gate length in figure 3.9(b). The reason is that C_g decreases, as we mentioned earlier as gate length decreases in figure 3.9(a). But g_m also decreases causing f_T to decrease in figure 3.8(b). The reason is that although C_g decreases as the gate length in figure 3.9(a) decreases, the decrease is not enough. When a parallel plate capacitance area is reduced by a factor of five, the capacitance value is theoretically reduced by a factor of five. However, the capacitance value of figure 3.9(a) only drops by a factor of about 1.5, so that f_T does not rise as expected in figure 3.9(b). The design of the T-gate and the passivation layer will both affect the C_g of the device, so improving the above two reasons is the key factor in improving the f_T. Another reason is the huge drop in g_m. The reduction in g_m is because the shorter gate length makes it easier for the

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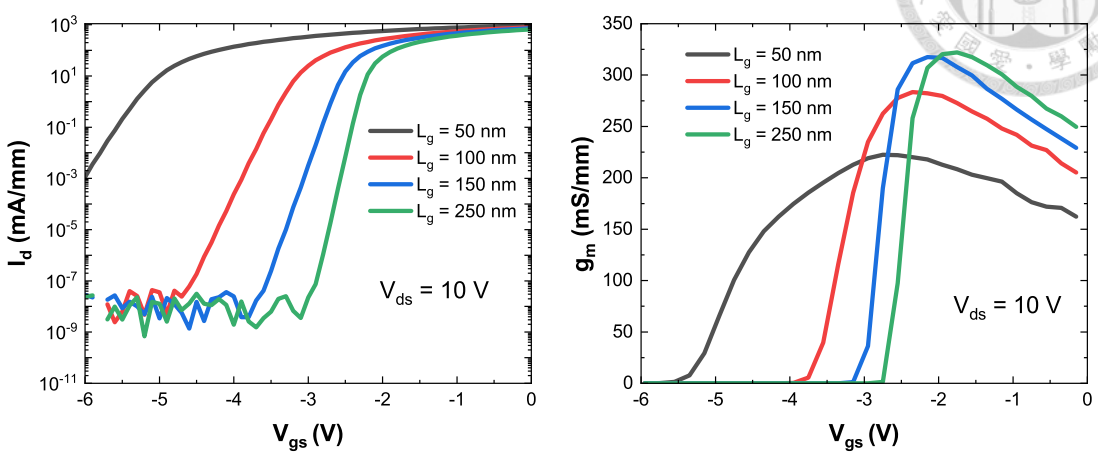
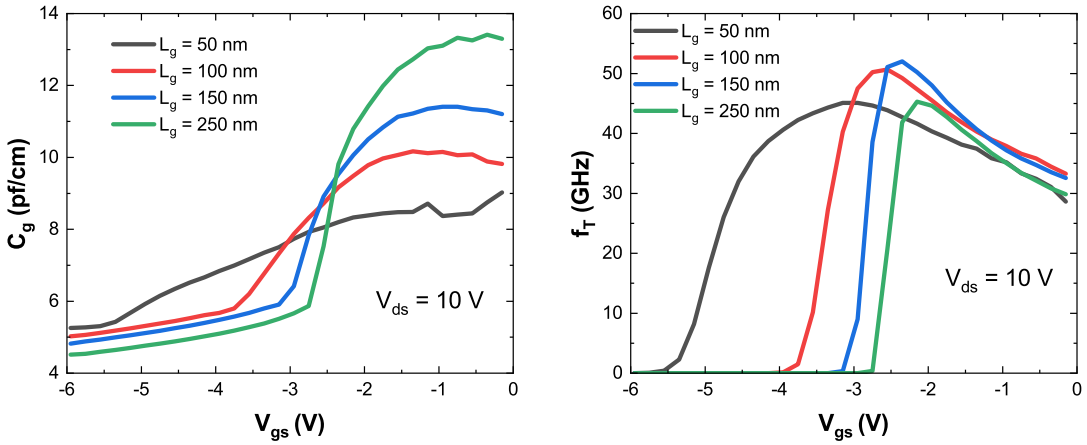
2DEG to flow through the gate from the bottom of the channel, making it difficult for the gate to control the channel. Therefore, to obtain high f_T, it is necessary to reduce C_g and



(a) (b)

Figure 3.8: Different gate length of (a) I_d (b) g_m.



(a) (b)

Figure 3.9: Different gate length of (a) C_g (b) f_T.

suppress the SCEs.

3.3 Scale down of L_{gd} and L_{gs}

In this section, we investigate the performance of the distance from the gate to the drain and the distance from the gate to the source on component electrical properties. We simulated five different L_{gd} and L_{gs} structures with a gate length of 250 nm. As

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Table 3.2: Comparison of the properties of the five structures with a gate length of 250 nm.

Structure	L_{gs} (nm)	L_{gd} (nm)	$I_{d,max}$ (mA/mm)	R_{on} (Ω·mm)	$g_{m,peak}$ (mS/mm)	C_g (pf/cm)	$f_{T,peak}$ (GHz)
A	1	3	741	2.83	321	11.5	44
B	1	2	737	2.37	323	11.2	45
C	1	1	733	1.92	320	11.1	46
D	0.5	2	814	2.11	357	12.2	46
E	0.5	1	810	1.67	356	11.8	47

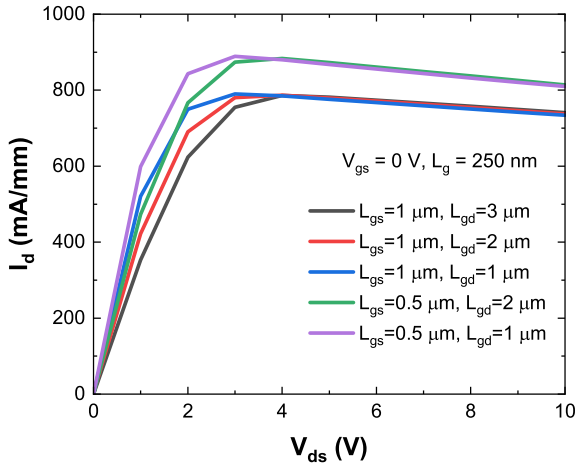

Figure 3.10: $I_d - V_{ds}$ characteristics for different L_{gd} and L_{gs}.

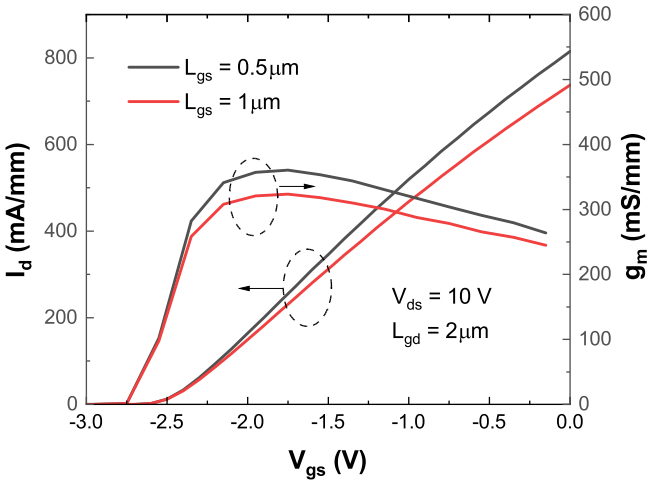

Figure 3.11: g_m and I_d–V_{gs} characteristics for devices with L_{gs} = 0.5 μm and L_{gs} = 1 μm respectively.

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shown in the figure 3.10, when L_{gd} decreases, the gate-drain distance decreases, so the gate-drain access region resistance also decreases. Therefore, when a small bias voltage is applied, the device with small L_{gd} has a larger drain current, which means that the R_{on} is smaller. A device with a small R_{on} means that this device consumes less power. Since the current characteristics are almost the same after entering the saturation region, when we operate at V_d=10 V, the frequency characteristics do not change much, as shown the in the table 3.2's structure A, B, and C. When L_{gs} decreases, the distance from the gate to the source decreases, so the gate-source access region resistance also decreases. Therefore, the maximum drain current of the device will increase accordingly. It is known that a transistor's maximum RF output power is proportional to I_d. Therefore, reducing the energy L_{gs} can improve the device's output power. Figure 3.12 shows the distribution of carrier density along channel for different L_{gd}. It can be found that the distribution of carrier density with L_{gs} of 0.5 μm has a greater variation with the change of V_{gs}, which means that the C_g of L_{gs} is larger. In the frequency characteristic, although reducing L_{gs}

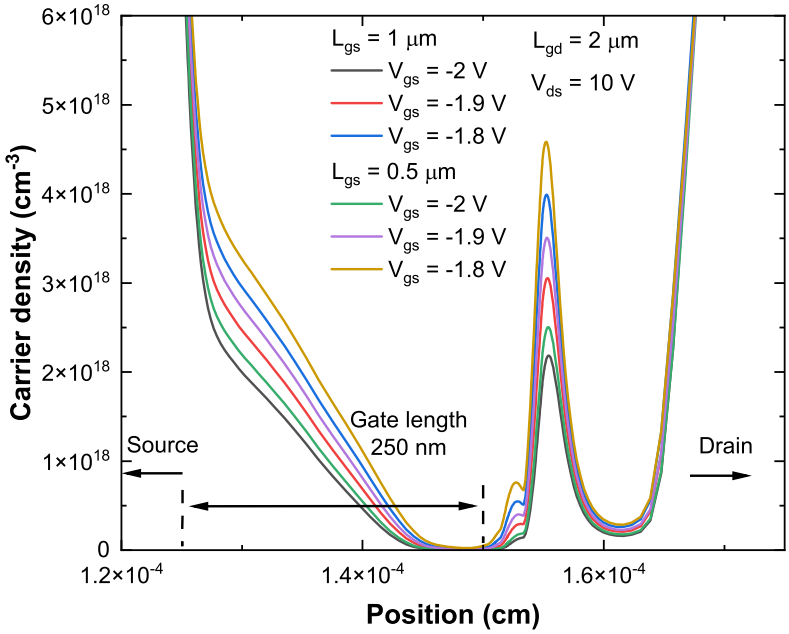

Figure 3.12: Distribution of carrier density along channel at V_{ds} = 10 V with L_{gs} = 0.5 μm and L_{gs} = 1 μm respectively.

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can increase the drain current, reducing L_{gs} will also increase C_g, so that f_T does not increase as expected, as shown in structures B and D of the table 3.2 and figure 3.11. It can be known from figure 3.12 that when V_{gs} changes, the change of carrier density of L_{gs}=0.5 μm is more than that of L_{gs}=1 μm. Therefore, the calculated C_g is larger.

Shortening L_{gs} and L_{gd} does not significantly improve the RF characteristics of the device, but it can improve the output power and power consumption of the device[25, 26].

3.4 Summary

As mentioned above, in order to obtain high f_T, it is necessary to reduce C_g and suppress SCEs. On the other hand, R_s is also a key factor affecting f_T. Higher drain current and g_m can be obtained because of lower R_s. Since R_s in this structure is 470 Ω/sq, the DC and RF characteristics of the device are limited. Therefore, the next chapter will optimize the epitaxial structure to reduce R_s and suppress SCEs, and improve the T-gate design and passivation layer to reduce C_g.

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Chapter 4

Epitaxial structure optimization of high-frequency GaN-HEMTs

Through the analysis in the previous chapter, we know that the DC and RF characteristics of the device can be improved by reducing R_s and suppressing the SCEs. We propose to improve the R_s of the device by optimizing the barrier layer. And by adding a C-doped buffer, reducing the thickness of the channel, and inserting the back barrier to suppress the SCEs.

4.1 Simulation model of GaN-HEMTs

The GaN-HEMT structure is shown in figure 4.1, grown on a high-resistance SiC substrate. The structure consists of the GaN buffer layer, an unintentionally doped GaN channel, a 1 nm-thick AlN spacer, and an undoped barrier layer. And the electron trap state is set at the surface of the GaN cap with 2 nm-thick. The distance between the source and gate is 0.2 μm. The distance between the drain and gate is 0.4 μm. As shown in figure 4.2, the gate uses the structure of a T-gate. The passivation layer is consisted of 20 nm-thick

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Si_3N_4 and 180 nm thick SiO_2. T-gate height is 200 nm. T-gate head length consists of 120 nm and L_g. The next chapter will discuss more details about T-gate and passivation layer and subsequent simulations using this gate structure.

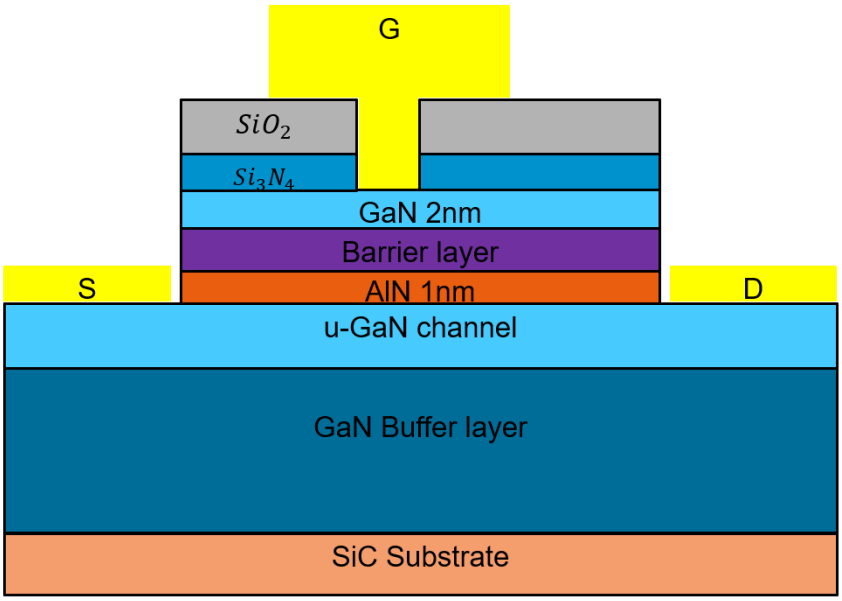

Figure 4.1: Schematic of simulation model.

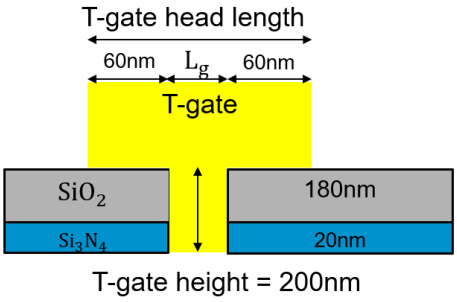

Figure 4.2: Schematic of T-gate.

4.2 Barrier layer

In conventional GaN-HEMTs, the formation of 2DEG is the polarization at the AlGaN/GaN interface and surface state. The 2DEG concentration greatly influences the electrical properties of the device, so it is necessary to optimize the barrier structure to increase the 2DEG concentration. Since AlGaN is limited by the stress problem and the

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Al composition does not exceed 30%, the 2DEG density of the AlGaN/GaN interface is low. Due to its low sheet resistance and high spontaneous polarization, the AlInGaN barrier is currently thought to be an efficient method to increase the 2DEG density and drain current density and g_m. On the other hand, due to the large polarization of AlInGaN, enough 2DEG can be formed with a thinner AlInGaN barrier. The thinner barrier layer helps to enhance the gate control capability, thereby suppressing the SCEs. Therefore, the AlInGaN barrier can improve the high-frequency characteristics of the device.

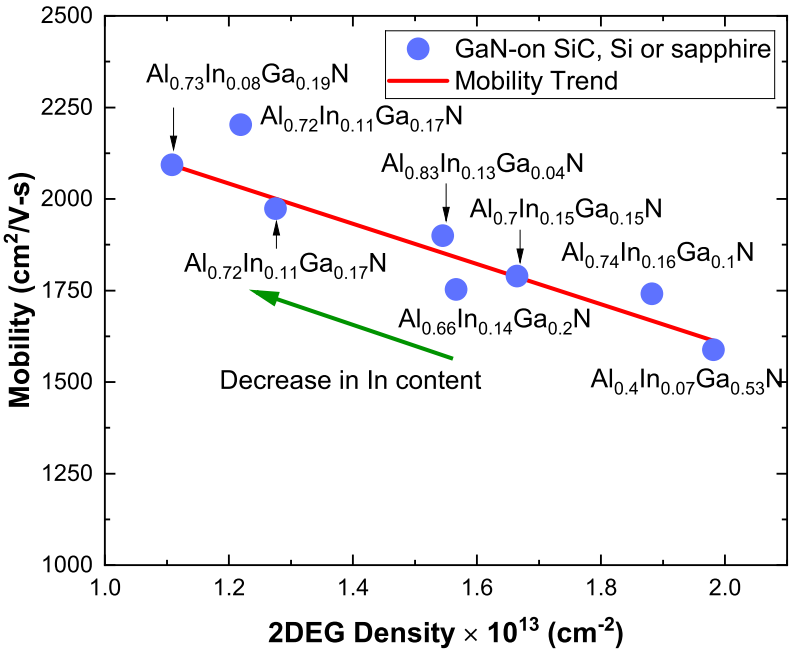

Figure 4.3: AlInGaN/GaN heterostructures' experimental mobility about 2DEG density and composition [8].

However, for transistors, carrier mobility can also greatly influence device characteristics. As seen from the figure 4.3, for the AlInGaN barrier, the 2DEG density change is larger than the mobility. When the 2DEG density is changed form 1.1×10^{13} cm^{-2} to 2×10^{13} cm^{-2}, the mobility changed form 2125 cm^2/Vs to 1625 cm^2/Vs. Therefore, we consider that 2DEG has a greater impact on device characteristics. In this section, we simulate different AlInGaN barrier compositions to obtain higher 2DEG concentrations. However, it is not considered if the lattice mismatch is much more serious than

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$Al_{0.3}Ga_{0.7}N$/GaN.The undoped AlInGaN barrier is 10 nm. The GaN channel is 100 nm. GaN surface potential is pinned in 1.5 eV.

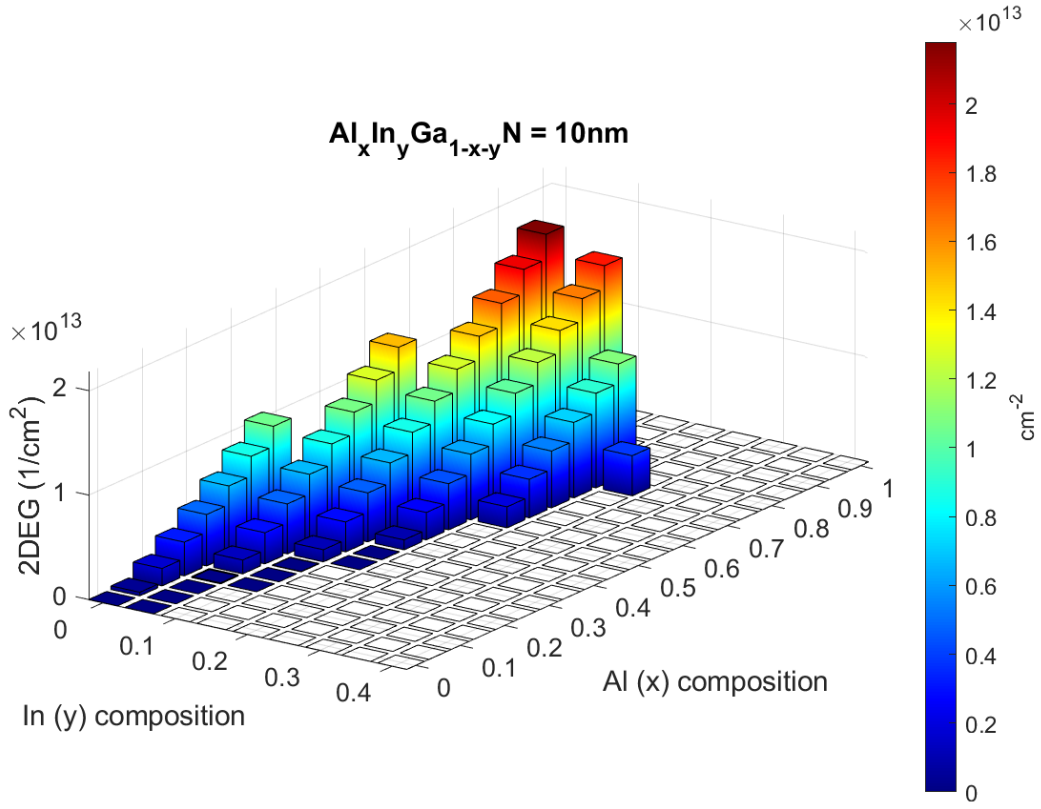

Figure 4.4: 3D bar graph of 2DEG concentrations with different AlInGaN compositions.

Table 4.1: Comparing the lattice constant and 2DEG density of AlInGaN with different compositions.

material	GaN	$Al_{0.3}Ga_{0.7}N$	$Al_{0.83}In_{0.17}N$	$Al_{0.8}In_{0.1}Ga_{0.1}N$
Lattice constant (Å)	3.189	3.166	3.185	3.163
Thickness (nm)	–	10	10	10
2DEG ($1/cm^2$)	–	8.66×10^{12}	1.55×10^{13}	2.19×10^{13}

Figure 4.4 shows the 2DEG concentration generated by different AlInGaN composition barriers. The empty space in the figure represents that the AlInGaN of this composition has a serious lattice mismatch with GaN, which represents that the degree of

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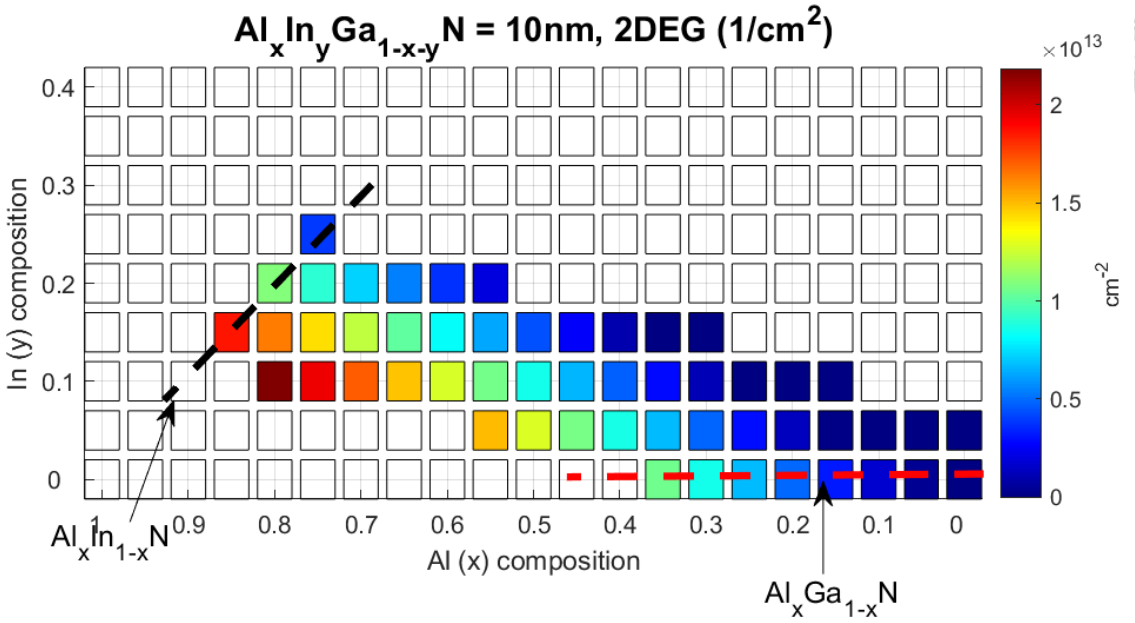

Figure 4.5: 2D profile of 2DEG concentrations with different AlInGaN compositions.

lattice mismatch exceeds that of the $Al_{0.3}Ga_{0.7}N$/GaN heterostructure or AlInGaN without this composition. The red dashed line represents the 2DEG concentration change of $Al_xGa_{1-x}N$, and the black dashed line represents the 2DEG density change of $Al_xIn_{1-x}N$ in figure 4.5. It shows that the 2DEG density is higher when the Al composition is higher or the In composition is lower. However, the lattice mismatch also needs to be considered, so $Al_{0.8}In_{0.1}Ga_{0.1}N$ would have the highest 2DEG density which lattice constant is similar to $Al_{0.3}Ga_{0.7}N$ in figure 4.5.

The result of table 4.1 shows the lattice constants and 2DEG density of three barrier layer materials. Although $Al_{0.8}In_{0.1}Ga_{0.1}N$ and $Al_{0.3}Ga_{0.7}N$ have lattice mismatch problems, the 2DEG density of $Al_{0.8}In_{0.1}Ga_{0.1}N$ is quite high. Although $Al_{0.83}In_{0.17}N$ is lattice matched, its 2DEG density is lower than that of $Al_{0.8}In_{0.1}Ga_{0.1}N$. Therefore, $Al_{0.8}In_{0.1}Ga_{0.1}N$ is chosen as the barrier layer material because its lattice mismatch problem is acceptable and has the highest 2DEG density. We simulated the 2DEG concentra-

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tions of $Al_{0.3}Ga_{0.7}N$, $Al_{0.83}In_{0.17}N$ and $Al_{0.8}In_{0.1}Ga_{0.1}N$ barriers at different thicknesses. As we know, the thickness of 2DEG increases as the thickness of the barrier increases, and it tends to saturate after a certain thickness. From the result of figure 4.6, when the thickness of the barrier layer is greater than 15 nm, the increase of the 2DEG density gradually saturates. However, the thickness of the barrier also affects the gate modulation capability,

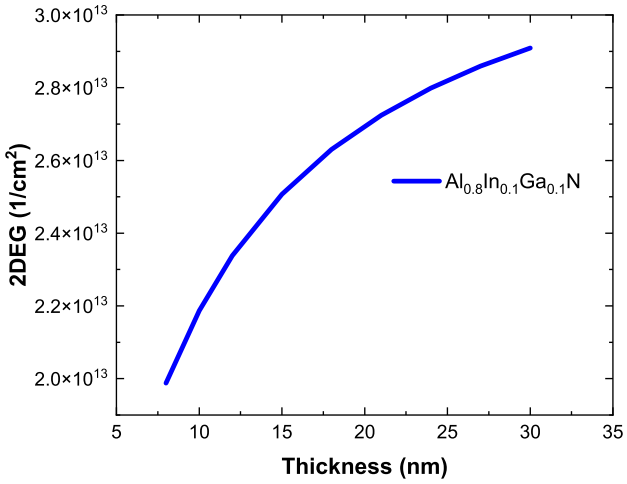

Figure 4.6: 2DEG concentration for different barrier layer thicknesses.

so we choose $Al_{0.8}In_{0.1}Ga_{0.1}N$ 10 nm thick as the barrier layer.

4.3 C-doped buffer and Channel thickness

Different configurations of buffer layers have been employed for high-frequency applications requiring short gate lengths. Due to the weak control of the gate to the channel, having a low resistivity GaN buffer layer causes some electrons from the source to drain to flow through the underlying buffer layer rather than through the active region of the device, resulting in buffer leakage current, which affects device performance. Therefore, a high resistivity is required for the GaN buffer layer to prevent buffer leakage current. Carbon doping can achieve this. Because Carbon (C) is a deep-level dopant with the self-compensation effect, it can replace Ga or N, working as donor or acceptor trapping centers

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to reduce leakage current.

Figure 4.7 presents the simulated band diagrams with a C-doped buffer for different channel thicknesses. We set the buffer layer to have a trap density of 1×10^{17} cm^{-3} as the C-doped buffer layer. The C-doped buffer can raise the conduction band of the buffer, which leads to enhancement of electron confinement, making the gate better control over the channel electrons. It can be seen that similar p-type doping is formed in the conduction band of the buffer so that the buffer has a high resistivity to restrict the path of electron flow. And it can be found that the thinner the channel thickness, the more significant the conduction band is raised, which means the better the confinement of electrons. So it can be expected to perform better in short L_g. Figure 4.8 presents the $I_g - V_{ds}$ characteristics for different channel thicknesses with L_g = 60 nm. The gate-drain bias V_{ds} is from 0.1 to 10 V, and the gate-source bias V_{gs} is swept from 0 to -8 V. It can be seen that a 50 nm-thick channel thickness can be turned off at about V_{gs}=-7 V, while a 250 nm-thick channel thickness cannot be turned off at V_{gs}=-8 V at V_{ds}=10 V.

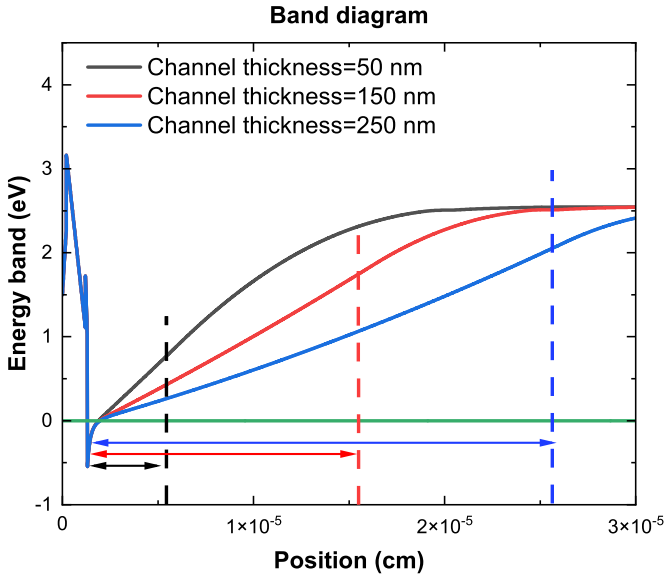

Figure 4.7: Band diagram for different channel thicknesses with C-doped buffer.

Next, the influence of SCEs on different channel thicknesses is discussed. The drain-

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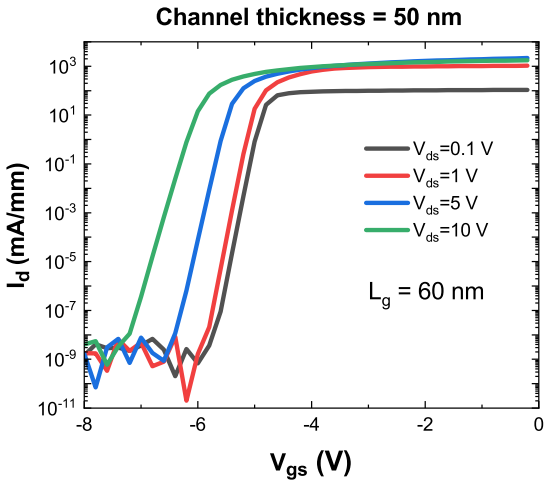
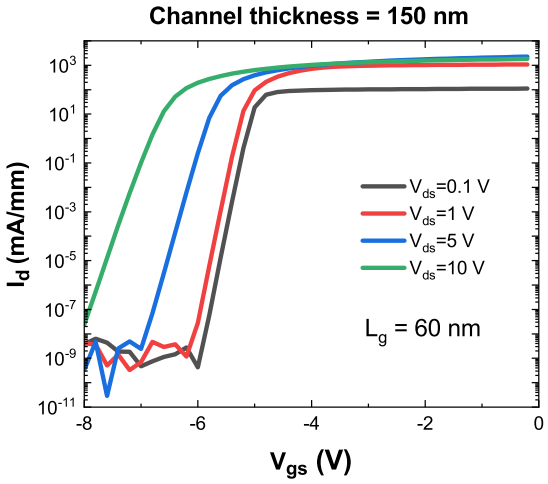


(a)



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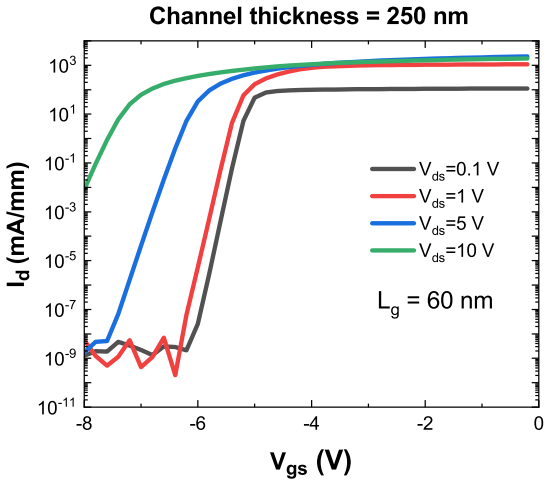

(c)

Figure 4.8: $I_d - V_{gs}$ characteristic of (a) 50 nm-thick GaN channel (b) 150 nm-thick GaN channel (c) 250 nm-thick GaN channel.

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induced barrier lowering (DIBL) and the subthreshold swing (SS) values are discussed to quantify the SCEs of the devices. In this work, V_{th} is defined as I_d=1×10^{-3} mA/mm. The DIBL describes the degree of V_{th} shift, which expressed a

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{ds}} = \frac{V_{th,sat} - V_{th,linear}}{V_{ds,sat} - V_{ds,linear}}, \tag{4.1}$$

where, $V_{ds,sat}$ and $V_{ds,linear}$ indicate the drain-source voltages of the device operating in saturation and linear region, respectively. $V_{th,sat}$ and $V_{th,linear}$ indicate the threshold voltages of the device operating in $V_{ds,sat}$ and $V_{ds,linear}$, respectively. The SS is used to describe the control capability of the gate to the channel switch, which is defined as the change in gate voltage that must be applied to create a one-decade increase in the drain current[27].

As shown in figure 4.9(a), the channel thickness is proportional to the V_{th} shift. The thinner the channel, the smaller the value of the V_{th} shift.

V_{th} shift is the change of V_{th} from V_{ds}= 0.1 V to 10 V. DIBL is calculated for ΔV_{ds}=[0.1, 10]V, with a turn on criterion for the drain current defined as I_d=1×10^{-3} mA/mm. SS is extracted directly from $I_d - V_{gs}$ characteristics at V_{ds}=10 V. As shown in figure 4.9(b) and figure 4.9(c), scaling channel thickness has a significant impact on the SCEs for a short L_g, as demonstrated by SS and DIBL. With the increase of channel thickness, DIBL and SS become larger, which means that SCEs become more and more severe.

Figure 4.10 shows the maximum g_m of the structure of a 50 nm-thick channel, the structure of a 150 nm-thick channel, and the structure of a 250 nm-thick channel is 533 mS/mm, 450 mS/mm, and 392 mS/mm, respectively. The latter means that the gate has

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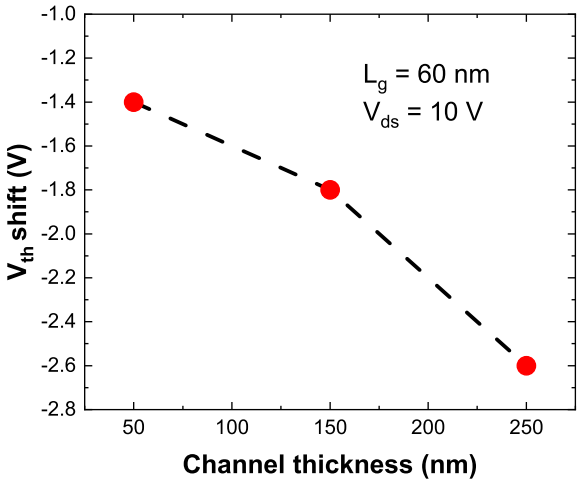
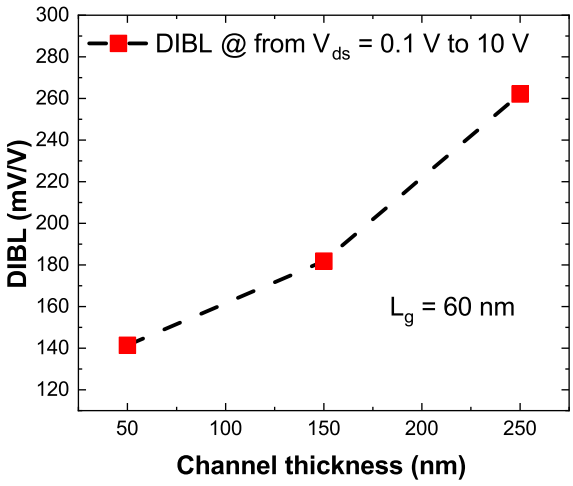


(a)



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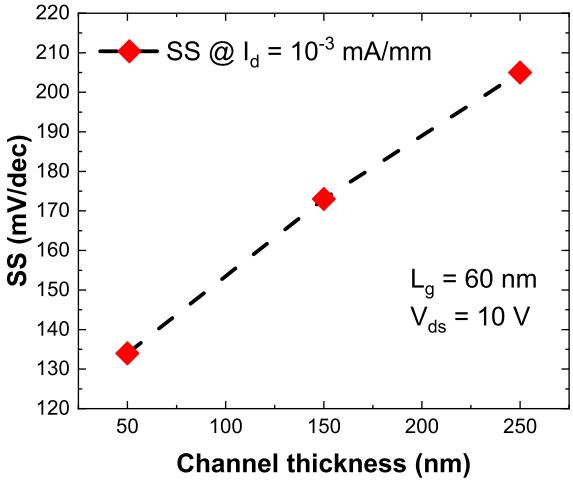

(c)

Figure 4.9: Results for different channel thickness (a) V_{th} shift (b) DIBL (c) SS.

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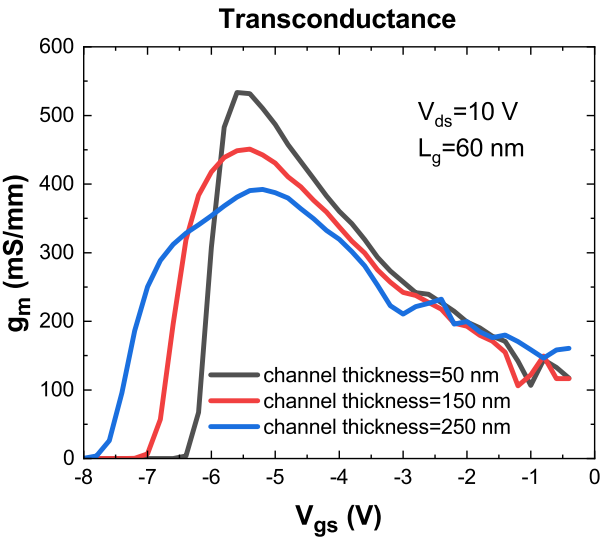

Figure 4.10: g_m of different channel thicknesses.

poor control over the channel, resulting in a decreased peak g_m. And the reduction of g_m also affects the RF performance. Therefore, the device's performance can be improved by reducing the thickness of the channel in short L_g.

4.4 Back barrier

To suppress the short channel effect more effectively, we propose to insert the AlGaN back barrier layer between the channel layer and the C-doped buffer. The AlGaN back barrier can raise conduction band energy to prevent the carrier injection from the buffer layer at high drain voltage, which can help to improve 2DEG confinement to overcome SCEs. Figure 4.11 presents the conduction band diagrams of AlGaN/GaN heterojunction with a 10 nm AlGaN back barrier. The back barrier is added between the buffer layer with a carbon doping concentration of 1×10^{17} cm^{-3} and the channel layer thickness of 50 nm. The AlGaN back barrier has an Al composition that ranges from 5 to 30 %. The conduction band bending of the channel rises with increasing Al composition, increasing the potential barrier height of the GaN/AlGaN barrier, which can effectively improve the

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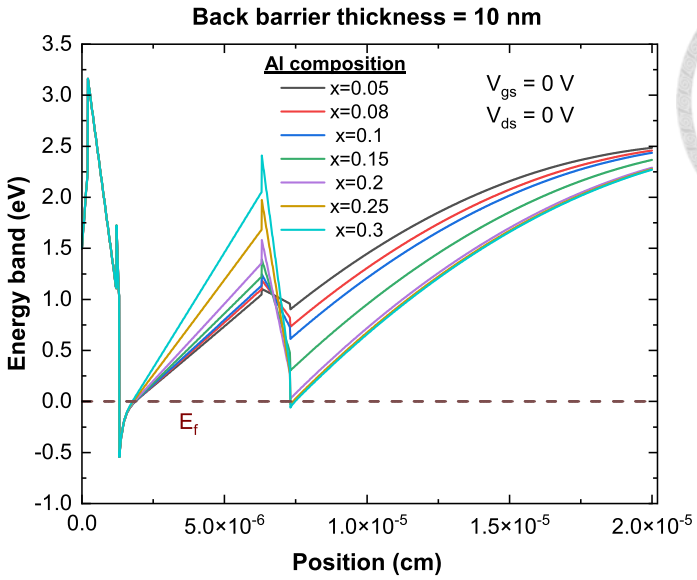

Figure 4.11: The result of conduction band diagrams in an $Al_xGa_{1-x}N$ back barrier for various Al compositions (x).

confinement of electrons. However, the high Al composition in the back barrier would increase defects in the back barrier so that electrons would flow to the buffer through paths formed by defects of the back barrier. Therefore, the low Al composition of < 10 % is appropriate for the AlGaN back barrier.

Figures 4.12(a) and (b) depict the effect of AlGaN back barrier layer thickness on 5 % and 8 % Al composition, respectively. As shown in figure 4.12 (c), although the increase in the thickness of the $Al_{0.1}Ga_{0.9}N$ back barrier has the most significant effect on the conduction band improvement, it is also easy to generate the second channel. When the $Al_{0.1}Ga_{0.9}N$ back barrier is above 40 nm, a second channel would be generated, which is unexpected. The second channel creates an additional current path that makes the gate difficult to control, making the SCEs even more severe. Then compare the I-V characteristics of different AlGaN back barriers at L_g = 60 nm.

Table 3.2 presents the different back barrier structures. It can be seen from figure 4.13 (c) that the second channel is generated when the thickness of AlGaN exceeds 40

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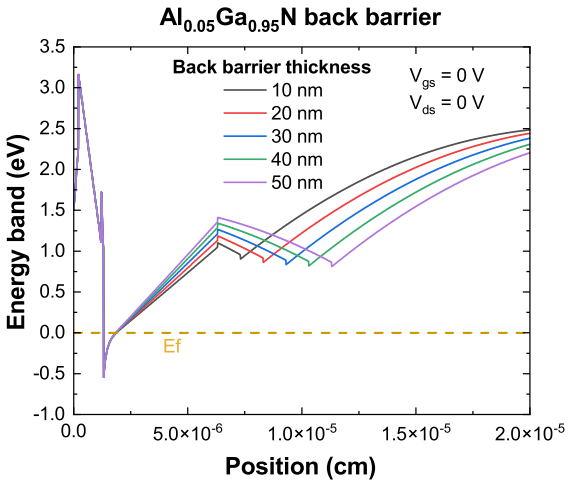
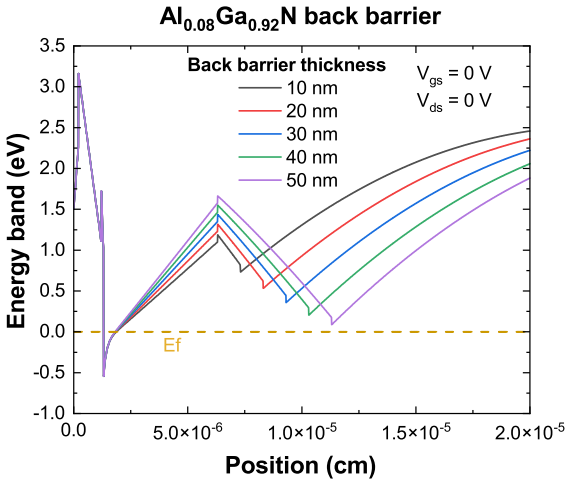


(a)



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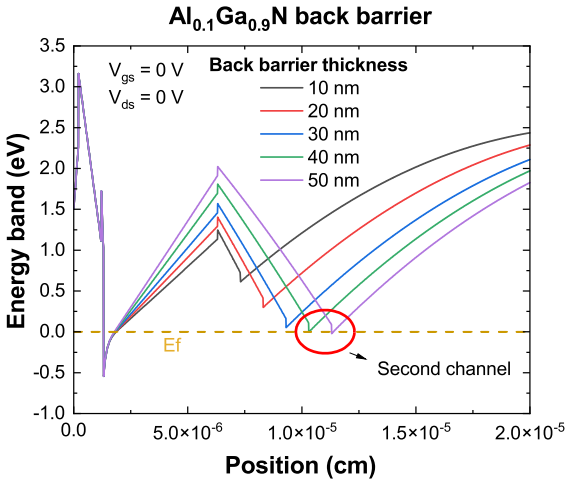

(c)

Figure 4.12: (a) $Al_{0.05}Ga_{0.95}N$ (b) $Al_{0.08}Ga_{0.92}N$ (c) $Al_{0.1}Ga_{0.9}N$ back barrier structure band diagram with different thicknesses.

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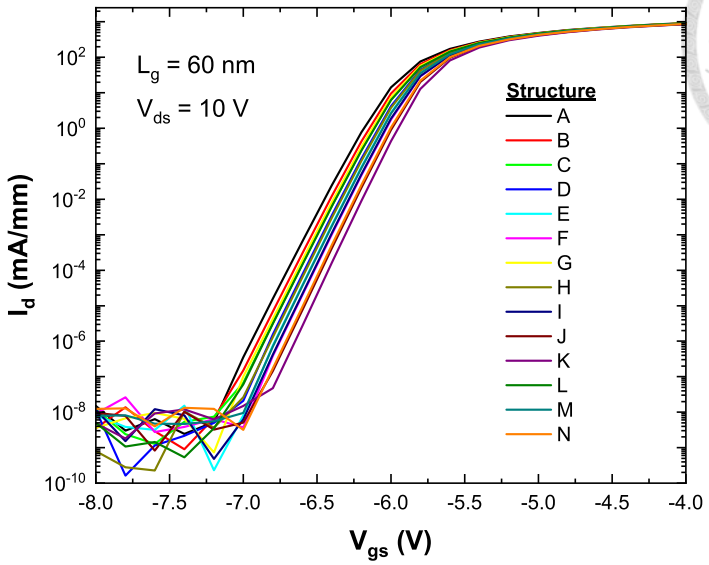

Figure 4.13: The $I_d - V_{gs}$ curves with different $Al_xGa_{1-x}N$ back barriers.

Table 4.2: Composition of different $Al_xGa_{1-x}N$ back-barriers.

Structure	Material	Thickness (nm)
A (no back barrier)	-	-
B	$Al_{0.05}Ga_{0.95}N$	10
C	$Al_{0.05}Ga_{0.95}N$	20
D	$Al_{0.05}Ga_{0.95}N$	30
E	$Al_{0.05}Ga_{0.95}N$	40
F	$Al_{0.05}Ga_{0.95}N$	50
G	$Al_{0.08}Ga_{0.92}N$	10
H	$Al_{0.08}Ga_{0.92}N$	20
I	$Al_{0.08}Ga_{0.92}N$	30
J	$Al_{0.08}Ga_{0.92}N$	40
K	$Al_{0.08}Ga_{0.92}N$	50
L	$Al_{0.1}Ga_{0.9}N$	10
M	$Al_{0.1}Ga_{0.9}N$	20
N	$Al_{0.1}Ga_{0.9}N$	30

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Table 4.3: Results of $I_d - V_{gs}$ characteristic with different $Al_xGa_{1-x}N$ back-barriers.

Structure	$I_{d,max}$ (mA/mm) (V_{gs} = 0 V) (V_{ds} = 10 V)	SS (mV/dec) (V_{ds} = 10 V)	$g_{m,peak}$ (mS/mm) (V_{ds} = 10 V)
A (no back barrier)	1751	127	532
B	1737	125	536
C	1729	123	540
D	1722	121	543
E	1713	119	547
F	1705	117	548
G	1734	123	539
H	1723	120	545
I	1712	118	551
J	1697	115	555
K	1688	113	558
L	1732	123	541
M	1719	119	549
N	1705	116	555

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nm. Therefore, the results of AlGaN thicknesses exceeding 40 nm are not discussed. Figure 4.13 shows serial $I_d - V_{gs}$ curves of different AlGaN back barriers at V_{ds} of 10 V. Structure A (black line) is the structure without a back barrier, with the largest leakage current and negative V_{th} shift. All other structures have back barriers, and it can be found that they all have smaller leakage currents than structure A and structure K (purple line) has the best performance. It means that the back barrier can effectively suppress SCEs.

Table 4.4: Comparing the high-frequency characteristic results of adding back barrier with different channel thickness.

Structure	Channel thickness (nm)	Back barrier	$g_{m,peak}$ (mS/mm) (V_{ds}=10 V)	f_T (GHz) (V_{ds}=10 V) (V_{gs}=-5.5 V)
A	50	$Al_{0.08}Ga_{0.92}N$	527	186
B	50	–	517	182
C	150	$Al_{0.08}Ga_{0.92}N$	455	157
D	150	–	433	153
E	250	$Al_{0.08}Ga_{0.92}N$	409	149
F	250	–	380	131

Figure 4.14 compares the effect of the back barrier on different channel thicknesses under short gate lengths. It can be noticed that the back barrier can effectively suppress the SCEs of the device. And it is found that the back barrier improves the ability to suppress the SCEs as the channel thickness increases. V_{th} shift, DIBL, and SS decrease the most at a channel thickness of 250 nm due to the insertion of the back barrier. It can be known from the table 4.4 that reducing the thickness of the channel and adding a back barrier layer can improve the high-frequency characteristics of the device. Therefore, 50 nm-thick $Al_{0.08}Ga_{0.92}N$ back barrier is suitable to be inserted between the C-doped buffer layer and the channel layer to suppress SCEs. And as the thickness of the channel increases, the

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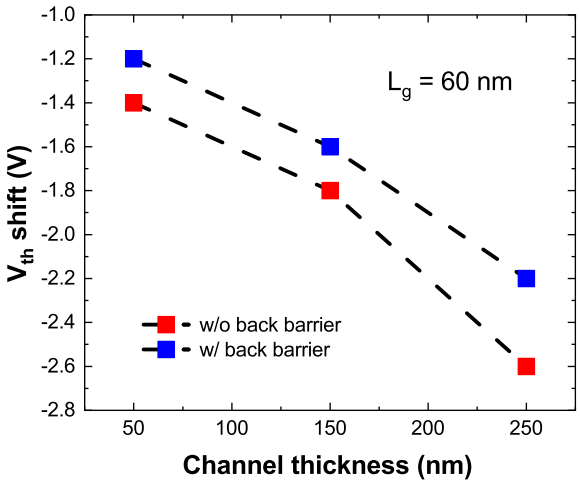
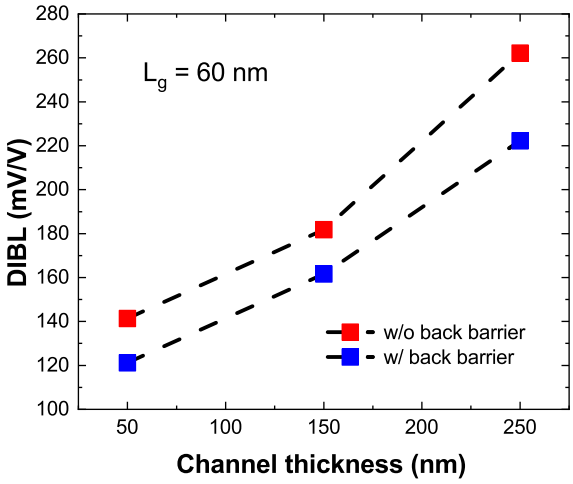


(a)



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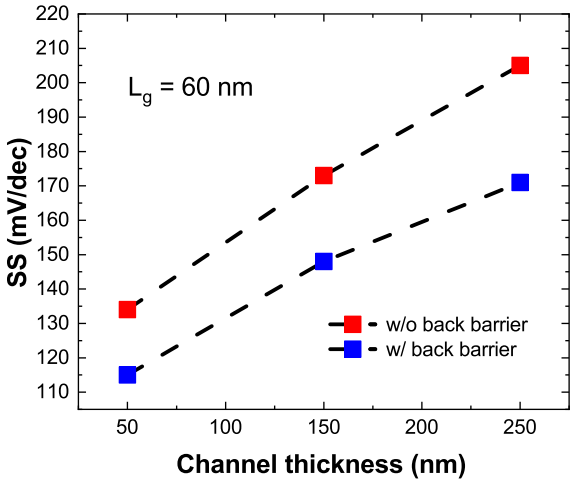

(c)

Figure 4.14: Results for different channel thickness with and without 50nm-thick $Al_{0.08}Ga_{0.92}N$ back-barrier (a) V_{th} shift (b) DIBL (c) SS.

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effect of the back barrier would also increase. Structure A has the highest f_T, so we use this structure for subsequent analysis.

4.5 Summary

In this chapter, the epitaxial structure is optimized, aiming at reducing R_s and suppressing the SCEs. The above results show that using AlInGaN can have a larger polarization field and generate more 2DEG density than AlGaN. Moreover, reducing the channel thickness and inserting the back barrier through a C-doped buffer can effectively suppress the deterioration of the device characteristics caused by the SCEs.

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Chapter 5

Results

This chapter will discuss the electrical properties of the epitaxial structure designed in the previous chapter. First, the electrical characteristics of shortening the gate length will be discussed. Second, the influence of contact and sheet resistance on electrical properties will be analyzed. Third, the impact of the high/low-k passivation layer will be discussed. Finally, the f_{max} of the device would be calculated.

5.1 Simulation model of GaN-HEMTs

The figure 5.1 shows the structure we proposed through the optimization of the epitaxial structure in the previous chapter, and the table 5.1 shows the simulated material parameters. The distance between source and gate is 0.2 μm. The distance between drain and gate is 0.4 μm. The R_s is 175 Ω/sq and R_c is 0.44 Ω·mm.

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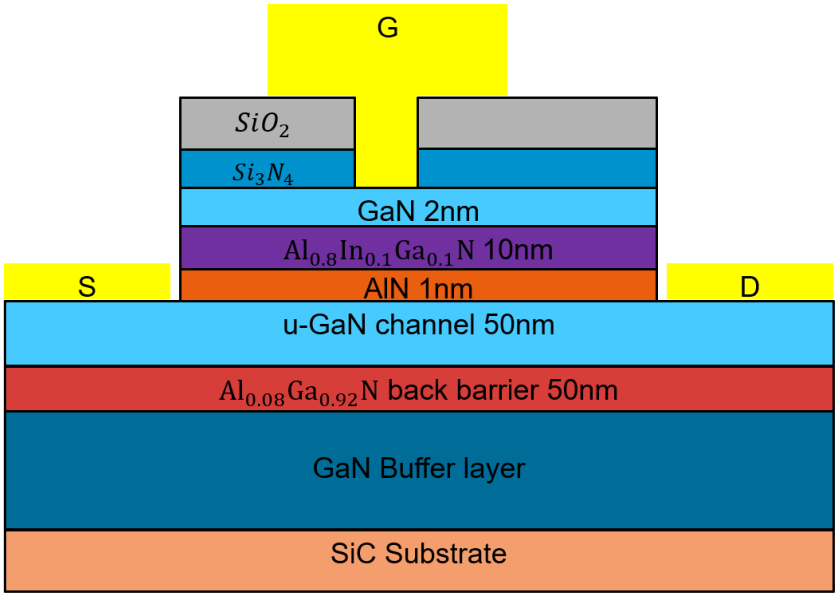

Figure 5.1: Schematic of epitaxial structure.

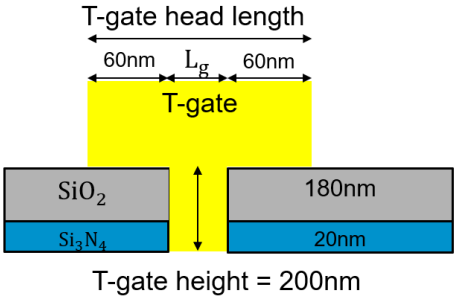

Figure 5.2: Schematic of T-gate.

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Table 5.1: The parameter of material in the simulation model.

Parameter/Material	GaN Buffer	AlGaN Back-barrier	GaN Channel	AlN	AlInGaN Barrier	GaN Cap
Bandgap (eV)	3.4	3.58	3.4	6	4.9	3.4
electron mobility ($cm^2V^{-1}s^{-1}$)	0.001	0.001	1782	20	20	0.001
hole mobility ($cm^2V^{-1}s^{-1}$)	10	10	10	10	10	10
Dielectric constant (ϵ_0)	10.4	10.39	10.4	10.31	10.82	10.4
thermal conductivity (W/cm-K)	1.3	1	1.3	2.85	0.2	1.3
trap concentration (cm^{-3})	1×10^{17}	-	-	-	-	1×10^{19}

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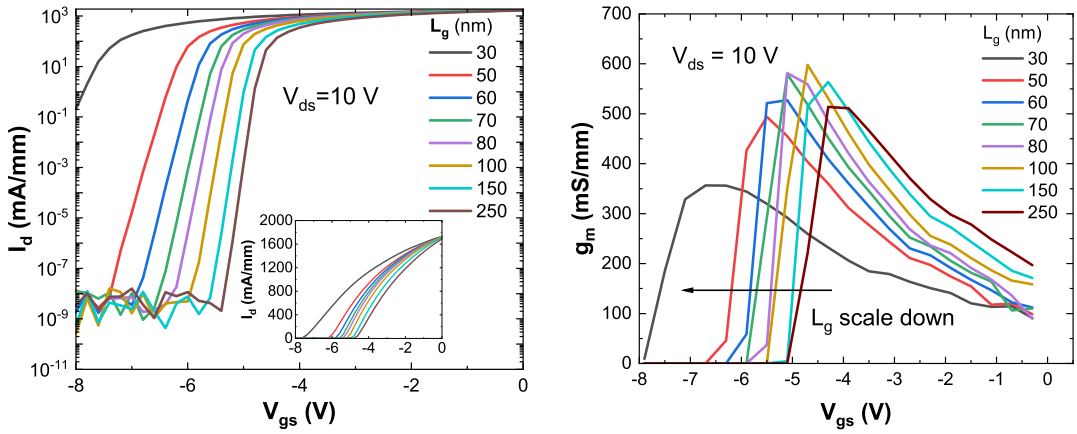
5.2 Scale down of gate length

Scale down of gate length (L_g) is the most direct way to improve f_T, but shortening the L_g would cause SCEs, resulting in a negative shift of the V_{th} and a drop in g_m, etc. The most fundamental problem is when the L_g is shortened, the control ability of the gate for the channel is reduced. So electrons can pass through the gate from the bottom of the channel, resulting in a decrease of g_m and f_T. Therefore, this section will discuss the device characteristics of different L_g and find the L_g with the best frequency performance. DC characteristics at V_{ds}=10 V are shown in figure 5.3 and figure 5.4. As shown in figure 5.3 and figure 5.4, a reduction in L_g results in negative shifts for V_{th}, g_m , and f_T. C_g decreases proportionally as L_g shrinks, which is consistent with the definition of C_g. And our proposed T-gate and passivation layer can indeed improve the problem that the experimental C_g cannot be improved as expected. Figure 5.5 presents the DC and



(a) (b)

Figure 5.3: Different gate lengths of (a) transfer characteristics and (b) g_m.

RF performance at V_{ds}=10 V for different L_g. The black line represents $g_{m,peak}$, which represents the g_m maximum in the $g_m - V_{gs}$ curve. The red line represents C_g at $f_{T,peak}$ voltage. The blue line represents the f_T maximum in the $f_T - V_{gs}$ curve. g_m rises as

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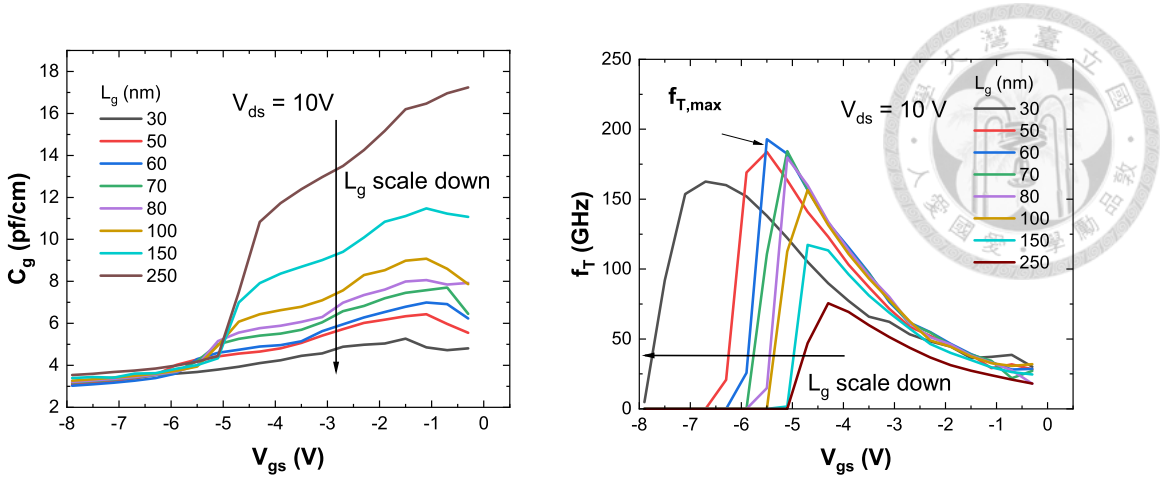

(a) (b)

Figure 5.4: Different gate lengths of (a) C_g and (b) f_T.

L_g shrinks at L_g>100 nm because the gate under this condition controls the channel well. Therefore, when L_g decreases, the drain current increases, and the $g_{m,peak}$ also increases. However, when L_g<100 nm, the gate's ability to control the channel gradually decreases, resulting in a decrease in $g_{m,peak}$. C_g decreases as L_g shrinks, roughly showing a linear change. When L_g>60 nm, f_T increases with the decrease of L_g, and under this condition, f_T is mainly dominated by C_g. The maximum value of f_T occurs at L_g=60 nm, which is 186 GHz. When L_g<60 nm, the SCEs are too severe, resulting in a decrease of g_m greater than that of C_g, and f_T decreases with the decrease of L_g. Under this condition, f_T is mainly dominated by g_m. Therefore, by reducing the influence of the short channel effect, the L_g can be continuously scaled down to obtain better RF performance. Figure 5.6 shows the device L_g scaling performance. The black line represents SS, which is calculated at I_d=10^{-3} mA/mm and V_{ds}=10 V. The red line represents DIBL, which is at I_d=10^{-3} mA/mm between V_{ds}=10 V and 0.1 V. SS and DIBL rise sharply at L_g <100 nm, which implies an enhanced short channel effect. When L_g scaled down to 30 nm, SS is 171 mV/dec, and DIBL is 282 mV/V, which means that there are serious SCEs that lead to the degradation of device characteristics.

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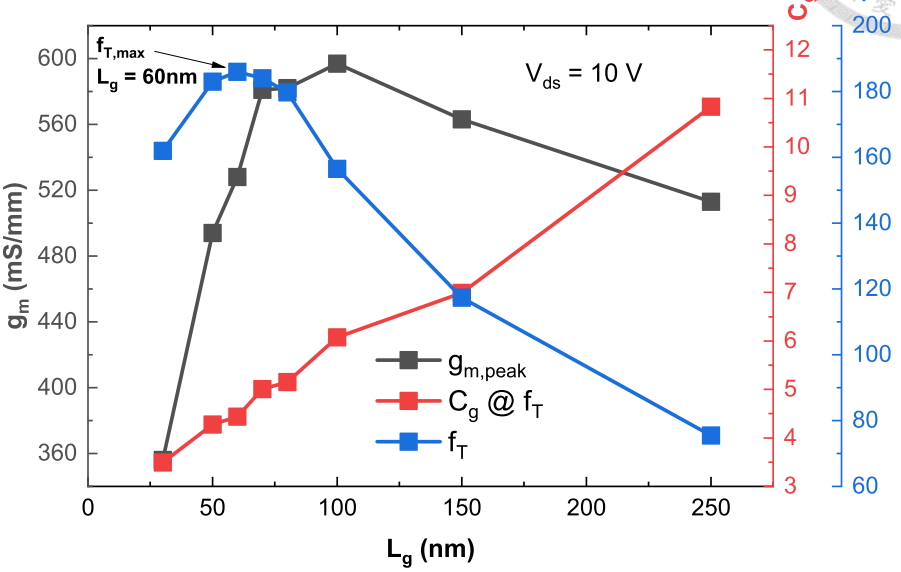

Figure 5.5: DC and RF performance scaled with L_g ranging from 250 to 30 nm.

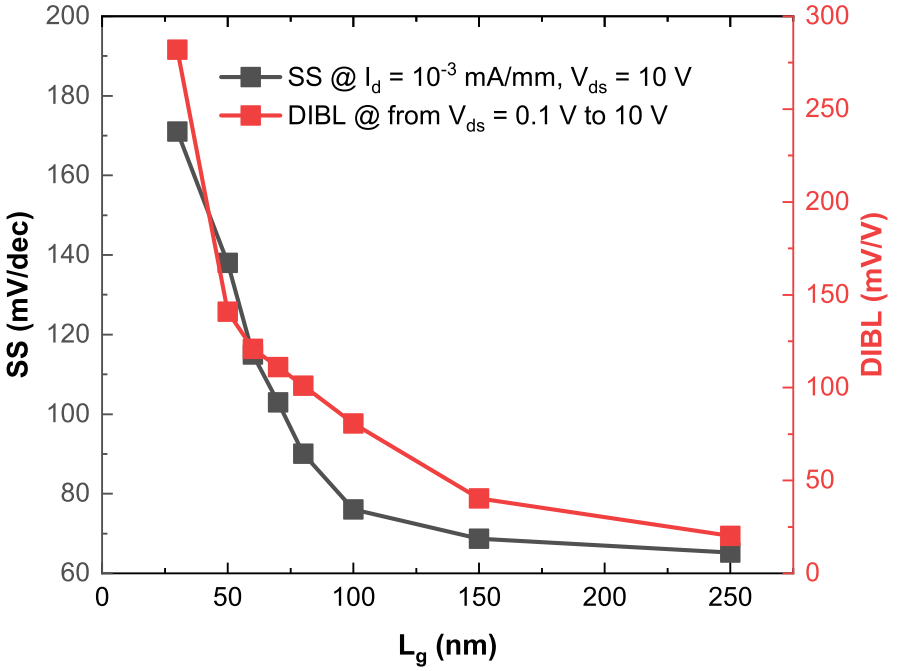

Figure 5.6: Performance of SS and DIBL scaled with L_g ranging from 250 to 30 nm.

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Table 5.2: The device performance of this work at V_{ds} = 10 V.

	This work
L_g(nm)	60
Barrier thickness (nm)	10
R_c (Ω·mm)	0.44
R_{sh} (Ω/sq)	175
f_T (GHz)	186
$g_{m,peak}$ (mS/mm)	528
DIBL (mV/V)	121
SS (mV/dec)	115
R_{on} (Ω·mm)	0.985

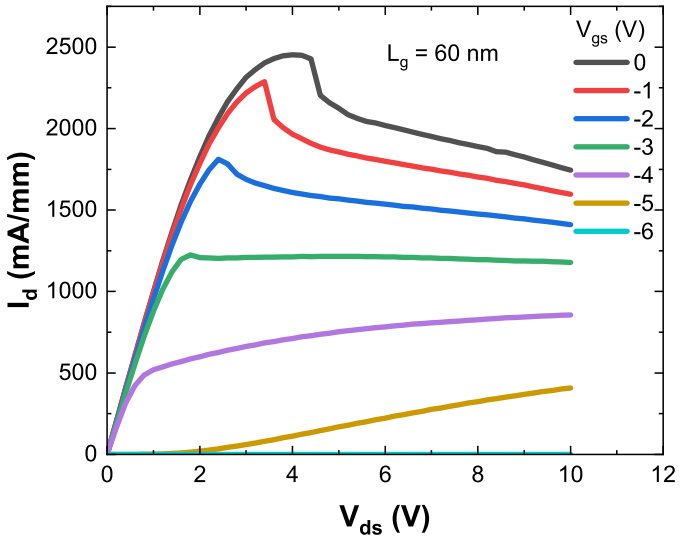

Figure 5.7: $I_d - V_{ds}$ characteristics of L_g=60 nm.

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Table 5.2 shows this structure of L_g = 60 nm at V_{ds}=10 V, DIBL and SS are 121 mV/V and 115 mV/dec respectively, which means that this structure can effectively suppress the short channel effect and make f_T and g_m achieve 186 GHz and 528 mS/mm, respectively.

5.3 Impact of contact resistance and sheet resistance on DC & RF characteristics

A good RF HEMT needs ohmic contacts with low contact resistance R_c. Lower R_c results in lower R_{on} and higher g_m and f_T. Therefore, we analyze the impact of contact resistance on DC & RF characteristics in this section. On the other hand, as mentioned above, R_s has a great influence on the electrical properties of the device. R_s is related to the 2DEG density and mobility of the channel, and the 2DEG density is determined by the epitaxial structure. Therefore, we will explore the relationship between 2DEG mobility and R_s and analyze the impact of R_s on DC & RF characteristics.

5.3.1 Contact resistance

The InAlGaN HEMTs with R_c of 0.51 Ω·mm extracted f_T of 102 GHz [5]. The InAlGaN HEMTs with regrown ohmic contact yielded R_c of 0.27 Ω·mm, which achieved f_T up to 230 GHz [18]. The InAlN HEMTs with R_c of 0.05 Ω·mm is measured, which exhibited f_T of 250 GHz [28]. We simulate DC characteristics of different R_c with L_g=60 nm. Figure 5.8 shows extracted R_c from 0.766 to 0.056 Ω·mm and R_s of 175 Ω/sq.

Figure 5.9(a) shows that maximum drain current density ($I_{d,max}$) obtained corresponding to R_c of 0.766 Ω·mm and R_c of 0.056 Ω·mm is 1506 mA/mm and 2506 mA/mm,

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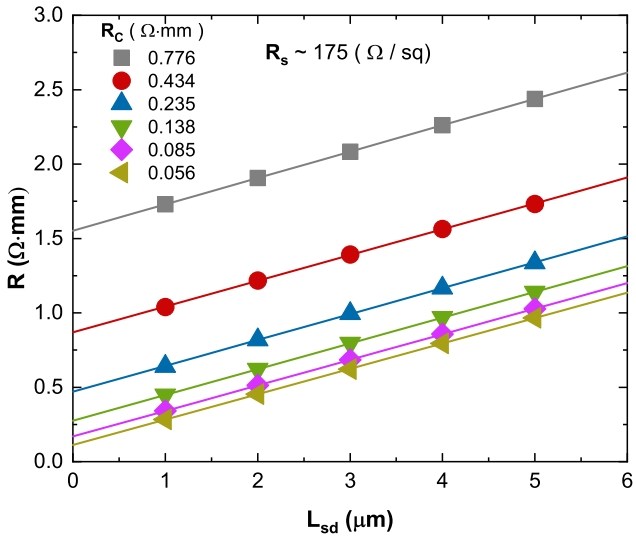
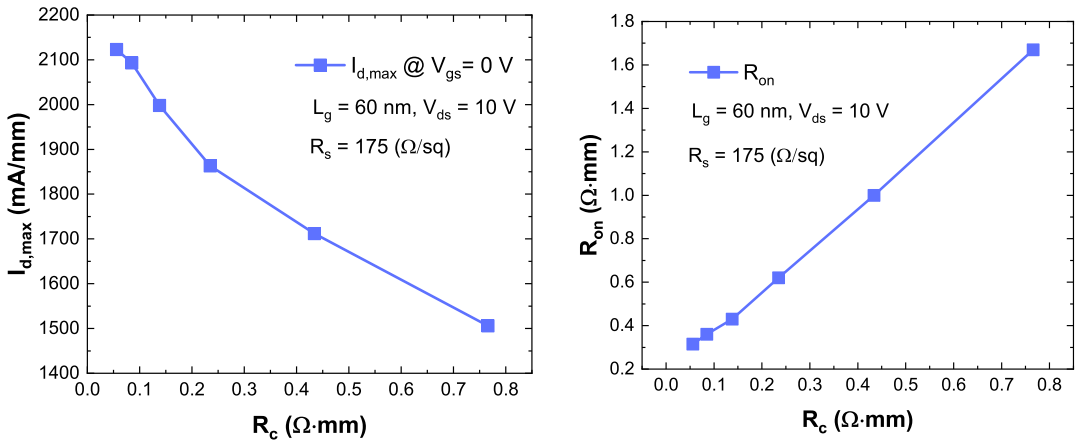


Figure 5.8: TLM simulation results.

respectively at V_{gs}=0 V and V_{ds}=10 V. It clearly demonstrates that lower the R_c, higher is the drain current density. It is known that $I_{d,max}$ is directly proportional to the RF output power of a transistor. So improving $I_{d,max}$ is an important factor for high power applications [29]. Figure 5.9(b) shows R_{on} corresponding to different R_c. It clearly demonstrates that R_c is proportional to R_{on} at V_{gs}=0 V. To reduce the system's power losses, it is preferable to reduce R_{on}. Therefore, a lower R_{on} is essential for switching applications. From the above, reducing R_c is the critical factor to improve the performance of high-power applications. Figure 5.10(a) depicts $g_{m,peak}$ corresponding to different R_c at V_{ds}=10 V.



(a) (b)

Figure 5.9: Different contact resistance of (a) $I_{d,max}$ (b) R_{on}.

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The $g_{m,peak}$ for R_c of 0.056 Ω·mm is up to 758 mS/mm. Since lowering R_c increases I_d and thus increases g_m, it demonstrates that lower the R_c, higher is the $g_{m,peak}$ as shown in figure 5.10(a). Figure 5.10(b) shows C_g corresponding to different R_c at V_{ds}=10 V at the voltage of f_T. It demonstrates that lower the R_c, higher is the C_g as shown in figure 5.10(b). Because the lower R_c can provide a larger I_d, the change of the carrier inside the device also increases, so the C_g also increases.

Since reducing R_c increases g_m, and f_T is proportional to g_m, smaller values of R_c can achieve higher f_T as shown in figure 5.10(c). Therefore reducing R_c can improve the RF performance of the device.

5.3.2 Sheet resistance

Sheet resistance determines device DC and RF characteristics. And R_s is proportional to 2DEG mobility. Because 2DEG mobility will be affected by 2DEG density or barrier material and thickness. And the process will also have a critical impact on 2DEG mobility. Therefore, we need to discuss the influence of different 2DEG mobility on device characteristics. We simulate R_s corresponding to different 2DEG mobility and constant 2DEG density. Analyze the properties of devices at different R_s.

Table 5.3: Sheet resistance corresponds to different 2DEG mobility.

μ_e (cm^2/Vs)	R_s (Ω/sq)
1240	250
1550	200
1782	175
2015	153
2170	148

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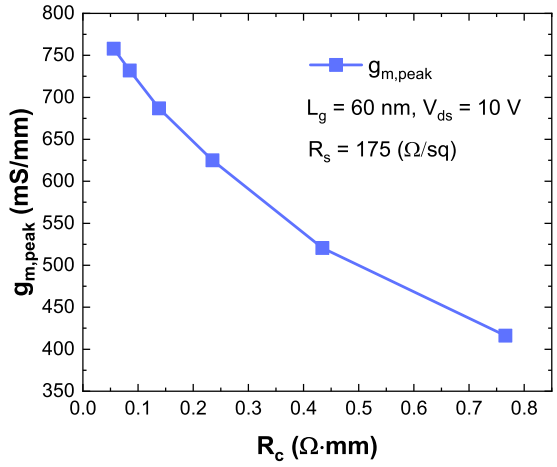
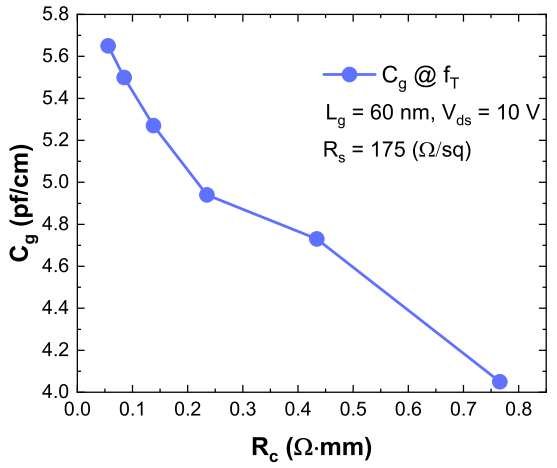


(a)



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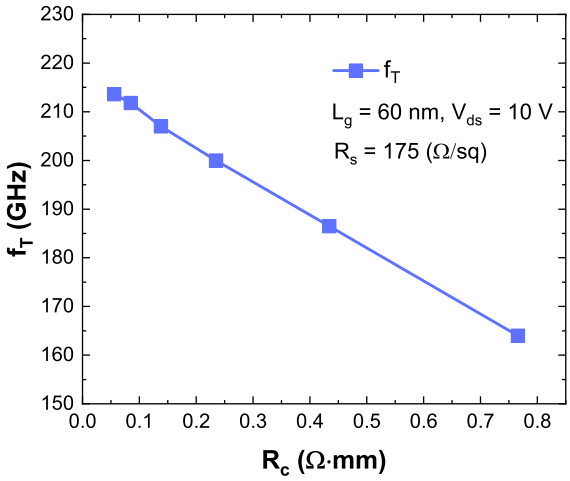

(c)

Figure 5.10: Different contact resistance of (a) $g_{m,peak}$ (b) C_g (c) f_T.

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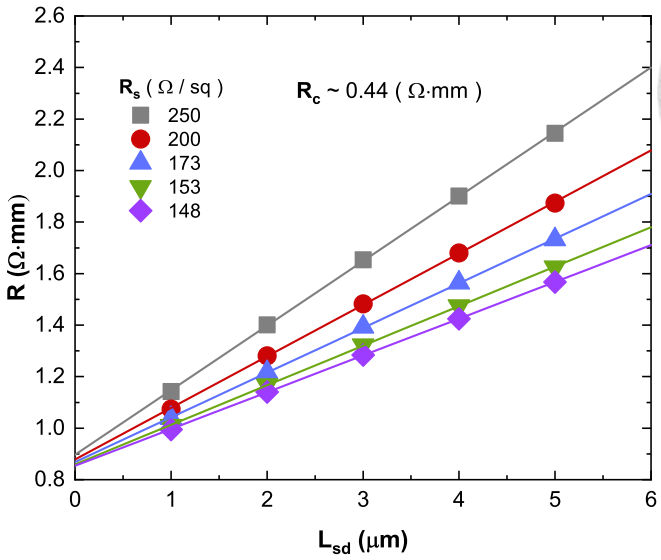
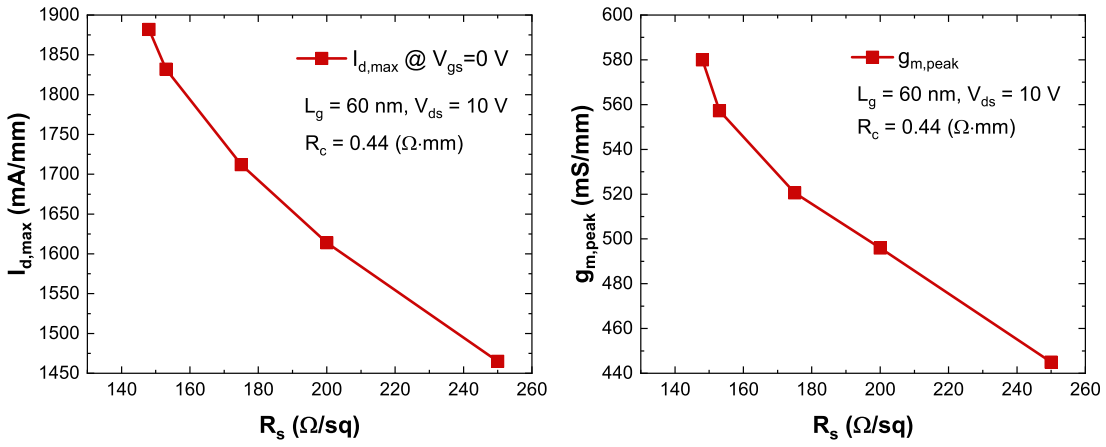


Figure 5.11: TLM simulation results.

Figure 5.11 shows extracted R_s from 250 to 148 Ω/sq and R_c of 0.44 Ω·mm. Table 5.3 shows that the larger the 2DEG mobility, the smaller the R_s. Figure 5.12(a) shows that $I_{d,max}$ corresponds to R_s of 250 to R_s of 148 Ω/sq at V_{gs}=0 V and V_{ds}=10 V. It demonstrates that lower the R_s, higher is the drain current density, since higher mobility provides higher current density. Figure 5.12(b) shows that $g_{m,peak}$ corresponds to R_s of 250 to R_s of 148 Ω/sq at V_{gs}=0 V and V_{ds}=10 V. Since drain current density is proportional to g_m, figure 5.12(a) and (b) will show the same trend.



(a) (b)

Figure 5.12: Different sheet resistance of (a) $I_{d,max}$ (b) g_m.

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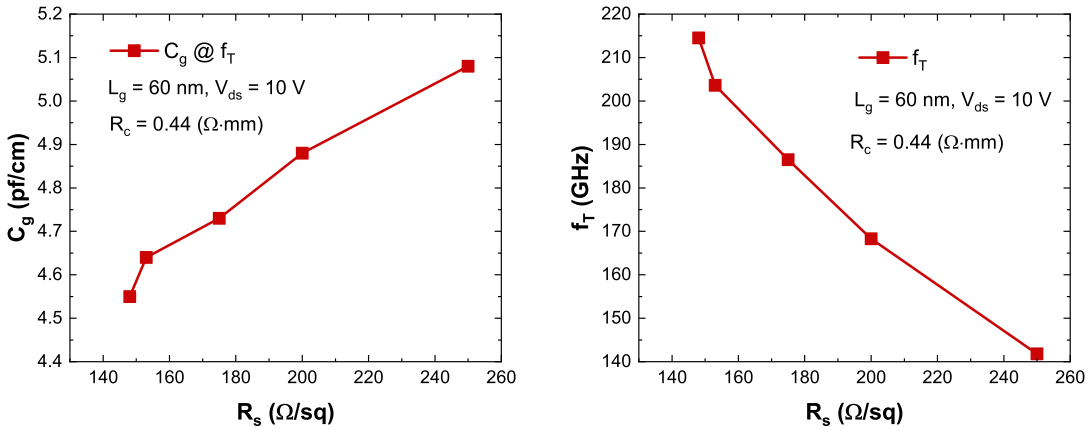
Figure 5.13(a) shows that lower R_s has lower C_g. Because the lower R_s represents higher mobility, high mobility can provide the carrier with faster speed and smaller delay time. As fewer carriers accumulate in the channel, C_g decreases. As shown in figure 5.12(a) and figure 5.13(a), the smaller R_s makes the g_m larger and the C_g smaller, so that the f_T is higher as shown in figure 5.13(b). As shown in figure 5.14, as mobility increases, the variation in carrier density with the change in V_{gs} decreases. Therefore, increasing mobility means decreasing R_s can reduce C_g and improve the RF performance of the device. This also means that when the speed of the carrier in the device is increased, the carrier can keep up with the higher operating frequency, and therefore has a higher f_T.

Since reducing R_s can increase g_m and reduce C_g at the same time, increasing 2DEG mobility will significantly improve the characteristics of devices in high-frequency applications. It can be seen from figure 5.14 that when V_{gs} changes, the carrier density of high



(a) (b)

Figure 5.13: Different sheet resistance of (a) C_g (b) f_T.

electron mobility changes less, so the calculated C_g is also smaller, which is consistent with figure 5.13.

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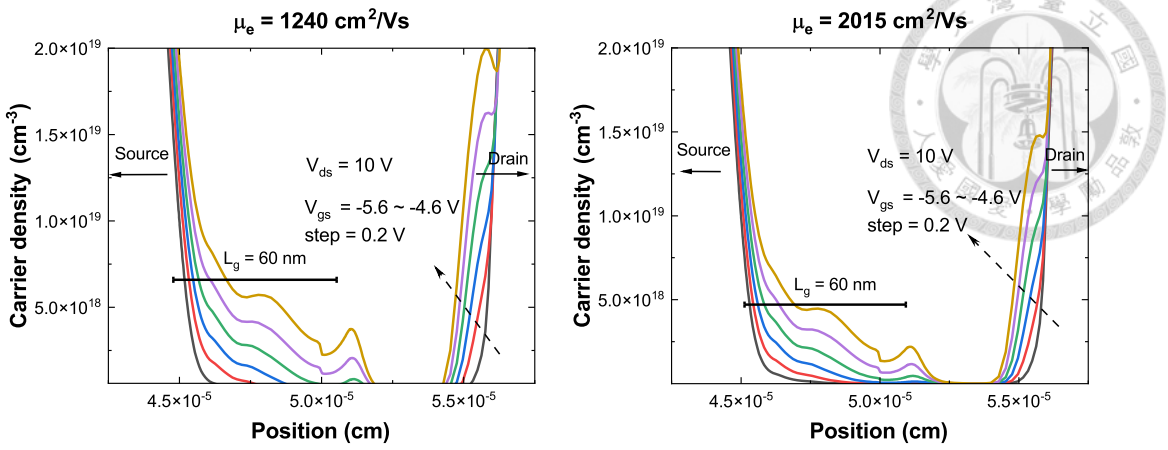

(a) (b)

Figure 5.14: Distribution of carrier density of (a) R_s=250 Ω/sq (b) R_s=153 Ω/sq.

5.4 Discuss the influence of high/low-k passivation layer and the design of T-gate structure

Generally, in GaN-HEMTs, if the L_g is to be shortened, the resistance R_g of the gate electrode will increase accordingly. In order to overcome this problem, the design of T-gate is adopted. The resistance of the gate is reduced by increasing the cross-sectional area above, as shown in figure 5.15. On the sidewall or T-gate head, although they do not directly contact the capping layer, the influence of the gate can still be transmitted to the channel through the passivation layer, and affect the density of 2DEG and the gate The equivalent length of the length. When the gate is equivalently increased by the passivation layer, the effect of shortening the gate length disappears or makes it difficult to optimize f_T. In order to solve the above problems, we choose low-K material or air as the side wall, so that the gate control force cannot be transmitted from the side wall, so as to reduce the equivalently increased L_g and the f_T is pushed towards better performance. However, switching to low-k would reduce the breakdown voltage, so we would explore the effect of different passivation layers on device performance[30].

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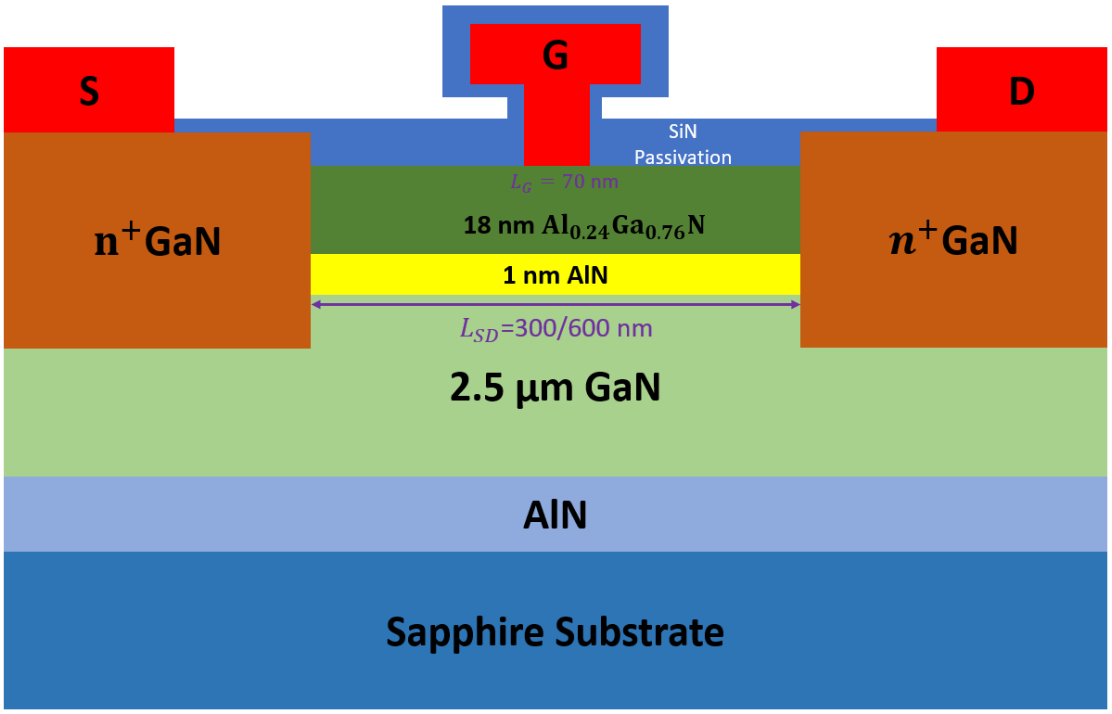

Figure 5.15: Schematic of T-gate [9].

Table 5.4: Parameters of different passivation layer materials.

Material	Dielectric constant (ϵ_r)
SiO_2	3.7
Si_3N_4	7.5
Air	1

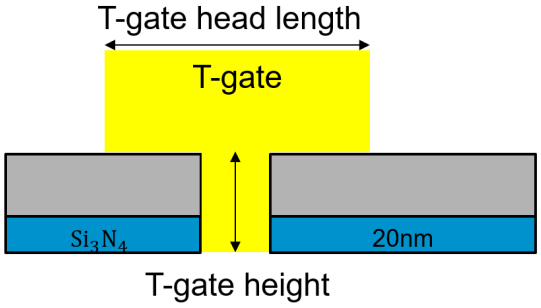

Figure 5.16: Schematic of the T-gate for this work.

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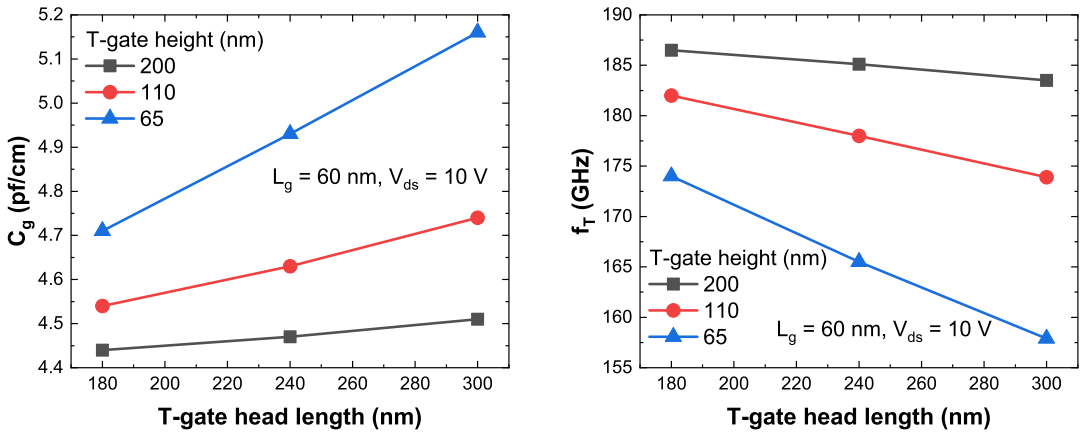
Figure 5.16 shows our designed T-gate structure, where the T-gate height is 20 nm-thick Si_3N_4 plus the thickness of the gray area. When changing the T-gate height, only the thickness of the gray area is changed, and Si_3N_4 remains unchanged because Si_3N_4 and GaN have good passivation, which reduces the occurrence of fermi-level pinning.

We will simulate the device characteristics of different T-gate structures with L_g=60 nm designs in SiO_2, Si_3N_4, and air passivation layer materials. Changing the passivation layer material only changes the gray area in figure 5.16. Table 5.4 shows the dielectric constant of different passivation layer materials. Table 5.4 shows the device characteristics of the passivation layers corresponding to SiO_2, Si_3N_4, and air with different T-gate structures. The T-gate structures consist of T-gate heights of 200 nm, 110 nm, and 65 nm. The T-gate structures consist of T-gate head lengths of 180 nm, 240 nm, and 300 nm.



(a) (b)

Figure 5.17: Different T-gate structures with SiO_2 passivation layer of (a) C_g (b) f_T.

Since T-gate affects the carrier density through the passivation layer, the range of the affected carrier density becomes larger, and the equivalent length representing the gate length increases. This increases the C_g and decreases the f_T of the device. This means that the T-gate increases the C_g and decreases the f_T of the device. As shown in figure 5.17, C_g is the gate capacitance of L_g=60 nm of the device at the voltage where f_T is the

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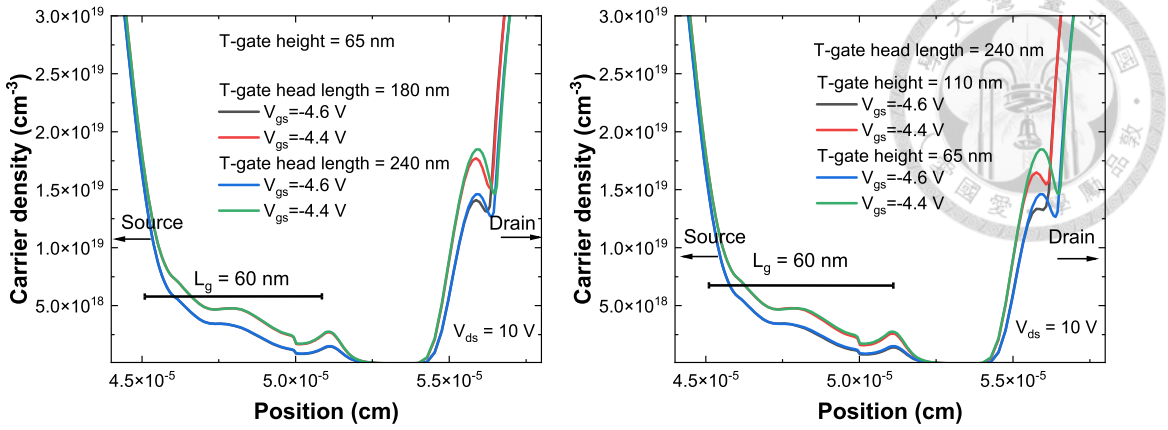

Figure 5.18: Distribution of carrier density at V_{ds}=10 V with different (a) T-gate head lengths and (b) T-gate heights.

maximum value and f_T represents the f_T maximum value of L_g=60 nm of the device at V_{ds}=10 V. When the T-gate height is 200 nm, since the T-gate is too far from the channel to have little effect on the carriers of the channel, the change of the T-gate structure hardly affects the C_g and f_T of the device. When the T-gate height is 110 nm, the T-gate affects the carrier density of the channel because the T-gate is closer to the channel. And when the T-gate head length is longer, the larger the range of carriers affected by the T-gate increases the effective gate length and makes C_g increase and f_T decrease. As shown in figure 5.18, when the T-gate head length is longer, or the T-gate height is shorter, the influence of the T-gate on the channel carriers is greater. It can be found that the T-gate depletes more carriers, and the change of these carriers will generate additional capacitance, increasing the C_g of the device. Figure 5.19 shows different T-gate structures with Si_3N_4 passivation layer of performance and this has the same trend as figure 5.17. As shown in figure 5.20(a), C_g with Si_3N_4 passivation layer is higher than C_g with SiO_2 passivation layer. The reason for this is that the dielectric constant of Si_3N_4 is higher than that of SiO_2, which means that T-gate has a stronger ability to affect carriers through Si_3N_4. Therefore f_T with Si_3N_4 passivation layer is lower than f_T with SiO_2 passivation layer in figure 5.20(b). As shown

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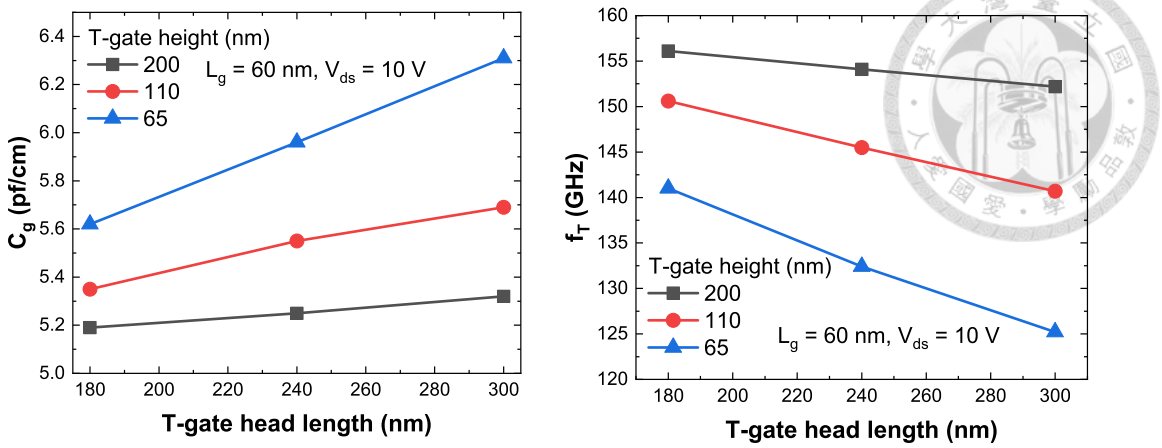
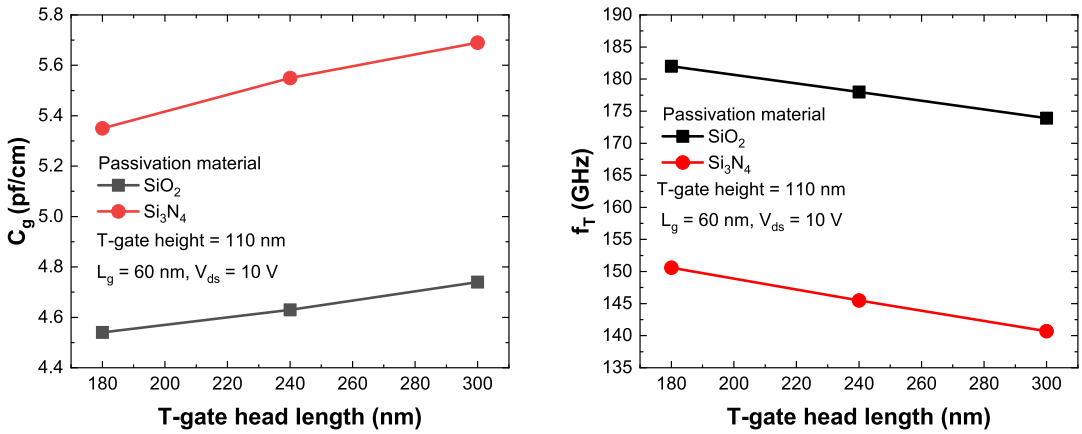


(a) (b)

Figure 5.19: Different T-gate structures with Si_3N_4 passivation layer of (a) C_g (b) f_T.

in figure 5.20, under the same T-gate structure, the f_T of the SiO_2 passivation layer is about 32 GHz higher than that of the Si_3N_4 passivation layer.



(a) (b)

Figure 5.20: Different T-gate head lengths correspond to SiO_2 and Si_3N_4 passivation layer with 110 nm-thick T-gate height of (a) C_g (b) f_T.

Figure 5.21 shows the channel carrier distribution for the same T-gate height and T-gate head length corresponding to SiO_2 and Si_3N_4 passivation layers. When V_{gs} changes, the Si_3N_4 passivation layer makes the channel carriers affected by the T-gate in a larger range and in more quantities, so the C_g of the device will be larger than that of the SiO_2 passivation layer.

The structure of the T-gate also has a great influence on the breakdown voltage. Our

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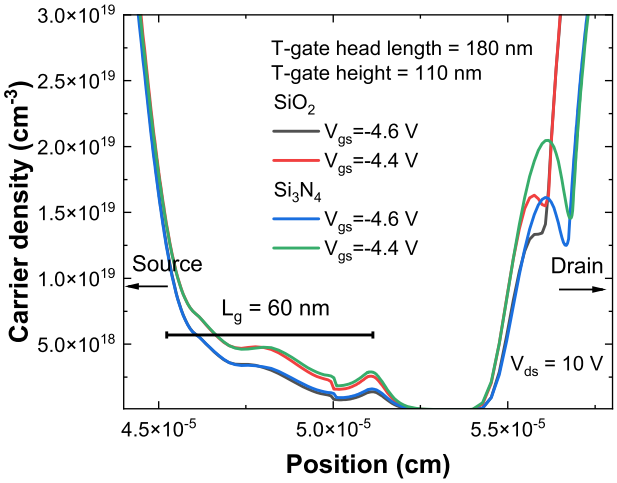
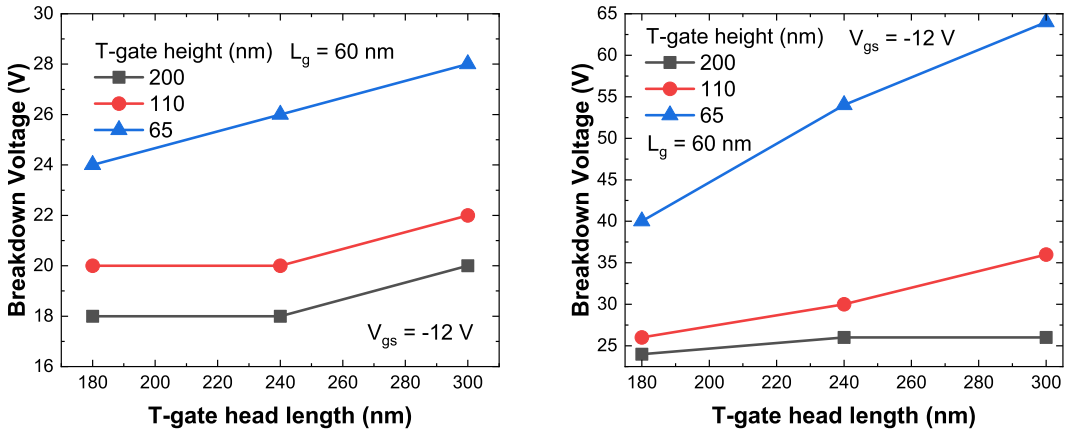


Figure 5.21: Distribution of carrier density with T-gate head length of 180 nm and T-gate height of 110 nm corresponds to SiO_2 and Si_3N_4 passivation layer.



(a) (b)

Figure 5.22: The breakdown voltage of different T-gate structures with (a) SiO_2 (b) Si_3N_4 passivation layer.

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definition of breakdown is the voltage at off-state at which the maximum electric field of the channel is 3.3 MV/cm[31]. Because the T-gate depletes the carrier of the channel to increase the channel resistance, the electric field is more uniformly distributed between the gate and the drain, and the maximum electric field at the gate edge is reduced. Therefore the breakdown voltage of the device increases. When the influence of the T-gate on the carriers in the channel increases, the breakdown voltage of the device increases, and f_T decreases due to the capacitance effect. As shown in figure 5.22, T-gate head length lengthening or T-gate height reduction would increase the breakdown voltage. And the breakdown voltage of the Si_3N_4 passivation layer is greater than that of the SiO_2 passivation layer because the high-k Si_3N_4 makes the T-gate deplete more carriers in the channel.

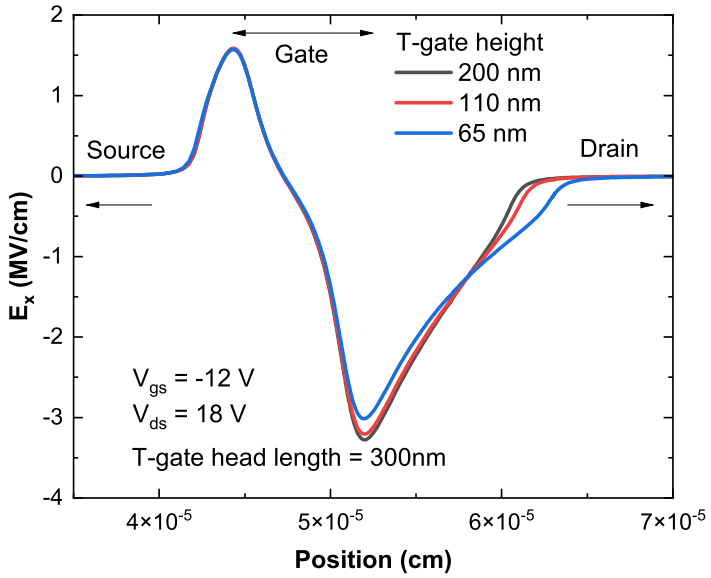

Figure 5.23: Electric field along the channel at V_{gs}=-12 V and V_{ds}=18 V.

Figure 5.23 shows the electric field along the channel in the off-state. It can be seen that when the T-gate head length is the same, the smaller the T-gate height is, the lower the electric field peak at the gate edge is, and the electric field near the drain increases. Figure 5.24 shows the carrier distribution along the channel in the off-state. It can be seen that when the T-gate head length is the same, the smaller the T-gate height is, the more carriers in the channel are depleted, which reduces the carrier density in the channel.

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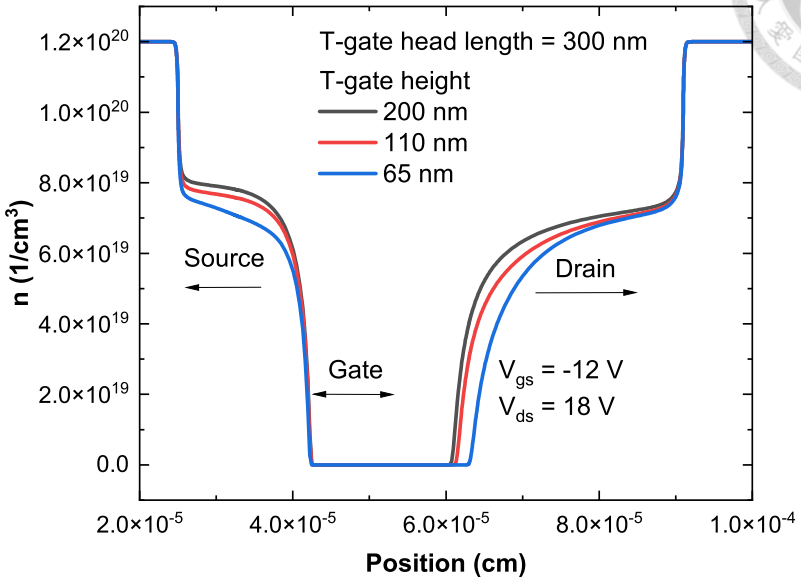

Figure 5.24: Carrier distribution along the channel at V_{gs}=-12 V and V_{ds}=18 V.

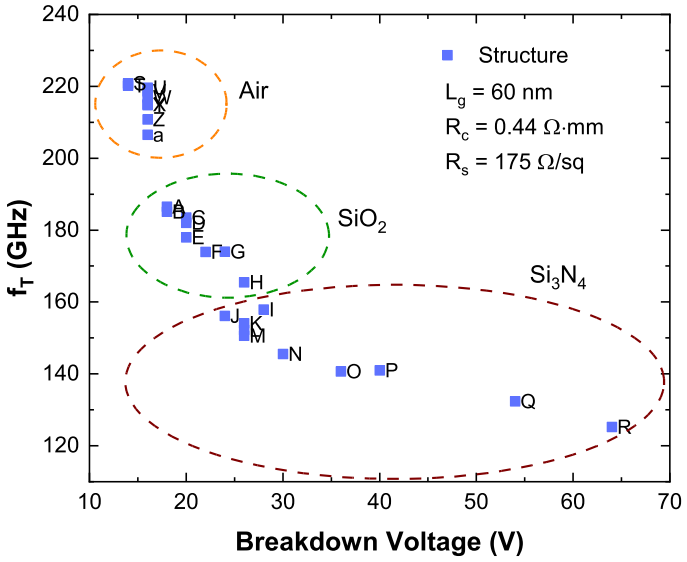

Figure 5.25: f_T and V_{BR} of different T-gate structures correspond to SiO_2, Si_3N_4 and air passivation layers.

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Table 5.5: Different T-gate structures with different passivation layer materials.

Structure	Material	T-gate height (nm)	T-gate head length (nm)
A	SiO_2	200	180
B	SiO_2	200	240
C	SiO_2	200	300
D	SiO_2	110	180
E	SiO_2	110	240
F	SiO_2	110	300
G	SiO_2	65	180
H	SiO_2	65	240
I	SiO_2	65	300
J	Si_3N_4	200	180
K	Si_3N_4	200	240
L	Si_3N_4	200	300
M	Si_3N_4	110	180
N	Si_3N_4	110	240
O	Si_3N_4	110	300
P	Si_3N_4	65	180
Q	Si_3N_4	65	240
R	Si_3N_4	65	300
S	Air	200	180
T	Air	200	240
U	Air	200	300
V	Air	110	180
W	Air	110	240
X	Air	110	300
Y	Air	65	180
Z	Air	65	240
a	Air	65	300

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Table 5.6: Results of different T-gate structures with different passivation layer materials.

Structure	$g_{m,peak}$ (mS/mm)	C_g (pf/cm)	f_T (GHz)	V_{BR} (V)
A	528	4.44	186	18
B	528	4.47	185	18
C	528	4.51	184	20
D	530	4.54	182	20
E	529	4.63	178	20
F	529	4.74	174	22
G	530	4.71	174	24
H	531	4.93	166	26
I	531	5.16	158	26
J	534	5.19	156	24
K	534	5.25	154	26
L	534	5.32	152	26
M	535	5.35	151	26
N	535	5.55	146	30
O	534	5.69	141	36
P	535	5.62	141	40
Q	534	5.96	132	54
R	537	6.31	125	64
S	528	3.81	221	14
T	528	3.81	220	16
U	528	3.82	220	16
V	528	3.84	219	16
W	527	3.87	217	16
X	527	3.90	215	16
Y	526	3.90	215	16
Z	526	3.97	211	16
a	525	4.05	207	16

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Material represents the material of the passivation layer. V_{BR} is the breakdown voltage. As shown in figure5.25 and the table 5.7, in order to improve the RF performance of the device, using air as the passivation layer can achieve higher f_T. To increase the breakdown voltage of the device, Si_3N_4 can be used as the passivation layer to have a higher breakdown voltage. The use of SiO_2 as the passivation layer has a balanced f_T and breakdown voltage.

5.5 Unit current gain frequency f_T and unit power gain cutoff frequency f_{max}

This section discusses the RF performance of the device. We first introduce small-signal modeling of GaN-HEMTs. As shown in figure 5.26, the equivalent circuit of the small signal model has eleven components, and these circuit components have their respective physical meanings in the device's operation.

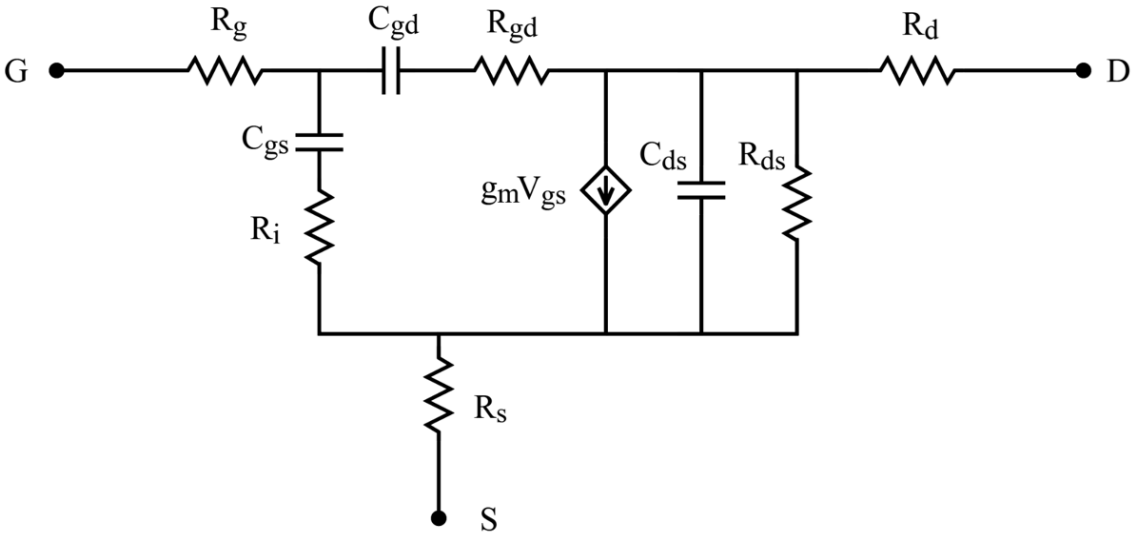

Figure 5.26: Small-signal model equivalent circuit of GaN-HEMTs [10].

The capacitances C_{gs} and C_{gd} reflect the variation of gate charge with changes in V_{gs}

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and V_{ds} respectively. C_{gs} is the larger quantity and usually about 10 times the size of C_{gd} and C_{ds}. The effects of geometric capacitance between the source and drain electrodes are taken into account by C_{ds}. The frequency of the device with unity gain is typically determined by these capacitances. They grow smaller as the device becomes smaller and have an inverse relationship with the maximum frequency of operation[32].

R_{ds} is the changing of drain current by the change of drain voltage. R_i means the lumped of distributed channel resistances. R_d, R_s, and R_g are the resistance of the metal of the drain, source, and gate, respectively.

Two significant indicators—the unity current-gain cutoff frequency (f_T) and the unity power gain cutoff frequency (f_{max})—are provided to characterize the RF performance of GaN-HEMTs and serve as a reference for choosing the suitable GaN-HEMTs for RF applications. f_T is the frequency at which the magnitude of short-circuit current gain h_{21} equals unity (or 0 dB), which can be expressed as

$$f_T = \frac{1}{2\pi\tau} = \frac{1}{2\pi}\frac{v_{e-eff}}{L_g} = \frac{1}{2\pi}\frac{g_m}{C_g}, \tag{5.1}$$

$$g_m = \frac{\partial I_d}{\partial V_{gs}}, \tag{5.2}$$

$$C_g = C_{gs} + C_{gd}, C_{gs} = \frac{\partial Q_g}{\partial V_{gs}}, C_{ds} = \frac{\partial Q_g}{\partial V_{ds}} \tag{5.3}$$

Equation (5.1) means the electron transition time under the gate. C_g is the total capacitance of the device seen from the gate. Q_g is the total carrier of the device seen from

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the gate. v_{e-eff} is the effective electron velocity. And f_{max} can be written as

$$f_{max} = \frac{f_T}{2\sqrt{\frac{(R_i+R_s+R_g)}{R_{ds}}} + (2\pi f_T)R_g C_{gd}}, \tag{5.4}$$

R_g, R_d, and R_s are extrinsic elements of the device. In our simulation, only intrinsic elements can be calculated. Therefore, when calculating f_{max}, it is necessary to use the extrinsic elements of the experimental results. Here we use the equation (5.2) to simulate

Table 5.7: Extrinsic elements from the experiment results [11].

Extrinsic element	Ω·mm
R_g	0.37
R_s	0.05
R_d	0.12

g_m under different V_{gs} and V_{ds}. As shown in figure 5.27, $g_{m,peak}$ can be as high as 590 mS/mm at V_{ds}=7 V, and there is still 528 mS/mm at V_{ds}=10V, which means that this device has a good suppression of the short channel effect caused by the increase of V_{ds}. It can be noticed here that it has reached its peak value. The g_m begins to drop quite severely as the V_{gs} is increased. The reason is that the g_m also significantly decreases after the peak value due to the self-heating effect, which means the v_e is reduced. Then analyze the capacitance part. As shown in figure 5.28, since the carrier under the gate increases greatly under V_{gs}=V_{th}, there are more changes in Q_g, resulting in a sharp rise in C_g. When V_{gs} is larger than V_{th}, the effect of increasing V_{gs} on C_g decreases, and it can be found that C_g presents a slight upward trend.

Then analyze the high-frequency performance part, f_T with different V_{gs} and V_{ds} can be seen in figure 5.29. f_T can be calculated by equation (5.1). As the results certify,

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InAlGaN/GaN HEMTs demonstrate that 190 GHz of f_T can be reached at the operation bias point of V_{ds}=7 V and V_{gs}=-5.1 V, which is the f_T maximum of the device. As the V_{gs} is increased, it can be seen that the f_T begins to decline pretty drastically after reaching its maximum value. The reason is that the g_m decreases significantly after the peak value, and the change in C_g is smaller. f_{max} with different V_{gs} and V_{ds} can be seen in figure 5.30. f_{max} can be calculated using the extrinsic elements of table 5.7 and equation (5.4). As the results show, InAlGaN/GaN HEMTs demonstrate that 339 GHz of f_{max} can be reached at the operation bias point of V_{ds}=10 V and V_{gs}=-5.5 V. From equation (5.4), it can be known that f_{max} and f_T have a positive correlation, so we can also improve the f_{max} of the device by optimizing the epitaxial structure. However, R_g also greatly influences the f_{max} of the device. Even if the device has a good f_T performance, if the R_g is too large, the performance of the f_{max} will be reduced. Therefore, reducing the R_g value in the process is also a key factor in improving the RF performance of the device. Our designed epitaxial structure f_T can reach 186 GHz, and f_{max} reach 339 GHz with L_g=60 nm at V_{ds}=10 V. Compared with the previous experimental results, our optimized epitaxial structure can greatly improve the RF characteristics.

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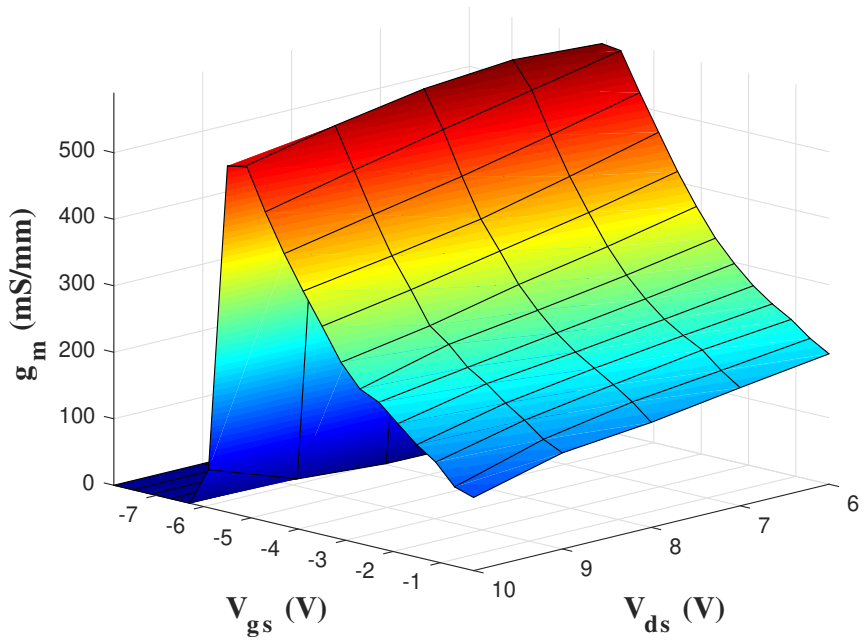

Figure 5.27: Extracted g_m of AlInGaN/GaN HEMTs with L_g=60 nm as a function of V_{ds} and V_{gs}.

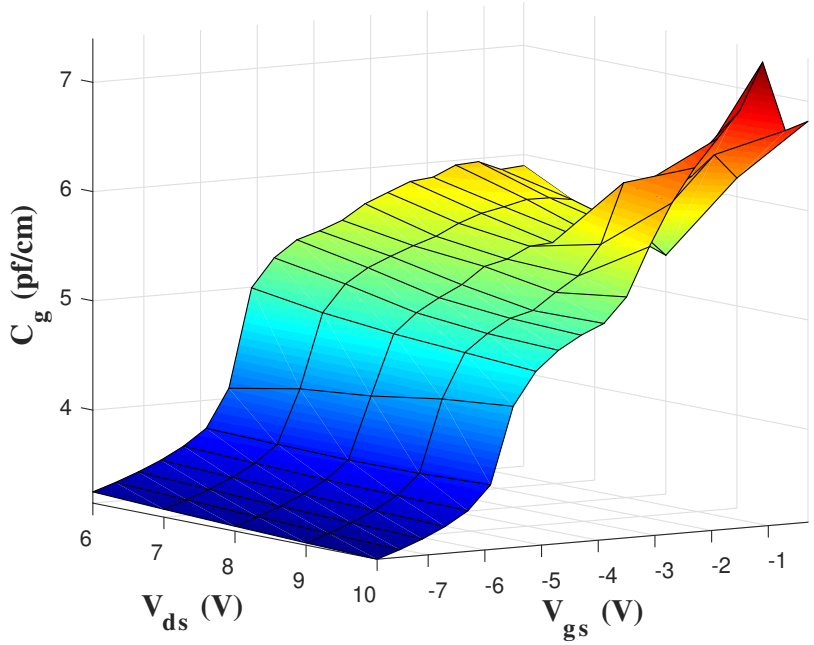

Figure 5.28: Extracted C_g of AlInGaN/GaN HEMTs with L_g=60 nm as a function of V_{ds} and V_{gs}.

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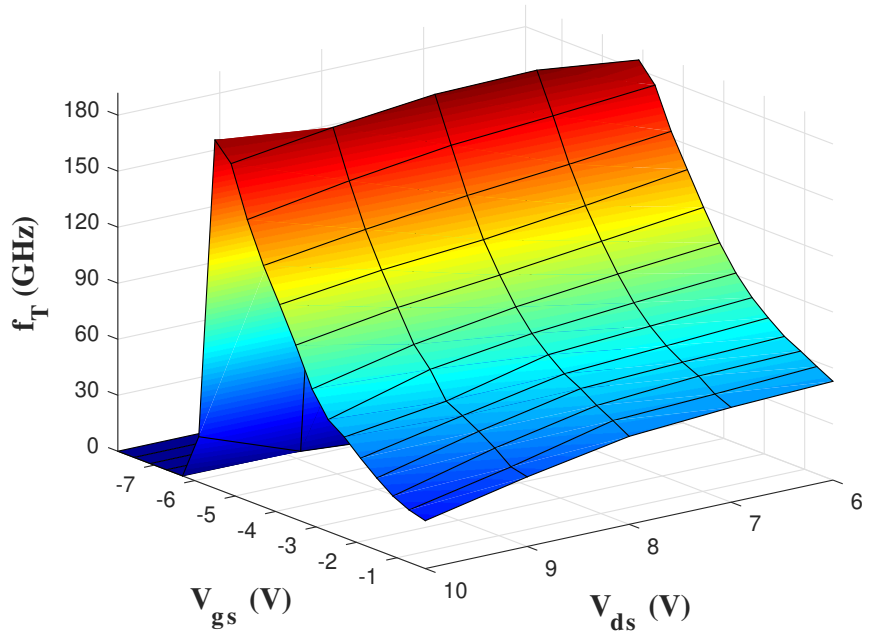

Figure 5.29: Extracted f_T of AlInGaN/GaN HEMTs with L_g=60 nm as a function of V_{ds} and V_{gs}.

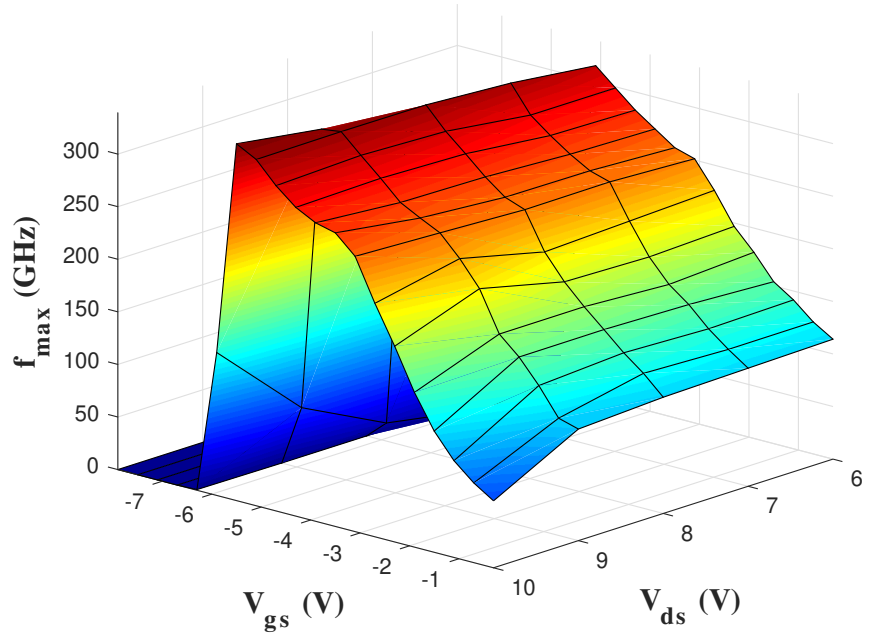

Figure 5.30: Extracted f_{max} of AlInGaN/GaN HEMTs with L_g=60 nm as a function of V_{ds} and V_{gs} through extrinsic elements[11] .

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Chapter 6

Conclusion

In this thesis, the experimental measurement results are fitted first to verify the correctness of the simulation method. The problem of experimental epitaxial structure is analyzed and optimized. We noticed that excessive C_g and SCEs and high R_s limit the f_T of the device. We propose to use AlInGaN as the barrier layer. We use the large polarization of AlInGaN to increase the 2DEG density of the device while avoiding the problem of lattice mismatch. It can reduce the R_s of the device and improve the electrical properties of the device. Apply C-doped buffer to reduce the channel thickness, and add AlGaN back-barrier to suppress the SCEs of the device. We then discuss the electrical properties of our proposed epitaxial structure. Analyze the effect of gate length, contact resistance, and sheet resistance on component performance. We find out that the device has the best RF performance when L_g=60 nm and find that optimizing R_c and R_s can significantly improve the device characteristics. Then, the influence of different T-gate and passivation layers on device characteristics are discussed, and the application of air, SiO_2, and Si_3N_4 as passivation layer materials to RF devices. Using air as a passivation layer can effectively reduce the capacitance effect generated by the T-gate and has the best

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RF characteristics, but it has a lower breakdown voltage. Using SiO_2 as the passivation layer can provide more balanced RF characteristics and breakdown voltage of the device. Using Si_3N_4 as the passivation layer reduces the RF characteristics of the device due to the capacitance effect generated by the T-gate. Still, it can increase the breakdown voltage of the device. Finally, using the experimentally measured extrinsic parameters to evaluate the f_{max} of the device, it is expected that the device can reach f_T of 186 GHz and f_{max} of 339 GHz at V_{ds}=10 V and L_g=60 nm.

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