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增強型氮化鎵電晶體導通暫態分析與閘極電阻最佳化設計

Turn-on Transition Analysis of Enhanced Mode GaN Transistors and Gate Resistance Optimization

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增強型氮化鎵電晶體導通暫態分析與閘極電阻最佳化設計

Turn-on Transition Analysis of Enhanced Mode GaN Transistors and Gate Resistance Optimization

本論文係張騰君（學號 R07921032）在國立臺灣大學電機工程學系完成之碩士學位論文，於民國 110 年 1 月 28 日承下列考試委員審查通過及口試及格，特此證明。

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中文摘要

近年來，高切換頻率之功率轉換器被廣泛應用於各式各樣的電子消費性產品中。高切換頻率功率轉換器有許多優點，包括更高的功率密度、更快速的暫態響應。隨著此趨勢，寬能隙元件如氮化鎵元件逐漸崛起，對比起傳統矽元件，氮化鎵元件更適合應用在高切換頻率的功率轉換器。然而在高頻應用下，氮化鎵元件的閘極驅動存在挑戰，相較於其他元件，氮化鎵元件的閘極較為脆弱，會因為電路板上寄生元件產生的額外電壓導致閘極過壓進而導致元件崩潰，此時閘極電路上的電阻扮演著抑制高頻效應的角色，但是傳統上設計閘極電阻的方式並未完善而會產生過度設計的問題。本論文提出針對增強型氮化鎵元件的驅動電路上閘極電阻設計最佳化，藉由以結構建立的氮化鎵元件等效電路模型，並運用雙脈衝實驗分析氮化鎵元件的切換行為，使用數學建模，找出在不同切換條件下合理的閘極電阻設計區間，也運用電腦軟體分析實體電路上的寄生電感參數，藉由還原真實寄生參數增加數學模型的精準度，並且透過電路模擬軟體與實際量測驗證模型，計算在不同閘極電阻下的切換損耗，以此論文之方式可以更精確地設計驅動氮化鎵元件的閘極電阻，使得過壓現象能避免，並且透過實際驗證切換損耗在設計下優於傳統設計。

關鍵字—增強型氮化鎵電晶體、閘極電阻、雙脈衝實驗、寄生電感參數

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Abstract

In recent years, high switching frequency power converters are widely used in consumers' electronic applications. High switching frequency converters feature high power-density and fast transient response. With this trend, wide bandgap components such as GaN devices have risen, they are more suitable for high frequency applications comparing to traditional silicon devices. However, there are issues of GaN devices gate driving need to be solved. One main issue is the fragility of gate. The induced voltage by parasitic components on the PCBs will damage the devices in high frequency applications. The gate resistance acts as the role to suppress the parasitic effects, but the design of the gate resistance is not optimized. This thesis proposes the optimization of the gate resistance. By modelling the GaN devices by their physical structure, double pulse test experiment is taken for analyzing the switching transition. The mathematical model is done in this thesis to find out the reasonable region for the gate resistance design. The parasitic extraction by software tool is also taken for the accurate analysis. With the verification by circuit simulation tools and hardware implementation, the switching loss and resistance design region can be obtained and the performance is verified to be better by proposed method.

Keywords—E-mode GaN, Gate Resistance, Double Pulse Test, Parasitic Inductance

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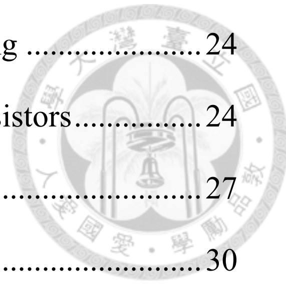

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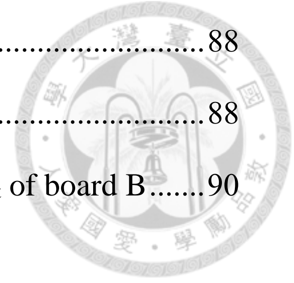

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Chapter 1 Introduction

1.1 Research Background

As the time and technology evolves, the trend of electronic devices has become thinner, lighter and smaller. The passive components in the circuit, such as capacitors and inductors, which occupy the superior part of the device volume, have a lot to do with their reduction of size. In the recent research area of power electronics, high efficiency and power density has been the target which researchers pursue for years [1], and the born of Gallium Nitride (GaN) transistor is the solution to the above-mentioned issues.

Due to the poor behavior of traditional silicon devices in high frequency applications, GaN transistor, which has the feature of low turn-on resistance, low internal capacitor and small device area, is considered to be the device of the new generation. GaN transistor allows the power converters to operate at high frequency region with its better performance, reduce the volume of power converters and further reach the goal of the converters' high efficiency and power density.

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1.2 Thesis Motivation

GaN devices has been more and more widely used in recent years. We can find GaN devices in many applications, such as the motor drive, fast-charging power bank, and envelope tracking ICs. The GaN devices feature their ability to be utilized in high frequency applications. However, there are still some issues need to be conquered of the GaN transistors [2], and one main issue is the breakdown of gate. The transistor will be disrupted when the induced voltage on the parasitic components makes the voltage on gate exceed its maximum value. We are introducing this issue more completely in section 2.4. On the other hand, the gate resistance serves as the role to suppress the excess driving voltage at the gate. When we design the gate resistance moderately, the issue of breakdown can be solved.

Traditionally, we may treat the driving loop of transistors as a simple RLC circuit [3]. Thus, the resistance can be easily design by the second order equations. However, the output loop will impact the switching transition dramatically since the equivalent circuit is not as simple as an RLC circuit. Thus, the precise model is required to do for the analysis of the gate resistance. We are doing this part more detailly in section 3.4.

When we use the traditional RLC model to model the switching behavior of GaN devices, the existing equation only marks the breakaway resistance that makes the circuit critical damped. When the circuit is critical damped, the oscillation terms of the

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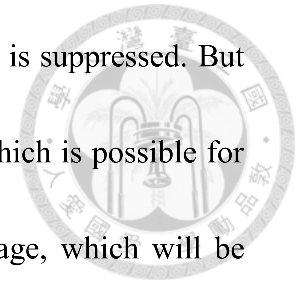

gate voltage is eliminated, and the impact of parasitic components is suppressed. But the design of gate resistance is not that simple, there is a region which is possible for the resistor design that satisfies the requirement of the gate voltage, which will be described detailly in section 4.3.

In the former research, some solutions to avoid the breakdown of gate have been proposed. RC snubber approach has been proposed in [4]. The RC snubber in paralleled with gate loop can make the excess energy dissipated by the snubber, but the price is that the parallel capacitor requires lots of gate charge, which will make the driving loss much bigger.

Dynamic gate resistance mechanism of the driver has been proposed in [5]. The idea is that when GaN transistor go through the miller plateau, the equivalent gate resistance is then increased to slow down the driving speed to minimize the parasitic effects. However, currently there is no complete analysis of the gate resistance design, which the gate resistance may possibly be over-designed.

Thus, the main idea of the thesis is the optimization of the gate resistance design, the complete analysis will be proposed in this thesis.

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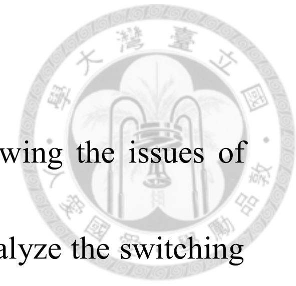
1.3 Thesis Outline



First of all, we are introducing the characteristics and reviewing the issues of switching transition of GaN transistors in chapter 2. In order to analyze the switching transition, the model building is necessary. We are doing the transistor and double pulse test circuit modelling, which is the testing environment of the transistor in chapter 3, and the analysis will also be done in the same chapter. The chapter 4 focuses on the implementation of the double pulse test circuit. We use ANSYS Q3D to extract the parasitic parameters on PCBs to model the real behavior of the experiment. Based on the real circuit parameters, the model verification will also be taken in the same chapter. The measurement result will be introduced in chapter 5. At last, chapter 6 concludes this thesis.

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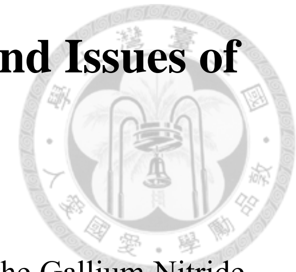

Chapter 2 Review of GaN Transistors and Issues of Switching Transition

In this chapter, we are going to give the brief introduction to the Gallium Nitride transistors, including the classification of different types of Gallium Nitride transistors, the experiment environment, and the issues of the switching behavior. First of all, the brief review of Gallium Nitride transistor is introduced in section 2.1. To analyze the behavior of switching device, we apply the double pulse test experiment, which is introduced in section 2.2. The cause of the non-ideal switching behavior in high frequency applications is parasitic effect, which will be briefly introduced in section 2.3. Section 2.4 introduces the challenge of Gallium Nitride transistor of its switching transition. The loss mechanism of Gallium Nitride transistor is introduced in section 2.5, and the section 2.6 gives the brief summary of this chapter.

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2.1 Brief Review of Gallium Nitride Transistors

There are two major types of Gallium Nitride (GaN) transistor currently used, normally-on and normally-off GaN transistors [6]. Normally-on GaN transistors, also known as the depletion-mode (D-mode) GaN transistors, are not widely commercially used due to the characteristic of the negative threshold voltage, which means they are under operation normally and are not compatible to most applications. Fig. 2.1 shows the I-V curve of the normally-on GaN Transistors. Thus, the following part will focus on the normally-off GaN transistors.

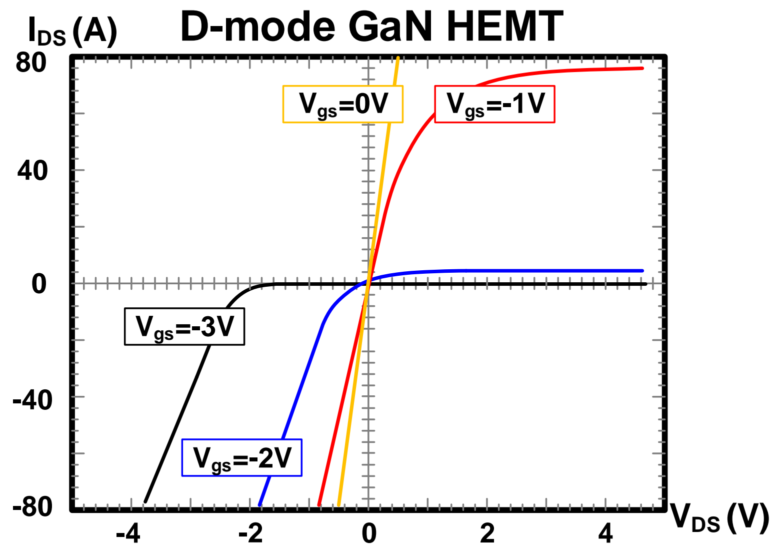

Fig. 2.1 The I-V curve of depletion mode GaN transistors [7]

There are two kinds of normally-off GaN transistors on the market, they are enhanced mode (E-mode) GaN and cascode mode GaN. Table 2.1 briefly compares the difference among two types of GaN devices and the silicon ones. Normally-off GaN devices, compared to normally-on ones, are normally cut-off and only triggered when

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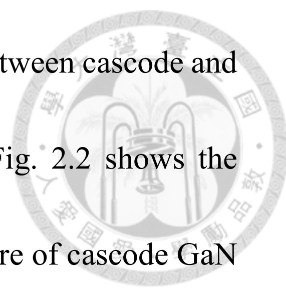

they are driven, which fit most of the applications. The difference between cascode and E-mode devices are mainly based on their electrical structures. Fig. 2.2 shows the electrical structure of the cascode GaN devices. The internal structure of cascode GaN devices are a traditional silicon MOSFET cascode with a D-mode GaN transistor, which is the reason why they are so-called cascode GaN. The low-voltage silicon MOSFET is used here to avoid introducing extra on-state resistance. The advantages of cascode GaN contain both of the silicon transistors' and GaN transistors', which the loss of the cascode GaN is smaller than silicon ones and they are more robust than the E-mode GaN devices due to the E-mode ones are more sensitive to the high frequency effects [6][8].

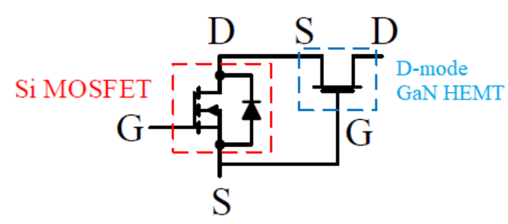

Fig. 2.2 The electrical structure of cascode mode GaN transistors [6]

	Cascode mode	**Enhanced mode**	**Silicon FET**
Type		Normally-off	
Vth	Low	Lower	High
Rds,on	Low	Lower	High
Switching Speed	Fast	Faster	Slow
Vgs_max	High	Low	High
Driving	Easy	Hard	Easy
Gate Breakdown	Little Chance	High Chance	No
Vsd	Low	High	Very Low
Qrr	Low	0	High

Table 2.1 Brief comparison of different type of GaN transistors and Silicon ones

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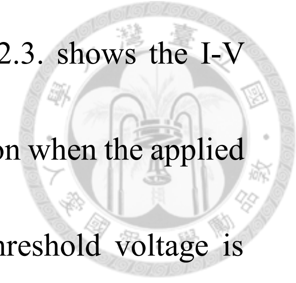

The E-mode GaN transistors are normally-off devices. Fig. 2.3. shows the I-V curve of E-mode GaN transistors. E-mode GaN transistors are turn on when the applied voltage on gate is larger than their threshold voltage, and the threshold voltage is positive which result in the normally-off behavior of E-mode GaN transistors.

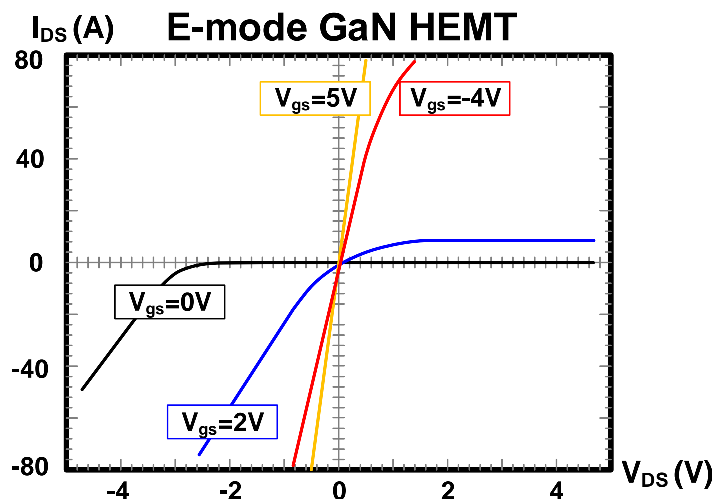

Fig. 2.3 The I-V curve of enhanced mode GaN transistors [7]

Fig 2.4 shows the physics structure of E-mode GaN devices. A thin layer of Aluminum Nitride (AlN) is grown on the silicon substrate to provide a seed layer for the subsequent growth of a GaN heterostructure. A heterostructure of aluminum gallium nitride (AlGaN) and then GaN is grown on the AlN. This layer provides a foundation on which to build the E-mode GaN transistors. A very thin AlGaN layer is then grown on top of the highly resistive GaN. It is this thin layer that creates a strained interface between the GaN and AlGaN crystals layers. This interface, combined with the intrinsic piezoelectric nature of GaN, creates a two-dimensional electronic gas (2DEG) which is

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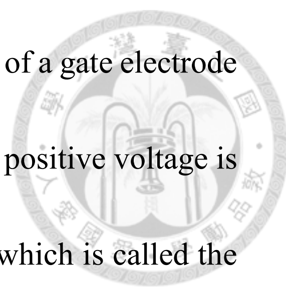
filled with highly mobile and abundant electrons. Further processing of a gate electrode forms a depletion region under the gate. To enhance the transistor, a positive voltage is applied to the gate in the same manner as turning on an n-channel, which is called the enhancement mode power HEMT [7].



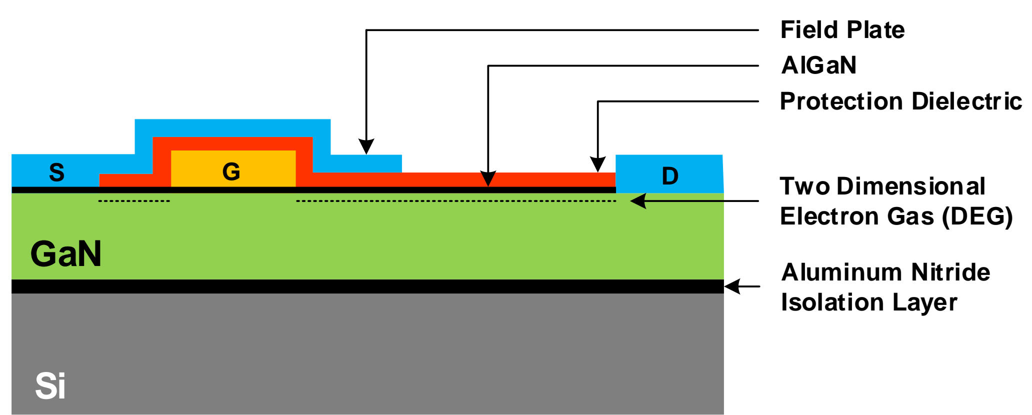


Fig. 2.4 The physics structure of E-mode GaN transistors [7]

For the devices on the market, there are some well-known manufacturers. GaNSystem and EPC are two major manufacturers of E-mode GaN devices, and Transphorm is the well-known manufacturer of cascode GaN devices. However, the applications of their products are quite different based on the specification of their GaN devices. Table 2.1 shows the comparison of the GaN devices of three manufacturers.

	EPC	GaN Systems	Transphorm
GaN-type	E-mode	E-mode	Cascode
Vds,max	15V~350V	100V,650V	650V,900V
Vgs,max	6V, -4V	7V, -10V	±18V
Rds,on	Very small	Very small	Small
Transistor Volume	Small	Small	Large
Package Inductance	Small	Small	Large

Table 2.2 Brief comparison of three manufacturers of GaN transistors [9] [10] [11]

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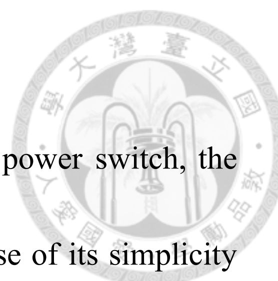
2.2 Introduction of Double Pulse Test



For the study and investigation of the switching behavior of power switch, the double pulse test (DPT) is chosen as the object of the study because of its simplicity and convenience [12]. Double pulse test circuit contains fewer components compared to the whole design of a power converter, and there is no needs of the consideration of control and thermal problems. Also, the double pulse test circuit let the switch operate at the desired voltage, current level and frequency. To sum up, double pulse test is a great solution to understanding the switching behavior of the switching devices.

Fig. 2.5 shows the circuit configuration of the double pulse test. The device under test (DUT) can be any switching device. The two states of the double pulse test circuit are shown in Fig. 2.6. When DUT is turn-on, the voltage V_{bus} is charging the output inductor, the current flows through the DUT and is increasing, the current flow is shown in left of Fig. 2.6. When DUT is turn-off, the current of inductor must be continued, flowing through the free-wheeling diode, which is shown in right of Fig 2.6.

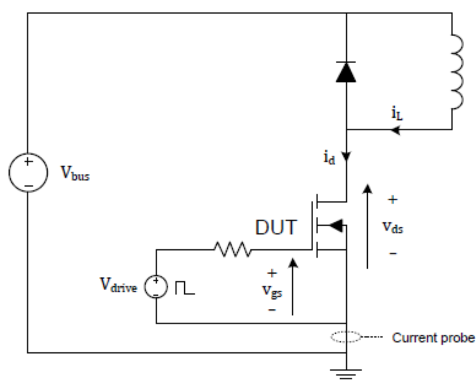


Fig. 2.5 Double pulse test circuit configuration

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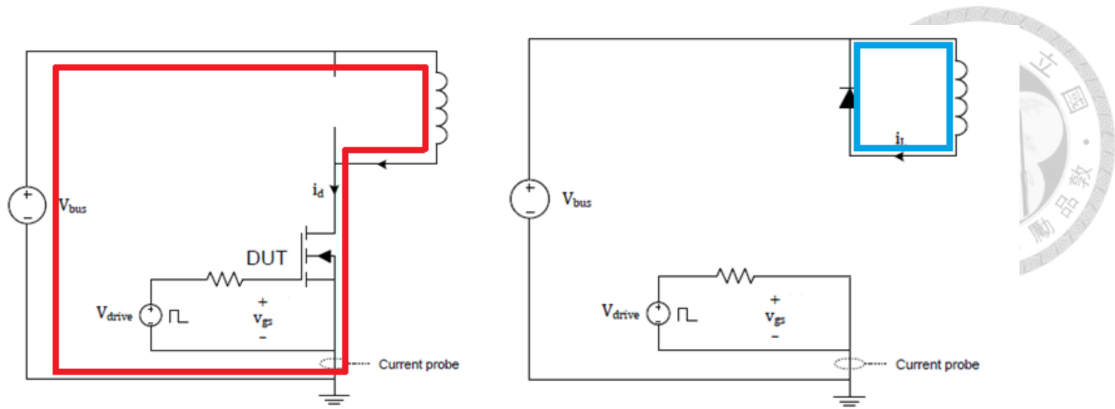

Fig. 2.6 Two states of the double pulse test circuit

The waveform of DPT is shown in Fig. 2.7. The operation is introduced below:

(1) T_0~T_1: DUT is first turn-on, the current is charging by the inductor to the desired current value.

(2) T_1~T_2: When current reaches desired value, DUT is first turn-off. At T_1, the turn-off transition waveforms at desired current level can be observed.

(3) T_2~T_3: After the short period of turn-off, DUT is then turn-on again at T_2, the turn-on transition waveforms can be observed at T_2, the current level is considered to be the same as T_1.

(4) T_1~T_3 can be considered as a 50% duty wave featuring the switching frequency. After T_3, the inductor current is slowly dissipated by the output diode.

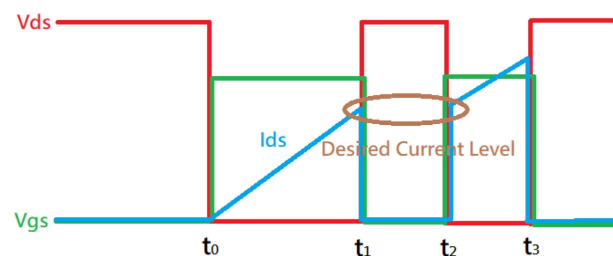

Fig. 2.7 Voltage and current waveforms of double pulse test

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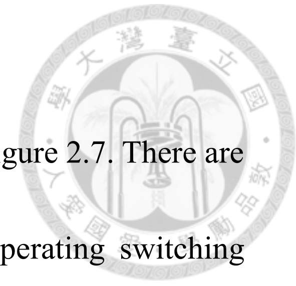
2.3 Parasitic Effects



The switching behavior of the transistors is not as ideal as the figure 2.7. There are some parasitic effects occur inevitably when power switch is operating switching transition, which are severe to the whole circuit behavior [8]. Parasitic components in the device and printed circuit board (PCB) are the cause of these non-ideal effect. They will be briefly introduced in this section.

Parasitic components are mainly classified as three types. They are parasitic resistance, capacitance and inductance. Parasitic resistance induced extra loss due to current flowing through. The parasitic resistance exists everywhere, e.g. DCR of the passive components, copper loss on PCB, equivalent resistance inside the power transistors. Parasitic capacitance exists mainly in power switches. Due to the structure of transistors, the capacitor-like behavior occurs between metals inside the transistor. The gate-source voltage (V_{gs}), the drain-source voltage (V_{ds}) represent the voltage across the parasitic capacitance of the transistors. Thus, the switching transition isn't the ideal square wave, it behaves like the RC charging circuit. On the other hand, due to equation (2.1), the voltage variation on the parasitic capacitance induces the extra current, which will influence the circuit behavior.

$$I_{C_{par}} = C_{par}\frac{dV_{C_{par}}}{dt} \tag{2.1}$$

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Parasitic inductance is another cause of the non-ideal effect in the circuit, however, it affects more significantly in high frequency applications and causes severe damage to the circuit. The parasitic inductor exists mainly in the current loop of PCB, the length of the current path is positive correlated to the value of the parasitic inductance. Due to equation (2.2), the current variation on the current path induces the voltage on parasitic inductance, which is the potential problem of the reliability of the circuit.

$$V_{L_{par}} = L_{par} \frac{dI_{L_{par}}}{dt} \tag{2.2}$$

The parasitic effects in the switching transition are impossible to avoid totally, there are some solutions to the problem derived from the parasitic effects. For the internal capacitance of the power switches, drivers have been invented to provide a large current charging the parasitic capacitance to make the switching transition faster, avoiding the extra time during switching transition. In order to reduce the effect of parasitic inductance, the current path on PCB is considered to be narrowed to minimize the parasitic inductance between the components. Some damping circuits are considered to be added. The resistor acts as a role to limit the switching speed of the circuit, reducing the dv/dt and di/dt event in the circuit. The RC snubber dissipates the excessed voltage in the circuit to make the parasitic effects smaller. However, the damping components cost more loss and volume, which is the choice of the designers

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2.4 Challenges of Switching Transition of GaN Transistors

As we introduced in section 2.1. Enhanced mode GaN transistor has the feature of lowest maximum gate-source voltage, also the smallest threshold voltage among different types of transistors. To make good use of E-mode GaN devices, the problems has to be taken into consideration seriously, especially in high frequency applications. The problems derived from the characteristics are briefly introduced in this section.

2.4.1 Breakdown of Gate

Take the E-mode GaN devices EPC2014C manufactured by EPC as example, the maximum ratings of electrical parameters of EPC2014C is shown in Fig. 2.8. The output characteristic is shown in Fig. 2.9.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	48	
I_D	Continuous (T_A = 25°C, $R_{\theta JA}$ = 43°C/W)	10	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	60	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Fig. 2.8 Maximum ratings of EPC2014C [13]

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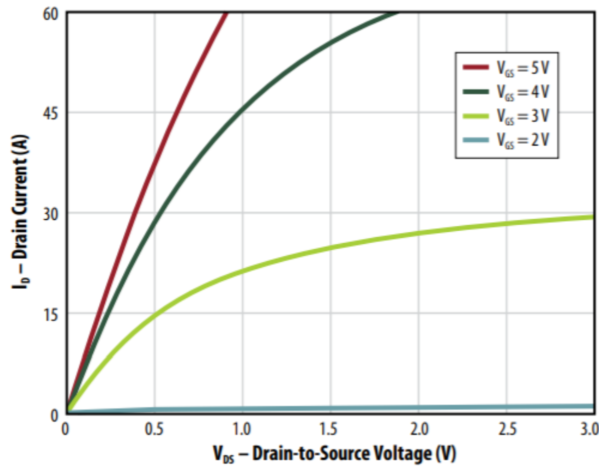

Fig 2.9 Output characteristic of EPC2014C [13]

For the best performance indicated by Fig. 2.9, the gate-source voltage is considered to be as close as 5V. Fig. 2.8 shows that the maximum gate-source voltage of EPC2014C is 6V, which means the margin between the maximum voltage and the required voltage is only 1V. The parasitic effects introduced in section 2.3 shows that the inductance between the components on PCB may possibly induce the extra voltage when the current flows through during the switching transition. The induced voltage will possibly make the gate-source voltage exceeds its maximum value, the breakdown of gate may occur and finally damage the transistors. Fig 2.10 illustrate the condition when breakdown of gate occurs during turn-on transition. The red curve is the ideal turn-on switching waveform of gate-source voltage of GaN transistor, however, parasitic components cause the oscillation of the voltage, which the orange curve indicates, may possibly make the gate-source voltage exceed the maximum value, damaging the GaN transistors.

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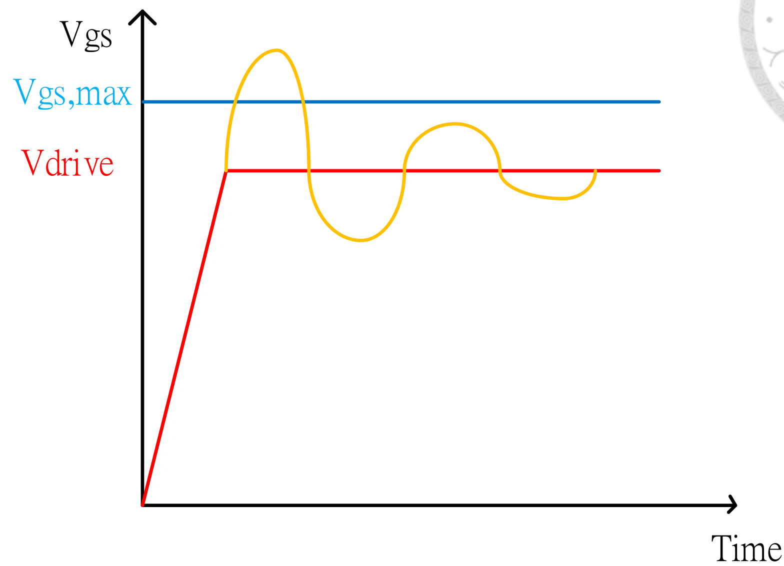

Fig 2.10 Voltage waveforms when breakdown of gate occurs

2.4.2 False-Triggering

Another issue cause by parasitic components is false-triggering [4]. The threshold voltage of E-mode GaN is much smaller than traditional silicon devices and other types of GaN. Referring to Fig. 2.11, the threshold voltage of EPC2014C is typically 1.4V, and the minimum is only 0.8V. False-triggering may happen due to the extreme low threshold voltage when gate-source voltage is oscillating during turn-off transition of GaN transistors. Fig. 2.12 shows the condition when false-triggering occurs. The orange curve indicates the oscillation caused by parasitic components, when the voltage rings above the threshold voltage, false triggering happens.

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Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 125 μA	40			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 32 V		50	100	μA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.4	2	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		50	100	μA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 2 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 10 A		12	16	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.8		V

Fig. 2.11 Static characteristics of EPC2014C [13]

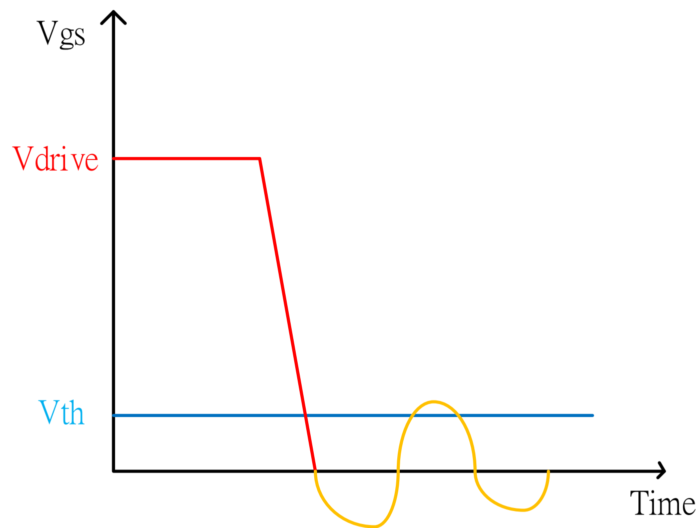

Fig 2.12 Voltage waveforms when false-triggering occurs

When above-mentioned events happen, the price is the malfunction of the whole circuit since the switching devices are usually the key component of the circuit. The importance of the suppression of parasitic effects is obviously shown. There is additional loss cause by parasitic components, however, the importance is not as large as breakdown of gate and false-triggering. The loss mechanism of GaN transistor will be introduced in next section.

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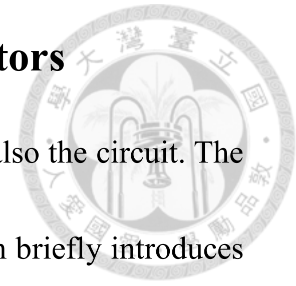
2.5 **Loss Mechanism of E-mode GaN Transistors**



Loss is the crucial index of the performance of the transistors, also the circuit. The loss estimation is an important lesson of the designers. This section briefly introduces the loss mechanism of E-mode GaN transistor. The loss can be classified into four types. They are switching loss, conduction loss, driving loss and parasitic loss [14].

2.5.1 Switching Loss

The switching loss of GaN transistor is mainly including V-I overlap loss and capacitor loss. When power transistor is operating its switching transition, the area of overlap between voltage and current waveform indicates the loss of switching transition. The ideal switching condition is zero current through the switch when turning-off and zero voltage across when turning-on, however, the loss is generated due to the non-ideal behavior which can be illustrated in Fig. 2.13, the blue-colored area shows the V-I overlap loss of turn-on transition.

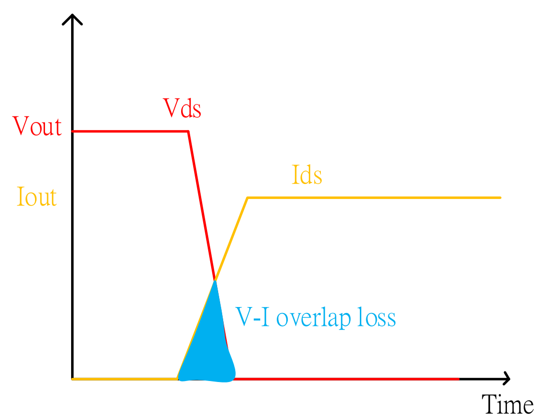


Fig. 2.13 V-I overlap loss of turn-on transition

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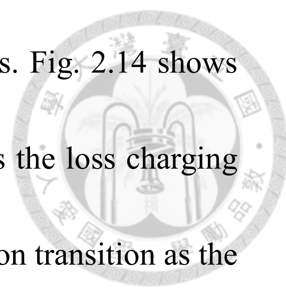

Another part of the switching loss is the parasitic capacitor loss. Fig. 2.14 shows the loss mechanism of capacitor loss. Capacitor loss E_{oss} represents the loss charging the parasitic capacitor of the switch. This energy is lost during turn-on transition as the capacitance is discharged through the channel of the switch. The equation for E_{oss} is described by equation (2.3).

$$E_{oss} = \int_{0}^{V_{out}} V_{ds}\, C_{oss}\, dV_{ds} \tag{2.3}$$

Capacitor loss E_{qoss} occurs when there is an opposite switch in the half-bridge configuration. The capacitor discharging current of the opposite switch induces the loss which is described by equation (2.4).

$$E_{qoss} = \int_{0}^{V_{out}} (V_{out} - V_{ds})\, C_{oss}\, dV_{ds} \tag{2.4}$$

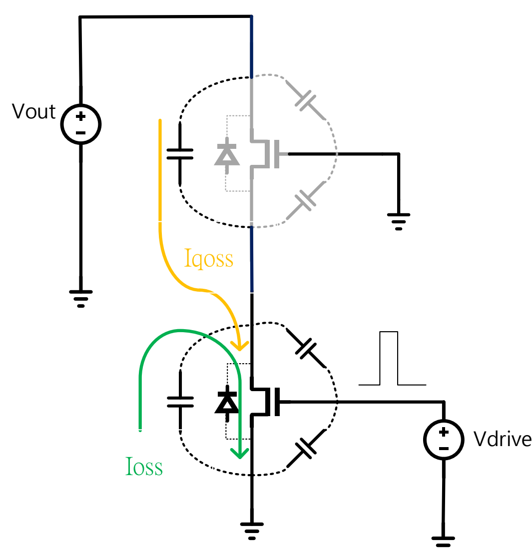

Fig. 2.14 Mechanism of capacitor loss in E-mode GaN transistors

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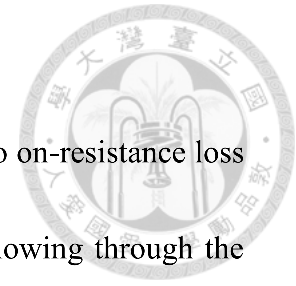

2.5.2 Conduction Loss

The conduction loss of GaN transistor are mainly classified into on-resistance loss and dead-time loss. When power transistor is operating, current flowing through the channel cause the on-resistance loss. The dead-time loss is related to the reverse conduction mode of E-mode GaN transistors.

As the transistor conducting, current flowing through the equivalent parasitic resistance inside the channel of the transistor induce on-resistance loss, which is familiar with other types of transistors. The main advantage of E-mode GaN transistors referred to on-resistance loss is that the on-resistance is usually much smaller than the others, which cost little on-resistance loss.

One advantage of E-mode GaN transistors is that they are allowed to operate at reverse conduction mode with its body-diode like behavior, and there is no an actual diode inside the physical structure of the transistor which avoid the loss of E_{qrr}. The dead-time loss occurs when the two switches of the half-bridge configuration are both reaching their turn-off state. The current inside the circuit is forced to flow through the reverse path, which is from source to drain of the transistor. In the meanwhile, the voltage across the drain and source will cause the addition dead-time loss which is illustrated in Fig. 2.15. With the current value increasing, the voltage across the source and drain V_{sd} is increasing simultaneously.

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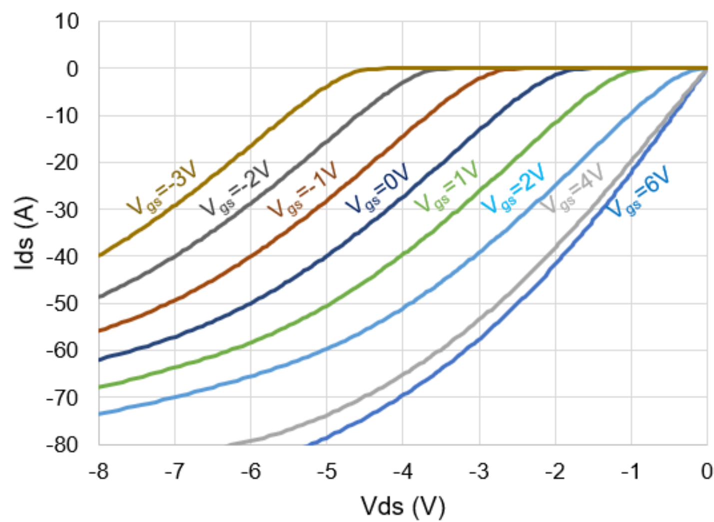

Fig. 2.15 V-I curve of the reverse conduction mode of E-mode GaN [14]

2.5.3 Driver Loss and Parasitic Loss

The mechanism of driver loss of E-mode GaN transistors is similar to other types of transistors. Due to the relatively small gate charge of E-mode GaN transistors, driver loss is smaller than other transistors, the driver loss equation is shown in (2.5).

$$P_{driver} = V_g \times Q_g \times f_{sw} \tag{2.5}$$

Parasitic loss happens everywhere in the circuit. The parasitic effects caused by parasitic components may directly or indirectly increase the loss. Parasitic resistances in the circuit cause resistive loss directly. Parasitic capacitance cause addition charge flows through, and parasitic inductance induce additional voltage across when current flows through, which are hard to estimate. The best way to reduce parasitic loss is minimize the parasitic effect as possible.

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2.6 Summary

This chapter reviews the characteristic of GaN transistors. From looking at the common GaN devices on the market, we find that the E-mode transistor has the best performance but rigorous driving condition, it is interested to find some solution to meet the requirement. When we need to analyze the switching transition, we apply double pulse test. The non-ideal effects of switching transition are caused by parasitic components, the challenge of E-mode transistors is mainly the breakdown of gate in turn-on transition and false-triggering in turn-off transition. And finally, the loss mechanism of E-mode GaN transistor is introduced. Since introduced in chapter 1, to furtherly optimize the gate resistor design, the modelling and analysis of switching transition in the point of view of voltage spike will be introduced in chapter 3 detailly.

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Chapter 3 Turn-on Transition Modelling and Analysis of E-mode GaN Transistors with Double Pulse Test

As introduced in chapter 1, the goal of this thesis is to optimize the design of gate resistor in turn-on transition to avoid the voltage spike causing the breakdown of gate. The traditional second-order RLC model cannot meet the requirement of the resistor design since the output circuit also impact the transistors' switching behavior. In order to optimize the design of gate resistor of the driving circuit, mathematical analysis is introduced in this chapter.

Section 3.1 gives the equivalent circuit modelling and the brief verification of the E-mode GaN transistors. Section 3.2 briefly introduce the turn-on transition of the E-mode GaN transistors based on the model in section 3.1. The equivalent circuit model of the double pulse test when turn-on transition is applied is derived in section 3.3 and the s-domain analysis of the circuit model is then done in section 3.4. Finally, section 3.5 summarizes this chapter.

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3.1 E-mode GaN Transistor Equivalent Circuit Modelling

In this section, the equivalent circuit model of E-mode GaN devices based on their physical structure is introduced [7] [15]. Basically, the GaN transistors behave similarly to the traditional silicon ones with a little difference. This thesis focuses on the EPC2014C manufactured by EPC, and the following parts are all mainly about the specifications of EPC2014C.

3.1.1 Physical-Structure-Based Modelling of GaN Transistors

Fig. 3.1 shows the physical structure of E-mode GaN manufactured by EPC, and Fig. 3.2 illustrates the equivalent circuit model of E-mode GaN transistors based on the physical structures.

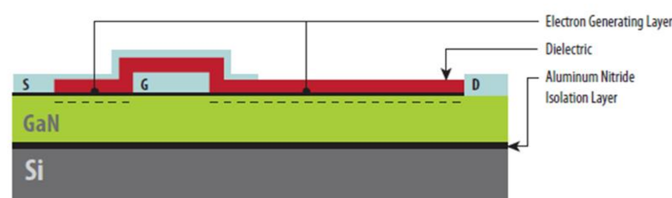

Fig. 3.1 Physical structure of E-mode GaN manufactured by EPC [7]

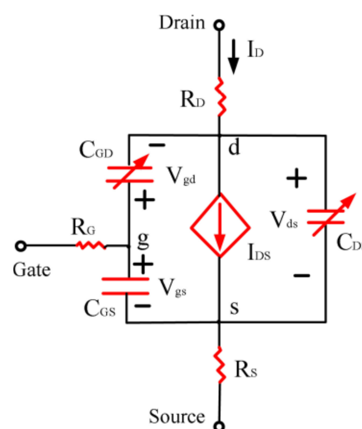

Fig. 3.2 Equivalent circuit model of EPC E-mode GaN [15]

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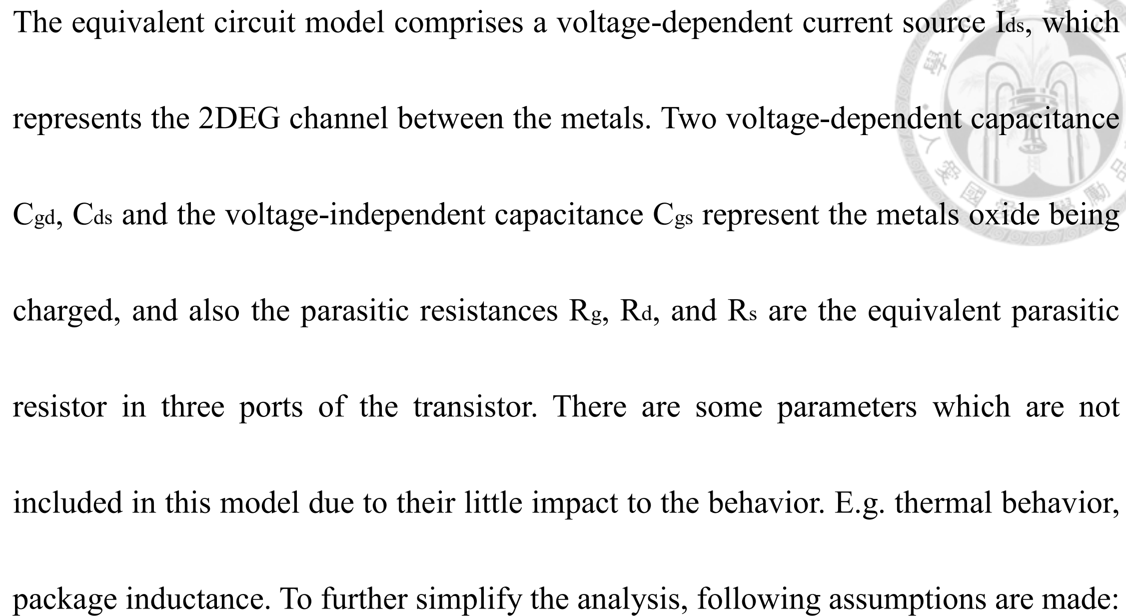

The equivalent circuit model comprises a voltage-dependent current source I_{ds}, which represents the 2DEG channel between the metals. Two voltage-dependent capacitance C_{gd}, C_{ds} and the voltage-independent capacitance C_{gs} represent the metals oxide being charged, and also the parasitic resistances R_g, R_d, and R_s are the equivalent parasitic resistor in three ports of the transistor. There are some parameters which are not included in this model due to their little impact to the behavior. E.g. thermal behavior, package inductance. To further simplify the analysis, following assumptions are made:

(1) The R_d and R_s are small enough compared to the on-resistance $R_{ds,on}$, so they are ignored during turn-on transition.

(2) The capacitance variation when voltage across capacitor changes is ignored because the variation is small enough when transistor is operating after Miller Plateau, which will be introduced in next section.

(3) Channel current model can be replaced by an equivalent on-resistance $R_{ds,on}$ due to the little variation when transistor is operating after Miller Plateau.

Fig 3.3 shows the equivalent circuit model of EPC E-mode GaN after reduction, and the verification is then shown in next paragraph.

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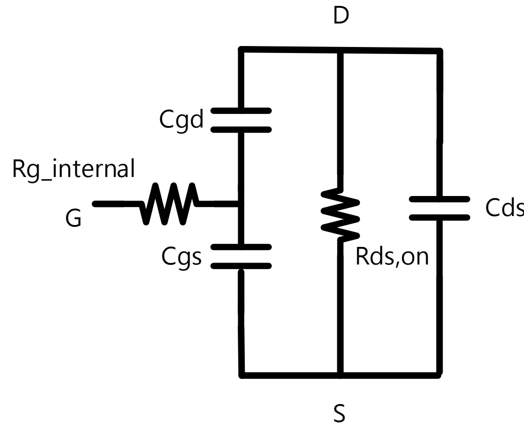

Fig. 3.3 Equivalent circuit model of EPC E-mode GaN after reduction

For the verification of the model, the SPICE model from EPC is applied. Fig 3.4 shows the SPICE model of EPC2014C. This SPICE model is made by manufacturers and is built based on Fig. 3.2. The goal of us is to verify the simplified model whether if it matches the SPICE model or not.

```
.subckt EPC2014C_test_1 gatein drainin sourcein
.param aWg=385 A1=13.125 k2=2.2767 k3=0.15 rpara=0.0074278 rpara_s_factor=0.15
+ a1Tc=0.003721 arTc=-0.0061 k2Tc=0.0006 x0_0=1.7025 x0_1=4.8632e-07 x0_0_TC=0 x0_1_TC=0
+ dgs1=4.3e-07 dgs2=2.6e-13 dgs3=0.8 dgs4=0.23
+ ags1=2.1427e-10 ags2=1.2058e-10 ags3=1.9336 ags4=0.20501
+ ags5=-1.5581e-13 ags6=-1.913 ags7=1.848
+ agd1=3.6643e-13 agd2=5.8313e-11 agd3=-0.95656 agd4=2.4275
+ agd5=1.0611e-11 agd6=-4.5909 agd7=21.025
+ agd8=3.1327e-12 agd9=-91.363 agd10=33.365
+ asd1=7.1887e-11 asd2=1.4655e-10 asd3=-4.8515 asd4=5.7344
+ asd5=1.3471e-10 asd6=-0.83699 asd7=53.776 rg_value=0.4

rd drainin drain {((1-rpara_s_factor)*rpara*(1-arTc*(Temp-25)))}
rs sourcein source {(rpara_s_factor*rpara*(1-arTc*(Temp-25)))}
rg gatein gate {(rg_value)}

gswitch drain source Value {if(v(drain,source)>0,
+       (A1*(1-a1Tc*(Temp-25))*log(1.0+exp((v(gate,source)-(k2*(1-k2Tc*(Temp-25))))/k3))*
+       v(drain,source)/(1 + (x0_0*(1-x0_0_TC*(Temp-25))+x0_1*(1-x0_1_TC*(Temp-25))*v(gate,source))*v(drain,source)) ),
+       (-A1*(1-a1Tc*(Temp-25))*log(1.0+exp((v(gate,drain)-(k2*(1-k2Tc*(Temp-25))))/k3))*
+       v(source,drain)/(1 + (x0_0*(1-x0_0_TC*(Temp-25))+x0_1*(1-x0_1_TC*(Temp-25))*v(gate,drain))*v(source,drain)) ) )}
*Model for voltage dependent gate-source capacitance
E_GS t1_gs b1_gs gate source 1.0
V_INGS 0 b1_gs 0V
C_IGS t1_gs 0 1.0E-6
G_GS gate source VALUE = {1E6*I(V_INGS)*
+ (ags1 + 0.5*ags2/(1.0 + exp( (v(gate,source)-ags3)/ags4 ))*exp( (v(gate,source)-ags3)/ags4 ) +
+ ags5/(1.0 + exp((v(source,drain)-ags6)/ags7))*exp((v(source,drain)-ags6)/ags7))}

*Model for voltage dependent gate-drain capacitance
E_GD t1_gd b1_gd gate drain 1.0
V_INGD 0 b1_gd 0V
C_IGD t1_gd 0 1.0E-6
G_GD gate drain VALUE = {1E6*I(V_INGD)*(agd1 + 0.5*ags2/(1.0 + exp((v(gate,drain)-ags3)/ags4))*exp((v(gate,drain)-ags3)/ags4) +
+ agd2/(1.0 + exp((v(gate,drain)-agd3)/agd4))*exp((v(gate,drain)-agd3)/agd4) +
+ agd5/(1.0 + exp((v(gate,drain)-agd6)/agd7))*exp((v(gate,drain)-agd6)/agd7) +
+ agd8/(1.0 + exp((v(gate,drain)-agd9)/agd10))*exp((v(gate,drain)-agd9)/agd10))}

*Model for voltage dependent source-drain capacitance
E_SD t1_ds b1_ds source drain 1.0
V_INSD 0 b1_ds 0V
C_ISD t1_ds 0 1.0E-6
G_SD source drain VALUE = {1E6*I(V_INSD)*(asd1 + asd2/(1 + exp((v(source,drain)-asd3)/asd4))*exp((v(source,drain)-asd3)/asd4) +
+ asd5/(1 + exp((v(source,drain)-asd6)/asd7))*exp((v(source,drain)-asd6)/asd7))}

.ends
```

Parameters

Resistors

Channel

Capacitors

Fig. 3.4 SPICE model of EPC2014C [13]

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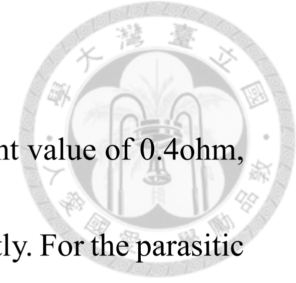
3.1.2 Parasitic Components Estimation



For the parasitic resistors, gate resistance R_g is set to the constant value of 0.4ohm, the drain resistance R_d and the source resistance R_s are ignored directly. For the parasitic capacitors, we first look into the gate-source capacitance C_{gs}. With the variation of V_{ds}, capacitance value must remain constant value as the definition. Fig. 3.5 shows the capacitance value of C_{gs} of the SPICE model using MATLAB when V_{ds} is applied from -30V to 30V. The verification shows that C_{gs} can be set to 214.2pF as a constant value.

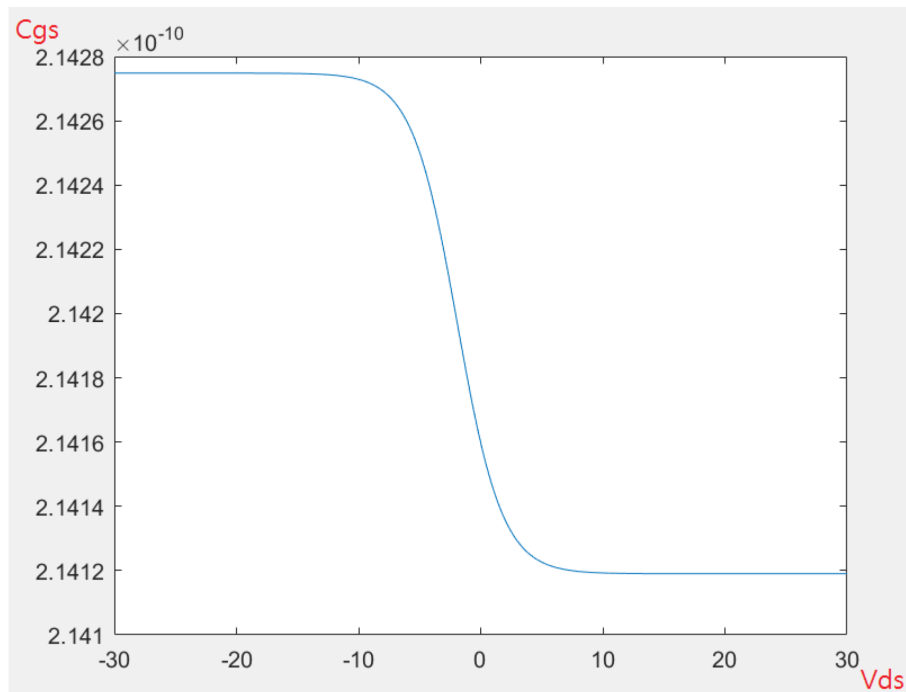


Fig. 3.5 C_{gs} value with the variation of V_{ds} from -30V to 30V

For the drain-source capacitance C_{ds}, the same procedure is done. Fig. 3.6 shows the capacitance value of C_{ds} of the SPICE model using MATLAB when V_{ds} is applied from -30V to 30V.

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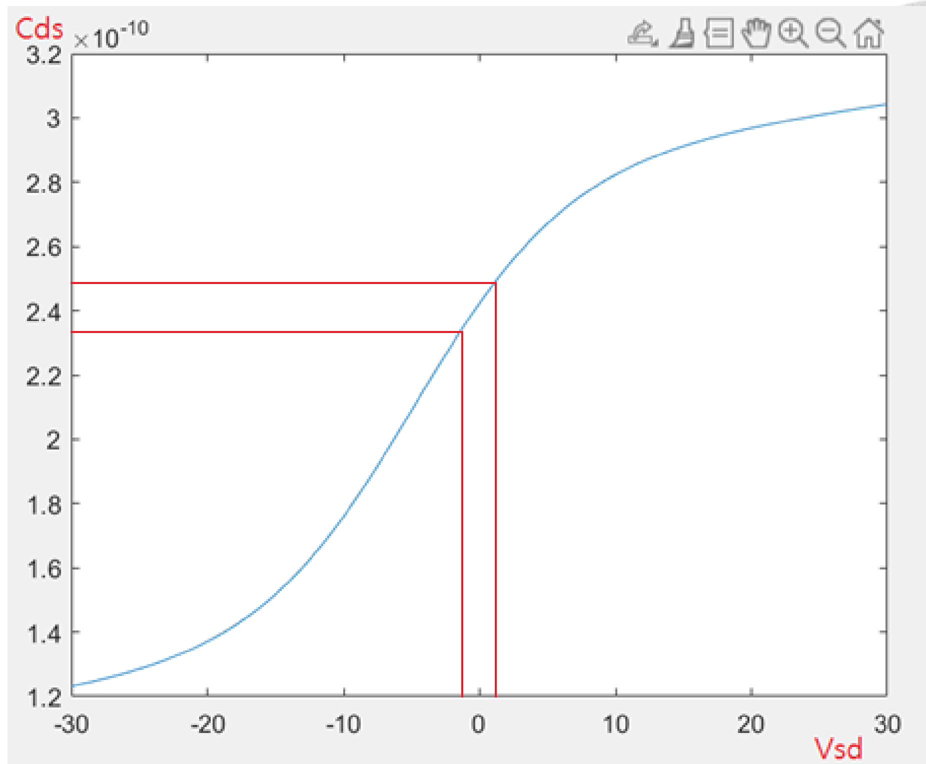

Fig. 3.6 C_{ds} value with the variation of V_{ds} from -30V to 30V

Since the turn-on transition is the main concern of this thesis, the voltage across drain and source when the switch is operating is nearly 0V ideally. Also, since the voltage spike happens when the GaN transistor operates at the region after Miller Plateau, which will be explained in next section, the V_{ds} value will not exceed $\pm$1V in practical. Thus, The C_{ds} value is estimated to be 240pF for turn-on transition within the red-line region show in Fig. 3.6.

For the gate-drain capacitance C_{gd}, also known as the miller capacitor, has some issues with their value compared to the datasheet. Fig. 3.7 shows the capacitance value of C_{gd} of the SPICE model using MATLAB when V_{gd} is applied from -10V to 10V, and Fig. 3.8 shows the estimated capacitance of EPC2014C from the datasheet.

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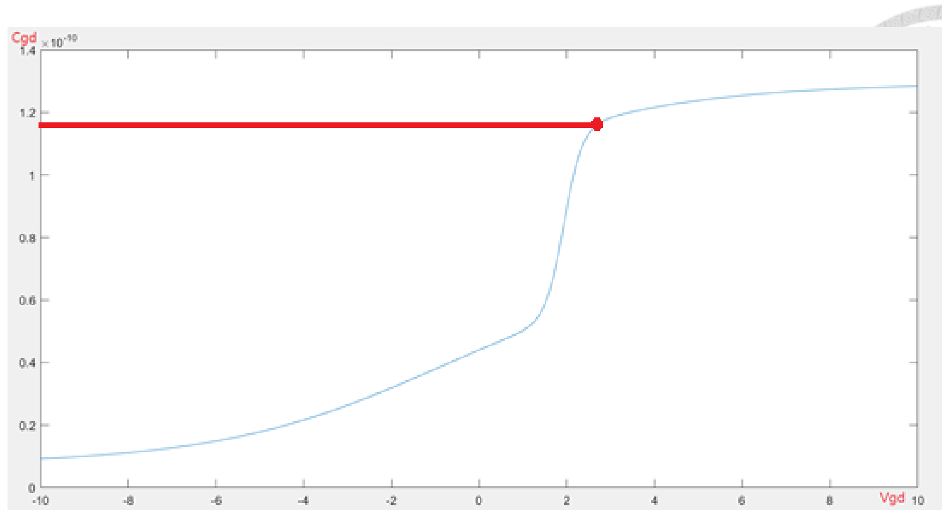

Fig. 3.7 C_{gd} value with the variation of V_{gd} from -10V to 10V

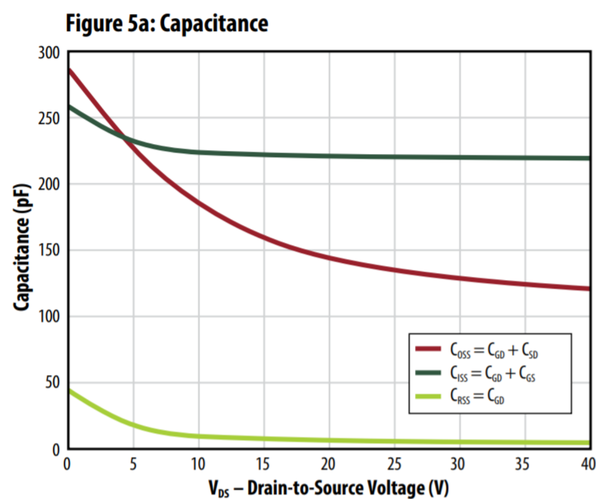

Fig. 3.8. C-V curve from datasheet of EPC2014C [13]

The issue is that the critical cause of the variation of C_{gd} in the SPICE model is the voltage across gate and drain, not the drain and source, which results in the difference between the verification and the datasheet. For the analysis of the turn-on transition, the V_{gd} value is considered to be similar to V_{gs} after Miller Plateau, and the capacitance value of V_{gd} varies little after the possible miller voltage. To simplified the analysis, C_{gd} is considered to be a constant value of 115pF.

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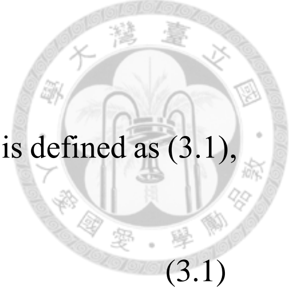
3.1.3 Channel Model Simplification



For the channel modelling, the current equation in SPICE model is defined as (3.1),

$$I_{channel} = \frac{A_1 \log(1 + e^{\frac{V_{gs}-k_2}{k_3}})V_{ds}}{1 + (x_0 + x_1 V_{gs})V_{ds}} \quad (3.1)$$

with the parameters of A_1=13.125, k_2=2.2767, k_3=0.15, x_0=1.7025, x_1=4.8632x10^{-7}.

We first ignore the parameter of x_1 since it is relatively small enough compared to others. The logarithmic term's simplification is shown in Fig. 3.9. When the exponential term is much larger than 1, the logarithmic term can be simplified into linear term. The expected simplification is shown in (3.2).

$$\log\left(1 + e^{\frac{V_{gs}-2.2767}{0.15}}\right) \rightarrow \frac{V_{gs} - 2.2767}{0.15} \quad (3.2)$$

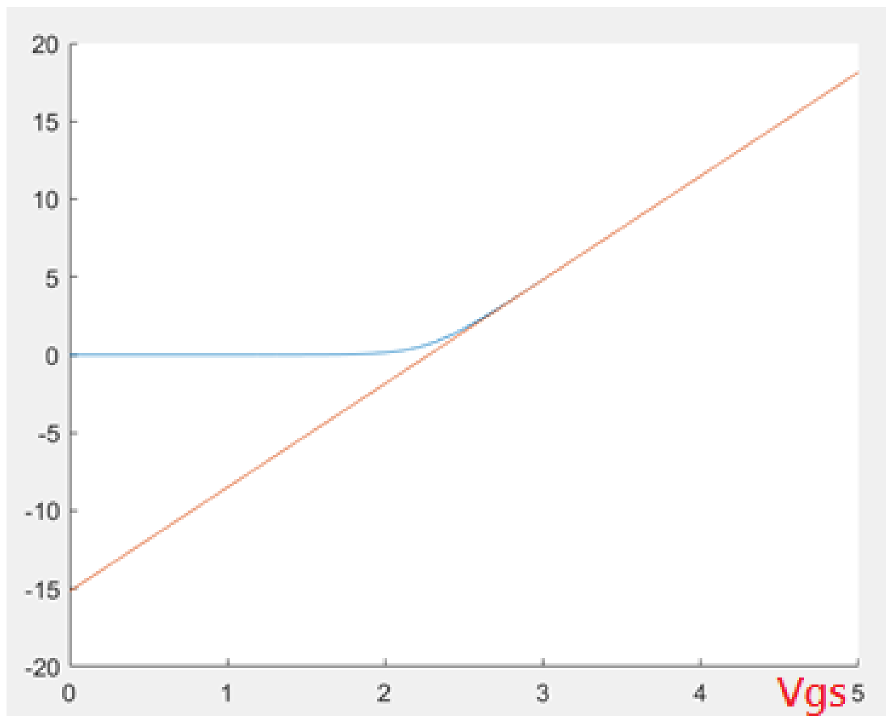


Fig. 3.9 Logarithmic term and the linear term comparison of channel current

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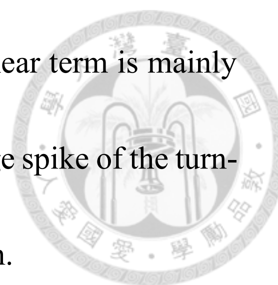

When voltage across gate and source is larger than 2.8V, the linear term is mainly the same as the logarithmic term as Fig. 3.10 shown. Since the voltage spike of the turn-on transition occurs here, it is reasonable to make the such reduction.

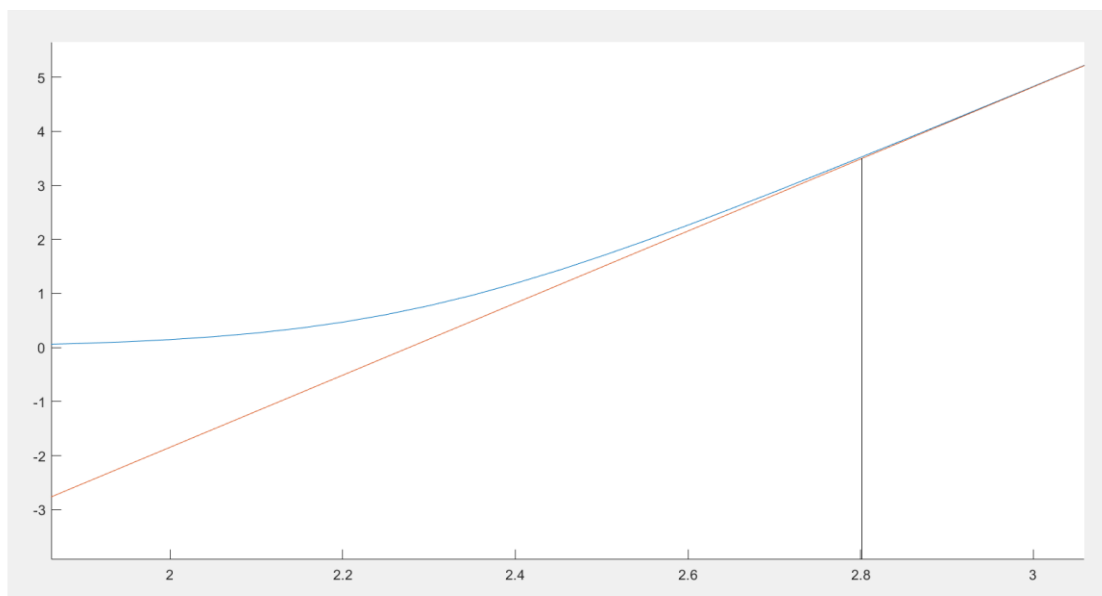

Fig. 3.10 Zoomed in of Fig. 3.9 when V_{gs} is applied from 2V to 3V

Following equations from (3.3) to (3.5) shows the equivalent turn-on resistance, and Fig. 3.11 plot the equivalent turn-on resistance varies with V_{gs} when channel current is 1A, 5A and 10A.

$$I_{channel} = \frac{87.5 \times (V_{gs} - 2.2767)V_{ds}}{1 + 1.7025V_{ds}} \tag{3.3}$$

$$V_{ds} = I_{channel} \times R_{ds,on} \tag{3.4}$$

$$R_{ds,on} = \frac{1 + 1.7025 \times I_{channel}}{87.5(V_{gs} - 2.2767)} \tag{3.5}$$

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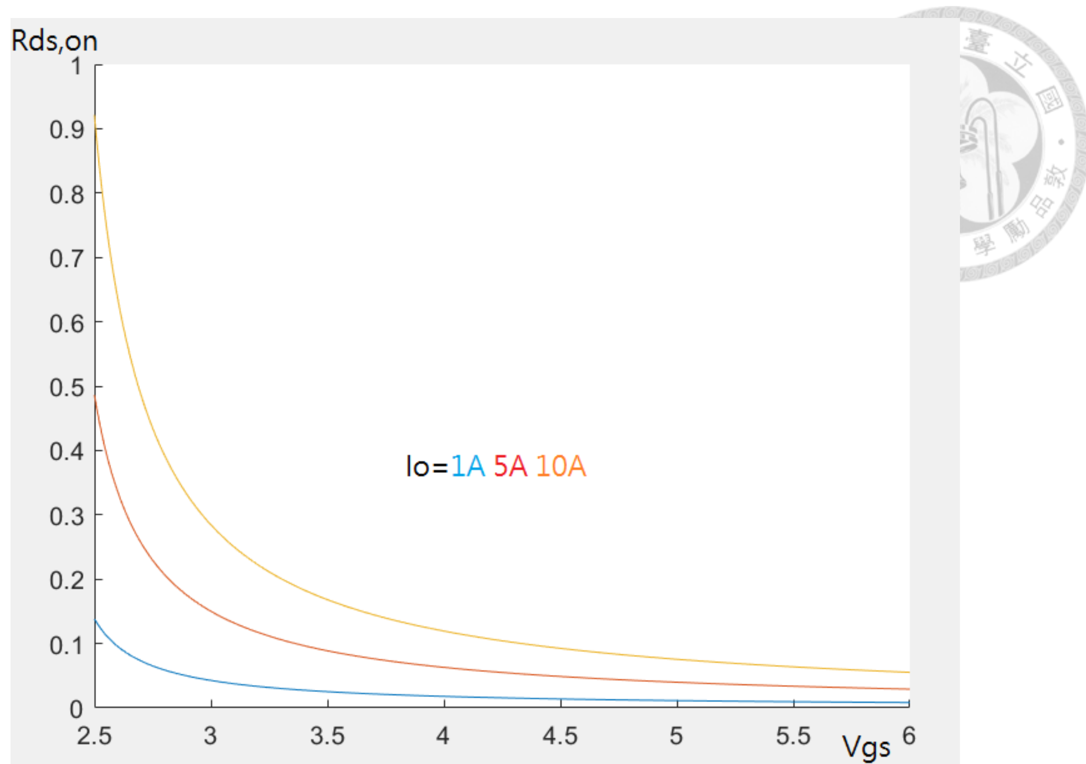

Fig. 3.11 Equivalent on-resistance curve when different channel current is applied

The on-resistance value varies when channel current differs. For the testing condition of the 1A output current, the on-resistance of EPC2014C is estimated to be 0.02ohm for the simplification. The estimated on-resistance will be different but remain nearly constant when applied voltage on gate and source being close to 6V.

3.1.4 Simulation Verification of EPC GaN Transistors Model

Table 3.1 shows the result of the simplified model based on SPICE model when 5V and 1A is applied to the channel of the transistor comparing with the datasheet typical value. The simulation of the simplified model using SIMPLIS is shown in next paragraph.

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	Datasheet (Typical)	Simplified Model
C_{gs}	213.5pF	214.2pF
C_{ds}	143.5pF	240pF
C_{gd}	6.5pF	115pF
$R_{ds,on}$	0.012ohm	0.02ohm
R_g	0.4ohm	0.4ohm

Table 3.1 Comparison between datasheet of EPC2014C and simplified model

Fig. 3.12 shows the simulation of the simplified model and the SPICE model under double pulse test (V_{ds}=5V, I_{out}=1A, other components remain the same). The red, green, blue curves are the waveform of the simplified model of turn-on transition, and the yellow, bright blue and purple curves are the SPICE model ones. The result indicates that the simplified model behaves highly similar to the original one.

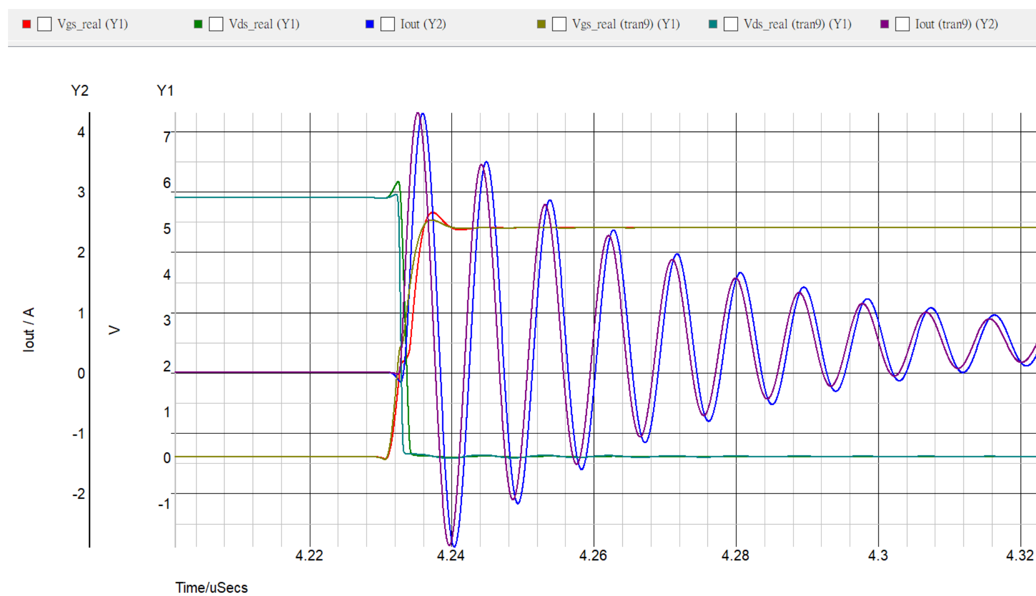

Fig. 3.12 Simulation of simplified GaN model and SPICE model

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3.2 Turn-on Transition of E-mode GaN Transistors

Switching transition of E-mode GaN transistor will be introduced in this section. Similar to MOSFETs, the turn-on phase is separated into five periods. The following paragraph explain the turn-on transition of E-mode GaN transistor step by step, and skips the turn-off transition since it goes through the dual procedure. To analyze the voltage spike of the turn-on transition, some critical positions of the turn-on transition are also introduced in this section.

Fig. 3.13 shows the waveforms of the turn-on transition. There are three main waveforms concerned here. They are gate-source voltage (V_{gs}), drain-source voltage (V_{ds}) and channel current (I_{ds}).

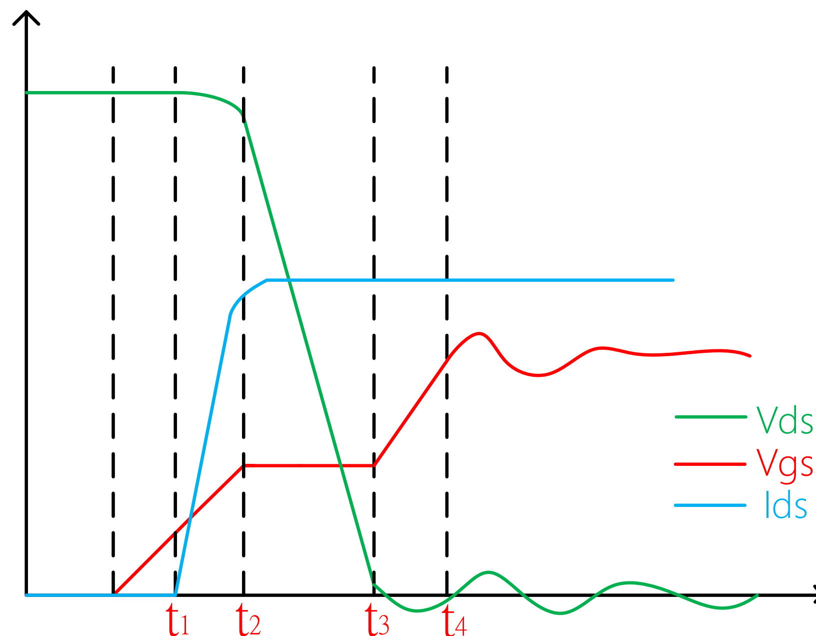

Fig. 3.13 Waveforms of turn-on transition of E-mode GaN transistor

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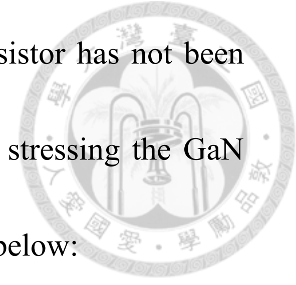

At initial, V_{gs} and I_{ds} are considered to be zero since the transistor has not been triggered. V_{ds} is considered to be the same as the output voltage stressing the GaN transistor. The five periods of the turn-on transition are introduced below:

(1) At t_0, the gate of the transistor starts to be charged, however, the channel is not opened since the voltage across gate and source has not reach the threshold voltage (V_{th}). Until V_{gs} is charged to V_{th}, period 1 ends.

(2) At t_1, V_{gs} reaches V_{th}, and the channel opens here. Current starts to flow through the channel of the transistor, the drain-source voltage here is discharged here but not obviously. V_{gs} keeps rising till the channel is fully opened, which means the channel current meets the output current, and the period 2 ends here.

(3) The so-called Miller Plateau represents the period between t_2 to t_3. During this period, the Vgs remains unchanged, which the voltage here is named after Miller voltage (V_{mp}). When channel is fully opened, the voltage across drain and source has the demand to be discharged from output voltage to zero. The relative impedance on gate-drain capacitance is much smaller than the gate-source one here, so the current is considered to go through C_{gd} totally. Thus, V_{gs} remains constant until V_{ds} is nearly discharged to zero, and V_{gd} is charged from V_{mp}-V_{out} to V_{mp}.

(4) After Miller Plateau, the voltage across C_{gd} and C_{gs} are mainly the same due to the zero voltage on C_{ds}. During t_3 to t_4, C_{gd} and C_{gs} are charged simultaneously from

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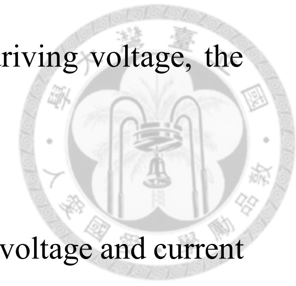

miller voltage to the driving voltage. When voltage reaches driving voltage, the driver stops and the period 4 ends.

(5) Due to the parasitic components in the circuit, the ringing of the voltage and current occurs. This is the reason of the breakdown of gate introduced in section 2.4. When the driver stops at t_4, the energy is still transferred between the parasitic inductors and capacitors to cause the event. The damping resistor is then crucial here acting as the dissipating component to release the excess energy.

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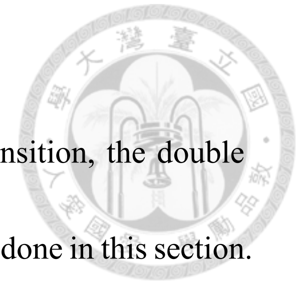
3.3 Double Pulse Test Circuit Modelling



To go further to the voltage spike analysis of the turn-on transition, the double pulse test circuit modelling and reduction of the turn-on transition is done in this section. As introduced in section 3.2, the oscillation between parasitic components is the main reason of the breakdown of gate. The behavior after Miller Plateau of the GaN transistor is the main concern. The mathematical analysis will be introduced in section 3.4 based on the model we derived in this section. Fig. 3.14 shows the double pulse test circuit when parasitic parameters are not considered, and the Fig. 3.15 shows the circuit with parasitic parameters.

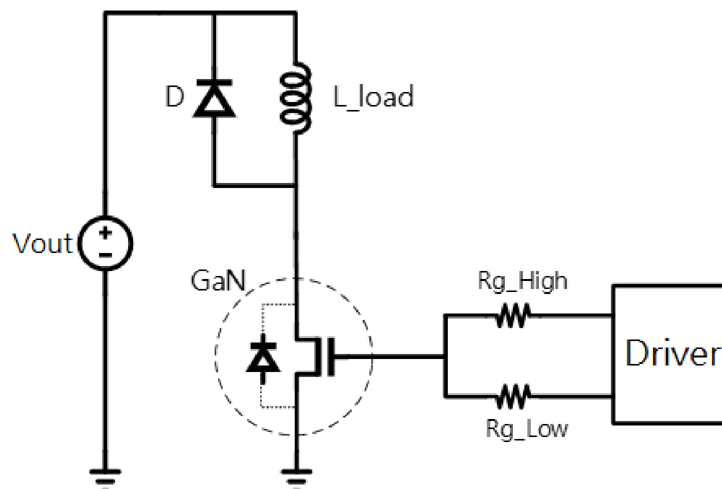


Fig. 3.14 Double pulse test circuit model without parasitic parameters

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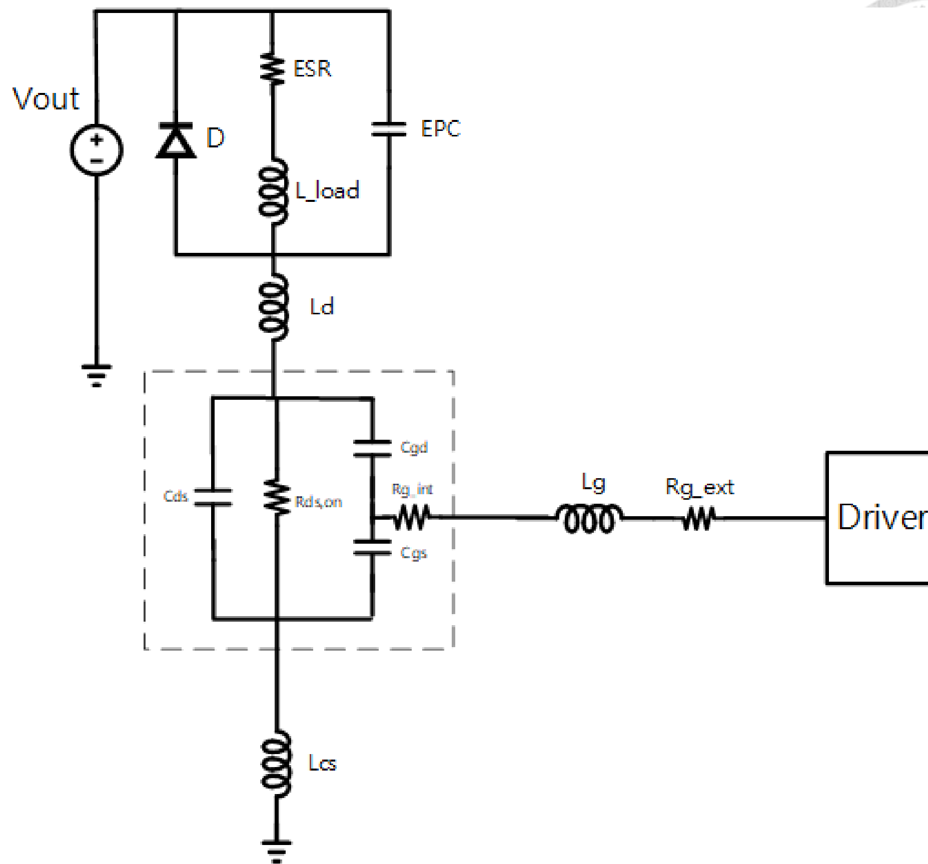

Fig. 3.15 Double pulse test circuit model with parasitic parameters

For the output circuit, ESR denotes the equivalent series resistor of the inductor, and the EPC denotes the equivalent parallel capacitance of the output diode and inductor. There are some parasitic inductors in the circuit. L_d denotes the drain inductance, representing the equivalent inductance between the drain pin of the GaN and the output inductor and diode. L_g denotes the equivalent inductance in the gate loop, and the L_{cs} denotes the common source inductance, which means the equivalent inductance between the overlapping path of the gate loop and the power loop.

We need to do some reduction of the double pulse test model, since the driver and the output circuit are not linear. Fig. 3.16. shows the driver reduction of the double pulse

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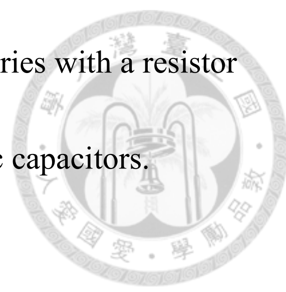

test circuit. The driver is considered to be an ideal voltage source series with a resistor since the driver serves as the source of current charging the parasitic capacitors.

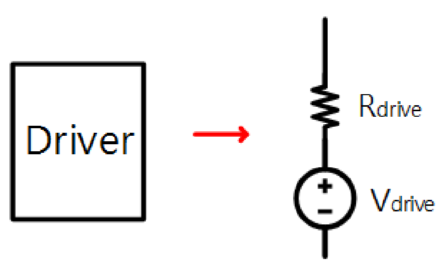

Fig. 3.16 Driver model reduction

During Turn-on transition, the output current is considered to be the constant since we assume that the switching transition is fleeting compared to the whole period. Fig. 3.17 shows the reduction of the output circuit.

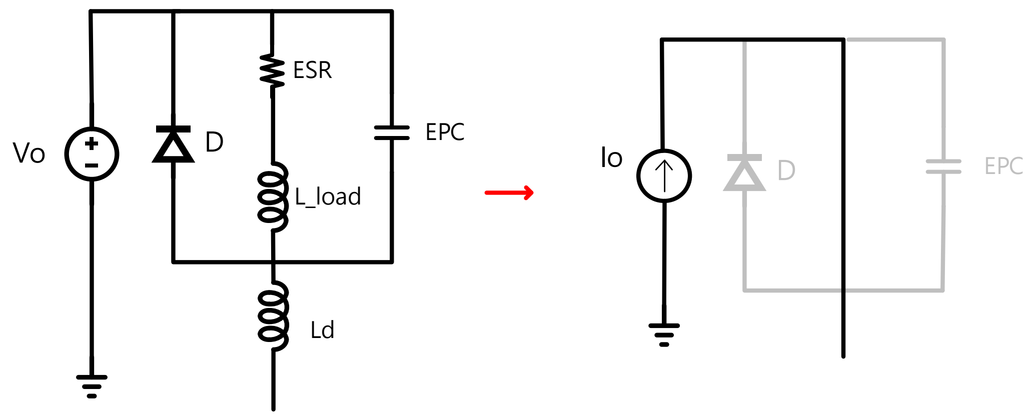

Fig. 3.17 Output circuit reduction

Since the output inductor is large enough, the voltage source and inductor can be treated as a constant current source. Also, the EPC is treated as an open circuit because EPC is small enough which makes the huge impedance. The diode is not working at turn-on transition after miller plateau, so we can simply ignore it. At last, we merge all

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the resistor into one at the gate loop for simple analysis. Fig. 3.18 shows the final model of the double pulse test circuit during turn-on transition after reduction.

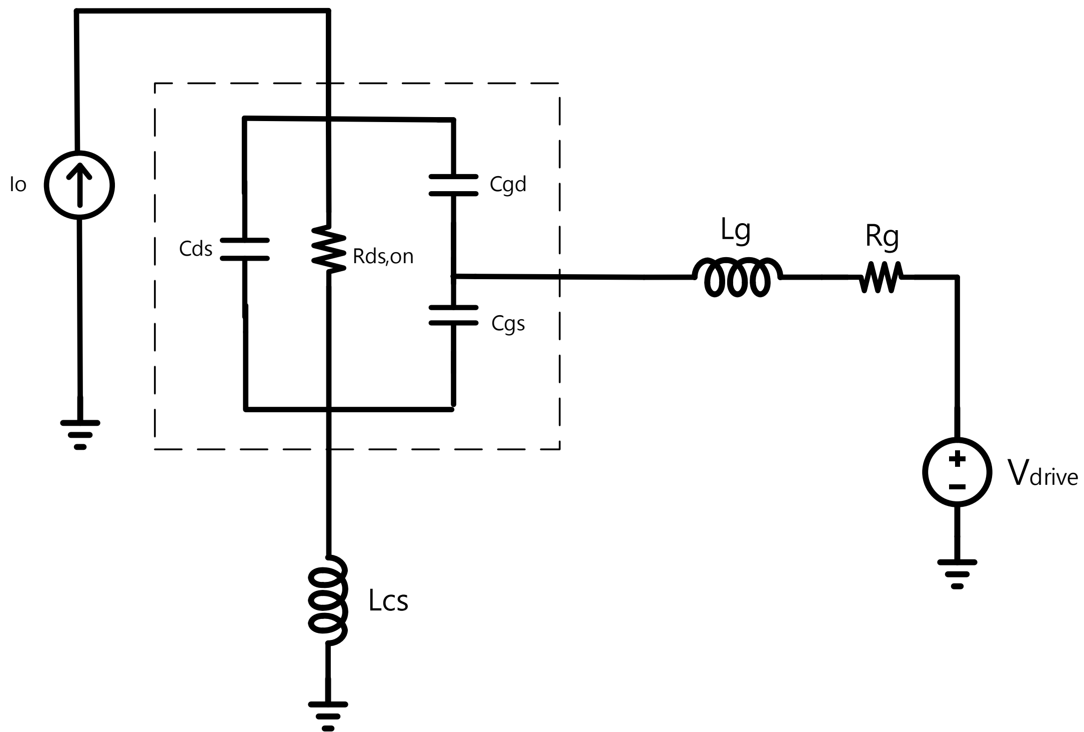

Fig. 3.18 Circuit model of double pulse test after reduction

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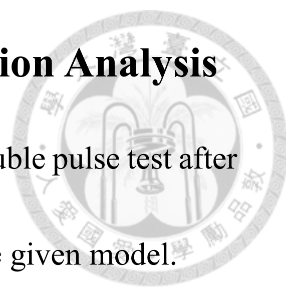

3.4 E-mode GaN Transistors Turn-on Transition Analysis

As introduced in section 3.3, the turn-on transition model of double pulse test after assumption is shown. In this section, we focus on the analysis of the given model. First of all, we need to derive the gate-source voltage equation of turn-on transition since we emphasize the voltage spike and the resonant part when gate-source voltage reaches driving voltage.

3.4.1 Second-order Model Approach

Fig. 3.19 shows the tradition of second-order model. If we are not considering the influence of output, the second-order RLC model gives the gate resistor criteria that is shown in equation (3.6) [3], which means the voltage is damped ($\zeta \geqq 1$) when gate resistor satisfies.

$$R_g \geq \sqrt{\frac{4(L_g + L_{cs})}{C_{gs}}} \qquad (3.6)$$

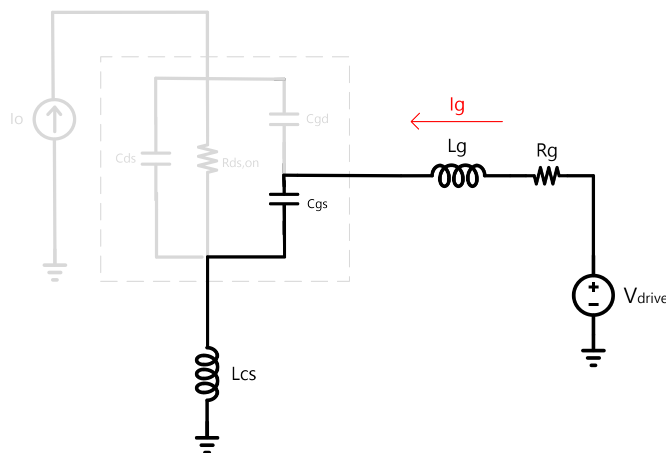

Fig. 3.19 RLC model of turn-on transition of E-mode GaN transistor

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Take the sum of gate inductance and common source inductance equaling to 6nH and C_{gs} equaling to 214.2pF as example, the required resistance is 10.58Ω by equation (3.6). Fig. 3.20 shows the result of circuit simulation using SPICE model provided by manufacturer when gate resistors are equaling to 2Ω (blue curve), 5Ω (green curve) and 10.58Ω (red curve). As shown in Fig. 3.20, red curve shows the waveform that is apparently more over-designed than the green curve, and the maximum voltage of blue curve does not reach the maximum value of gate voltage, which is suitable for the design. The traditional second-order design cannot meet the design requirement since it exists the better design. Table 3.2 shows the switching loss under double pulse test when output power is equal to 5W, the switching loss is improved by 4 times when 2Ω is chosen as gate resistance compared to the second order RLC design.

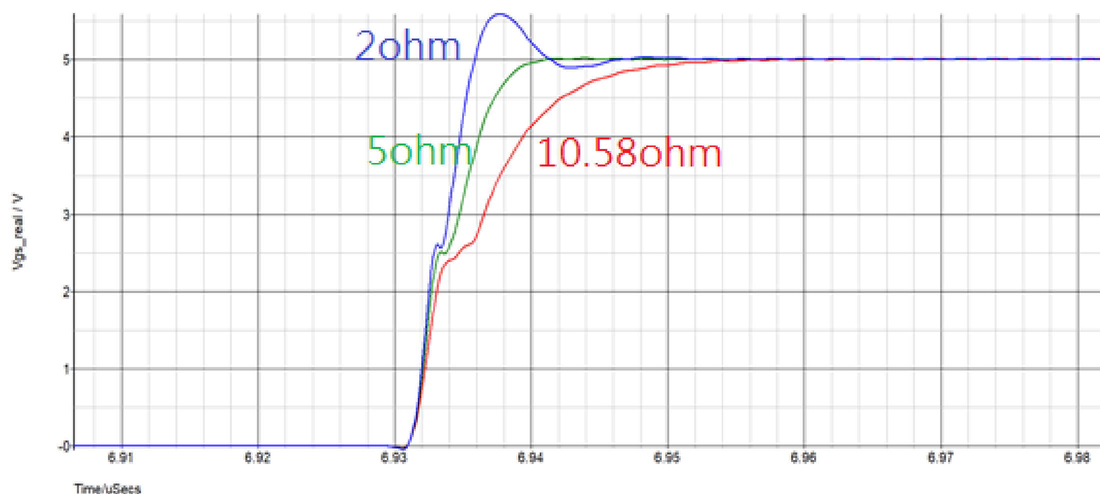

Fig. 3.20 Turn-on transition when resistor designed by second order approach

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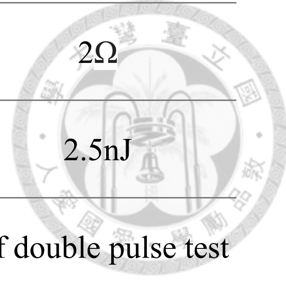

Rg	10.58Ω	5Ω	2Ω
Turn-on Loss	11.3nJ	4.1nJ	2.5nJ

Table 3.2 Switching loss comparison under different gate resistor of double pulse test

3.4.2 S-domain Voltage Equation Derivation

However, the voltage spike and the gate-source ringing are related to the output. Thus, the full model analysis is required to realize the overall behavior. Fig. 3.21 shows the circuit parameters for the analysis. According to the figure, there are three capacitors and two inductors in the circuit, which means we have five time-domain variables of the capacitor voltage and inductor current that require five equations to solve. The value of capacitors, inductors and resistors are treated as constant values for simple analysis, and the constant voltage source V_{drive} and constant current source I_o are applied at the output and driver separately.

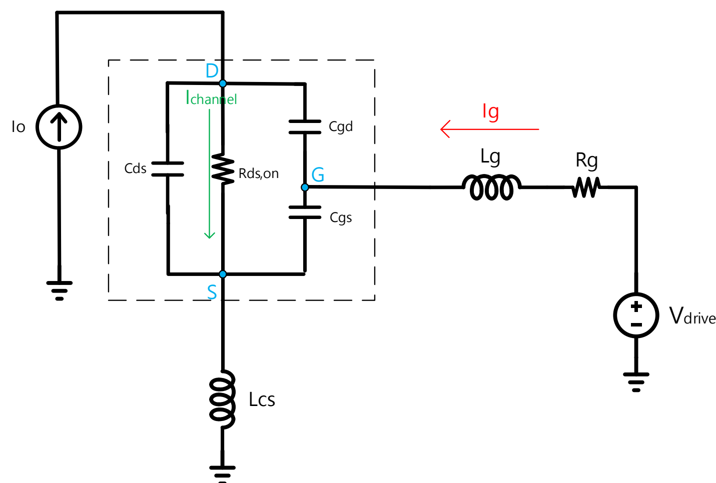

Fig. 3.21 Parameters for the turn-on switching transition analysis

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Following equations from (3.7) to (3.11) are the KVL and KCL equations to solve the voltage across C_{gs}. Equation (3.7) is the capacitor voltage balance of C_{gd}, C_{ds} and C_{gs} and Equation (3.8) shows the gate loop voltage balance. Equation (3.9) is the KCL equation of the gate, equation (3.10) is the KCL equation of the source and equation (3.11) is the drain one.

$$V_{gs}(t) = V_{gd}(t) + V_{ds}(t) \tag{3.7}$$

$$V_{gs}(t) = V_{drive} - R_g I_g(t) - L_g \frac{dI_g(t)}{dt} - L_{cs} \frac{dI_{cs}(t)}{dt} \tag{3.8}$$

$$C_{gd} \frac{dV_{gd}(t)}{dt} + C_{gs} \frac{dV_{gs}(t)}{dt} = I_g(t) \tag{3.9}$$

$$I_g(t) + I_o = I_{cs}(t) \tag{3.10}$$

$$C_{gd} \frac{dV_{gd}(t)}{dt} + I_o = C_{ds} \frac{dV_{ds}(t)}{dt} + \frac{V_{ds}(t)}{R_{ds,on}} \tag{3.11}$$

We eliminate two variables $I_{cs}(t)$ and $V_{ds}(t)$ by substituting equation (3.10) into (3.8) and equation (3.7) into (3.11). The equation (3.12) and (3.13) are the equations we obtain after substitution.

$$V_{gs}(t) = V_{drive} - R_g I_g(t) - (L_g + L_{cs}) \frac{dI_g(t)}{dt} \tag{3.12}$$

$$(C_{gd}+C_{ds}) \frac{dV_{gd}(t)}{dt} + \frac{V_{gd}(t)}{R_{ds,on}} + I_o = C_{ds} \frac{dV_{gs}(t)}{dt} + \frac{V_{gs}(t)}{R_{ds,on}} \tag{3.13}$$

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Since the time-domain differential equations are hard to solve here, we apply Laplace transform here to furtherly solve the equations. The equations (3.14) to (3.16) are the Laplace equations of equation (3.9), (3.12) and (3.13). For the simplification, the equation (3.17), (3.18) and (3.19) are the simplified notation of the capacitance and inductance.

$$C_{gd}(sV_{gd}(s) - V_{gd}(0)) + C_{gs}(sV_{gs}(s) - V_{gs}(0)) = I_g(s) \tag{3.14}$$

$$V_{gs}(s) = \frac{V_{drive}}{s} - R_g I_g(s) - L(sI_g(s) - I_g(0)) \tag{3.15}$$

$$C_{oss}\left(sV_{gd}(s) - V_{gd}(0)\right) + \frac{V_{gd}(s)}{R_{ds,on}} + \frac{I_o}{s} = C_{ds}(sV_{gs}(s) - V_{gs}(0)) + \frac{V_{gs}(s)}{R_{ds,on}} \tag{3.16}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{3.17}$$

$$L = L_g + L_{cs} \tag{3.18}$$

$$C_p = \sqrt{C_{gd}C_{gs} + C_{ds}C_{gd} + C_{ds}C_{gs}} \tag{3.19}$$

The solution of equation (3.14), (3.15) and (3.16) are shown in (3.20), and the parameters are listed below from (3.21) to (3.27).

$$V_{gs}(s) = \frac{b_0 + b_1 s + b_2 s^2 + b_3 s^3}{s + a_2 s^2 + a_3 s^3 + a_4 s^4} \tag{3.20}$$

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$$b_0 = V_{drive} \tag{3.21}$$

$$\begin{aligned} b_1 = {} & L I_g(0) + V_{drive} C_{oss} R_{ds,on} \\ & + R_g \left(I_o R_{ds,on} C_{gd} + C_{gs} V_{gs}(0) + C_{gd} V_{gd}(0) \right) \end{aligned} \tag{3.22}$$

$$\begin{aligned} b_2 = {} & L \left(C_{oss} R_{ds,on} I_g(0) + I_o R_{ds,on} C_{gd} + C_{gs} V_{gs}(0) + C_{gd} V_{gd}(0) \right) \\ & + R_g R_{ds,on} \left(C_{oss} \left(C_{gs} V_{gs}(0) + C_{gd} V_{gd}(0) \right) \right. \\ & \left. + C_{gd} \left(C_{ds} V_{gs}(0) - C_{oss} V_{gd}(0) \right) \right) \end{aligned} \tag{3.23}$$

$$\begin{aligned} b_3 = {} & L R_{ds,on} \left(C_{oss} \left(C_{gs} V_{gs}(0) + C_{gd} V_{gd}(0) \right) \right. \\ & \left. + C_{gd} \left(C_{ds} V_{gs}(0) - C_{oss} V_{gd}(0) \right) \right) \end{aligned} \tag{3.24}$$

$$L = L_g + L_{cs} \tag{3.25}$$

$$C_p = \sqrt{C_{gd} C_{gs} + C_{ds} C_{gd} + C_{ds} C_{gs}} \tag{3.26}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{3.27}$$

We need to separate the DC term of equation (3.20) for the analysis here. The DC term of the $V_{gs}(t)$ is V_{drive}, thus the s-domain term of V_{drive} is $\frac{V_{drive}}{s}$. Equation (3.28) shows the separation, and the parameters are shown from equation (3.29) to (3.34).

$$V_{gs}(s) = \frac{b_0 + b_1 s + b_2 s^2 + b_3 s^3}{s + a_2 s^2 + a_3 s^3 + a_4 s^4} = \frac{V_{drive}}{s} + \frac{N_0 + N_1 s + N_2 s^2}{1 + D_1 s + D_2 s^2 + D_3 s^3} \tag{3.28}$$

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$$N_0 = LI_g(0) + R_g\left(I_oR_{ds,on}C_{gd} + C_{gs}V_{gs}(0) + C_{gd}V_{gd}(0) - C_{iss}V_{drive}\right) \quad (3.29)$$

$$\begin{aligned} N_1 = {} & L\left(C_{oss}R_{ds,on}I_g(0) + I_oR_{ds,on}C_{gd} + C_{gs}V_{gs}(0) + C_{gd}V_{gd}(0) \right. \\ & \left. - C_{iss}V_{drive}\right) \\ & + R_gR_{ds,on}\left(C_{oss}\left(C_{gs}V_{gs}(0) + C_{gd}V_{gd}(0)\right)\right. \\ & \left. + C_{gd}\left(C_{ds}V_{gs}(0) - C_{oss}V_{gd}(0)\right) - V_{drive}{C_p}^2\right) \end{aligned} \quad (3.30)$$

$$\begin{aligned} N_2 = {} & LR_{ds,on}\left(C_{oss}\left(C_{gs}V_{gs}(0) + C_{gd}V_{gd}(0)\right)\right. \\ & \left. + C_{gd}\left(C_{ds}V_{gs}(0) - C_{oss}V_{gd}(0)\right) - V_{drive}{C_p}^2\right) \end{aligned} \quad (3.31)$$

$$D_1 = C_{oss}R_{ds,on} + C_{iss}R_g \quad (3.32)$$

$$D_2 = R_gR_{ds,on}{C_p}^2 + C_{iss}L \quad (3.33)$$

$$D_3 = LR_{ds,on}{C_p}^2 \quad (3.34)$$

When solution of $V_{gs}(s)$ is derived, we focus on the parameters of the denominator. In order to suppress the parasitic effects, the best case is that $V_{gs}(s)$ has no oscillation terms. When the solutions of the characteristic equation (D(s)) are all real numbers, then $V_{gs}(s)$ has no oscillation terms. Since D(s)=0 is a third-order equation, the three solution are either three real solution or a real solution with a pair of the complex conjugate solutions. From the theory of control system, at the breakaway point γ, which is defined as the point which satisfied $D(\gamma) = 0$ and also $\frac{dD(\gamma)}{ds} = 0$, the

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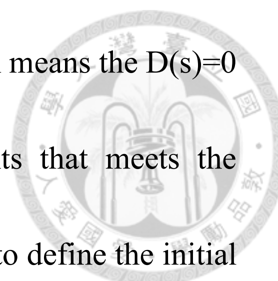
designed R_g and L can make D(s) has no imaginary solutions, which means the D(s)=0 has no oscillation terms. We need to find the breakaway points that meets the requirement [4]. Before finding out the breakaway points, we need to define the initial conditions first.



3.4.3 Initial Conditions

As introduced in section 3.2, the RLC resonant happens when the turn-on transition of GaN transistor goes through the Miller Plateau. The t=0 is defined at the time when Miller Plateau ends. There are three initial conditions we need to find, $V_{gs}(0)$, $V_{gd}(0)$ and $I_g(0)$. Taking the EPC2014C as the example, the output characteristic is shown in Fig. 3.22.

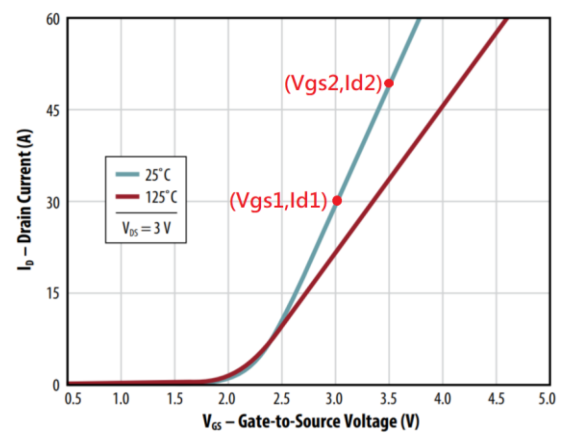


Fig. 3.22 Output characteristic of EPC2014C [13]

Behaving similar to the traditional MOSFET, equation (3.35) shows the channel current when MOSFET is operating at saturation region.

$$I_{ch} = \mu_n C_{ox} \frac{W}{2L} (V_{gs} - V_{th})^2 = K(V_{gs} - V_{th})^2 \tag{3.35}$$

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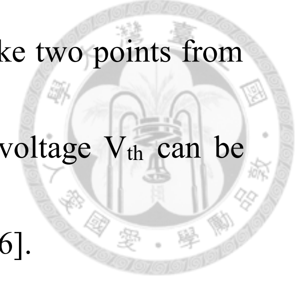

Define K as the constant of the parameters, we can simply take two points from the characteristic curve (V_{gs1}, I_{d1}) and (V_{gs2}, I_{d2}). The threshold voltage V_{th} can be defined as (3.36), and the miller voltage can be defined as (3.37) [16].

$$V_{th} = \frac{V_{gs1}\sqrt{I_{d2}} - V_{gs2}\sqrt{I_{d1}}}{\sqrt{I_{d2}} - \sqrt{I_{d1}}} \tag{3.36}$$

$$V_{gs,mp} = V_{th} + \sqrt{\frac{I_d}{K}} \tag{3.37}$$

For the gate-drain voltage initial condition, we can imply equation (3.38) and (3.39). Since the initial condition happens at the end of Miller Plateau, the voltage across the channel is nearly zero, which can be defined as (3.39).

$$V_{gd}(0) = V_{gs}(0) - V_{ds}(0) \tag{3.38}$$

$$V_{ds}(0) = I_{ch} \times R_{ds,on} \tag{3.39}$$

The last one we need to define is the driving current $I_g(0)$. We have introduced that the current flows through C_{gd} totally at the Miller Plateau. Comparing to the whole switching transition, Miller Plateau happens shortly. Thus, the current at Miller Plateau can be considered to be the constant value. Since the voltage across C_{gd} is charged from V_{mp}-V_{out} to V_{mp} here, the gate current is defined as (3.40)

$$I_g(0) = \frac{C_{gd} \times V_{out}}{t_{plat}} \tag{3.40}$$

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As shown in Fig. 3.23, the equivalent circuit at Miller Plateau is the RC circuit. The differential equation (3.41) needs to be solved to find the time domain equation $V_{gd}(t)$. The solution is displayed in (3.42) and the initial conditions (3.43) and (3.44) are required to be satisfied. Thus, (3.45) shows the solution of t_{plat} and the final solution of I_{plat} can be obtained by equation (3.40) and (3.45), which is shown in (3.46).

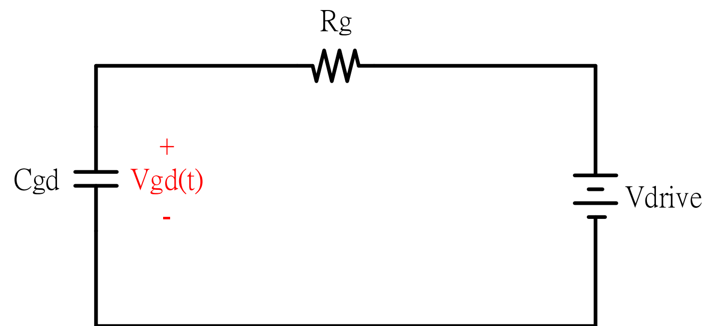

Fig. 3.23 Equivalent circuit model when Miller Plateau occurs

$$V_{drive} = R_g C_{gd} \frac{dV_{gd}(t)}{dt} + V_{gd}(t) \quad (3.41)$$

$$V_{gd}(t) = V_{drive} - R_g C_{gd} e^{-\frac{(t-t_0)}{R_g C_{gd}}} \quad (3.42)$$

$$\text{At } t = 0,\ V_{gd}(t) = V_{plat} - V_{out} \quad (3.43)$$

$$\text{At } t = t_{plat},\ V_{gd}(t) = V_{plat} \quad (3.44)$$

$$t_{plat} = R_g C_{gd} \ln\left(\frac{V_{out}+V_{drive}-V_{plat}}{V_{drive}-V_{plat}}\right) \quad (3.45)$$

$$I_{plat} = \frac{V_{out}}{R_g \ln\left(\frac{V_{out}+V_{drive}-V_{plat}}{V_{drive}-V_{plat}}\right)} \quad (3.46)$$

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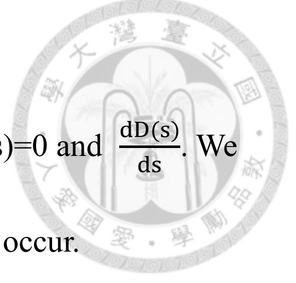
3.4.4 S-domain Analysis of Voltage Equation



Following equations (3.47) and (3.48) are two equations of D(s)=0 and $\frac{dD(s)}{ds}$. We need to determine the region in L-R_g plane where breakaway points occur.

$$1+\left(C_{oss}R_{ds,on}+C_{iss}R_g\right)s+\left(R_gR_{ds,on}{C_p}^2+C_{iss}L\right)s^2 + \left(LR_{ds,on}{C_p}^2\right)s^3=0 \tag{3.47}$$

$$\left(C_{oss}R_{ds,on}+C_{iss}R_g\right)+2\left(R_gR_{ds,on}{C_p}^2+C_{iss}L\right)s + 3\left(LR_{ds,on}{C_p}^2\right)s^2=0 \tag{3.48}$$

The solutions of the L and R_g are shown in equations (3.49) and (3.50). We use MATLAB to plot the breaking point curve on L-R_g plane. We utilize the parameters of EPC2014C (Cgs=214.2pF, Cgd=115pF, Cds=240pF), and the curves of the solution can be obtained. Fig. 3.24 shows the breakaway points on L-R_g plane when AC frequency is sweeping from 10MHz to 10GHz. Blue curve illustrates the full model and the orange one illustrates the second-order model, which is the curve of equation (3.51). The curves show the difference between traditional model and the full model.

$$R_g(s)=\frac{-2C_{iss}-s\left(C_{iss}C_{oss}R_{ds,on}+3R_{ds,on}{C_p}^2\right)-2s^2{C_p}^2{R_{ds,on}}^2C_{oss}}{s\left(C_{iss}+s{C_p}^2R_{ds,on}\right)^2} \tag{3.49}$$

$$L(s)=\frac{C_{iss}+2sR_{ds,on}{C_p}^2+s^2{C_p}^2{R_{ds,on}}^2C_{oss}}{s^2\left(C_{iss}+s{C_p}^2R_{ds,on}\right)^2} \tag{3.50}$$

$$R_g=\sqrt{\frac{4(L_g+L_{cs})}{C_{gs}}} \tag{3.51}$$

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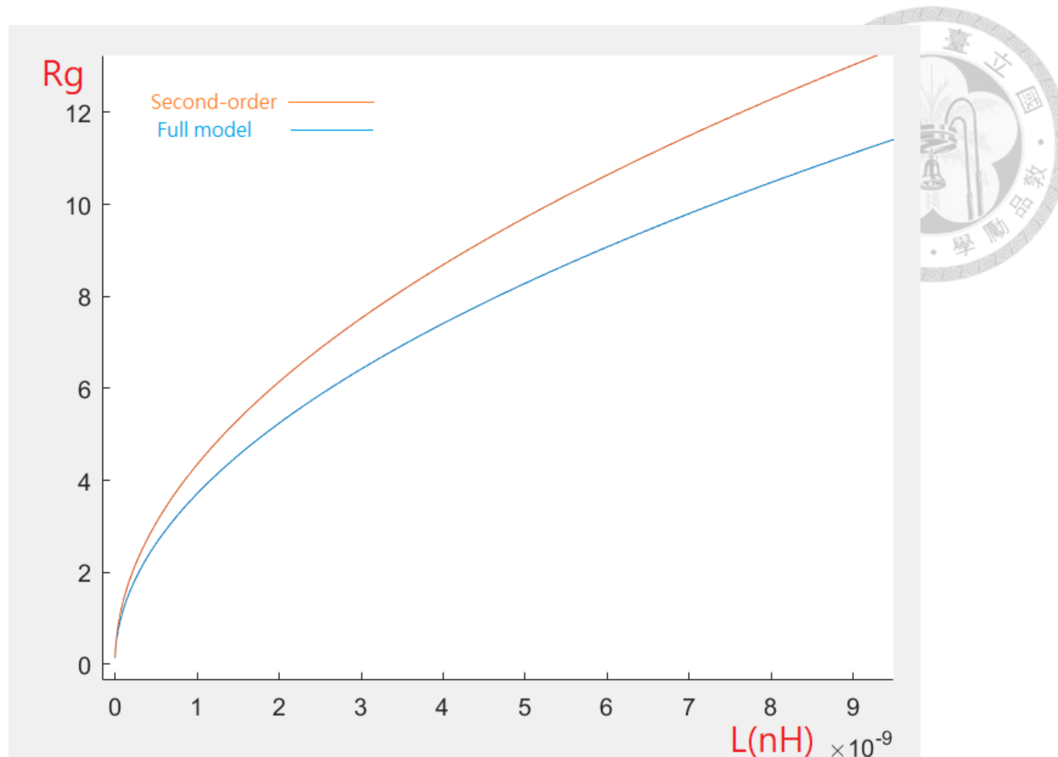

Fig. 3.24 Breakaway points at L-R_g plane using EPC2014C

The curve separates the plane into two parts, the (L,R_g) above the curve is the design where $V_{gs}(t)$ is damped and the (L,R_g) under the curve is the design where the damping ratio is smaller than 1.

Since the $V_{gs}(s)$ is obtained, and the initial conditions are all solved when GaN transistor is operating at the time when Miller Plateau ends, we have sufficient conditions to find out the critical resistance where voltage spike does not exceed the maximum value. Thus, the final thing we need to determine is the parasitic inductance to solve the critical resistance. The example of and model verification will be furtherly introduced in next chapter.

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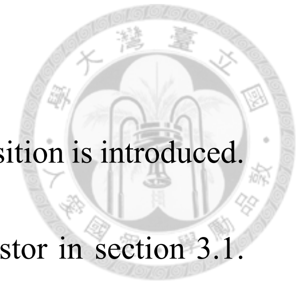
3.5 Summary



In this chapter, the complete model analysis of the turn-on transition is introduced. We first build the equivalent circuit model of E-mode GaN transistor in section 3.1. Based on the similar behavior of MOSFET, the double pulse test equivalent turn-on transition model is given in section 3.2 and 3.3. Finally, the full analysis is given in section 3.4, we find out the s-domain V_{gs} equation also the initial conditions. Also, with the control theory, we find out the breakaway points at L-R_g plane where the $V_{gs}(t)$ is damped. In next chapter, we are doing the hardware implementation to find out the real parasitic inductance on the PCB board to furtherly verify the model in this chapter also find the appropriate resistor design to meet the requirement of the voltage spike.

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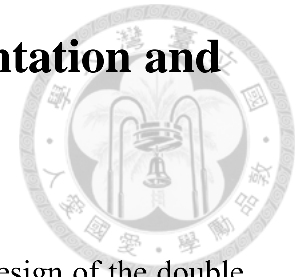

Chapter 4 Double Pulse Test Implementation and Model Verification

In this chapter, we focus on the printed circuit board (PCB) design of the double pulse test circuit. The layout concern and the parasitic inductance extraction will be introduced here. As introduced in chapter 2, parasitic components are the cause of the instability. Also, we derive the circuit model which shows the influence of the inductance in chapter 3. In section 4.1, we will introduce the decision of the output diode and inductor, also other components. In section 4.2, the PCB layout configuration and the parasitic inductance extraction using ANSYS Q3D extractor will be shown. The verification of the model derived in chapter 3 based on the real parameters of PCB will be introduced in section 4.3. And finally, section 4.4 concludes this chapter.

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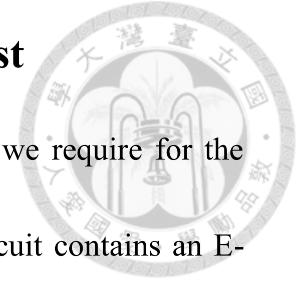
4.1 Components Decision of Double Pulse Test



Recalling the circuit topology of Fig. 3.14, the components we require for the measurement are introduced in this section. Double pulse test circuit contains an E-mode GaN transistor, a driver IC, an output diode and an inductor. Also, for the measurement of output current, we add a current shunt at the power loop.

For the E-mode GaN transistor, we have already derived and verified the circuit model of the transistor manufactured by EPC. We choose two transistors here, one is EPC2014C and the other one is EPC2022. The voltage, current level and other parameters of two transistors are shown in Table 4.1. Two transistors are for different applications, EPC2014C features its low input capacitance that is suitable for high frequency applications and EPC2022 has lower on resistance which fits high-power applications.

	EPC2014C	**EPC2022**
V_{ds} Maximum Rating	40V	100V
I_{ds} Maximum Rating	10A	90A
$R_{ds,on}$	16mΩ	3.2mΩ
C_{iss}(typical)	220pF	1400pF
C_{oss}(typical)	150pF	840pF
C_{rss}(typical)	6.5pF	7pF
R_{gate}	0.4Ω	0.3Ω

Table 4.1 Ratings table of EPC2014C and EPC2022 [13] [17]

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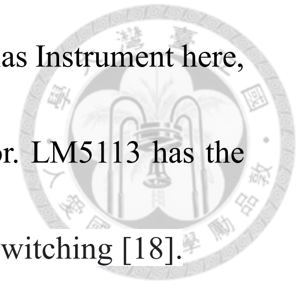

For the driver IC, we choose the LM5113 manufactured by Texas Instrument here, which is customized for the applications of E-mode GaN transistor. LM5113 has the internal pull-up resistor of 2.1Ω and is suitable for high frequency switching [18].

For the current shunt of the measurement, we choose the coaxial shunt SSDN-10 manufactured by T&M Research Products which features its high bandwidth up to 2GHz and its accurate resistance. The resistance of SSDN-10 is 0.1Ω, which will make little influence when it is in series connection with the transistor [19].

The most important thing we need to concern about the output diode and inductor is their equivalent parallel capacitance (EPC). As introduced in section 3.3, the output circuit can be considered as an ideal current source since the turn-on transition is short enough, the output inductor is large enough and the EPC is small enough, which makes the impedance ignorable. Also, the diode choice requires the fast recovery of the reversed charge since the switching frequency is set to be Megahertz level. Considering the restriction, the Schottky diode RB168MM150TF manufactured by Rohm Semiconductor and the inductor SER2211-273MED manufactured by Coilcraft are chosen to be the output circuit. The specification of these components is shown in table 4.2 and table 4.3. The EPC of the inductor can be calculated when self-resonant frequency is known by equation (4.1).

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Forward Voltage	Current Average	T_{rr} (Average)	EPC @ 5V 1MHz	EPC @ 10V 1MHz
0.76V	1A	7.15ns	30pF	23pF

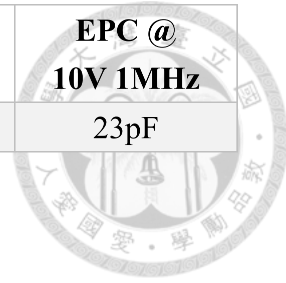

Table 4.2 Specification of RB168MM150TF [20]

Inductance	ESR	Self-resonant Frequency	EPC
27.3uH	6.84mΩ	12MHz	6.51pF

Table 4.3 Specification of SER2211-273MED [21]

$$f_s = \frac{1}{2\pi\sqrt{LC_p}} \quad (4.1)$$

4.2 PCB Layout Configuration and Parasitic Extraction

In section 4.1, the components decision of the double pulse test experiment is introduced. In this section, the PCB layout of the double pulse test and the parasitic inductance extraction will be illustrated. The footprint of EPC2014C and EPC2022 are different, thus two different boards are required for them. Fig. 4.1 shows two different footprints of EPC2014C and EPC2022. The reason of that drain and source are the interleaving pins is for the minimum parasitic effects.

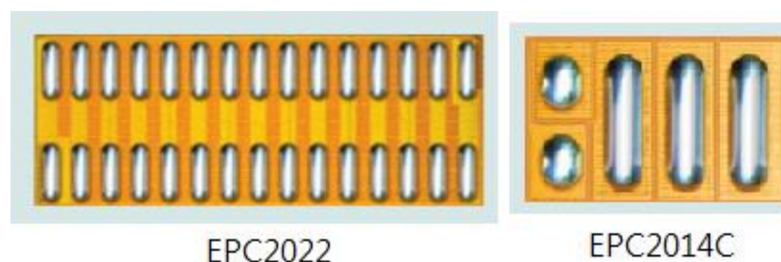

Fig. 4.1 Footprints of EPC2022 and EPC2014C [13] [17]

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From Fig. 4.2 to Fig. 4.5 shows the PCB layout of the EPC2014C testing board. Board A features the compact layout, that the current trace of power loop and gate loop is as short as possible which avoids the large parasitic inductance. Fig. 4.2 marks the key components, the power loop and the gate loop inside the circuit, and the following figures skip this part since the same definition as Fig. 4.2. Board B is the medium layout, and the Board C has the worst layout condition that its gate loop and power loop are all longer than others. Board D is the contrast one that the gate loop is the shortest and no external resistor but with the worst drain layout. Table 4.4 shows the result of parasitic extraction of four boards.

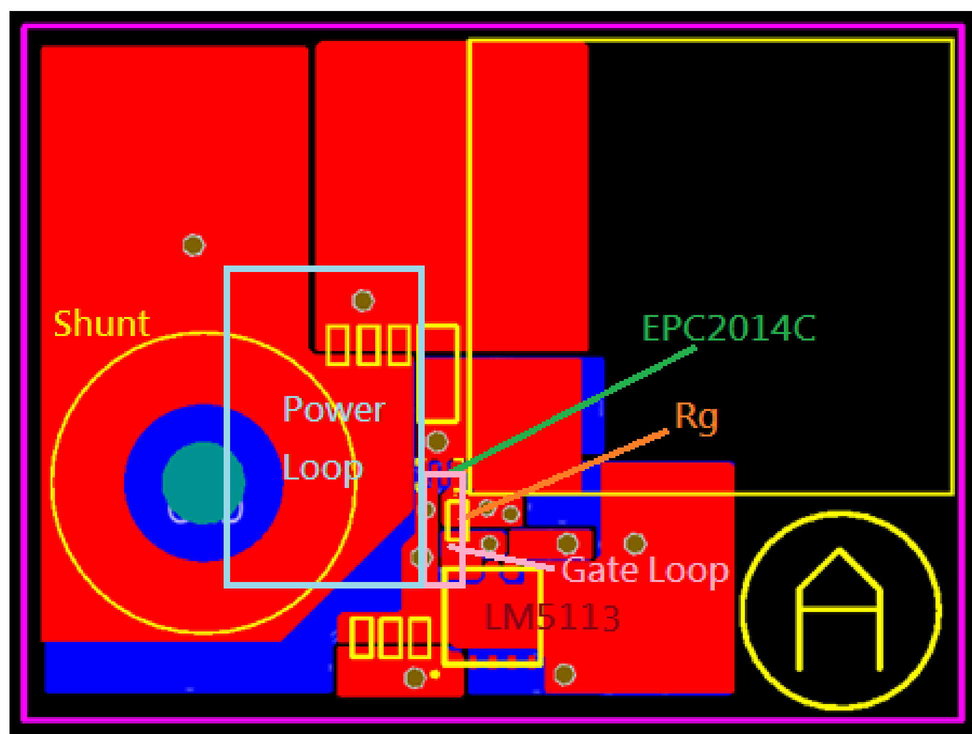

Fig. 4.2 Layout of double pulse test board A

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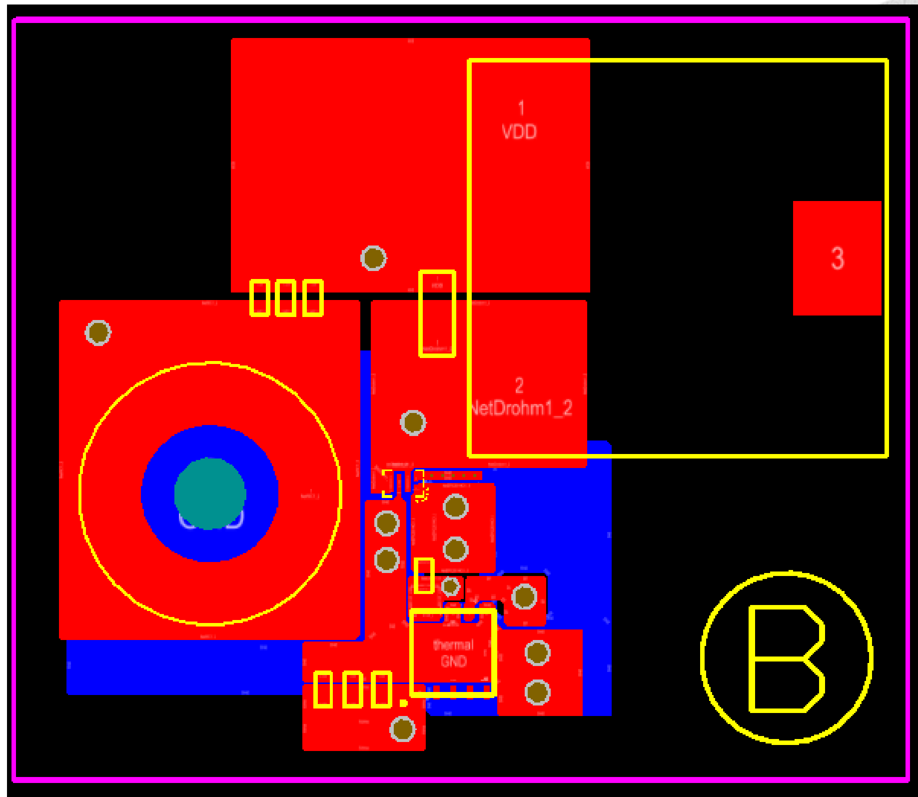

Fig. 4.3 Layout of double pulse test board B

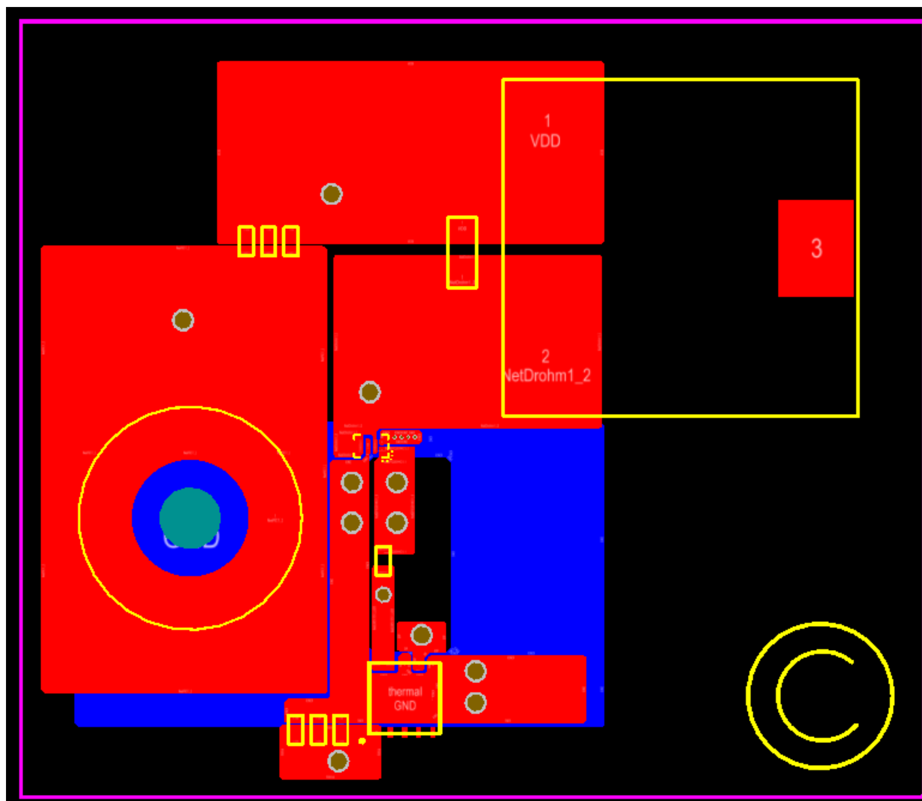

Fig. 4.4 Layout of double pulse test board C

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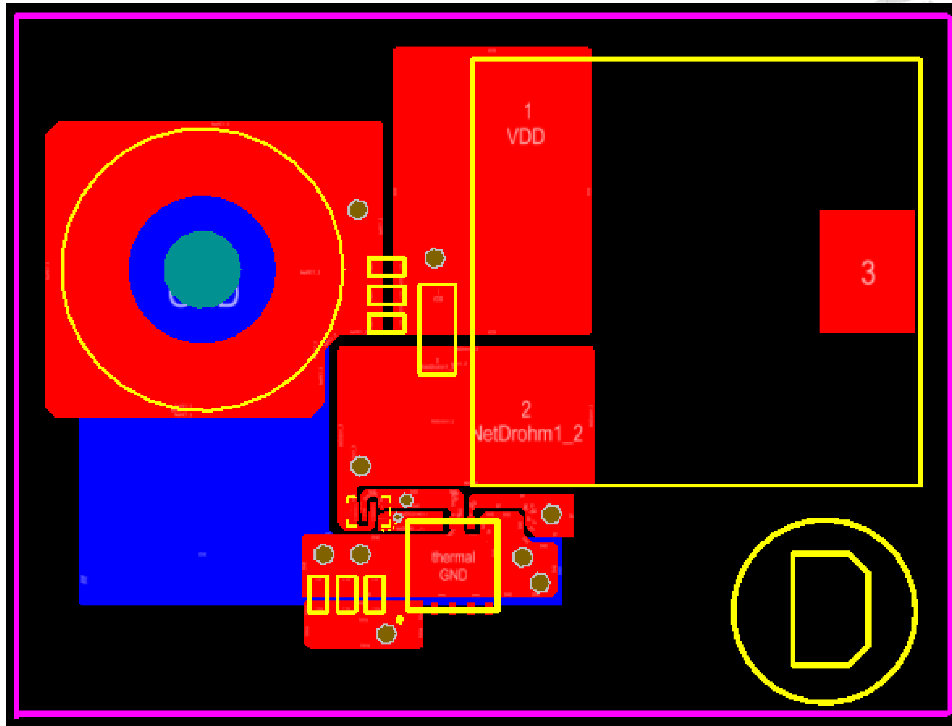

Fig. 4.5 Layout of double pulse test board D

	L_g	L_d	L_{cs}
Board A	0.99nH	0.69nH	0.31nH
Board B	2.99nH	1.62nH	0.48nH
Board C	7.02nH	1.96nH	0.39nH
Board D	0.82nH	4.08nH	1.15nH

Table 4.4 PCB extraction of testing boards of EPC2014C

On the other hand, board E and board F are the testing boards of EPC2022. Board E features worse layout condition as board C and board F is the medium one. The layout configuration of two boards are shown in Fig. 4.6 and 4.7, and the result of parasitic extraction is shown in Table 4.5.

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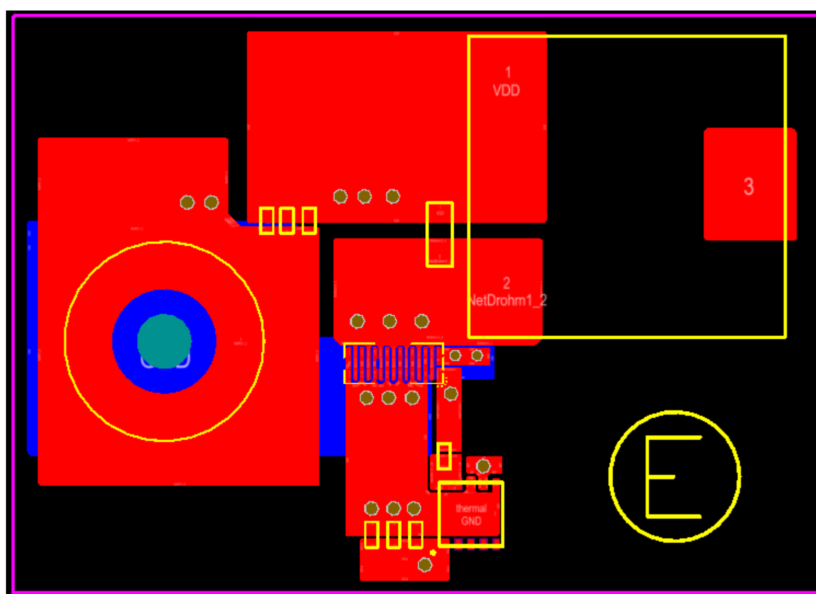

Fig. 4.6 Layout of double pulse test board E

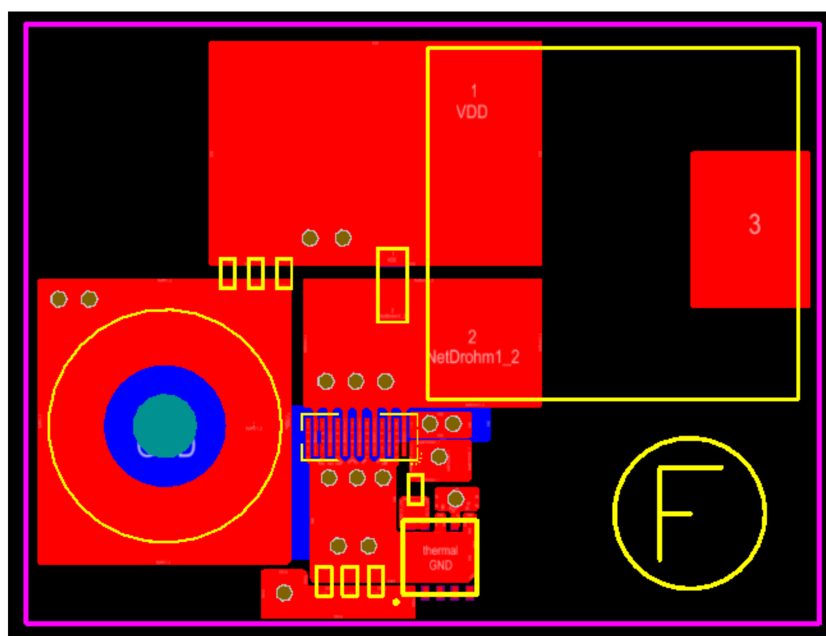

Fig. 4.7 Layout of double pulse test board F

	L_G	L_D	L_{CS}
BOARD E	4.23nH	1.02nH	0.71nH
BOARD F	2.05nH	1.15nH	1.04nH

Table 4.5 PCB extraction of testing boards of EPC2022

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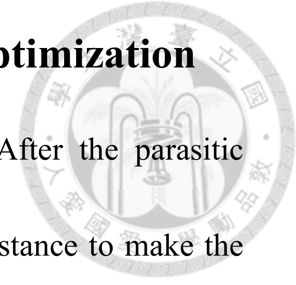
4.3 Circuit Model Verification and Design Optimization



Finally, we reach the final part before the measurement. After the parasitic extraction, we have sufficient conditions to derive the critical resistance to make the voltage spike at desire level. The verification contains three parts, first part is the model comparison of second order one and proposed one, the second part is the circuit simulation using SIMPLIS with model given by manufacturer and simplified model as Fig. 3.18. The third part is the critical resistor derivation using MATLAB by doing the inverse Laplace transform of the mathematical model with given initial conditions. The measurement result will be shown in chapter 5.

In chapter 3, we have derived the breakaway resistance of the full model of double pulse test, we first compare the difference between second order approximation and proposed model here. Taking board A as example, the sum of gate inductance and common source inductance is equal to 1.30nH, when we use the second model, the gate resistor is considered to be 4.93Ω by equation (3.6), the estimated breakaway resistance is 4.01Ω. Fig. 4.8 shows the verification of two method under double pulse test circuit simulation. Red curve is the proposed model and the green one is the second order one. The second order model is over-designed shown by the figure. The switching loss of second order approximation is 12.4nJ and the proposed one is 10.7nJ, which is improved by 25%.

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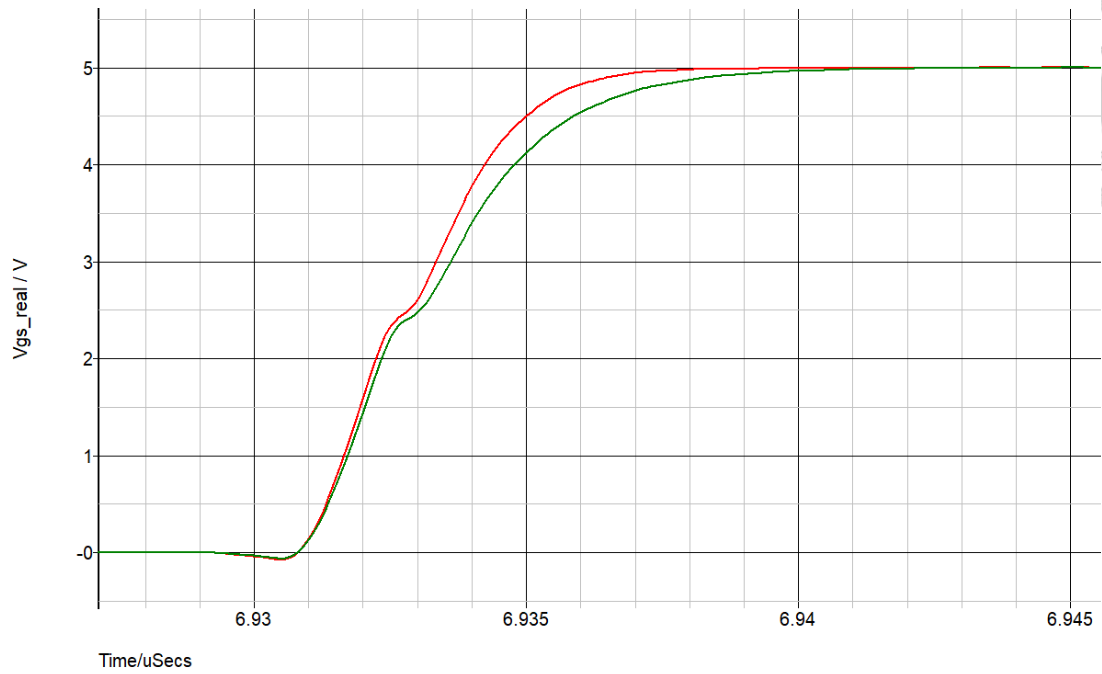

Fig. 4.8 V_{gs} waveforms of second order model and proposed model

As introduced in section 3.4, the initial conditions can be obtained by parameters given. For EPC2014C, we choose two specifications for the verification. One is 5V with the 1A channel current, and the other one is 10V with the 2A channel current. Table 4.6 shows the initial conditions of the EPC2014C testing circuit, and the circuit simulation configurations using EPC SPICE model and simplified model are shown in Fig. 4.9 and Fig. 4.10.

	V_{GS0}	V_{GD0}	I_{G0}
5V/1A	1.788V	1.764V	1.52A
10V/2A	1.908V	1.876V	1.98A

Table 4.6 Initial conditions of EPC2014C testing circuit

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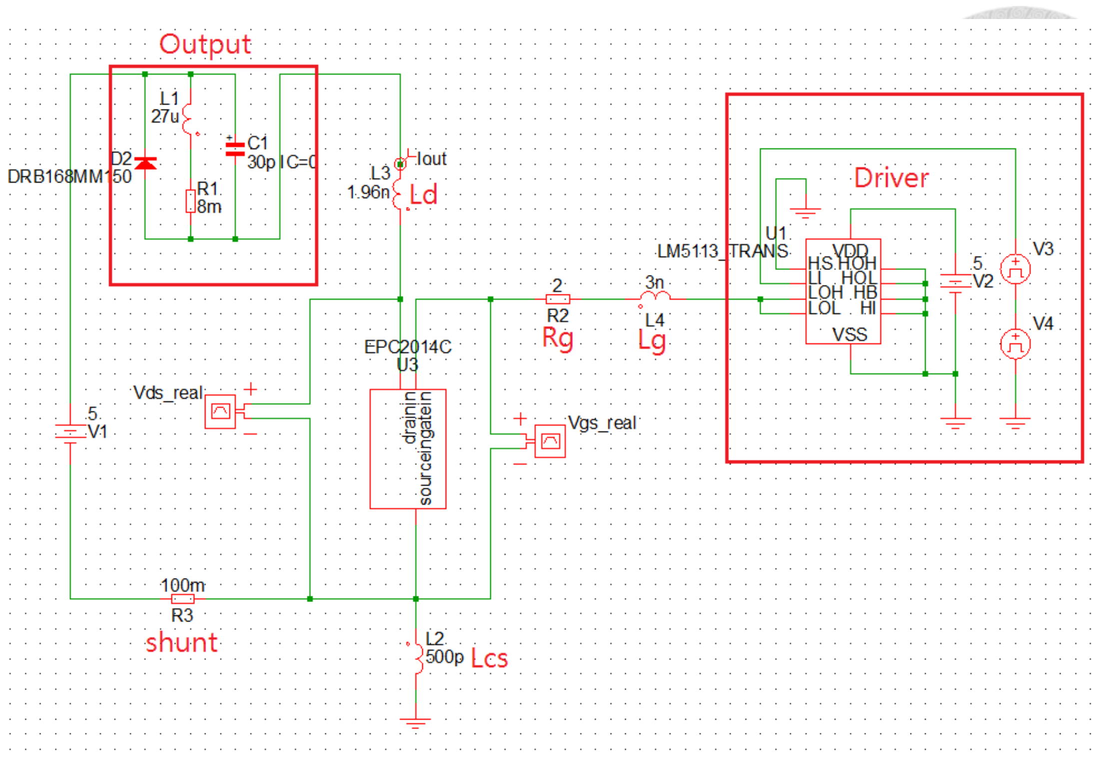

Fig. 4.9 Circuit simulation using EPC SPICE model

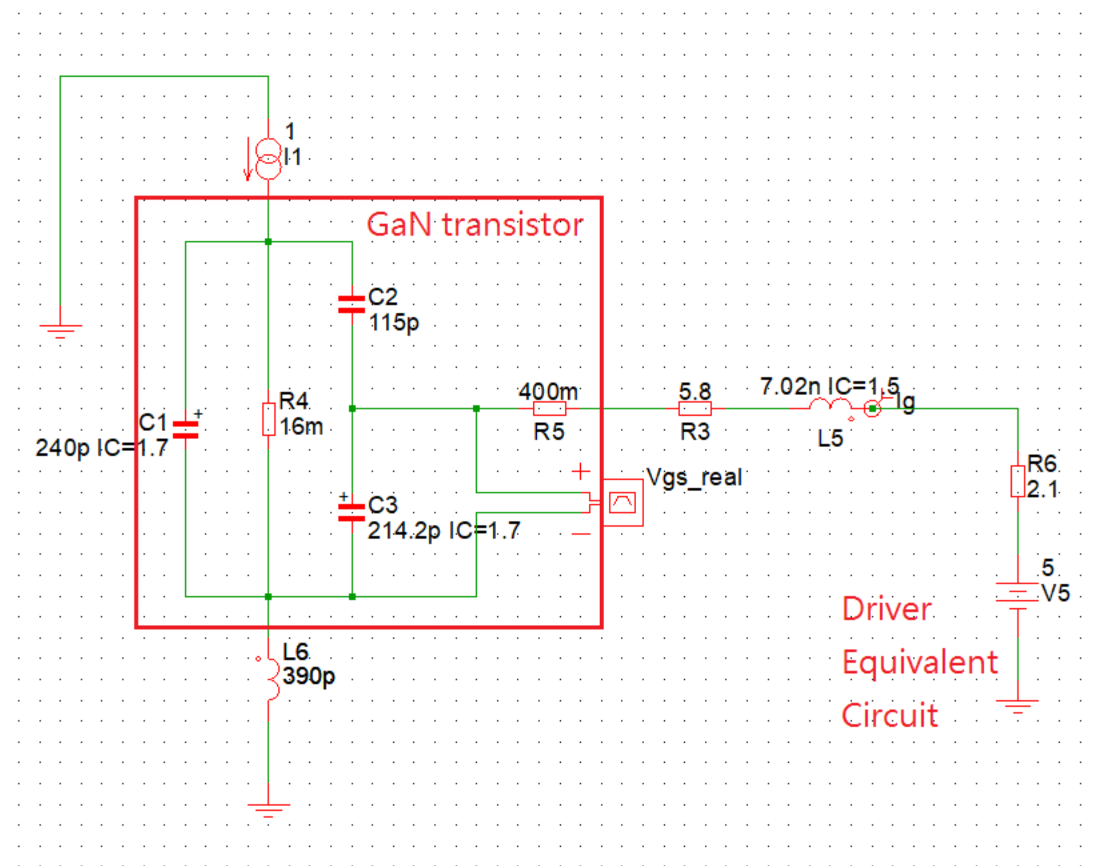

Fig. 4.10 Circuit simulation using simplified equivalent circuit model

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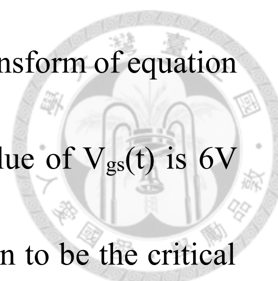

Table 4.7 shows the critical resistance using inverse Laplace transform of equation (3.28) with the parameters of EPC2014C. When the maximum value of $V_{gs}(t)$ is 6V after doing inverse Laplace transform, the resistance value is chosen to be the critical resistance. When resistance of gate loop is designed smaller than critical resistance, the breakdown of gate may occur. On the other hand, when resistance of the gate loop equals to $R_{G_breakaway}$, the damping ratio is considered to be 1, the voltage spike is suppressed under the design. The breakaway resistance has been derived in equation (3.49). When gate resistance is designed bigger than $R_{G_breakaway}$, it will be over-designed. The resistance choice of gate loop is defined as following equation (4.2).

$$R_{G_critical} \leq R_G \leq R_{G_breakaway} \tag{4.2}$$

	L_g+L_{cs}	$R_{G_critical}$@5V/1A	$R_{G_critical}$@10V/2A	$R_{G_breakaway}$
Board A	1.30nH	1.86Ω	2.15Ω	4.01Ω
Board B	3.47nH	4.15Ω	5.26Ω	7.91Ω
Board C	7.41nH	8.30Ω	10.81Ω	12.45Ω
Board D	1.97nH	2.58Ω	3.12Ω	4.94Ω

Table 4.7 Resistance design of different EPC2014C testing boards

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Following verification is based on the design of board B, Fig 4.11 shows the 5V/1A scale of the testing specification. The red curve shows the $V_{gs}(t)$ when $R_{g_external}$=1.65Ω, which means the gate resistance is equal to $R_{G_critical}$. Green curve shows the $V_{gs}(t)$ when $R_{g_external}$=5.41Ω, which means the gate resistance is equal to $R_{G_breakaway}$. Fig. 4.12 shows the waveforms of SPICE model when $R_{g_external}$=1.65Ω, and Fig. 4.13 shows the waveforms of SPICE model when $R_{g_external}$=5.41Ω. The maximum value of $V_{gs}(t)$ of SPICE model verification is about 5.7V and the maximum value of $V_{gs}(t)$ of simplified model is 5.9V when gate resistance is designed to be the value of $R_{G_critical}$. The deviation is reasonable due to the multiple reductions.

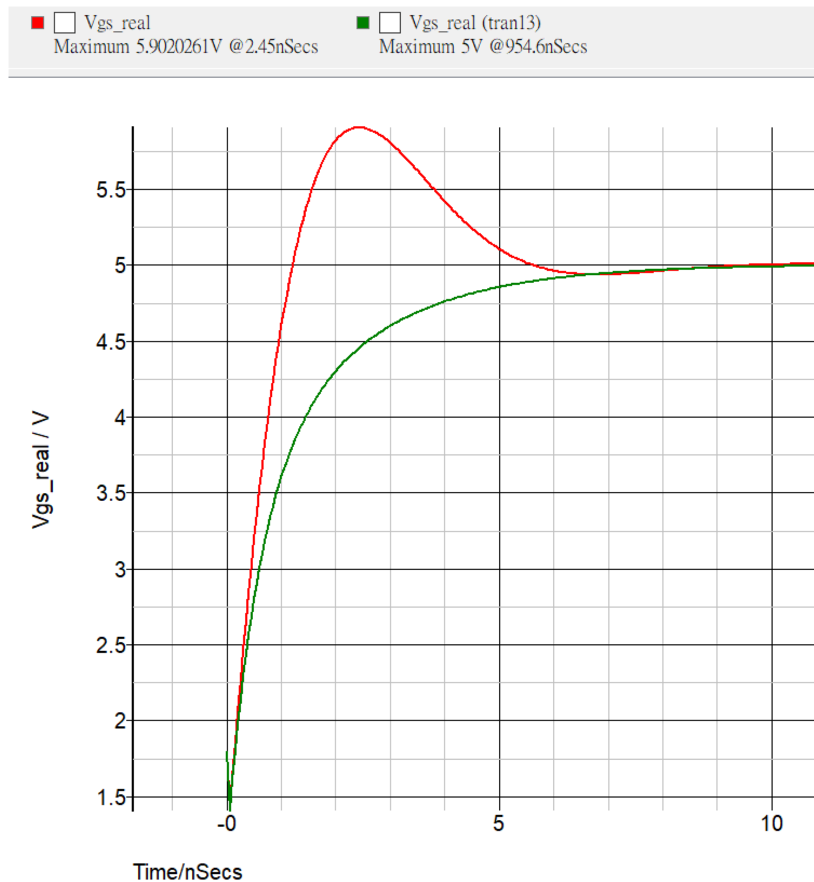

Fig. 4.11 Equivalent circuit model simulation of EPC2014C

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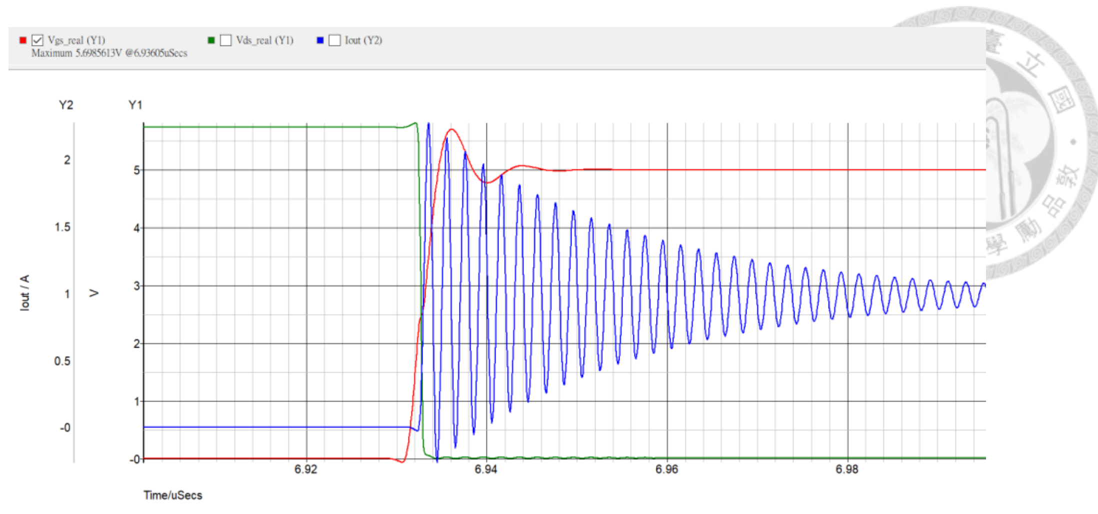

Fig. 4.12 SPICE simulation of EPC2014C when resistance equals to $R_{G_critcal}$

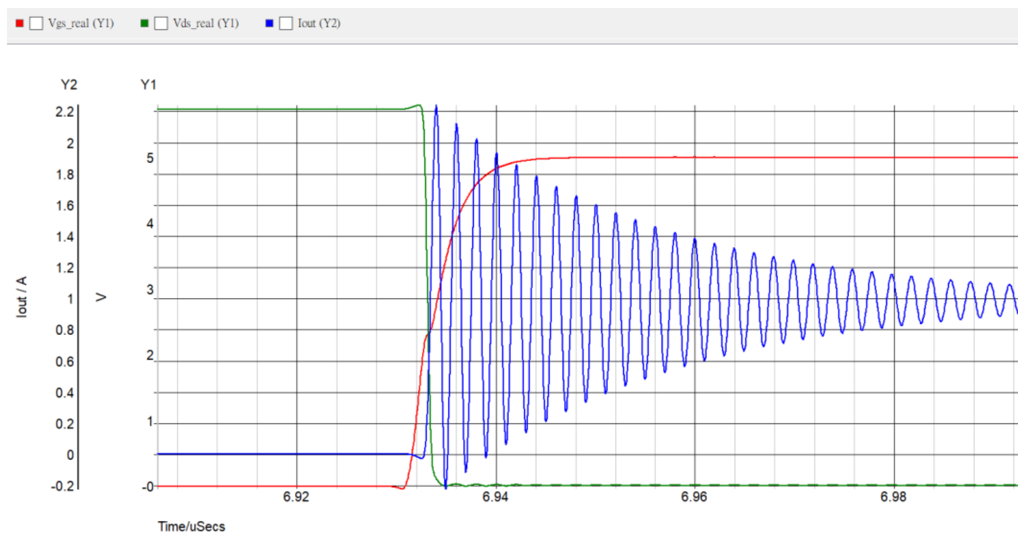

Fig. 4.13 SPICE simulation of EPC2014C when resistance equals to $R_{G_breakaway}$

We are doing the same procedure for EPC2022. Fig. 4.14 shows the output characteristic of EPC2022, table 4.8 shows the initial conditions based on the parameters of EPC2022, and table 4.9 shows the resistor design of two EPC2022 testing boards. Since the EPC2022 is for the large power applications, we applied two power levels of the design. One is 10V with the channel current of 2A and the other one is 25V with the channel current of 5A.

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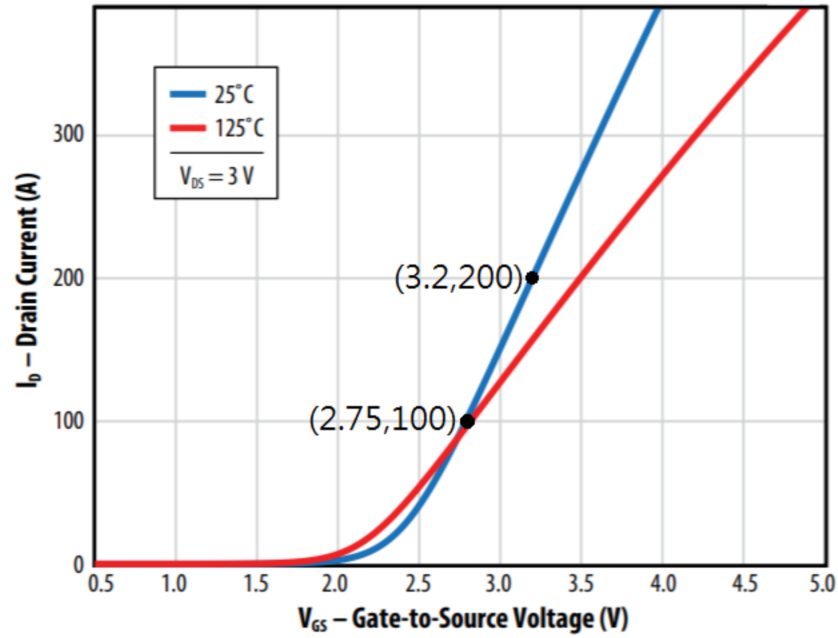

Fig. 4.14 Output characteristic of EPC2022 [17]

	V_{GS0}	V_{GD0}	I_{G0}
10V/2A	1.818V	1.812V	1.21A
25V/5A	1.917V	1.901V	2.57A

Table 4.8 Initial conditions of EPC2022 testing circuit

	L_g+L_{cs}	$R_{G_critical}$@10V/2A	$R_{G_critical}$@25V/5A	$R_{G_breakaway}$
Board E	4.94nH	1.41Ω	2.15Ω	3.43Ω
Board F	3.09nH	1.03Ω	1.43Ω	2.65Ω

Table 4.9 Resistance design of different EPC2022 testing boards

doi:10.6342/NTU202100458

Following verification is based on the design of board E, Fig 4.15 shows the 25V/5A scale of the testing specification. The driver contains the internal gate pull-up resistance of 2.1Ω and the gate resistor of EPC2022 is 0.3Ω, which means that we do not need to add the external gate resistance to avoid the breakdown of gate, since 2.4Ω is larger than $R_{G_critical}$. The red curve shows the $V_{gs}(t)$ when $R_{G_external}$=0Ω, and the green curve shows the $V_{gs}(t)$ when $R_{G_external}$=1.03Ω, which means the gate resistance is equal to $R_{G_breakaway}$. Fig. 4.16 shows the waveforms of SPICE model when $R_{G_external}$=0Ω, and Fig. 4.17 shows the waveforms of SPICE model when $R_{G_external}$=1.03Ω.

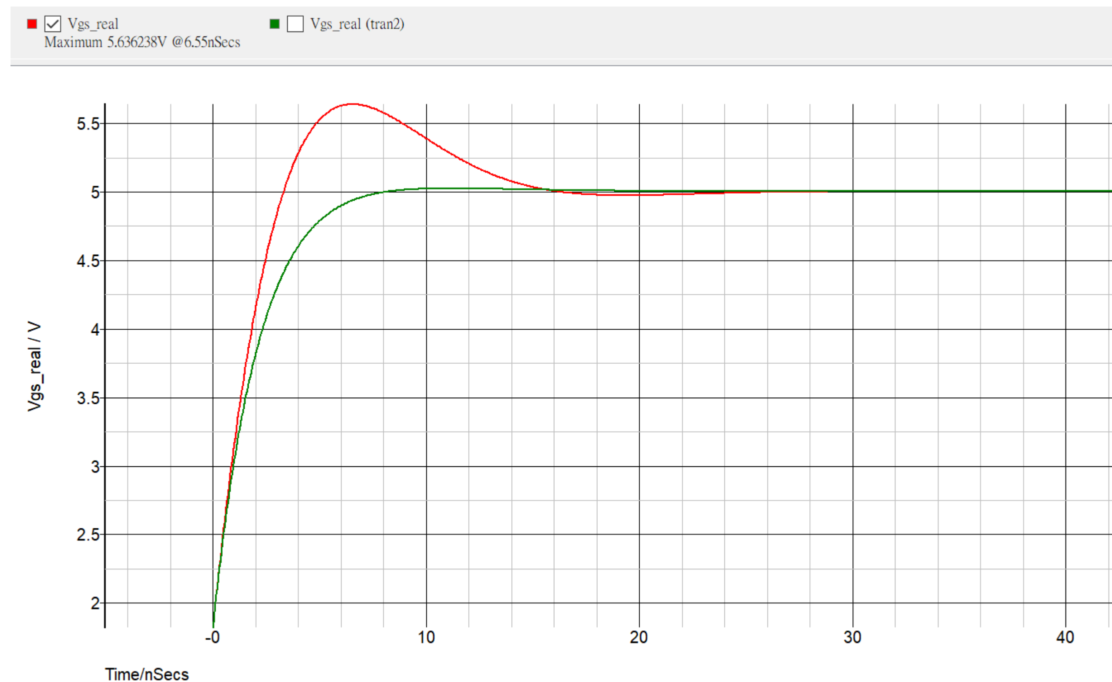

Fig. 4.15 Equivalent circuit model simulation of EPC2022

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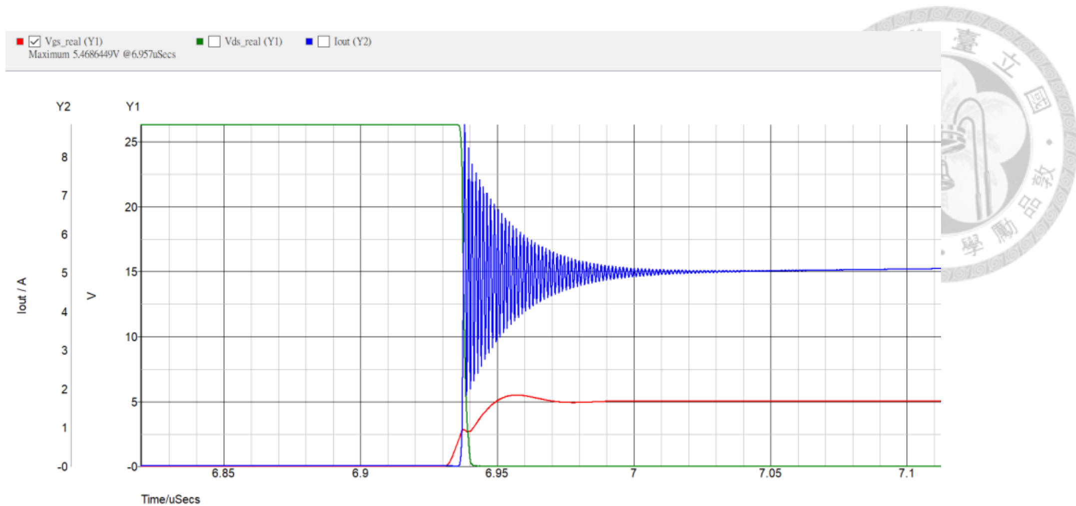

Fig. 4.16 SPICE simulation of EPC2022 when external resistance equals to zero

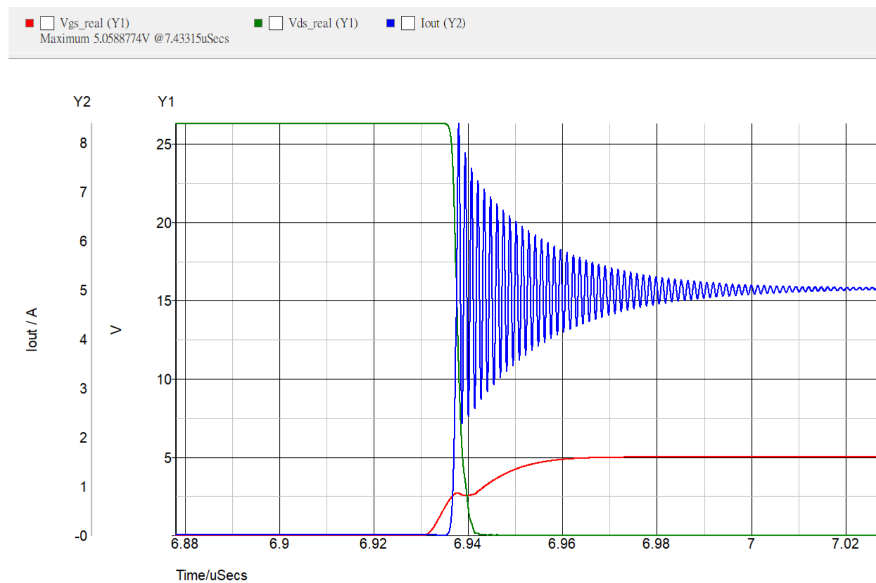

Fig. 4.17 SPICE simulation of EPC2022 when resistance equals to $R_{G_breakaway}$

The maximum value of $V_{gs}(t)$ of the simplified model is 5.64V when external gate resistance is equal to zero and voltage is damped when gate resistance is equal to $R_{G_breakaway}$. The SPICE model simulation shows that the maximum value of $V_{gs}(t)$ is 5.47V, which is smaller than the simplified one. The model is verified by circuit simulation and the deviation is acceptable due to the reduction of the circuit model.

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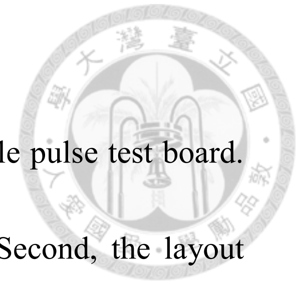
4.4 Summary



In this chapter, we have finished the PCB design of the double pulse test board. First, we have chosen the components to meet the restrictions. Second, the layout strategy of two different E-mode GaN transistor is introduced, and we also finished the parasitic inductance extraction to find the real circuit model based on the PCB design. And finally, the model derived in chapter 3 is also verified in this chapter with different approaches. The final thing we need to do is to do the measurement of the double pulse test experiment. The measurement set up, and the result of the experiment including voltage spike optimization and switching loss will be shown then in chapter 5.

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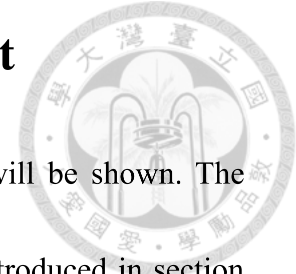
Chapter 5 Experiment Result



In this chapter, the result of double pulse test experiment will be shown. The measurement setup and the variables of the experiment will be introduced in section 5.1, and the measurement result and the switching loss calculation based on the measurement result will be displayed in section 5.2 then.

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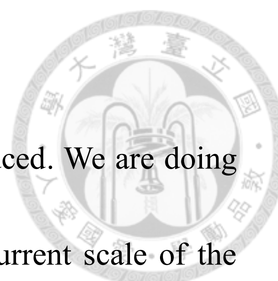
5.1 Experiment Setup



In this section, the overview of the experiment will be introduced. We are doing two groups of the experiment. Table 5.1 shows the voltage and current scale of the experiment, which is the same as the scale of the verification in section 4.3. The switching frequency of the transistor is the control variable, which is set to be 1MHz.

	EPC2014C	**EPC2022**
Low power	5V/1A	10V/2A
High power	10V/2A	25V/5A

Table 5.1 Voltage and current scales of the experiment

Fig. 5.1 presents the setup of the experiment. We are using FPGA board to provide the double pulse signal, the short probes on the PCB are to avoid the extra parasitic parameters for the accuracy of the measurement result.

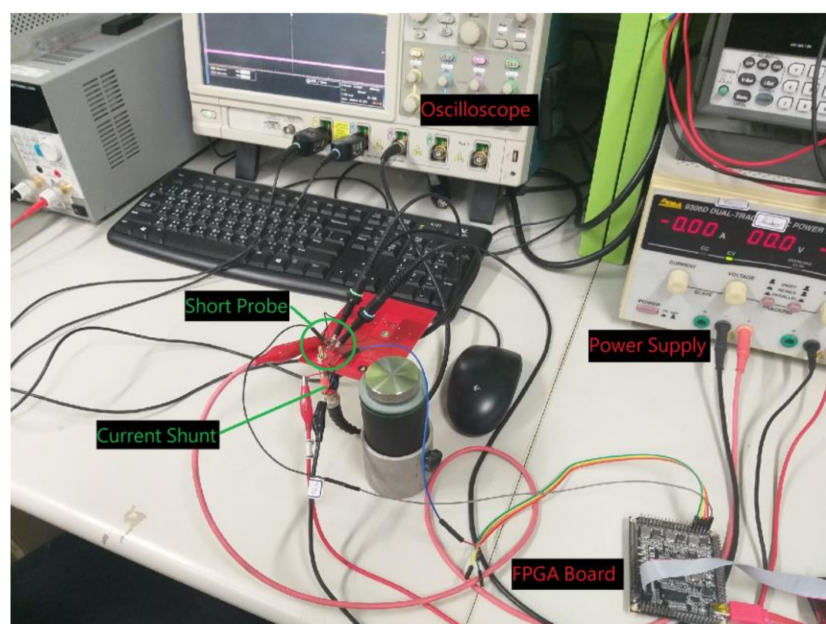


Fig. 5.1 Measurement setup of double pulse test experiment

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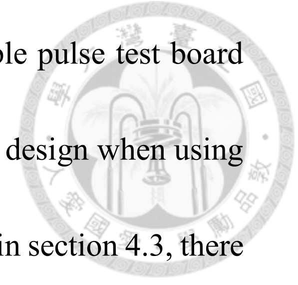

Table 5.2 shows the external resistor design of different double pulse test board using EPC2014C introduced in section 4.2, and table 5.3 shows the design when using EPC2022 as the switching device. As the mathematical verification in section 4.3, there exists the optimized external resistor design for each testing board. Some external resistors are designed to be zero, because the sum of the driver and transistor internal resistor is larger than the design one. The result based on the design and loss calculation will be shown in next section.

	Critical 5V/1A	**Critical 10V/2A**	**Breakaway**
Board A	0Ω	0Ω	1.6Ω
Board B	1.7Ω	2.8Ω	5.4Ω
Board C	4.8Ω	7.3Ω	10Ω
Board D	No gate external resistor		

Table 5.2 Optimized external resistor of testing board of EPC2014C

	Critical 10V/2A	**Critical 25V/5A**	**Breakaway**
Board E	0Ω	0Ω	1Ω
Board F	0Ω	0Ω	0Ω

Table 5.3 Optimized external resistor of testing board of EPC2022

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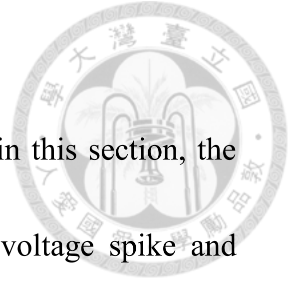
5.2 Measurement Result



The measurement result of double pulse test board is shown in this section, the waveforms will be displayed board by board, and the result of voltage spike and switching loss are given. The impact of parasitic inductance is suppressed under gate resistance designed as breakaway resistance, which will also be shown.

Board A features the strategy of compact layout. We do not need to add the external resistance to prevent the breakdown of gate since the sum internal resistance of driver and GaN device is larger than the critical resistance. Table 5.4 shows the voltage spike under different design criteria. Fig. 5.2 shows the waveforms of $V_{gs}(t)$, $V_{ds}(t)$ and $I_{ds}(t)$ when 5V/1A is applied and external resistor is equal to zero, and Fig 5.3 shows the waveforms when 10V/2A is applied and external resistor is equal to 1.6Ω.

The result shows that the voltage spike does not exceed maximum value when gate resistance is designed under proposed measure, and the parasitic effect caused by parasitic inductor is suppressed when breakaway resistance is applied.

Board A	**R_{g_ext}=0Ω**	**R_{g_ext}=1.6Ω**
5V/1A	5.575V	5.124V
10V/2A	5.675V	5.244V

Table 5.4 Results of voltage spike of Board A

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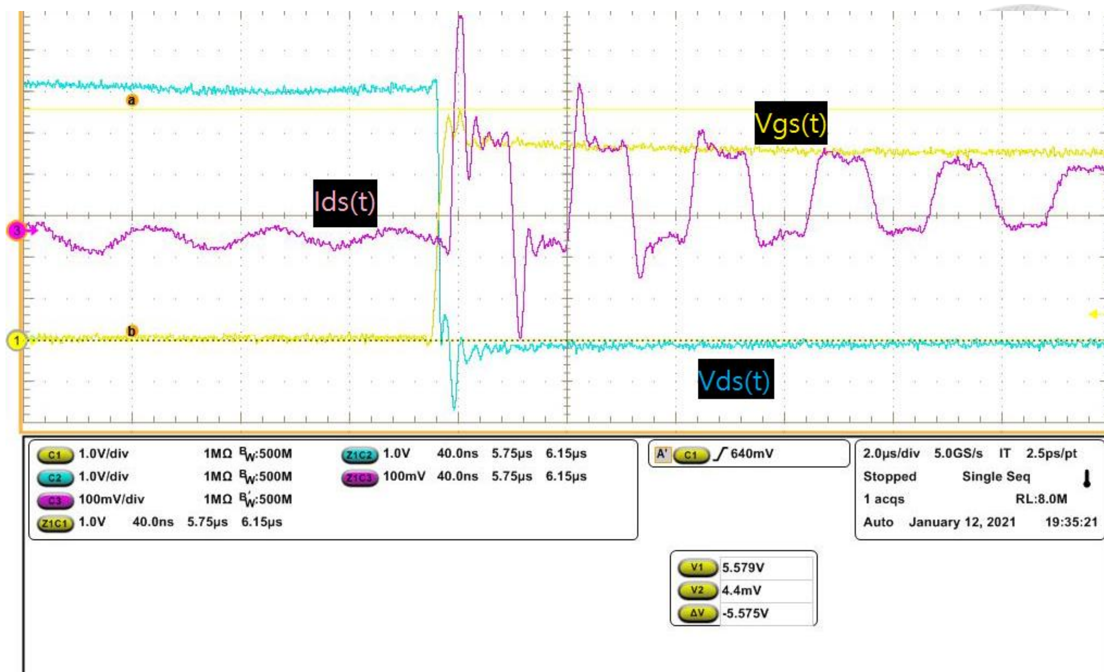

Fig. 5.2 Waveforms of board A when 5V/1A is applied and R_{g_ext}=0Ω

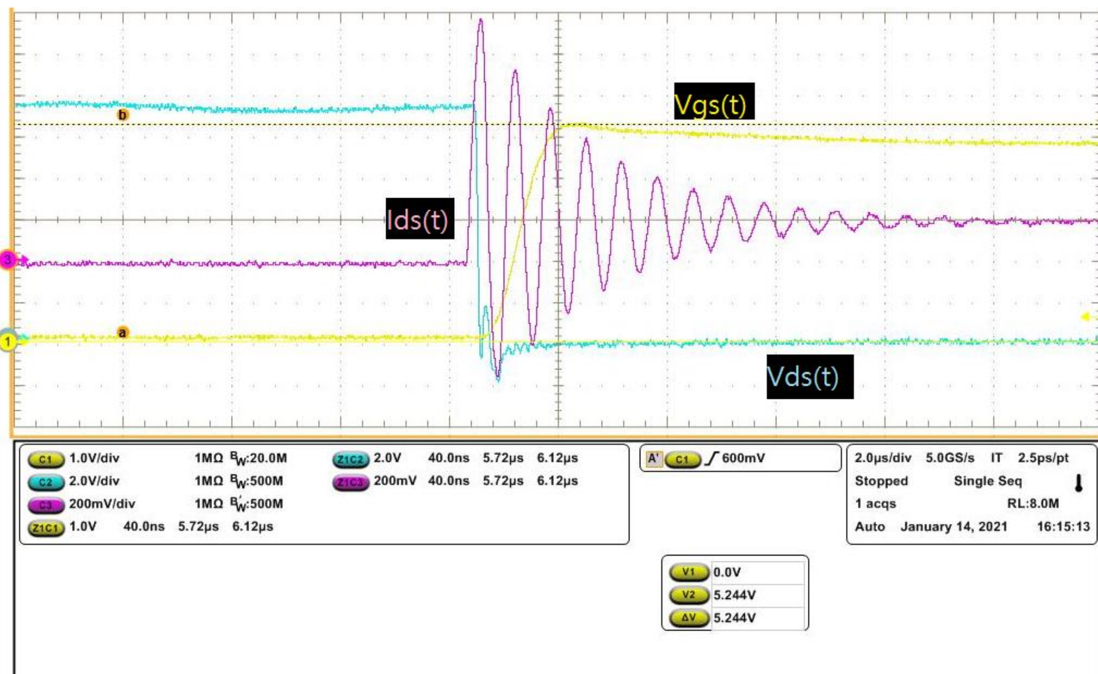

Fig. 5.3 Waveforms of board A when 10V/2A is applied and R_{g_ext}=1.6Ω

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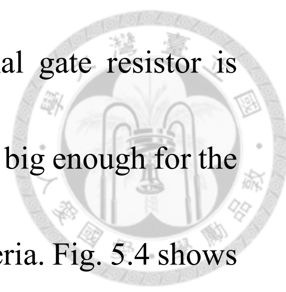

Board B features the strategy of normal layout. The external gate resistor is required since the sum of internal resistance of gate and driver is not big enough for the design. Table 5.5 shows the voltage spike under different design criteria. Fig. 5.4 shows the waveforms of $V_{gs}(t)$, $V_{ds}(t)$ and $I_{ds}(t)$ when 10V/2A is applied and external resistor is equal to 2.8Ω, which is the critical external resistance of the 10V/2A condition. Fig. 5.5 shows the waveforms when 5V/1A is applied and external resistor is equal to 5.4Ω, which is the breakaway external resistance of the 5V/1A condition.

Board B	**R_{g_ext}=1.7Ω**	**R_{g_ext}=2.8Ω**	**R_{g_ext}=5.4Ω**
5V/1A	6.059V	5.939V	≒5.2V
10V/2A	6.179V	6.079V	≒5.3V

Table 5.5 Results of voltage spike of Board B

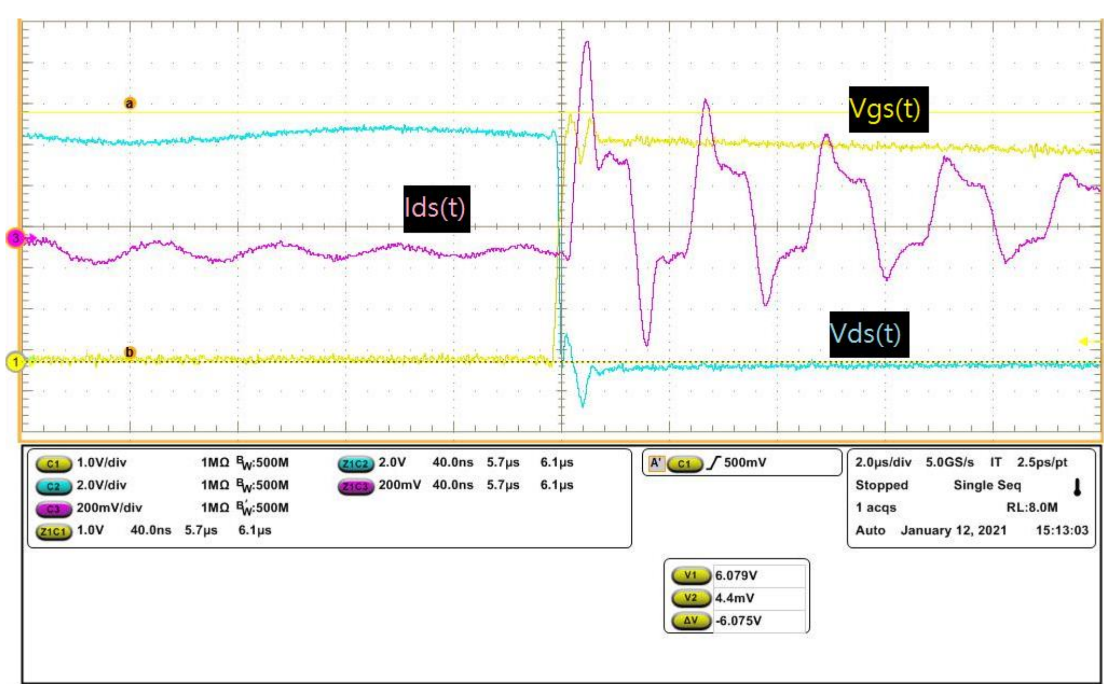

Fig. 5.4 Waveforms of board B when 10V/2A is applied and R_{g_ext}=2.8Ω

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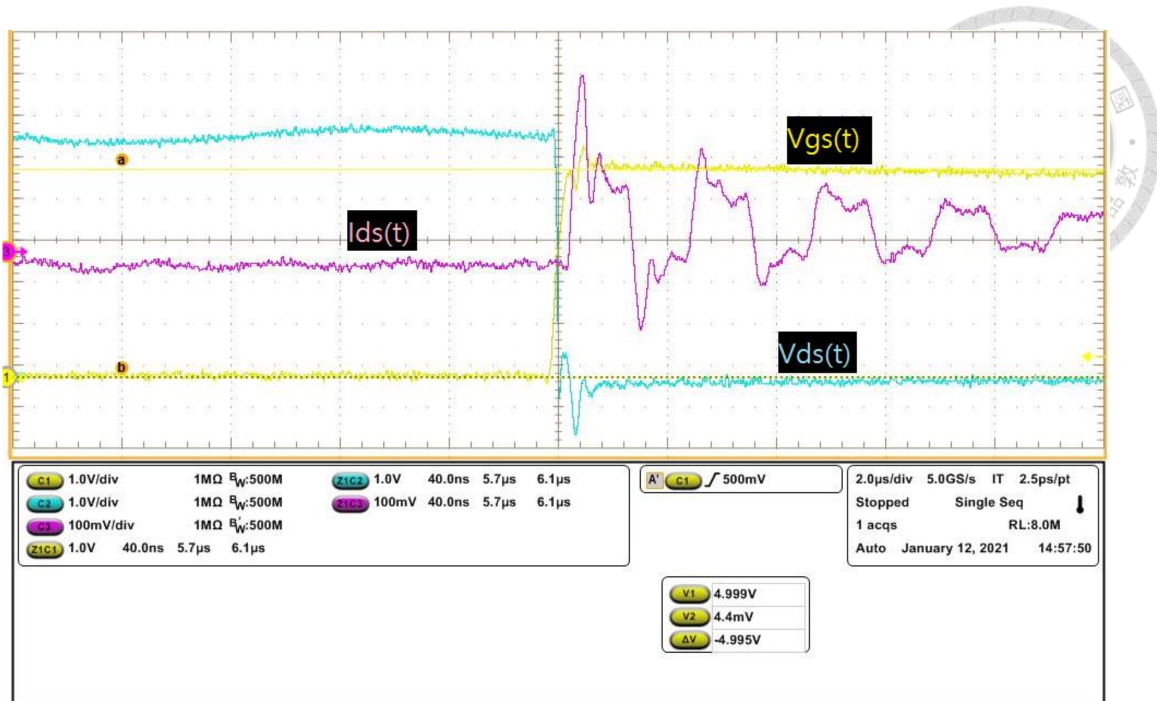

Fig. 5.5 Waveforms of board B when 5V/1A is applied and R_{g_ext}=5.4Ω

The result of board B has a little variation with the model estimation, the voltage spike can be observed when external resistor is equal to breakaway resistance, and the breakdown of gate is possibly occurred when resistance design is under the critical resistance. There are some possible reasons, one is the parasitic extraction definition. Since the gate loop and common source loop of the circuit are defined by user, the deviation may occur which results in the misestimation of the result. The other one is the reduction of the model. We ignore some conditions, but some ignored ones will still happen and impact the circuit such as the output not being the perfect current source and the output capacitance not being zero. The real components are not as ideal as we estimate. Thus, the result may not meet the expected values.

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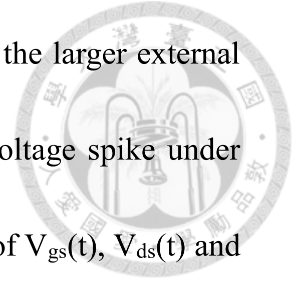

Board C features the strategy of loose layout, which requires the larger external resistance to suppress the parasitic effects. Table 5.6 shows the voltage spike under different design criteria of board C. Fig. 5.6 shows the waveforms of $V_{gs}(t)$, $V_{ds}(t)$ and $I_{ds}(t)$ when 5V/1A is applied and external resistor is equal to 4.8Ω, which is the critical external resistance of the 5V/1A condition. Fig. 5.7 and Fig. 5.8 show the waveforms when 10V/2A is applied and external resistor is equal to 7.3Ω and 10Ω, which are the critical and breakaway external resistance of the 10V/2A condition.

Board C	**R_{g_ext}=4.8Ω**	**R_{g_ext}=7.3Ω**	**R_{g_ext}=10Ω**
5V/1A	6.02V	5.802V	≒5.1V
10V/2A	6.4V	5.86V	≒5.1V

Table 5.6 Results of voltage spike of Board C

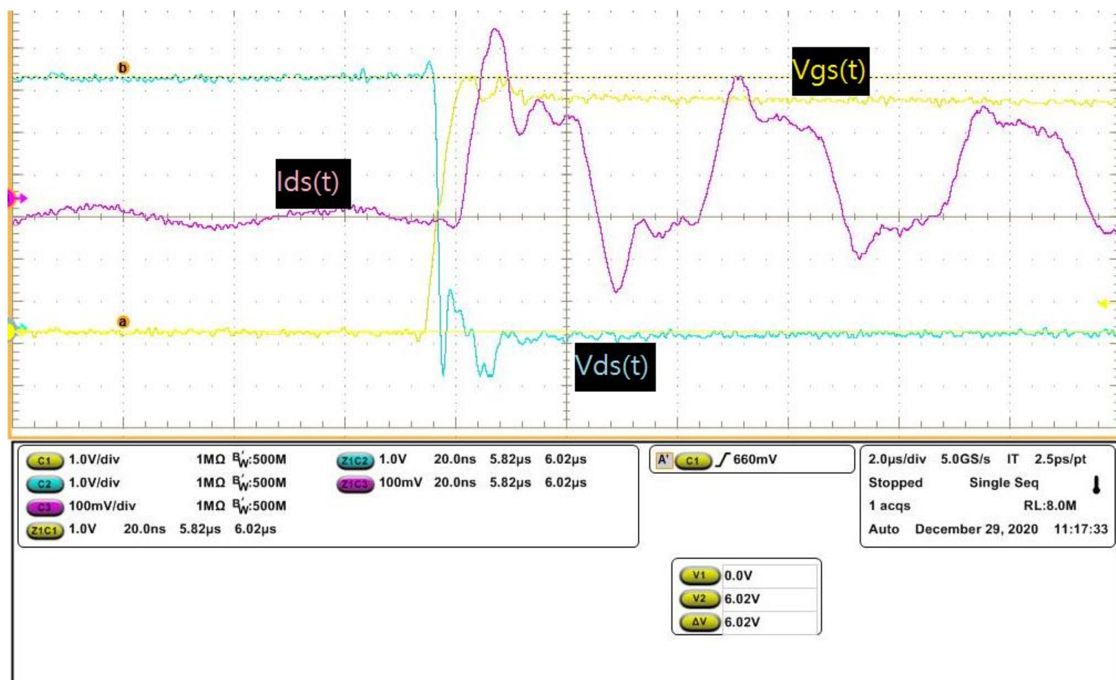

Fig. 5.6 Waveforms of board C when 5V/1A is applied and R_{g_ext}=4.8Ω

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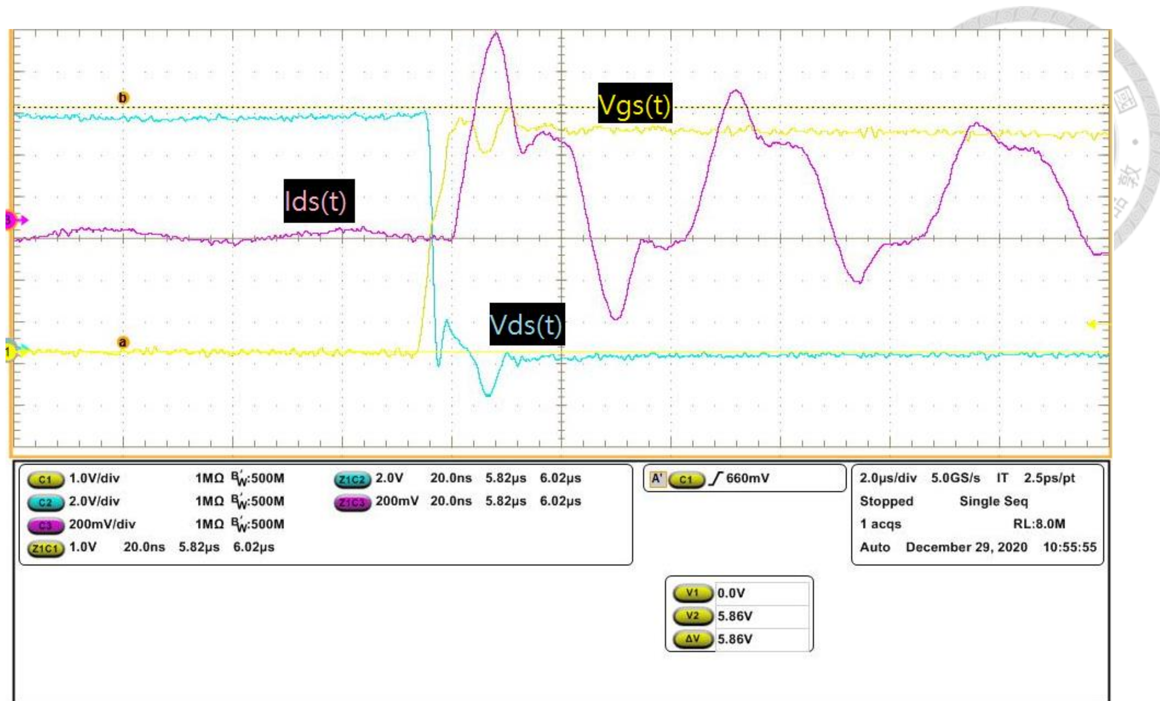

Fig. 5.7 Waveforms of board C when 10V/2A is applied and R_{g_ext}=7.3Ω

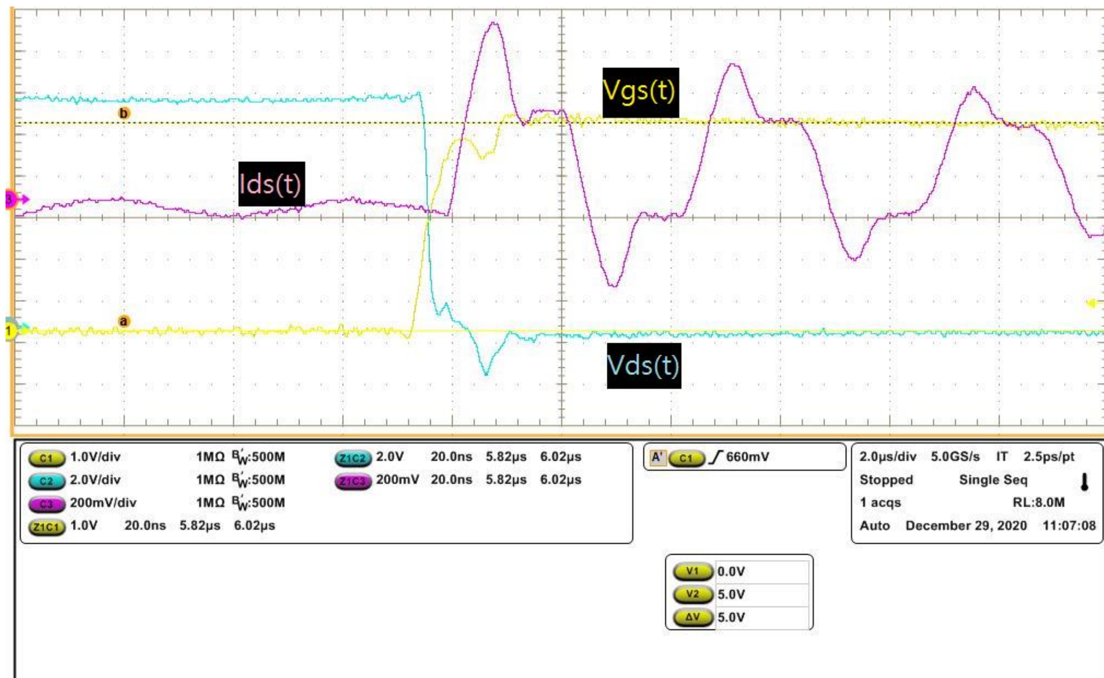

Fig. 5.8 Waveforms of board C when 10V/2A is applied and R_{g_ext}=10Ω

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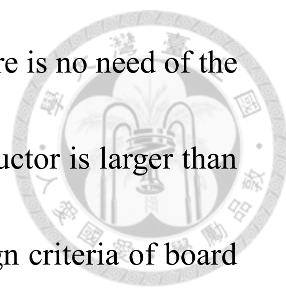

Board D features the best case of the testing condition, and there is no need of the external resistor to add to avoid the voltage spike, but the drain inductor is larger than other cases. Table 5.7 shows the voltage spike under different design criteria of board D. Fig. 5.9 shows the waveforms of $V_{gs}(t)$, $V_{ds}(t)$ and $I_{ds}(t)$ when 5V/1A is applied and Fig. 5.10 shows the 10V/2A ones.

Board D	**R_{g_ext}=0Ω**
5V/1A	5.184V
10V/2A	5.284V

Table 5.7 Results of voltage spike of Board D

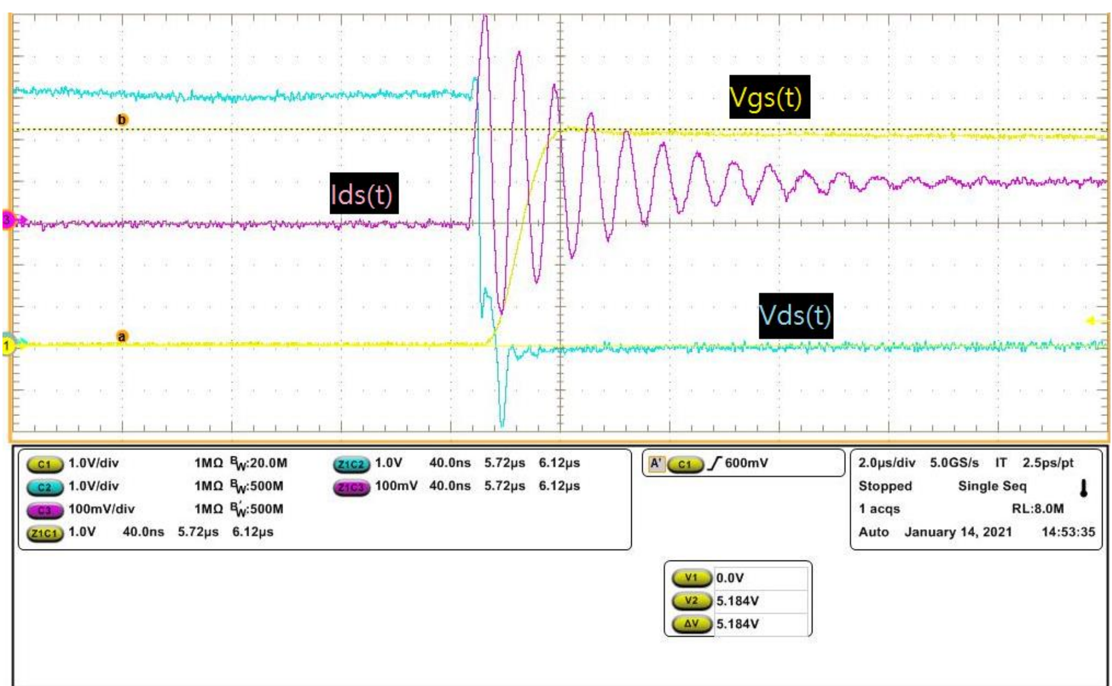

Fig. 5.9 Waveforms of board D when 5V/1A is applied

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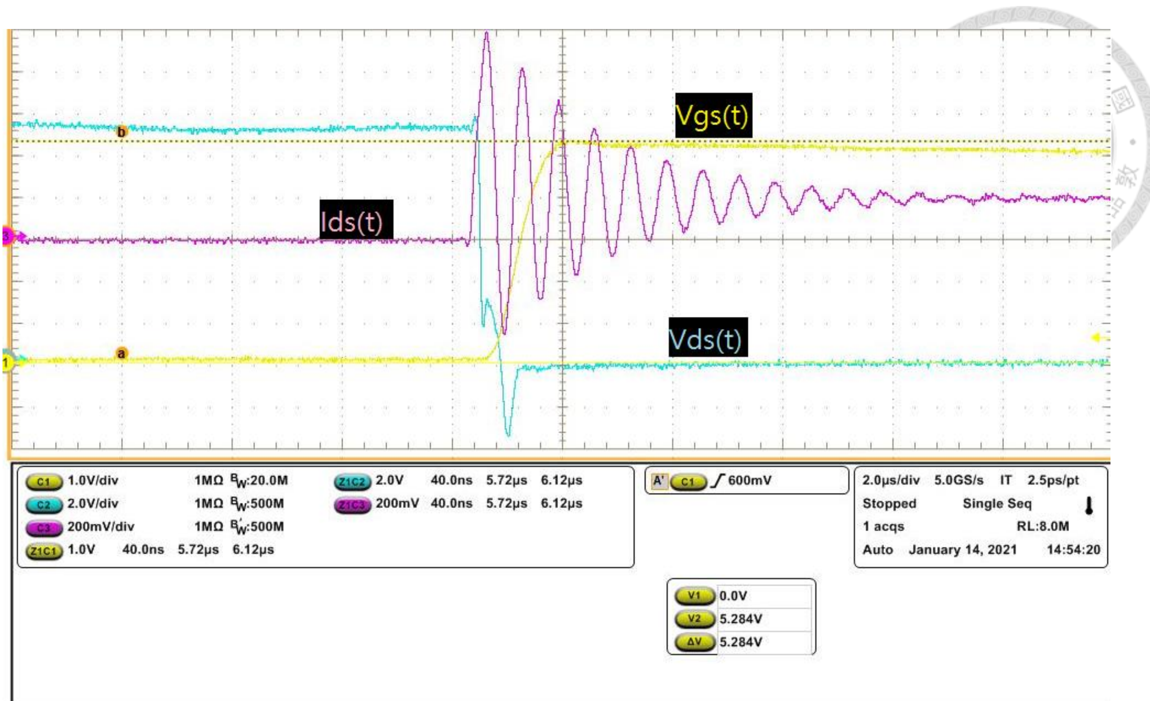

Fig. 5.10 Waveforms of board D when 10V/2A is applied

Board E and F are two comparison boards of EPC2022. Since the EPC2022 feature the bigger internal capacitance, the resistance design is not that rigorous as the EPC2014C ones. The testing conditions are 10V/2A and 25V/5A, the output influence is expected to be large since the output power is larger than EPC2014C ones. Table 5.8 and 5.9 shows the voltage spike under different design criteria of board E and F.

Board E	R_{g_ext}=0Ω	R_{g_ext}=1Ω
10V/2A	≒5.1V	5V
25V/5A	5.68V	5.5V

Table 5.8 Results of voltage spike of Board E

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Board F	R_{g_ext}=0Ω
10V/2A	5V
25V/5A	≒5.2V

Table 5.9 Results of voltage spike of Board F

Fig. 5.11 shows the waveforms when 10V/2A is applied and external resistor is equal to 1Ω, which is the breakaway external resistance of the 10V/2A condition of board E. Fig. 5.12 shows the waveforms when 25V/5A is applied and external resistor is zero, the voltage spike does not exceed the breakdown voltage, which matches the expected result.

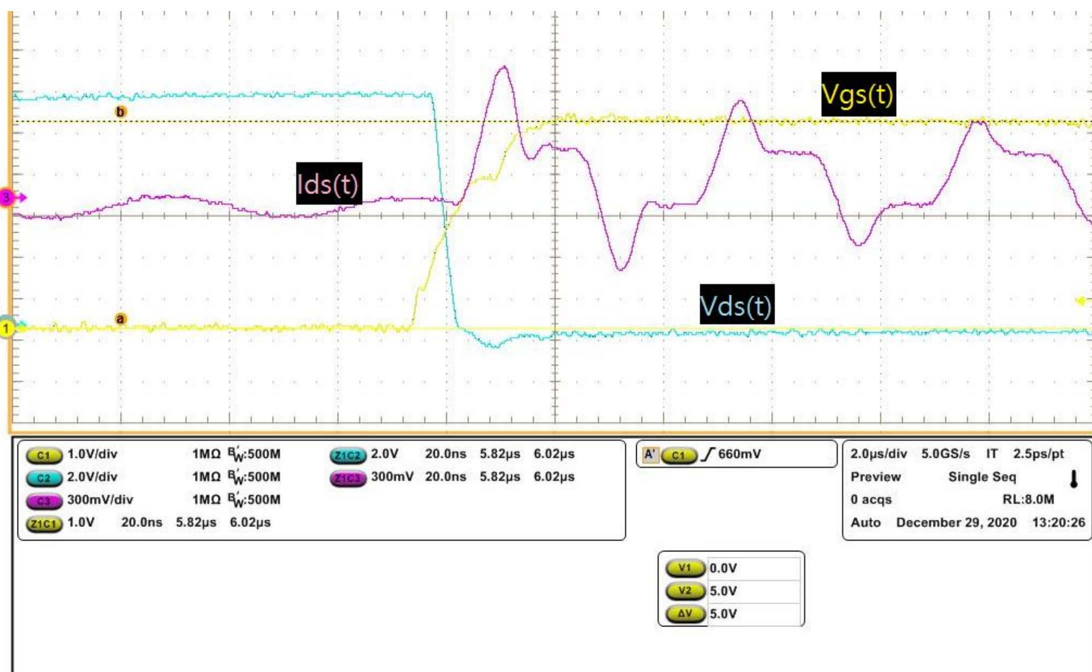

Fig. 5.11 Waveforms of board E when 10V/2A is applied and R_{g_ext}=1Ω

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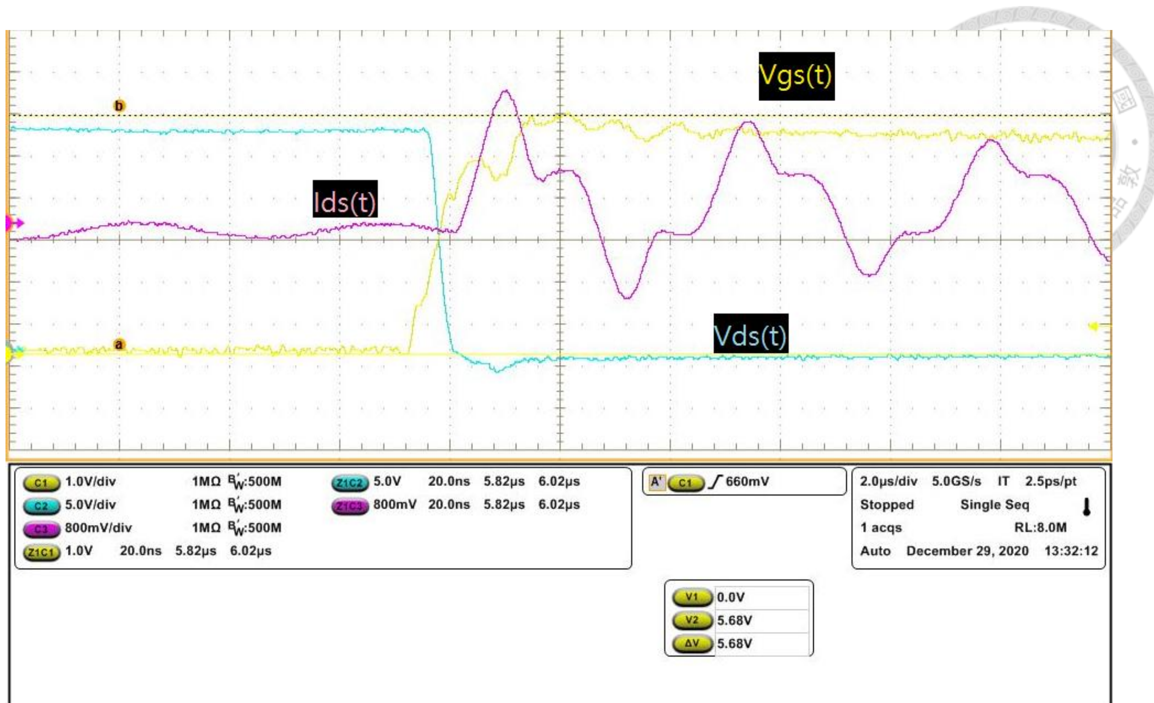

Fig. 5.12 Waveforms of board E when 25V/5A is applied and R_{g_ext}=0Ω

Fig. 5.13 shows the waveforms when 10V/2A is applied and Fig. 5.14 shows the waveforms when 25V/5A is applied of board F. The external resistance is zero due to that the parasitic inductance is small enough in gate loop.

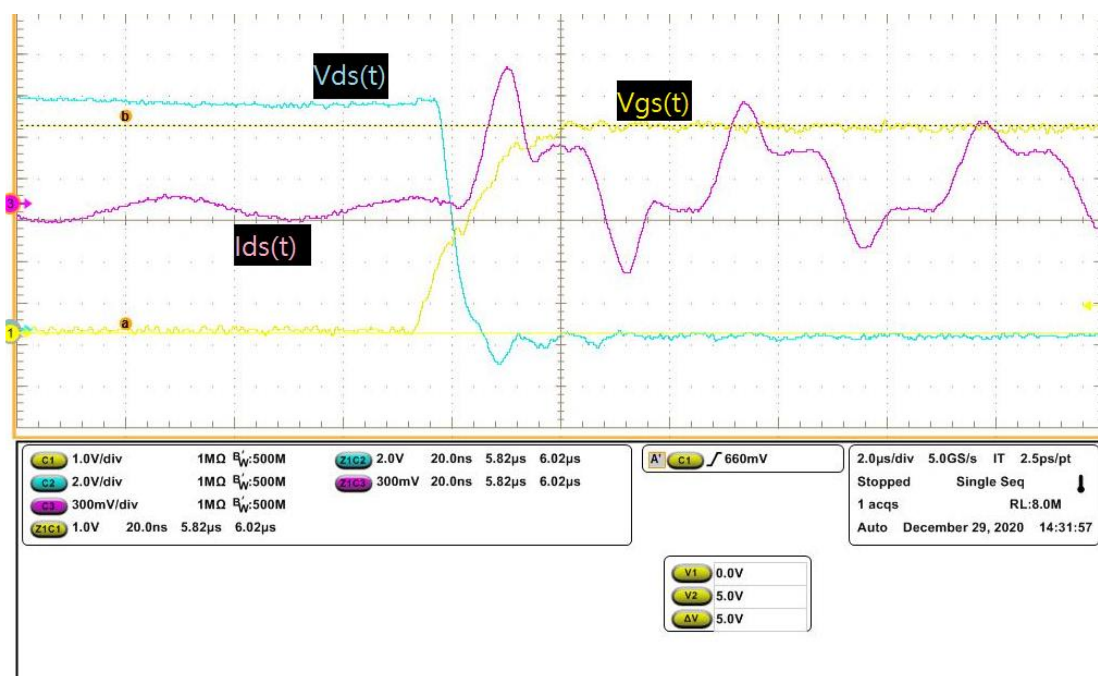

Fig. 5.13 Waveforms of board F when 10V/2A is applied

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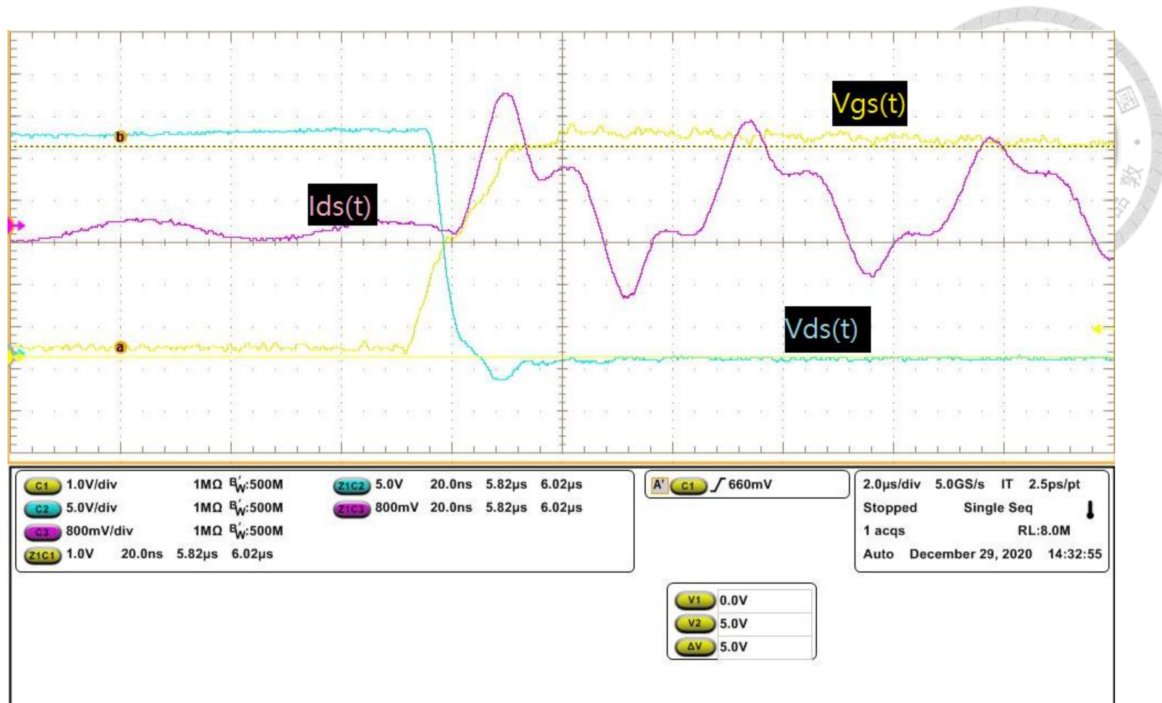

Fig. 5.14 Waveforms of board F when 25V/5A is applied

The measurement results are shown in former pages, the results roughly fit the verification in section 4.3. The voltage spike is expected to be exactly 6V when critical resistance is designed to be the gate resistance, and the voltage waveform is considered to be not oscillating when breakaway resistance is applied. There are the reasons make the result not match the expected value. Some are introduced before, and another reason is the non-ideal voltage source. The bulk capacitance is added at the voltage source to avoid the low-frequency resonance. However, there is still a little disturb on the voltage source which makes the voltage waveform distorted.

Fig. 5.15 shows the comparison figure of $V_{gs}(t)$ of measurement result, simulation result using SPICE model provided by EPC and MATLAB verification result of board C when 10V/2A is applied and gate resistance is equal to critical resistance

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(R_{g_ext}=7.3Ω). Fig. 5.16 shows the figure which 5V/1A is applied on board A and gate resistance is equal to breakaway resistance (R_{g_ext}=1.6Ω).

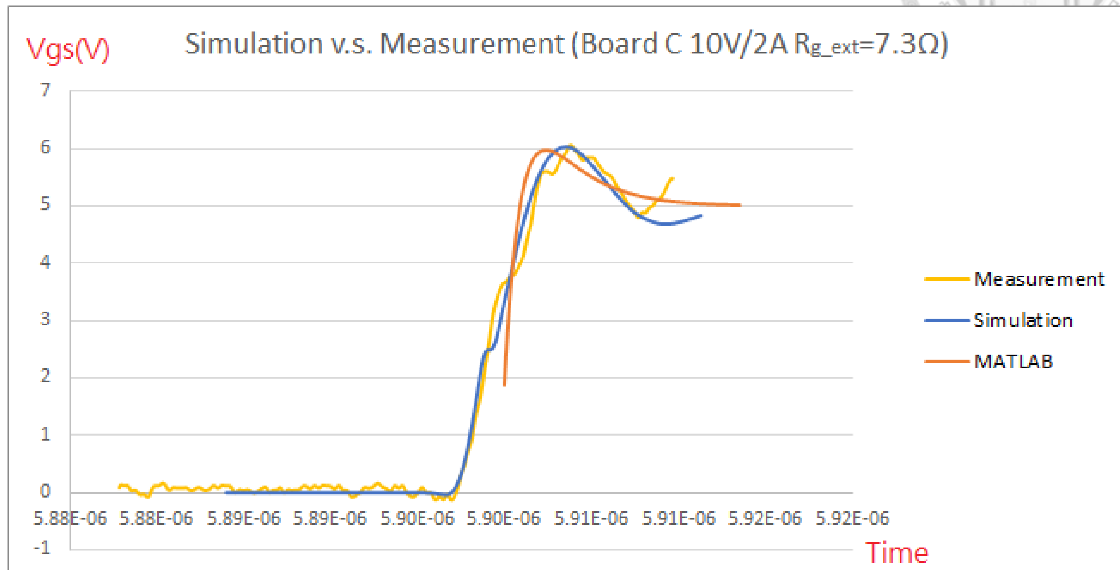

Fig. 5.15 Comparison figure of board C applying 10V/2A and critical resistance

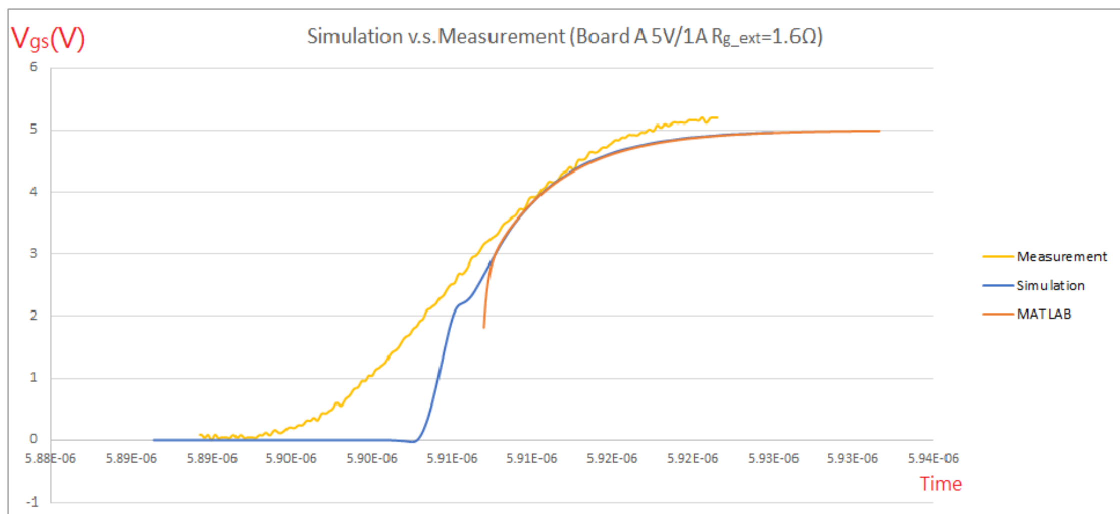

Fig. 5.16 Comparison figure of board A applying 5V/1A and breakaway resistance

The comparison figure of measurement and simulation shows that the result does not match very perfectly, however, the reason is mainly based on the modelling of the transistors. The initial voltage of the model, which is the miller voltage, is calculated based on the capacitance. Recalling the reduction of the model introducing in section

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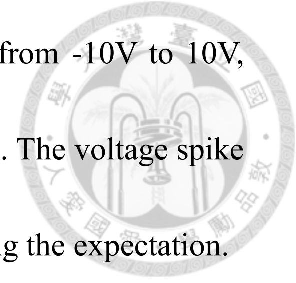

3.1, the C_{gd} has a huge variation when voltage across it varying from -10V to 10V, which results in the mismatch of the behavior before Miller plateau. The voltage spike of Fig. 5.15 and the ringing suppression of Fig. 5.16 are still meeting the expectation.

The switching loss reflects the performance of the switching transition. Thus, the switching loss estimation is crucial to the design of the circuit. Table 5.10 to 5.13 shows the switching loss experimental result compared with the simulation result on SIMPLIS of the testing boards of EPC2014C. Fig. 5.15 and 5.16 shows the switching loss experimental result of board B when gate external resistance is equal to 2.8Ω. By integrating the product of $V_{ds}(t)$ and $I_{ds}(t)$, the turn-on loss of switching transition is obtained.

Board A	**5V/1A**	**Experimental**	**10V/2A**	**Experimental**
R_{g_ext}=0Ω	8.8nJ	10nJ	42nJ	55nJ
R_{g_ext}=1.6Ω	10.7nJ	11.8nJ	47.3nJ	68nJ

Table 5.10 Switching loss table of board A

Board B	**5V/1A**	**Experimental**	**10V/2A**	**Experimental**
R_{g_ext}=1.7Ω	9.1nJ	11nJ	47.3nJ	47nJ
R_{g_ext}=2.8Ω	10.6nJ	13.6nJ	53.4nJ	66nJ
R_{g_ext}=5.4Ω	13nJ	15.2nJ	62.8nJ	71nJ

Table 5.11 Switching loss table of board B

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Board C	5V/1A	Experimental	10V/2A	Experimental
R_{g_ext}=4.8Ω	6.1nJ	8.4nJ	30.3nJ	54nJ
R_{g_ext}=7.3Ω	8.6nJ	12.6nJ	46.1nJ	66nJ
R_{g_ext}=10Ω	12.3nJ	14.8nJ	67.5nJ	70nJ

Table 5.12 Switching loss table of board C

Board D	5V/1A	Experimental	10V/2A	Experimental
R_{g_ext}=0Ω	8.8nJ	6.16nJ	42nJ	25nJ

Table 5.13 Switching loss table of board D

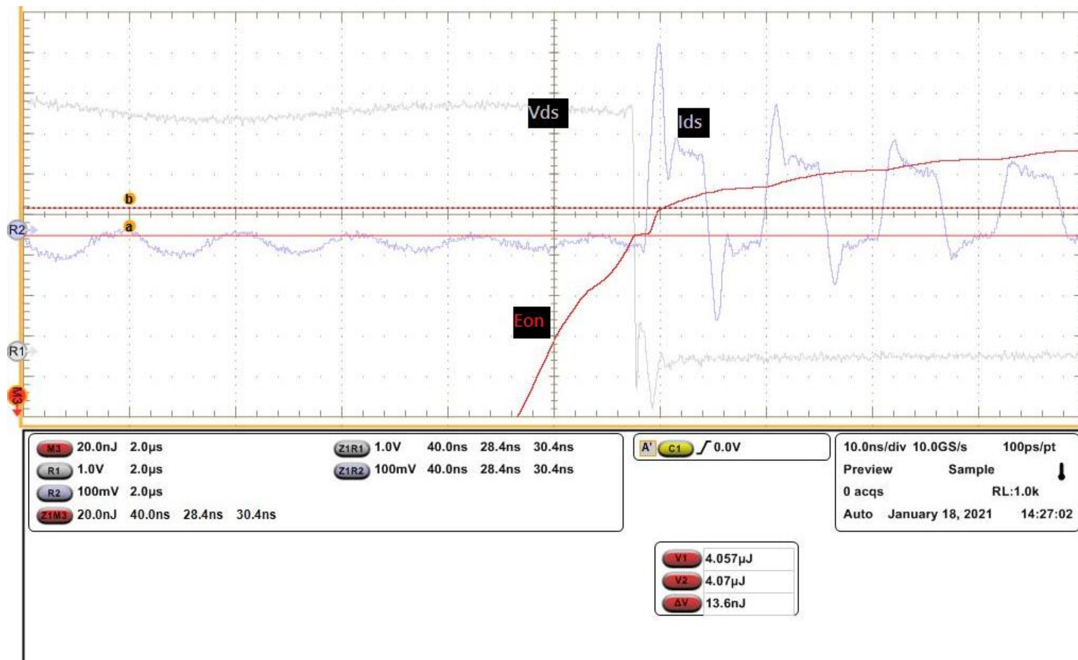

Fig. 5.17 Switching loss result when R_{g_ext}=2.8Ω and 5V/1A is applied on board B

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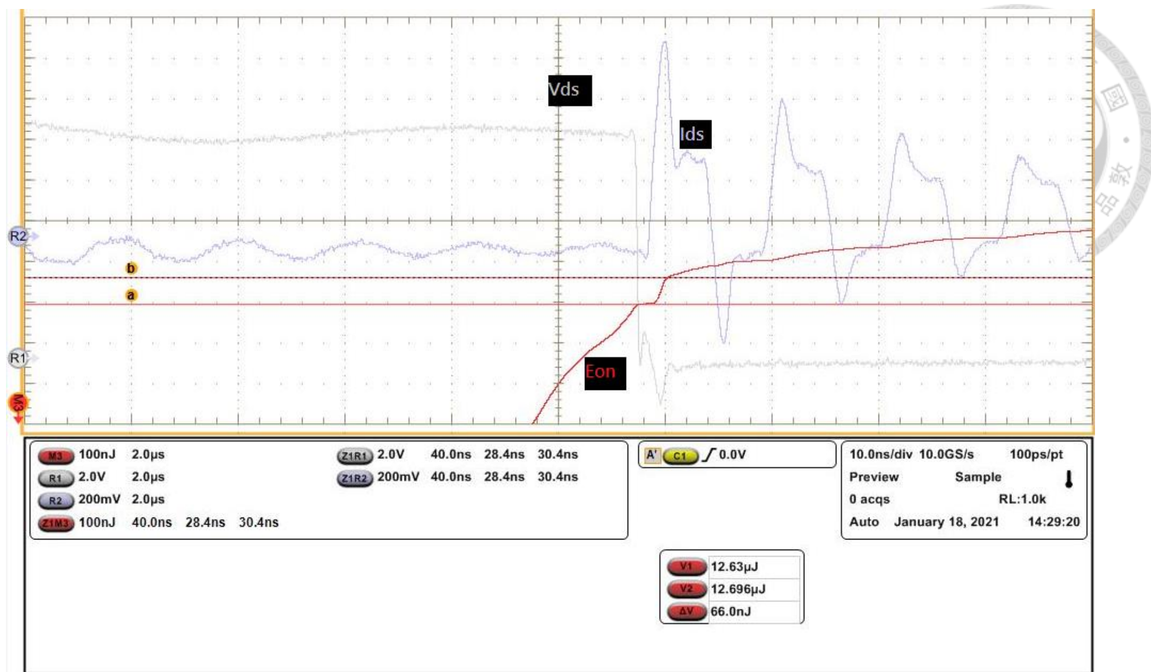

Fig. 5.18 Switching loss result when R_{g_ext}=2.8Ω and 10V/2A is applied on board B

The results of switching loss of different testing boards of EPC2014C are shown. However, there is error between simulation results and experimental results. The measurement results of switching loss are almost bigger than the experimental ones, the reasons are discussed below.

First, we apply current shunt for the measurement of current waveforms. When current flows through current shunt, there is the voltage across the shunt, which results in the extra voltage across the drain-source of the GaN transistor. Another reason is the low-frequency resonance of the power supply. The resonance causes the additional voltage on $V_{ds}(t)$ which makes the additional switching loss and also the conduction loss. Although the voltage mentioned above is not big enough to impact the overall switching behavior, it makes the switching loss larger than the theoretical values.

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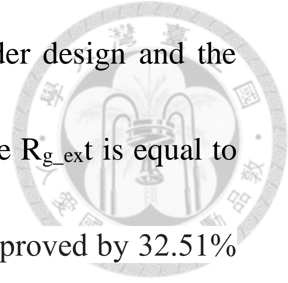

Table 5.14 compares the experimental results of second-order design and the proposed design of board B, the second-order design shows that the R_{g_ext} is equal to 5.9Ω to meet the critical-damping criteria. The switching loss is improved by 32.51% and 15.60% when 5V/1A and 10V/2A is applied by the proposed design.

	R_{g_ext}=1.7Ω	**R_{g_ext}=2.8Ω**	**R_{g_ext}=5.4Ω**	**R_{g_ext}=5.9Ω**	**Improvement**
5V/1A	11nJ	13.6nJ	15.2nJ	16.3nJ	32.51%
10V/2A	47nJ	66nJ	71nJ	78.2nJ	15.60%

Table 5.14 Comparison table of switching loss under different R_{g_ext} of board B

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Chapter 6 Conclusion and Future Works

6.1 Conclusion

In this thesis, the optimization of the gate resistance of E-mode GaN transistors has been proposed. The proposed solution focuses on the turn-on transition of E-mode GaN transistor. In order to avoid the breakdown of the gate caused by the induced voltage of parasitic inductance, the design region of the gate resistance is given and verified.

We apply double pulse test to analyze the switching behavior of switching devices. The non-ideal effect caused by parasitic inductance will impact the circuit dramatically due to the fragility of the gate of E-mode GaN devices. Thus, the equivalent circuit model based on the physical structure of E-mode GaN devices and double pulse test are built to further analyze the turn-on transition. Mathematical analysis has been given to find out the design region of gate resistance that the $V_{gs}(t)$ does not exceed the maximum value of GaN devices and also not be over-designed to make the switching loss smaller. The hardware implementation is then done to verify the proposed method. By different strategy of PCB layout, the gate resistance design differs case by case.

The measurement result shows that when gate resistance is designed within the region, the breakdown of gate will not occur and the switching loss is smaller than the second-order design ones by about 32.51%, which proves that the proposed method optimize the design of gate resistance of switching transition.

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6.2 Future Works

In this thesis, the gate resistance optimization of turn-on transition analysis has been proposed. However, there are still some works to do for this research.

First, the turn-off switching transition is another topic for the E-mode GaN devices, the equivalent circuit of turn-off transition is different. Also, the other issue introduced in section 2.4, the false-triggering, often happens at turn-off transition. To solve those problems, the further analysis is required for turn-off transition.

Second, the parasitic inductance is the main cause of the parasitic effects. If the parasitic inductance is minimized, the external resistance is possibly to be zero, the circuit performance will not be impact with the lack of gate resistance. Thus, the research of the PCB layout to minimize the parasitic inductance is another topic of this research. On the other hand, if we integrate the power GaN transistors in the integrated circuits (IC), the equivalent parasitic inductance will be extremely small when the current path is inside the IC.

The other research is replacing the resistor with other components. As we know, resistors serve as the components to dissipate the excess energy in the circuit. The gate resistance causes additional driving loss when driving current flows through. If we can replace the resistor with other passive components without sacrificing the circuit performance, the efficiency will be further improved.

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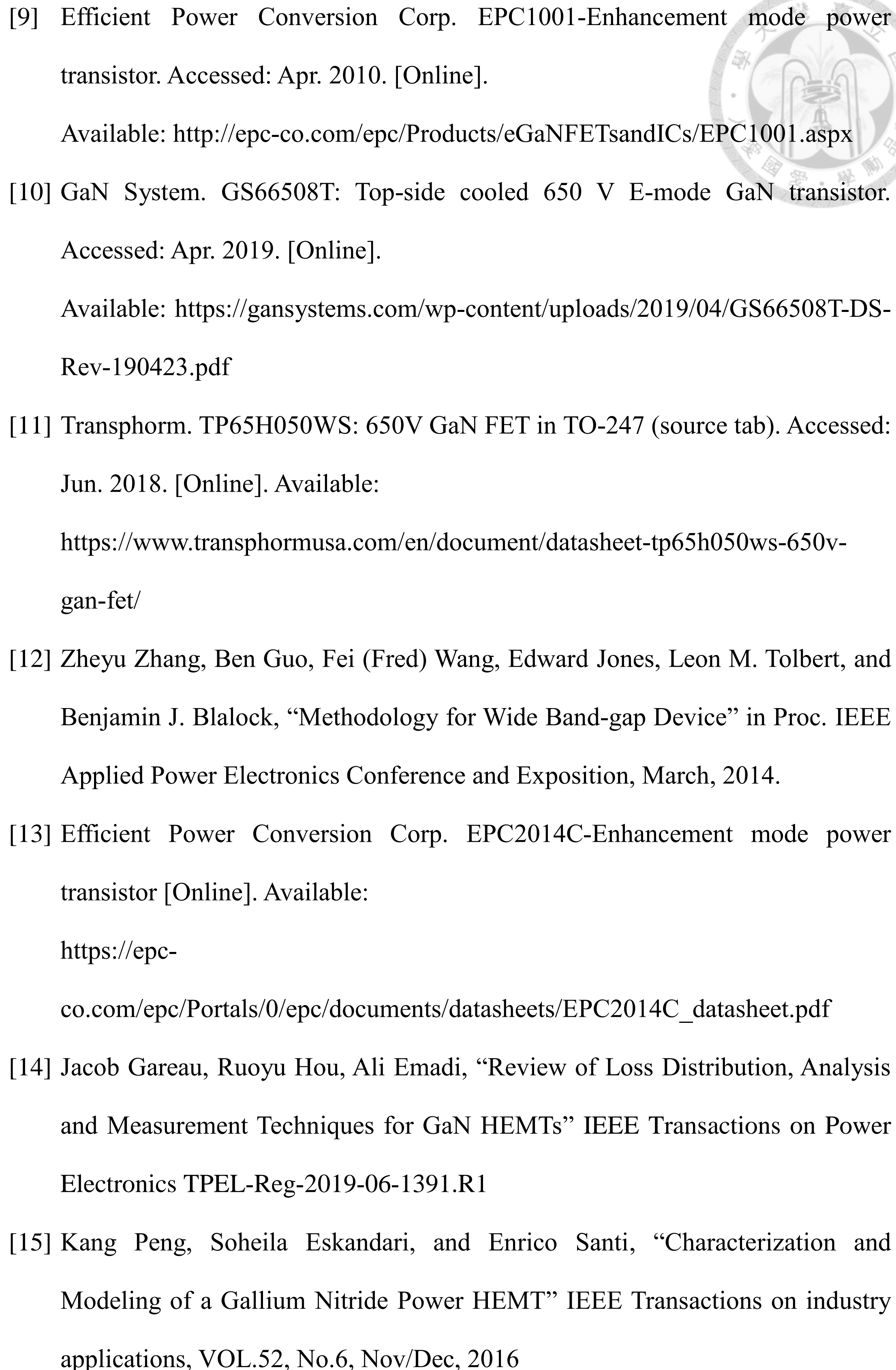

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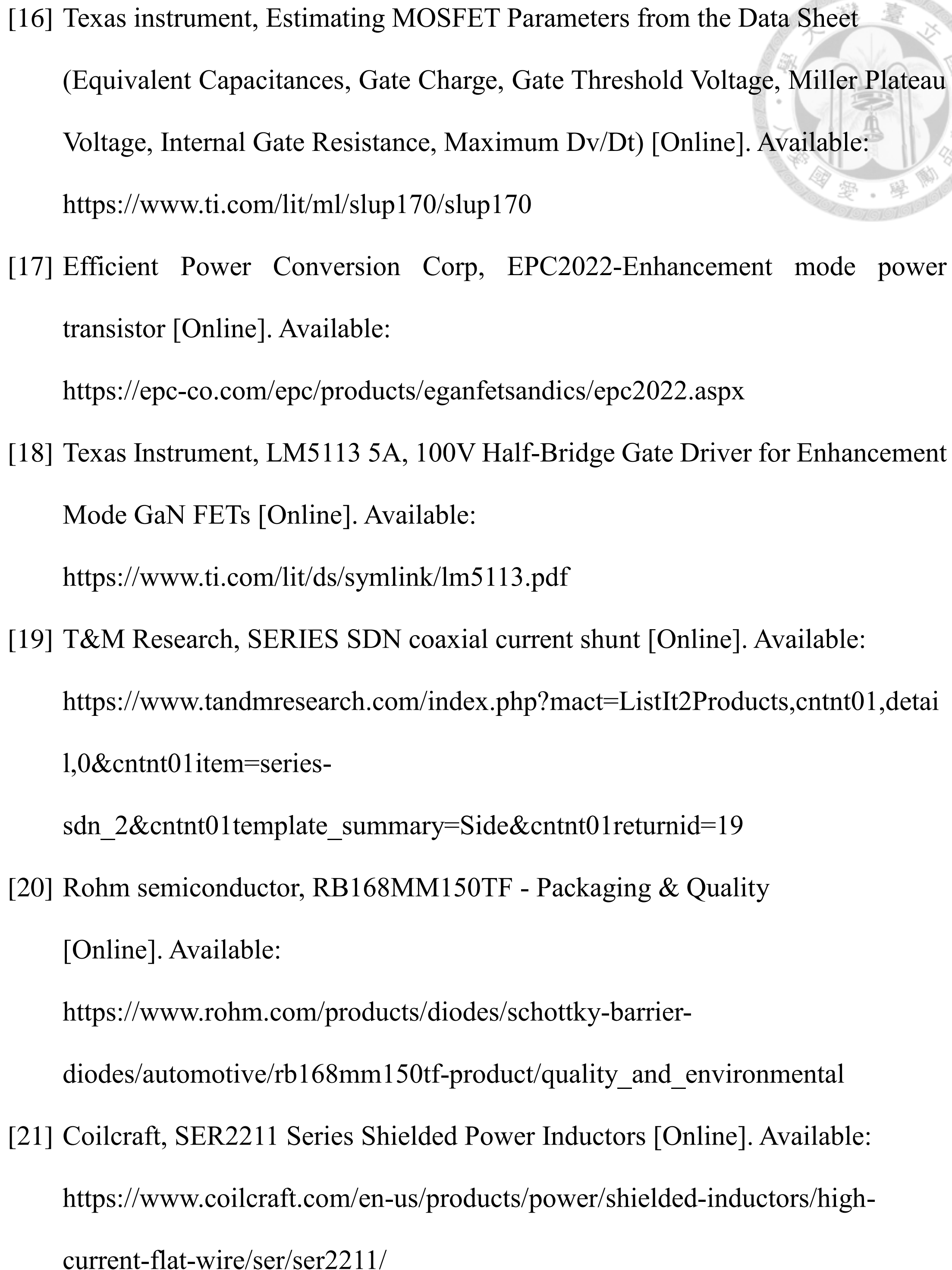

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