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Master Thesis

高能物理實驗的雙通道光學收發器的設計與分析

Design and Analysis of the Dual Channel Optical Transceivers MTx and MTRx for High Energy Physics Experiments

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高能物理實驗的雙通道光學收發器的設計與分析
Design and Analysis of the Dual Channel Optical Transceivers MTx and MTRx for High Energy Physics Experiments

本論文係李家豪君（R05543021）在國立臺灣大學物理學系、所完成之碩士學位論文，於民國 109 年 7 月 21 日承下列考試委員審查通過及口試及格，特此證明

口試委員：

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（指導教授）

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摘要

在高能物理實驗中，數據傳輸系統必須在嚴酷輻射環境，強磁場，大量的每束交叉相互作用，以及探測器前端與後端電子設備之間的距離較長的情況下運行。由於這些原因，有必要開發客製化的高速耐輻射數據收發器。本文介紹了雙通道微型光發射器（MTx），收發器（MTRx）和小封裝可插拔發射器（MTx-SFP）的設計，質量分析和老化試驗。收發器包含雷射驅動器（LOCld）和 850 nm 多模垂直共振腔面射型雷射（VCSEL）。所有模組，包括 3240 個 MTx，810 個 MTRx 和 600 個 MTx-SFP，在生產過程中均已通過 5.12 Gbps 眼圖測試，以此進行質量控制。MTx 和 MTRx 的成品率高達 4650 個模組總數的 98%。對 24 個光學收發器 (MTx)進行了 6000 小時的老化試驗並定期測試位元錯誤率和眼圖。

關鍵字: 高能物理, 光發射器, 光收發器, 光鏈路

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Abstract

In high energy physics experiments the data transmission system has to operate in a harsh radiation environment, strong magnetic fields, large number of interactions per bunch crossing, and a long distance between the on-detector front-end and the back-end electronics. For these reasons, high-speed radiation tolerance customized data transceivers must be developed. This thesis presents the design, quality analysis, and ageing tests for the dual-channel miniature optical transmitter (MTx), transceiver (MTRx), and the transmitter packaged in small form-factor pluggable format (MTx-SFP). The transceivers contain the link-on-chip laser driver (LOCld) and the multi-mode 850 nm vertical-cavity surface-emitting laser (VCSEL). All modules, including 3240 MTx, 810 MTRx and 600 MTx-SFP, have been tested for quality control during production using eye-diagram tests at 5.12 Gbps. The yield rates of MTx and MTRx were found to be as high as 98% for a total of 4650 modules. 24 transmitter modules have been monitored by testing the bit-error rate and using eye-diagram test periodically, over 6000 hours of burn-in.

Keywords: High Energy Physics, optical transmitter, optical transceiver, optical links

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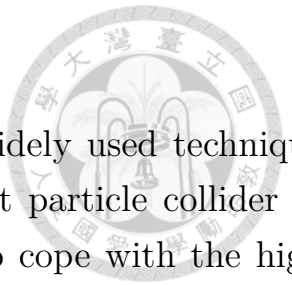
I Introduction



High-speed data transmission by optical links, is a widely used technique in high energy physics experiments, including the biggest particle collider in the world, the Large Hadron Collider (LHC). In order to cope with the high radiation dose and strong magnetic field requirements for high-speed data communication and long distance of transmission without detector signal loss, experiments in the LHC, including ATLAS and CMS, have developed customised optical transmission devices for their upcoming upgrades. This chapter gives a brief introduction about the LHC, the ATLAS experiment, an overview of the optical link systems and the module applications in the LHC during Phase-I and Phase-II upgrades.

I.1 The Large Hadron Collider

The world's most powerful and largest particle accelerator, LHC, consists of a 27 kilometre superconducting magnet-ring and accelerating structures which boost the energy of the particles and is located in a tunnel 100 metres underground at the European Organization for Nuclear Research (CERN), as shown in Fig. I.1 [1]. The LHC pushes protons or ions to close to the speed of light in two separate ultrahigh vacuum beam pipes travelling in opposite directions before they are made to collide.

There are four particle detectors (ATLAS, CMS, ALICE and LHCb) built around four points of collision and seven distinct experiments (ALICE, ATLAS, CMS, LHCb, LHCf, TOTEM and MoEDAL) in total at the LHC using their detectors to analyse the data from the collisions of particles.

The main goal of the LHC is to answer some questions beyond the Standard Model, for example, what is the origin of mass, search for evidence of supersymmetry, what are dark energy and dark matter, why is there more matter than antimatter in the universe, how does the quark-gluon plasma lead to the

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particles which constitute the matter of our universe···etc.

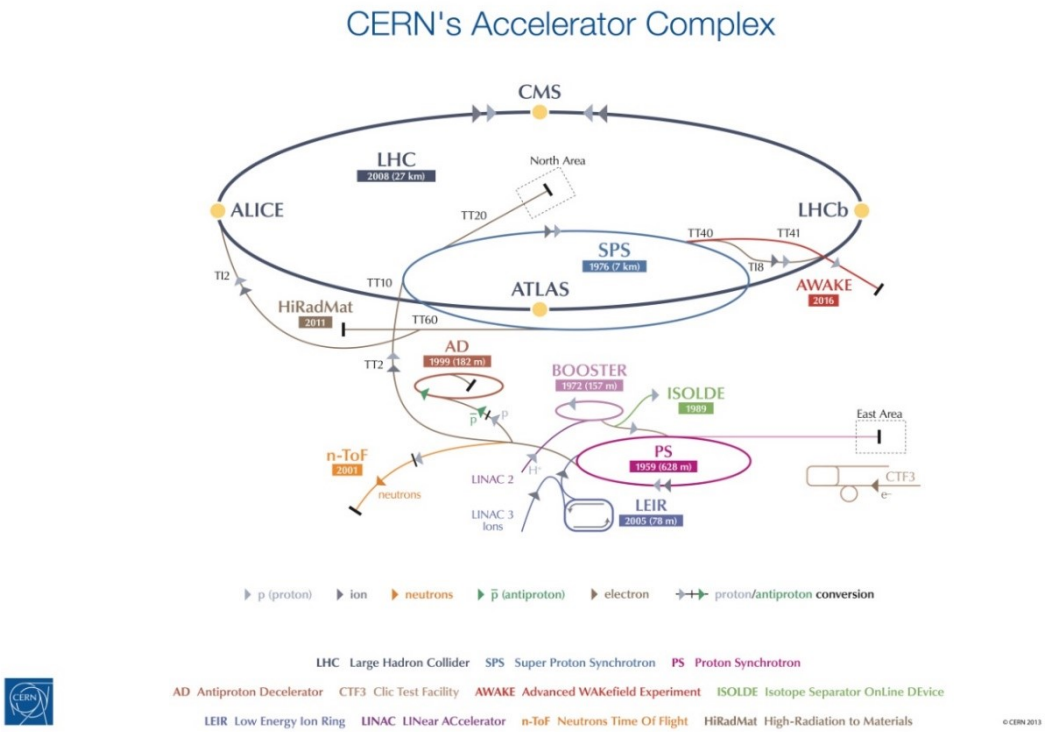

Figure I.1: The Large Hadron Collider in the CERN accelerator complex.

I.2 A Toroidal LHC Apparatus

The Toroidal LHC Apparatus (ATLAS) is the largest volume and one of the two general-purpose particle detectors in the LHC, as shown in Fig. I.2 [2]. ATLAS is in a shape of cylinder with 46 metres in length, 25 metres in diameter and weight of 7000 tonnes. The goal of the ATLAS is similar to the CMS, such as the search for the Higgs boson, and find evidence for Physics beyond the Standard Model.

The ATLAS detector is composed of the Inner Detector, the Calorimeter, the Muon Spectrometer and the Magnet System. The Inner Detector has three main components, the Pixel Detector, the Semiconductor Tracker (SCT) and the Transition Radiation Tracker (TRT), measuring the direction, momentum and charge of particles after the collisions. The Calorimeter has two main com-

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ponents, the Liquid Argon (LAr) Calorimeter and the Tile Hadronic Calorimeter, stopping electrons, photons, hadrons and measuring their energy deposits in the detector. The Muon Spectrometer consists of the Thin Gap Chambers, the Resistive Plate Chambers, the Monitored Drift Tubes, and the Cathode Strip Chambers. The Magnet System consists of the Central Solenoid Magnet, the Barrel Toroid, and the End-cap Toroid, helping ATLAS to bend the tracks of charged particles.

By using a specialised two-level online event selection system, Level-1 hardware trigger and a High-Level Trigger, there are approximately 1000 events from 1.7 billion proton-proton collisions per second, passed on to a data storage system for physics analysis.

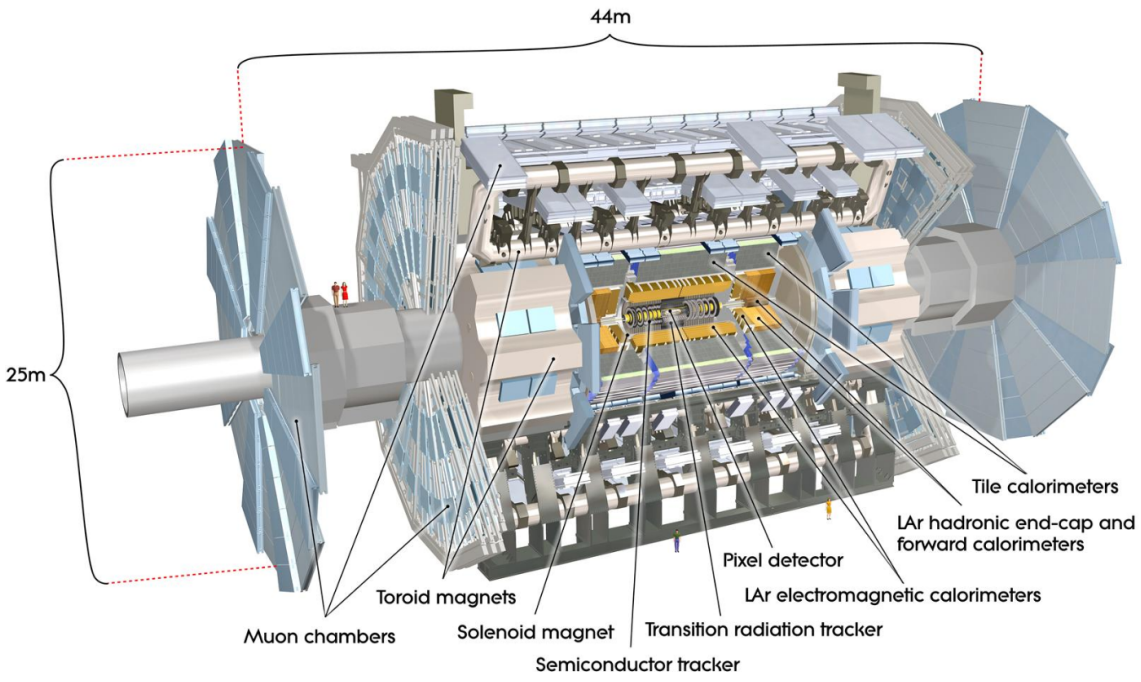

Figure I.2: The structure of the ATLAS detector.

I.2.1 The ATLAS phase-I upgrade

The ATLAS Liquid Argon (LAr) Calorimeter Phase-I upgrade will enhance the trigger energy resolution and efficiency for the selection of electrons, photons, τ leptons, jets, and missing transverse momentum, during the second-

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long shutdown of the LHC in the year 2018 [3]. The upgrade provides higher-granularity, higher-resolution, longitudinal shower information to the Level-1 hardware trigger and will enhance the ability for the measurement of the Higgs boson properties and the search for Physics beyond the Standard Model.

I.3 An overview of optical transceivers and data transmission links at the LHC

In high energy physics detectors, most of the communication systems are based on customized optical links, in order to meet the harsh radiation environment, the strong magnetic field, the need of high-speed data transmission, and the long distance between the on-detector front-end and the back-end electronics. There are three types of data typically carried by optical links. The first type is the timing, trigger and clock information from the back-ends to the front-ends. The second type is the slow-control data passed in both directions between the front-ends and the back-ends. And the third type is the trigger data and high-volume, low-latency DAQ from front-ends to back-ends [4].

The GigaBit Transceiver (GBT) chipset and the Versatile Link (VL) were developed for the Phase-I upgrades at the LHC, providing a data rate of 4.8 Gbps [5]. They aim at producing bi-directional optical links which can cope with high radiation doses, increase the data rate and reduce the power dissipation. Half of the link is located in a radiation environment, which requires custom, radiation hard electronics. The other half of the link is located in a radiation free environment, thus Commercial Off-The-Shelf (COTS) electronics can be used. The GBT chipset merges the timing and trigger signals, DAQ data, and slow controls into one single optical link. The schematic diagram of the GBT chipset is shown in Fig. I.3. There are three custom ASICs in the on-detector part of the GBT chipset. The GBTIA is a transimpedance amplifier, receiving serial input data from the photodiode (PD). The GBLD is a laser driver, modulating serial data from a laser. The GBTX is a transceiver, communicating with the detector front-end electronics [6].

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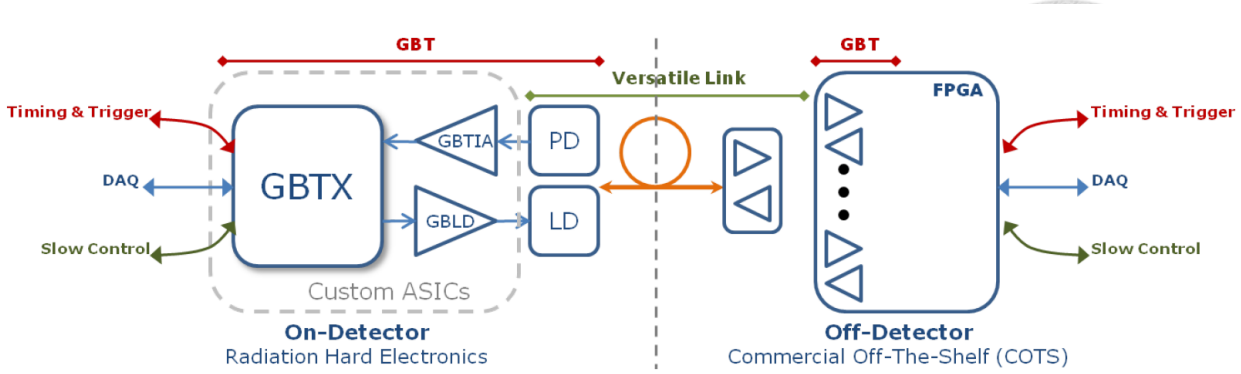

Figure I.3: Radiation hard bi-directional optical links architecture from on-detector front-end to off-detector back-end.

The transceiver ASIC in the Phase-II upgrades is the low power GBT (ipGBT), providing higher bandwidth and radiation tolerance level. The Versatile Link Plus (VL+) can operate at a data rate up to 2.5 Gbps in the downstream to the detector and 10 Gbps in the upstream off the detector. The characteristics of the transceiver chipset and the optical transceivers are shown in Tables I.1 and I.2 respectively [4].

heightEra	Component	Line speed	Capacity
Phase-1	GBT	4.8 Gb/s	DAQ: 2.56 Gb/s TTC:640 Mb/s Slow-control: 160 Mb/s
Phase-2	lpGBT	Down: 2.56 Gb/s	User: 1.28 Gb/s ASIC control: 80 Mb/s External control: 80 Mb/s
		5.12/10.24 Gb/s	DAQ:3.84(4.48) Gb/s with FEC12 (FEC5) ASIC control: 80 Mb/s External control: 80 Mb/s
			DAQ: 7.68(8.96) Gb/s with FEC12(FEC5) ASIC control: 80 Mb/s External control: 80 Mb/s

Table I.1: Characteristics of GBT and lpGBT developed for the Phase-I and Phase-II upgrades at the LHC.

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Era	Component	Max. link speed	Details
Phase-1	Versatile Link (VL)	5 Gb/s	Single-mode or multi-mode Package: Tx+Rx or 2Tx
Phase-2	Versatile Link Plus (VL+)	Rx:2.5 Gb/s Tx: 10 Gb/s	Multi-mode (850 nm) Package: 4Tx+1Rx

Table I.2: Characteristics of VL and VL+ developed for the Phase-I and Phase-II upgrades at the LHC.

I.4 Module applications of MTx and MTRx at the LHC

The miniature optical transmitter (MTx) and transceiver (MTRx) modules are both designed for the LAr phase-I upgrade. These two types of modules will be mounted on the LAr trigger Digitizer Boards (LTDBs) as data links and control links. MTx-SFP modules will be mounted on the trigger router boards in the forward muon New Small Wheel detector (NSW). The required transmission speed is 5.12 Gbps and receiving speed is 4.8 Gbps in the ATLAS phase-I upgrade [7].

The LTDBs are mounted in the Front-End crates for offering high-precision high-granularity information to the upgraded trigger processors, Feature Extractors (FEXs). A block diagram of the upgraded LAr trigger readout system is shown in Fig. I.4. Signals generated by the linear mixer in the Front-End Board are transmitted by the base plane to the LTDBs for digitization. The New Layer Sum Boards (LSB) and the base plane gives the LTDBs the capability to digitize information in the foremost and central layers of the EM calorimeters. The digitized information is converted to calibrated energies by the LAr Digital Processing System (LDPS). In addition, the LTDBs reproduce analogue sum and transmit them back to the Tower Builder Board (TBB) to maintain the current analogue trigger system working normally [3].

There are two signal transmission paths in the digital part of the LTDB, the data link and the TTC (Timing, Trigger and Control signals) link, as shown in Fig. I.5. Analogue super cell signals are first digitized by the ADC, after reorganized and serialized by LOCx2, the digital signals will be transmitted

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by the optical transmitter, MTx, through optical fibres. TTC links are used to transmit clock, slow control and monitoring signals. The GBTx and the GigaBit slow control adapter (GBT-SCA) are used to give clock and slow control signals to the LTDB, respectively. The VTRx is an optical transceiver developed by CERN [3].

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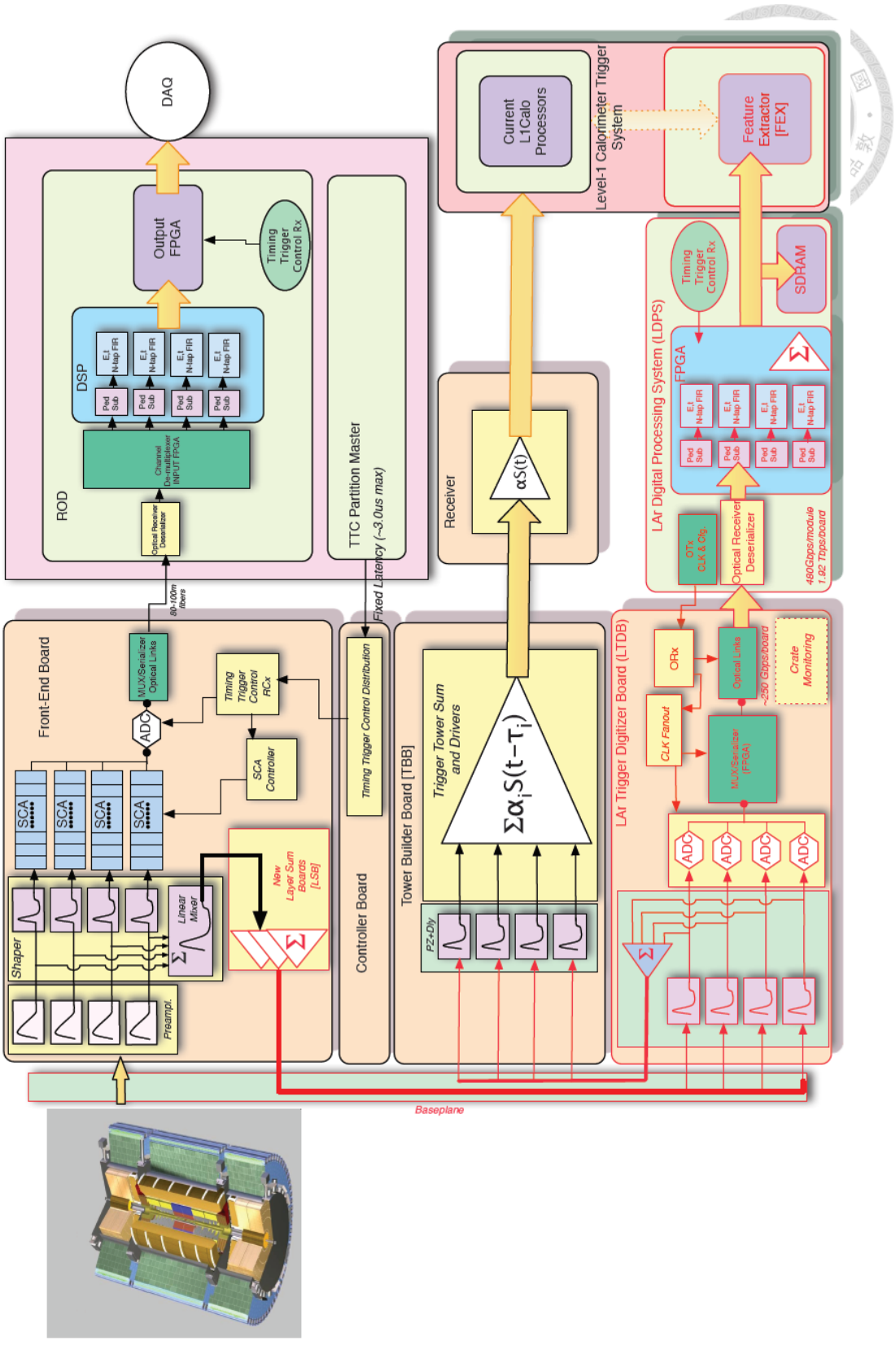

Figure I.4: A block diagram of the LAr trigger readout system in ATLAS phase-I upgrade.

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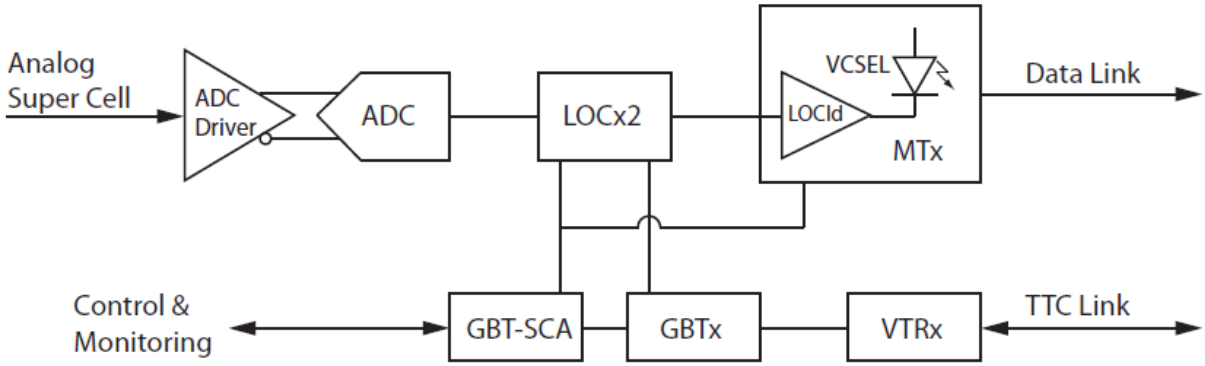

Figure I.5: Data links and TTC links in the LTDBs.

I.5 Scope and delimitations of the thesis

In the following chapters, information about the design, quality assurance and aging test of the miniature optical transmitter (MTx), transceiver (MTRx) and the MTx small form-factor pluggable format (MTx-SFP) will be given. Chapter 2 provides basic operational concepts for the electronic components that used in the modules, including Vertical-Cavity Surface-Emitting Lasers (VCSELs), Inter-Integrated Circuit Bus (I^2 C bus), Link-On-Chip laser driver (LOCld2) chips, Transmitter Optical Sub Assembly (TOSA), Receiver Optical Sub Assembly (ROSA), Transimpedance Amplifier (TIA) and optical fibres. Chapter 3 presents the production process of the modules and the definition of eye diagram parameters. Chapter 4 gives the quality assurance procedure for the modules and the analysis results for the data measured in the quality assurance tests. Chapter 5 discusses the procedure and analysis of burn-in test for the modules. Chapter 7 gives a conclusion for this thesis.

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II Optical electronic components

Due to the expected maximum instantaneous luminosity in the HL-LHC $L = 7.5 \times 10^{34} cm^{-2} s^{-1}$ and a total expected integrated luminosity of $4000 fb^{-1}$ [8], the large number of interactions per bunch crossing will be a big challenge for the current ATLAS trigger system. The corresponding radiation dose will exceed the original design specifications of the radiation tolerance for certain frond-end electronics. The simulated radiation maps for the displacement damage, the total ionizing dose and the total fluence of hadrons in the ATLAS detectors for over 10 years of operation at the HL-LHC are shown in Figures II.1, II.2 and II.3 respectively [9] [10]. These are the main reasons for the upgrade of the ATLAS trigger system.

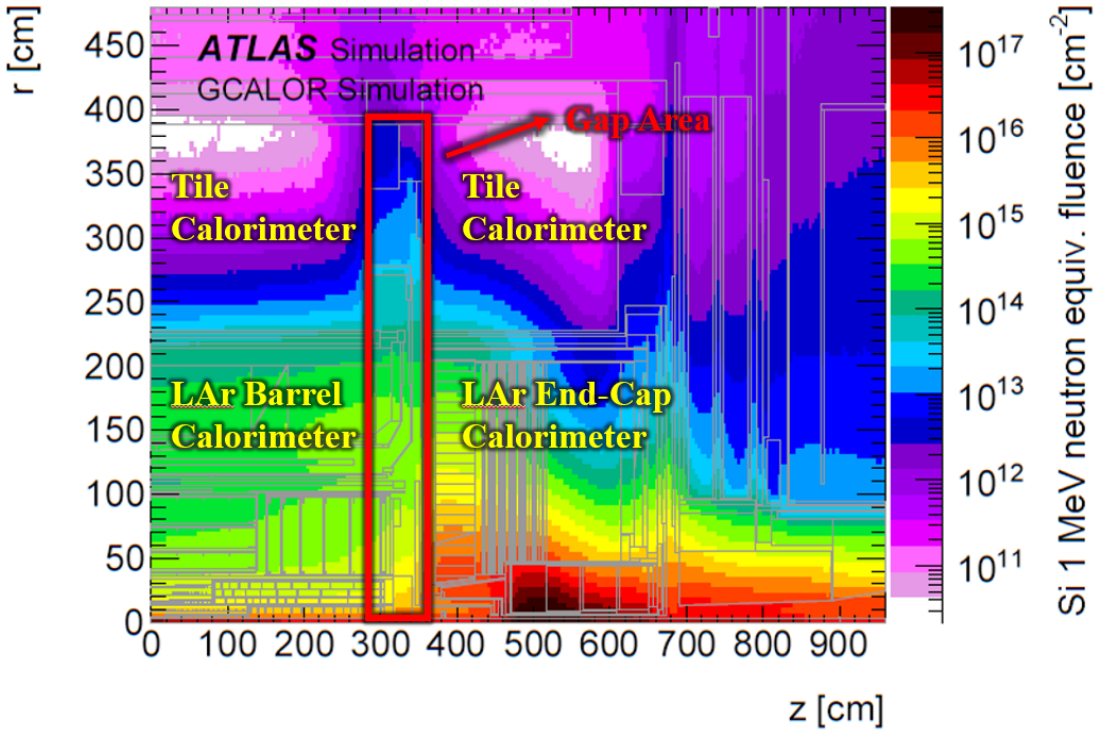

Figure II.1: Displacement damage in silicon for a total integrated luminosity of $4000 fb^{-1}$.

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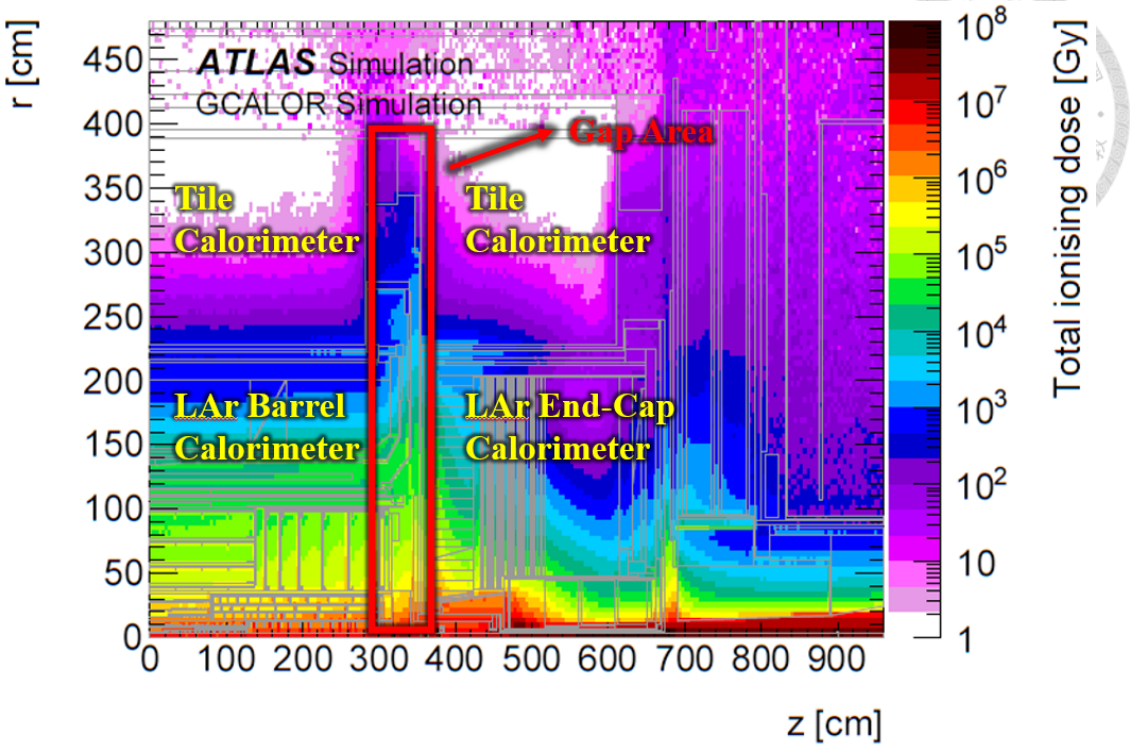

Figure II.2: Total ionizing dose for a total integrated luminosity of $4000 fb^{-1}$.

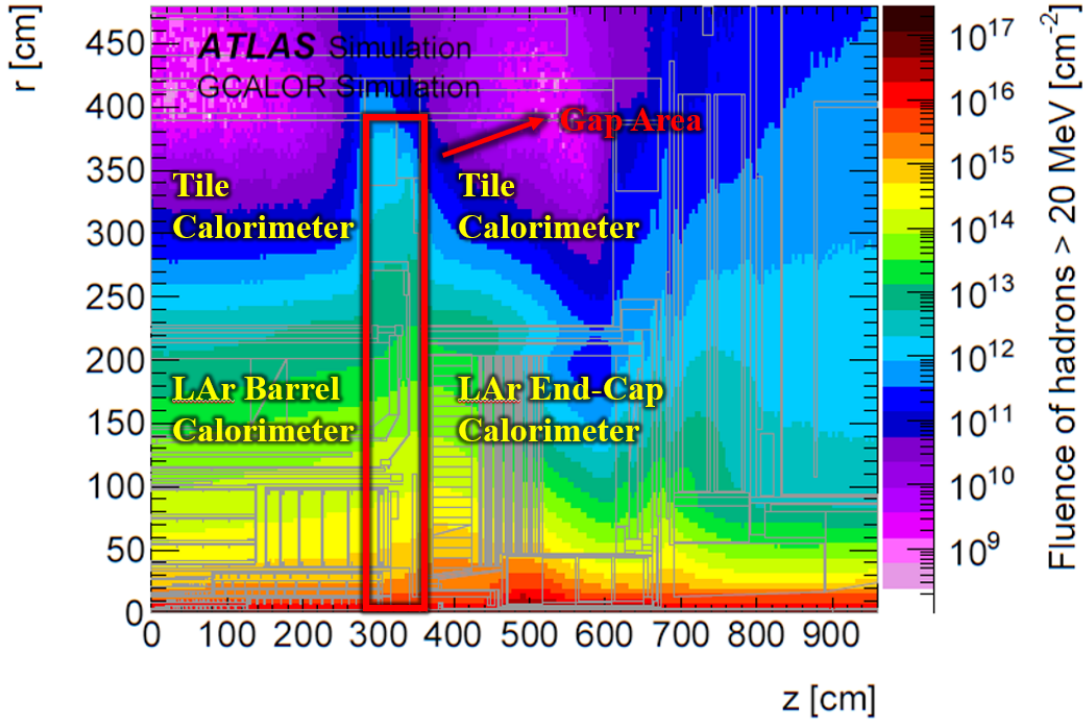

Figure II.3: Total fluence of hadrons for a total integrated luminosity of $4000 fb^{-1}$.

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Since the frond-end readout electronics of the ATLAS LAr calorimeter are mounted directly on the outer face of the end cap cryostats and the gap between the barrel and endcap calorimeters (see Fig. II.1), these on-detector electronics have to be radiation tolerant. The requirements of the radiation tolerance for the LAr frond-end electronics in the HL-LHC are given in Table II.1 [9], including the Total Ionizing Dose (TID), the Non-Ionizing Energy Loss (NIEL), the Single Event Effects (SEE). The corresponding safety factors for the uncertainty of simulation are given in brackets. The Low Voltage Power Supply (LVPS) is a power supply for the frond-end electronics, including the LTDBs [3]. The PP2 (Patch Panel 2) locations are inside the toroid of the detector. The fingers of the Tile calorimeter are located on the outer girder of the calorimeter. HEC is the hadronic endcap in the LAr calorimeter system (see Fig. I.2).

	TID [kGY]	NIEL [n_{eq}/cm^2]	SEE [h/cm^2]
ASIC	2.26 (2.25)	4.9×10^{13} (2)	7.7×10^{12} (2)
COTS (multiple lots)	30.2 (30)	19.6×10^{13} (8)	3.1×10^{13} (8)
COTS(single-lot)	7.5 (7.5)	4.9×10^{13} (2)	7.7×10^{12} (2)
LVPS between TileCal fingers (barrel)	6.0 (30)	4.4×10^{13} (8)	8.0×10^{12} (8)
LVPS ar PP2 (barrel)	0.39 (30)	2.4×10^{12} (8)	3.4×10^{11} (8)
LVPS between TileCal fingers (endcap)	4.26 (30)	9.8×10^{12} (8)	1.5×10^{12} (8)
HEC LVPS	0.32 (2.25)	2.4×10^{12} (2)	3.8×10^{11} (2)

Table II.1: Requirements of the radiation tolerance for the LAr front-end electronics in the HL-LHC.

The following sections introduce certain optical electronic components which are used in optical transmitter (MTx) and transceiver (MTRx) for the transmission of trigger signals in the ATLAS LAr calorimeters and the forward muon spectrometer.

II.1 Basic structure of Vertical-Cavity Surface-Emitting Lasers

The Vertical-Cavity Surface-Emitting Lasers (VCSELs) are used to change electrical signals to optical signal in all detectors for the readout and control

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systems in ATLAS. The VCSELs used in the MTx, MTRx and MTx-SFP modules are 10 Gbps 850 nm GaAs-based oxide-confined VCSELs. These VCSELs have to meet the requirements of radiation tolerance for the ATLAS detector upgrade, including the TID, SEE and NIEL (see Table II.1) [7]. The damage due to NIEL effect to the VCSELs, has been studied by examining the light degradation with 30 MeV and 70 MeV proton beams [11].

A VCSEL emits cylindrical light beam vertically from the top surface and is commonly used in multimode optical data links for a distance of few hundred metres. There are many advantages of using VCSELs instead of the edge Emitting Lasers (EELs), such as low cost (since VCSELs can be fabricated and tested at the wafer level. EELs, on the other hand, can only be tested in the end of the processing flow), low power consumption, low threshold current, easy fibre-coupling (because the VCSEL has cylindrical and low divergence output light beam) and capability of operating in high temperature.

The basic structure of a VCSEL is shown in Fig. II.4 [12]. The electrical current is injected from the top layer. The active layer is in the middle of two distrusted Bragg reflector (DBR) mirrors, which have high reflectivity and provide optical feedback. This active region usually formed by multiple quantum wells (QWs). The QWs generate photons which bounce up and down between the top and the bottom DBR mirror. In an oxide-confined VCSEL, an oxide layer is grown between an active layer and a DBR mirror. This oxide aperture can help to reshape the VCSEL lights into a more circular beam. In high-speed VCSELs, the design of the size of oxide apertures is smaller. Although a smaller size of aperture can also cause the VCSEL to be more sensitive to the working environment, such as humidity and temperature [11].

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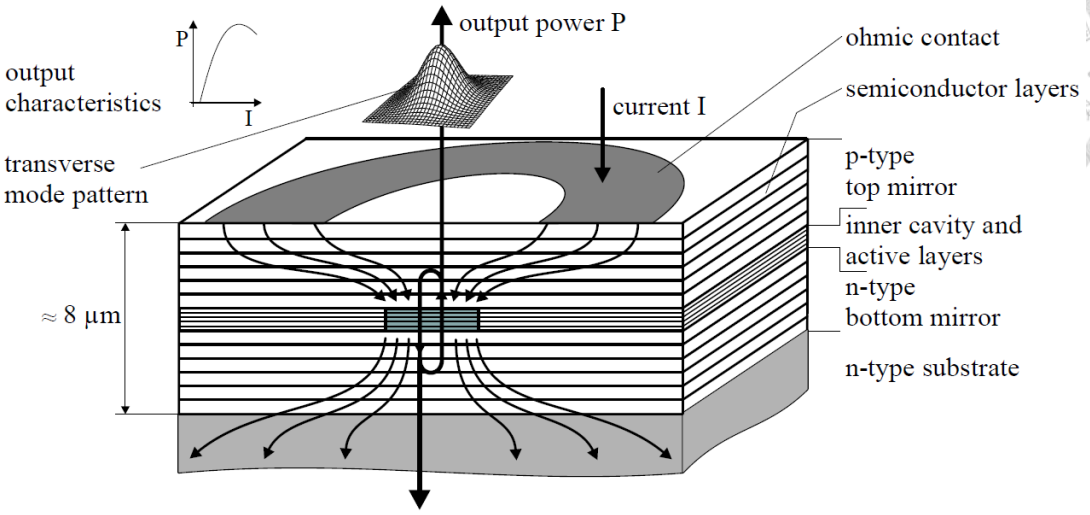

Figure II.4: Basic structure of a VCSEL.

II.2 Protocol of the Inter-Integrated Circuit Bus

The Inter-Integrated Circuit Bus (I^2C bus) is used for the communication of integrated circuit devices with relatively small amount of data and low speed in a short distance, usually between a microprocessor and a peripheral device such as data converter, sensor, memory chip or communication device. A I^2C bus has two bidirectional open collector or open drain lines, one of them is a serial data line (SDA), and the other one is a serial clock line (SCL). The data transmission speed of the I^2C bus is 100 kbit/s in the Standard-mode (Sm), 400 kbit/s in the Fast-mode (Fm), 1 Mbit/s in the Fast-mode Plus (Fm+), 3.4 Mbit/s in the High-speed mode (Hs-mode) and 5 Mbit/s in Ultra Fast-mode (UFm) [13]. All modes can transfer serial data in both directions of the lines except for the Ultra Fast-mode, which can only transfer serial data in one direction.

Every device which connects to the I^2C can be a transmitter or receiver, master or slave, and all devices have a unique address. The word master in I^2C means it is the device which produces clock signals, and initiates or terminates a transfer. The word slave in I^2C represents the device which is addressed by a master. There can be multiple masters connected to the I^2C and when more

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than one masters try to control the I^2C at the same time, the bus will use an arbitration procedure to make sure only one master is permitted to do so.

In the SDA line, the data can be changed only when the clock signal in the SCL line shows LOW (logical level "0" , usually is set as 30% of V_{DD}), as shown in the Fig. II.5 [13]. If the I^2C bus is free, the SDA and SCL will all show HIGH (logical level "1" , usually is set as 70% of V_{DD}), which is because both lines have pull up resistors to give them a default state.

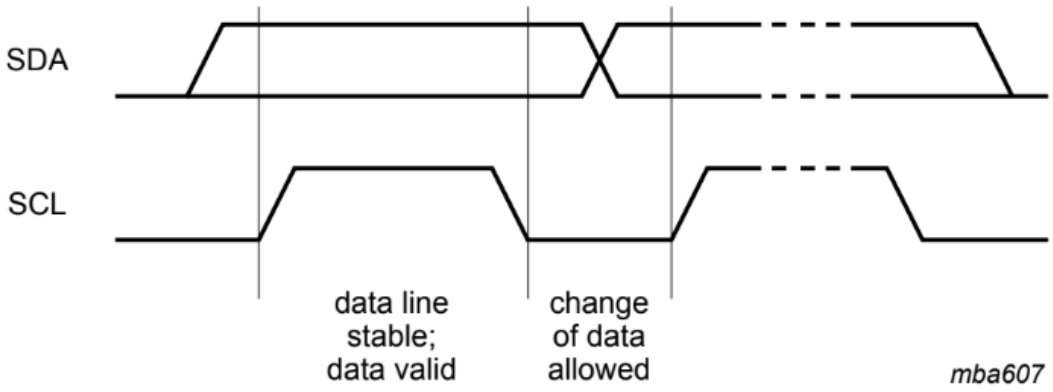

Figure II.5: Data transfer logic. Data on the SDA line can only be changed while the SCL line is LOW.

To start a transaction, the master will send a START condition by pulling the SDA line LOW while the SCL line is HIGH. The first 7 bits sent after the START condition is a slave address and the bit sent right after this address is a data direction bit (R/W). A "0" in this data direction bit means the master wants to send the data to the slave and a "1" means the master wants to read the data from the slave. Each data byte send on the SDA line must be 8 bits long followed by an acknowledge bit which tells the transmitter that the byte has been received. The first bit to be sent in a byte is the Most Significant Bit (MSB). A slave can hold the SCL line LOW to pause the transaction if there is something else it needs to perform first before transfer next byte, for example, it may need more time to store the received byte.

An Acknowledge signal will be generated when the SDA line is being pulled LOW by the receiver and stay in this state while the acknowledge clock pulse

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sent by the master is in the HIGH period, as shown in Fig. II.6 [13]. If the SDA stays HIGH during this clock pulse, a Not Acknowledge signal will be generated. In this case, the master can either terminate this transmission by sending a STOP condition or a repeated START (Sr) condition to start a new one.

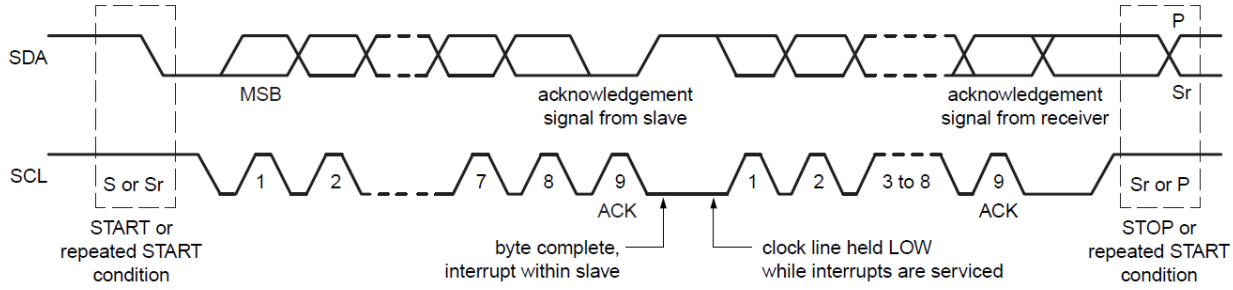

Figure II.6: Data transfer from START to STOP condition.

II.3 Pin map and Block diagram of link-on-chip laser driver

The link-on-chip laser driver (LOCld2) is a custom-designed high-speed dual-channel laser driver ASIC for two VCSELs. It is fabricated in a commercial 0.25 µm Silicon-on-Sapphire (SOS) Complementary Metal-Oxide-Semiconductor (CMOS) process with a two-wire serial I^2C interface for digital control of the peaking voltage, modulation current and bias current of the VCSEL light output. SOS is one of the silicon on insulator type of the CMOS technology to produce IC, which grows a thin silicon layer on the sapphire ($Al_2\ O_3$) substrate and has high radiation tolerance (due to the sapphire-based substrate), high frequency performance, low power consumption and low crosstalk [14].

The dimensions of the LOCld2 is 6 mm in width, 6 mm in length and 0.9 mm in height. The LOCld2 is capable of operating in 8 Gbps per channel and is assembled on a MTX module in QFN-40 (Quad Flat No-lead) format which is a package technology to connect the integrated circuits (ICs) to the printed circuit boards (PCBs) surface without drilling holes on the PCB to insert leads [15]. The LOCld2 laser driver used in a MTx module is shown in

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Fig. II.7. The pin map of the LOCld2 is listed in Table II.2 (this map is made by our group member, SMU).

The radiation tolerance of LOCld2 ASICs have been examined, so that the ASICs can meet the requirements (see Table II.1) of TID and SEE for the LAr upgrade [7]. The TID and SEE effect has been examined by using X-ray source and neutron beams [11]. Modules that fail in the eye diagram tests after the exposure of radiation may be able to recover by changing the value of peaking voltage [16].

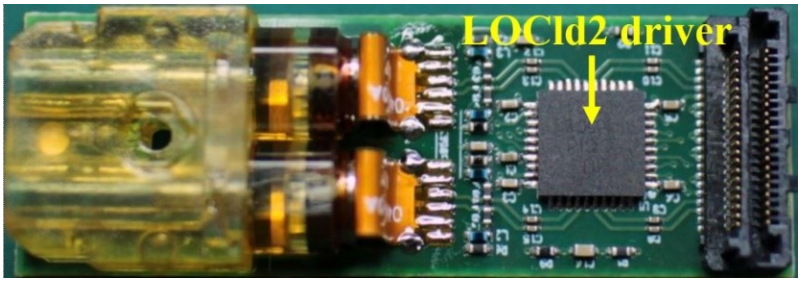

Figure II.7: Position of a LOCld2 on a MTX module.

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Pin number	Pin name	Description
1	Vcc1	3.3V power supply for channel 1
2	ExtR1	External resistor for channel 1
3	AD (0)	I^2C address AD (0)
4	AD (1)	I^2C address AD (1)
5	AD (2)	I^2C address AD (2)
6	AD (3)	I^2C address AD (3)
7	AD (4)	I^2C address AD (4)
8	DGND	I^2C Ground
9	ExtR2	External resistor for channel 2
10	Vcc2	3.3V power supply for channel 2
11	Vcc2	
12	Vcc2	
13	gnd2	Ground for channel 2
14	vi2-	Inverted data input for channel 2
15	vi2+	Non-inverted data input for channel 2
16	gnd2	Ground for channel 2
17	vo2+	Non-inverted Modulation output for channel 2
18	vo2-	Inverted Modulation output for channel 2
19	gnd2	Ground for channel 2
20	Vdd2	2.5V power supply for channel 2
21	Vdd2	
22	Ibias2	Bias current of laser for channel 2
23	gnd2	Ground for channel 2
24	resetB	I^2C reset
25	SDA	I^2C data line
26	SCL	I^2C clock line
27	DVDD	I^2C 2.5V power supply
28	gnd1	Ground for channel 1
29	Ibias1	Bias current of laser for channel 1
30	Vdd1	2.5V power supply for channel 1
31	Vdd1	
32	gnd1	Ground for channel 1
33	vo1-	Inverted Modulation output for channel 1
34	vo1+	Non-inverted Modulation output for channel 1
35	gnd1	Ground for channel 1
36	vi1+	Non-inverted data input for channel 1
37	vi1-	Inverted data input for channel 1
38	gnd1	Ground for channel 1
39	Vcc1	3.3V power supply for channel 1
40	Vcc1	

Table II.2: Pin map and function descriptions of a LOCld2 laser driver.

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LOCld2 has two driving channels, each channel has the same layout as the other version of laser driver, LOCld1. The block diagram of LOCld2 and LOCld1 are shown in Figures II.8 and II.9 respectively [16]. The I^2C slave module in LOCld2 is shared by two driving channels and has 4 registers. There are 7-stage differential amplifiers in each channel to create higher gain for large bandwidth, the last stage of the amplifier possesses two 50 Ω pull-up resistors to create a default logic state which can avoid self-bias of the inputs. Each driving channel has 5 bits of voltage DAC to control peaking voltages, 4 bits current DAC to control bias currents and 4 bits current DAC to control modulation currents.

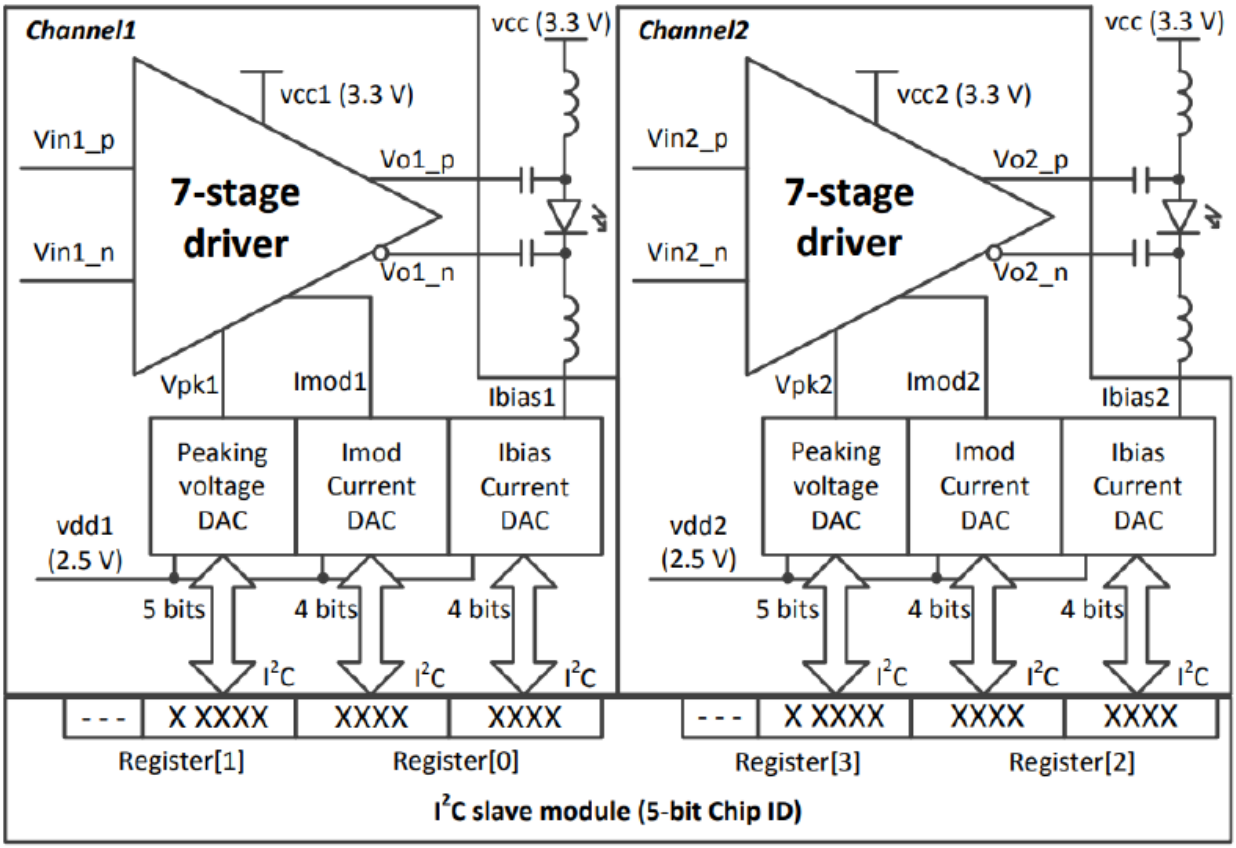

Figure II.8: Block diagram of LOCld2 laser driver which contains two driving channels shared with one I^2C slave module.

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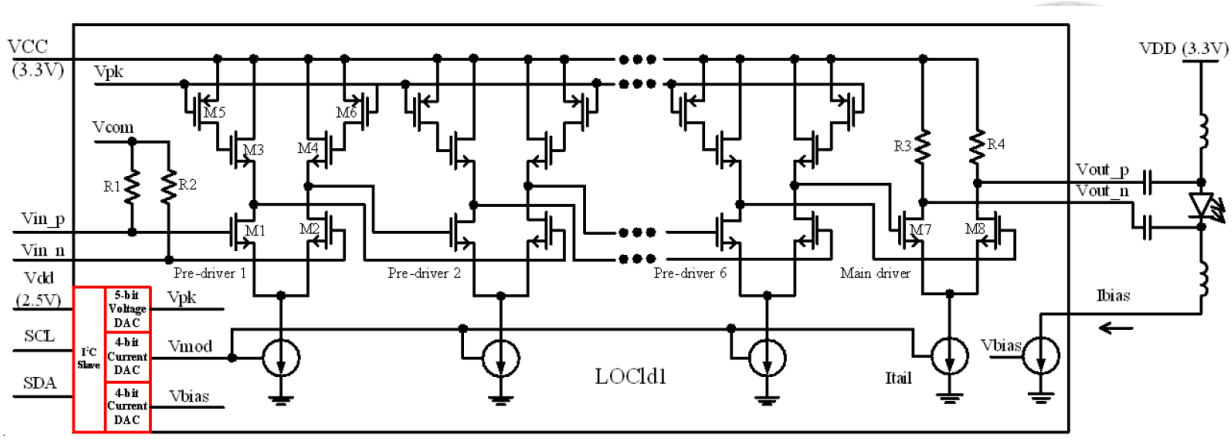

Figure II.9: Block diagram of LOCld1 which has the same electronic layout as the LOCld2 laser driver.

Before being soldered on the MTx, MTRx and MTx-SFP modules, all LOCld2 chips have been tested for reading and writing functions of I^2C and measured currents provided by 2.5 V and 3.3 V power supply voltage, using a matching socket as shown in Figures II.10 and II.11 (tested by Academia Sinica). This socket can build a connection between the pad of a LOCld2 chip and the carrier board.

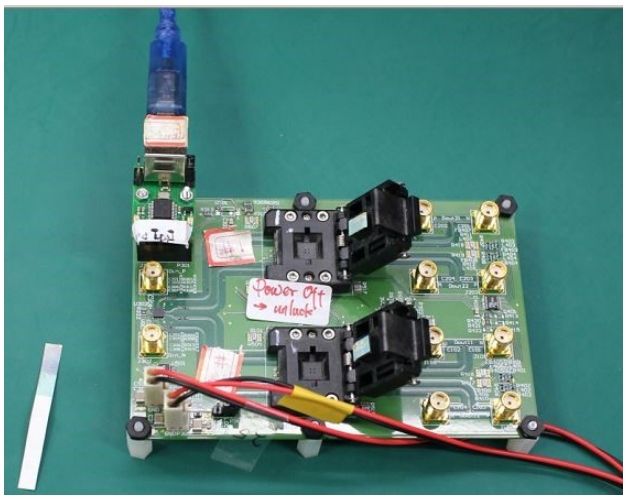

Figure II.10: Socket board used to test I^2C functions and currents of LOCld2 laser drivers.

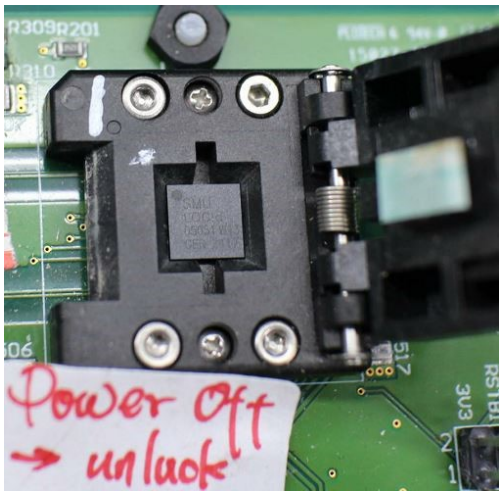

Figure II.11: Socket placed on the socket board to hold the LOCld2 laser driver.

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II.4 Structure and features of TOSAs and ROSAs

A Transmitter Optical Sub Assembly (TOSA) is used to convert electrical signals into optical signals, coupled to an optical fibre. A TOSA contains a focusing lens to help the light going through the centre of the optical fibre which is connected in the housing of the TOSA. It is completely sealed inside a TOSA to avoid effects which could damage the laser such as humidity. The TOSA also provides a path for heat dissipation to prevent a situation of overheating. Other components may as well be mounted in the TOSA, depending on the purpose of application. For instance, if a high-speed transmission is needed, some matching circuits may be added in the TOSA, such as a bias isolator or a termination. A schematic diagram is shown in Fig. II.12 to demonstrate the basic structure of a TOSA [17].

The type of TOSAs (TTF-1F59 from Truelight corp.) used in an MTx modules has been tested for radiation tolerance by using 30 and 70 MeV proton beams and demonstrated to meet the requirements of radiation tolerance for the ATLAS phase-I upgrade [11].

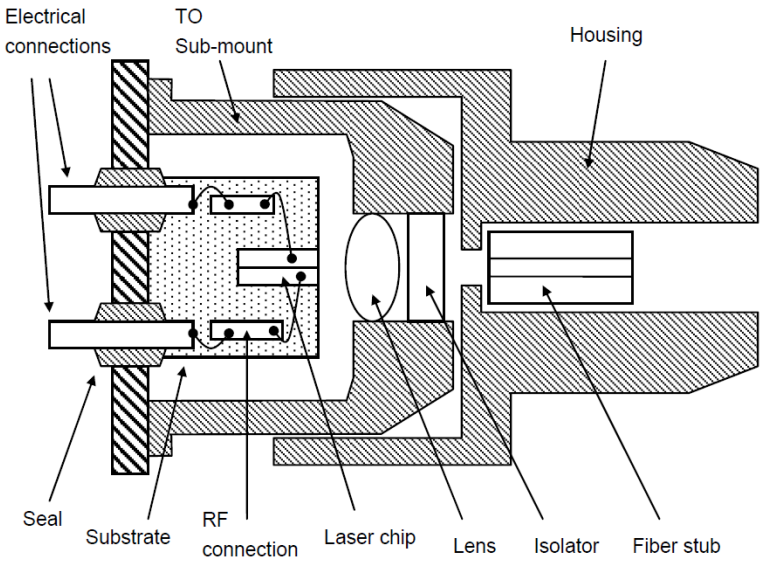

Figure II.12: The typical schematic diagram of a TOSA.

A Receiver Optical Sub Assembly (ROSA) is used to receive optical signals

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from the fibre and then reconstruct the original electrical signals. A ROSA contains a Photo Detector (PD) which converts the optical signals into electrical current signals, and a Transimpedance Amplifier (TIA) which converts the current signal into a voltage signal.

The ROSAs mounted on the MTRx modules consists GigaBit Transimpedance Amplifier (GBTIA) and a PIN diode. These ROSAs are all designed and produced by CERN in the Versitile Link project and have been tested for radiation tolerance meeting the requirements for the HL-LHC by using 60 MeV proton beams [18].

TOSAs and ROSAs (see Fig. II.13) are both assembled on the optical transceiver modules MTx and MTRx with two TOSAs on a MTx module, one TOSA and one ROSA on a MTRx module, as shown in Fig. II.14.

Figure II.13: A ROSA module.

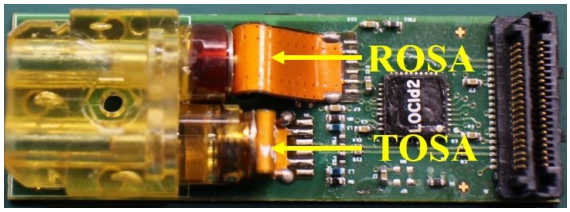

Figure II. 14: Positions of ROSA and TOSA on a MTRx module.

II.4.1 LI curve of the TOSAs used in MTx, MTRx and MTx-SFP modules

MTx modules use the TTR-1F59 type of TOSA. The optical power of this type of TOSAs has a specification range from 540 to 1020 µW while input 6 mA current. For this large deviation of optical power, optical power between 550 µW and 800 µW at 6 mA input current is chosen to be the selection criteria of TOSAs.

Fig. II.15 shows the light versus current curve (L-I curve) of 3533 TOSAs, tested separately before being assembled on MTx and MTRx modules. The wide deviation of optical powers between TOSAs with the same input current is mainly caused by alignment offset of VCSELs in TOSAs. Fig. II.16 shows

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the L-I curve from one of those TOSAs as a demonstration of a typical curve which shows good linearity between optical power and current.

The region with zero optical power values between current value 0 to 1 mA shows the optical loss caused by the reflectivity of top and bottom DBR mirrors and the light absorption of the medium between the mirrors is larger than the optical gain from the active layers of VCSELs.

The injection current when the optical gain equals to the loss is called threshold current, measured when the light starts to become measurable. After the threshold current, the slope between light and current is called quantum efficiency or slope efficiency [17]. It represents the conversion efficiency from current to light. This slope shows that first the light changes linearly with current, however as the current keeps increasing, the efficiency starts to decline.

The logical "0" level optical power is driven by the bias current. The logical "1" level optical power is driven by the bias current plus the modulation current. Since the quantum efficiency can be affected by the different operating temperature and ageing of the device, the bias current which is too close to the saturation region should not be selected, may cause considerable degradation of the optical power. On the other hand, if the bias current is set too close to the threshold current, the laser will be affected by spontaneous emission [17].

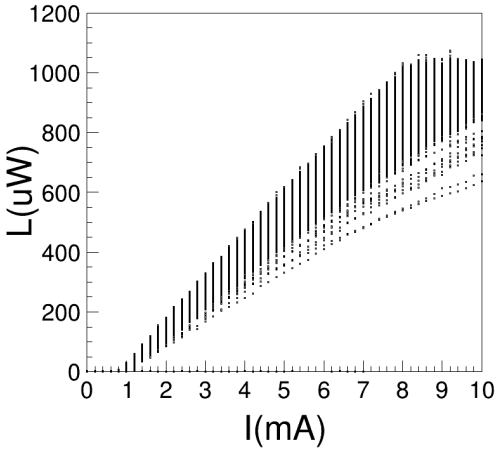

Figure II.15: LI curve of 3533 TOSAs with a threshold current around 1 mA.

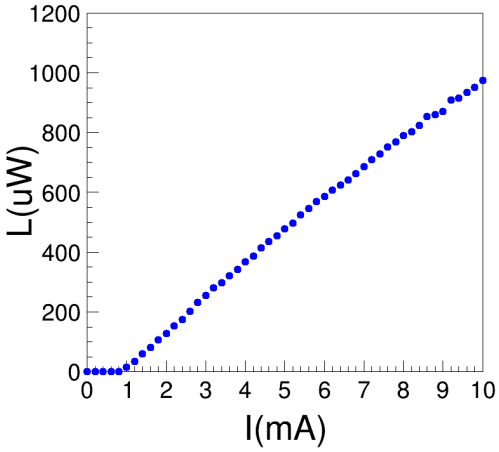

Figure II.16: LI curve of one of the 3533 TOSAs.

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II.4.2 Experiments for studying the features of TOSA optical spectra

Fig. II.17 shows an experiment to obtain a one dimensional optical spectrum of TOSA (TTF-1F59-427) light output in different angles. The distance between the TOSA and the photodetector is 41.2 mm to produce the far-field angle. During the experiment, the position of TOSA is fixed while the photodetector is moved parallel to the carrier of the TOSA by a step motor. A PDA-750 photodiode transimpedance amplifier is connected to the photodetector in order to measure the photocurrent generated by the detector. A piece of foil is pasted on the photodetector with a small window allowing light from the TOSA to pass through.

The experiment has tested the TOSA with different input currents, 4 mA, 6 mA and 8 mA in room conditions (temperature around 25℃ and humidity level between 70 and 80 %), as shown in Fig. II.18. The majority of optical power is detected to be around the centre of the TOSA light beam. The optical spectrum becomes wider with larger input currents, which shows that if the input current keeps increasing, the light will become harder to be captured by the optical fibres and hence cause lower coupling efficiency. This donut-shaped optical spectrum also indicates the importance of accurate fibre alignment while transmitting optical signals, since a small amount of axial tilt or transverse offset could cause a considerable loss of optical power.

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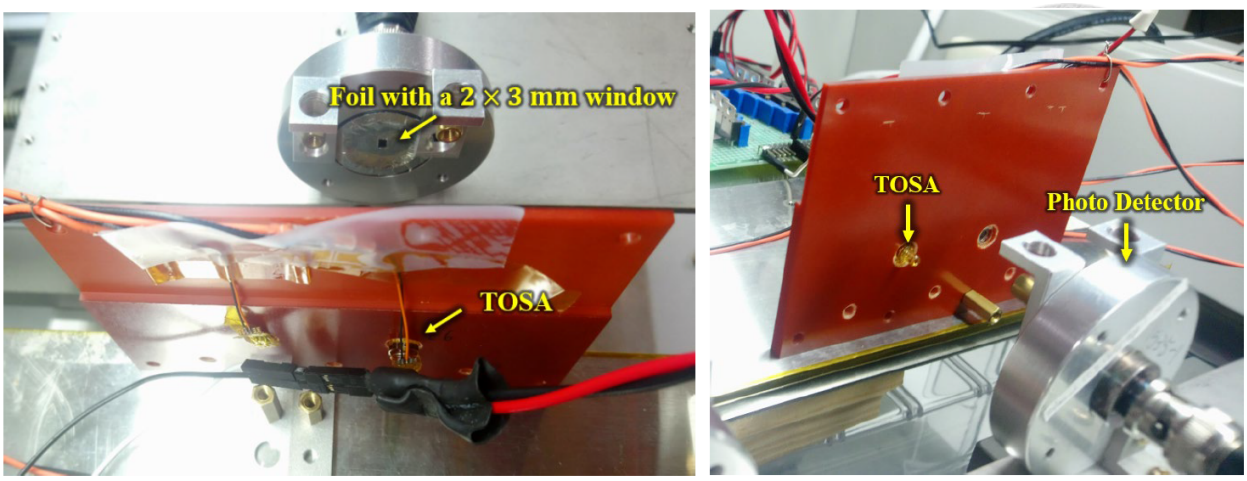

Figure II.17: Experimental setup for studying the output TOSA light distribution.

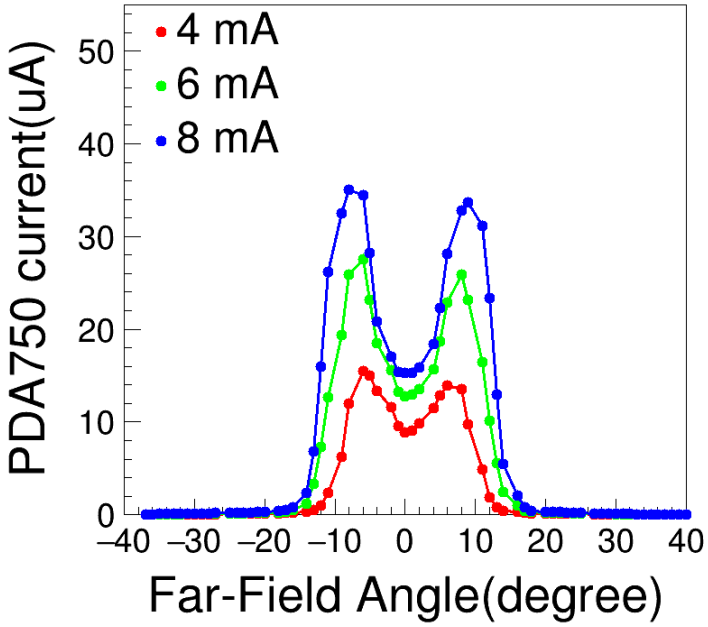

Figure II.18: Optical spectra of output TOSA light with input currents 4, 6 and 8 mA.

In order to study the behaviour of the output TOSA light without a focusing lens, we cut off the head of one TOSA to remove the lens (see Fig. II.19) and used the same experimental setup as the previous experiment (see Fig. II.17) to measure the optical spectrum. The distance between the glass surface of the TOSA and the photodetector is 50.9 mm.

Fig. II.20 shows a comparison of the optical spectra between a TOSA and a

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TOSA without focusing lens. The red curve is an optical spectrum of a TOSA measured at 4 mA. The green curve is an optical spectrum of a TOSA without a focusing lens, measured at 4 mA. The reason why the values in the green curve are lower than the values in the red curve is due to the different distance between the light source and the photodetector. In order to calibrate this light loss, we multiply all values in the green curve with 1.3, as shown in the blue curve in Fig. II.20. The far-field angle of the blue and red curve is only different by one degree. This fact indicates that the focusing lens in this type of TOSA does not contribute significantly on the divergence angle of light.

Figure II.19: A TOSA without focusing lens.

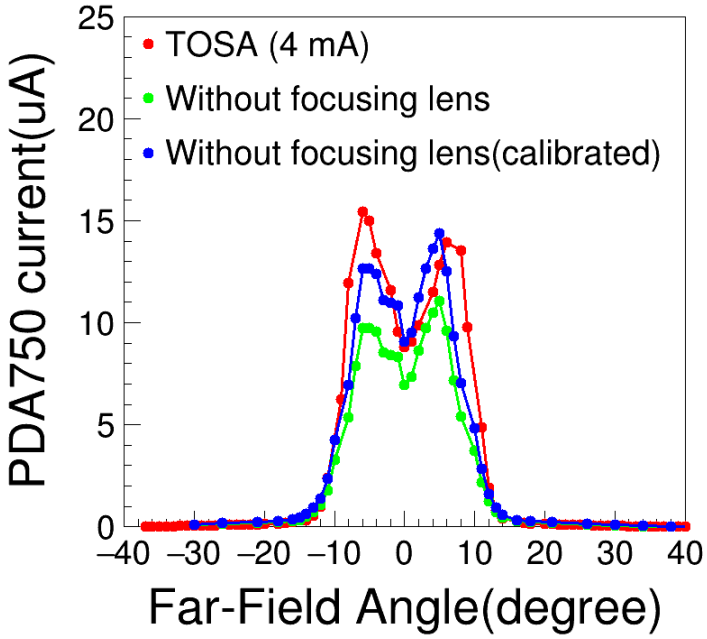

Figure II.20: Optical spectrum comparison of a TOSA and a TOSA without a focusing lens.

For the study of light output after going through an optical fibre, we connected the TOSA to a fibre optic cable which terminated with a Lucent con-

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nector (LC) on one end and a straight tip (ST) connector on the other end to measure one dimensional optical spectrum after light coupling. The experimental setup is shown in Fig. II.21. The distance between the ferrule of ST connector and the photodetector is 41.9 mm. After propagating through the fibre, the shape of the optical spectrum is modified and has a narrower far field angle than the spectrum detected directly from the TOSA. As shown in Fig. II.22, the optical spectrum of 3 mA input current has only one peak, but the spectrum driven by higher input currents still possesses two asymmetric peaks. The optical spectra have been reshaped by the optical fibre. One of the reasons for this reshaping is that the light which has large divergence angle before going into the fibre, may not be able to be captured by the fibre due to the small acceptance angle of the fibre. Another reason may be the attenuation of light as the light travels through the fibre, such light with too large a divergence angle, may not possess enough power to be detected.

Light coupling can heavily impact the performance of optical links. The main reason causing a low coupling efficiency may come from the laser-to-fibre stage. One of the reasons is the wider divergence angle of light. Another reason is the small diameter of fibre core which has a narrower acceptance angle than the photodetector.

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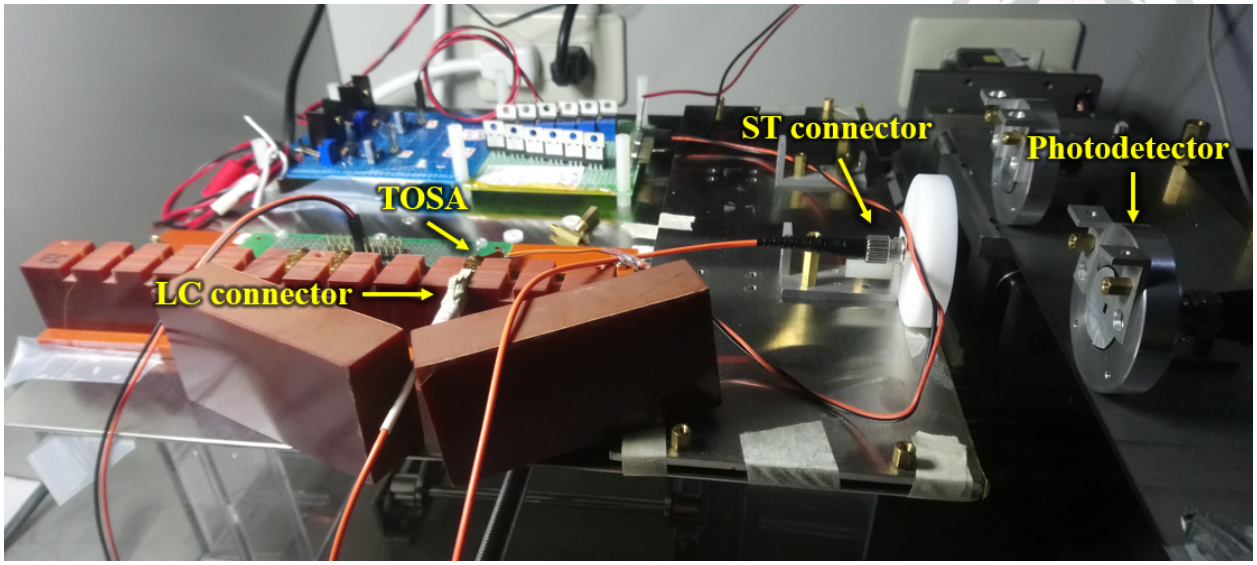

Figure II.21: Experimental setup for the study of the optical spectra of light passing through an optical fibre.

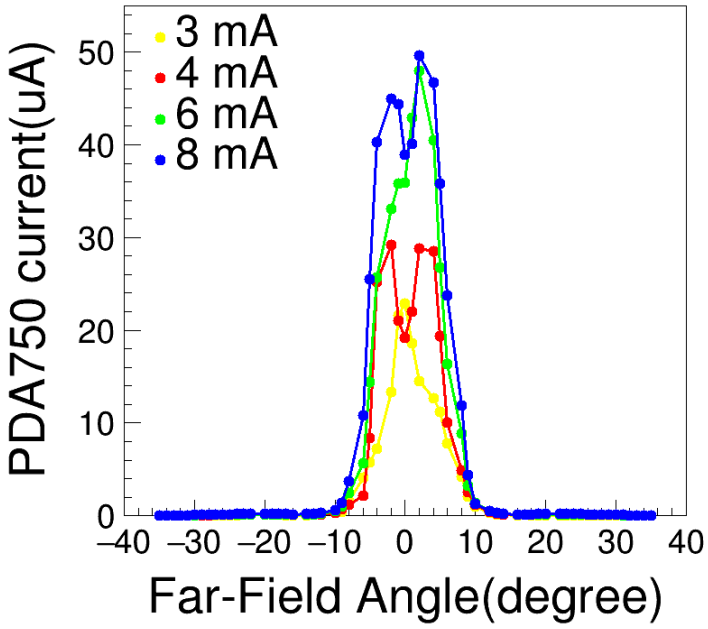

Figure II.22: Comparison of optical spectra with different input currents after TOSA coupling to an optical fibre.

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II.5 Operating principles of PIN photodiodes

The PIN photodiode is used to convert optical signals into electrical signals and is one of the components used in the ROSAs at the Versatile Link project. A PIN photodiode has an undoped intrinsic semiconductor region sandwiched between a p-type semiconductor and an n-type semiconductor. As photons hit the intrinsic region, the electrons in the valence band will jump to the conduction band therefore generate carriers in this region. The electrons of the carriers will then move to the n-type region while the holes of the carriers will move to the p-type region by the force of electric field in the intrinsic region. As the result, an electric current will be generated and flow into the circuit. For example, a typical 10 Gbps PIN photodiode(PIN-ULM-10-TT-V03 type from ULM photonics) with 70 µm active area diameter has responsivity around 0.6 A/W and dark current from 0.02 to 0.2 nA.

The InGaAs-based and GaAs-based PIN diodes in the Versatile Link project has been tested for radiation tolerance ability by using pion and neutron beams, as shown in Fig. II.23 [19]. The responsivity (η) in photodiodes is a ratio of electrical outputs and optical inputs. The relative responsivity (η/η_0) is a ratio of the measured values of responsivity and the initial values. In Fig. II.23, the InGaAs-based PIN photodiode shows a better performance in a high radiation environment but has larger leakage current in high fluence. The GaAs-based PIN photodiode in Fig 30 has 70 µm of active area diameter while the InGaAs-based PIN photodiode has 60 µm.

A correlation between electrical outputs and optical inputs of an InGaAs-based PIN photodiode with 60 µm of active area diameter is shown in Fig. II.24 [19]. The leakage current with zero optical input values, increases with higher fluence in InGaAs-based PIN photodiodes.

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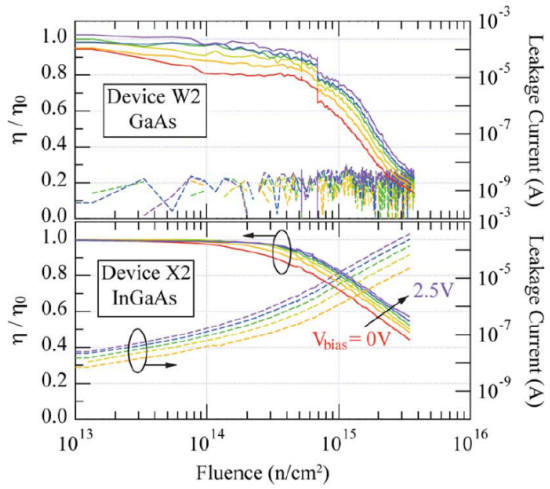

Figure II.23: Relative responsivity of InGaAs and GaAs-based PIN photodiodes exposed in pion and neutron beams with increasing reverse bias voltage from 0 V to 2.5 V.

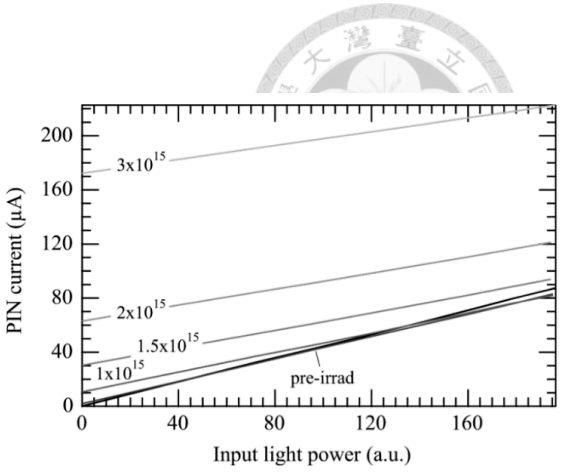

Figure II.24: Current output versus optical power input of an InGaAs-based PIN photodiode.

II.6 Operating principles of Transimpedance amplifier

The Transimpedance amplifier (TIA) is a circuit which used to convert the low-level input current into an output voltage. The TIA is one of the optical electronics components used in ROSAs, because the input current generated by the photo detector is usually not strong enough (it is in the microampere scale) to be used immediately [17]. The current must be first amplified in the TIA. The open loop gain of the amplifier is determined by the feedback resistor (R_F), as shown in Fig. II.25. Subsequently, the amplified current is converted into a differential output voltage. The schematic diagram of the TIA is shown in Fig. II.26 [20]. The differential cascade structure of the TIA can attain high power supply rejection ratio (PSRR), high common-mode rejection ratio (CMRR), low input referred noise, high transimpedance gain and high bandwidth [20].

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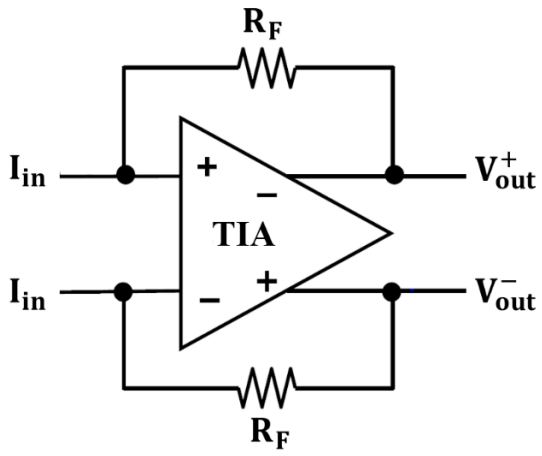

Figure II.25: The circuit of TIA with two feedback resistors.

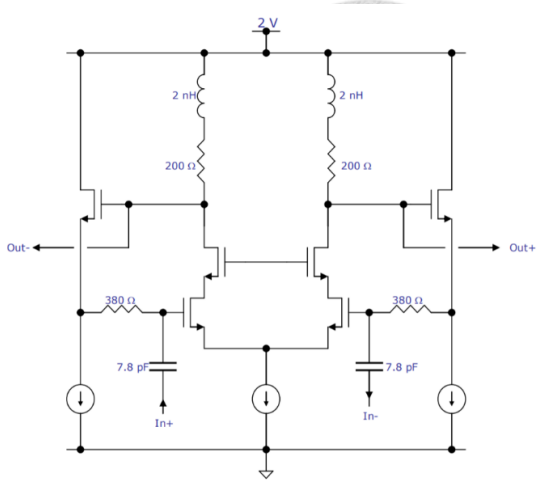

Figure II. 26: Schematic diagram of a TIA.

II.7 Definition of Radiation Hardness

Since most of the COTS electronics products could not work properly in a radiation environment, additional designs and tests to assure the reliability of radiation damage resistance are required. The tests usually include three types of radiation effects: the total ionizing dose (TID), the displacement damage and the single event effects (SEE).

The TID is the total dose that the electronics absorb cumulatively during the period of time. They are exposed to the ionizing radiation, typically Rad or Gy are used as units of measurement. The TID effect could cause some long-term degradation on the performance of the electronics. For example, it could generate leakage alongside the MOS transistor or produce carriers in the silicon dioxide insulation gate. When the holes are trapped in this area, the threshold voltage of the MOS transistors is shifted. This can cause the MOS to be switched on or off and even fail permanently. A commercially developed CMOS process can usually tolerate a few Krads without notable changes of power consumption. Analog devices such as amplifiers, ADC and DAC could be influenced even with a low TID.

The displacement damage happens when the atoms in the silicon lattice are

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moved by hadrons, resulting in device malfunction. This effect is particularly important for bipolar transistors and optical devices such as optical receivers, lasers, optocouplers and LEDs, while the CMOS ICs are usually not considered to be significantly influenced by the displacement damage. The Non-Ionizing Energy Loss (NIEL) is a used to calculate the quantity of energy loss caused by the displacement of atoms.

The SEE is the effect caused by a single interaction event, typically due to cosmic rays, in silicon. A high energy particle passes through the silicon wafer of a semiconductor and deposits enough charge to form an ionizing trace that could interfere with the performance of the electronics.

II.8 Basic structure and features of optical fibres

According to the theory of classical electromagnetic theory, electromagnetic waves can travel though a homogenous dielectric material in the speed of light. A waveguide geometry can be made to guide the waves to a desired destination. The size of the waveguide is proportional to the wavelength of the waves, meaning that a wave with high frequency requires smaller waveguide. An optical fibre is a kind of waveguide that transfers light waves [17].

The operation principle of optical fibres is based on the principle of total internal reflection. According to Snell's law [17]

$$n_1 sin(\theta_1) = n_2 sin(\theta_2)$$

, where the n_1 and n_2 are the indices of refraction for two different materials. The θ_1 and θ_2 are the incidence and reflection angle respectively. As shown in Fig. II.27 [17], assuming $n_1 < n_2$, when the light travels from the material with smaller index of refraction to another material, the reflection angle θ_2 will be smaller than the incidence angle θ_1. If the light travels from the other side which has larger index of refraction and the incidence angle exceeds the critical angle (θ_T), the light will bounce back to the material with larger index of refraction. This leads to the total internal reflection.

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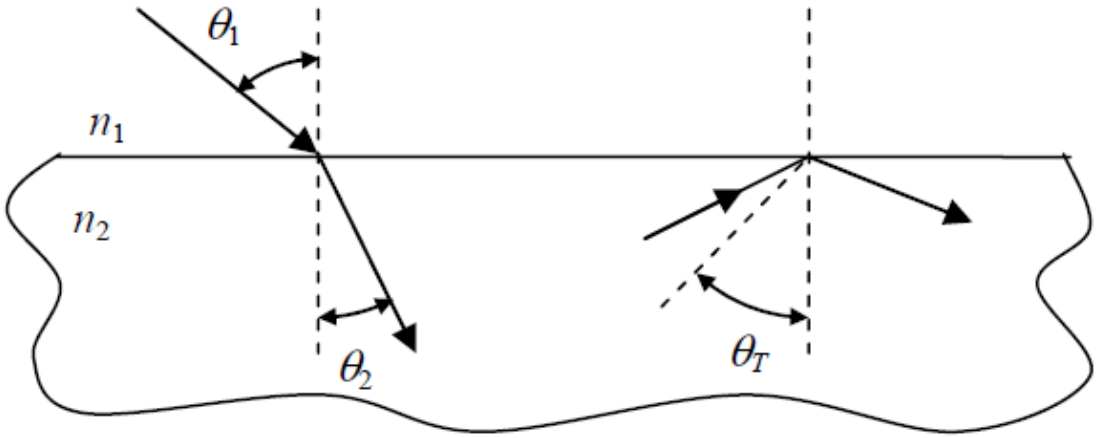

Figure II.27: Refraction and total internal reflection in two materials with different index of refraction.

The basic structure of an optical fibre consists of a core, a cladding and a protective jacket which protects the inner glass from scratches, as shown in Fig. II.28 [17]. The core has larger index of refraction and the cladding has smaller index. The most commonly used material to produce optical fibres is silica (SiO_2) due to its low optical attenuation which is much lower than the plastic optical fibres. Using dopants such as P_2O_5 and GeO_2 can shift the index of refraction a bit higher and other dopants such as B_2O_3 and F can shift the index a bit lower.

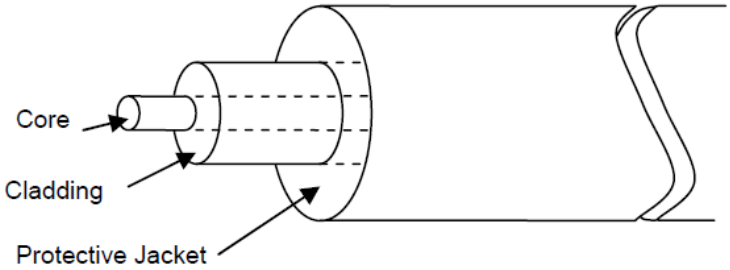

Figure II.28: Basic structure of an optical fibre.

Since each light reflection in an optical fibre can cause the energy to attenuate and eventually become invisible, this determines the kind of mode the fibre can support. Typically, the larger the core size is, the higher the numbers

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of modes the fibre can support. Different modes correspond to different paths of light traveling in the fibre. In Figures II.29a and II.29b, multi-mode fibres are shown with a step index of refraction in II.29a and graded index in II.29b. In II.29c, a single-mode fibre is shown. The step index fibre transfers a pulse in different modes which arrive at the destination in different times. This can cause pulse spreading and hence reduce the bit rate. The graded index fibre equalizes the velocity of different modes, reducing the pulse spreading. The single mode fibre allows only one mode to propagate, therefore has no pulse spreading and can transfer signal in longer distance than multi-mode fibres. The fibre type which is chosen for light transmission of MTx modules is the graded index one.

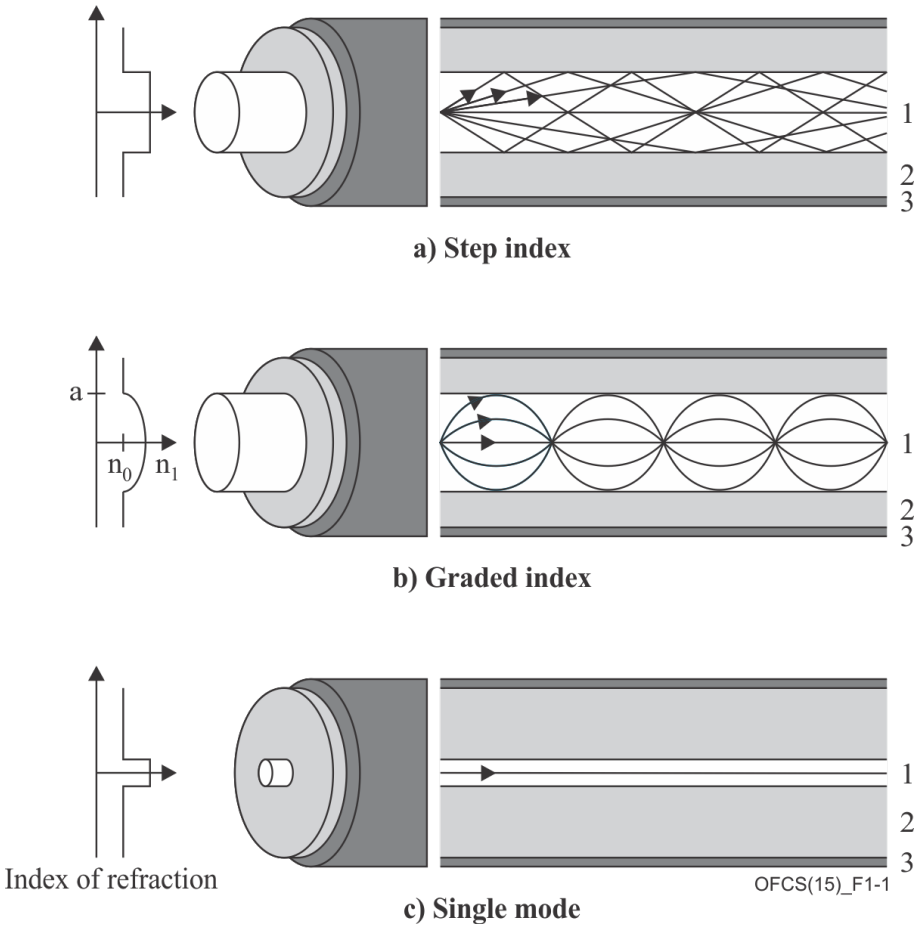

Figure II.29: Structure of single mode and multi-mode fibres. Multi-mode fibres with step and graded index of refraction are shown in II.29a and II.29b, respectively. Structure of a single mode fibre is shown in II.29c.

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II.9 Summary

In this chapter, the requirements of radiation tolerance for the LAr front-end electronics in the HL-LHC were presented. This is one of the main reasons for the upgrade of the current electronics in the detector.

The basic operating principles and features of optical electronics used in the MTx, MTRx and MTx-SFP were discussed, including the structure of VCSELs, protocol of I^2C bus, pin map and block diagram of the LOCld2 laser driver, structure of TOSAs and ROSAs, features of L-I curve of the TOSAs, experiments for studying divergence angle of TOSA lights, operation principle of PIN photodiodes and TIAs. The definition of radiation hardening were also provided.

The radiation tolerance of all opto-electronics used in the MTx, MTRx and MTx-SFP modules, including VCSELs, LOCld2 laser drivers, TOSA, ROSA and PIN photodiodes, were tested and proven to meet the requirements in the HL-LHC.

The L-I curve of all 3792 TOSAs used in the MTx, MTRx and MTx-SFP modules show that the threshold current for this type of TOSAs is around 1 mA. With the same input current, a large deviation of optical powers in this type of TOSAs is observed. For the uniformity of MTx, MTRx and MTx-SFP module performance, selection criteria were applied to the TOSAs during the module production process, selecting TOSAs which have optical power between 550 µW and 800 µW at 6 mA input current.

The optical spectra measured from the experiments of TOSA light output show that the divergence angle of light is approximately the same with or without the focusing lens in this type of TOSA. Furthermore, after light going through an optical fibre, the divergence angle becomes smaller due to light attenuation and due to the small acceptance angle of optical fibres.

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III Optical transceiver assembly

The optical transceivers are fabricated with the LOCld2 laser driver and multi-mode 850 nm VCSELs for data transmission over few hundred metres. This section presents the module assembly procedures of the miniature optical transmitter (MTx), transceiver (MTRx) and the transmitter which are packaged in small form-factor pluggable format (MTx-SFP). Including spares, there are 3240 MTx modules for data transmission, and 810 MTRx for clock and control signals required in the LAr phase-I upgrade. Those MTx and MTRx modules will be mounted on 150 LAr Trigger Digitizer Boards (LTDBs) [3]. 600 MTX-SFP modules, including spares, are required by the forward muon New Small Wheel detector (NSW) and will be mounted on 256 trigger router boards [21]. The yield rate of MTx and MTRx is as high as 98% for a total 4650 modules. Since these modules will be operated in a harsh radiation environment for more than ten years, radiation hardness studies have been performed for all opto-electronics devices.

III.1 Structure and module assembly procedure of Miniature Optical Transmitter

The Miniature Optical Transmitter (MTx) is a dual-channel miniature optical transmitter, fabricated by the LOCld2 laser driver and a pair of 10 Gbps TOSAs (TTF-1F59-427 from the Truelight Corp.), and consists of a multi-mode 850 nm VCSEL. The front and back side of a MTx module are shown in Figures III.1 and III.2, respectively. The LOCld2 chips and VCSELs packaged in TOSA, were all tested during the production process before being assembled in modules. In order to provide a more uniform response for channels 1 and 2, the two TOSAs on a MTx module have been selected to give approximately equal optical power.

The PCB of the module is made of FR-4 (Flame Retardant) material which is a glass-reinforced epoxy resin laminate material with high resistance on fire,

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high mechanical strength, low water absorption and high electrical insulating ability for a wide range of relative humidity [22]. The dimension of the PCB is 15 mm in width, 44 mm in length, and 1 mm in height.

The height of a MTx module is 6 mm. This height is restricted by the space left in the current LAr front end crate. The MTx module is designed in a mezzanine format due to the requirements of manual soldering and testing of VCSELs.

A 0.1 mm thick silicone based thermal conductive pad (H48-2K from T-Global Technology Corp.) is taped on the back side of MTx modules, as shown in Fig. III.2. This pad has low thermal impedance for heat dissipation of MTx modules, low oil blead and high dielectric breakdown voltage [23].

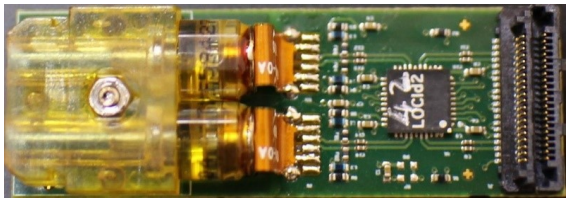

Figure III.1: The frond side of a MTx module.

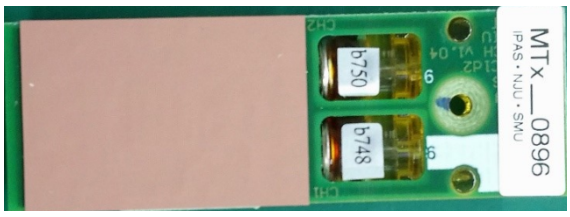

Figure III.2: The back side of a MTx module.

A dual channel latch is mounted on MTx modules for fibre alignment. The material of the latch is the same as the housing of TOSAs. They are both made of Polyetherimide (PEI), a material that has been tested by CERN and shown to have high radiation tolerance [24]. This type of latch is used for fibre ends which only consist of a ferrule, a metal flange and a spring, without the LC connector body, as shown in the yellow part of Fig. III.3. The assembly of the latch is demonstrated in Fig. III.4.

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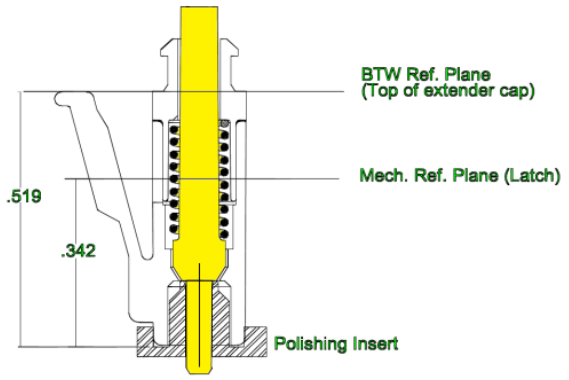

Figure III.3: A LC connector without a connector body.

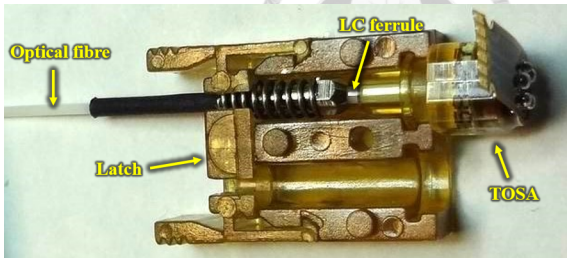

Figure III.4: Assembly of a dual channel latch, an optical fibre and a TOSA.

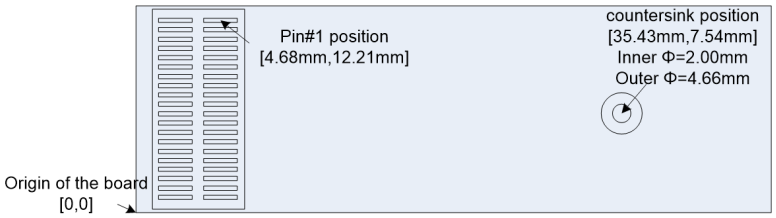

Figure III.5: MTx electrical interface by using a Samtec LSHM connector.

MTx is packaged with a Samtec LSHM connector (LSHM-120-02.5-L-DV-A), as shown in the Fig. III.5, a high density and high-speed razor beam hermaphroditic strip for board-to-board communication. The connector has 40 pins; the definition of those pins is shown in Table III.1. The countersink is used to screw the latch on the MTx module PCB, and fix the modules on the LTDB.

doi:10.6342/NTU202003796

Pin number	signal	Pin number	signal
2		1	ResetB
4		3	GND
6		5	DIN1-n
8		7	DIN1-p
10		9	GND
12		11	LD-V25-1
14	GND	13	LD-V25-1
16	AD0	15	
18	AD1	17	LD-V33-1
20	AD2	19	LD-V33-1
22	AD3	21	LD-V33-2
24	AD4	23	LD-V33-2
26	GND	25	
28	SCL	27	LD-V25-2
30	SDA	29	LD-V25-2
32	GND	31	GND
34		33	DIN2-n
36	I2-V25	35	DIN2-p
38	I2C-V25	37	GND
40		39	

Table III.1: Pin definition of a LSHM connector.

The MTx production process is described by the following steps:

1. Mount electronic components on the module PCB by using surface mount technology (SMT).

2. Solder a pair of TOSAs which had been tested and selected for approximately equal light on the module PCB. Since the TOSAs could easily be damaged by static electricity, we use electrostatic discharge (ESD) protection devices at all time and do not touch the copper part of the TOSAs. Using too much solder to weld TOSAs may produce a solder bump on the back side of MTx modules. Fig. III.6 shows a successful soldering of TOSAs on the PCB and Fig. III.7 shows an unsuccessful solder which cause bumps after adhering a thermal conductive pad.

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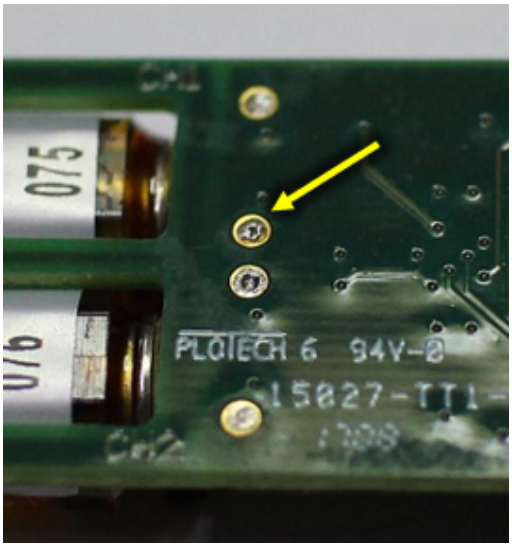

Figure III.6: Successful soldered case of TOSAs onto a MTx module.

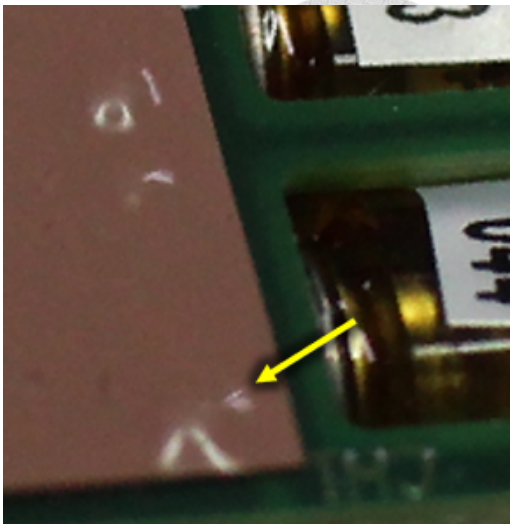

Figure III.7: Unsuccessful soldered case of TOSAs onto a MTx module.

3. Test the current of the circuit for possible shorts or opens and measure the bit error rate.

4. Use an ultrasonic cleaner filled with 75% Ethyl alcohol to remove the solder paste on the MTx modules for 30 minutes, as shown in Fig. III.8. Store the TOSAs in a shelf, to keep them out of Ethyl alcohol during cleaning, as shown in Fig. III.9.

Figure III.8: Ultrasonic cleaner for solder paste cleaning.

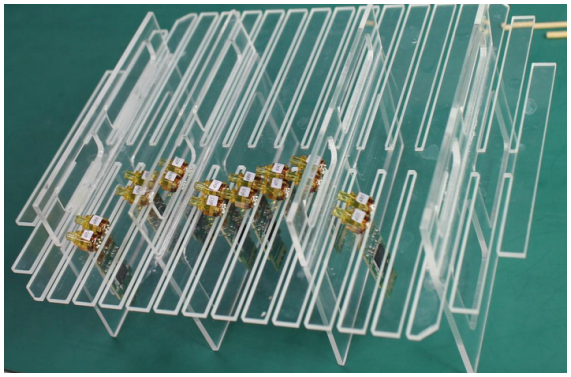

Figure III.9: A special shelf for hanging MTx modules.

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5. Assemble a latch on the module to hold the TOSAs parallel to each other, and help fibre-optic cables to plug-in.

6. Adhere a thermal conductive pad to cover and isolate the circuit on the back side of the module, as shown in Fig. III.10.

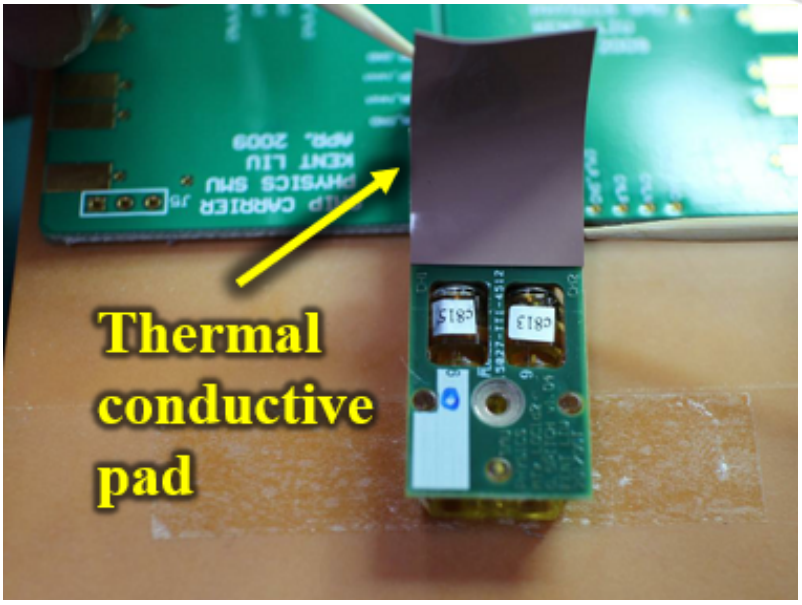

Figure III.10: Adhere a thermal conductive pad onto a MTx module

7. Attach a module ID label on the module.

8. Test for I^2C and 10 Gbps bit error rate of the module.

9. Test the eye diagram of the module for quality assurance analysis.

III.2 Structure and module assembly procedure of Miniature Optical Transceivers

Miniature Optical Transceiver (MTRx) modules have similar structure as MTx modules, as shown in Figures III.11 and III.12, the front side and back side of the module, respectively. A MTRx module has a TOSA for the transmitter channel and a ROSA for the receiver channel; the positions of these channels are shown in Fig. III.13. The ROSA used in MTRx modules is a customized optical receiver consisting of a photodiode and a Gigabit Transimpedance Amplifier

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(GBTIA), developed by CERN to collect current from the photodiode. The dimensions of a MTRx module are the same as the ones of the MTx module.

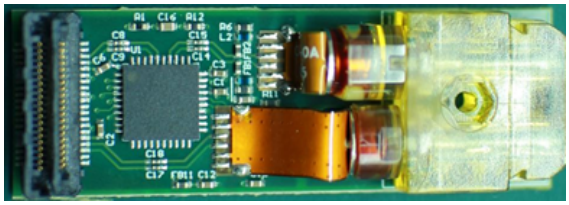

Figure III.11: The front side of a MTRx module.

Figure III.12: The back side of a MTRx module.

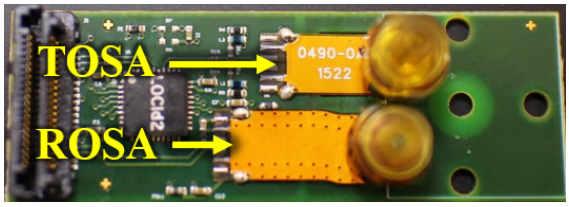

Figure III.13: The front side of a MTRx module without a latch.

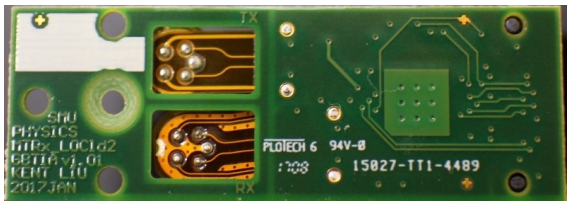

Figure III.14: The back side of a MTRx module without a latch and a thermal conductive pad.

The MTRx production process is described by the following steps:

1. Mount electronic components on the module PCB by using surface mount technology (SMT).

2. Solder one TOSA on the module PCB. Fig 49 shows the position of the solder point.

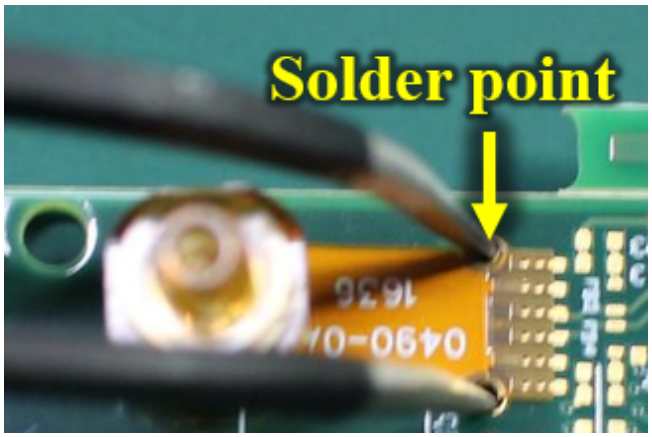

Figure III.15: Solder point position of a TOSA on a MTx module.

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3. Test the current of the circuit for possible shorts or opens and measure bit error rate.

4. Solder one ROSA on the module PCB.

5. Test the receive (RX) signal from the ROSA.

6. Use an ultrasonic cleaner filled with 75% Ethyl alcohol to remove the solder paste on the MTRx modules for 30 minutes.

7. Assemble a latch on the module.

8. Adhere a thermal conductive pad to cover and isolate the circuit on the back side of the module.

9. Attach a module ID label on the module.

10. Test for I^2C and 10 Gbps bit error rate of the module.

11. Test the eye diagram of the module for quality assurance analysis.

III.3 Structure and module assembly procedure of Miniature Optical Transmitter Small Form-Factor Pluggable

Miniature Optical Transmitter Small Form-Factor Pluggable (MTx-SFP) modules are MTx modules packaged in metallic SFP cages for high mechanical strength and easy plug-in for fibres. Figures III.16 and III.17 show the front side and back side of a MTx-SFP module, respectively. Fig. III.18 shows a MTx module before assembly into SFP cage.

Figure III.16: The front side of a MTx-SFP module.

Figure III.17: The back side of a MTx-SFP module.

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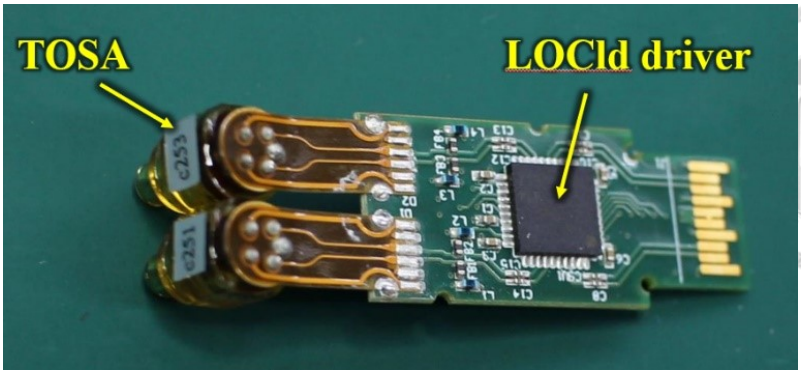

Figure III.18: A MTx module without a SFP cage.

The MTx-SFP production process is described by the following steps:

1. Mount electronic components on the module PCB by using surface mount technology (SMT).

2. Solder a pair of TOSAs which have been tested and selected for approximately equal light on the module PCB.

3. Test the current of the circuit for possible shorts or opens and measure the bit error rate.

4. Use an ultrasonic cleaner filled with 75% Ethyl alcohol to remove the solder paste on the MTx modules for 30 minutes.

5. Record the LOCld chip ID and TOSA ID to the datasheet.

6. Press the module into the SFP cage and put on a latch, as shown in Fig. III.19. Screw a cover on the SFP cage, as shown in Fig. III.20. Put on a ground ring to the SFP cage, as shown in Fig. III.21.

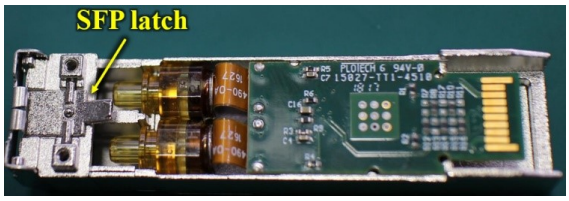

Figure III.19: Assembly of a MTx module in a SFP cage.

Figure III.20: Placement of a SFP cover into a SFP cage.

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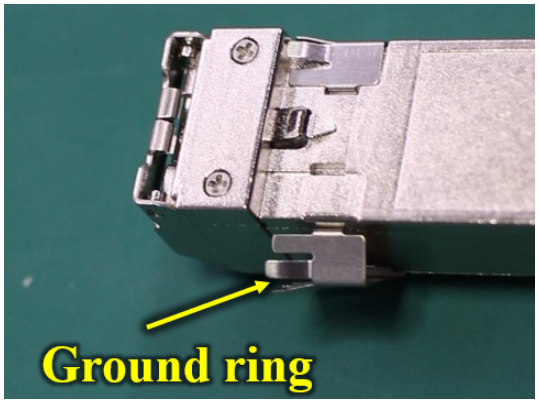

Figure III.21: Fixing a ground ring around a SFP cage.

7. Attach a module ID label on the module.
8. Test the module for I^2C and 10 Gbps bit error rate.
9. Test the eye diagram of the module for quality assurance analysis.

III.4 Definitions of Eye-diagram parameters

The eye-diagram is used to estimate the quality of input digital signals. It provides information such as the health of the system bandwidth, Bit-Error-Rate (BER) degradation, and long-pattern dependence of a signal. However, it can not reveal protocol or logical problems. The most commonly used digital signal coding scheme is the Non-Return-to-Zero (NRZ) code. As shown in Fig. III.22 [17], the logic number "1" and "0" are constant values in NRZ code form, while the physical signal which is typically represented by an optical waveform, the "1" and "0" are no longer constant values but have jitter, amplitude noise, or phase noise. The bit rate can be measured by the byte period (T_B). For example, assume the T_B is 1 ns and as shown in Fig. III.22, there are 10 bits of data transferred during this period of time, the bit rate is therefore 10 bits/ns (10 Gbps).

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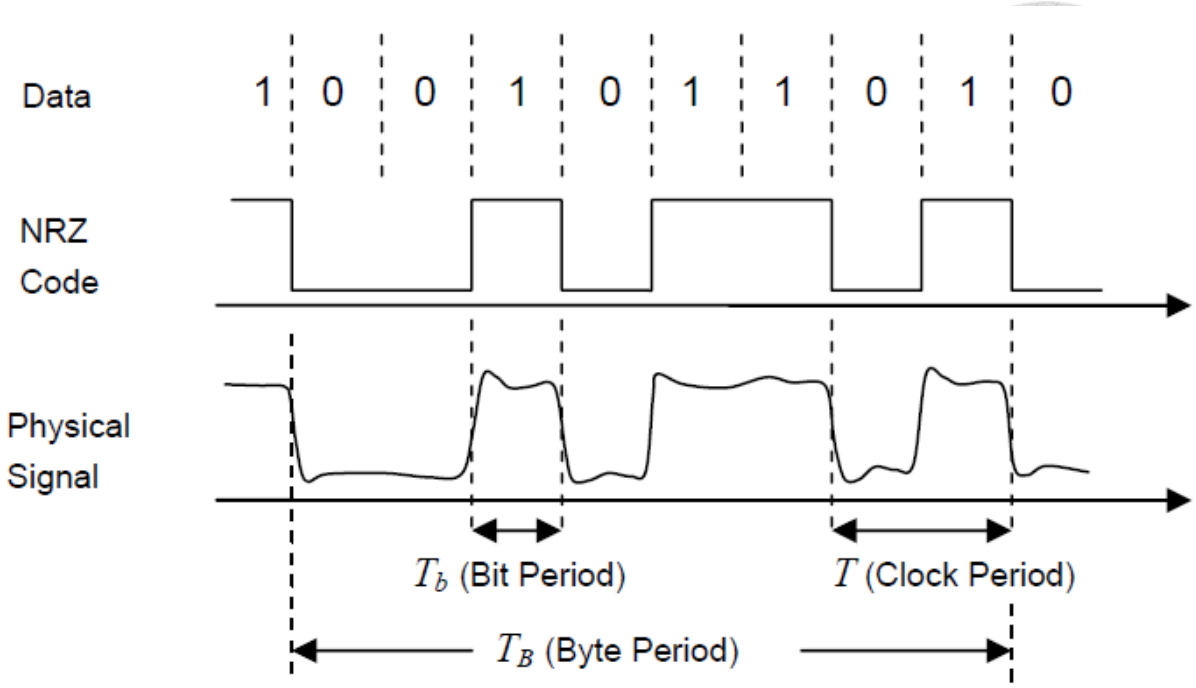

Figure III.22: Correlation of binary data, Non-Return-to-zero code and physical signals.

An eye-diagram represents high-speed digital signals in the time domain by overlapping many bit sequences on each other, which are supposed to cover all possible bit sequences, as shown in Fig. III.23 [25]. The ideal eye-diagram shape without any deviation of signals is of rectangular shape. There is a lot of information that can be found in an eye-diagram. Fig. III.24 [17] shows an eye-diagram with the main parameters that will be discussed in the following sections.

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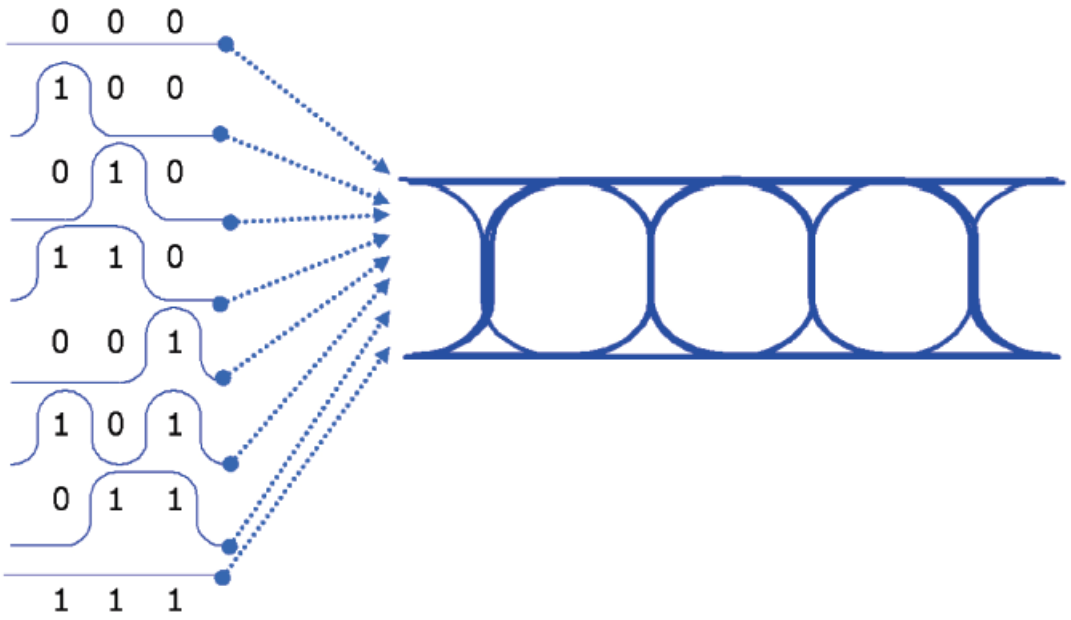

Figure III.23: Generation of an Eye-diagram by overlapping all possible bit sequences on the top of each other.

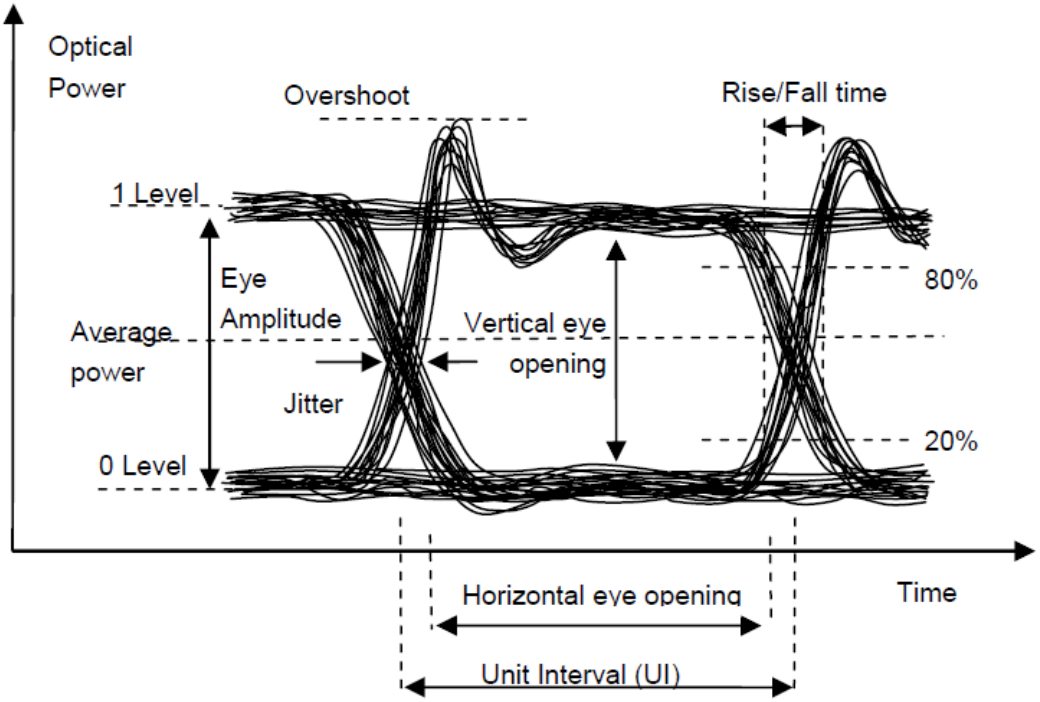

Figure III.24: Typical parameters of an eye-diagram.

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III.4.1 Average Optical Power

The average optical power (AOP) is estimated by calculating the average value between the logical "1" level and "0" level, as shown in the equation:

$$P_{avg} = \frac{(P_0 + P_1)}{2} \ ,$$

where P_{avg} is the AOP. P_0, P_1 are power levels of logical "0" and "1" respectively. The eye-diagram can only provide an estimated number of average optical power. To measure a more precise value of AOP, low bandwidth broad area detectors and optical power meters are required [17].

III.4.2 Optical Modulation Amplitude

The optical modulation amplitude (OMA), also known as "eye amplitude", is the difference between the logical "0" level and "1" level. This value is crucial for logic circuits of a receiver, to decide whether a received data bit is a "0" or a "1". The other important amplitude parameter is called the "eye height", as shown in Fig. III.25 [26], this is the difference between the $+3\sigma$ of the logical "1" level histogram and the -3σ of the logical "0" level histogram. The eye height is used to determine whether an error is detected, and hence it concerns the bit error rate.

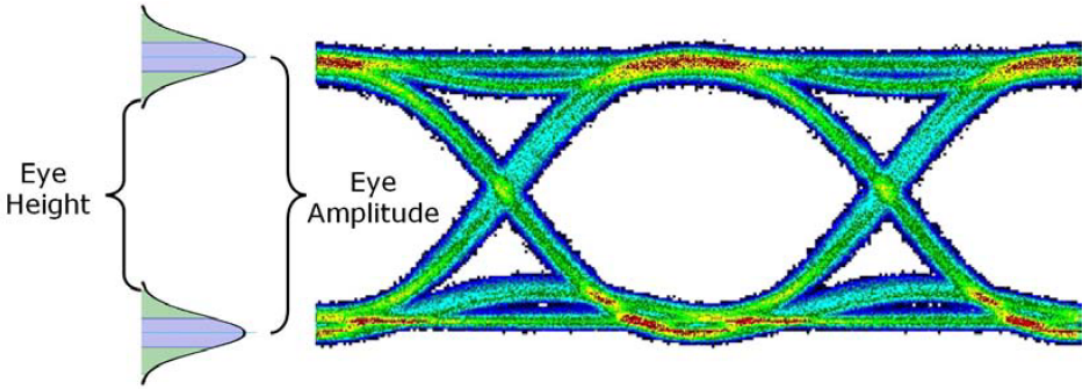

Figure III.25: OMA and eye height parameters.

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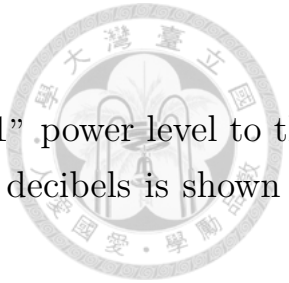
III.4.3 Extinction Ratio



The extinction ratio (ER) is the ratio of the logical "1" power level to the logical "0" power level. The definition of ER in units of decibels is shown in the following equation [17]:

$$ER(dB) = 10log_{10}\frac{P_1}{P_0}$$

Where P_0, P_1 are the power levels of logical "0" and "1", respectively.

A higher ER value can generate a lower bit error rate. In consideration of this and the fact that in signal transfer what matters is the difference between "1" level and "0" level, we hope that the "0" power level be zero or completely dark. This is, unfortunately, not practical in high bit rates due to the influence of turn-on delay and frequency chirp [17].

III.4.4 Jitter

Jitter, or phase noise, is one of the key parameters in an eye-diagram. It represents the timing divergence between data-bits and expected points, as shown in Fig. III.26 [26]. Jitter can be separated into two parts, random jitter and deterministic jitter [17].

The random jitter is an unpredictable random noise which could happen in all systems such as thermal noise from circuits. Its probability distribution function is the Gaussian distribution. The mean value of this distribution could be set at t = 0 or at the beginning of the unit interval. The rms value of the jitter (J_{rms}) is approximately taken as the standard deviation of the distribution. To calculate the total random jitter, the desired bit error rate can be used to determine how many samples we want to include. For example, if a 10^{-12} bit error rate is to be probed that would correspond to sampling 14 sigmas of the jitter distribution. The total random jitter is therefore $14 \times J_{rms}$.

The deterministic jitter (J_{det}) is predictable and bounded as long as the

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characteristic of the bit stream is known. This jitter could be caused by insufficient system bandwidth, crosstalk, or pulse width distortion. The total jitter of random jitter and deterministic jitter in the simplest form is described by the following equation [17]:

$$J_{total} = J_{det} + KJ_{rms} \ ,$$

where K is a constant for the desired bit error rate, for example, for a bit error rate of 10^{-12}, K equals 14. A function that can describe the total jitter in real applications can contain a lot of free parameters needed to be fit since there may be many sources of random or deterministic Jitter [17].

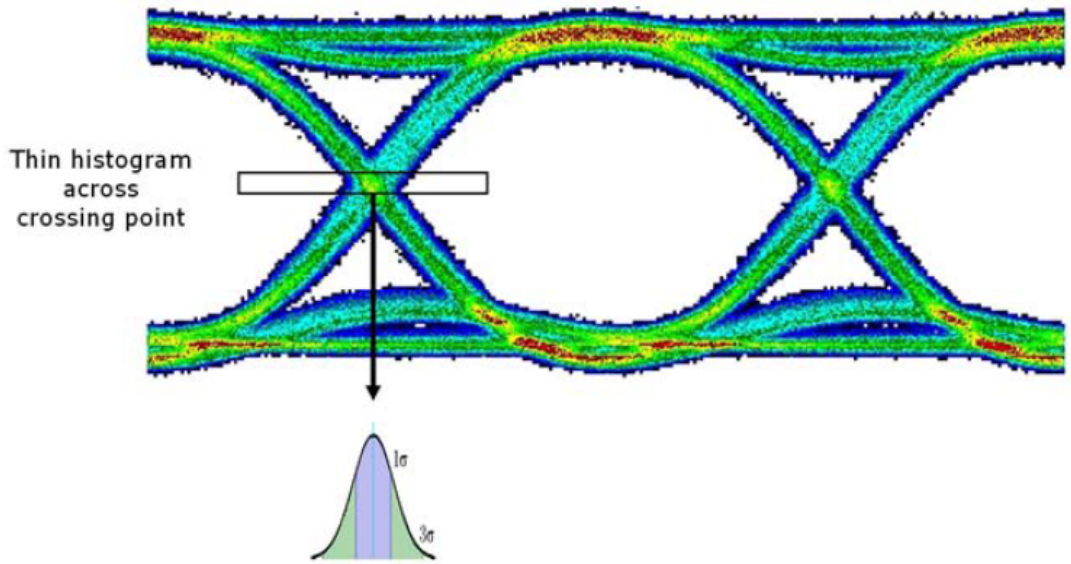

Figure III.26: Jitter in an eye-diagram.

III.4.5 Mask Margin

The mask is a predefined limit line in an eye-diagram which forms a "keep-out" region and represents a minimum requirement for the compliance test. If any sample hits the mask, it will be identified as an error. A mask margin test is a test for monitoring the quality of the production process. To measure the mask margin, the apparatus will increase the mask size linearly before reaching the samples of the actual eye. The mask margin is the percentage of margin by

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which the original mask has to increase, before a failure is detected, as shown in Fig. III.27 [26]. There are several factors that can cause inaccurate result of the mask margin test such as Jitter or noise floor of apparatus.

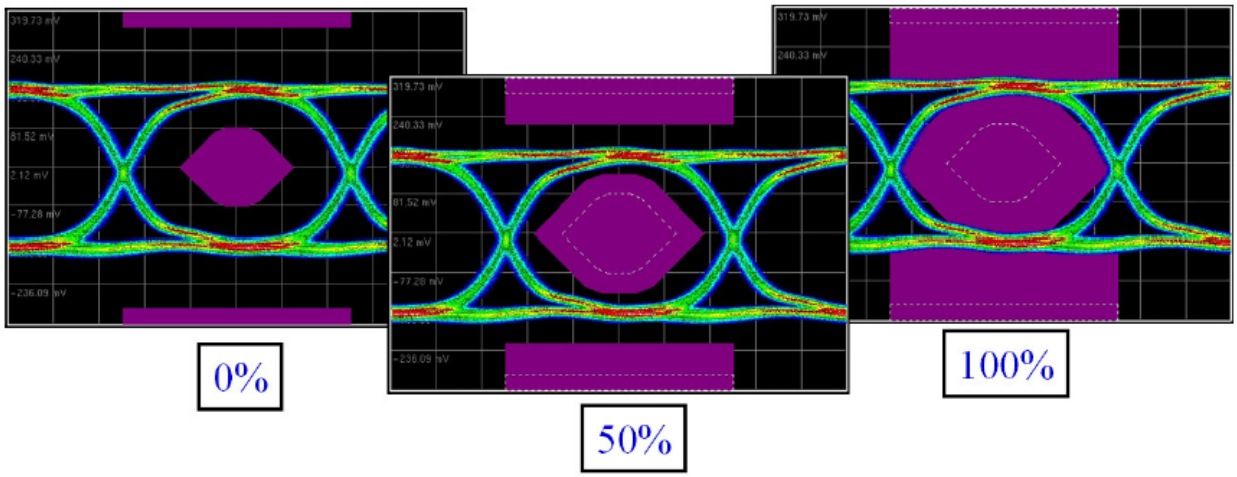

Figure III.27: Mask margin test with 0%, 50% and 100% mask margin value.

III.4.6 Logical "1" and "0" levels

As shown in Fig III.28 [26], the logical "1" level is the mean value of the distribution histogram which is created by all data samples on the upper area of the eye diagram within 40% to 60% region of the eye period. An eye period is the area between two logical level crossing points. For the logical "0" level, a similar procedure as the "1" level is followed. The mean value is calculated from the histogram created from all data samples on the bottom area of the eye diagram ,that lie within the 40% to 60% region of the eye period, as shown in Fig III.29 [26]. The width of the logical "1" and "0" states could be due to the noise coming from light source or the apparatus used to generate the eye-diagram.

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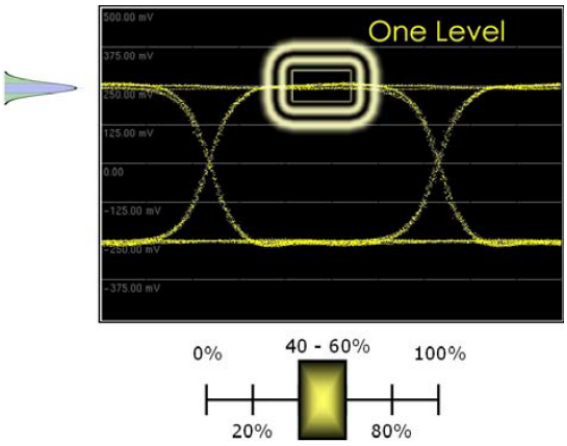

Figure III.28: The logical one level.

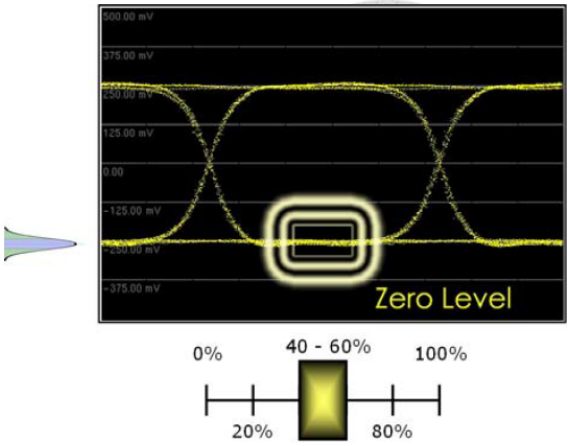

Figure III.29: The logical zero level.

III.4.7 Overshoot

Overshoot refers to the signal exceeding the steady state of logical "1" level during a "0" to "1" transition and may be caused by relaxation oscillation from the semiconductor laser. The other term is called undershoot which happens during a "1" to "0" transition, but is not as noticeable as the overshoot in optical signals due to the fact that an optical signal cannot be negative. Therefore, the undershoot in the electrical signal will not cause a large impact to the driven optical signal [17].

III.4.8 Unit interval

The unit interval (UI) is used to represent the width of one bit in the eye-diagram which is the time difference between two eye crossings. For example, one UI in a data stream with 10 Gbps bit rate is 100 ps. The UI is often used to normalise different data rates by replacing the unit of horizontal time axis, picoseconds, with UI. Using UI as unit can help the analysis of eye-diagrams which have different data rates [17].

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III.4.9 Rise-time and fall-time

The rise-time is the transition time for the signal to change from lower steady state to higher steady state. The fall-time is the transition time from higher to lower state. To avoid the noise from the "1" state and "0" state which may lead to incorrect measurement, the 20% level and 80% level are used to measure the rise and fall time, as shown in Figures III.30 and III.31 [26].

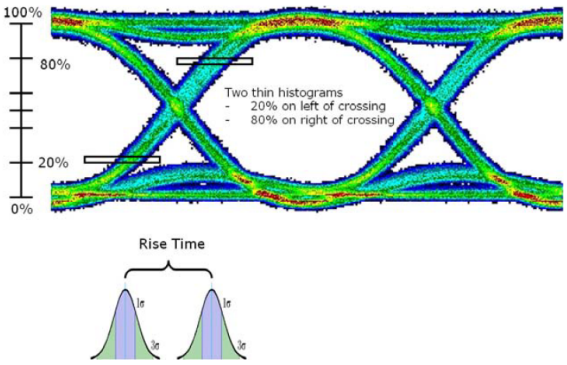

Figure III.30: Rise-time.

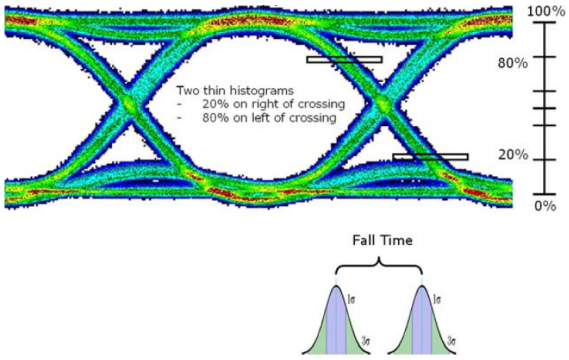

Figure III.31: Fall-time.

Rise-time and fall-time can be used to estimate the bandwidth of the signal since they correlate with the highest frequency of the signal. A smaller rise-time and fall-time can increase the bandwidth of signals but could also cause more overshoot or ringing which degrade the quality of the eye pattern [17].

III.5 Summary

In this chapter, the structure and assembly procedures of MTx, MTRx and MTx-SFP were demonstrated. Each MTx contains a pair of TOSAs, a LOCld2 laser driver, a module PCB, a thermal conductive pad and a dual-channel latch. Each MTRx contains similar components as MTx but with one TOSA as the transmitting component and one ROSA as the receiving component, instead of two TOSAs used in MTx and MTx-SFP modules. The MTx-SFP also has two TOSAs for data transmitting. The differences between a MTx-SFP and a MTx module is that a MTx-SFP module is packaged in a metallic SFP cage and this type of module does not adhere a thermal conductive pad like in MTx modules.

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The assembly procedures of these three types of optical transmission modules are similar; they all include SMT technology to produce PCB, TOSA or ROSA soldering, cleaning solder paste and tests for shorts or opens of the circuit, bit error rate, writing and reading functions of I^2C bus and eye-diagrams. There are only a few differences between the assembly procedures for MTx, MTRx and MTx-SFP modules. For a MTRx module, one has to solder a ROSA and test for the receiving signals. For a MTx-SFP module, the module needs to be packaged in a SFP cage.

An eye-diagram can be used to examine the quality of input digital signals by analysing the parameters and the shape of an eye-diagram. Definitions of the eye-diagram parameters are also presented in this chapter, including the AOP, OMA, ER, Jitter, mask margin, logical one and zero, overshoot, UI, Rise and fall time. In the following chapters, the parameters of eye-diagrams recorded in the quality assurance tests will be analysed.

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IV Quality assurance

This chapter introduces the quality assurance procedures and analysis for MTx, MTRx and MTx-SFP modules. MTx and MTRx modules will be mounted on the LAr trigger boards in ATLAS phase-I upgrade. Since these boards are located inside the detector, their maintenance of these modules after their commissioning will be difficult. Hence, tests for quality assurance before mounting these modules on the detector are necessary.

IV.1 Quality assurance and eye-diagram analysis of MTx modules

The quality assurance tests for MTx modules includes writing and reading functions of I^2C configuration, measurements of currents given by 2.5 V and 3.3 V power supply voltages, bit error rate of data transmission, measurement of optical power, and eye diagram analysis. The following subsections provide a block diagram and function descriptions of the carrier board for MTx module testing, definition of the I^2C configuration, and analysis of eye diagram parameters.

IV.1.1 Block diagram and functions of the carrier board for MTx module testing

A carrier board is used to test MTx modules for quality assurance. This carrier board provides power supplies, differential inputs and an interface of I^2C. The dimensions of this carrier board are 43.2 mm in width, 83.1 mm in length and 16 mm in height. The total power consumption of the board is 321 mW. The block diagram of the carrier board is shown in Fig. IV.1 (made by our group member SMU).

doi:10.6342/NTU202003796

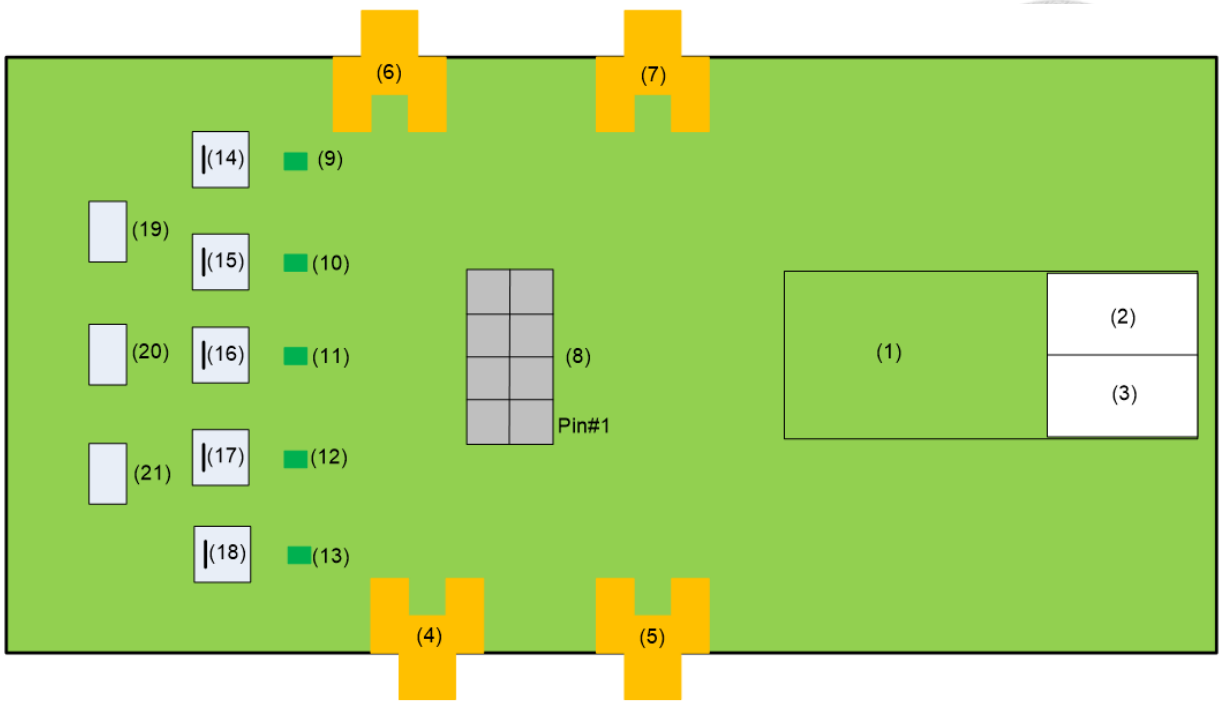

Figure IV.1: Block diagram of a MTx evaluation module (EVM) kit.

The function of each part on the MTx EVM kit is listed below:

(1) MTx transmitter module.

(2) Fibre latch for the channel 2 of the module.

(3) Fibre latch for the channel 1 of the module.

(4) Sub Miniature version A (SMA) connector for receiving inverted signal input (differential) of channel 1. The voltage swing, the difference between maximum output voltage and minimum output voltage, should be within the range of 100 mV to 1200 mV. Inline capacitors on the carrier board provide AC coupling to the signals, blocking the DC component of the signals.

(5) SMA connector for receiving the non-inverted signal input (differential) of channel 1.

(6) SMA connector for receiving the non-inverted signal input (differential) of channel 2.

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(7) SMA connector for receiving the inverted signal input (differential) of channel 2.

(8) 8-pin header for I/O configuration. The pin map of the header is shown in Table 6. Connecting pin ResetB to pin GND by jumpers can reset the I^2C circuit in LOCld2 chip. The pin SCL and SDA are an interface to I^2C.

Pin number	Signal
1	ResetB
2	GND
3	SCL
4	SDA
5	
6	GND
7	
8	GND

Table IV.1: Pin map of the 8-pin header

(9) LED indicates the power on of the I^2C 2.5 V.

(10) LED indicates the power on of the LOCld 2.5 V (channel 2).

(11) LED indicates the power on of the LOCld 3.3 V (channel 2).

(12) LED indicates the power on of the LOCld 3.3 V (channel 1).

(13) LED indicates the power on of the LOCld 2.5 V (channel 1).

(14) Jacket P5 for I^2C 2.5 V power supply for both channels. The current (Idd) of voltage source 2.5 V is 1.8 mA.

(15) Jacket P4 for LOCld 2.5 V power supply for channel 2. The current (Idd) of voltage source 2.5 V is 1.8 mA.

(16) Jacket P3 for LOCld 3.3 V power supply for channel 2. The current (Idd) of voltage source 3.3 V is 96 mA.

(17) Jacket P2 for LOCld 3.3 V power supply for channel 1. The current (Idd) of voltage source 3.3 V is 96 mA.

(18) Jacket P1 for LOCld 2.5 V power supply for channel 1. The current

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(Idd) of voltage source 2.5 V is 1.8 mA.

(19) Jumper for shorting all jackets of 3.3 V, so 3.3 V can be supplied by one jacket.

(20) Jumper for shorting all jackets of 2.5 V, so 2.5 V can be supplied by one jacket.

(21) Jumper for shorting all jackets of 2.5 V, so 2.5 V can be supplied by one jacket.

IV.1.2 Setting of I^2C configuration values in MTx modules

The output light of VCSELs in MTx modules is controlled by a LOCld2 laser driver through an I^2C bus. The carrier board provides an I^2C interface for reading and writing the configuration values in LOCld2 chips. The position of this interface on the carrier board is shown in the yellow rectangle in Fig 67. The configuration values are set to the same values for all modules during the quality assurance test.

The I^2C protocol used in MTx modules is shown in Table IV.2. The slave address has 7 bits, the first 5 bits transmit the chip ID and the last 2 bits transmit the internal register address. The chip ID bits, $A4$ to $A0$, are configured to "00000" by the $R4$ to $R13$ resisters on the carrier board. The position of those resisters is shown in the blue rectangle in Fig. IV.2. The eighth bit, R/W, determines the "read" ("R/W = 1") and "write" ("R/W = 0") functions.

The sixth and seventh bits, Reg2 and Reg 1, are used to configure the peaking voltage, the modulation current, and the bias current for VCSELs. For these two bits, "00" represents register 0 in the LOCld2 laser driver for channel 1, "01" represents register 1 for channel 1. "10" represents register 2 for channel 2 and "11" represents register 3 for channel 2. The content of these registers is shown in Table IV.3.

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	Start	Chip ID					REG		R/W		Data									Stop
SCL:		1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	
SDA:		A4	A3	A2	A1	A0	Reg2	Reg1	R/W	ack	D7	D6	D5	D4	D3	D2	D1	D0	ack	

Table IV.2: I^2C protocol.

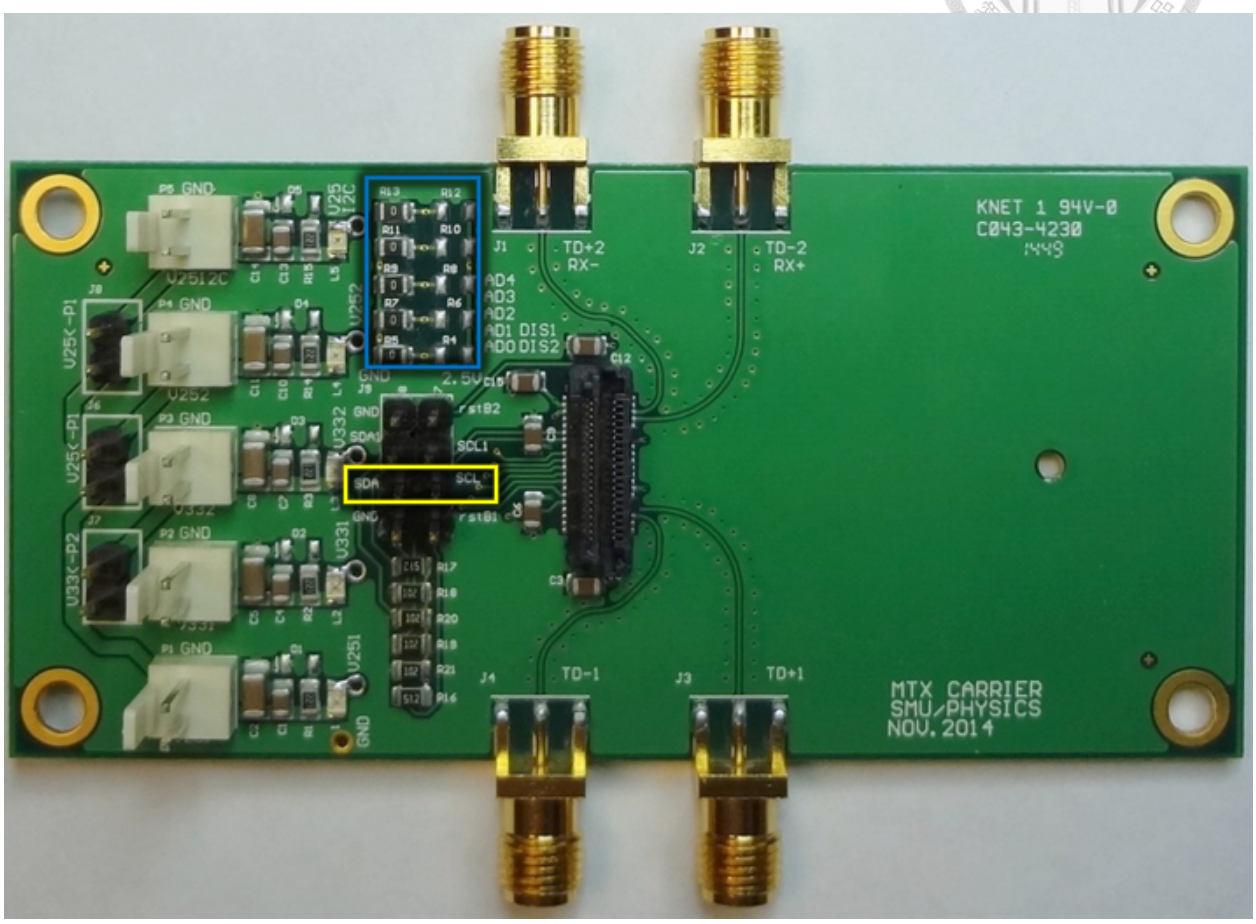

Figure IV.2: Top layer of the carrier board.

Channel 1															
Register 0 (Reg2 = 0, Reg 1 = 0)								Register 1 (Reg2 = 0, Reg 1 = 1)							
Modulation Current				Bias Current				N/A				Peaking Voltage			
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
M3	M2	M1	M0	B3	B2	B1	B0	x	x	x	V5	V4	V3	V2	V1
Channel 2															
Register 2 (Reg2 = 1, Reg 1 = 0)								Register 3 (Reg2 = 1, Reg 1 = 1)							
Modulation Current				Bias Current				N/A				Peaking Voltage			
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
M3	M2	M1	M0	B3	B2	B1	B0	x	x	x	V5	V4	V3	V2	V1

Table IV.3: Register content in a LOCld2 laser driver.

doi:10.6342/NTU202003796

The I^2C interface on the carrier board is connected to a USB module, which is then connected to a computer for LabVIEW control. The LabVIEW interface program is shown in Fig 68. After running the program, if the read values are not equal to the set values, the program will show a red-light ball as a result, to indicate an error.

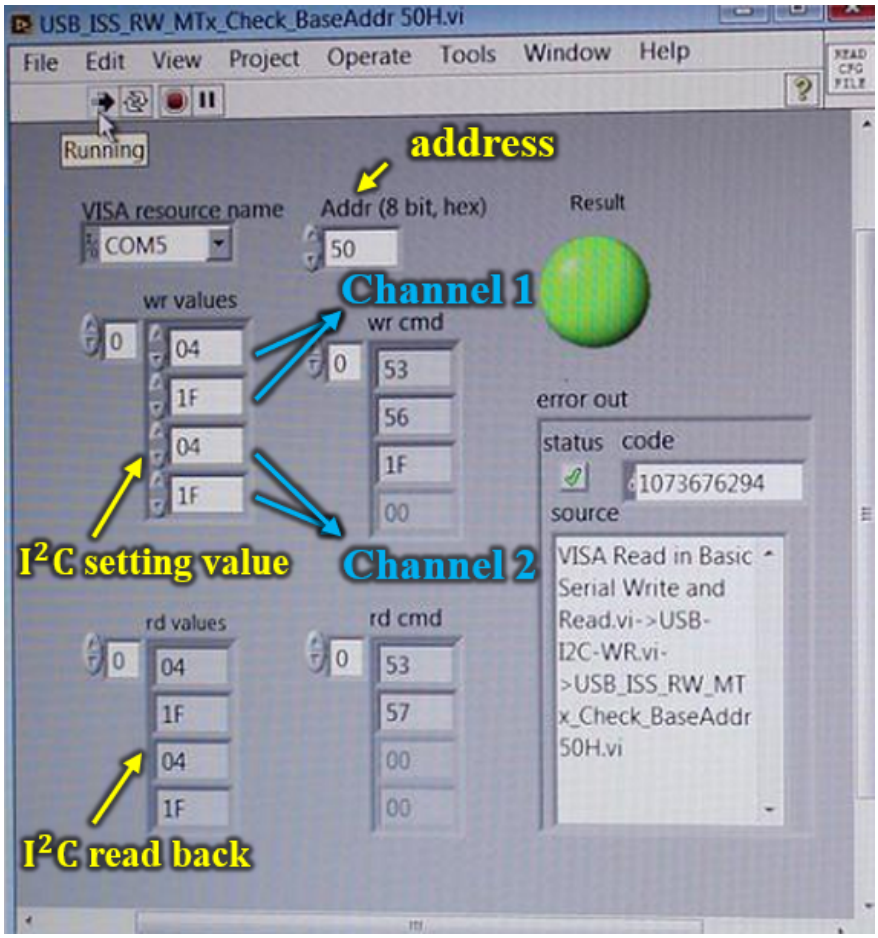

Figure IV.3: I^2C interface on a computer with the address, writing and reading values.

The I^2C setting values on this LabVIEW interface for configuring channel 1 and 2 in a LOCld2 chip is "04" for the modulation and bias current, and "1F" for the peaking voltage. These "041F" configuration values are applied to all modules during quality assurance tests. The definition of those configuration values and the calculation method of bias current, modulation current, and peaking voltage are given in the following paragraphs.

"041F" are hexadecimal numbers. For example, as shown in Table IV.3, in

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order to configure the modulation current in channel 1, we need to transmit 4 bits of a binary number, M3 to M0 in register 0. The leading (first) digit of the hexadecimal number "041F" is equal to "$M3M2M1M0$" in binary form. The value of the modulation current can be calculated by using the following equation:

$$I_{modulation} = 6.4mA + 0.4mA \times (M3M2M1M0),$$

where the binary number $M3M2M1M0$, has to be first converted into a decimal number, as shown in the following calculation:

$$I_{modulation} = 6.4mA + 0.4mA \times 0 = 6.4mA.$$

The equations for calculating bias current and peaking voltage are shown as follows:

$$I_{bias} = 2mA + 1mA \times (B3B2B1B0),$$

$$V_{peaking} = 1.47V + 0.0323V \times (V5V4V3V2V1).$$

By using the same procedure, convert the sub-leading (second) digit of the hexadecimal number "041F" into the binary number "0100" for the inputs of $B3B2B1B0$. The binary number "0100" is equal to the decimal number "4". Then the value of the bias current can be calculated as follows:

$$I_{bias} = 2mA + 1mA \times 4 = 6mA,$$

converting the third digit of the hexadecimal number "041F" into the binary number "0001" and use the fourth digit of this binary number as the value of $V5$. The trailing (fourth) digit of the hexadecimal number is equal to the binary number "1111". This four-digit binary number is the input of $V4V3V2V1$. Then we have $V5V4V3V2V1$ as "11111" in binary form. By converting this binary number "11111" into the decimal number "31", the peaking voltage can be calculated as follows:

$$V_{peaking} = 1.47V + 0.0323V \times 31 = 2.47V.$$

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IV.1.3 Quality assurance test procedure of MTx modules

All MTx modules have been tested for reading and writing functionality of I^2C and eye diagrams measured at 8.5 Gbps. Fig. IV.4 shows the working bench for quality assurance tests, including a DC power supply (IT6322B) to provide 3.3 V and 2.5V to the carrier board, a 10 Gbps dual channel Bit Error Rate Tester (BERT) to generate a series of logical ones and zeros for testing, a carrier board, an optical loss tester to measure optical power, an oscilloscope (DSA8300) to generate eye diagrams, and two computers to run I^2C and BERT programs respectively.

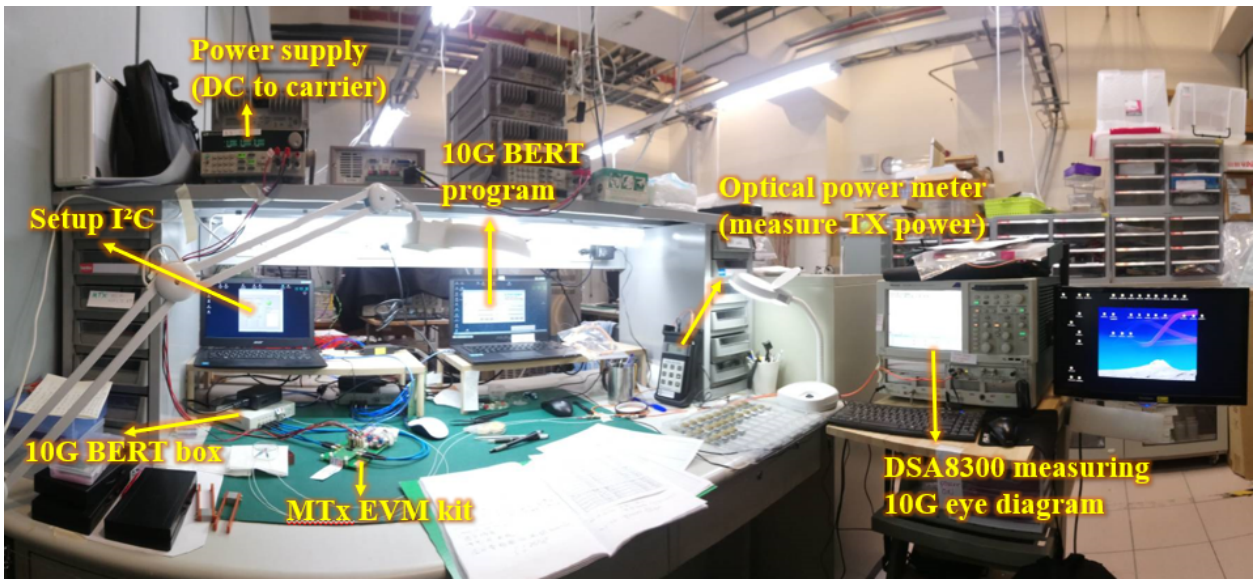

Figure IV.4: Working bench for quality assurance tests.

The following steps summarize the quality assurance procedure of MTx modules:

1. Mount a MTx module to the carrier board. (Before plugging or unplugging the module, make sure that the DC power supply has been turned off to avoid hot swapping.)

2. Turn on the DC power supply and check the reading of currents. Normally the current of 3.3 V is around 0.14 A and the current of 2.5 V is around

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0.014 A.

3. Run the I^2C program in the computer to set I^2C configure values and check the read back values.

4. Plug two fibres in the channel 1 and 2 of the module respectively and then run the BERT program in the computer to check the bit error rate.

The setup of the BERT box is shown in Fig. IV.5. The BERT box transmits electrical signals to the module and receives optical signals from the module. The BERT program interface is shown in Fig. IV.6. If a bit of output signals is not at the same logical level as it' s returning input signal, the program will identify this as an error. The total error indicates the total number of errors that have been counted after the program start. The error rate indicates the number of errors per unit time. Normally, the error rate is 10^{-12}.

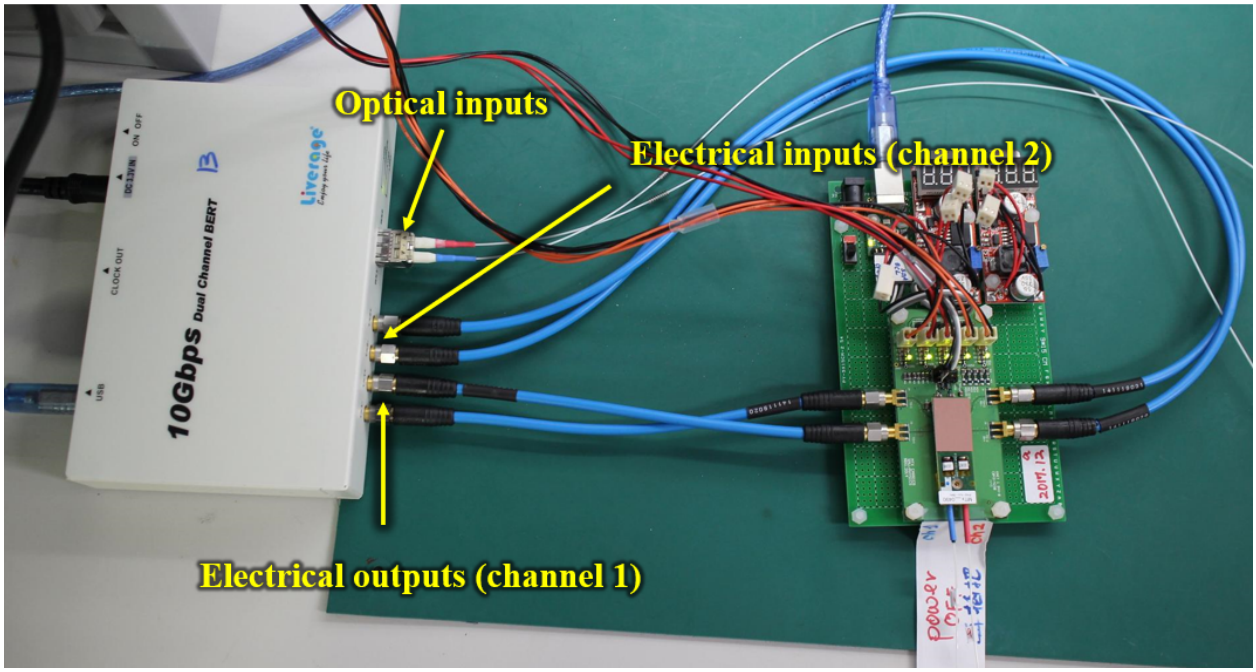

Figure IV.5: Setup of a bit-error rate test with a 10 Gbps dual channel BERT box, a carrier board and a MTx module.

doi:10.6342/NTU202003796

Figure IV.6: Interface of the BERT program on a computer including error rate, total error and time.

5. Unplug the optical fibres on the BERT and then connect these fibres to the optical loss tester for optical power measurement. (Set the wavelength of the optical loss tester to 850 nm) Normally, the values of optical power are between 600 to 900 μW.

6. Connect the fibre from the module to an oscilloscope to generate eye diagrams. (This step of MTx module quality assurance is taken by Liverage Corp. The eye diagrams of MTRx and MTX-SFP modules are measured in Academia Sinica.) An 8.5 Gbps eye diagram is shown in Fig IV.7. Some parameters of an eye diagram such as average power, extinction ratio, OMA, jitter RMS and mask margin are recorded for further analysis.

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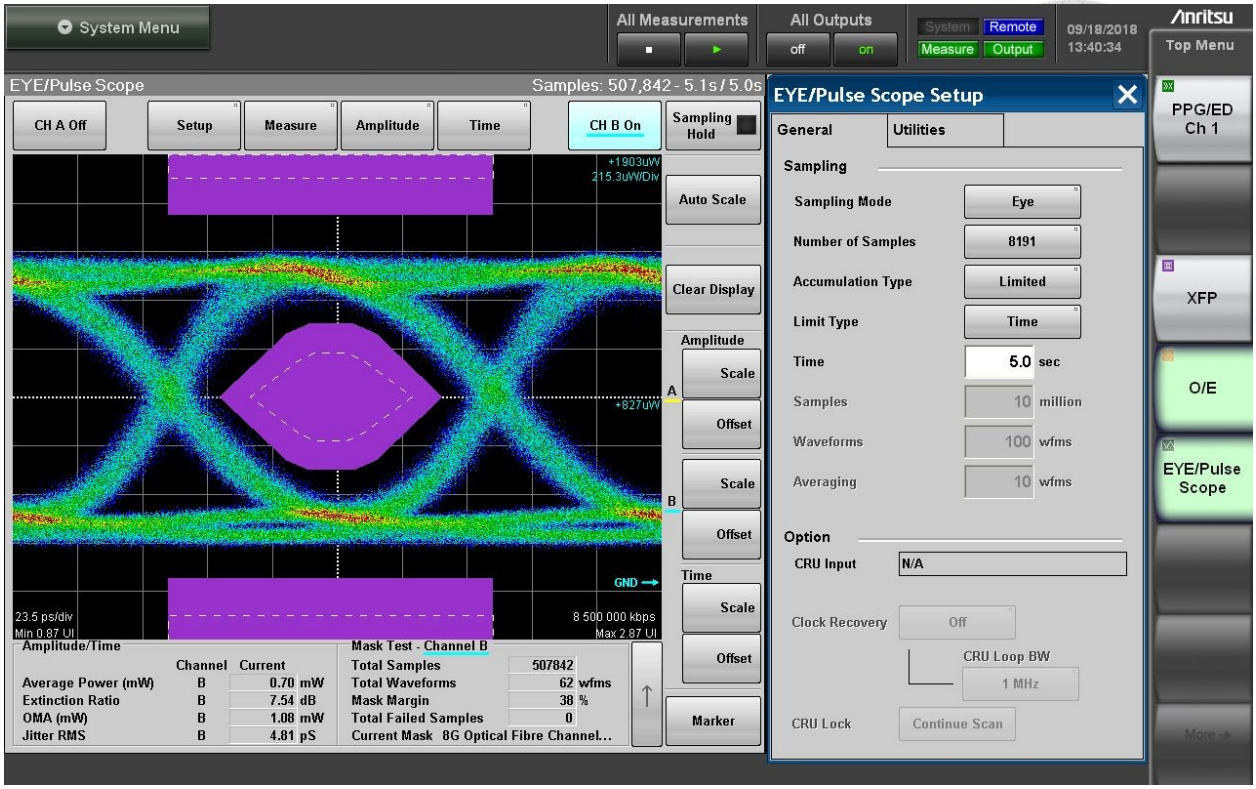

Figure IV.7: 8.5 Gbps Eye diagram of a MTx module.

IV.1.4 Analysis of eye diagrams measured in MTx quality assurance tests.

The uniformity of signal transmission performance is a strict requirement for MTx modules. To measure the uniformity of MTx modules, the eye diagram parameters of 440 MTx modules have been recorded and analysed. The eye diagrams of these modules are generated at 8.5 Gbps data rate, which is faster than the required data transmitting speed of MTx modules for the ATLAS Phase-I upgrade.

For achieving uniformity of response, TOSAs in a MTx module have been selected for approximately equal optical power at 6 mA input current. The ratio of TOSA optical power for MTx channels 1 and 2 is shown in Fig. IV. 8. The standard deviation of this ratio is within 2%. The ratios of channels 1 and 2 for AOP and OMA are shown in Figures IV.9 and IV.10, respectively. The standard deviations for these ratios are both within 4%. The main reason that causes the standard deviation to be wider than that for TOSA, is the

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systematic uncertainty produced during measurements of optical power. Such systematics are the axial tilt or transverse offset, which can cause poor coupling efficiency of light emitted from the VCSELs through TOSA lens to LC ferrules. The other reason that may cause the ratios of AOP and OMA to be wider, is the fluctuation of LOCld2 output bias current.

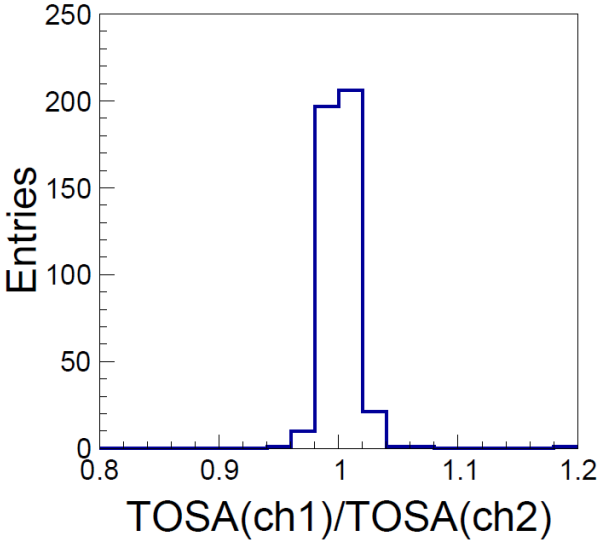

Figure IV.8: Ratio of TOSA optical power channels 1 and 2.

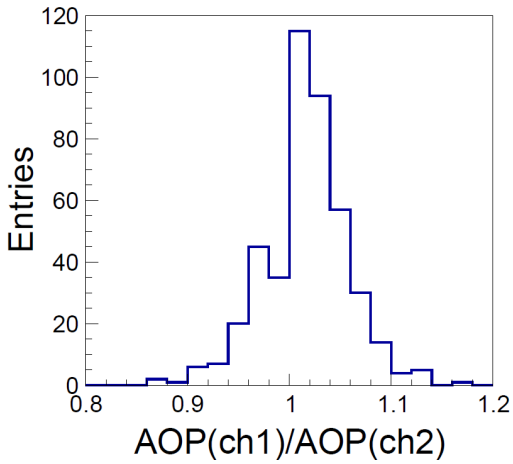

Figure IV.9: Ratio of AOP channels 1 and 2.

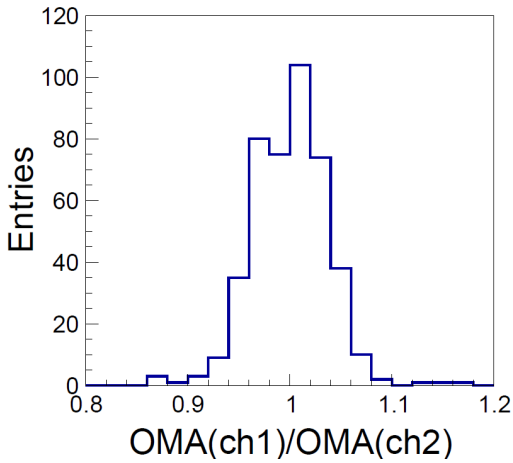

Figure IV.10: Ratio of OMA channels 1 and 2.

Figures IV.11 to IV.12 show the distributions of AOP and OMA, respectively. The values of AOP and OMA within module numbers 200 to 240 and 400 to 440 are significantly lower than the majority. The reason for this fluc-

doi:10.6342/NTU202003796

tuation of the AOP and OMA, is due to different provided batches of TOSAs, used to produce MTx modules, as shown in Fig. IV.13. For those channels that generate large fluctuations of optical outputs, one way to solve this problem is using LOCld2 chips to modulate the configuration values of those specific modules. As shown in Fig. IV.14, as the average optical power increases, the corresponding optical modulation amplitude will increase as well. This linear correlation shows that with a larger AOP, the difference between steady state "1" and "0" becomes larger and hence produces a wider vertical eye opening.

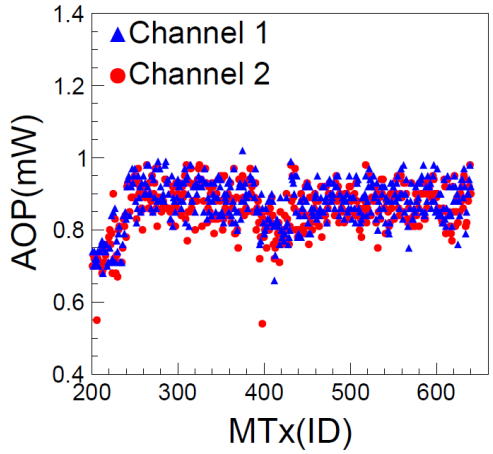

Figure IV.11: AOP distribution.

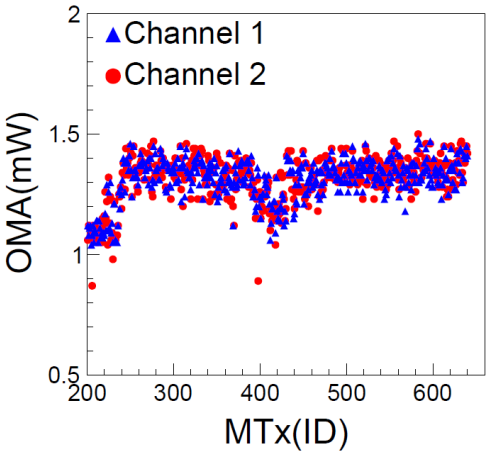

Figure IV.12: OMA distribution.

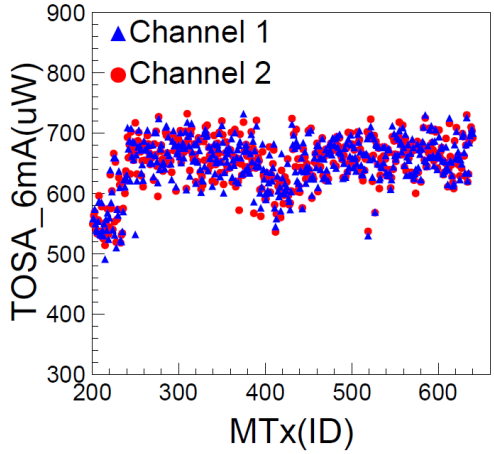

Figure IV.13: Optical power distribution of TOSAs.

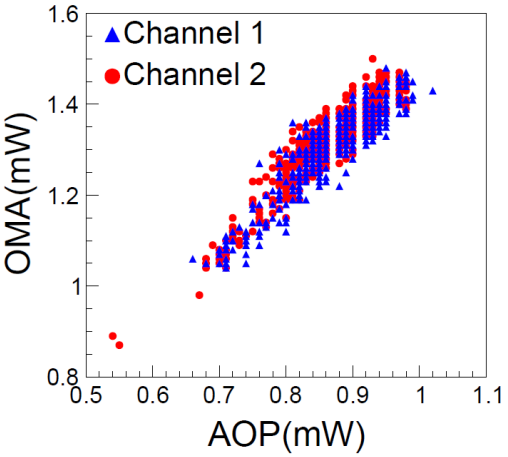

Figure IV.14: OMA versus AOP.

The other important parameter for assessing the uniformity of MTx modules, is the mask margin which indicates the opening of eye patterns without

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any noise from logical "0" and "1" level hitting the mask. The mask margin of this batch of MTx modules is around 39% before the first mask hit and has a standard deviation of 4.9%, as shown in Fig. IV.15. Fig. IV.16 shows a mask margin distribution of 440 MTx modules.

Jitters of these modules are shown in Fig. IV.17. There is one data point of jitter that is particularly high, around 12 ps. This data point is produced by the channel 1 of MTx module ID 442. The eye diagram of this channel is illustrated in Fig. IV.18, where a clear double line appears in the middle of the eye diagram.

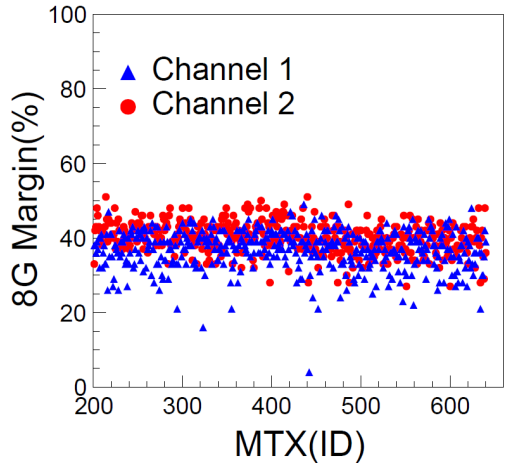

Figure IV.15: Mask margins versus MTx module IDs.

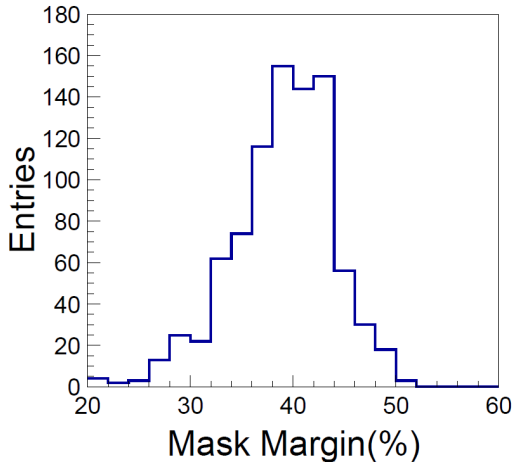

Figure IV.16: Mask margin distribution.

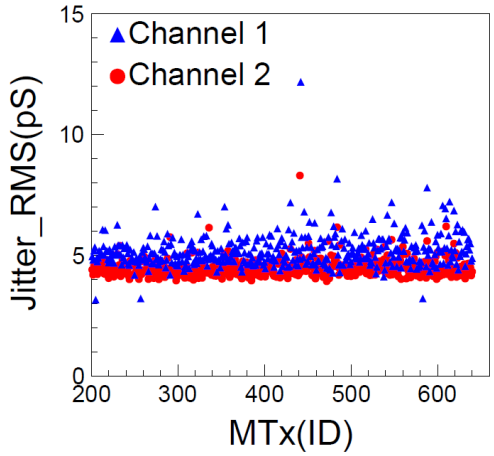

Figure IV.17: Jitters versus MTx module IDs.

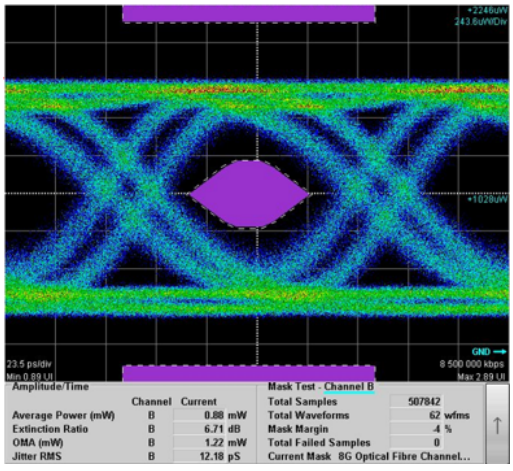

Figure IV.18: Eye diagram of MTx0442 channel 1.

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The mean and standard deviation of AOPs, OMAs, TOSA light at 6 mA, mask margins, jitters, extinction ratios, ratios of AOP channels 1 and 2, ratios of OMA channels 1 and 2 and ratios of TOSA light channels 1 and 2 for the tested 440 MTx modules, are listed in the following table, IV.4.

MTx		
	Mean	Standard Deviation
AOP (mW)	0.87	0.07
OMA (mW)	1.31	0.09
TOSA light at 6 mA (uW)	649.49	43.17
Mask Margin(%)	38.47	5.08
Jitter RMS (pS)	4.82	0.66
Extinction Ratio (dB)	7.53	0.34
AOP Ch1 (mW)	0.87	0.07
AOP Ch2 (mW)	0.86	0.07
OMA Ch1 (mW)	1.31	0.09
OMA Ch2 (mW)	1.31	0.10
TOSA light at 6 mA Ch1 (uW)	649.61	43.11
TOSA light at 6 mA Ch2 (uW)	649.38	43.23
Mask margin Ch1 (%)	36.78	5.30
Mask margin Ch2(%)	40.16	4.22
Jitter RMS Ch1 (pS)	5.17	0.69
Jitter RMS Ch2 (pS)	4.47	0.39
Extinction Ratio Ch1 (dB)	7.47	0.34
Extinction Ratio Ch2 (dB)	7.59	0.33
AOP (Ch1/Ch2)	1.02	0.05
OMA (Ch1/Ch2)	1.00	0.04
TOSA light at 6 mA (Ch1/Ch2)	1.00	0.02

Table IV.4: Means and standard deviations of measured MTx parameters.

IV.2 Quality assurance and eye-diagram analysis of MTRx modules

MTRx modules have the same quality assurance procedure for transmitter channels by using the same carrier board and I^2C configuration values, "041F". The eye diagrams of these transmitter channels have been tested in Academia Sinica by an oscilloscope (DSA8300) at 10 Gbps. A typical eye diagram of a MTRx transmitter channel is shown in Fig. IV.19. For the tests of the

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receiver part of MTRx channels, optical outputs of a MTRx transmitter channel are looped back to the receiver channel to generate electrical eye diagrams at 5.12 Gbps (This part of tests has been performed by SMU). Analysis for the parameters of transmitter channel outputs of 500 MTRx modules are given in this section.

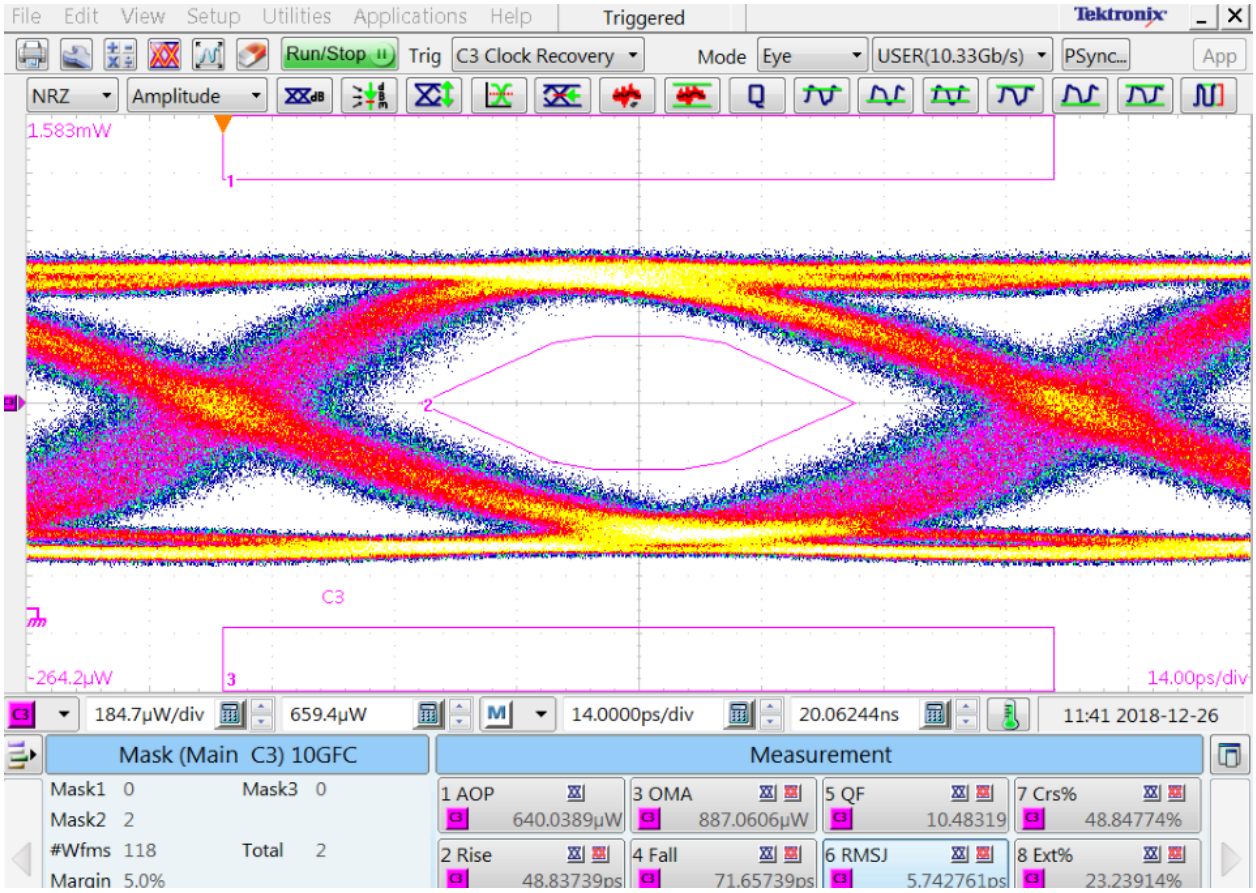

Figure IV.19: Eye diagram of a MTRx transmitter channel.

Figures IV.20 to IV.23 show distributions of AOP, OMA, TX power and TOSA optical power. The TX power is the optical power measured by connecting an optical fibre from a transmitter channel of a MTRx module to the optical loss tester. The TOSA optical power is the optical power measured by using a photo detector to detect light emitted from TOSAs at 6 mA input current. The distributions of AOP and TX power have larger standard deviation than the optical power distribution of TOSAs. This is caused by the current deviation of LOCld2 chips and measurement systematics. As shown in Fig. IV.24, OMA

doi:10.6342/NTU202003796

and AOP for MTRx transmitter channels also show linear correlation as the MTx modules.

The average optical power measured by the oscilloscope (DSA8300) is presumably consistent with the optical power measured from the optical loss tester. AOP and TX power have a linear dependence, as shown in Fig. IV.25. Comparing Fig. IV.20 with Fig. IV.22, the values of AOP are about 30% lower than TX power values. The reason is a shift of optical power between AOP and TX power distribution due to insufficient calibration of the oscilloscope.

TOSA optical power and TX power have a linear correlation as well, as shown in Fig. IV.26. There are a few data points which show high TOSA optical power with relatively low TX power, TX power < 700, that do not agree with the linear correlation, observed in the majority. These points are believed to be due to poor fibre coupling.

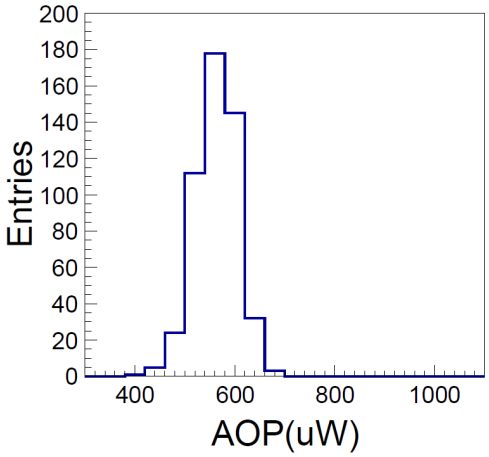

Figure IV.20: AOP distribution.

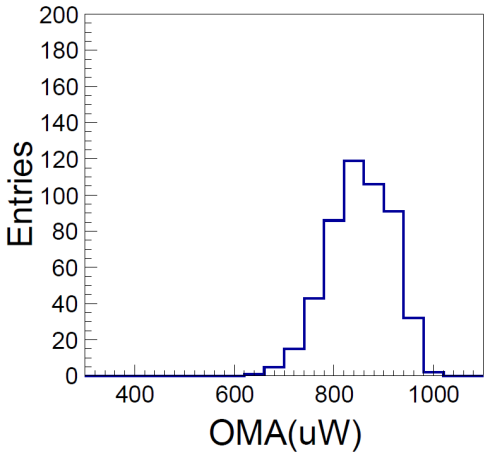

Figure IV.21: OMA distribution.

doi:10.6342/NTU202003796

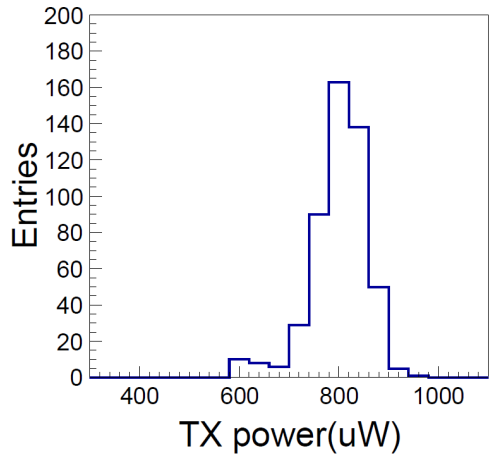

Figure IV. 22: Distribution of optical power measured by an optical loss tester.

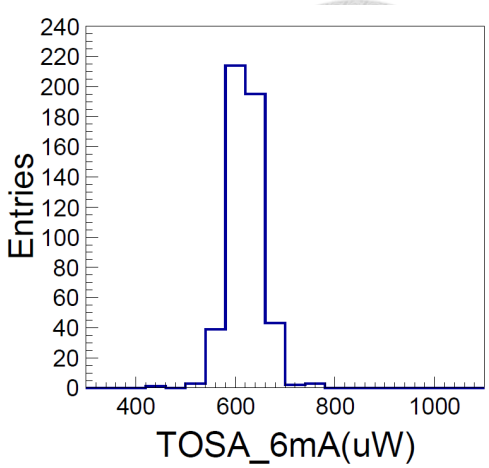

Figure IV.23: Distribution of TOSA optical power at 6 mA.

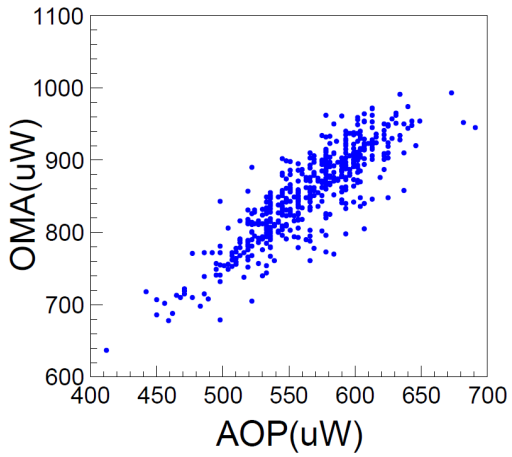

Figure IV.24: OMA versus AOP.

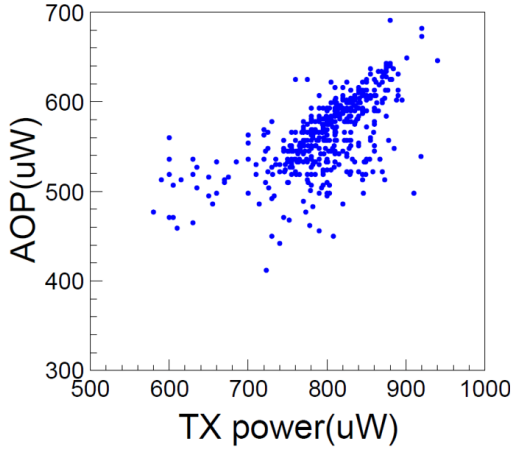

Figure IV.25: AOP versus optical power measured by an optical loss tester.

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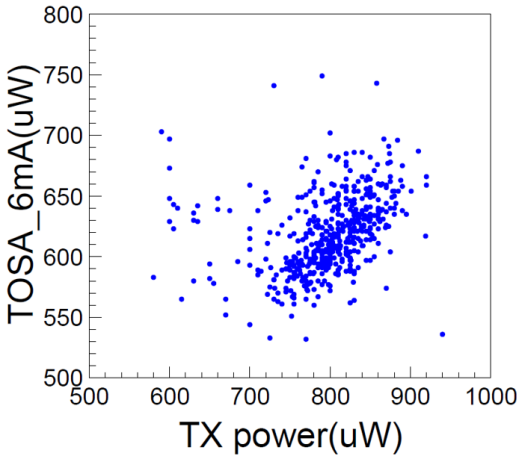

Figure IV.26: TOSA optical power versus optical power measured by an optical loss tester.

The means and standard deviations of AOPs, OMAs, TX powers, TOSA lights at 6 mA for the tested 500 MTRx modules are listed in the following table, IV.5.

	MTRx	
	Mean	Standard Deviation
AOP (uW)	563.78	40.03
OMA (uW)	851.88	61.97
TX power (uW)	797.89	56.54
TOSA light at 6 mA (uW)	619.31	32.83

Table IV.5: Means and standard deviations of measured MTRx parameters.

IV.3 Quality assurance and eye-diagram analysis of MTx-SFP modules

The quality assurance procedure of MTx-SFP modules is the same as the procedures for the transmitting channels of MTx and MTRx modules, albeit with a different carrier board to connect the SFP type of MTx modules, as shown in Fig. IV.27. This carrier board has the same functionality as the carrier board used to test the MTx and MTRx. Data were recorded from the quality assurance process for analysis, including optical power of TOSAs, TX power, AOP and OMA. The Eye diagrams for MTX-SFP modules were generated at 10 Gbps. Modules that have AOP less than 500 µW or TX power

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less than 550 µW are classified as B grade modules. A typical eye diagram for a MTX-SFP module is shown in Fig. IV.28. The following content of this section provides the analysis of 658 MTX-SFP modules.

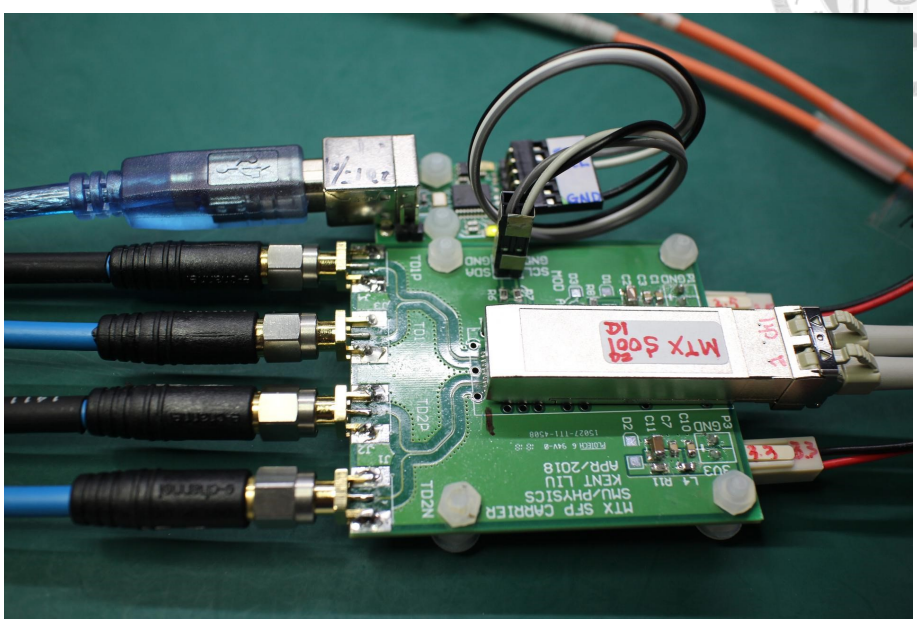

Figure IV.27: The Carrier board for quality assurance tests of MTx-SFP modules.

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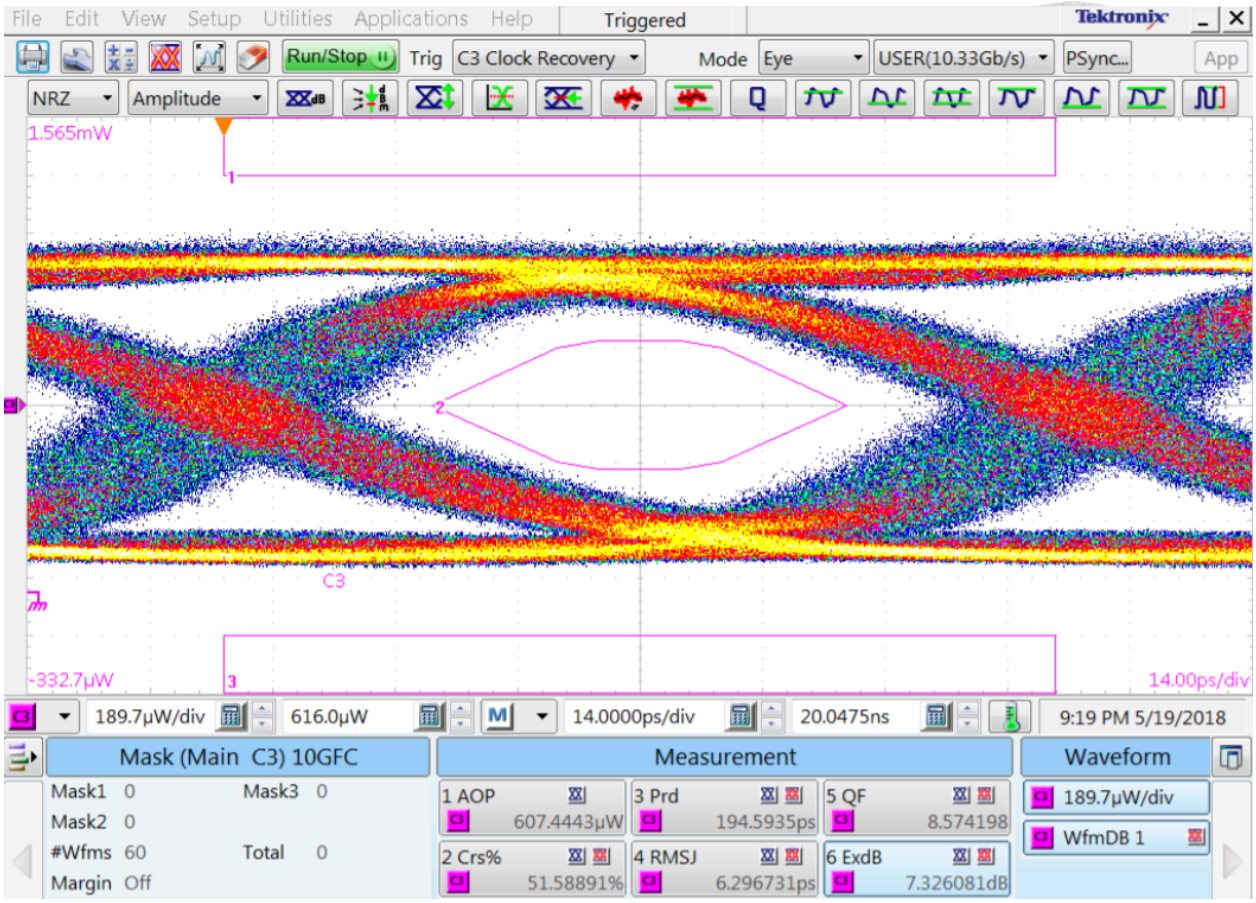

Figure IV.28: Eye diagram of a MTx-SFP module.

The correlation between OMA and AOP for MTx-SFP modules is also linear as the one for MTx and MTRx modules, as shown in Fig. IV.29 for both channels 1 and 2. As mentioned in the previous section, AOP values are supposed to be approximately equal to the TX power values. The AOP and TX power measured from MTX-SFP modules shows better linearity than MTRx modules, as shown in Fig. IV.30. This may be due to the SFP cage and LC connectors used in MTx-SFP modules, which offer a better fibre coupling efficiency than the MTRx modules.

The distributions of AOP, TX power and TOSA optical power of channels 1 and 2 for MTx-SFP are shown in Figures IV.31 to IV.36. The standard deviations of AOP and TX power are both larger than TOSA optical power due to the LOCld2 current deviation and systematic uncertainty caused by poor

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fibre coupling.

TOSAs have been paired for nearly equal VCSEL light power. As shown in Fig. IV.37, the standard deviation for the ratio of TOSA optical power channels 1 and 2 is 1%, while standard deviations for the AOP and TX power channels 1 and 2 ratios are around 8 to 9%. Comparing these values with the values in MTx modules, for the ratio of TOSAs, the standard deviations are both within 2% for MTx and MTx-SFP modules, but for the ratio of AOPs and the ratio of TX powers, the standard deviations in MTx-SFP modules are approximately two times as large as the values measured in MTx modules. This may be due to poor fibre alignment, LOCld2 current deviation or measurement systematics.

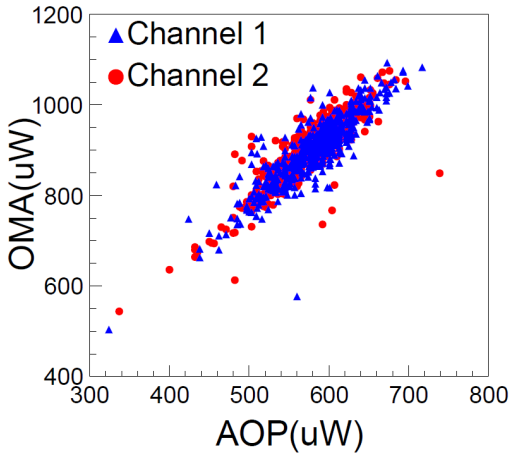

Figure IV.29: OMAs versus AOPs.

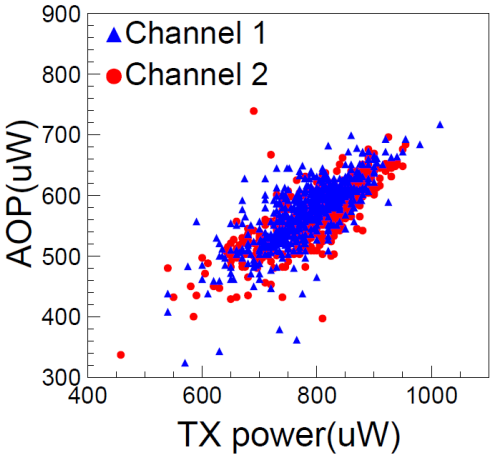

Figure IV.30: AOPs versus TX powers.

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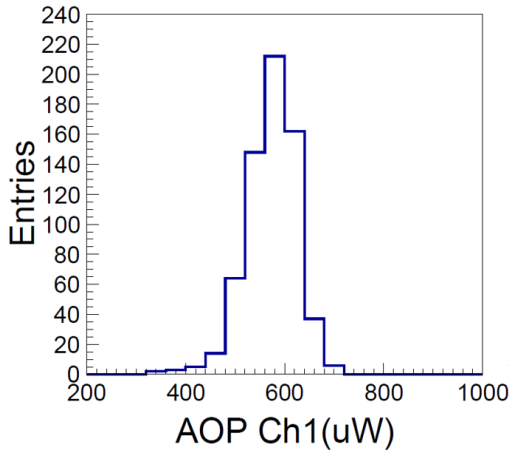

Figure IV.31: AOP distribution (channel 1).

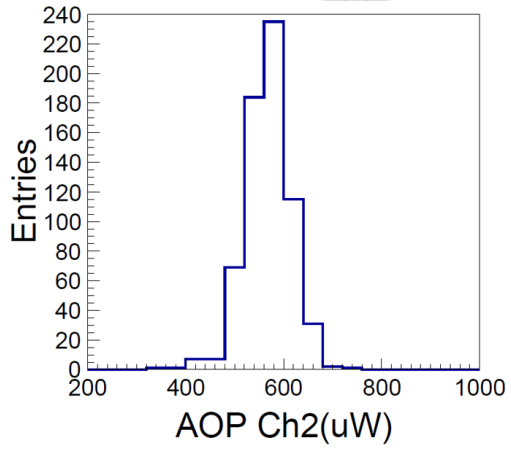

Figure IV.32: AOP distribution (channel 2).

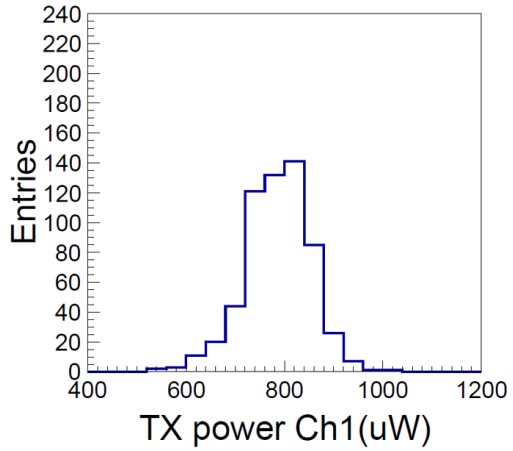

Figure IV. 33: TX power distribution (channel 1).

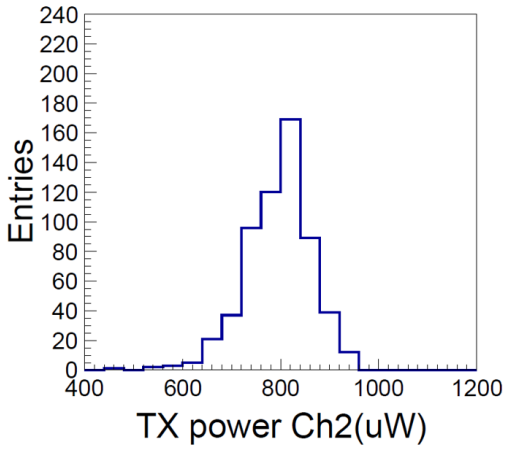

Figure IV. 34: TX power distribution (channel 2).

doi:10.6342/NTU202003796

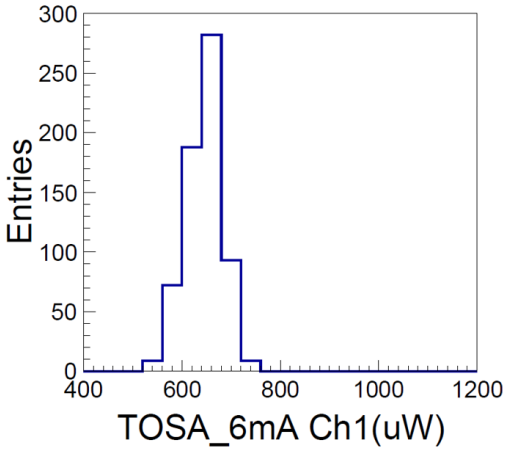

Figure IV.35: TOSA optical power distribution (channel 1).

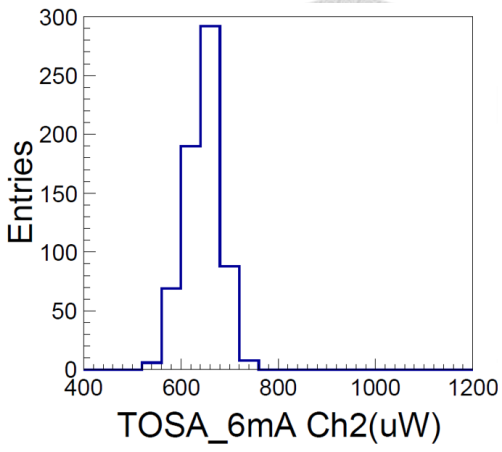

Figure IV.36: TOSA optical power distribution (channel 2).

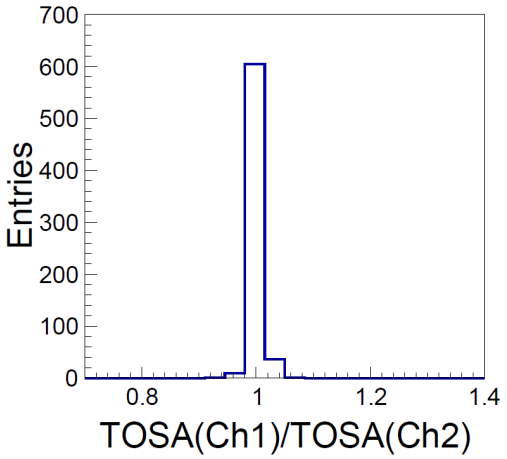

Figure IV.37: Ratio of TOSA optical powers channels 1 and 2.

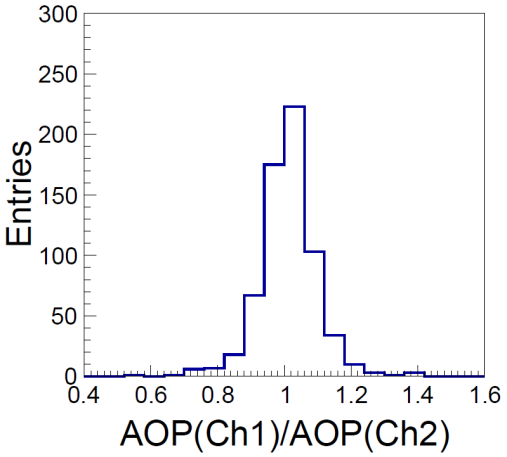

Figure IV.38: Ratio of AOP channels 1 and 2.

doi:10.6342/NTU202003796

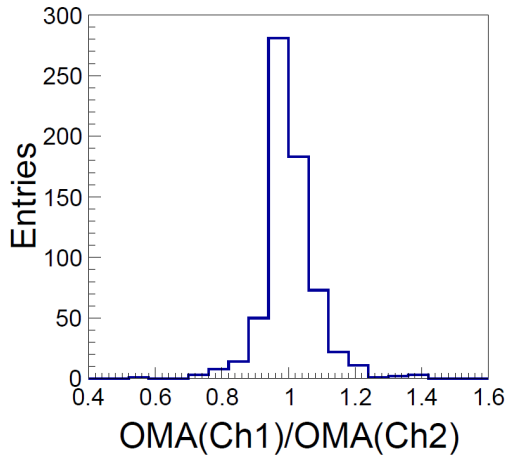

Figure IV.39: Ratio of OMA channels 1 and 2.

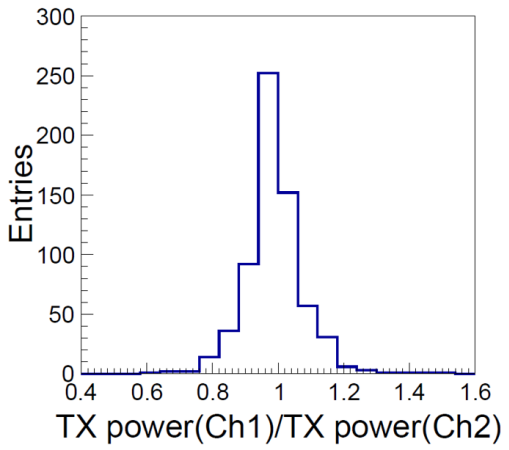

Figure IV.40: Ratio of TX power channels 1 and 2.

The means and standard deviations of AOPs, OMAs, TX powers, TOSA lights at 6 mA, ratios of AOP channels 1 and 2, ratios of OMA channels 1 and 2, ratios of TX power channels 1 and 2 and ratios of TOSA light channels 1 and 2 for the tested 658 MTx-SFP modules are listed in the following table, IV.6.

doi:10.6342/NTU202003796

MTx-SFP		
	Mean	Standard Deviation
AOP (uW)	569.33	48.08
OMA (uW)	897.82	72.27
TX power (uW)	787.53	66.86
TOSA light at 6 mA (uW)	644.65	35.10
AOP Ch1 (uW)	572.34	50.71
AOP Ch2 (uW)	566.33	45.08
OMA Ch1 (uW)	901.81	72.81
OMA Ch2 (uW)	893.83	71.51
TX power Ch1 (uW)	782.87	66.35
TX power Ch2 (uW)	792.19	67.04
TOSA light at 6 mA Ch1 (uW)	644.58	35.24
TOSA light at 6 mA Ch2 (uW)	644.72	34.96
AOP (Ch1/Ch2)	1.01	0.09
OMA (Ch1/Ch2)	1.01	0.09
TX power (Ch1/Ch2)	0.99	0.10
TOSA light at 6 mA (Ch1/Ch2)	1.00	0.01

Table IV.6: Means and standard deviations of measured MTx-SFP parameters.

IV.4 Summary

In this chapter, quality assurance procedures for MTx, MTRx and MTx-SFP modules, function definitions of the carrier board being used in the quality assurance tests, setting and calculating methods of I^2C configuration values and analysis of eye-diagram parameters, were discussed.

The I^2C configuration values have been set to "041F" for all modules in the quality assurance tests. This setting indicates that the bias current is set to be 6 mA, the modulation current is set to be 6.4 mA and the peaking voltage is set to 2.47 V. If some of the modules have optical power which is away from the majority, one of the solutions is to modify the I^2C configuration values.

The quality assurance procedures are the same for transmitting channels of all three types of modules. All procedures include tests for reading and writing functions of I^2C bus, bit error rate of data transmitting, measurements of power supply currents, optical power values by using an optical loss tester and eye-diagrams. For MTRx modules, the receiving channel of these modules

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use signals which loop back from the transmitting channel to test electrical eye-diagrams.

All of the TOSAs have been paired to approximately equal light power for channels 1 and 2 in MTx and MTx-SFP modules. The ratio of optical power for channels 1 and 2 in these two types of modules are within 2%. The AOPs, OMAs and tester-measured optical powers have larger standard deviations than the TOSA optical powers in all three types of modules. This is due to systematic uncertainty during measurements and the input current deviation of LOCls2 laser drivers. The linear correlation between AOPs and OMAs have been observed in all types of modules as well.

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V Ageing test of MTx modules

To study the ageing effect in MTx modules, 24 modules (module ID 0201 to 0224, 48 transmitter channels in total) were mounted on 3 panels, each panel carried 8 modules, for burn-in test. The setup of the test is shown in Fig. V.1. These modules were monitored in room condition (temperature around 25℃ and humidity level between 70 and 80 percent) for more than 6000 hours with no significant optical power degradation detected.

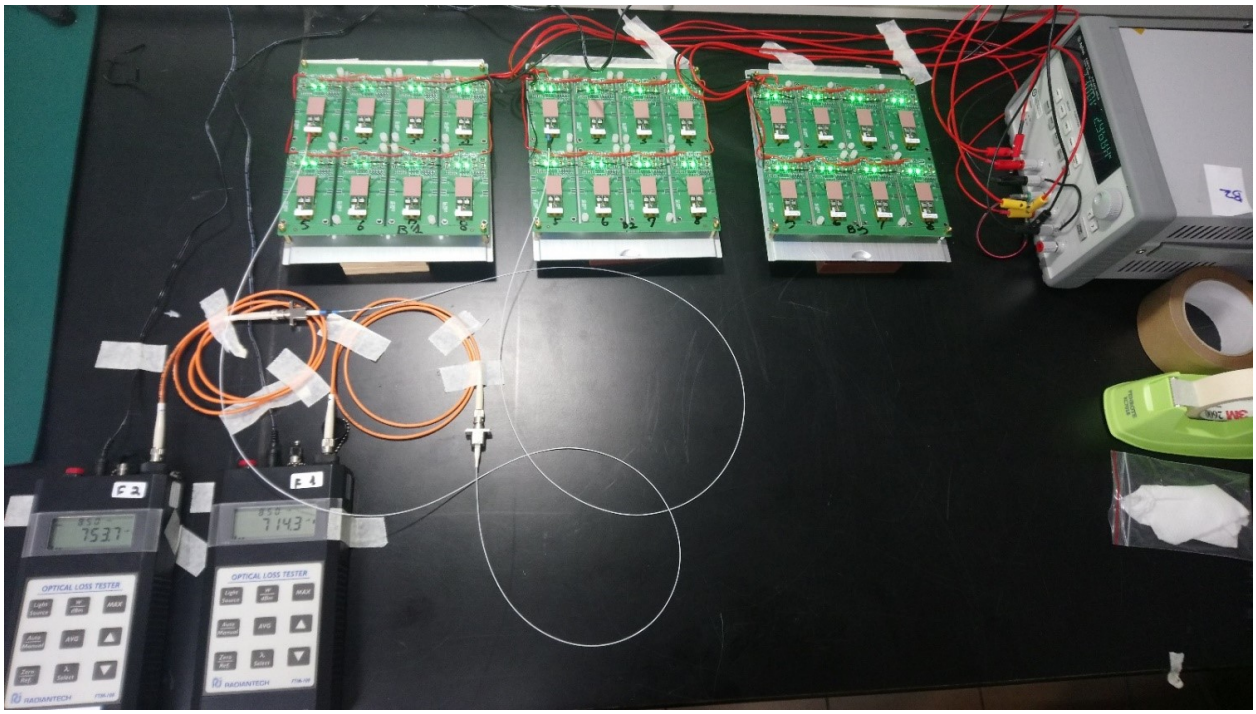

Figure V.1: Experimental setup of the Burn-in test.

The goal of the Burn-in test is to test the reliability of the modules and detect those modules which would fail in the initial, high-failure rate portion of a bathtub curve, also known as infant mortality failure, as shown in Fig. V.2 [17]. The idea is that if the period of burn-in test is sufficiently long, those modules that survive the test can then be considered mostly free of further early failures and therefore the reliability of these modules can be trusted in the long period of future operation in LAr.

doi:10.6342/NTU202003796

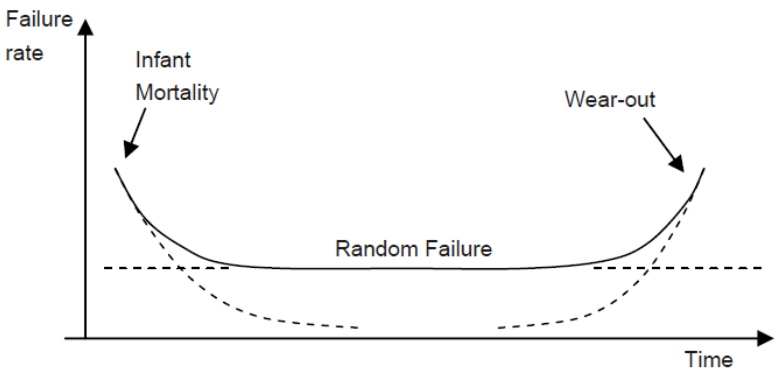

Figure V.2: A typical bathtub curve for electronics components.

During the Burn-in test, the modules have been powered by a DC power supply which provides currents to the panels. The values of these currents are 2.966 A and 0.119 A, given by 3.3 V and 2.5 V respectively. Two optical loss testers, labelled as "F1" and "F2" , have been constantly connected to two of the 48 channels via two optical fibres as samples from the 48 channels to monitor any rapid degradations of optical powers.

The optical power of all 48 channels was measured and recorded once a week using the F1 and F2 optical loss testers. Both optical loss testers have measured all 48 channels for cross checking with each other.

These modules were tested for providing the required reading and writing functionality of the I^2C configuration, the optical power via an optical loss tester, bit error rate and eye diagrams at 10 Gbps periodically in the quality assurance desk (see Fig. IV.4). AOPs and OMAs measured by eye diagrams and optical power measured via the optical loss testers, were recorded for further analysis.

Figures V.3 and V.4 display the values of monitored parameters, AOPs, OMAs and the tester-measured optical power, for over 6000 hours of testing time. During the Burn-in test, all three types of parameters for module ID 0202 in both channels have been shown to be consistent, demonstrating no sign of module malfunction due to ageing.

doi:10.6342/NTU202003796

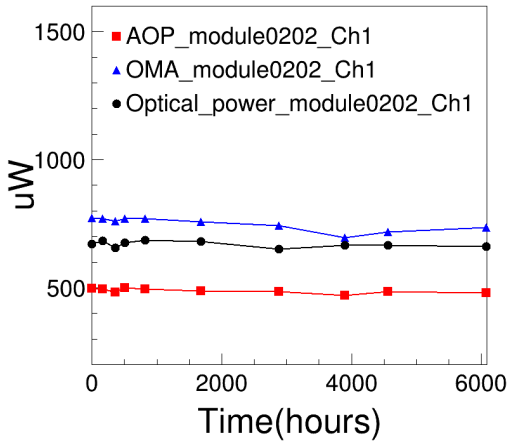

Figure V.3: AOP, OMA, Optical Power parameters versus testing time (Module 0202, Ch 1).

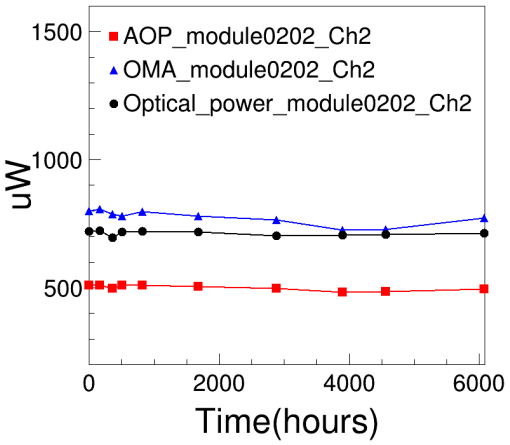

Figure V.4: AOP, OMA, Optical Power parameters versus testing time (Moudle 0202, Ch 2).

By dividing all parameters by their initial values measured at the beginning of the test, the deviation of these parameters over time can be examined. In Figures V.5 to V.10, all 24 modules are shown. In Figures V.5, V.7 and V.9, the parameters shown in black circular markers are apparently away from the majority and drop to around 0.9 to 0.8 right after the initial point. These values belong to module 0224. In Fig. V.11 we can see that all three types of parameters decrease in the first 500 hours in module 0224, however, they then stop dropping and remain stable after this point. This means that the earlier decline does not indicate module failure.

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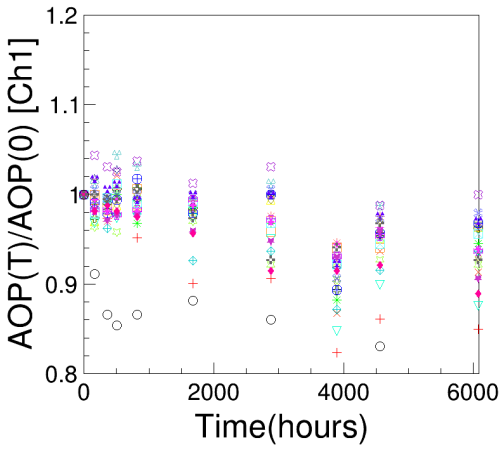

Figure V.5: Ratio of AOPs versus time (Ch 1).

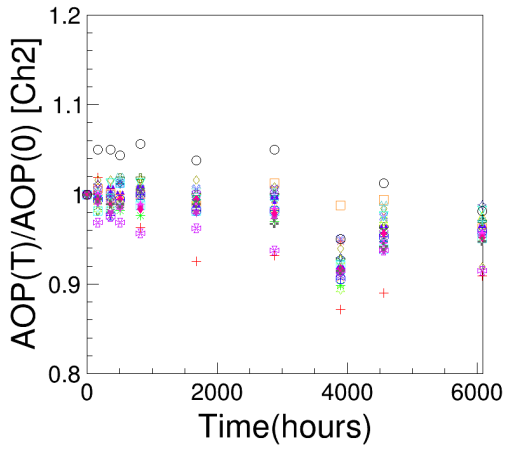

Figure V.6: Ratio of AOPs versus time (Ch 2).

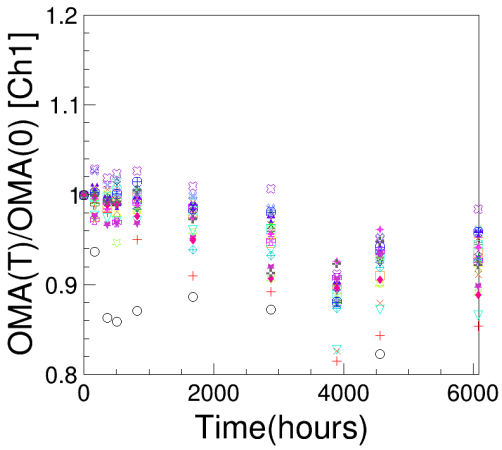

Figure V.7: Ratio of OMAs versus time (Ch 1).

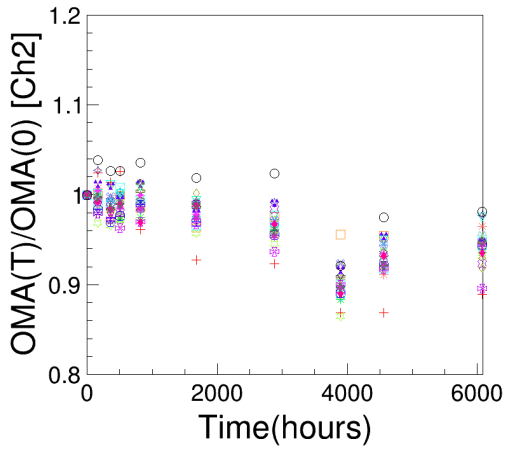

Figure V.8: Ratio of OMAs versus time (Ch 2).

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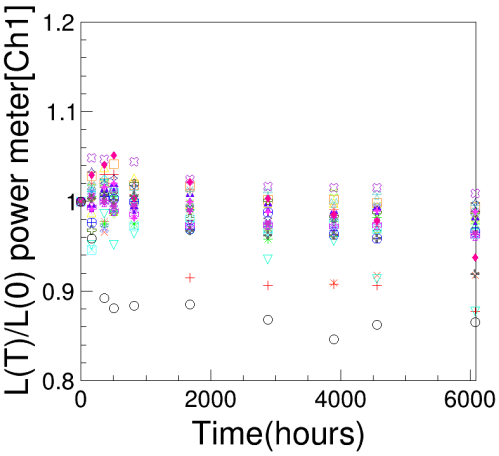

Figure V.9: Ratio of tester-measured optical powers versus time (Ch 1).

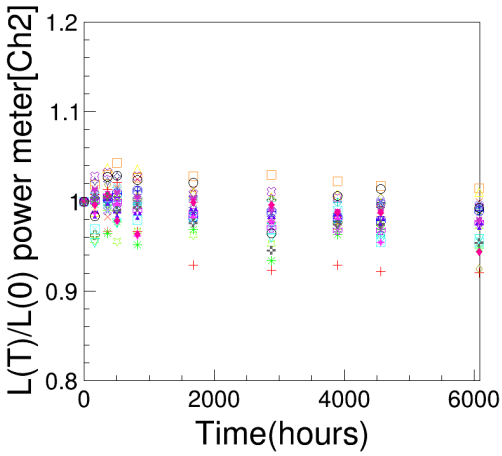

Figure V.10: Ratio of tester-measured optical powers versus time (Ch 2).

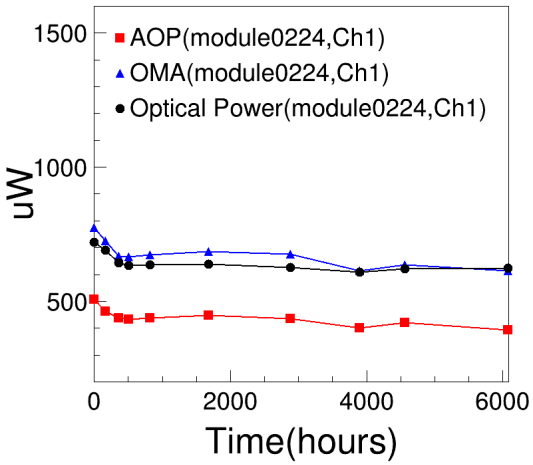

Figure V.11: Parameters versus time (module 0224, Ch 1).

For the data points on Fig. V.12, the AOP(T)/AOP(0) are calculated by taking a mean value of AOPs measured from all 48 channels and then divide this mean value by the initial mean value to illustrate the deviation of AOPs versus time compared with the initial measurements. The standard deviations of 48 channels are used as error bars for each data point in Fig. V.12. A dashed line is demonstrated as the base line on the plot.

A large drop after 4000 hours is observed in both AOP and OMA in Fig. V. 12. Since the optical power measured from the optical loss tester at 4000 hours remains normal, the problems for this drop may not be from the modules. Af-

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ter checking for other possible systematics, the reason for this degradation was found to be the fatigue of the compressing clip of the optical fibre used to measure the eye diagrams. After the drop, this fibre was replaced. Subsequently, the AOPs and OMAs values recovered to higher values.

Typically, if a MTx module is going to fail, the output light of the module will start to decrease rapidly and become completely dark within two weeks. In this case, if the optical power maintains a reasonable level for two weeks after a large decline is detected, then this decline is not caused by the deterioration of the module. The possible reasons may be a poor light coupling efficiency during measurement or the VCSEL intrinsic performance over a period of time.

According to the last data points of Fig. V.12, optical power degradation is within 5% after more than 6000 hours. These modules show no bit errors and have no sign of failures during the burn-in test.

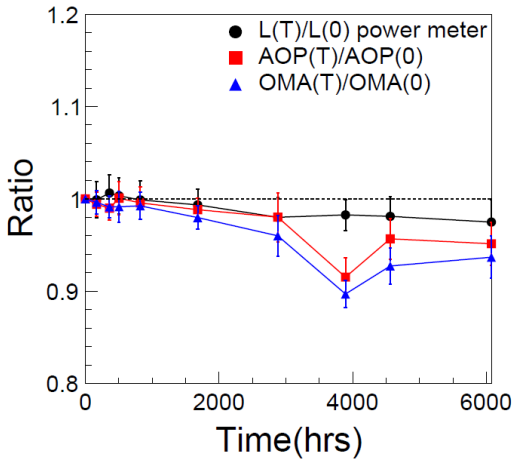

Figure V.12: Mean values of AOPs, OMAs, tester-measured optical power for 48 channels during the burn-in test with the standard deviations shown as error bars. The drop at around 4000 hours has been found to be due to fatigue of the optical fibre connector.

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VI Conclusions

The dual channel miniature optical transmitter, MTx, and transceiver, MTRx, are designed for improving the event trigger performance in the Liquid Argon (LAr) calorimeter. The small form-factor pluggable transmitter module, MTx-SFP, is designed for the forward muon New Small Wheel (NSW) detector. In order to meet the requirements for the data transmission speed (5.12 Gbps) in the ATLAS Phase-I upgrade, these modules are all optimised for high speed performance. The transmitter channels of these modules have been tested at a higher speed of 10 Gbps. The optical electronic components on these modules were tested and selected for high level of radiation tolerance to cope with the radiation dose during the high luminosity running, in HL-LHC.

The performance of the optical electronic components mounted on these modules was evaluated. Such components include VCSELs, I^2C bus, LOCld2 laser drivers, TOSAs, and ROSAs. The VCSELs are converters that change the electrical inputs into optical outputs. A I^2C bus is used as a communication device which helps LOCld2 laser drivers to control the light output of VCSELs. The LOCld2 laser driver is used to control the VCSELs by sending configuration values of bias current, modulation current and peaking voltage. In the quality assurance tests, the configuration values have been set to the same values for all modules. In a situation where the optical outputs of certain VCSELs show big deviations from the majority, customized configuration values to these specific modules, must be applied.

A TOSA is a converter to change the electrical signals into optical signals. TOSAs have a focusing lens and housing to improve light coupling efficiency to an optical fibre. The ROSA is a CERN developed optical receiver, which is used to convert optical inputs into electrical outputs. A LI curve of these TOSAs has been obtained and examined to evaluate for the performance of these TOSAs. Experiments for studying the shape of optical spectra of TOSAs, TOSAs without a focusing lens and light coming out of an optical fibre all show

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a donut-shaped optical spectrum, indicating the importance of good light coupling efficiency. A comparison between the optical spectra of TOSA and TOSA without a focusing lens, shows approximately the same far-field angle behaviour, indicating that the lens does not have a strong impact on the divergence angle of emitted light for this type of TOSAs. The optical spectrum measured from an optical fibre shows smaller far-field angle than the spectra measured from TOSAs. This may be due to the attenuation of light and due to the small acceptance angle of the optical fibre.

The assembly procedures of MTx, MTRx modules include PCB production by SMT technology, TOSA or ROSA soldering, cleaning of solder paste, latch assembly, thermal conductive pad adhering, tests for currents given from the power supply voltages, I^2C functions, 10 Gbps bit-error rate and eye diagrams. The MTx-SFP modules have a similar assembly procedure like MTx and MTRx, the differences between these procedures are that the MTx-SFP modules do not contain a thermal conductive pad, and use a metal SFP cage to hold these modules.

The quality assurance procedures of these three types of modules are the same for the transmitter channels. They include tests for reading and writing functionality of I^2C bus, 10 Gbps bit error rate, optical power measured by an optical loss tester and eye diagrams. For the receiver channels of MTRx modules, electrical eye diagrams are produced by looping light emitted from the transmitter channel, back to the receiver channel in a same module. The yield rate of MTx and MTRx modules is 98% for a total of 4650 modules tested.

The uniformity of module performance was examined by analysing the eye diagram parameters recorded from the quality assurance process. AOPs show a linear correlation with OMAs in all types of modules. The channels 1 and 2 ratios of AOPs and OMAs have larger standard deviations than the ratios of TOSAs in MTx and MTx-SFP modules and the standard deviations of AOP and OMA distributions are both higher than TOSA's in MTRx modules. These are caused by measurement systematics and bias current deviation of LOCld2

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chips. The mask margin of the MTx modules shows a good uniformity with a standard deviation of 5%.

In order to test the durability of MTx modules, 24 MTx modules were selected to a burn-in test for more than 6000 hours. These modules were monitored using eye diagrams at 10 Gbps with an oscilloscope, and optical power with an optical-loss tester, periodically. The AOPs, OMAs and the optical power measured by the optical-loss tester all show a degradation of order 5% after over 6000 hours of burn-in test.

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