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Doctoral Dissertation

適用於類比與混合訊號電路系統之時間延遲電路設計與製作

The Design and Realization of Time Delay Circuitry for Analog and Mixed-Signal Systems

林有銓

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誌謝

畢業十年後又再次回到學校拾起書本，靠的是堅持以及不斷的挑戰自我。由入學前的口試準備，入學後與一些比自己年輕十來歲的同學一同修課，以及準備資格考試、論文投稿到最後的口試。關關難過，但我還是秉持著挑戰自我的精神，一步一腳印堅持不放棄，這是對我自己的試鍊。

首先要感謝指導教授曹恆偉博士，給了我再一次挑戰自己的機會。並於學術研究上提供我諸多寶貴的意見。再來感謝我的口試委員，包括本校的盧奕璋教授、台灣科大的陳伯奇教授以及台北科大的黃育賢教授、雲林科大的黃崇禧教授與立積電子副總紀翔峰博士。在口試時給予我的指正與建議，使我的論文能夠更加完善，在未來的研究道路上也能秉持著更加專注與精實的態度來面對。

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摘要

由於 CMOS 製程不斷的演進以及操作電壓越來越低，使用傳統類比電路設計方式，要製作出低功耗以及小面積的電路變得越來越具挑戰性。因此，在一些高速但解析度要求適中的類比電路中，改用在時域中做信號處理的方式變得越來越廣泛。近年來，時間數位轉換器電路已經被廣泛應用在全數位式鎖相迴路以及時間模式的類比數位轉換器當中。在低電壓，低功率以及小面積的設計要求下，在時域中的信號處理電路在類比／混合模式電路系統中佔有著極大的優勢。

在本論文中，希望研發一些時域的信號轉換以及信號處理電路，以便應用在純類比或類比數位混合模式系統當中。首先，我們提出一種新型高速高解析度電壓對時間差轉換器電路，用以結合快閃式時間數位轉換器來實現高速類比數位轉換器。使用 0.18-μm CMOS 製程，所提出的類比數位轉換器在使用 1.8-V 操作電壓下，功耗為 16-mW。此外，在 400-MHz 的取樣頻率下量測 100-MHz 的弦波輸入信號，其信噪失真比以及無雜散動態範圍分別為 26.1 dB 以及 31.5 dB。

其次，我們提出一種新型的多相位時脈輸出電路及其在一維眼圖觀測電路的應用。使用 65nm CMOS 製程，所提出的一維眼圖觀測電路能忠實反映出接收信號眼開程度，用以協助串列接收器前端等化器作信號調適。在 10 Gbps 的資料傳輸速率下，使用 1-V 的操作電壓，量測到的功耗為 1.5-mW。佈局面積僅佔 0.027mm^2。

關鍵詞：電壓對時間轉換器，時間數位轉換器，時間模式類比數位轉換器，眼圖觀測，多相位產生器。

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Abstract

Owing to the advanced CMOS technology and downscaling supply voltage, analog circuit design in traditional voltage and current domains is becoming more and more of a challenge for both power reduction and area minimization. Time-domain signal processing is becoming increasingly prevalent in high-speed and moderate-accuracy analog circuitries. Recently, time-to-digital converters (TDCs) have been widely used in all digital PLL and time domain ADCs. An analog-type signal has to be converted to a time mode signal first and then time mode circuit TDC convert the time mode signal to digital code. The time domain processing circuits in analog circuitries will be greatly beneficial to a low-supply voltage, low power consumption and small area required design.

In this dissertation, several important time converting and processing circuits are proposed and implemented in some analog or mixed-mode circuits. First, a novel high-speed, high accuracy voltage-to-time difference converter (VTC) is presented and integrated with a flash type time-to-digital converter (TDC) to realize a high speed time-based ADC (TADC). Fabricated in a 0.18-μm CMOS technology, the proposed ADC consumes 16-mW at a 1.8-V supply voltage. Moreover, the measured signal to noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 26.1 dB

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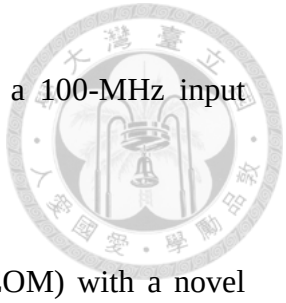

and 31.5 dB, respectively, at a 400-MHz sampling frequency for a 100-MHz input signal.

Next, an on-chip one-dimensional eye-opening monitor (1D-EOM) with a novel multi-phase clock generator circuit is proposed. Fabricated in a 65nm CMOS technology, the proposed 1D-EOM circuit can faithfully reflect the eye opening of the received data and assist the adaptations of equalizer in the front-end of a serial link receiver. The EOM circuit works at 10 Gbps data rate and its power consumption is only 1.5-mW at a 1-V supply voltage. The occupied layout area is 0.027mm^2.

***Keywords*: voltage-to-time difference converter (VTC), time-to-digital converter (TDC), time domain ADC, eye monitor, multi-phase generator.**

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Chapter 1

Introduction

1.1 Background

Due to the increasing demand of low power consumption, high operation speed, mixed-type circuit integration and small-die-area for integrated circuit, scaling down using CMOS technology is increasingly becoming dominant. Along with this trend, the speed and power consumption of digital circuits have shown significant improvement. However, designing analog circuits becomes difficult because of the drop in MOS intrinsic gain, increase in MOS leakage due to the thinning of the gate-oxide thickness, and decrease in the signal SNR, linearity, and device matching due to the reduction of supply voltage and MOS over-drive voltage. In order to overcome the above-mentioned problems, time-based or time-mode signal processing approach has been proposed [1]. By converting the voltage or current variables into corresponding time difference variables, signal processing in the analog domain is then transferred to processing in the

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digital domain, where circuit design is more robust to PVT variations.

Roberts and Ali-Bakhshian [1] present a short review of time-to-digital and digital-to-time converters (TDCs and DTCs, respectively) adopting a time-mode signal processing perspective. Moreover, some mixed-mode circuits are used to convert non-time-domain signals to time-domain signals like input signals or output signals. In Fig. 1-1 (a), if the input is an analog voltage, it can be converted into a time-difference variable by a voltage-to-time converter (VTC). After the time-mode signal processing (TMSP) in the digital domain, the time-mode signal can be converted back to a voltage signal by a time-to-voltage converter (TVC). Here, the VTC and TVC are bridging circuits and the conversion process is very critical to ensure that the converted signal is reliable. Conversely, in Fig. 1-1 (b), if the input is a digital signal, it can be converted into a time difference variable as well by a DTC circuit. After some time-mode processing, it can be converted back into the original form using a TDC circuit. Similar to VTC and TVC, the TDC and DTC design are crucial to the whole system's performance.

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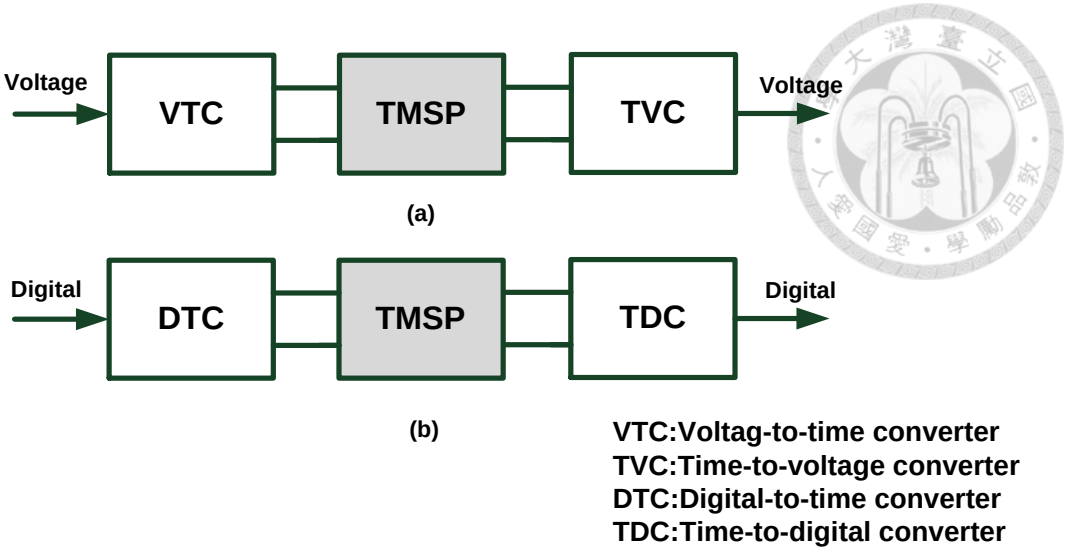

Figure 1-1 Time-Mode-Signal-Processing (TMSP) for processing analog and digital signals. (a) Voltage-in-voltage-out. (b) Digital-in-digital-out.

Due to the reasons described above, TMSP is becoming increasingly popular in several high-speed and moderate-accuracy analog circuits. For example, TDCs were used in all-digital phase-locked loops (ADPLLs) [2] and time-based analog-to-digital converters(ADCs) [3]－[6]. Again, a voltage-controlled oscillator (VCO) has been merged as a time-based quantizer in sigma-delta ADCs [7],[8]. It is a trend to convert an analog type signal to a time difference or a frequency difference signal, and then process the time domain signals using digital circuits. A growing number of published papers reporting such design in the time domain have demonstrated excellent performance compared to conventional designs in the voltage or current domain. Fig. 1-2 [7] shows a

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VCO-based quantizer circuit and the relevant signal waveforms. The operation can be understood as follows. First, a ring oscillator converts a voltage signal V_{tune} to multi-phase clock outputs continuously. Next, the multi-phase clock signals are employed to trigger counters to start counting within a fixed clock period. After that, the counter outputs are summed and the results are saved to registers. The conversion is completed within a clock cycle and the counter is then reset before starting next conversion. If the output frequency of the ring oscillator is proportional to the input voltage V_{tune}, the analog voltage is successfully quantized to the relevant digital code in nature. A ring oscillator plus some digital counters and adders perform a voltage-to-frequency conversion. The speed and accuracy of this quantizer take full advantage of modern CMOS processes since the ring oscillator's gate delay and clock phase spacing are reduced simultaneously with the process of scaling down. In addition, VCO-based quantizers can achieve first-order noise shaping of the quantization error. Although the nonlinearity in the VCO's transfer characteristic might seriously limit the resolution of VCO-based ADCs, sigma-delta feedback can be used to suppress the nonlinearity of the VCO quantizer. Consequently, VCO type quantizer has been widely adopted in continuous-time ΣΔ analog-to-digital converters. Fig. 1-3 is a proposed CT-sigma delta ADC. [7]

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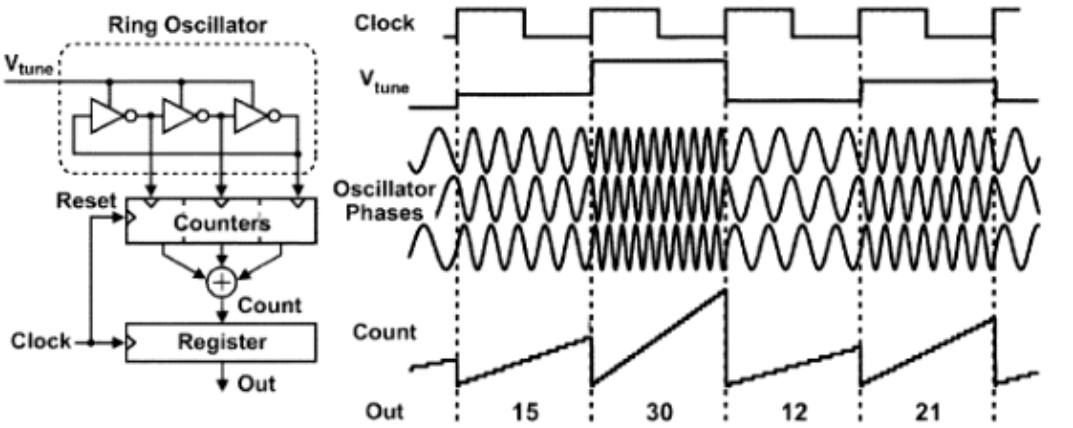

Figure 1-2 VCO employed as a quantizer [7]

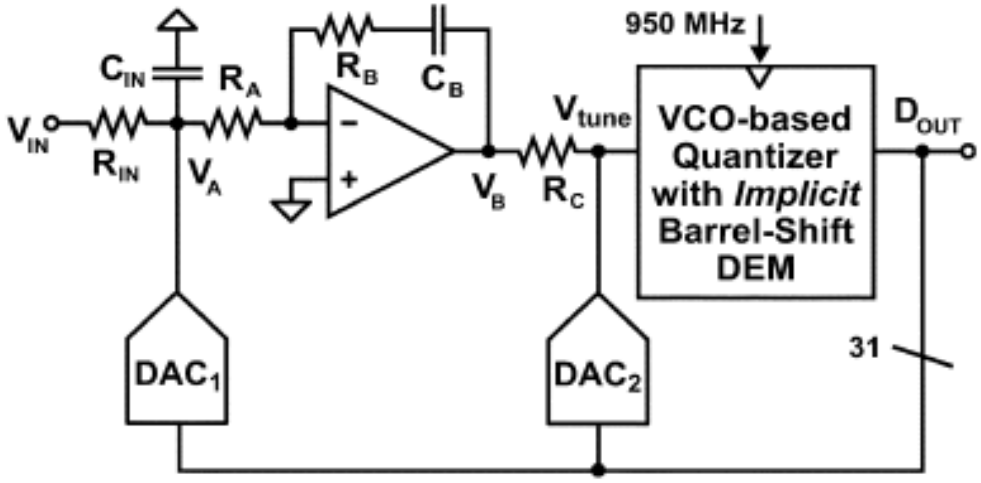

Figure 1-3 The proposed CT-sigma delta ADC [7]

Another popular example of TMSP application is the all-digital PLL circuits employing TDC. Fig. 1-4 (a) shows a simplified block diagram of a charge pump based all-digital phase-locked loop (ADPLL) [9]. It consists of a phase-to-digital converter

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(P2D), a digital loop filter, a digital controlled oscillator (DCO), and a feedback divider.

The P2D compares the phase difference between the reference clock F_{REF} and the feedback clock $F_{CKV,}$ and converts it to a digital code. This digital code is filtered by the first-order digital low-pass filter (LF) and is then used to adjust the DCO's phase or frequency. The P2D can be implemented as shown in Fig. 1-4 (b). It consists of a conventional phase/frequency detector (PFD) followed by a TDC. The PFD produces UP and DN pulses and the edge difference of UP and DN pulses is proportional to the phase error between the reference clock F_{REF} and feedback clock F_{CKV}. An L-bit TDC then digitizes the edge timing difference. The sign-bit of the TDC can also be generated according to the sampling results of the bottom D-flip flop. The operation of an ADPLL largely depends on the TDC resolution because it defines the resolution of PFD. A high-speed, high-accuracy TDC circuit (sub-gate delay resolution) design is often necessary in an ADPLL.

In Fig. 1-5, Lee et al. proposed a coarse-fine TDC design using an ADPLL [1]. It consists of an integer TDC and a sub-exponent TDC. The integer TDC is a conventional 5-bit TDC with one-bit resolution of two inverter delays. For the fractional time difference, a sub-exponent TDC to generate 1-of-n encoded 7b output with each bit representing a fraction $2^{-1},2^{-2},\ldots,2^{-6},2^{-7}$ of the two inverter delay is used. The output of a

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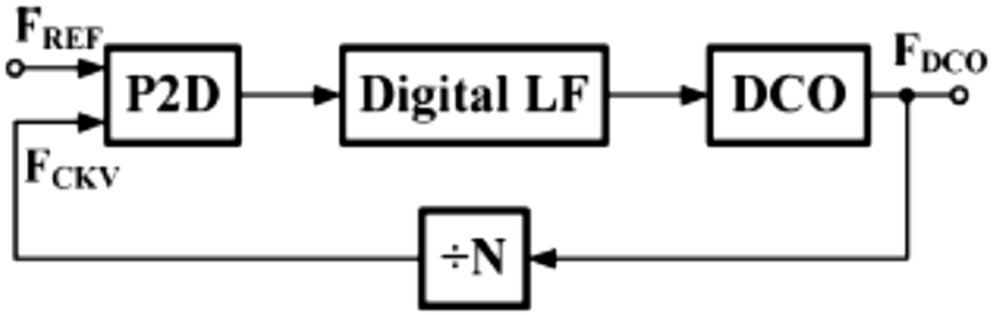
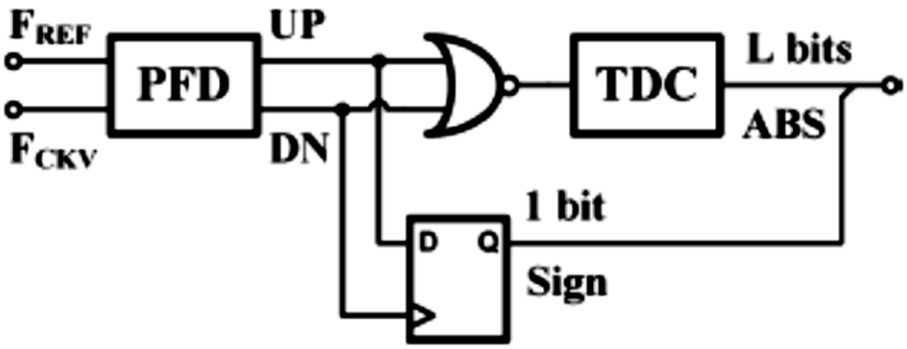
cascade of six stages of 2x time amplifiers (TAs) is tested by an integer checker. The integer checker is a one-bit TDC and outputs ONE if the input time difference is larger than τ, which is equal to one bit resolution of the integer TDC.



(a)



(b)

Figure 1-4 All-digital phase-locked loop. (a) Block diagram. (b) A P2D converter. [9]

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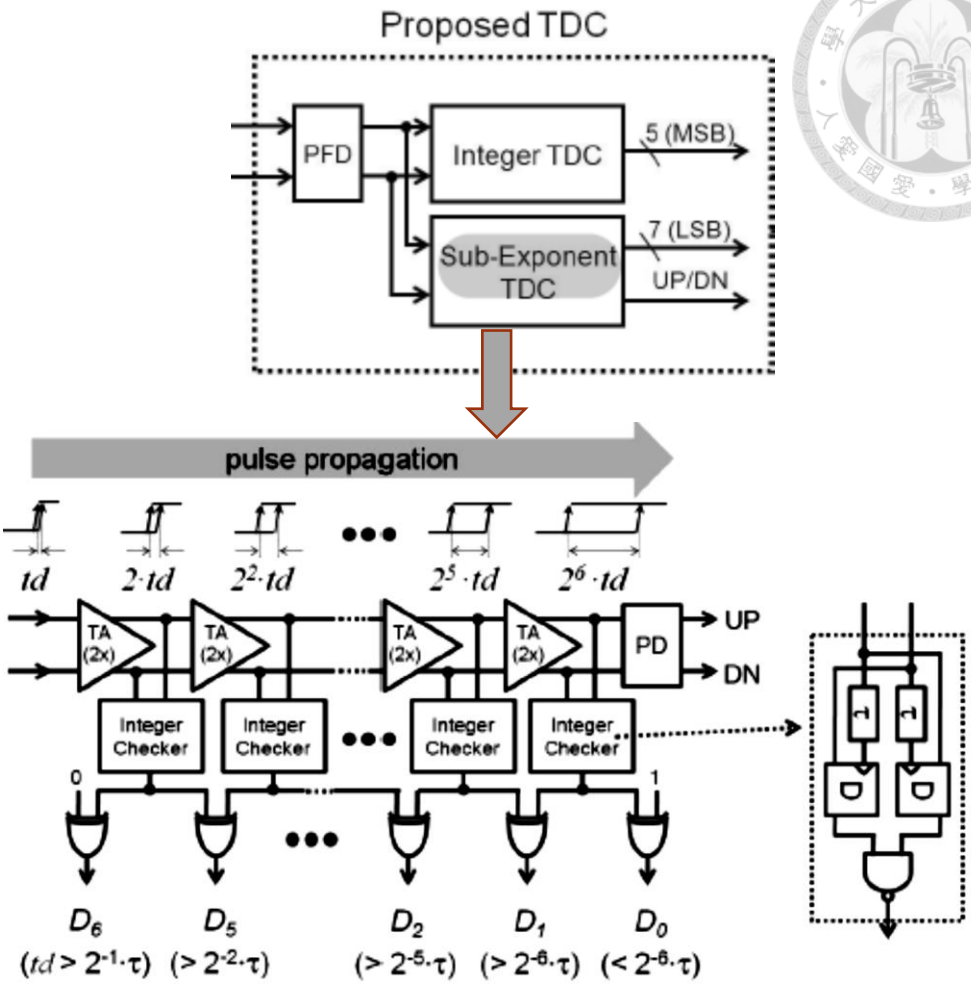

Figure 1-5 A coarse-fine TDC structure in all-digital phase-locked loop. [1]

1.2 Motivation and Research Goals

In this thesis, time mode circuits employed in two mixed-signal systems are presented and discussed. One is a high-speed time-based analog-to-digital converter system [37] and the other is an on-chip eye-opening measurement circuit for serial-link

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receiver equalizer adaptations [47]. Our research goal is to move more analog circuits to digital domain for not only power and area saving but also more robust circuit design over PVT variations.

1.2.1 Time-Base ADC System

High speed and low-to-medium resolution analog-to-digital converters (ADCs) have been widely employed in all kinds of receiver front-end such as disk drive read channel, ultra-wideband, serial links or optical communication. In these applications, power efficiency and area occupancy are often critical issues since usually there are multiple channels on the same die. Flash type ADCs have the advantage due to their simplest and fastest property. However, in conventional designs, the voltage comparators and reference circuit like resistors ladders and voltage buffers always dominate the power consumption of the whole ADC system. Folding architectures have a merit of low power dissipation but suffers from is growing load capacitance of the folder circuits which is proportional to the required resolution. Time-interleaved multi-channel ADCs are often a doable structure when speed and power are trade-off but this architecture needs more precise clock phases for sampling.

In this thesis, a time-based ADC design is proposed. An analog input voltage-type

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signal is converted to a time delay signal by a novel VTC circuit and the following flash TDC circuit then transfers this time delay to the corresponding digital code. Unlike conventional flash ADC designs, the comparator in the flash TDC is a time mode circuit like D-flip flops instead of voltage comparators. Voltage comparators often require a powerful preamplifier at its front end for amplifying a small analog signal to a logic level. The power consumption is always considerable to the whole ADC system.

1.2.2 Eye-Opening Monitor Circuit in Serial Link System

The purpose of an on-chip eye-opening monitor is to measure the eye quality information such as eye-height and eye-width of the received data before and after equalization in a serial link system. Due to the imperfect channel properties such as ISI, cross-talk, and reflection, continuous-time linear equalizer and decision feedback equalizer have widely been adopted in receiver front-end for signal equalizations.

In this thesis, a one-dimensional eye-opening monitor (1D-EOM) scheme with a novel multi-phase clock generator circuit is designed for wireline receiver front-end equalizer adaptations. The proposed multi-phase clock generator employs a simple VTC circuit without active or passive phase interpolation elements. It can provide 64 uniformly separated clock phases for sampling. For a Super Speed Universal Serial Bus

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(SuperSpeed USB) (USB3.1 Generation 2, data rate is 10Gb/s) application, the sampling phase resolution is 1.5626ps. The presented 1D-EOM consumes less power and occupies a small layout area compared to those of a traditional EOM circuit. Moreover, the measurement results show that the reported horizontal eye-opening value is proportional to the value from a real eye diagram monitor from the off-chip test buffer.

1.3 Dissertation Organizations

This dissertation is organized as follows. In chapter 2, several time mode circuits for analog and mixed-mode systems are introduced. In chapter 3, a time-domain ADC (TADC) is proposed. It consists of a delay-line-based VTC and a flash type TDC. The circuit implementation and chip measurements are also presented in this chapter. In chapter 4, an eye-opening monitor (EOM) circuit with a multi-phase clock generator is presented. A novel VTC circuit is included in this proposed EOM circuit. The VTC circuit can provide multi-phase clock outputs for EOM data sampling. The EOM circuit implementation and experimental results are also provided in this chapter. Finally, conclusion and discussions are given in chapter 5.

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Chapter 2

Time Mode Circuit in Analog and Mixed-Signal Systems

2.1 Introduction

In chapter 1, several time mode signal processing circuits in time-based ADCs (TADCs) and all-digital PLLs (ADPLLs) are introduced. In this chapter, two critical building blocks in common TADCs, a voltage to time-difference converter (VTC) and a time difference amplifier (TA) are introduced and discussed, respectively. The VTC is used for voltage to time difference conversion and TA is used for time difference amplification. Figure 2-1 (a)(b) show their the application in mixed signal systems. In Fig. 2-1 (a), a VTC is employed in the front- end of a time-based ADC. In Fig. 2-1 (b), a TA is used in a two-step TDC for amplifying MSB's residue. They are usually designed in pure analog circuits or some mixed-mode circuits. The performance of these two blocks will limit the speed and accuracy whole system. Due to this, some circuit design techniques and linearization methods in prior publications are also addressed in this

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chapter.

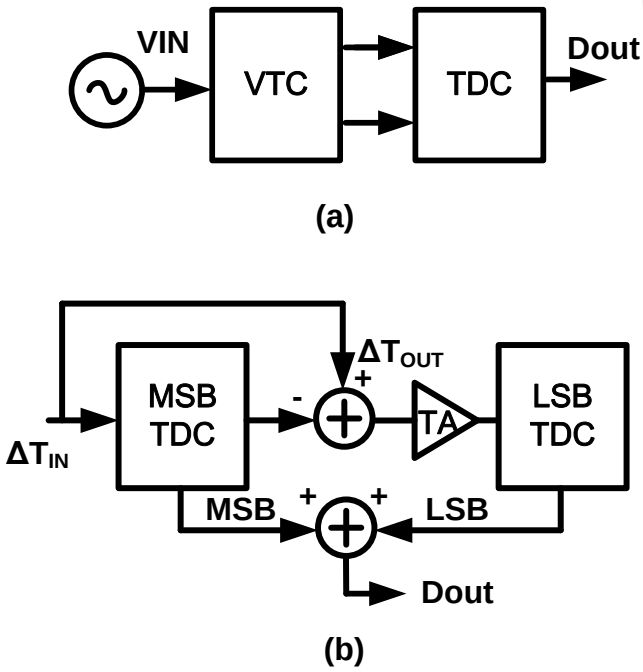

Figure 2-1 Time mode circuit in some mixed-signal systems. (a) VTC in the front-end of time-based ADC. (b) TA between two TDCs. Time mode circuit in mixed-mode system. (a) VTC in the front-end of time-based ADC. (b) TA between two TDCs.

2.2 Voltage-to-Time Difference Converter (VTC)

The voltage-to-time difference converter (VTC) is an interface circuit, transfer voltage information into time domain signals for time mode signal processing. The VTC operation is illustrated in Figs. 2-2 (a) and (b). It consists of two voltage-controlled delay units (VCDUs) and their inputs are differential voltage signals VIP and VIN. A test clock CKI input into two VCDUs and their output are delayed with respect to the

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differential voltage, resulting in the rising edge difference between two VCDU's output CKP and CKN. Assuming the two VCDUs are matched, we can write the edge difference as

$$\Delta T = (G \times VIP + d0) - (G \times VIN + d0) = G(VIP - VIN). \quad (2.1)$$

Eq. (2.1) shows the output time variable ΔT of VTC that is linearly proportional to the differential voltage input VIP minus VIN if the transfer gain of VCDUs is independent of input. G and d0 are the transfer gain and the intrinsic delay of VCDU. The output time signals can be processed by some time mode circuits like TDC, TA…etc.

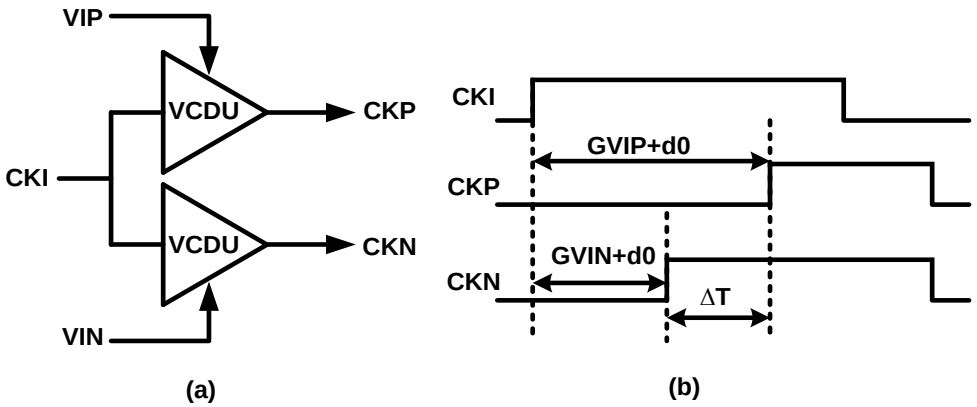

Figure 2-2 Illustrations of voltage-to-time difference conversion. (a) Block diagram (b) Timing diagram

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2.2.1 Linearization of VTC circuit

The linearity of VTC circuit will limit the input dynamic range of whole system. For example, if it is employed in the front-end of time-based ADC, its nonlinear behavior will degrade the overall ADC's performance. Due to this, several linearization methods have been proposed with an aim to enhance the linearity of the conversion. In [10] and [11], a delay-line-based ADC is proposed. Figure 2-3 (a) shows the circuit structure. It consists of a sample and hold circuit (S/H), a delay adjustment (DA) circuit and a delay-line based TDC.

A front-end S/H circuit samples the voltage input and then holds and converts it to a corresponding current signal by a degenerated differential pair amplifier DA as shown in Figure 2-3 (b) right side. The DA will output two current signals to discharge an initially pulled up capacitance in delay cells. The discharge rate is proportional to the current I over the capacitance C shown in Fig. 2.3 (c). To ensure linear conversion, the transconductance of the input NMOS differential pair M1 and M2 should be designed sufficiently large.

The sample and hold circuit is shown in the left side of Fig. 2-3 (b). Its operation is described as follow. In the sampling phase (S1~S4 are closed and S5~S8 are open), the

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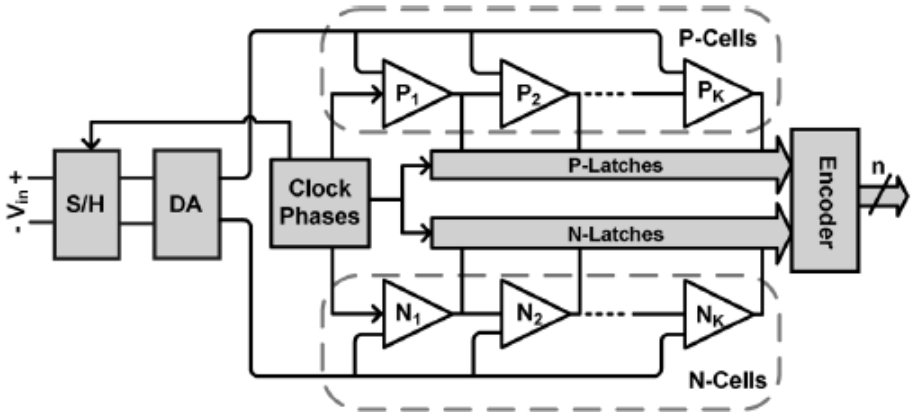
differential input Vin+ and Vin- are sampled on the top of the capacitances Cs and their bottom of the capacitances are connected to Vcm. The voltage across the top capacitor Cs is Vin_+ minus Vcm and the bottom one is Vin_- minus Vcm. In the converting phase (S1~S4 are open and S5~S8 are closed), the differential holding voltages (Vin_+−Vcm and Vin_-−Vcm) are then converted to corresponding currents (generated by diode-connected NMOS M9 and PMOS M10) to control the discharge current in delay cells (both P-cells and N-cells). Fig. 2-3 (c) is the scheme of the complete delay cell.

The delay-line-based ADC is fabricated in 65nm CMOS. The measured INL and DNL are +0.78LSB/-0.83LSB and +0.54LSB/-0.38LSB and it achieves an SNDR of 20.4dB at 1.2GS/s. The reported FOM is 196fJ/conversion step without using any calibration.



(a)

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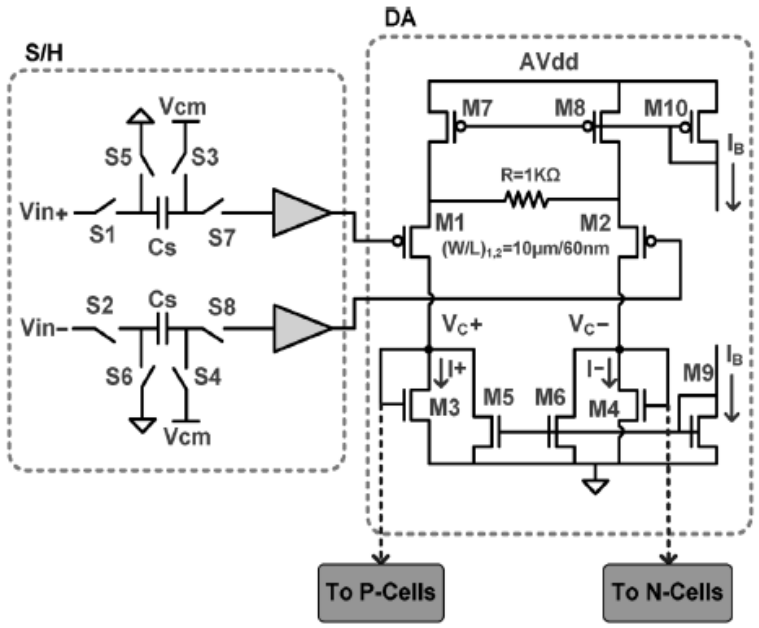

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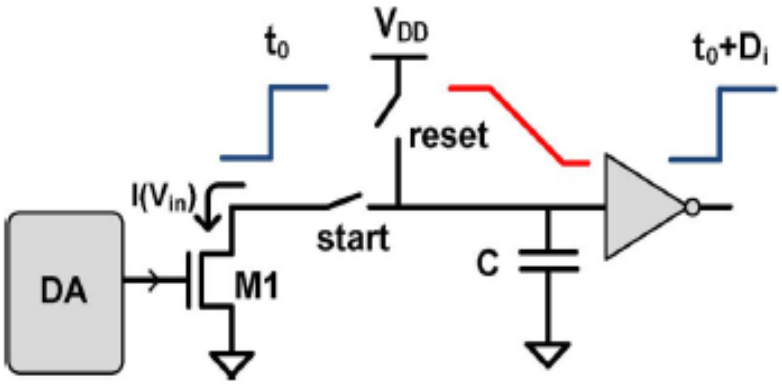

(c)

Figure 2-3 The delay-line based data converter [10].

(a) Delay-line based A/D converter implementation.

(b) Sample and hold circuit followed by a voltage to current converter.

(c) Controllable delay cells. (P-Cells and N-Cells).

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In [12], Pekau et al. proposed a current starved delay cell for voltage-to-time delay conversion. The detailed schematic is shown in Figure 2-4. Degeneration MOS (M7 and M8) and parallel staggered bias MOS (M9~M14) are combined in the discharge path of the delay cell in order to adjust its linearity. The presented VTC circuit can operate at high conversion speed but fine-tune of the staggered MOS device size is needed to obtain better linearity. This VTC is designed in a 0.13μm CMOS process and the simulation result shows the gain error is less than 2% over an input voltage range of 200mV. Input signals at frequencies up to 1GHz can be applied to the VTC without using a sample-and-hold circuit.

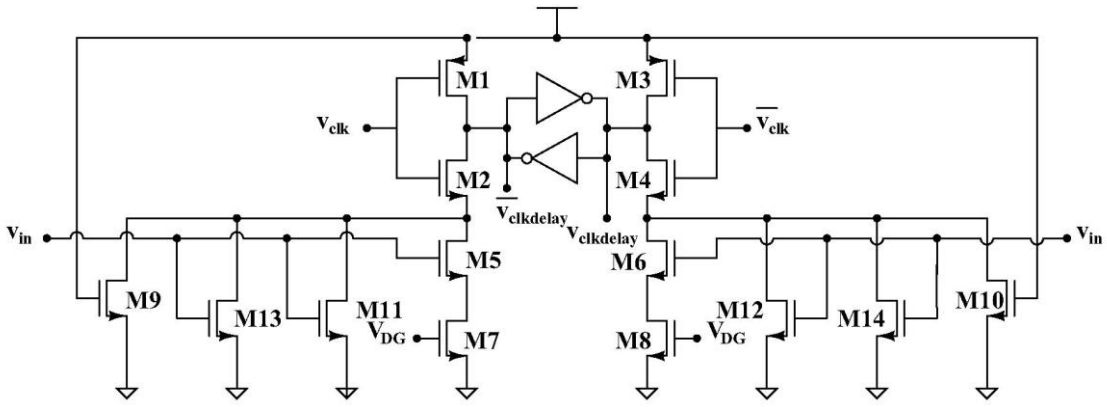

Figure 2-4 A current starved inverter with a degeneration cell and parallel bias devices [12].

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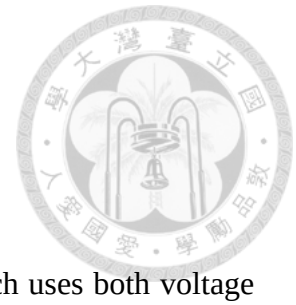

2.2.2 VTC in time-based ADC

In [13], Taehwan et al. proposed a hybrid pipelined ADC which uses both voltage and time domain information. The proposed new VTC scheme employs a scalable, power-efficient, residue voltage amplifier with minimum dc gain in its first stage while maintaining high linearity. This scheme not only reduces the power consumption of the ADC but also relaxes the design trade-off of the amplifier in a low supply voltage deep sub-micron process without sacrificing bandwidth. Figure 2-5 (a) is the proposed time-based pipelined ADC and Fig. 2-5 (b) and (c) are the conventional V-T conversion and the proposed new V-T conversion [13].

A conventional V-T conversion employed in noise-shaped two-step integration quantizer is shown in Fig. 2-5(b). The two-phase conversion results in the residue output in voltage domain after the amplification phase and is given by

$$V_o = \frac{C_S}{C_F}(V_{IN} - V_R)\frac{A}{1 + A\beta} - \frac{I_{DIS}T_o}{C_F}. \qquad (2.2)$$

Where A is the open loop dc gain of the amplifier and β is the feedback factor which is equal to $C_F/(C_S + C_F)$. The amplifier gain is not a constant and is affected by

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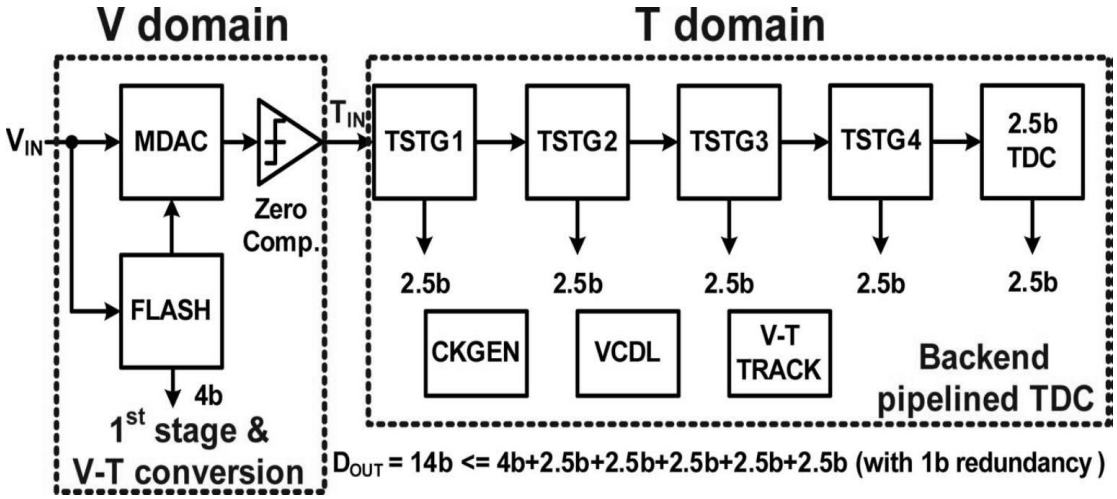
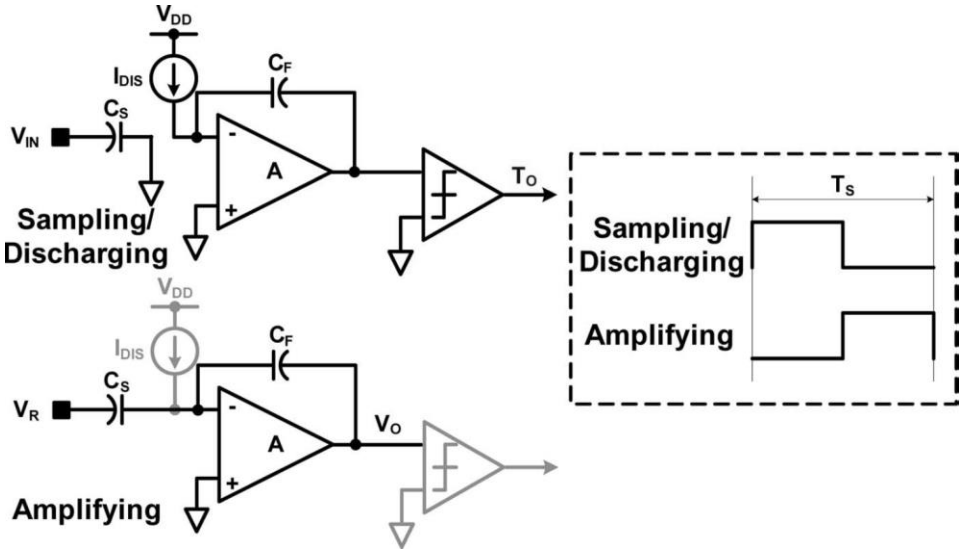
the output swing. Solving Eq. (2.2) , the time-domain output T_O at zero crossing is

$$T_o = \frac{C_S}{I_{DIS}}(V_{IN} - V_R)\frac{A}{1 + A\beta}. \quad (2.3)$$



(a)



(b)

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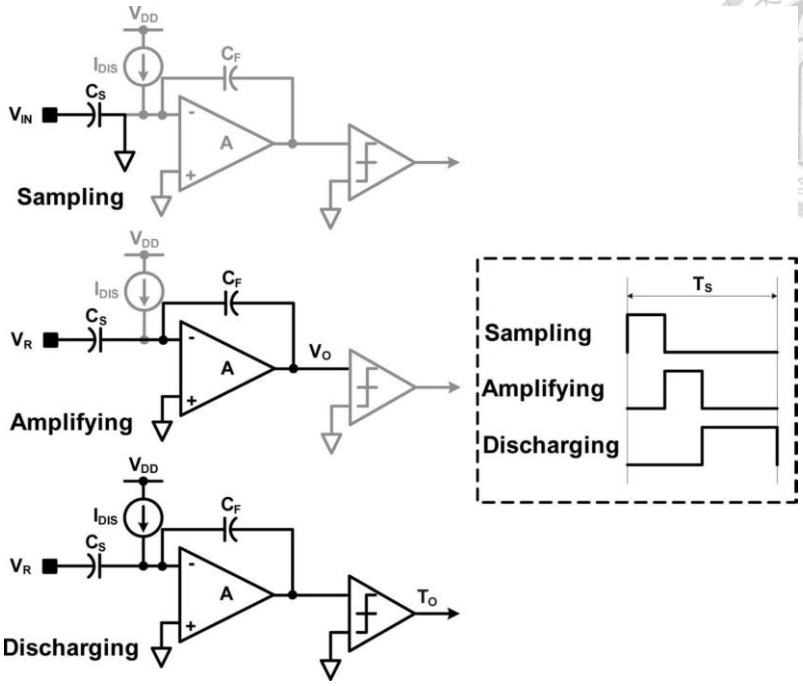

(c)

Figure 2-5 Time based pipelined ADC [13]. (a) Time based pipelined ADC implementation. (b) Conventional voltage-to-time conversion. (c) Proposed voltage-to-time conversion.

According to Eq. (2.3), a nonlinear error from the amplifier directly affects the time-domain output. Fig. 2-5 (c) shows the proposed three-phase V-to-T conversion. The charge stored in both sampling and feedback capacitors is discharged together. There is no charge loss on both capacitors and discharged together to measure the time of zero crossing. The residue output after the amplification phase is

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$$V_o = \left[\frac{C_S}{C_F}(V_{IN} - V_R) - \frac{I_{DIS}T_o}{C_F}\right]\frac{A}{1 + A\beta}\,. \tag{2.4}$$

The residue output in voltage domain is still affected by the amplifier characteristics. However, the time-domain output at zero crossing in the discharge phase is independent of the amplifier dc gain A and given by

$$T_o = \frac{C_S}{I_{DIS}}(V_{IN} - V_R)\,. \tag{2.5}$$

As a result, the time-domain output T_O is regardless of the amplifier characteristics in the proposed V-T conversion. Therefore, a low gain nonlinear amplifier can be used. Fig. 2-6 shows the linearity simulation using a residue amplifier with 24 dB open loop gain.

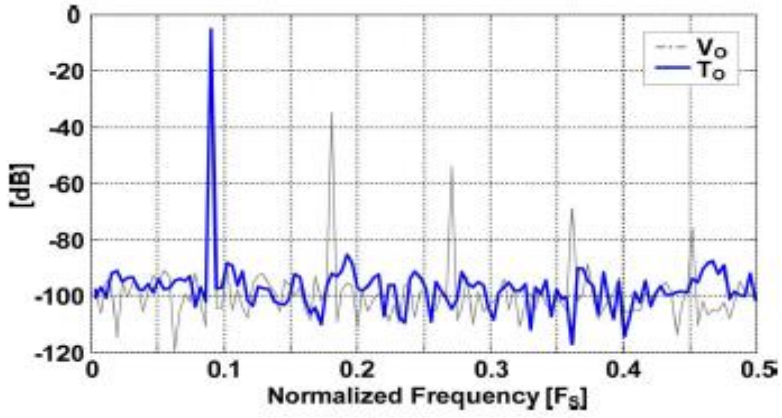

Figure 2-6 Linearity simulation of the proposed V-T conversion [13].

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2.3 Time Difference Amplifier (TA)

Low power and high resolution time-to-digital converters (TDCs) [14]－[16] have been widely used in mixed-signal circuits such as all-digital PLL (ADPLL) [17], time-domain analog-to-digital converters (ADCs) [18] － [21] and on-chip time measurement circuits [22]. To recognize a sub-gate delay time-difference signal, time-difference amplifier (TAMP) circuits have been developed in the front-ends of some TDCs to amplify a small time-difference signal. As shown in Figure 2-7, A TAMP can amplify a small time difference $\Delta\Phi_{in}$ to $\Delta\Phi_{out}$, and $\Delta\Phi_{out}$ is then fed into a LR-TDC (Low Resolution TDC) , it relaxes the resolution on TDC. Several type TAs are introduced in this section.

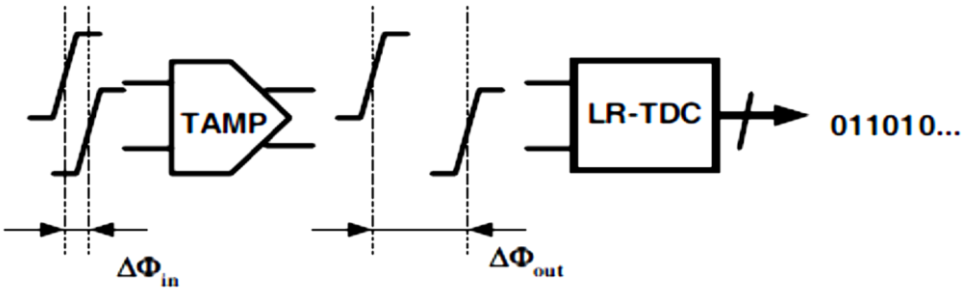

Figure 2-7 Time amplification relaxes resolution on TDC. [22]

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2.3.1 SR-Latch-type Time-Difference Amplifiers [23]

Set/reset (SR)–latch-type time-difference amplifiers [23]－[25] operating in the metastable region can amplify a very small time-difference signal (of a picosecond or sub-picosecond scale) to a sufficiently large time-difference signal (of a scale of several picoseconds). The TA was designed to facilitate improvement of TDC resolution. However, its linear range and metastable region are correlated.

The detailed circuit is presented in Figure 2-8 and relevant waveforms for inputs with small and large time-differences are presented in Figs. 2-9 (a) and (b), respectively. As shown in Fig. 2-9 (a), for a small input time-difference of T_D between *IN*A and *IN*B, the delay between *A6* and *B2* is $T_{OS} - T_D$ and that between *A2* and *B6* is $T_{OS} + T_D$, where T_{OS} is the time difference between *IN*A and A6 (or *IN*B and B6). The difference in the metastable time for *LA1* and *LB1* results in the doubling of the output delay between *Y*P and *Y*N. However, as shown in Fig. 2-9 (b), for input signals with a large time difference (T_D–T_{OS}), the delay between *A6* and *B2* is extremely small, resulting in a longer settling time for *LA1*. Consequently, the output time difference is over-amplified. As shown in Fig. 2-9 (b), the magnification ratio increases from 2 to 2.875.

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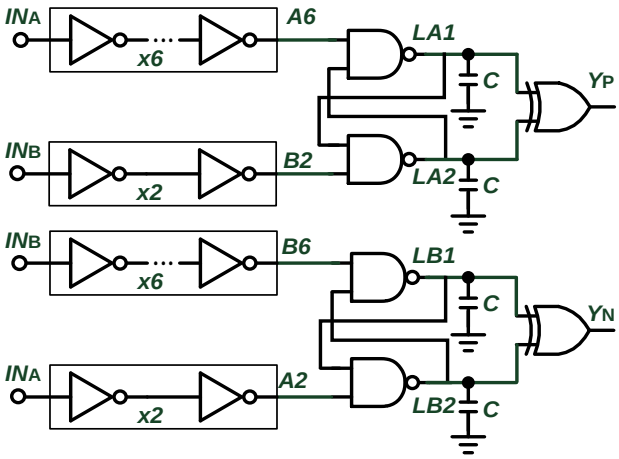
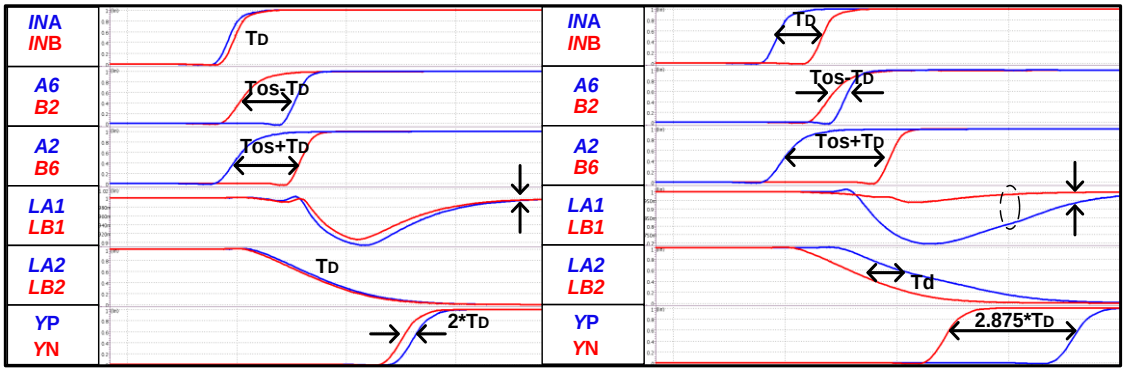


Figure 2-8 SR-latch-type TA schematic diagram.



(a) (b)

Figure 2-9 Operating principles for input signals with (a) a small time difference (T_D<<T_{OS}) and (b) a large time difference (T_D≈T_{OS}) .

2.3.2 Dependent Discharge Time-Difference Amplifier [2]

In [2], a dependent discharge time-difference amplifier is proposed which uses a cross-coupled circuit structure to get a gain of two. A simplified schematic is shown in Figure 2-10. Initially, node A and B are precharged to VDD when IN+ and IN- are low.

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OUT+ and OUT- are kept low and waiting for low to high transitions of IN+ and IN-. When IN+ or IN- rising edge occur, node A or B start to be discharged and the discharging is performed by self-inverter path (M1 or M3) and a dependent path (M2 or M4). The strength of one dependent path is determined by the discharging status of the counterpart node (M2 gate is controlled by node B and M4 gate is controlled by node A). The first transition makes the other transition slower by reducing the strength of the dependent path, resulting in an amplified time difference. Assume M1-M4 are identical, the first discharging is performed by two identical pull-down paths but the second discharging is performed by only one pull-down path. Therefore, the gain is roughly two when the IN+ and IN- rising edge are closed.

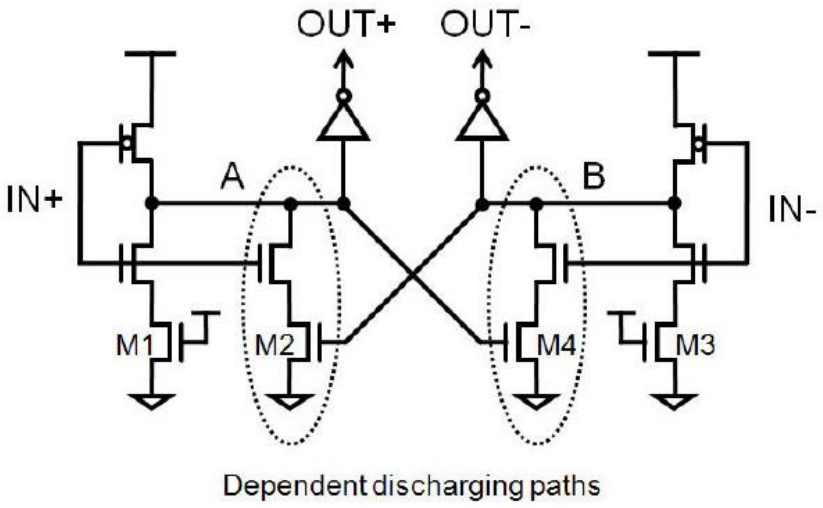

Figure 2-10 2X cross-coupled TA [2]

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2.3.3 Pulse-Train Based Time-Difference Amplifier [26]

The principle of the pulse-train based TA is illustrated in Fig. 2-11[26]. The idea is to generate N copies of pulses with the same pulse-width of Tin. It can be equivalent to a wider pulse with a pulse-width N×Tin. Since the N input pulses of OR gate cannot be overlapping, the buffer delay time τ_d in the delay chain should be longer than pulse-width Tin. This results in limiting the TA speed. In addition, the balanced rise time and fall time of each buffer is necessary in order to maintain the same pulse-width on N inputs of OR gate. The input switches of OR gate determine the number of pulses that goes into the OR gate and thus controls the gain.

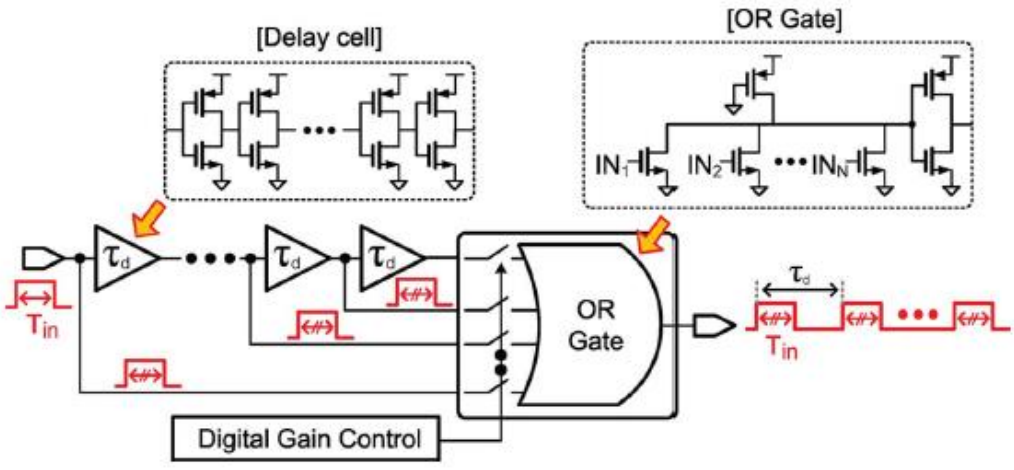

Figure 2-11 Pulse-train based TA [26]

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2.3.4 Closed Loop Controlled Time-Difference Amplifier [27]

In [27], a time difference amplifier whose gain is controlled by a closed loop is proposed. The principle of the proposed TA is illustrated in Fig. 2-12. The delay time of each delay cell is variable and can be changed by a control pin. In Fig. 2-12 (b), the delay time is 4:1 when the control signal is H:L. The connection of two cross-coupled delay chains is shown in Fig. 2-12 (a). Every delay cell output is used to control the delay time in another cross-coupled delay chain. When the rising edge pass through a delay cell, then the output goes high and another cross-coupled cell's delay time will become 4. For example, if the rising edge difference between in1 and in2 is 2 initially, they start to pass through the different delay chain respectively. In1 is from the left side to the right side and in2 is from the right side to the left side. Their rising edges will meet in where the bold arrows point. Then the delay time of all delay cells are frozen. The rising edge of in1 travel 5 delay cells and switch 5 delay cells to "H" in the bottom delay chain. The rising edge of in2 travel 3 delay cells and switch 3 delay cells to "H" in the top delay chain. Eventually, the output rising edge difference between out1 and out2 is 8 which is amplified by 4.

Fig. 2-13 shows a block diagram of the proposed closed loop control TA. A

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delay-locked loop (DLL) is employed to adjust the delay ratio of the variable delay cell with its delay switch of H/L to be 4. When the loop is locked, the delay ratio of the replica delay cell with its delay ratio H/L is adjusted to be 4, and the Vctrl is used to control the main delay cell of the cross-coupled delay chains.

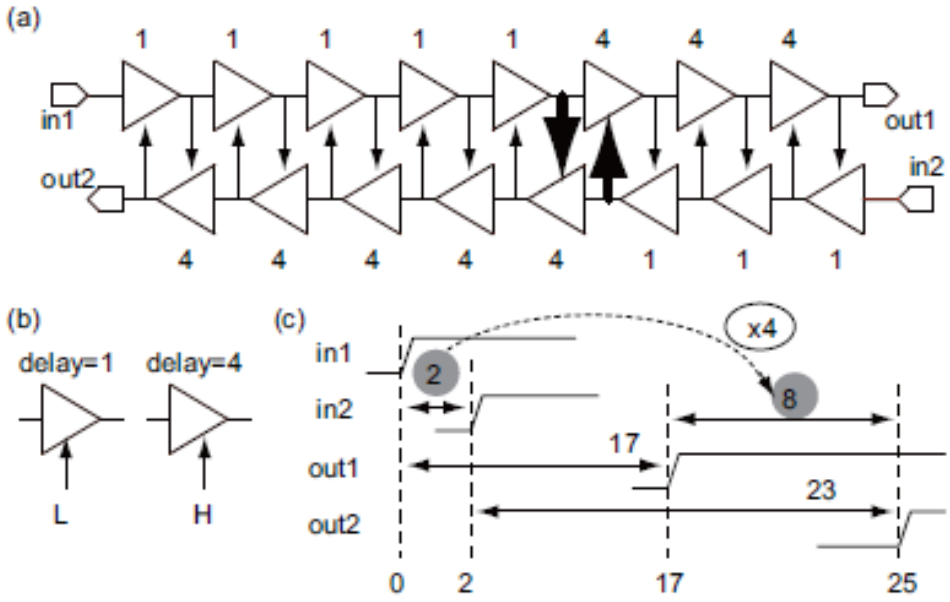

Figure 2-12 Basic idea of the proposed TA in [27]. (a) Cross coupled chains. (b) Variable delay cell (c) Timing diagram.

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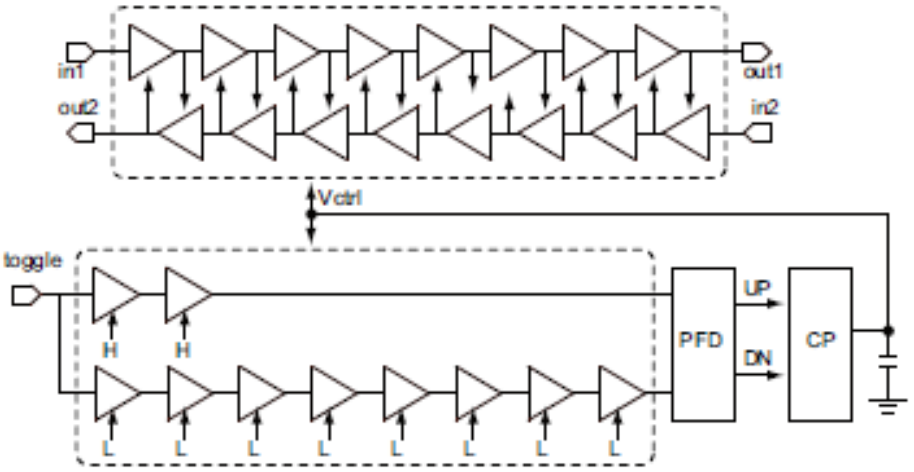

Figure 2-13 TA using DLL-like closed-loop control. [27]

2.4 Summary

Delay-lined-based analog to digital converter is suitable for high speed and low power applications since the time mode circuit can usually be implemented in the digital domain and is of great benefit to the process migration. The most important time mode circuits, VTC and TA are introduced and some state-of-the-art designs are presented as well in this section. VTC is usually used as the first stage of TADC. Its speed and accuracy directly limit the TADC's performance. TA is a time domain amplifier. It is often employed in a high-accuracy TDC for effectively amplifying the time residue. The amplifier gain linearity will affect the overall TDC's resolution.

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Chapter 3

A Time-Based Flash ADC

3.1 Introduction

Recently, picosecond or sub-picosecond resolution time-to-digital converters have been published [28]－[31]. These TDCs were developed using advances in processing technology and downscaling power supply voltages. Time-domain signal processing is becoming increasingly popular in high-speed and moderate-accuracy analog circuits. High-speed and low-supply voltage demanding designs facilitate developing time mode circuit and processing time information.

In this chapter, time-based analog-to-digital converters (TADCs) are introduced. These TADCs have achieved high performance, as reported in [10],[11] and [32],[33] . Among them, [10] and [11] are based on delay lines, whereas [32] and [33] are based on voltage-controlled oscillator. In addition, some voltage-domain ADCs also use auxiliary time-domain signal processing circuits to meet low supply voltage and low power consumption requirements; for example, in [34], Agnes et al. proposed a time-domain

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comparator in a voltage-mode successive approximation register ADC, and in [13], Oh et al. proposed a mixed-mode ADC, in which the first stage was a voltage-type flash ADC. It converted the most significant bits and concurrently transferred the residue signal to the time domain through a three-step integration quantizer. The subsequent stage is a pipelined TDC, used to convert the time-domain residue to the least significant bits (LSBs).

Figure 3-1 depicts a delay-line-based ADC circuit approach. PH1 and PH2 are two out-of-phase clocks. At the sampling phase (PH1), the sample-and-hold circuit samples the voltage-mode signal and all delay cell outputs are reset to 0. At the evaluation phase (PH2), the sampled signal, Vc, is used to tune the delay time of the inverter chain, and a short-duration test pulse is injected into the delay chains and flip-flops simultaneously. The test pulse travels down these inverters during PH2. The sampling flip-flops produce a thermometer code such as “1….1100..0”; the number of ones is the number of inverters that have been visited, and should be proportional to the sampling voltage. The advantage of this structure is that it is simple and easy to implement. However, this ADC structure suffers from a tradeoff between speed and resolution. Higher resolution results in longer latency because of the intrinsic delay of the inverter chains. In addition, the linearity of the inverter chains is a bottleneck in these types of ADCs if no auxiliary

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calibration circuit is included. Based on these considerations, such structure ADC is not suitable for high-speed and moderate-accuracy applications, unless more advanced processes are used. However, low supply voltage used in advanced processes may limit the dynamic range of traditional voltage-control delay cells.

This chapter is organized as follow. The operation principle of the proposed time-domain flash ADC is described in Section II. After that, the VTC implementations and simulation results are shown in Section III. Section IV is the flash TDC implementations. Then, the experimental results and summary are addressed in Section V and VI, respectively.

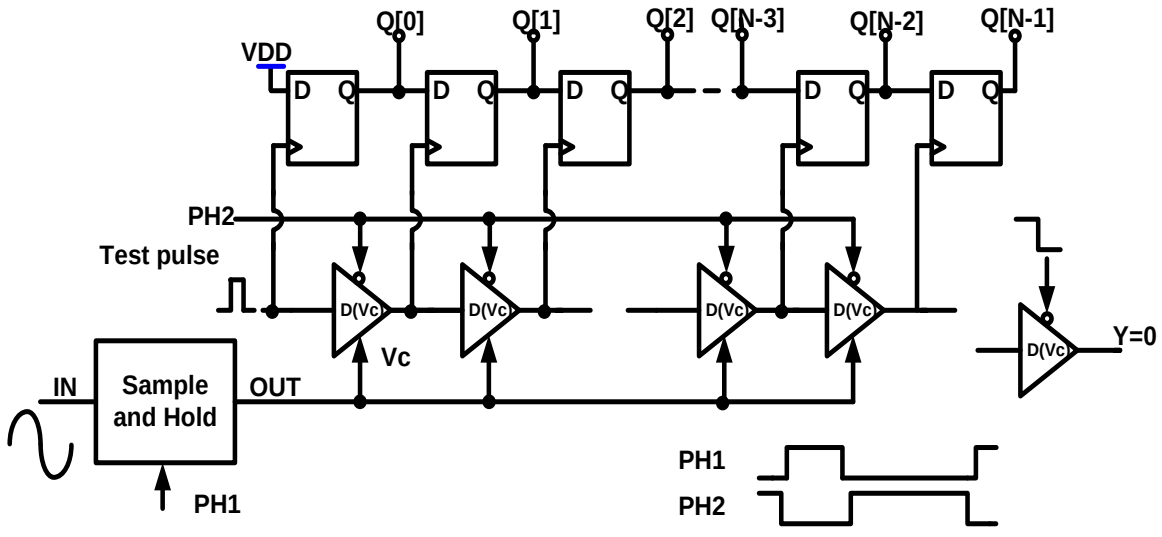

Figure 3-1 Basic structure of a delay-line-based ADC.

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3.2 Proposed Time Domain Flash ADC [37]

In this Section, we will propose a time based ADC design example. The target ADC design is for high-speed (>100MHz), moderate-resolution (4~7 bits) and low power consumption (<10mA) applications. Moving amounts of analog circuits to digital domain is the target of high speed and low power dissipation.

The proposed TADC performs a delay-based signal quantization [10]. That is, the sampling time is independent of input and the delay time is changed according to the analog input. Figure 3-2 shows the block diagram of our proposed TADC. The first stage is a voltage-to-time-difference converter (VTC). The voltage-domain input signal VIN is converted to two clocks Va and Vb outputs that are delayed signals with respect to a reference clock CLK. Their rising edge difference is proportional to VIN. The proposed VTC contains no sample-and-hold circuit because the overall intrinsic delay of the delay chain is much smaller than the sampling time. Therefore, the VIN change is a little bit when clock rising edge travels from the first stage to the last stage of the delay chain. It can be guaranteed by VTC dynamic simulation shown in Fig. 3-15.

The rising edge difference information is then transparent to the subsequent stage, a flash-type TDC. The flash type TDC output is 1-of-n code and can be periodically

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sampled by an n-bits sampler with a constant sample time Ts. The last stage is a code conversion block. The purpose is to transfer 1-of-n code to binary code.

The TADC timing diagram is shown in Figure 3-2. VIN is an analog input. V_a and V_b are defined as VTC clock outputs. The time skew between them is linearly proportional to VIN. The latency of the VTC should be shorter than a clock cycle. In this design, latency is 0.5 to 1 clock cycles. The flash TDC output C is a 32-bit 1-of-n code. Y is a 5-bit binary output that is generated by the code conversion block. The clock signal is also used as a reference clock for VTC delay cell input. The falling edge of the clock is used to capture the flash TDC results simultaneously. Subsequently, the code conversion circuit transfers the 1-of-n code into Gray code synchronized by the clock rising edge. Finally, the Gray code outputs are converted to binary code and synchronized again by the clock rising edge. Thus, the total ADC latency is 3.5 clock cycles.

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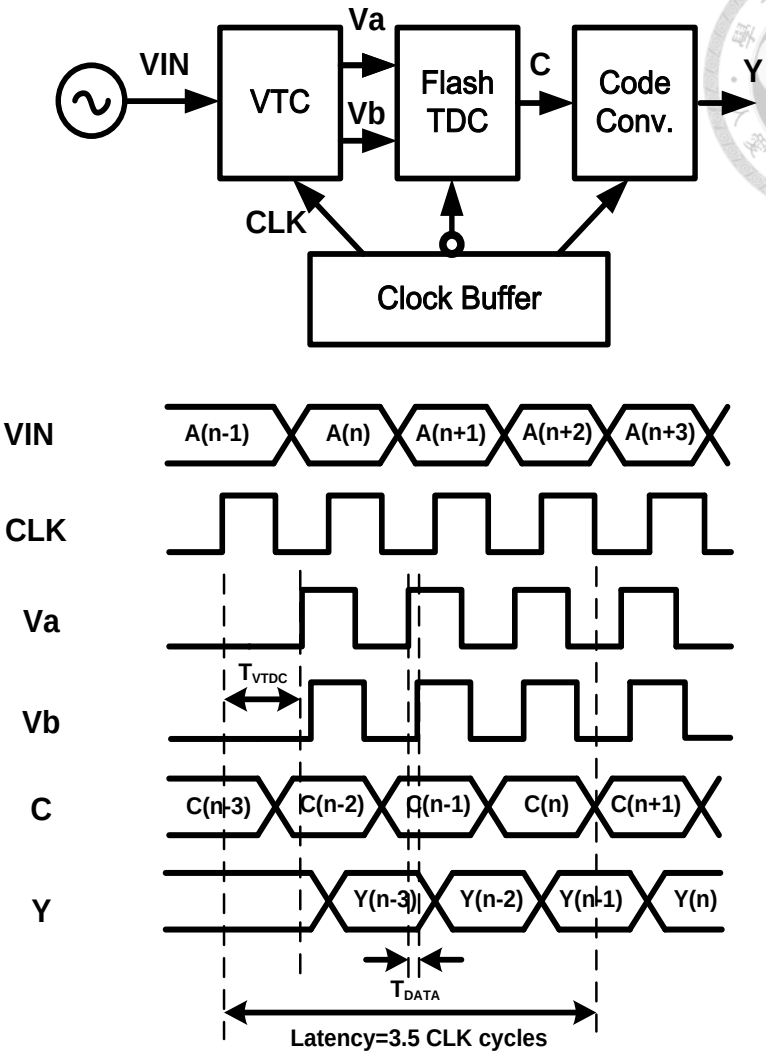

Figure 3-2 Block diagram of the proposed TADC and the relevant timing diagram.

3.3 Implementations of VTC

The principle and prior designs of VTC are also introduced in chapter 2. In this section, a delay-lined based VTC circuit is proposed for voltage-to-time conversion in the first stage of TADC [35][37]. In order to achieve high speed and high accuracy operation, the design and layout of some critical devices should be taken into account

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carefully. In this section, the corresponding design equations and post-layout simulation results are provided to demonstrate its function. Section 3.3.1 addresses the VTC circuit operating principle and design considerations. Some non-ideal effects in an imperfect circuit are also discussed. The simulation results are described in section 3.3.2.

3.3.1 VTC design [35]

The proposed VTC consists of a load control circuit, VREF generator, dual path delay chains and a phase detector. The block diagram was depicted in Figure 3-3 (a).A load control circuit can be divided into a load tuning circuit and two delay replica-biasing circuits. The load tuning circuit converts the input signal VIN to a differential signals Vctrlp and Vctrln are the inputs of two delay replica bias. The delay replica bias circuit will control the output swing of the replica delay cell by a negative feedback and then generate two pairs bias voltages Vcsp(Vcsn) and Vbnp(Vbnn) for the real delay cells (DPx and DNx) biasing. Figure 3-3 (b) shows the corresponding waveforms of VTC.

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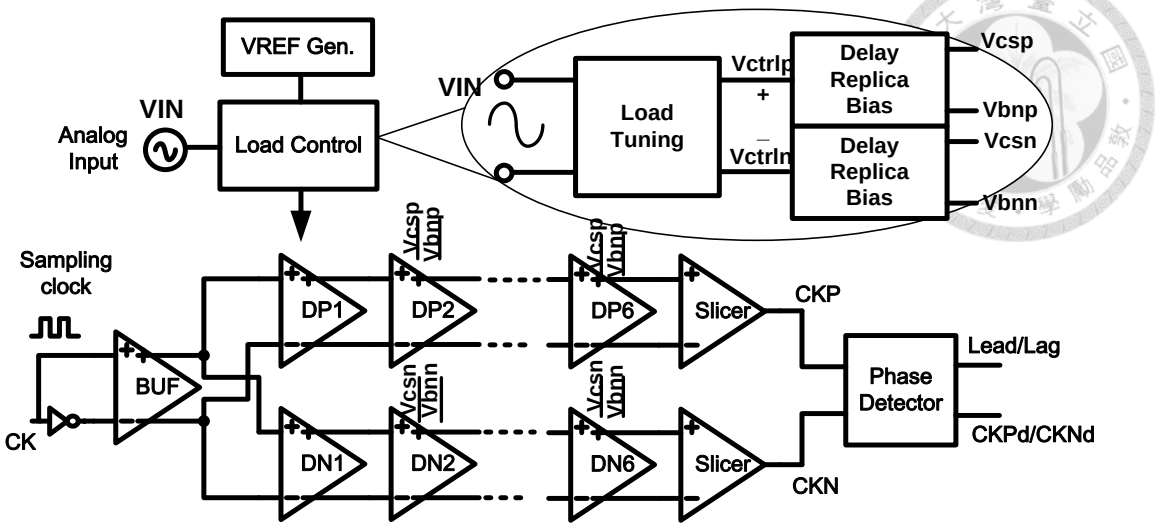
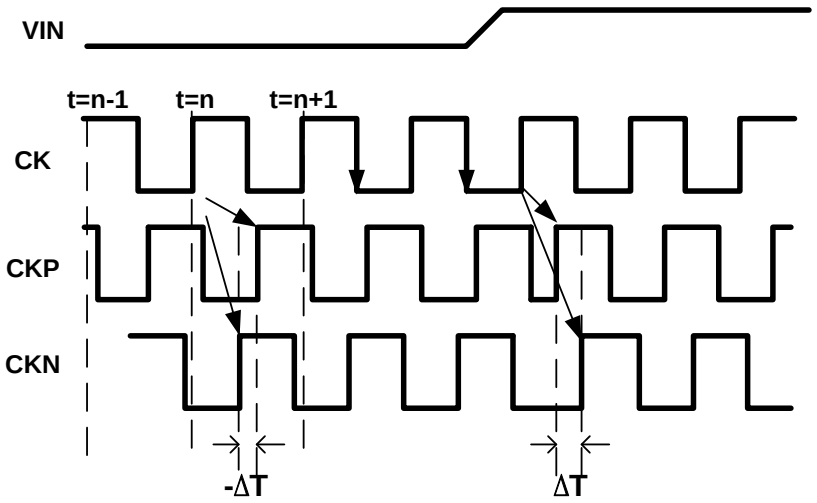


(a)



(b)

Figure 3-3 (a) Proposed VTC block diagram. (b) VTC output waveform.

The operation is described below. If Vctrlp is greater than Vctrln, the clock edge of CKP will lead CKN. In contrast, if Vctrln is greater than Vctrlnp, the result is inversed. Since the transfer curve of the delay time versus the control voltage is nonlinear, a load

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tuning circuit is needed for correcting this non-linearity. The delay replica bias circuit contains a replica of the delay cell, which controls the bias of the delay cell in order to force its output voltage to be clamped between 0 and Vctrlp,n. The dual path delay chain propagates the reference clock CK with a relevant delay time according to the delay control signals Vcsp,Vcsn,Vbnp and Vbnn. The delay chain output signals CKP and CKN have differential time difference properties and the waveforms shown in Figure 3-3 (b).

The purpose of the phase detector is to detect the VTC output signal in advance. The lead (or lag) flag indicates the polarity of analog input. It facilitates preventing the VTC outputs from unnecessarily entering some comparator units of the subsequent flash TDC, thereby markedly reducing power consumption. Only two thirds of the comparator units are toggled during each code conversion. CKPd and CKNd are the delayed signals with respect to CKP and CKN for compensating the latency of the phase detector. The phase detector circuit was implemented using a D-Flip-Flop.

The proposed load tuning circuit is shown in Figure 3-4 (a).The NMOS input degenerated differential pair (MN3 and MN4) with a PMOS diode connected load (MP2~MP5) converts the input differential signals VP and VN into a differential delay control voltages Vctrlp and Vctrln. The PMOS diode connected load is used to match

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the symmetric load of the delay cell in the dual path delay chain.

The delay cell with a symmetric load is proposed in [36]. It has a very broad delay range but the delay time is nonlinear with respect to the control voltage. In fact, the delay changes proportionally to $1/(V_{CTRL}-V_T)$, where V_{CTRL} is control voltage of the symmetric delay cell and V_T is the threshold voltage of the diode connected load (In our design is NMOS MNL1~MNL4 shown in Fig. 3-6 (a).). The transfer curve of delay time versus control voltage, V_{CTRL} is shown in Figure 3-5 (a). Figure 3-5(a) also shows that the characteristic curve will shift due to different process corners. This offset will limit the input dynamic range and overload the following TDCs as well. In order to mitigate this effect, a VREF generator circuit has been added as shown in the Figure 3-4 (b). The purpose is to sense NMOS MN1 and PMOS MP1 threshold voltage and then amplify the summation of their threshold voltage (V_x) by $(1+R_2/R_1)$. V_{REF} serves as the supply voltage of the diode connected load (MP2~MP5) and the output source follower circuit (MP7 and MP8 are input transistors) which is shown in Figure 3-4 (b). At slow P and slow N corners, the PMOS and NMOS will have a higher threshold voltage. This implies that V_X and V_{REF} are also higher and will shift the delay control voltage Vctrlp and Vctrln to a higher level in order to compensate the lower speed of delay cell. Eq. (3.3) is the design equation of VTC transfer gain. This compensation can be

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demonstrated roughly using this equation. Figure 3-5 (a) and (b) show the illustrations of uncompensated and compensated VTC transfer curve. The output time variable is defined as the rising edge difference between the two delay chains output, CKP and CKN, and it can be derived as follows:

$$\because \Delta T_{P,N} \propto \frac{C}{g_{m,delay}} \quad for\ all\ delay\ cells,$$

$$\therefore \Delta T = KN \times (\Delta T_P - \Delta T_N) = K\left(\frac{C/2K_N}{V_{CTRLP} - V_{TNL}} - \frac{C/2K_N}{V_{CTRLN} - V_{TNL}}\right) \quad \text{, and}$$

$$V_{CTRLP} = V_{REF} - 2V_{SGP2,3} + V_{SGP7} = V_{REF} - 2\left(\left|V_{T2,3}\right| + \sqrt{(I + \Delta I)/K_P}\right) + |V_{T7}|\,,$$

$$V_{CTRLN} = V_{REF} - 2V_{SGP4,5} + V_{SGP8} = V_{REF} - 2\left(\left|V_{T4,5}\right| + \sqrt{(I - \Delta I)/K_P}\right) + |V_{T8}|\,,$$

$$V_{REF} = \left(1 + \frac{R2}{R1}\right)(V_{SGP1} + V_{GSN1}) = \left(1 + \frac{R2}{R1}\right)\left(|V_{TP1}| + V_{TN1} + \sqrt{I_B/K_{P1}} + \sqrt{I_B/K_{N1}}\right), \tag{3.1}$$

$$\Delta \mathrm{T} = \frac{\mathrm{KN}(C/2K_N)}{(V_{REF} - |V_T| - V_{TNL}) - \sqrt{(I + \Delta I)/K_P}} - \frac{\mathrm{KN}(C/2K_N)}{(V_{REF} - |V_T| - V_{TNL}) - \sqrt{(I - \Delta I)/K_P}}$$

$$= \frac{\mathrm{KN}(C/2K_N)\left(\sqrt{(I + \Delta I)/K_P} - \sqrt{(I - \Delta I)/K_P}\right)}{\left[\left((V_{REF} - |V_T| - V_{TNL}) - \sqrt{(I + \Delta I)/K_P}\right)\left((V_{REF} - |V_T| - V_{TNL}) - \sqrt{(I - \Delta I)/K_P}\right)\right]}$$

$$\approx \sqrt{\frac{I}{K_P}} \times \frac{\left(\frac{\mathrm{KNC}}{2K_N}\right)\left[\left(1 + \frac{1}{2}\left(\frac{\Delta \mathrm{I}}{\mathrm{I}}\right) - \frac{1}{4}\left(\frac{\Delta \mathrm{I}}{\mathrm{I}}\right)^2 \pm \cdots\right) - \left(1 - \frac{1}{2}\left(\frac{\Delta \mathrm{I}}{\mathrm{I}}\right) - \frac{1}{4}\left(\frac{\Delta \mathrm{I}}{\mathrm{I}}\right)^2 \pm \cdots\right)\right]}{\left[(V_{REF} - |V_T| - V_{TNL}) - \sqrt{I/K_P}\right]^2}$$

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$$\approx \sqrt{\frac{1}{K_P I}} \times \frac{\left(\frac{\mathrm{KNC}}{2K_N}\right)\Delta I}{\left[(V_{REF} - |V_T| - V_{TNL}) - \sqrt{I/K_P}\right]^2}$$

$$\approx \sqrt{\frac{1}{K_P I}} \times \frac{\left(\frac{\mathrm{KNC}}{2K_N}\right)\left(\frac{\Delta V_{IN}}{\mathrm{R}}\right)}{\left[(V_{REF} - |V_T| - V_{TNL}) - \sqrt{I/K_P}\right]^2} \quad (3.2)$$

Where ΔT_P and ΔT_N are absolute delays of the two delay cells DPx and DNx, respectively. V_{CTRLP} and V_{CTRLN} are the control voltage of P-side and N-side delay cells, N is the total number of delay cells in one delay chain, K_P and K_N are the current gain of PMOS diode connected load (MP2~MP5) in Figure 3-4 (b) and NMOS symmetrical load of delay cell (MNL1~MNL4) in Figure 3-6 (a). C is the output capacitance of all delay cells and K is a constant. V_{TNL} is the threshold voltage of the NMOS symmetric load. $|V_{TP1}|$ and V_{TN1} are the threshold voltage of MP1 and MN1 in VREF generator circuit in Figure 3-4 (a) and I_B is their bias current. $|V_{T2,3}|, |V_{T4,5}|, |V_{T7}|$and $|V_{T8}|$ are the threshold voltage of PMOS devices MP2,MP3,MP4,MP5,MP7 and MP8 in load tuning circuit. To simplify this derivation, assume they are identical, and the threshold voltage is defined as$|V_T|$. By Eq. (3.1) and (3.2), the overall gain of VTC can be expressed as G, and

$$\mathrm{G} = \left(\frac{\Delta \mathrm{T}}{\Delta V_{IN}}\right)$$

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$$= \frac{\left(\sqrt{\frac{1}{K_P I}}\right)\left(\frac{\mathrm{KC}}{2K_N}\right)\left(\frac{\mathrm{N}}{\mathrm{R}}\right)}{\left[\underline{\underline{\left(\left(1+\frac{R2}{R1}\right)(|V_{TP1}|+V_{TN1})-|V_T|-V_{TNL}\right)}}+\left(\left(1+\frac{R2}{R1}\right)\left(\sqrt{\frac{I_B}{K_{P1}}}+\sqrt{\frac{I_B}{K_{N1}}}\right)-\sqrt{\frac{I}{K_P}}\right)\right]^2} \quad (3.3)$$

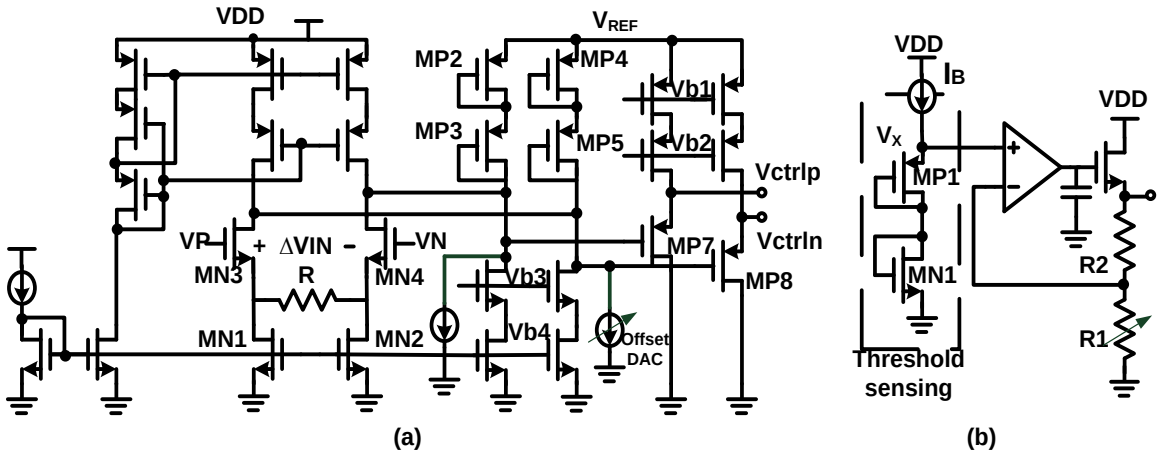

Figure 3-4 (a) Load tuning circuit. (b) VREF generator.

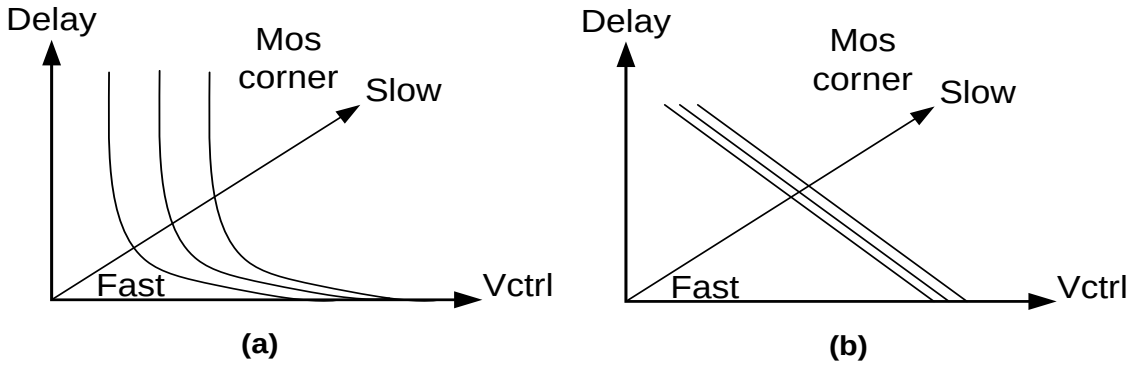

Figure 3-5 Illustrations of the (a) uncompensated process VTC and (b) compensated process VTC.

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The load tuning circuit is designed to provide a control voltage V_{CTRLP} and V_{CTRLN} expressed as Eq.(3.1). From Eq. (3.2), the output time variable, ΔT is linearly proportional to the analog input voltage ΔV_{IN} and the transfer gain *G* also derived in Eq. (3.3). Moreover, a proposed VREF generator circuit for compensating the threshold voltage variation at different MOS corner and the result is marked with double horizontal lines in Eq. (3.3). The delay chain circuit is used to process the sampling clock CK and generate time difference signals that are to be measured and quantized by the following TDCs. The overall delay time *Td* at the *kth* sample can be represented as Eq. (3.4)

$$Td(k) = N \times (Tint + Vin(k) \times G), \mathrm{Td} < \mathrm{Ts\ at\ any\ sample\ k} \qquad (3.4)$$

$$\mathrm{Fs} = 1/\mathrm{T_s} < 1/\big(\mathrm{N} \times (Tint + Vin,max \times G)\big) \quad , \qquad (3.5)$$

$$G < (\mathrm{T_s} - \mathrm{N} \times Tint)/(\mathrm{N} \times Vin,max) \quad , \qquad (3.6)$$

$$\mathrm{T_{res}} = \frac{Td,max}{2^{\mathrm{n}}} = \frac{Vin,max \times G}{2^{\mathrm{n}}} < \frac{\mathrm{T_s} - \mathrm{N} \times Tint}{\mathrm{N} \times 2^{\mathrm{n}}} \quad , \qquad (3.7)$$

Where Tint is the intrinsic delay of the symmetric delay cell, *G* is the VTC transfer gain, Tres is the time resolution of the time delay *Td,max* which is quantized into n bits, and N is the total delay cell number in the delay chain. In fact, *Td* should be less than a

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TDC sample time *Ts*, implying the maximum allowed transfer gain and time resolution in following n-bit TDC will be as given in Eq. (3.6) and Eq. (3.7). For example, if the TDC sampling frequency is 500 MHz, the intrinsic delay time of a delay cell is 200 picoseconds, delay chain number is 4, and input is quantized into 6 bits, then the maximum allowed time resolution of the following TDC is 4.7 picoseconds. Eq. (3.5) also gives the maximum allowed sampling frequency of the following TDC if VTC gain, intrinsic delay and input range are known.

The delay chain circuit consists of a clock buffer, a number of delay cells, and a voltage slicer circuit. A source coupled pair with a symmetric load delay cell is adopted, as shown in Figure 3-6 (a). The left side of Figure 3-6 (b) is a closed loop delay replica biasing circuit. The negative feedback mechanism forces Vb to be approximately equal to Vctrl. Since the bias circuit is a half replica of the delay cell, the mechanism also forces the output voltage of the delay cell to be clamped to Vctrl. In order to operate at high speed, a modified open loop replica bias circuit is used to force Vb close to Vctrl, as shown in the right side of Figure 3-6 (c). Substituting the NMOS transistor MNB1 for the PMOS transistor MPS1 in the Figure 3-6 (b) and the gate voltage of MN1 is equal to Vctrl plus a NMOS threshold voltage.

The purpose of the voltage slicer circuit is to amplify the delay cell output to the

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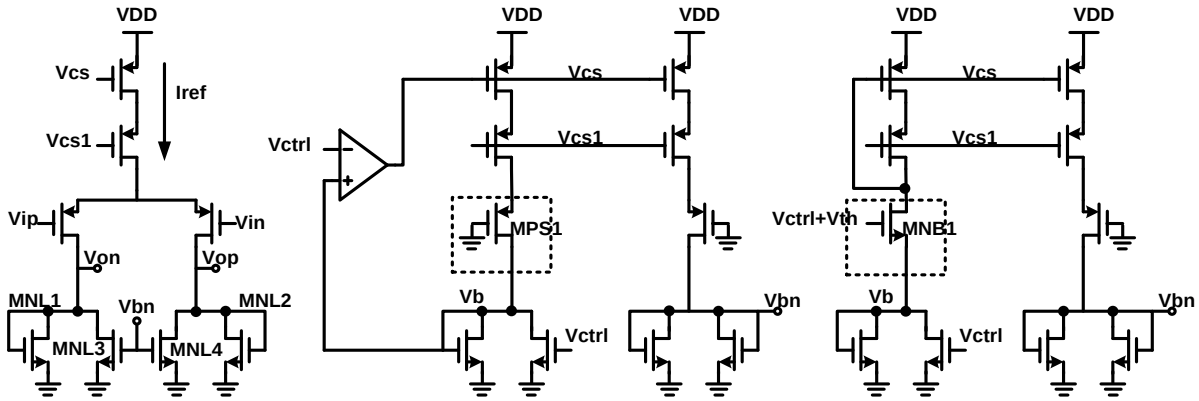
supply rail. It also contributes some nonlinearity in the VTC since the response time is not identical when a small or large swing input occurs at the slicer circuit. Fortunately, the delay chain with a large-scale output swing has a smaller delay time, which alleviates the design effort of the slicer since one can use a general amplifier circuit. The delay time of the slicer is also proportional to the delay time of the delay chain. Figure 3-7 shows the proposed slicer circuit. An operational transconductance amplifier with a dynamic tail current that is inversely proportional to Vctrl is used to further improve the linearity and power efficiency. The layout of the VTC circuit is completed using a 0.18μm CMOS process as shown in Figure 3-8.



(a) **(b)** **(c)**

Figure 3-6 (a) Symmetric delay cell circuit (b) Replica biasing circuit of the delay cell. (c) A modified replica biasing circuit of the delay cell.

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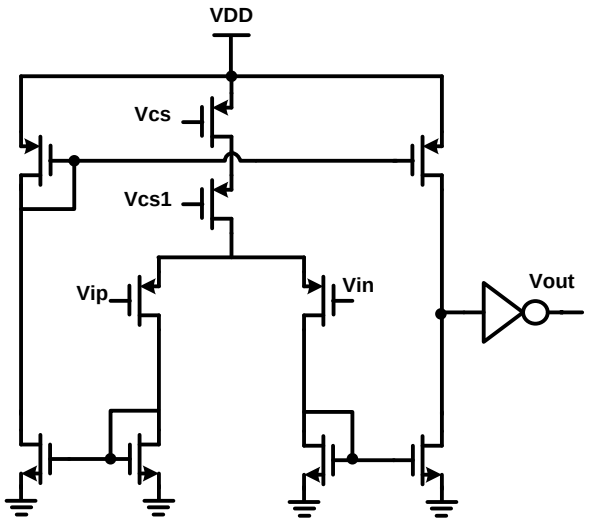

Figure 3-7 A voltage slicer circuit.

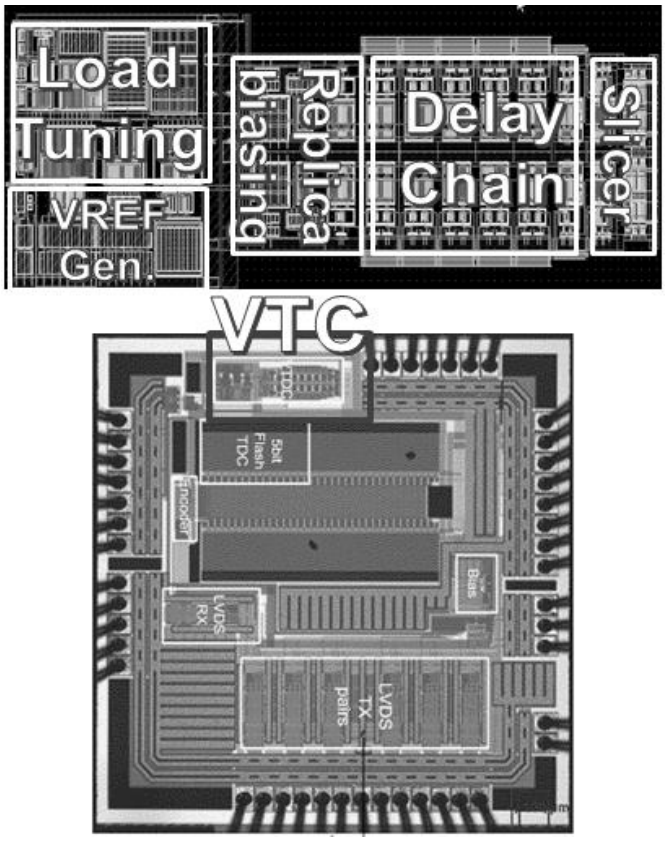

Figure 3-8 VTC layout in whole chip. (Area is 400μm by 100μm).

The delay time mismatch in a dual-delay-line structure is more severe than that in a

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single delay line. This mismatch further impairs the linearity of the VTC transfer gain. Equations (3.3), (3.8) and (3.9) provide calculations for the VTC influenced by imperfect device matching.

$$\mathrm{T_{LSB}} = G \times \mathrm{V_{LSB}} = \frac{\left(\sqrt{\frac{1}{K_P I}}\right)\left(\frac{\mathrm{KC}}{2K_N}\right)\left(\frac{\mathrm{N}}{\mathrm{R}}\right) \times \mathrm{V_{LSB}}}{\left[(V_{REF} - |V_T| - V_{TNL}) - \sqrt{I/K_P}\right]^2}$$

$$= f(N\ ,K_P\ ,|V_T|\ ,K_N\ ,V_{TNL}) \tag{3.8}$$

$$T_{LSB} = \left(\frac{\Delta|V_T| + \Delta V_{TNL}}{\left[(V_{REF} - |V_T| - V_{TNL}) - \sqrt{I/K_P}\right]^2} + \frac{\frac{1}{2}(-VREF + \Delta|V_T| + \Delta V_{TNL})\Delta K_P}{\left[(V_{REF} - |V_T| - V_{TNL}) - \sqrt{I/K_P}\right]^2 K_P} + \frac{\Delta N}{N} + \frac{-\Delta K_N}{K_N}\right) \times T_{LSB} \tag{3.9}$$

In Eq. (3.9), the first two terms error are the threshold and current gain mismatch of PMOS MP2~MP5 in the load tuning circuit. The last two terms error are from the delay cells mismatch. Figure 3-9 shows a Monte-Carlo simulation result at zero analog input of VTC. There are a total of 300 runs. The simulation result shows that the peak-to-peak delay variation is less than 25 picosecond. This is the minimum distinguishable resolution without calibration.

This variation of output time variable of VTC can be calibrated to further improve its resolution if necessary. For instance, the bias voltage of the delay cells can be fine-

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tune by using a replica delay cell while the delay time is locked by a delay-locked loop to reduce the mismatch effect. A cyclic delay structure can also reduce the number of delay element to just one, but a cyclic delay structure is difficult to operate at high speed.

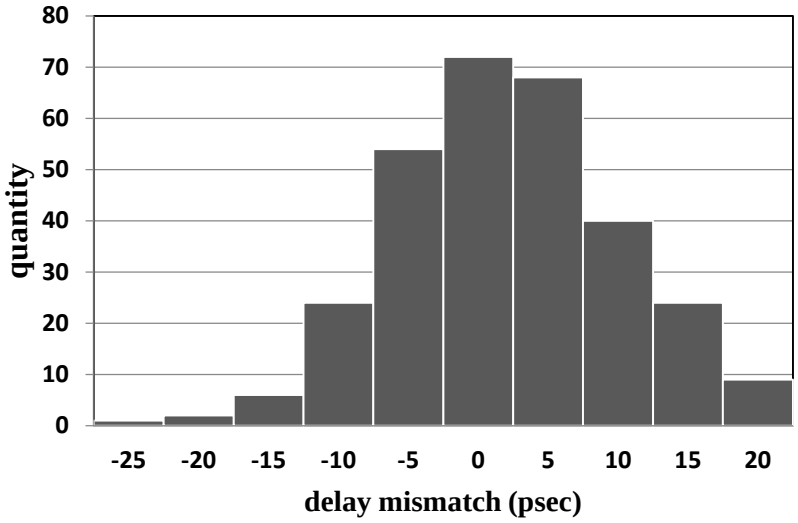

Figure 3-9 Monte-Carlo simulation results of VTC at zero analog input.

3.3.2 VTC Simulation Results

VTC is a critical building block in TADC. However, the change of VTC output time variable is very small and difficult to be distinguished at an off-chip noisy environment. Due to this, we will do more simulation to check its function and performance. In this section, the linearity of transfer characteristic, operating speed and signal bandwidth are simulated. According to these simulation results, ensured that the

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proposed VTC is suitable to be used in time-based ADCs.

First, the VTC transfer characteristic is checked to ensure the input range and linearity. The compensated and uncompensated VTC voltage versus delay time difference transfer curves are simulated by sweeping the DC input of the VTC and measuring the time difference between the output clocks, CKP and CKN. The compensated and uncompensated VTC transfer curves are shown in Figure 3-10. Figure 3-11 shows the calculated INL and DNL when the input is quantized into 6 bits. The DNL of the compensated and uncompensated VTC are -0.05~+0.12 LSB and -0.07~+0.14 LSB, respectively. The INL of the compensated and uncompensated VTC are -0.5~+0.6 LSB and -0.7~+0.9 LSB, respectively. Table 3.1 lists the calculated DNL and INL results of the compensated VTC if the DC inputs are quantized into 6, 7, and 8 bits, respectively. Fig. 3-12 also shows the VTC transfer characteristic over the process and temperature variation and compares the results with and without VREF generator. According to the simulation result, the VREF generator improves the transfer curve variation of VTC due to MOS threshold voltage variation at different corner (TT,SS and FF corner). However, by observing Eq. (3.3), MOS current gain drift of MP1 and MN1 in VREF generator and output capacitance change of delay cells because of temperature variations affect the transfer gain as well. An I_B offset current is provided in the VREF

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generator in order to compensate the temperature variations. Fig. 3-13 (a) and (b) shows the I_B current and maximum delay difference versus temperature variations with and without I_B offset current simulation results.

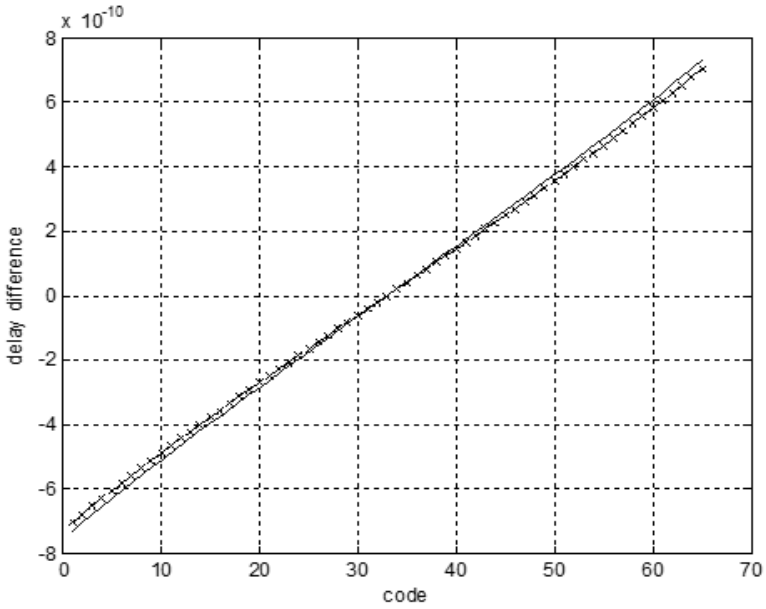

Figure 3-10 The delay transfer characteristic of compensated denoted by "−" and uncompensated VTC denoted by "x".

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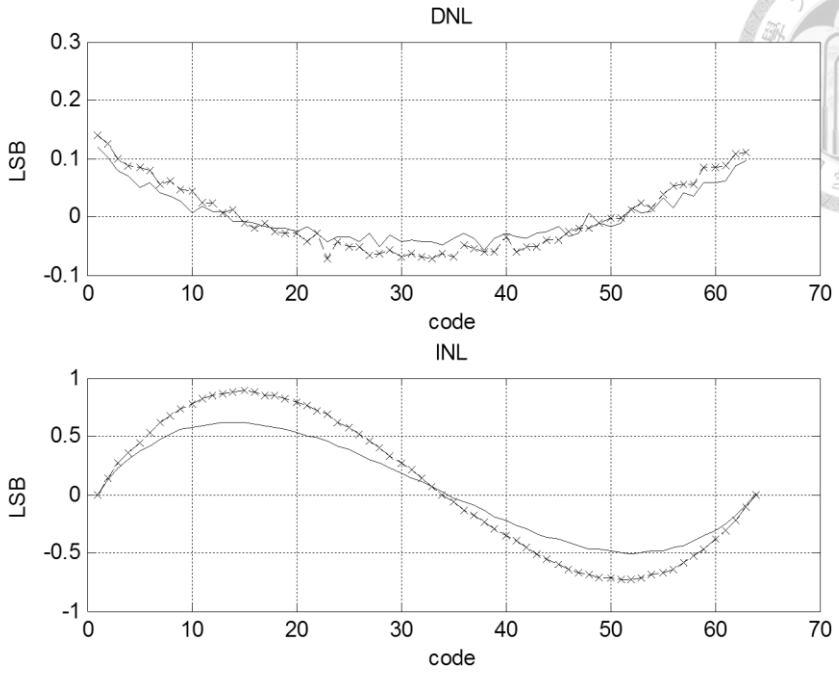

Figure 3-11 The simulated DNL and INL of compensated denoted by "−" and uncompensated VTC denoted by "x".

Table 3-1 The DNL and INL of compensated VTC while DC inputs are quantized into 6,7 and 8 bits.

Level	LSB(psec)	DNL(LSB)	INL(LSB)
64	22.8	-0.06~+0.12	-0.5~+0.6
128	11.4	-0.07~+0.12	-1.1~+1.2
256	5.7	-0.11~+0.16	-2.3~+2.4

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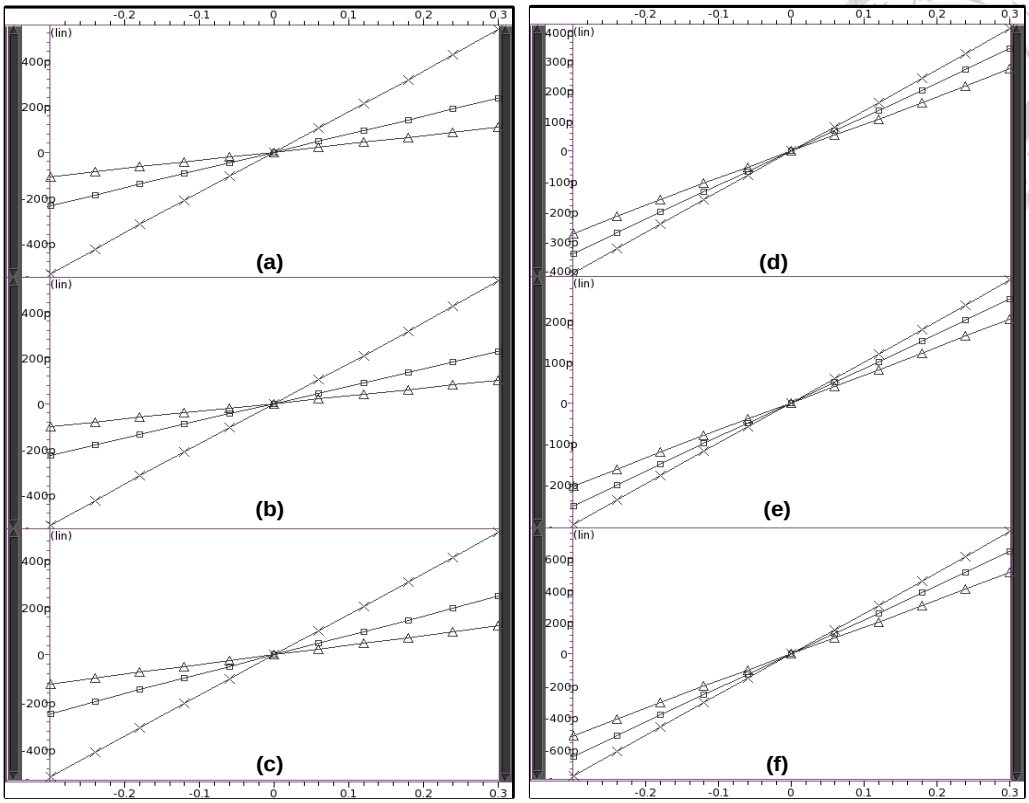

Figure 3-12 Simulated VTC transfer characteristic at different MOS corners and temperature. (“□” : TT corner, “Δ” :FF corner, “X”: SS corner), ((a)(d):temp=-10℃, (b)(e): temp=25℃, (c)(f):temp=120℃) (a)(b)(c) without VREF Gen. and (d)(e)(f) with VREF Gen.

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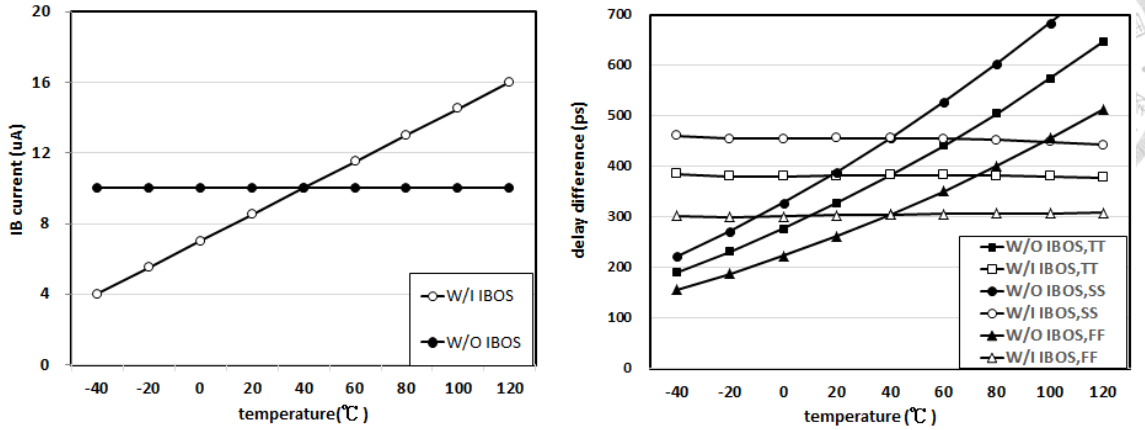

Figure 3-13 Simulated VTC output time difference variations versus temperature variation at different MOS corners with and without I_B offset current compensation. (a) I_B current with and without offset. (b) The maximum delay difference. @ TT,SS,FF corner.

Second, the operating speed of VTC will be examined. From Equation (3.5), the maximum allowed sampling frequency of the TDC stage is inversely proportional to the input signal amplitude. According to the simulation results shown in Figure 3-14, the maximum allowed sampling frequency is limited by the intrinsic delay of the delay chains, analog input swing and VTC transfer gain. The simulated output spectrum is shown in Fig 3-15. It addresses the dynamic performance of VTC. In this simulation, analog differential input swing is 0.8Vpp and its frequency is 124MHz, and sampling frequency is 500MHz. The reports SNDR and ENOB are 47.7dB and 7.6-bit,

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respectively.

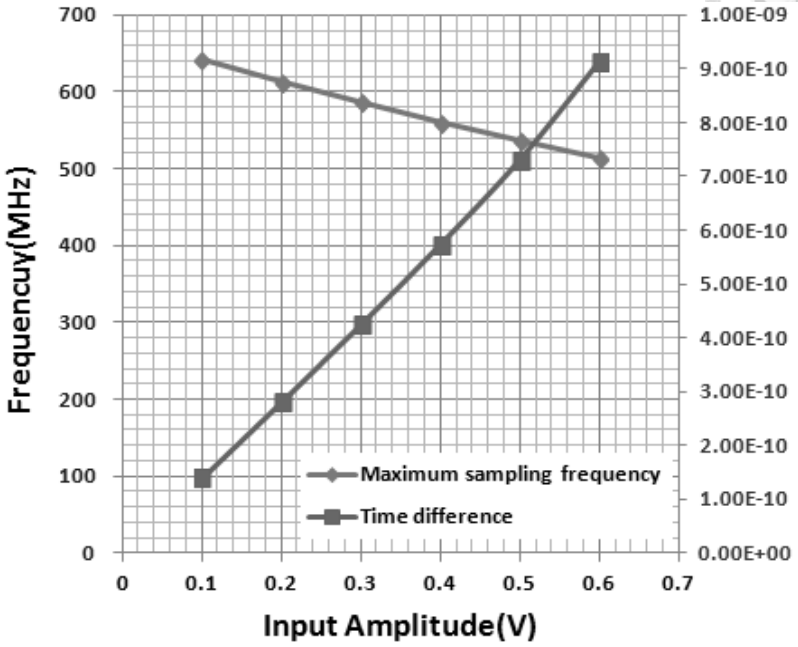

Figure 3-14 Simulated maximum allowed sampling frequency and output time difference versus input signal amplitude.

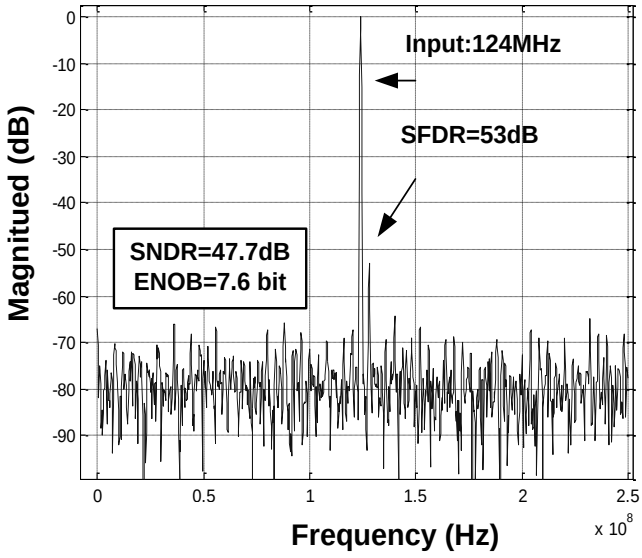

Figure 3-15 Simulated VTC output spectrum. (@$V_{in,diff}$=0.8Vpp, F_{in}=124MHz, F_s=500MHz)

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Third, the VTC bandwidth is addressed through the VTC transient simulations. For a given frequency reference clock CK (e.g., 500 MHz), the input sinusoidal signal frequency is swept and the output time difference is measured. Since the conversion of VTC is linear, the time difference values should also constitute a sinusoidal signal and their amplitude can be measured to find the bandwidth of the VTC. The frequency response of the VTC is shown in Figure 3-15. The VTC bandwidth is around 250 MHz, which implies the maximum bandwidth of whole ADC is 250MHz.

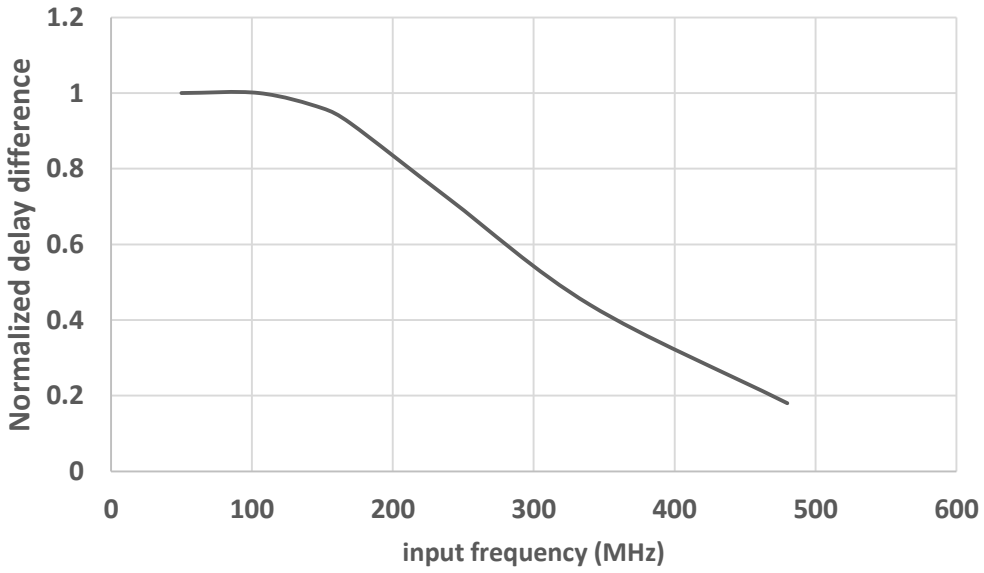

Figure 3-15 Frequency response of VTC

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3.4 Implementations of Flash TDC [37]

The input voltage-mode signal is converted into a relative time-difference signal by the VTC in sequence. The next stage, a flash TDC, then quantizes the time-difference signal to the relevant digital code. Figure 3-16 shows the proposed flash TDC architecture. It is composed of several time comparing units (including delay cells and a D-flip-flop), a digital error-recovery circuit (for bubble error elimination), and code converters (1-of-n code to Gray code, Gray code to binary code).

Analogous to a conventional voltage-type flash ADC, the flash TDC contains numerous comparator units composed of delay cells and D-flip-flops. They are used to replace the reference voltage and comparators in the voltage mode flash ADC. In a conventional voltage mode flash ADC design, the compared voltage is typically generated from a resistor string. The static current consumption in the resistor string is usually substantial because of the need for high speed, accurate settling and high noise immunity. Moreover, the comparator circuit often requires a high speed and high gain preamplifier circuit at its front end for amplifying the noise level voltage difference before slicing it at the logic level. For high-speed operation, significant current consumption in the pre-amplifier circuit is inevitable.

However, in the present work, D-flip-flops are adopted to compare the time

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difference in the flash TDC circuit. It is naturally digital and more robust than a conventional design in low-power-supply-voltage and noisy environment. Figure 3-17 (a) and (b) (c) contrast the comparator units of a flash ADC and a flash TDC.

Because the time resolution of the TDC is limited by the VTC intrinsic delay and the ADC sampling rate, one LSB delay in our design is roughly 25 picosecond in order to minimize the latency of VTC. The delay time is shorter than a gate delay in the 0.18-μm process. Structure in Fig. 3-17 (b) is not suitable for this design. Inverter pairs with distinct *RC* delay elements are used to implement the delay differences Td1 and Td1+ΔT shown in Fig. 3-17 (c). Given the superior matching properties of passive RC elements, the required accuracy is not difficult to achieve. In our design, capacitances are fixed and resistances are variable. The total resistance value of two paths is constant in all comparison units, as shown in Figure 3-18.

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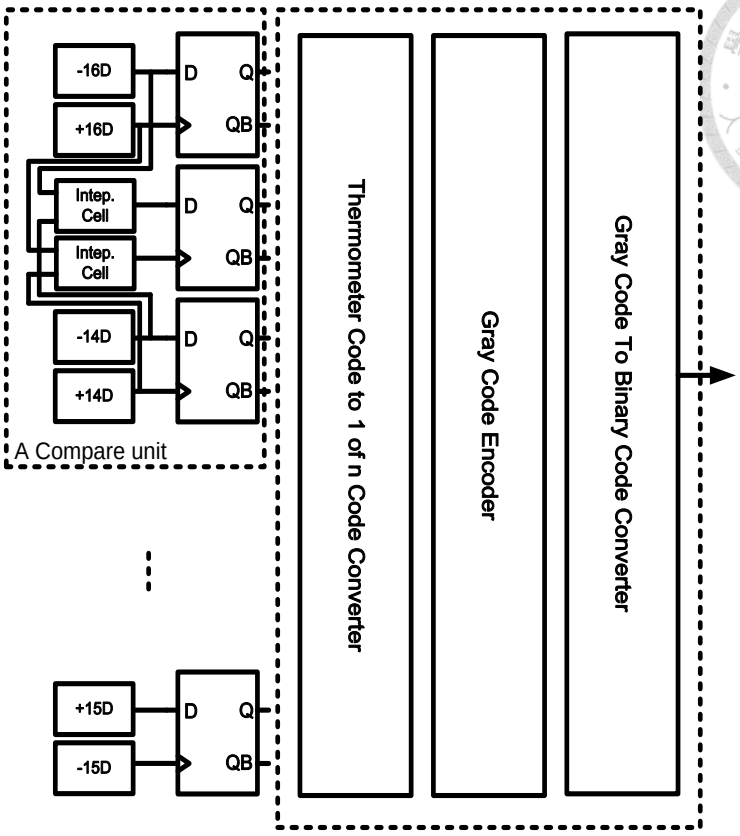

Figure 3-16 Proposed Flash TDC architecture.

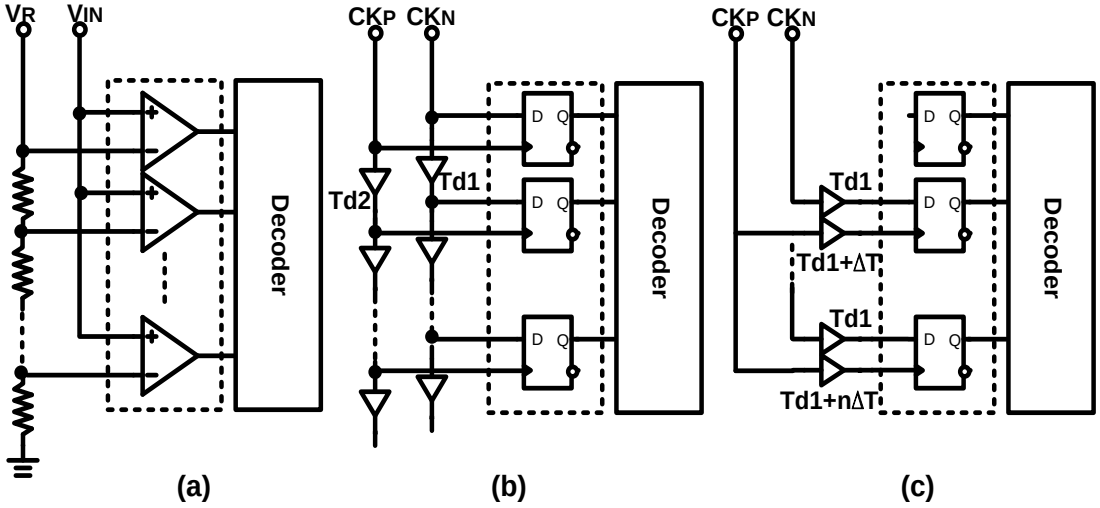

Figure 3-17 (a) Voltage domain flash ADC. (b)(c) Time domain flash TDC.

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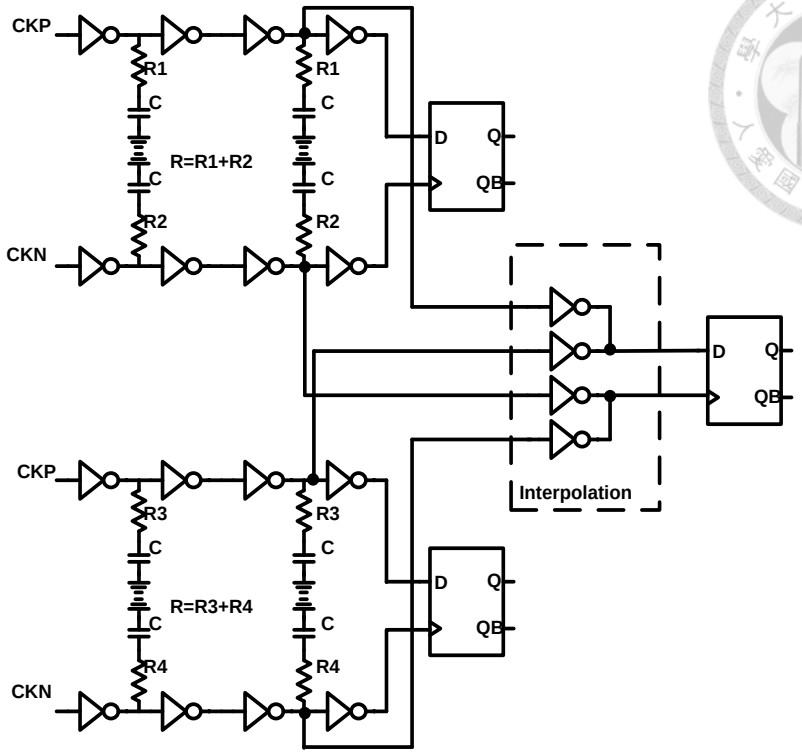

Figure 3-18 A complete time comparator units. It is composed of RC delay-lines, D-flip-flops and active interpolation inverters.

In Figure 3-18, the polysilicon resistors R_i and R_{i+1} have almost same layout area but different contact positions for varying their resistor values. The unit cell layout of resistors is to mitigate process variations. The design equation is given in Eq. (3.10).

$$R_i = R + i \times \Delta R, R_{i+1} = R - i \times \Delta R, \quad i = 1 \ldots 2n \text{ (if n bits ADC)} \qquad (3.10)$$

Figure 3-19 shows simulation results of the delay difference property of an

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inverter with an *RC* delay in TT, SS, and FF corner cases. Due to saving more power of time comparators, the interpolation structure is adopted. The time resolution of comparator unit is 50 picosecond ($\pm$25picosecond).The delay range is 400 picosecond. (=16×25 picosecond) . The simulations show that the range of ΔR is roughly equal to the resistor R value. The horizontal axis is the resistance value and the vertical axis is the delay difference between two delay lines. The simulation includes ±30% *RC* variation. Although such variation will result in ADC gain error and limit the ADC's input dynamic range, this is not a very critical issue for ADC performance because it can be easy to calibrate [37].

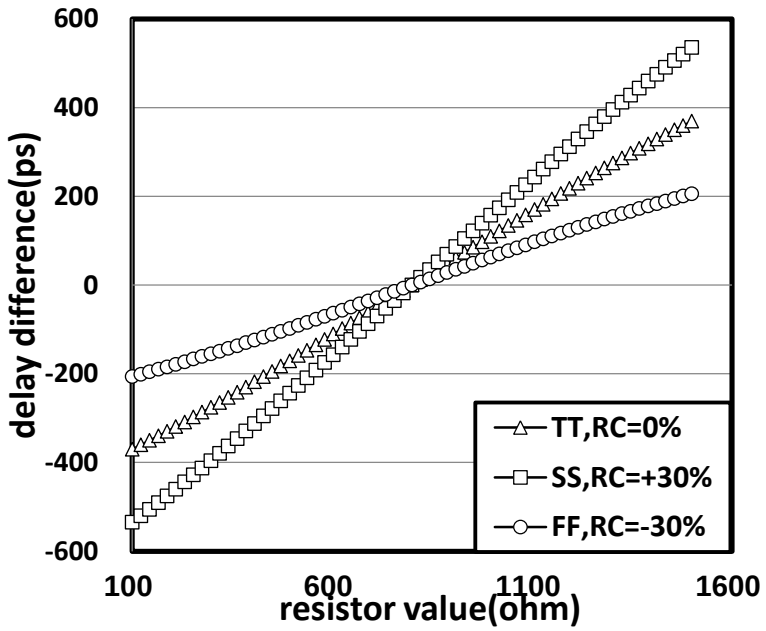

Figure 3-19 The simulated delay difference characteristics of RC inverter delay-lines.

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For the flip-flop design, high-speed true single-phase clock (TSPC) D-flip-flops are adopted. In order to reduce the power consumption and chip area aggressively, an interpolation scheme in conventional flash ADC is also used. Half of the *RC* delay elements that could be eliminated. Figure 3-17 depicts a complete comparator unit with active interpolation inverters.

The gain error and offset of the VTC transfer characteristics will limit the whole ADC dynamic range notwithstanding any compensation circuit inside the VTC. Extending the TDC input range is necessary to cover the PVT variation. In our design, two dummy comparator units are placed at the top and bottom of flash TDC. In addition, the bubble error in voltage-type flash ADC still occurs in the flash TDC if the layout of clock trace is not well matched. Comparing output of adjacent comparator unit results solves the bubble error problem. Furthermore, we convert the 1-of-n code to Gray code first. This facilitates reducing code transition errors resulting from the partial sampling effect of different D-flip flop due to their mismatch. The Gray code encoder is implemented using a ROM-based design.

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3.5 Experimental Results

The 5-bit TADC prototype was fabricated in a 0.18-μm CMOS process. Figure 3-20 shows a photograph of the chip. The active area is 0.37 mm^2 (including the VTC, TDC, and code converter).

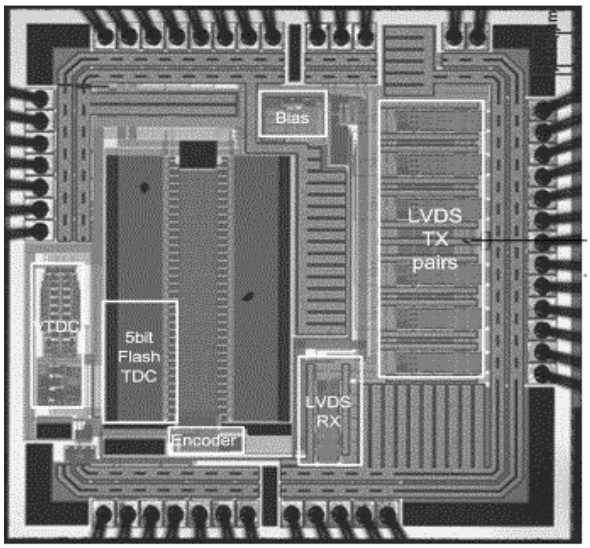

Figure 3-20 Test Chip Die Photograph.

Figure 3-21 shows the chip test plan for the proposed ADC; some interface circuits are included on this chip. These include low-voltage differential signaling (LVDS) TX pairs for high-speed digital output signal integrity, LVDS RX for high-speed ADC clock input-signal integrity, and some bias circuits for LVDS TX/RX. The input analog signal

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source is an RF signal generator. The clock source is a pulse pattern generator. Here, we implemented four copies of 5-bit flash TDCs for testing; these TADCs can be reconfigured as a 6-bit TADC with twice the data throughput rate in the future. In this prototype, however,only a 5-bit TADC is demonstrated.

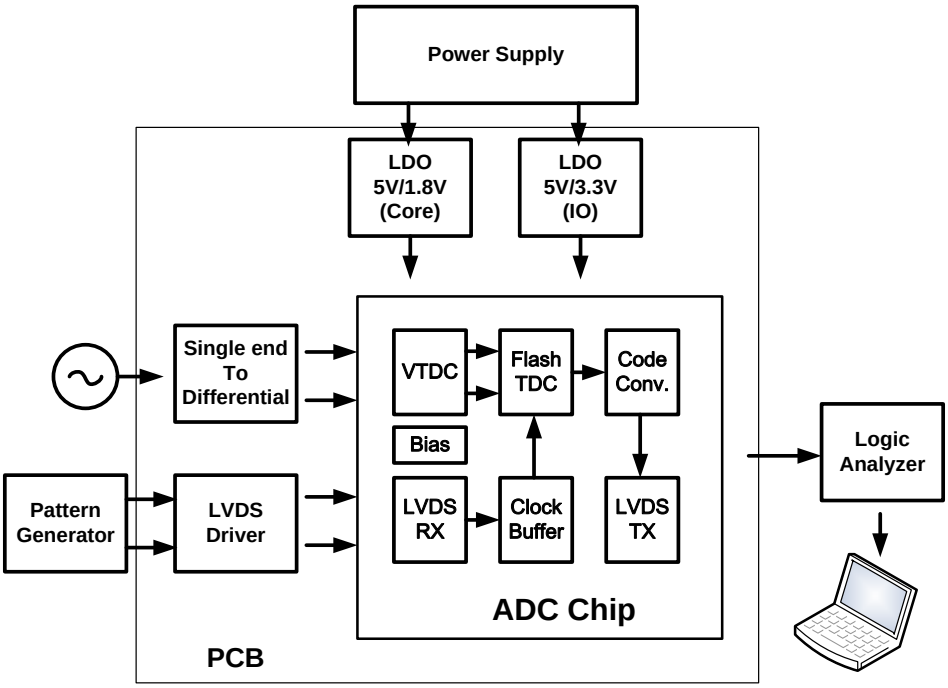

Figure 3-21 ADC chip test plan.

Figure 3-22 (a) and (b) shows the differential nonlinearity (DNL) and integral nonlinearity (INL) results obtained using the sine-wave code density test method at 400 MS/s with an input frequency of 1 MHz. The peak DNL and INL are 1 and 1.7 LSB,

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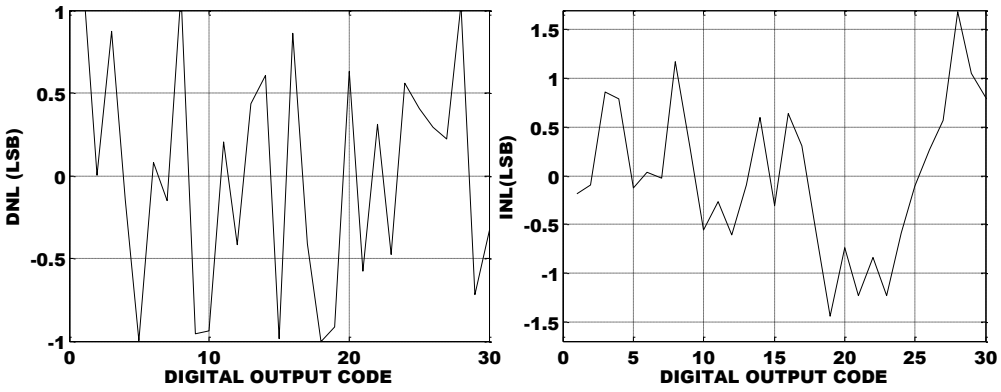
respectively. Figure 3-23 shows the measured spectrum at a 400-MHz sampling rate with an input at one fourth of the sampling rate; the SFDR and SNDR are 30.7 dB and 25.2 dB, respectively. The dynamic performance levels with respect to the input frequencies are shown in Figures 3-24 (a) and (b).



(a) (b)

Figure 3-22 Measured (a) DNL and (b) INL results at fs=400 MHz, fin=1 MHz .

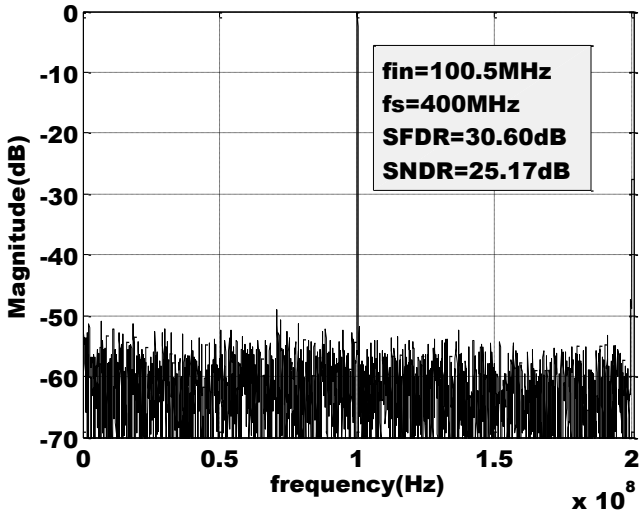


Figure 3-23 The measured output spectrum at fs=400 MHz, fin=100 MHz .

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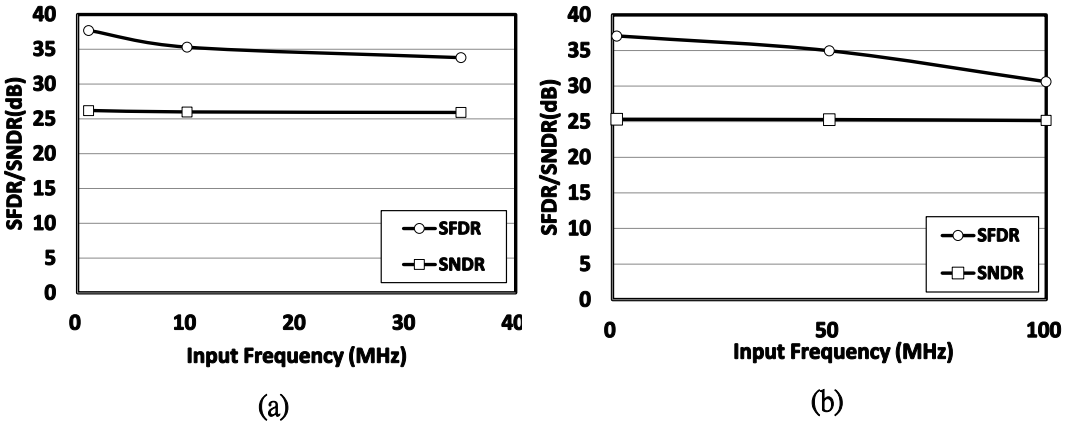

Figure 3-24 The measured SFDR and SNDR V.S. input frequency at (a) fs=100 MHz (b) fs=400MHz.

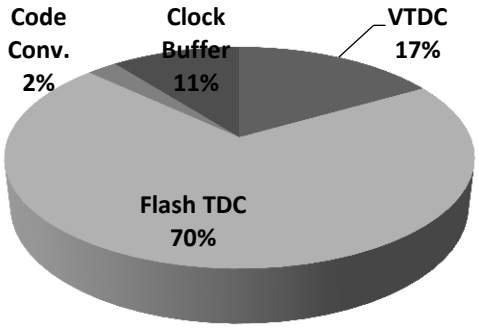

Figure 3-25 Power breakdown of the prototype ADC.

The total power consumption of the ADC is 16 mW at 1.8V supply. Figure 3-25 shows the power breakdown. The major power consumers are the VTC and flash TDC. The VTC consumes 17% of the total power because of high bandwidth requirements of the amplifier and buffer for delay-line bias regulated control. The flash TDC consumes 70% of the power of the ADC. The majority of the power is the dynamic current of the

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RC delay line in the comparison unit when delayed signals pass through it. Shrinking the inverters can reduce this significantly, but their sizes are limited by the device-matching consideration. The adoption of a more advanced process may effectively reduce the power consumption of the VTC and flash TDC.

Table 3-1 provides a performance summary of the prototype TADC. Table 3-2 shows a comparison with prior 0.18-μm CMOS high-speed ADCs with 3- to 7-bit resolution levels [38]—[43]. The figure of merit (FOM) is defined as following:

$$\mathrm{FOM} = \mathrm{Power}/(\mathrm{f_s} \times 2^{\mathrm{ENOB}}) \tag{3.11}$$

In table 3-3, the FOM results show that the power efficiency of the proposed TADC is sufficient and its performance is comparable to that of conventional voltage-type flash ADCs. Table 3-4 provides performance data of prior 4 to 8-bit high-speed-time-based ADC s for comparisons [44]—[47]. In [44], analog differential inputs are converted into two logic signals with a relevant time difference by two VTCs. After that, a Vernier type TDC is used to transfer the time difference to the relevant digital code. In this design, the ADC resolution and operating speed are limited by the long delay time of the cascaded delay cells. In [47], the proposed TADC is based on a

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remainder number system (RNS). It reduces the number of comparators and improves the power efficiency but the RNS system will exhibit an aliasing error if there is any impairment or noise in RNS quantizer. Sufficient numbers of quantization levels are therefore needed to minimize this error.

In [45] and [46], multiple VTCs are used in parallel to convert the input signal and the reference voltage simultaneously. The power consumption and input loading are doubled with the ADC resolution increased by every one bit. Moreover, the mismatch between these parallel VTCs needs to be calibrated [45] or averaged [46] by using auxiliary circuits. Compared to these time-based ADCs, the proposed VTDC only consumes less than 20% of total power. In other words, the majority of power consumption is due to digital circuits in the proposed TADC. It can be reduced significantly in case more advanced process is used.

Table 3-2 PERFORMANCE SUMMARY

Technology	0.18 μm CMOS
Resolution	5 bits
Supply Voltage	1.8V
Input Range	1Vpp
Sampling rate	0.4 GS/s
Power Consumption	20mW
DNL,INL @fin=1MHz	+/-1LSB, +/-1.7LSB
SFDR(@fin=100MHz)	30.7 dB

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SNDR(@fin=100MHz)	25.2 dB
ENOB(@fs=100MHz/400MHz)	4.01/3.89
FOM	2.69 pJ/conv.step

Table 3–3 PERFORMANCE COMPARISON (4-7 bits HIGH SPEED ADC IN 0.18 μm CMOS)

Ref.	Architecture	bits	fs(GS/s)	Power(mW)	Calibration	Area(mm^2)	FOM(pJ/Step)
[38]	Flash	4	4	43	None	0.06	2.14
[39]	Flash	4	4	78	Foreground	0.88	4.3
[40]	Flash	6	2	310	None	0.5	3.5
[41]	Flash	6	1	297	None	4	11.5
[42]	Flash	6	1	550	Foreground	1.96	16
[43]	Sub-Ranging	7	0.4	108	None	0.64	3.3
This work	Time-Flash	5	0.4	16(1.8v)	None	0.37	2.69

Table 3-4 PERFORMANCE COMPARISON (4-8 bits HIGH SPEED Time–Based ADC)

Ref.	Technology	bits	fs(GS/s)	Power(mW)	Calibration	Area(mm^2)	FOM(pJ/Step)
[44]	65 nm	4	5	34.6	Foreground	0.08	1
[45]	65 nm	6	10	98	Foreground	0.073	0.5
[46]	40 nm	7	2	27.4	None	0.052	0.21
[47]	65 nm	8	2	21	Foreground	0.08	0.12
This work	0.18 μm	5	0.4	16(1.8v)	None	0.37	2.69

3.5 Conclusions

In this chapter, a novel TADC is proposed and the prototype has been implemented in a 0.18-μm CMOS process. By using a front-end VTC circuit, traditional voltage or

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current domain signals can be more easily transferred to the time domain. The next stage, a flash TDC, contains nearly all digital circuit that is effective in low-power and high-speed design applications.

Conventionally, a high-speed voltage-type ADC tends to exhibit high power consumption in the comparator and reference circuits. The comparators in the proposed flash TDC are replaced with D-flip-flops and the reference voltage sources are replaced with different RC time constant delay cells, which are more robust in a low-voltage and noisy environment. Moreover, two TDCs can be integrated into one VTC through time interleaving to double the throughput rate. Compared with other high-speed ADCs, the proposed TADC is compatible with process scaling and is suitable for more advanced processes.

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Chapter 4

One Dimensional Eye-Opening Monitor (1D-EOM)

4.1 Introduction

The eye diagram is constructed from a digital waveform by folding the parts of the waveform corresponding to each individual bit into a single graph with signal amplitude on the vertical axis and time on the horizontal axis [48]. This is a methodology to represent and analyze a high-speed digital signal. By observing the eye diagram of a receiver, the link quality can be estimated and adjusted to reduce the bit error rate (BER) of data transmission. However, in many high-speed serial-link applications, it is usually difficult to measure the receiver signal and plot its eye diagram directly, for two main reasons. First, to drive a high-speed off-chip signal, a huge buffer size is inevitable, which always destroys the received signal, as a result of the excess capacitive loading. Second, due to the limited bandwidth of the buffer circuit, some inter-symbol interference will be introduced to the original received data. This implies that

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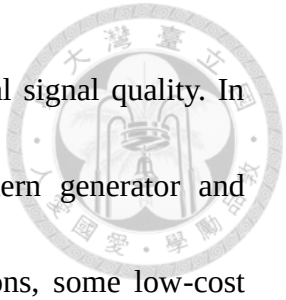

monitoring the off-chip eye diagram cannot truly reflect the internal signal quality. In addition, to obtain off-chip eye-diagram data, a high-speed pattern generator and oscilloscope are indispensable but typically costly. For these reasons, some low-cost on-chip eye-opening monitor (EOM) circuits have been proposed [49]－[60]. The built-in EOM circuits usually exist in parallel in the receiver data path in order to process the received data simultaneously. The extra loading contributed to the original data path is very small. Samrai and Yuan classified these on-chip EOM circuits into four types according to their architecture and hardware complexity [49]: the one-dimensional EOM (1D-EOM), the two-dimensional EOM (2D-EOM), the edge-based EOM, and the multi-sampling EOM.

A 1D-EOM quantifies the opening of data eyes by either the horizontal [50] or vertical [51],[52] dimensions. A 2D-EOM quantifies the eye-opening by measuring both the vertical and horizontal dimensions [53]－[57]. Edge-based EOMs quantify the eye opening by examining the edges of the data eyes [58]. Multi-sampling EOMs scan the data eyes both vertically and horizontally with a large number of samples [59]－[60]. Table 4.1 compares the strengths and weaknesses of different types of EOMs.

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Table 4.1 Strength and weakness comparisons of different type EOMs.

EOM Type	Clock phase	Compare level	Speed	Accuracy	Complexity
1-D H	Double	Single	Fast	Low	Low
1-D V	Single	Double	Fast	Low	Low
2-D	Double	Single	Fast	Medium	Medium
Edge	Multiple	Single	Slow	Medium	Medium
Multi-samples	Multiple	Multiple	Slow	High	High
This work	Multiple	Double	Medium	High	Low

The 1D-EOM, 2D-EOM, and edge-based EOM circuits typically output data in an analog or digital format to express the eye-opening size of the received data. This information can also be used to analyze the received signal integrity and channel loss. In many high-speed serial-link applications, the EOM circuit output is not only used to express the signal quality but also used to optimize the filter coefficients of the receiver front-end equalizer circuit, like the continuous time linear equalizer or the decision feedback equalizer, if the EOM output data rate is sufficiently fast.

In this chapter, an on-chip 1D-EOM scheme is proposed for equalizer adaptation based on multi-sampling EOMs. It can output the size of the horizontal eye-opening

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quickly enough to automatically optimize the high-frequency boost gain of the receiver equalizer. The extra overhead, including power consumption, hardware complexity, and excess load, is small enough to affect the original data path. This dissertation also proposes a novel multi-phase generator circuit without active or passive phase interpolator elements. The device mismatch problem that exists in the conventional interpolator circuit can be overcome by the proposed phase generator circuit.

This chapter is organized as follows. Section 4.2 describes the 1D-EOM architecture and its implementation. Section 4.3 presents the multi-phase generator circuit inside the 1D-EOM, and discusses the implementation in detail. Section 4.4 proposes a gain calibration scheme to fine tune the delay time of the phase generator. Section 4.5 details the measured performances, and Section 4.6 is a conclusion.

4.2 Proposed 1D-Horizontal EOM

Ellermeyer *et al*. [50] proposed a 1D horizontal EOM (1D-HEOM) circuit. This 1D-HEOM provides an analog output voltage that is proportional to the horizontal eye-opening of the received data. In this design, a rectangular eye-mask with fixed height is selected to compare with the real data. The maximum allowed width of the eye mask, *i.e.*, the eye traces that do not occur within the selected mask, is defined as the

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horizontal eye-opening. The result of this is not always accurate because the horizontal eye-opening varies with different selections of the eye-mask height. In addition, the rectangular eye-mask cannot always fit the profile of a real eye diagram. Consequently, the EOM reports an inaccurate analog output voltage.

Analui *et al*. [53] tried to fit eye-masks to the real eye diagram by combining more rectangular eye-masks of different heights and widths. These eye-masks had the same mask error rate. Krishnan and Pavan [60] reconstructed the whole eye by splitting the eye diagram into many small pixels and calculating the probability that the input waveform lay within each pixel. All pixel probability densities were saved and then the entire eye diagram was plotted.

The true eye diagram can be plotted but requires a large amount of data to be calculated. This has a long computational time and cannot easily be applied for real-time equalizer adaptations.With a trade-off between speed and accuracy, the proposed EOM circuit attempts to calculate the probability density in two given horizontal pixel lines in order to evaluate the horizontal eye-opening of the received data for equalizer adaptations. The architecture of the proposed EOM is illustrated in Figure 4-1 (a). The concept is to calculate the probability density of the waveform occurring in every pixel of the central rows (the blue-colored pixels). The operation is

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as follows. First, the input data is compared with the common-mode voltage and a voltage close to the common-mode voltage (*e.g.*, $y = 0$ and $y = \Delta v$). The comparison results are sampled by a fixed-phase clock (*e.g.*, $x = 1$). After K data points are compared, the sampling clock is switched to the next phase (*e.g.*, $x = 2$) and samples the next pixel. Their cumulative probability function (CDF) can be obtained by averaging the K points from the comparator. The difference between the CDFs at the two common-mode voltages (*i.e.*, $y = 0$ and $y = \Delta v$) is the probability density function (PDF) of the calculated pixel (*i.e.*, $x = 1$). The PDF for the N pixels can be obtained step-by-step (*i.e.*, $x = 1, 2, \dots, N$).

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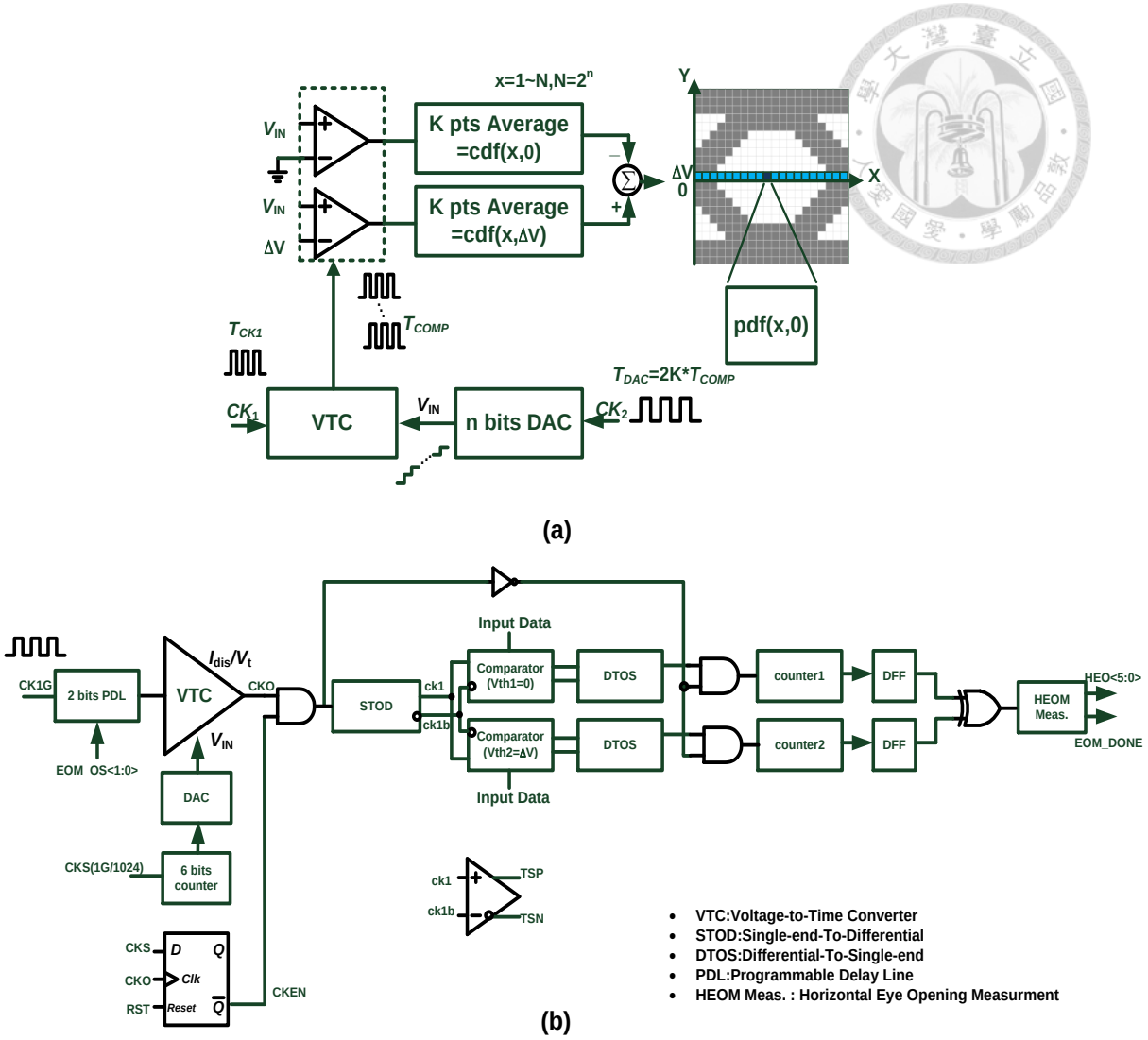

Figure 4-1 (a) The proposed 1D-EOM architecture. (b) The proposed 1D-EOM circuit block diagram.

In Figure 4-1, a voltage-to-time converter (VTC) and an *n*-bit digital-to-analog converter (DAC) are used to generate the multi-phase sampling clock for the comparators (*i.e.*, $x = 1, 2, \ldots, N$, $N = 2^n$). The time resolution of the clock phase is the bit time over the total pixel number in the horizontal dimension.

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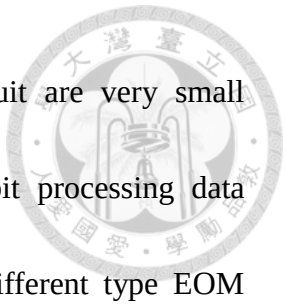

The power and area overheads of the proposed EOM circuit are very small compared to those of a traditional EOM circuit with a bit-by-bit processing data structure. Table 4.2 compares the power, area and data rate of different type EOM circuits. The implementation of the proposed EOM circuit is shown in Figure 4-1 (b). The differential inputs of the EOM are compared by comparators 1 and 2 simultaneously, and then the compared results are latched by the clock ck1 rising edge. The threshold voltages of the two comparators are the alternative current (AC) ground and an approximate AC ground, respectively. The differential sampling clocks ck1 and ck1b are converted by a single-to-differential conversion block. The various phases of the sampling clock are generated by the VTC block. The sampling clock source CK1G is provided by the clock and data recovery circuit. In addition, a two-bit programmable delay line (PDL) circuit is inserted in front of the VTC. The purpose of the PDL is to adjust the initial horizontal sampling position of the eye diagram.

The delayed CK1G signal is used as a reference clock for the VTC. The purpose of the VTC is to generate a clock signal output with uniform phase spacing where the spacing is proportional to the control voltage *V*IN. Here, a six-bit sequential ramp-up DAC provides the control voltage for the VTC. It consists of a current-mode DAC and an up-counter. Initially, the up-counter is reset to zero and the DAC output voltage *V*IN

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is set to its minimum. This forces the VTC output clock CKO to have the maximum delay time. After the first pixel calculation is completed, the up-counter ramps up and the DAC output *V*IN is incremented to reduce the VTC delay time pixel by pixel until all pixel calculations are finished. Due to the settling time requirement of the DAC, the VTC output clock CKO is valid only for half a cycle of the up-counter clock CKS. During the other half of the cycle of CKS, the VTC output signal is disabled.

In Figure 4-1 (b), the synchronization signal CKEN provides a mask signal to enable the VTC output CKO. Therefore, there is half a cycle of the counter clock CKS for the DAC settling time requirement every time the up-counter value is changed. The two parameters, I_{dis} and V_t, of the VTC are used to adjust its transfer gain and offset, respectively. Here, I_{dis} is defined as the discharge current and V_t is the threshold voltage of the comparator inside the VTC. Section 4.3 will discuss the VTC operation in detail.

The comparator adopted in the proposed EOM circuit is a current-mode logic (CML) D-flip-flop, consisting of two CML latches. A detailed schematic is shown in Figure 4-2. In order to achieve a small difference in the threshold voltages of the two comparators, one of the comparators in the input differential pair has a slightly different size. Following these two comparators is a differential-to-single-end block. The purpose of this block is to convert the differential output into a single-end rail-to-rail signal. The

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circuit implementation is shown in Figure 4-3. Some digital circuits, including counters, D-flip-flops, and XOR gates, are used to perform the CDF and PDF calculations. The calculated result is sent to the final stage to evaluate the size of the horizontal eye-opening. Finally, the proposed EOM circuit will provide a six-bit digital output signal HEO to express the size of the horizontal eye-opening.

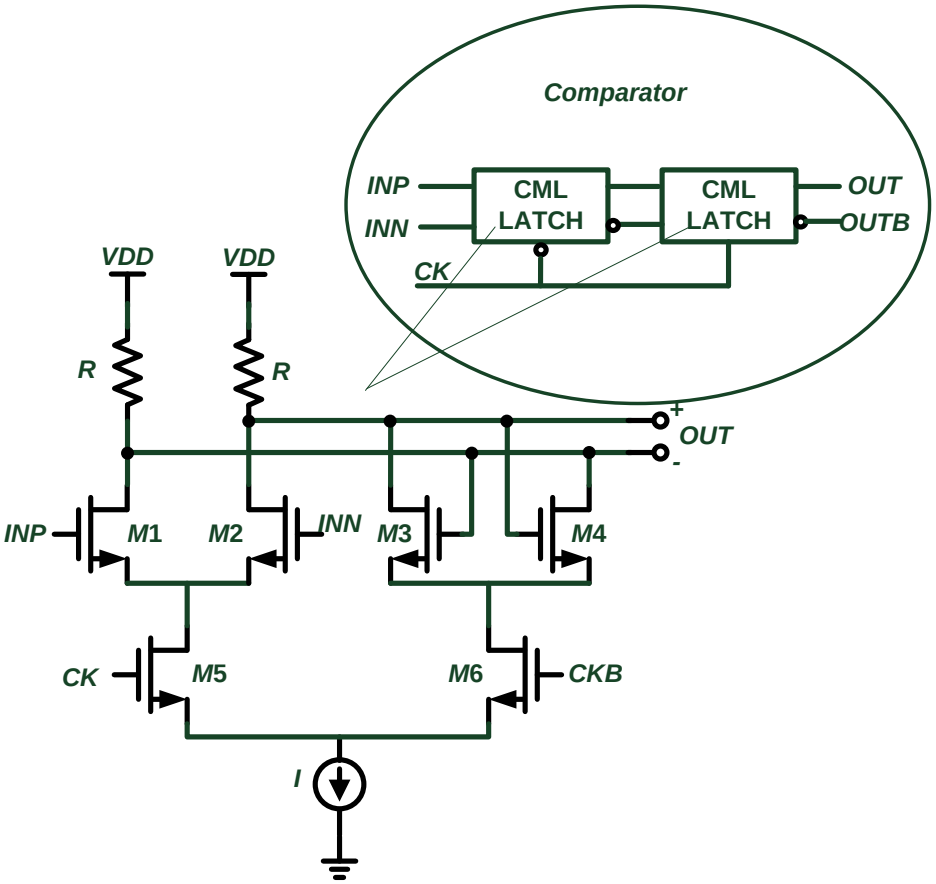

Figure 4-2 Comparator circuit.

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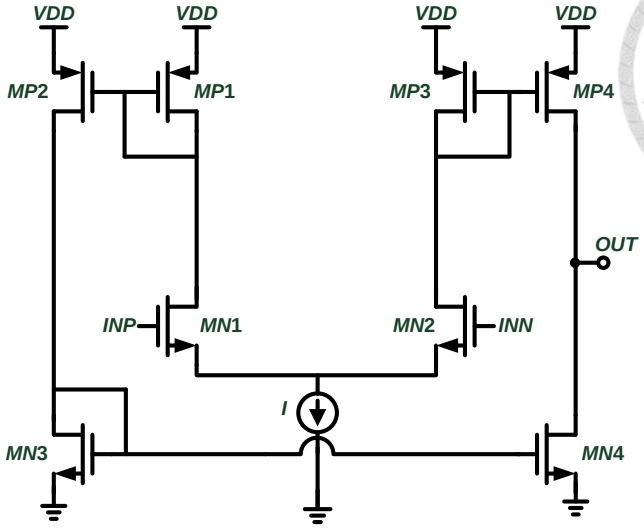

Figure 4-3. Differential-to-single end circuit.

Figure 4-4 shows the waveform from a 1D-HEOM simulation. Figure 4-4 (a) depicts the EOM input eye diagram. The input data rate is 10 Gbps and the channel loss is 5.4 dB. Figure 4-4 (b) displays the sampling clock, VTC DAC output, counter 1 output (CDF1), counter 2 output (CDF2), XOR gate output (PDF), and HEOM counter output (this value represents the horizontal eye-opening). Here, counter 1, counter 2, and the XOR gate are all ten bits and the HEOM output is six bits. The XOR gate output expresses the PDF of the horizontal pixels of the eye diagram, shown by waveform (5) in Figure 4-4 (b). It can be seen that data edge in some pixels occur if the pixels has large PDF values. The eye diagrams for different channel losses between 5 and 14 dB versus the 1D-HEOM simulation results are shown in Figure 4-5 and Figure 4-6 for

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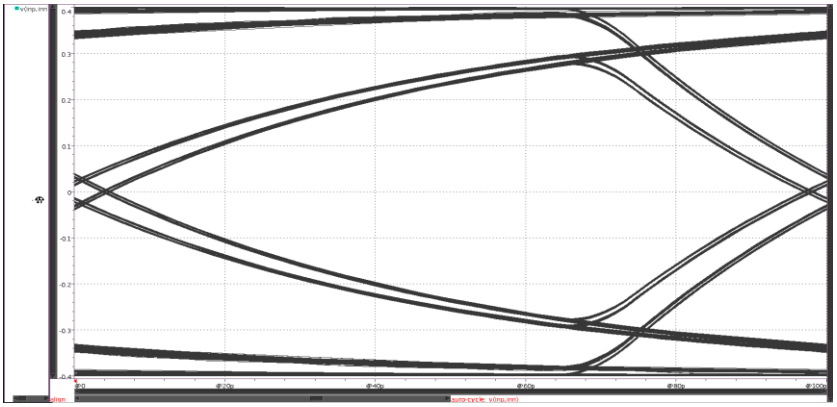
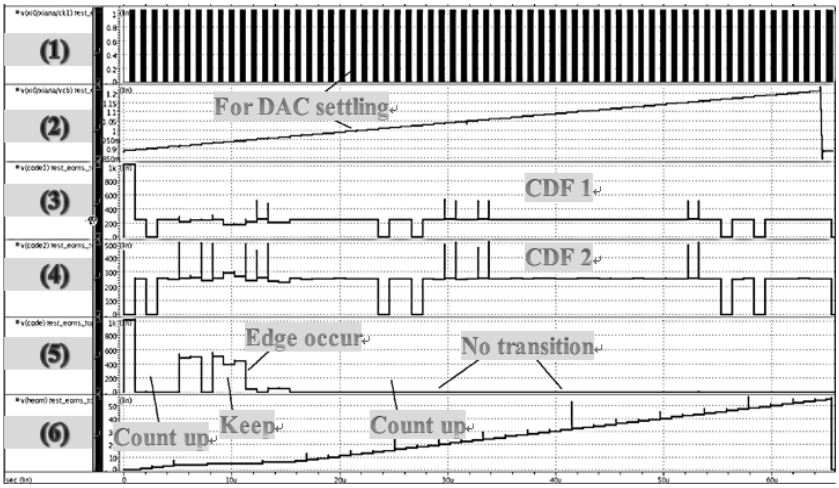
comparisons. Figure 4-4 (a) depicts the eye diagrams of the different EOM input data and Figure 4-4 (b) presents the corresponding PDF and the calculated HEOM results.



(a)



(b)

Figure 4-4 (a) EOM input eye diagram. (b) 1D-EOM related waveform.VTC output clock (for EOM sampling). (2) VTC DAC output. (3) Counter 1 output. (4) Counter 2 output. (5) XOR gate output. (6) HEOM<5:0> counter output results.

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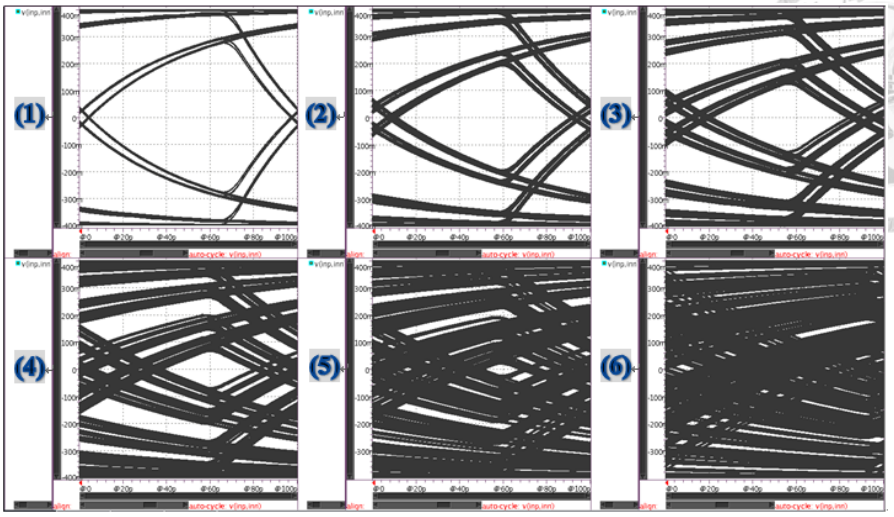

Figure 4-5 Input eye diagram VS. Different channel loss.

(1) Loss=5.4dB. (2) Loss=7.6dB. (3) Loss=9.5dB.

(4) Loss=11.1dB. (5) Loss=12.5dB. (6) Loss=13.7dB.

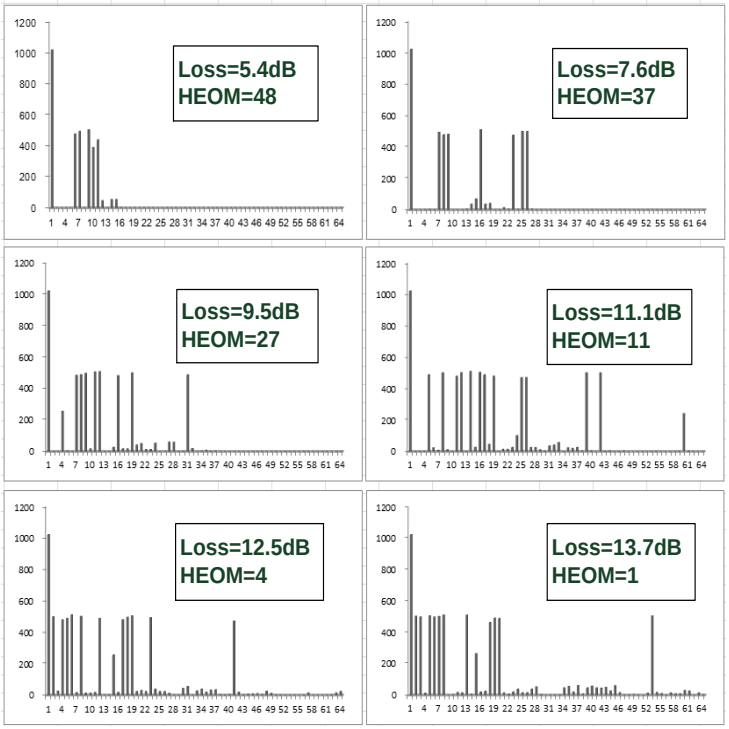

Figure 4-6 64 pixels PDF calculation results VS. Different channel model.

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4.3 Voltage-to-Tim Difference Converter (VTC)

The main functional block of the proposed 1D-EOM is the VTC. VTC, is a signal converter, convert a voltage-type signal to a time delay signal. It has been widely used in time-to-digital converter [61] or time domain ADC [62]. The purpose of the proposed VTC is to generate a clock signal for sampling the EOM horizontal pixel data. The sampling clock is shifted by a fixed delay once the PDF calculation for a pixel is completed. The VTC outputs a sampling clock with equal phase shift for the sampling input data of the EOM comparators. The basic concept of the proposed VTC is to adjust the fall time of the reference clock according to the analog control voltage *V*IN. A detailed schematic and the corresponding timing diagram are shown in Figure 4-7 (a) (b). Different *V*IN values imply different discharge levels, which ultimately result in different fall times. In Figure 4-7 (b), the discharge rate on node *V*C1 is constant and independent of *V*IN.

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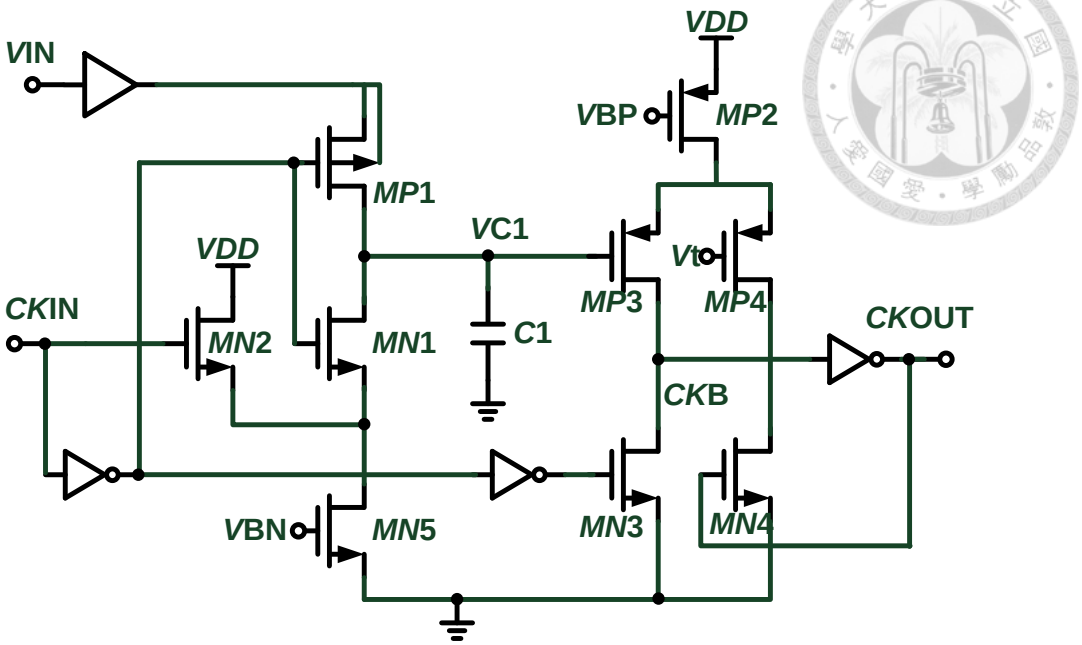
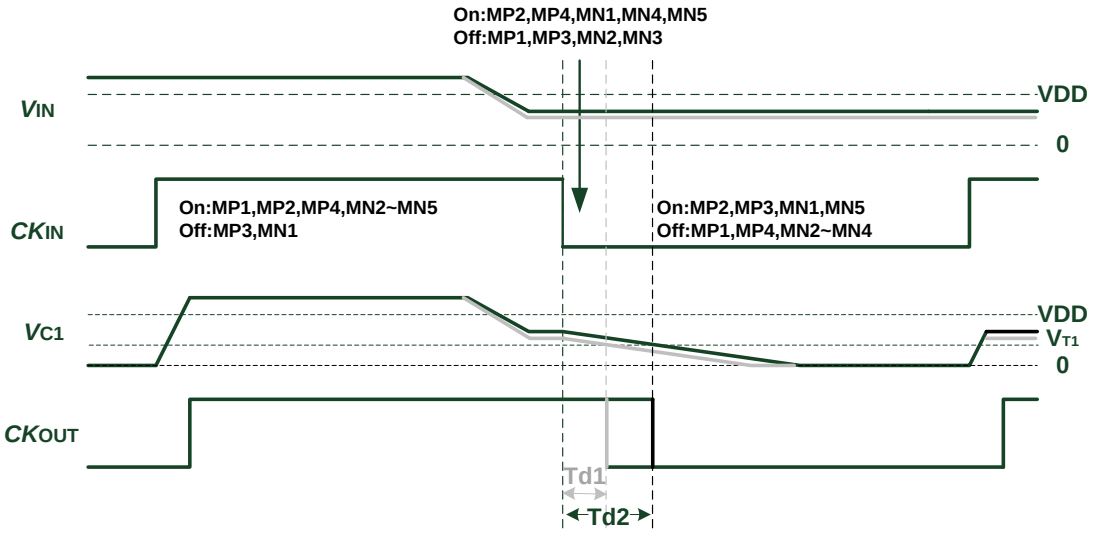


(a)



(b)

Figure 4-7 (a) Detail schematic of proposed VTC. (b) The corresponding timing diagram of proposed VTC

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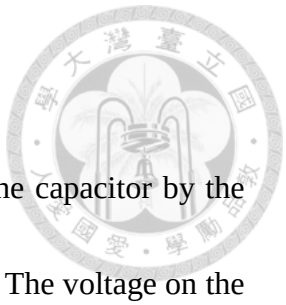

4.3.1 VTC operation

The input analog control voltage *V*IN (~*VDD*) is sampled on the capacitor by the PMOS switch MP1 when the reference clock *CK*IN is a logical high. The voltage on the capacitor *V*C1 will follow *V*IN until *CK*IN is changed to a logical low. This operation is defined as the sampling phase. During the sampling phase, transistors MP1, MP2, MP4 and MN2 to MN5 are turned on, and transistors MP3 and MN1 are turned off. Thus, the output signal *CK*OUT is pulled to a logical high after the delay from two inverters.

When *CK*IN switches to a logical low state, transistors MP1 and MN2 are opened and MN1 is closed. All current from *MN5* is switched to MN1. Transistors MN1 and MN5 constitute a discharge path to ground, where capacitor C_1 is discharged. This operation is defined as the discharge phase. The capacitor's output is connected to a comparator circuit, which is composed of transistors MP2 to MP4, MN3 and MN4. The waveform for node *V*C1 is shown in Figure 4-7 (b), where I/C_1 is the slew rate and *I* is the current through MN5. Since the fall time of the clock signal on node *V*C1 is extremely slow, the accuracy of the comparator threshold voltage has a significant effect on the overall delay time T_d etween CK_{IN} and CK_{OUT}.

The threshold of conventional inverter-based comparators is very sensitive to process–voltage–temperature (PVT) variations. This variation induces delay offsets in

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the VTC. The simulation presented in Figure 4-8 (a) illustrates this phenomenon.

The transfer gain of the VTC is almost constant but the offset is process-dependent. The offset variation can be alleviated by using complicated circuit techniques, such as body-bias compensation [63],[64]; however, this is not suitable for practical high-speed circuit design. A current-steering structure is sufficiently accurate compared to the practical inverter-based comparator. The threshold voltage is controlled satisfactorily by a preset voltage V_t and the source current of the transistor MP2. Figure 4-8 (b) shows the simulation results in contrast with Figure 4-8 (a). When *V*C1 is far from V_t, all the current from MP2 passes through MP4 and MN4. Once *V*C1 drops, transistor MP3 is turned on and a part of the current from MP2 flows through MP3 to charge the node $CK_{B.}$ When the voltage on node CK_B is sufficiently high, the output *CK*OUT changes into a low state. In the case that *CK*OUT becomes sufficiently low, transistor MN4 is turned off to block the short current path. Furthermore, transistor MN4 forms a positive feedback path to the node CK_B. It helps to speed up the transition of *CK*OUT.

This conversion is completed after a falling edge occurs at *CK*OUT. *V*C1 discharges continuously until the next rising edge occurs at the sampling clock. If the input voltage *V*IN (~*VDD*) is either larger or smaller than the comparator threshold, then the falling edge delay difference between *CK*IN and *CK*OUT is longer or shorter,

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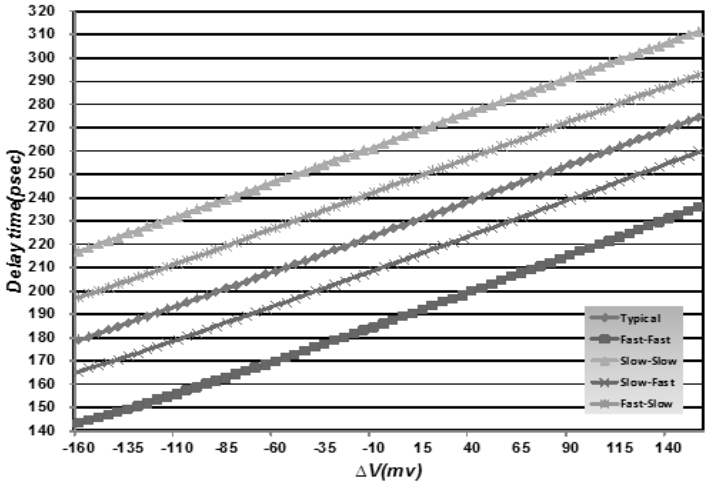
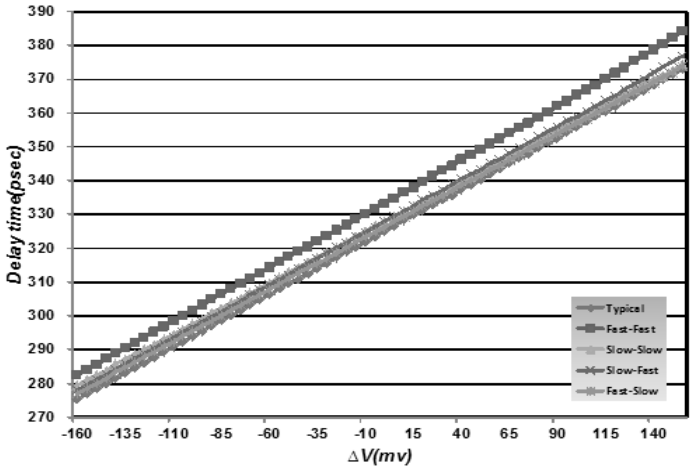
respectively. That is, a voltage-to-delay conversion is performed. Figure 4-9 shows the simulated eye diagram of the VTC output after the EOM is converted. The phase difference of the EOM clock is approximately 1.56 picoseconds.



(a)



(b)

Figure 4-8 (a) VTC transfer gain simulation results based on inverter based comparator. (b) VTC transfer gain simulation results based on the proposed comparator.

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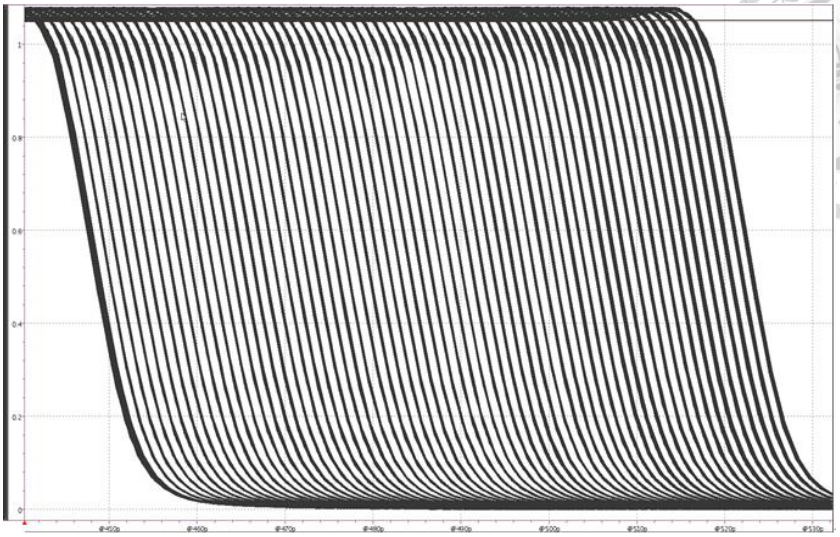

Figure 4-9 Simulated eye diagram of VTC output.

4.3.2 Circuit Design Considerations

Some critical design considerations are highlighted here. The first issue is the maximum and minimum *V*IN range. If the signal range for *V*IN is defined as $VDD \pm \Delta V$, then the upper bound of ΔV can be determined by the maximum allowed gate-to-source overdrive voltage of transistor MP1. In general, this is recommended to be less than 20% of *VDD* due to the process reliability issue. The lower bound is limited by the minimum gate-to-source voltage of the transistor MP3 that is turned off while *V*IN is sampled on the capacitor C_1. The input range of *V*IN can be derived from Equation (4.1):

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$$VIN, max = 1.2 \times VDD \ \ and$$

$$VIN, min \ = \ Vt \ + \sqrt{\frac{2 \times I_2}{K_4 \left(\frac{W}{L}\right)_4}} + \left(V_{tp4} - V_{tp3}\right) \ , \qquad (4.1)$$

where I_2 is defined as the current through transistor MP2.

The second design consideration is the short current issue in the circuit. When *CK*IN is a logical low and the gate of the transistor MP1 is set to *VDD*, there may be a short current path from *V*IN to ground in the case that *V*IN is much higher than *VDD*. This weak turn-on characteristic of MP1 will affect the accuracy of the total discharge current with the leakage error being signal-dependent. Furthermore, a weak MP1 would also lower the sampling speed and quality of the VTC; for example, this would enlarge the switch's RC time constant. The size of transistor MP1 should be selected to fit the minimum turn-on and maximum turn-off resistance values.

The transfer gain variation of the VTC was also addressed. The transfer gain can be derived as follows:

$$TD_{F(VIN)} = TD_{SW12} + \ TD_{DISCHARGE} + TD_{COMP}$$

$$\approx \ TD_{DISCHARGE} + TD_{COMP} = \frac{C_1}{I_{MN5}}(VIN - V_{T1}) + CONST. \qquad (4.2)$$

$$\mathrm{G} = \frac{\mathrm{d}TD_{F(VIN)}}{\mathrm{d}VIN} = \frac{C_1}{I_{MN5}} \qquad (4.3)$$

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where TD_F is defined as the falling-edge delay difference between CK_{IN} and CK_{OUT}. It is equal to the summation of TD_{SW12}, $TD_{DISCHARGE}$, and TD_{COMP}. TD_{SW12} is defined as the switching time when the current provided by the transistor MN5 is fully switched to MN1. $TD_{DISCHARGE}$ is the effective discharge time, starting from the point when MN1 is fully turned on to the point when VC1 drops below V_{T1}. The current passing through transistors MP3 and MP4 is equal during this period. TD_{COMP} is defined as the comparator response time. Compared to the other variables, TD_{SW12} can be neglected and TD_{COMP} can be assumed as a constant delay because the input slew rate of the comparator on node VC1 is almost the same regardless of the value of VIN. Consequently, the VTC transfer gain G is roughly equal to the capacitor C_1 value over the discharge current of transistor MN5. This result is shown in Equation (4.3) and TD_F can be rewritten as:

$$TD_{F(VIN)} = TD_{F(VIN,min)} + G \times (VIN - VIN, min) \quad (4.4)$$

According to Eq. (4.3), the transfer gain variation is dependent on the accuracy of capacitor C_1 and the discharge current I_{MN5}.

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4.3.3 VTC Linearity

The influence of linearity on the VTC can be analyzed in a different operation mode. In sample mode, the sampling switch's turn-on resistance *Ron* and drain-to-body junction inverse capacitance *Cdb* introduce signal-dependent errors if the sampling switch has body effect. Here, the sampling switch is a PMOS and the body is connected to *V*IN. Going from sample mode to hold mode, the aperture jitter of the sampling clock introduces signal-dependent errors due to its finite fall time. For a high-speed and high-accuracy data converter, a low-jitter clock circuit is required. However, here, it is necessary to enhance clock buffer driving capability to reduce sampling uncertainty in the sample mode.

In discharge mode, the accuracy of the current source MN5 and capacitor C_1 introduces signal-dependent errors. Here, a reasonably enlarged channel length for transistor MN5 and a metal-oxide-metal capacitor is used for C_1 to minimize these non-ideal effects. Furthermore, the second-order harmonic distortion contributed by the non-ideal current source MN5 can be eliminated by using the differential signal from the two VTCs, as shown by Equation (4.5):

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$$TD\_F(VDD+\Delta V)-TD\_F(VDD-\Delta V)=\frac{C_1(VDD+\Delta V)}{I+(\Delta V/R_o)}-\frac{C_1(VDD-\Delta V)}{I-(\Delta V/R_o)}$$
$$=\frac{C_1(VDD+\Delta V)}{I(1+\Delta I/I)}-\frac{C_1(VDD-\Delta V)}{I(1-\Delta I/I)}\sim\frac{C_1(\Delta V)}{I}\left(1-\frac{\Delta I}{I}+\left(\frac{\Delta I}{I}\right)^2-\cdots\right)$$
$$-\frac{C_1(\Delta V)}{I}\left(1+\frac{\Delta I}{I}+\left(\frac{\Delta I}{I}\right)^2+\cdots\right)\sim\frac{C_1(\Delta V)}{I}\left(\frac{\Delta I}{I}\right) \quad (4.5)$$

4.3.4 VTC Offset and gain Error

The transfer function of the VTC can be expressed as Equation (4.2). The offset error (*CONST*.) is the intrinsic delay variation of the VTC. The constant delay comes from the inverter delays plus the comparator response time which are both sensitive to PVT variations, and results in the measured eye shifting.

This shift can be compensated for by the front-end delay-line circuit and does not affect the EOM calculation results. The gain error is the result of variations in the current source MN5, capacitor C_1, and some parasitic capacitances linked to *V*C1. It results in eye-size mismatches and needs to be calibrated. Figure 4-10 shows the sampling clock variations due to the VTC offset and gain error. The gain error calibration scheme is provided in Section 4.4.

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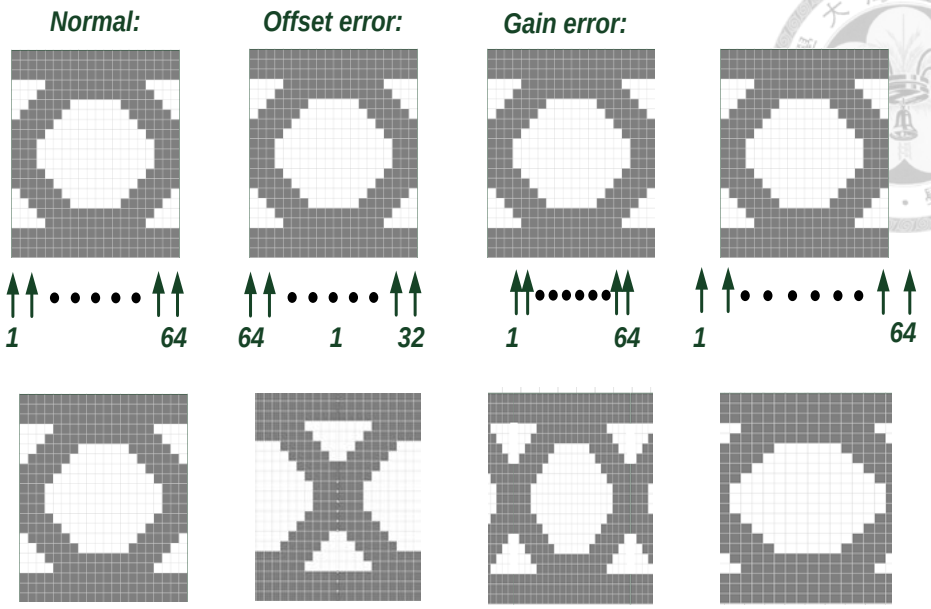

Figure 4-10 Sampling clock variations due to the offset and gain error of the VTC.

4.3.5 VTC jitter

The VTC output clock jitter will affect the measurement accuracy of horizontal eye-opening of the real data. Figure 4-11 is the simplified VTC noise model. Assuming that thermal noise is dominant, the noise power on *V*C1 is kT/C_1 in the sampling mode, where k is the Boltzmann constant and T is the absolute temperature. It is not the majority of VTC output jitter. In the discharge mode, VTC can be modeled as a lossless integrator. Suppose i_n is a noise current of MN5 that integrates on capacitor C_1 over a time interval t_d. The integrated noise voltage $\langle v_n^2 \rangle$ on capacitor C_1 is derived from [65] and can be expressed as follows:

$$\langle v_n^2 \rangle = \frac{S_{i_n}}{2{C_1}^2} t_d \quad , \tag{4.6}$$

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where S_{i_n} is the noise current spectra density of MN5 and t_d is defined as a discharge time. The discharge current *I* (through MN5) produces a mean-squared jitter $\langle \sigma_t^2 \rangle$ that can be derived as follows [18]:

$$\langle \sigma_t^2 \rangle = \frac{\langle v_n^2 \rangle}{(Slew\ rate)^2} = \frac{{C_1}^2 \langle v_n^2 \rangle}{I^2} = \frac{S_{i_n}}{2I^2} t_d \quad , \tag{4.7}$$

The slew rate of proposed VTC is constant and equals to the discharge current *I* over capacitance value C_1. Since the discharge time is defined as Equation (4.2) , Equation (4.7) can also be rewritten as follows:

$$\langle \sigma_t^2 \rangle = \frac{S_{i_n}}{2I^3} C_1 (VDD \pm \Delta V - V_1). \tag{4.8}$$

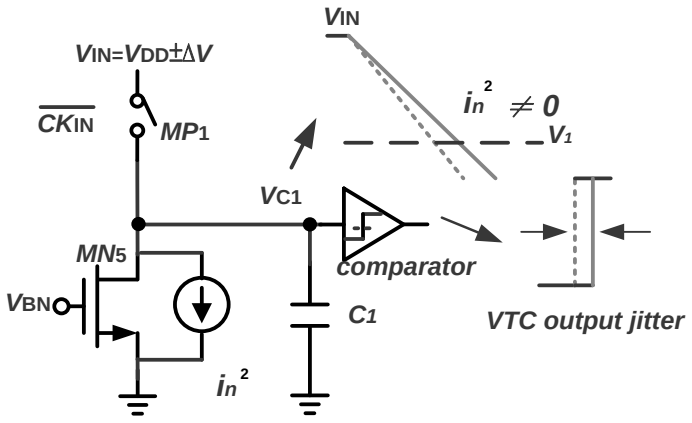

Figure 4-11 Sampling clock jitter due to discharge current source MN5.

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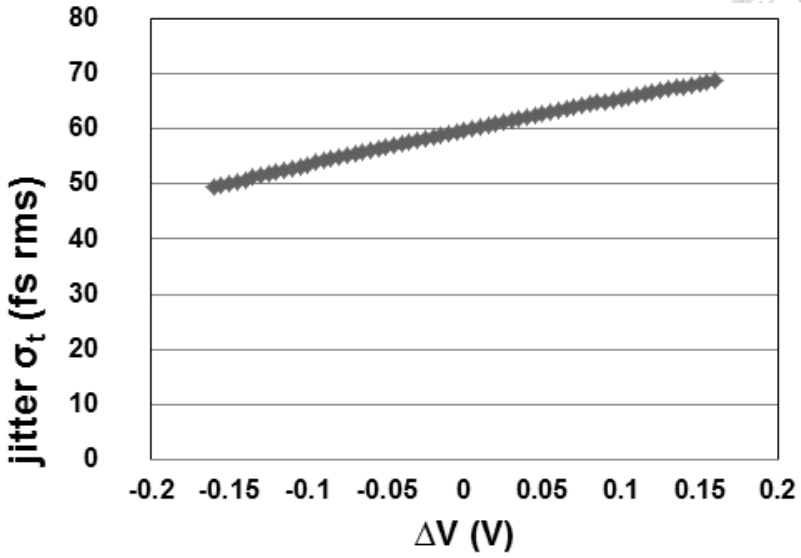

Figure 4-12 The hand-calculated VTC RMS jitter versus ΔV.

Using Eq. (4.8), the hand-calculated VTC RMS jitter versus ΔV is shown in Fig. 4-12. The results are 50 fs to 70 fs depending on different VIN levels. Figure 4-13 (a),(b) and (c) also show the simulated horizontal eye-opening versus VTC output clock with different RMS period jitter (PJ). According to the simulation results, the measurement error of the reported HEOM value is roughly 10%~15%. It can be estimated since it is closely related to the VTC RMS jitter. Also, the jitter can be further reduced by increasing the discharge current.

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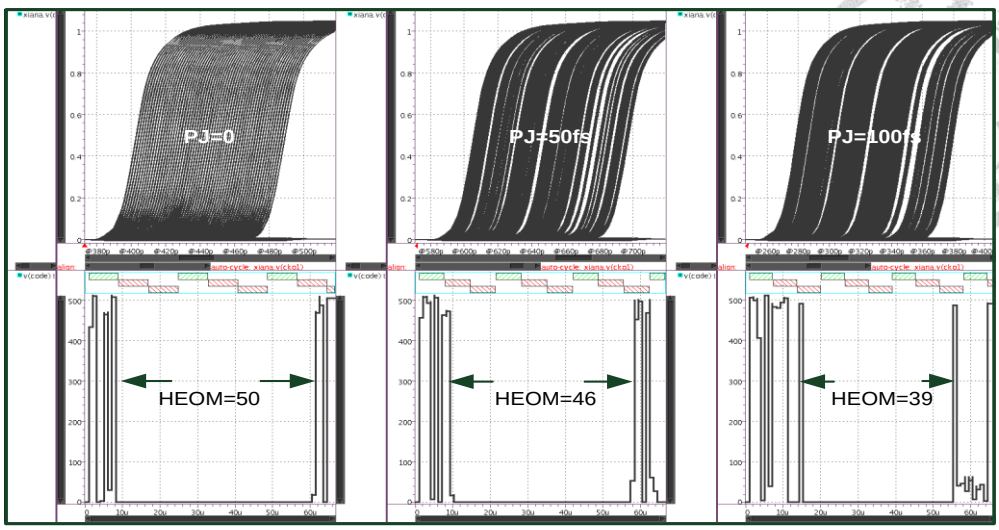

Figure 4-13 The simulated horizontal eye-opening versus VTC output with different RMS period jitter (PJ) at (a) PJ=0, HEOM=50, (b) PJ=50fs, HEOM=46, and (c) PJ=100fs, HEOM=39.

4.3.6 VTC Mismatch

The VTC mismatch is defined as the variation of the output clock phase difference. It will result in comparator sampling data uncertainty. According to Eq. (4.4), the mismatch of the falling-edge delay is due to VIN variation and VIN is supplied by a 6-bit DAC. The DAC mismatch will cause phase difference variation on VTC clock. Fig. 4-14 (a) (b) show the calculated differential non-linearity of the 6-bit DAC and the VTC output phase difference from the Monte Carlo simulation data. It demonstrates that the DAC output VIN and VTC output phase difference are fairly uniform. The simulated DNL of the 6-bit DAC and the VTC output phase difference are ±0.25 LSB

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(1LSB=5mv) and ±0.35 LSB (1LSB=1.5625ps) respectively.

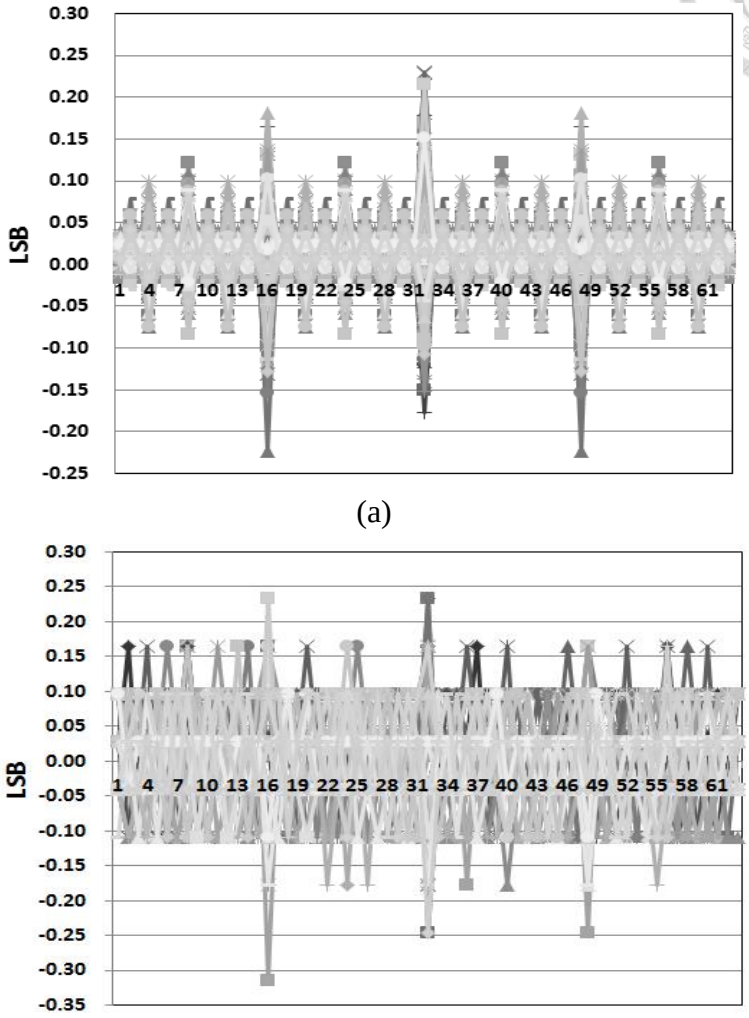

Figure 4-14 The simulated differential non-linearity (DNL) of (a) the 6-bit DAC, and (b) the VTC output phase difference.

4.4 VTC Gain Calibration

The offset and gain error of the VTC are sensitive to PVT variations. A block diagram of the proposed gain error calibration circuit is shown in Figure 4-15. VTC1 is the main delay circuit using in EOM and VTC2 is the auxiliary delay circuit duplicated

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from VTC1. The calibration procedure uses the following equations:

$$TD1,max = TD1,min + G \times (V_{IN,max} - V_{IN,min}), \quad (4.9)$$

$$TD1,min = TD2,min, \quad (4.10)$$

$$TD1,max = TD2,min + TD\_BUF = TD1,min + TD\_BUF, \text{ and}$$

$$G = \frac{TD\_BUF}{V_{IN,max} - V_{IN,min}}. \quad (4.11)$$

First, the minimum delay of VTC2 is set to that of VTC1 by appropriately adjusting the threshold V_t of the VTCs's internal comparator. The minimum delay extraction circuit is shown in Figure 4-15 (a). It consists of two VTCs, a current DAC, a phase comparator, and a counter. The operation can be explained as follows. Two VTCs output delayed clock signals CK_1 and CK_2, and their delay time is proportional to the magnitude of *V*IN. A phase comparator compares these two signals and outputs an indicator UP. If CK_1 leads CK_2, then the indicator UP outputs an active high. The UP signal is used to trigger the counter to increment. Initially, the UP counter is reset to zero. This forces the DAC to provide no offset outputs to V_{t1} or V_{t2}. Then, V_{t1} and V_{t2} are used to control the threshold voltage of the two VTCs and are equal in the initial state.

The purpose of the DAC is to provide an offset voltage to V_{t1} or V_{t2} according to

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the phase comparator decision (lead or lag) and the UP counter value. When the calibration process begins (the START signal is set to active high), the two VTC inputs *V*IN are shorted to V_{min} (the minimum allowed input voltage). If the two VTC circuits have a mismatch, then their outputs CK_1 and CK_2 have a phase difference. The phase comparator decides which output leads the other and then switches the DAC output to the lagging output.

The DAC provides an offset voltage to the lagging output according to the UP counter value until the phase comparator's decision is reversed. At this point, the offset calibration is completed and the UP counter's value is latched. The START signal is then set to inactive, waiting for the next calibration.

After the minimum delay extraction process, CK_1 and CK_2 are synchronized at V_{min} at the input to satisfy Eq. (4.10). Then the gain calibration process can start. Figure 4-15 (b) shows the gain error calibration scheme. The inputs *V*IN of VTC1 and VTC2 are set to V_{max} and V_{min}, respectively. The phase comparator compares the VTC1 output with the VTC2 output plus a buffer delay, where the delay time is denoted by *TD_BUF*. The buffer circuit is the same as the delay cell inside a built-in delay-locked loop (DLL). The target delay time of the DLL delay cell is set to be equal to the difference between the maximum delay and the minimum delay of VTC1 while it is locked.

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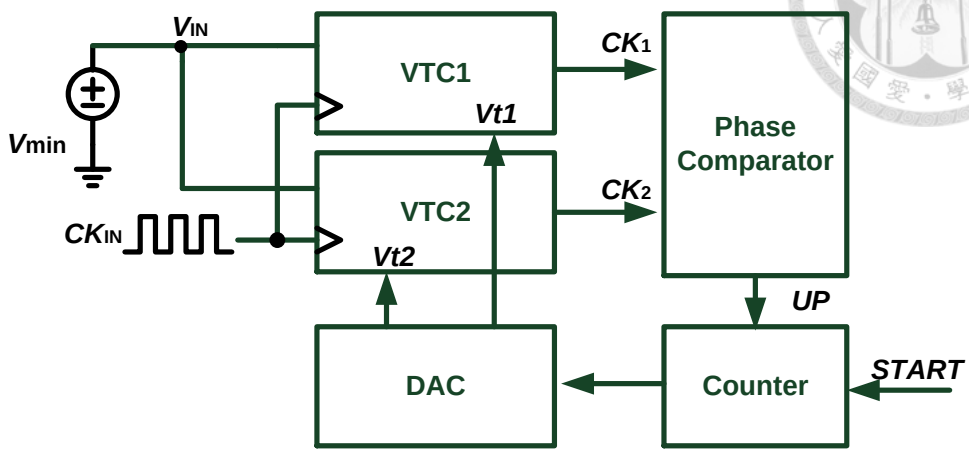
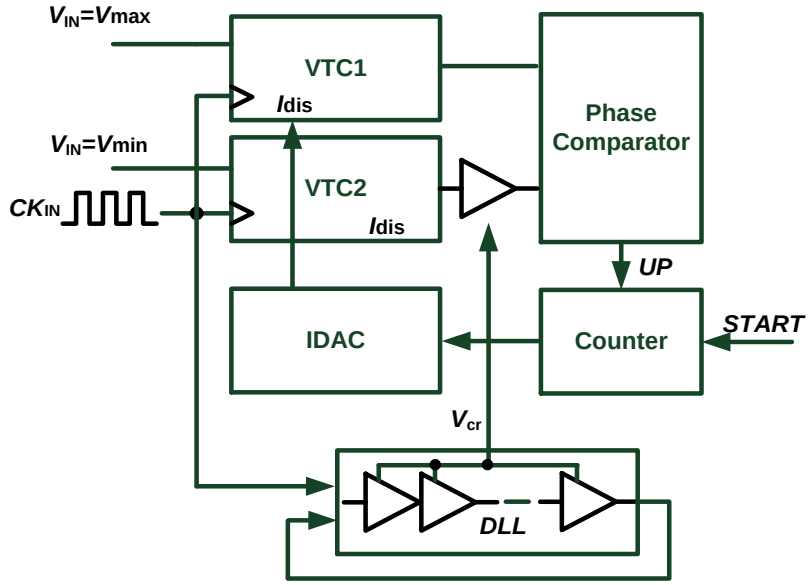


(a)



(b)

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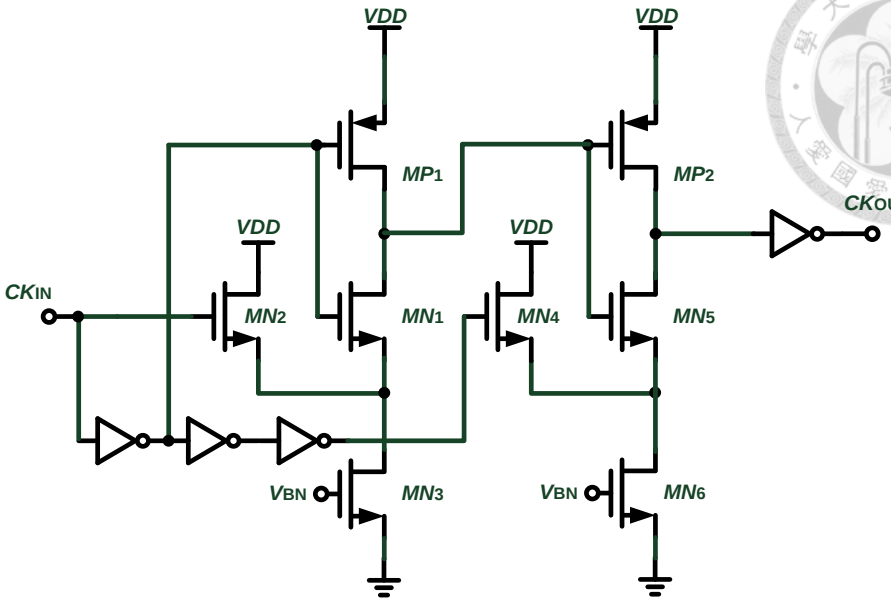

(c)

Figure 4-15 VTC gain error calibration circuit. (a) Minimum delay extraction scheme. (b) Gain calibration scheme. (c) DLL delay buffer circuit.

In Figure 4-15 (c), the DLL outputs a control voltage *V*cr to fine-tune the buffer delay to mitigate PVT variations. This calibration procedure is similar to the minimum delay extraction process. The only difference is that the DAC output is always switched to the current-calibrated VTC to provide an offset to the discharge current inside the VTC. The design must guarantee that the delay time of VTC1 at maximum *V*IN is longer than that of VTC2 at minimum *V*IN plus a buffer path in the initial state. As the UP counter is increments, the discharge current through the current DAC output increases until the phase comparator output polarity is reversed. The counter's result is

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latched, and the gain calibration process is finished. The transfer gain of VTC1 can be obtained by Equation (4.11).

Figure 4-16 shows the results of a Monte Carlo simulation, depicting the delay time mismatch between the VTC1 and VTC2 outputs when their input *V*IN is minimum. The standard deviation is 10.2 ps. Figure 4-17 (a) presents the proposed phase comparator circuit. It consists of a time difference amplifier [2] and a latch-type phase detector. Figure 4-17 (b) shows the simulation results for accuracy of the method with device mismatch. There are a total of one thousand samples in this simulation. It is not intuitive to see the calibration performance on 1D-EOM circuit. A two dimensional EOM model with VTC calibration scheme was built up and the simulated eye diagram is shown in Figure 4-18 (a) (b) and (c). The simulation results show the change of eye size during VTC calibration.

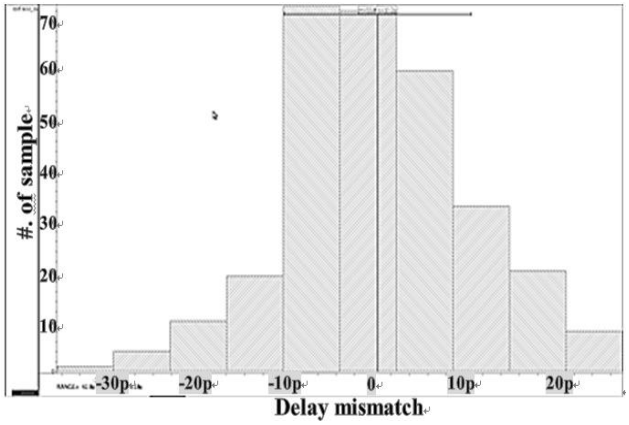

Figure 4-16 The delay mismatch of VTC1 and VTC2 at minimum *V*IN.

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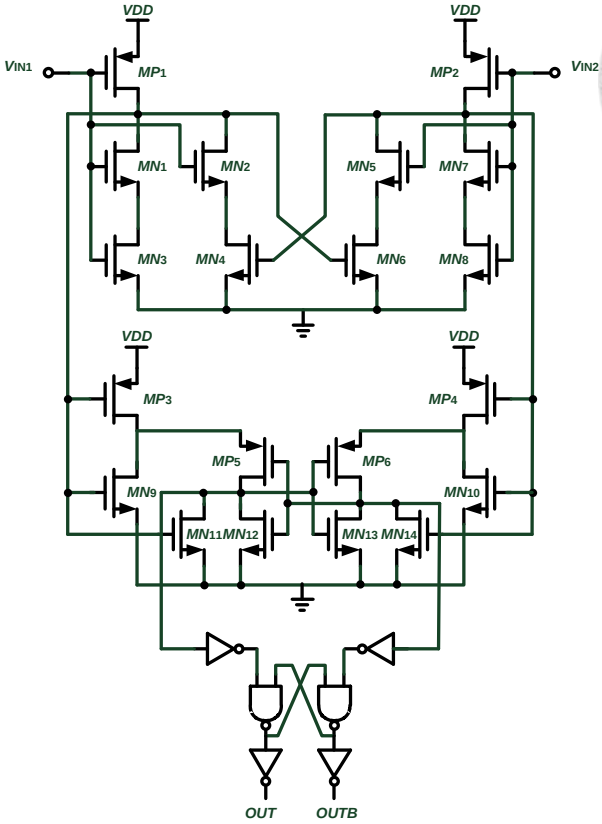
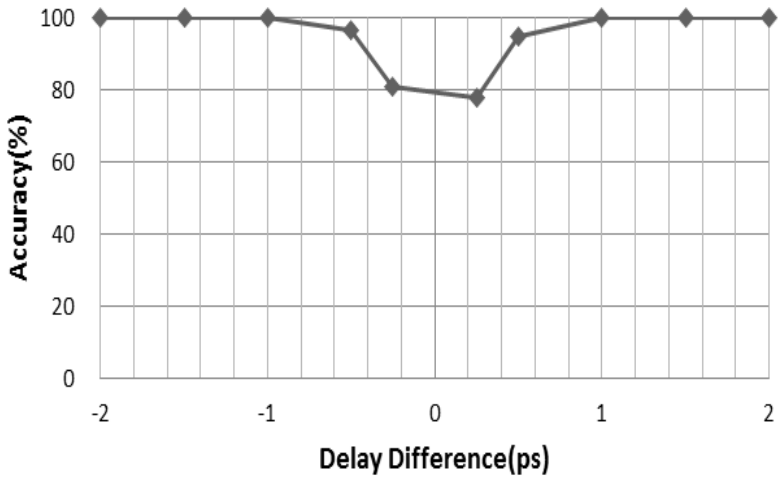


(a)



(b)

Figure 4-17 Phase comparator. (a) Schematic. (b) Accuracy.

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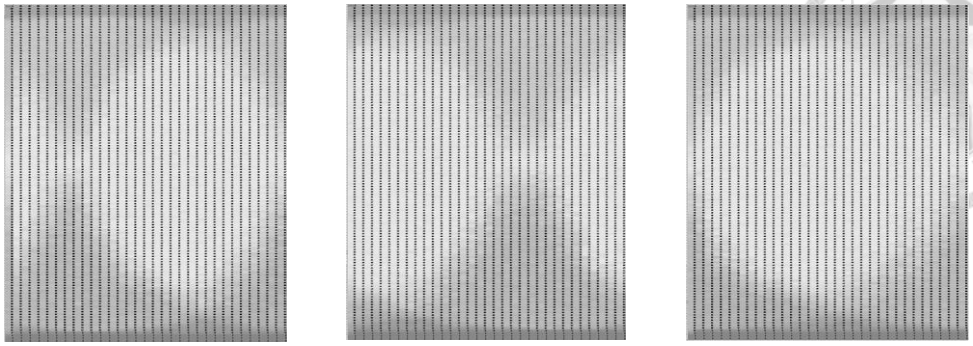

Figure 4-18 Simulated eye diagram during VTC calibration. (a) Before calibration. (b) During calibration. (c) After Calibration.

4.5 Experimental Results

The test chip is designed for the SuperSpeed Universal Serial Bus (USB) 10 Gbps (USB3.1 Generation 2) specification. The proposed 1D-EOM circuit was included in the receiver side. This chip was designed and fabricated using a 64-nm CMOS process. The layout area of the EOM is 60 μm × 450 μm and the total power consumption is 1.5 mW. Figure 4-19 shows the test chip die photograph and Figure 4-20 shows the power breakdown. The majority of power is consumed by two comparator circuits. STOD and DTOS blocks are also included. They all consume 70% of the total power. The major power consumers are high speed latch circuits. In addition, the VTC and logic circuit consumes 15% and 10% of the total power, respectively. The calibration circuit only consumes 5% because they are almost powered down after the calibration process is

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finished. The 1D-EOM circuit was used to capture the receiver's front-end equalizer output waveform and calculate its corresponding horizontal eye-opening. Then, the calculated result was compared to an expected eye-opening value. If too small, then the boost gain of the equalizer was enhanced to extend the horizontal eye-opening. The EOM results were updated every 64 μs.

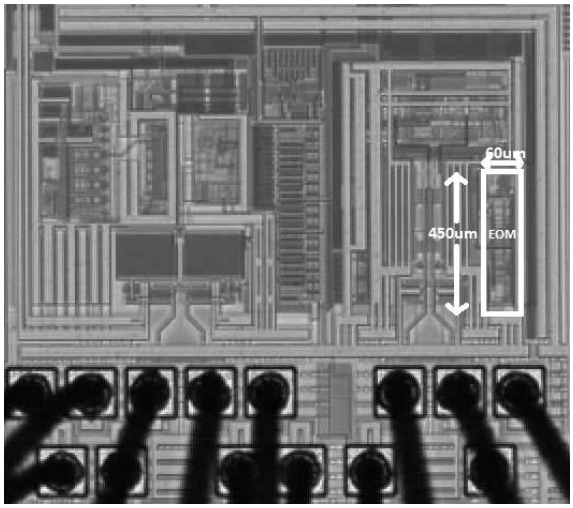

Figure 4-19 Test chip die photograph.

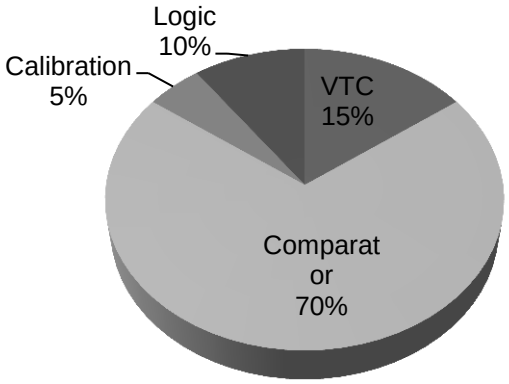

Figure 4-20 Power consumption breakdown.

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The measurement setup is shown in Figure 4-21. In order to compare the real eye diagram and the proposed EOM, a test buffer circuit was built into the test chip to drive the off-chip equalizer output signal as well. Therefore, the real eye diagram was obtained using an oscilloscope. To verify this chip, a BER test system was used to generate a SuperSpeed USB 10 Gbps compliance test pattern, where the test channel was a 14-cm USB 3.1 Generation 2 cable plus a short printed circuit board trace. The receiver equalizer was adapted to an optimized gain setting. After that, the amount of random jitter in the BER test system input was adjusted and the EOM results were simultaneously monitored by logic analyzer.

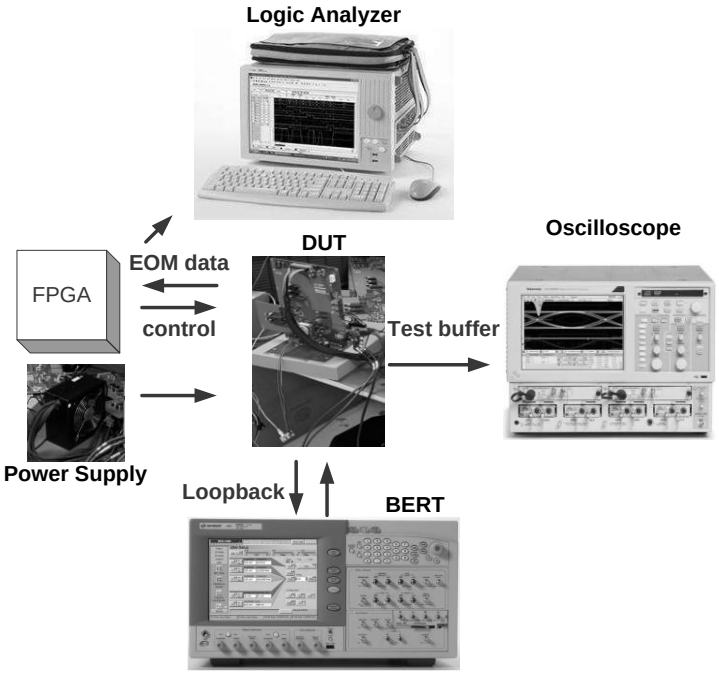

Figure 4-21 Measurement setup.

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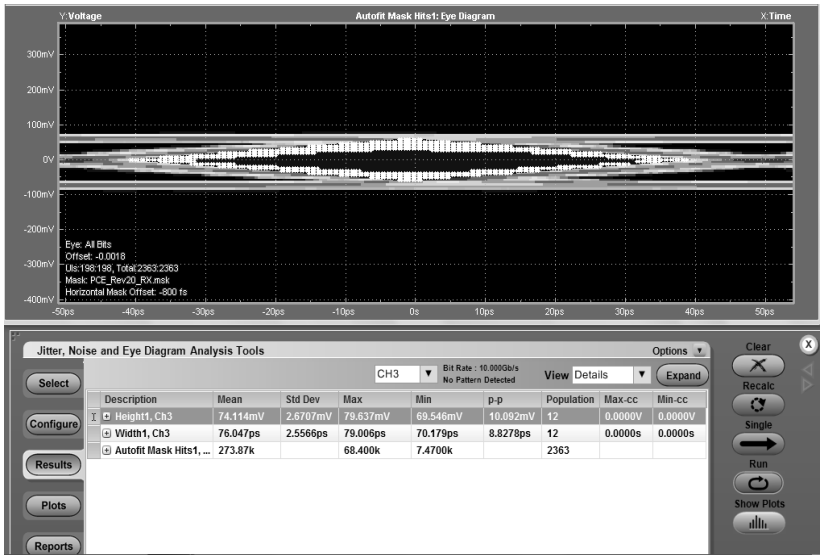
The measurement results are shown in Figure 4-22 (a) (b), Figure 4-23, and Figure 4-24 (a) (b) (c). The test condition is that the input has no random jitter. Figure 4-22(a) shows the test buffer eye diagram. The eye height is 140 mVpp and the eye width is 76 ps. Figure 4-22 (b) shows the six-bit 1D-EOM output and a finish indicator. The results are output by a logic analyzer. In this case, the 1D-HEOM six-bit output was 110101 (decimal value of 53), and the maximum value was 64. Figure 4-23 shows the HEOM results (decimal representation) against the input with different amounts of random jitter. Figure 4-24(a) (b) (c) shows the eye diagram before and after receiver equalization. The EOM result is also demonstrated in the top-left corner of every eye diagram during equalizer adaptations. Table 4.2 provides a performance comparison of prior EOMs.



(a)

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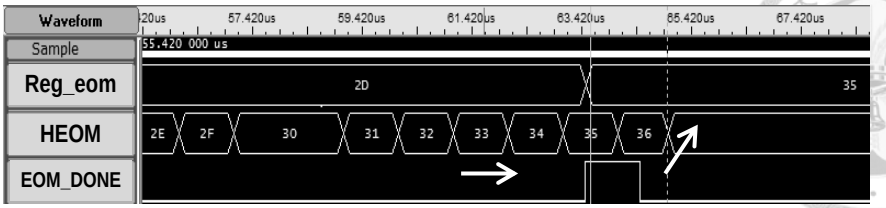

(b)

Figure 4-22 (a) Test buffer output eye diagram. (b) 1D-EOM output results.

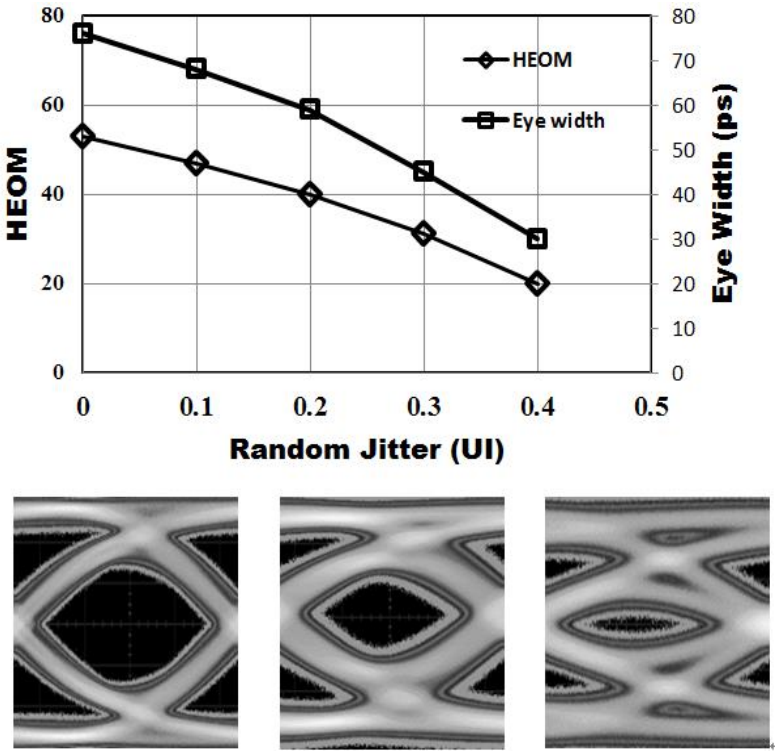

Figure 4-23 HEOM results VS. Input with Different Random Jitter (RJ).

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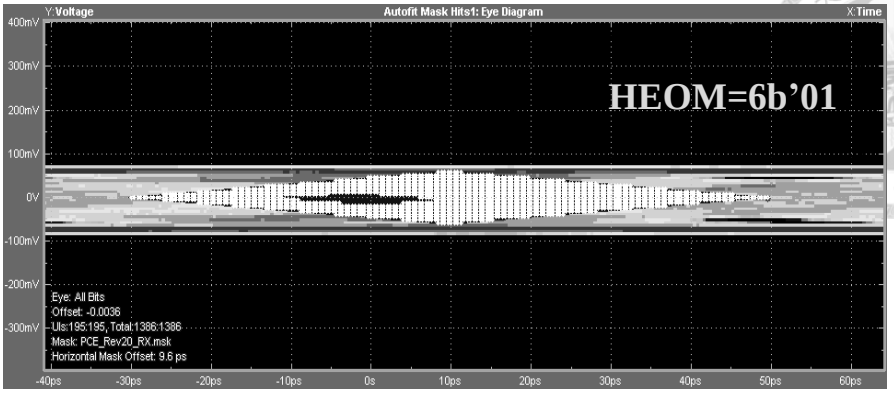
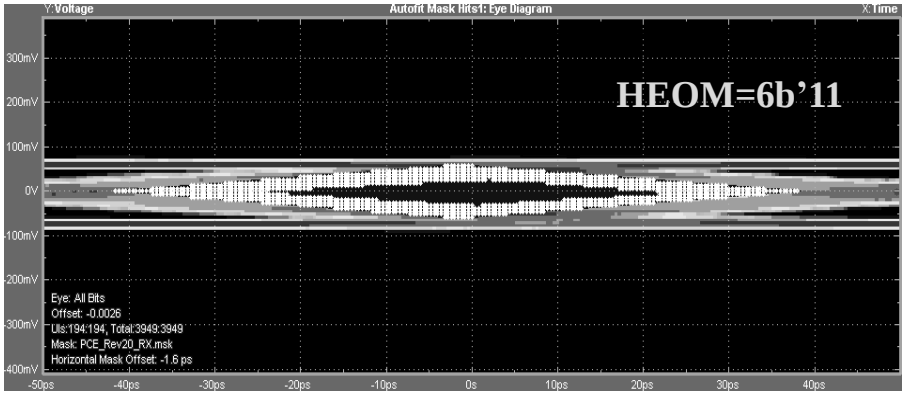
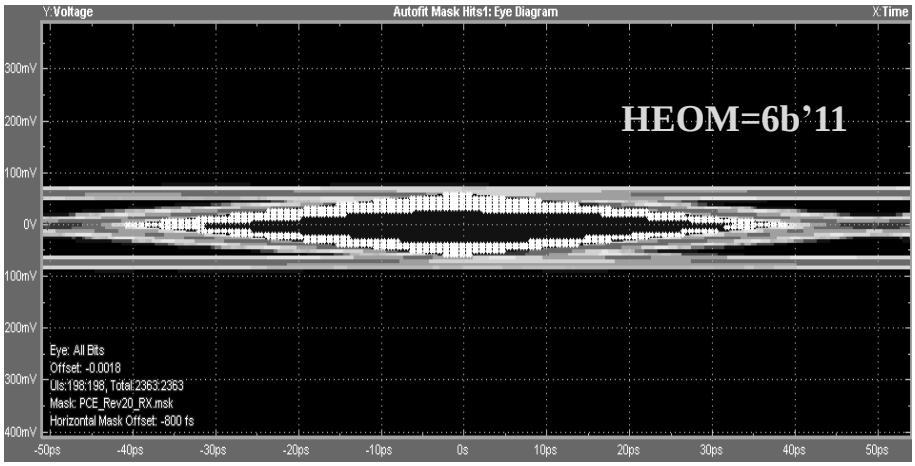


(a)



(b)



(c)

Figure 4-24 Eye diagram VS. HEOM results during equalizer adaptations. (a) Before equalization. (b) During equalization. (c) After equalization.

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Table 4.2 Performance comparisons of EOMs.

Reference	Technology	Type	Power (W)	Area (mm^2)	Speed (Gb/s)
Ellermeyer[44]	SiGe bipolar	1-DH	4.95	6	10
Kim[46]	0.18μm CMOS	1-DV	0.054	NA	1.25
Analui[47]	0.13μm CMOS	2-D	0.33	0.264	12.5
Noguchi[48]	0.18μm BiCMOS	2-D	0.72	0.5	38-42
Gerfers[49]	0.18μm CMOS	Edge	0.11	NA	2
This work[66]	65 nm CMOS	1-DH	0.0015	0.027	10

4.6 Conclusions

A low-cost, on-chip eye-opening monitor (EOM) circuit was presented in this chapter. In order to precisely measure the eye-opening, the whole eye diagram must be reconstructed instead of choosing some eye masks to fit the eye diagram. However, this results in long computational times to calculate the probability density functions for all pixels and cannot easily be applied for real-time equalizer adaptations. With a trade-off between speed and accuracy, a one-dimensional EOM structure was proposed to monitor the horizontal eye-opening in the eye diagram. Since the proposed EOM does not employ a bit-by-bit data processing structure, sampling data with different phases in parallel is not necessary. Power consumption can be greatly reduced, and all complicated phase interpolation circuits can be replaced with the proposed phase

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generator circuit. The mismatch problem that exists in the traditional phase interpolation circuits can be mitigated.

The EOM circuit was implemented and verified in a SuperSpeed USB 10 Gbps receiver prototype integrated chip using 64-nm CMOS technology. The measurement results demonstrated that the value reported by the horizontal EOM was closely correlated with the real eye width, which is helpful for equalizer adaptation. The total power consumption was 1.5 mW for a 1 V supply, which is much smaller than the traditional bit-by-bit data processing EOM.

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Chapter 5
Conclusion

5.1 Summary

In this dissertation, several time-domain processing circuits as well as the design and analysis of these circuits are presented. In chapter 2, a brief overview of two critical time mode circuits, VTC and TA are introduced. Some state-of-the-art designs are also presented in this chapter. Next, in chapter 3, a high-speed time-based ADC (TADC) is proposed and demonstrated in 0.18-μm CMOS technology. In this chapter, a novel VTC circuit is proposed. A load tuning circuit in the proposed VTC provides an adequate control voltage to a symmetric-type delay cell for the improvement of linearity. The post-layout simulation result shows that the proposed VTC circuit can provide 7 to 8 bits of accuracy for the TDCs and the sampling frequency of the following TDCs can be up to 500 MHz. The measurement results of TADC are also presented at the end of this chapter.

Finally, a time-domain design example is proposed in chapter 5. In this

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chapter, a multi-phase clock generator based on the VTC is proposed in the one-dimensional eye monitor (1D-EOM) circuit. It provides a sampling clock with an accurate phase difference for the EOM circuit. The proposed 1D-EOM circuit is implemented in 65-nm CMOS technology and the measurement results demonstrate that the value reported by the 1D-EOM can be used as a feedback parameter for equalizer adaptations. It occupies a small layout area and consumes less power than the conventional eye monitor circuit.

5.2 Future Works

The proposed time processing circuit specifications can be further improved to fit more accurate mixed-mode circuit design requirements. They are discussed as follows:

For the VTC circuit proposed in chapter 3, suggested to add an offset cancellation circuit in load-tuning circuit to improve the input dynamic range. Moreover, the mismatch of dual-delay lines also need to be taken into account if more accurate VTC design is needed. In addition to the mismatch effect, temperature variation also affect the transfer characteristic of VTC. Added an offset current that is proportional to the temperature variation in VREF generator circuit is good for temperature compensation. At last, the comparator unit of the flash TDC also needs to be calibrated to ensure a

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more accurate time delay between two RC-inverter paths of the comparator unit.

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