國立臺灣大學電機資訊學院電信工程學研究所

博士論文

Graduate Institute of Communication Engineering
College of Electrical Engineering and Computer Science
National Taiwan University

Doctoral Dissertation

微型化近橫向電磁合成傳輸線 CMOS 主動濾波器設計

Design of Miniaturized Synthetic Quasi-TEM Transmission-Line-Based CMOS Active Filter

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中華民國 100 年 12 月 23 日

December, 23, 2011

國立臺灣大學博士學位論文
口試委員會審定書

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本論文係李孟霖君（學號 D94942008）在國立臺灣大學電信工程所完成之碩（博）士學位論文，於民國一百年十二月二十三日承下列考試委員審查通過及口試及格，特此證明

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致謝

在台大電信所攻讀博士學位這些年來，關關難過，關關都要過。一路走來除了本身努力外還需許多貴人的提攜與幫助才能通過關關的考驗，完成這本博士論文。承蒙指導教授**莊晴光**博士之殷切指導，尤以恩師於課業上之悉心解惑，生活上及研究態度上之諄諄教誨，使學生受益匪淺，浩瀚師恩，永記在心，僅誌於此，表達由衷之敬意與感謝。另外也謝謝肝膽相照的師兄，吳憲順博士在我低潮時給予鼓勵並與我並肩作戰突破層層的試煉，在此也懷念一起小酌的時光。感謝口試委員許博文教授、黃天偉教授、張志揚教授、林育德教授、郭仁財教授、傅坤福教授、田慶誠教授與陳毓喬博士對論文不吝賜正並提出更多見解與看法，使論文更完整。另外感謝當年在準備博士班入學考時，黃正亮教授、蔡智明教授與魏炯權教授幫我寫推薦函使得能進入台大電信所做研究。

在剛進入台大時謝謝當年在電二館 525 室的明達、明峰、晉申，作敏、佩憙與子軒學長們幫助使我快速地融入所上的生活。其它學長明佑、政翰、世峰、卜華、志榮、安錫、瑞伯、松年、漢璋、士元、坤佑與琦學謝謝你們在生活上與計畫合作裡的協助。懷念與宗樺、宗男、兆祥、宜峰、哲均同學們及哲嘉、佑傑、婉婷、老盧、昱緯學弟妹們一起度過歡樂的時光。感謝坤堯與景富學弟在我最緊急時讓出無塵室讓我使用。還有偉強學弟在我超低落時陪我聊天並鼓勵，我也很佩服您不屈不撓的精神。同門的繼禾、憲宏、瑞琦與孟儒師兄們謝謝你們在研究上給予寶貴的意見使得研究得以順利進行與在緊急時給予協助。同門師弟妹們：王紳、思賢、啟洋、致嘉、昆宏、柏榮、昱瑞、育修、廷縉、釗偉、光甫、偉成、星瀚、奕鈞、彥翔、佩均、蘇黎、凱安、凱翔、瑜芝、俊慶、揚智、龍雨與衍嘉也謝謝你們的協助及留下一起討論研究與作業、做實驗、把酒言歡、一起下線拼到天亮、桃園 WICE 閉關修行、河堤與瑞穗單車行、九份金山行等美好的回憶。謝謝歷任助理郁萍與貞黛處理與張羅實驗室大小庶務使得我能專心於研究上。所

上的趙姐與季先生也謝謝你們熱心的幫忙。還有一些業界的前輩先進們謝謝你們提供業界實務的看法使得我的研究更完整。岳樺、識賢與慶文，瑩達與源峰學長，從在成大跟我一起奮戰到台大的士弘謝謝你們這些年的加油打氣。最後感謝我的家人在我念博班這段期間全力的支持讓我經濟上無後顧之憂，全力完成研究與論文著作，拿到博士學位。

多貴人相助才能突破關關的考驗，今後希望我也能成為他人的貴人幫助其達到理想。求學過程的結束是人生新階段的開始，今後需更努力地克服更險峻的挑戰與貢獻社會來報答貴人的幫助與家人之栽培，不辜負社會對博士的期盼。

摘要

本論文係討論高微型化三階主動微波帶通(bandpass)濾波器之設計，其實現於標準 0.18-μm 互補式金屬氧化物半導體(CMOS)1P6M 製程在 480 μm 厚的矽基板上，中心頻率在 1.58 GHz 且面積為 0.58% λ_0 × 0.44% λ_0，λ_0 是中心頻率在真空中的波長。在論文中，針對微型化程度與電氣特性來評價目前文獻所發表以半導體技術實現之射頻帶通濾波器，其結果以一圖來表示，由該圖顯示本文所提的 CMOS 主動濾波器為當今微型化程度最高的單晶主動濾波器，且其微型化程度趨近目前商用的 FBAR 帶通濾波器。本文提出新型合成傳輸線，該傳輸線不但承襲互補式金屬傳輸線(complementary-conducting-strip transmission line, CCS TL)具靈活合成導波特性，更進一步的能減少傳輸線所佔的面積而不會增加傳輸損耗。如此的傳輸線使得本文的 CMOS 主動帶通濾波器達到高微型化。此外，改良的 nMOS 交錯偶合對(cross-coupled pair)產生隨頻率變化的負電阻來補償傳輸線共振器裡隨頻率變化的損耗以增加共振器品質因子(quality factor)。如此，CMOS 主動帶通濾波器不但能獲得足夠的補償以降低插入損耗(insertion loss)，且能維持通帶(passband)平坦度並提升穩定度。基於上述技術，設計一階數皆為三以合成傳輸線為基礎具低通帶變形的 CMOS 主動帶通濾波器，所佔面積為 1099.47 μm × 837.48 μm 或為 0.58 % λ_0 × 0.44 % λ_0。在 1.8 V 電源供應下消耗 8 mA 的電流，1.58 GHz 中心頻率的插入損耗為 0.68 dB。通帶頻寬為 8% 且回流損失(Return Loss)大於 16 dB。通帶漣波(passband ripple)為 1.24 dB。

另外，針對已封裝 1.53-GHz CMOS 含晶片裡(on-chip) ESD 保護電路的主動帶通濾波器由晶片設計到封裝完整的討論寬上截止帶抑制(wide upper stopband suppression) 設計。在現存的文獻中這是第一次針對單晶射頻主動濾波器討論通帶外的訊號抑制。複合式並聯共振器(composite parallel resonator)裡的退化式 nMOS 交錯偶合對(degenerate nMOS cross-coupled pair)不但對共振頻率的訊號補償，也對

奇諧波假象(spurious)訊號補償。在此藉由電容負載式傳輸線共振器的方式來控制假象(spurious)訊號產生位置，使得單晶 CMOS 主動帶通濾波器具寬上截止帶抑制。而該 CMOS 主動帶通濾波器的晶片以 chip-on-board (COB) 方式來封裝，封裝後全部的面積為 3.71 mm × 2.50 mm。由等效集總(lumped)電路分析，封裝裡的接地磅線所伴隨而來的寄生電感將對通帶外訊號抑制造成影響，而此寄生效應會在封裝設計中降低。另外，磅線長度變異對於上截止帶訊號抑制的影響亦在本論文裡討論。此封裝後 CMOS 主動帶通濾波器在 3V 的電源供應下消耗 8 mA 的電流，中心頻率(f_0) 1.53 GHz 的插入損耗為 0.95 dB 而通帶頻寬為 3.1%。通帶外，在 $2f_0$ 與 $3f_0$ 的頻率響應抑制各為 44.57 dB 與 52.78 dB，而截止帶的抑制由 $1.09f_0$ 到 $10.05f_0$ 超過 35 dB。 ESD 保護能力量測顯示該單晶主動濾波器的 RF 埠在人體放電模式(Human-Body Model, HBM)下具有 500 V 的靜電保護能力。最後在-40℃到+80℃升溫測試中，該封裝後 CMOS 主動帶通濾波器的中心頻率漂移由 1.587 GHz 到 1.479 GHz 而飄移率為-0.9 MHz/℃。

Abstract

This dissertation presents a design of high miniaturized third-order transmission-line-based (TL-based) active bandpass filter (BPF), which is fabricated using standard 0.18-μm complementary metal-oxide-semiconductor (CMOS) one-poly six-metal (1P6M) technology on a silicon substrate with a thickness of 480 μm and designed at the central frequency of 1.58 GHz in a chip area of 0.58% λ_0 × 0.44% λ_0, λ_0 is the free-space wavelength at the central frequency. In this dissertation, the RF BPFs, which are fabricated in semiconductor technologies and presented in the published literature, are assessed against the degree of miniaturization and acceptability of performance. The statistics are summarized in a figure, which reveals that the CMOS TL-based active BPF herein has the lowest normalized area per resonator of active BPFs and the degree of miniaturization approaches the one of commercial FBAR devices. The new synthetic transmission line proposed in this dissertation has the widely flexibilities on the syntheses of guiding characteristics, like complementary-conducting-strip transmission line (CCS TL), and can further reduce the occupied chip area without compromising the transmission loss. Thus, such a synthetic transmission line enables the CMOS TL-based active BPF herein to be substantially miniaturized. Moreover, the frequency dependent negative conductance, which is produced from a modified nMOS cross-coupled pair,

compensates for the frequency dependent loss in the TL-based resonator to enhance the quality factor (Q factor) of a composite parallel resonator. Therefore, the CMOS TL-based active BPF acquires adequate loss compensation to reduce the insertion loss with good passband flatness and the stability is also improved. Based on the techniques mentioned above, an CMOS third-order TL-based active BPF with low passband disturbance is designed in a chip area of 1099.47 μm × 837.48 μm or 0.58% λ_0 × 0.44% λ_0. The prototype consumes a current of 8.0 mA from 1.8 V and has 0.68-dB insertion loss at the central frequency of 1.58 GHz. The 3dB bandwidth is 8% with the return losses more than 16 dB. The passband ripple is 1.24 dB.

Additionally, the comprehensive design of wide upper stopband suppression for a packaged 1.53 GHz CMOS active bandpass BPF with on-chip electrostatic discharge (ESD) protection circuits is developed from the chip level to the package in the second part of this dissertation. So far, this is the first time that outband spurious responses are discussed and presented in the design of RF monolithic active BPF. In a composite parallel resonator, not only the signal at fundamental frequency but also the spurious ones at odd-harmonic frequencies are enhanced by the degenerate nMOS cross-coupled pair. The spurious responses are controlled and shifted towards higher frequencies by using the capacitively loaded TL resonator method in the COMS active BPF design to achieve wide upper stopband suppression. The fabricated chip of the aforesaid CMOS

active BPF is packaged using the chip-on-board (COB) process in an area of 3.71 mm × 2.50 mm. In the lumped equivalent circuit analysis, the ground bondwires, which accompany the parasitic inductor at ground, in COB package influence the stopband suppression of the packaged CMOS active BPF and this parasitic effect is minimized in the package design. In addition, the influences of the variation in length per bondwire on the stopband suppression are also demonstrated. Measurement results indicate that the packaged CMOS active BPF has 0.95-dB insertion loss at a central frequency (f_0) of 1.53 GHz with a 3dB bandwidth of 3.1%, while a current of 8 mA is consumed from 3.0 V. The stopband suppressions at $2f_0$ and $3f_0$ are 44.57 dB and 52.78 dB, respectively. Furthermore, the suppression exceeds 35 dB from $1.09f_0$ to $10.05f_0$. The ESD tests demonstrate that the two RF ports of the prototype have the Human-Body Model (HBM) ESD protection level of 500 V. Finally, in the temperature variation measurement, the central frequency of the prototype shifts from 1.587 to 1.479 GHz with a shift rate of -0.9 MHz/℃ from -40℃ to +80℃.

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Chapter 1
Introduction

This chapter focuses on the introduction, including the research motivation, literature survey and statistics. Ultimately, the contributions and organization of this dissertation are addressed in this chapter.

1.1 Motivation

In radio frequency (RF) field, bandpass filters (BPFs) perform band selection and interference rejection. Thus, the acceptable performance for BPFs includes a low insertion loss, a high out-band rejection, a narrow passband and equal ripples, as shown in Fig. 1.1 to ensure good RF band selectivity and rejection of potential interference in the RF transceiver. Thus, to achieve the demand in Fig. 1.1, a high quality factor (Q factor) resonator for a BPF is necessary. Modern wireless communication is becoming lower-cost and increasingly using compact RF transceivers. Moreover, the demand of multi-band and multi-standard functionalities in small portable apparatuses is more and more rigorous. Under this trend, the miniaturization of the BPF to the highest degree facilitates compact and low-cost RF transceivers. However, during the process of miniaturizing BPFs, the increasing loss is inevitably compromised. Thus, the

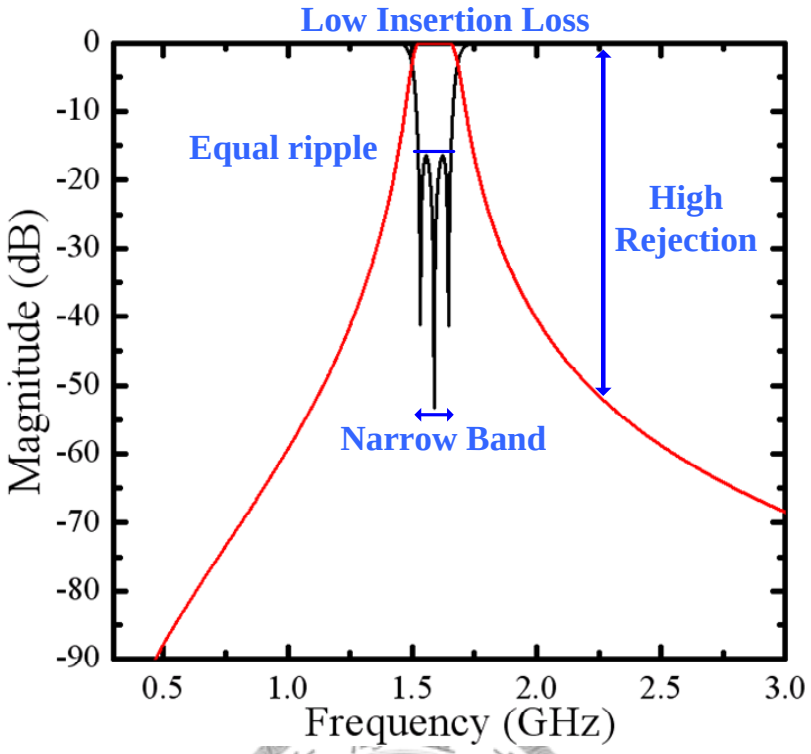


Fig. 1.1 Acceptable performance that a bandpass filter possesses

miniaturization of BPFs, while maintaining acceptable performance, is one of the most important challenges. Nowadays, the amplifiers, mixers, oscillators and digital logic circuits can be implemented and integrated using standard monolithic semiconductor technologies. Nevertheless, the off-chip BPFs are still required to construct a completed RF transceiver as shown in Fig. 1.2 (a). If the BPF is designed and fabricated using standard semiconductor technologies, potentially, the objective of system-on-chip (SoC) can be realized, as shown in Fig. 1.2 (b). The advantage of on-chip BPFs integrated in monolithic RF transceiver is as follows. Firstly, the size of the completed transceiver module can be substantially reduced. Secondly, decreasing the dependence of the off-chip BPF, the complexity of the transceiver module and the manufacture cost can be

reduced. However, for the compact on-chip BPF with good RF band selectivity, the active compensating mechanism is essential to enhance the *Q* factor of the resonator and then, the on-chip active BPF is proposed.

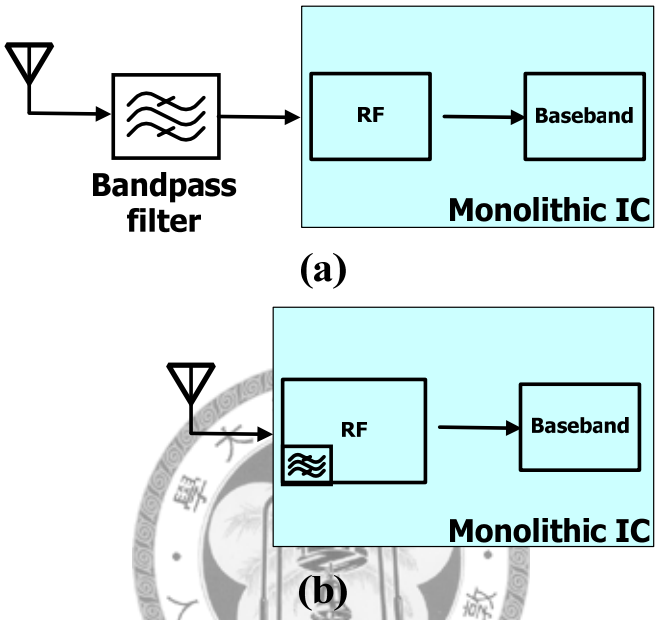


Fig. 1.2 (a) Monolithic receiver with off-chip BPF. (b) Monolithic receiver with on-chip active BPF.

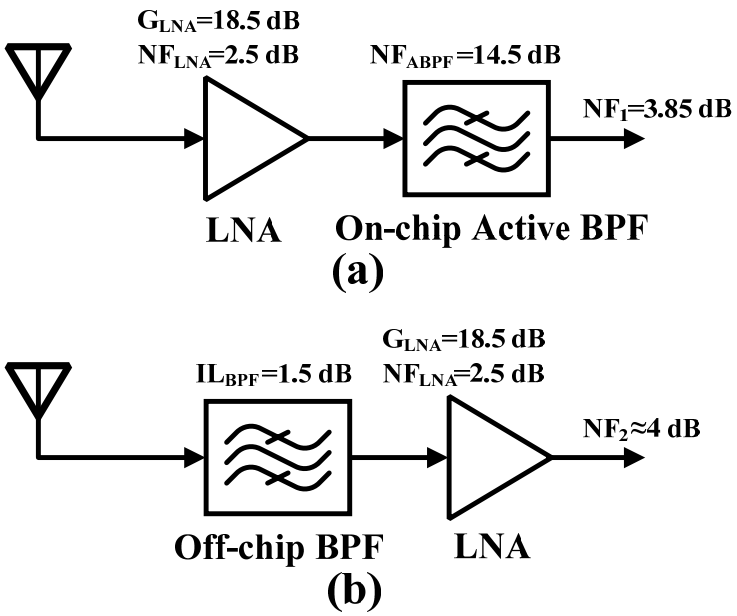


Fig. 1.3 Noise figure estimation (a) On-chip active BPF follows LNA. (b) LNA follows Off-chip BPF.

As the insertion loss of the on-chip active BPF is reduced, the noise figure is simultaneously generated from the transistors and proportional to the consumed current. The advanced and low-noise semiconductor process could facilitate the reduction of noise figure. Although the increasing noise figure is inevitable for the on-chip active BPF, a customized low noise amplifier (LNA) with good linearity can be placed in front of the on-chip active BPF, as shown in Fig. 1.3 (a), to suppress the inevitable noise figure. An example is described as follows. In practice, the LNA in CMOS process for global positioning system (GPS) application has about the gain, G_{LNA}, of 18.5 dB and noise figure, NF_{LNA}, of 2.5 dB. In Fig. 1.3 (a), the on-chip active BPF, which has the noise figure, NF_{ABPF}, of 14.5 dB, follows the LNA and the overall noise figure can be reduced to about 3.85 dB. For the typical architecture in Fig. 1.3 (b), the off-chip BPF, which has the insertion loss, IL_{BPF}, about 1.5 dB, is placed in front of the LNA. In other words, the off-chip BPF contributes the noise figure about 1.5 dB. Thus, the overall noise figure of the typical architecture in Fig. 1.3 (b) will be about 4 dB and almost equal to the one, calculated from the architecture that the on-chip active BPF follows the LNA in Fig. 1.3 (a). Otherwise, the received signal from the satellites is typically -130 dBm and can be amplified to about -108 dBm through the antenna and LNA. If the input third-order intermodulation intercept point (IIP_3) and input 1-dB compression point (P_{1dB}) of the on-chip active BPF are about -10 to -5 dBm and -20 to -15 dBm,

respectively, the signal couldn't be blocked. The above-mentioned reveals the potential of the on-chip active BPF in practical application.

1.2 Literature Survey and Statistics

Semiconductor technologies are used to fabricate highly miniaturized BPFs, such as integrated passive device (IPD) filter [1]. These BPFs must have a low insertion loss, a high out-band rejection, and a narrow passband, to ensure good RF band selectivity and rejection of potential interference in the RF transceiver. In this dissertation, two parameters are proposed herein to assess the miniaturization and acceptability of performance of the BPFs. The first factor is the normalized area per resonator (APR), and is expressed as,

$$\mathrm{APR} = \frac{A}{N \cdot (\lambda_0)^2} \times 100\ \% \tag{1.1}$$

where A and λ_0 are the physical area of the BPF and the free-space wavelength at the central frequency, respectively. N in (1.1) denotes the number of the resonators in the BPF. APR in (1.1) measures the miniaturization of the resonator, as required for use in a BPF. For example, an APR of 10^{-2} % indicates that one resonator can be realized in an area of 1.0% λ_0 by 1.0% λ_0. The second factor is the normalized 3dB bandwidth over the magnitude of the transmission coefficient (BOT), and is expressed as

$$\mathrm{BOT} = \frac{3\mathrm{dB\,Bandwidth}}{f_0 \cdot |S_{21}|} = \frac{\mathrm{Fractional\,Bandwidth}}{|S_{21}|} \qquad (1.2),$$

where f_0 is the central frequency of the passband for the BPF and $|S_{21}|$ is the magnitude of the transmission coefficient at the central frequency of the BPF. The BOT defined in (1.2) indicates RF band selectivity, combined with the inherent quality factor of the resonator. Typically a BPF that is constructed from a resonator of high quality factor (Q factor) can achieve an $|S_{21}|$ that approaches one with a narrow 3dB bandwidth and, therefore, a low BOT value, yielding acceptable performance of the BPF. Fig. 1.4, which includes the prototypes covering frequencies from 1.58 GHz to 65 GHz, plots the APR against BOT for monolithic BPFs that are constructed from at least two resonators. The statistics in Fig. 1.4 refer to BPFs that are in the small-signal operation and based on silicon-based IPD technologies [1], standard CMOS in this work and [2]-[11], GaAs pHEMT [12], GaAs HBT [13], GaAs MESFET [14], GaAs HJFET [15], micro-electro-mechanical systems (MEMS) [16] and thin-film bulk acoustic-wave resonator (FBAR) [17], [18]. For example, the FBAR filter [18], which comprises seven resonators, has an insertion loss of 1.8 dB, a 3dB bandwidth of 60 MHz, and a central frequency of 1.96 GHz, occupying an area of 0.56 mm^2. Based on (1.1) and (1.2), the APR is 3.42×10^{-4} % and BOT is 0.037, as shown in Fig. 1.4. These prototypes show the demand on filter design with the lowest APR and BOT for the high circuit

miniaturization and frequency selectivity.

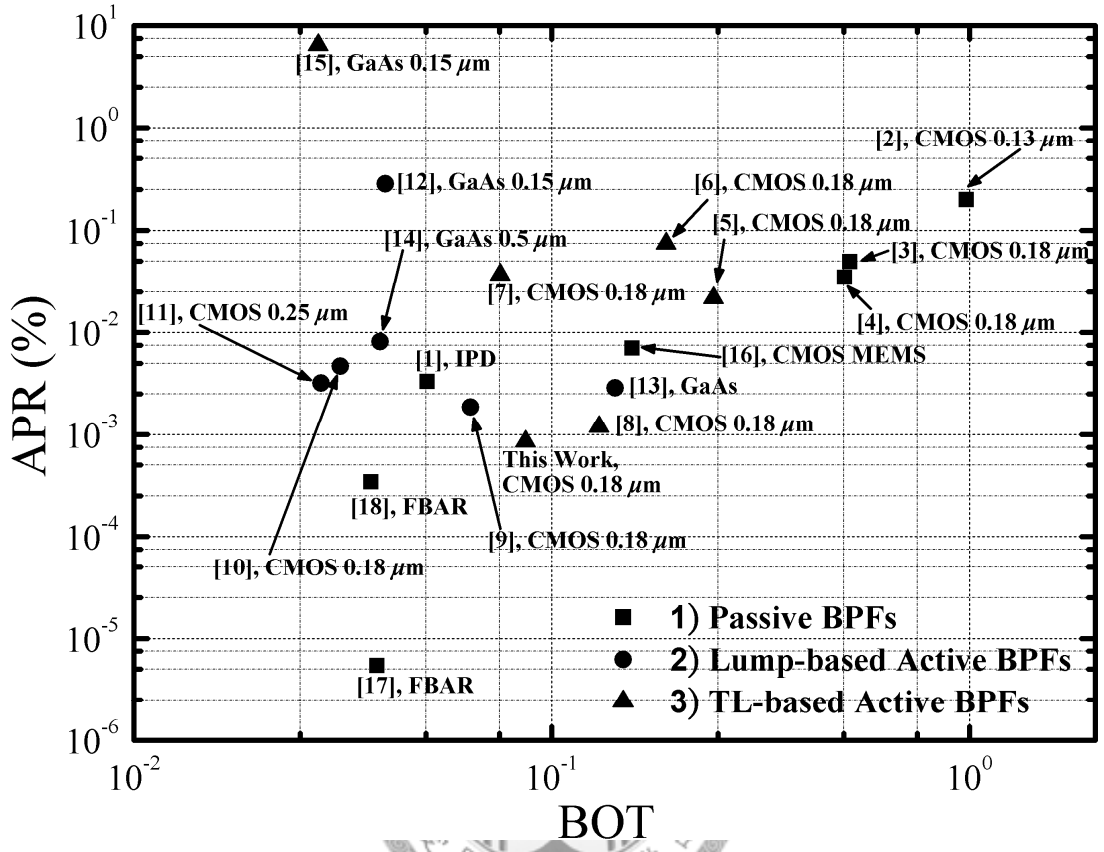


Fig. 1.4 APR(normalized area per resonator) against BOT(normalized 3dB bandwidth over the magnitude of the transmission coefficient) for BPFs fabricated using semiconductor technologies.

The statistics in Fig. 1.4 identify three categories:

1) The passive BPFs, constructed with monolithic transmission lines [2]-[4] and, lumped elements [1], [16]-[18] are represented by square symbols in Fig. 1.4. Since the *Q* factor of a typical monolithic transmission line is proportional to the square root of the frequency, the increasing *Q* factor of the resonator based on the monolithic transmission lines offers great opportunity to design on-chip passive bandpass filter, such as [2], and be directly integrated in the monolithic transceiver. However, the *Q*

factor of the passive transmission-line based resonator is still inadequate even at millimeter wave band and the insertion loss at the central frequency is significant, as shown in [2, Fig. 12]. Thus, Fig. 1.4 displays the passive BPFs, implemented in standard CMOS technology [2]-[4], which have a typical BOT of higher than 0.25. This result implies that the typical CMOS or GaAs processes severely limit the design of high-Q and narrowband monolithic filters strictly in the passive form. Additionally, to reduce the loss of the lumped elements implemented in the semiconductor technologies, the passive BPFs are designed and implemented respectively in IPD technology [1] based on the special semiconductor process and micromachining technology [16] based on MEMS. Thus, the insertion loss and chip area of the passive BPFs, implemented in non-typical CMOS process, can be simultaneously reduced. Different from the electromagnetic wave resonating in the resonator, the FBAR technology uses the bulk acoustic wave resonating in the resonator. The advantage of this technology lies in low propagation loss that acoustic wave suffers from in acoustic materials at low frequency and the acoustic wavelength which is three to four orders of magnitude less than the electromagnetic one. Therefore, the semiconductor-based FBAR passive filter [17], [18] has the lowest APR (5.43×10^{-6} % [17] and 3.42×10^{-4} % [18]) with a relatively low value of BOT (0.038 [17] and 0.037 [18], respectively), demonstrating the best tradeoff between BPF miniaturization and performances.

2) The BPF designs with lumped elements and transistors to reduce loss are lump-based active BPFs, and represented by dots [9]-[14] in Fig. 1.4. In order to compensate for the loss of the lumped elements, such as inductors, several techniques has been demonstrated to reduce the loss of BPFs, including transformer-based *Q*-enhancement method [10] [11] and compensation with the negative conductance connected to the lossy resonator tanks [9] [12]. The active BPFs have lower BOT (0.028 [11], which has an insertion loss of 0 dB, a 3dB bandwidth of 60 MHz, and a central frequency of 2.14 GHz) and exhibit *Q* enhancement by the active circuit compensation for the losses that occur in the passive devices. Additionally, ascribed to the greater part of the chip area occupied by the inductors, the inductorless active BPFs [13] [14] are proposed and demonstrate the miniaturization. The active circuits, such as gyrator or g_m-C cells, are designed to synthesize the required inductance by impedance transformation. Nevertheless, the inductance realized by these circuits is proportional to a capacitance and inversely proportional to the square of a transconductance and this means more current consumed will be paid for small inductance. In the other words, the inductorless active BPF is inappropriately designed at high frequency. Although the active filters can achieve lower BOT than the passive ones, the passband noise figure of the active prototypes, which is not easily observed in the Fig. 1.4, is relatively higher than that of the passive prototypes. The active devices, however, produce the extra noise

power to affect the signal to noise ratio in the passband.

3) The BPFs, in which the resonators consist of transmission lines (TLs) and transistors to compensate for loss, are regarded as TL-based active BPFs, and represented by triangular symbols [5]-[8], [15] and this work. The monolithic transmission-line-based active BPF [15] is designed at a central frequency of 65 GHz, occupying an area of 2.57 mm^2 and the APR is 6.45 %. In general, the lumped elements are usually adopted to design compact monolithic integrated circuit, such as above-mentioned lump-based active BPFs [9]-[14]. Thus, the APR of [9]-[14] ranges from 1.85×10^{-3} % [9] to 0.28 % [12] and is far smaller than [15]. While the synthetic transmission line, complementary-conducting-strip transmission line (CCS-TL) is proposed [19], the TL-based active BPF [5], designed based on CCS-TLs, is substantially miniaturized with the APR of 2.1×10^{-2} % in Fig 1.4. Then, the following [6] and [7] are respectively designed at Ka and K band. For further miniaturization, TL-based active BPFs in this work and [8] adopt the new synthetic transmission line and have lower APR values than lump-based active BPFs [9]-[14]. The most interesting finding from Fig. 1.4 is that both the lump-based active BPF (dots) and the TL-based active BPF (triangles) converge to the FBAR filter [18].

Stopband suppression is required for BPF designs. Related techniques, such as the stepped-impedance resonator (SIR) in [20] and multiple-mode resonator (MMR) in [21],

have been extensively realized in planar-printed-circuit-board (PCB) technologies. In semiconductor technologies, the active BPFs [5]-[15] in Fig. 1.4 merely focus on the loss compensation within a narrow passband, but the behavior of out-band responses are rarely mentioned. In addition to in-band loss compensation, the minimization of passband disturbance and prototype miniaturization, wide stopband with high spurious suppression is also important to prevent the out-band intermodulation product from falling within the passband of the active BPF, especially at a congested spectrum below 6 GHz. Take the prototype of 1.58 GHz CMOS active BFP with 8% 3dB bandwidth herein as an example, two tone signals at 875 MHz and 2.45 GHz are sent to this prototype, which causes the out-band second-order intermodulation product to appear at 1.575 GHz within the passband. The active compensating mechanism, which enhances out-band spurious responses, and the package, which accompanies parasitic effects, can influence the out-band response of the monolithic active BPFs. Appropriate modification for the active resonator can control the enhanced spurious responses and enable the active BPFs to have wide stopband suppression. The GaAs process provides ground via holes, which facilitate monolithic BPFs to be grounded in the package, and thus the ground parasitic inductance can be minimized. However, owing to the lack of ground via holes in standard CMOS technology, as the CMOS active BPFs are packaged, the effect of ground parasitic inductance needs to be characterized and

minimized by appropriate package design to achieve the desired stopband suppression.

1.3 List of Contributions

The contributions arising from this dissertation are as follows:

- The present semiconductor-technology based RF BPFs in published literature are assessed against the miniaturization and acceptability of performance. The statistics reveal the tendency of miniaturization.
- The new synthetic transmission line, which can simultaneously improve miniaturization without compromising transmission loss, is demonstrated.
- The loss compensation methodology, which can minimize the passband disturbance and stabilize the active BPF, is presented.
- The third-order TL-based active BPF herein is fabricated using CMOS 0.18-μm 1P6M technology and the measurement results confirm good passband flatness. The statistics show that the miniaturization of such a prototype is the best of present active BPFs and approaches the commercial FBAR device.
- This is the first time that the spurious response control is discussed and presented in the design of RF monolithic active BPF.
- For the packaged CMOS TL-based active BPF, the inductive parasitic effect, introduced from the package, is investigated and reduced to minimize the impact

on the stopband suppression.

1.4 Organization of This Dissertation

There are six chapters in this dissertation, and the rest is organized as follows:

Chapter 2 presents the guiding characteristics of the new synthetic transmission line. The conventional complementary-conducting-strip transmission line (CCS TL) and its design guideline is briefly reviewed. The design limit of the conventional CCS TL is discussed and broken through by the proposed new C-CCS TL. By comparing the guiding characteristics, which are extracted from the physical structures of conventional CCS TL and C-CCS TLs with fixed length, the C-CCS TL in whorl form can simultaneously improve miniaturization and reduce transmission loss.

Chapter 3 and Appendix present the design of active bandpass filter with low passband disturbance. Firstly, the adopted architecture of active BPF herein and the single-ended active compensating mechanism based on the nMOS cross-coupled pair are reviewed. However, the passband disturbance results from the frequency-dependent loss, canceled by the constant negative conductance. According to the design equation, which is presented to minimize the passband disturbance, a modified nMOS cross-coupled pair with the degenerate load is designed to produce the frequency-dependent negative conductance. From the circuit simulation for a physical composite parallel

resonator, composed of a TL-based resonator and a modified nMOS cross-coupled pair, the input conductance and its derivative both approach zero within a certain bandwidth and reveal that, in addition to loss compensation, the proposed modified nMOS cross-coupled pair can minimize the passband disturbance and stabilize the active BPF.

Chapter 4 demonstrates the implementation of the CMOS TL-based active BPF, based on the miniaturization technology in Chapter 2 and loss compensation methodology in Chapter 3, and the on-wafer measurement results. The prototype is design at the central frequency (f_0) of 1.58 GHz with 8% 3dB bandwidth and fabricated using standard 0.18-μm CMOS 1P6M technology on a silicon substrate with a thickness of 480-μm in a chip area of 0.58% λ_0 × 0.44% λ_0, λ_0 is the free-space wavelength at f_0. The measured *S*-parameters show that the passband ripple can be reduced by as much as 76.3% from that of the typical nMOS cross-coupled pair without degenerate loads and confirm the design methodology in Chapter 3 for minimizing the passband disturbance.

Chapter 5 demonstrates the design of wide stopband suppression for the CMOS TL-based active BPF comprehensively from the chip level to the package. Additionally, the measurement results confirm the packaged filter has the wide upper stopband, extended from 1.09f_0 to 10.05f_0, for the suppression level of 35 dB.

Chapter 6 concludes this dissertation.

Chapter 2
New Compact Synthetic Transmission Line

In this dissertation, the on-chip synthetic transmission line, the so-called condensed complementary-conducting-strip transmission line (C-CCS TL) is adopted to design CMOS TL-based active BPF. The C-CCS TLs, which have multiple signal lines in a unit cell and can substantially reduce the occupied chip area without compromising the transmission loss, are demonstrated and investigated in this chapter.

2.1 Review of Conventional CCS TL

The conventional CCS TL, which supports the quasi-TEM mode and is the forerunner of the C-CCS TL, had been demonstrated the widely flexibilities on the syntheses of guiding characteristics [19] [22] and the satisfaction of the metal density requirement in semiconductor technologies. As displayed in Fig. 2.1 (a), one signal line of the conventional CCS-TL is in a unit cell, whose dimensions are much smaller than a guiding wavelength at the operating frequency, and meanders in plane to reduce the chip area in Fig. 2.2 (a). Generally, the lumped elements are much smaller than the operating wavelength and so, can be used to miniaturize monolithic microwave and millimeter-

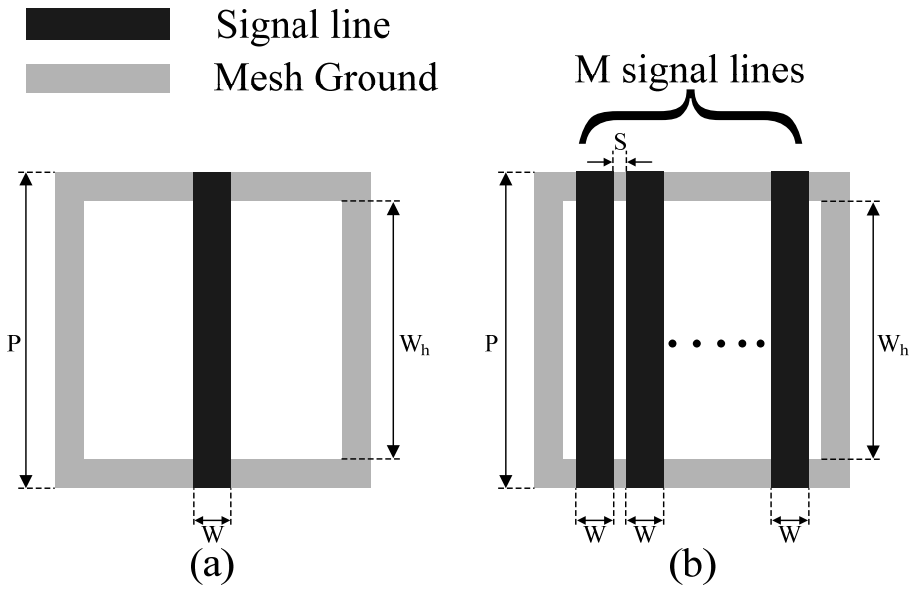


Fig. 2.1 Top-view of CCS unit cell. (a) Conventional CCS TL. (b) Condensed CCS TL.

$$\mathrm{ARF} = 1 - \frac{A_2}{A_1} = 1 - \frac{\left(\frac{8\pi}{3}\right)\left(\frac{P}{\lambda_0}\right)\left(\mathrm{SWF_{MS}}\right)^2}{\mathrm{SWF_{CCS\,TL}}} \tag{2.1}$$

$$\mathrm{AL} = \frac{\sqrt{A}}{Q\lambda_0} = \frac{\sqrt{P^2 \cdot N}}{Q\lambda_0} = \frac{P \cdot f_0 \sqrt{N}}{cQ} \tag{2.2}$$

wave integrated circuits (MMIC) based on lumped elements as much as possible. However, numerous prototypes [23]-[25], realized to verify the advantage of conventional CCS TLs, have been miniaturized more effectively than circuits based on lumped elements. Furthermore, the miniaturization of MMIC continues. The area reduction factor (ARF) of the circuit based on the CCS TL, which is defined in (2.1) [19], is inversely proportional to the periodicity (P, as shown in Fig. 2.1(a)) of the unit cell. The design guidelines, summarized as Area-Influence Loss (AL) in (2.2) and in [22,

Fig. 6], reveal that the quality factor (Q factor) of CCS TL is proportional to the periodicity in a certain range of characteristic impedances. To improve simultaneously the ARF and Q factor, the condensed CCS TL (C-CCS) is developed from the conventional CCS TL.

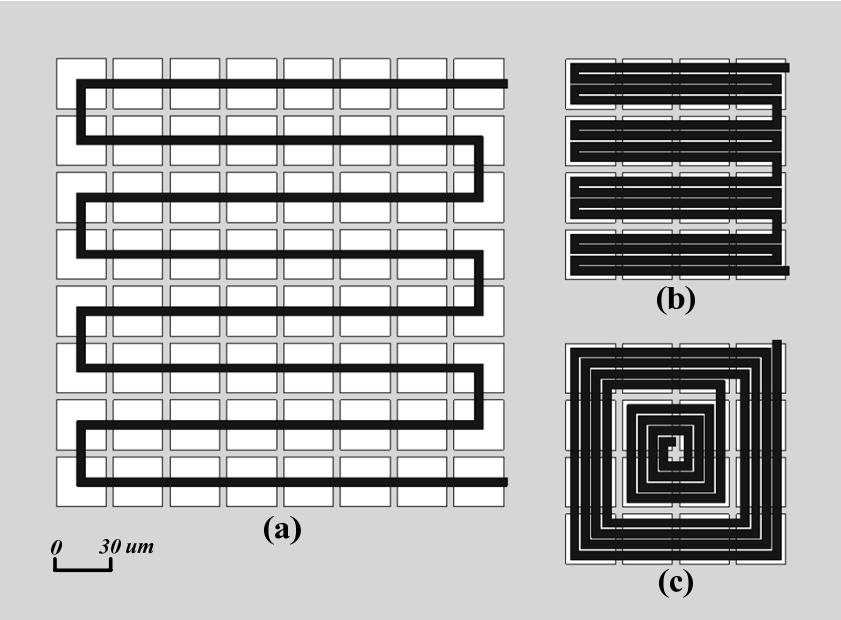


Fig. 2.2 CCS TLs with fixed length, 1920.0 μm, at fixed scale. (a) Conventional CCS TL. (b) Meander-forming C-CCS TL. (c) Whorl-forming C-CCS TL.

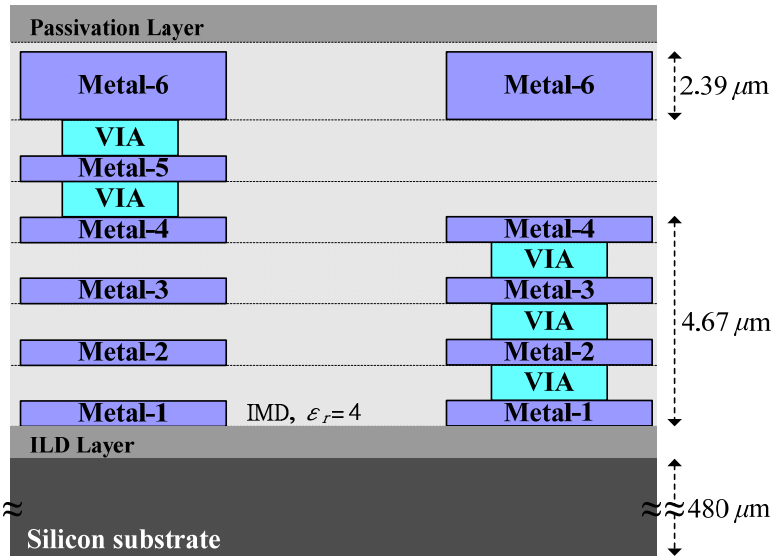


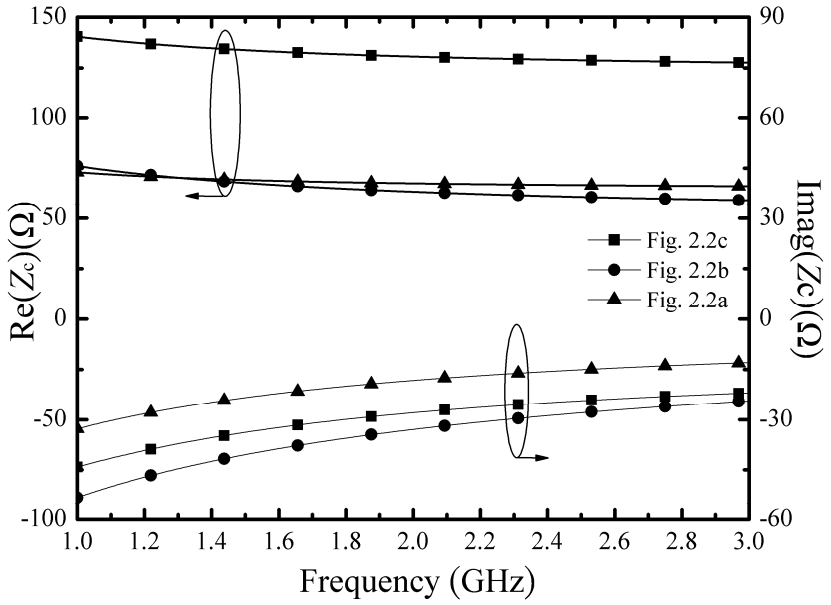
Fig. 2.3 Cross section of the standard 0.18-μm CMOS 1P6M technology.

2.2 New Condensed CCS TL

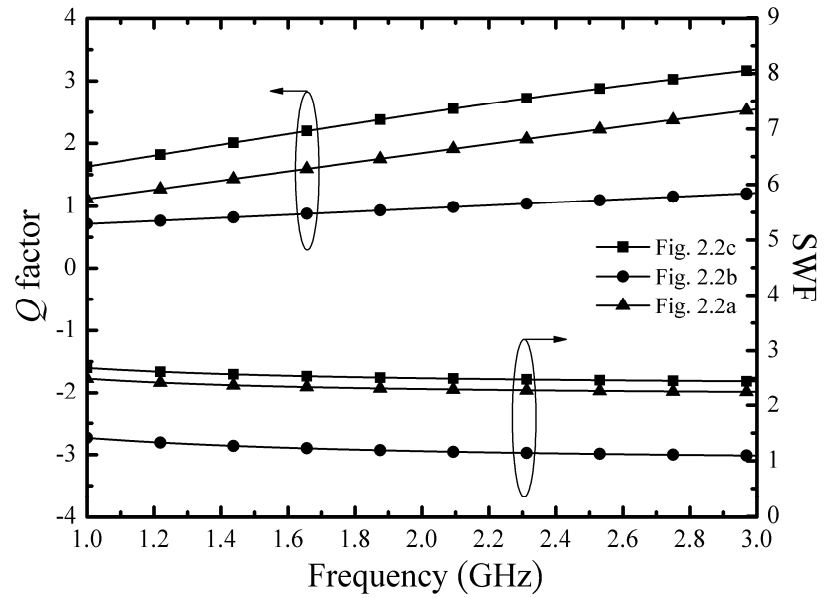
Fig. 2.2 (b) and 2.2 (c) present the C-CCS TL, in which multiple signal lines are confined to a unit cell, as shown in Fig. 2.1 (b). The possibility of miniaturization without compromising the *Q* factor of the C-CCS TL is investigated as follows. As displayed in Fig. 2.2, all of the CCS TLs employ the unit cell in Fig. 2.1, with a periodicity, P = 30.0 μm, a square opening of width, W_h = 26.3 μm in the mesh ground plane and a signal line of width, W = 4.5 μm. In Fig. 2.2 (b) and (c) the line spacing, S, between multiple signal lines in a unit cell is 1.2 μm. Standard 0.18-μm CMOS 1P6M technology involves six metal layers, as shown in Fig. 2.3. The signal line is realized by top metal layer, Metal-6, with a thickness of 2.39 μm. The mesh ground plane is made of metal layers from Metal-1 to Metal-4, yielding a thickness of 4.67 μm. The physical length of each of the three CCS TLs in Fig. 2.2 is 1920.0 μm. Fig. 2.2 (a) displays the conventional CCS TL that consists of 64 lattices. The C-CCS TLs in Fig. 2.2 (b) and 2.2 (c) with a unit cell that contains four signal lines, M=4, are composed of 16 lattices and occupy a quarter of the area that is occupied by the conventional CCS TL in Fig. 2.2(a). As reported in [19, Sec. II], reducing the periodicity, P, can increase the ARF. Additionally, for the C-CCS TL, increasing M, the number of single lines in a unit cell, can increase the ARF. Hence, the C-CCS TL can reduce the area of MMICs more than the conventional CCS TL. In Fig. 2.2 (b), which displays a meander-forming C-CCS TL,

the signal track meanders and is folded into a hairpin shape in a unit cell. In Fig. 2.2 (c), which displays a whorl-forming C-CCS TL, the signal track has the whorl form. Although Fig. 2.2 (b) and 2.2 (c) present the C-CCS TL with the same number of signals, M, in one periodicity for fixed physical length and area, different track arrangements produce different guiding characteristics. To extract the guiding characteristics of the CCS TLs in Fig. 2.2, a series of numerical analyses are conducted. The generalized two-port scattering parameters (*S*-parameters) are evaluated by conducting full-wave electromagnetic simulations, using the ANSYS High Frequency Structure Simulator (HFSS). Substituting the *S*-parameters, calculated by HFSS , into in [26, eqs. (7) and (8)], yields the guiding characteristics, including the characteristic impedance (Z_c), and the complex propagation constant (γ), which equals to $\alpha+j\beta$, where β and α, respectively, are the phase and attenuation constants of the transmission line.

Fig. 2.4 presents the simulated guiding characteristics of the CCS TLs in Fig. 2.2, and includes the characteristic impedance (Z_c), slow wave factor (SWF), quality factor (*Q* factor). Fig. 2.5 plots normalized propagation loss per guiding wavelength (λ_g). SWF is defined as β/β_0, where β_0 is the free-space phase constant and *Q* factor is defined as $\beta/(2\alpha)$. In Fig. 2.4 and Fig. 2.5, the triangles, dots and the squares represent the conventional CCS TL in Fig. 2.2 (a), the meander-forming C-CCS TL in Fig. 2.2 (b) and



(a)



(b)

Fig. 2.4. Guiding characteristics of CCS TLs in Fig. 2.2 (a) Characteristic impedance (Z_c). (b) Q factor and slow wave factor (SWF).

the whorl-forming C-CCS TL in Fig. 2.2 (c), respectively. Since the skin effect at low frequency causes the ohmic loss to dominate the total loss of the CCS TL, the imaginary part of Z_c, Im(Z_c) in Fig. 2.4 (a) is negative. In Fig. 2.4 (a), the real part of Z_c, Re(Z_c), of the whorl-forming C-CCS TL is 133.12 Ω at 1.58 GHz—almost twice that of the

conventional CCS TL and the meander-forming C-CCS TL. In Fig. 2.4 (b), the whorl-forming C-CCS TL has the highest SWF, 2.55, at 1.58 GHz exceeding the theoretical limit $\sqrt{\varepsilon_r} = 2$ for the quasi-TEM transmission line. The value ε_r is the relative dielectric constant of the inter media dielectric (IMD) of standard 0.18-μm CMOS 1P6M technology and equals 4. The conventional CCS TL has an SWF, which also exceeds 2, that approaches that of the whorl-forming C-CCS TL. The meander-forming C-CCS TL has the lowest SWF—half of that of the whorl-forming C-CCS TL. In Fig. 2.4 (b), the whorl-forming C-CCS TL has the highest Q factor, 2.13, at 1.58 GHz and the meander-forming one has the lowest. The whorl-forming C-CCS TL has the highest SWF and Q factor. Therefore, the whorl-forming C-CCS TL has the lowest normalized propagation loss in Fig. 2.5. However, the meander-forming C-CCS TL has the lowest Re(Z_c), SWF and Q factor. Although the areas and structural parameters are the same for both of the C-CCS TLs in Fig. 2.2 (b) and 2.2 (c), the different track arrangements enable the whorl-forming C-CCS TL to yield higher Re(Z_c) and lower normalized propagation loss than the meander-forming one. The comparisons in Fig. 2.5 demonstrate that the whorl-forming C-CCS TL can simultaneously improve miniaturization and reduce normalized propagation loss. Accordingly, the active BPF that is based on the whorl-forming C-CCS TL can be miniaturized without compromising performance.

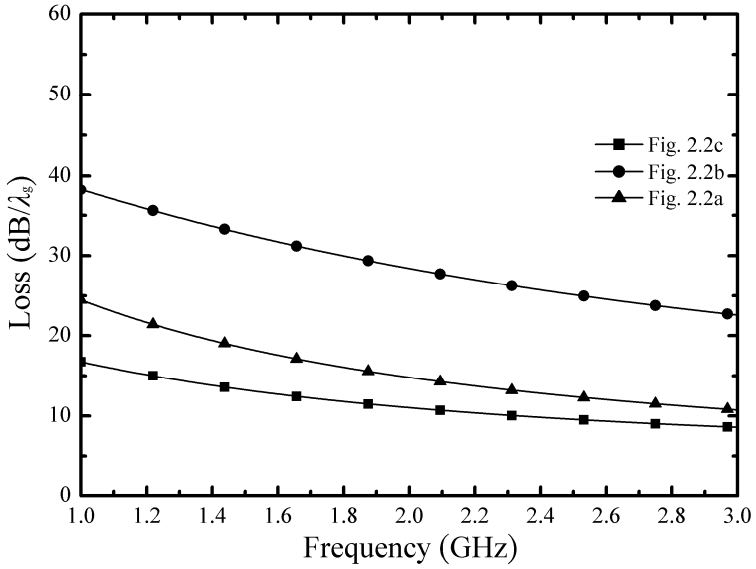


Fig. 2.5. Normalized propagation loss per guiding wavelength.

As documented in a textbook [27], the skin depth is inversely proportional to the square root of the frequency and the curves in Fig. 2.5 plot the frequency-dependence of the propagation losses of the CCS TL. The frequency-dependence of the propagation loss disturbs the passband flatness of the active BPF. The following chapter will present a design methodology that can enhance the *Q* factor of the on-chip TL-based resonator and maintain the passband flatness of an active BPF.

Chapter 3
Design of Active Bandpass Filter with Minimized Passband Disturbance

The CMOS active bandpass filter (BPF) uses the active compensating network to reduce the passband insertion loss. In addition to loss compensation, the active compensating network herein not only can minimize the passband disturbance but also improve the stability. Such a CMOS active BPF with minimized passband disturbance is demonstrated as follows.

3.1 Architecture of Active BPF

Fig. 3.1 presents the architecture of the third-order active BPF, which is implemented using standard 0.18-μm CMOS 1P6M technology. The third-order active BPF is composed of three composite parallel resonators, which are numbered from i=1 to i=3, and lumped coupling capacitors, C_{01} and C_{12}, as the immittance inverters. The voltage, V_D, at the D_i node is applied to the composite parallel resonator in Fig. 3.1. The capacitances of C_{01} and C_{12} are extracted based on the procedures in [28] for the required frequency response. The bias circuit is designed to include a pMOS current mirror to supply the drain currents to the composite parallel resonators. The total

consumed current from V_{DD} is controlled by V_C.

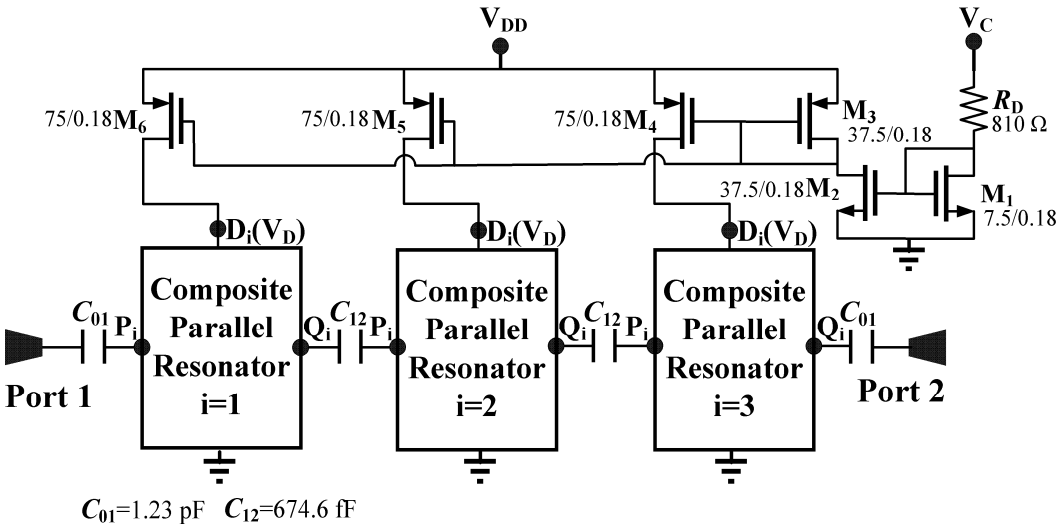


Fig. 3.1 Architecture of third-order active BPF that comprises three composite parallel resonators, which are numbered from i=1 to i=3.

3.2 *Q* enhancement using Negative Conductance Circuit

Fig 3.2 shows the composite parallel resonator [5], which is based on the CCS TL and the nMOS cross-coupled pair. The two terminals of the CCS TL and the two drain terminals of the nMOS cross-coupled pair are connected and correspond to the P_i and Q_i nodes in Fig. 3.1 and Fig. 3.2. Since the parasitic capacitance that is provided by the nMOS cross-coupled pair is a part of the composite parallel resonator, the CCS TL has a length of less than $\lambda_g/2$ where λ_g is the guiding wavelength of the used CCS TL at the resonant frequency, f_0. The composite parallel resonator operates single endedly, not differentially. Hence, the signal, between the P_i and Q_i nodes in Fig. 3.2, is the

superposition of differential-mode and common-mode signals [5]. Between the two drain terminals of an nMOS cross-coupled pair, differential-mode excitation produces negative conductance to compensate for the loss of the composite parallel resonator, and common-mode excitation results in the load. At the resonant frequency, the phase difference between two terminals of the CCS TL (or two drain terminals of an nMOS cross-coupled pair) is π. The differential-mode signal prevails over the common-mode signal in the composite parallel resonator [5]. Therefore, the admittance between the two drain terminals of the nMOS cross-coupled pair is $Y_{dd}(f)$ and the real part of the $Y_{dd}(f)$, Re($Y_{dd}(f)$) equals -g_m/2, where g_m is the transconductance of the nMOS transistor

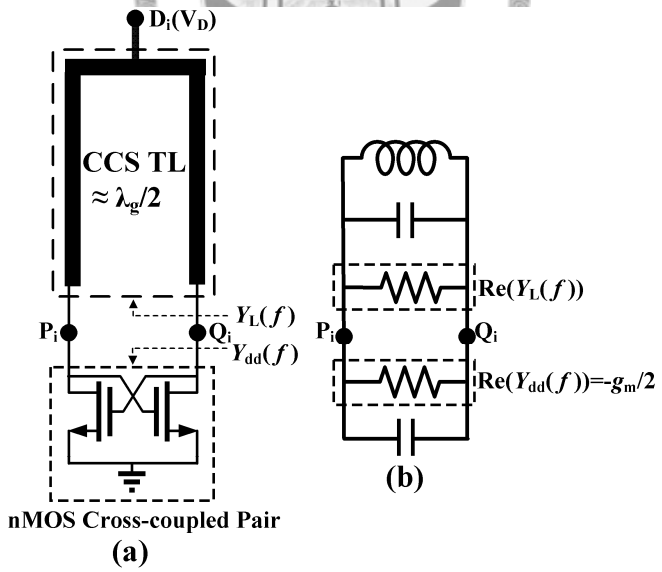


Fig. 3.2 Composite parallel resonator with negative conductance circuit (a) Schematic. (b) Equivalent lumped circuit at the resonant frequency.

in the small-signal operation. The admittance between the two terminals of the CCS TL is $Y_L(f)$ and the CCS TL is then equivalent to a parallel resonator with a parallel

conductance, Re($Y_L(f)$), which is the real part of $Y_L(f)$. Re($Y_{dd}(f)$) cancels Re($Y_L(f)$) with a proper V_D in Fig. 3.2 at the resonant frequency and the Q factor of the composite parallel resonator is enhanced. However, the ohmic loss of the CCS TL in Fig. 2.5, causes Re($Y_L(f)$) to depend on frequency but the negative conductance, Re($Y_{dd}(f)$), is the constant, $-g_m/2$. The total input conductance of the composite parallel resonator in Fig. 3.2 becomes frequency-dependent and the passband flatness of the active BPF is disturbed.

3.3 Design of Frequency-dependent Loss Compensation

The response of BPF is characterized by the Chebyshev response with various passband ripples [28], when the conductance of a parallel resonator is a constant zero at all frequencies. Therefore, to minimize the passband disturbance by the frequency-dependent Re($Y_L(f)$), (3.1) must be satisfied

$$\frac{\partial}{\partial f}\left(\mathrm{Re}(Y_L(f)) + \mathrm{Re}(Y_{dd}(f))\right)\Big|_{f=f_0} \approx 0 \qquad (3.1).$$

In Fig. 2.5, the derivative of the loss of CCS-TLs is negative and thus the derivative of Re($Y_L(f)$) is also negative. Consequently, the active compensating network must be modified to produce the frequency-dependent Re($Y_{dd}(f)$) with a positive derivative to

satisfy (3.1).

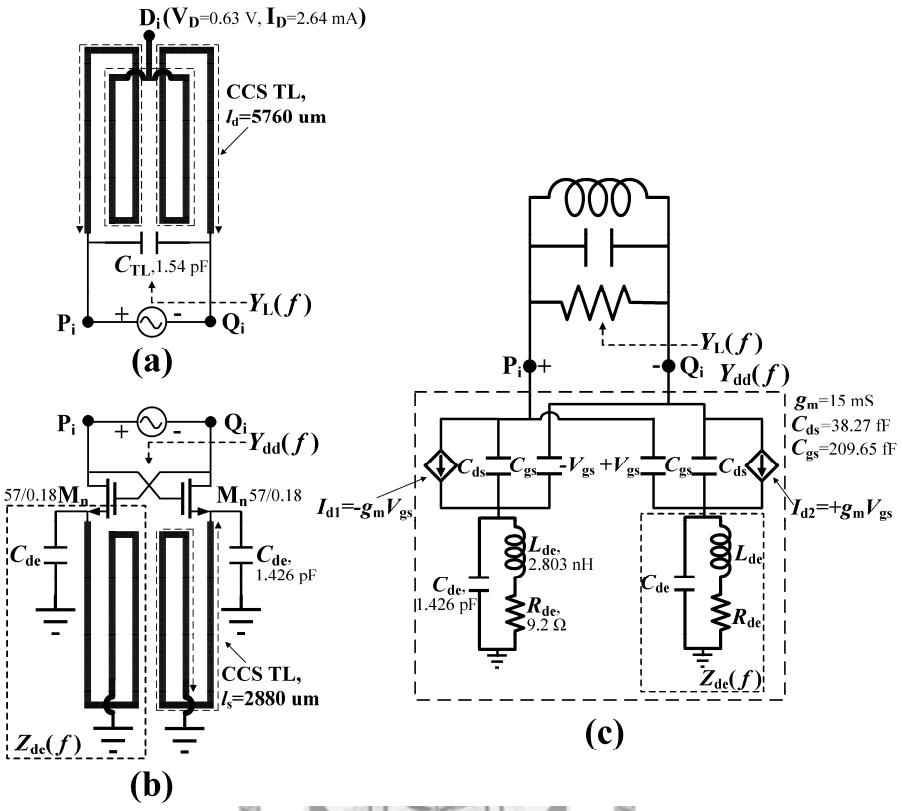


Fig. 3.3. Composite parallel resonator with frequency-dependent negative conductance compensation (a) TL-based resonator. (b) Active compensating network with the degenerate load. (c) Equivalent lumped circuit at the resonant frequency.

As presented in Fig. 3.3 (a), the TL-based resonator is composed of a CCS TL and a lumped capacitor with a capacitance, C_{TL} and the equivalent circuit is as shown in Fig. 3.3 (b). In Fig. 3.3 (b), the active compensating network comprises the nMOS cross-coupled pair and two identical degenerate loads. The degenerate load, which is realized by a short-circuited CCS TL connected in parallel with a shunt capacitor with a capacitance, C_{de}, is inserted between the source terminal of the nMOS transistor and the ground. Fig. 3.3 (c) represents the equivalent circuits of Fig. 3.3 (a) and Fig. 3.3 (b). The equivalent circuit of the degenerate load is represented as a parallel resonator that

consists of the inductance, L_{de}, the resistance, R_{de}, and C_{de}. The input impedance, looking into the degenerate load from the source terminal of nMOS transistor, is defined by $Z_{de}(f)$ and can be expressed by

$$Z_{de}(f) = \frac{R_{de} + j\omega L_{de}}{1 - \omega^2 L_{de} C_{de} + j\omega R_{de} C_{de}} \quad (3.2),$$

where ω equals $2\pi f$. The P_i and Q_i nodes in Fig. 3.3 combine the TL-based resonator in Fig. 3.3 (a) with the active compensating network in Fig. 3.3 (b) and the composite parallel resonator is formed. At the resonant frequency, the phase difference between the P_i and Q_i nodes equals π, the $Y_{dd}(f)$ shown in Fig. 3.3 (c) can be expressed by

$$Y_{dd}(f) = \frac{1}{2}\left(\frac{-g_m - 4\omega^2 C_{gs} C_{ds} \cdot Z_{de}(f) + j\omega(C_{gs} + C_{ds})}{1 + Z_{de}(f) \cdot (g_m + j\omega(C_{gs} + C_{ds}))}\right) \quad (3.3),$$

where C_{gs} and C_{ds} are the capacitance between the gate and source terminals and between the drain and source terminals, of the nMOS transistor, respectively. In (3.3), the real part of the $Y_{dd}(f)$, $\mathrm{Re}(Y_{dd}(f))$ is frequency-dependent and the derivative of $\mathrm{Re}(Y_{dd}(f))$, is determined by the degenerate load. Appropriate design of the degenerate load makes derivative of the $\mathrm{Re}(Y_{dd}(f))$ positive and approach the derivative of $|\mathrm{Re}(Y_L(f))|$. Therefore, (3.1) can be satisfied and the passband disturbance of the active BPF can be minimized. Equation (3.2) is substituted into (3.3) to yield $\mathrm{Re}(Y_{dd}(f))$ and

the derivative of Re($Y_{dd}(f)$) is obtained by differentiating Re($Y_{dd}(f)$)[see (A1) and (A2) in Appendix].

For verifying the validities of (3.2) and (3.3), the TL-based resonator in Fig. 3.3 (a) and the active compensating network in Fig. 3.3(b) are designed based on standard 0.18-μm 1P6M CMOS technology. In the BPF design, the resonant frequency of a composite parallel resonator, f_0, is 1.58 GHz. To achieve the TL-based active BPF with the highest miniaturization and acceptable performance, the whorl-forming C-CCS TL, which has four signal lines confined in one periodicity, is adopted with the following structural parameters, shown in Fig. 2.1 (b). P and W_h are 90.0 μm and 78.75 μm, respectively. The width, W, and the line spacing, S are 13.5 μm and 1.2 μm, respectively. The mesh ground plane is made of metal layers from Metal-1 to Metal-4 yielding a thickness of 4.67 μm. The signal line is realized by top metal layer, Metal-6, with a thickness of 2.39 μm. The guiding characteristics are computed as a Re(Z_c) of 103.9 Ω, a Q factor of 4.7 and an SWF of 2.85 at 1.58 GHz. The TL-based resonator in Fig. 3.3 (a) uses C_{TL} of 1.54 pF and the whorl-forming C-CCS TL with a length, l_D, of 5760.0 μm. The two nMOS transistors in the active compensating network in Fig. 3.3 (b) have a width of 1.5×38 μm and a length of 0.18 μm. In the degenerate load, C_{de} is 1.426 pF and the whorl-forming C-CCS TL, whose guiding characteristics are identical to those of the whorl-forming C-CCS TL used in the TL-based resonator, has a length, l_S, of 2880.0 μm.

At the resonant frequency, between the P_i and Q_i nodes with a phase difference of π, the equivalent lumped circuit of the composite parallel resonator is displayed in Fig. 3.3 (c). The parallel conductance of the TL-based resonator is $\mathrm{Re}(Y_L(f))$. After the practical circuits of the TL-based resonator and degenerate load, as presented in the next chapter, are calculated using the HFSS simulator, $\mathrm{Re}(Y_L(f))$ is 4.28 mS with a derivative of -3.596 mS/GHz at the resonant frequency. L_{de} of 2.803 nH and R_{de} of 9.2 Ω are extracted at the resonant frequency. When a current of 2.64 mA is consumed by the active compensating network from a V_D of 0.63 V at the D_i node, the transconductance, g_m, is 15 mS and, C_{gs} and C_{ds} are 209.65 fF and 38.27 fF, respectively. g_m, C_{gs}, C_{ds}, L_{de}, R_{de} and the given C_{de} are substituted into (A1) and (A2) and $\mathrm{Re}(Y_{dd}(f))$, -4.28 mS, and the derivative of $\mathrm{Re}(Y_{dd}(f))$, 3.757 mS/GHz, are obtained at the resonant frequency. In Fig. 3.3 (c), at the resonant frequency, the sum of the imaginary parts of $Y_L(f)$ and $Y_{dd}(f)$, $\mathrm{Im}(Y_L(f))$ and $\mathrm{Im}(Y_{dd}(f))$, is zero. $\mathrm{Re}(Y_L(f))$, 4.28 mS is clearly canceled by $\mathrm{Re}(Y_{dd}(f))$, -4.28 mS and the Q factor of the composite parallel resonator is thus enhanced. Equation (3.1), the sum of the derivative of $\mathrm{Re}(Y_L(f))$, -3.596 mS/GHz, and the derivative of $\mathrm{Re}(Y_{dd}(f))$, 3.757 mS/GHz, is 0.161 mS/GHz, or 1.61×10^{-3} mS/10MHz, which approaches zero. Consequently, the passband disturbance in the active BPF can be minimized.

The caption in Fig. 3.4 represents the composite parallel resonator, which is

composed of the TL-based resonator in Fig. 3.3 (a) and the active compensating network in Fig. 3.3 (b). The equivalent circuit of the resonator is shown in Fig. 3.3 (c). As shown in Fig. 3.4, $Y_{CPR}(f)$ is the input admittance, looking into the composite parallel resonator from the P_i node. The design is validated using the simulator, Agilent Advanced Design System (ADS) 2009. The curves with square and triangular symbols in Fig. 3.4 plot the input conductance, which is the real part of $Y_{CPR}(f)$, Re($Y_{CPR}(f)$), of the composite parallel resonator with and without the degenerate load, respectively. The composite parallel resonator without degenerate load, has a $Z_{de}(f)$ of zero, and consumes

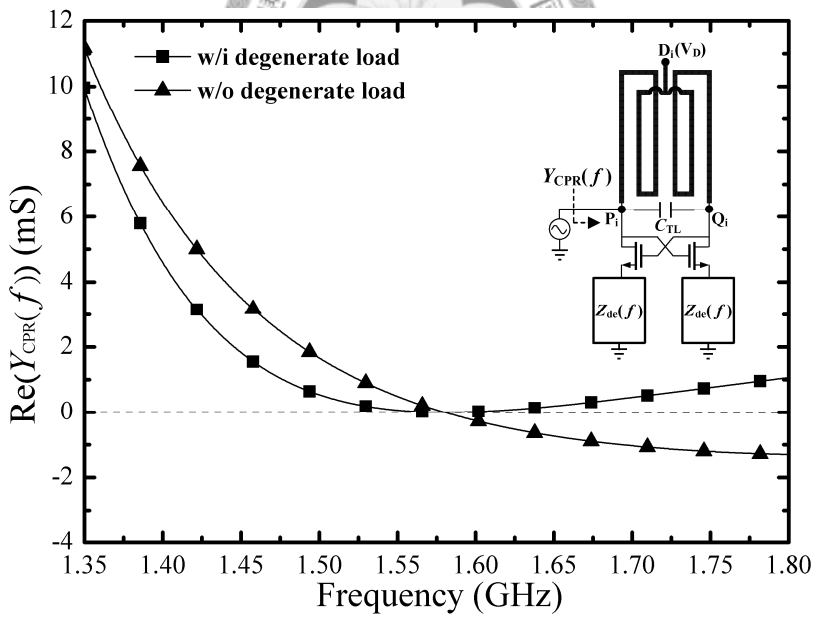


Fig. 3.4. Simulated Re($Y_{CPR}(f)$) of composite parallel resonator with and without degenerate load.

a current of 1.24 mA from a V_D of 0.57 V at D_i node. The curve with triangular symbols shows a Re($Y_{CPR}(f)$) that is reduced from 1.35 GHz with a negative derivative, and zero at 1.58 GHz. Above 1.58 GHz, Re($Y_{CPR}(f)$) is negative, implying potential instability of

the composite parallel resonator without the degenerate load. For the composite parallel resonator with the degenerate load, the curve with square symbols shows a similar trend to that with triangular symbols, except at frequencies above 1.5 GHz. The slope of $\mathrm{Re}(Y_{\mathrm{CPR}}(f))$ markedly declines from 1.5 GHz and a bandwidth, within which $\mathrm{Re}(Y_{\mathrm{CPR}}(f))$ is zero and the derivative of $\mathrm{Re}(Y_{\mathrm{CPR}}(f))$ approaches zero, from 1.56 GHz to 1.6 GHz is limited by the degenerate load. Above 1.6 GHz, $\mathrm{Re}(Y_{\mathrm{CPR}}(f))$ and the derivative of $\mathrm{Re}(Y_{\mathrm{CPR}}(f))$ are positive, revealing the stability of the composite parallel resonator with the degenerate load.

The aforementioned comparisons verify the feasibility of the demonstrated active compensating network with the degenerate load that can minimize the passband disturbance and stabilize the active BPF. The next chapter describes a practical prototype of the TL-based active BPF with the design methodology that is presented in this chapter.

Chapter 4
Prototype Implementation and Measurement Results

The practical prototype in CMOS 0.18-μm 1P6M technology and measurement results, which are exhibited in this chapter, reveals the feasibility of the proposed methodology in Chapter 2 and 3.

4.1 Prototype in CMOS 0.18-μm 1P6M Technology

Fig. 4.1 shows the prototype of a third-order TL-based active bandpass filter (BFP) in standard 0.18-μm complementary metal-oxide-semiconductor (CMOS) one-poly six-metal (1P6M) technology. The thickness of the silicon substrate is 480.0 μm. All capacitors are realized with metal-insulator-metal (MIM) topology with a capacitance density of 1.0 fF/μm^2. The susceptance of the composite parallel resonator, whose design is described in Chapter 3, is extracted and the two coupling capacitances of C_{01}, 1.23 pF and C_{12}, 674.6 fF, shown in Fig. 3.1, are calculated to meet the central frequency (resonant frequency), 1.58 GHz and bandwidth from 1.52 GHz to 1.64 GHz. The D_i, P_i and Q_i nodes of the composite parallel resonator in Fig. 3.3 correspond to the D_i, P_i and Q_i nodes in Fig. 4.1. The whorl-forming C-CCS TL, adopted in the TL-based

resonator, is implemented in 16 CCS cells, which occupy an area of 360.0 μm by 360.0 μm. The whorl-forming C-CCS TL, used in the degenerate load is implemented in 8 CCS cells, with an area of 360.0 μm by 180.0 μm. In the bias circuit, a pMOS current mirror is designed as shown in Fig. 3.1. In Fig. 4.1, the total area of the prototype without the contact pads is 1099.47 μm × 837.48 μm, corresponding to an area of 0.58% λ_0 × 0.44% λ_0. *S*-parameters of the whorl-forming C-CCS TLs and MIM capacitors, which are used in the prototype that is displayed in Fig. 4.1, are evaluated by ANSYS HFSS and the simulation results of the prototype are generated using Agilent ADS 2009.

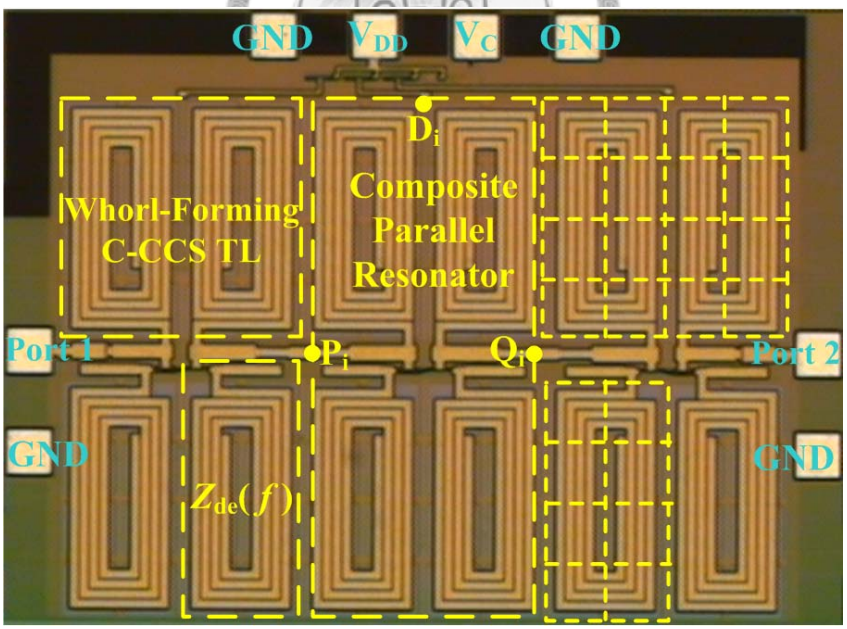
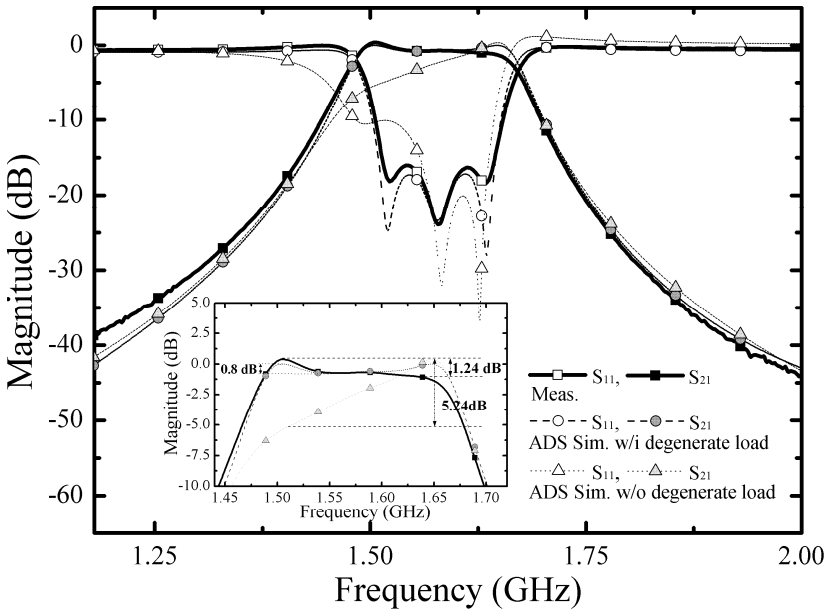


Fig. 4.1 Prototype of 1.58 GHz third-order active BPF in CMOS 0.18-μm 1P6M technology; chip area is 1099.47 μm by 837.48 μm.

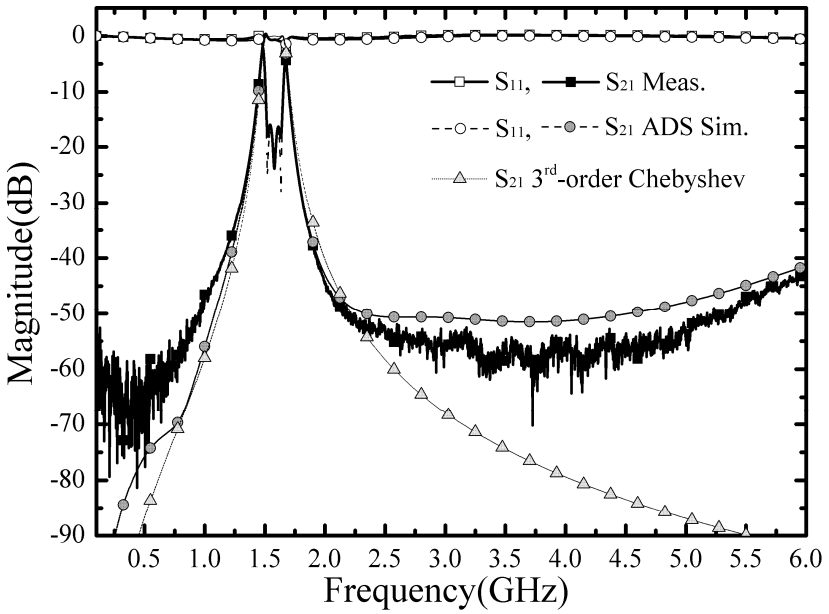
4.2 *S*-parameter Measurements

On-wafer measurements to characterize the two-port *S*-parameters of the prototype

in the 50-Ω system are performed using an Agilent E8361C performance network analyzer (PNA) after short-open-load-through (SOLT) calibration procedures are carried out. The prototype is connected to the PNA through Picoprobe un-balanced SG and GS probes, manufactured by GGB Industries Inc., Naples, FL. The output power of the PNA is set to -17.0 dBm in the small-signal experiments. Before the small-signal measurements are reported, contact pads applied to the RF input/output ports of the prototype in Fig. 4.1 are deembeded. The total power consumed by the prototype is 8.0 mA from a V_{DD} of 1.8 V, when V_c is set to 0.86 V. The solid curve with square symbols in Fig. 4.2 (a) has three reflection zeros with a return loss of more than 16.0 dB. It experimentally confirms the order of the prototype. The central frequency is 1.58 GHz. The 3dB bandwidth is 126.4 MHz, or 8.0% at the central frequency. In the caption of Fig. 4.2 (a), the doted curve with triangular symbols reveal the simulation results without the degenerate load, exhibiting a passband ripple of 5.24 dB. The dashed curve with dot symbols represents the simulation results with the degenerate load, showing a passband ripple of 0.8 dB. The comparison between these two curves shows that the proposed active compensating network with the degenerate load can reduce the passband ripple by as much as 84.73%. Additionally, the solid curve with square symbols shows that the measured insertion loss is 0.68 dB at the central frequency and a passband ripple is 1.24 dB. The measurement results agree with the simulation results



(a)



(b)

Fig. 4.2. Two-port *S*-parameters of prototype that is displayed in Fig. 4.1 in 50-Ω system. (a) Narrowband responses from 1.0 to 2.0 GHz. (b) Wideband responses from 0.1 GHz to 6 GHz.

with the degenerate load, except the difference in passband ripple. This improvement of the passband flatness, which relies on (3.1), is based on a major assumption that the g_m of two nMOS transistors is identical. However, the transistor mismatch, which is

generated by the process variation and the layout arrangement, makes each resonator have different Q factor and disturbs the passband flatness. The comparison between the curves in the caption of Fig. 4.2 (a) shows a little difference in the right corner of the passband, revealing about ±10% variation in the Q factor of the resonators. Therefore, as the measurement results are compared with the simulation data without the degenerate load, the passband ripple is reduced by 76.3%. The experimental data in Fig. 4.2 (a) prove the design methodology of the active compensating network presented in Chapter 3 minimizes the passband disturbance. Although similar designs for the lump-based active BPF have been described in [9], the realization of such an active BPF is based on differential topology. Fig. 4.2 (b) plots the wideband responses of the prototype from 0.1 GHz to 6 GHz. The solid curve with square symbols, which represents the measurement results, shows that the out-band suppressions at twice and triple the central frequency are 52.26 dB and 55.3 dB, respectively. The short-doted curve with triangular symbols in Fig. 4.2 (b) plots the ideal bandpass frequency response, which is characterized by the third-order Chebyshev polynomial with an identical return-loss to that of the prototype shown in Fig. 4.1 in the 50-Ω system. Both simulation and measurement results concerning the prototype are almost identical to the ideal Chebyshev response. The conductance of an ideal parallel resonator is a constant zero at all frequencies. However, as displayed in Fig. 3.4, the degenerate load limits a

bandwidth, within which the Q factor of the composite parallel resonator is enhanced (zero Re($Y_{CPR}(f)$)) and the derivative of Re($Y_{CPR}(f)$) approaches zero. Therefore, the difference below 1.49 GHz is caused by insufficient Q enhancement. The comparisons in Fig. 4.2 (b) verify that the design methodology that is proposed in Chapter 3 can be used to apply the classical filter syntheses [28] in the active BPF design based on standard 0.18-μm CMOS 1P6M technology.

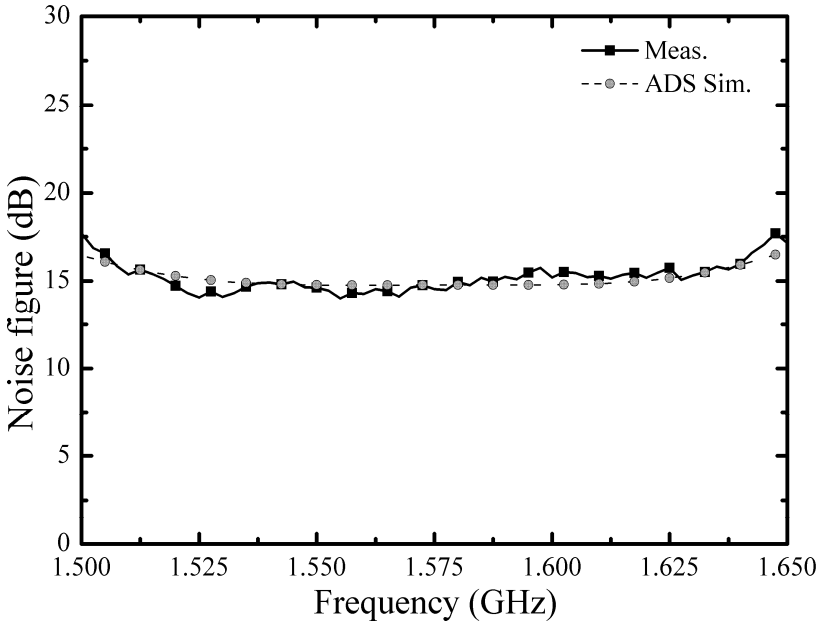


Fig. 4.3. Noise figure (NF) of the prototype that is displayed in Fig. 4.1.

4.2 Noise Figure and Linearity Characteristics

The noise figure (NF) and the linearity of the prototype are also obtained from the on-wafer measurements. The NF measurements are carried out at room temperature in a 50-Ω system. Fig. 4.3 reveals that the measured NF is consistent with the simulated result using ADS, around 15 dB from 1.52 GHz to 1.59 GHz and has a minimum value

of 14 dB at 1.56 GHz. The relationship between the noise figure of the active devices and the filter are analyzed and reported in the section IV of [5]. By properly selecting the size and the biasing point of the nMOS cross-coupled pair, the noise of the active device can be reduced, resulting in the NF improvement of the prototype.

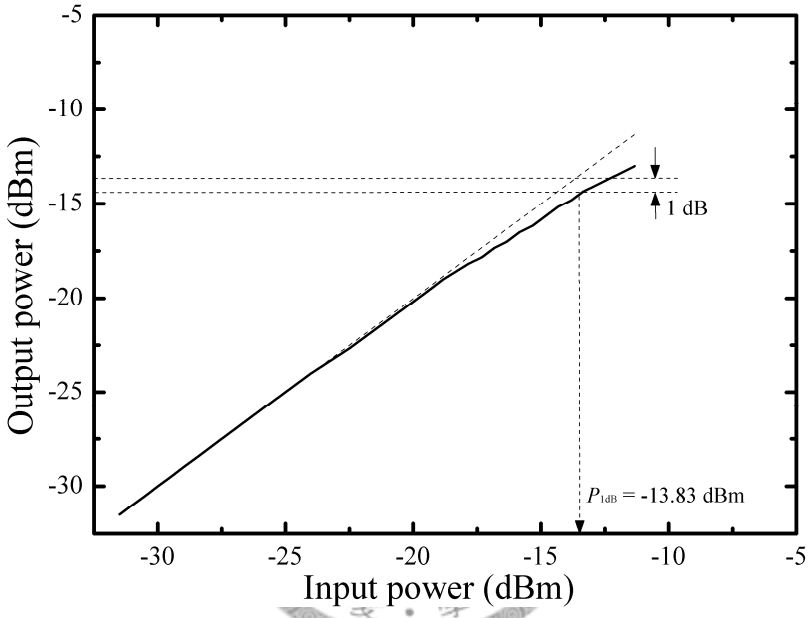
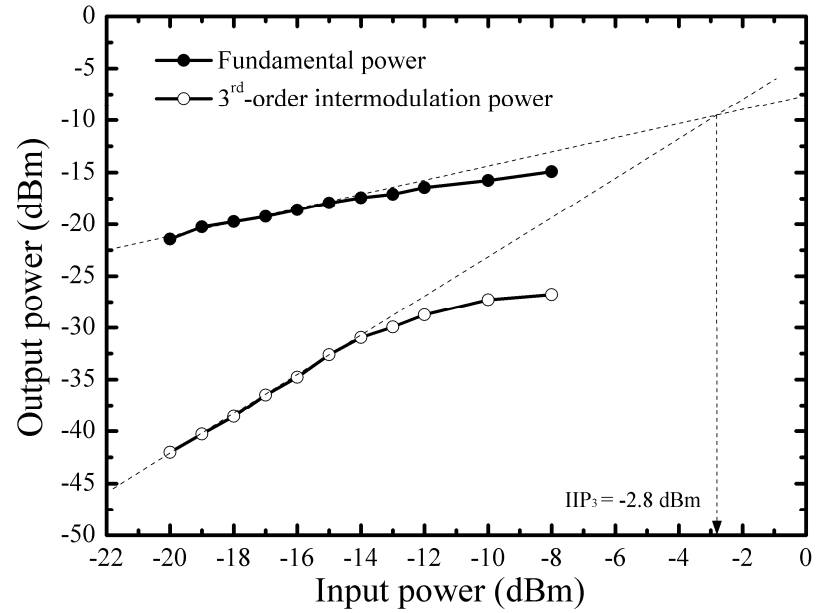
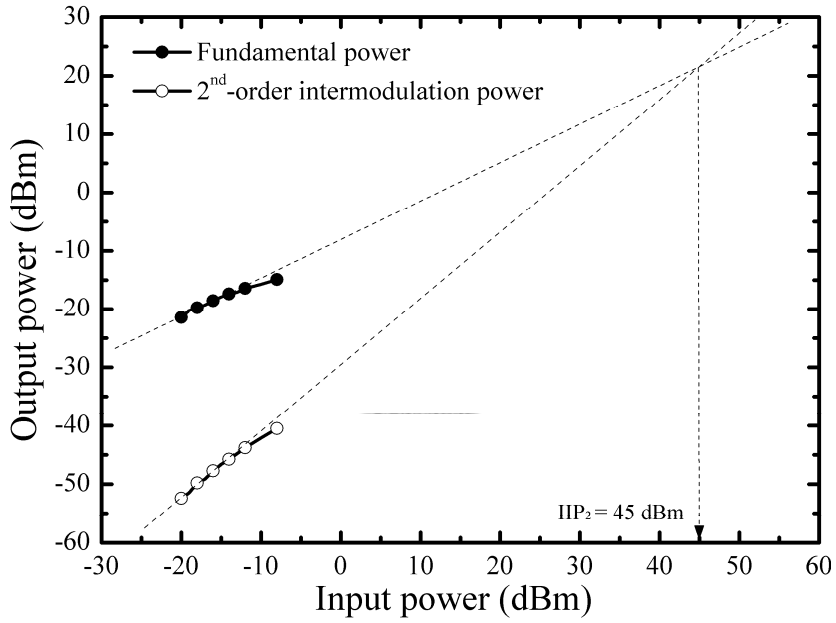


Fig. 4.4. Measured 1-dB compression point (P_{1dB}) of prototype shown in Fig. 4.1

Fig. 4.4 shows that the measured input 1-dB compression point (P_{1dB}) is -13.83 dBm at 1.58 GHz, with a power consumption of 14.4 mW from 1.8 V supply. To measure the effect of intermodulation, two test signals at 1.57 and 1.59 GHz are used; they cause the in-band third-order intermodulation products at 1.55 and 1.61 GHz. As displayed in Fig. 4.5 (a), the measured input third-order intermodulation intercept point (IIP_3) is -2.8 dBm. The second-order intermodulation product appears at 3.16 GHz without the passband. The high out-band suppression at twice the central frequency, as



(a)



(b)

Fig. 4.5. (a) Measured 3rd-order intermodulation intercept point (IIP_3). (b) Measured 2nd-order intermodulation intercept point (IIP_2) of prototype shown in Fig. 4.1.

shown in Fig. 4.2 (b), causes the measured input second-order intermodulation intercept point (IIP_2) to reach as high as 45 dBm in Fig. 4.5 (b). In the schematic of Fig. 3.1, the unbalanced loads at the two drain terminals, P_i and Q_i, of an nMOS cross-coupled pair initially limit the linearity of the prototype. For the requested frequency response, the

linearity of the prototype can be improved by properly selecting the susceptance slope parameter, which is related to the guiding characteristics of the on-chip synthetic transmission line, of the composite parallel resonator to reduce the difference in coupling capacitance between C_{01} and C_{12}.

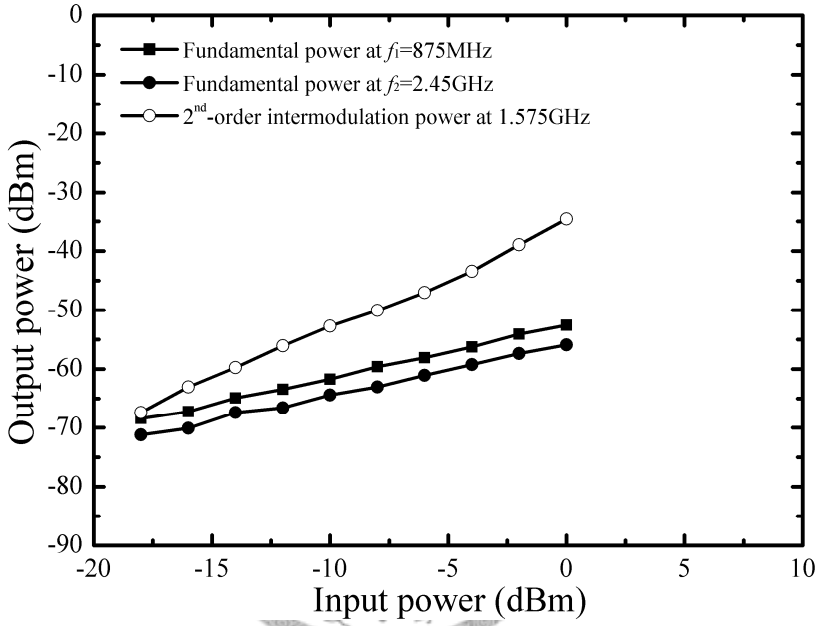


Fig. 4.6. Measured out-band 2nd-order intermodulation of prototype that is displayed in Fig. 4.1.

Although the active BPF exhibits high out-band suppression, resisting the out-band signal, a weak out-band signal still penetrates the active BPF. The nonlinearity of the active BPF causes out-band intermodulation product potentially to fall within the passband of the active BPF. If the two tone signals at f_1, 875 MHz and f_2, 2.45 GHz penetrate the prototype shown in Fig. 4.1, then the out-band second-order intermodulation product appears at 1.575 GHz within the passband. Fig. 4.6 shows the measured out-band second-order intermodulation with a consumed current of 8 mA

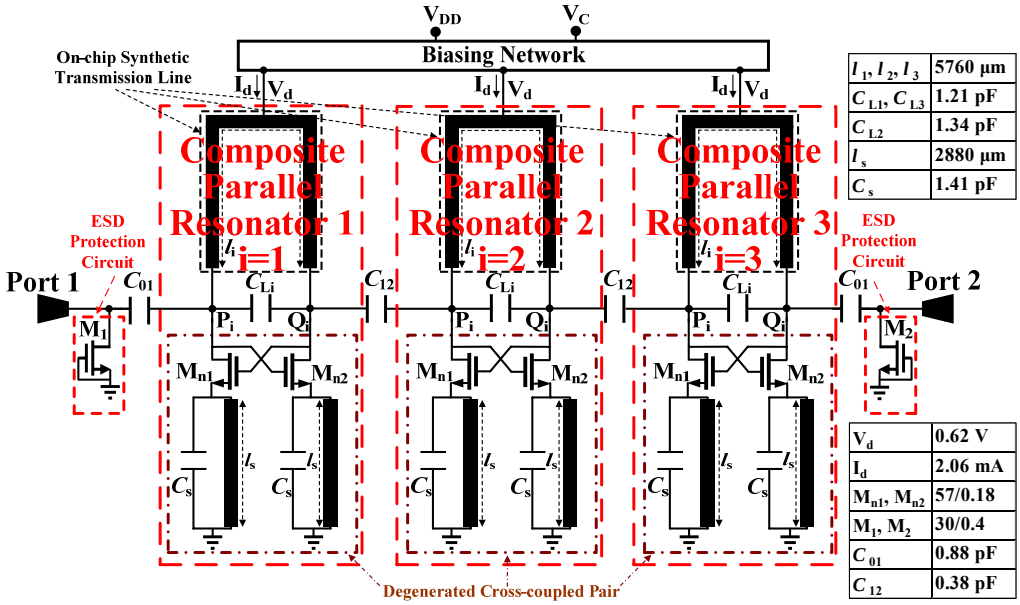
from 1.8 V supply. Since the two insertion losses at 2.45 GHz and 875 MHz without the passband are different, the curve with dot symbols, which represents the output power of the tone at 2.45 GHz, is different from the curve with square symbols, which represents the output power of the tone at 875 MHz in Fig. 4.6. As the input power increases from -18 dBm to 0 dBm, the output power of out-band second-order intermodulation product proportionally increases from -67.4 dBm to -34.6 dBm.

Chapter 5
Packaged CMOS TL-Based Active Bandpass Filter with Wide Stopband Supression

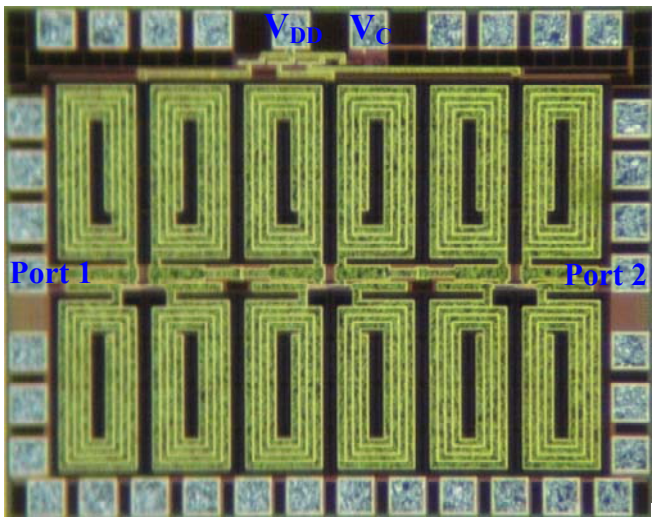
High miniaturization and in-band loss compensation with minimized passband disturbance for the transmission line (TL-based) active BPF are discussed from Chapter 2 to 4. However, this chapter focuses on the behavior of the composite parallel resonator out of the passband and the impact of the package parasitic on the stopband suppression. The measurement results show that the packaged CMOS TL-based active BPF herein has wide upper stopband, extended from $1.09f_0$ to $10.05f_0$, for the suppression level of 35 dB. Additionally, the *S*-parameters over a temperature variation from -40℃ to +80 ℃ are measured and reported in this chapter.

5.1 CMOS TL-Based Active BPF with High Stopband Suppression

Fig. 5.1 shows the schematic of a third-order transmission-line based (TL-based) active BPF, fabricated in 0.18-μm CMOS 1P6M technology, and the photograph of the prototype. The architecture is described in Chapter 3. Two gate-grounded nMOS



(a)



(b)

Fig. 5.1. 1.55 GHz third-order CMOS TL-based active BPF (a) Schematic (b) Prototype in 0.18-μm CMOS 1P6M technology in a chip area of 1.24 mm by 0.92 mm and a wafer thickness of 480 μm.

transistors (M1 and M2), which form the PS- and NS-mode current discharging paths, are inserted into the input and output ports for the electrostatic discharge (ESD) protection [29]. The on-chip synthetic TL, C-CCS TL, which is loaded with a lumped capacitor and a degenerated cross-coupled pair at P_i and Q_i nodes, forms a composite

parallel resonator in Fig. 5.1. The C-CCS TL, which is described in Chapter 2, has the attractive advantages of high-characteristic-impedance synthesis and substantial circuit miniaturization without compromising the transmission loss. A degenerated cross-coupled pair, which is theoretically and experimentally validated in Chapter 3 and 4, can be applied to design the input conductance of a composite parallel resonator as a constant value, which approaches zero, in a certain bandwidth to improve the passband flatness. However, the behavior of a composite parallel resonator out of the passband and its impact on the spurious responses is the main object of this chapter.

θ_{pq} is the phase difference between the two drain terminals of an nMOS cross-coupled pair at P_i and Q_i nodes. As the θ_{pq} equals 2π, 4π, 6π and $2n\pi$ at $2f_0$, $4f_0$, $6f_0$, and $2nf_0$ (where n is an integer and numbered from 1), the two drain terminals of nMOS cross-coupled pair at P_i and Q_i nodes are in phase. The degenerated cross-coupled pair becomes a load, and the Q factor of the composite parallel resonator can not be enhanced at even-harmonic frequencies as $2f_0$, $4f_0$, $6f_0$, and $2nf_0$. Similarly, the spurious responses at $2f_0$, $4f_0$, $6f_0$, and $2nf_0$ do not improve for the CMOS TL-based active BPF. Nevertheless, the degenerated cross-coupled pair provides differential negative conductance with θ_{pq} equal not only to π, but also to 3π, 5π, and $(2n-1)\pi$. Restated, the Q factor of the composite parallel resonator can be enhanced not only at f_0, but also at $3f_0$, $5f_0$, and $(2n-1)f_0$. Therefore, the CMOS TL-based active BPF exhibits significant

spurious responses at odd-harmonic frequencies as $3f_0$, $5f_0$, and $(2n-1)f_0$. An attempt is made to achieve wide upper stopband suppression for the CMOS TL-based active BPF with loss compensation based on the nMOS cross-coupled pair by using a capacitively loaded TL resonator [30]. For the composite parallel resonator in Fig. 5.1, the length of C-CCS TL is adjusted appropriately and C_{Li} can be estimated at the resonant frequency, f_0, to control the spurious responses and achieve the requested upper stopband suppression. The phenomena mentioned above can be quantitatively investigated through the resonator designs. Fig. 5.2 shows the comparisons between the five composite parallel resonators with the different length of C-CCS TL. During the designs, the guiding characteristics of the C-CCS TL and the size of two nMOS transistors in the cross-coupled pair are identical to those adopted in Chapter 3. The resonant (fundamental) frequency, f_0, is designed at 1.55 GHz, and the commercial software, Aiglent ADS, is applied to perform the circuit simulations for observing the input impedance magnitude of the resonators. Since composite parallel resonator in Fig. 5.1 (a) forms the parallel resonance, the input impedance magnitude has a first peak at f_0, and the other above peaks, due to the spurious phenomena. The f_{es1} in the Fig. 5.2 indicates the frequency of the second peak, implying the lowest frequency, at which the first enhanced spurious response occurs. The curve with hollow dots in Fig. 5.2 shows that the ratio of f_{es1} to f_0 increases from 3.31 to 6.09 while the electric length of the

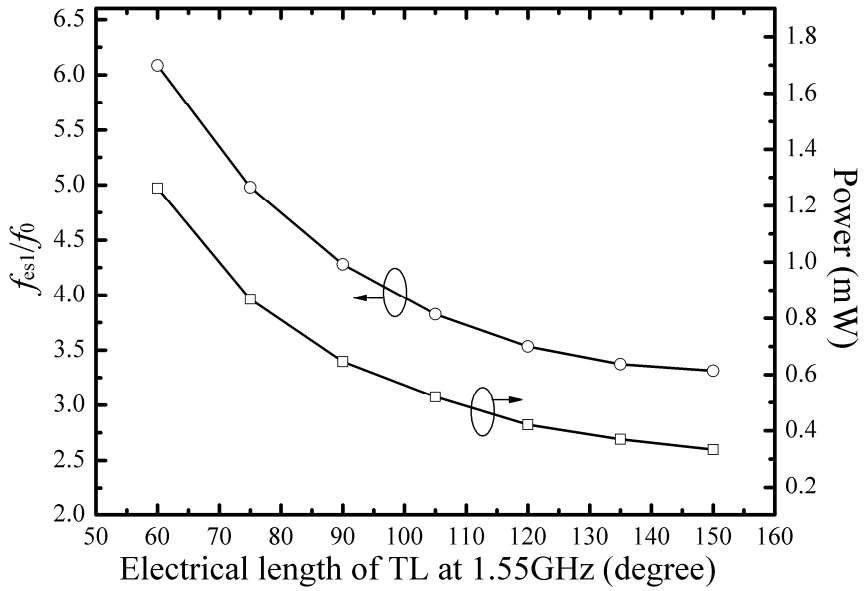


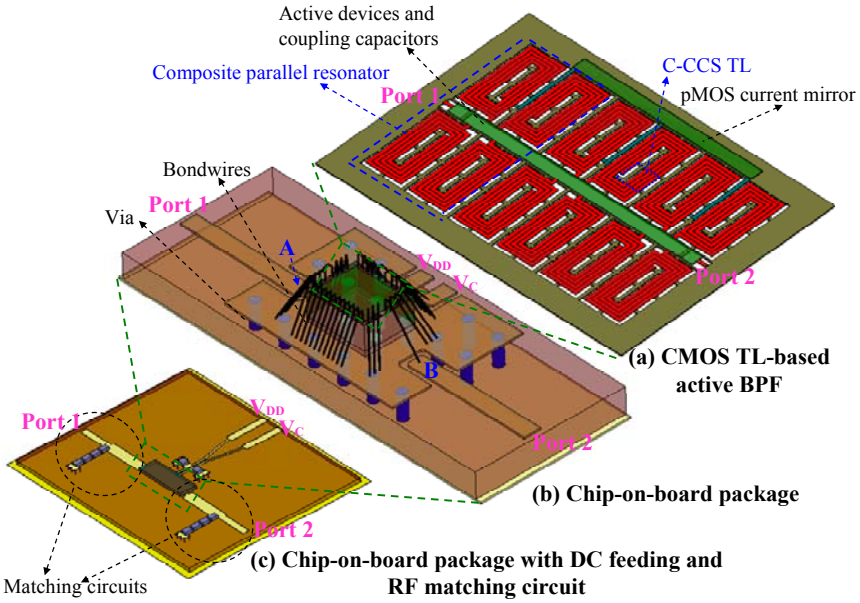
Fig. 5.2. The power consumptions and spurious responses of the composite resonators at 1.55 GHz.

C-CCS TL decreases from 150.6° to 60°, indicating the shift of the spurious responses away from the passband of the filter. The composite parallel resonator constructed with the shorter transmission line can assist the active BPF in realizing wider stopband suppression. Additionally, the curve with hollow squares shows the power consumption of a composite parallel resonator increases from 0.33 mW to 1.26 mW, while the length of the C-CCS TL decreases from 150.6° to 60°. Since the equivalent parallel conductance of the passive TL-based resonator is inversely proportional to the length of the C-CCS TL, the higher negative conductance from the degenerated cross-coupled pair is required for Q enhancement. The comparisons summarized above show the design approach to control the spurious responses for the monolithic TL-based active BPF. Moreover, the curves in Fig. 5.2 reveal the trade-off design between the spurious

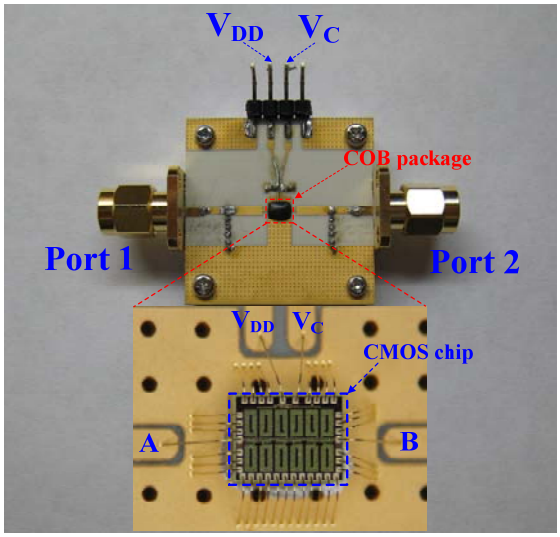
suppression and the power consumption of the proposed active BPF.

5.2 Package Design

The package for the proposed CMOS TL-based active BPF is realized by using the standard chip-on-board (COB) process, as shown in Fig. 5.3. The board is made of a two-layer laminated substrate, RO4003, with a thickness of 0.508 mm and a relative permittivity of 3.38. The fabricated chip shown in Fig. 5.1 (b) is attached to the board with silver glue, as shown in the top view of Fig. 5.3 (b). Wire bonding is adopted for electrical connections between the chip and the package, and a bondwire is made of gold with a diameter of 25.4 μm. The chip and bondwires are covered entirely by the plastic encapsulant with a relative permittivity of 9.2. In Fig. 5.3 (b), the area of the package is 3.71 mm by 2.50 mm and the board is fixed on an aluminum holder for a series of experiments. To investigate the impacts of the parasitic inductances on the proposed active BPF, the commercial software, ANSYS HFSS, is applied to extract the equivalent inductances of the bondwires. A DC bondwire in Fig. 5.3 has a length of 1.3 mm and produces a parasitic inductance of 1.5 nH. Since the biasing network is designed based on the pMOS current mirror, the parasitic inductances, which are produced from DC bondwires, seldom influences the frequency response. However, the parasitic inductances, originates from the RF and ground bondwires, substantially affect



(a)



(b)

Fig. 5.3 (a) Architecture of the COB package and the test module. (b) Complete COB package and the test module.

the frequency response, and need to be characterized. Fig. 5.4 shows the equivalent circuit of the proposed CMOS TL-based active BPF, including the package effect, in which L_{RF} and L_{gnd} represent the inductances of the bondwires at two RF ports and the ground of the monolithic filter. L_{RF}, which is generated from a RF bondwire with a

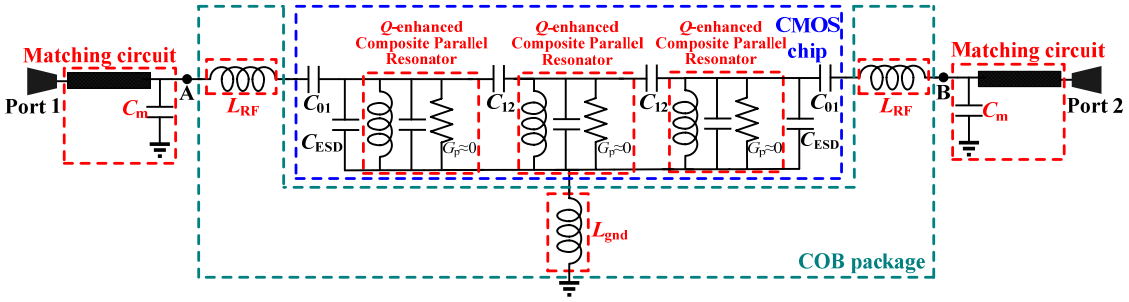


Fig. 5.4 Equivalent circuit of the packaged filter in Fig. 5.3 (b).

length of 1.3 mm, is 1.5 nH and degrades the in-band return loss. Thus, the external matching circuit is designed to absorb the L_{RF} in Fig. 5.3. Owing to the lack of ground via holes in the standard CMOS technology, the electrical grounding of the CMOS TL-based active BPF requires wire bonding, which produces the ground parasitic inductance. From the equivalent circuit in Fig. 5.4, the ground parasitic inductor and capacitive characteristic of the composite parallel resonator over resonance cause the series resonance, generating the additional transmission zero above the passband [31] to disturb the deserved stopband suppression. In Fig. 5.3, a ground bondwire has a length of 1.14 mm and generates an inductance of 1.1 nH. Increasing the number of the ground bondwires minimizes the ground parasitic inductance to reduce the impact on the deserved stopband suppression. Thus, in Fig. 5.3 (b), the number of ground bondwires increases up to 32; the total equivalent ground parasitic inductance, L_{gnd}, is produced as 0.072 nH. The extracted inductances are imported into the circuit simulations, performed by using the software, Agilent ADS, for evaluating the package effects on the frequency response. Fig. 5.5 shows the ADS simulation results of the filter design,

including the bondwire inductances, showing the central frequency of 1.546 GHz with an insertion loss of 0 dB. The design of monolithic CMOS active BPF, presented in this chapter, is identical to the one in Chapter 4, except the passband bandwidth and the additional ESD protection. The bandwidth is 3.1% at 1.55 GHz, 61.3% narrower than in Chapter 4.

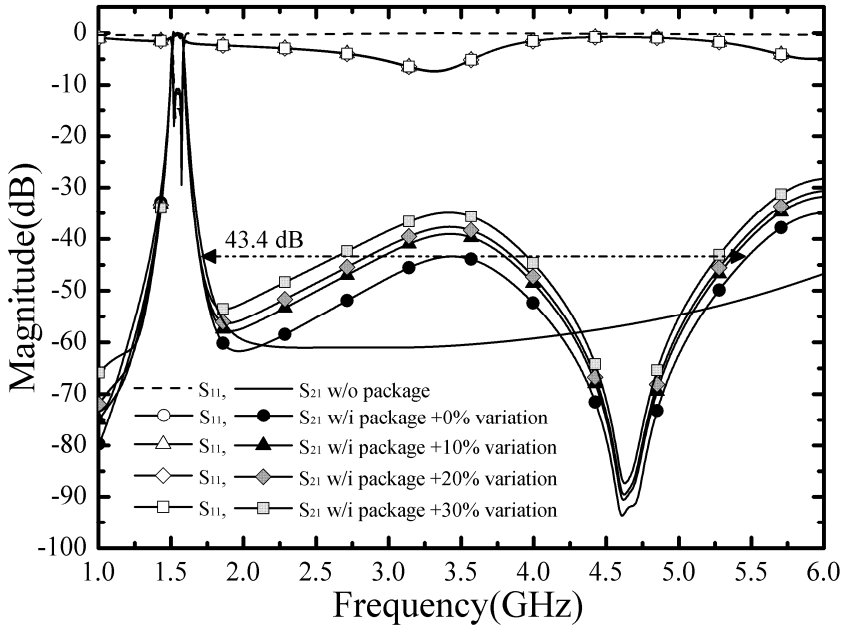


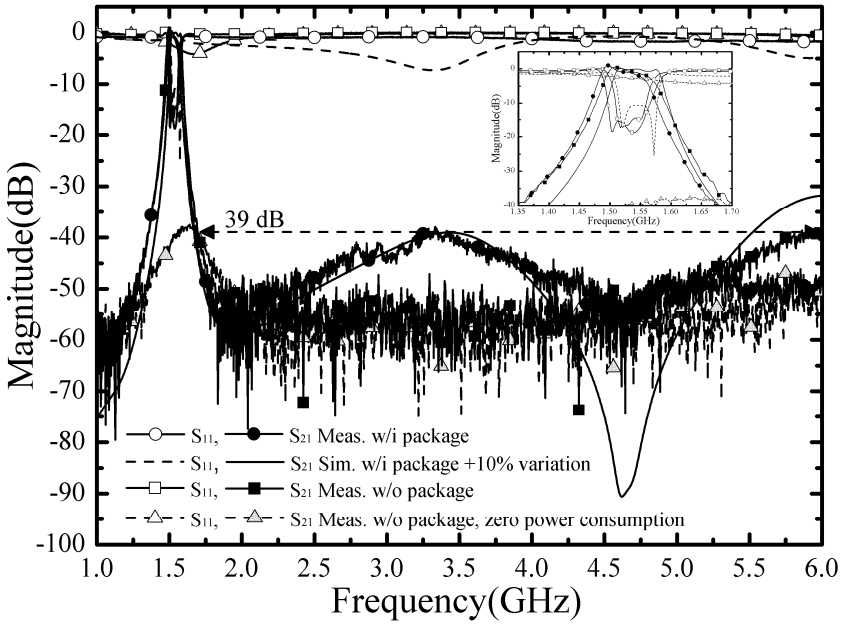
Fig. 5.5. The simulated frequency responses of the CMOS active BPF.

The curves with dots indicate that the ground bondwires cause a transmission zero at 4.61 GHz and disturb the flatness of the frequency response above 2 GHz, compared with the solid curve, which represents the CMOS TL-based active BPF without a package. Additionally, the stopband suppressions at $2f_0$ and $3f_0$ are 46.2 dB and 92.6 dB, respectively. Upper stopband suppression of the prototype in Fig. 5.3 (b) from 1.7 GHz to 5.48 GHz reduces to 43.4 dB, compared with the CMOS TL-based active BPF

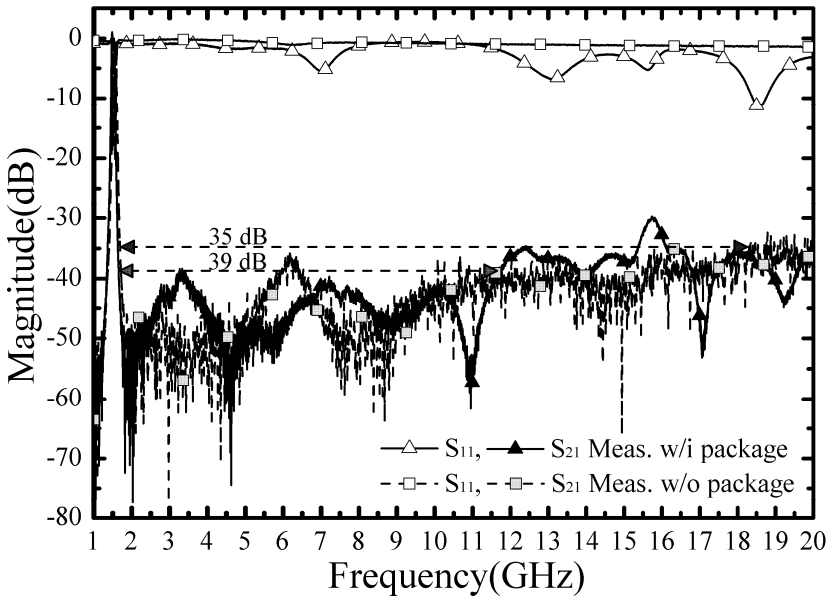
without a package. However, the variation in bondwires is unavoidable in the packaging process, and the inevitable variation in L_{gnd} influences the stopband frequency response of the packaged CMOS TL-based active BPF. As the length per bondwire varies from +10% to +30%, L_{gnd}, which is estimated by HFSS simulations, increases from 0.096 nH to 0.124 nH. The curves with triangles, diamonds and squares in Fig. 5.5 plot the simulated *S*-parameters with variations in length per bondwire from +10% to +30%. According to Fig. 5.5, as the variation in length per bondwire increases from 0% to +30%, the stopband suppressions at $2f_0$ and $3f_0$ are degraded from 46.2 dB to 37.2 dB and from 92.6 dB to 87.2 dB, respectively. Moreover, the upper stopband suppression from 1.7 GHz to 5.48 GHz is decreased from 43.4 dB to 34.9 dB. The curves in Fig. 5.5 show the impact of the variation in bondwires on the stopband suppression, revealing the acceptable tolerance in the package process.

5.3 Measurement and Comparison

On-wafer two-port measured *S*-parameters of the fabricated chip in Fig. 5.1 (b) in the 50-Ω system are obtained using an Agilent E8361C PNA and Picoprobe® un-balanced SG and GS probes. The output power of the PNA is set to -25.0 dBm in the small-signal experiments and short-open-load-through (SOLT) calibration procedures are carried out. The contact pads applied to the RF input/output ports are deembeded.



(a)



(b)

Fig. 5.6. Measured two-port *S*-parameters of the CMOS TL-based active BPF with/without package in 50-Ω system (a) from 1 to 6.0 GHz. (b) from 1 GHz to 20 GHz.

The insertion loss is as high as 37 dB with zero power consumption (V_C and V_{DD} are set to 0 V) in Fig. 5.6 (a). The prototype in Fig. 5.1 (b), including the complete biasing network, consumes 21 mW (7 mA) from a V_{DD} of 3.0 V while V_C is set to 2 V. On-wafer measurement results, represented by the curve with squares in Fig. 5.6 (a),

show 0.98 dB insertion loss at 1.536 GHz and 47.4 MHz (3.1%) 3dB bandwith with 15 dB return loss within the passband. However, the process variation, which makes the change of the parasitic capacitances of the nMOS cross-coupled pairs, produces the drift of the central frequency from 1.55 GHz to 1.536 GHz. The wide-band measurement results, represented by the curves with squares in Fig 5.6 (b), demonstrate the wide upper stopband, extended from $1.1f_0$ to $11.8f_0$ (f_0 is 1.536 GHz), for the suppression level of 35 dB.

The two-port *S*-parameters of the prototype in Fig. 5.3 (b) are measured with Agilent E8364B PNA after SOLT calibration procedures are performed in the 50-Ω system. The output power of the PNA is set to -25 dBm. The prototype in Fig. 5.3 (b) consumes 24 mW (8.0 mA) from a V_{DD} of 3.0 V at a V_C of 2.2 V. Additional 3-mW power (1-mA current) is consumed to compensate for the loss, which is generated from RF bondwires and matching circuits. According to the curves with hollow dots in Fig. 5.6 (a), measurement results agree with the simulation ones with the +10% variation in length per bondwire. The central frequency, f_0, is 1.53 GHz with a 0.95 dB insertion loss, and the 3dB bandwidth is 47.4 MHz (3.1%) with a return loss of 15 dB. Because of the CMOS process variation, the central frequency shifts down from 1.546 GHz to 1.53 GHz. In Fig. 5.6 (a), a transmission zero appears at 4.64 GHz; in addition, the measured stopband suppressions at $2f_0$ and $3f_0$ are 44.57 dB and 52.78 dB, respectively. In Fig. 5.6

(b), the curves with triangles, represents the prototype in Fig. 5.3 (b), shows that upper stopband suppression from $1.08f_0$ to $7.66f_0$ is maintained at higher than 39 dB. Otherwise, the wide upper stopband is extended from $1.09f_0$ to $10.05f_0$, for the suppression level of 35 dB in Fig. 5.6 (b). The capability of Human-Body Model (HBM) ESD protection at RF port under PS and NS modes is tested. The RF port is stressed from 0.25 kV(-0.25 kV) with 0.25 kV increase (decrease) per step, and the prototype in Fig. 5.3 (b) can sustain 0.5 kV in PS mode and -1 kV in NS mode at RF ports.

To evaluate the temperature variable, the prototype in Fig. 5.3 (b) is placed in a programmable temperature chamber, which varies the temperature from -40℃ to +80 ℃ and increases by +20℃. For the temperature characteristic of the semiconductor, under the fixed size, bias voltage and the consumed current, the transistor provides a higher g_m at a low temperature and provides a lower g_m at a high temperature. Therefore, to maintain the insertion loss at a central frequency lower than 1 dB at different temperatures, a larger consumed current is required at a high temperature by increasing V_C; in addition, a lower consumed current is required at a low temperature by decreasing V_C. Table 5.1 summarizes the consumed currents, values of V_C, and central frequencies for the prototype in Fig. 5.3 (b) at different temperatures under constant V_{DD} of 3.0 V. According to this table, during heating from -40℃ to +80℃, the consumed current increases from 4 mA to 13 mA and V_C increases from 1.31 V to 3.78

V. Fig. 5.7 illustrates the measured *S*-parameters for the temperature variation, and the central frequency shifts from 1.587 to 1.479 GHz with a shift rate of -0.9 MHz/℃ from -40℃ to +80℃. The central frequency shift results mainly from the parasitic capacitor, which proportionally varies with the bias voltage of a transistor. Thus, the central frequency shifts down with an increasing V_C.

Table 5.1. Summary of V_C, consumed currents and central frequencies from -40℃ to +80℃.

Temperature (℃)	V_C (V)	Consumed current (mA)	Central frequency (GHz)
+80	3.78	13	1.479
+60	3.05	11	1.496
+40	2.52	9	1.516
+20	2.12	8	1.534
0	1.77	6	1.551
-20	1.54	5	1.568
-40	1.31	4	1.587

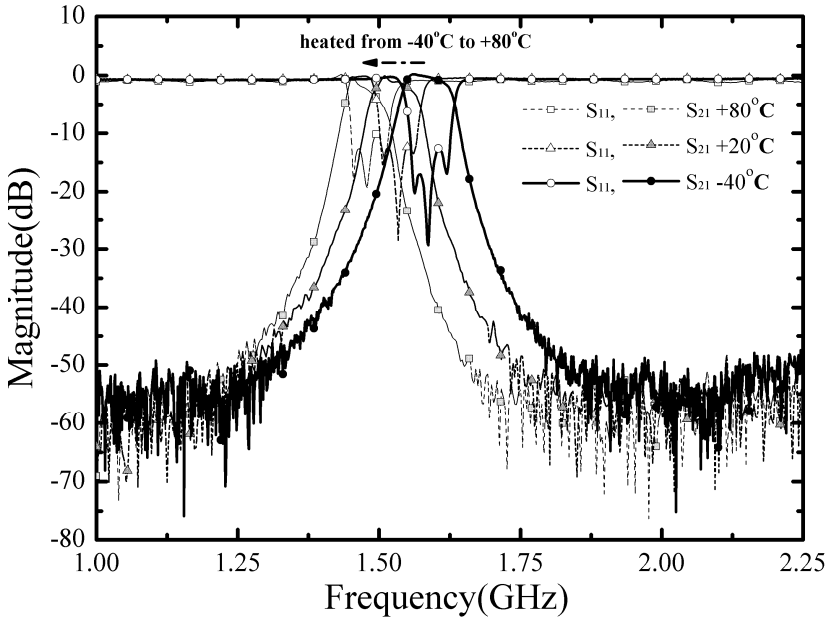


Fig. 5.7. Measured *S*-parameters of the prototype in Fig. 5.3 (b) with the temperature varied ranging from -40℃ to +80℃.

Table 5.2. Comparison of RF monolithic active BPF.

Prototype	[5]	[9]	[10]	[11]	[32]	[33]	This Work
Process	CMOS 0.18 μm	CMOS 0.18 μm	CMOS 0.18 μm	CMOS 0.25 μm	CMOS 0.18 μm	GaAs 1 μm MESFET	CMOS 0.18 μm
Chip area (mm^2)	1.08	0.81	2.25	1.89	0.63	4.96	0.86[#]
f_0 (GHz)	6.02	2.03	2.36	2.14	2.5	2.27	1.53
A_N (%)	4.3×10^{-2}	3.7×10^{-3}	1.4×10^{-2}	9.6×10^{-3}	4.4×10^{-3}	2.8×10^{-2}	2.2×10^{-3}
Order	2	4	3	3	2	3	3
BW (%)	18.9	6.4	2.54	2.8	28	5	3.1
P_D (mW)	5.4 (3mA @1.8V)	16.6 (9.2mA @1.8V)	8.8 (5.84mA @1.5V)	5 (2mA @2.5V)	5.6 (7mA @0.8V)	300[*]	24[*] (8mA @3V)
Type-based	TL	Lump	Lump	Lump	Lump	Lump	TL
Package	w/o	w/o	w/o	w/o	w/o	w/i	w/i
SS (dB) @ $2f_0/3f_0$	22/24	-	-	-	-	>40[*]	44.6/52.8[*]
SS level/ range	20 dB/ $1.36f_0$-$2.18f_0$	-	-	-	-	40 dB[*]/ $1.15f_0$-$4.19f_0$	39 dB[*]/ $1.08f_0$-$7.66f_0$ 35 dB[*]/ $1.09f_0$-$10.05f_0$

*Packaged measurement result [#]Not including bond pads

Table 5.2 summarizes the RF monolithic active BPFs, but the stopband suppression is rarely discussed in the present literature. In Table 5.2, SS means the stopband suppression and A_N is the chip area, which is normalized to the square of the free-space wavelength at the central frequency. The prototype in Fig. 5.3 (b), which is designed based on the transmission, demonstrates the highest stopband suppression at $2f_0$ and $3f_0$, even with the package. Although the prototype in [33] shows the stopband suppression better than 40 dB up to $4.19f_0$, this work can achieve wider stopband from $1.08f_0$ to

7.66f_0 for the suppression level of 39 dB and from 1.09f_0 to 10.05f_0 for the suppression level of 35 dB.

Chapter 6
Conclusions

This dissertation exhibits a comprehensive design of CMOS transmission-line-based (TL-based) active bandpass filter (BPF) from the chip level to the package. In the chip level, highly miniaturized on-chip synthetic TL, loss compensation methodology with minimized passband disturbance and spurious response control to achieve wide stopband suppression are discussed. The package for the proposed monolithic active BPF is presented and the accompanying parasitic effects on the stopband suppression of the packaged active BPF are also investigated. The conclusion and the suggested further research based on this dissertation are summarized as follows.

6.1 Summary

A TL-based active bandpass filter (BPF) is presented in the first part of this dissertation. The utilized technologies include the whorl-forming C-CCS TL, which greatly facilitates the miniaturization of the TL-based active BPF with acceptable performance and an improved active compensating network with the degenerate load to reduce the passband ripple. The relevant theory and design methodology are

comprehensively described. The statistics show that the demonstrated technologies can be used to make the normalized area per resonator (APR) and the normalized 3dB bandwidth over the transmission coefficient (BOT) of the TL-based active BPF, implemented in standard 0.18-μm CMOS 1P6M technology, approach those of the FBAR filters implemented using semiconductor technologies. Experimental results confirm that the passband ripple can be reduced by as much as 76.3% from that of the active compensating network without the degenerate load. Consequently, the presented TL-based active BPF in this dissertation reveals the perspective of monolithic integration in a standard CMOS process.

Additionally, a packaged third-order 1.53 GHz CMOS TL-based active BPF with wide stopband suppression is demonstrated in the second part of this dissertation. A capacitively loaded TL resonator is adopted in the design of packaged CMOS TL-based active BPF to control the spurious responses to achieve wide upper stopband suppression. The monolithic CMOS TL-based active BPF is packaged using the standard COB package and, from the equivalent circuit, increasing the number of ground bondwires the minimizes ground parasitic inductance to reduce the impact on the stopband suppression. Moreover, exactly how varying the length per bondwire affects the upper stopband suppression is analyzed. The measured *S*-parameters, while agreeing with the simulated ones, confirm that packaged CMOS TL-based active BPF

can possess high stopband suppressions of 44.57 dB at $2f_0$ and 52.78 dB at $3f_0$. Moreover, the wide upper stopband is extended from $1.09f_0$ to $10.05f_0$, for the suppression level of 35 dB. Furthermore, how the temperature variation influences the *S*-parameters of the packaged CMOS TL-based active BPF is discussed, in which the central frequency shifts from 1.587 to 1.479 GHz with a shift rate of -0.9 MHz/℃ from -40℃ to +80℃.

6.2 Suggestions for Further Research

In this dissertation, the new C-CCS TL is characterized and compared with the conventional CCS TL based on the two-port *S*-parameters, which is directly extracted from the physical transmission-line structure by the HFSS simulator to obtain the guiding characteristics. In further research, the mode analysis in the cross section can be carried out for more understanding of the new C-CCS TL. Moreover, it is interesting and necessary to develop the equivalent model, which can be directly used in the circuit simulation to reduce laborious full-wave electromagnetic simulation and accelerate the MMIC design. For the CMOS active BPF herein based on C-CCS TL, which assists in miniaturization, the design of frequency-dependent negative conductance results in in-band low insertion loss with good passband flatness and improve the stability. Additionally, good frequency selectivity and wide stopband with high suppression are

accomplished. According to the above mentioned, the perspective of co-design and integration of integrated circuits and BPFs in a standard CMOS process, further meeting the objective of system-on-chip (SoC), is revealed. In further research, the development of on-chip active BPF following LNA is effective to substantially improve noise figure. As mentioned in Chapter 4, appropriate selection the susceptance slope parameter of a composite parallel resonator to reduce the difference in coupling capacitance can achieve linearity improvement. Otherwise, based on all identical coupling capacitances, the requested susceptance slope parameter per composite parallel resonator can be synthesized. Ascribed to temperature-dependent g_m of a transistor, the frequency shift of the monolithic active BPF occurs over the temperature variation, as demonstrated in Chapter 5. Thus, the temperature compensation circuitry is required and integrated in the monolithic active BPF design to minimize the temperature impact. For other design extension, the monolithic active diplexer, which is a case in point, can be developed based on the active BPF design herein.

Appendix

In Chapter 3, the degenerate load, which is equivalent to a parallel resonator as shown in Fig. 3.3 (c), characterizes the $Y_{dd}(f)$ in (3.3) and $Z_{de}(f)$ is obtained in (3.2). Equation (3.2) is substituted into (3.3) to yield (A1), which yields $\mathrm{Re}(Y_{dd}(f))$:

$$\mathrm{Re}(Y_{dd}(f)) = -\frac{g_m}{2}\left(1-\frac{\omega^4 \cdot A+\omega^2 \cdot B+C}{D^2+E^2}\right) \tag{A1}$$

$$A = L_{de}^2 (C_{gs}-C_{ds})^2$$

$$B = L_{de}^2 g_m{}^2 + R_{de}^2 (C_{gs}+C_{ds})^2 - 4R_{de}^2 C_{gs} C_{ds} - 4R_{de} C_{gs} C_{ds} / g_m + R_{de} (C_{gs}+C_{ds})^2 / g_m$$

$$C = R_{de}^2 g_m^2 + R_{de} g_m$$

$$D = 1 + g_m R_{de} - \omega^2 L_{de} (C_{de}+C_{gs}+C_{ds})$$

$$E = \omega (g_m L_{de} + R_{de} (C_{de}+C_{gs}+C_{ds}))$$

In (A1), $\mathrm{Re}(Y_{dd}(f))$ is composed of not only the constant term, $-g_m/2$, but also the term that varies with frequency. Differentiating (A1) yields (A2).

$$\frac{\partial}{\partial f}\mathrm{Re}(Y_{dd}(f)) = -2g_m \pi\omega\left(\frac{\omega^4 L_{de}^2 \cdot F + 2\omega^2 L_{de}^2 \cdot G + H}{(D^2+E^2)^2}\right) \tag{A2}$$

$$\begin{aligned} F = {} & g_m{}^2 L_{de}^2 (C_{de}+2C_{gs})(C_{de}+2C_{ds}) \\ & + 2L_{de}((C_{gs}+C_{ds})^3 + C_{de}(C_{gs}-C_{ds})^2 - 4C_{gs}C_{ds}(C_{gs}+C_{ds})) \\ & + R_{de} C_{de} (C_{gs}+C_{ds})^2 (C_{de}+2(C_{gs}+C_{ds}))/g_m \\ & - 4R_{de} C_{gs} C_{ds} (C_{de}^2 + (C_{gs}+C_{ds})^2)/g_m \\ & + R_{de} (C_{gs}+C_{ds})^4 / g_m - 8R_{de} C_{de} C_{gs} C_{ds} (C_{gs}+C_{ds})/g_m \end{aligned}$$

$$G = -(C_{gs} - C_{ds})^2 + R_{de}^2 g_m^2 (4C_{gs}C_{ds} + C_{de}^2 + 2C_{de}(C_{gs} + C_{ds}))$$
$$+ R_{de} g_m (8C_{gs}C_{ds} - (C_{gs} + C_{ds})^2 + C_{de}^2 + 2C_{de}(C_{gs} + C_{ds}))$$

$$H = -g_m^2 L_{de}^2 + R_{de}^4 g_m^2 (C_{de} + 2C_{gs})(C_{de} + 2C_{ds})$$
$$+ R_{de}^3 g_m ((C_{de} + 2C_{gs})(C_{de} + 2C_{ds}) - 2(C_{gs} - C_{ds})^2)$$
$$- R_{de}^2 (2g_m^2 L_{de}(C_{de} + C_{gs} + C_{ds}) + 3(C_{gs} - C_{ds})^2)$$
$$- R_{de} g_m L_{de} (g_m^2 L_{de} + 2(C_{de} + C_{gs} + C_{ds})) - R_{de}(C_{gs} - C_{de})^2 / g_m$$

The simple design guideline is described as follows. Appropriate g_m, C_{gs} and C_{ds} are produced from the nMOS cross-coupled pair by adjusting the bias voltage, V_D applied to the active compensating network. When the length of the C-CCS TL used in the degenerate load is fixed, L_{de} and R_{de} are known. Then, $Z_{de}(f)$ is a function of C_{de}. By adjusting C_{de} and the bias voltage, V_D, accordingly, the $\mathrm{Re}(Y_{dd}(f))$ in (A1) that cancels $\mathrm{Re}(Y_L(f))$ can be derived and the positive derivative of $\mathrm{Re}(Y_{dd}(f))$ can be obtained and set to approach the derivative of $|\mathrm{Re}(Y_L(f))|$ in (A2). The parasitic capacitance that is provided by the active compensating network is deducted from C_{TL} in the TL-based resonator in Fig. 3.3 (c).

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