# 國立臺灣大學電機資訊學院光電工程學研究所

# 碩士論文

Graduate Institute of Photonics and Optoelectronics

College of Electrical Engineering and Computer Science

National Taiwan University

Master Thesis

二硫化鉬及二硫化鎢傳輸特性及其電晶體之研究
Studies of Materials and Transport Properties of
MoS<sub>2</sub> and WS<sub>2</sub> Based Transistors

陳品方

Pin-Fang Chen

指導教授:吳育任 博士

Advisor: Yuh-Renn Wu, Ph.D.

中華民國 110 年 07 月 July 2021

# 國立臺灣大學碩士學位論文 口試委員會審定書

二硫化鉬及二硫化鎢傳輸特性及其電晶體之研 究

Studies of Materials and Transport Properties of MoS2 and WS2 Based Transistors

本論文係陳品方君(學號 R08941028)在國立臺灣大學 光電工程學研究所完成之碩士學位論文,於民國 110 年 7 月 30 日承下列考試委員審查通過及口試及格,特此證明

中試委員:
(指導教授)

吳肇欣 (指導教授)

3長 3 稿

所長 黄建璋

### 致謝

從大學到碩士班這一路最感謝的便是我的指導教授吳育任教授。從大二下的固態電子學與老師結識,當時我正在為將來的走向而疑惑,好像在 ICS/CS 為顯學的時代,我又不太會電子學,也不會寫程式,研究要往哪裡去真的令人疑惑。還好那時突然腦袋撞到去加簽了固態電子學(我整個大學只加簽了這一門課),老師上課時很認真地講述著元件物理,甚麼 Conduction band 及 Valence Band 的,那能帶的變化搞得我頭很暈,但回去把書念一念又覺得很有成就感,便決定找吳老師做專題。找吳老師會談前,還有去老師的個人網頁看看,好像是做 LED 的,但腦袋也沒很清楚實際要做甚麼。找老師後,變成為老師的專題生,也才花了更多時間去理解固態物理、半導體物理。現在回想起來,覺得自己很矛盾,畢竟從大一計算機程式之後,我就決定我不要在寫程式,但不知幾時開始寫程式卻成為了自己專業的一部分,雖然不特別好,但卻堪用也持續在進步,多虧了這幾年的練習及老師的指導。老師一直教的是做事的方法,怎麼去很扎實地去處理問題、解決問題,也讓我有信心,即使未來脫離了我自己的領域,我也有機會繼續以扎實的態度去解決問題,真的很感謝老師的培育。

再來感謝的是蔡宗印學長。以前我們合作處理計畫時,學長總是處理的特別多,默默幫我扛下不少壓力,還教我怎麼處理很多的程式問題、基本物理及怎麼畫圖。在我當專題生時,我跟他合作總是偷懶,他也總是笑一笑,只能說我運氣不錯。此外,很感謝黃雋宇學長,雖然他與我的研究上並沒有直接的關聯,但他常與我們討論問題,並提出可行的方式,建議我們嘗試。還要感謝幾位已經步入職場的學長,當專題生的幾年有一起共事一起學習,還記得那時常與林稚皓學長一同在實驗室窩到頗晚。

還有我的幾位同學,從碩一進來的時候就一同在實驗室討論問題,一同成長,並互相督促。直到口試前,大家還是一起約時間練習報告,總是持續的一起進步,這也是碩士生涯能大大收穫的原因之一,因為有著很好的同儕。

最後,也很感謝臺積電技術經理 Edward,經理從去年十月我報告完蒙地卡羅開始,並一個月跟我 meeting 一次,雖然頗有壓力,但經理提出的意見很專業,因此讓我的研究與實際實驗有了更好的連結,並更透徹地去理解二維元件。

碩士兩年,再吳老師實驗室三年多,回首,自己成長很多,只能說自己也很幸運吧,從家庭、老師、朋友等等都是自己成長的養分。所以這本論文能完成, 要感謝的人真的很多,也很慶幸自己是個幸運的人。

# 中文摘要

本研究以蒙地卡羅法討論二硫化鉬以及二硫化鎢的傳輸特性,經模擬後得知二硫 化鉬及二硫化鎢的電子遷移率分別為  $171 \text{ cm}^2/\text{V-s}$  及  $83 \text{ cm}^2/\text{V-s}$ 。此外,能帶中, K 能谷以及Q能谷間的能量差是影響材料傳輸特性的重要因素。但若將二維材料周 圍以高介電係數材料包覆,遠程聲子散射將會成為最重要降低材料速度的因子。 我們將討論完的材料特性帶入二維奈米片電晶體討論元件特性。材料、閘極長度、 電極交疊區域、介電層以及電子摻雜將被討論。我們發現相較於二硫化鎢,二硫 化鉬會是較好的通道材料。至於介電層,因三氧化二鋁較二氧化鉿有較低的遠程 聲子散射,會是較好的介電層材料。電極交疊區域縮短以及摻雜能給電流帶來正 面的效應。至於閘極長度的選擇,則要在縮短閘極的好處以及閘極控制力下降間 來選擇。在眾多的參數間進行優化後,我們設計出一電晶體,其閘極長度七奈米, 電極交疊區域一奈米,介電層為等效氧化層厚度 0.8 奈米之氧化鋁以及電子摻雜 為  $4\times10^{13}$  cm<sup>-2</sup>。此電晶體在操作電壓 0.65 伏以及截止電流為  $1\times10^{-4}$   $\mu$  A/ $\mu$ m 下, 開路電流可達  $495~\mu$  A/ $\mu$ m,符合國際半導體技術發展藍圖於 2022 年對電流之要 求。此外,其亦展現出良好的閘極控制能力。

關鍵字:二維材料、二硫化鉬、二硫化鎢、蒙地卡羅法、二維材料奈米片電晶體



# **English Abstract**

Transport properties of MoS<sub>2</sub> and WS<sub>2</sub> are investigated by the Monte Carlo method. Intrinsic mobilities of MoS<sub>2</sub> and WS<sub>2</sub> are 171 cm<sup>2</sup>/V-s and 83 cm<sup>2</sup>/V-s. Besides, for the free-standing MoS<sub>2</sub> and WS<sub>2</sub>, the valley energy separation between the K and Q valley is the critical factor influencing transport. However, if 2D materials are stacked in high- $\kappa$  materials, remote phonon scattering becomes the most important scattering mechanism and degrades the performance of the material very much. In addition, 2D nanosheet transistors are discussed. Effects of the materials, the gate length ( $L_G$ ), the length of the underlap region ( $L_{un}$ ), dielectrics, and doping are studied. We found out MoS<sub>2</sub> is more suitable for the channel material. As for the dielectric, Al<sub>2</sub>O<sub>3</sub> is better than HfO<sub>2</sub> due to the weak remote phonon scattering.  $L_{un}$  and doping can bring positive effects on on-current  $(I_{on})$ . The selection of  $L_G$ is a trade-off between shrinking and gate control. After optimization, maximum I<sub>on</sub> happens at  $L_G$ =7nm,  $L_{un}$ =1nm, 0.8nm EOT of  $Al_2O_3$  dielectric and n-type doping of  $4\times10^{13}~\text{cm}^{-2}$ .  $I_{on}$  can reach 495  $\mu\text{A}/\mu\text{m}$  when the supply voltage is 0.65Vand off-current is  $\times 10^{-4} \ \mu\text{A}/\mu\text{m}$ , meeting the requirement of 2022 International Roadmap for Devices and Systems. Furthermore, it also demonstrates good gate

# English Abstract

control and electrostatics.

Keywords: 2D material, MoS<sub>2</sub>, WS<sub>2</sub>, Monte Carlo Method, 2D nanosheet

transistor



# **Contents**

Ve	erifica	tion Letter	i
A	cknow	vledgement	ii
CI	ninese	Abstract	iii
Eı	nglish	Abstract	iv
Li	st of l	Figures	ix
Li	st of T	Tables	xvi
1	Intr	oduction	1
	1.1	Overview of Two-dimensional Materials	1
	1.2	Introduction and Applications of TMD Materials	2
	1.3	Simulation of the Transport Properties	6
	1.4	$MoS_2$ and $WS_2$ FET	9
	1.5	Gate-All-Around Nanosheet Transistor	10
	1.6	International Roadmap for Devices and Systems	12

N Tr		B TF	$\mathbf{n}$
	<i>- L</i>	N 1	
' I N .	1 1 2	1 N 1	.,
	N'	NTE.	NTEN'

vii

2	Met	hodolog	sy · C · C	15
	2.1	Overvi	ew	15
	2.2	Scatter	ring Mechanism and Scattering Rate	15
		2.2.1	Acoustic Phonon Scattering	17
		2.2.2	Optical Phonon: Deformation Potential Scattering	18
		2.2.3	Intervalley Phonon Scattering	19
		2.2.4	Remote Phonon Scattering	20
	2.3	Multi-	valley Monte Carlo Method	22
		2.3.1	Monte Carlo Method	22
		2.3.2	Multi-valley and non-parabolic band conditions	25
		2.3.3	Transient Transport Calculation	26
	2.4	Monte	Carlo, Poisson and Drift-Diffusion Model	27
		2.4.1	Poisson and Drift-Diffusion Model	27
		2.4.2	Monte Carlo, Poisson and Drift-Diffusion Model	28
		2.4.3	Two Dimensional Poisson, Drift-Diffusion, and Schrodinger	
			Solver	29
3	Trai	ısport F	Properties of $MoS_2$ and $WS_2$	31
	3.1	•	iew	31
	3.2	Band s	structure	32
		3.2.1	Band structure by DFT	32
		3.2.2	Band structure fitting	33
	3 3	Intrine	ic Flectrical Transport Properties	34

CC	CONTENTS		
	3.4	Extrinsic Transport Properties	39
			。學
4	MoS	S <sub>2</sub> and WS <sub>2</sub> Based Transistor	44
	4.1	Structures and Simulation Model of 2D Nanosheet Transistors	44
	4.2	Comparision of Symmetrical and Asymmetrical Gate	48
	4.3	Effect of Dielectric	53
	4.4	Effect of $L_{un}$	55
	4.5	Effect of Doping	57
	4.6	Benchmark	61
5	Con	clusion and Future Work	63
Re	Reference		67
Ap	pend	ices	85
A	Defo	ormation potential constants for $\mathbf{MoS}_2$ and $\mathbf{WS}_2$	86



# **List of Figures**

1.1	The current density and the SS value from the experimental litera-	
	ture. The blue circles, A1 to A7, represent the datas of the $MoS_2$	
	FETs [1, 2, 3, 4, 5, 6, 7] and the red squares, B1 to B3, represent	
	the datas of the WS $_2$ FETs [8, 9, 10]	9
1.2	Evolution of the FET structure. (From Samsung website)	10
1.3	(a) $I_D$ - $V_G$ transfer curves and (b) cross-section of the IBM and	
	Samsung nanosheet GAA transistor	11
1.4	Cross section of the nanosheet FETs of IBM 2nm chip. (Figure	
	comes from IBM website)	12
1.5	Scaling of the standard cell [11]	12
2.1	(a) Schematic diagram of lattice vibration of acoustic phonon and	
	optical phonon (b) Phonon dispersion of MoS <sub>2</sub>	18

2.2	intervalley phonon scattering process in Mos <sub>2</sub> . Electrons can	A
	scatter from K valley to satellite Q valleys by absorbing or emitting	
	phonon. As electrons get higher energy, they are much easier to	
	have the K-to-Q intervalley phonon scattering	20
2.3	Schematic diagram of carrier transport in material	23
2.4	Flow chart of Monte Carlo method	24
2.5	(a)K valleys and Q valleys in the first Brillouin zone. (b)Intervalley	
	scattering from K valleys to neighboring K' valleys and satellite	
	Q valleys. In figure(a), there is one K valley and a symmetrical	
	K-like valley, K' valley, and six Q valleys in the first Brillouin zone.	
	The lowest conduction band is located in either K or K' valley. In	
	figure(b), the green and blue lines represent the K-to-Q inter-valley	
	scattering mechanism. The red line represents K-to-K' inter-valley	
	scattering mechanism.	26
2.6	Flow chart of the Monte Carlo, Poisson and Drift-Diffusion Model.	29
3.1	(a) Band structure of $MoS_2$ . (b) Band structure of $WS_2$	33
3.2	(a) Fitting of K valley in $MoS_2$ . (b) Fitting of Q valley in $MoS_2$ .	
	Blue lines represent the original data from the band structures, and	
	red lines are fitting curves of the E-K relation with non-parabolic	
	Eq. (2.14) or Eq. (2.15)	34

3.3	(a) Fitting of K valley in $WS_2$ . (b) Fitting of Q valley in $WS_2$ . Blue	-
	lines represent origin data from band structures, and red lines are	33
	fitting curves of E-K relation with non-parabolic Eq. 2.14 and Eq.	97079
	2.15	35
3.4	Electron-phonon scattering rates in MoS <sub>2</sub> via (a) emission and	
	(b) absorption of phonons calculated at room temperature. The	
	orange and purple lines represent acoustic phonon scattering rate	
	and optical deformation potential phonon scattering rate. The	
	green and blue lines represent intervalley scattering rates caused	
	by acoustic phonon and optical deformation potential phonon. The	
	red line indicates the total scattering rates of all mechanisms	36
3.5	Electron-phonon scattering rates in WS <sub>2</sub> via (a) emission and (b)	
	absorption of phonons calculated at room temperature	37
3.6	(a) Field-dependent mobilities and (b) field-dependent velocities	
	are shown. The red lines represent the intrinsic transport proper-	
	ties of MoS <sub>2</sub> , and the blue lines represent the intrinsic transport	
	properties of $WS_2$	38

3.1	(a) Average electron potential energy and (b) total scattering rates	
	of both MoS <sub>2</sub> and WS <sub>2</sub> . The average electron energy of WS <sub>2</sub> under	學
	low field is 0.039 eV and higher than $\Delta E_{KQ}$ . The corresponding	
	scattering rate of WS $_2$ in (b) is $5.4 \times 10^{13}~\text{s}^{-1}$ . The average electron	
	energy of MoS <sub>2</sub> under low field is 0.036 eV and higher than $\Delta E_{\mathit{KQ}}$ .	
	The corresponding scattering rate of $MoS_2$ in (b) is $1.1 \times 10^{13}$ s <sup>-1</sup> .	40
3.8	Remote phonon scattering rates of MoS <sub>2</sub> stacked into the different	
	dielectric at the K valley.	42
3.9	(a) Field-dependent mobilities and (b) field-dependent velocities of	
	MoS <sub>2</sub> with different dielectrics are shown. If MoS <sub>2</sub> are surrounded	
	by hBN or SiO <sub>2</sub> , remote phonon scattering has no prominent effect	
	on the electron transport properties. However, with $Al_2O_3$ or $HfO_2$	
	surrounding $MoS_2$ , mobilities are degraded a lot	43
3.10	(a) Field-dependent mobilities, and (b) field-dependent velocities	
	of $WS_2$ with different dielectrics.	43
4.1	Illustration of the $MoS_2$ nanosheet transistor structure	45
4.2	Illustration of asymmetrical MoS <sub>2</sub> nanosheet transistor structure.	45
4.3	Leakage current density vs. equivalent oxide thickness for different	
	dielectrics (Lo [12], Guha [13], Gusev [14], Britnell [15])	47
4.4	(a) $I_{DS}$ - $V_G$ transfer characteristics for the symmetrical $MoS_2$ nanosheet	
	transistor at $L_G$ =5 nm. (b) $I_{DS}$ - $V_{DS}$ output characteristics for the	
	symmetrical MoS <sub>2</sub> transistor at $L_G$ =5 nm	48

xii

4.5	(a) $I_{DS}$ - $V_G$ transfer characteristics for the asymmetrical $MoS_2$	A
	nanosheet transistor at $L_G$ =5nm. (b) $I_{DS}$ - $V_{DS}$ output characteris-	91
	tics for the asymmetrical $MoS_2$ nanosheet transistor at $L_G$ =5nm.	970191
		49
4.6	Transfer characteristics for the (a-d) ${\rm MoS}_2$ nanosheet transistor	
	with $L_G$ =5, 7, 12, 14nm. Transistors are operated at $V_{\it DD}$ =0.65V	
	and $I_{off}$ =1×10 <sup>-4</sup> $\mu$ A/ $\mu$ m following the IRDS	50
4.7	(a) The average of the electron density in the $MoS_2$ membrane. (b)	
	$R_c$ vs. the gate bias	51
4.8	(a) Subthreshold swing SS at $V_{\it DS}$ =0.65V as a function of $L_{\it G}$	
	and (b) DIBL at $I_{off}$ =1×10 <sup>-4</sup> $\mu$ A/ $\mu$ m as a function of $L_G$ for	
	symmetrical and asymmetrical $MoS_2$ nanosheet structure	52
4.9	Comparison of the performance of the transistors with different	
	structures, materials, and $L_G$	52
4.10	${\rm I}_{DS} ext{-}{ m V}_G$ transfer characteristics of the asymmetrical ${ m MoS}_2$ nanosheet	
	transistors with (a) $Al_2O_3$ and (b) $HfO_2$ dielectric	54
4.11	Comparison of the performance of the transistors with (a) $Al_2O_3$	
	and (b) HfO <sub>2</sub> dielectric. Al <sub>2</sub> O <sub>3</sub> dielectric demonstrates better per-	
	formance	55

4.12	Transfer characteristics of transistors with (a) $L_G$ =5nm, (b) $L_G$ =7nm,	A
	(c) $L_G$ =12nm and (d) $L_G$ =14nm. With longer $L_G$ , transistors	H. H.
	demonstrate better gate control. With shorter $L_u n$ , $I_{on}$ increases	
	but gate control degrades	56
4.13	(a) DIBL as a function of $L_G$ . (b) Conduction bands of the channels	
	in the transistor with $L_G$ =5 nm (solid line) and $L_G$ =14nm (dotted	
	line)	57
4.14	Comparison of the performance of the transistors with $L_{un}=1, 3,$	
	5, and 7nm and $L_G$ =5, 7, 10, 12, and 14nm. The transistors are	
	operated at $V_{DD}$ =0.65V and $I_{off}$ =1×10 <sup>-4</sup> $\mu$ A/ $\mu$ m and 0.8nm EOT	
	$Al_2O_3$ dielectric is used	58
4.15	Illustration of the $AlO_x$ doped $MoS_2$ nanosheet transistor	59
4.16	Linear relation between the doping concentration of $\mathrm{AlO}_x$ and the	
	induced eletron concentration of MoS <sub>2</sub> . The black dots are the	
	doping concentrations to be investigated	59
4.17	(a) Comparison of the transfer characteristics of the transistros	
	with $L_G$ =5nm, $L_{un}$ =1nm, and different concentrations of $MoS_2$	
	doping. (b) Comparison of $I_{on}$ and SS of transistors with different	
	doping concentrations at $I_{off}$ =1×10 <sup>-4</sup> $\mu$ A/ $\mu$ m and $V_{DD}$ =0.65V.	
	In figure(b), doping concentrations are gradually increasing from	
	the bottom point to the top point	60

LIST OF FIGURES xv

4.18	Benchmarks of (a) DIBL vs. $L_G$ and (b) $I_{DS}$ vs. SS value for Si
	GAA FETs. Only this work is the MoS <sub>2</sub> nanosheet transistor. The
	data from this work is labeled by the blue stars. The blue star in (b)
	is the best $I_{on}$ in this work. Label A to J corresponds to references
	[16, 17, 18, 19, 20, 21, 22, 23, 24, 25], respectively 62



# **List of Tables**

1.1	Intrinsic electron mobility of $MoS_2$ and $WS_2$ from the literatures .	7
1.2	IRDS roadmap (V $_{TH,sat}$ and I $_{on}$ are set at I $_{off}$ =100 pA/ $\mu$ m) [11] $$ .	13
3.1	Fundamental parameters of $MoS_2$ and $WS_2$ from DFT $\ \ldots \ \ldots$	33
3.2	Fitted effective mass and non-parabolic parameter, $\alpha$ of K and Q	
	valleys in $MoS_2$ and $WS_2$	34
3.3	Remote phonon modes for different dielectric materials. $\epsilon_r^o,\epsilon_r^i$ and	
	$\epsilon_r^{\infty}$ are low-frequency, intermediate and high-frequency permittivi-	
	ties, respectively.	41
4.1	Parameter settings for nanosheet transistors	46
<b>A</b> .1	Deformation potential constants for electron-phonon interaction in	
	the conduction band of K and Q valleys	87
A.2	Deformation potential constants for electron-phonon interaction in	
	the conduction band of K and Q valleys	88



# Chapter 1

# Introduction

### 1.1 Overview of Two-dimensional Materials

Two-dimensional (2D) materials are materials that can exist in a stable monolayer. Nowadays, 2D materials have caught a lot of attention and been widely researched for more than ten years. The first 2D material, graphene, was discovered in 2004 [26]. Besides the advantage of thickness, it also has unique electronic and optoelectronic properties. In electronic properties, graphene has mobility of up to  $1 \times 10^6$  cm<sup>2</sup>/V-s and Dirac cone, which is ideal for applications of transistors or electrodes [27, 28]. As for optoelectronic properties, it is ideal for transparent electrodes to replace ITO due to their thickness of one atom. In addition, graphene can also provide many functions in photovoltaic devices like transparent contacts, a channel for charge transport, and catalysts [29]. When putting lots of efforts to exploit graphene, people also began to look for other 2D materials, like graphene-

like silicene, black phosphorus, hBN, Transition Metal Dichalcogenides (TMD) materials (e.g., MoS<sub>2</sub>, PtSe<sub>2</sub>), and other Dichalcogenides (e.g., SnS<sub>2</sub>, SnSe<sub>2</sub>).

# 1.2 Introduction and Applications of TMD Materials

Although graphene is a good conductor, it has a limit of zero bandgaps to make transistors and specific optoelectronic devices. As a result, TMD materials are getting more popular. TMD materials have the composition of MX<sub>2</sub> (M=transition metal, X=S, Se, and Te) and have different structural phases. Unlike zero-bandgap graphene, TMD materials provide a wide range of bandgaps from metallic ones to semiconductors and electron affinities [30, 31], offering much more opportunities to design various kinds of electronic and optoelectronic devices.

Some TMD materials have bandgaps in the infrared and visible ranges, suitable for optic and optoelectronic applications [32]. To make optoelectronics, some researchers explored the optical and optoelectronic properties of TMD materials. Chen, S. F. calculated the absorption rate of MoS<sub>2</sub> and presented an idea of an intermediate band solar cell [33]. There are also papers exploring the possibilities of using TMD materials in gas sensors and photodetectors [34, 35]. Huo, Nengjie, et al. revealed that multilayer WS<sub>2</sub> nanoflake has high photosensitive characteristics. It also has different charge transfer phenomena between it and different gas molecules. The phenomena cause different photoelectrical properties in different gas environments. These properties provide the potential for gas sensors and photodetectors [36]. As for MoS<sub>2</sub>, its photoresponse is relatively slow due to O and

H<sub>2</sub>O vacancies on the surface of MoS<sub>2</sub>. Its photocurrent increases fast but decays very slow. However, by proper encapsulation, the photoresponse time can be under 10 ms [35]. Unlike n-type MoS<sub>2</sub> and WS<sub>2</sub>, WSe<sub>2</sub> exhibits n-type and p-type depending on metals' work functions and also has a fast response time of 20 ms [35]. The examples mentioned above demonstrate the potential for optoelectronic applications in the future.

In addition, as the gate length  $(L_G)$  of silicon-based transistors goes under 20 nm, severe short channel effect has become an important factor to limit scaling down of  $L_G$ . It causes direct source-to-drain tunneling current and degrades gate control. It is known that heavier effective mass, larger bandgap, and lower inplane dielectric can lower the influence of tunneling current. Fortunately, some TMD materials, like  $\epsilon_{MoS2} = 4$ , have lower in-plane dielectric constants. MoS<sub>2</sub> also has an effective mass of 0.5 and a bandgap around 1.8 eV. For the reasons mentioned above, MoS<sub>2</sub> is expected to have better performance of suppression of off-state leakage current and is seen as a candidate for the next-generation transistor [37, 38, 39]. Nowadays, negative capacitance field-effect transistors (NCFETs) with  $MoS_2$  have been proposed in researches. NCFETs use  $HfZrO_2$  and  $AlO_x$  as gate dielectric and MoS<sub>2</sub> as the channel. NCFETs show great immunity to short channel effect even in the sub-5-nm device [38]. Due to the improved gate control caused by the ultrathin body, NCFETs demonstrate ultra-low subthreshold swing (SS) value of 23 mV/dec, sub 60 mV/dec over six orders of I<sub>d</sub> modulation, on/off ratio as high as  $10^9$ , and gate leakage current of  $1 \times 10^{-13}$  A/ $\mu$ m [40]. Even under

a switching frequency of 10 kHz, they show hysteresis-free steep switching and SS value of sub 60 mV/dec [40]. Although NCFETs still have lots of challenges, they show great potential for scaling and ultra-low power applications.

TMD materials have also been widely used in other electronic devices. For example, MoS<sub>2</sub> is used as the field-effect transistor driving HfO<sub>2</sub> oxygen vacancies or hBN RRAM in 1T1R configuration or 1T-nR configuration. Due to the larger bandgap of monolayer MoS<sub>2</sub>, it increases the resistance of RRAM and then lowers off-state leakage current. Besides, it is so thin that nanoscale vias can be used to connect FETs in different memory layers, which is suitable for 3D monolithic integration. Low-temperature fabrication is also an advantage. The whole fabricated temperature is below 200°C [41, 42]. MoS<sub>2</sub> is also suitable for flexible nanoelectronics. It was deposited on commercially available paper substrates as a transistor channel. It demonstrated a high on/off ratio of 10<sup>9</sup>, mobility of 6 cm<sup>2</sup>/V-s, and durability of more than 10000 times of bending of 0.6 % strain [4]. With the advantage of the ultrathin body, TMD materials have been widely applied on not only NCFET but also large varieties of electronic devices. Besides devices, people try to integrate devices into a circiut. Li, Jiayi, et al. integrated two surface channel (TSC) transistors into 2T2R SRAM. Because TSC transistors can present AND or OR logic, and the the original 6T SRAM can be simplified to be 2T2R SRAM. The SRAM also had stable read/write ability, showing feasibility in the future [43].

Besides, because of the complement properties of TMD materials and graphene, they can be combined into heterostructures to extract advantages of both materials.

In this way, it is also possible to produce all-2D devices. At the same time, because of weak van der Waal bonds, heterostructures can skip the lattice mismatch problem [44]. Kim, Taesoo, et al. has used graphene/MoS<sub>2</sub> heterostructure in junction field-effect transistors (JFET). Because of the bandgap of MoS<sub>2</sub>, there is a Schottky barrier height between the interface of the heterostructure. By modulating the Fermi level of graphene, effective Schottky barrier height is modulated and then activates current transport in the graphene channel. With a bandgap of MoS and excellent mobility of graphene, mobility of 100 cm<sup>2</sup>/V-s and on/off ratio of 10<sup>8</sup> are measured in the JFET [45]. Up to now, heterostructure is still a popular topic to be explored.

In the early stage of researches, mechanical exfoliation was the most used approach to investigate properties of 2D materials. By mechanical exfoliation, monolayer 2D material is isolated from the bulk material with high-quality crystal. In addition, Huang, Yuan, et al. said the exfoliated area could be 20-60 times larger than the area in established exfoliation methods [46] with the addition of heat treatment. However, for the application of devices, large-scale synthesis methods with high quality, good uniformity, and high yield are necessary. So far, chemical vapor deposition (CVD) methods are commonly used because of their relative simplicity, diversity of precursors and fast growth rate [47]. Many papers have reported processes of growth of large-scale TMD materials through CVD. In 2012, Liu, Keng-Ku, et al. dip-coated (NH<sub>4</sub>)<sub>2</sub>MoS<sub>4</sub> precursor solution on Si/SiO<sub>2</sub> or sapphire substrates, followed by the two steps of high-temperature annealing. The

research showed that substrates and environments of annealing indeed had impacts on crystalline quality [48]. Different from solution-based deposition, others predeposited the metal on Si/SiO<sub>2</sub>. Then, sulfur is exposed to the thin-film metal for sulfurization. The size of the thin film only depends on the size of the substrate. Hence, it is much easier to scale up [49]. There are also papers proposing wafer-scale CVD of monolayer TMD materials. Chen, Jiajun, et al proposed a 2-inch wafer-scale deposition of WS<sub>2</sub> by CVD and thermal evaporation [50]. Xu, Hu, et al. introduced multilayer layer MoS<sub>2</sub> islands to improve the quality of crystal and fabricated FET arrays with mobility of 70 cm<sup>2</sup>/V-s [51]. Many groups are still devoted to pursuing high-quality crystals. However, measured mobility of TMD in large-scale deposition and performance of devices is still under simulation's prediction [52]. One of the major reasons is the high density of defects in the crystal [50].

# 1.3 Simulation of the Transport Properties

Because high defect density suppresses the performance of devices, we still need better growth methods. Besides, real performances of TMD devices are still needed to be known. By simulation, we can evaluate the theoretical properties of TMD materials and understand the upper limit of devices. Table 1.1 shows the intrinsic mobility of the commonly-seen TMD materials, MoS<sub>2</sub> and WS<sub>2</sub> from the simulation and the experiment. There are two characteristics in table 1.1. Firstly, as the previous section said, the mobilities from the simulation are generally larger

Table 1.1: Intrinsic electron mobility of MoS<sub>2</sub> and WS<sub>2</sub> from the literatures

Material	Simulation $\mu_e$ (cm <sup>2</sup> /V-s)	Experimental $\mu_e$ (cm <sup>2</sup> /V-s)
$MoS_2$	130 [53], 144 [54], 150 [55],	28 [37], 56 [56],
	250 [57], 284 [58]	70 [51],150 [59]
$\mathbf{WS}_2$	37 [60], 60 [54] , 320 [52],	20 [61], 44 [62], 83 [63]
	357 [58], 767 [60]	

than that from the experiments. The characteristic comes from the high defect density in the crystal. Therefore, if we don't want the device performance to be affected by the defects, we should build the simulation model to get the real transport properties. Secondly, there are obvious differences in the mobilities from the different simulation literature. Hence, at the same time, we need to realize the critical factor influencing the transport by the simulation. Understanding the factor could provide some approaches to enhance the device performance in the future.

Some approaches can simulate electrical properties of materials, like the Boltzmann transport equation (BTE) and Monte Carlo method [64]. Firstly, BTE describes the distribution function of electrons under external perturbation. Under consideration of carrier diffusion, applied fields, and scattering, the distribution function will go steady. In the end, using relaxation time approximation, transport properties, like mobility, conductivity, or diffusion constants, under an electric field of 1 kV/cm can be calculated. Many papers have used this to calculate the low-field mobility and proved that charged impurities limit currently reported mobility in

experiments [65]. Secondly, the Monte Carlo method is a numerical method that repeats random number sampling to simulate the phenomena, which are naturally probabilistic problems. When carriers transport materials, the process is also probabilistic. The whole transport contains a series of free flight and scattering events. In the simulation process, we need to select events according to probability repeatedly until the stop criteria appear. More details of how to select events are discussed in chapter 2. In the Monte Carlo Method, we can exert different electric fields to observe the flight and velocities without the limit of the low electric field. Therefore, we can extract high-field flight and saturation velocity by the approach. As devices scale down, electric fields in devices, especially transistors, are easy to be over 1 kV/cm. Hence, in the thesis, the Monte Caro method is used to calculate the transport properties of MoS<sub>2</sub> and WS<sub>2</sub>, such as mobility and saturation velocity. The results are discussed in chapter 3. When we simulate transport properties in materials, the scattering rate is of much importance. In the thesis, we use Fermi golden rule to calculate the scattering rate. Only by accurately estimating the scattering rate can we accurately calculate transport properties. More details of the calculation are discussed in chapter 2, and results are presented in chapter 3. After we know the transport properties of MoS<sub>2</sub> and WS<sub>2</sub>, those parameters and the Monte Carlo model can be put into Poisson, Drift-Diffusion, and Schrodinger Solver (DDCC) developed by our lab to discuss devices.

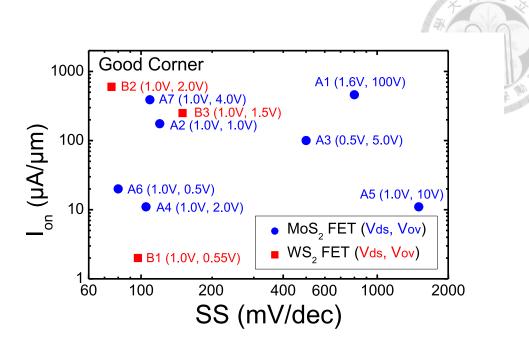


Figure 1.1: The current density and the SS value from the experimental literature. The blue circles, A1 to A7, represent the datas of the MoS<sub>2</sub> FETs [1, 2, 3, 4, 5, 6, 7] and the red squares, B1 to B3, represent the datas of the WS<sub>2</sub> FETs [8, 9, 10].

# **1.4** $MoS_2$ and $WS_2$ FET

Nowadays, many researchers are devoted to boosting the performance of the  $MoS_2$  and  $WS_2$  transistors. Figure 1.1 shows the current density and the SS values from the experimental literature. In the experiment, most of the  $V_{ds}$  and the gate drives are greater or equal to 1V to enhance the current. The phenomenon comes from the immature process of the two materials. Because of the immature process, it is hard to scale down the FET and keep the crystal quality good. Therefore, the performances of the  $MoS_2$  and  $WS_2$  FETs are experimentally worse than that of the Si devices. It is hard to know their potential for the next-generation transistors.

Consequently, we use the device simulation to scale down the channel length and neglect the degrading effect from the defects and get the true performance of the  $MoS_2$  and  $WS_2$  FETs in the future.

### 1.5 Gate-All-Around Nanosheet Transistor

Nowadays, with a shorter  $L_G$  in FET, gate control becomes more difficult. Replacing the planar FET, FinFETs are commonly used in chips to enhance gate control. However, when Moore's law goes under 5 nm technology node. Gate control of FinFET is not enough. Therefore, companies and researchers began adopting Gate-All-Around (GAA) or nanosheet FETs. With channel semiconductors surrounded

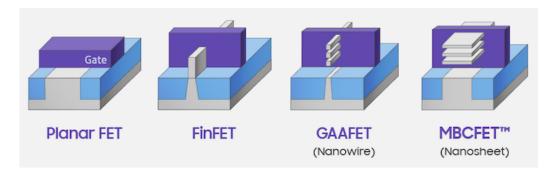


Figure 1.2: Evolution of the FET structure. (From Samsung website)

by gate metal and dielectrics, these new types of FETs can provide better gate control. Figure 1.2 shows the evolution of FETs. In 2017 VLSI, IBM and Samsung published stacked nanosheet GAA transistors. Their SS value and DIBL achieved 75 mV/dec and 32 mV/V at  $L_G$ =12nm [66]. Figure 1.3 shows the  $I_D$ - $V_G$  transfer curves and cross-section view of the stacked nanosheet GAA transistors. Intel also

published 3D-stacked NMOS-on-PMOS nanoribbon transistors in 2020 IEDM [16]. In 2021, IBM has claimed claimed they have finished 2nm chip technology by nanosheet technology, chips can achieve 45 percent higher performance and 75 percent lower energy use than worldwide most advanced 7 nm technology chips.

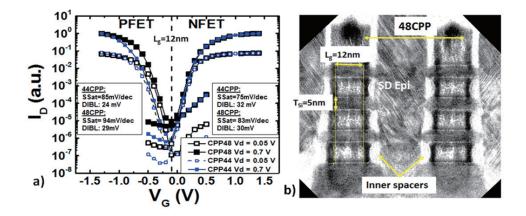


Figure 1.3: (a)  $I_D$ - $V_G$  transfer curves and (b) cross-section of the IBM and Samsung nanosheet GAA transistor.

With a very thin layer, MoS<sub>2</sub> can also be integrated into nanosheet transistors. In 2020 IEDM, Huang, Xiaohe, et al proposed 2-levels-stacked multi-bridge channels FET. With two nanosheet channels stacked between gates, this GAA-like transistors have SS values of nearly 60 mV/dec [67]. With the advantages of better gate control, 2D nanasheet transistors have the potential to be future transistors. Therefore, we discussed 2D nanosheet FETs and investigated the gate control and the current of the 2D nanosheet structure in chapter 4. Consequently, we optimized the 2D nanosheet transistors to meet the requirement of the International Roadmap for Devices and Systems (IRDS) for the future technology.

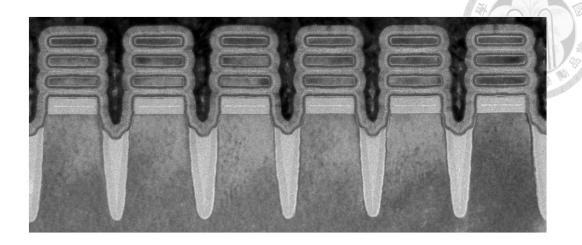


Figure 1.4: Cross section of the nanosheet FETs of IBM 2nm chip. (Figure comes from IBM website)

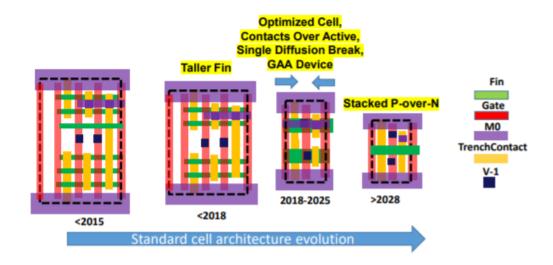


Figure 1.5: Scaling of the standard cell [11].

# 1.6 International Roadmap for Devices and Systems

The IRDS is a set of predictions of trends about devices, systems, and related technologies for the future fifteen years [11]. The roadmap shows the requirements for the future logic technologies to sustain Moore's scaling law. Table 1.2 shows

Table 1.2: IRDS roadmap (V  $_{TH,sat}$  and I  $_{on}$  are set at I  $_{off}$  =100 pA/ $\mu$ m) [11]

					1850 B			
Year	2020	2022	2025	2028	2031	2034		
Industry Node (nm)	5	3	2.1	1.5	1	0.7		
Device Architectures								
Device Structure	FinFET	FinFET	GAA	GAA	3DGAA	3DGAA		
Gate Length $L_G$ (nm)	20	18	14	12	12	12		
Device Electrical Specs								
Supply Voltage $V_{dd}$ (V)	0.7	0.7	0.65	0.65	0.6	0.55		
SS value (mV/dec)	72	75	63	68	65	65		
$V_{TH,sat}$ (mV)	345	363	312	341	326	326		
$R_{sd}$ (ohm- $\mu$ m)	285	271	257	244	232	221		
$I_{on} (\mu A/\mu m)$	484	495	546	521	459	347		
Energy per switch (fj)	0.66	0.65	0.49	0.47	0.40	0.33		

parts of the requirements of the device architectures and the device electrical specifications. As the previous section mentioned, the device structure will transit from FinFET to GAA FET to improve the electrostatics. Furthermore, after 2028, 3D GAA FET might become the mainstream with PMOS and NMOS stacked together, as shown in figure 1.5.

Besides the transition of the structure, the new electrical specifications of the device are also needed. To pursue lower power consumption, the supply voltage

 $(V_{dd})$  is also reduced. With the reduced  $V_{dd}$ , the gate drive is also reduced at the same time. SS value is requested to remain low to sustain the gate drive. In addition, reducing contact resistance  $(R_{sd})$  can also bring benefits to the performance. As for the current density, the leakage current  $(I_{off})$  target is under  $100 \text{ pA}/\mu\text{m}$  for the low-power applications. In the thesis, we will operate the 2D nanosheet transistor at  $V_{dd}$ =0.65V and  $I_{off}$ =100 pA/ $\mu$ m=1×10<sup>-4</sup>  $\mu$ A/ $\mu$ m to follow the IRDS requirement. Furthermore, the current density of the device will be compared with the  $I_{on}$  of the IRDS. In this way, we investigate whether the current density of the 2D nanosheet transistor is qualified for future technology.



# Chapter 2

# Methodology

### 2.1 Overview

In the chapter, we first describe the scattering rate and scattering mechanisms involved in the Monte Carlo method. Afterward, we introduce the multi-valley Monte Carlo method. This approach is used to calculate steady velocities and transient velocities of MoS<sub>2</sub> and WS<sub>2</sub>. Subsequently, Monte Carlo method and Poisson-and-drift-diffusion model are combined to simulate the devices. In the end, the device simulation software 2D-DDCC will be briefly introduced. Investigation of devices in chapter 4 is by the simulation software.

# 2.2 Scattering Mechanism and Scattering Rate

Due to lattice vibration and lattice imperfection, carriers don't transport in perfect periodic structures. When carriers go through those imperfections, they are 2. Methodology 16

deflected from its original trajectory into the new direction. The phenomenon is called scattering. As those imperfections are small, scatterings can be seen as perturbation. When those scatterings are seen as a perturbation, Fermi's golden rule is used to calculate the rate of scatterings, which is called the scattering rate. Fermi's golden rule can be written as

$$W(k) = \frac{2\pi}{\hbar} \sum_{k'} |M_{kk'}| \delta(E_k - E_{k'}), \qquad (2.1)$$

where W(k) is the scattering rate when the carrier is at the momentum of k,  $M_{kk'}$  is the scattering matrix element,  $E_k$  is the energy of the initial state and  $E_k'$  is the energy of the final state. There are two groups of scattering mechanisms, elastic scattering, and inelastic scattering. Elastic scattering indicates that in the process, energy is conserved. This group contains acoustic phonon scattering. On the other hand, the process of inelastic scattering involves the emission and absorption of energy. This group consists of optical deformation potential phonon scattering and acoustic deformation potential phonon scattering. In the thesis, both groups of mechanisms are included to discuss the scattering rates of  $MoS_2$  and  $WS_2$ . With these scattering rates, we can realize the effect of those imperfections on the transport of carriers. In the following sections, some important scattering mechanisms in TMD materials are listed and explained.

#### 17

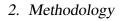
### 2.2.1 Acoustic Phonon Scattering

In the real crystal, atoms are not stationary in their positions. They vibrate like springs around their equilibrium positions. As atoms deviate from equilibrium, they cause strain in the crystal. Strain, in turn, influences the electronic states and results in strain energy. Phonon is proposed as a kind of particle to consider the effect of strain energy. Scatterings caused by lattice vibration are seen as a collision of electrons and phonons. Generally, as shown in figure 2.1, there are two phonon types: acoustic phonon and optical phonon. They respectively represent different modes of lattice vibration. When atoms in the unit cell move in the same direction, the derivative of displacement results in strain energy. Acoustic phonon is used to describe the phenomenon. Perturbation potential induced by the in-phase movement is given by

$$U_{ac} = D_{ac} \frac{\partial u}{\partial x} \tag{2.2}$$

where  $D_{ac}$  is the deformation potential in a specific valley for acoustic phonons and  $\frac{\partial u}{\partial x}$  is the derivative of displacement of two atoms.

In figure 2.1(b) [53], LA, TA, and ZA represent acoustic phonon branches of  $MoS_2$ . As shown in figure 2.1(b), when acoustic phonon momentum q=0, phonon energy is very small. When the material is under room temperature, we can see acoustic phonon scattering as elastic phonon scattering. In the thesis, we combine Eq. (2.1) and Eq. (2.2). After organization, acoustic phonon scattering rate is



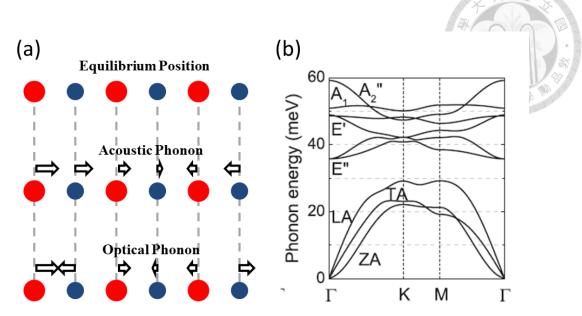


Figure 2.1: (a) Schematic diagram of lattice vibration of acoustic phonon and optical phonon (b) Phonon dispersion of MoS<sub>2</sub>

described by

$$W_{ac}(k) = \frac{\pi k_B T D_{ac}^2}{\hbar \rho v_{ac}^2} N_{2D}(E_k)$$
 (2.3)

where  $k_B$  is Boltzmann constant, T is temperature,  $N_{2D}(E_k)$  is the density of state of the energy level of  $E_k$ ,  $\rho$  is the mass density of 2D material,  $v_a$  is sound velocity. Due to small energy transfer, acoustic phonon scattering is the dominant scattering mechanism under low electric field or low electron energy.

# 2.2.2 Optical Phonon: Deformation Potential Scattering

Unlike the vibration mode of acoutsitc phonon, optical phonon happens when two atoms vibrate against each other. Energy perturbation caused by strain also appears and is proportional to the atomic displacement. Based on deformation potential

#### 2. Methodology

theory, perturbation potential can be described as



$$U_{dp} = D_{dp}u$$

where  $D_{dp}$  is the deformation potential of optical phonon, and u is the relative displacement of two atoms. The energy perturbation results in deformation potential scattering. As shown in figure 2.1(b), A1, A2", E', and E" represent optical phonon branches. When q is near 0, phonon energy is still not zero. Zero phonon energy indicates the process of electron and phonon interaction needs energy absorption or energy emission. With perturbation energy in Eq. (2.4), Eq. (2.1) can be written as

$$W_{dp}(k) = \frac{\pi D_{dp}^2}{2\rho\omega_o} \left[ n(\omega_o) + \frac{1}{2} \mp \frac{1}{2} \right] N_{2D}(E_k \pm \hbar\omega_o)$$
 (2.5)

### 2.2.3 Intervalley Phonon Scattering

As there are a variety of valleys in the band structure, carriers can transfer from one valley to another. As carriers scatter from valley to valley, the interaction is similar to deformation potential. The intervalley phonon scattering process needs to fulfill energy conservation when electrons absorb and emit phonon. Intervalley scattering rate can be written as

$$W_{ac/dp} = \frac{\pi D_{ac/dp}^2}{2\rho\omega_o} \left[ n(\omega_{ac/dp}) + \frac{1}{2} \mp \frac{1}{2} \right] N_{2D}(E_k \pm \hbar\omega_a c/dp)$$
 (2.6)

where footnotes "ac" or "dp" represent the phonon type involved in intervalley scattering. Figure 2.2 shows intervalley phonon scattering happening in  $MoS_2$ . As electrons absorb or emit phonon, they can scatter from K valley to satellite Q

valleys. In addition, electrons can also scatter from Q valley back to K valley in this way.

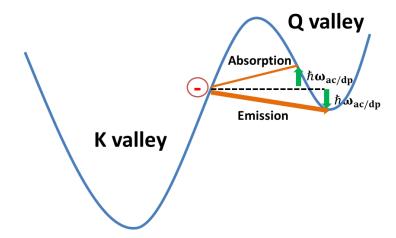


Figure 2.2: Intervalley phonon scattering process in MoS<sub>2</sub>. Electrons can scatter from K valley to satellite Q valleys by absorbing or emitting phonon. As electrons get higher energy, they are much easier to have the K-to-Q intervalley phonon scattering.

#### 2.2.4 Remote Phonon Scattering

When dielectric layers around 2D materials support polar vibrational modes, electrons in 2D materials excite phonon in those dielectrics via long-range Coulomb interactions. The phonon scattering is called "remote phonon scattering" or "surface-optical phonon scattering." Nowadays, when investigating the performance of 2D-material-based FET, remote phonon scattering plays a key role to affect transport [68, 69]. The process of remote phonon scattering is inelastic and has strong relationships with types of surrounding materials. The electron-phonon coupling

strength  $F^2$  is

$$F^{2} = \frac{\hbar\omega_{so}}{2A\epsilon_{o}} \left( \frac{1}{\epsilon_{tox}^{\infty} + \epsilon_{box}^{\infty}} - \frac{1}{\epsilon_{tox}^{o} + \epsilon_{box}^{o}} \right),$$



where  $\hbar\omega_{so}$  is phonon energy of remote phonon mode,  $\epsilon_{tox}^{\infty}$  is the high-frequency permittivity of the top oxide,  $\epsilon_{box}^{\infty}$  is the high-frequency permittivity of the bottom oxide,  $\epsilon_{tox}^{o}$  is the low-frequency permittivity of the top oxide, and  $\epsilon_{box}^{o}$  is the low-frequency permittivity of the bottom oxide. If there are two remote phonon modes in materials,  $F^{2}$  can be rewritten as [69]

$$F_1^2 = \frac{\hbar \omega_{so,1}}{2A\epsilon_o} \left( \frac{1}{\epsilon_{tox}^{int} + \epsilon_{box}^{int}} - \frac{1}{\epsilon_{tox}^o + \epsilon_{box}^o} \right), \tag{2.8}$$

$$F_2^2 = \frac{\hbar \omega_{so,2}}{2A\epsilon_o} \left( \frac{1}{\epsilon_{tox}^{\infty} + \epsilon_{box}^{\infty}} - \frac{1}{\epsilon_{tox}^{int} + \epsilon_{box}^{int}} \right), \tag{2.9}$$

where  $\epsilon_{tox}^{int}$  is intermediate permittivity of the tox oxide and  $\epsilon_{box}^{int}$  is intermediate permittivity of the bottom oxide. The frequency of remote phonon mode  $\omega_{so}$  is [70, 69]

$$\omega_{so,1} = \omega_{TO,1} \sqrt{\frac{\epsilon_{tox}^o + \epsilon_{box}^{\infty}}{\epsilon_{tox}^{int} + \epsilon_{box}^{\infty}}}$$
 (2.10)

$$\omega_{so,2} = \omega_{TO,2} \sqrt{\frac{\epsilon_{tox}^{int} + \epsilon_{box}^{\infty}}{\epsilon_{tox}^{\infty} + \epsilon_{box}^{\infty}}}.$$
 (2.11)

 $\omega_{TO,1}$  and  $\omega_{TO,1}$  are transverse optical-phonon frequencies in the dielectric. Scattering rate  $W_{so}$  is

$$W_{so}(k) = \frac{2\pi}{\hbar} \frac{1}{4\pi^2} \int \frac{e^2 F^2}{\epsilon(q,\omega)^2} \frac{\exp(-qd)}{2q}$$
$$\left[ n(\omega_o) + \frac{1}{2} \mp \frac{1}{2} \right] \delta(E_k - E_{k'} \pm \hbar \omega_{so}) dk'$$



q is wave vector  $|q_k - q_{k'}|$ , d is the thickness of 2D materials, and  $\epsilon(q, \omega)$  is the static screening of the 2D material, which is described as

$$\epsilon(q,\omega) = 1 + v_c(q)\Pi(q,\omega), \tag{2.13}$$

where  $v_c$  is  $\frac{e^2}{2\hat{\kappa}q}$ ,  $\hat{\kappa}$  is  $\frac{\epsilon^o_{tox}+\epsilon^o_{box}}{2}$  and we approximate  $\Pi(q,\omega)$  as  $\frac{m}{\pi\hbar^2}$ 

# 2.3 Multi-valley Monte Carlo Method

#### 2.3.1 Monte Carlo Method

The Monte Carlo method is a statistical approach to simulate random events. In the Monte Carlo method, random numbers are generated to simulate the real physical phenomenon of probabilistic nature, like carrier transport in materials[64]. Figure 2.3 is the schematic diagram of electron transport in the material. As an electric field is exerted on the material, it exerts an electric force on the electron. At the same time, the electron is accelerated. The electron begins to fly in the direction of the electric field. However, during flight, the electron will also scatter by phonon or other charged particles, like impurity. When scattering happens, the transport of the electron is influenced and mometum, and velocity are changed. After scattering, the electron will transport the material with the new momentum and velocities until the subsequent scattering happens. In the whole process, flight intervals between

two scattering events and states after scattering are probability problems. Hence, we can use the Monte Carlo method to generate random numbers to simulate the whole process and know the electron transport properties.

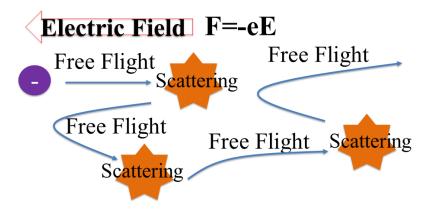


Figure 2.3: Schematic diagram of carrier transport in material.

The detailed steps of the Monte Carlo method are shown in figure 2.4. First of all, an electric field is exerted providing electric force to the electron. Secondly, according to the newly generated random number, the flight interval is decided. Afterward, the electron will fly for the flight interval. Thirdly, scattering mechanisms discussed in the previous section are included. A random number is generated to select a scattering event. If a scattering mechanism has a larger scattering rate, it has more chances to be selected. Fourthly, the final state of the electron after scattering event is decided by the selected scattering and newly generated random number. In the end, new momentum, carrier energy, velocities, and flight distance during the flight interval are determined and recorded. Subsequently, repeat the whole process until the condition, like total flight time or total flight distance, we set are fulfilled. The five steps mentioned above are the process of simulating

an electron. Hundreds of times of the process should be conducted to know the transport properties of carriers. In this way, the average velocities of carriers and mobilities will be known. In the thesis, to discuss mobilities and saturation velocities, the strength of electric fields ranges from  $1\times10^2$  V/cm to over  $4\times10^5$  V/cm. In addition, the carrier flys for 0.02 cm to make sure the carrier is in a steady state and not affected by the bias of random numbers. By these settings, field-dependent velocities are extracted.

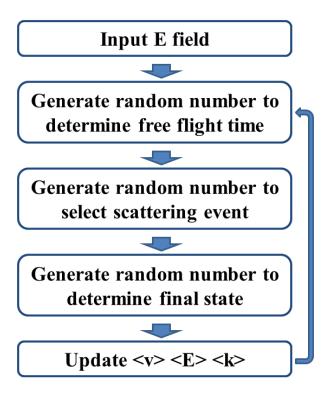


Figure 2.4: Flow chart of Monte Carlo method.

2. Methodology 2.

### 2.3.2 Multi-valley and non-parabolic band conditions

In the study of MoS<sub>2</sub> and WS<sub>2</sub>, the lowest valley in the conduction band is located in the K point of the hexagonal Brillouin zone. With symmetry of hexagon, there are two K-like valleys, K and K' valleys, respectively. Figure 2.5(a) shows the first Brillouin zone. Intervalley acoustic phonon scattering and intervalley optical phonon scattering happen between the two valleys. In addition, there are six satellite Q valleys around K valleys and with energy difference under 100 meV. As a result, those satellite valleys may cause strong phonon scattering between them. As a result, multi-valley Monte Carlo was adopted to deal with the effect of those satellite valleys in transport. Figure 2.5(b) shows the inter-valley scattering mechanism from K valley. By multi-valley model, the whole Brillouin zone is simplified into two kinds of valleys, which are the main factors to influence the transport.

To simplify the process of simulation, non-parabolic approximation

$$E(1 + \alpha E) = \frac{\hbar^2 k^2}{2m^*} \tag{2.14}$$

is used to describe K and Q valleys. With Eq. (2.14), we can use effective mass to describe low energy bands and  $\alpha$  to represent non-parabolic conditions of bands at high electron energy. Besides, Eq. (2.14) is mainly used to describe the isotropic valley, which has no evident difference in different transport directions. If the valley is anisotropic, Eq. (2.14) can be converted into

$$E(1 + \alpha E) = \frac{\hbar^2 k_x^2}{2m_x^*} + \frac{\hbar^2 k_y^2}{2m_y^*}$$
 (2.15)

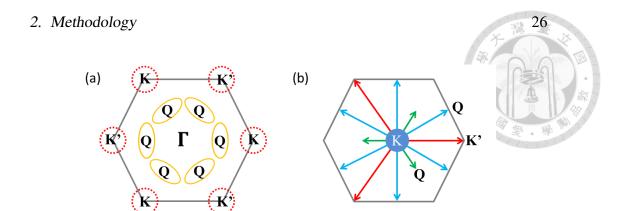


Figure 2.5: (a)K valleys and Q valleys in the first Brillouin zone. (b)Intervalley scattering from K valleys to neighboring K' valleys and satellite Q valleys. In figure(a), there is one K valley and a symmetrical K-like valley, K' valley, and six Q valleys in the first Brillouin zone. The lowest conduction band is located in either K or K' valley. In figure(b), the green and blue lines represent the K-to-Q inter-valley scattering mechanism. The red line represents K-to-K' inter-valley scattering mechanism.

### **2.3.3** Transient Transport Calculation

When transistors scale down, carriers in the channel are facing an electric field over  $1\times10^6$  V/cm. When carriers pass a short channel with such a large electric field, overshoot transport happens [71]. When overshoot transport happens, carriers transport through the channel with a less scattering process. The whole process is like ballistic transport. Therefore, when we discuss a channel that is shorter than 20 nm, field-dependent mobility in steady-state is not proper to describe the transport properties. Transient velocities of electrons should be considered. With the Monte Carlo method, not only steady transport properties but transient velocities can be calculated. The calculation of the transient transport will combine both the Monte Carlo method and the Poisson-and-drift-diffusion model. More detail will

be discussed in section 2.4.



## 2.4 Monte Carlo, Poisson and Drift-Diffusion Model

#### 2.4.1 Poisson and Drift-Diffusion Model

The Poisson equation is used to describe the relationship between carrier distribution in the device and potential. Poisson is

$$\nabla D = -\frac{1}{q} \nabla \epsilon \nabla E_c = q(N_A^- - N_d^+ + n - p + N_{trap}^{\pm})$$
 (2.16)

where D is electric potential, Ec is electron potential,  $N_A^-$  is the doping concentration of the acceptor,  $N_D^+$  is the doping concentration of the donor, n is the concentration of electron, p is the concentration of hole, and  $N_{trap}^{\pm}$  is concentration of trap. As source voltage bias is applied on the device, carrier distribution will change and there is the tilt of bands in the device. As current appears, we can use the drift-diffusion model to calculate the current. The drift-diffusion model is in equations

$$J_n = q\mu_n n\nabla V + qD_n \nabla n, \qquad (2.17)$$

$$J_p = q\mu_p p \nabla V - q D_p \nabla p, \qquad (2.18)$$

where  $J_n$  is electron current density,  $\mu_n$  is electron mobility,  $D_n$  is the electron diffusion coefficient,  $J_p$  is hole current density,  $\mu_p$  is hole mobility, and  $D_p$  is the hole diffusion coefficient. Eq. (2.17) consists of two parts. One is  $q\mu_n n\nabla V$  representing drift current in the device. Drift current comes from the acceleration

of the electric field in the device and is proportional to the gradient of electric potential  $\nabla V$ . The other one is  $qD_n\nabla n$  representing diffusion current in the device and is proportional to difference of electron concentration. Eq. (2.18) describes in the same thing. When we know the electric field and carrier distribution in the device, the total current can be solved with these equations.

#### 2.4.2 Monte Carlo, Poisson and Drift-Diffusion Model

We combine the Monte Carlo method into the Poisson-and-drift-diffusion model to consider the transient velocities. Firstly, we construct the material parameters and field-dependent velocities by the Monte Carlo method. Secondly, we solve the simulation model in the Poisson-and-drift-diffusion solver to get the distribution of the electric field along the channel. Thirdly, the distribution of the electric field is extracted and put into the Monte Carlo model to simulate the transient velocities. The electric field input of the Monte Carlo method varies with the position in the calculation of the transient velocities. Then, we calculate the electron velocities of the different positions in the channel and get the position-dependent velocities. The position-dependent velocities are the transient velocities. Then, transient velocities are put into the Poisson-and-drift-diffusion solver to get the new distribution of the electric fields. Afterward, the electric field from the Poisson-and-drift-diffusion solver and the transient velocities from the Monte Carlo method are calculated iteratively until the conduction band from the Poisson-and-drift-diffusion solver converges. In this way, the transient velocities are considered

29

in the device simulation.

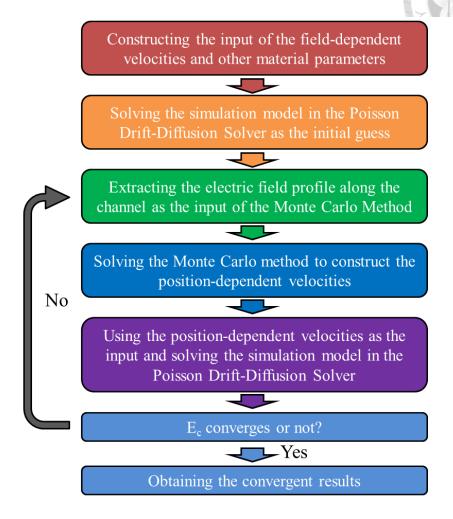


Figure 2.6: Flow chart of the Monte Carlo, Poisson and Drift-Diffusion Model.

# 2.4.3 Two Dimensional Poisson, Drift-Diffusion, and Schrodinger Solver

All calculation of the Poisson-and-drift-diffusion model is executed in Two Dimensional Poisson, Drift-Diffusion, and Schrodinger Solver (2D-DDCC). 2D-DDCC is a software developed by Professor Yuh-Renn Wu and his lab, optoelectronic

device simulation laboratory. The software is developed to describe optoelectronic and electronic devices ranging from LED, Solar Cell, LASER, 2D material-based transistors, etc [72, 73]. Besides 2D-DDCC, Professor's team has also developed the 1D-DDCC and the 3D-DDCC model. All three software have been applied on many devices, and results are published in SCI papers. In the thesis. to discuss transistors, 2D-DDCC is used to simulate the 2D nanosheet transistor.



# Chapter 3

# Transport Properties of $MoS_2$ and

# $\mathbf{WS}_2$

### 3.1 Overview

In the chapter, fundamental transport properties have been studied. Firstly, band structures of  $MoS_2$  and  $WS_2$  are calculated in QuantumATK, a density functional theory (DFT) software [74]. After getting band structures, acoustic phonon scattering and deformation potential scattering are calculated in section 3.3. Both phonon scattering mechanisms are intrinsic properties of materials, which naturally exist in every material. Hence, we call them intrinsic transport properties. The properties mainly dominate transport under low concentrations of impurities and carriers. Without the impurities and remote phonon effect, it is the upper limits of transport properties of materials. After the discussion of intrinsic transport

properties, those properties are going to be used in devices. Furthermore, with the monolayer structure stacked between two dielectric layers, transport properties are significantly influenced by the remote phonon scattering. Hence, remote phonon scattering will be discussed in section 3.4.

#### 3.2 Band structure

#### 3.2.1 Band structure by DFT

In the study, the geometry structure and band parameters come from DFT. LCAO calculator is used with local density approximation as an exchange correction function. The calculation is conducted in QuantumATK software. The crystal geometry is optimized until the atomic force decreases to values less than 0.005 eV/ $^{\rm A}$ . In addition, to make sure each layer of MoS $_{\rm 2}$  in the repeated unit cell won't interact with each other, the vacuum region is set to be 40  $^{\rm A}$ . Calculated lattice constants of MoS $_{\rm 2}$  and WS $_{\rm 2}$  are 3.12  $^{\rm A}$  and 3.123  $^{\rm A}$ , respectively. With the optimized structure, band structures are calculated and shown in figure 3.1. Bandgaps are 1.87 eV in MoS $_{\rm 2}$  and 1.99 eV in WS $_{\rm 2}$ . Lattice constants and bandgaps are in agreement with the results previously reported [75]. Besides the bandgap, the energy difference between K and Q valleys ( $^{\rm AE}_{KQ}$ ) and effective mass are also known. Table 3.1 shows the fundamental parameters from DFT.

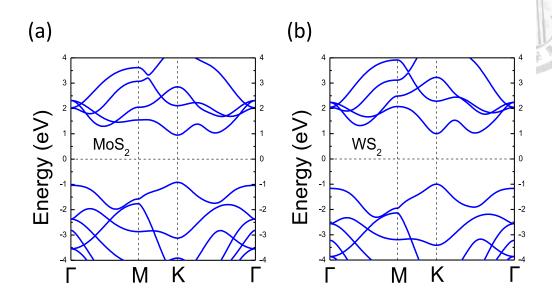


Figure 3.1: (a) Band structure of  $MoS_2$ . (b) Band structure of  $WS_2$ .

Table 3.1: Fundamental parameters of  $MoS_2$  and  $WS_2$  from DFT

Material	Lattice (Å)	Bandgap (eV)	$\Delta \mathrm{E}_{KQ}(\mathrm{meV})$
$MoS_2$	3.12	1.87	84.6
$\mathrm{WS}_2$	3.123	1.99	27.7

# 3.2.2 Band structure fitting

In the multivalley Monte Carlo model, the non-parabolic approximation is used to catch the E-K relation of the two materials. Due to nearly isotropic properties in K valleys of the two materials, Eq. (2.14) is used. As for Q valleys, with anisotropic energy surface, Eq. (2.15) is used. Table 3.2 shows the fitted parameters. Figures 3.2 and 3.3 show the comparison of the DFT original data and fitted data.

Table 3.2: Fitted effective mass and non-parabolic parameter,  $\alpha$  of K and Q valleys in MoS<sub>2</sub> and WS<sub>2</sub>

Material	$m_K \left(m_o\right)$	$\alpha_K$ (1/eV)	$\mathrm{m}_Q \ (\mathrm{m}_o)$	$\alpha_Q(1/\mathrm{eV})$
$MoS_2$	0.51	1.2	$m_x$ =0.56 $m_y$ =0.88	0.5
$\mathbf{WS}_2$	0.32	0.8	$m_y = 0.65 m_y = 0.64$	0.5

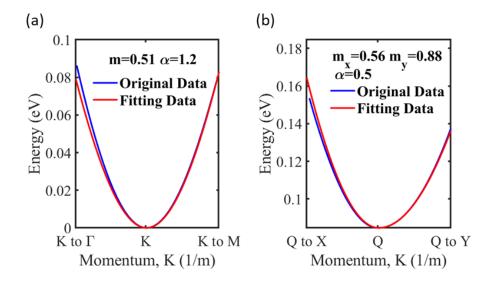


Figure 3.2: (a) Fitting of K valley in  $MoS_2$ . (b) Fitting of Q valley in  $MoS_2$ . Blue lines represent the original data from the band structures, and red lines are fitting curves of the E-K relation with non-parabolic Eq. (2.14) or Eq. (2.15).

# 3.3 Intrinsic Electrical Transport Properties

Intrinsic electrical transport properties of MoS<sub>2</sub> and WS<sub>2</sub> are decided by the phonon scatterings, including acoustic phonon scattering, optical phonon scattering, and intervalley scattering. In the section, scattering rates mentioned above were

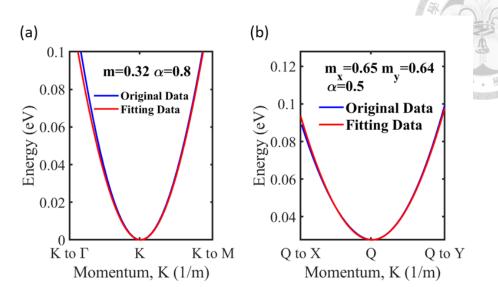


Figure 3.3: (a) Fitting of K valley in  $WS_2$ . (b) Fitting of Q valley in  $WS_2$ . Blue lines represent origin data from band structures, and red lines are fitting curves of E-K relation with non-parabolic Eq. 2.14 and Eq. 2.15.

discussed and results were put into the Monte Carlo method to see the mobilities and field-dependent velocities of both materials. We used deformation potentials and phonon energies from [52] and [75] to calculate the scattering rate. The detailed deformation potential constants and phonon energies are listed in Appendix A.

Figure 3.4 shows the calculated results of the scattering rate of MoS<sub>2</sub>. In figure 3.4(a), there are two apparent jumps in the total scattering rate. The first one is located at 48meV, and the second one is located at 110meV. When the electron energy is under 110 meV, intravalley scatterings, including acoustic phonon scattering and optical deformation potential phonon scattering, dominate the total scattering rate. When the electron energy is under 48meV, the acoustic phonon is dominant. When electrons reach 48meV, they begin to be scattered by emitting optical phonon

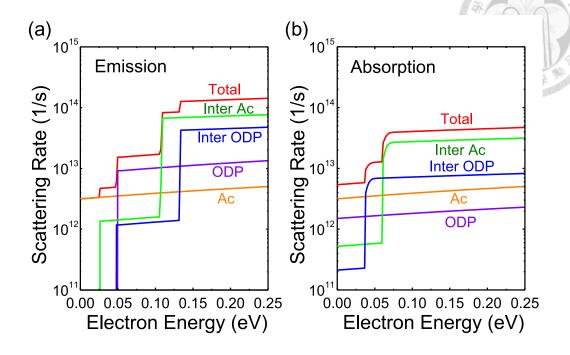


Figure 3.4: Electron-phonon scattering rates in  $MoS_2$  via (a) emission and (b) absorption of phonons calculated at room temperature. The orange and purple lines represent acoustic phonon scattering rate and optical deformation potential phonon scattering rate. The green and blue lines represent intervalley scattering rates caused by acoustic phonon and optical deformation potential phonon. The red line indicates the total scattering rates of all mechanisms.

and to the state with lower energy. With optical phonon scattering happening, the total emission scattering rate has a jump from  $3\times10^{12}~\rm s^{-1}$  to  $1\times10^{13}~\rm s^{-1}$  at the energy of 48 meV. Consequently, the first jump appears. Furthermore, when the electron energy is above 110 meV, the intervalley scattering comes into play, and the total scattering rate significantly increases over  $1\times10^{14}~\rm s^{-1}$ , which is ten times larger than the intravalley scattering rate. Because of the significant increase in the total scattering rate, the second jump happens at 110 meV in figure 3.4(a). In

addition, the intervalley scattering consists of K-to-K' intervalley scattering and K-to-Q intervalley scattering. K valley and K' valley have the same energy level, so K-to-K' intervalley scattering activates at 26 meV, which corresponds to acoustic phonon energy with the momentum of K. If electrons gain enough energy, K-to-Q intervalley scattering happens. With six satellite Q valleys around K valley, K-to-Q intervalley scattering works strongly and dominates the whole transport process. Figure 3.4(b) shows the same results. The difference is that this kind of scattering happens via the absorption of phonon.

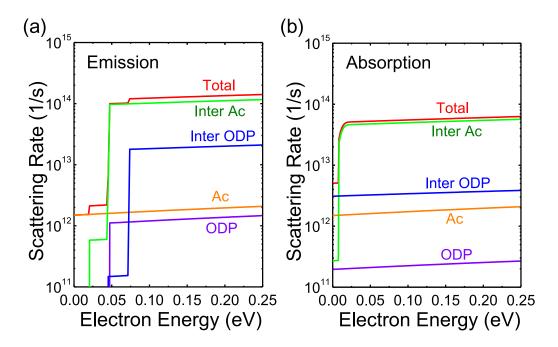


Figure 3.5: Electron-phonon scattering rates in  $WS_2$  via (a) emission and (b) absorption of phonons calculated at room temperature.

Figure 3.5 shows the calculated results of the scattering rate in  $WS_2$ . Different from  $MoS_2$ , there is only one noticeable jump around 50 meV in figure 3.5(a). The

reason is that  $\Delta E_{KQ}$  in WS<sub>2</sub> is only 27.7 meV. With the tiny $\Delta E_{KQ}$ , intravalley optical phonon scattering and intervalley scattering activate at almost the same energy level. As a result, there is only one clear jump in the total scattering rate. Besides, the energy difference between  $\Delta E_{KQ}$  and intervalley acoustic phonon energy is only 10 meV. Therefore, electrons in WS<sub>2</sub> are easier to absorb phonon at low energy compared to electrons in MoS<sub>2</sub>.

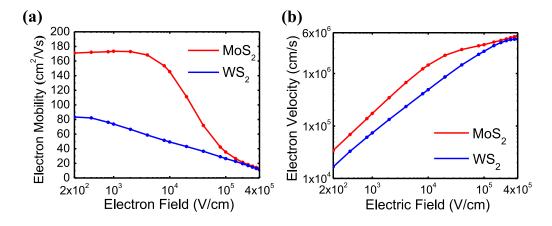


Figure 3.6: (a) Field-dependent mobilities and (b) field-dependent velocities are shown. The red lines represent the intrinsic transport properties of  $MoS_2$ , and the blue lines represent the intrinsic transport properties of  $WS_2$ .

After getting the scattering rates of both materials, we put them into the multivalley Monte Carlo model to calculate the intrinsic transport properties of the two materials. Field-dependent mobilities and velocities are shown in figure 3.6(a) and 3.6(b), respectively. The mobility of  $MoS_2$  is  $171 \text{ cm}^2/V$ -s, and the mobility of  $WS_2$  is  $83 \text{ cm}^2/V$ -s. The mobility of  $MoS_2$  is much higher than that of  $WS_2$ . However, there is no much difference in high field velocities. From figure 3.7,

we can see the reason for the difference in transport behavior between low field and high field. Figure 3.7(a) shows the average electron potential energy versus the electric field. Under a low electric field, electron potential energy in WS<sub>2</sub> is 0.039eV, which is higher than the  $\Delta E_{KQ}$  of WS<sub>2</sub> so intervalley phonon scattering begins. The total scattering rate of WS<sub>2</sub> at energy=0.039 eV is  $5.4\times10^{13}$  s<sup>-1</sup>. On the contrary, the electron potential energy of MoS<sub>2</sub> under a low field is 0.036 eV, which is much lower than the  $\Delta E_{KQ}$  of MoS<sub>2</sub>, so intervalley phonon scattering doesn't work intensely. The total scattering rate of MoS<sub>2</sub> at energy=0.036 eV is only  $1.1\times10^{13}$  s<sup>-1</sup>. With a lower scattering rate, the mobility of MoS<sub>2</sub> is much higher than that of WS<sub>2</sub>. As a result,  $\Delta E_{KQ}$  influences activation of intervalley phonon scattering and, then, significantly affects the mobility of both materials.

When the electric field is higher than  $1\times10^4$  V/cm, electrons gain enough energy and have a higher probability of transporting in higher energy states. When electrons have higher energy states, both materials have comparable scattering rates. Therefore, MoS<sub>2</sub> andWS<sub>2</sub> have saturated velocities of  $5.2\times10^6$  cm/s and  $4.5\times10^6$  cm/s at an electric field of  $4\times10^5$  V/cm. There is no much difference in the high-field velocities.

# 3.4 Extrinsic Transport Properties

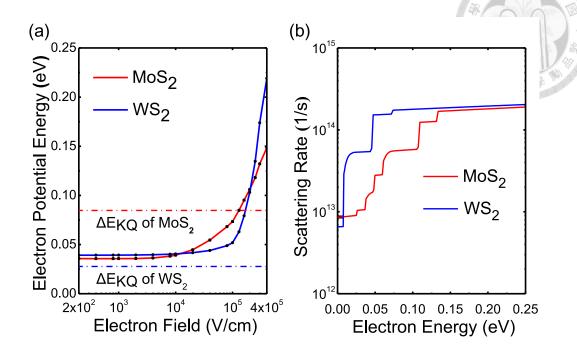


Figure 3.7: (a) Average electron potential energy and (b) total scattering rates of both  $MoS_2$  and  $WS_2$ . The average electron energy of  $WS_2$  under low field is 0.039 eV and higher than  $\Delta E_{KQ}$ . The corresponding scattering rate of  $WS_2$  in (b) is  $5.4 \times 10^{13}$  s<sup>-1</sup>. The average electron energy of  $MoS_2$  under low field is 0.036 eV and higher than  $\Delta E_{KQ}$ . The corresponding scattering rate of  $MoS_2$  in (b) is  $1.1 \times 10^{13}$  s<sup>-1</sup>.

#### 3.4.1 Remote Phonone Scattering

Remote phonon scattering has been verified as a critical factor to degrade the transport performance of TMD materials [68]. Therefore, to design devices, remote phonon scattering caused by dielectrics in FET should be considered in our transport model, especially when dielectrics consist of high- $\kappa$  materials. Here we discuss the remote phonon of some commonly used dielectric materials, including SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, and hBN. Table 3.3 shows the permittivity and transverse

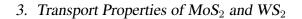
Table 3.3: Remote phonon modes for different dielectric materials.  $\epsilon_r^o$ ,  $\epsilon_r^i$  and  $\epsilon_r^\infty$  are low-frequency, intermediate and high-frequency permittivities, respectively.

Material	$SiO_2$	$Al_2O_3$	HfO <sub>2</sub>	hBN
$\epsilon_{r}^{o}\left(\epsilon_{0}\right)$	3.90	12.53	22.00	5.09
$\epsilon_r^i \left( \epsilon_0 \right)$	3.36	7.27	6.58	4.58
$\epsilon_r^{\infty} \left( \epsilon_0 \right)$	2.40	3.20	5.03	4.1
$\hbar\omega_{TO}^{1}\left(\mathrm{eV}\right)$	55.6	48.18	12.4	97.08
$\hbar\omega_{TO}^{2}\left(\mathrm{eV}\right)$	138.1	71.41	48.35	187.22

optical phonon frequency of these materials. Besides, in the nanosheet transistors, both top and bottom dielectrics surround the channel. Therefore, we only discussed the situation that 2D materials are stacked between the top and bottom dielectrics.

Calculation of the remote phonon scattering of  $MoS_2$  is shown in figure 3.8.  $MoS_2$  is stacked into the different dielectrics. With higher dielectric constant,  $HfO_2$ , and  $Al_2O_3$  have stronger remote phonon scattering. Besides, with lower-energy phonon modes, electrons are also scattered at lower energy states. On the contrary, remote phonon scatterings of hBN and  $SiO_2$  are weaker and activate at higher energy, so they have less impact on the transport properties.

Figure 3.9 shows the electrical transport properties considering the influences of the remote phonon scattering. If the dielectrics are hBN or  $SiO_2$ , the transport properties are close to the intrinsic transport properties. However, if dielectrics are  $Al_2O_3$  or  $HfO_2$ , the transport properties are degraded by the remote phonon



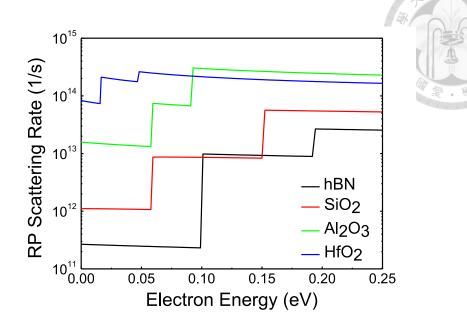


Figure 3.8: Remote phonon scattering rates of MoS<sub>2</sub> stacked into the different dielectric at the K valley.

scattering, which is due to the high dielectric constant and low-energy phonon modes of the high- $\kappa$  materials. The influences of the four dielectric materials on the transport are also verified by others [76, 68, 77]. The transport properties of WS<sub>2</sub> with different dielectrics are shown in figure 3.10. They have the similar characteristics as those of MoS<sub>2</sub>, but with stronger intrinsic phonon scattering, mobilities of WS<sub>2</sub> are lower than those of MoS<sub>2</sub>.

After discussing the transport properties of  $MoS_2$  and  $WS_2$  w/o and with different dielectrics, we know that  $MoS_2$  can perform better due to better intrinsic transport properties,. Therefore,  $MoS_2$  will be our first choice for the channel of the nanosheet transistors in the next chapter.



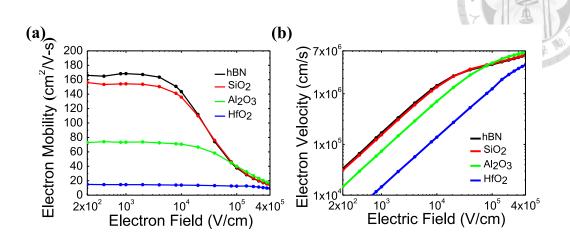


Figure 3.9: (a) Field-dependent mobilities and (b) field-dependent velocities of  $MoS_2$  with different dielectrics are shown. If  $MoS_2$  are surrounded by hBN or  $SiO_2$ , remote phonon scattering has no prominent effect on the electron transport properties. However, with  $Al_2O_3$  or  $HfO_2$  surrounding  $MoS_2$ , mobilities are degraded a lot.

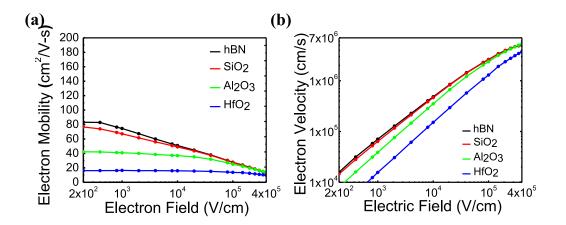


Figure 3.10: (a) Field-dependent mobilities, and (b) field-dependent velocities of  $WS_2$  with different dielectrics.



# **Chapter 4**

# MoS<sub>2</sub> and WS<sub>2</sub> Based Transistor

#### 4.1 Structures and Simulation Model of 2D Nanosheet

#### **Transistors**

In this chapter, subthreshold swing (SS), drain-induced barrier lowering (DIBL), and on-current ( $I_{on}$ ) will be discussed to see the gate controllability and the driving abilities of the 2D nanosheet transistors. We use  $MoS_2$  and  $WS_2$  as the channel. The channel of the transistor is a 0.6-nm-thick monolayer  $MoS_2$  or  $WS_2$  [67, 78]. Figure 4.1 shows the structure of the nanosheet transistor.  $L_G$  is the length of the top gate. In this structure, the bottom gate is symmetrical to the top gate. Therefore, the length of the bottom gate is also  $L_G$ . Besides, it is an underlap structure. Consequently, we leave a length of the underlap region ( $L_{un}$ ) between the gates and the source/drain (S/D) contact for the underlap region.

Besides the structure shown in figure 4.1, which has symmetrical top and

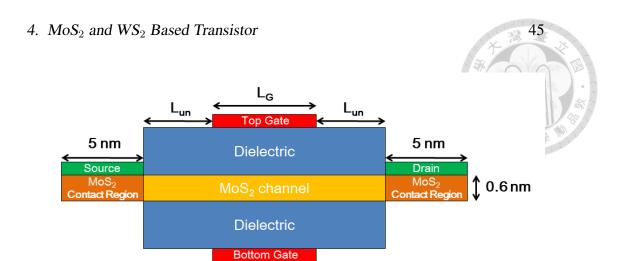


Figure 4.1: Illustration of the MoS<sub>2</sub> nanosheet transistor structure.

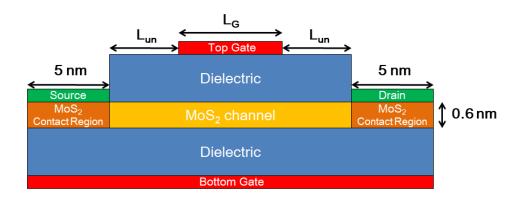


Figure 4.2: Illustration of asymmetrical MoS<sub>2</sub> nanosheet transistor structure.

bottom gates, we also discuss the nanosheet transistors with asymmetrical gates shown in figure 4.2. The bottom gate of the nanosheet transistor overlaps the S/D metal contact. With longer gate contact, the asymmetrical transistor has a longer effective  $L_G$ . Although longer  $L_G$  increases the gate capacitance, lowers the cutoff frequency and brings the negative influence to the RF applications, it has more possibility of inducing more carriers in the channel and offering better control [79, 80]. Later, we will compare the performances of the two structures.

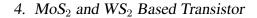
Table 4.1: Parameter settings for nanosheet transistors

Material	$MoS_2$	$\mathrm{WS}_2$	$Al_2O_3$	$HfO_2$
Band gap $E_g$ (eV)	1.87	1.99	8.9	5.5
Electron affinity $\chi$ (eV)	4.0 [83]	4.0 [84]	2.0	2.0
Electron effective mass $m^*$ ( $m^o$ )	0.51	0.32	1.0	0.21 [85]
Relative dielectric constant $\epsilon_r$ ( $\epsilon_o$ )	4.2 [86]	5.4 [87]	9.3	22

Afterward, factors like  $L_G$ , dielectrics,  $L_{un}$ , and doping will be discussed based on the structure with better performance to optimize the performance of the device.

Before the discussion, we need to choose suitable dielectrics first. In chapter 3, we discussed the commonly-used dielectrics like SiO<sub>2</sub>, hBN, Al<sub>2</sub>O<sub>3</sub>, and HfO<sub>2</sub>. The former two materials have slight degradation of mobilities. However, SiO<sub>2</sub> is not suitable for scaling down [12, 81]. As for hBN, it has a dielectric constant of only 5.09 [68]. If equivalent oxide thickness (EOT) is under 1nm, the thickness of hBN is under 1.3 nm, four layers of hBN, and can't sustain the gate leakage current under 1 A/cm<sup>2</sup> [15, 82]. Figure 4.3 shows the leakage current density for different dielectrics [12, 13, 14, 15, 81]. As a result, for better gate quality, Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> are better choices for dielectrics. We will discuss the thickness of Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> in the latter section to discuss the effect of the materials and EOT on the nanosheet transistors. Table 4.1 shows the parameter settings of the 2D materials and dielectrics.

Besides structures and dielectrics, the effects of changing  $L_G$ ,  $L_{un}$ , and dop-



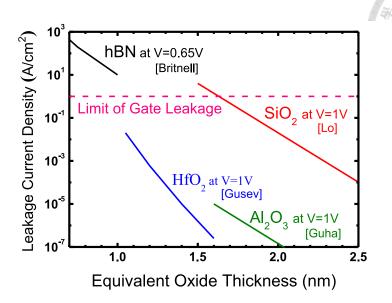


Figure 4.3: Leakage current density vs. equivalent oxide thickness for different dielectrics (Lo [12], Guha [13], Gusev [14], Britnell [15]).

ing are investigated, too. In addition, with dual gates in transistors, in the later discussion, drain currents are normalized by  $W_{eff}$ , which is equal to the double gate width. Furthermore, when we compare the  $I_{on}$  of the different transistors, the transistors are operated at the gate voltage  $V_G=V_{off}+V_{DD}$ , where  $V_{DD}$  is the supply voltage  $(V_{DD})$  and  $V_{off}$  is the gate voltage at which off-current  $(I_{off})$  happens. According to the IRDS,  $I_{off}$  should be fixed at  $1\times 10^{-4}~\mu\text{A}/\mu\text{m}$  for the low power applications and  $V_{DD}$  is 0.65V.

# 4.2 Comparision of Symmetrical and Asymmetrical

### Gate

Both symmetrical and asymmetrical  $MoS_2$  and  $WS_2$  nanosheet transistors with  $L_G$  of 14, 12, 10, 7, and 5nm are discussed.  $L_{un}$  is 5nm long, and the dielectric is 1nm EOT of  $Al_2O_3$ . 2D material has impurity doping of  $1\times10^{11}$  cm<sup>-2</sup> (1.67×10<sup>18</sup> cm<sup>-3</sup>). Total  $R_c$  including  $R_{c,source}$  and  $R_{c,drain}$  is 267  $\Omega \cdot \mu$ m. Figure 4.4 shows the transfer characteristics and output characteristics of the symmetrical  $MoS_2$  nanosheet transistor at  $L_G$ =5nm. Figure 4.5 shows the transfer characteristics and output characteristics of the asymmetrical  $MoS_2$  nanosheet transistor at  $L_G$ =5nm.

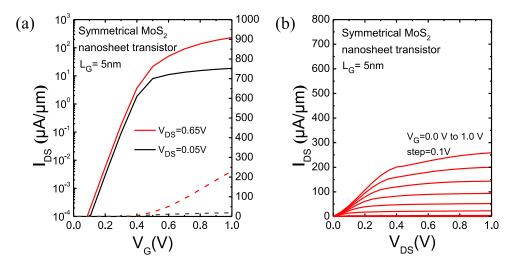


Figure 4.4: (a)  $I_{DS}$ - $V_G$  transfer characteristics for the symmetrical  $MoS_2$  nanosheet transistor at  $L_G$ =5 nm. (b)  $I_{DS}$ - $V_{DS}$  output characteristics for the symmetrical  $MoS_2$  transistor at  $L_G$ =5 nm.

When comparing the performance of the two structures, we discuss the transfer curves of the transistors at  $V_G-V_{off}$ . Figure 4.6 shows the transfer curves of

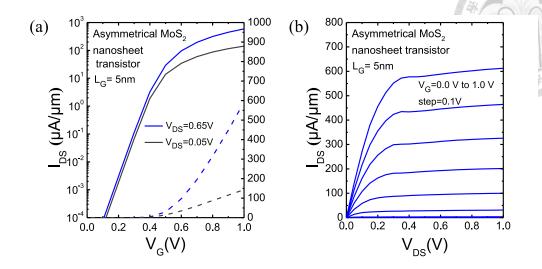


Figure 4.5: (a)  $I_{DS}$ - $V_G$  transfer characteristics for the asymmetrical  $MoS_2$  nanosheet transistor at  $L_G$ =5nm. (b)  $I_{DS}$ - $V_{DS}$  output characteristics for the asymmetrical  $MoS_2$  nanosheet transistor at  $L_G$ =5nm.

both structures at  $L_G$ =5, 7, 12, and 14nm. In the symmetrical structure, the largest  $I_{on}$  is at  $L_G$ =14nm and reaches 114  $\mu$ A/ $\mu$ m at  $V_{DS}$ = $V_G$ - $V_{off}$ =0.65V. In the asymmetrical structure, the largest  $I_{on}$  happens at  $L_G$ =7 nm and is 264  $\mu$ A/ $\mu$ m at  $V_{DS}$ = $V_G$ - $V_{off}$ =0.65V. In addition, no matter how long  $L_G$  is, the  $I_{on}$  of the asymmetrical MoS<sub>2</sub> nanosheet transistor is two times more than that of the symmetrical MoS<sub>2</sub> nanosheet transistor. There are two reasons. The first reason is that with a longer bottom gate, gates can induce two times more electrons in the channel. Figure 4.7(a) shows the electron density in the MoS<sub>2</sub> membrane. The second reason is that the bottom gate also causes more carriers in the overlap region between bottom and S/D metal. Figure 4.7(b) shows the relation between the contact resistance ( $R_c$ ) and the gate bias. When the gate bias is larger, the

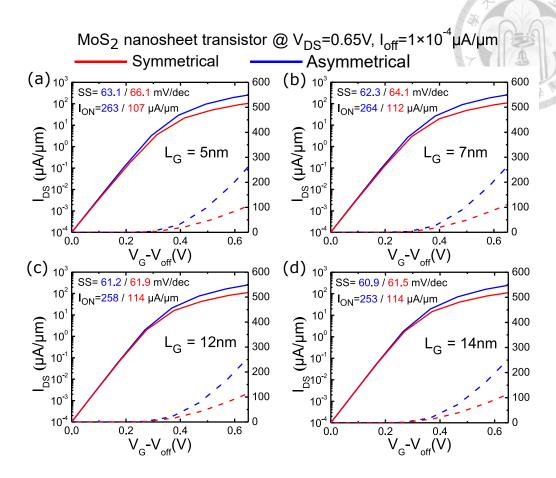


Figure 4.6: Transfer characteristics for the (a-d) MoS<sub>2</sub> nanosheet transistor with L<sub>G</sub>=5, 7, 12, 14nm. Transistors are operated at  $V_{DD}$ =0.65V and  $I_{off}$ =1×10<sup>-4</sup>  $\mu$ A/ $\mu$ m following the IRDS.

bottom gate of the asymmetrical structure can induce more carriers in the contact region and lowers the effect from Schottky barrier between S/D metal and MoS<sub>2</sub> [9]. Consequently, the  $R_c$  of the asymmetrical structure becomes  $105~\Omega \cdot \mu m$ , which is much smaller than  $267~\Omega \cdot \mu m$ . Lower  $R_c$  also causes benefits to the  $I_{on}$ . Although the contact resistance is totally reduced but the bottom gate has different influences on the source and drain contact. In figure 4.7(a), the electron density in the contact of the symmetrical structure is  $1 \times 10^{11}$ , which means gate bias doesn't affect the

contact resistance. Instead, the electron density in the source and drain of the asymmetrical structure is significantly enhanced and reduced. The gate bias in the drain depletes the electron, which causes larger  $R_c$ . However, the gate bias still decreases the  $R_c$ .

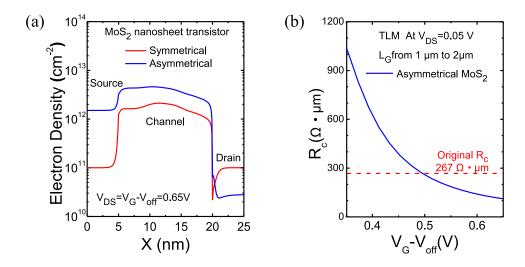


Figure 4.7: (a) The average of the electron density in the  $MoS_2$  membrane. (b)  $R_c$  vs. the gate bias.

Besides, figures 4.8(a) and 4.8(b) show DIBL and SS values as a function of  $L_G$ . The asymmetrical structure can keep SS value under 65 mV/dec and DIBL under 23 mV/V at  $L_G$ =5nm, demonstrating better gate control than the symmetrical structure. With a better gate control, gate drive at the limited supply voltage also increases.

The performances of WS<sub>2</sub> nanosheet transistors are also investigated and are summarized in figure 4.9. With a stronger scattering rate mentioned in chapter 3, the  $I_{on}$  of WS<sub>2</sub> transistors is lower than that of MoS<sub>2</sub> transistors. In addition, when



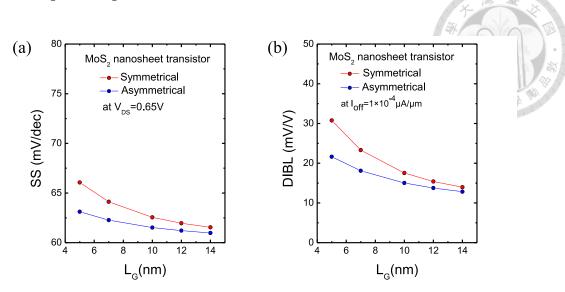


Figure 4.8: (a) Subthreshold swing SS at  $V_{DS}$ =0.65V as a function of  $L_G$  and (b) DIBL at  $I_{off}$ =1×10<sup>-4</sup>  $\mu$ A/ $\mu$ m as a function of  $L_G$  for symmetrical and asymmetrical MoS<sub>2</sub> nanosheet structure.

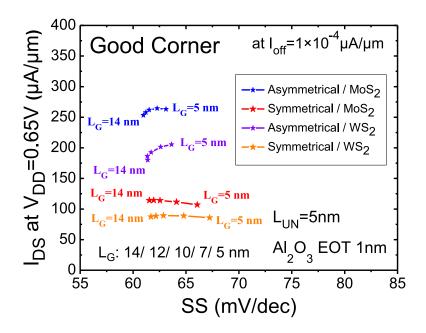


Figure 4.9: Comparison of the performance of the transistors with different structures, materials, and  $L_G$ .

 $L_G$ s scale down, the two designs show different trends of  $I_{on}$ . In the asymmetrical structure,  $I_{DS}$  are increasing when  $L_G$  is narrowing down. But when  $L_G$  scales down from 7nm to 5nm, the trend stops. The phenomenon comes from degradation of SS at  $L_G$ =5nm. When SS degrades, gate drive at  $V_{DD}$ =0.65V gets smaller. The effect of a smaller gate drive surpasses the benefit from  $L_G$  scaling down. Then, the  $I_{on}$  can't keep increasing. As for the symmetrical structure, scaling down can't increase  $I_{on}$ . The distinct phenomenon comes from the difference in the gate controllability between the two structures. The symmetrical structure has worse gate control. As  $L_G$  shrinks, the disadvantage of the SS degradation exceeds the advantage of enhancing electric fields. Consequently,  $I_{on}$  decreases with  $L_G$  scaling down. Therefore, if we want to pursue a higher  $I_{on}$  under limited  $V_{DD}$ , gate control is critical. If the transistor can't suppress short channel effects, shrinking  $L_G$  will make transistors worse. Finally, the performance of the asymmetrical  $MoS_2$  nanosheet transistor is the best. Therefore, in the later section, the asymmetrical structure and  $MoS_2$  are adopted to optimize the transistor.

## 4.3 Effect of Dielectric

EOT of dielectric is a critical factor influencing the performance of transistors. Nowadays, groups succeeded in growing  $HfO_2$  on  $MoS_2$  with an EOT of 1nm [88]. A model forecasts that to meet the requirement for the gate leakage of  $1A/cm^2$ , limits of EOT of  $Al_2O_3$  and  $HfO_2$  are 0.8nm and 0.9nm, respectively [89]. In the previous section, 1nm EOT  $Al_2O_3$  dielectric is discussed. However, when

 $L_G$  scales down to 5nm, 1nm EOT of  $Al_2O_3$  dielectric can't sustain very low SS and then slightly degrades  $I_{on}$ . As a result, a more aggressive design is needed to enhance the gate control and increase  $I_{on}$ . In the section, we use the asymmetrical  $MoS_2$  nanosheet transistors to investigate the effect of the dielectric. Dielectrics are  $Al_2O_3$  and  $HfO_2$ , with EOT ranging from 2nm to 0.8nm.

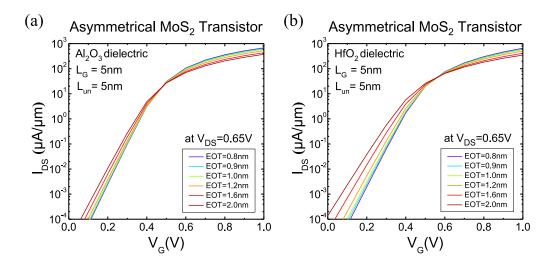


Figure 4.10:  $I_{DS}$ - $V_G$  transfer characteristics of the asymmetrical  $MoS_2$  nanosheet transistors with (a)  $Al_2O_3$  and (b)  $HfO_2$  dielectric.

Figure 4.10 shows the transfer characteristics of the transistors with the dielectric of  $Al_2O_3$  or  $HfO_2$ , respectively. With smaller EOT, the transfer curve is steeper, indicating smaller SS value. At the same time,  $I_{on}$  is also enhanced. Therefore, thinner EOT can boost the performance of the transistors.

We summarize the performance of the transistors with different dielectrics, EOTs, and  $L_G$  at  $V_{DS}=V_G-V_{off}=V_{DD}=0.65V$ . Comparing figures 4.11(a) and (b), the transistors with  $Al_2O_3$  show larger  $I_{on}$ . At  $L_G=5$ nm,  $I_{on}$  reaches 308  $\mu$ A/ $\mu$ m.

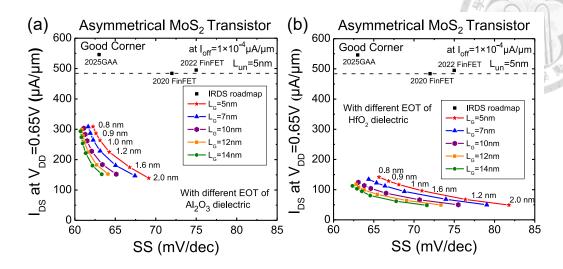


Figure 4.11: Comparison of the performance of the transistors with (a)  $Al_2O_3$  and (b)  $HfO_2$  dielectric.  $Al_2O_3$  dielectric demonstrates better performance.

As for HfO<sub>2</sub>, the maximum  $I_{on}$  is 141  $\mu$ A/ $\mu$ m. As a result, Al<sub>2</sub>O<sub>3</sub> is a better choice for the dielectric due to less impact from the remote phonon scattering. Besides, with thinner EOT, the gate control is improved. The benefits from scaling down of  $L_G$  appears. However, when we make EOT 0.8nm, which is the limit of the dielectric thickness,  $I_{on}$  still can't reach the requirement of the IRDS. As a result, the transistor structure needs other improvements.

# **4.4** Effect of $L_{un}$

In the previous section, the length of the discussed  $L_{un}$  is 5nm. However, it is possible to enhance  $I_{on}$  by selecting proper  $L_{un}$  [90]. In this section, we investigate the influences of  $L_{un}$  and select suitable  $L_{un}$  to increase  $I_{on}$ .

In figure 4.12, the drain currents of the transistors with different  $L_{un}$  are com-

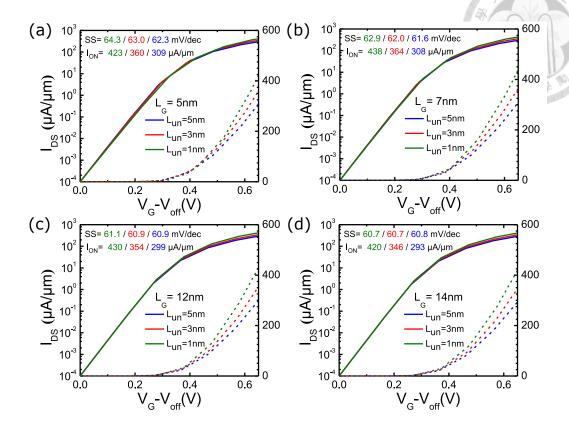


Figure 4.12: Transfer characteristics of transistors with (a)  $L_G$ =5nm, (b)  $L_G$ =7nm, (c)  $L_G$ =12nm and (d)  $L_G$ =14nm. With longer  $L_G$ , transistors demonstrate better gate control. With shorter  $L_u n$ ,  $I_{on}$  increases but gate control degrades.

pared at the same  $I_{off}=1\times10^{-4}~\mu\text{A}/\mu\text{m}$  and  $V_{DS}=0.65\text{V}$ . If  $L_{un}$  shrinks, currents are greatly enhanced beacause reducing  $L_{un}$  can effectively lowers the channel resistance. If  $L_{un}$  changes from 5nm to 1nm, the current at  $L_{G}=7\text{nm}$  increases from 308  $\mu\text{A}/\mu\text{m}$  to 438  $\mu\text{A}/\mu\text{m}$ , reaching 90% of the IRDS requirement. However, shorter  $L_{un}$  also brings DIBL and makes SS worse. In figure 4.13(a), when  $L_{un}$  shrinks down to 1nm, DIBL becomes stronger. Particularly at  $L_{G}=5\text{nm}$ , DIBL increases more than 30 mV/V. Figure 4.13(b) shows the conduction band of the transistor with  $L_{un}=1\text{nm}$ , and different  $L_{G}$  and  $V_{DS}$ . When  $L_{G}$  is 14nm, increasing

 $V_{DS}$  doesn't lower the potential barrier. On the contrary, when  $L_G$  is 5nm, the barrier maximum decreases with  $V_{DS}$  increasing. It means stronger DIBL exists in the shorter channel device and worsens the gate control. Figure 4.14 shows shrinking  $L_{un}$  causes higher  $I_{on}$  and worse SS. As  $L_{un}$  shrinks under 5nm, worse gate control causes less gate drive. Consequently, the maximum current of 438  $\mu$ A/ $\mu$ m appears at  $L_G$ =7nm.

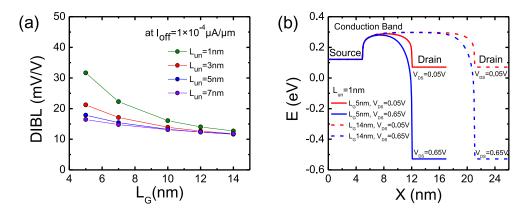


Figure 4.13: (a) DIBL as a function of  $L_G$ . (b) Conduction bands of the channels in the transistor with  $L_G$ =5 nm (solid line) and  $L_G$ =14nm (dotted line).

### 4.5 Effect of Doping

Doping can increase carrier density in the channel, but it is challenging to dope in an atomically thin layer. However, substoichiometric metal oxide has been studied to provide stable n-type and p-type doping in the 2D material layer [91, 92]. AlO $_x$  is n-type doping substoichiometric metal oxide. It can offer energy states beyond the bandgap of MoS $_2$  and induce more mobile electrons in MoS $_2$  [93]. Nowadays,

#### 4. MoS<sub>2</sub> and WS<sub>2</sub> Based Transistor

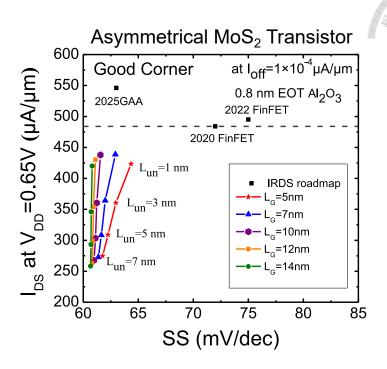


Figure 4.14: Comparison of the performance of the transistors with  $L_{un}$ =1, 3, 5, and 7nm and  $L_G$ =5, 7, 10, 12, and 14nm. The transistors are operated at  $V_{DD}$ =0.65V and  $I_{off}$ =1×10<sup>-4</sup>  $\mu$ A/ $\mu$ m and 0.8nm EOT Al<sub>2</sub>O<sub>3</sub> dielectric is used.

with one-sided AlO $_x$  capping on MoS $_2$ , the doping concentration in MoS $_2$  can reach  $2\times10^{13}$  cm $^{-2}$  [93]. Here we consider the undoped MoS $_2$  channel, which has electron concentration of  $1\times10^{11}$  cm $^{-2}$ , surrounded by the top and bottom AlO $_x$  to discuss the influences of the doping concentrations. Figure 4.15 shows the structure. First, devices with L $_G$ =100nm are used to discuss the relation between the doping concentration of AlO $_x$  and the induced electron concentration in MoS $_2$ . The relation is shown in figure 4.16. In this section, we have n-type AlO $_x$  with the doping concentrations of  $1.1\times10^{19}$ ,  $2.8\times10^{19}$ ,  $5.6\times10^{19}$ ,  $8.4\times10^{19}$ , and  $1.1\times10^{20}$  cm $^{-3}$  and the corresponding induced electron concentrations in MoS $_2$  are  $4\times10^{12}$ ,  $1\times10^{13}$ ,  $2\times10^{13}$ ,  $3\times10^{13}$  and  $4\times10^{13}$  cm $^{-2}$ .

58

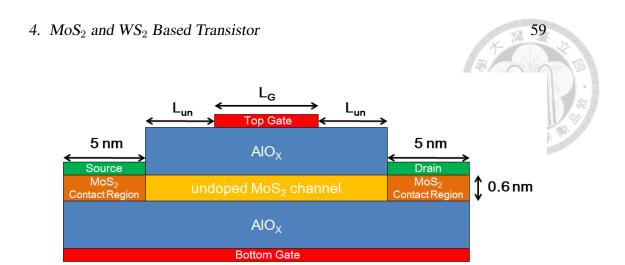


Figure 4.15: Illustration of the  $AlO_x$  doped  $MoS_2$  nanosheet transistor.

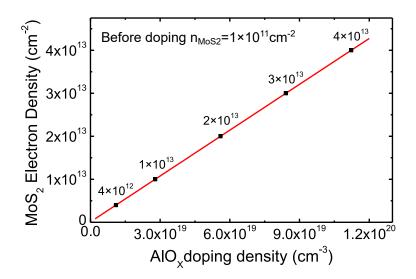


Figure 4.16: Linear relation between the doping concentration of  $AlO_x$  and the induced eletron concentration of  $MoS_2$ . The black dots are the doping concentrations to be investigated.

In figure 4.17(a), when the doping concentration increases, the threshold voltage ( $V_{TH}$ ) decreases.  $V_{TH}$  shifts rise from more electrons in the  $MoS_2$  channel. When comparing the performance, we also compare the transfer characteristics at  $V_G - V_{off}$ . Transistors operate at  $V_{DD}$ =0.65V. Figure 4.17(b) shows the perfor-

mance of the transistors with different doping concentrations. As doping increases, there is no influence on the gate control. Besides,  $I_{on}$  significantly increase. At  $L_G$ =7nm,  $L_{un}$ =1nm and n=3×10<sup>13</sup> cm<sup>-2</sup>,  $I_{on}$ =483  $\mu$ A/ $\mu$ m. Comparing to devices without doping,  $I_{on}$  increases 10%, and fulfills the requirement of the 2020 IRDS. If doping can reach n=4×10<sup>13</sup> cm<sup>-2</sup>,  $I_{on}$  reaches 495  $\mu$ A/ $\mu$ m, fulfilling the requirement of the 2022 IRDS. Therefore, if the process of doping won't infuence the quality of the inteface, substoichiometric metal oxide doping can bring benefits to the performance.

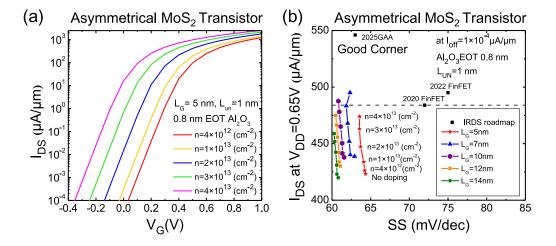


Figure 4.17: (a) Comparison of the transfer characteristics of the transistros with  $L_G$ =5nm,  $L_{un}$ =1nm, and different concentrations of MoS<sub>2</sub> doping. (b) Comparison of  $I_{on}$  and SS of transistors with different doping concentrations at  $I_{off}$ =1×10<sup>-4</sup>  $\mu$ A/ $\mu$ m and  $V_{DD}$ =0.65V. In figure(b), doping concentrations are gradually increasing from the bottom point to the top point.

#### 4.6 Benchmark

With 0.8nm EOT Al<sub>2</sub>O<sub>3</sub> dielectric,  $L_{un}$ =1nm,  $L_G$ =7nm, n-type doping=4×10<sup>13</sup> cm<sup>-2</sup>, the best performance of the MoS<sub>2</sub> nanosheet transistor is  $I_{on}$ =495  $\mu$ A/ $\mu$ m at  $I_{off}$ =1×10<sup>-4</sup>  $\mu$ A/ $\mu$ m. We compare the MoS<sub>2</sub> nanosheet transistors with Si GAA FETs. Benchmarks of DIBL vs.  $L_G$  and  $I_{DS}$  vs. SS value for Si GAA FETs are shown in figure 4.18 [16, 17, 18, 19, 20, 21, 22, 23, 24, 25]. We define the gate drive voltage  $V_{ov}$ = $V_G$ - $V_{TH}$ .  $V_{TH}$  is the gate bias at which the current density is 0.1  $\mu$ A/ $\mu$ m [16]. In figure 4.18(a), the MoS<sub>2</sub> nanosheet transistor demonstrates very low DIBL and shows good electrostatics. In figure4.18(b), low SS value shows good gate control. Besides gate control, with multiple improvements of the structures and doping,  $I_{on}$  can also reach  $I_{on}$  requirement of the IRDS.



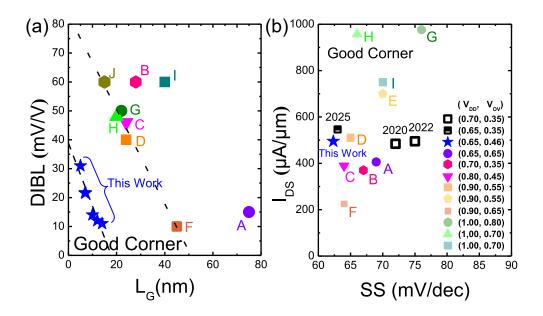


Figure 4.18: Benchmarks of (a) DIBL vs.  $L_G$  and (b)  $I_{DS}$  vs. SS value for Si GAA FETs. Only this work is the  $MoS_2$  nanosheet transistor. The data from this work is labeled by the blue stars. The blue star in (b) is the best  $I_{on}$  in this work. Label A to J corresponds to references [16, 17, 18, 19, 20, 21, 22, 23, 24, 25], respectively.



## Chapter 5

## **Conclusion and Future Work**

In chapter 3, the transport properties of  $MoS_2$  and  $WS_2$  are discussed with the Monte Carlo method. By this method, the intrinsic mobilities of  $MoS_2$  and  $WS_2$  are calculated to be 171 cm<sup>2</sup>/V-s and 83 cm<sup>2</sup>/V-s, respectively.  $\Delta E_{KQ}$  is the critical factor in influencing the transport properties of materials. With smaller  $\Delta E_{KQ}$ , K-to-Q intervalley phonon scattering activates earlier. With six satellite Q valleys, K-to-Q intervalley phonon scattering rate is almost ten times more than the sum of the other intrinsic phonon scattering rate. Transport properties are significantly degraded by K-to-Q intervalley scattering if the scattering mechanism activates too early.

When we design transistors, the dielectric is also an important factor. To pursue low EOT, high- $\kappa$  materials are selected to be dielectrics. However, with high dielectric constant and low-energy phonon mode, the remote phonon scattering from the high- $\kappa$  material degrades the transport a lot. MoS $_2$  stacked between Al $_2$ O $_3$ 

and  $HfO_2$  are 73 cm<sup>2</sup>/V-s and 15 cm<sup>2</sup>/V-s. On the contrary, although hBN and  $SiO_2$  are not suitable for scaling down, they have weak remote phonon scattering.

After discussing the transport properties of MoS<sub>2</sub> and WS<sub>2</sub>, both materials are used as the channels of 2D monolayer nanosheet transistors. Two structures of nanosheet transistors are compared. One structure is the transistor with dual symmetrical gates. The other one is the transisitor with dual gates but a wider bottom gate. With inducing double carriers in the channel and contact, the asymmetrical structure has two times more current at the same  $V_{DD}$ . As for materials of the channels, MoS<sub>2</sub> shows better performance than WS<sub>2</sub> due to a weaker scattering rate,. Because of better performance, the asymmetrical MoS<sub>2</sub> nanosheet is adopted to be optimized. We optimized transistors in several approaches, including  $L_G$ , dielectric,  $L_{un}$ , and doping. For  $L_G$ , scaling down of  $L_G$  is not certain to bring benefits to  $I_{on}$  at limited  $V_{DD}$ . If  $L_G$  shrinks, gate control has the possibility of being degraded too much. Consequently, shrinking  $L_G$  is a trade-off. EOT and materials of the dielectrics are also investigated. Smaller EOT can increase gate control and enhance  $I_{on}$ , but at the same time, gate leakage current must be considered. Furthermore, with weaker remote phonon scattering, Al<sub>2</sub>O<sub>3</sub> is a better choice for the dielectric. As for  $L_{un}$ , shrinking  $L_{un}$  increases  $I_{on}$  but also increases DIBL. At EOT=0.8nm,  $L_G$ =7nm, the transistor is not affected much by DIBL when shrinking  $L_{un}$  to 1nm. At  $V_{DD}$ =0.65V, it can reach 438  $\mu$ A/mum, which is 90 % of the requirement of the IRDS. As for doping, substoichiometric metal oxide doping is selected. AlO<sub>x</sub> dielectric is used to dope undoped MoS<sub>2</sub>. Doping increases  $I_{on}$ 

and doesn't influence the gate control. At a doping level of  $3\times10^{13}$ , nanosheet transistors can reach  $I_{on}$ =483  $\mu$ A/ $\mu$ m, close to the requirement of the 2020 IRDS. At a doping level of  $4\times10^{13}$ , nanosheet transistors can reach  $I_{on}$ =495  $\mu$ A/ $\mu$ m at  $V_{DD}$ =0.65V, meeting  $I_{on}$  requirement of the 2022 IRDS. Comparing with Si GAA FETs, MoS<sub>2</sub> nanosheet transistors show good electrostatics and gate control. After optimization,  $I_{on}$  also reaches the international requirement. As a result, MoS<sub>2</sub> nanosheet transistors indeed have the potential for the future technology.

In the future, there are several ways to enhance the performance of the transistors. The first way is by lowering the intrinsic scattering rates of TMD materials. In the literature, the band structures of  $MoS_2$  and  $WS_2$  are sensitive to strain [94]. With strain applied, it is possible to increase  $\Delta E_{KQ}$  and reduce the influence of the K-to-Q intervalley scattering [75]. By lowering the scattering rate, we can enhance mobilities and enlarge the probability of ballistic transport under a high electric field. Consequently,  $I_{on}$  will increase. Another way is about dielectrics. Although  $Al_2O_3$  is a suitable dielectric,  $HfO_2$  is a more commonly seen material for high-K dielectric because of its high dielectric contant. How to reduce remote phonon scattering caused by  $HfO_2$  becomes an important issue. Bi-layer dielectric, like  $Al_2O_3/HfO_2$ , has been proposed [95]. It might be a promising way to reduce the remote phonon scattering from  $HfO_2$ . For example, we can stack a few layers of hBN between  $MoS_2$  and  $HfO_2$ . With the longer distance between  $MoS_2$  and  $HfO_2$ , the Coulomb force is decreasing and reduce the remote phonon scattering. Therefore, bi-layer dielectric has the possibility to reduce EOT and enhance current.

#### 5. Conclusion and Future Work

66

These improvements have the possibility of enhancing  $I_{on}$  of the 2D transistors and making 2D transistor more suitable for the process and future technology.



### Reference

- [1] L. Yang, K. Majumdar, Y. Du, H. Liu, H. Wu, M. Hatzistergos, P. Hung, R. Tieckelmann, W. Tsai, C. Hobbs *et al.*, "High-performance MoS 2 field-effect transistors enabled by chloride doping: Record low contact resistance (0.5 kΩů μm) and record high drain current (460 μA/μm)," in 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers. IEEE, 2014, pp. 1–2. ix, 9
- [2] M.-C. Chen, K.-S. Li, L.-J. Li, A.-Y. Lu, M.-Y. Li, Y.-H. Chang, C.-H. Lin, Y.-J. Chen, Y.-F. Hou, C.-C. Chen *et al.*, "TMD FinFET with 4 nm thin body and back gate control for future low power technology," in *2015 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2015, pp. 32–2. ix, 9
- [3] A. Nourbakhsh, A. Zubair, A. Tavakkoli, R. Sajjad, X. Ling, M. Dresselhaus, J. Kong, K. Berggren, D. Antoniadis, and T. Palacios, "Serially connected monolayer MoS 2 FETs with channel patterned by a 7.5 nm resolution directed self-assembly lithography," in 2016 IEEE Symposium on VLSI Tech-

nology. IEEE, 2016, pp. 1-2. ix, 9

- [4] S. Park and D. Akinwande, "First demonstration of high performance 2D monolayer transistors on paper substrates," in 2017 IEEE International Electron Devices Meeting (IEDM). IEEE, 2017, pp. 5–2. ix, 4, 9
- [5] C. Huyghebaert, T. Schram, Q. Smets, T. K. Agarwal, D. Verreck, S. Brems, A. Phommahaxay, D. Chiappe, S. El Kazzi, C. L. De La Rosa *et al.*, "2D materials: roadmap to CMOS integration," in 2018 IEEE International Electron Devices Meeting (IEDM). IEEE, 2018, pp. 22–1. ix, 9
- [6] Q. Smets, G. Arutchelvan, J. Jussot, D. Verreck, I. Asselberghs, A. N. Mehta, A. Gaur, D. Lin, S. El Kazzi, B. Groven *et al.*, "Ultra-scaled MOCVD MoS 2 MOSFETs with 42nm contact pitch and 250μA/μm drain current," in 2019 IEEE International Electron Devices Meeting (IEDM). IEEE, 2019, pp. 23–2. ix, 9
- [7] A. S. Chou, P. C. Shen, C. C. Cheng, L. S. Lu, W. C. Chueh, M. Y. Li, G. Pitner, W. H. Chang, C. I. Wu, J. Kong et al., "High On-Current 2D nFET of 390\mu A/\mu m at V<sub>DS</sub>= 1V using Monolayer CVD MoS2 without Intentional Doping," in 2020 IEEE Symposium on VLSI Technology, VLSI Technology 2020. Institute of Electrical and Electronics Engineers Inc., 2020, p. 9265040. ix, 9
- [8] Y.-Y. Chung, K.-C. Lu, C.-C. Cheng, M.-Y. Li, C.-T. Lin, C.-F. Li, J.-H. Chen, T.-Y. Lai, K.-S. Li, J.-M. Shieh *et al.*, "Demonstration of 40-nm Channel

Length Top-Gate p-MOSFET of WS 2 Channel Directly Grown on SiO2/Si Substrates Using Area-Selective CVD Technology," *IEEE Transactions on Electron Devices*, vol. 66, no. 12, pp. 5381–5386, 2019. ix, 9

- [9] C.-S. Pang, P. Wu, J. Appenzeller, and Z. Chen, "Sub-1nm EOT WS 2-FET with I DS; 600μA/μm at V DS= 1V and SS; 70mV/dec at L G= 40nm," in 2020 IEEE International Electron Devices Meeting (IEDM). IEEE, 2020, pp. 3–4. ix, 9, 50
- [10] D. Lin, X. Wu, D. Cott, D. Verreck, B. Groven, S. Sergeant, Q. Smets, S. Sutar, I. Asselberghs, and I. Radu, "Dual gate synthetic WS 2 MOSFETs with  $120\mu\text{S}/\mu\text{m}$  Gm 2.7  $\mu\text{F/cm}$  2 capacitance and ambipolar channel," in 2020 IEEE International Electron Devices Meeting (IEDM). IEEE, 2020, pp. 3–6. ix, 9
- [11] "2020 IRDS roadmap," 2020. ix, xvi, 12, 13
- [12] S.-H. Lo, D. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's," *IEEE Electron Device Letters*, vol. 18, no. 5, pp. 209–211, 1997. xii, 46, 47
- [13] S. Guha, E. Cartier, N. Bojarczuk, J. Bruley, L. Gignac, and J. Karasinski, "High-quality aluminum oxide gate dielectrics by ultra-high-vacuum reactive atomic-beam deposition," *Journal of applied physics*, vol. 90, no. 1, pp. 512–514, 2001. xii, 46, 47

[14] E. Gusev, D. A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P. Jamison, D. Neumayer *et al.*, "Ultrathin high-K gate stacks for advanced CMOS devices," in *International Electron Devices Meeting. Technical Digest (Cat. No. 01CH37224)*. IEEE, 2001, pp. 20–1. xii, 46, 47

- [15] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, M. I. Katsnelson, L. Eaves, S. V. Morozov, A. S. Mayorov, N. M. Peres *et al.*, "Electron tunneling through ultrathin boron nitride crystalline barriers," *Nano letters*, vol. 12, no. 3, pp. 1707–1710, 2012. xii, 46, 47
- [16] C.-Y. Huang, G. Dewey, E. Mannebach, A. Phan, P. Morrow, W. Rachmady, I.-C. Tung, N. Thomas, U. Alaan, R. Paul *et al.*, "3-D Self-aligned stacked NMOS-on-PMOS nanoribbon transistors for continued Moore's law scaling," in 2020 IEEE International Electron Devices Meeting (IEDM). IEEE, 2020, pp. 20–6. xv, 11, 61, 62
- [17] R. Ritzenthaler, H. Mertens, V. Pena, G. Santoro, A. Chasin, K. Kenis, K. Devriendt, G. Mannaert, H. Dekkers, A. Dangol *et al.*, "Vertically stacked gateall-around Si nanowire CMOS transistors with reduced vertical nanowires separation, new work function metal gate solutions, and DC/AC performance optimization," in *2018 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2018, pp. 21–5. xv, 61, 62

[18] S.-G. Hur, J.-G. Yang, S.-S. Kim, D.-K. Lee, T. An, K.-J. Nam, S.-J. Kim, Z. Wu, W. Lee, U. Kwon *et al.*, "A practical Si nanowire technology with nanowire-on-insulator structure for beyond 10nm logic technologies," in *2013 IEEE international electron devices meeting*. IEEE, 2013, pp. 26–5. xv, 61, 62

- [19] H. Mertens, R. Ritzenthaler, A. Hikavyy, M.-S. Kim, Z. Tao, K. Wostyn, S. A. Chew, A. De Keersgieter, G. Mannaert, E. Rosseel *et al.*, "Gate-all-around MOSFETs based on vertically stacked horizontal Si nanowires in a replacement metal gate process on bulk Si substrates," in *2016 IEEE Symposium on VLSI Technology*. IEEE, 2016, pp. 1–2. xv, 61, 62
- [20] H. Mertens, R. Ritzenthaler, A. Chasin, T. Schram, E. Kunnen, A. Hikavyy, L.-Å. Ragnarsson, H. Dekkers, T. Hopf, K. Wostyn *et al.*, "Vertically stacked gate-all-around Si nanowire CMOS transistors with dual work function metal gates," in 2016 IEEE International Electron Devices Meeting (IEDM). IEEE, 2016, pp. 19–7. xv, 61, 62
- [21] S. Barraud, B. Previtali, C. Vizioz, J.-M. Hartmann, J. Sturm, J. Lassarre, C. Perrot, P. Rodriguez, V. Loup, A. Magalhaes-Lucas *et al.*, "7-levels-stacked nanosheet GAA transistors for high performance computing," in 2020 IEEE Symposium on VLSI Technology. IEEE, 2020, pp. 1–2. xv, 61, 62
- [22] S. Bangsaruntip, K. Balakrishnan, S.-L. Cheng, J. Chang, M. Brink, I. Lauer, R. Bruce, S. Engelmann, A. Pyzyna, G. Cohen *et al.*, "Density scaling with

gate-all-around silicon nanowire MOSFETs for the 10 nm node and beyond," in 2013 IEEE international electron devices meeting. IEEE, 2013, pp. 20–2. xv, 61, 62

- [23] I. Lauer, N. Loubet, S. Kim, J. Ott, S. Mignot, R. Venigalla, T. Yamashita, T. Standaert, J. Faltermeier, V. Basker *et al.*, "Si nanowire CMOS fabricated with minimal deviation from RMG FinFET technology showing record performance," in 2015 Symposium on VLSI Technology (VLSI Technology). IEEE, 2015, pp. T140–T141. xv, 61, 62
- [24] A. Veloso, G. Hellings, M. J. Cho, E. Simoen, K. Devriendt, V. Paraschiv, E. Vecchio, Z. Tao, J. Versluijs, L. Souriau *et al.*, "Gate-all-around NWFETs vs. triple-gate FinFETs: Junctionless vs. extensionless and conventional junction devices with controlled EWF modulation for multi-VT CMOS," in 2015 Symposium on VLSI Technology (VLSI Technology). IEEE, 2015, pp. T138–T139. xv, 61, 62
- [25] P. Nguyen, S. Barraud, C. Tabone, L. Gaben, M. Cassé, F. Glowacki, J.-M. Hartmann, M.-P. Samson, V. Maffini-Alvaro, C. Vizioz et al., "Dual-channel CMOS co-integration with Si NFET and strained-SiGe PFET in nanowire device architecture featuring sub-15nm gate length," in 2014 IEEE International Electron Devices Meeting. IEEE, 2014, pp. 16–2. xv, 61, 62
- [26] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically

thin carbon films," science, vol. 306, no. 5696, pp. 666–669, 2004. 1

- [27] H. Sun, X. Liu, Y. Su, B. Deng, H. Peng, S. Decurtins, S. Sanvito, S.-X. Liu, S. Hou, and J. Liao, "Dirac-cone induced gating enhancement in single-molecule field-effect transistors," *Nanoscale*, vol. 11, no. 27, pp. 13117–13125, 2019. 1
- [28] T. Kim, S. Fan, S. Lee, M.-K. Joo, and Y. H. Lee, "High-mobility junction field-effect transistor via graphene/MoS 2 heterointerface," *Scientific reports*, vol. 10, no. 1, pp. 1–8, 2020. 1
- [29] F. Bonaccorso, Z. Sun, T. Hasan, and A. Ferrari, "Graphene photonics and optoelectronics," *Nature photonics*, vol. 4, no. 9, p. 611, 2010. 1
- [30] A. Chaves, J. Azadani, H. Alsalman, D. R. da Costa, R. Frisenda, A. Chaves, S. H. Song, Y. Kim, D. He, J. Zhou et al., "Bandgap engineering of two-dimensional semiconductor materials," npj 2D Materials and Applications, vol. 4, no. 1, pp. 1–21, 2020. 2
- [31] P. Zhao, S. Desai, M. Tosun, T. Roy, H. Fang, A. Sachid, M. Amani, C. Hu, and A. Javey, "2D layered materials: From materials properties to device applications," in 2015 IEEE International Electron Devices Meeting (IEDM). IEEE, 2015, pp. 27–3. 2

[32] T. Mueller and E. Malic, "Exciton physics and device application of two-dimensional transition metal dichalcogenide semiconductors," *npj 2D Materials and Applications*, vol. 2, no. 1, pp. 1–12, 2018. 2

- [33] S.-F. Chen and Y.-R. Wu, "A design of intermediate band solar cell for photon ratchet with multi-layer MoS2 nanoribbons," *Applied Physics Letters*, vol. 110, no. 20, p. 201109, 2017. 2
- [34] M. Donarelli and L. Ottaviano, "2D materials for gas sensing applications: A review on graphene oxide, MoS2, WS2 and phosphorene," *Sensors*, vol. 18, no. 11, p. 3638, 2018. 2
- [35] N. Huo, Y. Yang, and J. Li, "Optoelectronics based on 2D TMDs and heterostructures," *Journal of Semiconductors*, vol. 38, no. 3, p. 031002, 2017. 2, 3
- [36] N. Huo, S. Yang, Z. Wei, S.-S. Li, J.-B. Xia, and J. Li, "Photoresponsive and gas sensing field-effect transistors based on multilayer WS 2 nanoflakes," *Scientific reports*, vol. 4, p. 5209, 2014. 2
- [37] H. Liu, A. T. Neal, and P. D. Ye, "Channel length scaling of MoS2 MOSFETs," *ACS nano*, vol. 6, no. 10, pp. 8563–8569, 2012. 3, 7
- [38] S. B. Desai, S. R. Madhvapathy, A. B. Sachid, J. P. Llinas, Q. Wang, G. H. Ahn, G. Pitner, M. J. Kim, J. Bokor, C. Hu *et al.*, "Mos2 transistors with 1-nanometer gate lengths," *Science*, vol. 354, no. 6308, pp. 99–102, 2016. 3

[39] A. Nourbakhsh, A. Zubair, R. N. Sajjad, A. Tavakkoli KG, W. Chen, S. Fang, X. Ling, J. Kong, M. S. Dresselhaus, E. Kaxiras *et al.*, "MoS2 field-effect transistor with sub-10 nm channel length," *Nano letters*, vol. 16, no. 12, pp. 7798–7806, 2016. 3

- [40] Z. Yu, H. Wang, W. Li, S. Xu, X. Song, S. Wang, P. Wang, P. Zhou, Y. Shi, Y. Chai *et al.*, "Negative capacitance 2D MoS 2 transistors with sub-60mV/dec subthreshold swing over 6 orders, 250 μA/μm current density, and nearly-hysteresis-free," in 2017 IEEE International Electron Devices Meeting (IEDM). IEEE, 2017, pp. 23–6. 3, 4
- [41] C.-H. Wang, C. McClellan, Y. Shi, X. Zheng, V. Chen, M. Lanza, E. Pop, and H.-S. P. Wong, "3D monolithic stacked 1T1R cells using monolayer MoS 2 FET and hBN RRAM fabricated at low (150 C) temperature," in 2018 IEEE International Electron Devices Meeting (IEDM). IEEE, 2018, pp. 22–5. 4
- [42] R. Yang, H. Li, K. K. Smithe, T. R. Kim, K. Okabe, E. Pop, J. A. Fan, and H.-S. P. Wong, "2D molybdenum disulfide (MoS 2) transistors driving RRAMs with 1T1R configuration," in 2017 IEEE International Electron Devices Meeting (IEDM). IEEE, 2017, pp. 19–5. 4
- [43] J. Li, J. Li, Y. Ding, C. Liu, X. Hou, H. Chen, Y. Xiong, D. W. Zhang, Y. Chai, and P. Zhou, "Highly Area-Efficient Low-Power SRAM Cell with 2 Transistors and 2 Resistors," in 2019 IEEE International Electron Devices Meeting (IEDM). IEEE, 2019, pp. 23–3. 4

[44] P. Solís-Fernández, M. Bissett, and H. Ago, "Synthesis, structure and applications of graphene-based 2D heterostructures," *Chemical Society Reviews*, vol. 46, no. 15, pp. 4572–4613, 2017. 5

- [45] T. Kim, S. Fan, S. Lee, M.-K. Joo, and Y. H. Lee, "High-mobility junction field-effect transistor via graphene/MoS 2 heterointerface," *Scientific reports*, vol. 10, no. 1, pp. 1–8, 2020. 5
- [46] Y. Huang, E. Sutter, N. N. Shi, J. Zheng, T. Yang, D. Englund, H.-J. Gao, and P. Sutter, "Reliable exfoliation of large-area high-quality flakes of graphene and other two-dimensional materials," *ACS nano*, vol. 9, no. 11, pp. 10612–10620, 2015. 5
- [47] P.-C. Shen, Y. Lin, H. Wang, J.-H. Park, W. S. Leong, A.-Y. Lu, T. Palacios, and J. Kong, "CVD technology for 2-D materials," *IEEE Transactions on Electron Devices*, vol. 65, no. 10, pp. 4040–4052, 2018. 5
- [48] K.-K. Liu, W. Zhang, Y.-H. Lee, Y.-C. Lin, M.-T. Chang, C.-Y. Su, C.-S. Chang, H. Li, Y. Shi, H. Zhang *et al.*, "Growth of large-area and highly crystalline MoS2 thin layers on insulating substrates," *Nano letters*, vol. 12, no. 3, pp. 1538–1544, 2012. 6
- [49] Y. Zhan, Z. Liu, S. Najmaei, P. M. Ajayan, and J. Lou, "Large-area vapor-phase growth and characterization of MoS2 atomic layers on a SiO2 substrate," *Small*, vol. 8, no. 7, pp. 966–971, 2012. 6

[50] C. Lan, Z. Zhou, Z. Zhou, C. Li, L. Shu, L. Shen, D. Li, R. Dong, S. Yip, and J. C. Ho, "Wafer-scale synthesis of monolayer WS 2 for high-performance flexible photodetectors by enhanced chemical vapor deposition," *Nano Research*, vol. 11, no. 6, pp. 3371–3384, 2018. 6

- [51] H. Xu, H. Zhang, Z. Guo, Y. Shan, S. Wu, J. Wang, W. Hu, H. Liu, Z. Sun, C. Luo *et al.*, "High-performance wafer-scale MoS2 transistors toward practical application," *Small*, vol. 14, no. 48, p. 1803465, 2018. 6, 7
- [52] Z. Jin, X. Li, J. T. Mullen, and K. W. Kim, "Intrinsic transport properties of electrons and holes in monolayer transition-metal dichalcogenides," *Physical Review B*, vol. 90, no. 4, p. 045422, 2014. 6, 7, 35, 86
- [53] X. Li, J. T. Mullen, Z. Jin, K. M. Borysenko, M. B. Nardelli, and K. W. Kim, "Intrinsic electrical transport properties of monolayer silicene and MoS 2 from first principles," *Physical Review B*, vol. 87, no. 11, p. 115418, 2013. 7, 17
- [54] T. Sohier, D. Campi, N. Marzari, and M. Gibertini, "Mobility of twodimensional materials from first principles in an accurate and automated framework," *Physical Review Materials*, vol. 2, no. 11, p. 114010, 2018.
- [55] E. Pascual, J. M. Iglesias, M. J. Martín, and R. Rengel, "Electronic transport and noise characterization in MoS2," *Semiconductor Science and Technology*, vol. 35, no. 5, p. 055021, 2020. 7

[56] A. T. Neal, H. Liu, J. Gu, and P. D. Ye, "Magneto-transport in MoS2: phase coherence, spin-orbit scattering, and the hall factor," *Acs Nano*, vol. 7, no. 8, pp. 7077–7082, 2013. 7

- [57] M. Hosseini, M. Elahi, M. Pourfath, and D. Esseni, "Strain induced mobility modulation in single-layer MoS2," *Journal of Physics D: Applied Physics*, vol. 48, no. 37, p. 375104, 2015. 7
- [58] Y. Lee, S. Fiore, and M. Luisier, "Ab initio mobility of single-layer MoS 2 and WS 2: comparison to experiments and impact on the device characteristics," in 2019 IEEE International Electron Devices Meeting (IEDM). IEEE, 2019, pp. 24–4. 7
- [59] Z. Yu, Y. Zhu, W. Li, Y. Shi, G. Zhang, Y. Chai, and X. Wang, "Toward High-mobility and Low-power 2D MoS 2 Field-effect Transistors," in 2018

  IEEE International Electron Devices Meeting (IEDM). IEEE, 2018, pp. 22–4. 7
- [60] G. Gaddemane, S. Gopalan, M. L. Van de Put, and M. V. Fischetti, "Limitations of ab initio methods to predict the electronic-transport properties of two-dimensional semiconductors: the computational example of 2H-phase transition metal dichalcogenides," *Journal of Computational Electronics*, vol. 20, no. 1, pp. 49–59, 2021. 7

[61] D. Braga, I. Gutierrez Lezama, H. Berger, and A. F. Morpurgo, "High-performance monolayer WS2 field-effect transistors on high- $\kappa$  dielectrics," *Nano letters*, vol. 12, no. 10, pp. 5218–5223, 2012. 7

- [62] S. Jo, N. Ubrig, H. Berger, A. B. Kuzmenko, and A. F. Morpurgo, "Monoand bilayer WS2 light-emitting transistors," *Nano letters*, vol. 14, no. 4, pp. 2019–2025, 2014. 7
- [63] Y. Cui, R. Xin, Z. Yu, Y. Pan, Z.-Y. Ong, X. Wei, J. Wang, H. Nan, Z. Ni, Y. Wu et al., "High-performance monolayer WS2 field-effect transistors on high-κ dielectrics," Advanced Materials, vol. 27, no. 35, pp. 5230–5234, 2015. 7
- [64] J. Singh, Electronic and optoelectronic properties of semiconductor structures.Cambridge University Press, 2007. 7, 22
- [65] N. Ma and D. Jena, "Charge scattering and mobility in atomically thin semi-conductors," *Physical Review X*, vol. 4, no. 1, p. 011043, 2014. 8
- [66] N. Loubet, T. Hook, P. Montanini, C.-W. Yeung, S. Kanakasabapathy, M. Guillom, T. Yamashita, J. Zhang, X. Miao, J. Wang *et al.*, "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," in *2017 Symposium on VLSI Technology*. IEEE, 2017, pp. T230–T231. 10
- [67] X. Huang, C. Liu, Z. Tang, S. Zeng, L. Liu, X. Hou, H. Chen, J. Li, Y.-G. Jiang, D. W. Zhang *et al.*, "High Drive and Low Leakage Current MBC FET

with Channel Thickness 1.2 nm/0.6 nm," in 2020 IEEE International Electron Devices Meeting (IEDM). IEEE, 2020, pp. 12–1. 11, 44

- [68] N. Ma and D. Jena, "Charge scattering and mobility in atomically thin semi-conductors," *Physical Review X*, vol. 4, no. 1, p. 011043, 2014. 20, 40, 42, 46
- [69] B. Hu, "Screening-induced surface polar optical phonon scattering in dual-gated graphene field effect transistors," *Physica B: Condensed Matter*, vol. 461, pp. 118–121, 2015. 20, 21
- [70] I.-T. Lin and J.-M. Liu, "Surface polar optical phonon scattering of carriers in graphene on various substrates," *Applied Physics Letters*, vol. 103, no. 8, p. 081606, 2013. 21
- [71] A. Ghis, E. Constant, and B. Boittiaux, "Ballistic and overshoot electron transport in bulk semiconductors and in submicronic devices," *Journal of applied physics*, vol. 54, no. 1, pp. 214–221, 1983. 26
- [72] J.-Y. Huang, E.-W. Chang, and Y.-R. Wu, "Optimization of MAPbI \_3-Based Perovskite Solar Cell With Textured Surface," *IEEE Journal of Photovoltaics*, vol. 9, no. 6, pp. 1686–1692, 2019. 30
- [73] T.-Y. Tsai, K. Michalczewski, P. Martyniuk, C.-H. Wu, and Y.-R. Wu, "Application of localization landscape theory and the k· p model for direct modeling

of carrier transport in a type II superlattice InAs/InAsSb photoconductor system," *Journal of Applied Physics*, vol. 127, no. 3, p. 033104, 2020. 30

- [74] S. Smidstrup, T. Markussen, P. Vancraeyveld, J. Wellendorff, J. Schneider, T. Gunst, B. Verstichel, D. Stradi, P. A. Khomyakov, U. G. Vej-Hansen et al., "QuantumATK: An integrated platform of electronic and atomic-scale modelling tools," J. Phys: Condens. Matter, vol. 32, p. 015901, 2020. 31
- [75] M. Hosseini, M. Elahi, M. Pourfath, and D. Esseni, "Strain-Induced Modulation of Electron Mobility in Single-Layer Transition Metal Dichalcogenides MX 2," *IEEE Transactions on Electron Devices*, vol. 62, no. 10, pp. 3192–3198, 2015. 32, 35, 65
- [76] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-κ insulator: The role of remote phonon scattering," *Journal of Applied Physics*, vol. 90, no. 9, pp. 4587–4608, 2001. 42
- [77] L. Zeng, Z. Xin, S. Chen, G. Du, J. Kang, and X. Liu, "Remote phonon and impurity screening effect of substrate and gate dielectric on electron dynamics in single layer MoS2," *Applied Physics Letters*, vol. 103, no. 11, p. 113505, 2013. 42
- [78] M. Okada, N. Okada, W.-H. Chang, T. Endo, A. Ando, T. Shimizu, T. Kubo, Y. Miyata, and T. Irisawa, "Gas-source CVD growth of atomic layered WS 2

from WF 6 and H 2 S precursors with high grain size uniformity," *Scientific reports*, vol. 9, no. 1, pp. 1–10, 2019. 44

- [79] Y. Wu, Y.-m. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhu, and P. Avouris, "High-frequency, scaled graphene transistors on diamond-like carbon," *Nature*, vol. 472, no. 7341, pp. 74–78, 2011. 45
- [80] A. Sanne, R. Ghosh, A. Rai, M. N. Yogeesh, S. H. Shin, A. Sharma, K. Jarvis, L. Mathew, R. Rao, D. Akinwande *et al.*, "Radio frequency transistors and circuits based on CVD MoS2," *Nano letters*, vol. 15, no. 8, pp. 5039–5045, 2015. 45
- [81] J. Robertson and R. M. Wallace, "High-K materials and metal gates for CMOS applications," *Materials Science and Engineering: R: Reports*, vol. 88, pp. 1–41, 2015. 46
- [82] T. Knobloch, Y. Y. Illarionov, F. Ducry, C. Schleich, S. Wachter, T. Müller, M. Waltl, M. Lanza, M. I. Vexler, M. Luisier et al., "On the suitability of hBN as an insulator for 2D material-based ultrascaled CMOS devices," arXiv preprint arXiv:2008.04144, 2020. 46
- [83] S. Walia, S. Balendhran, Y. Wang, R. Ab Kadir, A. Sabirin Zoolfakar, P. Atkin, J. Zhen Ou, S. Sriram, K. Kalantar-Zadeh, and M. Bhaskaran, "Characterization of metal contacts for two-dimensional MoS2 nanoflakes," *Applied Physics Letters*, vol. 103, no. 23, p. 232105, 2013. 46

[84] T. Yamaguchi, R. Moriya, Y. Inoue, S. Morikawa, S. Masubuchi, K. Watanabe, T. Taniguchi, and T. Machida, "Tunneling transport in a few monolayer-thick WS2/graphene heterojunction," *Applied Physics Letters*, vol. 105, no. 22, p. 223109, 2014. 46

- [85] T. Ando, N. D. Sathaye, K. V. Murali, and E. A. Cartier, "On the Electron and Hole Tunneling in a HfO2 Gate Stack With Extreme Interfacial-Layer Scaling," *IEEE electron device letters*, vol. 32, no. 7, pp. 865–867, 2011. 46
- [86] T. Cheiwchanchamnangij and W. R. Lambrecht, "Quasiparticle band structure calculation of monolayer, bilayer, and bulk MoS 2," *Physical Review B*, vol. 85, no. 20, p. 205302, 2012. 46
- [87] A. Hichri, I. B. Amara, S. Ayari, and S. Jaziri, "Dielectric environment and/or random disorder effects on free, charged and localized excitonic states in monolayer WS2," *Journal of Physics: Condensed Matter*, vol. 29, no. 43, p. 435305, 2017. 46
- [88] W. Li, J. Zhou, S. Cai, Z. Yu, J. Zhang, N. Fang, T. Li, Y. Wu, T. Chen, X. Xie *et al.*, "Uniform and ultrathin high-κ gate dielectrics for two-dimensional electronic devices," *Nature Electronics*, vol. 2, no. 12, pp. 563–571, 2019. 53
- [89] Y.-C. Yeo, T.-J. King, and C. Hu, "MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations," *IEEE Transactions on Electron Devices*, vol. 50, no. 4, pp. 1027–1035, 2003.

[90] H. Zhang, B. Shi, L. Xu, J. Yan, W. Zhao, Z. Zhang, Z. Zhang, and J. Lu, "Sub-5 nm Monolayer MoS2 Transistors toward Low-Power Devices," ACS Applied Electronic Materials, vol. 3, no. 4, pp. 1560–1571, 2021. 55

- [91] A. Leonhardt, D. Chiappe, V. V. Afanas' ev, S. El Kazzi, I. Shlyakhov, T. Conard, A. Franquet, C. Huyghebaert, and S. de Gendt, "Material-Selective Doping of 2D TMDC through Al x O y Encapsulation," ACS applied materials & interfaces, vol. 11, no. 45, pp. 42 697–42 707, 2019. 57
- [92] K. Xu, Y. Wang, Y. Zhao, and Y. Chai, "Modulation doping of transition metal dichalcogenide/oxide heterostructures," *Journal of Materials Chemistry C*, vol. 5, no. 2, pp. 376–381, 2017. 57
- [93] C. J. McClellan, E. Yalon, K. K. Smithe, S. V. Suryavanshi, and E. Pop, "High Current Density in Monolayer MoS2 Doped by AlO x," *ACS nano*, vol. 15, no. 1, pp. 1587–1596, 2021. 57, 58
- [94] S.-F. Chen and Y.-R. Wu, "Electronic properties of MoS2 nanoribbon with strain using tight-binding method," *physica status solidi* (*b*), vol. 254, no. 2, p. 1600565, 2017. 65
- [95] X. Zou, J. Xu, H. Huang, Z. Zhu, H. Wang, B. Li, L. Liao, and G. Fang, "A comparative study on top-gated and bottom-gated multilayer MoS2 transistors with gate stacked dielectric of Al2O3/HfO2," *Nanotechnology*, vol. 29, no. 24, p. 245201, 2018. 65



# **Appendices**



# **Appendix A**

# **Deformation potential constants for**

# $MoS_2$ and $WS_2$

Deformation potential constants of  $MoS_2$  and  $WS_2$  in first brillouin are given in Table A.1 and Table A.2 [52]. In the tables, "ac" means acousite phonon and "dp" means deformation potential optical phonon.

Table A.1: Deformation potential constants for electron-phonon interaction in the conduction band of K and Q valleys.

				* POTO 101(0)
Transition	Phonon mode	Phonon energy (meV)	$MoS_2$	Units
$K \to K$	ac, $\Gamma$	0	4.5	eV
	dp, $\Gamma$	49.5	5.8	10 <sup>8</sup> eV/cm
$K \to K \text{'}$	ac, K	26.1	1.4	10 <sup>8</sup> eV/cm
	dp, K	46.8	2.0	10 <sup>8</sup> eV/cm
$K \to Q$	ac, Q	20.7	0.93	10 <sup>8</sup> eV/cm
	dp, Q	48.1	1.9	10 <sup>8</sup> eV/cm
$K \rightarrow Q$	ac, M	24.2	4.4	10 <sup>8</sup> eV/cm
	dp, M	47.5	5.6	10 <sup>8</sup> eV/cm
$\text{Q1} \rightarrow \text{Q1}$	ас, Г	0	2.8	eV
	dp, $\Gamma$	49.5	7.1	10 <sup>8</sup> eV/cm
$Q1 \rightarrow Q2(Q6)$	ac, Q	20.7	2.1	10 <sup>8</sup> eV/cm
	dp, Q	48.1	4.8	10 <sup>8</sup> eV/cm
$\text{Q1} \rightarrow \text{Q3}(\text{Q5})$	ac, M	24.2	2.0	10 <sup>8</sup> eV/cm
	dp, M	47.5	4.0	10 <sup>8</sup> eV/cm
$\text{Q1} \rightarrow \text{Q4}$	ac, K	26.1	4.8	10 <sup>8</sup> eV/cm
	dp, K	46.8	6.5	10 <sup>8</sup> eV/cm
$\text{Q1} \rightarrow \text{K}$	ac, Q	20.7	1.5	10 <sup>8</sup> eV/cm
	dp, Q	48.1	2.4	10 <sup>8</sup> eV/cm
$\text{Q1} \rightarrow \text{K'}$	ac, M	24.2	4.4	10 <sup>8</sup> eV/cm
	dp, M	47.5	6.6	10 <sup>8</sup> eV/cm

Table A.2: Deformation potential constants for electron-phonon interaction in the conduction band of K and Q valleys.

				~9J9J6J
Transition	Phonon mode	Phonon energy (meV)	$WS_2$	Units
${\rm K} \to {\rm K}$	ac, $\Gamma$	0	3.2	eV
	dp, $\Gamma$	46.8	3.1	10 <sup>8</sup> eV/cm
$K \to K \text{'}$	ac, K	45.0	1.4	10 <sup>8</sup> eV/cm
	dp, K	45.0	1.1	10 <sup>8</sup> eV/cm
$\mathbf{K} \to \mathbf{Q}$	ac, Q	20.7	0.93	10 <sup>8</sup> eV/cm
	dp, Q	45.9	1.6	10 <sup>8</sup> eV/cm
$K \to Q \textrm{'}$	ac, M	24.2	4.4	10 <sup>8</sup> eV/cm
	dp, M	45.8	4.7	10 <sup>8</sup> eV/cm
$\text{Q1} \rightarrow \text{Q1}$	ас, Г	0	1.8	eV
	dp, $\Gamma$	46.8	3.4	10 <sup>8</sup> eV/cm
$\text{Q1} \rightarrow \text{Q2}(\text{Q6})$	ac, Q	17.7	1.7	10 <sup>8</sup> eV/cm
	dp, Q	45.9	2.3	10 <sup>8</sup> eV/cm
$\text{Q1} \rightarrow \text{Q3}(\text{Q5})$	ac, M	19.6	1.5	10 <sup>8</sup> eV/cm
	dp, M	45.8	1.9	10 <sup>8</sup> eV/cm
$\text{Q1} \rightarrow \text{Q4}$	ac, K	20.5	3.7	10 <sup>8</sup> eV/cm
	dp, K	45.0	3.1	10 <sup>8</sup> eV/cm
$\text{Q1} \rightarrow \text{K}$	ac, Q	17.7	1.4	10 <sup>8</sup> eV/cm
	dp, Q	45.9	1.3	10 <sup>8</sup> eV/cm
$\text{Q1} \rightarrow \text{K'}$	ac, M	19.6	4.0	10 <sup>8</sup> eV/cm
	dp, M	45.8	4.6	10 <sup>8</sup> eV/cm