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低功耗三角積分時間至數位轉換器

Delta-Sigma Time-to-Digital Converters for Low Power Applications

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本論文係張智凱君（R03943042）在國立臺灣大學電子工程學研究所完成之碩士學位論文，於民國 105 年 7 月 18 日承下列考試委員審查通過及口試及格，特此證明

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Delta-Sigma Time-to-Digital Converters for Low Power Applications

By

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THESIS

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摘要

此論文中闡述了低功耗的三角積分時間至數位轉換器的設計技巧，以時間暫存器來傳遞時域的量化誤差來達到高解析度的時間至數位轉換器。利用 90-nm CMOS 製程，所提出的一階三角積分時間至數位轉換器，操作在 0.3 伏特的情況下，晶片功耗為 1.5 微瓦，並且在 50k 赫茲的頻寬內有效位元數(ENOB)為 10.9 位元。此外，進一步利用相同的設計技巧實現二階的三角積分時間至數位轉換器，並以此時間至數位轉換器應用至電容式感測器介面電路，操作在 0.6 伏特的情況下，晶片功耗為 11 微瓦，此電容式感測器介面電路輸入電容範圍為 0~5 皮法拉，並在 2k 赫茲的頻寬內效位元數(ENOB)為 9.8 位元。

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Abstract

The thesis presents low power design techniques for delta-sigma time-to-digital (TDC) converters. By using time register to transfer the time-domain quantization error, the resolution of the TDC can be improved due to noise-shaping of the quantization error. Fabricated in 90-nm CMOS, the first-order delta-sigma TDC consumes a current of 5 μA from a 0.3-V supply. The circuit demonstrates an equivalent number of bits (ENOB) of 10.9 bits in 50 kHz signal bandwidth. Moreover, a capacitance-to-digital (CDC) converter with a second-order delta-sigma TDC is also presented. Consuming 18.4 μA from a 0.6-V supply, the second-order CDC achieves an ENOB of 9.8 bits in 2 kHz signal bandwidth with an input capacitance range of 5 pF.

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Chapter 1

Introduction

1.1 Motivation

In recent years, CMOS has become more attractive due to its low cost in volume and inherent capability in high level integration. Since the progress of CMOS process is driven by the digital circuits, the device size decreases in advance CMOS technology. This progress results in a reduction of the transistor gate-oxide thickness, thus, lower operation voltage of the transistors. Due to the lower operation voltage, the intrinsic gain of a single transistor becomes lower and so as the input voltage range. As a result, the analog design becomes more challenge in nanotechnology.

To lower the design challenge of the analog design, digital-assisted analog design becomes more important. Therefore, time-mode signal processing (TMSP) gains more interest. Using TMSP, conventional representation of the signal in voltage domain is replaced by representation of the signal in time domain. Thus, the signal is represented by the time difference between two signal rising edge. Exploiting the time-mode operation, many power-hungry and large area analog circuits can be replaced by digital circuits. On the other hand, layout of highly digital circuits can be automatically generated by digital synthesis. Therefore, various architecture of the time-to-digital

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converters have been published to accomplished a more energy efficient and cost effective system. Since the gate delay increases as supply voltage decreases, the resolution of a conventional delay-line based TDC is proportional to the supply voltage. A higher supply voltage is needed to enhance the resolution of a delay-line based TDC which results in higher power consumption. Other approaches such as successive approximation (SAR) and two-step TDC have published to achieve higher resolution without raising the supply voltage. However, complex calibration is needed to overcome the PVT variation and process mismatch because of analog parameter dependency of these TDC. In addition to these TDCs, ΔΣ TDC paves a way to achieve sub-gate delay resolution without calibration. Several ΔΣ TDC has been published to achieve more energy efficient ΔΣ TDC. In this thesis, ΔΣ TDC design techniques are proposed to enhance the TDC performance and a capacitance-to-digital converter (CDC) is fabricated with a proposed second-order ΔΣ TDC using the proposed techniques.

1.2 Thesis organization

This thesis is organized as follows. In Chapter 2, the background of the TDC, and several prior arts of the TDC circuits with an emphasis on ΔΣ TDC is provided. In Chapter 3, a noise-shaping TDC with gated-ring oscillator is presented. By exploiting gated-free operation, the timing error associated with charge injection and leakage from the oscillator can be reduced. As a result, the proposed architecture achieves higher resolution in low power design. Based-on Chapter 3, a capacitance-to-digital converter with a low power second-order ΔΣ TDC is proposed in Chapter 4. Finally, a conclusion is provided in the Chapter 5.

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Chapter 2

Background

2.1 Applications

Time-to-digital converter (TDC) has been used in a wide variety applications such as all-digital phase-locked loops (ADPLL), biomedical imaging time-of-flight (ToF) positron emission tomography (PET), fluorescence life time imaging microscopy (FLIM) and ToF range finding.

In biomedical imaging or range finding applications, TDC often integrated with single-photo avalanche diode (SPAD). For PET application, the TDC is used to detect two gamma rays from the annihilation events that happened in a patient's body. Detecting the time difference between the two gamma rays to analysis the location of the emission, the TDC resolution directly impact the signal-to-noise ratio (SNR) of the image.

Another important application for the TDC is FLIM. In this application, the TDC detects the decay time of the fluorophore. One can obtaine the chemical or physical properties depending on the lifetime of the fluorophore. In general, the lifetime of fluorophore ranging from nanosecond to millisecond. However, the fluorophore lifetime is sensitive to environment interference and is decreased by the interference. Therefore, the typical TDC for FLIM application is designed to have about 50 ps resolution with

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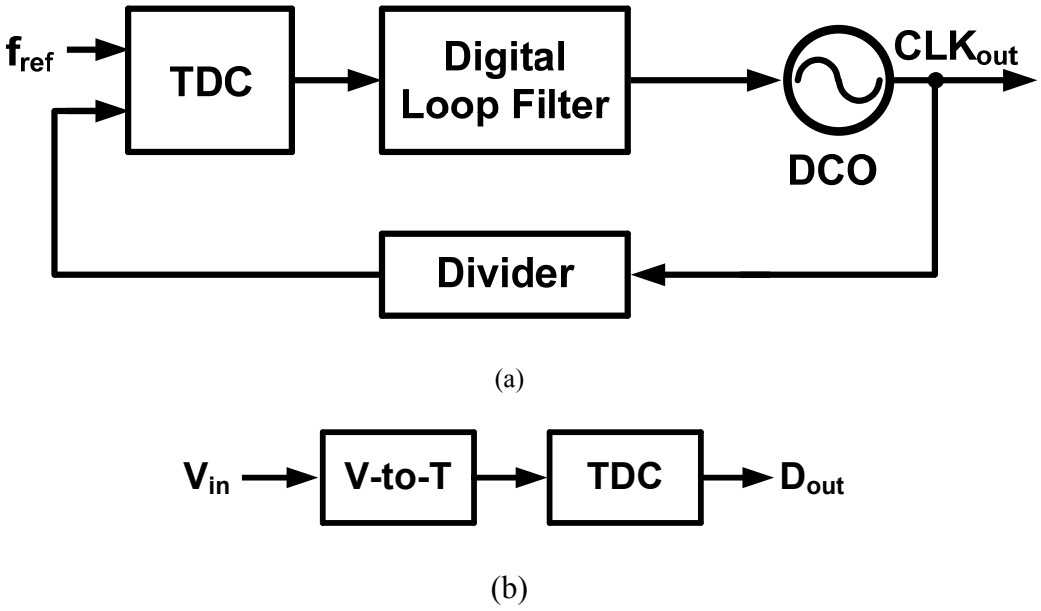

(a)

(b)

Fig. 2.1. (a) General architecture of ADPLL (b) and time-mode ADC.

50 ns dynamic range. Moreover, since the deadtime of the SPAD is reduced to nanosecond. The deadtime of the TDC becomes the main issue in the FLIM application.

The TDC also plays an important role in ADPLL since it can replace the traditional analog intensive phase detector and charge pump as shown in Fig 2.1 (a). The highly digital architecture can simplify the design complexity of the circuits in advance CMOS technology and can utilize digital loop filter instead of the area consuming RC loop filter. The programmability of the loop parameter is also an attractive advantage for the ADPLL design. In the ADPLL application, the trend for the TDC is to achieve high resolution since the resolution of the TDC dominates the in-band phase noise of the ADPLL. The single-sided noise power spectral density S_{TDC} is givn by

$$S_{TDC}(f) = \frac{2}{f_{ref}} \frac{(2\pi \cdot f_{out} \cdot \tau_{tdc})^2}{12} \left(\frac{\sin(\pi f / f_{ref})}{\pi f / f_{ref}} \right)^2 \qquad (2.1.1)$$

where f_{ref} is the reference frequency, f_{out} the ADPLL output frequency, and τ_{tdc} the TDC resolution. The TDC should have large dynamic range to detect large phase error.

In recent years, time mode signal processing (TMSP) also gains more interest because

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of the difficulties in design analog circuits at low operation voltage. Fig 2.1 (b) shows an example of time-mode analog-to-digital converter which is composed of a voltage-to-time converter and a time-to-digital converter.

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2.2 Performance metrics of TDC

2.2.1 Static performance

The static input-output behavior of an ideal TDC is given by a quantization characteristic as shown in Fig 2.2. The term quantization characteristic means that a continuous time inputs being mapped to the digital words. The step width of the quantization characteristic (T_{LSB}) is the least significant bit (LSB) of a TDC, which means the range of the time interval being mapped to a single digital word. Different from an ideal TDC that the first step occurs at the position $T_{00\ldots01} = T_{LSB}$, the first step and the complete characteristic of a practical TDC might be shifted along the time axis. The converter is said to have an offset error if the characteristic is shifted. In general, the gain of a ideal TDC k_{TDC} is the steepness of the quantization characteristic which shown as the slope of the dot line in Fig 2.2. For a practical TDC, the gain may be varied from its ideal value. The variation of the gain is quantified by the gain error E_{gain}, which can be expressed as

$$E_{gain} = \frac{1}{T_{LSB}}(T_{11\ldots11} - T_{00\ldots01}) - (2^N - 2). \quad (2.2.1)$$

It should be noted that the offset and gain error of the converter can be modeled by an additive or multiplicative term to the input time interval, so those errors do not cause non-linear distortion.

Non-linear imperfection in a TDC is its deviation of the quantization characteristic from its ideal shape and can be specified through the differential nonlinearity (DNL) and the integral nonlinearity (INL). DNL is defined as the difference between the actual and the ideal step widths in the quantization characteristic The INL is a macroscopic description of the arching of the quantization characteristic which defined as the

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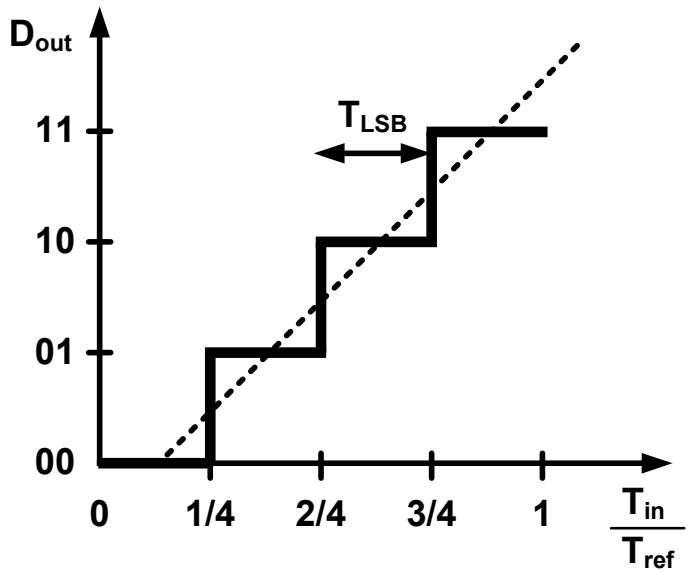

Fig. 2.2. Quantization characteristic of the TDC.

deviation of the step position from its ideal value normalized to one T_{LSB}. The ideal value is defined by a straight line that can be a line connecting the first and the last step or a best fit line. Usually, DNL and INL are normalized to one T_{LSB}.

2.2.2 Dynamics performance

For the static performance of the converter multiple measurement are average thus that any noise can be removed from the measurement results. For practical use, the noise can't be neglected and reduces the effective resolution. For classical analog-to-digital converter, the dynamics performance is verified by applying a sinusoidal signal and evaluating the output spectrum. The resulting spectrum contains a peak at signal frequency and smaller peaks at multiples of the signal frequency and a noise floor. The smaller peaks are cause by the non-linear imperfections of the converter and the noise floor results from both quantization and physical noise. The signal-to-noise-and-distortion ratio is (SNDR) defined by

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$$SNDR = 10 \cdot log\left(\frac{P_{\text{signal}}}{P_{\text{noise.floor}} + P_{\text{non-linear}}}\right). \quad (2.2.2)$$

For TDC measurement, the problem is that it is hard to generate a time domain sinusoidal waveform with an accuracy better than the TDC. Thus, the single-shot precision (SSP) test is used to test the TDC. Instead of applying a sinusoidal time interval to the TDC, the SSP test is done by applying a fixed time interval *T* repeatedly to the TDC. The TDC would produce the same output in each measurement without noise. However, noise causes the variation of the measurement results. The standard deviation of the output is the SSP results of the TDC which describes the capability of a TDC to reproduce the measurement in the presence of noise. In general, the single-shot precision depends on the measured time interval. The reason for this is that the delay along delay line is the accumulated gate delay of the delay cell and each delay element contributes certain delay variation. The longer measured time interval the more delay cells are used and contribute to the overall timing variation.

Due to the fact that the SNR of a TDC is hard to be measured, the definition of a TDC dynamic range is not the same as the ADCs. Therefore, the dynamic range of the TDC is simply defined as the maximum time interval that can be measured.

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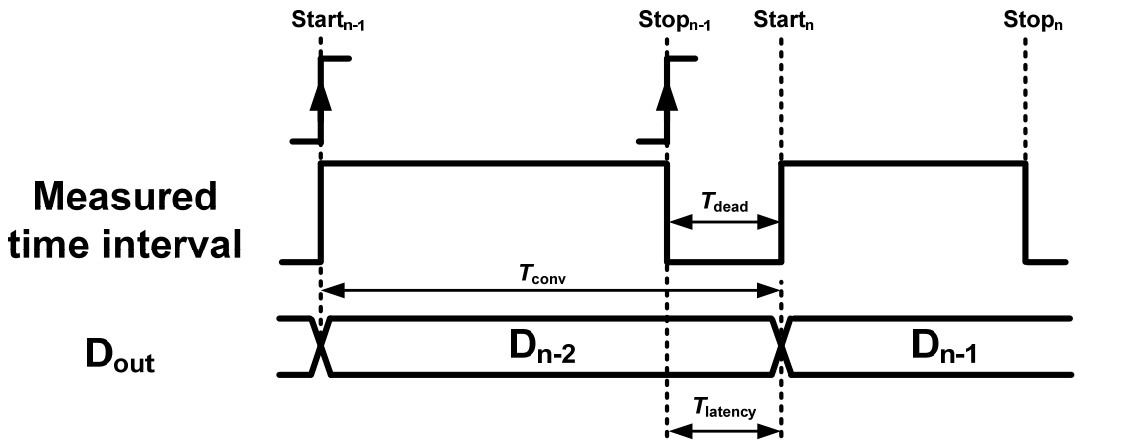

Fig. 2.3. Timing figure of the time-to-digital conversion.

2.2.3 Counting rate and dead time

It is apparently that the measurement of a time interval takes time. The time between the start event and output of the measurement result is specified as the conversion time T_{conv} and time between the stop events and the output results is called latency $T_{latency}$ as shown in Fig 2.3. The time for a TDC to start a new measurement after the end of the previous measurement is called dead time T_{dead}.

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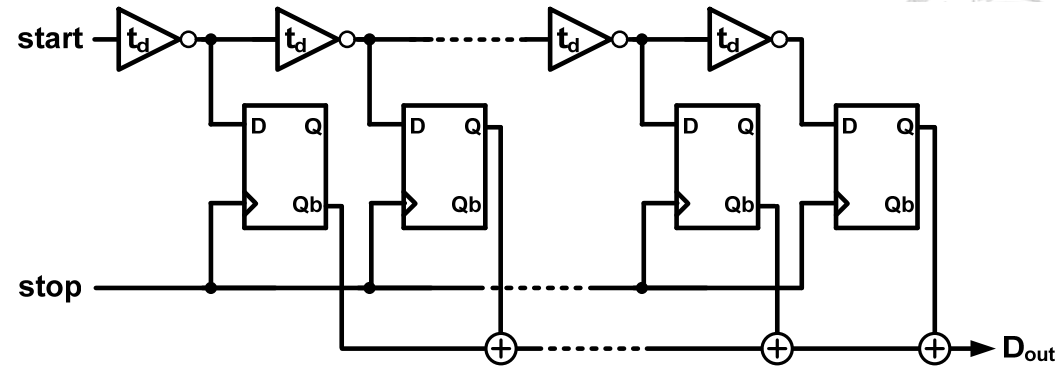
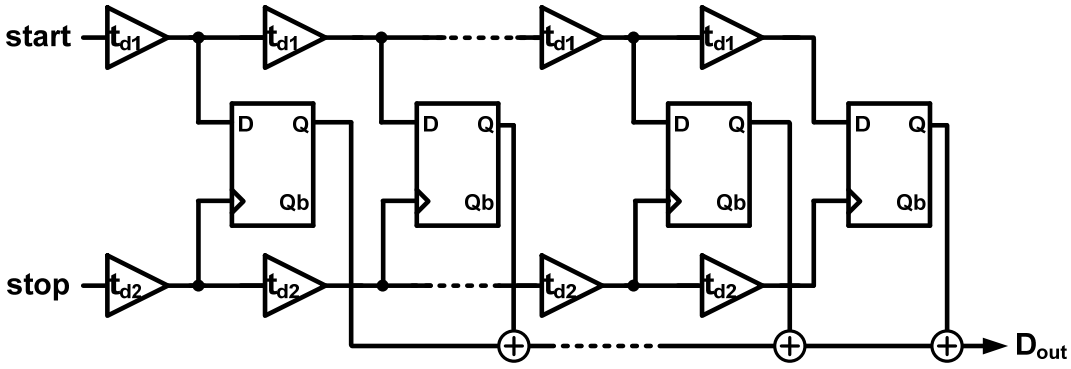


(a)



(b)

Fig. 2.4. (a) Conventional delay-line-based TDC and (b) Vernier type delay-line-based TDC.

2.3 General TDC architecture

Fig 2.4 (a) shows a conventional delay-line-based digital TDC which is also called flash TDC. This architecture uses only standard cell of the CMOS process which is suitable for advance CMOS technology. Featuring low cost, low power and high integration level, this architecture gains particular interest. And the resolution of the TDC can be expressed as

$$T_{\mathrm{LSB}} = t_{\mathrm{d}}. \tag{2.3.1}$$

The main drawback of this TDC is that the timing resolution of the TDC is limited to its minimum gate delay which is about tens of picoseconds in 90-nm CMOS.

The improvement of the resolution can be achieved by employing a Vernier type

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delay-line to the conventional architecture as shown in Fig 2.4 (b) [1]. For the improved TDC, the *start* and *stop* are both fed to a series of delay cells and are fed into an arbiter in each stage. The delay t_{d2} is designed to be smaller than the delay t_{d1} so that the *stop* signal can catch up the start signal along the delay line stages. The output code of the TDC is the summation of the stage output. By adding another delay-line at the stop signal path, the resolution of the conventional delay-line-based TDC can be improved to

$$T_{LSB} = t_{d1} - t_{d2}. \tag{2.3.2}$$

Theoretically, the resolution of the improved TDC can be design to be any value. The difference of the delay t_{d1} and t_{d2} can be made to be as small as possible. In practice, the resolution of the TDC is limited by the process variation. Mismatch of the delay cells and physical noise of the transistors would limit its overall resolution. Besides, this architecture needs extra hardware for extending input range. For the Vernier delay line, the maximum dynamic range is limited to

$$T_{DR} = N \cdot T_{LSB}, \tag{2.3.3}$$

where N is the number of delay cells in the delay line. Introducing a clock signal with the period equal to the dynamic range of the Vernier delay line T_{DR} and counts the rising edge of the clock, the dynamic range of the TDC can be sufficiently extended. Calibration circuit is needed to insure that the clock period is equal to the dynamic range of the Vernier delay line T_{DR} [1]. A Vernier ring TDC has been published to overcome the limitation of the input range [2] without the need of calibration.

Time amplification TDC achieves high resolution with low area [3]. This TDC employed a two steps conversion to resolve the time interval. The input time interval is first quantized by a coarse TDC to generate the coarse output code and the residual time from the coarse TDC is fed to a time amplifier. The fine TDC then resolves the amplified residual time and produces the fine output code. The key building block of the

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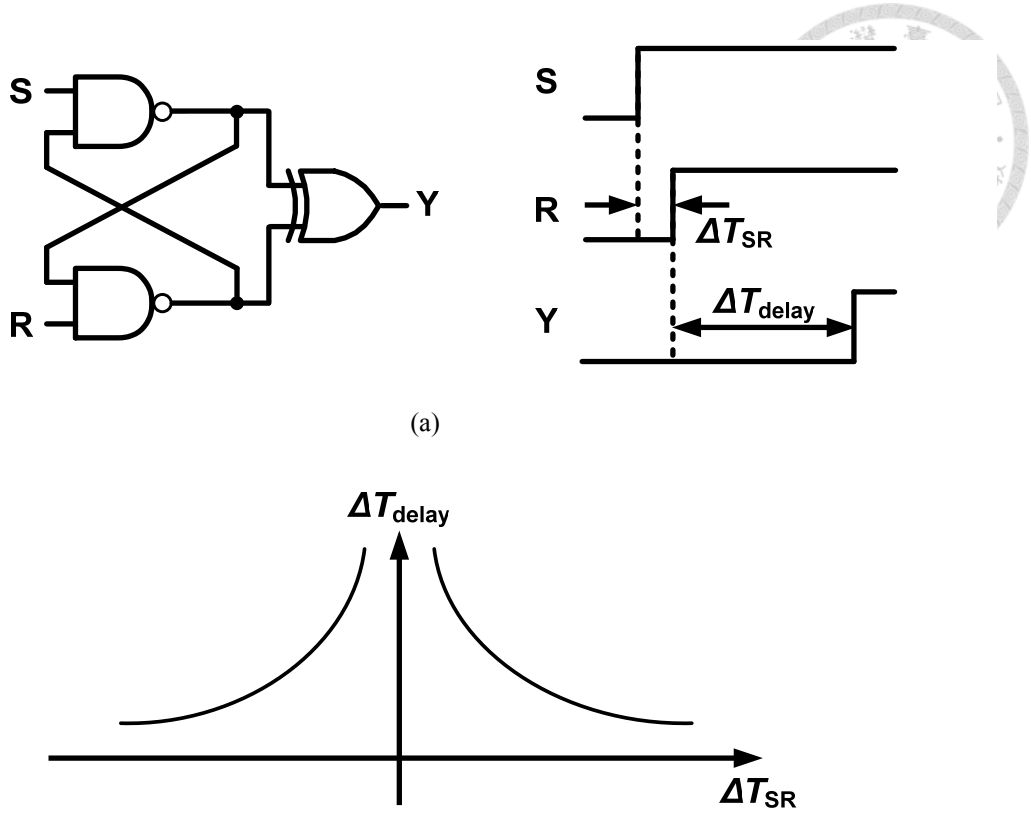

Fig. 2.5. (a) SR latch followed by an XOR with its timing diagram and (b) the relationship between the delay time of SR latch and the input time difference.

TDC is the time amplifier (TA) utilizes the metastability of a SR latch to amplify a time interval. The SR latch exhibits variable delay when nearly coincident input edges are fed to the SR latch as shown in Fig 2.5 (a). Fig 2.5 (b) shows the relationship between the delay time of SR latch and the input time difference. The relationship can be described as [3]

$$\Delta T_{\text{delay}} = \tau \cdot \left(\log V_{\text{TH}} - \log \left| \alpha \cdot \Delta T_{\text{SR}} \right| \right), \tag{2.3.4}$$

where τ and α are constant defined by the physical quantities, and V_{TH} is the threshold voltage of the exclusive OR (XOR). Adding a delay T_{off} in one of the input path, the transfer curve shown in Fig 2.5 (b) can be shifted for the y-axis. Combining two SR latch with additional delay T_{off}, the time amplifier can be realized as shown in Fig 2.6. The time amplifier output time T_{out} is the delay time of the top SR latch minus the delay

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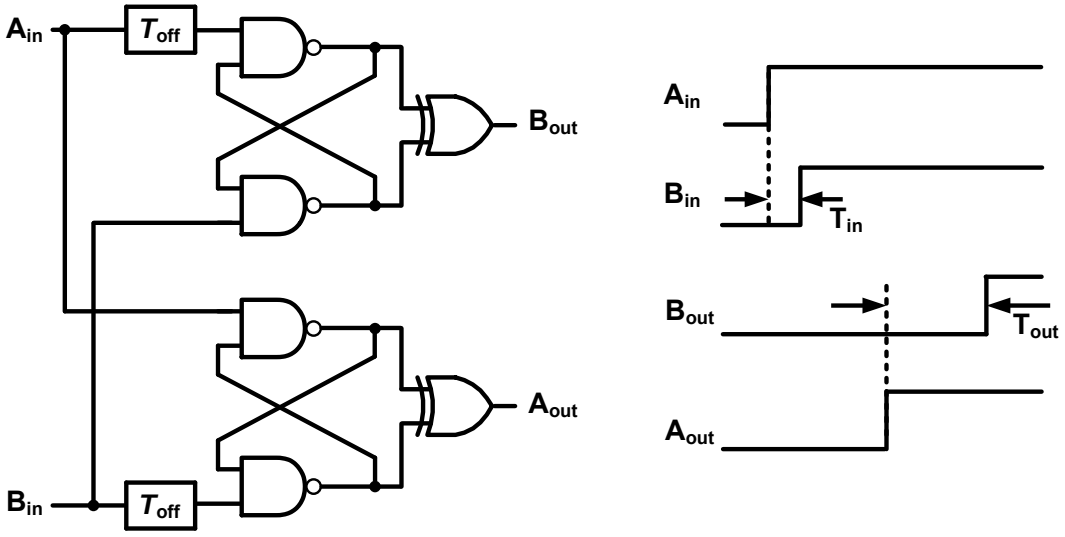
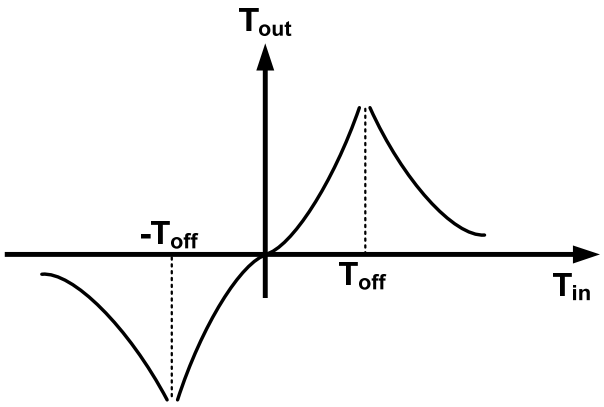


(a)



(b)

Fig. 2.6. (a)Concept of a TA (b) and input/output transfer curve of a TA

time of the bottom SR latch and can be described as follows

$$T_{\text{out}} = \Delta T_{\text{delay,top}} - \Delta T_{\text{delay,bot}}. \tag{2.3.5}$$

Substituting (2.3.4) into (2.3.5), the output time can be rearranged as

$$T_{\text{out}} = \tau \cdot \left[\log\left(T_{\text{off}} + T_{\text{in}}\right) - \log\left(T_{\text{off}} - T_{\text{in}}\right) \right]. \tag{2.3.6}$$

where T_{in} is the time difference between the two input edges and is ranging from -T_{off} to T_{off}. By adding the time amplifier to realize the two-step TDC, the resolution of the time domain quantizer can be greatly relaxed.

Time-to-digital converter based on cyclic time domain successive approximation

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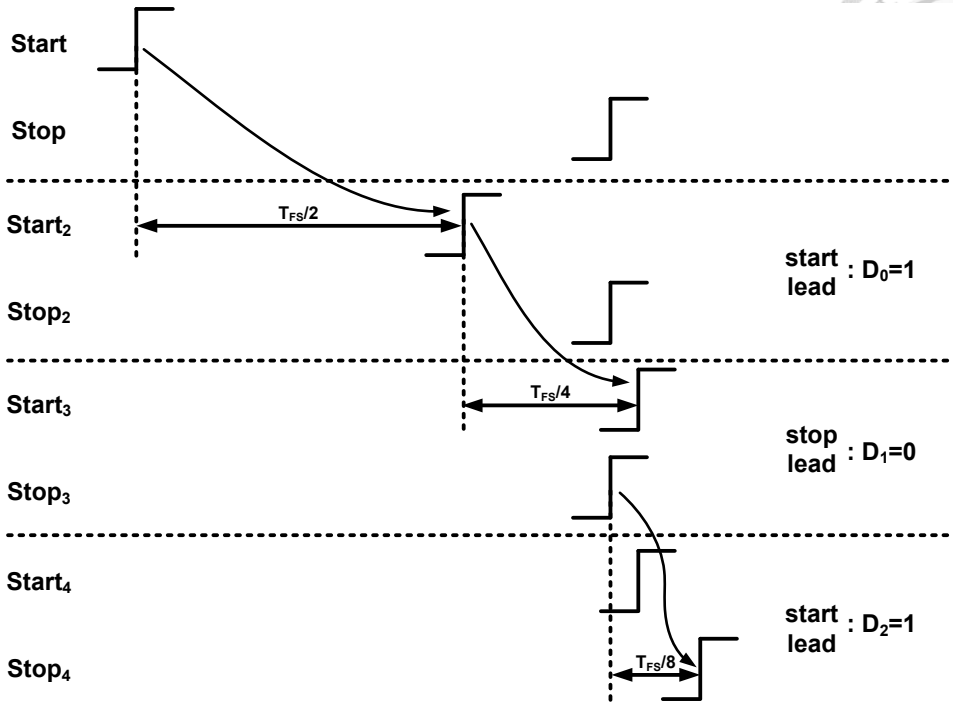

Fig. 2.7. Conceptual timing diagram of a 3-bit CTDSA.

(CTDSA) achieves high resolution with wide dynamic range [4]. The conceptual timing diagram of a 3-bit CTDSA is shown in Fig 2.7. The CTDSA measures the time difference between two signal, *start* and *stop* in Fig 2.7. At the beginning of the measurement, the signal *start* is delayed by a time $T_{FS}/2$. The delayed signal is shown as $start_2$ in Fig 2.7 and the MSB of the TDC is determined to be one since the signal $start_2$ leads the signal $stop_2$. The signal $start_2$ would then be delayed by a time $T_{FS}/4$ and the second bit is generated to be zero because the signal $stop_3$ leads signal $start_3$. Finally, the $stop_3$ is delayed by a time $T_{FS}/8$ and the LSB is one. Compare to the delay-line based TDC, the successive approximation (SAR) method can effectively reduce the required hardware for wide sensing range due to the use of single delay element with adjustable delay time. The delay cell with adjustable delay time is fulfilled by using cascaded inverter with digital controlled capacitive loading.

Although the TDC with time amplification or successive approximation can achieves high resolution, complicated calibration is needed to calibrate the time amplifier's gain

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or the delay time of the delay element.

Apart from the TDC mentioned above, several architectures have been published to achieve fine-resolution. A pipeline TDC [5] achieves 300-MHz conversion rate with 1.76-ps resolution and a cyclic TDC [6] achieves 10-MHz conversion with 0.63-ps resolution while consuming 0.82 mW. For those TDCs, sophisticated calibration usually needed to calibrate its non-linearity. A stochastic TDC [7] realized in 14nm FinFET technology has been proposed to achieve 1.17-ps resolution with 100-MHz conversion rate without calibration.

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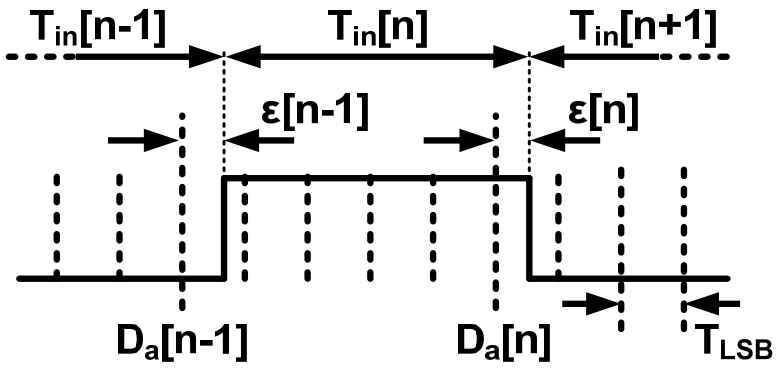

Fig. 2.8. Continuous time measurement of the interval.

2.4 Delta-sigma TDC

Before this section, the mentioned TDC operations are analogous to the conventional flash, two step, pipeline, SAR ADC. In this section, the TDC analogous to ΔΣ ADC that achieves the noise-shaping property is presented. The effective resolution can be greatly improved as the quantization noise is first-order shaped. Fig 2.8 shows a measured time interval $T_{in}[n]$ represented by a pulse width and a delay-line-based TDC continuously measures the time. The dot-line shows the continuous quantization of the time interval and the time T_{in} can be described as follow

$$\left(D_a[n]-D_a[n\text{-}1]\right)\cdot T_{LSB}=T_{in}[n]-\left(\varepsilon[n]-\varepsilon[n\text{-}1]\right). \qquad (2.4.1)$$

where the $D_a[n]$ and $D_a[n\text{-}1]$ are the accumulated digital outputs, T_{LSB} the timing

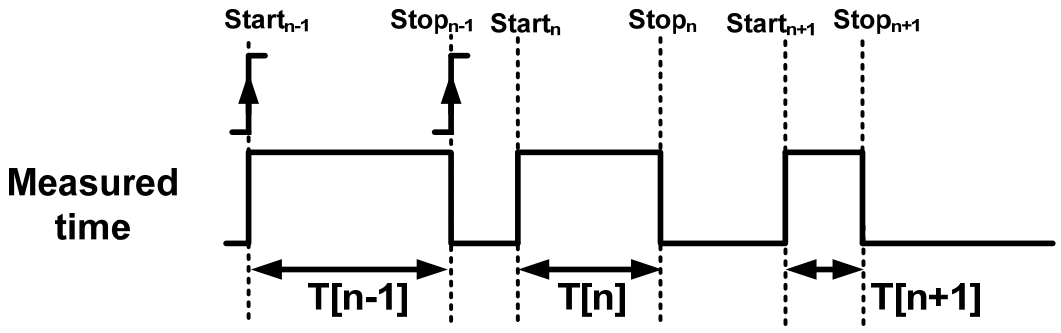

Fig. 2.9. Discrete time measurement of the time interval.

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resolution of the TDC, ε[n] and ε[n-1] are the quantization errors. Equation (2.4.1) shows that the total quantization error within the time $T_{in}[n]$ is the difference of two quantization errors from the consecutive delay line sampling. Taking z-transform of (2.4.1) yields

$$(1\text{-}z^{-1})\cdot D_a(z)\cdot T_{LSB} = D_{out}(z)\cdot T_{LSB} = T_{in}(z) - \varepsilon(z)\cdot(1\text{-}z^{-1}), \tag{2.4.2}$$

which shows the quantization noise is first-order shaped. The theoretical *rms* value of the quantization noise power can be written as

$$\varepsilon_{rms} = \frac{T_{LSB}}{\sqrt{12}}\cdot\frac{\pi^L}{\sqrt{2L+1}}\cdot OSR^{-(L+1/2)}, \tag{2.4.3}$$

where the *OSR* is the oversampling ratio, and *L* is the order of the noise-shaping function.

In practice, the measurement of the input time interval is non-continuous as shown in Fig 2.9. The measurement of a time interval is often initiated by the rising edge of signal

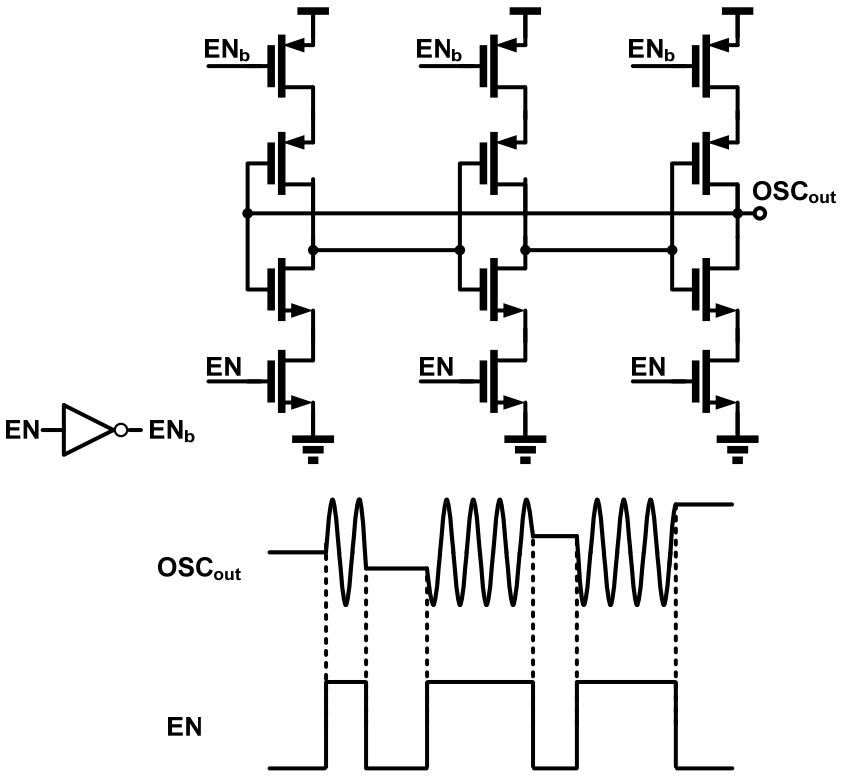

Fig. 2.10. Schematic of GRO and its transient operation.

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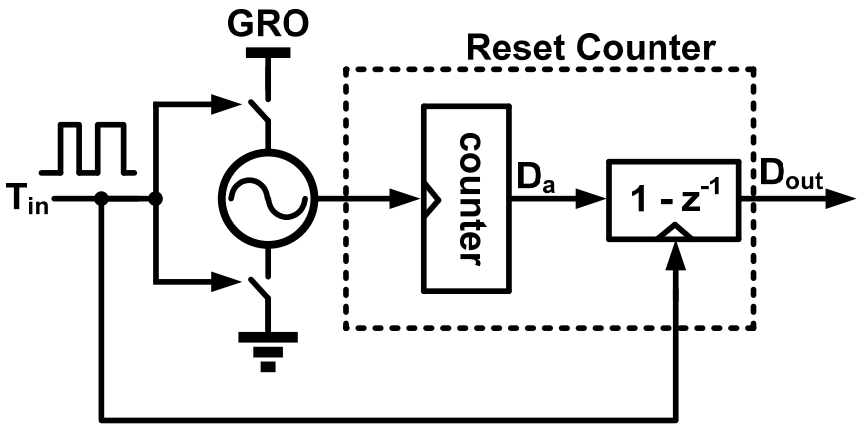

Fig. 2.11. Architecture of the GRO-TDC.

start and ends at the falling edge of the signal *stop* and the next measurement will not start until the next rising edge of signal *start.*

Due to the fact that the measurement is discrete, a TDC with gated-ring oscillator (GRO) [8] is proposed to achieve the noise-shaping property. The simplified schematic of the GRO is shown in Fig 2.10 , consists of three cascaded inverters and three pairs of switches controlled by the signal EN & EN_b. The GRO only oscillates when the signal EN is high and hold its phase when EN is low. Feeding the input time to the GRO as shown in Fig 2.11, the conceptual operation principle of GRO-TDC is shown in Fig 2.12. Controlling the by the measured time, the GRO only oscillates during the measured time interval. The digital output is produced by counting the rising edge of the GRO during the measured time interval. The discrete measurement of the GRO-TDC can be mapped into a continuous measurement of a delay-line-based TDC shown in Fig 2.8 which achieves first-order noise shaping of the quantization noise. The output of the GRO-TDC can be represented as follow

$$D_{\text{out}}[\text{n}]=\frac{T_{\text{in}}[\text{n}]}{T_{\text{LSB}}}-\frac{\left(\varepsilon[\text{n}]-\varepsilon[\text{n-1}]\right)}{T_{\text{LSB}}}. \tag{2.4.4}$$

Using GRO to realize the ΔΣ TDC, the GRO-TDC achieves sub-gate delay resolution while occupying low area without calibration. Compare to other TDCs, the GRO-TDC

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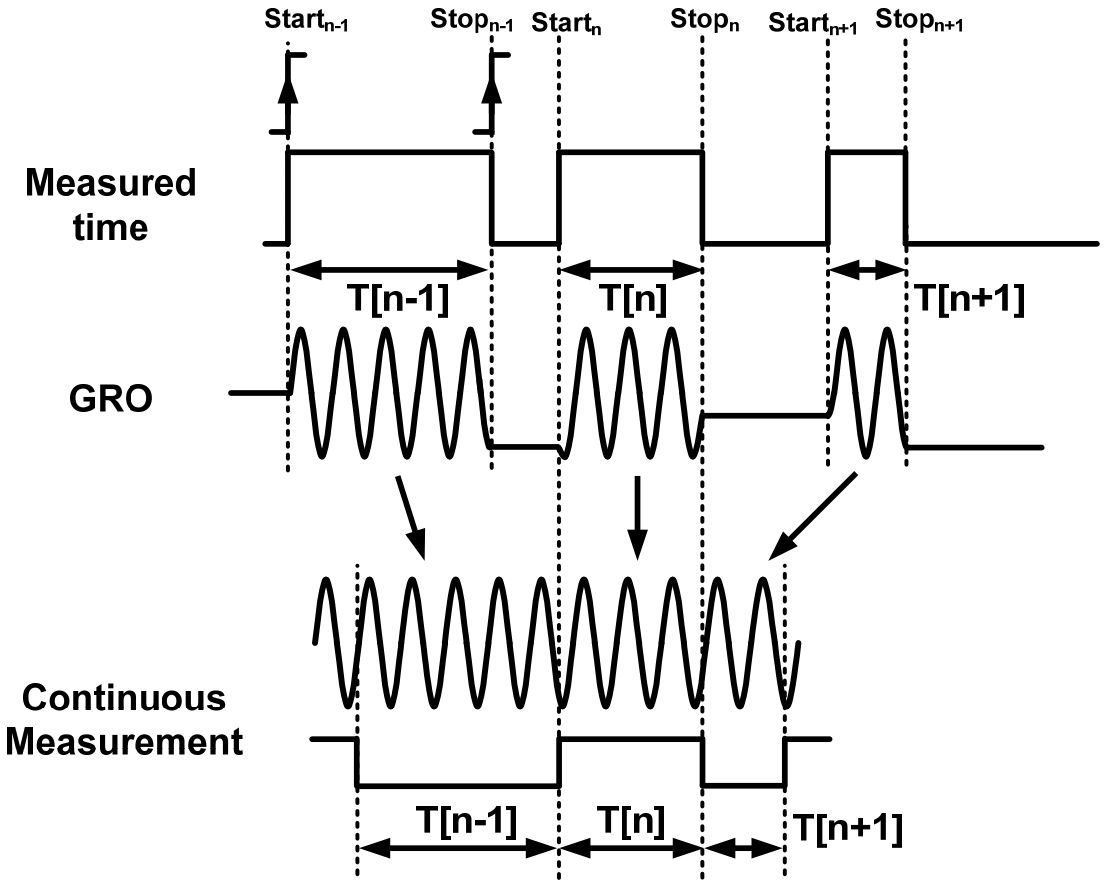

Fig. 2.12. Illustration of noise shaping in the discrete time measurement.

consumes large power due to the use of a multi-path GRO. Ideally, the phase is preserved completely when the GRO is turn off. However, the charge injection from the switches and the leakage of the transistors cause harmful error to the oscillator phase as shown in Fig 2.13. Multi-path structure reduces the leakage problem at the cost of high power consumption.

Many other ΔΣ TDCs have been published to mitigate the leakage problem. Fig 2.14 shows a conceptual timing diagram of a switched-ring oscillator TDC [9]. The SRO-TDC uses the input time window as the control signal of the ring oscillator. The SRO oscillates at its maximum frequency f_{max} when the input is high and oscillates at the minimum frequency f_{min} when the input is low. The phase change of the SRO within

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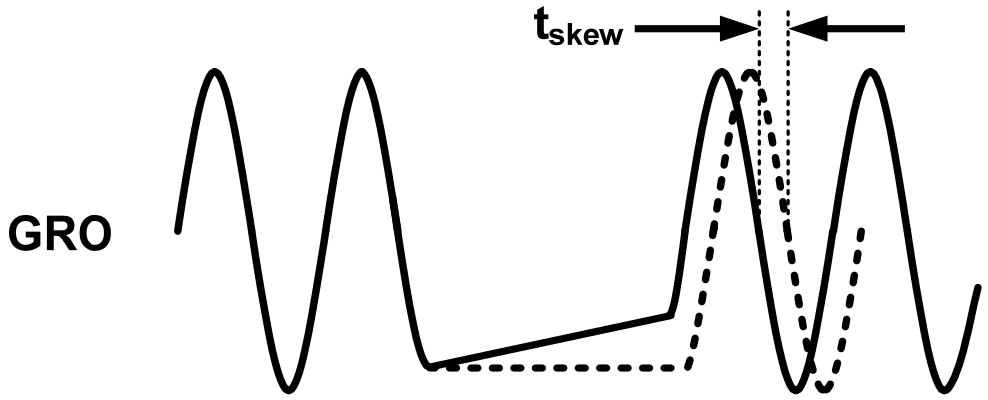

Fig. 2.13. Leakage induced timing skew error in GRO.

a sampling period can be described as

$$\phi_{\mathrm{SRO}}[\mathrm{n}] = 2\pi \cdot D_{\mathrm{out}}[\mathrm{n}] + \phi_Q[\mathrm{n}] - \phi_Q[\mathrm{n+1}], \tag{2.4.5}$$

where the D_{out} is the digital output of the TDC and ϕ_Q the quantization error. The digital output is the number of oscillator rising edges happened within a clock cycle. And the input T_{in} is represented as

$$2\pi \cdot T_{\mathrm{in}}[\mathrm{n}] \cdot (f_{\max} - f_{\min}) = \phi_{\mathrm{SRO}}[\mathrm{n}] - T_{\mathrm{C}} \cdot f_{\min}. \tag{2.4.6}$$

Substituting (2.4.6) into (2.4.5), the TDC output can be obtained as

$$D_{\mathrm{out}}[\mathrm{n}] = T_{\mathrm{in}}[\mathrm{n}] \cdot (f_{\max} - f_{\min}) + T_{\mathrm{C}} \cdot f_{\min} - \frac{\phi_Q[\mathrm{n}] - \phi_Q[\mathrm{n+1}]}{2\pi}, \tag{2.4.7}$$

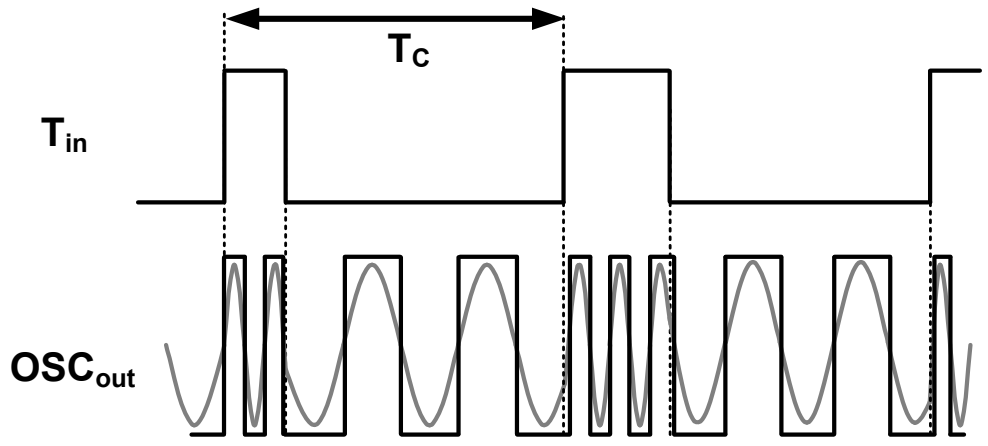

Fig. 2.14. Operation of the SRO-TDC.

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which shows the first-order shaped of the quantization noise. Since the ring oscillator is not fully gated, the leakage problem can be reduced. Although the leakage problem can be reduced, the raw resolution T_{LSB} of the SRO-TDC becomes $1/(f_{max}-f_{min})$. Compare to the GRO-TDC which has a raw resolution of $1/f_{max}$, the SRO-TDC has a reduction in its raw resolution. Thus, the SRO-TDC needs high *OSR* to achieve high resolution. Besides, the SRO is always oscillating even if there is no input feeding into the TDC, the power of the TDC therefore increases.

A 1-1-1 MASH ΔΣ TDC is presented to further improve the ΔΣ TDC performance [10]. Similar to a 1-1-1 MASH ΔΣ ADC, a third-order ΔΣ TDC is formed by cascading three first-order ΔΣ TDC. The 1-1-1 MASH ΔΣ TDC works as follow: the measured input time is fed to the first ΔΣ TDC and the first ΔΣ TDC produces the digital output

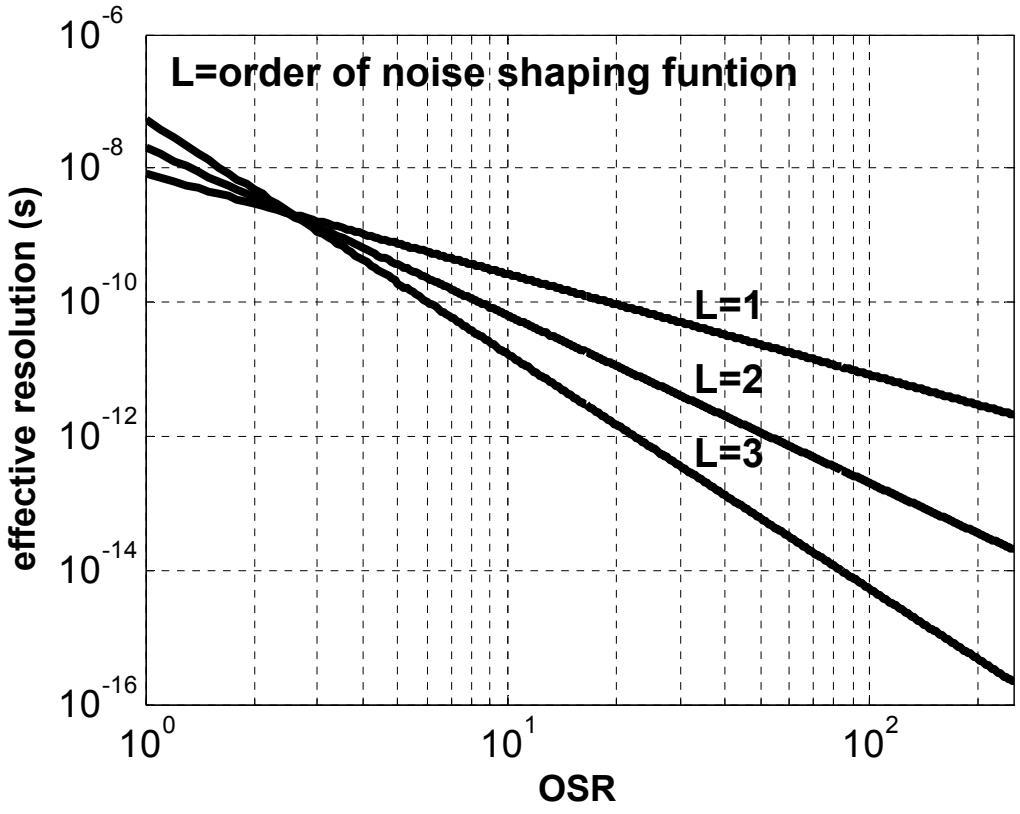

Fig. 2.15. Simulation results of the ΔΣ TDC effective resolution.

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D_{out1}. Then, the time domain quantization error of the first TDC is fed to the second TDC and the quantization error of the second TDC is fed to the third TDC. With the help of digital signal processing the combination of the three TDC output achieves third-order noise-shaping. Considering the z-transform of a ΔΣ TDC digital output, each output of the three stages is:

$$D_{out1}(z)\cdot T_{LSB} = T_{in}(z)+\varepsilon_1(z)\cdot(z^{-1}-1) \tag{2.4.8}$$

$$D_{out2}(z)\cdot T_{LSB} = \varepsilon_1(z)+\varepsilon_2(z)\cdot(z^{-1}-1) \tag{2.4.9}$$

$$D_{out3}(z)\cdot T_{LSB} = \varepsilon_2(z)+\varepsilon_3(z)\cdot(z^{-1}-1), \tag{2.4.10}$$

where T_{LSB} is the oscillation period of the oscillator used in the ΔΣ TDC. By combining the three stage outputs in the digital domain, the overall digital output of the 1-1-1 MASH ΔΣ TDC is

$$D_{out}(z) = D_{out1}(z) + D_{out2}(z)\cdot(1-z^{-1}) + D_{out3}(z)\cdot(1-z^{-1})^2 \tag{2.4.11}$$

$$= \frac{T_{in}(z)}{T_{LSB}} + \frac{\varepsilon_3(z)\cdot(1-z^{-1})^3}{T_{LSB}}, \tag{2.4.12}$$

where ε_3 is the quantization error in the third stage. According to (2.4.3), the *rms* value of quantization noise power of a third-order ΔΣ TDC is 100 times lower than the first-order ΔΣ TDC if the OSR is chosen to be 20. Due to the large improvement of the quantization noise power in the proposed TDC, the requirement of the oscillation period T_{LSB} for a high resolution TDC can be released. To mitigate the leakage problem of the ring oscillator, the ring oscillator in the 1-1-1 MASH ΔΣ TDC uses large capacitance. Simulation has been done for an example TDC with T_{LSB} equals to 16 ns. Fig 2.15 shows the simulated effective resolution of the ΔΣ TDC with different order of noise shaping function. If an OSR of 250 is employed, the third-order TDC can achieve a 0.2-fs resolution which is much lower the physical noise floor of the TDC. It should be

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noted here that the oscillator period T_{LSB} of each stage should be the same to completely cancel the quantization error of the first stage and the second stage.

A 1-3 MASH forth-order ΔΣ TDC [11] achieves picosecond resolution with an OSR of 5. The forth-order ΔΣ TDC is capable of achieving high resolution with high signal bandwidth. This TDC is implemented using two stage architectures. The first stage is the conventional first-order ΔΣ GRO-TDC. Consisting of a GRO-TDC and an error-feedback filter, the second stage is implemented as a third-order ΔΣ TDC. The high order ΔΣ TDC enhances the signal bandwidth of the TDC but the resolution of the TDC still suffered from the GRO leakage current and the switching noise from the switches.

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Chapter 3

A Noise-Shaping Time-to-Digital Converter with Gated-Free Ring Oscillator

3.1 Introduction

An energy efficient delta-sigma time-to-digital converter (TDC) is presented in this chapter. The proposed delta-sigma TDC achieves high resolution by leveraging oversampling and noise-shaping. Compared with conventional circuit techniques, non-ideal effects associated with switching noise and transistor leakage can be generally prevented due to the use of a gated-free ring oscillator and leakage-suppression switches in the circuit implementation.

The remainder of this chapter is organized as follows. Section 2 describes the architecture of the proposed ΔΣ TDC while the circuit design and experimental results are presented in Section 3 and 4, respectively. Finally, a conclusion is provided in Section 5.

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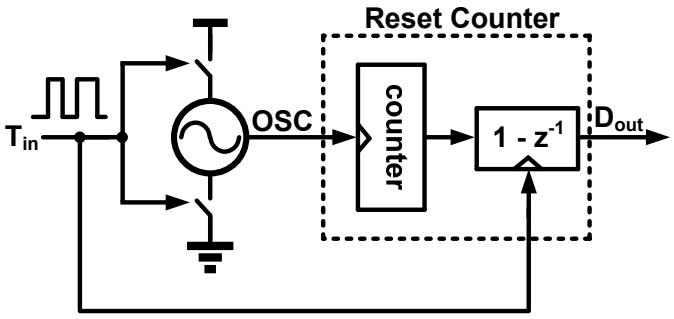

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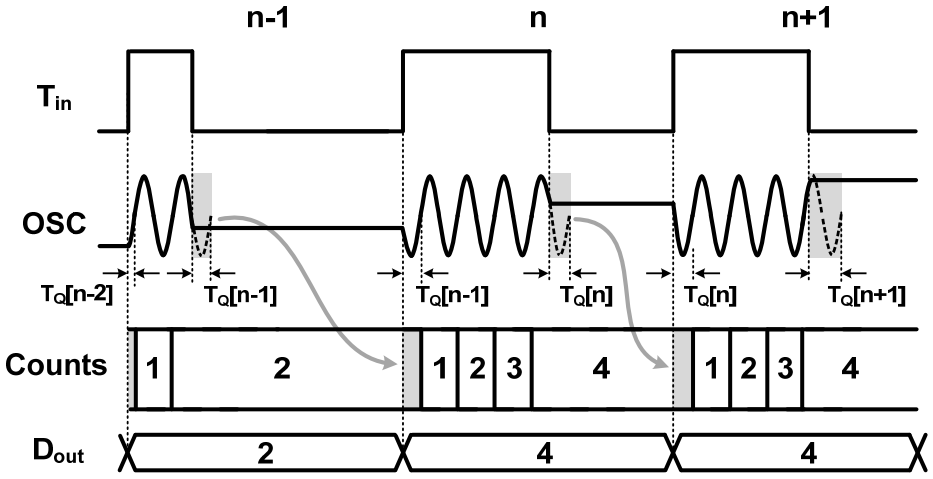

(b)

Fig. 3.1. (a)The simplified block diagram and (b) the timing diagram of the GRO-TDC.

3.2 Proposed delta-sigma TDC

3.2.1 Conventional gated ring oscillator TDC

A simplified block diagram of a conventional ΔΣ TDC using gated ring oscillator [8] and its timing diagram are shown in Fig. 3.1. The measurement of the input time interval is conducted by enabling the ring oscillator and counting the rising edges during this period of time. The ring oscillator oscillates when the input at T_{in} is high. On the other hand, when T_{in} goes low, the oscillator preserves the oscillation state by holding

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the charge at the output node. As illustrated in Fig. 3.1(b), the solid line of OSC indicates the oscillator output waveforms while the dotted line shows the expected waveforms if the ring oscillator is not gated. By preserving the oscillation state, the quantization error is transferred to the next cycle. Consequently, the input can be expressed as

$$T_{in}[n]=D_{out}[n]\cdot T_{GRO}+T_Q[n-1]-T_Q[n] \tag{3.2.1}$$

where the T_{GRO} is the oscillation period of the gated ring oscillator and T_Q is the quantization error of the TDC. According to (3.2.1), it is apparent that the quantization noise of the gated ring oscillator TDC is first-order noise shaped. However, special care has to be taken in the ring oscillator design to mitigate its non-ideal effects such as switching noise from gating transistors and leakage of the inverter stages. In order to avoid the error caused by switching noise and leakage, the transistor size and the output capacitance of the inverter stages should be relatively large. As a result, the oscillation frequency of the gated ring oscillator is severely limited, making it less attractive for high-resolution TDC designs.

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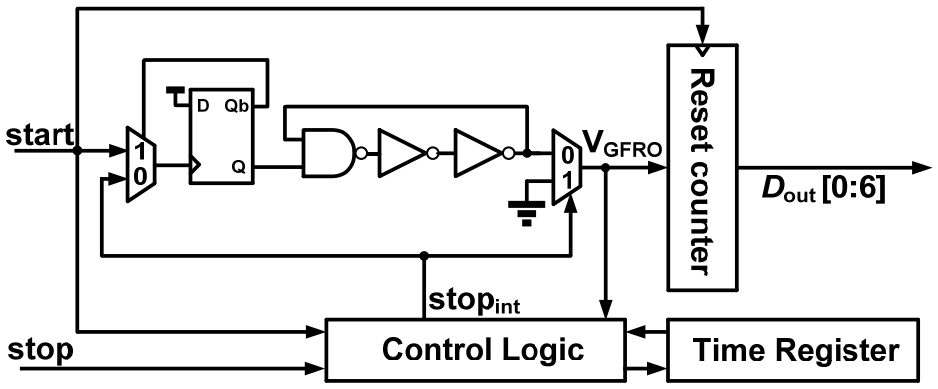

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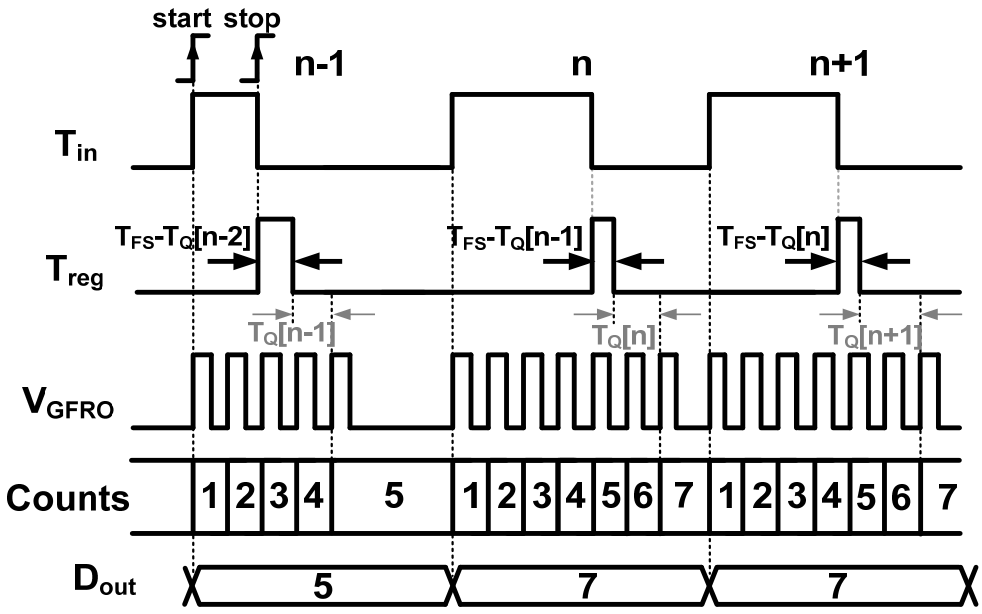

(b)

Fig. 3.2. (a) The architecture of the proposed ΔΣ TDC and (b) its conceptual timing diagram.

3.2.2 Proposed delta-sigma TDC

Figure 3.2 shows the proposed ΔΣ TDC and its conceptual timing diagram. Unlike conventional gated ring oscillator TDC, the proposed circuit does not preserve the state of the ring oscillator and no gating transistors are required. Instead, a NAND gate is added in the ring to control its oscillation as shown in Fig. 3.2(a). As illustrated in Fig. 3.2(b), the ring of the proposed TDC starts oscillating at the rising edge of the start signal. At the rising edge of stop, the time register generates a time interval T_{reg}, which

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is given by T_{FS} minus the time-domain quantization error from the previous cycle, that is T_{FS}-T_Q[n-1]. T_{FS} represents the full scale discharge time of the capacitor. After the falling edge of T_{reg}, the control signal $stop_{int}$ is triggered and fed to the multiplexers to stop the oscillation. It is noted that the time interval from the falling edge of T_{reg} to the second rising edge of V_{GFRO} is the quantization error T_Q[n]. Therefore, this error is memorized in the time register for the next cycle and the digital output is obtained by counting the rising edge at the output of the ring oscillator. In order to have a gated-free operation, the proposed TDC allows the oscillator to start at the same state rather than preserve the state of the ring oscillator. By shifting the time-domain quantization error as illustrated in Fig. 3.2(b), the input time interval of the TDC is given by

$$T_{in}[n] = (D_{out}[n]-1)\cdot T_{GFRO} - T_{FS} + T_Q[n-1] - T_Q[n] \tag{3.2.2}$$

where T_{GFRO} is the period at the output of the gated-free ring oscillator. The T_{FS} is a constant time interval due to the time register. With z-transform of (3.1.2), the digital code at the output can be expressed as

$$D_{out}[z] = \frac{T_{in}(z) + T_{FS} + (1-z^{-1})T_Q(z)}{T_{GFRO}} + 1, \tag{3.2.3}$$

showing a first-order noise shaping property for the TDC. The reason for the plus one at the digital output is that the gated-free ring oscillator is always stopped at the first rising edge after the stop signal is rising.

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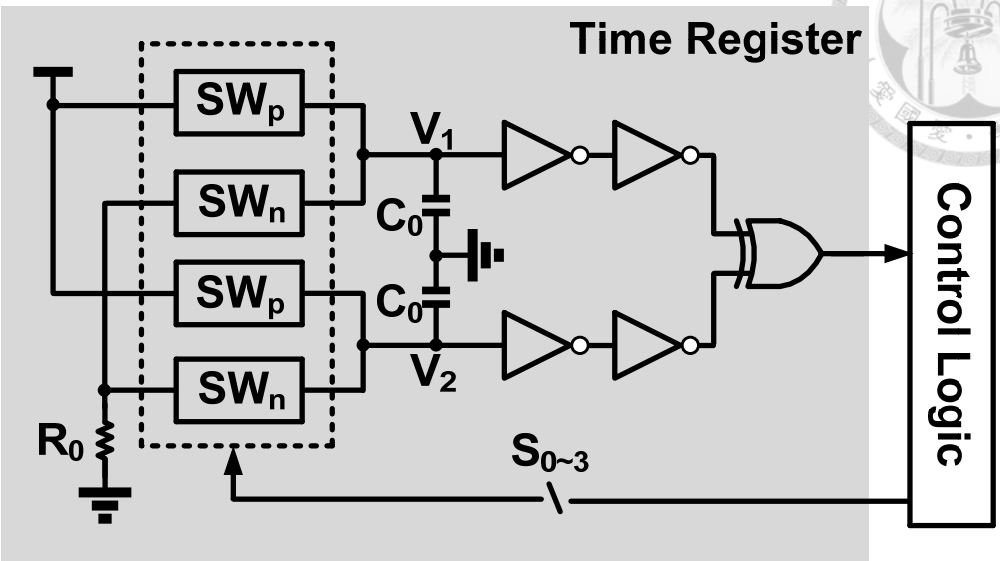

Fig. 3.3. Block diagram of the time register.

3.3 Circuit implementation

3.3.1 Time Register

To realize the operation of the proposed TDC, a time register is utilized in the design, consisting of switches SW_n and SW_p, two capacitors, a resistor and logic gates as shown in Figure 3.3. Unlike voltage-mode ADC circuits, the time-domain quantization error is difficult to be memorized and transferred. Therefore, a time-to-voltage operation is adopted to store the time-domain information [6] and the two capacitors operating alternatively in consecutive cycles are used for this purpose. Figure 3.4 shows the transient operation of the time register by illustrating the nodal voltage V_1 and V_2. At the end of the measured time interval, in other words, the rising edge of the signal *stop*, the first capacitor starts to discharge. The full scale discharge time of the capacitor is T_{FS} defined by the RC time constant of the circuits. For instance, the T_{FS} is simply $0.693 \cdot R_0C_0$ if the inverter threshold is $V_{DD}/2$. Since the first capacitor has been discharged for a time interval of $T_Q[n\text{-}1]$ during the previous cycle, the remaining

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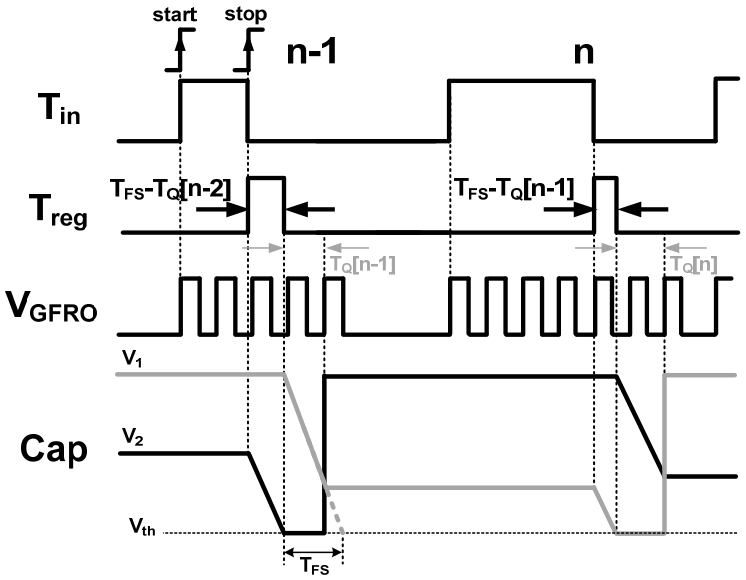

Fig. 3.4. Transient operation of the time register.

discharge time of first capacitor would be T_{FS}-$T_Q[n\text{-}1]$ in the n^{th} cycle, as depicted in Fig. 3.4. As the voltage of the first capacitor drops to the switching threshold of the inverter, the time register starts discharging the second capacitor until the second rising edge of the ring oscillator. Consequently, the time-domain quantization error of current cycle $T_Q[n]$ is memorized by the second capacitor while the first capacitor is reset to V_{DD}. The operations of the two capacitors exchange in the next cycle to generate the required T_{reg} for the TDC. It is noted that T_{FS} should be larger than $2 \cdot T_{GFRO}$ to ensure the time register work properly. The mismatch of the two capacitors is neglected here because the noise caused by the mismatch of the two capacitors would be filtered out by the decimation filter for filtering out high frequency quantization noise.

3.3.2 Leakage Suppression Switches

Although the leakage problem is alleviated for the ring oscillator due to the absence of the gating transistors, it may still lead to undesirable errors for the time register. Due to the low voltage operation in the proposed design, the size of switches should be large

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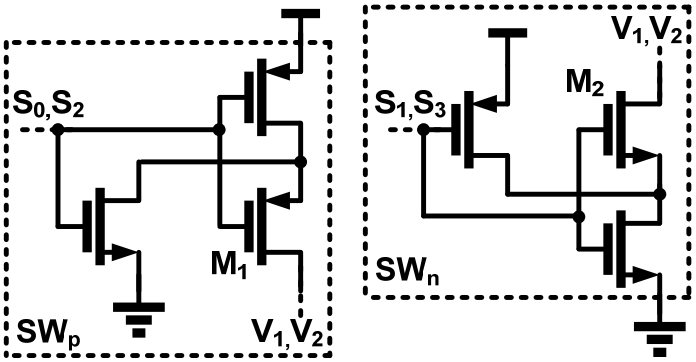

Fig. 3.5. Schematics of the leakage suppression switches

enough to minimize the time to charge the capacitor otherwise the conversion speed and the input range is limited. But the leakage problem becomes exaggerated as the large size switches is used. Therefore, a leakage-suppression technique [12] is adopted to realize the switches SW_p and SW_n. Figure 3.5 shows the circuit schematic of the switches controlled by S_0-S_3. When the leakage suppression switches are off, negative voltages V_{sg} and V_{gs} are provided for M_1 and M_2, respectively. The reversed source-gate voltage results in a significant reduction of the leakage current. Compared with the single transistor switches, the leakage suppression technique consumes more power and occupies more area. Since the ring oscillator often operates at a frequency much higher than the input rate, using the leakage-suppression switches in the gated ring oscillator is impractical due to excessive power overhead. The cascaded structure of the leakage suppressions limits the oscillator frequency. On the other hand, as these switches in the proposed TDC only toggles once in each clock cycle, it is well suited for the implementation of the time register

3.3.3 Gated-free ring oscillator

One of the key building blocks of the proposed TDC is the gated-free ring oscillator. The schematic of the gated-free ring oscillator is shown in Fig 3.6. To ensure the proposed TDC work properly, the frequency variation of the gated-free ring oscillator

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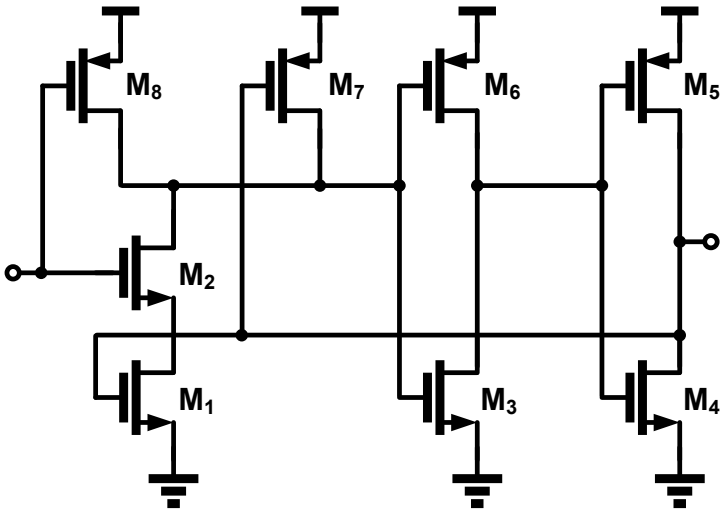

Fig. 3.6. Schematic of the gated-free ring oscillator

should be considered. In order to realize a high resolution TDC, it is better to minimize the period of the ring oscillator (T_{GFRO}). Due to the limited speed of the counter, the period of gated-free ring oscillator is designed to be 6 ns. The lengths of the transistors are designed to be slightly larger than the minimum size of the device to mitigate the process variation. From one hundred times Monte-Carlo (MC) simulations, the standard deviation of the oscillation period is 270 ps. Because of the large passive device size used in the time register, the standard deviation of full scale discharge time (T_{FS}) of the time register is only 8 ps which is tolerable in the proposed design.

3.3.4 Noise analysis

Considering the quantization noise power, the SNR of the proposed TDC can be calculated as [10]

$$SNR = 10\log\left(\frac{P_{\text{signal}}}{P_{\text{q.rms}}}\right) \tag{3.3.1}$$

$$=10\cdot\log\left[6(2L+1)\right]-10\cdot L+20\cdot(L+\frac{1}{2})\cdot\log(\text{OSR})+20\cdot\log(2^{N}\text{-}1), \tag{3.3.2}$$

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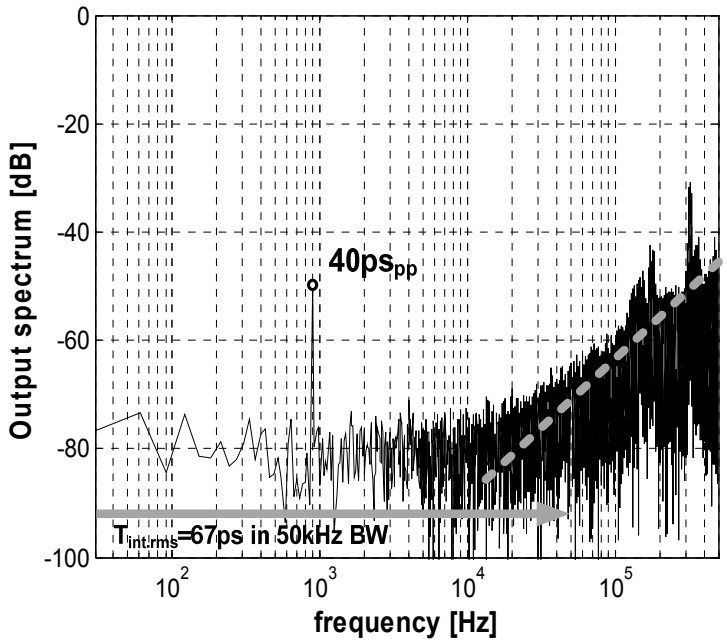

Fig. 3.7. Simulated output spectrum of the TDC.

where *L* is the order of the noise function, *OSR* oversampling ratio, and *N* the bits of the quantizer. In the proposed design, the *L* is set to be 1, the OSR is set to be 10, and a 7 bits quantizer is used. The theoretical SNR of the proposed TDC is calculated to be 74.6 dB, that is, an ENOB of 12.1 bits. However, the resolution of a practical TDC is limited by the jitter from the ring oscillator, the jitter from the time register, and the charge injection and charge redistribution from the switches. Those circuit non-idealities severely degrade the TDC performance especially in the low voltage design. Among those non-idealities, the jitter from the ring oscillator dominates the TDC performance. The charge redistribution and the charge injection can be neglected here because of the large capacitor used in the time register and the thermal noise from the switches and the resistor only depend on the size of the capacitor. Large device size is used to implement the inverters to suppress the flicker noise. In order to achieve a micro-power design, the transistors of the ring oscillator can't be excessively large and so as the parasitic capacitance. The size of the transistors used in the ring oscillator is just slightly larger

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than the minimum size to mitigate the process variation. Assuming that the jitter of the ring oscillator is caused by white noise, the *SNR* of the TDC can be derived as

$$SNR = 10\log\left(\frac{\frac{T_{\text{signal}}^{\ 2}}{2}}{\frac{\sigma_{\text{jitter}}^2}{OSR}}\right) \tag{3.3.3}$$

where T_{signal} is the full scale of the input time, and the σ_{jitter} is the *rms* jitter of the ring oscillator. The transistor level simulation shows that the *rms* jitter of the ring oscillator is about 29 ps. Thus, for an OSR of 10, the theoretical *SNR* of the TDC is 94.6 dB. Fig 3.7 shows the simulated output spectrum of the TDC with the presence of ring oscillator jitter. The integrated noise within 50-kHz bandwidth is 67 ps.

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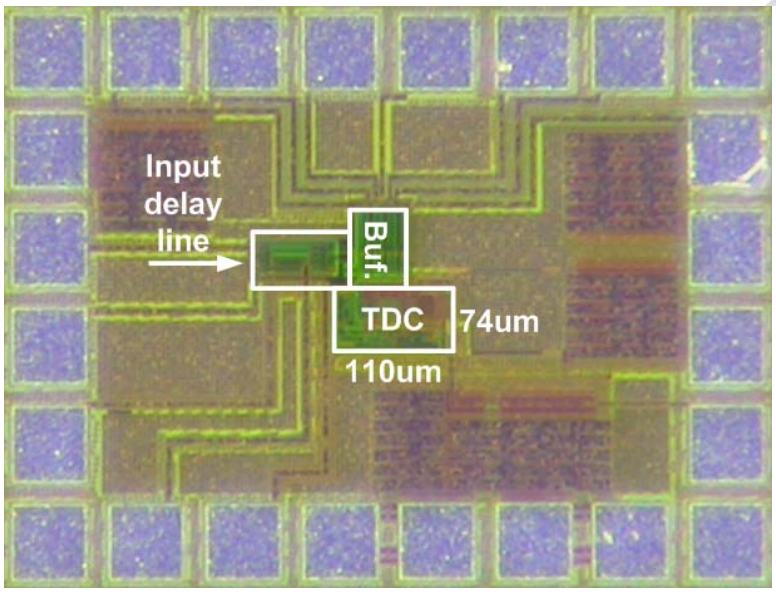

Fig. 3.8. Chip photo.

3.4 Experimental Results

3.4.1 Measurement at 0.3-V supply voltage

The TDC is fabricated by using a 90-mm CMOS process. Figure 3.8 shows the photomicrograph of the prototype circuit with a chip area of 0.0082 mm^2. Operated at a full scale input of 700 ns, the core circuit consumes a total power of 1.5 μW from a 0.3-V supply.

The static characteristics of the TDC were first investigated by applying a ramp input. For a 1-MHz input signal and a 0.999998-MHz clock, the transfer curve is obtained as shown in Fig. 3.9(a) after filtering the output with a 50-kHz digital low-pass filter. Figure 3.9(b) illustrates the integral nonlinearity (INL), which is extracted from the linear fit of the transfer curve, indicating a maximum INL value of +1.83/-1.84 LSB. With a 40-ps peak-to-peak sinusoidal input at 885 Hz, the power spectrum density (PSD) of the TDC output is characterize. The experimental results are shown in Fig. 3.10, where the first-order noise shaping is clearly observed. Note that, since it is difficult to generate a highly linear time-domain sinusoidal input, a small input signal generated by

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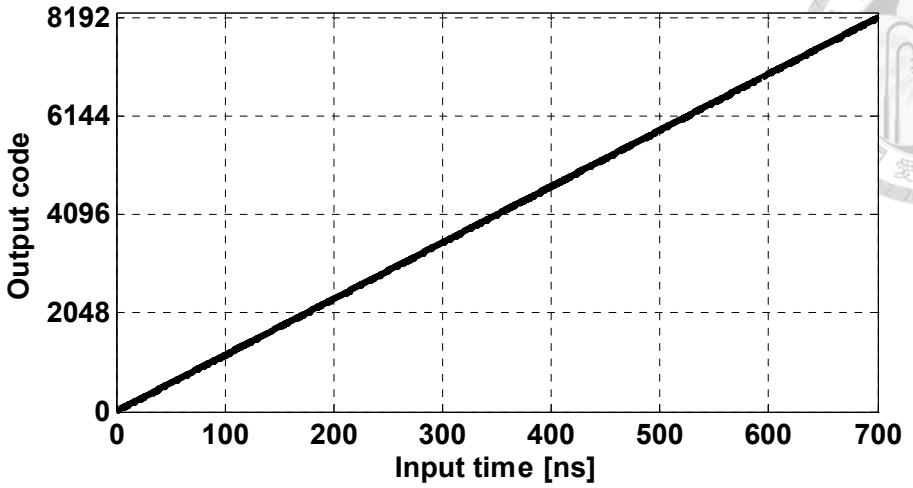
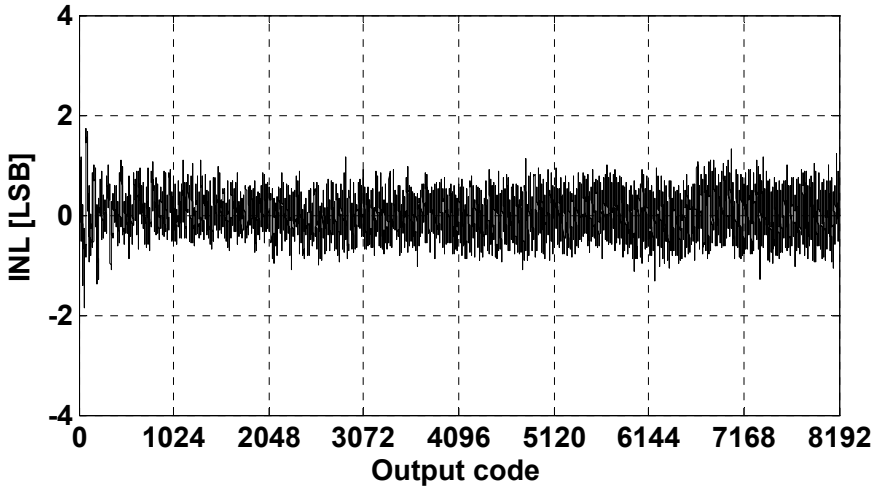


(a)



(b)

Fig. 3.9 Measured (a) DC transfer curve and (b) corresponding INL at 0.3-V supply.

an on-chip delay line is used to evaluate the TDC noise performance as shown in Fig. 3.11. Adding varactors on the delay path, the delay of the *stop* signal is controlled by applying sinusoidal wave to the varactors. Using this method, the input jitter can be minimized since the jitter from the instrument can be removed. The measured integrated noise of the proposed TDC is 113 ps within a bandwidth of 50 kHz. In contrast to the simulation results, the low frequency noise from the flicker noise in the ring oscillator and the supply noise dominates the overall resolution.

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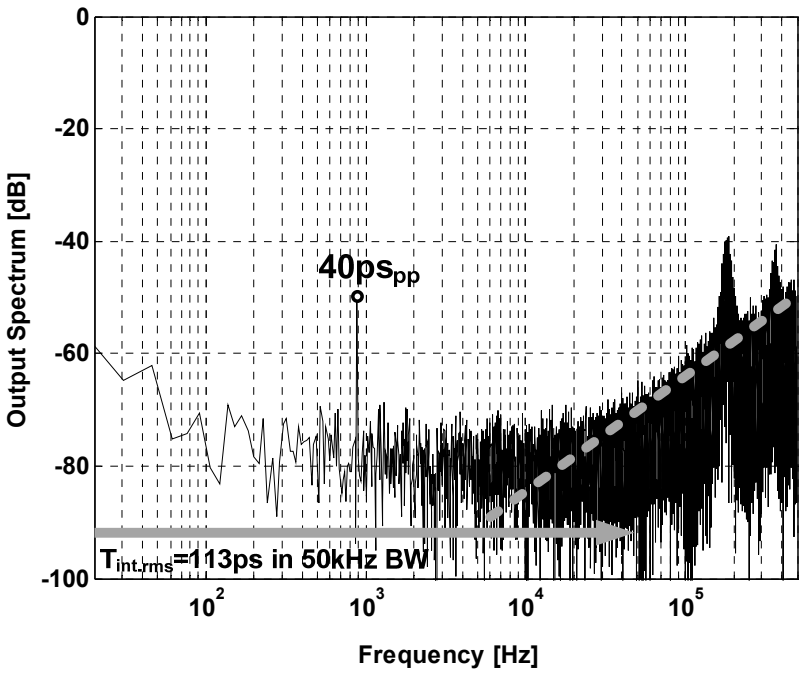

Fig. 3.10 Measured PSD for a 885-Hz input at 0.3-V supply.

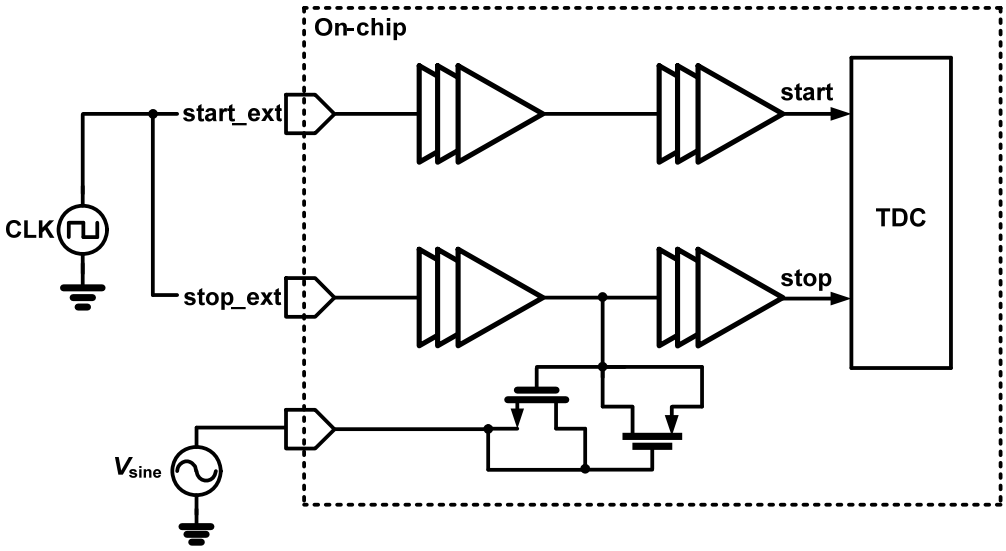

Fig. 3.11 Schematic of input-delay lines.

In addition, single-shot-precision (SSP) test was performed by applying a constant input to the TDC. In order to minimize the input clock jitter, the time difference of the two input clocks is generated by the delay of a connector cable. The experimental results of the SSP are shown in Fig. 3.12. With an input of 3.1 ns, the RMS noise of the filtered output code is 75.6 ps. It is noted that the discrepancy between the RMS noise

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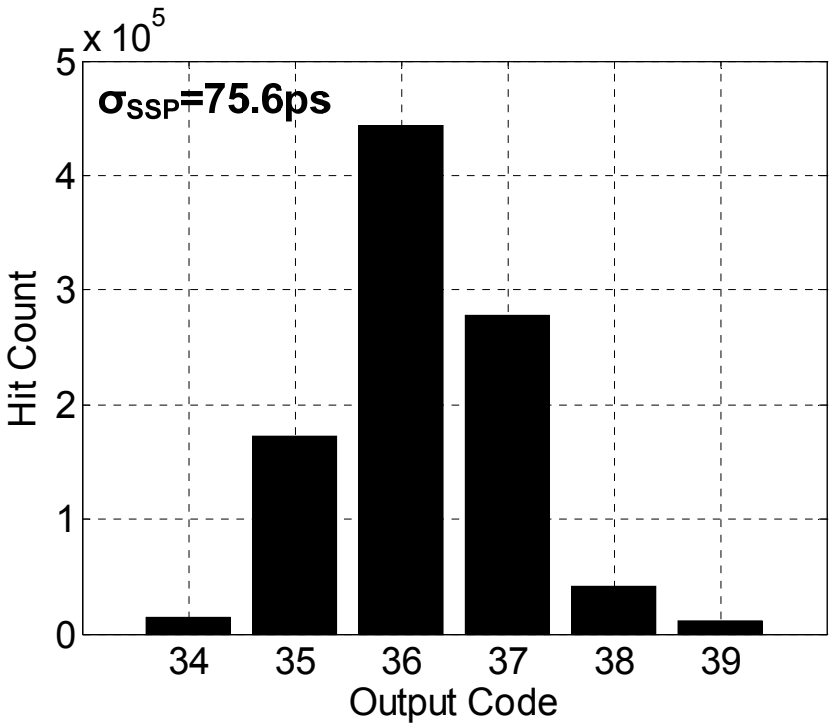

Fig. 3.12 Measured single-shot precision of the prototype TDC at 0.3-V supply.

from the SSP test and the integrated noise from the dynamics test is due to the different measurement setup.

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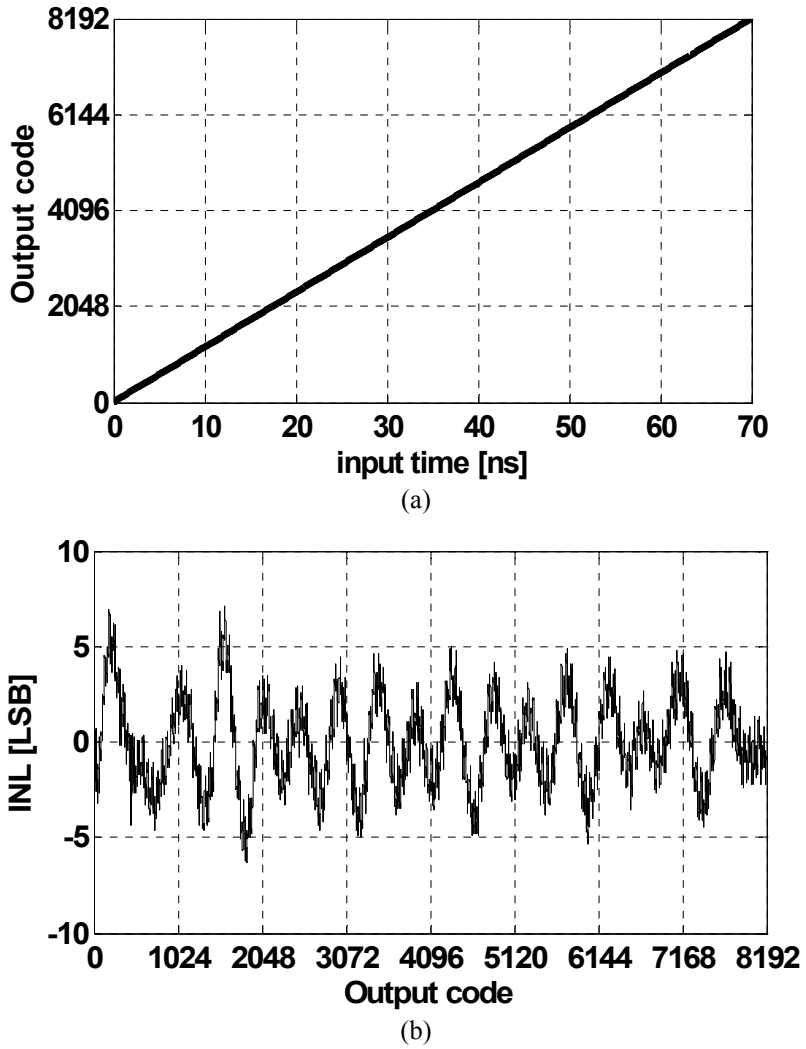

Fig. 3.13 Measured (a) DC transfer curve and (b) corresponding INL at 0.6V-supply.

3.4.2 Measurement at 0.6-V supply voltage

The power consumption of the TDC at 0.6-V supply voltage is 56 μW with a full-scale input range of 70 ns. By applying a 10-MHz and a 9.9999-MHz clock to the TDC, the measured DC transfer curve is obtained after filtering the output code with a 250-kHz digital filter as shown in Fig 3.13. The INL of the proposed TDC is obtained from the deviation of the transfer curve from the best fit line as shown in Fig 3.13 (b) and the worst case INL is +7.1/-6.3 LSB.

Fig 3.14 shows the output spectrum for a 10-ps peak-to-peak, 22.6-kHz time-domain

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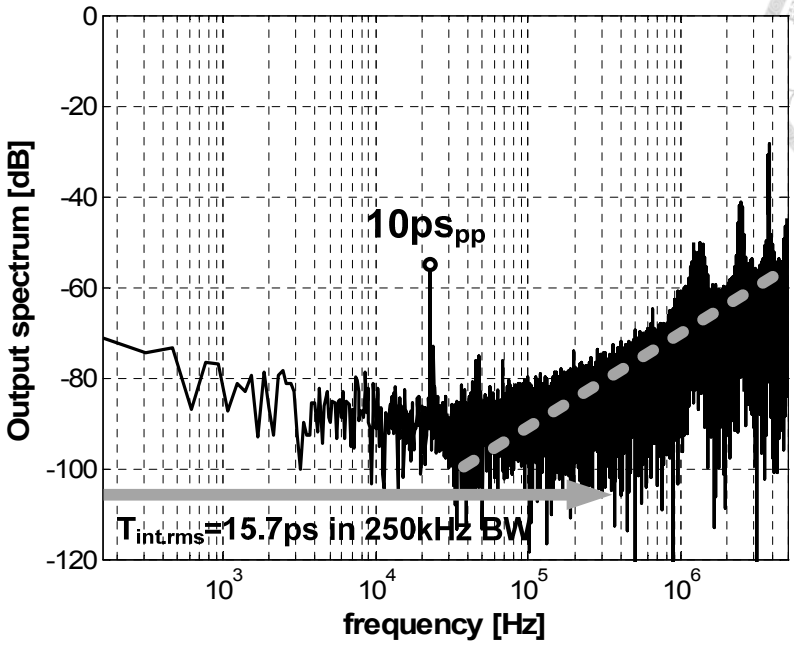

Fig. 3.14 Measured PSD for a 22.6-kHz input at 0.6-V supply..

sine-wave input. The integrated noise within 250 kHz is 15.7 ps. The results of SSP test is shown in Fig 3.15 with an approximately constant input of 197 ps and the RMS noise of the filtered output code is 3.2 ps.

The GFRO is the major source of the thermal/flicker noise within the TDC. The device noise of the GFRO shows as the phase noise of the GFRO and the phase noise exhibits $1/f^2$ and $1/f^3$ profiles in the thermal and flicker noise limited regions. Because of the reset counter, the output of the TDC has a flat spectrum in the thermal noise limited region. In the flicker noise limited region, the spectrum exhibits -10dB/decade slope.

To best characterize the TDC performance, the calculation of the ENOB considers both the linearity and the noise performance of the TDC [11]. The SNDR of the TDC is defined as

$$SNDR_{\mathrm{TDC}} = 10\log_{10}\left(\frac{P_{\mathrm{S}}}{P_{\mathrm{D}} + P_{\mathrm{N}}}\right), \tag{3.4.1}$$

where Ps, P_{D} and P_{N} are time-domain signal power, distortion power, and noise power of the TDC, respectively. The three parameters, Ps, P_{D} and P_{N}, are calculated according

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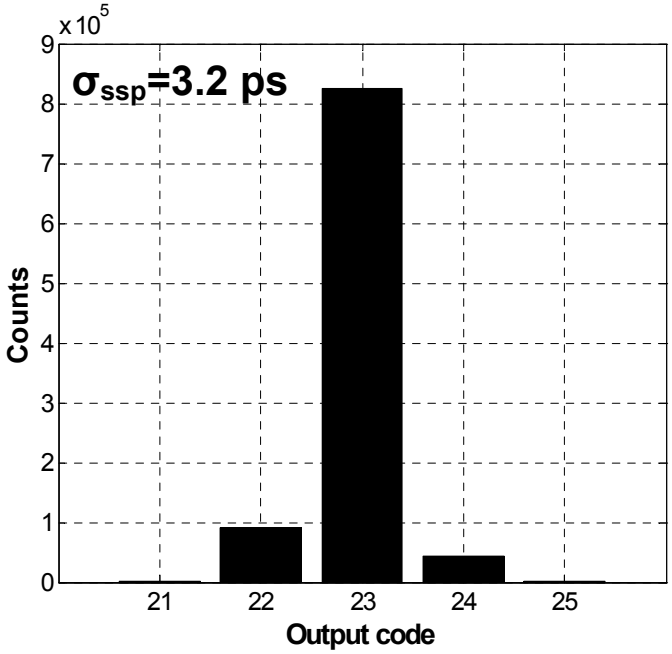

Fig. 3.15 Measured single-shot precision of the prototype TDC at 0.6-V supply.

to the static test and the SSP test as

$$P\text{S}=\frac{1}{2}\cdot(\frac{1}{2}\cdot T_{\text{range}})^2 \tag{3.4.2}$$

$$P_{\text{D}} = P_{\text{S}}\cdot 10^{-(6.02\cdot N_{\text{lin}}+1.76)/10} \tag{3.4.3}$$

$$P_{\text{N}} = \sigma_{\text{SSP}}^2 \ . \tag{3.4.4}$$

where N_{lin} is defined as $N_{\text{lin}} = \text{Bits} - \log_2(\text{INL+1})$. Then the ENOB of the TDC can be

Table 3-1 TDC PERFORMANCE AND COMPARISON WITH STATE-OF-THE-ART.

	Delta Sigma TDC					
	[8]	[9]	[10]	[11]	**This Work**	
Order	1st	1st	3rd	4th	**1st**	
Process(nm)	130	90	130	65	**90**	
Supply(V)	1.5	1	1.2	1	**0.3**	**0.6**
Area(mm^2)	0.04	0.02	0.11	0.03	**0.0082**	
f_{BW}(MHz)	1	1	0.1	15	**0.05**	**0.25**
f_s(MS/s)	50	500	50	150	**1**	**10**
T_{range}(ns)	12.29	12.5	20	5.4	**700**	**70**
resolution (ps)	0.28*	1.09*	5.6	2.64*	**391***	**54***
Power(uW)	21000	2000	1700	3520	**1.5**	**56**
FoM(pJ/conv.)	-	0.86	-	0.19	**0.0076**	**0.112/0.018****

*Estimated resolution $(\sqrt{T_{\text{int},rms}^2\cdot 12})$.

**The FoM is calculated without distortion power.

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obtained as

$$ENOB_{\text{TDC}} = \frac{SNDR - 1.76}{6.02} \tag{3.4.5}$$

For comparison, a widely used figure of merit (FoM) is given as [4]

$$FoM_{TDC} = \frac{Power}{2^{ENOB} \cdot 2 \cdot BW} \tag{3.4.6}$$

The performance of TDC is tabulated in Table 3-1. With 1.5-μW power, 10.9 ENOB and 50-kHz bandwidth, the proposed circuit demonstrates the lowest FoM among the state-of-the-art TDC designs. Table 3-1 also shows the TDC performance while operating at 0.6-V supply. The TDC achieves an ENOD of 10 bits at 250-kHz signal bandwidth and draws a total power of 56 μW from 0.6-V supply. As the non-ideal effects associated with the switching noise and transistor leakage are alleviated in the proposed circuit technique, the trade-off between oscillation frequency and timing skew error is therefore relaxed such that the performance of the TDC can be optimized.

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3.5 Conclusion

This chapter presents a highly-digital ΔΣ TDC using a gated-free ring oscillator. Fabricated in a 90-nm CMOS process, the circuit achieves an ENOB of 10.9 bits with 50 kHz bandwidth while consuming 5 μA from a power supply of 0.3V. Operating at 0.6-V supply voltage, the proposed TDC achieves 10 bits ENOB with 250 kHz bandwidth and draws 93 μA from a power supply of 0.6V. It is well suited for low-cost and low-power time-to-digital conversions with sufficiently high resolution.

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Chapter 4

Time-Mode Capacitive Sensor Interface with Second-Order ΔΣ Time-to-Digital Converter

4.1 Introduction

Capacitive sensors present high power consumption and low conversion speed due to the use of analog-to-digital converter (ADC) and the capacitance-to-voltage circuits [15][16]. Additionally, the reduction of the supply voltage in nanometer technologies leads to the scaling difficulties in mixed-signal data conversion based on a signal representation in voltage-domain. In order to overcome the limitations that the ADC-based interface circuits present for capacitive sensor, several time-mode capacitive sensor interfaces has been published [17][18][19]. To achieve high resolution with energy efficiency, second-order ΔΣ modulator has been implemented in the proposed design. In this chapter, ΔΣ capacitance-to-digital (CDC) converter with capacitance-to-time converter and a proposed second-order ΔΣ time-to-digital (TDC) converter is presented. Instead of using the MASH architecture, the proposed ΔΣ TDC composed of only one oscillator and the Gated-delay buffers. Based on the concept of time register, the gated-delay buffers memorize the quantization error of the TDC and

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feedback to the input of the TDC to fulfill the second-order ΔΣ modulator. Due to the highly digital architecture and the signal representation in the time-domain, the TDC allows reducing the required supply voltage and the power consumption with sufficient resolution.

The rest of this chapter is organized as follows. Section 4.2 illustrates the architecture of the proposed second-order ΔΣ capacitance-to-digital converter, while detail circuit implementation and experimental results are presented in Section 4.3 and 4.4, respectively. Finally, a conclusion is provided in Section 4.5.

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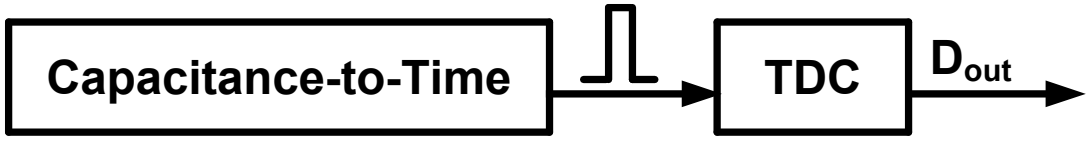

Fig. 4.1. Time-mode capacitance-to-digital converter.

4.2 Proposed capacitance-to-digital converter

The proposed capacitance-to-digital converter consists of a capacitance-to-time converter and a second-order ΔΣ TDC as shown in Fig 4.1. To better understand the operation principle of proposed second-order ΔΣ TDC, a 1-1 MASH ΔΣ TDC [13] will be illustrated before the proposed TDC.

4.2.1 1-1 MASH ΔΣ TDC

To enhance the TDC performance, high order ΔΣ TDC implemented using MASH structure has been demonstrated in [10][11]. In order to give an insight to the proposed

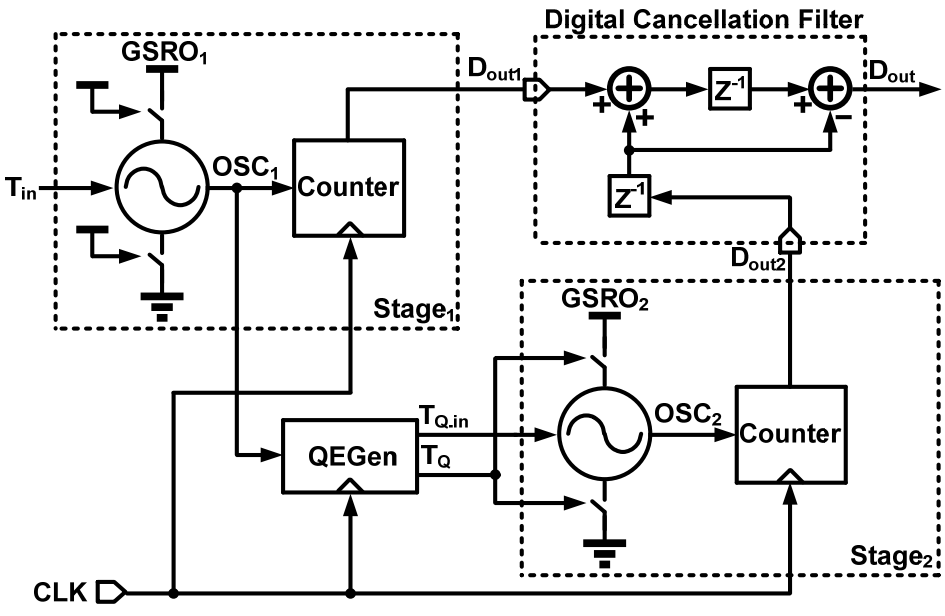

Fig. 4.2. Simplified block diagram of the 1-1 MASH ΔΣ TDC.

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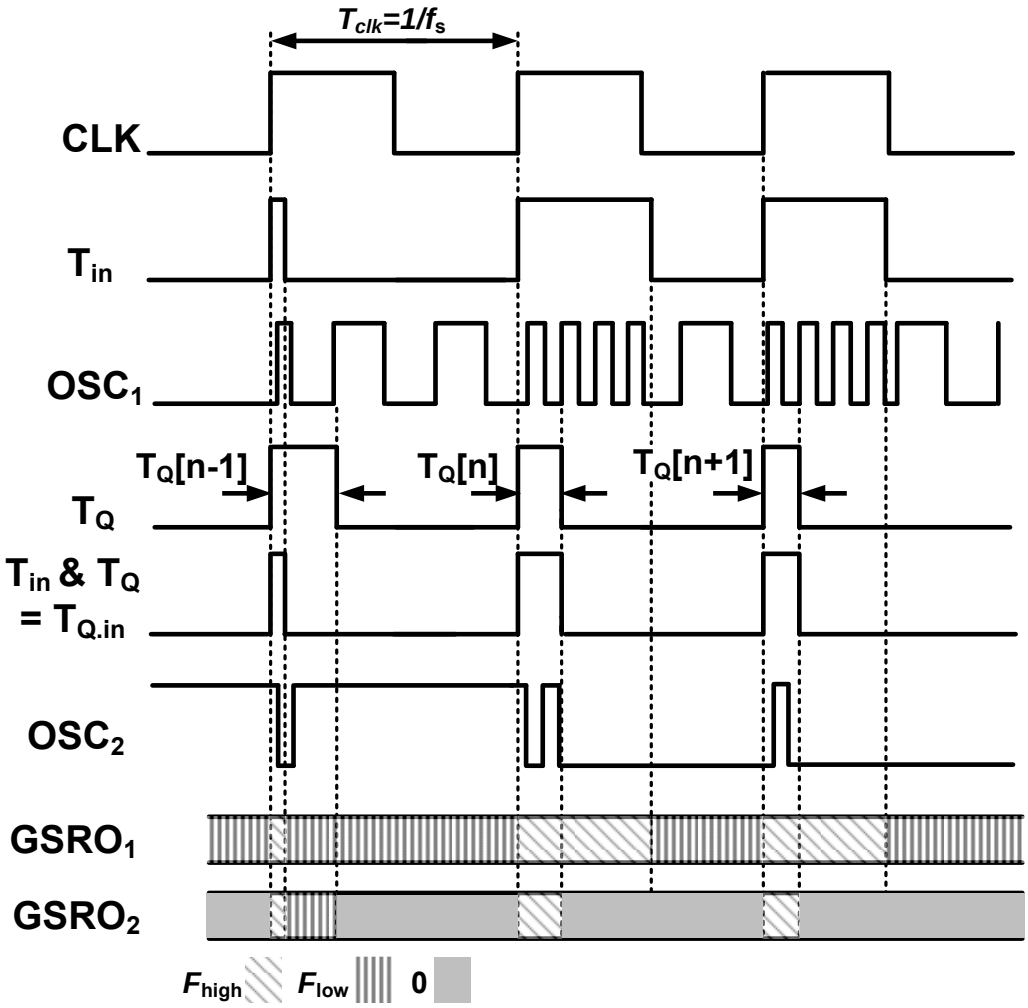

Fig. 4.3. Timing diagram of the 1-1 MASH ΔΣ TDC.

second-order ΔΣ TDC structure, a 1-1 MASH second-order ΔΣ TDC [13] is presented first. The time domain analysis of 1-1 MASH second-order ΔΣ TDC will be performed and the noise-shaping of the quantization noise power is proven by taking z-transform of the analysis results.

Simplified block diagram of a 1-1 MASH second-order ΔΣ TDC [13] and its timing diagram is shown in Fig. 4.2 and Fig 4.3, respectively. Controlled by two digital signals, a gated switched-ring oscillator (GSRO) has 3 oscillation frequencies: F_{high}, F_{low} and 0. The second-order ΔΣ TDC works as follows: The input T_{in} controls the $GSRO_1$ frequency. When the T_{in} becomes logic high, the $GSRO_1$ oscillates at high frequency

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F_{high}. The gated scheme is not used in the $GSRO_1$. Thus the $GSRO_1$ works as a switched-ring oscillator (SRO), and the first stage operates as a SRO-TDC [9]. The counter produces digital output by counting the rising edges of the $GSRO_1$. And the quantization error generator (QEgen) will propagate the quantization error of $stage_1$ to the input of the second gated switched-ring oscillator ($GSRO_2$). The frequency of the oscillator should be larger than the sampling frequency for QEgen to generate the quantization error every clock cycle. And the output of the two stages can be written as

$$D_{out1}[n]=\frac{T_{in}[n]}{T_{high}}+\frac{\left(T_{clk}-T_{in}[n]\right)}{T_{low}}+\frac{\left(\phi_{Q1}[n]-\phi_{Q1}[n-1]\right)}{2\pi} \tag{4.2.1}$$

$$D_{out2}[n]=\frac{T_{Q.in}[n]}{T_{high}}+\frac{\left(T_{Q}[n]-T_{Q.in}[n]\right)}{T_{low}}+\frac{\left(\phi_{Q2}[n]-\phi_{Q2}[n-1]\right)}{2\pi} \tag{4.2.2}$$

where

$$\frac{\phi_{Q1}[n]}{2\pi}=\frac{T_{Q.in}[n]}{T_{high}}+\frac{\left(T_{Q}[n]-T_{Q.in}[n]\right)}{T_{low}} \tag{4.2.3}$$

and ϕ_{Q1} and ϕ_{Q2} is the phase domain quantization error of $stage_1$ and $stage_2$, respectively. $T_{high}=1/F_{high}$, $T_{low}=1/F_{low}$ and T_{clk} is one sampling clock period. The equation (4.2.3) is true only when the frequency of the two oscillators $GSRO_1$ and $GSRO_2$ is perfectly matched otherwise the quantization error of $stage_1$ can't be completely cancelled. Combining (4.2.1), (4.2.2), and (4.2.3) the output of the 1-1 MASH second-order ΔΣ TDC is

$$D_{out}[n]=D_{out2}[n-2]+D_{out1}[n-1]-D_{out2}[n-1] \tag{4.2.4}$$

$$=\frac{T_{in}[n-1]}{T_{high}}+\frac{(T_{clk}-T_{in}[n-1])}{T_{low}}$$

$$-\frac{\phi_{Q2}[n-1]+2\cdot\phi_{Q2}[n-2]-\phi_{Q2}[n-3]}{2\pi}. \tag{4.2.5}$$

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Taking the z-transform of (4.2.5) yields

$$D_{\text{out}} = z^{-1}T_{in}\left(F_{\text{high}} - F_{\text{low}}\right) + T_{\text{clk}} \cdot F_{\text{low}} - \left(1 - z^{-1}\right)^2 \frac{\phi_{\text{Q2}}}{2\pi}. \quad (4.2.6)$$

Equation (4.2.6) shows that second-order shaping of the quantization error is achieved with this 1-1 MASH TDC.

4.2.2 Proposed second-order ΔΣ TDC

Instead of using 1-1 MASH architecture, a second-order ΔΣ TDC using error feedback structure is proposed in this time mode ΔΣ CDC. As shown in Fig. 4.4, the proposed ΔΣ TDC consists of a gated switched-ring oscillator (GSRO), a quantization error generator (QEgen), gated-delay buffers (GDBs), and a counter. The timing diagram of the proposed TDC shown in Fig. 4.5 which indicates the difference between a first-order ΔΣ TDC using switched-ring oscillator and the proposed TDC using gated switched-ring oscillator with error feedback structure. As the previous section described, the frequency of the SRO in a SRO-TDC is controlled by the input signal T_{in} and the digital output code of a SRO-TDC can be expressed as (4.2.1). Replacing the SRO with a GSRO and it can be seen from Fig. 4.5 that the GSRO has a gated state. This gated state is controlled by the output of the GDBs. And the frequency of the GSRO is still controlled by T_{in}. To allow a low frequency and low power operation, the proposed second-order ΔΣ TDC uses only one GSRO with a low gated time. The low gated time scheme mitigates the leakage effect of the GSRO without adding too much load capacitance to the ring oscillator. The detail operations of the TDC work as follows: The gated switched-ring oscillator will oscillate at the higher frequency when T_{in} is at logic high. And the counter counts the rising edge of the oscillator. Unlike the 1-1 MASH architecture, the quantization error generator will propagate the quantization error to

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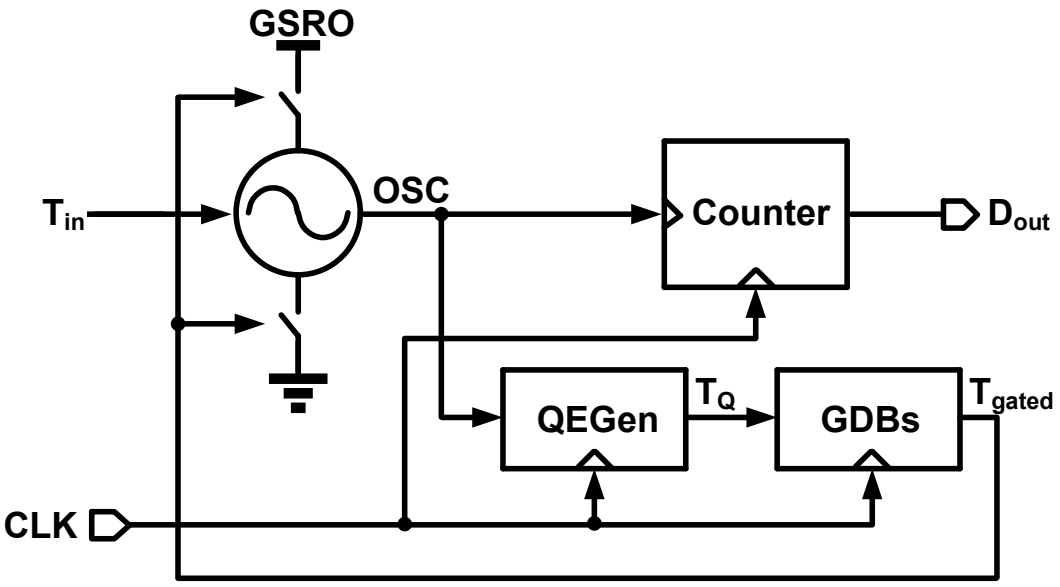

Fig. 4.4. Proposed second-order ΔΣ TDC.

gated-delay buffers. Then the time domain quantization error is memorized in gated-delay buffers. And the GDBs form a time interval T_{gated} and subtracted it from input time by gated the gated switched-ring oscillator. Hence the output of the proposed TDC is given by

$$D_{\text{out}}[\text{n}]=\frac{T_{\text{in}}[\text{n}]-T_{\text{off}}+T_Q[\text{n}-1]-T_Q[\text{n}]}{T_{\text{high}}}$$

$$+\frac{\left(T_{\text{clk}}-T_{in}[\text{n}]\right)}{T_{\text{low}}}+\frac{\left(-\phi_{\text{Q}}[\text{n}]+\phi_{\text{Q}}\ [\text{n}+1]\right)}{2\pi} \qquad (4.2.7)$$

where the phase domain quantization error

$$\phi_{\text{Q}}[\text{n}]=\frac{2\pi T_{\text{Q}}[\text{n}]}{T_{\text{high}}}, \qquad (4.2.8)$$

and T_{off} is a constant time interval. The magnitude of T_{off} will be described in section 4.3.3. And it should be noted that (4.2.8) is only valid when T_{in} is larger than $T_{\text{off}}+T_{\text{Q}}$. So the input time should always be larger than $T_{\text{off}}+T_{\text{Q}}$ to insure the second-order noise-shaping property of the proposed TDC. Since the required input time is shorter than the pulses generated by the capacitance-to-time converter from the parasitic

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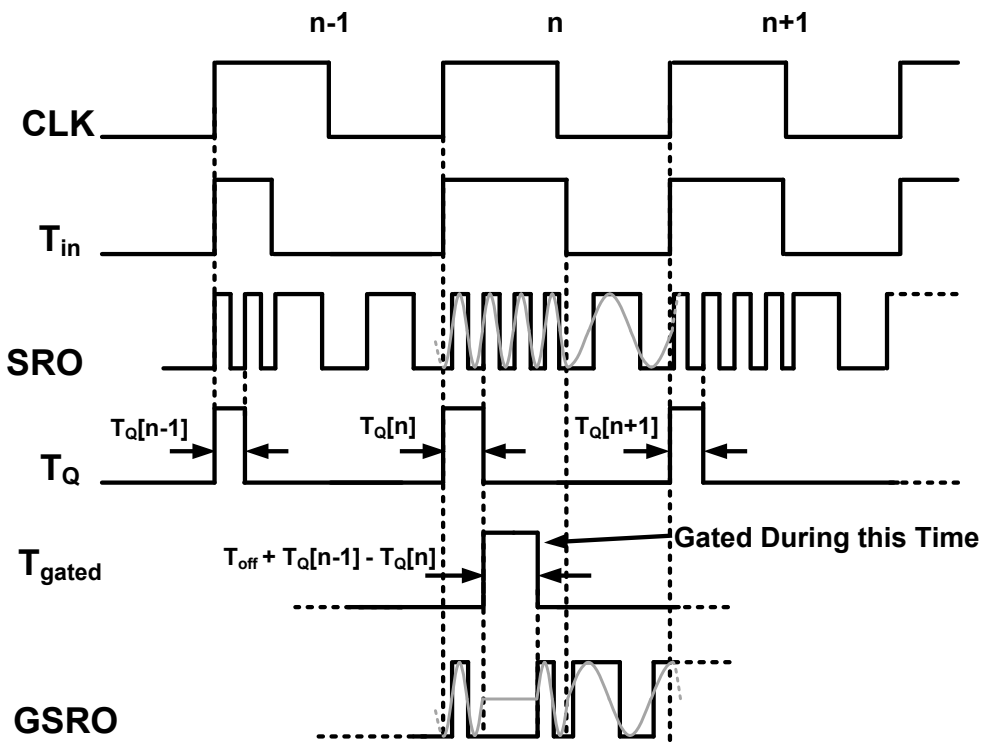

Fig. 4.5. Timing diagram of the proposed ΔΣ TDC.

capacitance, the proposed TDC works properly in the proposed capacitance-to-digital converter. Substituting (4.2.8) into (4.2.7), the output of the proposed TDC is given as

$$D_{\text{out}}[\text{n}] = T_{\text{in}}[\text{n}]\left(\frac{1}{T_{\text{high}}} - \frac{1}{T_{\text{low}}}\right) - \frac{T_{\text{off}}}{T_{\text{high}}} + \frac{T_{\text{clk}}}{T_{\text{low}}} + \frac{\phi_Q[\text{n+1}]-2\phi_Q[\text{n}]+\phi_Q[\text{n-1}]}{2\pi} \qquad (4.2.9)$$

With z-transform of (4.2.9), the digital code at the output can be expressed as

$$D_{\text{out}}(\text{z}) = T_{\text{in}}(\text{z})\cdot\left(\frac{1}{T_{\text{high}}} - \frac{1}{T_{\text{low}}}\right) - \frac{T_{\text{off}}}{T_{\text{high}}} + \frac{T_{\text{clk}}}{T_{\text{low}}} + \frac{\text{z}\cdot(1-\text{z}^{-1})^2\phi_Q(\text{z})}{2\pi}, \qquad (4.2.10)$$

showing a second-order noise shaping property for the TDC.

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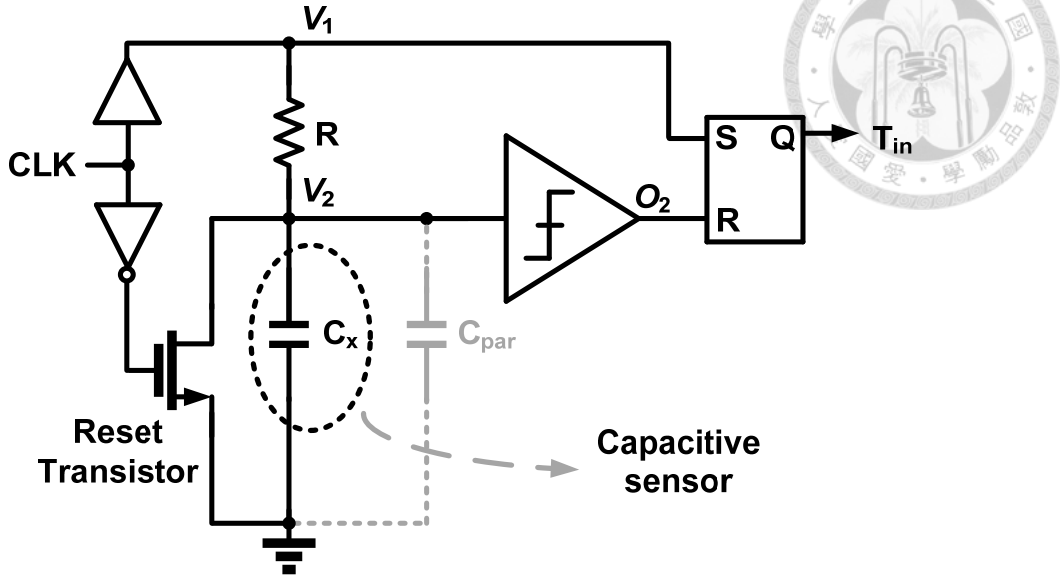
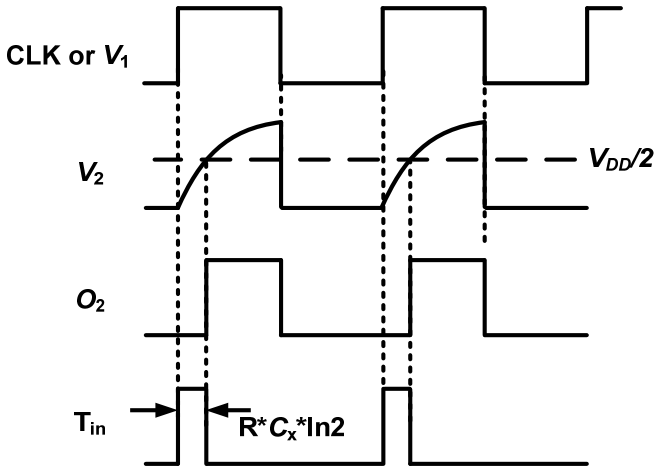


(a)



(b)

Fig. 4.6. (a) Capacitance-to-time converter and (b) its timing diagram.

4.2.3 Capacitance-to-time converter

As shown in Fig 4.6, the capacitance-to-time converter uses simple RC charging circuit with a comparator and a SR latch to produce pulses linearly proportional to sensor capacitance C_x [14]. After V_1 rises to V_{DD} the voltage at node V_2 can be expressed as

$$V_2(t) = V_{DD} \cdot \left(1 - e^{-t/RC_x}\right) \tag{4.2.11}$$

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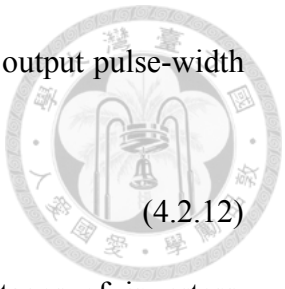

And the comparator threshold is designed to be $V_{DD}/2$. So that the output pulse-width is given by

$$T_{in} = R \cdot C_x \cdot ln2 \tag{4.2.12}$$

To save power the comparator is implemented using several stages of inverters. Though the inverter is often not used as a comparator because its threshold voltage is not well-defined, it is proper to be used as a threshold detector in this case. The transient timing diagram of the converter is shown in Fig. 3(b). It can be seen that the input range of the capacitance-to-time converter is defined by the resistor (R), comparator threshold (V_{thre}), clock period (T_{clk}), and the clock duty (D). So that the maximum sensing capacitance is

$$C_{max} = \frac{T_{clk} \cdot D}{R \cdot \ln\left[V_{DD}/(V_{DD} - V_{thre})\right]}. \tag{4.2.13}$$

In this design, T_{clk} is 1 μs, duty cycle is set to 80%, R is 150 kΩ, and V_{thre}, the inverter threshold is set to $V_{DD}/2$. This corresponds to a maximum sensing capacitance of 7.7-pF for the capacitance-to-time converter.

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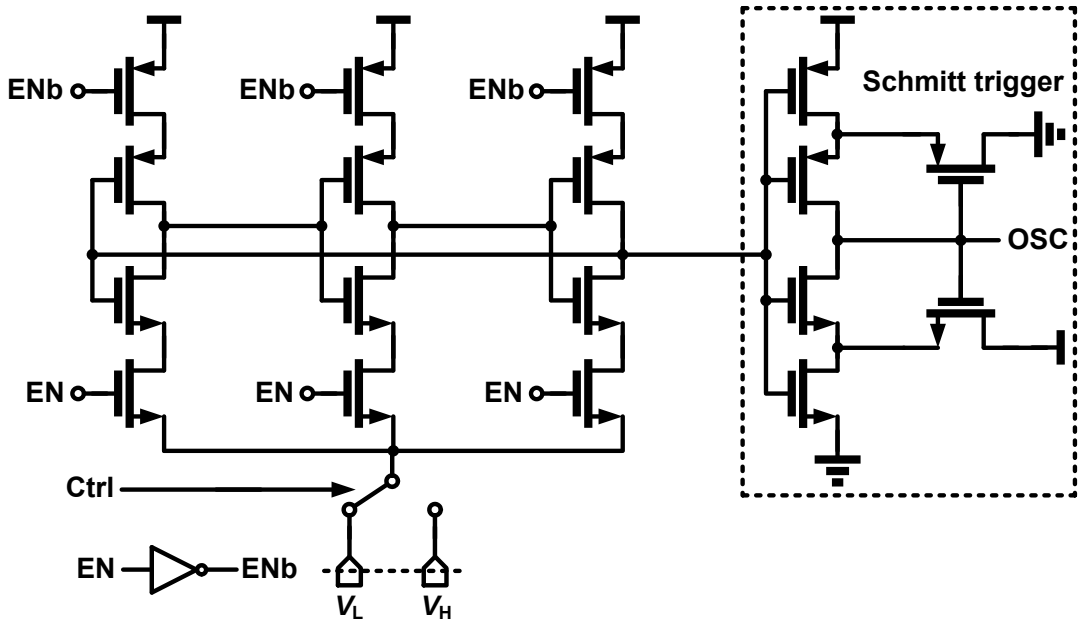

Fig. 4.7. Gated switched-ring oscillator.

4.3 Circuit implementation

4.3.1 Gated switched-ring oscillator

In order to achieve micro-power ΔΣ TDC, the GSRO is implemented using only three cascaded tri-state inverters shown in Fig. 4.7. And the frequency control is done by switching the ground voltage [9] of the cascaded inverters. Switching the ground voltage between V_L and V_H ensures fast switching frequency of the ring oscillator. An important issue should be addressed here is that a large phase error would be introduced in the gated state of the ring oscillator. This happened when the voltage of output stage is gated near the transition threshold of the output stage. The leakage may cause false transition at the oscillator output stage and will severely degrade the TDC performance. Simply place a Schmitt trigger at the output of the ring oscillator can solve this problem. The hysteresis characteristic of the Schmitt trigger allows some voltage margin to prevent false transition of the output stage.

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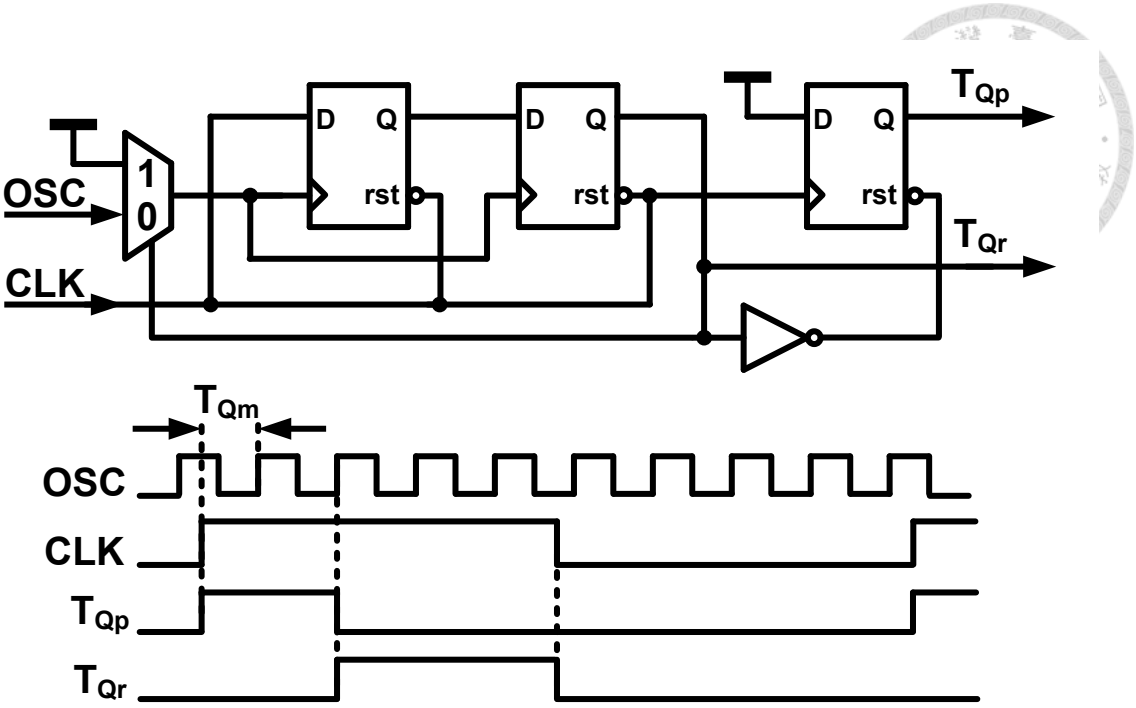

Fig. 4.8. Quantization error generator.

4.3.2 Quantization error generator

Figure 4.8 shows the detail implementation of the QEgen. Although the quantization error of the TDC, denoted as T_{Qm} in Fig. 4.8., can be generated by using one D flip-flop, the dead-zone problem of the D flip-flop may happened when the width of T_{Qm} is too small. Similar to the design in [13], the QEgen adds a static phase offset of 2π to avoid the dead-zone problem of the D flip-flop. Since the D flip-flop is unused after generating the output pulses, the high frequency signal *OSC* from ring oscillator toggling at the clocking gate of the D flip-flop wasted a lot of power. By adding a multiplexer in front of the clocking gate, the wasted power can be reduced. The QEgen generates two signals T_{Qp} and T_{Qr} to the GDBs. The time difference between the rising edges of the two signals is time domain quantization error T_Q plus a static offset time T_{high}.

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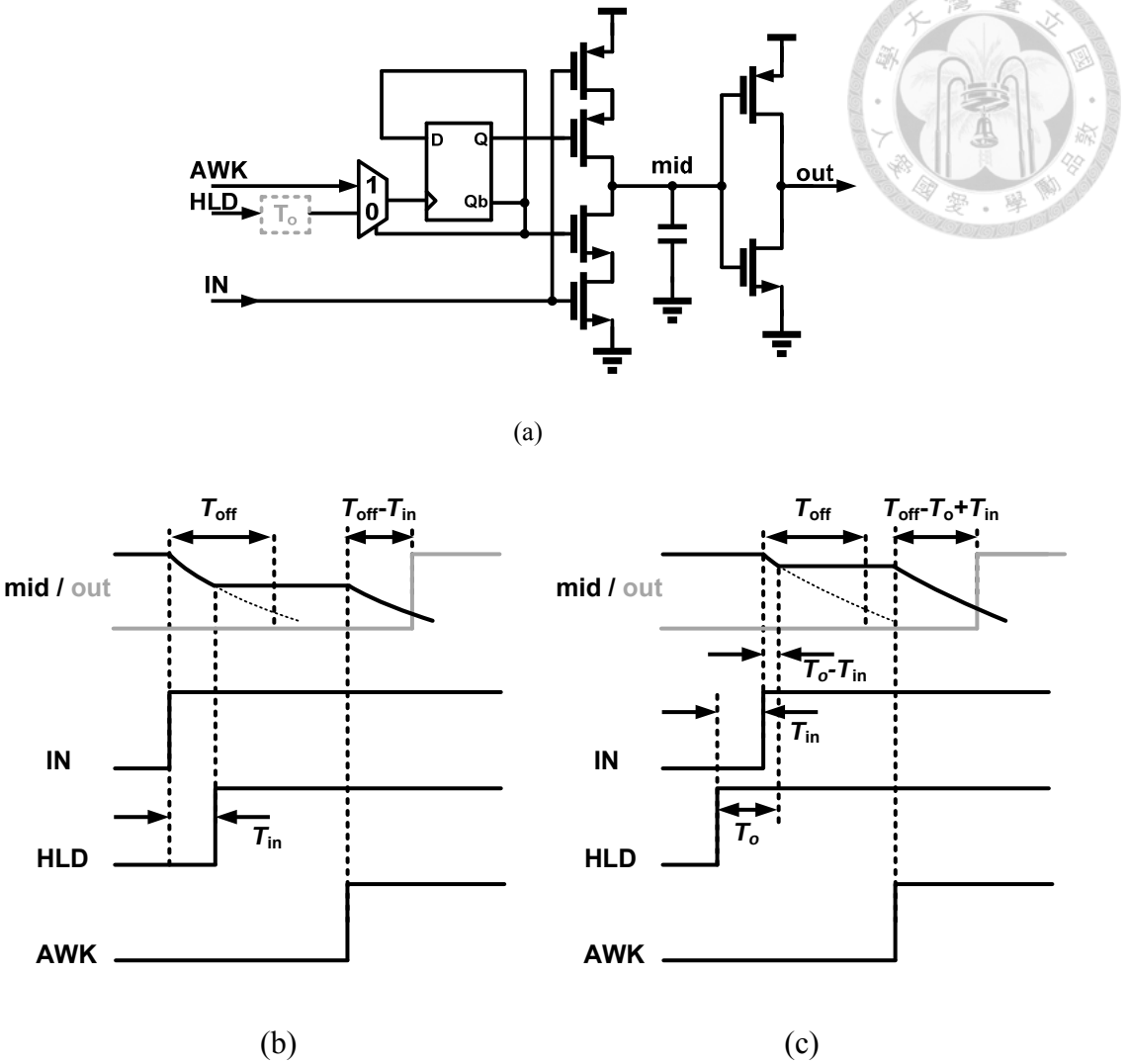

Fig. 4.9. (a) Gated-delay buffer unit and its timing diagram (b) without and (c) with delay cell T_o.

4.3.3 Gate-delay buffers

The schematic of a GDB unit is shown in Fig. 4.9(a). Based on the circuit proposed in [6], the GDB utilizes a time-to-voltage conversion and a gated scheme to memorize the time interval. As from the timing diagram in Fig. 4.9(b), the node *mid* is discharged from supply voltage after the signal *IN* is rising to logic high. And after the rising edge of *HLD*, the voltage of the node *mid* is held until the rising edge of *AWK*. Since the time for the node *mid* discharge from supply voltage to the output inverter threshold is

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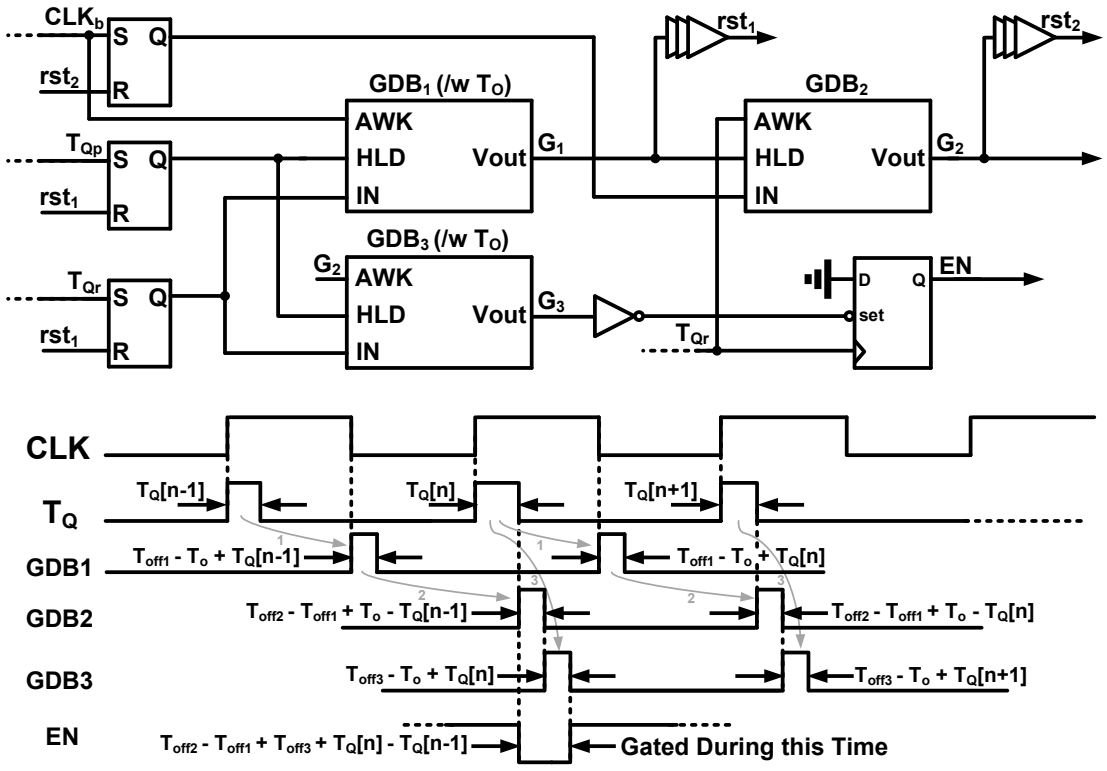

Fig. 4.10. Circuits schematic of the proposed error feedback structure.

constant, the time from the rising edge of *AWK* to the rising edge of *out* is T_{off} - T_{in}. Hence the time information can be shifted. Arbitrarily adding a delay T_o at *HLD* one can obtain the input time in another polarity as shown in Fig. 4.9(c). To make sure the GDB work functionally, the discharge time should be larger than the input time (T_{in}). If the GDB is implemented with the time delay T_o, the relationship between the design parameter is: $T_{off} > T_o > T_{in}$. The T_{off} is set to be $1.5 \cdot T_o$ and T_o is set to be $1.5 \cdot T_{in}$ to ensure that T_{off} is always larger than T_o and T_o is larger than T_{in} over PVT variations.

The detail schematic of the GDBs structure and its conceptual timing diagram is shown in Fig. 4.10. Three input signals fed to the three SR latches in this GDBs structure to provide adequate input time for the GDBs. It can be seen from Fig. 4.10 that the first gated-delay buffer (GDB_1) and the third gated-delay buffer (GDB_3) are identical and fed with the same input time. The two GDBs are used to obtain the

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positive quantization error of the TDC since the two GDBs is implemented with an extra time delay T_o. The GDB_1 shift the quantization error from the rising edge of the CLK signal to the falling edge of the CLK signal every clock cycle. The GDB_2 then obtains GDB_1 output time T_{off1} - T_o + T_Q[n-1] (T_{off1} - T_o +T_Q[n]) and shift it to the falling edge of T_Q[n] (T_Q[n+1]) and forms a time interval T_{off2} - T_{off1} + T_o - T_Q[n-1] (T_{off2} - T_{off1} + T_o - T_Q[n]). Then the GDB_3 will be awaked by the output of the GDB_2. Thus the GDB_3 generates a time interval of T_{off3} - T_o + T_Q[n] (T_{off3} - T_o + T_Q[n+1]) right after the end of the GDB_2 output time. So the overall gated time is T_{off2} - T_{off1} + T_{off3} + T_Q[n] - T_Q[n-1] as shown in Fig. 4.10. Considering the design constraints mentioned above, the maximum gated time can be obtained as $T_{g,max} = 3.25T_Q = 3.25T_{high}$.

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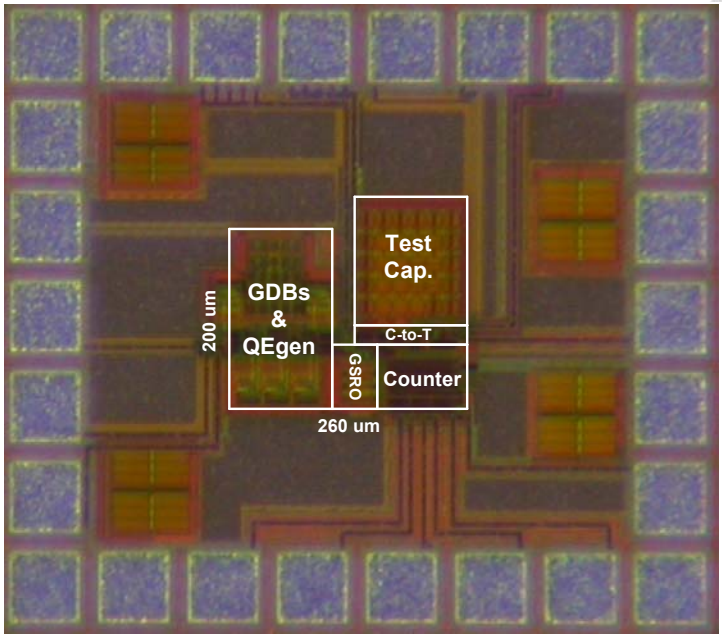

Fig. 4.11. Chip photo.

4.4 Experimental Results

Fig. 4.11 shows the microphotograph of the proposed capacitance-to-digital converter with a core area of 0.042 μm^2. Fabricated in 90-nm CMOS process, this CDC consumes 11 μW from 0.6-V supply voltage. The $sinc^2$ digital filter of the delta-sigma modulator is fulfilled using MATLAB.

The measurements have been divided into two parts: the test of noise performance with different capacitance and the linearity test using four combinations of three capacitors. Fig. 4.12 shows the time mode ΔΣ modulator's output spectrum. It can be observed that the 40dB/decade of the quantization noise is achieved in the second-order ΔΣ CDC. The low frequency noise of the proposed CDC mainly comes from the flicker noise of the comparator in the capacitance-to-time converter.

After two-point calibration, the noise performance of the fabricated circuit was

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evaluated by obtained the RMS noise of the proposed CDC as shown in Fig. 4.13. With maximum input capacitance of 5pF, the RMS noise of the prototype chip is 1.63fF. The signal-to-noise ratio (SNR) is calculated as

$$SNR = 20\log(\frac{Cap.Range/2\sqrt{2}}{Cap.Resolution}). \quad (4.4.1)$$

From (4.4.1), the SNR of the proposed time-mode capacitance-to-digital converter is 60.7 and the effective number of bits (ENOB) is 9.8.

Different from the static test in the voltage-domain ADC, it's hard to generate capacitive ramp input. And one might expect that it is possible to test the CDC with three or more off-chip capacitor with a precise impedance analyzer. Practically, this method does not work because of the parasitic capacitance of the capacitor. The parasitic capacitance changes every time the capacitor moves its position. Hence, to characterize the linearity of the proposed CDC, four combinations of three capacitors is used to test the CDC as shown in Fig. 4.14. The linearity of the CDC is calculated to be

$$\lambda = \frac{D_4 - D_3}{D_2 - D_1} - 1 \quad (4.4.2)$$

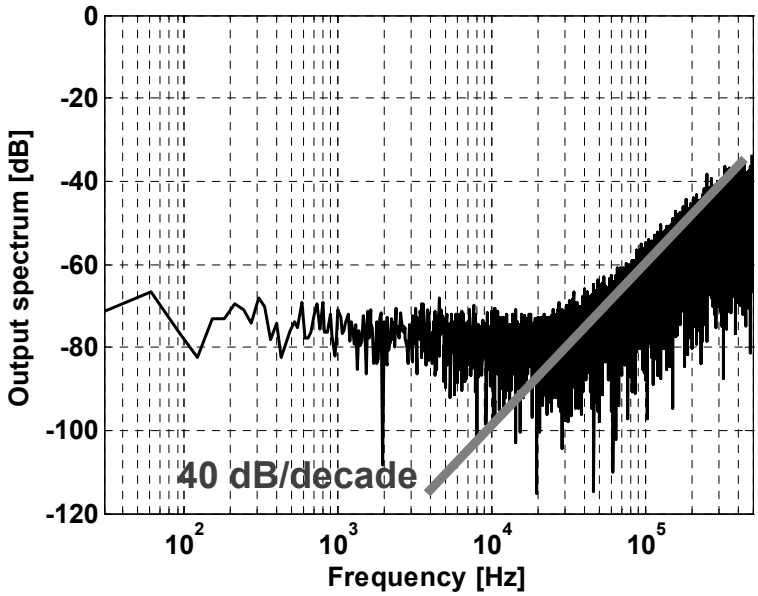

Fig. 4.12. Output spectrum with 3pF input.

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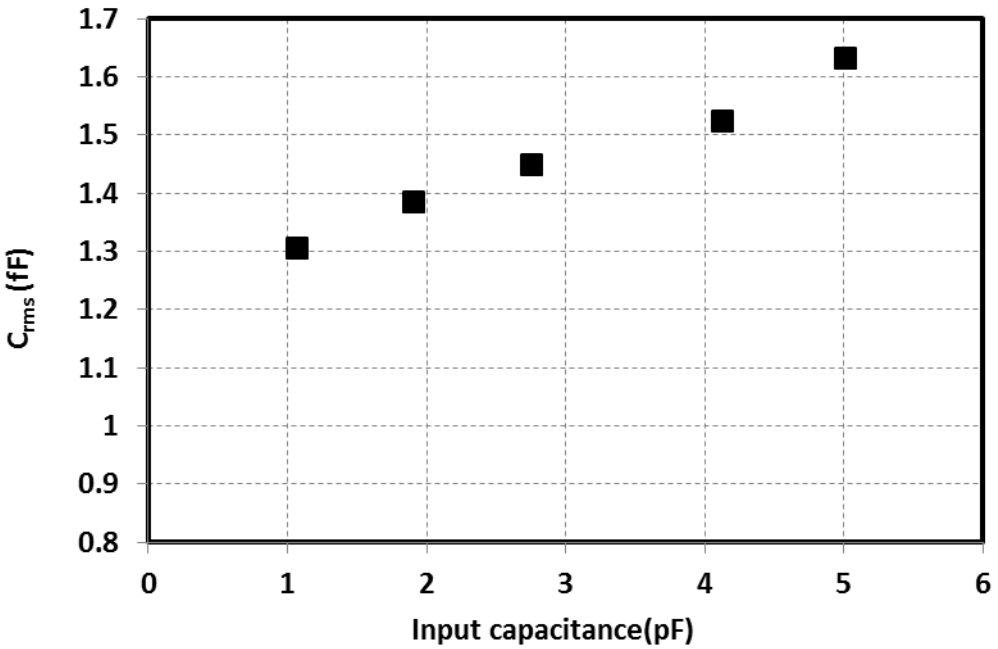

Fig. 4.13. Measured RMS noise of the CDC.

where $D_{1\sim4}$ are the corresponding digital output of the four combinations input capacitance $C_{1\sim4}$. With two on-chip capacitors C_1 and C_{on} and an off-chip capacitor C_{off}, the linearity of the CDC is obtained by first measuring the two combinations C_2 and C_4

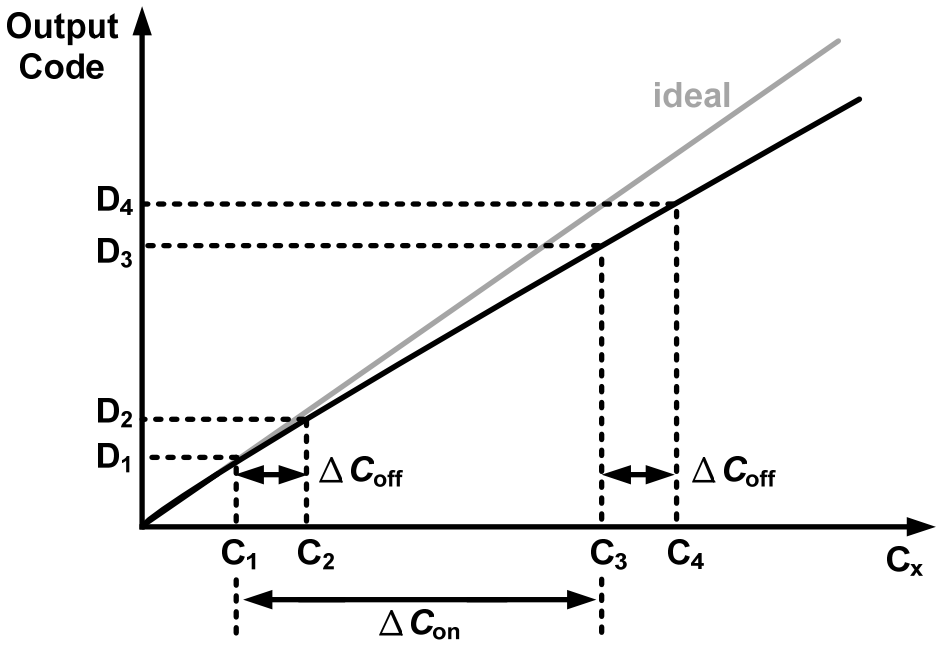

Fig. 4.14. Linearity test setup

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Table 4-1 COMPARE WITH STATE-OF-THE-ART

	[15]	[16]	[17]	[18]	[19]	**This work**
Supply(V)	1.2	1.2/0.9	N/A	3.3	1	**0.6**
Power(uW)	10.3	0.16	1.86	210	14	**11**
Meas.T(ms)	0.8	4	0.019	7.6	0.21	**0.25**
Tech(nm)	160	180	40	350	160	**90**
Area(mm^2)	0.28	0.49	0.0017	0.51	0.05	**0.042**
FoM(pJ/step)	3.8	1.3	0.14	140	1.87	**3.06**
ENOB	12.5	11.8	7.96	13.5	10.6	**9.81**
Type	ΔΣ	SAR	IDCD	PWM	PWM	**TD ΔΣ**
Input Range(pF)	0.54~1.06	2.5~75.3	0.7-10000	0-6.8	0~8	**0~5**

then remove the off-chip capacitor to measure C_1 and C_3. Using this method, the linearity of the proposed CDC is obtained as 8.5 bits.

Although this method can't characterize the whole transfer curve of the proposed CDC, it's well suited for verifying the nonlinearity of the proposed CDC. Since the TDC measured the time interval by counting the rising edge of the ring oscillator during the time interval, the proposed TDC is inherently linear. Therefore, the overall linearity is limited by the capacitance-to-time conversion. Due to the slew rate of the RC charge circuit varied with different input capacitors, the comparator exhibits different delay with different input capacitors. In fact, the simulated transfer curve of the CDC is just as shown in Fig. 4.14.

For comparison, the figure of merit (FoM) defined as

$$FoM = \frac{Power \cdot Meas.T}{2^{ENOB}}, \tag{4.4.3}$$

is used in Table-4.1. The proposed CDC achieves 9.81 bits resolution while operate at 0.6-V supply voltage. The *FoM* of the CDC is calculated to be 3.06 pJ/step, which is comparable to the state-of-the-arts CDC.

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4.5 Conclusion

A time-mode capacitance-to-digital converter is presented in this section. Fabricated in 90-nm CMOS process, the CDC achieves an ENOB of 9.8 bits with 2 kHz bandwidth while consuming 11 μW from 0.6-V supply. By using time-mode operation, the supply voltage can be reduced while achieving sufficient resolution. With highly digital architecture, proposed CDC can be easily designed in advanced CMOS technology.

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Chapter 5

Conclusion

In the thesis, low power ΔΣ TDC design technique and its application to CDC is proposed. In Chapter 3, a ΔΣ TDC with gated-free ring oscillator is proposed. Using a gated-free ring oscillator and leakage-suppression switches in the circuit implementation, non-ideal effects associated with switching noise and transistor leakage can be reduced. Consequently, the trade-off between oscillation frequency and timing skew error caused by circuit non-idealities is relaxed such that the performance of the TDC can be optimized. By using a standard 90-nm CMOS process, the fabricated circuit exhibits an ENOB of 10.9 bits with 50 kHz bandwidth while consuming 5 μA from a power supply of 0.3V. Based on the measurement results, the TDC achieves a *FoM* of 7.6fJ/conversion which is the best among state-of-the-art TDCs.

Base on the same time-mode design technique, a second-order ΔΣ TDC is added in the time-mode capacitive sensor interface at Chapter 4. By leveraging the time-mode design technique with a highly digital capacitance-to-time converter, a low voltage operation can be applied to the CDC. As a result, the power consumption of the CDC is reduced while achieving sufficient resolution. By using a standard 90-nm CMOS process, the proposed CDC with the second order ΔΣ TDC is exhibited an ENOB of 9.8

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bits with 0.25 ms measurement time. With a full-scale input of 5pF, the CDC consumes a total power of 11 μW from 0.6-V supply. The *FoM* of the CDC is calculated to be 3.1 pJ/step, which is comparable to the state-of-the-art CDC.

With the proposed design technique, the TDC is capable of achieving high resolution with low power. The high performance TDC makes the time-mode signal processing a promising way in the future design.

doi:10.6342/NTU201601745

Reference

[1] P. Dudek, S. Szczepanski and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line", *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 240-247, 2000.

[2] J. Yu , F. F. Dai and R. C. Jaeger, "A 12 bit Vernier ring time-to-digital converter in 0.13 μm digital CMOS technology", *IEEE J. Solid-State Circuits*, vol. 45, pp. 830-842, 2010.

[3] M. Lee and A. A. Abidi, "A 9 b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that amplifies a time residue", *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769-777, 2008.

[4] A. Mäntyniemi, T. Rahkonen and J. Kostamovaara, "A CMOS time-to-digital converter (TDC) based on a cyclic time domain successive approximation interpolation method", *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3067-3078, 2009.

[5] J.-S. Kim, Y.-H. Seo, Y. Suh, H.-J. Park and J.-Y. Sim, "A 300-ms/s, 1.76-ps-resolution, 10-b asynchronous pipelined time-to-digital converter with on-chip digital background calibration in 0.13 um CMOS", *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 516-526, 2013.

[6] S.-J. Kim, T. Kim, and H. Park, “A 0.63ps, 12b, synchronous cyclic TDC using a time adder for on-chip jitter measurement of a SoC in 28nm CMOS technology”,

doi:10.6342/NTU201601745

in *VLSI Circuits Dig. Tech. Papers*, Jun. 2014.

[7] S.-J. Kim, W. Kim, M. Song, J. Kim, T. Kim, and H. Park, “A 0.6 V 1.17 ps PVT-tolerant and synthesizable time-to-digital converter using stochastic phase interpolation with 16× spatial redundancy in 14 nm FinFET technology,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[8] M. Z. Straayer and M. H. Perrott, "A multi-path gated ring oscillator TDC with first-order noise shaping", *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1089-1098, 2009.

[9] A. Elshazly, S. Rao, B. Young and P. K. Hanumolu, "A noise-shaping time-to-digital converter using switched-ring oscillators—Analysis, design, and measurement techniques", *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1184-1197, 2014.

[10] Y. Cao, W. D. Cock, M. Steyaert and P. Leroux, "1-1-1 MASH ΔΣ time-to-digital converters with 6 ps resolution and third-order noise-shaping", *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2093-2106, 2012.

[11] W. Yu, K. Kim and S. Cho, "A 0.22 ps rms integrated noise 15 MHz bandwidth fourth-order ΔΣ time-to-digital converter using time-domain error-feedback filter", *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1251-1262, 2015.

[12] K. Ishida, K. Kanda, A. Tamtrakarn, H. Kawaguchi, and T. Sakurai, “Managing sub-threshold leakage in charge-based analog circuits with low-VTH transistors by analog T- switch (AT-switch) and super cut-off CMOS (SCCMOS),” *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 859–867, Apr.2006.

[13] W. Yu, "A 148 fs_{rms} integrated noise 4 MHz bandwidth second-order ΔΣ

doi:10.6342/NTU201601745

time-to-digital converter with gated switched-ring oscillator", *IEEE Trans. Circuits Syst. I*, vol. 61, no. 8, pp. 2281-2289, 2014.

[14] J. H.-L. Lu , M. Inerowicz , S. Joo , J. K. Kwon and B. Jung, "A low-power, wide-dynamic-range semi-digital universal sensor readout circuit using pulse width modulation", *IEEE Sensors J.*, vol. 11, pp. 1134-1144, 2011.

[15] Z. Tan, R. Daamen, A. Humbert, Y. Ponomarev, Y. Chae and M. Pertijs, "A 1.2-V 8.3-nJ CMOS humidity sensor for RFID applications", *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2469-2477, 2013.

[16] H. Ha, D. Sylvester, D. Blaauw and J. Sim, "A 160 nW 63.9 fJ/conversion-step capacitance-to-digital converter for ultra-low-power wireless sensor nodes", *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 220-221.

[17] W. Jung, S. Jeong, S. Oh, D. Sylvester and D. Blaauw, "A 0.7 pF-to-10 nF fully digital capacitance-to-digital converter using iterative delay-chain discharge", *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 484-485.

[18] Z. Tan, S. Shalmany, G. Meijer and M. Pertijs, "An energy-efficient 15-bit capacitive-sensor interface based on period modulation", *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1703-1711, 2012.

[19] Y. He, Z. Chang, L. Pakula, S.-H Shalmany and M. Pertijs, " A 0.05mm^2 1V capacitance-to-digital converter based on period modulation", *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 486-487.

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