國立臺灣大學電機資訊學院電機工程學系

碩士論文

Department of Electrical Engineering
College of Electrical Engineering and Computer Science
National Taiwan University

Master Thesis

搭載動態偏壓導通時間產生器之新型電荷幫浦式固定導通時間控制降壓型轉換器設計與實現

Design and Implementation of A Novel Charge-Pump Constant On-Time Controlled Buck Converter with Dynamic-Biased On-Time Generator

徐士傑

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中華民國 109 年 5 月

May, 2020

doi:10.6342/NTU202000925

國立臺灣大學碩士學位論文
口試委員會審定書

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本論文係徐士傑君（學號 R06921022）在國立臺灣大學電機工程學系完成之碩士學位論文，於民國 109 年 5 月 29 日承下列考試委員審查通過及口試及格，特此證明。

口試委員：陳昇然 （簽名）

（指導教授）

劉作堂 陳耀銘

系主任 吳忠幟 （簽名）

Acknowledgements

First of all, I would like to express my sincere gratitude to my advisor, Dr. Jim Chen, for his guidance, encouragement, and patience. I benefited a lot from his critical challenge and helpful suggestions during every discussion throughout these years of master's study. He is always generous and supportive to me for conference, internship, exchange and many other opportunities. Thank him for giving me a lot of flexibilities to explore every possibility in both research and life. Without him, it won't be possible for me to achieve what I have done today.

I would also like to give specific appreciation to Prof. Tsorng-Juu Liang and Prof. Chien-Hung Tsai. They led me into the field of Power Electronics and helped me build up the fundamental knowledge of power management IC design. Both of them have a great impact on my life and my future career.

In addition, I would like to thank to Prof. Yaow-Ming Chen and Prof. Shen-Iuan Liu for serving as my oral defense committee members. Their insightful comments and valuable suggestions inspire me to look an issue from different angles.

I am deeply indebted to the PELAB members at NTU, especially for the Power IC group. It has been an honor to collaborate with intelligent, hardworking and friendly colleges: Mr. Ting-Hung Wang, Mr. Yuan-Chih Lin, Mr. Chia-Sung Yu, Mr. Ching-Hsiang Cheng, Mr. Chieh-Ju Tsai, Mr. Ding-Tang Chen, Mr. Zheng-Zih Yuan, Mr. Yu-Chen Li, Mr. Sheng-Hsiang Pan, Mr. Chi-Hsin Kuo, Mr. Ray Wu, Mr. Wen-Chin Liu, Mr. Jheng-An Juan Lu, Mr. Tzu-Hao Chien, Mr. Sheng Teng Li, Mr. Chang-Yang Hong, Mr. Teng Chang, Mr. Pin-Ying Wang, Mr. Ping-Kun Chou, Mr. Yen-Ming Chen, Mr. Cheng-Chieh Hu, and Mr. Joseph Chao. I cherish the moment when we stay numerous day and night together in the lab and encourage each other. They bring me a lot of fun and make the life of my master's study delightful and memorable.

doi:10.6342/NTU202000925

I am also beholden to Novatek Microelectronics Cooperation and Hon Hai Technology Group for providing scholarship to me.

Last but not least, I would like to thank my parents, Jin-Wang Hsu and Ming-Jing Lin, for their endless love and unconditional support. Because of them, I can pursue my master degree without the worries behind.

I would like to give special mention to my college, Mr. Chieh-Ju Tsai, who came up with the idea of the proposed CPCOT control scheme. Thank him for his generous helping, guidance and expert knowledge for my research.

I would also like to thank Taiwan Semiconductor Research Institute (TSRI) for chip fabrication support and SIMPLIS Technologies Corporation, U.S.A, for providing SIMPLIS simulation tool.

doi:10.6342/NTU202000925

中文摘要

近年來，漣波調變固定導通時間控制因為具有快速負載暫態響應、高輕載效率及架構簡單的特性，被廣泛應用於電源管理晶片。在電腦、智慧型手機等許多消費性電子產品中，為了縮小體積並且達到低輸出漣波電壓的需求，具低等效串聯電阻的積層陶瓷電容經常被使用於轉換器的輸出電容。然而，使用積層陶瓷電容之漣波調變固定導通時間控制降壓型電源轉換器可能會面臨到次斜波震盪的問題。

為了解決上述的次斜波問題，本論文提出了電荷幫浦式固定導通時間控制。此控制架構同時保有傳統漣波調變固定導通時間控制之快速負載暫態響應及高輕載效率的優點。除此之外，本論文也提出了動態偏壓導通時間產生器之技術，設法減低控制器之靜態電流消耗。

上述所提出之控制架構晶片使用台積電 0.18 μm CMOS 製程實現，可應用在切換頻率高達 8 百萬赫茲的降壓型電源轉換器中。此外，本論文利用描述函數的數學分析對電荷幫浦式固定導通時間控制架構推導小信號模型，進而分析系統穩定度及暫態響應。最後，透過模擬及實測結果驗證所提出的控制理論。量測結果顯示當輸入電壓為 3.3 伏特時，此降壓型轉換器可以操作在 0.25 安培至 1.25 安培的負載電流並可提供 0.6 伏特至 1.3 伏特的輸出電壓。當輸出電壓為 1.0 伏特，負載由 0.25 安培上升至 1.25 安培的暫態回復時間為 1.5 微秒，量測到的輸出壓降為 60 毫伏特。

關鍵字-降壓型電源轉換器、電源管理晶片、漣波調變固定導通時間控制、電荷幫浦式固定導通時間控制、描述函數、小信號模型。

doi:10.6342/NTU202000925

Abstract

Recently, ripple-based constant on-time (RBCOT) control has been widely used in power management integrated circuit (PMIC) due to features of fast load transient response, high light-load efficiency and simple implementation. In many applications such as personal computers, smartphones, and other consumer electronics, multilayer ceramic capacitors with low equivalent series resistance (ESR) are preferred because of compact size and small output voltage ripple requirement. However, a buck converter with RBCOT control may encounter the subharmonic oscillation, especially while low ESR ceramic capacitors are used as converter's output capacitors.

In this thesis, a charge-pump constant on-time (CPCOT) control scheme is proposed to overcome the subharmonic issue. This control method can also achieve fast transient response and maintain high efficiency under the light-load condition, which are the inherent advantages of RBCOT control scheme. In addition, a dynamic-biased technique for on-time generator is introduced to reduce quiescent current of the controller.

The proposed control was implemented into a monolithic IC using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm CMOS process for a buck converter with switching frequency up to 8 MHz. Furthermore, small-signal model of the CPCOT control was derived based on the describing function (DF) technique to predict system stability and transient response. Finally, simulation and measurement results are given to verify the proposed concepts. The measurement results show that the buck converter can operate under load current between 0.25 A and 1.25 A and produce output voltage from 0.6 V to 1.3 V while the input voltage is 3.3 V. The measured undershoot is 60 mV with 1.5 μs settling time when the load current is increased from 0.25 A to 1.25 A under 1.0 V output voltage.

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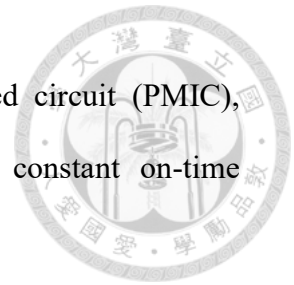

Index Terms—buck converter, power management integrated circuit (PMIC), ripple-based constant on-time (RBCOT) control, charge-pump constant on-time (CPCOT) control, describing function (DF), small signal model

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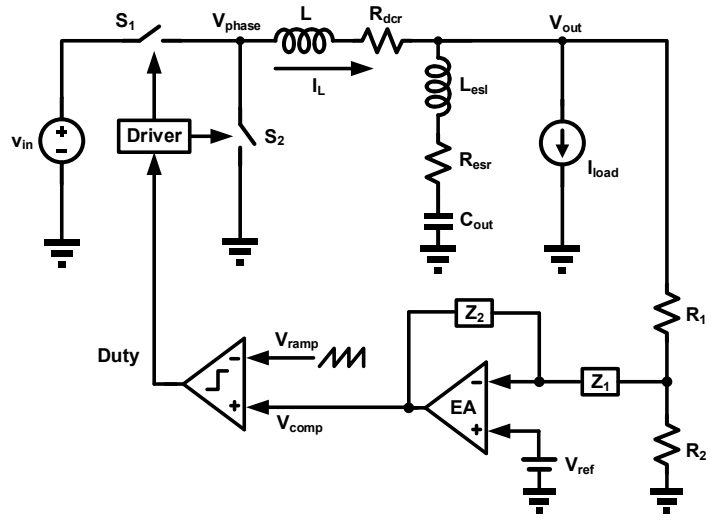
Chapter 1 Introduction

1.1 Research Background

Generally speaking, control schemes for DC-DC converter can be classified into three types: voltage mode control, current mode control, and ripple-based control. Fig. 1.1 shows the simplified circuit diagrams of the three different control methods for buck converter. S_1 and S_2 are high-side and low-side switches of buck converter respectively. R_{esr} and L_{esl} are equivalent series resistance (ESR) and equivalent series inductance (ESL) of the output capacitor C_{out}, and R_{dcr} is the DC resistance (DCR) of the inductor L. Constant on-time control, which is one of ripple-based control techniques, has gained much more attention in point-of-load (POL) buck converters application recently. Compared with the traditional voltage mode and current mode control, this control structure has the following three main features: 1) simple circuit architecture without any error amplifier compensation and current sensing network, 2) fast load transient response because of direct output voltage feedback, and 3) good light-load efficiency due to inherent characteristic of switching frequency reduction in discontinuous conduction mode (DCM).



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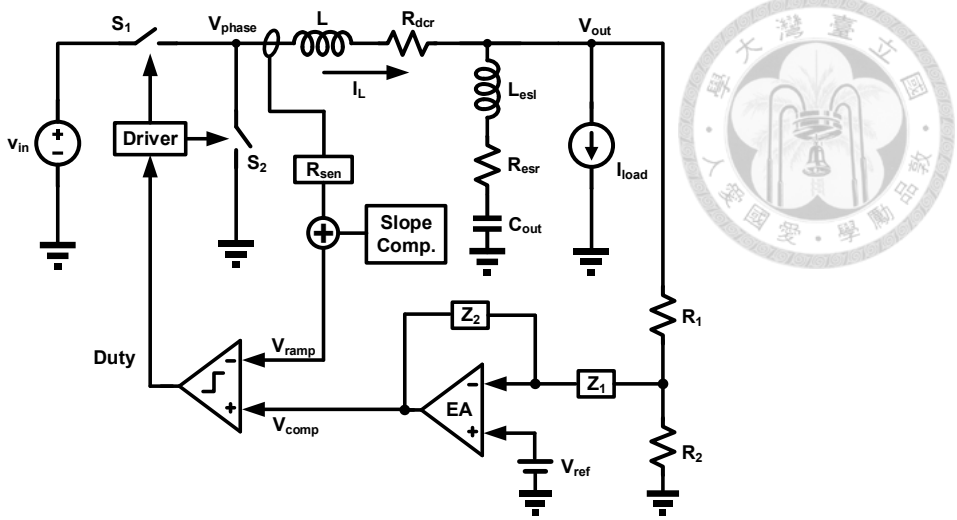

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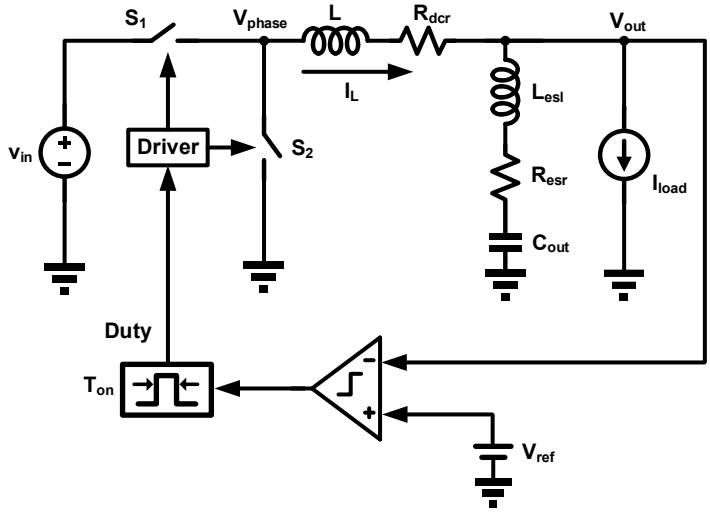

(c)

Fig. 1.1 Circuit diagrams of different control methods for buck converter: (a) voltage mode control, (b) current mode control, and (c) ripple-based control

Nowadays, computing and mobile devices, such as personal computers, laptops and smartphones have become a large market for the power supply industry. Aggressive use of these devices has put forward more challenging requirements for their diverse applications, increasing functionalities and decreasing size. Therefore, the demand for DC-DC buck converter, which is core of power management integrated circuit (PMIC), becomes more and more stringent. To achieve high performance, a buck converter is required to have fast transient response, large output load current, small output voltage ripple, high efficiency, and compact size.

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In recent years, the high switching frequency operation is preferred to shrink inductor and output capacitor size on printed-circuit-board (PCB) and improve the load transient response. Fig. 1.2 shows the vision for evolution of power supply on chip (PwrSoC) technology [1]. The ultimate target is to develop new miniaturized product formats that can be referred to as power supply in package (PwrSiP) and power supply on chip (PwrSoC). Thus, ripple-based control schemes, such as constant on-time control, have been widely used because they are more appropriate for high switching frequency operation than traditional voltage mode or current mode control, which needs large current consumption error amplifiers or complex current sensing network when the switching frequency increases.

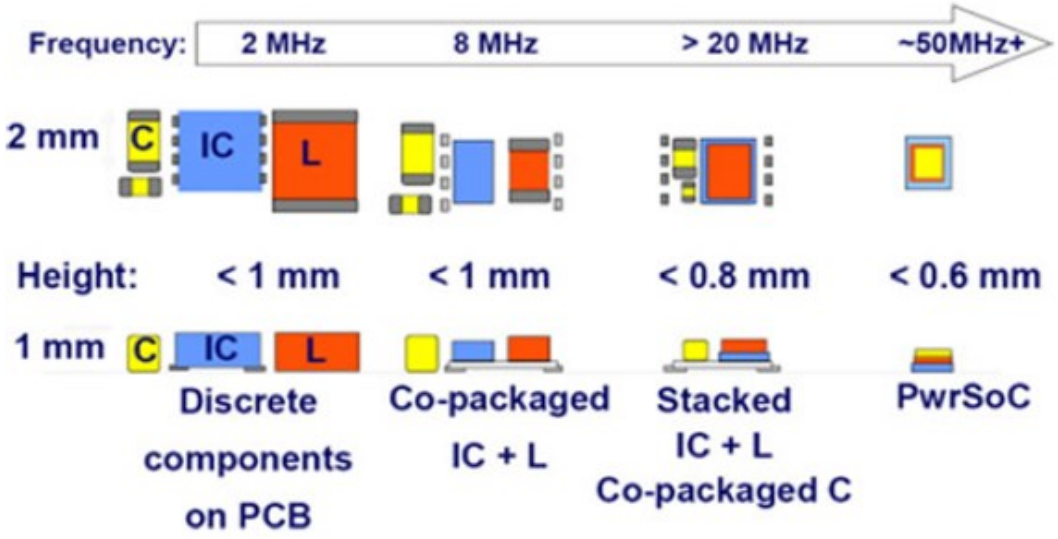

Fig. 1.2 Vision for evolution of PwrSoC technology [1]

As technologies blossoming, the central processor unit (CPU) development rapidly progresses. The specification of the maximum current slew rate of the CPU is important for the design of the power supply, in particular, the output filter size and control bandwidth. As a result of persistent high operating clock frequency and growing current demand, the current slew rate of the CPU has dramatically increased and could be higher than one ampere per nanosecond, as shown in Fig. 1.3 [2].

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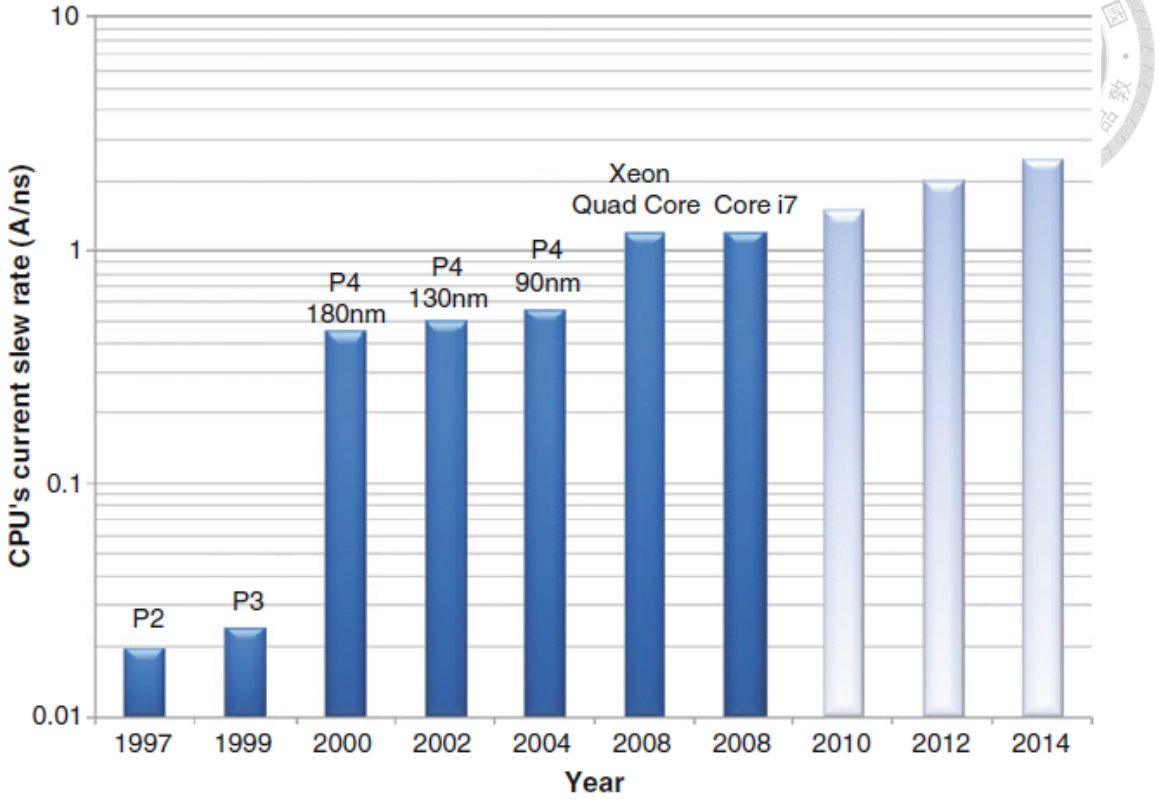

Fig. 1.3 Current slew rate evolution of Intel® microprocessor [2]

Fig. 1.4 shows the transient waveform of voltage regulator (VR) output voltage under the step load current change of CPU. For load step-up, output voltage should drop down and settle within the tolerance band. Accordingly, the dc-dc converter supplying power to CPU is expected to accommodate such a drastic current change immediately. Otherwise, the large undershoot may cause system lock-up or data corruption. To maintain proper and reliable system operation, the VR of CPU relies on many bulky output capacitors on the motherboards to reduce voltage droop during load transient. Fig. 1.5 shows today's motherboard using Intel's quad-core i7 microprocessor for a desktop computer [3].

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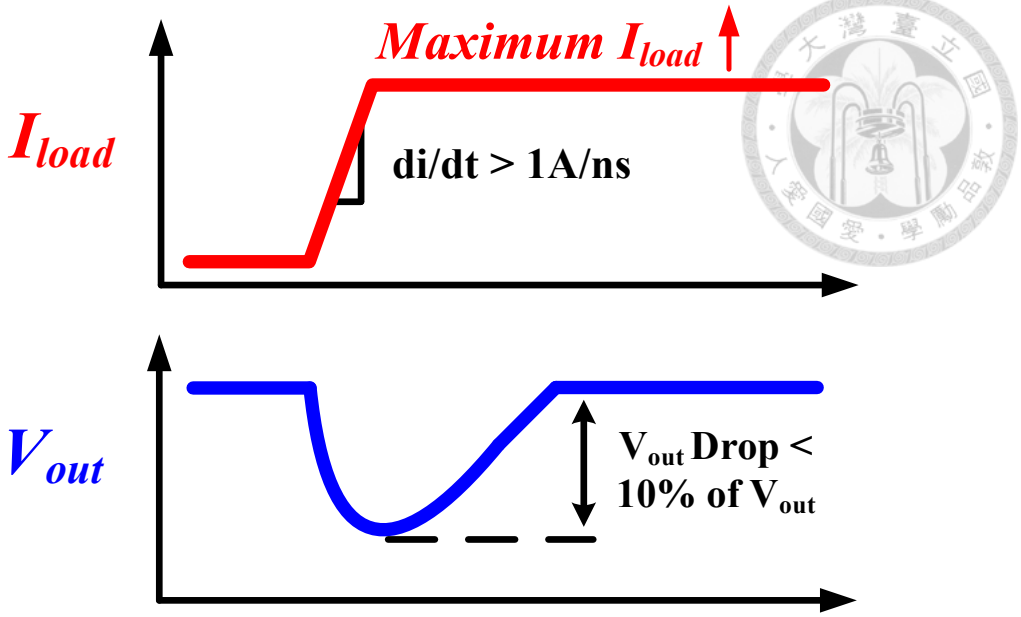

Fig. 1.4 Waveform of output voltage during step-up load transient

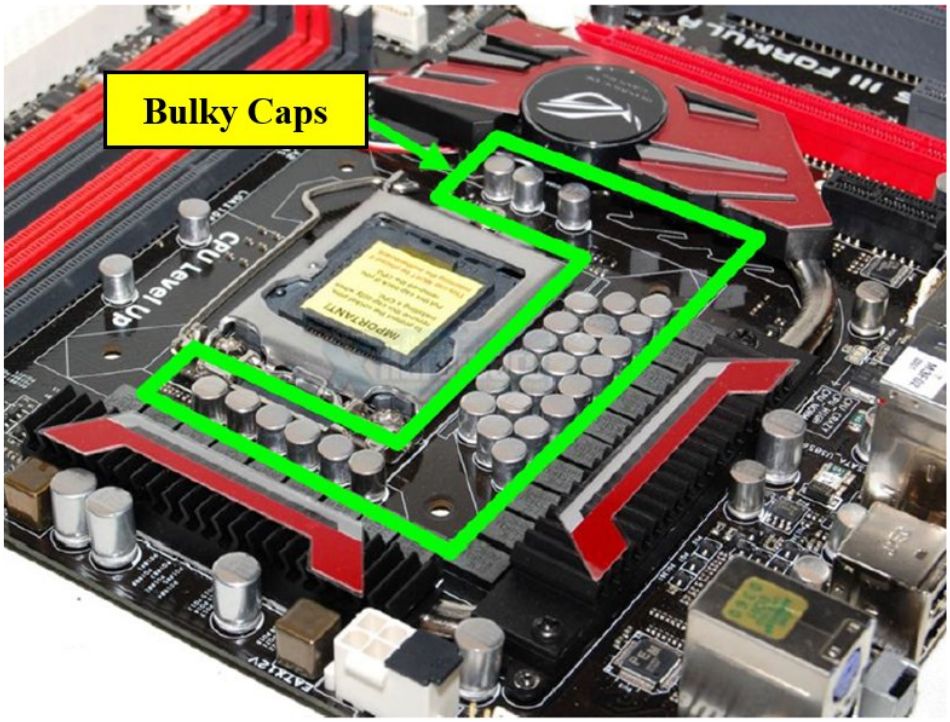

Fig. 1.5 Motherboard of a desktop computer with an Intel i7 microprocessor [3]

However, the bulky capacitors not only occupy the precious motherboard space, but also increase the component cost. Since the trend of electronic devices tends to become lighter and thinner in the future, the space for the CPU VR will be further squeezed. Therefore, constant on-time control is a popular control scheme in voltage regulators for microprocessor because of its fast transient response characteristic.

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Besides handling the ever-increasing current slew rate, improving the light-load efficiency is another critical requirement for the CPU VR. According to the CPU power chart shown in Fig. 1.6 [4], the CPU of a typical notebook computer goes into sleep states very frequently and spends 80% of the time at light load condition. Hence, light-load efficiency of the VR is important for battery life extension. As we know, switching-related loss dominates the total loss at the light load condition. Consequently, constant on-time control has become a suitable choice among many PMIC designs, since this control method naturally reduces converter switching frequency in discontinuous conduction mode. Compared to conventional constant frequency control, the COT control scheme possesses better conversion efficiency under the light-load operation. Moreover, it can switch between continuous conduction mode (CCM) and discontinuous conduction mode (DCM) automatically and smoothly.

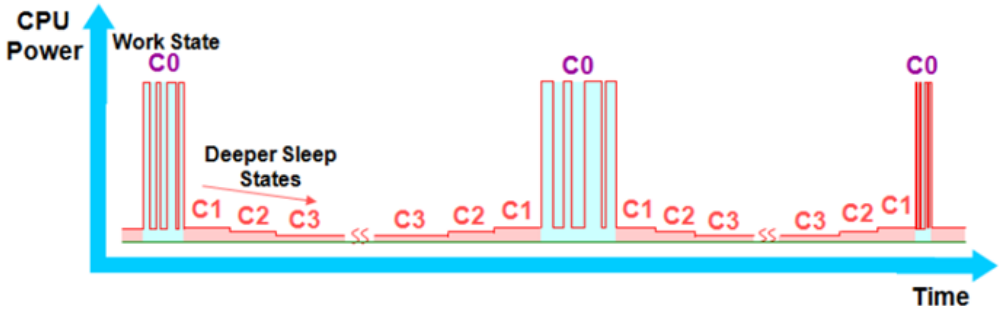

Fig. 1.6 CPU power chart [4]

1.2 Thesis Motivation

The aforementioned characteristics make COT control scheme attractive, especially for computer and portable electronic devices. With the increasing focus on reliability and size consideration of converter design, the ceramic capacitors with low ESR become more and more popular in many applications. Nonetheless, the buck converter with RBCOT control scheme is intrinsically unstable if the ESR of output capacitor is not large enough, which needs ramp compensation technique to enhance loop stability.

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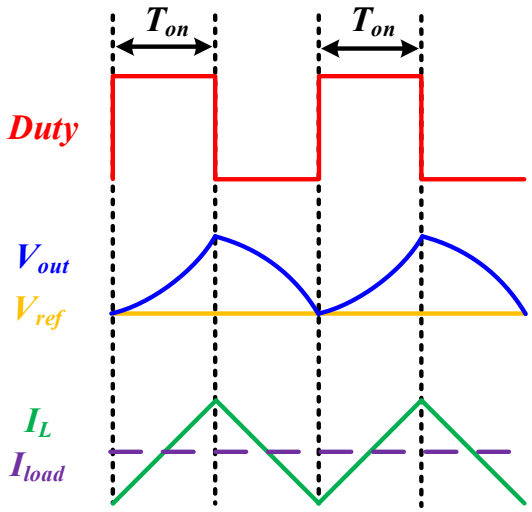
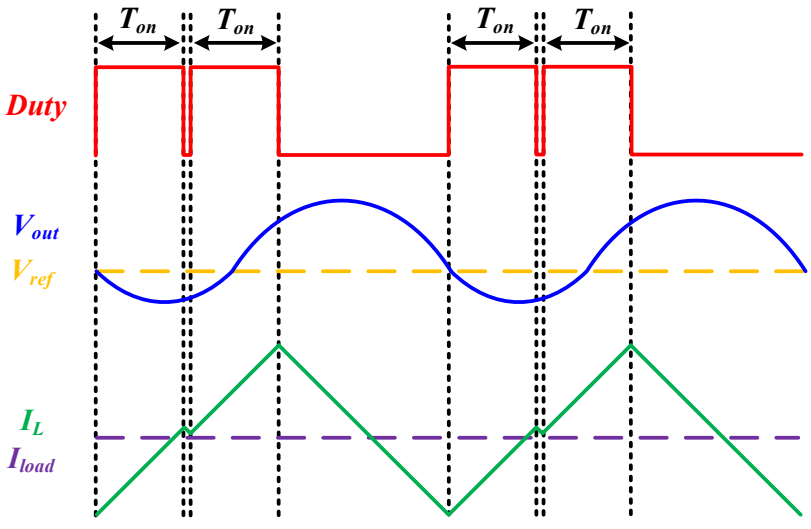
Fig. 1.7(a) and (b) show the steady-state waveforms of a RBCOT controlled buck converter under the condition of the output capacitor with large and low ESR, respectively [5]. It is known that the output voltage is made up of an equivalent series resistor (ESR) ripple voltage and capacitor ripple voltage. The ESR ripple is a reflection of inductor current ripple; besides, there is no time delay effect between ESR ripple voltage and inductor current waveforms. However, the time delay coming from the capacitor ripple voltage degrades loop stability and introduces subharmonic oscillation.



(a)



(b)

Fig. 1.7 Waveforms of the RBCOT controlled buck converter [5]:

(a) Using large ESR output capacitor, and (b) Using low ESR output capacitor

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As shown in Fig. 1.7(a), when the voltage across the ESR is large enough to dominate the output voltage, the RBCOT controlled buck converter operates normally. Nevertheless, when the capacitor ripple voltage dominates the output voltage, as shown in Fig. 1.7(b), the subharmonic oscillation occurs.

In order to alleviate the stability problem, different ramp compensation techniques have been developed in [6]-[9]. However, the injected ramp also brings about some potential problems, such as subharmonic oscillation in DCM operation and excessive load transient response under large duty cycle working condition. In this thesis, a RBCOT controlled buck converter with novel charge-pump ramp compensation is proposed to overcome the aforementioned challenges. Without any current sensing or direct voltage detecting of inductor, this control scheme generates compensation ramp according to input and output voltage by a simple charge-pump circuit. Consequently, compared with previous ramp compensation techniques [6]-[9], the proposed method reduces the complexity of circuit implementation to keep the circuit architecture simple, which is the main feature of RBCOT control.

1.3 Thesis Outline

In this thesis, a novel charge-pump constant on-time (CPCOT) controlled buck converter with dynamic-biased on-time generator was presented and implemented into a monolithic IC using 0.18um CMOS process. The proposed control method solves the subharmonic instability issue caused by the low ESR ceramic output capacitors while retaining the natural advantages of conventional RBCOT control scheme. This thesis consists of six chapters and the detailed outline is elaborated as follows.

Chapter 1 briefly introduces three main control schemes for DC-DC converter and reveals the popularity of the constant on-time control method nowadays. However, a COT controlled buck converter may encounter the subharmonic oscillation, especially

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while using low ESR ceramic output capacitors. The primary objective of this work is to propose a new ramp compensation technique to guarantee the system stability of a COT controlled buck converter.

Chapter 2 gives a literature survey about previous research works of RBCOT controlled buck converter with various types of ramp compensation. Then, a comparison table for different ramp compensation approaches is presented, including the simplified circuit diagrams and limitations of each method.

Chapter 3 illustrates the concept of the proposed CPCOT controlled buck converter. The dynamic-biased technique for the on-time generator to reduce quiescent current of the controller is also explained. In addition, the small-signal model of CPCOT controlled buck converter are derived based on the describing function method, including the reference-to-output transfer function and output impedance. After that, the stability criterion and design guideline of the charge-pump compensation ramp are provided to achieve stable operation and good dynamic performance.

Chapter 4 presents the circuit implementation of the proposed CPCOT control scheme. Three main sub-block circuits, inclusive of modulation comparator, dynamic-biased on-time generator and charge-pump ramp compensation network, are demonstrated in detail.

Chapter 5 shows the experimental results of a buck converter with the proposed CPCOT control integrated circuit fabricated in a 0.18um CMOS process. The steady-state and load transient response waveforms are provided to verify the proposed concepts. The chip micrograph, layout of printed circuit board (PCB) and the experimental platform are shown as well.

Chapter 6 provides conclusions of the work with the summary of actions taken and the directions for future work.

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Chapter 2 Review of Previous Ramp Compensation Methods for RBCOT Controlled Buck Converter

As shown in previous chapter, a buck converter with RBCOT control scheme may suffer from subharmonic oscillation, in particular, while low ESR ceramic capacitors are used as converter's output capacitors. To solve the instability problem, many ramp compensation techniques have been proposed and the small-signal models are also derived based on the describing function method [6]-[9]. This chapter gives a brief literature survey about previous research works on RBCOT control scheme with different types of ramp injection. The concept and the limitation of each ramp compensation approach will be discussed.

2.1 Stability Analysis of RBCOT Controlled Buck Converter

Accurate model of RBCOT control is important because subharmonic oscillation occurs while using low ESR ceramic capacitors. The instability is due to the lagging phase of the capacitor voltage ripple relative to the inductor current ripple. Therefore, the RBCOT control is modeled based on a describing function by Dr. Jian Li [4] such that the stability criteria can be identified. To capture the nonlinearity of the circuit, the power stage as well as the inner voltage feedback is considered as a single entity. By doing this, the influence from capacitor voltage ripple is considered and included in the modeling result. The modeling concept is shown as Fig. 2.1. A small-signal sinusoidal perturbation is injected into the reference signal, and the time domain output voltage variation is calculated. After the time domain relation between reference signal perturbation and output voltage variation is obtained, the result can be transferred into

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frequency domain using Fourier analysis.

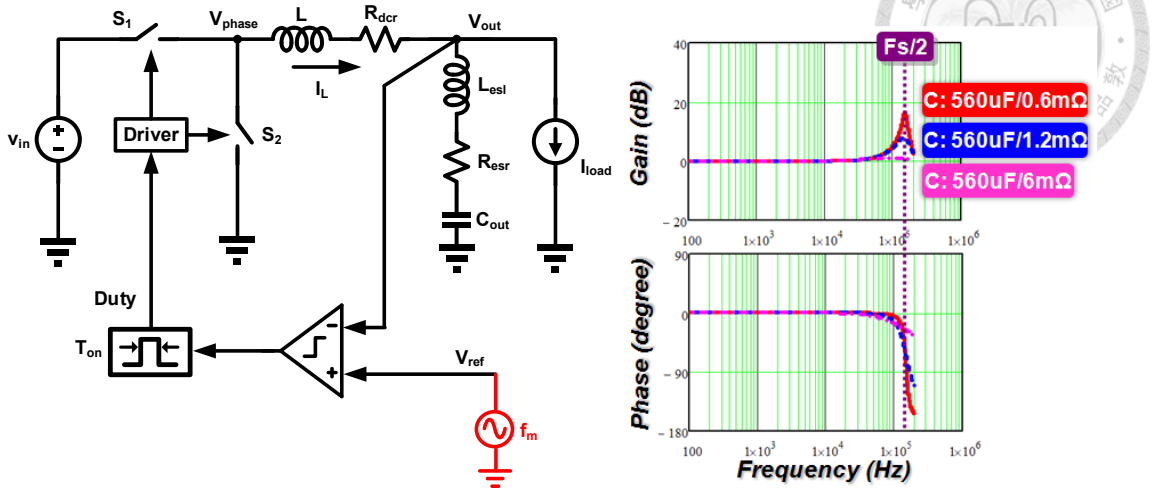

Fig. 2.1 Modeling concept and result for RBCOT controlled buck converter based on describing function method [4]

Based on Padé approximation, the transfer function from reference voltage to output voltage is simplified to a fourth-order equation, as expressed in (2.1):

$$G_{vr}(s)=\frac{v_{out}(s)}{v_{ref}(s)}\approx\frac{1+R_{esr}C_{out}s}{\left(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}\right)\left(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}\right)} \tag{2.1}$$

Where,

$$\omega_1=\frac{\pi}{T_{on}},\ Q_1=\frac{2}{\pi},\ \omega_2=\frac{\pi}{T_{sw}},\ Q_2=\frac{T_{sw}}{\pi\left(R_{esr}C_{out}-\frac{T_{on}}{2}\right)}$$

According to (2.1) and Fig. 2.1,the quality factor Q_2 increases as R_{esr} decreases, which causes the peaking effect at half of switching frequency [4]. Hence, the stability criterion is derived based on maintaining a positive Q_2, in other word, to make sure the complex poles at half of switching frequency must be in the left-half plane. Therefore, the critical condition for stability is obtained, as shown in (2.2):

$$R_{esr}C_{out}>\frac{T_{on}}{2} \tag{2.2}$$

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2.2 Previous Ramp Compensation Techniques to Eliminate Subharmonic Oscillation

To deal with the subharmonic oscillation issue, ramp compensation approaches are known as effective solutions to improve the stability for constant on-time control. Throughout these years, various ramp compensation schemes have been proposed in academia and industry, including adding fixed external ramp [6], adding inductor current ramp [7], adding virtual inductor ramp [8], and adding capacitor current ramp [9]. Detailed analysis of these four approaches will be presented in this section.

It is known that the ESR ripple, which carries real-time inductor current ripple information, should dominate the output voltage for stable operation of RBCOT controlled buck converter. Therefore, the basic concept of different ramp compensation techniques is to enhance the ESR ripple component for stability, as shown in Fig. 2.2. And the stability criterion turns into (2.3), where R_{comp} is the equivalent ramp compensation resistance.

$$\left(R_{esr}+R_{comp}\right)C_{out}>\frac{T_{on}}{2} \tag{2.3}$$

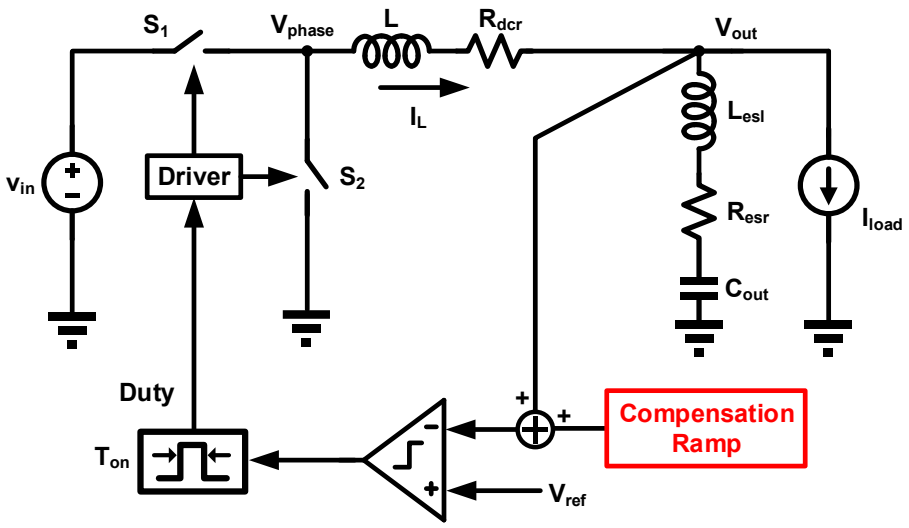

Fig. 2.2 RBCOT controlled buck converter with ramp compensation

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2.2.1 RBCOT Control with Fixed External Ramp Compensation

As we know, the external ramp is used to avoid subharmonic oscillation in the peak current mode control [4]. A similar concept can be applied to ripple-based constant on-time control, as shown in Fig. 2.3. The external ramp starts to build up at the end of the on-time period and resets at the beginning of the on-time period in every switching cycle. It can be easily implemented inside controller IC with a current source charging a capacitor and a PWM signal controlled switch. With the help of the external ramp which is in the same phase as the ESR voltage ripple, the delay effect caused by the capacitor voltage ripple is alleviated. Consequently, the RBCOT controlled buck converter with external ramp compensation can operate stably while using low ESR output capacitors.

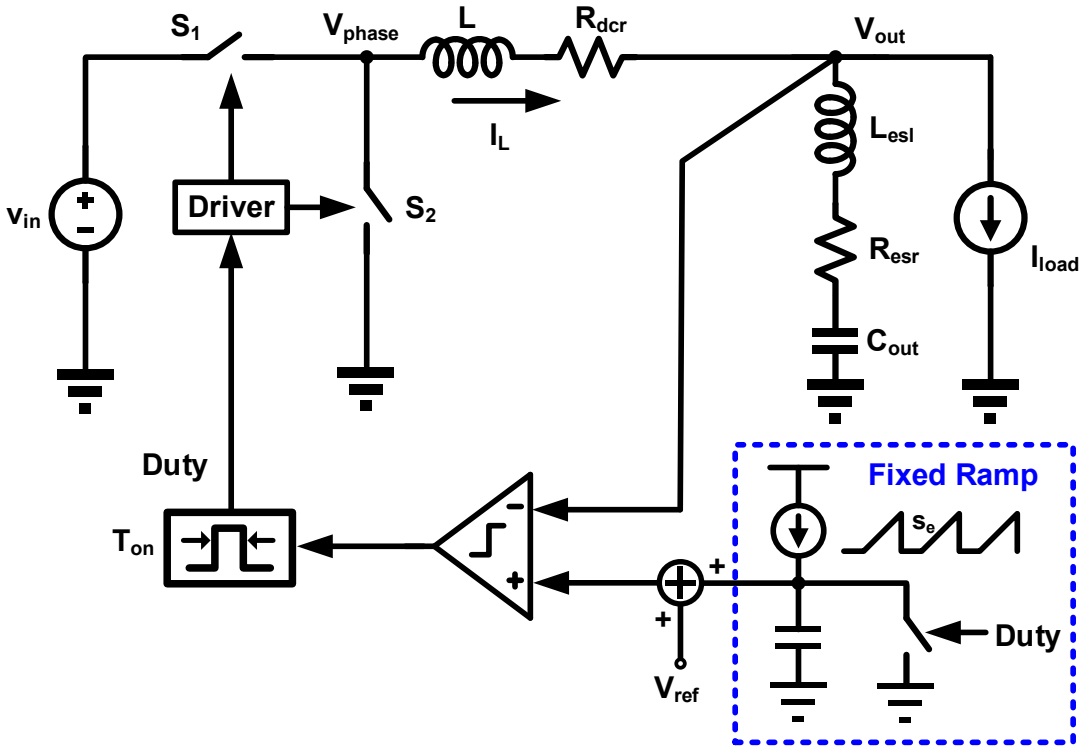

Fig. 2.3 RBCOT controlled buck converter with external ramp compensation

With the external ramp compensation, the small-signal reference-to-output transfer function is derived in [6] based on the time-domain DF method, as shown in (2.4):

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$$G_{vr}(s) \approx \frac{1}{1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}} \cdot \frac{\left(1+\frac{s}{Q_1\omega_2}+\frac{s^2}{\omega_2^2}\right)\left(1+R_{esr}C_{out}s\right)}{\left(1+\frac{s}{Q_1\omega_2}+\frac{s^2}{\omega_2^2}\right)\left(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}\right)+\frac{S_e}{S_f}R_{esr}C_{out}T_{sw}s^2} \quad (2.4)$$

Where,

$$\omega_1 = \frac{\pi}{T_{on}}, Q_1 = \frac{2}{\pi}, \omega_2 = \frac{\pi}{T_{sw}}, Q_2 = \frac{T_{sw}}{\pi\left(R_{esr}C_{out} - \frac{T_{on}}{2}\right)}, s_f = R_{esr}\frac{V_{out}}{L},$$

s_e = slope of the external ramp during t_{off}

Since the transfer function (2.4) is in a nonfactorized complicated form, the poles become very difficult to identify and the relations between the locations of the poles, the quality factors, and the circuit parameters are not clear. According to [6], the transfer function shown in (2.4) can be factorized as (2.5), where $\omega_{p1}, \omega_{p2}, Q_{p1}, Q_{p2}$ depend on the slope of external ramp.

$$G_{vr}(s) \approx \frac{1}{1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}} \cdot \frac{\left(1+\frac{s}{Q_1\omega_2}+\frac{s^2}{\omega_2^2}\right)\left(1+R_{esr}C_{out}s\right)}{\left(1+\frac{s}{Q_{p1}\omega_{p1}}+\frac{s^2}{\omega_{p1}^2}\right)\left(1+\frac{s}{Q_{p2}\omega_{p2}}+\frac{s^2}{\omega_{p2}^2}\right)} \quad (2.5)$$

Although the subharmonic oscillation issue of RBCOT controlled buck converter can be solved by adding an external ramp, the design of the fixed external ramp is critical as it affects the positon and damping of double poles, ω_{p1} and ω_{p2}.When the external ramp is too small, both pairs of double poles are located at half of switching frequency. Hence, the Q factor is very large which reveals that the stability margin becomes worse. When the external ramp is too large, the two pairs of double poles are separated and the peaking of gain curve is reduced. However, the low frequency double pole will cause a phase drop in the lower frequency range and the peaking of the two pairs of double poles will become larger as the external ramp increases. Therefore, either too small or too large external ramp is detrimental to the load transient

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performance. In addition, for large duty cycle operations, the *Q* factor would increase and the double pole move toward low frequency and degrade the phase margin significantly [6]. Thus, a potential low-frequency high peaking of the output impedance may lead to an oscillatory transient response.

2.2.2 RBCOT Control with Inductor Current Ramp Compensation

The use of an additional current feedback path is another practical ramp compensation approach for the RBCOT controlled buck converter with low ESR output capacitors. This method is compensating the direct feedback loop by adding the inductor current ramp to the output voltage signal, as shown in Fig. 2.4. The sensed inductor current signal, which is in phase with the ESR ripple, reduces the influence of the capacitor ripple to ensure the stability.

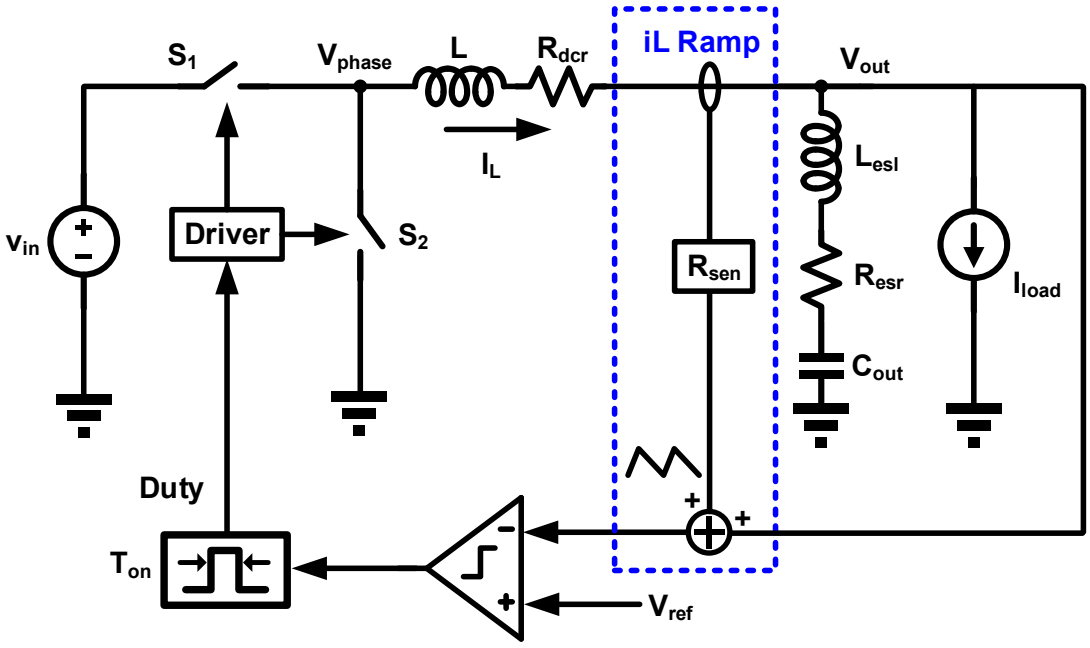

Fig. 2.4 RBCOT controlled buck converter with inductor current ramp compensation

Following the same modeling methodology, the reference-to-output transfer function after introducing the inductor current ramp compensation can be derived as (2.6):

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$$G_{vr}(s) \approx \frac{1 + R_{esr} C_{out} s}{\left(1 + \frac{s}{Q_1 \omega_1} + \frac{s^2}{\omega_1^2}\right)\left(1 + \frac{s}{Q_2 \omega_2} + \frac{s^2}{\omega_2^2}\right)} \tag{2.6}$$

Where,

$$\omega_1 = \frac{\pi}{T_{on}}, Q_1 = \frac{2}{\pi}, \omega_2 = \frac{\pi}{T_{sw}}, Q_2 = \frac{T_{sw}}{\pi\left[(R_{sen} + R_{esr})C_{out} - \frac{T_{on}}{2}\right]},$$

R_{sen} = sensing gain of the additional current loop

Therefore, the stability criterion is obtained, as expressed in (2.7):

$$(R_{sen} + R_{esr}) C_{out} > \frac{T_{on}}{2} \tag{2.7}$$

By comparing (2.1) and (2.6), Q_2 shows that the inductor current ramp compensation equivalently increases the ESR of the output capacitors. Without the need for a large ESR, the additional current ramp signal releases the stability constraint. Consequently, based on the stability criterion (2.7), the sensing gain R_{sen} can be used as a design parameter to avoid subharmonic oscillation for various output capacitors.

Although the inductor current ramp compensation method can enhance loop stability and provide a desired damping, it changes the property of the output impedance [7]. The low-frequency output impedance becomes resistive which is equal to the current sensing gain, R_{sen}. Therefore, by adding inductor current information, adaptive voltage positioning (AVP) is observed in time domain due to the dc information of inductor current. In some applications, such as voltage regulators for microprocessors where constant output impedance is required, this control structure can be used to meet the design target. For other applications without such a requirement, output voltage should be regulated and the voltage droop caused by the sensed inductor current is undesired. On top of that, employing the inductor current sensing network makes the control structure more complicated and less attractive.

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2.2.3 RBCOT Control with Virtual Inductor Current Ramp Compensation

To stabilize the RBCOT controlled buck converter with low ESR output capacitors, the virtual inductor current (VIC) ramp compensation technique is proposed [8] and widely utilized in many industry products. The concept of this approach is to improve system stability without sensing current information or adding extra components. Fig. 2.5 shows that this method generates the inductor current ripple waveform by integrating the phase voltage V_{phase} through the $R_{vic}C_{vic}$ integrator and removing its DC value by the dc value extractor. The "virtual" inductor current ramp is then added to the PWM modulator input to enhance the effect of ESR ripple for better stability. Moreover, if the control scheme is implemented in IC with driver embedded, no additional pin is required while using this compensation method because V_{phase} signal is already available in IC.

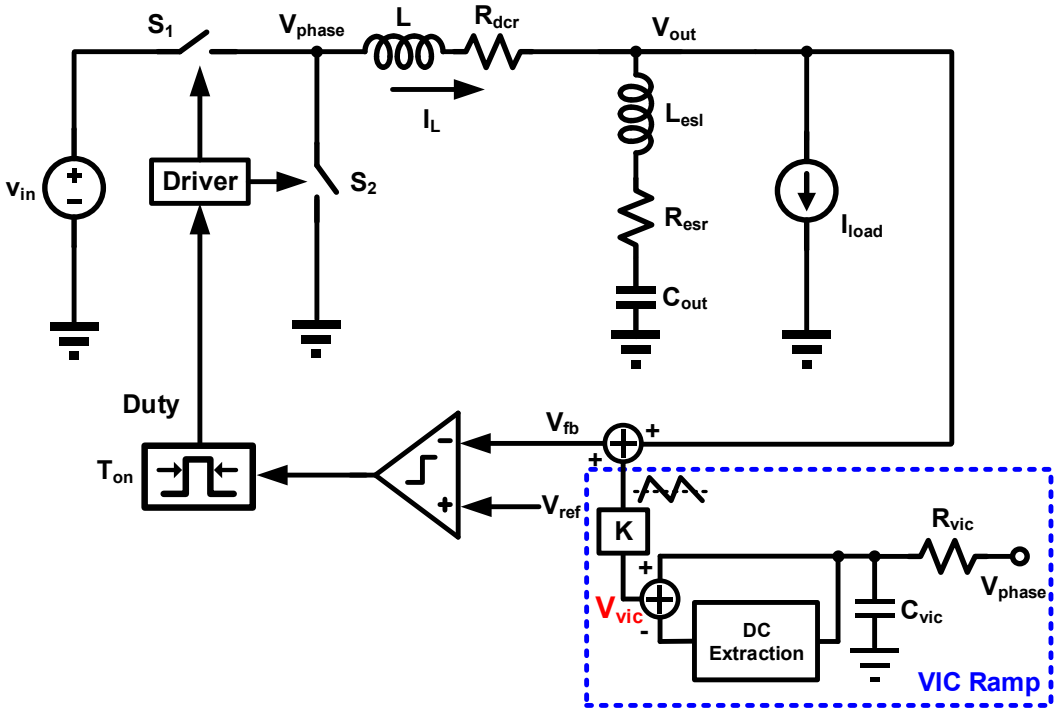

Fig. 2.5 RBCOT controlled buck converter with virtual inductor current ramp compensation

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According to [8] and a series of complicated calculation, the reference-to-output transfer function after adding the virtual inductor current ramp compensation can be obtained as (2.8):

$$G_{vr}(s) \approx \frac{1+R_{esr}C_{out}s}{\left(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}\right)\left(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}\right)} \tag{2.8}$$

Where,

$$\omega_1=\frac{\pi}{T_{on}},\ Q_1=\frac{2}{\pi},\ \omega_2=\frac{\pi}{T_{sw}},\ Q_2=\frac{T_{sw}}{\pi\left[(R_v+R_{esr})C_{out}-\frac{T_{on}}{2}\right]},\ R_v=\frac{LK}{R_{vic}C_{vic}}$$

Hence, the stability criterion is derived, as shown in (2.9):

$$(R_v+R_{esr})C_{out} > \frac{T_{on}}{2} \tag{2.9}$$

As can be seen from (2.9), with proper design of VIC circuit, there is no subharmonic oscillation for the RBCOT controlled buck converter with low ESR output capacitors, even though the output voltage waveform is dominated by capacitor ripple.

This ramp compensation scheme greatly improves the stability in CCM operation, but it is observed that subharmonic oscillation may occur in DCM operation, as shown in Fig. 2.6. This phenomenon is undesirable because the output voltage ripple becomes excessively large and the switching loss increases. To make sure the system stable in DCM operation, the slope of V_{fb} should be less than zero during T_3 period, when both high-side and low-side switches are off. In accordance with [10], the DCM stability criterion of RBCOT controlled buck converter with virtual inductor current ramp compensation is derived as follows:

$$K < \frac{I_{load}R_{vic}C_{vic}}{V_{out}C_{out}} \tag{2.10}$$

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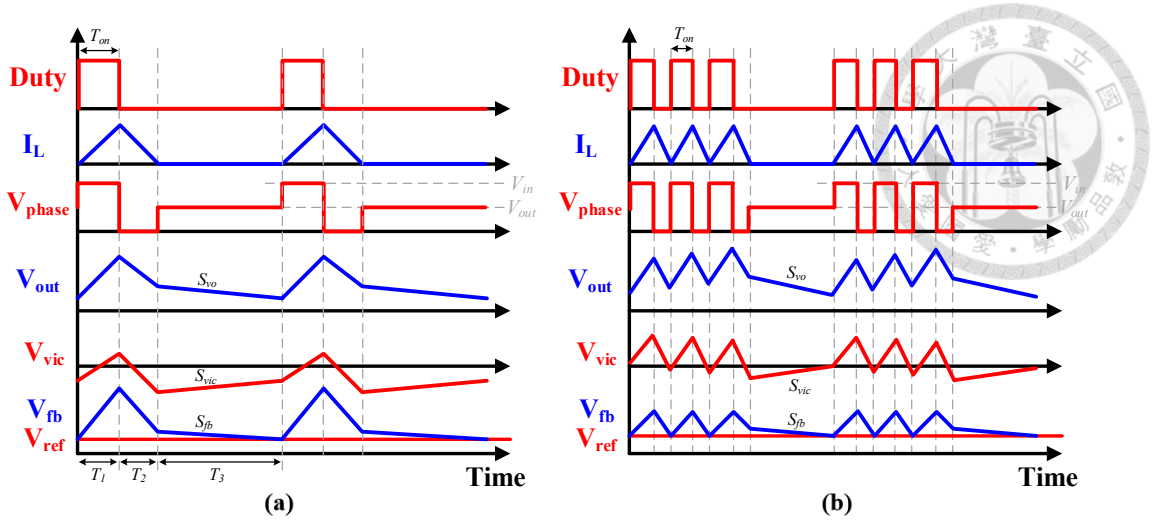

Fig. 2.6 Operation waveforms of RBCOT with VIC control in DCM: (a) stable case, and (b) unstable case

On the basis of (2.9), the larger is the K value, the better is the CCM stability. From (2.10), however, too large K value violates the DCM stability criterion. Therefore, there is a range of K value that guarantees the system stability under both CCM and DCM conditions. Combining the stability criteria (2.9) and (2.10), the overall stability boundary of K value is given in the following equation:

$$\left(\frac{T_{on}}{2}-R_{esr}C_{out}\right)\frac{R_{vic}C_{vic}}{LC_{out}} < K < \frac{I_{load}R_{vic}C_{vic}}{V_{out}C_{out}} \tag{2.11}$$

2.2.4 RBCOT Control with Capacitor Current Ramp Compensation

The fourth method reported in the literature is to enhance the effect ESR ripple by adding capacitor current ramp [9]. The concept of the capacitor current compensated RBCOT control is illustrated in Fig. 2.7, where K_s is the capacitor current signal amplification gain. Since the sensed capacitor current ripple can be sufficiently amplified, not limited by the output voltage ripple specification, the total feedback ripple can be dominated by the virtual ESR ripple. Besides, the aforementioned output

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voltage droop issue while using inductor current ramp compensation is eliminated, because capacitor current does not contain DC value. As a consequence, compared with other ramp compensation techniques, this method not only improves the loop stability but also maintains the property of ultralow output impedance.

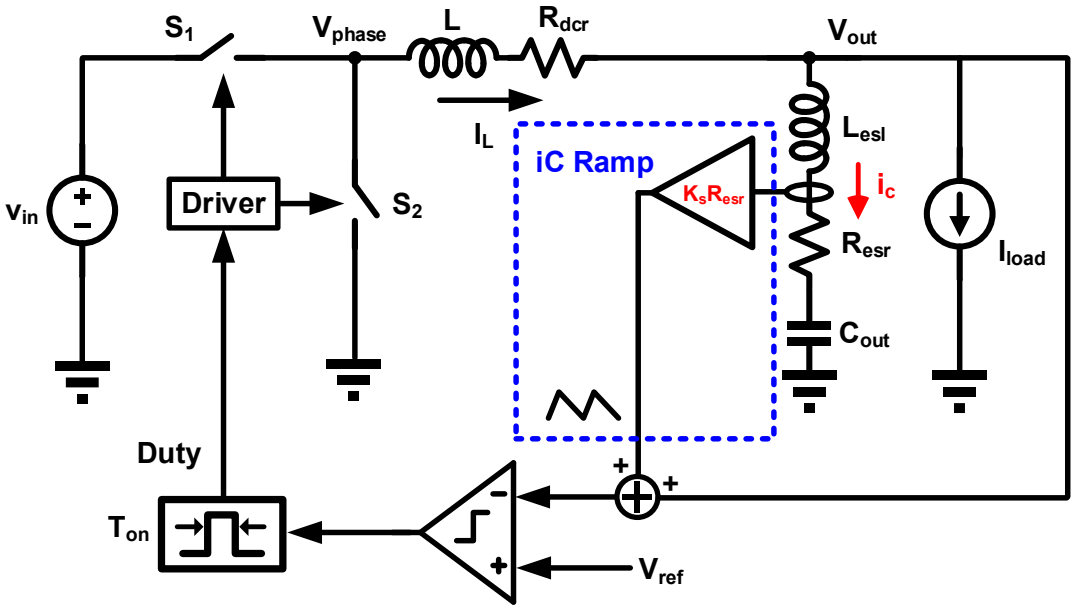

Fig. 2.7 RBCOT controlled buck converter with capacitor current ramp compensation

With the capacitor current ramp compensation, the small-signal reference-to-output transfer function is derived in [9] as follows:

$$G_{vr}(s) \approx \frac{1+R_{esr}C_{out}s}{\left(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}\right)\left(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}\right)} \tag{2.12}$$

Where,

$$\omega_1=\frac{\pi}{T_{on}}, Q_1=\frac{2}{\pi}, \omega_2=\frac{\pi}{T_{sw}}, Q_2=\frac{T_{sw}}{\pi\left[(K_sR_{esr}+R_{esr})C_{out}-\frac{T_{on}}{2}\right]},$$

K_s = capacitor current signal amplification gain

Thus, the stability criterion is obtained, as expressed in (2.13):

$$(K_sR_{esr}+R_{esr})C_{out} > \frac{T_{on}}{2} \tag{2.13}$$

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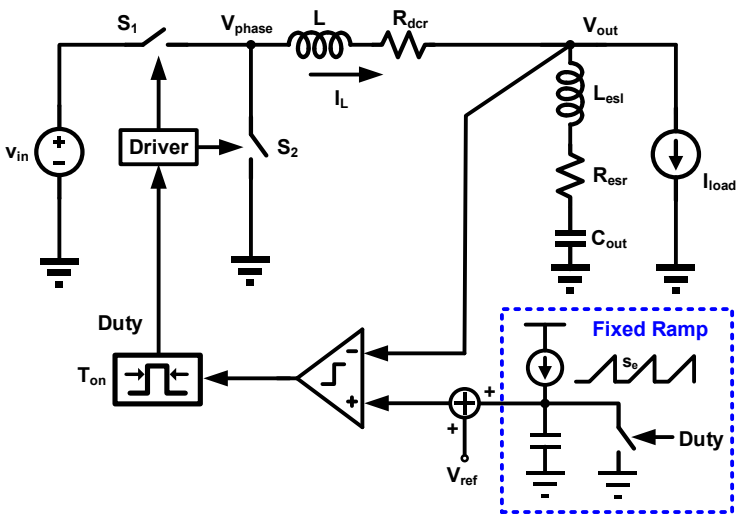
It is seen that if the gain K_s is too large, the overdamped double pole will slow down the transient response; if the gain K_s is too small, the complex double pole will lead to subharmonic oscillation. Even though the gain K_s is properly designed, the distortion of sensed signal, caused by the time constant mismatch between capacitor current sensing network and the output capacitor, can bring about an oscillatory transient response [11].

For practical application, the influence on accuracy of sensed current due to the parasitic parameters (such as ESL effect of the capacitor, ESL due to the trace) needs to be taken into consideration. This is one reason why this method is not as popular as inductor current ramp compensation in commercial products nowadays.

2.3 Summary

This chapter reviews the previous research works on RBCOT control scheme with various types of ramp compensation. Table 2.1 summarizes the comparison between each method.

Table 2.1 Comparison between RBCOT controlled buck converter with different ramp compensation methods

Ramp Compensation Type	Circuit Diagram and Limitation
Fixed External Ramp	 **Limitation: Cannot achieve proper damping at large duty cycle**

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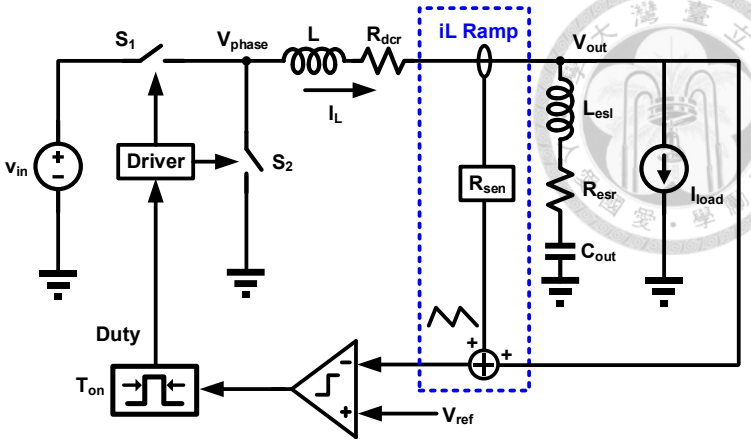
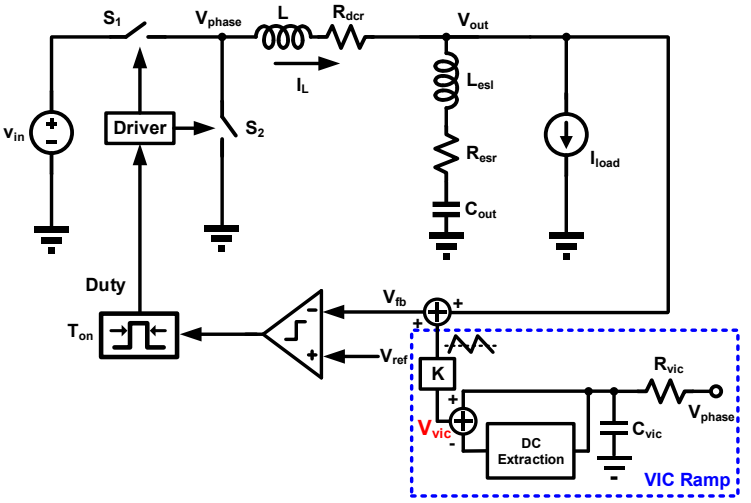
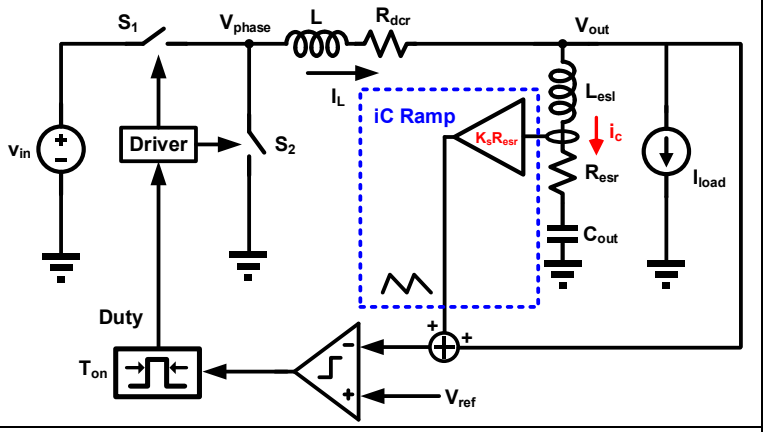
Inductor Current Ramp	 **Limitation: An undesirable output voltage droop due to resistive output impedance at low frequency**
Virtual Inductor Current Ramp	 **Limitation: May be unstable in DCM operation**
Capacitor Current Ramp	 **Limitation: Distortion of sensed signal caused by time constant mismatch between capacitor current sensing network and the output capacitor**

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Chapter 3 Proposed Charge-Pump Constant On-Time (CPCOT) Controlled Buck Converter with Dynamic-Biased On-Time Generator

As mentioned in chapter 2, ripple-based constant on-time (RBCOT) control with different kinds of ramp compensation has been widely adopted in buck converter to solve the instability and noise-margin issues caused by the low ESR output capacitors. However, the injected compensation ramp also brings about some potential problems, such as undesirable output voltage droop, deterioration in load transient performance at large duty cycle and subharmonic oscillation in DCM operation. In this chapter, a RBCOT controlled buck converter with charge-pump ramp compensation is proposed to overcome the aforementioned challenges while retaining the natural advantages of RBCOT control scheme. The circuit configuration will be demonstrated first, and time-domain operating principle will be explained. In addition, the concept of dynamic-biased on-time generator, which is proposed to reduce quiescent current of the controller, will be illustrated. Finally, the small-signal model of the proposed CPCOT controlled buck converter operated in continuous conduction mode (CCM) will be derived based on the describing function (DF) methodology and verified by SIMPLIS simulation.

3.1 Description of Proposed CPCOT Control Scheme

Fig. 3.1 demonstrates the circuit diagram of proposed CPCOT control scheme for a buck converter. Without any current sensing or direct voltage detecting of inductor, this scheme generates compensation ramp according to input voltage V_{in} and output voltage V_{out} by a simple charge-pump circuit. The charge-pump circuit, formed by a pair of voltage controlled current sources with transconductance G_{mH}, G_{mL} and switches,

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charges and discharges the capacitor C_{cp} linearly. Thus, the charge-pump compensation ramp, which enhances the effect of ESR ripple for better stability, can be easily generated. In addition, this ramp signal is coupled to reference voltage V_{ref} through a coupling capacitor C_{ac} instead of adding ramp on the output voltage. Therefore, compared to other ramp compensation methods proposed by the previous literature, there is no need for wide-bandwidth adder in this control scheme at high switching frequency operation.

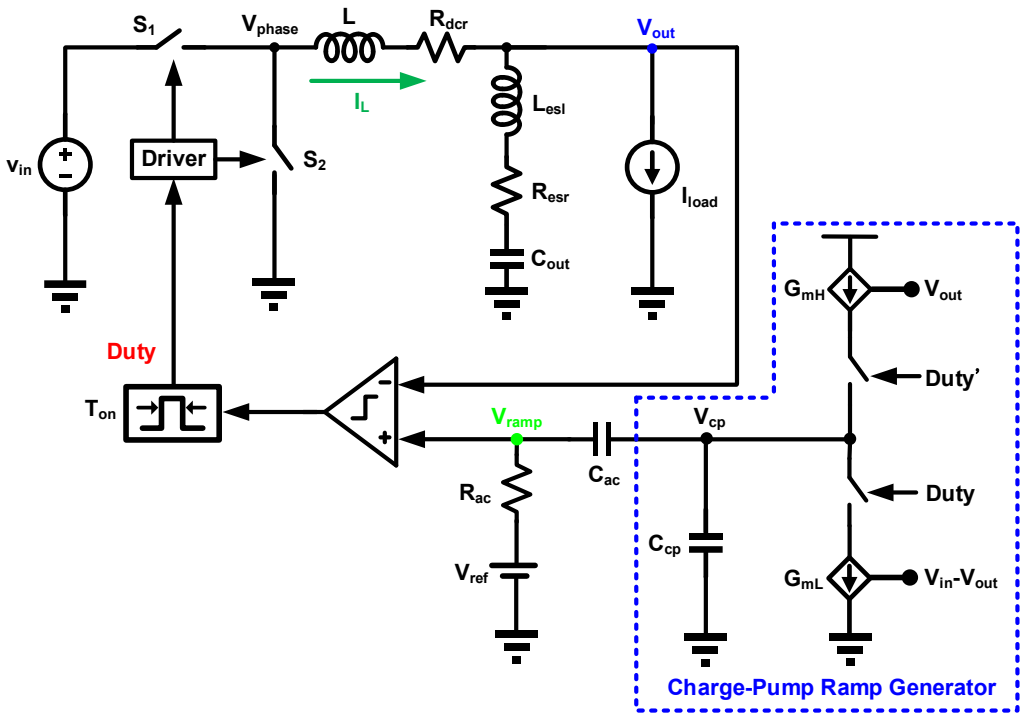


Fig. 3.1 Circuit diagram of proposed CPCOT control scheme for a buck converter

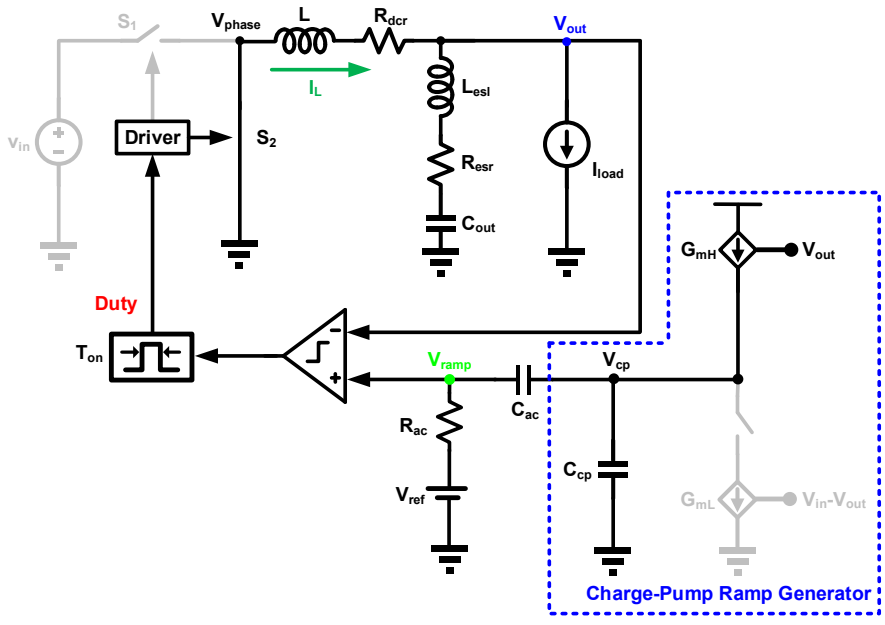
For the steady-state operation, the duty cycle signal *Duty* and the inverted duty cycle signal *Duty'* control the high/low-side power switches and high/low-side current sources of the charge-pump ramp generator. Therefore, when the high-side power switch S_1 of the buck converter turns off, as shown in Fig. 3.2(a), the high-side current source of the ramp generator starts to charge the capacitor C_{cp} until the comparator detects the output voltage V_{out} lower that the ramp voltage V_{ramp}, which triggers the on-time generator and then turns on the high-side power switch S_1 again. On the other hand,

doi:10.6342/NTU202000925

when the high-side switch S_1 of the buck converter turns on, as shown in Fig. 3.2(b), the low-side current source of the ramp generator will discharge the capacitor C_{cp} for a period equaled to on-time T_{on}. As a result, unlike the external ramp or VIC methods, this control scheme generates a ramp signal automatically and naturally completes the summation procedure through a coupling capacitor C_{ac}. In other words, the control scheme generates inverse ramp and add to reference voltage V_{ref} automatically rather than uses an adder to inverse the ramp and to add reference voltage and ramp voltage. The detailed modulation waveforms are demonstrated in Fig. 3.3. From Fig. 3.1 and Fig. 3.3, the rising slope S_{en} and falling slope S_{ef} of the ramp voltage V_{ramp} can be derived as (3.1) and (3.2), respectively. It is derived based on the assumption $\frac{1}{2\pi R_{ac}C_{ac}} \ll f_{sw}$, which insures that the charge-pump compensation ramp is well coupled to reference voltage without distortion.

$$S_{en} = \frac{G_{mH}V_{out}}{C_{cp}} \tag{3.1}$$

$$S_{ef} = \frac{G_{mL}\left(V_{in} - V_{out}\right)}{C_{cp}} \tag{3.2}$$



(a)

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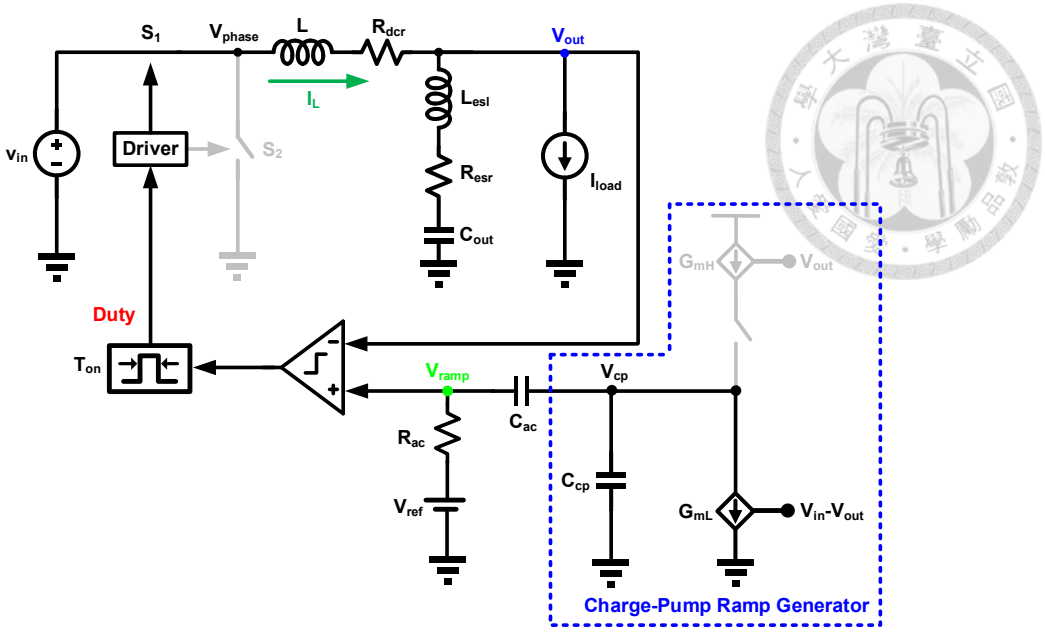

(b)

Fig. 3.2 Operation of charge-pump ramp generator at:

(a) duty cycle off interval, and (b) duty cycle on interval

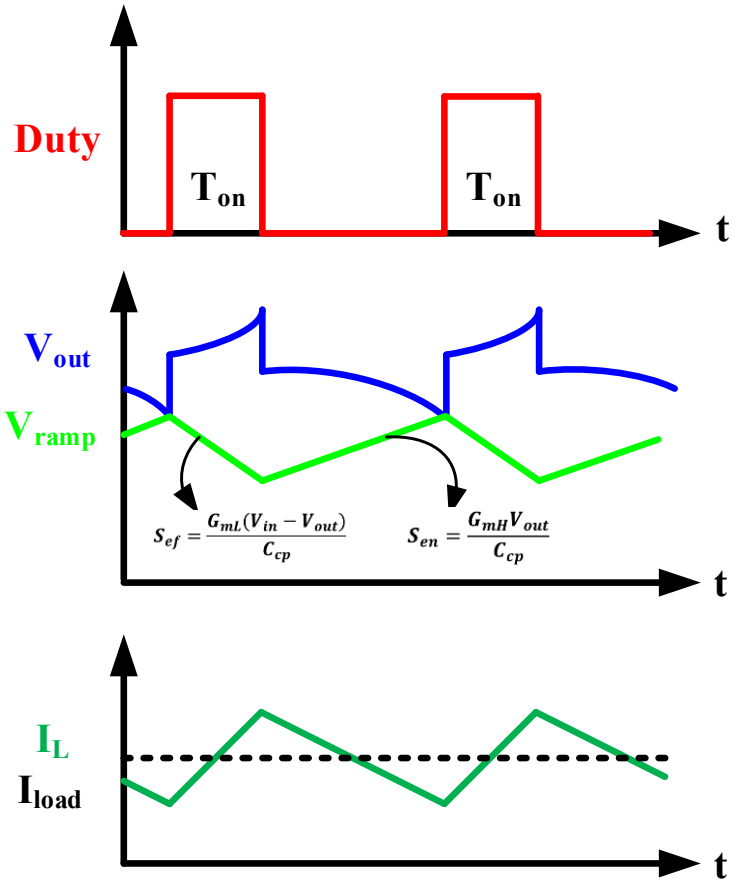

Fig. 3.3 Modulation waveforms of proposed CPCOT controlled buck converter

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3.2 Dynamic-Biased Technique for On-Time Generator

In high switching frequency design, the comparator inside the conventional on-time generator consumes large current to minimize the delay time. Hence, it dominates the quiescent power consumption of the controller. To solve this issue, the dynamic-biased technique is developed to bias the comparator efficiently. Fig. 3.4 shows the concept and waveform of proposed dynamic-biased technique in comparison with traditional constant-biased method. With applying on-time ramp signal to the bias circuit, the bias current of comparator inside on-time generator can be modulated dynamically. Details about the circuit implementation will be introduced in Section 4.2.

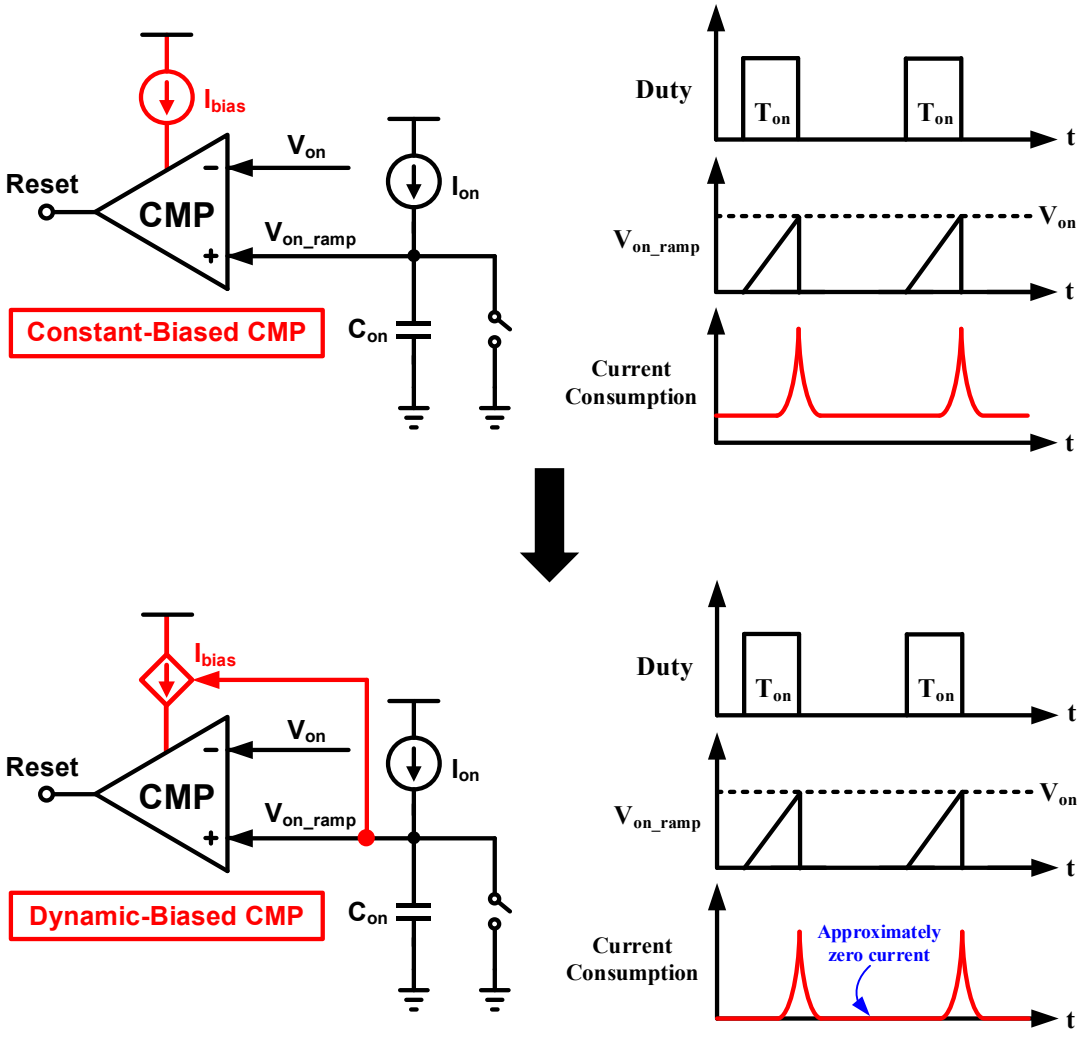

Fig. 3.4 Concept of proposed dynamic-biased comparator for on-time generator

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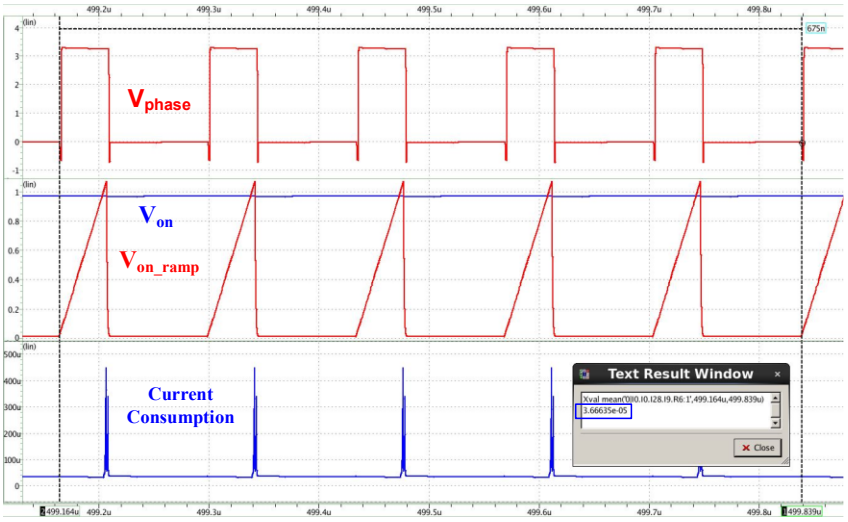
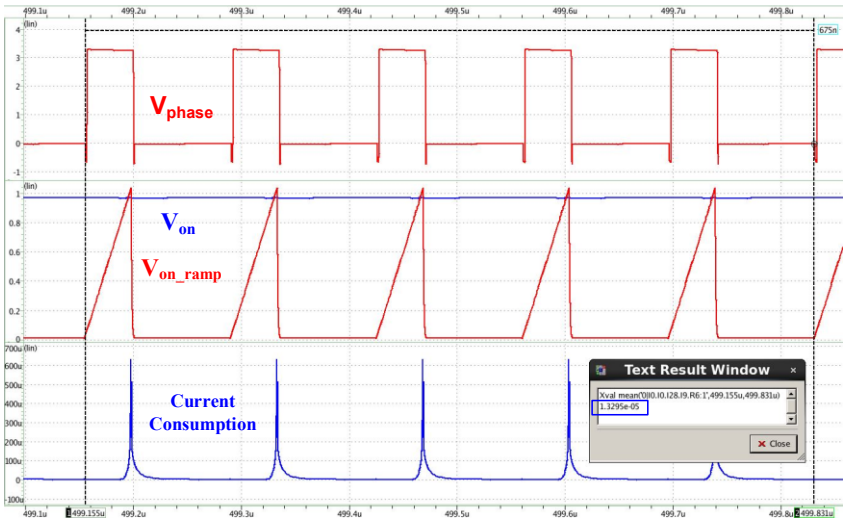
Fig. 3.5 shows the simulation results of average current consumption of on-time comparator in a period of operation with and without dynamic-biased technique. According to the simulation results, the average current consumption of on-time comparator is reduced by 64% compared with the traditional constant-biased method in CCM. In addition, since switching frequency is proportional to load current in DCM due to characteristic of constant on-time control, dynamic-biased method can further reduce power consumption of controller in DCM to improve light-load efficiency.



(a)



(b)

Fig. 3.5 Simulation results of the average current consumption of on-time comparator in CCM (V_{in}=3.3 V, V_{out}=1.0 V) with: (a) constant-biased method [36.66 µA], and (b) dynamic-biased method [13.30 µA]

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3.3 Small-Signal Model Derivation

To thoroughly understand the characteristics of the proposed CPCOT control scheme, the small-signal model will be derived in this section. Since the conventional low-frequency average model ignores ripple information in modulator input, it is accurate at frequencies much lower than the switching frequency. In this section, the describing function (DF) method [4] is used to model the nonlinear constant on-time modulator for the proposed CPCOT control scheme to obtain transfer functions of reference-to-output and output impedance. This method considers all the nonlinearities due to inductor current feedback and capacitor voltage feedback and is accurate up to half of the switching frequency. The reference-to-output transfer function $G_{vr}(s)$ can be used to judge the locations of the poles so that the system stability can be investigated. On the other hand, the output impedance $Z_o(s)$ can be used to predict the load transient response. Based on the derived transfer functions, the optimal design guidelines for the charge-pump compensation ramp is provided from the stability margin and transient performance points of view.

3.3.1 Reference-to-Output Transfer Function $v_{out}(s)/v_{ref}(s)$

To model the proposed CPCOT controlled buck converter much more accurately, describing function (DF) method is adopted since this approach preserved ripple-frequency components during derivation. The accuracy of DF modeling methodology is up to half of switching frequency. In CPCOT control, as shown in Fig. 3.6, the non-linear constant on-time modulator consists of switches, the inductor current, the modulation comparator and the on-time generator. Following the DF modeling methodology, all of them are treated as a single entity to model instead of breaking them into parts. According to the DF method, a sinusoidal perturbation with a small magnitude at frequency f_m is injected through the reference voltage v_{ref} firstly. Then, the

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perturbed duty cycle expression in the time domain can be found out based on the waveform. Next, Fourier analysis is applied to calculate the perturbation frequency component of the duty cycle and the inductor current. At last, the describing function from the reference voltage to the inductor current can be obtained. Fig. 3.7 shows the modulation waveforms with perturbation. To simplify the complexity of derivation, the following assumptions were assumed:

(i) Inductor current slopes during on-time and off-time remain constant.

(ii) Comparing to reference voltage, the magnitude of perturbation is much smaller.

(iii) The perturbation frequency f_m and the switching frequency f_{sw} are commensurable, which means that $N \cdot f_{sw} = M \cdot f_m$, where N and M are positive integers.

(iv) The design of time constant $R_{ac}C_{ac}$ insures the correctness of (3.1) and (3.2), which means that the ramp voltage V_{ramp} is a perfect triangular ramp without distortion.

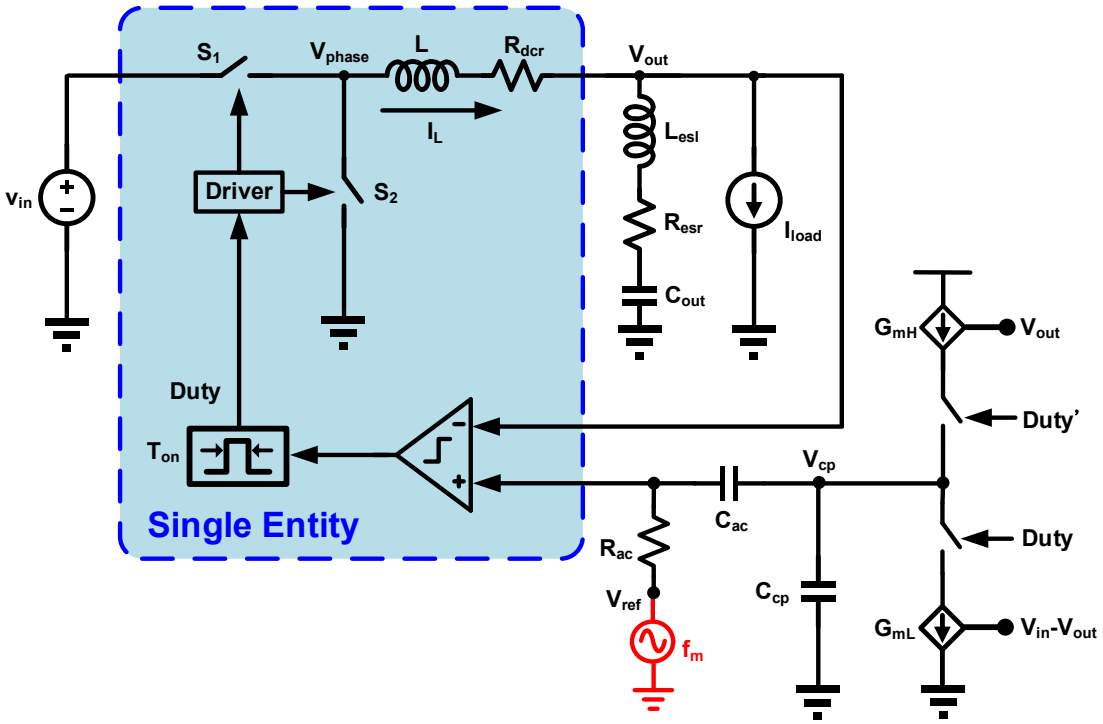

Fig. 3.6 Model methodology for reference-to-output transfer function of proposed CPCOT controlled buck converter

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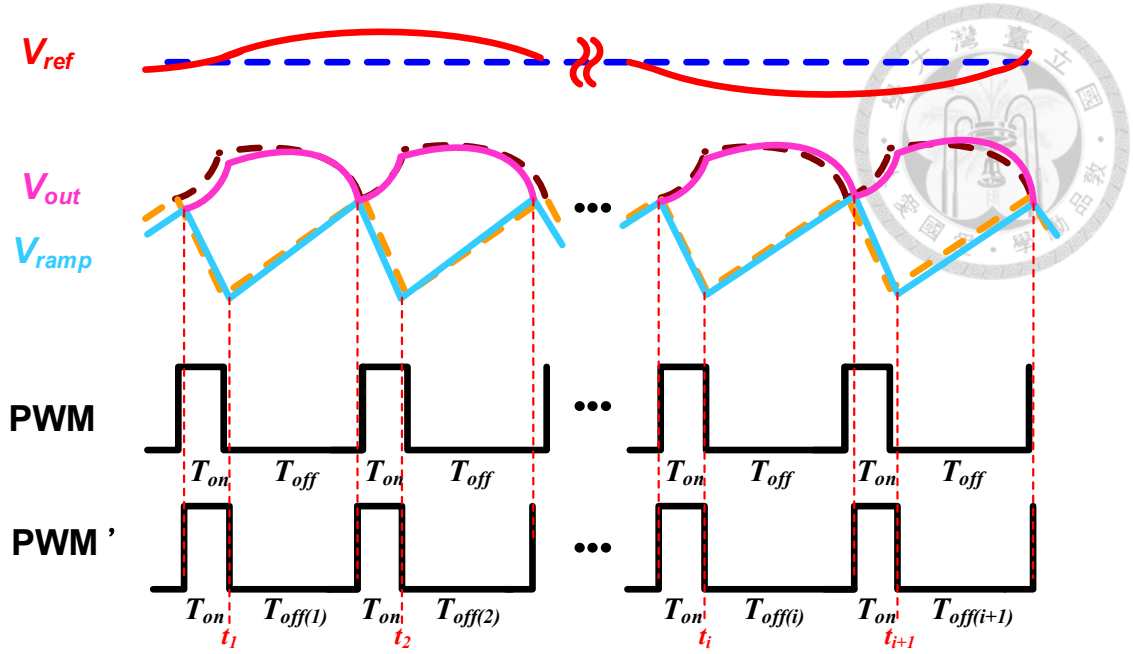

Fig. 3.7 Perturbed modulation waveforms in the proposed CPCOT control

Step 1: Off-time calculation from time waveforms

When a perturbation v_{ref} is applied for modeling, the modulation waveforms under CCM operation are shown in Fig. 3.7. Because the on-time is fixed, the off-time is modulated by the perturbed signal v_{ref}, as expressed in (3.3), where $\hat{r}$ represents the magnitude of the perturbed signal.

$$v_{ref}(t) = r_o + \hat{r}\sin(2\pi f_m t), \hat{r} << r_o \tag{3.3}$$

Based on the modulation law, it is found that:

$$V_{ramp}(t_{i-1} + T_{off(i-1)}) + S_n T_{on} - S_f T_{off(i)} + \int_{t_{i-1}+T_{off(i-1)}}^{t_i+T_{off(i)}} \frac{[i_L(t) - I_{load}]}{C_{out}} \cdot dt = V_{ramp}(t_i + T_{off(i)}) \tag{3.4}$$

where $T_{off(i)}$ is the off-time of the i_{th} cycle, $S_n = \frac{R_{esr}(V_{in}-V_{out})}{L}$, and $S_f = \frac{R_{esr}V_{out}}{L}$. Assuming $T_{off(i)} = T_{off} + \Delta T_{off(i)}$, where T_{off} is the stead-state off time and $\Delta T_{off(i)}$ is the i_{th} cycle off-time perturbation, then the off-time can be obtained from equation (3.3) and (3.4).

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Step 2: Fourier analysis of inductor current

The perturbed duty cycle can be expressed by the unit step function as (3.5); whereas the perturbed inductor current can be expressed based on the perturbed duty cycle as (3.6):

$$d(t)\Big|_{0\le t\le t_M+T_{off(M)}+T_{on}} = \sum_{i=1}^{M}\left[u\left(t-t_i-T_{off(i)}\right)-u\left(t-t_i-T_{off(i)}-T_{on}\right)\right] \tag{3.5}$$

$$i_L(t)\Big|_{0\le t\le t_M+T_{off(M)}+T_{on}} = \int_0^t\left[\frac{V_{in}}{L}d(t)\Big|_{0\le t\le t_M+T_{off(M)}+T_{on}}-\frac{V_{out}}{L}\right]dt+i_{Lo} \tag{3.6}$$

Then, Fourier analysis can be used to derive the Fourier coefficient C_m at perturbation frequency f_m. By substituting (3.5) into (3.6), the Fourier coefficient C_m of the inductor current is derived as (3.7):

$$\begin{aligned} c_{m(i_L)} &= j\frac{2f_m}{N}\int_0^{t_M+T_{off(M)}+T_{on}} i_L(T)e^{-j2\pi f_m t}dt \\ &= \frac{1}{N\pi}\frac{V_{in}}{L}e^{-j2\pi f_m T_{off}}\left(e^{-j2\pi f_m T_{on}}-1\right)\left[\sum_{i=1}^{M}\left(e^{-j2\pi f_m(i-1)T_{sw}}\sum_{k=1}^{i}\Delta T_{off(k)}\right)\right] \end{aligned} \tag{3.7}$$

Step 3: Transfer function derivation

According to [12], based on (3.3), (3.4) and (3.7), the transfer function from the reference voltage to inductor current can be derived as (3.8):

$$\frac{i_L(s)}{v_{ref}(s)} = \frac{1}{1+sR_{ac}\left(\frac{C_{ac}C_{cp}}{C_{ac}+C_{cp}}\right)}\cdot\frac{f_s\left(1-e^{-sT_{on}}\right)\left(1-e^{-sT_{sw}}\right)}{S_f\left[\left(1+\frac{T_{off}}{2R_{esr}C_{out}}+\frac{S_{en}}{S_f}\right)-\left(1-\frac{2T_{on}+T_{off}}{2R_{esr}C_{out}}+\frac{S_{en}}{S_f}\right)e^{-sT_{sw}}\right]}\cdot\frac{V_{in}}{sL} \tag{3.8}$$

With reference-to-inductor current transfer function, the reference-to-output transfer function $G_{vr}(s)$ can be calculated as (3.9):

$$\begin{aligned} G_{vr}(s) &= \frac{v_{out}(s)}{v_{ref}(s)} = \frac{i_L(s)}{v_{ref}(s)}\cdot\frac{v_{out}(s)}{i_L(s)} \\ &= \frac{1}{1+sR_{ac}\left(\frac{C_{ac}C_{cp}}{C_{ac}+C_{cp}}\right)}\cdot\frac{f_s\left(1-e^{-sT_{on}}\right)\left(1-e^{-sT_{sw}}\right)}{S_f\left[\left(1+\frac{T_{off}}{2R_{esr}C_{out}}+\frac{S_{en}}{S_f}\right)-\left(1-\frac{2T_{on}+T_{off}}{2R_{esr}C_{out}}+\frac{S_{en}}{S_f}\right)e^{-sT_{sw}}\right]}\cdot\frac{V_{in}}{sL}\cdot\left(R_{esr}+\frac{1}{sC_{out}}\right) \end{aligned} \tag{3.9}$$

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Based on Padé approximation, (3.9) can be further simplified and pole/zero locations can be separated. Then the approximation of reference-to-output transfer function $G_{vr}(s)$ is expressed as (3.10).

$$G_{vr}(s)=\frac{v_{out}(s)}{v_{ref}(s)}\approx\frac{1}{1+sR_{ac}\left(\frac{C_{ac}C_{cp}}{C_{ac}+C_{cp}}\right)}\cdot\frac{1+sR_{esr}C_{out}}{\left(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}\right)\cdot\left(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}\right)} \tag{3.10}$$

Where,

$$\omega_1=\frac{\pi}{T_{on}},\ Q_1=\frac{2}{\pi},\ \omega_2=\frac{\pi}{T_{sw}},\ Q_2=\frac{T_{sw}}{\pi\left[(R_{cp}+R_{esr})C_{out}-\frac{T_{on}}{2}\right]},\ R_{cp}=\frac{LG_{mH}}{C_{cp}}$$

From (3.10), it can be observed that there is a low-frequency pole related to the charge-pump ramp compensation network. In addition to the low-frequency pole, there are two pairs of high-frequency pole and the locations are half switching frequency and twice on-time period, respectively, which are related to the direct voltage feedback loop. Due to the Padé approximation, the accuracy of this small-signal model is up to half switching frequency. To verify the derived reference-to-output transfer function $G_{vr}(s)$, the SIMPLIS simulation tool is adopted. The simulation circuit and the circuit parameters are shown in Fig. 3.8 and Table 3.1 respectively.

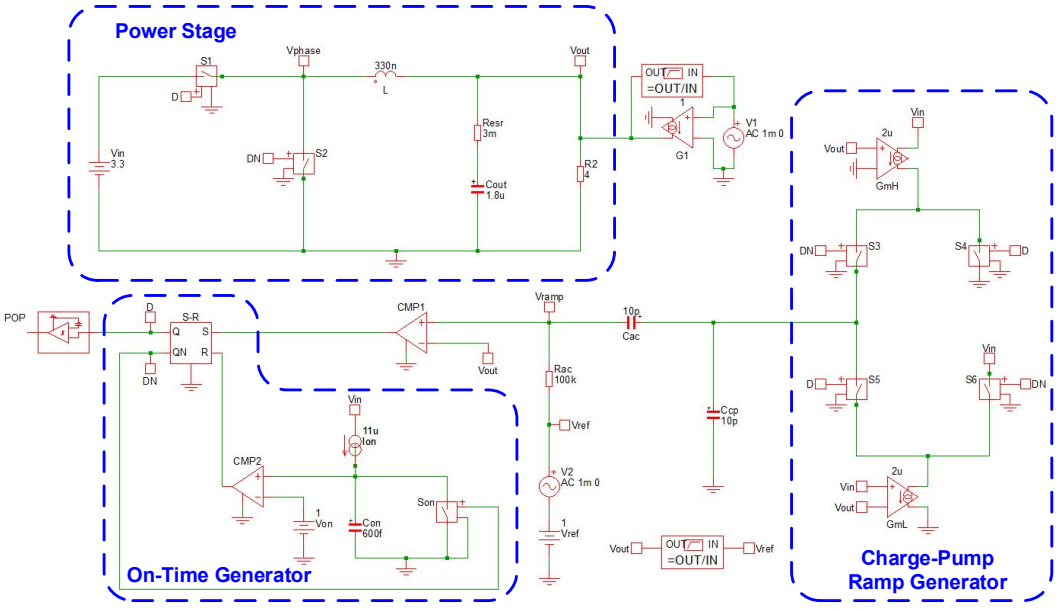

Fig. 3.8 Simulation circuit for CPCOT control scheme

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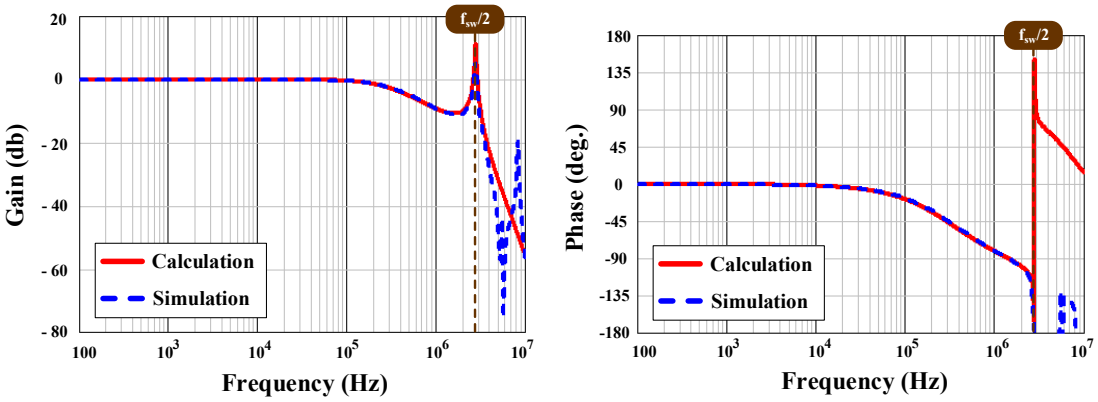
Table 3.1 Circuit parameters for the simulation of CPCOT control

Parameters	Values	
Input voltage V_{in}	3.3 V	
Output voltage V_{out}	1.0 V	
Switching frequency f_{sw}	5.6 MHz	
Inductor L	330 nH	
Output capacitor C_{out}	1.8 μF	
ESR of output capacitor R_{esr}	3 mΩ	
Charge-pump capacitor C_{cp}	10 pF	
Coupling capacitor C_{ac}	10 pF	
Coupling resistor R_{ac}	100 kΩ	
Transconductance G_{mH}	0.4 μA/V (case 1)	2 μA/V (case 2)
Transconductance G_{mL}	0.4 μA/V (case 1)	2 μA/V (case 2)

Fig. 3.9 shows the Bode plots of the reference-to-output transfer function under two design cases of quality factor Q_2. From the Fig. 3.9, the calculated results are well matched with the simulation results for both low quality factor Q_2 and high quality factor Q_2 conditions. Therefore, the derived reference-to-output transfer function is verified.



(a)

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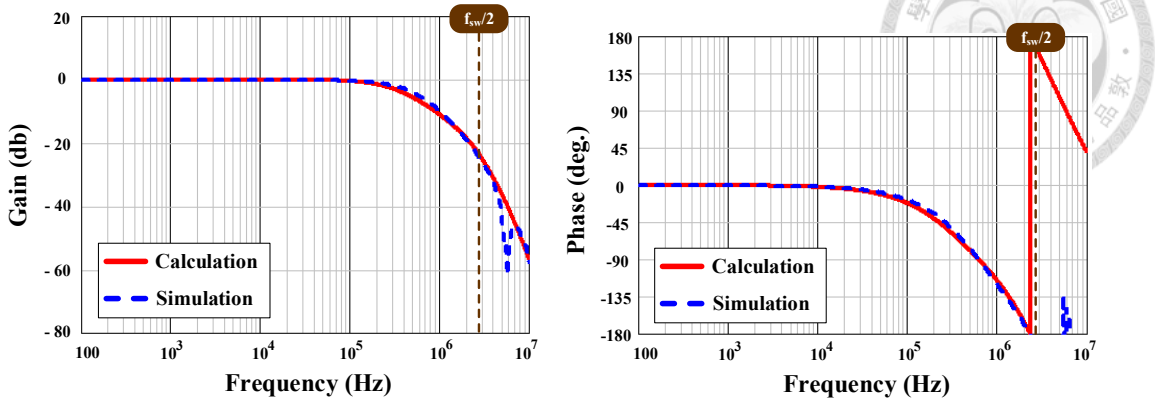

(b)

Fig. 3.9 Model verification of reference-to-output transfer function:

(a) case 1: $Q_2 \approx 34.5$, and (b) case 2: $Q_2 \approx 0.6$

(Dotted line: SIMPLIS simulation, Solid line: Calculation)

From the reference-to-output transfer function $G_{vr}(s)$ in (3.10), the complex poles at half of switching frequency may go to the right-half plane and cause instability. To avoid instability, the design of the charge-pump ramp compensation must satisfy the stability criterion in (3.11):

$$\left(R_{cp}+R_{esr}\right)C_{out} > \frac{T_{on}}{2} \tag{3.11}$$

By comparing (2.1) and (3.10), we see that adding the charge-pump ramp equivalently increases the ESR of the output capacitors. Consequently, with the proper design of charge-pump ramp circuit, there is no subharmonic oscillation for the CPCOT controlled buck converter using low ESR output capacitors, even though the output voltage waveform is dominated by capacitor ripple.

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3.3.2 Output Impedance Transfer Function $v_{out}(s)/i_{out}(s)$

The output impedance can be also derived based on a similar methodology. As shown in Fig. 3.10, a sinusoidal perturbation with a small magnitude at the frequency f_m is injected through the output current i_{out}. Then, based on the perturbed output voltage waveform, the describing function from the output current i_{out} to the output voltage v_{out} can be found out through the mathematical derivation of describing function [4][12].

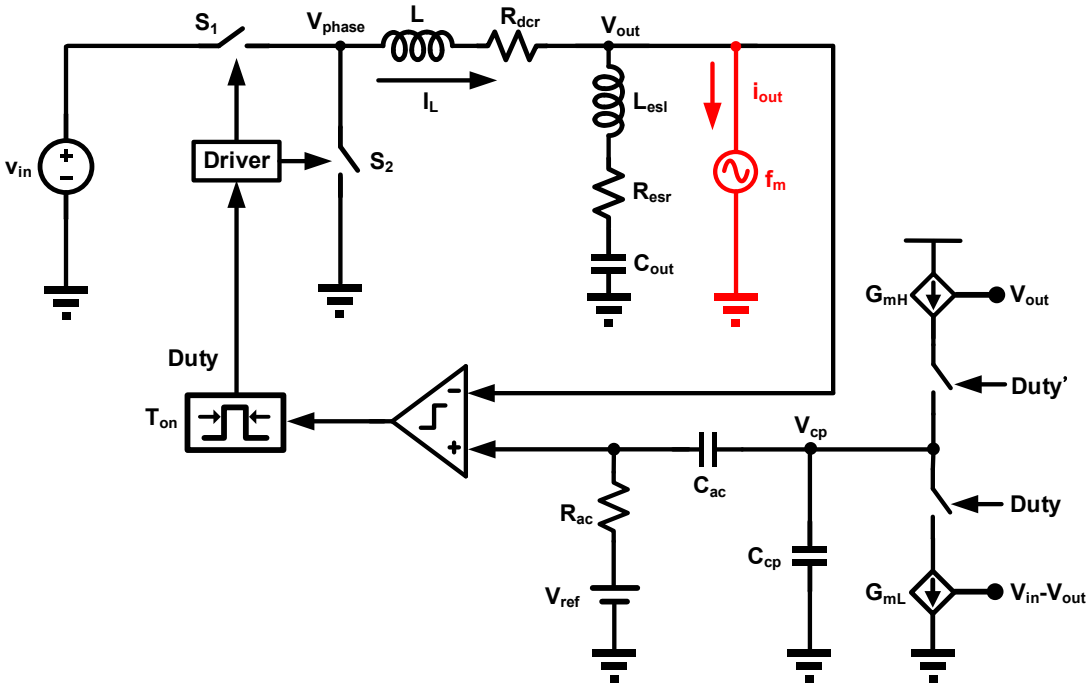

Fig. 3.10 Modeling methodology for output impedance transfer function of proposed CPCOT controlled buck converter

In the s-domain, the output impedance is derived as (3.12):

$$Z_o(s)=\frac{v_{out}(s)}{i_{out}(s)}=\frac{sR_{ac}\left(\frac{C_{ac}C_{cp}}{C_{ac}+C_{cp}}\right)}{1+sR_{ac}\left(\frac{C_{ac}C_{cp}}{C_{ac}+C_{cp}}\right)}\cdot \left(\frac{f_s\left(1-e^{-sT_{on}}\right)\left(1-e^{-sT_{sw}}\right)}{S_f\left[\left(1+\frac{T_{off}}{2R_{esr}C_{out}}+\frac{S_{en}}{S_f}\right)-\left(1-\frac{2T_{on}+T_{off}}{2R_{esr}C_{out}}+\frac{S_{en}}{S_f}\right)e^{-sT_{sw}}\right]}\cdot\frac{V_{in}}{sL}-1\right)\cdot\left(R_{esr}+\frac{1}{sC_{out}}\right) \quad (3.12)$$

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Equation (3.12) can be simplified by Padé approximation, and the simplified output impedance is expressed as (3.13):

$$Z_o(s) \approx \frac{sR_{ac}\left(\frac{C_{ac}C_{cp}}{C_{ac}+C_{cp}}\right)}{1+sR_{ac}\left(\frac{C_{ac}C_{cp}}{C_{ac}+C_{cp}}\right)} \cdot \left(\frac{1+sR_{esr}C_{out}}{\left(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}\right)\cdot\left(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}\right)} - 1 \right) \cdot \left(R_{esr} + \frac{1}{sC_{out}} \right) \quad (3.13)$$

The SIMPLIS simulation tool is used to verify the derived output impedance transfer function. The circuit parameters for the simulation are listed in Table 3.1. Fig. 3.11 shows that the simulated and calculated output impedance transfer functions are well matched under different design values of quality factor Q_2. It is found that the output impedance is very low throughout a wide frequency range, which means the proposed CPCOT control retains the fast load transient response characteristic of traditional RBCOT control even without outer loop compensation.

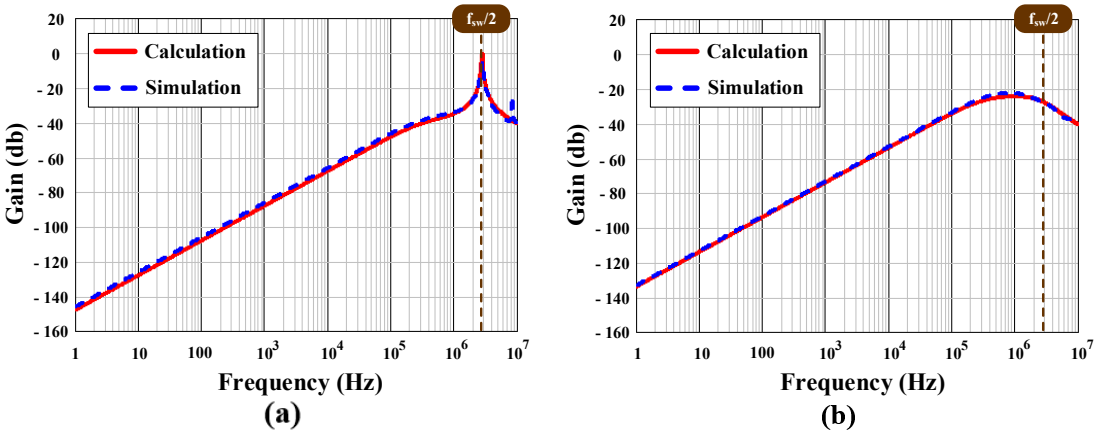

Fig. 3.11 Model verification of output impedance transfer function:

(a) case 1: $Q_2 \approx 34.5$, and (b) case 2: $Q_2 \approx 0.6$

(Dotted line: SIMPLIS simulation, Solid line: Calculation)

However, the magnitude and the shape of the output impedance are affected by the design of charge-pump ramp generator. According to (3.10) and Fig. 3.11, the quality factor Q_2 of double pole reduces as R_{cp} increases, so the double pole peaking of output impedance at half of switching frequency is damped. When Q_2 is too low with over

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designed R_{cp} , the double pole is overdamped and becomes two spilt single poles. The pole at lower frequency determines the settling time of transient response. As a result, a reasonable choice of R_{cp} could provide proper damping for optimal load transient response. In accordance with [9], selecting a Q_2 around 0.6-1 is reasonable since a high-Q double-pole has a peaking effect, whereas a low-Q double pole boosts the magnitude of output impedance at a lower frequency. From the output impedance point of view, high-Q peaking leads to large transient deviation, but too low Q is also undesirable due to the long settling time. Therefore, based on the derived small-signal model, the design parameters of G_{mH} and C_{cp} can be determined appropriately to make sure the quality factor Q_2 within a reasonable range.

3.4 Comparison with Other Ramp Compensation Methods

Compared with the fixed external ramp compensation method [6], the proposed charge-pump ramp compensation is more suitable for wide-range operations because there is no low-frequency complex poles, which cause peaking in low frequency. Moreover, the proposed CPCOT control is more straightforward for analysis and easier to design since this control scheme can separate pole/zero location easily as mentioned in Section 3.3.

Different form compensating the loop by the inductor current ramp [7], which increases the output impedance and causes undesirable output voltage droop, the proposed CPCOT control maintains fast load transient response characteristic of RBCOT control due to very low output impedance throughout a wide frequency range.

Unlike adding the virtual inductor current ramp [8], there is no stability issue in DCM operation since the CPCOT control scheme does not exist the additional third slope in ramp compensation after inductor current reaches zero and both switches of

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buck converter are turned off. Therefore, this control scheme can steadily operate in DCM without adding extra control circuits, which inevitably increase the complexity of circuit implementation. Moreover, from the circuit implementation point of view, there is no need for wide-bandwidth adder in CPCOT control scheme at high switching frequency operation.

In comparison with the capacitor current ramp compensation approach [9], the CPCOT control does not require any current sensing technique which has the sensing accuracy issue and makes the control structure more complicated and less attractive, especially under high switching frequency operation.

3.5 Summary

A modified RBCOT control with charge-pump compensation ramp is proposed to enhance system stability. The circuit diagram and the operating principle of CCM are thoroughly described in Section 3.1. Then, the dynamic-biased technique for the on-time generator to reduce the quiescent current of the controller is also introduced in Section 3.2. In Section 3.3, the small-signal model and stability criteria are developed which serves good design guideline. In Section 3.3.1, the reference-to-output transfer function which can be used for stability investigation is derived. In Section 3.3.2, the output impedance transfer function which can be used to predict the load transient response is derived. Both of the transfer functions $G_{vr}(s)$ and $Z_o(s)$ are derived using describing approach and approximated by Padé approximation. The model results for the CPCOT controlled buck converter are shown in Table 3.2. To investigate whether the proposed charge-pump ramp compensation technique is better than previously reported ramp compensation methods [6]-[9], a brief comparison form the design limitation point of view is described in Section 3.4.

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Table 3.2 Small-signal transfer functions of the proposed CPCOT control

Transfer Function	Expression Equation
Reference-to-Output	$G_{vr}(s) \approx \frac{1}{1+sR_{ac}\left(\frac{C_{ac}C_{cp}}{C_{ac}+C_{cp}}\right)} \cdot \frac{1+sR_{esr}C_{out}}{\left(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}\right)\cdot\left(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}\right)}$
Output Impedance	$Z_o(s) \approx \frac{sR_{ac}\left(\frac{C_{ac}C_{cp}}{C_{ac}+C_{cp}}\right)}{1+sR_{ac}\left(\frac{C_{ac}C_{cp}}{C_{ac}+C_{cp}}\right)} \cdot \left(\frac{1+sR_{esr}C_{out}}{\left(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}\right)\cdot\left(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}\right)} -1 \right) \cdot \left(R_{esr}+\frac{1}{sC_{out}} \right)$
$\omega_1 = \frac{\pi}{T_{on}}, Q_1 = \frac{2}{\pi}, \omega_2 = \frac{\pi}{T_{sw}}, Q_2 = \frac{T_{sw}}{\pi\left[(R_{cp}+R_{esr})C_{out} - \frac{T_{on}}{2}\right]}, R_{cp} = \frac{LG_{mH}}{C_{cp}}$	

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Chapter 4 Circuit Implementation of CPCOT Control Scheme

The RBCOT controlled buck converter with the proposed charge-pump ramp compensation technique is designed and fabricated in TSMC 18-μm technology. Fig. 4.1 shows the full circuit architecture of the proposed control scheme. In this chapter, the circuit structure and implementation of the three main sub-blocks, including the modulation comparator, dynamic-biased on-time generator, and charge-pump ramp generator, will be introduced in detail.

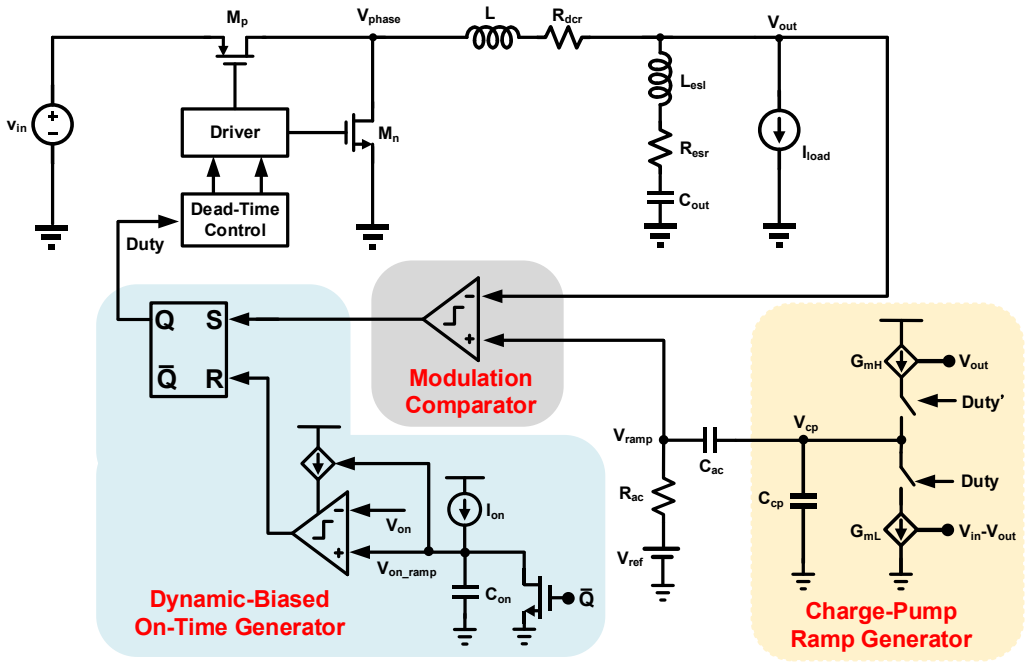

Fig. 4.1 Full circuit architecture of the CPCOT controlled buck converter

4.1 Implementation of Modulation Comparator

In recent years, the high switching frequency operation is preferred to shrink inductor and output capacitor size on printed-circuit-board (PCB) and improve the load transient response. Hence, the effect of modulation comparator delay becomes very critical because the delay time deteriorates system stability, especially for the small on-time situations.

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To make the stability criterion shown in (3.11) more accurate, it is necessary to take the delay-time effect into consideration during the describing function derivation [8]. Fig. 4.2 shows the practical modulation waveforms of the proposed CPCOT control considering the delay-time effect, where T_d represents the delay time of the modulation comparator. The delay time is defined as the time period between the instant of modulation comparator input intersection and the high-side switch turning on. Therefore, the stability criterion of CPCOT control considering the delay-time effect is obtained, as expressed in (4.1):

$$\left(R_{cp}+R_{esr}\right)C_{out} > \frac{T_{on}}{2}+T_d \tag{4.1}$$

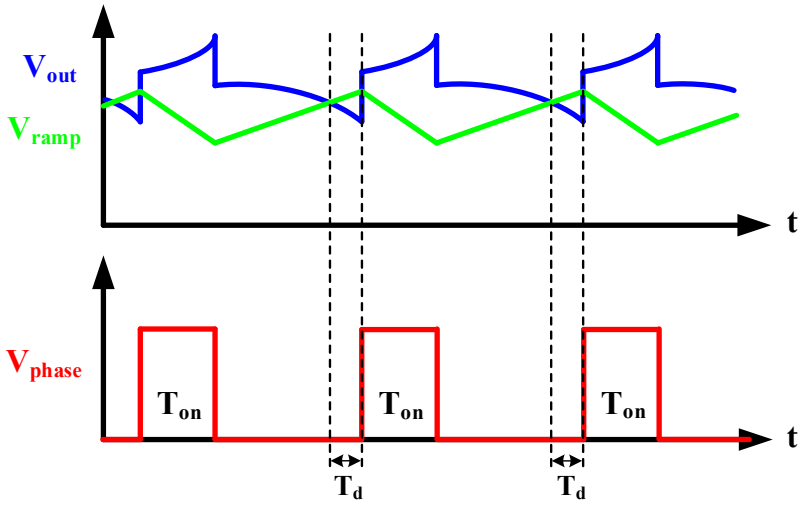

Fig. 4.2 Practical modulation waveforms of the proposed CPCOT control considering modulation comparator delay

Since too much time delay might cause the system unstable, the modulation comparator faces a stringent design requirement. According to Fig. 4.3, the cross-couple and resistive-load amplifiers have faster respond in normal design, which are suitable for MHz switching converter [13]. Therefore, modulation comparator shown in Fig. 4.1 is implemented by the cross-coupled amplifier to achieve ns delay with few tens of μA average current consumption.

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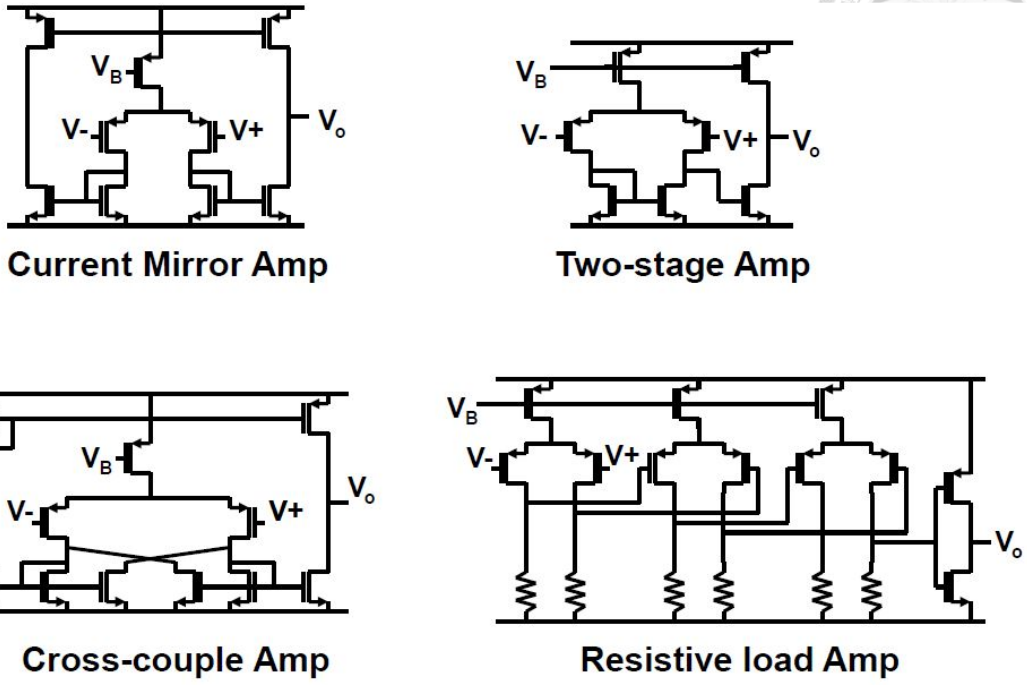

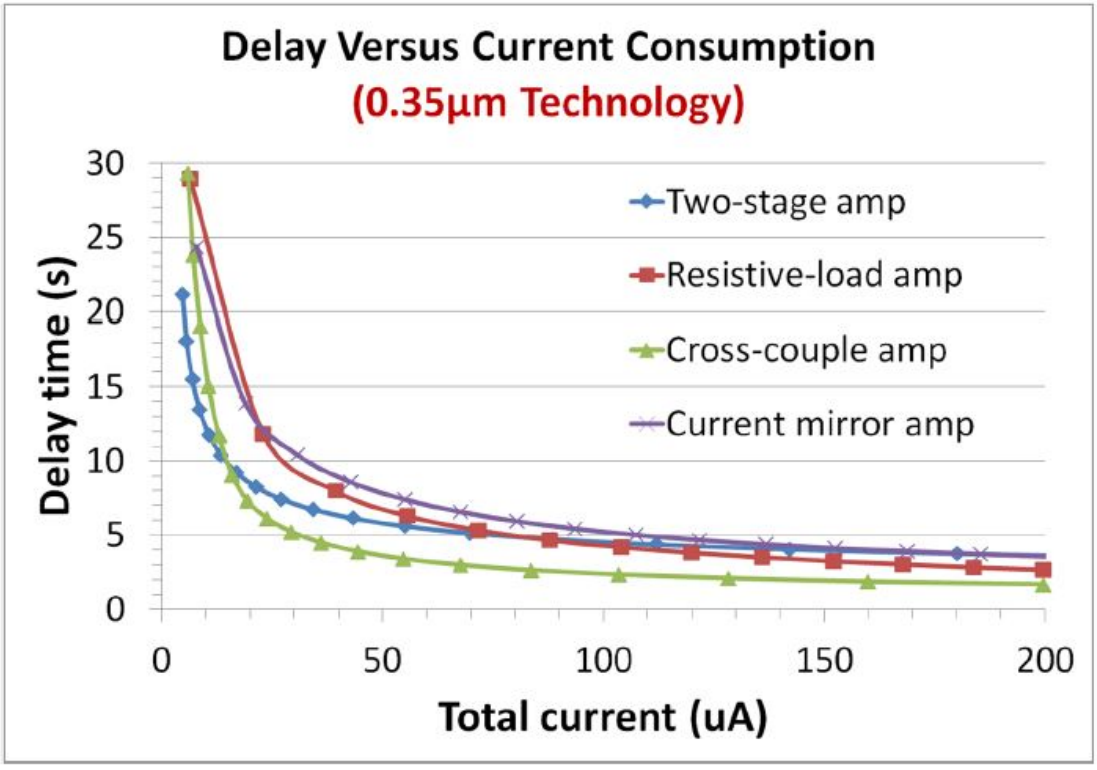

Fig. 4.3 Delay versus current consumption of different types of comparator [13]

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Fig. 4.4 shows the complete circuit implementation of the modulation comparator in the proposed CPCOT controller, which is implemented by a differential input pair with the cross-coupled load. The cross-coupled configuration introduces a positive feedback in the circuit, which provides high gain to reduce propagation delay. The size of each transistor is shown in Table 4.1.

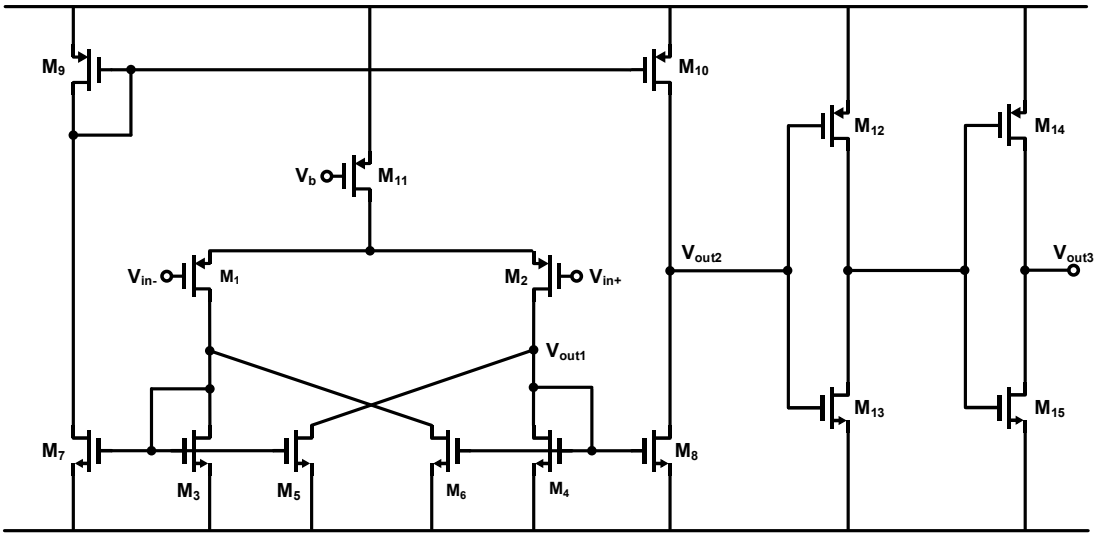

Fig. 4.4 Circuit implementation of the modulation comparator

Table 4.1 Size of each transistor in the modulation comparator

Transistor	Size (W/L/M)	Transistor	Size (W/L/M)
M_1	500n / 300n / 8	M_9	500n / 400n / 1
M_2	500n / 300n / 8	M_{10}	500n / 400n / 1
M_3	1μ / 400n / 1	M_{11}	500n / 1μ / 24
M_4	1μ / 400n / 1	M_{12}	3μ / 350n / 1
M_5	1μ / 400n / 1	M_{13}	1μ / 350n / 1
M_6	1μ / 400n / 1	M_{14}	3μ / 350n / 1
M_7	500n / 400n / 1	M_{15}	1μ / 350n / 1
M_8	500n / 400n / 1		

There are two paths of feedback inside this circuit: a negative feedback path through the common source node of M_1 and M_2, and a positive feedback path through the gate of M_5 and the drain of M_6 and vice versa.

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The positive feedback can be easily understood looking at the small signal variations in the first stage output voltage node V_{out1}. Assuming a small signal decrease of ΔV_{out1}, it means a decrease of M_6 gate voltage. This fact leads to a decrease of I_{d6}. The drop of I_{d6} forces an increase of I_{d3} with the result of enhancing the gate voltage of transistor M_5, which leads to an increase of I_{d5}. Therefore, the enhanced current discharges the output capacitance and contributes to a further decrease in V_{out1}. If the opposite initial assumption is made (small signal increase of ΔV_{out1}), the effect and the analysis are analogous.

The same deductive reasoning is applied for the negative feedback path. Assuming a small signal decrease of ΔV_{out1}, it leads to a decrease of I_{d6} and therefore of I_{d1}. However, the current biasing the input differential pair is constant and a I_{d1} drop forces an increase of I_{d2}. This current charges the output capacitance and contributes to an increase in V_{out1}, working against the discharge carried out by the positive feedback path.

This amplifier uses the negative resistance of the cross-coupled load to compensate for the positive resistance of the diode load and achieve a higher gain. The output resistance of the first stage is given by (4.2):

$$R_{out} \approx \frac{1}{g_{m4} - g_{m5}} \tag{4.2}$$

Assuming $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$ and $g_{m5} = g_{m6}$, the dc gain of the first stage can be derived as (4.3):

$$A_v = \frac{\Delta V_{out1}}{\Delta V_{in}} = g_{m2} R_{out} = \frac{g_{m2}}{g_{m4} - g_{m5}} \tag{4.3}$$

From the equation above, it can be seen that if $g_{m4,5} = g_{m3,6}$, the gain could be infinite.

doi:10.6342/NTU202000925

However, the critical defect of this amplifier is the limited output swing, which is clamped by the diode-connected transistors. As shown in Fig. 4.4, the lowest voltage of V_{out1} is zero, but the highest voltage of V_{out1} is only a diode forward voltage over 0 V. Obviously, this is not the way of operation expected from a comparator. Therefore, it is necessary to add a second stage to provide a higher gain and a full-swing output.

The simplest solution is to use a push-pull second stage, which is formed by transistors M_7-M_{10}. This is mainly an inverter stage whose current is given using the diode load as a mirror and therefore uses the mirrors to perform a differential to single-ended conversion. The overall gain of cross-coupled amplifier with push-pull stage will become higher and is given by (4.4).

$$A_v = \frac{\Delta V_{out2}}{\Delta V_{in}} = g_{m8}\left(r_{o8} \parallel r_{o10}\right) \cdot \frac{g_{m2}}{g_{m4} - g_{m5}} \tag{4.4}$$

The inverter chains M_{12}-M_{15} are used to increase the response of the comparator output signal. In addition, they can act as a driver stage such that the transistors M_7 and M_8 can be made smaller to reduce the parasitic capacitance at the gates of M_7 and M_8 for a faster response [14].

Fig. 4.5 shows the test bench and the frequency response Bode diagram of the modulation comparator simulation. The DC gain of the modulation comparator is 70 dB and the 3 dB bandwidth is around 8.25 MHz with 50 fF load and 1.0 V $V_{in,cm}$. According to simulation results shown in Fig. 4.6, the delay time of the modulation comparator is around 10 ns, which is still acceptable for the proposed CPCOT controlled buck converter under MHz switching frequency operation without subharmonic oscillation phenomenon.

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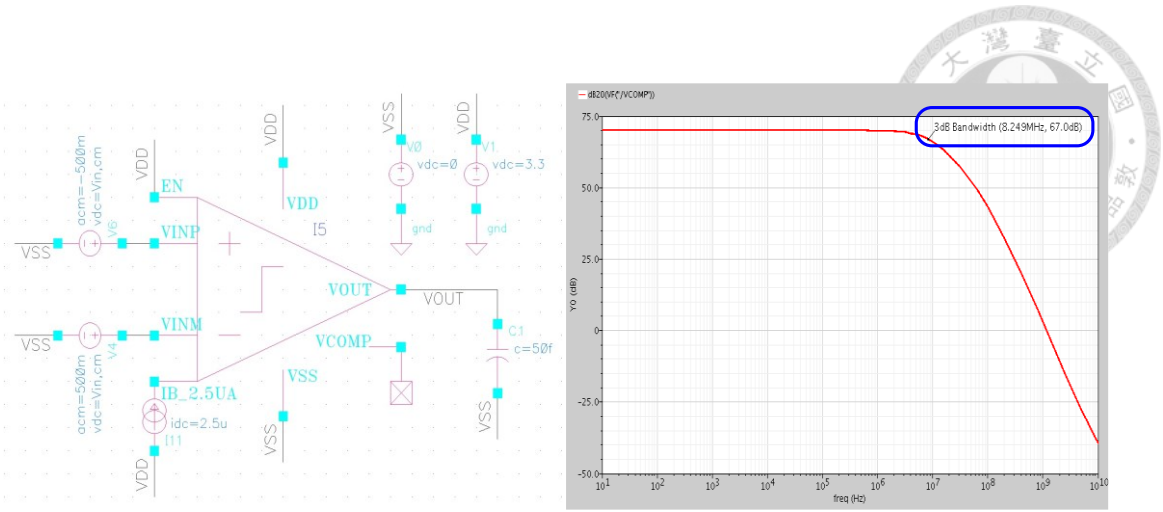

Fig. 4.5 Test bench and the frequency response Bode diagram of the modulation comparator simulation

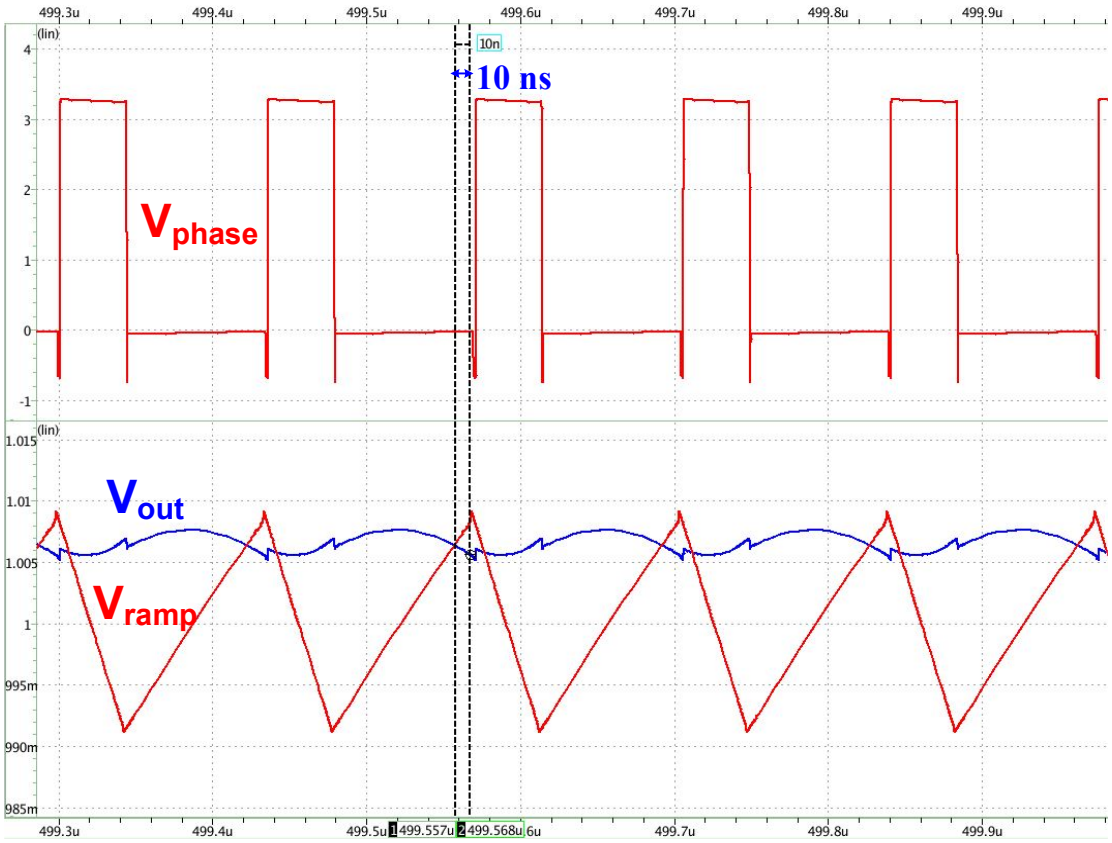

Fig. 4.6 Simulated modulation waveforms of CPCOT controlled buck converter with the designed modulation comparator (V_{in} = 3.3 V, V_{out} = 1.0 V)

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4.2 Implementation of Dynamic-Biased On-Time Generator

Fig. 4.7 shows the fundamental structure of the basic constant on-time generator to realize the fixed pulse of one period. The current I_{on} charges C_{on} to increase V_{on_ramp} from zero to V_{on}. The on-time can be derived as (4.5) with its characteristics proportional to V_{on} and inversely proportional to I_{on}. The on-time value can be adjusted by different C_{on}, I_{on}, and V_{on}.

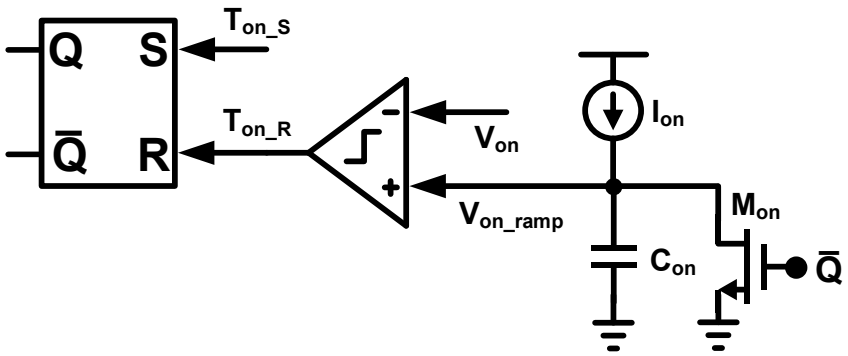

Fig. 4.7 Model of the basic constant on-time generator

$$T_{on} = \frac{C_{on} \cdot V_{on}}{I_{on}} \tag{4.5}$$

Fig. 4.8 illustrates the ideal operation of constant on-time generator. The switching period T_{sw} is defined as a period that starts when V_{out} falls below V_{ramp} and terminates when the next switching starts again. At the beginning of T_{sw}, the modulation comparator output T_{on_S} becomes high to trigger the on-time pulse when V_{out} falls below V_{ramp}. Meanwhile, the MOSFET M_{on} controlled by the signal $\bar{Q}$ turns off. Thereafter, the current source I_{on} starts to charge the capacitor C_{on}, so the voltage V_{on_ramp} linearly increases during the T_{on} period. When V_{on_ramp} reaches the upper threshold V_{on}, the on-time comparator output T_{on_R} becomes high and the T_{on} period is terminated. In the meantime, V_{on_ramp} is reset to zero by signal $\bar{Q}$ and prepared to trigger in the next period.

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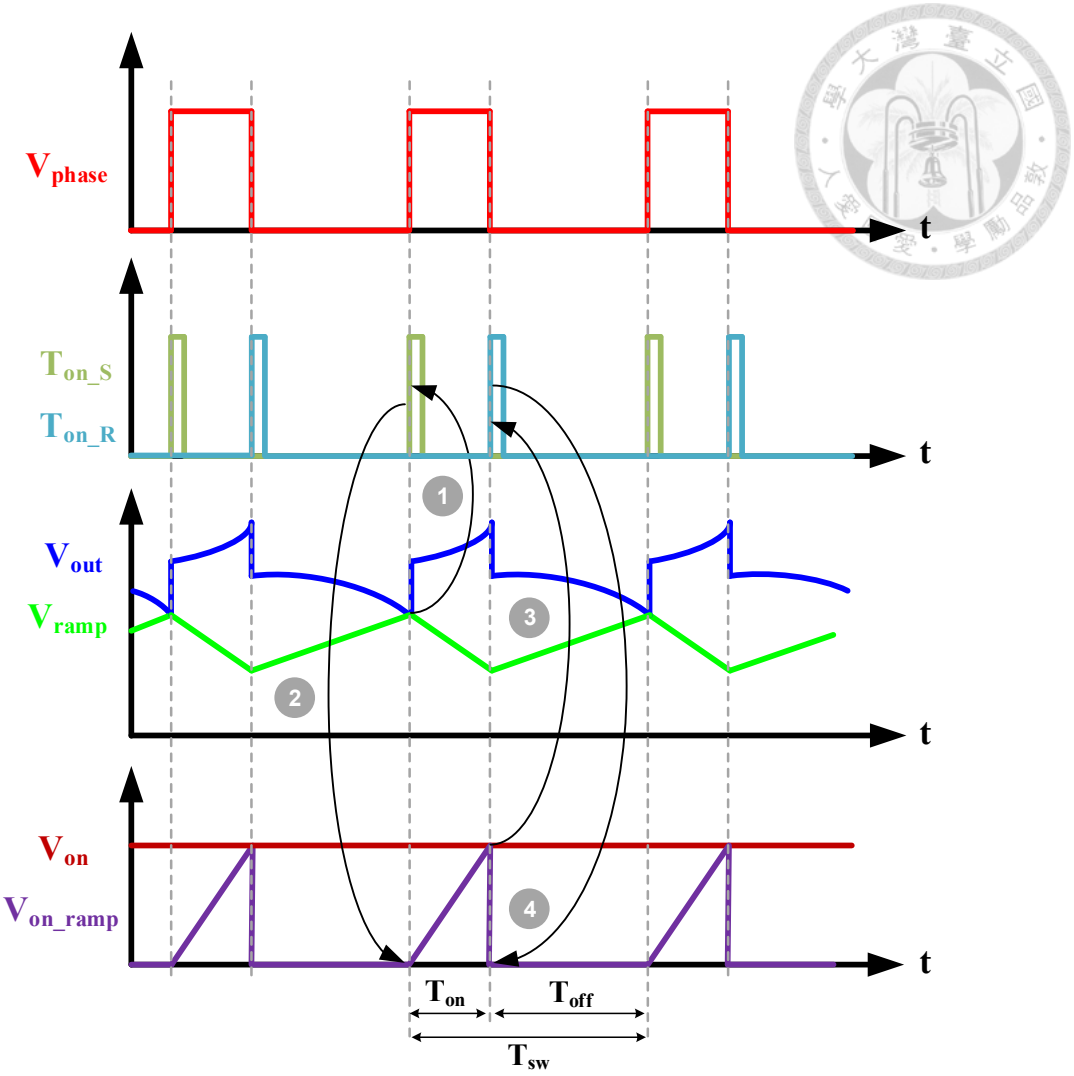

Fig. 4.8 Ideal operating waveforms of constant on-time generator

However, in practice, there is a delay-time effect of the on-time comparator, which increases the design value of the generated on-time, as shown in Fig. 4.9. If the switching frequency is as high as the MHz range, the delay time of on-time comparator $T_{on,d}$ cannot be ignored. The delay time is defined as the time period between the instant of on-time comparator input intersection and the high-side switch turning off. Therefore, the stability criterion of CPCOT control considering both delay-time effect of modulation comparator and on-time comparator is obtained, as expressed in (4.6):

$$\left(R_{cp}+R_{esr}\right)C_{out}>\frac{T_{on,ideal}+T_{on,d}}{2}+T_d \tag{4.6}$$

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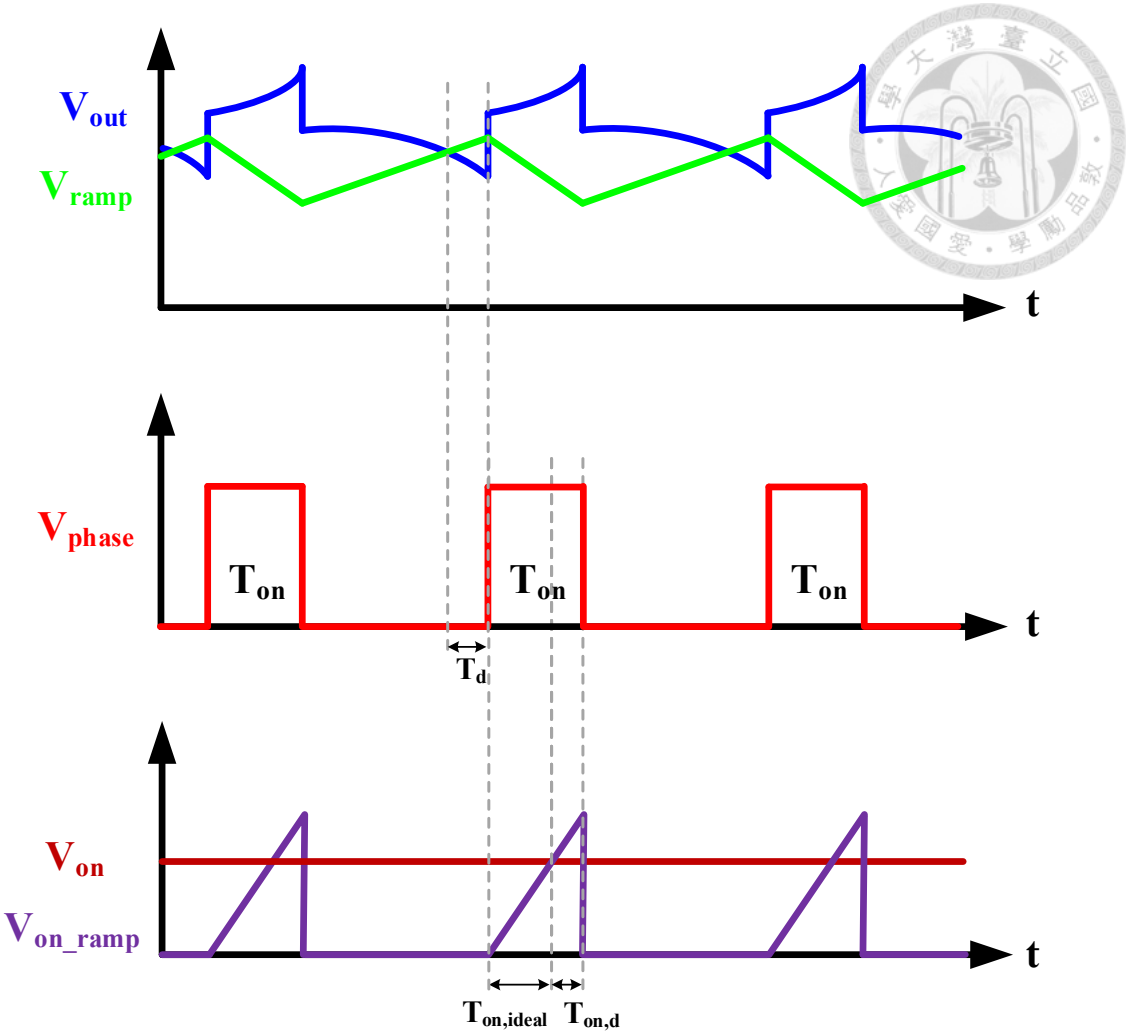

Fig. 4.9 Practical operating waveforms of constant on-time generator considering on-time comparator delay

To minimize the delay time for high switching frequency operation, the conventional on-time generator needs a high-speed comparator which consumes large current and dominates the power consumption of the controller. In order to reduce the quiescent current of CPCOT control IC, a dynamic-biased technique reusing on-time ramp information is proposed to bias the on-time comparator efficiently, as mentioned in Section 3.2. Fig. 4.10 shows the structure of the dual-mode constant on-time generator, including both traditional constant-biased mode and proposed dynamic-biased mode for the on-time comparator.

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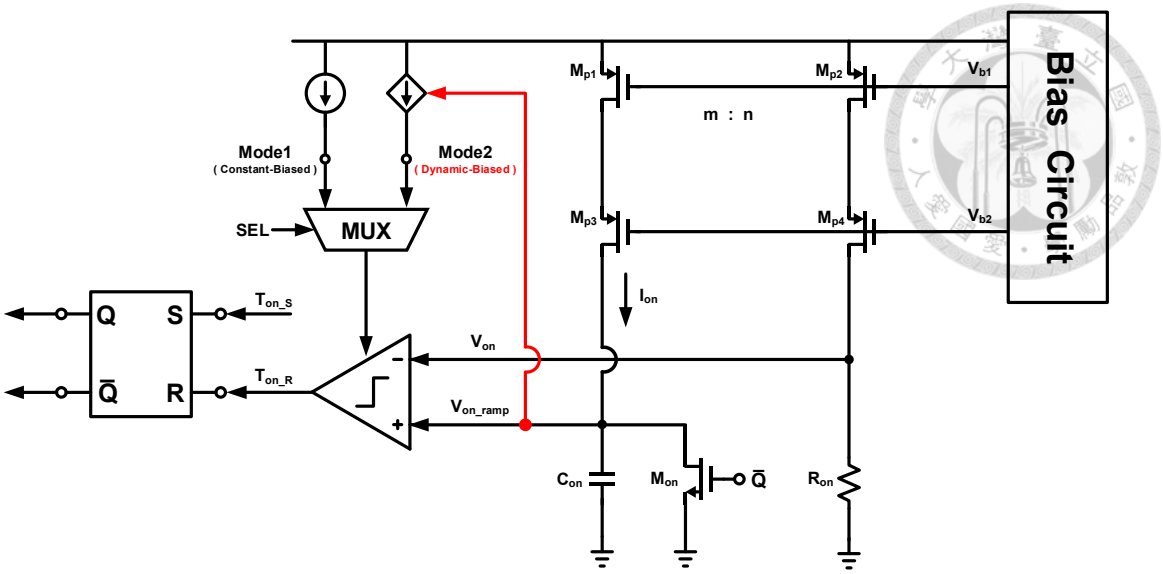

Fig. 4.10 Structure of dual-mode constant on-time generator

In this circuit design, the charging current I_{on} and threshold voltage V_{on} is generated by the bias circuit and resistor R_{on}. As a result, the ideal on-time period $T_{on,ideal}$ can be expressed as (4.7), which is determined by R_{on} , C_{on} and the current mirror ratio.

$$T_{on,ideal} = \frac{C_{on} \cdot V_{on}}{I_{on}} = \frac{n}{m} \cdot C_{on} \cdot R_{on} \tag{4.7}$$

Fig. 4.11 shows the circuit implementation of the proposed dynamic-biased on-time comparator. It consists of a source-coupled pair, a tail-current source, a cross-coupled load, inverter chains, and a mux to select traditional constant-biased mode or proposed dynamic-biased mode. The size of each transistor is shown in Table 4.2.

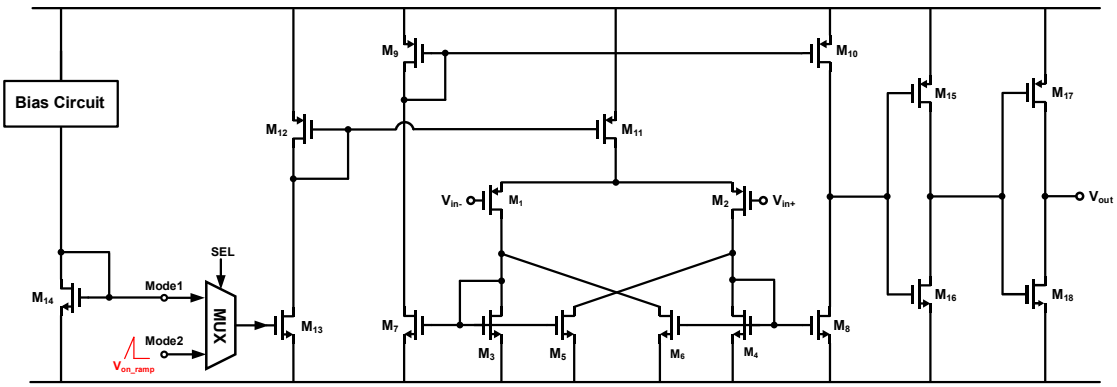

Fig. 4.11 Circuit implementation of the dynamic-biased on-time comparator

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Table 4.2 Size of each transistor in the dynamic-biased on-time comparator

Transistor	Size (W/L/M)	Transistor	Size (W/L/M)
M_1	4μ / 300n / 1	M_{10}	500n / 400n / 1
M_2	4μ / 300n / 1	M_{11}	500n / 1μ / 24
M_3	1μ / 400n / 1	M_{12}	500n / 1μ / 2
M_4	1μ / 400n / 1	M_{13}	1μ / 500n / 2
M_5	1μ / 400n / 1	M_{14}	1μ / 500n / 2
M_6	1μ / 400n / 1	M_{15}	3μ / 350n / 1
M_7	500n / 400n / 1	M_{16}	1μ / 350n / 1
M_8	500n / 400n / 1	M_{17}	3μ / 350n / 1
M_9	500n / 400n / 1	M_{18}	1μ / 350n / 1

Fig. 4.12 shows that the DC gain of the on-time comparator is 60 dB and the 3 dB bandwidth is around 26 MHz with 50 fF load and 1.0 V $V_{in,cm}$. According to simulation results, as shown in Fig. 4.13, the delay time of the on-time comparator is around 5 ns.

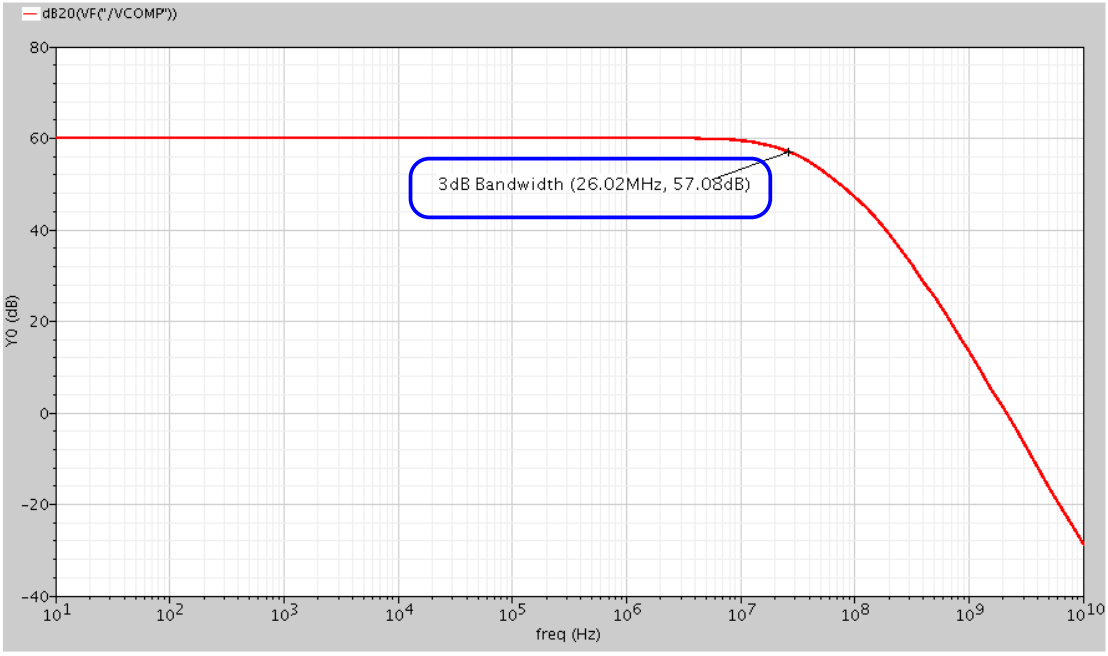

Fig. 4.12 Simulated gain plot of the dynamic-biased on-time comparator

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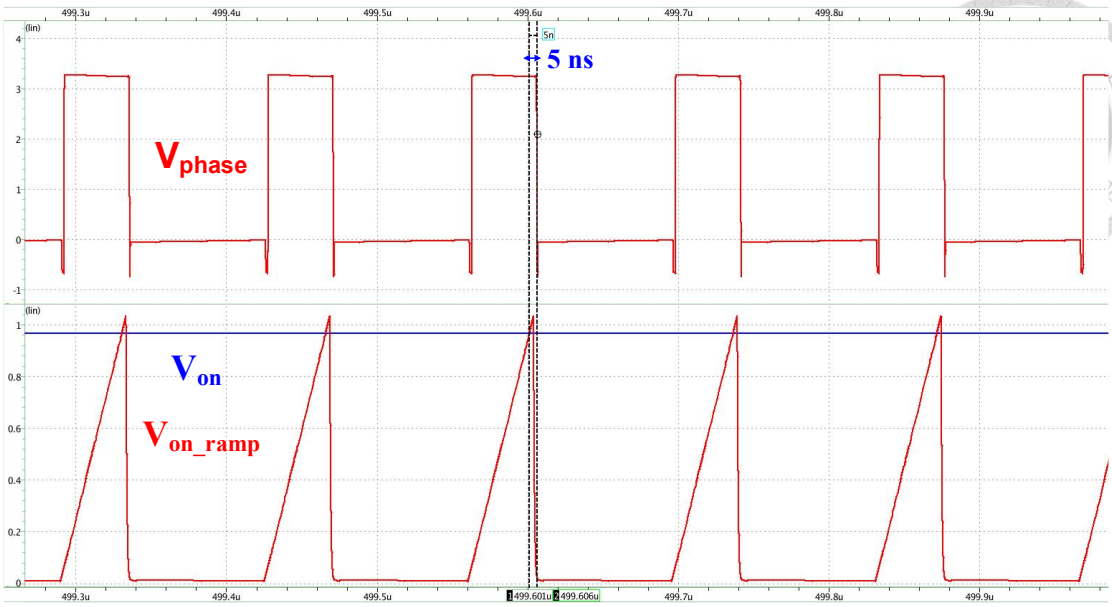
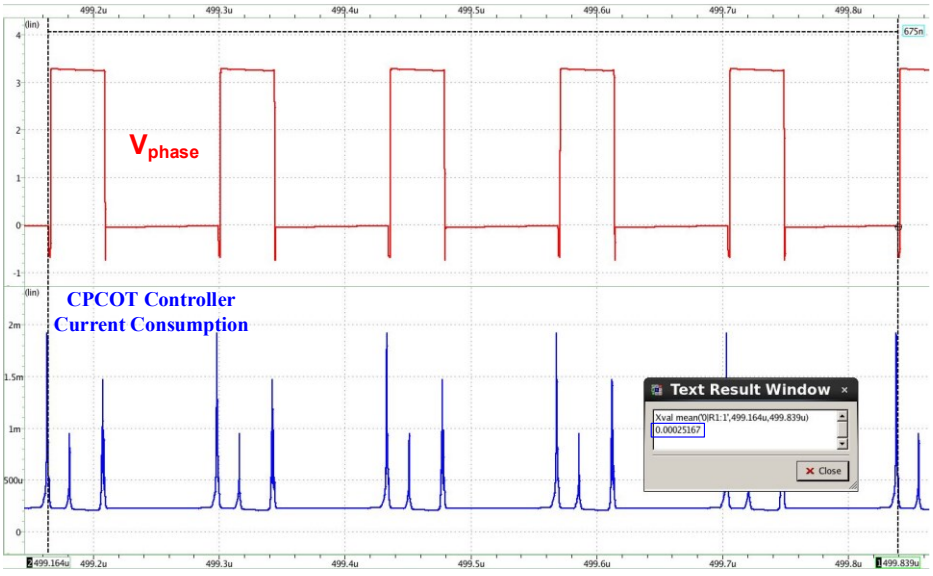


Fig. 4.13 Simulated waveforms of constant on-time generator with the designed dynamic-biased on-time comparator (V_{in} = 3.3 V, V_{out} = 1.0 V)

Due to the proposed dynamic-biased technique for the constant on-time generator, the average current consumption of CPCOT controller in a period of CCM operation is reduced from 251.67 μA to 227.72 μA, as shown in Fig. 4.14. Compared with traditional constant-biased method, the power consumption of CPCOT controller is decreased by 8.6%. Therefore, this proposed biased technique can easily reduce the quiescent current of controller to save power loss for higher efficiency.



(a)

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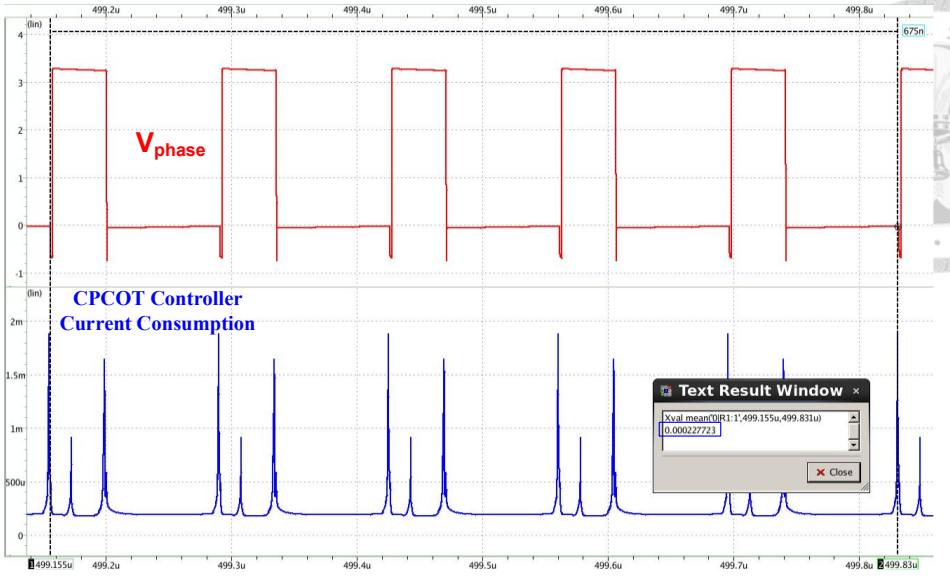

(b)

Fig. 4.14 Simulation results of the average current consumption of CPCOT controller in CCM (V_{in} = 3.3 V, V_{out} = 1.0 V) with: (a) constant-biased mode [251.67 µA], and (b) dynamic-biased mode [227.72 µA]

4.3 Implementation of Charge-Pump Ramp Generator

As shown in Fig. 4.15, the charge-pump ramp generator is formed by a pair of voltage controlled current sources with transconductance G_{mH}, G_{mL} and switches to charge and discharge the capacitor C_{cp} linearly. Then, this ramp signal is coupled to reference voltage V_{ref} through a capacitor C_{ac} and a resistor R_{ac} to enhance the effect of ESR ripple for better stability.

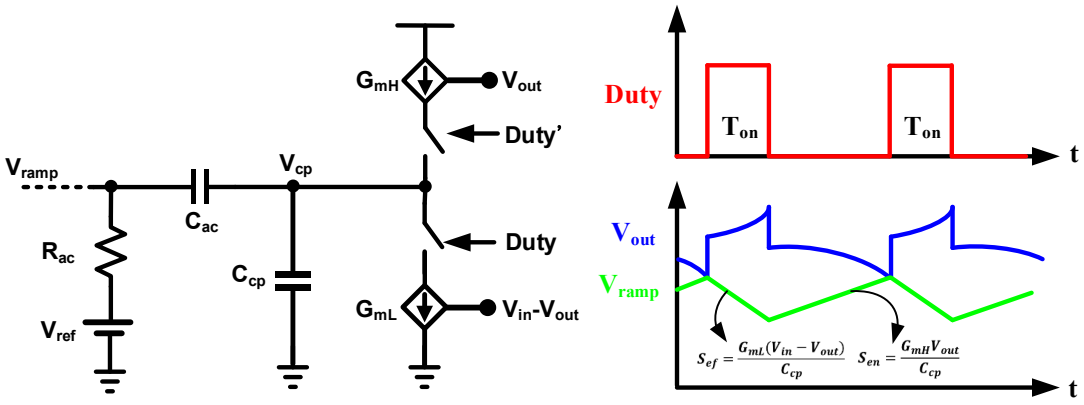

Fig. 4.15 Structure of the charge-pump ramp generator

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To make sure the ramp voltage V_{ramp} is a perfect triangular ramp without distortion, the design parameters, R_{ac} and C_{ac}, need to be chosen carefully. Fig. 4.16 illustrates that if the value of C_{ac} is designed too small, the charge-pump compensation ramp cannot be well coupled to reference voltage V_{ref} due to attenuation.

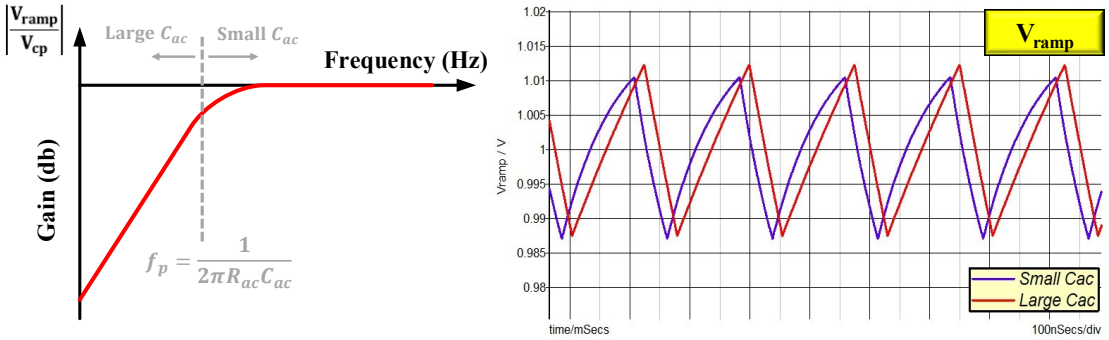

Fig. 4.16 Design consideration of AC-coupled path for the charge-pump ramp

Fig. 4.17 shows the circuit implementation of the transconductor G_{mH} in Fig. 4.15, which is used to charge the capacitor C_{cp} during off-time period. It is based on an operational amplifier driving an NMOS M_1 and a grounded resistance R_H in a negative feedback loop. Then, the output current I_{out} of the V-I converter with input voltage V_{out} is given by (4.8):

$$I_{out} = \frac{V_{out}}{R_H} \tag{4.8}$$

Therefore, the transconductance G_{mH} is given by (4.9):

$$G_{mH} = \frac{I_{out}}{V_{out}} = \frac{1}{R_H} \tag{4.9}$$

As a result, the rising slope of the ramp voltage V_{ramp} during off-time period can be obtained as (4.10):

$$S_{en} = \frac{G_{mH} V_{out}}{C_{cp}} \tag{4.10}$$

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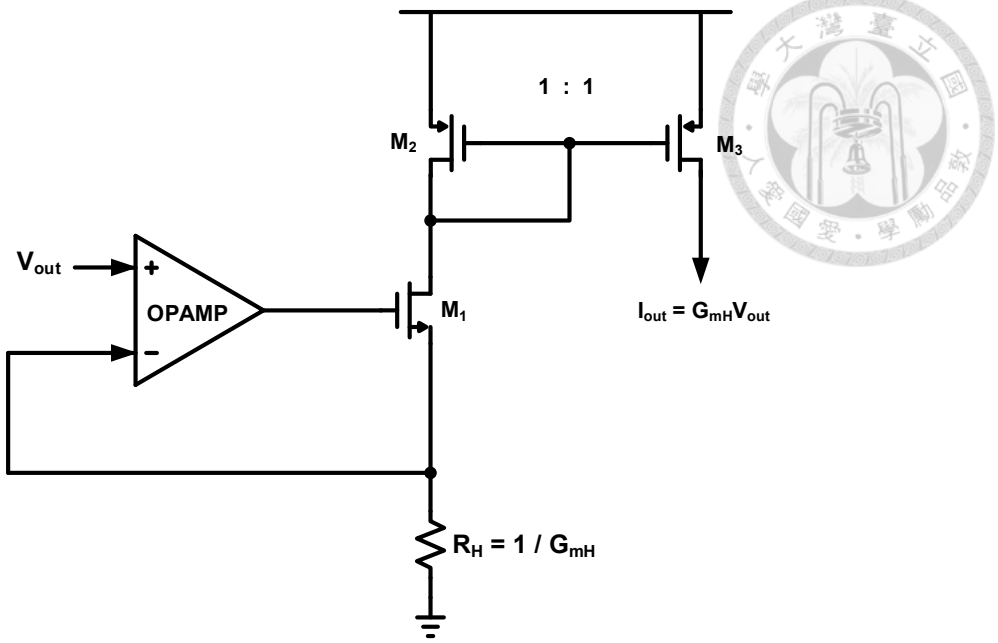

Fig. 4.17 Circuit implementation of the transconductor G_{mH}

Fig. 4.18 shows the circuit implementation of the transconductor G_{mL} in Fig. 4.15, which is used to discharge the capacitor C_{cp} during on-time period. The size of each transistor is shown in Table 4.3. It is realized by the simple differential pair with source degeneration using resistor R_L. Assuming the voltage across the resistor R_L is equal to the input voltage, which means $V_{gs2} - V_{gs1} \approx 0$, then the output current I_{out} of the transconductor with input voltage $V_{in} - V_{out}$ is given by (4.11):

$$I_{out} = \frac{V_{in} - V_{out}}{R_L} = G_{mL}(V_{in} - V_{out}) \tag{4.11}$$

Therefore, the transconductance G_{mL} is given by (4.12):

$$G_{mL} \approx \frac{1}{R_L} \tag{4.12}$$

As a consequence, the falling slope of the ramp voltage V_{ramp} during on-time period can be obtained as (4.13):

$$S_{ef} = \frac{G_{mL}\left(V_{in} - V_{out}\right)}{C_{cp}} \tag{4.13}$$

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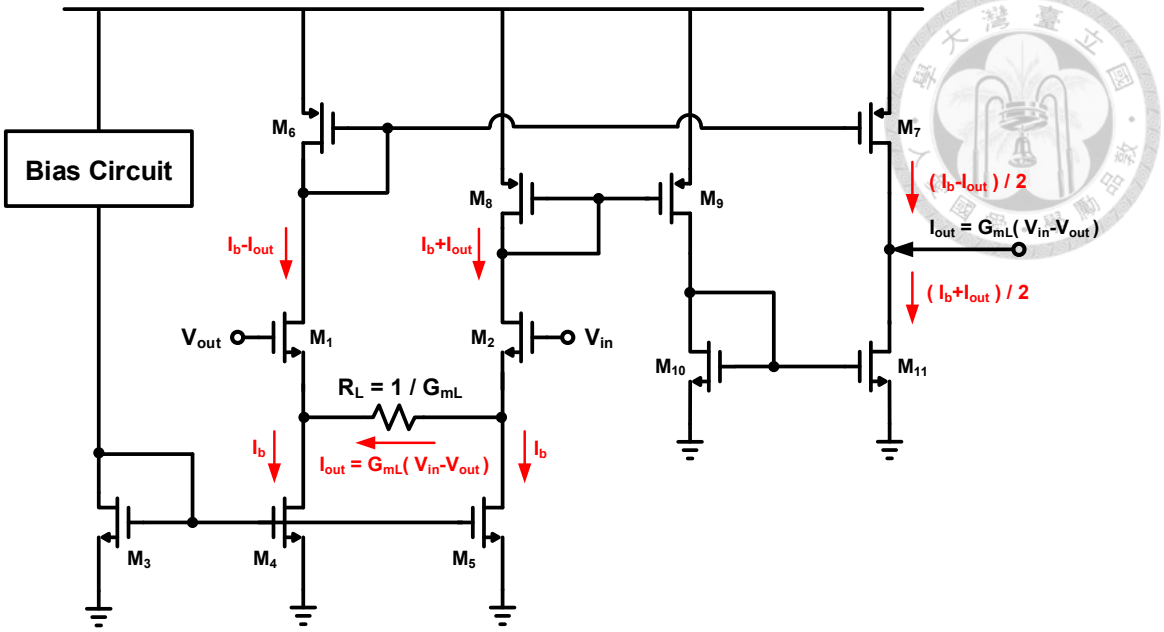

Fig. 4.18 Circuit implementation of the transconductor G_{mL}

Table 4.3 Size of each transistor in the transconductor G_{mL}

Transistor	Size (W/L/M)	Transistor	Size (W/L/M)
M_1	8μ / 350n / 4	M_7	2μ / 1μ / 4
M_2	8μ / 350n / 4	M_8	2μ / 1μ / 8
M_3	2μ / 1μ / 2	M_9	2μ / 1μ / 4
M_4	2μ / 1μ / 8	M_{10}	2μ / 1μ / 2
M_5	2μ / 1μ / 8	M_{11}	2μ / 1μ / 2
M_6	2μ / 1μ / 8		

According to [15], the disadvantage of this transconductor is that large resistor value is needed in order to maintain a wider linear input range. Owing to $G_{mL} \approx 1/R_L$, the higher transconductance is limited by the smaller resistor. Hence, there is a tradeoff between wide linear input range and higher transconductance which is mainly determined by a resistor.

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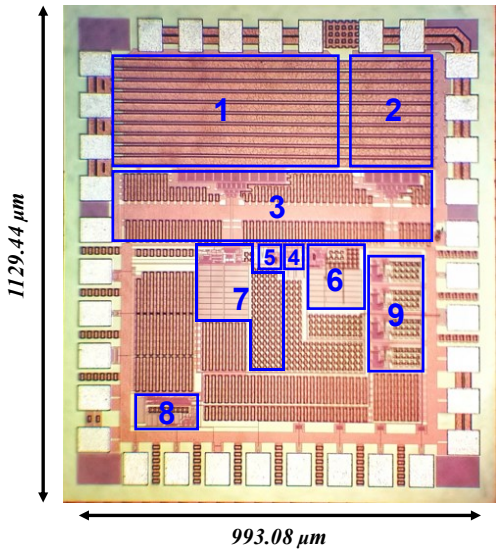
Chapter 5 Simulation and Experiment Results

In this chapter, the simulation and experiment results will be given to verify the proposed CPCOT controlled buck converter with dynamic-biased on-time generator. The experimental platform and printed circuit boards (PCB) will be introduced first. Then, the simulation and experiment results of steady-state operation, load transient response, dynamic-biased technique and efficiency curve will be demonstrated. Finally, a performance comparison table with prior arts in the design of constant on-time controlled buck converter will be shown.

5.1 Specification

The proposed charge-pump constant on-time controlled buck converter with dynamic-biased on-time generator was fabricated into IC using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm CMOS process. The chip micrograph is shown in Fig. 5.1, which consists of power MOS, power MOS gate driver, dead-time controller, modulation comparator, on-time generator, charge-pump ramp generator, bias circuit, test circuit and bypass capacitors. The chip area including all bounding pads is approximately 1.12 mm^2.



1. Power PMOS
2. Power NMOS
3. Driver
4. Dead-Time Controller
5. Modulation Comparator
6. On-Time Generator
7. Charge-Pump Ramp Generator
8. Bias Circuit
9. Test Circuit

Fig. 5.1 Chip micrograph

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Table 5.1 lists the specification and the circuit parameters of this converter. The off-chip inductor, IHLP5050EZERR33M5A from Vishay Intertechnology, is 330 nH. The output capacitor, C0816X5R0J105M050AC from TDK Corporation, is 1.8 μF. This converter can produce adjustable output voltage from 0.6 V to 1.3 V while the input voltage is 3.3 V. Besides, it is capable of supplying load current from 0.25 A to 1.25 A. Under the ranges described above, the circuit is guaranteed to work properly. The experimental results show that the on-time is fixed as 54 ns during steady-state operation and the switching frequency varies from 3.52 MHz to 8.14 MHz under different working conditions.

Table 5.1 Specification and circuit parameters for the proposed CPCOT controlled buck converter

Power Stage Parameters	**Values**
Input voltage V_{in}	3.3 V
Output voltage V_{out}	0.6 - 1.3 V
Load range I_{load}	0.25 - 1.25 A
Switching frequency f_{sw}	3.52 - 8.14 MHz
Inductor L	330 nH
DCR of inductor R_{dcr}	1 mΩ
Output capacitor C_{out}	1.8 μF
ESR of output capacitor R_{esr}	3 mΩ
ESL of output capacitor L_{esl}	75 pH

Control Stage Parameters	**Values**
Charge-pump capacitor C_{cp}	10 pF
Coupling capacitor C_{ac}	10 pF
Coupling resistor R_{ac}	100 kΩ
Transconductance G_{mH}	2 μA/V
Transconductance G_{mL}	2 μA/V

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5.2 Printed Circuit Board (PCB) Design and Experimental Platform

5.2.1 Printed Circuit Board (PCB) Design

Fig. 5.2 shows the prototype of the proposed charge-pump constant on-time controlled buck converter with dynamic-biased on-time generator. The length and the width of the printed circuit board (PCB) is 9.25 cm and 8.5 cm respectively. The PCB schematic and layout are demonstrated in Fig. 5.3 and Fig. 5.4.

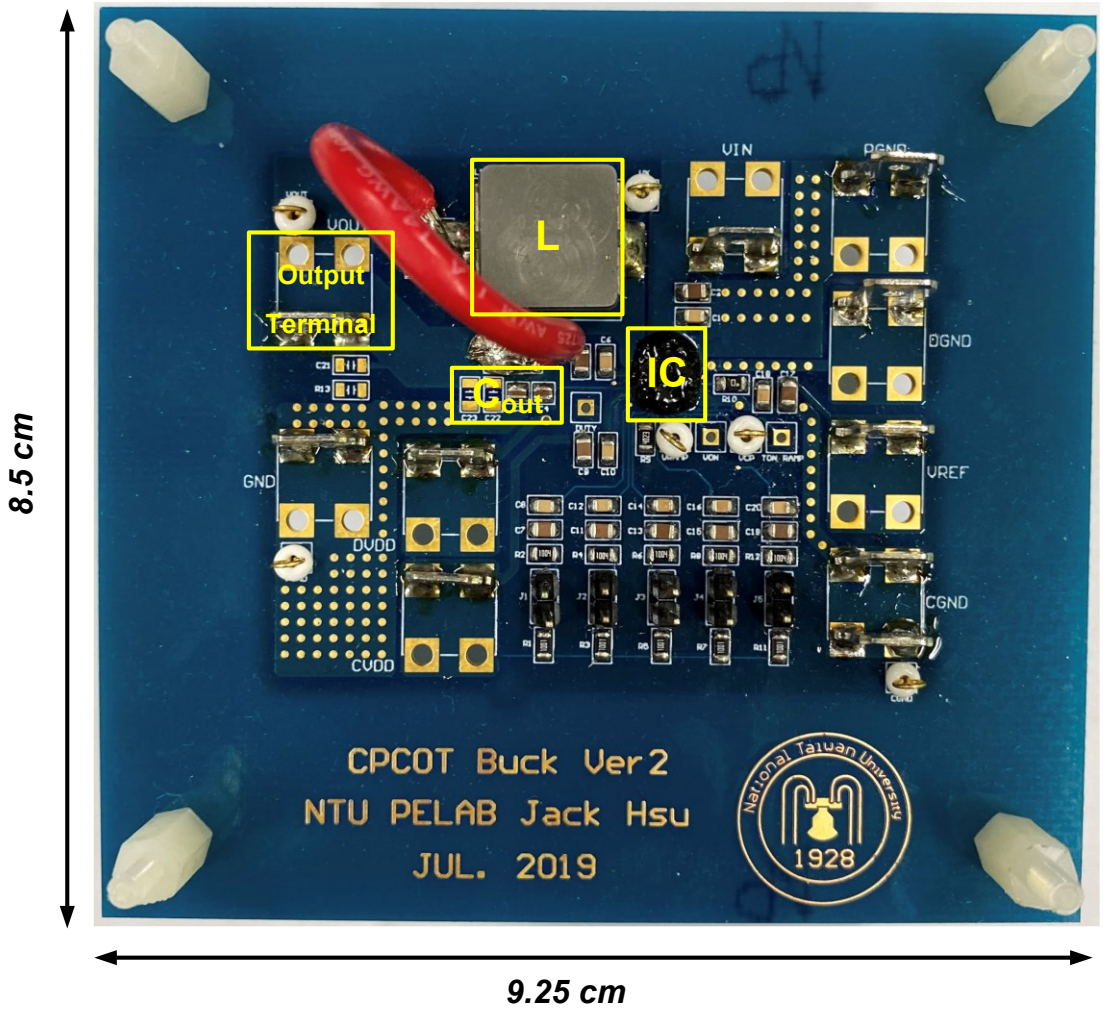

Fig. 5.2 Prototype of the proposed CPCOT controlled buck converter

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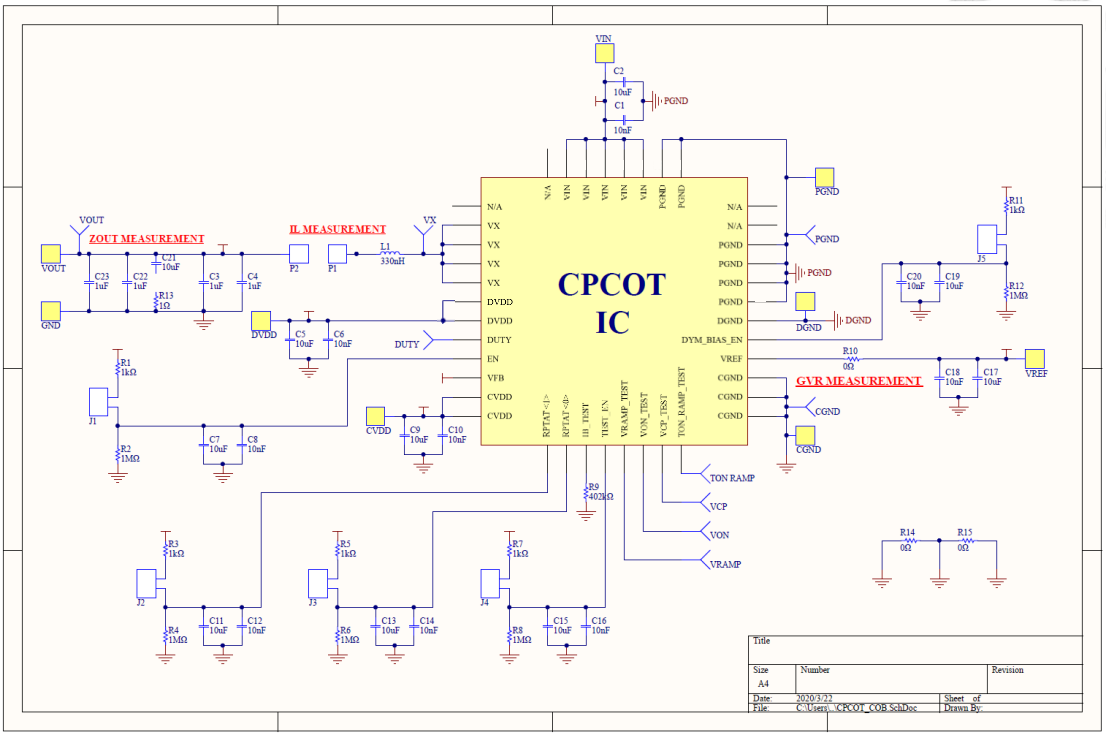

Fig. 5.3 PCB schematic of the proposed CPCOT controlled buck converter

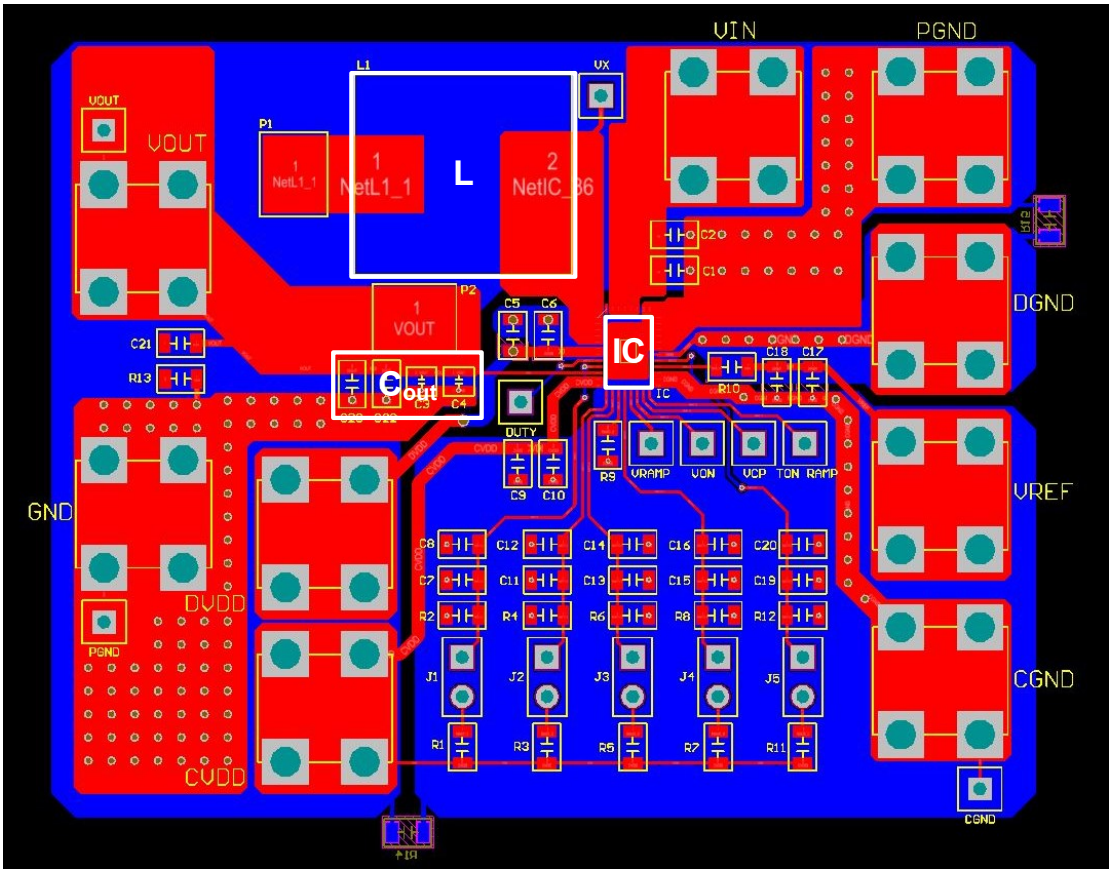

Fig. 5.4 PCB layout of the proposed CPCOT controlled buck converter

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To reduce the parasitic inductance and resistance effect, the proposed control IC is wired and bounded directly to the printed circuit board by chip on board (COB) method. Fig. 5.5 shows the bonding diagram of the chip and the pin configuration is listed in Table 5.2.

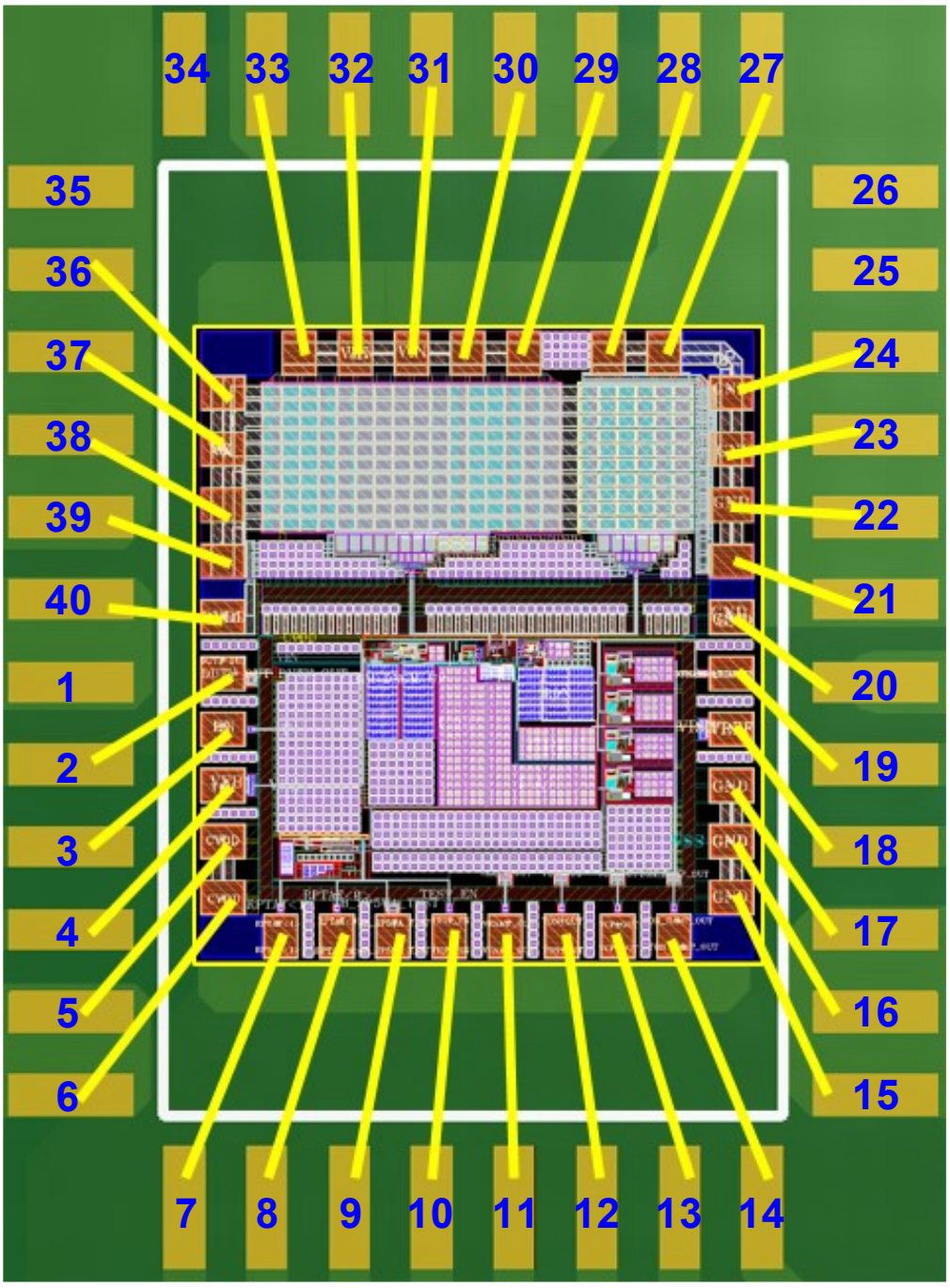

Fig. 5.5 Bonding diagram

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Table 5.2 Pin configuration

Pin Number	Symbol	Description
1, 40	DVDD	Supply voltage for internal gate driver
2	DUTY	Test point for the Duty signal
3	EN	Tie high to enable the IC
4	VFB	Output voltage sense point for modulation and charge-pump ramp generation
5, 6	CVDD	Supply voltage for internal controller
7	RPTAT < 1 >	Control bits for adjusting the bias current value
8	RPTAT < 0 >	
9	IB TEST	Test point for the bias current measurement
10	TEST EN	Tie high to enable the testing function for V_{ramp}, V_{on}, V_{cp}, and $V_{on\ ramp}$ signal
11	VRAMP TEST	Test point for the V_{ramp} signal
12	VON TEST	Test point for the V_{on} signal
13	VCP TEST	Test point for the V_{cp} signal
14	VON RAMP TEST	Test point for the $V_{on\ ramp}$ signal
15, 16, 17	CGND	Controller ground
18	VREF	External reference voltage for adjusting output voltage DC level
19	DYN BIAS EN	Tie high to enable the dynamic-biased technique for on-time generator
20	DGND	Gate driver ground
21, 22, 23, 24, 27, 28	PGND	Power stage ground
29, 30, 31, 32, 33	VIN	Power stage input voltage
36, 37, 38, 39	VX	Power stage switching node
25, 26, 34, 35	N/A	

doi:10.6342/NTU202000925

5.2.2 Experimental Platform

The experimental platform for the buck converter with proposed control is shown in Fig. 5.6 and the measurement setup is illustrated in Fig. 5.7. The DC power supply provides the DC voltage for VIN, DVDD, CVDD, and VREF. The DC electronic load is connected to the buck converter output for setting static load. The Richtek load transient tool [16] contains a micro controller to drive a MOSFET for switching load resistors on and off, thereby creating a high slew rate dynamic load (~500ns rising/falling time). By measuring the regulator output voltage during the fast load step, the regulator control loop behavior can be observed.

The oscilloscope graphically displays the voltage and current signal over time. The waveform can then be analyzed for properties such as time interval, frequency, amplitude, average value, and others. The electronic multimeter is used to report the current consumption of the dc power supply with great precision during efficiency measurement.

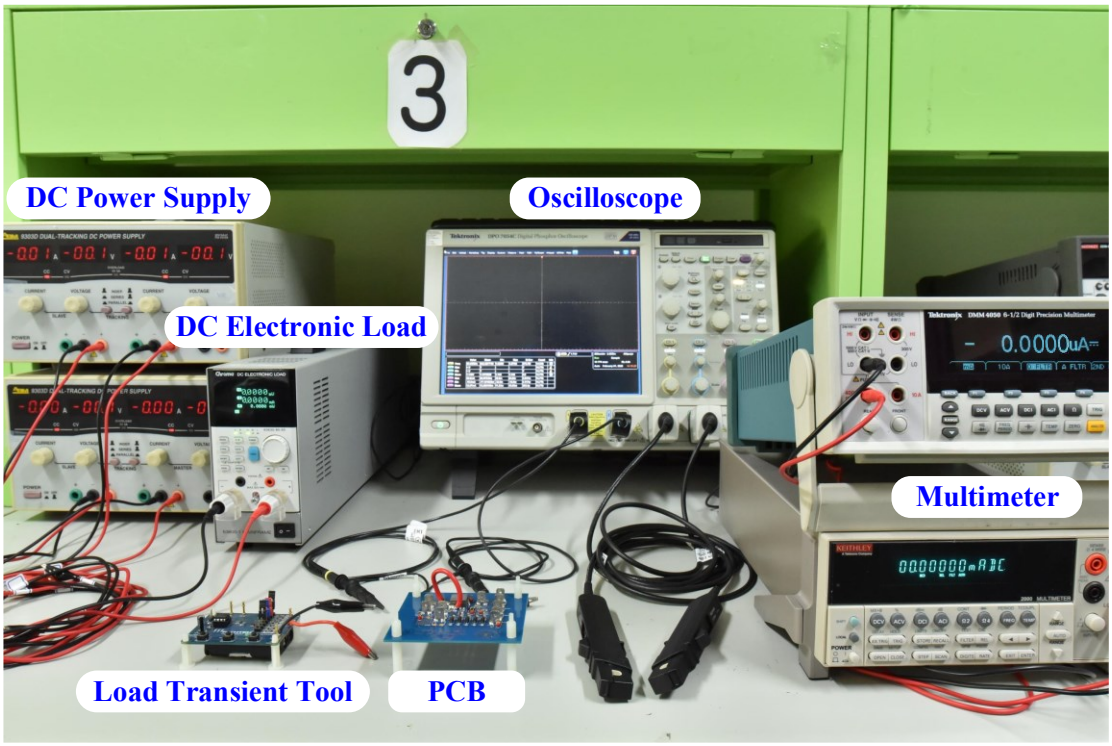

Fig. 5.6 Experimental platform

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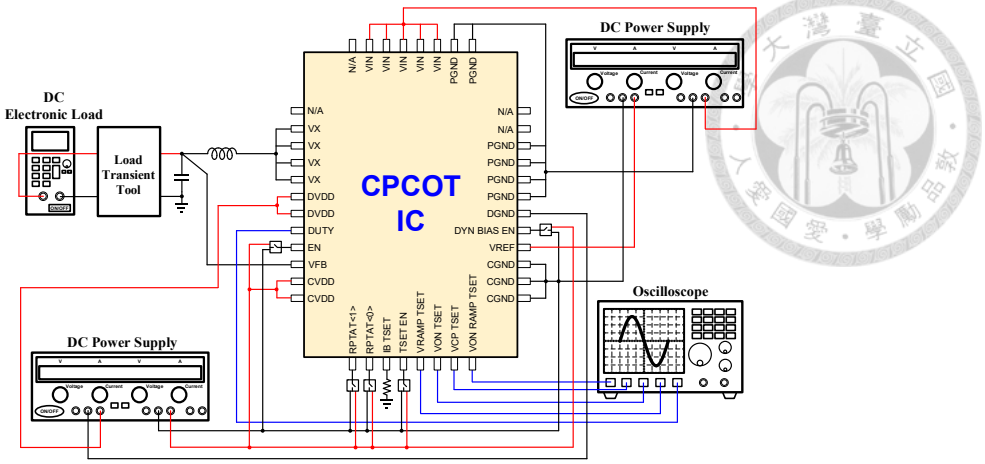


Fig. 5.7 Measurement setup

5.3 Simulation and Measurement Results

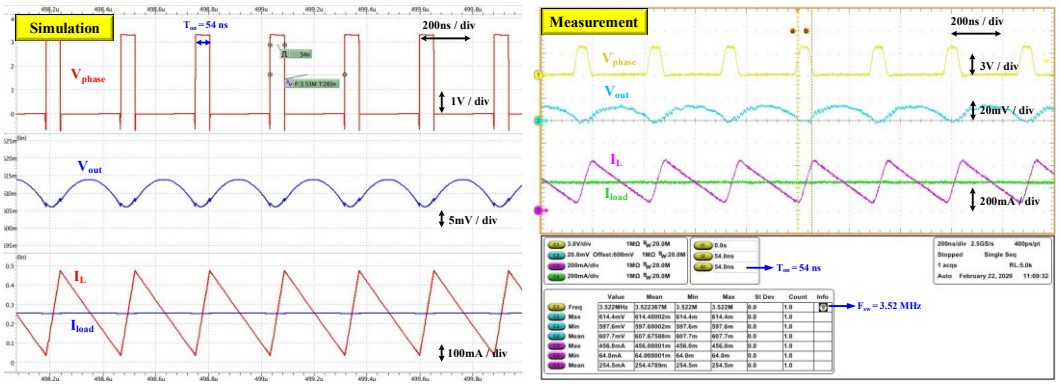
5.3.1 Steady-State Operation

Fig. 5.8, Fig. 5.9, and Fig. 5.10 show the simulated and measured waveforms of the steady-state operation under various test conditions. For the measured waveforms, the yellow line, CH1, is switching node of power stage; the blue line, CH2, is output voltage; the purple line, CH3, is inductor current; the green line, CH4, is load current. To reduce the noise in measured signals, the bandwidth limit setting is set as 20 MHz. The output voltage is measured by probing the output terminal in Fig. 5.2 instead of directly probing on the output capacitor. Thus, there is a small difference for output voltage DC level between simulated and measured waveforms due to the parasitic resistance of PCB trace. According to the figures, the output voltage and the inductor current are out of phase because of low ESR ceramic output capacitors. Even when ESR of output capacitor is reduced to 3 mΩ, the system stability is guaranteed under different working conditions due to the injection of charge-pump compensation ramp. Both simulation and measurement results show that the on-time is fixed as 54 ns during steady-state operation. However, the off-time is adjusted automatically to regulate the output voltage. Therefore, the switching frequency is varied under different duty and

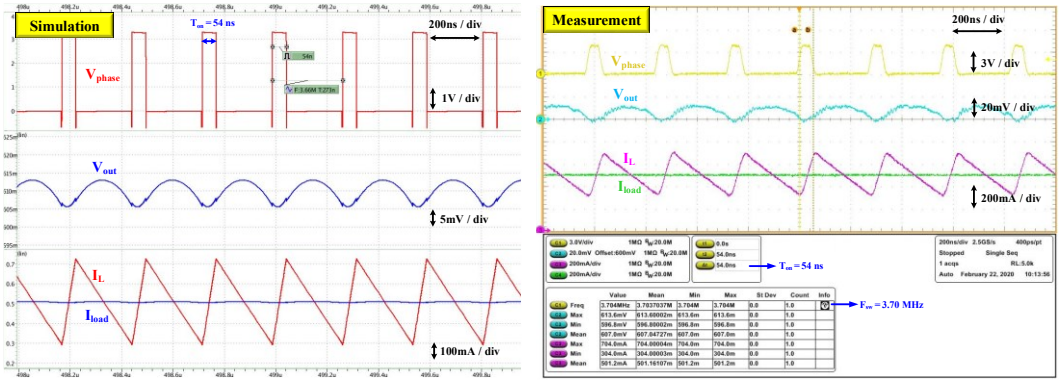
doi:10.6342/NTU202000925

loading conditions. According to [17], the switching frequency of constant on-time controlled buck converter in CCM can be expressed as (5.1), where $R_{on,P}$ and $R_{on,N}$ are the on-resistances of power PMOS and power NMOS, respectively.

$$f_{sw} = \frac{\frac{V_{out}}{V_{in}} + \frac{(R_{on,N} + R_{dcr}) \cdot I_{load}}{V_{in}}}{1 - \frac{(R_{on,P} - R_{on,N}) \cdot I_{load}}{V_{in}}} \cdot \frac{1}{T_{on}} \tag{5.1}$$



(a)



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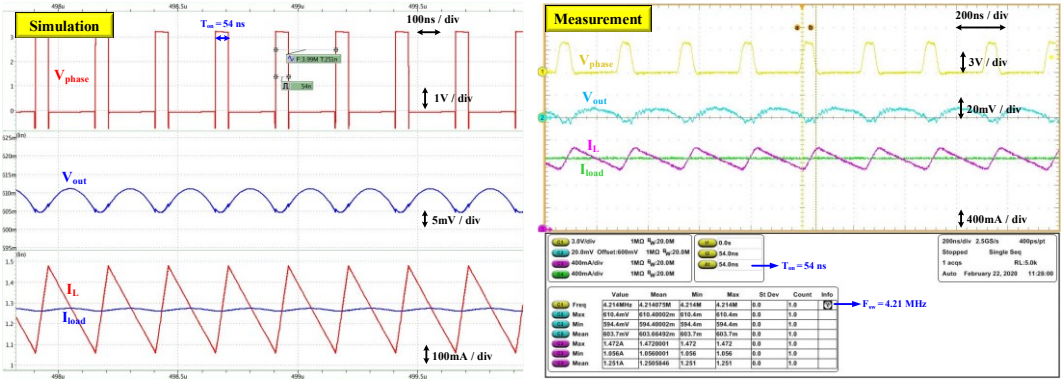

(c)

Fig. 5.8 Steady-state waveforms under V_{in} = 3.3 V, V_{out} = 0.6 V:

(a) I_{load} = 0.25 A, (b) I_{load} = 0.5 A, and (c) I_{load} = 1.25 A

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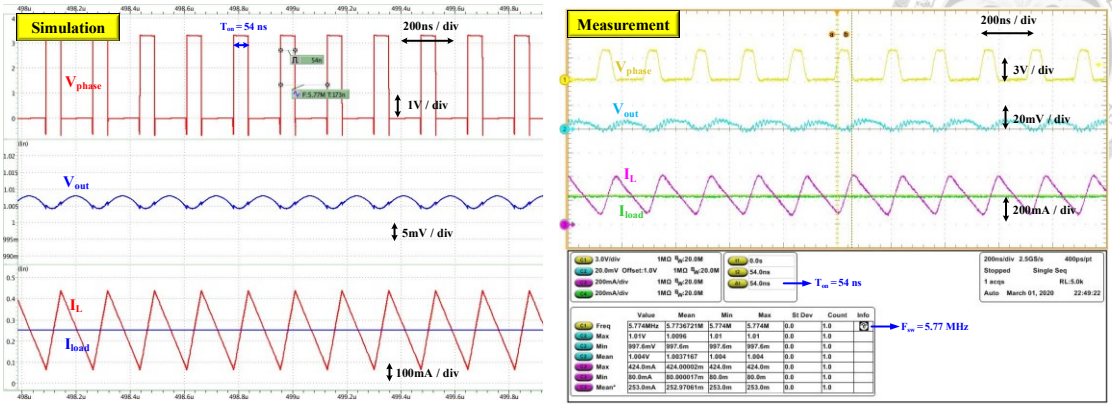
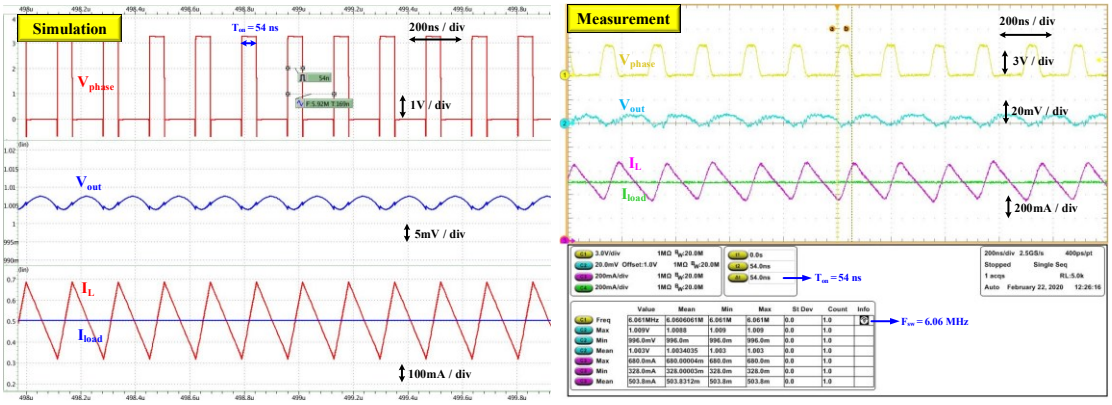
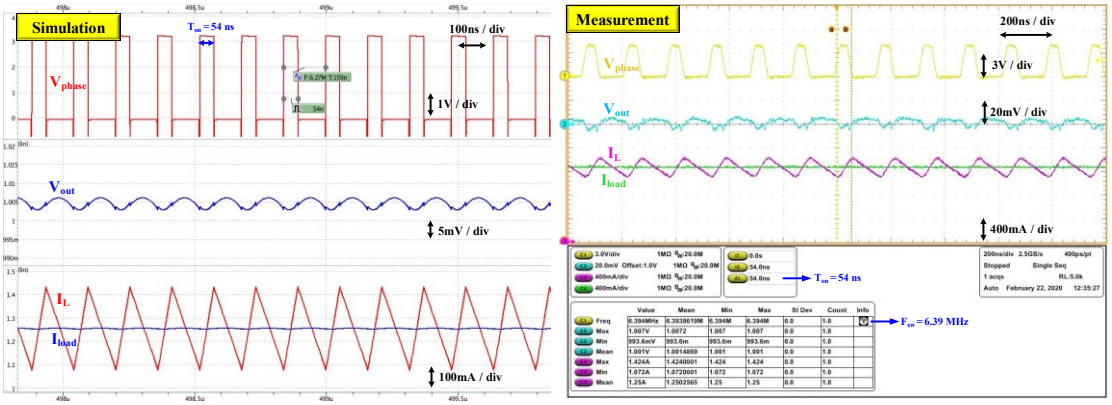


(a)



(b)

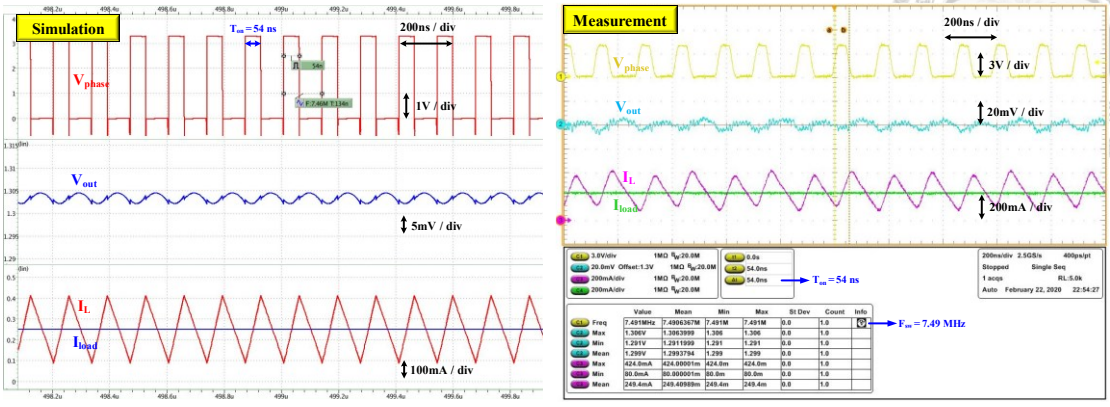


(c)

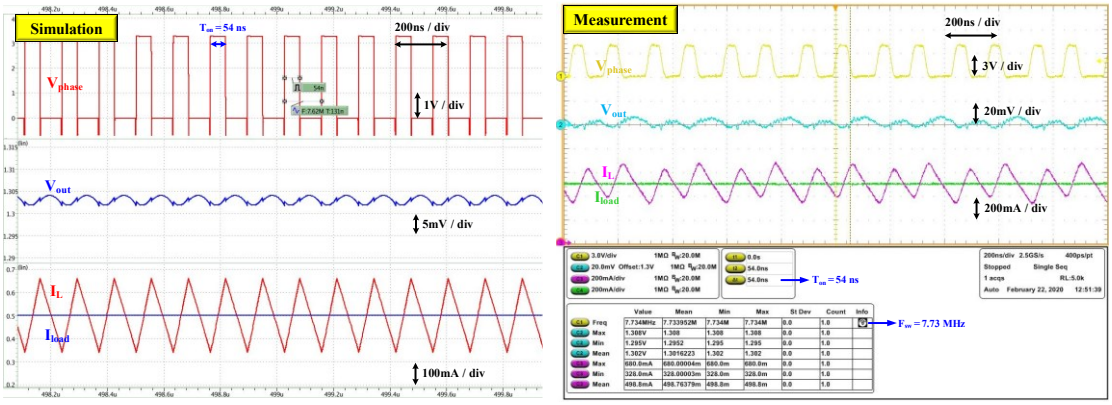
Fig. 5.9 Steady-state waveforms under V_{in} = 3.3 V, V_{out} = 1.0 V:

(a) I_{load} = 0.25 A, (b) I_{load} = 0.5 A, and (c) I_{load} = 1.25 A

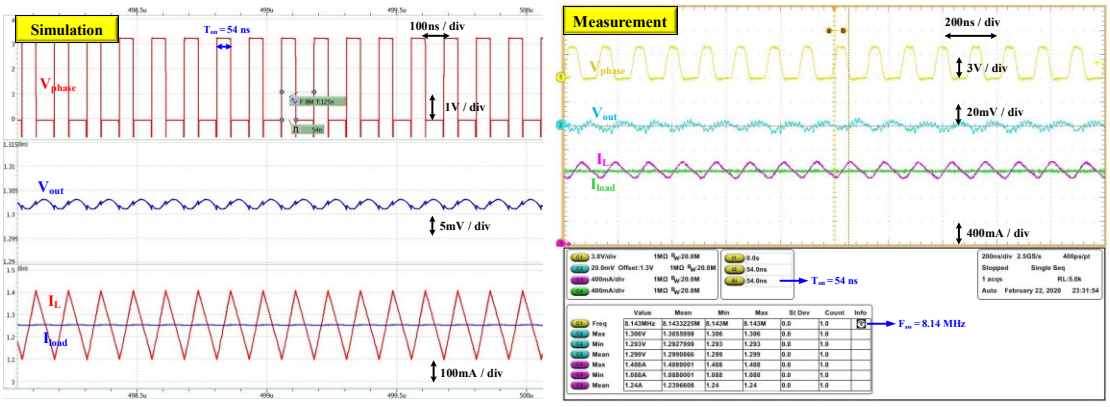
doi:10.6342/NTU202000925



(a)



(b)



(c)

Fig. 5.10 Steady-state waveforms under V_{in} = 3.3 V, V_{out} = 1.3 V:

(a) I_{load} = 0.25 A, (b) I_{load} = 0.5 A, and (c) I_{load} = 1.25 A

doi:10.6342/NTU202000925

The simulation and measurement results of on-time value and switching frequency under steady-state operation are summarized in Table 5.3 and Table 5.4.

Table 5.3 Simulation and measurement results of on-time value under steady-state operation of different working conditions

Test Conditions			T_{on}	
V_{in}	V_{out}	I_{load}	Post-Sim	Measurement
3.3 V	0.6 V	0.25 A	~ 54 ns	~ 54 ns
3.3 V	0.6 V	0.50 A	~ 54 ns	~ 54 ns
3.3 V	0.6 V	1.25 A	~ 54 ns	~ 54 ns
3.3 V	1.0 V	0.25 A	~ 54 ns	~ 54 ns
3.3 V	1.0 V	0.50 A	~ 54 ns	~ 54 ns
3.3 V	1.0 V	1.25 A	~ 54 ns	~ 54 ns
3.3 V	1.3 V	0.25 A	~ 54 ns	~ 54 ns
3.3 V	1.3 V	0.50 A	~ 54 ns	~ 54 ns
3.3 V	1.3 V	1.25 A	~ 54 ns	~ 54 ns

Table 5.4 Simulation and measurement results of switching frequency under steady-state operation of different working conditions

Test Conditions			F_{sw}	
V_{in}	V_{out}	I_{load}	Post-Sim	Measurement
3.3 V	0.6 V	0.25 A	3.53 MHz	3.52 MHz
3.3 V	0.6 V	0.50 A	3.66 MHz	3.70 MHz
3.3 V	0.6 V	1.25 A	3.99 MHz	4.21 MHz
3.3 V	1.0 V	0.25 A	5.77 MHz	5.77 MHz
3.3 V	1.0 V	0.50 A	5.92 MHz	6.06 MHz
3.3 V	1.0 V	1.25 A	6.27 MHz	6.39 MHz
3.3 V	1.3 V	0.25 A	7.46 MHz	7.49 MHz
3.3 V	1.3 V	0.50 A	7.62 MHz	7.73 MHz
3.3 V	1.3 V	1.25 A	8.00 MHz	8.14 MHz

doi:10.6342/NTU202000925

5.3.2 Load Transient Response

Fig. 5.11, Fig. 5.12, and Fig. 5.13 display the simulated and measured waveforms of the step-up load transient response under 0.6 V, 1.0 V, and 1.3 V output voltage, respectively. The step load changes from 0.25 A to 1.25 A with a slew rate of 1 A/ns for simulation and 1 A/500 ns for measurement due to the slew rate limit of Richtek load transient tool [16]. Hence, the measured performance cannot achieve 100% duty ratio with on-time extension during step-up load transient as the simulation result.

Fig. 5.11 indicates that the measured undershoot voltage is 55 mV and settling time is 1.0 μs when V_{out} is 0.6 V. Fig. 5.12 shows that the measured output voltage recovers in 1.5 μs with an undershoot of 60 mV when V_{out} is 1.0 V. Fig. 5.13 demonstrates that the measured undershoot voltage is 65 mV and settling time is 1.5 μs when V_{out} is 1.3 V. There is no ringing-back phenomenon on output voltage waveform in each case. The measurement results of step-up load transient response are very close to the simulation results, as shown in Table 5.5.

Table 5.5 Simulation and measurement results of step-up load transient response under different working conditions

Test Conditions			Undershoot		Settling Time	
V_{in}	V_{out}	I_{load}	Post-Sim	Measurement	Post-Sim	Measurement
3.3 V	0.6 V	0.25 A – 1.25 A	50 mV	55 mV	1.0 μs	1.0 μs
3.3 V	1.0 V	0.25 A – 1.25 A	55 mV	60 mV	1.5 μs	1.5 μs
3.3 V	1.3 V	0.25 A – 1.25 A	60 mV	65 mV	1.5 μs	1.5 μs

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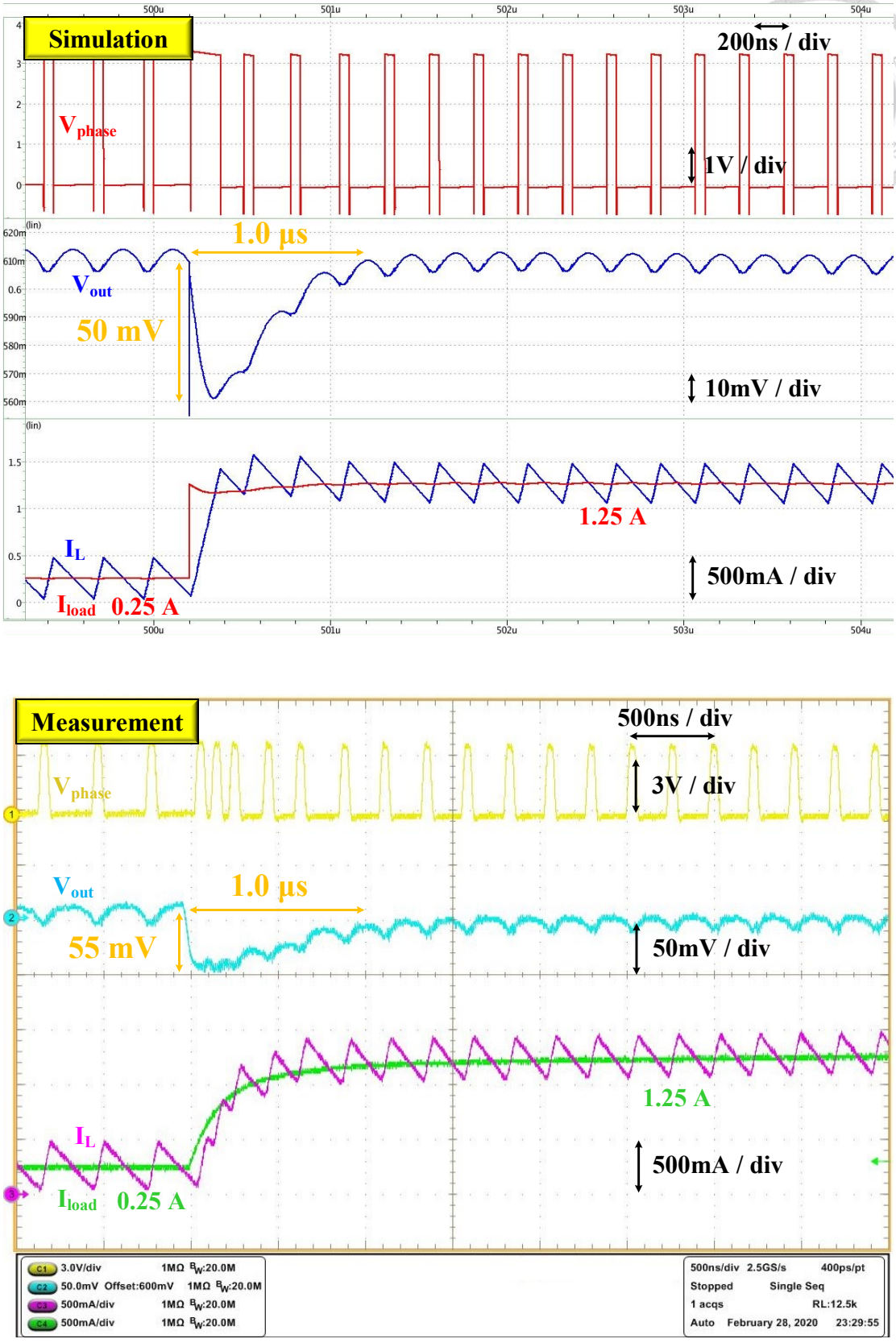

Fig. 5.11 Simulated and measured waveforms of the step-up load transient response under 3.3 V-0.6 V

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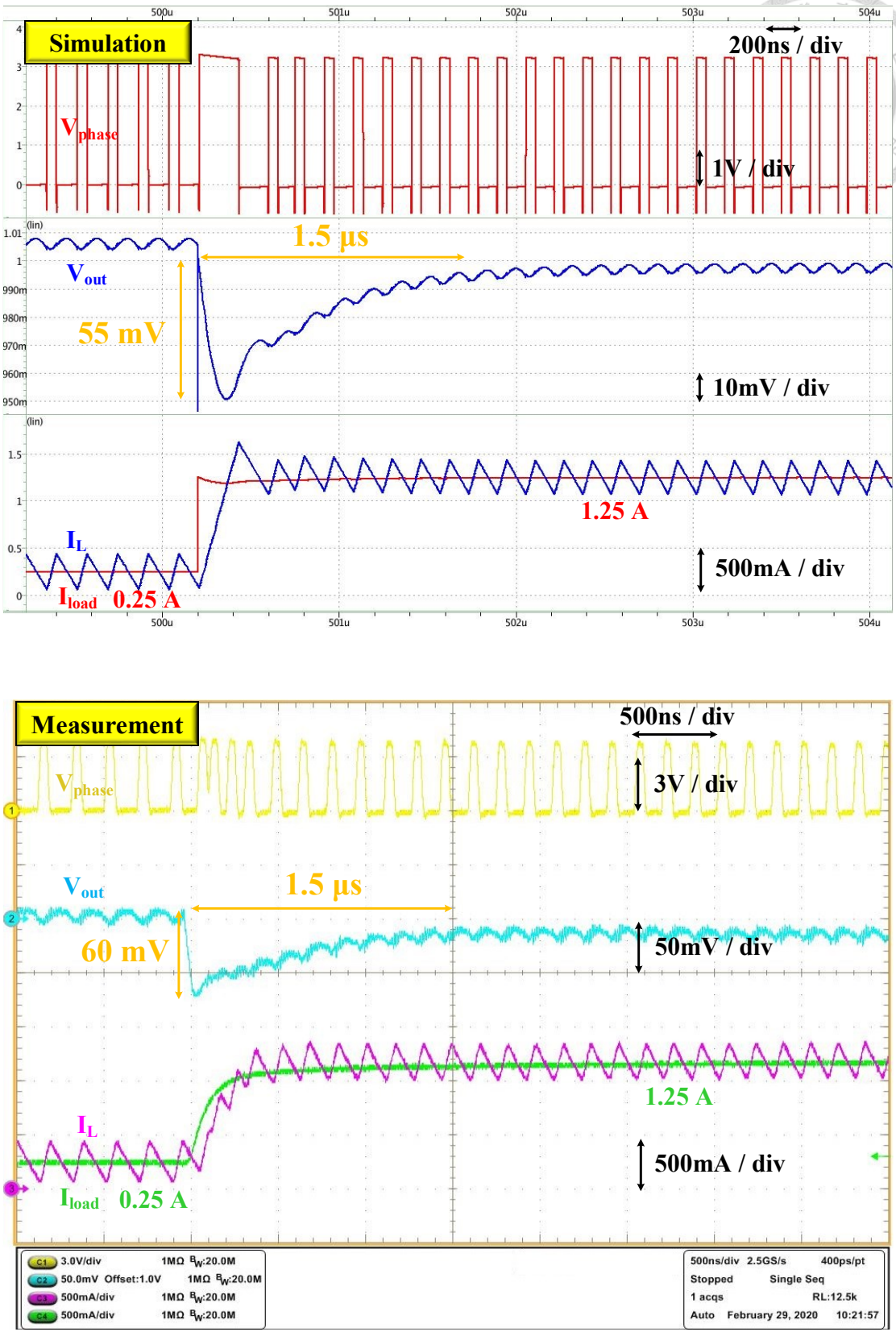

Fig. 5.12 Simulated and measured waveforms of the step-up load transient response under 3.3 V-1.0 V

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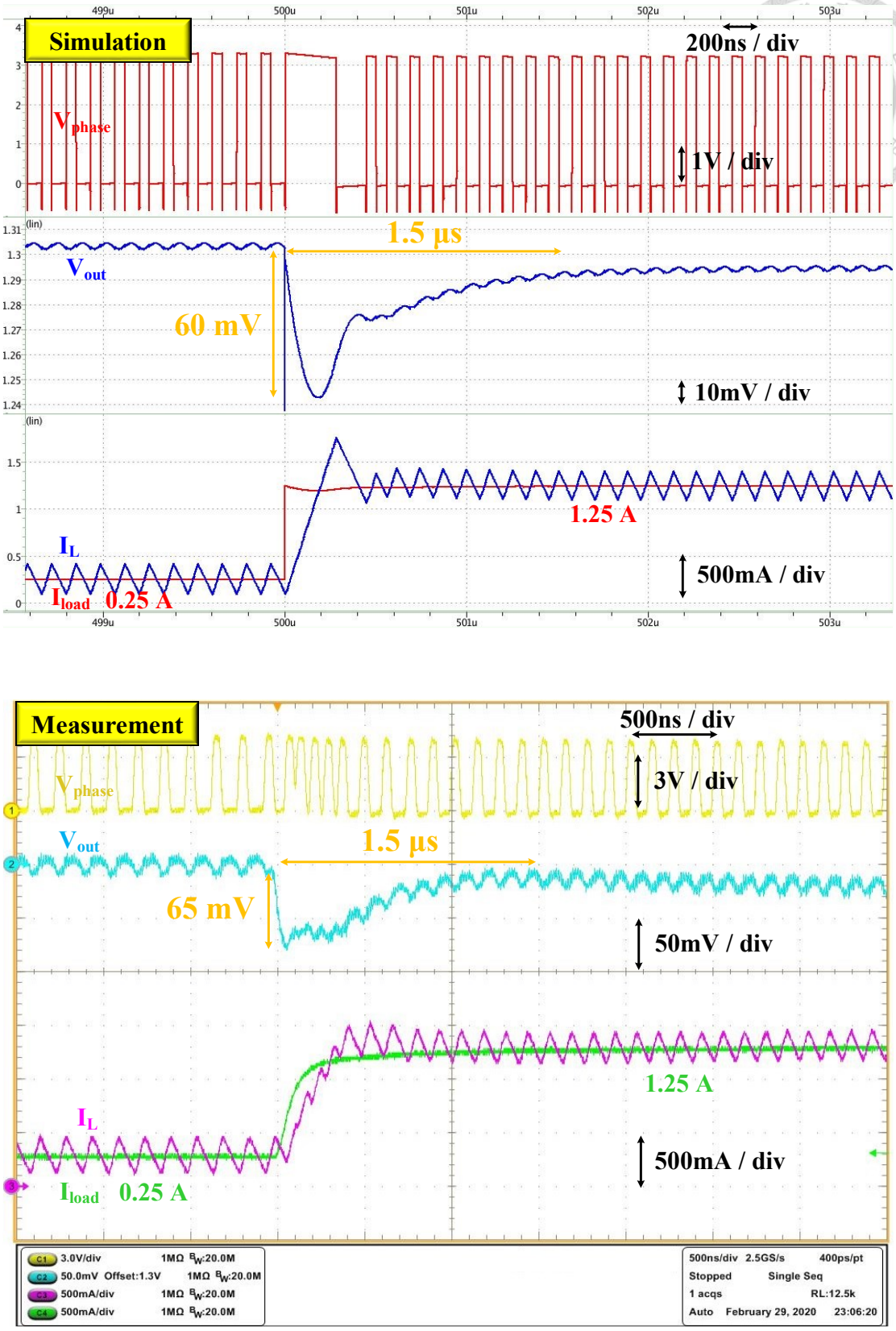

Fig. 5.13 Simulated and measured waveforms of the step-up load transient response under 3.3 V-1.3 V

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Fig. 5.14, Fig. 5.15, and Fig. 5.16 show the simulated and measured waveforms of the step-down load transient response at 0.6 V, 1.0 V, and 1.3 V output voltage, respectively. The step load changes from 1.25 A to 0.25 A with a slew rate of 1 A/ns for simulation and 1 A/500 ns for measurement due to the slew rate limit of Richtek load transient tool [16]. Fig. 5.14 displays that the measured overshoot voltage is 70 mV and settling time is 1.5 μs when V_{out} is 0.6 V. Fig. 5.15 indicates that the measured output voltage recovers in 1.5 μs with an overshoot of 80 mV when V_{out} is 1.0 V. Fig. 5.16 points out that the measured overshoot voltage is 80 mV and settling time is 2.0 μs when V_{out} is 1.3 V. The measurement results of step-down load transient response are similar to the simulation results, as shown in Table 5.6.

Table 5.6 Simulation and measurement results of step-down load transient response under different working conditions

Test Conditions			Overshoot		Settling Time	
V_{in}	V_{out}	I_{load}	Post-Sim	Measurement	Post-Sim	Measurement
3.3 V	0.6 V	1.25 A – 0.25 A	100 mV	70 mV	1.5 μs	1.5 μs
3.3 V	1.0 V	1.25 A – 0.25 A	85 mV	80 mV	1.5 μs	1.5 μs
3.3 V	1.3 V	1.25 A – 0.25 A	85 mV	80 mV	2.0 μs	2.0 μs

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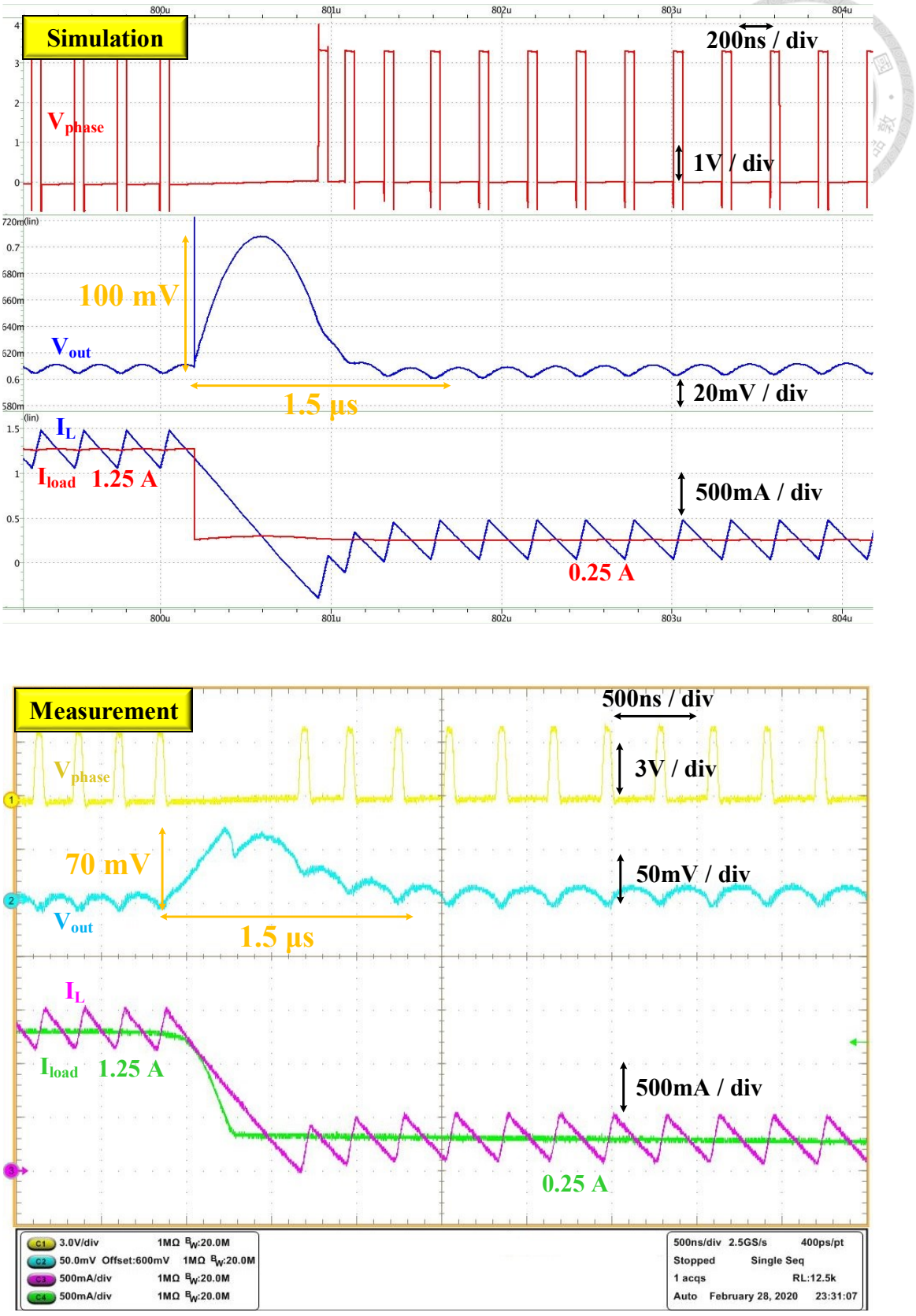

Fig. 5.14 Simulated and measured waveforms of the step-down load transient response under 3.3 V-0.6 V

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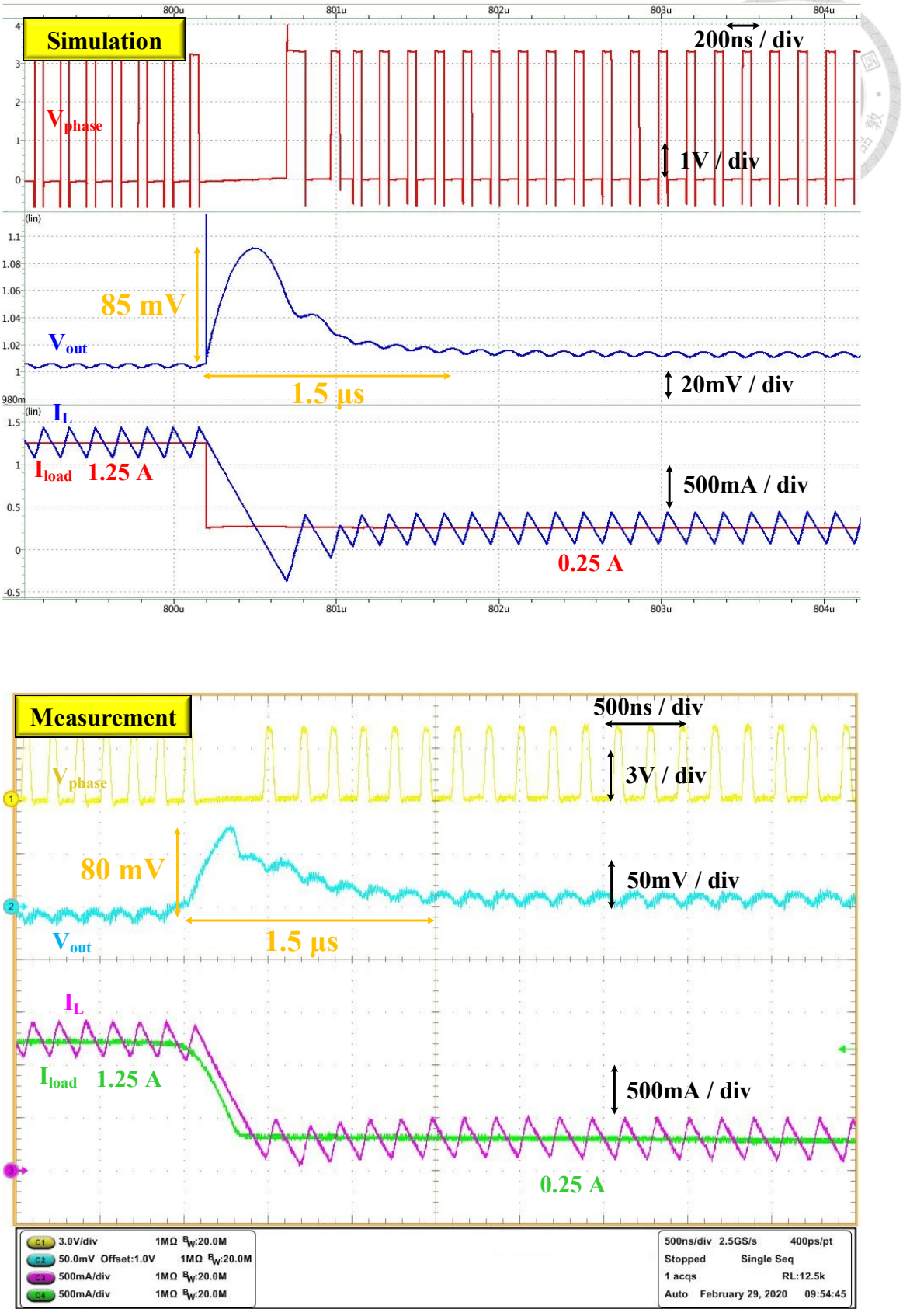

Fig. 5.15 Simulated and measured waveforms of the step-down load transient response under 3.3 V-1.0 V

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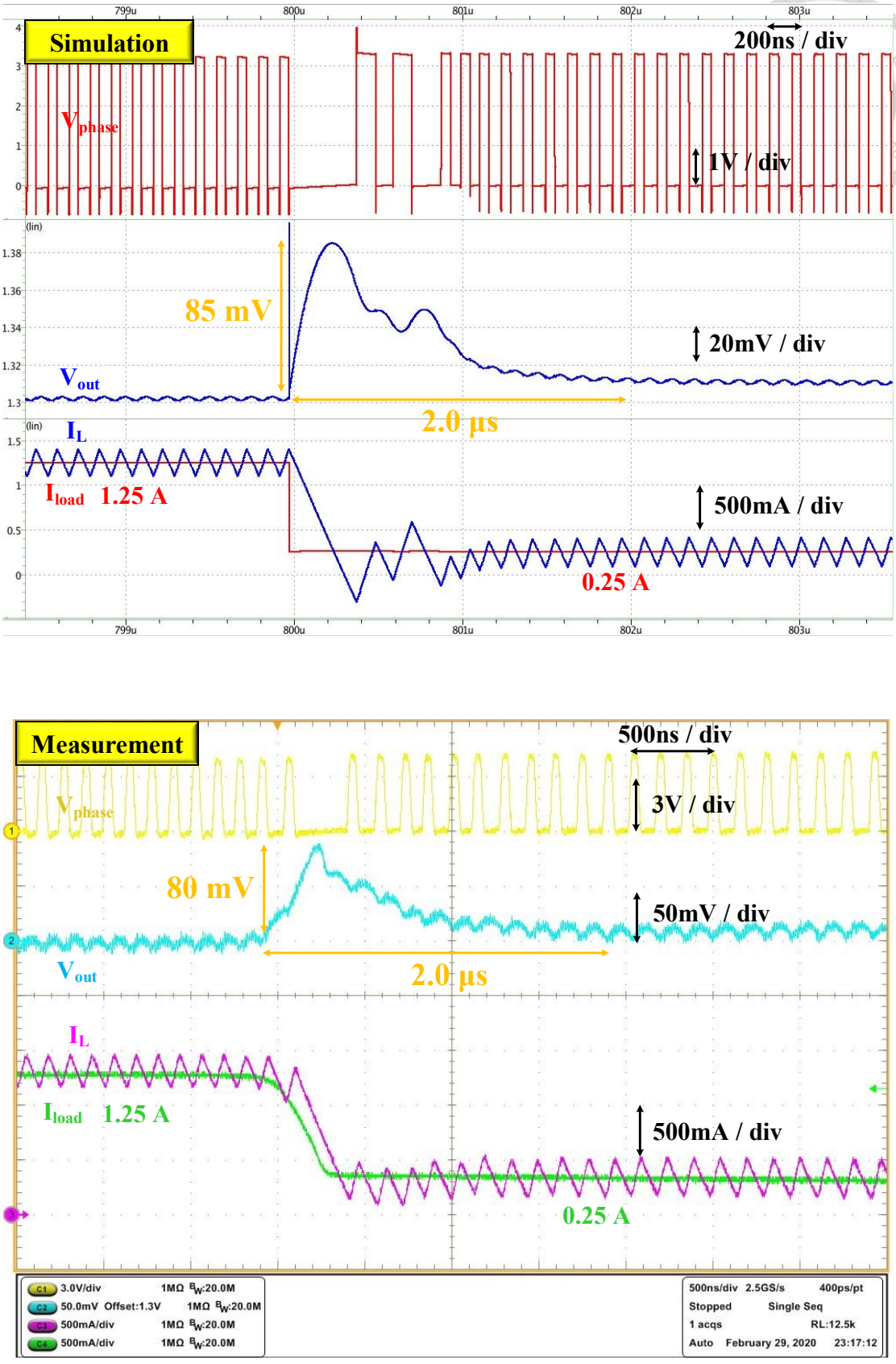

Fig. 5.16 Simulated and measured waveforms of the step-down load transient response under 3.3 V-1.3 V

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5.3.3 Dynamic-Biased Technique for On-Time Generator

Fig. 5.17 and Fig. 5.18 show the simulated and measured average current consumption of CPCOT controller with and without the proposed dynamic-biased technique. According to the simulation results, the average current consumption of CPCOT controller in a period of CCM operation is reduced from 220 μA to 199 μA, as shown in Fig. 5.17. As for the measurement results, the average current consumption of CPCOT controller in a period of CCM operation is decreased from 219 μA to 194 μA, as displayed in Fig. 5.18. Both results show that the power consumption of CPCOT controller is reduced around 10 %. Compared with traditional constant-biased method for the on-time generator, it is apparent that the proposed dynamic-biased technique can effectively reduce the quiescent current of controller to save more power loss for achieving higher efficiency.

(a)

(b)

Fig. 5.17 Simulation results of the average current consumption of CPCOT controller in CCM (V_{in} = 3.3 V, V_{out} = 0.6 V) with: (a) constant-biased mode [220 μA], and (b) dynamic-biased mode [199 μA]

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(a)

(b)

Fig. 5.18 Measurement results of the average current consumption of CPCOT controller in CCM (V_{in} = 3.3 V, V_{out} = 0.6 V) with: (a) constant-biased mode [219 µA], and (b) dynamic-biased mode [194 µA]

5.3.4 Efficiency Plot

Fig. 5.19 shows the efficiency plot of the proposed CPCOT controlled buck converter as the load current ranges from 0.25 A to 1.25 A at V_{in} = 3.3 V and V_{out} = 1.0 V. The measured peak efficiency is 85.80 %, occurring when I_{load} = 0.5 A. According to the brief summary of some common power loss equations for buck converter shown in [18], the calculated efficiency should consider the power MOS conduction loss, ESR conduction loss, DCR conduction loss, power MOS switching loss, and the gate drive loss. In this thesis, the inductor loss and the controller power loss are also taken into consideration during calculation. Therefore, the difference between the measured and calculated efficiency may come from the PCB parasitic effect due to nonoptimized board layout.

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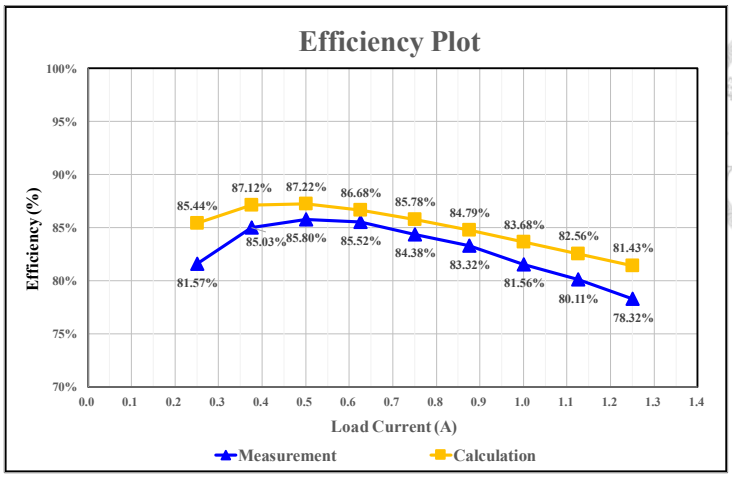

Fig. 5.19 Efficiency plot of the proposed CPCOT controlled buck converter

5.4 Comparison with Previous Published Works

Table 5.7 lists a performance comparison with other state-of-the-art single-phase buck converters [19]-[23]. Compared with other previous published works, the measurement results of the proposed CPCOT controlled buck converter achieve highest switching frequency and provide widest range of the output voltage. In addition, it can be seen that the external inductor and capacitor of the proposed buck converter are the smallest due to high switching frequency operation.

Table 5.7 Performance comparison with other state-of-the-art single-phase buck converters

		This Work	[18] 2019 TPE	[19] 2019 TIE	[20] 2018 TPE	[21] 2018 JSSC	[22] 2013 TPE
Control Scheme		COT + Charge-Pump Ramp	COT + Active Ripple Compensation	AOT + PLL	AOT + Ripple Reshaping Technique	Quasi-V^2 + Time Domain Controller	AOT + Load Current Correction Technique
Process		0.18 µm	0.5 µm BCD	0.35 µm	28 nm	0.35 µm	0.35 µm
Inductor		330 nH	2.2 µH	4.7 µH	1 µH	2.2 µH	4.7 µH
Output Capacitor		1.8 µF	88 µF	10 µF	4.7 µF	4.7 µF	8.9 µF
Input Voltage		3.3 V	4.5 - 30 V	3.0 - 3.7 V	2.6 - 3.63 V	3.3 V	3.3 - 4.2 V
Output Voltage		0.6 - 1.3 V	1.05 V	1.2 - 1.8 V	1.05 V	1.5 - 1.8 V	1.2 V
Load Range		0.25 - 1.25 A	0 - 4.0 A	0 - 0.7 A	0.3 - 1.7 A	0.025 - 0.7 A	0.005 - 0.8 A
Switching Frequency		3.52 - 8.14 MHz	0.35 - 1 MHz	1 MHz	2.5 MHz	1.97 - 2.02 MHz	0.75 MHz
Min. Output Ripple		8 mV	8 mV	45 mV	6 mV	3 mV	10 mV
Peak Efficiency		85.8 %	97 %	90 %	94 %	92 %	86.6 %
Chip Area (with PADs)		1.12 mm^2	N/A	1.97 mm^2	2.5 mm^2	0.913 mm^2	1.90 mm^2
Light-to-Heavy Load Transient Response	I_{load} Step (Rise Time)	0.25 - 1.25 A @V_{out} = 1.0 V (~ 500 ns)	0.4 - 3.2 A @V_{out} = 1.05 V (~ 10 µs)	0.1 - 0.5 A @V_{out} = 1.8 V (~ 2 µs)	0.3 - 1.7 A @V_{out} = 1.05 V (N/A)	0.17 - 0.68 A @V_{out} = 1.7 V (N/A)	0.15 - 0.65 A @V_{out} = 1.2 V (~ 2 µs)
	V_{out} Droop (% of V_{out})	60 mV (6.00 %)	25 mV (2.38 %)	200 mV (11.11 %)	75 mV (7.14 %)	38 mV (2.24 %)	53 mV (4.42 %)
	Settling Time	1.5 µs	28 µs	0.96 µs	4 µs	2.5 µs	3 µs

doi:10.6342/NTU202000925

Chapter 6 Conclusions and Future Works

6.1 Conclusions

In recent years, ripple-based constant on-time (RBCOT) control has been more and more popular in industry products due to features of simple implementation, high light-load efficiency and fast transient response. In many applications such as laptop, cell phone and other portable devices, low ESR capacitors such as multilayer ceramic capacitors are preferred due to small size and small output voltage ripple requirement. However, for the buck converters with low ESR output capacitors, the conventional ripple-based constant on-time control may suffer from the subharmonic oscillation due to the lagging phase of the capacitor voltage ripple relative to the inductor current ripple.

In this thesis, a charge-pump constant on-time (CPCOT) control scheme is proposed to solve the subharmonic issue without any current sensing or direct voltage detecting technique. Consequently, compared with previous ramp compensation methods [6]-[9], the proposed method reduces the complexity of circuit implementation. Besides, the proposed CPCOT control can achieve fast transient response and good light load efficiency, which are the inherent advantages of RBCOT control scheme. A dynamic-biased technique for on-time generator is also proposed to reduce quiescent current of the controller.

To thoroughly investigate the characteristics of the proposed CPCOT control scheme, a complete small-signal model of the CPCOT controlled buck converter in CCM operation was derived based on the describing function (DF) technique. According to the analysis of the small-signal model, the design guidelines for the charge-pump compensation ramp is obtained from both stability margin and transient performance points of view.

The proposed CPCOT control scheme and dynamic-biased technique were

doi:10.6342/NTU202000925

implemented into integrated circuit (IC) for a buck converter using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm CMOS process with a chip area of 1.12mm^2. The circuit structure and implementation of the three main sub-blocks, including the modulation comparator, dynamic-biased on-time generator, and charge-pump ramp generator, are described in this thesis.

Finally, both simulation and experiment results are given to verify the proposed concepts. This converter can produce adjustable output voltage from 0.6 V to 1.3 V and supply load current from 0.25 A to 1.25 A while the input voltage is 3.3 V. The stability of the proposed buck converter is guaranteed under the working conditions described above. According to simulated and measured waveforms, the on-time is fixed as 54 ns during steady-state operation, and the switching frequency is up to 8 MHz. The experimental results of load transient response are very similar to the simulation results. In addition, both simulation and experiment results show that the power consumption of CPCOT controller is reduced around 10 % due to the proposed dynamic-biased technique for the on-time generator. The measured peak efficiency of the proposed buck converter achieves 85.80 %, occurring when V_{in} = 3.3 V, V_{out} = 1.0 V, and I_{load} = 0.5 A.

doi:10.6342/NTU202000925

6.2 Future Works

1. Since the proposed CPCOT control scheme is a clock-free architecture, it suffers from significant steady-state switching frequency variation when the input voltage, output voltage, and the load current are changed. In other words, a power converter with CPCOT control scheme may become a frequency interference source, which degrades the performance of surrounding analog circuits through electromagnetic interference (EMI). The switching frequency variation can be suppressed by adding an adaptive on-time mechanism to dynamically adjust the on-time duration based on the input voltage, output voltage, and load current. Therefore, the proposed converter can keep approximately constant switching frequency during its static operation which minimizes the EMI at some sensitive bands of certain frequencies in the system.
2. It is known that the switching frequency of RBCOT controlled buck converter in DCM operation is proportional to the output loading condition I_{load}, which is similar to the pulse frequency modulation (PFM) control. To reduce the switching power loss for high efficiency in DCM operation, adding DCM operating mechanism to the proposed CPCOT control architecture is necessary. As a result, it can retain the inherent advantage of RBCOT control scheme in DCM operation to achieve good light-load efficiency. As such, the proposed CPCOT control method could be more suitable for the recent portable electronics because of its power-saving ability under light-load operation.
3. For a given setting of input voltage, output voltage and output load current, there is an optimal design for the charge-pump compensation ramp. However, for the PMIC applications nowadays, a buck converter must be able to cover the wide-range operation. Therefore, how to design the charge-pump compensation ramp to

doi:10.6342/NTU202000925

achieve converter stability and optimal load transient performance under different working conditions is an interesting topic for future investigation.

4. In this thesis, the small-signal model of the proposed CPCOT controlled buck converter operated in continuous conduction mode had been derived based on the describing function methodology and verified by SIMPLIS simulation tool. The experiment is also expected to be conducted to verify the derived reference-to-output and output impedance transfer functions.

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