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原子層成長氧化層/砷化鎵之介面特性研究

Interfacial Electrical Properties of Y_2O_3/GaAs and Al_2O_3/GaAs MOS capacitors

張從文

Tsung-Wen Chang

指導教授： 洪銘輝 博士

郭瑞年 博士

Advisor：Minghwei Hong, Ph.D.

Raynien Kwo, Ph.D.

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摘要

因為相對高的電子遷移率，砷化鎵被視為取代矽基材的重要材料，因為其和矽相對小的晶格差，而被廣泛的研究。同時，原子層沉積由於其相當好的覆蓋性以及成長速度控制，也已經被產業廣泛的使用。

和產業上使用矽和二氧化矽之介面不同，砷化鎵和高介電係數氧化層很難維持良好的介面特性，因此電容電壓量測下，頻率分散是很常見的現象，此篇論文致力於研究邊界缺陷和介面缺陷在不同氧化層在砷化鎵上的行為。頻率分散主要由於穿隧效應去和半導體載子進行交換，因次對溫度不應該有響應。然而在多數報導中，頻率分散對溫度的響應均被觀測到。

本實驗使用原子層沉積氧化鋁和氧化釔成長在砷化鎵上，量測電容電壓、電容頻率、電導電壓、電流電壓及准靜態電容電壓等方式分析介面缺陷和邊界缺陷在電性上的表現。從中的分析可以得知，氧化釔以及砷化鎵顯示相當良好的介面特性，相反的氧化鋁以及砷化鎵的介面態位密度則相當高。同時在變溫量測時，頻率分散在氧化釔以及砷化鎵的電壓電容特性隨著溫度改變，經過模擬和實驗的比較可以得知，此現象無法以已經被發表之隨溫度變化的缺陷截面積解釋。本論文提出嚴謹的計算及模擬顯示出此現象應歸因於隨溫度變化的氧化釔砷化鎵能量差，成功的解釋了隨溫度變化的頻率分散。

關鍵字：頻率分散、砷化鎵、氧化釔、邊界缺陷、氧化鋁。

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Abstract

Due to the relatively high electron mobility, GaAs and InGaAs are the leading candidates as n-channel materials in post-Si generation. $In_{0.53}Ga_{0.47}As$ inversion channel n-MOSFETs have been demonstrated promising device performance using atomic-layer-deposited (ALD) high-k dielectrics. [1] However, a lattice constant of 5.87Å of $In_{0.53}Ga_{0.47}As$ is difficult to be integrated onto the platform a Si(001) wafer. Instead, GaAs, with a lattice constant of 5.65Å, is about half of the lattice mismatch between $In_{0.53}Ga_{0.47}As$ and Si. Owing to the advantages mentioned above, GaAs and low-In content InGaAs metal-oxide- semiconductor (MOS) capacitors have been intensively studied, aiming for developing high speed and low power devices. Besides, with excellent uniformity and conformal coverage in nanometer thick film growth, atomic layer deposition (ALD) has been widely employed in depositing high-k dielectrics for MOSFETs since the 45 nm node. Therefore, as an urgent issue, intensive efforts in ALD high-k dielectrics on GaAs(001) have been carried out to characterize and perfect these interfaces.

Frequency dispersion (FD) is an important index for characterizing oxide-semiconductor interfaces. ALD-oxides on GaAs usually give a large FD in capacitance-voltage (CV) curves of the MOS capacitors (MOSCAPs), particularly on n-GaAs. [2,3] Research efforts have been carried out to explain the origin of the large FD in oxides/(In)GaAs interfaces. A model assuming an exponentially decaying spatial distribution of traps from the oxide/semiconductor interface into the bulk oxide layer explained the large FD of CVs at accumulation by the interfacial traps. [4] However, this model failed to explain the dispersion in the low frequency range and the temperature-dependent dispersion. Later, a distributed border trap model based on tunneling

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mechanism between the oxide/semiconductor interface and the trap states in gate dielectric accounted for the large FD of CVs and conductance (GV) at accumulation. [5] Also, Chen et al combined these two models to fit the CV and GV characteristics in depletion region to inversion region. [6] However, most reported high-k/III-V systems yielded high trap densities up to 10^{13} $eV^{-1}cm^{-2}$ as well as undesired interfacial native oxides, such that the corresponding analyses on capacitance-frequency (CF) characteristics lead to unconvincing results. [7,8] The very few high-k/GaAs(001) hetero-structures reported with low interfacial trap densities (D_{it}'s) are ultra-high vacuum (UHV) e-beam evaporated $Ga_2O_3(Gd_2O_3)$ and ALD-Y_2O_3 on GaAs(001). [9]

In the thesis, Al_2O_3 and Y_2O_3 were atomic-layer-deposited (ALD) on molecular beam epitaxy grown GaAs-(4×6). Oxide capacitance was carefully extracted by consider the accumulation layer thickness in GaAs. The oxide/semiconductor interface were characterized using CV characteristic, CF characteristic, QSCV measurement and conductance method. The CF analyses are in agreement with the conclusions given by QSCV and GV measurements for both hetero-structures. Both systems exhibit similar border trap densities, but greatly different D_{it}*'s*. Moreover, the D_{it} spectrum without mid gap peak is observed in Y_2O_3/GaAs samples. Showing low density of states below $10^{12}cm^{-2}eV^{-1}$, Y_2O_3/GaAs hetero-structure is promising for achieving inversion channel MOSFET with subthreshold swing under 75mV/dec. Another important issue discussed in the thesis is the temperature dependence frequency dispersion. After the simulation, the observed temperature dependence of frequency dispersion pointed out a temperature dependent barrier height, which is further confirmed by J-E characteristic. We concluded that the barrier height is temperature dependent, and should be extracted by electrical measurement. Moreover, the commonly observed temperature dependent frequency

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dispersion result from the temperature dependent barrier height (tunneling attenuation coefficient). Thus, the border trap density should be plotted with the right barrier height.

Keyword: GaAs, Y_2O_3, Al_2O_3, border traps, frequency dispersion

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1. Introduction

1.1 Background

In the past 40 years, SiO_2/Si has served as the transistor gate dielectric and channel materials in Si CMOS technology. Aiming for higher speed, lower power consumption and higher transistor density, the Si CMOS technology is kept scaling down. The so called "Moore's Law" was observed and described the in by Gordon E. Moore in 1965 as shown in **Fig 1-1**. SiO_2 thickness has been scaling down at 0.7 per generation until 130nm nodes, as at 90nm and 65nm nodes the SiO_2 ran out of atoms. The scaling of SiO_2 gate dielectric thickness suffers from large gate leakage. To keep Moore's Law, the semiconductors industry face unavoidable challenge to find an alternative dielectric to replace SiO_2. The gate leakage current is related to the physical thickness of gate oxide, while the capacitance is proportional to dielectric constant divided by gate oxide thickness. Therefore, the semiconductor industry search for an alternative insulting material with a higher relative dielectric constant to replace SiO_2. Note that the material have to be compatible with CMOS technology and high thermal stability and low density of states in contact with channel material Silicon.

Owing to the high dielectric constant, the HfO_x based high-κ became the leading candidates for replacing the long-standing SiO_2. HfO_2 benefit from forming stable

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interfacial layer of SiO_x and $HfSiO_x$ with Si, and exhibit good interface with Si. However, Fermi-level pinning occurs at HfO_x-poly-Si gate. To avoid the Hf-Si bonds, The doped poly-Si gate is replaced by metal gate to prevent poly-Si gate depletion. [10] In 2007, Hf-based oxide as gate dielectric and metal gate has been employed in Intel's 45nm node, which is the demonstration of working 45nm processor integrating high-k with metal gate. The breakthrough of HKMG technology has helped to continue the scaling down of semiconductor industry.

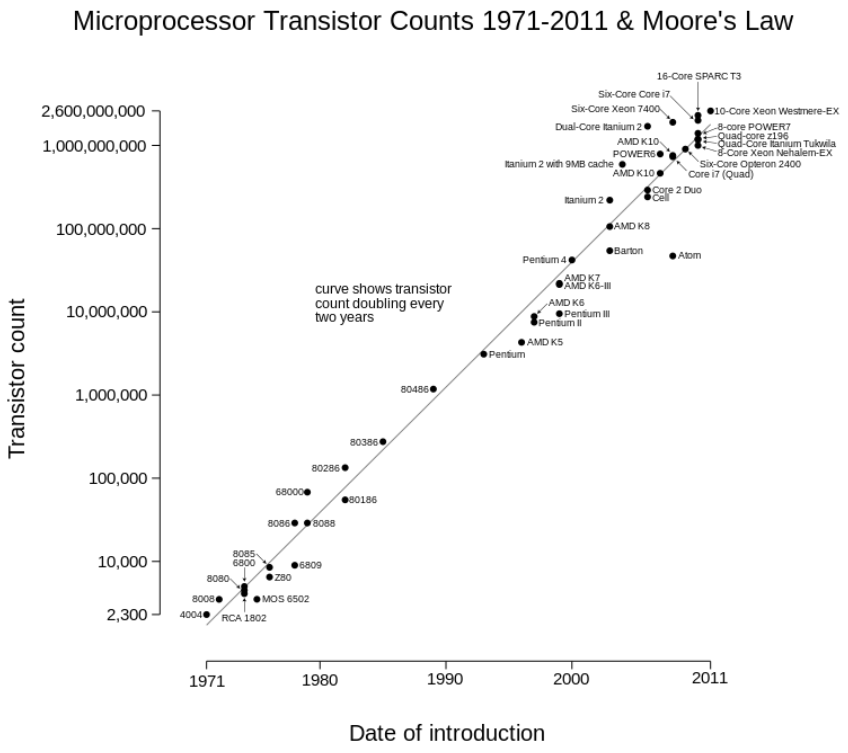

Fig 1-1 The Moore's Law of CPU transistor counts against dates of introduction; note the logarithmic vertical scale; the line corresponds to exponential growthwith transistor count doubling every two years.

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1.2 Ultimate CMOS: III-V compounds

For ultimate CMOS, the performance cannot be simply fulfilled by using Si as channel material even with HKMG technology. The drive current in saturation region of MOSFET can be simply expressed by $I_{Dsat}=W_gQ\mu E$, where W_g is the gate width, Q is the surface charge, μ is the carrier mobility. Compared to Si channel, III-V compounds possess high electron or hole mobility for future MOS transistor application as shown in **Table 1-2**. $In_{0.53}Ga_{0.47}As$ and GaAs with more than five times larger electron mobility than Si, is promising for high speed and high performance MOS device. Owing to high electron mobility and direct band gap, GaAs and InGaAs has been leading candidates to replace long-standing Si channel.

To replace the Si channel in Si CMOS technology, there are serval challenges must be overcome as follows. (1) Small lattice mismatch with Si for integration with mature Si CMOS technology. (2) Thermal stability interface with high dielectric constant oxides compatible with CMOS process. (3) Low interfacial density of states with high dielectric constant gate dielectric. (4) Suitable band gap to avoid short channel effect such as band-to-band tunneling. Therefore, GaAs is outstanding in III-V compounds with only 4% lattice mismatch with Si, 8500cm^2/V-s electron mobility and 1.424eV band gap energy. Although $In_{0.53}Ga_{0.47}As$ has extremely high electron mobility of 12000 cm^2/V-s, but large

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lattice mismatch with Si and small band gap energy is not suitable for future CMOS technology.

Over 40 years, the excellent Si/SiO_2 interface is the backbone of semiconductor industry. The ability to continuous downscaling of the dimension of Si-based MOSFET is attributed to SiO_2's superior electrical and material properties. Which are low leakage current, ultra high thermal stability and low interfacial traps with Si. To replace the Si channel with III-V compounds, the excellent interfacial properties is required.

Table 1-1. List of electrical and basic parameter of semiconductors.

	symbol	**Si**	**Ge**	**GaAs**	**InAs**	**$In_{0.53}Ga_{0.47}As$**	**unit**
Dielectric constant	κ	11.7	16.2	12.9	15.15	13.9	-
Band gap energy	E_g	1.12	0.661	1.424	0.354	0.74	eV
Intrinsic carrier concentration	n_i	1×10^{10}	2×10^{13}	2.1×10^{6}	1×10^{15}	6.3×10^{11}	cm^{-3}
Electron mobility	μ_e	1400	3900	8500	40000	12000	$cm^2/V\text{-}s$
Hole mobility	μ_h	450	1900	400	500	300	$cm^2/V\text{-}s$
Electron effective mass	m^*_e	$0.98m^*$	$1.6\ m^*$	$0.063\ m^*$	$0.023\ m^*$	$0.041m^*$	-
Hole effective mass	m^*_h	$0.49\ m^*$	$0.33\ m^*$	$0.51\ m^*$	$0.41\ m^*$	$0.45\ m^*$	-
Lattice mismatch with Si		0%	4.17%	4.08%	11.55%	8.06%	

1.3 High-k dielectric on GaAs

Unlike the case of SiO_2 on Si, the native oxide of GaAs are not stable and leaky. Different methods and treatments have been adopted to oxidize GaAs surface, including

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thermal, anodic, and plasma oxidation of GaAs. [11] But, the As_2O_3 and As_2O_5 on GaAs surface cause the Fermi-level pinning at the interface. The first encouraging result to unpin GaAs Fermi-level is Gadolinium Oxide on GaAs. Lateral, different kinds of high-κ dielectric on GaAs had been reported, including La_2O_3, Y_2O_3 and HfO_2 on GaAs. Among all the reported works, large mid-gap Dit(E) peak > $10^{13}cm^{-2}eV^{-1}$ and large frequency dispersion in capacitance-voltage measurement is still observed.

To find a suitable gate dielectric on GaAs, serval different high-k material are listed as **Table 1-2**. Aiming for high performance MOS device, the high-κ/GaAs hetero-structure should have some critical properties. Sufficient valance band offset and conduction band offset between high-κ material and GaAs is necessary to prevent gate leakage under large bias. In **Table 1-3**, great potential of rare-earth oxide is presented with high dielectric constant and enough band offset.

Table 1-2. List of common used dielectric properties

Dielectric	SiO_2	Al_2O_3	HfO_2	Gd_2O_3	Y_2O_3	La_2O_3
Dielectric constant κ	3.9	9	20	14	20	30
Band gap (E_g)	8.9	8.7	5.7	5.8	5.8	4.3
Conduction band offset with GaAs (eV)	3.3	3.2	1.5	1.55	2.2	2.4
Valance band offset with GaAs (eV)	4.2	4.1		2.85	2.1	0.5

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1.4 Frequency dispersion and border traps analysis

It is well-known that the traps level inside semiconductor bandgap can reduce the device performance and cause Fermi-level pinning. The subthreshold swing will reflect the density of states inside GaAs bandgap. Therefore, lots of characterization methods have been developed in order to probe the trap density inside GaAs bandgap. But, with low conduction band density of states, the traps inside conduction band could drastically reduce GaAs based n-MOSFET performance. The traps inside conduction band could result in insufficient mobility far from theory prediction and low inversion channel concentration. So, we are looking forward to characterize the traps inside the conduction band. Some reliable results have been carried out to probe the traps inside conduction band. For example, split C-V and Hall measurement have been measured, and the difference between two measurements is attributed to traps response. [12] The distribution of *Dit* inside the conduction band was then evaluated by combining the split C-V method and Hall measurement. However, the fast traps and slow traps cannot be distinguished using the above method. Fortunately, the frequency dispersion at accumulation in C-V measurement can provide us some useful information.

Frequency dispersion (F. D.) in C-V measurement arise when trap states can communicate with semiconductors energy band. Therefore, F. D. is used for

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oxide/semiconductor interfacial properties characterization. Unlike the ideal C-V characteristic of SiO_2/Si case free from frequency dispersion, large frequency dispersion is usually observed in C-V characteristic of high-k oxide/GaAs MOS devices as listed in **Table 1-3**. To understand the physical origin of frequency dispersion, different model has been carried out to explain the observed phenomenon. It was not until Hasegawa proposed the high density of interfacial states for anodic oxides on GaAs surface that workers generally ascribe the anomaly to a high density of interfacial states. [4] However, at accumulation region, the time constant of interfacial traps is far too short for the range of frequencies below 1kHz. On the other hands, traps inside the gate insulator close to interface can communicate with conduction or valance band through tunneling, and do have longer time constant consistent with experimental data. Yu Yuan has proposed a distributed model based on tunneling mechanism for border traps to explain the observed frequency dispersion. [5]

Table 1-3. Frequency dispersion in C-V measurement of different works

Structure	**F. D.**	**Structure**	**F. D.**	**reference**
Al_2O_3/p-GaAs	11.1%	Al_2O_3/n-GaAs	52.8%	[13]
Al_2O_3/AlN/p-GaAs	13.4%	Al_2O_3/AlN/n-GaAs	26.5%	[14]
Al_2O_3/p-GaAs	9.0%	Al_2O_3/n-GaAs	22.2%	**This work**
Al_2O_3/Y_2O_3/p-GaAs	4.4%	Al_2O_3/Y_2O_3/n-GaAs	12.2%	**This work**

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2. Theory and Instruments

2.1 Film deposition methods

2.1.1 Molecular Beam Epitaxy (MBE)

Molecular beam epitaxy (MBE) was first developed by A. Y. Cho and J. R. Arthur in early 1970s. MBE is a process for growing thin, epitaxy films of a wide variety of materials, including semiconductors, oxides and toplogical insulators. In the MBE process, the beam of atoms or molecules in an ultra-high-vacuum (~10^{-10}torr) are incident upon a heated crystal to form a crystalline layer. Note that the composition of the films can be changed rapidly, and produce almost atomically abrupt interface. The ability of producing a large range of unique structure such as supper-lattice and quantum-well device is benefit from the cleanliness of the growth environment, precise control of composition and excellent thickness control.

The growth rate for MBE is determined by the source flux, so the composition of the grown epi-layer and doping concentration can be estimated by the source evaporation rate. To grow a high quality thin film, the time for deposition of a monolayer should be longer than the surface-diffusion-incorporation time to avoid the incorporated atoms from being buried by the incoming monolayer. Moreover, the substrate temperature is an important parameter during MBE process. Growth under low substrate temperature, the

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rearrangement is not sufficient and lead to poor crystal quality. If the substrate temperature is too high, atoms may desorb from surface. Growth at an adequate growth temperature, atoms have enough energy to move to the proper position and not desorb from the surface.

In Fig 2-1, a typical MBE system is shown. During the growth, effusion cells are heated by a foil heater. Reflective high energy electron diffraction (RHEED) is used for define the crystal quality and the surface structure of a growing film. And liquid nitrogen cooled shrouds and cooling equiment with fluid water are the coolant.

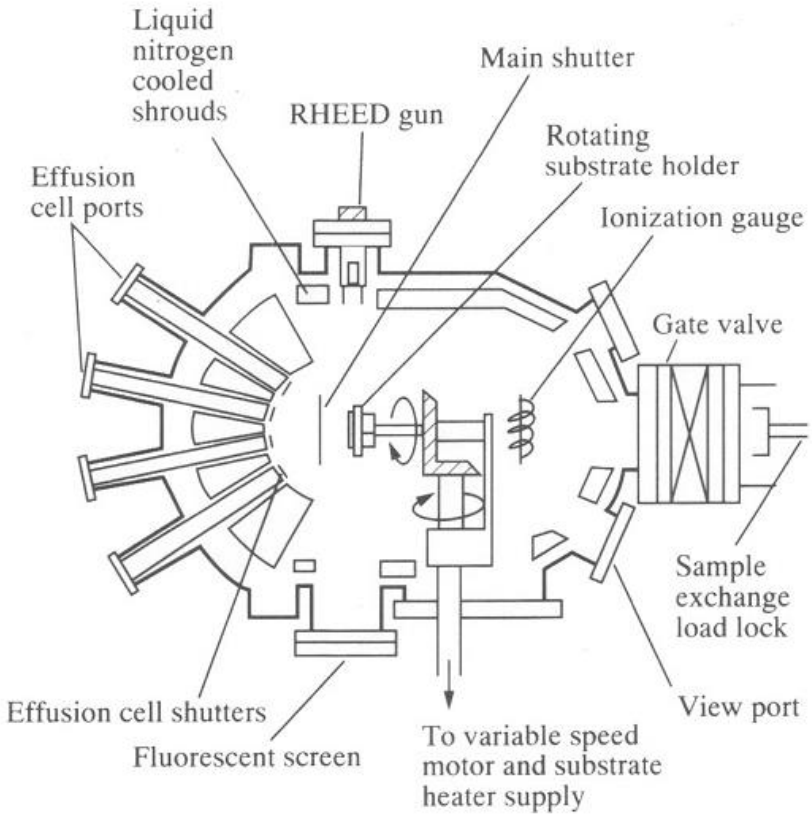

Fig. 2-1 The typical construction of a MBE system.

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2.1.2 Atomic layer deposition (ALD)

Atomic-layer-deposition (ALD) is a thin film technology based on surface controlled thin film deposition. The technique was first developed for nanolaminate insulators and zinc sulfide phosphor films for thin film electroluminescent displays. And now become a powerful resource for highly competitive products and advance nanotechnology research. ALD is well-known for its precise thickness control, pin hole free and excellent conformal thin films for 3-D structure device. [15]

Unlike the conventional chemical vapor deposition (CVD), ALD is a self-limiting growth mechanism. Based on the self-limiting reactions, ALD have superior conformity on high aspect ratio structure. A general ALD process consists of four steps as shown in Fig. 2-2, including (1) pulse of the precursor A into the chamber and react with the substrate through a self-limiting process that only one monolayer is formed at the surface, (2) purge of inert gas such as nitrogen to carry out the unreacted precursors and by-products, (3) pulse of counter reactant precursor B into the chamber and Ligant-exchange between A and B, (4) purge of inert gas such as nitrogen to carry out the unreacted precursors and by-products. To grow a desired material thickness, the process is then cycled until the thickness is achieved. Moreover, serval condition is crucial for ALD

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growth, including proper growth temperature, small precursor size and volatile by-product.

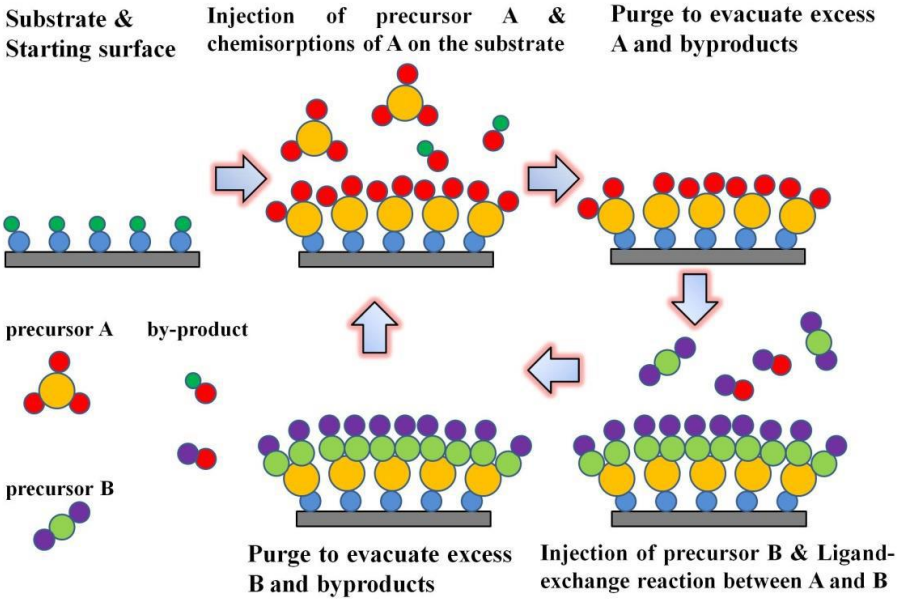

Fig. 2-2 illustration of ALD reaction cycle

2.2 Metal-Oxide-Semiconductor Capacitors (MOSCAPs)

Excellent oxide/semiconductor interface is the backbone of the CMOS technology. So, characterization of metal-oxide-semiconductor hetero-structure become an urgent issue and widely studied. The MOS structure was first proposed by Moll and Pfannand Garrett in 1959. The first successful MIS structure was soon carried out in 1960 by Ligenza and Spitzer using thermal grown SiO_2 on Si. [16] Lateral, Nicollian and Brews have developed a comprehensive and in-depth treatment of MOSCAPsa. [17] Since the system is directly related to most devices and integrated circuits. Metal-oxide-

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semiconductor capacitors (MOSCAPS) is widely applied for study of oxide/semiconductor interface.

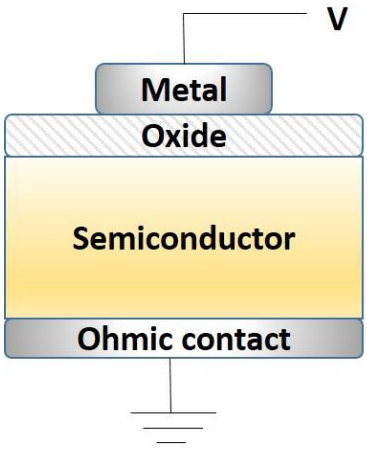

Fig. 2-3 Typical MOSCAP.

2.2.1 Measurement equipment

To characterize the MOSCAPs, capacitance-voltage (C-V) characteristic, current-voltage (I-V) characteristic, conductance method (G-V) and quasi-static CV (QSCV) measurement are the common use measurements. C-V curves of MOSCAPs were measured with a DC voltage and a small AC current (25mV~30mV) from 100Hz to 1MHz using Agilent 4284A LCR Meter. J-E characteristic were measured using Agilent 4156C Precision Semiconductor Parameter Analyzer and HP 8510C network analyzer. Note that all the measurement were measured in the dark to prevent extra generation of carriers.

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2.2.2 Conduction mechanisms in dieletric films

The conduction mechanism in high κ dieletric thin films plays an important role in application of high κ material. Since the application of dielectric films is a major subject for the semiconductors industry especially for CMOS technique. Diligent studies have been carried out to examine the conduction mechanism in dielectric films. The conduction in thin dielectric films can be classified into electrode-limited conduction mechanism and bulk-limited conduction mechanism. The electrode-limited conduction mechanism depends on the physical properties between the electrode dielectric interface such as barrier height and effective mass difference. While the bulk-limited conduction mechanism depends on the electrical properties of dielectric itself, such as trap level and trap density. [18]

The Shottky emission, Fowler-Nordhiem tunneling and direct tunneling are the main electrode-limited conduction mechanisms. Shottky emission occurs if the electrons can obtain enough thermal energy to overcome the energy barrier between electrode (semiconductor) and dielectric. The so called thermionic emission is one of the most commonly observed conduction mechanism. The expression of Shottky emission is as followed.

$$J = AT^2 \exp\left(\frac{-\mathrm{q}\left(\phi_B - \sqrt{qE/(4\pi\varepsilon_r\varepsilon_o)}\right)}{kT}\right) \quad (1)$$

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Where A is the Richardson constant, T is the absolute temperature, $q\phi_B$ is the conduction band offset, E is the electrical field across the insulator, k is the Boltzman's constant, ε_o is the permittivity in vacuum and ε_r is the optical dielectric constant. Note that Shottky emission is not strongly dependent of gate voltage. To verify a Shottky emission, the plot of $\log(J/T^2)$ versus $E^{1/2}$ should be linear.

When the energy of the incident is less than the potential barrier, quantum theory predicted that the electron wave function can penetrate through the barrier. Fowler-Nordhiem tunneling (F-N) occurs when large electrical field is applied, so that the electron can tunnel through the triangular potential barrier. Using the well-known WENTZEL-KRAMERS-BRILLOUIN (WKB) approximation and Taylor expansion near Fermi-level, the expression of F-N tunneling can be expressed by

$$J = \frac{q^3 E^2}{8\pi h q \phi_B} \exp\left(\frac{-8\pi(2qm_T)^{1/2}}{3hE}\phi_B{}^{3/2}\right) \quad (2)$$

Where m_T is the effective tunneling mass in the dielectric. The FN tunneling occurs at high electrical field. To verify the FN tunneling, the plot of $\ln(J/E^2)$ versus 1/E must be linear, with the slope related to the barrier height as follow.

$$S = -6.83 \times 10^7 \sqrt{\frac{m_T}{m_0}\phi_B{}^3} \quad (3)$$

If the bias across the dielectric is not large enough, the electron have to tunnel through the whole dielectric thickness. In general, when the oxide thickness less than

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3.5nm, direct tunneling dominates. While oxide layer thicker than 5nm, FN tunneling dominates. The illustration of the three different electrode-limited conduction mechanism are shown in Fig. 2-4.

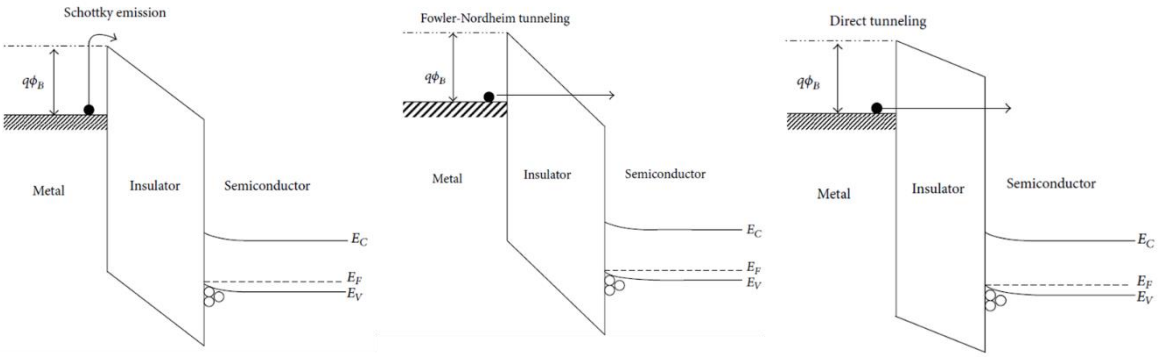

Fig. 2-4 Band diagram of Shottky emission, FN tunneling and direct tunneling

Unlike electrode-limited conduction, bulk-limited conduction depend on the electrical properties of the dielectric. Poole-Frenkel Emission, Ohmic conduction, Hopping conduction and Grain-boundary-limited conduction are the commonly observed bulk-limited conduction mechanism. Poole-Frenkel Emission is so called internal Shottky emission. The electrons in the trapping center with enough thermal energy can excited to dielectric conduction band. Hopping conduction happens when trapped electrons tunnel from one trap site to another in the dielectric films. While Grain-boundary-limited conduction is observed in a polycrystalline dielectric material. The grain boundary would build a grain boundary potential energy related to the grain boundary trap density.

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2.2.3 Ideal CV characteristics

To characterize the MOS structure, C-V characteristic is powerful and provide some important parameters. The MOS capacitance is extracted from the admittance measurement by the LCR meter.

$$Y = i\omega C + G \tag{3}$$

Where Y is the measured admittance, G is conductance and C is the capacitance. And the MOS capacitance is defined as the differential of charge change by gate bias.

$$C = \frac{dQ}{dV_g} \tag{4}$$

For an ideal MOSCAP, the measured capacitance equals to oxide capacitance in series with semiconductor capacitance. For simplicity, we assumed the flat band voltage equals to zero. We now consider an ideal metal/oxide/p-semiconductor system under different bias. The C-V curves and band diagram are shown in Fig. 2-5 and Fig. 2-6.

(1) Gate bias V = 0 V (flat band)

This is so called the flat band condition, which occurs when the Fermi-level of semiconductor is aligned with metal Fermi-level. Therefore, no extra charge and field exist in the system. And now, the semiconductor capacitance is given by

$$C_{FB} = \frac{\varepsilon_s}{L_D} \quad L_D = \sqrt{\frac{kT\varepsilon_s}{N_A q^2}} \tag{5}$$

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ε_s is the permittivity of semiconductor, N_A is the doping concentration and L_D is the Debye length in the semiconductor. The Debye length is defined by the distance in semiconductor which local electrical field can affect the distribution of free charge carriers.

(2) Gate bias V <0 (accumulation region)

Under negative bias, holes accumulate at p-semiconductor surface and an accumulation layer of holes is induced. When a small AC signal is applied, the hole would immediately response to the voltage change as illustrate in Fig 2.6 (a). When the semiconductor capacitance is much larger than oxide capacitance, the measured capacitance is just-like a parallel-plate capacitor equals to oxide capacitance. But, the keep scaling down of CET make oxide capacitance close to semiconductor capacitance, which will be detail discussed in Chapter 4.

$$C_{(acc)} = \frac{1}{\frac{1}{C_s} + \frac{1}{C_{ox}}} \approx C_{ox} \tag{6}$$

(3) Gate bias V <0 $\psi_B > \psi_s > 0$ (depletion region)

In this region, space charge region is formed. ψ_B is the Fermi-level potential with respect to midgap, while ψ_s is surface Fermi-level.

$$\psi_{Bp} \approx \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{7}$$

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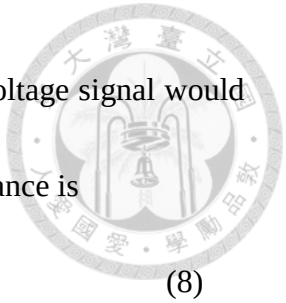

And no accumulation of charge near the surface. A small AC voltage signal would cause a change in the space charge width. Thus the measure capacitance is

$$C_{(del)} \approx \frac{1}{\frac{\varepsilon_s}{W_D} + \frac{1}{C_{ox}}} \tag{8}$$

(4) Gate bias V < 0, $2\psi_B > \psi_s > \psi_B$ (weak inversion region)

In weak inversion region, the maximum depletion width is not reached. But the very small inversion carrier is accumulated at the surface. Therefore, the capacitance is just like the case in depletion region. The maximum depletion width is given by

$$W_D = \sqrt{\frac{4\varepsilon_s kT ln(N_A/n_i)}{q^2 N_A}} \tag{9}$$

(5) Gate bias $V < 0$, $\psi_s > 2\psi_B$ (strong inversion region)

In strong inversion region, the electron accumulate at the semiconductor surface if the minority response time can respond to the measure frequency. Thus the capacitance equals to the oxide capacitance. But if the measure frequency is too high that the minority carrier response cannot follow, the measured capacitance equals to C_{min} as shown in Fig. 2-6 (c). Moreover, if the DC sweep is too fast for minority carrier to response, deep depletion would be observed as in Fig. 2-5 (d).

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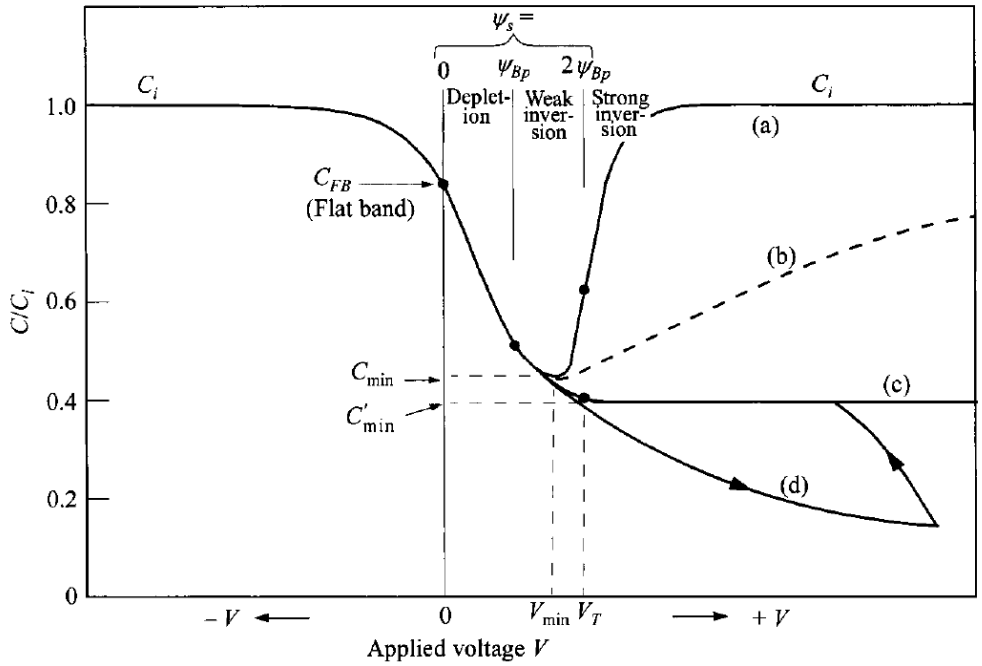

Fig. 2-5 MOS C-V curves. (a) low frequency (b) intermediate frequency (c) high frequency (d) deep depletion.

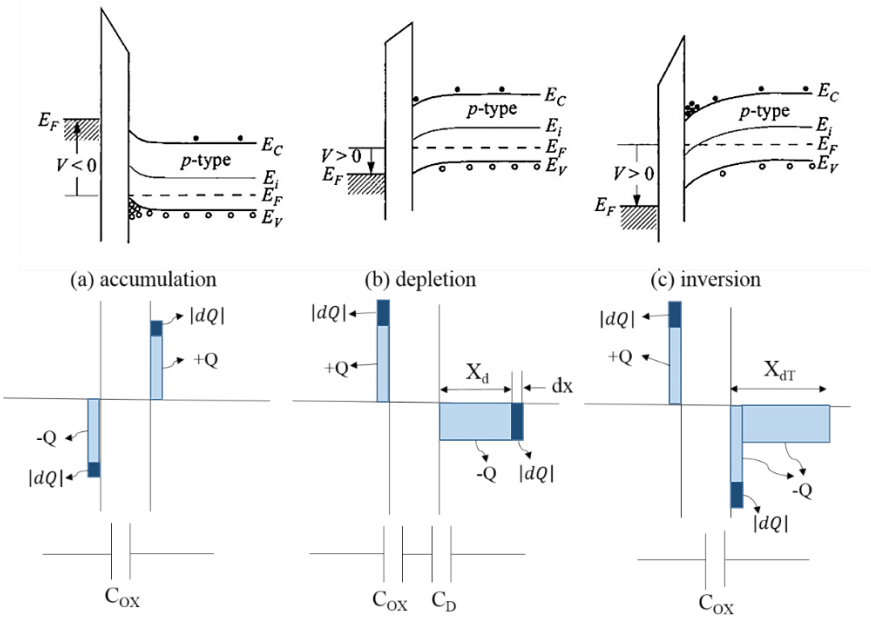

Fig. 2-6 Band diagram of ideal MOSCAP at (a) accumulation region (b) depletion region (c) inversion region.

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2.2.4 D_{it} extraction methods

In non-ideal case, charge would be trapped in the oxide or at the oxide/semiconductor interface. The trap would exchange charge with semiconductor bands and result in nonideal C-V characteristic, such as “stretch-out” effect, frequency dispersion, trap-induced inversion humps, Fermi-level pining and so on. Moreover, the traps affect charge transport in the channel in MOSFET application. In the past years, diligent efforts and characterization were carried out to probe the so called interfacial traps at oxide/semiconductor interface. Fig. 2-7 shows the equivalent circuits incorporating C_{it} (interfacial traps capacitance).

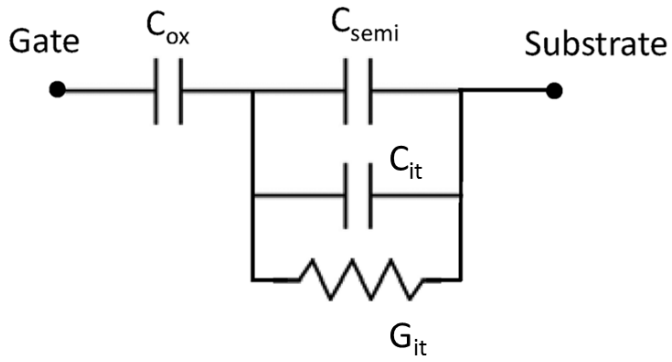

Fig. 2-7 Equivalent circuits including interface-trap effect

Terman method

Terman method is a method which can extract D_{it} from high frequency measured C-V characteristics. It was first proposed by Terman in 1965, which was one of the first

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methods for extracting interfacial traps density. Terman method assumed that the interfacial traps cannot response to high-frequency AC signals but can response to the DC signals, leading to C-V curves stretch-out. With the measured high-frequency capacitance, we can deduce the depletion capacitance and the corresponding surface potential as in Fig 2.8. Differentiate the difference between the ideal $V_g - \psi_s$ calculated from theory and the one obtained from measurement. We can extract the D_{it} value using the relation.

$$D_{it} = \frac{C_{ox}}{q^2}\frac{d\Delta V_G}{d\psi_s} \tag{10}$$

Fig. 2-8 Equivalent circuits at high frequency

QSCV measurement

It was so called low frequency method and was first developed by Berglund. [19] Unlike Terman method, QSCV measurement use DC current sweep at very low rate to ensure every trap response to applied voltage. The measure capacitance is obtained integration of total current divided by change of gate bias.

$$\mathrm{C} = \frac{\Delta \mathrm{Q}}{\Delta V_g} \quad \Delta \mathrm{Q} = \int I dt \tag{11}$$

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At low measurement frequency, the G_{it} (conductance) can be neglected. The corresponding equivalent circuit is shown in Fig 2.9. With Berglund integral, one con derive the ψ_s-V_G relationship.

$$\frac{d\psi_s}{dV_G} = \frac{C_{ox}}{C_{ox} + C_D + C_{it}} = 1 - \frac{(C_D + C_{it})}{C_{ox} + C_D + C_{it}} = 1 - \frac{C_{LF}}{C_{ox}} \tag{12}$$

$$\psi_s(V_2) - \psi_s(V_1) = \int_{V_1}^{V_2} 1 - \frac{C_{LF}}{C_{ox}}\,\mathrm{dV} + \text{constant} \tag{13}$$

Again, we can use the ideal $V_g - \psi_s$ calculated from theory and the one obtained from measurement. We can extract the D_{it} value using the above equation.

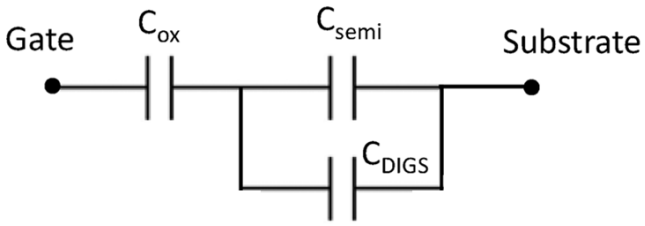

Fig. 2-9 Equivalent circuits at low frequency

Conductance method

The conductance method is first proposed by Nicollian and Goetzberger in 1967. [17] Conductance method is well-known for its ability of measuring interface trap of densities lower than 10^{10} $cm^{-2}eV^{-1}$. The conductance method extract the D_{it} value from the

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equivalent parallel conductance (G_p) of an MOSCAP. By dividing the parallel conductance by the measured frequency, one can derive the D_{it} value.

$$\frac{G_P}{\omega} = \frac{C_{it}\omega\tau_{it}}{1+(\omega\tau_{it})^2} \tag{14}$$

Where $\tau_{it} = \frac{\exp(\Delta E/k_B T)}{\sigma v_t N}$, ΔE is the trap level from band edge, σ is the capture-cross-section, v_t is the thermal velocity and N is the conduction band/valance band density of states. However, the above equation is valid for single level trap. In real case we have to consider a continuous distributed trap energy in the band gap. Leads to

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}}\ln[1+(\omega\tau_{it})^2] \tag{15}$$

At $\omega = 1/\tau_{it}$, $\frac{G_P}{\omega}$ reach its maximum value, and the interfacial trap density is

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{max} \tag{16}$$

Note that the conductance method is only valid in depletion region, while the equivalent circuit cannot be applied in inversion and accumulation region. Since the interfacial trap time constant is related to the temperature and trap energy level, the various temperatures of measurement is needed to obtain completed D_{it} spectrum in semiconductor.

Gray-Brown method

Gray-Brown method move the semiconductor Fermi-level by changing the measure temperature as shown in Fig. 2-10. As we know, the Fermi-level in bulk GaAs move

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toward the band edge as temperature decrease. This Fermi-level movement would not affected by interfacial traps since it is the bulk property. However, the interfacial trap is charged or discharged when the Fermi-level moves, and the surface potential is changed. Therefore, the flat band voltage changes to compensate the interfacial trap effect. The interfacial trap density can be extracted from the following relation.

$$D_{it} = \frac{C_{ox}[\left(V_{fb}^{T_{i+1}} - V_{fb}^{T_i}\right) - (E_f^{T_{i+1}} - E_f^{T_i})/q]}{q(E_f^{T_{i+1}} - E_f^{T_i})} \quad (17)$$

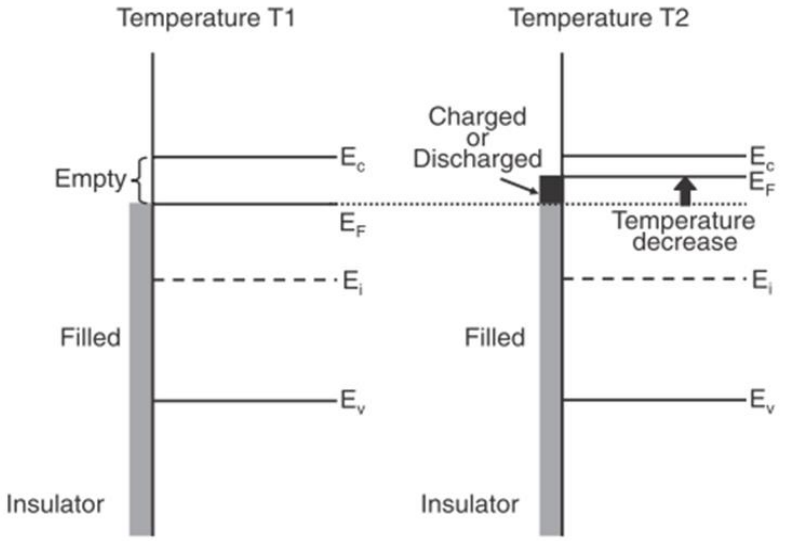

Fig. 2-10 Illustration of Gray-Brown method

2.3 Interfacial trap and border traps model

Unlike the ideal SiO_2/Si interface with extremely low trap density, it is hard to achieve low D_{it} in high-κ/(In)GaAs, resulting in large frequency dispersion in CV curves. Research efforts have been carried out to explain the origin of the large FD in

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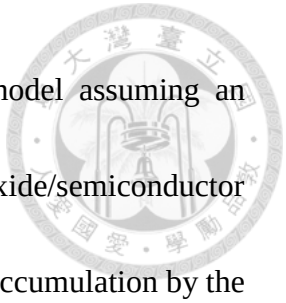

oxides/(In)GaAs interfaces. In 1980, Hasegawa has proposed a model assuming an exponentially decaying spatial distribution of traps from the oxide/semiconductor interface into the bulk oxide layer to explain the large FD of CVs at accumulation by the interfacial traps. [4] The equivalent circuit is shown in Fig. 2-8. The parallel capacitance, conductance and assumed traps distribution are as follows.

$$N_T(x) = N_{T0}\exp(-\alpha x) \tag{18}$$

$$C_{it} = \frac{q^2 N_{T0}}{2\kappa}(\omega\tau_0)^{(\alpha/2\kappa)} \int_0^{1/\omega\tau_0} z^{(\alpha/2\kappa)} \tan^{-1}(z)dz \tag{19}$$

$$G_{it} = \frac{q^2 N_{T0}}{4\kappa}(\omega\tau_0)^{(\alpha/2\kappa)} \int_0^{1/\omega\tau_0} z^{(\alpha/2\kappa)} \ln(1+z^{-2})dz \tag{20}$$

α is the decay constant for interfacial traps distribution, which is about 1 nm^{-1}, κ is the tunneling attenuation constant and N_T is the trap density at the interface. However, the time constant of interfacial traps is far too short for the range of measure frequencies below 1kHz. The interfacial traps model cannot fully explain the measured C-V characteristic. Thus, Yu Yuan has proposed a distributed model for border traps in 2011 based on tunneling mechanism. [5] Unlike previous publication, which the border traps are modeled by a lump RC circuit. The proposed model reflect the distributed nature of traps over the depth in gate oxide. In the model, the traps inside gate dielectric close to interface can exchange with semiconductor conduction/valance band through tunneling as shown in Fig. 2-11.

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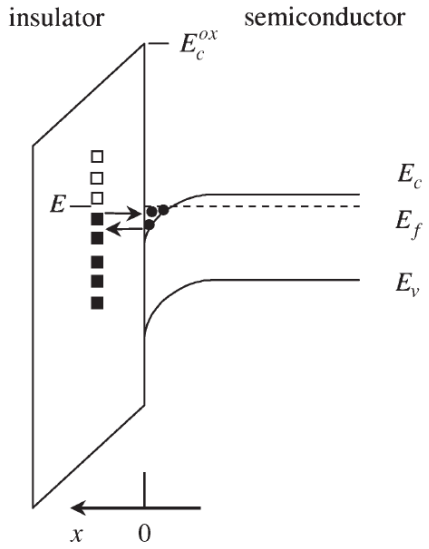

Fig. 2-11 Schematic diagram of tunneling between border traps in dielectric and the conduction band of semiconductor

The border traps within depth Δx at x is represented by ΔC_{bt} and connected with ΔG_{bt}. The traps that reside inside the dielectric possess a longer time constant than that of the interfacial traps. One can use the Wentzel-Kramers-Brillouin (WKB) approximation to derive the time constant τ(x) of border traps at depth x into the dielectric. ΔC_{bt} and ΔG_{bt} are related by the time constant τ(x).

$$\Delta C_{bt} = q^2 N_{bt} \Delta x \quad \frac{\Delta C_{bt}}{\Delta G_{bt}} = \tau(x) = \tau_0 \exp(2\kappa x) \tag{21}$$

Where τ_0 is the time constant of the interfacial traps; κ is the attenuation coefficient for the electron wave decay under the band offset barrier; N_{bt} is the border trap density in units of cm^{-3}. For Y_2O_3 and Al_2O_3 on n-GaAs, the attenuation coefficient κ is given by

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$$\kappa = \sqrt{2m(E_{offset})}/\hbar \tag{22}$$

Moreover, the time constant of interfacial traps τ_0 can be determined by the following relationship

$$\tau_0 = \left(\sigma v_{th} N_{eff}\right)^{-1} \exp(|E_M - E_{Fs}|/kT) \tag{23}$$

Where σ is the capture cross section (10^{-15}cm^2), v_{th} the electron thermal velocity, E_M the edge of majority carrier band, E_{Fs} the surface Fermi level and N_{eff} the effective conduction band density of states. The corresponding RC equivalent circuits for border traps model is shown in Fig. 2-12, and the recursive nature of the border traps gives the differential equation for the admittance as follow.

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\varepsilon_{ox}} + \frac{j\omega q^2 N_{bt}}{1 + \omega\tau_0 e^{2\kappa x}} \tag{24}$$

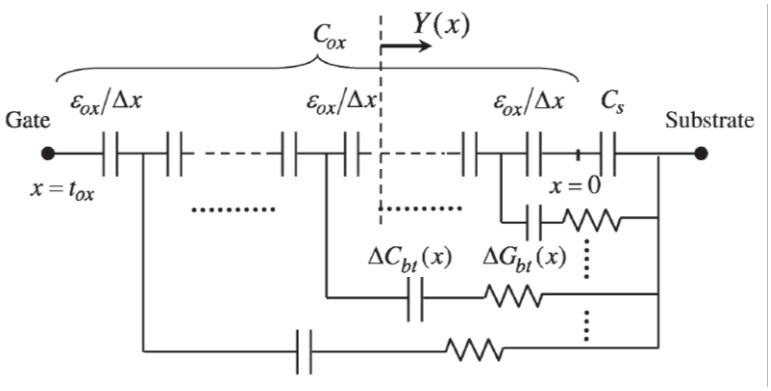

Fig. 2-12 RC equivalent circuit for border trap model

With the combination of the interfacial model and border trap model, we can better understand the frequency dispersion in C-V measurement. We can also extract the trap properties with the two models.

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3. Experimental Procedures

3.1 Sample Preparation

The growth of ALD-Al_2O_3(5nm)/ALD-Y_2O_3(2nm) and ALD-Al_2O_3 on freshly MBE grown p- and n-GaAs(001)-4×6 were carried out in a multi-chamber MBE/ALD/analyses UHV system as shown in Fig. 3-1. The system consist of one solid source GaAs-based III-V MBE chamber, one Ge-based MBE chamber, two arsenic-free oxide deposition chambers, in-situ XPS analytical systems, in-situ SPM systems and in-situ ALD chamber. All the systems are linked together under ultra-high vacuum.

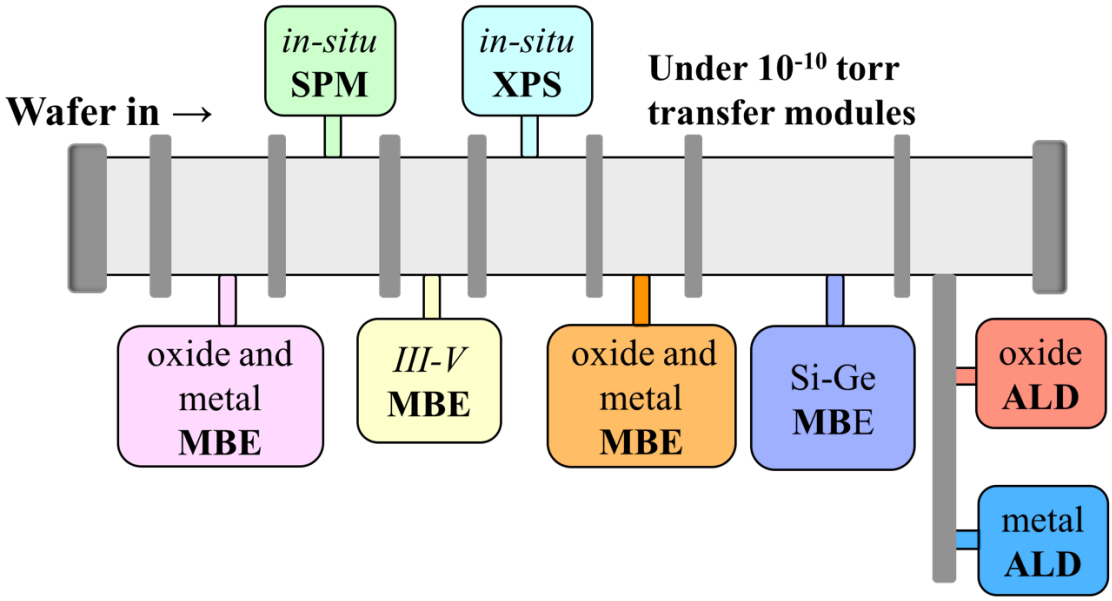

Fig. 3-1 Schematic diagram of multi-chamber MBE/ALD/analyses UHV system

3.2 Preparation of GaAs (001)-4×6 surface

In this work, the 2-inch n^+-GaAs (001) and p^+-GaAs (001) wafers were used as the substrate. Before the growth, the wafers was heated to about 600^{O}C to desorb the

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native oxide. To avoid trap diffusion from GaAs wafers, supper-lattice of GaAs(10 Å)/AlGaAs(10Å) was first deposited on GaAs wafer before GaAs buffer layer deposition. After supper-lattice deposition, a 100nm thick n-/p- GaAs buffer layer with $1-5\times 10^{17}\ cm^{-3}$ Si/Be doped were epitaxial deposited. We then transfer the wafers to an As-free chamber for surface reconstruction. The reflection High-energy Electron Diffraction (RHEED) was used for monitoring the GaAs surface reconstructions. After serval minutes annealing at 550°C, GaAs surface reconstructed from 2×4 to 4×6 surface reconstruction.

3.3 Atomic-layer-deposited high κ

Lateral, the samples were subsequently transferred into the ALD chamber for oxide deposition. In deposition of Al_2O_3(5nm)/Y_2O_3(2nm)/GaAs samples, the films were deposited at 270°C with $Y(ETCP)_3$ and H_2O as precursors. [20] The growth rate is about ~0.15nm/cycle. After 1nm Y_2O_3 deposition, the samples were transfer into an ultra-high vacuum chamber for UHV annealing. The UHV annealing remedy the interface and get rid of unreacted precursors as well as ligands. We then transfer the wafer back to ALD chamber to finish the growth. An ALD-Al_2O_3 capping layer of 5nm-thick on top of the Y_2O_3/GaAs has prevented Y_2O_3 from moisture absorption in air. In deposition of

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Al_2O_3/GaAs samples, The Al_2O_3 films were deposited at 320°C by using TMA (TriMethylAluminium) and de-ionized H_2O as precursors.

3.4 Post deposition annealing condition

Optimized post deposition annealing (PDA) was conducted at 900°C for 60s in N_2 for Y_2O_3/GaAs samples, and 550°C 30s in N_2 followed by 850°C 10s in He for Al_2O_3/GaAs samples, prior to the gate metal deposition.

3.5 Metal electrode deposition

The gate metal of the MOSCAPs was deposited by e-beam evaporation of nickel (Ni) 100nm through a shadow mask with $7.85 \times 10^{-5}\ cm^2$ in area, the back contact was deposited by thermal evaporation of gold (Au) 100nm/ titanium (Ti) 30nm. The Schematics of MOSCAPs structure are shown in Fig. 3-2.

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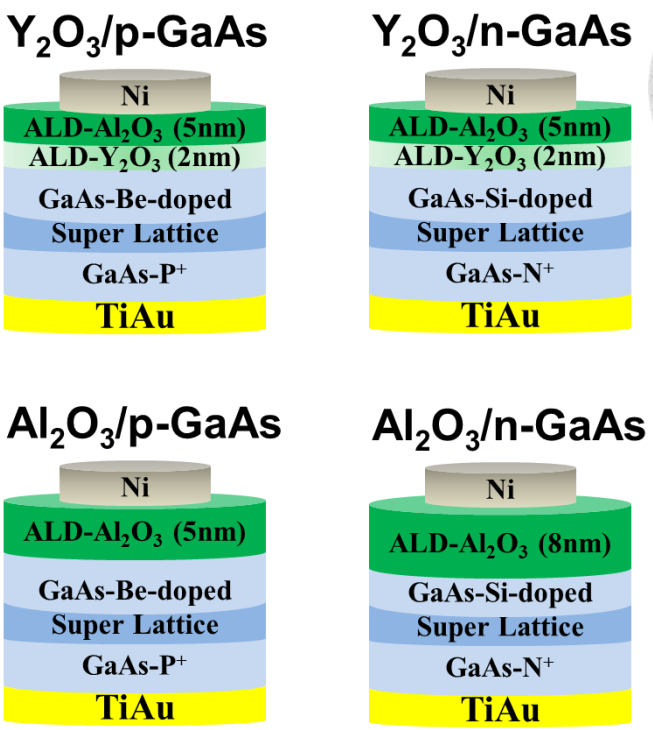

Fig. 3-2 Schematic cross-section of GaAs MOSCAP with Ni metal gate and Ti/Au back electrode.

3.6 Electrical measurement

The CV characteristic and conductance characteristics were measured at room temperature with frequency from 100Hz to 1MHz using Agilent 4284 LCR meter. The current versus voltage (I-V) characteristics and QSCV were measured in dark at room temperature by Precision Semiconductor Parameter Analyzer Agilent 4156C.

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4. Results and Discussion

4.1 Comparison of C-V characteristic between Al_2O_3 and Y_2O_3 passivated GaAs surface

GaAs and InGaAs are the leading candidates to replace Si as the n-channel material for future complementary MOSFETs because of their relatively high electron mobilities. With a lattice mismatch of 8% with Si(001), $In_{0.53}Ga_{0.47}As$ is difficult to be integrated onto the Si(001) platform. In comparison, GaAs with a smaller lattice mismatch of 4% with Si is much easier to be grown on Si(001). Besides, with excellent uniformity and conformal coverage in nanometer thick film growth, atomic layer deposition (ALD) has been widely employed in depositing high-κ dielectrics for MOSFETs since the 45 nm node. Therefore, as an urgent issue, intensive efforts in ALD high-κ dielectrics on GaAs(001) have been carried out to characterize and perfect these interfaces. C-V characteristic is one of the most useful measurement to characterize the oxide/semiconductor interface through MOSCAPs device. And most of the fundamental problem in the device performance, reliability and stability are related to the oxide/semiconductor interface quality. In this part, comparison of C-V curves between Al_2O_3/GaAs and Y_2O_3/GaAs is demonstrated. Moreover, some carefully extraction of oxide capacitance is calculated.

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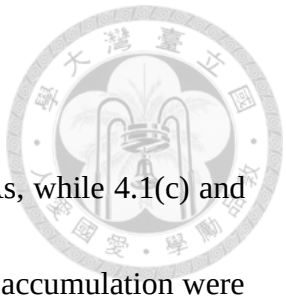

4.1.1 CV characteristics

Figure 4.1 (a) and 1(b) show the CVs of Y_2O_3 on p- and n-GaAs, while 4.1(c) and 4.1 (d) show those of Al_2O_3 on p- and n-GaAs. FDs of 4% (12%) in accumulation were measured for Y_2O_3/p(n)-GaAs, smaller than those of 9% (22.2%) for Al_2O_3/p(n)-GaAs. Unlike other work using ex-situ ALD approach usually give a large FD as in Table. 4-1. Ex-situ AlN passivation layer and sulfur-passivation GaAs surface still result in large frequency dispersion. [13,14] Our in-situ ALD approach without passivation layer and surface treatment result in reasonable frequency dispersion. Both Al_2O_3/GaAs and Y_2O_3/GaAs samples show typical C-V characteristics for p-type samples and small frequency dispersion from inversion to accumulation. However, large difference in n-type counterparts is observed. The much smaller frequency dispersion at depletion region is observed in Y_2O_3/GaAs sample than Al_2O_3/GaAs sample, indicating lower interfacial trap density. Note that no inversion behavior is observed, which is attributed to the long minority carrier response time.

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Table. 4-1 frequency dispersion in C-V measurement of different works

Structure	**F. D.**	**Structure**	**F. D.**	**reference**
Al_2O_3/p-GaAs	11.1%	Al_2O_3/n-GaAs	52.8%	G. B et, al
Al_2O_3/AlN/p-GaAs	13.4%	Al_2O_3/AlN/n-GaAs	26.5%	T. Aoki et,al
Al_2O_3/p-GaAs	9.0%	Al_2O_3/n-GaAs	22.2%	**This work**
Al_2O_3/Y_2O_3/p-GaAs	4.4%	Al_2O_3/Y_2O_3/n-GaAs	12.2%	**This work**

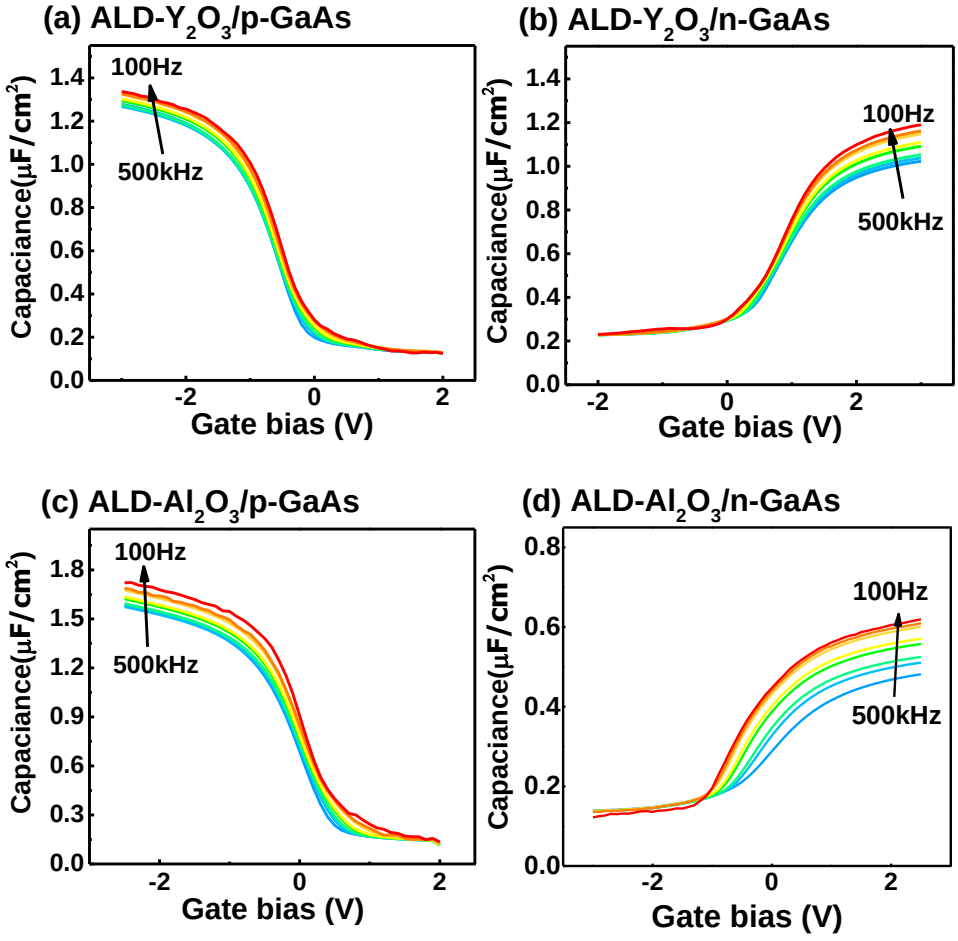

Fig. 4-1 CVs of MOSCAPs of ALD-Y_2O_3 on (a) p-type and (b) n-type GaAs, and ALD-Al_2O_3 on (c) p-type and (d) n-type GaAs.

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Furthermore, we have measured CVs at 150°C at different frequency to investigate the interfacial and border trap responses in depletion and weak inversion regions. Figure 4-2 shows the CVs of Y_2O_3 and Al_2O_3 on n-GaAs measured at 150°C in dark. With a band gap of 1.42 eV and a low conduction band density of states, GaAs possesses a relatively longer minority-carrier response time than Si, such that minority carriers should not respond to common measured frequencies in inversion region even at 150°C. As GaAs possess a very long minority carrier generation time, and therefore, cannot follow the measurement frequency even at high temperatures. The humps in depletion and weak inversion regions of Al_2O_3/n-GaAs are therefore attributed to the trap-induced capacitance responses rather than a true inversion behavior as shown in Fig. 4-2.

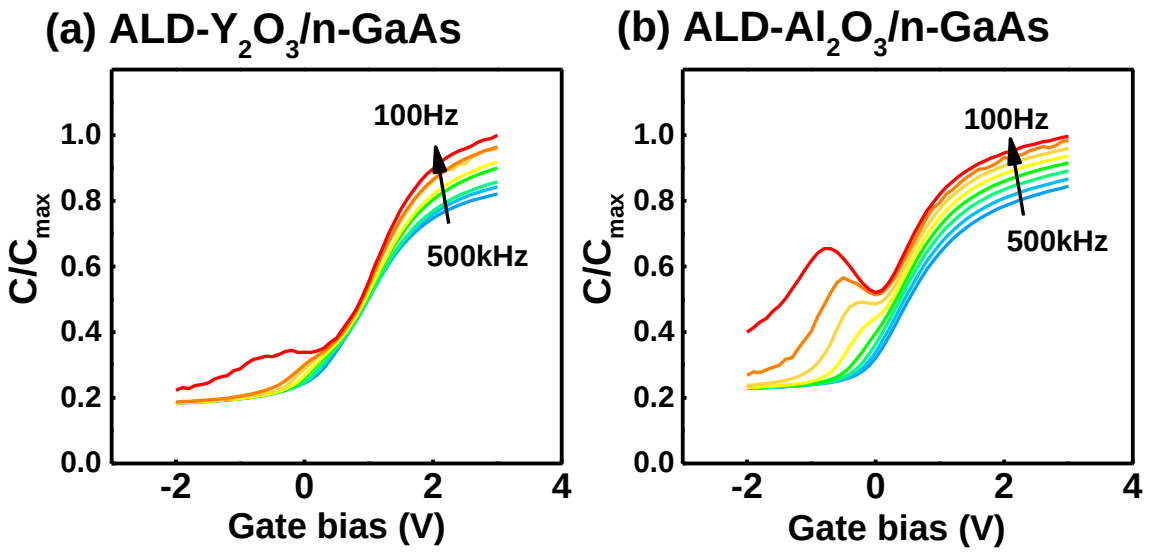

Fig. 4-2. CVs of ALD (a) -Y_2O_3 and (b) -Al_2O_3 on n-GaAs measured at 150°C**.**

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4.1.2 Oxide capacitance and electrical parameters

Effective oxide thickness is an important index for characterization MOS structure. In the past, we simply use the maximum capacitance in CV to determine the oxide capacitance. Here, the maximum capacitance of Y_2O_3/n-GaAs and Y_2O_3/n-GaAs are 1.336 μF/cm^2 and 1.189μF/cm^2, respectively. If we determine the oxide capacitance through maximum capacitance, the Y_2O_3/n-GaAs and Y_2O_3/p-GaAs would give different results. But, Y_2O_3/n-GaAs and Y_2O_3/p-GaAs with the same oxide stacks should give the same oxide capacitance. Therefore, we cannot simply determine the oxide capacitance by the maximum capacitance at accumulation. The measured capacitance at accumulation equals to oxide capacitance in series with semiconductor capacitance. When the oxide capacitance is relative small, we can ignore the contribution of semiconductor capacitance. However, as the oxide thickness is thin enough, the semiconductor capacitance have to be considered.

To derive semiconductor capacitance, two condition are considered. [21] At low electrical field region, the capacitance of semiconductor is dominated by finite density of states. Under the approximation of 3-D electron gas, Boltzman distribution and Possion equation, the surface carrier concentration is given by

$$N_s \approx \left(2n_{p0}p_{p0}\right)^{\frac{1}{2}} L_D \exp(\beta\varphi_s/2) \tag{25}$$

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Here, $\beta = \frac{q}{k_B T}$, n_{p0} and p_{p0} are electron concentration and hole concentration in the bulk, L_D is Debye length mention above and φ_s is the surface potential. Now the semiconductor capacitance at accumulation dominated by finite density of states is

$$C_{acc}^{DOS} = \frac{q\partial N_s}{\partial \varphi_s} = \frac{q^2}{2k_B} \times \frac{N_s}{T} \tag{26}$$

At high electrical field region, the accumulation layer is affected by the 2-D quantization of carriers. The accumulation thickness can be expressed by

$$C_{acc}^{thickness} = \frac{\varepsilon_{GaAs}}{Z_{acc}} \approx \left(\frac{11\varepsilon_{GaAs}^2 q^2}{72\hbar^2}\right) \times m_{GaAs}^{1/3} \times N_s^{1/3} \tag{27}$$

Where ε_{GaAs} is the permittivity of GaAs, Z_{acc} is the average thickness of 2D electron gas and m_{GaAs} is the perpendicular effective mass of GaAs. To obtain the total accumulation capacitance

$$(C_{total})^{-1} = (C_{acc}^{DOS})^{-1} + (C_{acc}^{thickness})^{-1} \tag{28}$$

To further understand the behavior of capacitance versus surface carrier density. We plotted the capacitance versus surface carrier density diagram for p-GaAs and n-GaAs substrate at Fig. 4-3 (a) and (b). At low electrical field, the p-GaAs and n-GaAs capacitance-carrier density curve are identical. But at large electrical field, the capacitance are dominated by the thickness of 2-D electron gas layer, which is related to the effective mass of the carrier. The electron effective mass of GaAs is $0.063m_0$, which is about an order smaller than the hole effective mass of GaAs $0.51m_0$. The much smaller

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effective mass result in much smaller semiconductor capacitance, which explains the observed lower C_{max} at GaAs n-type samples than p-type counterparts. From Fig. 4-3, at surface carrier density of $10^{13}cm^{-2}$, the capacitance of semiconductor is 3.36 μF/cm^2 and 6.31 μF/cm^2, respectively. The semiconductor capacitance of 3.36 μF/cm^2 and 6.31 μF/cm^2 correspond to accumulation thickness of 3.40nm and 1.81nm. Comparing the capacitance of semiconductor to the oxide capacitance, which is about 1-2 μF/cm^2, the semiconductor capacitance cannot be neglected.

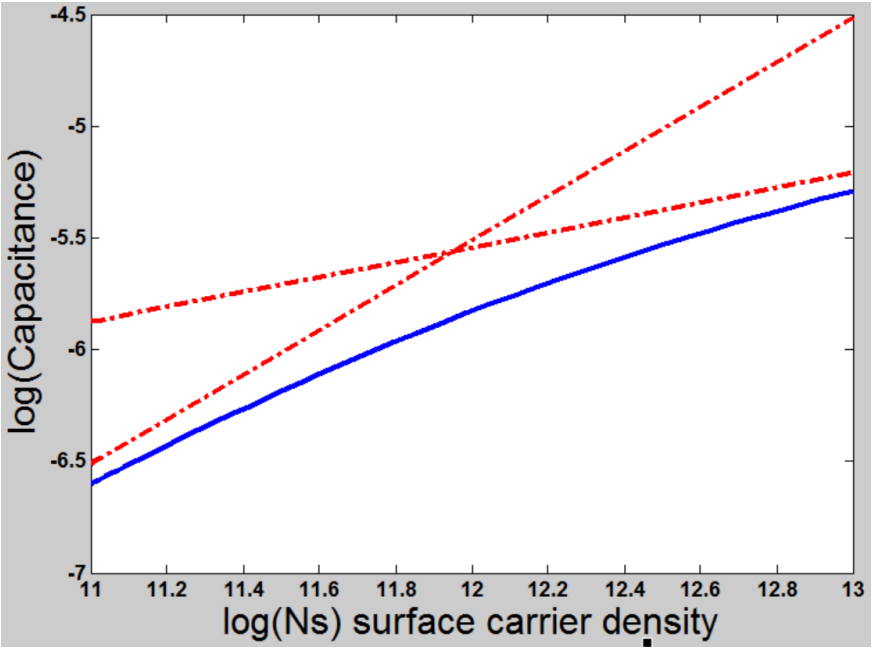

Fig. 4-3 (a) p-type accumulation capacitance versus surface carrier density. Blue line is the C_{total} versus carrier density. While the red lines are the C_{acc}^{DOS} and $C_{acc}^{thickness}$ versus carrier density, respectively.

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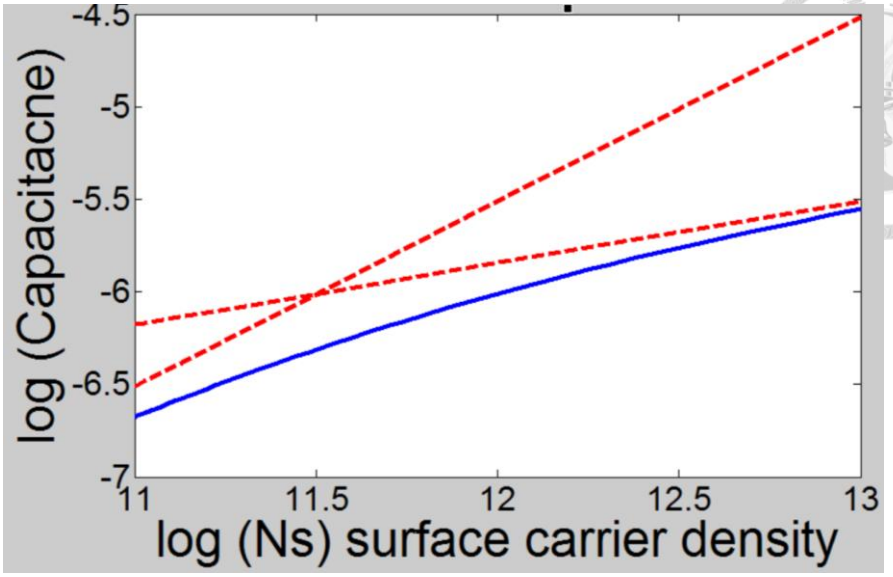

Fig. 4-3 (b) n-type accumulation capacitance versus surface carrier density. Blue line is the C_{total} versus carrier density. While the red lines are the C_{acc}^{DOS} and $C_{acc}^{thickness}$ versus carrier density, respectively.

Before we start to calculate the oxide capacitance of the Y_2O_3/Al_2O_3 and Al_2O_3 stacks, we first have to know the Debye length of GaAs, which can be extracted from the doping concentration of GaAs substrate. Fortunately, we can extract the doping concentration by the measured C_{min}.

$$C_{min} = \frac{\varepsilon_s}{W_D}, W_D = \sqrt{\frac{4\varepsilon_s kT ln(N_A/n_i)}{q^2 N_A}} \tag{29}$$

The Debye length and flat band capacitance are as follows

$$L_D = \sqrt{\frac{kT\varepsilon_s}{N_A q^2}} \quad C_{FB} = \frac{\varepsilon_s}{L_D} \tag{30}$$

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The flat band voltage is the corresponding gate voltage when measured capacitance equals to flat band capacitance. Note that high frequency measured C-V is used to ensure no traps response.

Next, we have to know the surface carrier density at accumulation region. We assumed that there is no trap response at high frequency, and the surface carrier density at accumulation region is estimated by

$$N_s \approx \int_{V_{FB}}^{V_{acc}} C_m dV \tag{31}$$

Where V_{FB} is the flat-band voltage V_{acc} is the gate bias at C_{max}, and C_m is the measured capacitance at high frequency (500kHz). For convenience, I summarize the parameters of all samples in Table. 4-2. In order to get the accurate C_{ox}, C_{ox} was first estimated by the C_{max} at p-type samples accumulation. Then we do the calculation above to extract the oxide capacitance. Note that the Al_2O_3/n-GaAs gives large frequency dispersion such that the calculation is meaningless.

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Table. 4-2 electrical parameter calculated by using estimation of $C_{ox}=C_{max}$

structure	Y_2O_3/n-GaAs	Y_2O_3/p-GaAs
Al_2O_3/Y_2O_3	5nm/2nm	5nm/2nm
$C_{max}(\mu F/cm^2)$	1.189	1.336
$C_{min}(\mu F/cm^2)$	0.230	0.127
$N_A(/cm^3)$	1.19×10^{18}	2.90×10^{17}
$L_D(nm)$	5.00	10.11
$C_{FB}(\mu F/cm^2)$	0.843	0.690
$V_{FB}(V)$	1.5	-0.6
$N_s(/cm^2)$	1.30×10^{13}	1.95×10^{13}
$C_{acc}^{GaAs}(\mu F/cm^2)$	3.103	6.86
$m_{GaAs}(m_0)$	0.063	0.51
$C_{ox}(\mu F/cm^2)$	**1.53**	**1.55**
$EOT(\text{nm})$	**2.25**	**2.23**

After the carefully extraction of all the critical parameter, Cox now can be calculated by using

$$\frac{1}{C_{acc}^{1MHz}} = \frac{1}{C_{ox}} + \frac{1}{C_{acc}^{GaAs}} \quad (32)$$

Here we use C_{acc}^{1MHz}, the high frequency measured capacitance at accumulation to make

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sure no trap response at this frequency, and we get the whole capacitance from semiconductor carrier response. Now the Y_2O_3/p-GaAs and Y_2O_3/n-GaAs give the same oxide capacitance. Note that the recalculated C_{ox} is about $1.55\mu F/cm^2$, which is larger than the first estimation of $1.336\mu F/cm^2$. This indicates that the first estimation might cause some error. Therefore, we further recalculate the parameter follow the same procedure as above, but change the C_{ox} as the one we obtained. The recalculated parameters are listed at Table. 4-3.

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Table. 4-3 electrical parameter calculated by using estimation of C_{ox} with the first calculation.

structure	Y_2O_3/n-GaAs	Y_2O_3/p-GaAs
Al_2O_3/Y_2O_3	5nm/2nm	5nm/2nm
$C_{max}(\mu F/cm^2)$	1.189	1.336
$C_{min}(\mu F/cm^2)$	0.230	0.127
$N_A(/cm^3)$	1.12×10^{18}	2.79×10^{17}
$L_D(nm)$	5.14	10.3
$C_{FB}(\mu F/cm^2)$	0.913	0.653
$V_{FB}(V)$	1.6	-0.7
$N_s(/cm^2)$	0.9×10^{13}	1.60×10^{13}
$C_{acc}^{GaAs}(\mu F/cm^2)$	2.8	6.3
$m_{GaAs}(m_0)$	0.063	0.51
$C_{ox}(\mu F/cm^2)$	**1.60**	**1.60**
EOT(nm)	**2.15**	**2.15**

In Table. 4-3, the same oxide capacitance for p-GaAs and n-GaAs are presented, which is close to the one we obtained at the first calculation. In this section, we concluded that the extraction of oxide capacitance should consider the semiconductor capacitance at

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accumulation. With right characterization, Al_2O_3/Y_2O_3/p-GaAs and Al_2O_3/Y_2O_3/n-GaAs with the same oxide stacks gave the same oxide capacitance. Moreover, Y_2O_3 passivated GaAs surface demonstated excellent C-V characteristic with extremely small frequency dispersion.

4.2 CF characteristics and Simulations

As we commonly use frequency dispersion as an important index for characterizing oxide-semiconductors interface. Researchers are eager to know the physical origin of frequency dispersion. As mention in Chapter 2, two important models were proposed and explain the physical origin of frequency dispersion. The most reasonable explanation of frequency dispersion at accumulation is the exchange of charge between the border trap inside the oxides and the semiconductors. To analyze the interfacial traps and border traps response, capacitance-log(frequency) (CF) characteristics were employed.

With the models mentioned above, we can combine the two models together as shown in Fig. 4-4.

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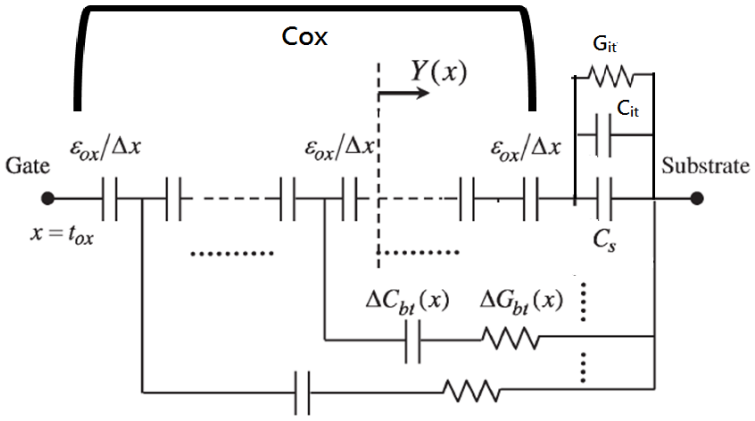

Fig. 4-4 Equivalent circuit combined border traps and interfacial traps

Here, initial admittance is given by $Y(0) = j\omega(C_{it} + C_s) + G_{it}$ as follows.

$$C_{it} = \frac{q^2 N_{T0}}{2\kappa}(\omega\tau_0)^{(\alpha/2\kappa)} \int_0^{1/\omega\tau_0} z^{(\alpha/2\kappa)} \tan^{-1}(z)dz \tag{33}$$

$$G_{it} = \frac{q^2 N_{T0}}{4\kappa}(\omega\tau_0)^{(\alpha/2\kappa)} \int_0^{1/\omega\tau_0} z^{(\alpha/2\kappa)} \ln(1+z^{-2})dz \tag{34}$$

And the admittance follows the below differential equation

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\varepsilon_{ox}} + \frac{j\omega q^2 N_{bt}}{1+\omega\tau_0 e^{2\kappa x}} \tag{35}$$

Where τ_0 is the time constant of the interfacial traps; κ is the attenuation coefficient for the electron wave decay under the band offset barrier; N_{bt} is the border trap density in units of cm^{-3}. Finally, we can simulate the CF characteristic using the above model.

In Fig. 4-5, we have simulated the CF characteristics of interfacial traps dominated condition and border traps dominated condition. It is clear that the linear relation in the semi-log diagram indicates a border traps dominate condition, while a convex CF curve

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indicates high interfacial trap density. For interfacial trap dominated condition, there is almost no frequency dispersion below 1kHz.

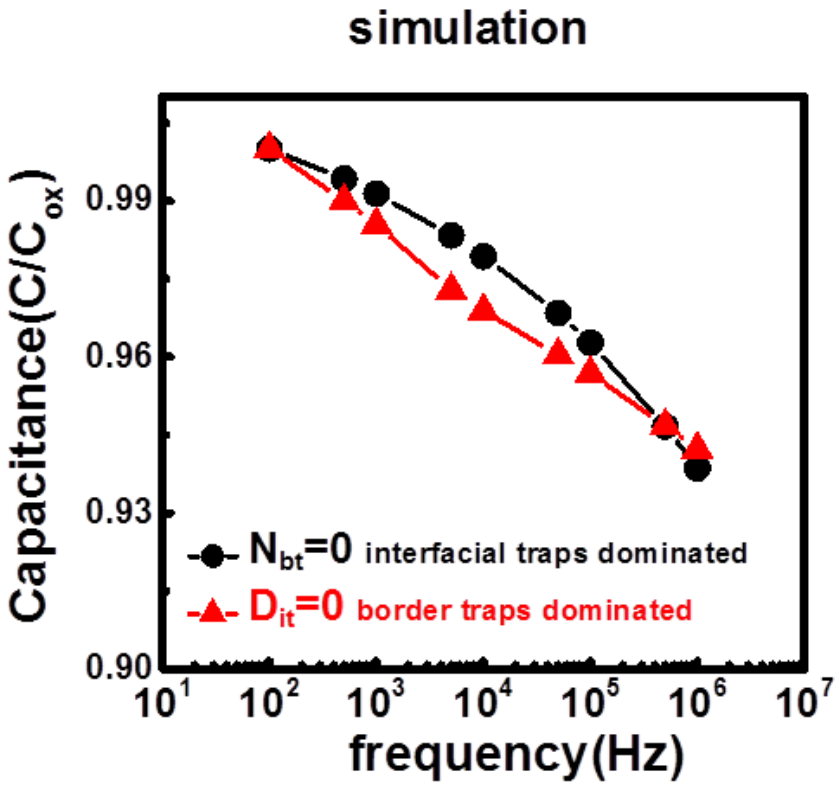

Fig. 4-5 The simulation of C-log(F) characteristics. The black line corresponds to a interfacial-trap dominated C-log(F) curve with a simulation parameter N_{bt} (border trap density) set to be zero, whereas the red line corresponds to a border-traps dominated C-log(F) curve with a simulation parameter D_{it} (interfacial trap density) set to be zero.

Fig. 4-6 shows the CF characteristic of Y_2O_3/GaAs and Al_2O_3/GaAs in Fig. 4.5 (a) and (b). The linear relation in the semi-log diagram for Y_2O_3/n-GaAs MOSCAP was observed from 100Hz to 100kHz in Fig. 4-6 (b), indicating that border traps dominate

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over the interfacial traps. This result also implies that the Y_2O_3/n-GaAs interface is nearly free from interfacial traps in accumulation. The deviation of the linear relationship at 500kHz might be caused by parasitic resistance and capacitance or the time constant discussed in the next section. The variation of normalized capacitance values from 1 kHz to 100 Hz was nearly identical in Al_2O_3/n-GaAs and Y_2O_3/n-GaAs, implying a similar border trap density in both systems near the conduction band. Furthermore, dispersion of Al_2O_3/n-GaAs was significantly larger in higher frequency region (>1 kHz), implying a higher D_{it} over the border trap density near the conduction band. Comparing Fig. 4-6(a) and 4-6(b), smaller frequency dispersion for p-type samples than that in n-type samples in accumulation region indicates less border trap responses near the valance band edge.

The dispersion in the depletion region is another important index to study the behavior of the trap responses. The Fermi level at GaAs surface in depletion region is away from the band edges, so the time constant of interfacial traps is therefore longer than that in accumulation region, suggesting a less degree of response for border traps from the oxide layer in depletion region. Figure 4.6 (c) shows the CF characteristics in depletion region for Y_2O_3/p-GaAs at gate bias of -0.5V (black hollow circles) and for Al_2O_3/p-GaAs at -0.2V (red solid circles). Figure 4.6 (d) shows the CF characteristics in depletion region for Y_2O_3/n-GaAs at gate bias of 0.5V (black hollow circles) and for

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Al_2O_3/n-GaAs at -0.2V (red solid circles). The biases were determined when the surface potential is around +0.4 eV for p-GaAs and -0.4 eV for n-GaAs systems. In the n-GaAs system, compared to the high frequency region (> 1 kHz), FD is relatively small in the low frequency region (1 kHz - 100 Hz). This is indicative of less border trap responses in depletion region. Dispersion of 38.4% for Al_2O_3/n-GaAs being much larger than 13.2% for Y_2O_3/n-GaAs indicates that there are much more interfacial traps in the Al_2O_3/GaAs interface. Having examined the dispersion spreading through the measured frequencies in both Y_2O_3 and Al_2O_3 on p- and n-GaAs in depletion region, we observed more border trap responses in p-GaAs than those in the n-GaAs.

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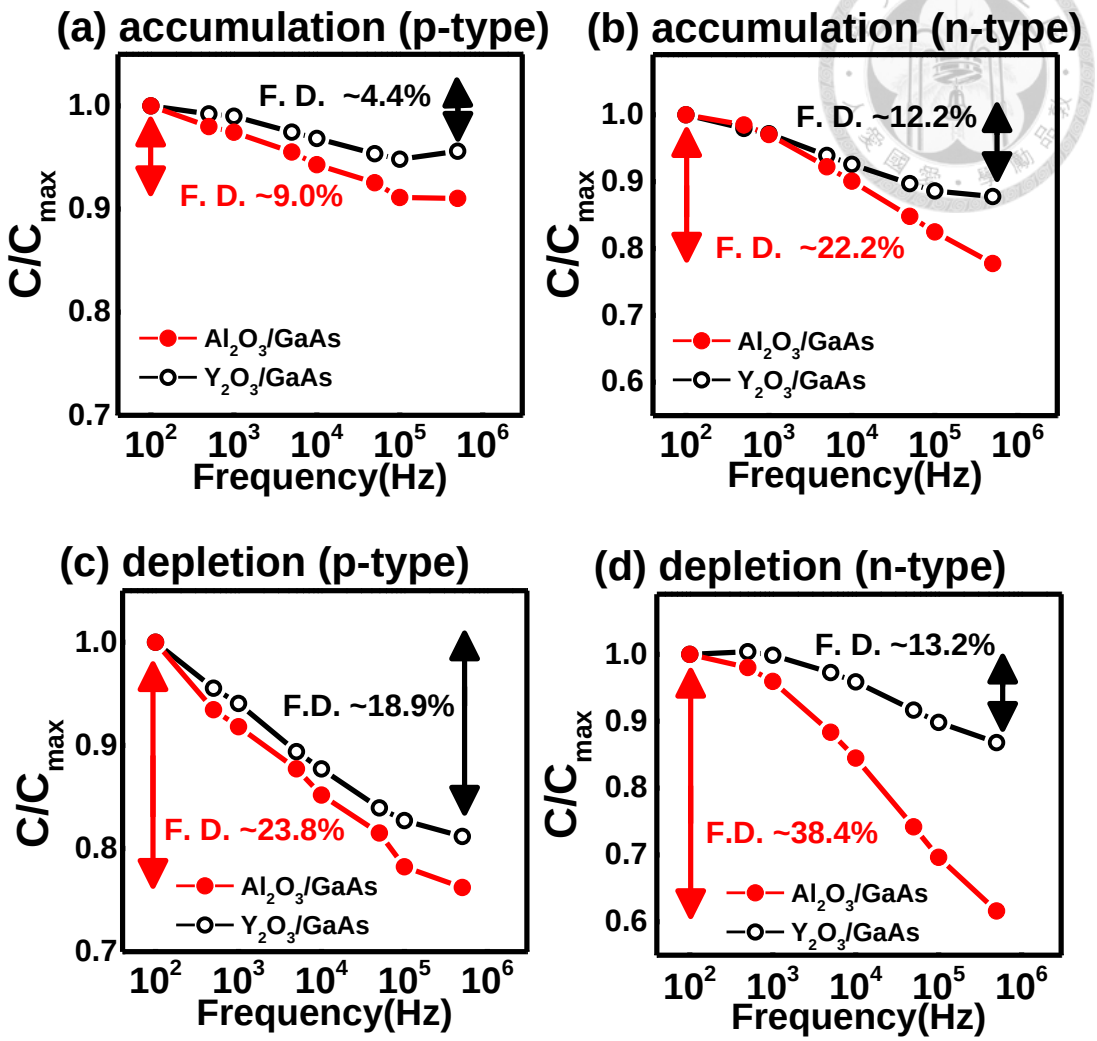

Fig. 4-6 CFs of ALD-Y_2O_3 and -Al_2O_3 on (a) p-type and (b) n-type GaAs in accumulation region, and (c) p-type and (d) n-type GaAs in depletion region.

4.3 QSCV and conductance measurement

For III-V based MOS device, mid-gap peak feature is commonly observed in D_{it} spectrum, causing the reduction of device performance. The MOSFET device performance is predominately determined by the traps density at oxide/semiconductor interface. Since the high trap density would cause Fermi-level pining and insufficient

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mobility, it is an urgent issue to understand the trap distribution in GaAs band gap. In this part, we have employed QSCVs and GVs to investigate the Fermi-level movement efficiency and D_{it} spectra within GaAs band gap. Comparison between Al_2O_3/GaAs and Y_2O_3/GaAs interface is also discussed.

Conductance method is known as a precise measurement for extracting interfacial traps density. However, the conductance method can only probe a small part of D_{it} spectrum inside GaAs band gap. Notice that the border traps would not contribute to conductance $(\frac{G_p}{\omega})$ peak, but would exhibit a tail at low frequency region, which is not observe in our data. The D_{it} values extracted by the GVs in depletion region around 4×10^{11} $eV^{-1}cm^{-2}$ for Y_2O_3/n-GaAs and 5×10^{12} $eV^{-1}cm^{-2}$ for Al_2O_3/n-GaAs as marked in solid triangle in Fig. 4-8.

QSCV measurement is first developed by Berglund. The main concept of QSCV measurement is detecting the “stretch-out” phenomenon mentioned in chapter 2. To ensure every trap response to the extra applied voltage. We keep DC sweep rate slow as 1mV/sec. The DC voltage step is about 25mV to 45mV. In order not to integral to many noise, the integration time is set us 2s. Compensation of leakage current time is integrated for 1.6 seconds. The Agilent 4156C Precision Semiconductor Parameter Analyzer has offer a procedure to measure the C_{offset}.

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Fig. 4-7 shows the QSCV in blue dots and the corresponding CV characteristic. Since the QSCV curve can detect trap with long time constant, the mismatch between QSCV curve and CV curve is attributed to border traps response. In Fig. 4-7 (a) and (c), the QSCV curves match with the C-V curves near valance band edge, indicative of a low border trap density in p-type accumulation region, resulting in much smaller frequency dispersion than n-type samples. In contrast, the capacitance values of the QSCVs in accumulation in n-type samples are much larger than those from CVs as shown in Fig. 4-7 (b) and (d), indicative of a high border trap density near the conduction band. In depletion region, the difference of capacitance values between QSCV and CV measurement is much smaller than accumulation region, implying a minor border traps response in depletion region.

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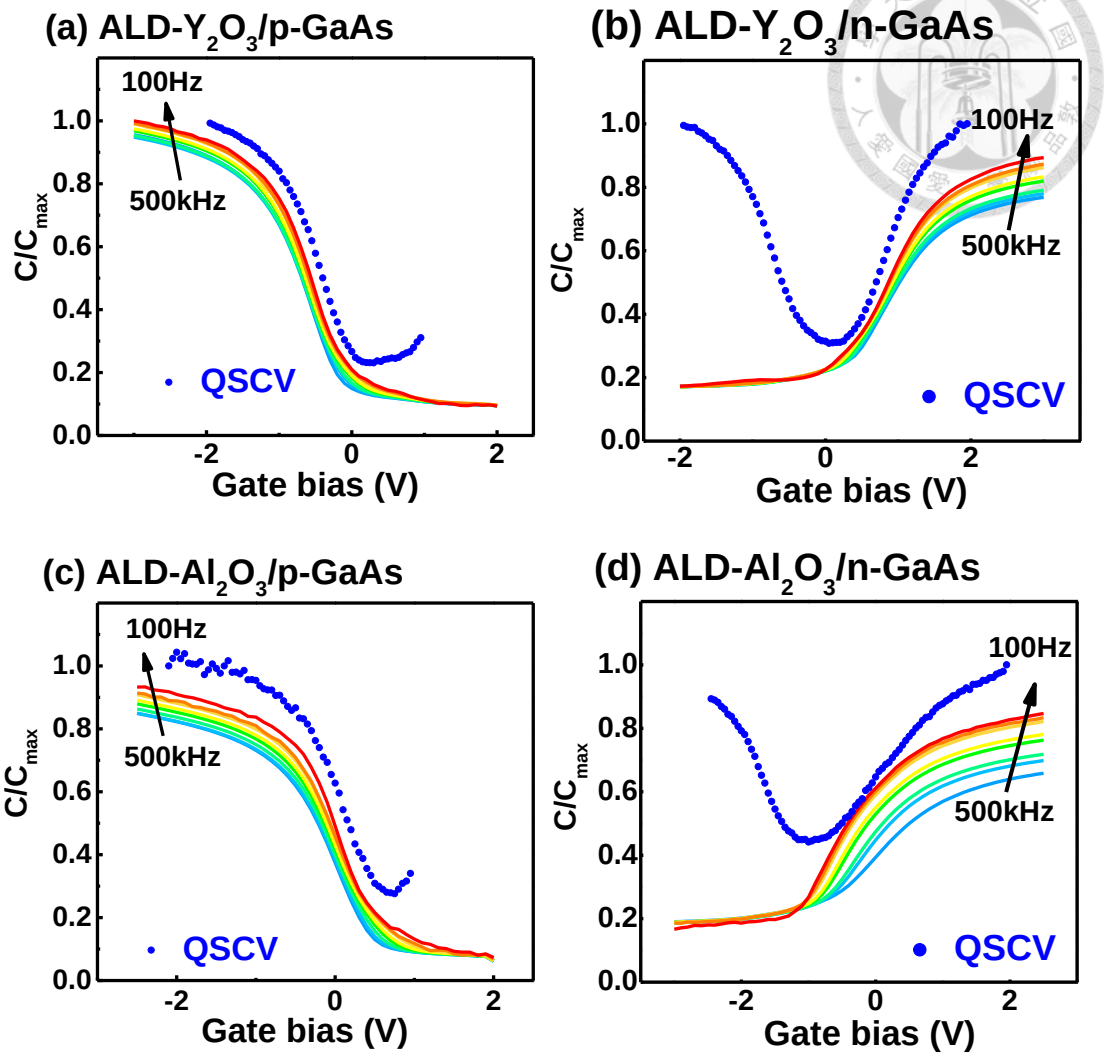

Fig. 4-7 CVs and QSCVs of MOSCAPs of ALD-Y_2O_3 on (a) p-type and (b) n-type GaAs, and ALD-Al_2O_3 on (c) p-type and (d) n-type GaAs.

To extract the relation between surface potential and gate voltage, Berglund integral is employed. The derivation of Berglund integral are as follows.

$$\mathrm{d}Q_g = C_m(V_G) \times dV_G = C_{ox} \times dV_{ox} \tag{35}$$

$$V_G = C_{ox} \times V_{ox} \qquad dV_G = d\phi_s + dV_{ox} \tag{36}$$

$$\frac{C_m(V_G)}{C_{ox}} = \frac{dV_{ox}}{dV_G} = 1 - \frac{d\phi_s}{dV_G} \tag{37}$$

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$$\phi_s(V_2) - \phi_s(V_1) = \int_{V_1}^{V_2} (1 - \frac{C_m(V_G)}{C_{ox}}) \quad (38)$$

We compare the Berglund integral obtained relation of surface potential and voltage with the simulation using MatLab software with the parameter obtained in chapter 4.2. We can derive the D_{it} spectrum using

$$D_{it} = \frac{1}{q} \frac{C_{ox} d(V_g^{ideal}{}_g(\phi_s) - V_g^{Berglund}(\phi_s))}{d\phi_s} \quad (39)$$

The D_{it}'s extracted by QSCVs are around (0.5-2) × 10^{12} $eV^{-1}cm^{-2}$ for Y_2O_3/GaAs and (0.4-10) × 10^{12} $eV^{-1}cm^{-2}$ for Al_2O_3/GaAs as shown in Fig. 4-8. Similar D_{it} values extracted by QSCVs and GVs in depletion region further confirmed the absence of border traps responses.

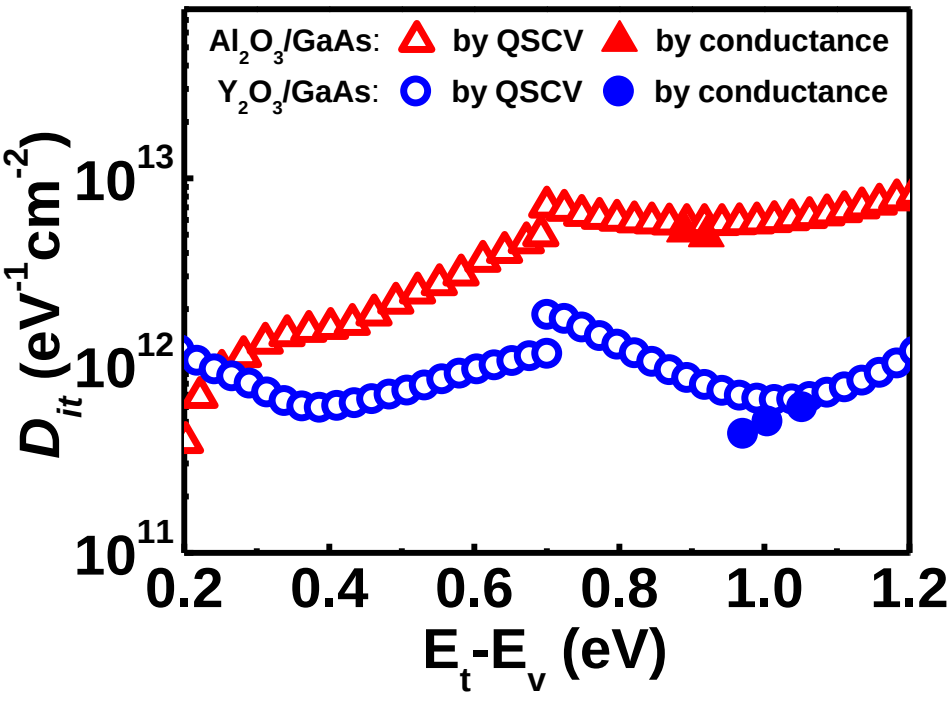

Fig 4.8 D_{it} spectra of ALD-Y_2O_3 and -Al_2O_3 on GaAs by QSCVs and GVs.

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Showing low density of states below $10^{12}cm^{-2}eV^{-1}$, Y_2O_3/GaAs hetero-structure show Dit spectrum without mid gap peaks. With high thermal stability, Y_2O_3/GaAs is promising for achieving inversion channel MOSFET with subthreshold swing under 75mV/dec. However, the trap density inside conduction band is still not detected yet. And we further measure some electrical properties at different temperature and analysis for Al_2O_3/Y_2O_3/GaAs samples.

4.4 Multiple temperature measurement of Y_2O_3/n-GaAs

4.4.1 Temperature dependence C-V C-F characteristic and barrier lowering

Some basic property for Semiconductor would vary with temperature, including thermal velocity, trap capture cross section, intrinsic carrier density, Fermi-level and etc. Moreover, as the trap capture time constant is longer at lower temperature, it is essential to measure to CV characteristic at low temperature to confirm the true carrier response. In Fig. 4-9, CVs at different measured temperature were shown, and true accumulation is reached according to CV measured at 77K. Since GaAs possess a very long minority carrier respond time, the inversion humps in CV measured at 423K is attributed to trap-induced capacitance response. Note that the larger frequency dispersion at elevated measure temperature and CV “stretch-out” were observed.

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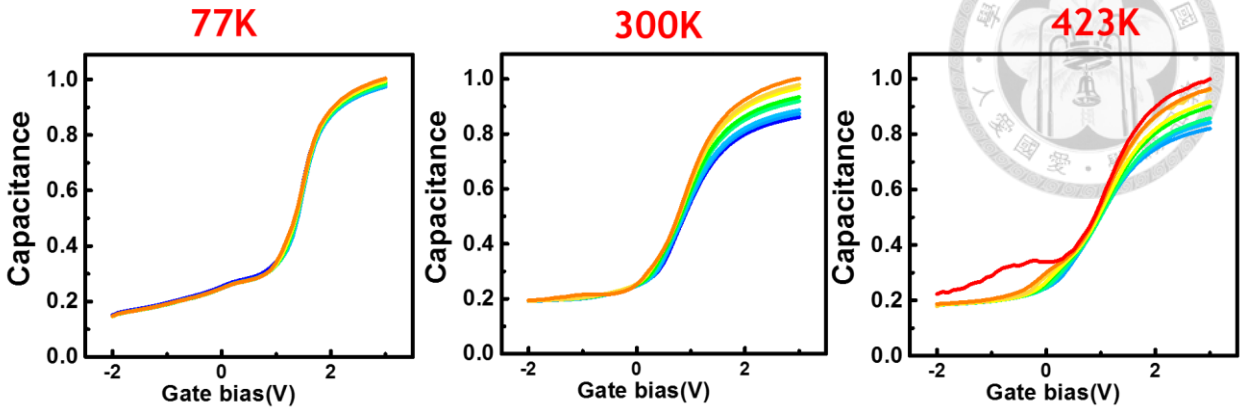

Fig. 4-9 CVs of Y_2O_3/n-GaAs at different temperature.

To understand the temperature dependence CV frequency dispersion, we have plotted the CF characteristic for different temperature in Fig. 4-10. Notice that capacitance values at 500kHz measured at different temperature is the same, indicative of true carrier response without trap response and trap time constant about 10^{-6} sec. However, as we mentioned above, the linear relation in the semi-log diagram indicates a constant spatial distribution of border traps. The border traps exchange charge with semiconductor through tunneling. Tunneling mechanism in itself is temperature independent. However, the temperature dependent frequency dispersion in CV

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measurement is commonly observed, with the origin no understood.

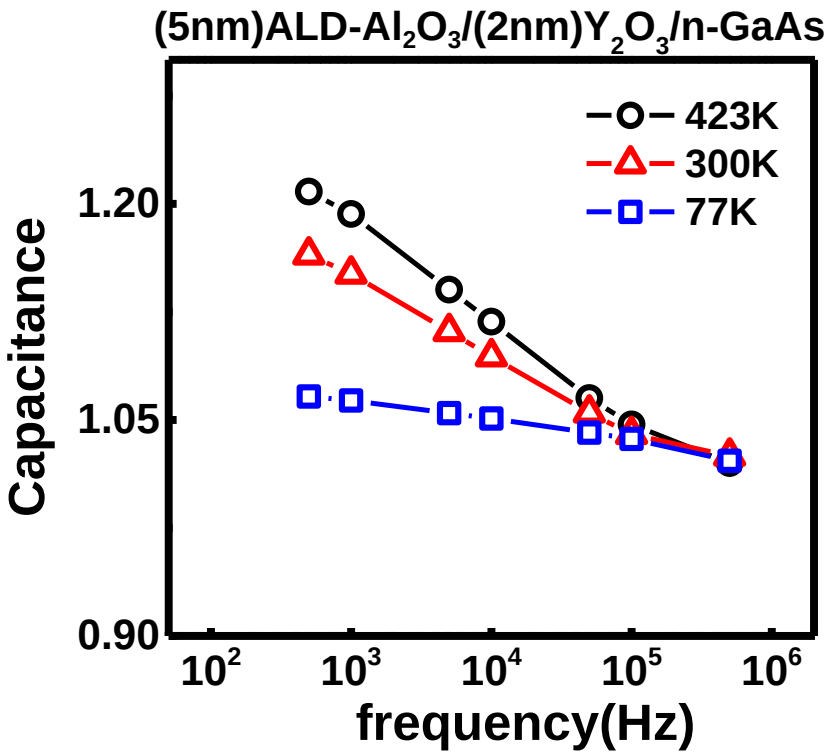

Fig. 4-10 CF characteristic of Y_2O_3/n-GaAs at different temperature

The reported work explained the phenomena through the change of capture cross section at different temperature. [22] Trap capture, is a multiple phonon emission process, and the capture cross section is given by [23].

$$\sigma_C = \sigma_C \exp(-\frac{\Delta E_b}{kT}) \tag{40}$$

Capture cross section is directly related to the trap time constant at interface, the time constant increase as temperature decrease and vice versa. We thus simulate the CF characteristic with different time constant to see the trend. The fixed parameter are dielectric constant κ=20, attenuation coefficient $\kappa = 7nm^{-1}$, semiconductor

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capacitance $C_s = 3 \times 10^{-6}F$, border traps density $N_{bt} = 1 \times 10^{20}cm^{-3}$ and C_{ox}=1.41 $\times 10^{-6}F$. The trap time constant at interface of $1 \times 10^{-11}s$, $1 \times 10^{-9}s$, $1 \times 10^{-7}s$ and $1 \times 10^{-5}s$ is plotted in Fig. 4-11.

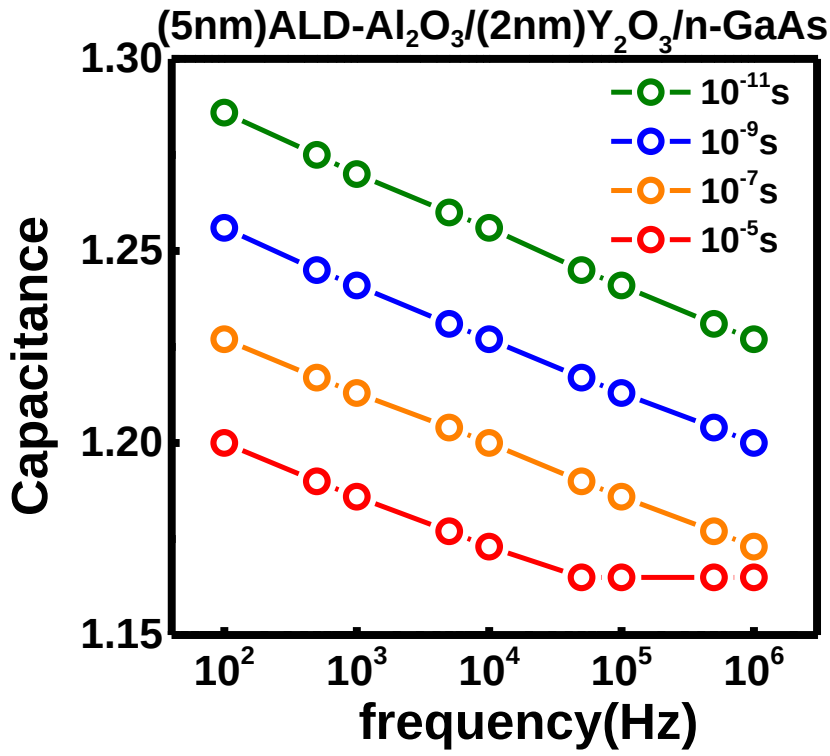

Fig. 4-11 CF simulation with fixed parameter of dielectric constant κ=20, $\kappa = 7nm^{-1}$, $C_s = 3 \times 10^{-6}F$, $N_{bt} = 1 \times 10^{20}cm^{-3}$, C_{ox}=1.41 $\times 10^{-6}F$ and traps time constant of $1 \times 10^{-11}s$, $1 \times 10^{-9}s$, $1 \times 10^{-7}s$ and $1 \times 10^{-5}s$ are plotted in red, orange, blue and olive, respectively.

The CF simulation of different time constant is not consistent with what we measured in Fig. 4-10. In Fig. 4-11, the slope of CF characteristic is unchanged for

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different time constant, while the measured CF characteristic shown a great difference in slope. Therefore, the change of capture cross section at different temperature cannot explain our data. We have to seek for the reason why the frequency dispersion is temperature dependent. The change of semiconductor capacitance and oxide capacitance slightly change with temperature, the left parameter is the attenuation coefficient κ. Now, we fixed the parameters dielectric constant κ=20, $C_s = 3 \times 10^{-6} F$, $N_{bt} = 1 \times 10^{20} cm^{-3}$, C_{ox}=$1.41 \times 10^{-6} F$ and traps time constant of $1 \times 10^{-10} s$. The attenuation coefficient of $3nm^{-1}$, $5nm^{-1}$,$7nm^{-1}$ and $9nm^{-1}$ is plotted in Fig. 4-12.

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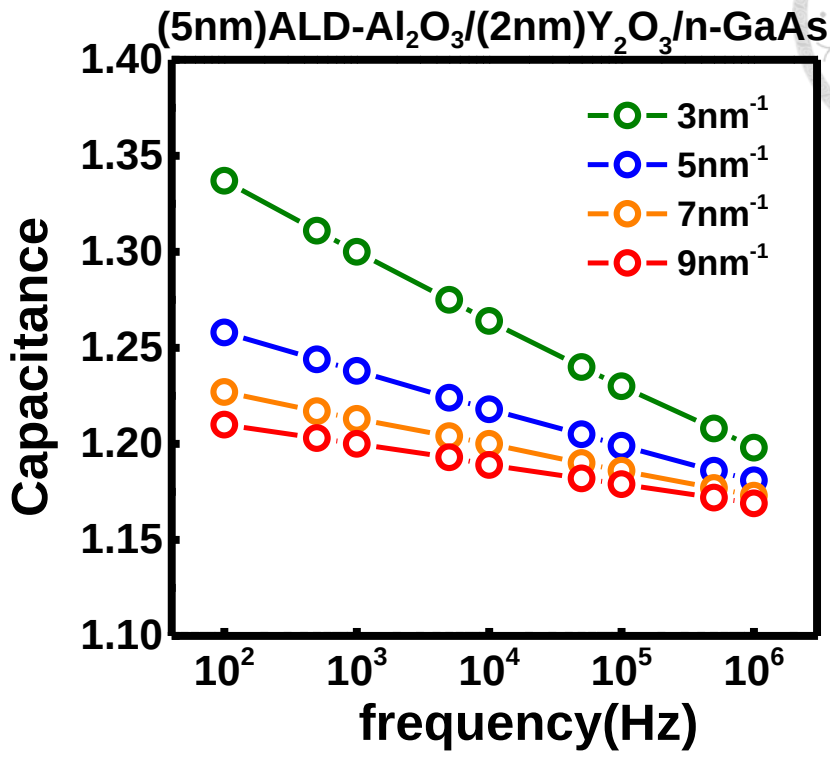

Fig. 4-12 CF simulation with fixed parameter of dielectric constant κ=20, traps time constant of $1 \times 10^{-7}s$, $C_s = 3 \times 10^{-6}F$, $N_{bt} = 1 \times 10^{20}cm^{-3}$, C_{ox}=$1.41 \times 10^{-6}F$ and attenuation coefficient of $9nm^{-1}$, $7nm^{-1}$,$5nm^{-1}$ and $3nm^{-1}$ are plotted in red, orange, blue and olive, respectively.

Now, the CF characteristic is much like the one we obtained in our measurement with different slope at different temperature, we concluded that change of attenuation coefficient at different temperature lead to temperature dependent frequency dispersion. The attenuation coefficient is determined by the conduction band offset as follows.

$$\kappa = \sqrt{2m(E_{offset})}/\hbar \qquad (41)$$

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The barrier of MOS structure has been reported to vary with temperature ($\phi(T) = \phi_0 - \gamma T$). The physical origin of the observed phenomena is still under debate. One explanation is the coupling between longitudinal and transverse components of the electron thermal energy. [24] The main idea is the difference of carrier effective mass between the oxide and semiconductor results in a reduction of barrier height of MOS devices. Another explanation is that temperature dependence of the observed macroscopic barrier height should be attributed to the thermal fluctuations of the microscopic local barrier height. [25] However, the physical origin is still under debated. We then measure J-E characteristic at different temperature to extract the barrier height in our system.

4.4.2 J-E characteristic and barrier height lowering

In this part, J-E characteristic of Y_2O_3/n-GaAs is measured at different temperature to deduce the relation between conduction band-offset and temperature. As mentioned in Chapter 2, there are three main conduction mechanism in oxide layer, including direct tunneling, FN tunneling and Shottky emission. Direct tunneling happens at thin oxide layer (<4nm), while our Al_2O_3/Y_2O_3/n-GaAs samples have 7nm thick oxide layer. As shown in Fig 4.13, the current is small even at elevated measure temperature, which is no

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consistence with Shottky emission J-E behavior that occurs at high temperature, low electrical field.

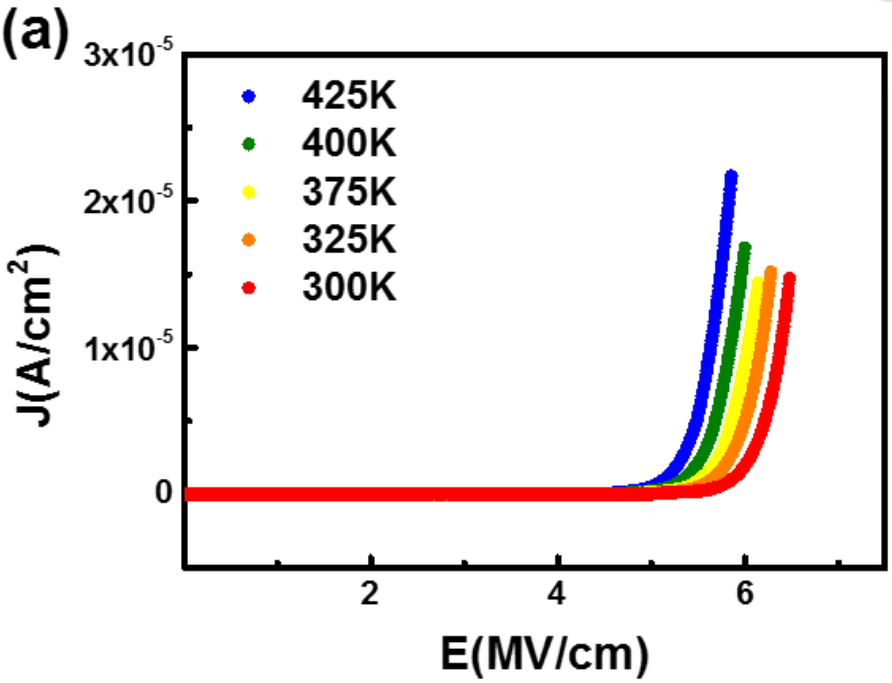

Fig. 4-13 J-E characteristic of Ni/Al_2O_3/Y_2O_3/GaAs at different temperature

FN tunneling curve, also called as field emission, occurs at large field. For a conventionally F-N tunneling, the $\ln\left(\frac{J}{E}\right)$ versus 1/E should be linear, and the barrier height is a function of the slope.

$$\text{slope} = -6.83 \times 10^7 \times \sqrt{\left(\frac{m_T}{m_0}\right)\phi_B^3} \tag{42}$$

Where ϕ_B is the barrier height, while m_T and m_0 is the tunneling mass and electron mass.

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But with a bilayer system of Al_2O_3/Y_2O_3/n-GaAs, we cannot directly use the conventional FN formula. As illustrated in Fig. 4-14, the tunneling barrier is not a triangular barrier. The band diagram is as follows

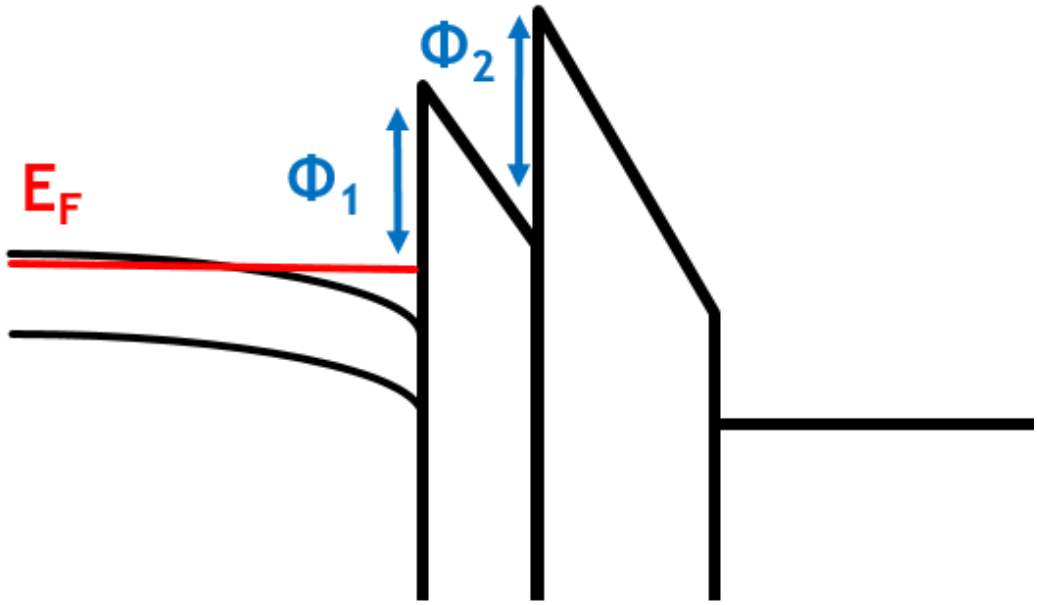

Fig. 4-14 Band diagram of Y_2O_3/n-GaAs at accumulation

Where ϕ_1 is the conduction band offset of GaAs and Y_2O_3, and ϕ_2 is the conduction band offset of Y_2O_3 and Al_2O_3. As mentioned, we assumed that the barrier seen by the electron inside GaAs for Y_2O_3 and Al_2O_3 is $\phi_1 - \gamma T$ and $\phi_1+\phi_2 - \gamma T$, respectively. In the reported study, band offset between Al_2O_3 and GaAs is 3.2eV, while band offset between Y_2O_3 and GaAs is 2.2 eV. The potential barier ϕ_2 is given by 1eV. [26, 27] The final formula for FN tunneling current and constant C are

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$$\mathrm{J} = \frac{4q\pi m}{h^3}\frac{(k_B T)^2}{C^2}\mathrm{T}(\mathrm{E}_F)\ , C \tag{43}$$

$$= k_B T\sqrt{\frac{8\pi^2 m}{h^2}}\sqrt{\int_0^{Turing\ points}\frac{1}{\sqrt{q\phi(x)-E_F}}dx}$$

There h is plank constant, $\mathrm{T}(\mathrm{E}_F)$ is the tunneling probability, E the electrical field and m the electron effective mass in dielectric ($0.25m_0$ for Y_2O_3 and Al_2O_3). Since the barrier is not a triangle barrier, the WKB approximation give the results of tunneling probability and C(no longer constant) are as follows

$$\mathrm{T}(\mathrm{E}_F) = \exp\left(-2\sqrt{\frac{8\pi^2 m}{h^2}}\sqrt{\int_0^{Turing\ points}\sqrt{q\phi(x)-E_F}\,dx}\right) \tag{43}$$

$$\mathrm{T}(\mathrm{E}_F) = \exp\left(-\frac{4}{3}\sqrt{\frac{8\pi^2 m}{h^2}}\frac{(q\phi_1)^{\frac{3}{2}}-(q\phi_1-2qE)^{\frac{3}{2}}+(q\phi_1+q)^{\frac{3}{2}}}{qE}\right) \tag{44}$$

$$C = k_B T\sqrt{\frac{8\pi^2 m}{h^2}}\frac{2((q\phi_1)^{\frac{1}{2}}-(q\phi_1-2qE)^{\frac{1}{2}}+(q\phi_1+q)^{1/2})}{qE} \tag{45}$$

Now, the $\ln(J/E^2)$ versus $1/E$ is no longer linear. The relation between $\ln(J\times C^2)$ versus $\frac{(q\phi_1)^{3/2}-(q\phi_1-2qE)^{\frac{3}{2}}+(q\phi_1+q)^{3/2}}{qE}$ should be linear with a slope of -3.43×10^7. By carefully fitting of the measurement curve as shown in Fig. 4-15 as

$$\mathrm{X}=\frac{(q\phi_1)^{3/2}-(q\phi_1-2qE)^{\frac{3}{2}}+(q\phi_1+q)^{3/2}}{qE} \tag{46}$$

$$\mathrm{Y}=\ln\left(\mathrm{J}\times k_B T\sqrt{\frac{8\pi^2 m}{h^2}}\left(\frac{2\left((q\phi_1)^{\frac{1}{2}}-(q\phi_1-2qE)^{\frac{1}{2}}+(q\phi_1+q)^{\frac{1}{2}}\right)}{qE}\right)^2\right) \tag{47}$$

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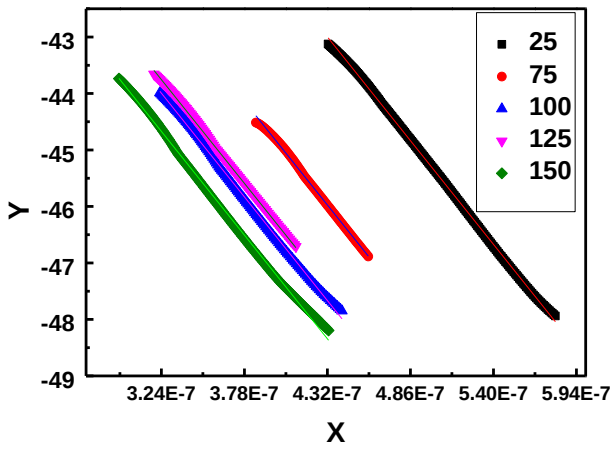

Fig. 4-15 Plot of the linear relation between X and Y

The only parameter is the conduction band offset ϕ_1. ϕ_1 at different temperature is plotted in Fig. 4-16 and listed in Table. 4-4. The slope of linear relation of $\phi_1(\mathrm{T}) = \phi_1(0) - \gamma T$, γ is about 4×10^{-3}eV/K.

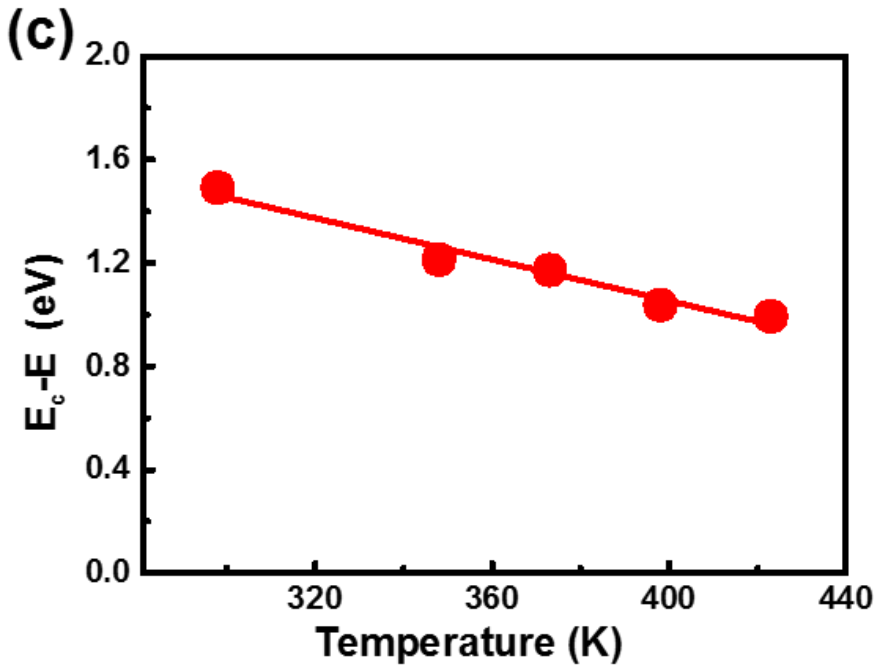

Fig. 4-16 The barrier height between Y_2O_3 and GaAs versus temperature

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Table. 4-4 List of barrier height versus temperature between Y_2O_3 and GaAs

^{O}C	K	ϕ_1(eV)
25	298	1.49
75	348	1.21
100	373	1.07
125	398	1.03
150	423	0.99

Clearly, the temperature dependence of barrier height is observed. If we use the $\phi_1(\mathrm{T}) = \phi_1(0) - \gamma T$ relation, $\phi_1(77)$ at 77K is 2.32eV, which is close to the barrier height of (2.2eV) measured by XPS measurement. We concluded that the temperature dependent barrier height have caused the temperature dependent frequency dispersion.

At last, the border trap density can be extracted by the frequency dispersion analysis, after carefully fitting with border traps and interfacial traps models. The trap density inside the conduction band is plotted in Fig. 4-17. Using the frequency dispersion analysis, trap inside conduction band that cannot be extracted from conventional method including conductance method and QSCV. Small amount of interfacial traps density is found near conduction band. In contrast, the border traps density boosted inside conduction band.

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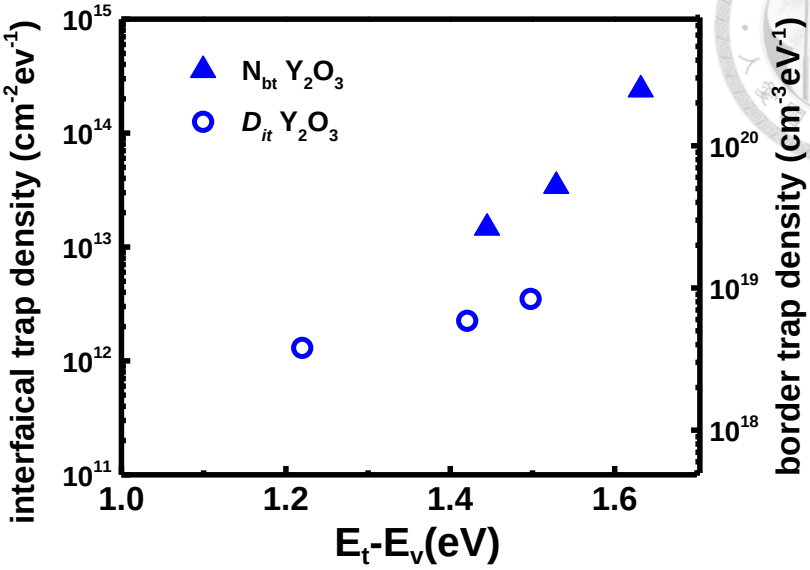

Fig. 4-17. Interfacial trap density D_{it} and border trap density N_{bt} were plotted on a log scale, on the left and right axis, respectively. The blue triangles show the border traps density, while the blue hollow circles show the interfacial trap density, respectively.

5. Conclusion

In the first part, we have compared the Y_2O_3/GaAs and Al_2O_3/GaAs interface. In conclusion, both oxides on GaAs showed typical CV at p-type samples. But for n-type samples, Y_2O_3 has effectively passivated the GaAs surface with extremely small frequency dispersion from depletion to accumulation, while large dispersion and stretch out is found in Al_2O_3/n-GaAs samples. Y_2O_3/GaAs interface showed an order lower interfacial traps density than Al_2O_3/GaAs extracted by QSCV and GV measurement. D_{it} spectrum without obvious mid gap peaks for Y_2O_3/GaAs interface.

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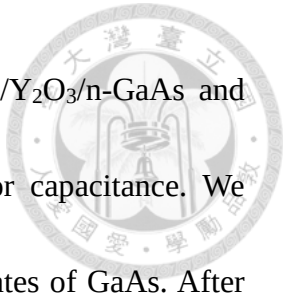

Next, we observed different maximum capacitance for Al_2O_3/Y_2O_3/n-GaAs and Al_2O_3/Y_2O_3/p-GaAs, which reveals the influence of semiconductor capacitance. We carefully studied the accumulation layer thickness and density of states of GaAs. After iteration of characterization, same oxide capacitance is observed in n- and p-Al_2O_3/Y_2O_3/GaAs. After the characterization, CF characteristic is simulated and compared with experiments. The linear relation in the semi-log diagram for Y_2O_3/n-GaAs indicates border traps dominated condition. While the convex curve is observed for Al_2O_3/n-GaAs in CF characteristic, indicative of interfacial traps dominated condition.

In the final parts, we observed temperature dependent frequency dispersion. Most reported works explain the phenomena by change of capture cross section with temperature. However, with the simulation of CF characteristic, the change of time constant cannot explain the measured results. Instead, the change of barrier height can explain our data. We confirmed the barrier height lowering by measuring the FN tunneling in MOS structure and deduce the barrier height at room temperature and high temperature. At last, the border traps and interfacial trap density is extracted by frequency dispersion analysis, and a high border traps density is observed inside conduction band.

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References

1. Y. C. Chang, W. H. Chang, C. Merckling, J. Kwo, M. Hong, Appl. Phys. Lett. 102 (2013) 093506
2. G. Brammertz, H.C. Lin, K. Martens, D. Mercier, S. Sioncke, A. Delabie, W.E. Wang, M. Caymax, M. Meuris, M. Heyns, Appl. Phys. Lett. 93 (2008) 183504
3. T. Aoki, N. Fukuhara, T. Osada, H. Sazawa, M. Hata, and T. Inoue Appl. Phys. Lett. 105 (2014) 033513.
4. H. Hasegawa, T. Sawada, IEEE Trans. Electron Dev. 27 (1980) 1055-1061.
5. Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P.C. McIntyre, P.M. Asbeck, M.J.W. Rodwell, Y. Taur, IEEE Electron Device Lett. 32 (2011) 485-487.
6. H.P. Chen, Y. Yuan, B. Yu, J. Ahn, P.C. McIntyre, P.M. Asbeck, M.J.W. Rod IEEE Trans. Electron Dev. 59 (2012) 2383.well, IEEE Trans. Electron Dev. 59 (2012) 2383-2389.
7. R.V. Galatage, D.M. Zhernokletov, H. Dong, B. Brennan, C.L. Hinkle, R.M. Wallace, E.M. Vogel, J. Appl. Phys. 116 (2014) 014054.
8. S. Gu, J. Min, Y. Taur, P.M. Asbeck, Solid-State Electron. 118 (2016) 18-25.
9. K. H. Shiu, C.H. Chiang, Y.J. Lee, W.C. Lee, P. Chang, L.T. Tung, M. Hong, J. Kwo, W. Tsai, J. Vac. Sci. Technol. B 26 (2008) 1132-1135.
10. H. R. Huff, A. Hou, C. Lim, Y. Kim, J. Barnett, G. Bersuker, G. A. Brown, C. D. Young, P. M. Zeitzoff, J. Gutt, P. Lysaght, M. I. Gardner, and R. W. Murto, *Microelectron. Eng.* 69, 152 (2003).
11. S. P. Murarka, Appl. Phys. Lett. 26, 180 (1975)
12. N. Taoka, M. Yokoyama, S.-H. Kim, R. Suzuki, S.-H. Lee, R. Iida, T. Hoshii, W. Jevasuwan, T. Maeda, T. Yasuda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, Appl. Phys. Lett. 103, 143509 (2013).
13. G. Brammertz, H.-C. Lin, K. Martens, D. Mercier, S. Sioncke, A. Delabie, W. E. Wang, M. Caymax, M. Meuris, and M. Heyns, Appl. Phys. Lett. 93, 183504 (2008).
14. T. Aoki, N. Fukuhara, T. Osada, H. Sazawa, M. Hata, and T. Inoue Appl. Phys. Lett. 105 (2014) 033513.
15. K. J. Morton, G. Nieberg, S. Bai, S. Y. Chou, Nanotech. 19 (2008) 345301
16. W. G. Spitzer and J. R. Ligenza, J. Phys. Chem. Solids 17, 196 (1961)
17. E.H. Nicollian and J. R. Brews, MOS Physics & Technology ~Wiley, New York, 1982!
18. F.-C. Chiu, Adv. Mater. Sci. Eng., vol. 2014, 1–18 (2014)

doi:10.6342/NTU201704148

19. C. N. Berglund IEEE Trans. Electron Dev, 13 (1966) 701-705
20. S.Y. Wu, K.H. Chen, Y.H. Lin, C.K. Cheng, C.H. Hsu, J. Kwo, M. Hong, Microelectron. Eng. 147 (2015) 310-313
21. S. Takagi, IEEE Trans. Electron Dev, 42 (1995) 2125-2130
22. A. Vais, H. C. Lin, C. Dou, K. Maetens, T. Ivanov, Q. Xie, F. Tang, M, Givens, J, Maes, N, Collaert, J. P. Raskin, K. Demeyer, A. Thean, Appl. Phys. Lett. 107, 053504 (2015)
23. C. H. Henry, D. V. Lang, Phys. Bev. B 15, 989
24. L. F. Mao, Appl. Phys. Lett. 90, 183511 (2007)
25. D. Schroeder, A. Avellen, Appl. Phys. Lett. 82, 4510 (2003);
26. M.L. Huang, Y C. Chang, C.H. Chang, T. D. Lin, J. Kwo, M. Hong, Appl. Phys. Lett. 89 (2006) 012903.
27. C.L. Hinkle, C. Fulton, R.J. Nemanich, G. Lucovsky, Microelectron. Eng. 72 (2004) 257–262

Appendix – Dry etching of (5nm)Al_2O_3/(2nm)Y_2O_3 bi-layer oxide stack

Inductive coupled plasma reactive ion etching (ICP-RIE) is an etching technique combine both chemical reactions etching and ion-induced etching. In comparison with wet etching process, dry etching has the advantage of selective etching along vertical direction and forms an anisotropy profile. In general, there are two etching mechanism in ICPRIE process, one is physical bombardment and the other is chemical reactions. There is no selectivity of ion bombardment, the selectivity removal of surface atoms is achieved by plasma-induced gaseous etchant atoms chemically reacts with surface. Taking consideration of ultra-thin thickness in sub-10nm for high-κ dielectrics and complicated

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geometry for device structure, dry etching is much more suitable than wet etching owing to its precise control on etching rate and anisotropic etching profile.

In this part, we tested different recipes for dry etch of Al_2O_3/Y_2O_3 bi-layer stacks before and after 900°C 60s annealing. And we have found that the bi-layer Al_2O_3/Y_2O_3 oxide stacks are extremely hard to etch after 900°C 60s annealing. To determine the etching thickness, we used lithography to define the etched and not etched region, and atomic force microscopy (AFM) to determine the etched thickness.

1. Dry etching of Al_2O_3/Y_2O_3 without 900°C annealing

First, we study the etching of Al_2O_3/Y_2O_3 bi-layer before high temperature annealing. We use BCl_3 as etchant because Y_2O_3 and Al_2O_3 can be react with Cl-based etchant, forming YCl_3 and Al_2Cl_6 byproducts. The recipe is 5sccm BCl_3/15sccm Ar under 20W RF bias for 20s. The etching depth is about 7nm as shown in Fig 1. Using BCl_3/Ar plasma, the bi-layer stacks can be easily etched.

Etch recipe: 5sccm BCl_3 + 15sccm Ar under 20W RF bias

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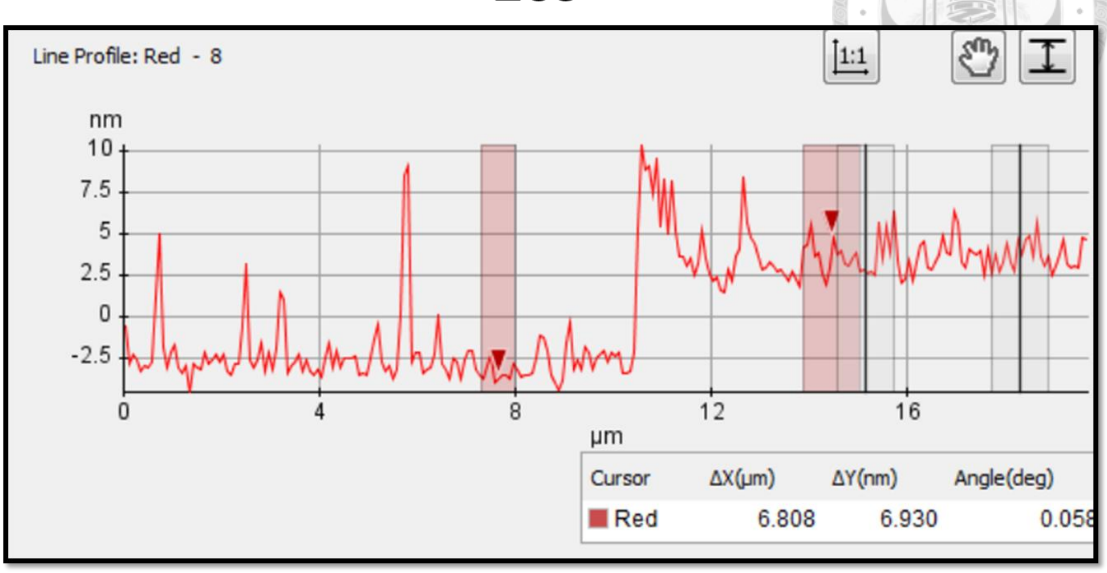

Fig 1. Etching profile of (5nm)Al_2O_3/(2nm)Y_2O_3 without high temperature annealing using BCl_3/Ar measured by AFM

2. Dry etch of Al_2O_3/Y_2O_3 after 900°C annealing

2-1. Recipe of 30sccm CHF_3 15W RF bias

CHF_3 is used for etching Al_2O_3 in previous work. Thus, we first try the CHF_3 dry etching recipe for etching Al_2O_3/Y_2O_3 bi-layer stacks after 900°C annealing. After 60s, 120s, 180s and 240s of dry etching, the etched depth is 2.6nm, 4,7 nm, 6.3nm and 6.4nm, respectively as shown in Fig 2. It is shown that the etching end is at about 6.4nm with CHF_3 as etchant.

Etch recipe: 30sccm CHF_3 under 15W RF bias

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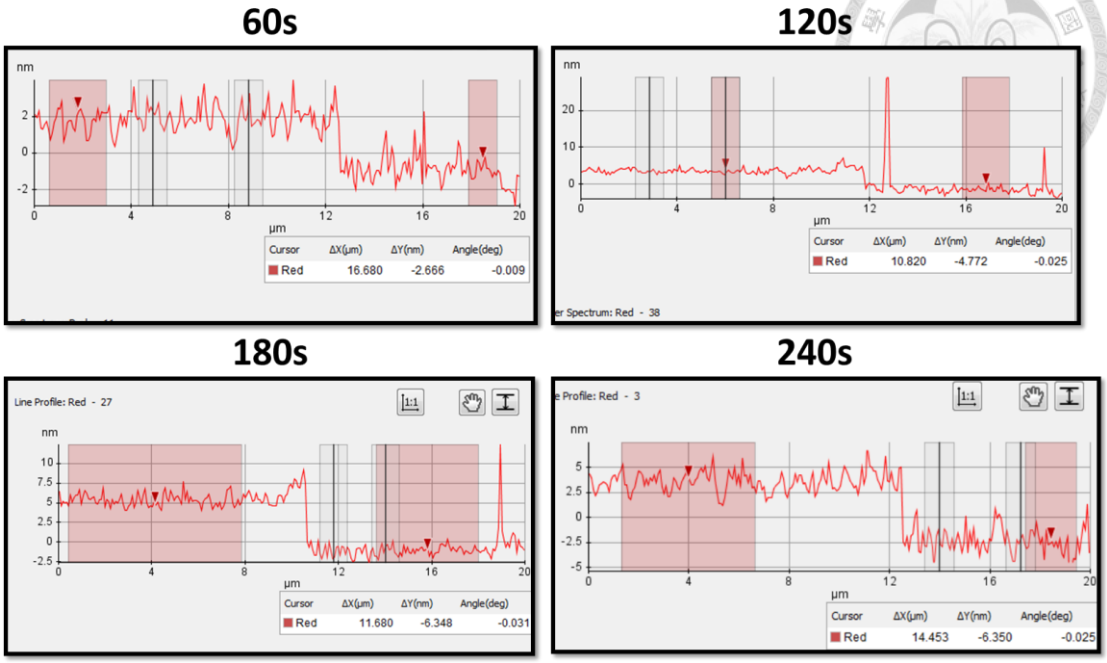

Fig 2. Etching profile of (5nm)Al_2O_3/(2nm)Y_2O_3 after 900°C annealing using CHF_3 measured by AFM

2-2. Recipe of 5sccm BCl_3/15sccm Ar under 20W RF bias

Based on the result above, the BCl_3/Ar plasma can easily etch Al_2O_3/Y_2O_3 bi-layer oxide. Moreover, using BCl_3 was more controllable than Cl_2, which avoid the over etch of Ⅲ-Ⅴ substrate. Therefore, we tried the recipe of BCl_3/Ar plasma. After 30s, 50s and 70s BCl_3/Ar plasma etching, the etching depth were 5.4nm, 6.0nm and 6.1nm, respectively. Both BCl_3/Ar and CHF_3 cannot etch the whole Al_2O_3/Y_2O_3 bi-layer after high temperature annealing.

Etch recipe: 5sccm BCl_3 + 15sccm Ar under 20W RF bias

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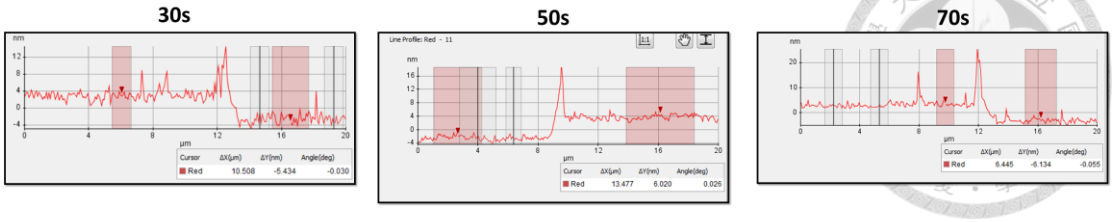

Fig. 3 Etching profile of (5nm)Al_2O_3/(2nm)Y_2O_3 after 900°C annealing using BCl_3/Ar measured by AFM

2-3. Two step etching

Since the above recipe cannot etch the (5nm)Al_2O_3/(2nm)Y_2O_3 after 900°C annealing. We believed that some compound was formed at the interface of Y_2O_3 and Al_2O_3 after 900°C annealing. We thus have to use the BCl_3/Cl_2 plasma, which would etch our GaAs substrate with a very fast rate. To avoid over etching, we used two steps etch. At the first step, we etch the rest capping Al_2O_3 using BCl_3/Ar plasma, and then we use BCl_3/Cl_2 plasma to etch the rest oxide stack. According to the above result, etch end is reached after 30s etching under BCl_3/Ar plasma. So we use BCl_3/Ar 30s as the first step of etching. After the first step, different etching time using 5sccm BCl_3/15sccm Cl_2 under 30W bias was conducted as shown in Fig 3. It was shown that the etched depth was 8.4nm, 6.9nm, 15nm and 1204.7nm after 30s, 40s, 50s and 80s for BCl_3/Cl_2 plasma. Note that after 40s etched, deep holes were observed in the AFM profile, showing poor selectivity

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of Al_2O_3/Y_2O_3 bi-layer over GaAs substrate. The poor reproducibility and poor selectivity over gate dielectric through GaAs make the process uncontrollable.

Etch recipe: (1) 5sccm BCl_3 + 15sccm Ar under 20W RF bias 20s

(2) 5sccm BCl_3 + 15sccm Cl_2 under 30W RF bias

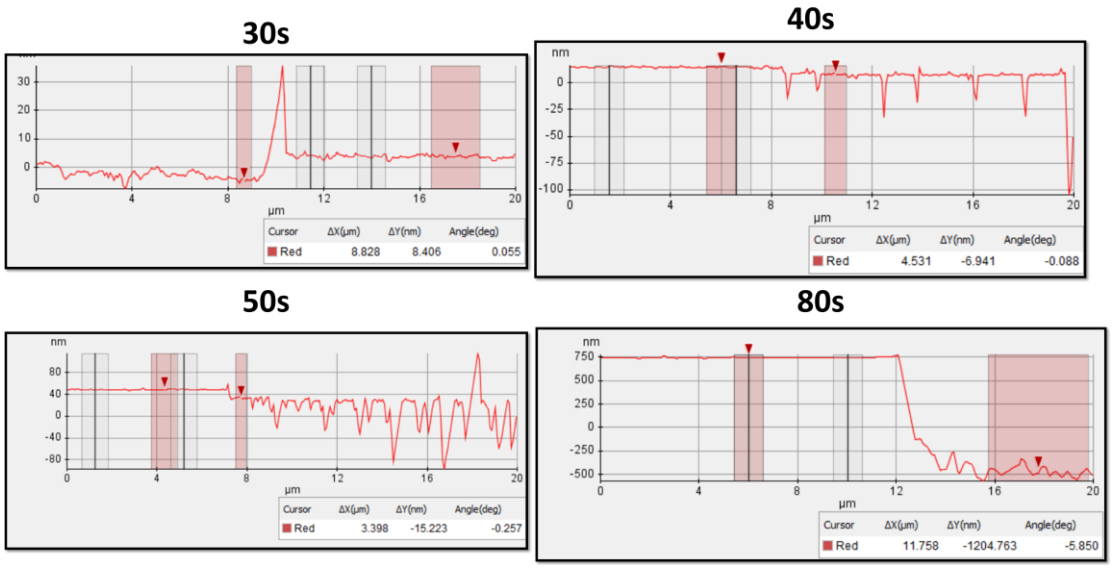

Fig 3. Etching profile of (5nm)Al_2O_3/(2nm)Y_2O_3 after 900°C annealing using first step of BCl_3/Ar plasma and second step of BCl_3/Cl_2 plasma measured by AFM

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