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Master Thesis

具電感電流均流校正技術之快速鎖定延遲鎖定迴路應用於暫態調變固定導通時間控制之四相位降壓型轉換器

An Inductor Current Balancing Technique for Fast-locking Delay-locked Loop Based Four-phase Buck Converter with Transient-modulated Constant On-time Control for Fast Load Transient Response

葛致杰

Chih-Chieh Ko

指導教授：陳中平 博士

Advisor：Charlie, Chung-Ping Chen, Ph.D.

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An Inductor Current Balancing Technique for Fast-locking
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英文審定書

An Inductor Current Balancing Technique

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By

Chih-Chieh Ko

THESIS

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摘要

本論文提出了一個快速鎖定延遲鎖定迴路應用於暫態調變固定導通時間控制之四相位降壓型轉換器，並且提出了一個新穎的電感電流均流校正技術，稱為脈衝寬度縮減技術，其可同時校正多相位轉換器中各相位脈衝寬度調變信號的責任週期與相位差。

為了達到更快速的負載暫態響應，我們在延遲鎖定迴路中，採用改良式的雙緣觸發之相位偵測器，亦即自動切換單／雙緣觸發之相位偵測器，藉以達成快速鎖定的機制。

本研究使用之降壓型轉換器，操作於一千萬赫茲之切換頻率，並使用三百三十奈米亨利之電感與二十二微米法拉之電容。輸入電壓為三點三伏特，輸出電壓為一點八伏特，而負載電流範圍為零點四安培到一點四安培。本作品在台積電零點一八微米互補式金屬氧化物半導體製程下，佔晶片面積六點一七毫米平方公尺。

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Abstract

This thesis presents a fast-locking delay-locked loop (DLL) based four-phase DC-DC buck converter, which is manipulated by transient-modulated constant on-time control (TMCOT). Besides, a novel inductor current balancing method called pulse-width-shrunk technique (PWST) is proposed and it is capable of simultaneously calibrating the duty cycle and the phase error of pulse-width modulation (PWM) signals in the DLL-based multi-phase converter.

For the sake of much faster load transient response, the DLL adopts a modified dual edge triggered phase detector (DET-PD), namely automatic switching single/dual edge triggered phase detector (ASS/DET-PD), to accomplish the fast-locking mechanism.

The buck converter is operated at 10 MHz switching frequency, and it employs a 330 nH inductor and a 22 μF output capacitor. The input voltage is 3.3V, and the output voltage is 1.8V. The load current ranges from 0.4A to 1.4A. The fully-integrated circuit is implemented in TSMC 0.18-μm CMOS process and the chip area is 6.17mm^2.

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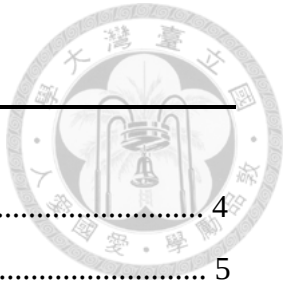

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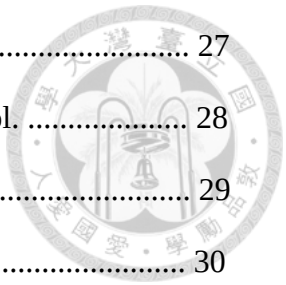

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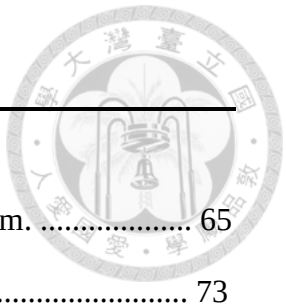

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Chapter1 Introduction

1-1 Research Motivation

Over the past decades, DC-DC converters have developed vigorously and flourished in the field of power management IC. Nowadays, to get high performance computing (HPC), CPUs, especially in the advanced low-voltage CMOS process, not only need more rapid load transient response, but should also have the capability for operating a wide range of load currents. Furthermore, reaching high efficiency is another momentous issue in power conversion systems, whose applications include recently prevalent portable and mobile devices. With more and more diverse and complicated demands of electronic systems, single-phase DC-DC converters are gradually not able to satisfy all kinds of requirements. As a result, multi-phase DC-DC converters are used to overcome those problems.

Compared to single-phase architectures, multi-phase converters provide a better output voltage ripple [1], shorter load transient response time [2], [3], and lower conduction loss. However, in the multi-phase structure, if unequal currents flow across each phase of power-trains, the efficiency of the converter will severely degrade [4]. In addition, duty cycle and phase mismatch among the individual phases also abates the effect of output voltage ripple cancellation, which afterwards deteriorates the load transient response. Hence, the balance of inductor currents in each phase is very crucial for multi-phase converters.

There are two fundamental solutions to current balancing. The first method is so-called passive current sharing, which is based on duty cycle calibration [5], [6]. Nevertheless, it only matches the duty cycle of pulse-width modulation (PWM) signals in each phase, but the inductor currents are still uneven as a result of

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component mismatch and parasitic elements through every path. The other approach that is referred to as active current sharing is the most common way to balance currents [2], [7], [8]. At the beginning, it senses the average inductor current of each phase. Next, comparing with one another, and finally calibrating the PWM signals to make the current equivalent. However, although the mean currents become the same, we still cannot ensure whether each of PWM signals has precise and constant phase error. For instance, in four-phase converters, every PWM signal should be accurately separated by an identical phase error of 90^{o}. Yet, if different phase errors occur between four PWM signals, the ability to suppress ripples will be diminished.

In order to concurrently calibrate the duty cycle and the phase error of PWM signals, we demonstrate an innovative inductor current balancing means, called pulse-width-shrunk technique (PWST). Firstly, we use an interior DLL to complete four-phase synchronization with an exact phase error of 90^{o}. Secondly, the proposed current balancing circuit will calibrate the duty cycle of the DLL outputs according to the sensed four-phase inductor currents. In this way, we can attain the adjustment of the duty cycle and the phase error at the same time. Moreover, for the purpose of much quicker load transient response, the DLL is designed as a fast-locking architecture, whose core circuit is composed of an automatic switching single/dual edge triggered phase detector (ASS/DET-PD). Eventually, we also employ the transient-modulated constant on-time control (TMCOT) to resolve the slow transient response problem in normal COT converters.

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1-2 Thesis Overview

Apart from the introduction and the motivation in Chapter1, the remainder of this thesis contains the following. Chapter 2 begins with a brief overview of a DC-DC buck converter and the control methods. Chapter 3 expresses a single-phase converter associated with the proposed TMCOT control mechanism and its implementation. Then, chapter 4 introduces the proposed four-phase buck converter, including the operation of fast-locking DLL, the principle of inductor current balancing technique, and the numerical analysis of the related research topics. After that, the simulation and measurement results are illustrated in chapter 5; ultimately, chapter 6 states the conclusion and future works.

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Chapter2 Fundamentals of DC-DC Buck Converter

2-1 Operation Concept of Buck Converter

An elementary buck converter, which comprises a single-pole double-throw (SPDT) and a LC low pass filter, is responsible for DC-to-DC power conversion and steps down the input voltage (V_{IN}) to the output voltage (V_{OUT}) [9].

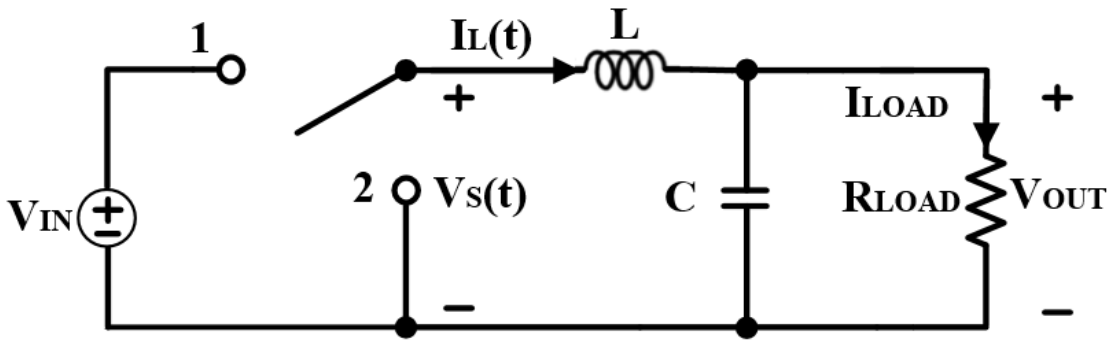

Fig. 2.1 A simple buck converter circuit.

As shown in Fig. 2.1, when the switch is in the position 1, the switching node voltage $V_S(t)$ equals the source voltage V_{IN}, and $V_S(t)$ becomes zero while the switch transfers to the position 2. It should be mentioned here that two switches cannot be turned on simultaneously since concurrent conduction will drain the energy from input source to the ground and result in a tremendous energy loss. The switch node shifts periodically, which leads $V_S(t)$ to a periodic rectangular waveform. As the switching cycle repeats endlessly, a fixed switching frequency occurs. We then define the switching frequency f_S and switching period $T_S = 1 / f_S$ so that we can describe the behavior of $V_S(t)$ as Fig. 2.2. The duty cycle D means the ratio of the time in which the switch keeps in the position 1, and thus $0 \leq D \leq 1$. Oppositely, the complement of the duty cycle, D′, denotes the fraction of the time when the switch stays in the

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position 2, and is also depicted as (1 - D).

$$D = \frac{Turn{-}on\ time\ of\ switch\ in\ position\ 1}{T_S}, 0 \le D \le 1 \quad (2.1)$$

$$D' = 1 - D \quad (2.2)$$

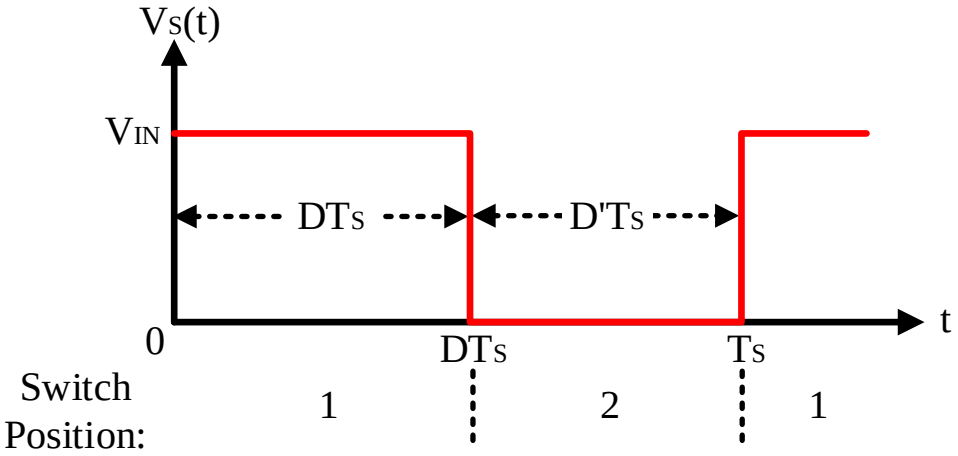

Fig. 2.2 The periodic waveform of Vs(t).

Through the Fourier analysis, we realize that the dc component of a periodic rectangular waveform $V_S(t)$ is equivalent to its average value $<V_S>$, which is given by:

$$< V_S >= \frac{1}{T_S}\int_0^{T_S} V_S(t)dt \quad (2.3)$$

Calculate the area under the curve in Fig. 2.2 to obtain the integral value of Eq. (2.3), we can acquire the following equation:

$$< V_S >= \frac{1}{T_S}(DT_S V_{IN}) = DV_{IN} \quad (2.4)$$

From Eq. (2.4), we can know that the dc component of $V_S(t)$ is equal to the input source voltage multiplied by the duty cycle, i.e., the switch decreases the input voltage by a factor of D times.

Recall that Fig. 2.1 illustrates a LC low pass filter that allows the dc component of $V_S(t)$ to pass, but blocks the components at the switching frequency and harmonics. In

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consequence, the output voltage $V_{OUT}(t)$ is substantially identical to the dc component of $V_S(t)$.

$$V_{OUT}(t) \approx < V_S > = DV_{IN} \tag{2.5}$$

Finally, from the converter pictured in Fig. 2.1, which employs lossless elements, we can draw the output characteristic of a fundamental buck converter in terms of the duty cycle according to Eq. (2.5).

Fig. 2.3 manifests that because $0 \leq D \leq 1$, the output voltage V_{OUT} of a buck converter has lower or equal value in contrast to the input voltage V_{IN}.

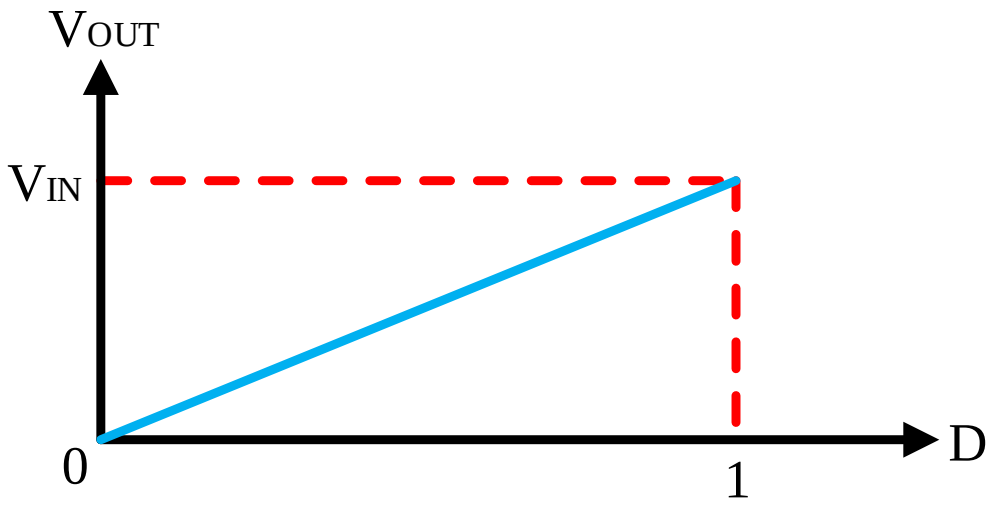

Fig. 2.3 The dc output voltage V_{OUT} of a buck converter in terms of the duty cycle D.

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2-2 Fixed-frequency Control

In a typical dc-dc converter application, no matter how the input voltage $V_{IN}(t)$ or the load current $I_{LOAD}(t)$ alter, the output voltage $V_{OUT}(t)$ should always keep invariable. As a result, constructing a feedback system does help achieve the object.

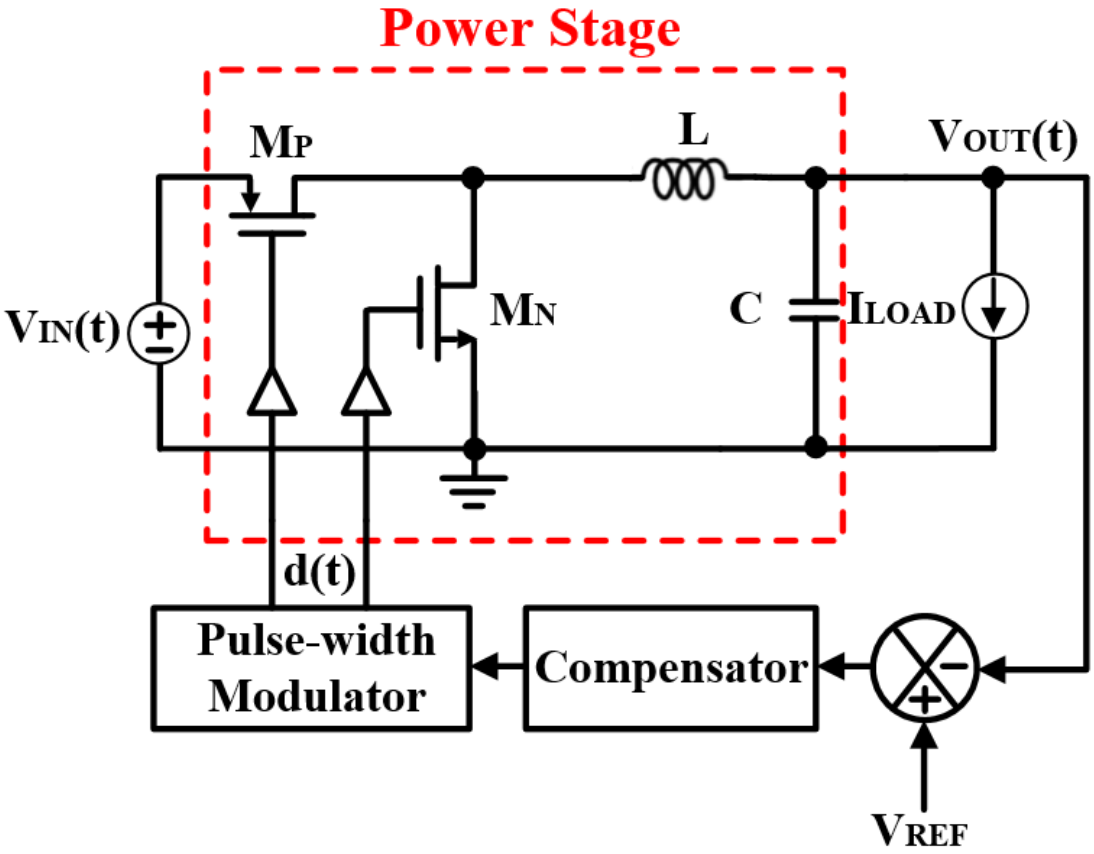

Fig. 2.4 Block diagram of a standard buck converter system.

Fig. 2.4 is a standard buck converter system. Aside from the power stage mentioned above, there additionally involves three primary blocks in the system. The first one is a subtractor used to extract the difference between the output voltage $V_{OUT}(t)$ and a reference voltage V_{REF} ,which is usually generated by a bandgap circuit. The second is a compensator accounting for producing feedback signals. The last one is a pulse-width modulator that generates a control signal to manage the power stage. The classification of the control methods can be enumerated into two main categories [10]:

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fixed-frequency control and ripple-based control. The fixed-frequency control requires a clock signal to define the switching frequency, and it contains voltage-mode control ,which provides a basic voltage feedback, and current-mode control, which needs an extra path with current-sensing information. Contrarily, instead of requiring an exterior clock signal to trigger the start of each switching cycle, the ripple-based control has a variable switching frequency, and it can also be classified into hysteretic control, constant off-time control, constant on-time control and V-square (V^2) control.

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2-2-1 Voltage-mode Control (VMC)

Fig. 2.5 demonstrates a common voltage-mode controlled buck converter. An error amplifier is manipulated to amplify the difference between the feedback output voltage and the reference voltage, and then produces an error signal $V_C(t)$ to control the change of the duty cycle. For example, when the output voltage $V_{OUT}(t)$ increases, the output of the negative feedback error amplifier $V_C(t)$ decreases. Then, the duty cycle d(t) accordingly reduces, which causes the decrease of $V_{OUT}(t)$. Eventually, the output voltage is adjusted back to be stable, i.e., $V_{OUT}(t) = V_{REF}$.

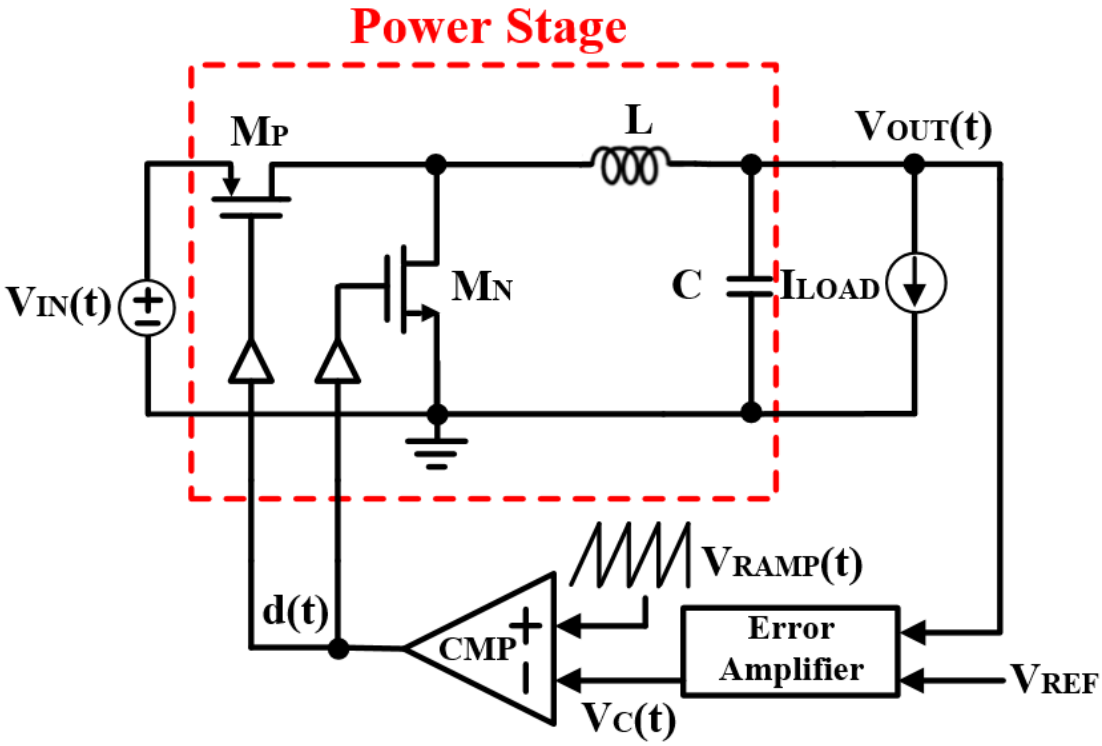

Fig. 2.5 A voltage-mode controlled buck converter.

To accomplish fixed-frequency control, the clock signal CLK(t) determines the switching frequency and indicate the beginning of each switching cycle. The ramp signal $V_{RAMP}(t)$, which is synchronized to CLK(t), is compared with $V_C(t)$ to generate the duty cycle d(t), as pictured in Fig. 2.6. When $V_{RAMP}(t)$ is smaller than $V_C(t)$, d(t) is high, M_P turns on, and M_N turns off. On the contrary, when $V_{RAMP}(t)$ becomes higher

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than $V_C(t)$, d(t) shifts to low, then M_P turns off, and M_N turns on. Therefore, because the buck converter keeps steady by means of the output voltage feedback, this control method is called voltage-mode control.

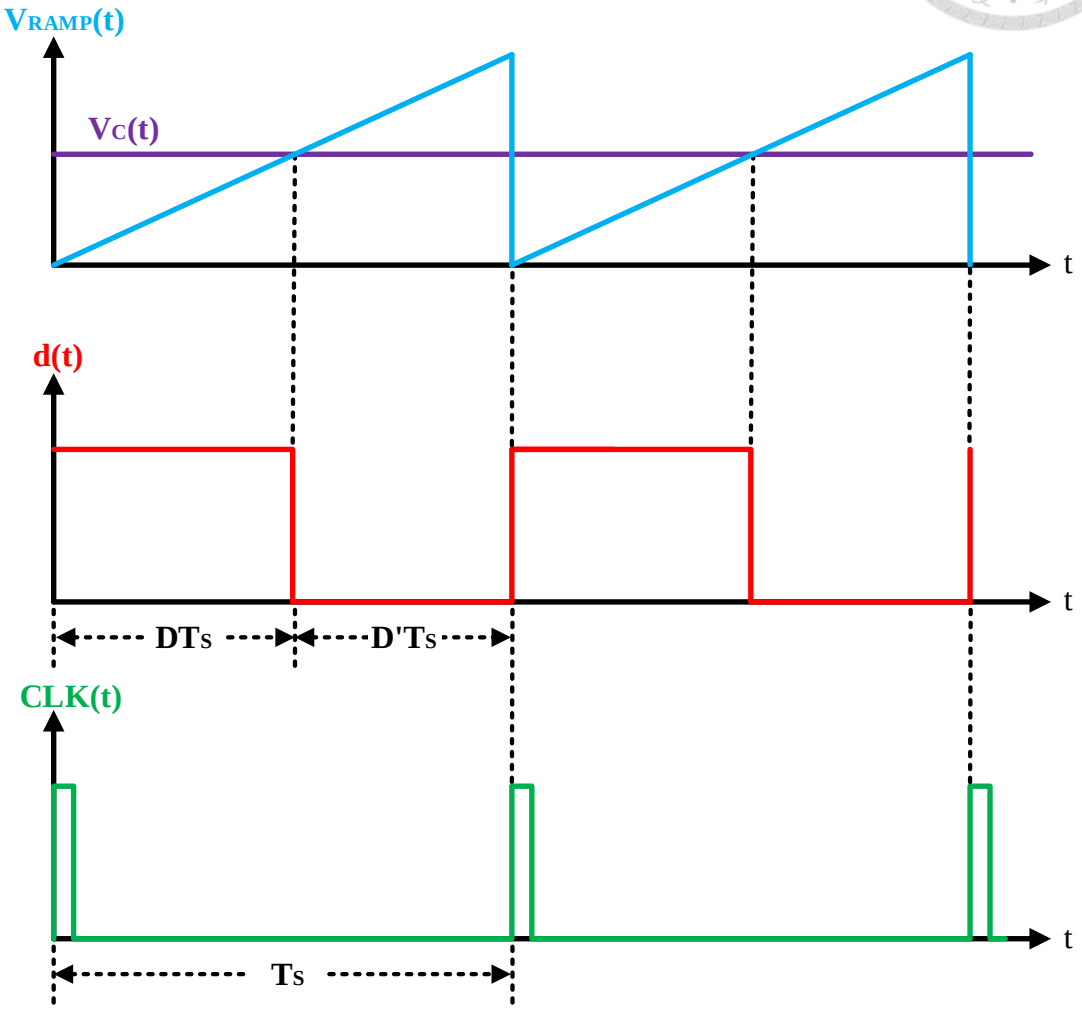

Fig. 2.6 The operation of the voltage-mode controlled buck converter.

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2-2-2 Current-mode Control (CMC)

Excluding the previously mentioned circuit blocks in voltage-mode control in Fig. 2.5, a sensed inductor current V_{Lx} is coupled with V_{RAMP} to yield a summation voltage V_{SUM}. Unlike solely one loop in voltage-mode control, there are two loops in current-mode control, including inner current loop and outer voltage loop, as drawn in Fig. 2.7.

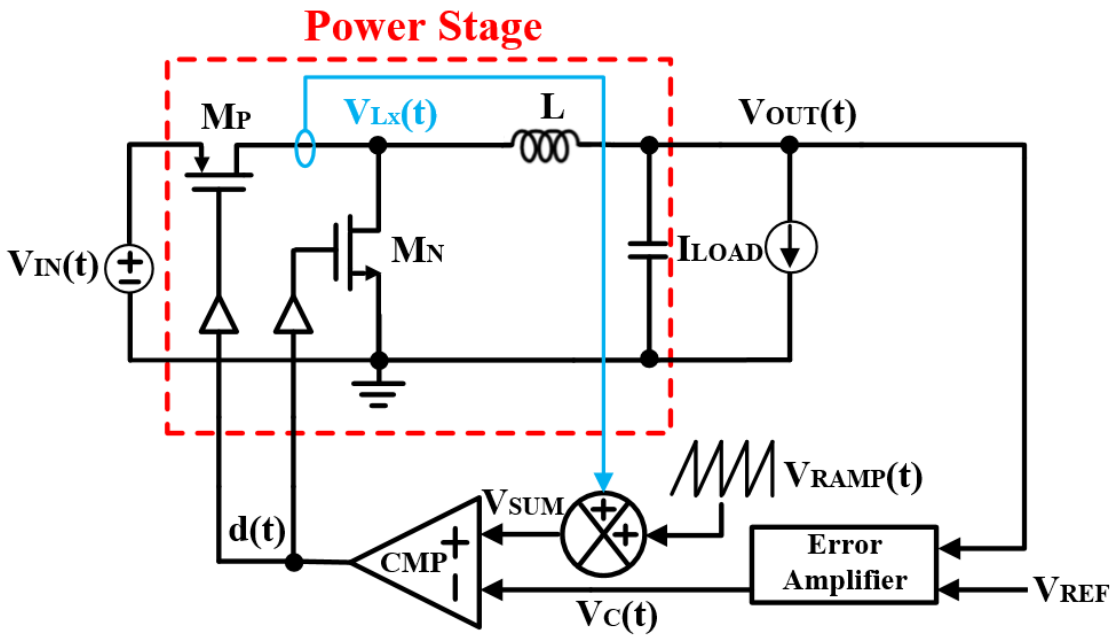

Fig. 2.7 A current-mode controlled buck converter.

Instead of directly comparing $V_{RAMP}(t)$ with $V_C(t)$ to deciding d(t) as voltage-mode control, the current-mode control compares the sensed inductor current $V_{Lx}(t)$ plus $V_{RAMP}(t)$ to $V_C(t)$. For more easy understanding, here we use $V_C(t)$ minus $V_{RAMP}(t)$ to present the operation waveform, as Fig. 2.8 shows.

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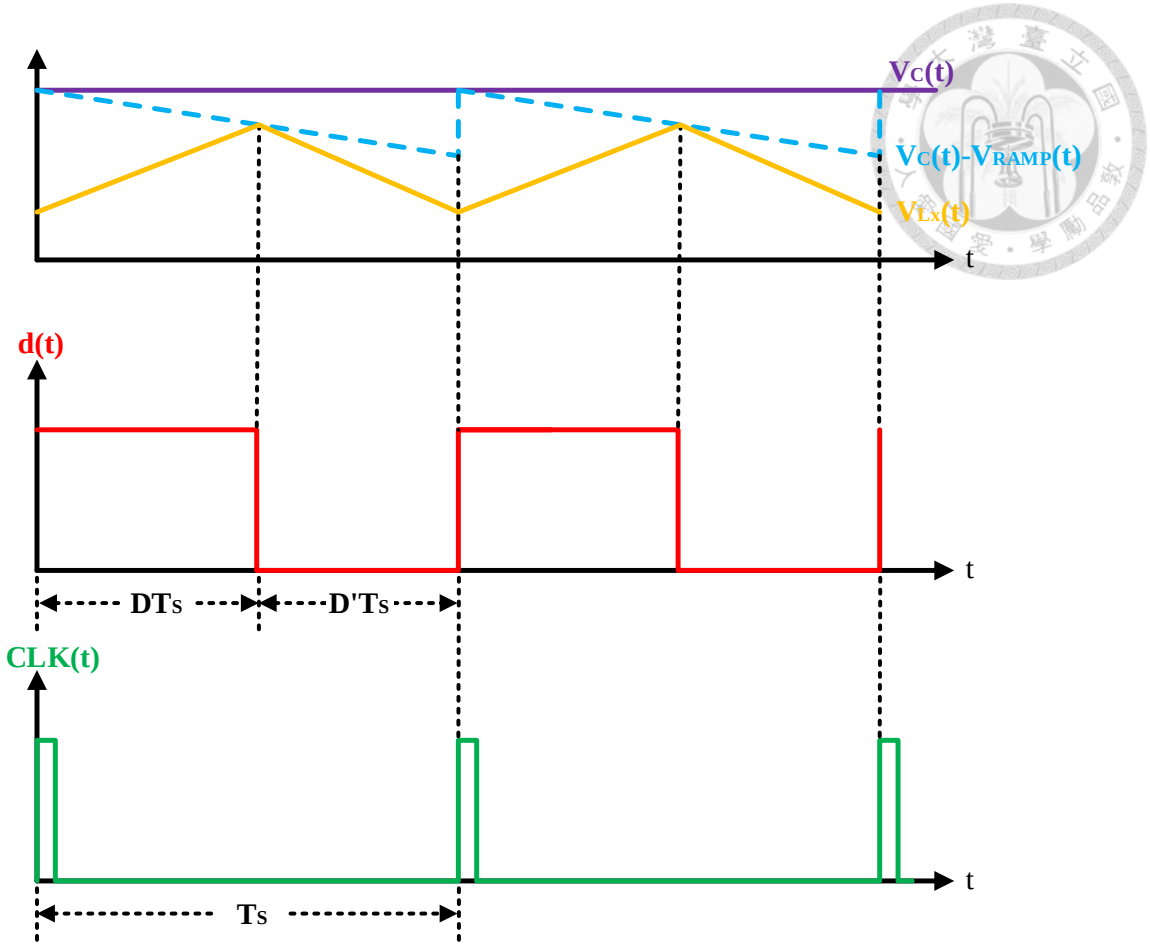

Fig. 2.8 The operation of the current-mode controlled buck converter.

While d(t) is high, M_P turns on so that the inductor current and $V_{Lx}(t)$ gradually increase. When $V_{Lx}(t)$ reaches $V_C(t)$ - $V_{RAMP}(t)$, the duty cycle d(t) becomes low, and at this moment, M_P turns off making the inductor current and $V_{Lx}(t)$ begin to diminish. As the duty cycle is determined by the peak value of $V_{Lx}(t)$, we also refer to this approach as peak-current-mode control in traditional power electronics.

Note that in voltage-mode control, any variation in the input voltage $V_{IN}(t)$ or in the load current $I_{LOAD}(t)$ must be originally detected as an output change before calibrating by the feedback loop. This connotes a disadvantage of slow response. Differently, the current-mode control senses the inductor current which rises with a

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proportion depending on $V_{IN}(t)$ - $V_{OUT}(t)$. This implies that the system will respond immediately according to the alteration of $V_{OUT}(t)$, which stands for faster response in the current-mode control. However, requiring a high-speed and accurate current sensor and having two feedback loops making circuit analysis more complicated are disinclined trade-offs for the current-mode control.

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2-3 Ripple-based Control

The ripple-based control or the output-ripple-based control signifies that the dc-dc converter takes the output voltage ripple as pulse-width modulation (PWM) information. Fig. 2.9 provides a block diagram of a typical ripple-based controlled buck converter.

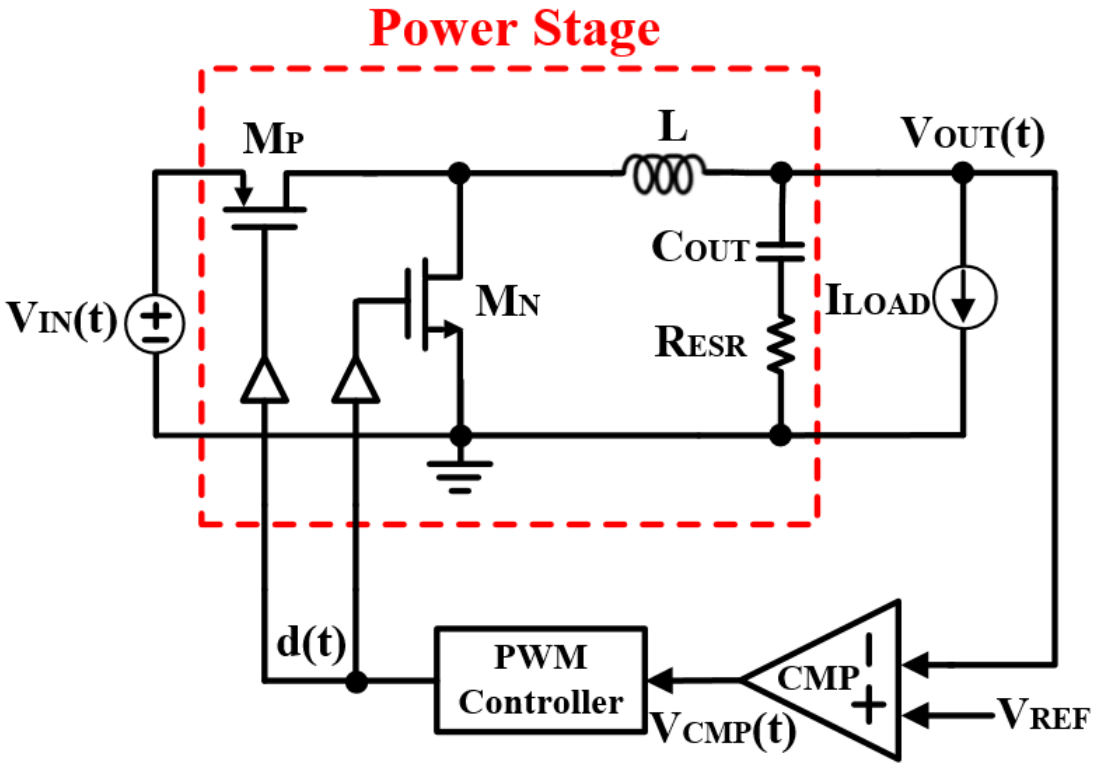

Fig. 2.9 Block diagram of a typical ripple-based controlled buck converter.

The output voltage $V_{OUT}(t)$ is sent to the inverting input of a comparator either directly or via a feedback filter. By comparing the output voltage $V_{OUT}(t)$ as feedback, which involves the information of the output ripple, with a reference voltage V_{REF}, the comparator output $V_{CMP}(t)$ through a PWM controller can determine the parameters about the operation of charging or discharging state, e.g., on-time, off-time, switching frequency and duty cycle.

Without an error amplifier, a clock signal and complex compensation, the ripple-based controlled buck converter has advantages of low cost and low quiescent

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current that resulting in excellent conversion efficiency. Furthermore, directly monitoring output voltage by the comparator with large bandwidth also guarantees quick transient response. Most importantly, the variable switching frequency varies proportionally depending on the output load, which enables the buck converter to extremely save the switching loss under the light load, and thus maintain high efficiency. This outstanding feature lets the ripple-based controlled converter be extensively employed in most power management designs.

The following will briefly introduce two common examples of ripple-based control, including hysteretic control and constant on-time control.

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2-3-1 Hysteretic Control

Fig. 2.10 displays the structure of a buck converter with hysteretic control. The main characteristic of the hysteretic control is that the output oscillates within a predefined error band, referred to as hysteretic band or hysteretic window (V_H).

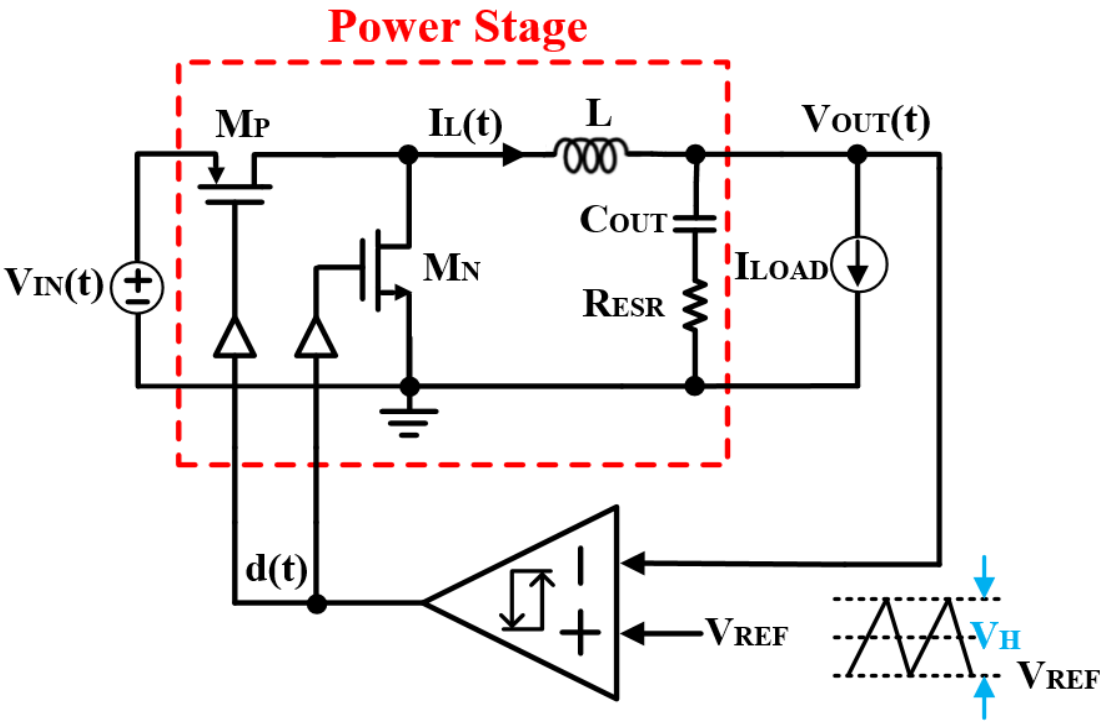

Fig. 2.10 A hysteretic controlled buck converter.

While the power MOS M_P turns on, the inductor current $I_L(t)$ rises. Then, the ac component of the inductor current flows into the output capacitor C_{OUT} and equivalent series resistance (ESR, or R_{ESR}), which brings about voltage raise in the output voltage $V_{OUT}(t)$. When $V_{OUT}(t)$ increases up to the upper bound of the comparator, namely $V_{REF} + V_H$, M_P turns off, and $I_L(t)$ starts to fall causing discharge of $V_{OUT}(t)$. When M_P drops below the lower bound of the comparator, V_{REF}, M_P turns on again, and $I_L(t)$ and $V_{OUT}(t)$ charge once more in the next switching cycle. The operation process is portrayed in Fig. 2.11.

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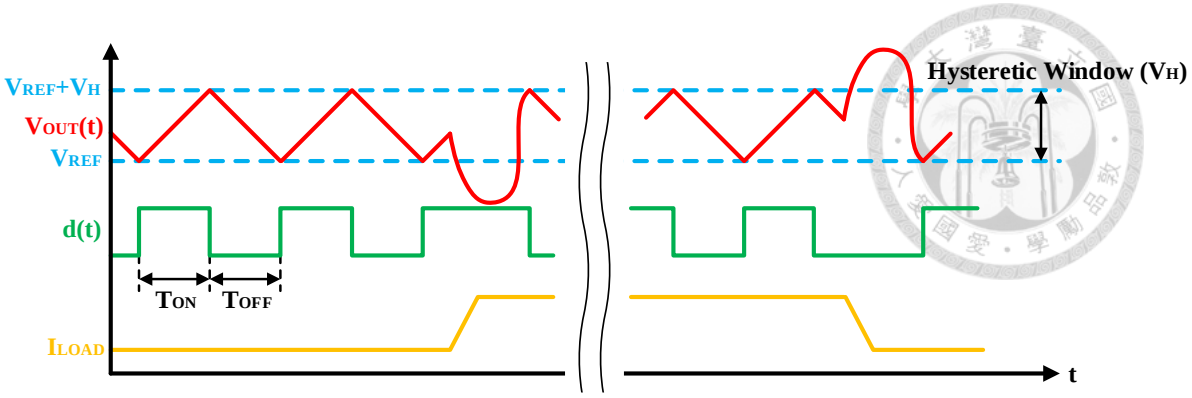

Fig. 2.11 The operation of the hysteretic controlled buck converter.

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2-3-2 Constant On-time Control

Fig. 2.12 presents a basic constant on-time controlled buck converter, which comprehends not only a comparator, but a mono-stable multi-vibrator (MMV). Unlike the hysteretic control in which the adjustments of turn-on and turn-off time are decided by the upper bound and the lower bound, the constant on-time control only has a lower threshold V_{REF}.

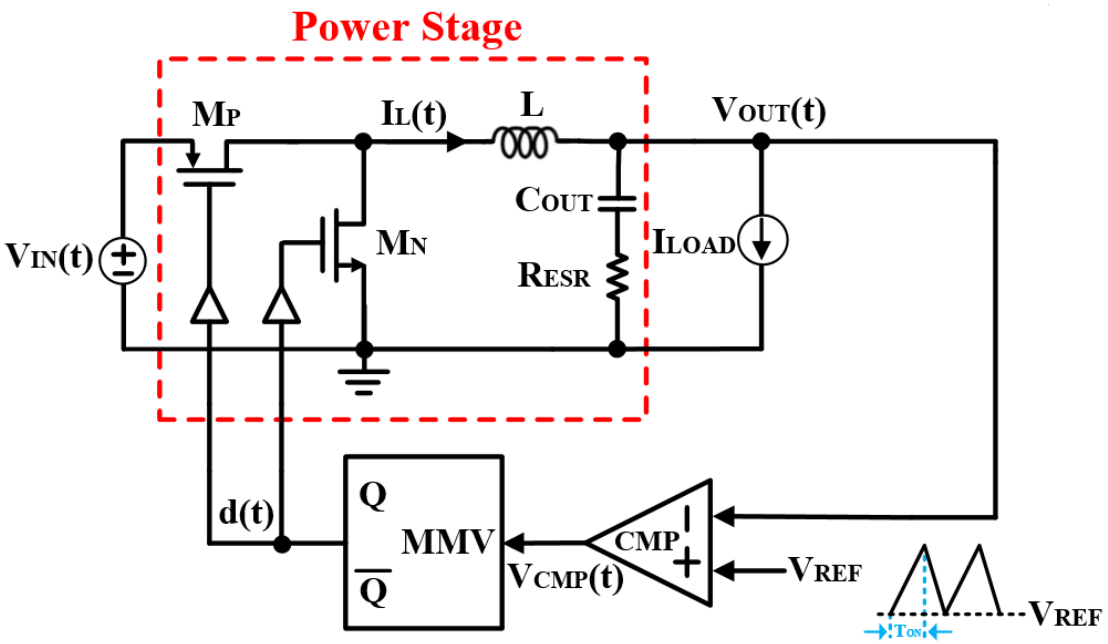

Fig. 2.12 A constant on-time controlled buck converter.

In the discharge period, the output voltage $V_{OUT}(t)$ gradually falls until it is below V_{REF}. Next, $V_{OUT}(t)$ initiates the charge period within a predefined on-time interval T_{ON}, which is determined by the MMV. After the on-time period runs out, the MMV triggers M_P to turn off again, $V_{OUT}(t)$ begins to step down and repeats the next switching cycle. The operation process is depicted in Fig. 2.13.

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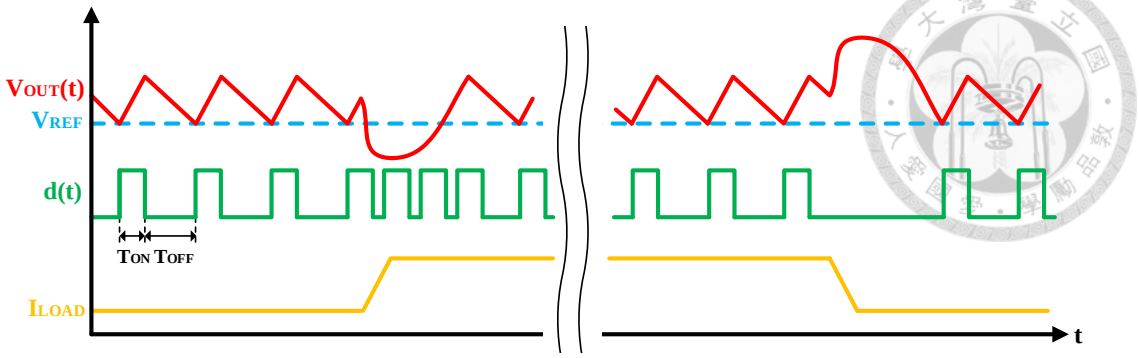

Fig. 2.13 The operation of the constant on-time controlled buck converter.

In virtue of the lower bound managing the duty cycle, the constant on-time control is also called valley control, and it implements at a relatively constant frequency in contrast with the hysteretic control. Eq. (2.6) reports the switching frequency in the constant on-time control [11], which, apparently, relates to the input voltage, the output voltage and T_{ON} merely.

$$f_S = \frac{V_{OUT}}{V_{IN} T_{ON}} \tag{2.6}$$

Note that as one of the ripple-based controlled converters, whose output ripple is dominated by the ESR, the constant on-time control necessitates an output capacitor with a large enough ESR so as to ensure the system ability. That is to say, the output capacitor and the ESR require satisfying the following equation [11].

$$R_{ESR} \cdot C_{OUT} \geq \frac{T_{ON}}{2} \tag{2.7}$$

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Chapter3 Transient-modulated Constant On-time Controlled Single-phase Buck Converter

3-1 Architecture of Proposed Single-phase Buck Converter

Before introducing the overall four-phase buck converter, we focus on the implementation of a single-phase buck converter for a start. Fig. 3.1 is the proposed single-phase buck converter. It consists of a pair of power MOSFETs and gate drivers, an operational transconductance amplifier (OTA), a comparator, a pulse-width modulator, and a dead-time control circuit. Owing to the feedback path of the output voltage, the OTA, taken to detect the variation of the output load, receives V_{OUT} and a reference voltage (V_{REF}) to generate a V_{OTA} first. Then, the V_{OTA} is compared with a V_{SUM}, which contains the peak and valley information of the inductor current, and the comparator produces a V_{CMP} to regulate the pulse-width modulator. Fig. 3.2 shows the circuit of the OTA. The design of the cascode OTA circuit forms a single-stage amplifier that provides high gain and only one dominant pole [12].

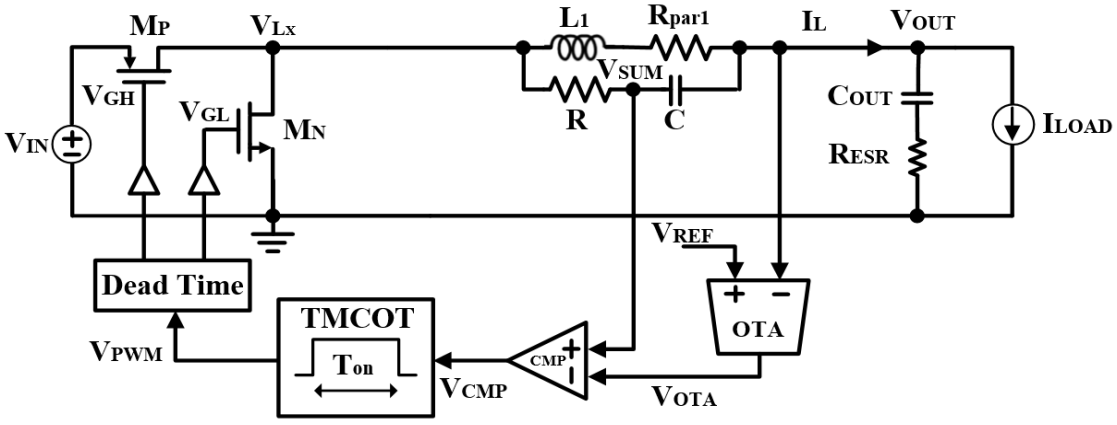

Fig. 3.1 The architecture of the proposed single-phase buck converter.

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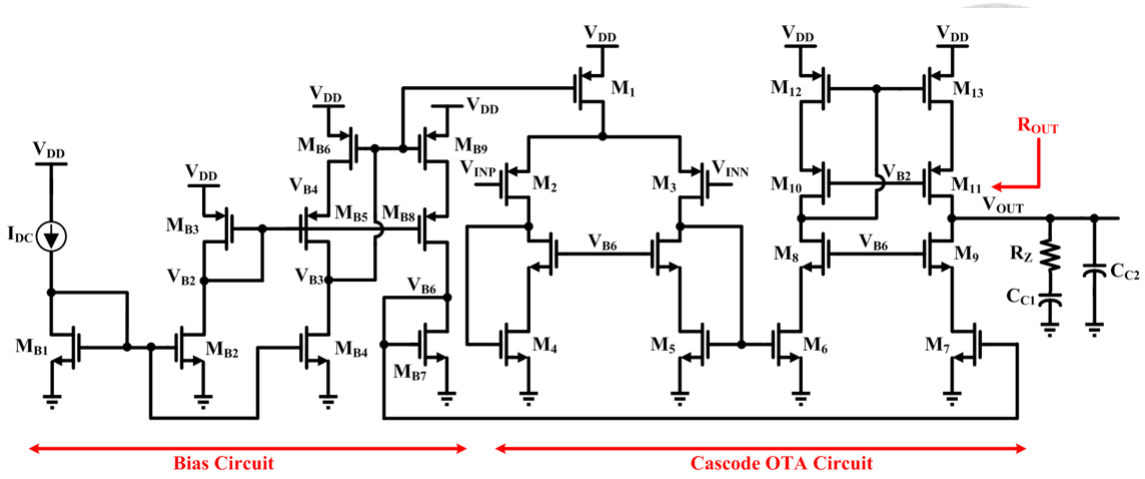

Fig. 3.2 The OTA circuit.

Through the pulse-width modulator of constant on-time control, the V_{OTA} can further decide the duty cycle of V_{PWM}. In fact, for accelerating load transient response, we have improved the traditional constant on-time control to a transient-modulated constant on-time control, and we will expound it in the next chapter 3-2. The gate driver with dead-time control circuit is depicted in Fig. 3.3, and Fig. 3.4 illustrates its timing diagram. M_P and M_N are both power transistors. As shown in Fig. 3.4, when the PWM signal changes from low to high, V_{MN} becomes low with little delay, and M_N turns off. Next, V_{MN_D} and V_{MP} vary, and then M_P turns on. Contrarily, when the PWM signal alters from high to low, V_{MP} becomes high with some delay, and M_P turns off. Later, V_{MP_D} and V_{MN} shift, and then M_N turns on. This protective mechanism can prevent M_P and M_N from conducting simultaneously, and hence there is no current flowing from the power supply to the ground.

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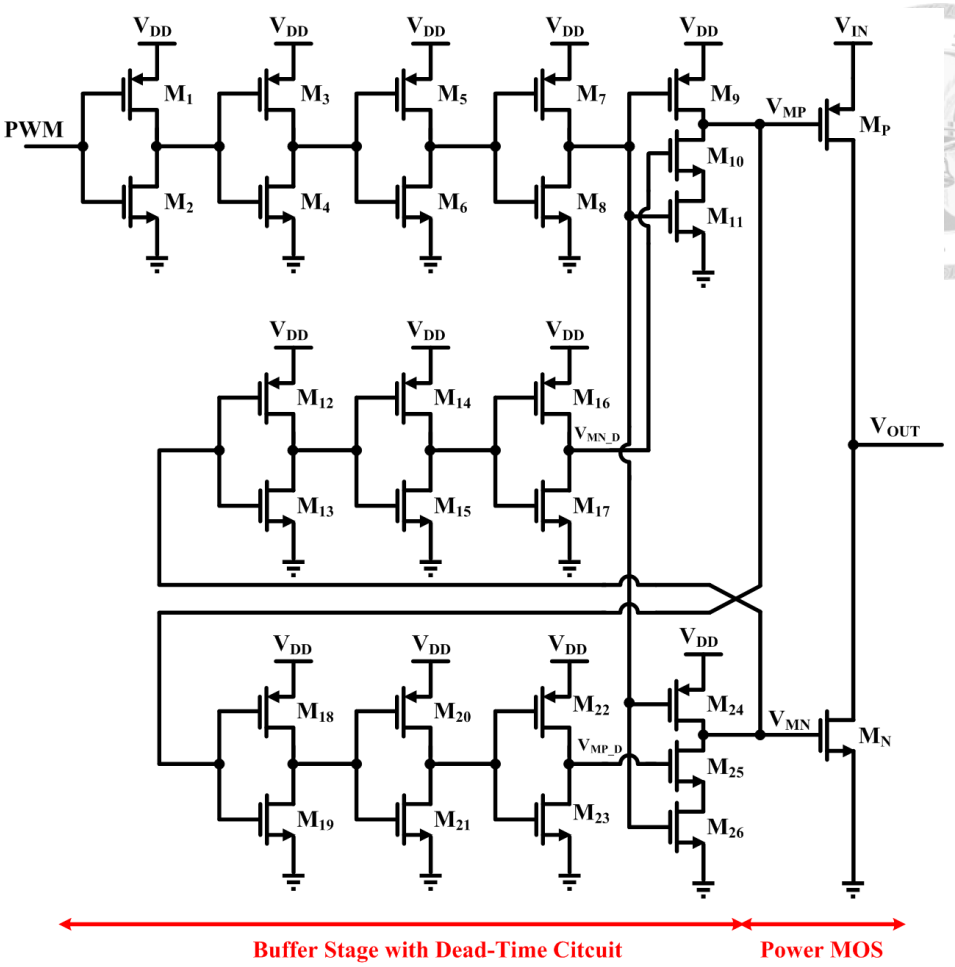

Fig. 3.3 The circuit of the gate driver with dead-time control.

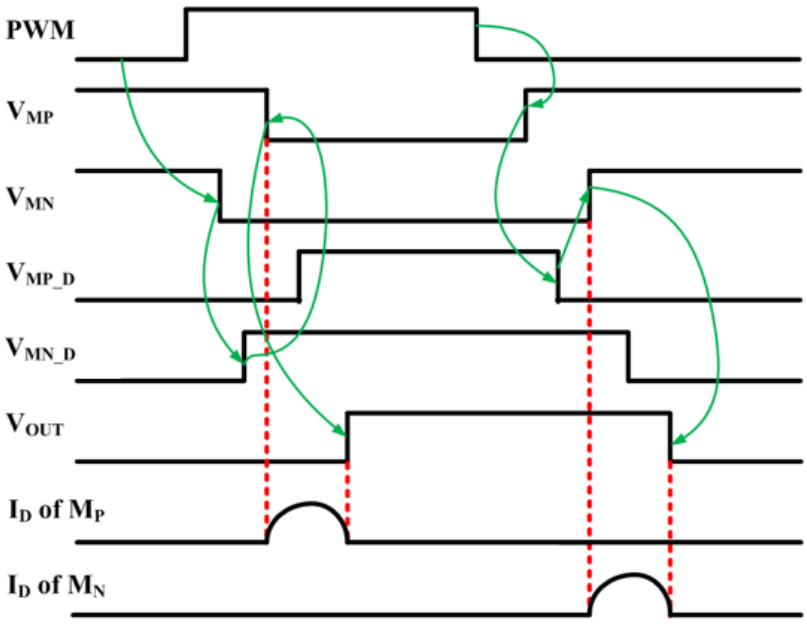

Fig. 3.4 The timing diagram of the gate driver with dead-time control.

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Lastly, to avoid inrush current at the moment when the buck converter starts, we even build a soft start circuit drawn in Fig. 3.5. M_1-M_5 are current mirror structures. In order to get small current I_{CP} and thus postpone the rising time of V_{SLOPE}, the gate lengths of M_1-M_5 are designed to be larger. Then, by comparing sawtooth wave V_{RAMP} and V_{SLOPE}, we can acquire a PWM signal of V_{SOFT_OUT} that expands from narrow breadth to broad width. Fig. 3.6 illustrates the simulation result of the soft start circuit. The soft start time is about 110 μs, and the peak inductor current is around 1.1 A, so it will not damage the transistors.

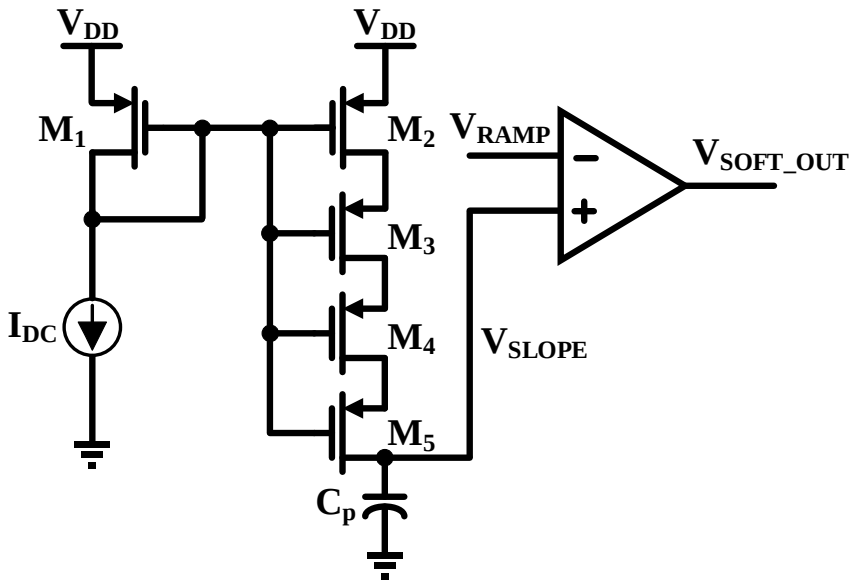

Fig. 3.5 The soft start circuit.

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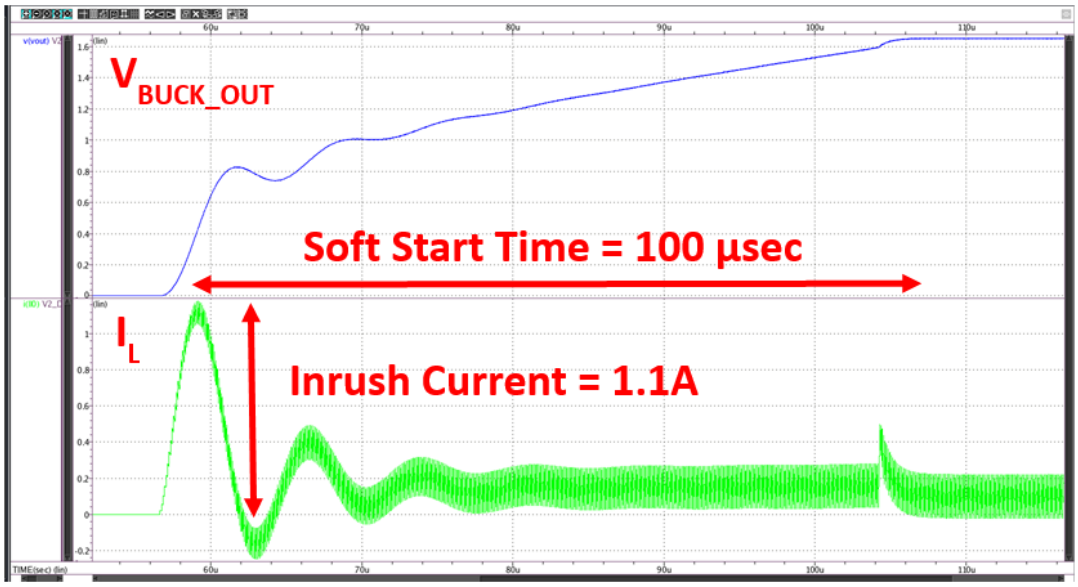

Fig. 3.6 The simulation result of the soft start circuit.

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3-2 Transient-modulated Constant On-time Control (TMCOT)

This part will chiefly emphasize how we ameliorate the conventional constant on-time (COT) control. There is a critical limitation in the traditional COT control. As depicted in Fig. 3.7. While the load current rises, the inductor current continually charge and discharge since the on-time duty cycle of V_{PWM} is constant. This disadvantage substantially decreases the load transient response speed. For this reason, we propose a modified transient-modulated constant on-time (TMCOT) mechanism to improve this slow load transient problem.

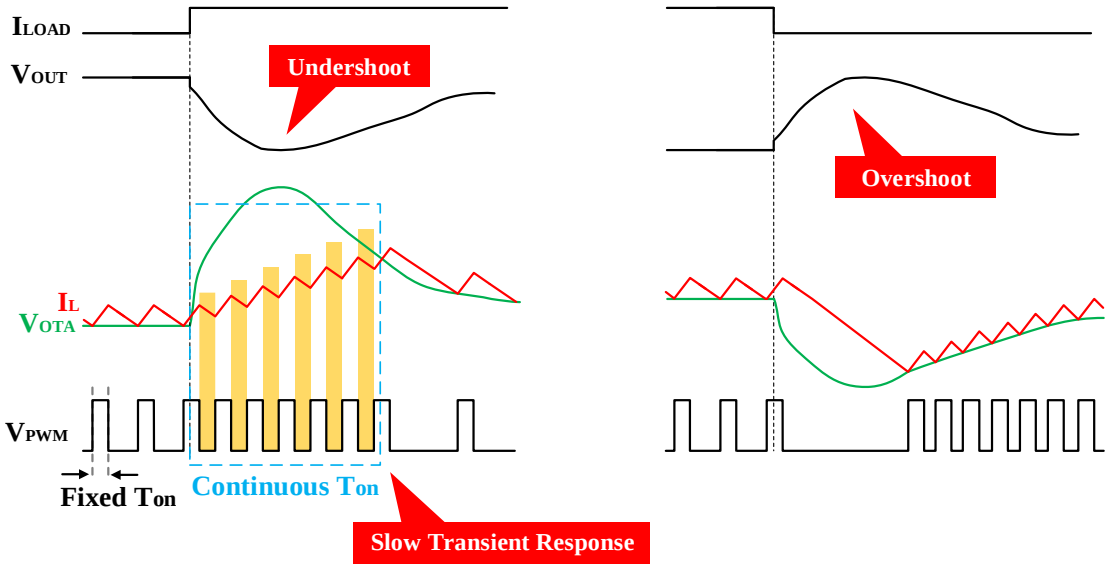

Fig. 3.7 COT limitation: slow load transient response time.

Fig. 3.8 manifests TMCOT control circuit, and Fig. 3.9 clarifies the concept of transient enhancement. First, M_1 and M_2 organize a current mirror, and charge the C_{PW} to generate a sawtooth voltage V_{SAW}. V_{SAW} and reference voltage $V_{REF\_TO\_CLK}$ are sent to comparator, and then produce a PWM signal of V_{RST}. Under usual circumstance, the TMCOT control is like an ordinary COT control. V_Q, or V_{PWM} in the whole buck converter displayed in Fig. 3.1, is determined by the comparison result

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of V_{SAW} and $V_{REF\_TO\_CLK}$, so the on-time of V_{PWM} is fixed generally. Nevertheless, if the variation of the load current happens, i.e., the output voltage V_{OUT} changes, the OTA in Fig. 3.1 will detect the output deviation and accordingly alter V_{OTA}. Subsequently, the output of the comparator, V_S (or V_{CMP} in Fig. 3.1), will widen the duty cycle so that V_Q can increase its on-time. Consequently, the inductor current will maintain charge during the load transient, and the transient response time will also considerably diminish.

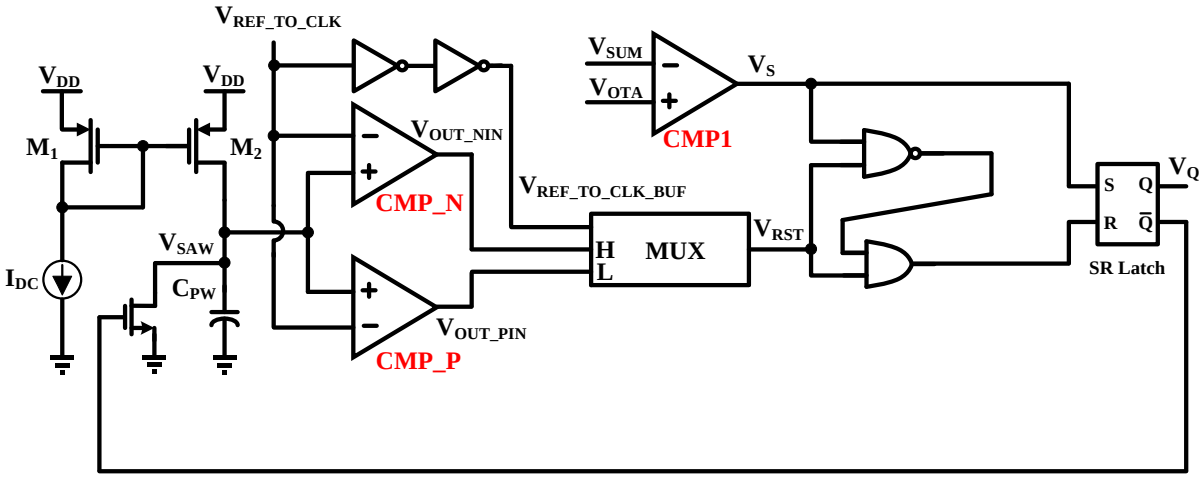

Fig. 3.8 The TMCOT control circuit.

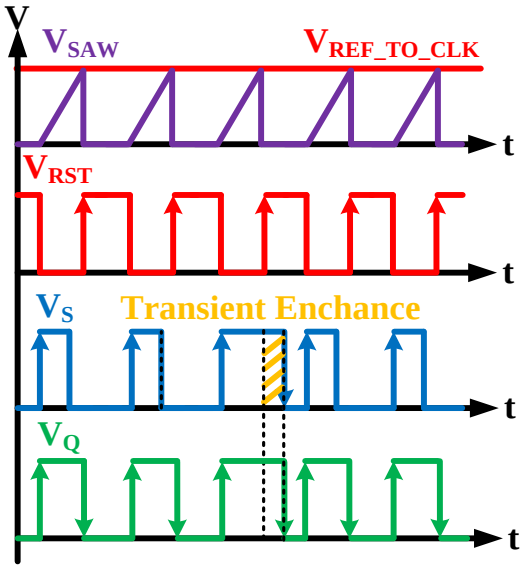

Fig. 3.9 The concept of transient enhancement.

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Note that here we pick high speed comparators to satisfy the demand of 10 MHz switching frequency. Fig. 3.10 expresses the high speed comparator circuit, which includes a pre-amplifier, a latch, and an output buffer.

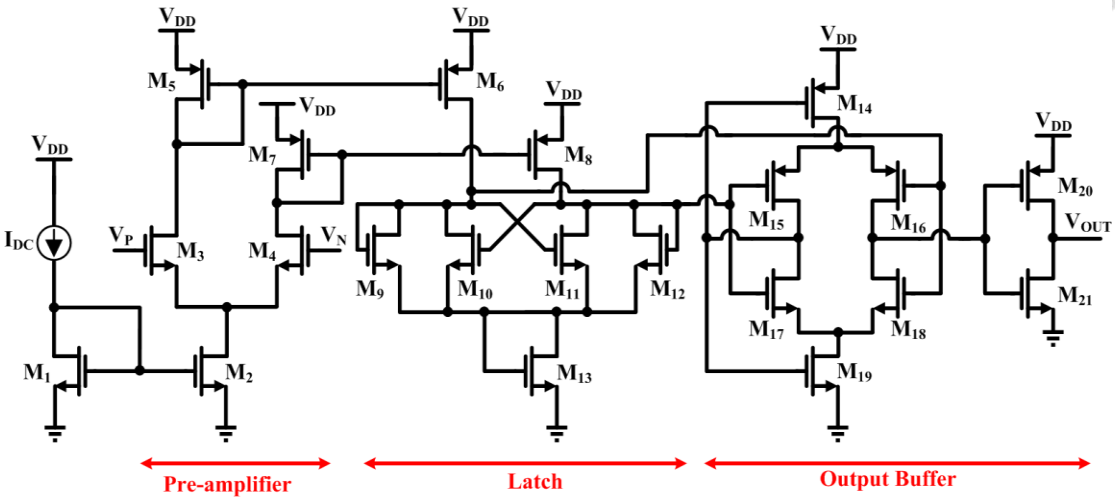

Fig. 3.10 The high speed comparator circuit.

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Chapter4 System Architecture and Proposed Techniques

4-1 Overall System Architecture

The block diagram of the proposed four-phase converter is illustrated in Fig. 4.1. Besides the components of the main phase loop mentioned in chapter 3, there are some extra circuits in phase 0°, including a DLL, a current balancing circuit, and a current sensor. Additionally, the complete four-phase structure comprises other three phases, that is, phase 90°, phase 180°, and phase 270°. Initially, the DLL in the principal phase has the PWM generated by the TMCOT delayed by 90°, 180°, and 270°. Then, the current balancing circuit will calibrate their duty cycles and phase errors on the basis of the mean inductor current. The current sensors in four-phase loops detect the inductor currents I_{L1}-I_{L4}, and average them to obtain a reference value of the inductor current. By comparing the reference current with I_{L2}, I_{L3}, and I_{L4} respectively, we can correct the duty cycles in three sub-phases until their average inductor currents all become the same.

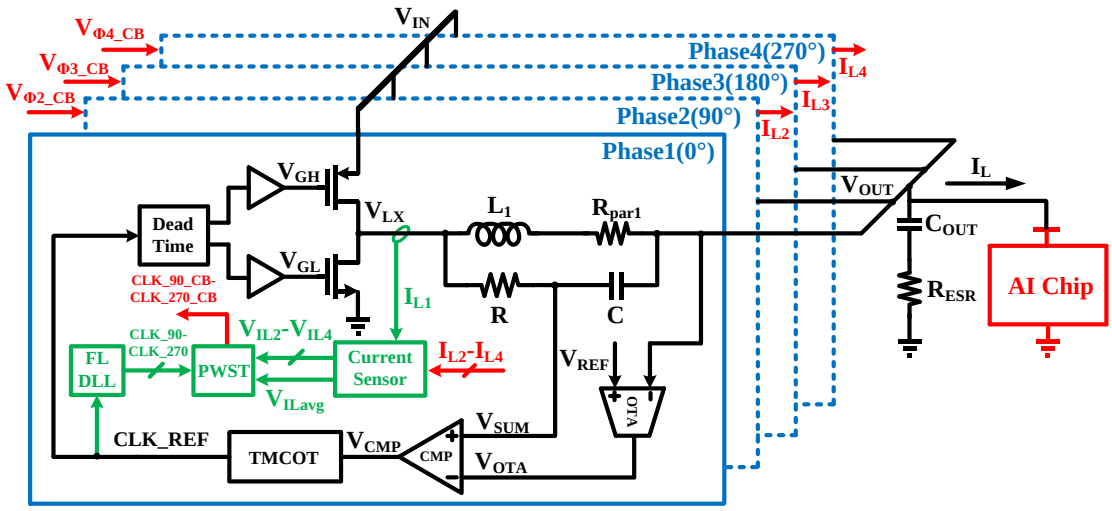

Fig. 4.1 The timing diagram of the gate driver with dead-time control.

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The current sensor circuit is drawn in Fig. 4.2 [12]. Among the current sensor, the OP Amp we adopt is the folded cascode structure, pictured in Fig. 4.3. As for the detailed approach to current sharing, we will explain in chapter 4-5 later.

The proposed four-phase buck converter is operated at 10 MHz switching frequency, and it employs a 330 nH inductor and a 22 μF output capacitor. The input voltage is 3.3V, and the output voltage is 1.8V. The load current can range from 0.4A to 1.4A.

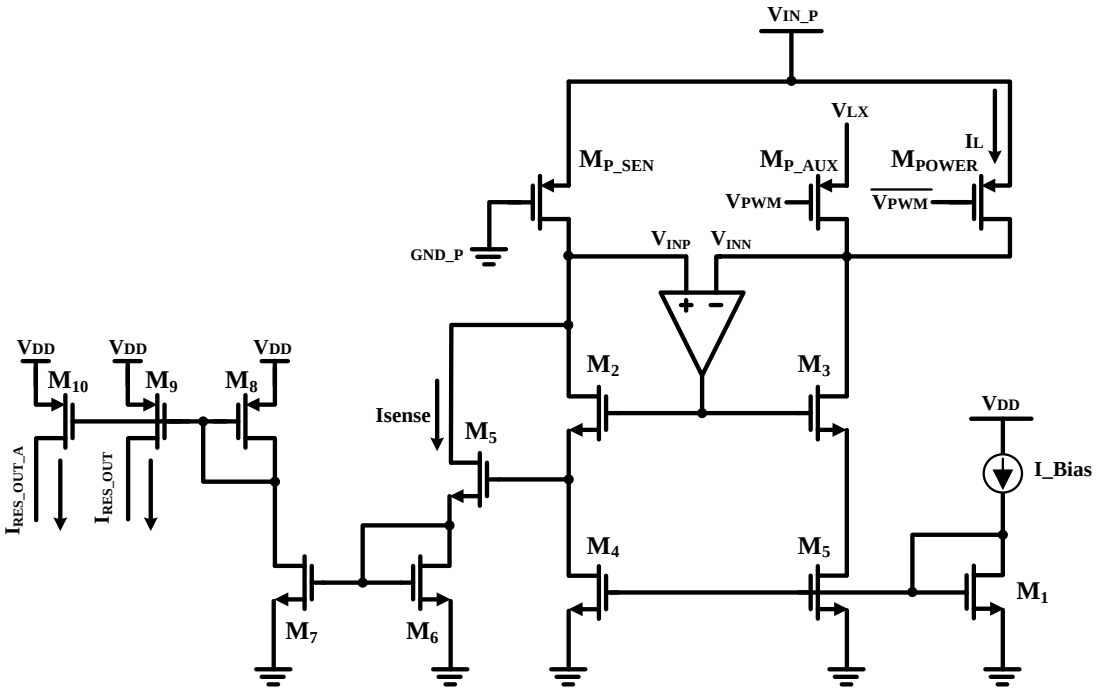

Fig. 4.2 The current sensor circuit.

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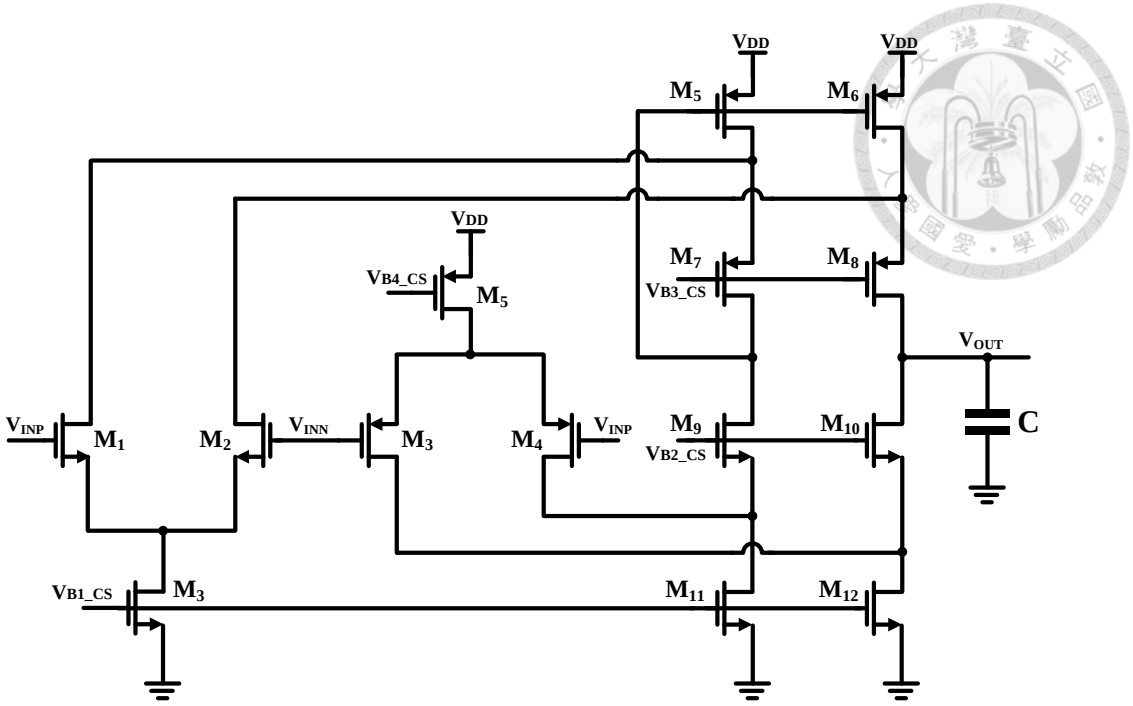

Fig. 4.3 The folded cascade OP AMP circuit.

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4-2 Fast-locking Delay-locked Loop (DLL)

Unlike direct exterior clocks out of the system, using an interior DLL to generate multi-phase PWM signals, such as CLK_90, CLK_180 and CLK_270, is inefficient because it is implied that there is one more loop increasing the transient time of the whole converter. Thus, we purposely choose a fast-locking architecture so as to accelerate load transient response. Its block diagram is shown in Fig. 4.4 .The proposed fast-locking DLL consists of an automatic switching single/dual edge triggered phase detector (ASS/DET-PD), a charge pump (CP), a capacitor as a low pass filter (LPF), and eight delay cells that constitute a voltage-controlled delay line (VCDL).

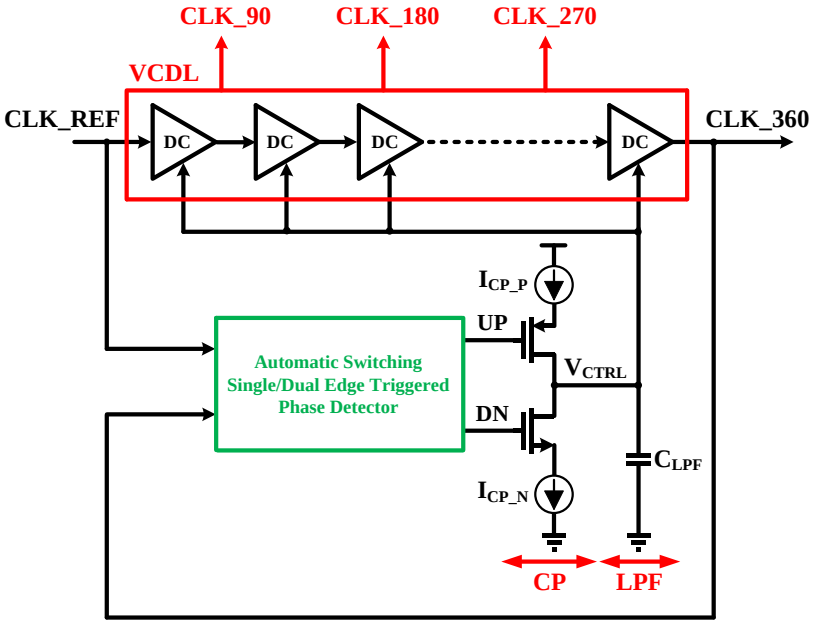

Fig. 4.4 The proposed fast-locking DLL architecture.

Among them, the ASS/DET-PD, which is improved from a conventional dual edge triggered phase detector (DET-PD), is the most significant core circuit since it is responsible for fast-locking implementation. Actually, when CLK_REF and CLK_VCDL are fed into a DET-PD, the DET-PD will detect their phase errors of

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positive and negative edge simultaneously. That is to say, the DET-PD performs detection two times during one reference period. Consequently, in comparison with single edge triggered phase detector (SET-PD), which implements detection only one time in one reference clock, the bandwidth of the DET-PD-based DLL is twice as big as that of the SET-PD-based DLL. The relation between them is expressed as follows:

$$\omega_{n_{DET-PD}} = \frac{I_{CP}K_{VCDL}\cdot(2F_{REF})}{C_{LPF}} = 2 \cdot \omega_{n_{SET-PD}} \tag{4.1}$$

Owing to the double bandwidth, the lock speed of the DET-PD-based DLL is also enhanced up to approximately two times [13], and the theoretically mathematical proof will be demonstrated in the next chapter 4-3. What is more, the formula for the loop stability is the ratio of the bandwidth to the operating frequency:

$$\frac{\omega_{n_{DET-PD}}}{2F_{REF}} = \frac{\omega_{n_{SET-PD}}}{F_{REF}} = \frac{I_{CP}K_{VCDL}}{C_{LPF}} \tag{4.2}$$

Even if the bandwidth rises, the DLL still remains stable because of the parameters (Icp, K_{VCDL}, and C_{LPF}) keeping constant. In other words, DET-PD-based DLL can achieve fast lock without reducing the system stability.

However, there is a fatal drawback in the traditional DET-PD when the duty cycles of its two inputs do not coincide with each other [13]. As shown in Fig. 4.5(a), the positive edges of the reference clock (CLK_REF) and the VCDL output clock (CLK_VCDL) are locked at the *n*th cycle, but their negative edges are still not in locking state. Thus, the phase offset between the two negative edges leads the DET-PD to producing a DN signal to decrease their delay difference. Afterward at the *n*+1th cycle, the delay of CLK_VCDL lags more, which results in the release of the lock at the positive edges of CLK_REF and CLK_VCDL, and correspondingly causes an UP signal generated from the DET-PD. Subsequently, the delay of CLK_VCDL further leads at the *n*+2th cycle on account of the UP signal. Such consecutive operation repeats over and over again so that CLK_VCDL cannot stop tracking

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CLK_REF. This unstable and undesired condition is illustrated in Fig. 4.5(b).

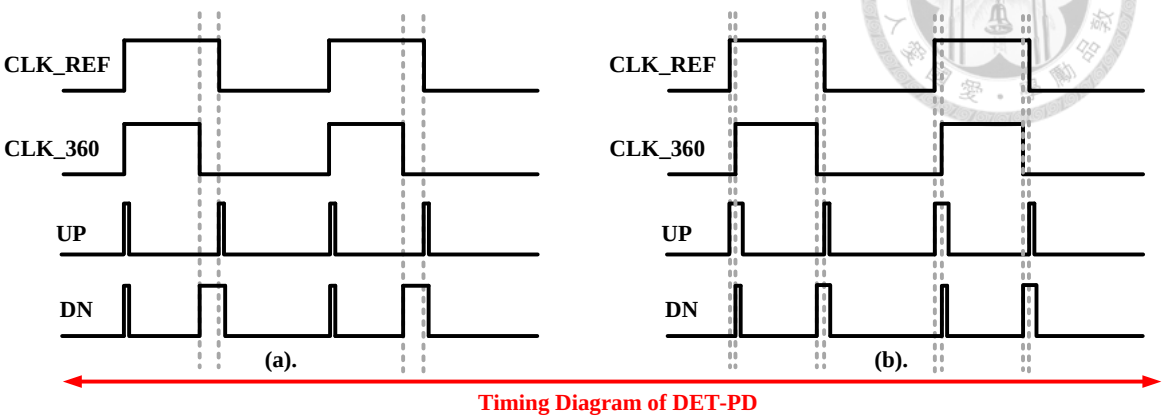

Fig. 4.5 The drawback of DET-PD.

To get over the problem of a conventional DET-PD, this thesis proposes an automatic switching single/dual edge triggered phase detector (ASS/DET-PD). The ASS/DET-PD, combining the advantages of the SET-PD and the DET-PD, can not only accomplish fast lock, but fixedly lock at a single edge. Fig. 4.6 shows the structure of the ASS/DET-PD. The upper part is a DET-PD, which is established with a positive edge triggered phase detector (PET-PD) and a negative edge triggered phase detector (NET-PD) connected parallel to each other. Both of them adopt the framework of the dynamic phase detector, drawn in Fig. 4.7, and the timing diagram of its operation is depicted in Fig. 4.8.

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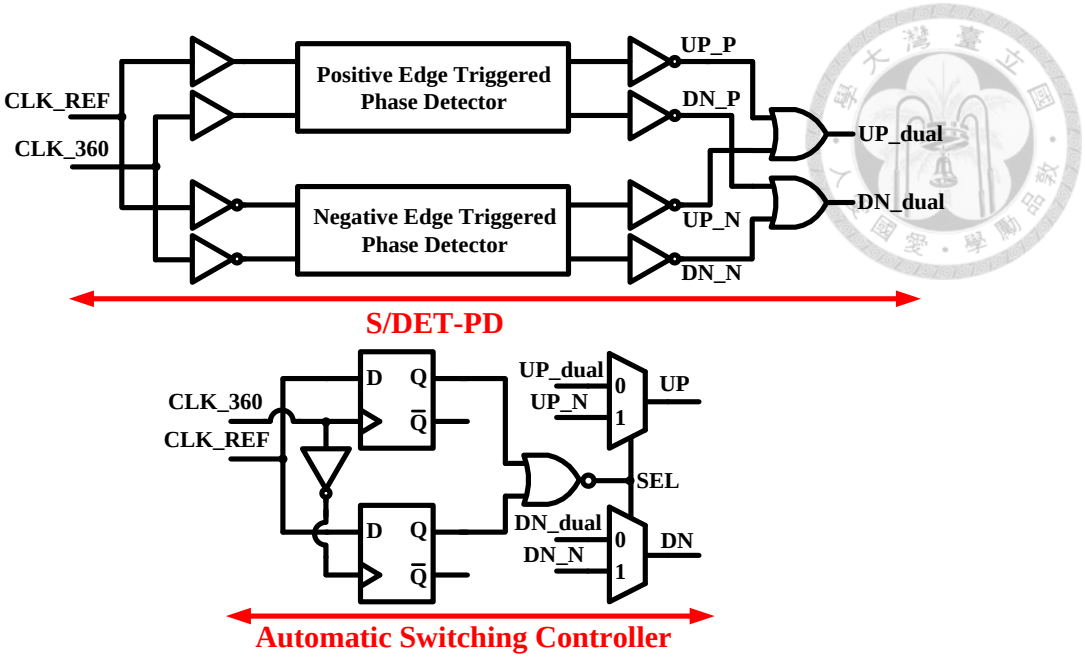

Fig. 4.6 The proposed ASS/DET-PD.

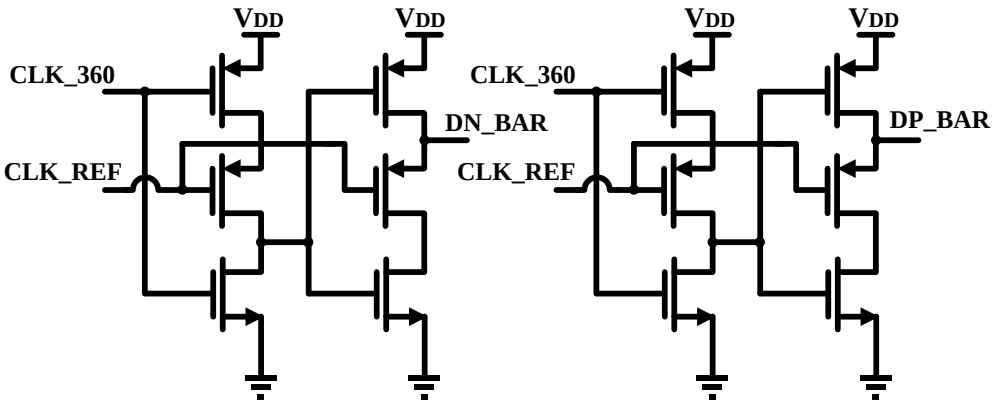

Fig. 4.7 The dynamic phase detector.

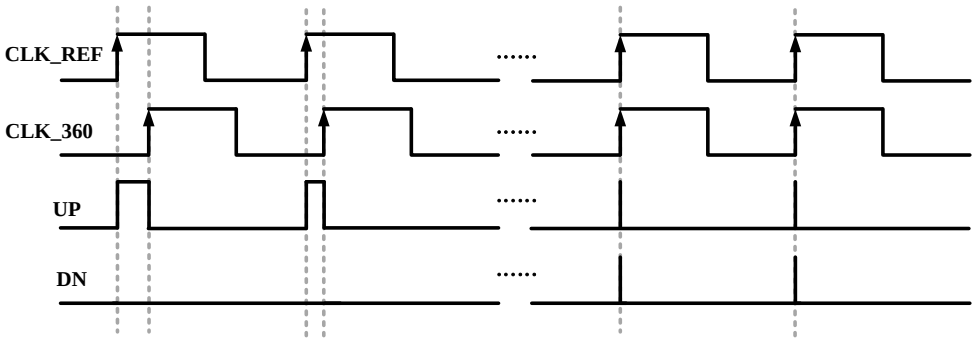

Fig. 4.8 The timing diagram of the dynamic phase detector.

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The PET-PD detects the delay difference between positive edges of CLK_REF and CLK_VCDL, and if CLK_VCDL leads CLK_REF, it will produce a DN_P signal; inversely, if CLK_VCDL lags CLK_REF, an UP_P signal will be transmitted. Relatively, NET-PD accounts for negative edges of CLK_REF and CLK_VCDL, and generates UP_N and DN_N. After emerging the output signals of the PET-PD and the NET-PD, UP_dual and DN_dual are yielded. The lower part of Fig. 4.6, including a NOT gate, two DFFs, a NOR gate, and two 2-to-1 MUXs, is a controller that determines the switch between SET-PD and DET-PD modes. The control rule is illustrated in Fig. 4.9. Here, we assume that the duty cycle of CLK_VCDL is slightly wider than that of CLK_REF. In fact, because of the non-ideal characteristics of a DLL, the duty cycle of CLK_VCDL can hardly match the duty cycle of CLK_REF flawlessly. Therefore, we can make the assumption if we even intentionally design the duty cycle of CLK_VCDL to become larger.

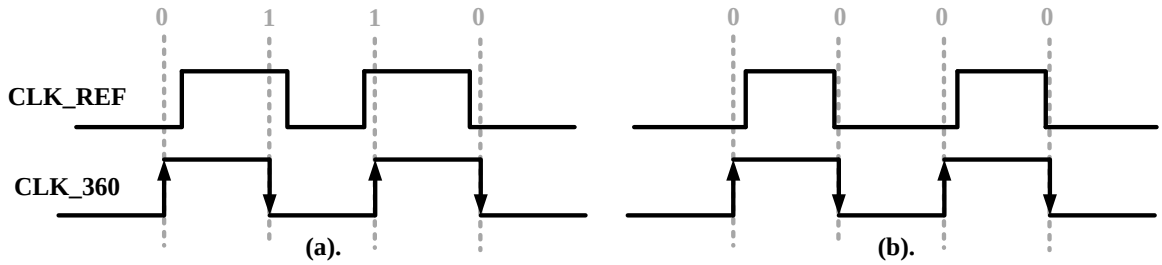

Fig. 4.9 The control rule of the ASS/DET-PD.

Originally, as expressed in Fig. 4.10(a), while the DLL proceeds toward the locked state, CLK_VCDL may lead or lag CLK_REF. At this time, the controller manipulates both the positive and negative edges of CLK_VCDL to sample CLK_REF. If the patterns of “0/1” or “1/0” are sampled, the SEL of the 2-to-1 MUXs will gain a signal of “0”. Then, the ASS/DET-PD will switch to the DET-PD mode, and act as a

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common DET-PD generating the output of UP_dual and DN_dual to execute the fast-locking mechanism. On the other hand, when the DLL extremely approaches the locked state, as pictured in Fig. 4.10(b), the duty cycle of CLK_VCDL will fully cover up the duty cycle of CLK_REF. At this moment, the controller receives the pattern of "0/0", and the SEL becomes "1".

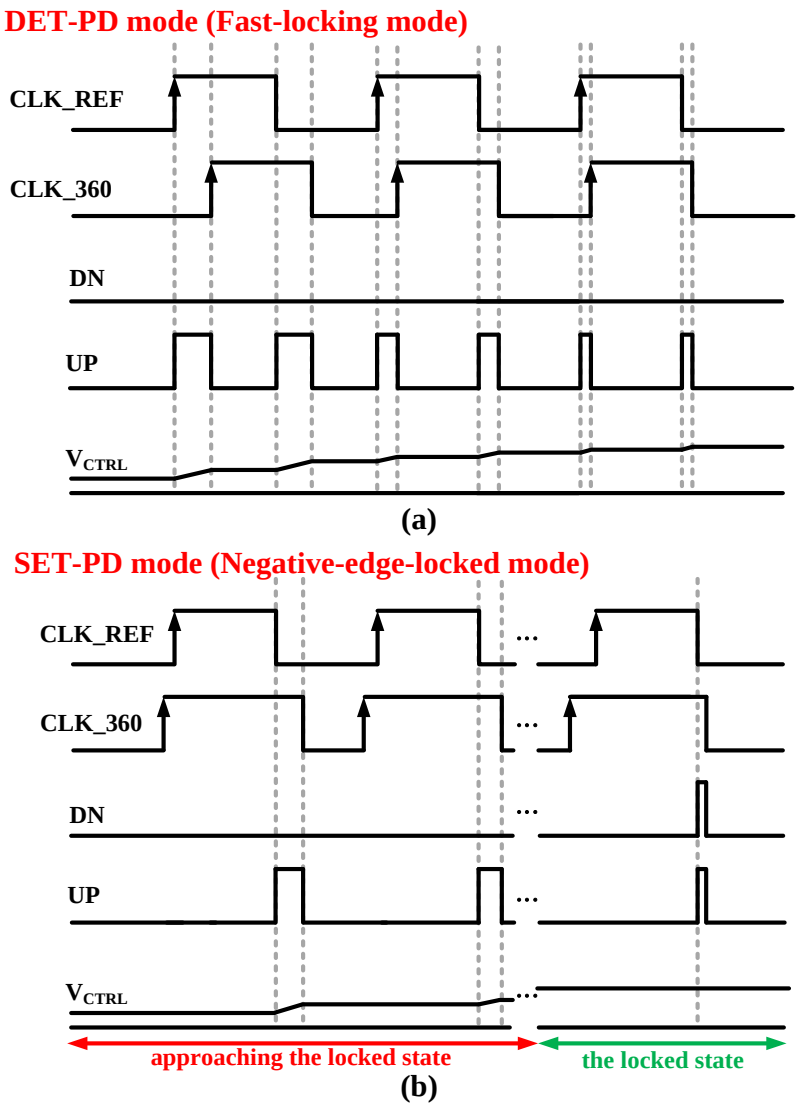

Fig. 4.10 the timing diagram of (a) the DET-PD mode and (b) the SET-PD mode.

As a consequence, the ASS/DET-PD automatically switches to the SET-PD mode, which enables CLK_VCDL to lock at either positive or negative edge of CLK_REF.

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Note that the DLL here is selected to be locked at the negative edge on purpose, so the ASS/DET-PD will produce the output of UP_N and DN_N in the SET-PD mode. The detailed reason will be elaborated in chapter 4-5.

After the ASS/DET-PD generates the UP and DN signals, the CP converts them into current signals. Next, the sole capacitor, which is used as an LPF, will be charged or discharged according to the direction of currents from the CP. The LPF produces a control voltage (V_{CTRL}) to decide the magnitude of the delay applying to delay cells. The eight-stage DCs construct an entire VCDL, and every two DCs eventually delay CLK_VCDL by 90° in the locked state. During the locking process, if CLK_VCDL leads CLK_REF, the ASS/DET-PD will yield a DN signal, which discharges the LPF and reduces the V_{CTRL}. With the lower V_{CTRL}, the magnitude of the delay in the DCs will be raised so that CLK_VCDL lags to track CLK_REF. On the contrary, if CLK_VCDL lags CLK_REF, the ASS/DET-PD will send an UP signal, which charges the LPF and increases the V_{CTRL}. With the higher V_{CTRL}, the value of the delay in the DCs will be lessened so that CLK_VCDL leads to chase CLK_REF. The Fig. 4.11 and the Fig. 4.12 show the circuits of the CP with the LPF and the unitary DC, respectively. The DC is based on the configuration of the current starved delay element. The proposed fast-locking DLL operates at the reference frequency of 5-23 MHz and implements the duty cycle ranging between 15-70%. Both of the properties totally cover the request of the four-phase buck converter we have designed.

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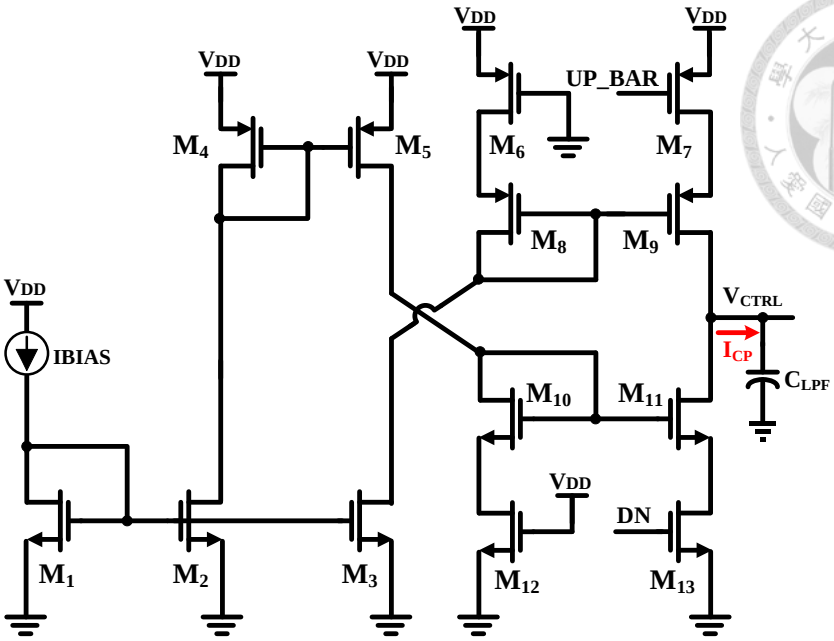

Fig. 4.11 The charge pump with the LPF.

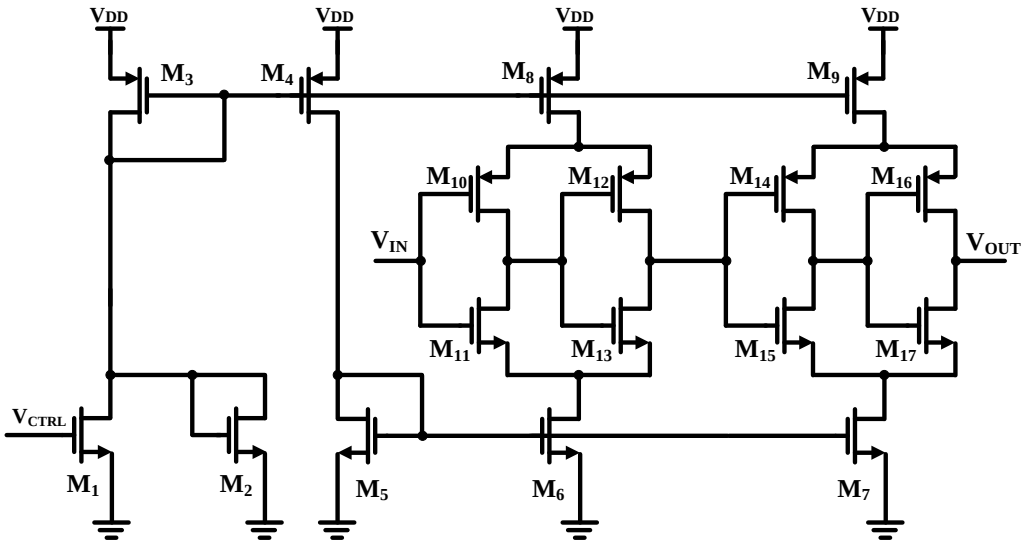

Fig. 4.12 The delay cell.

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4-3 Numerical Analysis of Fast-locking Theme

As mentioned above in chapter 4-2, while the ASS/DET-PD switches to the DET-PD mode, it works as an ordinary DET-PD that produces the output of UP_dual and DN_dual to operate the fast-locking function. Fig. 4.13 illustrates the output characteristic of a conventional DET-PD in terms of delay [14].

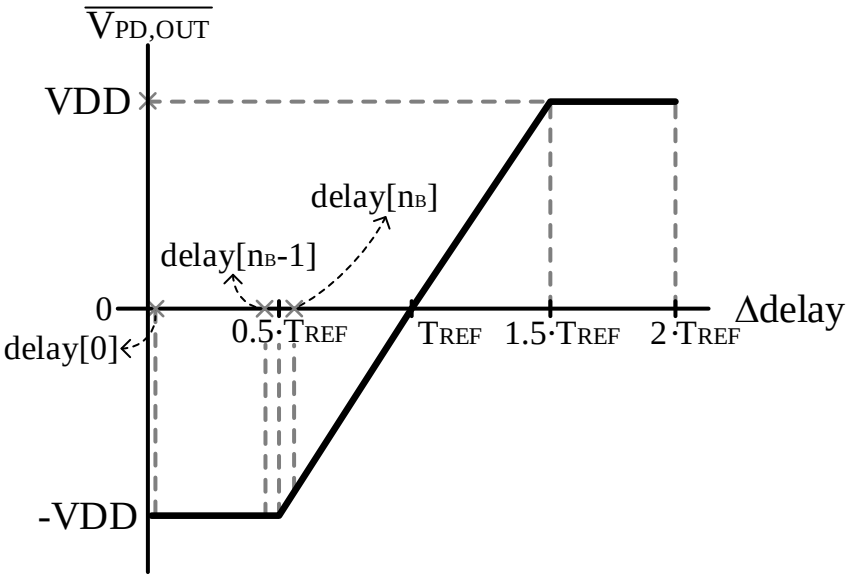

Fig. 4.13 The output characteristic of a conventional DET-PD.

The variation of the VCDL control voltage V_{CTRL}, ΔV_{CTRL}, charged on the loop filter by the CP during one period of the reference clock (T_{REF}) is given by:

$$\Delta V_{CTRL} = \frac{\Delta Q}{C_{LPF}} = \frac{I_{UP}T_{UP} - I_{DN}T_{DN}}{C_{LPF}} \quad (4.3)$$

where C_{LPF} is the capacitance of the low pass filter.

(T_{UP} - T_{DN}) is the time that the net current flows through the loop filter during one reference clock, and thus we can express it by a portion of T_{REF}, i.e., αT_{REF}. The proportional coefficient of α can also be described as the average voltage of UP_dual voltage minus DN_dual voltage with respect to VDD. Moreover, with the assumption that $I_{UP} = I_{DN} = I_{CP}$, we can then rewrite ΔV_{CTRL} as:

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$$\Delta V_{CTRL} = \frac{\Delta Q}{C_{LPF}} = \frac{I_{CP}(T_{UP}-T_{DN})}{C_{LPF}} = \frac{I_{CP}\cdot\alpha T_{REF}}{C_{LPF}} \quad (4.4)$$

$$\text{where } \alpha = \frac{\overline{V_{PD,OUT}}(delay[n])}{V_{DD}} \quad (4.5)$$

The change of the VCDL delay shows negative correlation with the variation of the VCDL control voltage ΔV_{CTRL}:

$$\Delta delay = -K_{VCDL} \cdot \Delta V_{CTRL} \quad (4.6)$$

After that, the delay of the DLL at the *n*+1th iteration can be represented as:

$$delay[n+1] = delay[n] + \Delta delay$$
$$= delay[n] - \frac{I_{CP}\cdot K_{VCDL}}{C_{LPF}} \cdot \alpha T_{REF} \quad (4.7)$$

$I_{CP}\cdot K_{VCDL}/C_{LPF}$ is the same as the DLL bandwidth divided by the reference frequency Eq. (4.2), so we can further simplify Eq. (4.7) as:

$$delay[n+1] = delay[n] - \frac{\omega_n}{F_{REF}} \cdot \alpha T_{REF} \quad (4.8)$$

Obviously, the output characteristic of the DET-PD in Fig. 4.13 is partitioned into two distinct delay zone. One is the linear region between $0.5\cdot T_{REF}$ and $1.5\cdot T_{REF}$, and the other is the constant region between 0 and $0.5\cdot T_{REF}$ as well as $1.5\cdot T_{REF}$ and $2\cdot T_{REF}$. Accordingly, we will analyze the output characteristic into two different sections.

First, when delay[n] is at the left constant region, that is, between 0 and $0.5\cdot T_{REF}$, the output characteristic is a constant of –VDD and hence α is -1 from Eq. (4.5).

$$\alpha = \frac{\overline{V_{PD,OUT}}(delay[n])}{V_{DD}} = \frac{-V_{DD}}{V_{DD}} = -1 \quad (4.9)$$

By combining Eq. (4.8) and Eq. (4.9), when the delay[n] is between 0 and $0.5\cdot T_{REF}$, it can be denoted as:

$$delay[n] = delay[0] + n \cdot (\frac{\omega_n}{F_{REF}} \cdot T_{REF}) \quad (4.10)$$

where delay[0] represents the initial delay of the DLL.

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If we consider the boundary iteration of the left constant region, which means that the constant output characteristic is applied up to the n_Bth iteration, we can gain the following:

$$delay[n_B] = delay[0] + n_B \cdot (\frac{\omega_n}{F_{REF}} \cdot T_{REF}) \quad (4.11)$$

Second, while delay[n] is at the left linear region, namely between $0.5 \cdot T_{REF}$ and T_{REF}, α is then given by:

$$\alpha = \frac{\overline{V_{PD,OUT}}(delay[n])}{V_{DD}} = \frac{\frac{V_{DD}}{0.5 \cdot T_{REF}} \cdot (delay[n] - T_{REF})}{V_{DD}}$$
$$= \frac{2}{T_{REF}}(delay[n] - T_{REF}) \quad (4.12)$$

Alike, if the linear output characteristic is applied to iterations after the n_Bth iteration, the following equation can be derived from Eq. (4.8) and Eq. (4.12).

$$delay[n] - T_{REF} = \left(1 - \frac{2 \cdot \omega_n}{F_{REF}}\right)^{n-n_B} \cdot (delay[n_B] - T_{REF}) \quad (4.13)$$

Then, substitute Eq. (4.11) into the Eq. (4.13).

$$delay[n] - T_{REF}$$
$$= \left(1 - \frac{2 \cdot \omega_n}{F_{REF}}\right)^{n-n_B} \cdot \left(delay[0] + n_B \cdot \left(\frac{\omega_n}{F_{REF}} \cdot T_{REF}\right) - T_{REF}\right) \quad (4.14)$$

If delay[n] becomes T_{REF}, the DLL is called locked. Nevertheless, it necessitates infinite iterations from Eq. (4.14), which connotes meaninglessness. Instead, we assume that if the difference between the delay of the DLL at the n_Tth iteration and one period of the reference clock is no more than ε, which stands for the maximum static phase offset, we consider the DLL locked, i.e.,

$$|delay[n_T] - T_{REF}|$$
$$= \left|\left(1 - \frac{2 \cdot \omega_n}{F_{REF}}\right)^{n_T-n_B} \cdot \left(delay[0] + n_B \cdot \left(\frac{\omega_n}{F_{REF}} \cdot T_{REF}\right) - T_{REF}\right)\right| \leq \varepsilon \quad (4.15)$$

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Besides, we know that $0.5 \cdot T_{REF}$ exists between delay[n_B] and delay [n_B-1] , and n_B is an integer, so, according to Eq. (4.11), n_B can be obtained from the following equations.

$$n_B - 1 < \frac{0.5 \cdot T_{REF} - delay[0]}{\frac{\omega_n}{F_{REF}} \cdot T_{REF}} < n_B \tag{4.16}$$

$$n_B = \left\lceil \frac{0.5 \cdot T_{REF} - delay[0]}{\frac{\omega_n}{F_{REF}} \cdot T_{REF}} \right\rceil \tag{4.17}$$

Note that since n_B exists at the boundary between the constant region and the linear region, n_B is 0 in the case of delay[0] > $0.5 \cdot T_{REF}$.

On the other hand, if a DLL adopting SET-PD that has linear output characteristic from 0 to $2 \cdot T_{REF}$, we can also acquire the following equation by the same derivation as above.

$$|delay[n_T] - T_{REF}| = \left| \left(1 - \frac{\omega_n}{F_{REF}}\right)^{n_T} \cdot (delay[0] - T_{REF}) \right| \leq \varepsilon \tag{4.18}$$

Ultimately, while the DET-PD and the SET-PD are implemented in the DLL respectively, the relative locking speed or the relative number of cycles required for the lock can be given by:

$$n_{T_{DET-PD}} = \frac{n_{T_{SET-PD}} \cdot \ln\left(1 - \frac{\omega_n}{F_{REF}}\right) + \ln\left(\frac{delay[0] - T_{REF}}{delay[0] + n_B \cdot \left(\frac{\omega_n}{F_{REF}} T_{REF}\right) - T_{REF}}\right)}{\ln\left(1 - \frac{2 \cdot \omega_n}{F_{REF}}\right)} + n_B \tag{4.19}$$

Assuming that the DET-PD-based DLL and the SET-PD-based DLL are both operated at the reference frequency of 10MHz with the loop bandwidth of 200kHz. We can draw the locking speed enhancement in relation to the maximum static phase offset ε, as displayed in Fig. 4.14.

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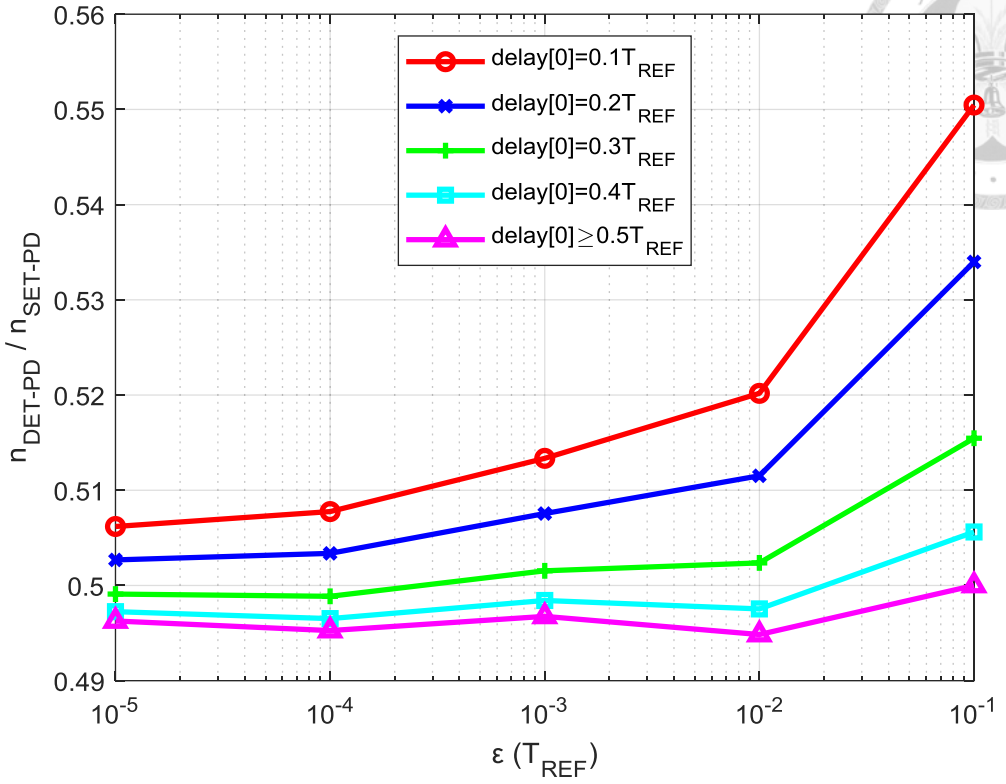

Fig. 4.14 The locking speed enhancement in terms of ε and delay[0].

In the Fig. 4.14, ε represents the locking accuracy, and $10^{-5}\cdot T_{REF}$ implies that it is more accurate than $10^{-1}\cdot T_{REF}$. The initial condition delay[0] determines the locking time, and in the case of delay[0] $\geq 0.5\cdot T_{REF}$, the locking speed of the DET-PD-based DLL is always two times greater than the SET-PD-based DLL. Even in the case of delay[0] $< 0.5\cdot T_{REF}$, the number of the locking cycles are almost close to two times for the SET-PD-based DLL. Consequently, we can confirm that the DET-PD-based DLL has more rapid locking speed than the SET-PD-based DLL, which successfully helps our buck converter achieve shorter load transient response time.

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4-4 Effects of Duty Cycle and Phase Error Mismatch

An advantageous characteristic for multi-phase converters is less conduction loss. If an *n*-phase converter is employed, power dissipation will decrease by a factor of n times theoretically. That is to say, growth of the efficiency has something to do with the multi-phase of the power-trains. Generally speaking, the duty cycle of PWM signals in each phase must maintain the same, and the phase error between each of PWM signals must keep the interval of $(360/n)^{o}$. However, if any deviation unfortunately occurs, uneven inductor current will be distributed among the power-trains, and the efficiency will then sharply degrade [15].

Practically, there are two main sources bringing about the current mismatch. One is duty cycle mismatch, and the other is parasitic series resistance mismatch or equivalent series resistance (ESR) mismatch. In order to separately analyze the contribution of two mismatch causes, we build a model of an *n*-phase converter, pictured in Fig. 4.15, where D_i represents the duty cycle ratio of the *i*th PWM signals.

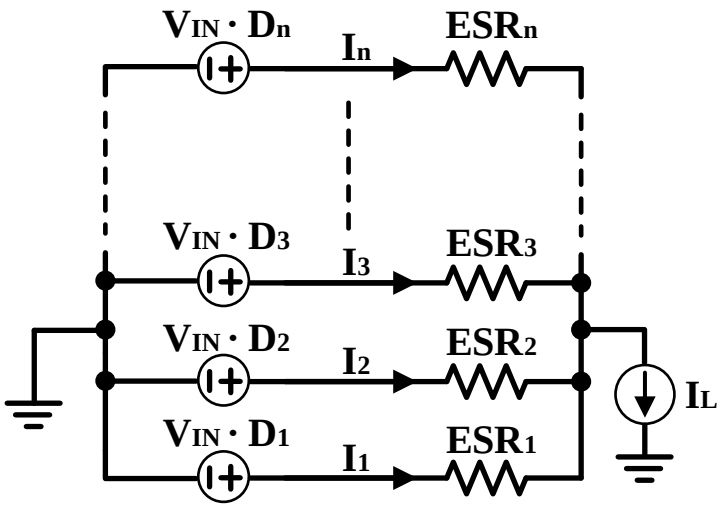

Fig. 4.15 The model of an *n*-phase converter for analysis.

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Initially, we assume that all the duty cycles are matched and only the resistance of the *i*th power-train is distinct by ΔESR from the resistances in the other power-trains, which are all equivalent to ESR. From [4], we can derive that while the duty cycles and the ESRs are both matched, the current variation ΔI_i of the *i*th power-train with regard to the ideal current I_i is:

$$\left(\frac{\Delta I_i}{I_i}\right)_{ESR} = -\frac{n-1}{n} \cdot \frac{\Delta ESR}{ESR} \tag{4.20}$$

where ESR involves all the series resistances in each power-train and is equal to ESR = R_{SW} + R_L + R_{others}. Additionally, R_{SW} = D · R_{PMOS} + (1 – D) · R_{NMOS} is the resistance of switching transistors, R_L represents the ESR of the power inductor, and R_{others} expresses all other series resistances in the power-train. To fairly compare, we assume that the summation of the ESRs of all the power-trains remains unchanged. In consequence, we can acquire the following equation:

$$(ESR' + \Delta ESR) + (n-1) \cdot \left(ESR' - \frac{\Delta ESR}{n-1}\right) = n \cdot ESR' \tag{4.21}$$

where ESR′ is the average resistance of all the power-trains, and ΔESR is the resistance mismatch. In this way, we can also ensure that the output voltage keeps constant regardless of the mismatch. The first term, (ESR′ + ΔESR), indicates the resistance of the *i*th power-train. The second term, (ESR′ - ΔESR / (n - 1)), manifests the resistance of other power-trains. From the model of the converter illustrated in Fig. 4.15, the currents of the power-trains are given by:

$$I_{i,\Delta ESR} = \frac{ESR' - \frac{\Delta ESR}{n-1}}{(n-1)\cdot(ESR'+\Delta ESR)+(ESR'-\frac{\Delta ESR}{n-1})} \cdot I_L \tag{4.22}$$

$$I_{others,\Delta ESR} = \frac{1}{n-1}(I_L - I_i) \tag{4.23}$$

Next, the conduction loss and the efficiency are given by:

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$$P_{loss,\Delta ESR} =$$

$$I_i^2 \cdot (ESR' + \Delta ESR) + (n-1) \cdot I_{others}^2 \cdot (ESR' - \frac{\Delta ESR}{n-1}) \quad (4.24)$$

$$\eta_{\Delta ESR} = \frac{V_O I_O}{V_O I_O + P_{loss,\Delta ESR}} \quad (4.25)$$

Assuming that a four-phase converter (n=4) is provided with average ESR of 150mΩ. Fig. 4.16 represents that with 10% ESR variation, the current in the power-train and the converter efficiency shift by 3.6% and 0.007%, respectively.

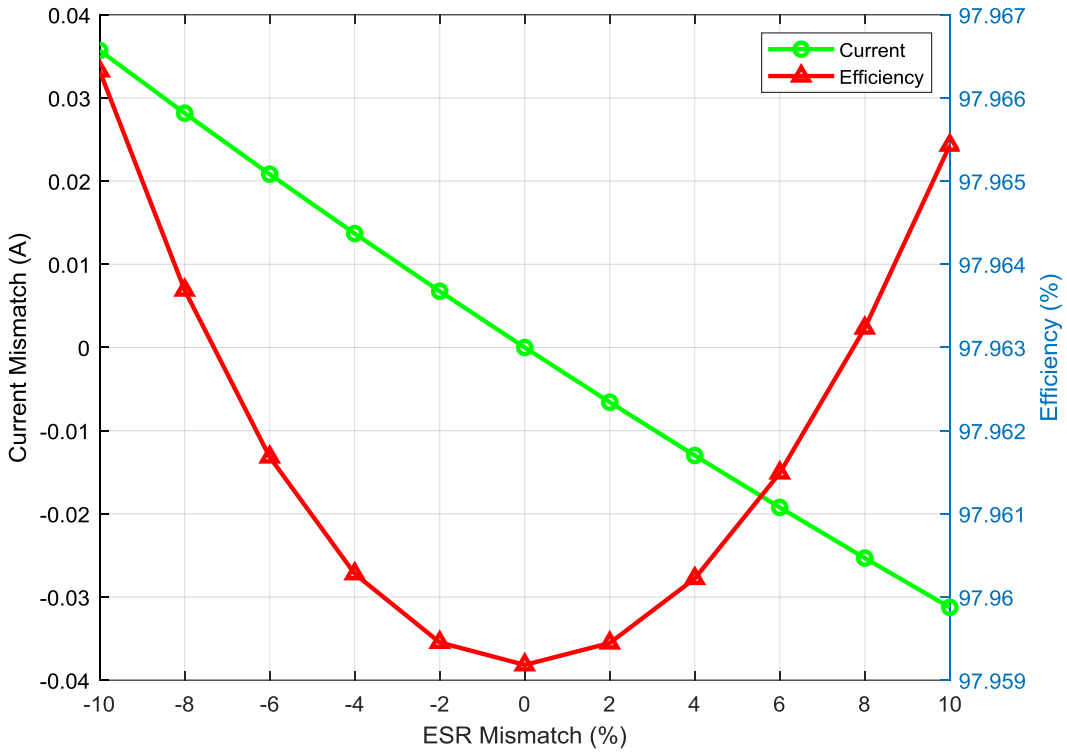

Fig. 4.16 Effect of the ESR mismatch (V_{IN} = 3.3V, V_O = 1.8V and I_L = 1A).

On the other hand, now we assume that all the ESRs are matched and only the duty cycle of the *i*th power-train is different by ΔD from the other duty cycles, which are all equivalent to D. Likewise, when the duty cycles and the ESRs are both matched,

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the current variation ΔI_i of the *i*th power-train with respect to the ideal current I_i can be derived from [4] as well:

$$\left(\frac{\Delta I_i}{I_i}\right)_D = \frac{n-1}{n} \cdot \frac{V_{IN}\Delta D}{ESR} \tag{4.26}$$

Similarly for an impartial comparison, we assume that the duty cycle mismatch ΔD between the *i*th power-train and the other power-trains is equitably distributed to hold the same output voltage. Therefore, we can describe ΔD_i as:

$$\Delta D_i = -(n-1) \cdot \Delta D_{others} \tag{4.27}$$

From the model of the converter depicted in Fig. 4.15, the current in each power-train is given by:

$$I_{i,\Delta D} = \frac{I_L}{n} + \frac{V_{IN}\Delta D_i}{ESR} \tag{4.28}$$

$$I_{others,\Delta D} = \frac{I_L}{n} + \frac{V_{IN}\Delta D_{others}}{ESR} = \frac{1}{n-1}(I_L - I_i) \tag{4.29}$$

Then, the conduction loss and the efficiency are given by:

$$P_{loss,\Delta D} = I_i^2 \cdot ESR + (n-1) \cdot I_{others}^2 \cdot ESR) \tag{4.30}$$

$$\eta_{\Delta D} = \frac{V_O I_O}{V_O I_O + P_{loss,\Delta D}} \tag{4.31}$$

Under the same conditions as Fig. 4.16, the Fig. 4.17 manifests that with 10% duty cycle variation, the current in the power-train and the converter efficiency vary by 160% and 13.3%, respectively.

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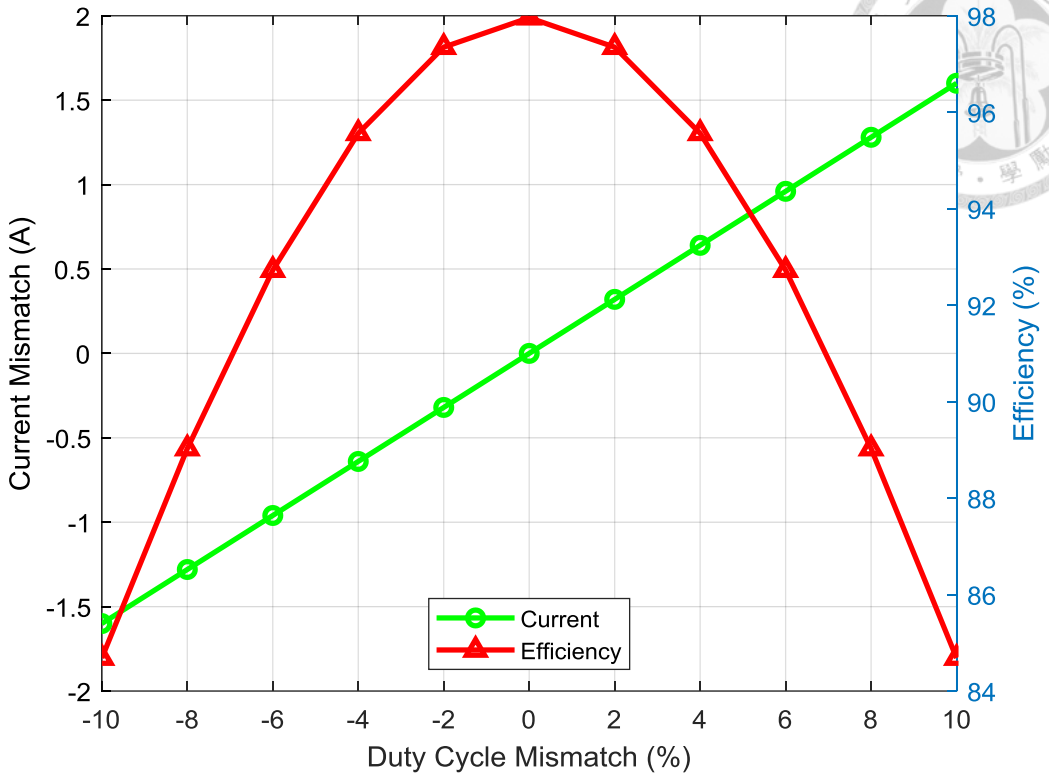

Fig. 4.17 Effect of the duty cycle mismatch (V_{IN} = 3.3V, V_O = 1.8V and I_L = 1A).

The primary reason for this enormous degradation is that the serious duty cycle mismatch leads to the huge unbalanced current distribution. In truth, we can also forecast this condition from the following formula derived from [6]:

$$\left(\frac{\Delta I_i}{I_i}\right)_D = \frac{n-1}{n} \cdot \frac{1}{1-\eta} \cdot \left(\frac{\Delta D}{D}\right) \tag{4.32}$$

For instance, assuming that efficiency is equal to 95% (η = 0.95), Eq. (4.32) indicates that the current mismatch of the power-train ($\Delta I_i/I_i$) is magnified by about 20 times in regard to the duty cycle mismatch ($\Delta D/D$). As a result, we can conclude that rather than the ESR mismatch, the duty cycle mismatch majorly and severely influences the inductor current mismatch, and hence we have to calibrate the duty cycle variation.

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4-5 Pulse-width-shrunk Technique (PWST)

In order to solve the unbalance of the inductor currents in four-phase paths, we demonstrate a pulse-width-shrunk technique (PWST) that not merely calibrates the duty cycles, but maintains all the phases with fixedly and uniformly spaced intervals.

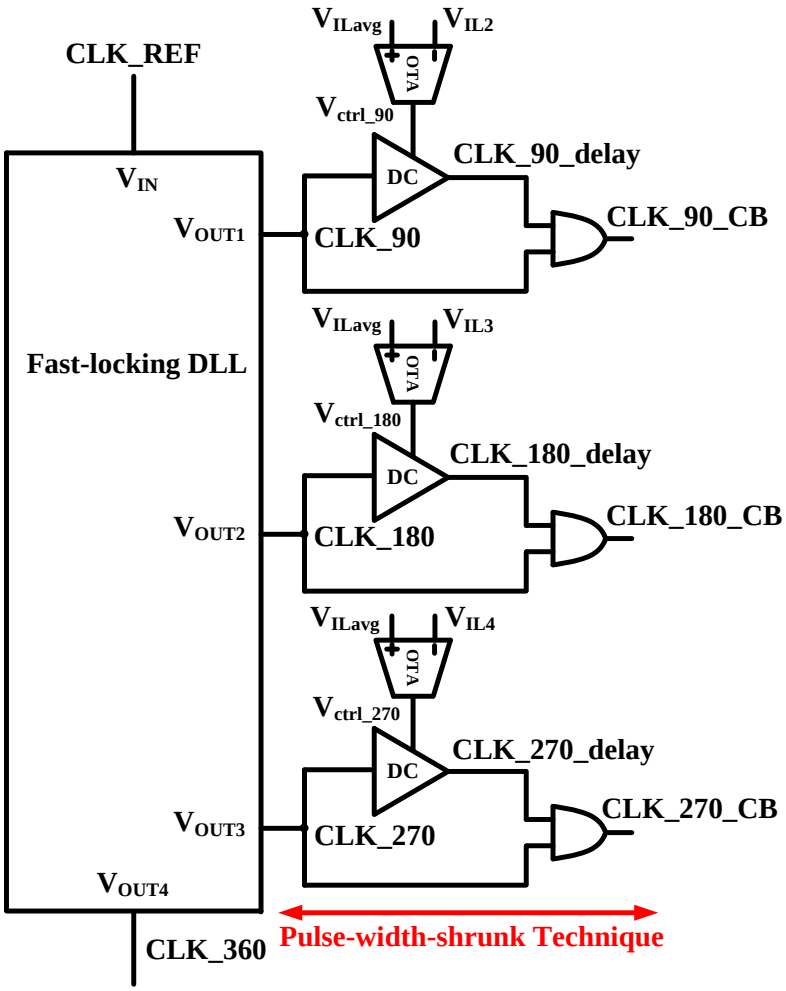

Fig. 4.18 The PWST with the fast-locking DLL.

The PWST with the proposed fast-locking DLL is illustrated in the Fig. 4.18. The PWM signal CLK_REF, which is generated by TMCOT control in the first main phase, is fed into the DLL as a reference frequency for producing other three-phase PWM signals including CLK_90, CLK_180, and CLK_270. Nevertheless,

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considering the non-ideal characteristics of the DLL, these three sub-phase signals will not have equivalent duty cycles in reality. Actually, even though most researches do not employ a DLL to generate the multi-phase clocks [2], [7], [8], [15], [16], there are still duty cycle errors resulting from the inaccuracies in their own duty cycle loops. Accordingly, we combine a delay cell (DC) and an AND logic gate with an OTA to construct a set of the pulse-width-shrunk circuit, and the operation of the PWS circuit is depicted in Fig. 4.19.

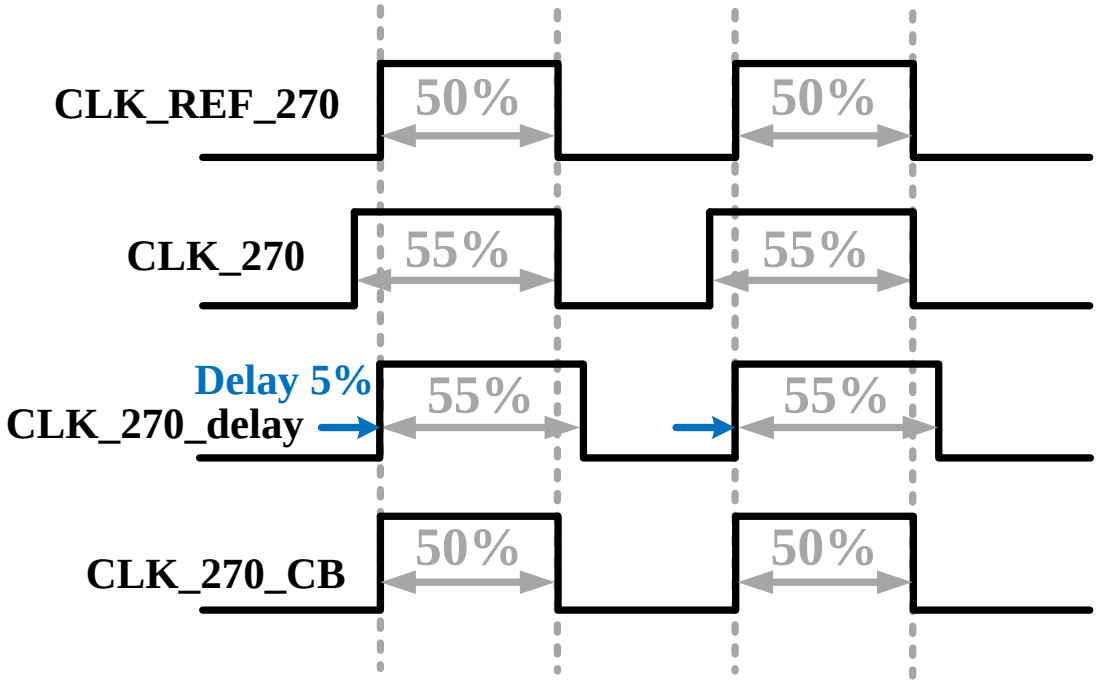

Fig. 4.19 The operation of the PWS circuit.

We assume that CLK_REF_270 is an ideal PWM signal we crave, whereas CLK_270 is the true one we get from the DLL. Recalling what we have mentioned in chapter 4-2, the output of the DLL is designed to be locked at the negative edge, and it has a little wider duty cycle than CLK_REF. Here we take CLK_270 with a 55% duty cycle for example. Incipiently, CLK_270 is transmitted to a DC, and then the DC delays CLK_270 to yield CLK_270_delay. Afterwards, CLK_270 and

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CLK_270_delay are passed through an AND gate to acquire CLK_270_CB. The OTA receives V_{IL4} and V_{ILavg}, both of which are produced by the current sensor, and represent the average inductor current in phase 270° and in all of the four-phase respectively. With the deviation of V_{IL4} and V_{ILavg}, the OTA amplifies their error and outputs a V_{ctrl_270} to adjust the delay magnitude of the DC. The DC continuously postpones CLK_270_delay, and thus the duty cycle of CLK_270_CB shrinks little by little to be aligned with CLK_REF_270. Lastly, V_{IL4} and V_{ILavg} become equal, V_{ctrl_270} of the OTA output keeps invariable, and the balance of the inductor current in phase 270° is finished. Such an instance also applies to CLK_90 and CLK_180. It is noteworthy that in view of the negative-edge-locked feature of the DLL, the PWM signals in each phase hold a precise and unaltered phase error of 90° despite the process of the unceasing calibration. In other words, aside from the duty cycle, the PWST can also correct the phase error meanwhile.

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Chapter5 Simulation and Measurement Results

5-1 Pre-simulation Results

The following simulation results of this part are all according to pre-sim results.

Fig. 5.1 – 5.3 show that when the load current steps up from 0.4A to 1.4A, the four-phase inductor currents balancing process (the upper part) and the transient response of the output voltage (the lower part) at three different corners are:

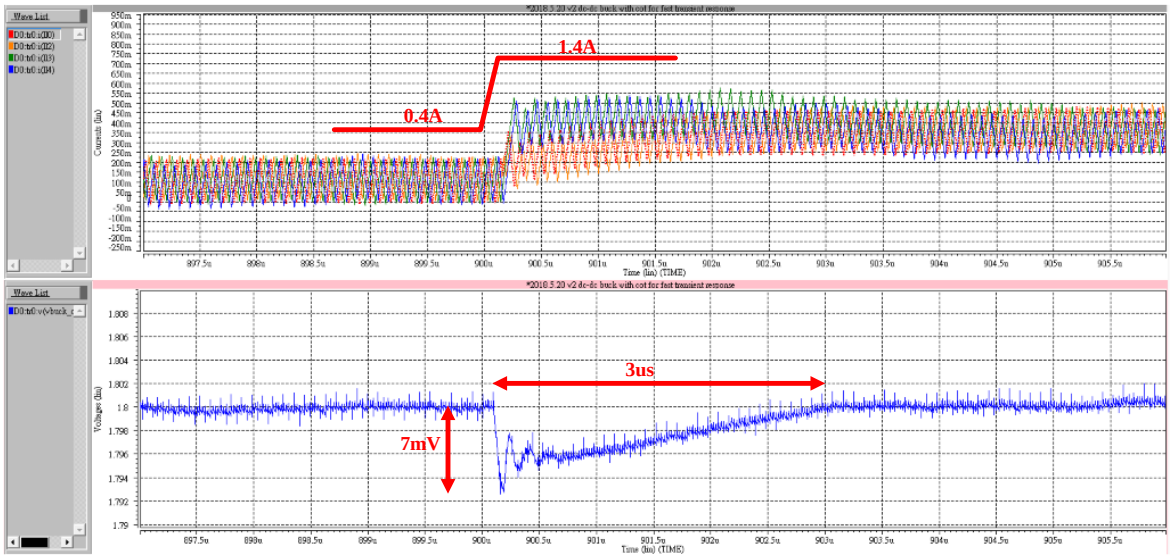

Fig. 5.1 Load current steps up from 0.4A to 1.4A.

(TT, 27°C, and with supply voltage of 3.3V)

Note that while the load current changes, the four-phase inductor currents are temporarily out of balancing. The reason is that the DLL is instantaneously out of lock and requires re-locking for a short time, which gives rise to momentary unbalancing of the four-phase inductor currents until the DLL finishes locking again.

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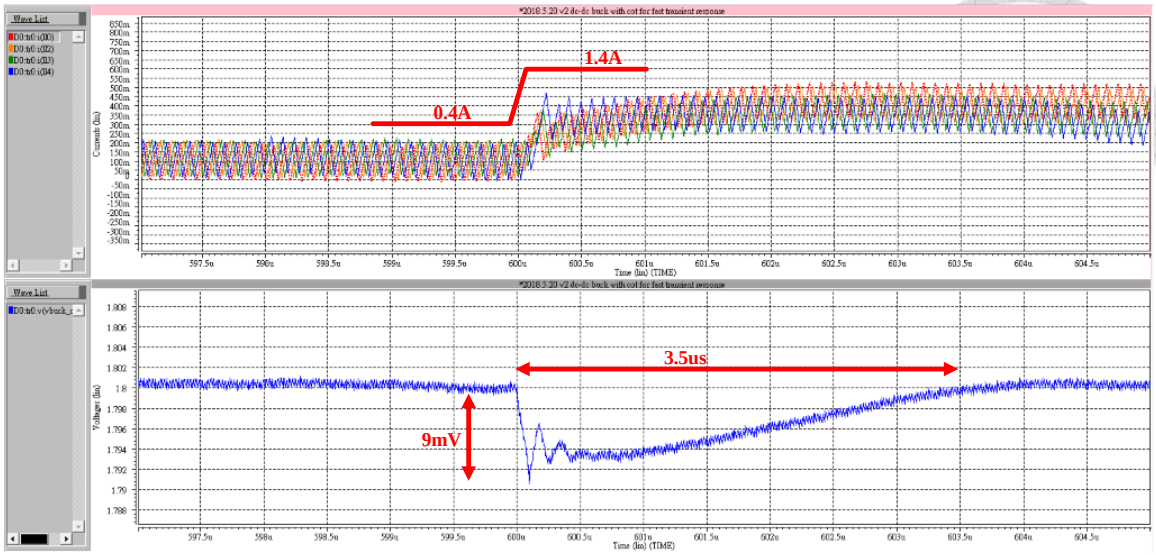

Fig. 5.2 Load current steps up from 0.4A to 1.4A.

(SS, 125°C, and with supply voltage of 2.97V)

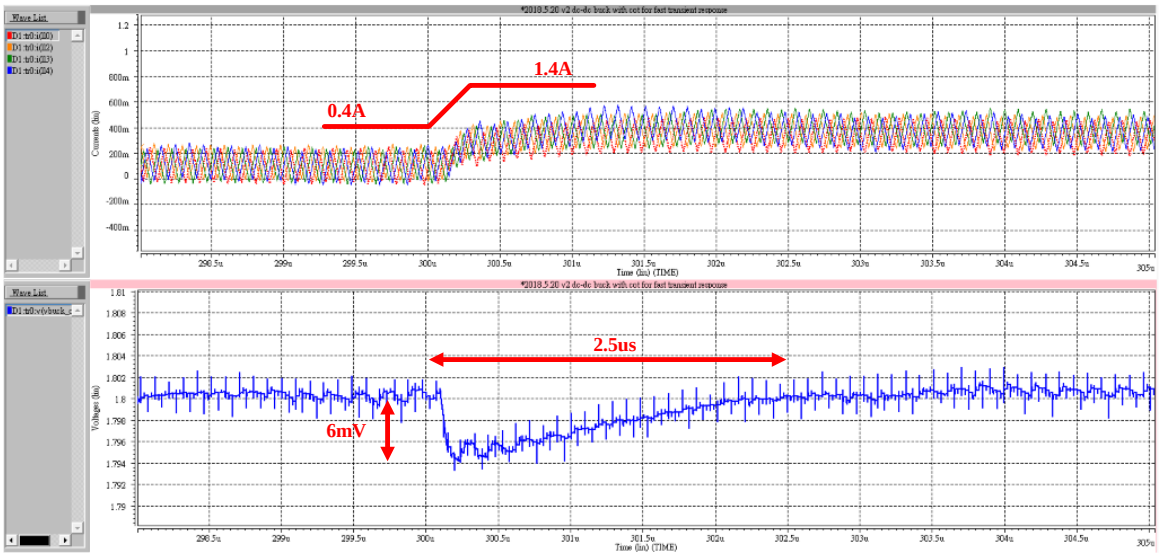

Fig. 5.3 Load current steps up from 0.4A to 1.4A.

(FF, -40°C, and with supply voltage of 3.63V)

Fig. 5.4 – 5.6 show that when the load current steps down from 1.4A to 0.4A, the four-phase inductor currents balancing process (the upper part) and the transient response of the output voltage (the lower part) at three different corners are:

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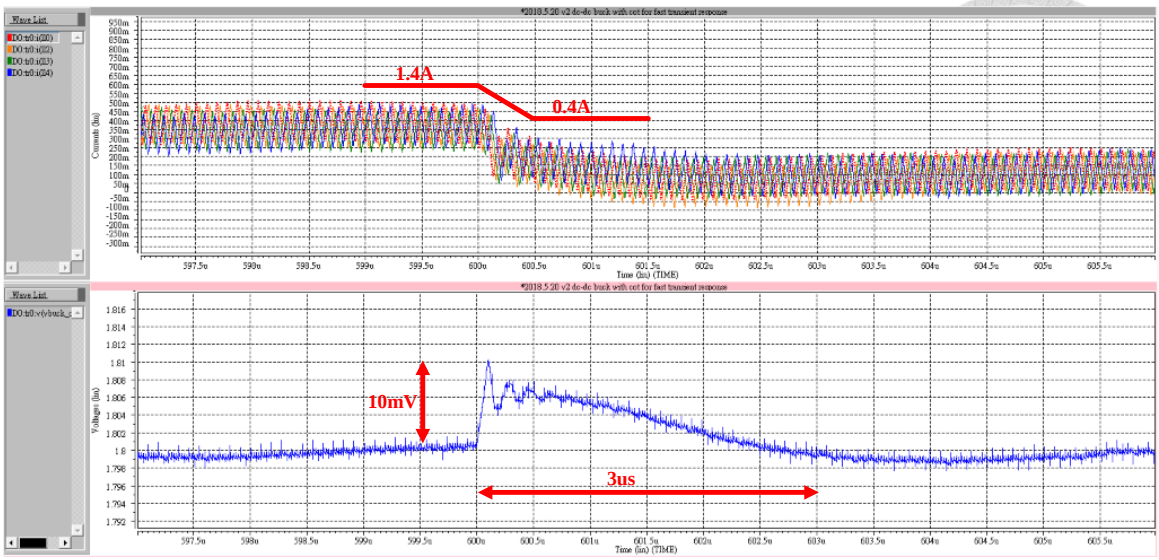

Fig. 5.4 Load current steps down from 1.4A to 0.4A.

(TT, 27℃, and with supply voltage of 3.3V)

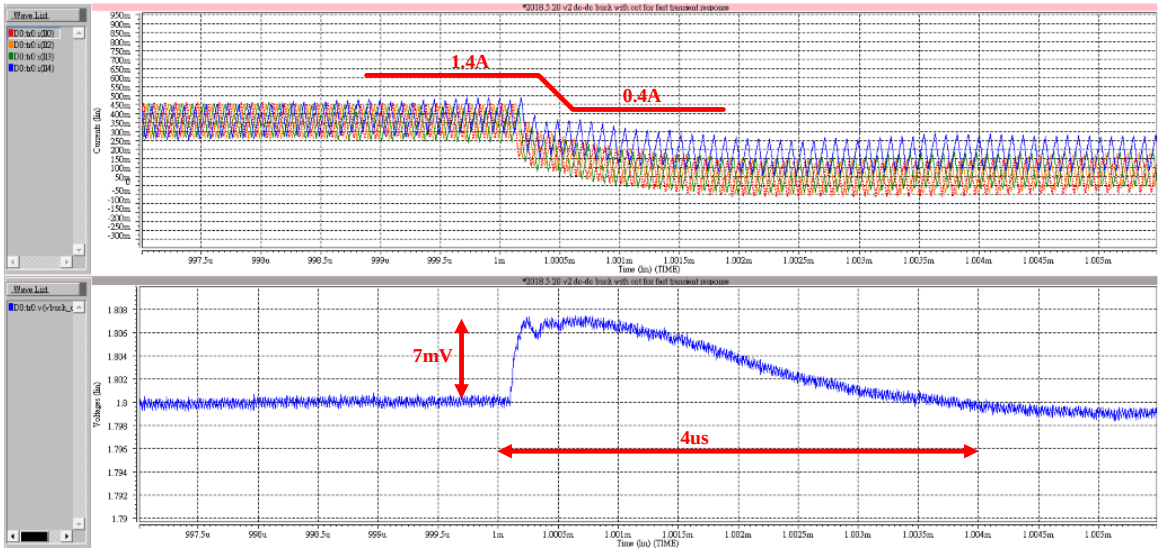

Fig. 5.5 Load current steps down from 1.4A to 0.4A.

(SS, 125℃, and with supply voltage of 2.97V)

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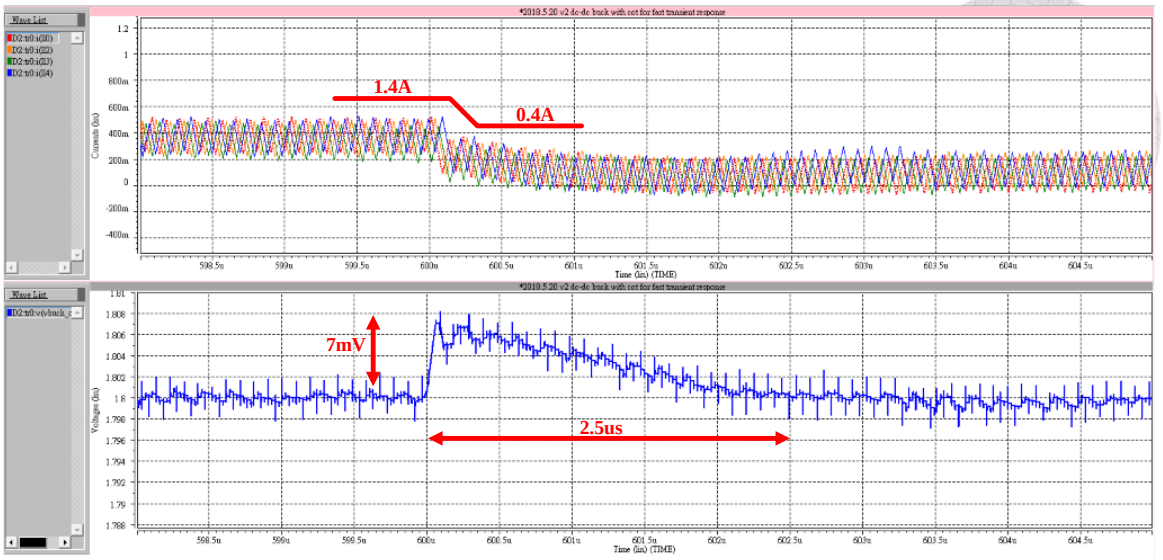

Fig. 5.6 Load current steps down from 1.4A to 0.4A.

(FF, -40°C, and with supply voltage of 3.63V)

Fig. 5.7 – 5.9 demonstrate that when the buck converter is in the light-load condition, the waveform of the four-phase inductor currents at three distinct corners are:

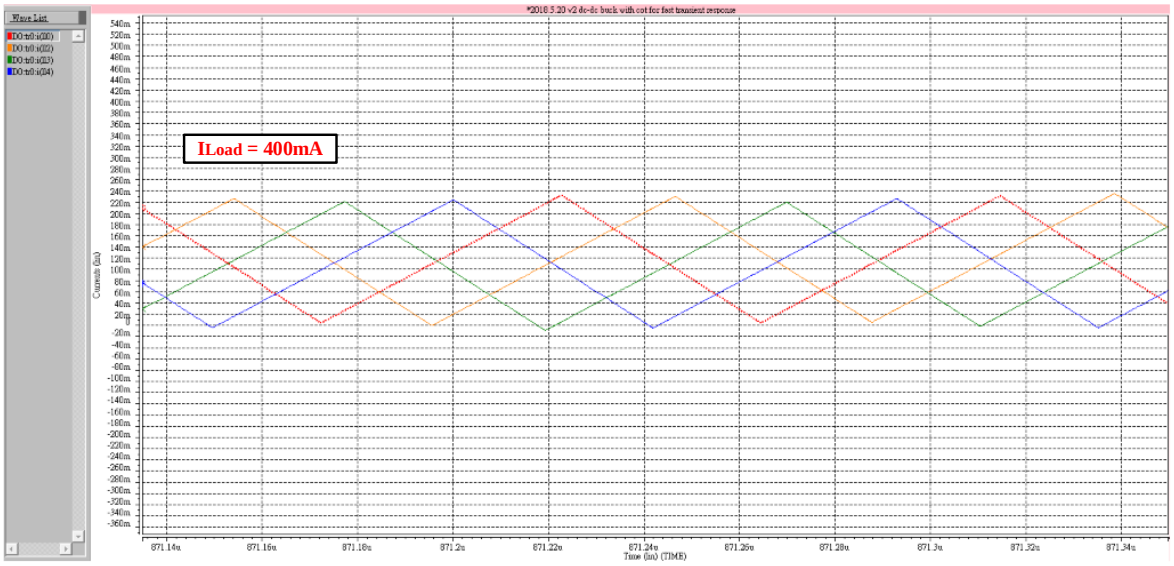

Fig. 5.7 The waveform of the four-phase inductor currents under the light load.

(TT, 27°C, and with supply voltage of 3.3V)

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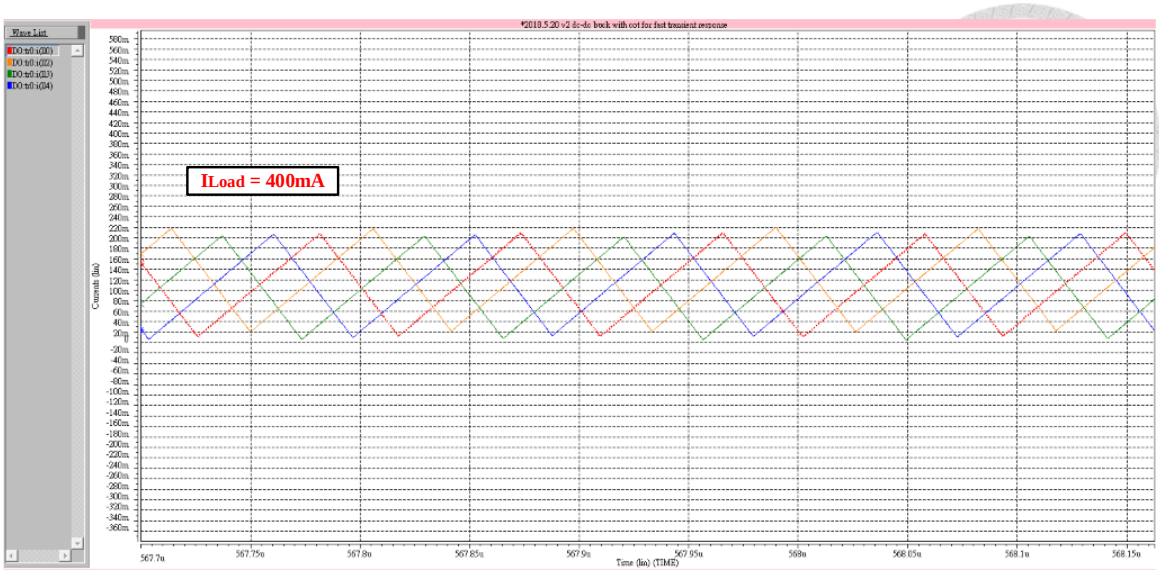

Fig. 5.8 The waveform of the four-phase inductor currents under the light load.

(SS, 125℃, and with supply voltage of 2.97V)

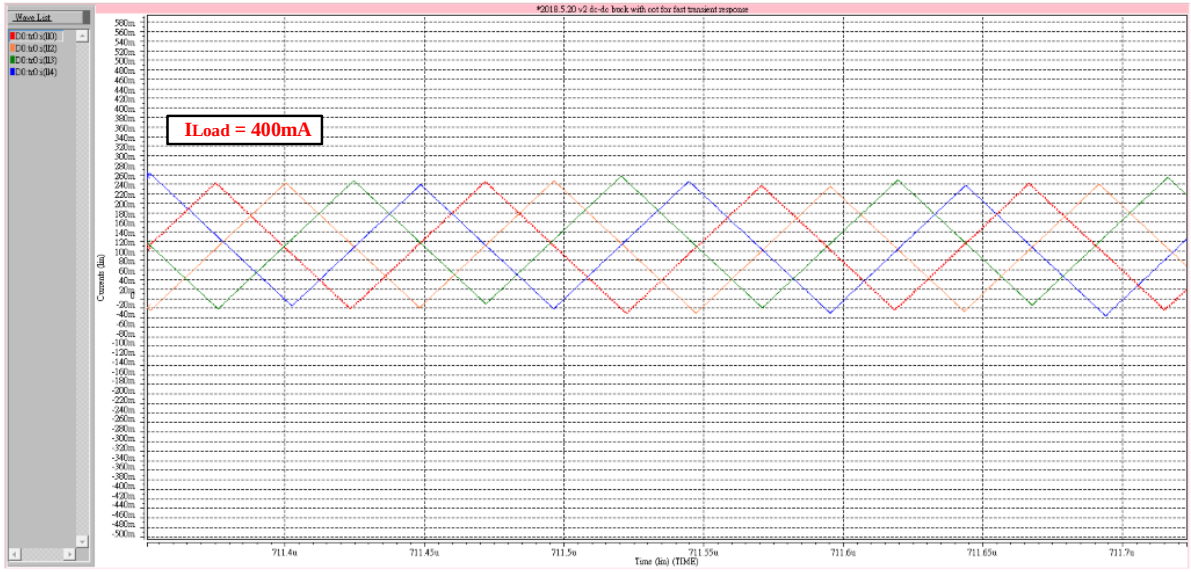

Fig. 5.9 The waveform of the four-phase inductor currents under the light load.

(FF, -40℃, and with supply voltage of 3.63V)

Fig. 5.10 – 5.12 demonstrate that when the buck converter is in the heavy-load condition, the waveform of the four-phase inductor currents at three distinct corners are:

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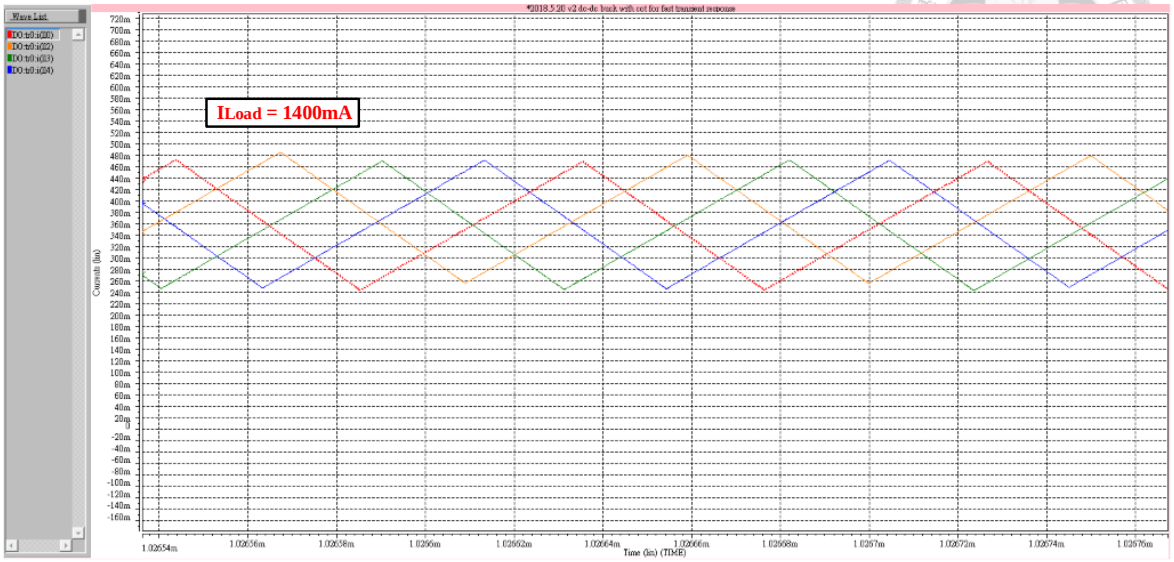

Fig. 5.10 The waveform of the four-phase inductor currents under the heavy load.

(TT, 27℃, and with supply voltage of 3.3V)

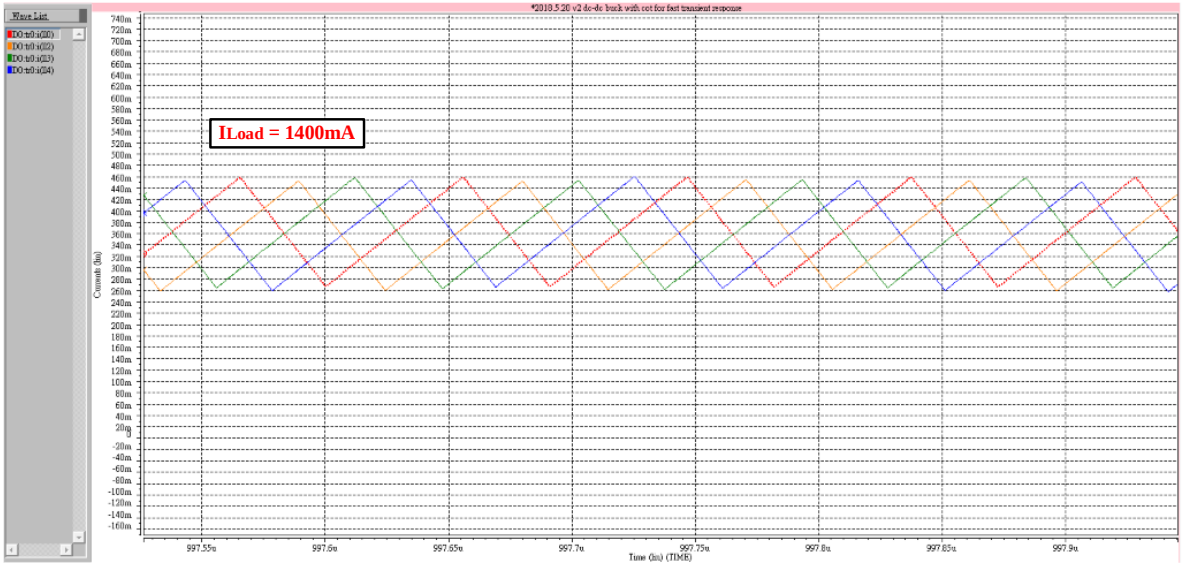

Fig. 5.11 The waveform of the four-phase inductor currents under the heavy load.

(SS, 125℃, and with supply voltage of 2.97V)

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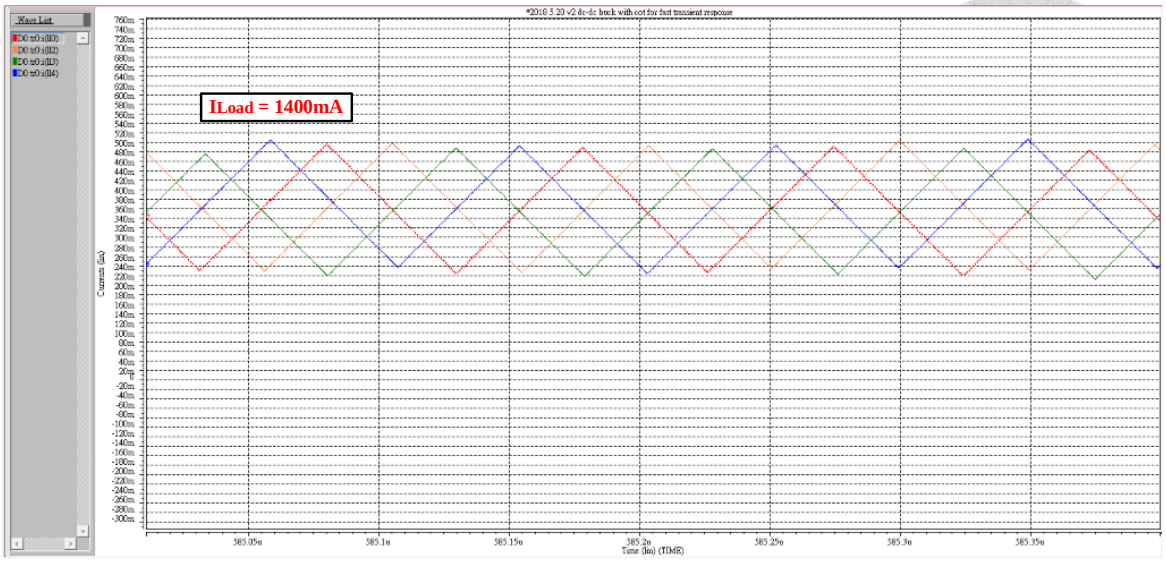

Fig. 5.12 The waveform of the four-phase inductor currents under the heavy load.

(FF, -40°C, and with supply voltage of 3.63V)

doi:10.6342/NTU201900285

5-2 Post-simulation Results

The following simulation results of this part are all according to post-sim results.

Fig. 5.13 – 5.15 manifest that when the load current steps up from 0.4A to 1.4A, the four-phase inductor currents balancing process (the upper part) and the transient response of the output voltage (the lower part) at three unequal corners are:

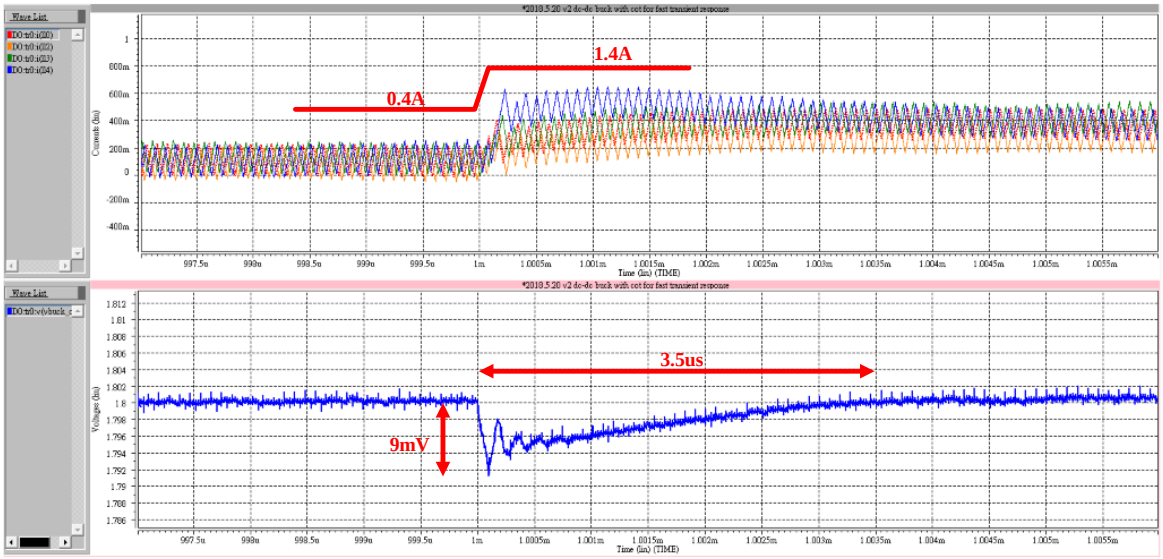

Fig. 5.13 Load current steps up from 0.4A to 1.4A.

(TT, 27℃, and with supply voltage of 3.3V)

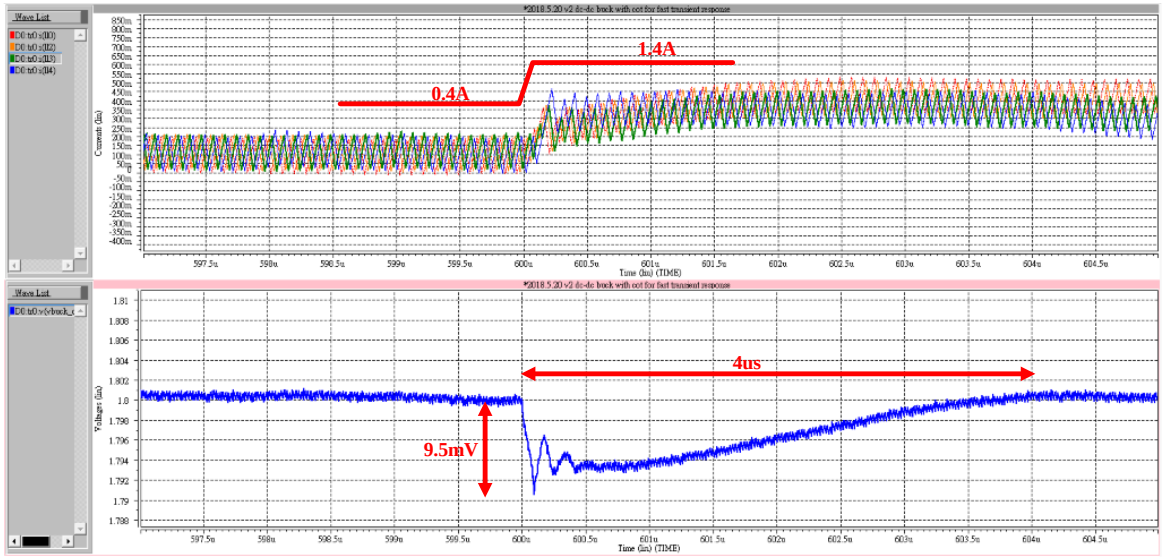

Fig. 5.14 Load current steps up from 0.4A to 1.4A.

(SS, 125℃, and with supply voltage of 2.97V)

doi:10.6342/NTU201900285

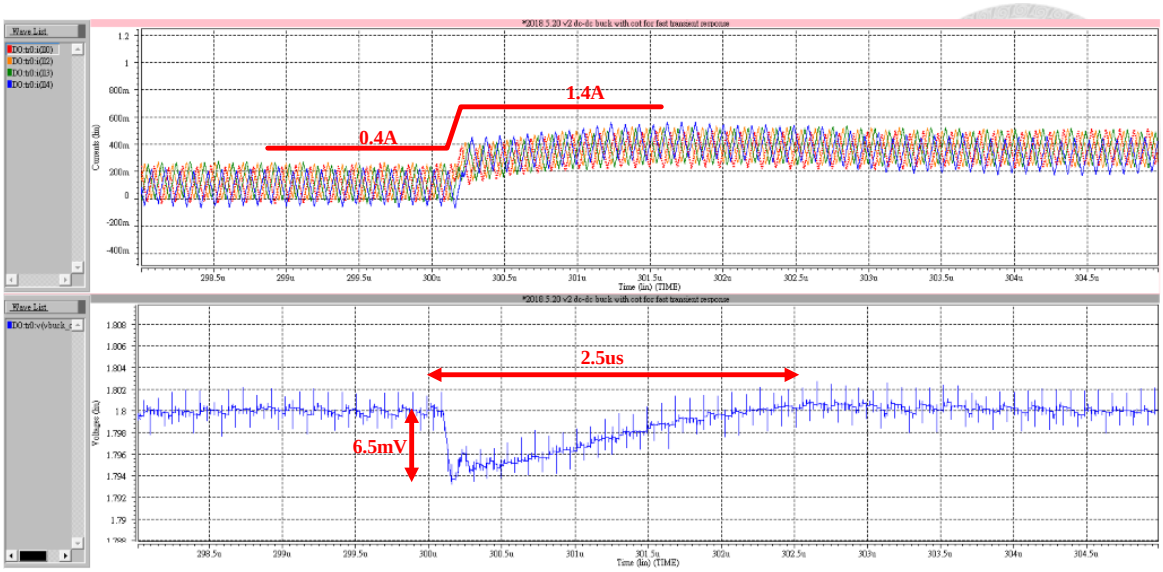

Fig. 5.15 Load current steps up from 0.4A to 1.4A.

(FF, -40°C, and with supply voltage of 3.63V)

Fig. 5.16 – 5.18 manifest that when the load current steps down from 1.4A to 0.4A, the four-phase inductor currents balancing process (the upper part) and the transient response of the output voltage (the lower part) at three unequal corners are:

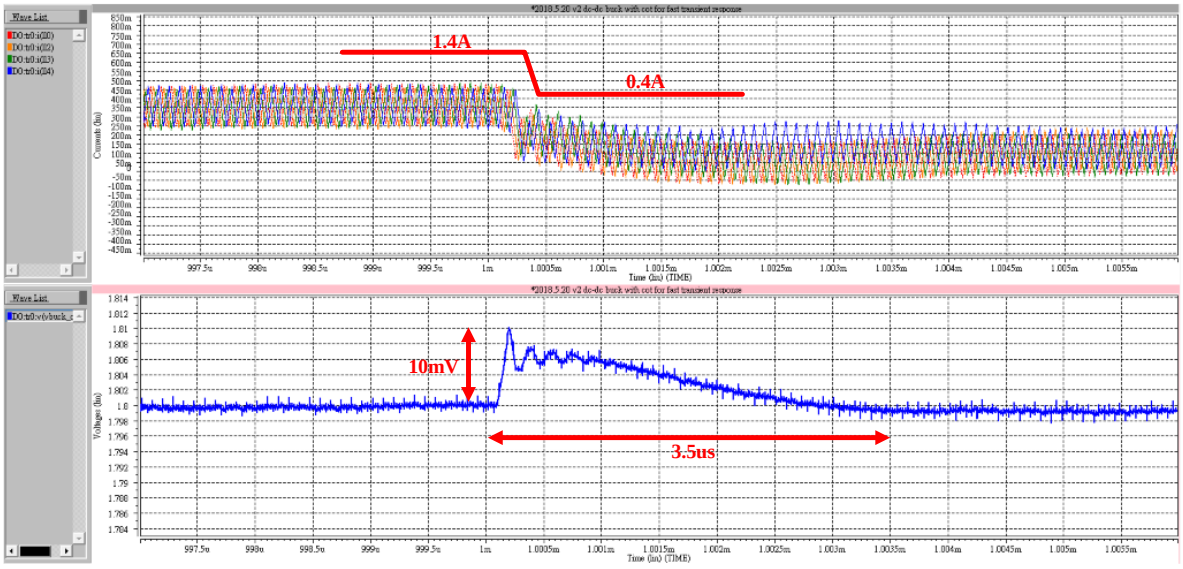

Fig. 5.16 Load current steps down from 1.4A to 0.4A.

(TT, 27°C, and with supply voltage of 3.3V)

doi:10.6342/NTU201900285

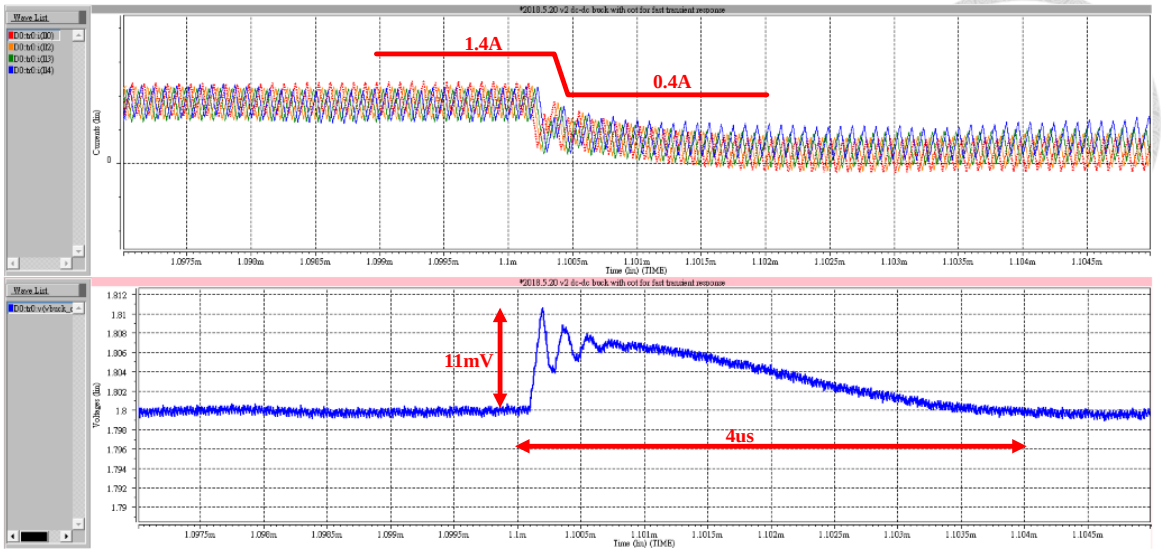

Fig. 5.17 Load current steps down from 1.4A to 0.4A.

(SS, 125℃, and with supply voltage of 2.97V)

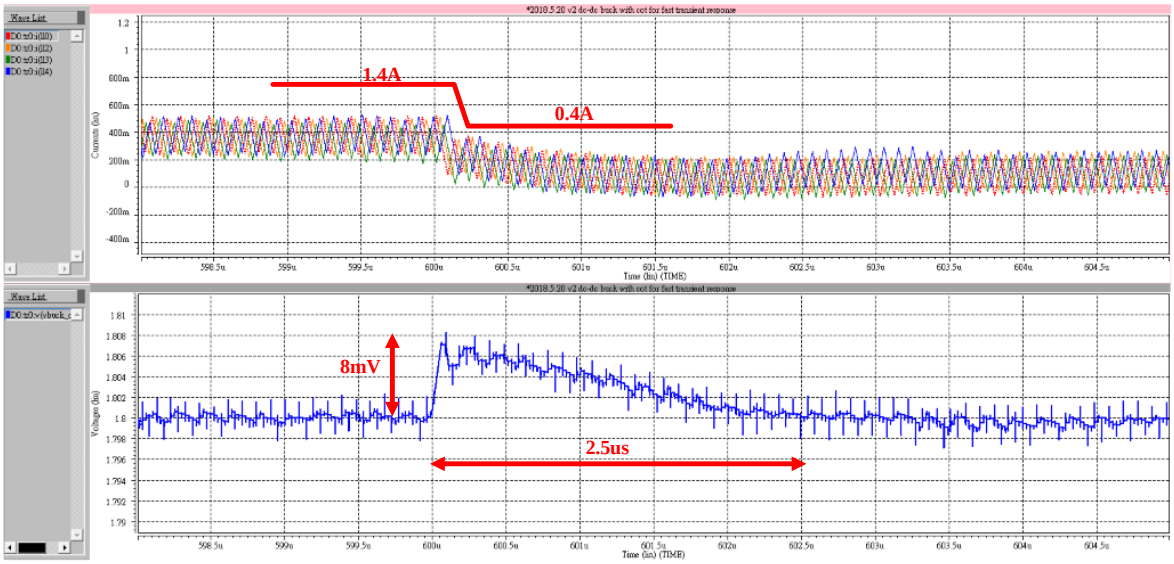

Fig. 5.18 Load current steps down from 1.4A to 0.4A.

(FF, -40℃, and with supply voltage of 3.63V)

Fig. 5.19 – 5.21 indicate that when the buck converter is in the light-load condition, the waveform of the four-phase inductor currents at three disparate corners are:

doi:10.6342/NTU201900285

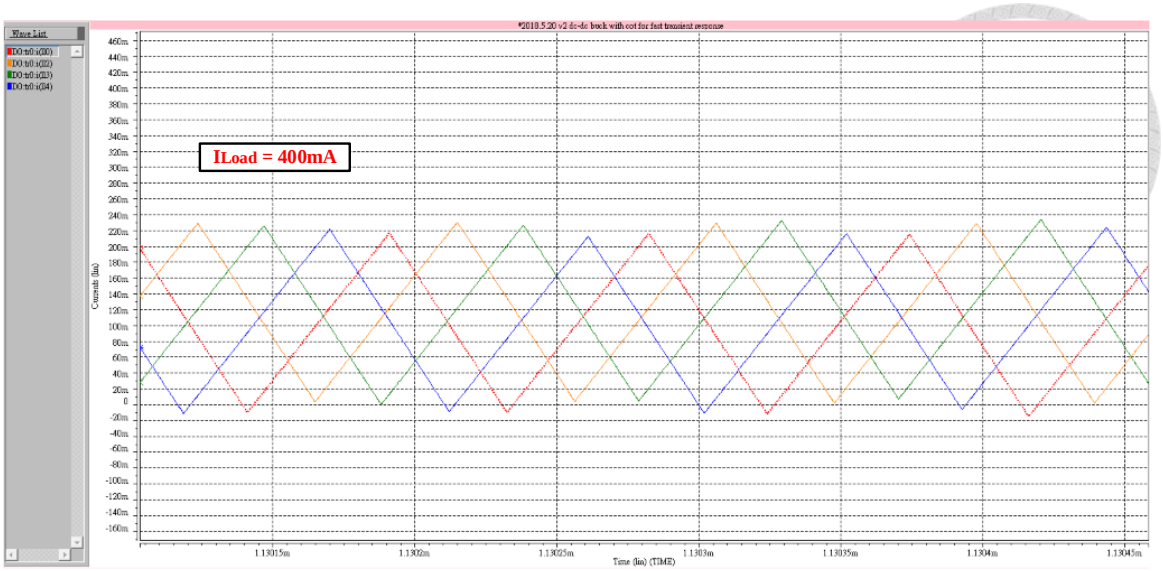

Fig. 5.19 The waveform of the four-phase inductor currents under the light load.

(TT, 27℃, and with supply voltage of 3.3V)

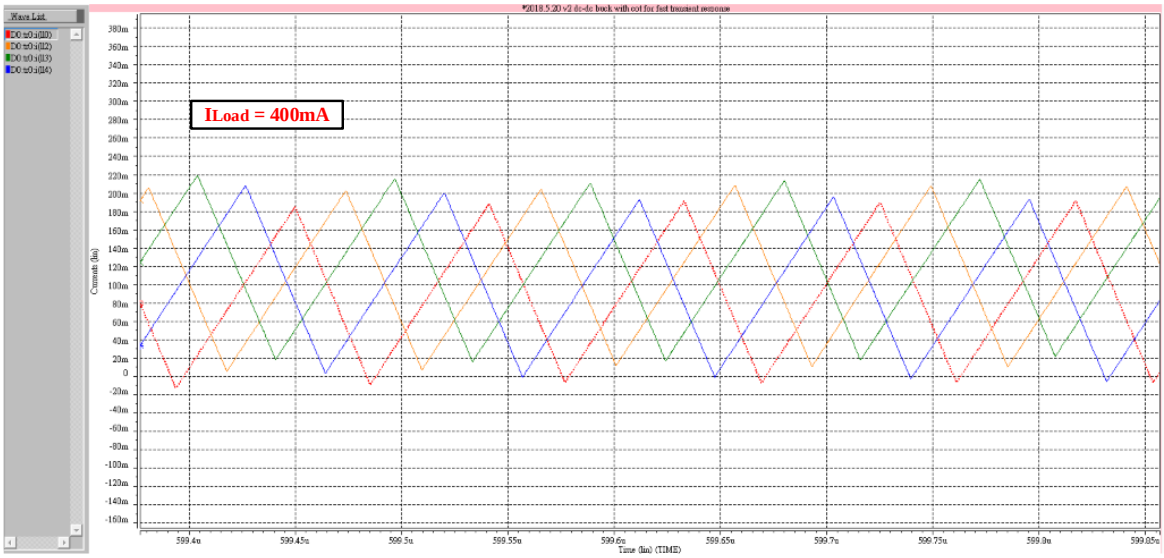

Fig. 5.20 The waveform of the four-phase inductor currents under the light load.

(SS, 125℃, and with supply voltage of 2.97V)

doi:10.6342/NTU201900285

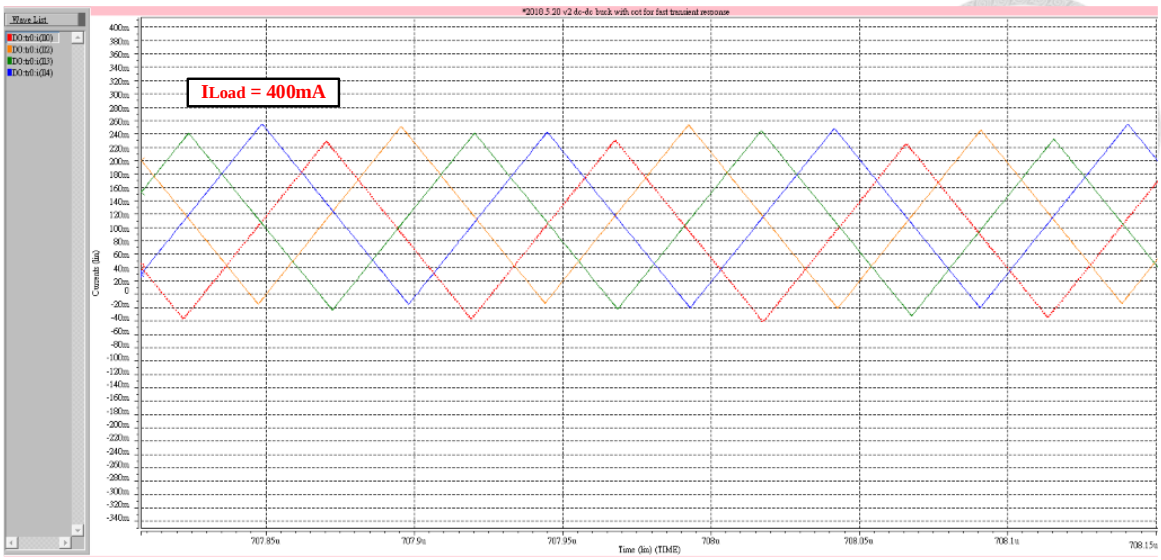

Fig. 5.21 The waveform of the four-phase inductor currents under the light load.

(FF, -40°C, and with supply voltage of 3.63V)

Fig. 5.22 – 5.24 indicate that when the buck converter is in the heavy-load condition, the waveform of the four-phase inductor currents at three disparate corners are:

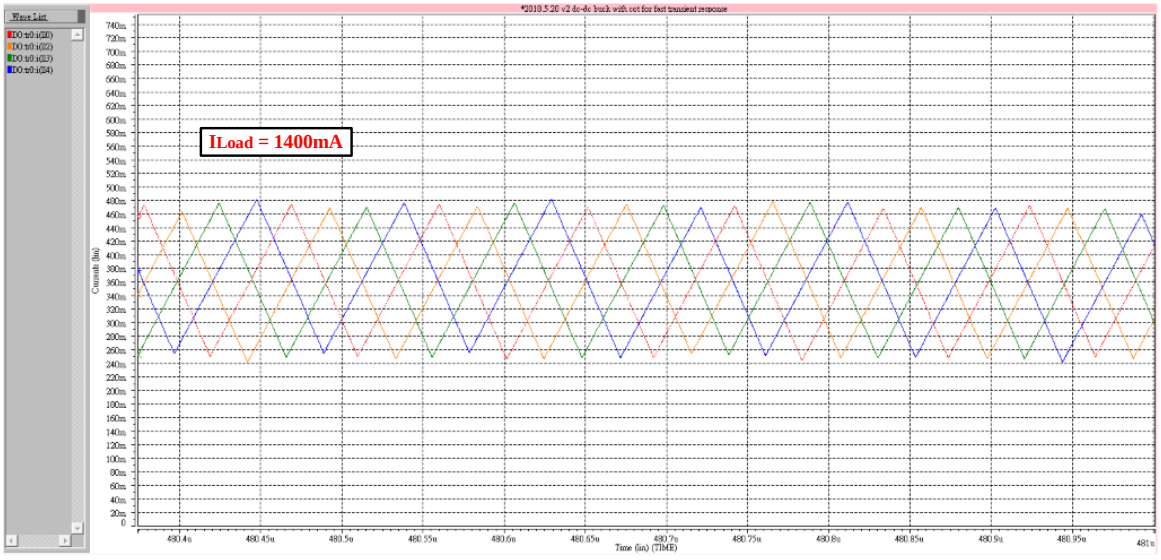

Fig. 5.22 The waveform of the four-phase inductor currents under the heavy load.

(TT, 27°C, and with supply voltage of 3.3V)

doi:10.6342/NTU201900285

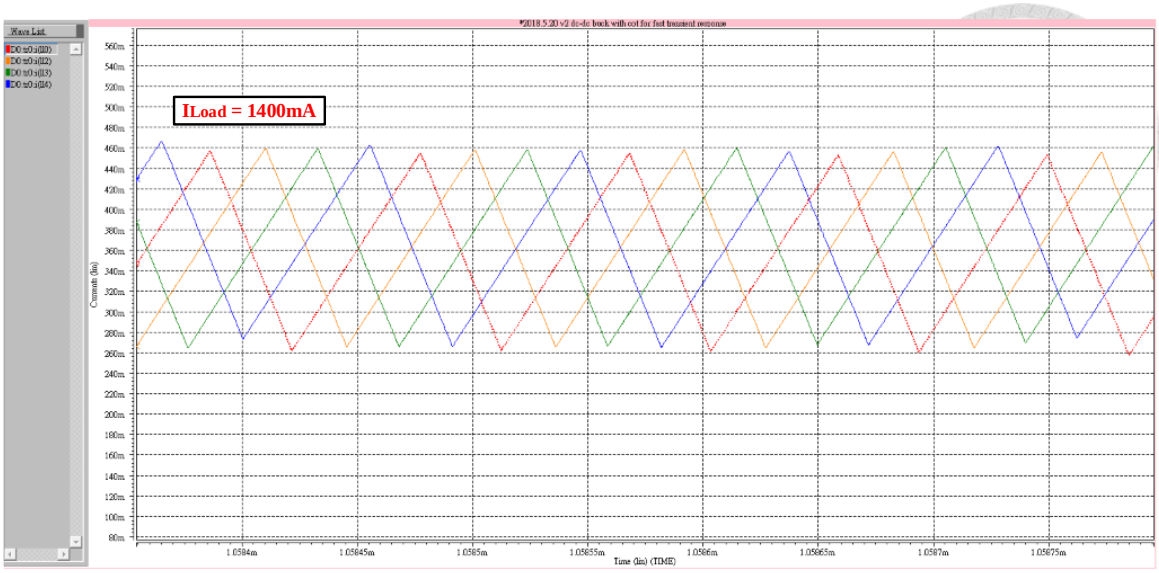

Fig. 5.23 The waveform of the four-phase inductor currents under the heavy load.

(SS, 125°C, and with supply voltage of 2.97V)

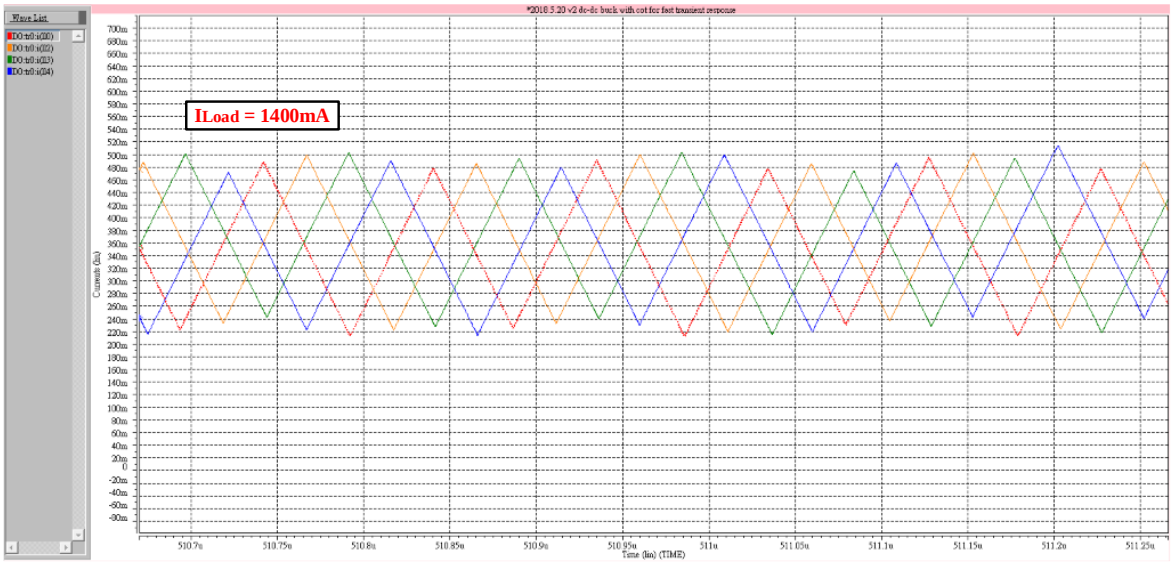

Fig. 5.24 The waveform of the four-phase inductor currents under the heavy load.

(FF, -40°C, and with supply voltage of 3.63V)

doi:10.6342/NTU201900285

In the end, we incorporate the pre-simulation and the post-simulation results, and list a comparison table, illustrated in Table 5.1. In summary, we can realize the extremely fast transient response and exceedingly small overshoot and undershoot voltage.

Table 5.1 The result comparison between the pre-sim and the post-sim.

Pre-simulation	**Step-up**		**Step-down**	
	Voltage Drop	**Transient Time**	**Voltage Peak**	**Transient Time**
TT 27°C 3.3V	**7mV**	**3μs**	**10mV**	**3μs**
SS 125°C 2.97V	**9mV**	**3.5μs**	**7mV**	**4μs**
FF -40°C 3.63V	**6mV**	**2.5μs**	**7mV**	**2.5μs**
Post-simulation	**Step-up**		**Step-down**	
	Voltage Drop	**Transient Time**	**Voltage Peak**	**Transient Time**
TT 27°C 3.3V	**9mV**	**3.5μs**	**10mV**	**3.5μs**
SS 125°C 2.97V	**9.5mV**	**4μs**	**11mV**	**4μs**
FF -40°C 3.63V	**6.5mV**	**2.5μs**	**8mV**	**2.5μs**

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5-3 Measurement Results

The chip is fabricated in TSMC 0.18μm 3.3V CMOS process. The layout and the die photo is illustrated in Fig. 5.25 and Fig. 5.26, respectively. The chip size totally occupies 2.3998mm * 2.5724 mm.

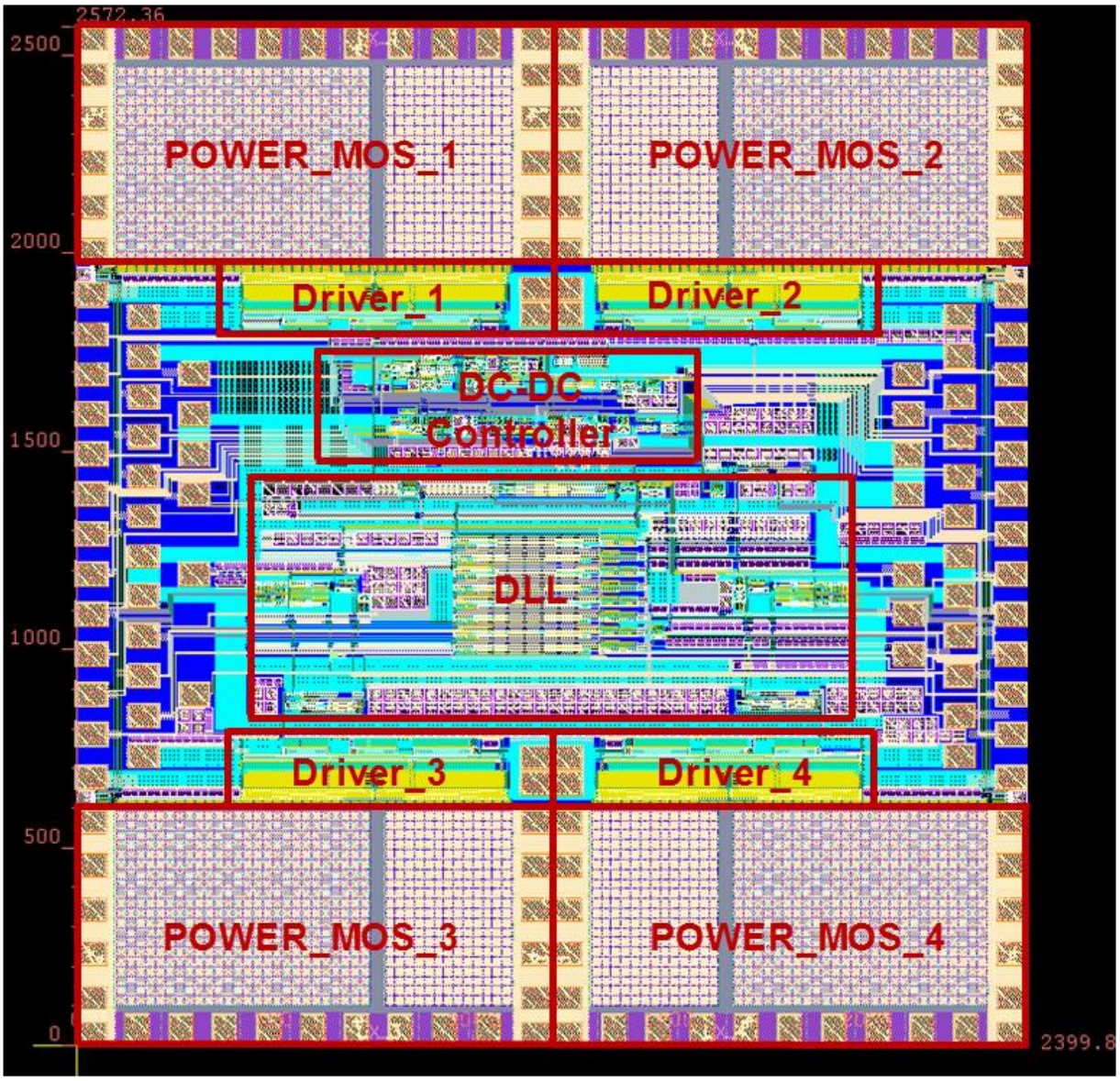

Fig. 5.25 The chip layout.

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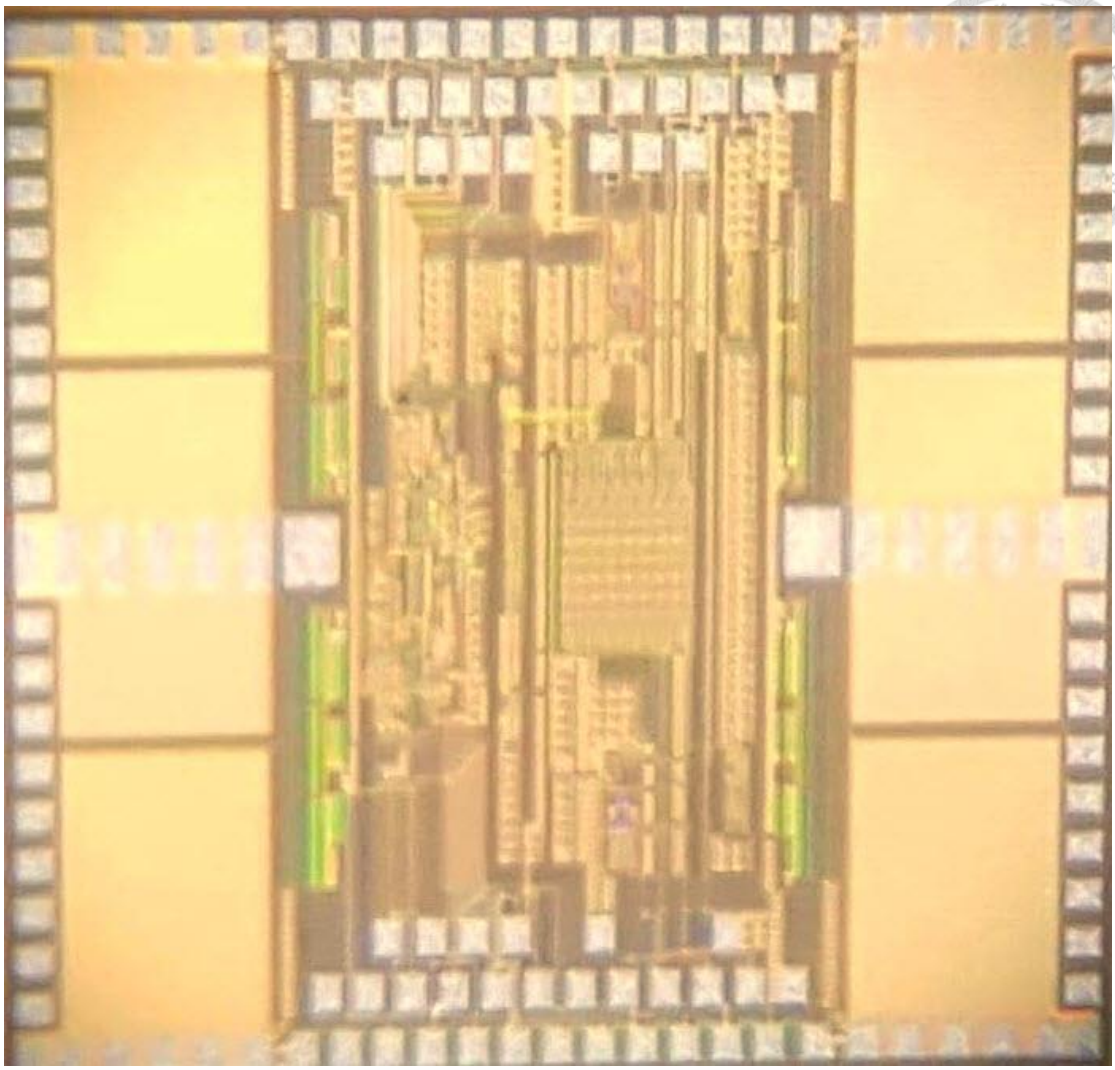

Fig. 5.26 The die photo.

doi:10.6342/NTU201900285

5-3-1 Measurement Setup

The measurement setup is expressed in Fig. 5.27. In order to maintain the stability of the voltage supply, we employ the linear voltage regulator (LM317), which is able to produce steady voltage. We also manipulate five power supplies, four of which provide the input voltages VIN_P in four phases, and drive the circuit with VDD_D. The last one serves LDO_ARRAY_1 and LDO_ARRAY_2 to generate VDD, bias voltage, and reference voltage. This chip offers three pins for adjusting the operating frequency. VTOOTH_COT and VTOOTH_SAW are used to regulate the switching frequency and the soft-start frequency, respectively. We can also acquire the information about the reference frequency of the DLL by observing VSAW_TO_FREQ, which prevents the DLL from out of lock. The output pin of the error amplifier in the first phase, referred to as VREF_OTA, is taken to set the resistors and the capacitors to compensate the system. Considering the convenience of measuring and debugging sub-circuits, we further design lots of switches, including VSS_EN, LT_DVS, VRAMP_EN, SEL_SAW, INCR_DELAY and DECR_DELAY.

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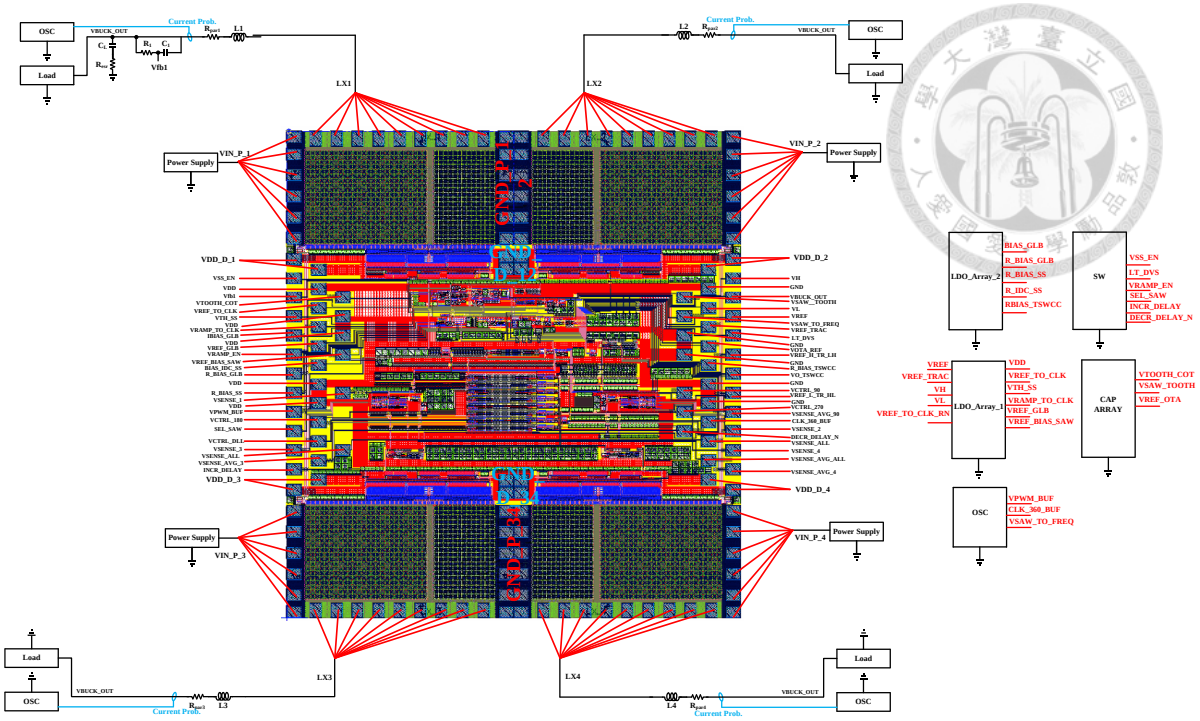

Fig. 5.27 The measurement setup.

As far as the measurement priority is concerned, we first confirm whether the buck converter in the main phase works normally and rightly or not. Next, we adopt Oscilloscope Agilent DSO80404B to check if the DLL is correctly locked by examining the waveforms of VPWM_BUF and CLK_360_BUF. At last, we measure the whole system, and the key points involve the stability of V_{OUT}, load transient response, reference tracking response and the effect of the four-phase current balancing.

The PCB board setup is pictured in Fig. 5.28, and its magnification photo is represented in Fig 5.29.

doi:10.6342/NTU201900285

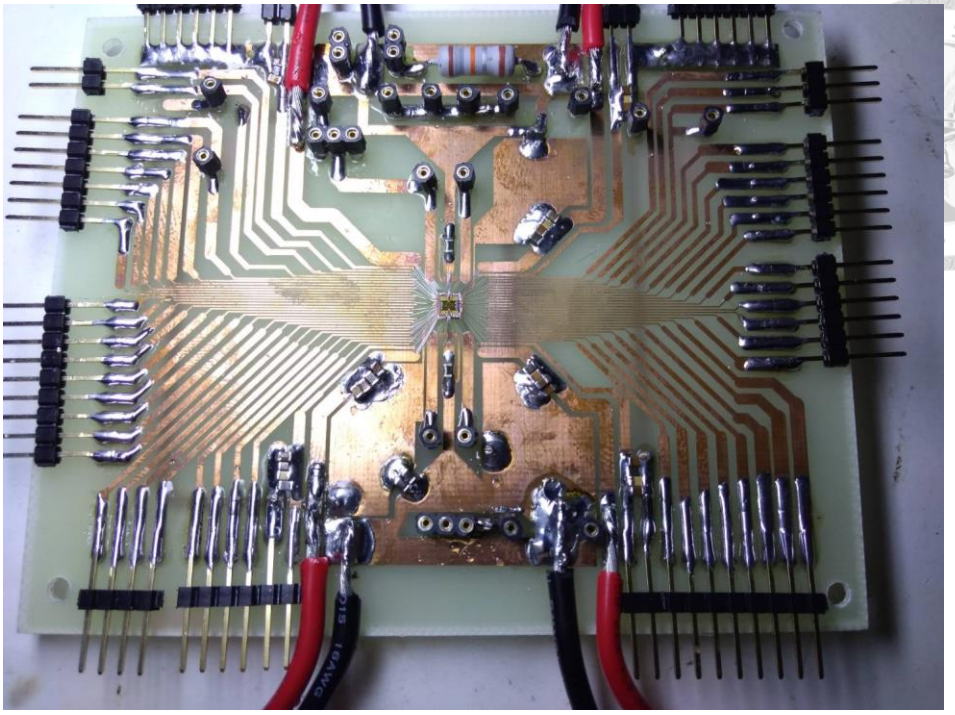

Fig. 5.28 The PCB board setup.

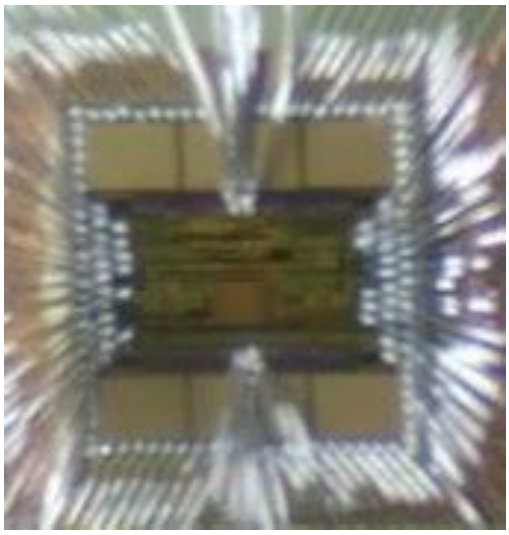

Fig. 5.29 The magnification photo of the PCB board setup.

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5-3-2 Measurement Waveforms

So far we have measured the single-phase buck converter in the main phase. The waveforms, including the inductor current I_L, V_{SUM}, the output voltage V_{OUT}, and V_{Lx}, are shown in Fig. 5.30 and Fig. 5.31.

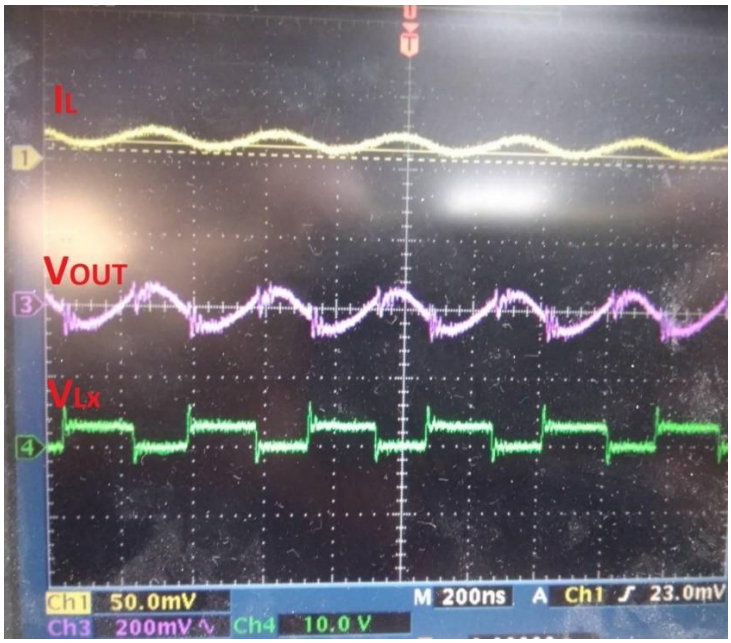

Fig. 5.30 The waveforms of I_L, V_{OUT}, and V_{Lx}.

Fig. 5.31 The waveforms of I_L, V_{SUM}, V_{OUT}, and V_{Lx}.

doi:10.6342/NTU201900285

As a result of the parasitic element effect, the switching frequency ranges only from 2.5MHz to 3.3MHz, which is too low to enable the proposed DLL to be locked. Therefore, the proposed four-phase buck converter, whose designed switching frequency is approximately 10MHz, does not work as anticipated. We have to try to solve the parasitic effect in the future.

Fig. 5.32 and Fig. 5.33 demonstrate how the output voltage responds when the output load current steps up and steps down.

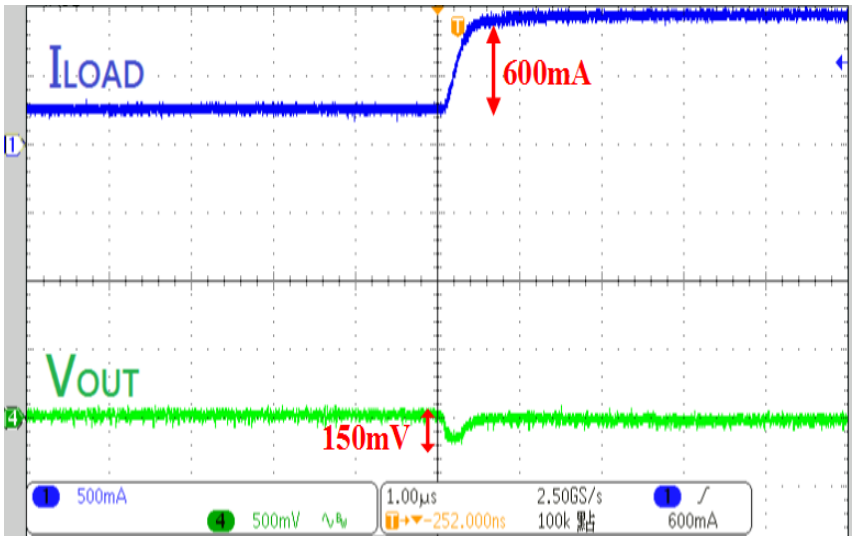

Fig. 5.32 The waveforms of I_{LOAD}, and V_{OUT} show when the load current steps up.

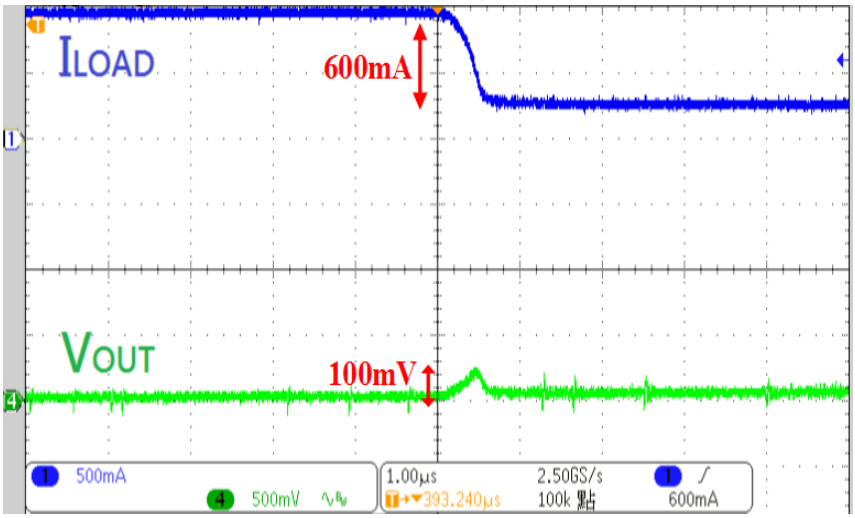

Fig. 5.33 The waveforms of I_{LOAD}, and V_{OUT} show when the load current steps down.

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Table 5.2 The measurement summary.

f_{SW}	**2.5 - 3.3 MHz**
ΔI_{LOAD}	**600 mA**
Voltage Drop	**150 mV**
Voltage Peak	**100 mV**

The measurement summary in Table 5.2 states that the proposed four-phase buck converter appropriately operates the loop solely in the first phase since the proposed DLL is out of lock. As a consequence, the load current does not provide high enough magnitude, and furthermore, the undershoot voltage and the overshoot voltage are much worse than the simulation results.

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Chapter6 Conclusion and Future Work

6-1 Conclusion

In order to achieve fast load transient response in the DLL-based four-phase buck converter, this work proposes an automatic switching single/dual edge triggered phase detector (ASS/DET-PD) applying to the fast-locking DLL. In addition, we employ transient-modulated constant on-time control (TMCOT) to further surmount the COT limitation, which leads to slow transient response. Ultimately, this research features a pulse-width-shrunk technique that solves the inductor current balancing problem to avoid aggravated output voltage ripple and declining in efficiency.

The simulation results expound the remarkable current balancing effect, accomplishing ultra-low undershoot and overshoot voltage, but unfortunately, the experimental results does not correspond with the desired results as the unexpected switching frequency occurs.

6-2 Future Work

The measurement results display the partial work of the proposed four-phase buck converter, which is due to parasitic element effect causing low switching frequency. In the future, we have to solve the parasitic effect problem incipiently, in particular parasitic capacitance, and then certify that our proposed work can carry out the inductor current balancing properly.

After fulfilling the inductor current balancing, this research can continue to raise the switching frequency, heighten the load current, contract the chip area, ameliorate the power density, etc.

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