國立臺灣大學電機資訊學院電子工程學研究所

碩士論文

Graduate Institute of Electronic Engineering
College of Electrical Engineering and Computer Science
National Taiwan University

Master Thesis

一個以雙迴路非同步控制之九十奈米十位元每秒取樣二億次的逐漸趨近式類比數位轉換器

A 10-bit 200-MS/s SAR ADC with Dual-loop Asynchronous Control in 90nm CMOS

許力元

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家人：謝謝爸媽還有兩個可愛的弟弟。

女友：謝謝妳的陪伴還有不放棄

台大 BL405 實驗室的大家

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中文摘要

本論文提出一個應用於逐漸趨近式類比至數位轉換器的電路設計技術，並且基於所提出的技術，實現一個使用九十奈米製程的單通道十位元每秒取樣二億次的非同步逐漸趨近式類比至數位轉換器。該技術為雙迴路非同步控制，其大幅降低因傳統非同步控制架構的現在，在最低有效位元階段造成時間浪費的問題，提升操作速度。

本設計使用台積電 90-nm UTM CMOS 製程來實作晶片，其核心的電路面積為 192 μm × 115 μm。佈局後模擬結果顯示，此設計在 0.9 伏特的電壓與每秒取樣二億取樣的操作速度下，總消耗功率為 1.61 mW，有效位元數為 9.26 bits，每次資料轉換所消耗的能量為 13fJ。預估最大 DNL 與 INL 的一個標準差分別為 0.298LSB 與 0.35 LSB。

本次設計已於 2019/07/10 下線，目前正在製作階段。排定於 2019/09/26 晶片製作完成

關鍵字：高速；非同步控制；逐漸趨近式；類比至數位轉換器

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ABSTRACT

This thesis proposes a control architecture for successive-approximation (SAR) analog-to-digital converters (ADCs). A single-channel 10-bit 200-MS/s asynchronous SAR ADC in 90-nm CMOS process was realized based on the proposed architecture. The proposed architecture is a dual-loop asynchronous control scheme. It reduce the waste time problem in LSB steps, which result from the architectural limitation of a conventional asynchronous control. Therefore, increase the speed.

The physical design was implement in TSMC 90-nm CMOS process. The core area is 115 μm × 192 μm. From post-layout simulation, at 0.9 V supply voltage and 200-MS/s sampling rate, the total power consumption is 1.61 mW, and ENOB is 9.26 bits. The prediction of maximum 1-sigma DNL and INL are 0.298 LSB and 0.35 LSB respectively

This design is in fabrication process and was taped out at 2019/07/10。The chip out was scheduled to 2019/09/26.

Keywords: high-speed, asynchronous control, successive approximation, analog-to-digital converter

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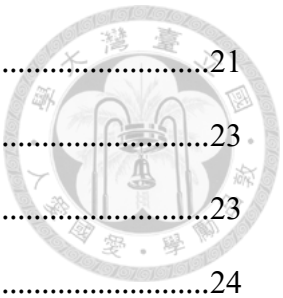

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Chapter 1 Introduction

1.1 Motivation

In the next five years, analog ICs are expected to show the strongest growth rate among major integrated circuit market categories, according a report from IC Insight [1]. The report forecasts that revenues for analog products—including both general purpose and application-specific devices—will increase by a compound annual growth rate of 6.6%. Fig. 1.1 shows the forecasted 2017-2022 growth rate of analog ICs among other categories compared to the projected total IC market annual growth rate during a five-year period. In analog ICs, data-converter ICs are widely used in the end-use applications such as communications and consumer applications as components. Data-converters are forecast to continue growing with double-digit sales gains expected in three of the next five years.

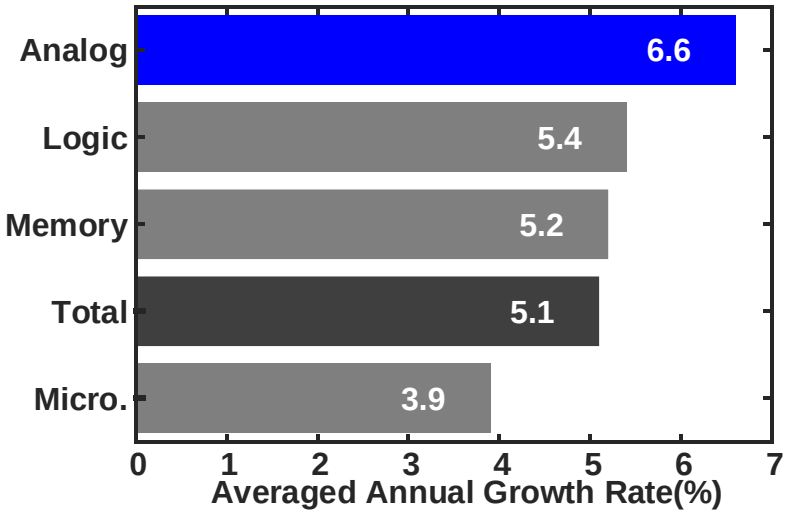

Fig. 1.1 Growth rate forecast of IC markets (2017-2022F)

Analog-to-digital converters (ADCs) are a kind of data-converter ICs. They perform the function of converting continuous-time and continuous-amplitude analog signal to the discrete-time and discrete-amplitude digital signal, a main function in signal processing.

There are many types of ADC which can be categorized by their specification,

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typically by sampling frequency and resolution. The Flash ADC is ranked for highest sampling frequency (1GS/s to tens GS/s) and with lowest resolution. The pipelined ADC, which ranged from high sampling frequency (up to several hundred MS/s) with medium-to-high resolution, and the successive-approximation-register (SAR) ADC, which is low-to-medium sampling frequency (tens MS/s) and low-to-medium resolution. There are still other types of ADC derived from the mentioned ones above. Fig. 1.2 shows all kinds of ADC described above.

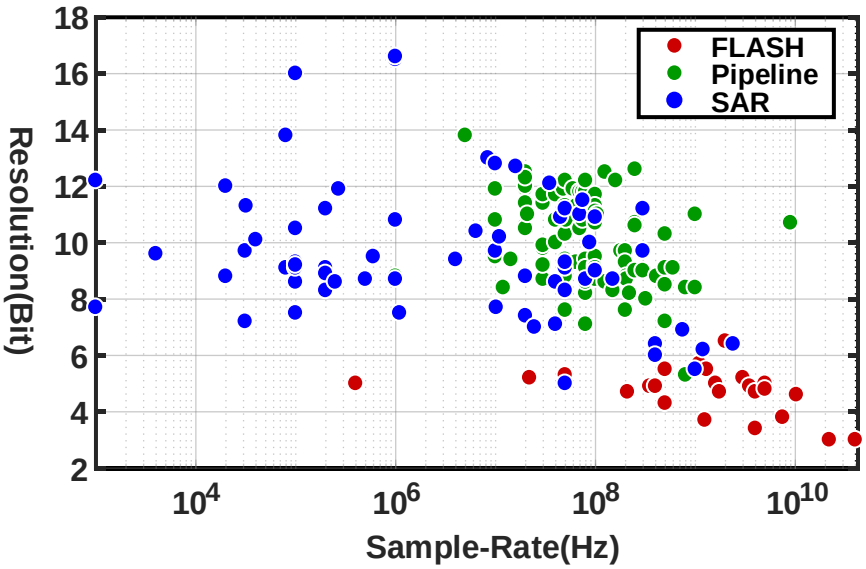

Fig. 1.2 Resolution and sampling frequency of ADC from ISSCC and VLSI

As feature size of CMOS device keep down scaling, the speed of digital circuits gain many benefits because of the parasitic capacitances of device shrinking. Furthermore, the supply voltage of CMOS devices has also decreased to around one volt, which helps reduce power dissipation of digital circuits. However, from the perspective view of analog circuit, lower supply voltage means lower analog signal swing thus lower SNR and larger variation. As most functional blocks are digital circuits, however, the successive approximation register (SAR) ADC evolution rapidly during recent years. A SAR ADC typically consists of a single comparator, a capacitive-DAC (CDAC), a sample-and-hold

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and a control logic, which are all very suitable for low voltage operation since all of these can functionally work in a wide range of operating voltage. In addition, small feature size means the SAR control logic can operate in a high-speed, thus not only the operating voltage, but also the performance of SAR ADC has improved. Fig. 1.3 shows a trend of high speed ADCs from 2000 to 2018 [2]. The SAR-based time-interleaved ADC has replace the role of FLASH type ADC in the ultra-high sampling frequency.

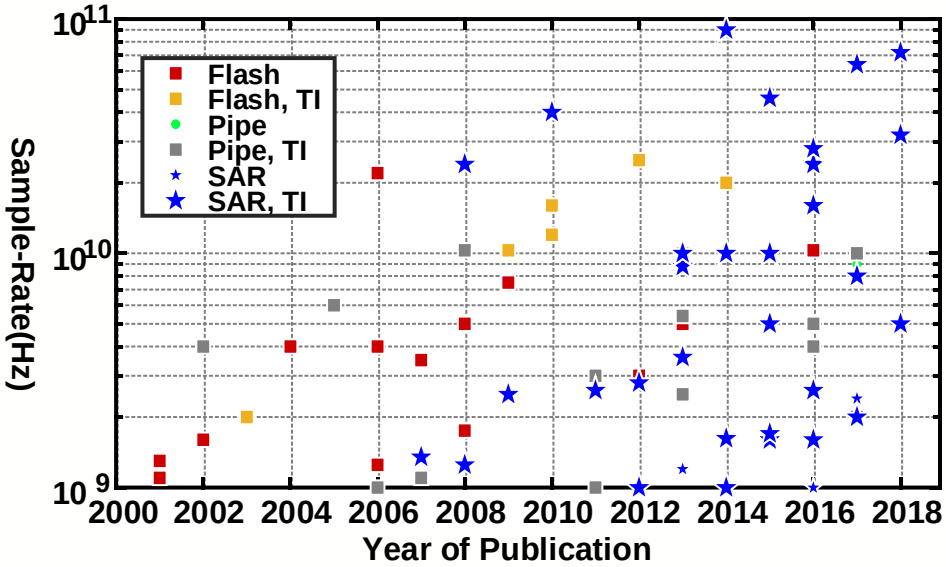

Fig. 1.3 Architecture Trends of ultra-high speed ADC

Recent researches for improving sampling frequency of SAR ADC have been published. Self-timing control logics [3]-[6] make the controlling clock of the comparator in a SAR ADC become self-adaption. The comparator circuit of SAR ADC also improved in comparison speed by using double-tail current [7]-[9] or high gain preamp [10]-[12] to break the need for compromising between noise and speed of the traditional latch-type comparator [13]-[15]. Various redundancy techniques [16]-[22]have been proposed to relax the CDAC settling time. Implementation of SAR logic with latch circuits [23]-[25] replace edge-triggered flip-flop to reduce logic delay and simply the complexity. There are still other techniques [26]-[29] were proposed to increase the speed of SAR ADC.

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1.2 Thesis Organization

The organizations of this thesis focus on high-speed SAR ADC design.

Chapter 2 introduce the general behaviors of an ADC that commonly used in evaluating its performance.

Chapter 3 introduce SAR ADC operation and analyze

Chapter 4 illustrates the design and circuit of the proposed SAR ADC.

Chapter 5 present the physical design of the proposed SAR ADC and its post-layout simulation

Chapter 6 is the measurement considerations

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Chapter 2 Fundamentals of Analog-to-Digital Conversion

This chapter go through fundamentals of analog-to-digital(A/D) conversion. Section 2.1, introduce two basic A/D functions, sampling and quantization. Section 2.2 and 2.3 gives some important performance metrics used to evaluate A/D conversion. They are categorized into static specifications and dynamic specifications.

2.1 Introduction

As a bridge between analog and digital world, A/D conversion bring information in nature phenomena, into digital data formats that can be used in computation. Fig. 2.1 shows this concept. First, we use sensors to transduce nature signals like sound, pressures, luminance and so on to analog signals, typically in the electronic forms. Then sampling and quantizing them into digital words.

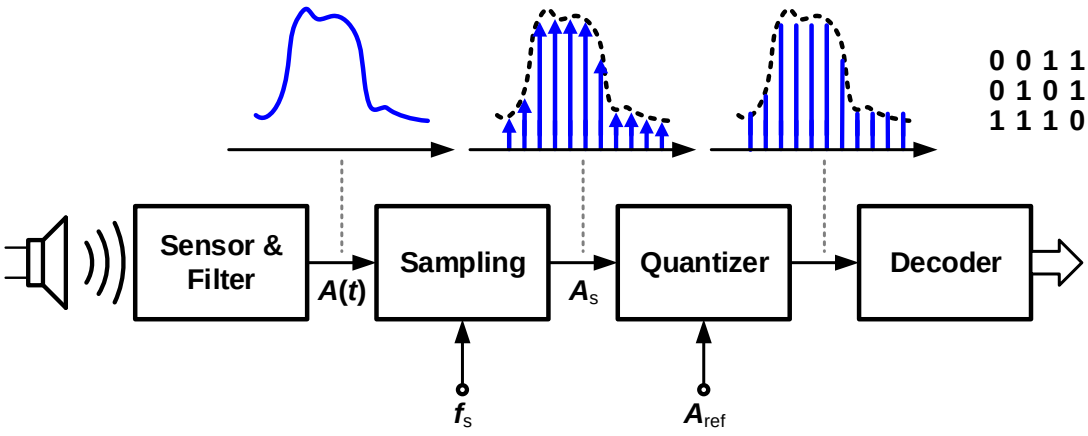

Fig. 2.1 Concept of Analog-to-digital Conversion

2.1.1 Sampling

Sampling functions often locate at the most front-end of A/D conversion in order to relax the timing requirements of quantization. They sample an analog waveform and store the results in memory elements. An ideal sampling scheme is a period train of impulses

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multiple an analog waveform,A(t). Fig. 2.2 depict this scheme.

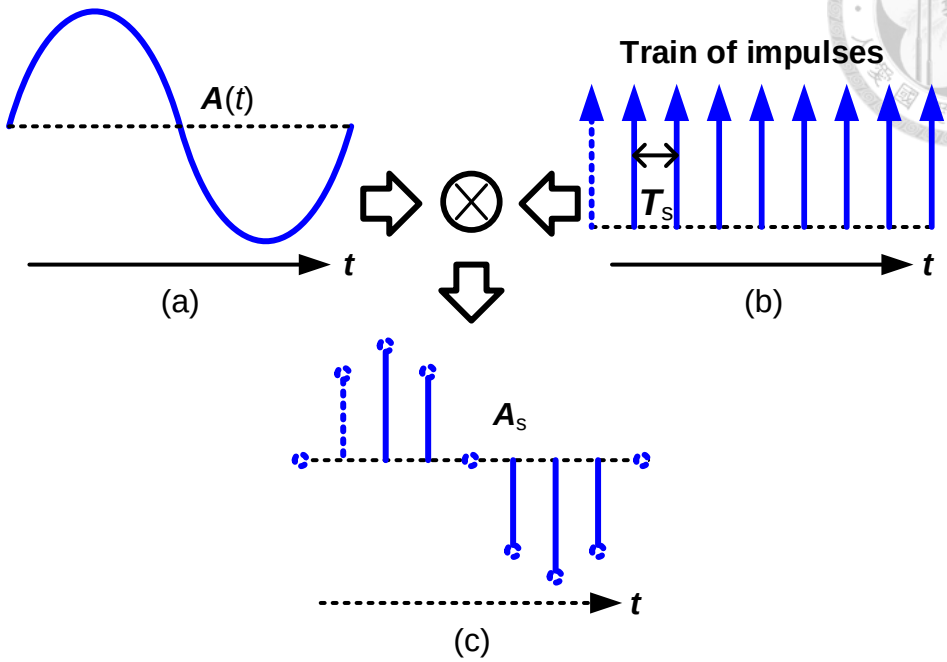

Fig. 2.2 An ideal sampling scheme, (a) analog input,(b) ideal sampling signal and (c) sampled signal of (a)

An ideal sampled signal in the above figure can be expressed by the following equation

$$A_s(t) = A(t) \times \sum_{i=-\infty}^{+\infty} \delta(t - iT_s)$$

where $\delta(\cdot)$ is the Dirac delta function and T_s is the time interval of sampling instants. Eq2.1 is the time domain representation of sampling. When analyze the effect of sampling a signal, we use Fourier Transform (FT) to express $A_s(t)$ in the frequency domain.

$$A_s(j\omega) = \frac{1}{T_s} \times \sum_{i=-\infty}^{+\infty} A(j(\omega - i\omega_s))$$

Eq2.2 reveals that after sampling, the sampled signal in frequency domain is the sum of shifted versions of the frequency representation of the original analog waveform.

Before going further discuss on eq2.2, it has been rise that we have to use a sampling

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signal which is shaped as like the Dirac delta function. Since the Dirac delta function only exist in theory, it does not arise anywhere in a practical physical realization. A more practical description of sampling an analog waveform is using a track-and-hold (T&H) signal. A T&H scheme using a rectangular wave like fig2.3b to "track" the input signal during tracking (acquisition) time. The remaining duration in a period is called a hold time where the last tracking moment of an input signal is stored and keep.

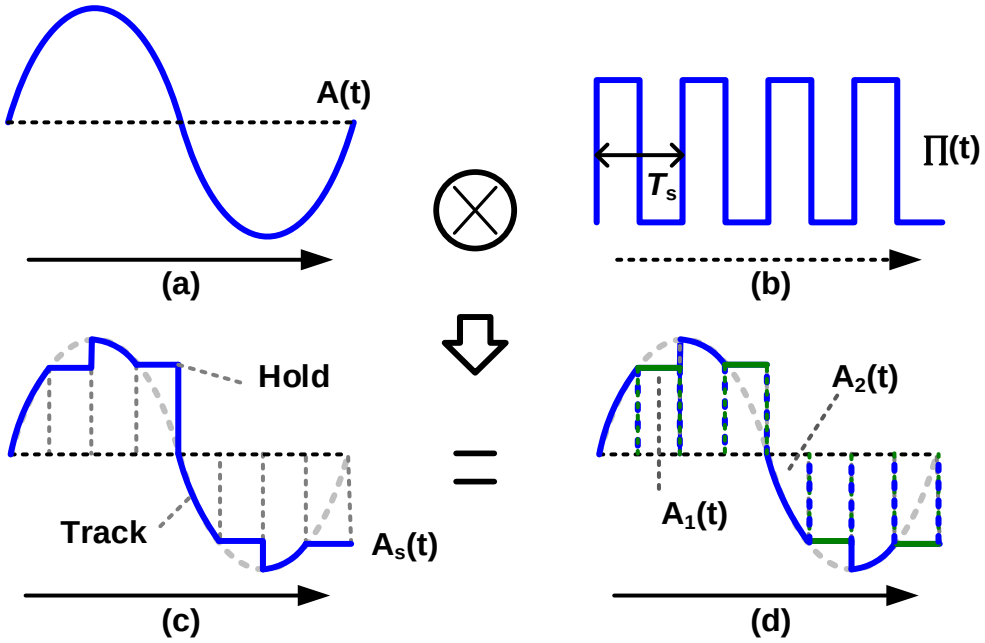

Fig. 2.3 An track-and-hold sampling scheme, (a) analog input,(b) T&H signal,(c) sampled signal using T&H and (d) another expression of (c)

Assuming the acquisition and hold time each occupy half in a period, the sampled waveform in fig. 2.3c can be decomposed into two modified rectangular waves, $A_1(t)$ and $A_2(t)$, as shown in fig2.4d.

$$A_s(t) = A_1(t) + A_2(t)$$

$A_1(t)$ is the hold portion of the T&H output whose amplitude is the hold values

$$A_1(t) = \left[A(t) \sum_{i=-\infty}^{+\infty} \delta(t - iT_s - \frac{T_s}{2})\right] \otimes \Pi\left(\frac{2t}{T_s} - \frac{1}{2}\right)$$

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$A_2(t)$ is the track portion of $A_s(t)$

$$A_2(t) = A(t)\left[\Pi\left(\frac{2t}{T_s} - \frac{1}{2}\right) \otimes \sum_{i=-\infty}^{+\infty} \delta(t - iT_s)\right]$$

The output spectrum is the sum of eq 2.5 and 2.6 in the frequency domain

$$A_s(f) = e^{-3j\pi f T_s/2} \frac{\sin(\pi f T_s/2)}{\pi f T_s} \sum_{i=-\infty}^{+\infty} A\left(f - \frac{i}{T_s}\right) + \sum_{i=-\infty}^{+\infty} e^{-ji\pi/2} \frac{\sin(i\pi/2)}{i\pi} A\left(f - \frac{i}{T_s}\right)$$

All summation terms in eq2.5 contain with sinc function. It means that the output amplitude is attenuated. For example, as f approach $2/T_s$, the attenuation result in eq 2.5 is

$$\left|A_s(f)|_{f \to 2/T_s}\right| = \frac{1}{2}|1.636 + j(-0.636)| = -1.1\text{dB}$$

When T&H place at the front end of ADC, however, the sinc distortion is not a concern since we only quantize the hold portion of a T&H output signal and the hold values are just the sampled points of input waveform we want to quantize them.

2.1.2 Quantization

The main functions of A/D conversion are sampling and quantization. While sampling result in a input signal to be discrete in time, it still continuous in amplitude. If we want to use a digital word with N-bit digits to represent the quantization result of a sampled signal,then

$$A_s(t) = A(nT_s)|_{n\in\mathbb{N}} = \lim_{N\to\infty} \sum_{i=1}^{N} D_i[n] \cdot 2^{-i} A_{ref}\,|_{n\in\mathbb{N}}$$

where n is an index variable, A_{ref} is an analog reference quantity which is used to represent the unit-less digital numbers in the physical domain and $D_i[n]$ is the i-th bit of output digital word. Eq2.6 reveal that only when the number of bits, N, approach infinity that eq2.6 satisfies. It is not physical allowable. For a limit number of bits, eq2.6

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is rewritten as

$$\mathrm{A_s}(t) \pm \mathrm{A_q}(t) = \sum_{i=1}^{\mathrm{N}} \mathrm{D}_i[n] \cdot 2^{-i} \mathrm{A}_{ref} \,|_{n \in \mathbb{N}}$$

where $\mathrm{A_q}(\mathrm{t})$ is the so-called quantization error. In order to produce acquirable finite number of bit, when quantizing a sampled signal, we allow some quantization errors.

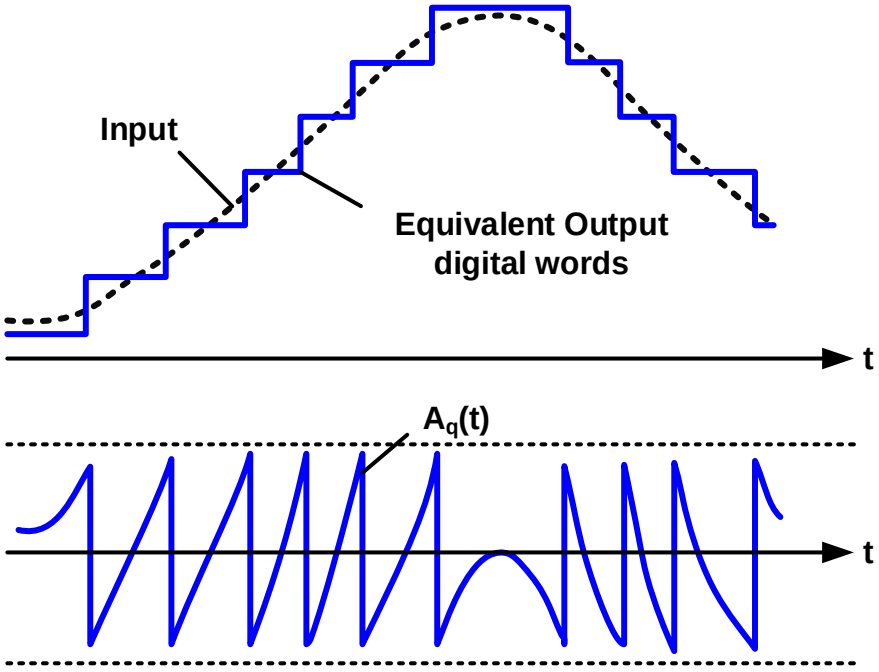

Fig. 2.4 (a) an analog input and its digital equivalent (b) quantization error of (a) result from A/D conversion

Fig2.7 shows a time-domain waveform example of quantization error. where $\mathrm{A_{LSB}}$ in fig2.7b is the least significant bit (LSB) which correspond for the smallest analog input change that cause output digital word change and it can be expressed as

$$\mathrm{A_{LSB}} = \frac{A_{\mathrm{ref}}}{2^N}$$

To analyze the impact on ADC performance due to quantization errors. When $\mathrm{N} \geq 6$, an approximation to calculate this impact can be made. Assuming $\mathrm{A_q}$ is a uniformly disturbed random variable range between$-\mathrm{A_{LSB}}/2 \leq A_q \leq +A_{LSB}/2$, then the average

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power result from A_q is

$$P_{q,avg} = \frac{1}{A_{LSB}} \int_{-A_{LSB}/2}^{+A_{LSB}/2} A_q^2 \, dA_q = \frac{A_{LSB}^2}{12}$$

Unlike commonly noise-induced powers that are caused from physical phenomenon, the power of quantization error comes from mathematical modelling.

2.2 Static Specifications

Static specifications, such as offset error, gain error, differential non-linearity and integral non-linearity provide information about how close an analog input signal is matched to the output digital word that it should ideally corresponds to. In fact, we use a time-varying dynamic signal, typical a sinusoid wave with very low frequency to measure those specifications. Since using analog input with near-DC like frequency to measuring these specifications, they are referred as static specification.

Static specifications can be present by using transfer function. A transfer function is a mathematical function, which theoretically models a device's output for each possible input. Fig 2.8 is the ideal transfer function of a 3-bit ADC

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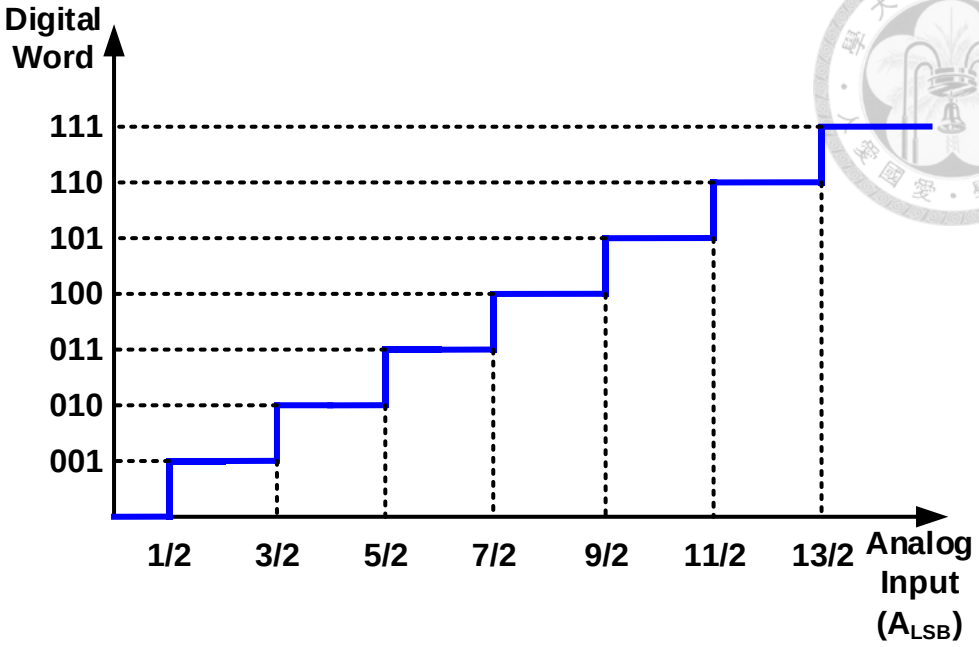

Fig. 2.5 Ideal transfer function of a 3-bit ADC

2.2.1 Offset Error

Offset error is the difference between the first measured transition point (lowest in voltage) and the first ideal transition point. Fig2.9 shows a TF example of an ADC with offset error (assume no other non-idealities)

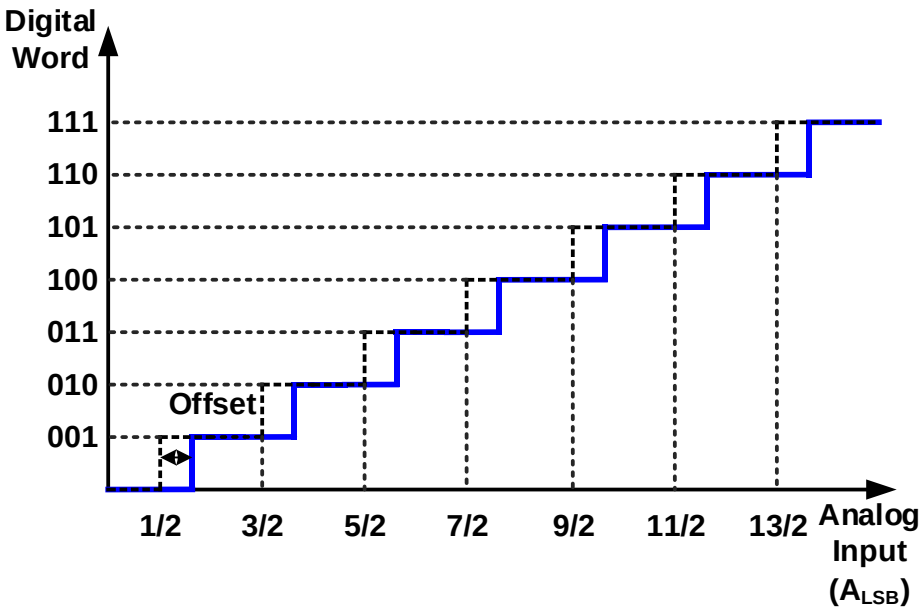

Fig. 2.6 Transfer function of a 3-bit ADC with offset error

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Offset error can also be expressed by equation

$$\text{Offset Error} = \frac{A_{0\to1}}{A_{LSB}} - \frac{1}{2}$$

where $A_{0\to1}$ is the analog input that cause output word change from 0 to 1.

2.2.2 Gain error

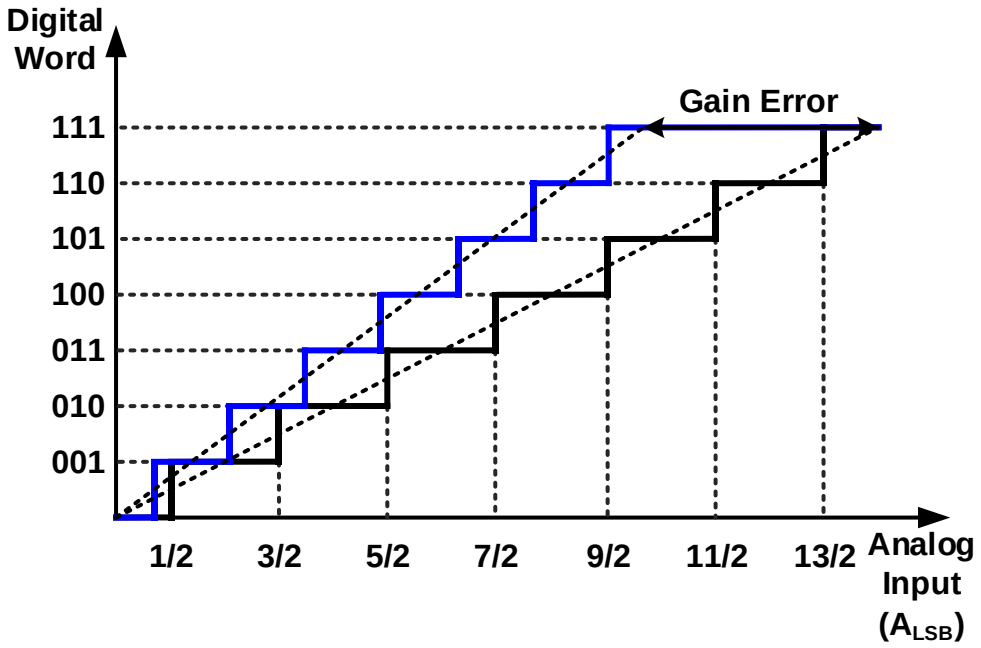

Fig. 2.7 Transfer function of a 3-bit ADC with gain error

Gain error is the difference between the ideal slope between zero and full-scale input and the actual slope between the measured zero point and full-scale input . Offset errors are zeroed out for this error calculation. Fig.2.10 shows a gain error example and eq.2.10 is the mathematical representation

$$\text{Gain Error} = \frac{A_{0\to1} - A_{2^N-2\to2^N-1}}{A_{LSB}} - (2^N - 2)$$

where $A_{2^N-2\to2^N-1}$ is the analog input that cause last output word transition.

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Previous discussions on offset error and gain error do not influence the linearity of over-all transfer function. A transfer function that is linearity can be expressed as $y(x) = ax + b$, where a and b correspond for gain and offset respectively. Gain and offset error can just be modeled into these two coefficients correspondingly and still satisfies the requirements of linearity. However, when the line of a transfer function bends like fig 2.8, following merits can be applied to measure how curable the line is.

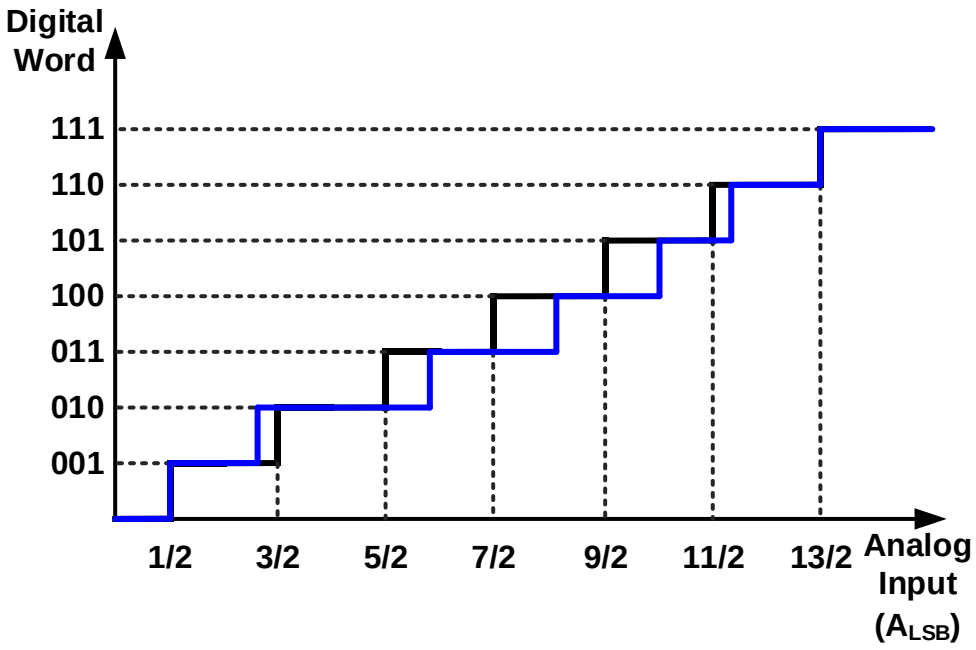

Fig. 2.8 Non-linearity of a 3-bit ADC

2.2.3 **Differential Non-linearity (DNL)**

Ideally, analog input in(de)crease one A_{LSB} will cause one digital output word transition, or we can say for every output code, it will represent an analog segments that ideally equals a A_{LSB}. The width of a segment is called a code width. When non-linearity exist in the A/D transfer function, code widths will derivate from one A_{LSB}. DNL is used to evaluate this deviation for every possible output code from its ideal code width

$$\mathrm{DNL}(i) = \frac{A_{i+1} - A_i}{A_{LSB}} - 1, 1 \le i \le 2^N - 2$$

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where N is the resolution, and A_i is the analog input that cause output code transition from . Fig2.11 shows the DNL plot of fig2.10 and it can be seen that the DNL of fig2.10 is between -0.4 and $+0.6$

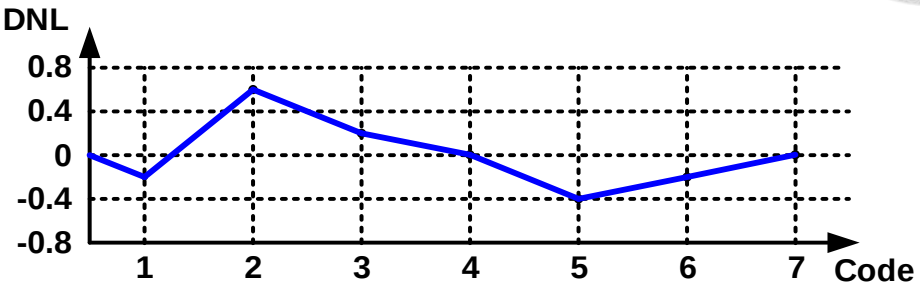

Fig. 2.9 Differential non-linearity of Fig. 2.8

A more intuitive definition of DNL is to define it to be the maximum absolute deviation of code widths from A_{LSB} among all possible output words.

$$\text{DNL} = \max_{1 \le i \le 2^N - 2} \left| \frac{A_{i+1} - A_i}{A_{LSB}} - 1 \right|$$

where N is the resolution of the ADC, A_i is the analog input value that cause output word transition from i to $i+1$. Above DNL definition make it become a single value instead of 2^N numbers. By adapting eq2.1, the DNL of fig2.10 is 0.6 rather than $0, -0.2, +0.6, +0.2, \ldots$ and the single value 0.6 tell us that the smallest width of analog input segment in fig2.11 is at least $\geq 0.4A_{LSB}$. The larger number of resolution,N, the more advantage of using eq2.12 to define the DNL.

2.2.4 Integral Non-linearity (INL)

The INL is the deviations of actual analog input values, which result in output word transition, from their corresponding ideal ones. In an ADC, A_i is the analog input that cause output code transit from i to $i+1$. If an ADC is ideal, then A_i will locate at ith A_{LSB} precisely. When non-linearity exist, it causes A_i drift from ith A_{LSB}. INL is used to calculate the drift of all A_i and be expressed as eq

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$$\mathrm{INL}(i) = \frac{A_i - (i - 0.5) \times A_{LSB}}{A_{LSB}}, 1 \le i \le 2^N - 1$$

Fig.212 shows the INL of fig2.09

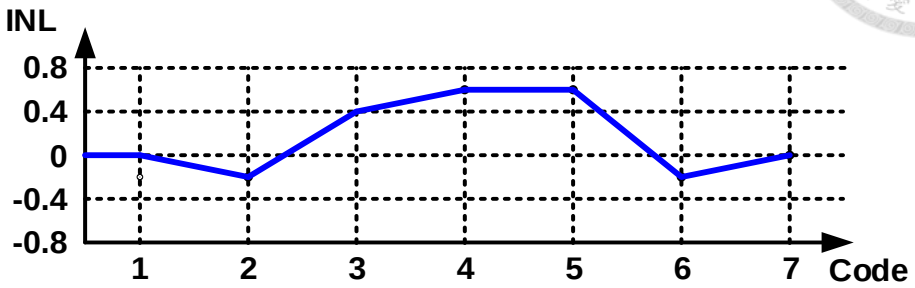

Fig. 2.10 Integral non-linearity of Fig. 2.8

Another perspective of INL is that the word 'Integral' of INL comes from the fact that INL(i) is the 'accumulation' of non-linearity errors from zero analog input to ith A_{LSB} input value. Since DNL(i) corresponds for i th non-linearity of i th A_{LSB} segment, for INL(i), we can sum up all the DNLs before ith A_{LSB} to represent INL(i).

$$\mathrm{INL(i)} = \sum_{j=0}^{i-1} \mathrm{DNL}(j),$$

In fact, the TF curve used in fig2.10 to demonstrate the INL has been calibrate the offset error and gain error. Calculation of the INL of an ADC based on calibrating out its offset error and gain error is a kind of end-point method because now the line decided by first and last analog values that cause output word transition are now match the ideal ADC transfer curve exactly. The INL definitions that obey the absolute requirements are important in measurement and industrial systems. For systems that offset and gain error are acceptable, best-fit method can be applied to calculate the INL. This method will result in minimized INL error. Fig2.14 shows the INL based on best-fit method

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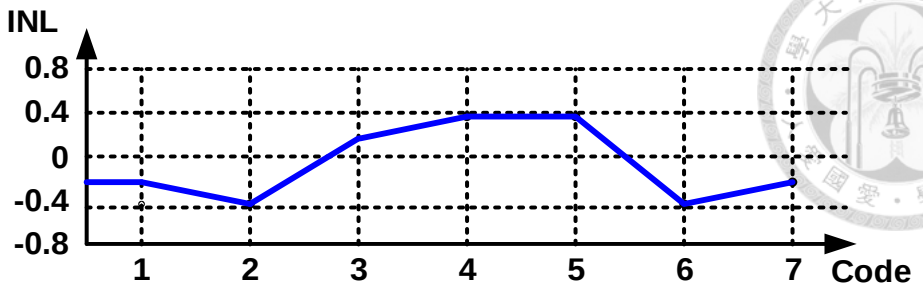

Fig. 2.11 Integral non-linearity of Fig. 2.8(best-fit method)

2.2.5 **Missing code**

When maximum DNL of an ADC equals 1, it means at least one possible output code is miss and will never appear at the output of the ADC. Fig2.12 shows an ADC transfer curve with missing code. In the figure, output word 101 is missed. For an ADC to have no missing code, it must guarantee to has maximum DNL less than 1 or if maximum INL$\leq$ 0.5.

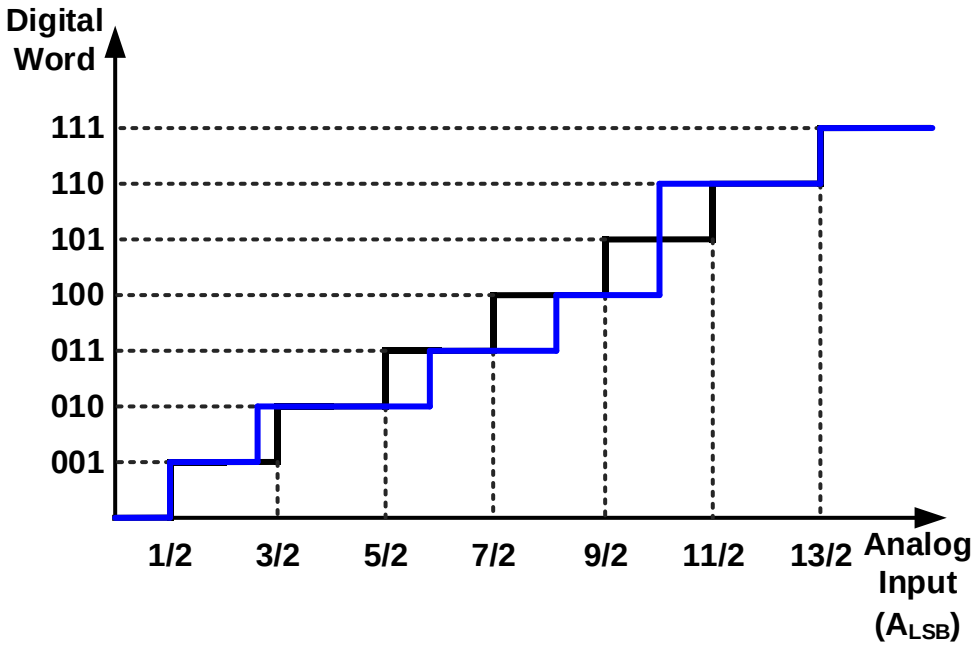

Fig. 2.12 Transfer function of a 3-bit ADC with missing code 101

2.2.6 **Non-monotonic**

An ADC is monotonic is that an increase (or decrease) in the analog input will always

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produce no change or an increase (or decrease) in digital code. Fig 2.13 shows an ADC with non-monotonic in its transfer function. In digital control system, non-monotonic in ADC will cause serve problem and must be strictly forbidden.

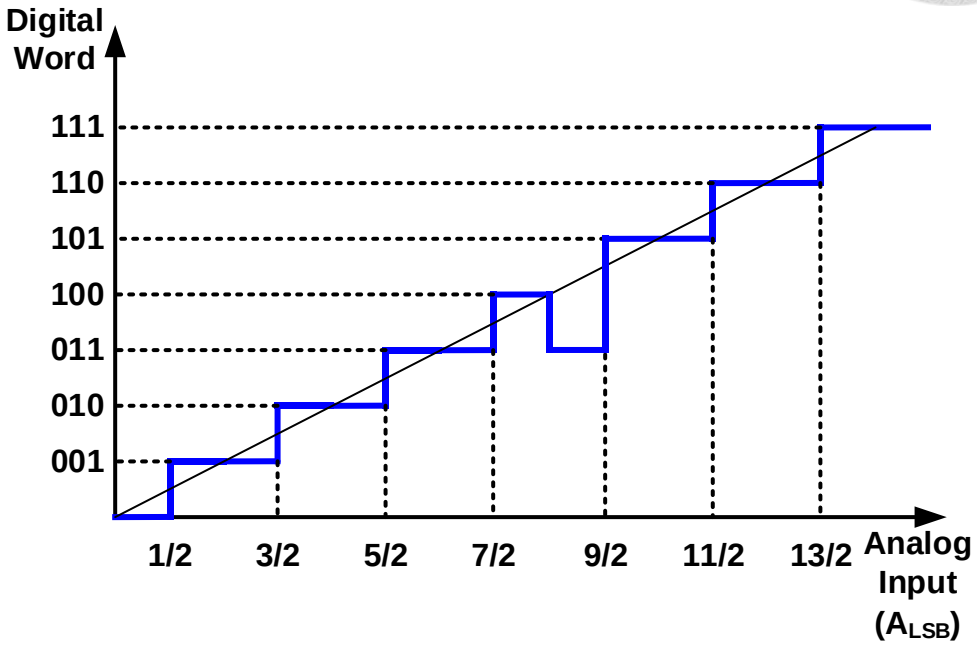

Fig. 2.13 Non-monotonic transfer function of a 3-bit ADC

2.3 Dynamic specifications

Dynamic specifications include signal-to-noise ratio (SNR), total harmonic distortion (THD), signal-to-noise and distortion ratio (SNDR), Spurious-Free Dynamic Range (SFDR), effective resolution (ER), effective number-of-bits (ENOB) and effective resolution bandwidth (ERBW). Unlike static specifications, which tell if the conversion result is accurate, dynamic specifications tell how us repeatable the conversion result is. Conversion result that is repeatable means for a deterministic input like a single-tone sinusoid wave, one can always observe at the output bits of an ADC that output patterns of some bits, typical the patterns of most-significant bits (MSBs), are repeating, while the reminding bits, typical the least-significant bits(LSBs), are random dithering.

When measuring ADC dynamic performance, we apply a sinusoid wave input with

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full-scale in amplitude and frequency in interested, collect lots of output digital word that are equivalent to the input wave. Those output words then send to the function of Fast-Fourier Transform (FFT) to shows them with their frequency spectrums. Fig 2.14 shows an FFT example of ADC output digital words

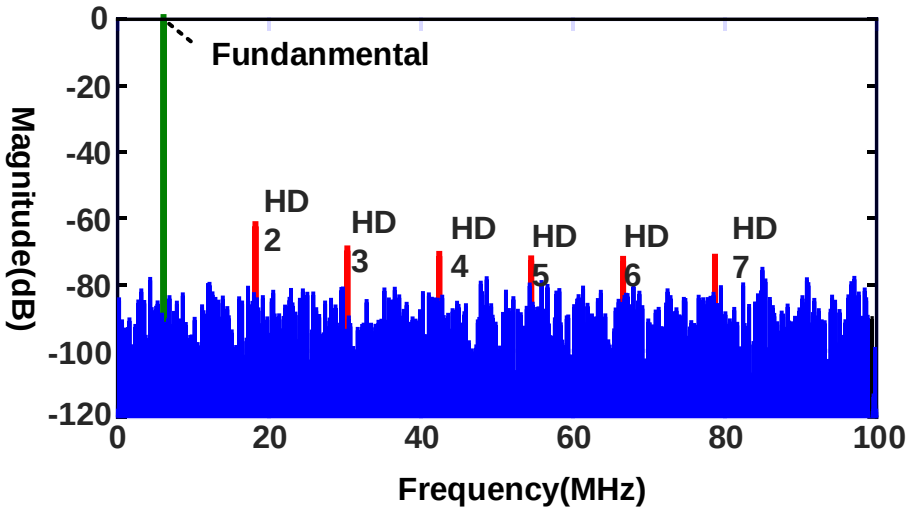

Fig. 2.14 A typical frequency spectrum of ADCs output result shows (a) fundamental (green) (b) harmonic distortion (HD) (red),and (c) other noise (blue) components

Since non-linearity and electronic noise co-exist in a real ADC, it can be seen in fig2.14 that now the output of an ADC contains not only the desired (green) but the unwanted(red and blue) frequency components. We will use the magnitudes of output spectrums to evaluate the dynamic specifications of ADCs.

2.3.1 Signal-to-noise ratio (SNR)

Signal-to-noise ratios of ADCs represent the input signal power over the power of noises like fig2.14(c). Typically given in dB, the expression for SNR is

$$\mathrm{SNR(dB)} = 10\log\frac{signal\ \ power}{noise\ \ power}$$

Assume that the input signal is a sinewave with a peak-to-peak value equal to the full-scale reference voltage,A_{ref}, of the converter and then the signal power is

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$$\text{signal power} = \frac{1}{1/f_{sig.}} \int_{t=0}^{t=1/f_{sig}} \mathrm{A}_{ref} \cdot \sin^2(2\pi f_{sig.} t) dt = \frac{A_{ref}^2}{8}$$

A_{ref} can be expressed in terms of A_{LSB} and the signal power of exxx becomes

$$\text{signal power} = \frac{2^{2N} A_{LSB}^2}{8}$$

recall from section 2.1.2 that quantization error is the fundamental error even in an ideal ADC, then the power of quantization error set the SNR limitation of a N-bit ADC. We write down the SNR here

$$\mathrm{SNR}_{ideal} = 10 \log \frac{\frac{2^{2N} A_{LSB}^2}{8}}{\frac{A_{LSB}^2}{12}} = 1.76 + \mathrm{N} \times 6.02$$

For a 10-bit ideal ADC, its ideal SNR is $1.76 + 10 \times 6.02 = 61.96$ dB and this value set the dynamic performance limitation of 10-bit ADC since no other noise sources and non-linearity induced errors take into consideration.

2.3.2 Total harmonic distortion (THD),

Harmonic distortion is the un-wanted signal tones like those marked in green in the Fig. 2.14. Unlike noise, which usually refer to electronic noises that result from random motions of electronics in materials, harmonic distortions are derived from non-linear transfer function of circuits and are depend on input signal tone. THD can be expressed of the rms sum of the powers of the harmonic components (spurs) ratioed to the input signal power

$$\mathrm{THD} = 10 \log \left(\frac{Powers\ \ of\ \ second\ \ and\ \ higher\ \ harmonics}{signal\ \ power} \right) \qquad (2.1)$$

2.3.3 Effective number-of-bits (ENOB)

Effective number of bits (ENOB) based on the SNDR is a measure of the dynamic performance of an ADC and its associated circuitry. The units of measure for SNDR is

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dB and the units of measure for ENOBs is bits. One can change SNDR into ENOB with the following

$$\text{ENOB} = \frac{SNDR - 1.76}{6.02} \tag{2.2}$$

2.3.4 Signal-to-noise and distortion ratio (SNDR)

The SNDR is calculated by combining of SNR and total harmonic distortion (THD). SNDR is the ratio of the RMS amplitude of the fundamental input frequency of the input signal to the RMS sum of all other spectral components below one half of the sampling frequency (excluding DC). The definition of the SNDR can be expressed as:

$$\text{SNDR} = 10\log\left(\frac{signal\ \ power}{power\ \ of\ \ all\ \ unwanted\ \ componets}\right) \tag{2.3}$$

2.3.5 Spurious-free dynamic range (SFDR)

Spurious free dynamic range (SFDR) is the ratio of fundamental signal to the largest spurious signal in the output. The definition of the SFDR can be expressed as:

$$\text{SFDR} = 10\log\left(\frac{signal\ \ power}{Largest\ \ Spurious\ \ Power}\right) \tag{2.4}$$

2.3.6 Effective resolution (ER)

ER is measured by collecting a statistical sample of many conversions with a clean, “noiseless” DC in signal. The units of measure for ER are bits

2.3.7 Effective resolution bandwidth (ERBW)

Effective resolution bandwidth is the frequency bandwidth where SNDR is guaranteed not to degrade more than 3dB

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Chapter 3 High-Speed Design Considerations of Single-Channel SAR ADC

3.1 Introduction

As mentions in the motivation section of chapter 1, trends for achieve highest ADC speed are using time-interleaving technique, and TI-SAR ADC has replaced the FLASH type ADCs. Time interleaving is an ADC timing allocation technique by using multiplexing and de-multiplexing. It distribute the already tense clock time equally to several ADCs to release the even more tighten timing requirements of single ADC for the same speed specification. For instance, Fig. 3.1 shows a 4-channel time-interleaved ADC. Assume this ADC target for 1GS/s and 10-bit resolution, if we use single channel SAR ADC that its internal operation frequency need more than 10GHz that still hard realize in today's technology. But with time-interleaving assistant, now the 1GS/s target can multiplex to this ADC, every channel operate at 250MS/s and its internal operation only need 2.5GHz clock frequency, which is commonly seen in today's clock source.

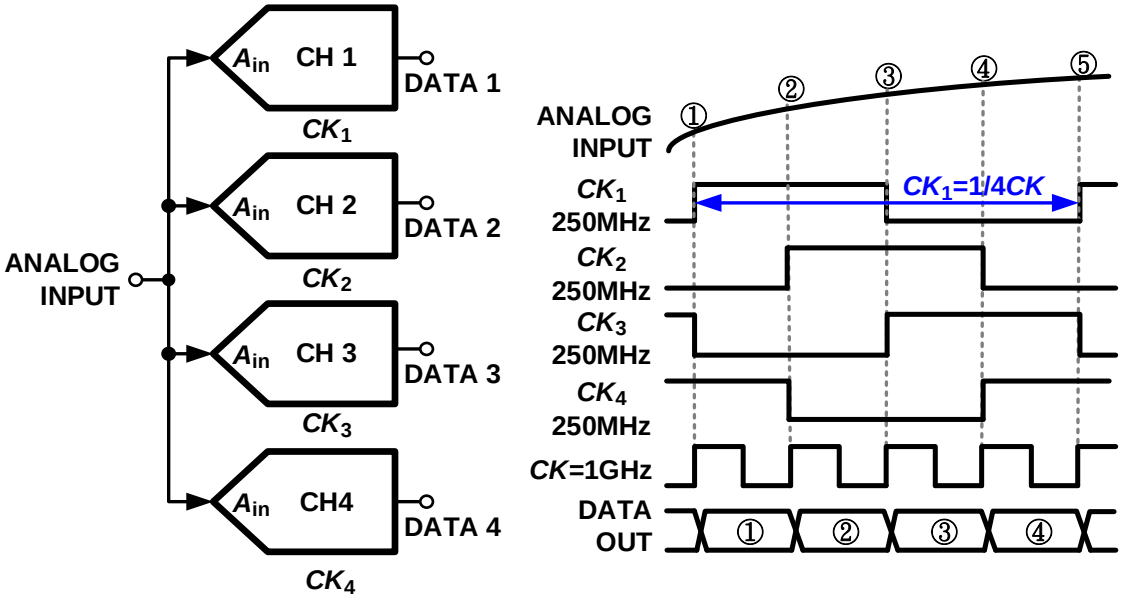

Fig. 3.1 A 4-channel time-interleaved ADC operate at 1GS/s.

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Although time-interleaved technique applied to all kinds of ADC, when it comes to consider physical design, area occupation becomes a serious problem because now a N-channel time-interleaved ADC will at least N times larger area than single-channel ones with same type ADC. The straightest way to reduce ADC area in silicon realization is by using advanced process technology to implement the physical design. Since SAR ADC is less complexity in architecture and survival well in advanced process nodes. Time-interleaved SAR (TI-SAR) ADCs are commonly adapted for high-speed application. Table 1 shows some most recent high-speed application using TI-SAR ADC published in top journal and conferences.

Publication	JSSC'19[33]	JSSC'18[34]	ISSCC'19[35]	VLSI'18[36]
Technology	28nm CMOS	14nm FinFET	7nm FinFET	16nm FinFET
Architecture	TI-SAR	TI-SAR	TI-SAR	TI-SAR
Sample-rate	56GS/s	72GS/s	28GS/s	56GS/s
Resolution	8bit	8bit	8bit	8bit

Table 1 Trends for ADC selection in high-speed application

Two ways to further increase speed of TI-SAR ADC are using more channels and keep speed up single-channel SAR ADC. Reminder sections of this chapter will focus on speed-up single-channel SAR ADC. Section 3.1 analyze a single-channel SAR ADC by finding its speed limitations. Sec.3.2 introduce three technique that reduce waste time when allocate timings to control the SAR ADC. Section3.2 will describe how to use latch logic to implement the SAR operation. Section3.3 examine two search algorithms that allow DAC settling error or comparator decision error.

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3.2 Operations of SAR ADC

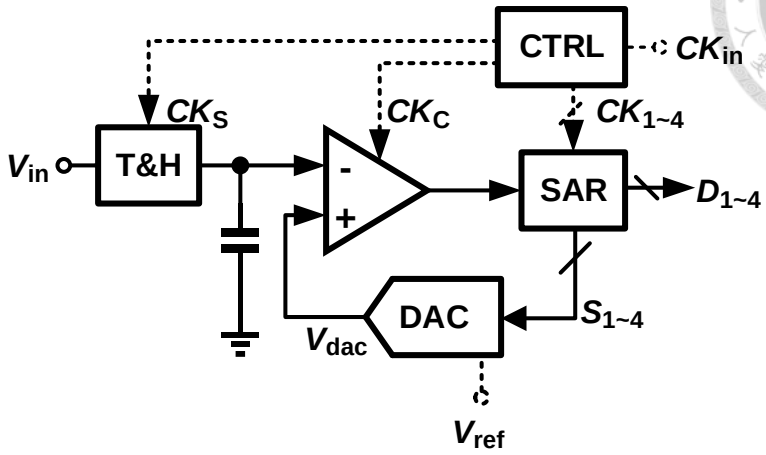

Fig. 3.2 General architecture of SAR ADC

Fig. 3.2 shows a general architecture of SAR ADC that implement the binary search algorithm as mentioned in xxxx. Building blocks of this architecture include a track-and-hold (T&H), a digital-to-analog converter (DAC), a comparator, a SAR logic and a control logic. The control logic sequentially determines each bit according to the output of the comparator. To learn more about the sequential operation of SAR ADC, consider the timing diagram, which is shown in Fig. 3.3.

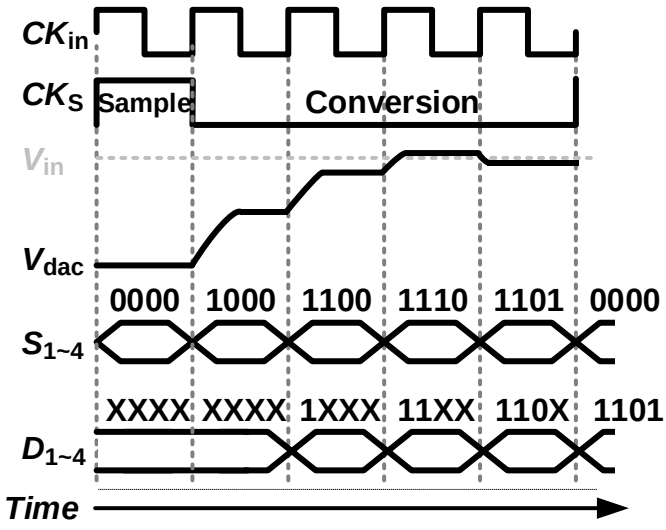

Fig. 3.3 Timing diagram of a 4-bit SAR ADC

After sampling, the SAR ADC enters the conversion mode. The control logic first

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assumes that the MSB bit is 1 and the remaining bits are 0, and then sends this guess to the DAC to generate $0.5V_{ref}$. The comparator then compares the sampled signal with the output of the DAC. If the result is that the sampled signal is greater than $0.5V_{ref}$, then the MSB bit is set to 1 or the MSB bit is set to 0. This completes the first step of the sequential operation. The guess of the second step will refer to the result of the first step. If the MSB bit is 1, then the guess is 1100 and sent it to the DAC to generate $0.75V_{ref}$; if the MSB bit is 0, then the guess is 0100, so the DAC generates $0.25V_{ref}$. Then the comparator compares the DAC output with the sampled signal for a second time, and determines the second bit to be 1 or 0 according to the comparison result. This completes the second step of the sequential operation. The remaining steps will follow the result of the previous steps until solving the LSB bit.

To analyze the speed of the SAR ADC, we will examine a SAR ADC with charge redistribution DAC as shown in Fig. 3.4.

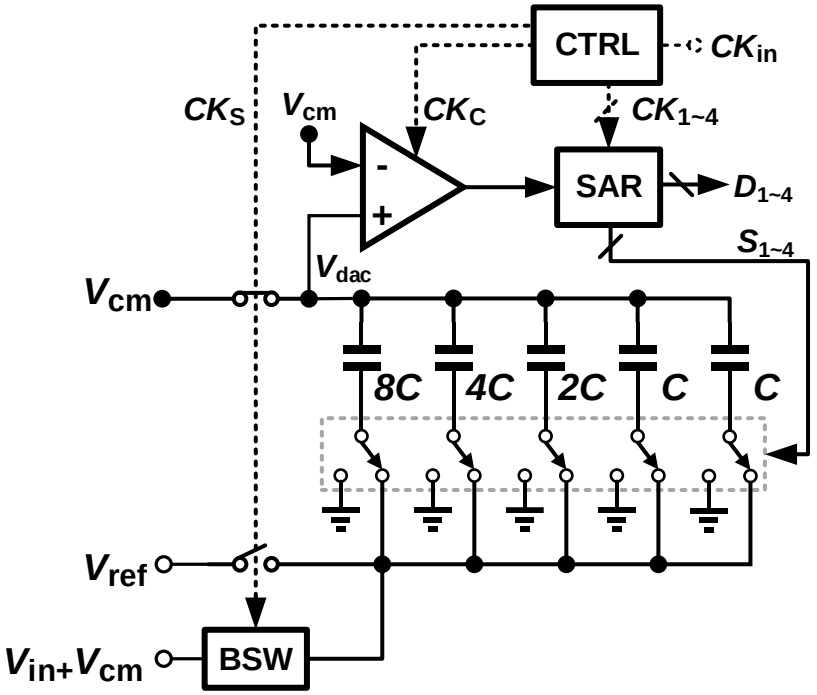

Fig. 3.4 A 4-bit example of charge-redistribution SAR ADC

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This SAR ADC uses a capacitive-DAC (CDAC) and incorporates a sampling switch into the CDAC. The benefit of this architecture is that it saves area and allows for differential input of SAR ADCs. The operations of a charge-redistribution SAR ADC is similar to those in Fig. 3.3. However, now the CDAC combine both storing input charge and providing comparator reference voltage as shown in Fig. 3.5. During the sampling phase, the capacitor array of the CDAC samples the input by connecting input to the bottom-plates of the array. At the same time, a common-mode voltage, V_{cm}, is connected to the top-plates of the array.

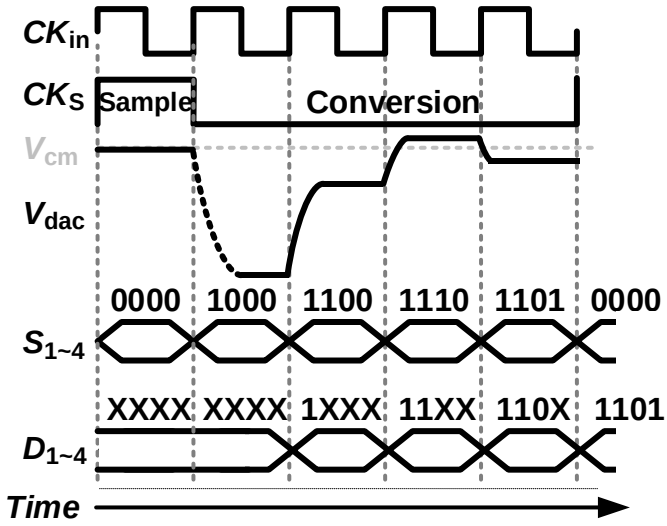

Fig. 3.5 Timing diagram of a 4-bit charge-redistribution SAR ADC-

3.3 Settling time of capacitive-DAC

To estimate CDAC settling time, we first modeling the dynamic behavior at the output of the CDAC due to input switching, and then we use this switch-induced output behavior to calculate the CDAC settling time requirement at different cycles for a charge-redistribution SAR ADC. A slice of CDAC structure is depict in Fig. 3.6.

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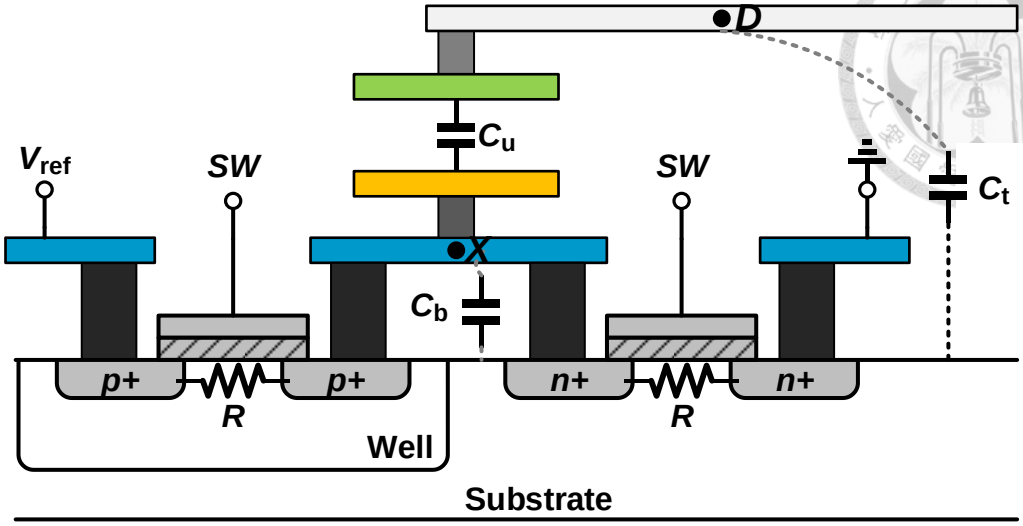

Fig. 3.6 A unit-capacitor structure used to model the CDAC settling time

This structure include three capacitors,C_u, $C_b$and C_t. C_u is a unit-capacitor that will be used to interact with other unit-capacitors to perform the charge redistribution function. C_b represent the total parasitic capacitance at the bottom-plate of C_u. C_t account for total parasitic capacitance at the top-plate of C_u. Resistors drawn in Fig. 3.6 represent the turn-on resistance of the MOS switch and all the other series resistance from bottom-plate of C_u.

Combine all the information mentioned in this paragraph, a circuit model could be derived as below figure and a N-bit CDAC model can be constructed by it

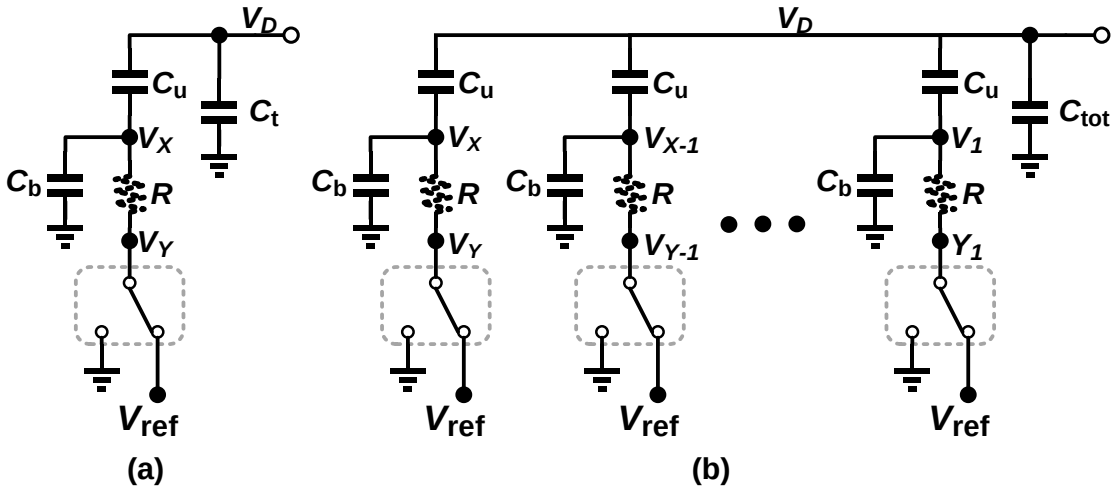

Fig. 3.7 (a) Circuit model of Fig. 3.6 and (b) $2^N$of (a) construct a N-bit CDAC

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Using the circuit model of Fig. 3.7b, we apply KCL at V_D yield (3.1), where C_{tot} is the total top-plate parasitic capacitance of all unit-capacitor, V_X is the node voltage at X-th unit-capacitor

$$\sum_{X=1}^{2^N} C_u (V_D' - V_X') = -C_{tot} V_D' \tag{3.1}$$

Substitute $C_{tot} = 2^N \cdot \alpha_t \cdot C_u$ and rearrange (3.1), we get V_X' where α_t is the fractional top-plate parasitic capacitance of a unit-capacitor

$$\sum_{X=1}^{2^N} V_X' = 2^N (1 + \alpha_t) V_D' \tag{3.2}$$

Integrate both sides of (3.2) yield (3.3), where b_0 is the constant of integration

$$\sum_{X=1}^{2^N} V_X = 2^N (1 + \alpha_t) V_D + b_0 \tag{3.3}$$

Until now, we have derived two equality equations (3.2) and (3.3) of a N-bit CDAC between its output voltage at top-plate and all the node voltages at its bottom-plates.

To find a transient relationship between node V_x and V_D, we also apply KCL to Fig. 3.7a and write down

$$C_u (V_D' - V_X') = C_b V_X' + \frac{V_X - V_Y}{R} \tag{3.4}$$

where V_Y is a binary constant, either 0 or V_{ref} depend on switching. In order to substitute V_X and V_X' in (3.4), we extend the equality of (3.4) to all 2^N unit-capacitors and sum up all the equalities. Beside, replace C_b with $\alpha_b C_u$, where α_b is the fractional bottom-plate parasitic capacitance of a unit-capacitor

$$\sum_{X=1}^{2^N} C_u (V_D' - V_X') = \sum_{X=1}^{2^N} \alpha_b C_u V_X' + \sum_{X=Y=1}^{2^N} \frac{V_X - V_Y}{R} \tag{3.5}$$

Rearrange and simply (3.5)

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$$V_D' = \frac{1}{2^N}\left[(1+\alpha_b)\sum_{X=1}^{2^N} V_X' + \frac{1}{RC_u}\sum_{X=1}^{2^N} V_X - \frac{1}{RC_u}\sum_{Y=1}^{2^N} V_Y\right] \quad (3.6)$$

Now substitute (3.2) and (3.3) into (3.6). After some reductions and rearrangements

$$\tau V_D' + V_D = \frac{1}{2^N(1+\alpha_t)}\sum_{Y=1}^{2^N} V_Y \quad (3.7)$$

$$\tau = RC_u\left(\alpha_b + \frac{\alpha_t}{1+\alpha_t}\right) \quad (3.8)$$

(3.7) is a first-order differential equation that describe the dynamic behavior of the output voltage of the N-bit CDAC under given switching pattern and (3.8) is the time constant of the CDAC. In a charge-redistribution SAR ADC, the SAR logic will control the CDAC like Fig. 3.7b switching from one input pattern to another one depend on previous output result of the comparator. Assume the SAR logic switches M unit-capacitors, then the forced response of the CDAC is

$$V_{D,forced} = \frac{M}{2^N(1+\alpha_t)}\left(1-e^{-t/\tau}\right) \pm V_{ref} \quad (3.9)$$

where $\pm V_{ref}$ means those M unit-capacitors may switching from ground to V_{ref} or V_{ref} to ground and τ is the time constant as (3.8)

Parasitic capacitance at the bottom- and top-plate unit-capacitor will affect the transient response since they are weighting factors of the time constant as shown in (3.8). Rewriting (3.8) in two terms form gives more clear insights.

$$\tau = RC_u\alpha_b + RC_u\frac{\alpha_t}{1+\alpha_t} \quad (3.10)$$

First term in the right hand side of (3.10) tells that the bottom-plate parasitic capacitance α_b adjust RC_u proportionally. A large α_b ($\geq$ unity) times RC_u and may therefore underestimate CDAC settling time if estimating α_b loosely. The second term specifies the time constant adjust by top-plate parasitic capacitance α_t. For large α_t, $\frac{\alpha_t}{1+\alpha_t}$

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approach unity and the second term simply to RC_u. From these two terms, it concludes that in order to reduce CDAC settling time, not only the RC_u time constant but also the bottom-plate parasitic capacitance should take into consideration when designing CDAC, at least first approaching.

Next, we use (3.9) to analyze the settling time requirement of CDAC at different step of a charge-redistribution SAR. Strictly speaking, only provide every step infinite time for settling that them can reach their steady state, no matter switching 2^{N-1} or 1 unit-capacitor at MSB or LSB step. Since it is impossible to allocate an infinite or a very long time at every step for output voltage settling to steady state, there always exists a settling error at every step. A reasonable settling error at *i*-th step, which is labeled as ε_D here, is absolute less than $0.5A_{LSB}$ [32].

$$\varepsilon_{D,i} = \left|V_{\mathrm{D,forced}}(\infty) - V_{\mathrm{D,forced}}(\Delta_{t,i})\right| \leq \frac{A_{\mathrm{ref}}}{2^{N+1}(1+\alpha_t)} \tag{3.11}$$

where $\Delta_{t,i}$ is the settling time at *i*-th step, A_{ref} is the analog reference quantity, N is the resolution and α_t is the top-plate parasitic capacitance. Substitute (3.9) into (3.11) and after some simplification, we arrive the *i*-th CDAC settling time requirement of a charge-redistribution SAR ADC

$$\Delta_{t,i} = \tau \ln 2 + \tau \ln M \tag{3.12}$$

For the binary-weighted CDAC, 2^{N-1} unit-capacitors are switched in the first step, 2^{N-2} unit-capacitors are switched in the second step and so on for the next steps. The following table shows the settling time required for a 10-bit charge redistribution SAR ADC with binary-weighted CDAC.

No. of *i*-th step	1	2	3	4	5	6	7	8	9	10
Settling time($\tau \ln 2$)	10	9	8	7	6	5	4	3	2	1

Table 2 Settling time for each step of a 10-bit charge-redistribution SAR ADC

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A SAR ADC with synchronous control, each step is assigned the same time. The time must at least satisfies the worst-case settling time. For an N-bit charge-redistribution SAR this time equals

$$\text{time assigned for each step for DAC settling} \geq N \cdot \tau \ln 2 \quad (3.13)$$

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Chapter 4 A 10-Bit 200-MS/s SAR ADC

4.1 Introduction

In the previous chapter, we introduced the operations of a SAR ADC. In order to achieve high-speed, the bottlenecks in allocation of time for each operation step of a SAR ADC have been analyzed. The worst-case comparator comparison time, T_c, and the worst-case CDAC settling time, T_{dac}, are derived. It also introduces how to use asynchronous control and redundancy algorithms to reduce T_c and T_{dac}, respectively. Furthermore, the SAR logic delay depending on the design complexity can also be greatly reduced by using latch logic to implement. It seems that the main bottlenecks that limit the speed of the SAR ADC have been identified and resolved. However, those solutions can still be optimized. First, as shown in Fig. 4.1, it notices that even a SAR ADC with asynchronous control can make the Tc self-adapting; the Tdac of each step is still equals worst-case one.

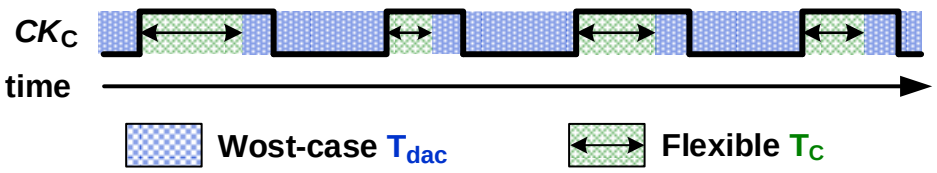

Fig. 4.1 Illustration of speed limitation of an asynchronous control

In order to trace the cause that result in tdac can only be a fixed time and this time equals worst-case settling time, we should analyze the architecture of asynchronous control. A conventional architecture of asynchronous control is like that shown in Fig. 4.2.

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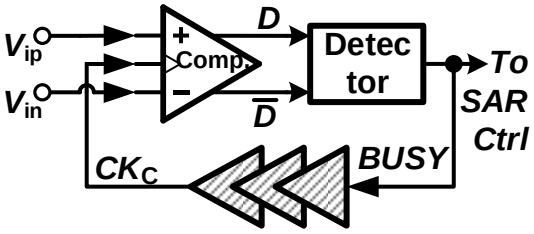

Fig. 4.2 A conventional architecture of asynchronous control

At each conversion step, CK_C first transits from logic LOW to logic HIGH to indicate that the comparator begins to compare the inputs. After a period time of comparison, D and DB are transformed from same logic LOW state to LOW/HIGH or HIGH/LOW state to conclude the end of comparison of this conversion step. After comparison, there are two main mechanisms start to operate. One is the comparison result will send to the SAR logic to switch the corresponding capacitor of that step, the other mechanism is to reset comparator to clear it output to prepare for the next step. By using an asynchronous control, a detector is insert between SAR controller and comparator outputs. This detector is used to indicate that where there is a comparison result at comparator's outputs. A BUSY signal is generated not only to trigger the SAR controller to execute the SAR logic but also means the outputs of comparator are occupied with data therefore need to be cleared.

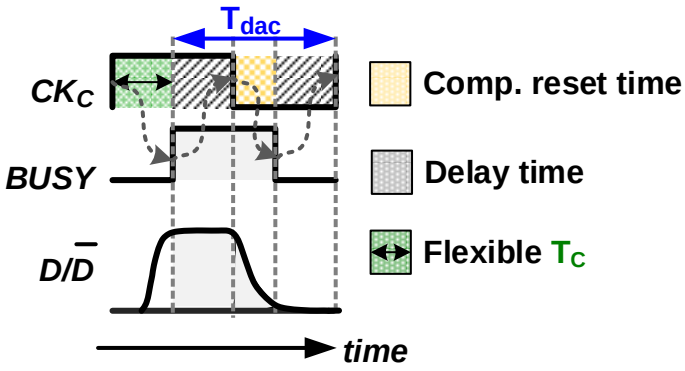

Fig. 4.3 Timing diagram of asynchronous control

Notice that there is a buffer chain placed between the BUSY and CK_C signal node.

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This placement is to ensure that T_{dac} can meet the settling time requirement of MSB capacitor switching. From the previous section, we know that the settling time required for each step decrease as the switching capacitance becomes smaller. However, the delay added to the asynchronous control does not decrease as the switching capacitance becomes smaller. That is to say, even if the capacitance switching of the latter steps has reached the target requirements, the comparator still has to wait for a while before starting the comparison of the next step. The idle time of the DAC and the comparator inevitably becomes a wasting. Fig. 4.4 depicts the inevitable increase in waste time as step increases.

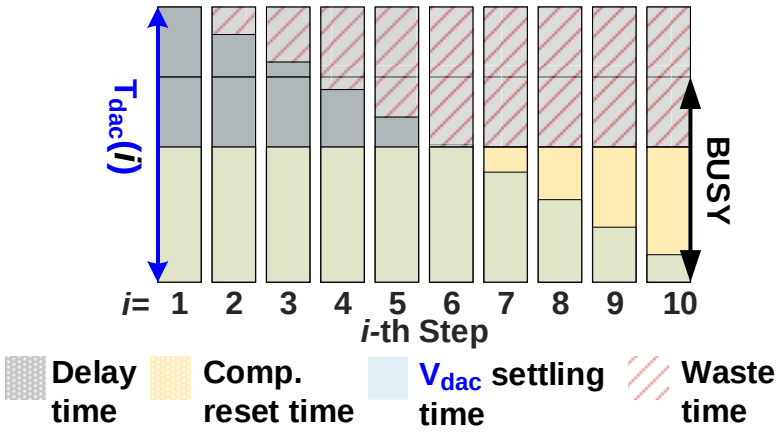

Fig. 4.4 Timing allocations of conventional asynchronous control

Unfortunately, in the LSB steps, even the redundant algorithm is used to reduce T_{dac} and therefore reduce added delay time; the comparator reset time is longer than the requirements of DAC settling time. In other words, in LSB steps, adding delay is not needed at all! The following figure emphasizes that, even if the added delay is reduced, there is still a waste of time in the LSB steps.

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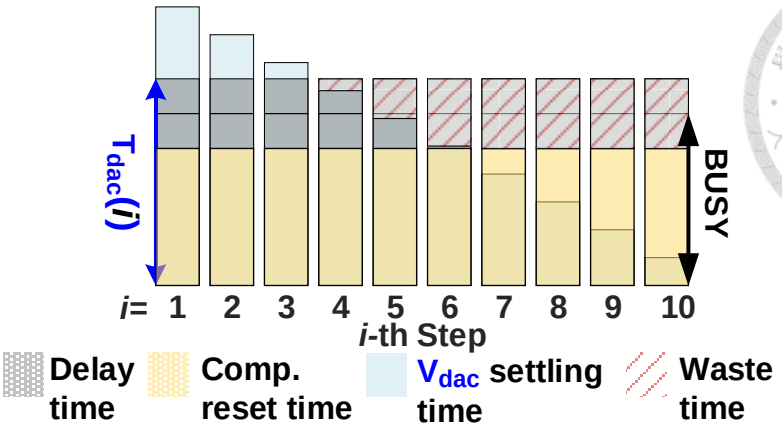


Fig. 4.5 Waste time still exist even with redundancy

4.2 Proposed dual-loop asynchronous control

Traditional asynchronous control adds delay to ensure enough time for DAC settling, but the delay placed at the loop that controls the comparator. So not only the requirement of DAC settling time is guaranteed by adding delay but also the BUSY time(the time that comparison result is valid at comparator's outputs) is extend a delay time because now the CK_C has to wait a delay then can be pull down to reset the comparator.

Concept of dual-loop asynchronous control is to split a single loop that responding for both DAC settling and comparator reset to two loops, one for guaranteeing DAC settling and the other provide path for comparator reset. Fig. 4.6 illustrates this concept.

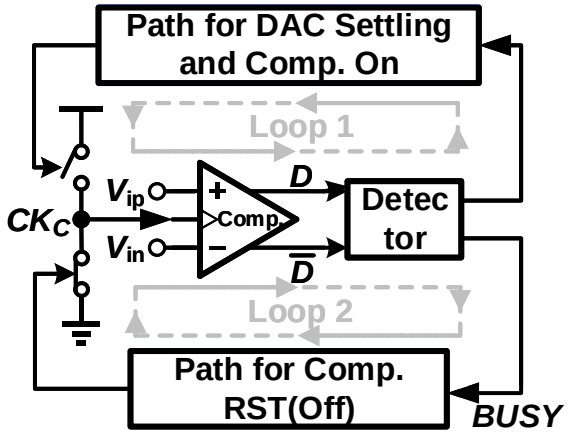


Fig. 4.6 Concept of dual-loop asynchronous control, it split on/off path of comparators

doi:10.6342/NTU201902051

With dual-loop asynchronous control, the buffer chain no longer delays the resetting of the comparator. From now on, resetting the comparator (BUSY=1 to 0) for preparing next comparison and adding delay to ensure DAC settling can be controlled separately. Fig. 4.7 shows the timing allocations for the dual-loop.

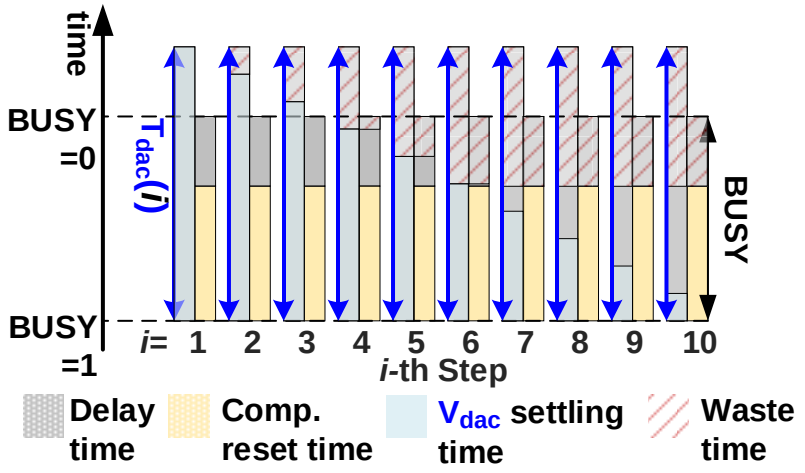


Fig. 4.7 Timing allocations of dual-loop asynchronous control

Several works have published to realize the concept of dual-loop asynchronous control and try to gain all the benefit from the separate timing allocations. A work from [23] proposed two techniques, which called “Fast Comparator Auto-reset” and “Successive Acceleration Mechanism”. The first one tries to provide short delay path to shorten the delay from BUSY signal on to CKC signal off, therefore speed-up clearing the comparison results at outputs of comparator to get ready for the next step. The second one reduce the added delay for DAC settling successively from MSB steps to LSB steps. If we apply this two techniques to a 10-bit dual-loop asynchronous SAR ADC, then the timing allocation will look like that shows in Fig. 4.8.

doi:10.6342/NTU201902051

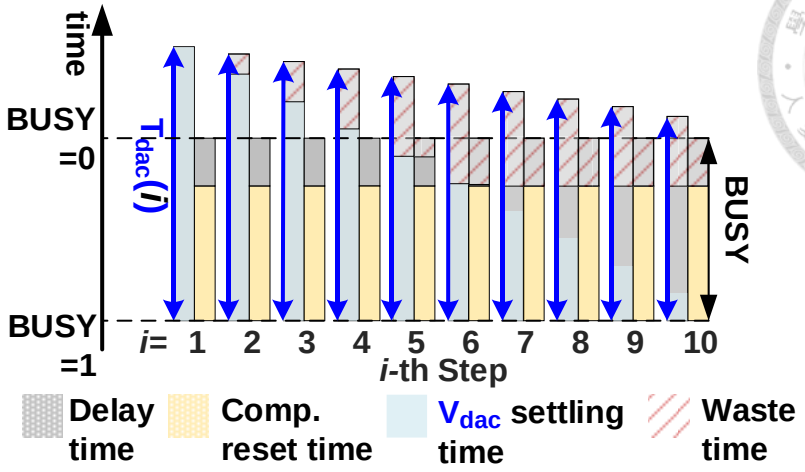


Fig. 4.8 Timing allocations of dual-loop asynchronous control with techniques from

The technique of gradually reducing the delay time of each step proposed by [23] is not designed by an adapting manner. That is, the amount of reduced time will suffer from process variations. A process insensitive delay time reduction is presented in [11]. The reduction time not estimate by simulation, on the contrary, it extend the concept of self-timing control for comparator to a self-timed DAC. When the corresponding capacitors of each step are switched and settles, an indicator will trig the comparator to do next comparison. However, as shown in Fig. 4.9, waste time exist because in LSB steps the self-timed DAC has to wait until the BUSY signal comes back to 0.

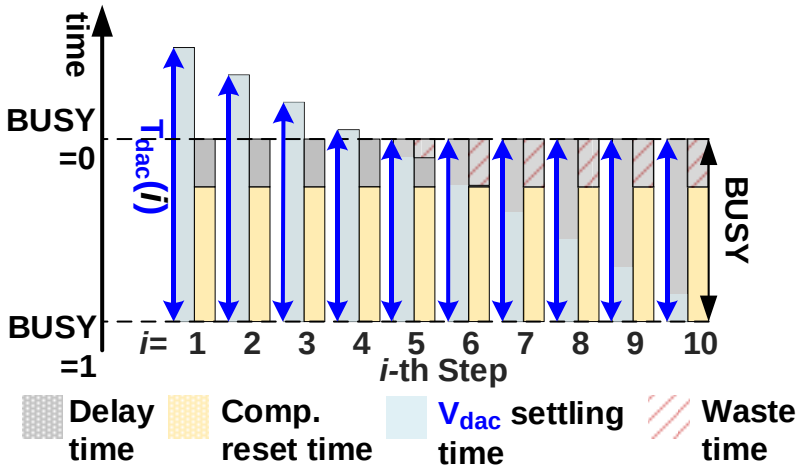


Fig. 4.9 Timing allocations of process insensitive dual-loop asynchronous control

doi:10.6342/NTU201902051

The goal for the proposed dual-loop asynchronous control aimed at shortest comparator BUSY time and therefore further reduce the waste time.

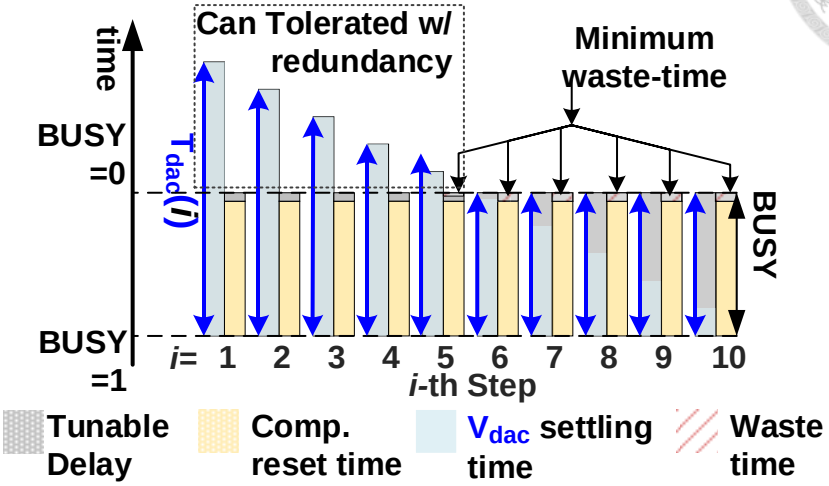


Fig. 4.10 Goal of the proposed dual-loop asynchronous control

Fig. 4.11 shows the circuit design of the proposed dual-loop asynchronous control. The proposed dual-loop simple contains a NAND gate, a tunable delay line, a negative pulse generator and two switches. The proposed dual-loop offer the shortest BUSY to CKC delay path because now the BUSY signal DIRECTLY turn on the reset switch, SW_N to reset CKC.

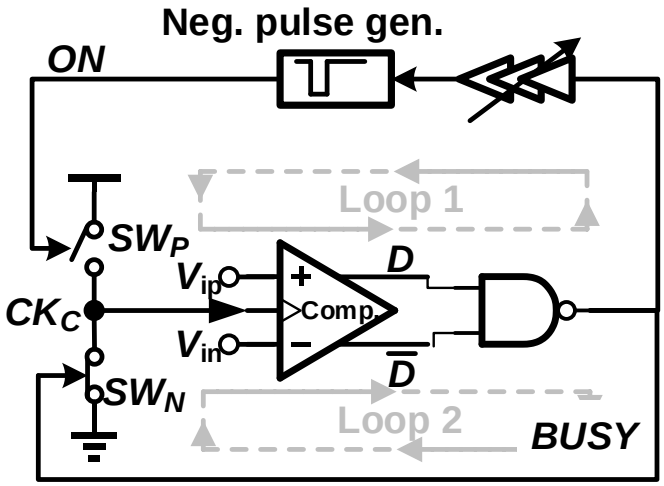


Fig. 4.11 Proposed dual-loop asynchronous control

doi:10.6342/NTU201902051

4.3 Architecture of the proposed SAR ADC

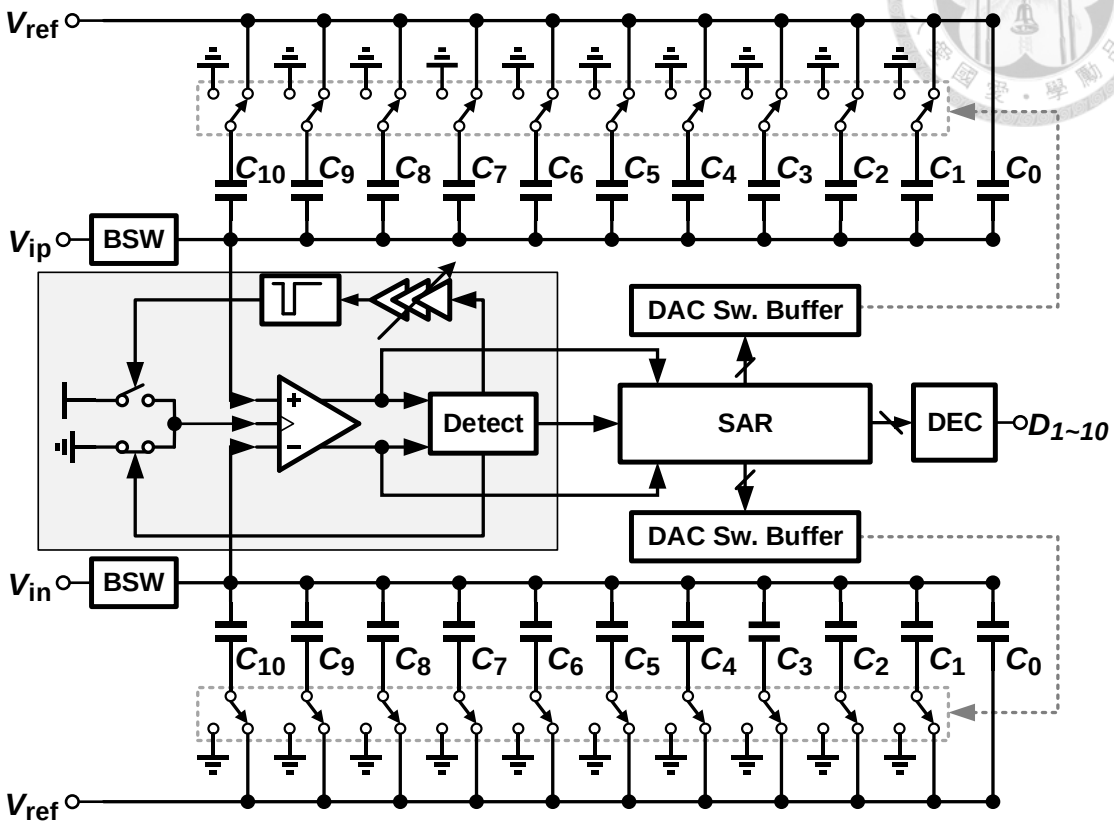


Fig. 4.12 Architecture of proposed SAR ADC

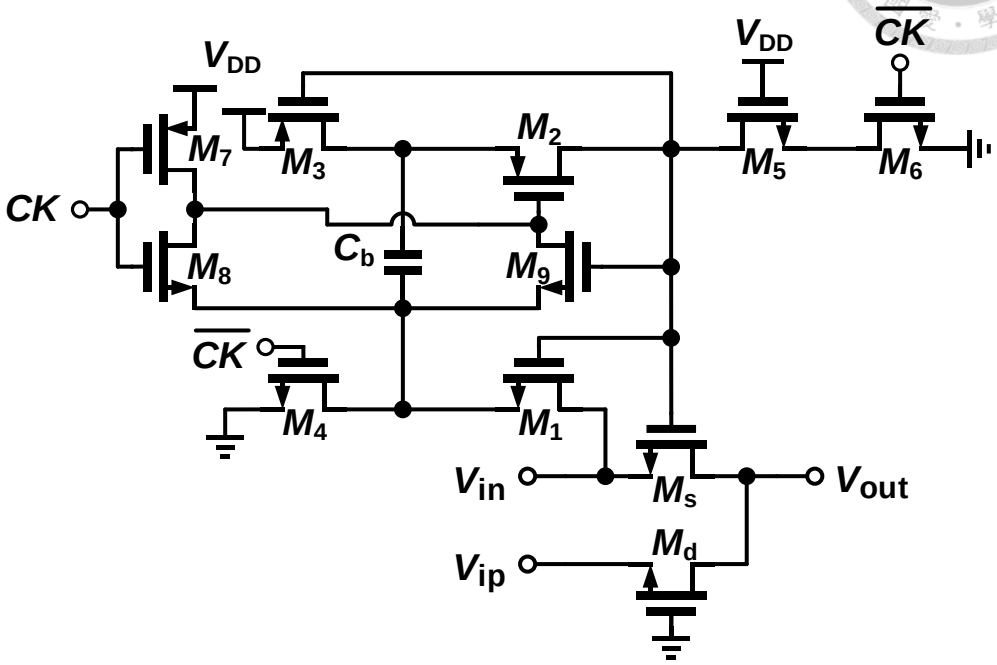
State	Sample	Conversion Steps(Raw bit)										
		1	2	3	4	5	6	7	8	9	10	11
Operation scheme	Reset/	Proposed Dual-Loop Asyn. Ctrl. + Latch logic										
Switching method	Sample	Switch back		Set-and-down								
Capacitor value(fF)		N/A	252	126	64	32	16	8	6	4	2	1
Bit weight		504	252	128	64	32	16	12	8	4	2	1
Error tolerance(LSB)		8	8	6	6	6	6	2	0	0	0	0
Search algorithm		Non-binary algorithm										
Calibration	None											

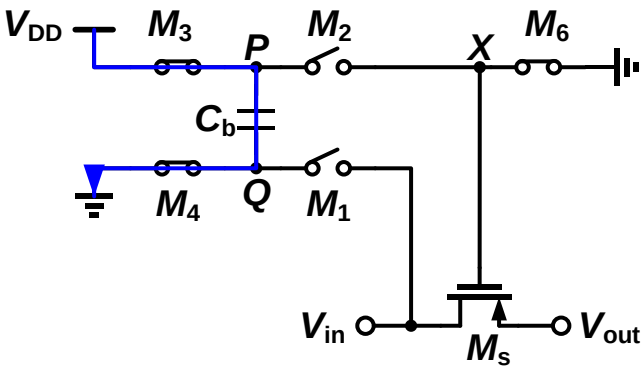
Table 3 Operation Scheme of proposed SAR ADC

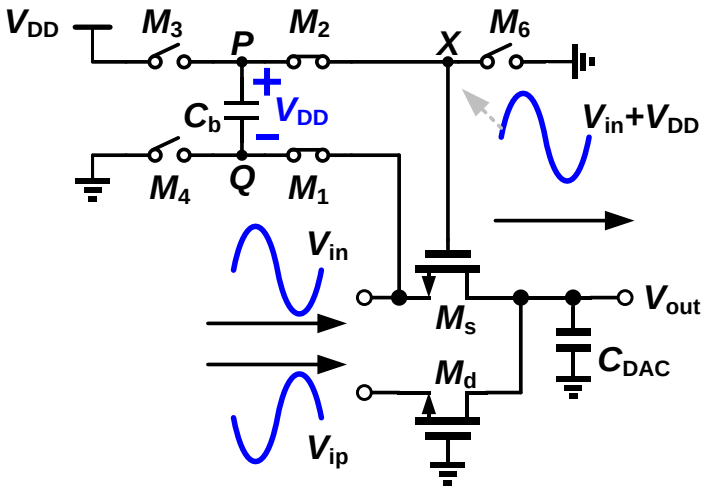
doi:10.6342/NTU201902051

4.4 Circuit implementation

4.4.1 Bootstrapped Switch







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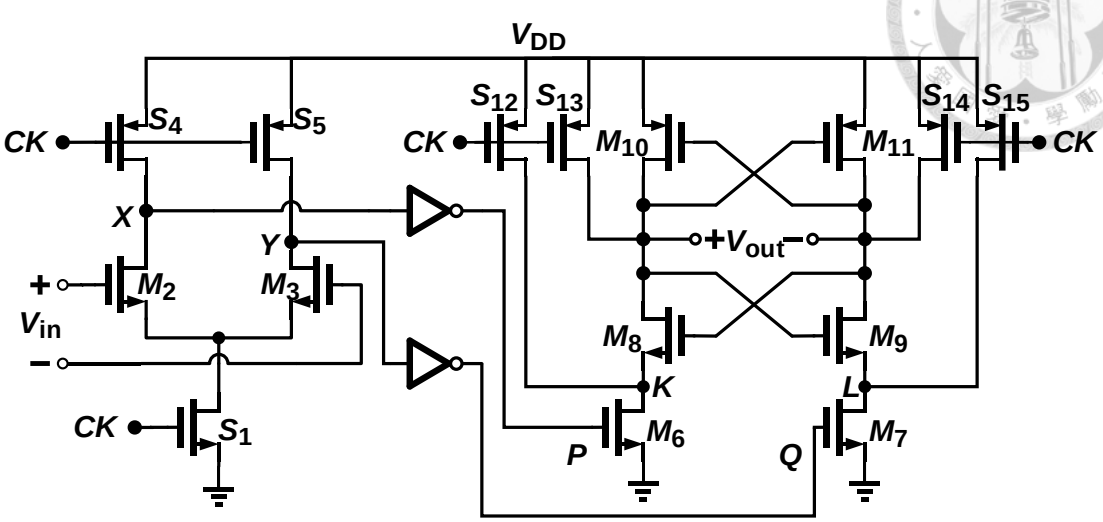
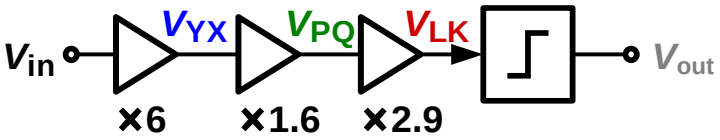
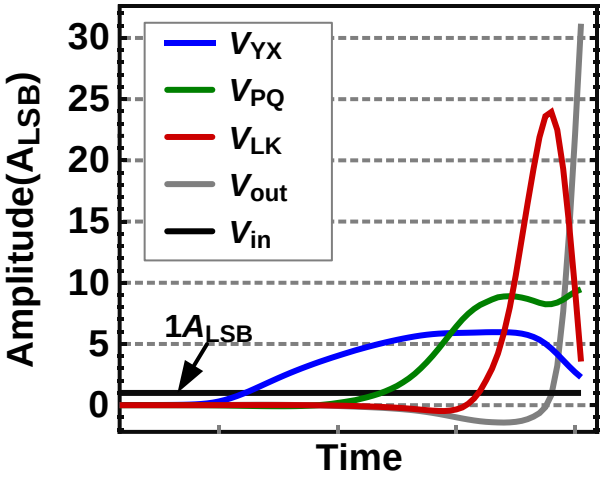
4.4.2 Three-stage dynamic comparator







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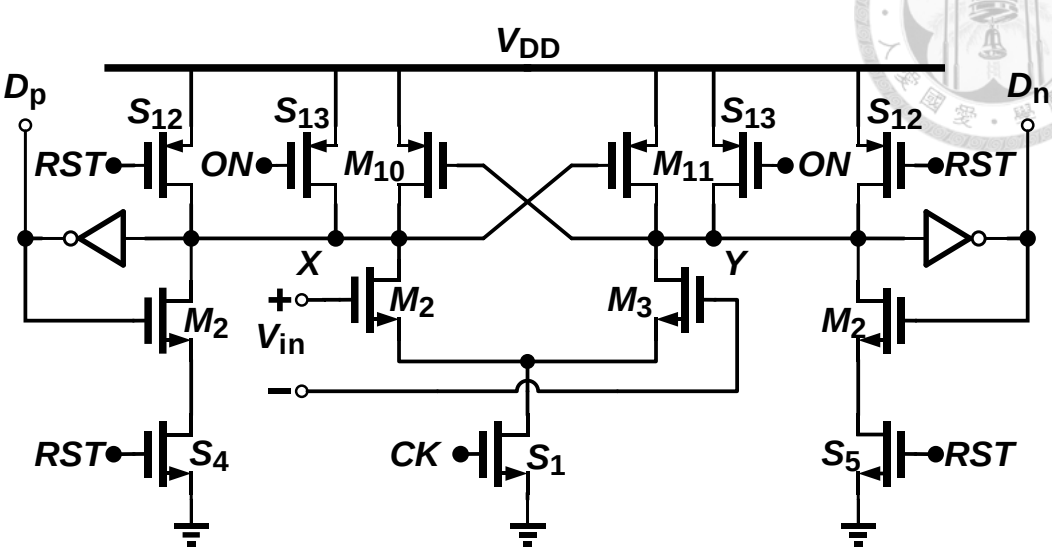
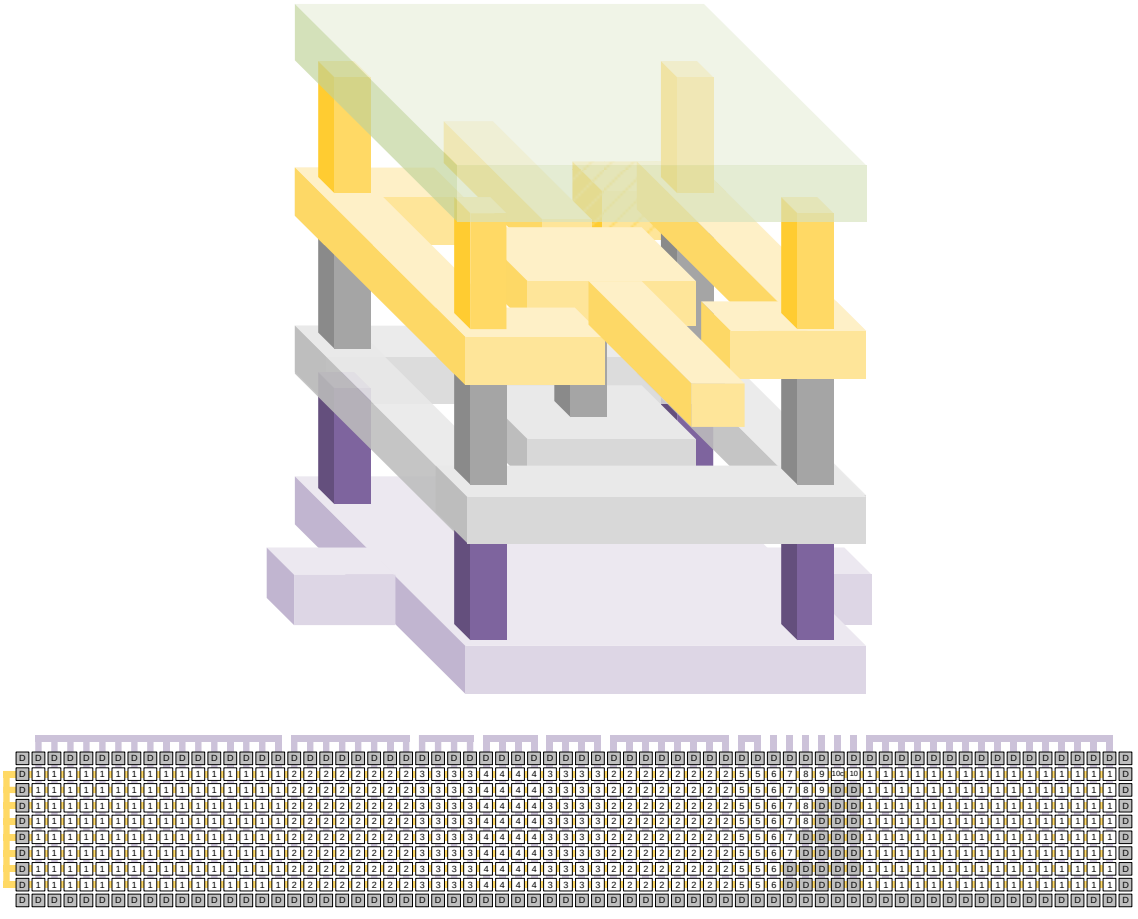
4.4.3 Latch SAR logic



4.4.4 DAC



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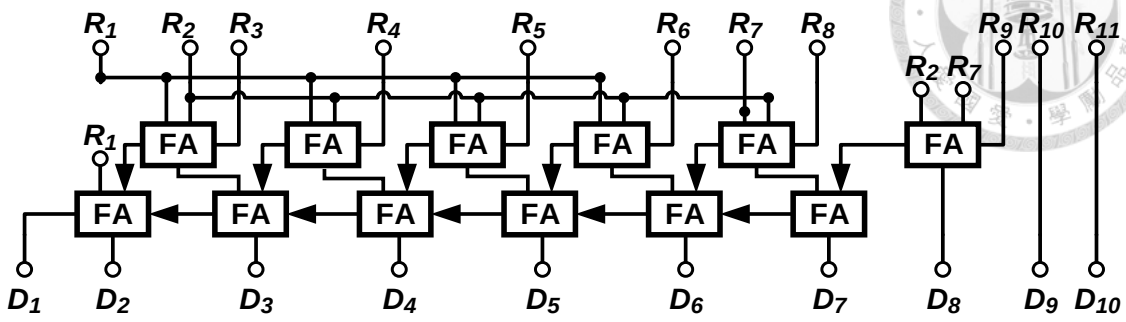
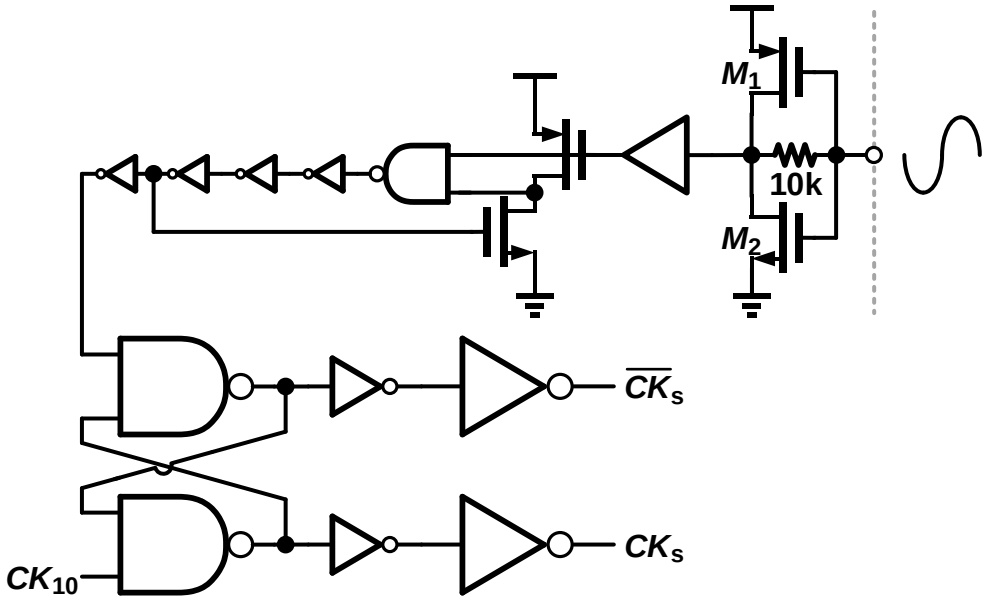
4.4.5 **Decoder**



4.4.6 **Sampling clock generator**



doi:10.6342/NTU201902051

Chapter 5 Post-Layout Simulations

This design is fabricated by TSMC 90nm 1P9M UTM CMOS process. Fig. 5.1 and Fig. 5.2 show the floor plan and the physical design of the proposed ADC, respectively.

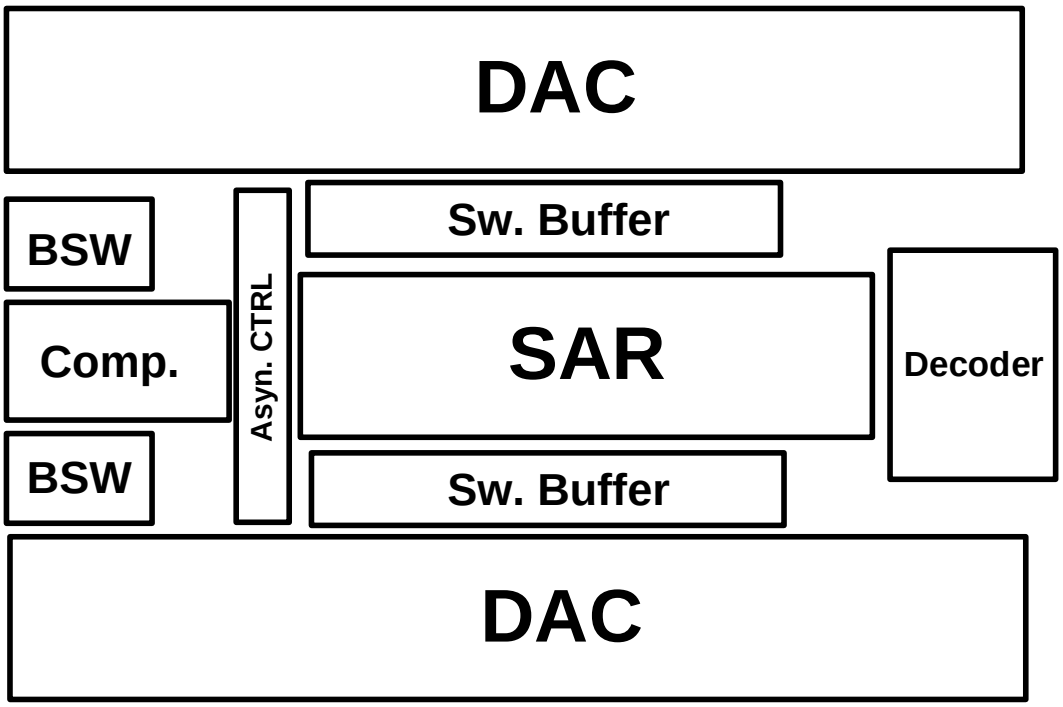


Fig. 5.1 Floor plan of the proposed SAR ADC

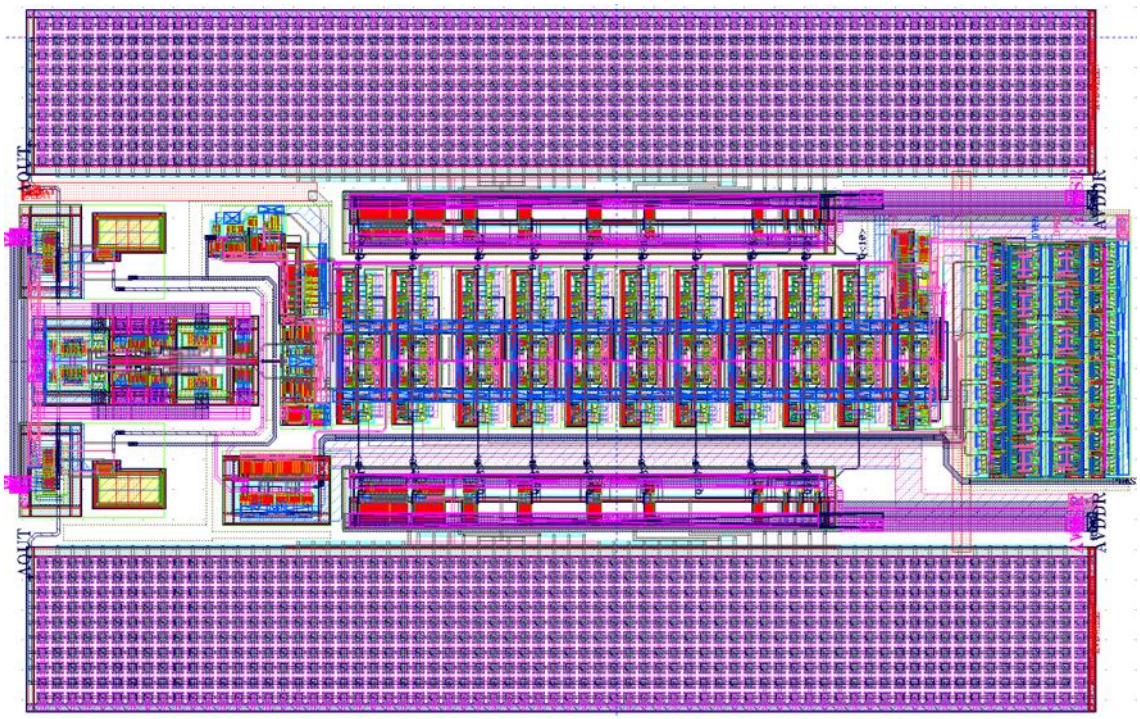


Fig. 5.2 Physical design of the proposed SAR ADC

doi:10.6342/NTU201902051

The post layout simulation was executed by HSPICE. Unless otherwise mentioned, the simulation conditions were set at 25°C, TT corner, 1 V supply voltage, 1.6 V peak-to-peak input swing, 200-MS/s sampling rate, and 256 sample points for FFT. The input frequency was set at Nyquist-rate.

Table 4 and Fig. 5.3 depict the dynamic performance under process variation with typical condition. The worst case is SS corner, which sampling-rate is degraded to 160 MS/s. The maximum power is 2.24 mW happened at FF corner and the minimum power is 1.43 mW happened at SS corner. ENOB keeps at least near 9.9 bit or up cross all corners.

Corner	ENOB(bits)	SNDR(dB)	Power(mW)
TT	9.9206	61.4820	1.92
FF	9.9220	61.4904	2.24
SF	10.0306	62.1442	1.92
FS	9.8979	61.3454	1.95
SS(160MS/s)	9.9313	61.5464	1.43

Table 4 SNDR performance and power consumption under process variation

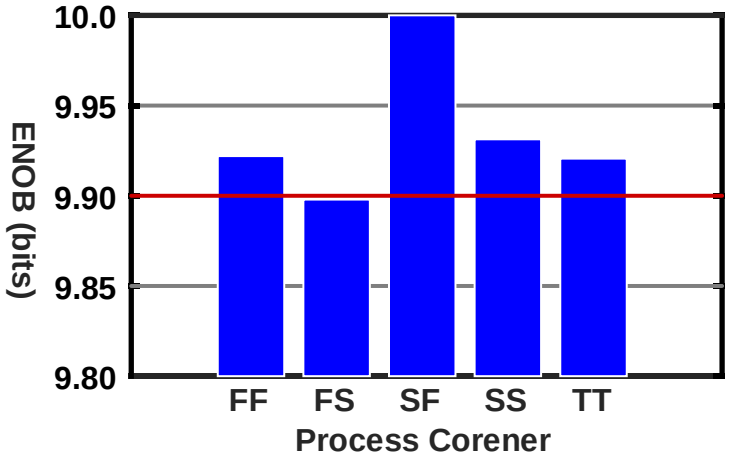


Fig. 5.3 Nyquist-rate ENOB under process variation

doi:10.6342/NTU201902051

Table 5 and Fig. 5.4 describe the dynamic performance under supply voltage ± 10 % variation with typical case. Fig. 5.5 plot the ADC output spectrums at different supply voltage. As supply voltage is reduced to 0.9V, the ENOB is 9.8841 bit, which is the worst one under this simulation and the power is 1.61mW. The maximum power reached 2.29mW at 1.1V supply voltage. ENOB keeps at least near 9.9 bit or up.

Voltage(V)	ENOB(bits)	SNDR(dB)	Power(mW)
0.9	9.8841	61.2623	1.61
1.0	9.9206	61.4820	1.92
1.1	10.0002	61.9612	2.29

Table 5 SNDR performance and power consumption under voltage variation

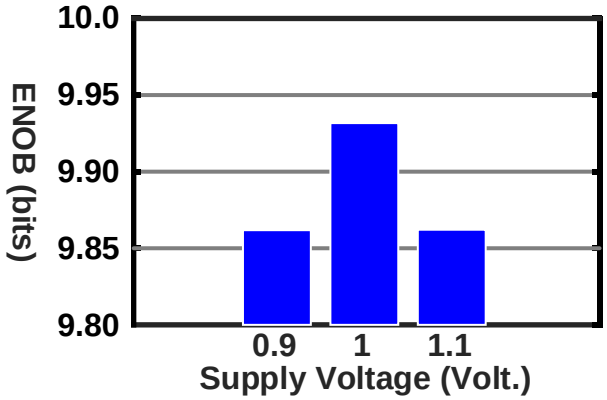


Fig. 5.4 Nyquist-rate ENOB under voltage variation

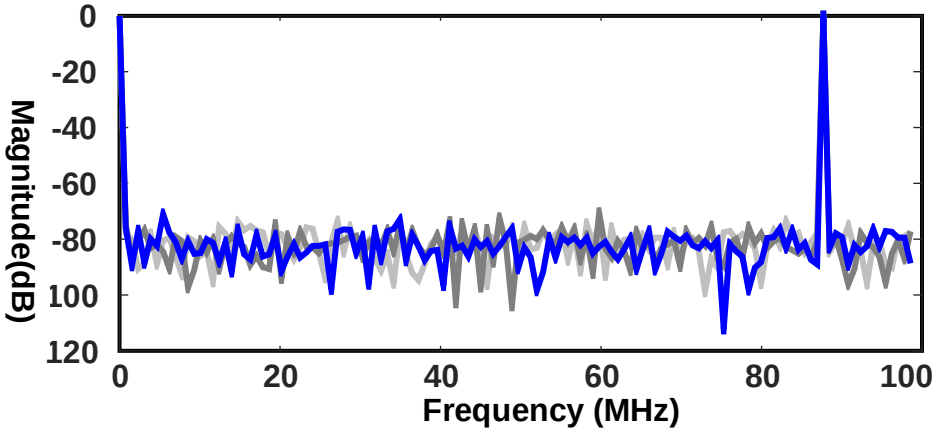


Fig. 5.5 Nyquist-rate output spectrum under voltage variation

doi:10.6342/NTU201902051

Table 6 and Fig. 5.6 describe the dynamic performance under temperature range from 0°C to 100°C. Fig. 5.7 plot the ADC output spectrums at different temperatures. Worst-case ENOB is 9.8792 bit at 0°C while power is at the lowest value, 1.86mW. The maximum power happened at 80°C and consumed 2.08mW. ENOB keeps at least 9.8 bits.

Temperature(℃)	ENOB(bits)	SNDR(dB)	Power(mW)
0	9.8792	61.2328	1.86
20	9.9122	61.4314	1.90
40	9.9789	61.8330	1.95
60	9.9169	61.4597	2.01
80	9.8655	61.1503	2.08
100	10.0378	62.1876	2.01

Table 6 SNDR performance and power consumption under temperature variation

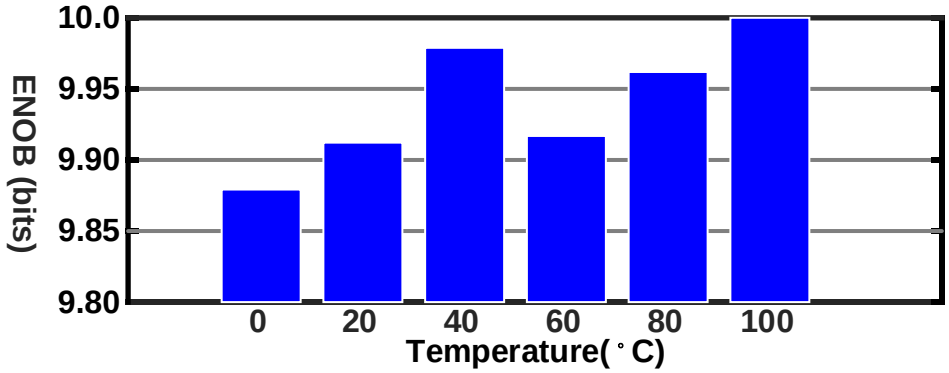


Fig. 5.6 Nyquist-rate ENOB under temperature variation

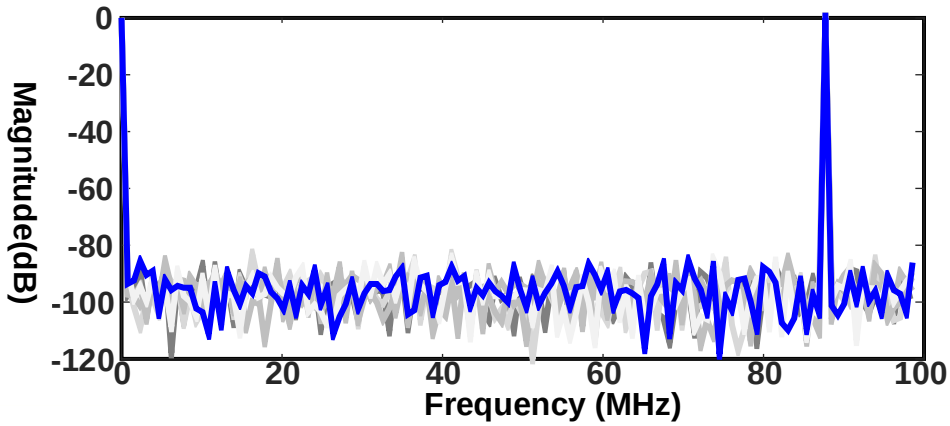


Fig. 5.7 Nyquist-rate output spectrum under temperature variation

doi:10.6342/NTU201902051

Fig. 6.8 summarizes the ENOB drift based on operating voltage or operating temperature or process variation. As can be seen in that figure, only when the process is located at SS corner that the sample-rate of this design should be reduced. Beside SS corner, the proposed SAR ADC can keep ENOB at least 9.85 bit at 200MS/s.

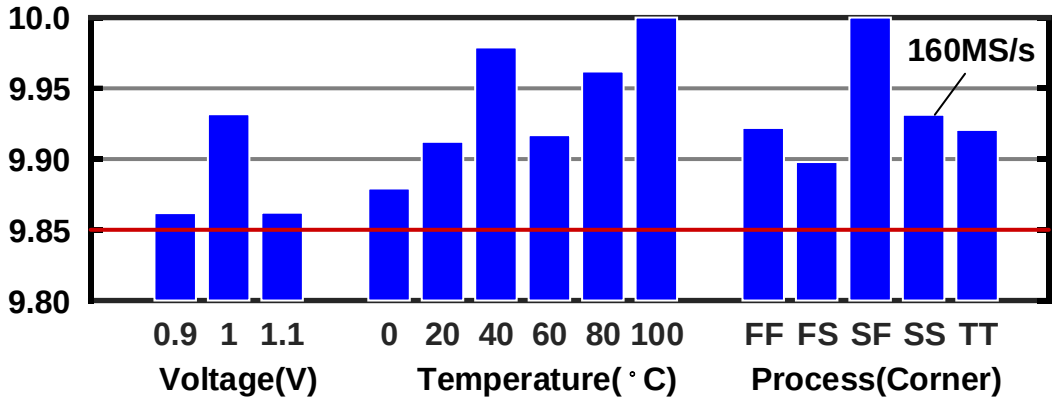


Fig. 5.8 Cross comparison of Nyquist-rate ENOB changed in either voltage, temperature, or process corner variations

Next, a PVT simulation is made to check the performance at extreme conditions. A common extreme PVT simulation setting is list in Table 7. The simulation results are list in Table 8. The worst ENOB is 9.5656 bit and the maximum power comes to 2.5mW.

No.	Case	Process Corner(P)	Voltage(V)	Temperature(T)
1	Typical	Typical-Typical(TT)	1.0V	27C
2	Best	Fast-Fast(FF)	1.1V	0C
3	Worst	Slow-Slow(SS)	0.9V	100C

Table 7 Settings for Extreme PVT conditions

Case	ENOB(bits)	SNDR(dB)	Power(mW)
Typical	9.9206	61.4820	1.92
Best	9.9588	61.7120	2.50
Worst(120MS/s)	9.8656	61.1509	0.98

Table 8 SNDR performance and power consumption under PVT variation

doi:10.6342/NTU201902051

Table 9 and Fig. 5.9 illustrate the dynamic performance under different input frequencies. The ENOB is 10.0619 bits with 9 MHz input frequency and 9.9206 bits with 90 MHz input frequency. ENOB can still keep at 9.9150 bits even with R+C+CC parasitic Fig. 5.10 plot the output spectrums under different input frequencies.

Input Frequency(Hz)	ENOB(bits)	SNDR(dB)	Power(mW)
9E+06	10.0619	62.3326	1.89
2E+07	9.9663	61.7571	1.90
4E+07	9.8913	61.3056	1.91
6E+07	9.9381	61.5874	1.91
7E+07	9.9468	61.6397	1.92
9E+07	9.9206	61.4820	1.92
9E+07(R+C+CC)	9.9150	61.4483	1.92

Table 9 SNDR performance and power consumption under different input frequencies

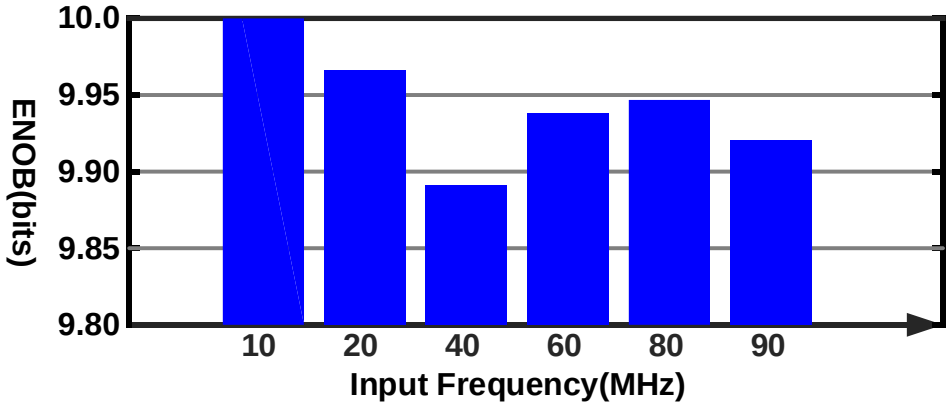


Fig. 5.9 Nyquist-rate ENOB under different input frequencies

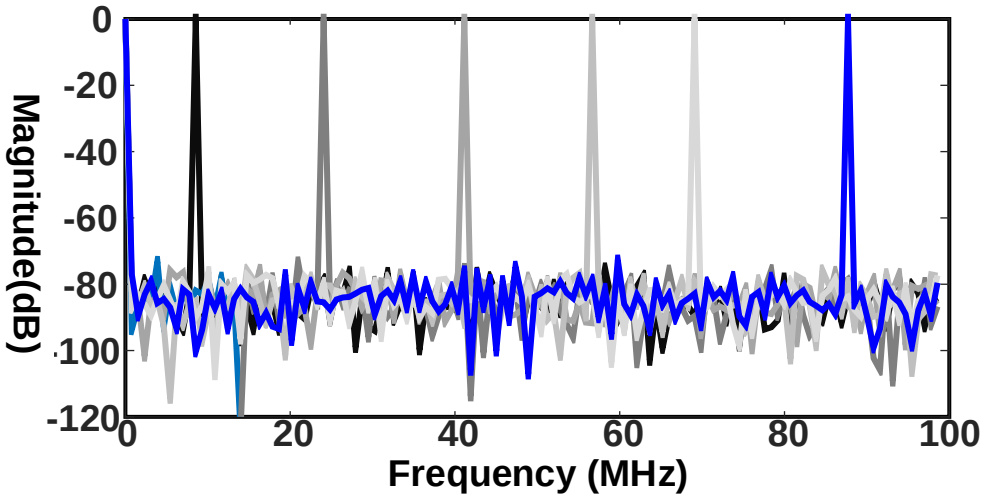


Fig. 5.10 Nyquist-rate output spectrum under different input frequencies

doi:10.6342/NTU201902051

Fig. 5.11 shows the static performance of the proposed SAR ADC. The maximum minimum DNL are +0.031 LSB and -0.156 LSB respectively. The maximum and minimum INL are +0.162 LSB and -0.225 LSB respectively. The average power consumption is divided into analog, digital and reference parts. They consumed 635uW, 943uW, and 341uW respectively. Fig. 5.12 shows the pie chart of power consumptions. Table 10 summarizes the performance of the proposed SAR ADC from simulation results.

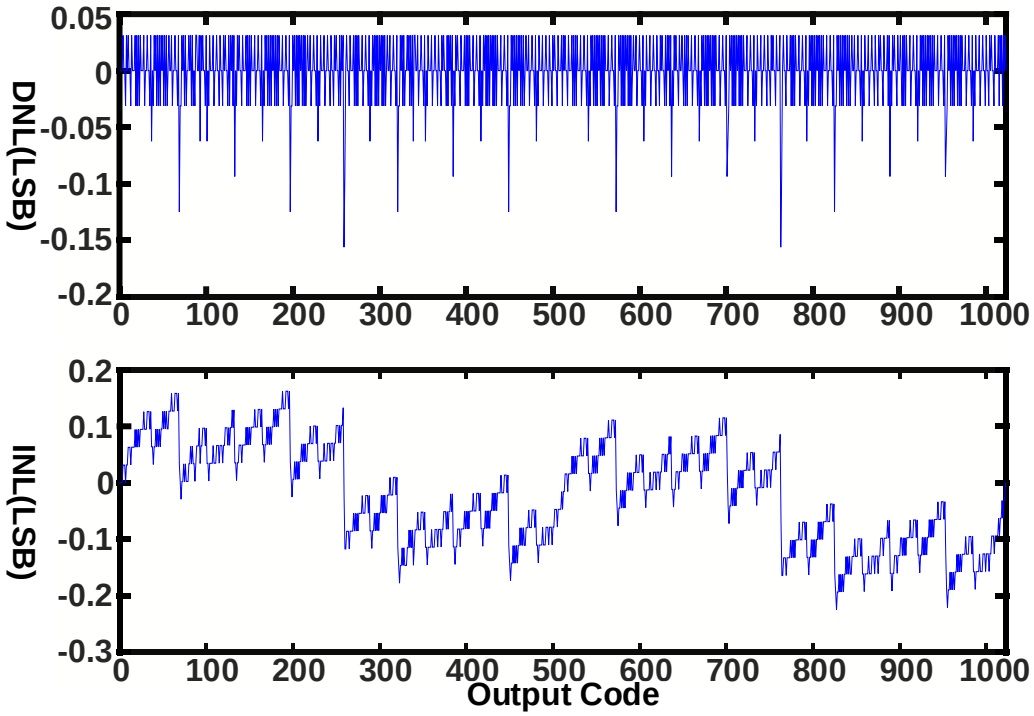


Fig. 5.11 DNL and INL of the proposed SAR ADC from post-layout simulation

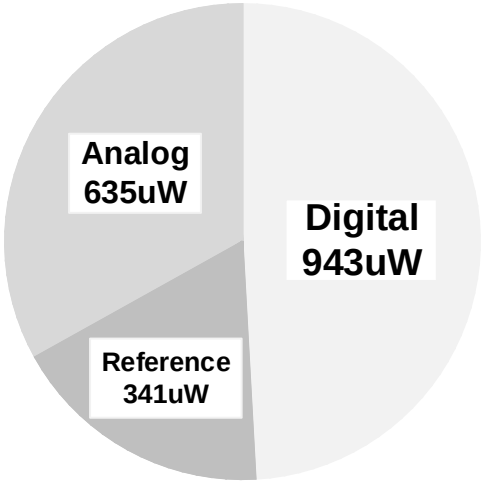


Fig. 5.12 Power consumptions of the proposed SAR ADC

doi:10.6342/NTU201902051

	Spec.	Pre-sim.	Post-sim.
Resolution(bit)	10	10	10
Sample-rate(MS/s)	200	200	200
Input Range(Vpp)	N/A	1.9	1.6
DNL(LSB)	N/A	N/A	0.031/-0.156
INL(LSB)	N/A	N/A	0.162/-0.225
SNDR@DC(dB)	N/A	62.4	61.8
SNDR@NQ(dB)	N/A	61.8	61.5
THD(dB)	N/A	-75.6	-71.6
SFDR(dB)	N/A	77.7	76.4
ERBW(MHz)	100	100	100
ENOB(bit)	≥9.0	9.97	9.92
Supply	≤1.0	1	1
Power(mW)	≤2.0	1.76	1.92
Area(mm^2)	N/A	N/A	0.022
Technology	90nm CMOS	90nm CMOS	90nm CMOS

Table 10 Performance summary of the post-layout simulation

doi:10.6342/NTU201902051

Chapter 6 Measurement Considerations

Since the proposed design is still under manufacturing process at the time of writing this thesis, there was no measurement result yet. In order to ensure that the chip after fabrication can be verified, this design considers the impacts on circuit performance from the non-idealities of chip fabrication, packaging, and PCB assembly processes. Section 6.1 describes the noise coupling phenomena. Section 6.2 descrbes various noise suppression techniques used in this design. Section 6.3 is the result of the simulation after the full wafer layoutNoise coupling

6.1 Noise coupling in the proposed ADC

6.1.1 Substrate noise

Noise coupling is that activing signals in one circuit couple into other circuits therefore degrading their performance [37]. A kind of noise coupling in this work is the so-called “substrate noise”, which often resulting in today’s heavily-doped substrate type of CMOS process technologies [38]. Fig. 6.1 shows that all the ground voltages in the proposed design are bouncing when the output signal $\mathrm{CLK_{LA}}$ transiting its state. $\mathrm{CLK_{LA}}$ is used to synchronize the output codes of the ADC and the testing equipment, a logic analyzer. This signal allows the logic analyzer exactly capture the digital codes from the ADC. Although $\mathrm{CLK_{LA}}$ relax the difficulties of measuring output digital codes, its switching couple to the substrate of the chip and degrade the performances of ADC.

The reason why noise coupling into the substrate can easy spreading all over the chip is because the low resistivity bulk acts like a lumped substrate node, noise propagates with little attenuation throughout the entire chip. Fig. 6.1 shows all the ground planes in this design and a resistive substrate model in the background. Fig. 6.3 shows how substrate noise as $\mathrm{CLK_{LA}}$ induced one propagate to entire chip grounds.

doi:10.6342/NTU201902051

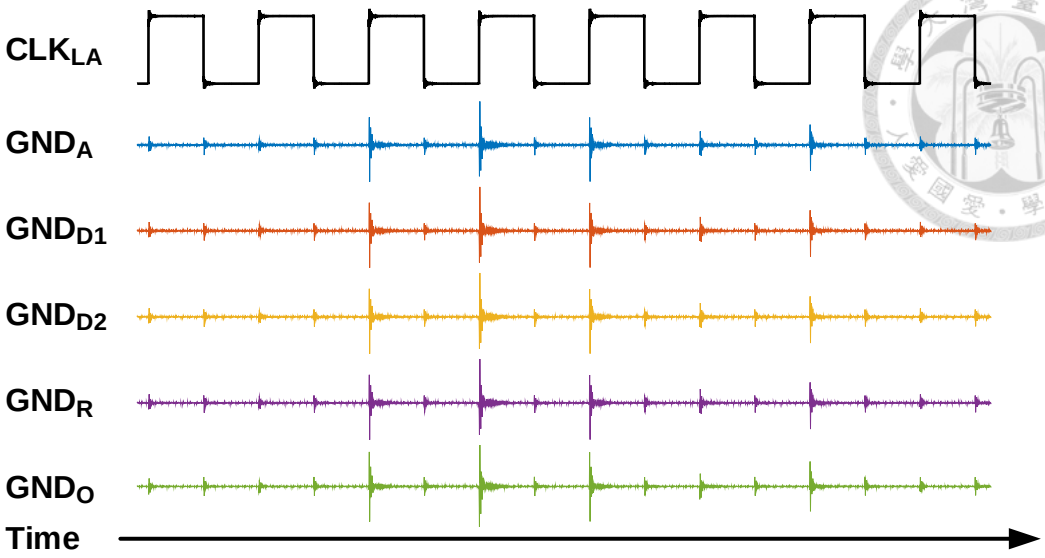


Fig. 6.1 Ground bouncing due to output clock signal coupling to substrate

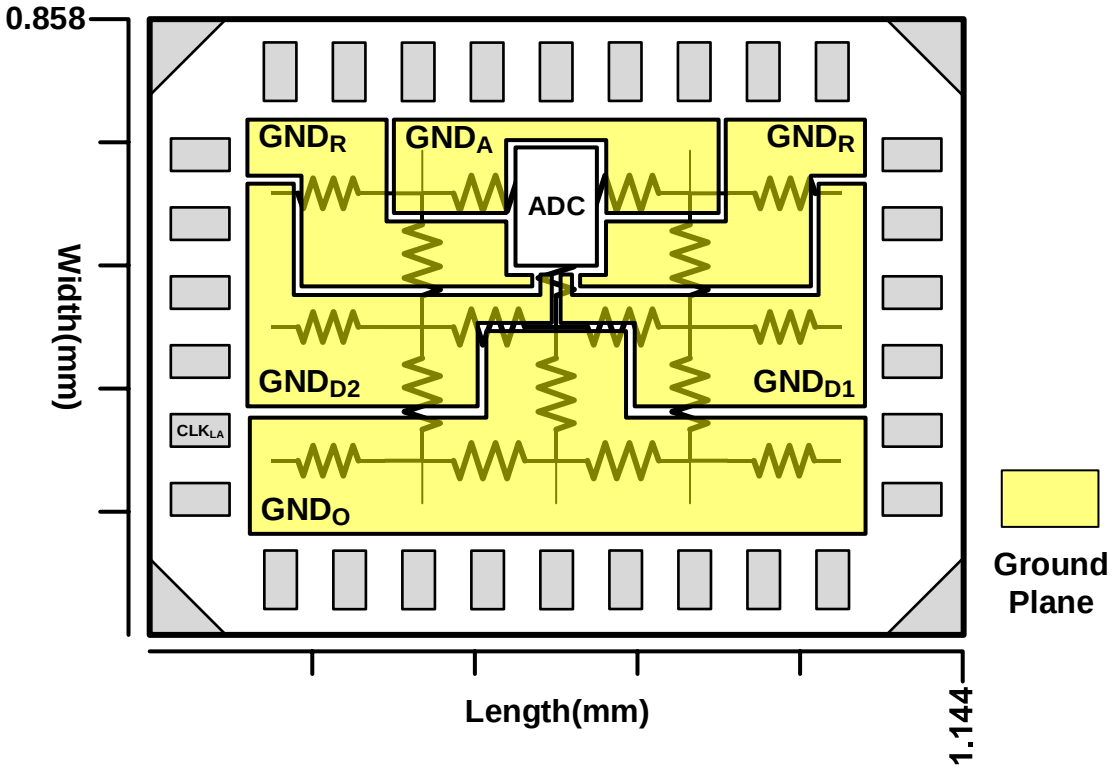


Fig. 6.2 Ground planes in this work and a resistive substrate model in the background

doi:10.6342/NTU201902051

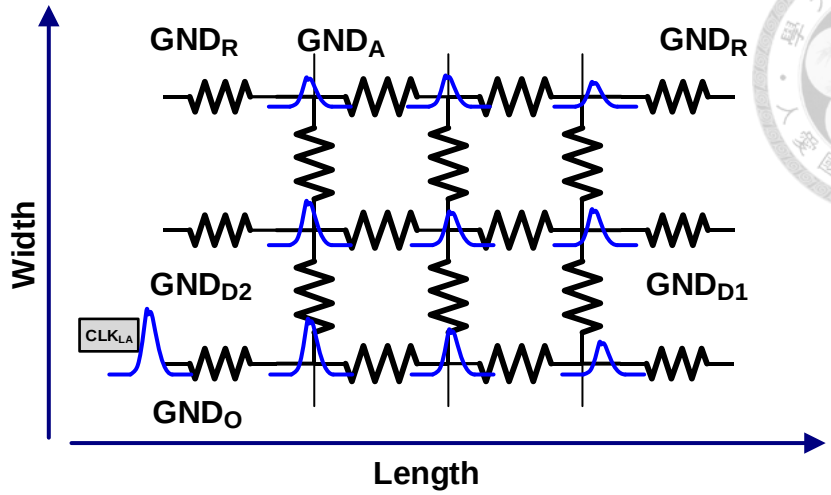


Fig. 6.3 Coupling noise is distributed through resistive substrate network

6.1.2 **Power supply noise**

Most functional blocks of a high-speed SAR ADCs are digital circuits, they requires a large amount of transient current to charge or discharge their loading. Those currents are suppled from out-side the chip through bonding wires. Since there is a gap in height between the PCB/package and the chip. Bonding wires connect to chip will appear inductive parasitic. Fig. 6.4 shows the connection of power domains and PCB of this work.

Power supplies of this design are divided into five domains, they are analog power, VDD_A; reference power, VDD_R; digital power, VDD_{D1}, digital power for sampling clock, VDD_{D2} and output buffer power, VDD_O. By doing so, noise resulting from transient current through inductive parasitic of bonding wire will not couple to other blocks through power line distribution since the powers are separated. However, functional blocks under a certain power domain still suffer from their own power supply noise. Fig. 6.5 recorded a period of voltage waveforms of this work. As can be seen in the figure, output buffer draws maximum current and therefore produce largest power supply noise,

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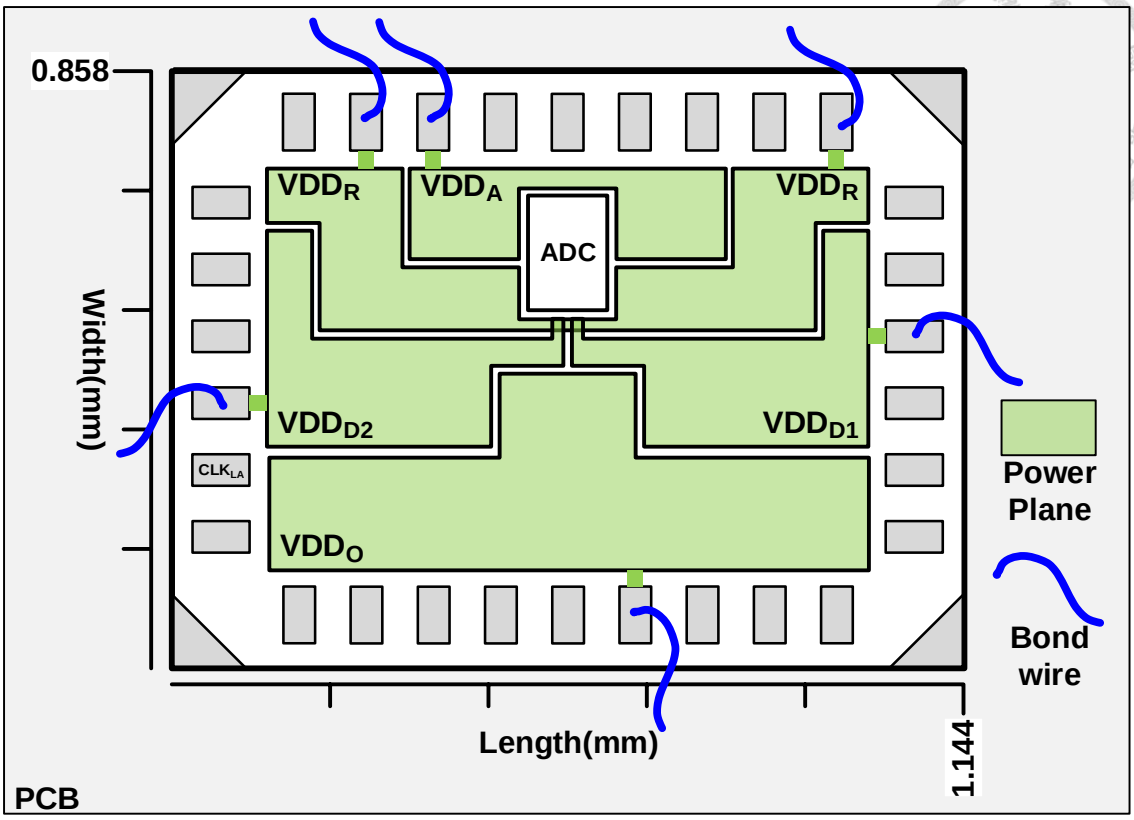

Fig. 6.4 Power domains of this work and their connections to PCB through inductive bonding wires

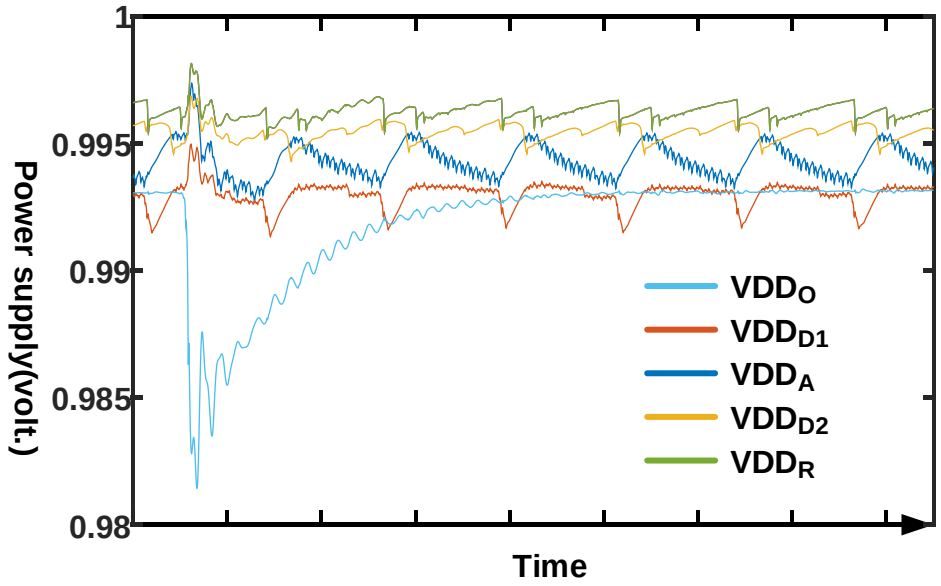

Fig. 6.5 Power supply noises of this work due to transient current pass through inductive bond wires

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6.1.3 Signal crosstalk

It has encouraged to add seal ring and corner to protect the chip to prevent it be damaged from dicing [39]. However, sear ring and corner also provide a low impedance path for noise coupling to entire chip [40]. Fig. 6.6 shows how high swing, high switching noise PADs couple noise through low impedance sear ring to sensitive analog input PADs.

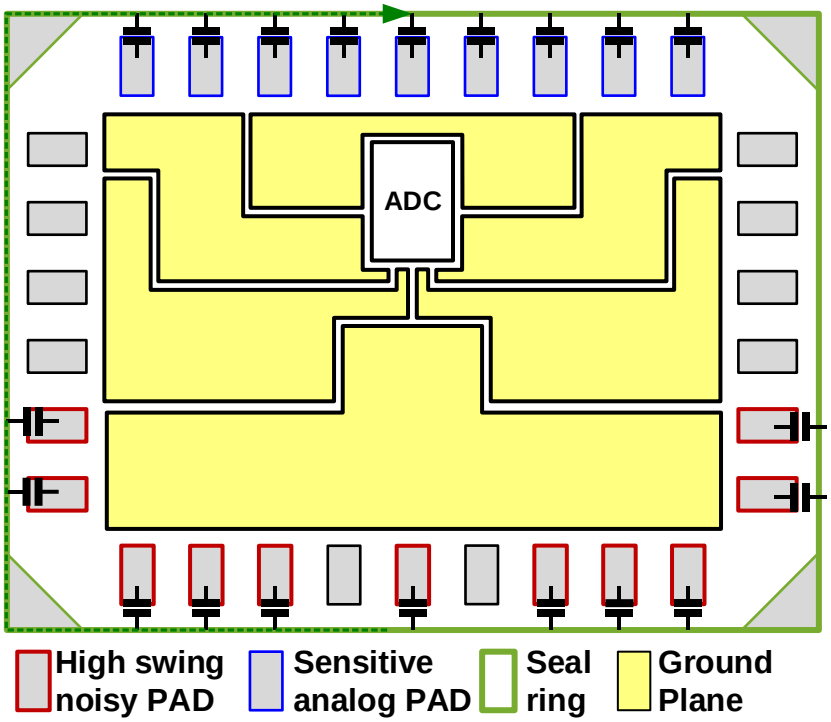

Fig. 6.6 Signal coupling through low impedance seal ring in this work

6.2 Design for noise coupling suppression

Beside basic isolation measures such as multiple power domain, sensitive and noisy PADs separation. Many advanced isolation measures are also applied in this design. Fig. 6.7 shows blocks in the ADC layout and those in the layout of CHIP that using Deep N-well layer to implement their NMOS. Deep N-well can be used to reduce noise coupling to substrate and reduce noise reception to sensitive circuits.

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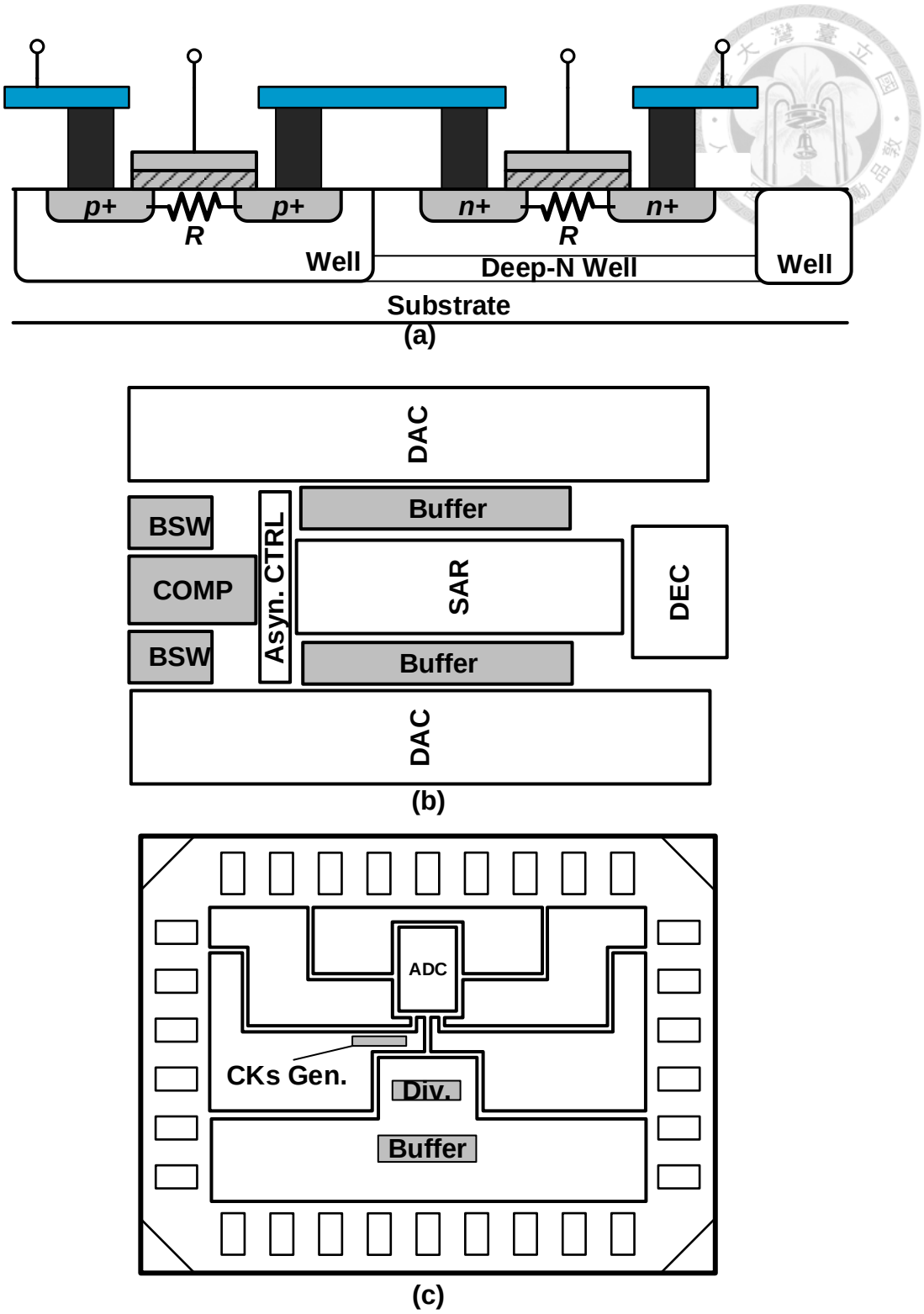

Fig. 6.7 (a)Deep N-Well is used to isolate NMOS from resistive substrate. (b),(c) Sensitive circuit blocks using Deep N-Well to isolate noise coupling are marked in gray

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Suppression of power supply noises is by inserting damping resistor and adding decoupling capacitor. Although ground and power planes have their own equivalent resistance and therefore adds some damping. However, resistances come from those planes are strong geometry depend and usually are very low values. To ensure critical damping exists, we series a resistor between the power PAD and the corresponding power plane. The value of the resistor depend on the decoupling capacitance and the target inductance. Equation (3.1) indicate how to calculate the critical resistance. Where C_{dep} is the decoupling capacitance and L_{bond} is the target parasitic inductance of bond wire.

$$R_{crit.} = 2 \times \sqrt{\frac{L_{bond}}{C_{dep}}} \tag{6.1}$$

Fig. 6.8 shows the circuit model of damping insertion of this design and how critical damping works. The model include a inductive bond wire, L_{bond}, and the suppression insertion, $R_{crit.}$ and C_{dep}.

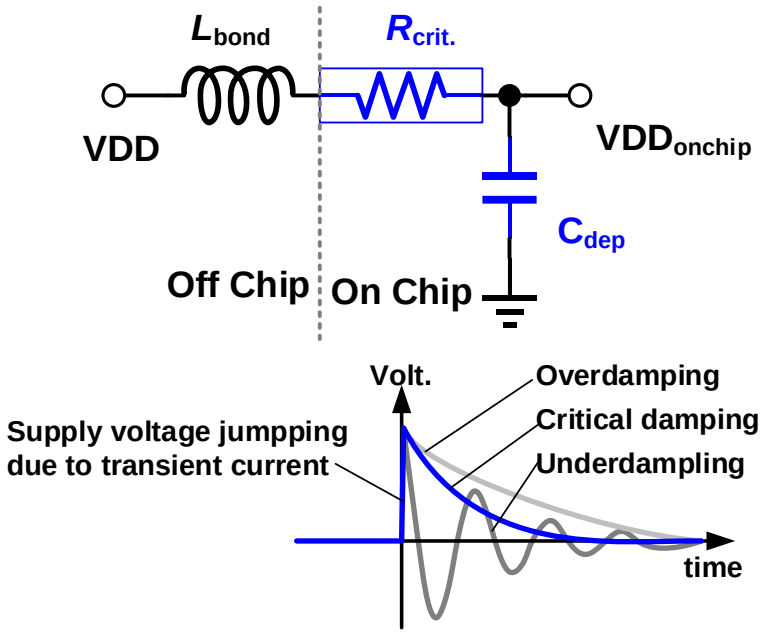

Fig. 6.8 Circuit model for suppression of power supply noise in this work

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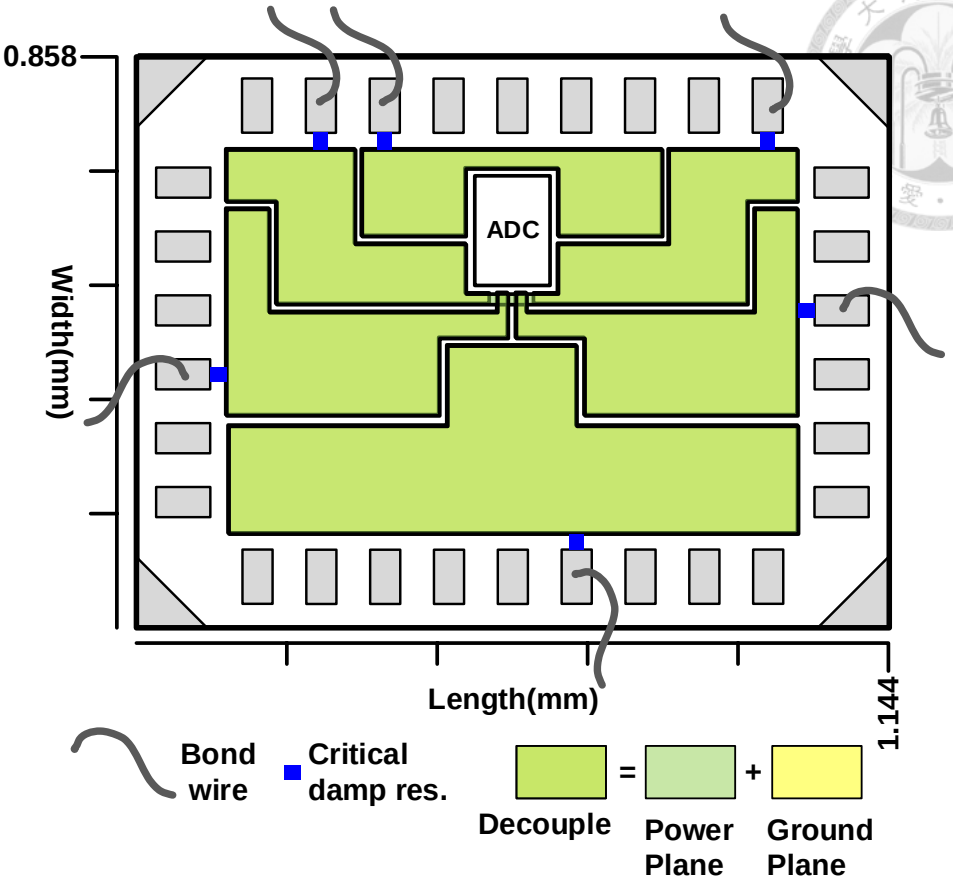

Fig. 6.9 Decoupling capacitors adding to this work by the parasitic capacitance between the power and ground planes

Finally, crosstalk through low impedance seal ring to sensitive PADs are prevent by shielding. Three dedicated shielding metals surrounded target PADs as shown in Fig. 6.10. First shielding metal colored in blue in Fig. 6.10 surrounded most sensitive analog input PADs, Ain and Aip, and was connected to a quiet common mode voltage, Vcm. Second shielding metal colored in red is used to protect reference voltage from noise interference to ensure its precision and it is connected to a quiet ground voltage, GND. The last shielding metal is colored in green and is connected to a quiet power voltage GND. It surrounding noisy and high swing digital output PADs to shunt their switching noise to outside the chip rather than let them coupling into seal ring and spread to entire chip PADs.

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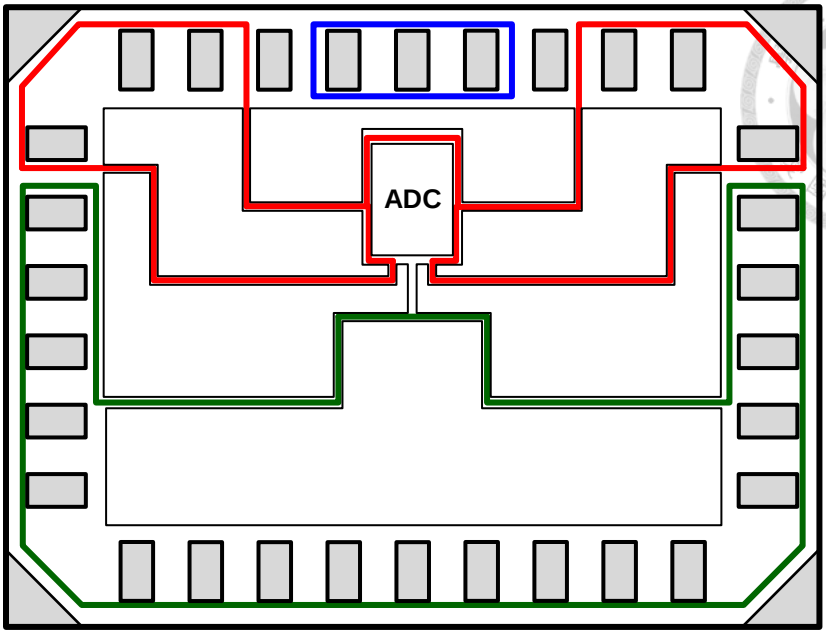

Fig. 6.10 Three shielding metals surrounded different PAD groups to pervert crosstalk

6.3 Chip floor plan and layout

The proposed 10-bit 200-MS/s SAR ADC is fabricated in TSMC 90-nm UTM CMOS technology. The floor plan of chip is shown in Fig. 6.11. The chip area is 0.9815 mm2 in size of 1144 μm × 858 μm, and the layout area of the proposed ADC is 0.02208 mm2 in size of 115 μm × 192 μm. The area of reference buffer and CDAC occupy about 7.62 % and 44 % of the core area respectively. Comparator and bootstrapped switches occupy about 6.6 % and 3.4 % of the core area, respectively. The whole digital parts of the proposed SAR ADC, which includes SAR latch logic, SAR logic controller, proposed dual-loop asynchronous controller, and decoder occupies 26% of the core area. The entire chip layout includes noise suppression physical design mentioned in previous section is shown in Fig. 6.12.

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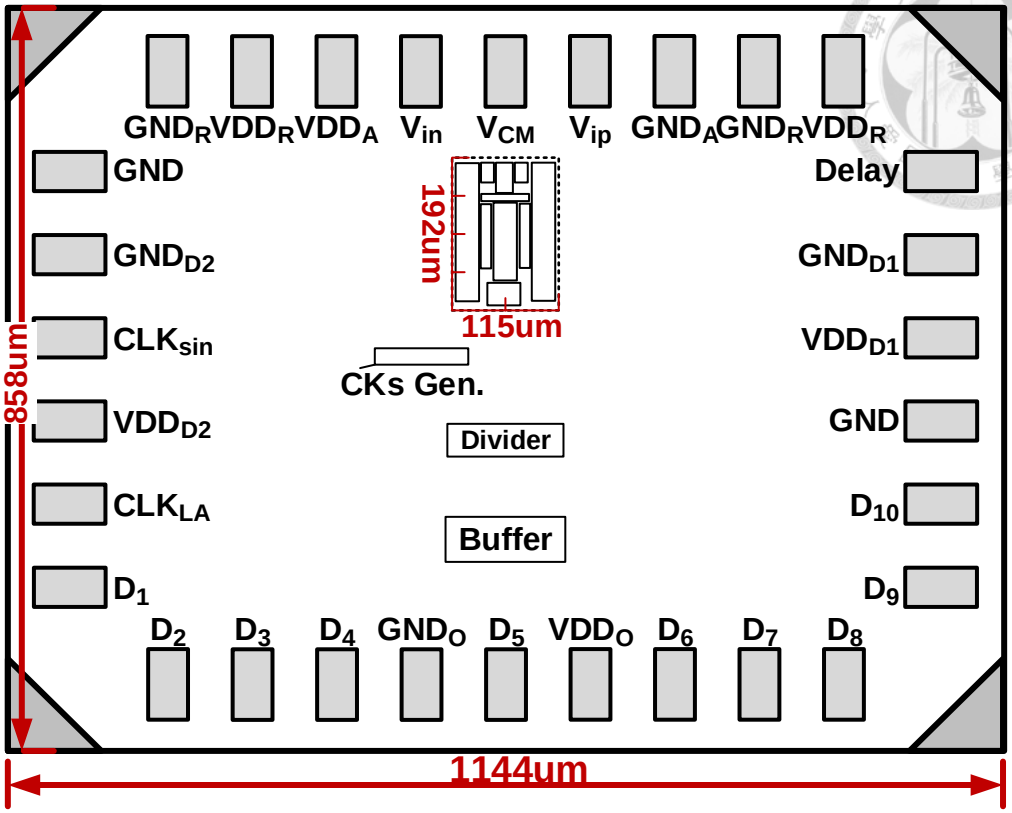

Fig. 6.11 Chip floor plan of the proposed SAR ADC

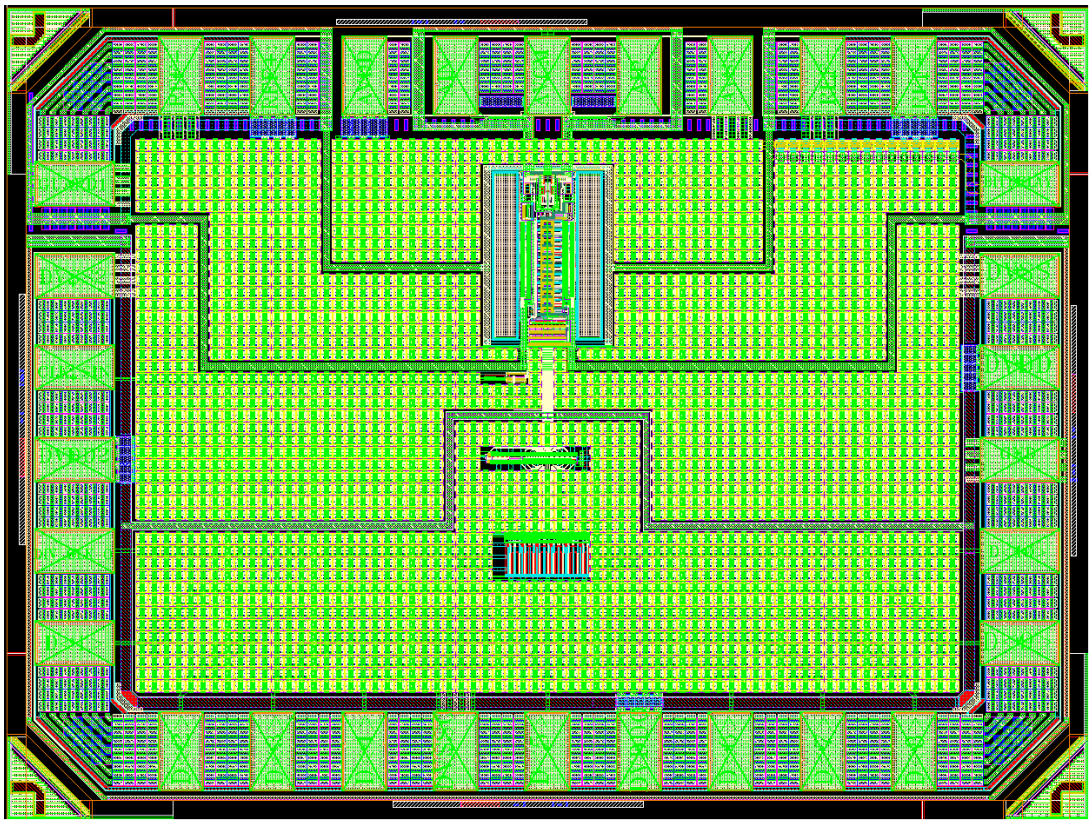

Fig. 6.12 Chip layout of the proposed SAR ADC

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6.4 Full-chip simulation and performance prediction

Fig. 6.13 shows the full-chip static performance. The peak-to-peak DNL and INL worsen than those only from ADC layout without considering peripheral parasitic. The full-chip peak-to-peak DNL and INL are +0.097/-0.538 LSB and +0.518/-0.48 LSB respectively. There is no missing code existing. The negative peak near the middle of output code in the DNL plot is caused by capacitor mismatching while the actual MSB capacitance is smaller than the ideal one. It results in a drop in the INL plot.

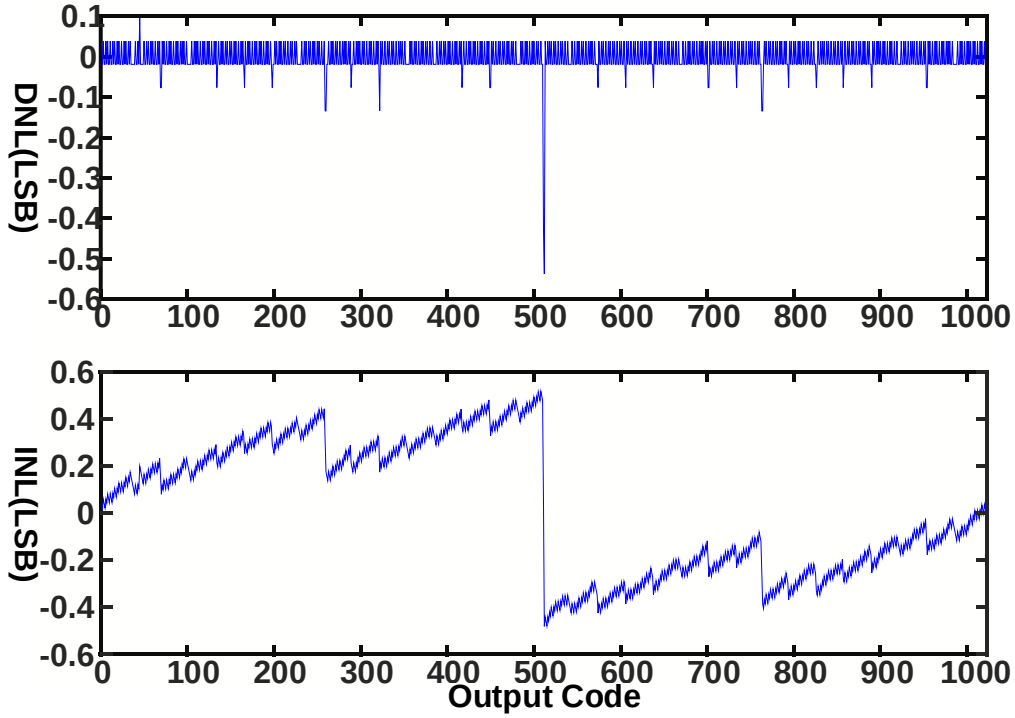

Fig. 6.13 Full-chip static performance simulation

The dynamic performances are all degraded due to the parasitic now comes from all over the chip. Table 11 shows both the static and dynamic performances before and after including the full-chip parasitic. The simulated full-chip SNDR, SFDR, and THD are 59.41 dB, 67.19 dB and -64.94 dB respectively. The full-chip Nyquist-rate ENOB is degraded to 9.8 bits.

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	Spec.	ADC Only	Full-Chip
Resolution(bit)	10	10	10
Sample-rate(MS/s)	200	200	200
Input Range(Vpp)	N/A	1.6	1.6
DNL(LSB)	N/A	0.031/-0.156	0.097/-0.538
INL(LSB)	N/A	0.162/-0.225	0.518/-0.48
SNDR@DC(dB)	N/A	61.8	60.2
SNDR@NQ(dB)	N/A	61.5	60.1
THD(dB)	N/A	-71.6	-65.2
SFDR@DC(dB)	N/A	76.4	66.5
ERBW(MHz)	100	100	100
ENOB@NQ(bit)	≥9.0	9.92	9.69
Supply	≤1.0	1	1
Power(mW)	≤2.0	1.92	*1.92
Area(mm^2)	N/A	0.022	0.9815
Technology	90nm CMOS	90nm CMOS	90nm CMOS

***w/o including peripheral powers**

Table 11 Full-chip performance of the proposed SAR ADC

Although resistors and coupling capacitors have been added to the power supplies of this work, power noises still exist unless inductive parasitic disappear. Different bond-wire inductances will make the damping becomes over-, critical-, or under-damped since damping resistor and decoupling capacitor are fixed. Before simulating the performance degradation due to over- or under- estimated bond wire inductance, a substrate model like that in Fig. 6.14 should be added to co-simulate noise coupling from the substrate.

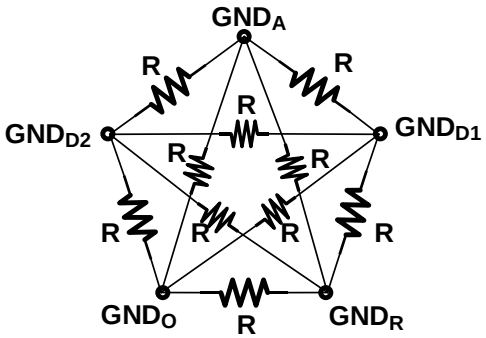

Fig. 6.14 A resistive network is used to model the substrate of this work

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Table 12 and Fig. 6.15 describe the dynamic performance under different bond wire inductances and substrate resistance. The parasitic inductance for critical damping insertion in this design is 2nH. As parasitic inductance is about 2nH, the ENOB is 9.11 bit with 1-ohm substrate resistance and 9.26 bit with 5-ohm substrate resistance, respectively. If the real parasitic inductance is great than 2nH, then the damping insertion becomes under-damped one. At under-damped condition, ENOB degraded rapidly because the power supply induced errors and noises are gradually growth.

Bond-wire Inductance(nH)	ENOB(Bit)	
	R=1ohm	R=5ohm
1	9.4569	9.6388
2	9.1113	9.2597
3	8.7361	8.7628
4	8.3258	8.6603
5	8.3253	8.4378

Table 12 ENOB versus bond wire inductance an Nyquist-rate input frequency, 200MS/s

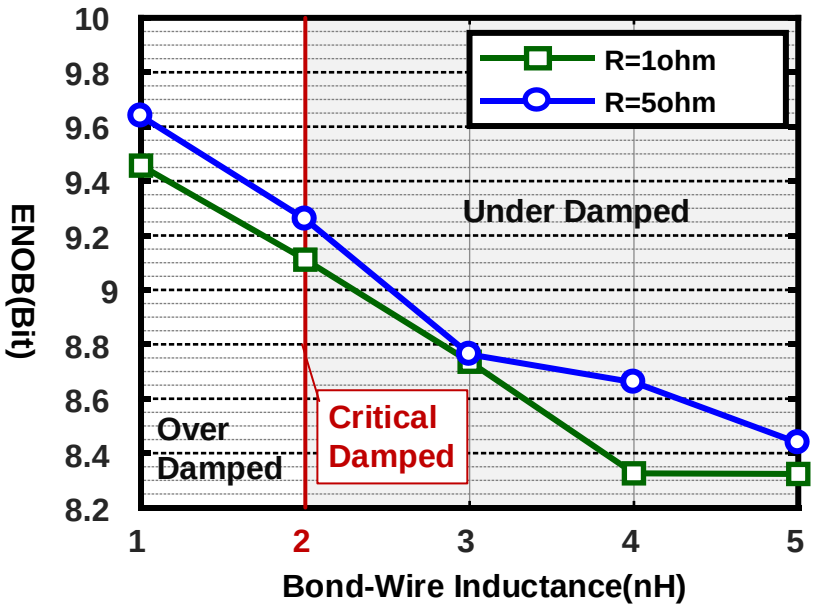

Fig. 6.15 ENOB@Nyquist-rate versus bond wire parasitic inductance

Fig. 6.16 shows the static performance prediction of the proposed SAR ADC with 2% mismatch in unit-capacitance. The maximum 1-sigma INL is 0.297 LSB and the maximum 1-sigma DNL is 0.35 LSB. These results predict that there may be no missing

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code (DNL= -1 LSB) within 3-sigma (95%) chip products

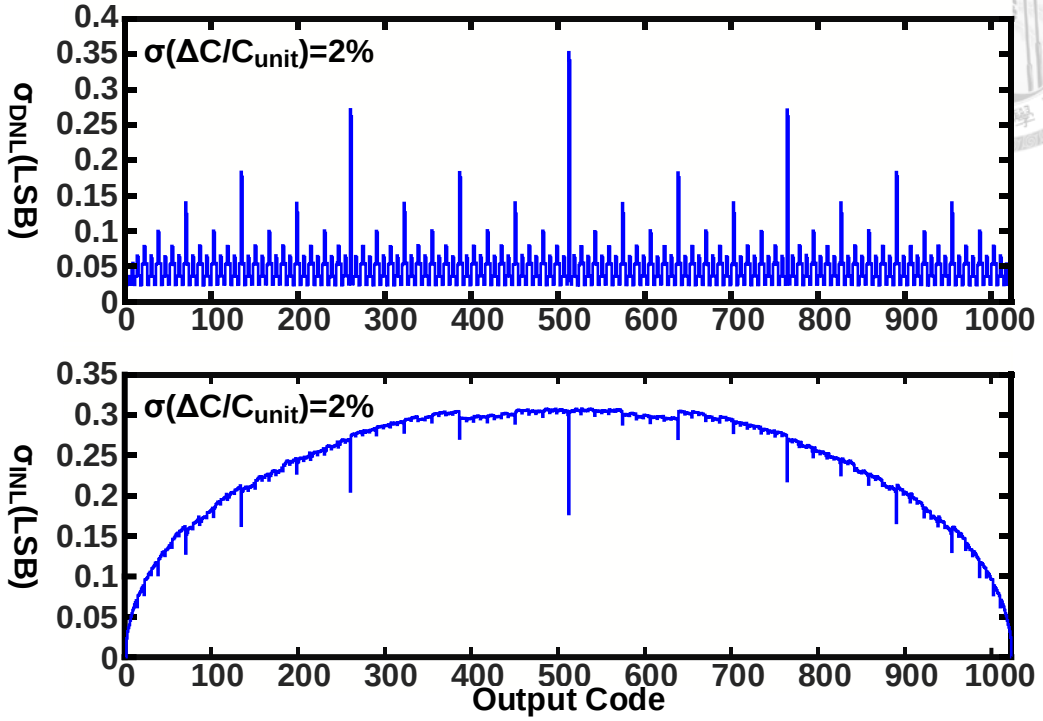

Fig. 6.16 MATLAB DNL (top) and INL (bot.) performance prediction with 2% standard deviation of unit-capacitance mismatch for 1000 times Monte-Carlo runs

Fig. 6.17 shows the dynamic performance prediction of the proposed SAR ADC with 2% mismatch in unit-capacitance. The mean ENOB in that prediction is 9.70, which is strongly match that result with SPICE simulation. Table 13 is the comparison table.

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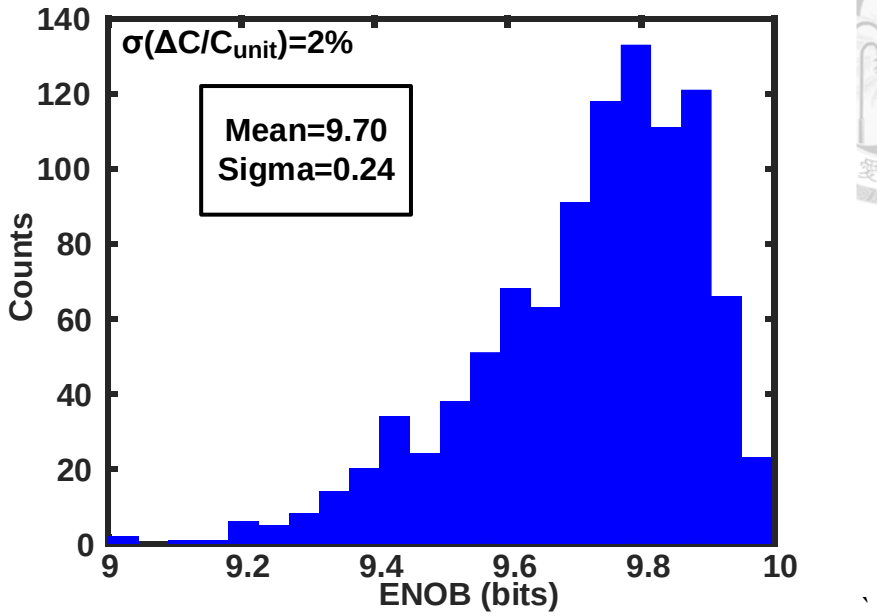

Fig. 6.17 MATLAB dynamic performance prediction with 2% standard deviation of unit-capacitance mismatch for 1000 times Monte-Carlo runs

Parameter	This Work	CICC'12 [41]	ASSCC'13 [25]	JSSC'15 [19]	JSSC'15 [22]	VLSI'17 [42]
Architecture	SAR	SAR	SAR	SAR	SAR	SAR
Process	90nm CMOS	65nm CMOS	40nm CMOS	28nm CMOS	20nm CMOS	14nm FinFET
Resolution(Bit)	10bit	10bit	10bit	10bit	10bit	12bit
Supply (Volt.)	0.9	1.2	0.8	1	1	0.85
Sample-rate (MS/s)	200	220	200	240	320	300
ENOB(bit)	9.26	8.3	9.2	9.19	9.14	9.75
Power(mW)	1.6	4.3	0.818	0.68	1.52	3.5
Active area (mm^2)	0.022	0.015	0.013	0.003	0.001	0.006
FoM (fJ/Conv.-step)	13	63	9.2	7.8	8.1	12.7

Table 13 Comparison table

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Chapter 7 Conclusions

In the last section of chapter 6, we summarized and predicted the dynamic performance of the proposed design due to static error source like mismatch in unit-capacitance and bond-wire parasitic inductance. However, in a real environment, circuit noise such as flicker noise and thermal noise should also take into consideration. Table 14 shows all the noise and error sources that contribute to ENOB degradation.

Part A: Design Parameter		
Parameter	Unit	Value
Input Frequency	Hz	9.92E+07
Resolution	bit	10
Reference Voltage	V	1.00E+00
Total Top-plate Sampling Cap.	F	5.05E-13
Total Top-plate Parasitic Cap.	F	1.09E-13
Comparator	F	1.54E-14
Sampling Switch	F	7.75E-15
Interconnection	F	4.35E-14
Shielding	F	4.20E-14
Full-Scale Swing,Vpp	V	1.65E+00
Part B: Noise Power Contribution		
Quantization Error, $\sigma^2_{\text{Quan.}}$	V^2	2.15E-07
Comparator Noise, $\sigma^2_{\text{Comp.}}$	V^2	1.59E-07
Sampling Error, σ^2_{jitter}	V^2	1.32E-07
Non-uniform Quantization Error, σ^2_{DNL}	V^2	7.04E-08
Reference Error, $\sigma^2_{\text{Ref.}}$	V^2	6.51E-08
DAC Switch Noise, σ^2_{DAC}	V^2	1.53E-08
BSW Noise, σ^2_{Sample}	V^2	1.35E-08
Part C: SNR & ENOB Calculation		
Total Noise Power	V^2	6.63E-07
SNR	dB	57.1
ENOB	Bit	9.19

Table 14 Noise and error table of the proposed design

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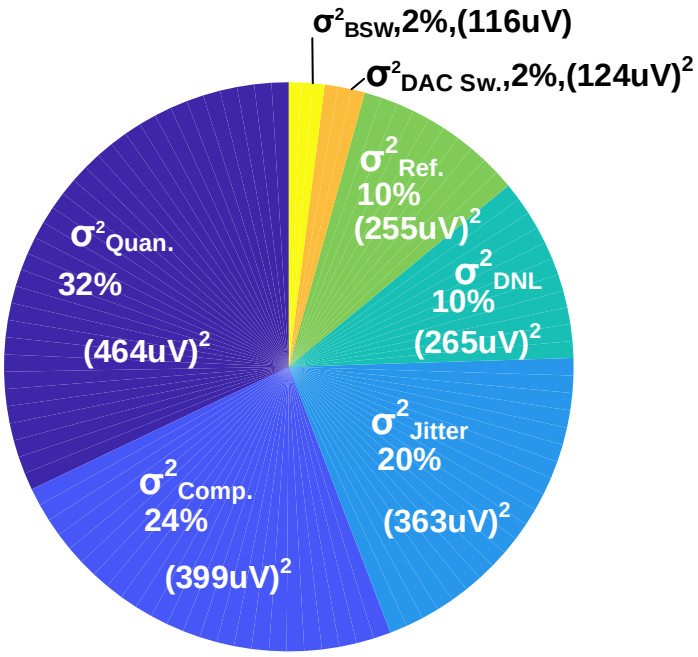
$$\mathrm{SNR_{NQ}} = 10\log\frac{\text{Signal Power}}{\sigma^2_{\text{Quan.}} + \sigma^2_{\text{DNL}} + \sigma^2_{\text{Comp.}} + \sigma^2_{\text{Jitter}} + \sigma^2_{\text{Ref.}} + \sigma^2_{\text{DAC Sw}} + \sigma^2_{\text{BSW}}} \quad (7.1)$$

Noise & Error Sources	σ(LSB)
$\sigma^2_{\text{Quan.}}$: Quantization Error	0.29
$\sigma^2_{\text{Comp.}}$: Comparator Noise	0.25
σ^2_{Jitter} : Sampling Jitter Induced Error	0.23
σ^2_{DNL} : Non-uniform Quantization Error,	0.17
$\sigma^2_{\text{Ref.}}$: Reference Regulator Error	0.16
$\sigma^2_{\text{DAC Sw.}}$: DAC Switch Noise	0.08
σ^2_{BSW} : BSW Noise	0.07



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