國立臺灣大學電機資訊學院電子工程學研究所

碩士論文

Graduate Institute of Electronics Engineering
College of Electrical Engineering & Computer Science
National Taiwan University

Master Thesis

應用於無線壓阻感測器之前端電路與超再生接收機設計

Design of Front-end Circuits and a Super-Regenerative Receiver for Wireless Piezoresistive Sensing Applications

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中華民國一百年十一月

November, 2011

國立臺灣大學碩士學位論文
口試委員會審定書

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本論文係蕭博允君（R98943027）在國立臺灣大學電子工程學研究所完成之碩士學位論文，於民國一百年十一月九日承下列考試委員審查通過及口試及格，特此證明

口試委員：

（指導教授）

系主任、所長

Design of Front-end Circuits and a Super-Regenerative Receiver for Wireless Piezoresistive Sensing Applications

By

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THESIS

Submitted in partial fulfillment of the requirement
for the degree of Master of Science in Electronics Engineering
at National Taiwan University
Taipei, Taiwan, R.O.C.

Nov. 2011

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To My Dear Family

致謝

兩年半的碩士生涯到此是告一個段落了。仔細想想這兩年多來的點點滴滴，有太多的酸甜苦辣值得慢慢回味，也有太多人值得我去感謝。

首先我要先感謝我的家人對我的支持，讓我可以在研究的生涯沒有後顧之憂。再來要感謝我的指導老師林宗賢博士。很感謝當初有機會能讓我在老師的研究團隊中逐步學習、成長。在平常研究時遭遇瓶頸，教授也會適時為我指引方向。並且在與教授的討論及報告中，我學習到做研究應有的態度和解決問題的方法、以及培養實事求是、自動自發的精神。

感謝口試委員李洪松博士、楊清淵教授與劉深淵教授抽空前來給我們指導，提供了許多論文、晶片實作與設計上的建議與經驗分享，讓我的論文能更臻於完善。

感謝 BL430 實驗室的大家。從我一開始進去時碰到的學長姐，包括博班學長 Mark 學長、豪哥、Jolin、Jack、Copa，以及 96 級的各個學長姊（奶哥、Mike、慧賢學姊、翔翔及丞諺），每個人都不吝於分享自己所學並願意將自己的經驗傳授給實驗室的後生晚輩。感謝之前畢業的 97 級學長姐們（A0、Zion、Jenwhite、小羅、以及小青蛙），你們不僅提供了我們許多寶貴的經驗與討論的對象、同時樹立了良好的典範。我要特別感謝 A0 學長，在一起做 DEMO 的時間裡，學到了很多東西，你的想法與態度都是我還需要學習的地方。感謝同屆的同學們，在碩一與阿廣一起下線的日子，松林的“我不行了”，D4 的科學人(ZZzzz…)，阿堅真的很厲害。從一起修課、一起熬夜下線等，累積了許多共同的回憶，你們也是平常討論時最主要的討論對象，畢竟有了一起努力的夥伴，會提升工作時的效能。也要感謝 99 級的學弟們，Kiwi 羽球進步神速，龍爺表示“小的榮幸”，Jeff 的 AOC 很強，必青與 Jamtu 認真的研究態度，你們從一進實驗室就展現出相當高的研究水準，並且為實驗室付出自己的心力不餘遺力。

還要感謝很多很多我的朋友、以及高中畢聯會的同學們。當我有需要的時候總是可以跟你們尋求協助，跟你們聊天與溝通的同時也可以消除壓力、使我重拾面對研究的勇氣。

摘要

本作品中實踐了一個應用於無線壓阻感測器之前端電路設計以及操作於四億赫茲且是低功率消耗之超再生接收機。

提出的應用於壓阻式感測器之前端電路中，採用一振盪器將電阻的資訊轉成頻率資訊，並使用一混頻器將頻率降頻到低頻做解調。降頻等效上為一時間上的放大器，讓系統對於電阻的靈敏度更好。為了在感測前讓混頻器的輸出頻率固定，振盪器從較高的頻率慢慢校正至與參考頻率固定的一頻率。此前端電路是使用台積電 0.35 微米製程設計，振盪器頻率設計為 24 MHz、校正後混波器輸出頻率為 100 kHz、整體消耗功率為 1 mW、電阻的靈敏度為 7 kHz/Ω。

提出的超再生接收機使用三角積分調變器的原理去解調接收到的訊號，以改善傳統解調器解析度收到參考時脈的限制。另外提出了一快速頻率校正的機制運用逐步逼近法的原理將接收機中振盪器的頻率在 12 個參考週期內校正到所想要的頻段，即 400 MHz。此接收機是使用台積電 0.18 微米製程設計，消耗功率為 1.35 mW、接收器的靈敏度為-50 dBm，當接收 1 Mbps 的訊號時，能源效益為 1.35 nJ/bit，頻率校正的時間為 250 ns。

Abstract

In this work, the front-end circuit and a 400-MHz super-regenerative receiver for piezoresistive sensing applications are implemented.

The proposed front-end circuit for piezoresistive sensor composes an oscillator to transfer the resistance information into frequency domain and a mixer to down-convert the frequency to lower frequency for digitizing the resistance information. The down-conversion operation is an amplifier in time domain which can increase the system sensitivity to resistance variation. To calibrate the output frequency of mixer before sensing, the oscillation frequency is tuned from the maximum frequency to fix the difference with the reference frequency. The front-end circuit is fabricated in a TSMC 0.35-μm CMOS technology. The oscillation frequency is 24 MHz; the output frequency of mixer is 100 kHz. The total front-end circuit consumes 1 mW with 3-V supply. The system sensitivity is 7 kHz/Ω.

The proposed super-regenerative receiver adopts the theorem of delta-sigma modulator to demodulate the received signal to improve the limitation of the conventional demodulator. A fast frequency calibration is also proposed by the meaning of SAR algorithm to regulate the oscillation frequency to the specific frequency band, 400 MHz. The receiver is fabricated in TSMC 0.18-μm CMOS technology. It consumes 1.37 mW with 1-V supply. The system sensitivity is -50 dBm. The energy efficiency is 1.37 nJ/bit with 1-Mbps input signal. The calibration time is 250 ns.

Contents

Chapter 1 Introduction **1**

1.1 Motivation 1
1.2 Thesis Overview 3

Chapter 2 Design and Implementation of a Front-end Circuit for Piezoresistive Sensing Applications **4**

2.1 Introduction 4
2.2 The Proposed Front-end Circuit Architecture 5
2.3 Circuit Implementations 8
2.3.1 Sensor-merged Ring Oscillator 8
2.3.2 Mixer and F-to-D Converter 14
2.3.3 Frequency Calibration Controller 16
2.4 Measurement Setup and Experimental Results 18
2.4.1 Measurement Setup 18
2.4.2 Experimental Results 20

Chapter 3 Introduction of a Super-Regenerative Receiver **24**

3.1 The Fundamental of SR-RX 24
3.1.1 Linear Mode 24
3.1.2 Logarithmic Mode 25
3.1.3 Self-Quenching Mode 26
3.1.4 Comparison 27
3.2 The Generic architecture of SR-RX 27
3.2.1 Mathematical Analysis of SR-RX 29
3.2.2 Conventional Demodulator of SR-RX 31
3.3 Summary 33

Chapter 4 Design and Implementation of SR-RX with ΔΣ-PWD and Fast Frequency Calibration **34**

4.1 Introduction 34
4.2 The Proposed SR-RX Transmitter Architecture 34
4.3 Design Considerations and System Analysis 35
4.3.1 Delta-Sigma Pulse-width Digitizer (ΔΣ-PWD) 36
4.3.2 Fast Frequency Calibration 39

4.4 Circuit Implementations 44
4.4.1 Low Noise Amplifier and Digital-controlled Oscillator 44
4.4.2 Envelope Detector and Limiting Amplifier 46
4.4.3 Charge Pump and Integration Capacitor 48
4.4.4 Circuits Implementations in Fast Frequency Calibration 49
4.5 Measurement Setup and Experimental Results 51
4.5.1 Measurement Setup 51
4.5.2 Device-Under-Test Print-Circuit Board 52
4.5.3 Experimental Results 53

Chapter 5 Conclusions and Future Works **59**

5.1 Conclusions 59
5.2 Future Works 59

References **62**

List of Figures

Fig. 1.1 Architecture of SoC for wireless piezoresistive sensing applications..... 1

Fig. 2.1 Architecture of microcantilever for DNA detection. 4

Fig. 2.2 Conventional way for resistance variation detection architecture (a) bridge architecture (b) current sensing architecture. 6

Fig. 2.3 Proposed DNA detection architecture. 6

Fig. 2.4 Operation of down-conversion. 7

Fig. 2.5 Sensor-merged ring oscillator. 9

Fig. 2.6 Simulation result of different cases. 12

Fig. 2.7 Simulation result of oscillation frequency vs. sensing resistor. 13

Fig. 2.8 The transfer curve of oscillation frequency vs. digital control code. 14

Fig. 2.9 Mixer and F-to-D converter. 15

Fig. 2.10 Simulation result of frequency pulling. 16

Fig. 2.11 Frequency calibration architecture. 17

Fig. 2.12 Simulation result of frequency calibration. 18

Fig. 2.13 (a) SoC architecture (b) Chip photograph. 19

Fig. 2.14 Measurement setup. 20

Fig. 2.15 Temporal responses of frequency variation for match and mismatch DNA conditions. 21

Fig. 2.16 Temporal responses of frequency variation for match DNA with different concentrations. 22

Fig. 3.1 Operation of linear mode SR-RX. 25

Fig. 3.2 Operation of logarithmic mode SR-RX. 26

Fig. 3.3 Operation of self-quenching mode SR-RX. 26

Fig. 3.4 Comparison of three mode operation. 27
Fig. 3.5 (a) Generic SR-RX architecture (b) Timing diagram of SR-RX 28
Fig. 3.6 The parallel LC tank 29
Fig. 3.7 (a) Conventional demodulator architecture (b) operation principle of demodulator 32
Fig. 4.1 The proposed SR-RX architecture. 34
Fig. 4.2 (a) The ΔΣ-PWD architecture (b) Linear model. 36
Fig. 4.3 Output spectrum of ΔΣ-PWD in MATLAB simulation. 38
Fig. 4.4 System operation of SR-RX. 39
Fig. 4.5 The architecture of fast frequency calibration 40
Fig. 4.6 Operation timing diagram of the proposed architecture. 43
Fig. 4.7 Circuit topology of LNA and DCO. 44
Fig. 4.8 Simulated frequency cover range of DCO. 45
Fig. 4.9 (a)Conventional envelope detector (b)Presented envelope detector (c)Simulated waveform of envelope detector. 47
Fig. 4.10 Limiting amplifier. 48
Fig. 4.11 Charge pump and integration capacitor. 49
Fig. 4.12 (a) Dual phase detector (b) Charge pump (c) Operation waveform. 50
Fig. 4.13 Measurement setup 51
Fig. 4.14 Chip micrograph 52
Fig. 4.15 PCB for SR-RX testing 53
Fig. 4.16 (a) Measured DCO output frequency, before and after frequency calibration. (b) Measured calibration time 54
Fig. 4.17 Spectrum at the ΔΣ-PWD output. 55
Fig. 4.18 (a) Measured output pulse-width vs. P_{IN} (b) Measured output pulse-width vs. input frequency. 56

Fig. 4.19 Transmitted and received data at 1 Mbps..... 57

Fig. 4.20 Measured bit error rate. 57

List of Tables

Table 2-1 Performance summary of the DNA detection SoC 23

Table 4-1 Design specifications 35

Table 4-2 Performance Summary 58

Table 4-3 Comparison table 58

Chapter 1

Introduction

1.1 Motivation

For today's society, the aging population makes the high demand of fully integrated healthcare system, such as the wireless physiological recording system that can collect a patient's health information and inform the doctor for emergency or the wireless diseases detection mechanism with the help of piezoresistive sensor to sense the existence of specific protein or DNA stream in patients' blood [1]-[3]. For these applications, high resolution front-end circuit and low-power radio-frequency (RF) topology are required.

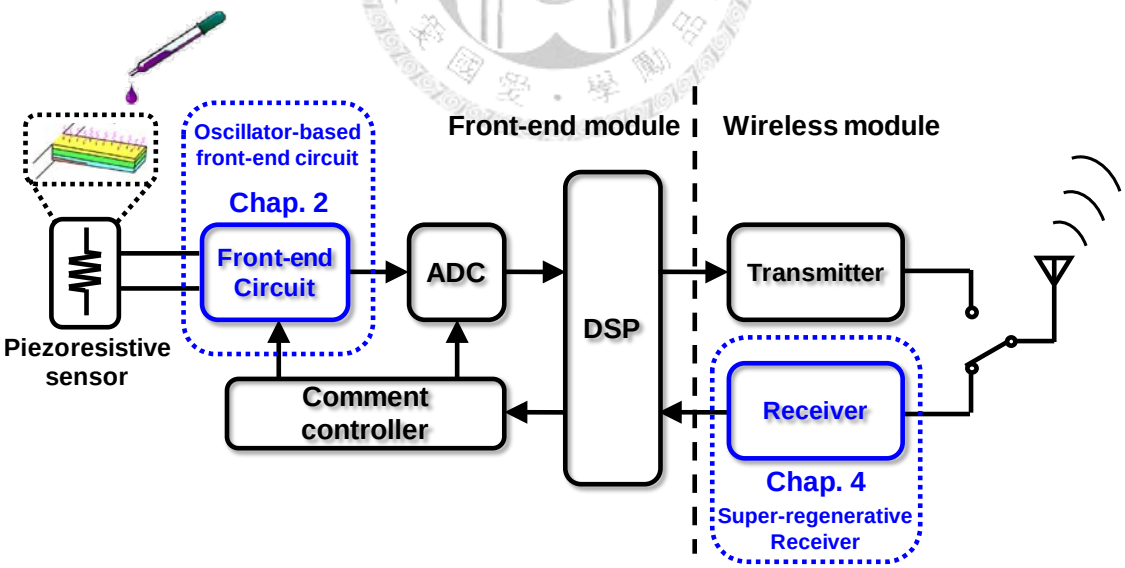


Fig. 1.1 Architecture of SoC for wireless piezoresistive sensing applications.

Fig. 1.1 shows the general architecture for a wireless piezoresistive sensor system. The front-end circuit and analog-to-digital converter (ADC) transfer the sensor

information into digital domain. The digital signal processor package digital output and transmit the signal to the external nodes. A receiver is used in the SoC for receiving command from the external controller to control the front-end circuit. This thesis focuses on the front-end circuit and the receiver design.

There are some existing architectures for piezoresistive sensor front-end circuit. However, in some applications such as DNA sensing, the resolution of the front-end resolution is critical design constrain for the small resistance variation. To meet the specific application of piezoresistive sensor, the design of front-end circuit is based on the DNA sensing application. The resistance variation in this application is much smaller than other applications. Hence, the resolution of the front-end circuit is the most critical part.

In many biomedical wireless modules, consuming much lower power to extend the life time is necessary for the system devices. For the low-power and high energy efficiency receiver, the design considerations of the receiver are summarized as follows:

1. The power consumption should be as low as possible, because of the limited power budget, and the inconvenience of changing battery.
2. The receiver should have minimum external devices for highly integrated system that can integrate the transceiver and front-end circuit together.
3. Reasonable data rates are demanded to transmit patient health data.
4. The start-up time of receiver must be as short as possible for the system power efficiency.

For such application scenarios, the super-regenerative receiver (SR-RX) is an appropriate candidate. The operation principle of the SR-RX has been widely

described in many literatures. The SR-RX is known for its hardware simplicity, short turn-on time, and high energy efficiency operation.

1.2 Thesis Overview

This thesis introduces a high sensitivity front-end circuit and a super-regenerative receiver with low power consumption and low energy efficiency operation.

In Chapter 2, the oscillator-based front-end circuit with self-calibration mechanism is presented. The system considerations about oscillator design and frequency calibration are addressed. Then the circuit implementations and measurement result are presented in detail.

In Chapter 3, the fundamental operation in super-regenerative receiver will be shortly addressed, followed by the introduction of the generic SR-RX architecture. In Chapter 4, the proposed SR-RX with ΔΣ-PWD and fast frequency calibration is presented with its design consideration. Then the circuit implementations and measurement result are presented in detail. Finally, the conclusions and future work of this thesis are described in Chapter 5.

Chapter 2

Design and Implementation of a Front-end Circuit for Piezoresistive Sensing Applications

2.1 Introduction

This chapter introduces an oscillator-based self-calibrated front-end circuit for DNA detection application with piezoresistive microcantilever. Next section introduces the design considerations with carefully analysis. Then the circuit implementations are presented. Followings are the measurement setup and experimental results.

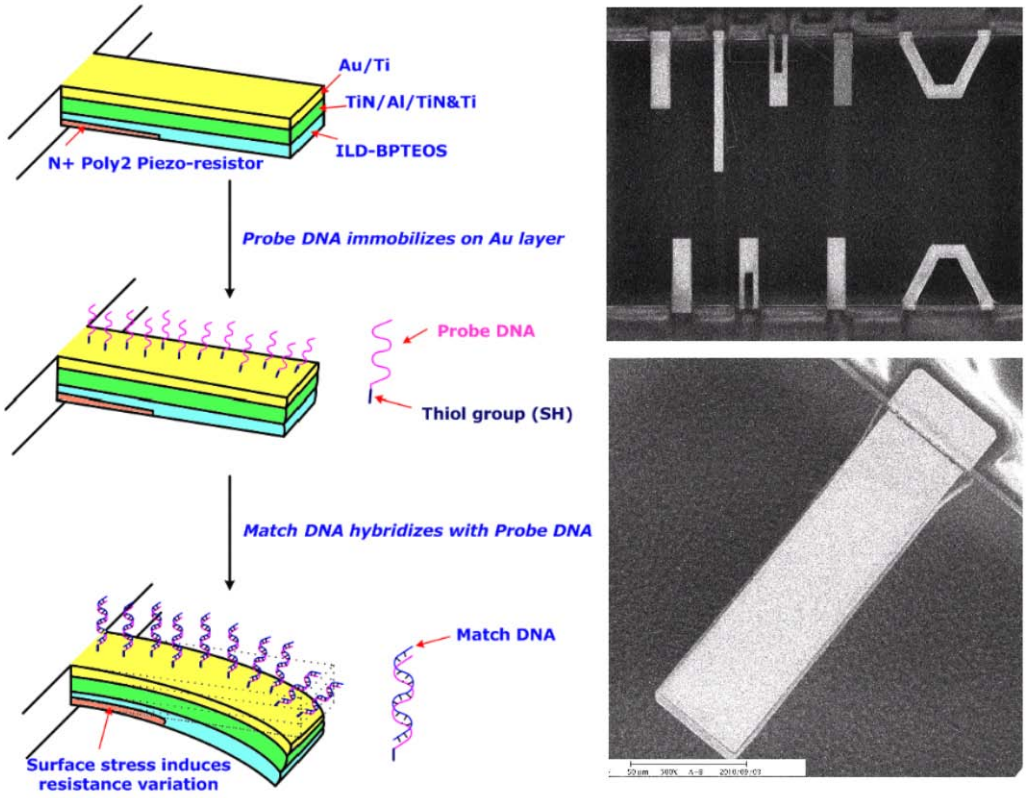
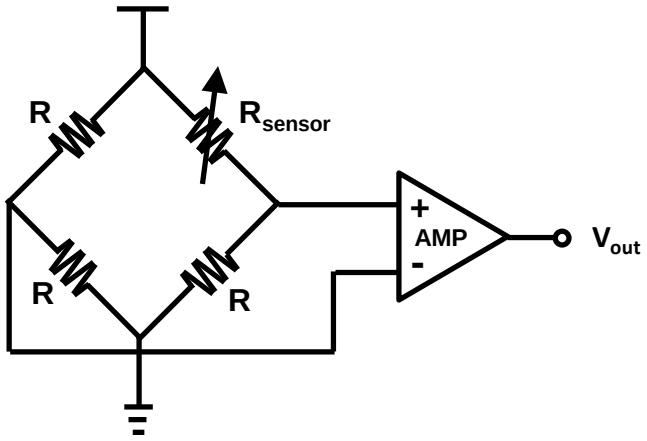


Fig. 2.1 Architecture of microcantilever for DNA detection.

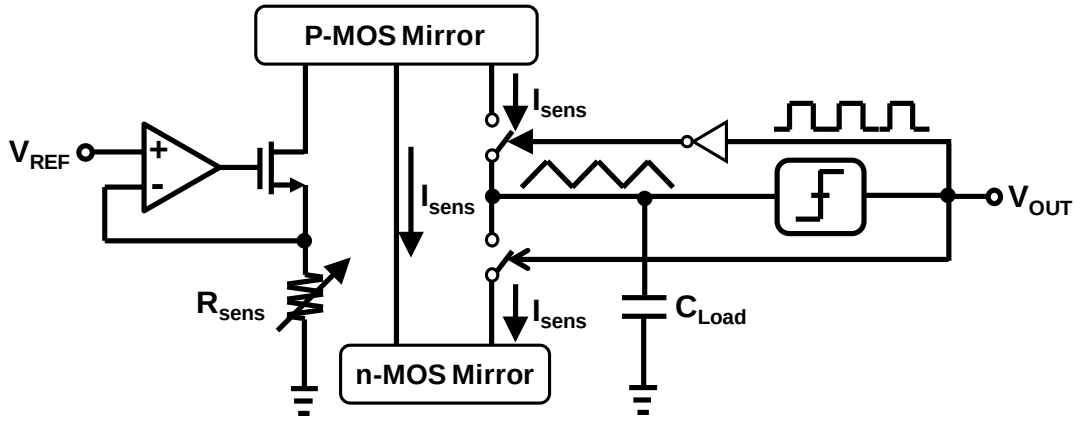
2.2 The Proposed Front-end Circuit Architecture

The main target for detecting the piezoresistive microcantilever is to separate the different equivalent resistance between the connections of probe DNA and target DNA as shown in Fig. 2.1. The probe DNA is the DNA that is used for experimental test. The target DNA is embedded on the microcantilever after post-processing [4][5].

After the probe DNA hybridizing with the target DNA because of the matching generic series, the cantilever may bend over and the equivalent resistance will change (increase or decrease may vary due to architecture and material). In this application, the resistance variation is as low as 0.02% of the original resistance. In the published papers, there are many way that are adopted to detect the resistance variation [6]-[8]. One conventional way to detect the variation of resistor may apply bridge topology which may suffer from the resistor offset problem as shown in [9] as shown in Fig. 2.2 (a). Another high dynamic range sensing topology by monitoring the current on the resistance can detect very wide range (140 dB) resistor variation [10][11] as shown in Fig. 2.2 (b). However, the resolution is not smaller enough to separate the tiny variation because of the limitation of clock frequency of the decoder that is used to transfer the resistance to digital code.



(a)



(b)

Fig. 2.2 Conventional way for resistance variation detection architecture (a) bridge architecture (b) current sensing architecture.

In this work, we proposed an oscillator-based self-calibrated topology as shown in Fig. 2.3. The system composes of an sensor-merged oscillator, a buffer, a divider, a mixer, a frequency to digital (F-to-D) converter, and a calibration controller.

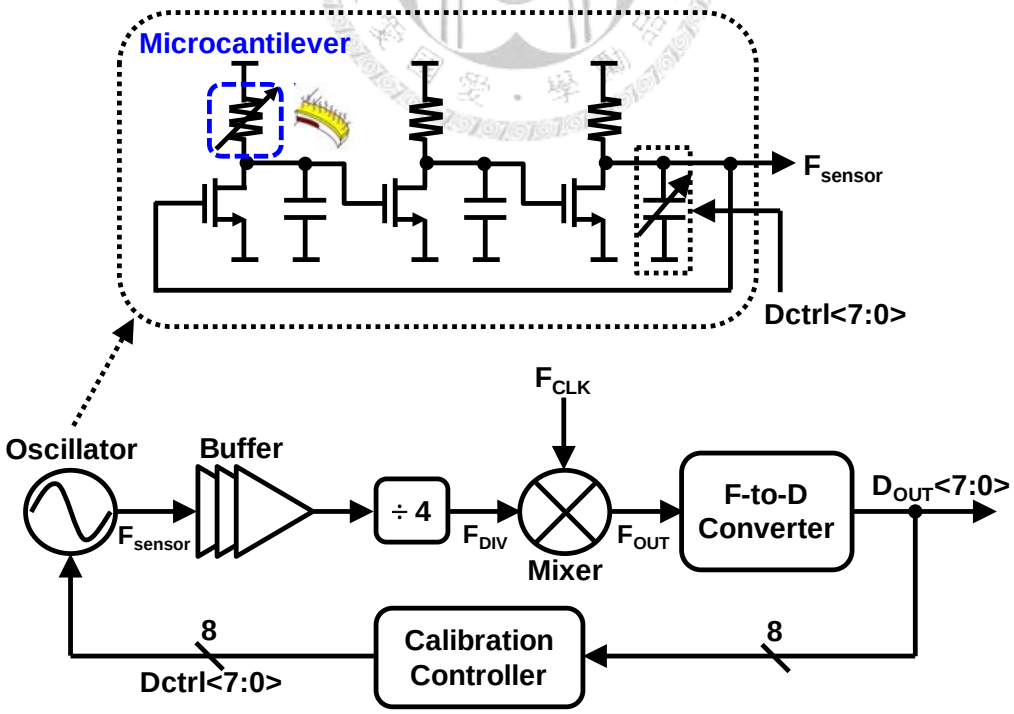


Fig. 2.3 Proposed DNA detection architecture.

The microcantilever is embedded in the ring oscillator whose frequency is decided by the three delay element with different time constant. The detail analysis with the oscillation frequency and the sensing resistance will be analyzed in the following section. The oscillation frequency is pull to rail-to-rail by an inverter buffer for the digital circuit. A divided by 4 block is connected at the output of the buffer which can make sure that the output clock is 50% duty cycle and to prevent the frequency-pulling due to the external clock F_{CLK} at another input of mixer. The mixer down-converts the frequency difference between F_{CLK} and F_{DIV} to the output frequency at F_{OUT}. Then the digital output can be obtained through the F-to-D converter to convert the output frequency to the digital code.

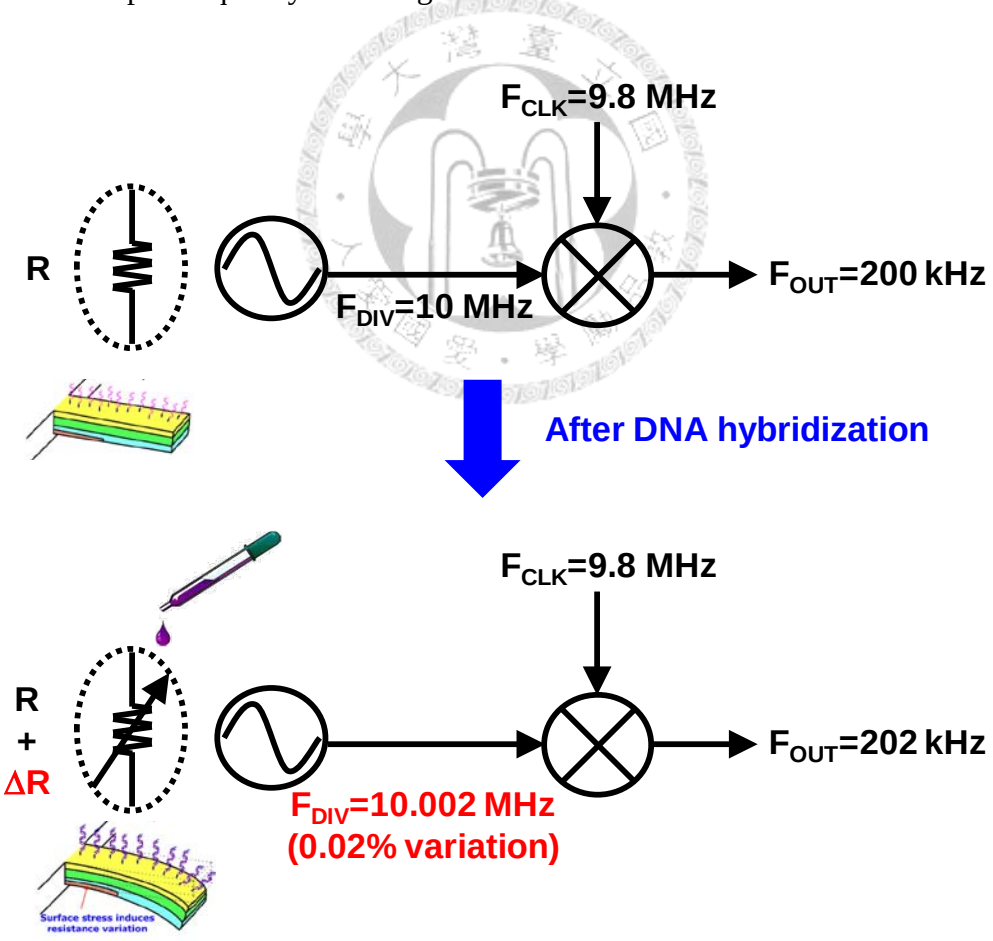


Fig. 2.4 Operation of down-conversion.

From this topology, the resistance variation is reflected by the output frequency of oscillator. The small variation that is caused by the resistance is amplified in the time domain due to the down-converter action. An example is shown in Fig. 2.4. The original frequency variation is 2 kHz. Compared with the oscillation frequency 10 MHz, the variation is hard to tell. Hence, the down-converter is designed to amplify the variation frequency in time domain. The output frequency is 200 kHz which is quite smaller for the variation frequency to separate. The required resolution of the decoder is much relaxed to design.

The output frequency of the oscillator before sensing resistance is varied due to process, voltage, and temperature variation. Hence, a calibration loop must be added in the system that can calibrate the oscillation frequency. In the proposed system, a self-calibrated scheme is adopted for frequency tuning which will be told in detail later.

2.3 Circuit Implementations

The proposed oscillator-based self-calibrated front-end circuit is depicted in Fig. 2.3. The calibration controller is implemented by Verilog synthesis. The detailed circuit implementations are introduced next with simulation results.

2.3.1 Sensor-merged Ring Oscillator

As shown in the sensor merged oscillator is composed by three delay stages. The oscillation frequency is decided by three-stage time constant. Because of the system detection requirement, the frequency shift due to the resistance variation must be as large as possible. In circuit analysis, R_1=R_2, C_1=C_2, and three MOS is equivalent for simplicity. The following is three cases.

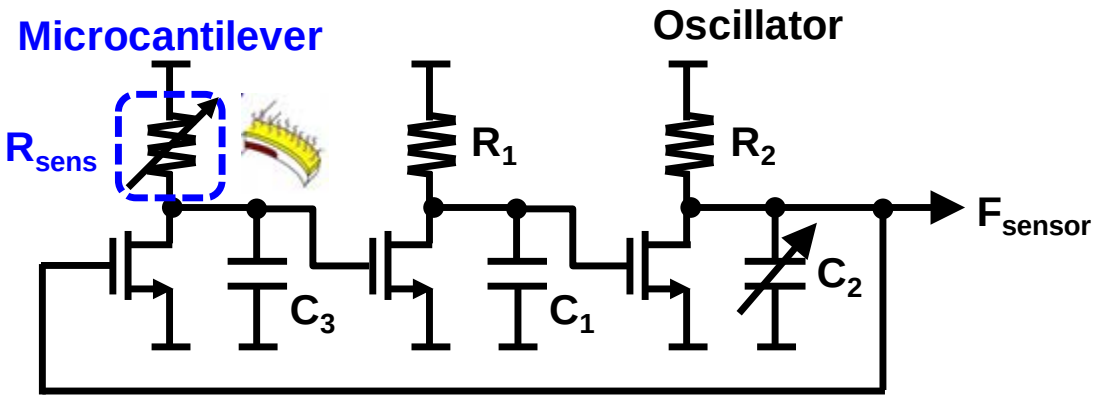


Fig. 2.5 Sensor-merged ring oscillator.

Case I: $R_{sens}C_3=R_1C_1$

From mathematical analysis, the loop gain of the oscillator can be obtained as

$$H(s) = -\frac{A^3}{\left(1+\frac{s}{\omega_0}\right)^3} \tag{2-1}$$

Where

$$\omega_0 = \frac{1}{R_1C_1} \tag{2-2}$$

The circuit oscillates when the phase shift of frequency dependent term equals 180°, that is the imaginary part of the loop gain is zero when s=jω. Then we can get the function

$$3\frac{\omega_{osc}}{\omega_0} - \frac{\omega_{osc}^3}{\omega_0^3} = 0 \tag{2-3}$$

And hence

$$\omega_{osc} = \sqrt{3}\omega_0 \tag{2-4}$$

To analyze the frequency drift due to the resistance variation, the assumption is made that Δω is the frequency shift due to the resistance change. Then from the equation (2-1) loop gain changes to

$$H(s) = -\frac{A^3}{\left(1+\frac{s}{\omega_0}\right)^2\left(1+\frac{s}{\omega_0+\Delta\omega}\right)} \approx -\frac{A^3}{\left(1+\frac{s}{\omega_0}\right)^2\left[1+\frac{s}{\omega_0}(1-\frac{\Delta\omega}{\omega_0})\right]} \quad (2\text{-}5)$$

By calculating the imaginary part of the loop gain, the oscillation frequency is shown as

$$\omega'_{osc} = \sqrt{3+\frac{2\Delta\omega}{\omega_0}}\omega_0 \approx \omega_{osc} + \sqrt{\frac{1}{3}}\Delta\omega \quad assume \ \frac{\Delta\omega}{\omega_0} \ll 1 \quad (2\text{-}6)$$

Which we can find out that the output frequency is a linear function of the small resistor drift coefficient Δω with a one over square root three constant slope.

Case II: $R_{sens}C_3$<R_1C_1

For the case that ω_{sens} is larger than the ω_0 the loop gain can be derived as

$$H(s) = -\frac{A^3}{\left(1+\frac{s}{\omega_0}\right)^2\left(1+\frac{s}{\omega_{sens}}\right)} \quad \omega_{sens} \geq \omega_0 \quad (2\text{-}7)$$

Calculate the oscillation frequency by making the imaginary part as zero

$$\omega_{osc}\left(\frac{1}{\omega_{sens}}+\frac{2}{\omega_0}\right)-\frac{\omega_{osc}^2}{\omega_0^2\omega_{sens}} = 0 \quad (2\text{-}8)$$

Rearranging the equation above that we can get the oscillation frequency

$$\omega_{osc} = \sqrt{\omega_0\left(\omega_0+2\omega_{sens}\right)} \quad (2\text{-}9)$$

As shown in Case I the oscillation frequency, to analysis the frequency drift due to the resistance shift the Δω is modeled as the variation.

$$H(s) = -\frac{A^3}{\left(1+\frac{s}{\omega_0}\right)^2\left(1+\frac{s}{\omega_{sens}+\Delta\omega}\right)} \approx -\frac{A^3}{\left(1+\frac{s}{\omega_0}\right)^2\left[1+\frac{s}{\omega_{sens}}(1-\frac{\Delta\omega}{\omega_{sens}})\right]} \quad (2\text{-}10)$$

By calculating the imaginary part of the loop gain, the oscillation frequency is shown as

$$\omega'_{osc} \approx \omega_{osc} + \sqrt{\frac{\omega_0}{\omega_0+2\omega_{sens}}}\Delta\omega < \omega_{osc} + \sqrt{\frac{1}{3}}\Delta\omega \quad (2\text{-}11)$$

From the equation that when the $\omega_{sens}>\omega_0$,the frequency slope with small resistor range is smaller than Case I.

Case III: $R_{sens}C_3>R_1C_1$

The pole of the sensor stage is assumed to be ω_{sens} that is much smaller than the other two stages. Followed by the analysis above, the loop gain of the oscillator is

$$H(s) = -\frac{A^3}{\left(1+\frac{s}{\omega_0}\right)^2\left(1+\frac{s}{\omega_{sens}}\right)} \qquad \omega_{sens} < \omega_0 \quad (2\text{-}12)$$

As calculated above

$$\omega_{osc} = \sqrt{\omega_0\left(\omega_0+2\omega_{sens}\right)} \quad (2\text{-}13)$$

As shown in Case I, to analysis the frequency drift due to the resistance shift the Δω is modeled as the variation.

$$H(s) = -\frac{A^3}{\left(1+\frac{s}{\omega_0}\right)^2\left(1+\frac{s}{\omega_{sens}+\Delta\omega}\right)} \approx -\frac{A^3}{\left(1+\frac{s}{\omega_0}\right)^2\left[1+\frac{s}{\omega_{sens}}(1-\frac{\Delta\omega}{\omega_{sens}})\right]} \quad (2\text{-}14)$$

By calculating the imaginary part of the loop gain, the oscillation frequency is shown as

$$\omega'_{osc} \approx \omega_{osc} + \sqrt{\frac{\omega_0}{\omega_0+2\omega_{sens}}}\Delta\omega > \omega_{osc} + \sqrt{\frac{1}{3}}\Delta\omega \quad (2\text{-}15)$$

From the equation that when the $\omega_{sens}<\omega_0$, the frequency slope with small resistor range is larger than Case I.

From the three cases above, to sum up, the RC design of the sensing stage should be larger than other stage. The simulation result is shown in Fig. 2.6. From the figure, the simulation result has the same tendency of our analysis above.

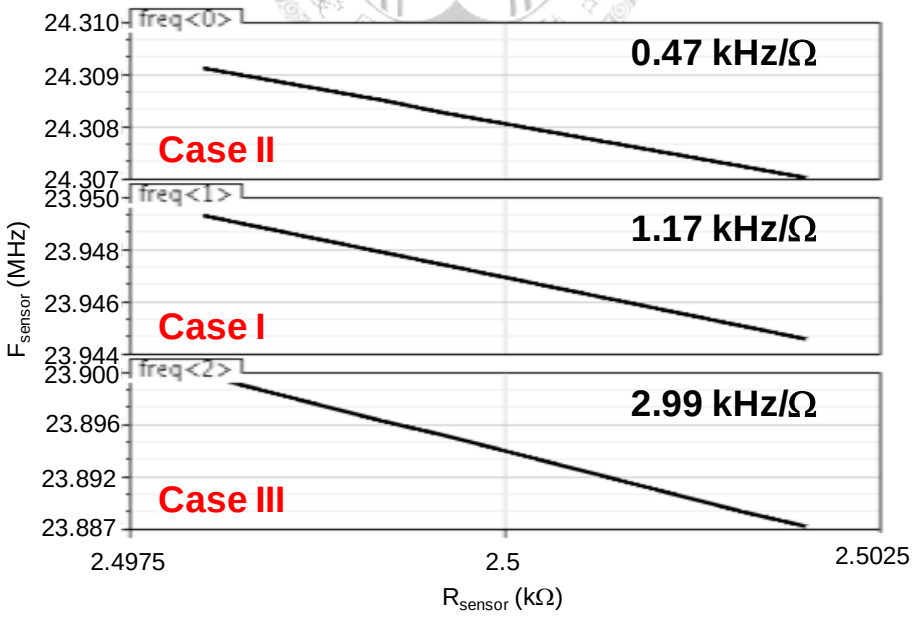


Fig. 2.6 Simulation result of different cases.

The phenomenon also can be explained in the large signal view. The ring oscillator can be viewed as feedback system with three delay cells with different time constant RC. Case I means that three delay cells contribute same delay time for the specific loop delay time. Case II means that the sensor stage with smaller RC time constant contributes less delay and the other two stages contribute more delay. On the other hand, Case III means that the sensor stage with larger RC time constant has more delay time than other two stages. For example, if the output frequency is 25 MHz, the loop delay should be 40 ns. For Case III, the sensor delay may contribute 20 ns while other two delay cells contribute 10 ns, respectively. The resistance variation reflects the time constant of the delay cell. Because that the sensor stage contributes large delay time, the variation of the time constant is also larger than that in Case II and Case I. Hence, the frequency slope versus the sensor resistance is largest in three cases.

After analyzing the RC design of each stage, the ring oscillator is designed with optimized output frequency slope, as shown in Fig. 2.7. The sensing resistor is designed to be 2.5 kΩ; the output frequency F_{sensor} is set to 24 MHz; the slope is 7 kHz/Ω. The resistance variation due to DNA hybridization can be as small as 0.02% of the sensing resistor. Hence, the output frequency drift is around

$$\Delta f = 7kHz/\Omega \times 2.5k\Omega \times 0.02\% = 3.5kHz \tag{2-16}$$

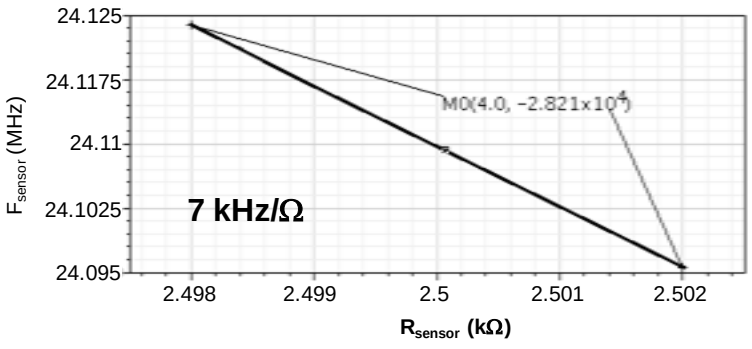


Fig. 2.7 Simulation result of oscillation frequency vs. sensing resistor.

Because of the PVT variation, the oscillation frequency is drifted away from the wanted frequency. The oscillator adopts the 8-bits capacitor array to regulate the output frequency. Fig. 2.8 shows the transfer curve of the oscillation frequency with different control bits.

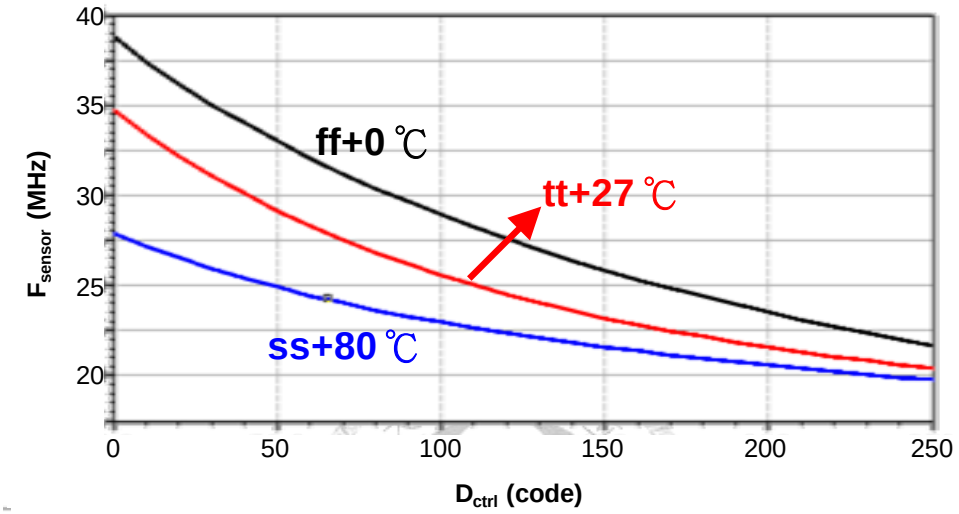


Fig. 2.8 The transfer curve of oscillation frequency vs. digital control code.

2.3.2 Mixer and F-to-D Converter

From the above analysis, it can be concluded that the output frequency variation due to DNA hybridization is 3.5 kHz. To separate the difference of oscillation frequency, the resolution of F-to-D converter must smaller than 3.5 kHz. As shown in Fig. 2.4, the operation of mixer amplifies the frequency difference on time-domain. The circuit implementations of the mixer and F-to-D converter are shown in Fig. 2.9.

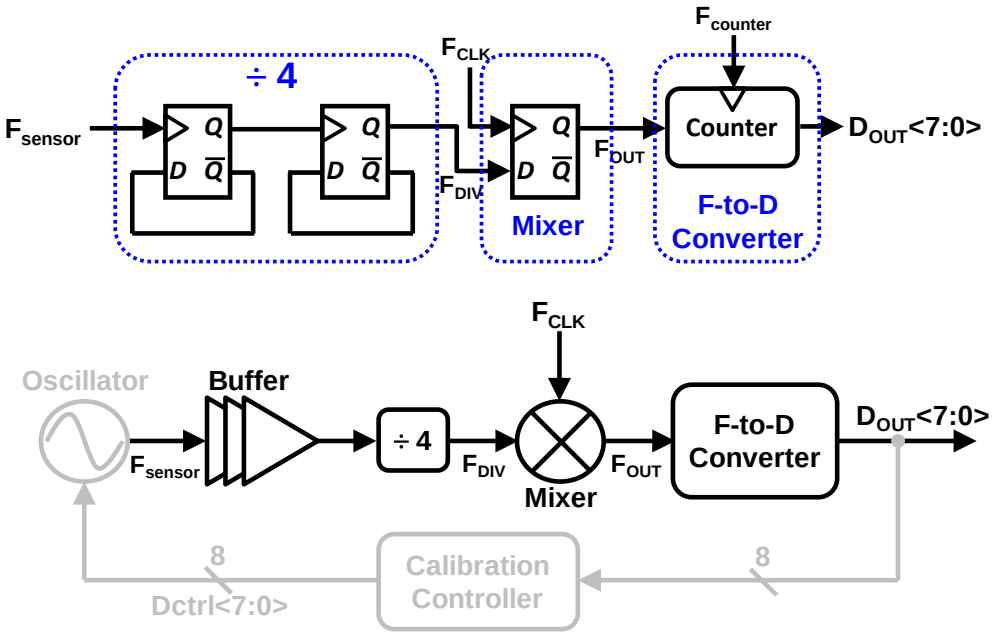


Fig. 2.9 Mixer and F-to-D converter.

The output of oscillator is send into a divided by 4 block to prevent frequency pulling between F_{CLK} and F_{sensor}. Because that F_{CLK} is given from instrument, the driving ability is stronger that the output of oscillation. Hence, when two frequency is very close, the oscillation frequency will be pulled to the frequency of F_{CLK}. Without the divider, the pulling range is about 30 kHz that may limit the detection range of DNA hybridization. With the divider to act as a buffer, the pulling range will be reduced to less than 5 kHz. The simulation result is shown in Fig. 2.10. A DFF is used to act as mixer. The divided signal F_{DIV} is sampled by the external clock F_{CLK} and the output frequency is the frequency of the subtraction of F_{DIV} and F_{CLK}. The F-to-D converter is a counter that transfers the period of the output frequency to digital code.

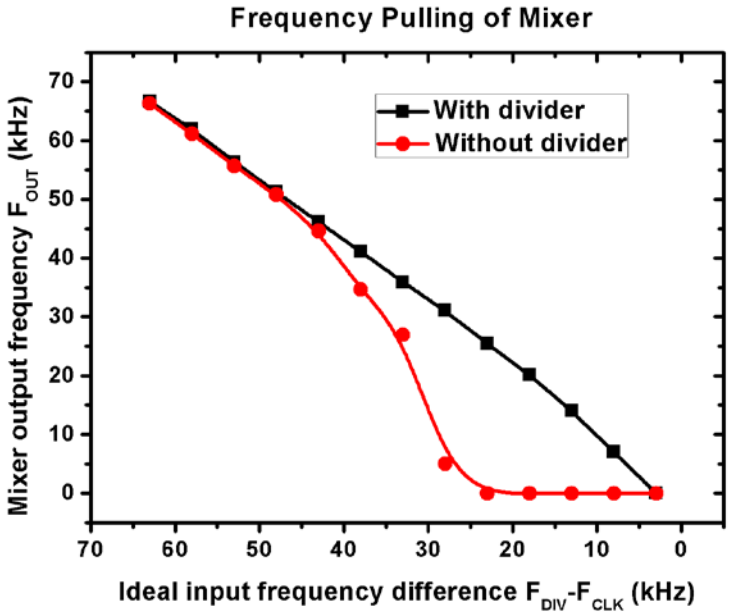


Fig. 2.10 Simulation result of frequency pulling.

The design of mixer output frequency F_{OUT} is based on the sensing resistor variation which causes 3.5 kHz frequency drift. If the F_{OUT} is designed too high, the time difference is hard to tell. For example, for F_{OUT}=500 kHz, after DNA hybridization, F_{OUT}=503.5 kHz. The period difference is 14 ns, which means that the counter clock $F_{counter}$ must larger than 71MHz. The clock rate is not practical for low-power design. Hence the F_{OUT} must be as low as possible. However, if the output frequency is too low, the frequency change will become too low that make the mixer output frequency very close to 0 Hz which will mistake the frequency information. In the presented system, F_{OUT} is designed to be 100 kHz. After DNA hybridization, F_{OUT}=103.5 kHz which means that counter clock $F_{counter}$ is larger than 3 MHz. Hence in our design, $F_{counter}$ is 5 MHz.

2.3.3 Frequency Calibration Controller

The ring oscillator for front-end sensing is sensitive to the PVT variation and the sensor resistance value which may vary due to post-process variation and the sensor

shape. Hence, a calibration scheme is required to establish the initial frequency before DNA hybridization. In the proposed calibration scheme the target frequency is based on the mixer output frequency F_{OUT}. The architecture is shown in Fig. 2.11. A 8-bit cap array with control signal D_{ctrl}<7:0> is added in ring oscillator to regulate the oscillation frequency. The initial value of D_{ctrl} is 0000000, which means the oscillation frequency is the maximum in tuning range. Output frequency is also the maximum if the F_{CLK} is fixed. A target digital code is stored in a register array to compare the output digital code of counter D_{sens} and the target digital code D_{Target}. The difference of the digital code is accumulated in another register that stores the control code D_{ctrl} to regulate oscillation frequency. Initially, F_{DIV} is larger than F_{CLK}. When calibrating, if F_{DIV} goes lower than F_{CLK}, the mixer frequency is still the difference of two frequencies with absolute value. Hence, the calibration scheme needs to make sure that the F_{DIV} won't go lower than F_{CLK} to prevent positive feedback.

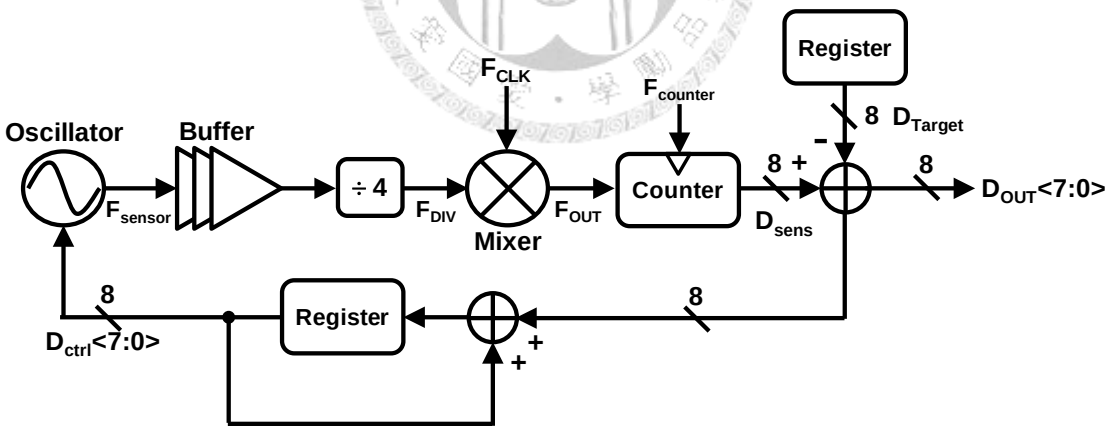


Fig. 2.11 Frequency calibration architecture.

From the Fig. 2.12, the simulation result shows that the operation of the frequency calibration. The upper graph is the decimal value of D_{ctrl}<7:0> that increases slowly to make the mixer output frequency close to the target frequency. The down graph shows the output waveform of mixer. At the beginning of calibration, the frequency of output

frequency is much higher than the target frequency 100 kHz. After frequency calibration, the output frequency of mixer can be calculated to be 98.4 kHz. The resolution of the calibration is acceptable.

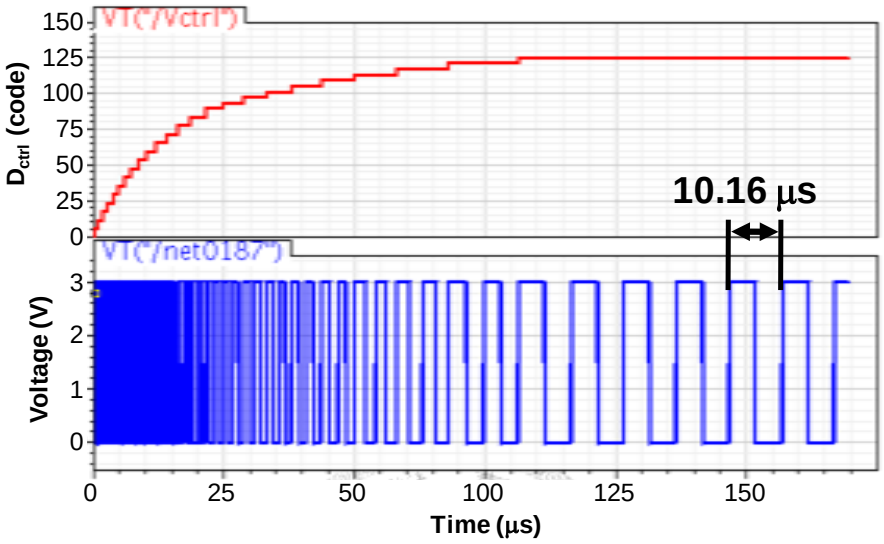


Fig. 2.12 Simulation result of frequency calibration.

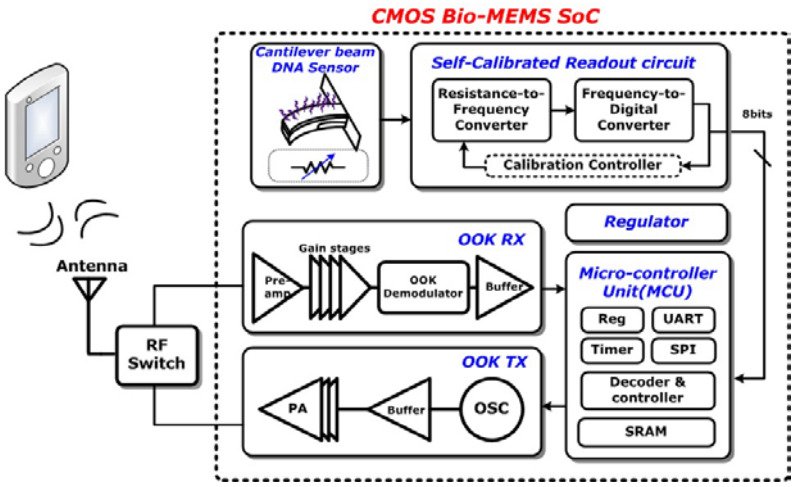
2.4 Measurement Setup and Experimental Results

This section presents the testing environment, including the instruments and component circuits on the PCB. The experimental results of the proposed circuit will also be presented.

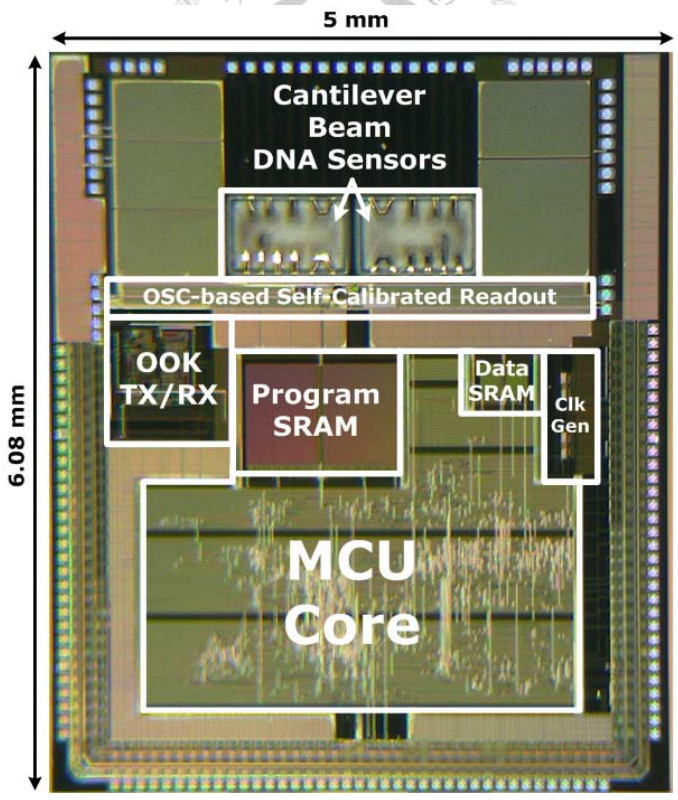
2.4.1 Measurement Setup

The chip is implemented in a 0.35-µm CMOS bio-MEMS process. The chip is originally designed for SoC that concludes DNA microcantilever with different shape (with the cooperation of Prof. Chih-Ting Lin and his research group), front-end circuit, and wireless RF module at back-end (with the cooperation of Prof. Shey-Shi Lu and his research group) as shown in Fig. 2.13(a). The chip photograph is shown in Fig.

2.13(b). The total chip area is occupied with 5 mm x 6.08 mm. The oscillator-based self-calibrated readout circuit occupies small area compared with other building block.



(a)



(b)

Fig. 2.13 (a) SoC architecture (b) Chip photograph.

The measurement setup is shown in Fig. 2.14. The mixer clock F_{CLK} and counter clock $F_{counter}$ is given by a function generator for different frequency. The output frequency of counter is monitored by oscilloscope to observe the output frequency variation.

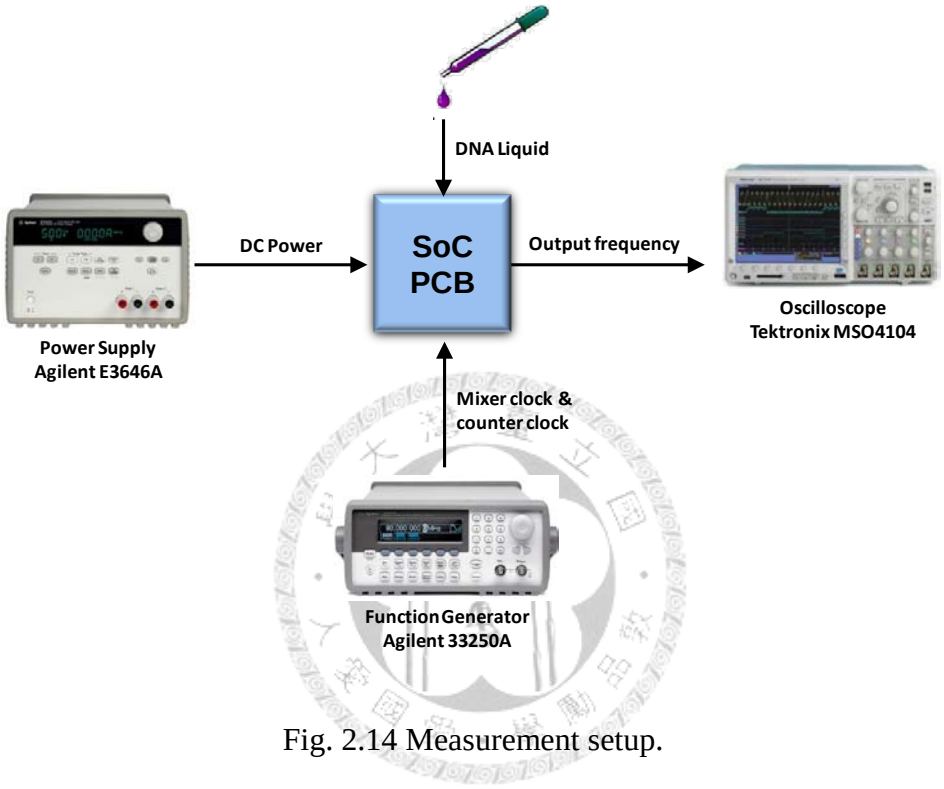


Fig. 2.14 Measurement setup.

2.4.2 Experimental Results

The measured characteristics of frequency variation versus time of the DNA SoC are shown in Fig. 2.15, where black squares and red circles represent match and mismatch DNAs, respectively. In these experiments, phosphate buffered saline (PBS) buffer is injected to initialize the DNA sensor. After the DNA sample injection and hybridization, unbinding DNAs are washed away by the PBS buffer. Finally, the sensing chamber is dried to obtain steady signals. Clearly, from Fig. 2.15, the difference of frequency-variation between match and mismatch DNA samples is 130 kHz. This result demonstrates unequivocally the sensing capability of the developed DNA SoC. It can be noted that there is 50 kHz frequency change in mismatch sample

which is resulted from the non-specific binding of mismatch DNAs. This non-specific binding phenomenon has the same effect in match DNAs experiments. Therefore, this shifting can be eliminated by post signal process.

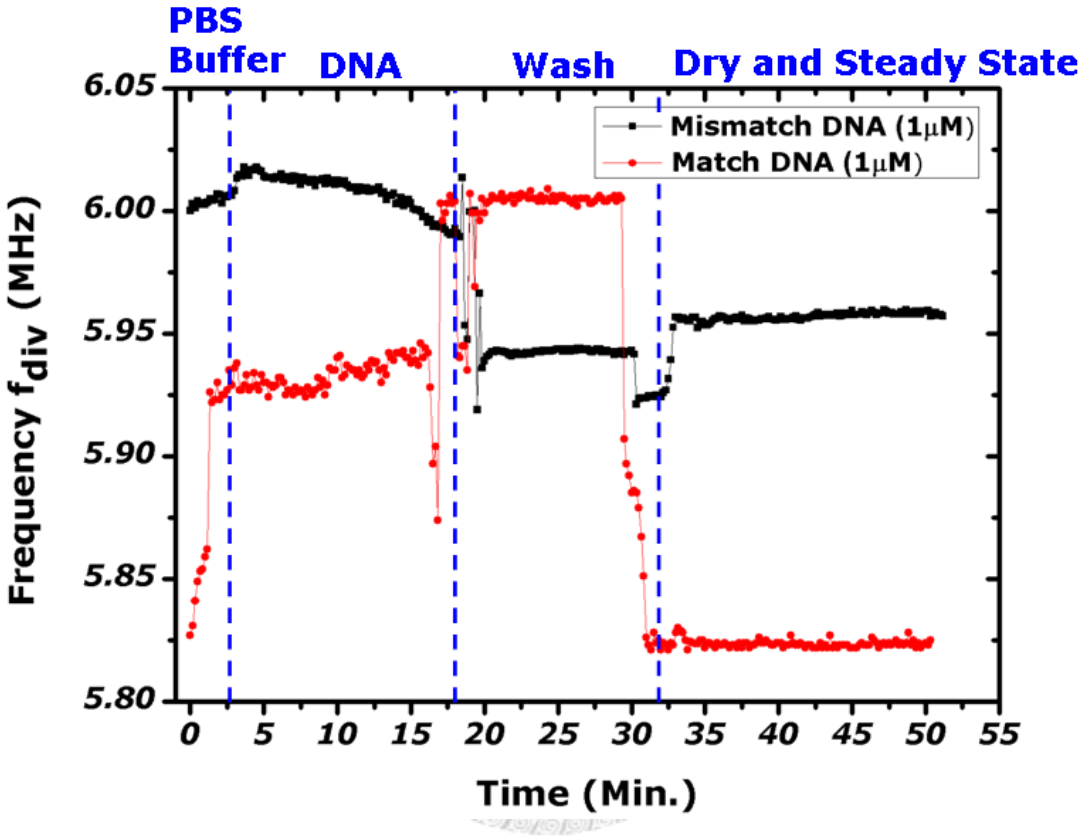


Fig. 2.15 Temporal responses of frequency variation for match and mismatch DNA conditions.

Fig. 2.16 shows the experimental result of match DNAs in different concentrations. The experimental protocol is the same as previous experiments but this experiment is designed to evaluate the sensitivity. In the graph, 200 kHz and 125 kHz frequency changes are induced by 1μM and 100 pM DNA, respectively. As a result, it presents an available detection range from 100 pM to 1 μM. This performance also demonstrates the developed DNA SoC is functional for most clinical applications.

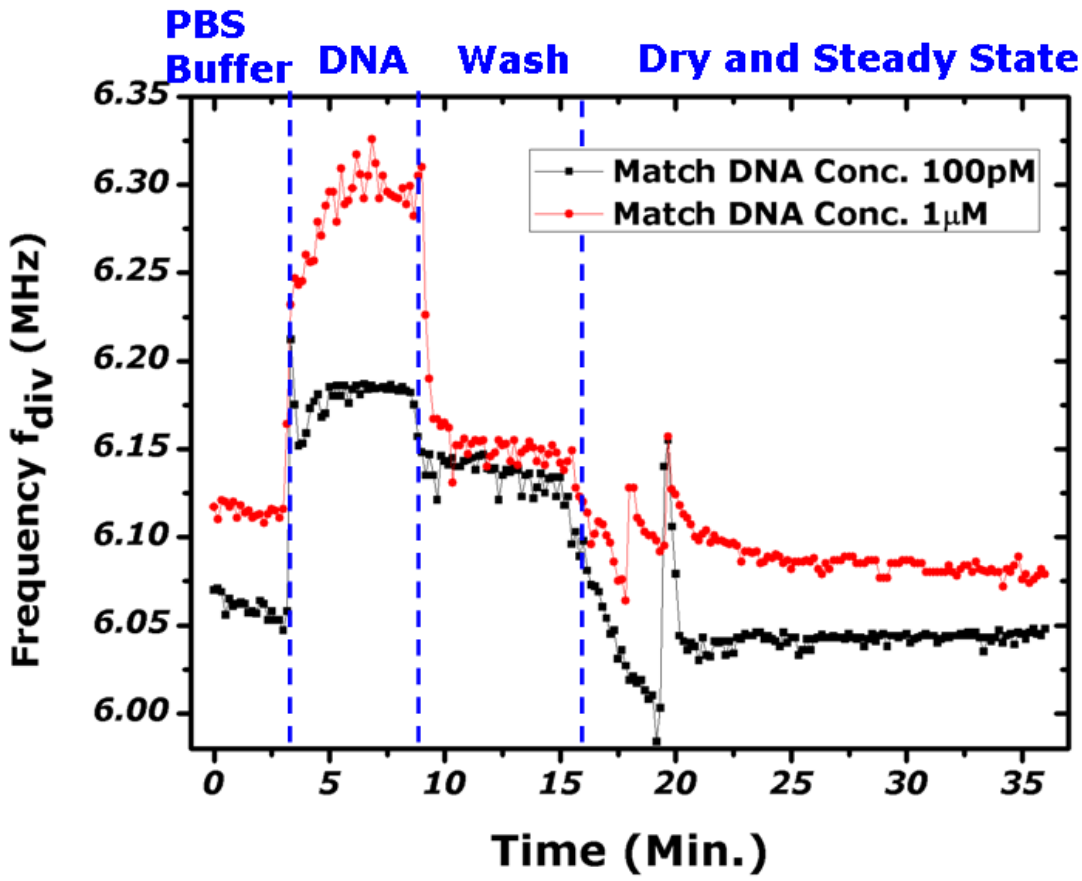


Fig. 2.16 Temporal responses of frequency variation for match DNA with different concentrations.

From the above measurement, the output frequency shift is larger than what we expected when designing system. To enlarge the detection range, the mixer output is set to 300 kHz for larger detection range. The measured frequency in Fig. 2.15 and Fig. 2.16 is the F_{CLK} plus the output frequency of mixer. However, because the digital circuit in calibration and the MCU shares the same power domain, the failure of SRAM implementation makes the supply node and ground node short. Hence, the calibration scheme is unable to measure.

Table 2-1 shows the summary table of the DNA detection SoC. The oscillation frequency is 24 MHz, the detection sensitivity is designed 7 kHz/Ω. The total front-end system consumes 1 mW with 3-V supply.

Table 2-1 Performance summary of the DNA detection SoC

Technology	TSMC 0.35μm Bio-MEMS CMOS
Chip Area	30.4 mm^2
DNA sensor	
Structure	Cantilever Beam
Dimension (length, wide, thickness)	180, 80, 1.5 (μm)
Resistance	2.5 kΩ
Self-calibrated Readout Circuit	
Power Consumption	1 mW @ 3 V
OSC Frequency	24 MHz
Detection Sensitivity	7 kHz/Ω
Digital Output Resolution	2 kHz/LSB
Resistance Resolution	< 0.02 %

Chapter 3

Introduction of a Super-Regenerative Receiver

3.1 The Fundamental of SR-RX

The SR-RX was invented by Armstrong in 1922. The main characteristics of the SR-RX are the low power operation and theoretically high front-end gain, which is suitable for demodulating amplitude-shift keying (ASK) and on-off keying (OOK) signal [12]. However the disadvantages of the SR-RX are bad frequency selectivity and requirement of high quality factor passive components [13][14]. However, for the biomedical applications, the power consumption is the most critical consideration in wireless system. The SR-RX is an appropriate candidate for this scenario.

The basic operation of super regenerative receiver is categorized into three modes: linear mode, logarithmic mode, and self-quenching mode. The following is going to introduce these three operation modes and analysis the pros and cons of each operation modes [15].

3.1.1 Linear Mode

The fundamental operation of SR-RX is based on the start-up time of oscillator which is influenced by the injected signal power. As shown in Fig. 3.1, the core circuit is an oscillator which is controlled by a signal called quench signal. When quench signal is high, the oscillator can start oscillation. When quench signal is low, on the other hand, the oscillator is turned off.

The start-up time of the oscillator is based on the amplitude of the injected signal from antenna. When the receiver receives ASK ‘0’, the oscillator need to spend more

time to start oscillation, while need less time to build oscillation when receives ASK '1'.

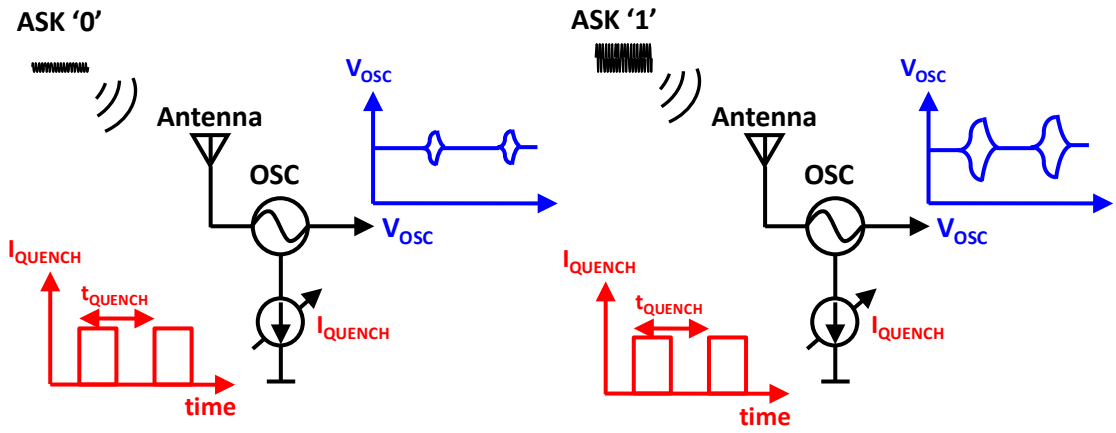


Fig. 3.1 Operation of linear mode SR-RX.

For linear mode operation, the oscillation built in a quench cycle is reset before the output voltage reaches saturation value. As shown in Fig. 3.1, when receiver detects ASK '1', the final voltage of oscillator is larger than the final value when receiver detects ASK '0'. For the demodulation of the linear mode operation SR-RX, ADC is required for separating the output voltage of oscillator which is hold before the quench signal goes down [16][17].

3.1.2 Logarithmic Mode

When receiver operates in logarithmic mode, the quench period is long enough that the oscillation value reaches saturation value before quench signal goes down as shown in Fig. 3.2. When the antenna receives ASK '0', because the start-up time depends on the injected signal, the pulse-width of oscillator is shorter. However, when receiving ASK '1', the output pulse-width is longer than that in receiving '0'. Hence, by comparing the pulse-width of the oscillator envelope, the receiver can separate the different input signal [18].

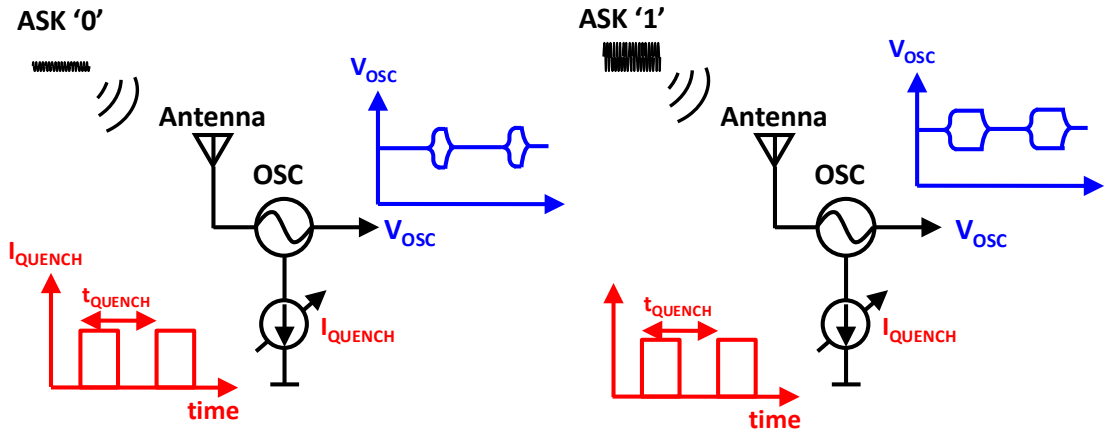


Fig. 3.2 Operation of logarithmic mode SR-RX.

3.1.3 Self-Quenching Mode

The self-quenching receiver operates somewhat differently. The quench signal is generated by the oscillator itself. From Fig. 3.3 that presents the operation principle of self-quenching mode, the appearance period of output pulse-width depends on the input signal power. When oscillation reaches a critical value, the quench signal turns down automatically, and turns on after a specific time. When receiving ASK '0', there are less pulse-width because the start-up time is longer. ASK '1' signal will cause the output pulse-width appears more than the ASK '0'. To demodulate the signal, a time-to-digital converter (TDC) is required for detect the output appearance period.

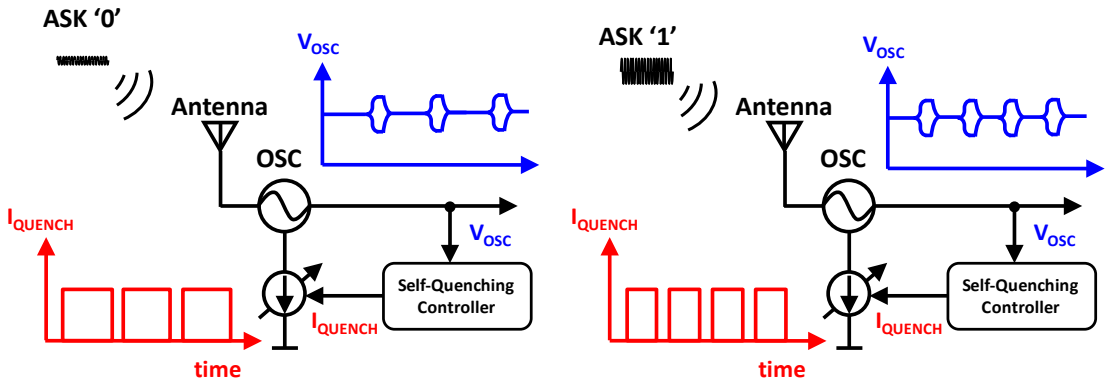


Fig. 3.3 Operation of self-quenching mode SR-RX.

3.1.4 Comparison

To summarize the difference between these three types of operation mode, the linear mode demodulator requires a ADC for separate the final value of the oscillation voltage. The logarithmic mode needs a counter to count the pulse-width while the self-quenching mode needs a TDC for demodulating data. However for high resolution ADC and TDC the power consumption will increase for high data rate. Hence, to reach low power operation the proposed SR-RX operates in logarithmic mode.

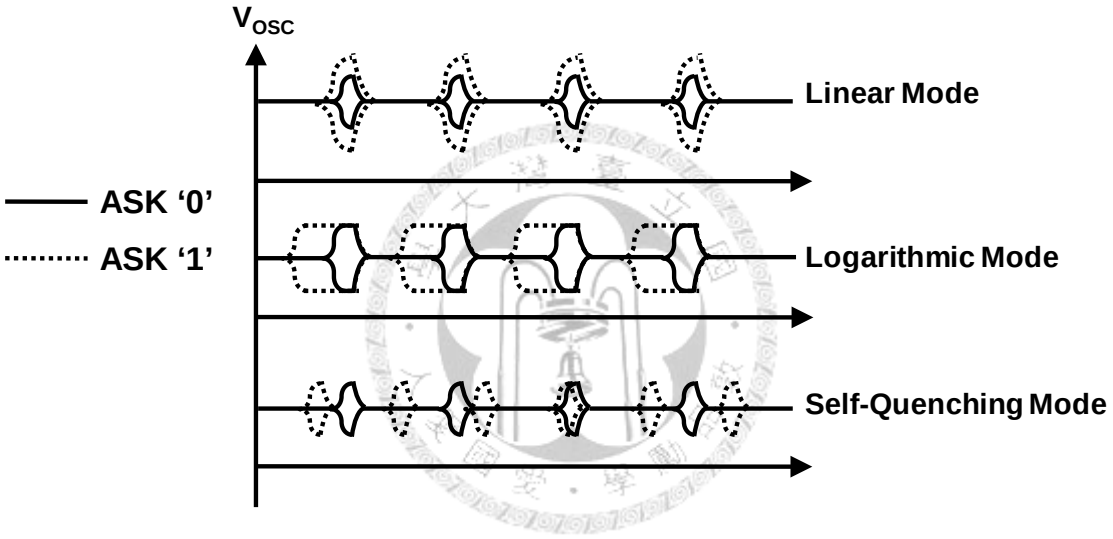
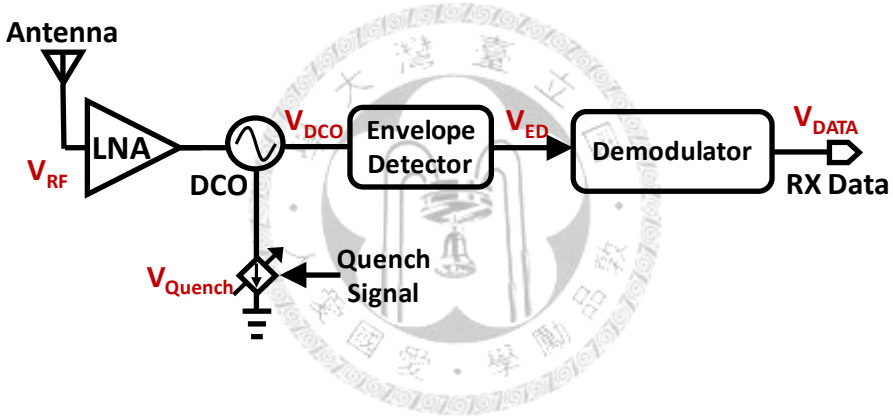


Fig. 3.4 Comparison of three mode operation.

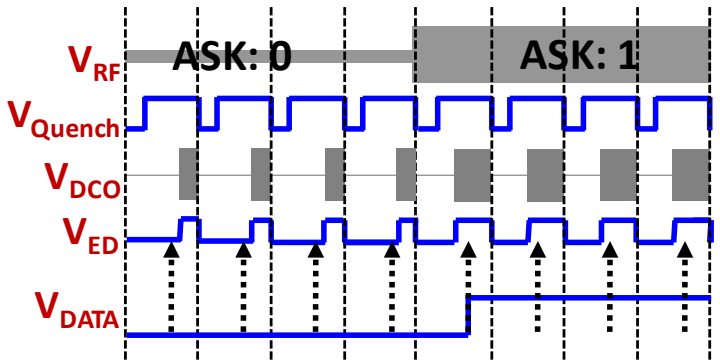
3.2 The Generic architecture of SR-RX

Currently, the generic SR-RX architecture can be shown in Fig. 3.5(a). It composes of front-end low noise amplifier (LNA), digital-controlled oscillator (DCO), envelope detector (ED), and demodulator. In some published papers, the system will add a frequency calibration loop for calibrating the frequency of DCO, which will be introduced later. To understand the operation of the SR-RX operation, it is shown in Fig. 3.5(b) which is the timing diagram of the SR-RX operation. The input signal V_{RF} is amplified by the LNA. The purpose of the LNA is to provide a signal at proper level

to the oscillator. Because DCO is periodically turned on and off by the quench signal V_{Quench} from the quench controller, the oscillations build up and decay periodically. The time for the oscillation grows up to a saturated level is the start-up time and it varies with the input signal level. That is, the input data is represented by the oscillation start-up time. When we receive ASK '0', it requires long start-time for DCO to reach a saturated level. But only need short start-up time for DCO to reach a saturated level when receiving ASK '1'. To get the information on the start-up time, an envelope detector is used to detect the envelope of the oscillator output. Then, a demodulator following the envelope detector recovers the base-band signal.



(a)



(b)

Fig. 3.5 (a) Generic SR-RX architecture (b) Timing diagram of SR-RX

Because of the direct relationship between the start-up time and the input signal power, the simple modulation of an on-off keying signal is suitable for the super-regenerative receiver. The connection between the start-up time and the input signal will be introduced next.

3.2.1 Mathematical Analysis of SR-RX

A fundamental process in the super-regenerative receiver is a successive build-up and decay of self-oscillations in the oscillator. To analyze the operation of the receiver, a simple equivalent circuit is used. The equivalent circuit is a parallel LC tank to model the DCO circuit as shown in Fig. 3.6 [19].

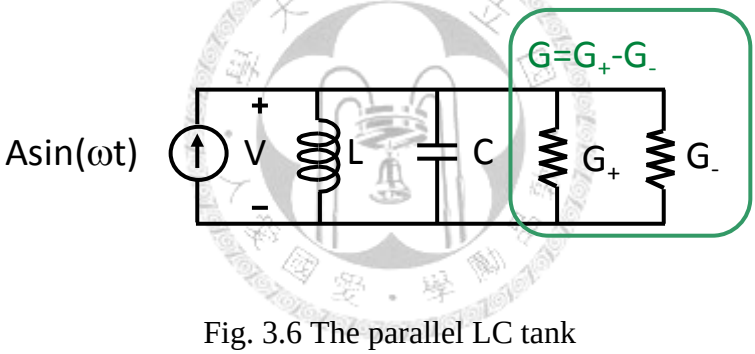


Fig. 3.6 The parallel LC tank

This circuit is composed of an inductor L, a capacitor C, and a conductance G which is composed of a positive conductance from loss of resonator and a negative conductance that is induced from the cross-coupled pair in oscillator. As shown in Fig. 3.6, the input signal is represented as Asin(ωt), where A is the amplitude of the input signal, ω is the frequency of the input signal, and V expresses the voltage across the parallel LC tank. The relationship between the voltage V and the input signal is what we are interested in. For the parallel LC tank, the quality factor can be expressed as

$$Q = \sqrt{\frac{C}{L}} \times \frac{1}{G} \tag{3-1}$$

And the magnitude of its impedance is

$$|Z| = \frac{1}{L} \cdot \frac{G/2C}{\sqrt{(G/2C)^2 + (\omega - \omega_0)^2}}, \tag{3-2}$$

where ω_0 is the resonant frequency. The voltage across the LC tank is the input signal multiplied by the impedance while the conductance G is positive. Furthermore, the transient expression for the voltage V should be examined. The equation of the voltage V across the LC tank is

$$C\frac{dV}{dt} + GV + \frac{1}{L}\int V dt = A\sin(\omega t) \tag{3-3}$$

By differentiating (2-3), (2-4) is derived

$$C\frac{d^2V}{dt^2} + G\frac{dV}{dt} + \frac{V}{L} = A\omega\cos(\omega t) \tag{3-4}$$

Solving (2-4) for V, we can get

$$V = k_1 e^{(-\alpha + j\omega_d)t} + k_2 e^{(-\alpha - j\omega_d)t} + \frac{A\sin(\omega t + \phi)}{\sqrt{G^2 + \left(\omega C - 1/\omega L\right)^2}} \tag{3-5}$$

$$\alpha = G/2C \tag{3-6}$$

$$\omega_d = \sqrt{\left(\frac{1}{LC} - \left(\frac{G}{2C}\right)^2\right)} = \sqrt{\left(\omega_0^2 - \alpha^2\right)}, \tag{3-7}$$

Where α is the damping factor and ω_d is the frequency of the damped oscillation. The first two terms in (2-5) are the free responses which are not affected by the input signal, and the third term is the forced response due to the input signal. Under these initial conditions,

$$V = 0 \text{ and } A\sin(\omega t) = 0, \tag{3-8}$$

The values of k_1 and k_2 can be solved. The resultant values of k_1 and k_2 are

$$k_1 = \frac{A\left[G\omega + \left(1/\omega C - \omega L\right)\left(-\alpha - j\omega_d\right)\right]}{2j\omega_d\left[G^2 + \left(1/\omega C - \omega L\right)^2\right]} \tag{3-9}$$

$$k_2 = -\frac{A\left[G\omega + \left(1/\omega C - \omega L\right)\left(-\alpha + j\omega_d\right)\right]}{2j\omega_d\left[G^2 + \left(1/\omega C - \omega L\right)^2\right]} \tag{3-10}$$

If the input frequency ω is equal to the resonant frequency ω_0, both the values of k_1 and k_2 are simplified to

$$k_1 = \frac{A\omega_0}{2j\omega_d G} \tag{3-11}$$

$$k_2 = -\frac{A\omega_0}{2j\omega_d G} \tag{3-12}$$

Therefore, (2-5) can be expressed as

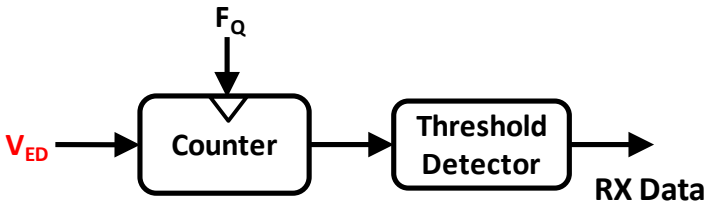
$$V = \frac{A}{G}\frac{\omega_0}{\omega_d}e^{-\alpha t}\sin\left(\omega t\right) + \frac{A\sin\left(\omega_0 t + \phi\right)}{G} \tag{3-13}$$

The first term is the major term in the super-regeneration, and the second term represents the steady state voltage produced by the input signal. If the damping factor α is negative, the first term increases exponentially, and is eventually larger than the steady-state voltage. Otherwise, if the damping factor is positive, the steady-state voltage dominates the voltage across the resonant circuit. In the SR-RX, the damping factor transits from positive to negative successively and this periodic shut-down of the oscillator is called quenching. Therefore, when the conductance is negative, the first term increases from an initial voltage which is the steady-state voltage. When the conductance is negative, the steady-state voltage determines the voltage across the LC tank.

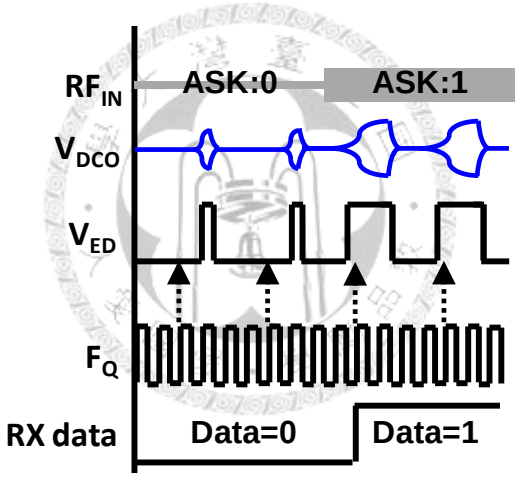
3.2.2 Conventional Demodulator of SR-RX

The demodulator for SR-RX that operates in logarithmic mode can be implemented in a simple digital circuit as shown in Fig. 3.7(a). The demodulator is required to separate the difference of the output pulse-width of envelope detector V_{ED}. To demodulate the signal, a counter with operation frequency F_Q is adapted to count the width of the output pulse-width [18]. After counting the pulse-width, a threshold

detector can decide the received signal based on the counted number. For larger pulse-width, the output code of counter is larger. Hence, the demodulated RX data is '1'. On the other hand, if the output code of the counter is less than the threshold, the demodulated RX data is '0'.



(a)



(b)

Fig. 3.7 (a) Conventional demodulator architecture (b) operation principle of demodulator

As shown in Fig. 3.7(b), the resolution of the demodulator is limited by the sampling frequency of counter F_Q. The time resolution can be derive as

$$\Delta_T = \frac{1}{F_Q} \tag{3-14}$$

Hence, to derive the pulse-width noise PSD of the conventional demodulator, the PSD can be derived as

$$S_{PW\_conventional} = \frac{\Delta_T^2}{12}\frac{1}{F_{Quench}} = \frac{1}{12(F_Q^2 F_{Quench})} \tag{3-14}$$

From the PSD we can summarize that the noise density is reduced only if the sampling frequency or the quench frequency increases. However, increasing the operation frequency of the demodulator will cause the power consumption increasing and the digital circuit complexity increasing.

3.3 Summary

This chapter introduced an overview of the basic principle of SR-RX. There are three operation modes: linear mode, logarithmic mode and self-quenching mode. The linear mode and self-quenching mode suffer from the complex demodulator and higher power consumption. In the generic operation of SR-RX, the logarithmic mode is an appropriate option for low power operation. The conventional demodulator of SR-RX is implemented by the counter with higher count frequency which will decide the quantization noise and resolution of demodulator. To improve the resolution will also increase the total power consumption of demodulator.

Chapter 4

Design and Implementation of SR-RX with ΔΣ-PWD and Fast Frequency Calibration

4.1 Introduction

This chapter introduces an SR-RX with ΔΣ-PWD and fast frequency calibration. At first, the receiver architecture is discussed. Next section introduces the design considerations with carefully analysis. Then the circuit implementations are presented. Followings are the measurement setup and experimental results.

4.2 The Proposed SR-RX Transmitter Architecture

The architecture of proposed SR-RX is shown in Fig. 4.1. The system comprises of front-end circuit, low noise amplifier (LNA) and digital-controlled oscillator (DCO), envelope detector (ED) and limiter amplifier (LM), a ΔΣ pulse-width digitizer (ΔΣ-PWD) for demodulator and a quench controller. The decimation filter is implemented in a FPGA board.

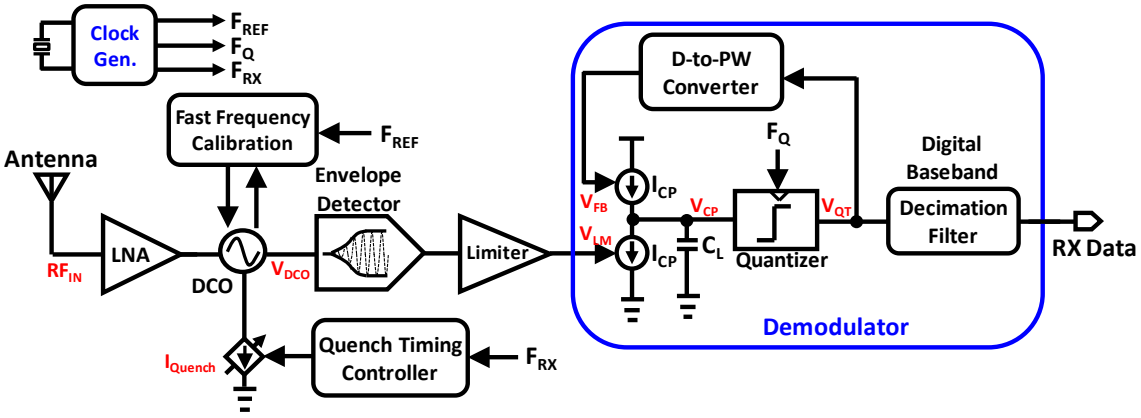


Fig. 4.1 The proposed SR-RX architecture.

The RF signal RF_{IN} is received by antenna. The LNA and DCO detect the power of received signal and is detected by separating the pulse-width of ED. The LM is used to amplify the ED output to rail-to-rail. Then the ΔΣ-PWD demodulates the received signal. The detail operation will be introduced in the following section. The system specifications are shown in Table 3-1.

Table 4-1 Design specifications

Process	TSMC 0.18-μm CMOS
Supply Voltage	1 V
Operating Frequency	400 MHz
Data Rate	1 Mbps
Sensitivity	<-75 dBm
Modulation	ASK/OOK
Power Consumption	< 1.5 mW
Energy Efficiency	< 1.5 nJ/b

4.3 Design Considerations and System Analysis

For the proposed SR-RX, the ΔΣ-PWD for demodulator can be viewed as the delta-sigma modulator in pulse-width domain. Taking advantage of oversampling and noise-shaping in ΔΣ modulator, the ΔΣ-PWD can achieve high resolution and lower quantization noise. To short the system start-up time of the receiver, the frequency calibration in DCO is necessary to regulate the operation frequency of DCO to the desired value. Hence, in the following, these two system design consideration will be described in detail.

4.3.1 Delta-Sigma Pulse-width Digitizer (ΔΣ-PWD)

The ΔΣ-PWD, which is shown in Fig. 4.2(a), comprises a charge pump, an integration capacitor, a quantizer, a digital to pulse-width (D-to-PW) converter, and a decimation filter which is implemented in FPGA. Compared with the conventional feed-back path to control the quench controller [20][21], the proposed ΔΣ-PWD controls the charge pump upper current source signal for system simplicity.

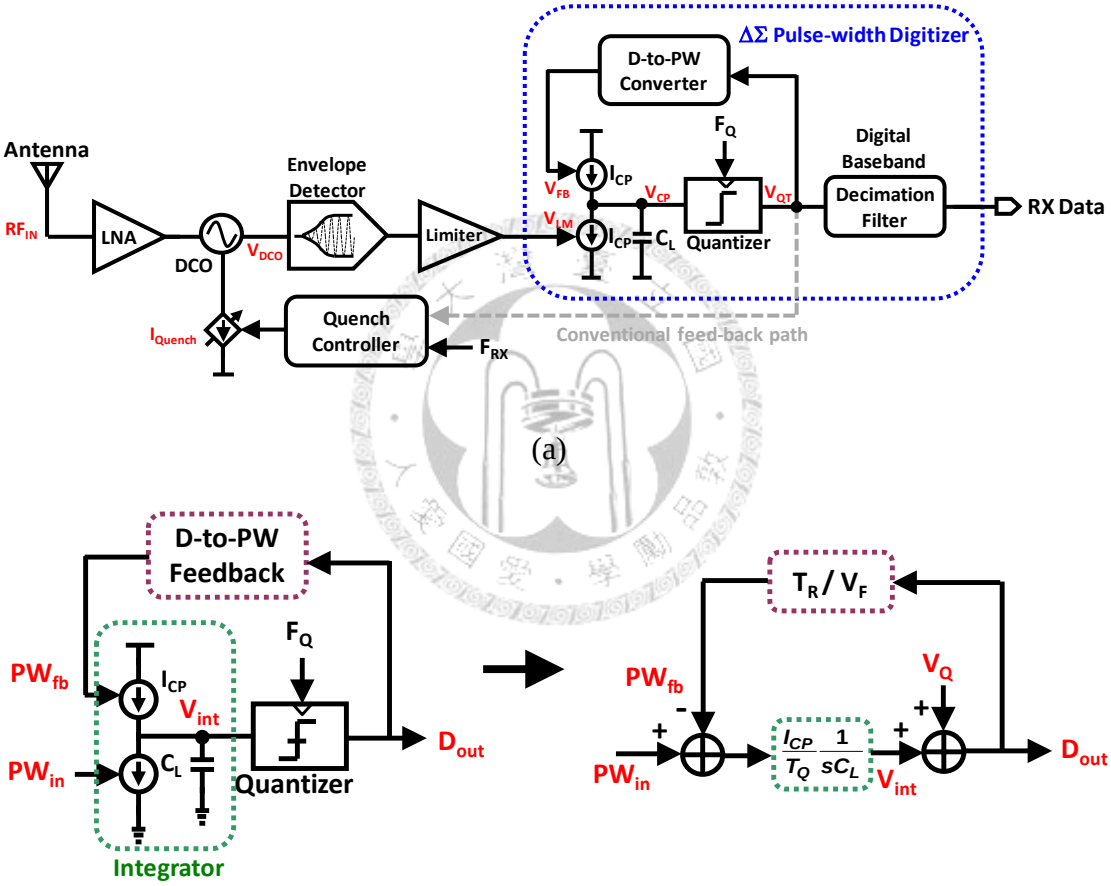


Fig. 4.2 (a) The ΔΣ-PWD architecture (b) Linear model.

To analysis the ΔΣ-PWD operation, the linear model of the demodulator is shown in Fig. 4.2(b). The input is the pulse-width from the limiter amplifier. To model charge pump and integration capacitor, T_Q is the quench period; I_{CP} is the current of the charge pump; C_L is the capacitor for integrator. To model the D-to-PW converter, T_R is

the feedback resolution and V_F is the full swing in quantizer output. To get the signal transfer function (STF) and noise transfer function (NTF) from quantizer, the transfer function between input pulse-width PW_{in} and D_{out} is

$$STF = \frac{\omega_L}{s+\omega_L}\frac{V_F}{T_R} \tag{4-1}$$

The transfer function between quantization noise and D_{out} is

$$NTF = \frac{s}{s+\omega_L} \tag{4-2}$$

Where

$$\omega_L = \frac{I_{CP}T_R}{C_L T_Q V_F} \tag{4-3}$$

From STF, The coefficient V_F/T_R is the domain transformation from voltage domain to time domain. In NTF, there is no that domain transformation. From the equation, the STF is a low pass filter that the signal in the bandwidth will have no effect. However, the low-frequency quantization noise will be noise-shaped by NTF with the high-pass characteristic.

From Fig. 4.3, the MATLAB simulation of the ΔΣ-PWD is shown. The parameter of the system is shown in below. I_{CP}=25 μA, T_Q=125 ns, T_R=31.25 ns, C_L=10 pF, V_F=1V. The simulation result can be found that the noise shaping in the in-band is 20 dB/dec. The total SNR is around 16 dB, which is good enough for OOK demodulator. The input signal is 010101… periodic signal with 500-kHz frequency which represents the OOK input signal with 1-Mbps data rate.

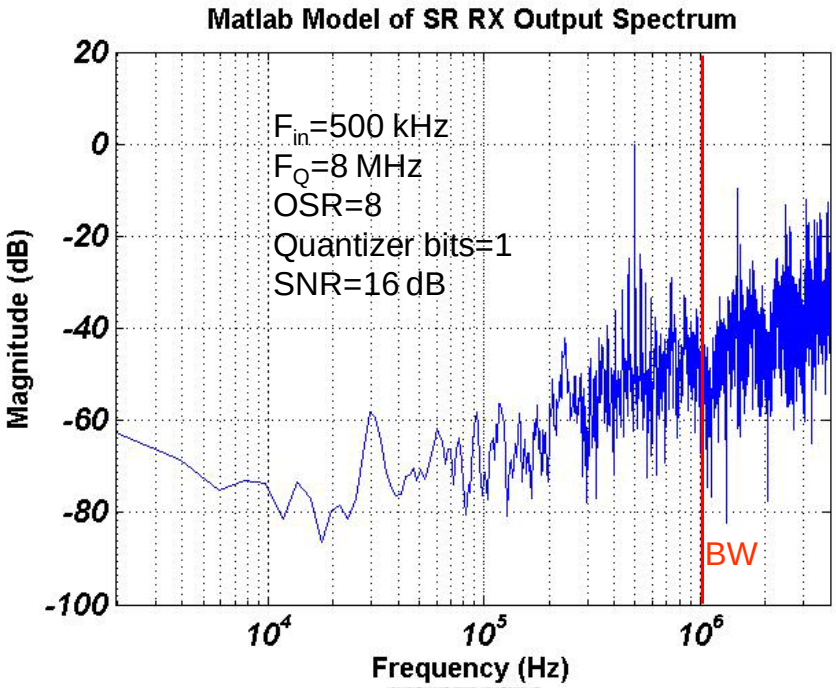


Fig. 4.3 Output spectrum of ΔΣ-PWD in MATLAB simulation.

The operation of the ΔΣ-PWD is illustrated in Fig. 4.4 (in the case of a 1-Mbps data rate, T_{DATA} = 1 μs). At 8× oversampling rate, the quantizer is clocked at 8 MHz, i.e. T_Q is 125 ns. Subsequently, T_R is 31.25 ns. I_{Quench} current pulse-width is $0.75T_Q$ which is 93.75 ns. The output pulse-width of limiter amplifier is smaller when receiving ASK '0'. The pulse-width will control the down current source. Because the pulse-width of limiter output is small, if the feed-back pulse-width is wide than the limiter output pulse-width, the integrator voltage will increase. When the integrated voltage exceeds the threshold voltage of quantizer, the output code will turn from '0' to '1'. From the graph, it is obvious that when receiver detect ASK '0', the output digital code of quantizer will have more '0' than '1' in 8 quench period. On the other hand, when receiving ASK '1', the output digital code of quantizer will have more '1' than '0' in 8 quench period.

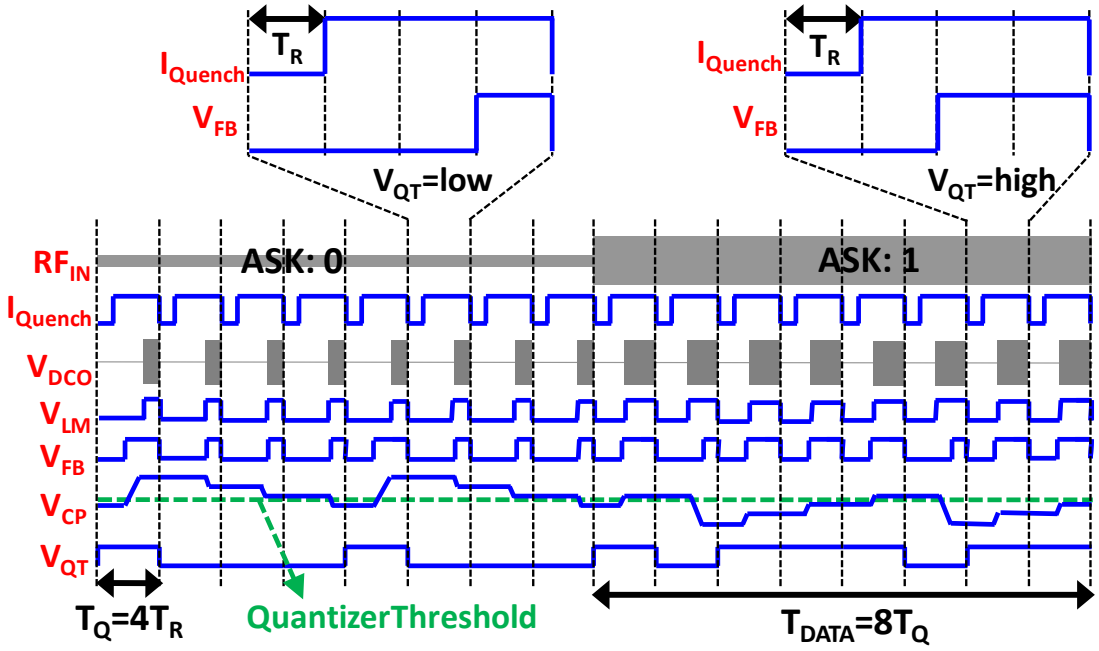


Fig. 4.4 System operation of SR-RX.

4.3.2 Fast Frequency Calibration

For the receiver that is integrated in a wireless biomedical module, the receiver tends to receive the operation command to control the front-end circuit. Hence, the receiver is operated in duty-cycled mode. For the short period of the turn on time, the receiver's start-up time must be as short as possible to reduce the operation duty cycle of receiver. In conventional, the frequency calibration is implemented by a phase-lock loop (PLL) for accurate frequency calibration [19]. However, the current consumption of the PLL will consume too many power when turn on and the turn-on time will be limited by the PLL loop bandwidth. For practical, when the receiver is in receiving mode, the PLL is turned off. The control voltage of the oscillator will leak to the substrate for sub-micron process. Hence, the frequency will drift with an unknown value. Another calibration scheme based on the digital frequency calibration scheme is presented in [20]. However, the calibration time is still limited by the counter

frequency for the resolution and the calibration time consideration. To reduce the calibration time will constrain the calibration resolution.

To improve the power and the calibration time consumption, a fast frequency calibration is proposed [22]. As shown in Fig. 4.5, the calibration scheme comprises a divider by 8, a phase selector, a dual phase detector, a charge-pump, comparator and a SAR logic controller.

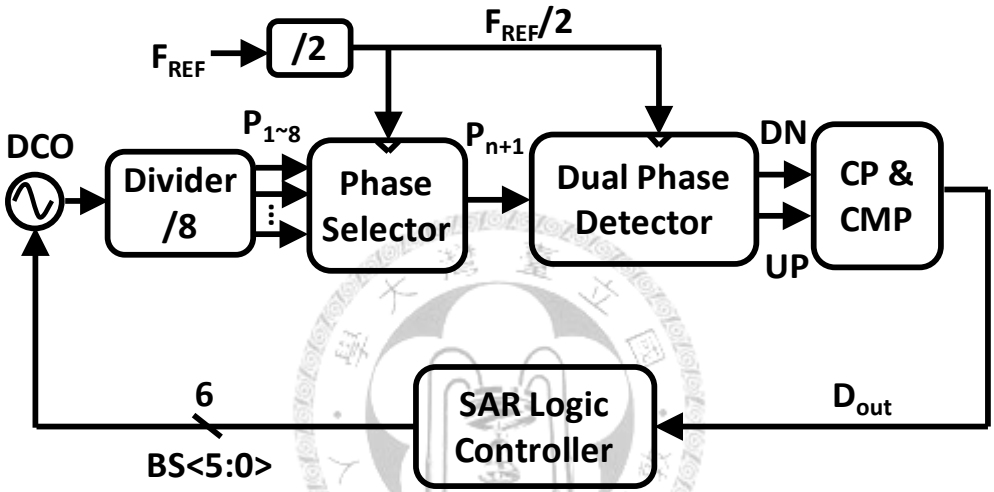


Fig. 4.5 The architecture of fast frequency calibration.

The operation of the fast frequency calibration is based on the SAR principle. Initially, the DCO band selection code (BS<5:0>, SAR Controller output) is set to the mid-level (100000 for the 6-bit codes). As shown in Fig. 4.6(a), the DCO output is divided by 8 to generate 8 phase signals, P_1~P_8. Next, the phase selector selects the phase P_{n+1}, the one that has a rising transition right after the edge of $F_{REF}/2$. ($F_{REF}/2$ is obtained by dividing the FREF by 2, which is ensured a 50% duty-cycle signal.) Then, the dual phase detector takes the rising-edge and falling-edge phase differences between P_{n+1} and $F_{REF}/2$ to generate the UP and DN signals, respectively as shown in Fig. 4.6 (b). The UP/DN signals drive the two charge pumps and generate V_+ and V_-. The comparator (CMP) compare the two signals (V_+ and V_-), and the output indicates

whose frequency of the two, P_{n+1} and $F_{REF}/2$, is higher or lower. If $F_{DCO} > 8F_{REF}$, the PW of $F_{REF}/2$ (period of 1 F_{REF} cycle) is longer than that of the phase signal P_{n+1} (period of 1 F_{DCO} cycle), which means the UP pulse-width is longer than the DN pulse-width. The simplified frequency comparison circuit is shown in Fig. 4.6 (c). Hence, the CMP output will be "1". On the other hand, if $F_{DCO} < 8F_{REF}$, the CMP will generate a "0". The CMP output will be used to update the DCO band selection code through the SAR logic controller. This process repeats until all 6 bits are determined, which can be accomplished within 12 reference cycles which is

$$T_{CAL} = 12T_{ref} = 240ns \tag{4-4}$$

To estimate the calibration resolution of this calibration scheme, we assume that the DCO resolution of the cap-array is Δ_{DCO}. In ideal case which means that the nonideality is ignored in calibration circuits such as current mismatch of charge pump and offset of comparator. Then the calibration frequency error at the final value will be Δ_{DCO} which in our case is about 1.5 MHz/code.

If we take the current mismatch in charge pump Δ_{CP} and the comparator offset $V_{OFF,CMP}$ into consideration, assume Δ_{CP} is 5% mismatch between up and down current source which is 0.5μA; the comparator offset is assume 1 mV. The time domain error between $F_{DCO}/16$ and $F_{REF}/2$ will be calculated as follow

$$25\mu A\frac{\Delta T_{error}}{C_{Load}} = V_{off,CMP} \tag{4-5}$$

Where the ΔT_{error} is modeling the timing error at the charge pump input which can be seen as the PW error of the P_{n+1} caused by the mismatch of the circuit, and C_{Load} is the load capacitor at the output of charge pump which is 300 fF. The only nonideality that causes the calibration error is the input referred offset of the comparator that is

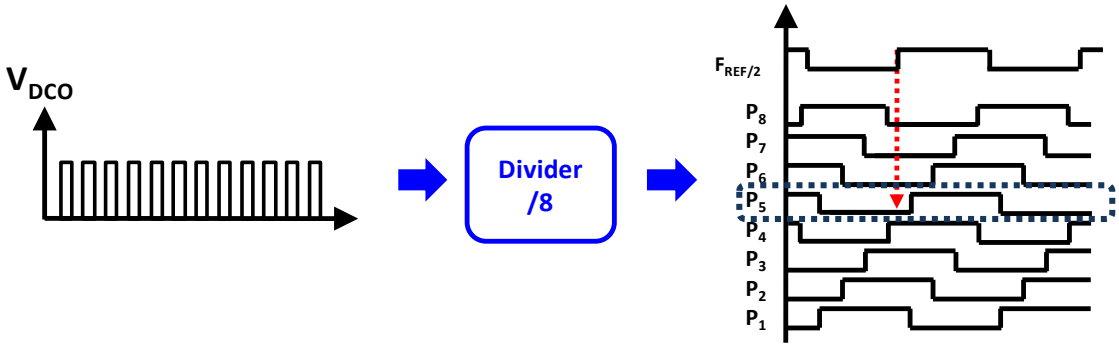
assumed 10 mV for worst case. Then the time error ΔT_{error} can be calculated to be 0.12 ns, which means that the period of the DCO output voltage can be calculated as

$$T_{DCO} = \frac{\left(2T_{REF} + \Delta T_{error}\right)}{16} = 2.5075ns \tag{4-6}$$

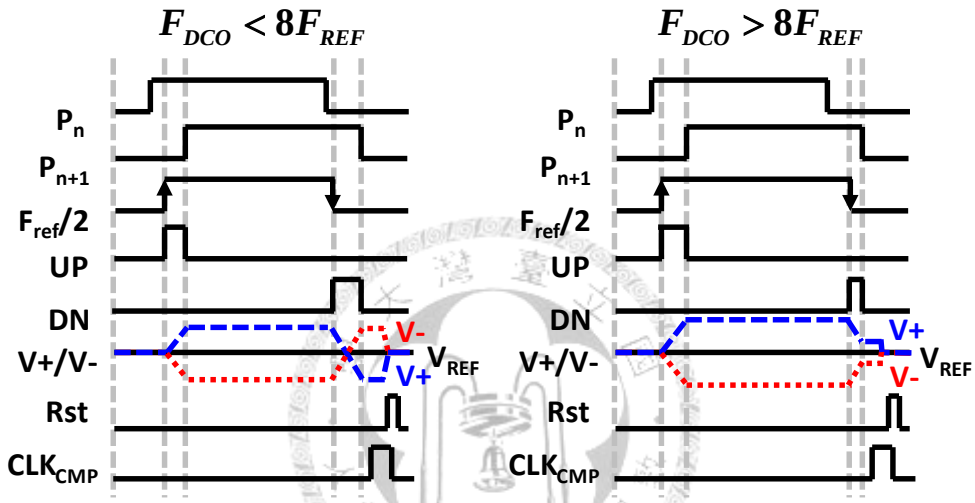
Then adding two nonidealities together for their independency can get the final frequency calibration error which is

$$\Delta f_{error} = \Delta_{DCO} + \left| \left(8F_{REF} - \frac{1}{T_{DCO}} \right) \right| = 2.2MHz \tag{4-7}$$

From the above analysis, the frequency error of the proposed calibration scheme is higher than the conventional calibration ways. However, the super-regenerative receiver suffers from the frequency selectivity because of the low-Q on-chip passive component. Hence the frequency resolution is relaxed. For the application scenario, the start-up time of the receiver is more important than the calibration resolution. Hence, the proposed calibration scheme is making a tradeoff between the resolution and the calibration time.



(a)



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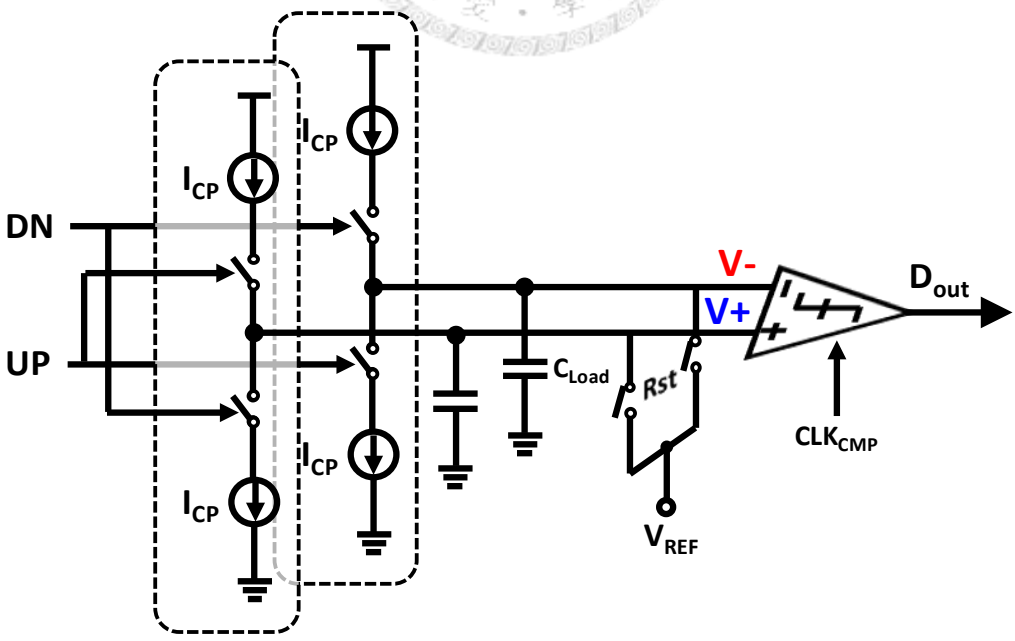


(c)

Fig. 4.6 Operation timing diagram of the proposed architecture.

4.4 Circuit Implementations

The proposed SR-RX is depicted in Fig. 4.1. The quench controller is implemented by Verilog synthesis. The detailed circuit implementations are introduced next with simulation results.

4.4.1 Low Noise Amplifier and Digital-controlled Oscillator

The receiver front-end is composed by a low noise amplifier (LNA) and digital-controlled oscillator (DCO). The circuit architecture is shown in Fig. 4.7. LNA is build by the outer four transistors, two source-degenerative inductors, and a current source I_{LNA}. DCO is designed with two cross-coupled transistor, LC resonator, and current source I_{DCO}.

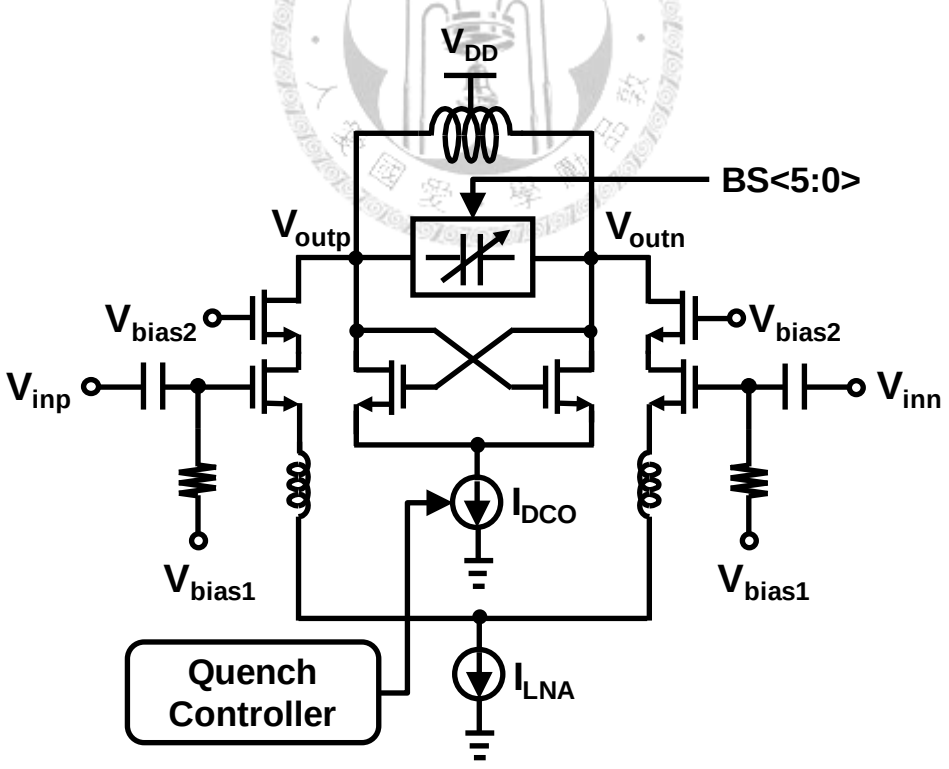


Fig. 4.7 Circuit topology of LNA and DCO.

To improve the isolation between the LNA output and the antenna, the cascode differential-type LNA topology is adopted here. The LNA utilizes on-chip inductor as its source degeneration inductors for impedance matching and noise optimization [23]. The LNA transforms the received input signal into currents which are then injected into the DCO.

The 400-MHz DCO adopts N-core LC-tank oscillator architecture to optimize the current consumption and the input-referred noise of the front-end circuit. The DCO is periodically quenched by controlling the bias current, producing periodically changing output waveform whose envelope depends on the input RF signal level. A 6-bit programmable capacitor array is incorporated to compensate for the center frequency deviation due to process, supply voltage, and temperature variations. The programmable bits are generated by the fast frequency calibration output. In order to widen the input power detection range, the gains of the LNA and DCO are designed to be digitally programmable by controlling the bias currents of the LNA and DCO.

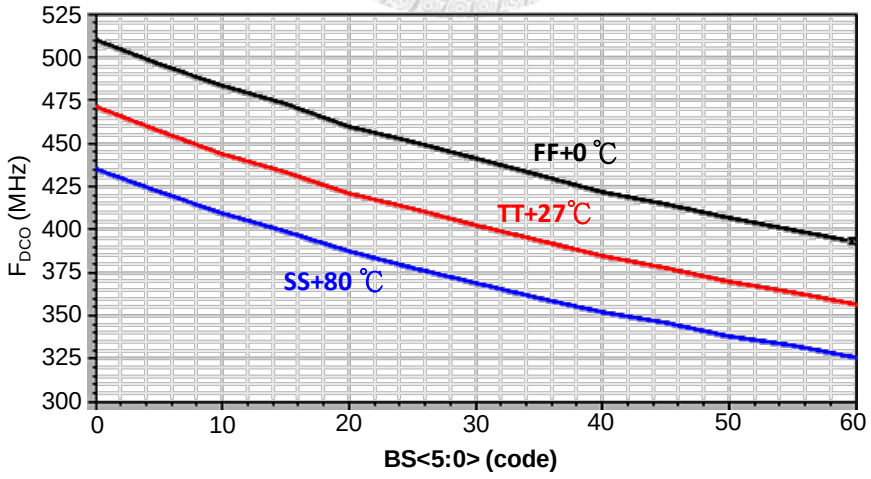


Fig. 4.8 Simulated frequency cover range of DCO.

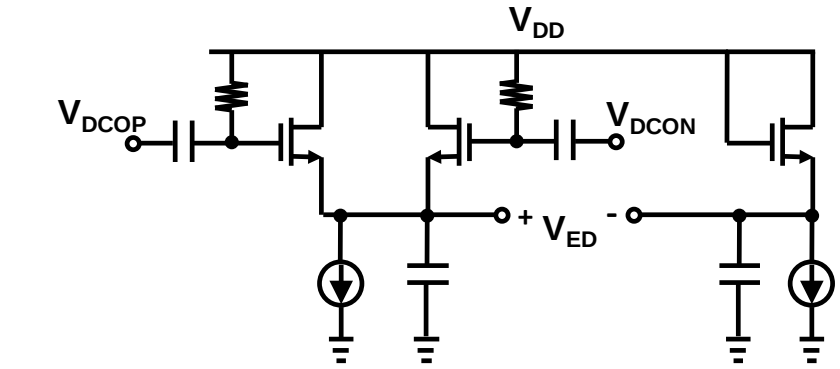
Fig. 4.8 shows the post layout simulation of the frequency covering range of DCO. 400 MHz is covered in three corners to ensure the receiver operation frequency.

4.4.2 Envelope Detector and Limiting Amplifier

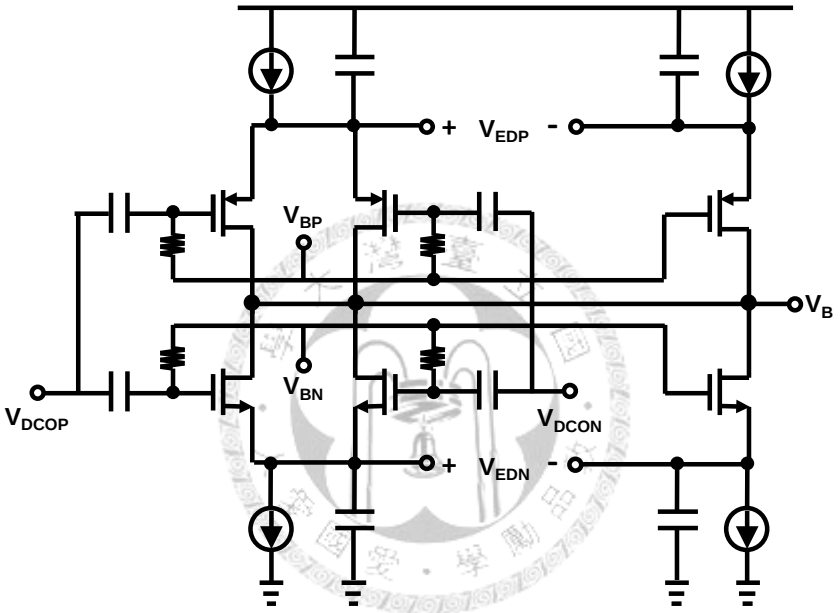
An ED in the SR-RX is employed to rectify the DCO output (V_{DCO}) and extract the envelope content of the signal (V_{ED}). In the conventional pseudo-differential ED circuit [24], as depicted in Fig. 4.9(a), signal V_{ED+} measures the single-ended envelope of the DCO output. However, the periodic quenching operation of the DCO results in a common-mode (of V_{DCO+} and V_{DCO-}) fluctuation, which produces disturbance at signal V_{ED+}. This leads to unwanted glitches at the ED output ($V_{ED} = V_{ED+} - V_{ED-}$) and slows down the circuit response.

In this work, a complementary differential ED architecture is implemented, as shown in Fig. 4.9(b). Other than the NMOS pair which now generates the V_{EDN+}, a complementary PMOS pair is added to the detector to also measure the envelope of the DCO output and generate V_{EDP+}. By taking the detector output as $V_{ED} = (V_{EDP+} - V_{EDP-}) - (V_{EDN+} - V_{EDN-})$, the common-mode fluctuation can be largely removed. Moreover, by re-using the same bias current for the PMOS and NMOS pairs, the detector gain is increased by a factor of 2 without consuming extra current. A minor penalty of the proposed circuit is that the circuit headroom is reduced.

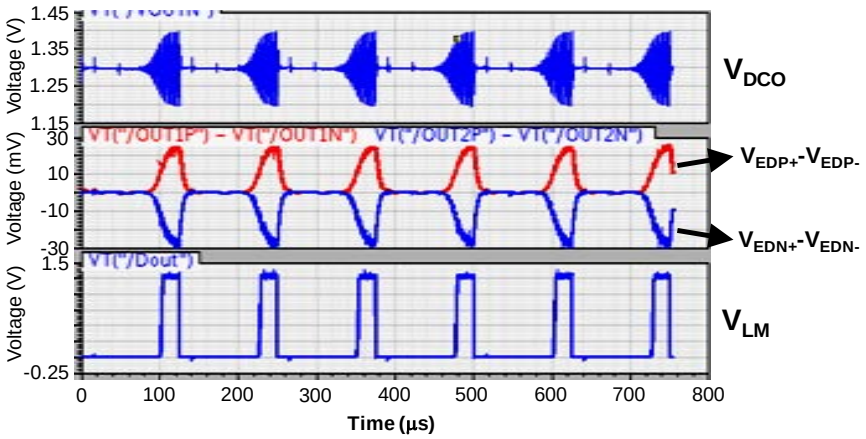
Fig. 4.9 (c) presents the simulated waveforms. The top plot shows the DCO output (V_{DCO}) waveform. The second plot shows the output waveform of the envelope detector. The third plot is the output waveform of the limiting amplifier which pulls the envelope to the rail-to-rail.



(a)



(b)



(c)

Fig. 4.9 (a)Conventional envelope detector (b)Presented envelope detector (c)Simulated waveform of envelope detector.

The limiting amplifier is implemented in Fig. 4.10. A complementary differential architecture is adopted here to interface with the preceding complementary differential ED circuit. The limiting amplifier is designed to be a high gain amplifier with little offset for threshold detection of the output of envelope detector. In this design, the threshold level is programmable through adjusting the bias current, I_N (ranging from 6 μA to 9 μA) and the I_P is 10 μA.

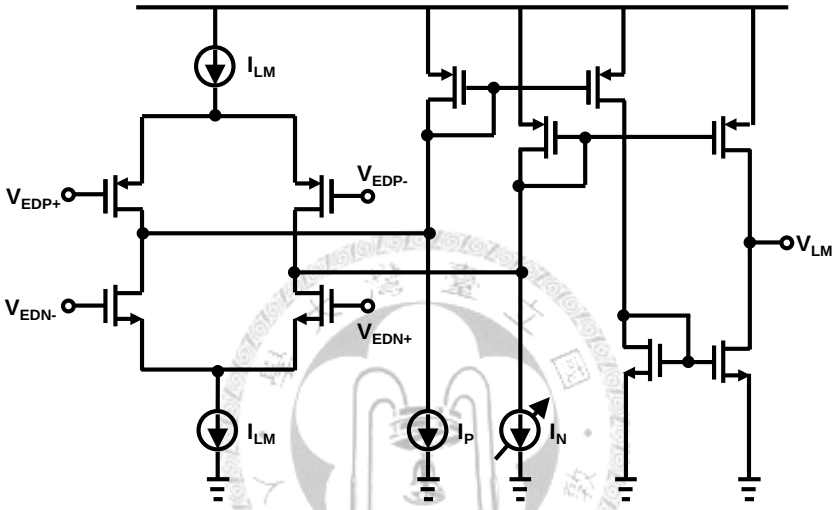


Fig. 4.10 Limiting amplifier.

4.4.3 Charge Pump and Integration Capacitor

The CP converts the PW difference between the feedback pulse-width (V_{FB}) and the V_{LM} into current pulses. These current pulses are then injected into the integration capacitors, C_L. As shown in Fig. 4.11, the CP with the integration capacitors adopt a differential structure, for this topology has a better power-supply-rejection ratio and better suppression of noise coupling from the digital circuits. The common-mode feedback scheme is applied to the CP to set the DC voltage at the CP output, which determines the bias point for the following quantizer. As mentioned previously, the CP noise directly injects into the loop. The CP noise is mainly optimized by increasing the transistor size and reducing the transconductance of the current source devices.

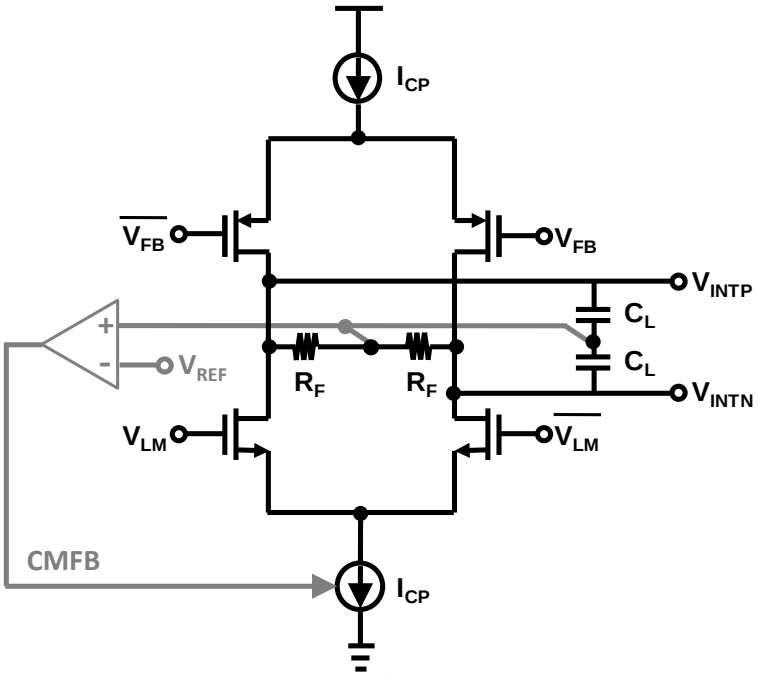
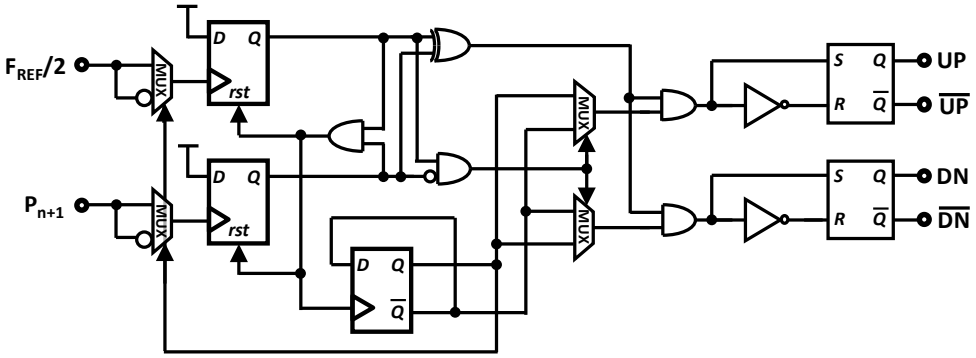


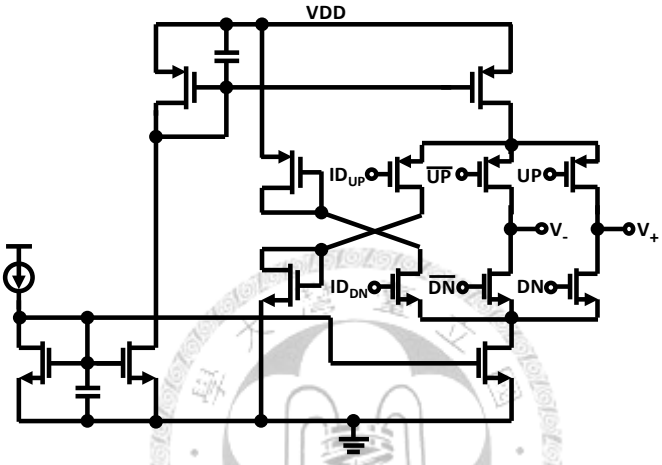
Fig. 4.11 Charge pump and integration capacitor.

4.4.4 Circuits Implementations in Fast Frequency Calibration

The architecture of the fast frequency calibration is shown in Fig. 4.5. The dual phase detector to generate the UP and DN signal as the inputs of charge pump is shown is Fig. 4.12 (a). The charge pump shown in Fig. 4.12 (b) is similar as shown before. However the CMFB is eliminated because the output voltage of the CP will be reset to the reference voltage each frequency comparison period. There is no integration operation as the ΔΣ-PWD. The simulated output waveform is shown in Fig. 4.12 (c). The band selection (BS) is set to the specific value to ensure that the DCO frequency is close to the 8 times of reference clock frequency. The total simulated calibration time is 240 ns which is same as the calculated value.



(a)



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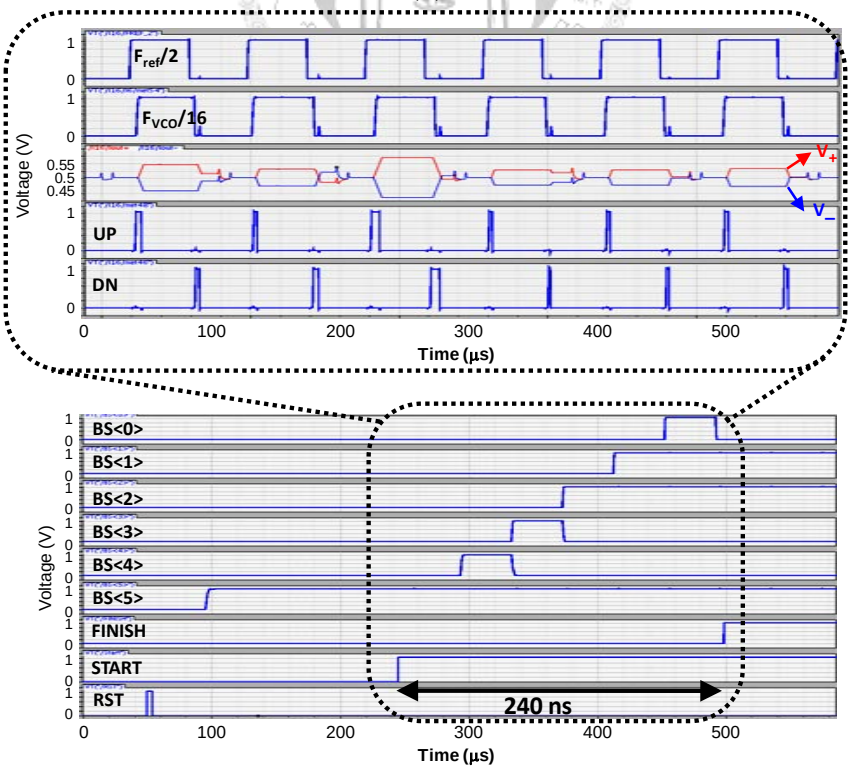


(c)

Fig. 4.12 (a) Dual phase detector (b) Charge pump (c) Operation waveform.

4.5 Measurement Setup and Experimental Results

This section presents the testing environment, including the instruments and component circuits on the device under test (DUT) board. The experimental results of the proposed circuit will also be presented.

4.5.1 Measurement Setup

Fig. 4.13 shows the measurement environment of the SR-RX. The DC supply is generated by a LT3020 LDO to lower the supply noise from external 60-Hz noise. The reference clock is generated by a function generator. The SIPO controller is generated by a printer port of a PC to control the bias current and the band selection of DCO from external.

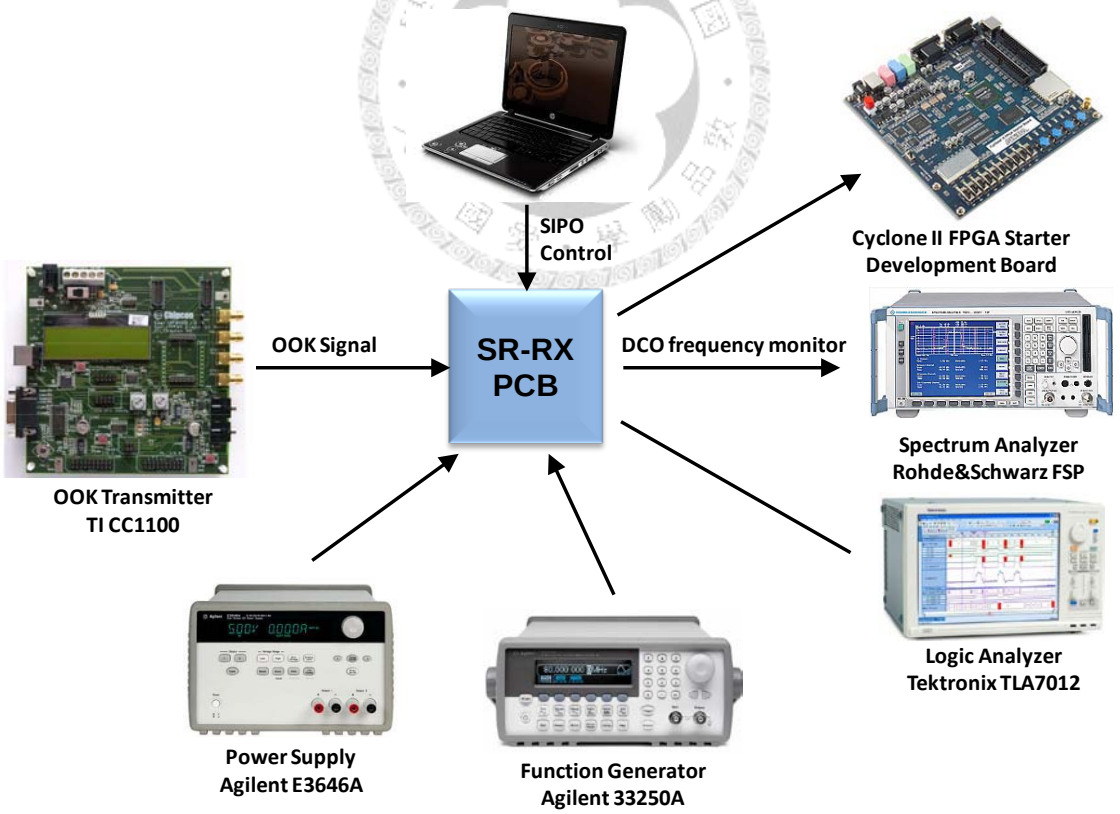


Fig. 4.13 Measurement setup.

The spectrum analyzer is used to measure the output frequency of DCO to verify the function of fast frequency calibration. The logic analyzer is used to analyze the output spectrum of ΔΣ-PWD. FPGA board is used to implement the decimation filter of the ΔΣ-PWD and demodulate the received data and compute the bit error rate (BER) of the receiver.

4.5.2 Device-Under-Test Print-Circuit Board

The receiver is designed in TSMC 1P6M 0.18-μm CMOS process. The raw die is directly mounted on print-circuit-board (PCB). Including the ESD-protection pads, this chip occupies an area of 1.5 mm × 1.55 mm. Because the system needs a high-Q inductor for better sensitivity, the area of the inductor is quite large. Except the inductor, the core area is only about 0.5 mm^2. The chip micrograph is shown in Fig. 4.14.

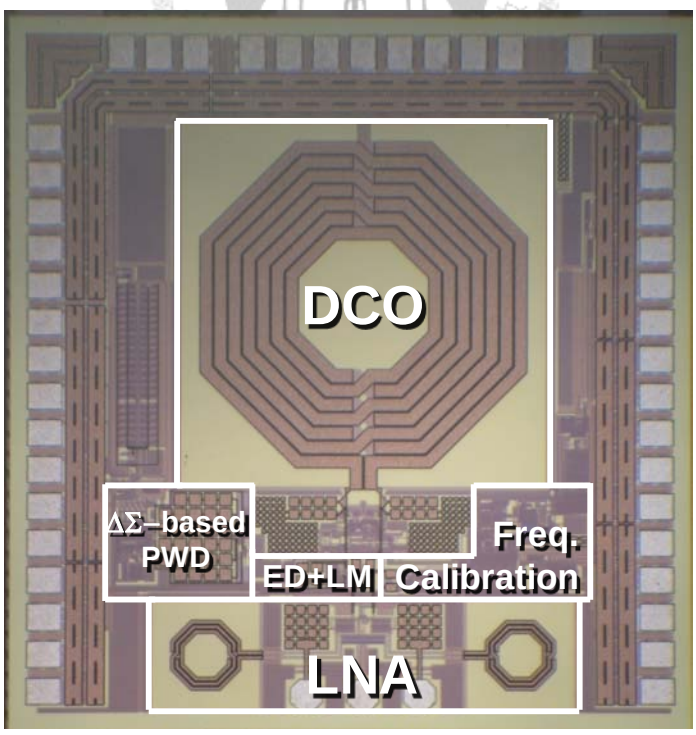


Fig. 4.14 Chip micrograph

A PCB is fabricated in order to test the SR-RX, and the PCB for the DUT is shown in Fig. 4.15. There are 6 power domains that is supplied by different LDO components: analog, digital, and 3V which is used for FPGA board. The 3-bit SIPO control signals are connected to the signal board. The data and clock are also connected to pins and sent to the chip. The input of the LNA is connected by a transformer and a matching network before receiving the signal from antenna. The output of ΔΣ-PWD will connect to the logic analyzer (LA) for spectrum analysis or connect to FPGA for demodulation.

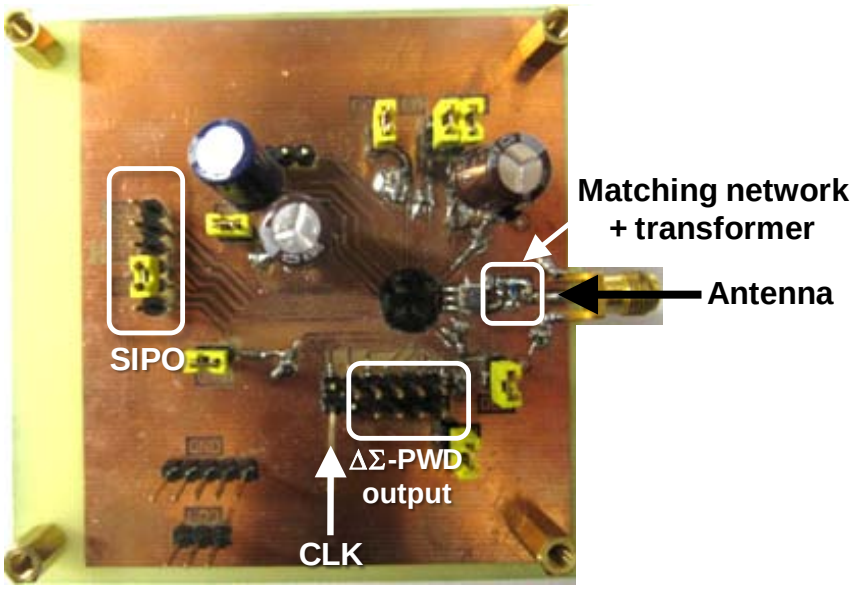


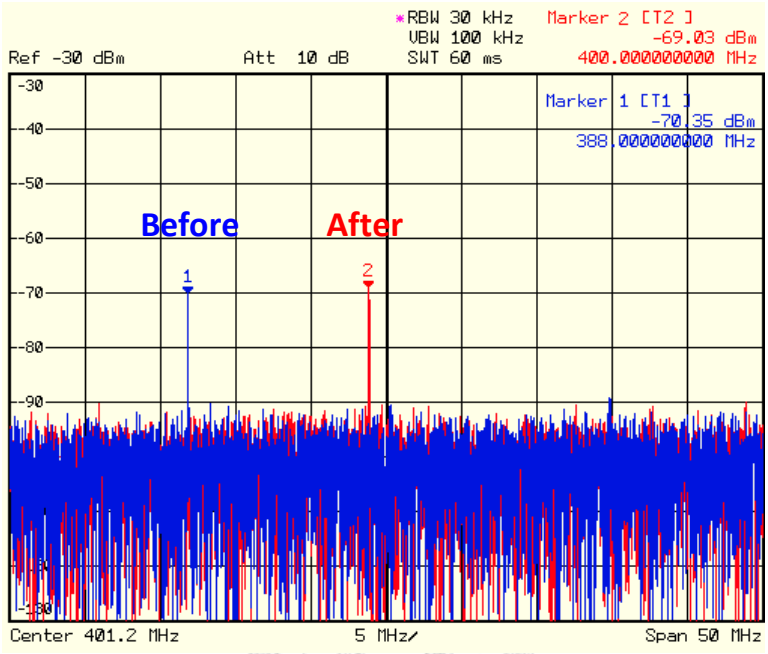
Fig. 4.15 PCB for SR-RX testing

4.5.3 Experimental Results

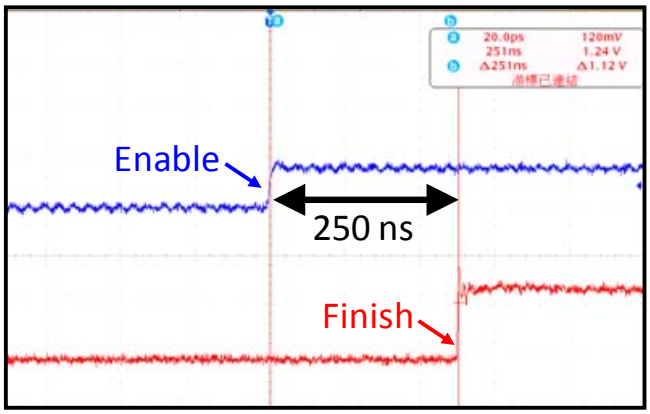
The proposed SR-RX incorporating the ΔΣ-PWD and the fast frequency calibration dissipates 1.37 mA from a 1-V supply. The RX front-end which employs an on-chip inductor (Q~7) draws 900 μA, while the PWD only draws 60 μA.

To examine the effect of frequency calibration, a spectrum analyzer is used to monitor the LNA input to observe the leakage signal from the DCO. As shown in Fig.

4.16 (a), before calibration, the initial oscillation frequency is at 388 MHz. After the frequency calibration, the DCO frequency is moved to near the desired 400 MHz. The reference frequency is chosen at 50 MHz. Fig. 4.16 (b) shows the calibration time, which is about 250 ns. This is close to the predicted 12 cycles (240 ns). This calibration time is less than the time span for transmitting one-bit data at 1 Mbps (1μs).



(a)



(b)

Fig. 4.16 (a) Measured DCO output frequency, before and after frequency calibration. (b) Measured calibration time.

Fig. 4.17 shows the measure spectrum at the ΔΣ-PWD output. An external transmitter (from CC1100) sends OOK signal with periodic 101010 data with output power of -50 dBm to the RX chip. The ΔΣ-PWD output bit stream is recorded by a logic analyzer and converted to the output spectrum. For an OSR of 8, the SNR is around 10.8 dB, estimated with a bandwidth of 500 kHz. The idle tone in the MATLAB model simulation is eliminated because of the noise dithering of the pulse-width at the output of limiting amplifier. Hence, the idle tone in the 1st-order DSM can be reduced by noise dithering. However, the in-band noise floor is increased.

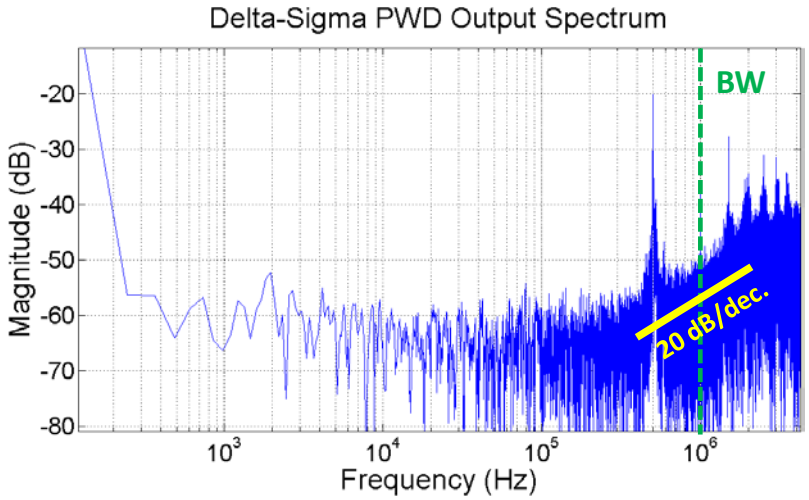
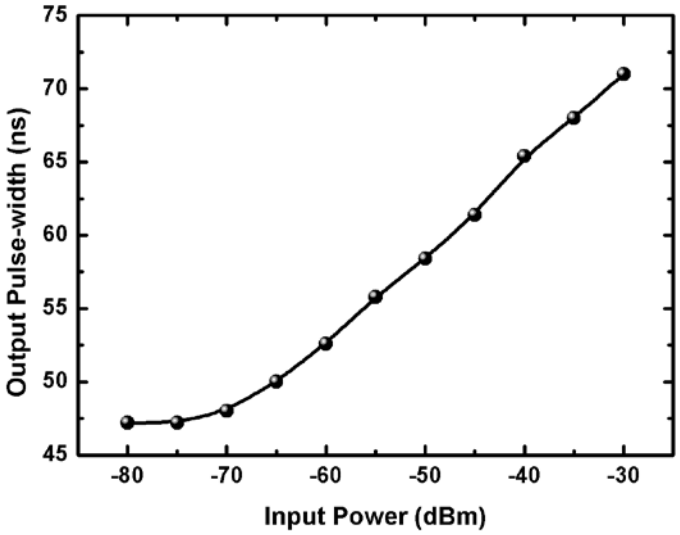
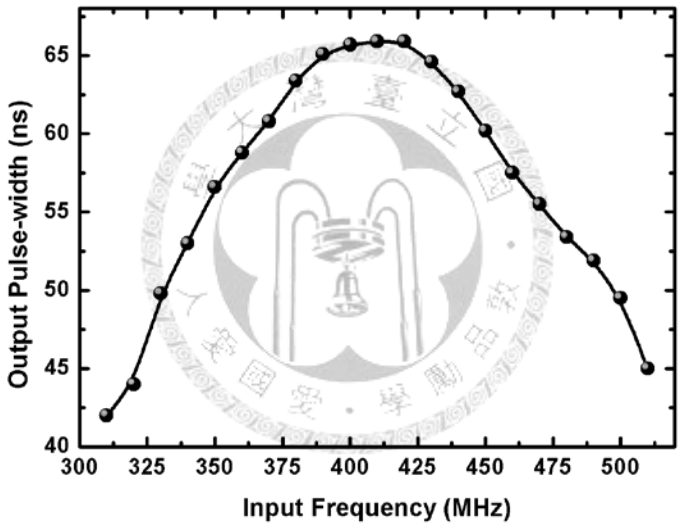


Fig. 4.17 Spectrum at the ΔΣ-PWD output.

Fig. 4.18(a) shows the recorded PW at the limiting amplifier output versus the input power (P_{in}). From the graph, it is observed that when the input power is larger than -75 dBm, the output PW is increased with input power. Fig. 4.18(b) shows the measured frequency selectivity profile. The 3-dB bandwidth is around 13 MHz. The frequency selectivity is limited by the low-Q passive component (Q~7 for on-chip inductor). To enhance the frequency selectivity, off-chip high-Q inductors or Q-enhancement mechanism can be considered.



(a)



(b)

Fig. 4.18 (a) Measured output pulse-width vs. P_{IN} (b) Measured output pulse-width vs. input frequency.

To demonstrate the overall RX operation, the output over-sampled code is decimated to extract the baseband data. Fig. 4.19 shows the transmitted and received data waveforms at 1-Mbps data rate. The transmitted data are sent by the CC1100, and are received/demodulated by the proposed RX with the ΔΣ-PWD. As shown in Fig. 4.19, the proposed SR-RX functions correctly.

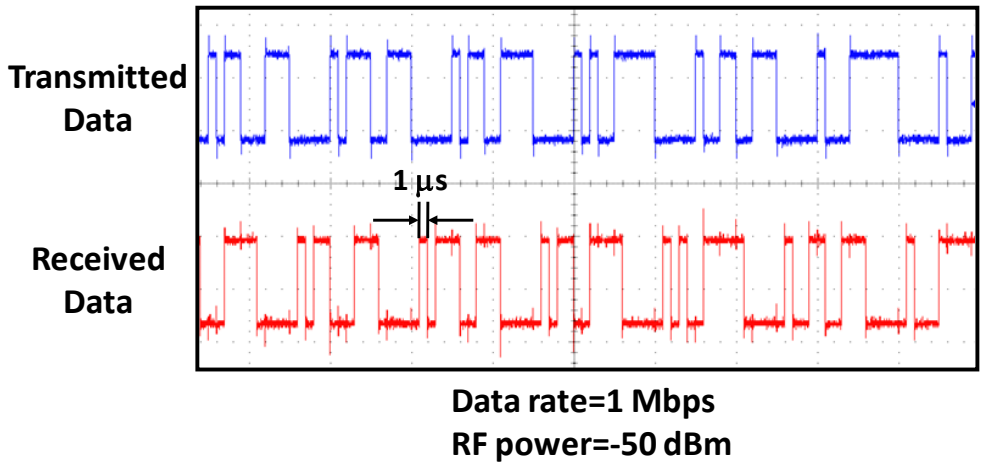


Fig. 4.19 Transmitted and received data at 1 Mbps.

Fig. 4.20 shows the measured bit error rate of the receiver. The FPGA send a PRBS to CC1100 and transmit to the proposed receiver. And the receiver demodulates the bit stream by FPGA and compared with the transmitted waveform. The number of bits for comparison is 1024. For BER less than 0.1%, the comparison will have 0 or 1 error bit when the BER is less than 0.1%.

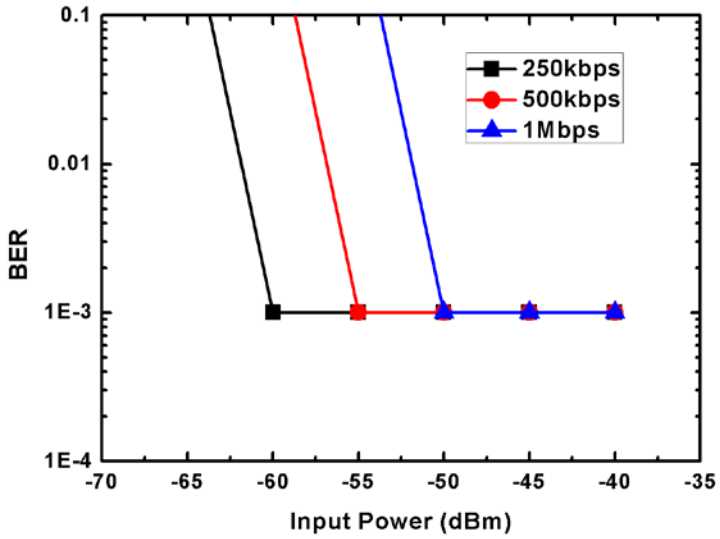


Fig. 4.20 Measured bit error rate.

Table 3.1 shows the measured result compared with the original design target. Table 3.2 shows the comparison table with the published papers.

Table 4-2 Performance Summary

	Design Target	Measurement Result
Process	TSMC 0.18-μm CMOS	TSMC 0.18-μm CMOS
Supply Voltage	1 V	1 V
Data Rate	1 MHz	1 Mbps
Center Frequency	400 Mbps	400 MHz
Seneitivity	<-75 dBm	-50 dBm
Modulation	ASK/OOK	OOK
Power Consumption	< 1.5 mW	1.37 mW
Energy Efficiency	< 1.5 nJ/b	1.37 nJ/b

Table 4-3 Comparison table

	This work	07'JSSC [19]	09'JSSC [18]	10'JSSC [21]
Process	**0.18 μm**	0.13 μm	0.18 μm	0.18 μm
Supply	**1 V**	1.2 V	1 V	1.3 V
Operation Freq.	**400 MHz**	2.4 GHz	400 MHz	400 MHz
Modulation	**ASK/OOK**	OOK	OOK	ASK/OOK
Power	**1.37 mW**	3.3 mW	0.35 mW	0.9 mW
Energy/bit	**1.37 nJ/b**	6.7 nJ/b	2.9 nJ/b	5.8 nJ/b
Data Rate	**1 Mbps**	500 kbps	120 kbps	156 kbps
Sensitivity	**-50 dBm**	-80 dBm	-93 dBm	-80 dBm
PW Detector	**ΔΣ-PWD**	Over- sample	Over- sample	ΔΣ-PWD
DCO Resonator	**On-chip**	On-chip	PCB	On-chip
Freq. Cal. Time	**250 ns**	83 μs	NA	1.5 μs

Chapter 5
Conclusions and Future Works

5.1 Conclusions

This thesis introduces two systems blocks for wireless piezoresistive sensing applications. First, an oscillator-based self-calibrated front-end circuit is presented with high sensitivity to the resistance variation. The second system is a super-regenerative receiver with ΔΣ-PWD and fast frequency calibration.

In the front-end circuit design, an oscillator transfers the resistance information into frequency domain and a mixer down converts the frequency to lower frequency for demodulation. The down-conversion operation means the amplification in time domain to enhance the system sensitivity to the resistance variation.

In the receiver design, the proposed super-regenerative receiver adopts the ΔΣ-PWD to demodulate the received signal to improve the limitation of the conventional demodulator. A fast frequency calibration is also proposed to regulate the oscillation frequency to the specific frequency band with the SAR algorithm to finish the calibration in 12 reference cycles.

5.2 Future Works

The all digital operation is required in down-conversion system for the front-end circuit. It will consume too much power to pull the oscillation output signal to full swing. Hence, the power consumption can be reduced by implement the passive mixer

with analog switches which can operate in very low power consumption. And the dynamic range of mixer can be increased.

The DCO oscillation frequency is drifted when receiving data in reality for a long while. Hence, instead of the foreground calibration as shown in this thesis, the back-ground calibration should be implemented in the SR-RX to prevent the operation frequency drifting for temperature or voltage variation. The sensitivity of the receiver can be more enhanced with other mechanism such as Q-enhancement technique.

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